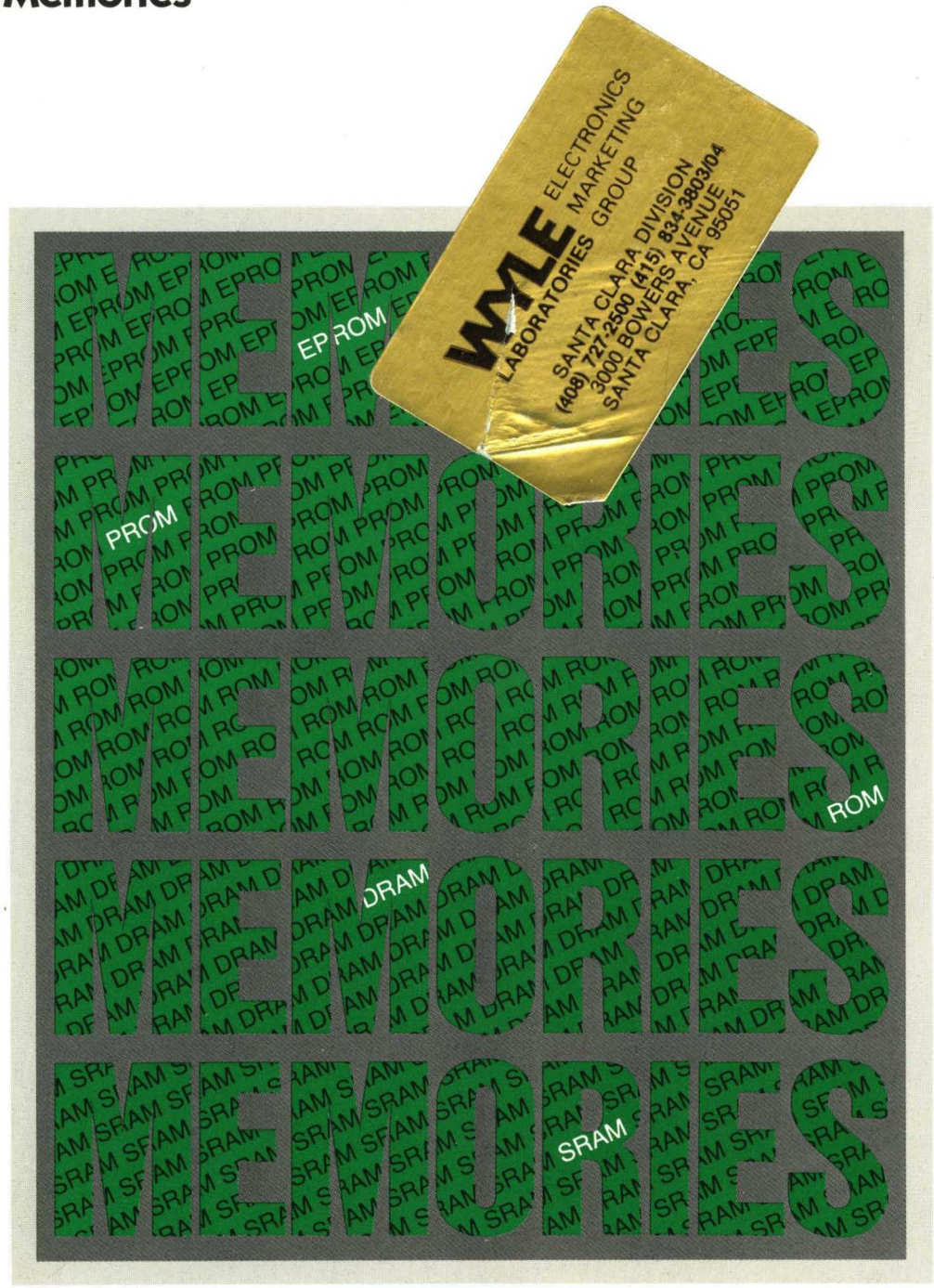
# Bipolar/MOS Memories

1984 Data Book






ADVANCED MICRO DEVICES

1

# Advanced Micro Devices

# Bipolar/MOS Memories Data Book

The International Standard of Quality guarantees the AQL on all electrical parameters, AC and DC, over the entire operating range.



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# NUMERICAL DEVICE INDEX (Cont.)

## NUMERICAL DEVICE INDEX (Cont.)

# Bipolar PROM

## Functional Index and Selection Guide

Listed according to organization and access time.

| Part Number | Organization | Access Time COM'L/MIL Max | $I_{CC}$ COM'L/MIL Max | Output | Number of Pins | Packages | Page No. |
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| Am27S18 | 32 x 8 | 40/50 | 115/115 | OC | 16 | D,P,F,L | 2-24 |
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| Am27LS19[1] | 32 x 8 | 50/65 | 80/80 | 3S | 16 | D,P,F,L | 2-24 |
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| Am27S12A | 512 x 4 | 30/40 | 130/130 | OC | 16 | D,P,F,L | 2-13 |
| Am27S13A | 512 x 4 | 30/40 | 130/130 | 3S | 16 | D,P,F,L | 2-13 |
| Am27S12 | 512 x 4 | 50/60 | 130/130 | OC | 16 | D,P,F,L | 2-13 |
| Am27S13 | 512 x 4 | 50/60 | 130/130 | 3S | 16 | D,P,F,L | 2-13 |
| Am27S25 | 512 x 8 | N.A.[2]/N.A.[2] | 185/185 | 3S | 24 | D,P,F,L | 2-34 |
| Am27S25A | 512 x 8 | N/A.[4]/N.A.[4] | 185/185 | 3S | 24 | D,P,F,L | 2-34 |
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| Am27S29 | 512 x 8 | 55/70 | 160/160 | 3S | 20 | D,P.L | 2-46 |
| Am27S30 | 512 x 8 | 55/70 | 175/175 | OC | 24 | D,P,F,L | 2-51 |
| Am27S31 | 512 x 8 | 55/70 | 175/175 | 3S | 24 | D,P,F,L | 2-51 |
| Am27S15 | 512 x 8 | 60/90 | 175/185 | 3S | 24 | D,P,F,L | 2-18 |
| Am27S32A | 1024 x 4 | 35/45 | 140/145 | OC | 18 | D,P,F,L | 2-56 |
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| Am27S35A | 1024 x 8 | N.A.[4]/N.A.[4] | 185 | 3S | 24 | D,P,F,L | 2-61 |
| Am27S35 | 1024 x 8 | N.A.[2]/N.A.[2] | 185 | 3S | 24 | D,P,F,L | 2-61 |
| Am27S37A | 1024 x 8 | N.A.[4]/N.A.[4] | 185 | 3S | 24 | D,P,F,L | 2-61 |
| Am27S37 | 1024 x 8 | N.A.[2]/N.A.[2] | 185 | 3S | 24 | D,P,F,L | 2-61 |
| Am27S180A | 1024 x 8 | 35/50 | 185/185 | OC | 24 | D,P,F,L | 2-122 |
| Am27S181A | 1024 x 8 | 35/50 | 185/185 | 3S | 24 | D,P,F,L | 2-122 |
| Am27S280A | 1024 x 8 | 35/50 | 185/185 | OC | 24 | D,P,F,L | 2-122 |
| Am27S281A | 1024 x 8 | 35/50 | 185/185 | 3S | 24 | D,P,F,L | 2-122 |
| Am27S180 | 1024 x 8 | 60/80 | 185/185 | OC | 24 | D,P,F,L | 2-122 |
| Am27S181 | 1024 x 8 | 60/80 | 185/185 | 3S | 24 | D,P,F,L | 2-122 |
| Am27S280 | 1024 x 8 | 60/80 | 185/185 | OC | 24 | D,P,F,L | 2-122 |
| Am27S281 | 1024 x 8 | 60/80 | 185/185 | 3S | 24 | D,P,F,L | 2-122 |
| Am27PS181 | 1024 x 8 | | | 3S | 24 | D,P,F,L | 2-122 |
| Am27PS281 | 1024 x 8 | | | 3S | 24 | D,P,F,L | 2-122 |

## BIPOLAR PROM (Cont.)

| Part Number | Organization | Access Time COM'L/MIL Max | $I_{CC}$ COM'L/MIL Max | Output | Number of Pins | Packages | Page No. |
|---|---|---|---|---|---|---|---|
| Am27S75A | 2048 x 4 | N.A. | 185/185 | 3S | 24 | D,P | 2-99 |
| Am27S75 | 2048 x 4 | N.A. | 185/185 | 3S | 24 | D,P | 2-99 |
| Am27S184A | 2048 x 4 | 35/45 | 150/150 | OC | 18 | D,P,F,L | 2-128 |
| Am27S185A | 2048 x 4 | 35/45 | 150/150 | 3S | 18 | D,P,F,L | 2-128 |
| Am27S184 | 2048 x 4 | 50/55 | 150/150 | OC | 18 | D,P,F,L | 2-128 |
| Am27S185 | 2048 x 4 | 50/55 | 150/150 | 3S | 18 | D,P,F,L | 2-128 |
| Am27LS184 | 2048 x 4 | 60/65 | 120/125 | OC | 18 | D,P,F,L | 2-128 |
| Am27LS185 | 2048 x 4 | 60/65 | 120/125 | 3S | 18 | D,P,F,L | 2-128 |
| Am27PS185 | 2048 x 4 | 60/65 | 150/75[5] | 3S | 18 | D,P,F,L | 2-128 |
| Am27S45A | 2048 x 8 | N.A.[4] | 185/185 | 3S | 24 | D,P,L | 2-78 |
| Am27S45 | 2048 x 8 | N.A.[2] | 185/185 | 3S | 24 | D,P,L | 2-78 |
| Am27S47A | 2048 x 8 | N.A.[4] | 185/185 | 3S | 24 | D,P,L | 2-78 |
| Am27S47 | 2048 x 8 | N.A.[2] | 185/185 | 3S | 24 | D,P,L | 2-78 |
| Am27S190A | 2048 x 8 | 35/50 | 185/185 | OC | 24 | D,P,F,L | 2-134 |
| Am27S191A | 2048 x 8 | 35/50 | 185/185 | 3S | 24 | D,P,F,L | 2-134 |
| Am27S290A | 2048 x 8 | 35/50 | 185/185 | OC | 24 | D,P,F,L | 2-134 |
| Am27S291A | 2048 x 8 | 35/50 | 185/185 | 3S | 24 | D,P,F,L | 2-134 |
| Am27S190 | 2048 x 8 | 50/65 | 185/185 | OC | 24 | D,P,F,L | 2-134 |
| Am27S191 | 2048 x 8 | 50/65 | 185/185 | 3S | 24 | D,P,F,L | 2-134 |
| Am27S290 | 2048 x 8 | 50/65 | 185/185 | OC | 24 | D,P,F,L | 2-134 |
| Am27S291 | 2048 x 8 | 50/65 | 185/185 | 3S | 24 | D,P,F,L | 2-134 |
| Am27PS191 | 2048 x 8 | 65/75 | 185/80[5] | 3S | 24 | D,P,F,L | 2-134 |
| Am27PS291 | 2048 x 8 | 65/75 | 185/80[5] | 3S | 24 | D,P,F,L | 2-134 |
| Am27S85A | 4096 x 4 | N.A. | 185/185 | 3S | 24 | D,P | 2-110 |
| Am27S85 | 4096 x 4 | N.A. | 185/185 | 3S | 24 | D,P | 2-110 |
| Am27S40A | 4096 x 4 | 35/50 | 165/170 | OC | 20 | D,P,L | 2-67 |
| Am27S41A | 4096 x 4 | 35/50 | 165/170 | 3S | 20 | D,P,L | 2-67 |
| Am27S40 | 4096 x 4 | 50/65 | 165/170 | OC | 20 | D,P,L | 2-67 |
| Am27S41 | 4096 x 4 | 50/65 | 165/170 | 3S | 20 | D,P,L | 2-67 |
| Am27PS41 | 4096 x 4 | 50/65 | 170/85[5] | 3S | 20 | D,P,L | 2-67 |
| Am27S43A | 4096 x 8 | N.A. | 185 | 3S | 24 | D,P,F,L | 2-73 |
| Am27S43 | 4096 x 8 | N.A. | 185 | 3S | 24 | D,P,F,L | 2-73 |
| Am27PS43 | 4096 x 8 | N.A. | N.A. | 3S | 24 | D,P,F,L | 2-73 |
| Am27S49A | 8192 x 8 | 40/55 | 190/190 | 3S | 24 | D,P,L | 2-84 |
| Am27S49 | 8192 x 8 | 55/65 | 190/190 | 3S | 24 | D,P,L | 2-84 |

Notes: 1. Replaces Am27LS08/09
2. Contains built-in pipeline registers: nominal address to clock setup time = 35ns (typ), clock to output = 20ns (typ).
3. 300-mil lateral pin spacing.
4. Contains built-in pipeline registers: nominal address to clock setup time = 25ns (typ), clock to output = 15ns (typ).
5. $I_{CC}$ are power up and power down current limits respectively.

# Bipolar Memory RAM

Functional Index and Selection Guide

**BIPOLAR ECL RAM**
Listed according to organization and access time.

| Part Number | Organization | Access Time COM'L/MIL Max | $I_{EE}$ COM'L/MIL Max | ECL Series | Number of Pins | Packages | Page No. |
|---|---|---|---|---|---|---|---|
| Am10415SA | 1024 x 1 | 15/20 | -150/-165 | 10K | 16 | D,P,F,L | 3-40 |
| Am100415A | 1024 x 1 | 15/- | -150/- | 100K | 16 | D,P,F,L | 3-47 |
| Am10415A | 1024 x 1 | 20/25 | -150/-165 | 10K | 16 | D,P,F,L | 3-40 |
| Am100415 | 1024 x 1 | 20/- | -150/- | 100K | 16 | D,P,F,L | 3-47 |
| Am10415 | 1024 x 1 | 35/40 | -150/-165 | 10K | 16 | D,P,F,L | 3-40 |
| Am10474A | 1024 x 4 | 15/20 | -230/-255 | 10K | 24 | D,F,L | 3-52 |
| Am100474A | 1024 x 4 | 15/- | -230/- | 100K | 24 | D,F,L | 3-54 |
| Am10474 | 1024 x 4 | 25/30 | -230/-220 | 10K | 24 | D,F,L | 3-52 |
| Am100474 | 1024 x 4 | 25/- | -200/- | 100K | 24 | D,F,L | 3-54 |
| Am10470SA | 4096 x 1 | 15/20 | -230/-255 | 10K | 18 | D,F[1],L | 3-56 |
| Am100470SA | 4096 x 1 | 15/- | -230/- | 100K | 18 | D,F[1],L | 3-63 |
| Am10470A | 4096 x 1 | 25/30 | -200/-220 | 10K | 18 | D,F[1],L | 3-56 |
| Am100470A | 4096 x 1 | 25/- | -195/- | 100K | 18 | D,F[1],L | 3-63 |
| Am10470 | 4096 x 1 | 35/40 | -200/-220 | 10K | 18 | D,F[1],L | 3-56 |
| Am100470 | 4096 x 1 | 35/- | -195/- | 100K | 18 | D,F[1],L | 3-63 |

Note: 1. For flat package consult factory.

**BIPOLAR TTL RAM**
Listed according to organization and access time.

| Part Number | Organization | Access Time COM'L/MIL Max | $I_{CC}$ COM'L/MIL Max | Output | Number of Pins | Packages (Note 1) | Page No. |
|---|---|---|---|---|---|---|---|
| Am27S02A | 16 x 4 | 25/30 | 100/105 | OC | 16 | D,P,F,L | 3-23 |
| Am27S03A | 16 x 4 | 25/30 | 100/105 | 3S | 16 | D,P,F,L | 3-23 |
| Am27S06A | 16 x 4 | 25/30 | 100/105 | OC | 16 | D,P,F,L | 3-17 |
| Am27S07A | 16 x 4 | 25/30 | 100/105 | 3S | 16 | D,P,F,L | 3-17 |
| Am29705A | 16 x 4 | 28/30 | 210/210 | 3S | 28 | D,P,F,L | 3-1 |
| Am27S02 | 16 x 4 | 35/50 | 105/105 | OC | 16 | D,P,F,L | 3-23 |
| Am27S03 | 16 x 4 | 35/50 | 125/125 | 3S | 16 | D,P,F,L | 3-23 |
| Am27S06 | 16 x 4 | 35/50 | 100/105 | OC | 16 | D,P,F,L | 3-17 |
| Am27S07 | 16 x 4 | 35/50 | 100/105 | 3S | 16 | D,P,F,L | 3-17 |
| Am3101A | 16 x 4 | 35/50 | 100/105 | OC | 16 | D,P,F,L | 3-68 |
| Am3101-1 | 16 x 4 | 35/50 | 100/105 | OC | 16 | D,P,F,L | 3-68 |
| Am74/5489-1 | 16 x 4 | 35/50 | 100/105 | OC | 16 | D,P,F,L | 3-68 |
| Am74/54S189 | 16 x 4 | 35/50 | 125/125 | 3S | 16 | D,P,F,L | 3-68 |
| Am74/54S289 | 16 x 4 | 35/50 | 105/105 | OC | 16 | D,P,F,L | 3-68 |
| Am74/5489 | 16 x 4 | 50/60 | 100/105 | OC | 16 | D,P,F,L | 3-68 |
| Am3101 | 16 x 4 | 50/60 | 100/105 | OC | 16 | D,P,F,L | 3-68 |
| Am27LS02 | 16 x 4 | 55/65 | 35/38 | OC | 16 | D,P,F,L | 3-23 |
| Am27LS03 | 16 x 4 | 55/65 | 35/38 | 3S | 16 | D,P,F,L | 3-23 |
| Am27LS06 | 16 x 4 | 55/65 | 35/38 | OC | 16 | D,P,F,L | 3-17 |
| Am27LS07 | 16 x 4 | 55/65 | 35/38 | 3S | 16 | D,P,F,L | 3-17 |
| Am31L01A | 16 x 4 | 55/65 | 35/38 | OC | 16 | D,P,F,L | 3-68 |
| Am31L01 | 16 x 4 | 80/90 | 35/38 | OC | 16 | D,P,F,L | 3-68 |
| Am27LS00A | 256 x 1 | 35/45 | 115/115 | 3S | 16 | D,P,F,L | 3-29 |

## BIPOLAR TTL RAM (Cont.)

| Part Number | Organization | Access Time COM'L/MIL Max | $I_{CC}$ COM'L/MIL Max | Output | Number of Pins | Packages (Note 1) | Page No. |
|---|---|---|---|---|---|---|---|
| Am27LS01A | 256 x 1 | 35/45 | 115/115 | OC | 16 | D,P,F,L | 3-29 |
| Am27LS00-1A | 256 x 1 | 35/45 | 115/115 | 3S | 16 | D,P,F,L | 3-29 |
| Am27LS01-1A | 256 x 1 | 35/45 | 115/115 | OC | 16 | D,P,F,L | 3-29 |
| Am27LS00 | 256 x 1 | 45/55 | 70/70 | 3S | 16 | D,P,F,L | 3-29 |
| Am27LS01 | 256 x 1 | 45/55 | 70/70 | OC | 16 | D,P,F,L | 3-29 |
| Am27LS00-1 | 256 x 1 | 45/55 | 70/70 | 3S | 16 | D,P,F,L | 3-29 |
| Am27LS01-1 | 256 x 1 | 45/55 | 70/70 | OC | 16 | D,P,F,L | 3-29 |
| Am93412A | 256 x 4 | 35/45 | 155/170 | OC | 22[3] | D,P,F,L | 3-34 |
| Am93422A | 256 x 4 | 35/45 | 155/170 | 3S | 22[3] | D,P,F,L | 3-34 |
| Am93L412A | 256 x 4 | 45/55 | 80/90 | OC | 22[3] | D,P,F,L | 3-34 |
| Am93L422A | 256 x 4 | 45/55 | 80/90 | 3S | 22[3] | D,P,F,L | 3-34 |
| Am93412 | 256 x 4 | 45/60 | 155/170 | OC | 22[3] | D,P,F,L | 3-34 |
| Am93422 | 256 x 4 | 45/60 | 155/170 | 3S | 22[3] | D,P,F,L | 3-34 |
| Am93L412 | 256 x 4 | 60/75 | 80/90 | OC | 22[3] | D,P,F,L | 3-34 |
| Am93L422 | 256 x 4 | 60/75 | 80/90 | 3S | 22[3] | D,P,F,L | 3-34 |
| Am93415A | 1024 x 1 | 30/40 | 155/170 | OC | 16 | D,P,F,L | 3-11 |
| Am93425A | 1024 x 1 | 30/40 | 155/170 | 3S | 16 | D,P,F,L | 3-11 |
| Am93L425A | 1024 x 1 | 45/55 | 65/75 | 3S | 16 | D,P,F,L | 3-11 |
| Am93415 | 1024 x 1 | 45/65 | 155/170 | OC | 16 | D,P,F,L | 3-11 |
| Am93425 | 1024 x 1 | 45/65 | 155/170 | 3S | 16 | D,P,F,L | 3-11 |

Notes: 1. D = Hermetic DIP, P = Molded DIP, F = Cerpak, L = Chip-Pak™.
2. Complement of data in is available on the outputs in the write mode when both $\overline{CS}$ and $\overline{WE}$ are low.
3. Cerpak (F) is 24 pin.

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

# MOS Memory

Functional Index and Selection Guide

## 1K STATIC RAMs

Listed according to organization and access time.

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) | | Pins | Supply Voltage (V) | Temp Range | Package | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Standby | Active | | | | | |
| Am9122-25 | 256 x 4 | 25 | N/A | 660 | 22 | 5 | C | D,P | 4-87 |
| Am9122-35 | 256 x 4 | 35 | N/A | 660 | 22 | 5 | C,M | D,P | 4-87 |
| Am91L22-35 | 256 x 4 | 35 | N/A | 440 | 22 | 5 | C | D,P | 4-87 |
| Am91L22-45 | 256 x 4 | 45 | N/A | 440 | 22 | 5 | C,M | D,P | 4-87 |
| Am91L22-60 | 256 x 4 | 60 | N/A | 248 | 22 | 5 | C | D,P | 4-87 |
| Am9101D | 256 x 4 | 250 | 47 | 315 | 22 | 5 | C | D,P | 4-58 |
| Am9111D | 256 x 4 | 250 | 47 | 315 | 18 | 5 | C | D,P | 4-67 |
| Am9112D | 256 x 4 | 250 | 47 | 315 | 16 | 5 | C | D,P | 4-75 |
| Am9101C | 256 x 4 | 300 | 47 | 315 | 22 | 5 | C,M | D,P | 4-58 |
| Am91L01C | 256 x 4 | 300 | 38 | 189 | 22 | 5 | C,M | D,P | 4-58 |
| Am9111C | 256 x 4 | 300 | 47 | 315 | 18 | 5 | C,M | D,P | 4-67 |
| Am91L11C | 256 x 4 | 300 | 38 | 189 | 18 | 5 | C,M | D,P | 4-67 |
| Am9112C | 256 x 4 | 300 | 47 | 315 | 16 | 5 | C,M | D,P | 4-75 |
| Am91L12C | 256 x 4 | 300 | 38 | 189 | 16 | 5 | C,M | D,P | 4-75 |
| Am9101B | 256 x 4 | 400 | 47 | 290 | 22 | 5 | C,M | D,P | 4-58 |
| Am91L01B | 256 x 4 | 400 | 38 | 173 | 22 | 5 | C,M | D,P | 4-58 |
| Am9111B | 256 x 4 | 400 | 47 | 290 | 18 | 5 | C,M | D,P | 4-58 |
| Am91L11B | 256 x 4 | 400 | 38 | 173 | 18 | 5 | C,M | D,P | 4-58 |
| Am9112B | 256 x 4 | 400 | 47 | 290 | 16 | 5 | C,M | D,P | 4-75 |
| Am91L12B | 256 x 4 | 400 | 38 | 173 | 16 | 5 | C,M | D,P | 4-75 |
| Am9101A | 256 x 4 | 500 | 47 | 290 | 22 | 5 | C,M | D,P | 4-58 |
| Am91L01A | 256 x 4 | 500 | 38 | 173 | 22 | 5 | C,M | D,P | 4-58 |
| Am9111A | 256 x 4 | 500 | 47 | 290 | 18 | 5 | C,M | D,P | 4-58 |
| Am91L11A | 256 x 4 | 500 | 38 | 173 | 18 | 5 | C,M | D,P | 4-58 |
| Am9112A | 256 x 4 | 500 | 47 | 290 | 16 | 5 | C,M | D,P | 4-75 |
| Am91L12A | 256 x 4 | 500 | 38 | 173 | 16 | 5 | C,M | D,P | 4-75 |

## 4K STATIC RAMs

Listed according to organization and access time.

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) | | Pins | Supply Voltage (V) | Temp Range | Package | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Standby | Active | | | | | |
| Am2148-35 | 1024 x 4 | 35 | 165 | 990 | 18 | 5 | C | D,L | 4-13 |
| Am2149-35 | 1024 x 4 | 35 | N/A | 990 | 18 | 5 | C | D | 4-13 |
| Am2148-45 | 1024 x 4 | 45 | 165 | 990 | 18 | 5 | C,M | D,L | 4-13 |
| Am21L48-45 | 1024 x 4 | 45 | 110 | 688 | 18 | 5 | C | D,L | 4-13 |
| Am2149-45 | 1024 x 4 | 45 | N/A | 990 | 18 | 5 | C,M | D | 4-13 |
| Am21L49-45 | 1024 x 4 | 45 | N/A | 688 | 18 | 5 | C | D,L | 4-13 |
| Am2148-55 | 1024 x 4 | 55 | 165 | 990 | 18 | 5 | C,M | D,L | 4-13 |
| Am21L48-55 | 1024 x 4 | 55 | 110 | 688 | 18 | 5 | C | D,L | 4-13 |
| Am2149-55 | 1024 x 4 | 55 | N/A | 990 | 18 | 5 | C,M | D | 4-13 |
| Am21L49-55 | 1024 x 4 | 55 | N/A | 688 | 18 | 5 | C | D,L | 4-13 |
| Am2148-70 | 1024 x 4 | 70 | 165 | 990 | 18 | 5 | C,M | D,L | 4-13 |
| Am21L48-70 | 1024 x 4 | 70 | 110 | 688 | 18 | 5 | C | D,L | 4-13 |
| Am2149-70 | 1024 x 4 | 70 | N/A | 990 | 18 | 5 | C,M | D | 4-13 |
| Am21L49-70 | 1024 x 4 | 70 | N/A | 688 | 18 | 5 | C | D,L | 4-13 |
| Am9114E | 1024 x 4 | 200 | | 350 | 18 | 5 | C,M | D,P | 4-81 |
| Am91L14E | 1024 x 4 | 200 | | 250 | 18 | 5 | C | D,P | 4-81 |
| Am9114C | 1024 x 4 | 300 | | 350 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am91L14C | 1024 x 4 | 300 | | 250 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am9124C | 1024 x 4 | 300 | 150 | 350 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am91L24C | 1024 x 4 | 300 | 100 | 250 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am9114B | 1024 x 4 | 450 | | 350 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am91L14B | 1024 x 4 | 450 | | 250 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am9124B | 1024 x 4 | 450 | 150 | 350 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am91L24B | 1024 x 4 | 450 | 100 | 250 | 18 | 5 | C,M | D,P,F | 4-81 |
| Am21L41-12 | 4096 x 1 | 120 | 25 | 200 | 18 | 5 | C | D,P | 4-1 |
| Am21L41-15 | 4096 x 1 | 150 | 25 | 200 | 18 | 5 | C | D,P | 4-1 |
| Am21L41-20 | 4096 x 1 | 200 | 25 | 200 | 18 | 5 | C | D,P | 4-1 |
| Am21L41-25 | 4096 x 1 | 250 | 25 | 200 | 18 | 5 | C | D,P | 4-1 |
| Am9044B | 4096 x 1 | 450 | | 350 | 18 | 5 | C,M | D,P | 4-38 |
| Am90L44B | 4096 x 1 | 450 | | 250 | 18 | 5 | C,M | D,P | 4-38 |
| Am9044C | 4096 x 1 | 300 | | 350 | 18 | 5 | C,M | D,P | 4-38 |
| Am90L44C | 4096 x 1 | 300 | | 250 | 18 | 5 | C,M | D,P | 4-38 |
| Am9044D | 4096 x 1 | 250 | | 350 | 18 | 5 | C,M | D,P | 4-38 |

## 4K STATIC RAMs (Cont.)

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) | | Pins | Supply Voltage (V) | Temp Range | Package | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Standby | Active | | | | | |
| Am90L44D | 4096 x 1 | 250 | | 250 | 18 | 5 | C,M | D,P | 4-38 |
| Am9044E | 4096 x 1 | 200 | | 350 | 18 | 5 | C | D,P | 4-38 |
| Am90L44E | 4096 x 1 | 200 | | 250 | 18 | 5 | C | D,P | 4-38 |
| Am9244B | 4096 x 1 | 450 | 150 | 350 | 18 | 5 | C,M | D,P | 4-38 |
| Am92L44B | 4096 x 1 | 450 | 100 | 250 | 18 | 5 | C,M | D,P | 4-38 |
| Am9244C | 4096 x 1 | 300 | 150 | 350 | 18 | 5 | C,M | D,P | 4-38 |
| Am92L44C | 4096 x 1 | 300 | 100 | 250 | 18 | 5 | C,M | D,P | 4-38 |
| Am9244D | 4096 x 1 | 250 | 150 | 350 | 18 | 5 | C,M | D,P | 4-38 |
| Am92L44D | 4096 x 1 | 250 | 100 | 250 | 18 | 5 | C,M | D,P | 4-38 |
| Am9244E | 4096 x 1 | 200 | 150 | 350 | 18 | 5 | C | D,P | 4-38 |
| Am92L44E | 4096 x 1 | 200 | 100 | 250 | 18 | 5 | C | D,P | 4-38 |
| Am2147-35 | 4096 x 1 | 35 | 165 | 990 | 18 | 5 | C | D | 4-7 |
| Am2147-45 | 4096 x 1 | 45 | 165 | 990 | 18 | 5 | M | D,L | 4-7 |
| Am2147-55 | 4096 x 1 | 55 | 165 | 990 | 18 | 5 | C,M | D,L | 4-7 |
| Am2147-70 | 4096 x 1 | 70 | 110 | 880 | 18 | 5 | C,M | D,L | 4-7 |
| Am21L47-45 | 4096 x 1 | 45 | 83 | 688 | 18 | 5 | C | D | 4-7 |
| Am21L47-55 | 4096 x 1 | 55 | 83 | 688 | 18 | 5 | C | D | 4-7 |

## 16K STATIC RAMs

Listed according to organization and access time.

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) | | Pins | Supply Voltage (V) | Temp Range | Package | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Standby | Active | | | | | |
| Am9128-70 | 2048 x 8 | 70 | 165 | 770 | 24 | 5 | C | D,P | 4-93 |
| Am9128-90 | 2048 x 8 | 90 | 165 | 990 | 24 | 5 | M | D | 4-93 |
| Am9128-10 | 2048 x 8 | 100 | 165 | 660 | 24 | 5 | C | D,P | 4-93 |
| Am9128-12 | 2048 x 8 | 120 | 165 | 825 | 24 | 5 | M | D | 4-93 |
| Am9128-15 | 2048 x 8 | 150 | 83/165 | 550 | 24 | 5 | C,M | D,P | 4-93 |
| Am9128-20 | 2048 x 8 | 200 | 165 | 770/880 | 24 | 5 | C,M | D,P | 4-93 |
| Am2167-35 | 16384 x 1 | 35 | 165 | 660 | 20 | 5 | C | D,P | 4-20 |
| Am2167-45 | 16384 x 1 | 45 | 83 | 660/880 | 20 | 5 | C,M | D,P | 4-20 |
| Am2167-55 | 16384 x 1 | 55 | 83 | 660 | 20 | 5 | C,M | D,P | 4-20 |
| Am2167-70 | 16384 x 1 | 70 | 165 | 660 | 20 | 5 | C,M | D,P | 4-20 |

*Available in 1984

## DYNAMIC RAMs

Listed according to organization and access time.

| Part Number | Organization | Access Time (ns) | Power Dissipation (mW) | | Pins | Supply Voltage (V) | Temp Range | Package | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| | | | Standby | Active | | | | | |
| Am9016F | 16384 x 1 | 150 | 20 | 420 | 16 | +12 ±5 | C | P,D,L | 4-26 |
| Am9016E | 16384 x 1 | 200 | 20 | 420 | 16 | +12 ±5 | C,L | P,D,L | 4-26 |
| Am9016D | 16384 x 1 | 250 | 20 | 420 | 16 | +12 ±5 | C,L | P,D,L | 4-26 |
| Am9016C | 16384 x 1 | 300 | 20 | 420 | 16 | +12 ±5 | C,L | P,D,L | 4-26 |
| Am9064-10 | 65536 x 1 | 100 | 22 | 384 | 16 | +5 ±10 | C | P,D | 4-43 |
| Am9064-12 | 65536 x 1 | 120 | 22 | 330 | 16 | +5 ±10 | C | P,D | 4-43 |
| Am9064-15 | 65536 x 1 | 150 | 22 | 300 | 16 | +5 ±10 | C | P,D | 4-43 |

## ROMs

Listed according to organization and access time.

| Part Number | Organization | Access Time (ns) | Temp Range | Supply Voltage | Pins | Operating Power Max (mW) | Outputs | Page No. |
|---|---|---|---|---|---|---|---|---|
| Am9218B | 2048 x 8 | 450 | C,M | +5 | 24 | 368 | 3-State | 5-1 |
| Am9218C | 2048 x 8 | 350 | C | +5 | 24 | 368 | 3-State | 5-1 |
| Am9232D | 4096 x 8 | 250 | C | +5 | 24 | 420 | 3-State | 5-6 |
| Am9233D | 4096 x 8 | 250 | C | +5 | 24 | 420 | 3-State | 5-6 |
| Am9232C | 4096 x 8 | 300 | C | +5 | 24 | 420 | 3-State | 5-6 |
| Am9233C | 4096 x 8 | 300 | C | +5 | 24 | 420 | 3-State | 5-6 |
| Am9232B | 4096 x 8 | 450 | C,M | +5 | 24 | 420 | 3-State | 5-6 |
| Am9233B | 4096 x 8 | 450 | C,M | +5 | 24 | 420 | 3-State | 5-6 |
| Am9264D | 8192 x 8 | 250 | C | +5 | 24 | 440 | 3-State | 5-11 |
| Am9265D | 8192 x 8 | 250 | C | +5 | 28 | 440,110[1] | 3-State | 5-16 |
| Am9264C | 8192 x 8 | 300 | C | +5 | 24 | 440 | 3-State | 5-11 |
| Am9265C | 8192 x 8 | 300 | C | +5 | 28 | 440,110[1] | 3-State | 5-16 |
| Am9264B | 8192 x 8 | 450 | C,M | +5 | 24 | 440 | 3-State | 5-11 |
| Am9265B | 8192 x 8 | 450 | C,M | +5 | 28 | 440,110[1] | 3-State | 5-16 |
| Am92128D | 16384 x 8 | 250 | C | +5 | 28 | 440,137[1] | 3-State | 5-21 |

## ROMs (Cont.)

| Part Number | Organization | Access Time (ns) | Temp Range | Supply Voltage | Pins | Operating Power Max (mW) | Outputs | Page No. |
|---|---|---|---|---|---|---|---|---|
| Am92128C | 16384 x 8 | 300 | C | +5 | 28 | 440,137[1] | 3-State | 5-21 |
| Am92128B | 16384 x 8 | 450 | C,M | +5 | 28 | 440,137[1] | 3-State | 5-21 |
| Am92256D | 32768 x 8 | 250 | C | +5 | 28 | 660,165[1] | 3-State | 5-26 |
| Am92256C | 32768 x 8 | 300 | C | +5 | 28 | 660,165[1] | 3-State | 5-26 |
| Am92256B | 32768 x 8 | 450 | C | +5 | 28 | 660,165[1] | 3-State | 5-26 |

Note: 1. Standby

## U.V. ERASABLE PROMs

Listed according to organization and access time.

| Part Number | Organization | Access Time (ns) | Temp Range | Operating Power – Act/Stby Max (mW) | Supply Voltages | Outputs | Number of Pins | Page No. |
|---|---|---|---|---|---|---|---|---|
| Am1702A-1 | 256 x 8 | 550 | C,L | 676 | –9,+5 | 3-State | 24 | 6-1 |
| Am1702AL-1 | 256 x 8 | 550 | C,L | N/A | –9,+5 | 3-State | 24 | 6-1 |
| Am1702A-2 | 256 x 8 | 650 | C,L | 676 | –9,+5 | 3-State | 24 | 6-1 |
| Am1702AL-2 | 256 x 8 | 650 | C,L | N/A | –9,+5 | 3-State | 24 | 6-1 |
| Am1702A | 256 x 8 | 1000 | C,L | 676 | –9,+5 | 3-State | 24 | 6-1 |
| Am1702AL | 256 x 8 | 1000 | C,L | N/A | –9,+5 | 3-State | 24 | 6-1 |
| Am9716 | 2048 x 8 | 300 | C | 525/132 | +5 | 3-State | 24 | 6-8 |
| Am2716-1 | 2048 x 8 | 350 | C,I,L | 525/132 | +5 | 3-State | 24 | 6-8 |
| Am2716-2 | 2048 x 8 | 390 | C | 525/132 | +5 | 3-State | 24 | 6-8 |
| Am2716 | 2048 x 8 | 450 | C,I,L,M | 525/132 | +5 | 3-State | 24 | 6-8 |
| Am2732A-2 | 4096 x 8 | 200 | C,I,L | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2732A-20 | 4096 x 8 | 200 | C,I,L,M | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2732A | 4096 x 8 | 250 | C,I,L | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2732A-25 | 4096 x 8 | 250 | C,I,L,M | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2732A-3 | 4096 x 8 | 300 | C,I,L | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2732A-30 | 4096 x 8 | 300 | C,I,L | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2732-1 | 4096 x 8 | 350 | C | 787/157 | +5 | 3-State | 24 | 6-14 |
| Am2732-2 | 4096 x 8 | 390 | C | 787/157 | +5 | 3-State | 24 | 6-14 |
| Am2732 | 4096 x 8 | 450 | C,I,L,M | 787/157 | +5 | 3-State | 24 | 6-14 |
| Am2732A-4 | 4096 x 8 | 450 | C,I,L | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2732A-45 | 4096 x 8 | 450 | C,I,L,M | 512/132 | 5V | 3-State | 24 | 6-14 |
| Am2764-2 | 8192 x 8 | 200 | C,I | 525/105 | +5 | 3-State | 28 | 6-27 |
| Am2764 | 8192 x 8 | 250 | C,I,M | 525/105 | +5 | 3-State | 28 | 6-27 |
| Am2764-3 | 8192 x 8 | 300 | C,I | 525/105 | +5 | 3-State | 28 | 6-27 |
| Am2764-4 | 8192 x 8 | 450 | C,I,M | 525/105 | +5 | 3-State | 28 | 6-27 |
| Am27128-1 | 16384 x 8 | 150 | C,I | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-15 | 16384 x 8 | 150 | C,I | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-2 | 16384 x 8 | 200 | C,I,L | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-20 | 16384 x 8 | 200 | C,I,L,M | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128 | 16384 x 8 | 250 | C,I,L | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-25 | 16384 x 8 | 250 | C,I,L,M | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-3 | 16384 x 8 | 300 | C,I,L | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-30 | 16384 x 8 | 300 | C,I,L | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-4 | 16384 x 8 | 450 | C,I,L | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27128-45 | 16384 x 8 | 450 | C,I,L,M | 512/132 | 5V | 3-State | 28 | 6-42 |
| Am27256-1 | 32768 x 8 | 170 | C | 525/132 | +5 | 3-State | 28 | 6-51 |
| Am27256-2 | 32768 x 8 | 200 | C,I,M | 525/132 | +5 | 3-State | 28 | 6-51 |
| Am27256 | 32768 x 8 | 250 | C | 525/132 | +5 | 3-State | 28 | 6-51 |
| Am27256-3 | 32768 x 8 | 300 | C | 525/132 | +5 | 3-State | 28 | 6-51 |
| Am27256-4 | 32768 x 8 | 450 | C | 525/132 | +5 | 3-State | 28 | 6-51 |
| Am27512 | 65536 x 8 | 250 | C,I,M | 525/132 | +5 | 3-State | 28 | 6-59 |

## ELECTRICALLY ERASABLE PROMs

Listed according to organization and access time.

| Part Number | Organization | Access Time (ns) | Temp Range | Operating Power – Act/Stby Max (mW) | Supply Voltages | Outputs | Number of Pins | Page No. |
|---|---|---|---|---|---|---|---|---|
| Am9864-2 | 8192 x 8 | 200 | C,M | 350/100 | +5 | 3-State | 28 | 6-36 |
| Am9864 | 8192 x 8 | 250 | C,M | 350/100 | +5 | 3-State | 28 | 6-36 |
| Am9864-3 | 8192 x 8 | 300 | C,M | 350/100 | +5 | 3-State | 28 | 6-36 |

**Temperature Ranges**

C = Commercial 0°C to 70°C
M = Military –55°C to +125°C
L = Extended –55°C to +85°C or +100°C
I = Industrial –40°C to +85°C

**Package Types**

D = Cerdip
P = Plastic
F = Flat Pack
L = Leadless Chip Carrier

# Testing High-Performance Bipolar Memory

by
Bob Lutz
Advanced Micro Devices

1

## INTRODUCTION

During the last several years, the state-of-the art of TTL compatible bipolar memory integrated circuits has advanced very rapidly. Device complexity has increased dramatically not only in terms of the memory storage capacity but also by the addition of new on-chip functions such as the inclusion of output data registers. Simultaneously, advances in bipolar LSI design and manufacturing technology have generated significant improvements in the performance levels of bipolar memory. Similarly, the complexity and performance levels of systems which employ these devices have grown. The concomitant growth of system complexity has placed additional demands on both the device manufacturer and the user's incoming inspection area to assure the performance capabilities of each component before it is assembled into the system.

Several test equipment manufacturers now supply sophisticated, computer controlled testers for these inspection tasks. Most of this equipment is inherently capable of the millivolt and nanosecond accuracies which are required; most memory testers can generate the complex waveforms and test patterns needed. However, the details of applying this equipment to a specific test problem, including the problem of interfacing the tester to the device-under-test, are usually left to the user. The purpose of this application note is to discuss several problems which are frequently encountered when testing high performance bipolar memory devices, and to acquaint the user with how such problems may be identified, measured and corrected.

## WHAT MAKES A MEMORY GOOD?

Before discussing the specifics of bipolar memory testing problems, it is important to understand the basic characteristics which these devices should exhibit. Clearly each device must meet all product specification parameters but, first and foremost, a bipolar memory should be fast! Address access time (delay from address input to data output), enable access time and enable recovery time should be as small as possible. High performance is often the primary reason for using bipolar memory. Similarly, the performance of the ideal bipolar memory should remain relatively constant with changes in supply voltage, ambient temperature and output load capacitance. Fast devices, offering stable performance over a broad range of conditions, permit the user to qualify a smaller number of part types; one fast device can accommodate many standard as well as high performance applications. Such devices provide added safety margin for the system design, permit simplification of system test and debug and assure trouble-free system performance in the field. Hence the "best" memory is a fast, stable device which not only meets a given user specification, but also offers the extra performance needed for a broad range of applications.

Advanced Micro Devices offers a family of bipolar Random Access Memories (RAMs) and Programmable Read Only Memories (PROMs) which are designed to meet this idealized definition as closely as possible. First, each AMD device is designed to meet a "military design goal." This means AMD bipolar memories are designed to provide the extra margins and higher output drive capabilities needed to assure proper performance over the extended miliary supply voltage and operating temperature ranges. This often necessitates the use of more advanced design techniques such as on-chip regulators, temperature and voltages compensation networks and feedback circuits. Second, AMD has conceived and developed an advanced, oxide separated, ion implanted manufacturing process called IMOX™. Developed specifically for the production of high density bipolar memories, this technology provides both high density and excellent performance in a truly reliable and manufacturable process. This combination of advanced design and fabrication technologies assures the military user of receiving components which are intended for his application while providing the commercial user with the extra margins, performance advantages and procurement benefits mentioned above.

## THE SYSTEM ENVIRONMENT

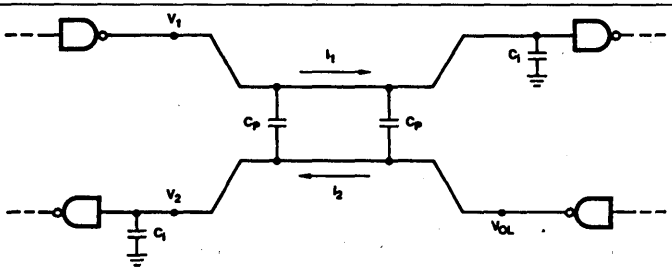
To understand the problems of high-performance memory testing, it is helpful to understand the electrical environment in which the memory devices will actually operate, i.e., the typical system environment. The system designer must address and resolve several critically important questions if the system is to consistently perform to its design specifications. These questions include:

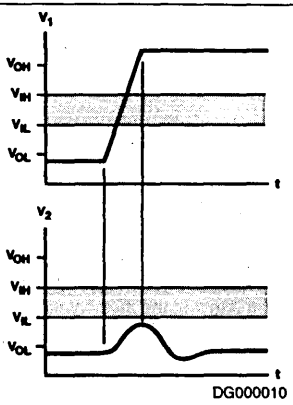
1. What noise voltages can the system's logic and memory devices tolerate?
2. What are the sources of system noise?
3. What can be done to control and minimize this noise?

The first question is answered relatively easily. The magnitude of noise which can be tolerated relates directly to the worst case noise immunity specified for the logic family. Noise immunity is simply the difference between the worst case output levels ($V_{OH}$ and $V_{OL}$) of the driving circuit and the worst case input voltage requirements ($V_{IH}$ and $V_{IL}$, respectively) of the receiving circuit. For TTL devices the worst case noise immunity is typically 400mV for both the high and low logic levels.

If "system noise" is defined as the sum of things which subtract from this noise immunity, several sources can be identified. A few of the most important sources found in a digital, TTL system are listed below:

- Cross-Talk: The desire to pack system components as tightly as possible inevitably causes signal wires or PC board traces to be placed in close proximity. The lead-to-lead capacitance and mutual inductance thus created (see Figure 1) causes "noise" voltages to appear when adjacent signal paths switch.
- Transmission Line Reflections: Like it or not, every signal path in the system has transmission line characteristics. TTL signal paths are usually not designed as transmission lines, with predictable and uniform characteristic impedances. This is partly because of the higher costs implied for multilayer PC boards with internal ground planes, termination resistors, etc. It is also the result of TTL logic's limited ability to drive the low impedance lines provided by current PC board technologies. Hence, TTL signal paths do exhibit the ringing and reflection problems associated with improperly terminated transmission lines. These reflections subtract from the available noise immunity as shown in Figure 2.

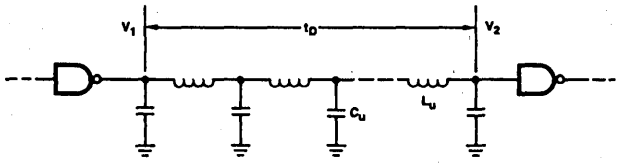


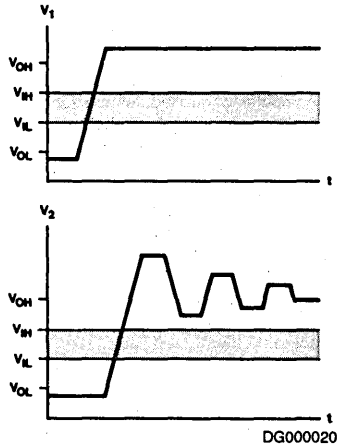




DG000010

As $V_1$ switches, $I_1$ flows to charge the input capacitance $C_i$. $I_2$ flows as a result of mutual inductance. The $V_1$ voltage change is also coupled directly to $V_2$ through the parasitic line-to-line capacitances, $C_P$.

**Figure 1. An Example of Cross-Talk**

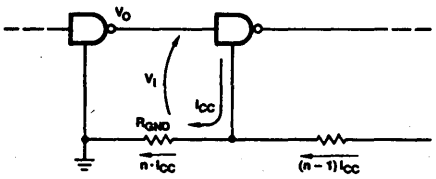



DG000020

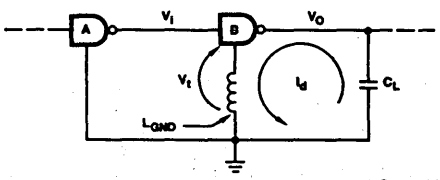
The unit length capacitance and inductance ($C_U$ and $L_U$) give each system connection transmission line characteristics. Without a matched termination, switching at $V_1$ causes reflection voltages to appear at $V_2$, reducing noise immunity.

**Figure 2. Line Reflections**




$V_i = V_O - (n \cdot I_{CC})\ R_{GND}$

**a) DC Ground "Noise"**




DG000030

When $V_i$ goes HIGH, $V_O$ goes LOW discharging $C_L$. The discharge current $I_d$ flows through the ground inductance $L_{GND}$, creating a transient voltage $V_t$. The input voltage seen by gate B is actually $V_i - V_t$.

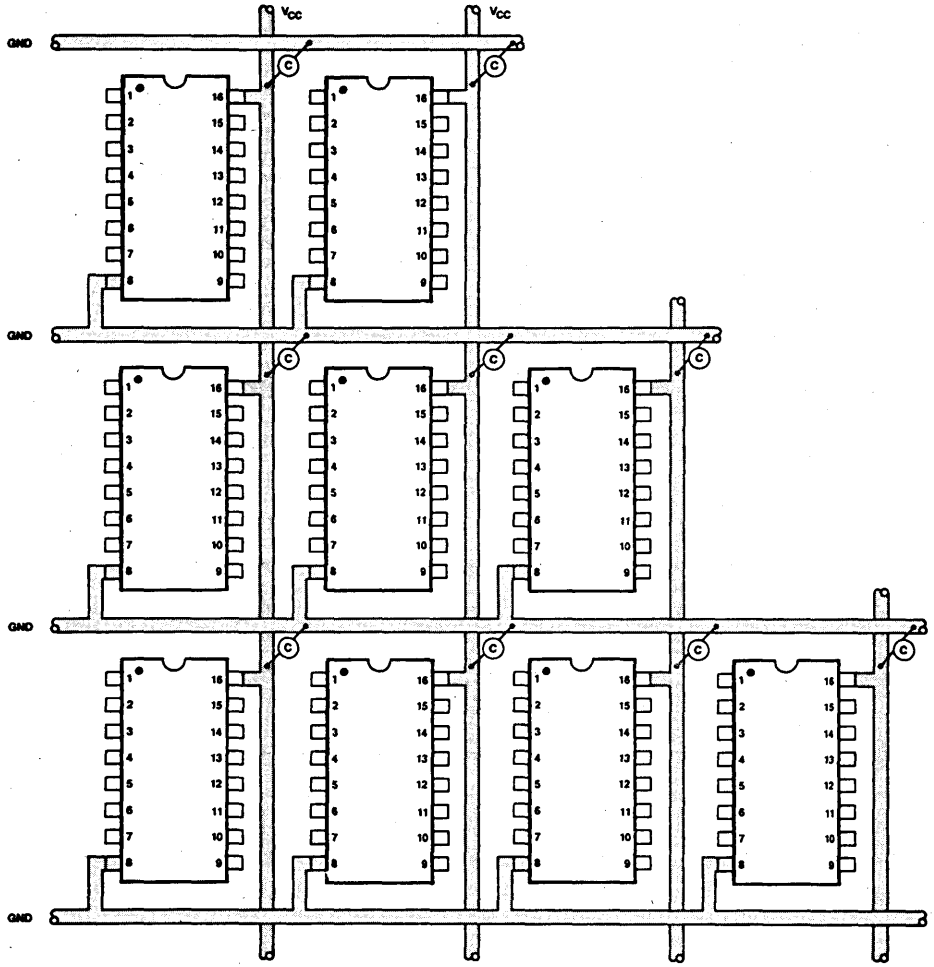
**b) Transient Ground Noise**

**Figure 3.**

- Ground Network Noise: Most high-performance systems employ large numbers of high-performance ICs. These devices typically draw large $I_{CC}$ currents from the power supply. Cumulatively, these currents can reach several amperes per board. Such currents, flowing in the ground network, cause non-negligible DC voltage drops to occur; not all device ground pins are at zero volts. Since the output levels and the input thresholds of each TTL device reference the local ground (Figure 3a), these drops also subtract from the available noise immunity. Additional noise margin losses occur each time the device outputs switch. This occurs because large currents must flow to rapidly charge and discharge the interconnect and input capacitances which load each output. These charging currents flow in a loop

(Figure 3b) through the ground network which is normally a simple interconnection of wires, each with some value of resistance and inductance per unit length. Some additional resistive drops occur. But, the rapid changes in these currents (large di/dt), occurring as charging starts and stops, mean a transient ground noise voltage is also generated. This voltage obeys the law of $v = L(di/dt)$ where L is the ground circuit inductance and di/dt is the rate of change of the charging currents. Notice that adding local bypass capacitors can only reduce this voltage by paralleling the ground inductance with the $V_{CC}$ network inductance. Bypassing cannot eliminate this problem because these capacitors shunt the devices and not the ground and $V_{CC}$ network inductances where the noise is generated.

Controlling and minimizing noise in a digital system becomes more challenging as the system performance requirements increase. These requirements demand devices capable of short propagation delays, e.g., ultra-fast memories with excellent drive characteristics to minimize fully loaded access times.




Note: Transient ground current flow in four directions from each device ground: right and left on the ground bus; up and down the $V_{CC}$ bus after passing through the local bypass capacitor, C. Equivalent ground inductance is very low.

**Figure 4. Example of an AC Ground Mesh**

Since noise margin violations result in system malfunctions, the system designer must define a set of rules governing the physical construction techniques to be used within the system. These rules address a host of considerations including power distribution, AC grounding, lead placement, line termination requirements, logic loading (fan in and fan out) and interconnect delays. Specifying these rules is a complex process of making appropriate cost-performance tradeoffs.

For a medium to high performance system, these rules might specify arranging devices in an array with $V_{CC}$ power traces running vertically up the columns while ground metal running horizontally between the rows. Inserting bypass capacitors at each grid intersection forms an AC ground mesh (Figure 4), limiting the amount of ground inductance at each array site. If limits are also placed on the total capacitance each device may drive (cumulative interconnect and input capacitance on

all outputs), the total charging currents may be controlled thus limiting the noise immunity eroded by ground circuit noise. Similarly, the distance between adjacent traces and the maximum length of unterminated lines may be specified to control noise immunity losses caused by cross-talk and termination mismatches. Ultra-high performance systems may require additional measures; e.g., multilayer boards with true ground planes or increased usage of line drivers and receivers. Though the preceding descriptions have been simplified, it should be clear that distances between driving and receiving devices, the quantity and distribution of load capacitance, as well as the AC ground network integrity are all essential elements of the system design.

## THE MEMORY TEST ENVIRONMENT

Ideally the test system hardware and fixtures would be designed to even more stringent rules than those used for the system. This is reasonable as the tester is the standard employed for accepting or rejecting components used in the system. Because a collection of additional objectives constrain the test environment, designing test hardware to equally or more stringent rules is usually impractical.

Memory testers must test many types of components under a variety of conditions. Tests performed include DC parametric tests, functional and AC tests with complex test patterns and margin tests to assure device operation at the extremes of applied conditions and supply voltage. To accomplish this, connections to sets of programmable input drivers and output receivers (comparators), multiple device bias and power supplies, relays to permit connection of the DC parametric test unit, and special load circuits must all converge at the test site.

To provide flexibility and facilitate repair, test hardware must be modular. This requirement dictates placing the hardware (drivers, receivers, etc.) on many small PC boards which then must talk to the DUT (device under test) through additional wiring and connectors.

Frequently the quantity of parts tested necessitates mating an automatic device handler to the tester. Handlers also provide capabilities for testing at temperature extremes when needed. The DUT must be tested inside this equipment, requiring still more wiring between the test head and the actual test site.

Ideally, all test hardware would be located immediately adjacent to the test site to minimize cross-talk, reflections and ground noise. However, this objective must be compromised to address the other objectives and constraints outlined above. Techniques commonly employed in making this compromise are illustrated in Figure 5. Notice that DUT drivers are remote from the test site, driving signal to the DUT through "series terminated" transmission lines. Similarly the receivers are some distance from the test site, receiving signals from the DUT through a series of connectors and wires which can degrade the signal. Most annoying of all, the test site ground connection has been compromised. This signal path must carry heavy transient and DC currents during test and should provide a very solid, low impedance reference against which all AC and DC tests are made. Accumulating resistance and inductance in this path jeopardizes the integrity of all test results.

Hence, the electrical environment provided at the test site is generally inferior to the actual system environment where the memory component will be used.

## TEST RELATED PROBLEMS AND SOLUTIONS

Accurately measuring or verifying memory performance in the test system environment requires a recognition of its inherent limitations. Outlined below are five problem areas commonly encountered when testing high-performance bipolar memories. Methods of identifying and alleviating these problems are indicated.

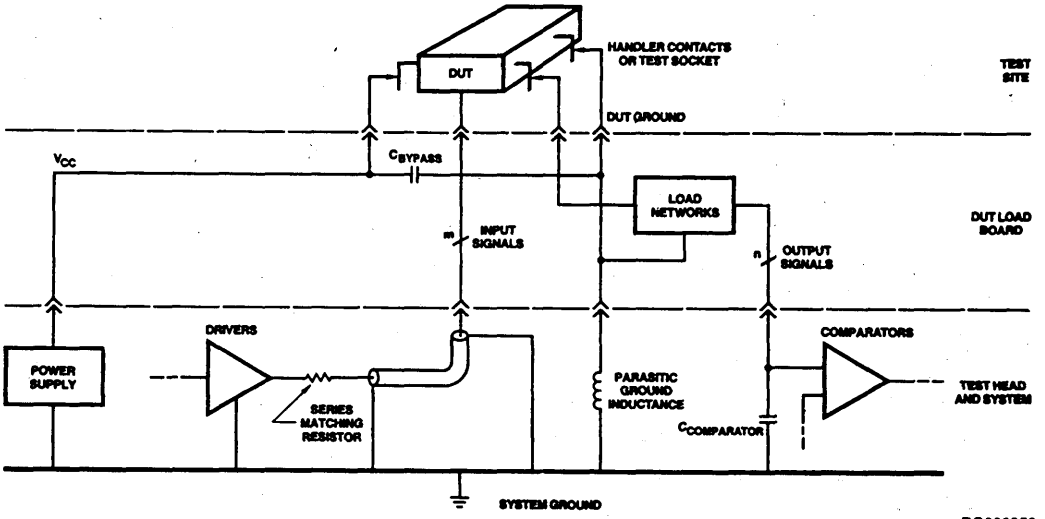



**Figure 5. The Test System Environment**

- Contending with Ground Noise: Ground noise is one of the most common and troublesome test problems. As defined above, ground noise is caused by switching currents flowing through the ground network impedance. Whereas the system environment (Figure 4) may provide multiple low inductance ground paths into a ground mesh or plane, the tester provides one long, higher inductance path back to the test system ground (Figure 5). This path includes handler con-

tacts, connectors and the DUT load board, all of which increase ground inductance and resistance. Transient currents which result when the DUT switches can be enormous. Consider the case of a byte wide (8 output) memory functional test. At some point in the test sequence, all memory outputs will switch from high to low ($V_{OH}$ to $V_{OL}$) at the same instant, discharging all eight load capacitances simultaneously. If the input capacitance of the receiver is 40pF and the interconnect capacitance of the test fixture is 10pF, the total load capacitance driven by all device outputs would be 400pF. A fast memory device could discharge this load at a 1V/ns rate. The relationship i = C(dv/dt) implies peak charging currents of 400mA must flow through ground. As Figure 6 illustrates, this charging current does not build to its full value instantaneously. For a fast device the time required to go from zero to full charging current would approximate 2ns. A resultant ground current di/dt of 200mA/ns is implied. If the ground inductance is 1 nanohenry (approximate inductance of 1 inch of straight, small gauge wire), then v = L(di/dt) predicts AC ground noise of 200mV. As you have probably guessed, the typical test site ground inductance exceeds 1nh. The path is longer and it is usually not a straight line connection. Actual tester ground noise of up to 800mV is common when testing high-performance byte wide memories. This noise can be measured easily with a high bandwidth oscilloscope by attaching the scope ground to the actual test system ground and monitoring the DUT ground pin with one channel.

Excessive ground noise creates several problems: First, this noise is capacitively coupled to the input drive signals through the DUT input capacitances; if large enough, DC coupling through the DUT input clamp diodes can occur (Figure 7). The DUT output levels are, of course, referenced to the DUT ground potential whereas the receiver board is referenced to test system ground, introducing inaccuracy in access time measurements, etc.

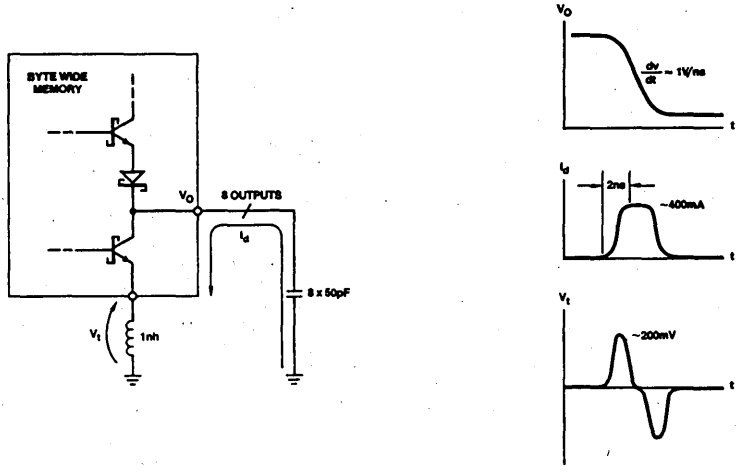
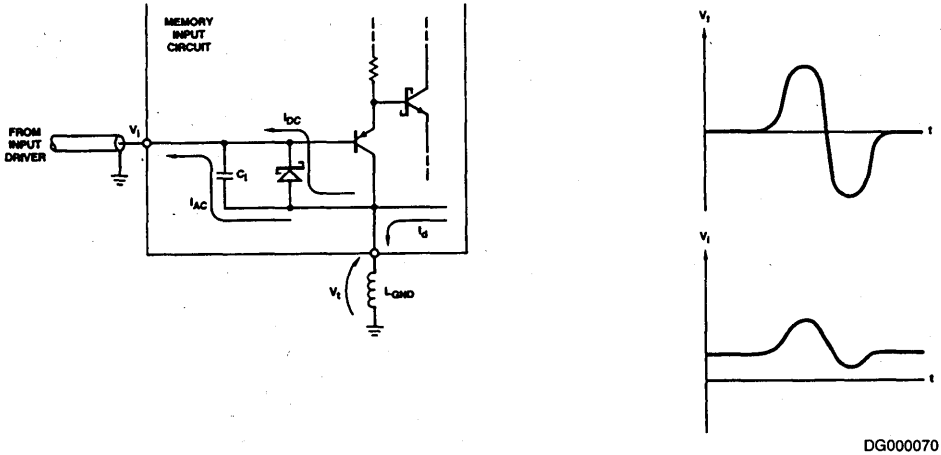



**Figure 6. Byte Wide Memory Ground Transients**




For small magnitudes of noise, $V_t$, noise is AC coupled to the inputs through the input capacitance, $C_i$. If $V_i$ is low, large positive values of $V_t$ may momentarily forward bias the input clamp diode, creating a DC coupling.

**Figure 7. Ground Noise Coupling to the Inputs**

Worst of all, severe ground noise can make functional testing at or near the guaranteed input levels ($V_{IH}$ and $V_{IL}$) impossible. To demonstrate, assume the device ground noise reaches a positive 0.8V with respect to test system ground during output switching. Assume the input driver high level is programmed to 2.0V, minimum $V_{IH}$ for most TTL devices. The actual voltage between a "high" DUT input and its ground is only 1.2V. The typical room temperature threshold voltage of a TTL device is 1.5V, and the device interprets 1.2V as a logic "low." This causes the memory to access a new memory location momentarily. The resultant momentary change in output data interferes with access time measurements. In severe cases, this momentary switching of output data creates additional ground noise which also feeds back to the inputs resulting in sustained oscillations. This noise interaction can also be viewed with a dual trace oscilloscope as shown in Figure 8. Channel A of the scope is connected to the address input while channel B monitors the DUT ground pin. The input voltage, as seen by the DUT, can be viewed directly by putting the scope in "A – B," algebraic subtract mode. Note the scope ground is connected to test system ground as before. Attaching scope ground to the DUT pin ground should be avoided as this creates a "ground loop." If connected this way, large noise currents flow in the alternate ground path provided by the scope back to earth ground; this interferes with the scope's ability to measure high-speed events and modifies the condition which is to be observed.

Several techniques can be employed to reduce ground noise problems:

- Keep the ground path as short as possible; use large diameter wire and "straight line" wiring techniques.
- Minimize the number of series connections in the DUT ground path; provide as many parallel ground connections as possible through each remaining connector.
- If the system uses a Kelvin (force – sense) ground system, terminate the system by shorting force to sense on the DUT load board. Kelvin systems provide DC accuracy, but their response times are much too slow to aid in the suppression of ground noise at the test site. Terminating Kelvin early sacrifices a little DC accuracy, but the ability to use the previous sense line as second, low impedance ground path usually improves the overall test accuracy.
- Provide multiple high frequency bypass capacitors as close as possible to the DUT, and again on the DUT load board. This allows the $V_{CC}$ wiring to serve as an extra AC ground path for high frequency ground noise.
- Reduce the DUT load capacitance (receiver and interconnect capacitance) as much as possible; avoid using low values of load resistors. Both techniques reduce the transient currents, thus improving test accuracy. When necessary, DUT output drive capability can usually be verified with DC tests.
- If $V_{IL}$ and $V_{IH}$ tests are necessary, measure the maximum amount of ground noise that the specific device type to be tested generates in the actual test site. Set the input drive levels no tighter than "$V_{IH}$ plus the maximum noise" and "$V_{IL}$ minus the maximum noise." Using tighter limits over tests the device!
- Alternatively, use DC bench tests on a sample basis to verify that input margins are acceptable. This is a sound practice as the input thresholds of bipolar devices are extremely insensitive to fabrication process variations. Virtually any process variation or defect which would result in a threshold failure would also result in the catastrophic failure of other tests.

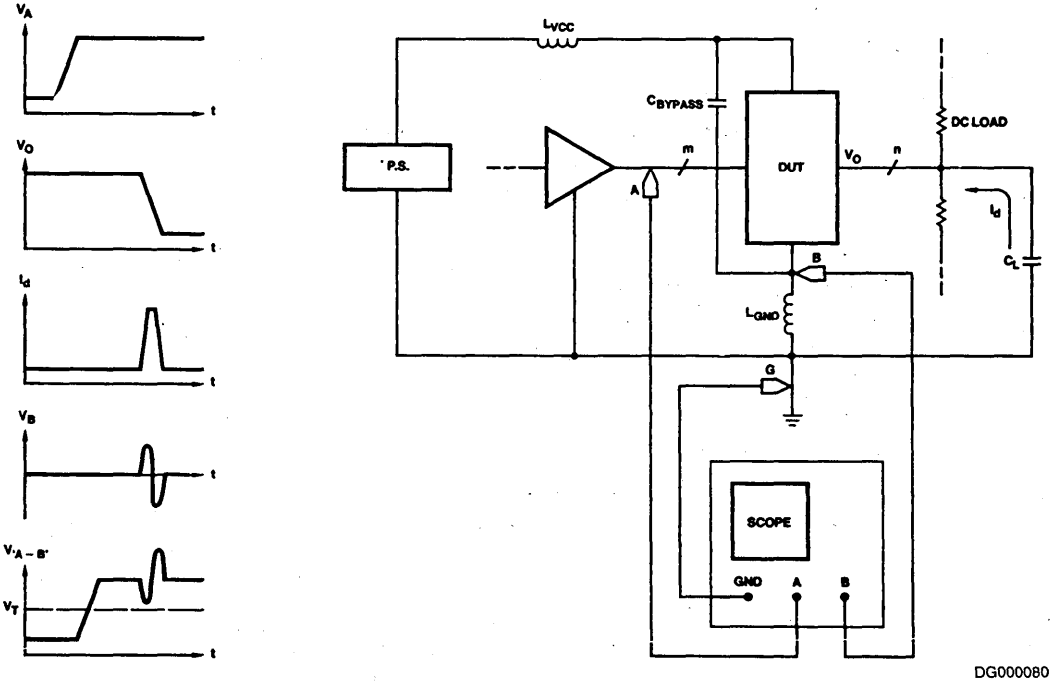



**Figure 8. Monitoring Ground Noise**

- DC verification of $V_{IL}$ and $V_{IH}$ can also be performed on the test system, but care must be exercised to insure that input voltages NEVER cross through the 0.8V to 2.0V window; voltages residing in this window can cause the DUT to switch, triggering sustained oscillations.

- The Output "Tank Circuit": A second common problem encountered is resonance in the circuitry which connects the DUT outputs to the output comparators or receivers. This resonance occurs because the wire connecting the DUT outputs to the receivers is actually an inductor connected in series with the comparator input capacitance, forming a series resonant tank circuit (Figure 9). This load circuit is quite different from the typical loading situation found in a system environment. Notice that the capacitance in the tester tends to be a single large value of capacitance, lumped at the end of the DUT output drive line. The load capacitance in the system is generally smaller and it is distributed along the drive line; this configuration looks much more like a transmission line, with per unit length values of inductance and capacitance, than it does a resonant tank. The resonant frequencies found at the test site vary with wire length and capacitive load, but tend to be in the 100 – 500MHz range. The input voltage sensed by the receiver is actually the voltage at the center connection within the tank circuit, which can ring violently when the outputs switch; measurement errors of 5ns or more can occur. A good evaluation technique for this problem is to compare the waveforms observed at the output of the device with a "shmoo plot" of the output. Assuming a simple pattern is used, differences in these results may indicate a resonance problem.

Corrective action for this problem includes:

- Use short, low inductance connections from the DUT output to the receiver; minimize comparator and interconnect capacitance. Both techniques raise the resonant frequency of the tank circuit which limits the time measurement error and reduces the DUT's ability to stimulate ringing in the tank.

- Use twisted pair wiring techniques to connect DUT outputs to the receivers. Though this raises the capacitance slightly, it reduces the purely inductive character of the interconnect, usually tending to reduce ringing.

- Minimizing Cross-Talk: Cross-talk between the input and output lines of the DUT is also a common problem. Obviously, the greater the number of paths which must be packed into a given area, the greater the problem. The signal coupling that occurs adds noise to both the input lines, making $V_{IH}$ and $V_{IL}$ testing difficult, and output lines, reducing the accuracy of timing measurements. Techniques which tend to reduce cross-talk include the following:

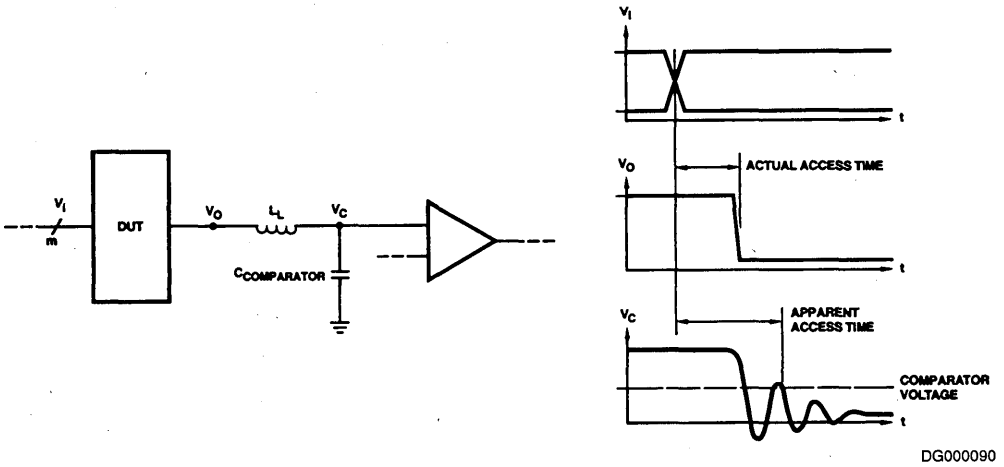
  - Keep wires as short as possible and avoid laying wires on top of each other.

  - Reduce output loading to minimize the magnitude of current transients which could be coupled into adjacent lines.

  - Use twisted pair or coaxial cable wherever possible; take care to tie all grounds from these transmission lines together at both ends.

  - Use ground plane or ground mesh techniques in the load board and the handler interface if possible. A true ground plane permits the use "strip" transmission lines which not only minimize cross-talk, but also reduce ground noise.

Though expensive, ground plane techniques offer the test engineer a consistent reference voltage which can be used to identify and segregate the various components and sources of noise.




$L_L$, the interconnect inductance and $C_{COMPARATOR}$ form a series resonant tank circuit which can cause time measurement errors.

**Figure 9. Resonance of the Outputs**

## Conclusion

Advanced Micro Devices has invested significantly in the development of advanced, high-performance bipolar memory technologies and products. As the preceding discussion demonstrates, the memory tester presents a very different environment to the memory device than does the system. The additional constraints placed on the tester virtually guarantee that devices which function in this "worst case" environment will perform satisfactorily in the system. However, this worst case environment may also selectively reject the best performing devices; i.e., those with the fastest access times and best drive characteristics. This occurs because high-perfor-

mance devices magnify the problems found in the tester environment. The information presented here should aid the component engineer in recognizing and resolving these special test environment problems. Attention to these details will reward the bipolar memory user by assuring acceptance of the best and broadest range of bipolar memories currently available.

# Bipolar Programmmable Read Only Memory (PROM) Index

# Guide to the Programming of AMD's Generic Bipolar PROMs

Application Note
by
AMD Bipolar Memory Product Engineering



## GENERIC SERIES CHARACTERISTICS

The AMD line of Generic Bipolar PROMs incorporate common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

## PROM Programming Equipment Guide

| **Source and Location** | Data I/O 10525 Willows Rd. N.E. Redmond, WA 98052 | | Pro-Log Corporation 2411 Garden Road Monterey, CA 93940 | International Microsystems, Inc. 11554 C. Avenue Auburn, CA 93940 | Kontron Electronic, Inc. 630 Price Avenue Redwood City, CA 94063 | Digelec, Inc. 7335 E. Acoma Dr. Scottsdale, AZ 85260 | | Stag Systems, Inc. 528-5 Weddell Dr. Sunnyvale, CA 94086 |
|---|---|---|---|---|---|---|---|---|
| **Programmer Model(s)** | Model 5, 7 and 9 Systems 17, 19, 29 and 100 | | M900, M900B, M910, M920 and M980 | IM1010 | MPP-80 | UPP-801 | UPP-803 | PPX |
| **AMD Generic Bipolar PROM Personality Module** | 909-1286-1 919-1286-1 Rev H | Unipak Rev 003 (Family and Pin Code) | PM 9058 | IM AMDGEN1 | MOD 14 | PM 102 | FAM-12 | PM 2000 Code 90 |
| **Socket Adapters and Configurators** | | | | | | | | |
| Am27S18/19 Am27LS18/19 | 715-1407-1 | 16 02 | PA 16-6 and 32 x 8(L) | IM 32 x 8-16-AMD | SA 3-1 B 32 x 8/16 | DIS-156 AM | DA 22 | AM 110-2 |
| Am27S20/21 | 715-1408-1 | 16 01 | PA 16-5 and 256 x 4(L) | IM 256 x 4-16-AMD | SA 4-2 B 256 x 4/16 | DIS-133 AM | DA 21 | AM 130-2 |
| Am27S12/13 | 715-1408-2 | 16 03 | PA 16-5 and 512 x 4(L) | IM 512 x 4-16-AMD | SA 4-1 B 512 x 4/16 | DIS-134 AM | DA 21 | AM 130-3 |
| Am27S15 | 715-1411-1 | | PA 24-14 and 512 x 8(L) | IM 512 x 8-24-27S15-AMD | SA 17-3 B 512 x 8/24 | DIS-165 AM | DA 33 | |
| Am27S25 | 715-1617 | 62 65 | PA 24-16 and 512 x 8(L) | IM 512 x 8-24-27S25-AMD | SA 31-2 B 512 x 8/24 | DIS-213 AM | DA 31 | AM 190-2 |
| Am27S27 | 715-1412-2 | | PA 22-4 and 512 x 8(L) | IM 512 x 8-22-27S27-AMD | SA 18 B 512 x 8/22 | DIS-168 AM | DA 28 | |
| Am27S28/29 | 715-1413 | 16 09 | PA 20-4 and 512 x 8(L) | IM 512 x 8-20-AMD | SA 6 B 512 x 8/20 | DIS-158 AM | DA 34 | AM 120-3 |
| Am27S30/31 | 715-1545 | 16 36 | PA 24-13 and 512 x 8(L) | IM 512 x 8-24-AMD | SA 22-6 B 512 x 8/24 | DIS-135 AM | DA 29 | |
| Am27S32/33 | 715-1414 | 16 38 | PA 18-6 and 1024 x 4(L) | IM 1024 x 4-18-AMD | SA 24 B 1024 x 4/18 | DIS-136 AM | DA 38 | AM 170-2 |
| Am27S35 Am27S37 | 715-1723 | 62 66 | PA 24-18 and 1025 x 8(L) | IM 1024 x 8-27S35/37-AMD | SA 31-1 B 1024 x 8/24 | DIS-218 AM | DA 65 | AM 190-3 |
| Am27S180/181 Am27PS181 | 715-1545-2 | 16 37 | PA 24-13 and 1024 x 8(L) | IM 1024 x 8-24-AMD | SA 22-7 B 1024 x 8/24 | DIS-137 AM | DA 29 | AM 100-6 |
| Am27S280/281 Am27PS281 | | 16 37 | | IM 1024 x 8-24-27S280/281-AMD | | DIS-214 AM | DA 60 | |
| Am27S184/185 Am27LS184/185 Am27PS185 | 715-1616 | 16 06 | PA 18-8 and 2048 x 4(L) | IM 2048 x 4-18-AMD | SA 4-4 B 2048 x 4/18 | DIS-211 AM | DA 23 | AM 140-3 |
| Am27S190/191 Am27PS191 | 715-1688-1 | 16 68 | PA 24-17 and 2048 x 8(L) | IM 2048 x 8-24-AMD | SA 22-10 B 2048 x 8/24 | DIS-151 AM | DA 61 | AM 100-5 |
| Am27S290/291 Am27PS291 | 715-1688-2 | 16 68 | PA 24-28 and 2048 x 8(L) | IM 2048 x 8-24-27S290/291-AMD | SA 29 B 2048 x 8/24 | DIS-215 AM | DA 62 | AM 190-7 |
| Am27S40/41 Am27PS41 | 715-1282 | | PA 20-9 and 4096 x 4(L) | IM 4096 x 4-20-AMD | SA 30 B 4096 x 4/20 | DIS-216 AM | DA 63 | AM 120-6 |
| Am27S45 Am27S47 | 715-1660 | | | IM 2048 x 8-24-27S45/47-AMD | SA 31 B 2048 x 8/24 | | DA 64 | AM 170-3 |
| Am27S43 | 715-1698-002 | | | IM 4096 x 8-24-AMD | | | | |



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## PROGRAMMING

The entire Generic PROM Series is manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50μsec, the 20 volt supply is removed, the chip is enabled, and the output level sensed to determine if the link has opened. Most links will open within 50μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5msec. If a link has not opened after a total elapsed programming time of 400msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 180mA until the fuse link is opened, after which the current drops to approximately 90mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including $V_{CC}$ should be removed for a period of 5 seconds after which programming may be resumed.

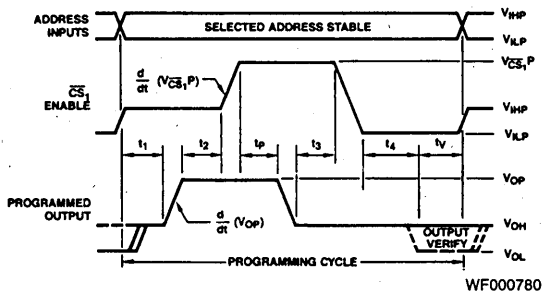
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

## PROGRAMMING PARAMETERS

| Symbol | Parameters | Min | Max | Units |
|---|---|---|---|---|
| $V_{CCP}$ | $V_{CC}$ During Programming | 5.0 | 5.5 | Volts |
| $V_{IHP}$ | Input HIGH Level During Programming | 2.4 | 5.5 | Volts |
| $V_{ILP}$ | Input LOW Level During Programming | 0.0 | 0.45 | Volts |
| $V_{\overline{CS}_1P}$ | $\overline{CS}_1$ Voltage During Programming | 14.5 | 15.5 | Volts |
| $V_{OP}$ | Output Voltage During Programming | 19.5 | 20.5 | Volts |
| $V_{ONP}$ | Voltage on Outputs Not to be Programmed | 0 | $V_{CCP}$ + 0.3 | Volts |
| $I_{ONP}$ | Current into Outputs Not to be Programmed | | 20 | mA |
| $d(V_{OP})/dt$ | Rate of Output Voltage Change | 20 | 250 | V/μsec |
| $d(V_{\overline{CS}_1})/dt$ | Rate of $\overline{CS}_1$ Voltage Change | 100 | 1000 | V/μsec |
| $t_P$ | Programming Period — First Attempt | 50 | 100 | μsec |
| | Programming Period — Subsequent Attempts | 5.0 | 15 | msec |

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays $t_1$, $t_2$, $t_3$ and $t_4$ must be greater than 100ns; maximum delays of 1μsec are recommended to minimize heating during programming.
3. During $t_V$, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to $V_{ONP}$ through resistor R which provides output current limiting.

## PROGRAMMING WAVEFORMS

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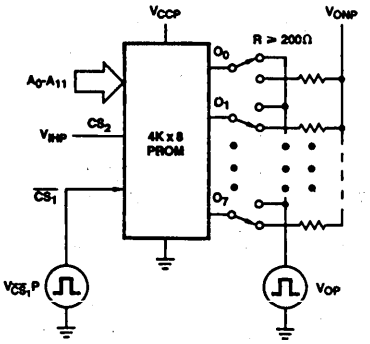
## SIMPLIFIED PROGRAMMING DIAGRAM

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## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ASCII BPNF

An example of an ASCII type in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 2048 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output $O_7$.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.5 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

## TYPICAL PAPER TAPE FORMAT

| | | |
|---|---|---|
| ØØØ | BPNPPNNNPF | WORD ZERO Ⓡ Ⓛ |
| | BPPPPPPNNF | COMMENT FIELD Ⓡ Ⓛ |
| Ø02 | BNNNPPPPNF | ANY Ⓡ Ⓛ |
| | BNNNNNNNNF | TEXT Ⓡ Ⓛ |
| Ø04 | BPNNNNNNPF | CAN Ⓡ Ⓛ |
| | BNPPNPPNNF | GO Ⓡ Ⓛ |
| Ø06 | BPNNPPPNNF | HERE Ⓡ Ⓛ |
| • | • | • |
| 2047 | BNNNPPPNNF | END Ⓡ Ⓛ |

Ⓡ = CARRIAGE RETURN
Ⓛ = LINE FEED

AF000100

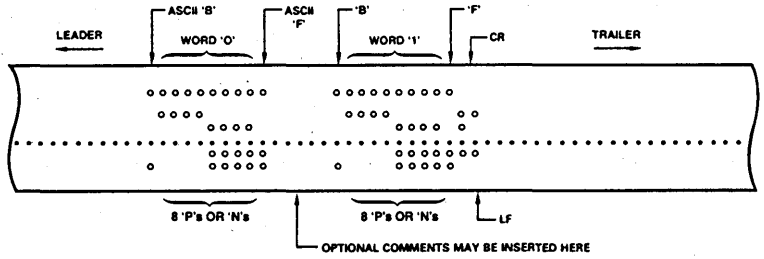
## RESULTING DEVICE TRUTH TABLE

## ($\overline{CS}_1$ LOW AND $CS_2$ $CS_3$ HIGH)

| $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $O_7$ | $O_6$ | $O_5$ | $O_4$ | $O_3$ | $O_2$ | $O_1$ | $O_0$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | L | L | L | L | L | L | L | L | L | L | H | L | H | H | L | L | L | H |
| L | L | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | L | L |
| L | L | L | L | L | L | L | L | L | H | L | L | L | L | H | H | H | H | L |
| L | L | L | L | L | L | L | L | L | H | H | L | L | L | L | L | L | L | L |
| L | L | L | L | L | L | L | L | H | L | L | H | L | L | L | L | L | L | H |
| L | L | L | L | L | L | L | L | H | L | H | L | H | H | L | H | H | L | L |
| L | L | L | L | L | L | L | L | H | H | L | H | L | L | H | H | H | L | L |
| | | | | | | • | | | | | | | | • | | | | |
| H | H | H | H | H | H | H | H | H | H | H | L | L | L | L | H | H | H | L |

AF000110

## ASCII PAPER TAPE

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# Guide to the Analysis of Programming Problems

Application Note
by
AMD Bipolar Memory Product Engineering

## INTRODUCTION

Advanced Micro Devices' Generic Series of Programmable Read Only Memory (PROM) circuits have been designed to provide extremely high programming yields. Available programming currents are over designed by a factor of four and special circuitry accessible only during testing is incorporated into each product to eliminate ordinarily difficult to detect shorts and opens in the array and decoders. As a result, unique decoding and very large fusing currents are virtually assured to the user. AMD PROMs have test fuses programmed prior to shipment as a further guarantee. The results of such extensive testing and design considerations are programming yields consistently in the 98% to 99.5% range.

Key to the achievement of such yields is a programmer properly calibrated to the AMD specification with good contactors, "clean" electrical wave forms and properly functioning subcircuits. In the event that your programming yields fall below 98%, you should investigate the characteristics of the failed devices to find a prominent failure mode, then use the attached information as a guide to resolving the problem. Simple problems can be very costly if not detected and corrected.

Should you continue to have trouble optimizing your programming yield, contact your AMD representative or local programmer manufacturer representative.

## Guide to the Analysis of Programming Problems

| Primary Symptom | Secondary Symptom | Possible Causes |
|---|---|---|
| I) Units fail to program all desired bits | A) Binary blocks of missing data | 1) Address driver output which remains continuously low or continuously high.<br>2) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V.<br>3) Poor, intermittent or no electrical contact to one or more address input pins.<br>Any of the above may result in over programming half the array and not programming the other half. |
| | B) Random bits of missing data | 1) Address driver with a "low" voltage greater than 0.5V or a "high" voltage less than 2.4V.<br>2) Poor electrical contact to address, chip enable and output pins.<br>3) Excessive transient noise on $V_{CC}$, output pin ( > 20.5V), or ground pins. Check with a high speed storage oscilloscope for peak values during programming. Use transient suppression networks where appropriate.<br>4) Programmer does not comply with AMD Programming Specification. (See Programming Parameters.)<br>Examples:<br>— Output voltage during programming less than 19.5V<br>— $V_{CC}$ during programming less than 5.0V<br>— $\overline{CS}$ voltage during programming less than 14.5V |
| | C) All data associated with a single output missing | 1) Poor or no electrical contact to that output pin.<br>2) Defective current switch in programmer. |
| | D) No data change | 1) Wrong device or programming socket.<br>2) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.)<br>Examples:<br>— Output voltage during programming less than 19.5V<br>— $V_{CC}$ during programming less than 5.0V<br>— $\overline{CS}$ voltage during programming less than 14.5V |

| Primary Symptom | Secondary Symptom | Possible Causes |
|---|---|---|
| II) Over-Programmed Devices | A) One output continuously at a Logic "1" | 1) Programmer does not comply with AMD's Programming Specifications. (See Programming Parameters.)<br>Examples:<br>— Output voltage during programming greater than 20.5V<br>— Programmer timing incorrect |
| | | 2) Open outputs can appear to be programmed to Logic "1" with the presence of a pullup resistor even though the device has not actually been programmed. |
| | | 3) Excessive voltage transients on output lines during programming. Be sure appropriate transient suppression networks are placed on the outputs. (See Figure 1.) |
| | B) All outputs continuously at a Logic "1" | 1) No $V_{CC}$ applied to device. |
| | | 2) No ground applied to device. |
| | | 3) Incorrect device type. |
| | | 4) Incorrect programming socket. |
| | | 5) Excessive voltage transients on output lines. Use transient suppression network shown in Figure 1. |

## DEFINITIONS

**Fuse**

— Conductive Platinum-Silicide link used as a memory element in Advanced Micro Devices' PROM circuits.

**Unprogrammed Bit**

— A conductive fuse.

**Programmed Bit**

— A nonconductive fuse, that is one which has been opened.

**Output Low (Logic "0")**

— An output condition created by an unprogrammed bit.

**Output High (Logic "1")**

— An output condition created by a programmed bit.

**Failure to Program**

— A device failure in which a fuse selected to be opened failed to open during the fusing operation.

**Over Programmed**

— A device failure in which a fuse which was not selected to open nevertheless opened during the fusing operation.

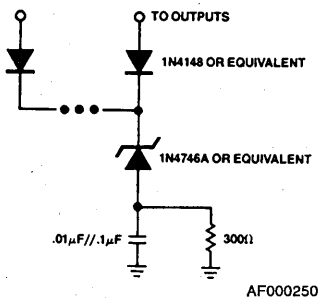
**Address Driver**

— The voltage source which drives an individual address pin in the PROM. This source is part of the programmer and drives the address pin with "0"s (0V to .45V) and "1"s (2.4V to 5.5V) depending on instructions from the programmer control circuitry. There is a separate address driver for every PROM address pin.

**Programmer**

— A system capable of providing the appropriate array of signals to a PROM circuit to cause certain user controlled bits to be programmed (i.e., fuses opened) in the device. As a minimum it consists of a memory containing the pattern to be programmed, control circuitry to sequence the addressing and fusing control pulses, power supplies, and address drivers.

**TRANSIENT SUPPRESSION NETWORK**

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Notes: 1. Clamp diodes should be connected to each output as close as physically possible to the device pin.
2. $V_{CC}$ should be decoupled at the device pin using .01μF//.1μF capacitors.
3. AMD recommends that all address pins be decoupled using .001μF capacitors.

## SUMMARY

The Advanced Micro Devices' bipolar memory process has been described with particular emphasis on programmable-read-only memories. An advanced form of the low-power Schottky process is used in conjunction with a highly reliable and stable platinum silicide fuse. Extensive testing and screening have been used to assure that the products will meet all specification after the user has placed his program into the device and that the circuit reliability will be outstanding.

The purpose of this report is to present a description of Advanced Micro Devices' Bipolar PROM circuits, their manufacturing process and their reliability. Included is a discussion of the wafer fabrication in which an advanced, highly reliable platinum silicide fuse is utilized, a description of the circuits and their testing, an analysis of the fusing characteristics of platinum silicide and supportive reliability data.

The products evaluated in this report are members of a generic family of field programmable-read-only memories (PROMs) from 256 bits through 16384 bits. Advanced Micro Devices utilizes two manufacturing processes. The first is the platinum-silicide Schottky, washed emitter process described in this report. The second is the IMOX™process. IMOX is the trademark name for a selective oxide isolation process which employs ion-implantation of various transistor elements. This improved process incorporates many of the technologies previously developed, such as platinum silicide fuses, dual layer metal, and platinum-silicide Schottkies. IMOX allows further reduction in chip size due to tighter device spacings and device dimensions. All new product developments for the PROM family use the IMOX process. This high density process allows Advanced Micro Devices to continue to supply very high speed, high performance products while increasing device complexity. The circuit design concepts are similar on each of the PROMs with the result that the products can be programmed using the same hardware. Only the socket adaptor required for the PROM configuration and pin count is different. The same programming algorithm is used for all devices with completely satisfactory results. The PROMs utilize a platinum Schottky diode structure with barrier metal. Dual-layer metallization is also employed to maximize speed and minimize chip size. All Advanced Micro Devices' circuits receive screening per MIL-STD-883, Method 5004 class C or better. Part of the 883 flow involves sample acceptance tests in which all temperature requirements are sampled to Lot Tolerance Percent Defective (LTPD) plans. A 5% LTPD corresponds to about a 0.65% Acceptance Quality Level (AQL). In late 1983, Micro Devices announced a new program that guarantees the highest quality levels for semiconductor devices in the industry. The new program is called INTERNATIONAL STANDARD 1000. Under INT-STD-1000 all Bipolar Memory PROMs are sampled to a 0.1% AQL. This is a statement of AMD's commitment to excellence.

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## THE PROCESS TECHNOLOGY

Advanced Micro Devices has chosen a platinum silicide Schottky, washed emitter, dual-layer metal process for its bipolar PROMs. Platinum silicide has been chosen as the material to form the fuse for several reasons. First, it has been demonstrated to be an extremely reliable fuse material. It does not have the growback phenomenon common to nichrome technologies; it is not moisture sensitive in freeze-out tests; it is less fragile than nichrome and it does not have mass transport problems associated with moderate current densities. Second, the manufacturing process is easily controlled with regard to reliability factors and fusing currents. Third, the fuses are quite easy to form during the manufacturing process without a substantial number of additional processing steps.

Figure 2 is a cross section of a transistor and a fuse. A heavily doped buried layer diffusion is first performed to allow for the fabrication of NPN transistors with low saturation resistances. A thin epitaxial layer is grown followed by isolation and base diffusions. The isolation and base are effectively self-aligned using a composite masking approach. A short series of steps results in the definition of polycrystalline silicon in the shape of the fuse.

A second composite mask now defines all the emitter, contact, Schottky diode and ohmic contact areas.

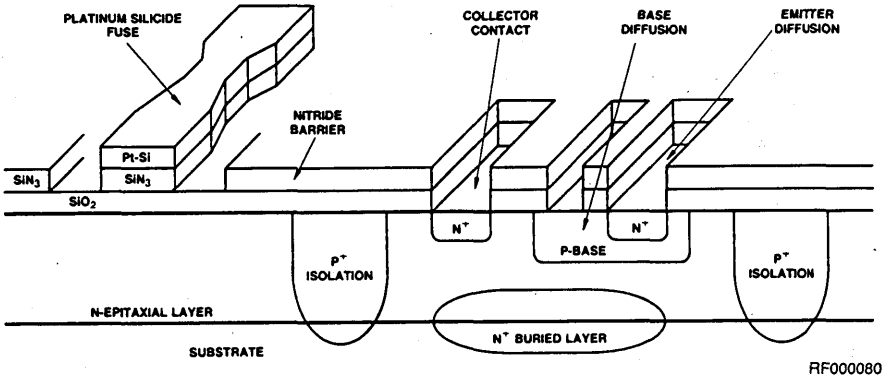


**Figure 2. Transistor & Fuse Structures.**

Following the emitter diffusion and the contact mask, platinum is sputtered over the entire wafer. Since all contacts, Schottkies and fuses are exposed at this point, an alloying operation allows platinum silicide to form. The residual platinum is etched off the wafer leaving the silicide contacts, Schottkies, and fuses. After this step, the semiconductor elements of the circuit have been completely formed, and all that remains is the interconnect metallization.

To form the interconnects, aluminum is used as the primary conducting element. Aluminum has a very strong affinity for silicon, including that in platinum silicide. To retain the advantages of the very stable platinum silicide Schottky devices, it is necessary to sputter an inactive metal, tungsten, with a small amount of titanium as a bonding agent over the surface of the wafers to serve as a barrier to the diffusion or microalloying of the aluminum. Aluminum is now evaporated over the surface of the wafers and conventional masking and

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etching cycles are used to define the aluminum interconnections. Figure 3 shows the structure of this metal layer.

To complete the dual-layer metallization structure, silicon dioxide is chemically vapor deposited on the wafer and etched with interlayer metal contact openings (vias). A second layer of aluminum is then placed on top of the dielectric. This layer has a thickness substantially greater than the first one and is especially suited for power busses and output lines.

To complete the circuit, a passivation layer is deposited over the top of the wafers and etched at the appropriate locations to allow for bonding pad contact.

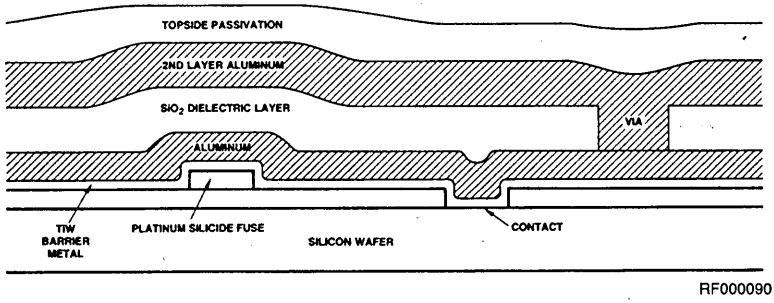



**Figure 3. 2 Layer Metallization Structure.**

## PROGRAMMABLE READ-ONLY MEMORY CIRCUITRY

Advanced Micro Devices' bipolar PROM designs have the general configuration shown in Figure 4. Although the figure is for that of the Am27S20, the circuit techniques are the same for the entire generic family of PROMs.

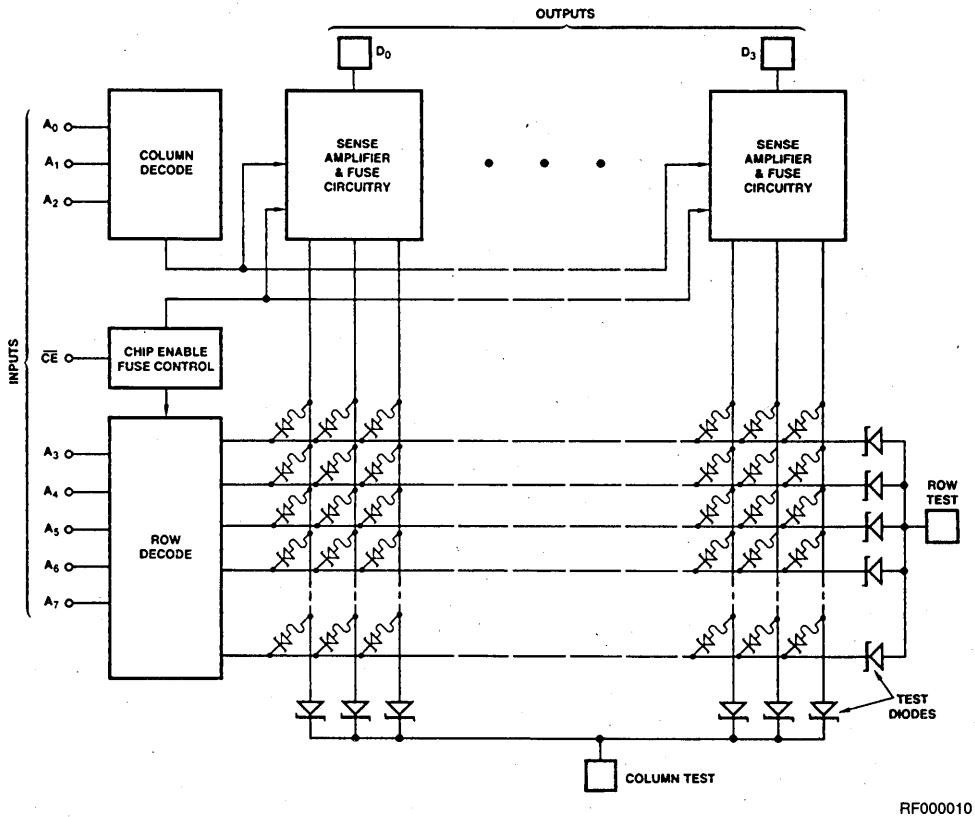



**Figure 4. PROM Circuitry Block Diagram**

### Input, Memory & Output Circuitry

Two groups of input buffers and decoders called "X" and "Y" are used to drive word lines and columns respectively. The X-decode addresses ($A_3 - A_7$) have Schottky clamp diode protected, PNP inputs for minimum loading. (Figure 5). The X-input buffers ($A_3 - A_7$) provide A and $\overline{A}$ outputs to a Schottky decode matrix which selects one of 64 word drivers. The word line drivers are very fast high current, high voltage, non-saturating buffers providing voltage pull down to the selected word line.

The Y-decode address buffers ($A_0 - A_2$) are also Schottky diode clamped, PNP inputs driving a Schottky diode matrix. However, this diode matrix selects one of eight columns on each of the four output bits. The selected column line drives the sense amplifier input to a high level in the case of a blown fuse, or current is shunted through an unblown fuse through the selected word driver to ground resulting in a "low" input to the sense amplifier.

The sense amplifier is a proprietary fast level shifter-inverter with temperature and voltage threshold sensitivities compensated for the driving circuitry. Each of the four sense amplifiers in this circuit provides active drive to an output buffer.

Each output buffer also contains a disable input, which is driven from the chip-enable buffer. The chip-enable buffer input is a Schottky diode clamped PNP buffered design with an active pull up and pull down to drive the output buffer. Additionally, the chip-enable gate contains circuitry to provide fuse control as described below.

### Fusing Circuitry

Platinum silicide fuses as implemented in Advanced Micro Devices' PROMs have extremely high fuse current to sense current ratios. Sensing normally requires that only a few hundred microamps flow through the fuse, whereas absolute minimum requirements for opening the fuse are approximately 100 times that amount. This provides a significant safety margin for transient protection and long-term reliability.

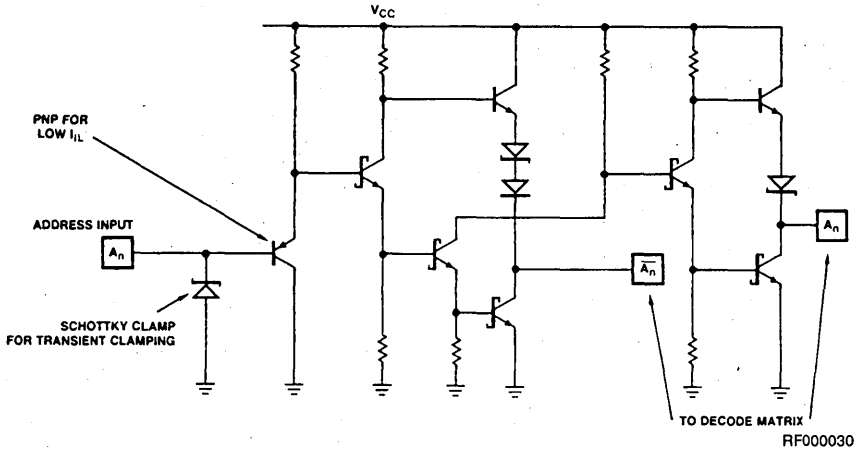



**Figure 5. Input Buffer Schematic**

High-yield fusing of platinum silicide fuses requires that a substantial current be delivered to each fuse. This current is sourced from the output terminals through darlingtons which can drive the column lines when enabled. These darlingtons are driven directly from the output and are selected by the Y-decode column select circuitry. Current during fusing flows from the output through the darlington directly to the fuse through the selected array Schottky and finally through the word-driver output transistor to ground. This path is designed for a very large fusing current safety margin.

The control circuitry works as follows: After $V_{CC}$ is applied, the appropriate address is selected and the $\overline{CE}$ input is taken to a logic high, the programmer applies 20 volts to the bit output to be programmed. The application of the 20 volts simultaneously deselects the output buffer to prevent destructive current flow, and powers down internal circuitry unneeded during fusing to minimize chip heating.

It also enables the darlington base drive circuitry, makes power available to the darlington from the output and enables the fusing control circuitry. At this point, the PROM is ready for the control line at the chip-select pin to release the selected word driver to allow current flow through the fuse. This technique is particularly advantageous because the control signal does not supply the large fusing currents. They are supplied through the darlington from the output power supply. Some care must be taken to avoid excessive line inductance on the output line. Reasonable and normal amounts of care will reward the user with high-programming yields.

### Special Test Circuitry

All Advanced Micro Devices PROMs include high-threshold voltage gates paralleling several address lines to allow the selection of special test words and the deselection of the columns to allow for more complete testing of the devices. Additionally, special test pads accessible prior to assembly allow for testing of some key attributes of the devices. The function of these special circuits will be described in more detail in the section, "Testing", later in this report.

## THE PLATINUM SILICIDE FUSE

### Fusing Technique

Advanced Micro Devices' PROM circuits have been designed to use a programming algorithm which minimizes the requirements on the programmer yet allows the circuit to fuse the platinum silicide links quickly and reliably. Specifically, the following sequence of events must take place:

1. $V_{CC}$ power is applied to the chip;
2. The appropriate address is selected;
3. The chip is deselected;
4. The programming voltage is applied to one output;
5. The chip enable voltage is raised to enable high-threshold voltage gate. This action gates the current flow through the proper fuse resulting in an open fuse in a few microseconds;
6. The output voltage is lowered; the programming voltage is removed.
7. The device is enabled and the bit is sensed to verify that the fuse is blown. In the unusual event that the fuse does not verify as blown, a sequence of much longer pulses is applied to the fuse at a high duty cycle until the fuse opens; and,
8. The sequence of 2 through 7 is repeated for each bit which must be fused.

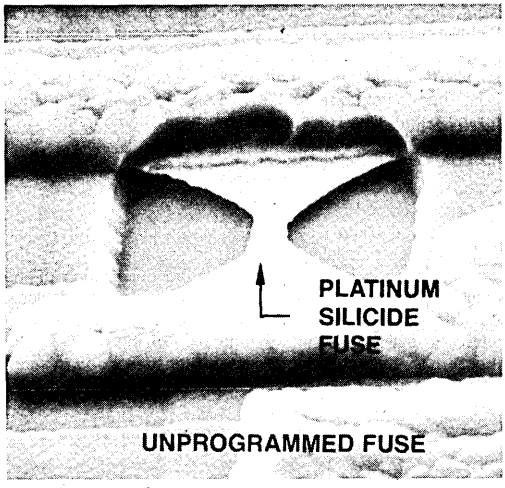
There are several advantages to this technique. First, the two high current power sources, $V_{CC}$ and the voltage applied to the output do not have critical timing requirements. The low current chip select pin gates the fusing current into the circuit. Since it is generally desirable to gate the fusing current into the chip at relatively fast rates, the use of the chip select for this purpose avoids the speed trade-off which would exist using the output voltage as the control. The output voltage must not be raised too quickly to avoid breakdown and latchback conditions which might occur with sub-microsecond rise times on the output.

The second major advantage of this technique is that in the event that the fuse does not open during the first attempt to blow it, a near DC condition may be safely applied to it with no danger of developing a reliability problem such as that which occurs with nichrome fuses. This will be discussed in more detail later. The algorithm can therefore be designed first to minimize the time required to program the PROM, i.e. with a fast first pulse, and second, to maximize the probability that any circuit will program. Most PROMs do, of course, fuse satisfactorily with all short pulses. However, it is impossible for any manufacturer to guarantee absolutely that all fuses in all circuits receive 100 percent of the rated fusing current during programming.

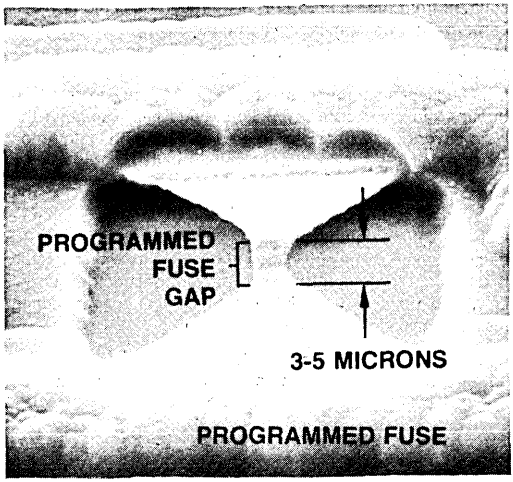
Circuit defects which may be resistant to pre-programming testing prevent such a guarantee. It is, therefore, quite important to have a fuse material insensitive to marginal conditions. Even the application of single, short pulses does not guarantee that no fuse received marginal amounts of current during fusing. The silicide fuse provides this safety margin and allows the programmer to maximize the possibility of fusing by applying near DC condition to the fuses.

### Fuse Characteristics

When a fast (less than 500ns rise time) current pulse is applied to a fuse, the fuse voltage rises abruptly to a value approaching the level anticipated from calculations of the room temperature resistance. However, it quickly falls to a value of approximately two volts. This value is nearly independent of the applied current. During this period of time, typically, the fuse is molten. Very abruptly, the fuse current drops to zero indicating the separation of the platinum silicide into two distinct sections. Scanning Electron Microscope photographs of the resulting fuses (see Figure 6) indicate that the typical case is a sharp, clean separation in excess of a micron. This separation occurs in the center of the fuse because the bow-tie structure (see Figure 7) concentrates the energy density in the center away from the aluminum lines. The energy density in the center of the fuse is capable of creating temperatures substantially greater than required to melt the silicide. The very abrupt, high power applied to the fuse melts the fuse center and results in a wicking of material on either side due to surface tension.




Unprogrammed Fuse




Programmed Fuse

Figure 6.

### Reliability of Fuses Programmed Under Non-optimal Conditions

The marginally opened fuse has been studied in some detail even though it rarely occurs in practice. Under conditions where the fuse is purposely blown at much slower rates, it is possible for the fuse to assume a high impedance state which is sensed as an open fuse by the circuit. This occurs because the fuse cools before separation is achieved. Electrical and SEM studies of fuses blown with these characteristics indicate that a small conductive path of silicon remains of sufficiently high resistance to prevent appropriate power transfer required for complete opening on subsequent applications of power. Under these slow-blow conditions, the thermal conductivity of the silicon nitride pedestal on which the fuse rests, the silicon dioxode beneath that and the silicon chip become factors because sufficient time exists for the heat flow to carry a significant amount of energy away from the fuse. This is extremely unusual in practice since it requires a rather narrow set of conditions. However, a number of PROMs have been specially programmed under these unusual conditions which can cause this type of fuse to occur. These devices have been life tested for over two thousand hours. No failures occurred in any of these circuits. It is clear from this study that partially opened platinum silicide fuses are stable. Although it is very rare to see such a fuse in a circuit which has been programmed under normal conditions, Advanced Micro Devices believes that such fuses do not represent a reliability hazard based on this study and the results of the other studies run on the programmable-read-only memories. It should be noted that most manufacturers carefully specify the conditions under which their devices *must* be programmed in order to avoid reliability problems. Reliability data available on these devices must be assumed to have been generated using optimally programmed devices. Advanced Micro Devices believes that the study described here and four billion fuse hours of data from many production lots of PROMs demonstrate the capability of the platinum silicide fuse under a wide variety of conditions.

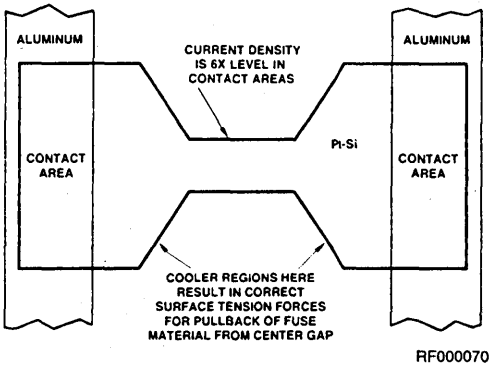



**Figure 7. Bowtie Fuse Design**

## FINAL TESTING OF ADVANCED MICRO DEVICES' MEMORIES

### Wafer Level Tests

In addition to all the standard DC tests, Advanced Micro Devices performs a series of special tests to conform to the screening of criteria of MIL-STD-883, Method 5004 3.3 and the 0.1% AQL INT-STD-1000. Also, AMD performs special tests to increase the confidence level of unique address selection and to demonstrate fusing capability on all columns and word drivers. To accomplish this, diodes are connected from the column lines and the word lines to special test pads which are accessible only during wafer probing. (See Figure 4). Using these diodes, Advanced Micro Devices confirms that each word driver is capable of sinking sufficient current to blow fuses, has appropriate saturation characteristics for AC performance, and has sufficient voltage breakdown to withstand fusing voltages. In addition, using special software, a sequence of tests dramatically increases the confidence of unique address selection on the address decoding. All darlingtons are checked to confirm that sufficient current drive is available to blow fuses from any column. Schottky diode array leakage is also checked to affirm that it is sufficiently low so as not to overload the pull down circuitry.during the high-voltage application of fusing. Finally, high voltages are applied to the inputs and outputs to remove potentially weak devices before the PROM's are assembled.

### Test Fusing

Each PROM has two additional word drivers connected to special test fuses. These test words are valuable in demonstrating beyond reasonable doubt that the device is capable of opening fuses in all columns. They also increase the confidence level in unique addressing. Furthermore, the test words serve as correlatable measures of the access times that the user can expect from his devices after he has placed his own program in the memory. These test words are not visible to the user unless he applies special voltages to certain address pins. Figure 8 is a diagram of this input circuit. One hundred percent of the PROM devices shipped from Advanced Micro Devices have had AC testing for access and enable times at high-and low-power supply voltages to affirm their AC characteristics.

The result of this extensive testing at both the wafer and finished device level is a product with very high-programming yields and virtually guaranteed AC performance after the user places his program in the parts. Additionally, the high voltage tests provide an additional level of confidence that the oxide and junction integrity is excellent in each circuit and that the devices will be relatively insensitive to small transients common to programming equipment.

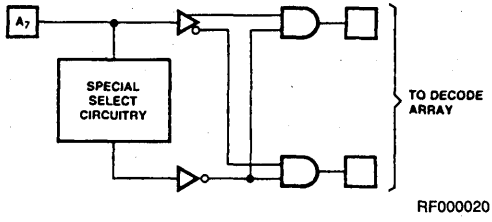
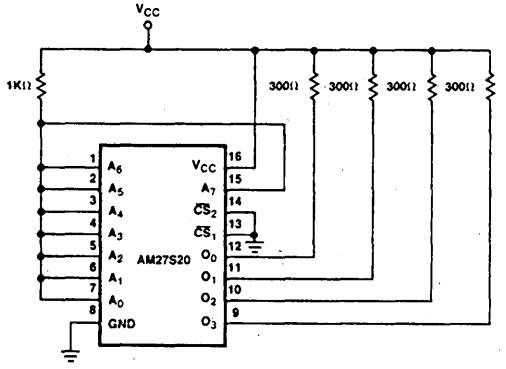



**Figure 8. Special Input Circuit Used for Array Deselection and Test Word Check.**

## RELIABILITY TESTING

Advanced Micro Devices has an ongoing reliability program to evaluate its bipolar memory products. Reliability testing conforms to MIL-STD-883 Method 1005 Condition C. Examples of the test circuits used are shown in Figure 9. Data has now been accumulated on the process described here in excess of ten thousand hours on some devices. Over forty billion fuse hours have been completed with no fuse oriented failures

Advanced Micro Devices selects samples of its product stratified by product type at periodic intervals for this testing. Figure 10 is a tabulation of the results of the lots placed on test during this period of time. The data demonstrates a highly reliable process. The fuse has an immeasurably low contribution to the failure rate at this point in the reliability testing.

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**Condition C – Static**

## BIPOLAR MEMORY RELIABILITY SUMMARY

| Product | Production Lots | Units Tested | Total Unit Hours (thousands) | Total Fuse Hours (billions) | Unit Failures | Fuse Related Failures | Unit Failure Rate @ 60% Confidence %/1000 hrs at 125°C | Unit Failure Rate* @ 60% Confidence %/1000 hrs at 70°C |
|---|---|---|---|---|---|---|---|---|
| 27S18/19 (256 bit PROM) | 5 | 491 | 982 | .251B | 0 | 0 | 0.10 | 0.0010 |
| 27S20/21 (1K bit PROM) | 16 | 1321 | 2207 | 2.260B | 2** | 0 | 0.01 | 0.0001 |
| 27S12/13 (2K bit PROM) | 11 | 571 | 1840 | 3.768B | 0 | 0 | 0.05 | 0.0005 |
| 27S15 27S27 27S28/29 27S32/33 (4K bit PROM) | 24 | 1870 | 1408 | 5.767B | 0 | 0 | 0.07 | 0.0007 |
| 27S180/181 (8K bit PROM) | 12 | 463 | 926 | 7.586B | 0 | 0 | 0.11 | 0.0010 |
| 27S184/185 IMOX (8K bit PROM) | 15 | 556 | 1112 | 9.109B | 0 | 0 | 0.09 | 0.0008 |
| 27S190/191 IMOX (16K bit PROM) | 2 | 69 | 795 | 13.025B | 0 | 0 | 0.12 | 0.0011 |
| Totals for PROM products | 85 | 5341 | 9270 | 41.766B | 2** | 0 | 0.02 | 0.0002 |

* Assuming on activation energy of 1.0 eV.
** Oxide failure.

# Am27S12/13

512 x 4 Bit Generic Series Bipolar PROM



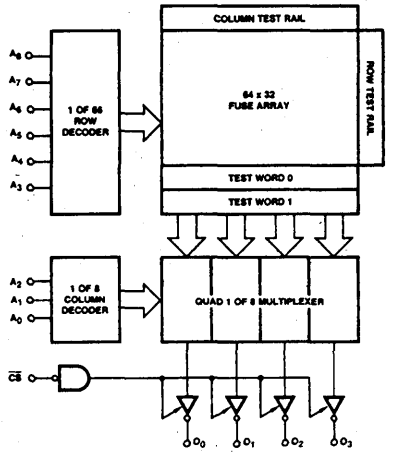
## DISTINCTIVE CHARACTERISTICS

- High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select

## GENERAL DESCRIPTION

The Am27S12A/12 and Am27S13A/13 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 4 configuration, they are available in both open collector Am27S12A/12 and three-state Am27S13A/13 output versions. After programming, stored information is read on outputs $O_0 - O_3$ by applying unique binary addresses to $A_0 - A_8$ and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, $O_0 - O_3$ go to the off or high impedance state.

## BLOCK DIAGRAM

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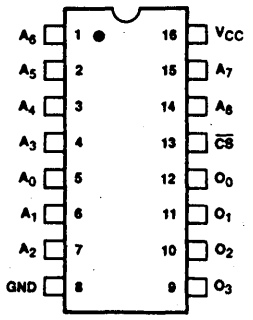
## PRODUCT SELECTOR GUIDE

| Access Time | 30ns | 40ns | 50ns | 60ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Open Collector | Am27S12A | | Am27S12 | |
| Three-State | Am27S13A | | Am27S13 | |

03208B

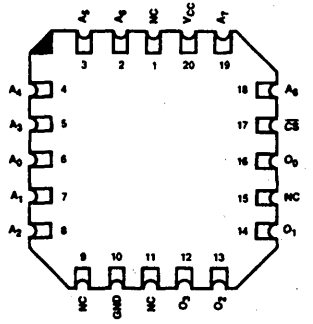
## CONNECTION DIAGRAM
Top View

### DIP




CD000590

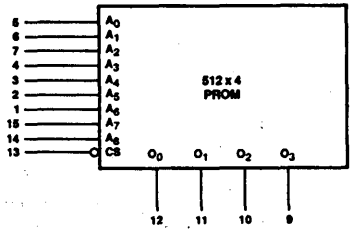
### Chip-Pak™ L-20-1




CD000600

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000090

$V_{CC}$ = Pin 16
GND = Pin 8

## ORDERING INFORMATION

Am27S12 A P C B

- B — Burn-in Option
  B suffix denotes 160 hour burn-in.
- C — Temperature
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- P — Package
  D – 16-pin ceramic DIP
  F – 16-pin flatpak
  L – 20-pin leadless chip carrier
  P – 16-pin plastic DIP
- A — Speed Select
  See Product Selector Guide
- Am27S12 — Device Type

Am27S12, Am27S12A — Open Collector

Am27S13, Am27S13A — Three state

| Valid Combinations | |
|---|---|
| Am27S12<br>Am27S12A<br>Am27S13<br>Am27S13A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

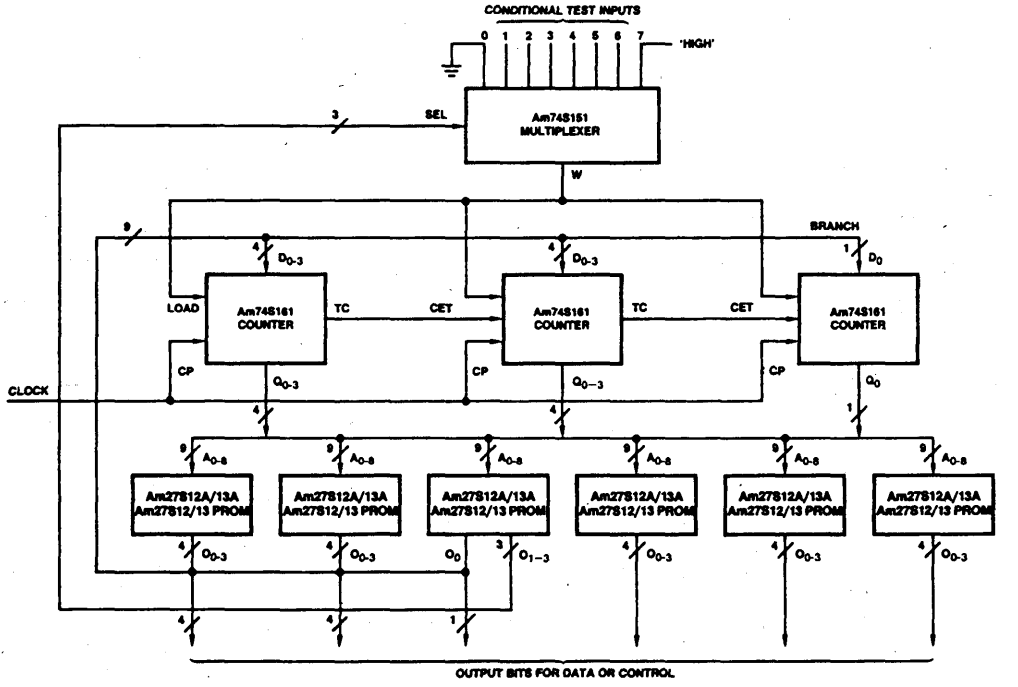
## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## APPLYING THE Am27S12A/12 AND Am27S13A/13

The Am27S12A/12 and Am27S13A/13 can be used with a high speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the Am27S12A/12 or Am27S13A/13 PROMs.




AF000240

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

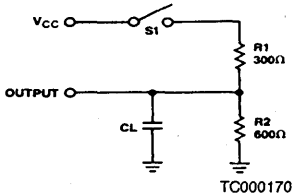
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.45 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | | 25 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND<br>$V_{CC}$ = MAX | | | | 100 | 130 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{CS}$ = 2.4V | (Note 2) | $V_O$ = 4.5V | | | 40 | µA |
| | | | | $V_O$ = 2.4V | | | 40 | |
| | | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | | 4 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | | 8 | | |

Notes:

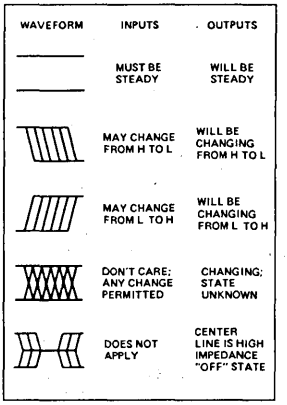
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORM




KS000010

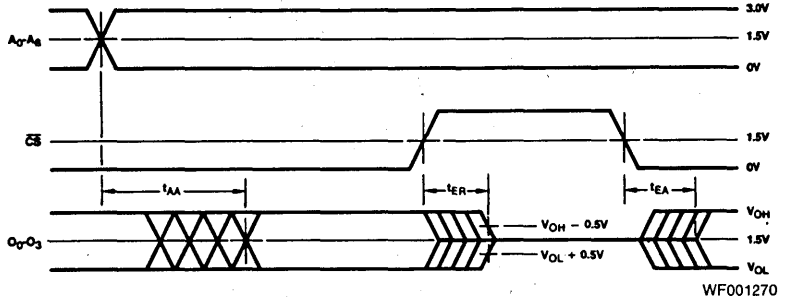
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 30 | 50 | | 30 | 60 | ns |
| | | | A | | 20 | 30 | | 20 | 40 | ns |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 15 | 25 | | 15 | 30 | ns |
| | | | A | | 15 | 20 | | 15 | 25 | ns |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 15 | 25 | | 15 | 30 | ns |
| | | | A | | 15 | 20 | | 15 | 25 | ns |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L = 30pF$.
2. For open collector outputs, $t_{EA}$ and $t_{ER}$ are tested with $S_1$ closed to the 1.5V output level. $C_L = 30pF$.
3. For three state outputs, $t_{EA}$ is tested with $C_L = 30pF$ to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L = 5pF$. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH} - 0.5V$; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL} + 0.5V$ level.

## SWITCHING WAVEFORMS




WF001270

Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S15

4096-Bit Generic Series Bipolar PROM
(512 x 8 Bits with Output Data Latches)

## DISTINCTIVE CHARACTERISTICS

- On-chip data latches
- Latched true and complemented output enables for easy word expansion
- Predetermined OFF outputs on power-up
- Fast access time — 60ns commercial and 90ns military maximum
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Member of generic PROM series utilizing standard programming algorithm

## GENERAL DESCRIPTION

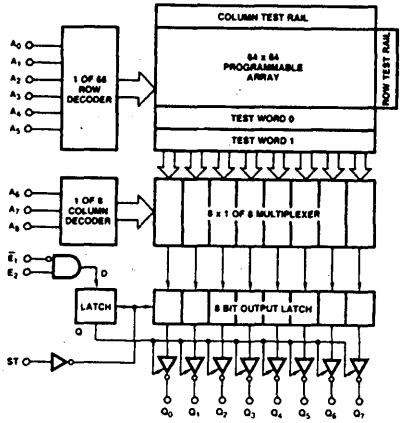
The Am27S15 is an electrically programmable Schottky read only memory incorporating on-chip data and enable latches. The device is organized as 512 words of 8 bits and features three-state outputs with full 16mA drive capability.

When in the transparent mode, with the strobe (ST) input HIGH, reading stored data is accomplished by enabling the chip ($\overline{E}_1$ LOW and $E_2$ HIGH) and applying the binary word address to the address inputs, $A_0 - A_8$. In this mode, changes of the address inputs cause the outputs, $Q_0 - Q_7$, to read a different stored word; changes of either enable input level disable the outputs, causing them to go to the high impedance state.

Dropping the strobe input to the LOW level places the device in the latched mode of operation. The output condition present (reading a word of stored data or disabled) when the strobe goes LOW remains at the outputs, regardless of further address or enable transitions, until a positive (LOW to HIGH) strobe transition occurs. With the strobe HIGH, $Q_0 - Q_7$ again respond to the address and enable input conditions.

If the strobe is LOW (latched mode) when $V_{CC}$ power is first applied, the outputs will be in the disabled state, eliminating the need for special "power-up" design precautions.

## BLOCK DIAGRAM

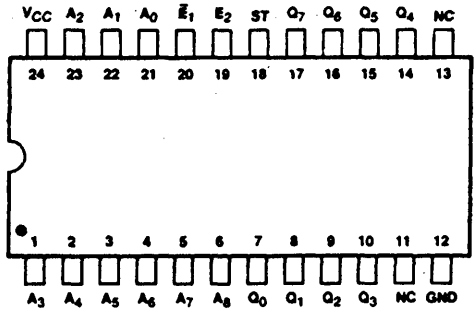



## PRODUCT SELECTOR GUIDE

| Access Time | 60ns | 90ns |
|---|---|---|
| Temperature Range | C | M |
| Part Number | Am27S15 | |

03183C

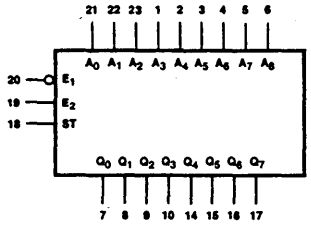
## CONNECTION DIAGRAM
### Top View




CD001010

Note: Pin 1 is marked for orientation. NC = No Connection

## LOGIC SYMBOL




LS000100

$V_{CC}$ = Pin 24
GND = Pin 12
(Pin 11 and 13 open)

## ORDERING INFORMATION

**Am27S15** **P** **C** **B**

- **B** — Burn-in Option
  B suffix indicates 160 hour burn-in.
- **C** — Temperature
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- **P** — Package
  D – 24-pin ceramic DIP
  F – 24-pin flatpak
  P – 24-pin plastic DIP
- **Am27S15** — Device Type
  512 x 8 PROM

| Valid Combinations | |
|---|---|
| Am27S15 | PC, PCB, DC, DCB, DM, DMB, FM, FMB |

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

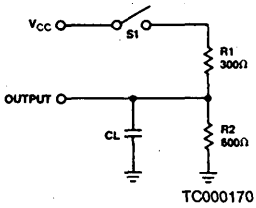
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L | 2.7 | | | Volts |
| | | | MIL | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.5 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 4) | | 2.0 | | | Volts |
| $V_{IL}$ | Input Low Level | Guaranteed input logical LOW voltage for all inputs (Note 4) | COM'L | | | 0.85 | Volts |
| | | | MIL | | | 0.80 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | COM'L | | | −0.100 | mA |
| | | | MIL | | | −0.150 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | 25 | µA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 2) | COM'L | −20 | | −70 | mA |
| | | | MIL | −15 | | −65 | |
| $I_{CC}$ | Power Supply Current | All Inputs = GND<br>$V_{CC}$ = MAX | COM'L | | 125 | 175 | mA |
| | | | MIL | | 125 | 185 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | 1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX,<br>$\overline{VE}_1$ = 2.4V<br>$VE_2$ = 0.4V | $V_O$ = 4.5V | | | 40 | µA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 3) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 3) | | | 12 | | |

Notes:

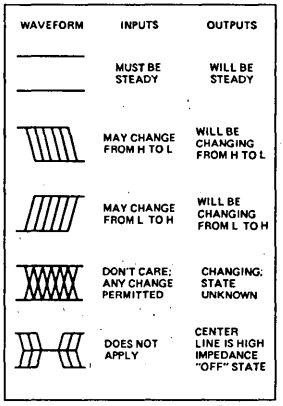
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORM




KS000010

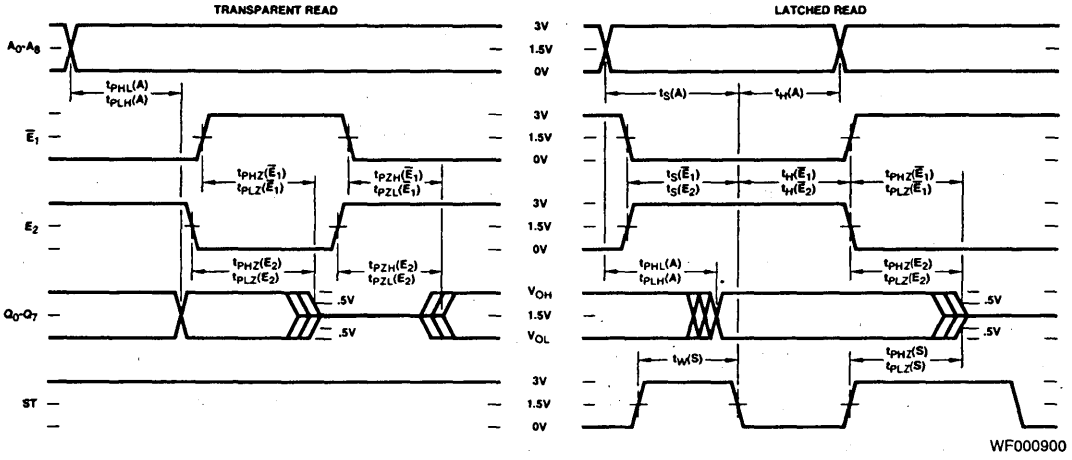
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbols | Description | Test Conditions | C devices | | | M devices | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| 1 | $t_{PHL}(A)$<br>$t_{PLH}(A)$ | Transparent Mode Address to Output Access Time | $C_L$ = 30pF<br>$S_1$ Closed.<br>(See Switching Test Circuit above) | | 35 | 60 | | 35 | 90 | ns |
| 2 | $t_W(S)$ | Strobe Pulse Width (HIGH) | | 30 | 10 | | 40 | 10 | | ns |
| 3 | $t_S(A)$ | Address to Strobe (LOW) Set-up Time | | 60 | 35 | | 90 | 35 | | ns |
| 4 | $t_H(A)$ | Address to Strobe (LOW) Hold Time | | 0 | −10 | | 5 | −10 | | ns |
| 5 | $t_S(\overline{E}_1)$<br>$t_S(E_2)$ | Enable to Strobe (LOW) Set-up Time | | 40 | | | 50 | | | ns |
| 6 | $t_H(\overline{E}_1)$<br>$t_H(E_2)$ | Enable to Strobe (LOW) Hold Time | | 10 | 0 | | 10 | 0 | | ns |
| 7 | $t_{PZH}(\overline{E}_1, E_2)$<br>$t_{PZL}(\overline{E}_1, E_2)$ | Transparent Mode Enable to Output Enabled (HIGH or LOW) Time | $C_L$ = 30pF<br>$S_1$ Closed for $t_{PZL}$, & Open for $t_{PZH}$ | | 20 | 40 | | 20 | 50 | ns |
| 8 | $t_{PZH}(S)$<br>$t_{PLZ}(S)$ | Strobe Detach (HIGH) to Output Disabled (OFF or HIGH impedance) Time | $C_L$ = 5pF<br>$S_1$ Closed for $t_{PLZ}$<br>& Open for $t_{PHZ}$<br>(Note 2) | | | 35 | | | 45 | ns |
| 9 | $t_{PHZ}(\overline{E}_1, E_2)$<br>$t_{PLZ}(\overline{E}_1, E_2)$ | Transparent Mode Enable to Output Disabled (OFFor high impedance) Time | | | 20 | 40 | | 20 | 50 | ns |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$ − 0.5V and $V_{OL}$ + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input rise and fall times (10% to 90%) of 5ns or less.

## SWITCHING WAVEFORMS




WF000900

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S18/S19 Family

32 x 8 Bit Generic Series Bipolar PROM

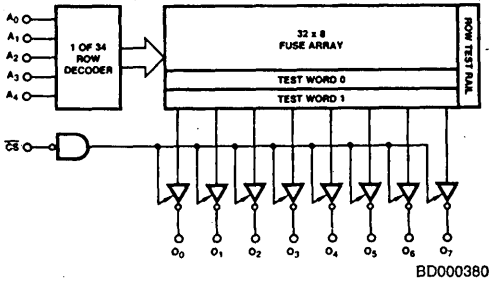
## DISTINCTIVE CHARACTERISTICS

- Ultra High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select

## GENERAL DESCRIPTION

The Am27S18/19 family is composed of high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both collector and three-state output versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_4$ and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to logic HIGH, $O_0 - O_7$ go to the OFF or high impedance state.

## BLOCK DIAGRAM




BD000380

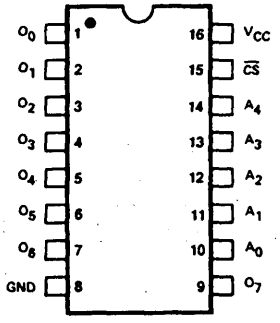
## PRODUCT SELECTOR GUIDE

| Access Time | 15ns | 20ns | 25ns | 35ns | 40ns | 50ns | 55ns | 70ns |
|---|---|---|---|---|---|---|---|---|
| Temperature Range | C | M | C | M | C | M | C | M |
| Open Collector | 27S18SA | | 27S18A | | 27S18 | | 27LS18 | |
| Three-State | 27S19SA | | 27S19A | | 27S19 | | 27LS19 | |

03209B

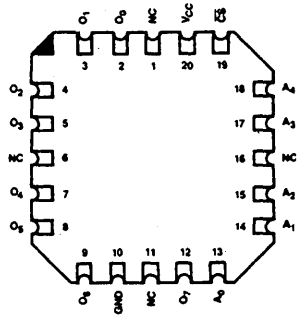
## CONNECTION DIAGRAM
Top View

*D-16
*P-16




CD000520

L-20-1

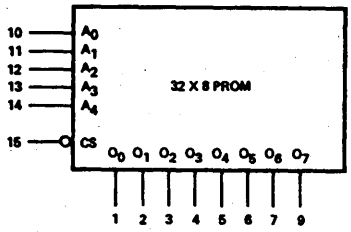



CD000530

Note: Pin 1 is marked for orientation

*Also available in 16-pin flatpak. Connections identical to DIPs.

## LOGIC SYMBOL




LS000070

## ORDERING INFORMATION

**Am27S18 SA P C B**

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- C — Temperature: C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- P — Package: D – 16-pin ceramic DIP; F – 16-pin flatpak; L – 20-pin leadless chip carrier; P – 16-pin plastic DIP
- SA — Speed Select: See Product Selector Guide
- Am27S18 — Device Type

Device Type

Am27S18, Am27S18A — Open Collector

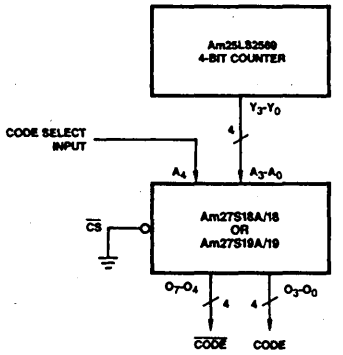
Am27S19, Am27S19A — Three state

Am27LS19A — Low Power

| Valid Combinations | |
|---|---|
| Am27S18 | PC, PCB, |
| Am27S19 | DC, DCB, |
| Am27S18A | LC, LCB, |
| Am27S19A | DM, DMB, |
| Am27S18SA | FM, FMB, |
| Am27S19SA | LM, LMB |
| Am27LS18 | |
| Am27LS19 | |

## APPLICATIONS

the Am27S18SA/18A/18 and Am27S19SA/19A/19 PROMs may be used as code converters. Examples include conversion of hexadecimal, octal of BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am27S18SA/18A/18 or Am27S19SA/19A/19 to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.




AF000160

### TRUTH TABLE

| ADDRESS | | | | | COMPLEMENT | | | | TRUE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $O_7$ | $O_6$ | $O_5$ | $O_4$ | $O_3$ | $O_2$ | $O_1$ | $O_0$ | |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | EXCESS THREE CODE |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | |
| 0 | 1 | 0 | 1 | 0 | X | X | X | X | X | X | X | X | |
| 0 | 1 | 0 | 1 | 1 | X | X | X | X | X | X | X | X | |
| 0 | 1 | 1 | 0 | 0 | X | X | X | X | X | X | X | X | |
| 0 | 1 | 1 | 0 | 1 | X | X | X | X | X | X | X | X | |
| 0 | 1 | 1 | 1 | 0 | X | X | X | X | X | X | X | X | |
| 0 | 1 | 1 | 1 | 1 | X | X | X | X | X | X | X | X | |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | GRAY CODE |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | |

AF000170

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

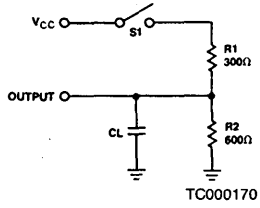
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.45 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | | 25 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND, $V_{CC}$ = MAX | | 27S Devices | | 90 | 115 | mA |
| | | | | 27LS Devices | | 60 | 80 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$V_{\overline{CS}}$ = 2.4V | | $V_O$ = 4.5V | | | 40 | µA |
| | | | Note 2 | $V_O$ = 2.4V | | | 40 | |
| | | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | | 4 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | | 8 | | |

Notes:

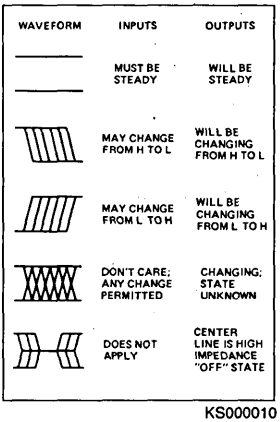
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORM




KS000010

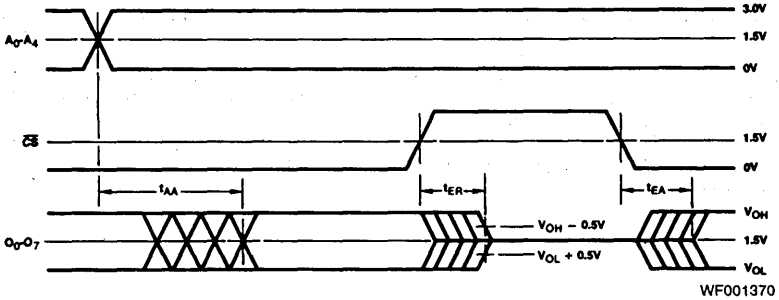
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 25 | 40 | | 25 | 50 | ns |
| | | | A | | 18 | 25 | | 18 | 35 | |
| | | | SA | | 12 | 15 | | 12 | 20 | |
| | | | LS | | 30 | 55 | | 30 | 70 | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 15 | 25 | | 15 | 30 | |
| | | | A | | 13 | 20 | | 13 | 25 | |
| | | | SA | | 10 | 15 | | 10 | 20 | |
| | | | LS | | 22 | 40 | | 22 | 50 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 15 | 25 | | 15 | 30 | |
| | | | A | | 13 | 20 | | 13 | 25 | |
| | | | SA | | 10 | 15 | | 10 | 20 | |
| | | | LS | | 18 | 35 | | 18 | 40 | |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L = 30pF$.
2. For open collector outputs, $t_{EA}$ and $t_{ER}$ are tested with $S_1$ closed to the 1.5V output level. $C_L = 30pF$.
3. For three-state outputs, $t_{EA}$ is tested with $C_L = 30pF$ to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L = 5pF$. High to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH} - 0.5V$; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL} + 0.5V$ level.

## SWITCHING WAVEFORMS




WF001370

Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S20/S21

256 x 4 Bit Generic Series Bipolar PROM



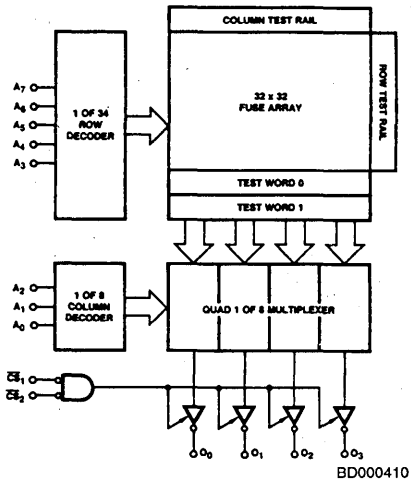
## DISTINCTIVE CHARACTERISTICS

- High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select

## GENERAL DESCRIPTION

The Am27S20A/20 and Am27S21A/21 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 256 x 4 configuration, they are available in both open collector and three-state output versions. After programming, stored information is read on outputs $O_0$–$O_3$ by applying unique binary addresses to $A_0$–$A_7$ and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, at a logic LOW. If either chip select input goes to logic HIGH, $O_0$–$O_3$ go to the OFF or high impedance state.

## BLOCK DIAGRAM




BD000410

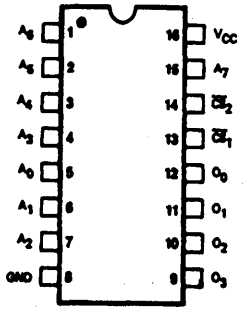
## PRODUCT SELECTOR GUIDE

| Access Time | 30ns | 40ns | 45ns | 60ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Open Collector | 27S20A | | 27S20 | |
| Three-State | 27S21A | | 27S21 | |

03206B

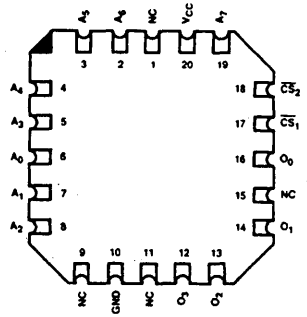
## CONNECTION DIAGRAM
Top View

DIP




CD000570

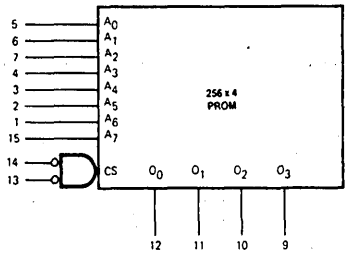
Chip-Pak™
L-20-1




CD000580

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000080

## ORDERING INFORMATION

Am27S20 A P C B

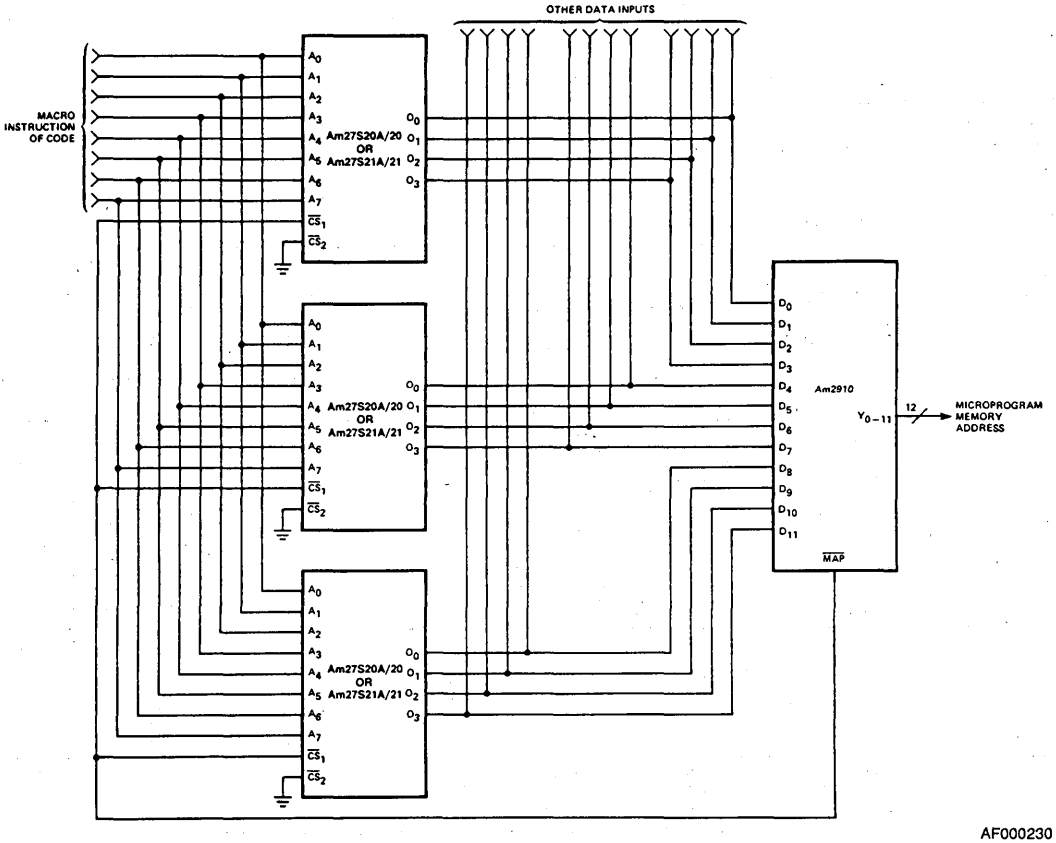
- B — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 16-pin ceramic DIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
- A — Speed Select
  - See Product Selector Guide
- Am27S20 — Device Type
  - Am27S20, Am27S20A: Open Collector
  - Am27S21, Am27S21A: Three state

| Valid Combinations | |
|---|---|
| Am27S20<br>Am27S20A<br>Am27S21<br>Am27S21A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## APPLYING THE Am27S20A/20 AND Am27S21A/21

Typical application of the Am27S20A/20 and Am27S21A/21 is shown below. The Am27S20A/20 and the Am27S21A/21 are employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the $A_0$–$A_7$ inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The $\overline{MAP}$ output of the Am2910 is connected to the $\overline{CS}_1$ input of the Am27S20A/20/21A/21 such that when the $\overline{CS}_1$ input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am27S20A/20 or in the three-state mode in the case of the Am27S21A/21. In both cases the $\overline{CS}_2$ input is grounded; thus data from other sources are free to drive the D inputs of the Am2910 when $\overline{MAP}$ is HIGH.




AF000230

## MICROPROGRAMMING INSTRUCTION MAPPING

### OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

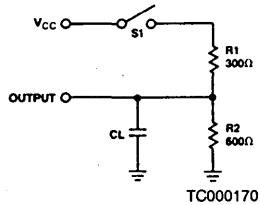
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.45 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | | 25 | μA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND<br>$V_{CC}$ = MAX | | | | 100 | 130 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{CS}_1$ = 2.4V | (Note 2) | $V_O$ = 4.5V | | | 40 | μA |
| | | | | $V_O$ = 2.4V | | | 40 | |
| | | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | | 4 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | | 8 | | pF |

Notes:

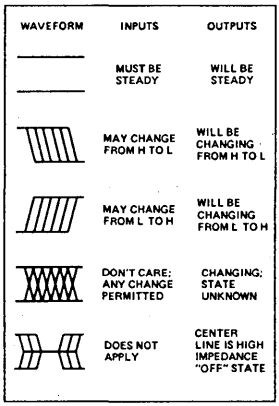
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORMS




KS000010

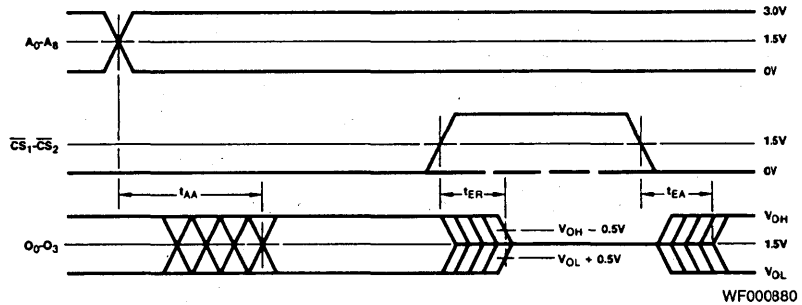
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 25 | 45 | | 25 | 60 | ns |
| | | | A | | 20 | 30 | | 20 | 40 | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 15 | 20 | | 15 | 30 | |
| | | | A | | 15 | 20 | | 15 | 25 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 15 | 20 | | 15 | 30 | |
| | | | A | | 15 | 20 | | 15 | 25 | |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L = 30pF$.
2. For open collector outputs, $t_{EA}$ and $t_{ER}$ are tested with $S_1$ closed to the 1.5V output level. $C_L = 30pF$.
3. For three-state outputs, $t_{EA}$ is tested with $C_L = 30pF$ to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L = 5pF$. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}-0.5V$; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL}+0.5V$ level.

## SWITCHING WAVEFORMS




WF000880

Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S25

512 x 8 Generic Series Bipolar IMOX™
Registered PROM with $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ INPUTS

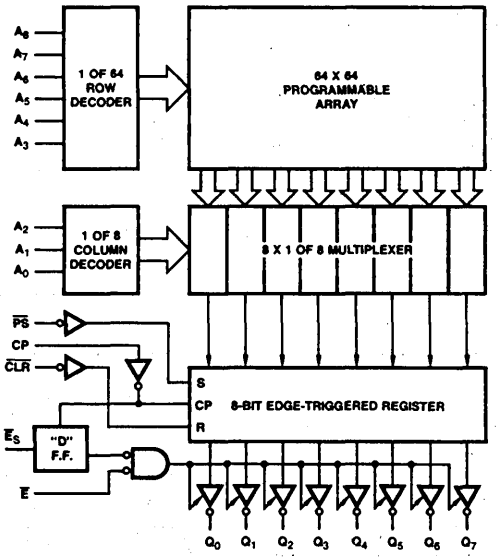
## DISTINCTIVE CHARACTERISTICS

- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Buffered common $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ > 98%)

## GENERAL DESCRIPTION

The Am27S25A/25 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 512-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S25A/25 also offer maximum flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

## BLOCK DIAGRAM




BD000460

## PRODUCT SELECTOR GUIDE

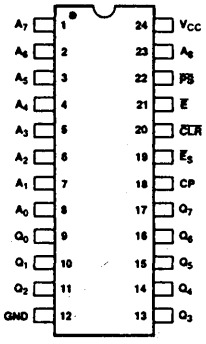
| Access Time | 30ns | 35ns | 50ns | 55ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Part Number | 27S25A | | 27S25 | |

IMOX is a trademark of Advanced Micro Devices, Inc.

03300B

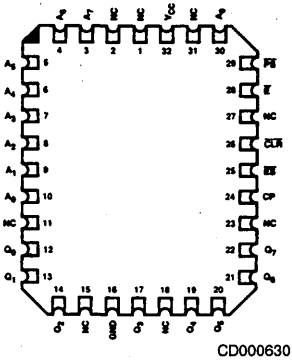
## CONNECTION DIAGRAM
Top View

### DIP




CD001020

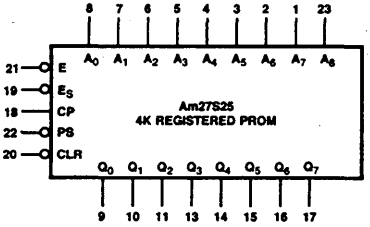
### Chip-Pak™ L-32-2



CD000630

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000110

$V_{CC}$ = Pin 24
GND = Pin 12

## ORDERING INFORMATION

**Am27S25 A P C B**

- B — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 16-pin ceramic DIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
- A — Speed Select
  - See Product Selector Guide
- Am27S25 — Device Type
  - 512 x 8 Bipolar PROM

| Valid Combinations | |
|---|---|
| Am27S25 | PC, PCB, DC, DCB, |
| Am27S25A | LC, LCB, DM, DMB, FM, FMB, LM, LMB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

## PRODUCT OVERVIEW

When $V_{CC}$ power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($Q_0 - Q_7$) to be in the OFF or high-impedance state. Reading data is accomplished by first applying the binary word address to the address inputs ($A_0 - A_8$) and a logic LOW to the synchronous enable ($\overline{E}_S$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable ($\overline{E}$) is also LOW, stored data will appear on the outputs ($Q_0 - Q_7$). If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state regardless of the state of $\overline{E}$. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

The Am27S25 has buffered asynchronous $\overline{\text{PRESET}}$ and $\overline{\text{CLEAR}}$ inputs. These functions are common to all registers and are useful during power up timeout sequences. With outputs enabled the $\overline{\text{PS}}$ input asserted LOW will cause all outputs to be set to a logic 1 (HIGH) state. When the $\overline{\text{CLR}}$ input is LOW, the internal flip-flops of the data register are reset and, a logic 0 (LOW) will appear on all outputs. These functions will control the state of the data register, independent of all other inputs but exclusive of each other.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

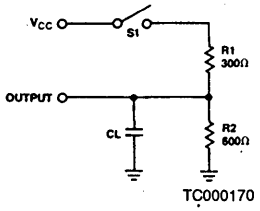
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.38 | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 2) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 2) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | μA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 3) | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND, $V_{CC}$ = MAX | | | 120 | 185 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{VE}$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | μA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 4) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 4) | | | 12 | | |

Notes:

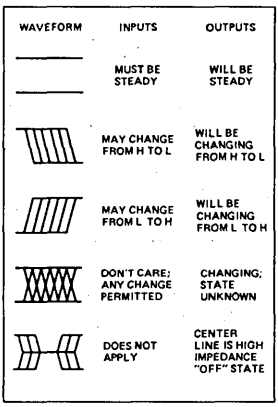
1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORM




KS000010

Notes:

1. $C_L$ = 50pF for all switching characteristics except $t_{PLZ}$ and $t_{PHZ}$.
2. $C_L$ = 5pF for $t_{PLZ}$ and $t_{PHZ}$.
3. $S_1$ is closed for all tests except for $t_{PZH}$ and $t_{PHZ}$.
4. All device test loads should be located within 2" of device outputs.

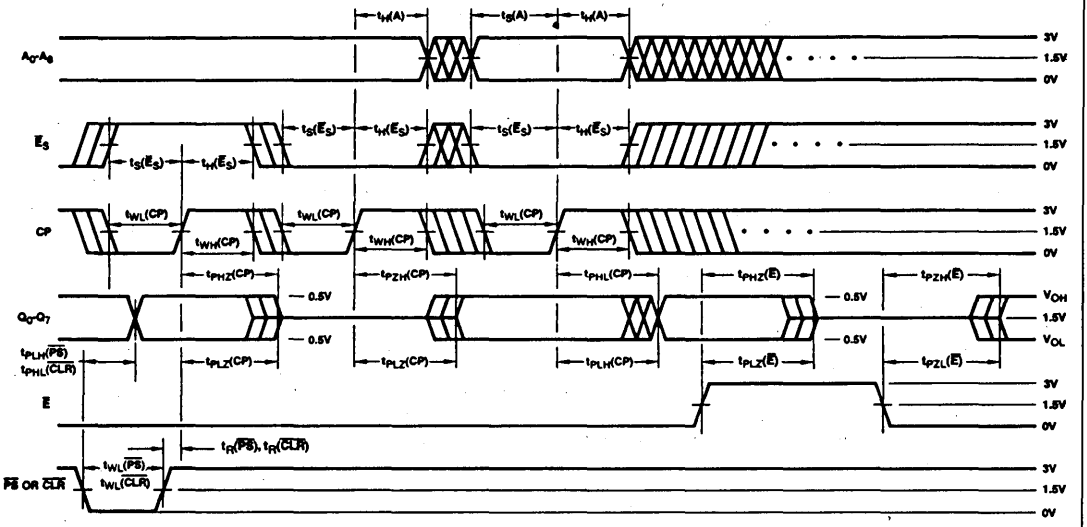
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{SA}$ | Address to CP (HIGH) Setup Time | | STD | 50 | 35 | | 55 | 35 | | ns |
| | | | | A | 30 | 35 | | 35 | 35 | | ns |
| 2 | $t_{H}(A)$ | Address to CP (HIGH) Hold Time | | | 0 | −10 | | 0 | −10 | | ns |
| 3 | $t_{PHL}(CP)$ | Delay from CP (HIGH) to Output (HIGH or LOW) | All Outputs Simultaneous | STD | | 15 | 27 | | 15 | 30 | ns |
| | | | | A | | 15 | 20 | | 15 | 25 | ns |
| 4 | $t_{PLH}(CP)$ | | Single Output (Note 3) | STD | | 13 | 20 | | 13 | 26 | ns |
| | | | | A | | 13 | 15 | | 13 | 23 | ns |
| 5 | $t_{WH}(CP)$ | CP Width (HIGH or LOW) | | | 20 | | | 20 | | | ns |
| 6 | $t_{WL}(CP)$ | | | | | | | | | | |
| 7 | $t_{S}(\overline{E}_S)$ | $\overline{E}_S$ to CP (HIGH) Setup Time | | | 10 | 5 | | 15 | 5 | | ns |
| 8 | $t_{H}(\overline{E}_S)$ | $\overline{E}_S$ to CP (HIGH) Hold Time | | | 5 | −2 | | 5 | −2 | | ns |
| 9 | $t_{PHL}(\overline{CLR})$ | Delay from $\overline{PRESET}$ or $\overline{CLEAR}$ (LOW) to Output (LOW or HIGH) | | STD | | 16 | 25 | | 16 | 30 | ns |
| 10 | $t_{PLH}(\overline{PS})$ | | | A | | 16 | 20 | | 16 | 25 | |
| 11 | $t_{R}(\overline{PS})$ | $\overline{PRESET}$ or $\overline{CLEAR}$ Recovery (Inactive) to CP (HIGH) | | | 20 | 10 | | 25 | 10 | | ns |
| 12 | $t_{R}(\overline{CLR})$ | | | | | | | | | | |
| 13 | $t_{WL}(\overline{PS})$ | $\overline{PRESET}$ or $\overline{CLEAR}$ Pulse width | | | 20 | 10 | | 25 | 10 | | ns |
| 14 | $t_{WL}(\overline{CLR})$ | | | | | | | | | | |
| 15 | $t_{PZL}(CP)$ | Delay from CP (HIGH) to Active Output (HIGH or LOW) | | STD | | 18 | 35 | | 18 | 45 | ns |
| 16 | $t_{PZH}(CP)$ | | | A | | 18 | 25 | | 18 | 30 | |
| 17 | $t_{PZL}(\overline{E})$ | Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) | | STD | | 15 | 35 | | 15 | 45 | ns |
| 18 | $t_{PZH}(\overline{E})$ | | | A | | 15 | 25 | | 15 | 30 | ns |
| 19 | $t_{PLZ}(CP)$ | Delay from CP (HIGH) to Inactive Output (OFF or High Impedance)(Note 4) | | STD | | 21 | 35 | | 21 | 45 | ns |
| 20 | $t_{PHZ}(CP)$ | | | A | | 21 | 25 | | 21 | 30 | ns |
| 21 | $t_{PLZ}(\overline{E})$ | Delay from $E_1$ (HIGH) to Inactive Output (OFF or High Impedance)(Note 4) | | STD | | 15 | 35 | | 15 | 45 | ns |
| 22 | $t_{PHZ}(\overline{E})$ | | | A | | 15 | 25 | | 15 | 30 | ns |

Notes:

1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.
3. Single register performance numbers provided for comparison with discrete register test data.
4. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$−0.5V and $V_{OL}$+0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.

## SWITCHING WAVEFORMS




WF000930

### NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device $V_{CC}$ and ground terminals. Multiple capacitors are recommended, including a 0.1$\mu$Farad or larger capacitor and a 0.01$\mu$Farad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any test.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S27

512 x 8 Bit Generic Series Bipolar Registered PROM
with D-Type Output Data Register

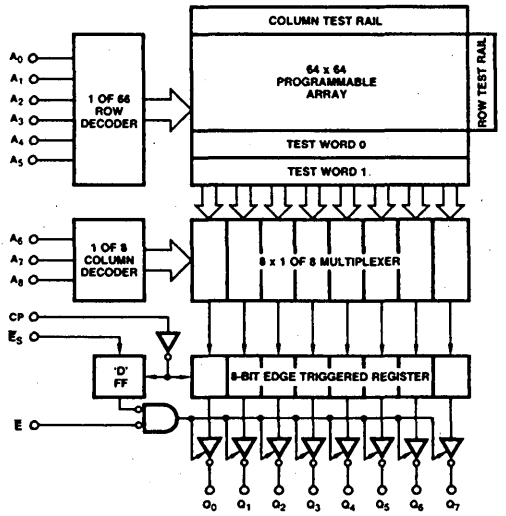
## DISTINCTIVE CHARACTERISTICS

- On-chip edge-triggered registers — Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 55ns address setup and 27ns clock to output times
- Excellent performance over the military range
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)

## GENERAL DESCRIPTION

The Am27S27 is a 512 word x 8-bit PROM which incorporates an on-chip D-type, master-slave data register with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost of pipelined microprogrammed system and other designs wherein accessed PROM data is temporarily stored in a register. The Am27S27 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

## BLOCK DIAGRAM

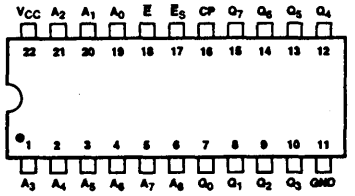



## PRODUCT SELECTOR GUIDE

| Access Time | 55ns | 65ns |
|---|---|---|
| Temperature Range | C | M |
| Part Number | Am27S27 | |

03185C

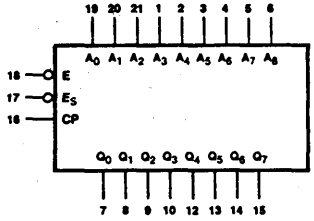
## CONNECTION DIAGRAM
### Top Views




CD000670

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000130

## ORDERING INFORMATION

**Am27S27** **P** **C** **B**

- **B** — Burn-in Option
  B suffix denotes 160 hour burn-in.
- **C** — *Temperature*
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- **P** — Package
  D – 22-pin CERDIP
  P – 22-pin plastic DIP
- **Am27S27** — Device Type
  512 x 8 Registered PROM

| Valid Combinations | |
|---|---|
| Am27S27 | PC, PCB, DC, DCB, DM, DMB |

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## PRODUCT OVERVIEW

When $V_{CC}$ power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs, $Q_0 - Q_7$, to be in the OFF or high impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, $A_0 - A_8$, and a logic LOW to the synchronous output enable, $\overline{E}_S$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}$, is also LOW, stored data will appear on the outputs, $Q_0 - Q_7$. If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

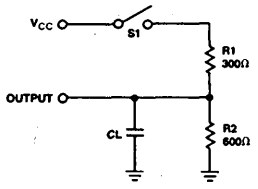
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN., $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN., $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.38 | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 4) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 4) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX., $V_{IN}$ = 0.45V | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 25 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 5.5V | | | | 1.0 | mA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX., $V_{OUT}$ = 0.0V (Note 2) | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND<br>$V_{CC}$ = MAX. | | | 130 | 185 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{VE}$ = 2.4V | $V_O$ = 4.5V | | | 40 | μA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 3) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 3) | | | 12 | | |

Notes:

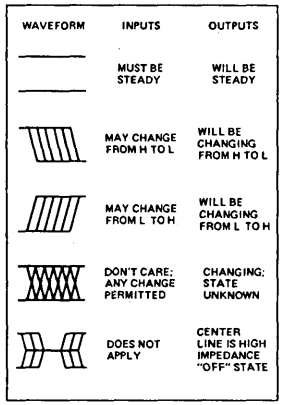
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORM



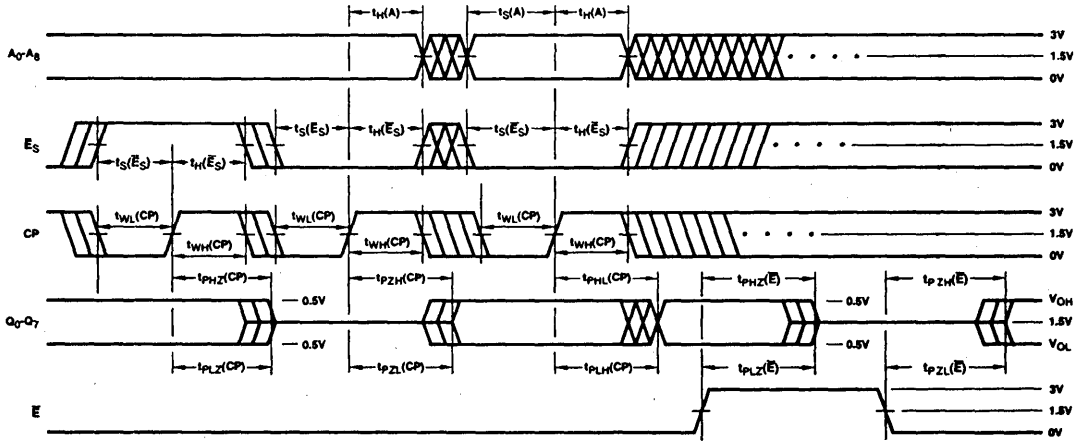

KS000010

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | C devices | | | M devices | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | |
| 1 | $t_S(A)$ | Address to CP (HIGH) Setup Time | $C_L$ = 30pF, $S_1$ closed. (See Switching Test Circuit above) | 55 | 40 | | 65 | 40 | | ns |
| 2 | $t_H(A)$ | Address to CP (HIGH) Hold Time | | 0 | −15 | | 0 | −15 | | ns |
| 3 | $t_{PHL}(CP)$ $t_{PLH}(CP)$ | Delay from CP (HIGH) to Output (HIGH or LOW) | | | 15 | 27 | | 15 | 30 | ns |
| 4 | $t_{WH}(CP)$ $t_{WL}(CP)$ | CP Width (HIGH or LOW) | | 30 | 10 | | 40 | 10 | | ns |
| 5 | $t_S(\overline{E}_S)$ | $\overline{E}_S$ to CP (HIGH) Setup Time | | 25 | 10 | | 30 | 10 | | ns |
| 6 | $t_H(\overline{E}_S)$ | $\overline{E}_S$ to CP (HIGH) Hold Time | | 0 | −10 | | 0 | −10 | | ns |
| 7 | $t_{PZL}(CP)$ $t_{PZH}(CP)$ | Delay from CP (HIGH) to Active Output (HIGH or LOW) | $C_L$ = 30pF, $S_1$ closed for $t_{PZL}$ and open for $t_{PZH}$ | | 15 | 35 | | 15 | 45 | ns |
| 8 | $t_{PZL}(\overline{E})$ $t_{PZH}(\overline{E})$ | Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) | | | 15 | 40 | | 15 | 45 | ns |
| 9 | $t_{PLZ}(CP)$ $t_{PHZ}(CP)$ | Delay from CP (HIGH) to Inactive Output(OFF or High Impedance) | $C_L$ = 5pF (Note 1), $S_1$ closed for $t_{PLZ}$ and open for $t_{PHZ}$ | | 15 | 35 | | 15 | 45 | ns |
| 10 | $t_{PLZ}(\overline{E})$ $t_{PHZ}(\overline{E})$ | Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance) | | | 10 | 30 | | 10 | 40 | ns |

Notes:

1. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$−0.5V and $V_{OL}$+0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
2. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.




WF000950

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S28/29

512 x 8 Bit Generic Series Bipolar PROM

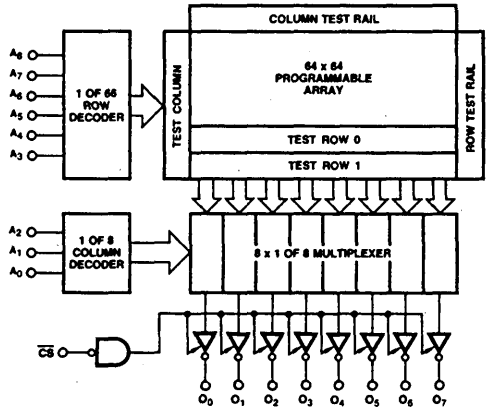
## DISTINCTIVE CHARACTERISTICS

- High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select

## GENERAL DESCRIPTION

The Am27S28A/28 and Am27S29A/29 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S28A/28 and three-state Am27S29A/29 output versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_8$ and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, $O_0 - O_7$ go to the OFF or high impedance state.

## BLOCK DIAGRAM



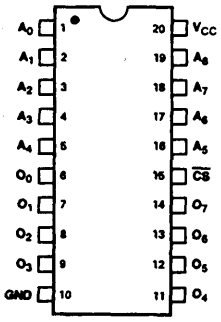

## PRODUCT SELECTOR GUIDE

| Access Time | 40ns | 50ns | 55ns | 70ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Open Collector | 27S28A | | 27S28 | |
| Three-State | 27S29A | | 27S29 | |

03328B

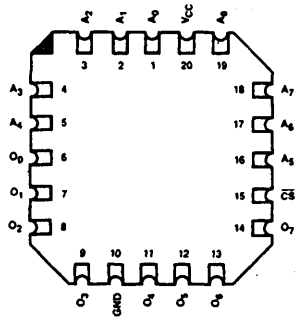
## CONNECTION DIAGRAM
Top View

### DIP




CD000680

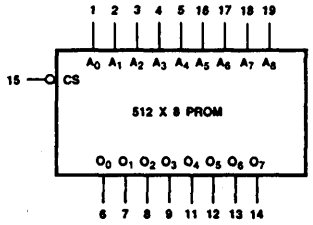
### Chip-Pak™ L-20-1




CD000690

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000140

$V_{CC}$ = Pin 20
GND = Pin 10

## ORDERING INFORMATION

**Am27S28 A P C B**

- **B** — Burn-in Option
  B suffix denotes 160 hour burn-in.
- **C** — Temperature
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- **P** — Package
  D – 20-pin ceramic DIP
  L – 20-pin leadless chip carrier
  P – 20-pin plastic DIP
- **A** — Speed Select
  See Product Selector Guide
- **Am27S28** — Device Type
  Am27S28, Am27S28A: Open Collector
  Am27S29, Am27S29A: Three state

| Valid Combinations | |
|---|---|
| Am27S28<br>Am27S28A<br>Am27S29<br>Am27S29A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>LM, LMB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

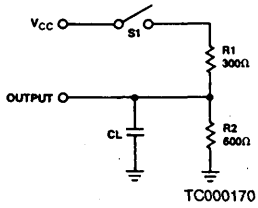
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | | 25 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND<br>$V_{CC}$ = MAX | | | | 105 | 160 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{CS}$ = 2.4V | (Note 2) | $V_O$ = 4.5V | | | 40 | µA |
| | | | | $V_O$ = 2.4V | | | 40 | |
| | | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | | 4 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | | 8 | | |

Notes:

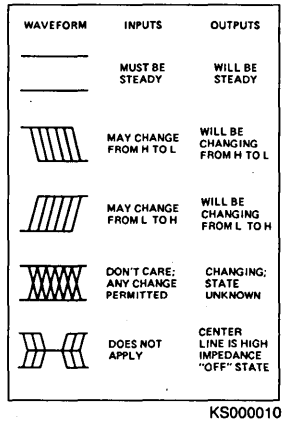
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORM




KS000010

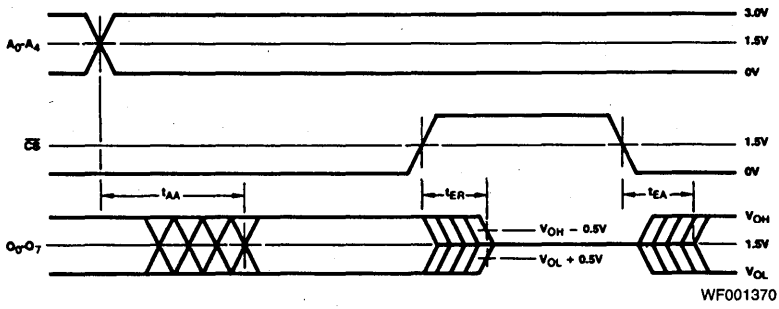
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 35 | 55 | | 35 | 70 | ns |
| | | | A | | 30 | 35 | | 30 | 45 | ns |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 15 | 25 | | 15 | 30 | ns |
| | | | A | | 12 | 20 | | 12 | 25 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 15 | 25 | | 15 | 30 | ns |
| | | | A | | 12 | 20 | | 12 | 25 | ns |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L = 30pF$.
2. For open collector outputs, $t_{EA}$ and $t_{ER}$ are tested with $S_1$ closed to the 1.5V output level. $C_L = 30pF$.
3. For three-state outputs, $t_{EA}$ is tested with $C_L = 30pF$ to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L = 5pF$. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}-0.5V$; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL}+0.5V$ level.

## SWITCHING WAVEFORMS




WF001370

Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S30/31

512 x 8 Bit Generic Series Bipolar PROM



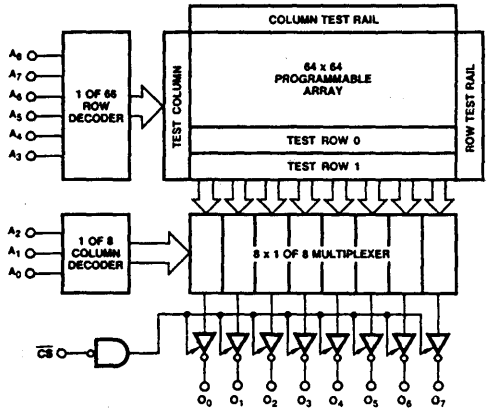
## DISTINCTIVE CHARACTERISTICS

- High Speed — 35ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select

## GENERAL DESCRIPTION

The Am27S30A/30 and Am27S31A/31 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S30A/30 and three-state Am27S31A/31 output versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_8$ and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and $CS_3$ and $CS_4$ HIGH. All other valid input conditions on $\overline{CS}_1$, $\overline{CS}_2$, $CS_3$ and $CS_4$ place $O_0 - O_7$ into the OFF or high impedance state.

## BLOCK DIAGRAM




BD000480

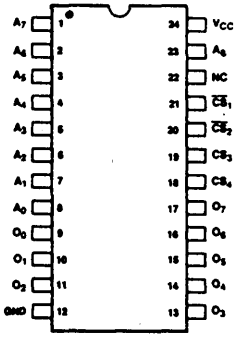
## PRODUCT SELECTOR GUIDE

| Access Time | 40ns | 50ns | 55ns | 70ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Open Collector | 27S30A | | 27S30 | |
| Three-State | 27S31A | | 27S31 | |

03207B

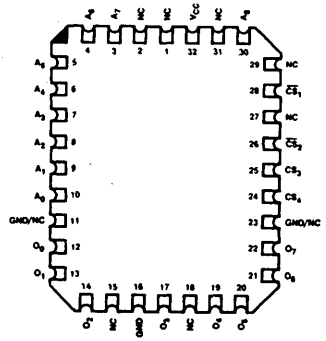
## CONNECTION DIAGRAM
Top View

### DIP




CD000700

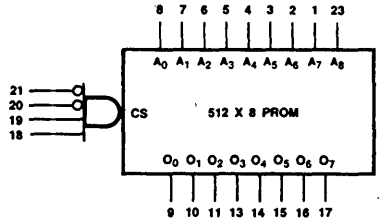
### Chip-Pak™ L-32-2




CD000710

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000150

$V_{CC}$ = Pin 24
GND = Pin 12
(Pin 22 Open)

## ORDERING INFORMATION

Am27S30 A P C B

- B — Burn-in Option
  B suffix denotes 160 hour burn-in.
- C — Temperature
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- P — Package
  D – 24-pin ceramic DIP
  F – 24-pin flatpak
  L – 32-pin leadless chip carrier
  P – 24-pin plastic DIP
- A — Speed Select
  See Product Selector Guide
- Am27S30 — Device Type
  Am27S30, Am27S30A: Open Collector
  Am27S31, Am27S31A: Three state

| Valid Combinations | |
|---|---|
| Am27S30<br>Am27S30A<br>Am27S31<br>Am27S31A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

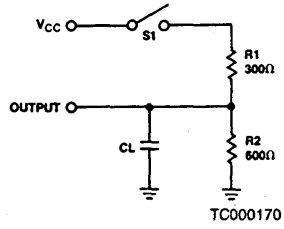
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | | 25 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND<br>$V_{CC}$ = MAX | | | | 115 | 175 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{V_{CS}}$ = 2.4V | | $V_O$ = 4.5V | | | 40 | µA |
| | | | (Note 2) | $V_O$ = 2.4V | | | 40 | |
| | | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | | 4 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | | 8 | | pF |

Notes:

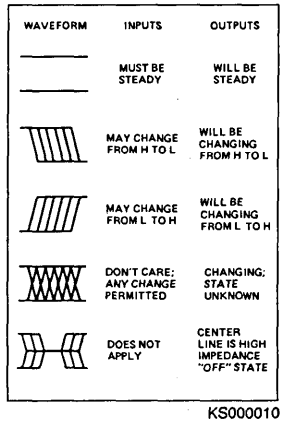
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORMS




KS000010

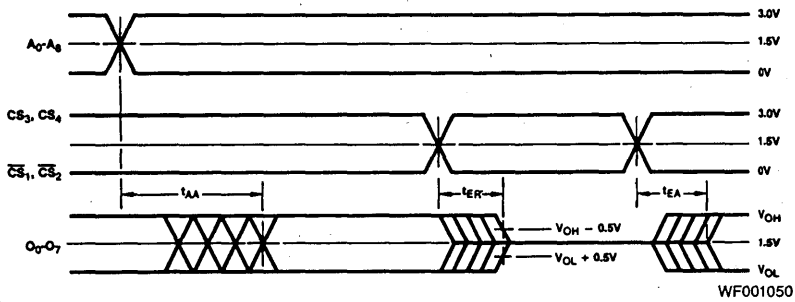
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 35 | 55 | | 35 | 70 | ns |
| | | | A | | 30 | 35 | | 30 | 45 | ns |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 15 | 25 | | 15 | 30 | ns |
| | | | A | | 12 | 20 | | 12 | 25 | ns |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 15 | 25 | | 15 | 30 | ns |
| | | | A | | 12 | 20 | | 12 | 25 | ns |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L = 30pF$.
2. For open collector outputs, $t_{EA}$ and $t_{ER}$ are tested with $S_1$ closed to the 1.5V output level. $C_L = 30pF$.
3. For three-state outputs, $t_{EA}$ is tested with $C_L = 30pF$ to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L = 5pF$. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}-0.5V$; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL}+0.5V$ level.

## SWITCHING WAVEFORMS




WF001050

Note: Level on output while chip is disabled is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S32/33

1024 x 4 Bit Generic Series Bipolar PROM

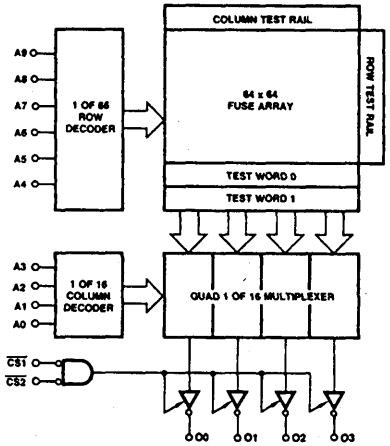
## DISTINCTIVE CHARACTERISTICS

- High Speed
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select

## GENERAL DESCRIPTION

The Am27S32A/32 and Am27S33A/33 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 4 configuration, they are available in both open collector Am27S32A/32 and three-state Am27S33A/33 output versions. After programming, stored information is read on outputs $O_0 - O_3$ by applying unique binary addresses to $A_0 - A_9$ and holding the chip select input, $\overline{CS}_1$, and $\overline{CS}_2$ LOW. If the chip select input goes to a logic HIGH, $O_0 - O_3$ go to the OFF or high impedance state.

## BLOCK DIAGRAM




BD000500

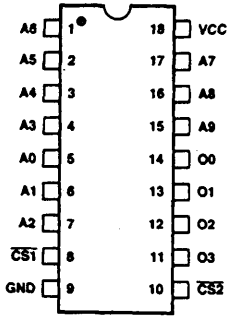
## PRODUCT SELECTOR GUIDE

| Access Time | 35ns | 45ns | 55ns | 70ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Open Collector | 27S32A | | 27S32 | |
| Three-State | 27S33A | | 27S33 | |

03226B

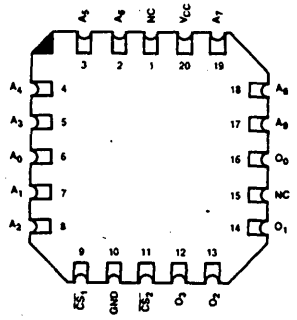
## CONNECTION DIAGRAM
### Top View

**DIP**




CD000720

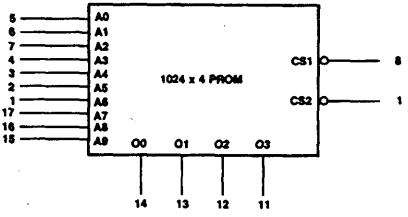
**Chip-Pak™ L-20-1**




CD000730

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000160

$V_{CC}$ = Pin 18
GND = Pin 9

## ORDERING INFORMATION

**Am27S32 A P C B**

- **B** — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- **C** — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **P** — Package
  - D – 18-pin ceramic DIP
  - L – 20-pin leadless chip carrier
  - P – 18-pin plastic DIP
- **A** — Speed Select
  - See Product Selector Guide
- **Am27S32** — Device Type
  - Am27S32, Am27S32A: Open Collector
  - Am27S33, Am27S33A: Three state

| Valid Combinations | |
|---|---|
| Am27S32<br>Am27S32A<br>Am27S33<br>Am27S33A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>LM, LMB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

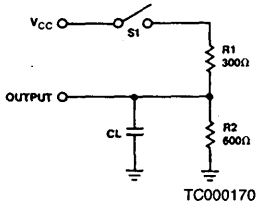
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.45 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | 25 | μA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND,<br>$V_{CC}$ = MAX | COM'L | | 105 | 140 | mA |
| | | | MIL | | 105 | 145 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{VCS}_1$ = 2.4V | $V_O$ = 4.5V | | | 40 | μA |
| | | | (Note 2) $V_O$ = 2.4V | | | 40 | |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | 12 | | |

Notes:

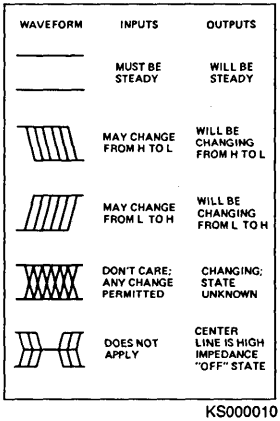
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORM




KS000010

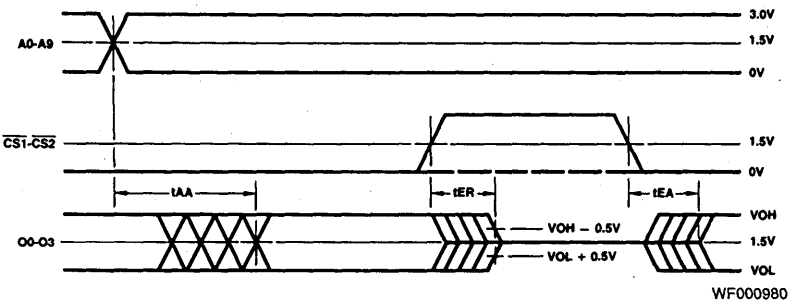
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 38 | 55 | | 38 | 70 | ns |
| | | | A | | 25 | 35 | | 25 | 45 | ns |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 20 | 25 | | 20 | 30 | ns |
| | | | A | | 18 | 25 | | 18 | 30 | ns |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 20 | 25 | | 20 | 30 | ns |
| | | | A | | 18 | 25 | | 18 | 30 | |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L$ = 30pF.
2. For open collector outputs, $t_{EA}$ and $t_{ER}$ are tested with $S_1$ closed to the 1.5V output level. $C_L$ = 30pF.
3. For three-state outputs, $t_{EA}$ is tested with $C_L$ = 30pF to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L$ = 5pF. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}$–0.5V; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL}$+0.5V level.

## SWITCHING WAVEFORMS




WF000980

Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S35/37

1024 x 8 Bit Generic Series IMOX™ Bipolar High Performance Registered PROM with Programmable $\overline{\text{INITIALIZE}}$



## DISTINCTIVE CHARACTERISTICS

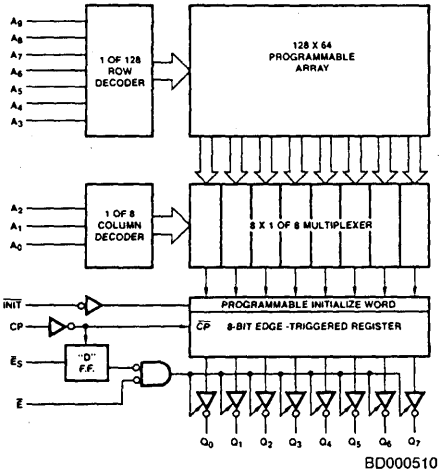
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- Versatile synchronous or asynchronous enables for simplified word expansion
- Versatile programmable register $\overline{\text{INITIALIZE}}$ either asynchronous (Am27S35A/35) or synchronous (Am27S37A/37)
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ > 98%)

## GENERAL DESCRIPTION

The Am27S35A/35 and Am27S37A/37 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 8 configuration, they are available in both open collector Am27S35A/35 and three-state Am27S37A/37 output versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_8$ and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and $CS_3$ and $CS_4$ HIGH. All other valid input conditions on $\overline{CS}_1$, $\overline{CS}_2$, $CS_3$ and $CS_4$ place $O_0 - O_7$ into the OFF or high impedance state.

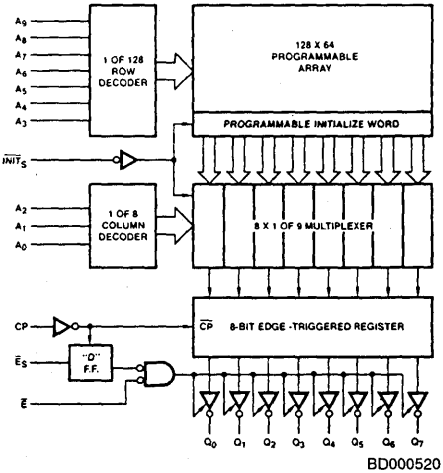
## BLOCK DIAGRAM

**Am27S35**




BD000510

**Am27S37**



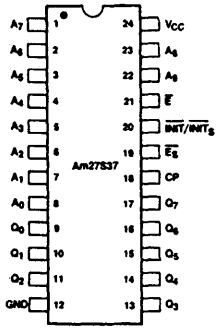

BD000520

## PRODUCT SELECTOR GUIDE

| Access Time | 35ns | 40ns | 40ns | 45ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Asynchronous Initialize | Am27S35A | | Am27S35 | |
| Synchronous Initialize | Am27S37A | | Am27S37 | |

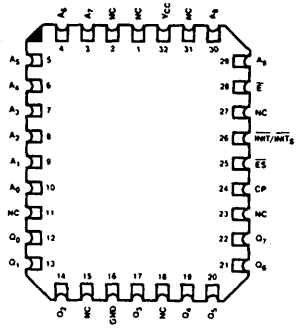
## CONNECTION DIAGRAM
Top View

### DIP




CD000740

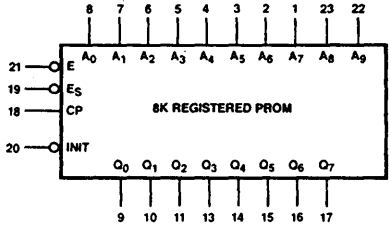
### Chip-Pak™ L-32-2




CD000750

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000170

$V_{CC}$ = Pin 24
GND = Pin 12

## ORDERING INFORMATION

**Am27S35 A P C B**

- B — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 24-pin ceramic DIP
  - F – 24-pin flatpak
  - L – 32-pin leadless chip carrier
  - P – 24-pin plastic DIP
- A — Speed Select
  - See Product Selector Guide

Device Type

- Am27S35, Am27S35A — Asynchronous
- Am27S37, Am27S37A — Synchronous

| Valid Combinations | |
|---|---|
| Am27S35<br>Am27S35A<br>Am27S37<br>Am27S37A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

Chip-pak is a trademark of Advanced Micro Devices, Inc.

## DETAILED DESCRIPTION

The Am27S35A/35 and Am27S37A/37 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 1024-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S35A/35 and Am27S37A/37 also offer maximum flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When $V_{CC}$ power is first applied, the synchronous enable ($\overline{E}_S$) flip-flop will be in the set condition causing the outputs ($Q_0$–$Q_7$) to be in the OFF or high impedance state. Reading data is accomplished by first applying the binary word address to the address inputs ($A_0$–$A_9$) and a logic LOW to the synchronous enable ($\overline{E}_S$). During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock (CP), data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable ($\overline{E}$) is also LOW, stored data will appear on the outputs ($Q_0$–$Q_7$). If $\overline{E}_S$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state regardless of the value of $\overline{E}$. The outputs may be disabled at any time by switching $\overline{E}$ to a HIGH level. Following the positive clock edge the address and synchronous enable inputs are free to change; changes will not affect the outputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

These devices also contain a built-in initialize function. When activated, the initialize control input ($\overline{INIT}$) causes the contents of an additional (1025th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating $\overline{INIT}$ will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S35A/35 has an asynchronous initialize input ($\overline{INIT}$). Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the slave flip-flops of the register independent of all other inputs (including CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

The Am27S37A/37 has a synchronous $\overline{INIT}_S$ input. Applying a LOW to the $\overline{INIT}_S$ input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including CP). To bring this data to the device outputs, the synchronous enable ($\overline{E}_S$) should be held LOW until the next LOW-to-HIGH transition of the clock (CP). Following this, the data will appear on the outputs after the asynchronous enable ($\overline{E}$) is brought LOW.

## OBTAINING PROGRAMMED UNITS

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

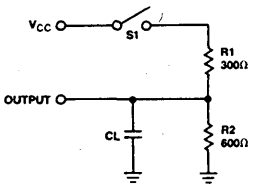
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 0.38 | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 2) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 2) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | µA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 3) | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND, $V_{CC}$ = MAX | | | 130 | 185 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$V_{E_1}$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | µA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 4) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 4) | | | 12 | | |

Notes:

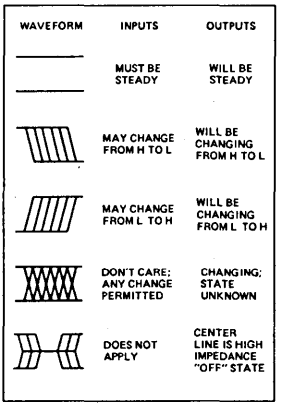
1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORMS




KS000010

Notes:

1. $C_L$ = 50pF for all switching characteristics except $t_{PLZ}$ and $t_{PHZ}$.
2. $C_L$ = 5pF for $t_{PLZ}$ and $t_{PHZ}$.
3. $S_1$ is closed for all tests except for $t_{PZH}$ and $t_{PHZ}$.
4. All device test loads should be located within 2" of device outputs.

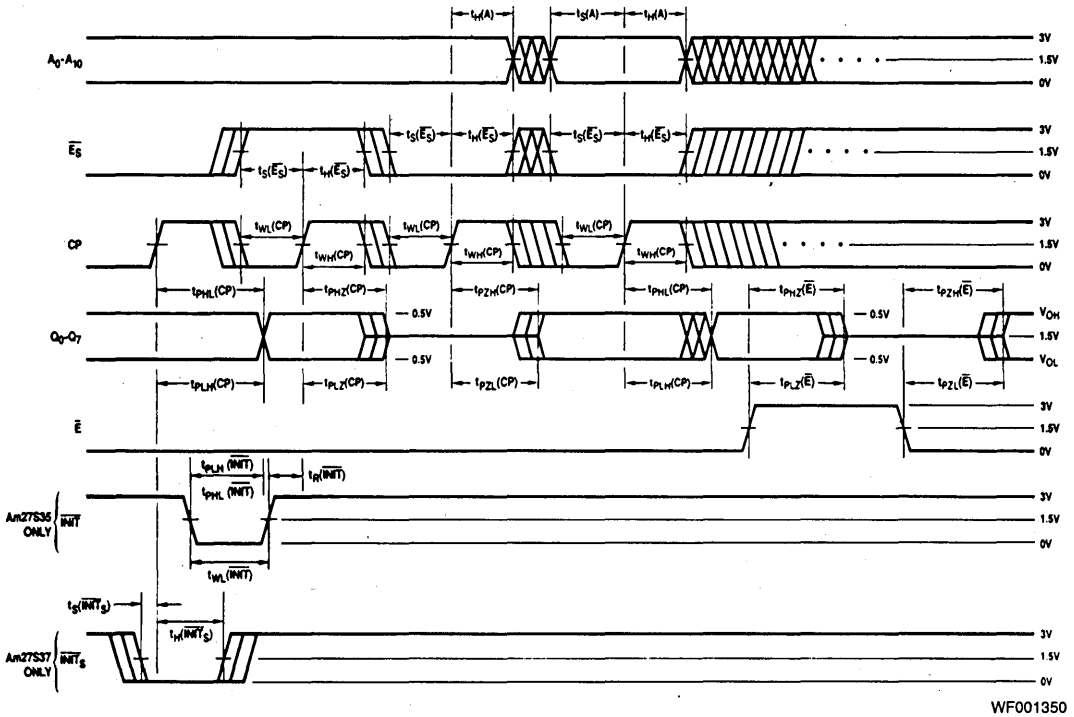
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | STD C devices Min | STD C devices Max | STD M devices Min | STD M devices Max | A C devices Min | A C devices Max | A M devices Min | A M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_S$(A) | Address to CP (HIGH) Setup Time | | 35 | | 40 | | 40 | | 45 | | ns |
| 2 | $t_H$(A) | Address to CP (HIGH) Hold Time | | 0 | | 0 | | 0 | | 0 | | |
| 3 | $t_{PHL}$(CP) | Delay from CP (HIGH) to Output (HIGH or LOW) | All Outputs Simultaneous | | 20 | | 25 | | 25 | | 30 | |
| 4 | $t_{PLH}$(CP) | | Single Output (Note 3) | | 18 | | 21 | | 20 | | 23 | |
| 5 | $t_{WH}$(CP)<br>$t_{WL}$(CP) | CP Width (HIGH or LOW) | | 20 | | 20 | | 20 | | 20 | | |
| 6 | $t_s(\overline{ES})$ | OSCP to CP (HIGH Setup Time | | 15 | | 15 | | 15 | | 15 | | |
| 7 | $t_H(\overline{ES})$ | $\overline{ES}$ to CP (HIGH) Hold Time | | 5 | | 5 | | 5 | | 5 | | |
| 8 | $t_{PHL}(\overline{INIT})$<br>$t_{PLH}$ | Delay from $\overline{INIT}$(LOW) to Outputs (LOW or HIGH) | Am27S35 Only | | 30 | | 35 | | 35 | | 40 | |
| 9 | $t_R(\overline{INIT})$ | $\overline{INIT}$ Recovery (Inactive) to CP (HIGH) | | 20 | | 20 | | 20 | | 20 | | |
| 10 | $t_{WL}(\overline{INIT})$ | $\overline{INIT}$ Pulse Width | | 25 | | 30 | | 25 | | 30 | | |
| 11 | $t_S(\overline{INIT_S})$ | $\overline{INIT_S}$ to CP (HIGH) Setup Time | Am27S37 Only | 25 | | 30 | | 30 | 35 | | | |
| 12 | $t_H(\overline{INIT_S})$ | $\overline{INIT_S}$ to CP (HIGH) Hold Time | | 0 | | 0 | | 0 | | 0 | | |
| 13 | $t_{PZL}$(CP)<br>$t_{PZH}$(CP) | Delay from CP (HIGH) to Active Output (HIGH or LOW) | | | 25 | | 30 | | 30 | | 35 | |
| 14 | $t_{PZL}(\overline{E})$<br>$t_{PZH}(\overline{E})$ | Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) | | | 25 | | 30 | | 30 | | 35 | |
| 15 | $t_{PLZ}$(CP)<br>$t_{PHZ}$(CP) | Delay from CP (HIGH) to Inactive Output (OFF or HIGH Impedance) (Note 4) | | | 25 | | 30 | | 30 | | 35 | |
| 16 | $t_{PLZ}(\overline{E})$<br>$t_{PHZ}(\overline{E})$ | Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or High Impedance) (Note 4) | | | 25 | | 30 | | 30 | | 35 | |

Notes:

1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C
2. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.
3. Single register performance numbers provided for comparison with discrete register test data.
4. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$ − 0.5V and $V_{OL}$ + 0.5v output levels respectively. All other switching parameters are tested from and to the 1.5V old threshold levels.

## SWITCHING WAVEFORMS
**(See Notes on Testing)**




WF001350

### NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device $V_{CC}$ and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.1μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any test.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S40/S41

4096 x 4 Bit Generic Series Bipolar IMOX™ PROM
(with ultra fast access time)



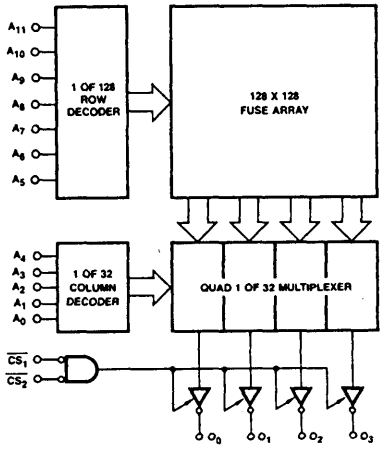
## DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (35ns max) — Fast access time Standard version (50ns max) — allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

## GENERAL DESCRIPTION

The Am27S40A, Am27S41A, Am27S40, and Am27S41 are high speed electrically programmable Schottky read only memories. Organized in 4096 x 4 configuration, they are available in both open collector (Am27S40A and Am27S40) and three-state (Am27S41A and Am27S41) output versions. After programming, stored information is read on outputs $O_0 - O_3$ by applying unique binary addresses to $A_0 - A_{11}$ and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, LOW. If either chip select input goes to a logic HIGH, $O_0 - O_3$ go to the OFF or HIGH impedance state.

## BLOCK DIAGRAM



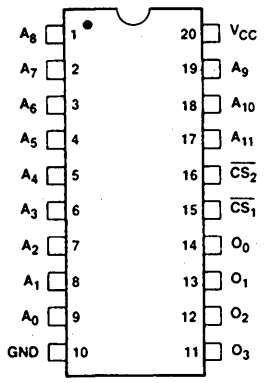

BD000330

## PRODUCT SELECTOR GUIDE

| Access Time | 35ns | 50ns | | 65ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Open Collector | 27S40A | 27S40A | 27S40 | 27S40 |
| Three-State | 27S41A | 27S41A | 27S41<br>27PS41 | 27S41<br>27PS41 |

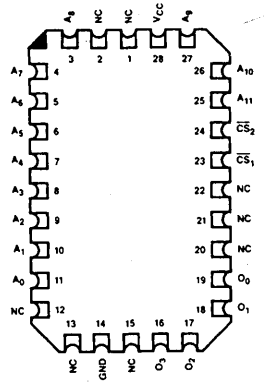
## CONNECTION DIAGRAM
Top View

### DIP




CD000410

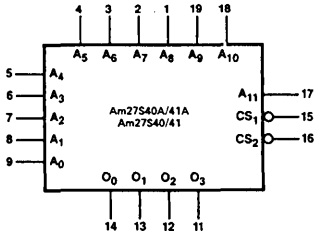
### Chip-Pak™




CD000420

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000040

$V_{CC}$ = Pin 20
GND = Pin 10

## ORDERING INFORMATION

**Am27S40 A P C B**

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- C — Temperature: C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- P — Package: D – 20-pin ceramic DIP; L – 28-pin leadless chip carrier; P – 20-pin plastic DIP
- A — Speed Select: See Product Selector Guide
- Am27S40 — Device Type

Device Type

| | |
|---|---|
| Am27S40<br>Am27S40A | Open Collector |
| Am27S41<br>Am27S41A | Three State |
| Am27PS41 | Power Switched |

| Valid Combinations | |
|---|---|
| Am27S40<br>Am27S40A<br>Am27S41<br>Am27S41A<br>Am27PS41 | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

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02122B

## POWER SWITCHING

The Am27PS41 is a power switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, $I_{CC}$ is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS41 is selected by a low level on $\overline{CS}_1$, a current surge is placed on the $V_{CC}$ supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 20 to pin 10 at each device. (See Figure 1.)

2. Address access time ($t_{AA}$) can be optimized if a chip enable set-up time ($t_{EAS}$) of greater than 25ns is observed. Negative set-up times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

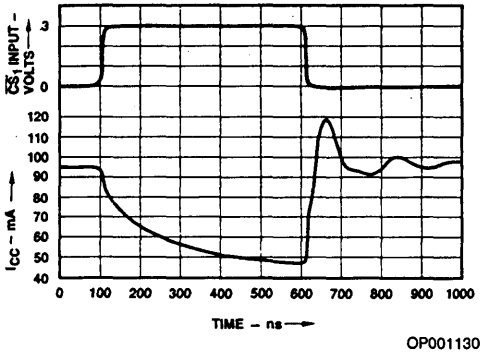
| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ (TS Devices only) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L | | | 0.45 | Volts |
| | | | MIL | | | 0.50 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 4) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 4) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | μA |
| $I_{SC}$ (TS Devices only) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V<br>(Note 2) | COM'L | −20 | −40 | −90 | mA |
| | | | MIL | −15 | −40 | −90 | |
| $I_{CC}$ | Power Supply Current | All inputs = GND,<br>$V_{CC}$ = MAX<br>$\overline{CS}_1$ = 2.7V, All other inputs = GND | COM'L | | 110 | 165 | mA |
| | | | MIL | | 110<br>50 | 170<br>85 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$V_{\overline{CS}_1}$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | μA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 3) | | | 5.0 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 3) | | | 8.0 | | |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

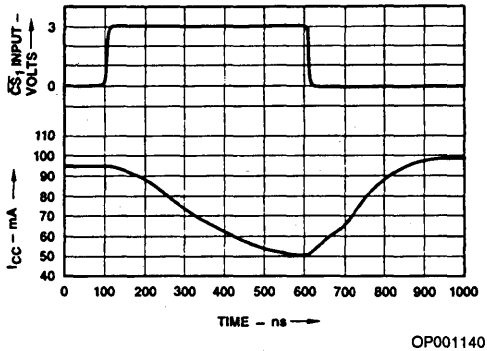
## DC OPERATING CHARACTERISTICS

Typical $I_{CC}$ Current Surge without 0.1mF
($I_{CC}$ is Current Supplied by $V_{CC}$ Power Supply)



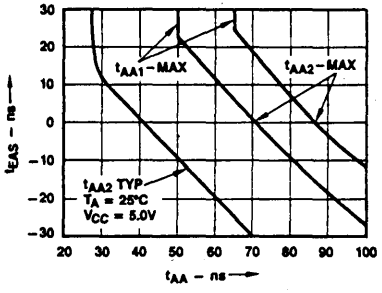

OP001130

Typical $I_{CC}$ Current Surge with 0.1mF
($I_{CC}$ is Current Supplied by $V_{CC}$ Power Supply)



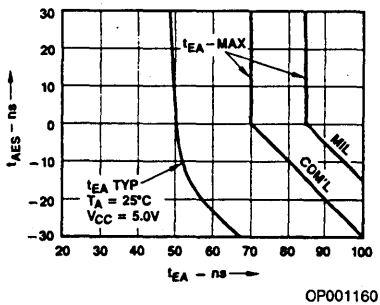

OP001140

Figure 1. $I_{CC}$ Current




OP001150

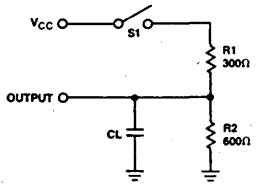
Figure 2A. $t_{AA}$ versus $t_{EAS}$




OP001160

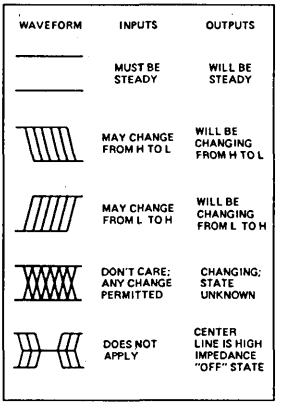
Figure2B. $t_{EA}$ versus $t_{AES}$

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORMS




KS000010

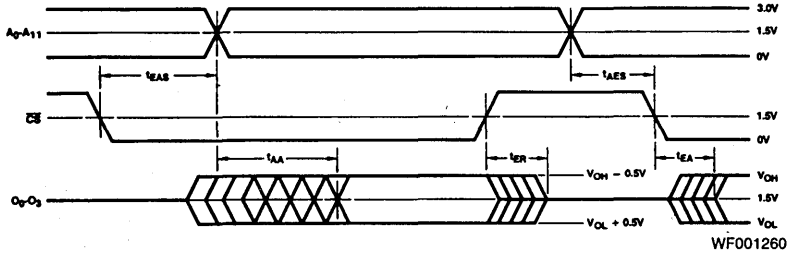
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | 27S C devices Min | 27S C devices Max | 27S M devices Min | 27S M devices Max | 27PS C devices Min | 27PS C devices Max | 27S M devices Min | 27S M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 50 | | 65 | | 50 | | 65 | ns |
| | | | A | | 35 | | 50 | | | | | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 25 | | 30 | | 70 | | 85 | |
| | | | A | | 25 | | 30 | | | | | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 25 | | 30 | | 25 | | 30 | |
| | | | A | | 25 | | 30 | | | | | |
| 4 | $t_{AAPS}$ | Power Switched Address Access Time (27PS devices only) | STD | | | | | | 70 | | 85 | |
| | | | A | | | | | | | | | |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L$ = 30pF. $t_{EAS}$ is defined as chip enable setup time.
2. For the three-state output, $t_{EA}$ is tested with $C_L$ = 30pF to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L$ = 5pF. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}$−0.5V; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL}$+0.5V level.

## SWITCHING WAVEFORMS




WF001260

Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S43

4096 x 8 Bit Generic Series Bipolar IMOX™ PROM



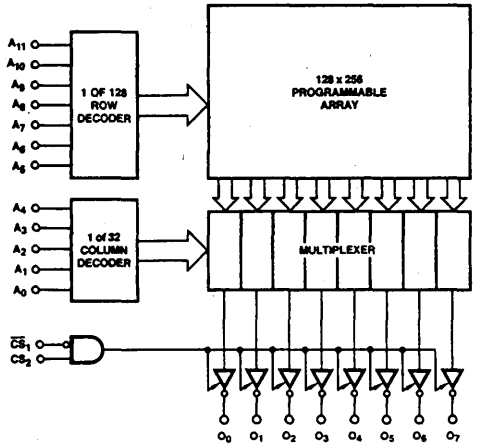
## DISTINCTIVE CHARACTERISTICS

- Ultra fast access time
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Voltage and temperature compensated providing extremely flat AC performance over military range

## GENERAL DESCRIPTION

The Am27S43A and Am27S43 are high speed electrically programmable Schottky read only memories. Organized in 4096 x 8 configuration, they are available in three-state (Am27S43A and Am27S43) output versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_{11}$ and holding the chip select input, $\overline{CS}_1$, LOW and $CS_2$, HIGH. If $\overline{CS}_1$ goes to logic HIGH or $CS_2$ goes to logic LOW, $O_0 - O_7$ go to the OFF or HIGH impedance state.

## BLOCK DIAGRAM




BD000350

## PRODUCT SELECTOR GUIDE

| Access Time | 40ns | 55ns | | 65ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Three-State | Am27S43A | Am27S43A | Am27S43 | Am27S43 |

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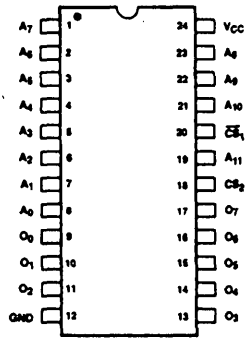
03190B

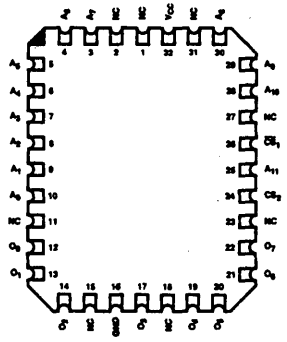
## CONNECTION DIAGRAM
Top View

### DIP




CD000500

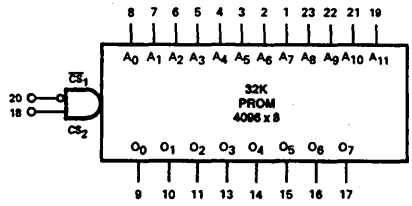
### Chip-Pak™ L-32-2




CD000510

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000120

$V_{CC}$ = Pin 24
GND = Pin 12

## ORDERING INFORMATION

**Am27S43** **A** **P** **C** **B**

- **B** — Burn-in Option
  B suffix denotes 160 hour burn-in.
- **C** — Temperature
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- **P** — Package
  D – 24-pin ceramic DIP
  L – 33-pin leadless chip carrier
  P – 24-pin plastic DIP
- **A** — Speed Select
  See Product Selector Guide
- **Am27S43** — Device Type
  Am27S43 Three state
  Am27S43A

| Valid Combinations | |
|---|---|
| Am27S43<br>Am27S43A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>LM, LMB |

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## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

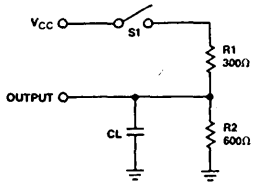
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 2) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 2) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | μA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 3) | | −15 | −40 | −100 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND,<br>$V_{CC}$ = MAX | COM'L | | 135 | 185 | mA |
| | | | MIL | | 135 | 185 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{CS}_1$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | μA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 4) | | | 5.0 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 4) | | | 8.0 | | |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT

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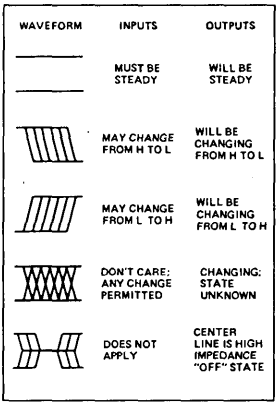
## KEY TO SWITCHING WAVEFORMS

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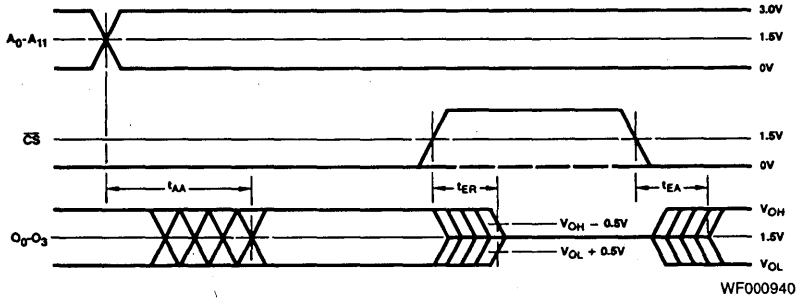
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AD}$ | Address Access Time | STD | | 35 | 55 | | 35 | 65 | ns |
| | | | A | | 30 | 40 | | 30 | 55 | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 20 | 35 | | 20 | 40 | |
| | | | A | | 20 | 30 | | 20 | 35 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 20 | 35 | | 20 | 40 | |
| | | | A | | 20 | 30 | | 20 | 35 | |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L$ = 30pF.
2. For three-state outputs, $t_{EA}$ is tested with $C_L$ = 30pF to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L$ = 5pF. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}$–0.5V; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL}$+0.5V level.

## SWITCHING WAVEFORMS

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Note: Level on output while $\overline{CS}_1$ is HIGH or $CS_2$ LOW is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S45/47

2048 x 8 Generic Series IMOX™ Bipolar High
Performance Registered PROM with Programmable $\overline{\text{INITIALIZE}}$

## DISTINCTIVE CHARACTERISTICS

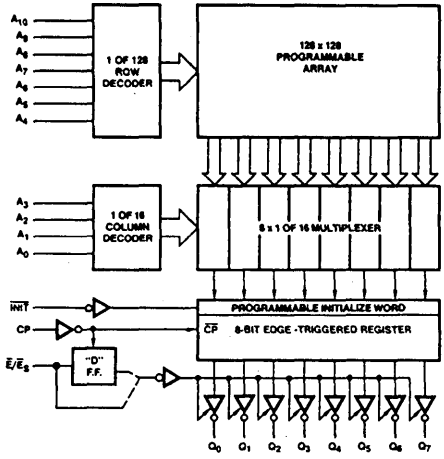
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- User programmable for synchronous or asynchronous enable for simplified word expansion
- Versatile programmable register $\overline{\text{INITIALIZE}}$ either asynchronous (Am27S45A/45) or synchronous (Am27S47A/47)
- Slim, 24-pin, 300-mil lateral center package occupies approximately 1/3 the board space required by standard discrete PROM and register
- Consumes approximately 1/2 the power of separate PROM/register combination for improved system reliability
- Platinum-Silicide fuses guarantee high reliability, fast programming, and exceptionally high programming yields (typ > 98%)

## GENERAL DESCRIPTION

These 16K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 2048 x 8 configuration, they are available in both versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_{10}$ and holding $\overline{CS}_1$ LOW and $CS_2$ and $CS_3$ HIGH. All other valid input conditions on $\overline{CS}_1$, $CS_2$, and $CS_3$ place $O_0 - O_7$ into the OFF or HIGH impedance state.

## BLOCK DIAGRAMS

**Am27S45A/45**

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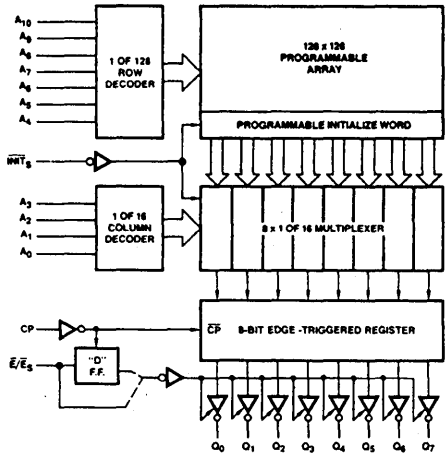
**Am27S47A/47**




BD000370

## PRODUCT SELECTOR GUIDE

| Access Time | 40ns | 45ns | | 50ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Synchronous Initialize | Am27S47A | Am27S47A | Am27S47 | Am27S47 |
| Asynchronous Initialize | Am27S45A | Am27S45A | Am27S45 | Am27S45 |

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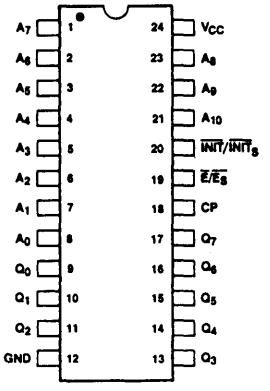
03186B

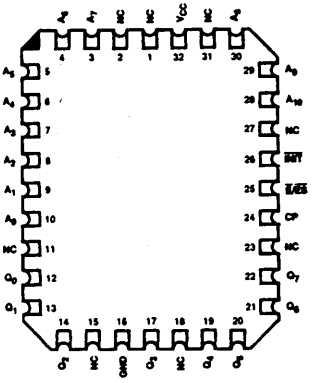
## CONNECTION DIAGRAM
### Top View

**DIP**




CD000460

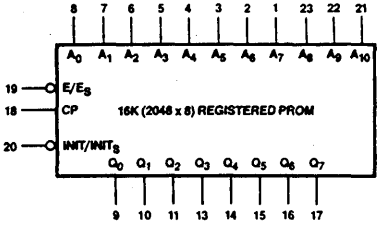
**Chip-Pak™ L-32-2**




CD000470

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL

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VCC = Pin 24
GND = Pin 12

## ORDERING INFORMATION

**Am27S45 A P C B**

- B — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 24-pin ceramic DIP, 300 mil spacing
  - F – 24-pin flatpak
  - L – 32-pin leadless chip carrier
  - P – 24-pin plastic DIP, 300 mil spacing
- A — Speed Select
  - See Product Selector Guide
- Am27S45 — Device Type
  - Am27S45, Am27S45A: Asynchronous
  - Am27S47, Am27S47A: Synchronous

| Valid Combinations | |
|---|---|
| Am27S45<br>Am27S45A<br>Am27S47<br>Am27S47A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## DETAILED DESCRIPTION

The Am27S45A/45 and Am27S47A/47 are Schottky TTL programmable read only memories (PROMs) incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 2048-word by 8-bit organization and are available with three-state outputs. Designed to optimize system performance, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register. The Am27S45A/45 and Am27S47A/47 also offer maximum flexibility for system design by providing either synchronous or asynchronous initialize, and synchronous or asynchronous output enable.

When $V_{CC}$ power is first applied, the state of the outputs will depend on whether the enable has been programmed to be a synchronous or asynchronous enable. If the synchronous enable ($\overline{E}_S$) is being used, the register will be in the set condition causing the outputs ($Q_0$ to $Q_7$) to be in the OFF or HIGH impedance state. If the asynchronous enable ($\overline{E}$) is being used, the outputs will come up in the OFF or HIGH impedance state only if the enable ($\overline{E}$) input is at a logic HIGH level. Reading data is accomplished by first applying the binary word address to the address inputs ($A_0$ through $A_{10}$) and a logic LOW to the enable input. During the address setup time, the stored data is accessed and loaded into the master flip-flops of the data register. Upon the next LOW-to-HIGH transition of the clock input (CP), data is transferred to the slave flip-flops which drive the output buffers, and the accessed data will appear at the outputs ($Q_0$ through $Q_7$). If the asynchronous enable ($\overline{E}$) is being used, the outputs may be disabled at any time by switching the enable to a logic HIGH, and may be returned to the active state by switching the enable back to the logic LOW state. For devices using the synchronous enable ($\overline{E}_S$), the outputs will go into the OFF or HIGH impedance state upon the next positive clock edge after the synchronous enable input is switched to a HIGH level. If the synchronous enable pin is switched to a logic LOW, the next positive clock edge will return the output to the active state. Following a positive clock edge, the address and synchronous enable inputs are free to change, since no change in the output will occur until the next LOW-to-HIGH transition of the clock. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs.

The on-chip edge-triggered register simplifies system timing since the PROM clock may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

These devices also contain a built-in initialize function. When activated, the initialize control input ($\overline{INIT}$) causes the contents of an additional (2049th) 8-bit word to be loaded into the on-chip register. This extra word is user programmable. Since each bit is individually programmable, the initialize function can be used to load any desired combination of HIGHs and LOWs into the register. In the unprogrammed state, activating $\overline{INIT}$ will perform a register CLEAR (all outputs LOW). If all bits of the initialize word are programmed, activating $\overline{INIT}$ performs a register PRESET (all outputs HIGH).

This ability to tailor the initialize outputs to the system requirements simplifies system design and enhances performance. The initialize function is useful during power up and timeout sequences. This flexible feature can also facilitate implementation of other sophisticated functions such as a built-in "jump-start" address.

The Am27S45A/45 has an asynchronous initialize input ($\overline{INIT}$). Applying a LOW to the $\overline{INIT}$ input causes an immediate load of the programmed initialize word into the master and slave flip-flops of the register independent of all other inputs (including CP). The initialize data will appear at the device outputs after the outputs are enabled by bringing the asynchronous enable ($\overline{E}$) LOW.

The Am27S47A/47 has a synchronous $\overline{INIT}_S$ input. Applying a LOW to the $\overline{INIT}_S$ input causes an immediate load of the programmed initialize word into the master flip-flops of the register only independent of all other inputs (including CP). To bring this data to the outputs of a device with a synchronous enable, the synchronous enable ($\overline{E}_S$) should be held LOW until the next LOW-to-HIGH transition of the clock (CP). For a device with an asynchronous enable, the data will appear at the device outputs after the next LOW-to-HIGH clock transition if the enable ($\overline{E}$) is held LOW.

### OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

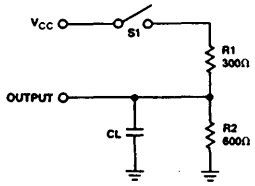
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.38 | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 2) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 2) | | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | | 40 | μA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 3) | | | −20 | −40 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND, $V_{CC}$ = MAX | | | | 130 | 185 | mA |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$V_E$ = 2.4V | (Note 4) | $V_O$ = $V_{CC}$ | | | 40 | μA |
| | | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | | 12 | | pF |

Notes:

1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT

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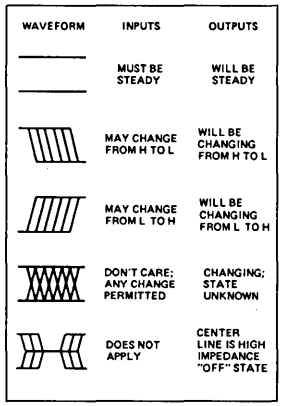
## KEY TO SWITCHING WAVEFORMS

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Notes:

1. $C_L$ = 50pF for all switching characteristics except $t_{PLZ}$ and $t_{PHZ}$.
2. $C_L$ = 5pF for $t_{PLZ}$ and $t_{PHZ}$.
3. $S_1$ is closed for all tests except for $t_{PHZ}$ and $t_{PZH}$.
4. All device test loads should be located within 2″ of device outputs.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | STD C devices Min | STD C devices Max | STD M devices Min | STD M devices Max | A C devices Min | A C devices Max | A M devices Min | A M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_S$(A) | Address to CP (HIGH) Setup Time | | 40 | | 45 | | 45 | | 50 | | ns |
| 2 | $t_H$(A) | Address to CP (HIGH) Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 3 | $t_{PHL}$(CP) | Delay from CP (HIGH) to Output (HIGH or LOW) | All Outputs Simultaneous | | 20 | | 25 | | 25 | | 30 | ns |
| 4 | $t_{PLH}$(CP) | | Single Output (Note 3) | | 18 | | 21 | | 20 | | 23 | ns |
| 5 | $t_{WH}$(CP)<br>$t_{WL}$(CP) | CP Width (HIGH or LOW) | | 20 | | 20 | | 20 | | 20 | | ns |
| 6 | $t_S(\overline{E}_S)$ | $\overline{E}_S$ to CP (HIGH) Setup Time | | 15 | | 15 | | 15 | | 15 | | ns |
| 7 | $t_H(\overline{E}_S)$ | $\overline{E}_S$ to CP (HIGH) Hold Time | | 5 | | 5 | | 5 | | 5 | | ns |
| 8 | $t_{PHL}(\overline{INIT})$<br>$t_{PLH}(\overline{INIT})$ | Delay from $\overline{INIT}$ (LOW) to Outputs (LOW or HIGH) (Note 5) | | | 30 | | 35 | | 35 | | 40 | ns |
| 9 | $t_R(\overline{INIT})$ | $\overline{INIT}$ Recovery (Inactive) to CP (HIGH) (Note 5) | | 20 | | 20 | | 20 | | 20 | | ns |
| 10 | $t_{WL}(\overline{INIT})$ | $\overline{INIT}$ Pulse Width (Note 5) | | 25 | | 30 | | 25 | | 30 | | ns |
| 11 | $t_S(\overline{INIT}_S)$ | $\overline{INIT}_S$ to CP (HIGH) Setup Time (Note 6) | | 25 | | 30 | | 30 | | 35 | | ns |
| 12 | $t_H(\overline{INIT}_S)$ | $\overline{INIT}_S$ to CP (HIGH) Hold Time (Note 6) | | 0 | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{PZL}$(CP)<br>$t_{PZH}$(CP) | Delay from CP (HIGH) to Active Output (HIGH or LOW) (Note 7) | | | 25 | | 30 | | 30 | | 35 | ns |
| 14 | $t_{PLZ}$(CP)<br>$t_{PHZ}$(CP) | Delay from CP (HIGH) to Inactive Output (OFF or HIGH Impedance) (Notes 4 and 7) | | | 25 | | 30 | | 30 | | 35 | ns |
| 15 | $t_{PZL}(\overline{E})$<br>$t_{PZH}(\overline{E})$ | Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) (Note 8) | | | 25 | | 30 | | 30 | | 35 | ns |
| 16 | $t_{PLZ}(\overline{E})$<br>$t_{PHZ}(\overline{E})$ | Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or HIGH Impedance) (Notes 4 and 8) | | | 25 | | 30 | | 30 | | 35 | ns |

Notes:

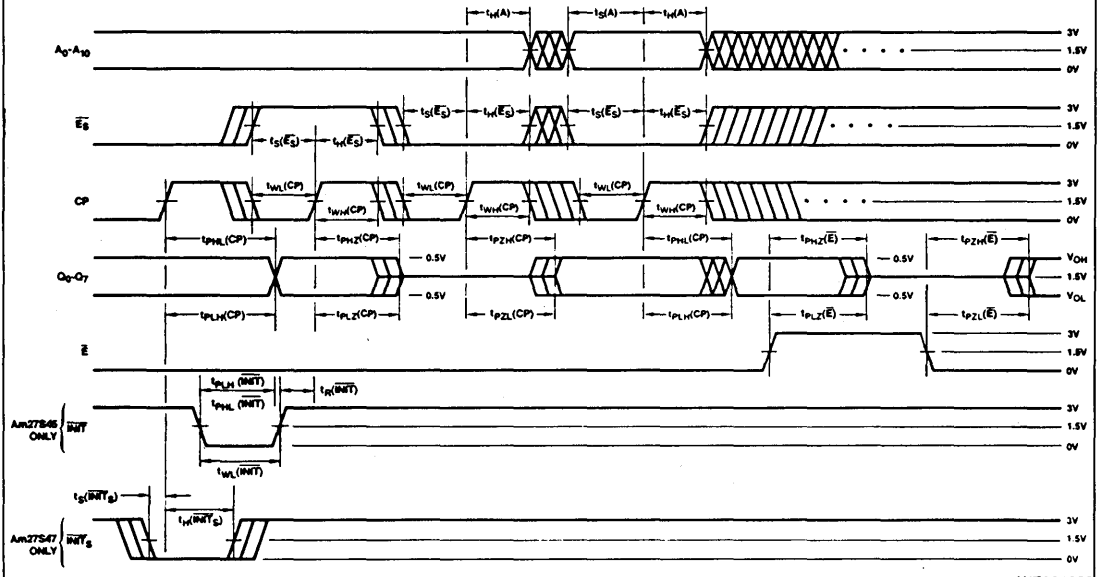
1. Typical values at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.
3. Single register performance numbers provided for comparison with discrete register test data.
4. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$−0.5V and $V_{OL}$+0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
5. Applies only to the Am27S45A/45 (asynchronous $\overline{INITIALIZE}$ function).

## SWITCHING CHARACTERISTICS (Cont.)

6. Applies only to the Am27S47A/47 (synchronous $\overline{\text{INITIALIZE}}$ function).
7. Applies only when synchronous $\overline{\text{ENABLE}}$ function is used.
8. Applies only when asynchronous $\overline{\text{ENABLE}}$ function is used.

## SWITCHING WAVEFORMS

**(See Notes on Testing)**

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### NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device $V_{CC}$ and ground terminals. Multiple capacitors are recommended, including a 0.1$\mu$Farad or larger capacitor and a 0.1$\mu$Farad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S49

8192 x 8 Generic Series Bipolar IMOX™ PROM

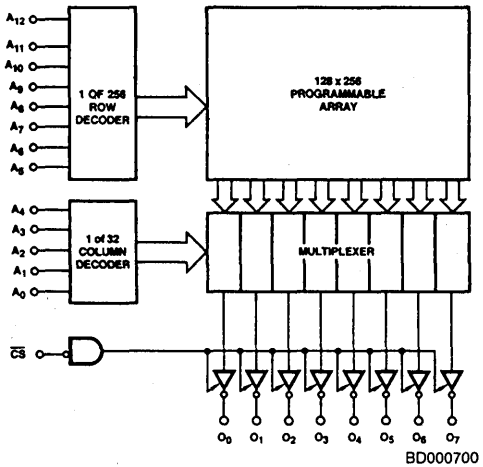
## DISTINCTIVE CHARACTERISTICS

- Ultra fast access time
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range

## GENERAL DESCRIPTION

The Am27S49A and Am27S49 are high speed electrically programmable Schottky read only memories, organized in 8192 x 8 configuration. Outputs are three-state. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_{12}$ and holding the chip select input, LOW. If CS goes to logic HIGH, $O_0 - O_7$ goes to the OFF, or HIGH impedance, state.

## BLOCK DIAGRAM



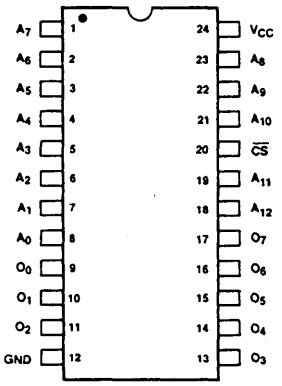

BD000700

## PRODUCT SELECTOR GUIDE

| Access Time | 40ns | 55ns | | 65ns |
|---|---|---|---|---|
| Temperature Range | C | M | C | M |
| Three-State | Am27S49A | Am27S49A | Am27S49 | Am27S49 |

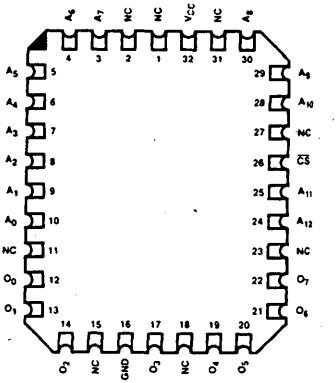
## CONNECTION DIAGRAM
### Top View

**DIP**




CD001030

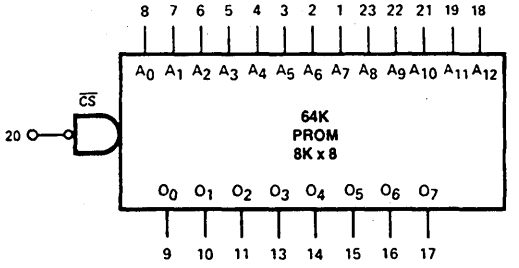
**Chip-Pak™ L-32-2**




CD000970

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000280

## ORDERING INFORMATION

**Am27S49 A P C B**

- **B** — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- **C** — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **P** — Package
  - D – 24-pin ceramic DIP
  - L – 32-pin leadless chip carrier
  - P – 24-pin plastic DIP
- **A** — Speed Select
  - See Product Selector Guide
- **Am27S49** — Device Type
  - 8192 x Bipolar PROM

| Valid Combinations | |
|---|---|
| Am27S49<br>Am27S49A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>LM, LMB |

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

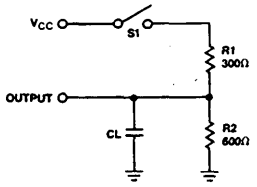
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 2) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 2) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | µA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 3) | | −15 | −40 | −100 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND,<br>$V_{CC}$ = MAX | COM'L | | 160 | 190 | mA |
| | | | MIL | | 160 | 190 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$V_{CS}$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | µA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 4) | | | 5.0 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 4) | | | 8.0 | | |

Notes:

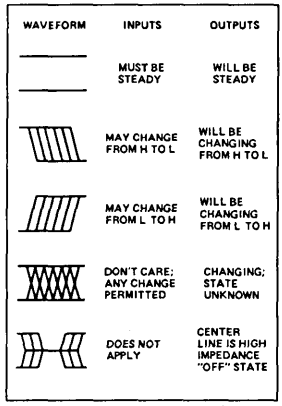
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
3. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST WAVEFORM




TC000170

## KEY TO SWITCHING WAVEFORMS




KS000010

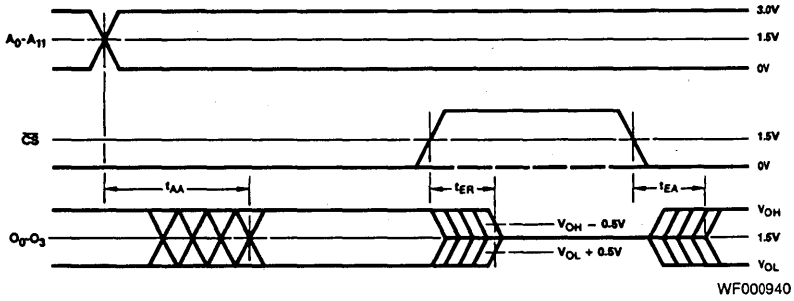
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 35 | 55 | | 35 | 65 | ns |
| | | | A | | 30 | 40 | | 30 | 55 | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 20 | 35 | | 20 | 40 | |
| | | | A | | 20 | 30 | | 20 | 35 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 20 | 35 | | 20 | 40 | |
| | | | A | | 20 | 30 | | 20 | 35 | |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L$ = 30pF.
2. For three-state outputs, $t_{EA}$ is tested with $C_L$ = 30pF to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L$ = 5pF. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}$ – 0.5V; LOW to high impedance tests are made with $S_1$ closed to the $V_{OL}$ + 0.5V level.

## SWITCHING WAVEFORMS




WF000940

Note: Output level while $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S65

(1024 x 4) 4-Wide Bipolar IMOX™ Registered PROM
with SSR™ Diagnostics Capability

## DISTINCTIVE CHARACTERISTICS

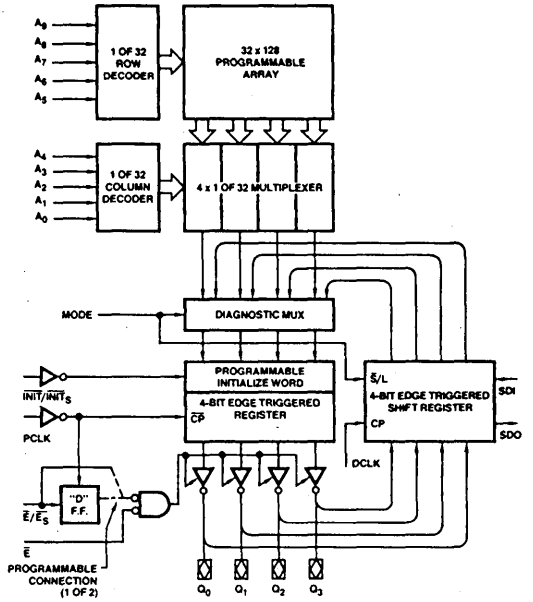
- Highest density fastest performance PROM organization
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable synchronous and asynchronous Enables
- User-programmable for synchronous or asynchronous Initialize
- Increased drive capability, 24mA $I_{OL}$

## GENERAL DESCRIPTION

The Am27S65A/65 (1024-word by 4-bit)is Schottky TTL Programmable Read-only Memory (PROM) incorporating true D-type master-slave data registers on chip. This device is available with three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls. Designed to optimize system performance and provide the systems designer with on-chip SSR diagnostic capability, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

The on-chip edge-triggered register simplifies system timing since the PROM Clock (PCLK) may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

## BLOCK DIAGRAM




BD000680

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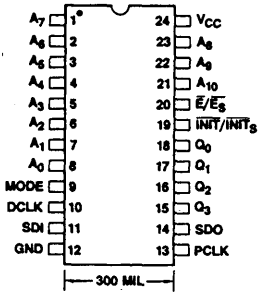
05271A

## PRODUCT SELECTOR GUIDE

| Access Time | 25ns | 30ns | | 35ns |
|---|---|---|---|---|
| Temperature Range | C | C | M | M |
| Part Number | 27S65A | 27S65 | 27S65A | 27S65 |

## CONNECTION DIAGRAM
## Top View

**Am27S65**
**(1024K x 4)**




CD000550

**Chip-pak™**
**Am27S65**
**(1024K x 4)**


Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am27S65 A P C B**

- **B** — Burn-in Option
  - B suffix indicates 160 hour burn-in.
- **C** — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **P** — Package
  - D – 24-pin slim DIP
  - L – 28-pin leadless chip carrier
- **A** — Speed Select
  - 27S65 = Standard
  - 27S65A = High Speed
- **Am27S65** — Device Type
  - 1024 x Bipolar IMOX Registered PROM

| Valid Combinations | |
|---|---|
| Am27S65<br>Am27S65A | DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>LM, LMB |

## MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK as long as no set up or hold times are violated.

| Inputs | | | | | Outputs | | | Operation |
|---|---|---|---|---|---|---|---|---|
| SDI | MODE | DCLK | PCLK | *$\overline{INIT_S}$ | SDO | Shadow Register | Pipeline Register | |
| X | L | ↑ | – | X | $S_3$ | $S_n \leftarrow S_{n-1}$<br>$S_0 \leftarrow SDI$ | NA | Serial Shift; $SDI \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SDO$ |
| X | L | – | ↑ | H | $S_3$ | NA | $Q_n \leftarrow$ ARRAY DATA | Normal Load Pipeline Register from PROM |
| X | L | – | ↑ | L | $S_3$ | NA | $Q_n \leftarrow$ INIT DATA | Synchronous Initialize Pipeline Register |
| L | H | ↑ | – | X | SDI | $S_n \leftarrow Q_n$ | NA | Load Shadow Register from OUTPUTS ($Q_0 - Q_3$) |
| X | H | – | ↑ | X | SDI | NA | $Q_n \leftarrow S_n$ | Load Pipeline Register from Shadow Register |
| H | H | ↑ | – | X | SDI | Hold | NA | No-Op |

**FUNCTION TABLE DEFINITIONS**

**INPUTS**

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

**OUTPUTS**

SDO = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

## DETAILED DESCRIPTION

The Am27S65A/65 contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies the shadow register is intended to be a copy (shadow) of the normal output data register. The shadow register can be used in a systematic way to control and observe the output data register in order to exercise any desired system function during a diagnostic test mode.

## DIAGNOSTIC PIN DESCRIPTION

In general, the implementation of Serial Shadow Register (SSR) diagnostics requires the addition of four extra device pins. These pins are

**Mode Control (MODE)**

Controls the source data for both sets of registers. MODE input is LOW in the normal mode of operation. The PROM array is the input source for the output data registers and the shadow register is in the shift mode ($SDI \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3$/SDO). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output registers or output data bus information may be loaded into the shadow registers.

**Diagnostics Clock (DCLK)**

The diagnostics clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DCLK.

**Serial Data Input (SDI)**

This pin performs two functions depending on the state of the MODE input. If MODE is LOW, the SDI pin is a data transfer pin for serial data ($SDI \rightarrow S_0$. If the MODE input is HIGH, the SDI pin is operating as a control pin where SDI asserted LOW permits output data to be loaded into the shadow register on the next LOW-to-HIGH transition of DCLK. SDI asserted HIGH represents a NO-OP function on this device.

**Serial Data Output (SDO)**

This pin operates as a transfer pin for serial data when the MODE input is LOW ($S_3 \rightarrow$ SDO). When MODE is HIGH and SDI operates as a control pin, the SDO pin operates as a pass through SDI control. SDO is an active totem-pole output.

**DESCRIPTION OF REGISTER CONTROL FUNCTIONS**

In order to offer the system designer maximum flexibility these devices contain a programmable output enable pin and/or a programmable register initialize pin. The unprogrammed state of these pins is asynchronous operation. Should the system design require, either function may be changed to a synchronous mode of operation by programming an architecture word. The functions available are

Asynchronous $\overline{\text{Enable}}$ ($\overline{E}$)

Synchronous $\overline{\text{Enable}}$ ($\overline{E_S}$)

Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$)

Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}_S}$)

The Asynchronous $\overline{\text{Enable}}$ ($\overline{E}$) allows direct control of the three-state output drivers.

The Synchronous $\overline{\text{Enable}}$ ($\overline{E_S}$) is useful where more than one Registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

The initialize function is a programmable word which can be loaded into the output data registers under single pin control. Since each bit is individually programmable, the initialize function can be used to load any combination of HIGHs or LOWs into the output data register. This feature is a superset of commonly used preset and clear functions.

Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$) can be used to generate any arbitrary microinstruction for system interrupt or Reset. This is useful during power-up or timeout sequences.

Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}_S}$) is useful for "trap jumps" or interrupts where execution on the next LOW-to-HIGH Clock transition is required. During this operation MODE input must be held low.

The Am27S65A/65 contains an additional Asynchronous $\overline{\text{Enable}}$ ($\overline{E}$) input on Pin 21 which is not programmable (see block diagram for correct logical implementation).

## PROGRAMMING

The Am27S65A/65 Registered PROM is manufactured with a conductive Platinum-Silicide link at each bit location. The output of this memory with the link in place is LOW. In addition to the programmable fusible link array these devices contain two (2) architecture fuses to program the $\overline{\text{ENABLE}}$ and $\overline{\text{INITIALIZE}}$ input functionality. With these links intact both functions will operate asynchronously. The two-bit architecture word will program functionality according to Table 1.

**TABLE 1**

| Architecture Data Word (Hex) | Am27S65A/65 Input Function | |
|---|---|---|
| | Pin 20 | Pin 19 |
| 0 | Asynchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}}$) | Asynchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}}$) |
| 8 | Synchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}}_\text{S}$) | Asynchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}}$) |
| 4 | Asynchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}}$) | Synchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}}_\text{S}$) |
| C | Synchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}}_\text{S}$) | Synchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}}_\text{S}$) |

An additional four-bit word is available for programming the initialization word. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

Programming each bit location (e.g. opening the fusible links) is accomplished by the following sequence: 1) Power is first applied to $V_{CC}$; 2) SDI input is raised to $V_{IHH}$ (15 volts). This biases internal conditioning and verification circuitry; 3) The appropriate address is selected; 4) a logic HIGH is applied to the MODE input followed by a LOW-to-HIGH transition of PCLK. This will load the output data registers with active HIGH data to protect the outputs during programming; 5) The output to be programmed is then raised to $V_{OP}$ (20 volts). Current from this 20 volt supply is then gated through the addressed fuse by raising the MODE input from a logic HIGH to $V_{IHH}$ (15 volts); 6) After 50$\mu$s, the 20 volt supply is removed; 7) The MODE input is taken from $V_{IHH}$ to a logic LOW. Each data verification must be preceded by a positive going (LOW-to-HIGH) transition of PCLK. This will load the array data into the output data registers. The outputs are then sensed to determine if the link has opened. Most links will open within 50$\mu$s.

Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5ms. If a link has not opened after a total elapsed programming time of 400ms, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to a HIGH level.

When Pin 19 is raised to a logic HIGH level, the programming circuitry for the array is selected and the programming circuitry for the architecture and initialize words is deselected. When Pin 19 is asserted LOW the array programming circuitry is deselected and the programming circuitry for the architecture and initialize words is selected. The architecture and initialize words are then addressed via the $A_0$ input. $A_0$ input LOW addresses the architecture word while $A_0$ input HIGH addresses the initialize word.

An easy implementation would be to invert the next higher address from a PROM programmer and apply this signal to Pin 19. The array, architecture and initialize words would then be programmed according to Table 2.

**TABLE 2**

| Device | Pin 19 | Array Programming Address Field (Hex) | Architecture Word Address (Hex) | Initialize Word Address (Hex) |
|---|---|---|---|---|
| Am27S65A/65 | $\overline{A_{10}}$ | 000 thru 3FF | 400 | 401 |

Special verification circuitry within the device will permit the architecture word to be presented at the outputs for programming verification.

The unused DCLK pin should be terminated either HIGH or LOW during programming in order to avoid the possibility of oscillation.

When programming the Am27S65, Pins 20 and 21 should be held LOW throughout the programming and verification cycle.

High-yield fusing of the Platinum-Silicide fuses requires that a substantial current be delivered to the decoded and selected fuse. The fusing current path has been designed to provide a large fusing current safety margin. This, however, generates large current transients at the time MODE input goes to $V_{IHH}$ and a proportional current decrease at the time the fuse opens. The magnitude of this current change can be between 50 and 150mA with rise or fall times of 2 to 10ns. Some care must be taken to avoid excessive line inductance in the output line to maximize; fusing yields.

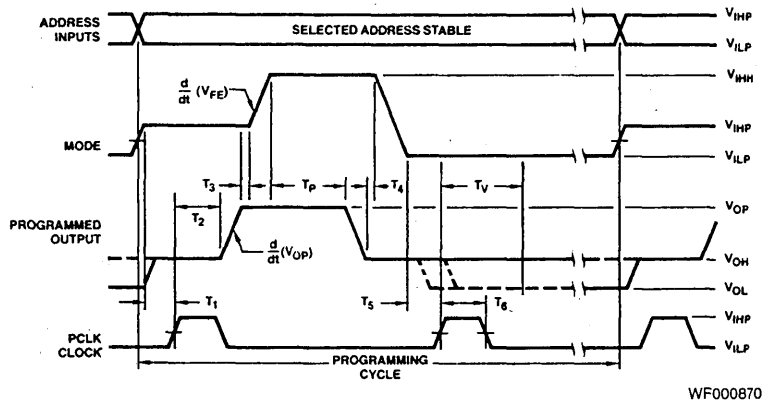
The PROMs may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device for more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including $V_{CC}$ should be removed for a period of 5 seconds after which programming may be resumed.

When all programming has been completed the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an undesired link has been fused. Should this occur, immediately check the programming equipment to make sure all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing. Typical programming yields exceed 98%. Fusing extra bits is generally related to programming equipment problems.

## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IHH}$ | Control Pin Extra High Level | SDI @ 10 – 40mA | 14.5 | 15 | 15.5 | Volts |
| | | MODE @ 10 – 40mA | 14.5 | 15 | 15.5 | |
| $V_{OP}$ | Program Voltage @ 15 – 200mA | | 19.5 | 20 | 20.5 | Volts |
| $V_{IHP}$ | Input High Level During Programming and Verify | | 2.4 | 5 | 5.5 | Volts |
| $V_{ILP}$ | Input Low Level During Programming and Verify | | 0.0 | 0.3 | 0.5 | Volts |
| $V_{CCP}$ | $V_{CC}$ During Programming @ $I_{CC}$ = 50 – 200mA | | 5 | 5.2 | 5.5 | Volts |
| $dV_{OP}/dt$ | Rate of Output Voltage Change | | 20 | | 250 | V/μsec |
| $dV_{FE}/dt$ | Rate of Fusing Enable Voltage Change (MODE Rising Edge) | | 50 | | 1000 | V/μsec |
| $t_P$ | Fusing Time First Attempt | | 40 | 50 | 100 | μsec |
| | Subsequent Attempts | | 4 | 5 | 10 | msec |
| $t_1 - t_6$ | Delays Between Various Level Changes | | 100 | 200 | 1000 | ns |
| $t_V$ | Period During which Output is Sensed for $V_{Blown}$ Level | | | | 500 | ns |
| $V_{ONP}$ | Pull-Up Voltage On Outputs Not Being Programmed | | $V_{CCP}$ – 0.3 | $V_{CCP}$ | $V_{CCP}$ + 0.3 | Volts |
| R | Pull-Up Resistor On Outputs Not Being Programmed | | 0.2 | 2 | 5.1 | kΩ |

## PROGRAMMING WAVEFORMS

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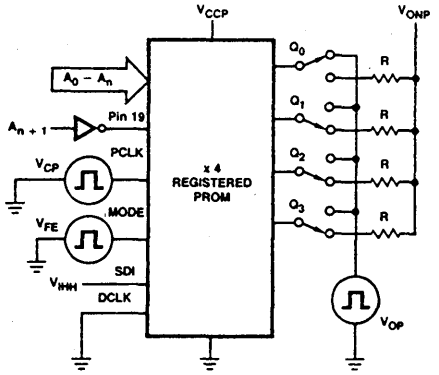
### SIMPLIFIED PROGRAMMING DIAGRAM




PF000110

### PROGRAMMING EQUIPMENT INFORMATION

| | |
|---|---|
| Source and Location | Data I/O<br>10525 Willows Rd. N.E.<br>Redmond, WA 98052 |
| Programmer Mode(s) | Systems 17, 19, 29, and 100 |
| AMD Personality Module | UNIPAK Rev. 005*<br>UNIPAK 2 Rev. V05* |
| Socket Adapter | 351A-073 |

Rev shown is minimum approved revision.



05271A

# APPLYING SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS IN BIPOLAR MICROCOMPUTERS

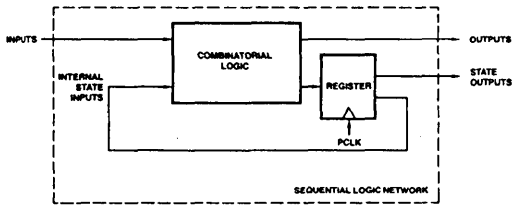
## DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals — address, data, control, and status — to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

## TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.

**Figure 1**

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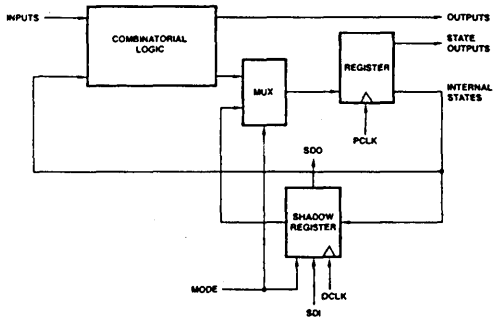
A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

## SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.

**Figure 2**

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Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

When normal pipeline registers are replaced by SSR diagnostics pipeline registers, system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

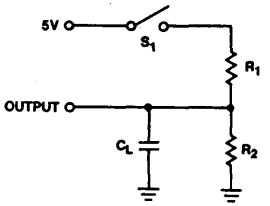
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | See Note 2 | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | See Note 2 | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ ($Q_0$ − $Q_3$) = −2mA | 2.4 | 3.7 | | Volts |
| | | | $I_{OH}$ (SDO) = −0.5mA | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L $I_{OL}$ ($Q_0$ − $Q_3$) = 24mA | | 0.35 | 0.5 | Volts |
| | | | MIL $I_{OL}$ ($Q_0$ − $Q_3$) = 18mA | | | | |
| | | | $I_{OL}$ (SDO) = 4mA | | | | |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max, $V_{IN}$ = 0.4V | | | −40 | −250 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max | $V_{IN}$ = 2.7V | | | 25 | μA |
| | | | $V_{IN}$ = 5.5V | | | 40 | |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max, $V_{OUT}$ = 0V (Note 3) | $Q_0$ − $Q_3$ | −20 | −40 | −90 | mA |
| | | | SDO | −10 | | −85 | |
| $I_{CEX}$ | Output Leakage Current (Three-State) ($Q_0$ − $Q_3$) | $V_{CC}$ = Max, $\overline{E}/E_S$ = 2.4V (Note 4) | $V_{OUT}$ = $V_{CC}$ | | | 50 | μA |
| | | | $V_{OUT}$ = 0.4V | | | −0.15 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max, All Inputs = 2.4V | | | 135 | 185 | mA |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | 12 | | pF |

Notes:

1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT

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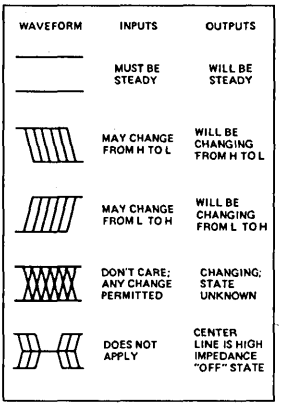
## KEY TO SWITCHING WAVEFORMS




KS000010

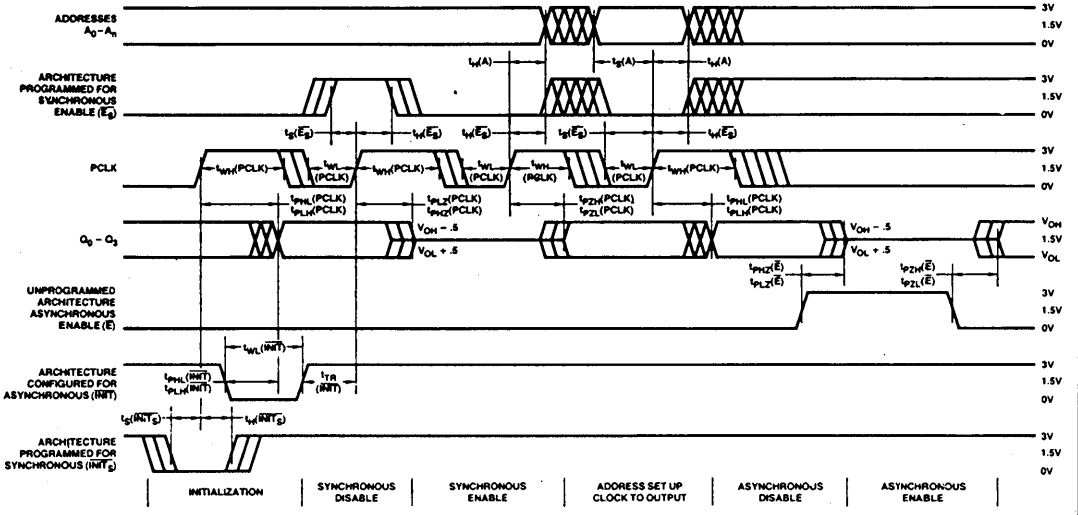
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | "A" Versions COM'L Min | "A" Versions COM'L Max | "A" Versions MIL Min | "A" Versions MIL Max | Standard Versions COM'L Min | Standard Versions COM'L Max | Standard Versions MIL Min | Standard Versions MIL Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_S(A)$ | Address to PCLK (HIGH) Setup Time | 25 | | 30 | | 30 | | 35 | | ns |
| 2 | $t_H(A)$ | Address to PCLK (HIGH) Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| 3 | $t_{PHL}$(PCLK) | Delay from PCLK (HIGH) to Output (HIGH or LOW) | 4 | 12 | 4 | 17 | 4 | 15 | 4 | 20 | ns |
| 4 | $t_{PLH}$(PCLK) | | | | | | | | | | |
| 5 | $t_{WL}$(PCLK) | Clock Pulse Width for Output Data Registers (LOW or HIGH) | 15 | | 20 | | 20 | | 20 | | ns |
| 6 | $t_{WH}$(PCLK) | | | | | | | | | | |
| 7 | $t_{PZL}(\overline{E})$ | Asynchronous Enable - Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) (See Note 4) | | 17 | | 22 | | 20 | | 25 | ns |
| 8 | $t_{PZH}(\overline{E})$ | | | | | | | | | | |
| 9 | $t_{PLZ}(\overline{E})$ | Asynchronous Disable - Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or HIGH Impedance) (See Notes 3 and 4) | | 17 | | 22 | | 20 | | 25 | ns |
| 10 | $t_{PHZ}(\overline{E})$ | | | | | | | | | | |
| 11 | $t_S(\overline{ES})$ | $\overline{ES}$ to PCLK (HIGH) SetUp Time (See Note 5) | 12 | | 12 | | 15 | | 15 | | ns |
| 12 | $t_H(\overline{ES})$ | $\overline{ES}$ to PCLK (HIGH) Hold Time (See Note 5) | 0 | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{PZL}$(PCLK) | Synchronous Enable - Delay from PCLK (HIGH) to Active Output (HIGH or LOW) (See Note 5) | | 17 | | 22 | | 20 | | 25 | ns |
| 14 | $t_{PZH}$(PCLK) | | | | | | | | | | |
| 15 | $t_{PLZ}$(PCLK) | Synchronous Disable - Delay from PCLK (HIGH) to Inactive Output (OFF or HIGH Impedance) (See Notes 3 and 5) | | 17 | | 22 | | 20 | | 25 | ns |
| 16 | $t_{PHZ}$(PCLK) | | | | | | | | | | |
| 17 | $t_{PHL}(\overline{INIT})$ | Delay from Asynchronous $\overline{INIT}$ (LOW) to Outputs (LOW or HIGH) (See Note 6) | | 25 | | 30 | | 30 | | 35 | ns |
| 18 | $t_{PLH}(\overline{INIT})$ | | | | | | | | | | |
| 19 | $t_R(\overline{INIT})$ | Asynchronous $\overline{INIT}$ Recovery ($\overline{INIT}$ 5) to PCLK (HIGH) (See Note 6) | 20 | | 25 | | 25 | | 30 | | ns |
| 20 | $t_{WL}(\overline{INIT})$ | Asynchronous $\overline{INIT}$ Pulse Width (LOW) (See Note 6) | 20 | | 20 | | 25 | | 25 | | ns |
| 21 | $t_S(\overline{INIT})$ | Synchronous $\overline{INIT}$ (LOW) to PCLK (HIGH) Set-Up Time (See Note 7) | 15 | | 20 | | 20 | | 25 | | ns |
| 22 | $t_H(\overline{INIT})$ | Synchronous $\overline{INIT}$ (LOW) to PCLK (HIGH) Hold Time (See Note 7) | 5 | | 5 | | 5 | | 5 | | ns |

See also AC test loads and notes 2, 3, 8, 9, 10.

## SWITCHING WAVEFORMS

for Typical Registered PROM applications
(See Notes on Testing)




WF000830

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | COM'L Min | COM'L Max | MIL Min | MIL Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | $t_S$(SDI) | Serial Data In to DCLK (HIGH) SetUp Time | 25 | | 30 | | ns |
| 2 | $t_H$(SDI) | Serial Data In to DCLK (HIGH) Hold Time | 0 | | 0 | | |
| 3 | $t_S$(MODE) | MODE to PCLK (HIGH) or DLCK(HIGH) SetUp Time | 25 | | 30 | | |
| 4 | $t_H$(MODE) | MODE to PCLK (HIGH) or DCLK (HIGH) Hold Time | 0 | | 0 | | |
| 5 | $t_s$(Q) | Output to DCLK (HIGH) Setup Time | 25 | | 30 | | |
| 6 | $t_H$(Q) | Output to DCLK (HIGH) Hold Time | 10 | | 15 | | |
| 7 | $t_{PHL}$(DCLK) | Delay from DCLK (HIGH) to Serial Data Output (HIGH or LOW) | | 30 | | 40 | |
| 8 | $t_{PLH}$(DCLK) | | | | | | |
| 9 | $t_{PHL}$(SDI) | Delay from Serial Data Input (LOW or HIGH) to Serial Data Output (LOW or HIGH)-MODE Input HIGH | | 25 | | 30 | |
| 10 | $t_{PLH}$(SDI) | | | | | | |
| 11 | $t_{WL}$(DCLK) | Clock Pulse Width for Diagnostic Register(LOW or HIGH) | 25 | | 25 | | |
| 12 | $t_{WH}$(DCLK) | | | | | | |

Notes:

1. Typical values are taken at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.
3. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$ – 0.5V and $V_{OL}$ + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
4. Applies only if the architecture is configured for Asynchronous $\overline{\text{Enable}}$.
5. Applies only if the architecture word has been programmed for a Synchronous $\overline{\text{Enable}}$ input.
6. Applies only if the architecture is configured for Asynchronous $\overline{\text{Initialize}}$.
7. Applies only if the architecture word has been programmed for a Synchronous $\overline{\text{Initialize}}$ input.
8. Component values for AC TEST LOAD are: $R_1$ = 300, $R_2$ = 600, and $C_L$ = 50pF for $Q_0 - Q_3$ outputs, $R_1$ = 1100, $R_2$ = 2400, and $C_L$ = 15pF for SDO output.
9. All device test loads should be located within 2" of device outputs.
10. $S_1$ is open for $t_{PHZ}$ and $t_{PZH}$ tests. $S_1$ is closed for all other AC tests.



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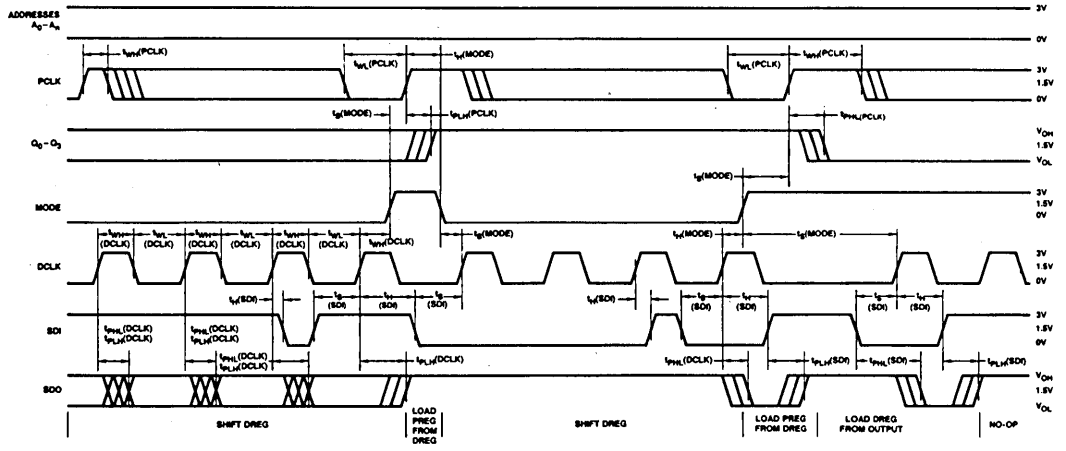
## SWITCHING WAVEFORMS

for Diagnostics applications

(See Notes on Testing)




WF000840

## NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device $V_{CC}$ and ground terminals. Multiple capacitors are recommended, including a 0.1$\mu$Farad or larger capacitor and a 0.01$\mu$Farad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S75

(2048 x 4) 4-Wide Bipolar IMOX™
Registered PROM with SSR™ Diagnostics Capability



## DISTINCTIVE CHARACTERISTICS

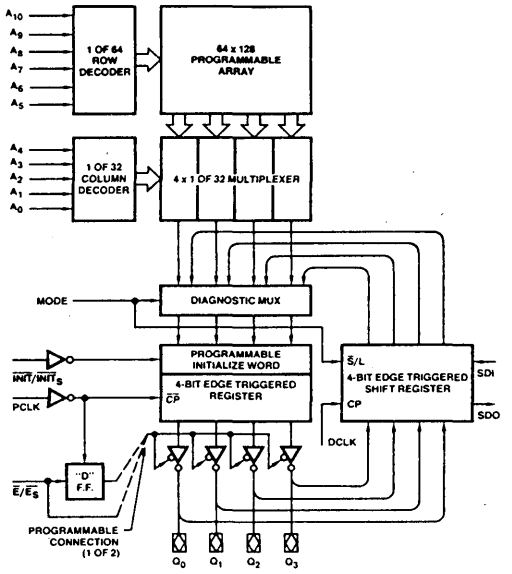
- Highest density fastest performance PROM organization
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable synchronous and asynchronous Enables
- User-programmable for synchronous or asynchronous Initialize
- Increased drive capability, 24mA $I_{OL}$

## GENERAL DESCRIPTION

The Am27S75A/75 (2048-word by 4-bit) is Schottky TTL Programmable Read-only Memory (PROM) incorporating true D-type master-slave data registers on chip. This device is available with three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls. Designed to optimize system performance and provide the systems designer with on-chip SSR diagnostic capability, this device also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

The on-chip edge-triggered register simplifies system timing since the PROM Clock (PCLK) may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

## BLOCK DIAGRAM



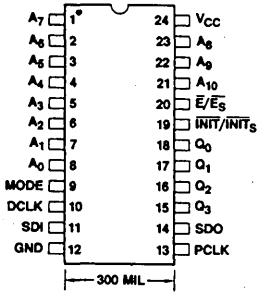

BD000390

## PRODUCT SELECTOR GUIDE

| Access Time | 25ns | 30ns | | 35ns |
|---|---|---|---|---|
| Temperature Range | C | C | M | M |
| Part Number | 27S75A | 27S75 | 27S75A | 27S75 |

## CONNECTION DIAGRAM
Top View

**Am27S75**
**(2048 x 4)**




CD000550

**Chip-Pak™**
**Am27S75**
**(2048 x 4)**


Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am27S75 A D C B**

- **B** — Burn-in Option
  - C = No Burn-in
  - B = 160hr Burn-in
- **C** — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – CERDIP
  - L – Chip-pak*
- **A** — Speed Select
  - No Code = Standard
  - A = High Speed
- **Am27S75** — Device Type
  - 2048 x Bipolar IMOX Registered PROM

| Valid Combinations | |
|---|---|
| Am27S75<br>Am27S75A | DC,DCB,<br>LC,LCB,<br>DM,DMB,<br>LM,LMB |

*Chip-pak are rated at maximum case temparature only. This package will be available soon. Consult factory.

This device is also available in die form to commercial and military specifications.
Pad layout and bonding diagram available upon request.

Chip-pak is a trademark of Advanced Micro Devices, Inc.

## MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK as long as no set up or hold times are violated.

| Inputs | | | | | Outputs | | | Operation |
|---|---|---|---|---|---|---|---|---|
| SDI | MODE | DCLK | PCLK | $\overline{INIT}$s* | SDO | Shadow Register | Pipeline Register | |
| X | L | ↑ | – | X | $S_3$ | $S_n \leftarrow S_{n-1}$<br>$S_0 \leftarrow$ SDI | NA | Serial Shift; SDI → $S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3$/SDO |
| X | L | – | ↑ | H | $S_3$ | NA | $Q_n \leftarrow$ ARRAY DATA | Normal Load Pipeline Register from PROM |
| X | L | – | ↑ | L | $S_3$ | NA | $Q_n \leftarrow$ INIT DATA | Synchronous Initialize Pipeline Register |
| L | H | ↑ | – | X | SDI | $S_n \leftarrow Q_n$ | NA | Load Shadow Register from OUTPUTS ($Q_0 - Q_3$) |
| X | H | – | ↑ | X | SDI | NA | $Q_n \leftarrow S_n$ | Load Pipeline Register from Shadow Register |
| H | H | ↑ | – | X | SDI | Hold | NA | No-Op |

**MODE SELECT TABLE DEFINITIONS**

**INPUTS**

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

**OUTPUTS**

SDO = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

## DETAILED DESCRIPTION

The Am27S75A/75 contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies the shadow register is intended to be a copy (shadow) of the normal output data register. The shadow register can be used in a systematic way to control and observe the output data register in order to exercise any desired system function during a diagnostic test mode.

### DIAGNOSTIC PIN DESCRIPTION

In general, the implementation of Serial Shadow Register (SSR) diagnostics requires the addition of four extra device pins. These pins are

**Mode Control (MODE)**

Controls the source data for both sets of registers. MODE input is LOW in the normal mode of operation. The PROM array is the input source for the output data registers and the shadow register is in the shift mode (SDI → $S_0$ → $S_1$ → $S_2$ → $S_3$/SDO). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output registers or output data bus information may be loaded into the shadow registers.

**Diagnostics Clock (DCLK)**

The diagnostics clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DCLK.

**Serial Data Input (SDI)**

This pin performs two functions depending on the state of the MODE input. If MODE is LOW, the SDI pin is a data transfer pin for serial data (SDI → $S_0$. If the MODE input is HIGH, the SDI pin is operating as a control pin where SDI asserted LOW permits output data to be loaded into the shadow register on the next LOW-to-HIGH transition of DCLK. SDI asserted HIGH represents a NO-OP function on this device.

**Serial Data Output (SDO)**

This pin operates as a transfer pin for serial data when the MODE input is LOW ($S_3$ → SDO). When MODE is HIGH and SDI operates as a control pin, the SDO pin operates as a pass through of SDI control. SDO is an active totem-pole output.

### DESCRIPTION OF REGISTER CONTROL FUNCTIONS

In order to offer the system designer maximum flexibility these devices contain a programmable output enable pin and/or a programmable register initialize pin. The unprogrammed state of these pins is asynchronous operation. Should the system design require, either function may be changed to a synchronous mode of operation by programming an architecture word. The functions available are

Asynchronous $\overline{\text{Enable}}$ ($\overline{E}$)

Synchronous $\overline{\text{Enable}}$ ($\overline{E_S}$)

Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$)

Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}_S}$)

The Asynchronous $\overline{\text{Enable}}$ ($\overline{E}$) allows direct control of the three-state output drivers.

The Synchronous $\overline{\text{Enable}}$ ($\overline{E_S}$) is useful where more than one Registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

The initialize function is a programmable word which can be loaded into the output data registers under single pin control. Since each bit is individually programmable, the initialize function can be used to load any combination of HIGHs or LOWs into the output data register. This feature is a superset of commonly used preset and clear functions.

Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$) can be used to generate any arbitrary microinstruction for system interrupt or Reset. This is useful during power-up or timeout sequences.

Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}_S}$) is useful for "trap jumps" or interrupts where execution on the next LOW-to-HIGH Clock transition is required. During this operation MODE input must be held low.

The Am27S65A/65 contains an additional Asynchronous $\overline{\text{Enable}}$ ($\overline{E}$) input on Pin 21 which is not programmable (see block diagram for correct logical implementation).

The Am27S85A/85 contains a single programmable multifunctional input on Pin 19. The unprogrammed state of this pin operates as an Asynchronous $\overline{\text{Enable}}$ ($\overline{E}$) input. The architecture word permits programming the functionality to Synchronous $\overline{\text{Enable}}$ ($\overline{E_S}$), Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$), or Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}_S}$).

## PROGRAMMING

The Am27S75A/75 Registered PROM is manufactured with a conductive Platinum-Silicide link at each bit location. The output of these memories with the link in place is LOW. In addition to the programmable fusible link array these devices contain two (2) architecture fuses to program the $\overline{\text{ENABLE}}$ and $\overline{\text{INITIALIZE}}$ input functionality. With these links intact both functions will operate asynchronously. The two-bit architecture word will program functionality according to Table 1.

**TABLE 1**

| Architecture Data Word (Hex) | Am27S75A/75 Input Function | |
|---|---|---|
| | Pin 20 | Pin 19 |
| 0 | Asynchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}}$) | Asynchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}}$) |
| 8 | Synchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}_S}$) | Asynchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}}$) |
| 4 | Asynchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}}$) | Synchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}_S}$) |
| C | Synchronous $\overline{\text{ENABLE}}$ ($\overline{\text{E}_S}$) | Synchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}_S}$) |

An additional four-bit word is available for programming the initialization word. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

Programming each bit location (e.g. opening the fusible links) is accomplished by the following sequence: 1) Power is first applied to $V_{CC}$; 2) SDI input is raised to $V_{IHH}$ (15 volts). This biases internal conditioning and verification circuitry; 3) The appropriate address is selected; 4) a logic HIGH is applied to the MODE input followed by a LOW-to-HIGH transition of PCLK. This will load the output data registers with active HIGH data to protect the outputs during programming; 5) The output to be programmed is then raised to $V_{OP}$ (20 volts). Current from this 20 volt supply is then gated through the addressed fuse by raising the MODE input from a logic HIGH to $V_{IHH}$ (15 volts); 6) After 50$\mu$s, the 20 volt supply is removed; 7) The MODE input is taken from $V_{IHH}$ to a logic LOW. Each data verification must be preceded by a positive going (LOW-to-HIGH) transition of PCLK. This will load the array data into the output data registers. The outputs are then sensed to determine if the link has opened. Most links will open within 50$\mu$s. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5ms. If a link has not opened after a total elapsed programming time of 400ms, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to a HIGH level.

When Pin 19 is raised to a logic HIGH level, the programming circuitry for the array is selected and the programming circuitry for the architecture and initialize words is deselected. When Pin 19 is asserted LOW the array programming circuitry is deselected and the programming circuitry for the architecture and initialize words is selected. The architecture and initialize words are then addressed via the $A_0$ input. $A_0$ input LOW addresses the architecture word while $A_0$ input HIGH addresses the initialize word.

An easy implementation would be to invert the next higher address from a PROM programmer and apply this signal to Pin 19. The array, architecture and initialize words would then be programmed according to Table 2.

**TABLE 2**

| Device | Pin 19 | Array Programming Address Field (Hex) | Architecture Word Address (Hex) | Initialize Word Address (Hex) |
|---|---|---|---|---|
| Am27S75A/75 | $\overline{A_{11}}$ | 000 thru 7FF | 800 | 801 |

Special verification circuitry within the device will permit the architecture word to be presented at the outputs for programming verification.

The unused DCLK pin should be terminated either HIGH or LOW during programming in order to avoid the possibility of oscillation.

High-yield fusing of the Platinum-Silicide fuses requires that a substantial current be delivered to the decoded and selected fuse. The fusing current path has been designed to provide a large fusing current safety margin. This, however, generates large current transients at the time MODE input goes to $V_{IHH}$ and a proportional current decrease at the time the fuse opens. The magnitude of this current change can be between 50 and 150mA with rise or fall times of 2 to 10ns. Some care must be taken to avoid excessive line inductance in the output line to maximize fusing yields.

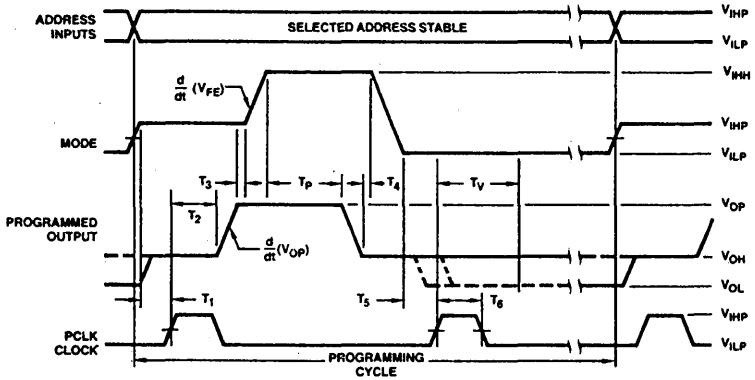
The PROMs may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device for more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including $V_{CC}$ should be removed for a period of 5 seconds after which programming may be resumed.

When all programming has been completed the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an undesired link has been fused. Should this occur, immediately check the programming equipment to make sure all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins and that the programming voltages are within the specified limits. All these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing. Typical programming yields exceed 98%. Fusing extra bits is generally related to programming equipment problems.

## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IHH}$ | Control Pin Extra High Level | SDI @ 10 – 40mA | 14.5 | 15 | 15.5 | Volts |
| | | MODE @ 10 – 40mA | 14.5 | 15 | 15.5 | |
| $V_{OP}$ | Program Voltage @ 15 – 200mA | | 19.5 | 20 | 20.5 | Volts |
| $V_{IHP}$ | Input High Level During Programming and Verify | | 2.4 | 5 | 5.5 | Volts |
| $V_{ILP}$ | Input Low Level During Programming and Verify | | 0.0 | 0.3 | 0.5 | Volts |
| $V_{CCP}$ | $V_{CC}$ During Programming @ $I_{CC}$ = 50 – 200mA | | 5 | 5.2 | 5.5 | Volts |
| $dV_{OP}/dt$ | Rate of Output Voltage Change | | 20 | | 250 | V/μsec |
| $dV_{FE}/dt$ | Rate of Fusing Enable Voltage Change (MODE Rising Edge) | | 50 | | 1000 | V/μsec |
| $t_P$ | Fusing Time First Attempt | | 40 | 50 | 100 | μsec |
| | Subsequent Attempts | | 4 | 5 | 10 | msec |
| $t_1 - t_6$ | Delays Between Various Level Changes | | 100 | 200 | 1000 | ns |
| $t_V$ | Period During which Output is Sensed for $V_{Blown}$ Level | | | | 500 | ns |
| $V_{ONP}$ | Pull-Up Voltage On Outputs Not Being Programmed | | $V_{CCP}$ – 0.3 | $V_{CCP}$ | $V_{CCP}$ + 0.3 | Volts |
| R | Pull-Up Resistor On Outputs Not Being Programmed | | 0.2 | 2 | 5.1 | kΩ |

## PROGRAMMING WAVEFORMS

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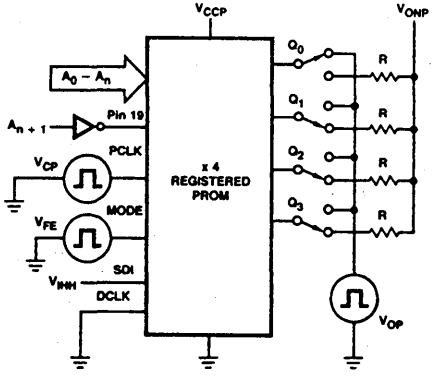
### SIMPLIFIED PROGRAMMING DIAGRAM

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### PROGRAMMING EQUIPMENT INFORMATION

| | |
|---|---|
| Source and Location | Data I/O<br>10525 Willows Rd. N.E.<br>Redmond, WA 98052 |
| Programmer Mode(s) | Systems 17, 19, 29, and 100 |
| AMD Personality Module | UNIPAK Rev. 005*<br>UNIPAK 2 Rev. V05* |
| Socket Adapter | 351A-073 |

*Rev shown is minimum approved revision.

# APPLYING SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS IN BIPOLAR MICROCOMPUTERS

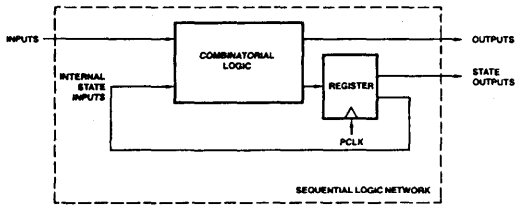
## DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals – address, data, control, and status – to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs and determine whether the system is functioning correctly.

## TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.

**Figure 1**

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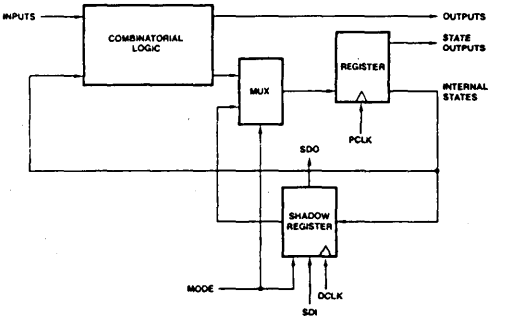
A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

## SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.

**Figure 2**

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Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicato or shadow of each state flip/flop in an additional registor. Tho shadow register can be loaded serially via tho sorial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into tho internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

When normal pipeline registers are replaced by SSR diagnostics pipeline registers, system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

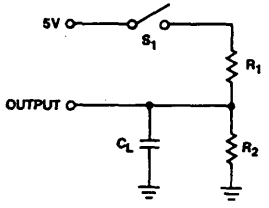
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | See Note 2 | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | See Note 2 | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ ($Q_0$ − $Q_3$) = −2mA | 2.4 | 3.7 | | Volts |
| | | | $I_{OH}$ (SDO) = −0.5mA | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L $I_{OL}$ ($Q_0$ − $Q_3$) = 24mA | | 0.35 | 0.5 | Volts |
| | | | MIL $I_{OL}$ ($Q_0$ − $Q_3$) = 18mA | | | | |
| | | | $I_{OL}$ (SDO) = 4mA | | | | |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max, $V_{IN}$ = 0.4V | | | −40 | −250 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max | $V_{IN}$ = 2.7V | | | 25 | µA |
| | | | $V_{IN}$ = 5.5V | | | 40 | |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max, $V_{OUT}$ = 0V (Note 3) | $Q_0$ − $Q_3$ | −20 | −40 | −90 | mA |
| | | | SDO | −10 | | −85 | |
| $I_{CEX}$ | Output Leakage Current (Three-State) ($Q_0$ − $Q_3$) | $V_{CC}$ = Max, $\overline{VE}/E_S$ = 2.4V (Note 4) | $V_{OUT}$ = $V_{CC}$ | | | 50 | µA |
| | | | $V_{OUT}$ = 0.4V | | | −0.15 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max, All Inputs = 2.4V | | | 135 | 185 | mA |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | 12 | | pF |

Notes:

1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT

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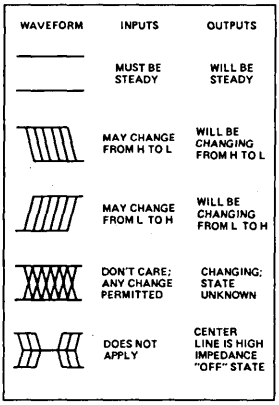
## KEY TO SWITCHING WAVEFORMS

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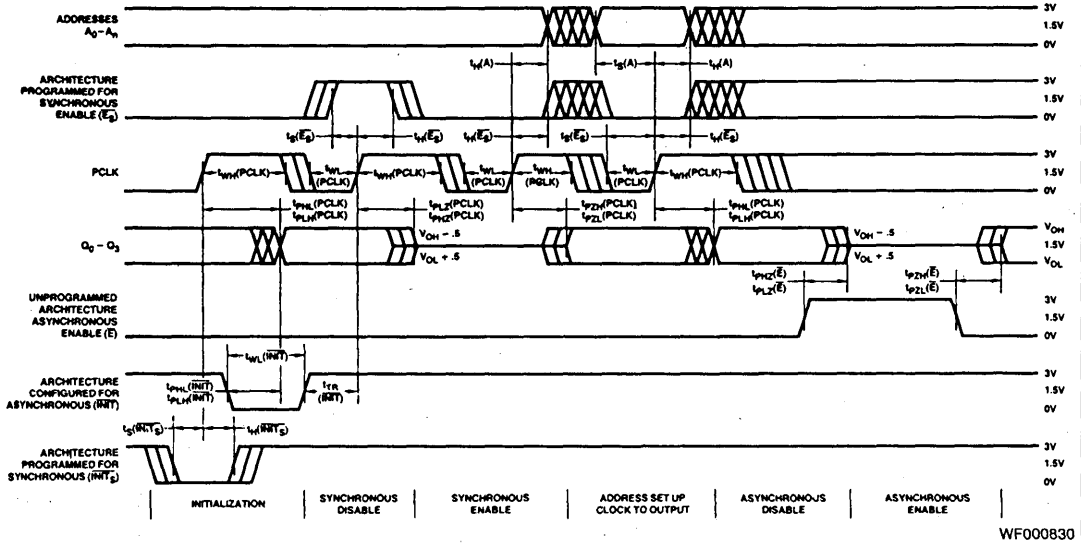
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | "A" Versions COM'L Min | "A" Versions COM'L Max | "A" Versions MIL Min | "A" Versions MIL Max | Standard Versions COM'L Min | Standard Versions COM'L Max | Standard Versions MIL Min | Standard Versions MIL Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_S(A)$ | Address to PCLK (HIGH) Setup Time | 25 | | 30 | | 30 | | 35 | | ns |
| 2 | $t_H(A)$ | Address to PCLK (HIGH) Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| 3 | $t_{PHL}$(PCLK) | Delay from PCLK (HIGH) to Output (HIGH or LOW) | 4 | 12 | 4 | 17 | 4 | 15 | 4 | 20 | ns |
| 4 | $t_{PLH}$(PCLK) | | | | | | | | | | |
| 5 | $t_{WL}$(PCLK) | Clock Pulse Width for Output Data Registers (LOW or HIGH) | 15 | | 20 | | 20 | | 20 | | ns |
| 6 | $t_{WH}$(PCLK) | | | | | | | | | | |
| 7 | $t_{PZL}(\overline{E})$ | Asynchronous Enable - Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) (See Note 4) | | 17 | | 22 | | 20 | | 25 | ns |
| 8 | $t_{PZH}(\overline{E})$ | | | | | | | | | | |
| 9 | $t_{PLZ}(\overline{E})$ | Asynchronous Disable - Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or HIGH Impedance) (See Notes 3 and 4) | | 17 | | 22 | | 20 | | 25 | ns |
| 10 | $t_{PHZ}(\overline{E})$ | | | | | | | | | | |
| 11 | $t_S(\overline{ES})$ | $\overline{ES}$ to PCLK (HIGH) Set-Up Time (See Note 5) | 12 | | 12 | | 15 | | 15 | | ns |
| 12 | $t_H(\overline{ES})$ | $\overline{ES}$ to PCLK (HIGH) Hold Time (See Note 5) | 0 | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{PZL}$(PCLK) | Synchronous Enable - Delay from PCLK (HIGH) to Active Output (HIGH or LOW) (See Note 5) | | 17 | | 22 | | 20 | | 25 | ns |
| 14 | $t_{PZH}$(PCLK) | | | | | | | | | | |
| 15 | $t_{PLZ}$(PCLK) | Synchronous Disable - Delay from PCLK (HIGH) to Inactive Output (OFF or HIGH Impedance) (See Notes 3 and 5) | | 17 | | 22 | | 20 | | 25 | ns |
| 16 | $t_{PHZ}$(PCLK) | | | | | | | | | | |
| 17 | $t_{PHL}(\overline{INIT})$ | Delay from Asynchronous $\overline{INIT}$ (LOW) to Outputs (LOW or HIGH) (See Note 6) | | 25 | | 30 | | 30 | | 35 | ns |
| 18 | $t_{PLH}(\overline{INIT})$ | | | | | | | | | | |
| 19 | $t_R(\overline{INIT})$ | Asynchronous $\overline{INIT}$ Recovery ($\overline{INIT}$ 5) to PCLK (HIGH) (See Note 6) | 20 | | 25 | | 25 | | 30 | | ns |
| 20 | $t_{WL}(\overline{INIT})$ | Asynchronous $\overline{INIT}$ Pulse Width (LOW) (See Note 6) | 20 | | 20 | | 25 | | 25 | | ns |
| 21 | $t_S(\overline{INIT})$ | Synchronous $\overline{INIT}$ (LOW) to PCLK (HIGH) Set-Up Time (See Note 7) | 15 | | 20 | | 20 | | 25 | | ns |
| 22 | $t_H(\overline{INIT})$ | Synchronous $\overline{INIT}$ (LOW) to PCLK (HIGH) Hold Time (See Note 7) | 5 | | 5 | | 5 | | 5 | | ns |

See also AC test loads and notes 2, 3, 8, 9, 10.

## SWITCHING WAVEFORMS

for Typical Registered PROM applications
(See Notes on Testing)

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## DIAGNOSTIC MODE SWITCHING CHARACTERISTICS

### OVER OPERATING RANGE (Unless otherwise noted)

| No. | Symbol | Description | COM'L Min | COM'L Max | MIL Min | MIL Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | $t_S$(SDI) | Serial Data In to DCLK (HIGH) Set-Up Time | 25 | | 30 | | ns |
| 2 | $t_H$(SDI) | Serial Data In to DCLK (HIGH) Hold Time | 0 | | 0 | | |
| 3 | $t_S$(MODE) | MODE to PCLK (HIGH) or DLCK(HIGH) Set-Up Time | 25 | | 30 | | |
| 4 | $t_H$(MODE) | MODE to PCLK (HIGH) or DCLK (HIGH) Hold Time | 0 | | 0 | | |
| 5 | $t_s$(Q) | Output to DCLK (HIGH) Setup Time | 25 | | 30 | | |
| 6 | $t_H$(Q) | Output to DCLK (HIGH) Hold Time | 10 | | 15 | | |
| 7 | $t_{PHL}$(DCLK) | Delay from DCLK (HIGH) to Serial Data Output (HIGH or LOW) | | 30 | | 40 | |
| 8 | $t_{PLH}$(DCLK) | | | | | | |
| 9 | $t_{PHL}$(SDI) | Delay from Serial Data Input (LOW or HIGH) to Serial Data Output (LOW or HIGH)-MODE Input HIGH | | 25 | | 30 | |
| 10 | $t_{PLH}$(SDI) | | | | | | |
| 11 | $t_{WL}$(DCLK) | Clock Pulse Width for Diagnostic Register(LOW or HIGH) | 25 | | 25 | | |
| 12 | $t_{WH}$(DCLK) | | | | | | |

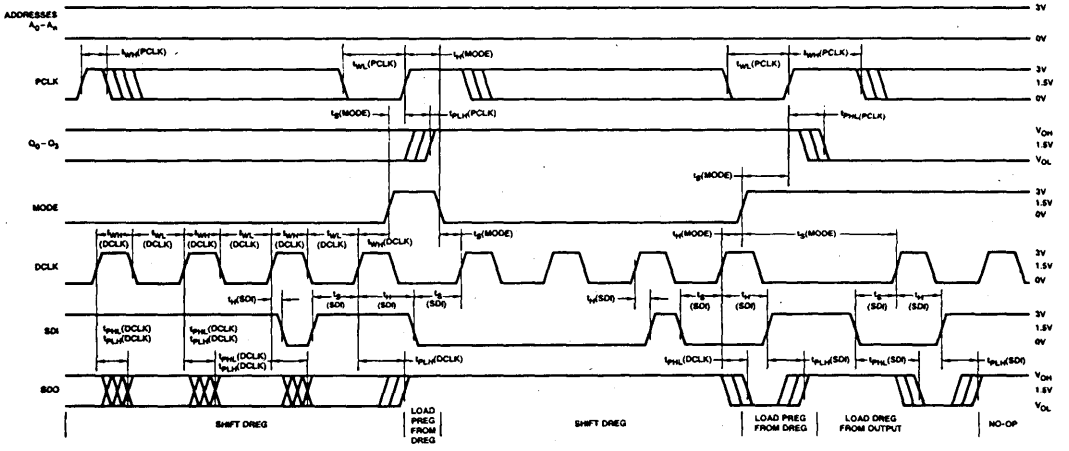
Notes:

1. Typical values are taken at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.
3. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$ – 0.5V and $V_{OL}$ + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
4. Applies only if the architecture is configured for Asynchronous $\overline{\text{Enable}}$.
5. Applies only if the architecture word has been programmed for a Synchronous $\overline{\text{Enable}}$ input.
6. Applies only if the architecture is configured for Asynchronous $\overline{\text{Initialize}}$.
7. Applies only if the architecture word has been programmed for a Synchronous $\overline{\text{Initialize}}$ input.
8. Component values for AC TEST LOAD are: $R_1$ = 300, $R_2$ = 600, and $C_L$ = 50pF for $Q_0$ – $Q_3$ outputs, $R_1$ = 1100, $R_2$ = 2400, and $C_L$ = 15pF for SDO output.
9. All device test loads should be located within 2″ of device outputs.
10. $S_1$ is open for $t_{PHZ}$ and $t_{PZH}$ tests. $S_1$ is closed for all other AC tests.

## SWITCHING WAVEFORMS

for Diagnostics applications

(See Notes on Testing)

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## NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device $V_{CC}$ and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S85

(1024 x 4) 4-Wide Bipolar IMOX™
Registered PROM with SSR™ Diagnostics Capability

## DISTINCTIVE CHARACTERISTICS

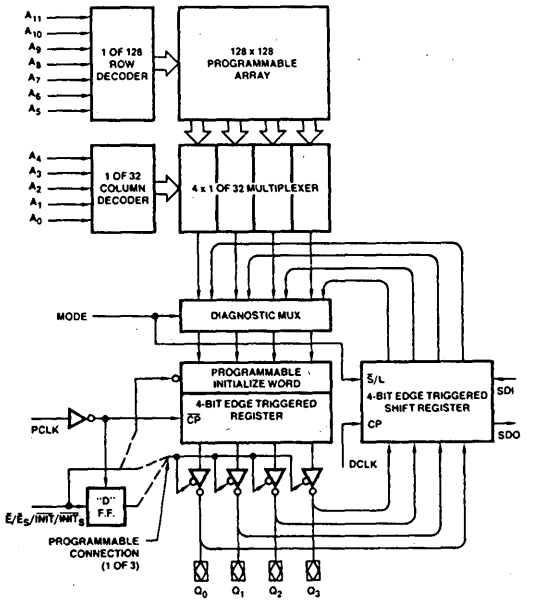
- Highest density fastest performance PROM organization
- On-chip edge-triggered registers — ideal for pipelined microprogrammed systems
- On-chip diagnostic shift register for serial observability and controllability of the output register
- User-programmable synchronous and asynchronous Enables
- User-programmable for synchronous or asynchronous Initialize
- Increased drive capability, 24mA $I_{OL}$

## GENERAL DESCRIPTION

The Am27S85A/85 (4096-word by 4-bit) is Schottky TTL Programmable Read-only Memory (PROM) incorporating true D-type master-slave data registers on chip. This device is available with three-state outputs compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls. Designed to optimize system performance and provide the systems designer with on-chip SSR diagnostic capability, these devices also substantially reduce the cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

The on-chip edge-triggered register simplifies system timing since the PROM Clock (PCLK) may be derived directly from the system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

## BLOCK DIAGRAM




BD000400

IMOX and SSR are trademarks or Advanced Micro Devices, Inc.

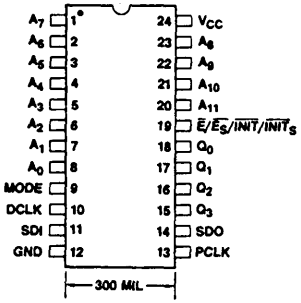
05273A

## PRODUCT SELECTOR GUIDE

| Access Time | 25ns | 30ns | | 35ns |
|---|---|---|---|---|
| Temperature Range | C | C | M | M |
| Part Number | 27S85A | 27S85 | 27S85A | 27S85 |

## CONNECTION DIAGRAM
Top View

**Am27S85**
**(4K x 4)**




CD000560

**Chip-Pak™**
**Am27S85**
**(4K x 4)**


Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am27S85 A P C B**

- B — Burn-in Option
  - C = No Burn-in
  - B = 160hr Burn-in
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – CERDIP
  - L – Chip-pak*
- A — Speed Selection
  - No Code = Standard
  - A = High Speed
- Am27S85 — Device Type
  - 1024 x Bipolar IMOX Registered PROM

| Valid Combinations | |
|---|---|
| Am27S75<br>Am27S75A | DC,DCB,<br>LC,LCB,<br>DM,DMB<br>LM,LMB |

*Chip-pak are rated at maximum case temperature only. This package will be available soon. Consult Factory.

This device is also available in die form to commercial and military specifications.
Pad layout and bonding diagram available upon request.

Chip-pak is a trademark of Advanced Micro Devices, Inc.

## MODE SELECT TABLE

Data transfers into the shadow register occur on the LOW-to-HIGH transition of DCLK. MODE and SDI determines what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. MODE selects whether the data source is the data input or the shadow register output.

Because of the independence of the clock inputs, data can be shifted in the shadow register via DCLK and loaded into the pipeline register from the data input via PCLK as long as no set up or hold times are violated.

| Inputs | | | | | Outputs | | | Operation |
|---|---|---|---|---|---|---|---|---|
| SDI | MODE | DCLK | PCLK | *<br>$\overline{INITs}$ | SDO | Shadow Register | Pipeline Register | |
| X | L | ↑ | – | X | $S_3$ | $S_n \leftarrow S_{n-1}$<br>$S_0 \uparrow SDI$ | NA | Serial Shift; $SDI \rightarrow S_0 \rightarrow S_1 \rightarrow S_2 \rightarrow S_3/SDO$ |
| X | L | – | ↑ | H | $S_3$ | NA | $Q_n \leftarrow$ ARRAY DATA | Normal Load Pipeline Register from PROM |
| X | L | – | ↑ | L | $S_3$ | NA | $Q_n \leftarrow$ INIT DATA | Synchronous Initialize Pipeline Register |
| L | H | ↑ | – | X | SDI | $S_n \leftarrow Q_n$ | NA | Load Shadow Register from OUTPUTS ($Q_0 - Q_3$) |
| X | H | – | ↑ | X | SDI | NA | $Q_n \leftarrow S_n$ | Load Pipeline Register from Shadow Register |
| H | H | ↑ | – | X | SDI | Hold | NA | No-Op |

**MODE SELECT TABLE DEFINITIONS**

**INPUTS**

H = HIGH
L = LOW
X = Don't Care
– = Steady State LOW or HIGH or HIGH-to-LOW transition
↑ = LOW-to-HIGH transition

SDO = Serial Data Output
$S_3 - S_0$ = Shadow Register Outputs (internal to devices)
$Q_3 - Q_0$ = Pipeline Register Outputs
NA = NOT applicable: Output is not a function of the specified input combinations

*Applies only if the architecture word has been programmed for Synchronous Initialize operation.

## DETAILED DESCRIPTION

The Am27S85A/85 contains a 4-bit parallel data register in the array-to-output path intended for normal registered data operations. In parallel with the output data registers is another 4-bit register with shifting capability, called a shadow register. As the name implies the shadow register is intended to be a copy (shadow) of the normal output data register. The shadow register can be used in a systematic way to control and observe the output data register in order to exercise any desired system function during a diagnostic test mode.

### DIAGNOSTIC PIN DESCRIPTION

In general, the implementation of Serial Shadow Register (SSR) diagnostics requires the addition of four extra device pins. These pins are

**Mode Control (MODE)**

Controls the source data for both sets of registers. MODE input is LOW in the normal mode of operation. The PROM array is the input source for the output data registers and the shadow register is in the shift mode (SDI→$S_0$→$S_1$→$S_2$→$S_3$/SDO). MODE input HIGH allows transfer of data for diagnostic testing. Shadow register data may be loaded into the output registers or output data bus information may be loaded into the shadow registers.

**Diagnostics Clock (DCLK)**

The diagnostics clock is used to load or shift the data into the shadow register. Transfer occurs on the LOW-to-HIGH transition of DCLK.

**Serial Data Input (SDI)**

This pin performs two functions depending on the state of the MODE input. If MODE is LOW, the SDI pin is a data transfer pin for serial data (SDI→$S_0$). If the MODE input is HIGH, the SDI pin is operating as a control pin where SDI asserted LOW permits output data to be loaded into the shadow register on the next LOW-to-HIGH transition of DCLK. SDI asserted HIGH represents a NO-OP function on this device.

**Serial Data Output (SDO)**

This pin operates as a transfer pin for serial data when the MODE input is LOW ($S_3$→SDO). When MODE is HIGH and SDI operates as a control pin, the SDO pin operates as a pass through of SDI control. SDO is an active totem-pole output.

### DESCRIPTION OF REGISTER CONTROL FUNCTIONS

In order to offer the system designer maximum flexibility these devices contain a programmable output enable pin and/or a programmable register initialize pin. The unprogrammed state of these pins is asynchronous operation. Should the system design require, either function may be changed to a synchronous mode of operation by programming an architecture word. The functions available are

Asynchronous $\overline{\text{Enable}}$ ($\overline{\text{E}}$)

Synchronous $\overline{\text{Enable}}$ ($\overline{\text{E}}_S$)

Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$)

Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}_S$)

The Asynchronous $\overline{\text{Enable}}$ ($\overline{\text{E}}$) allows direct control of the three-state output drivers.

The Synchronous $\overline{\text{Enable}}$ ($\overline{\text{E}}_S$) is useful where more than one Registered PROM is bussed together for word depth expansion. In this case, the enable becomes the most significant address bit and, as such, must be synchronized with the data.

The initialize function is a programmable word which can be loaded into the output data registers under single pin control. Since each bit is individually programmable, the initialize function can be used to load any combination of HIGHs or LOWs into the output data register. This feature is a superset of commonly used preset and clear functions.

Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$) can be used to generate any arbitrary microinstruction for system interrupt or Reset. This is useful during power-up or timeout sequences.

Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}_S$) is useful for "trap jumps" or interrupts where execution on the next LOW-to-HIGH Clock transition is required. During this operation MODE input must be held low.

The Am27S85A/85 contains a single programmable multifunctional input on Pin 19. The unprogrammed state of this pin operates as an Asynchronous $\overline{\text{Enable}}$ ($\overline{\text{E}}$) input. The architecture word permits programming the functionality to Synchronous $\overline{\text{Enable}}$ ($\overline{\text{E}}_S$), Asynchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}$), or Synchronous $\overline{\text{Initialize}}$ ($\overline{\text{INIT}}_S$).

## PROGRAMMING

The Am27S85A/85 Registered PROMs is manufactured with a conductive Platinum-Silicide link at each bit location. The output of this memory with the link in place is LOW. In addition to the programmable fusible link array this device contains two (2) architecture fuses to program the $\overline{\text{ENABLE}}$ and $\overline{\text{INITIALIZE}}$ input functionality. With these links intact both functions will operate asynchronously. The two-bit architecture word will program functionality according to Table 1.

**TABLE 1**

| Architecture Data Word (Hex) | Am27S85A/85 Input Function |
|---|---|
| | Pin 19 |
| 0 | Asynchronous $\overline{\text{ENABLE}}$ ($\overline{E}$) |
| 8 | Synchronous $\overline{\text{ENABLE}}$ ($\overline{E_S}$) |
| 4 | Asynchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}}$) |
| C | Synchronous $\overline{\text{INITIALIZE}}$ ($\overline{\text{INIT}_S}$) |

An additional four-bit word is available for programming the initialization word. The unprogrammed state of this word will initialize the data registers with all outputs LOW.

Programming each bit location (e.g. opening the fusible links) is accomplished by the following sequence: 1) Power is first applied to $V_{CC}$; 2) SDI input is raised to $V_{IHH}$ (15 volts). This biases internal conditioning and verification circuitry; 3) The appropriate address is selected; 4) a logic HIGH is applied to the MODE input followed by a LOW-to-HIGH transition of PCLK. This will load the output data registers with active HIGH data to protect the outputs during programming; 5) The output to be programmed is then raised to $V_{OP}$ (20 volts). Current from this 20 volt supply is then gated through the addressed fuse by raising the MODE input from a logic HIGH to $V_{IHH}$ (15 volts); 6) After 50$\mu$s, the 20 volt supply is removed; 7) The MODE input is taken from $V_{IHH}$ to a logic LOW. Each data verification must be preceded by a positive going (LOW-to-HIGH) transition of PCLK. This will load the array data into the output data registers. The outputs are then sensed to determine if the link has opened. Most links will open within 50$\mu$s.

Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5ms. If a link has not opened after a total elapsed programming time of 400ms, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to a HIGH level.

When Pin 19 is raised to a logic HIGH level, the programming circuitry for the array is selected and the programming circuitry for the architecture and initialize words is deselected. When Pin 19 is asserted LOW the array programming circuitry is deselected and the programming circuitry for the architecture and initialize words is selected. The architecture and initialize words are then addressed via the $A_0$ input. $A_0$ input LOW addresses the architecture word while $A_0$ input HIGH addresses the initialize word.

An easy implementation would be to invert the next higher address from a PROM programmer and apply this signal to Pin 19. The array, architecture and initialize words would then be programmed according to Table 2.

**TABLE 2**

| Device | Pin 19 | Array Programming Address Field (Hex) | Architecture Word Address (Hex) | Initialize Word Address (Hex) |
|---|---|---|---|---|
| Am27S85A/85 | $\overline{A_{12}}$ | 000 thru 0FFF | 1000 | 1001 |

Special verification circuitry within the device will permit the architecture word to be presented at the outputs for programming verification.

The unused DCLK pin should be terminated either HIGH or LOW during programming in order to avoid the possibility of oscillation.

High-yield fusing of the Platinum-Silicide fuses requires that a substantial current be delivered to the decoded and selected fuse. The fusing current path has been designed to provide a large fusing current safety margin. This, however, generates large current transients at the time MODE input goes to $V_{IHH}$ and a proportional current decrease at the time the fuse opens. The magnitude of this current change can be between 50 and 150mA with rise or fall times of 2 to 10ns. Some care must be taken to avoid excessive line inductance in the output line to maximize fusing yields.

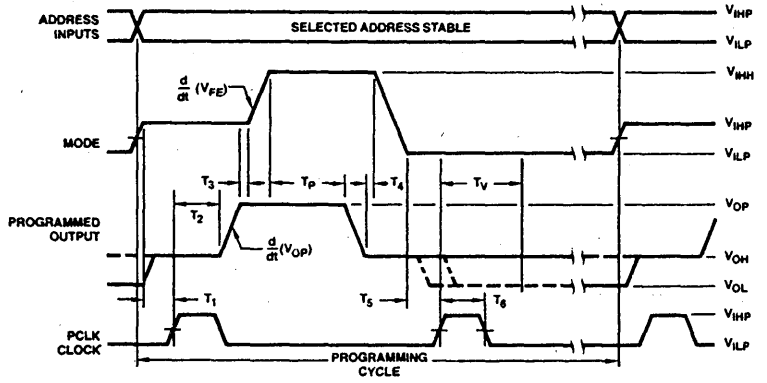
The PROMs may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device for more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including $V_{CC}$ should be removed for a period of 5 seconds after which programming may be resumed.

When all programming has been completed the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an undesired link has been fused. Should this occur, immediately check the programming equipment to make sure all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing. Typical programming yields exceed 98%. Fusing extra bits is generally related to programming equipment problems.

## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IHH}$ | Control Pin Extra High Level | SDI @ 10 – 40mA | 14.5 | 15 | 15.5 | Volts |
| | | MODE @ 10 – 40mA | 14.5 | 15 | 15.5 | |
| $V_{OP}$ | Program Voltage @ 15 – 200mA | | 19.5 | 20 | 20.5 | Volts |
| $V_{IHP}$ | Input High Level During Programming and Verify | | 2.4 | 5 | 5.5 | Volts |
| $V_{ILP}$ | Input Low Level During Programming and Verify | | 0.0 | 0.3 | 0.5 | Volts |
| $V_{CCP}$ | $V_{CC}$ During Programming @ $I_{CC}$ = 50 – 200mA | | 5 | 5.2 | 5.5 | Volts |
| $dV_{OP}/dt$ | Rate of Output Voltage Change | | 20 | | 250 | V/μsec |
| $dV_{FE}/dt$ | Rate of Fusing Enable Voltage Change (MODE Rising Edge) | | 50 | | 1000 | V/μsec |
| $t_P$ | Fusing Time First Attempt | | 40 | 50 | 100 | μsec |
| | Subsequent Attempts | | 4 | 5 | 10 | msec |
| $t_1 - t_6$ | Delays Between Various Level Changes | | 100 | 200 | 1000 | ns |
| $t_V$ | Period During which Output is Sensed for $V_{Blown}$ Level | | | | 500 | ns |
| $V_{ONP}$ | Pull-Up Voltage On Outputs Not Being Programmed | | $V_{CCP}$ – 0.3 | $V_{CCP}$ | $V_{CCP}$ + 0.3 | Volts |
| R | Pull-Up Resistor On Outputs Not Being Programmed | | 0.2 | 2 | 5.1 | kΩ |

## PROGRAMMING WAVEFORMS

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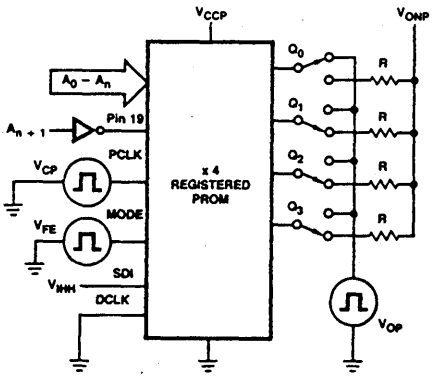
### SIMPLIFIED PROGRAMMING DIAGRAM

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### PROGRAMMING EQUIPMENT INFORMATION

| | |
|---|---|
| Source and Location | Data I/O<br>10525 Willows Rd. N.E.<br>Redmond, WA 98052 |
| Programmer Mode(s) | Systems 17, 19, 29, and 100 |
| AMD Personality Module | UNIPAK Rev. 005*<br>UNIPAK 2 Rev. V05* |
| Socket Adapter | 351A-073 |

*Rev shown is minimum approved revision.

# APPLYING SERIAL SHADOW REGISTER (SSR) DIAGNOSTICS IN BIPOLAR MICROCOMPUTERS

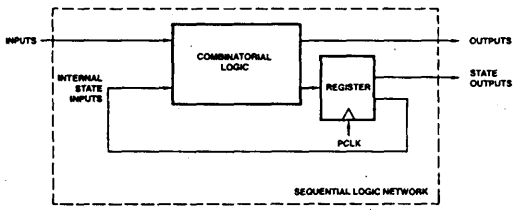
## DIAGNOSTICS

A diagnostics capability provides the necessary functionality as well as a systematic method for detecting and pin-pointing hardware related failures in a system. This capability must be able to both *observe* intermediate test points and *control* intermediate signals – address, data, control, and status – to exercise all portions of the system under test. These two capabilities, observability and controllability, provide the ability to establish a desired set of input conditions and state register values, sample the necessary outputs, and determine whether the system is functioning correctly.

## TESTING COMBINATIONAL AND SEQUENTIAL NETWORKS

The problem of testing a combinational logic network is well understood. Sets of input signals (test vectors) are applied to the network and the network outputs are compared to the set of computed outputs (result vectors). In some cases sets of test vectors and result vectors can be generated in a computer-aided environment, minimizing engineering effort. Additionally, fault coverage analysis can be automated to provide a measure of how efficient a set of test vectors is at pin-pointing hardware failures. For example, a popular measure of fault coverage computes the percentage of stuck-at-ones (nodes with outputs always HIGH) and stuck-at-zeros (nodes with outputs always LOW) a given set of test vectors will discover.

**Figure 1**

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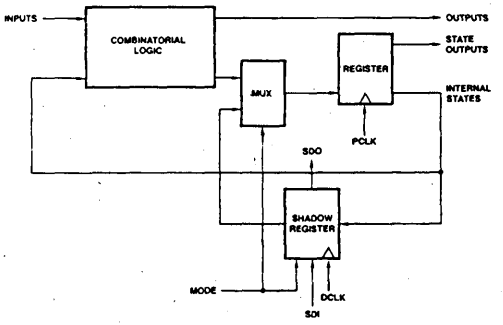
A sequential network (Figure 1) is much more difficult to test systematically. The outputs of a sequential network depend not only on the present inputs but also on the internal state of the network. Initializing the internal state register to the value necessary to test a given set of inputs is difficult at best, and not easily automated. Additionally, observing the internal state of a sequential network can be very difficult and time consuming if the state information is not directly available. For example, consider the problem of determining the value of an internal 16-bit counter if only a carry-out signal is available. The counter must be clocked until it reaches the carry-out state and the starting value computed. Up to 65,535 clock cycles may be necessary! An easier method must exist. Serial Shadow Register diagnostics provides this method.

## SERIAL SHADOW REGISTER DIAGNOSTICS

Serial Shadow Register diagnostics provides sufficient observability and controllability to turn any sequential network into a combinational network. This is accomplished by providing the means to both initialize (control) and sample (observe) the state elements of a sequential network. Figure 2 shows the method by which Serial Shadow Register diagnostics accomplishes these two functions.

**Figure 2**

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Serial Shadow Register diagnostics utilizes an extra multiplexer on the input of each state register and a duplicate or shadow of each state flip/flop in an additional register. The shadow register can be loaded serially via the serial data input (thus the name Serial Shadow Register diagnostics) for controllability. Once the desired state information is loaded into the serial register it can be transferred into the internal state register by selecting the multiplexer and clocking the state register with PLCK. This allows any internal state to be set to a desired state in a simple, quick, and systematic manner.

Internal state information can be sampled by loading the serial register from the state register outputs. This state information can then be shifted out via the serial data output to provide observability. Notice that the serial data inputs and outputs can be cascaded to make long chains of state information available on a minimum number of connections.

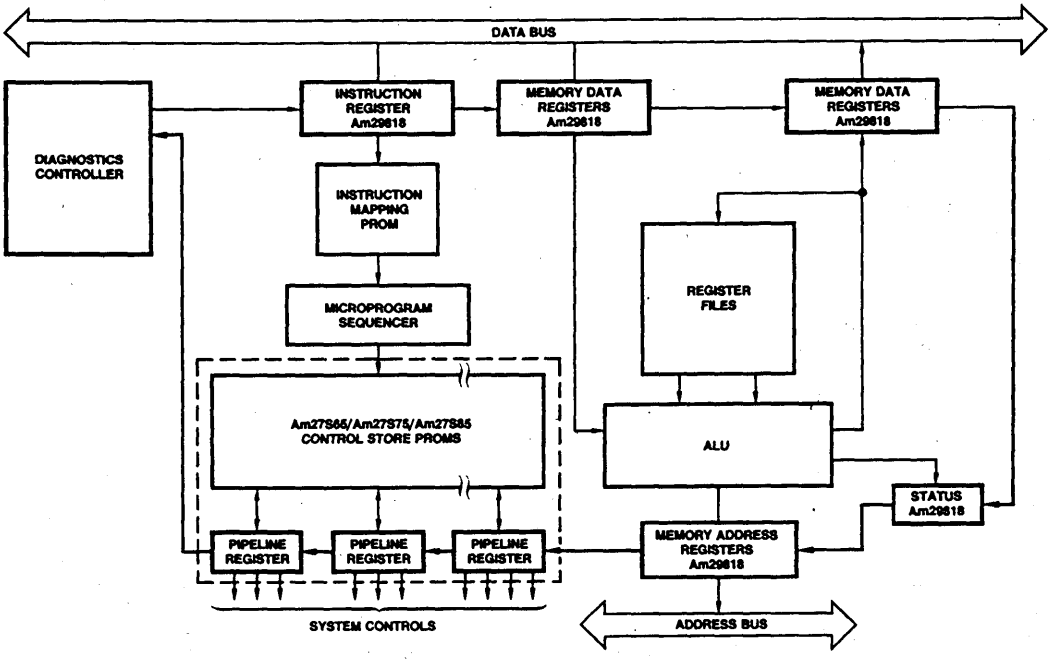
In effect, Serial Shadow Register diagnostics breaks the normal feedback path of the sequential network and establishes a logical path with which inputs can be defined and outputs sampled. This means that those techniques which have been developed to test combinational networks can be applied to any sequential network in which Serial Shadow Register diagnostics is utilized.

When normal pipeline registers are replaced by SSR diagnostics pipeline registers, system debug and diagnostics are easily implemented. State information which was inaccessible is now both observable and controllable. Figure 3 shows a typical computer system using the Am29818's and Am27S85's.

Serial paths have been added to all the important state registers (macro instruction, data, status, address, and micro instruction registers). This extra path will make it easier to diagnose system failures by breaking the feed-back paths and turning sequential state machines into combinatorial logic blocks. For example, the status outputs of the ALU may be checked by loading the micro instruction register with the necessary micro instruction. The desired ALU function is then executed and the status outputs captured in the status register. The status bits can then be serially shifted out and checked for validity.

A single diagnostic loop was shown in Figure 3 for simplicity, but several loops can be employed in more complicated systems to reduce scan time. Additionally, the Am29818s can be used to sample intermediate test points not associated with normal state information. These additional test points can further ease diagnostics, testability and debug.

## Figure 3. Typical System Configuration

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Typical computer system with Am27S85 registered PROMS implementing SSR diagnostics

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

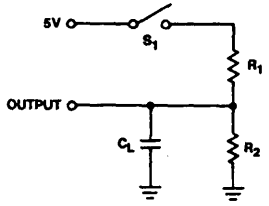
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | See Note 2 | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | See Note 2 | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ ($Q_0$ − $Q_3$) = −2mA | 2.4 | 3.7 | | Volts |
| | | | $I_{OH}$ (SDO) = −0.5mA | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | COM'L $I_{OL}$ ($Q_0$ − $Q_3$) = 24mA | | 0.35 | 0.5 | Volts |
| | | | MIL $I_{OL}$ ($Q_0$ − $Q_3$) = 18mA | | | | |
| | | | $I_{OL}$ (SDO) = 4mA | | | | |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max, $V_{IN}$ = 0.4V | | | −40 | −250 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max | $V_{IN}$ = 2.7V | | | 25 | μA |
| | | | $V_{IN}$ = 5.5V | | | 40 | |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max, $V_{OUT}$ = 0V (Note 3) | $Q_0$ − $Q_3$ | −20 | −40 | −90 | mA |
| | | | SDO | −10 | | −85 | |
| $I_{CEX}$ | Output Leakage Current (Three-State) ($Q_0$ − $Q_3$) | $V_{CC}$ = Max, $\overline{E}/\overline{E_S}$ = 2.4V (Note 4) | $V_{OUT}$ = $V_{CC}$ | | | 50 | μA |
| | | | $V_{OUT}$ = 0.4V | | | −0.15 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max, All Inputs = 2.4V | | | 135 | 185 | mA |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | 5 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | 12 | | pF |

Notes:

1. Typical values are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment (see Notes on Testing).
3. Only one output should be shorted at a time. Duration of the short circuit should not be more than one second.
4. For devices using the synchronous enable, the device must be clocked after applying these voltages to perform this measurement.
5. These parameters are not 100% tested, but are periodically sampled.

## SWITCHING TEST CIRCUIT

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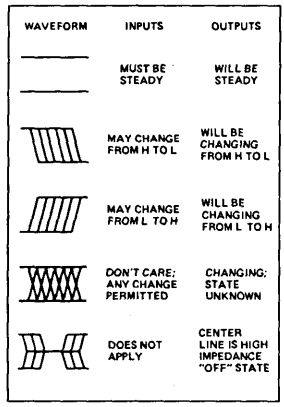
## KEY TO SWITCHING WAVEFORMS




KS000010

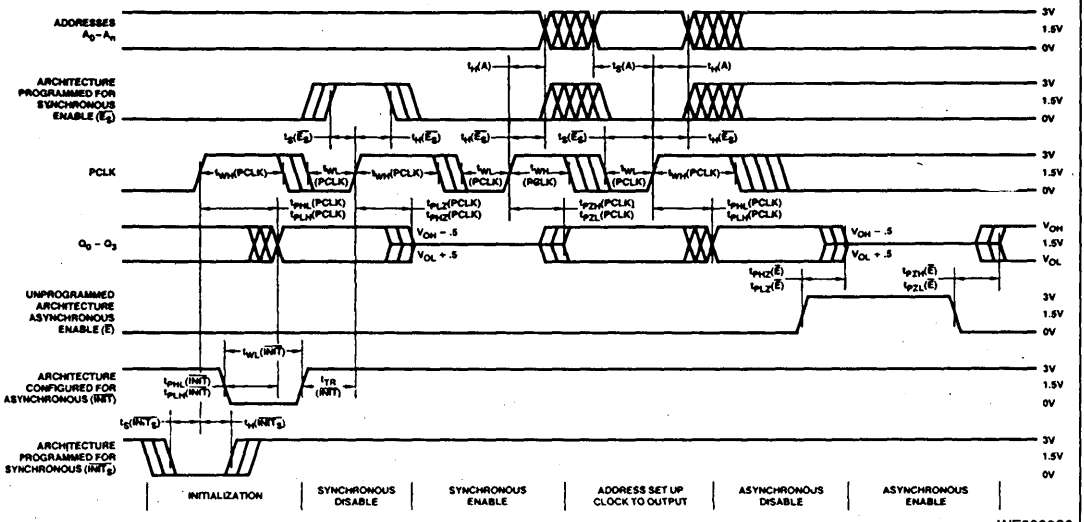
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | "A" Versions COM'L Min | "A" Versions COM'L Max | "A" Versions MIL Min | "A" Versions MIL Max | Standard Versions COM'L Min | Standard Versions COM'L Max | Standard Versions MIL Min | Standard Versions MIL Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_S$(A) | Address to PCLK (HIGH) Setup Time | 25 | | 30 | | 30 | | 35 | | ns |
| 2 | $t_H$(A) | Address to PCLK (HIGH) Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| 3 | $t_{PHL}$(PCLK) | Delay from PCLK (HIGH) to Output (HIGH or LOW) | 4 | 12 | 4 | 17 | 4 | 15 | 4 | 20 | ns |
| 4 | $t_{PLH}$(PCLK) | | | | | | | | | | |
| 5 | $t_{WL}$(PCLK) | Clock Pulse Width for Output Data Registers (LOW or HIGH) | 15 | | 20 | | 20 | | 20 | | ns |
| 6 | $t_{WH}$(PCLK) | | | | | | | | | | |
| 7 | $t_{PZL}(\overline{E})$ | Asynchronous Enable - Delay from $\overline{E}$ (LOW) to Active Output (HIGH or LOW) (See Note 4) | | 17 | | 22 | | 20 | | 25 | ns |
| 8 | $t_{PZH}(\overline{E})$ | | | | | | | | | | |
| 9 | $t_{PLZ}(\overline{E})$ | Asynchronous Disable - Delay from $\overline{E}$ (HIGH) to Inactive Output (OFF or HIGH Impedance) (See Notes 3 and 4) | | 17 | | 22 | | 20 | | 25 | ns |
| 10 | $t_{PHZ}(\overline{E})$ | | | | | | | | | | |
| 11 | $t_S(\overline{ES})$ | $\overline{ES}$ to PCLK (HIGH) Set-Up Time (See Note 5) | 12 | | 12 | | 15 | | 15 | | ns |
| 12 | $t_H(\overline{ES})$ | $\overline{ES}$ to PCLK (HIGH) Hold Time (See Note 5) | 0 | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{PZL}$(PCLK) | Synchronous Enable - Delay from PCLK (HIGH) to Active Output (HIGH or LOW) (See Note 5) | | 17 | | 22 | | 20 | | 25 | ns |
| 14 | $t_{PZH}$(PCLK) | | | | | | | | | | |
| 15 | $t_{PLZ}$(PCLK) | Synchronous Disable - Delay from PCLK (HIGH) to Inactive Output (OFF or HIGH Impedance) (See Notes 3 and 5) | | 17 | | 22 | | 20 | | 25 | ns |
| 16 | $t_{PHZ}$(PCLK) | | | | | | | | | | |
| 17 | $t_{PHL}(\overline{INIT})$ | Delay from Asynchronous $\overline{INIT}$ (LOW) to Outputs (LOW or HIGH) (See Note 6) | | 25 | | 30 | | 30 | | 35 | ns |
| 18 | $t_{PLH}(\overline{INIT})$ | | | | | | | | | | |
| 19 | $t_R(\overline{INIT})$ | Asynchronous $\overline{INIT}$ Recovery ($\overline{INIT}$ 5) to PCLK (HIGH) (See Note 6) | 20 | | 25 | | 25 | | 30 | | ns |
| 20 | $t_{WL}(\overline{INIT})$ | Asynchronous $\overline{INIT}$ Pulse Width (LOW) (See Note 6) | 20 | | 20 | | 25 | | 25 | | ns |
| 21 | $t_S(\overline{INIT})$ | Synchronous $\overline{INIT}$ (LOW) to PCLK (HIGH) Set-Up Time (See Note 7) | 15 | | 20 | | 20 | | 25 | | ns |
| 22 | $t_H(\overline{INIT})$ | Synchronous $\overline{INIT}$ (LOW) to PCLK (HIGH) Hold Time (See Note 7) | 5 | | 5 | | 5 | | 5 | | ns |

See also AC test loads and noises 2, 3, 8, 9, 10.

## SWITCHING WAVEFORMS

for Typical Registered PROM applications
(See Notes on Testing)

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## DIAGNOSTIC MODE SWITCHING CHARACTERISTICS

**OVER OPERATING RANGE**(Unless otherwise noted)

| No. | Symbol | Description | COM'L Min | COM'L Max | MIL Min | MIL Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | $t_S$(SDI) | Serial Data In to DCLK (HIGH) Set-Up Time | 25 | | 30 | | ns |
| 2 | $t_H$(SDI) | Serial Data In to DCLK (HIGH) Hold Time | 0 | | 0 | | |
| 3 | $t_S$(MODE) | MODE to PCLK (HIGH) or DLCK(HIGH) Set-Up Time | 25 | | 30 | | |
| 4 | $t_H$(MODE) | MODE to PCLK (HIGH) or DCLK (HIGH) Hold Time | 0 | | 0 | | |
| 5 | $t_S$(Q) | Output to DCLK (HIGH) Setup Time | 25 | | 30 | | |
| 6 | $t_H$(Q) | Output to DCLK (HIGH) Hold Time | 10 | | 15 | | |
| 7 | $t_{PHL}$(DCLK) | Delay from DCLK (HIGH) to Serial Data Output (HIGH or LOW) | | 30 | | 40 | |
| 8 | $t_{PLH}$(DCLK) | | | | | | |
| 9 | $t_{PHL}$(SDI) | Delay from Serial Data Input (LOW or HIGH) to Serial Data Output (LOW or HIGH)-MODE Input HIGH | | 25 | | 30 | |
| 10 | $t_{PLH}$(SDI) | | | | | | |
| 11 | $t_{WL}$(DCLK) | Clock Pulse Width for Diagnostic Register(LOW or HIGH) | 25 | | 25 | | |
| 12 | $t_{WH}$(DCLK) | | | | | | |

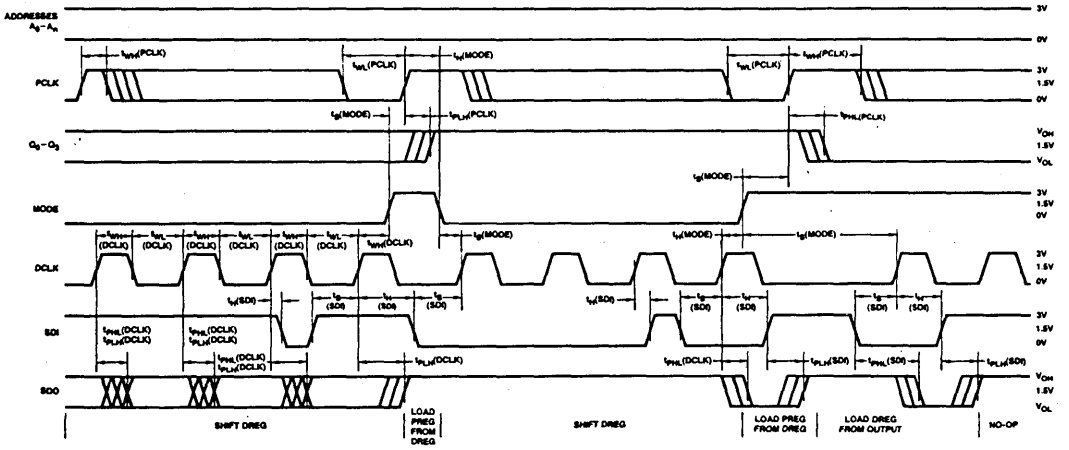
Notes:

1. Typical values are taken at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.
3. $t_{PHZ}$ and $t_{PLZ}$ are measured to the $V_{OH}$ – 0.5V and $V_{OL}$ + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
4. Applies only if the architecture is configured for Asynchronous $\overline{\text{Enable}}$.
5. Applies only if the architecture word has been programmed for a Synchronous $\overline{\text{Enable}}$ input.
6. Applies only if the architecture is configured for Asynchronous $\overline{\text{Initialize}}$.
7. Applies only if the architecture word has been programmed for a Synchronous $\overline{\text{Initialize}}$ input.
8. Component values for AC TEST LOAD are: $R_1$ = 300, $R_2$ = 600, and $C_L$ = 50pF for $Q_0$ – $Q_3$ outputs, $R_1$ = 1100, $R_2$ = 2400, and $C_L$ = 15pF for SDO output.
9. All device test loads should be located within 2" of device outputs.
10. $S_1$ is open for $t_{PHZ}$ and $t_{PZH}$ tests. $S_1$ is closed for all other AC tests.

## SWITCHING WAVEFORMS

for Diagnostics applications

(See Notes on Testing)

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## NOTES ON TESTING

Incoming test procedures on these devices should be carefully planned, taking into account the high performance and output drive capabilities of the parts. The following notes may be useful.

1. Ensure that adequate decoupling capacitance is employed across the device $V_{CC}$ and ground terminals. Multiple capacitors are recommended, including a 0.1μFarad or larger capacitor and a 0.01μFarad or smaller capacitor placed as close to the device terminals as possible. Inadequate decoupling may result in large variations of power supply voltage, creating erroneous function or transient performance failures.
2. Do not leave any inputs disconnected (floating) during any tests.
3. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S181/281 Family

1024 x 8 Bit Generic Series Bipolar IMOX™ PROM

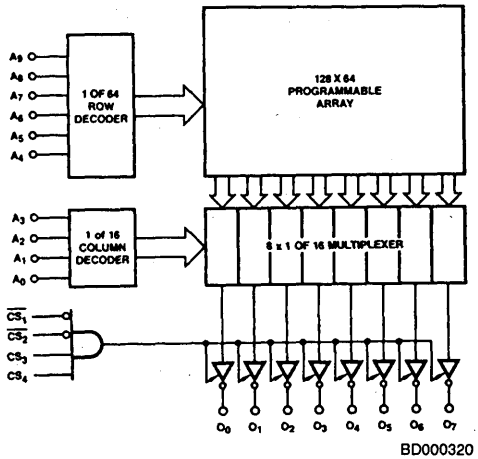
## DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Rapid recovery from power-down state provides minimum delay

## GENERAL DESCRIPTION

These 8K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 1024 x 8 configuration, they are available in both the standard 600-mil package and the space-saving THIN-DIP, 300-mil package versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_9$ and holding $\overline{CS}_1$ and $\overline{CS}_2$ LOW and $CS_3$ and $CS_4$ HIGH. All other input combinations on $\overline{CS}_1$, $\overline{CS}_2$, $CS_3$ and $CS_4$ place $O_0 - O_7$ into the OFF or high impedance state and reduce $I_{CC}$ by more than 50%.

## BLOCK DIAGRAM




BD000320

## PRODUCT SELECTOR GUIDE

| Access Time | 35ns | 50ns | | 60ns | 65ns | | 75ns | 80ns |
|---|---|---|---|---|---|---|---|---|
| Temperature Range | C | C | M | C | C | M | M | M |
| Open Collector | 27S180A<br>27S280A | | 27S180A<br>27S280A | 27S180<br>27S280 | | | | 27S180<br>27S181 |
| Three-State | 27S181A<br>27S281A | 27PS181A<br>27PS281A | 27S181A<br>27S281A | 27S181<br>27S281 | 27PS181<br>27PS281 | 27PS181A<br>27PS281A | 27PS181<br>27PS281 | 27S280<br>27S281 |

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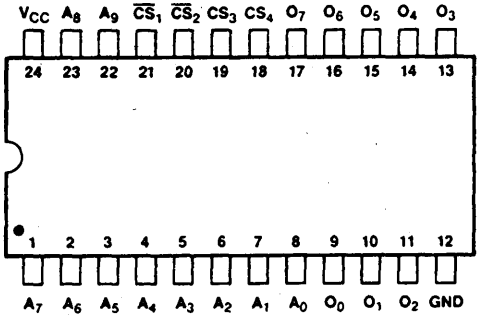
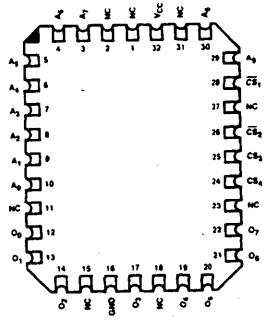
## CONNECTION DIAGRAM
### Top View

**DIP**




CD000790

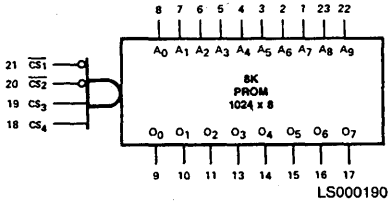
**Chip-Pak™ L-32-2**



CD000820

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000190

$V_{CC}$ = Pin 24
GND = Pin 12

## ORDERING INFORMATION

**Am27S12 A P C B**

- B — Burn-in Option
  - B suffix indicates 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 24-pin ceramic DIP
  - F – 24-pin flatpak
  - L – 32-pin leadless chip carrier
  - P – 24-pin plastic DIP
  - Note: Series 700 divices are packaged in standard 600 mil DIPs; 200 devices are packaged in space saving 300 mil DIPs.
- A — Speed Select
  - See Product Selector Guide
- Am27S12 — Device Type
  - Output Configuration – See Product Selector Guide
  - 27S – Standard Devices
  - 27PS – Power Switched Devices

| Valid Combinations | |
|---|---|
| Am27S180<br>Am27S180A<br>Am27S181<br>Am27S181A<br>Am27PS181 | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |
| Am27S280<br>Am27S280A<br>Am27S281<br>Am27S281A<br>Am27PS281 | PC, PCB,<br>DC, DCB,<br>DM, DMB |

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## NOTES ON POWER SWITCHING

The Am27PS181A/181 and Am27PS281A/281 are power switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, $I_{CC}$ is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS181A/181 and Am27PS281A/281 are selected, a current surge is placed on the $V_{CC}$ supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 1.)
2. Address access time ($t_{AA}$) can be optimized if a chip enable setup time ($t_{EAS}$) of greater than 25ns is observed. Negative setup times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 4) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 4) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | μA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 2) | COM'L | −20 | −40 | −90 | mA |
| | | | MIL | −15 | −40 | −90 | |
| $I_{CC}$ | Power Supply Current | All Inputs = GND | | | 115 | 185 | mA |
| $I_{CCD}$ | Power Down Supply Current | $\overline{CS}_1$ = 2.7V; All other inputs = GND | | | 50 | 80 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$V\overline{CS}_1$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | μA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 3) | | | 4.0 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 3) | | | 8.0 | | |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.



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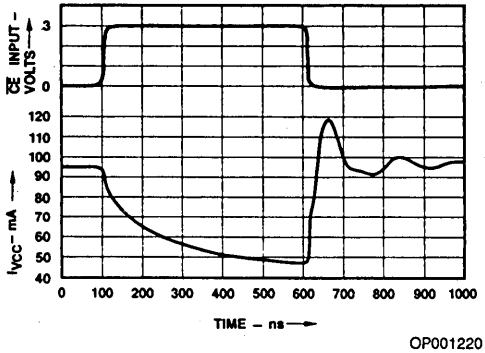
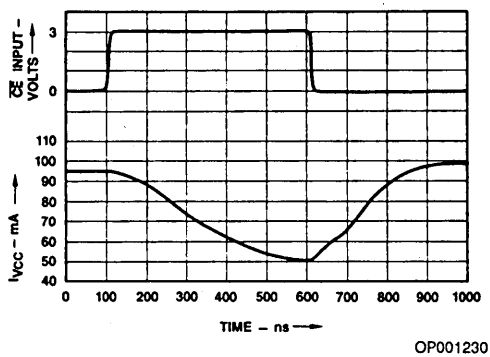
## DC OPERATING CHARACTERISTICS

Typical $I_{VCC}$ Current Surge without 0.1μF
($I_{VCC}$ is Current Supplied by $V_{CC}$ Power Supply)



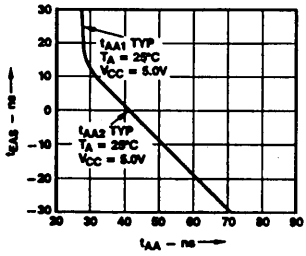

OP001220

Typical $I_{VCC}$ Current Surge with 0.1μF
($I_{VCC}$ is Current Supplied by $V_{CC}$ Power Supply)



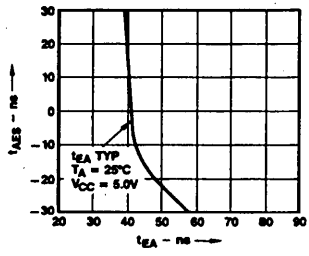

OP001230

Figure 1. $I_{CC}$ Current




OP001110

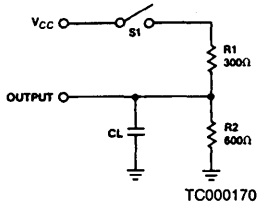
Figure 2A. $t_{AA}$ versus $t_{EAS}$




OP001120

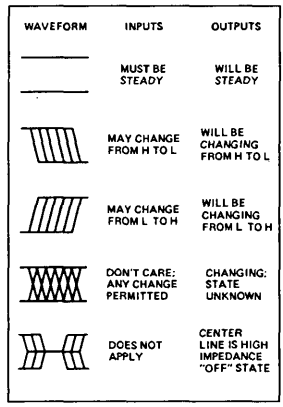
Figure 2B. $t_{EA}$ versus $t_{AES}$

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORMS




KS000010

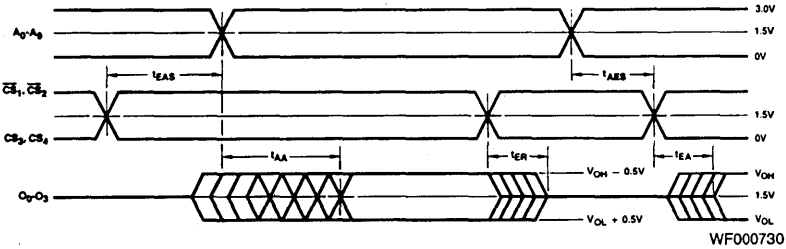
## SWITCHING CHARACTERISTICS *over operating range unless otherwise specified*

| No. | Symbol | Description | | 27S Commercial Min | 27S Commercial Max | 27S Military Min | 27S Military Max | 27PS Commercial Min | 27PS Commercial Max | 27PS Military Min | 27PS Military Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 60 | | 80 | | 65 | | 75 | ns |
| | | | A | | 35 | | 50 | | 50 | | 65 | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 40 | | 50 | | 80 | | 90 | |
| | | | A | | 25 | | 30 | | 65 | | 75 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 40 | | 50 | | 35 | | 45 | |
| | | | A | | 25 | | 30 | | 25 | | 30 | |
| 4 | $t_{AAPS}$ | Power Switched Address Access Time (27PS devices only) | STD | | | | | | 80 | | 90 | |
| | | | A | | | | | | 65 | | 75 | |

Notes:

1. $t_{AA}$ is tested with switch $S_1$ closed and $C_L$ = 30pF.
2. For open collector outputs, $t_{EA}$ and $t_{ER}$ are tested with $S_1$ closed to the 1.5V output level. $C_L$ = 30pF.
3. For three-state outputs, $t_{EA}$ is tested with $C_L$ = 30pF to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L$ = 5pF. HIGH to high impedance tests are made to an output voltage to with $S_1$ open to $V_{OH}$–0.5V with $S_1$ open; LOW to high impedance tests are made to the $V_{OL}$+0.5V level with $S_1$ closed.

## SWITCHING WAVEFORMS




WF000730

Note: Level on output while chip is disabled is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S184/185 Series

2048 x 4 Bit Generic Series Bipolar IMOX™ PROM

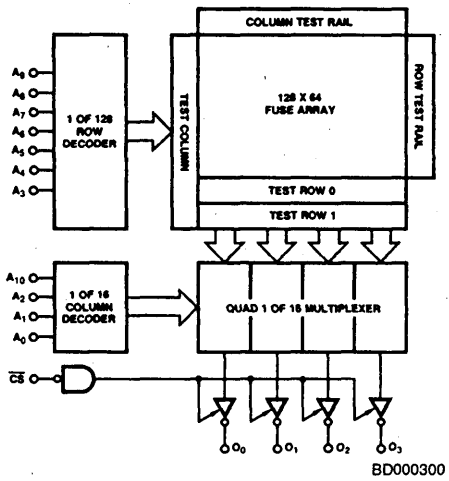
## DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (35ns max) — Fast access time Standard version (50ns max) — allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

## GENERAL DESCRIPTION

The Am27S184/5 series is comprised of high speed electrically programmable Schottky read only memories. Organized in 2048 x 4 configuration, they are available in both open collector and three-state output versions. After programming, stored information is read on outputs $O_0 - O_3$ by applying unique binary addresses to $A_0 - A_{10}$ and holding the chip select input, $\overline{CS}$ LOW. If the chip select input goes to a logic HIGH, $O_0 - O_3$ go to the OFF or high impedance state.

## BLOCK DIAGRAM




BD000300

## PRODUCT SELECTOR GUIDE

| Access Time | 35ns | 45ns | 50ns | 55ns | 60ns | 65ns |
|---|---|---|---|---|---|---|
| Temperature Range | C | M | C | M | C | M |
| Open Collector | 27S184A | 27S184A | 27S184 | 27S184 | 27LS184 | 27LS184 |
| Three-State | 27S185A | 27S185A | 27S185<br>27PS185 | 27S185<br>27PS185 | 27LS185 | 27LS185 |

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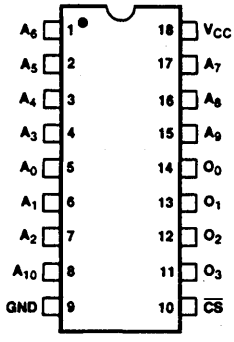
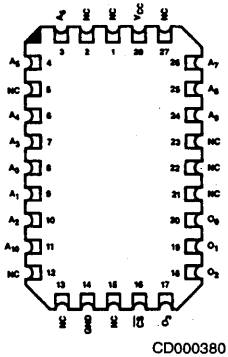
## CONNECTION DIAGRAM
### Top View

**DIP**




CD000370

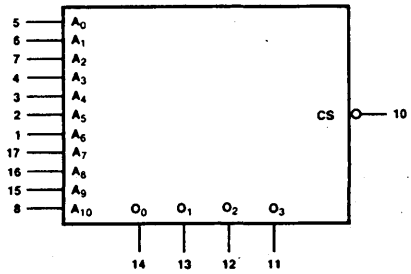
**Chip-Pak™ L-28-2**



CD000380

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000010

$V_{CC}$ = Pin 18
GND = Pin 9

## ORDERING INFORMATION

**Am27S184 A P C B**

- B — Burn-in Option
  - B suffix indicates 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 18-pin ceramic DIP
  - F – 18-pin flatpack
  - L – 28-pin leadless chip carrier
  - P – 18-pin plastic DIP
- A — Speed Select
  - See Product Selector Guide
- Am27S184 — Device Type
  - Output Configuration – See Product Selector Guide
  - 27S – Standard Devices
  - 27PS – Power Switched Devices
  - 27LS – Low Power Devices

| Valid Combinations | |
|---|---|
| Am27S184 | PC, PCB |
| Am27S184A | DC, DCB |
| Am27S185 | LC, LCB, |
| Am27S185A | DM, DMB, |
| Am27PS185 | FM, FMB, |
| Am27LS184 | LM, LMB |
| Am27LS184A | |
| Am27LS185 | |
| Am27LS185A | |

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## POWER SWITCHING

The Am27PS185 is a power switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, $I_{CC}$ is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS185 is selected by a low level on $\overline{CS}$, a current surge is placed on the $V_{CC}$ supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 18 to pin 9 at each device. (See Figure 1.)

2. Address access time ($t_{AA}$) can be optimized if a chip enable set-up time ($t_{EAS}$) of greater than 25ns is observed. Negative set-up times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics see Figures 2A and 2B.)

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

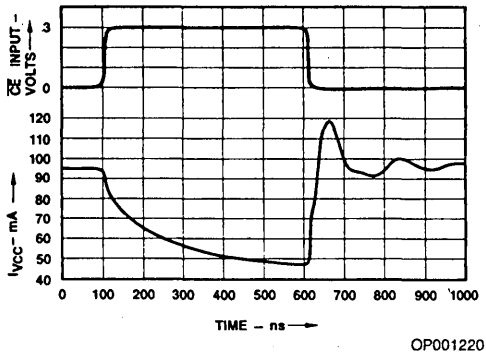
| Symbol | Parameters | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.020 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | μA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX<br>$V_{OUT}$ = 0.0V (Note 4) | STD, LS devices | −20 | −45 | −90 | mA |
| | | | PS devices | −15 | −40 | −90 | |
| $I_{CC}$ | Power Supply Current | All inputs = GND<br>$V_{CC}$ = MAX | STD, PS devices | | 105 | 150 | mA |
| | | | LS devices | | 80 | 125 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$\overline{CS}$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | μA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 5) | | | 5.0 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 5) | | | 8.0 | | |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. These parameters are not 100% tested, but are periodically sampled.

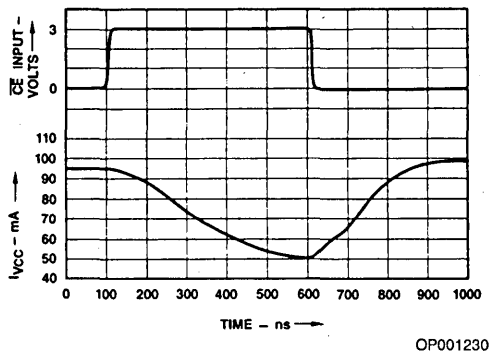
## DC OPERATING CHARACTERISTICS

Typical $I_{VCC}$ Current Surge without 0.1μf
($I_{VCC}$ is Current Supplied by $V_{CC}$ Power Supply)



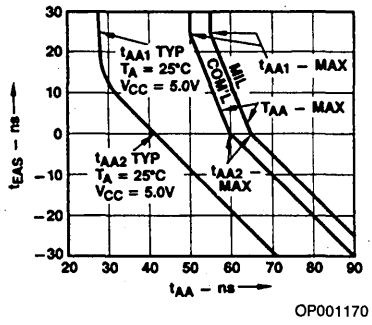

OP001220

Typical $I_{VCC}$ Current Surge with 0.1μf
($I_{VCC}$ is Current Supplied by $V_{CC}$ Power Supply)



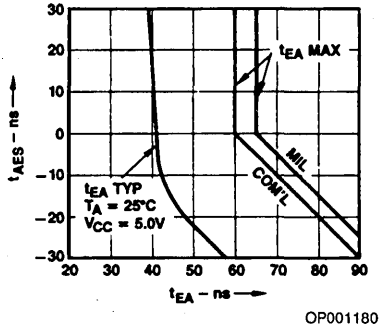

OP001230

Figure 1. $I_{CC}$ Current




OP001170

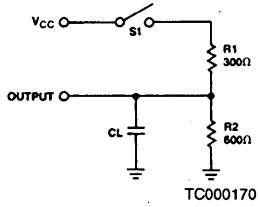
Figure 2A. $T_{AA}$ versus $T_{EAS}$




OP001180

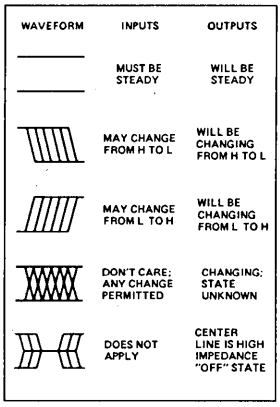
Figure 2B. $T_{EA}$ versus $T_{AES}$

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORMS

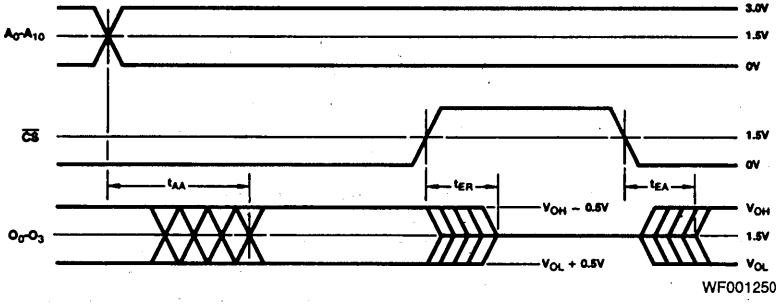



KS000010

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | C devices Min | C devices Typ | C devices Max | M devices Min | M devices Typ | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 30 | 50 | | 30 | 55 | ns |
| | | | A | | 28 | 35 | | 28 | 45 | |
| | | | PS | | 28 | 50 | | 28 | 55 | |
| | | | LS | | 40 | 60 | | 40 | 65 | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 10 | 25 | | 10 | 30 | |
| | | | A | | 10 | 25 | | 10 | 30 | |
| | | | PS | | 41 | 60 | | 41 | 65 | |
| | | | LS | | 10 | 25 | | 10 | 30 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 10 | 25 | | 10 | 30 | |
| | | | A | | 10 | 25 | | 10 | 30 | |
| | | | PS | | 41 | 60 | | 41 | 65 | |
| | | | LS | | 10 | 25 | | 10 | 30 | |
| 4 | $t_{AAPS}$ | Power Switched Address Access Time (27 PS devices only) | | | 10 | 25 | | 10 | 30 | |

## SWITCHING WAVEFORMS




WF001250

Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

# Am27S191/291 Family

2048 x 8 Bit Generic Series Bipolar IMOX™ PROM

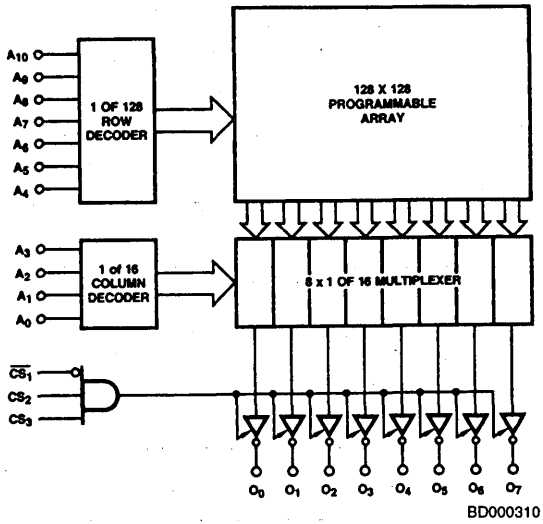
## DISTINCTIVE CHARACTERISTICS

- Fast access time allows high system speed
- 50% power savings on deselected parts — enhances reliability through total system heat reduction (27PS devices)
- Plug in replacement for industry standard product — no board changes required
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Rapid recovery from power-down state provides minimum delay (27PS devices)

## GENERAL DESCRIPTION

These 16K PROMs are high speed electrically programmable Schottky read only memories. Organized in the industry standard 2048 x 8 configuration, they are available in both the standard 600-mil package and the space-saving THIN-DIP, 300-mil package versions. After programming, stored information is read on outputs $O_0 - O_7$ by applying unique binary addresses to $A_0 - A_{10}$ and holding $\overline{CS}_1$ LOW and $CS_2$ and $CS_3$ HIGH. All other input combinations on $\overline{CS}_1$, $CS_2$, and $CS_3$ place $O_0 - O_7$ into the OFF or high impedance state and reduce $I_{CC}$ by more than 50%.

## BLOCK DIAGRAM




## PRODUCT SELECTOR GUIDE

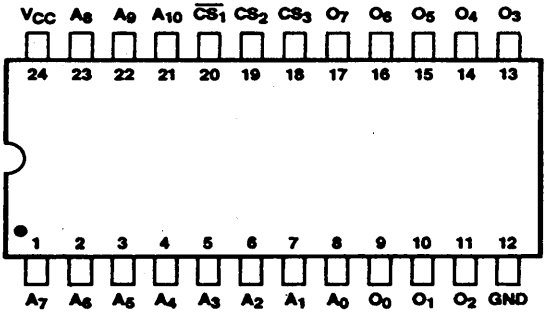
| Access Time | 35ns | 50ns | | 65ns | | 75ns |
|---|---|---|---|---|---|---|
| Temperature Range | C | C | M | C | M | M |
| Open Collector | 27S190A<br>27S290A | 27S190<br>27S290 | 27S190A<br>27S290A | | 27S190<br>27S290 | |
| Three-State | 27S191A<br>27S291A | 27S191<br>27S291<br>27PS191A<br>27PS291A | 27S191A<br>27S291A | 27PS191<br>27PS291 | 27S191<br>27S291<br>27PS191A<br>27PS291A | 27PS191<br>27PS291 |

IMOX is a trademark of Advanced Micro Devices, Inc.

02121B

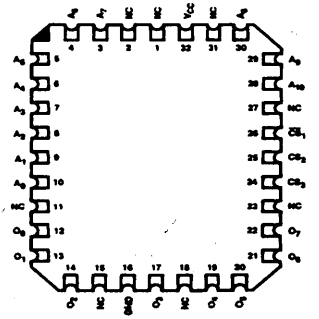
## CONNECTION DIAGRAM
Top View

### DIP




CD000390

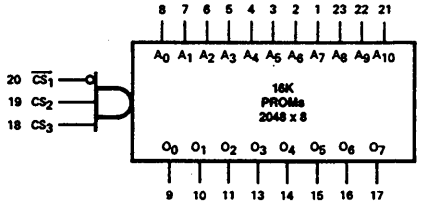
### Chip-Pak™ L-32-2



CD000400

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000030

$V_{CC}$ = Pin 18
GND = Pin 9

## ORDERING INFORMATION

**Am27S291 A P C B**

- **B** — Burn-in Option
  - B suffix indicates 160 hour burn-in.
- **C** — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **P** — Package
  - D – 24-pin ceramic DIP
  - F – 24-pin flatpak
  - L – 32-pin leadless chip carrier
  - P – 24-pin plastic DIP
  - Note: Series 700 devices are packaged in structured 600 mil DIPs; 200 devices are packaged in space-saving 300 mil DIPs.
- **A** — Speed Select
  - See Product Selector Guide
- **Am27S291** — Device Type
  - Output Configuration – See Product Selector Guide
  - 27S – Standard Devices
  - 27PS – Power Switched Devices

| Valid Combinations | |
|---|---|
| Am27S190<br>Am27S190A<br>Am27S191<br>Am27S191A<br>Am27PS191<br>Am27PS191A | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |
| Am27S290<br>Am27S290A<br>Am27S291<br>Am27S291A<br>Am27PS291<br>Am27PS291A | PC, PCB,<br>DC, DCB,<br>DM, DMB |

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## NOTES ON POWER SWITCHING

The Am27PS191A/191 and Am27PS291A/291 are power switched devices. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, $I_{CC}$ is reduced to less than half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS191A/191 and Am27PS291A/291 are selected, a current surge is placed on the $V_{CC}$ supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1$\mu$f ceramic capacitor be connected from pin 24 to pin 12 at each device. (See Figure 1.)
2. Address access time ($t_{AA}$) can be optimized if a chip enable set-up time ($t_{EAS}$) of greater than 25ns is observed. Negative set-up times on chip enable $t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B)

## OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error and higher cost.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +$V_{CC}$ max
DC Voltage Applied to Outputs
During Programming ..... 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) ..... 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

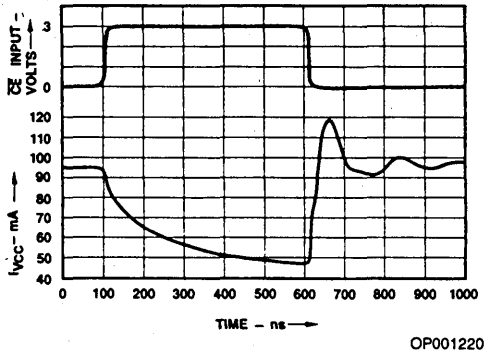
| Symbol | Parameter | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ (27TS Devices only) | Output HIGH Voltage | $V_{CC}$ = MIN, $I_{OH}$ = −2.0mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $I_{OL}$ = 16mA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | 0.50 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 4) | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 4) | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.45V | | | −0.010 | −0.250 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = $V_{CC}$ | | | | 40 | µA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 2) | COM'L | −20 | −40 | −90 | mA |
| | | | MIL | −15 | −40 | −90 | |
| $I_{CC}$ | Power Supply Current | All Inputs = GND | | | 115 | 185 | mA |
| $I_{CCD}$ (27PS Devices only) | Power Down Supply Current | $\overline{CS}_1$ = 2.7V; All other inputs = GND | | | 50 | 80 | |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{CC}$ = MAX<br>$V_{\overline{CS}_i}$ = 2.4V | $V_O$ = $V_{CC}$ | | | 40 | µA |
| | | | $V_O$ = 0.4V | | | −40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0V @ f = 1MHz (Note 3) | | | 4.0 | | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0V @ f = 1MHz (Note 3) | | | 8.0 | | |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## DC OPERATING CHARACTERISTICS

Typical $I_{VCC}$ Current Surge without 0.1μF
($I_{VCC}$ is Current Supplied by $V_{CC}$ Power Supply)

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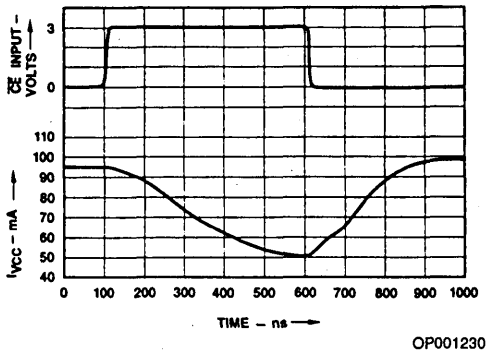
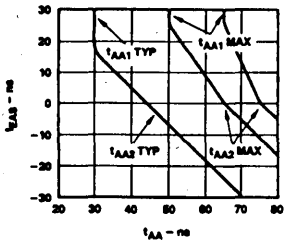
Typical $I_{VCC}$ Current Surge without 0.1μF
($I_{VCC}$ is Current Supplied by $V_{CC}$ Power Supply)



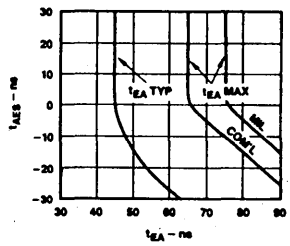

OP001230

Figure 1. $I_{CC}$ Current




OP001190

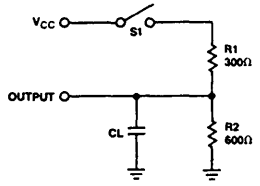
Figure 2A. $t_{AA}$ vs $t_{EAS}$ (Am27PS191A/291A)




OP001200

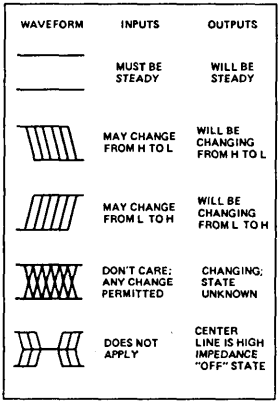
Figure 2B. $t_{EA}$ vs $t_{AES}$

## SWITCHING TEST CIRCUIT




TC000170

## KEY TO SWITCHING WAVEFORMS




KS000010

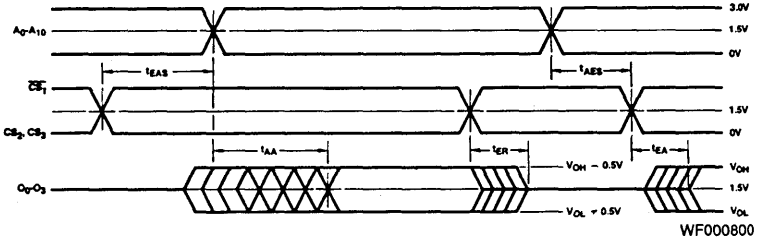
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | 27S C devices Min | 27S C devices Max | 27S M devices Min | 27S M devices Max | 27PS C devices Min | 27PS C devices Max | 27S M devices Min | 27S M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AA}$ | Address Access Time | STD | | 50 | | 65 | | 65 | | 75 | ns |
| | | | A | | 35 | | 50 | | 50 | | 65 | |
| 2 | $t_{EA}$ | Enable Access Time | STD | | 25 | | 30 | | 80 | | 90 | |
| | | | A | | 25 | | 30 | | 65 | | 75 | |
| 3 | $t_{ER}$ | Enable Recovery Time | STD | | 25 | | 30 | | 35 | | 45 | |
| | | | A | | 25 | | 30 | | 25 | | 30 | |
| 4 | $t_{AAPS}$ | Power Switched Address Access Time (27PS devices only) | STD | | | | | | 80 | | 90 | |
| | | | A | | | | | | 65 | | 75 | |

Notes: 5. $t_{AA}$ is tested with switch $S_1$ closed and $C_L = 30pF$.

6. $t_{EA}$ is tested with $C_L = 30pF$ to the 1.5V level; $S_1$ is open for high impedance to HIGH tests and closed for high impedance to LOW tests. $t_{ER}$ is tested with $C_L = 5pF$. HIGH to high impedance tests are made with $S_1$ open to an output voltage of $V_{OH}-0.5V$ with $S_1$ open; LOW-to-high impedance tests are made to the $V_{OL}+0.5V$ level with $S_1$ closed. $ICOL

## SWITCHING WAVEFORMS




WF000800

Note: Level on output while $\overline{CS_1}$ is HIGH or $CS_2$ or $CS_3$ are LOW is determined externally.

For programming information, please see "Guide to the *Programming* of AMD's Generic Bipolar PROMs", page 2-1.

# Replacement Referrals

| Part Number | Replaced by |
|---|---|
| Am27S20 | Am29760A |
| Am27S21 | Am29761A |
| Am29770 | Am27S12 |
| Am29771 | Am27S13 |
| Am29775 | Am27S27 |

# Bipolar Random Access Memories (RAM) Index

# Am29705A/707

16-Word by 4-Bit 2-Port RAM

## DISTINCTIVE CHARACTERISTICS

- 16-word by 4-bit, 2-port RAM
- Two output ports, each with separate output control
- Separate four-bit latches on each output port (Am29707 has separate output control)
- Data output is noninverting with respect to data input
- Chip select and write enable inputs for ease in cascading
- Am29707 offers 20% improved cycle time over Am29705A when used with Am29203 in three address architecture
- Am29705A is a pin-for-pin replacement for the Am29705 but is significantly faster on critical paths

## GENERAL DESCRIPTION

The Am29705A is a 16-word by 4-bit, two-port RAM. This RAM features two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit Latch but a common Latch Enable (LE) input is used to control all eight latches. The device has two Write Enable ($\overline{WE}$) inputs and is designed such that the Write Enable 1 ($\overline{WE_1}$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge triggered.

The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

The Am29705A features three-state outputs and several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE}$-A input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE}$-B input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

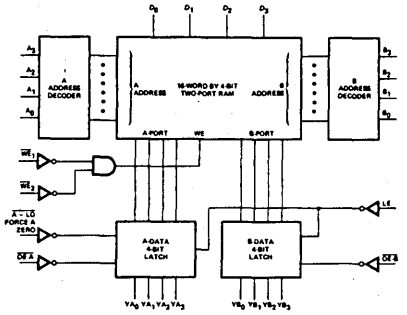
The Write Enable inputs control the writing of new data into the RAM. When both Write Enable inputs are LOW, new data is written into the word selected by the B-address field. When either Write Enable input is HIGH, no data is written into the RAM.

The Am29707 is an identical circuit to the Am29705A, except each output port has a separate Latch Enable (LE) input. An extra write enable input ($\overline{WE_2}$) may be connected directly to the IEN of the Am29203 for improved cycle times over the Am29705A. The $\overline{WE}$/BLE input can then be connected directly to system clock.

The Am29705A is a plug-in replacement for the Am29705, but is significantly faster. The Am29705A and Am29707 feature AMD's advanced ion-implanted micro-oxide (IMOX™) processing.

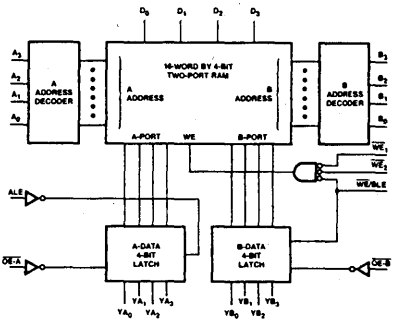
## BLOCK DIAGRAMS

Am29705A



BD000780

Am29707



BD000790

## RELATED PRODUCTS

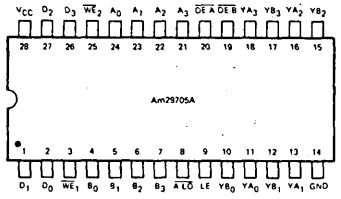
| | | | |
|---|---|---|---|
| Am29751A | Bipolar PROM | Am2904 | Status and Shift Control Unit |
| Am2921 | One-of-Eight Decoder | Am2910A | Microprogram Controller |
| Am25LS138 | One-of-Four Decoder | Am2914 | Vectored Priority Interrupt Controller |
| Am25LS139 | Dual One-of-Four Decoder | Am2940 | DMA Address Generator |
| Am25LS157 | Quad 2-by-1 MUX | Am2950-54 | 8 Bit Bidirectional I/O Port |
| Am29203 | Four Bit Bipolar Microprocessor Slice | Am29118 | 8 Bit Bidirectional I/O Port with ACC |
| Am2902A | Carry Look Ahead Generator | | |

IMOX is a trademark of Advanced Micro Devices, Inc.

03587D

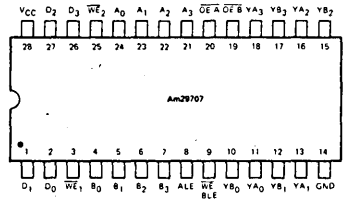
## CONNECTION DIAGRAMS – TOP VIEWS

**D-28-1***
**P-28-1***




CD001060

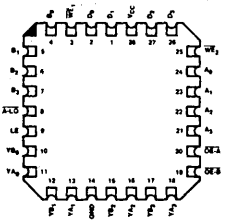
**D-28-1***
**P-28-1***




CD001050

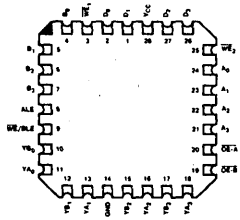
*Devices are also offered in a 28 pin flatpak.
Connections are the same as DIPs.

**L-28-1**



CD001080

**L-28-1**

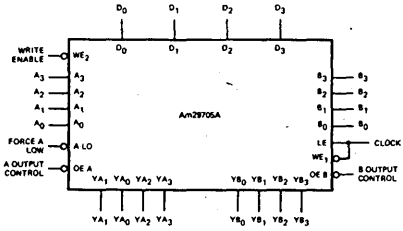


CD001070

Note: Pin 1 is marked for orientation

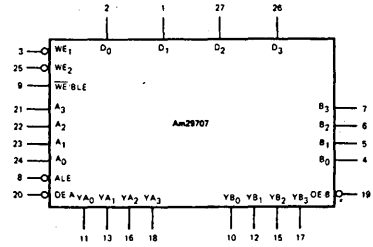
## LOGIC SYMBOLS

**Am29705A**



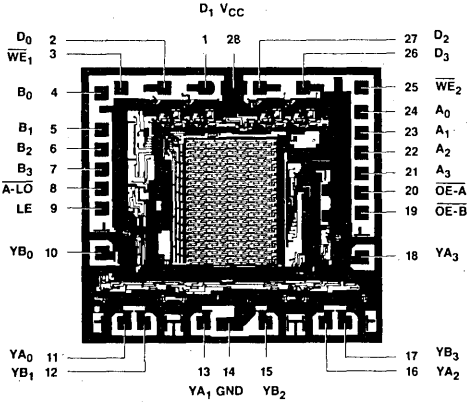

LS000340

**Am29707**




LS000330

## METALLIZATION AND PAD LAYOUT




DIE SIZE: .104 x .96

## ORDERING INFORMATION

Am29707 A D C B

- B — Burn-In Option: B = 96 hour burn-in
- C — Temperature Range: C = 0 to +70°C; M = −55 to +125°C
- D — Package: D = 28 pin ceramic SLIMDIP; F = 28 pin Flat Pak; L = 28 pin Chip Pak; P = 28 pin Molded Dip; X = 28 Dice
- A — Speed: See Product Select Guide
- Am29707 — Part Number

| Valid Combinations | |
|---|---|
| Am29707 | DC, DCB, DMB,FMB, LC, LMB, PC, XC, XM |
| Am29707 | DC, DCB, DMB, FMB, LC, LMB, PC, XC, XM |

## PIN DESCRIPTION

**$D_0 - D_3$** **Data Inputs**
New data is written into the RAM through these inputs.

**$A_0 - A_3$** **The A-Address Inputs**
The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

**$B_0 - B_3$** **The B-Address Inputs**
The four bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

**$YA_0 - YA_3$** **The Four A-Data Latch Outputs**

**$YB_0 - YB_3$** **The Four B-Data Latch Outputs**

**$\overline{WE}_1$, $\overline{WE}_2$** **Write Enables**
When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

**$\overline{OE}$-A** **A-Port Output Enable**
When $\overline{OE}$-A is LOW, data in the A-Data Latch is present at the $YA_i$ outputs. If $\overline{OE}$-A is HIGH the $YB_i$ outputs are in the high-impedance (off) state.

**$\overline{OE}$-B** **B-Port Output Enable**
When $\overline{OE}$-B is LOW, data in the B-Data Latch is present at the $YB_i$ outputs. When $\overline{OE}$-B is HIGH the $YB_i$ outputs are in the high-impedance (off) state.

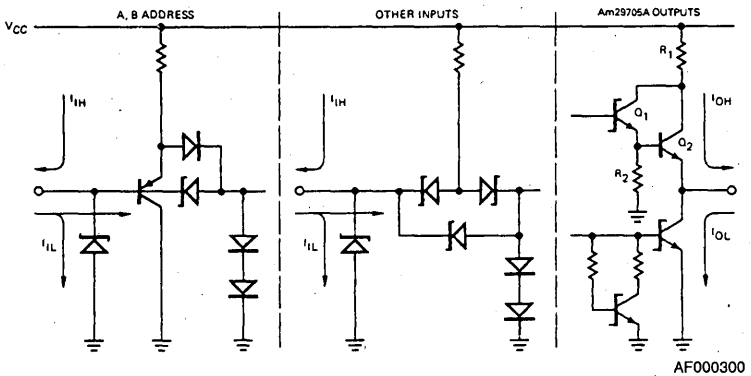
**LE** **Latch Enable**
The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs. (Am29705A only.)

**$\overline{A\text{-}LO}$** **Force A Zero**
This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed. (Am29705A only.)

**ALE** **A-Output Port Latch Enable**
When ALE is HIGH, the A latch is open (transparent) and data from the RAM, as selected by the A address field, is present at the A output. When ALE is LOW, the A latch is closed and retains the last data read from the RAM independent of the current A address field input. (Am29707 only.)

**$\overline{WE}$/BLE** **Write Enable/B-Output Port Latch Enable**
When $\overline{WE}$/BLE is LOW together with $\overline{WE}_1$ and $\overline{WE}_2$, new data is written into the word selected by the B address field. When $\overline{WE}$/BLE or any Write Enable input is HIGH, no data is written into the RAM.
$\overline{WE}$/BLE also controls the B output port. When $\overline{WE}$/BLE is HIGH, the B latch is open (transparent), and when this input is LOW, the B latch is closed (Am29707 only).

## INPUT/OUTPUT CURRENT INTERFACE CONDITIONS




Note: Actual current flow direction shown.

## FUNCTION TABLES

### Am29705A

#### WRITE CONTROL

| $\overline{WE_1}$ | $\overline{WE_2}$ | Function | RAM Outputs at Latch Inputs | |
|---|---|---|---|---|
| | | | A-Port | B-Port |
| L | L | Write D into B | A data (A ≠ B) | Input Data |
| L | L | Write D into B | (A = B) Input Data | Input Data |
| X | H | No Write | A Data | B Data |
| H | X | No Write | A Data | B Data |

H = HIGH L = LOW X = Don't Care

#### YA READ

| Inputs | | | YA Output | Function |
|---|---|---|---|---|
| $\overline{OE}$-A | A-$\overline{LO}$ | LE | | |
| H | X | X | Z | High Impedance |
| L | L | X | L | Force YA LOW |
| L | H | H | A-Port RAM Data | Latches Transparent |
| L | H | L | NC | Latches Retain Data |

H = HIGH X = Don't Care NC = No Change
L = LOW Z = High Impedance

#### YB READ

| Inputs | | YB Output | Function |
|---|---|---|---|
| $\overline{OE}$-B | LE | | |
| H | X | Z | High Impedance |
| L | H | B-Port RAM Data | Latches Transparent |
| L | L | NC | Latches Retain Data |

H = HIGH X = Don't Care NC = No change
L = LOW Z = High Impedance

### Am29707

#### WRITE CONTROL

| $\overline{WE_1}$ | $\overline{WE_2}$ | $\overline{WE}$/BLE | Function | RAM Outputs at Latch Inputs | |
|---|---|---|---|---|---|
| | | | | A-Port | B-Port |
| L | L | L | Write D into B | A Data (A = B) | Input Data |
| X | X | H | No Write | A Data | B Data |
| X | H | X | No Write | A Data | B Data |
| H | X | X | No Write | A Data | B Data |

H = HIGH L = LOW X = Don't Care

#### YA READ

| Inputs | | YA Output | Function |
|---|---|---|---|
| $\overline{OE}$-A | ALE | | |
| H | X | Z | High Impedance |
| L | H | A-Port RAM Data | Latches Transparent |
| L | L | NC | Latches Retain Data |

H = HIGH D = Don't Care NC = No Change
L = LOW Z = High Impedance

#### YB READ

| Inputs | | YB Output | Function |
|---|---|---|---|
| $\overline{OE}$-B | $\overline{WE}$/BLE | | |
| H | X | Z | High Impedance |
| L | H | B-Port RAM Data | Latches Transparent |
| L | L | NC | Latches Retain Data |

H = HIGH D = Don't Care NC = No Change
L = LOW Z = High Impedance

## LOADING RULES (In Unit Loads)

| Input/Output | Pin No.'s | Input Unit Load | Fan-out Output HIGH | Fan-out Output LOW |
|---|---|---|---|---|
| $D_1$ | 1 | 1 | – | – |
| $D_0$ | 2 | 1 | – | – |
| $\overline{WE_1}$ | 3 | 1 | – | – |
| $B_0$ | 4 | 0.55 | – | – |
| $B_1$ | 5 | 0.55 | – | – |
| $B_2$ | 6 | 0.55 | – | – |
| $B_3$ | 7 | 0.55 | – | – |
| $\overline{A\text{-}LO}$ (29705A Only) | 8 | 1 | – | – |
| LE (29705A Only) | 9 | 1 | – | – |
| ALE (29707 Only | 8 | 1 | – | – |
| $\overline{WE}$/BLE (29707 Only) | 9 | 1 | – | – |
| $YB_0$ | 10 | – | 100/200 | 33 |
| $YA_0$ | 11 | – | 100/200 | 33 |
| $YB_1$ | 12 | – | 100/200 | 33 |
| $YA_1$ | 13 | – | 100/200 | 33 |
| GND | 14 | – | – | – |
| $YB_2$ | 15 | – | 100/200 | 33 |
| $YA_2$ | 16 | – | 100/200 | 33 |
| $YB_3$ | 17 | – | 100/200 | 33 |
| $YA_3$ | 18 | – | 100/200 | 33 |
| $\overline{OE}$-B | 19 | 1 | – | – |
| $\overline{OE}$-A | 20 | 1 | – | – |
| $A_3$ | 21 | 0.55 | – | – |
| $A_2$ | 22 | 0.55 | – | – |
| $A_1$ | 23 | 0.55 | – | – |
| $A_0$ | 24 | 0.55 | – | – |
| $\overline{WE_2}$ | 25 | 1 | – | – |
| $D_3$ | 26 | 1 | – | – |
| $D_2$ | 27 | 1 | – | – |
| $V_{CC}$ | 28 | – | – | – |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground
Potential Continuous ..... −0.5V to +7.0V
DC Voltage Applied to OUtput
for HIGH Output State ..... −0.5V to +$V_{CC}$max
DC Input Voltage ..... −0.5V to +5.5V
DC Output Current, Into
Output ..... 30mA
DC Input Current ..... −30mA to +5.0mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions (Note 1) | | Min | Typ (Note 2) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = MIN.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | MIL, $I_{OH}$ = −2.0mA | 2.4 | | | Volts |
| | | | COM'L, $I_{OH}$ = −4.0mA | 2.4 | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA (MIL) | | | 0.5 | Volts |
| | | | $I_{OL}$ = 20mA (COM) | | | 0.5 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs | | | | 0.8 | Volts |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = MIN., $I_{IN}$ = −18mA | | | | −1.5 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX.,<br>$V_{IN}$ = 0.5V | All | | | −0.36 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 2.7V | | | | 20 | μA |
| $I_I$ | Input HIGH Current | $V_{CC}$ = MAX., $V_{IN}$ = 55V | | | | 0.1 | mA |
| $I_O$ | Off State (High Impedance) Output Current | $V_{CC}$ = MAX.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $V_O$ = 2.4V | | | 20 | μA |
| | | | $V_O$ = 0.5V | | | −20 | |
| $I_{SC}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = MAX. | | −30 | | −85 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = MAX.<br>(Worst case $I_{CC}$ is at minimum temperature)<br>(Note 4) | | | | | mA |
| | | | $T_A$ = 0°C to +70°C | | | 210 | |
| | | | $T_A$ = 70°C | | | 170 | |
| | | | $T_C$ = −55°C to +125°C | | | 210 | |
| | | | $T_C$ = 125°C | | | 150 | |

Notes:

1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC}$ = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded except $\overline{OE\text{-}A}$ and $\overline{OE\text{-}B}$ = 2.4V.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| Parameters | From | To | Test Conditions | COM'L | MIL |
|---|---|---|---|---|---|
| Access Time | A Address Stable or B Address Stable | YA Stable or YB Stable | LE = HIGH | 25 | 30 |
| Turn-On Time | $\overline{OE}$-A or $\overline{OE}$-B LOW | YA or YB Stable | | 20 | 20 |
| Turn-Off Time | $\overline{OE}$-A or $\overline{OE}$-B HIGH | YA or YB Off | $C_L$ = 5pF Note 1 | 20 | 20 |
| Reset Time | $\overline{A\text{-}LO}$ LOW | YA LOW | | 20 | 20 |
| Latch Enable Time | LE HIGH | YA and YB Stable | | 20 | 22 |
| Transparency | $\overline{WE_1}$ and $\overline{WE_2}$ LOW | YA or YB | LE = HIGH | 30 | 35 |
| | D | YA or YB | LE = HIGH | 30 | 35 |

Note 1. Measured from 1.5V at the input to 0.5V change in the output level.

## MINIMUM SETUP AND HOLD TIME (In ns)

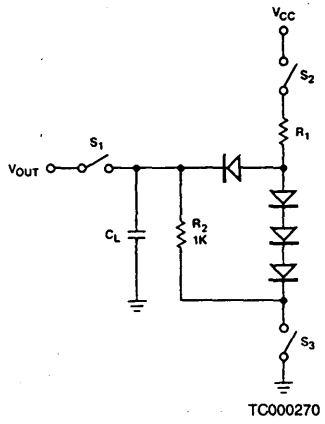
| Parameters | From | To | Test Conditions | COM'L | MIL |
|---|---|---|---|---|---|
| Data Setup Time | D Stable | Either $\overline{WE}$ HIGH | | 12 | 15 |
| Data Hold Time | Either $\overline{WE}$ | D Changing | | 0 | 0 |
| Address Setup Time | B Stable | Both $\overline{WE}$ LOW | | 6 | 8 |
| Address Hold Time | Either $\overline{WE}$ HIGH | B Changing | | 0 | 0 |
| Latch Close Before Write Begins | LE LOW | $\overline{WE_1}$ LOW | $\overline{WE_2}$ LOW | 0 | 0 |
| | LE LOW | $\overline{WE_2}$ LOW | $\overline{WE_1}$ LOW | 0 | 0 |
| Address Setup Before Latch Closes | A or B Stable | LE LOW | | 12 | 15 |

## MINIMUM PULSE WIDTHS

| Parameters | Input | Pulse | Test Conditions | COM'L | MIL |
|---|---|---|---|---|---|
| Write Pulse Width | $\overline{WE_1}$ | HIGH-LOW-HIGH | $\overline{WE_2}$ LOW | 15 | 15 |
| | $\overline{WE_2}$ | HIGH-LOW-HIGH | $\overline{WE_1}$ LOW | 15 | 15 |
| A Latch Reset Pulse | $\overline{A\text{-}LO}$ | HIGH-LOW-HIGH | | 15 | 15 |
| Latch Data Capture | LE | LOW-HIGH-LOW | | 15 | 18 |

Note: The Am29705A meets or exceeds all of the specifications of the Am29705.

## A. THREE-STATE OUTPUTS




TC000270

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

Notes:

1. $C_L$ = 50pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. $S_1$, $S_2$, $S_3$ are closed during function tests and all A.C. tests except output enable tests.
3. $S_1$ and $S_3$ are closed while $S_2$ is open to $t_{PZH}$ test. $S_1$ and $S_2$ are closed while $S_3$ is open for $t_{PZL}$ test.
4. $C_L$ = 5pF for output disable tests.

**TEST OUTPUT LOADS FOR Am29705A**

| Pin # (DIP) | Pin Label | Test Circuit | $R_1$ | $R_2$ |
|---|---|---|---|---|
| – | $YA_0 - YA_3$, $YB_0 - YB_3$ | A | 230 | 1k |

### Notes on Testing

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful:

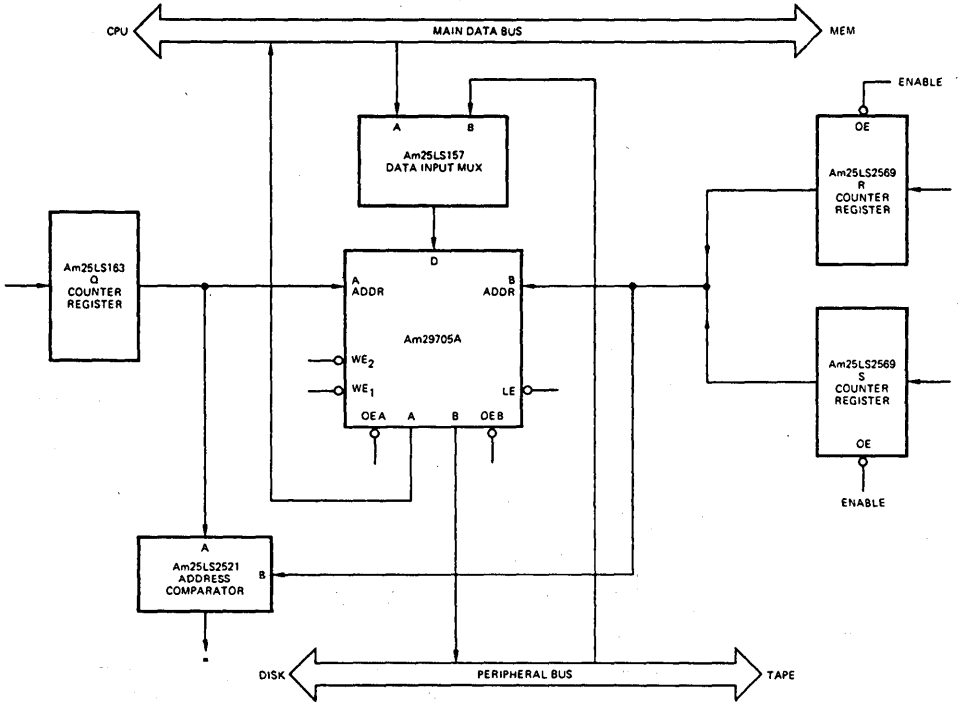
1. Insure the part is adequately decoupled at the test head. Large changes in $V_{CC}$ current as the device switches may cause erroneous function failures due to $V_{CC}$ changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400mA in 5–8ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach $V_{IL}$ or $V_{IH}$ until the noise has settled. AMD recommends using $V_{IL} \leqslant 0V$ and $V_{IH} \geqslant 3V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide Fairchild Sentry programs, under license.

## USING THE Am29705A AND Am29707

The Am2903 and Am29203 each contain only 16 scratch-pad registers plus the Q register. For applications which require more than 17 registers, the register set of the Am2903 and Am29203 can be easily expanded.

- Use the Am29705A with the Am2903A
- Use the Am29707 with the Am29203

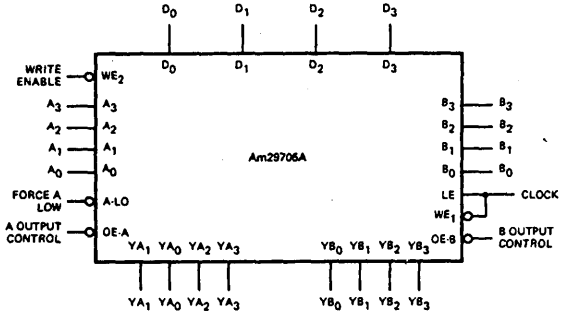
For further applications information on using the Am29705A with the Am2903A, see Chapter III of *Bit Slice Microprocessor Design*, Mick and Brick, McGraw-Hill Publications.




AF000270

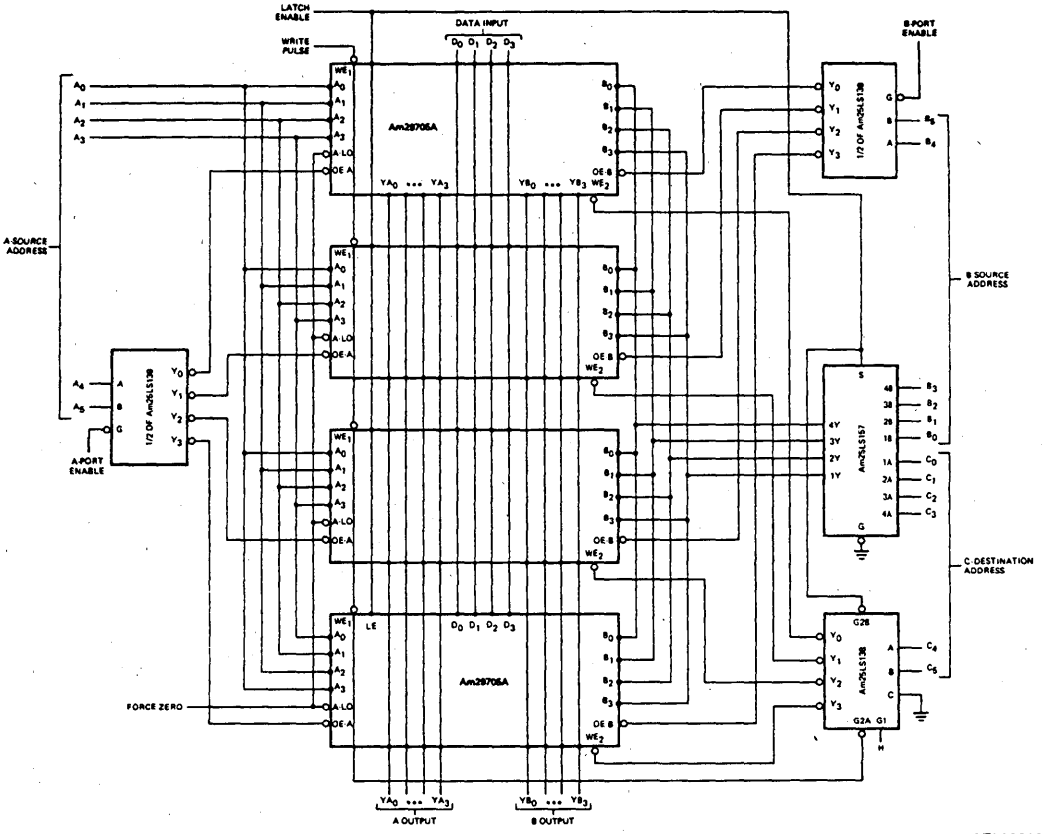
The Am29705A as a two-way interface buffer. Data may be passed between the main data bus and the peripheral data bus under I/O control. The two-port RAM allows data to be written into buffer storage from a peripheral device, using the B address port and the S counter register, while it is being read into main memory, using the A address port and the Q counter register. This simultaneous read/write capability facilitates DMA transfers because the CPU can ignore write requests from the peripheral device. Data output from CPU to the peripheral device is handled by sequential write and read operations. Data is written into buffer storage from the CPU, using the B address port and the R counter register. It is read onto the peripheral device using the B address port and either the R register, for single word transfers, or the S register, for block transfers.

## APPLICATIONS (Cont.)




LS000350

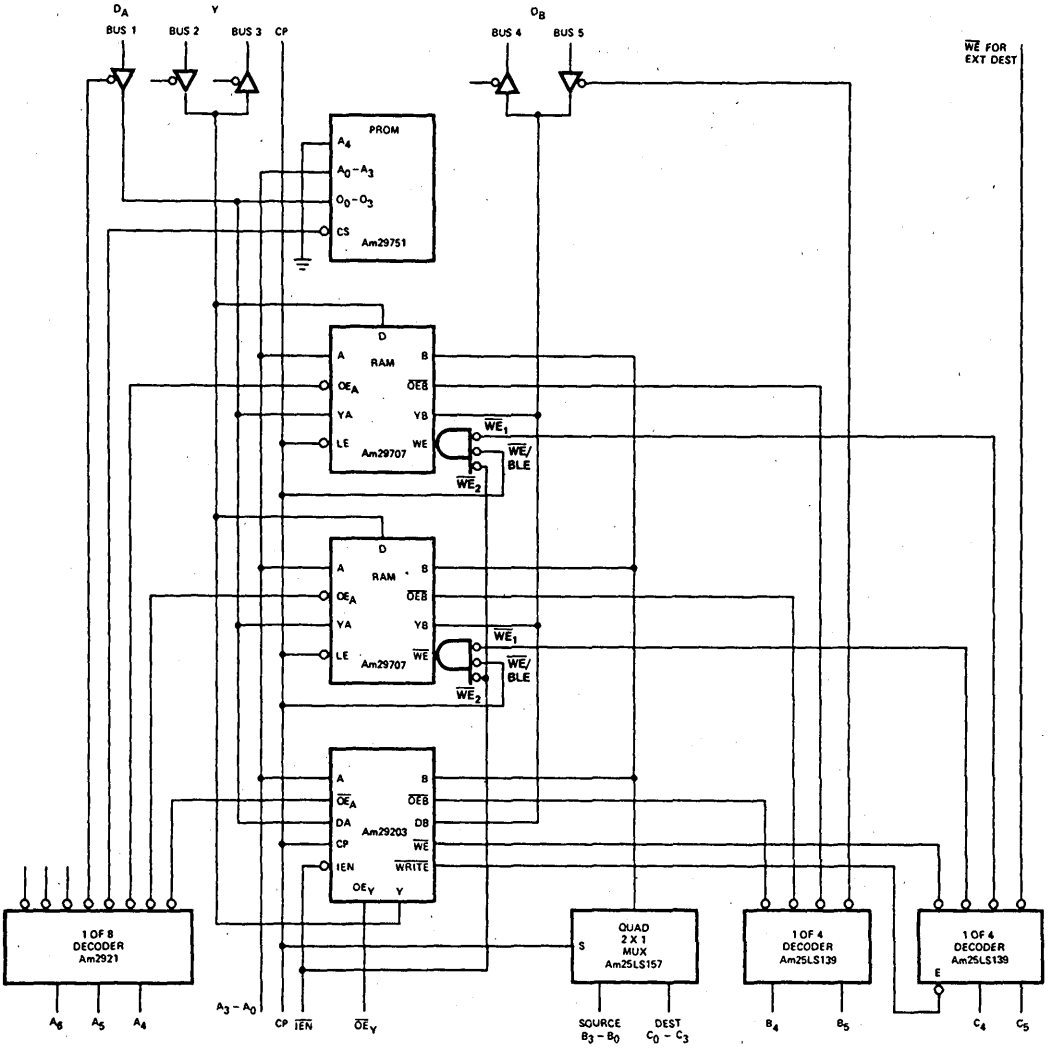
A 16-word by 4-bit two-port RAM with LE and $WE_1$ connected to make the device appear edge triggered. $WE_1$ and $WE_2$ are logically identical but are electrically slightly different. For synchronous operation without possibility of race, $WE_1$ should be connected to LE.




AF000290

A 64-word by 4-bit three address memory. Data is read from the A address to the YA outputs and from the B address to the YB outputs while the latch enable is HIGH. When the latch enable goes LOW, the YA and YB data is held in the internal latches, and the RAM B address is switched to the C-destination address lines. A write pulse will then deposit the input data into the location selected by the C address.

## APPLICATIONS (Cont.)




### Am29203 EXPANDED MEMORY

A 48-word by 4-bit expanded memory for the Am29203 using the Am29707. The Am29751 PROM serves as a constant store.

# Am93415/425

1024 x 1 bit TTL Bipolar IMOX™ RAM



## DISTINCTIVE CHARACTERISTICS

- Fully decoded 1024-word x 1-bit RAMs
- Ultra-high speed (SA) version:
  Address Access time typically 17ns
  High Speed (A) version:
  Address Access time typically 22ns
  Standard version:
  Address Action time typically 30ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am93425 series) or with open collector outputs (Am93415 series)
- Electrically tested and optically inspected die for the assemblers of hybrid products
- Plug in replacement for Fairchild 93415A/415 and 93425A/425, and Intel 2115/2125 series
- $I_{CC}$ decreases as temperature increases

## GENERAL DESCRIPTION

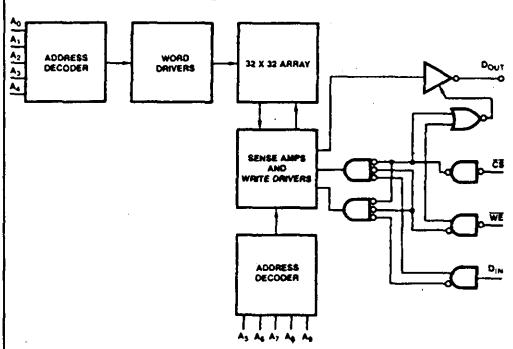
The Am93415 and Am93425 are fully decoded 1024 x 1 RAMs built with Schottky diode clamped transistors in conjunction with internal ECL circuitry. They are ideal for use in high speed control and buffer memory applications. Easy memory expansion is provided by an active LOW chip select input ($\overline{CS}$) and either open collector or three-state outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the data input ($D_{IN}$) is written into the addressed memory word and the output circuitry preconditioned so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output ($D_{OUT}$).

During the writing operation or any time the chip select line is HIGH the output of the memory goes to an inactive high impedance state.

## BLOCK DIAGRAM




BD000630

## MODE SELECT TABLE

| Inputs | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | $D_{OUT}$ | Mode |
| H | X | X | *HIGH-Z | Not Selected |
| L | L | L | *HIGH-Z | Write "0" |
| L | L | H | *HIGH-Z | Write "1" |
| L | H | X | Selected Data | Read |

H = HIGH L = LOW X = Don't Care
*HIGH-Z implies outputs are disabled or off. This condition is defined as a high impedance state for the Am93425 series and as an output high level for the Am93415 series.

## PRODUCT SELECTOR GUIDE

| Access Time | 20ns | 30ns | | 40ns | 45ns | 60ns |
|---|---|---|---|---|---|---|
| Temperature Range | C | C | M | M | C | M |
| Open Collector | Am93415SA | Am93415A | Am93415SA | Am93415A | Am93415 | Am93415 |
| Three-State | Am93425SA | Am93425A | Am93425SA | Am93425A | Am93425 | Am93425 |

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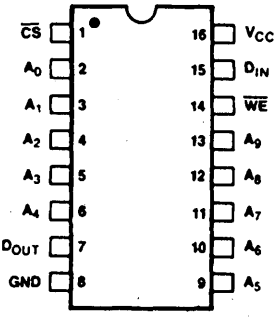
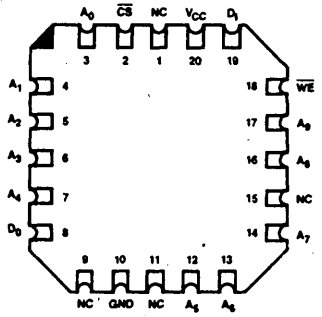
03195B

## CONNECTION DIAGRAM
Top View




CD000900




CD000910

## ORDERING INFORMATION

Am93425 SA P C B

- B — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 16-pin ceramic DIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
- SA — Speed Select
  - See Product Selector Guide
- Am93425 — Device Type
  - Am93415 series – Open Collector
  - Am93425 series – Three state

| Valid Combinations | |
|---|---|
| Am93415 | PC, |
| Am93415A | DC, DCB, |
| Am93415SA | LC, LCB, |
| Am93425 | DM, DMB, |
| Am93425A | FM, FMB, |
| Am93425SA | LM, LMB |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

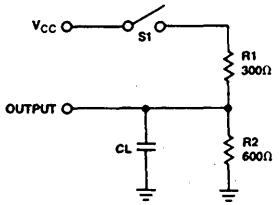
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | MAX | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −10.3mA | COM'L | 2.4 | 3.4 | | Volts |
| | | | $I_{OH}$ = −5.2mA | MIL | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | $I_{OL}$ = 16mA | | 0.33 | 0.45 | Volts |
| $V_{IH}$ | Input HIGH Level (Note 3) | Guaranteed input logical HIGH voltage for all inputs | | | 2.1 | 1.6 | | Volts |
| $V_{IL}$ | Input LOW Level (Note 3) | Guaranteed input logical LOW voltage for all inputs | | | | 1.5 | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.40V | | | | −90 | −400 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 4.5V | | | | 1 | 40 | μA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V | | | | −50 | −100 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND $V_{CC}$ = MAX | $T_A$ = 70°C | STD devices | | 100 | 130 | mA |
| | | | | L devices | | 55 | 75 | |
| | | | $T_A$ = 0°C | STD devices | | | 155 | |
| | | | | L devices | | | 80 | |
| | | | $T_A$ = −55°C | STD device | | | 170 | |
| | | | | L devices | | | 90 | |
| $V_{CL}$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −10mA | | | | −0.850 | −1.5 | Volts |
| $I_{CEX}$ | Output Leakage Current | $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{OUT}$ = 2.4V | | Am93415 Series Only | | 0 | 100 | μA |
| | | | | Am93425 Series Only | | 0 | 50 | |
| | | $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{OUT}$ = 0.5V, $V_{CC}$ = MAX | | Am93425 Series Only | −50 | 0 | | |
| $C_{IN}$ | Input Pin Capacitance | See Note 4 | | | | 4 | | pF |
| $C_{OUT}$ | Output Pin Capacitance | See Note 4 | | | | 7 | | pF |

Notes:

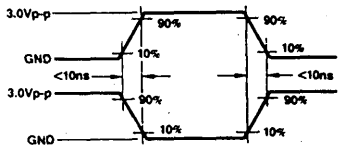
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies only to devices with three-state outputs. (Am93425 series)
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Input and output capacitance measured on a sample basis using pulse technique.

## SWITCHING TEST CIRCUIT



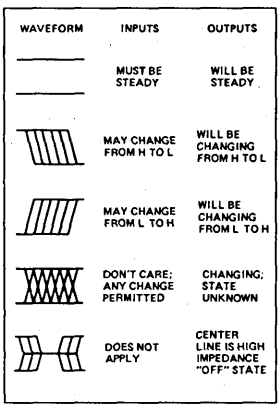

TC000170

## SWITCHING TEST WAVEFORM




TW000030

## KEY TO SWITCHING WAVEFORMS




KS000010

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am93415A/25A C devices Min | Am93415A/25A C devices Max | Am93415A/25A M devices Min | Am93415A/25A M devices Max | Am93415/25 C devices Min | Am93415/25 C devices Max | Am93415/25 M devices Min | Am93415/25 M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output | | 30 | | 40 | | 45 | | 60 | ns |
| 2 | $t_{PHL}(A)$ | | | | | | | | | | |
| 3 | $t_{PZH}\overline{CS}$ | Delay from Chip Select to Active Output and Correct Data | | 20 | | 30 | | 35 | | 45 | ns |
| 4 | $t_{PZL}\overline{CS}$ | | | | | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable to Active Output and Correct Data (Write Recovery) | | 25 | | 35 | | 40 | | 50 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | | | | | |
| 7 | $t_s(A)$ | Setup Time Address (Prior to Initiation of Write) | 5 | | 5 | | 10 | | 15 | | ns |
| 8 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 9 | $t_s(DI)$ | Setup Time Data Input (Prior to Initiation of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 10 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 11 | $t_s(\overline{CS})$ | Setup Time Chip Select (Prior to Initiation of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 12 | $t_h(\overline{CS})$ | Hold Time Chip Select (After Termination of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 13 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to Insure Write | 20 | | 30 | | 30 | | 40 | | ns |
| 14 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select to Inactive Output (HIGH-Z) | | 20 | | 30 | | 35 | | 50 | ns |
| 15 | $t_{PLZ}(\overline{CS})$ | | | | | | | | | | |
| 16 | $t_{PHZ}(\overline{WE})$ | Delay from Write Enable to Inactive Output (HIGH-Z) | | 20 | | 30 | | 35 | | 35 | ns |
| 17 | $t_{PLZ}(\overline{WE})$ | | | | | | | | | | |

## SWITCHING CHARACTERISTICS (Cont.)

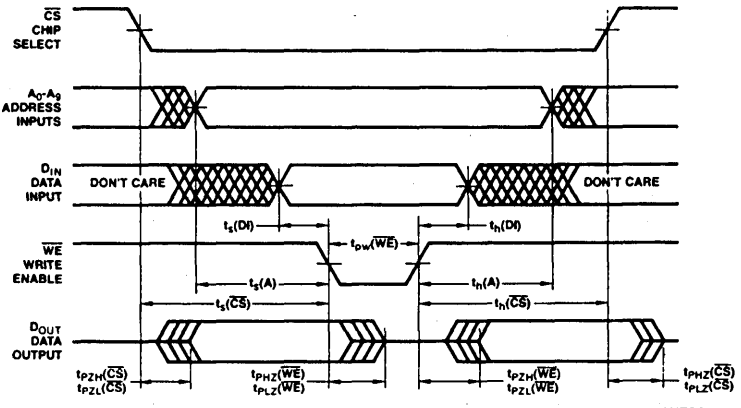
| No. | Symbol | Description | Am93415SA/25SA C devices Min | Am93415SA/25SA C devices Max | Am93415SA/25SA M devices Min | Am93415SA/25SA M devices Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output (Address Access Time) | | 20 | | 30 | ns |
| 2 | $t_{PHL}(A)$ | | | | | | |
| 3 | $t_{PZH}(\overline{CS})$ | Delay from Chip Select to Active Output and Correct Data | | 15 | | 25 | ns |
| 4 | $t_{PZL}(\overline{CS})$ | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable to Active Output and Correct Data (Write Recovery) | | 15 | | 25 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | |
| 7 | $t_s(A)$ | Setup Time Address (Prior to Initiation of Write) | 5 | | 5 | | ns |
| 8 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 0 | | 5 | | ns |
| 9 | $t_s(DI)$ | Setup Time Data Input (Prior to Initiation of Write) | 0 | | 5 | | ns |
| 10 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 0 | | 5 | | ns |
| 11 | $t_s(\overline{CS})$ | Setup Time Chip Select (Prior to Initiation of Write) | 5 | | 5 | | ns |
| 12 | $t_h(\overline{CS})$ | Hold Time Chip Select (After Termination of Write) | 0 | | 5 | | ns |
| 13 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to Insure Write | 15 | | 25 | | ns |
| 14 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select to Inactive Output (HIGH-Z) | | 20 | | 30 | ns |
| 15 | $t_{PLZ}(\overline{CS})$ | | | | | | |
| 16 | $t_{PHZ}(\overline{WE})$ | Delay from Write Enable to Inactive Output (HIGH-Z) | | 15 | | 25 | ns |
| 17 | $t_{PLZ}(\overline{WE})$ | | | | | | |

Notes:

1. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with $S_1$ closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
2. For open collector devices (Am93415 series), all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CE}$) inputs to the Data Output ($D_{OUT}$), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.
3. For 3-state output devices (Am93425 series), $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with $S_1$ open, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PZH}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with $S_1$ open and $C_L \leq 5pF$ and are measured between the 1.5V level on the input to the $V_{OH} - 500mV$ level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with $S_1$ closed and $C_L \leq 5pF$ and are measured between the 1.5V level on the input and the $V_{OL} + 500mV$ level on the output.

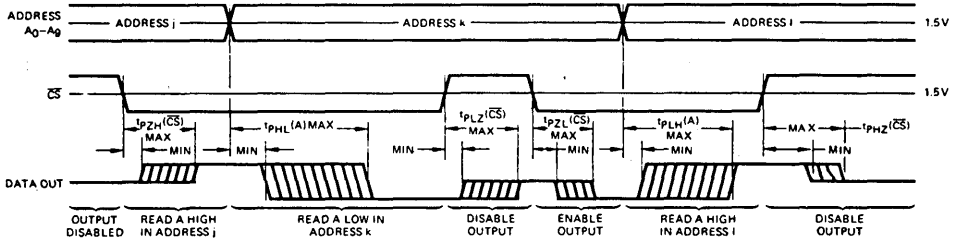
## SWITCHING WAVEFORMS

### WRITE MODE




WF001150

### READ MODE




WF001140

Switching delays from address and chip select inputs to the data output. For the Am93425A/425 disabled output is "OFF", represented by a single center line. For the Am93415A/415 a disabled output is HIGH.

# Am27S06/7

64-Bit Noninverting Bipolar RAM



## DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit low power Schottky RAMs
- High-speed: Address access time typically 40ns
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs (Am27LS07) or with open collector outputs (Am27LS06)
- Electrically tested and optically inspected die for the assemblers of hybrid products

## GENERAL DESCRIPTION

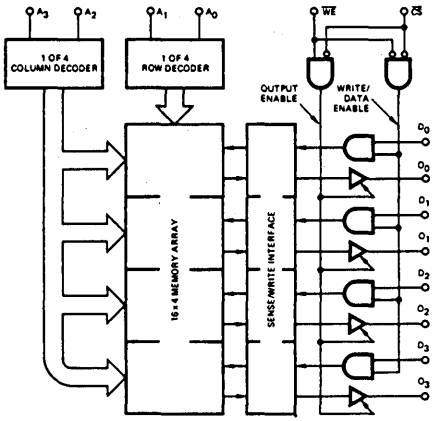
The Am27LS06 and Am27LS07 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs or three-state outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74LS189.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs $D_0$ to $D_3$ is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four noninverting outputs $O_0$ to $O_3$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

## BLOCK DIAGRAM




BD000560

## MODE SELECT TABLE

| Input | | Data Output Status $O_{0-3}$ | Mode |
|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | | |
| L | L | Output Disabled | Write |
| L | H | Selected Word | Read |
| H | X | Output Disabled | Deselect |

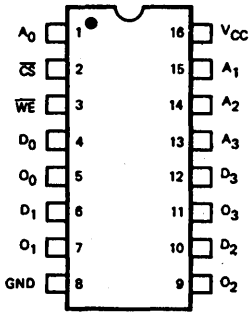
H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

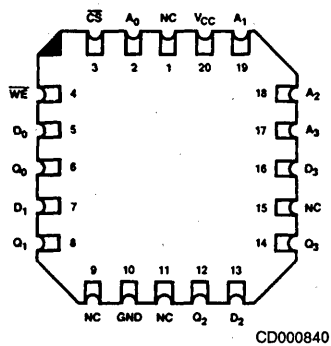
| Access Time | 25ns | 30ns | 35ns | 50ns | 55ns | 65ns |
|---|---|---|---|---|---|---|
| Temperature Range | C | M | C | M | C | M |
| Open Collector | 27S06A | 27S06A | 27S06 | 27S06 | 27LS06 | 27LS06 |
| Three-State | 27S07A | 27S07A | 27S07 | 27S07 | 27LS07 | 27LS07 |

03205C

## CONNECTION DIAGRAM
### Top View



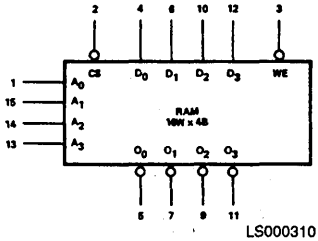

CD000870




CD000840

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000310

## ORDERING INFORMATION

**Am27S06 A P C B**

- **B** — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- **C** — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **P** — Package
  - D – 16-pin ceramic DIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
- **A** — Speed Select
  - See Product Selector Guide
- **Am27S06** — Device Type
  - Output Configuration
  - See Product Selector Guide

| Valid Combinations | |
|---|---|
| Am27S06<br>Am27LS06<br>Am27S07<br>Am27LS07 | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

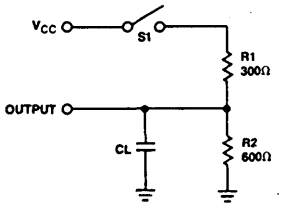
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameters | Test Conditions | | | 27S06/7 Min | 27S06/7 Typ | 27S06/7 Max | 27LS06/7 Min | 27LS06/7 Typ | 27LS06/7 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −5.2mA | | 2.4 | 3.2 | | 2.4 | 3.6 | | Volts |
| | | | $I_{OH}$ = −2.0mA | | | | | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA | | | 350 | 450 | | 280 | 450 | mV |
| | | | $I_{OL}$ = 20mA | | | 380 | 500 | | 310 | 500 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | | | 2.0 | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | | | | 0.8 | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.40V | $\overline{WE}$, $D_0$–$D_3$, $A_0$–$A_3$ | | | −15 | −250 | | −15 | −250 | µA |
| | | | $\overline{CS}$ | | | −30 | −250 | | −30 | −250 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.4V | | | | 0 | 10 | | 0 | 10 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −45 | −90 | −20 | −45 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All Inputs = GND, $V_{CC}$ = MAX | COM'L | | | 75 | 100 | | 30 | 35 | mA |
| | | | MIL | | | 75 | 105 | | 30 | 38 | |
| $V_{CL}$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −0.85 | −1.2 | | −0.85 | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{\overline{CS}}$ = $V_{IH}$ or $V_{\overline{WE}}$ = $V_{IL}$, $V_{OUT}$ = 2.4V | | | | 0 | 40 | | 0 | 40 | µA |
| | | $V_{\overline{CS}}$ = $V_{IH}$ or $V_{\overline{EW}}$ = $V_{IL}$, $I_{VOUT}$ = 0.4V, $V_{CC}$ = MAX | | (Note 2) | −40 | 0 | | −40 | 0 | | |

Notes:

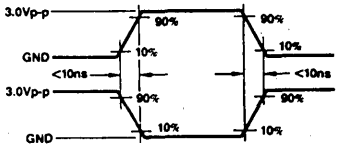
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

## SWITCHING TEST CIRCUIT



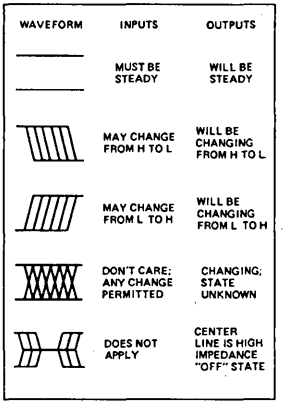

TC000170

## SWITCHING TEST WAVEFORM




TW000030

## KEY TO SWITCHING WAVEFORMS




KS000010

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am27S06A/7A A C devices Min | Am27S06A/7A A C devices Max | Am27S06A/7A A M devices Min | Am27S06A/7A A M devices Max | Am27S06/7 STD C devices Min | Am27S06/7 STD C devices Max | Am27S06/7 STD M devices Min | Am27S06/7 STD M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}$(A) | Delay from Address to Output | | 25 | | 30 | | 35 | | 50 | ns |
| 2 | $t_{PHL}$(A) | | | | | | | | | | |
| 3 | $t_{PZH}(\overline{CS})$ | Delay from Chip Select (LOW) to Active Output and Correct Data | | 15 | | 20 | | 17 | | 25 | ns |
| 4 | $t_{PZL}(\overline{CS})$ | | | | | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery-See Note 1) | | 20 | | 25 | | 35 | | 40 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | | | | | |
| 7 | $t_s$(A) | Setup Time Address (Prior to Initiation of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 8 | $t_h$(A) | Hold Time Address (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 9 | $t_s$(DI) | Setup Time Data Input (Prior to Termination of Write) | 20 | | 25 | | 25 | | 25 | | ns |
| 10 | $t_h$(DI) | Hold Time Data Input (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 11 | $t_{pw}(\overline{WE})$ | MIN Write Enable Width Pulse to Insure Write | 20 | | 25 | | 25 | | 25 | | ns |
| 12 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select (HIGH) to inactive Output (HI-Z) | | 15 | | 20 | | 17 | | 25 | ns |
| 13 | $t_{PLZ}(\overline{CS})$ | | | | | | | | | | |
| 14 | $t_{PLZ}(\overline{WE})$ | Delay from Write Enable (LOW) to Inactive Output (HI-Z) | | 20 | | 25 | | 25 | | 35 | ns |
| 15 | $t_{PHZ}(\overline{WE})$ | | | | | | | | | | |

## SWITCHING CHARACTERISTICS (Cont.)

| No. | Symbol | Description | Am27LS06A/7A C devices Min | Am27LS06A/7A C devices Max | Am27LS06/7 M devices Min | Am27LS06/7 M devices Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output | | 55 | | 65 | ns |
| 2 | $t_{PHL}$ | | | | | | |
| 3 | $t_{PZH}(\overline{CS})$ | Delay from Chip Select to Active Output and Correct Data | | 30 | | 35 | ns |
| 4 | $t_{PZL}(\overline{CS})$ | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery-See Note 2) | | 30 | | 35 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | |
| 7 | $t_s(A)$ | Setup Time Address (Prior to Initiation of Write) | 0 | | 0 | | ns |
| 8 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 0 | | 0 | | ns |
| 9 | $t_s(DI)$ | Setup Time Data Input (Prior to Termination of Write) | 45 | | 55 | | ns |
| 10 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 0 | | 0 | | ns |
| 11 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to Insure Write | 45 | | 55 | | ns |
| 12 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select to Inactive Output (HI-Z) | | 30 | | 35 | ns |
| 13 | $t_{PLZ}(\overline{CS})$ | | | | | | |
| 14 | $t_{PLZ}(\overline{WE})$ | Delay from Write Enable (LOW) to Inactive Output (HI-Z) | | 30 | | 35 | ns |
| 15 | $t_{PHZ}(\overline{WE})$ | | | | | | |

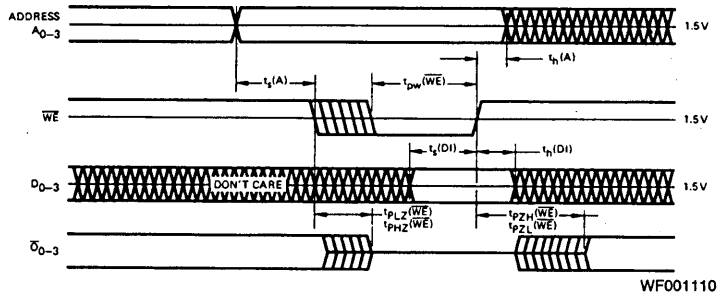
Notes:

1. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with $S_1$ closed and $C_L$ = 30pF with both input and output timing referenced to 1.5V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output ($D_{OUT}$), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed and $C_L$ = 30pF; and with both the input and output timing referenced to 1.5V.
4. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with $S_1$ open, $C_L$ = 30pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed, $C_L$ = 30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with $S_1$ open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input to the $V_{OH}$ – 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with $S_1$ closed and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the $V_{OL}$ + 500mV level on the output.

## SWITCHING WAVEFORMS

### WRITE MODE

### ($\overline{CS}$ = LOW unless otherwise noted)

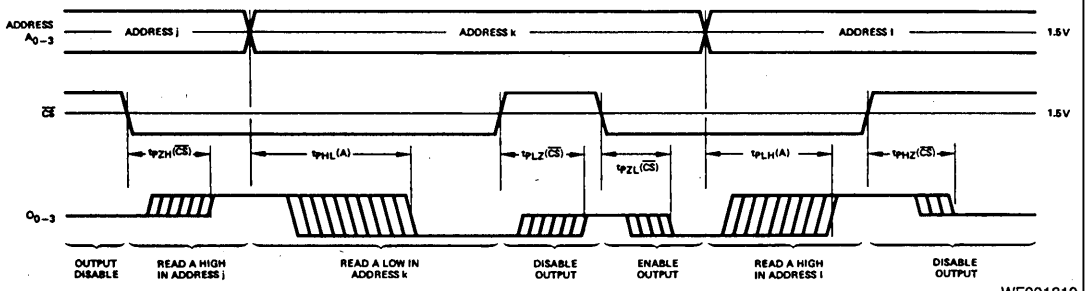



WF001110

Write Cycle Timing. The cycle in initiated by an address change. After $t_s(A)$min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S07A/07) while the write enable is LOW.

## SWITCHING WAVEFORMS

### READ MODE




WF001210

Switching delays from address and chip select inputs to the data output. For the Am27S06A/06 disabled output is "OFF", represented by a single center line. For the Am27S06A/06 disabled output is HIGH.

# Am27S02/3

64-Bit Schottky Bipolar RAM

## DISTINCTIVE CHARACTERISTICS

- Ultra-Fast "A" Version: Address access time 25ns
- Low Power
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with open collector outputs (Am27S02/02A) or with three-state outputs (Am27S03/03A)
- Pin compatible replacements for 3101A, 74S289, 93403, 6560 (use Am27S02A/02); for 74S189, 6561, DM8599 (use Am27S03A/03)

## GENERAL DESCRIPTION

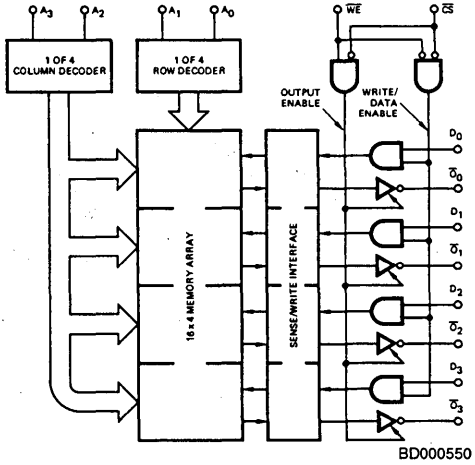
The Am27S02/02A and Am27S03/03A are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am27S02/02A) or three-state outputs (Am27S03/03A). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs $D_0$ to $D_3$ is written into the addressed memory word and preconditions the output circuitry so that correct data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

## BLOCK DIAGRAM




BD000550

## MODE SELECT TABLE

| Input | | Data Output Status $\overline{O}_0 - \overline{O}_3$ | Mode |
|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | | |
| L | L | Output Disabled | Write |
| L | H | Selected Word (Inverted) | Read |
| H | X | Output Disabled | Deselect |

H = HIGH
L = LOW
X = Don't Care

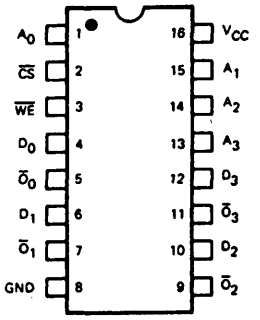
## PRODUCT SELECTOR GUIDE

| Access Time | 25ns | 30ns | 35ns | 50ns | 55ns | 65ns |
|---|---|---|---|---|---|---|
| Temperature Range | C | M | C | M | C | M |
| Open Collector | Am27S02A | Am27S02A | Am27S02 | Am27S02 | Am27LS02 | Am27LS02 |
| Three-State | Am27S03A | Am27S03A | Am27S03 | Am27S03 | Am27LS03 | Am27LS03 |

02191C

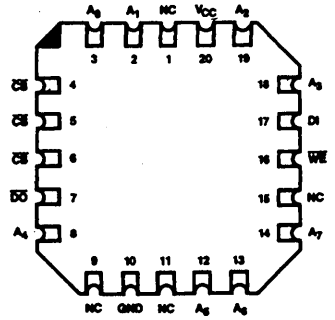
## CONNECTION DIAGRAM
### Top View

**DIP**




CD000830

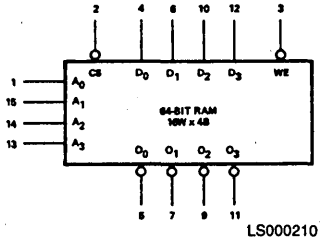
**L-20-2**




CD000890

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000210

## ORDERING INFORMATION

**Am27S02 A P C B**

- **B** — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- **C** — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **P** — Package
  - D – 16-pin ceramic DIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
- **A** — Speed Select
  - See Product Selector Guide
- **Am27S02** — Device Type
  - *Output Configuration*
  - See Product Selector Guide

| Valid Combinations | |
|---|---|
| Am27S02<br>Am27LS02<br>Am27S03<br>Am27LS03 | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |
| Am27S02A<br>Am27S03A | PC, PCB,<br>DC, DCB,<br>DM, DMB |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

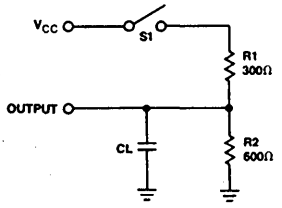
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameters | Test Conditions | | | 27S02/3 Min | 27S02/3 Typ | 27S02/3 Max | 27LS02/3 Min | 27LS02/3 Typ | 27LS02/3 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −5.2mA | COM'L | 2.4 | 3.2 | | 2.4 | 3.6 | | Volts |
| | | | $I_{OH}$ = −2.0mA | MIL | | | | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA | | | 350 | 450 | | 280 | 450 | mV |
| | | | $I_{OL}$ = 20mA | | | 380 | 500 | | 310 | 500 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for All Inputs (Note 3) | | | 2.0 | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed Input Logical LOW Voltage for All Inputs (Note 3) | | | | | 0.8 | | | 0.8 | |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.40V | $\overline{WE}$, $D_0$–$D_3$, $A_0$–$A_3$ | | | −15 | −250 | | −15 | −250 | µA |
| | | | $\overline{CS}$ | | | −30 | −250 | | −30 | −250 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.4V | | | | 0 | 10 | | 0 | 10 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −45 | −90 | −20 | −45 | −90 | mA |
| $I_{CC}$ | Power Supply Current | All Inputs = GND $V_{CC}$ = MAX | COM'L | | | 75 | 100 | | 30 | 35 | |
| | | | MIL | | | 75 | 105 | | 30 | 38 | |
| $V_{CL}$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −0.85 | −1.2 | | −0.85 | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{OUT}$ = 2.4V | Am27S02A/03A Am27S02/03 | | | 0 | 40 | | 0 | 40 | µA |
| | | $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{OUT}$ = 0.4V, $V_{CC}$ = MAX | (Note 2) | | −40 | 0 | | −40 | 0 | | |

Notes:

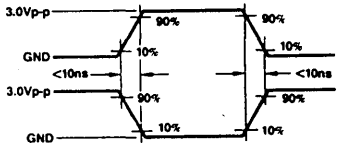
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

## SWITCHING TEST CIRCUIT



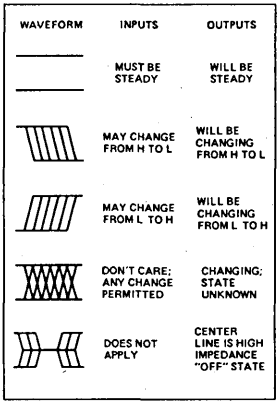

TC000170

## SWITCHING TEST WAVEFORM




TW000030

## KEY TO THE SWITCHING WAVEFORMS




KS000010

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified

| No. | Symbol | Description | Am27S02/3 A C devices Min | Am27S02/3 A C devices Max | Am27S02/3 A M devices Min | Am27S02/3 A M devices Max | Am27S02/3 STD C devices Min | Am27S02/3 STD C devices Max | Am27S02/3 STD M devices Min | Am27S02/3 STD M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output | | 25 | | 30 | | 35 | | 50 | ns |
| 2 | $t_{PHL}(A)$ | | | | | | | | | | |
| 3 | $t_{PZH}(\overline{CS})$ | Delay from Chip Select (LOW) to Active Output and Correct Data | | 15 | | 20 | | 17 | | 25 | ns |
| 4 | $t_{PZL}(\overline{CS})$ | | | | | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery- See Note 1) | | 20 | | 25 | | 35 | | 40 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | | | | | |
| 7 | $t_s(A)$ | Setup Time Address (Prior to Initiation of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 8 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 9 | $t_s(DI)$ | Setup Time Data Input (Prior to Termination of Write) | 20 | | 25 | | 25 | | 25 | | ns |
| 10 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 11 | $t_{pw}(\overline{WE})$ | MIN Write Enable Pulse Width to Insure Write | 20 | | 25 | | 25 | | 25 | | ns |
| 12 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select (HIGH) to inactive Output (HI-Z) | | 15 | | 20 | | 17 | | 25 | ns |
| 13 | $t_{PLZ}(\overline{CS})$ | | | | | | | | | | |
| 14 | $t_{PLZ}(\overline{WE})$ | Delay from Write Enable (LOW) to Inactive Output (HI-Z) | | 20 | | 25 | | 25 | | 35 | ns |
| 15 | $t_{PHZ}(\overline{WE})$ | | | | | | | | | | |

## SWITCHING CHARACTERISTICS (Cont.)

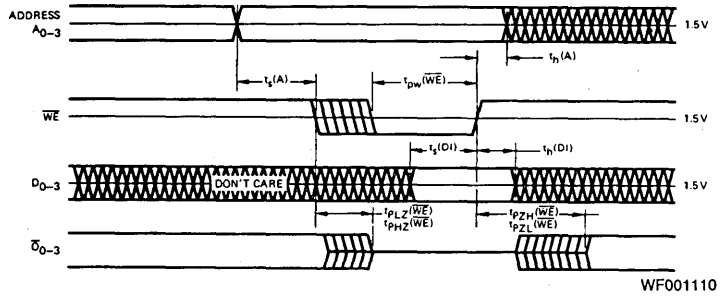
| No. | Symbol | Description | Am27LS02/3 C devices Min | Am27LS02/3 C devices Max | Am27LS02/3 M devices Min | Am27LS02/3 M devices Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output | | 55 | | 65 | ns |
| 2 | $t_{PHL}(A)$ | | | | | | |
| 3 | $t_{PZH}(\overline{CS})$ | Delay from Chip Select to Active Output and Correct Data | | 30 | | 35 | ns |
| 4 | $t_{PZL}(\overline{CS})$ | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery - See Note 2) | | 30 | | 35 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | |
| 7 | $t_s(A)$ | Setup Time Address (Prior to Initiation of Write) | 0 | | 0 | | ns |
| 8 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 0 | | 0 | | ns |
| 9 | $t_s(DI)$ | Setup Time Data Input (Prior to Termination of Write) | 45 | | 55 | | ns |
| 10 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 0 | | 0 | | ns |
| 11 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to Insure Write | 45 | | 55 | | ns |
| 12 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select to Inactive Output (HI-Z) | | 30 | | 35 | ns |
| 13 | $t_{PLZ}(\overline{CS})$ | | | | | | |
| 14 | $t_{PLZ}(\overline{WE})$ | Delay from Write Enable (LOW) to Inactive Output (HI-Z) | | 30 | | 35 | ns |
| 15 | $t_{PHZ}(\overline{WE})$ | | | | | | |

Notes:

1. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with $S_1$ closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output ($D_{OUT}$), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.
4. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with $S_1$ open, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed, $C_L = 30pF$ and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with $S_1$ open and $C_L \leq 5pF$ and are measured between the 1.5V level on the input to the $V_{OH}$=mNg500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with $S_1$ closed and $C_L \leq 5pF$ and are measured between the 1.5V level on the input and the $V_{OL}$+500mV level on the output.

## SWITCHING WAVEFORMS

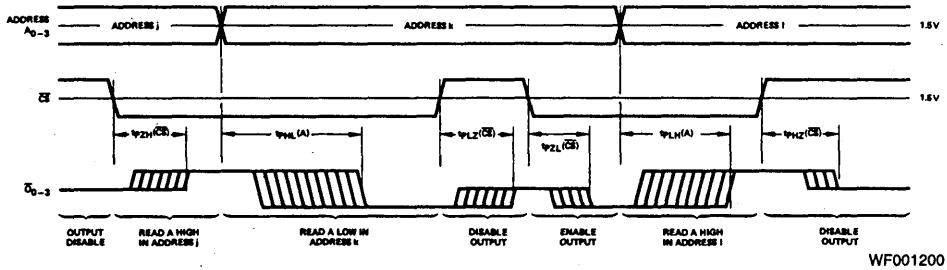
### WRITE MODE




Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$min must be allowed before the address may be changed again. The output will be inactive (floating for the Am27S03A/03) while the write enable is ($\overline{WE}$) LOW.

## SWITCHING WAVEFORMS (Cont.)

### READ MODE




WF001200

Switching delays from address and chip select inputs to the data output. For the Am27S03A/03 disabled output is "OFF", represented by a single center line. For the Am27S02A/02, a disabled output is HIGH.

# Am27LS00/01 Series

256-Bit Low-Power Schottky Bipolar RAM

## DISTINCTIVE CHARACTERISTICS

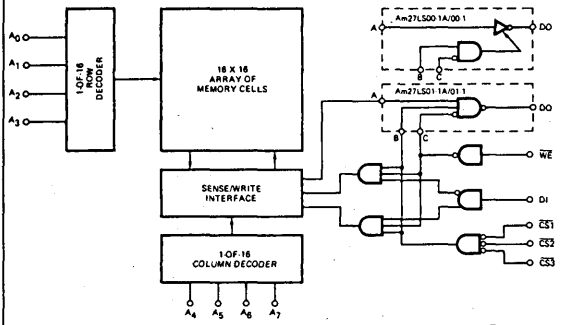
- High-Speed
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate the write recovery glitch
- Available with three-state outputs or with open collector outputs
- Both inverting and non-inverting versions available.

## GENERAL DESCRIPTION

The Am27LS00/01 family is comprised of fully decoded bipolar random access memories for use in high-speed buffer memories. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am27LS00 devices) or open collector output (Am27LS01 devices). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output of the -1 device is active and inverts the value of DI (White Transparent Operation). The other devices disable the output during the period $\overline{WE}$ is low. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

## BLOCK DIAGRAM




BD000590

## MODE SELECT TABLE

| Input | | | Data Output Status $\overline{DO}$ ($t_{n+1}$) | Mode |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | DI | | |
| H | X | X | Inverted/Disabled* | No Selection |
| L | L | L | Output Disabled | Write '0' |
| L | L | H | Output Disabled | Write '1' |
| L | H | X | Selected Bit (Inverted) | Read |

H = HIGH
L = LOW
X = Don't Care

*Inverted = -1 Devices
Disabled = All Other Devices

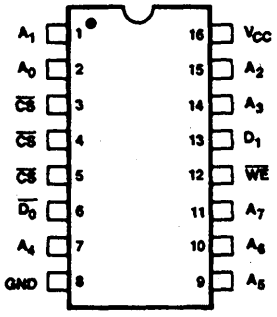
## PRODUCT SELECTOR GUIDE

| Access Time | | 35ns | 45ns | | 55ns |
|---|---|---|---|---|---|
| Temperature Range | | C | C | M | M |
| Open Collector | STD | Am27LS01A | Am27LS01 | Am27LS01A | Am27LS01 |
| | Write Transparent | Am27LS01-1A | Am27LS01-1 | Am27LS01-1A | Am27LS01-1A |
| Three-State | STD | Am27LS00A | Am27LS00 | Am27LS00A | Am27LS00 |
| | Write Transparent | Am27LS00-1A | Am27LS00-1 | Am27LS00-1A | Am27LS00-1 |

03233C

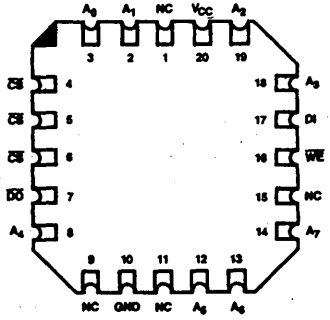
## CONNECTION DIAGRAM
Top View

DIP




CD000880

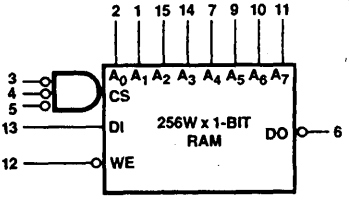
Chip-Pak™




CD000890

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000200

## ORDERING INFORMATION

**Am27LS00 1A D C B**

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- C — Temperature: C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 16-pin ceramic DIP; F – 16-pin flatpak; L – 20-pin leadless chip carrier; P – 16-pin plastic DIP
- 1A — Speed Select: See Product Selector Guide
- Am27LS00 — Device Type

Three state: Am27LS00, Am27LS00A, Am27LS00-1, Am27LS00-1A

Open collector: Am27LS01, Am27LS01A, Am27LS01-1, Am27LS01-1A

| Valid Combinations | |
|---|---|
| Am27LS00 | PC, |
| Am27LS00A | DC, DCB, |
| Am27LS00-1 | LC, LCB, |
| Am27LS00-1A | DM, DMB, |
| Am27LS01 | FM, FMB, |
| Am27LS01A | LM, LMB |
| Am27LS01-1 | |
| Am27LS01-1A | |

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to ground potential
(Pin16 to Pin8) continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +$V_{CC}$
Output Current, into Outputs ..... 30mA
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

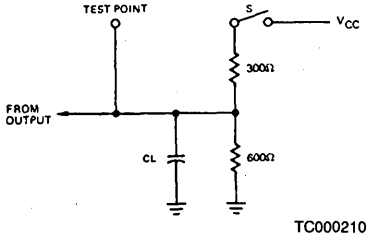
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −5.2mA | COM'L | 2.4 | 3.2 | | Volts |
| | | | $I_{OH}$ = −2.0mA | MIL | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA | | | 0.3 | 0.45 | Volts |
| $V_{IH}$ | Input HIGH Level | Guaranteed input logical HIGH voltage for all inputs (Note 3) | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed input logical LOW voltage for all inputs (Note 3) | | | | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.40V | | | | 0.030 | 0.25 | mA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.7V | | | | < 1 | 20 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V | | | −20 | −30 | −60 | mA |
| $I_{CC}$ | Power Supply Current | All inputs = GND, $V_{CC}$ = MAX | | "A" version | | 80 | 115 | mA |
| | | | | Standard | | 55 | 70 | |
| $V_{CL}$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −0.850 | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{\overline{CS}}$ = $V_{IH}$ or $V_{\overline{WE}}$ = $V_{IL}$, $V_{OUT}$ = 2.4V | | | | 0 | 30 | µA |
| | | $V_{\overline{CS}}$ = $V_{IH}$ or $V_{\overline{WE}}$ = $V_{IL}$, $V_{OUT}$ = 0.4V, $V_{CC}$ = MAX | | (Note 2) | −30 | 0 | | µA |

Notes:

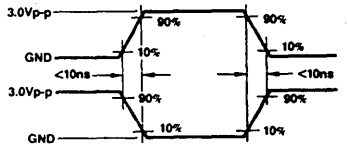
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## SWITCHING TEST CIRCUIT



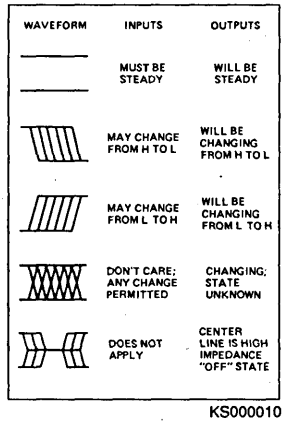

TC000210

## SWITCHING TEST WAVEFORM




TW000030

## KEY TO SWITCHING WAVEFORMS




KS000010

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

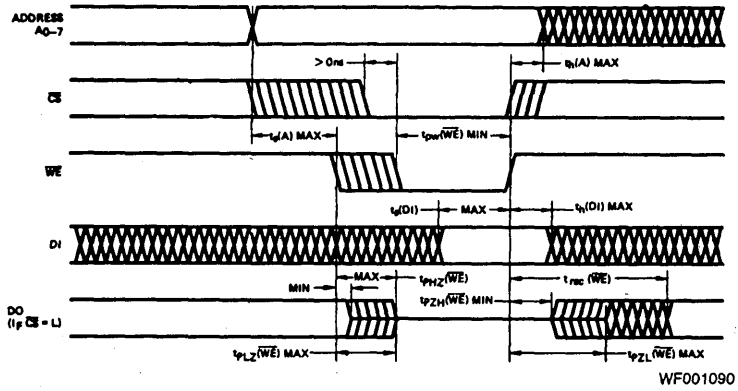
| No. | Symbol | Description | Am27LS00A/01A family | | | | Am27S00/01 family | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | C devices | | M devices | | C devices | | M devices | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{PLH}$(A) | Delay from Address to Output | | 35 | | 45 | | 45 | | 55 | ns |
| 2 | $t_{PHL}$(A) | | | | | | | | | | |
| 3 | $t_{PZH}(\overline{CS})$ | Delay from Chip Select (LOW) to to Active Output and Correct Data | | 25 | | 25 | | 25 | | 30 | ns |
| 4 | $t_{PZL}(\overline{CS})$ | | | | | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data | 5 | | 5 | | 5 | | 5 | | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | | | | | |
| 7 | $t_{rec}(\overline{WE})$ | Delay from Write Enable (HIGH) to Correct Output Data | | 35 | | 45 | | 45 | | 55 | ns |
| 8 | $t_s$(A) | Setup Time Address (Prior to Initiation of Write) | | 0 | | 5 | | 0 | | 5 | ns |
| 9 | $t_h$(A) | Hold Time Address (After Termination of Write) | | 0 | | 5 | | 0 | | 5 | ns |
| 10 | $t_s$(DI) | Setup Time Data Input (Prior to Termination of Write) | | 25 | | 30 | | 30 | | 55 | ns |
| 11 | $t_h$(DI) | Hold Time Data Input (After Termination of Write) | | 5 | | 5 | | 0 | | 5 | ns |
| 12 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to Insure Write | 25 | | 30 | | 30 | | 35 | | ns |
| 13 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select (HIGH) to Inactive Output (HI-Z) | | 25 | | 25 | | 25 | | 30 | ns |
| 14 | $t_{PLZ}(\overline{CS})$ | | | | | | | | | | |
| 15 | $t_{PLZ}(\overline{WE})$ | Delay from Write Enable (LOW) to Inactive Output (HI-Z) (Note 6) | | 30 | | 40 | | 30 | | 40 | ns |
| 16 | $t_{PHZ}(\overline{WE})$ | | | | | | | | | | |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is termilneted. (No write recovery glitch.)
3. $t_{PLH}$(A) and $t_{PHL}$(A) are tested with S closed and $C_L$ = 50 pF with both input and output timing referenced to 1.5V.
4. For open collector, all delays from write Enable($\overline{WE}$) or Chip Select($\overline{CS}$) inputs to the Data Output($D_{OUT}$), $t_{PLZ}(\overline{WE})$, $t_{PZL}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed and $C_L$ = 50pF and with both the input and output timimg referenced to 1.5V.
5. For 3-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with S open, $C_L$ = 50pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with S closed, $C_L$ = 50 pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with S open and $C_L \leq$ 5pF and are measured between the 1.5V level on the input and the $V_{OL}$+500mV level on the output.
6. Does not apply to -1 devices.

## SWITCHING WAVEFORMS

### WRITE MODE

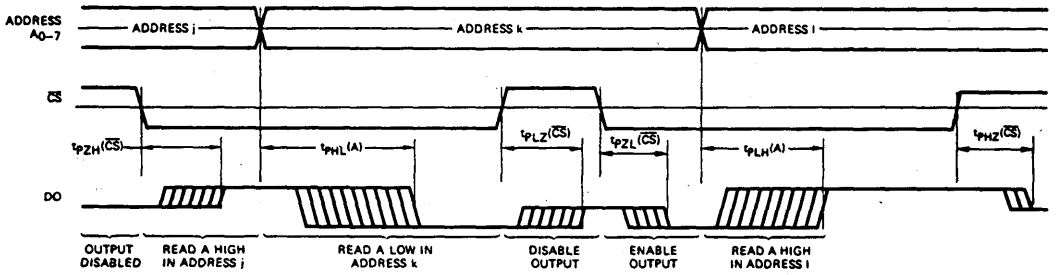



WF001090

Write Cycle Timing. The cycle is initiated by an address change. After $t_s$(A) max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h$(A) max must be allowed before the address may be changed again. The output will be inactive (floating for the Am27LS00-1A/00-1) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.



### READ MODE




WF001100

Switching delays from address and chip select inputs to the data output. For the Am27LS00-1A/00-1 disabled output is "OFF," represented by a single center line. For the Am27LS01-1A/01-1, a disabled output is HIGH.

# Am93412/422 Family

256 x 4-bit TTL Bipolar IMOX™ RAM

## DISTINCTIVE CHARACTERISTICS

- High-speed
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with 3-state outputs or with open collector outputs
- Power dissipation decreases with increasing temperature

## GENERAL DESCRIPTION

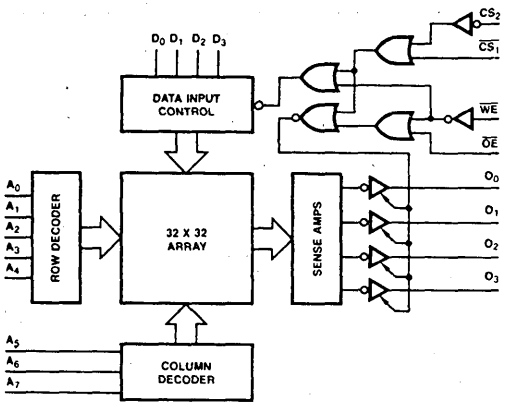
The Am93412/22 family is comprised of 1024-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in high-speed control and buffer memory applications. Each memory is organized as a fully decoded 256-word memory of four bits per word. Easy memory expansion is provided by an active LOW chip select one ($\overline{CS_1}$) and active HIGH chip select two ($CS_2$) as well as open collector OR tieable outputs (Am93412) or 3-state outputs (Am93422).

An active LOW write line ($\overline{WE}$) controls the writing/reading operation of the memory. When the chip select one ($\overline{CS_1}$) and write line ($\overline{WE}$) are LOW and chip select two ($CS_2$) is HIGH, the information on data inputs ($D_0$ through $D_3$) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select one ($\overline{CS_1}$) LOW and the chip select two ($CS_2$) HIGH and the write line ($\overline{WE}$) HIGH and with the output enable ($\overline{OE}$) LOW. The information stored in the addressed word is read out on the noninverting outputs ($O_0$ through $O_3$).

The outputs of the memory go to an inactive high-impedance state whenever chip select one ($\overline{CS_1}$) is HIGH, chip select two ($CS_2$) is LOW, output enable ($\overline{OE}$) is HIGH, or during the writing operation when write enable ($\overline{WE}$) is LOW.

## BLOCK DIAGRAM




BD000600

## MODE SELECT TABLE

| Input | | | | | Output | |
|---|---|---|---|---|---|---|
| $CS_2$ | $\overline{CS_1}$ | $\overline{WE}$ | $\overline{OE}$ | $D_n$ | $O_n$ | Mode |
| L | X | X | X | X | *HIGH Z | Not Select |
| X | H | X | X | X | *HIGH Z | Not Select |
| H | L | H | H | X | *HIGH Z | Output Disable |
| H | L | H | L | X | Selected Data | Read Data |
| H | L | L | X | L | *HIGH Z | Write "0" |
| H | L | L | X | H | *HIGH Z | Write "1" |

H = HIGH L = LOW X = Don't Care

*High Z implies outputs are disabled or off. This condition is defined as a high impedance state for the Am93422A/422 and as output high level for the Am93412A/412.

## PRODUCT SELECTOR GUIDE

| Access Time | 35ns | 45ns | | 55ns | 60ns | | 75ns |
|---|---|---|---|---|---|---|---|
| Temperature Range | C | C | M | M | C | M | M |
| Open Collector | Am93412A | Am93412<br>Am93L412A | Am93412A | Am93L412A | Am93L412 | Am93412 | Am93L412 |
| Three-State | Am93422A | Am93422<br>Am93L422A | Am93422A | Am93L422A | Am93L422 | Am93422 | Am93L422 |

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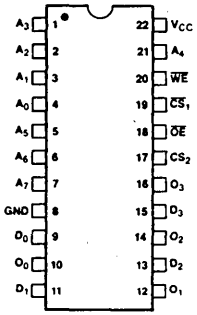
03080B

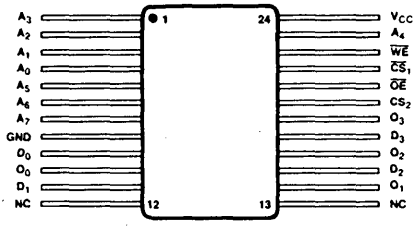
## CONNECTION DIAGRAM
Top View

**DIP**



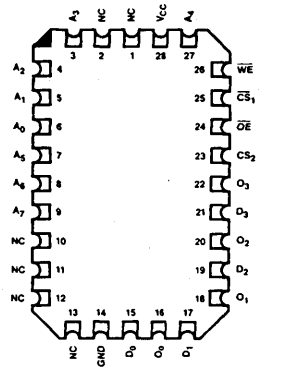

CD000610

**Flat Package**




CD001000

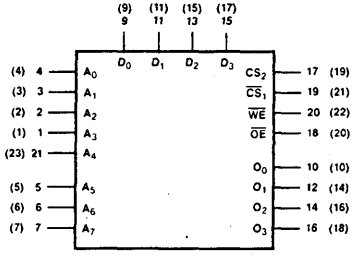
**Chip-pak™ L-28-2**




CD000620

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000220

## ORDERING INFORMATION

**Am93422 A P C B**

- B — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 22-pin ceramic DIP
  - F – 24-pin flatpak
  - L – 28-pin leadless chip carrier
  - P – 22-pin plastic DIP
- A — Speed Select
  - See Product Selector Guide
- Am93422 — Device Type
  - Am93412 family – Open Collector
  - Am93422 family – Three state

| Valid Combinations | |
|---|---|
| Am93412 | PC, PCB, |
| Am93412A | DC, DCB, |
| Am93L412 | LC, LCB, |
| Am93L412A | DM, DMB, |
| Am93422 | FM, FMB, |
| Am93422A | LM, LMB |
| Am93L422 | |
| Am93L422A | |

Chip-pak is a trademark of Advanced Micro Device, Inc.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +$V_{CC}$ max
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

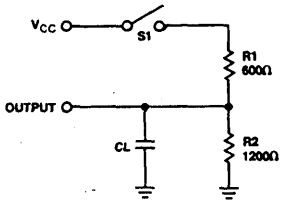
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −5.2mA | | 2.4 | 3.6 | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 8.0mA | | | 0.350 | 0.45 | Volts |
| $V_{IH}$ | Input HIGH Level (Note 3) | Guaranteed input logical HIGH voltage for all inputs | | | 2.1 | 1.6 | | Volts |
| $V_{IL}$ | Input LOW Level (Note 3) | Guaranteed input logical LOW voltage for all inputs | | | | 1.5 | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.40V | | | | −100 | −300 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 4.5V | | | | 1 | 40 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | | | −90 | mA |
| $I_{CC}$ | Power Supply Current | ALL inputs = GND $V_{CC}$ = MAX | $T_A$ = 70°C | STD devices | | 100 | 130 | mA |
| | | | | L devices | | 55 | 75 | |
| | | | $T_A$ = 0°C | STD devices | | | 155 | |
| | | | | L devices | | | 80 | |
| | | | $T_A$ = −55°C | STD devices | | | 170 | |
| | | | | L devices | | | 90 | |
| $V_{CL}$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −10 mA | | | | −0.850 | −1.5 | Volts |
| $I_{CEX}$ | Output Leakage Current | $V_{OUT}$ = 2.4V | Am 93422A/422 | | | 0 | 50 | µA |
| | | $V_{OUT}$ = 0.5V, $V_{CC}$ = MAX | Am93422A/422 | | −50 | 0 | | |
| | | $V_{OUT}$ = 4.5V | Am 93412A/412 | | | 0 | 100 | |
| $C_{IN}$ | Input Pin Capacitance | See Note 5 | | | | 4 | | pF |
| $C_{OUT}$ | Output Pin Capacitance | See Note 5 | | | | 7 | | pF |

Notes:

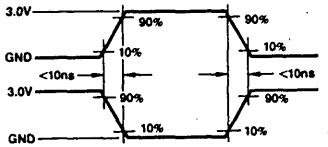
1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Applies only to devices with three-state outputs (Am93422 family)
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
5. Input and output capacitance measured on a sample basis @ f = 1.0MHz.

## SWITCHING TEST CIRCUIT



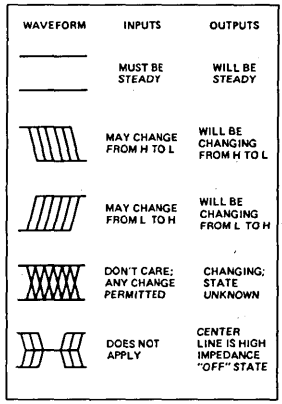

TC000200

## SWITCHING TEST WAVEFORMS




TW000040

## KEY TO SWITCHING WAVEFORMS




KS000010

3

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am93412A/422A C devices Min | Am93412A/422A C devices Max | Am93412A/422A M devices Min | Am93412A/422A M devices Max | Am93412/422 C devices Min | Am93412/422 C devices Max | Am93412/422 M devices Min | Am93412/422 M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}$(A)(Note 1) | Delay from Address to Output (Address Access Time) | | 35 | | 45 | | 45 | | 60 | ns |
| 2 | $t_{PHL}$(A)(Note 1) | | | | | | | | | | |
| 3 | $t_{PZH}(\overline{CS_1},CS_2)$ | Delay from Chip Select to Active Output and Correct Data | | 25 | | 35 | | 30 | | 45 | ns |
| 4 | $t_{PZL}(\overline{CS_1},CS_2)$ | | | | | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable to Active Output and Correct Data (Write Recovery) | | 25 | | 40 | | 40 | | 50 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | | | | | |
| 7 | $t_{PZH}(\overline{OE})$ | Delay from Output Enable to Active Output and Correct Data | | 25 | | 35 | | 30 | | 45 | ns |
| 8 | $t_{PZL}(\overline{OE})$ | | | | | | | | | | |
| 9 | $t_s$(A) | Setup Time Address (Prior to Initiation of Write) | 5 | | 5 | | 10 | | 10 | | ns |
| 10 | $t_h$(A) | Hold Time Address (After Termination of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 11 | $t_s$(DI) | Setup Time Data Input (Prior to Initiation of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 12 | $t_h$(DI) | Hold Time Data Input (After Termination of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 13 | $t_s(\overline{CS_1},CS_2)$ | Setup Time Chip Select (Prior to Initiation of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 14 | $t_h(\overline{CS_1},CS_2)$ | Hold Time Chip Select (After Termination of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 15 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to Insure Write | 20 | | 35 | | 30 | | 40 | | ns |
| 16 | $t_{PHZ}(\overline{CS_1},CS_2)$ | Delay from Chip Select to Inactive Output (HIGH-Z) | | 30 | | 35 | | 30 | | 45 | ns |
| 17 | $t_{PLZ}(\overline{CS_1},CS_2)$ | | | | | | | | | | |
| 18 | $t_{PHZ}(\overline{WE})$ | Delay from Write Enable to Inactive Output (HIGH-Z) | | 30 | | 40 | | 35 | | 45 | ns |
| 19 | $t_{PLZ}(\overline{WE})$ | | | | | | | | | | |
| 20 | $t_{PHZ}(\overline{OE})$ | Delay from Output Enable to Inactive Output (HIGH-Z) | | 30 | | 35 | | 30 | | 45 | ns |
| 21 | $t_{PLZ}(\overline{OE})$ | | | | | | | | | | |

## SWITCHING CHARACTERISTICS (Cont.)

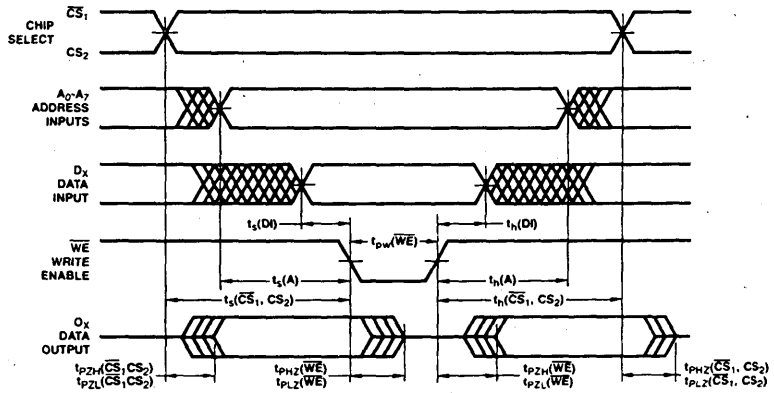
| No. | Symbol | Description | Am93L412A/422A C devices Min | Am93L412A/422A C devices Max | Am93L412A/422A M devices Min | Am93L412A/422A M devices Max | Am93L412/422 C devices Min | Am93L412/422 C devices Max | Am93L412/422 M devices Min | Am93L412/422 M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}$(A)(Note 1) | Delay from Address to Output (Address Access Time) | | 45 | | 55 | | 60 | | 75 | ns |
| 2 | $t_{PHL}$(A)(Note 1) | | | | | | | | | | |
| 3 | $t_{PZH}(\overline{CS_1},CS_2)$ | Delay from Chip Select to Active Output and Correct Data | | 30 | | 40 | | 35 | | 45 | ns |
| 4 | $t_{PZL}(\overline{CS_1},CS_2)$ | | | | | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable to Active Output and Correct Data (Write Recovery) | | 40 | | 45 | | 45 | | 50 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | | | | | |
| 7 | $t_{pzh}(\overline{OE})$ | Delay from Output Enable to Active Output and Correct Data | | 30 | | 40 | | 35 | | 45 | ns |
| 8 | $t_{PZL}(\overline{OE})$ | | | | | | | | | | |
| 9 | $t_s$(A) | Setup Time Address (Prior to Initiation of Write) | 5 | | 10 | | 10 | | 10 | | ns |
| 10 | $t_h$(A) | Hold Time Address (After Termination of Write) | 5 | | 5 | | 5 | | 10 | | ns |
| 11 | $t_s$(DI) | Setup Time Data Input (Prior to Initiation of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 12 | $t_h$(DI) | Hold Time Data Input (After Termination of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 13 | $t_s(\overline{CS_1},CS_2)$ | Setup Time Chip Select (Prior to Initiation of Write) | 5 | | 5 | | 5 | | 5 | | ns |
| 14 | $t_h(\overline{CS_1},CS_2)$ | Hold Time Chip Select (After Termination of Write) | 5 | | 5 | | 5 | | 10 | | ns |
| 15 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to insure Write | 35 | | 40 | | 45 | | 55 | | ns |
| 16 | $t_{PHZ}(\overline{CS_1},CS_2)$ | Delay from Chip Select to Inactive Output (HIGH-Z) | | 30 | | 40 | | 35 | | 45 | ns |
| 17 | $t_{PLZ}(\overline{CS_1},CS_2)$ | | | | | | | | | | |
| 18 | $t_{PHZ}(\overline{WE})$ | Delay from Write Enable to Inactive Output (HIGH-Z) | | 35 | | 40 | | 40 | | 45 | ns |
| 19 | $t_{PLZ}(\overline{WE})$ | | | | | | | | | | |
| 20 | $t_{PHZ}(\overline{OE})$ | Delay from Output Enable to Inactive Output (HIGH-Z) | | 30 | | 40 | | 35 | | 45 | ns |
| 21 | $t_{PLZ}(\overline{OE})$ | | | | | | | | | | |

Notes:

1. $t_{PLH}$(A) and $t_{PHL}$(A) are tested with $S_1$ closed and $C_L$ = 15pF with both input and output timing referenced to 1.5V.
2. For open collector devices, all delays from Write Enable ($\overline{WE}$) or selects ($\overline{CS_1}$, $CS_2$,$\overline{OE}$) inputs to the Data Output ($O_0 - O_3$) ($t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$, $t_{PLZ}(\overline{OE})$ $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}, CS_2)$ and $t_{PZL}(\overline{OE})$) are measured with $S_1$ closed and $C_L$ = 15pF; and with both the input and output timing referenced to 1.5V.
3. For 3-state output devices, $t_{PZH}(\overline{WE})$, $t_{PZH}(\overline{CS_1}, CS_2)$ and $t_{PZH}(\overline{OE})$ are measured with $S_1$ open, $C_L$ = 15pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$, $t_{PZL}(\overline{CS_1}\ CS_2)$ and $t_{PZL}(\overline{OE})$ are measured with $S_1$ closed, $C_L$ = 15pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$, $t_{PHZ}(\overline{CS_1}, CS_2)$ and $t_{PHZ}(\overline{OE})$ are measured with $S_1$ open and $C_L \leqslant$ 5pF and are measured between the 1.5V level on the input to the $V_{OH}$ – 500mV level on the output. $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS_1}, CS_2)$ and $t_{PLZ}(\overline{OE})$ are measured with $S_1$ closed and $C_L \leqslant$ 5pF and are measured between the 1.5V level on the input and the $V_{OL}$ + 500mV level on the output.

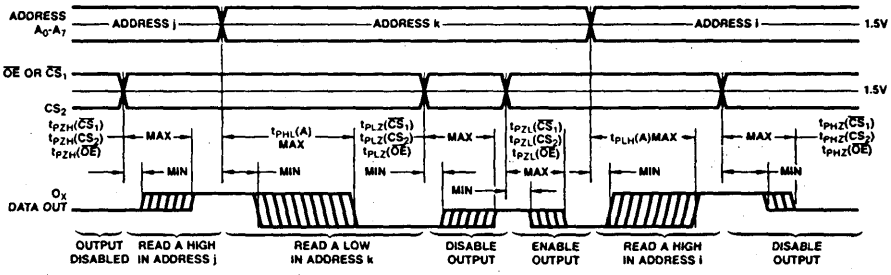
## SWITCHING WAVEFORMS

### WRITE MODE (WITH $\overline{OE}$ = LOW)




WF001120

### READ MODE




WF001130

Switching delays form address input, output enable input and the chip select inputs to the data output. For the Am93422A/422 disabled output is "OFF", represented by a single center line. For the Am93412A/412, a disabled output is HIGH.

# Am10415

1024 x 1 IMOX™ ECL Bipolar RAM

## DISTINCTIVE CHARACTERISTICS

- Fast access time (10ns typ.) — improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL — no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

## GENERAL DESCRIPTION

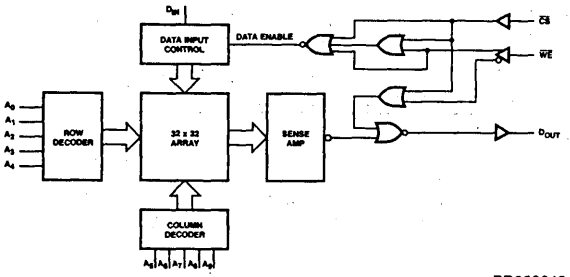
The Am10415SA, Am10415A and Am10415 are fully decoded 1024-bit ECL RAMs organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input ($D_{IN}$) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output ($D_{OUT}$).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

## BLOCK DIAGRAM




BD000640

## MODE SELECT TABLE

| Input | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | $D_{OUT}$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

| Access Time | 15ns | 20ns | 20ns | 25ns | 35ns | 40ns |
|---|---|---|---|---|---|---|
| Temperature Range | C | M | C | M | C | M |
| Part Number | Am10415SA | Am10415SA | Am10415A | Am10415A | Am10415 | Am10415 |

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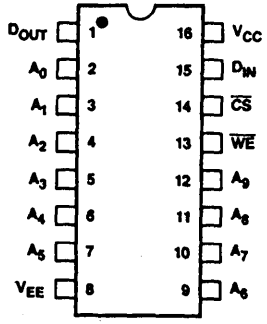
01419B

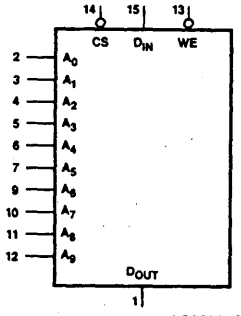
## CONNECTION DIAGRAM
Top View




CD000920

TO BE DETERMINED

## LOGIC SYMBOL




LS000240



## ORDERING INFORMATION

Am10415 SA P C B

- B — Burn-in Option
  B suffix denotes 160 hour burn-in.
- C — Temperature
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- P — Package
  D – 16-pin ceramic DIP
  F – 16-pin flatpak
  L – 20-pin leadless chip carrier
  P – 16-pin plastic DIP
- SA — Speed Select
  See Product Selector Guide
- Am10415 — Device Type
  1024 x 1 ECL Bipolar RAM

| Valid Combinations | |
|---|---|
| Am10415<br>Am10415A<br>Am10415SA | PC, PCB,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
$V_{EE}$ Pin Potential to GND Pin ..... −7.0V to +0.5V
Input Voltage (DC) ..... $V_{EE}$ to +0.5V
Output Current (DC Output HIGH) ..... −30mA to +0.1mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... −5.46V to −4.94V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... −5.72V to −4.68V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS (Commercial)

| Symbol | Parameter | Test Conditions | | | B (Note 3) | Typ (Note 1) | A (Note 3) | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage HIGH | $V_{IN} = V_{IHA}$ or $V_{ILB}$ | Loading is 50Ω to −2.0V | $T_A = 0°C$ | −1000 | | −840 | mV |
| | | | | $T_A = +25°C$ | −960 | | −810 | |
| | | | | $T_A = +75°C$ | −900 | | −720 | |
| $V_{OL}$ | Output Voltage LOW | | | $T_A = 0°C$ | −1870 | | −1665 | mV |
| | | | | $T_A = +25°C$ | −1850 | | −1650 | |
| | | | | $T_A = +75°C$ | −1830 | | −1625 | |
| $V_{OHC}$ | Output Voltage HIGH | $V_{IN} = V_{IHB}$ or $V_{ILA}$ | | $T_A = 0°C$ | −1020 | | | mV |
| | | | | $T_A = +25°C$ | −980 | | | |
| | | | | $T_A = +75°C$ | −920 | | | |
| $V_{OLC}$ | Output Voltage LOW | | | $T_A = 0°C$ | | | −1645 | mV |
| | | | | $T_A = +25°C$ | | | −1630 | |
| | | | | $T_A = +75°C$ | | | −1605 | |
| $V_{IH}$ | Input Voltage HIGH | Guaranteed Input Voltage HIGH for All Inputs (Note 4) | | $T_A = 0°C$ | −1145 | | −840 | mV |
| | | | | $T_A = +25°C$ | −1105 | | −810 | |
| | | | | $T_A = +75°C$ | −1045 | | −720 | |
| $V_{IL}$ | Input Voltage LOW | Guaranteed Input Voltage LOW for All Inputs (Note 4) | | $T_A = 0°C$ | −1870 | | −1490 | mV |
| | | | | $T_A = +25°C$ | −1850 | | −1475 | |
| | | | | $T_A = +75°C$ | −1830 | | −1450 | |
| $I_{IH}$ | Input Current HIGH | $V_{IN} = V_{IHA}$ | | $T_A = 0$ to $+75°C$ | | | 220 | µA |
| $I_{IL}$ | Input Current LOW<br>Chip Select ($\overline{CS}$)<br>All Other Inputs | $V_{IN} = V_{ILB}$ | | $T_A = +25°C$ | 0.5<br>−50 | | 170 | mA |
| $I_{EE}$ | Power Supply Current (Pin 8) | All Inputs and Outputs Open | | $T_A = 0°C$ | −150 | −105 | | mA |
| | | | | $T_A = +75°C$ | | −90 | | |

Notes:

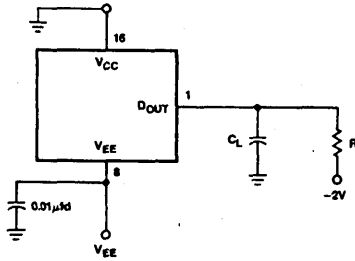
1. Typical values are at $V_{EE} = -5.2V$, $T_A = 25°C$ and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical thermal resistance values of the package are:
   $\theta_{JA}$ (Junction to Ambient) = 90°C/Watt (still air)
   $\theta_{JA}$ (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   $\theta_{JC}$ (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## DC CHARACTERISTICS (Military)

| Symbol | Parameter | Test Conditions | | | B (Note 3) | Typ (Note 1) | A (Note 3) | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage HIGH | $V_{IN} = V_{IHA}$ or $V_{ILB}$ | Loading is 50Ω to −2.0V | $T_A = -55°C$ | −1070 | | −860 | mV |
| | | | | $T_A = +125°C$ | −860 | | −650 | |
| $V_{OL}$ | Output Voltage LOW | | | $T_A = -55°C$ | −1900 | | −1690 | |
| | | | | $T_A = +125°C$ | −1800 | | −1570 | mV |
| $V_{OHC}$ | Output Voltage HIGH | $V_{IN} = V_{IHB}$ or $V_{ILA}$ | | $T_A = -55°C$ | −1090 | | | |
| | | | | $T_A = +125°C$ | −880 | | | |
| $V_{OLC}$ | Output Voltage LOW | | | $T_A = -55°C$ | | | −1670 | mV |
| | | | | $T_A = +125°C$ | | | −1550 | |
| $V_{IH}$ | Input Voltage HIGH | Guaranteed Input Voltage HIGH for All Inputs (Note 4) | | $T_A = -55°C$ | −1215 | | −860 | mV |
| | | | | $T_A = +125°C$ | −1005 | | −650 | |
| $V_{IL}$ | Input Voltage LOW | Guaranteed Input Voltage LOW for All Inputs (Note 4) | | $T_A = -55°C$ | −1900 | | −1515 | mV |
| | | | | $T_A = +125°C$ | −1800 | | −1395 | |
| $I_{IH}$ | Input Current HIGH | $V_{IN} = V_{IHA}$ | | $T_A = -55°C$ | | | 250 | µA |
| $I_{IL}$ | Input Current LOW<br>Chip Select ($\overline{CS}$)<br>All Other Inputs | $V_{IN} = V_{ILB}$ | | $T_A = -55°C$ | 0.5<br>−50 | | 170 | µA |
| $I_{EE}$ | Power Supply Current (Pin 8) | All Inputs and Outputs Open | | $T_A = -55°C$ | −165 | −115 | | mA |
| | | | | $T_A = +125°C$ | | −80 | | |

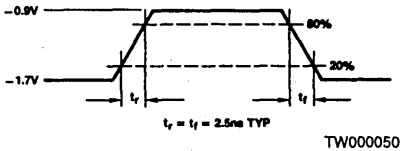
Note: See DC CHARACTERISTICS table (Commercial).

## SWITCHING TEST CIRCUIT




TC000220

## SWITCHING TEST WAVEFORM




TW000050

## KEY TO SWITCHING TEST WAVEFORM

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | MUST BE STEADY | WILL BE STEADY |
| ——— | | |
| ⫽⫽⫽ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| ⫽⫽⫽ | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| ⫽⫽⫽ | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN |
| ⫽⫽⫽ | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

KS000010

$R_T = 50\Omega$ temination of measurement system
$C_L = 30pF$(including stray jig capacitance)

## SWITCHING CHARACTERISTICS (Commercial)

| No. | Symbol | Parameters | Test Conditions | Am10515SA Min | Am10515SA Typ (Note 1) | Am10515SA Max | Am10415A Min | Am10415A Typ (Note 1) | Am10415A Max | Am10415 Min | Am10415 Typ (Note 1) | Am10415 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ MODE** | | | | | | | | | | | | | |
| 1 | $t_{ACS}$ | Chip Select Access Time | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | | 6 | 8 | | 6 | 8 | | 7 | 10 | ns |
| 2 | $t_{RCS}$ | Chip Select Recovery Time | | | 5 | 8 | | 5 | 8 | | 7 | 10 | ns |
| 3 | $t_{AA}$ | Address Access Time | | | 10 | 15 | | 13 | 20 | | 20 | 35 | ns |
| **WRITE MODE** | | | | | | | | | | | | | |
| 4 | $t_W$ | Write Pulse Width (to Guarantee Writing) | $t_{WSA} = t_{WSA}$(Min) | 10 | 6 | | 12 | 9 | | 25 | 15 | | ns |
| 5 | $t_{WSD}$ | Data Setup Time Prior to Write | | 2 | 0 | | 4 | 0 | | 5 | 0 | | ns |
| 6 | $t_{WHD}$ | Data Hold Time After Write | | 2 | 0 | | 4 | 0 | | 5 | 0 | | ns |
| 7 | $t_{WSA}$ | Address Setup Time Prior to Write | $t_W = t_W$(Min) | 3 | 0 | | 5 | 3 | | 8 | 5 | | ns |
| 8 | $t_{WHA}$ | Address Hold Time After Write | | 2 | 0 | | 3 | 0 | | 4 | 1 | | ns |
| 9 | $t_{WSCS}$ | Chip Select Setup Time Prior to Write | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | 2 | 0 | | 4 | 0 | | 5 | 0 | | ns |
| 10 | $t_{WHCS}$ | Chip Select Hold Time After Write | | 2 | 0 | | 4 | 0 | | 5 | 0 | | ns |
| 11 | $t_{WS}$ | Write Disable Time | | | 5 | 10 | | 5 | 10 | | 7 | 10 | ns |
| 12 | $t_{WR}$ | Write Recovery Time | | | 6 | 12 | | 10 | 15 | | 14 | 20 | ns |
| **RISE TIME AND FALL TIME** | | | | | | | | | | | | | |
| 13 | $t_r$ | Output Rise Time | Measured between 20% and 80% points | | 5 | | | 5 | | | 5 | | ns |
| 14 | $t_f$ | Output Fall Time | | | 5 | | | 5 | | | 5 | | |
| **CAPACITANCE** | | | | | | | | | | | | | |
| 15 | $C_{IN}$ | Input Pin Capacitance | Measure with a Pulse Technique | | 4 | 5 | | 4 | 5 | | 4 | 5 | pF |
| 16 | $C_{OUT}$ | Output Pin Capacitance | | | 7 | 8 | | 7 | 8 | | 7 | 8 | |

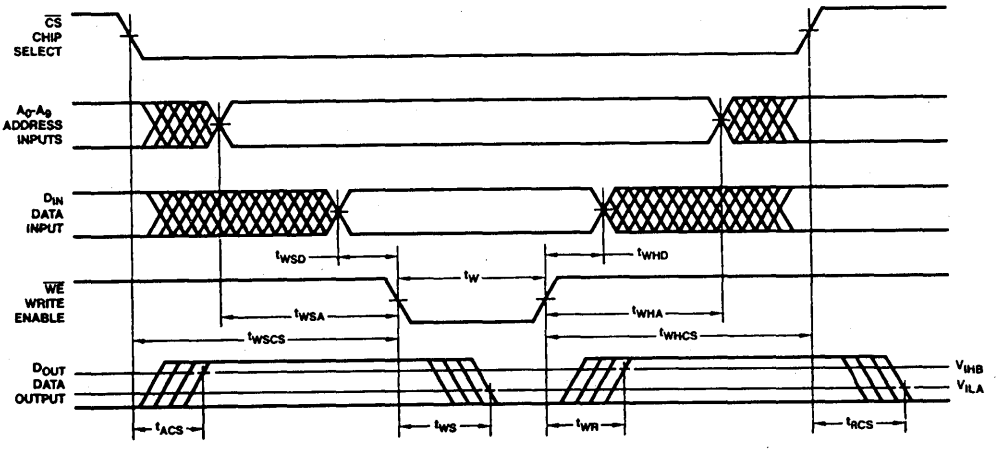
## SWITCHING CHARACTERISTICS (Military)

| No. | Symbol | Parameters | Test Conditions | Am10415SA Min | Am10415SA Typ (Note 1) | Am10415SA Max | Am10415A Min | Am10415A Typ (Note 1) | Am10415A Max | Am10415 Min | Am10415 Typ (Note 1) | Am10415 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ MODE** | | | | | | | | | | | | | |
| 1 | $t_{ACS}$ | Chip Select Access Time | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | | 6 | 10 | | 6 | 12 | | 7 | 15 | ns |
| 2 | $t_{RCS}$ | Chip Select Recovery Time | | | 5 | 10 | | 5 | 12 | | 7 | 15 | ns |
| 3 | $t_{AA}$ | Address Access Time | | | 10 | 20 | | 13 | 25 | | 20 | 40 | ns |
| **WRITE MODE** | | | | | | | | | | | | | |
| 4 | $t_W$ | Write Pulse Width (to Guarantee Writing) | $t_{WSA} = t_{WSA}(Min)$ | 13 | 6 | | 16 | 9 | | 25 | 15 | | ns |
| 5 | $t_{WSD}$ | Data Setup Time Prior to Write | | 3 | 0 | | 4 | 0 | | 7 | 0 | | ns |
| 6 | $t_{WHD}$ | Data Hold Time After Write | | 3 | 0 | | 4 | 0 | | 7 | 0 | | ns |
| 7 | $t_{WSA}$ | Address Setup Time | $t_W = t_W(Min)$ | 4 | 0 | | 5 | 3 | | 8 | 5 | | ns |
| 8 | $t_{WHA}$ | Address Hold Time After Write | | 3 | 0 | | 4 | 0 | | 7 | 1 | | ns |
| 9 | $t_{WSCS}$ | Chip Select Setup Time Prior to Write | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | 3 | 0 | | 4 | 0 | | 7 | 0 | | ns |
| 10 | $t_{WHCS}$ | Chip Select Hold Time After Write | | 3 | 0 | | 4 | 0 | | 7 | 0 | | ns |
| 11 | $t_{WS}$ | Write Disable Time | | | 5 | 10 | | 5 | 10 | | 7 | 10 | ns |
| 12 | $t_{WR}$ | Write Recovery Time | | | 6 | 12 | | 10 | 15 | | 14 | 20 | ns |
| **RISE TIME AND FALL TIME** | | | | | | | | | | | | | |
| 13 | $t_r$ | Output Rise Time | Measured between 20% and 80% points | | 5 | | | 5 | | | 5 | | ns |
| 14 | $t_f$ | Output Fall Time | | | 5 | | | 5 | | | 5 | | ns |
| **CAPACITANCE** | | | | | | | | | | | | | |
| 15 | $C_{IN}$ | Input Pin Capacitance | Measure with a Pulse Technique | | 4 | 5 | | 4 | 5 | | 4 | 5 | pF |
| 16 | $C_{OUT}$ | Output Pin Capacitance | | | 7 | 8 | | 7 | 8 | | 7 | 8 | pF |

Note: See DC CHARACTERISTICS table (Commercial).

## SWITCHING WAVEFORMS

### WRITE MODE



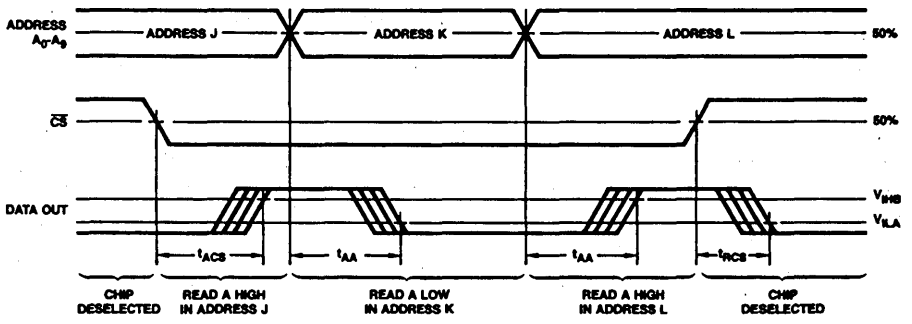

WF001160



01419B

## SWITCHING WAVEFORMS (Cont.)

### READ MODE




WF001170

# Am100415

1024 x 1 IMOX™ II ECL Bipolar RAM



## DISTINCTIVE CHARACTERISTICS

- Fast access time (10ns typ.) — improves system cycle speeds
- Enhanced output voltage level compensation providing 6X (improvement in) $V_{OL}$ and $V_{OH}$ stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

## GENERAL DESCRIPTION

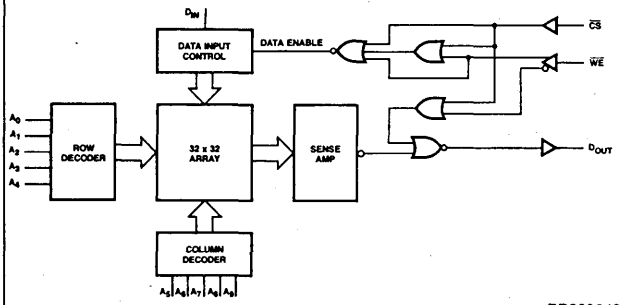
The Am100415A and Am100415 are fully decoded 1024-bit ECL RAMs organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, $A_0$ through $A_9$. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input ($D_{IN}$) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch."

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output ($D_{OUT}$).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

## BLOCK DIAGRAM




BD000640

## MODE SELECT TABLE

| Input | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | $D_{OUT}$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

H = HIGH
L = LOW
X = Don't Care

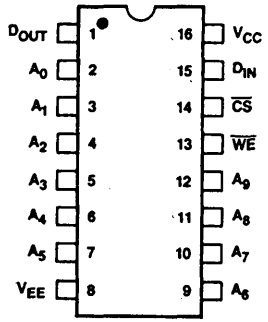
## PRODUCT SELECTOR GUIDE

| Access Time | 15ns | 20ns |
|---|---|---|
| Part Number | Am100415A | Am100415 |

01418B

## CONNECTION DIAGRAM
Top View

DIP

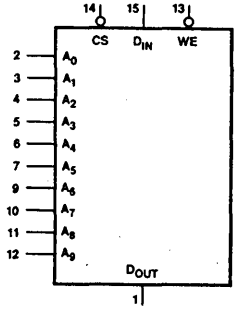



CD000920

Chip-Pak™

TO BE DETERMINED

## LOGIC SYMBOL




LS000240

## ORDERING INFORMATION

Am100415 A P C B

- B — Burn-in Option
  B suffix denotes 160 hour burn-in.
- C — Temperature
  C – Commercial (0°C to +70°C)
- P — Package
  D – 16-pin ceramic DIP
  L – 20-pin leadless chip carrier
  P – 16-pin plastic DIP
- A — Speed Select
  See Product Selector Guide
- Am100415 — Device Type
  1024 x ECL Bipolar RAM

| Valid Combinations | |
|---|---|
| Am100415<br>Am100415A | PC, PCB,<br>DC, DCB,<br>LC, LCB |

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
$V_{EE}$ Pin Potential to
GND Pin ..... −7.0V to +0.5V
Input Voltage (DC) ..... $V_{EE}$ to +0.5V
Output Current (DC Output HIGH) ..... −30mA to +0.1mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +85°C
Supply Voltage ..... −5.7V to −4.2V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

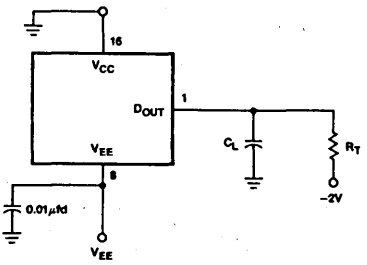
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | B (Note 3) | Typ (Note 1) | A (Note 3) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage HIGH | $V_{IN} = V_{IHA}$ or $V_{ILB}$ | Loading is 50Ω to −2.0V | −1025 | −955 | −880 | mV |
| $V_{OL}$ | Output Voltage LOW | | | −1810 | −1715 | −1620 | mV |
| $V_{OHC}$ | Output Voltage HIGH | $V_{IN} = V_{IHB}$ or $V_{ILA}$ | | −1035 | | | mV |
| $V_{OLC}$ | Output Voltage LOW | | | | | −1610 | mV |
| $V_{IH}$ | Input Voltage HIGH | Guaranteed Input Voltage HIGH for all inputs (Note 4) | | −1165 | | −880 | mV |
| $V_{IL}$ | Input Voltage LOW | Guaranteed Input Voltage LOW for all inputs (Note 4) | | −1810 | | −1475 | mV |
| $I_{IH}$ | Input Current HIGH | $V_{IN} = V_{IHA}$ | | | | 220 | mA |
| $I_{IL}$ | Input Current LOW<br>Chip Select ($\overline{CS}$)<br>All Other Inputs | $V_{IN} = V_{ILB}$ | | 0.5<br>−50 | | 170 | mA |
| $I_{EE}$ | Power Supply Current (Pin 8) | All Inputs and Outputs Open | | −150 | −105 | | mA |

Notes:

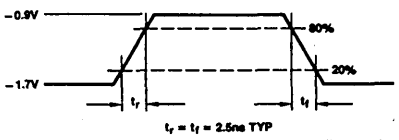
1. Typical values are at $V_{EE} = -4.5V$, $T_A = 25°C$ and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   $\theta_{JA}$ (Junction to Ambient) = 90°C/Watt (still air)
   $\theta_{JA}$ (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   $\theta_{JC}$ (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## SWITCHING TEST CIRCUIT



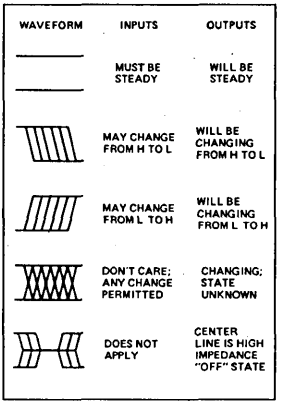

TC000220

## SWITCHING TEST WAVEFORM




TW000050

## KEY TO SWITCHING WAVEFORMS




KS000010

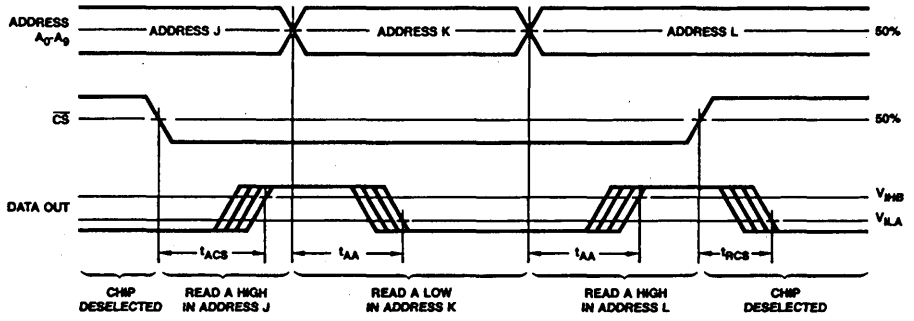
$R_T$ = 50Ω termination of measurement system
$CP_L$ = 30pF (including stray jig capacitance)

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Parameters | Test Conditions | Am100415A Min | Am100415A Typ (Note 1) | Am100415A Max | Am100415 Min | Am100415 Typ (Note 1) | Am100415 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **READ MODE** | | | | | | | | | | |
| 1 | $t_{ACS}$ | Chip Select Access Time | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | | 5 | 8 | | 5 | 8 | ns |
| 2 | $t_{RCS}$ | Chip Select Recovery Time | | | 5 | 8 | | 5 | 8 | |
| 3 | $t_{AA}$ | Address Access Time | | | 10 | 15 | | 12 | 20 | |
| **WRITE MODE** | | | | | | | | | | |
| 4 | $t_W$ | Write Pulse Width (to Guarantee Writing) | $t_{WSA} = t_{WSA}$(Min) | 10 | 6 | | 12 | 9 | | ns |
| 5 | $t_{WSD}$ | Data Setup Time Prior to Write | | 2 | 0 | | 4 | 0 | | ns |
| 6 | $t_{WHD}$ | Data Hold Time After Write | | 2 | 0 | | 4 | 0 | | ns |
| 7 | $t_{WSA}$ | Address Setup Time Prior to Write | $t_W = t_W$(Min) | 3 | 0 | | 5 | 3 | | ns |
| 8 | $t_{WHA}$ | Address Hold Time After Write | | 2 | 0 | | 3 | 0 | | ns |
| 9 | $t_{WSCS}$ | Chip Select Setup Time Prior to Write | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | 2 | 0 | | 4 | 0 | | ns |
| 10 | $t_{WHCS}$ | Chip Select Hold Time After Write | | 2 | 0 | | 4 | 0 | | ns |
| 11 | $t_{WS}$ | Write Disable Time | | | 5 | 10 | | 5 | 10 | ns |
| 12 | $t_{WR}$ | Write Recovery Time | | | 6 | 12 | | 7 | 15 | ns |
| **RISE TIME AND FALL TIME** | | | | | | | | | | |
| 13 | $t_r$ | Output Rise Time | Measured between 20% and 80% points | | 5 | | | 5 | | ns |
| 14 | $t_f$ | Output Fall Time | | | 5 | | | 5 | | |
| **CAPACITANCE** | | | | | | | | | | |
| 15 | $C_{IN}$ | Input Pin Capacitance | Measure with a Pulse Technique | | 4 | 5 | | 4 | 5 | pF |
| 16 | $C_{OUT}$ | Output Pin Capacitance | | | 7 | 8 | | 7 | 8 | |

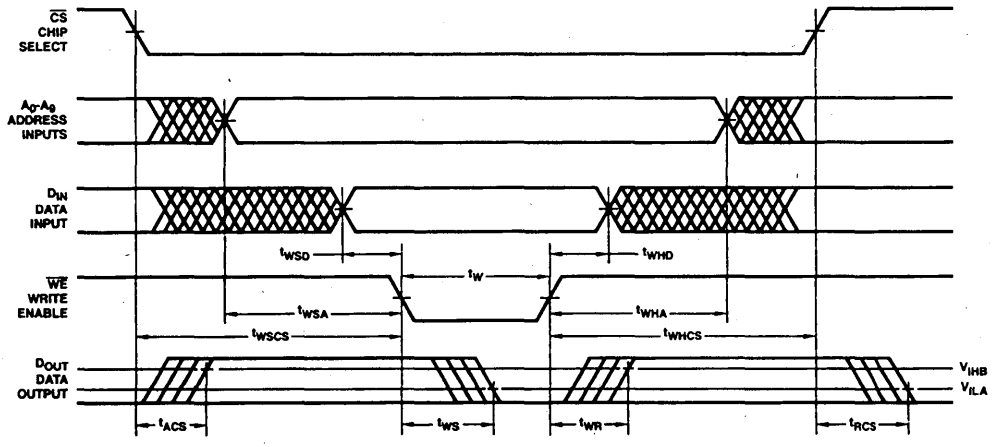
## SWITCHING WAVEFORMS

### READ MODE




WF001170

### WRITE MODE




WF001160

# Am10474

1024 x 4 IMOX™ ECL Bipolar RAM

ADVANCED INFORMATION

## DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) — improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL — no board changes required
- Internally voltage and temperature compensated providing flat AC performance
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

## GENERAL DESCRIPTION

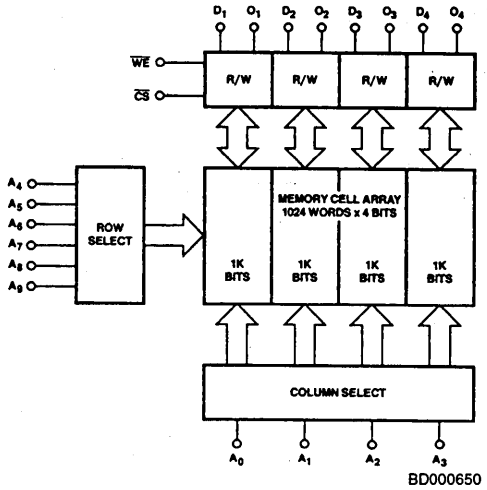
The Am10474SA, Am10474A and Am10474 are fully decoded 4096-bit ECL RAMs organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, $A_0$ through $A_9$. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input ($D_1 - D_4$) are written into the addressed memory words.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting outputs $D_1 - D_4$.

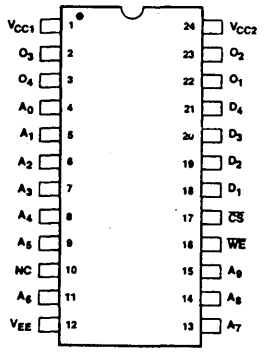
During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

## BLOCK DIAGRAM



## CONNECTION DIAGRAM
### Top View

**DIP**

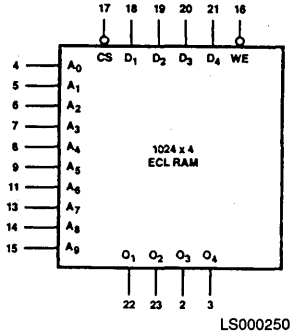



CD000930

**Chip-Pak™**


Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000250



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# Am100474

ECL 1024 x 4 IMOX™ Bipolar RAM

ADVANCED INFORMATION

## DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) — improves system cycle speeds
- Fully compatible with 100K series ECL logic — no board changes required
- Enhanced output voltage level compensation providing 6X (improvement in) $V_{OL}$ and $V_{OH}$ stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

## GENERAL DESCRIPTION

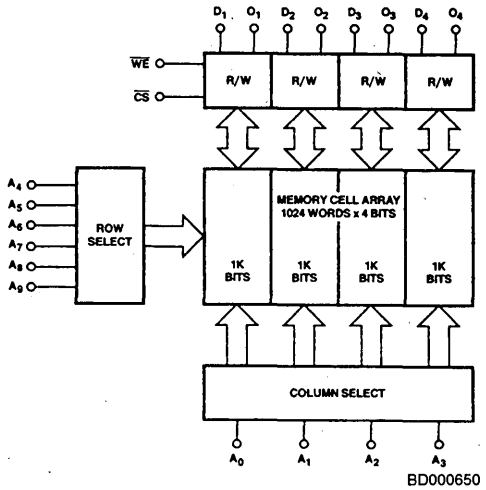
The Am100474SA, Am100474A and Am100474 are fully decoded 4096-bit ECL RAMs organized 1024 words by 4 bits. Word selection is achieved by means of a 10-bit address, $A_0$ through $A_9$. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and unterminated OR tieable emitter follower outputs.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data inputs ($D_1 - D_4$) are written into the addressed memory words.

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed words is read out on the noninverting outputs $O_1 - O_4$.

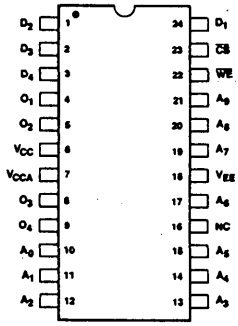
During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

## BLOCK DIAGRAM



## CONNECTION DIAGRAM
Top View

### DIP

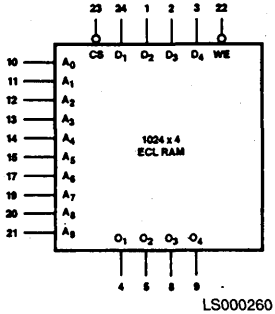



CD000940

### Chip-Pak™


Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000260



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# Am10470

4096 X 1 IMOX™ ECL Bipolar RAM

## DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) — improves system cycle speeds
- Fully compatible with standard voltage compensated 10K series ECL — no board changes required
- Internally voltage compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

## GENERAL DESCRIPTION

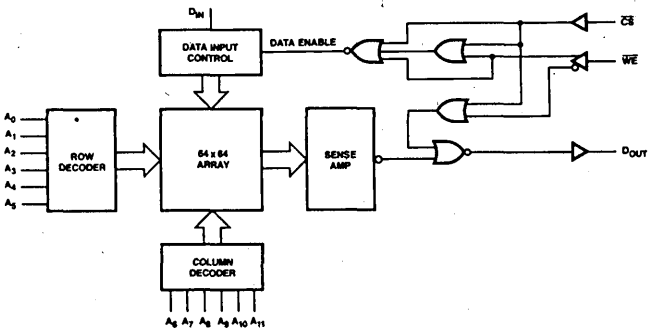
The Am10470SA, Am10470A and Am10470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, $A_0$ through $A_{11}$. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input ($D_{IN}$) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output ($D_{OUT}$).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

## BLOCK DIAGRAM




BD000660

## MODE SELECT TABLE

| Input | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | $D_{OUT}$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

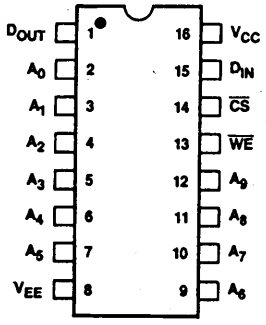
H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

| Access Time | 15ns | 20ns | 25ns | 30ns | 35ns | 40ns |
|---|---|---|---|---|---|---|
| Temperature Range | C | M | C | M | C | M |
| Part Number | Am10470SA | Am10470SA | Am10470A | Am10470A | Am10470 | Am10470 |

## CONNECTION DIAGRAM
Top View

DIP



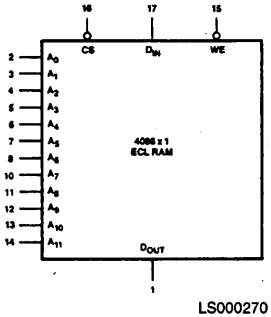

CD000920

Chip-Pak™

TO BE DETERMINED

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000270

## ORDERING INFORMATION

Am10470 SA D C B

- B — Burn-in Option
  - B suffix denotes 160 hour burn-in.
- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 16-pin ceramic DIP
  - F – 16-pin flatpak
  - L – 20-pin leadless chip carrier
  - P – 16-pin plastic DIP
- SA — Speed Select
  - See Product Selector Guide
- Am10470 — Device Type
  - 4096 x ECL Bipolar RAM

| Valid Combinations | |
|---|---|
| Am10470<br>Am10470A<br>Am10470SA | DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
$V_{EE}$ Pin Potential to GND Pin ..... −7.0V to +0.5V
Input Voltage (DC) ..... $V_{EE}$ to +0.5V
Output Current (DC Output HIGH) ..... −30mA to +0.1mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... −5.46V to −4.94V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... −5.72V to −4.68V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS (Commercial)

| Symbol | Parameter | Test Conditions | | | B (Note 3) | Typ (Note 1) | A (Note 3) | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage HIGH | $V_{IN} = V_{IHA}$ or $V_{ILB}$ | Loading is 50Ω to −2.0V | $T_A = 0°C$ | −1000 | | −840 | mV |
| | | | | $T_A = +25°C$ | −960 | | −810 | |
| | | | | $T_A = +75°C$ | −900 | | −720 | |
| $V_{OL}$ | Output Voltage LOW | | | $T_A = 0°C$ | −1870 | | −1665 | mV |
| | | | | $T_A = +25°C$ | −1850 | | −1650 | |
| | | | | $T_A = +75°C$ | −1830 | | −1625 | |
| $V_{OHC}$ | Output Voltage HIGH | $V_{IN} = V_{IHB}$ or $V_{ILA}$ | | $T_A = 0°C$ | −1020 | | | mV |
| | | | | $T_A = +25°C$ | −980 | | | |
| | | | | $T_A = +75°C$ | −920 | | | |
| $V_{OLC}$ | Output Voltage LOW | | | $T_A = 0°C$ | | | −1645 | mV |
| | | | | $T_A = +25°C$ | | | −1630 | |
| | | | | $T_A = +75°C$ | | | −1605 | |
| $V_{IH}$ | Input Voltage HIGH | Guaranteed Input Voltage HIGH for All Input (Note 4) | | $T_A = 0°C$ | −1145 | | −840 | mV |
| | | | | $T_A = +25°C$ | −1105 | | −810 | |
| | | | | $T_A = +75°C$ | −1045 | | −720 | |
| $V_{IL}$ | Input Voltage LOW | Guaranteed Input Voltage Low for All Inputs (Note 4) | | $T_A = 0°C$ | −1870 | | −1490 | mV |
| | | | | $T_A = +25°C$ | −1850 | | −1475 | |
| | | | | $T_A = +75°C$ | −1830 | | −1450 | |
| $I_{IH}$ | Input Current HIGH | $V_{IN} = V_{IHA}$ | | $T_A = 0°C$ to +75°C | | | 220 | µA |
| $I_{IL}$ | Input Current LOW Chip Select ($\overline{CS}$) All Other Inputs | $V_{IN} = V_{ILB}$ | | $T_A = +25°C$ | 0.5 −50 | | 170 | µA |
| $I_{EE}$ | Power Supply Current (Pin 9) | All Inputs and Outputs Open | Am10470A and Am10470 | $T_A = 0°C$ | −200 | −160 | | mA |
| | | | | $T_A = +75°C$ | | −145 | | |
| | | | Am10470SA | $T_A = 0°C$ | −230 | −180 | | |

Notes:

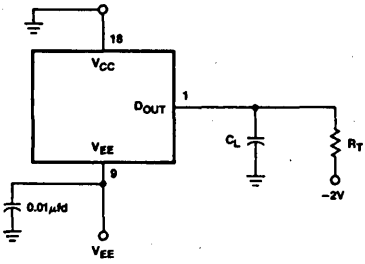
1. Typical values are at $V_{EE} = -5.2V$, $T_A = 25°C$ and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical thermal resistance values of the package are:
   $\theta_{JA}$ (Junction to Ambient) = 90°C/Watt (still air)
   $\theta_{JA}$ (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   $\theta_{JC}$ (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## DC CHARACTERISTICS (Military)

| Symbol | Parameter | Test Conditions | | | B (Note 3) | Typ (Note 1) | A (Note 3) | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage HIGH | $V_{IN} = V_{IHA}$ or $V_{ILB}$ | Loading is 50Ω to −2.0V | $T_A = -55°C$ | −1070 | | −860 | mV |
| | | | | $T_A = +125°C$ | −860 | | −650 | |
| $V_{OL}$ | Output Voltage LOW | | | $T_A = -55°C$ | −1900 | | −1690 | mV |
| | | | | $T_A = +125°C$ | −1800 | | −1570 | |
| $V_{OHC}$ | Output Voltage HIGH | $V_{IN} = V_{IHB}$ or $V_{ILA}$ | | $T_A = -55°C$ | −1090 | | | mV |
| | | | | $T_A = +125°C$ | −880 | | | |
| $V_{OLC}$ | Output Voltage LOW | | | $T_H = -55°C$ | | | −1670 | mV |
| | | | | $T_A = +125°C$ | | | −1550 | |
| $V_{IH}$ | Input Voltage HIGH | Guaranteed Input Voltage HIGH for All Inputs (Note 4) | | $T_A = -55°C$ | −1215 | | −860 | mV |
| | | | | $T_A = +125°C$ | −1005 | | −650 | |
| $V_{IL}$ | Input Voltage LOW | Guaranteed Input Voltage LOW for All Inputs (Note 4) | | $T_A = -55°C$ | −1900 | | −1515 | mV |
| | | | | $T_A = +125°C$ | −1800 | | −1395 | |
| $I_{IH}$ | Input Current HIGH | $V_{in} = V_{IHA}$ | | $T_A = -55°C$ | | | 250 | μA |
| $I_{IL}$ | Input Current LOW<br>Chip Select($\overline{CS}$)<br>All Other Inputs | $V_{IN} = V_{ILB}$ | | $T_A = -55°C$ | 0.5<br>−50 | | 170 | μA |
| $I_{EE}$ | Power Supply Current (Pin 9) | All Inputs and Outputs Open | Am10470A and Am10470 | $T_A = -55°C$ | −220 | −175 | | mA |
| | | | | $T_A = +125°C$ | | −160 | | |
| | | | Am 10470SA | $T_A = -55°C$ | −255 | −200 | | |

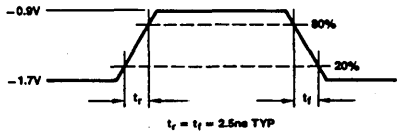
Note: See DC CHARACTERISTICS table (Commercial)

## SWITCHING TEST CIRCUIT



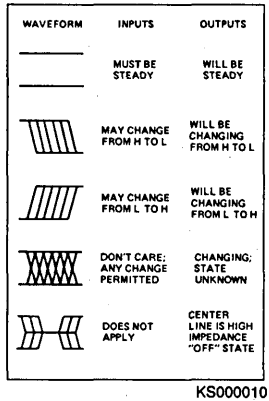

TC000230

## SWITCHING TEST WAVEFORM




TW000050

## KEY TO SWITCHING WAVEFORMS




KS000010

$R_T$ = 50Ω termination of measurement system
$C_L$ = 30pF (including stray jig capacitance)

## SWITCHING CHARACTERISTICS (Commercial)

| No. | Symbol | Parameters | Test Conditions | Am100470SA Min | Am100470SA Typ (Note 1) | Am100470SA Max | Am100470A Min | Am100470A Typ (Note 1) | Am100470A Max | Am100470 Min | Am100470 Typ (Note 1) | Am100470 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ MODE** | | | | | | | | | | | | | |
| 1 | $t_{ACS}$ | Chip Select Access Time | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | | 6 | 8 | | 8 | 10 | | 10 | 15 | ns |
| 2 | $t_{RCS}$ | Chip Select Recovery Time | | | 6 | 8 | | 8 | 10 | | 10 | 15 | ns |
| 3 | $t_{AA}$ | Address Access Time | | | 12 | 15 | | 18 | 25 | | 25 | 35 | ns |
| **WRITE MODE** | | | | | | | | | | | | | |
| 4 | $t_W$ | Write Pulse Width (to Guarantee Writing) | $t_{WSA} = t_{WSA}$(Min) | 15 | 8 | | 20 | 10 | | 25 | 15 | | ns |
| 5 | $t_{WSD}$ | Data Setup Time Prior to Write | | 2 | 0 | | 2 | 0 | | 5 | 1 | | ns |
| 6 | $t_{WHD}$ | Data Hold Time After Write | | 2 | 0 | | 2 | 0 | | 5 | 1 | | ns |
| 7 | $t_{WSA}$ | Address Setup Time Prior to Write | $t_W = t_W$(Min) | 2 | 0 | | 2 | 0 | | 5 | 1 | | ns |
| 8 | $t_{WHA}$ | Address Hold Time After Write | | 2 | 0 | | 2 | 0 | | 5 | 1 | | ns |
| 9 | $t_{WSCS}$ | Chip Select Setup Time Prior to Write | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | 2 | | | 2 | 0 | | 5 | 1 | | ns |
| 10 | $t_{WHCS}$ | Chip Select Hold Time After Write | | 2 | 0 | | 2 | 0 | | 5 | 1 | | ns |
| 11 | $t_{WS}$ | Write Disable Time | | | 6 | 8 | | 8 | 10 | | 7 | 15 | ns |
| 12 | $t_{WR}$ | Write Recovery Time | | | 6 | 8 | | 8 | 10 | | 10 | 20 | ns |
| **RISE TIME AND FALL TIME** | | | | | | | | | | | | | |
| 13 | $t_r$ | Output Rise Time | Measured between 20% and 80% points | | 3 | | | 3 | | | 3 | | ns |
| 14 | $t_f$ | Output Fall Time | | | 3 | | | 3 | | | 3 | | ns |
| **CAPACITANCE** | | | | | | | | | | | | | |
| 15 | $C_{IN}$ | Input Pin Capacitance | Measure with a Pulse Technique on a Sample Basis. | | 4 | 5 | | 4 | 5 | | 4 | 5 | pF |
| 16 | $C_{OUT}$ | Output Pin Capacitance | | | 7 | 8 | | 7 | 8 | | 7 | 8 | |

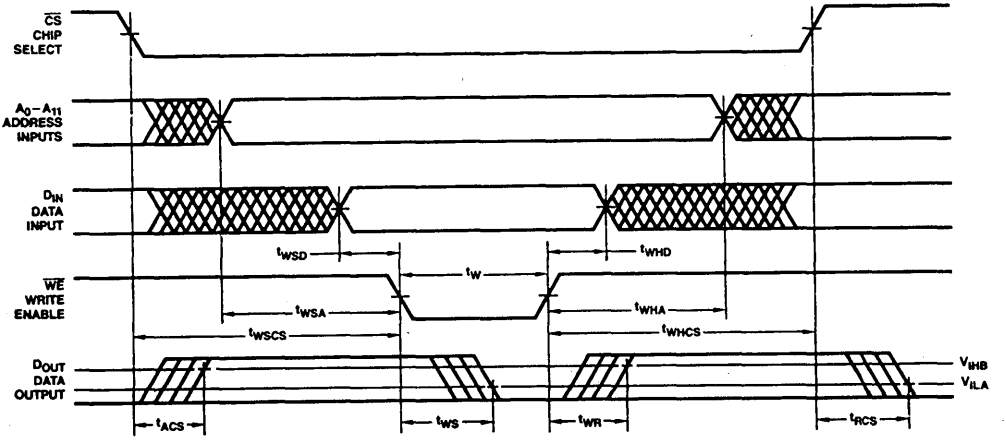
## SWITCHING CHARACTERISTICS (Military)

| No. | Symbol | Parameters | Test Conditions | Am100470SA Min | Am100470SA Typ (Note 1) | Am100470SA Max | Am100470A Min | Am100470A Typ (Note 1) | Am100470A Max | Am100470 Min | Am100470 Typ (Note 1) | Am100470 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ MODE** | | | | | | | | | | | | | |
| 1 | $t_{ACS}$ | Chip Select Access Time | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | | 8 | 10 | | 10 | 15 | | 15 | 20 | ns |
| 2 | $t_{RCS}$ | Chip Select Recovery Time | | | 8 | 10 | | 10 | 15 | | 15 | 20 | ns |
| 3 | $t_{AA}$ | Address Access Time | | | 17 | 20 | | 20 | 30 | | 30 | 40 | ns |
| **WRITE MODE** | | | | | | | | | | | | | |
| 4 | $t_W$ | Write Pulse Width | $t_{WSA} = t_{WSA}(Min)$ | 18 | 14 | | 22 | 17 | | 25 | 20 | | ns |
| 5 | $t_{WSD}$ | Data Setup Time Prior to Write | | 3 | 0 | | 5 | 0 | | 7 | 2 | | ns |
| 6 | $t_{WHD}$ | Data Hold Time After Write | | 3 | 0 | | 5 | 0 | | 7 | 2 | | ns |
| 7 | $t_{WSA}$ | Address Setup Time Prior to Write | $t_W = t_W(Min)$ | 3 | 0 | | 5 | 0 | | 7 | 2 | | ns |
| 8 | $t_{WHA}$ | Address Hold Time | | 3 | 0 | | 5 | 0 | | 7 | 2 | | ns |
| 9 | $t_{WSCS}$ | Chip Select Setup Time Prior to Write | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ fo $V_{OH}$) | 3 | 0 | | 5 | 0 | | 7 | 2 | | ns |
| 10 | $t_{WHCS}$ | Chip Select Hold Time After Write | | 3 | 0 | | 5 | 0 | | 7 | 2 | | ns |
| 11 | $t_{WS}$ | Write Disable Time | | | 8 | 10 | | 10 | 12 | | 7 | 15 | ns |
| 12 | $t_{WR}$ | Write Recovery Time | | | 8 | 10 | | 10 | 12 | | 10 | 20 | ns |
| **RISE TIME AND FALL TIME** | | | | | | | | | | | | | |
| 13 | $t_r$ | Output Rise Time | Measured between 20% and 80% points | | 3 | | | 3 | | | 3 | | ns |
| 14 | $t_f$ | Output Fall Time | | | 3 | | | 3 | | | 3 | | ns |
| **CAPACITANCE** | | | | | | | | | | | | | |
| 15 | $C_{IN}$ | Input Pin Capacitance | Measure with a Pulse Technique on a Sample Basis. | | 4 | 5 | | 4 | 5 | | 4 | 5 | pF |
| 16 | $C_{OUT}$ | Output Pin Capacitance | | | 7 | 8 | | 7 | 8 | | 7 | 8 | pF |

Note: See DC CHARACTERISTICS table (Commercial)

## SWITCHING WAVEFORMS

### WRITE MODE



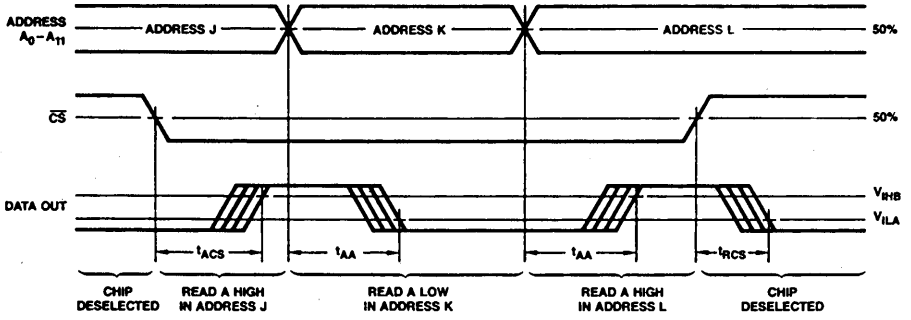

WF001180



03224B

## SWITCHING WAVEFORMS (Cont.)

### READ MODE




WF001190

# Am100470

4096 x 1 IMOX™ ECL Bipolar RAM

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Fast access time (12ns typ) — improves system cycle speeds
- Enhanced output voltage level compensation providing 6X (improvement in) $V_{OL}$ and $V_{OH}$ stability over supply and temperature ranges
- Internally voltage and temperature compensated providing flat AC performance
- Outputs preconditioned during write cycle eliminating write recovery glitch
- Emitter follower outputs — easy wire-ORing
- Power dissipation decreases with increasing temperature

## GENERAL DESCRIPTION

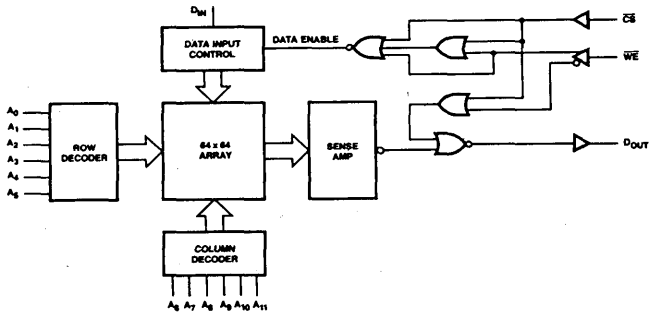
The Am100470SA, Am100470A and Am100470 are fully decoded 4096-bit ECL RAMs organized 4096 words by one bit. Bit selection is achieved by means of a 12-bit address, $A_0$ through $A_{11}$. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and an unterminated OR tieable emitter follower output.

An active LOW write line ($\overline{WE}$) controls the write/read operation of the memory. When the chip select and write lines are LOW, the data input ($D_{IN}$) is written into the addressed memory word simultaneously preconditioning the output so true data is present when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the 'write recovery glitch.'

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the noninverting output ($D_{OUT}$).

During the writing operation or when the chip select line is HIGH the output of the memory goes to a LOW state.

## BLOCK DIAGRAM




BD000660

## MODE SELECT TABLE

| Input | | | Output | |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | $D_{IN}$ | $D_{OUT}$ | Mode |
| H | X | X | L | Not Selected |
| L | L | L | L | Write "0" |
| L | L | H | L | Write "1" |
| L | H | X | $D_{OUT}$ | Read |

H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

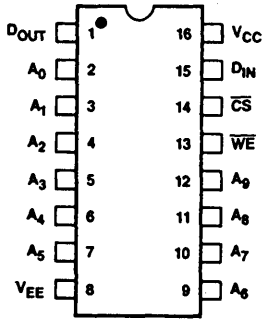
| Access Time | 15ns | 20ns | 35ns |
|---|---|---|---|
| Part Number | Am100470SA | Am100470A | Am100470 |

IMOX is a tradement of Advanced Micro Devices, Inc.

03225B

## CONNECTION DIAGRAM
Top View

DIP



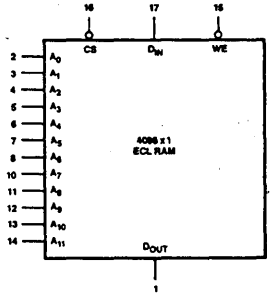

CD000920

Chip-Pak™

TO BE DETERMINED

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000270

## ORDERING INFORMATION

Am100470 SA D C B

- Burn-in Option
  B suffix denotes 160 hour burn-in.
- Temperature
  C – Commercial (0°C to +70°C)
- Package
  D – 18-pin ceramic DIP
  L – 20-pin leadless chip carrier
- Speed Select
  See Product Selector Guide
- Device Type
  4096 x 1 ECL Bipolar RAM

| Valid Combinations | |
|---|---|
| Am100470<br>AM100470A<br>Am100470SA | DC, DCB,<br>LC, LCB |

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
$V_{EE}$ Pin Potential to GND Pin ..... −7.0V to +0.5V
Input Voltage (DC) ..... $V_{EE}$ to +0.5V
Output Current (DC Output HIGH) ..... −30mA to +0.1mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... −5.7V to −4.2V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

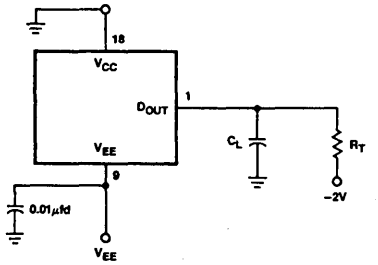
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | B (Note 3) | Typ (Note 1) | A (Note 3) | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output Voltage HIGH | $V_{IN} = V_{IHA}$ or $V_{ILB}$ | Loading is 50Ω to −2.0V | −1025 | −955 | −880 | mV |
| $V_{OL}$ | Output Voltage LOW | | | −1810 | −1715 | −1620 | mV |
| $V_{OHC}$ | Output Voltage HIGH | $V_{IN} = V_{IHB}$ or $V_{ILA}$ | | −1035 | | | mV |
| $V_{OLC}$ | Output Voltage LOW | | | | | −1610 | mV |
| $V_{IH}$ | Input Voltage HIGH | Guaranteed Input Voltage HIGH for all inputs (Note 4) | | −1165 | | −880 | mV |
| $V_{IL}$ | Input Voltage LOW | Guaranteed Input Voltage LOW for all inputs (Note 4) | | −1810 | | −1475 | mV |
| $I_{IH}$ | Input Current HIGH | $V_{IN} = V_{IHA}$ | | | | 220 | μA |
| $I_{IL}$ | Input Current LOW<br>Chip Select($\overline{CS}$)<br>All Other Inputs | $V_{IN} = V_{ILB}$ | | 0.5<br>−50 | | 170 | μA |
| $I_{EE}$ | Power Supply Current (Pin 9) | All Inputs and Outputs Open | Am100470A/Am100470 | −195 | −160 | | mA |
| | | | Am100470SA | −230 | −180 | | |

Notes:

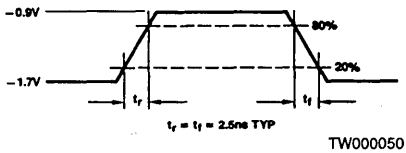
1. Typical values are at $V_{EE} = -4.5V$, $T_A = 25°C$ and maximum loading.
2. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   $\theta_{JA}$ (Junction to Ambient) = 90°C/Watt (still air)
   $\theta_{JA}$ (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   $\theta_{JC}$ (Junction to Case) = 25°C/Watt
3. Definition of symbols and terms used in this product specification: The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

## SWITCHING TEST CIRCUIT




TC000230

## SWITCHING TEST WAVEFORMS




TW000050

## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | MUST BE STEADY | WILL BE STEADY |
| ——— | | |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN |
| | DOES NOT APPLY | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

KS000010

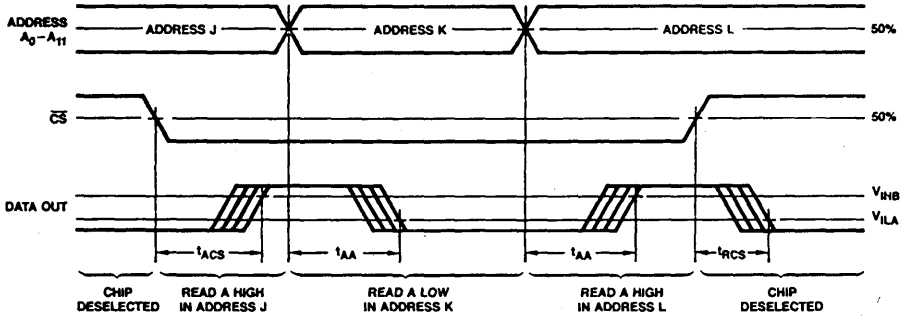
$R_T$ = 50Ω termination of measurement system
$C_L$ = 30pF (including stray jig capacitance)

## SWITCHING CHARACTERISTICS (Commercial)

| No. | Symbol | Parameters | Test Conditions | Am100470SA Min | Am100470SA Typ (Note 1) | Am100470SA Max | Am100470A Min | Am100470A Typ (Note 1) | Am100470A Max | Am100470 Min | Am100470 Typ (Note 1) | Am100470 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ MODE** | | | | | | | | | | | | | |
| 1 | $t_{ACS}$ | Chip Select Access Time | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | | 6 | 8 | | 8 | 10 | | 10 | 15 | ns |
| 2 | $t_{RCS}$ | Chip Select Recovery Time | | | 6 | 8 | | 8 | 10 | | 10 | 15 | ns |
| 3 | $t_{AA}$ | Address Access Time | | | 12 | 15 | | 18 | 25 | | 25 | 35 | ns |
| **WRITE MODE** | | | | | | | | | | | | | |
| 4 | $t_W$ | Write Pulse Width (to Guarantee Writing) | $t_{WSA} = t_{WSA}$(Min) | 15 | | | 20 | | | 25 | 18 | | ns |
| 5 | $t_{WSD}$ | Data Setup Time Prior to Write | | 2 | | | 2 | | | 5 | 1 | | ns |
| 6 | $t_{WHD}$ | Data Hold Time After Write | | 2 | | | 2 | | | 5 | 1 | | ns |
| 7 | $t_{WSA}$ | Address Setup Time Prior to Write | $t_W = t_W$(Min) | 3 | | | 3 | | | 10 | 5 | | ns |
| 8 | $t_{WHA}$ | Address Hold Time After Write | | 2 | | | 2 | | | 5 | 1 | | ns |
| 9 | $t_{WSCS}$ | Chip Select Setup Time Prior to Write | Measured at 50% of input to valid output ($V_{ILA}$ for $V_{OL}$ or $V_{IHB}$ for $V_{OH}$) | 2 | | | 2 | | | 5 | 1 | | ns |
| 10 | $t_{WHCS}$ | Chip Select Hold Time After Write | | 2 | | | 2 | | | 5 | 1 | | ns |
| 11 | $t_{WS}$ | Write Disable Time | | | 6 | 8 | | 8 | 10 | | 7 | 15 | ns |
| 12 | $t_{WR}$ | Write Recovery Time | | | 6 | 8 | | 8 | 10 | | 10 | 20 | ns |
| **RISE TIME AND FALL TIME** | | | | | | | | | | | | | |
| 13 | $t_r$ | Output Rise Time | Measured between 20% and 80% points | | 2 | | | 2 | | | 2 | | ns |
| 14 | $t_f$ | Output Fall Time | | | 2 | | | 2 | | | 2 | | |
| **CAPACITANCE** | | | | | | | | | | | | | |
| 15 | $C_{IN}$ | Input Pin Capacitance | Measure with a Pulse Technique on a Sample Basis. | | 4 | 5 | | 4 | 5 | | 4 | 5 | pF |
| 16 | $C_{OUT}$ | Output Pin Capacitance | | | 7 | 8 | | 7 | 8 | | 7 | 8 | |

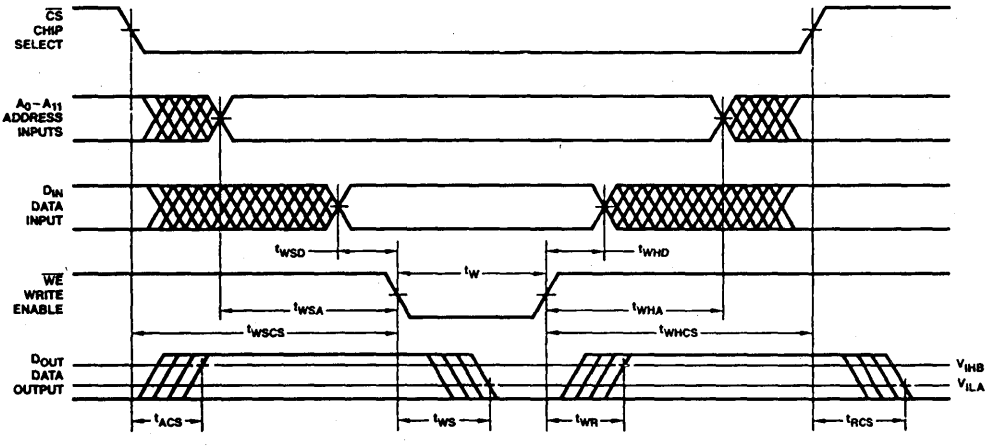
## SWITCHING WAVEFORMS

### READ MODE




WF001190

### WRITE MODE




WF001180

# Am3101 Family

64-Bit Write Transparent Schottky Bipolar RAM

## DISTINCTIVE CHARACTERISTICS

- Standard Version: Address access time 50ns
- Low Power: $I_{CC}$ typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Available with open collector outputs or with three-state outputs (Am74S189 and Am54S189)
- High Speed
- Fully decoded 16-word x 4 bit Schottky RAMs

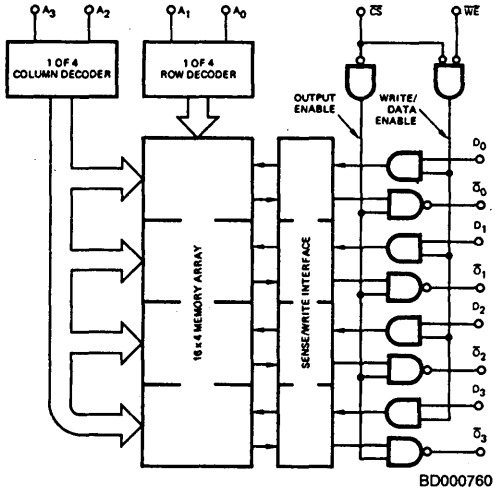
## GENERAL DESCRIPTION

The Am3101 family is comprised of 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs. Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line ($\overline{WE}$) controls the writing/reading operation of the memory. Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

When the chip select line is HIGH, the four outputs of the memory go to an inactive high impedance state.

## BLOCK DIAGRAM




BD000760

## MODE SELECT TABLE

| Input | | Data Output Status $\overline{O}_0 - \overline{O}_3$ | Mode |
|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | | |
| L | L | Output Disabled | Write |
| L | H | Selected Word (Inverted) | Read |
| H | X | Output Disabled | Deselect |

## MODE SELECT TABLE*

| Input | | Data Output Status $\overline{O}_0 - \overline{O}_3$ | Mode |
|---|---|---|---|
| $\overline{CS}$ | $\overline{WE}$ | | |
| L | L | Data In (Inverted) | Write |
| L | H | Selected Word (Inverted) | Read |
| H | X | Output and Write Disabled | Deselect |

*For Write Transparent Parts

H = HIGH L = LOW = Don't Care

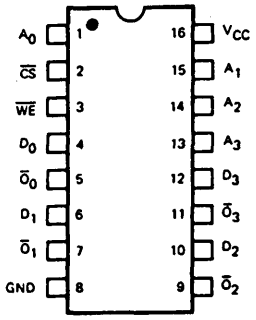
## PRODUCT SELECTOR GUIDE

| Access Time | 35ns | 50ns | | 55ns | 60ns | 65ns | 80ns | 90ns |
|---|---|---|---|---|---|---|---|---|
| Temperature Range | C | C | M | C | M | M | C | M |
| Open Collector | Am3101A Am74S289 | | Am3101A Am54S289 | | | | | |
| Three State | Am74S189 | | Am54S189 | | | | | |
| Open Collector (Write Transparent) | Am3101-1 Am7489-1 | Am3101 Am7489 | Am3101-1 Am5489-1 | Am31L01A | Am3101 Am5489 | Am31L01A | Am31L01 | Am31L01 |

03203B

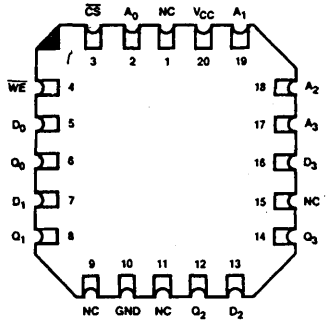
## CONNECTION DIAGRAM
### Top View

**DIP**




CD000830

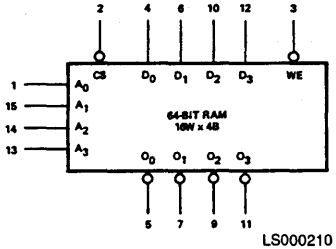
**Chip-Pak™**




CD000840

Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS000210

## ORDERING INFORMATION

**Am31L01 D C B**

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- C — Temperature: C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 16-pin ceramic DIP; F – 16-pin flatpak; L – 20-pin leadless chip carrier; P – 16-pin plastic DIP
- Am31L01 — Device Type: See Product Selector Guide.

| Valid Combinations | |
|---|---|
| Am3101<br>Am3101A<br>Am31L01<br>Am31L01A<br>Am3101-1 | PC,<br>DC, DCB,<br>LC, LCB,<br>DM, DMB,<br>FM, FMB,<br>LM, LMB |

**For 7489 family devices**

**Am54S189 W B**

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- W — Package: J – 16-pin ceramic DIP; N – 16-pin plastic DIP; W – 16-pin flatpak; L – 20-pin leadless chip carrier
- Am54S189 — Device Type: See Product Selector Guide.

| Valid Combinations | |
|---|---|
| Am7489<br>Am74S189<br>Am74S289 | N, J, JB,<br>LC*, LCB* |
| Am5489<br>Am54S189<br>Am54S289 | J, JB, W, WB<br>LM*, LMB* |
| *LC, LCB, LM, LMB suffixes are identical to those of the 3101 family. | |

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03203B

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage to Ground Potential
(Pin 18 to Pin 8) ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State ..... −0.5V to $V_{CC}$ max
DC input voltage ..... −0.5V to +5.5V
Output Current, into Outputs ..... 20mA
DC input Current ..... −30mA to +5.0mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameters | Test Conditions | | | All Other Part No: Min | Typ | Max | 31L01A/31L01 Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ (Note 2) | Output HIGH Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −5.2mA | COM'L | 2.4 | 3.2 | | | | | Volts |
| | | | $I_{OH}$ = −2.0mA | MIL | | | | | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16mA (STD) $I_{OL}$ = 8mA (L) | | | 350 | 450 | | 280 | 450 | mV |
| | | | $I_{OL}$ = 20mA (STD) $I_{OL}$ = mA (L) | | | 380 | 500 | | 310 | 500 | |
| $V_{IH}$ | Input HIGH Level | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3) | | | 2.0 | | | 2.0 | | | Volts |
| $V_{IL}$ | Input LOW Level | Guaranteed Input Logical LOW Voltage for all Inputs (Note 3) | | | | | | | | 0.8 | |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = MAX, $V_{IN}$ = 0.40V | $\overline{WE}$, $D_0 - D_3$, $A_0 - A_3$ | | | −15 | −250 | | −30 | −250 | µA |
| | | | $\overline{CS}$ | | | −30 | −250 | | −30 | −250 | |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = MAX, $V_{IN}$ = 2.4V | | | | 0 | 10 | | 0 | 10 | µA |
| $I_{SC}$ (Note 2) | Output Short Circuit Current | $V_{CC}$ = MAX, $V_{OUT}$ = 0.0V (Note 4) | | | −20 | −45 | −90 | | | | mA |
| $I_{CC}$ | Power Supply Current | All Inputs = GND $V_{CC}$ = MAX | | COM'L | | 75 | 100 | | 25 | 35 | |
| | | | | MIL | | 75 | 105 | | 25 | 38 | |
| $V_{CL}$ | Input Clamp Voltage | $V_{CC}$ = MIN, $I_{IN}$ = −18mA | | | | −0.85 | −1.2 | | −0.85 | −1.2 | Volts |
| $I_{CEX}$ | Output Leakage Current | $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{OUT}$ = 2.4V | | | | 0 | 40 | | 0 | 40 | µA |
| | | $\overline{CS}$ = $V_{IH}$ or $\overline{WE}$ = $V_{IL}$ $V_{OUT}$ = 0.4V, $V_{CC}$ = MAX | | (Note 2) | −40 | 0 | | | | | |

Notes:

1. Typical limits are at $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. This applies to three-state devices only.
3. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

**SWITCHING TEST CIRCUIT**

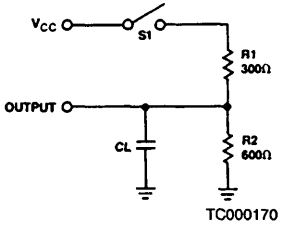



Figure 3

**SWITCHING TEST WAVEFORM**

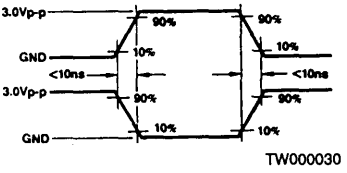
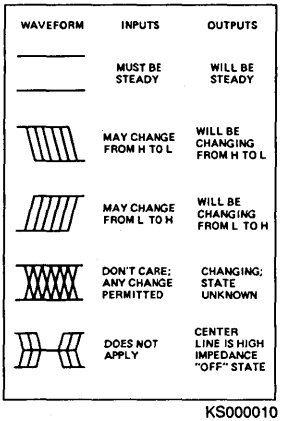



Figure 4

**KEY TO SWITCHING WAVEFORMS**




3

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

**Standard Power Delves**

| No. | Symbol | Description | Am3101-1•Am54/7489-1 C devices Min | Am3101-1•Am54/7489-1 C devices Max | Am3101-1•Am54/7489-1 M devices Min | Am3101-1•Am54/7489-1 M devices Max | Am3101•Am54/7489 C devices Min | Am3101•Am54/7489 C devices Max | Am3101•Am54/7489 M devices Min | Am3101•Am54/7489 M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output | | 35 | | 50 | | 50 | | 60 | ns |
| 2 | $t_{PHL}(A)$ | | | | | | | | | | |
| 3 | $t_{PZL}(\overline{CS})$ | Delay from Chip Select (LOW) to Active Output and Correct Data | | 17 | | 25 | | 30 | | 40 | ns |
| 4 | $t_{PZL}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2) | | 35 | | 50 | | 50 | | 60 | ns |
| 5 | $t_s(A)$ | Setup Time Address (Prior to Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 6 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 7 | $t_s(DI)$ | Setup Time Data Input (Prior to Initiation of Write) | 25 | | 25 | | 30 | | 30 | | ns |
| 8 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 9 | $t_{pw}(\overline{WE})$ | MIN Write Enable Pulse Width to Insure Write | 25 | | 25 | | 30 | | 30 | | ns |
| 10 | $t_{PLZ}(\overline{CS})$ | Delay from Chip Select (HIGH) to Inactive Output (Hi-Z) | | 17 | | 25 | | 30 | | 40 | ns |
| 11 | $t_{PLH}(DI)$ | Delay from Data Input to Correct Data Output ($\overline{WE} = \overline{CS} = V_{IL}$) | | 35 | | 50 | | 50 | | 60 | ns |
| 12 | $t_{PHL}(DI)$ | | | | | | | | | | |

Notes:

1. Output is conditioned to data in (inverted) during write to insure correct data is present on all outputs during write and after write is terminated.
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with $S_1$ closed and $C_L = 30pF$ with both input and output timing referenced to 1.5V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output ($D_{OUT}$), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed and $C_L = 30pF$; and with both the input and output timing referenced to 1.5V.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am3101A•Am54S/74S189 C devices Min | Am3101A•Am54S/74S189 C devices Max | Am3101A•Am54S/74S189 M devices Min | Am3101A•Am54S/74S189 M devices Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output | | 35 | | 50 | ns |
| 2 | $t_{PHL}(A)$ | | | | | | |
| 3 | $t_{PZH}(\overline{CS})$ | Delay from Chip Select (LOW) to Active Output and Correct Data | | 17 | | 25 | ns |
| 4 | $t_{PZL}(\overline{CS})$ | | | | | | |
| 5 | $t_{PZH}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2) | | 35 | | 40 | ns |
| 6 | $t_{PZL}(\overline{WE})$ | | | | | | |
| 7 | $t_s(A)$ | Setup Time Address (Prior to Initiation of Write) | 0 | | 0 | | ns |
| 8 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 0 | | 0 | | ns |
| 9 | $t_s(DI)$ | Setup Time Data Input (Prior to Termination of Write) | 25 | | 25 | | |
| 10 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 0 | | 0 | | ns |
| 11 | $t_{pw}(\overline{WE})$ | MIN Write Enable Pulse Width to Insure Write | 25 | | 25 | | ns |
| 12 | $t_{PHZ}(\overline{CS})$ | Delay from Chip Select (HIGH) to Inactive Output (Hi-Z) | | 17 | | 25 | ns |
| 13 | $t_{PLZ}(\overline{CS})$ | | | | | | |
| 14 | $t_{PLZ}(\overline{WE})$ | Delay from Write Enable (LOW) to Inactive Output (Hi-Z) | | 35 | | 50 | |
| 15 | $t_{PHZ}(\overline{WE})$ | | | | | | |

Notes:

1. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs during write and after write is terminated. (No recovery glitch.)
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with $S_I$ closed and $C_L$ = 30pF with both input and output timing referenced to 1.5V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output ($D_{OUT}$), $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}$ ($\overline{WE}$) and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed and $C_L$ = 30pF; and with both the input and output timing referenced to 1.5V.
4. For three-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with $S_1$ open. $C_L$ = 30pF and with both the input and output timeing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed. $C_L$=30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with $S_1$ open and $C_L \leqslant$ 5pF and are measured between the 1.5V level on the input to the $V_{OH}$ – 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with $S_1$ closed and $C_L \leqslant$ 5pF and are measured between the 1.5V level on the input and the $V_{OL}$ + 500mV level on the output.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

**Low Power Devices**

| No. | Symbol | Description | Am31L01A C devices Min | Am31L01A C devices Max | Am31L01A M devices Min | Am31L01A M devices Max | 31L01 C devices Min | 31L01 C devices Max | 31L01 M devices Min | 31L01 M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{PLH}(A)$ | Delay from Address to Output | | 55 | | 65 | | 80 | | 90 | ns |
| 2 | $t_{PHL}(A)$ | | | | | | | | | | |
| 3 | $t_{PZL}(\overline{CS})$ | Delay from Chip Select to Active Output and Correct Data | | 30 | | 35 | | 60 | | 70 | ns |
| 4 | $t_{PZL}(\overline{WE})$ | Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery) (Note 2) | | 30 | | 35 | | 80 | | 100 | ns |
| 5 | $t_s(A)$ | Setup Time Address (Prior to Initiation of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 6 | $t_h(A)$ | Hold Time Address (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 7 | $t_s(DI)$ | Setup Time Data Input (Prior to Initiation of Write) | 45 | | 55 | | 60 | | 80 | | ns |
| 8 | $t_h(DI)$ | Hold Time Data Input (After Termination of Write) | 0 | | 0 | | 0 | | 0 | | ns |
| 9 | $t_{pw}(\overline{WE})$ | Min Write Enable Pulse Width to Insure Write | 45 | | 55 | | 60 | | 80 | | ns |
| 10 | $t_{PLZ}(\overline{CS})$ | Delay from Chip Select to Inactive Output (HIGH-Z) | | 30 | | 35 | | 50 | | 60 | ns |
| 11 | $t_{PLH}(DI)$ | Delay from Data Input to Correct Data Output ($\overline{WE}$ = $\overline{CS}$=$V_{1L}$ | | 55 | | 65 | | 80 | | 90 | ns |
| 12 | $t_{PHL}(DI)$ | | | | | | | | | | |

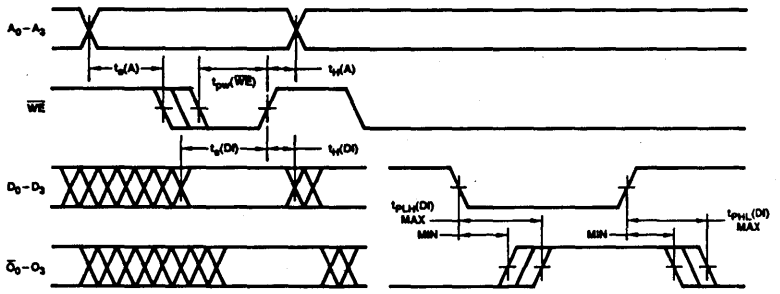
## SWITCHING CHARACTERISTICS (Cont.)

Notes:

1. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch.)
2. $t_{PLH}(A)$ and $t_{PHL}(A)$ are tested with $S_1$ closed and $C_L$ = 30pF with both input and output timing referenced to 1.5V.
3. For open collector, all delays from Write Enable ($\overline{WE}$) or Chip Select ($\overline{CS}$) inputs to the Data Output ($D_{OUT}$, $t_{PLZ}(\overline{WE})$, $t_{PLZ}(\overline{CS})$, $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed and $C_L$ = 30pF; and with both the input and output timing referenced to 1.5V.
4. For three-state output, $t_{PZH}(\overline{WE})$ and $t_{PZH}(\overline{CS})$ are measured with $S_1$ open, $C_L$ = 30pF and with both the input and output timing referenced to 1.5V. $t_{PZL}(\overline{WE})$ and $t_{PZL}(\overline{CS})$ are measured with $S_1$ closed, $C_L$ = 30pF and with both the input and output timing referenced to 1.5V. $t_{PHZ}(\overline{WE})$ and $t_{PHZ}(\overline{CS})$ are measured with $S_1$ open and $C_L \leq 5$pF and are measured between the 1.5V level on the input to the $V_{OH}$ − 500mV level on the output. $t_{PLZ}(\overline{WE})$ and $t_{PLZ}(\overline{CS})$ are measured with $S_1$ closed and $C_L \leq 5$pF and are measured between the 1.5V level on the input and the $V_{OL}$ + 500mV level on the output.

## SWITCHING WAVEFORMS

### WRITE MODE

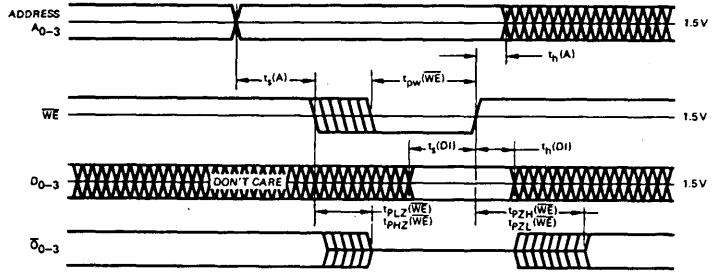



WF001080

Write Cycle Timing. The cycle is initiated by an address change. After $t_S(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive (floating for the Am54S/74S189) while the write enable is ($\overline{WE}$) LOW.

**Am3101-1/54/7489-1/3101/54/7489**

### WRITE MODE



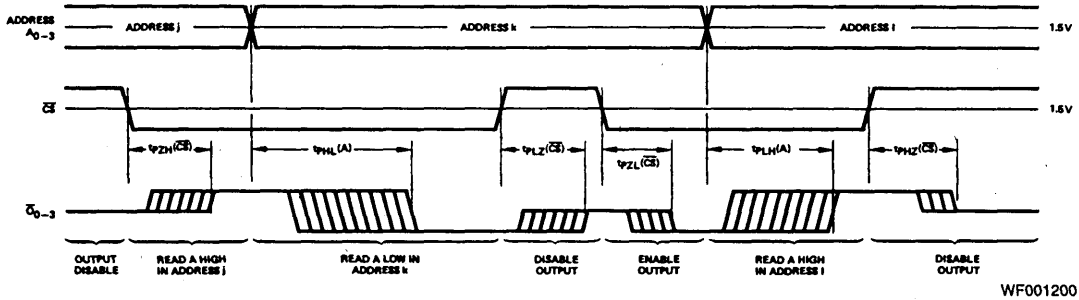

WF001110

Write Cycle Timing. The cycle is initiated by an address change. After $t_S(A)$ min, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min must be allowed before the address may be changed again. The output will be inactive (floating for the Am54S/74S189) while the write enable is ($\overline{WE}$) LOW.

**3101A/54S/74S289/54S/74S189**

## SWITCHING WAVEFORMS (Cont.)

### READ MODE

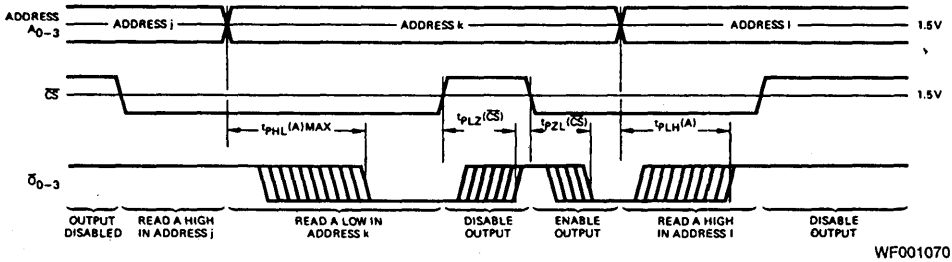



WF001200

Switching delays from address and chip select inputs to the data output. For the Am54S/74S189 disabled output is "OFF", represented by a single center line. For the Am3101A/Am54S/74S289, a disabled output is HIGH.

**Am3101A/54S/74S289/54S/74S189**

### READ MODE




WF001070

Switching delays from address and chihp select inputs to the data output. For the Am31L01, a disabled output is HIGH.

**Am31L01A/31L01**

# Replacement Referrals

| Part Number | Replaced by |
|---|---|
| Am29702 | Am27S02 |
| Am29703 | Am27S03 |
| Am29700 | Am27S06A |
| Am29701 | Am27S07A |
| Am29720 | Am27LS01 |
| Am29721 | Am27LS00 |

# MOS Random Access Memories (RAM) Index

# Am21L41

4096 x 1 Static RAM

## DISTINCTIVE CHARACTERISTICS

- Fully static storage and interface circuitry
- Automatic power-down when deselected
- Low power dissipation
  - Am21L41; 220mW active, 27.5mW power down
- High output drive
- TTL compatible interface levels
- No power-on current surge

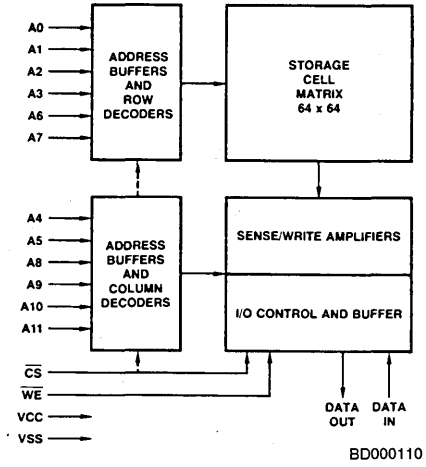
## GENERAL DESCRIPTION

The Am21L41 is a high performance, 4096-bit, static, read/write, random access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard Schottky TTL loads or up to six standard TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CS} \geqslant VIH$), the Am21L41 automatically enters a power-down mode which reduces power dissipation by as much as 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a 3-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

## BLOCK DIAGRAM



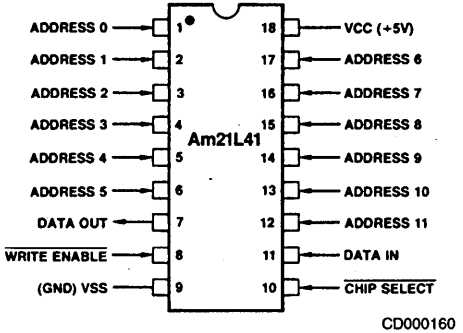

BD000110

## PRODUCT SELECTOR GUIDE

| Part Number | Am21L41-12 | Am21L41-15 | Am21L41-20 | Am21L41-25 |
|---|---|---|---|---|
| Maximum Access Time (ns) | 120 | 150 | 200 | 250 |
| Maximum Active Current (mA) | 55 | 40 | 40 | 40 |
| Maximum Standby Current (mA) | 10 | 5 | 5 | 5 |

03078B

## CONNECTION DIAGRAM
### Top View

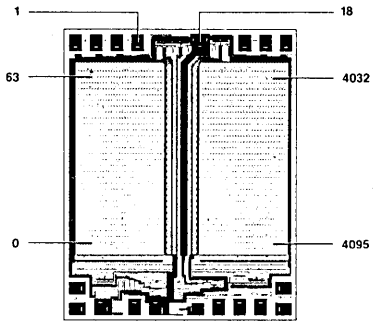



CD000160

Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| $A_0$ | $A_2$ |
| $A_1$ | $A_5$ |
| $A_2$ | $A_4$ |
| $A_3$ | $A_3$ |
| $A_4$ | $A_8$ |
| $A_5$ | $A_7$ |
| $A_6$ | $A_1$ |
| $A_7$ | $A_0$ |
| $A_8$ | $A_{11}$ |
| $A_9$ | $A_9$ |
| $A_{10}$ | $A_{10}$ |
| $A_{11}$ | $A_6$ |




DIE SIZE: 0.130 x 0.106

**Figure 2. Bit Mapping Information**

## ORDERING INFORMATION

**Am21L41-12 P C**

- C — Temperature: C – Commercial (0°C to +70°C)
- P — Package: D – 18-pin CERDIP; P – 18-pin plastic DIP
- 12 — Speed Select: 12 – 120ns; 15 – 150ns; 20 – 200ns; 25 – 250ns
- Am21L41 — Device Type: 4k x 1 SRAM

| Valid Combinations | |
|---|---|
| Am21l41-12<br>Am21l41-15<br>Am21l41-20<br>Am21l41-25 | DC,PC |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... 0°C to +70°C
Supply Voltage ..... −0.5V to +7.0V
All Signal Voltage with
respect to ground ..... −1.5V to +7.0V
Power Description ..... 1.2W
DC Output Current ..... 20mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Temperature ..... 0°C to +70°C

Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

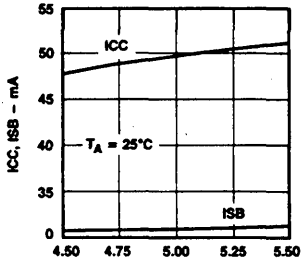
| Symbol | Parameter | Test Conditions | | Am21L41-12 Min | Am21L41-12 Max | Am21L41-15 Am21L41-20 Am21L41-25 Min | Am21L41-15 Am21L41-20 Am21L41-25 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | $V_{CC}$ = 4.5V | −4 | | −4 | | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | $T_A$ = 70°C | 8 | | 8 | | mA |
| $V_{IH}$ | Input High Voltage | | | 2.0 | 6.0 | 2.0 | 6.0 | Volts |
| $V_{IL}$ | Input Low Voltage | | | −3.0 | 0.8 | −3.0 | 0.8 | Volts |
| $I_{IX}$ | Input Load Current | $V_{SS} \leq V_I \leq V_{CC}$ | | | 10 | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND $\leq V_O \leq V_{CC}$ Output Disabled | $T_A$ = 70°C | −10 | 10 | −10 | 10 | µA |
| $I_{OS}$ | Output Short Circuit Current | GND $\leq V_O \leq V_{CC}$ (Note 2) | 0 to+ 70°C | −120 | 120 | −120 | 120 | mA |
| $C_I$ | Input Capacitance (Note 1) | Test Frequency = 1.0 MHz $T_A$ = 25°C, All pins at 0V | | | 5.0 | | 5.0 | pF |
| $C_O$ | Output Capacitance (Note 1) | | | | 6.0 | | 6.0 | |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | Max $V_{CC}$, $\overline{CS} \leq V_{IL}$ | $T_A$ = 0°C | | 55 | | 40 | mA |
| $I_{SB}$ | Automatic $\overline{CS}$ Power Down Current | Max $V_{CC}$, (CS $\leq V_{IH}$) (Note 5) | | | 10 | | 5.0 | mA |

Notes:

1. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
2. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.5V and output loading of the specified IOL/IOH and $C_L$ = 30pF load capacitance (reference Figure 1.).
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. A pull up resistor to VCC on the $\overline{CS}$ input is required to keep the device deselected during VCC power up otherwise ISB will exceed values given.
6. Chip deselected greater than 55ns prior to selection.
7. Chip deselected less than 55ns prior to selection.
8. At any given temperature and voltage condition, tHZ is less than tLZ for all devices. Transition is measured at VOH −500mV and VOL +500mV levels on the output from 1.5V level on the input with load shown in Figure 1 using CL = 5pF.
9. $\overline{WE}$ is high for read cycle.
10. Device is continuously selected, $\overline{CS}$ = VIL.
11. Address valid prior to or coincident with $\overline{CS}$ transition low.

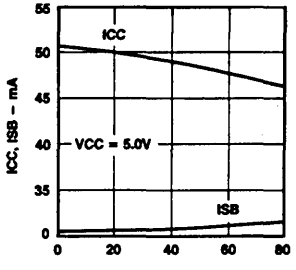
## DC OPERATING CHARACTERISTICS

### Supply Current Versus Supply Voltage



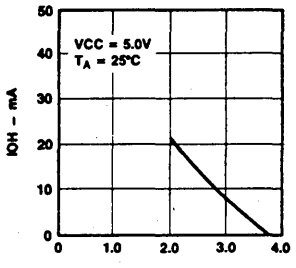

OP000820

### Supply Current Versus Ambient Temperature



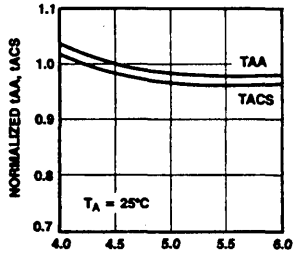

OP000830

### Output Source Current Versus Output Voltage



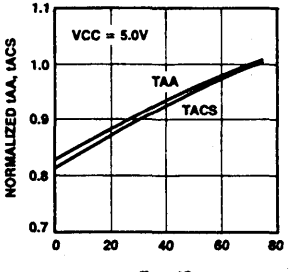

OP000840

### Normalized Access Time Versus Supply Voltage



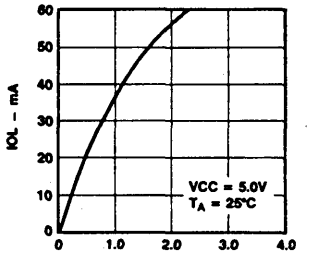

OP000760

### Normalized Access Time Versus Ambient Temperature



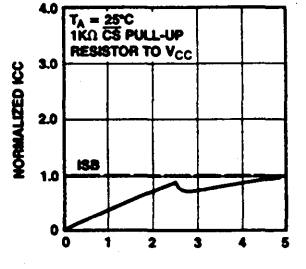

OP000850

### Output Sink Current Versus Output Voltage



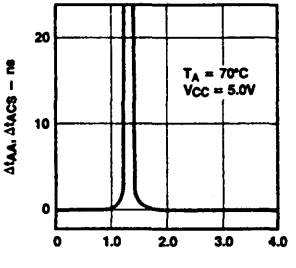

OP000860

### Typical Power-On Current Versus Power Supply



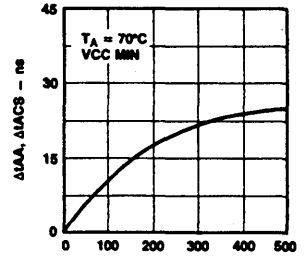

OP000870

### Access Time Change Versus Input Voltage



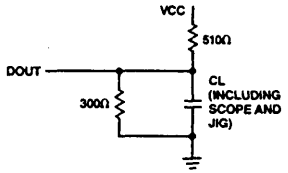

OP000800

### Access Time Change Versus Output Loading




OP000880

## SWITCHING TEST CIRCUIT




TC000030

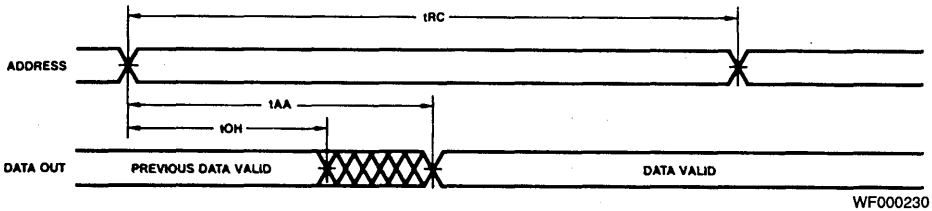
**Figure I. Output Load**

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | Am21L41-12 Min | Am21L41-12 Max | Am21L41-15 Min | Am21L41-15 Max | Am21L41-20 Min | Am21L41-20 Max | Am21L41-25 Min | Am21L41-25 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | | | |
| 1 | $t_{RC}$ | Address Valid to Address Do Not Care Time (Read Cycle Time) | | 120 | | 150 | | 200 | | 250 | | ns |
| 2 | $t_{AA}$ | Address Valid to Data Out Valid Delay (Address Access Time) | | | 120 | | 150 | | 200 | | 250 | ns |
| 3 | $t_{ASC1}$ | Chip Select Low to Data Out Valid | Note 6 | | 120 | | 150 | | 200 | | 250 | ns |
| 4 | $t_{ASC2}$ | | Note 7 | | 130 | | 160 | | 200 | | 250 | ns |
| 5 | $t_{LZ}$ | Chip Select Low to Data Out On (Note 8) | | 10 | | 10 | | 10 | | 10 | | ns |
| 6 | $t_{HZ}$ | Chip Select High to Data Out Off (Note 8) | | 0 | 60 | 0 | 60 | 0 | 60 | 0 | 60 | ns |
| 7 | $t_{OH}$ | Address Unknown to Data Out Unknown Time | | 10 | | 10 | | 10 | | 10 | | ns |
| 8 | $t_{PD}$ | Chip Select High to Power Low Delay | | | 60 | | 60 | | 60 | | 60 | ns |
| 9 | $t_{PU}$ | Chip Select Low to Power High Delay | | 0 | | 0 | | 0 | | 0 | | ns |
| **Write Cycle** | | | | | | | | | | | | |
| 10 | $t_{WC}$ | Address Valid to Address Do Not Care Time (Write Cycle Time) | | 120 | | 150 | | 200 | | 250 | | ns |
| 11 | $t_{WP}$ | Write Enable Low to Write Enable High Time (Note 4) | | 60 | | 60 | | 60 | | 75 | | ns |
| 12 | $t_{WR}$ | Write Enable High to Address Do Not Care Time | | 10 | | 15 | | 20 | | 20 | | ns |
| 13 | $t_{WZ}$ | Write Enable Low to Data Out Off Delay (Note 8) | | 0 | 70 | 0 | 80 | 0 | 80 | 0 | 80 | ns |
| 14 | $t_{DW}$ | Data in Valid to Write Enable High Time | | 50 | | 60 | | 60 | | 75 | | ns |
| 15 | $t_{DH}$ | Write Enable Low to Data In Do Not Care Time | | 10 | | 10 | | 10 | | 10 | | ns |
| 16 | $t_{AS}$ | Address Valid to Write Enable Low Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 17 | $t_{CW}$ | Chip Select Low to Write Enable High Time (Note 4) | | 110 | | 135 | | 180 | | 230 | | ns |
| 18 | $t_{OW}$ | Write Enable High to Output Turn On (Note 8) | | 0 | | 0 | | 0 | | 0 | | ns |
| 19 | $t_{AW}$ | Address Valid to End of Write | | 110 | | 135 | | 180 | | 230 | | ns |

## SWITCHING WAVEFORMS

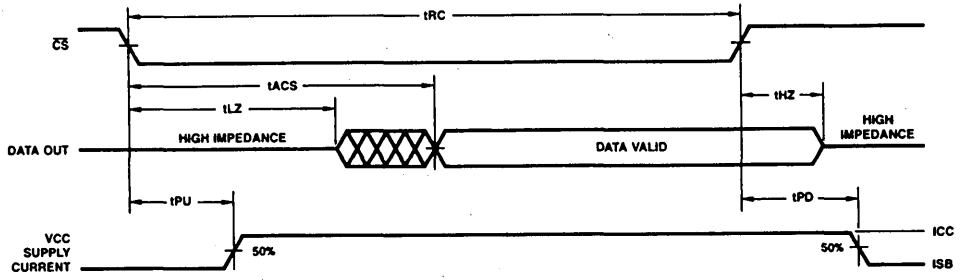
### READ CYCLE NO. 1 (Notes 9, 10)




WF000230

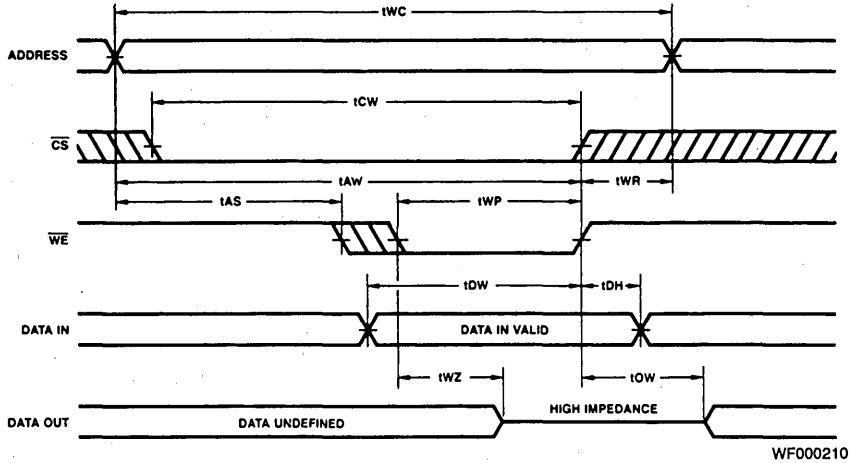
## SWITCHING WAVEFORMS (Cont.)

### READ CYCLE NO. 2 (Notes 9, 11)



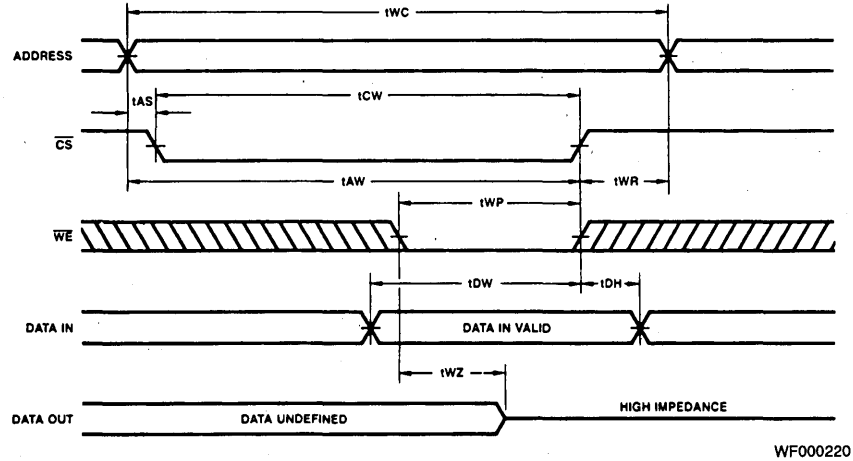

WF000240

### WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)




WF000210

### WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)




WF000220

Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

# Am2147

4096 x 1 Static RAM

## DISTINCTIVE CHARACTERISTICS

- High speed — access times down to 35ns maximum
- Automatic power-down when deselected
- Low power dissipation
- High output drive
- TTL compatible interface levels
- No power-on current surge

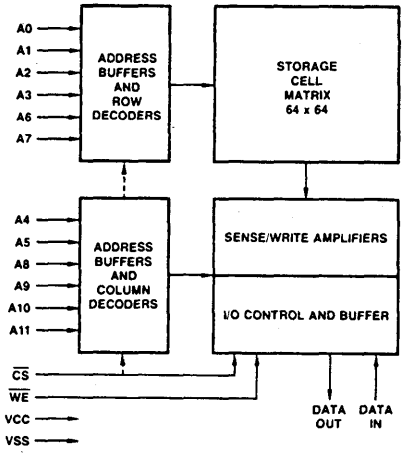
## GENERAL DESCRIPTION

The Am2147 is a high performance, 4096-bit, static, read/write, random access memory. It is organized as 4096 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to seven standard TTL loads or up to six Schottky TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CS} \geq V_{IH}$), the Am2147 automatically enters a power-down mode which reduces power dissipation by more than 85%. When selected, the chip powers up again with no access time penalty.

Data In and Data Out use separate pins on the standard 18-pin package. Data Out is the same polarity as Data In. Data Out is a 3-state signal allowing wired-or operation of several chips. Data In and Data Out may be connected together for operation in a common data bus environment.

## BLOCK DIAGRAM




BD000050

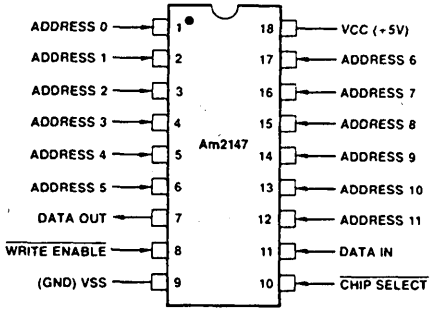
## PRODUCT SELECTOR GUIDE

| Part Number | Am2147-35 | Am2147-45 | Am21L47-45 | Am2147-55 | Am21L47-55 | Am2147-70 | Am21L47-70 |
|---|---|---|---|---|---|---|---|
| Maximum Access time (ns) | 35 | 45 | 45 | 55 | 55 | 70 | 70 |
| Maximum Active Current (mA) | 180 | 180 | 125 | 180 | 125 | 160 (180 mil) | 125 |
| Maximum Standby Current (mA) | 30 | 30 | 15 | 30 | 15 | 20 (30 mil) | 15 |
| Full Military Operating Range Version | | Yes | | Yes | | Yes | |

01940C

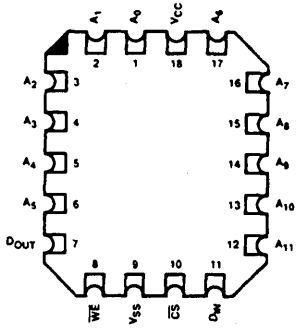
## CONNECTION DIAGRAM
Top View

### DIP




CD000090

### Chip-Pak™ L-18-2

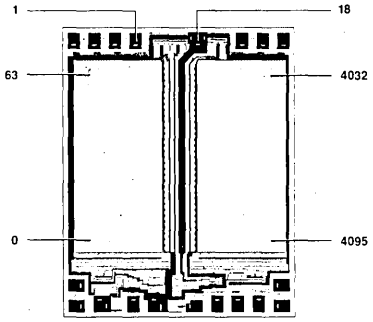



CD000100

Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| $A_0$ | $A_2$ |
| $A_1$ | $A_5$ |
| $A_2$ | $A_4$ |
| $A_3$ | $A_3$ |
| $A_4$ | $A_8$ |
| $A_5$ | $A_7$ |
| $A_6$ | $A_1$ |
| $A_7$ | $A_0$ |
| $A_8$ | $A_{11}$ |
| $A_9$ | $A_9$ |
| $A_{10}$ | $A_{10}$ |
| $A_{11}$ | $A_6$ |




DIE SIZE: 0.130 x 0.106

**Figure 2. Bit Mapping Information**

## ORDERING INFORMATION

**Am2147-35 D C B**

- B — Burn-in Option
  - B suffix indicates 160 hour burn-in
- Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 18-pin CERDIP
  - L – 18-pin leadless chip carrier
  - F – 18-Pin flatpak
- Speed Select
  - 35 – 35ns
  - 45 – 45ns
  - 55 – 55ns
  - 70 – 70ns
- Device Type
  - Am2147 – 4k x 4 SRAM
  - Am21L47 – Same, Low Power

| Valid Combinations | | |
|---|---|---|
| Am2147-35 (2147 only) | | DC, DCB, LC |
| -45 | Am2147 | DC, DCB, DM DMB LC, LM, LMB |
| | Am21L47 | DC, DCB, LC |
| -55 | Am2147 | DC, DM, FM LC, LM, DCB DMB, FMB LCB, LMB |
| | Am21L47 | DC, DCB, LC |
| -70 | Am2147 | DC, DCB, DM DMB, LC, LCB LM, LMB |
| | Am21L47 | DC, DCB, LC |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
Signal Voltages with
respect to ground ..... −3.5V to +7.0V
Power Description ..... 1.2W
DC Output Current ..... 20mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

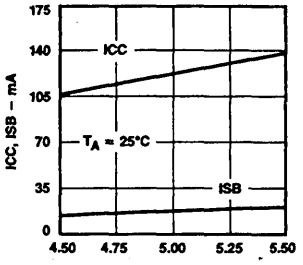
| Symbol | Parameter | Test Conditions | | Am2147-35 Am2147-45 Am2147-55 Min | Am2147-35 Am2147-45 Am2147-55 Max | Am21L47-45 Am21L47-55 Am21L47-70 Min | Am21L47-45 Am21L47-55 Am21L47-70 Max | Am2147-70 Min | Am2147-70 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | $V_{CC}$ = 4.5V | −4 | | −4 | | −4 | | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | $T_A$ = 70°C | 12 | | 12 | | 12 | | mA |
| | | | $T_A$ = 125°C | 8 | | N/A | | 8 | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | 6.0 | 2.0 | 6.0 | 2.0 | 6.0 | Volts |
| $V_{IL}$ | Input Low Voltage | | | −3.0 | 0.8 | −3.0 | 0.8 | −3.0 | 0.8 | Volts |
| $I_{IX}$ | Input Load Current | $V_{SS} \leq V_I \leq V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O \leq V_{CC}$ Output Disables | $T_A$ = −55 to+ 125°C | −50 | 50 | −50 | 50 | −50 | 50 | µA |
| $C_I$ | Input Capacitance | Test Frequency = 1.0 MHz $T_A$ = 25°C, All pins at 0V, $V_{CC}$ = 5V | | | 5 | | 5 | | 5 | pF |
| $C_O$ | Output Capacitance | | | | 6 | | 6 | | 6 | |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | Max $V_{CC}$ $\overline{CS} \leq V_{IL}$ Output Open | $T_A$ = 70°C | | 155 | | 105 | | 135 | mA |
| | | | $T_A$ = 0°C | | 180 | | 125 | | 160 | |
| | | | $T_A$ = −55°C | | 180 | | N/A | | 180 | |
| $I_{SB}$ | Automatic $\overline{CS}$ Power Down Current | Max $V_{CC}$, ($\overline{CS} \geq$ $V_{IH}$) (Note 3) | $T_A$ = 0 to 70°C | | 30 | | 15 | | 20 | mA |
| | | | $T_A$ = −55 to+ 125°C | | 30 | | N/A | | 30 | |

Notes:

1. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified $I_{OL}/I_{OH}$ and 30pF load capacitance. Output timing reference is 1.5V for 2147-35 and 0.8/2.0V for −45, −55 and −70 parts.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to $V_{CC}$ on the $\overline{CS}$ input is required to keep the device deselected during $V_{CC}$ power up. Otherwise $I_{SB}$ will exceed values given.
4. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
5. Chip deselected greater than 55ns prior to selection.
6. chip deselected less than 55ns prior to selection.
7. At any given temperature and voltage condition, $t_{HZ}$ is less than $t_{LZ}$ for all devices. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.

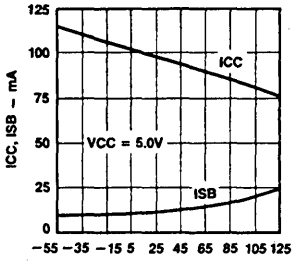
## DC OPERATING CHARACTERISTICS

### Supply Current Versus Supply Voltage



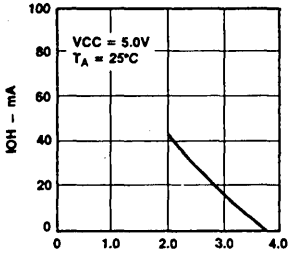

OP000430

### Supply Current Versus Ambient Temperature



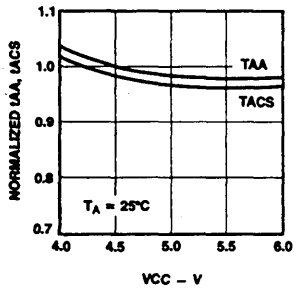

OP000440

### Output Source Current Versus Output Voltage



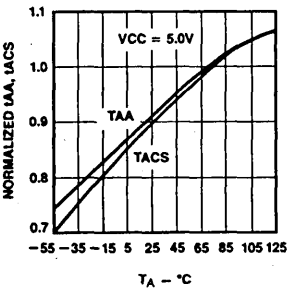

OP000220

### Normalized Access Time Versus Supply Voltage



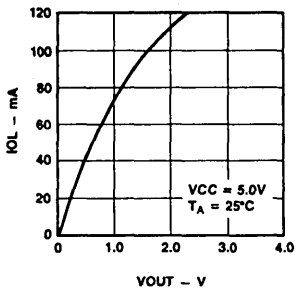

OP000760

### Normalized Access Time Versus Ambient Temperature



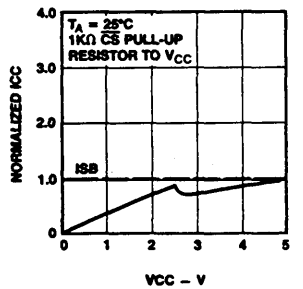

OP000230

### Output Sink Current Versus Output Voltage



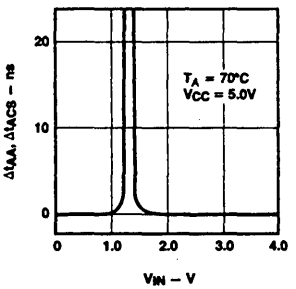

OP000240

### Typical Power-On Current Versus Power Supply



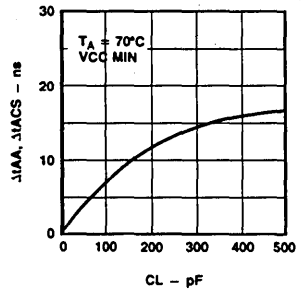

OP000870

### Access Time Change Versus Input Voltage




OP000800

### Access Time Change Versus Output Loading




OP000270

## SWITCHING TEST CIRCUITS

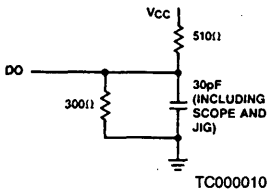



**Figure 1. Output Load**

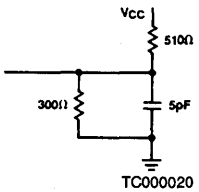



**Figure 2. Output Load for $t_{HZ}$, $t_{LZ}$, $t_{OW}$, $t_{WZ}$**

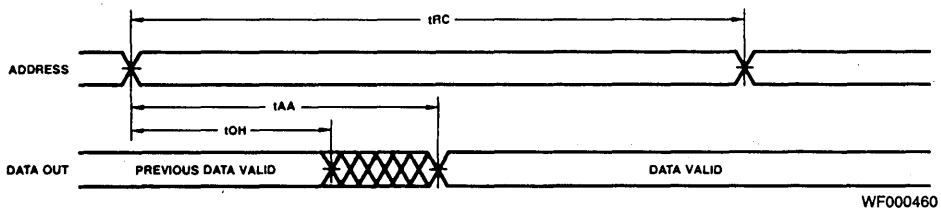
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am2147-35 Min | Am2147-35 Max | Am2147-45 Am21L47-45 Min | Am2147-45 Am21L47-45 Max | Am2147-55 Am21L47-55 Min | Am2147-55 Am21L47-55 Max | Am2147-70 Am21L47-70 Min | Am2147-70 Am21L47-70 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | | |
| 1 | $t_{RC}$ | Address Valid to Address Do Not Care Time (Read Cycle Time) | 35 | | 45 | | 55 | | 70 | | ns |
| 2 | $t_{AA}$ | Address Valid to Data Out Valid Delay (Address Access Time) | | 35 | | 45 | | 55 | | 70 | ns |
| 3 | $t_{ACS1}$ | Chip Select Low to Data Out Valid — Note 5 | | 35 | | 45 | | 55 | | 70 | ns |
| 4 | $t_{ACS2}$ | Chip Select Low to Data Out Valid — Note 6 | | 35 | | 45 | | 65 | | 80 | ns |
| 5 | $t_{LZ}$ | Chip Select Low to Data Out On (Note 7) | 5 | | 5(10*) | | 10 | | 10 | | ns |
| 6 | $t_{HZ}$ | Chip Select High to Data Out Off (Note 7) | 0 | 30 | 0 | 30 | 0 | 30 | 0 | 40 | ns |
| 7 | $t_{OH}$ | Address Unknown to Data Out Unknown Time | 5 | | 5 | | 5 | | 5 | | ns |
| 8 | $t_{PD}$ | Chip Select High Power Down Delay | | 20 | | 20 | | 20 | | 30 | ns |
| 9 | $t_{PU}$ | Chip Select Low to Power Up Delay | 0 | | 0 | | 0 | | 0 | | ns |
| **Write Cycle** | | | | | | | | | | | |
| 10 | $t_{WC}$ | Address Valid to Address Do Not Care (Write Cycle Time) | 35 | | 45 | | 55 | | 70 | | ns |
| 11 | $t_{WP}$ | Write Enable Low to Write Enable High (Note 2) | 20 | | 25 | | 25 | | 40 | | ns |
| 12 | $t_{WR}$ | Write Enable High to Address | 0 | | 0 | | 10 | | 15 | | ns |
| 13 | $t_{WZ}$ | Write Enable Low to Output in High Z (Note 6) | 0 | 20 | 0 | 25 | 0 | 25 | 0 | 35 | ns |
| 14 | $t_{DW}$ | Data In Valid to Write Enable High | 20 | | 25 | | 25 | | 30 | | ns |
| 15 | $t_{DH}$ | Data Hold Time | 10 | | 10 | | 10 | | 10 | | ns |
| 16 | $t_{AS}$ | Address Valid to Write Enable Low | 0 | | 0 | | 0 | | 0 | | ns |
| 17 | $t_{CW}$ | Chip Select Low to Write Enable High (Note 2) | 35 | | 45 | | 45 | | 55 | | ns |
| 18 | $t_{OW}$ | Write Enable High to Output in Low Z (Note 6) | 0 | | 0 | | 0 | | 0 | | ns |
| 19 | $t_{AW}$ | Address Valid to End of Write | 35 | | 45 | | 45 | | 55 | | ns |

*Military version only.

## SWITCHING WAVEFORMS

### READ CYCLE NO. 1 (Notes 8, 9)

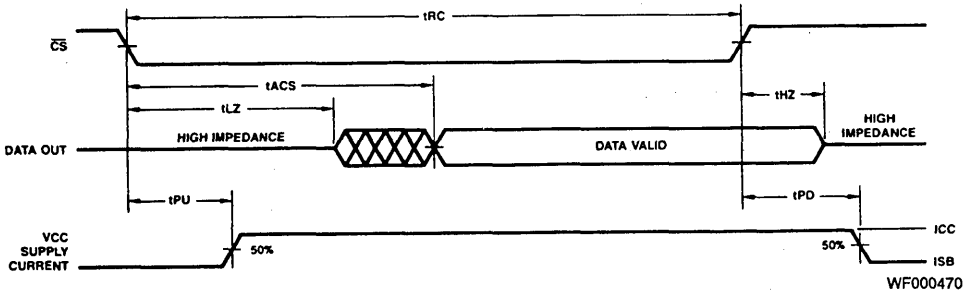





01940C

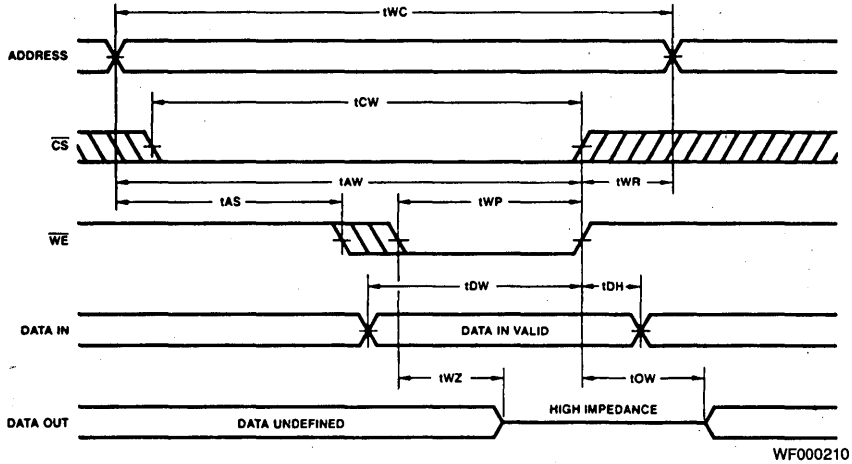
## SWITCHING WAVEFORMS (Cont.)

### READ CYCLE NO. 2 (Notes 8, 10)



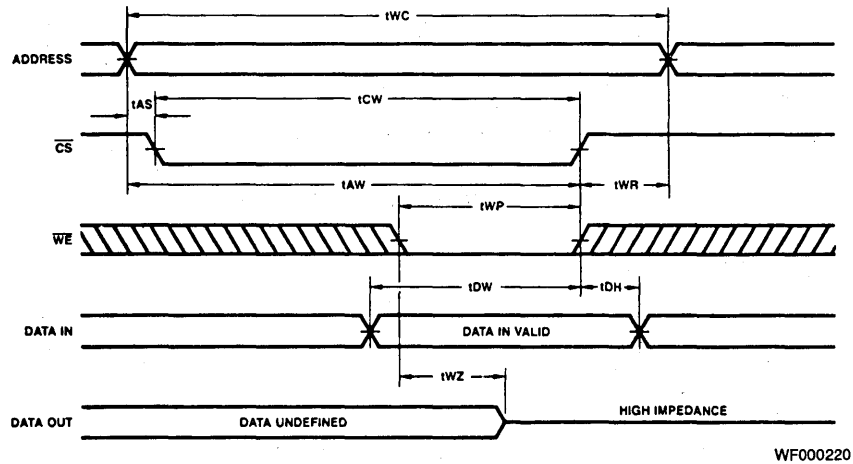

WF000470

### WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)




WF000210

### WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)




WF000220

Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

# Am2148/49

1024 x 4 Static RAM

## DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35ns
- Fully static storage and interface circuitry
- Automatic power-down when deselected (Am2148)
- TTL compatible interface levels
- Low power dissipation
  - Am2148: 990mW active, 165mW power down
  - Am21L48: 688mW active, 110mW power down
- High output drive
  - Up to seven standard TTL loads

## GENERAL DESCRIPTION

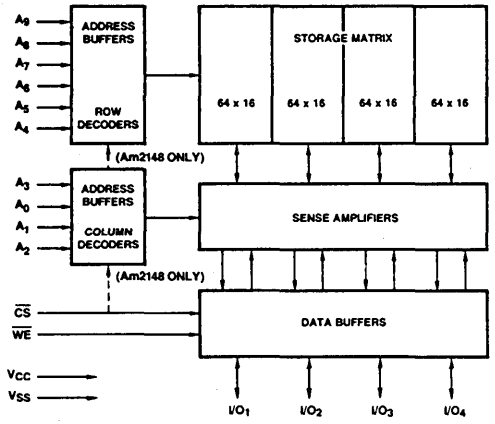
The Am2148 and Am2149 are high performance, static, N-Channel, read/write, random access memories, organized as 1024 x 4. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. The Am2148 and Am2149 are the same except that the Am2148 offers an automatic $\overline{CS}$ power down feature.

The Am2148 remains in a low-power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements.

The Am2148 power decreases from 990mW to 165mW in the standby mode. The $\overline{CS}$ input does not affect the power dissipation of the Am2149.

Data readout is not destructive and has the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied.

## BLOCK DIAGRAM




BD000270

## PRODUCT SELECTOR GUIDE

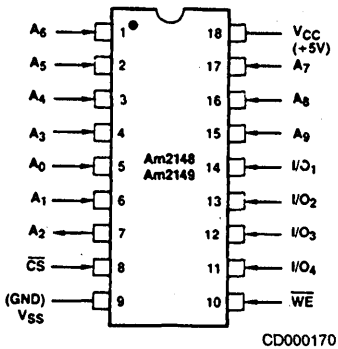
| Part Number | | Am2148/9 -35 | Am2148/9 -45 | Am21L48/9 -45 | Am2148/9 -55 | Am21L48/9 -55 | Am2148/9 -70 | Am21L48/9 -70 |
|---|---|---|---|---|---|---|---|---|
| Maximum Access Time (ns) | | 35 | 45 | 45 | 55 | 55 | 70 | 70 |
| $I_{CC}$ Max (mA) | 0 to +70°C | 180 | 180 | 125 | 180 | 125 | 180 | 125 |
| $I_{SB}$* Max (mA) | 0 to +70°C | 30 | 30 | 20 | 30 | 20 | 30 | 20 |
| $I_{CC}$Max (mA) | −55 to +125°C | N/A | 180 | N/A | 180 | N/A | 180 | N/A |
| $I_{SB}$* Max (mA) | −55 to +125°C | N/A | 30 | N/A | 30 | N/A | 30 | N/A |

*Am2148 and Am21L48 only.

03210D

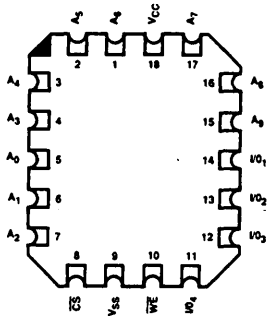
## CONNECTION DIAGRAM
Top View

### D-18




CD000170

### L-18-2

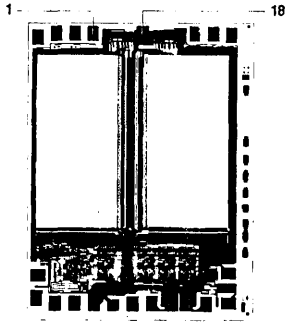



CD000350

Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| $A_0$ | $A_7$ |
| $A_1$ | $A_8$ |
| $A_2$ | $A_9$ |
| $A_3$ | $A_6$ |
| $A_4$ | $A_5$ |
| $A_5$ | $A_4$ |
| $A_6$ | $A_3$ |
| $A_7$ | $A_2$ |
| $A_8$ | $A_1$ |
| $A_9$ | $A_0$ |




DIE SIZE: 0.107 x 0.145

**Figure 2. Bit Mapping Information**

## ORDERING INFORMATION

**Am2148-55 D M B**

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- M — Temperature: C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 18-pin CERDIP; L – 18-pin leadless chip carrier
- 55 — Speed Select: 35 – 35ns; 45 – 45ns; 55 – 55ns; 70 – 70ns
- Am2148-55 — Device Type:
  - Am2148 – 1k x 4 SRAM with power down failure
  - Am21L48 – Same, Low Power
  - Am2149 – 1k x 4 SRAM
  - Am21L49 – Same, Low Power

| Valid Combinations | | |
|---|---|---|
| -35 (Am2148/9 only) | | DC, LC |
| -45 | Am2148/9 | DC, DM, DMB LC, LM, LMB |
| | L devices | DC, LC |
| -55 | Am2148/9 | DC, DM, DMB LC, LM, LMB |
| | L devices | DC, LC |
| -70 | Am2148/9 | DC, DM, DMB LC, LM, LMB |
| | L devices | DC, LC |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
Signal Voltages with
respect to ground ..... −3.5V to +7.0V
Power Description ..... 1.2W
DC Output Current ..... 20mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

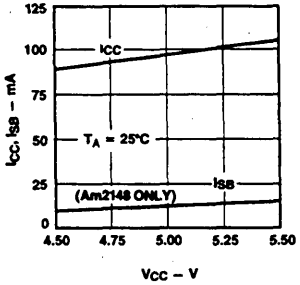
| Symbol | Parameter | Test Conditions | | Standard | | Low Power | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | $V_{CC}$ = 4.5V | −4 | | −4 | | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | $T_A$ = 70°C | 8 | | 8 | | mA |
| | | | $T_A$ = 125°C | 8 | | N/A | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | 6.0 | 2.0 | 6.0 | Volts |
| $V_{IL}$ | Input Low Voltage | | | −3.0 | 0.8 | −3.0 | 0.8 | Volts |
| $I_{IX}$ | Input Load Current | $V_{SS} \leq V_I \leq V_{CC}$ | | | 10 | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O \leq V_{CC}$ Output Disabled | $T_A$ = −55 to+125°C | −50 | 50 | −50 | 50 | µA |
| $C_I$ | Input Capacitance | Test Frequency = 1.0 MHz $T_A$ = 25°C, All Pins at 0V, $V_{CC}$ = 5V (Note 12) | | | 5 | | 5 | pF |
| $C_{I/O}$ | Input/Output Capacitance | | | | 7 | | 7 | |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | Max $V_{CC}$, $\overline{CS} \leq V_{IL}$ Output Open | $T_A$ = 0 to+ 70°C | | 180 | | 125 | mA |
| | | | $T_A$ = −55 to+125°C | | 180 | | N/A | |
| $I_{SB}$ | Automatic $\overline{CS}$ Power Down Current | Max $V_{CC}$, ($\overline{CS} \geq V_{IH}$) | $T_A$ = 0 to+70°C | | 30 | | 20 | mA |
| | | | $T_A$ = −55 to+125°C | | 30 | | N/A | |
| $I_{PO}$ | Peak Power-On Current | Max $V_{CC}$, ($\overline{CS} \geq V_{IH}$) (Note 3) | $T_A$ = 0 to+70°C | | 50 | | 30 | mA |
| | | | $T_A$ = −55 to+125°C | | 50 | | N/A | |
| $I_{OS}$ | Output Short Circuit Current | GND ≤ $V_O \leq V_{CC}$ (Note 11) | $T_A$ = 0 to+70°C | | ±275 | | ±275 | mA |
| | | | $T_A$ = −55 to+125°C | | ±350 | | ±350 | |

Notes:

1. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified $I_{OL}/I_{OH}$ and 30pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull up resistor to $V_{CC}$ on the $\overline{CS}$ input is required to keep the device deselected during $V_{CC}$ power up. Otherwise $I_{PO}$ will exceed values given (Am2148 only).
4. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
5. Chip deselected greater than 55ns prior to selection.
6. Chip deselected less than 55ns prior to selection.
7. At any given temperature and voltage condition, $t_{HZ}$ is less than $t_{LZ}$ for all devices. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. These parameters are sampled and not 100% tested.
8. $\overline{WE}$ is high for read cycle.
9. Device is continuously selected, $\overline{CS} = V_{IL}$.
10. Address valid prior to or coincident with $\overline{CS}$ transition low.
11. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
12. This parameter is sampled and not 100% tested.

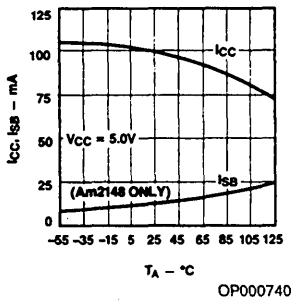
## DC OPERATING CHARACTERISTICS

**Supply Current Versus Supply Voltage**



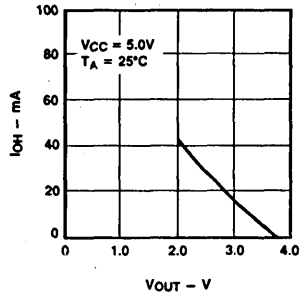

OP000730

**Supply Current Versus Ambient Temperature**



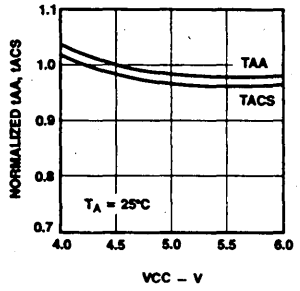

OP000740

**Output Source Current Versus Output Voltage**



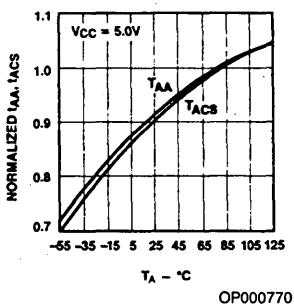

OP001080

**Normalized Access Time Versus Supply Voltage**



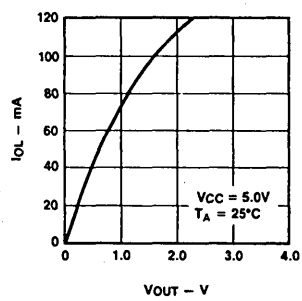

OP000760

**Normalized Access Time Versus Ambient Temperature**



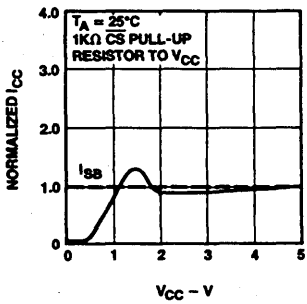

OP000770

**Output Sink Current Versus Output Voltage**



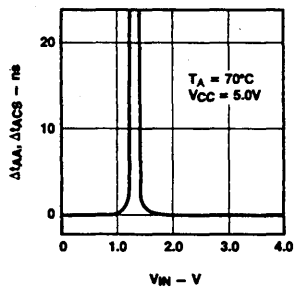

OP001090

**Typical Power-On Current Versus Power Supply**



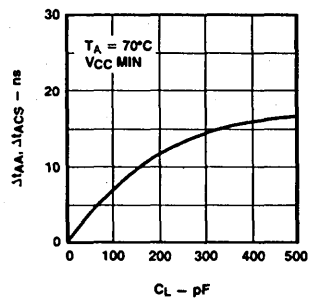

OP000790

**Access Time Change Versus Input Voltage**



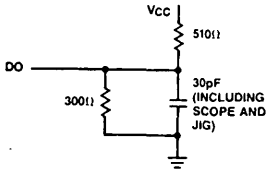

OP000800

**Access Time Change Versus Output Loading**



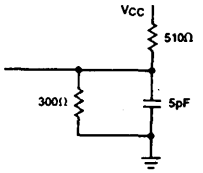

OP001100

## SWITCHING TEST CIRCUITS




TC000060

**Figure 1. Output Load**




TC000070

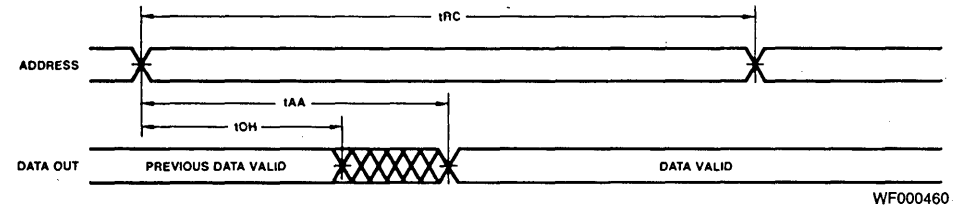
**Figue 2. Output Load for $t_{HZ}$, $t_{LZ}$, $t_{OW}$, $t_{WZ}$**

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

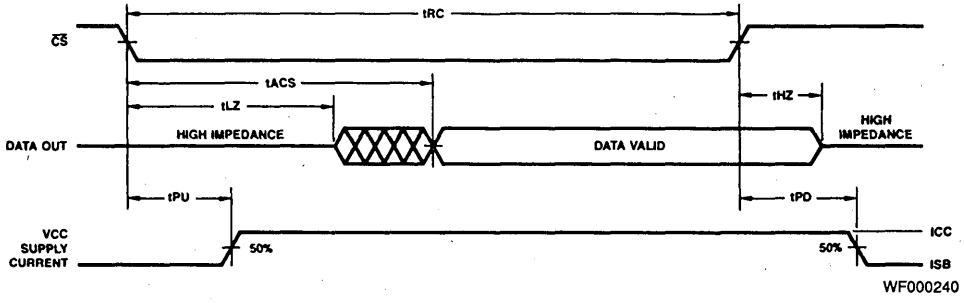
| No. | Symbol | Description | | Am2148/9-35 Min | Am2148/9-35 Max | Am2148/9-45 Am21L48/9-45 Min | Am2148/9-45 Am21L48/9-45 Max | Am2148/9-55 Am21L48/9-55 Min | Am2148/9-55 Am21L48/9-55 Max | Am2148/9-70 Am21L48/9-70 Min | Am2148/9-70 Am21L48/9-70 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | | | |
| 1 | $t_{RC}$ | Address Valid to Address Do Not Care Time (Read Cycle Time) | | 35 | | 45 | | 55 | | 70 | | ns |
| 2 | $t_{AA}$ | Address Valid to Data Out Valid Delay (Address Access Time) | | | 35 | | 45 | | 55 | | 70 | ns |
| 3 | $t_{ACS1}$ | Chip Select Low to Data Out Valid (Am2148 only) | Note 5 | | 35 | | 45 | | 55 | | 70 | ns |
| 4 | $t_{ACS2}$ | | Note 6 | | 45 | | 55 | | 65 | | 80 | |
| 5 | $t_{ACS}$ | Chip Select Low to Data Out Valid (Am2149 only) | | | 15 | | 20 | | 25 | | 30 | ns |
| 6 | $t_{LZ}$ | Chip Select Low to Data Out On (Note 7) | Am2148 | 10 | | 10 | | 10 | | 10 | | ns |
| | | | Am2149 | 5 | | 5 | | 5 | | 5 | | |
| 7 | $t_{HZ}$ | Chip Select High to Data Out Off (Note 7) | | 0 | 20 | 0 | 20 | 0 | 20 | 0 | 20 | ns |
| 8 | $t_{OH}$ | Address Unknown to Data Out Unknown Time | | 0 | | 5 | | 5 | | 5 | | ns |
| 9 | $t_{PD}$ | Chip Select High to Power Down Delay | Am2148 | | 30 | | 30 | | 30 | | 30 | ns |
| 10 | $t_{PU}$ | Chip Select Low to Power Up Delay | Am2148 | 0 | | 0 | | 0 | | 0 | | ns |
| **Write Cycle** | | | | | | | | | | | | |
| 11 | $t_{WC}$ | Address Valid to Address Do Not Care (Write Cycle Time) | | 35 | | 45 | | 55 | | 70 | | ns |
| 12 | $t_{WP}$ | Write Enable Low to Write Enable High (Note 2) | | 30 | | 35 | | 40 | | 50 | | ns |
| 13 | $t_{WR}$ | Write Enable High to Address | | 5 | | 5 | | 5 | | 5 | | ns |
| 14 | $t_{WZ}$ | Write Enable Low to Output in High Z (Note 7) | | 0 | 10 | 0 | 15 | 0 | 20 | 0 | 25 | ns |
| 15 | $t_{DW}$ | Data In Valid to Write Enable High | | 20 | | 20 | | 20 | | 25 | | ns |
| 16 | $t_{DH}$ | Data Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 17 | $t_{AS}$ | Address Valid to Write Enable Low | | 0 | | 0 | | 0 | | 0 | | ns |
| 18 | $t_{CW}$ | Chip Select Low to Write Enable High (Note 2) | | 30 | | 40 | | 50 | | 65 | | ns |
| 19 | $t_{OW}$ | Write Enable High to Output in Low Z (Note 7) | | 0 | | 0 | | 0 | | 0 | | ns |
| 20 | $t_{AW}$ | Address Valid to End of Write | | 30 | | 40 | | 50 | | 65 | | ns |

## SWITCHING WAVEFORMS

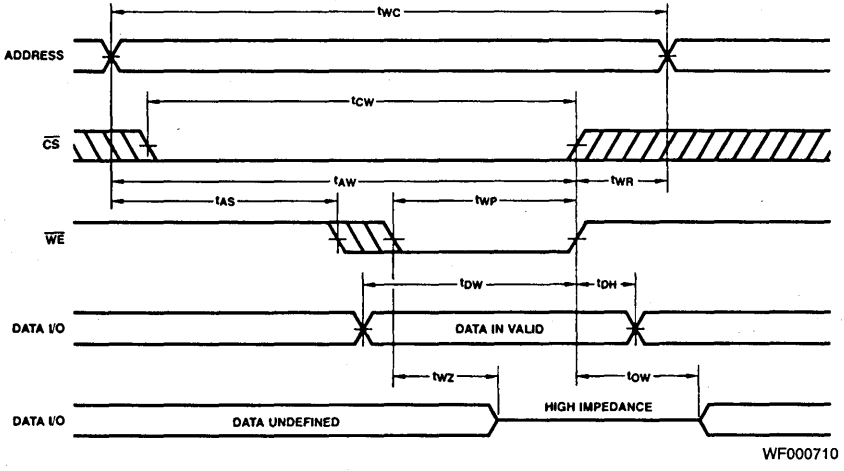
### READ CYCLE NO. 1 (Notes 8, 9)




### READ CYCLE NO. 2 (Notes 8, 10)

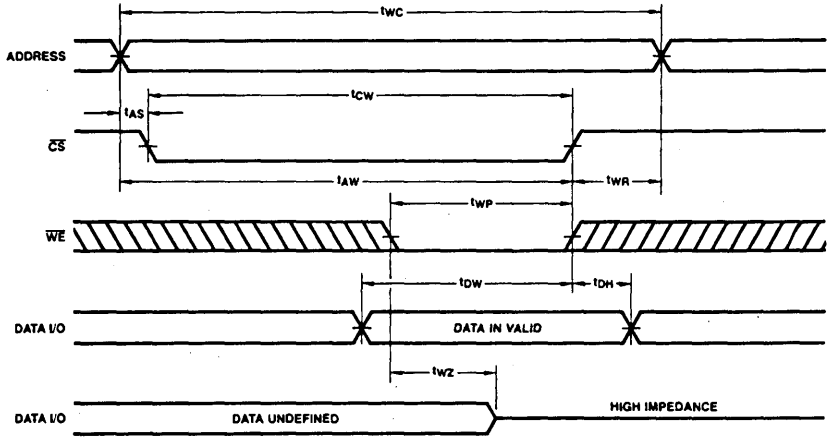



### WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



## SWITCHING WAVEFORMS (Cont.)

### WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)




WF000720

Note: If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

# Am2167

16,384 x 1 Static RAM

## DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 35ns maximum
- Automatic power down when deselected
- Low power dissipation
  - Am2167: 660mW active, 110mW power down
- High output drive
  - Up to seven standard TTL loads or six Schottky TTL loads
- TTL compatible interface levels
- No power-on current surge

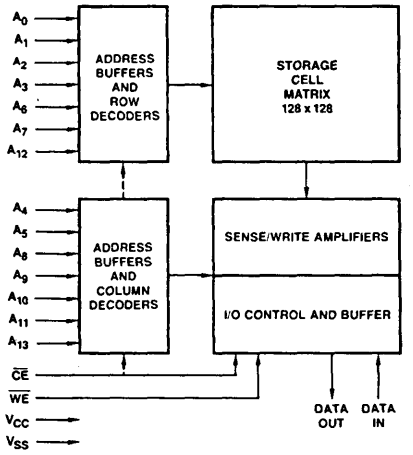
## GENERAL DESCRIPTION

The Am2167 is a high performance, 16,384-bit, static, read/write, random access memory. It is organized as 16,384 words by one bit per word. All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive up to six standard Schottky TTL loads or up to seven standard TTL loads.

Only a single +5 volt power supply is required. When deselected ($\overline{CE} \geq V_{IH}$), the Am2167 automatically enters a power-down mode which reduces power dissipation by 80%.

Data In and Data Out use separate pins and are the same polarity allowing them to be connected together for operation in a common data bus environment. Data Out is a three-state output allowing similar devices to be wire-OR'd together.

## BLOCK DIAGRAM



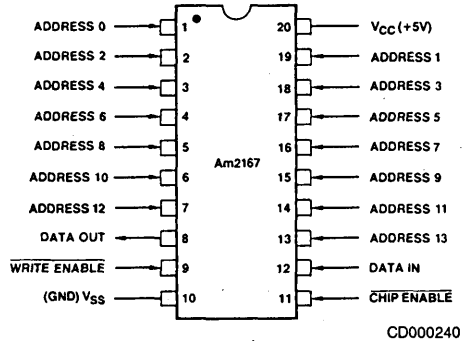

BD000170

## PRODUCT SELECTOR GUIDE

| Part Number | Am2167-35 | Am2167-45 | Am2167-55 | Am2167-70 |
|---|---|---|---|---|
| Maximum Access Time (ns) | 35 | 45 | 55 | 70 |
| Maximum Active Current (mA) | 120 | 120 (160 mil) | 120 (160 mil) | 120 (160 mil) |
| Maximum Standby Current (mA) | 20 | 20 (30 mil) | 20 (30 mil) | 20 (30 mil) |
| Full Military Operating Range Version | No | Yes | Yes | Yes |

03211D

## CONNECTION DIAGRAM
### Top View
### D-20-1, P-20-1

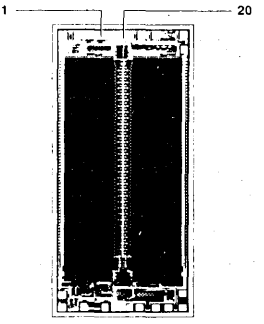



CD000240

Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| **External** | **Internal** |
| $A_0$ | $A_1$ |
| $A_1$ | $A_6$ |
| $A_2$ | $A_2$ |
| $A_3$ | $A_5$ |
| $A_4$ | $A_3$ |
| $A_5$ | $A_0$ |
| $A_6$ | $A_4$ |
| $A_7$ | $A_{13}$ |
| $A_8$ | $A_{10}$ |
| $A_9$ | $A_6$ |
| $A_{10}$ | $A_{11}$ |
| $A_{11}$ | $A_9$ |
| $A_{12}$ | $A_{12}$ |
| $A_{13}$ | $A_7$ |




DIE SIZE: 0.121 x 0.249

**Figure 3. Bit Mapping Information**

## ORDERING INFORMATION

**Am2167-45 D M B**

- B — Burn-in Option: B suffix denotes 160 hour burn-in.
- M — Temperature: C – Commercial (0°C to +70°C); M – Military (–55°C to +125°C)
- D — Package: D – 20-pin CERDIP; P – 20-pin plastic DIP
- 45 — Speed Select: 35 – 35ns; 45 – 45ns; 55 – 55ns; 70 – 70ns
- Am2167 — Device Type: 16k x 1 SRAM

| Valid Combinations | |
|---|---|
| Am2167-35 | PC, DC |
| Am2167-45 | PC, DC<br>DM, DMB |
| Am2167-55 | PC, DC,<br>DM, DMB |
| Am2167-70 | PC, DC<br>DM, DMB |



03211D

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
Signal Voltages with
respect to ground ..... −3.0V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 10mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

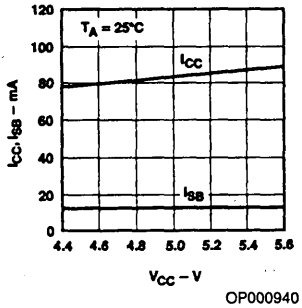
| Symbol | Parameter | Test Conditions | | Am2167-35 Min | Am2167-35 Max | Am2167-45 Am2167-55 Am2167-70 Min | Am2167-45 Am2167-55 Am2167-70 Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V | $V_{CC}$ = 4.5V | −4 | | −4 | | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | COM'L | 16 | | 16 | | mA |
| | | | MIL | 12 | | 12 | | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | 6.0 | 2.0 | 6.0 | Volts |
| $V_{IL}$ | Input Low Voltage | | | −3.0 | 0.8 | −3.0 | 0.8 | Volts |
| $I_{IX}$ | Input Load Current | $V_{SS} \leq V_I \leq V_{CC}$ | | | 10 | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O \leq V_{CC}$ Output Disabled | | −50 | 50 | −50 | 50 | µA |
| $C_I$ | Input Capacitance | Test Frequency = 1.0 MHz $T_A$ = 25°C, All pins at 0V, $V_{CC}$ = 5V | | | 5 | | 5 | pF |
| $C_O$ | Output Capacitance | | | | 6 | | 6 | |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | Max $V_{CC}$, CE ≤ $V_{IL}$ Output Open | COM'L | | 120 | | 120 | mA |
| | | | MIL | | N/A | | 160 | |
| $I_{SB}$ | Automatic CE Power Down Current | MAX $V_{CC}$, (CE ≥ $V_{IH}$) (Note 3) | COM'L | | 20 | | 20 | mA |
| | | | MIL | | N/A | | 30 | |

Notes:

1. Test conditions assume signal transition times of 5ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified $I_{OL}/I_{OH}$ and 30pF load capacitance. Output timing reference is 1.5V.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. A pull-up resistor to $V_{CC}$ on the $\overline{CE}$ input is required to keep the device deselected during $V_{CC}$ power up. Otherwise $I_{SB}$ will exceed values given.
4. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
5. The device must be selected during the previous cycle. Otherwise $t_{AA}$ and $t_{RC}$ are equivalent to $t_{ACS}$.
6. At any given temperature and voltage condition, $t_{HZ}$ is less than $t_{LZ}$ for all devices. Transition is measured ±500mV from steady state voltage with load specified in Figure 2 for $t_{HZ}$, $t_{LZ}$, $t_{OW}$ and $t_{WZ}$.
7. $\overline{WE}$ is high for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition low.

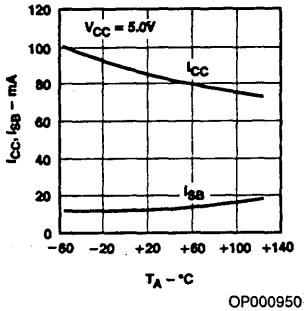
## DC OPERATING CHARACTERISTICS

### Supply Current versus Supply Voltage



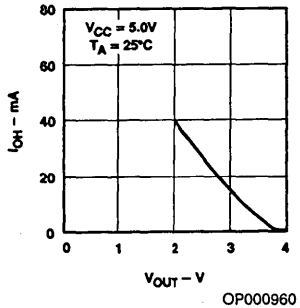

OP000940

### Supply Current versus Ambient Temperature



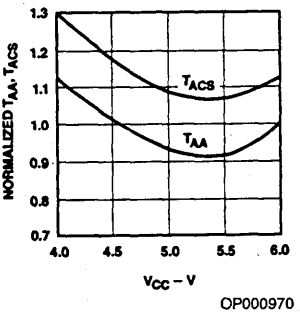

OP000950

### Output Source Current versus Output Voltage



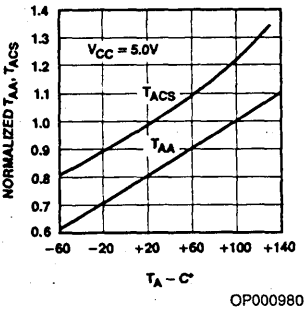

OP000960

### Normalized Access Time versus Supply Voltage



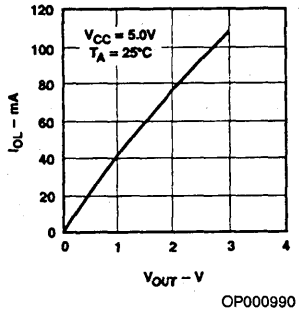

OP000970

### Normalized Access Time versus Ambient Temperature



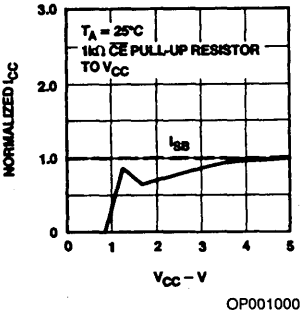

OP000980

### Output Sink Current versus Output Voltage



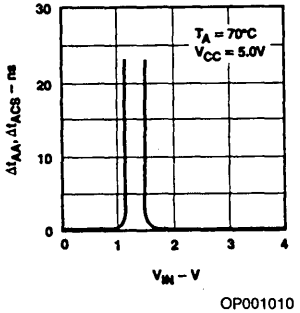

OP000990

### Typical Power-On Current versus Power Supply



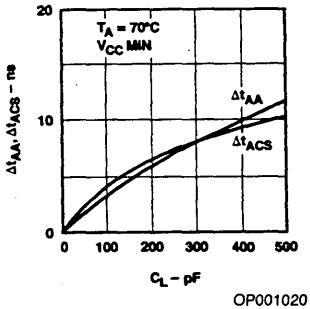

OP001000

### Access Time Change versus Input Voltage




OP001010

### Access Time Change versus Output Loading




OP001020

## SWITCHING TEST CIRCUITS

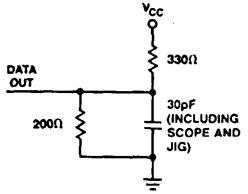



**Figure 1. Output Load**

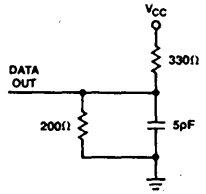


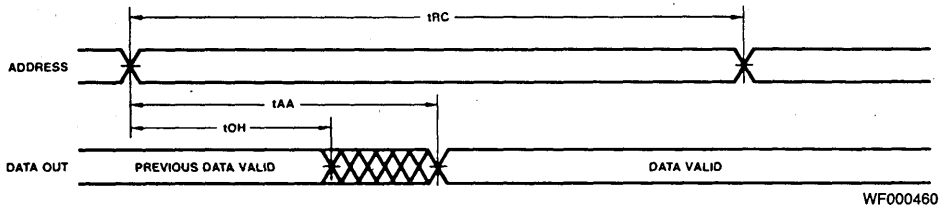

**Figure 2. Output Load for $t_{HZ}$, $t_{LZ}$, $t_{OW}$, $t_{WZ}$**

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am2167-35 | | Am2167-45 | | Am2167-55 | | Am2167-70 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | | | | | | |
| 1 | $t_{RC}$ | Address Valid to Address Do Not Care Time (Read Cycle Time) (Note 5) | 30 | | 40 | | 50 | | 70 | | ns |
| 2 | $t_{AA}$ | Address Valid to Data Out Valid Delay (Address Access Time) (Note 5) | | 30 | | 40 | | 50 | | 70 | ns |
| 3 | $t_{ACS}$ | Chip Enable Low to Data Out Valid (Chip Enable Access Time) | | 35 | | 45 | | 55 | | 70 | ns |
| 4 | $t_{LZ}$ | Chip Enable Low to Data Out On (Note 6) | 5 | | 5 | | 5 | | 5 | | ns |
| 5 | $t_{HZ}$ | Chip Enable High to Data Out Off (Note 6) | 0 | 20 | 0 | 25 | 0 | 30 | 0 | 40 | ns |
| 6 | $t_{OH}$ | Address Unknown to Data Out Unknown Time | 5 | | 5 | | 5 | | 5 | | ns |
| 7 | $t_{PD}$ | Chip Enable High to Power Down Delay | | 25 | | 30 | | 30 | | 55 | ns |
| 8 | $t_{PU}$ | Chip Enable Low to Power Up Delay | 0 | | 0 | | 0 | | 0 | | ns |
| **Write Cycle** | | | | | | | | | | | |
| 9 | $t_{WC}$ | Address Valid to Address Do Not Care (Write Cycle Time) | 30 | | 40 | | 50 | | 70 | | ns |
| 10 | $t_{WP}$ | Write Enable Low to Write Enable High (Note 2) | 20 | | 20 | | 25 | | 40 | | ns |
| 11 | $t_{WR}$ | Write Enable High to Address | 0 | | 0 | | 0 | | 0 | | ns |
| 12 | $t_{WZ}$ | Write Enable Low to Output in High Z (Note 6) | 0 | 20 | 0 | 20 | 0 | 25 | 0 | 35 | ns |
| 13 | $t_{DW}$ | Data In Valid to Write Enable High | 15 | | 15 | | 20 | | 30 | | ns |
| 14 | $t_{DH}$ | Data Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| 15 | $t_{AS}$ | Address Valid to Write Enable Low | 5 | | 5 | | 5 | | 5 | | ns |
| 16 | $t_{CW}$ | Chip Enable Low to Write Enable High (Note 2) | 30 | | 40 | | 50 | | 55 | | ns |
| 17 | $t_{OW}$ | Write Enable High to Output in Low Z (Note 6) | 0 | | 0 | | 0 | | 0 | | ns |
| 18 | $t_{AW}$ | Address Valid to End of Write | 30 | | 40 | | 50 | | 70 | | ns |

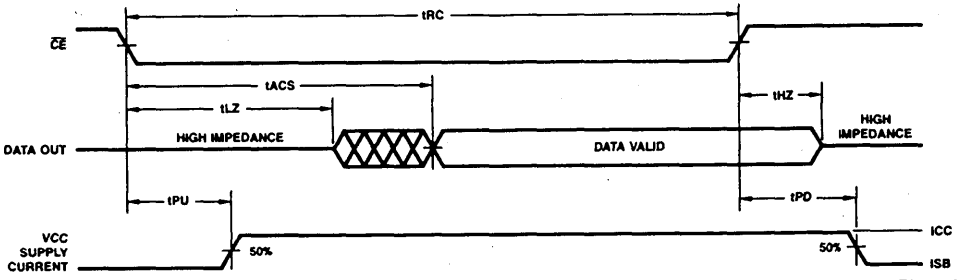
## SWITCHING WAVEFORMS

### READ CYCLE NO. 1 (Notes 5, 7)



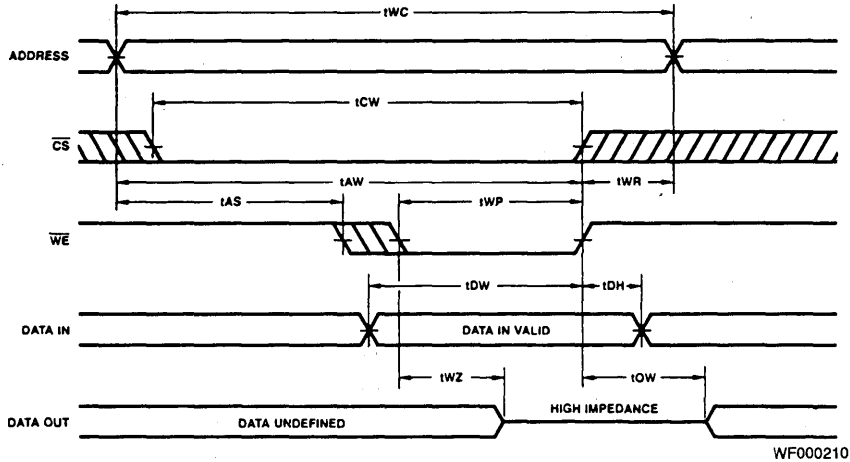
## SWITCHING WAVEFORMS (Cont.)

### READ CYCLE NO. 2 (Notes 7, 8)



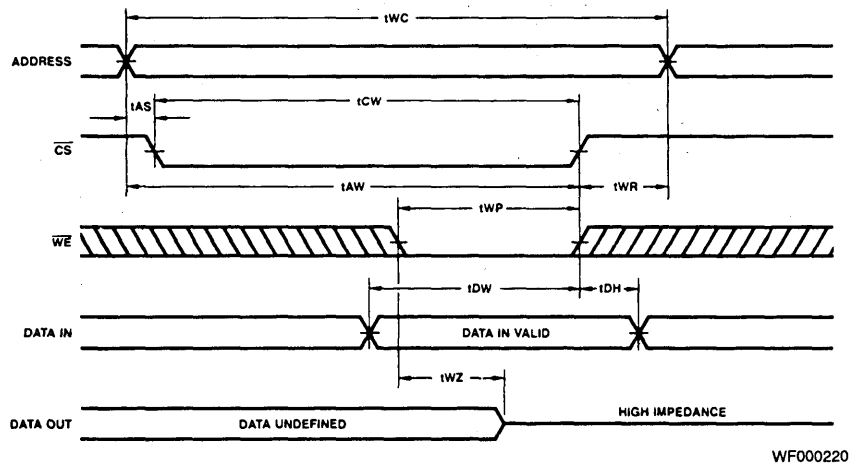

WF000280

### WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)




WF000210

### WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)




WF000220

Note: If $\overline{CE}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

# Am9016

16,384 x 1 Dynamic RAM

## DISTINCTIVE CHARACTERISTICS

- Replacement for MK4116
- High-speed operation – 150ns access, 320ns cycle (COM'L); 200ns access, 375ns cycle (MIL)
- Three-state output
- $\overline{RAS}$ only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output

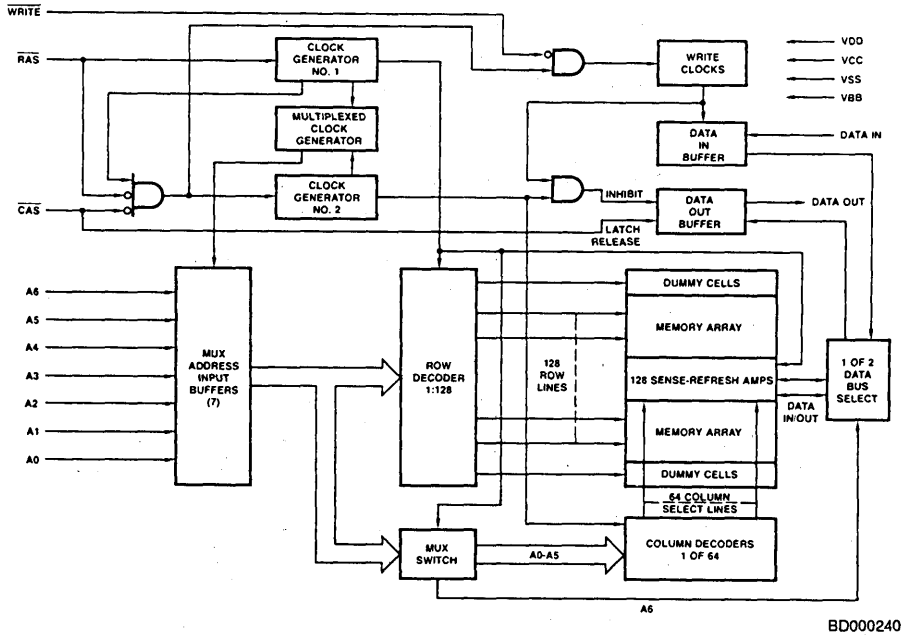
## GENERAL DESCRIPTION

The Am9016 is a high-speed, 16K-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP or 18-pin leadless chip carrier. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share seven input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance and power dissipation.

The 3-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

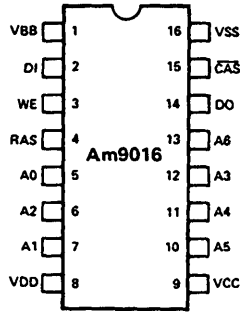
## BLOCK DIAGRAM




03258C

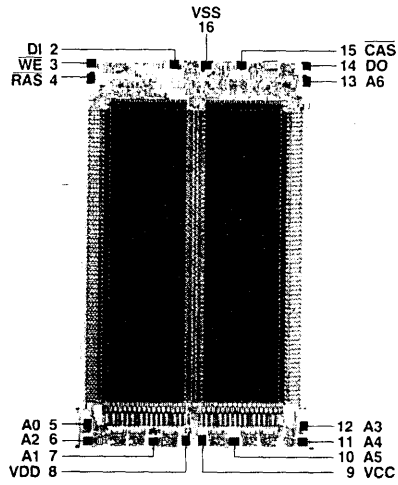
## CONNECTION DIAGRAM
Top View

DIP




CD000300

## Metallization and Pad Layout




DIE SIZE 0.107" x 0.205"

## ORDERING INFORMATION

**Am9016 E D C**

C – Temperature
- C – Commercial (0°C to +70°C)
- L – Extended (–55°C to +85°C)

D – Package
- D – 16-pin CERDIP
- P – 16-pin plastic

E – Speed Select
- F – 150ns
- E – 200ns
- D – 250ns
- C – 300ns

Am9016 – Device Type
16k x 1 DRAM

| Valid Combinations | |
|---|---|
| C, D, E | DC, PC, DL |
| F | DC, PC |

## APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

### OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1. The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2. After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3. Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4. $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least eight initialization cycles which exercise $\overline{RAS}$ before valid memory accesses are begun.

### ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

### REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

### DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

### DATA OUTPUT CONTROL

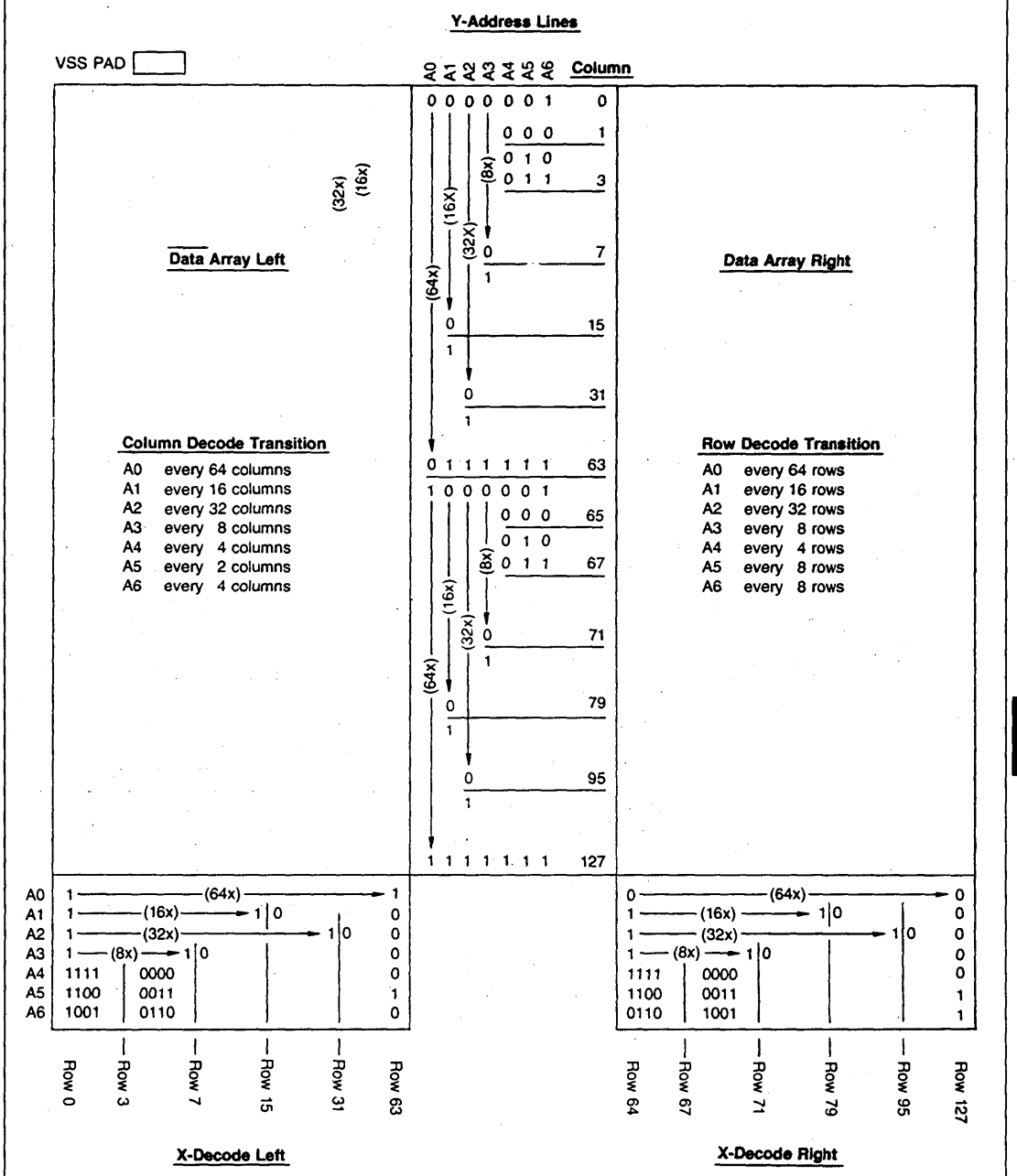
Any time $\overline{CAS}$ is high the data output will be off (after tOFF). The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

### POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.




TOPOLOGICAL BIT MAP

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +85°C
Voltage on any pin with
respect to $V_{BB}$ ..... −0.5V to +20V
Positive Supply Voltages with
respect to ground ..... −1.0V to +15.0V
DC Layout Voltage ..... −0.5V to +7.0V
$V_{BB} - V_{SS}$ Differentials given
$V_{DD} - V_{SS} > 0V$ ..... 0W
Power Dissipation ..... 1.0W
Short Circuit Output Current ..... 50mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Positive Supply Voltage $V_{DD}$ ..... +10.8V to +13.2V
$V_{CC}$ ..... +4.5V to +5.5V
Negative Supply Voltage $V_{BB}$ ..... −4.5V to −5.5V

Extended (L) Devices
Temperature ..... −55°C to +85°C
Positive Supply Voltage $V_{DD}$ ..... +10.8V to +13.2V
$V_{CC}$ ..... +4.5V to +5.5V
Negative Supply Voltage $V_{BB}$ ..... −4.5V to −5.5V

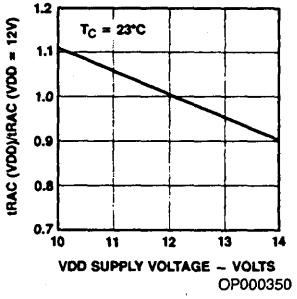
*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -5.0mA$ | | 2.4 | | $V_{CC}$ | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 4.2mA$ | | $V_{SS}$ | | 0.40 | Volts |
| $V_{IH}$ | Input HIGH Voltage for Address, Data In | | | 2.4 | | 7.0 | Volts |
| $V_{IHC}$ | Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$ | | | 2.7 | | 7.0 | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −1.0 | | 0.80 | Volts |
| $I_{IX}$ | Input Load Current | $V_{SS} \leq V_I \leq 7V$ | | −10 | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | $V_{SS} \leq V_O \leq V_{CC}$, Output OFF | | −10 | | 10 | µA |
| $I_{CC}$ | $V_{CC}$ Supply Current | Output OFF (Note 4) | | −10 | | 10 | µA |
| $I_{BB}$ | Supply Current, Average | Standby, $\overline{RAS} \geq V_{IHC}$ | $0°C \leq T_A \leq +70°C$ | | | 100 | µA |
| | | | $-55°C \leq T_A \leq +85°C$ | | | 200 | |
| | | Operating, Minimum Cycle Time | $0°C \leq T_A \leq +70°C$ | | | 200 | |
| | | | $-55°C \leq T_A \leq +85°C$ | | | 400 | |
| $I_{DD}$ | $V_{DD}$ Supply Current Average | $\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times, Operating $I_{DD1}$ | | | | 35 | mA |
| | | $\overline{RAS} \leq V_{IL}$, $\overline{CAS}$ Cycling, Minimum Cycle Times, Page Mode $I_{DD4}$ | | | | 27 | |
| | | $\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IHC}$, Minimum Cycle Times, $\overline{RAS}$ Only Refresh $I_{DD3}$ | | | | 27 | |
| | | $\overline{RAS} \leq V_{IHC}$ Standby $I_{DD2}$ | $0°C \leq T_A \leq +70°C$ | | | 1.5 | |
| | | | $-55°C \leq T_A \leq +85°C$ | | | 2.25 | |
| $C_I$ | Input Capacitance | Inputs at 0V, f = 1MHz, Nominal Supply Voltages | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | | | 10 | pF |
| | | | Address, Data In | | | 5.0 | |
| $C_O$ | Output Capacitance | Output OFF | | | | 7.0 | |

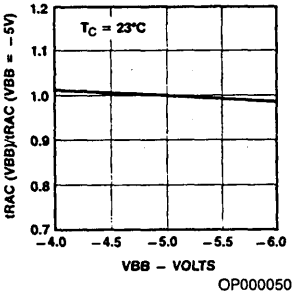
## DC OPERATING CHARACTERISTICS

### Typical Access Time (Normalized) $t_{RAC}$ Versus $V_{DD}$



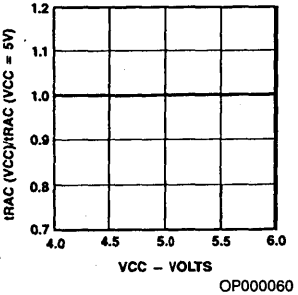

OP000350

### Typical Access Time (Normalized) $t_{RAC}$ Versus $V_{BB}$



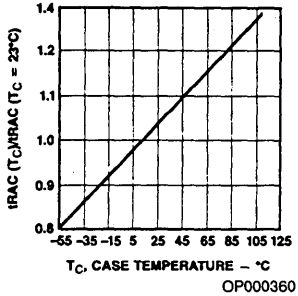

OP000050

### Typical Access Time (Normalized) $t_{RAC}$ Versus $V_{CC}$



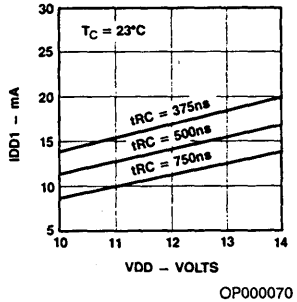

OP000060

### Typical Access Time (Normalized) $t_{RAC}$ Versus Case Temperature



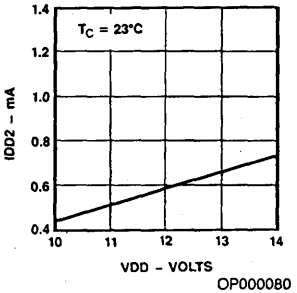

OP000360

### Typical Operating current $I_{DD1}$ Versus $V_{DD}$



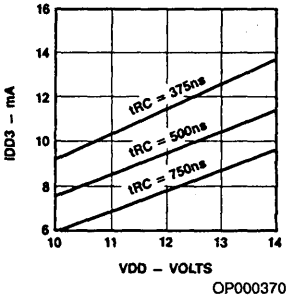

OP000070

### Typical Standby Current $I_{DD2}$ Versus $V_{DD}$



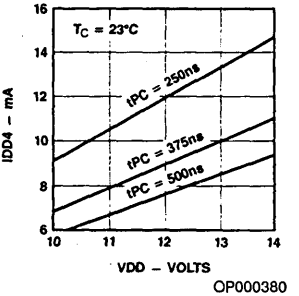

OP000080

### Typical Refresh Current $I_{DD3}$ Versus $V_{DD}$



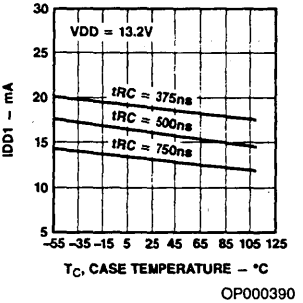

OP000370

### Typical Page Mode Current $I_{DD4}$ Versus $V_{DD}$




OP000380

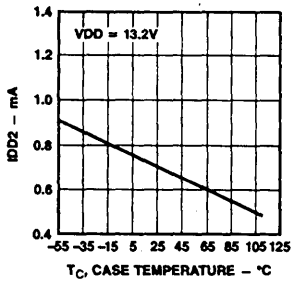
### Typical Operating Current $I_{DD1}$ Versus Case Temperature




OP000390

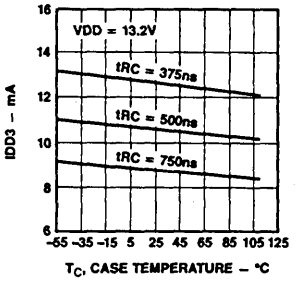
## DC OPERATING CHARACTERISTICS (Cont.)

**Typical Standby Current $I_{DD2}$ Versus Case Temperature**



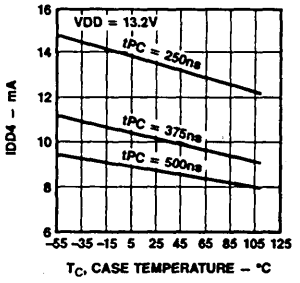

OP000400

**Typical Refresh Current $I_{DD3}$ Versus Case Temperature**



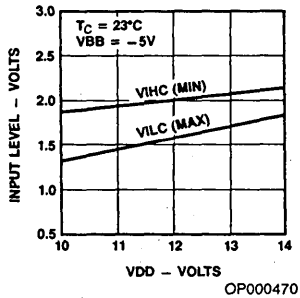

OP000410

**Typical Page Mode Current $I_{DD4}$ Versus Case Temperature**



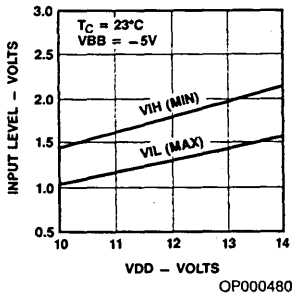

OP000420

**Input Voltage Levels Versus $V_{DD}$**



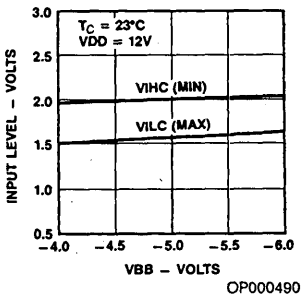

OP000470

**Input Voltage Levels Versus $V_{DD}$**



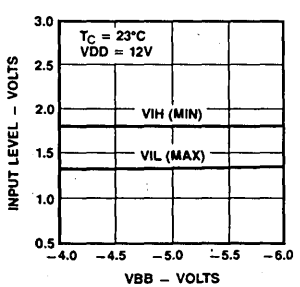

OP000480

**Input Voltage Levels Versus $V_{BB}$**



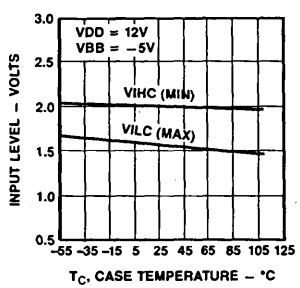

OP000490

**Input Voltage Levels Versus $V_{BB}$**



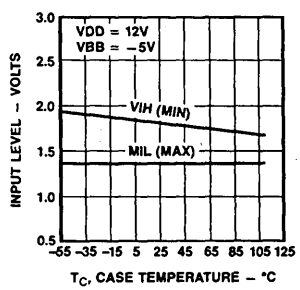

OP000500

**Input Voltage Levels Versus Case Temperature**




OP000510

**Input Voltage Levels Versus Case Temperature**




OP000520

## DC OPERATING CHARACTERISTICS (Cont.)

### TYPICAL CURRENT WAVEFORMS


WF000310

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | | Am9016C Min | Am9016C Max | Am9016D Min | Am9016D Max | Am9016E Min | Am9016E Max | Am9016F Min | Am9016F Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{AR}$ | $\overline{RAS}$ LOW to Column Address Hold Time | | 200 | | 160 | | 120 | | 95 | | ns |
| 2 | $t_{ASC}$ | Column Address Setup Time | $0°C \leq T_A \leq +70°C$ | −10 | | −10 | | −10 | | −10 | | ns |
| | | | $-55°C \leq T_A \leq +85°C$ | 0 | | 0 | | 0 | | NA | | ns |
| 3 | $t_{ASR}$ | Row Address Setup Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 4 | $t_{CAC}$ | Access Time from $\overline{CAS}$ (Note 6) | | | 185 | | 165 | | 135 | | 100 | ns |
| 5 | $t_{CAH}$ | $\overline{CAS}$ LOW to Column Address Hold Time | | 85 | | 75 | | 55 | | 45 | | ns |
| 6 | $t_{CAS}$ | $\overline{CAS}$ Pulse Width | $0°C \leq T_A \leq +70°C$ | 185 | 10,000 | 165 | 10,000 | 135 | 10,000 | 100 | 10,000 | ns |
| | | | $-55°C \leq T_A \leq +85°C$ | 185 | 5000 | 165 | 5000 | 135 | 5000 | NA | NA | ns |
| 7 | $t_{CP}$ | Page Mode $\overline{CAS}$ Precharge Time | | 100 | | 100 | | 80 | | 60 | | ns |
| 8 | $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | $0°C \leq T_A \leq +70°C$ | −20 | | −20 | | −20 | | −20 | | ns |
| | | | $-55°C \leq T_A \leq +85°C$ | 0 | | 0 | | 0 | | NA | | ns |
| 9 | $t_{CSH}$ | $\overline{CAS}$ Hold Time | | 300 | | 250 | | 200 | | 150 | | ns |
| 10 | $t_{CWD}$ | $\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | | 145 | | 125 | | 95 | | 70 | | ns |
| 11 | $t_{CWL}$ | $\overline{WE}$ LOW to $\overline{CAS}$ HIGH Setup Time | | 100 | | 85 | | 70 | | 50 | | ns |
| 12 | $t_{DH}$ | $\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7) | | 85 | | 75 | | 55 | | 45 | | ns |
| 13 | $t_{DHR}$ | $\overline{RAS}$ LOW to Data In Valid Hold Time | | 200 | | 160 | | 120 | | 95 | | ns |
| 14 | $t_{DS}$ | Data in Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Setup Time (Note 7) | | 0 | | 0 | | 0 | | 0 | | ns |
| 15 | $t_{OFF}$ | $\overline{CAS}$ HIGH to Output OFF Delay | | 0 | 60 | 0 | 60 | 0 | 50 | 0 | 40 | ns |
| 16 | $t_{PC}$ | Page Mode Cycle Time | | 295 | | 275 | | 225 | | 170 | | ns |
| 17 | $t_{RAC}$ | Access Time from $\overline{RAS}$ (Note 6) | | | 300 | | 250 | | 200 | | 150 | ns |
| 18 | $t_{RAH}$ | $\overline{RAS}$ LOW to Row Address Hold Time | | 45 | | 35 | | 25 | | 20 | | ns |
| 19 | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | $0°C \leq T_A \leq +70°C$ | 300 | 10,000 | 250 | 10,000 | 200 | 10,000 | 150 | 10,000 | ns |
| | | | $-55°C \leq T_A \leq +85°C$ | 300 | 5000 | 250 | 5000 | 200 | 5000 | NA | NA | ns |
| 20 | $t_{RC}$ | Random Read or Write Cycle Time | | 460 | | 410 | | 375 | | 320 | | ns |
| 21 | $t_{RCD}$ | $\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6) | | 35 | 115 | 35 | 85 | 25 | 65 | 20 | 50 | ns |
| 22 | $t_{RCH}$ | Read Hold Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 23 | $t_{RCS}$ | Read Setup Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 24 | $t_{REF}$ | Refresh Interval | | | 2 | | 2 | | 2 | | 2 | ms |
| 25 | $t_{RMW}$ | Read Modify Write Cycle Time | | 600 | | 500 | | 405 | | 320 | | ns |

| No. | Symbol | Description | | Am9016C Min | Am9016C Max | Am9016D Min | Am9016D Max | Am9016E Min | Am9016E Max | Am9016F Min | Am9016F Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 26 | $t_{RP}$ | $\overline{RAS}$ Precharge Time | | 150 | | 150 | | 120 | | 100 | | ns |
| 27 | $t_{RSH}$ | $\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay | | 185 | | 165 | | 135 | | 100 | | ns |
| 28 | $t_{RWC}$ | Read/Write Cycle Time | | 525 | | 425 | | 375 | | 320 | | ns |
| 29 | $t_{RWD}$ | $\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9) | | 260 | | 210 | | 160 | | 120 | | ns |
| 30 | $t_{RWL}$ | $\overline{WE}$ LOW to $\overline{RAS}$ HIGH Setup Time | | 100 | | 85 | | 70 | | 50 | | ns |
| 31 | $t_T$ | Transition Time | | 3 | 50 | 3 | 50 | 3 | 50 | 3 | 35 | ns |
| 32 | $t_{WCH}$ | Write Hold Time | | 85 | | 75 | | 55 | | 45 | | ns |
| 33 | $t_{WCR}$ | $\overline{RAS}$ LOW to Write Hold Time | | 200 | | 160 | | 120 | | 95 | | ns |
| 34 | $t_{WCS}$ | $\overline{WE}$ LOW to $\overline{CAS}$ LOW Setup Time (Note 9) | $0°C \leq T_A \leq +70°C$ | −20 | | −20 | | −20 | | −20 | | ns |
| | | | $-55°C \leq T_A \leq +85°C$ | 0 | | 0 | | 0 | | NA | | |
| 35 | $t_{WP}$ | Write Pulse Width | | 85 | | 75 | | 55 | | 45 | | ns |

Notes:

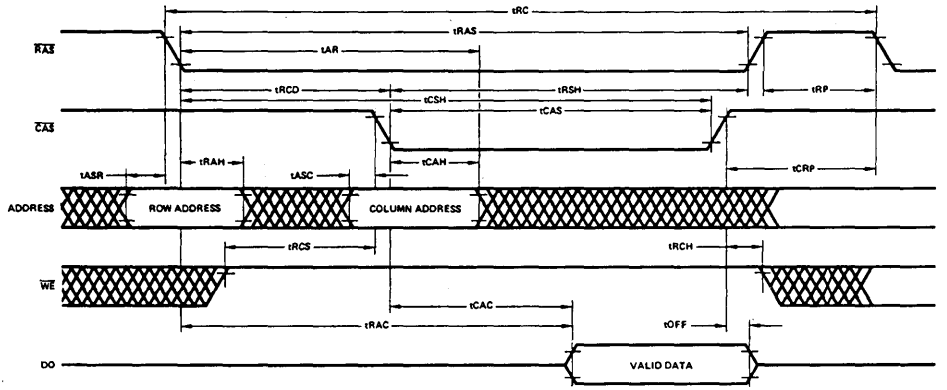
1. All voltages referenced to $V_{SS}$.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. $V_{CC}$ is used in the output buffer only. $I_{CC}$ will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, $V_{CC}$ is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode $V_{CC}$ may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low read data. Access timing will depend on the relative positions of their falling edges. When $t_{RCD}$ is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When $t_{RCD}$ is more than the maximum value shown access time depends on $\overline{CAS}$ and $t_{CAC}$ governs. The maximum value listed for $t_{RCD}$ is shown for reference purposes only and does not restrict operation of the part.

## SWITCHING CHARACTERISTICS (Cont.)

7. Timing reference points for data input setup and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least eight initialization cycles that exercise $\overline{RAS}$ should be performed after power-up and before valid operations are begun.
9. The $t_{WCS}$, $t_{RWD}$ and $t_{CWD}$ parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most $t_{WCS}$, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least $t_{RWD}$ and $t_{CWD}$ respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.

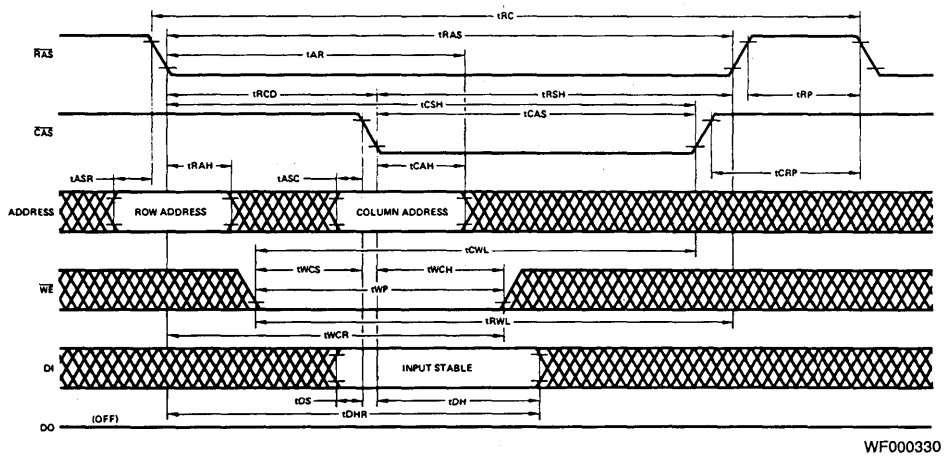
## SWITCHING WAVEFORMS

### READ CYCLE




WF000320

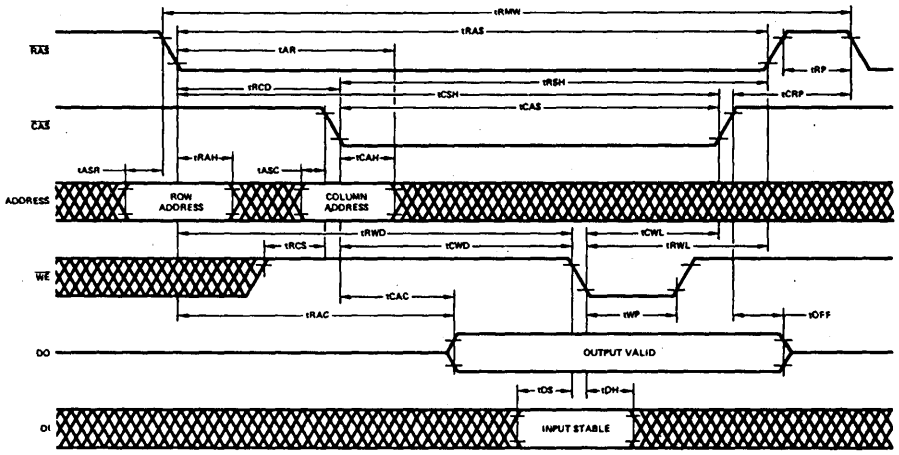
### WRITE CYCLE (EARLY WRITE)




WF000330

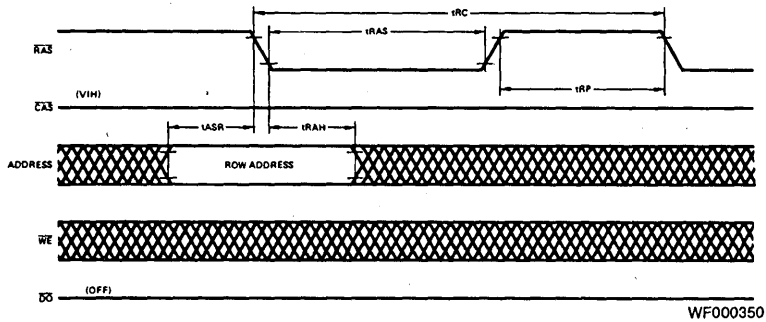
## SWITCHING WAVEFORMS (Cont.)

### READ-WRITE/READ-MODIFY-WRITE CYCLE




WF000340

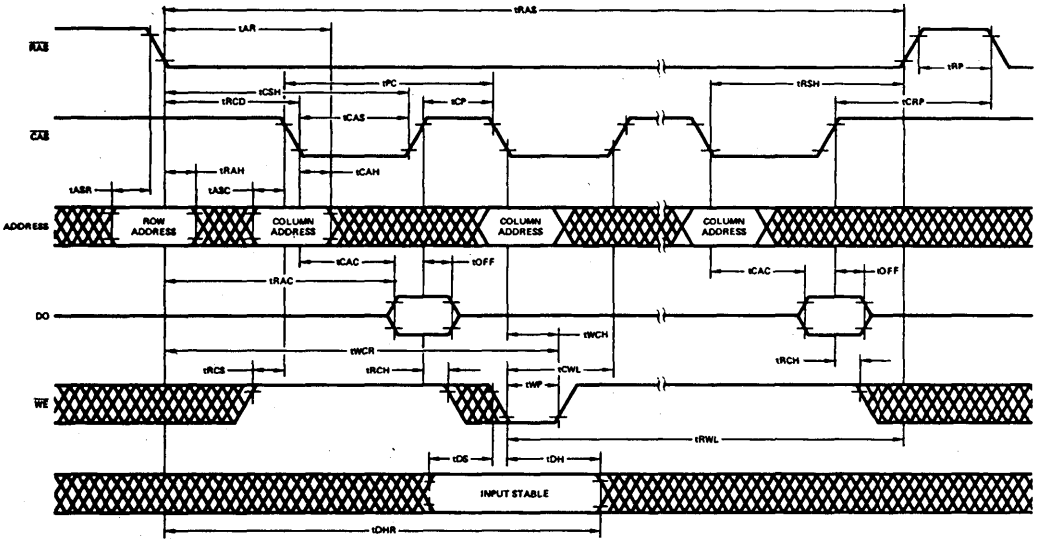
### RAS ONLY REFRESH CYCLE




WF000350

## SWITCHING WAVEFORMS (Cont.)

### PAGE MODE CYCLE




WF000360

# Am9044/9244

4096 x 1 Static RAM

## DISTINCTIVE CHARACTERISTICS

- LOW OPERATING AND STANDBY POWER
- Access times down to 200ns
- Am9044 is a direct plug-in replacement for 4044
- Am9244 pin and function compatible with Am9044 and 4044 plus $\overline{CS}$ power down feature
- High output drive — 4.0mA sink current @ 0.4V
- TTL identical interface logic levels

## GENERAL DESCRIPTION

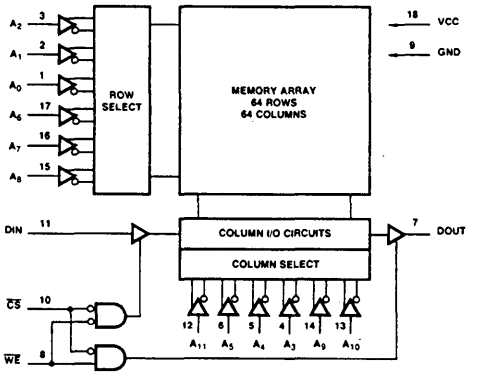
The Am9044 and Am9244 are high performance, static, N-Channel, read/write, random access memories organized as 4096 x 1. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of about 30%. The Am9044 and Am9244 are the same except that the Am9244 offers an automatic $\overline{CS}$ power down feature.

The Am9244 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements.

The Am9244 power decreases from 385mW to 165mW in the standby mode, and the Am92L44 from 275mW to 110mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9044.

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9244 and Am9044 provide increased short circuit current for improved drive.

## BLOCK DIAGRAM



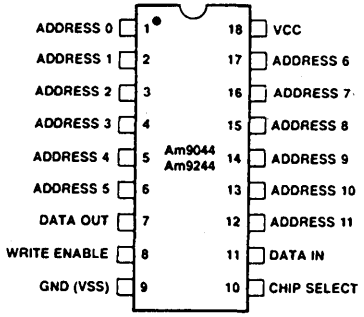

BD000090

## PRODUCT SELECTOR GUIDE

| Access Times | 450ns | 300ns | 250ns | 200ns |
|---|---|---|---|---|
| Standard Device | Am9044B<br>Am9244B | Am9044C<br>Am9244C | Am9044D<br>Am9244D | Am9044E<br>Am9244E |
| Low Power | Am90L44B<br>Am92L44B | Am90L44C<br>Am92L44C | Am90L44D | |

03254C

## CONNECTION DIAGRAM
### Top View

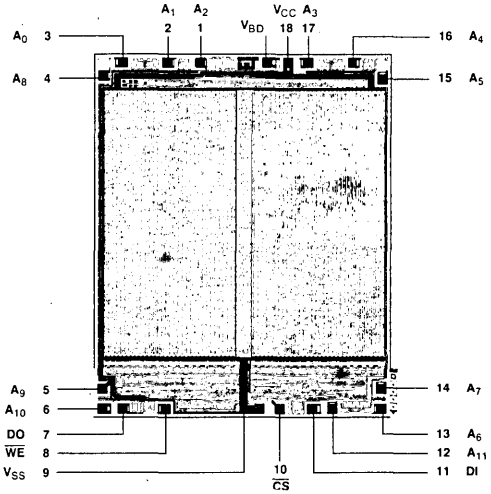



CD000140

Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| $A_0$ | $A_2$ |
| $A_1$ | $A_1$ |
| $A_2$ | $A_0$ |
| $A_3$ | $A_8$ |
| $A_4$ | $A_9$ |
| $A_5$ | $A_{10}$ |
| $A_6$ | $A_3$ |
| $A_7$ | $A_4$ |
| $A_8$ | $A_5$ |
| $A_9$ | $A_7$ |
| $A_{10}$ | $A_6$ |
| $A_{11}$ | $A_{11}$ |




DIE SIZE 0.137" x 0.167"

**Figure 1. Bit Mapping Information**

## ORDERING INFORMATION

**Am9044 B P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 18-pin CERDIP
  - P – 18-pin plastic DIP
- B — Speed Select
  - B – 450ns D – 250ns
  - C – 300ns E – 200ns

Device Type
4096 x 1 Static RAM

| Valid Combinations | |
|---|---|
| B | PC, DC, DM |
| C | PC, DC, DM |
| D | PC, DC, DM (9044/9244 only) |
| E (9044/9244 only) | PC, DC |

AM9044 – 4k x 1 SRAM
AM90L44 – Same, Low Power
AM9244 – 4k x 1 SRAM with power down feature
AM92L44 – Same, Low Power



03254C

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
All Signal Voltage with
respect to ground ..... −0.5V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 10mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

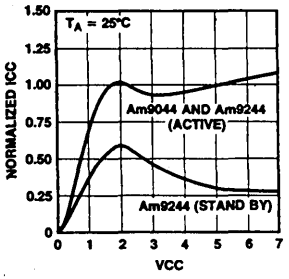
*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH}$ = 2.4V, $V_{CC}$ = 4.5V | $T_A$ = 70°C | | −1.0 | | | mA |
| | | | $T_A$ = 125°C | | −0.4 | | | |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.4V | $T_A$ = 70°C | | 4.0 | | | mA |
| | | | $T_A$ = 125°C | | 3.2 | | | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | 0.5 | | 0.8 | V |
| $I_{IX}$ | Input Load Current | $GND \leq V_{IN} \leq V_{CC}$ | | | | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | $0.4V \leq V_O \leq V_{CC}$, Output Disabled | $T_A$ = +70°C | | −50 | | 50 | µA |
| | | | $T_A$ = +125°C | | −10 | | 10 | |
| $I_{CC}$ | Operating Supply Current | $V_{CC}$ = Max, $\overline{CS} \leq V_{IL}$ (9244 only) | $T_A$ = 0°C | Standard devices | | | 70 | mA |
| | | | | L devices | | | 50 | |
| | | | $T_A$ = −55°C | Standard devices | | | 80 | |
| | | | | L devices | | | 60 | |
| $I_{PD}$ | Automatic $\overline{CS}$ Power Down Current | $V_{CC}$ = Max, $\overline{CS} \geq V_{IH}$ | $T_A$ = 0°C | 9244 | | | 30 | mA |
| | | | | 92L44 | | | 20 | |
| | | | $T_A$ = −55°C | 9244 | | | 33 | |
| | | | | 92L44 | | | 22 | |

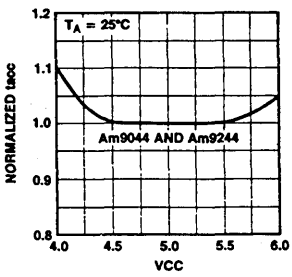
## DC OPERATING CHARACTERISTICS

**Typical ICC Versus VCC Characteristics**



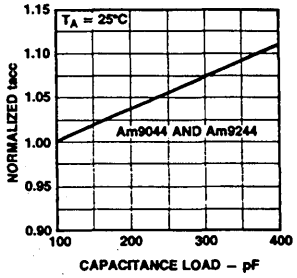

OP000890

**Typical tacc Versus VCC Characteristics**




OP000900

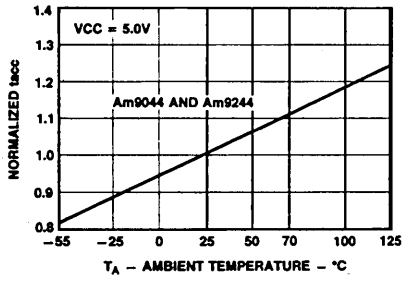
**Typical C Load Versus Normalized tacc Characteristics**




OP000910

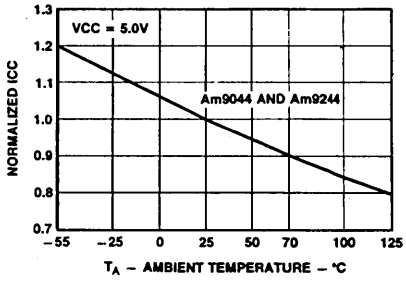
## DC OPERATING CHARACTERISTICS (Cont.)

**Normalized tacc Versus Ambient Temperature**




OP000920

**Normalized ICC Versus Ambient Temperature**




OP000930

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

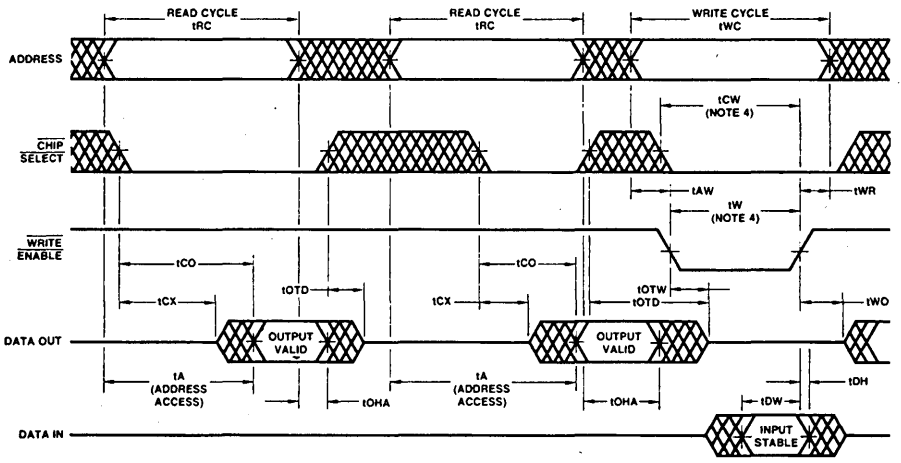
| No. | Symbol | Description | | B devices Min | B devices Max | C devices Min | C devices Max | D devices Min | D devices Max | E devices Min | E devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | | | |
| 1 | $t_{RC}$ | Address Valid to Address Do Not Care Time (Read Cycle Time) | | 450 | | 300 | | 250 | | 200 | | |
| 2 | $t_A$ | Address Valid to Data Out Valid Delay (Address Access Time) | | | 450 | | 300 | | 250 | | 200 | |
| 3 | $t_{CO}$ | Chip Select Low to Data Out Valid (Note 5) | Am9044 | | 100 | | 100 | | 70 | | 70 | |
| | | | Am9244 | | 450 | | 300 | | 250 | | 200 | ns |
| 4 | $t_{CX}$ | Chip Select Low to Data Out On | | 20 | | 20 | | 20 | | 20 | | |
| 5 | $t_{OTD}$ | Chip Select High to Data Out Off | | | 100 | | 80 | | 60 | | 60 | |
| 6 | $t_{OHA}$ | Address Unknown to Data Out Unknown Time | | 20 | | 20 | | 20 | | 20 | | |
| **Write Cycle** | | | | | | | | | | | | |
| 7 | $t_{WC}$ | Address Valid to Address Do Not Care Time (Write Cycle Time) | | 450 | | 300 | | 250 | | 200 | | |
| 8 | $t_W$ | Write Enable Low to Write Enable High Time (Note 4) | Am9044 | 200 | | 150 | | 100 | | 100 | | |
| | | | Am9244 | 250 | | 200 | | 150 | | 150 | | |
| 9 | $t_{WR}$ | Write Enable High to Address Do Not Care Time | | 0 | | 0 | | 0 | | 0 | | |
| 10 | $t_{OTW}$ | Write Enable Low to Data Out Off Delay | | | 100 | | 80 | | 60 | | 60 | |
| 11 | $t_{DW}$ | Data In Valid to Write Enable High Time | | 200 | | 150 | | 100 | | 100 | | |
| 12 | $t_{DH}$ | Write Enable Low to Data In Do Not Care Time | | 0 | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{AW}$ | Address Valid to Write Enable Low Time | | 0 | | 0 | | 0 | | 0 | | |
| 14 | $t_{PD}$ | Chip Select High to Power Low Delay (Am9244 only) | | | 200 | | 150 | | 100 | | 100 | |
| 15 | $t_{PU}$ | Chip Select Low to Power High Delay (Am9244 only) | | 0 | | 0 | | 0 | | 0 | | |
| 16 | $t_{CW}$ | Chip Select Low to Write Enable High Time (Note 4) | Am9044 | 200 | | 150 | | 100 | | 100 | | |
| | | | Am9244 | 250 | | 200 | | 150 | | 150 | | |
| 17 | $t_{WO}$ | Write Enable High To Output Turn On | | | 100 | | 100 | | 70 | | 70 | |

4



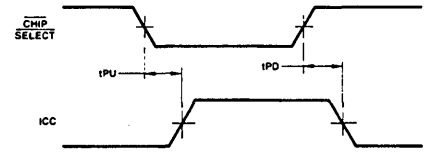
03254C

## SWITCHING WAVEFORMS




WF000190

## Power Down Waveform (Am 9244 only)




WF000180

# Am9064

65,536 x 1 Dynamic RAM

## DISTINCTIVE CHARACTERISTICS

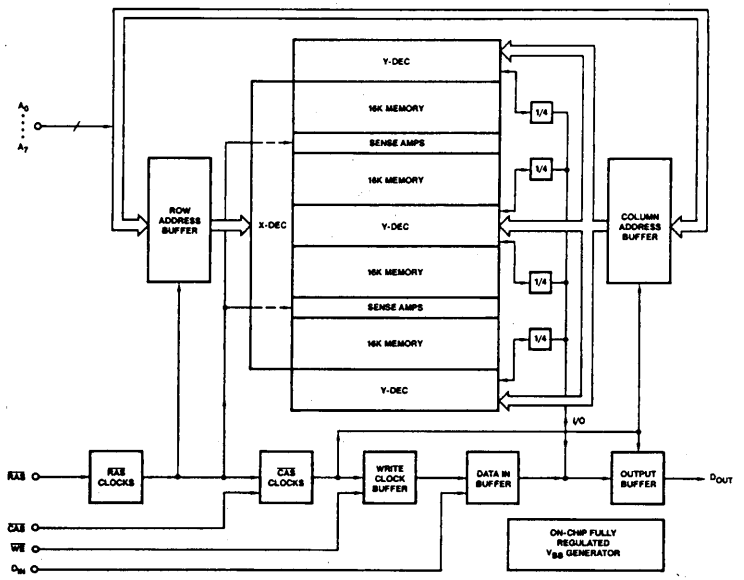
- High speed $\overline{RAS}$ access of 100 and 120ns
- Single +5V ±10% power supply
- Low power 22mW standby
  - 330mW active — 220ns cycle time
  - 385mW active — 190ns cycle time
- Read, Write, Read-Modify-Write, Page-Mode and $\overline{RAS}$-Only refresh capability
- $\overline{CAS}$ controlled three-state output
- Fast cycle times of 190 and 220ns

## GENERAL DESCRIPTION

The Am9064 is a high speed, high-performance dynamic RAM, organized 65,536 x 1 and manufactured using advanced NMOS silicon-gate technology. The design is optimized for both high speed and low power dissipation, and only a single +5V supply is needed because the on-chip substrate-bias generator (compensated for temperature and supply variations) provides the necessary back bias.

The Am9064 features multiplexed addressing, and all input signals, including clocks, are TTL-compatible; input and output signals are the same polarity, and the three-state output buffer is $\overline{CAS}$ controlled. The Hi-C single-transistor memory cell is used to enhance signal margin and reduce the $\alpha$-particle-induced soft-error rate.

## BLOCK DIAGRAM



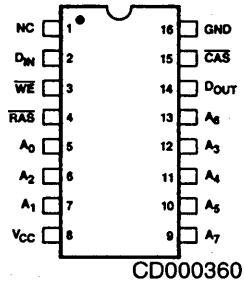

BD000150

## PRODUCT SELECTOR GUIDE

| Part Number | Am9064-10 | Am9064-12 | Am9064-15 |
|---|---|---|---|
| $\overline{RAS}$ Access Time | 100 | 120 | 150 |
| $\overline{CAS}$ Access Time | 55 | 65 | 75 |

03759B

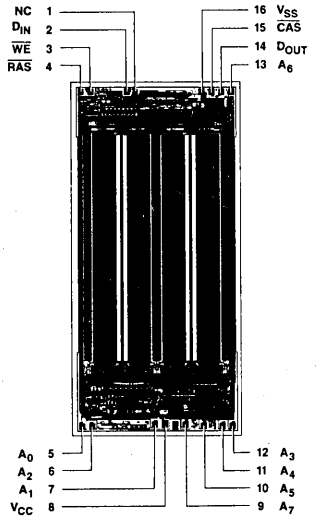
## CONNECTION DIAGRAM
## TOP VIEW




CD000360

Note: Pin 1 is marked for orientation

## Metallization and Pad Layout




Die Size
(Incl. Strip-Chip)
145 Mils x 313 Mils

## ORDERING INFORMATION

**Am9064-10 P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
- P — Package
  - D – 16-pin CERDIP
  - P – 16-pin plastic
- 10 — Speed Select
  - 10 – 100ns
  - 12 – 120ns
  - 15 – 150ns
- Am9064 — Device Type
  - 64k x 1 DRAM

| Valid Combinations | |
|---|---|
| Am9064-10<br>Am9064-12<br>Am9064-15 | PC, DC |

## PIN DESCRIPTION

**$A_0 - A_7$** Eight multiplexed inputs, first provide eight row address inputs and then eight column address inputs, all within one normal memory cycle. The eight row address inputs (meeting the setup and hold times $t_{ASR}$ and $t_{RAH}$) are latched in by $\overline{RAS}\downarrow$. The eight column address inputs, (meeting the setup and hold times $t_{ASC}$, $t_{CAH}$ and $t_{AR}$ are latched in by $\overline{CAS}\downarrow$. The combined row and column address inputs (16 total) will select one of 65,536 memory bits for Read, Write, or Read-Modify-Write operation. In addition, the memory refresh function is also performed in any memory cycle (including $\overline{RAS}$ only refresh cycle), on two of 256 rows specified by $A_0 - A_6$, while $A_7$ is not used. Page-mode cycles excluded.)

**$D_{IN}$** The Data Input. The data input, (meeting setup and hold times $t_{DS}$, $t_{DH}$ and $t_{DHR}$) is latched in by either $\overline{WE}\downarrow$ or $\overline{CAS}\downarrow$ whichever comes later, while $\overline{RAS}$ is LOW.

**$\overline{RAS}$** The Row-Address-Strobe control clock. $\overline{RAS}\downarrow$ latches the row address on $A_0 - A_7$ and activates a memory cycle. $\overline{RAS}\uparrow$ ends the active memory cycle and precharges the memory's dynamic circuits. Memory cycle time, as defined by the $\overline{RAS}$ clock, has a very large operating range; however $\overline{RAS}$ LOW pulse width ($t_{RAS}$) and $\overline{RAS}$ HIGH pulse width ($t_{RP}$ must satisfy the specified minimum and maximum values in order to maintain continuous memory operation and data retention. $\overline{RAS}$ alone controls memory refresh function.

**$\overline{CAS}$** The Column-Address-Strobe control clock. With $\overline{RAS}$ LOW, $\overline{CAS}\downarrow$ latches the column address and activates the memory input and output operations. With $\overline{WE}$ LOW, $\overline{CAS}$ controls the input timing; with $\overline{WE}$ HIGH, $\overline{CAS}$ controls the timing of valid output. $\overline{CAS}$ HIGH turns off $D_{OUT}$ ($D_{OUT}$ = high impedance). In page-mode, $\overline{CAS}$ cycle time defines the page-mode cycle time.

**$\overline{WE}$** The Write Enable Control Clock. $\overline{WE}$ timing relative to $\overline{CAS}$ and $\overline{RAS}$ will define one of three memory cycles. 1) $\overline{RAS}$ and $\overline{CAS}$ both LOW, and $\overline{WE}$ HIGH will define a read cycle; 2) $\overline{WE}$ LOW (meeting the setup and hold times $t_{WCS}$, $t_{WCH}$ and $t_{WCR}$) will define an Early Write Cycle; 3) $\overline{WE}$ first HIGH and then LOW (meeting $t_{CWD}$ and $t_{RWD}$ delay times) will define a Read-Write/Read-Modify-Write Cycle.

**$D_{OUT}$** The three-state output. The $D_{OUT}$ is controlled mainly by $\overline{CAS}$. Valid output appears on $D_{OUT}$ in a Read Cycle after access time has elapsed ($t_{CAC}$ or $t_{RAC}$, whichever applies). Last valid $D_{OUT}$ remains valid as long as $\overline{CAS}$ is LOW. $D_{OUT}$ can be turned off only with $\overline{CAS}\uparrow$.

## APPLICATION INFORMATION

### DEVICE DESCRIPTION

The Am9064 is a state-of-the-art high performance 64K DRAM combining the fastest DRAM speed available (100ns access time) with low power (standby current < 4mA). It is designed to operate with a single +5V power supply, and all inputs/output voltage levels are TTL compatible, making the Am9064 easy to integrate into a wide range of systems. The Am9064 is offered in two grades of operating ambient temperature range, the commercial grade (Am9064-12DC) covers from 0 to +70°C and the extended grade (Am9064-12CDC) covers from −55 to +110°C military applications. Where the memory system reliability is of primary importance, the Am9064 design provides the solution with the following safety features:

**The Am9064:**

- Allows $V_{CC}$ power-up with floating input levels without causing excess $I_{CC}$ current surges (see Initialization).

Can tolerate real time $V_{CC}$ fluctuation between 4.5 and 5.5V while memory chip is in operation.

- Accepts input voltage transition overshoot ($V_{CC}$ +1V) and undershoot (−2V).
- Is fabricated with an NMOS technology that is optimized to provide very high 64K DRAM device latch-up voltage, typically in excess of 10V; (however, it is not recommended to operate Am9064 with $V_{CC}$ over +7V; see Maximum Ratings).

The fast switching characteristics of the Am9064 are designed to fit into memory system constraints. For a fast Read Cycle, Am9064 offers fast $t_{CAC}$ (about 50 to 55% of $t_{RAC}$), thus providing 45 to 50% of $t_{RAC}$ access time for address multiplexing on a memory board. For a Write operation, fast $t_{RWL}$ and $t_{CWL}$ allow fast Read-Write or Read-Modify-Write cycles, useful for memory systems which include Error Detection/Correction (EDC) schemes to boost memory reliability. (For a detailed reference on EDC, see "Am2960 Series Dynamic Memory Support Handbook," AMD Application.)

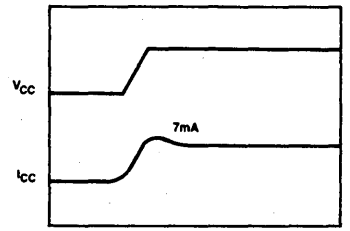
The Am9064 includes all standard 64K DRAM memory cycles: Read, Early Write (for the case of common I/O), Read-Write or Read-Modify-Write, $\overline{RAS}$-Only Refresh, and Page-Mode cycles. Two clock inputs ($\overline{RAS}$ and $\overline{CAS}$) are needed to latch the multiplexed row and column addresses on the eight address inputs, $A_0 - A_7$, and a third clock input ($\overline{WE}$) distinguishes between Read and Write cycles. Proper input or output operation on each memory bit requires all three timing control clocks ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$). Memory refresh operation is most efficient through the $\overline{RAS}$-Only Refresh Cycle when using a dynamic RAM controller like Am2964B. The Am9064 accomplishes 128 refresh cycles ($A_0 - A_6$) in 2ms and 256 refresh cycles ($A_0 - A_7$) in 4ms. Multiplexed address inputs allow the Am9064 to be packaged in a standard 16-pin DIP with pin 1 not connected. With pin 1 uncommitted, the Am9064 is compatible with the JEDEC standards for the 64K DRAM and allows for future expansion to 256K DRAM.

### DEVICE INITIALIZATION

An initial pause of 100μs is required after $V_{CC}$ power-up. This time delay is needed for the on-chip substrate-bias generator to pump enough negative charge into the substrate to establish the operating back bias voltage. This is followed by a wake-up sequence of eight (8) $\overline{RAS}$ cycles to initialize the internal dynamic circuits. If the device remains in standby

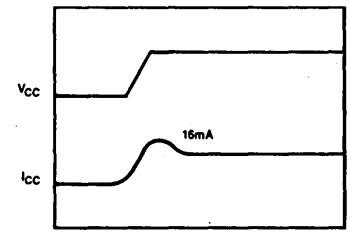
mode for more than 2ms while $V_{CC}$ is on, the wake-up sequence of any eight $\overline{RAS}$ cycles will be necessary prior to normal operation. A power-up safety feature has been designed into the Am9064; special circuits within the chip prevent current surges during initial system power-up. These circuits allow the Am9064 to be powered up to a standby mode (where current is low and output is in high impedance) independent of the initial $\overline{RAS}$ input logic level. (See Figures 1 and 2). The power-up circuit is completely transparent to normal circuit operation.

**Figure 1. $V_{CC}$ Supply Current Waveform during $V_{CC}$ Power up, $\overline{RAS} = \overline{CAS} = V_{CC}$**




AF000010

**Figure 2. $V_{CC}$ Supply Current Waveform during $V_{CC}$ Power Up, $\overline{RAS} = \overline{CAS} = V_{SS}$**




AF000020

### ADDRESSING

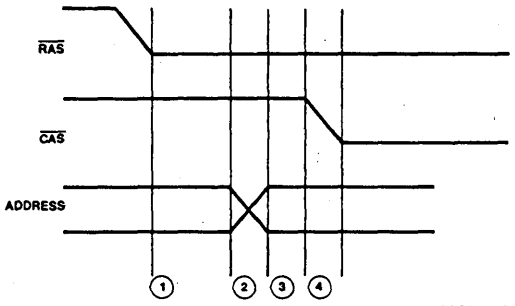
Eight address inputs are multiplexed to provide 16 address bits. The first set of eight address inputs (Row address) is latched by $\overline{RAS}$, and the second set (Column address) is latched by $\overline{CAS}$. Together, the 16 address bits will decode one of 65,536 cell locations.

Proper address multiplexing requires that $\overline{CAS}$ follow $\overline{RAS}$ by a specified delay time ($t_{RCD}$). Minimum $t_{RCD}$ is determined by the following equation:

$t_{RCD}$ (min) = $t_{RAH}$ + 2$t_T$ + $t_{ASC}$ where $t_{RAH}$ and $t_{ASC}$ are specified DRAM characteristics, and 2$t_T$ are the address and $\overline{CAS}$ transition times, dependent on the memory board design. The maximum $t_{RCD}$ is derived from the access time limits.

$t_{RCD}$ (max) = $t_{RAC}$ − $t_{CAC}$. If $t_{RCD}$ (max) is exceeded, the access time will be determined by $t_{CAC}$. The multiplex timing window of interest for system design is $t_{RCD}$ (max) — $t_{RAH}$ (see Figure 3).

**Figure 3. Address Multiplex Timing Window**
**$t_{RCD}$ (Max) - $t_{RAH} \geq 2$ ($t_T$ + Skew) + $t_{ASC}$**




AF000030

① $t_{RAH}$
② $t_T$ + skew (address input $A_0$-$A_7$ relative to $\overline{RAS}$)
③ $t_{ASC}$
④ $t_T$ + skew ($\overline{CAS}$ relative to $\overline{RAS}$)

## OPERATING CYCLES

### READ CYCLE

The Memory Read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from HIGH to LOW. The $\overline{CAS}$ clock must also make a transition from HIGH to LOW at the specified $t_{RCD}$ timing limits when the column addresses are latched. These clocks are linked in such a manner that the access time of the device is independent of the address multiplex window, however the $\overline{CAS}$ clock must be active before or at the $t_{RCD}$ maximum for an access (data valid) from the $\overline{RAS}$ clock edge to be valid ($t_{RAC}$). If the $t_{RCD}$ maximum condition is not met, the access ($t_{CAC}$) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as shown in the functional block diagram. This gating feature on the $\overline{CAS}$ clock allows the external $\overline{CAS}$ signal to become active as soon as the row address hold time ($t_{RAH}$) specification has been met and thus defines the $t_{RCD}$ minimum specification. The time difference between $t_{RCD}$ minimum and $t_{RCD}$ maximum can be used to absorb skew delays in switching the address bus from row to column addresses to generate the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for certain minimums ($t_{RAS}$ for the $\overline{RAS}$ clock; $t_{CAS}$ for the $\overline{CAS}$ clock) and the $\overline{RAS}$ clock must stay inactive for a minimum time ($t_{RP}$). The former is for the completion of the cycle in progress and the latter allows the device internal circuitry to be precharged for the next active cycle.

$D_{OUT}$ is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the high impedance mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10ns ($t_{CRP}$) into the next cycle. To perform a Read Cycle, the Write Enable ($\overline{WE}$) input must be held HIGH from the time the $\overline{CAS}$ clock makes its active transition ($t_{RCS}$) to the time when it transitions into the inactive mode ($t_{RCH}$).

### WRITE CYCLE

A Write Cycle is similar to a Read Cycle except that the Write Enable ($\overline{WE}$) clock must go active LOW at or before the time that the $\overline{CAS}$ clock goes active. In this case the cycle in progress is referred to as an early Write Cycle. In an early Write Cycle, the Write Clock and $D_{IN}$ are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the Write Cycle: the

column-strobe-to-write lead time ($t_{CWL}$) and the row-strobe-to-write lead time ($t_{RWL}$). These are the minimum times that the $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{WE}$ clock LOW).

It is also possible to perform a late Write Cycle. For this cycle, the Write Clock is activated after $\overline{CAS}$ goes LOW, which is beyond $t_{WCS}$ minimum time so the parameters $t_{CWL}$ and $t_{RWL}$ must be satisfied before terminating this cycle. The difference between an early Write Cycle and a late Write Cycle is that in a late Write Cycle the Write Enable clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — ($t_{RWL} + t_{RP} + 2t_T$).

At the start of a Write Cycle. $D_{OUT}$ is in a Hi-Z condition and remains so throughout the cycle. It remains Hi-Z because the active transition of the Write Enable clock prevents the $\overline{CAS}$ clock from enabling the output buffers, as shown in the Functional Block Diagram. This characteristic can be effectively utilized in a system that has a common input/output bus, with the only stipulation being the system must use only the early write mode.

### READ-MODIFY-WRITE AND READ-WRITE CYCLES

As the name implies, both a Read and a Write Cycle are accomplished at the same cell location during a single access. The Read-Modify-Write Cycle is similar to the late Write Cycle discussed above.

For the Read-Modify-Write Cycle, a normal Read Cycle is initiated with the $\overline{WE}$ clock HIGH. After the data is read, $\overline{WE}$ is transitioned to LOW and $D_{IN}$ is setup and held with respect to the active edge of $\overline{WE}$. This cycle assumes a zero modify time between read and write.

Another variation of the Read-Modify-Write Cycle is the Read-Write Cycle, in which the two parameters, $t_{RWD}$ and $t_{CWD}$ play an important role. A Read-Write Cycle starts as a normal Read Cycle with the $\overline{WE}$ clock being transitioned at minimum $t_{RWD}$ or minimum $t_{CWD}$ time, depending upon the application. This results in starting a write operation to the selected cell even before $D_{OUT}$ occurs. In this case, $D_{IN}$ is set up with respect to the $\overline{WE}$ clock active edge.

### PAGE-MODE CYCLES

Page-mode operation allows faster successive data operations at the 256 column locations. Page access ($t_{CAC}$) on the Am9064 is typically half the regular $\overline{RAS}$ clock access ($t_{RAC}$). Page-mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit address field. There are two controlling factors which serve to limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on-time limits the number of sequential page accesses possible. Ten microseconds will provide approximately 50 successive page accesses for every row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal Read or Write cycle, followed by the shorter $\overline{CAS}$ cycles ($t_{PC}$). The $\overline{CAS}$ cycle time ($t_{PC}$) consists of the $\overline{CAS}$ clock active time, ($t_{CAS}$) the $\overline{CAS}$ clock precharge time ($t_{CP}$) and two transitions. In addition to Read and Write cycles, a Read-Modify-Write Cycle can also be performed in a page-mode operation. For a Read-Modify-Write or Read-Write type cycle, the conditions normal to that mode of operation will apply in the page-mode also. Any combination of Read, Write and Read-Modify-Write cycles can be performed to suit any particular application.

### REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature; therefore, to retain the correct information, the bits need to be refreshed at least once every 2ms. This is accomplished by sequentially cycling through the 128 row address locations every 2ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with the particular row decoded.

### $\overline{RAS}$-Only Refresh

When the memory component is in standby, the $\overline{RAS}$-Only Refresh scheme is employed. This refresh method performs a $\overline{RAS}$-Only cycle on all 128 row addresses every 2ms; the row addresses are latched with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. The $\overline{CAS}$ clock is not required and should be inactive, or HIGH, to conserve power.

### DATA OUTPUT OPERATION

The Am9064 has a $\overline{CAS}$ controlled three-state data output ($D_{OUT}$) which remains valid from the access time as long as $\overline{CAS}$ is LOW. $d_{OUT}$ can be turned off to the high impedance state only when $\overline{CAS}$ is HIGH, and remains in Hi-Z as long as $\overline{CAS}$ stays HIGH. The output data is the same polarity as the input data. The following table summarizes the $D_{OUT}$ state for various cycles.

| Type of Cycle | | $D_{OUT}$ |
|---|---|---|
| Read Cycle | | Data from Addressed Memory Cell |
| Early Write Cycle | | Hi-Z |
| Delayed Write Cycle | | Indeterminate, until after $t_{RAC}$ and $t_{CAC}$ |
| $\overline{RAS}$ Refresh Cycles | $\overline{CAS}$ HIGH | Hi-Z |
| | $\overline{CAS}$ LOW | Data from Last Read Cycle |
| $\overline{CAS}$-Only Cycle $\overline{RAS}$ HIGH | | Hi-Z |
| Read-Modify-Write Cycle | | Data from Addressed Memory Cell |

### ON-CHIP SUBSTRATE-BIAS GENERATOR

The Am9064 has an on-chip substrate-bias ($V_{BB}$) generator integrated into the DRAM peripheral circuitry. This accomplishes three purposes:

1. It allows the use of single +5V supply ($V_{CC}$), so it does away with the need for an external $V_{BB}$ supply. This has become the standard for all NMOS DRAMs 64K and higher.
2. It maintains the high performance of the N-channel MOSFET by providing a stable negative voltage bias (−3V) on the p-type substrate, reducing the parasitic PN junction capacitance and the body effect of the MOSFET threshold voltage.
3. It avoids minority charge injection from a node voltage undershoot to −2V on all inputs.

In addition to the above design features, the fact that the bias generator* is incorporated on-chip makes it possible to shield the $V_{BB}$ bias level from any fluctuations of the external $V_{CC}$ power supply. This on-chip generator has the following characteristics:

1. $V_{BB}$ level is independent of $V_{CC}$, for $V_{CC} \geq 3V$.
2. $V_{BB}$ level is compensated for temperature variation.
3. Upper and lower levels of $V_{BB}$ are regulated.

In summary, the $V_{BB}$ bias-generator can tolerate a $V_{CC}$ range of 3 to 8V, temperature range of −55 to +110°C, and cycle dependent capacitive coupling.

## ALPHA-PARTICLE-INDUCED SOFT ERRORS

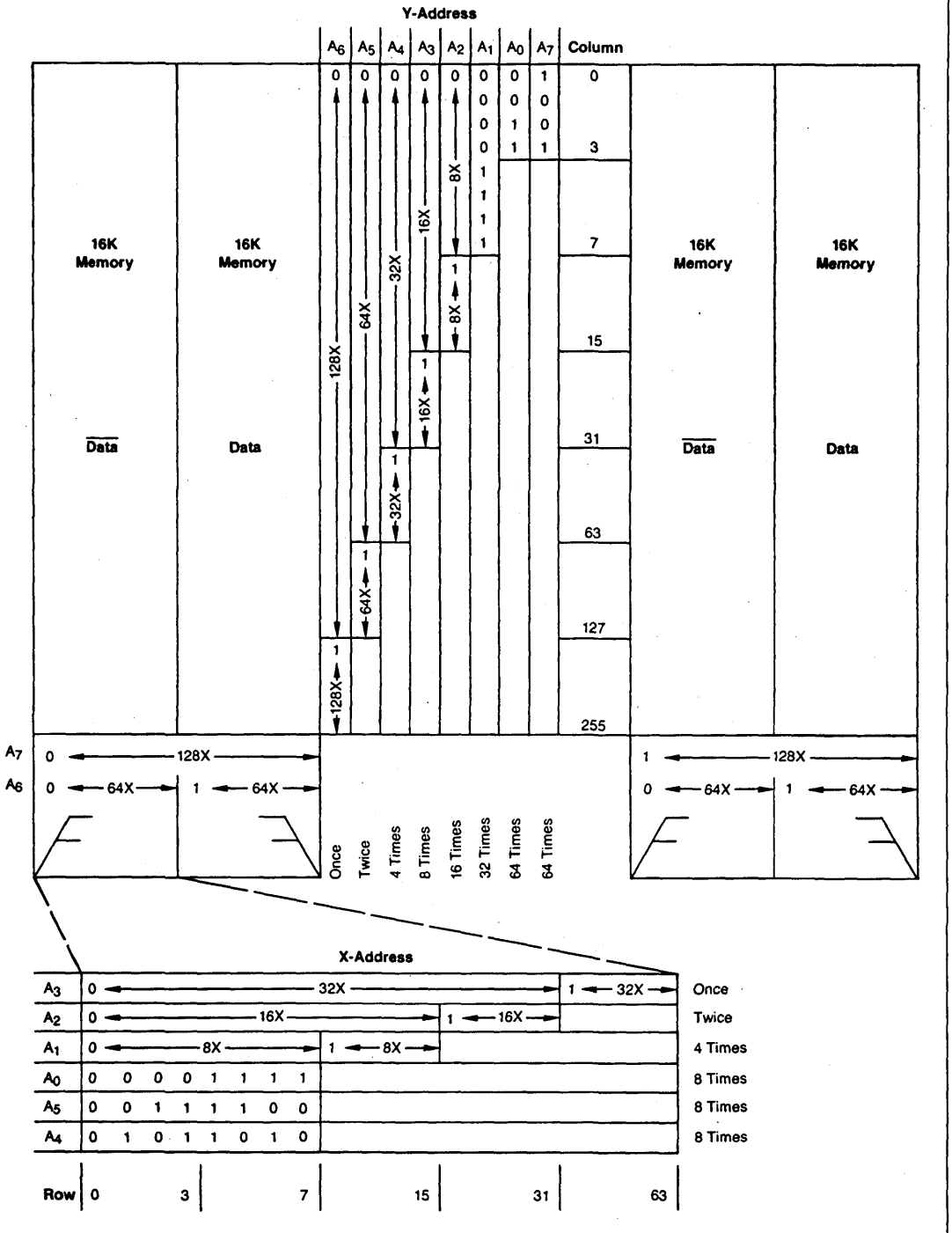
One of the primary causes of soft errors in DRAMs is due to the presence of alpha-particles emitted from the decay of uranium and thorium in the IC packaging materials. When an alpha-particle enters the silicon chip substrate, approximately one million electron-hole pairs are created in the bulk silicon. These generated carriers diffuse and the electrons are collected by depletion layers resulting in the partial or total filling of initially empty potential wells. If the "collection efficiency" times the number of generated carriers exceeds the critical charge in the memory cell a "soft error" will result. A recently published study (*"Drift Collection of Alpha Generated Carriers and Design Implications,"* C. Hu, ISSCC 82) shows that the "collection efficiency" is directly proportional to the width of the depletion layers. Solutions to the alpha problem are implemented in the Am9064 in the following ways:

1. Incorporation of new process technology for the Hi-C* capacitor memory cell.
2. Using low-alpha-source packaging materials.

The Hi-C* capacitor memory cell helps solve the alpha problem in two significant ways. First, it increases the memory charge storage by ~ 30%, thus boosting up the "critical charge." Second, it reduces the memory cell junction depletion width by a factor of ~ 5 to 10, thus reducing the collection efficiency significantly.

*Patent pending.

## AM9064 TOPOLOGICAL BIT MAP

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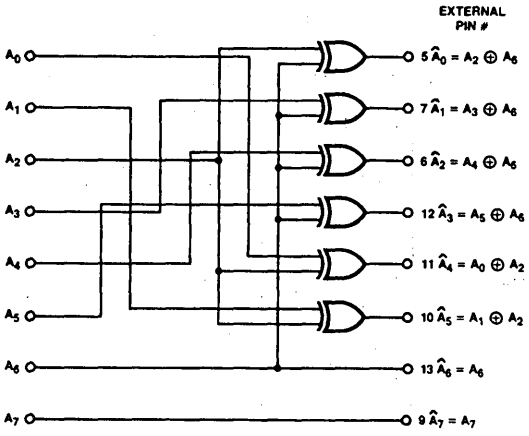
## ROW TOPOLOGICAL DESCRAMBLE




Ân = EXTERNAL OR PIN ADDRESS
An = INTERNAL ADDRESS

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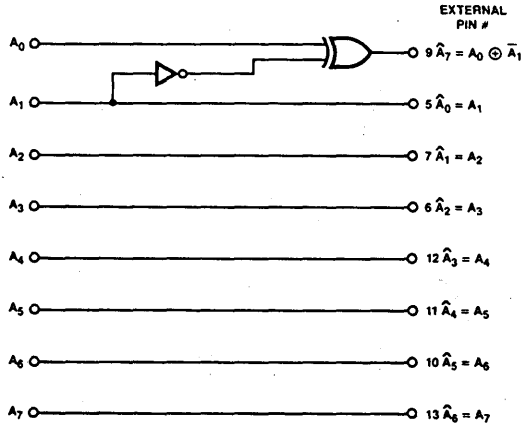
## COLUMN TOPOLOGICAL DESCRAMBLE




Ân = EXTERNAL OR PIN ADDRESS
An = INTERNAL ADDRESS

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −10°C to +80°C
Voltage on any pin with
respect to ground ..... −2V to +7.5V
Supply Voltage ..... −1V to +7.5V
Power Dissipation ..... 1.0W
Short Circuit Output Current ..... 50mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Temperature ..... 0°C to +70°C

Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

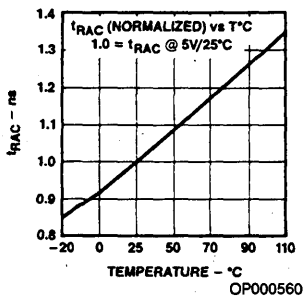
## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Operating Current (Note 1) Average Power Supply Current | $\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC}$ = Min | Am9064-10 | – | 70 | mA |
| | | | AM9064-12 | – | 60 | |
| | | | Am9064-15 | – | 55 | |
| $I_{CC2}$ | Standby Current Power Supply Current | $\overline{RAS} = \overline{CAS} = V_{IH}$ | | – | 4.0 | mA |
| $I_{CC3}$ | Refresh Current (Note 1) Average Power Supply Current | $\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$; $t_{RC}$ = Min | Am9064-10 | – | 55 | mA |
| | | | Am9064-12 | – | 50 | |
| | | | Am9064-15 | – | 45 | |
| $I_{CC4}$ | Page Mode Current (Note 1) Average Power Supply Current | $\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling; $t_{PC}$ = Min | Am9064-10 | – | 50 | mA |
| | | | Am9064-12 | – | 45 | |
| | | | Am9064-15 | – | 40 | |
| $I_{ILK}$ | Input Leakage Current | Any Input; $V_{SS} \leq V_{IN} \leq V_{CC}$ | | −10 | +10 | µA |
| $I_{OLK}$ | Output Leakage Current | Data Out Disabled, $V_{SS} \leq V_{OUT} \leq V_{CC}$ | | −10 | +10 | µA |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −5.0mA | | 2.4 | | – |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = +4.2mA | | – | 0.4 | V |
| $C_{IN1}$ | Input Capacitance $A_0 - A_7, D_{IN}$ | | | | 5 | pF |
| $C_{IN2}$ | Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | | | | 7 | pF |
| $C_{OUT}$ | Output Capacitance $D_{OUT}$ | | | | 6 | pF |

Note: 1 $I_{CC}$ is depedent on output loading and cycle time. Specified values are measured with output open.

## DC OPERATING CHARACTERISTICS

**Typical Access Time (Normalized) $t_{RAC}$ versus Case Temperature**



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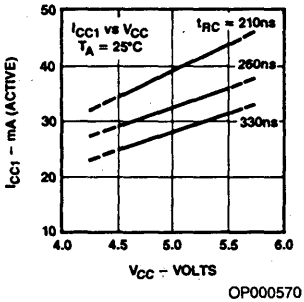
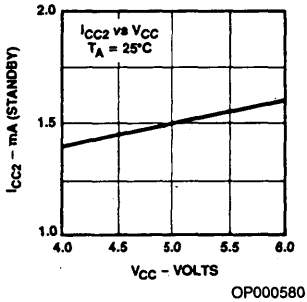
**Typical Operating Current $I_{CC1}$ versus $V_{CC}$**



OP000570

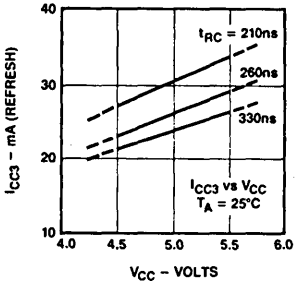
**Typical Standby Current $I_{CC2}$ versus $V_{CC}$**



OP000580

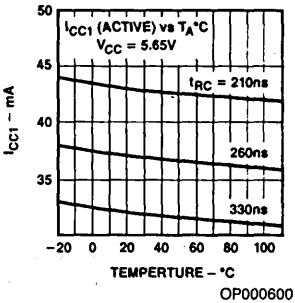
## DC OPERATING CHARACTERISTICS (Cont.)

**Typical Refresh Current $I_{CC3}$ versus $V_{CC}$**




OP000590

**Typical Operating Current $I_{CC1}$ versus Case Temperature**

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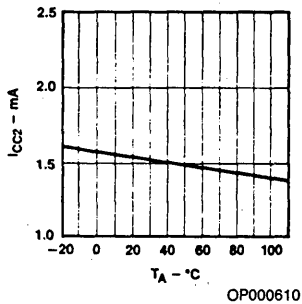
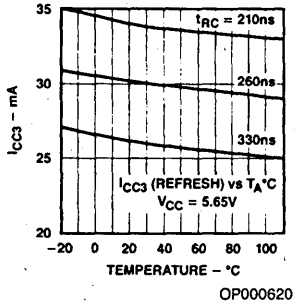
**Typical Standby Current $I_{CC2}$ versus Case Temperature**



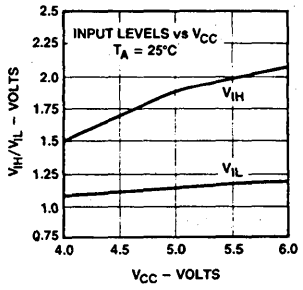

OP000610

**Typical Refresh Current $I_{CC3}$ versus Case Temperature**



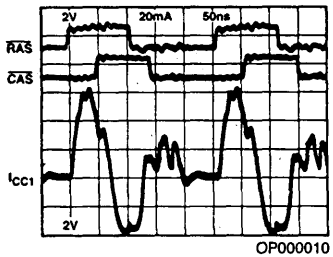

OP000620

**Input Voltage Levels versus $V_{CC}$**



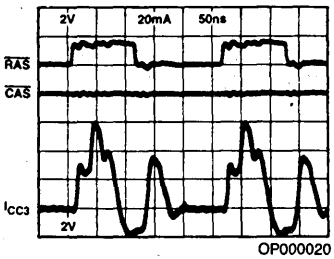

OP000630

**$\overline{RAS}/\overline{CAS}$ Cycle**




OP000010

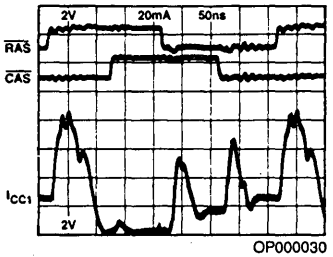
**Long $\overline{RAS}/\overline{CAS}$ Cycle**




OP000020

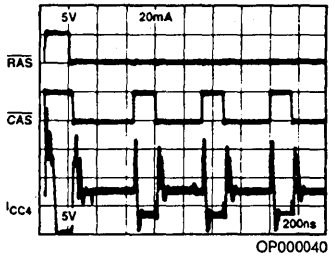
## DC OPERATING CHARACTERISTICS (Cont.)

**$\overline{RAS}$ Only Cycle**




OP000030

**Page-Mode Only**




OP000040

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am9064-10 Min | Am9064-10 Max | Am9064-12 Min | Am9064-12 Max | Am9064-15 Min | Am9064-15 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{RAC}$ | Access Time from $\overline{RAS}$ (Notes 6 and 7) | | 100 | | 120 | | 150 | ns |
| 2 | $t_{CAC}$ | Access Time from $\overline{CAS}$ (Notes 6 and 7) | | 55 | | 65 | | 75 | ns |
| 3 | $t_{REF}$ | Time Between Refresh | | 2 | | 2 | | 2 | ms |
| 4 | $t_{RP}$ | $\overline{RAS}$ Precharge Time | 80 | | 90 | | 100 | | ns |
| 5 | $t_{CPN}$ | $\overline{CAS}$ Precharge Time (Non-Page Cycles) | 30 | | 30 | | 30 | | ns |
| 6 | $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | −10 | | −10 | | −10 | | ns |
| 7 | $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time (Notes 6 and 8) | 25 | 45 | 30 | 55 | 30 | 75 | ns |
| 8 | $t_{RSH}$ | $\overline{RAS}$ Hold Time | 55 | | 65 | | 75 | | ns |
| 9 | $t_{CSH}$ | $\overline{CAS}$ Hold Time | 100 | | 120 | | 150 | | ns |
| 10 | $t_{ASR}$ | Row Address Setup Time | 0 | | 0 | | 0 | | ns |
| 11 | $t_{RAH}$ | Row Address Hold Time | 15 | | 20 | | 20 | | ns |
| 12 | $t_{ASC}$ | Column Address Setup Time | 0 | | 0 | | 0 | | ns |
| 13 | $t_{CAH}$ | Column Address Hold Time | 25 | | 25 | | 30 | | ns |
| 14 | $t_{AR}$ | Column Address Hold Time to $\overline{RAS}$ | 70 | | 80 | | 105 | | ns |
| 15 | $t_T$ | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | 3 | 50 | ns |
| 16 | $t_{OFF}$ | Output Buffer Turn Off Delay (Note 9) | 0 | 35 | 0 | 40 | 0 | 40 | ns |
| **Read and Refresh Cycles** | | | | | | | | | |
| 17 | $t_{RC}$ | Random Read Cycle Time | 190 | | 220 | | 260 | | ns |
| 18 | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 100 | 10,000 | 120 | 10,000 | 150 | 10,000 | ns |
| 19 | $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 55 | 10,000 | 65 | 10,000 | 75 | 10,000 | ns |
| 20 | $t_{RCS}$ | Read Command Setup Time | 0 | | 0 | | 0 | | ns |
| 21 | $t_{RCH}$ | Read Command Hold Time to $\overline{CAS}$ (Note 10) | 0 | | 0 | | 0 | | ns |
| 22 | $t_{RRH}$ | Read Command Hold Time to $\overline{RAS}$ (Note 10) | 0 | | 0 | | 0 | | ns |
| **Write Cycle** | | | | | | | | | |
| 23 | $t_{RC}$ | Random Write Cycle Time | 190 | | 220 | | 260 | | ns |
| 24 | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 100 | 10,000 | 120 | 10,000 | 150 | 10,000 | ns |
| 25 | $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 55 | 10,000 | 65 | 10,000 | 75 | 10,000 | ns |
| 26 | $t_{WCS}$ | Write Command Setup Time (Note 11) | 0 | | −10 | | −10 | | ns |
| 27 | $t_{WCH}$ | Write Command Hold Time | 20 | | 25 | | 35 | | ns |
| 28 | $t_{WCR}$ | Write Command Hold Time to $\overline{RAS}$ | 65 | | 80 | | 110 | | ns |
| 29 | $t_{WP}$ | Write Command Pulse Width | 20 | | 25 | | 35 | | ns |
| 30 | $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 30 | | 40 | | 45 | | ns |
| 31 | $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 30 | | 40 | | 45 | | ns |
| 32 | $t_{DS}$ | Data in Setup Time (Note 12) | 0 | | 0 | | 0 | | ns |
| 33 | $t_{DH}$ | Data In Hold Time (Note 12) | 20 | | 25 | | 35 | | ns |
| 34 | $t_{DHR}$ | Data In Hold Time to $\overline{RAS}$ | 65 | | 80 | | 110 | | ns |
| **Read-Modify-Write Cycle** | | | | | | | | | |
| 35 | $t_{RWC}$ | Read-Modify-Write Cycle Time | 205 | | 240 | | 280 | | ns |
| 36 | $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay (Note 11) | 80 | | 95 | | 120 | | ns |
| 37 | $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay (Note 11) | 35 | | 40 | | 45 | | ns |
| **Page-Mode Cycle** | | | | | | | | | |
| 38 | $t_{PC}$ | Page-Mode Read or Write Cycle | 105 | | 120 | | 145 | | ns |
| 39 | $t_{CP}$ | $\overline{CAS}$ Precharge Time, Page-Mode | 40 | | 45 | | 60 | | ns |
| 40 | $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 55 | 10,000 | 65 | 10,000 | 75 | 10,000 | ns |

Notes:

1. $I_{CC}$ is dependent on output loading and cycle time. Specified values are measured with output open.
2. Capacitance measured with a Boonton Meter or calculated from the equation: $C = 1\Delta t/\Delta V$.
3. An initial pause of 100μsec is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. AC characteristics assume $t_T = 5$ns.
5. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between these two levels.
6. Maximum $t_{RCD}$ is specified as a reference point only. If $t_{RCD} \leq$ maximum allowed, access time is $t_{RAC}$. If $t_{RCD} > t_{RCD}$ (max), either access time is controlled exclusively by $t_{CAC}$, or $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the specified maximum.
7. Output load is equivalent to two standard TTL loads and 100pF.
8. $t_{RCD}$ (min) = $t_{RAH} + t_{ASC} + 2t_T$.
9. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a Read Cycle.
11. $t_{WCS}$, $t_{CWD}$ and $t_{RWD}$ are specified as reference points and are not restrictive operating parameters. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an early Write Cycle and the

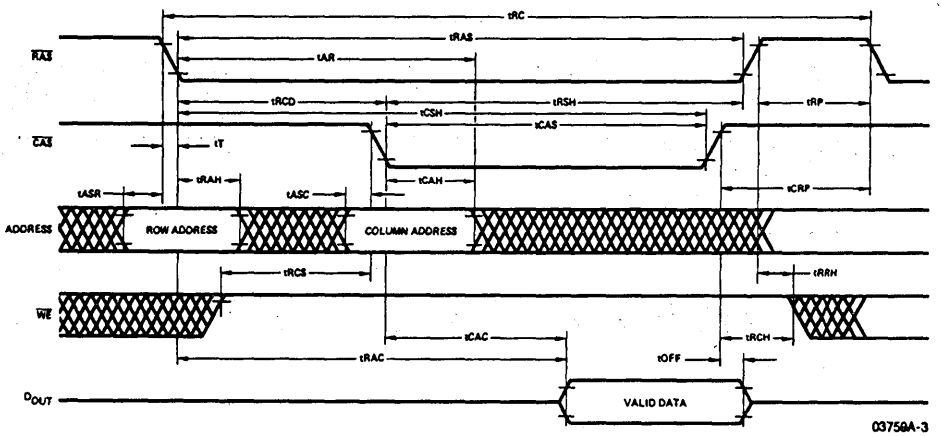
## SWITCHING CHARACTERISTICS (Cont.)

$D_{OUT}$ pin will remain Hi-Z throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is Read-Write Cycle and $D_{OUT}$ will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of $D_{OUT}$ (at access time) is indeterminate.

12. These parameters are referenced to $\overline{CAS}$ leading edge in early Write cycles and to $\overline{WE}$ leading edge in delayed Write or Read-Modify-Write cycles.

## SWITCHING WAVEFORMS

### READ CYCLE

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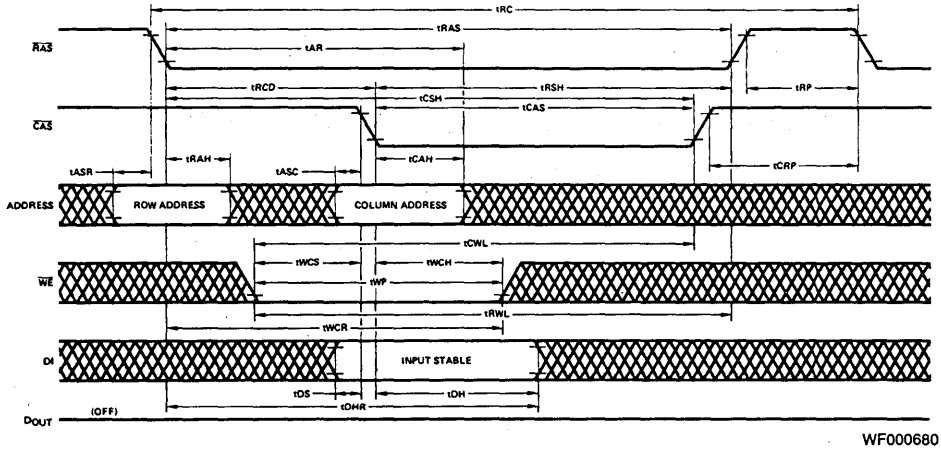
WF000480

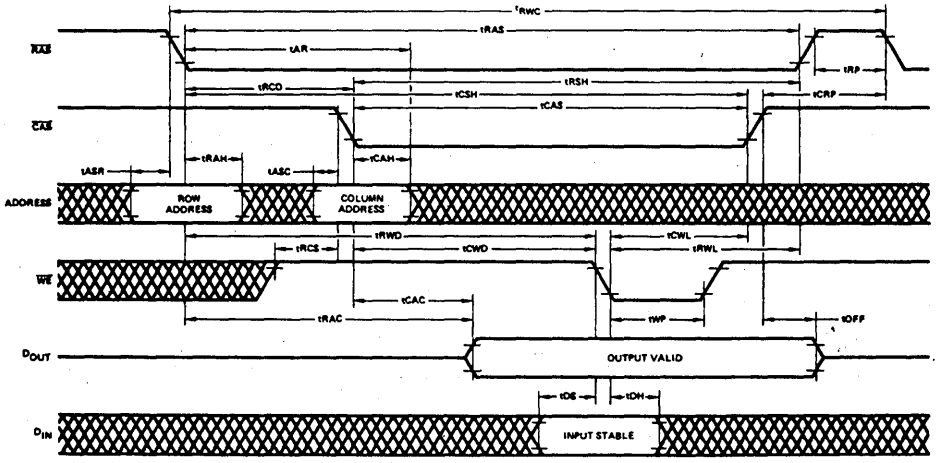
### WRITE CYCLE




WF000680

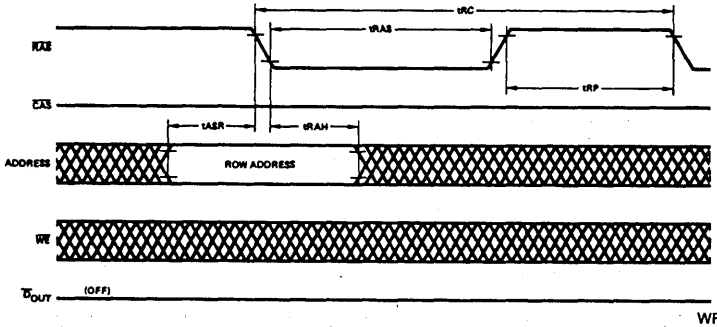
## SWITCHING WAVEFORMS (Cont.)

### READ-WRITE/READ-MODIFY-WRITE CYCLE




WF000690

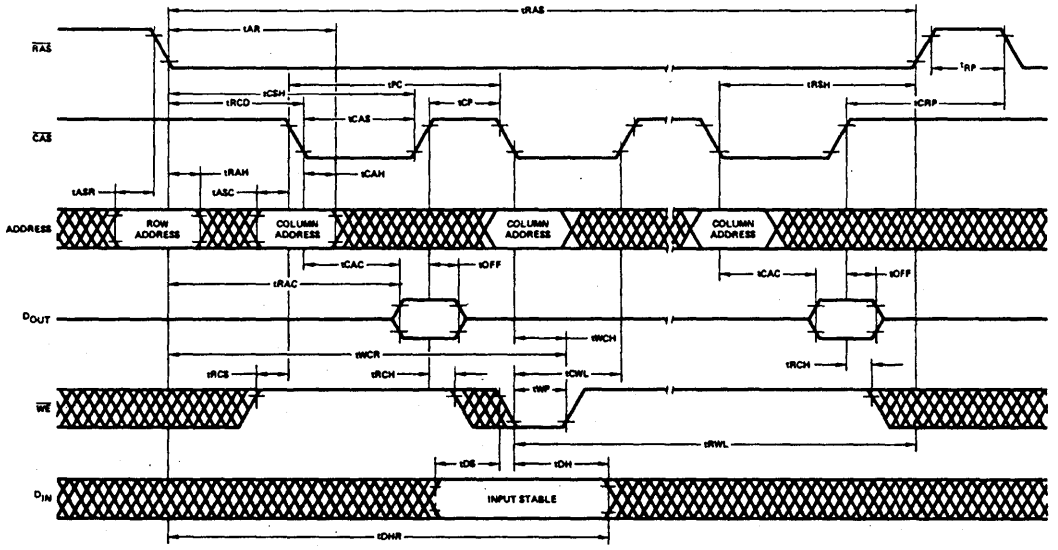
### RAS-ONLY REFRESH CYCLE




WF000370

## SWITCHING WAVEFORMS (Cont.)

### PAGE-MODE CYCLE




WF000380

# AM9101 Family

256 x 4 Static RAM

## DISTINCTIVE CHARACTERISTICS

- Low operating power
  125mW typ; 290mW maximum — standard power
  100mW typ; 175mW maximum — low power
- Logic voltage levels identical to TTL
- High output drive — two full TTL loads
- High noise immunity — full 400mV
- Two chip enable inputs
- Output disable control

## GENERAL DESCRIPTION

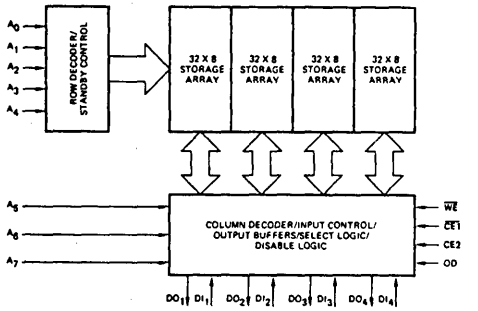
The Am9101/AM91L01 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L01 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are fully static and no refresh operations, sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

## BLOCK DIAGRAM



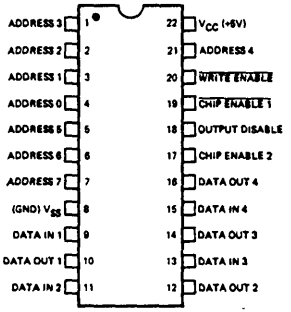

BD000100

## PRODUCT SELECTOR GUIDE

| Part Number | Am2101 | Am2101-2 | Am9101A<br>Am91L01A<br>Am2101-1 | Am9101B<br>Am91L01B | Am9101C<br>Am91L01C | Am9101D |
|---|---|---|---|---|---|---|
| Access Time | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |

03255C

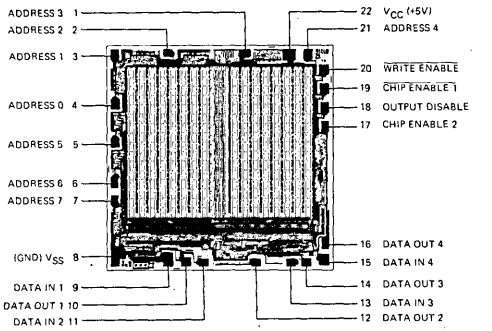
## CONNECTION DIAGRAM
### Top View




CD000150

Note: Pin 1 is marked for orientation

## Metallization and Pad Layout




DIE SIZE 0.132" x 0.131"

## ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Times | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |
| 0 to +70°C | Molded DIP | Standard | P2101 | P2101-2 | P2101-1<br>AM9101APC | AM9101BPC | AM9101CPC | AM9101DPC |
| | | Low | | | AM91L01APC | AM91L01BPC | AM91L01CPC | |
| | Hermetic DIP | Standard | C2101 | C2101-2 | C2101-1<br>AM9101ADC | AM9101BDC | AM9101CDC | AM9101DDC |
| | | Low | | | AM91L01ADC | AM91L01BDC | AM91L01CDC | |
| −55 to +125°C | Hermetic DIP | Standard | | | AM9101ADM | AM9101BDM | AM9101CDM | |
| | | Low | | | AM91L01ADM | AM91L01BDM | AM91L01CDM | |

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

**$\overline{CE1}$, CE2** Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ is low and CE2 is high.

**$\overline{WE}$** Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

**$t_{OD}$** Output enable time. Delay time from falling edge of OD to output on.

**$t_{RC}$** Read Cycle Time. The minimum time required between successive address changes while reading.

**$t_A$** Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

**$t_{CO}$** Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

**$t_{OH}$** Minimum time which will elapse between change of address and any change of the data output.

**$t_{DF1}$** Time delay between output disable HIGH and output data float.

**$t_{DF2}$** Time delay between chip enable OFF and output data float.

**$t_{WC}$** Write Cycle Time. The minimum time required between successive address changes while writing.

**$t_{AW}$** Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

**$t_{WP}$** The minimum duration of a LOW level on the write enable guaranteed to write data.

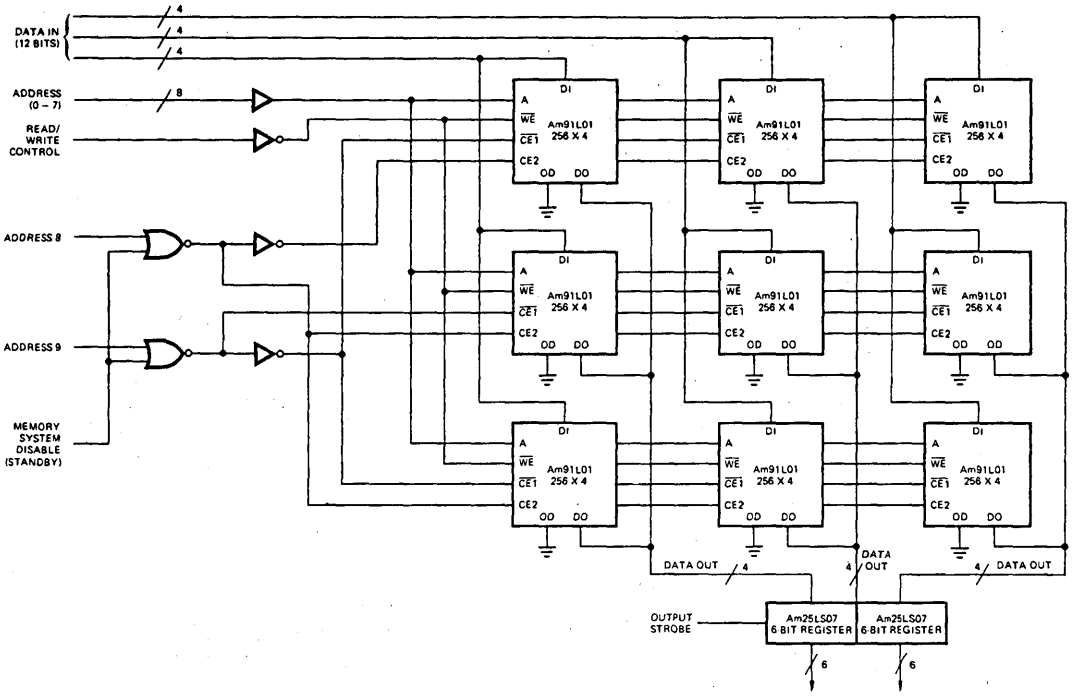
**$t_{WR}$** Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

**$t_{DW}$** Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

**$t_{DH}$** Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

**$t_{CW}$** Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

## APPLICATIONS




AF000090

EMORY SYSTEM 768 WORDS BY 12 BITS PER WORD

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +7.0V
DC Layout Voltage ..... −0.5V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 20mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Am9101/ Am91L01 Min | Am9101/ Am91L01 Max | Am2101 Min | Am2101 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min | $I_{OH}$ = −200μA | | 2.4 | | | | V |
| | | | $I_{OH}$ = −150μA | | | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min | $I_{OL}$ = 3.2mA | | | 0.4 | | | V |
| | | | $I_{OL}$ = 2.0mA | | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | −0.5 | 0.65 | V |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = Max, 0 ≤ $V_{IN}$ ≤ 5.25V | | | | 10 | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{\overline{CE}}$ = $V_{IH}$ | $V_O$ = $V_{CC}$ | C devices | | 5.0 | | 15 | μA |
| | | | | M devices | | 10 | | | |
| | | | $V_O$ = 0.4V | | | −10 | | −50 | |
| $I_{CC_1}$ | Power Supply Center | Data Out Open $V_{CC}$ = Max $V_{IN}$ = $V_{CC}$ | $T_A$ = 25°C | Am9101A/B | | 50 | | | mA |
| | | | | Am9101/C/D/E | | 55 | | | |
| | | | | Am91L01A/B | | 31 | | | |
| | | | | Am91L01C/D/E | | 34 | | | |
| | | | | Am2101 | | | | 60 | |
| | | | $T_A$ = 0°C (C devices only) | Am9101A/B | | 55 | | | |
| | | | | Am9101C/D/E | | 60 | | | |
| | | | | Am91L01A/B | | 33 | | | |
| | | | | Am91L01C/D/E | | 36 | | | |
| | | | | Am2101 | | | | 70 | |
| | | | $T_A$ = −55°C (M devices only) | Am9101A/B | | 60 | | | |
| | | | | Am9101C/D/E | | 65 | | | |
| | | | | Am91L01A/B | | 37 | | | |
| | | | | Am91L01C/D/E | | 40 | | | |
| | | | | Am2101 | | | | | |
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1MHz, $V_{IN}$ = 0V | | | | 6 | | 8 | pF |
| $C_O$ | Output Capacitance | $T_A$ = 25°C, f = 1MHz, $V_O$ = 0V | | | | 9 | | 12 | |

## DC CHARACTERISTICS (Cont.)

### STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

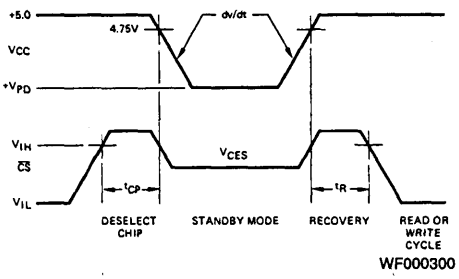
| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A$ = 0°C, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L01 | | 11 | 25 | mA |
| | | | | Am9101 | | 13 | 31 | |
| | | | $V_{PD}$ = 2.0V | Am91L01 | | 13 | 31 | |
| | | | | Am9101 | | 17 | 41 | |
| | | $T_A$ = −55°C, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L01 | | 11 | 28 | mA |
| | | | | Am9101 | | 13 | 34 | |
| | | | $V_{PD}$ = 2.0V | Am91L01 | | 13 | 34 | |
| | | | | Am9101 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/μs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |

#### POWER DOWN STANDBY OPERATION

The Am9101/AM91L01 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5 – 2.0 volts (see table and graph). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

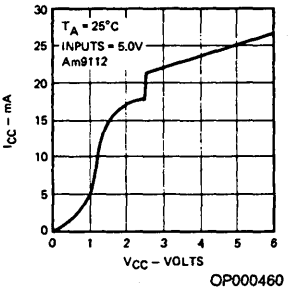
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

## DC OPERATING CHARACTERISTICS



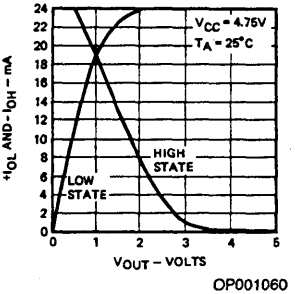

WF000300

**Typical Power Supply Current Versus Voltage**




OP000460

**Typical Output Current Versus Voltage**



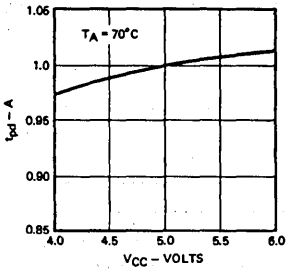

OP001060



03255C

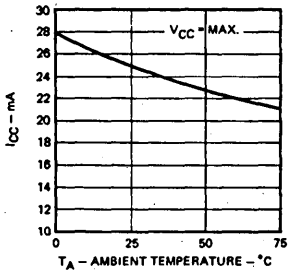
## DC OPERATING CHARACTERISTICS (Cont.)

**Access Time Versus $V_{CC}$ Normalized to $V_{CC} = +5.0$ Volts**



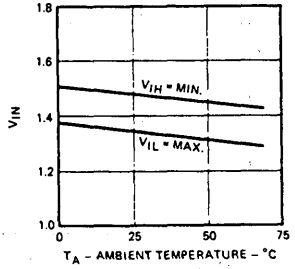

OP000100

**Typical Power Supply Current Versus Ambient Temperature**



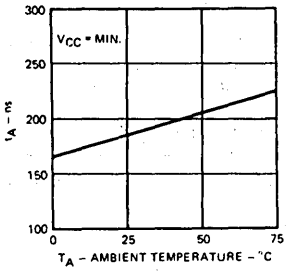

OP001070

**Typical $V_{IN}$ Limits Versus Ambient Temperature**



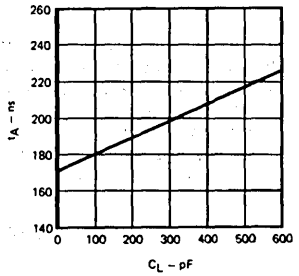

OP001030

**Typical $t_A$ Versus Ambient Temperature**




OP001040

**Typical $t_A$ Versus $C_L$**




OP001050

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

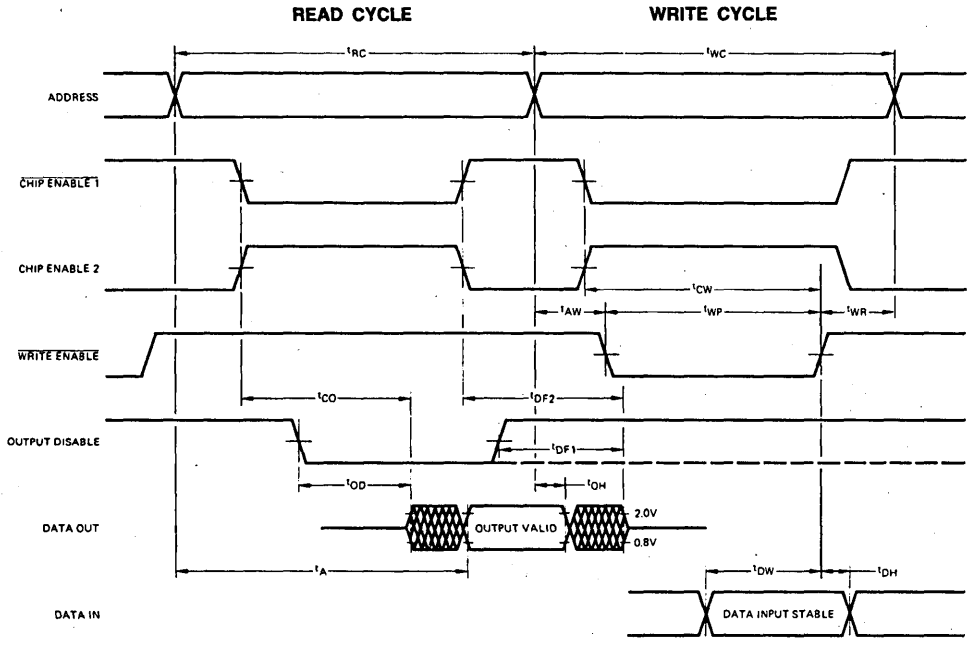
| No. | Symbol | Description | Am2101 Min | Am2101 Max | Am2101-2 Min | Am2101-2 Max | Am2101-1 Min | Am2101-1 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{RC}$ | Read Cycle Time | 1000 | | 650 | | 500 | | ns |
| 2 | $t_A$ | Access Time | | 1000 | | 650 | | 500 | ns |
| 3 | $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 800 | | 400 | | 350 | ns |
| 4 | $t_{OD}$ | Output Disable to Output ON Delay | | 700 | | 350 | | 300 | ns |
| 5 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 0 | | 0 | | 0 | | ns |
| 6 | $t_{DF1}$ | Output Disable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | ns |
| 7 | $t_{DF2}$ | Chip Enable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | ns |
| 8 | $t_{WC}$ | Write Cycle Time | 1000 | | 650 | | 500 | | ns |
| 9 | $t_{AW}$ | Address Set-up Time | 150 | | 150 | | 100 | | ns |
| 10 | $t_{WP}$ | Write Pulse Width | 750 | | 400 | | 300 | | ns |
| 11 | $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 900 | | 550 | | 400 | | ns |
| 12 | $t_{WR}$ | Address Hold Time | 50 | | 50 | | 50 | | ns |
| 13 | $t_{DW}$ | Input Data Set-up Time | 700 | | 400 | | 280 | | ns |
| 14 | $t_{DH}$ | Input Data Hold Time | 100 | | 100 | | 100 | | ns |

Note: 1. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

| No. | Symbol | Description | Am9101A Am91L01A Min | Am9101A Am91L01A Max | Am9101B Am91L01B Min | Am9101B Am91L01B Max | Am9101C Am91L01C Min | Am9101C Am91L01C Max | Am9101D Min | Am9101D Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{RC}$ | Read Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| 2 | $t_A$ | Access Time | | 500 | | 400 | | 300 | | 250 | ns |
| 3 | $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 200 | | 175 | | 150 | | 125 | ns |
| 4 | $t_{OD}$ | Output Disable to Output ON Delay | | 175 | | 150 | | 125 | | 100 | ns |
| 5 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 40 | | 40 | | 40 | | 30 | | ns |
| 6 | $t_{DF1}$ | Output Disable to Output OFF Delay | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | ns |
| 7 | $t_{DF2}$ | Chip Enable to Output OFF Delay | 10 | 125 | 10 | 125 | 10 | 100 | 10 | 100 | ns |
| 8 | $t_{WC}$ | Write Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| 9 | $t_{AW}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| 10 | $t_{WP}$ | Write Pulse Width | 175 | | 150 | | 125 | | 100 | | ns |
| 11 | $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 175 | | 150 | | 125 | | 100 | | ns |
| 12 | $t_{WR}$ | Address Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{DW}$ | Input Data Set-up Time | 150 | | 125 | | 100 | | 85 | | ns |
| 14 | $t_{DH}$ | Input Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |

Note: 1. Both $\overline{CE1}$ and CE2 must be true to enable the chip.

## SWITCHING WAVEFORMS




WF000200

# Am9111 Family

256 x 4 Static RAM

## DISTINCTIVE CHARACTERISTICS

- Low operating power dissipation
  125mW typ; 290mW maximum — standard power
  100mW typ; 175mW maximum — low power
- DC standby mode reduces power up to 84%
- High noise immunity — full 400mV
- Uniform switching characteristics — access times insensitive to supply variations, addressing patterns and data patterns
- Output disable control
- Zero address setup and hold times for simplified timing

## GENERAL DESCRIPTION

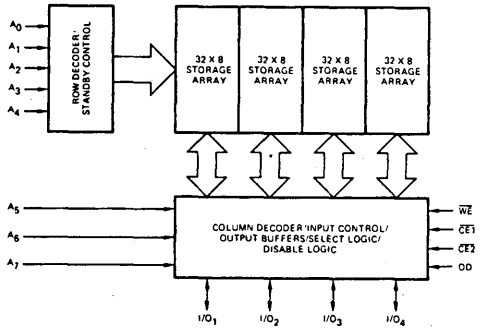
The Am9111/Am91L11 series of devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 200ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth. The input data and output data signals are bussed together to share common I/O pins. This feature not only decreases the package size, but also helps eliminate external logic in bus-oriented memory systems

These memories may be operated in a DC standby mode for reductions of as much as 84% of the normal power dissipation. Data can be retained with a power supply as low as 1.5 volts. The low power Am91L11 series offer reduced power dissipation during normal operating conditions and even lower dissipation in the standby mode.

The Chip Enable input control signals act as high order address lines and they control the write amplifier and the output buffers. The Output Disable signal provides independent control over the output state of enabled chips.

These devices are fully static and no refresh operations, sense amplifiers or clocks are required. Input and output signal levels are identical to TTL specifications, providing simplified interfacing and high noise immunity. The outputs will drive two full TTL loads for increased fan-out and better bus interfacing capability.

## BLOCK DIAGRAM



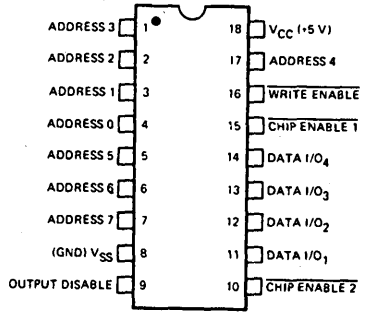

BD000220

## PRODUCT SELECTOR GUIDE

| Part Number | Am2111 | Am2111-2 | Am9111A<br>Am91L11A<br>Am2111-1 | Am9111B<br>Am91L11B | Am9111C<br>Am91L11C | Am9111D |
|---|---|---|---|---|---|---|
| Access Time | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |

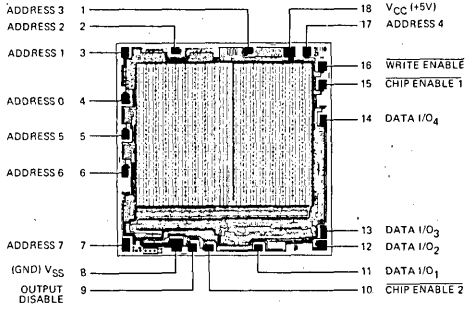
03256C

## CONNECTION DIAGRAM
### Top View




CD000320

## Metallization and Pad Layout




DIE SIZE: 0.132" x 0.131"

## ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Times | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |
| 0 to +70°C | Molded DIP | Standard | P2111 | P2111-2 | P2111-1<br>AM9111APC | AM9111-BPC | AM9111CPC | AM111DPC |
| | | Low | | | AM91L11APC | AM91L11BPC | AM91L11CPC | |
| | Hermetic DIP | Standard | C2111 | C2111-2 | C2111-1<br>AM9111ADC | AM9111BDC | AM9111CDC | AM9111DDC |
| | | Low | | | AM91L11ADC | AM91L11BDC | AM91L11CDC | |
| −55 to +125°C | Hermetic DIP | Standard | | | AM9111ADM | AM9111BDM | AM9111CDM | |
| | | Low | | | AM91L11ADM | AM91L11BDM | AM91L11CDM | |

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

$\overline{CE1}$, $\overline{CE2}$ Chip Enable Signals. Read and Write cycles can be executed only when both $\overline{CE1}$ and $\overline{CE2}$ are LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

$t_{OD}$ Output enable time. Delay time from falling edge of OD to output on.

$t_{RC}$ Read Cycle Time. The minimum time required between successive address changes while reading.

$t_A$ Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

$t_{CO}$ Access Time from Chip Enable. The minimum time during which the chip enable must be LOW prior to reading data on the output.

$t_{OH}$ Minimum time which will elapse between change of address and any change of the data output.

$t_{DF1}$ Time delay between output disable HIGH and output data float.

$t_{DF2}$ Time delay between chip enable OFF and output data float.

$t_{WC}$ Write Cycle Time. The minimum time required between successive address changes while writing.

$t_{AW}$ Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

$t_{WP}$ The minimum duration of a LOW level on the write enable guaranteed to write data.

$t_{WR}$ Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

$t_{DW}$ Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

$t_{DH}$ Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

$t_{CW}$ Chip Enable Time during Write. The minimum duration of a LOW level on the Chip Select prior to the rising edge of $\overline{WE}$ to guarantee writing.

## APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9111 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

This bussed I/O approach cuts down the package pin count allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9111 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

The Output Disable control signal is provided to prevent signal contention for the bus lines, and to simplify tri-state bus control in the external circuitry. If the chip is enabled and the output is enabled and the memory is in the Read state, then the output buffers will be impressing data on the bus lines. At that point, if the external system tries to drive the bus with data, in preparation for a write operation, there will be conflict for domination of the bus lines. The Output Disable signal allows the user direct control over the output buffers, independent of the state of the memory. Although there are alternative ways to resolve the conflict, normally Output Disable will be held high during a write operation.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +7.0V
DC Layout Voltage ..... −0.5V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 20mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | Am9111/ Am91L11 Min | Am9111/ Am91L11 Max | Am2111 Min | Am2111 Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min | $I_{OH}$ = −200μA | | 2.4 | | | | V |
| | | | $I_{OH}$ = −150μA | | | | 2.2 | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min | $I_{OL}$ = 3.2mA | | | 0.4 | | | V |
| | | | $I_{OL}$ = 2.0mA | | | | | 0.45 | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | −0.5 | 0.65 | V |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = Max, 0 ≤ $V_{IN}$ ≤ 5.25V | | | | 10 | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $\overline{CE}$ = $V_{IH}$ | $V_O$ = $V_{CC}$ | C devices | | 5.0 | | 15 | μA |
| | | | | M devices | | 10 | | | |
| | | | $V_O$ = 0.4V | | | −10 | | −50 | |
| $I_{CC1}$ | Power Supply Center | Data Out Open $V_{CC}$ = Max $V_{IN}$ = $V_{CC}$ | $T_A$ = 25°C | Am9111A/B | | 50 | | | mA |
| | | | | Am9101C/D/E | | 55 | | | |
| | | | | Am91L01A/B | | 31 | | | |
| | | | | Am91L11C/D/E | | 34 | | | |
| | | | | Am2111 | | | | 60 | |
| | | | $T_A$ = 0°C (C devices only) | Am9101A/B | | 55 | | | |
| | | | | Am9101C/D/E | | 60 | | | |
| | | | | Am91L11A/B | | 33 | | | |
| | | | | Am91L11C/D/E | | 36 | | | |
| | | | | Am2111 | | | | 70 | |
| | | | $T_A$ = −55°C (M devices only) | Am9111A/B | | 60 | | | |
| | | | | Am9111C/D/E | | 65 | | | |
| | | | | Am91L01A/B | | 37 | | | |
| | | | | Am91L01C/D/E | | 40 | | | |
| | | | | Am2111 | | | | | |
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1MHz, $V_{IN}$ = 0V | | | | 6 | | 8 | pF |
| $C_O$ | Output Capacitance | $T_A$ = 25°C, f = 1MHz, $V_O$ = 0V | | | | 11 | | 15 | |

## DC CHARACTERISTICS (Cont.)

### STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

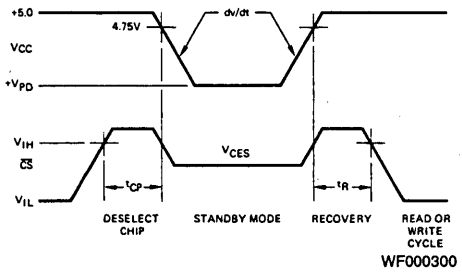
| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A$ = 0°C, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L11 | | 11 | 25 | mA |
| | | | | Am9111 | | 13 | 31 | |
| | | | $V_{PD}$ = 2.0V | Am91L11 | | 13 | 31 | |
| | | | | Am9111 | | 17 | 41 | |
| | | $T_A$ = −55°C, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L11 | | 11 | 28 | mA |
| | | | | Am9111 | | 13 | 34 | |
| | | | $V_{PD}$ = 2.0V | Am91L11 | | 13 | 34 | |
| | | | | Am9111 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/μs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |

#### POWER DOWN STANDBY OPERATION

The Am9111/Am91L11 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5–2.0 volts (see table and graph below). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

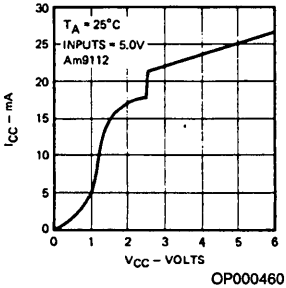
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

## DC OPERATING CHARACTERISTICS



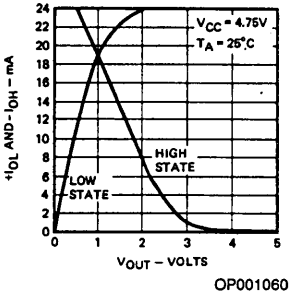
WF000300

**Typical Power Supply Current Versus Voltage**



OP000460

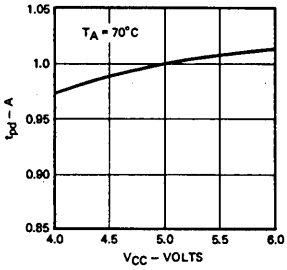
**Typical Output Current Versus Voltage**



OP001060

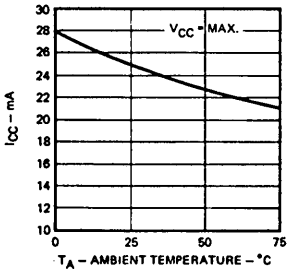
## DC OPERATING CHARACTERISTICS (Cont.)

**Access Time Versus $V_{CC}$ Normalized to $V_{CC} = +5.0$ Volts**



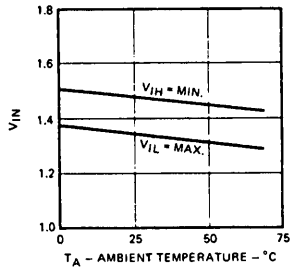

OP000100

**Typical Power Supply Current Versus Ambient Temperature**



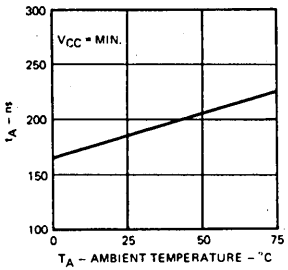

OP001070

**Typical $V_{IN}$ Limits Versus Ambient Temperature**



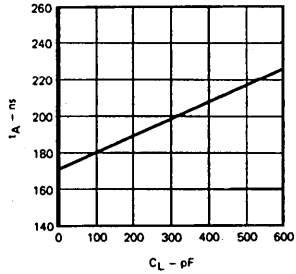

OP001030

**Typical $t_A$ Versus Ambient Temperature**




OP001040

**Typical $t_A$ Versus $C_L$**




OP001050

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

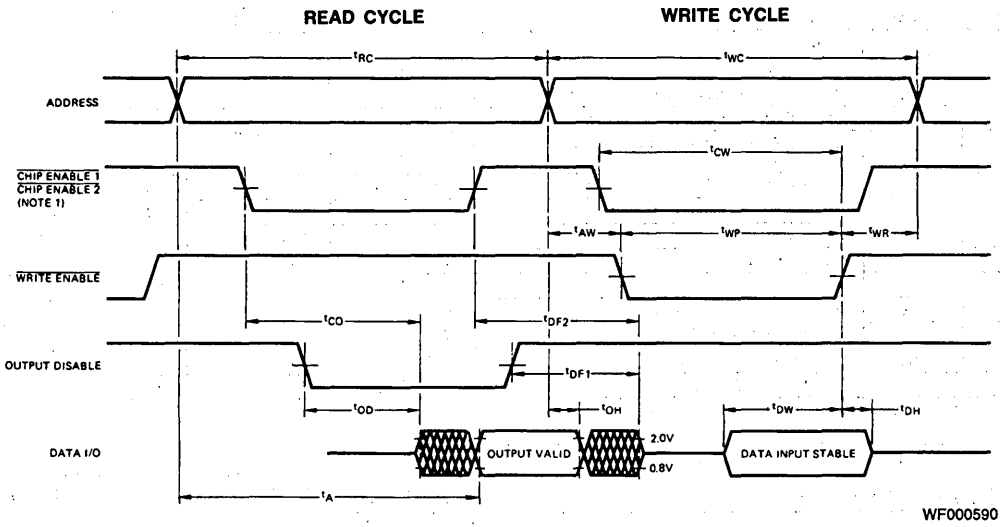
| No. | Symbol | Description | Am2111 | | Am2111-2 | | Am2111-1 | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{RC}$ | Read Cycle Time | 1000 | | 650 | | 500 | ns | |
| 2 | $t_A$ | Access Time | | 1000 | | 650 | | 500 | ns |
| 3 | $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 800 | | 400 | | 350 | ns |
| 4 | $t_{OD}$ | Output Disable to Output ON Delay | | 700 | | 350 | | 300 | ns |
| 5 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 0 | | 0 | | 0 | | ns |
| 6 | $t_{DF1}$ | Output Disable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | ns |
| 7 | $t_{DF2}$ | Chip Enable to Output OFF Delay | 0 | 200 | 0 | 150 | 0 | 150 | ns |
| 8 | $t_{WC}$ | Write Cycle Time | 1000 | | 650 | | 500 | | ns |
| 9 | $t_{AW}$ | Address Set-up Time | 150 | | 150 | | 100 | | ns |
| 10 | $t_{WP}$ | Write Pulse Width | 750 | | 400 | | 300 | | ns |
| 11 | $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 900 | | 550 | | 400 | | ns |
| 12 | $t_{WR}$ | Address Hold Time | 50 | | 50 | | 50 | | ns |
| 13 | $t_{DW}$ | Input Data Set-up Time | 700 | | 400 | | 280 | | ns |
| 14 | $t_{DH}$ | Input Data Hold Time | 100 | | 100 | | 100 | | ns |

Note: 1. Both $\overline{CE1}$ and $\overline{CE2}$ must be LOW to enable the chip.

| No. | Symbol | Description | Am9111A Am91L11A | | Am9111B Am91L11B | | Am9111C Am91L11C | | Am9111D | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{RC}$ | Read Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| 2 | $t_A$ | Access Time | | 500 | | 400 | | 300 | | 250 | ns |
| 3 | $t_{CO}$ | Chip Enable to Output ON Delay (Note 1) | | 200 | | 175 | | 150 | | 125 | ns |
| 4 | $t_{OD}$ | Output Disable to Output ON Delay | | 175 | | 150 | | 125 | | 100 | ns |
| 5 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 40 | | 40 | | 40 | | 30 | | ns |
| 6 | $t_{DF1}$ | Output Disable to Output OFF Delay | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | ns |
| 7 | $t_{DF2}$ | Chip Enable to Output OFF Delay | 10 | 150 | 10 | 125 | 10 | 125 | 10 | 100 | ns |
| 8 | $t_{WC}$ | Write Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| 9 | $t_{AW}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| 10 | $t_{WP}$ | Write Pulse Width | 175 | | 150 | | 125 | | 100 | | ns |
| 11 | $t_{CW}$ | Chip Enable Set-up Time (Note 1) | 175 | | 150 | | 125 | | 100 | | ns |
| 12 | $t_{WR}$ | Address Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{DW}$ | Input Data Set-up Time | 150 | | 125 | | 100 | | 85 | | ns |
| 14 | $t_{DH}$ | Input Data Hold Time | 0 | | 0 | | 0 | | 0 | | ns |

Note: 1. Both $\overline{CE1}$ and $\overline{CE2}$ must be LOW to enable the chip.

## SWITCHING WAVEFORMS



# Am9112

256 x 4 Static RAM

## DISTINCTIVE CHARACTERISTICS

- Low operating power dissipation
  125mW typ; 290mW maximum — standard power
  100mW typ; 175mW maximum — low power
- High noise immunity — full 400mV
- Uniform switching characteristics — access times insensitive to supply variations, address patterns and data patterns
- Bus-oriented I/O data
- Zero address, setup and hold times guaranteed for simpler timing
- Direct plug-in replacement for 2112 type devices

## GENERAL DESCRIPTION

The Am9112/Am91L12 series of products are high performance, low power, 1024-bit, static read/write random access memories. They offer a range of speeds and power dissipations including versions as fast as 200ns and as low as 100mW typical.

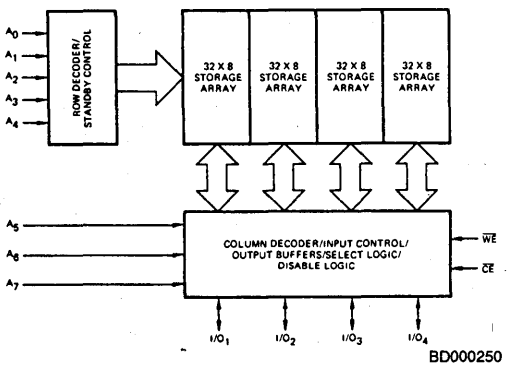
Each memory is implemented as 256 words by 4-bits per word. This organization allows efficient design of small memory systems and permits finer resolution of incremental memory word size relative to 1024 by 1 devices. The output and input data signals are internally bussed together and share 4 common I/O pins. This feature keeps the package size small and provides a simplified interface to bus-oriented systems.

The Am9112/Am91L12 memories may be operated in a DC standby mode for reductions of as much as 84% of the normal operating power dissipation. Thought the memory cannot be operated, data can be retained in the storage cells with a power supply as low as 1.5 volts. The Am91L12 versions offer reduced power during normal operating conditions as well as even lower dissipation in standby mode.

The eight Address inputs are decoded to select 1-of-256 locations within the memory. The Chip Enable input acts as a high-order address in multiple chip systems. It also controls the write amplifier and the output buffers in conjunction with the Write Enable input. When $\overline{CE}$ is low and $\overline{WE}$ is high, the write amplifiers are disabled, the output buffers are enabled and the memory will execute a read cycle. When $\overline{CE}$ is low and $\overline{WE}$ is low, the write amplifiers are enabled, the output buffers are disabled and the memory will execute a write cycle. When $\overline{CE}$ is high both the write amplifiers and the output buffers are disabled.

These memories are fully static and require no refresh operations or sense amplifiers or clocks. All input and output voltage levels are identical to standard TTL specifications, including the power supply.

## BLOCK DIAGRAM



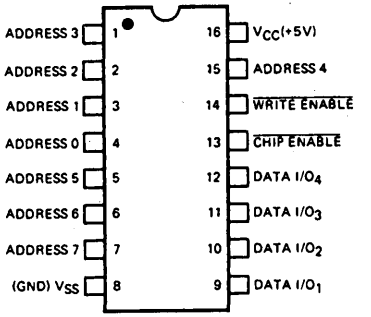

BD000250

## PRODUCT SELECTOR GUIDE

| Part Number | Am2112 | Am2112-2 | Am9112A Am91L12A | Am9112B Am91L12B | Am9112C Am91L12C | Am9112D |
|---|---|---|---|---|---|---|
| Access Time | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |

03257C

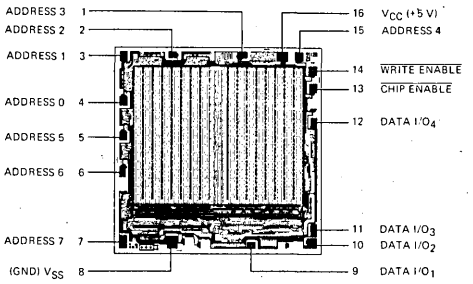
## CONNECTION DIAGRAM
## Top View




CD000340

Note: Pin 1 is marked for orientation

## Metallization and Pad Layout




DIE SIZE 0.132" x 0.131"

## ORDERING INFORMATION

| Ambient Temperature Specification | Package Type | Power Type | Access Times | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 1000ns | 650ns | 500ns | 400ns | 300ns | 250ns |
| 0 to +70°C | Molded DIP | Standard | P2112 | P2112-2 | AM9112APC | AM9112BPC | AM9112CPC | AM9112DPC |
| | | Low | | | AM91L12APC | AM91L12BPC | AM91L12CPC | |
| | Hermetic DIP | Standard | C2112 | C2112-2 | AM9112ADC | AM9112BDC | AM9112CDC | AM9112DDC |
| | | Low | | | AM91L12ADC | AM91L12BDC | AM91L12CDC | |
| −55 to +125°C | Hermetic DIP | Standard | | | AM9112ADM | AM9112BDM | AM9112CDM | |
| | | Low | | | AM91L12ADM | AM91L12BDM | AM91L12CDM | |

## DEFINITION OF TERMS

### FUNCTIONAL TERMS

$\overline{CE}$ Active LOW Chip Enable. Data can be read from or written into the memory only if $\overline{CE}$ is LOW.

$\overline{WE}$ Active LOW Write Enable. Data is written into the memory if $\overline{WE}$ is LOW and read from the memory if $\overline{WE}$ is HIGH.

**Static RAM** A random access memory in which data is stored in bistable latch circuits. A static memory will store data as long as power is supplied to the chip without requiring any special clocking or refreshing operations.

**N-Channel** An insulated gate field effect transistor technology in which the transistor source and drain are made of N-type material, and electrons serve as the carriers between the two regions. N-Channel transistors exhibit lower thresholds and faster switching speeds than P-Channel transistors.

### SWITCHING TERMS

$t_{RC}$ Read Cycle Time. The minimum time required between successive address changes while reading.

$t_A$ Access Time. The time delay between application of an address and stable data on the output when the chip is enabled.

$t_{CO}$ Output Enable Time. The time during which $\overline{CE}$ must be LOW and $\overline{WE}$ must be HIGH prior to data on the output.

$t_{OH}$ Minimum time which will elapse between change of address and any change of the data output.

$t_{DF}$ Time which will elapse between a change on the chip enable or the right enable and on data outputs being driven to a floating status.

$t_{WC}$ Write Cycle Time. The minimum time required between successive address changes while writing.

$t_{AW}$ Address Set-up Time. The minimum time prior to the falling edge of the write enable during which the address inputs must be correct and stable.

$t_{WP}$ The minimum duration of a LOW level on the write enable guaranteed to write data.

$t_{WR}$ Address Hold Time. The minimum time after the rising edge of the write enable during which the address must remain steady.

$t_{DW}$ Data Set-up Time. The minimum time that the data input must be steady prior to the rising edge of the write enable.

$t_{DH}$ Data Hold Time. The minimum time that the data input must remain steady after the rising edge of the write enable.

$t_{CW}$ Chip Enable Time During Write. The minimum duration of a LOW level on the Chip Select while the write enable is LOW to guarantee writing.

## APPLICATION INFORMATION

These memory products provide all of the advantages of AMD's other static N-channel memory circuits: +5 only power supply, all TTL interface, no clocks, no sensing, no refreshing, military temperature range available, low power versions available, high speed, high output drive, etc. In addition, the Am9112 series features a 256 x 4 organization with common pins used for both Data In and Data Out signals.

This bussed I/O approach keeps the package pin count low allowing the design of higher density memory systems. It also provides a direct interface to bus-oriented systems, eliminating bussing logic that could otherwise be required. Most microprocessor systems, for example, transfer information on a bidirectional data bus. The Am9112 memories can connect directly to such a processor since the common I/O pins act as a bidirectional data bus.

If the chip is enabled ($\overline{CE}$ low) and the memory is in the Read state ($\overline{WE}$ high), the output buffers will be turned on and will be driving data on the I/O bus lines. If the external system tries to drive the bus with data, there may be contention for control of the data lines and large current surges can result. Since the condition can occur at the beginning of a write cycle, it is important that incoming data to be written not be entered until the output buffers have been turned off.

These operational suggestions for write cycles may be of some help for memory system designs:

1. For systems where $\overline{CE}$ is always low or is derived directly from addresses and so is low for the whole cycle, make sure $t_{WP}$ is at least $t_{DW}$ + $t_{DF}$ and delay the input data until $t_{DF}$ following the falling edge of $\overline{WE}$. With zero address set-up and hold times it will often be convenient to make $\overline{WE}$ a cycle-width level ($t_{WP} = t_{WC}$) so that the only subcycle timing required is the delay of the input data.

2. For systems where $\overline{CE}$ is high for at least $t_{DF}$ preceeding the falling edge of $\overline{WE}$, $t_{WP}$ may assume the minimum specified value. When $\overline{CE}$ is high for $t_{DF}$ before the start of the cycle, then no other subcycle timing is required and $\overline{WE}$ and data-in may be cycle-width levels.

3. Notice that because both $\overline{CE}$ and $\overline{WE}$ must be low to cause a write to take place, either signal can be used to determine the effective write pulse. Thus, $\overline{WE}$ could be a level with $\overline{CE}$ becoming the write timing signal. In such a case, the data set-up and hold times are specified with respect to the rising edge of $\overline{CE}$. The value of the data set-up time remains the same and the value of the data hold time should change to a minimum of 25ns.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +7.0V
DC Layout Voltage ..... −0.5V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 20mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | | C devices Min | C devices Max | M devices Min | M devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $I_{OH}$ = −200 µA | | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $I_{OL}$ = 3.2mA | | | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | $V_{CC}$ | 2.0 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | −0.5 | 0.8 | −0.5 | 0.8 | V |
| $I_{LI}$ | Input Load Current | $V_{CC}$ = Max, 0V ≤ $V_{IN}$ ≤ $V_{CC}$ Max | | | | 10 | | 10 | µA |
| $I_{IO}$ | I/O Leakage Current | $\overline{CE}$ = $V_{IH}$ | $V_O$ = $V_{CC}$ | | | 5 | | 10 | µA |
| | | | $V_O$ = 0.4V | | | −10 | | −10 | |
| $I_{CC}$ | Power Supply Current | Data Out Open, $V_{CC}$ = Max, $V_{IN}$ = $V_{CC}$ | $T_A$ = 25°C | 9112A/B | | 50 | | 50 | mA |
| | | | | 9112C/D/E | | 55 | | 55 | |
| | | | | 91L12A/B | | 31 | | 31 | |
| | | | | 91L12C/D/E | | 34 | | 34 | |
| | | | $T_A$ = 0°C | 9112A/B | | 55 | | | |
| | | | | 9112C/D/E | | 60 | | | |
| | | | | 91L12A/B | | 33 | | | |
| | | | | 91L12C/D/E | | 36 | | | |
| | | | $T_A$ = −55°C | 9112A/B | | | | 60 | |
| | | | | 9112C/D/E | | | | 65 | |
| | | | | 91L12A/B | | | | 37 | |
| | | | | 91L12C/D/E | | | | 40 | |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V, $T_A$ = 25°C, f = 1MHz | | | | 6 | | 6 | pF |
| $C_O$ | Output Capacitance | $V_O$ = 0V, $T_A$ = 25°C, f = 1MHz | | | | 11 | | 11 | |

## STANDBY OPERATING CONDITIONS OVER TEMPERATURE RANGE

| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{PD}$ | $V_{CC}$ in Standby Mode | | | | 1.5 | | | |
| $I_{PD}$ | $I_{CC}$ in Standby Mode | $T_A$ = 0°C, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L12 | | 11 | 25 | mA |
| | | | | Am9112 | | 13 | 31 | |
| | | | $V_{PD}$ = 2.0V | Am91L12 | | 13 | 31 | |
| | | | | Am9112 | | 17 | 41 | |
| | | $T_A$ = −55°C, All Inputs = $V_{PD}$ | $V_{PD}$ = 1.5V | Am91L12 | | 11 | 28 | mA |
| | | | | Am9112 | | 13 | 34 | |
| | | | $V_{PD}$ = 2.0V | Am91L12 | | 13 | 34 | |
| | | | | Am9112 | | 17 | 46 | |
| dv/dt | Rate of Change of $V_{CC}$ | | | | | | 1.0 | V/µs |
| $t_R$ | Standby Recovery Time | | | | $t_{RC}$ | | | ns |
| $t_{CP}$ | Chip Deselect Time | | | | 0 | | | ns |
| $V_{CES}$ | $\overline{CE}$ Bias in Standby | | | | $V_{PD}$ | | | Volts |

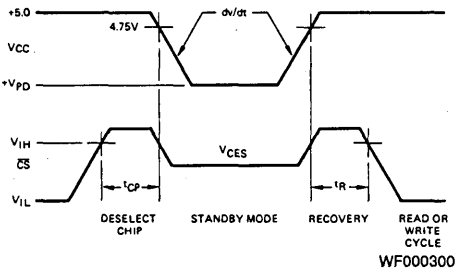
## DC CHARACTERISTICS (Cont.)

### POWER DOWN STANDBY OPERATION

The Am9112/Am91L12 Family is designed to maintain storage in a standby mode. The standby mode is entered by lowering $V_{CC}$ to around 1.5 – 2.0 volts (see table and graph). When the voltage to the device is reduced, the storage cells are isolated from the data lines, so their contents will not change. The standby mode may be used by a battery operated backup power supply system, or, in a large system, memory pages not being accessed can be placed in standby to save power. A standby recovery time must elapse following restoration of normal power before the memory may be accessed.

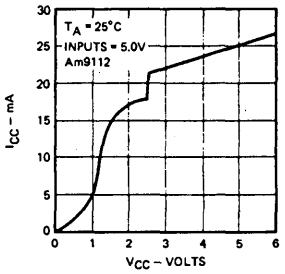
To ensure that the output of the device is in a high impedance OFF state during standby, the chip select should be held at $V_{IH}$ or $V_{CES}$ during the entire standby cycle.

## DC OPERATING CHARACTERISTICS



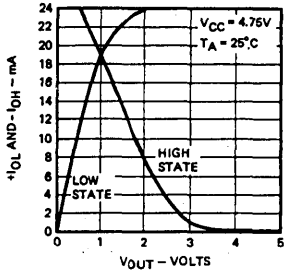
WF000300

**Typical Power Supply Current Versus Voltage**



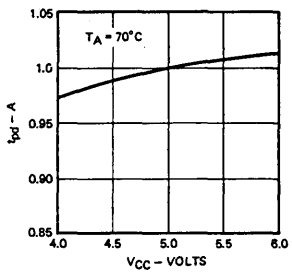
OP000460

**Typical Output Current Versus Voltage**



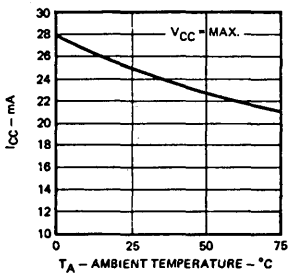
OP001060

**Access Time Versus $V_{CC}$ Normalized to $V_{CC}$ = +5.0 Volts**



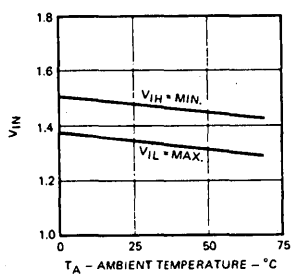
OP000100

**Typical Power Supply Current Versus Ambient Temperature**



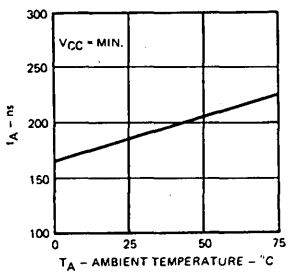
OP001070

**Typical $V_{IN}$ Limits Versus Ambient Temperature**



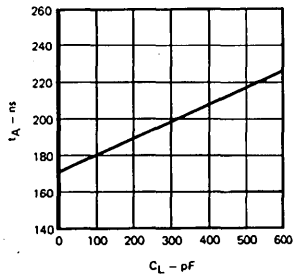
OP001030

**Typical $t_A$ Versus Ambient Temperature**



OP001040

**Typical $t_A$ Versus $C_L$**



OP001050

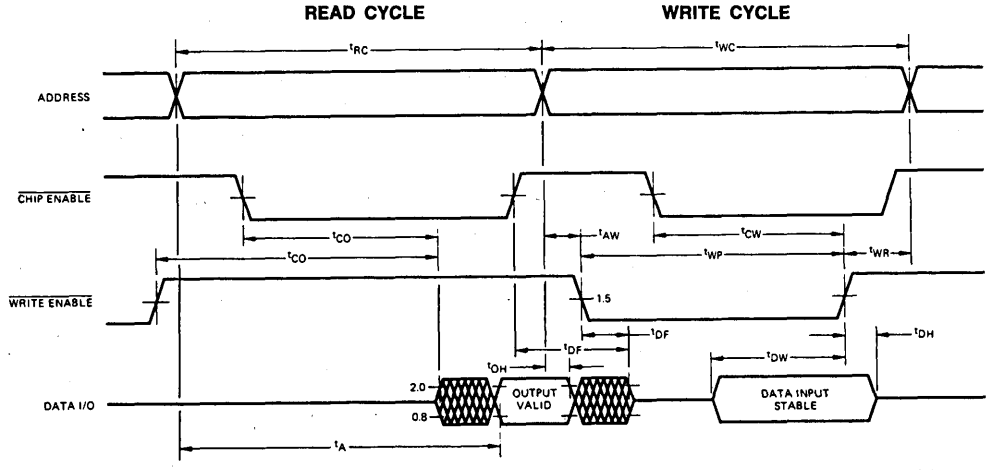
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am9112A Am91L12A Min | Am9112A Am91L12A Max | Am9112B Am91L12B Min | Am9112B Am91L12B Max | Am9112C Am91L12C Min | Am9112C Am91L12C Max | Am9112D Min | Am9112D Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{RC}$ | Read Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| 2 | $t_A$ | Access Time | | 500 | | 400 | | 300 | | 250 | ns |
| 3 | $t_{CO}$ | Output Enabled to Output ON Delay (Note 1) | 5.0 | 175 | 5.0 | 150 | 5.0 | 125 | 5.0 | 100 | ns |
| 4 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | 40 | | 40 | | 40 | | 30 | | ns |
| 5 | $t_{DF}$ | Output Disabled to Output OFF Delay (Note 2) | 5.0 | 125 | 5.0 | 100 | 5.0 | 100 | 5.0 | 75 | ns |
| 6 | $t_{WC}$ | Write Cycle Time | 500 | | 400 | | 300 | | 250 | | ns |
| 7 | $t_{AW}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | ns |
| 8 | $t_{WR}$ | Address Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| 9 | $t_{WP}$ | Write Pulse Width (Note 3) | 175 | | 150 | | 125 | | 100 | | ns |
| 10 | $t_{CW}$ | Chip Enable Set-up Time | 175 | | 150 | | 125 | | 100 | | ns |
| 11 | $t_{DW}$ | Input Data Set-up Time | 150 | | 125 | | 100 | | 85 | | ns |
| 12 | $t_{DH}$ | Input Data Hold Time (Note 4) | 0 | | 0 | | 0 | | 0 | | ns |

Notes:

1. Output is enabled and $t_{CO}$ commences only with both $\overline{CE}$ LOW and $\overline{WE}$ HIGH.
2. Output is disabled and $t_{DF}$ defined from either the rising edge of $\overline{CE}$ or the falling edge of $\overline{WE}$.
3. Minimum $t_{WP}$ is valid when $\overline{CE}$ has been HIGH at least $t_{DF}$ before $\overline{WE}$ goes LOW. Otherwise $t_{WP(min).} = t_{DW(min.)} + t_{DF(max.)}$.
4. When $\overline{WE}$ goes HIGH at the end of the write cycle, it will be possible to turn on the output buffers if $\overline{CE}$ is still LOW. The data out will be the same as the data just written and so will not conflict with input data that may still be on the I/O bus.

## SWITCHING WAVEFORMS (Note 5)




WF000610

5. See "Application Information" section of this specification.

# Am9114/24

1024 x 4 Static RAM

## DISTINCTIVE CHARACTERISTICS

- Low operating and standby power
- Access times down to 200ns
- Am9114 is a direct plug-in replacement for 2114
- Am9124 pin and function compatible with Am9114 and 2114, plus $\overline{CS}$ power down feature
- High output drive — 4.0mA sink current @ 0.4V — 9124
  3.2mA sink current @ 0.4V — 9114
- TTL identical input/output levels

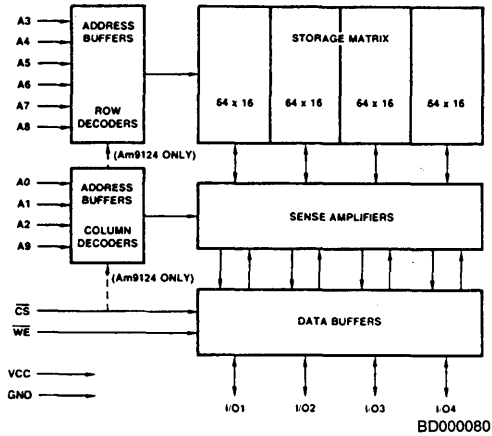
## GENERAL DESCRIPTION

The Am9114 and Am9124 are high performance, static, N-Channel, read/write, random access memories organized as 1024 x 4. Operation is from a single 5V supply, and all input/output levels are identical to standard TTL specifications. Low power versions of both devices are available with power savings of over 30%. The Am9114 and Am9124 are the same except that the Am9124 offers an automatic $\overline{CS}$ power down feature.

The Am9124 remains in a low power standby mode as long as $\overline{CS}$ remains high, thus reducing its power requirements. The Am9124 power decreases from 368mW to 158mW in the standby mode, and the Am91L24 from 262mW to 105mW. The $\overline{CS}$ input does not affect the power dissipation of the Am9114. (See Figure 1, page 4).

Data readout is not destructive and the same polarity as data input. $\overline{CS}$ provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 4.0mA for Am9124 and 3.2mA for Am9114 provides increased short circuit current for improved capacitive drive.

## BLOCK DIAGRAM

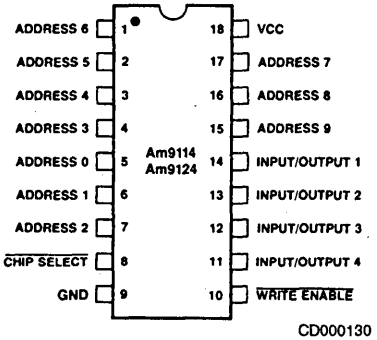



## PRODUCT SELECTOR GUIDE

| Access Times | 450ns | 300ns | 200ns |
|---|---|---|---|
| Standard Device | Am9114B<br>Am9124B | Am9114C<br>Am9124C | Am9114E |
| Low Power | Am91L14B<br>Am91L24B | Am91L14C<br>Am91L24C | Am91L14E |

01454D

## CONNECTION DIAGRAM
### Top View




CD000130

Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| $A_0$ | $A_9$ |
| $A_1$ | $A_8$ |
| $A_2$ | $A_7$ |
| $A_3$ | $A_0$ |
| $A_4$ | $A_1$ |
| $A_5$ | $A_2$ |
| $A_6$ | $A_3$ |
| $A_7$ | $A_4$ |
| $A_8$ | $A_5$ |
| $A_9$ | $A_6$ |

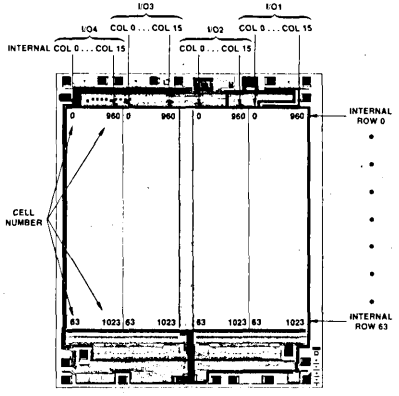



**Figure 2. Bit Mapping Information**

## ORDERING INFORMATION

**Am9114 E P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - D – 18-pin CERDIP
  - P – 18-pin plastic DIP
- E — Speed Select
  - B – 450ns
  - C – 300ns
  - E – 200ns
- Am9114 — Device Type
  - AM9114 – 1k x 4 SRAM
  - AM91L14 – Same, Low Power
  - AM9124 – 1k x 4 SRAM with power down feature
  - AM91L24 – Same, Low Power

| Valid Combinations | |
|---|---|
| B | PC, DC, DM |
| C | PC, DC, DM |
| E Am9114/ 91L14 only | PC, DC DM (9114 only) |

## Application Table

| | | Worst Case Current (mA at 0°C) | |
|---|---|---|---|
| **Configuration** | **Part Number** | **100% Duty Cycle** | **50% Duty Cycle** |
| 2K x 8 | 9114 | 280 | 280 |
| | 91L14 | 200 | 200 |
| | 9124 | 200 | 160 |
| | 91L24 | 140 | 110 |
| 4K x 12 | 9114 | 840 | 840 |
| | 91L14 | 600 | 600 |
| | 9124 | 480 | 420 |
| | 91L24 | 330 | 285 |
| 8K x 16 | 9114 | 2240 | 2240 |
| | 91L14 | 1600 | 1600 |
| | 9124 | 1120 | 1040 |
| | 91L24 | 760 | 700 |

Figure 1. Supply Current Advantage of Am9124.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
Signal Voltages with
respect to ground ..... −3.0V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 10mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

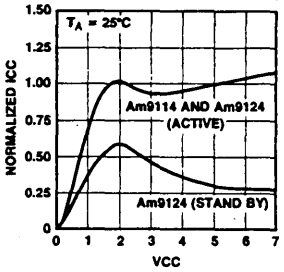
| Symbol | Parameter | Test Conditions | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output HIGH Current | $V_{CC}$ = +4.5V, $V_{OH}$ = 2.4V | 91(L)14 | | −1.0 | | | mA |
| | | | 91(L)24 | | −1.4 | | | |
| $I_{OL}$ | Output LOW Current | $V_{OL}$ = 0.4V | $T_A$ = 70°C | 91(L)14 | 3.2 | | | |
| | | | | 91(L)24 | 4.0 | | | |
| | | | $T_A$ = +125°C | 91(L)14 | 2.4 | | | |
| | | | | 91(L)24 | 3.2 | | | |
| $V_{IH}$ | Input HIGH Voltage | | | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | | −3.0 | | 0.8 | |
| $I_{IX}$ | Input Load Current | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | | | | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | $T_A$ = +70°C | | −10 | | 10 | |
| | | | $T_A$ = +125°C | | −50 | | 50 | |
| $I_{OS}$ | Output Short Circuit Current | Note 2 | 91(L)14C | | | | 75 | mA |
| | | | 91(L)24C | | | | 95 | |
| | | | 91(L)14M | | | | 75 | |
| | | | 91(L)24M | | | | 115 | |
| $C_{IN}$ | Input Capacitance | Note 1 | f = 1.0 MHz, $T_A$ = 25°C, All pins at 0V | | | 3 | 5 | pF |
| $C_{I/O}$ | I/O Capacitance | | | | | 5 | 6 | |
| $I_{CC}$ | Operating Supply Current | $V_{CC}$ = Max, $\overline{CS}$ ≤ $V_{IL}$ for 9124 | $T_A$ = 25°C | Standard devices | | 60 | | mA |
| | | | | L devices | | 40 | | |
| | | | $T_A$ = 0°C | Standard devices | | 70 | | |
| | | | | L devices | | 50 | | |
| | | | $T_A$ = −55°C | Standard devices | | 80 | | |
| | | | | L devices | | 60 | | |
| $I_{PD}$ | Automatic $\overline{CS}$ Power Down Current (9124/L24 only) | $V_{CC}$ = Max, $\overline{CS}$ ≥ $V_{IH}$ | $T_A$ = 25°C | 9124 | | 24 | | |
| | | | | 91L24 | | 15 | | |
| | | | $T_A$ = 0°C | 9124 | | | 30 | |
| | | | | 91L24 | | | 20 | |
| | | | $T_A$ = −55°C | 9124 | | | 33 | |
| | | | | 91L24 | | | 22 | |

Notes:

1. Typical values are for $T_A$ = 25°C, nominal supply voltage and nominal processing parameters.
2. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
3. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of one standard TTL gate plus 100pF.
4. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
5. Chip Select access time ($t_{CO}$) is longer for the Am9124 than for the Am9114. The specified address access time will be valid only when Chip Select is low soon enough for $t_{CO}$ to elapse.

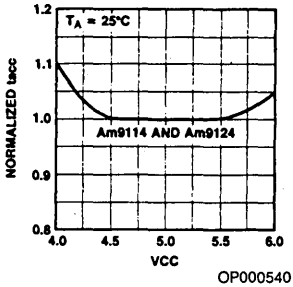
## DC OPERATING CHARACTERISTICS

### Typical $I_{CC}$ Versus $V_{CC}$ Characteristics



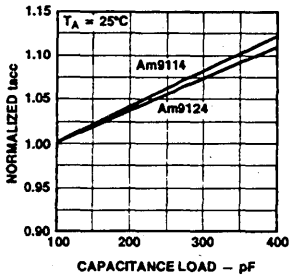

OP000530

### Typical $t_{acc}$ Versus $V_{CC}$ Characteristics



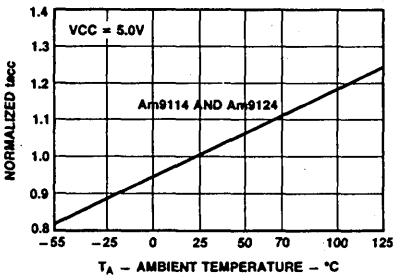

OP000540

### Typical C Load Versus Normalized $t_{acc}$ Characteristics



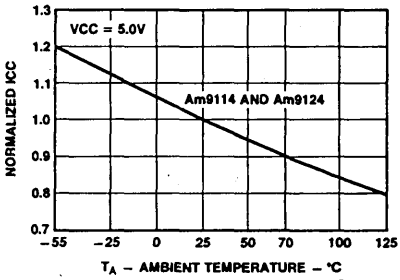

OP000550

### Normalized $t_{acc}$ Versus Ambient Temperature




OP000200

### Normalized $I_{CC}$ Versus Ambient Temperature

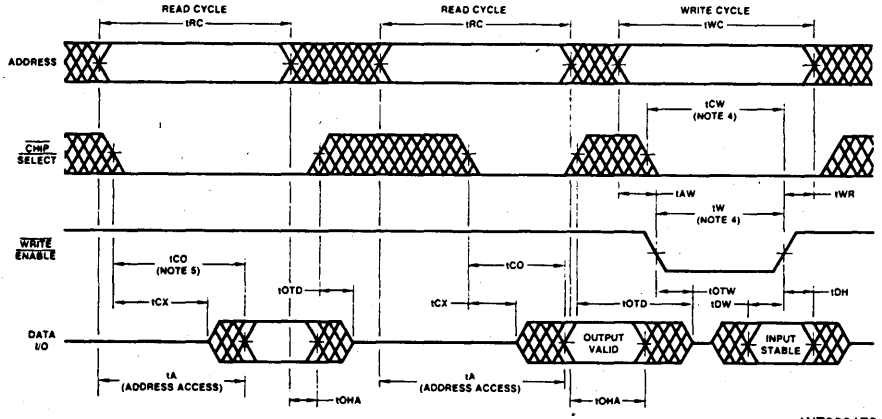



OP000210

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

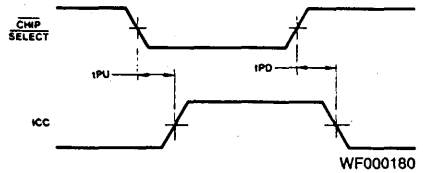
| No. | Symbol | Description | | B devices Min | B devices Max | C devices Min | C devices Max | E devices Min | E devices Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | |
| 1 | $t_{RC}$ | Address Valid to Address Do Not Care Time (Read Cycle Time) | | 450 | | 300 | | 200 | | ns |
| 2 | $t_A$ | Address Valid to Data Out Valid Delay (Address Access Time) | | | 450 | | 300 | | 200 | ns |
| 3 | $t_{CO}$ | Chip Select Low to Data Out Valid (Note 5) | Am9114 | | 120 | | 100 | | 70 | ns |
| | | | Am9124 | | 420 | | 280 | | NA | ns |
| 4 | $t_{CX}$ | Chip Select Low to Data Out On | | 10 | | 10 | | 10 | | ns |
| 5 | $t_{OTD}$ | Chip Select High to Data Out Off | | | 100 | | 80 | | 60 | ns |
| 6 | $t_{OHA}$ | Address Unknown to Data Out Unknown Time | | 50 | | 50 | | 50 | | ns |
| **Write Cycle** | | | | | | | | | | |
| 7 | $t_{WC}$ | Address Valid to Address Do Not Care Time (Write Cycle Time) | | 450 | | 300 | | 200 | | ns |
| 8 | $t_W$ | Write Enable Low to Write Enable High Time (Note 4) | Am9114 | 200 | | 150 | | 120 | | ns |
| | | | Am9124 | 250 | | 200 | | NA | | ns |
| 9 | $t_{WR}$ | Write Enable High to Address Do Not Care Time | | 0 | | 0 | | 0 | | ns |
| 10 | $t_{OTW}$ | Write Enable Low to Data Out Off Delay | | | 100 | | 80 | | 60 | ns |
| 11 | $t_{DW}$ | Data in Valid to Write Enable High Time | | 200 | | 150 | | 120 | | ns |
| 12 | $t_{DH}$ | Write Enable Low to Data In Do Not Care Time | | 0 | | 0 | 0 | 0 | | ns |
| 13 | $t_{AW}$ | Address Valid to Write Enable Low Time | | 0 | | 0 | | 0 | | ns |
| 14 | $t_{PD}$ | Chip Select High to Power Low Delay (Am9124 only) | | | 200 | | 150 | | 100 | ns |
| 15 | $t_{PU}$ | Chip Select Low to Power High Delay (Am9124 only) | | 0 | | 0 | | 0 | | ns |
| 16 | $t_{CW}$ | Chip Select Low to Write Enable High Time (Note 4) | Am9114 | 200 | | 150 | | 120 | | 90 |
| | | | Am9124 | 250 | | 200 | | NA | | ns |

## SWITCHING WAVEFORMS




WF000170

## POWER DOWN WAVEFORM (Am9124 ONLY)




WF000180

# Am9122

256 x 4 Static RAM

## DISTINCTIVE CHARACTERISTICS

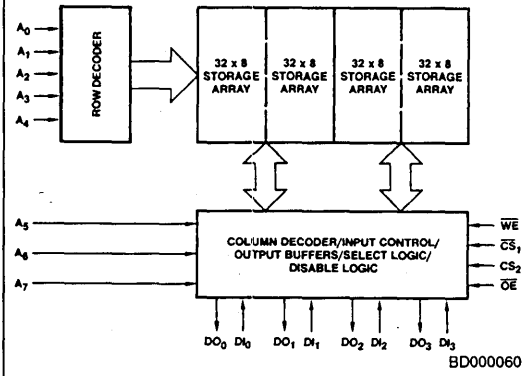
- High performance replacement for 93422/93L422
- Fast access times — as low as 25ns
- Low power dissipation
  - Low power: 248/440mW (Commercial)
    495mW (Military)
- Single 5 volt power supply — ±10% tolerance both commercial and military

## GENERAL DESCRIPTION

The Am9122/Am91L22 series is a MOS pin-for-pin and functional replacement for the 93422/93L422 bipolar memories. These devices are high-performance, low-power, 1024-bit, static, read/write random access memories. They offer a wide range of access times including versions as fast as 25ns. Each memory is implemented as 256 words by 4 bits per word. This organization permits efficient design of small memory systems and allows finer resolution of incremental memory depth.

The Am9122/91L22 employs an output enable and two chip enable inputs to give the user better data control. High noise immunity, high output drive (4 TTL loads) and TTL logic voltage levels allow easy conversion from bipolar to MOS. 10% power supply tolerances give better margins in the memory system. As with all AMD MOS RAMs, the Am9122/91L22 is guaranteed to 0.1% AQL.

## BLOCK DIAGRAM




BD000060

## MODE SELECT TABLE

| Inputs | | | | | Outputs | Mode |
|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CS_1}$ | $CS_2$ | $\overline{WE}$ | $D_0$–$D_3$ | | |
| X | H | X | X | X | High Z | Not Selected |
| X | X | L | X | X | High Z | Not Selected |
| L | L | H | H | X | $O_0$–$O_3$ | Read Stored Data |
| X | L | H | L | L | High Z | Write "0" |
| X | L | H | L | H | High Z | Write "1" |
| H | L | H | H | X | High Z | Output Disabled |
| H | L | H | L | L | High Z | Write "0" (Output Disabled) |
| H | L | H | L | H | High Z | Write "1" (Output Disabled) |

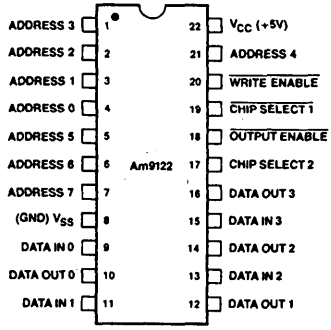
H = HIGH Voltage
L = LOW Voltage
X = Don't Care (HIGH or LOW)
High Z = High Impedance

## PRODUCT SELECTOR GUIDE

| Part Number | | Am9122-25 | Am9122-35 | Am91L22-35 | Am9122-45 | Am91L22-60 |
|---|---|---|---|---|---|---|
| Maximum Access Time (ns) | | 25 | 35 | 35 | 45 | 60 |
| Maximum Operating Current (mA) | 0° to 70°C | 120 | 120 | 80 | 80 | 45 |
| | −55° to 125°C | N/A | 135 | N/A | 90 | N/A |

01547C

## CONNECTION DIAGRAM
### Top View

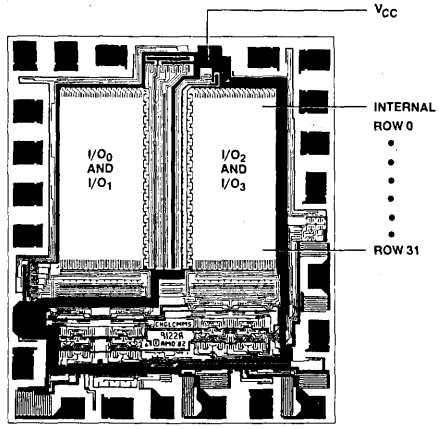



CD000110

Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| $A_0$ | $A_0$ |
| $A_1$ | $A_1$ |
| $A_2$ | $A_2$ |
| $A_3$ | $A_3$ |
| $A_4$ | $A_4$ |
| $A_5$ | $A_5$ |
| $A_6$ | $A_6$ |
| $A_7$ | $A_7$ |




## ORDERING INFORMATION

**Am9122-25 P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - P – 22-pin plastic DIP
  - D – 22-pin CERDIP
- 25 — Speed Select
  - 25 – 25ns
  - 35 – 35ns
  - 45 – 45ns
  - 60 – 60ns
- Am9122 — Device Type
  - AM9122 – 256 x 4 SRAM
  - AM91L22 – Same, Low Power

| Valid Combinations | |
|---|---|
| Am9122-25 (9122 only) | PC, DC |
| Am9122-35 | PC, DC<br>DM (9122 only) |
| Am9122-45 (91L22 only) | PC, DC, DM |
| Am9122-60 (91L22 only) | PC, DC |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 20mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

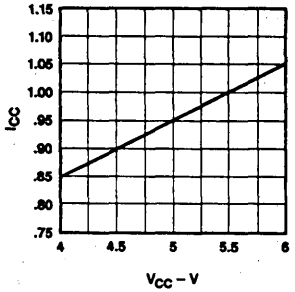
| Symbol | Parameter | Test Conditions | | Am91L22-60 | | | Am91L22-35 Am91L22-45 | | | Am9122-25 Am9122-35 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min | $I_{OH}$ = −5.2mA | 2.4 | | | 2.4 | | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min | $I_{OL}$ = 8.0mA | | | 0.4 | | | 0.4 | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.1 | | $V_{CC}$ | 2.1 | | $V_{CC}$ | 2.1 | | $V_{CC}$ | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −3.0 | | 0.8 | −3.0 | | 0.8 | −3.0 | | 0.8 | Volts |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max, $V_{IN}$ = Gnd | | | | 10 | | | 10 | | | 10 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max, $V_{IN}$ = $V_{CC}$ | | | | 10 | | | 10 | | | 10 | µA |
| $V_{CD}$ | Input Diode Clamp Voltage | | | | | Note 4 | | | Note 4 | | | Note 4 | Volts |
| $I_{OFF}$ | Output Current (High-Z) | $V_{OL} \leq V_{OUT} \leq V_{OH}$ Output Disabled | $T_A$ = Max | −50 | | 50 | −50 | | 50 | −50 | | 50 | µA |
| $I_{OS}$ | Output Short Circuit Current (Note 3) | $V_{CC}$ = Max $V_{OUT}$ = GND | Commercial | | | −70 | | | −70 | | | −70 | mA |
| | | | Military | | | −80 | | | −80 | | | −80 | |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max, $I_{OUT}$ = 0mA | $T_A$ = 70°C | | | 40 | | | 70 | | | 110 | mA |
| | | | $T_A$ = 0°C | | | 45 | | | 80 | | | 120 | |
| | | | $T_A$ = −55°C | | | N/A | | | 90 | | | 135 | |
| $C_{IN}$ | Input Capacitance $V_{IN}$ = 0V | $T_A$ = 25°C, f=1MHz $V_{CC}$ = 4.5v | | | 3 | 5 | | 3 | 5 | | 3 | 5 | pF |
| $C_{OUT}$ | Output Capacitance $V_{OUT}$ = 0V | | | | 5 | 8 | | 5 | 8 | | 5 | 8 | |

Notes:

1. The temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. A two minute warm up period is required for −55°C operation.
2. $T_W$ measured at $t_{WSA}$ = min; $t_{WSA}$ measured at $t_W$ = min.
3. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
4. The NMOS process does not provide a clamp diode. However, the Am9122/91L22 is insensitive to −3V DC input levels and −5V undershoot pulses of less than 10ns (measured at 50% point).
5. Test conditions assume signal transition times of 10ns or less, timing reference levels of 1.5V and output loading of the specified $I_{OL}/I_{OH}$ and 30pF load capacitance as in Figure 1a.
6. Transition is measured at $V_{OH}$ −500mV or $V_{OL}$ +500mV levels on the output from 1.5V level on the input with load shown in Figure 1b.

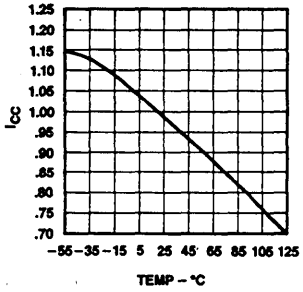
## DC OPERATING CHARACTERISTICS

**Normalized $I_{CC}$ versus Supply Voltage**



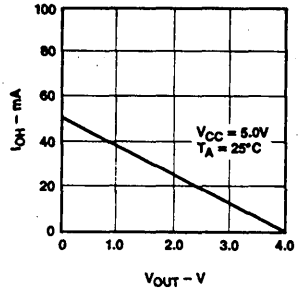

OP000120

**Normalized $I_{CC}$ versus Ambient Temperature**



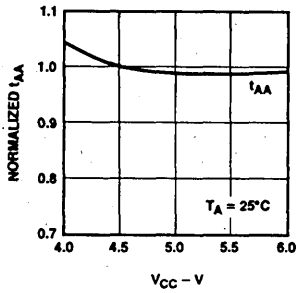

OP000130

**Output Source Current versus Output Voltage**



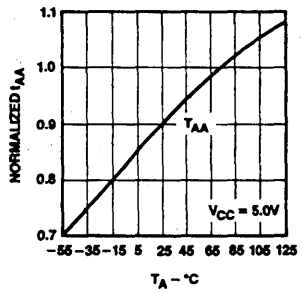

OP000140

**Normalized Access Time versus Supply Voltage**



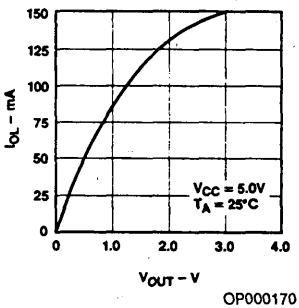

OP000150

**Normalized Access Time versus Ambient Temperature**



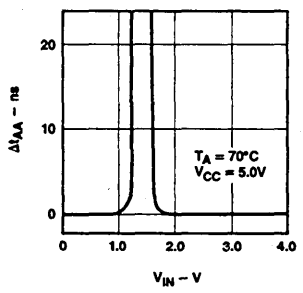

OP000160

**Output Sink Current versus Output Voltage**



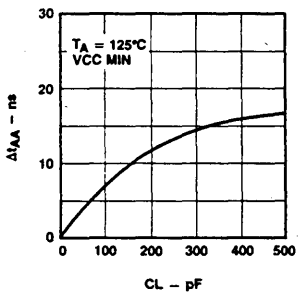

OP000170

**Access Time Change versus Input Voltage**




OP000180

**Access Time Change versus Output Loading**




OP000190

## SWITCHING TEST CIRCUITS

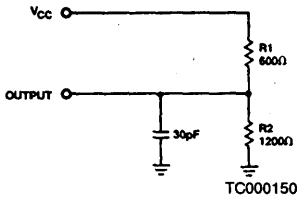



Figure 1a.

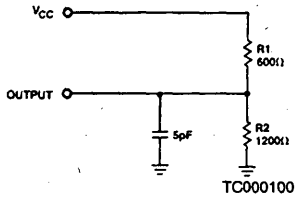



Figure 1b.

## SWITCHING TEST WAVEFORM

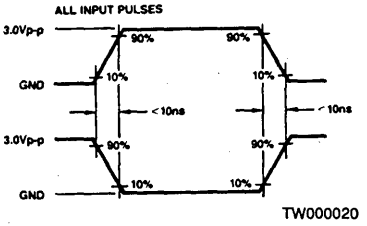


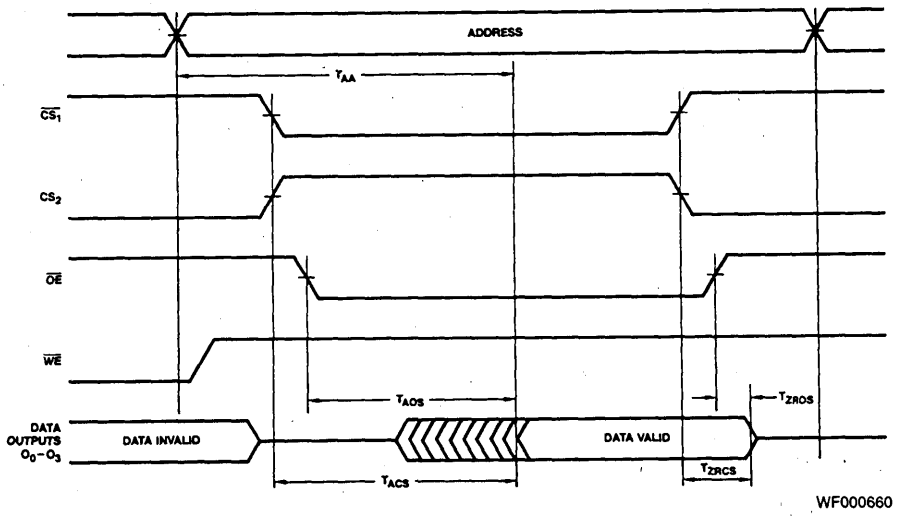

Figure 2.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified

| No. | Symbol | Description | Am9122-25 | | Am91L22-35 Am9122-35 | | Am91L22-45 | | Am91L22-60 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{ACS}$ | Chip Select Time | | 15 | | 25 | | 30 | | 35 | ns |
| 2 | $t_{ZRCS}$ | Chip Select to High-Z (Note 6) | | 20 | | 30 | | 30 | | 35 | ns |
| 3 | $t_{AOS}$ | Output Enable Time | | 15 | | 25 | | 30 | | 35 | ns |
| 4 | $t_{ZROS}$ | Output Enable to High-Z (Note 6) | | 20 | | 30 | | 30 | | 35 | ns |
| 5 | $t_{AA}$ | Address Access Time | | 25 | | 35 | | 45 | | 60 | ns |
| 6 | $t_{ZWS}$ | Write Disable to High-Z (Note 6) | | 20 | | 30 | | 35 | | 40 | ns |
| 7 | $t_{WR}$ | Write Recovery Time | | 20 | | 25 | | 40 | | 45 | ns |
| 8 | $t_W$ | Write Pulse Width (Note 2) | 15 | | 25 | | 30 | | 40 | | ns |
| 9 | $t_{WSD}$ | Data Setup Time Prior to Write | 5 | | 5 | | 5 | | 5 | | ns |
| 10 | $t_{WHD}$ | Data Hold Time After Write | 5 | | 5 | | 5 | | 5 | | ns |
| 11 | $t_{WSA}$ | Address Setup Time (Note 2) | 5 | | 5 | | 10 | | 10 | | ns |
| 12 | $t_{WHA}$ | Address Hold Time | 5 | | 5 | | 5 | | 5 | | ns |
| 13 | $t_{WSCS}$ | Chip Select Setup Time | 5 | | 5 | | 5 | | 5 | | ns |
| 14 | $t_{WHCS}$ | Chip Select Hold Time | 5 | | 5 | | 5 | | 5 | | ns |

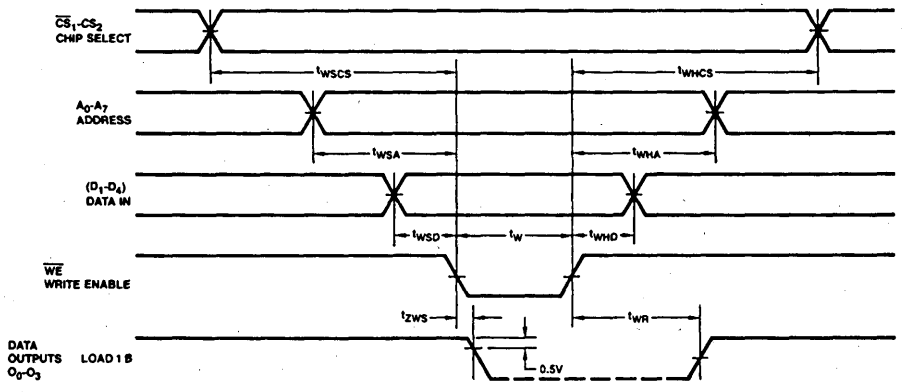
## SWITCHING WAVEFORMS

### READ MODE



## SWITCHING WAVEFORMS (Cont.)

### WRITE MODE




WF000670

(All above measurements implemented to 1.5V unless otherwise stated.)

Note: Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed to in various applications as long as the worst case limits are not violated.

# Am9128

2048 x 8 Static RAM

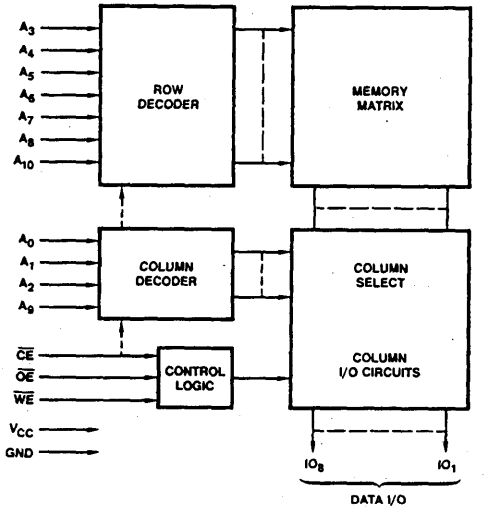
## DISTINCTIVE CHARACTERISTICS

- Logic voltage levels compatible with TTL
- Three-state output buffers-common I/O
- $I_{CC}$ max as low as 100mA
- $T_{AA}/T_{ACS}$ as low as to 70ns
- Power down mode ($I_{SB}$ as low as 15mA)

## GENERAL DESCRIPTION

The Am9128 is a 16,384-bit static Random Access Read-write Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5V supply simplify system designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROM's).

## BLOCK DIAGRAM



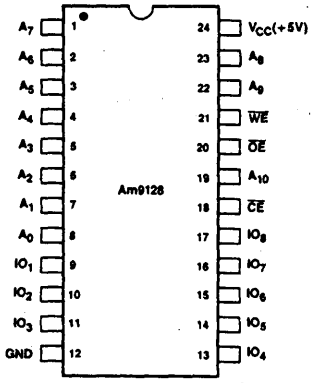

BD000280

## PRODUCT SELECTOR GUIDE

| Part Number | | Am9128-70 | Am9128-90 | Am9128-10 | Am9128-12 | Am9128-15 | Am9128-20 |
|---|---|---|---|---|---|---|---|
| Maximum Access Time (ns) | | 70 | 90 | 100 | 120 | 150 | 200 |
| Maximum Operating Current (mA) | 0°C to 70°C | 140 | N/A | 120 | N/A | 100 | 140 |
| | −55° to 125°C | N/A | 180 | N/A | 150 | 150 | 150 |
| Maximum Standby Current (mA) | 0° to 70°C | 30 | N/A | 15 | N/A | 15 | 30 |
| | −55° to 125°C | N/A | 30 | N/A | 30 | 30 | 30 |

02050C

## CONNECTION DIAGRAM
### Top View




Note: Pin 1 is marked for orientation

## BIT MAP

| Address Designators | |
|---|---|
| External | Internal |
| $A_3$ | $AX_0$ |
| $A_4$ | $AX_1$ |
| $A_5$ | $AX_2$ |
| $A_6$ | $AX_3$ |
| $A_7$ | $AX_4$ |
| $A_8$ | $AX_5$ |
| $A_{10}$ | $AX_6$ |
| $A_0$ | $AY_0$ |
| $A_1$ | $AY_1$ |
| $A_2$ | $AY_2$ |
| $A_9$ | $AY_3$ |

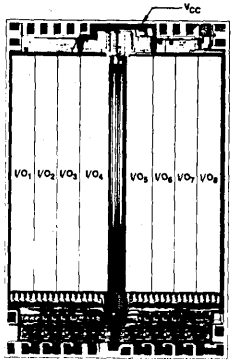



**Figure 2. Bit Mapping Information**

## ORDERING INFORMATION

**Am9128-90 D M B**

- B — Burn-in Option
  - Blank = Not Burned In
  - B = 160 Hr Burn-In
- M — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 24-pin CERDIP
  - P – 24-pin plastic
- 90 — Speed Select
  - 70 – 70ns
  - 10 – 100ns
  - 15 – 150ns
  - 20 – 200ns
  - 90 – 90ns
  - 12 – 120ns
- Am9128 — Device Type
  - 2k x 8 Static SRM

| Valid Combinations | |
|---|---|
| Am9128-70<br>Am9128-10 | DC, DCB<br>PC,PCB |
| Am9128-90<br>Am9128-12 | DM, DMB |
| Am9128-15<br>Am9128-20 | DC, DCB<br>PC,PCB<br>DM,DMB |

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
Signal Voltages with
respect to ground ..... −3.0V to +7.0V
Power Description ..... 1.0W
DC Output Current ..... 10mA

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

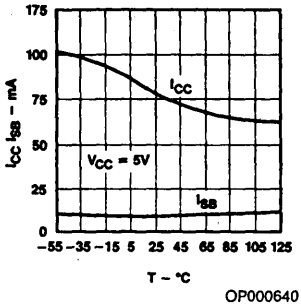
| Symbol | Parameter | Test Conditions | | Am9128-90 Am9128-10 Min | Am9128-90 Am9128-10 Max | Am9128-15 Min | Am9128-15 Max | Am9128-70 Am9128-12 Am9128-20 Min | Am9128-70 Am9128-12 Am9128-20 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| $I_{OH}$ | Output HIGH Current | $V_{OH}$ = 2.4V | $V_{CC}$ = 4.5V | −2 | | −2 | | −2 | | mA |
| $I_{OL}$ | Output LOW Current | $V_{OL}$ = 0.4V | | 4 | | 4 | | 4 | | mA |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | $V_{CC}$ + 1.0 | 2.0 | $V_{CC}$ + 1.0 | 2.0 | $V_{CC}$ + 1.0 | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | −0.5 | 0.8 | Volts |
| $I_{IX}$ | Input Load Current | $V_{SS} \leq V_I \leq V_{CC}$ | | | 10 | | 10 | | 10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O \leq V_{CC}$ Output Disabled | | | 10 | | 10 | | 10 | µA |
| $C_{IN}$ | Input Capacitance | Test Frequency = 1.0 MHz, $T_A$ = 25°C, All pins at 0V | $V_{CC}$ = 5.0V | | 6 | | 6 | | 6 | pF |
| $C_{I/O}$ | Input/Output Capacitaance | | | | 7 | | 7 | | 7 | |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | Max $V_{CC}$, $\overline{CE} \leq V_{IL}$ Outputs Open | COM'L | | 120 | | 100 | | 140 | mA |
| | | | MIL | | 180 | | 150 | | 150 | |
| $I_{SB}$ | Automatic $\overline{CE}$ Power Down Current | Max $V_{CC}$, $\overline{CE} \geq V_{IH}$ | COM'L | | 15 | | 15 | | 30 | mA |
| | | | MIL | | 30 | | 30 | | 30 | |
| $I_{PO}$ | Peak Power On Current | $V_{CC}$ = GND to $V_{CC}$ Max $\overline{CE} \geq V_{IH}$ (Note 2) | COM'L | | 15 | | 15 | | 30 | mA |
| | | | MIL | | 30 | | 30 | | 30 | |

Notes:

1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ Low and $\overline{WE}$ Low. Both signals must be Low to initiate a write and either signal can terminate a write by going High. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. A pull up resistor to $V_{CC}$ on the $\overline{CE}$ input is required during power up to keep the device deselected, otherwise $I_{PO}$ will exceed values given.
3. The operating ambient temperature range is guaranteed with transverse air flow of 400 linear feet per minute.
4. At any given temperature and voltage condition, $t_{HZ}$ is less than $t_{LZ}$ for all devices.
5. $\overline{WE}$ is High for read cycle.
6. Device is continuously selected, $\overline{CE} = V_{IL}$.
7. Address valid prior to or coincident with $\overline{CE}$ transition Low.
8. $\overline{OE} = V_{IL}$.
9. $C_L$ = 100pF for Am9128-10/-12/-15/-20. $C_L$ = 30pF for Am9128-70/90.
10. Transition is measured at 1.5V on the input to $V_{OH}$ − 500mV and $V_{OL}$ + 500mV on the outputs using the load shown in Figure 1. $C_L$ = 5pF.
11. Am9128-20 only.

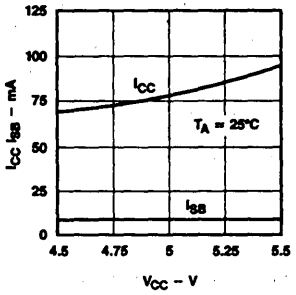
## DC OPERATING CHARACTERISTICS

**Supply Current Versus Ambient Temperature**



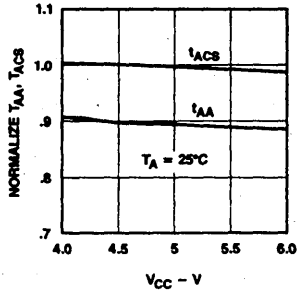

OP000640

**Supply Current Versus Supply Voltage**



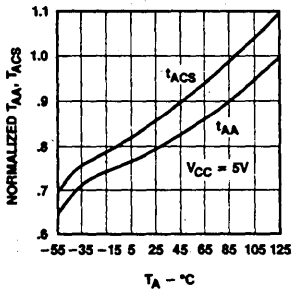

OP000650

**Normalized Access Time Versus Supply Voltage**



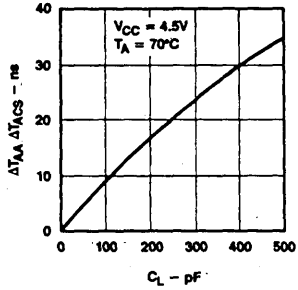

OP000660

**Normalized Access Time Versus Ambient Temperature**



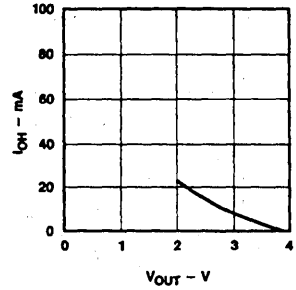

OP000670

**Access Time Change Versus Output Loading**



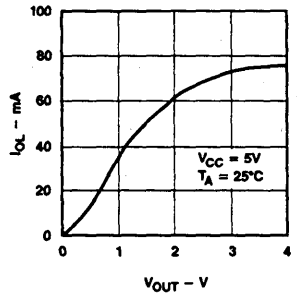

OP000680

**Output Source Current Versus Output Voltage**



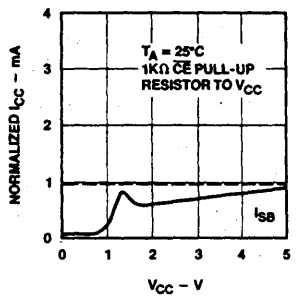

OP000690

**Output Sink Current Versus Output Voltage**



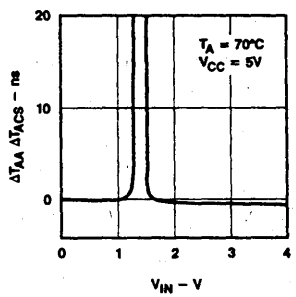

OP000700

**Typical Power-On Current Versus Power Supply**




OP000710

**Access Time Change Versus Input Voltage**

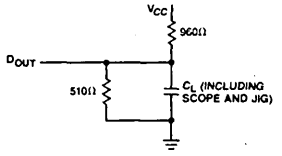



OP000720

## SWITCHING TEST CONDITIONS

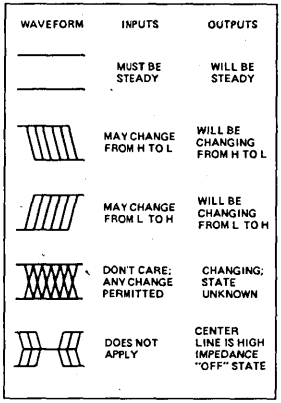
| | |
|---|---|
| Input Pulse Levels | 0 to 3.0V |
| Input Rise and Fall Times | 10ns |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |

## SWITCHING TEST CIRCUIT




TC000110

## KEY TO SWITCHING WAVEFORMS




KS000010

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

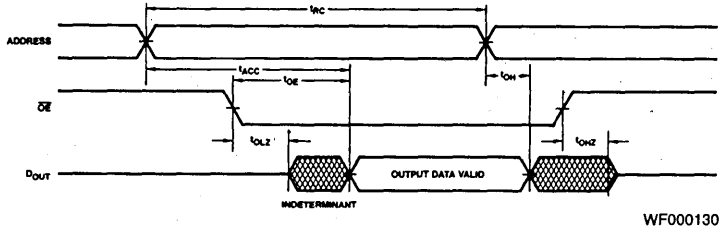
| No. | Symbol | Description | | Am9128-70 Min | Am9128-70 Max | Am9128-90 Min | Am9128-90 Max | Am9128-10 Min | Am9128-10 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | |
| 1 | $t_{RC}$ | Read Cycle Time | | 70 | | 90 | | 100 | | ns |
| 2 | $t_{ACC}$ | Address Access Time (Note 9) | | | 70 | | 90 | | 100 | ns |
| 3 | $t_{ACS}$ | Chip Select Access Time (Note 9) | | | 70 | | 90 | | 100 | ns |
| 4 | $t_{OE}$ | Output Enable Time (Note 9) | COM'L | | 40 | | N/A | | 50 | ns |
| | | | MIL | | N/A | | 50 | | N/A | |
| 5 | $t_{OH}$ | Output Hold Time from Address Change | | 5 | | 5 | | 5 | | ns |
| 6 | $t_{CLZ}$ | Output in LOW-Z from $\overline{CE}$ (Notes 4, 10) | | 5 | | 5 | | 5 | | ns |
| 7 | $t_{CHZ}$ | Output in HIGH-Z from $\overline{CE}$ (Notes 4, 10) | | | 35 | | 40 | | 40 | ns |
| 8 | $t_{OLZ}$ | Output in LOW-Z from $\overline{OE}$ (Notes 4, 10) | | 5 | | 5 | | 5 | | ns |
| 9 | $t_{OHZ}$ | Output in HIGH-Z from $\overline{OE}$ (Notes 4, 10) | | | 30 | | 35 | | 35 | ns |
| 10 | $t_{PU}$ | Chip Selection to Power Up Time | | 0 | | 0 | | 0 | | ns |
| 11 | $t_{PD}$ | Chip Deselection to Power Down Time | | | 40 | | 45 | | 50 | ns |
| **Write Cycle** | | | | | | | | | | |
| 12 | $t_{WC}$ | Write Cycle Time | | 70 | | 90 | | 100 | | ns |
| 13 | $t_{CW}$ | Chip Selection to End of Write (Note 1) | 0°C to +70°C | 60 | | N/A | | 90 | | ns |
| | | | −55°C to −125°C | N/A | | 80 | | N/A | | |
| 14 | $t_{AS}$ | Address Setup Time | | 5 | | 10 | | 10 | | ns |
| 15 | $t_{WP}$ | Write Pulse Width (Note 1) | | 40 | | 55 | | 60 | | ns |
| 16 | $t_{WR}$ | Write Recovery Time | | 5 | | 5 | | 5 | | ns |
| 17 | $t_{DS}$ | Data Setup Time | | 30 | | 35 | | 40 | | ns |
| 18 | $t_{DH}$ | Data Hold Time | | 5 | | 5 | | 5 | | ns |
| 19 | $t_{WLZ}$ | Output in LOW-Z from $\overline{WE}$ (Notes 4, 10) | | 5 | | 5 | | 5 | | ns |
| 20 | $t_{WHZ}$ | Output in HIGH-Z from $\overline{WE}$ (Notes 4, 10) | | | 30 | | 35 | | 35 | ns |
| 21 | $t_{AW}$ | | | 65 | | 80 | | 80 | | ns |

## SWITCHING CHARACTERISTICS (Cont.)

| No. | Symbol | Description | | Am9128-12 Min | Am9128-12 Max | Am9128-15 Min | Am9128-15 Max | Am9128-20 Min | Am9128-20 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | | | |
| 1 | $t_{RC}$ | Read Cycle Time | | 120 | | 150 | | 200 | | ns |
| 2 | $t_{ACC}$ | Address Access Time (Note 9) | | | 120 | | 150 | | 200 | ns |
| 3 | $t_{ACS}$ | Chip Select Access Time (Note 9) | | | 120 | | 150 | | 200 | ns |
| 4 | $t_{OE}$ | Output Enable Time (Note 9) | COM'L | | N/A | | 60 | | 70 | ns |
| | | | MIL | | 70 | | 70 | | 80 | |
| 5 | $t_{OH}$ | Output Hold Time from Address Change | | 5 | | 5 | | 5 | | ns |
| 6 | $t_{CLZ}$ | Output in LOW-Z from $\overline{CE}$ (Notes 4, 10) | | 5 | | 5 | | 5 | | ns |
| 7 | $t_{CHZ}$ | Output in HIGH-Z from $\overline{CE}$ (Notes 4, 10) | | | 50 | | 55 | | 55 | ns |
| 8 | $t_{OLZ}$ | Output in LOW-Z from $\overline{OE}$ (Notes 4, 10) | | 5 | | 5 | | 5 | | ns |
| 9 | $t_{OHZ}$ | Output in HIGH-Z from $\overline{OE}$ (Notes 4, 10) | | | 45 | | 50 | | 50 | ns |
| 10 | $t_{PU}$ | Chip Selection to Power Up Time | | 0 | | 0 | | 0 | | ns |
| 11 | $t_{PD}$ | Chip Deselection to Power Down Time | | | 55 | | 60 | | 60 | ns |
| **Write Cycle** | | | | | | | | | | |
| 12 | $t_{WC}$ | Write Cycle Time | | 120 | | 150 | | 200 | | ns |
| 13 | $t_{CW}$ | Chip Selection to End of Write (Note 1) | COM'L | N/A | | 120 | | 150 | | ns |
| | | | MIL | 105 | | 130 | | 160 | | |
| 14 | $t_{AS}$ | Address Setup Time | | 10 | | 20 | | 20 | | ns |
| 15 | $t_{WP}$ | Write Pulse Width (Note 1) | | 70 | | 85 | | 100 | | ns |
| 16 | $t_{WR}$ | Write Recovery Time | | 5 | | 5 | | 5 | | ns |
| 17 | $t_{DS}$ | Data Setup Time | | 45 | | 50 | | 60 | | ns |
| 18 | $t_{DH}$ | Data Hold Time | | 5 | | 5 | | 5 | | ns |
| 19 | $t_{WLZ}$ | Output in LOW-Z from $\overline{WE}$ (Notes 4, 10) | | 5 | | 5 | | 5 | | ns |
| 20 | $t_{WHZ}$ | Output in HIGH-Z from $\overline{WE}$ (Notes 4, 10) | | | 50 | | 50 | | 50 | ns |
| 21 | $t_{AW}$ | | | 105 | | 120 | | 120 | | ns |

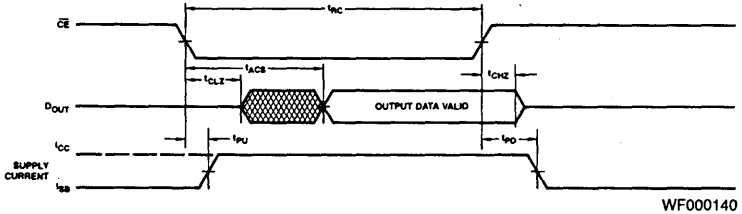
## SWITCHING WAVEFORMS

### READ CYCLE NO. 1 (Notes 5, 6)




WF000130

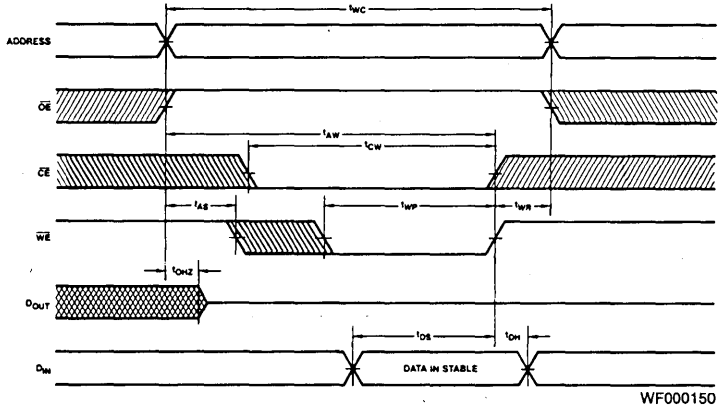
### READ CYCLE 2 (Notes 5, 7, 8)




WF000140

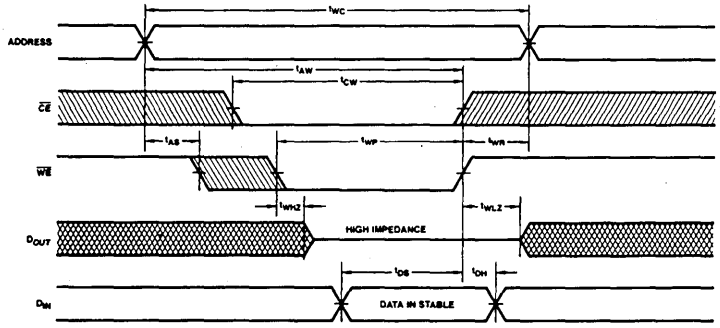
## SWITCHING WAVEFORMS (Cont.)

### WRITE CYCLE 1




WF000150

### WRITE CYCLE NO. 2 (Notes 7, 8)




WF000160

# MOS Read Only Memories (ROM) Index

# Am9218

2048 x 8 ROM

## DISTINCTIVE CHARACTERISTICS

- Plug-in replacement for 8316E; 2716 compatible
- Access times as fast as 350 ns
- 3 fully programmable Chip Selects — increased flexibility
- Logic voltage levels compatible with TTL
- Three-state output buffers — simplified expansion
- Low power dissipation

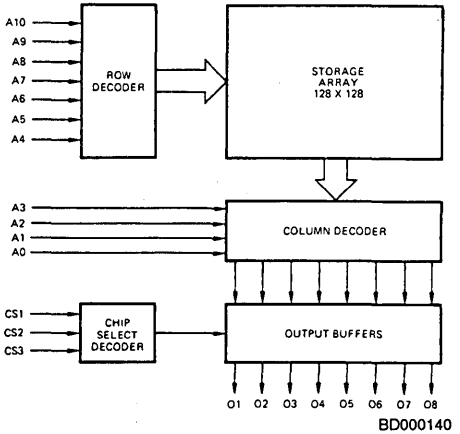
## GENERAL DESCRIPTION

The Am9218 devices are high performance, 16384-bit, static, mask programmed, read only memories. Each memory is implemented as 2048 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes as small as 2048 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Three programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 8 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9218 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by whatever address is present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

## BLOCK DIAGRAM



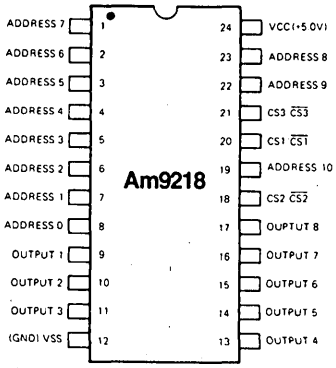

BD000140

## PRODUCT SELECTOR GUIDE

| Access Times | 450ns | 350ns |
|---|---|---|
| Part Number | Am9218B | Am9218C |

03243 C

## CONNECTION DIAGRAM
### Top View




CD000210

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am9218 B P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - C – 24-pin CERDIP
  - D – 24-pin ceramic
  - P – 24-pin plastic
- B — Speed Select
  - B – 450ns
  - C – 350ns
- Am9218 — Device Type
  - 2k x 8 ROM

| Valid Combinations | |
|---|---|
| 9218B | PC, CC, DC, DM |
| 9218C | PC, CC, DC |

## PROGRAMMING INSTRUCTIONS

### CUSTOM PATTERN ORDERING INFORMATION

The Am9218 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.
Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

### FIRST CARD

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 9218 |
| 65 thru 72 | Optional Information |

### SECOND CARD

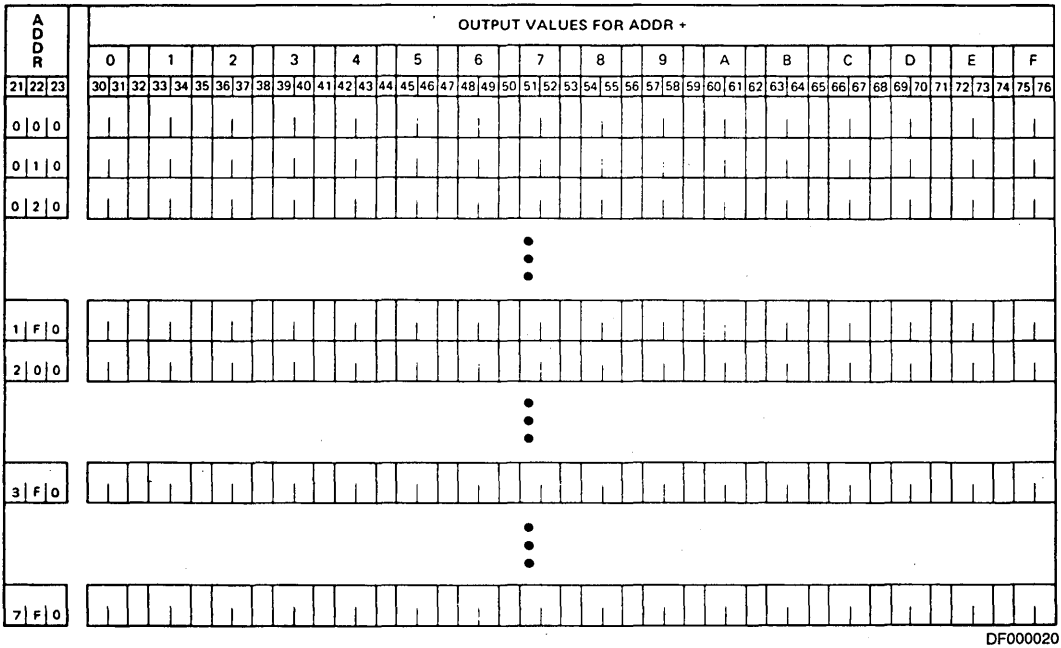
| Column Number | Description |
|---|---|
| 29 | CS3 input required to select chip (0 or 1) |
| 31 | CS2 input required to select chip (0 or 1) |
| 33 | CS1 input required to select chip (0 or 1) |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 2048 data cards are required.

| Column Number | |
|---|---|
| 10, 12, 14, 16, 18 20, 22, 24, 26, 28, 30 | Address input pattern with the most significant bit (A10) in column 10 and the least significant bit (A0) in column 30. |
| 40, 42, 44, 46, 48 50, 52, 54 | Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 128 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through 7F: 128 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.




DF000020

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... +7.0V
DC Signal Voltage applied to outputs ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V
Power Dissipation ..... 1.0W

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

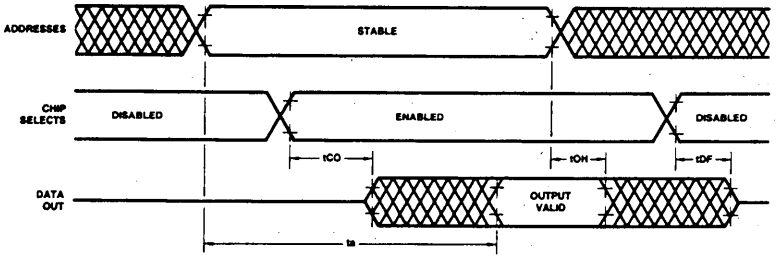
| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage | $I_{OH} = -200\mu A$ | C devices | 2.4 | | | V |
| | | | M devices | 2.2 | | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 3.2$ mA | C devices | | | 0.4 | |
| | | | M devices | | | 0.45 | |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ +1.0V | |
| $V_{IL}$ | Input Low Voltage | | | −0.5 | | +0.8 | |
| $I_{LO}$ | Output Leakage Current | Chip Disabled | | | | 10 | µA |
| $I_{LI}$ | Input Leakage Current | | | | | 10 | |
| $I_{CC}$ | Power Supply Current | | C devices | | | 70 | mA |
| | | | M devices | | | 80 | |
| $C_{IN}$ | Input Capacitance | $T_A = 25°C$, f = 1MHz All pins at 0V | | | | 7 | pF |
| $C_{OUT}$ | Output Capacitance | | | | | 7 | |

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | Am9218B | | Am9218C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 1 | $t_A$ | Address to Output Access Time | tr = tf = 20ns Output load: One Standard TTL Gate plus 100pF (Note 1) | | 450 | | 350 | ns |
| 2 | $t_{CO}$ | Chip Select to Output ON Delay | | | 150 | | 130 | ns |
| 3 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | ns |
| 4 | $t_{DF}$ | Chip Select to Output OFF Delay | | | 150 | | 130 | ns |

Note: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

### SWITCHING WAVEFORMS




WF000030

# Am9232/33

4096 x 8 ROM

## DISTINCTIVE CHARACTERISTICS

- Access time selected to 300ns
- Fully capacitive inputs — simplified driving
- Two mask programmable chip selects — increased flexibility
- Three-state output buffers — simplified expansion
- Two different pinouts for universal application
- Non-connect option on chip selects

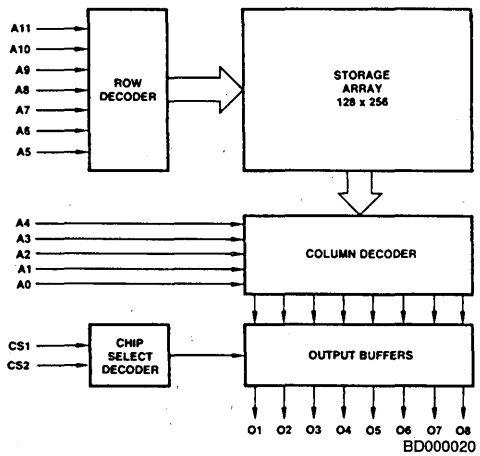
## GENERAL DESCRIPTION

The Am9232/33 devices are high performance, 32,768-bit, static, mask programmed, read only memories. Each memory is implemented as 4096 words by 8 bits per word. This organization simplifies the design of small memory systems and permits incremental memory sizes of 4096 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

Two programmable Chip Select input signals are provided to control the output buffers. Each Chip Select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional AM9232/33 devices and other three-state components.

These memories are fully static and require no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output voltage levels are compatible with TTL specifications.

## BLOCK DIAGRAM



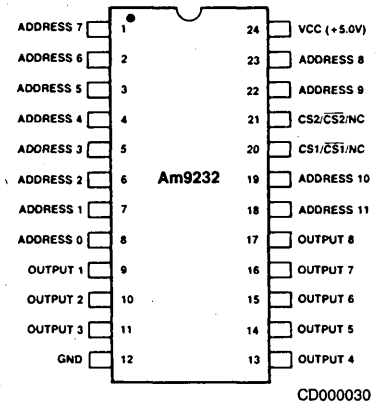

BD000020

## PRODUCT SELECTOR GUIDE

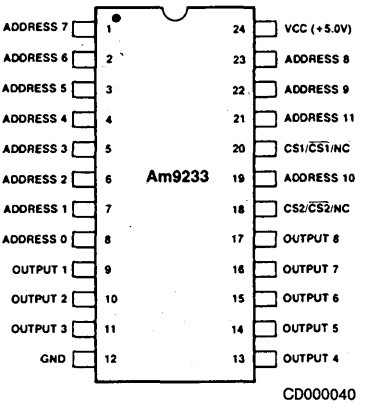
| Access Times | 450ns | 300ns |
|---|---|---|
| Part Number | Am9232B<br>Am9233B | Am9232C<br>Am9233C |

03249C

## CONNECTION DIAGRAM
### Top View




CD000030




CD000040

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am9232 B P C**

- Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 24-pin ceramic DIP
  - C – 24-pin CERDIP
  - P – 24-pin plastic DIP
- Speed Select
  - B – 450ns
  - C – 300ns
- Device Type
  - Am9232 – pinout #1
  - Am9233 – pinout #2

| Valid Combinations | |
|---|---|
| Am9232B<br>Am9233B | PC, CC<br>DM, DC |
| Am9232C<br>Am9233C | PC, CC<br>DC |

5

# PROGRAMMING INSTRUCTIONS

## CUSTOM PATTERN ORDERING INFORMATION

The Am9232 is programmed from punched cards, card coding forms or paper tape in card image format as shown below.
Logic "1" = a more positive voltage (normally +5.0V)
Logic "0" = a more negative voltage (normally 0V)

### FIRST CARD

| Column Number | Description |
|---|---|
| 10 thru 29 | Customer Name |
| 32 thru 37 | Total number of "1's" contained in the data. This is optional and should be left blank if not used. |
| 50 thru 62 | 9232 or 9233 |
| 65 thru 72 | Optional Information |

### SECOND CARD

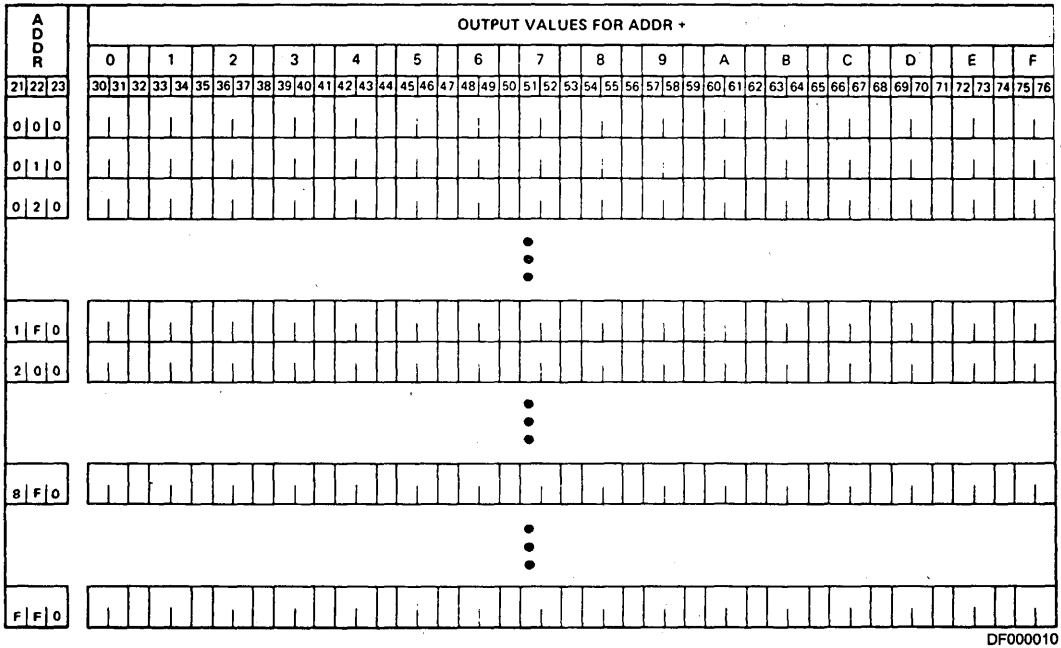
| Column Number | Description |
|---|---|
| 31 | CS2 input required to select chip (0 or 1); If CS2 = NC, column 31 = 2. |
| 33 | CS1 input required to select chip (0 or 1); If CS1 = NC, column 33 = 2. |

Two options are provided for entering the data pattern with the remaining cards.

**OPTION 1** is the Binary Option where the address and data are presented in binary form on the basis of one word per card. With this option 4096 data cards are required.

| Column Number | |
|---|---|
| 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30 | Address input pattern with the most significant bit (A11) in column 8 and the least significant bit (A0) in column 30. |
| 40, 42, 44, 46, 48 50, 52, 54 | Output pattern with the most significant bit (O8) in column 40 and the least significant bit (O1) in column 54. |
| 73 thru 80 | Coding these columns is not essential and may be used for card identification purposes. |

**OPTION 2** is the Hexadecimal Option and is a much more compact way of presenting the data. This format requires only 256 data cards. Each data card contains the 8-bit output information for 16 storage locations in the memory. The address indicated in columns 21, 22 and 23 is the address of the data presented in columns 30 and 31. Addresses for successive data are assumed to be in incremental ascending order from the initial address. Since the address in columns 21, 22 and 23 always points only to the first data on the card, column 23 is always zero. Columns 21 and 22 take all hex values from 00 through FF:256 cards in all. Data is entered in hex values and may be any combination of 8 bits, that is, hex values from 00 through FF.




DF000010



03249C

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... +7.0V
DC Signal Voltage applied to outputs ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V
Power Dissipation ..... 1.0W

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | $V_{CC} = 4.75$ | 2.4 | | | Volts |
| | | | $V_{CC} = 4.50$ | 2.2 | | | |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ +1.0V | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Load Current | $GND \leq V_I \leq V_{CC}$ | | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $GND \leq V_O \leq V_{CC}$ Chip Disabled | +70°C | | | 10 | μA |
| | | | +125°C (DM) | | | 50 | |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 0°C | | | 80 | mA |
| | | | −55°C (DM) | | | 100 | |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1.0MHz All pins at 0V | | | | 7.0 | pF |
| $C_O$ | Output Capacitance | | | | | 7.0 | pF |

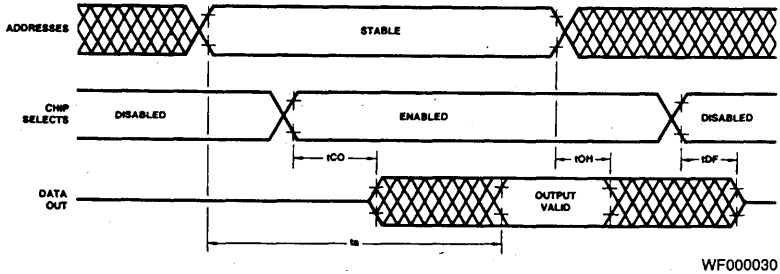
5

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | Am9232/33B | | Am9232/33C | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| 1 | $t_A$ | Address to Output Access Time | tr = tf = 20ns<br>Output load:<br>One Standard TTL Gate<br>plus 100pF (Note 1) | | 450 | | 300 | ns |
| 2 | $t_{CO}$ | Chip Select to Output ON Delay | | | 150 | | 120 | ns |
| 3 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | ns |
| 4 | $t_{DF}$ | Chip Select to Output OFF Delay | | | 150 | | 120 | ns |

Note: 1. Timing reference levels: High = 2.0V, Low = 0.8V.

## SWITCHING WAVEFORMS




WF000030

# Am9264

64K (8192 x 8) ROM

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Enhanced manufacturability with post-metal programming
- Access time — 250ns (max)
- Single +5V ±10% power supply
- Fully static operation
- Completely TTL compatible
- Pin compatible with 16K/32K/64K EPROMs/ROMs

## GENERAL DESCRIPTION

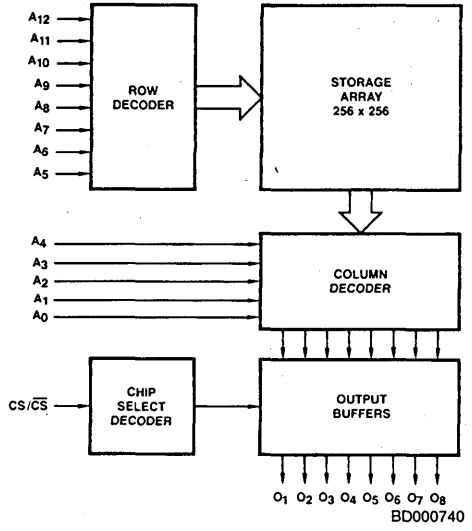
The Am9264 high performance read only memory is organized 8192 words by 8 bits with access time of less than 250ns. This organization simplifies the design of small memory systems and permits incremental memory sizes of 8192 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

The programmable chip select input signal is provided to control the output buffers. Chip Select Polarity may be provided by the customer thus allowing the addressing of 2 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9264 devices and other three state components.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) will result in faster turn around time for new or old patterns. This technique will allow us to test wafers before committing customer patterns to categorize speed and power dissipation requirements.

## BLOCK DIAGRAM

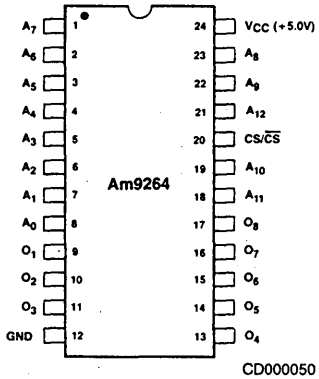



## PRODUCT SELECTOR GUIDE

| Access Times | 450ns | 300ns | 250ns |
|---|---|---|---|
| Part Number | Am9264B | Am9264C | Am9264D |

01241B

## CONNECTION DIAGRAM
### Top View




Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am9264 B P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - C – 24-pin CERDIP
  - D – 24-pin ceramic DIP
  - P – 24-pin plastic DIP
- B — Speed Select
  - B – 450ns
  - C – 300ns
  - D – 250ns
- Am9264 — Device Type
  - 8k x 8 ROM

| Valid Combinations | |
|---|---|
| Am9264B | PC, CC<br>DC, DM |
| Am9264C | PC, CC<br>DC |
| Am9264D | PC, CC<br>DC |

## ROM CODE DATA

### EPROM

AMD's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs programmed with identical data should be submitted. AMD will read the programmed EPROM and generate an Intel Hex paper tape. The second EPROM is compared with Intel Hex paper tape to insure that both EPROMs have identical data. Then AMD generates a PG tape (Pattern Generation) which is used to make masks after customer gives a code approval. One of the EPROMs is erased and then it is programmed from AMD's data base. The AMD programmed EPROM is returned to the customer for code verification of the ROM program. Unless otherwise requested, AMD will not proceed until the customer verifies the program in the returned EPROM. AMD requests a written verification form (supplied by AMD with programmed EPROM) signed by customer before proceeding to any further work.

The following EPROMs should be used for submitting ROM CODE DATA:

| ROM | | EPROM | |
|---|---|---|---|
| | | Preferred | Optional |
| Am9218 | 2K x 8 | 2716 | 2516/2-2708 |
| Am9232/33 | 4K x 8 | 2732 | 2532/2-2716 |
| Am9264 | 8K x 8 | 2764 | 4-2716/2-2732 |
| Am9265 | 8k x 8 | 2764 | 4-2176/2-2732 |

If more than one EPROM is used to specify one ROM pattern, (i.e., 4 16K EPROMs or 2 32K EPROMs for one 64K ROM) two complete sets of programmed EPROMs should be submitted. In this instance, the programmed EPROMs must clearly state which of the two or four EPROMs is for lower and upper address locations in the ROM.

### CARD FORMAT

If customer prefers to submit punch cards, be sure to provide the industry standard formats, such as:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
MOTOROLA HEXADECIMAL
EA OCTAL
G.I. BINARY

### CHIP SELECT INFORMATION

Regardless of the method of submitting ROM CODE DATA (EPROM or CARDs), the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

### KEY POINTS

- Obtain AMD's 5 digit code number from product marketing
- Supply chip select information
- Supply customer part number and appropriate AMD part number
- Supply marking information
- Instruction on whether prototype approval is required prior to production or AMD is allowed to go straight to production (in case of code change or error, customer is liable for all products in line) after customer code approval.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... +7.0V
DC Signal Voltage applied to outputs ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V
Power Dissipation ..... 1.0W

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

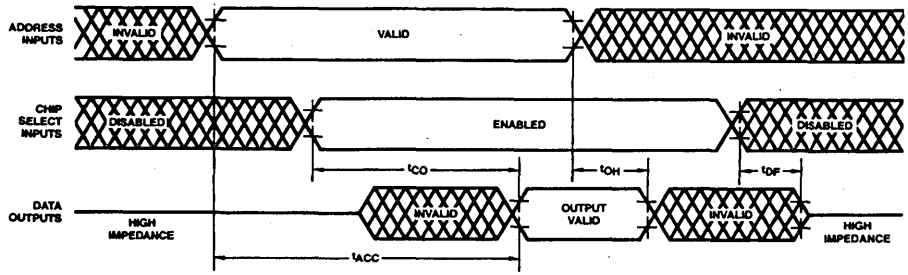
| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -200\mu A$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ +1.0V | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $GND \leq V_O \leq V_{CC}$ Chip Disabled | +70°C | | | 10 | μA |
| | | | +125°C (DM) | | | 50 | |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 0°C | | | 80 | mA |
| | | | −55°C (DM) | | | 100 | |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1.0MHz | | | | 7.0 | pF |
| $C_O$ | Output Capacitance | All pins at 0V | | | | 7.0 | pF |

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | Am9264B | | Am9264C | | Am9264D | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_A$ | Address to Output Access Time | $t_r = t_f = 20ns$ | | 450 | | 300 | | 250 | ns |
| 2 | $t_{CO}$ | Chip Select to Output ON Delay | Output Load: One Standard TTL Gate Plus 100pF (Note 1) | | 150 | | 120 | | 100 | ns |
| 3 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | 20 | | ns |
| 4 | $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | | 100 | | 80 | ns |

Note: 1. Timing reference levels: High = 2.0V. Low = 0.8V.

### SWITCHING WAVEFORMS




WF000050

# Am9265

64K (8192 x 8) ROM

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Access time — 250ns (max)
- Automatic power down feature controlled by separate $\overline{CE}$ pin.
- Separate $\overline{OE}$ pin for tri-state output control
- Two programmable chip selects with no-connect option
- Pin compatible with 28 pin 64K and higher density ROMs/EPROMs
- Completely TTL compatible

## GENERAL DESCRIPTION

The Am9265 high performance read only memory is organized 8192 words by 8 bits with access times of less than 250ns. This organization simplifies the design of small memory systems and permits incremental memory sizes of 8192 words. The fast access times provided allow the ROM to service high performance microcomputer applications without stalling the processor.

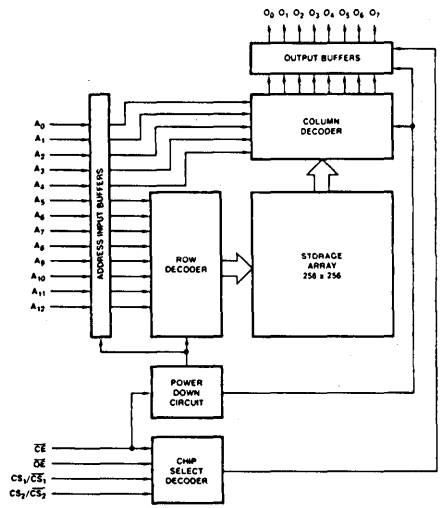
Two programmable chip select inputs are provided to control the output buffers. Chip select polarity may be specified by the customer thus allowing the addressing of 4 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am9265 devices and other three state components. No-connect option on chip selects can be provided if desired by the customer.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The Am9265 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 80mA to 20mA, a 75% reduction.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

## BLOCK DIAGRAM



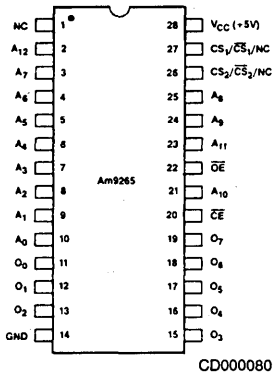

BD000290

## PRODUCT SELECTOR GUIDE

| Access Times | 450ns | 300ns | 250ns |
|---|---|---|---|
| Part Number | Am9265B | Am9265C | Am9265D |

01674C

## CONNECTION DIAGRAM
### Top View




CD000080

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am9265 B P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- P — Package
  - C – 24-pin CERDIP
  - D – 24-pin ceramic DIP
  - P – 24-pin plastic DIP
- B — Speed Select
  - B – 450ns
  - C – 300ns
  - D – 250ns
- Am9265 — Device Type
  - 8k x 8 ROM

| Valid Combinations | |
|---|---|
| Am9265B | PC, CC<br>DC, DM |
| Am9265C | PC, CC<br>DC |
| Am9265D | PC, CC<br>DC |

5

## ROM CODE DATA

AMD's preferred method of receiving ROM code data is in EPROM. Two identically programmed EPROMs should be submitted for code verification purposes. AMD will read one of the EPROMs and store contents in a floppy disk. The contents of the second EPROM are compared with the stored data for consistency. The second EPROM is erased and then reprogrammed and submitted to the customer for verification of the ROM code, along with code listing. Unless otherwise requested, AMD will not proceed until production is authorized by means of a signed MOS ROM verification form (submitted with code verification data).

The following EPROMs should be used for submitting ROM code data:

| ROM | | EPROM | |
|---|---|---|---|
| | | Preferred | Optional |
| Am9218 | 2K x 8 | 2716 | 2716 |
| Am9232/33 | 4K x 8 | 2732 | 2532/2-2716 |
| Am9264 | 8K x 8 | 2764 | 4-2716/2-2732 |
| Am9265 | 8k x 8 | 2764 | 4-2176/2-2732 |

If more than one EPROM is used to specify a ROM pattern, the upper and lower address locations must be clearly specified.

### CARD FORMAT

If card decks are preferred as code inputs, the following industry standard formats are acceptable:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
MOTOROLA HEXADECIMAL
EA OCTAL
G.I. BINARY

### PAPER TAPE FORMAT

If punched paper tape is preferred as code input, most industry standard formats are acceptable. Verify with factory before submittal.

### CHIP SELECT INFORMATION

Regardless of the method of submitting ROM code data, the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

### KEY POINTS

- Supply 2 sets of identically programmed EPROMs.
- Specify customer part number and appropriate AMD part number.
- Supply marking information.
- Identify upper and lower address location when more than one EPROM is used.
- Cover EPROM window with opaque material to prevent bit loss.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... +7.0V
DC Signal Voltage applied to outputs ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V
Power Dissipation ..... 1.0W

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -400\mu A$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ +1.0V | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $GND \leq V_O \leq V_{CC}$ Chip Disabled | +70°C | | | 10 | μA |
| | | | +125°C (DM) | | | 50 | |
| $I_{CC1}$ | $V_{CC}$ Standby Current | | 0°C | | | 20 | mA |
| | | | −55°C (DM) | | | 25 | |
| $I_{CC2}$ | $V_{CC}$ Operating Current | | 0°C | | | 80 | mA |
| | | | −55°C (DM) | | | 100 | |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1.0MHz All pins at 0V | | | | 7.0 | pF |
| $C_O$ | Output Capacitance | | | | | 7.0 | pF |

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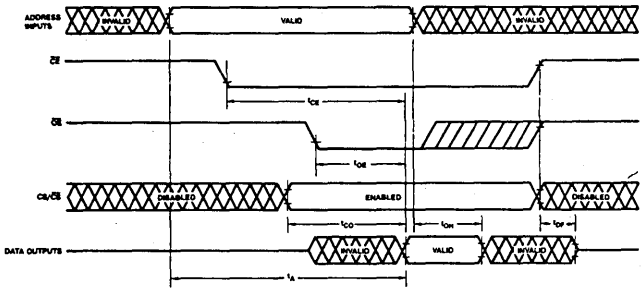
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | Am9265B | | Am9265C | | Am9265D | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_A$ | Address to Output Access Time | tr = tf = 10ns Output Load One Standard TTL Gate Plus 100pF (Note 1) | | 450 | | 300 | | 250 | ns |
| 2 | $t_{CO}$ | Chip Select to Output ON Delay | | | 150 | | 120 | | 100 | ns |
| 3 | $t_{OE}$ | Output Enable to Output ON Delay | | | 150 | | 120 | | 100 | ns |
| 4 | $t_{CE}$ | $\overline{CE}$ to Output ON Delay | | | 450 | | 300 | | 250 | ns |
| 5 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | 20 | | ns |
| 6 | $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | | 100 | | 80 | ns |

Notes:
1. Timing reference levels:High = 2.0V, Low = 0.8V.
2. $t_{DF}$ is the worst case OFF delay. If $\overline{OE}$ occurs before $\overline{CE}$ and CS/$\overline{CS}$ are disabled, then $t_{DF}$ is referenced to $\overline{OE}$ only. If $\overline{OE}$, CS/$\overline{CS}$ and $\overline{CE}$ are disabled simultaneously, then $t_{DF}$ is referenced to all three.

## SWITCHING WAVEFORMS




WF000060

# Am92128

128K (16,384 x 8) ROM

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Access time — 250ns (max)
- Single +5V ±10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin
- Separate $\overline{OE}$ pin for three-state output control
- Programmable chip select with no-connect option
- Pin compatible with 28-pin and high density ROMs/EPROMs

## GENERAL DESCRIPTION

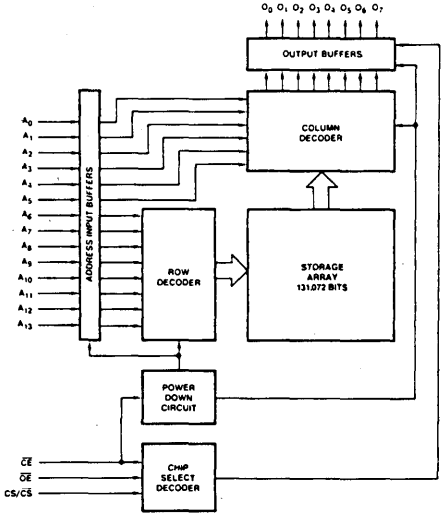
The Am92128 high performance read only memory is organized 16,384 words by 8 bits and has access times of less than 250ns. This organization simplifies the design of memory systems and permits incremental memory sizes of 16,384 bytes. The fast access times provided allow the ROM to service high performance microcomputer applications without inserting wait states.

One programmable chip select input is provided to control the output buffers. Chip select polarity may be specified by the customer thus allowing the addressing of 2 memory chips without external gating. The outputs of the unselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am92128 devices and other three-state components.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

## BLOCK DIAGRAM




BD000010

## MODE SELECT TABLE

| $\overline{CS}$ or CS | | $\overline{CE}$ | $\overline{OE}$ | Mode | Outputs | Power |
|---|---|---|---|---|---|---|
| H | L | L | X | Deselected | High-Z | Active |
| H | L | H | X | Deselected | High-Z | Standby |
| L | H | L | H | Inhibit | High-Z | Active |
| L | H | H | X | Deselected | High-Z | Standby |
| L | H | L | L | Read | $D_{OUT}$ | Active |

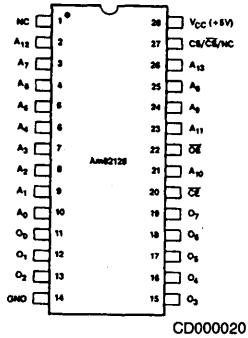
H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

| Access Times | 450ns | 300ns | 250ns |
|---|---|---|---|
| Part Number | Am92128B | Am92128C | Am92128D |

03181B

## CONNECTION DIAGRAM
### Top View




CD000020

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am92128 B P C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
- P — Package
  - C – 28-pin CERDIP
  - D – 28-pin ceramic DIP
  - P – 28-pin plastic DIP
- B — Speed Select
  - B – 450ns
  - C – 300ns
  - D – 250ns
- Am92128 — Device Type
  - 16k x 8 ROM

| Valid Combinations | |
|---|---|
| Am92128B | PC, CC, DM |
| Am92128C | PC, CC |
| Am92128D | PC, CC |

## ROM CODE DATA

AMD's preferred method of receiving ROM code data is in EPROM. Two identically programmed EPROMs should be submitted for code verification purposes. AMD will read one of the EPROMs and store contents in a floppy disk. The contents of the second EPROM are compared with the stored data for consistency. The second EPROM is erased and then reprogrammed and submitted to the customer for verification of the ROM code, along with code listing. Unless otherwise requested, AMD will not proceed until production is authorized by means of a signed MOS ROM verification form (submitted with code verification data).

The following EPROMs should be used for submitting ROM code data:

| ROM | | EPROM | |
|---|---|---|---|
| | | Preferred | Optional |
| Am9217/18 | 2K x 8 | 2716 | 2516/2-2708 |
| Am9232/33 | 4K x 8 | 2732 | 2532/2-2716 |
| Am9264 | 8K x 8 | 2764 | 4-2716/2-2732 |
| Am9264 | 8K x 8 | 2764 | 4-2716/2-2732 |
| Am9128 | 16k x 8 | 2128 | 2-2764 |

If more than one EPROM is used to specify a ROM pattern, the upper and lower address locations must be clearly specified.

### CARD FORMAT

If card decks are preferred as code inputs, the following industry standard formats are acceptable:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
MOTOROLA HEXADECIMAL
EA OCTAL
G.I. BINARY

### PAPER TAPE FORMAT

If punched paper tape is preferred as code input, most industry standard formats are acceptable. Verify with factory before submittal.

### CHIP SELECT INFORMATION

Regardless of the method of submitting ROM code data, the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

### KEY POINTS

- Supply 2 sets of identically programmed EPROMs.
- Specify customer part number and appropriate AMD part number.
- Supply marking information.
- Identify upper and lower address location when more than one EPROM is used.
- Cover EPROM window with opaque material to prevent bit loss.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... +7.0V
DC Signal Voltage applied to outputs ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V
Power Dissipation ..... 1.0W

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.5V to +5.5V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

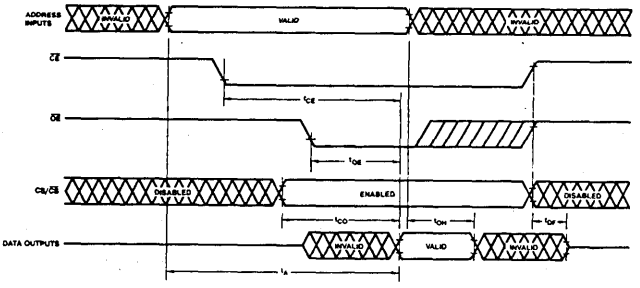
| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -400\mu A$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ +1.0V | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $GND \leq V_O \leq V_{CC}$ Chip Disabled | +70°C | | | 10 | µA |
| | | | +125°C (DM) | | | 50 | |
| $I_{CC1}$ | $V_{CC}$ Standby Current | | 0°C | | | 25 | mA |
| | | | −55°C (DM) | | | 30 | |
| $I_{CC2}$ | $V_{CC}$ Operating Current | | 0°C | | | 80 | mA |
| | | | −55°C (DM) | | | 100 | |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1.0MHz All pins at 0V | | | | 7.0 | pF |
| $C_O$ | Output Capacitance | | | | | 7.0 | pF |

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | Am92128B | | Am92128C | | Am92128D | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_A$ | Address to Output Access Time | tr = tf = 10ns Output Load: One Standard TTL Gate Plus 100pF (Note 1) | | 450 | | 300 | | 250 | ns |
| 2 | $t_{CO}$ | Chip Select to Output ON Delay | | | 150 | | 120 | | 100 | ns |
| 3 | $t_{OE}$ | Output Enable to Output ON Delay | | | 150 | | 120 | | 100 | ns |
| 4 | $t_{CE}$ | $\overline{CE}$ to Output ON Delay | | | 450 | | 300 | | 250 | ns |
| 5 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | 20 | | ns |
| 6 | $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | | 100 | | 80 | ns |

Notes:
1. Timing reference levels:High = 2.0V, Low = 0.8V.
2. $t_{DF}$ is the worst case OFF delay. If $\overline{OE}$ occurs before $\overline{CE}$ and CS/$\overline{CS}$ are disabled, then $t_{DF}$ is referenced to $\overline{OE}$ only. If $\overline{OE}$, CS/$\overline{CS}$ and $\overline{CE}$ are disabled simultaneously, then $t_{DF}$ is referenced to all three.

## SWITCHING WAVEFORMS




WF000020

# Am92256

256K (32,768 x 8) ROM

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Access time — 250ns (max)
- Single +5V ±10% power supply
- Automatic power down feature controlled by separate $\overline{CE}$ pin
- Separate $\overline{OE}$ pin for three-state output control
- Pin compatible with 28-pin high density ROMs/EPROMs
- TTL compatible

## GENERAL DESCRIPTION

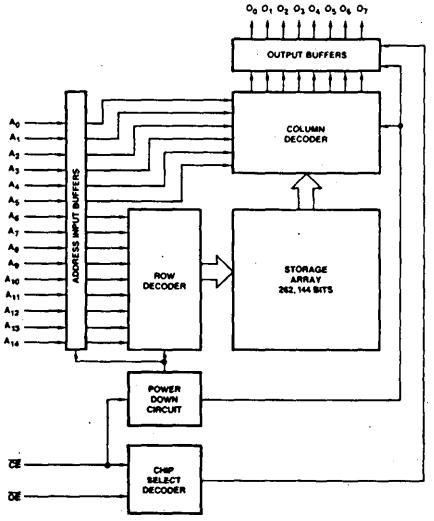
The Am92256 high performance read only memory is organized 32,768 words by 8 bits and has access times of less than 250ns. This organization simplifies the design of memory systems and permits incremental memory sizes of 32,768 bytes. The fast access times provided allow the ROM to service high performance microcomputer applications without inserting wait states.

The Am92256 features an automatic stand-by mode. When deselected by $\overline{CE}$, the maximum supply current is reduced from 120mA to 30mA, a 75% reduction. The outputs of the deselected chips are turned off and assume a high impedance state. This permits wire-ORing with additional Am92256 devices and other three-state components.

This memory is fully static and requires no clock signals of any kind. A selected chip will output data from a location specified by the address present on the address input lines. Input and output levels are compatible with TTL specifications. A separate $\overline{OE}$, output enable pin, controls outputs providing greater system flexibility and eliminating bus contention.

The ability to program customer code at the last step of fabrication (Post Metal Programming Technique) results in faster turn around time for new or old patterns. This technique also allows testing of wafers to categorize speed and power dissipation before committing customer patterns.

## BLOCK DIAGRAM




BD000260

## MODE SELECT TABLE

| $\overline{CE}$ | $\overline{OE}$ | Mode | Outputs | Power |
|---|---|---|---|---|
| H | X | Deselect | High-Z | Standby |
| L | H | Inhibit | High-Z | Active |
| L | L | Read | $D_{OUT}$ | Active |

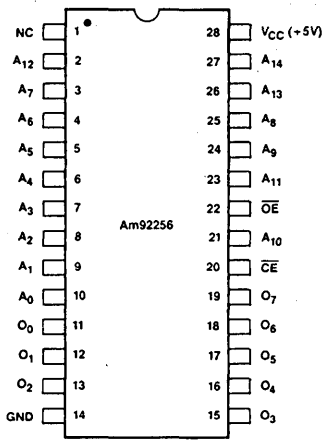
H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

| Access Times | 450ns | 300ns | 250ns |
|---|---|---|---|
| Part Number | Am92256B | Am92256C | Am92256D |

03180B

## CONNECTION DIAGRAM
### Top View




CD000010

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am92256 B P C**

- **C** — Temperature
  - C – Commercial (0°C to +70°C)
- **P** — Package
  - D – 28-pin CERDIP
  - P – 28-pin plastic DIP
- **B** — Speed Select
  - B – 450ns
  - C – 300ns
  - D – 250ns
- **Am92256** — Device Type
  - 32k x 8 ROM

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## ROM CODE DATA

AMD's preferred method of receiving ROM code data is in EPROM. Two identically programmed EPROMs should be submitted for code verification purposes. AMD will read one of the EPROMs and store contents in a floppy disk. The contents of the second EPROM are compared with the stored data for consistency. The second EPROM is erased and then reprogrammed and submitted to the customer for verification of the ROM code, along with code listing. Unless otherwise requested, AMD will not proceed until production is authorized by means of a signed MOS ROM verification form (submitted with code verification data).

The following EPROMs should be used for submitting ROM code data:

| ROM | | EPROM | |
|---|---|---|---|
| | | Preferred | Optional |
| Am9218 | 2K x 8 | 2716 | 2716 |
| Am9232/33 | 4K x 8 | 2732 | 2532/2-2716 |
| Am9264 | 8K x 8 | 2764 | 4-2716/2-2732 |
| Am9265 | 8k x 8 | 2764 | 4-2176/2-2732 |
| Am9128 | 16K x 8 | 27128 | 2-2764 |
| Am92256 | 32K x 8 | 2-27128 | 42764 |

If more than one EPROM is used to specify a ROM pattern, the upper and lower address locations must be clearly specified.

### CARD FORMAT

If card decks are preferred as code inputs, the following industry standard formats are acceptable:

AMD HEXADECIMAL (PREFERRED)
INTEL HEXADECIMAL
INTEL BPNF
OTOROLA HEXADECIMAL
EA OCTAL
GI BINARY

### PAPER TAPE FORMAT

If punched paper tape is preferred as code input, most industry standard formats are acceptable. Verify with factory before submittal.

### CHIP SELECT INFORMATION

Regardless of the method of submitting ROM code data, the chip select information must be specified at the time of customer input data. EPROMs do not have programmable chip selects and, therefore, cannot provide the required chip select information.

### KEY POINTS

- Supply 2 sets of identically programmed EPROMs.
- Specify customer part number and appropriate AMD part number.
- Supply marking information.
- Identify upper and lower address location when more than one EPROM is used.
- Cover EPROM window with opaque material to prevent bit loss.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... +7.0V
DC Signal Voltage applied to outputs ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to +7.0V
Power Dissipation ..... 1.0W

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Temperature ..... 0°C to +70°C

Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH} = -400\mu A$ | | 2.4 | | | Volts |
| $V_{OL}$ | Output LOW Voltage | $I_{OL} = 3.2mA$ | | | | 0.4 | Volts |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ +1.0V | Volts |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | | 0.8 | Volts |
| $I_{LI}$ | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $GND \leq V_O \leq V_{CC}$ Chip Disabled | +70°C | | | 10 | μA |
| | | | | | | | |
| $I_{CC1}$ | $V_{CC}$ Standby Current | | 0°C | | | 30 | mA |
| | | | | | | | |
| $I_{CC2}$ | $V_{CC}$ Operating Current | | 0°C | | | 120 | mA |
| | | | | | | | |
| $C_I$ | Input Capacitance | $T_A = 25°C$, f = 1.0MHz All pins at 0V | | | | 7.0 | pF |
| $C_O$ | Output Capacitance | | | | | 7.0 | pF |

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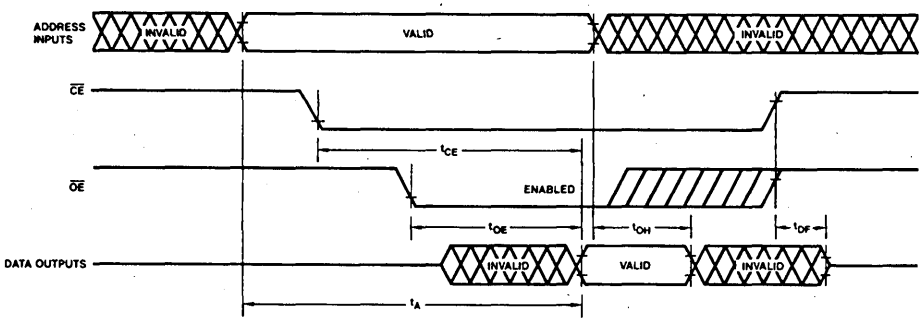
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | Am92256B Min | Am92256B Max | Am92256C Min | Am92256C Max | Am92256D Min | Am92256D Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_A$ | Address to Output Access Time | tr = tf = 10ns Output Load: One Standard TTL Gate Plus 100pF (Note 1) | | 450 | | 300 | | 250 | ns |
| 2 | $t_{OE}$ | Output Enable to Output ON Delay | | | 150 | | 120 | | 100 | ns |
| 3 | $t_{CE}$ | $\overline{CE}$ to Output ON Delay | | | 450 | | 300 | | 250 | ns |
| 4 | $t_{OH}$ | Previous Read Data Valid with Respect to Address Change | | 20 | | 20 | | 20 | | ns |
| 5 | $t_{DF}$ | Chip Select to Output OFF Delay | | | 120 | | 100 | | 80 | ns |

Notes:
1. Timing reference levels: High = 2.0V Low = 0.8V.
2. $t_{DF}$ is the worst case OFF delay. If $\overline{OE}$ occurs before $\overline{CE}$ is disabled, then $t_{DF}$ is referenced to $\overline{OE}$ only. If $\overline{OE}$, and $\overline{CE}$ are disabled simultaneously, then $t_{DF}$ is referenced to both.

## SWITCHING WAVEFORMS




WF000010

# MOS UV Erasable Programmable ROM (EPROM) Index

# Am1702A

256 x 8-Bit Programmable ROM

## DISTINCTIVE CHARACTERISTICS

- Access times down to 550 nanoseconds
- 100% tested for programmability
- Inputs and outputs TTL compatible
- Three-state output — wired-OR capability
- Typical programming time of less than 2 minutes/device
- Clocked VGG mode for lower power dissipation

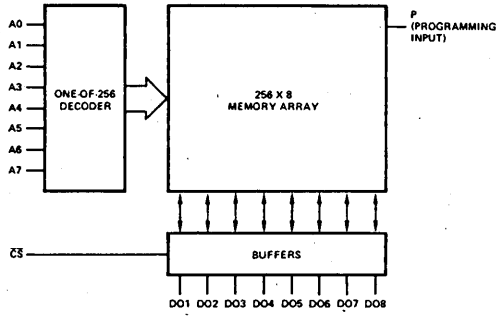
## GENERAL DESCRIPTION

The Am1702A is a 2048-bit electrically programmable ultraviolet light erasable Read Only Memory. It is organized as 256 by 8 bits. It is packaged in a 24 pin dual in-line hermetic cerdip package with a foggy lid.

The transparent lid allows the user to erase any previously stored bit pattern by exposing the die to an ultraviolet (UV) light source. Initially, and after each erasure, all 2048 bits are in the zero state (output low). The data is selectively written into specified address locations by writing in ones.

A low power version, the Am1702AL, is available which permits the VGG input to be clocked for lower average power dissipation.

## BLOCK DIAGRAM




BD000180

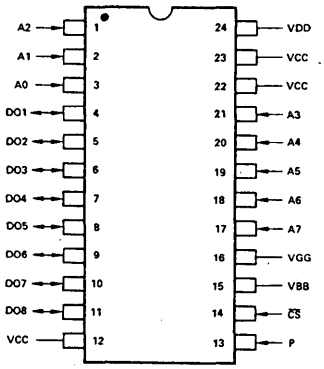
## PRODUCT SELECTOR GUIDE

| Access Time (ns) | | | Clocked VGG |
|---|---|---|---|
| 1000 | 650 | 550 | |
| Am1702A | Am1702A-2 | Am1702A-1 | No |
| Am1702AL | Am1702AL-2 | Am1702AL-1 | Yes |
| Am9702AHDL | Am9702A-2HDL | Am9702A-1HDL | No |
| Am90702ALHDL | Am9702AL-2HDL | Am9702AL-1HDL | Yes |



04989A

## CONNECTION DIAGRAM
### Top View




CD000250

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am1702A L- 2 D C**

- C – Temperature Range
  - C – Commercial (0°C to +70°C)
  - L – Extended (–55°C to +100°C)
- D – Package
  - D – 24-pin CERDIP
- 2 – Speed Select
  - See Product Selector Guide
- L – Clocked VGG
  - See Product Selector Guide
- Am1702A – Device Type
  - 256 x 8 ROM

| Valid Combinations | | |
|---|---|---|
| | | Clocked VGG |
| Am1702A<br>Am1702A-2<br>Am1702A-1 | DC,<br>DC,<br>DC | NO |
| Am1702AL<br>Am1702AL-2<br>Am1702AL-1 | DL,<br>DL,<br>DL | YES |
| Am9702AHDL<br>Am9702A-2HDL<br>Am9702AL-1HDL | DL,<br>DL,<br>DL | NO |
| Am90702AL-HDL<br>Am90702AL-2HDL<br>Am90702AL-1HDL | DL | YES |

### PROGRAMMING THE Am1702A

Each storage node in the Am1702A consists of an MOS transistor whose gate is not connected to any circuit element. The transistors are all normally off, making all outputs LOW in an unprogrammed device. A bit is programmed to a HIGH by applying a large negative voltage to the MOS transistor; electrons tunnel through the gate insulation onto the gate itself. When the programming voltage is removed, a charge is left on the gate which holds the transistor on. Since the gate is completely isolated, there is no path by which the charge can escape, except for random high energy electrons which might retunnel through the gate insulation. Under ordinary conditions retunneling is not significant. The application of high energy to the chip through X-rays or UV light (via the quartz window) raises energy levels so that the charge can escape from the gate region, erasing the program and restoring the device to all LOW.

In order to program a specified byte, all 8 address lines must be in the binary complement of the address desired when pulsed VDD and VGG move to their negative level. The complemented address must be stable for at least tACW before VDD and VGG make their negative transitions. The voltage swing of the address lines during programming is between −47V ±1V and 0V. The addresses must then make a transition to the true state at least tATW before the program pulse is applied. For good data retention, the addresses should be programmed in sequence from 0 to 255, a minimum of 32 times. DO1 through DO8 are used as the data inputs to program the desired pattern. A low level at the data input (−47V ±1V) will program the selected bit to 1 and a high level (0V) will program it to a 0. All 8 bits addressed are programmed simultaneously.

Programming Boards are available for the Data I/O automatic programmer (part number 1010/1011), for the Spectrum Dynamics programmer (part number 434-549), and for the Pro-Log programmer (part number PM9001).

### ERASING THE Am1702A

The Am1702A may be erased (restored to all LOW's) by exposing the die to ultraviolet light from a high intensity source. The recommended dosage is 6 W-sec/cm$^2$ at a wavelength of 2537 Å. The Ultraviolet Products, Inc., models UVS-54 or S-52 can erase the Am1702A in about 15 minutes, with the devices held one inch from the lamp. (Caution should be used when Am1702A's are inspected under fluorescent lamps after being programmed, as some fluorescent lamps may emit sufficient UV to erase or "soften" the PROM.)

### CAUTION

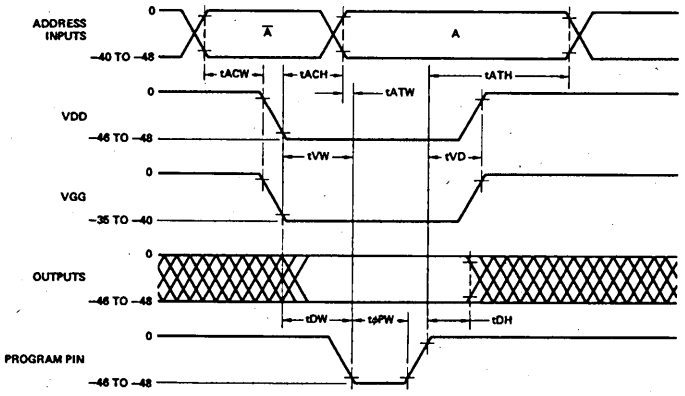
Ultraviolet radiation is invisible and can damage human eyes. Precautions should be taken to avoid exposure to direct or reflected ultraviolet radiation. It will often be convenient to fully enclose the ultraviolet source and the EROMs being erased to prevent accidental exposure.

Ultraviolet lamps can also ionize oxygen and create ozone which is harmful to humans. Erasing should be carried out in a well ventilated area in order to minimize the concentration of ozone.

## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI1P}$ | Input Current, Address and Data | $V_I = -48V$ | | | 10 | mA |
| $I_{LI2P}$ | Input Current, Program and $V_{GG}$ Inputs | $V_I = -48V$ | | | 10 | mA |
| $I_{BB}$ | $V_{BB}$ Current | | | 0.05 | | mA |
| $I_{DDP}$ | $I_{DD}$ Current During Programming Pulse | $V_{DD} = V_{Prog} = -48V$, $V_{GG} = -35V$ | | 200 | Note 8 | mA |
| $V_{IHP}$ | Input HIGH Voltage | | | | 0.3 | Volts |
| $V_{IL1P}$ | Voltage Applied to Output to Program a HIGH | | −46 | | −48 | Volts |
| $V_{IL2P}$ | Input LOW Level on Address Inputs | | −40 | | −48 | Volts |
| $V_{IL3P}$ | Voltage Applied to $V_{DD}$ and Program Inputs | | −46 | | −48 | Volts |
| $V_{IL4P}$ | Voltage Applied to $V_{GG}$ Input | | −35 | | −40 | Volts |
| $t_{\phi PW}$ | Programming Pulse Width | $V_{GG} = -35V$, $V_{DD} = V_{Prog} = -48V$ | | | 3.0 | ms |
| $t_{DW}$ | Data Set-up Time | | 25 | | | μs |
| $t_{DH}$ | Data Hold Time | | 10 | | | μs |
| $t_{VW}$ | $V_{GG}$ and $V_{DD}$ Set-up Time | | 100 | | | μs |
| $t_{VD}$ | $V_{GG}$ and $V_{DD}$ Hold Time | | 10 | | 100 | μs |
| $t_{ACW}$ | Address Set-up Time (Complement) | | 25 | | | μs |
| $t_{ACH}$ | Address Hold Time (Complement) | | 25 | | | μs |
| $t_{ATW}$ | Address Set-up Time (True) | | 10 | | | μs |
| $t_{ATH}$ | Address Hold Time (True) | | 10 | | | μs |
| | Duty Cycle | | | | 20 | % |

## PROGRAMMING WAVEFORMS




WF000270

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +85°C
Input and Supply Voltages
Operating ..... $V_{CC}$ −20V to $V_{CC}$ +0.5V
Programming ..... −50V
Power Dissipation ..... 1.0W

*The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.*

## OPERATING RANGES

Temperature
1702 Devices ..... 0°C to +70°C
9702 Devices ..... −55°C to +85°C

Supply Voltages
$V_{CC}$, $V_{BB}$ ..... +4.75V to +5.25V
$V_{DD}$, $V_{GG}$ ..... −8.55V to +9.45V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

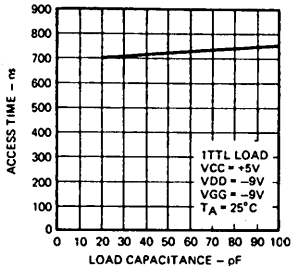
| Symbol | Parameter | Test Conditions | Am1702A Am9702A Min | Typ | Max | Am1702AL Am9702AL Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|---|---|
| $I_{CF1}$ | Output Clamp Current | $T_A$ = 0°C, $V_O$ = −1.0V | | 8 | 14 | | 5.5 | 8 | mA |
| $I_{CF2}$ | Output Clamp Current | $T_A$ = 25°C, $V_O$ = −1.0V | | | 13 | | 5 | 7 | mA |
| $I_{DD0}$ | $V_{DD}$ Current (Note 4) | $V_{GG}$ = $V_{CC}$, $I_{OL}$ = 0mA, $\overline{CS}$ = $V_{CC}$ −2.0, $T_A$ = 25°C | | | | | 7 | 10 | mA |
| $I_{DD1}$ | | $I_{OL}$ = 0mA, $\overline{CS}$ = $V_{CC}$ −2.0, $T_A$ = 25°C | | 35 | 50 | | 35 | 50 | mA |
| $I_{DD2}$ | | $I_{OL}$ = 0mA, $\overline{CS}$ = 0, $T_A$ = 25°C | | 32 | 46 | | 32 | 46 | mA |
| $I_{DD3}$ | | $I_{OL}$ = 0mA, $\overline{CS}$ = $V_{CC}$ −2.0, $T_A$ = 0°C | | 38 | 60 | | 38 | 60 | mA |
| $I_{GG}$ | $V_{GG}$ Current | | | | 1.0 | | | 1.0 | µA |
| $I_{LI}$ | Input Leakage Current | $V_I$ = 0V | | | 1.0 | | | 1.0 | µA |
| $I_{LO}$ | Output Leakage Current | $\overline{CS}$ = $V_{CC}$ −2.0, $V_O$ = 0V | | | 1.0 | | | 1.0 | µA |
| $I_{OH}$ | Output Source Current | $V_O$ = 0V | −2.0 | | | −2.0 | | | mA |
| $I_{OL}$ | Output Sink Current | $V_O$ = 0.45V | 1.6 | 4 | | 2.0 | | | mA |
| $V_{IH}$ | Input HIGH Level | | $V_{CC}$ −2.0 | | $V_{CC}$ +0.3 | $V_{CC}$ −2.0 | | $V_{CC}$ +0.3 | Volts |
| $V_{IL}$ | Input LOW Level | | −1.0 | | 0.65 | −1.0 | | 0.65 | Volts |
| $V_{OH}$ | Output HIGH Level | $I_{OH}$ = −200µA | 3.5 | 4.5 | | 3.5 | 4.5 | | Volts |
| $V_{OL}$ | Output LOW Level | $I_{OL}$ 1.6mA | | −3.0 | 0.45 | | | | Volts |
| | | $I_{OL}$ 2.0mA | | | | | | 0.4 | |
| $C_I$ | Input Capacitance | $T_A$ = 25°C, All unused pins are at $V_{CC}$ | | | | | 8 | 15 | pF |
| $C_O$ | Output Capacitance | | | | | | 10 | 15 | pF |
| $C_{VGG}$ | $V_{GG}$ Capacitance | | | | | | | 30 | pF |

Notes:

1. During read operations VGG may be clocked high to reduce power consumption. This involves swinging VGG up to VCC. See "Clocked VGG Operation". This mode is possible only with the Am1702AL.
2. During Read operations:
   Pins 12, 13, 15, 22, 23 = +5.0V ±5%
   Pins 16, 24 = −9.0V ±5%
   During Program operations:
   $t_A$ = 25°C
   Pins 12, 22, 23 = 0V
   Pins 13, 24 are pulsed low from 0V to −47V ±1V
   Pin 15 = +12.0V ±10%
   Pin 16 is pulsed low from 0V to −37.5V ±2.5V
3. Typical values are for $T_A$ = 25°C, nominal supply voltages and nominal processing parameters.
4. IDD may be reduced by pulsing the VGG supply between VCC and −9V. VDD current will be directly proportional to the VGG duty cycle. The data outputs will be unaffected by address or chip select changes while VGG is at VCC. For this option specify AM1702AL.
5. VIL = 0V, VIH = 4.0V, tr = tf ⩽ 50ns, Load = 1 TTL gate.
6. The output will remain valid for tOHC after the VGG pin is raised to VCC, even if address change occurs.
7. These parameters are guaranteed by design and are not 100% tested.
8. Do not allow IDD to exceed 300mA for more than 100µsec.

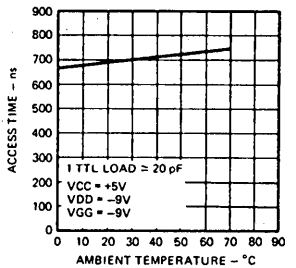
## DC OPERATING CHARACTERISTICS

### Access Time Versus Load Capacitance



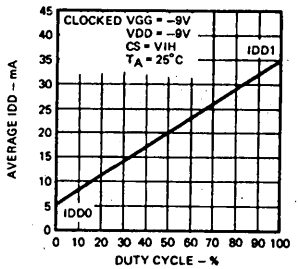

OP000280

### Access Time Versus Temperature



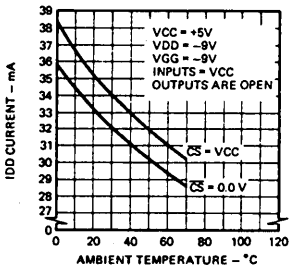

OP000290

### Average Current Versus Duty Cycle for Clocked VGG



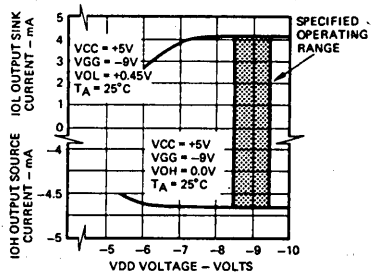

OP000300

### IDD Current Versus Temperature



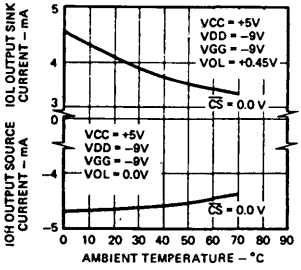

OP000310

### Output Current Versus VDD Supply Voltage



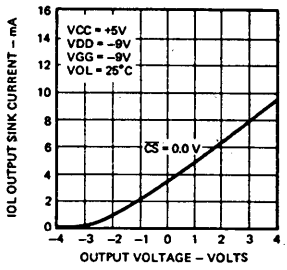

OP000320

### Output Current Versus Temperature




OP000330

### Output Sink Current Versus Output Voltage



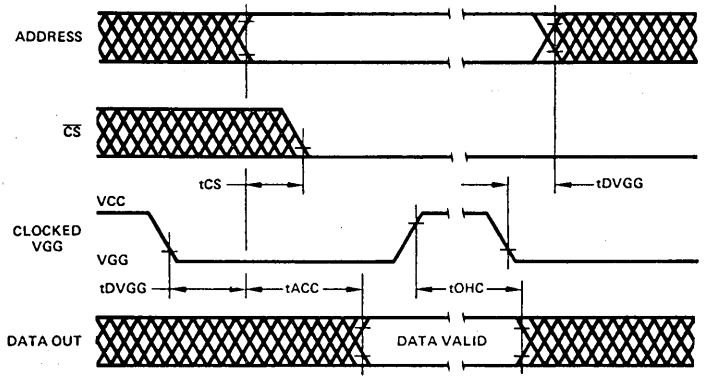

OP000340

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Am1702A-1 Am1702AL-1 Am9702A-1 Am9702AL-1 | | Am1702A-2 Am1702AL-2 Am9702A-2 Am9702AL-2 | | Am1702A Am1702AL Am9702A Am9702AL | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | $t_{ACC}$ | Address to Output Access Time | | 550 | | 650 | | 1000 | ns |
| 2 | $t_{CO}$ | Output Delay from $\overline{CS}$ | | 450 | | 350 | | 900 | ns |
| 3 | $t_{\overline{CS}}$ | Chip Select Delay | | 100 | | 300 | | 100 | ns |
| 4 | $t_{DVGG}$ | Set-up Time, $V_{GG}$ | 0.3 | | 0.3 | | 0.4 | | μs |
| 5 | $t_{OD}$ | Output Deselect | | 300 | | 300 | | 300 | ns |
| 6 | $t_{DH}$ | Previous Read Data Valid | | 100 | | 100 | | 100 | ns |
| 7 | $t_{OHC}$ | Data Out Valid from $V_{GG}$ (Note 6) | | 5.0 | | 5.0 | | 5.0 | μs |
| 8 | freq. | Repetition Rate | | 1.8 | | 1.6 | | 1.0 | MHz |

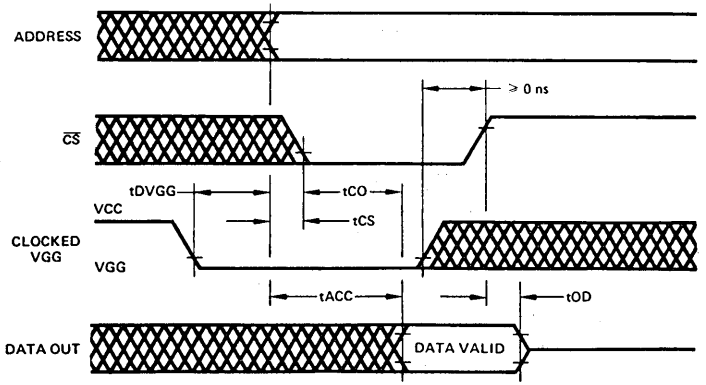
## SWITCHING WAVEFORMS

### READ OPERATION (Note 2)




WF000440

### DESELECTION




WF000450

Note 1: CLOCKED VGG OPERATION

The VGG input may be clocked between +5V (VCC) and −9V to save power. To read the data, the chip select ($\overline{CS}$) must be low ($\leq$ VIL) and the VGG level must be lowered to −9V at least tDVGG prior to the address selection. Once the data has appeared at the output and the access time has elapsed, VGG may be raised to +5V. The data output will remain stable for tOHC. To deselect the chip, $\overline{CS}$ is raised to $\geq$ VIH, and the output will go the high impedance state after tOD. The chip will be deselected when $\overline{CS}$ is raised to VIH whether the VGG is at +5V or at −9V.

# Am2716/Am9716

2048 x 8-Bit UV Erasable PROM

## DISTINCTIVE CHARACTERISTICS

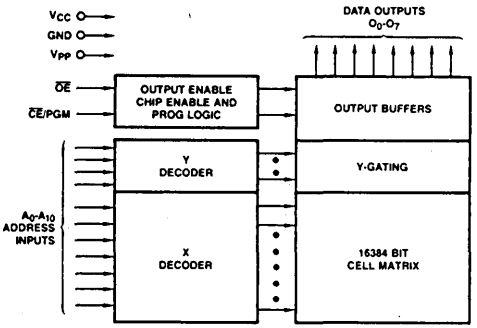
- Direct replacement for Intel 2716
- Interchangeable with Am9218 — 16K ROM
- Single +5V power supply
- Low power dissipation
  - 525mW active
  - 132mW standby
- Fully static operation — no clocks
- Three-state outputs

## GENERAL DESCRIPTION

The Am2716/Am9716 is a 16384-bit ultraviolet erasable and programmable read-only memory. It is organized as 2048 words by 8 bits per word, operates from a single +5V supply, has a static standby mode and features fast single address location programming.

Because the Am2716/Am9716 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 100 seconds.

## BLOCK DIAGRAM




BD000190

## MODE SELECT TABLE

| $\overline{CE}$/PGM (18) | $\overline{OE}$ (20) | $V_{PP}$ (21) | Outputs (9–11, 13–17) | Mode |
|---|---|---|---|---|
| L | L | $V_{CC}$ | $D_{OUT}$ | Read |
| H | X | $V_{CC}$ | High Z | Standby |
| Pulsed L to H | H | $V_{PP}$ | $D_{IN}$ | Program |
| L | L | $V_{PP}$ | $D_{OUT}$ | Program Verify |
| L | H | $V_{PP}$ | High Z | Program Inhibit |

H = HIGH
L = LOW
X = Don't Care

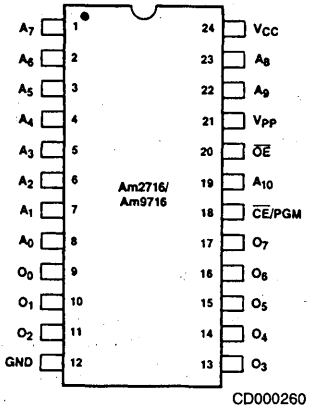
## PRODUCT SELECTOR GUIDE

| Access Time | 300ns | 350ns | 390ns | 450ns |
|---|---|---|---|---|
| Part Numbers | Am9716 | Am2716-1 | Am2716-2 | Am2716 |

00913B

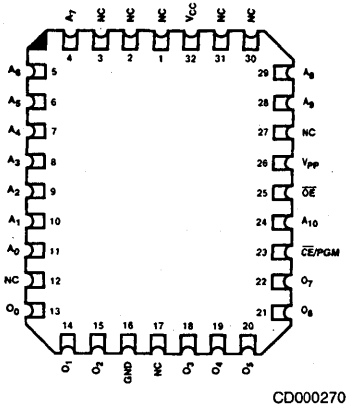
## CONNECTION DIAGRAM
### Top View

**DIP**




CD000260

**Chip-Pak™ L-32-2**




CD000270

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am2716-1 L I**

- I — Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- L — Package
  - D – 24-pin CERDIP
  - L – 32-pin leadless chip carrier
- 1 — Speed Select
  - See product selector guide
- Am2716 — Device Type
  - 2k x 8 EPROM

| Valid Combinations | |
|---|---|
| Am9716 | DC, LC |
| Am2716 | DC, LC, DI, LI, DL, LL, DM, LM |
| Am2716-1 | DC, LC, DI, LI, DL, LL |
| Am2716-2 | DC, LC |

6





00913B

## ERASING THE Am2716/Am9716

In order to clear all locations of their programmed contents, it is necessary to expose the Am2716/Am9716 to an ultraviolet light source. A dosage of 15 Wseconds/cm$^2$ is required to completely erase an Am2716/Am9716. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å)] with intensity of 12000 uW/cm$^2$ for 15 to 20 minutes. The Am2716/Am9716 should be about one inch from the sourse and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2716/Am9716, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to florescent light and sunlight will eventually erase the Am2716/Am9716, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

## PROGRAMMING THE Am2716/Am9716

Upon delivery, or after each erasure the Am2716/Am9716 has all 16384 bits in the "1," or high state. "0s" are loaded into the Am2716/Am4716 through the procedure of programming.

The programming mode is entered when +25V is applied to the $V_{PP}$ pin and when $\overline{OE}$ is at $V_{IH}$. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL high level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC level to the $\overline{CE}$/PGM input is prohibited when programming.

## READ MODE

The Am2716/Am9716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$) for all devices. Data is available at the outputs 120ns or 150ns ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The Am2716/Am9716 has a standby mode which reduces the active power dissipation by 75%, from 525mW to 132mW (values for 0 to +70°C). The Am2716/Am9716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

## OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAM INHIBIT

Programming of multiple Am2716/Am9716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2716/Am9716s may be common. A TTL level program pulse applied to an Am2716/Am9716's $\overline{CE}$/PGM input with $V_{PP}$ at 25V will program that Am2716/Am9716. A low level $\overline{CE}$/PGM input inhibits the other Am2716/Am9716 from being programmed.

## PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with $V_{PP}$ at 25V. Except during programming and program verify, $V_{PP}$ must be at $V_{CC}$.

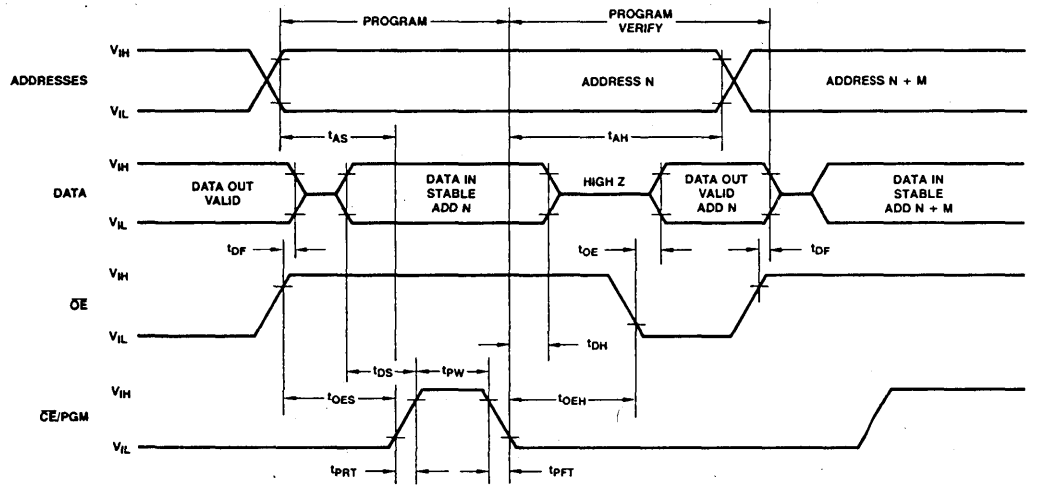
## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current | $V_{IN}$ = 5.25/0.45V | | 10 | μA |
| $I_{PP1}$ | $V_{PP}$ Supply Current | $\overline{CE}/PGM = V_{IL}$ | | 5 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current During Programming Pulse | $\overline{CE}/PGM = V_{IH}$ | | 30 | mA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | 100 | mA |
| $V_{IL}$ | Input Low Level | | −0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$ +1 | Volts |
| $t_{AS}$ | Address Set-up time | Input $t_R$ and $t_F$ (10% to 90%) = 20ns<br>Input Signal Levels = 0.8 to 2.2V<br>Input Timing Reference Level = 1V and 2V<br>Output Timing Reference Level = 0.8V and 2V | 2 | | μs |
| $t_{OES}$ | Output Enable Set-up Time | | 2 | | μs |
| $t_{DS}$ | Data Set-up Time | | 2 | | μs |
| $t_{AH}$ | Address Hold Time | | 2 | | μs |
| $t_{OEH}$ | Output Enable Hold Time | | 2 | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | μs |
| $t_{DF}$ | Output Disable to Output Float Delay($\overline{CE}$/PGM = $V_{IL}$) | | 0 | 120 | ns |
| $t_{OE}$ | Output Enable to Output Delay ($\overline{CE}/PGM = V_{IL}$) | | | 120 | ns |
| $t_{PW}$ | Program Pulse Width | | 45 | 55 | ms |
| $t_{PRT}$ | Program Pulse Rise Time | | 5 | | ns |
| $t_{PFT}$ | Program Pulse Fall Time | | 5 | | ns |

Notes:

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into the socket when $V_{PP}$ = 25 volts is applied. Also, during $\overline{OE} = \overline{CE}/PGM = V_{IH}$, $V_{PP}$ must not be switched from 5 volts to 25 volts or vice versa.

## PROGRAMMING WAVEFORMS

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## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −65°C to +135°C
Voltage on All Inputs/
Outputs (except $V_{PP}$ ..... +6V to −0.3V
Voltage on $V_{PP}$ during
programming ..... +26.5V to −0.3V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltages (2716, 2716-2) ..... +4.75V to +5.25V
(9716, 2716-1) ..... +4.5V to +5.5V

Industrial (I) Devices
Temperature ..... −40°C to +85°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{L1}$ | Input Load Current | $V_{IN} = V_{CC}$ Max | | | | 10 | μA |
| | | $V_{IN} = 0V$ | | | | 10 | |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{CC}$ Max | | | | 10 | |
| | | $V_{OUT} = 0V$ | | | | 10 | |
| $I_{PP}$ | Programming Current | $V_{PP} = V_{CC}$ Max | | | | 5 | mA |
| $I_{CCSB}$ | Standby Supply Current | $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ | C devices | | | 25 | |
| | | | All others | | | 30 | |
| $I_{CCOP}$ | Operating Supply Current | $\overline{OE} = \overline{CE} = V_{IL}$ | C devices | | | 100 | |
| | | | I devices | | | 110 | |
| | | | L, M devices | | | 115 | |
| $V_{IL}$ | Input Low Voltage | | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ + 1.0V | |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 2.1$ mA, $V_{CC}$ = Min | | | | 0.45 | |
| $V_{OH}$ | Output High Voltage | $I_{OH} = -400\mu A$, $V_{CC}$ = Min | | 2.4 | | | |
| $C_{IN}$ | Input Capacitance | $V_{IN} = 0V$ | | | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_O = 0V$ | | | 8 | 12 | |



00913B

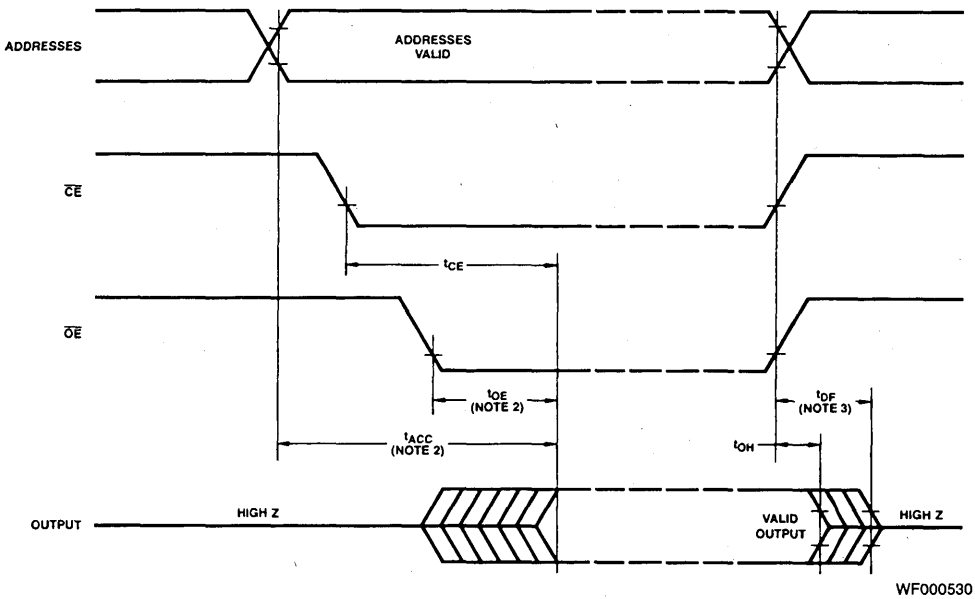
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions (Note 3) | Min Values | Maximum Values | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | All Types | 9716 DC | 2716-1 DC | 2716-2 DC | 2716 DC | 2716-1 DI/DL | 2716 DI/DL/DM | |
| 1 | $t_{ACC}$ | Address to Output Delay | $\overline{CE} = \overline{OE} = V_{IL}$ | | 300 | 350 | 390 | 450 | 350 | 450 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | $\overline{OE} = V_{IL}$ | | 300 | 350 | 390 | 450 | 350 | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | $\overline{CE} = V_{IL}$ | | 120 | 120 | 120 | 120 | 150 | 150 | ns |
| 4 | $t_{DF}$ | Output Enable High to Output Float | $\overline{CE} = V_{IL}$ | 0 | 100 | 100 | 100 | 100 | 130 | 130 | ns |
| 5 | $t_{OH}$ | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | | | | | ns |

Notes:

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply current would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. Other Test Conditions:
   a) Output Load: 1 TTL gate and $C_L = 100pF$
   b) Input Rise and Fall Times: $\leq 20ns$
   c) Input Pulse Levels: 0.8 to 2.2V
   d) Timing Measurement Reference Level:
      Inputs: 1V and 2V
      Outputs: 0.8V and 2V
4. This parameter is only sampled and is not 100% tested.

## SWITCHING WAVEFORMS

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Notes: 1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
3. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

6

# Am2732

4096 x 8-Bit UV Erasable PROM

Military, Industrial and Commercial

## DISTINCTIVE CHARACTERISTICS

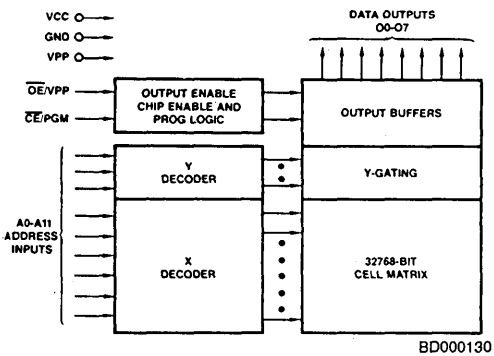
- Direct replacement for Intel 2732
- Pin compatible with Am9233 — 32K ROM
- Fast access time — 350ns and 450ns
- Low power dissipation
- Three-state outputs
- TTL compatible inputs/outputs

## GENERAL DESCRIPTION

The Am2732 is a 32768-bit ultraviolet erasable and programmable read-only memory. It is organized as 4096 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2732 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 200 seconds.

## BLOCK DIAGRAM

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## MODE SELECT TABLE

| $\overline{CE}$/PGM (18) | $\overline{OE}$/$V_{PP}$ (20) | Outputs (9–11, 13–17) | Mode |
|---|---|---|---|
| L | L | $D_{OUT}$ | Read |
| H | X | High Z | Standby |
| L | $V_{PP}$ | $D_{IN}$ | Program |
| L | L | $D_{OUT}$ | Program Verify |
| H | $V_{PP}$ | High Z | Program Inhibit |

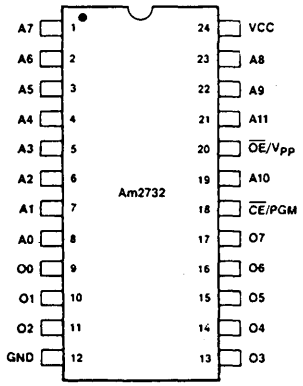
H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

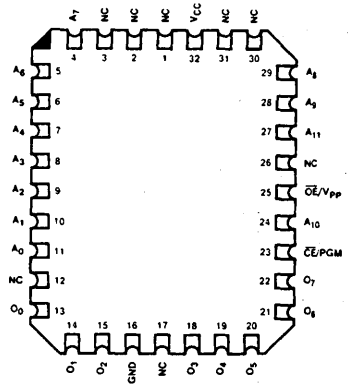
| Access Time | 450ns | 350ns |
|---|---|---|
| Part Numbers | Am2732 | Am2732-1 |

00912C

## CONNECTION DIAGRAM
### Top View




CD000190




CD000200

## ORDERING INFORMATION

**Am2732-1 D C**

- Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 24-pin CERDIP
  - L – 32-pin leadless chip carrier
- Speed Select
  - –1 option indicates access time of 350ns
- Device Type
  - 4k x 8 EPROM

| Valid Combinations | |
|---|---|
| Am2732-1 | DC, LC |
| Am2732 | DC, LC, DI, LI, DL, LL, DM, LM |

## ERASING THE Am2732

In order to clear all locations of their programmed contents, it is necessary to expose the Am2732 to an ultraviolet light source. A dosage of 15 Wseconds/$cm^2$ is required to completely erase an Am2732. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000$\mu$W/$cm^2$ for 15 to 20 minutes. The Am2732 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2732, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am2732, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

## PROGRAMMING THE Am2732

Upon delivery, or after each erasure the Am2732 has all 32768 bits in the "1", or high state. "0"s are loaded into the Am2732 through the procedure of programming.

The programming mode is entered when +25V is applied to the $\overline{OE}$/VPP pin. A 0.1$\mu$F capacitor must be placed across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL high level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{CE}$/PGM input is prohibited when programming.

## READ MODE

The Am2732 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$/VPP) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs 120ns ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The Am2732 has a standby mode which reduces the active power dissipation by 80%, from 787mW to 157mW (values for 0°C to + 70°C). The Am2732 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

## OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAM INHIBIT

Programming of multiple Am2732s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2732s may be common. A TTL level program pulse applied to an Am2732's $\overline{CE}$/PGM input with VPP at 25V will program that Am2732. A high level $\overline{CE}$/PGM input inhibits the other Am2732 from being programmed.

## PROGRAM VERIFY

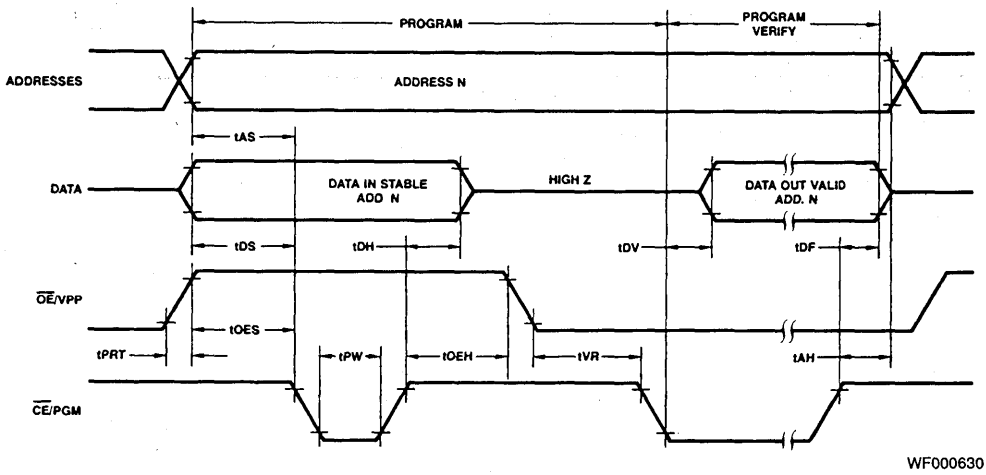
A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$/VPP and $\overline{CE}$ at VIL. Data should be verified $t_{DV}$ after the falling edge of $\overline{CE}$.

## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{L1}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | μA |
| $V_{OL}$ | Output Low Voltage During Verify | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH} = -400\mu A$ | 2.4 | | | Volts |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | | 150 | mA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | | 0.8 | Volts |
| $V_{IH}$ | Input High Level (All Inputs Except $\overline{OE}/V_{PP}$) | | 2.0 | | $V_{CC}+1$ | Volts |
| $I_{PP}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$ | | | 30 | mA |
| $t_{AS}$ | Address Set-up Time | Input $t_R$ and $t_F$(10% to 90%) = 20ns<br>Input Signal Levels = 0.8 to 2.2V<br>Timing Measurement Reference Level:<br>Inputs: 1V and 2V<br>Outputs: 0.8V and 2V | 2 | | | μs |
| $t_{OES}$ | Output Enable Set-up Time | | 2 | | | μs |
| $t_{DS}$ | Data Set-up Time | | 2 | | | μs |
| $t_{AH}$ | Address Hold Time | | 2 | | | μs |
| $t_{OEH}$ | Output Enable Hold Time | | 2 | | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | | μs |
| $t_{DF}$ | Chip Enable to Output Float Delay | | 0 | | 120 | ns |
| $t_{DV}$ | Data Valid from $\overline{CE}$ ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$) | | - | | 1 | ns |
| $t_{PW}$ | Program Pulse Width | | 45 | | 55 | ms |
| $t_{PRT}$ | Program Pulse Rise Time | | 50 | | - | ns |
| $t_{VR}$ | $V_{PP}$ Recovery Time | | 2 | | - | ns |

Note: 1. When programming the Am2732, a 0.1μF capacitor is required across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device.

## PROGRAMMING WAVEFORMS

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00912C

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −65°C to +135°C
Voltage on All Inputs/
Outputs (except $V_{PP}$) ..... +6V to −0.3V
Voltage on $V_{PP}$ during
programming ..... +26.5V to −0.3V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage (2732, 2732-2) ..... +4.75V to +5.25V
(2732, 2732-1) ..... +4.5V to +5.5V

Industrial (I) Devices
Temperature ..... −40°C to +85°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

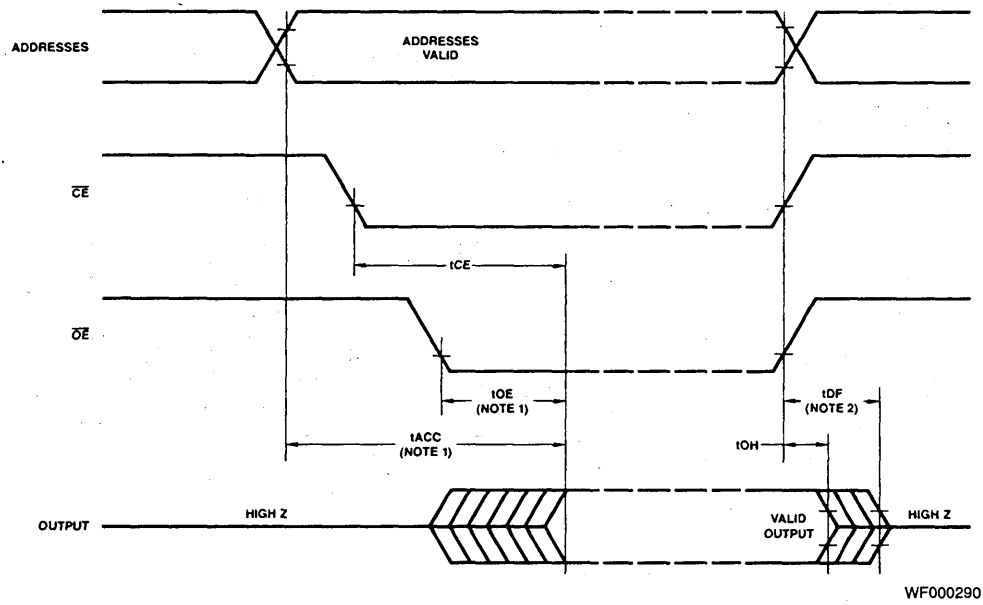
| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{CC}$ Max | | | | 10 | µA |
| | | $V_{IN} = 0$ | | | | 10 | |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{CC}$ Max | | | | 10 | |
| | | $V_{OUT} = 0V$ | | | | 10 | |
| $I_{CCSB}$ | Standby Supply Current | $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ | C devices | | | 30 | mA |
| | | | I devices | | | 40 | |
| | | | L, M devices | | | 45 | |
| $I_{CCOP}$ | Operating Supply Current | $\overline{OE} = \overline{CE} = V_{IL}$ | C devices | | | 150 | |
| | | | I devices | | | 165 | |
| | | | L, M devices | | | 175 | |
| $V_{IL}$ | Input Low Voltage | | | −0.1 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$ +1.0V | |
| $V_{OL}$ | Output Low Voltage | $I_{OL} = 2.1$ mA | | | | 0.45 | |
| $V_{OH}$ | Output High Voltage | $I_{OH} = -400µA$ | | 2.4 | | | |
| $C_{IN1}$ | Input Capacitance | $V_{IN} = 0V$ (Note 1) | | | 4 | 6 | pF |
| $C_{IN2}$ | $\overline{OE}/V_{PP}$ Input capacitance | $V_{IN} = 0V$ (Note 1) | | | | 20 | |
| $C_{OUT}$ | Output Capacitance | $V_{OUT} = 0V$ (Note 1) | | | | 12 | |

Note 1. This parameter is only sampled and is not 100% tested.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | | 2732-1 DC Min | 2732-1 DC Max | 2732-2 DC Min | 2732-2 DC Max | 2732 DI 2732 DL 2732 DM Min | 2732 DI 2732 DL 2732 DM Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load = 1 TTL gate $C_L$ = 100pF $t_R$ and $t_F \leq$ 20ns Input pulse level: 0.8V to 2.2V Timing measurement and reference level: Inputs: 1V and 2V Outputs 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 350 | | 450 | | 450 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | | $\overline{OE} = V_{IL}$ | | 350 | | 450 | | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 120 | | 120 | | 150 | ns |
| 4 | $t_{DF}$ | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | 0 | 100 | 0 | 100 | 0 | 130 | ns |
| 5 | $t_{OL}$ | Address to Output hold | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | 0 | | 0 | | ns |

## SWITCHING WAVEFORMS (Note 1)

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Notes: 1. OE may be delayed up to 330ns after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

6

# Am2732A

4096 x 8-Bit UV Erasable and one-time programmable EPROMs

## DISTINCTIVE CHARACTERISTICS

- Fast access times — 200ns, 250ns, 300ns, 450ns
- New low-cost plastic package for applications not requiring reprogramming
- Low power dissipation
  - 525mW active, 130mW standby
- Three-state outputs
- Pin compatible with Am9233 — 32K-bit ROM
- Separate chip enable and output enable

## GENERAL DESCRIPTION

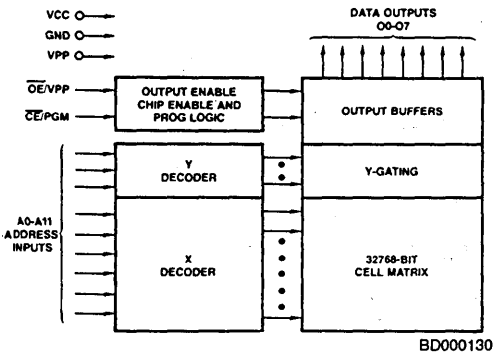
The Am2732A is a 32768-bit UV-light erasable and electrically programmable read-only memory, organized as 4096 words by 8-bits. The standard Am2732A offers an access time of 250ns, allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention in a multiple-bus microprocessor system, Am2732A offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random.

The part is available in an economical plastic package for applications which do not require reprogramming.

## BLOCK DIAGRAM

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## MODE SELECT TABLE

| $\overline{CE}$/PGM (18) | $\overline{OE}$/$V_{PP}$ (20) | Outputs (9–11, 13–17) | Mode |
|---|---|---|---|
| L | L | $D_{OUT}$ | Read |
| H | X | High Z | Standby |
| L | $V_{PP}$ | $D_{IN}$ | Program |
| L | L | $D_{OUT}$ | Program Verify |
| H | $V_{PP}$ | High Z | Program Inhibit |

H = HIGH
L = LOW
X = Don't Care

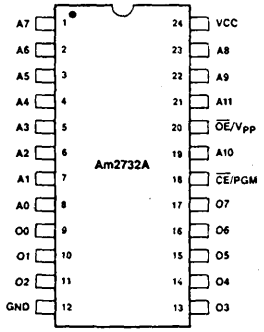
## PRODUCT SELECTOR GUIDE

| Access Times | 200ns | | 250ns | | 300ns | | 450ns | |
|---|---|---|---|---|---|---|---|---|
| Power Supply Tolerance | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% |
| Part Number | Am2732A-2 | Am2732A-20 | Am2732A-2 | Am2732A-25 | Am2732A-3 | Am2732A-30 | Am2732A-4 | Am2732A-45 |

04043C

## CONNECTION DIAGRAM
### Top View

**D-24-4**




CD000280

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am2732A-20 D L**

- L — Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 24-pin CERDIP w/window
  - P – 24-pin plastic DIP
- Am2732A-20 — Speed Select
  - See Product Select Guide

| Valid Combinations | |
|---|---|
| Am2732A | PC, DC, DI, DL |
| Am2732A-2<br>Am2732A-3<br>Am2732A-4<br>Am2732A-30 | DC, DI, DL |
| Am2732A-20<br>Am2732A-25<br>Am2732A-45 | DC, DI, DL, DM |

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### ERASING THE Am2732A (Does Not Apply to Am2732APC)

In order to erase the Am2732A, it is necessary to expose it to an ultraviolet light source. A dosage of 15 Wseconds/$cm^2$ is required for complete erasing. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537Å) with intensity of 12000$\mu$W/$cm^2$ for 15 to 20 minutes. The Am2732A should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2732A, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer the exposure to fluorescent light and sunlight will eventually erase the Am2732A, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

### PROGRAMMING THE Am2732A

Upon delivery, or after each erasure the Am2732A has all 32768 bits in the "1", or high state. "0"s are loaded into the Am2732A through the procedure of programming.

The programming mode is entered when +21V is applied to the $\overline{OE}$/VPP pin. A 0.1$\mu$F capacitor must be placed across $\overline{OE}$/VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins; 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. The only requirement is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{CE}$/PGM input is prohibited when programming.

### READ MODE

The Am2732A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$/VPP) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs 100ns ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

### STANDBY MODE

The Am2732A has a standby mode which reduces the active power dissipation by 75%, from 525 to 130mW (values for 0 to +70°C). The Am2732A is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### PROGRAM INHIBIT

Programming of multiple Am2732As in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2732A's may be common. A TTL level program pulse applied to an Am2732A's $\overline{CE}$/PGM input with VPP at 21V will program that Am2732A. A high-level $\overline{CE}$/PGM input inhibits the other Am2732A's from being programmed.

### PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$/VPP and $\overline{CE}$ at $V_{IL}$. Data should be verified $t_{DV}$ after the falling edge of $\overline{CE}$.

### SYSTEM APPLICATION FOR Am2732A

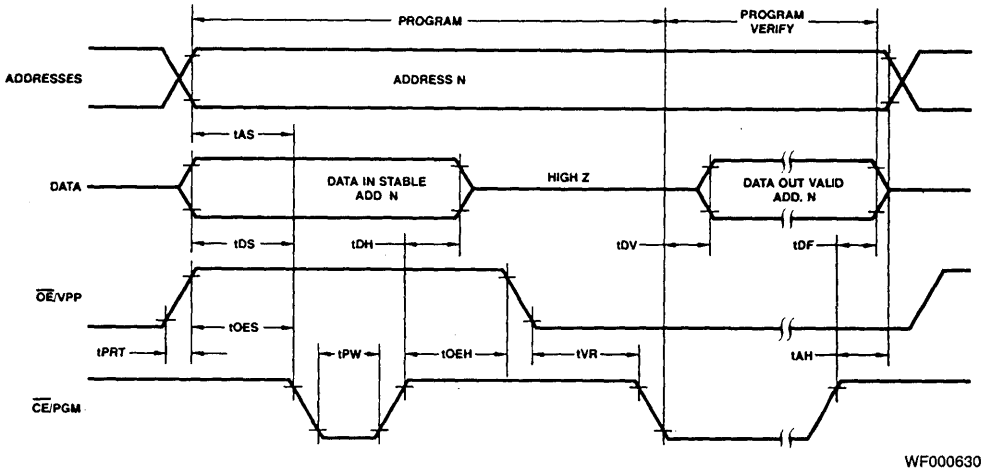
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1$\mu$F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on Am2732A arrays, a 4.7$\mu$F bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 10 | µA |
| $V_{OL}$ | Input Low Voltage During Verify | $I_{OL}$ = 2.1mA | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH}$ = −400µA | 2.4 | | Volts |
| $I_{CC}$ | $V_{CC}$ Supply Current | | | 100 | mA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Level (All Inputs Except $\overline{OE}/V_{PP}$) | | 2.0 | $V_{CC}$ +1 | Volts |
| $I_{PP}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$ | | 30 | mA |
| $t_{AS}$ | Address Set-up time | Input $t_R$ and $t_F$ (10% to 90%) = 20ns<br>Input Signal Levels = 0.8 to 2.2V<br>Input Timing Reference Level = 1V and 2V<br>Output Timing Reference Level = 0.8V and 2V | 2 | | µs |
| $t_{OES}$ | Output Enable Set-up Time | | 2 | | µs |
| $t_{DS}$ | Data Set-up Time | | 2 | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | µs |
| $t_{OEH}$ | Output Enable Hold Time | | 2 | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | µs |
| $t_{DF}$ | Chip Enable to Output Float Delay | | 0 | 130 | ns |
| $t_{DV}$ | Data Valid From $\overline{CE}$ ($\overline{CE} = V_{IL}$,$\overline{OE} = V_{IL}$) | | | 1 | µs |
| $t_{PW}$ | Program Pulse Width | | 45 | 55 | ms |
| $t_{PRT}$ | Program Pulse Rise Time | | 50 | | ns |
| $t_{VR}$ | $V_{PP}$ Recovery Time | | 2 | | ns |

Note: 1. When programming the Am2732A, it is advisable to connect a 0.1µF capacitor between $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

## PROGRAMMING WAVEFORMS




WF000630

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −65°C to +135°C
Voltage on All Inputs/
Outputs (except $V_{PP}$) ..... +6V to −0.3V
Voltage on $V_{PP}$ during
programming ..... +22 to −0.3V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature
Commercial ..... 0°C to +70°C
Industrial ..... −40°C to +85°C
Extended ..... −55°C to +100°C
Military ..... −55°C to +125°C

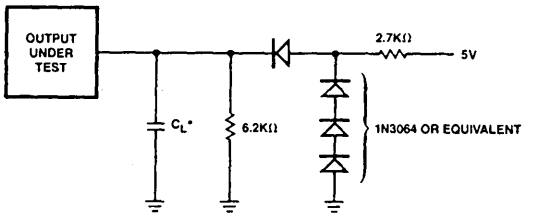
Supply Voltages
Am2732A, -2, -3, -4 ..... +4.75V to +5.25V
Am2732A-20, -25, -30, -40 ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0 to 5.5V | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0 to 5.5V | | | 10 | µA |
| $I_{PP1}$ | $V_{PP}$ Current Read (Note 2) | $V_{PP}$ = 5.5V | | | 1 | mA |
| $I_{CC1}$ | $V_{CC}$ Standby Current (Notes 2, 7) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ | | | 25 | mA |
| $I_{CC2}$ | $V_{CC}$ Active Current (Note 2) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | | | 100 | mA |
| $V_{IL}$ | Input Low Voltage | 0 to 70°C | −0.1 | | +0.8 | Volts |
| $V_{IL}$ | Input Low Voltage | (−40 to +85°C, −55 to +100°C, −55 to +125°C) | −0.1 | | +0.6 | Volts |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$+1 | Volts |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400µA | 2.4 | | | Volts |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 4 | 6 | pF |
| $C_{IN2}$ | $\overline{OE}$/$V_{PP}$ Input Capacitance | $V_{IN}$ = 0V | | | 20 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | | 12 | pF |

## SWITCHING TEST CIRCUIT




TC000120

*Note: $C_L$ = 100pF including jig capacitance.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

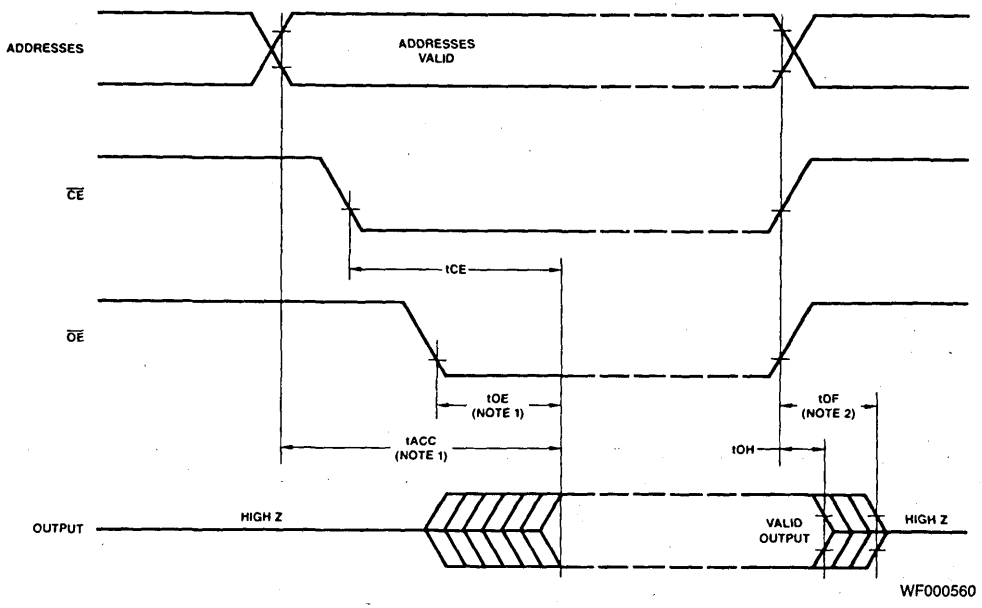
| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 2732APC | Maximum Values 2732A-2 2732A-20 | Maximum Values 2732A 2732A-25 | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1 TTL gate and $C_L$ = 100pF<br>Input Rise and Fall Times ≤ 20ns<br>Input Pulse levels: 0.45 to 2.4V<br>Timing Measurement Reference Level:<br>Inputs: 0.8V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 250 | 200 | 250 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | | $\overline{OE} = V_{IL}$ | | 250 | 200 | 250 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 100 | 70 | 100 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | | 90 | 60 | 90 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | | ns |

| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 2732A-3 2732A-30 | Maximum Values 2732A-4 2732A-45 | Units |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1 TTL gate and $C_L$ = 100pF<br>Input Rise and Fall Times ≤ 20ns<br>Input Pulse levels: 0.45 to 2.4V<br>Timing Measurement Reference Level:<br>Inputs: 0.8V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | | $\overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 150 | 150 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | | 130 | 130 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | ns |

Notes:

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. Typical values are for nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
5. Caution: The 2732A must not be removed from or inserted into a socket or board when $V_{PP}$ or $V_{CC}$ is applied.
6. Unless otherwise specified under Test Conditions, all values apply to the appropriate temperature ranges as defined in Ordering Information of this specification.
7. $I_{CC1}$ limit is 35mA for Am2732APC.

## SWITCHING WAVEFORMS




Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

# Am2764

8192 x 8-Bit UV Erasable and one-time programmable PROMs

## DISTINCTIVE CHARACTERISTICS

- Fast access time — 200ns, 250ns, and 300ns
- New low-cost plastic package for applications not requiring reprogramming
- Low power dissipation
  - 525mW active, 105mW standby
- ±10% power supply tolerance available
- Pin compatible with Am9265 — 64K ROM
- Fast programming time

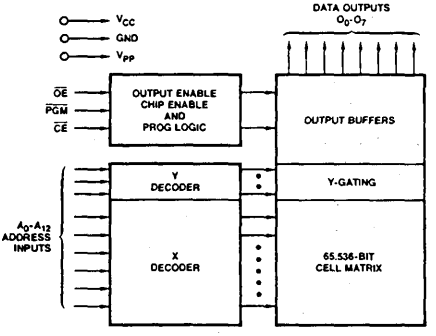
## GENERAL DESCRIPTION

The Am2764 is a 65536-bit ultraviolet erasable and programmable read-only memory. It is organized as 8192 words by 8 bits per word, operates from a single +5V supply, has a static standby mode, and features fast single address location programming.

Because the Am2764 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random.

The part is available in an economical plastic package for applications which do not require reprogramming.

## BLOCK DIAGRAM




BD000160

## MODE SELECT TABLE

| $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (22) | $V_{PP}$ (1) | Outputs (11–13, 15–19) | Mode |
|---|---|---|---|---|---|
| L | L | H | $V_{CC}$ | $D_{OUT}$ | Read |
| H | X | X | $V_{CC}$ | High Z | Standby |
| L | X | L | $V_{PP}$ | $D_{IN}$ | Program |
| L | L | H | $V_{PP}$ | $D_{OUT}$ | Program Verify |
| H | X | X | $V_{PP}$ | High Z | Program Inhibit |

H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

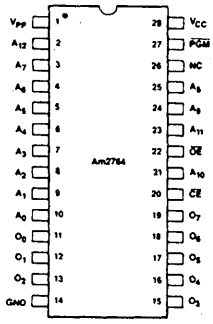
| Access Times | 200ns | | 250ns | | 300ns | | 450ns | |
|---|---|---|---|---|---|---|---|---|
| Power Supply Tolerance | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% |
| Part Number | Am2764-2 | Am2764-20 | Am2764 | Am2764-25 | Am2764-3 | Am2764-30 | Am2764-4 | Am2764-45 |

6

01942E

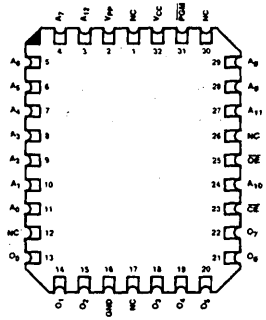
## CONNECTION DIAGRAM
### Top View

**D-28-1**
**P-28-1**




CD000220

**L-32-2**



CD000230

Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am2764-20 L L**

- Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- Package
  - D – 28-pin CERDIP
  - P – 28-pin plastic DIP
  - L – 32-pin leadless chip carrier
- Speed Select
  - See Product Select Guide
- Device Type
  - 8k x 8 EPROM

| Valid Combinations | |
|---|---|
| Am2764 | PC, DC, OI, DL, LC, LI, LL |
| Am2764-2<br>Am2764-20 | DC, DI, LC, LI |
| Am2764-25<br>Am2764-45 | DC, DI, DL, DM, LC, LI, LL, LM |
| Am2764-3<br>Am2764-30<br>Am2764-4 | DC, DI, DL, LC, LI, LL |

### ERASING THE Am2764 (Does Not Apply to Am2764PC)

In order to clear all locations of their programmed contents, it is necessary to expose the Am2764 to an ultraviolet light source. A dosage of 15 Wseconds/cm$^2$ is required to completely erase an Am2764. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000$\mu$W/cm$^2$ for 15 to 20 minutes. The Am2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2764, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537A, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am2764, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

### PROGRAMMING THE Am2764

Upon delivery, or after each erasure the Am2764 has all 65536 bits in the "1", or high state. "0"s are loaded into the Am2764 through the procedure of programming.

The programming mode is entered when +21V is applied to the VPP pin. A 0.1$\mu$F capacitor must be placed across VPP and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{PGM}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{PGM}$ input is prohibited when programming.

### REDUCING PROGRAMMING TIME OF Am2764

Since the introduction of the 5V 16K-bit EPROM (Am2716), the program pulse width ($T_{PW}$) of EPROMs has been specified at 50ms per address. Thus the total programming time for the Am2764 would be almost seven minutes (50ms x 8192 = 410sec). It is clearly desirable to reduce this programming time. By using interactive programming techniques, it is possible to reduce programming time for the Am2764 to a minimum of about 45sec and typically in the range of 90sec. The flow chart on Page 6-32 shows the Interactive Programming Algorithm. When using the standard programming technique, each address is given a 50ms program pulse sequentially and then the entire EPROM memory is verified. Interactive algorithms reduce programming time by using shorter (1ms) program pulse and giving each address only as many pulses as necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 15 pulses. When the data is correctly verified, the address is given an additional 4X ms "overprogram" pulse; where X is a count of the number of 1ms pulse interactions that are required (thus the "overprogram" pulse can vary from a minimum of 4ms to a maximum of 60ms). This whole process is repeated while sequencing through each address of the Am2764. The algorithm is done at $V_{CC} = V_{PP} = 6V$ to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5V \pm 5\%$.

### READ MODE

The Am2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

### STANDBY MODE

The Am2764 has a standby mode which reduces the active power dissipation by 80%, from 525mW to 105mW (values for 0°C to +70°C). The Am2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### PROGRAM INHIBIT

Programming of multiple Am2764s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ or $\overline{PGM}$, all like inputs (including $\overline{OE}$) of the parallel Am2764s may be common. A TTL low-level program pulse applied to an Am2764's $\overline{PGM}$ input with VPP at 21V and $\overline{CE}$ low will program that Am2764. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other Am2764s from being programmed.

### PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$ and $\overline{CE}$ at $V_{IL}$. Data should be verified $t_{OE}$ after the falling edge of $\overline{OE}$. $\overline{PGM}$ must be at $V_{IH}$.

### SYSTEM APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1$\mu$F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7$\mu$F bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

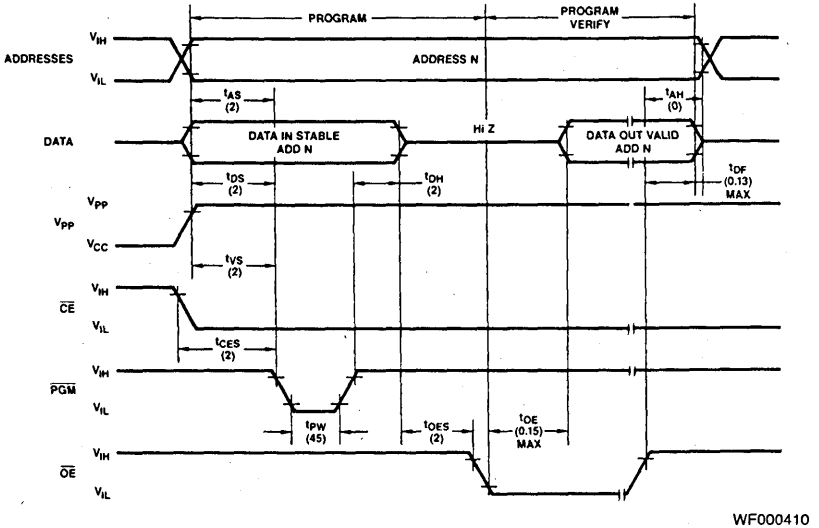
## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 10 | μA |
| $V_{OL}$ | Output Low Voltage During Verify | $I_{OL} = 2.1mA$ | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH} = -400\mu A$ | 2.4 | | Volts |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Active) | | | 100 | mA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$ +1 | Volts |
| $I_{PP}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | 30 | mA |
| $t_{AS}$ | Address Set-up time | Input $t_R$ and $t_F$ (10% to 90%) = 20ns<br>Input Pulse Levels = 0.45 to 2.4V<br>Input Timing Reference Level = 1V and 2V<br>Output Timing Reference Level = 0.8V and 2V | 2 | | μs |
| $t_{OES}$ | Output Enable Set-up Time | | 2 | | μs |
| $t_{DS}$ | Data Set-up Time | | 2 | | μs |
| $t_{AH}$ | Address Hold Time | | 0 | | μs |
| $t_{OEH}$ | Output Enable Hold Time | | 2 | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | μs |
| $t_{DF}$ | Chip Enable to Output Float Delay | | 0 | 130 | ns |
| $t_{VS}$ | $V_{PP}$ Setup Time | | 2 | | μs |
| $t_{PW}$ | $\overline{PGM}$ Pulse Width | | 45 | 55 | ms |
| $t_{CES}$ | $\overline{CE}$ Set-up Time | | 2 | | μs |
| $t_{OE}$ | Data Valid From $\overline{OE}$ | | | 150 | ns |

Notes:

1. *Caution: If $V_{CC}$ is not applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$, the 2764 could be damaged.*
2. When programming the Am2764, a 0.1μF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

## STANDARD PROGRAMMING WAVEFORMS (Notes 1, 2 and 3)




WF000410

Notes:

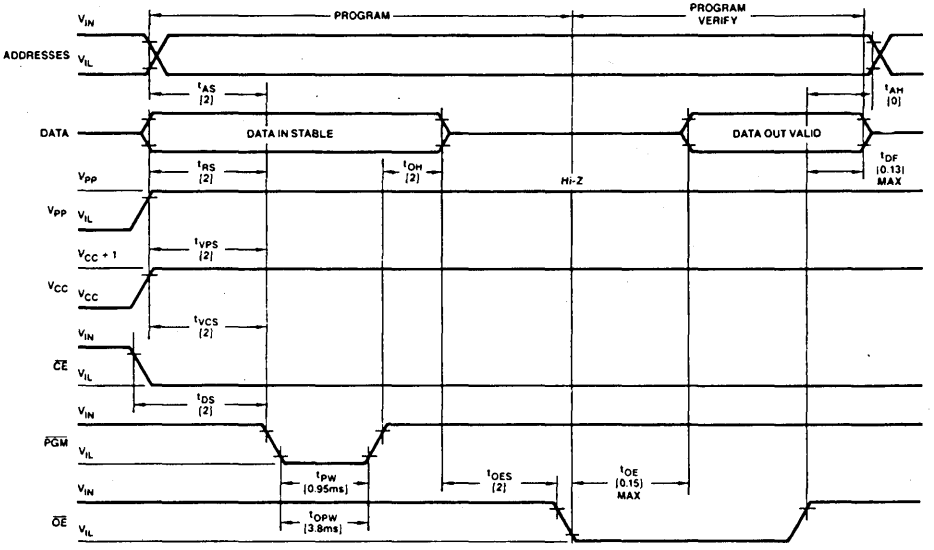
1. All times shown in ( ) are minimum and in μsec unless otherwise specified.
2. The input timing reference level is 1V for a $V_{IL}$ and 2V for a $V_{IH}$.
3. $t_{OE}$ and $t_{DF}$ are characteristics of the device but must be accommodated by the programmer.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | μA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | | 0.8 | Volts |
| $V_{IH}$ | Input High Level | | 2.0 | | $V_{CC}$ +1 | Volts |
| $V_{OL}$ | Output Low Voltage During Verify | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH}$ = -400μA | 2.4 | | | Volts |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | | 100 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current (Program) | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |
| $t_{AS}$ | Address Setup Time | | 2 | | | μs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | | μs |
| $t_{DS}$ | Data Setup Time | | 2 | | | μs |
| $t_{AH}$ | Address Hold Time | | 0 | | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | | μs |
| $t_{DF}$ | Chip Enable to Output Float Delay | | 0 | | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | | μs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | | μs |
| $t_{PW}$ | $\overline{PGM}$ Initial Program Pulse Width | | 0.95 | 1.0 | 1.05 | ms |
| $t_{OPW}$ | $\overline{PGM}$ Overprogram Pulse Width | (see Note 2) | 3.8 | | 63 | ms |
| $t_{CES}$ | $\overline{CE}$ Setup Time | | 2 | | | μs |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | | 150 | ns |

Notes:

1. *Caution: If $V_{CC}$ is not applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$, the 2764 could be damaged.*
2. When programming the Am2764, a 0.1μF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

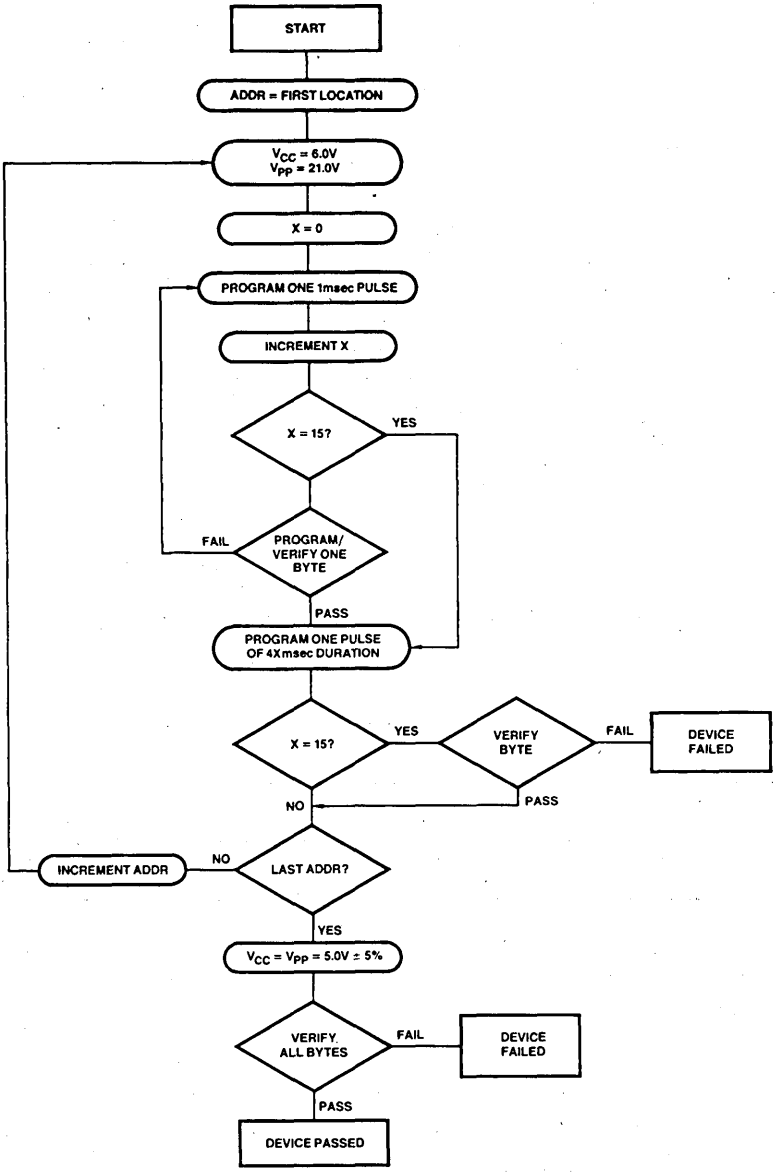
## INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS (Notes 1, 2 and 3)




WF000390

Notes:
1. All times shown in [ ] are minimum and in μsec unless otherwise specified.
2. The input timing reference level is .8V for a $V_{IL}$ and 2V for a $V_{IH}$.
3. $T_{OE}$ and $t_{DF}$ are characteristics of the device but must be accommodated by the programmer.

## INTERACTIVE PROGRAMMING FLOW CHART




PF000010

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... +22V to −0.6V
DC Voltage Applied to All Inputs/
Outputs ..... +7.0V to −0.6V
DC Layout Voltage ..... −0.5V to +7.0V
Power Dissipation ..... 1.0W
DC Output Current ..... 20mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature
Commercial ..... 0°C to +70°C
Industrial ..... −40°C to +85°C
Extended ..... −55°C to +100°C
Military ..... −55°C to +125°C

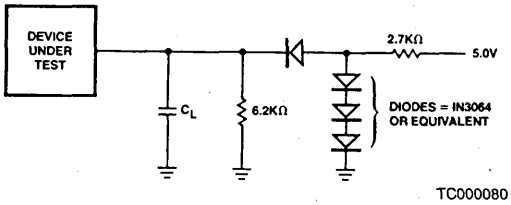
SupplyVoltages
Am2764,-2,-3,-4 ..... +4.75V to +5.25V
Am2764-20,-25,-30,-40 ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to 5.5V | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to 5.5V | | | 10 | µA |
| $I_{PP1}$ | $V_{PP}$ Current Read (Note 2) | $V_{PP}$ = 5.5V | | | 5 | mA |
| $I_{CC1}$ | $V_{CC}$ Standby Current (Notes 2, 7) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ (0°C to +70°C) | | | 20 | mA |
| $I_{CC1}$ | $V_{CC}$ Standby Current (Note 2) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ (−40°C to +85°C, −55°C to +100°C, −55°C to +125°C) | | | 25 | mA |
| $I_{CC2}$ | $V_{CC}$ Active Current (Note 2) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | | | 100 | mA |
| $V_{IL}$ | Input Low Voltage | 0°C to 70°C | −0.1 | | +0.8 | Volts |
| $V_{IL}$ | Input Low Voltage | (−40°C to +85°C, −55°C to +100°C, −55°C to +125°C) | −0.1 | | +0.6 | Volts |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$+1 | Volts |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400µA | 2.4 | | | Volts |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 8 | 12 | pF |

## SWITCHING TEST CIRCUIT




$C_L$ = 100pF including jig capacitance

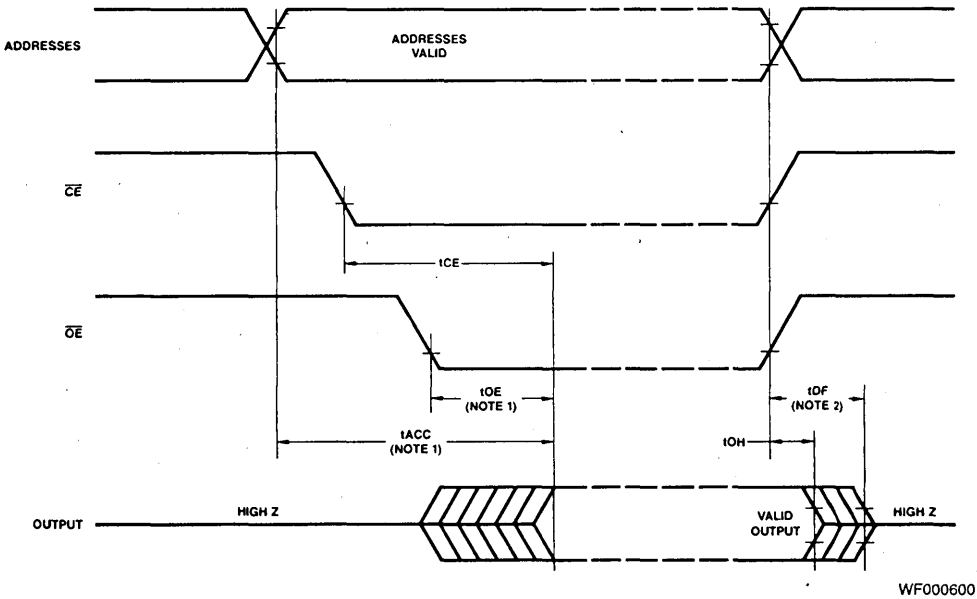
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 2764-20 2764-2 | 2764-25 2764 2764PC | 2764-30 2764-3 | 2764-45 2764-4 | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1 TTL gate and $C_L$ = 100pF Input Rise and Fall Times ≤ 20ns Input Pulse levels: 0.45V to 2.4V Timing measurement reference level: Inputs: 1V and 2V Outputs: 0.8V and 2V | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | 200 | 250 | 300 | 450 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | | $\overline{OE}$ = $V_{IL}$ | | 200 | 250 | 300 | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE}$ = $V_{IL}$ | | 75 | 100 | 120 | 150 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE}$ = $V_{IL}$ | 0 | 60 | 85 | 105 | 130 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever Occured First | | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | 0 | | | | | ns |

Notes:

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. Typical values are for nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
5. Caution: The 2764 must not be removed from or inserted into a socket or board when $V_{PP}$ or $V_{CC}$ is applied.
6. Unless otherwise specified under Test Conditions, all values apply to the appropriate temperature ranges as defined in Ordering Information of this specification.
7. $I_{CC1}$ = 25mA for Am2764-4 and Am2764-45, and the Am2764PC.

## SWITCHING WAVEFORMS

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Notes: 1. OE may be delayed up to $t_{ACC}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

# Am9864

8192 x 8-Bit Electrically Erasable PROM

## DISTINCTIVE CHARACTERISTICS

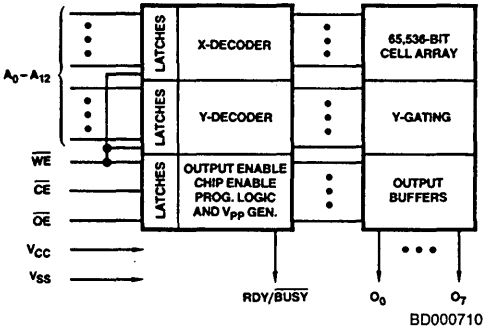
- 5V only operation
- Ready/Busy Pin for end of write indication
- Fast Read Access Time
  Am9864-2 — 200ns
  Am9864 — 250ns
  Am9864-3 — 350ns
- Data Protection Features to prevent writes from occurring during $V_{CC}$ power up/down
- Minimum endurance of 10,000 write cycles per byte with a 10 year data retention

## GENERAL DESCRIPTION

The Am9864 is a 65,536 bit Electrically Erasable Programmable Read Only Memory (EEPROM), organized as 8192 words by 8 bits per word. It operates from a single 5 volt supply and has a fully self timed write cycle with address, data and control lines latched during the write operation. The Am9864 is fabricated on AMD's highly manufacturable N-Channel Silicon gate process, and uses AMD's proprietary EEPROM technology to achieve the Electrically Alterable Nonvolatile Storage. This technology employs the industry accepted Fowler-Nordheim tunneling across a thin oxide.

The Am9864 provides on chip the logic necessary to interface with most microprocessors. The latched inputs and self timed write cycle free the microprocessor to perform other tasks during a write. A transparent automatic erase before write enhances system performance.

## BLOCK DIAGRAM




BD000710

## MODE SELECT TABLE

| CE (20) | OE (22) | WE (27) | R/B (1) | I/O (11–13, 15–19) | Mode |
|---|---|---|---|---|---|
| L | L | H | H | Data Out | Read |
| L | H | ⊓ | L | Data In | Write |
| H | X | X | H | Hi Z | Standby |
| L | H | H | H | Hi Z | Read Inhibit |
| L | L | ⊓ | H | Hi Z | Write Inhibit |

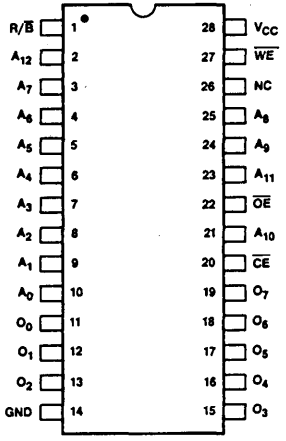
H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

| Part Number | Am9864-2 | Am9864-20 | Am9864 | Am9864-25 | Am9864-3 |
|---|---|---|---|---|---|
| Supply Voltage | 5V ±5% | 5V ±10% | 5V ±5% | 5V ±10% | 5V ±5% |
| Temperature Range | 0 to 70°C | | 0 to 70°C | | 0 to 70°C |
| Access Time | 200ns | | 250ns | | 350ns |
| Chip Select | 200ns | | 250ns | | 350ns |
| Output Enable | 75ns | | 100ns | | 120ns |

05003A

## CONNECTION DIAGRAM
### Top View




CD000980

## ORDERING INFORMATION

**Am9864-2 D C**

- C – Temperature: C – Commercial (0°C to +70°C)
- D – Package: D – 28-pin CERDIP
- 2 – Speed and Power Supply Tolerance: See Product Selector Guide
- Am9864-2 – Device Type: 64k EEPROM

| Valid Combinations | |
|---|---|
| Am9864<br>Am9864-25<br>Am9864-3<br>Am9864-30<br>Am9864-45 | DC |

### Read Mode

The Am9864 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs $t_{OE}$ after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

### Standby Mode

The Am9864 has a standby mode which reduces the active power dissipation by 60%, from 525mW to 210mW (values for 0 to 70°C). The Am9864 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

### Data Protection

The Am9864 incorporates several features that prevent unwanted write cycles during $V_{CC}$ power up and power down. These features protect the integrity of the stored data.

To avoid the initiation of a write cycle during $V_{CC}$ power up and power down, a write cycle is locked out for $V_{CC}$ less than 3.8 volts. It is the user's responsibility to insure that the control levels are logically correct when $V_{CC}$ is above 3.8 volts.

There is a $\overline{WE}$ lockout circuit that prevents WE pulses of less than 20ns duration from initiating a write cycle.

When the $\overline{OE}$ control is in logic zero condition, a write cycle cannot be initiated.

### Write Mode

The Am9864 has a write cycle that is similar to that of a Static RAM. The write cycle is completely self timed, and initiated by a low going pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$ the address information is latched. On the rising edge, the data and the control pins ($\overline{CE}$ and $\overline{OE}$) are latched. The Ready/Busy pin (pin 1) goes to a logic low level indicating that the Am9864 is in a write cycle which signals the microprocessor host that the system bus is free for other activity. When Ready/Busy goes back to a high the Am9864 has completed writing, and is ready to accept another cycle.

### Output Or-Tieing

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

### Ready/Busy Pin

The Ready/Busy output (pin 1) when tied to a system interrupt allows a writing operation to be defined by one microprocessor cycle time. The state of this output is determined by the Am9864 and must not be externally forced. When not used this pin must be kept floating.

## SYSTEM APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EEPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +125°C
Ambient Temperature with
Power Applied ..... −10°C to +80°C
Voltage on All Inputs/with
Respect to GND ..... +6.25V to −0.6V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature ..... 0°C to +70°C

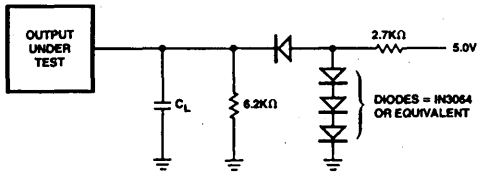
Supply Voltage ..... +4.5V to +5.5V
*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = 0 to 5.5V | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0 to 5.5V | | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ Current (Standby) | $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ | | | 40 | mA |
| $I_{CC2}$ | $V_{CC}$ Current (Active) | $\overline{OE} = \overline{CE} = V_{IL}$ | | | 100 | mA |
| $I_{CC}$ | $V_{CC}$ Current (Write) | $\overline{WE}$ = ⊓⊔, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ | | | 120 | mA |
| $V_{IL}$ | Input Low Voltage | | −0.1 | | .8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$ + 1 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | .45 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400µA | 2.4 | | | V |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 4 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $\overline{OE} = \overline{CE} = V_{IH}$ | | 8 | 12 | pF |

Note 1. This parameter is only sampled and not 100% tested.

## SWITCHING TEST CIRCUIT




TC000250

$C_L$ = 100pF, including jig capacitance.

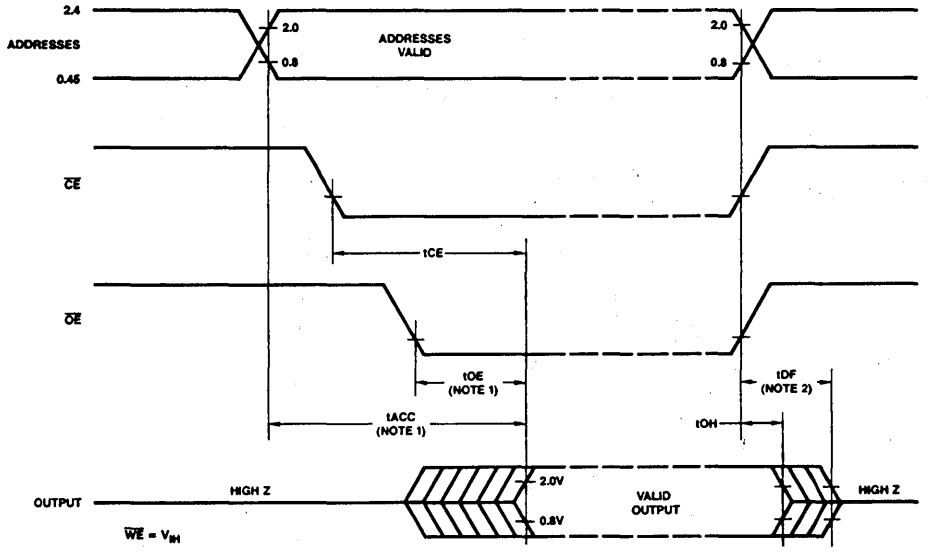
## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Parameter | Test Conditions | | Am9864-2, 20 Min | Am9864-2, 20 Max | Am9864, -25 Min | Am9864, -25 Max | Am9864-3 Min | Am9864-3 Max | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **READ** | | | | | | | | | | | |
| 1 | $t_{ACC}$ | Address to Output Delay | $\overline{WE}$ = $V_{IH}$ Output Load: 1 TTLgate and $C_L$ = 100pF Input Rise and Fall Times: ≤20ns Input Pulse Levels: 0.45 to 2.4V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | | 200 | | 250 | | 350 | ns |
| 2 | $t_{CE}$ | $\overline{CE}$ to Output Delay | | $\overline{OE}$ = $V_{IL}$ | | 200 | | 250 | | 350 | |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE}$ = $V_{IL}$ | | 75 | | 100 | | 120 | |
| 4 | $t_{DF}$ (Note 1) | Output Enable High to Output Float | | $\overline{CE}$ = $V_{IL}$ | 0 | 60 | 0 | 60 | 0 | 80 | |
| 5 | $t_{OH}$ (Note 1) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ WhicheverOccurred First | | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$ | 0 | | 0 | | 0 | | |
| **WRITE** | | | | | | | | | | | |
| 1 | $t_{AS}$ | Address to Write Setup Time | | | 20 | | 20 | | 60 | | ns |
| 2 | $t_{CS}$ | $\overline{CE}$ to Write Setup Time | | | 20 | | 20 | | 20 | | |
| 3 | $t_{WP}$ | Write Pulse Width | | | 100 | | 100 | | 150 | | |
| 4 | $t_{AH}$ | Address Hold Time | | | 80 | | 80 | | 100 | | |
| 5 | $t_{DS}$ | Data Setup Time | | | 50 | | 50 | | 70 | | |
| 6 | $t_{DH}$ | Data Hold Time | | | 20 | | 20 | | 20 | | |
| 7 | $t_{CH}$ | $\overline{CE}$ Hold Time | | | 50 | | 50 | | 50 | | |
| 8 | $t_{OES}$ | $\overline{OE}$ Setup Time | | | 20 | | 20 | | 20 | | |
| 9 | $t_{OEH}$ | $\overline{OE}$ Hold Time | | | 35 | | 35 | | 35 | | |
| 10 | $t_{DB}$ | Time to Device Busy | | | | 100 | | 100 | | 100 | |
| 11 | $t_{WR}$ | Bytes Write Cycle | | | | 10 | | 10 | | 20 | ms |
| 12 | $t_{RE}$ | Write Recovery Time | | | 0 | | 0 | | 0 | | ns |
| 13 | $t_{RBO}$ (Note 2) | R/$\overline{B}$ to Output Time | | | | 50 | | 50 | | 50 | |
| 14 | | Number of Writes per Byte | | | 10 | | 10 | | 10 | | x1000 |

Notes:
1. This parameter is sampled and is not 100% tested.
2. If $\overline{CE}$ and $\overline{OE}$ = $V_{IL}$ when RB is going to $V_{OH}$, then $D_{OUT}$ becomes valid after $t_{RBO}$ ns.

## SWITCHING WAVEFORMS

### READ

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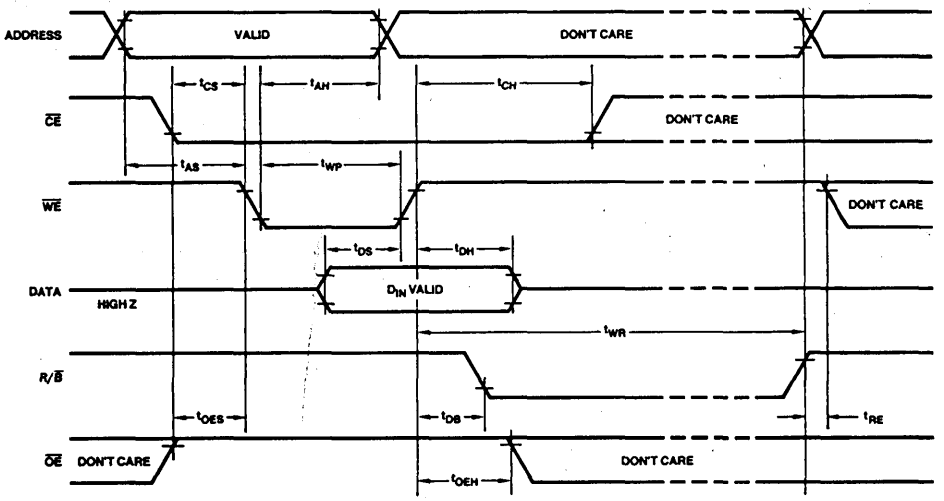
Notes:
1. $\overline{OE}$ may be delayed up to $t_{ACC}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

### WRITE




WF001300



05003A

# Am27128

16,384 x 8-Bit UV Erasable PROM

## DISTINCTIVE CHARACTERISTICS

- Fast access time — as low as 150ns
- Low power consumption
- Separate chip enable and output enable controls
- TTL compatible inputs/outputs
- Pin compatible to Am2764 EPROM and Am92128-128K ROM
- Fast programming time (3 min typical)

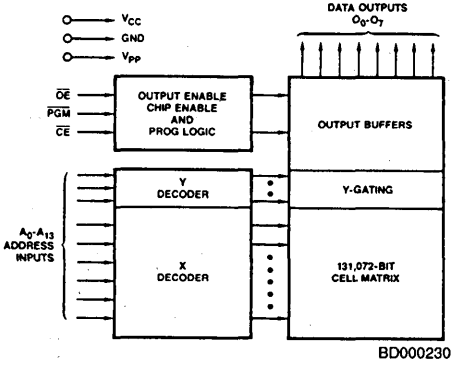
## GENERAL DESCRIPTION

The Am27128 is a 131,072-bit UV-light erasable and electrically programmable read-only memory. It is organized as 16384 words by 8-bits per word. The standard Am27128 offers access time of 250ns, allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention in a multiple-bus microprocessor system, the Am27128 offers separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random. To reduce programming time, the Am27128 may be programmed using 1ms pulses. Typically, Am27128 can be programmed in three minutes. See Flow Chart on page 6-41 for details.

## BLOCK DIAGRAM




BD000230

## MODE SELECT TABLE

| $\overline{CE}$ (20) | $\overline{OE}$ (22) | $\overline{PGM}$ (27) | $V_{PP}$ (1) | Outputs (11–13, 15–19) | Mode |
|---|---|---|---|---|---|
| L | L | H | $V_{CC}$ | $D_{OUT}$ | Read |
| H | X | X | $V_{CC}$ | High Z | Standby |
| L | H | L | $V_{PP}$ | $D_{IN}$ | Program |
| L | L | H | $V_{PP}$ | $D_{OUT}$ | Program Verify |
| H | X | X | $V_{PP}$ | High Z | Program Inhibit |

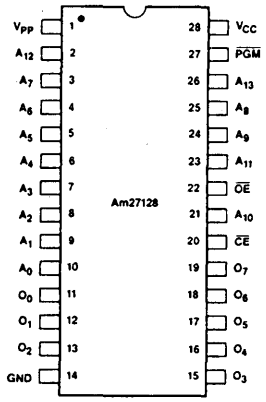
H = HIGH
L = LOW
X = Don't Care

## PRODUCT SELECTOR GUIDE

| Access Times | 150ns | | 200ns | | 250ns | | 300ns | | 450ns | |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply Tolerance | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% |
| Part Number | Am27128-1 | Am27128-15 | Am27128-2 | Am27128-20 | Am27128 | Am27128-25 | Am27128-3 | Am27128-30 | Am27128-4 | Am27128-45 |

03138D

## CONNECTION DIAGRAM
### Top View




CD000330

*Note: Pin 1 is marked for orientation*

## ORDERING INFORMATION

**Am27128-30 D C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 28-pin CERDIP
- 30 — Speed Select
  - See Product Selector Guide
- Am27128 — Device Type
  - 16k x 8 EPROM

| Valid Combinations | |
|---|---|
| Am27128-1<br>Am27128-15 | DC, DI |
| Am27128-2<br>Am27128-3<br>Am27128-30<br>Am27128-4 | DC, DI, DL |
| Am27128-20<br>Am27128-25<br>Am27128-45 | DC, DI, DL,<br>DM |

## ERASING THE Am27128

In order to clear all locations of their programmed contents, it is necessary to expose the Am27128 to an ultraviolet light source. A dosage of 15 Wseconds/cm$^2$ is required to completely erase an Am27128. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000$\mu$W/cm$^2$ for 15 to 20 minutes. The Am27128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27128, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537A, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27128, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

## PROGRAMMING THE Am27128

Upon delivery, or after each erasure the Am27128 has all 131,072 bits in the "1", or high state. "0"s are loaded into the Am27128 through the procedure of programming.

The programming mode is entered when +21V is applied to the $V_{PP}$ pin. A 0.1$\mu$F capacitor must be placed across $V_{PP}$ and ground to suppress spurious voltage transients which may damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL low level pulse is applied to the $\overline{PGM}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC low level to the $\overline{PGM}$ input is prohibited when programming.

## REDUCING PROGRAMMING TIME OF THE Am27128

Since the introduction of the 5V 16K-bit EPROM (Am2716), the program pulse width ($T_{PW}$) of EPROMs has been specified at 50ms per address. Thus the total programming time for the Am27128 would be almost fourteen minutes (50ms x 16,384 = 820sec). It is clearly desirable to reduce this programming time. By using interactive programming techniques, it is possible to reduce programming time for the Am27128 to a minimum of about 90sec and typically in the range of 180sec. The flow chart on Page 6-47 shows the Interactive Programming Algorithm. When using the standard programming technique, each address is given a 50ms program pulse sequentially and then the entire EPROM memory is verified. Interactive algorithms reduce programming time by using a shorter (1ms) program pulse and giving each address only as many pulses as necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 15 pulses. When the data is correctly verified, the address is given an additional 4X ms "overprogram" pulse; where X is a count of the number of 1ms pulse interactions that are required (thus the "overprogram" pulse can vary from a minimum of 4ms to a maximum of 60ms). This whole process is repeated while sequencing through each address of the Am27128. The algorithm is done at $V_{CC} = V_{PP} = 6V$ to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5V \pm 5\%$.

## READ MODE

The Am27128 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The Am27128 has a standby mode which reduces the active power dissipation by 80%, from 525mW to 130mW (values for 0°C to +70°C). The Am27128 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

## OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAM INHIBIT

Programming of multiple Am27128s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ or $\overline{PGM}$, all like inputs (including $\overline{OE}$) of the parallel Am27128s may be common. A TTL low-level program pulse applied to an Am27128's $\overline{PGM}$ input with $V_{PP}$ at 21V and $\overline{CE}$ low will program that Am27128. A high-level $\overline{CE}$ or $\overline{PGM}$ input inhibits the other Am27128s from being programmed.

## PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$ and $\overline{CE}$ at $V_{IL}$. Data should be verified $t_{OE}$ after the falling edge of $\overline{OE}$. $\overline{PGM}$ must be at $V_{IH}$.

## SYSTEM APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1$\mu$F ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7$\mu$F bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

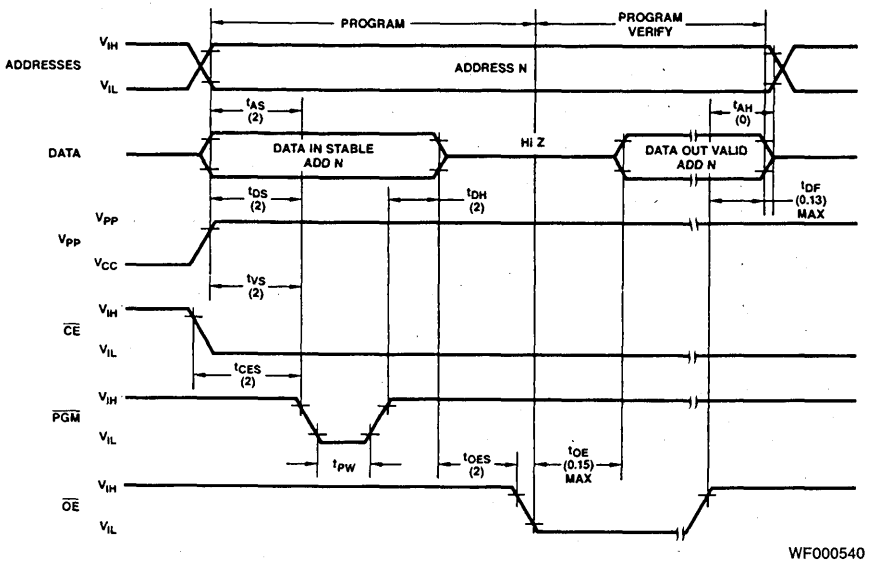
## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 10 | μA |
| $V_{OL}$ | Output Low Voltage During Verify | $I_{OL} = 2.1mA$ | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH} = -400\mu A$ | 2.4 | | Volts |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Active) | | | 100 | mA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Level | | 2.0 | $V_{CC}$ +1 | Volts |
| $I_{PP}$ | $V_{PP}$ Supply Current | $\overline{CE} = V_{IL} = \overline{PGM}$ | | 30 | mA |
| $t_{AS}$ | Address Setup time | Input $t_R$ and $t_F$ (10% to 90%) = 20ns<br>Input Pulse Levels = 0.45V to 2.4V<br>Input Timing Reference Level = 1V and 2V<br>Output Timing Reference Level = 0.8V and 2V | 2 | | μs |
| $t_{OES}$ | Output Enable Setup Time | | 2 | | μs |
| $t_{DS}$ | Data Setup Time | | 2 | | μs |
| $t_{AH}$ | Address Hold Time | | 0 | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | μs |
| $t_{DF}$ | Chip Enable to Output Float Delay | | 0 | 130 | ns |
| $t_{VS}$ | $V_{PP}$ Setup Time | | 2 | | μs |
| $t_{PW}$ | $\overline{PGM}$ Pulse Width | | 45 | 55 | ms |
| $t_{CES}$ | $\overline{CE}$ Setup Time | | 2 | | μs |
| $t_{OE}$ | Data Valid From $\overline{OE}$ | | | 150 | ns |

Notes:

1. *Caution: If $V_{CC}$ is not applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$, the 27128 could be damaged.*
2. When programming the Am27128, a 0.1μF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

## PROGRAMMING WAVEFORM (Notes 1, 2 and 3)




Notes:

1. All times shown in ( ) are minimum and in μsec unless otherwise specified.
2. The input timing reference level is 1V for a $V_{IL}$ and 2V for a $V_{IH}$.
3. $t_{OE}$ and $t_{DF}$ are characteristics of the device but must be accommodated by the programmer.

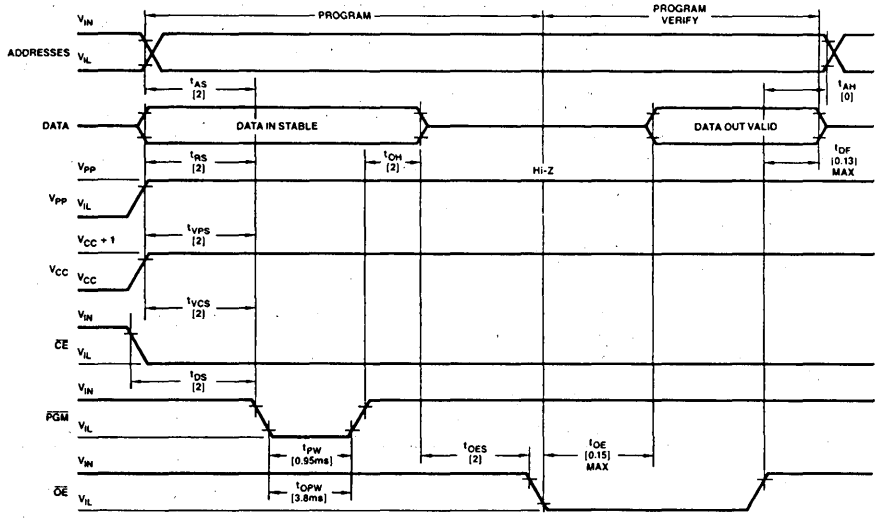
## INTERACTIVE PROGRAMMING ALGORITHM

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | μA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | | 0.8 | Volts |
| $V_{IH}$ | Input High Level | | 2.0 | | $V_{CC}$ +1 | Volts |
| $V_{OL}$ | Input Low Voltage During Verify | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH}$ = -400μA | 2.4 | | | Volts |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | | 100 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current (Program) | $\overline{CE} = V_{IL} = \overline{PGM}$ | | | 30 | mA |
| $t_{AS}$ | Address Setup Time | | 2 | | | μs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | | μs |
| $t_{DS}$ | Data Setup Time | | 2 | | | μs |
| $t_{AH}$ | Address Hold Time | | 0 | | | μs |
| $t_{DH}$ | Data Hold Time | | 2 | | | μs |
| $t_{DF}$ | Chip Enable to Output Float Delay | | 0 | | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | | μs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | | μs |
| $t_{PW}$ | $\overline{PGM}$ Initial Program Pulse Width | | 0.95 | 1.0 | 1.05 | ms |
| $t_{OPW}$ | $\overline{PGM}$ Overprogram Pulse Width | (see Note 2) | 3.8 | | 63 | ms |
| $t_{CES}$ | $\overline{CE}$ Setup Time | | 2 | | | μs |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | | 150 | ns |

Notes:

1. *Caution: If $V_{CC}$ is not applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$, the Am27128 could be damaged.*
2. When programming the Am27128, a 0.1μF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.

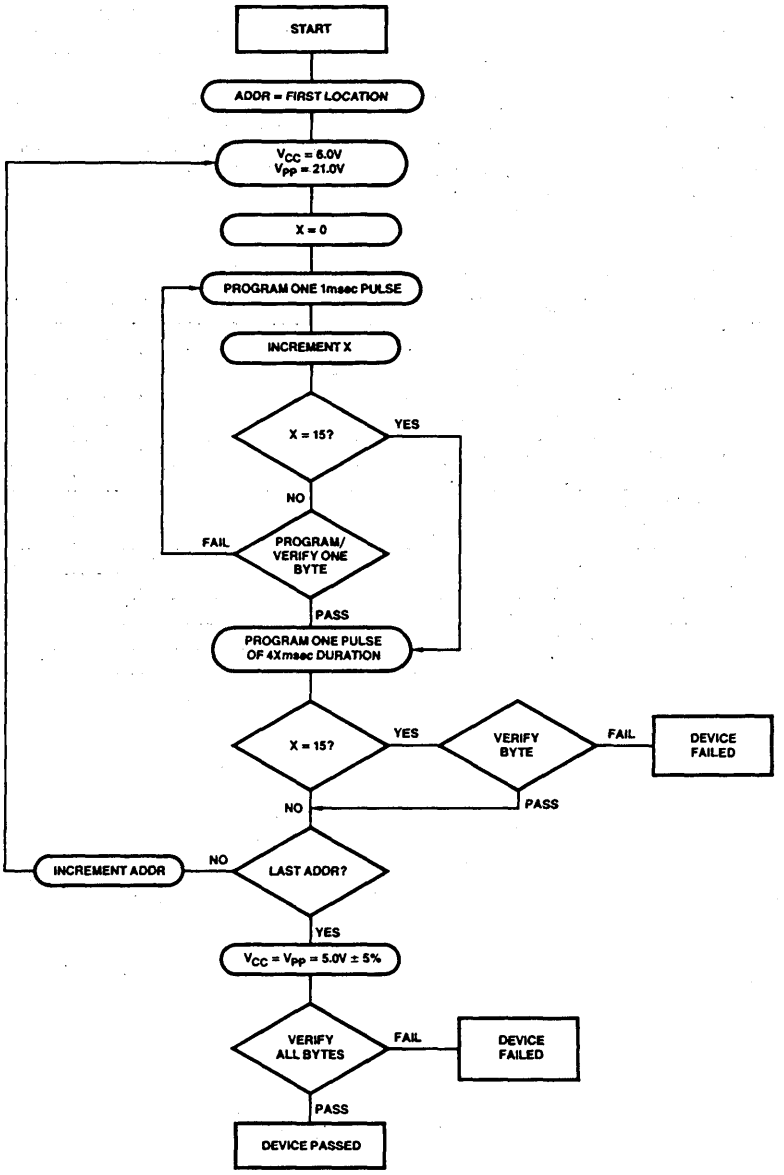
## INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS (Notes 1, 2 and 3)




WF000550

Notes:
1. All times shown in [ ] are minimum and in μsec unless otherwise specified.
2. The input timing reference level is .8V for a $V_{IL}$ and 2V for a $V_{IH}$.
3. $t_{OE}$ and $t_{DF}$ are characteristics of the device but must be accommodated by the programmer.

## INTERACTIVE PROGRAMMING FLOW CHART




PF000020

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −10°C to +80°C
Voltage on All Inputs/Outputs
(except $V_{PP}$) ..... +7V to −0.6V
Voltage on $V_{PP}$ during
programming ..... +22v to −0.6v

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature
Commercial ..... 0°C to +70°C
Industrial ..... −40°C to +85°C
Extended ..... −55°C to +100°C
Military ..... −55°C to +125°C

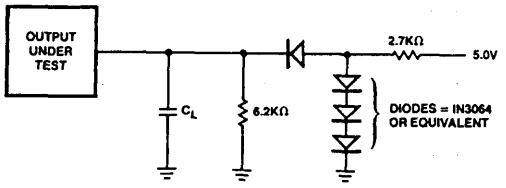
Supply Voltages
Am2732A, -2, -3, -4 ..... +4.75V to +5.25V
Am2732A-20, -25, -30, -40 ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to 5.5V | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to 5.5V | | | 10 | µA |
| $I_{PP1}$ | $V_{PP}$ Current Read (Note 2) | $V_{PP}$ = 5.5V | | | 5 | mA |
| $I_{CC1}$ | $V_{CC}$ Standby Current (Notes 2, 6) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ | | | 25 | mA |
| $I_{CC2}$ | $V_{CC}$ Active Current (Note 2) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | | | 100 | mA |
| $V_{IL}$ | Input Low Voltage | | −0.1 | | +0.8 | Volts |
| $V_{IL}$ | Input Low Voltage (Am27128-20DM, Am27128-25DM and Am27128-45DM Only) | | −0.1 | | +0.6 | Volts |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$+1 | Volts |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400µA | 2.4 | | | Volts |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 8 | 12 | pF |

## SWITCHING TEST CIRCUIT




TC000130

$C_L$ = 100pF, including jig capacitance

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 27128-15 27128-1 | Maximum Values 27128-20 27128-2 | Maximum Values 27128-25 27128 | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1TTL gate and $C_L$ = 100pF Input Rise and Fall Times ≤ 20ns Input Pulse levels: 0.45 to 2.4V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 150 | 200 | 250 | ns |
| 2 | $t_{CE}$ | CE Output Delay | | $\overline{OE} = V_{IL}$ | | 150 | 200 | 250 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 75 | 75 | 100 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | 0 | 60 | 60 | 85 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | | ns |

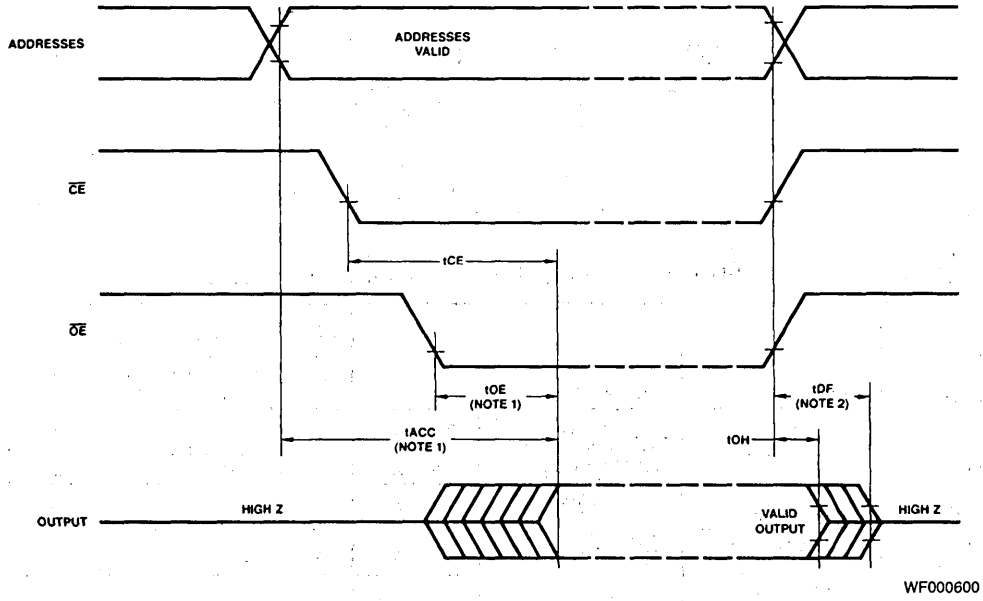
| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 27128-30 27128-3 | Maximum Values 27128-45 27128-4 | Units |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1TTL gate and $C_L$ = 100pF Input Rise and Fall Times ≤ 20ns Input Pulse levels: 0.45 to 2.4V Timing Measurement Reference Level: Inputs: 1V and 2V Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 2 | $t_{CE}$ | CE Output Delay | | $\overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 120 | 150 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | 0 | 105 | 130 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | ns |

Notes:

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. Typical values are for nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
5. Caution: The 27128 must not be removed from or inserted into a socket or board when $V_{PP}$ or $V_{CC}$ is applied.
6. $I_{CC1}$, Max for Am27128-4 and Am27128-45 is 40mA.

6

## SWITCHING WAVEFORMS




WF000600

Notes: 1. OE may be delayed up to $t_{ACC}$-$t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

# Am27256

32,768 x 8-Bit UV Erasable PROM

## DISTINCTIVE CHARACTERISTICS

- Fast access time — as low as 170ns
- Low power consumption
- Separate chip enable and output enable controls
- Pin compatible to Am2764 EPROM, Am27128 EPROM and and Am92256 – 256K ROM
- Fast programming time (5 min typical)
- Auto select mode for automated programming

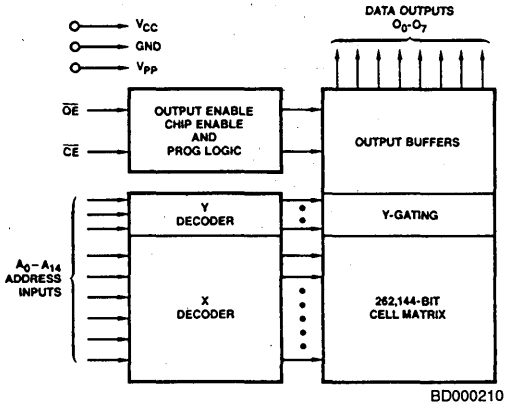
## GENERAL DESCRIPTION

The Am27256 is a 262,144 bit UV-light erasable and electrically programmable read-only memory. It is organized as 32,768 words by 8-bits per word. The standard Am27256 offers access time of 250ns, allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention on a multiple-bus microprocessor system, the Am27256 offers separate output enable ($\overline{OE}$) and chip enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random. To reduce programming time, the Am27256 may be programmed using 1ms pulses. Typically, the Am27256 can be programmed in five minutes.

## BLOCK DIAGRAM




BD000210

## MODE SELECT TABLE

| $\overline{CE}$ (20) | $\overline{OE}$ (22) | Ag (24) | $V_{PP}$ (24) | Outputs (11–13, 15–19) | Mode |
|---|---|---|---|---|---|
| L | L | X | $V_{CC}$ | $D_{OUT}$ | Read |
| L | H | X | $V_{CC}$ | High Z | Output Disable |
| H | X | X | $V_{CC}$ | High Z | Standby |
| L | H | X | $V_{PP}$ | $D_{IN}$ | Program |
| H | L | X | $V_{PP}$ | $D_{OUT}$ | Program Verify |
| H | H | X | $V_{PP}$ | High Z | Program Inhibit |
| L | L | H | $V_{CC}$ | Code | Auto Select |

H = HIGH
L = LOW
X = Don't Care

Note: X can be either L or H
$V_H$ = 12.0V ±0.5V

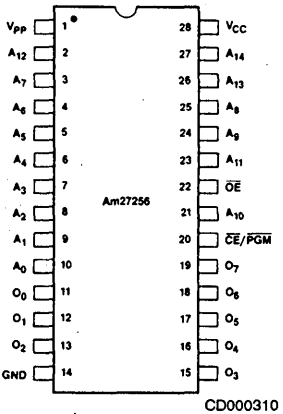
## PRODUCT SELECTOR GUIDE

| Access Time | 170ns | 200ns | | 250ns | | 300ns | | 450ns | |
|---|---|---|---|---|---|---|---|---|---|
| Supply Tolerance | ±5% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% | ±5% | ±10% |
| Part Number | Am27256-1 | Am27256-2 | Am27256-20 | Am27256 | Am27256-25 | Am27256-3 | Am27256-30 | Am27256-4 | Am27256-45 |

6

04069B

## CONNECTION DIAGRAM
### Top View




Note: Pin 1 is marked for orientation

## ORDERING INFORMATION

**Am27256-1 D C**

- C — Temperature: C – Commercial (0°C to +70°C)
- D — Package: D – 28-pin CERDIP
- Speed Select: See Product Selector Guide
- Am27256-1 — Device Type: 32k x 8 EPROM

| Valid Combinations | |
|---|---|
| Am27256-1<br>Am27256-15 | DC |
| Am27256-2<br>Am27256-20<br>Am27256<br>Am27256-3<br>Am27256-30<br>Am27256-4 | DC, DI, DL |
| Am27256-25<br>Am27256-40 | DC, DI, DL,<br>DM |

## ERASING THE Am27256

In order to clear all locations of their programmed contents, it is necessary to expose the Am27256 to an ultraviolet light source. A dosage of 15 Wseconds/cm$^2$ is required to completely erase an Am27256. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm$^2$ for 15 to 20 minutes. The Am27256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27256, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27256, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

## PROGRAMMING THE Am27256

Upon delivery, or after each erasure the Am27256 has all 262,144 bits in the "1", or high state. "0"s are loaded into the Am27256 through the procedure of programming.

The programming mode is entered when 13.0V is applied to the $V_{PP}$ pin, $\overline{OE}$ is at TTL-high and CE is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins.

The flow chart of Page 4 shows the Interactive Programming Algorithm. Interactive algorithms reduce programming time by using short (1ms) program pulses and giving each address only as many pulses as necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. When the data is correctly verified, the address is given an additional 3X ms "overprogram" pulse; where X is a count of the number of 1ms pulse interactions that are required (thus the "over program" pulse can vary from a minimum of 3ms to a maximum of 75ms). This whole process is repeated while sequencing through each address of the Am27256. The algorithm is done at $V_{CC} = V_{PP} = 6V$ to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the final address is completed, the entire EPROM memory is verified at $V_{CC} = V_{PP} = 5V \pm 5\%$.

## AUTO SELECT MODE

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the Am27256.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 (pin 24) of the Am27256. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 (pin 10) from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during Auto Select Mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am27256 these two identifier bytes are given in the table on the next page. All identifiers for manufacturer and device codes will possess odd parity, with the MSB ($O_7$) defined as the parity bit.

## READ MODE

The Am27256 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs ($t_{OE}$) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The Am27256 has a standby mode which reduces the active power dissipation by 80%, from 525mW to 130mW (values for 0 to +70°C). The Am27256 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

## OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAM INHIBIT

Programming of multiple Am27256s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ or $\overline{OE}$, all like inputs of the parallel Am27256s may be common. A TTL low-level program pulse applied to an Am27256's $\overline{CE}$ input with $V_{PP}$ at 12.5V and $\overline{OE}$ high will program that Am27256. A high-level $\overline{CE}$ input inhibits the other Am27256s from being programmed.

## PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}$ at $V_{IL}$, $\overline{CE}$ at $V_{IH}$ and $V_{PP}$ at 12.5V to 13.3V.

## SYSTEM APPLICATIONS

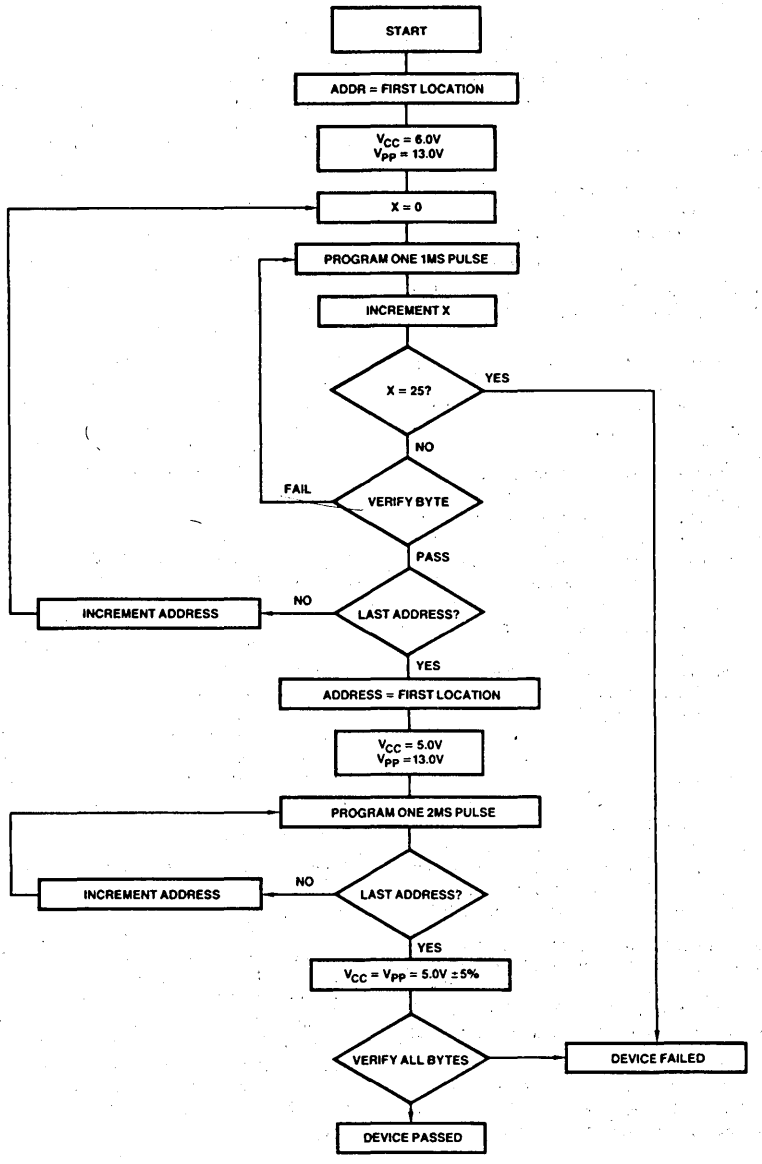
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

**IDENTIFIER BYTES**

| Identifier | $A_0$ (10) | $O_7$ (19) | $O_6$ (18) | $O_5$ (17) | $O_4$ (16) | $O_3$ (15) | $O_2$ (13) | $O_1$ (12) | $O_0$ (11) | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | $V_{IL}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| Device Code | $V_{IH}$ | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04 |

Notes: 1. Ag = 12.0V ±0.5V
2. $A_1 - A_6$, $A_{10} - A_{14}$, $\overline{CE}$, $\overline{OE} = V_{IL}$.

## INTERACTIVE PROGRAMMING FLOW CHART

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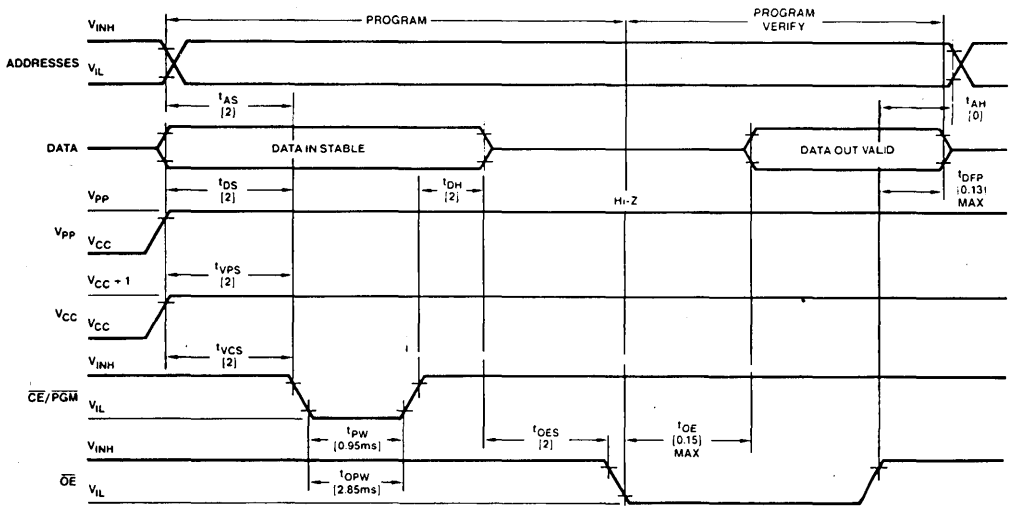
## PROGRAMMING

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | | 10 | µA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | | 0.8 | Volts |
| $V_{IH}$ | Input High Level | | 2.0 | | $V_{CC}$ + 1 | Volts |
| $V_{OL}$ | Output Low Voltage During Verify | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH}$ = -400µA | 2.4 | | | Volts |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Program and Verify) | | | | 100 | mA |
| $I_{PP2}$ | $V_{PP}$ Supply Current (Program) | CE = $V_{IL}$ | | | 30 | mA |
| $V_{ID}$ | $A_9$ Auto Select Voltage | | 11.5 | | 12.5 | Volts |
| $t_{AS}$ | Address Setup Time | | 2 | | | µs |
| $t_{OES}$ | $\overline{OE}$ Setup Time | | 2 | | | µs |
| $t_{DS}$ | Data Setup Time | | 2 | | | µs |
| $t_{AH}$ | Address Hold Time | | 0 | | | µs |
| $t_{DH}$ | Data Hold Time | | 2 | | | µs |
| $t_{DFP}$ (Note 3) | Output Enable to Output Float Delay | | 0 | | 130 | ns |
| $t_{VPS}$ | $V_{PP}$ Setup Time | | 2 | | | µs |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | | µs |
| $t_{PW}$ | $\overline{CE}/\overline{PGM}$ Initial Program Pulse Width | | 0.95 | 1.0 | 1.05 | ms |
| $t_{OPW}$ | $\overline{CE}/\overline{PGM}$ Overprogram Pulse Width | (see Note 2) | 1.95 | | 78.85 | ms |
| $t_{OE}$ | Data Valid from $\overline{OE}$ | | | | 150 | ns |

Notes: 1. *Caution: If $V_{CC}$ is not applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$, the Am27256 could be damaged.*
2. When programming the Am27256, a 0.1µF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.
3. This parameter is only sampled and not 100% tested.

## INTERACTIVE PROGRAMMING ALGORITHM WAVEFORMS (Notes 1, 2 and 3)

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Notes: 1. All times shown in [ ] are minimum and in µsec unless otherwise specified.
2. The input timing reference level is .8V for a $V_{IL}$ and 2V for a $V_{IH}$.
3. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +125°C
Ambient Temperature with
Power Applied ..... −10°C to +80°C
Voltage on all inputs ..... +6.25V to −0.6V
$V_{PP}$ Supply Voltage with Respect to
Ground During Programming ..... +13.5V to −0.6V
Voltage on pin 24 ..... +13.5V to −0.6V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature ..... 0°C to +70°C

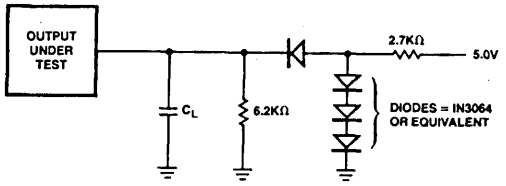
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0v to 5.5V | | | 10 | μA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to 5.5V | | | 10 | μA |
| $I_{PP1}$ | $V_{PP}$ Current Read (Note 2) | $V_{PP}$ = 5.5V | | | 5 | mA |
| $I_{CC1}$ | $V_{CC}$ Standby Current (Notes 2, 6) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ | | | 25 | mA |
| $I_{CC2}$ | $V_{CC}$ Active Current (Note 2) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | | | 100 | mA |
| $V_{IL}$ | Input Low Voltage | | −0.1 | | +0.8 | Volts |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{CC}$+1 | Volts |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400μA | 2.4 | | | Volts |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 4 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 8 | 12 | pF |

## SWITCHING TEST CIRCUIT




TC000130

$C_L$ = 100pF, including jig capacitance

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

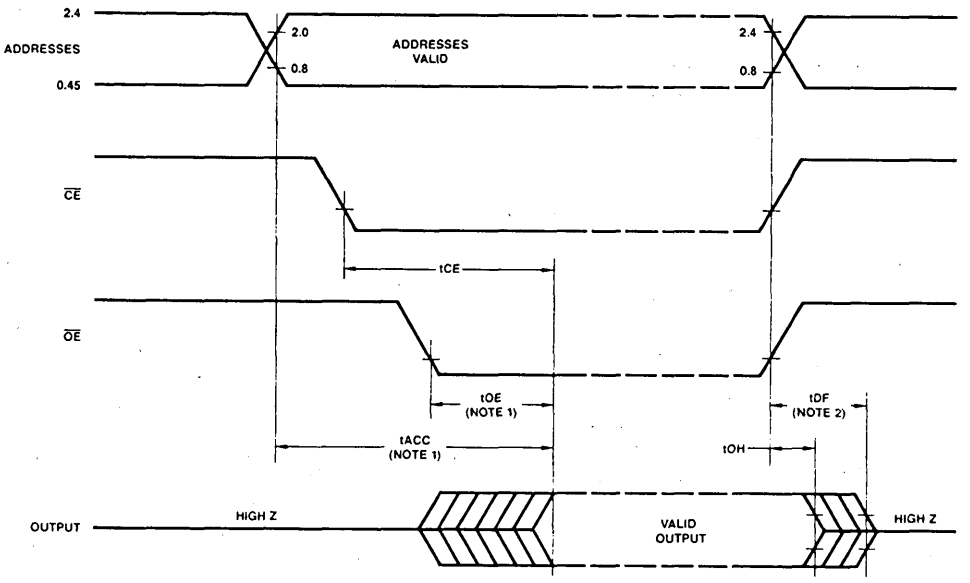
| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 27256-15 27256-1 | Maximum Values 27256-20 27256-2 | Maximum Values 27256-25 27256 | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1TTL gate and $C_L$ = 100pF<br>Input Rise and Fall Times ≤ 20ns<br>Input Pulse levels: 0.45 to 2.4V<br>Timing Measurement Reference Level:<br>Inputs: 1V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 170 | 200 | 250 | ns |
| 2 | $t_{CE}$ | Chip Enable to Output Delay | | $\overline{OE} = V_{IL}$ | | 170 | 200 | 250 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 75 | 75 | 100 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | 0 | 60 | 60 | 60 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | | ns |

| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 27256-30 27256-3 | Maximum Values 27256-45 27256-4 | Units |
|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1TTL gate and $C_L$ = 100pF<br>Input Rise and Fall Times ≤ 20ns<br>Input Pulse levels: 0.45 to 2.4V<br>Timing Measurement Reference Level:<br>Inputs: 1V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 2 | $t_{CE}$ | Chip Enable to Output Delay | | $\overline{OE} = V_{IL}$ | | 300 | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 120 | 150 | ns |
| 4 | $t_{DF}$ (Note 4) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | 0 | 105 | 130 | ns |
| 5 | $t_{OH}$ (Note 4) | Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | ns |

Notes:

1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. $V_{PP}$ may be connected directly to $V_{CC}$ except during programming. The supply would then be the sum of $I_{CC}$ and $I_{PP1}$.
3. Typical values are for nominal supply voltages.
4. This parameter is only sampled and not 100% tested.
5. Caution: The Am27256 must not be removed from or inserted into a socket or board when $V_{PP}$ or $V_{CC}$ is applied.
6. $I_{CC1}$ max is 40mA for 27256-4.

## SWITCHING WAVEFORMS

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Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

# Am27512

65,536 x 8-Bit UV Erasable PROM

PRELIMINARY

## DISTINCTIVE CHARACTERISTICS

- Fast access time — as low as 250ns
- Programming voltage: 12.5V
- low Power consumption
  - Active: 525mW
  - Standby: 132mW
- Single 5V power supply
- ±10% $V_{CC}$ supply tolerance available
- Fully static operation – no clocks
- Separate chip enable and output enable controls
- TTL compatible inputs/outputs
- 28-pin JEDEC approved Am27512 pin-out
- Pin compatible to Am2764, Am27256, Am27128 EPROMS and Am92256 – 256K ROM
- Fast programming time
- Auto select mode for automated programming

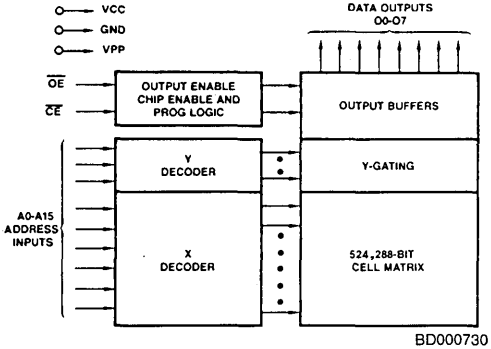
## GENERAL DESCRIPTION

The Am27512 is a 524,288 bit UV-light erasable and electrically programmable read-only memory. It is organized as 65,536 words by 8-bits per word. The standard Am27512 offers a fast 250ns access time allowing operation with high-speed microprocessors without any WAIT state.

To eliminate bus contention in a multi-bus microprocessor system, the Am27512 offers separate Output Enable ($\overline{OE}$) and Chip Enable ($\overline{CE}$) controls.

All signals are TTL levels, including programming signals. Bit locations may be programmed singly, in blocks or at random. To reduce programming time, the Am27512 may be programmed using 1ms pulses. The Am27512 can be programmed in as little as six minutes.

## BLOCK DIAGRAM

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## MODE SELECT TABLE

| Inputs | | | Output | Mode |
|---|---|---|---|---|
| $\overline{CE}/\overline{PGM}$ | $\overline{OE}/V_{PP}$ | $A_9$ | | |
| L | L | X | $D_{OUT}$ | Read |
| L | H | X | HIGH Z | Output Disable |
| H | X | X | HIGH Z | Standby |
| L | $V_{PP}$ | X | $D_{IN}$ | Program |
| L | L | X | $D_{OUT}$ | Program Verify |
| H | $V_{PP}$ | X | HIGH Z | Program Inhibit |
| L | L | H | CODE | Auto Select |

## PRODUCT SELECTOR GUIDE

| Part Number | Am27512 | Am27512-25 | Am27512-3 | Am27512-30 | Am27512-45 |
|---|---|---|---|---|---|
| Supply Voltage | 5V±5% | 5V±10% | 5V±5% | 5V±10% | 5V±10% |
| Access Time | 250ns | | 300ns | | 450ns |
| Chip Enable Delay | 250ns | | 300ns | | 450ns |
| Output Enable Delay | 100ns | | 120ns | | 150ns |

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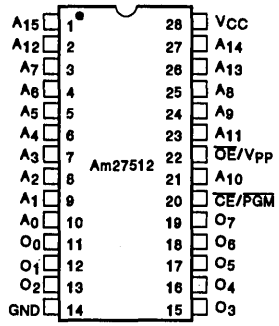
## CONNECTION DIAGRAM
### Top View

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Note: Pin 1 is marked for orientation

$A_0 - A_{15}$: Address
$O_0 - O_7$: Outputs
$\overline{OE}/V_{PP}$: Output Enable/$V_{PP}$
$\overline{CE}/\overline{PGM}$: Chip Enable/Program

## ORDERING INFORMATION

**Am27512-25 D C**

- C — Temperature
  - C – Commercial (0°C to +70°C)
  - I – Industrial (–40°C to +85°C)
  - L – Extended (–55°C to +100°C)
  - M – Military (–55°C to +125°C)
- D — Package
  - D – 28-pin CERDIP
- 25 — Speed Select
  - No code, Am27512-25 } 250ns
  - Am27512-3, Am27512-30 } 300ns
  - Am27512-45 450ns
- Am27512 — Device Type
  - 8-bit UV erasable PROM

| Valid Combinations | |
|---|---|
| Am27512-3<br>Am27512-30 | DC, DI, DL |
| No Code<br>Am27512-25<br>Am27512-45 | DC, DI,<br>DL, DM |

## ERASING THE Am27512

In order to clear all locations of their programmed contents, it is necessary to expose the Am27512 to an ultraviolet light source. A dosage of 15 Wseconds/cm$^2$ is required to completely erase an Am27512. This dosage can be obtained by exposure to an ultraviolet lamp [(wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm$^2$ for 15 to 20 minutes. The Am27512 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27512, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27512 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

## PROGRAMMING THE Am27512

Upon delivery, or after each erasure, the Am27512 has all 65,536 bytes in the "1," or high state. "0"s are loaded into the Am27512 through the procedure of programming.

The programming mode is entered when 12.5V is applied to the $\overline{OE}/V_{PP}$ pin, and $\overline{CE}/\overline{PGM}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins.

The flow chart on Page 6 shows the Interactive Programming Algorithm. Interactive algorithms reduce programming time by using short (1ms) program pulses and giving each address only as many pulses as necessary in order to reliably program the data. After each pulse is applied to a given address, the data in that address is verified. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the Am27512. This part of the algorithm is done at $V_{CC}$ = 6.0V to assure that each EPROM bit is programmed to a sufficiently high threshold voltage. After the entire memory has been programmed with the 1ms program pulse, the entire memory is given an additional "overprogram" by cycling through each address and applying an additional 2ms program pulse. After the final address is completed, the entire EPROM memory is verified at $V_{CC}$ = 5V±5%.

## AUTO SELECT MODE

The Auto Select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the Am27512.

To activate this mode, the programming equipment must force 11.5 to 12.5V on address line $A_{PP}$(pin 24) of the Am27512. Two identifier bytes may then be sequenced from the device outputs by toggling address line $A_0$ (pin 10) from $V_{IL}$ to $V_{IH}$. All other address lines must be held at $V_{IL}$ during Auto Select Mode.

Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am27512 these two identifier bytes are given in the table on the next page. All identifiers for manufacturer and device codes will possess odd parity, with the MSB ($O_7$) defined as the parity bit.

## READ MODE

The Am27512 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs $t_{OE}$ after the falling edge of OE, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

## STANDBY MODE

The Am27512 has a standby mode which reduces the active power dissipation by 75% from 525mW to 132mW (values for 0 to +70°C). The Am27512 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

## OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2 line control function is provided to allow for:
1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

## PROGRAM INHIBIT

Programming of multiple Am27512s in parallel with different data is also easily accomplished. Except for $\overline{CE}/\overline{PGM}$, all like inputs including $\overline{OE}/V_{pp}$ of the parallel Am27512s may be common. A TTL low-level program pulse applied to an Am27512s $\overline{CE}/\overline{PGM}$ input with $\overline{OE}/V_{PP}$ at 12.5V will program that Am27512. A high-level $\overline{CE}/\overline{PGM}$ inputs inhibits the other Am27512s from being programmed.

## PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify must be performed with $\overline{OE}/V_{PP}$ and $\overline{CE}/\overline{PGM}$ at $V_{IL}$. Data should be verified $t_{DV}$ after the falling edge of $\overline{CE}$.

## SYSTEM APPLICATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. A 0.1μF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between $V_{CC}$ and GND to minimize transient effects. In addition, to overcome the voltage droop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7μF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −10°C to +135°C
Voltage on All Inputs and $V_{CC}$
with Respect to GND ..... +6.25V to −0.6V
$V_{PP}$ Supply Voltage with Respect
to Ground During Programming ..... +13.5V to −0.6V
Voltage on Pin 24 with Respect
to Ground ..... +13.5V to −0.6V

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Temperature
Commercial ..... 0°C to +70°C
Industrial ..... −40°C to +85°C
Extended ..... −55°C to +100°C
Military ..... −55°C to +125°C

Supply Voltages
Am27512, -3, -4 ..... +4.75V to +5.25V
Am27512, -25, -30, -45 ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Symbol | Parameter | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN}$ = 0V to 5.5V | | | | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = 0V to 5.5V | | | | 10 | µA |
| $I_{CC1}$ | $V_{CC}$ Standby Current (Note 5) | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IL}$ | C devices | | | 25 | mA |
| | | | M devices | | | 40 | |
| $I_{CC2}$ | $V_{CC}$ Active Current (Note 5) | $\overline{OE}$ = $\overline{CE}$ = $V_{IL}$ | C devices | | | 100 | mA |
| | | | M devices | | | 120 | |
| $V_{IL}$ | Input Low Voltage | | | −0.1 | | +0.8 | Volts |
| $V_{IH}$ | Input High Voltage | | | 2.0 | | $V_{CC}$+1 | Volts |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.1mA | | | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = −400µA | | 2.4 | | | Volts |
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V (Note 3) | | | 5 | 7 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V (Note 3) | | | 8 | 12 | pF |
| $C_{IN2}$ | $\overline{OE}$/$V_{PP}$ Input Capacitance | $V_{IN}$ = 0V (Note 3) | | | 12 | 20 | pF |
| $C_{IN3}$ | $\overline{CE}$/$\overline{PGM}$ Input Capacitance | $V_{IN}$ = 0V (Note 3) | | | 9 | 12 | pF |

Notes:

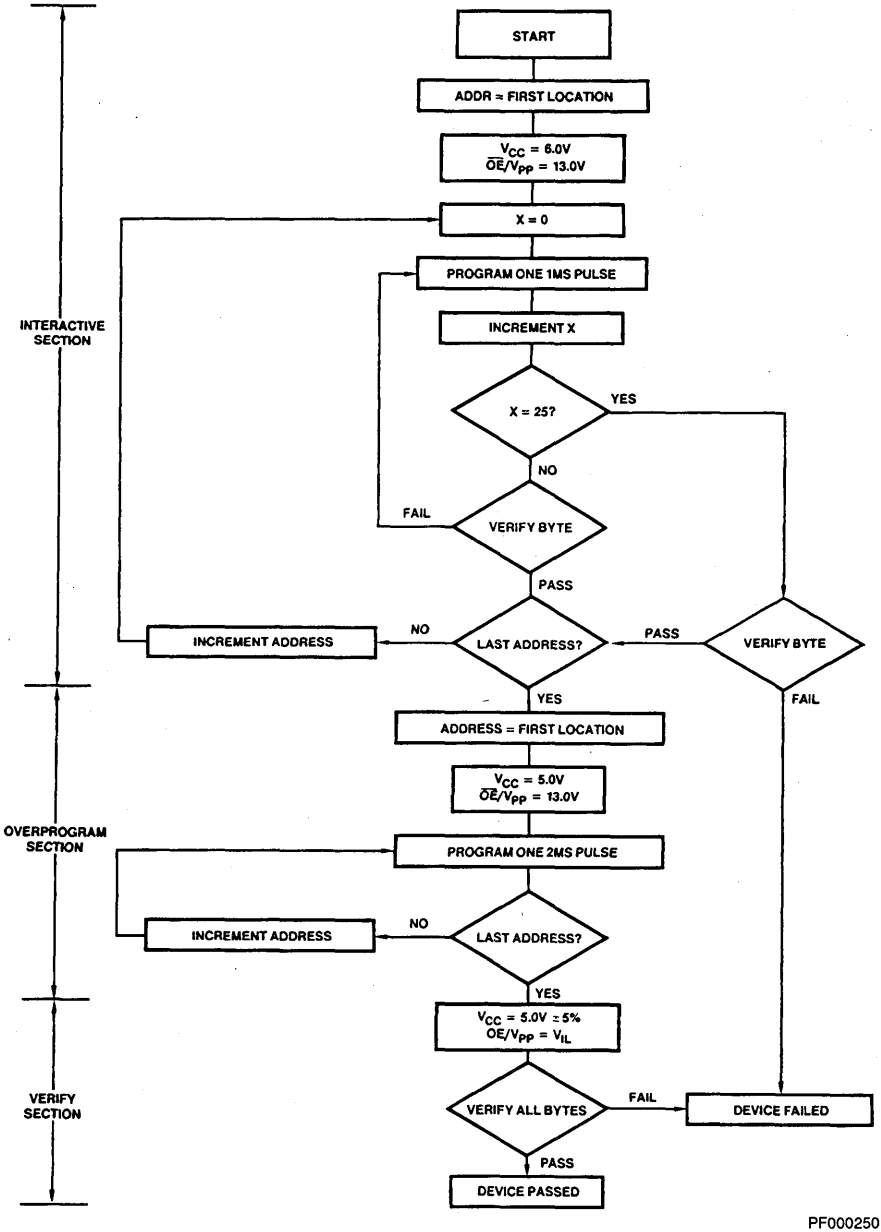
1. $V_{CC}$ must be applied simultaneously or before $V_{PP}$ and removed simultaneously or after $V_{PP}$.
2. Typical values are for nominal supply voltages.
3. This parameter is only sampled and not 100% tested.
4. Caution: The Am27512 must not be removed from or inserted into a socket or board when Vpp or $V_{PP}$ is applied.
5. $I_{CC1}$ max is 40mA and $I_{CC2}$ max is 120mA for Am27512-45.

### IDENTIFIER BYTES

| Identifier | $A_0$ (10) | $O_7$ (19) | $O_6$ (18) | $O_5$ (17) | $O_4$ (16) | $O_3$ (15) | $O_2$ (13) | $O_1$ (12) | $O_0$ (11) | Hex Data |
|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer Code | L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01 |
| Device Code | H | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 85 |

Notes: 1. $A_9$ = 12.0V ±0.5V.
2. $A_1$ − $A_6$, $A_{10}$ − $A_{15}$, $\overline{CE}$, $\overline{OE}$ = $V_{IL}$.
3. $A_{14}$=Don't Care.

## INTERACTIVE PROGRAMMING FLOW CHART




PF000250

## INTERACTIVE PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

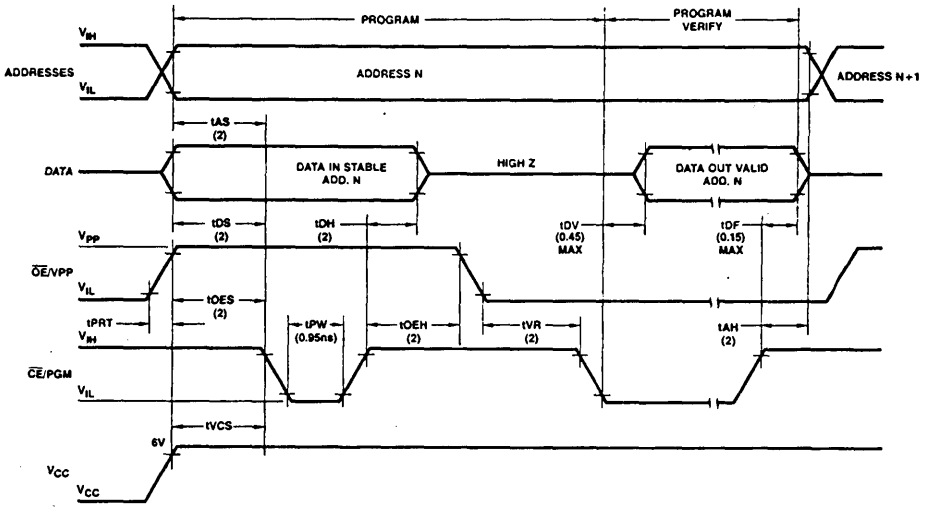
| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Current (All Inputs) | $V_{IN} = V_{IL}$ or $V_{IH}$ | | 10 | μA |
| $V_{OL}$ | Output Low Voltage During Verify | $I_{OL} = 2.1$ mA | | 0.45 | Volts |
| $V_{OH}$ | Output High Voltage During Verify | $I_{OH} = -400$μA | 2.4 | | Volts |
| $I_{CC}$ | $V_{CC}$ Supply Current (Program and Verify) | | | 150 | mA |
| $V_{IL}$ | Input Low Level (All Inputs) | | -0.1 | 0.8 | Volts |
| $V_{IH}$ | Input High Level (All Inputs Except $\overline{OE}/V_{PP}$) | | 2.0 | $V_{CC}+1$ | Volts |
| $I_{PP}$ | $V_{PP}$ Supply Current (Program) | $\overline{CE} = V_{IL}$, $\overline{OE}/V_{PP} = 12.5V$ | | 30 | mA |
| $V_{ID}$ | $A_9$ Auto Select Voltage | | 11.5 | 12.5 | Volts |

## SWITCHING PROGRAMMING CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address Setup Time | Input tR and tF (10% to 90%) = 20ns<br>Input Signal Levels = 0.8 to 2.2V<br>Timing Measurement Reference Level:<br>Inputs: 1V and 2V<br>Outputs: 0.8V and 2V | 2 | | μS |
| $t_{OES}$ | Output Enable Setup Time | | 2 | | μS |
| $t_{DS}$ | Data Setup Time | | 2 | | μS |
| $t_{AH}$ | Address Hold Time | | 2 | | μS |
| $t_{OEH}$ | Output Enable Hold Time | | 2 | | μS |
| $t_{DH}$ | Data Hold Time | | 2 | | μS |
| $t_{DF}$ (Note 2) | Chip Enable to Output Float Delay | | 0 | 150 | ns |
| $t_{DV}$ (Note 2) | Data Valid from $\overline{CE}$ ($\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$) | | | 450 | ns |
| $t_{PW}$ | Program Pulse Width | | .95 | 3.15 | ms |
| $t_{PRT}$ | Program Pulse Rise Time | | 50 | | ns |
| $t_{VR}$ | $V_{PP}$ Recovery Time | | 2 | | μS |
| $t_{VCS}$ | $V_{CC}$ Setup Time | | 2 | | μS |

Notes:
1. When programming the Am27512, a 0.1μF capacitor is required across $\overline{OE}/V_{PP}$ and ground to suppress spurious voltage transients which may damage the device.
2. This parameter is only sampled and is not 100% tested.

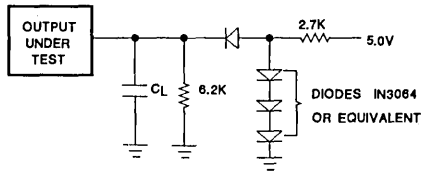
## PROGRAM WAVEFORMS




WF001330

Notes: 1. All times shown in ( ) are minimum in μsec unless otherwise specified.
2. $t_{DV}$ and $t_{DF}$ are characteristics at the device but must be accommodated by the programmer.

## SWITCHING TEST CIRCUIT



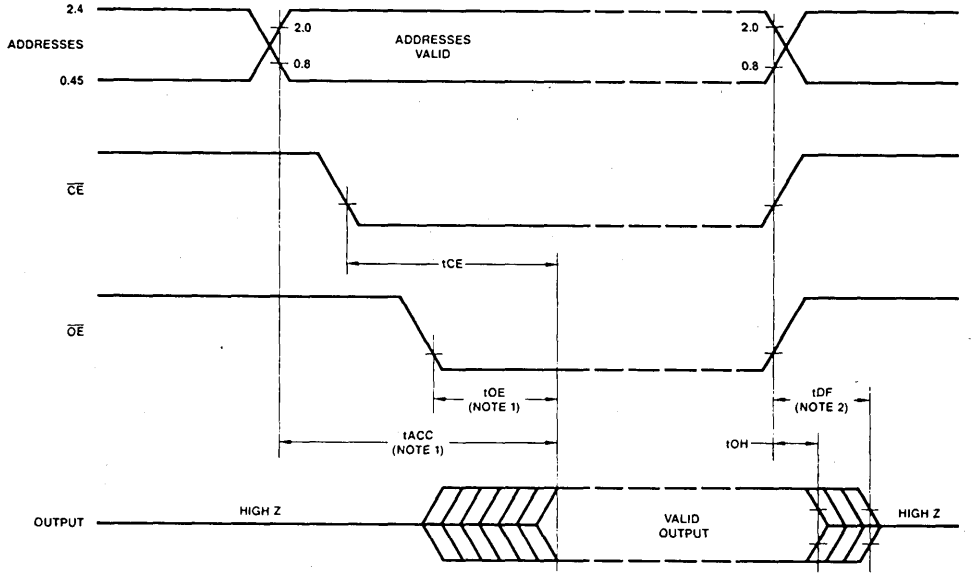

TC00025R

$C_L$ = 100pF, including jig capacitance.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified

| No. | Symbol | Description | Test Conditions | | Min Values All Types | Maximum Values 27512-25 27512 | Maximum Values 27512-30 27512-3 | Maximum Values 27512-45 | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | $t_{ACC}$ | Address to Output Delay | Output load: 1TTL gate and $C_L$ = 100pF<br>Input Rise and Fall Times ≤ 20ns<br>Input Pulse Levels: 0.45 to 2.4V<br>Timing Measurement Reference Level:<br>Inputs: 1V and 2V<br>Outputs: 0.8V and 2V | $\overline{CE} = \overline{OE} = V_{IL}$ | | 250 | 300 | 450 | ns |
| 2 | $t_{CE}$ | Chip Enable to Output Delay | | $\overline{OE} = V_{IL}$ | | 250 | 300 | 450 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Delay | | $\overline{CE} = V_{IL}$ | | 100 | 120 | 150 | ns |
| 4 | $t_{DF}$ (Note 3) | Output Enable High to Output float | | $\overline{CE} = V_{IL}$ | 0 | 60 | 105 | 130 | ns |
| 5 | $t_{OH}$ (Note 3) | Output Hold from Addresses,CE orOE Whichever Occured First | | $\overline{CE} = \overline{OE} = V_{IL}$ | 0 | | | | ns |

## SWITCHING WAVEFORMS




WF001320

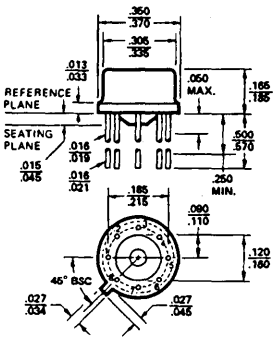
Notes: 1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{OE}$ without impact on $t_{ACC}$.
2. $t_{DF}$ is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

# General Information Index

# Package Outlines

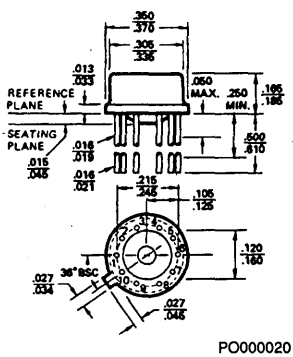
## METAL CAN PACKAGES

### H-8-1



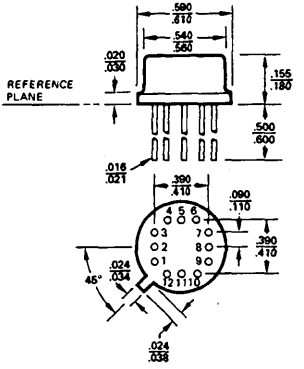

PO000010

### H-10-1




PO000020

### G-12-1

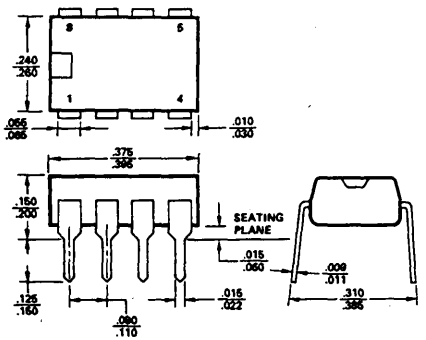



PO000030

Note. Standard lead finish is bright acid tin plate or gold plate.

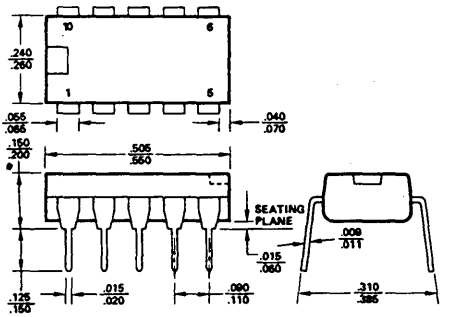
## MOLDED DUAL IN-LINE PACKAGES

### P-8-1



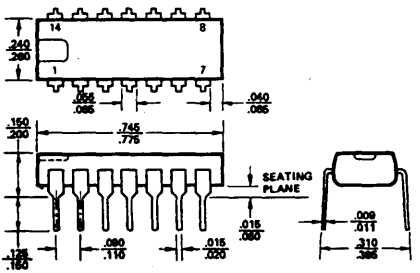

PO000040

### P-10-1



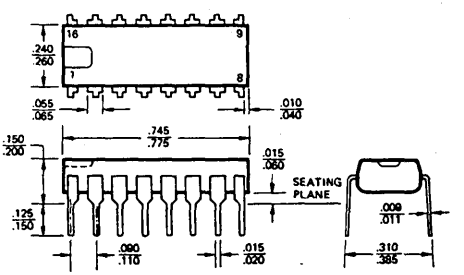

PO000050

### P-14-1




PO000060

### P-16-1




PO000070

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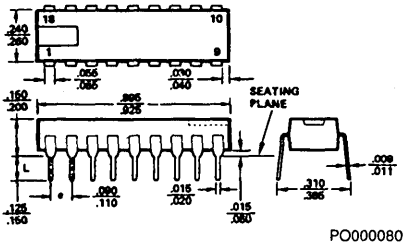
## Package Outlines (Cont.)

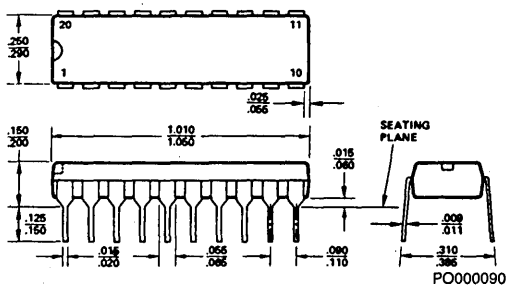
### MOLDED DUAL IN-LINE PACKAGES (Cont.)

P-18-1



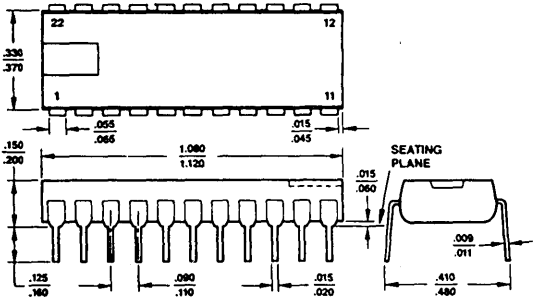

PO000080

P-20-1



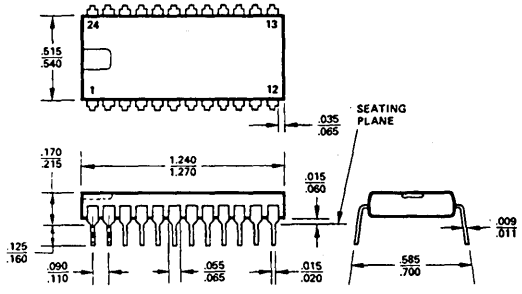

PO000090

P-22-1



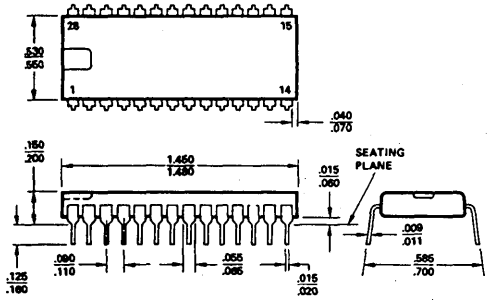

PO000100

P-24-1



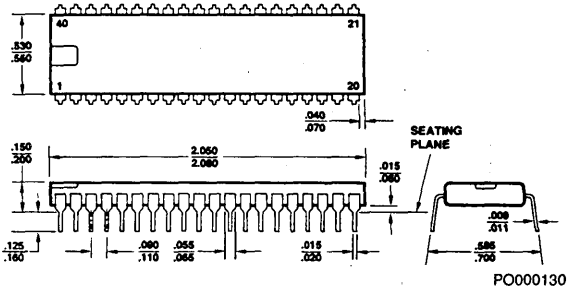

PO000110

P-28-1




PO000120

P-40-1



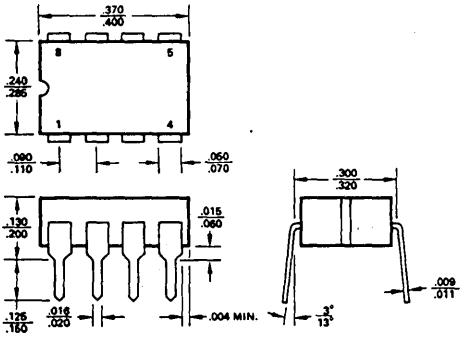

PO000130

Note. Standard lead finish is tin plate or solder dip.

## Package Outlines (Cont.)

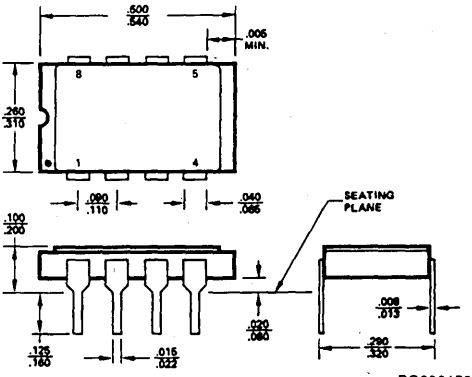
### HERMETIC DUAL IN-LINE PACKAGES

**D-8-1**



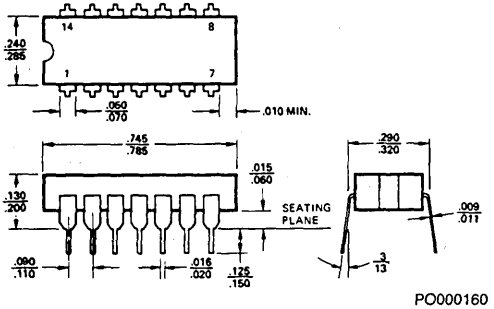

PO000140

**D-8-2**



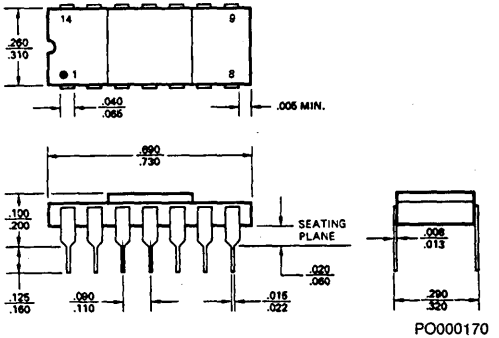

PO000150

**D-14-1**



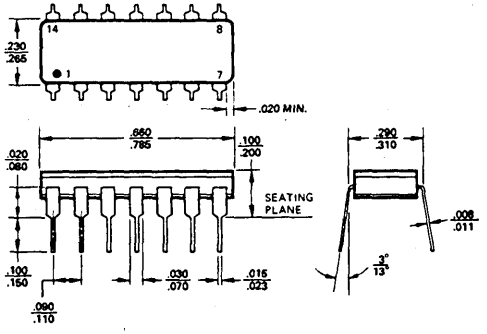

PO000160

**D-14-2**




PO000170

**D-14-3**




PO000180

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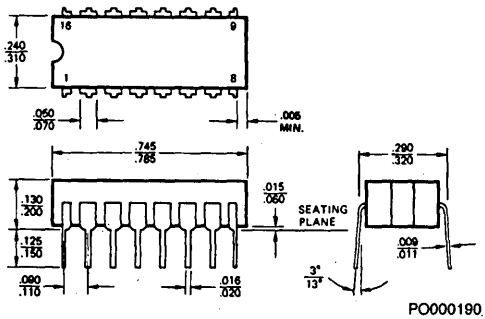
## Package Outlines (Cont.)

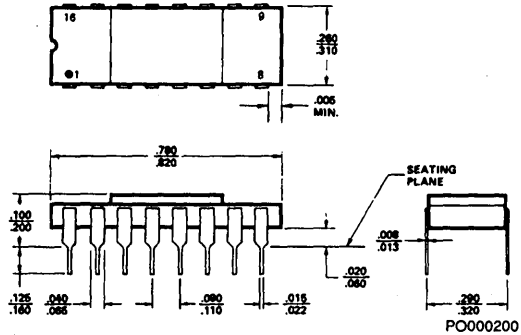
### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

**D-16-1**



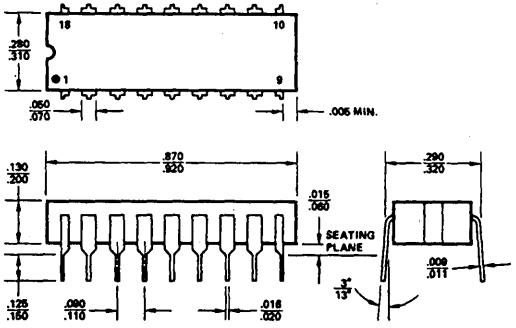

PO000190

**D-16-2**



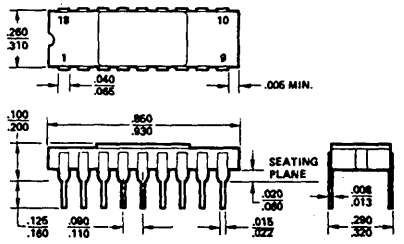

PO000200

**D-18-1**



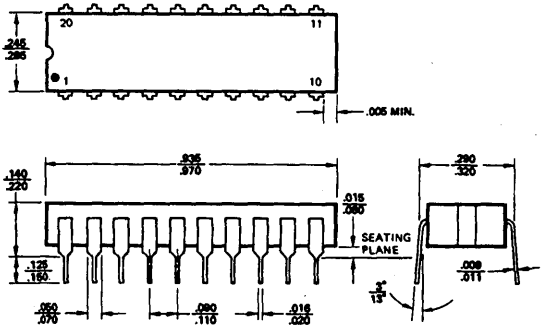

PO000210

**D-18-2**



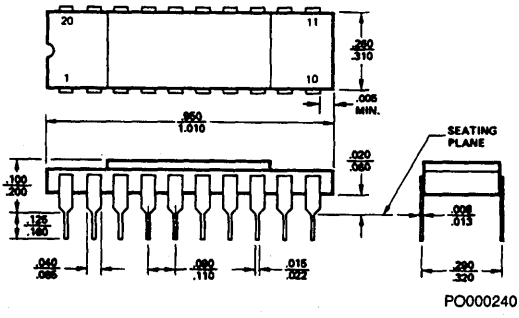

PO000220

**D-20-1**




PO000230

**D-20-2**

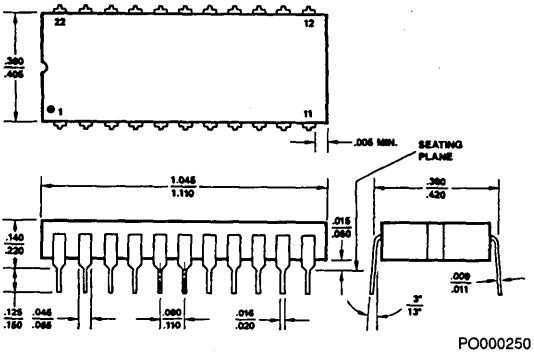



PO000240

## Package Outlines (Cont.)

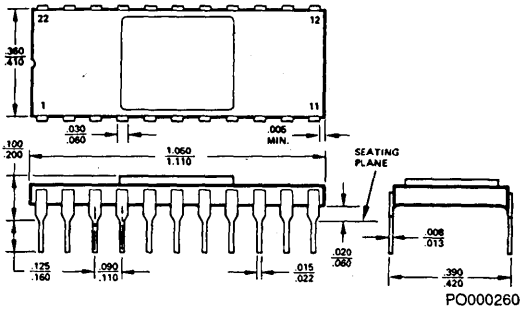
### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

**D-22-1**



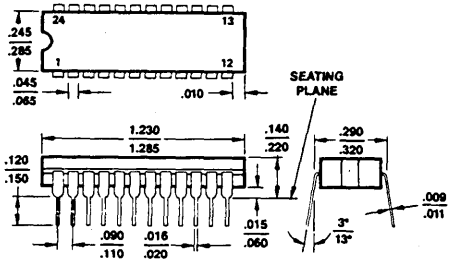

PO000250

**D-22-2**



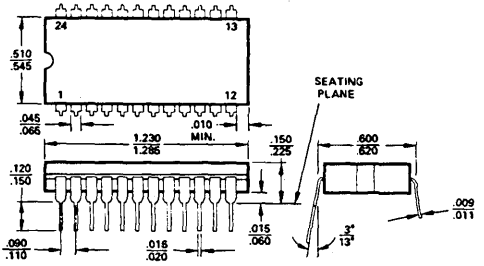

PO000260

**D-24-SLIM**



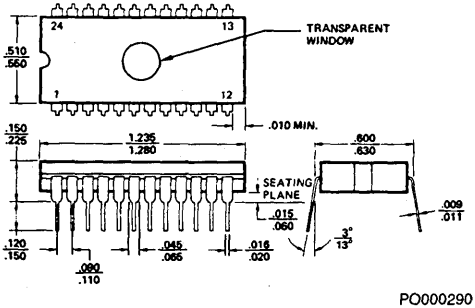

PO000270

**D-24-1 and D-24-4**



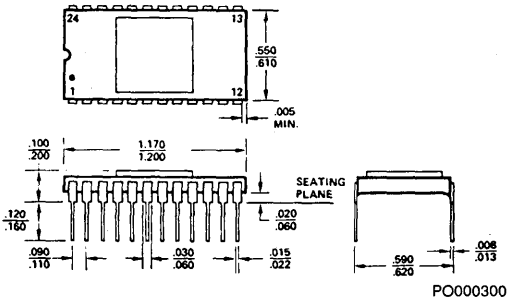

PO000280

**D-24-4**




PO000290

**D-24-2**




PO000300

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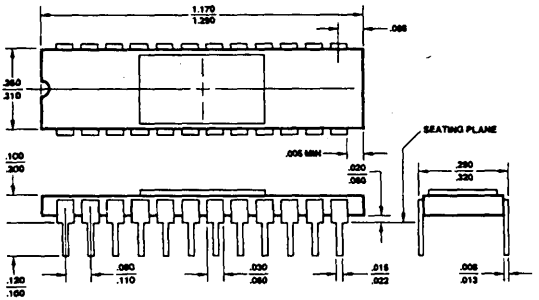
03515C-CPM

## Package Outlines (Cont.)

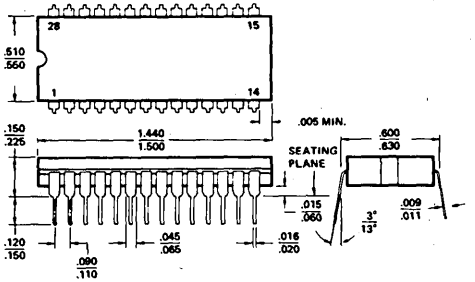
### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

**D-24-2S**



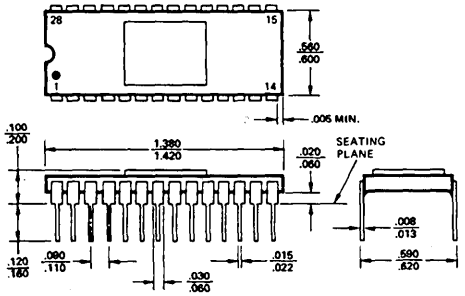

PO000310

**D-28-1**



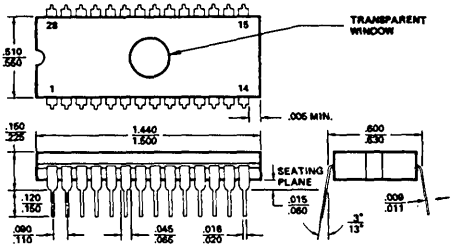

PO000320

**D-28-2**



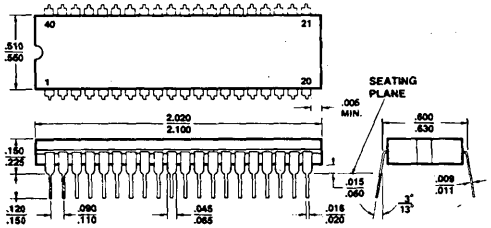

PO000330

**D-28-3**



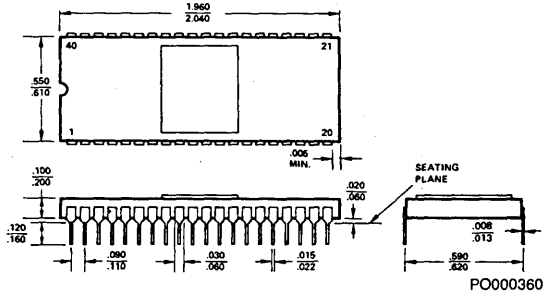

PO000340

**D-40-1**




PO000350

**D-40-2**

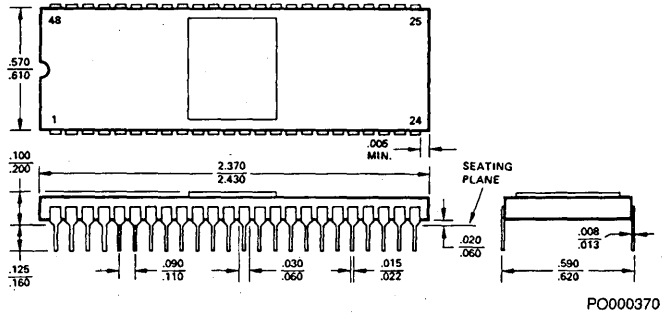



PO000360

## Package Outlines (Cont.)

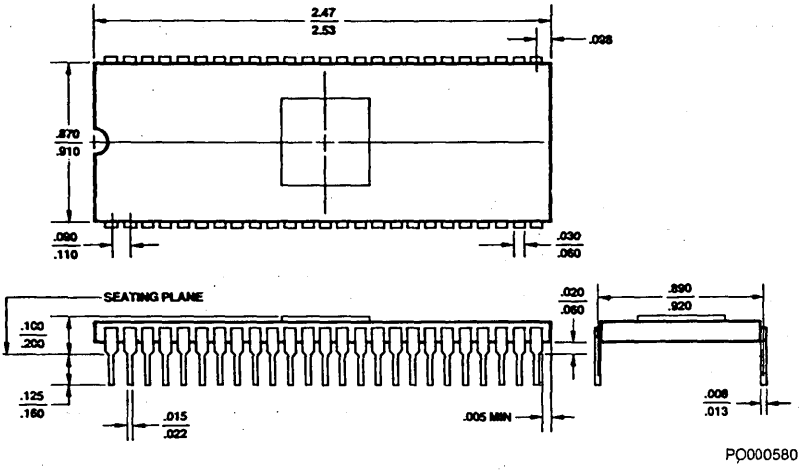
### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

D-48-2



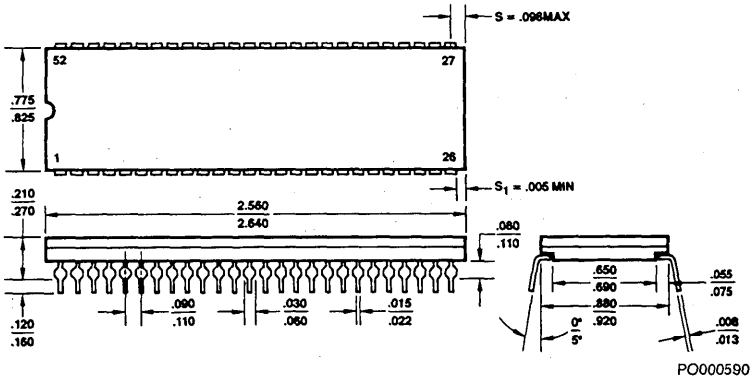

PO000370

D-50-2




PO000580

D-52-3




PO000590

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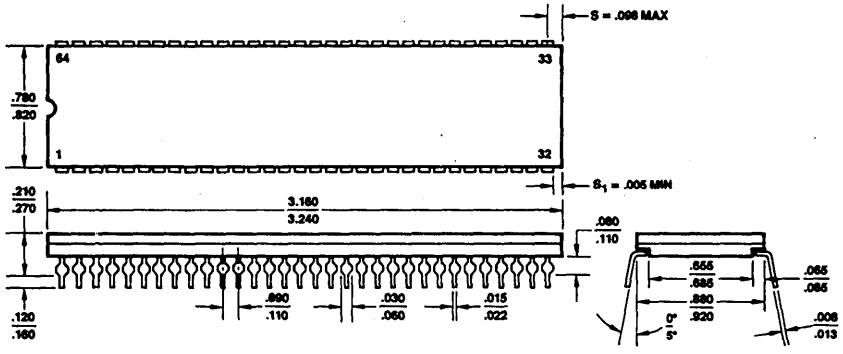
## Package Outlines (Cont.)

### HERMETIC DUAL IN-LINE PACKAGES (Cont.)

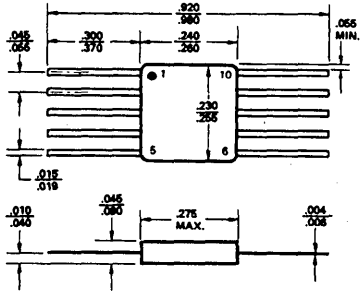
**D-64-3**




PO000600

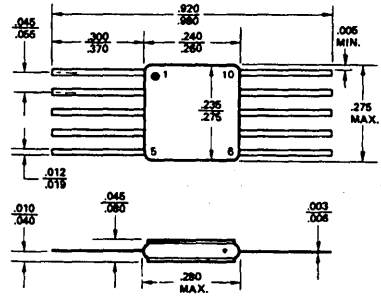
### FLAT PACKAGES

**F-10-1**



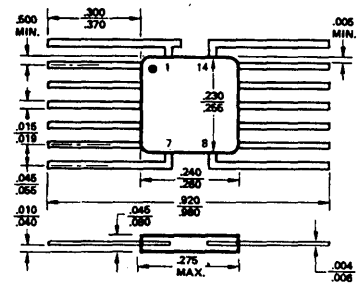

PO000380

**F-10-2**



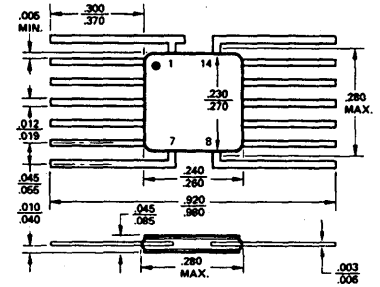

PO000390

**F-14-1**




PO000400

**F-14-2**

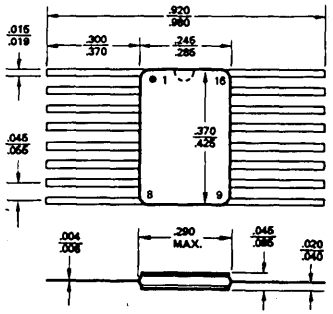



PO000410

## Package Outlines (Cont.)

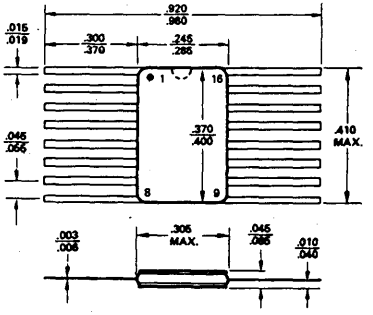
### FLAT PACKAGES (Cont.)

F-16-1




PO000420

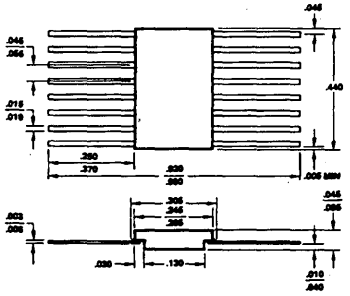
F-16-2




PO000430

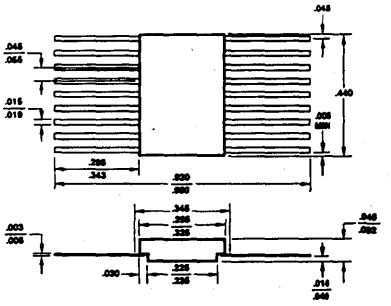
Note: Notch is pin 1 index on cerpack.

F-16-3



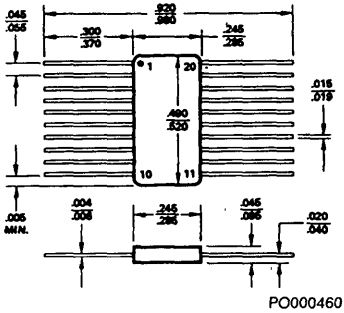

PO000440

F-18-3



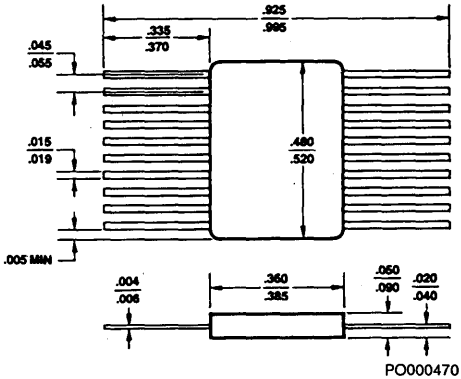

PO000450

F-20-1




PO000460

F-20-1L




PO000470

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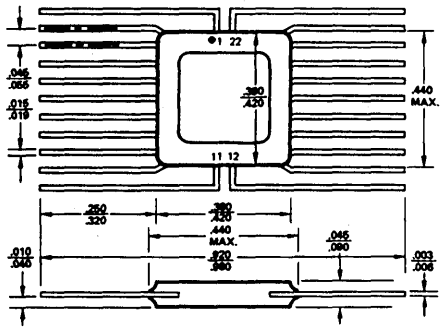
## Package Outlines (Cont.)

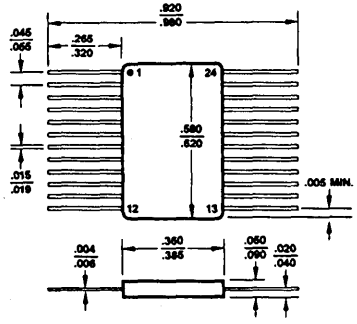
### FLAT PACKAGES (Cont.)

F-22-1



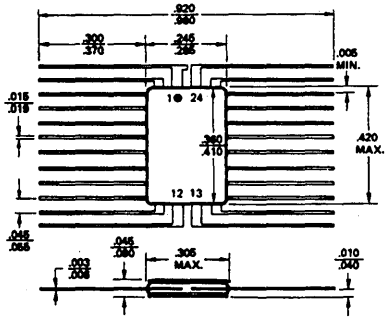
PO000480

F-24-1



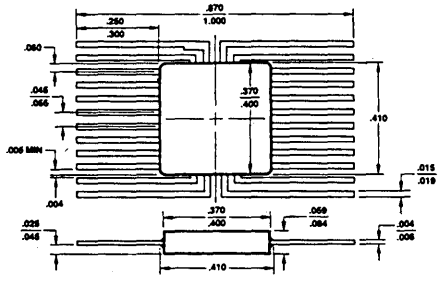
PO000490

F-24-2



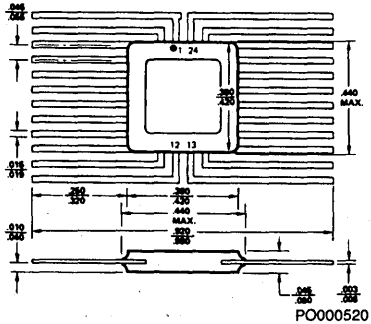
PO000500

F-24-2S



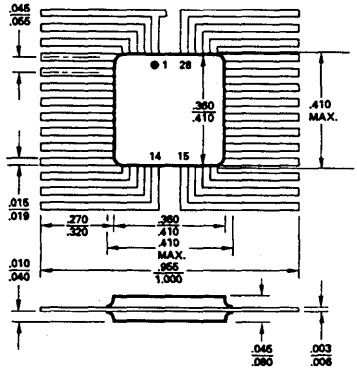
PO000510

F-24-3



PO000520

F-28-1

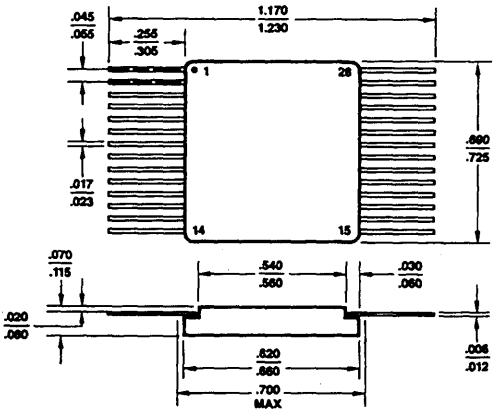


PO000530

## Package Outlines (Cont.)

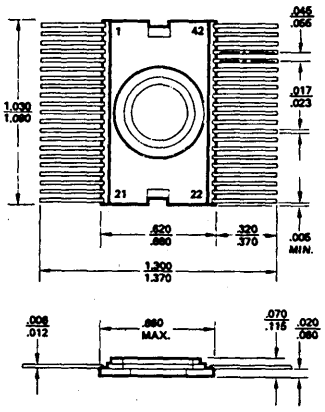
### FLAT PACKAGES (Cont.)

F-28-2 and F-28-3



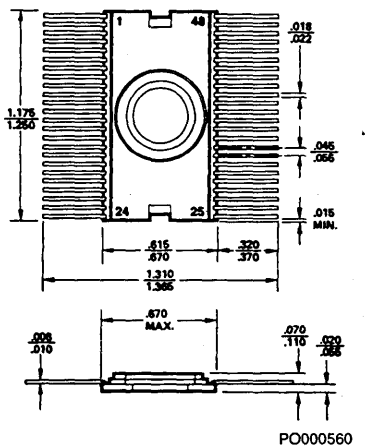

PO000540

F-42-1



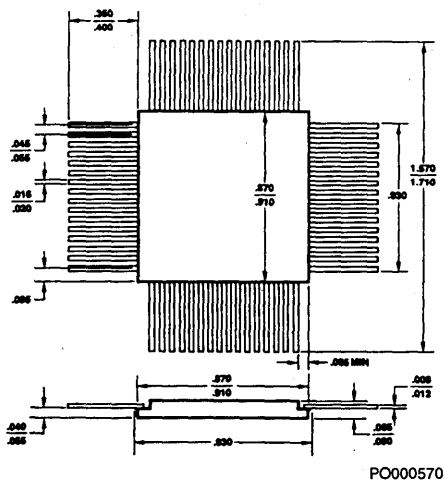

PO000550

F-48-2




PO000560

F-64-3S




PO000570

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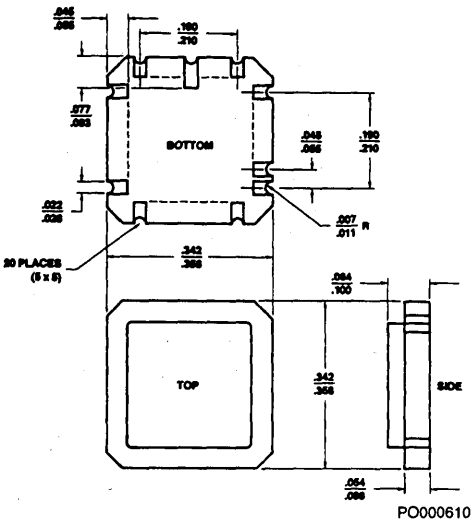
## Package Outlines (Cont.)

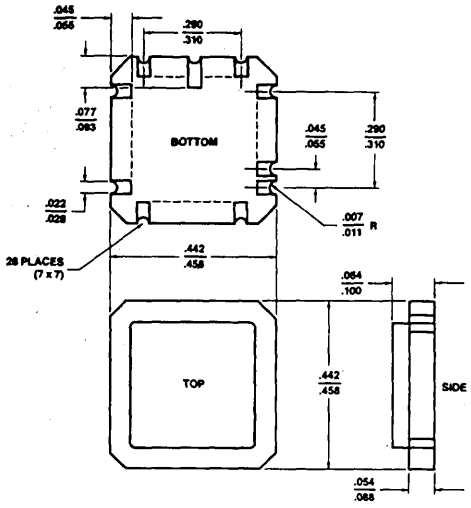
### SQUARE CHIP CARRIER FAMILY

L-20-1



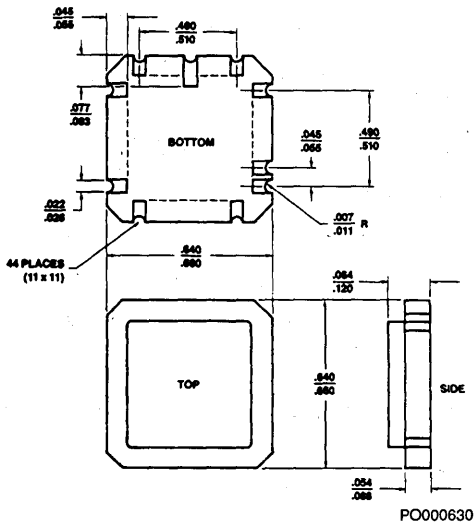

PO000610

L-28-1



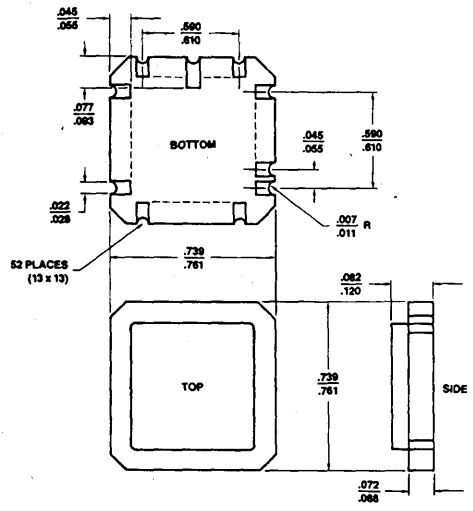

PO000620

L-44-1




PO000630

L-52-1

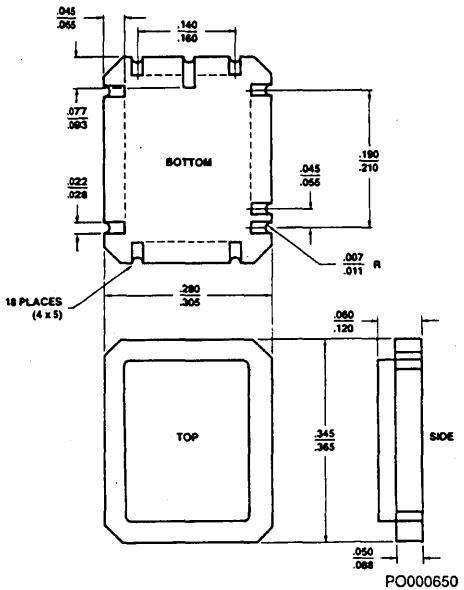



PO000640

## Package Outlines (Cont.)

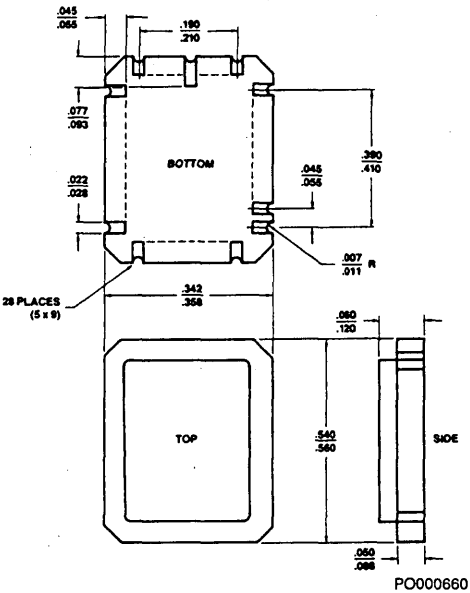
### RECTANGULAR CHIP CARRIER FAMILY

L-18-2



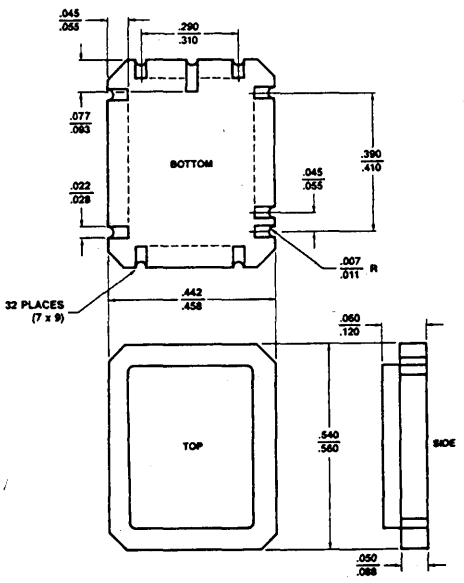

PO000650

L-28-2




PO000660

L-32-2




PO000670

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Advanced Micro Devices maintains a network of representatives and distributors in the U.S. and around the world. Consult the listing below for an address nearest you.

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