GUIDE TO STANDARD MOS PRODUCTS &

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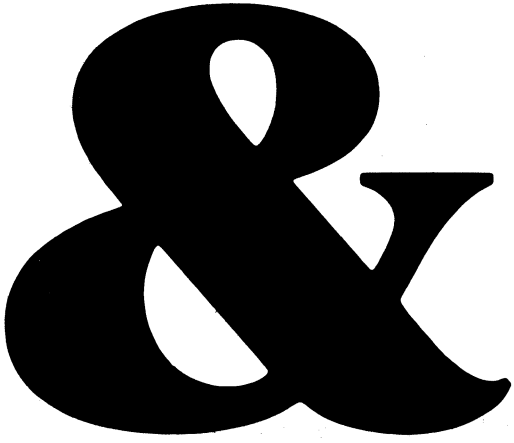
May
1975

AMI

AMI®
AMERICAN MICROSYSTEMS, INC.



- ☐ AMI CUSTOM MOS/LSI CAPABILITIES
- ☐ LIQUID CRYSTAL DISPLAYS
- ☐ WATCHES AND WATCH PRODUCTS
- ☐ DESCRIPTION OF MOS PROCESSES
- ☐ AMI PRODUCT ASSURANCE PROGRAM
- ☐ APPLICATION NOTES

AMERICAN MICROSYSTEMS, INC.

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Information furnished by AMI in this catalog is believed to be accurate and reliable. Devices sold by AMI are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale. AMI makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. AMI reserves the right to change specifications and prices at any time and without notice. **Advanced Product Description** means that this product has not been produced in volume, the specifications are preliminary and subject to change, and device characterization has not been done. Therefore, prior to designing any product into a system, it is necessary to check with AMI for current information.

This catalog prepared for American Microsystems, Inc., by The Vada Company; cover design and interior design by Steven Jacobs Design.

Printed in USA 5-75-50M

EDGE INDEX

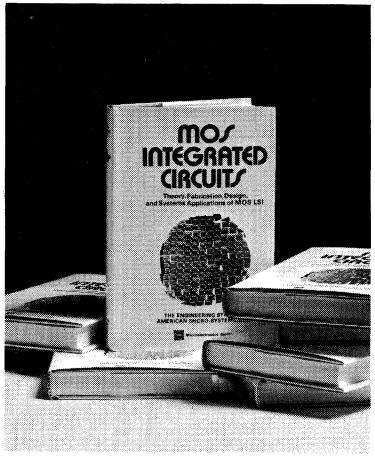
Introduction

Among MOS integrated circuit manufacturers, American Microsystems enjoys a unique position. Besides being the first successful volume producer of MOS integrated circuits (since 1966), AMI today has the largest MOS/LSI design engineering staff in the industry, the most comprehensive manufacturing and product testing facilities, and a more complete repertoire of in-production MOS processes than any other manufacturer. The ability to design, manufacture, and test are the three prerequisites that any manufacturer must have in depth, in order to ship reliable state-of-the-art MOS/LSI products and support successful supplier-user relationships year after year. Because at AMI we excel at all three, in 1974 alone, we shipped over 15,000,000 MOS integrated circuits.

This Guide to Standard MOS Products is the first single volume comprehensive catalog of standard products issued by AMI. We have endeavored to incorporate the best features of organization and content, so that all product data sections and indices are easy to identify by color, and are clearly separated from other information in the catalog. Particular attention was given to the technical data on products, so that it is comprehensive and makes the application of the products easy and convenient for the circuit designer. The catalog also contains other informative technical data, which makes it useful as a general reference to key parts of the MOS technology and its applications. Finally, with the sections on Custom Capabilities, Watches and Watch Products, and the AMI Product Assurance Program, we also present a comprehensive profile of all AMI capabilities.

In the future, as in the past, AMI will be dedicated to serve the advanced MOS/LSI market. In the years ahead, use of MOS will rapidly become more and more pervasive – both in the industrial and consumer sectors – and AMI will commit its full capabilities toward being the Number One producer of MOS products.

How to make it small.



We wrote the book on it.

As the world's largest and most experienced exclusive supplier of MOS/LSI, it's hardly surprising that AMI has produced the only definitive work on the subject.

In it we describe the theory, design, fabrication and systems application of MOS. It's published by Van Nostrand Reinhold, runs 474 pages and costs $18. If you'd like a list of bookstores that carry Van Nostrand books, contact the AMI sales office nearest you. We'll tell you the nearest place to pick up a copy.

And we certainly know how to turn theory into practice. AMI makes more MOS devices than anyone else. Our standard product line includes RAMs, ROMs, shift registers, multiplexers, timing circuits, discretes, music circuits, UARTs, keyboard encoders and character generators. Even liquid crystal displays and drivers, programmable processors, digital clocks, calculator kits.

And if you're looking for a custom circuit, we can help you there, too. We've already designed more than 800 of them. Unlike the other MOS companies, we can use five production processes: P-Channel, N-Channel, Silicon Gate, Ion Implant and C-MOS.

So the next time you're ordering MOS products, specify AMI. We not only make the best circuits on the market. We've also written the book that shows how we make them that good.

American Microsystems, Inc., 3800 Homestead Road, Santa Clara, California 95051.

AMI

AMERICAN MICROSYSTEMS, INC.

Numerical Index

Functional Index

Industry Crossreference Guide

FAIRCHILD

Device No.	AMI Replacement
3337	S1685
3514	S3514
35342	S1103
35345	S1103-1

GENERAL INSTRUMENTS

Device No.	AMI Replacement
AY-5-1013	S1883
R03-16,382	S8996
R05-8192	S8865

INTEL

Device No.	AMI Replacement
1103	S1103
1103-1	S1103-1
1103A	S1103A
1103A-1	S1103A-1
1103A-2	S1103A-2
2146	S146

M.I.L.

Device No.	AMI Replacement
1103	S1103
1103-1	S1103-1
2146	S146

NATIONAL SEMICONDUCTOR

Device No.	AMI Replacement
MM5316	S1998
5232	S5232
5233	S3514

SIGNETICS

Device No.	AMI Replacement
1103	S1103
1103-1	S1103-1
2146	S146

STANDARD MICROSYSTEMS

Device No.	AMI Replacement
COM2017	S1883

TEXAS INSTRUMENTS

Device No.	AMI Replacement
TMS6011	S1883
3113	S2181A
3114	S2181A

WESTERN DIGITAL

Device No.	AMI Replacement
TR1602A	S1883

MOSTEK

Device No.	AMI Replacement
MK2400P	S8773
2500	S5232
2600	S3514
4006	S4006
4008	S4008
4008-9	S4008-9

MOTOROLA

Device No.	AMI Replacement
MC6800	S6800
MC6820	S6820
MC6850	S6850
MCM6810	S6810
MCM6830	S6830
6605L	S6605
6605L-1	S6605A

1

Ordering Information / Packaging

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Mr. Arie Goldstein, General Manager
Mr. E.H. Nuriel, Comp. Sales Manager

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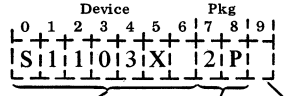
Mr. P.J. Moolman, Mgr. Dir.
Mr. Lionel DuToit, Sales Dir.

Ordering Information

With the distribution of this Guide to Standard MOS Products, AMI is implementing a new simplified ordering system. With this system, it is possible to completely specify any standard device in this catalog with a 7 to 9-digit alphanumeric description, in a manner that is compatible with AMI's automatic order processing system. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.



Device Number – prefix S, followed by up to six digits. Commonly there is only one letter S, followed by four numeric digits; in this case positions 5 and 6 are left blank. Any number exceeding a total of seven digits, such as S1103A-1 is written abbreviated, as S1103A1.

Package Type – a two digit alphanumeric designation in which the number designates the basic package type and the letter designates the pin count, along with other package parameters. The numbers are coded as follows:

1 – Plastic package

2 – Cer-DIP package

3 – SLAM package

4 – Ceramic (three-layer) package

5 – TO type package

(See page 1-13 for envelope drawings of all packages.)

Reserved for special usage; leave blank unless instructed otherwise on data sheet.

All orders (except those in sample quantities) are normally shipped in plastic carriers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.

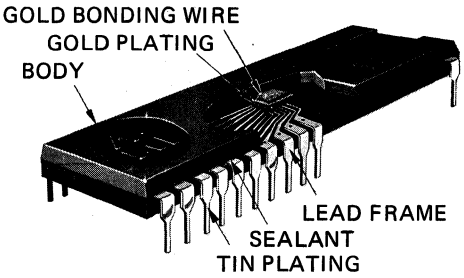
Packages

PLASTIC PACKAGE

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/LSI applications. The package consists of a silicone body, transfer-molded directly onto the assembled lead frame and die. The lead frame is Kovar or Alloy 42, with external pins tin plated. Internally, there is a 50 μin. gold spot on each die attach pad and on bonding fingertips. Gold bonding wire is attached with thermocompression gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Available in: 14, 16, 18, 22, 24, and 40 pin configurations.

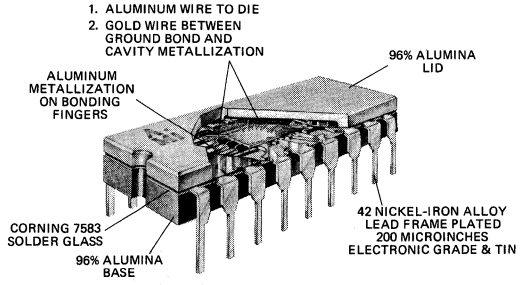


Cer-DIP PACKAGE

The Cer-DIP dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package, yet approaches plastic in cost. It is a military approved type package, with excellent reliability characteristics. Although the Cer-DIP concept has been around for a number of years, AMI leads the technology with this package, having eliminated the device instability and corrosion problems of earlier Cer-DIP processes.

The package consists of a 96% Alumina (Al_2O_3) base and the same material lid, hermetically fused onto the base with Corning 7583 solder glass (at approximately 475°C). Inert gasses are sealed inside the die cavity.

Available in: 16, 18, 22, 24, and 28 pin configurations.

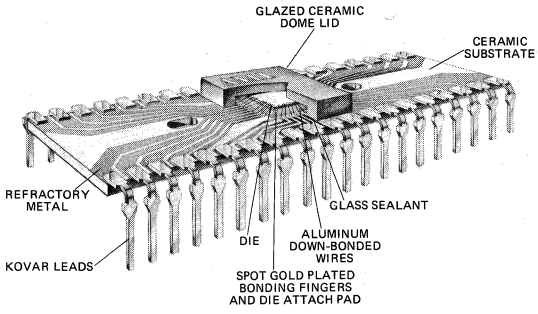


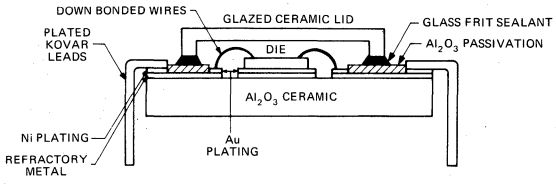
SLAM PACKAGE

The SLAM (single layer metallization) dual-in-line package is an AMI innovation that offers a lower cost alternative to three-layer ceramic packages, without sacrifice of performance or reliability.

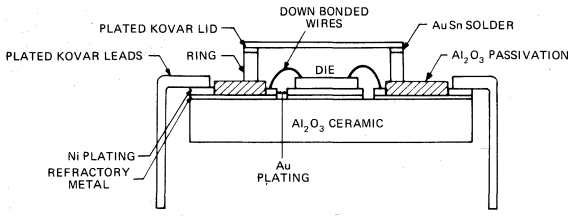
The SLAM package uses the same basic materials as ceramic, but is constructed in a simpler and thereby more reliable manner. It uses a 96% Alumina base, one basic refractory metallization layer, coated with an Alumina passivation layer, and brazed-on Kovar leads. The leads are suitable for either socket insertion or soldering. Either a glazed ceramic or a Kovar lid is used to hermetically seal the package. The glazed ceramic lid is attached with a low temperature controlled devitrified glass frit sealant, but a gold-silicon eutectic solder is used for Kovar lids.

Available in: various 14 to 40 pin configurations.



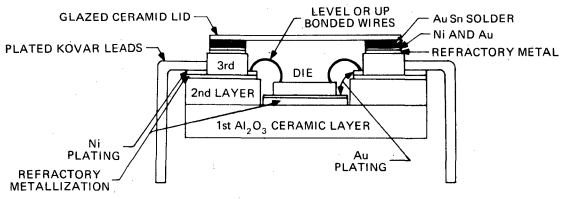


GLASS SEAL PACKAGE



METAL SEAL PACKAGE

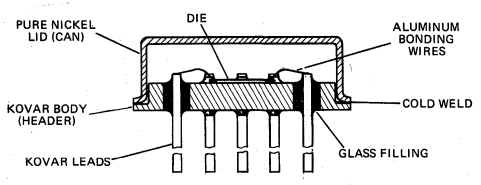
CERAMIC PACKAGE



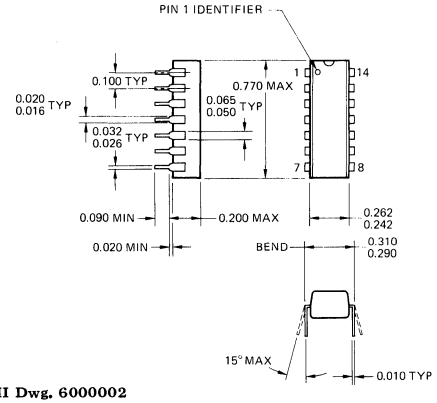
Industry standard high performance, high reliability package, made of three layers of Al_2O_3 ceramic and nickel-plated refractory metal. The cavity is sealed with a glazed ceramic lid, using a controlled devitrified low temperature glass sealant. Package leads are of Kovar, nickel-plated and solder dipped for socket insertion or soldering.

TO PACKAGE

Industry standard metal can package for small lead count dies. The package consists of a Kovar body, a pure nickel lid, and Kovar leads, brazed in with a glass seal. The lid is sealed onto the body by cold welding, which assures hermeticity of the package.

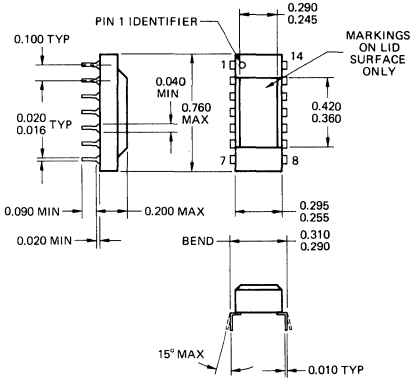


PACKAGE 1D – 14-PIN PLASTIC



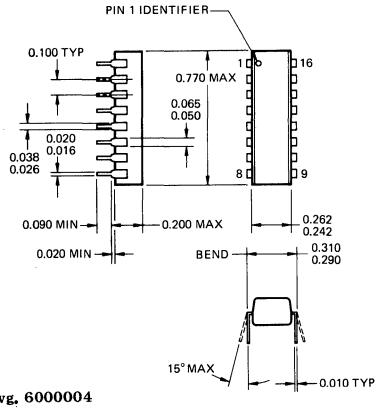
AMI Dwg. 6000002

PACKAGE 4D – 14 PIN CERAMIC



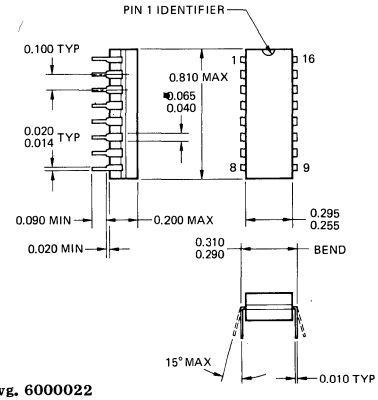
AMI Dwg. 6000001

PACKAGE 1U – 16-PIN PLASTIC



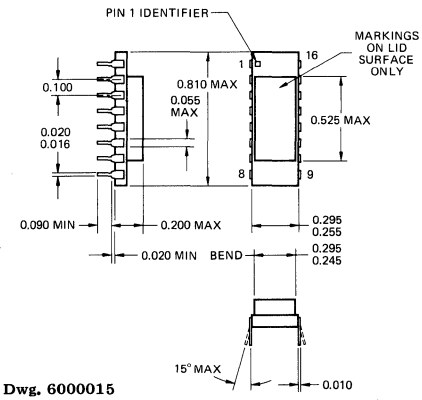
AMI Dwg. 6000004

PACKAGE 2H – 16-PIN Cer-DIP



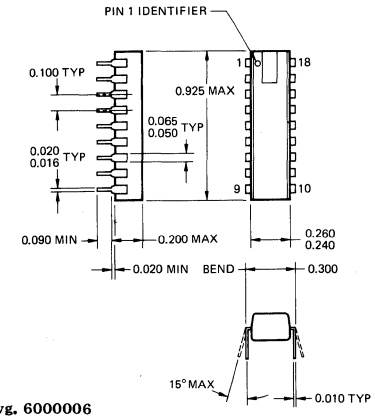
AMI Dwg. 6000022

PACKAGE 3H or 4H < 16-PIN SLAM (3H) / 16-PIN CERAMIC (4H)



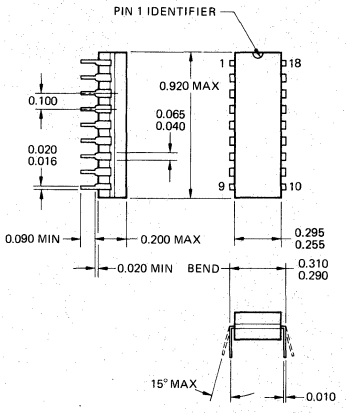
AMI Dwg. 6000015

PACKAGE 1P – 18-PIN PLASTIC



AMI Dwg. 6000006

PACKAGE 2P – 18-PIN Cer-DIP



AMI Dwg. 6000021

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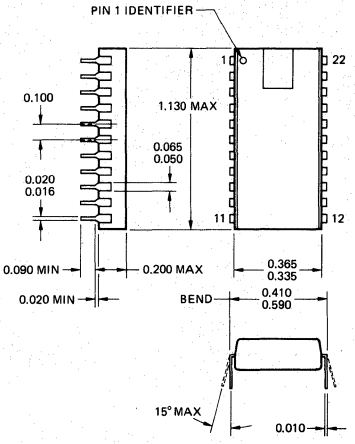
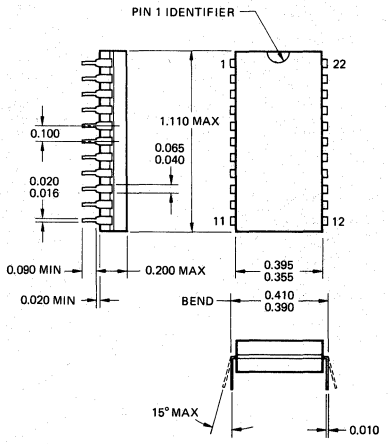


AMI Dwg. 6000025

PACKAGE 2C – 22-PIN Cer-DIP



AMI Dwg. 6000026

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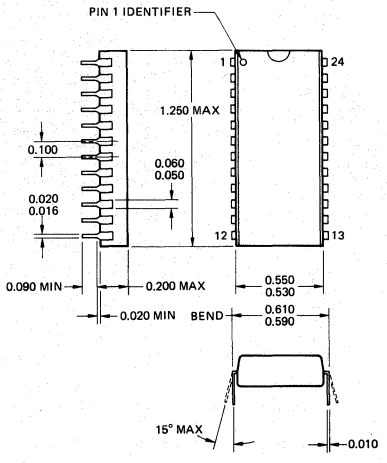
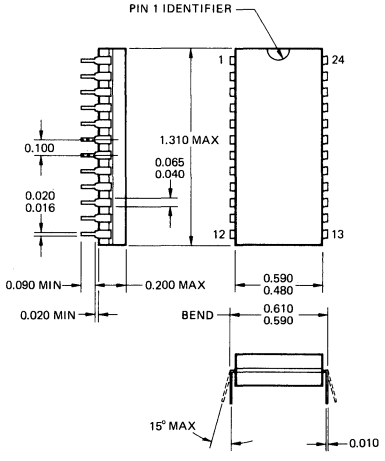


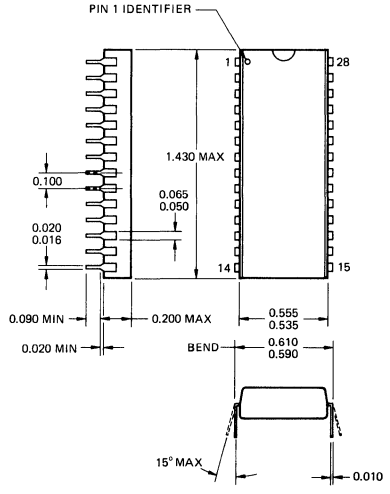
AMI Dwg. 6000008

PACKAGE 2L – 24-PIN Cer-DIP



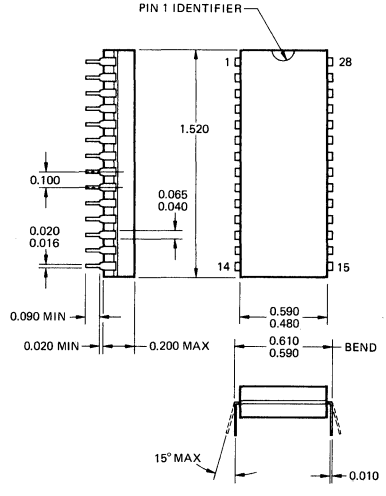
AMI Dwg. 6000027

PACKAGE 1Z – 28-PIN PLASTIC



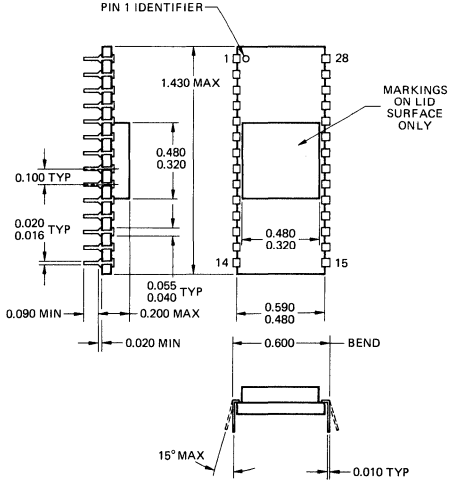
AMI Dwg. 6000017

PACKAGE 2I – 28-PIN Cer-DIP



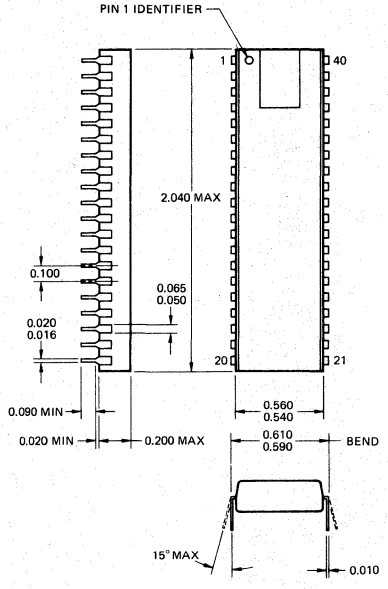
AMI Dwg. 6000028

PACKAGE 3I – 28-PIN SLAM



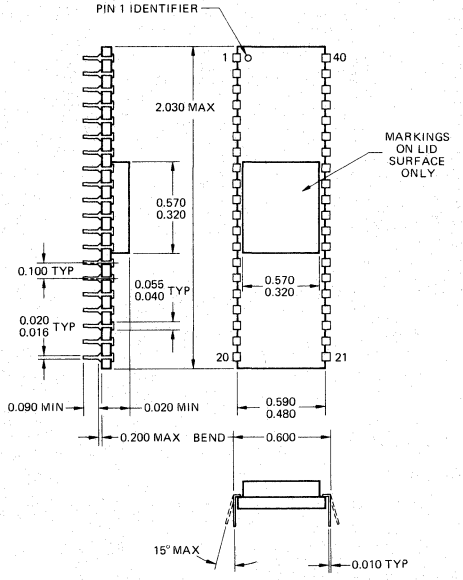
AMI Dwg. 6000009

PACKAGE 1T – 40-PIN PLASTIC



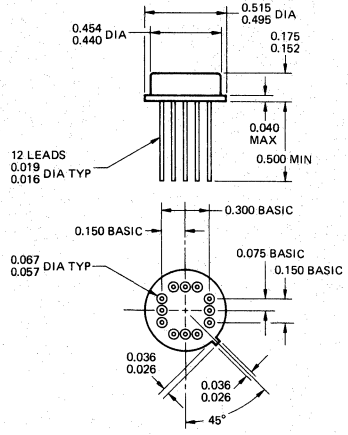
AMI Dwg. 6000012

PACKAGE 3M – 40-PIN SLAM



AMI Dwg. 6000011

PACKAGE 5F – (SIMILAR TO TO-8)



AMERICAN MICROSYSTEMS, INC.

TERMS OF SALE

1. **ACCEPTANCE:** THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices quoted for the items described above and acknowledged hereby are firm and not subject to audit, price revision, or price redetermination.

2. **PAYMENTS:**
(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer. The Seller reserves the right to ship to its order and make collection by sight draft with bill of lading attached.

3. **TAXES:** Unless otherwise specifically provided herein, the amount of any present or future sales, revenue, excise or other tax applicable to the products covered by this order or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer or, in lieu thereof, the Buyer shall provide the Seller with an appropriate tax exemption certificate.

4. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, Railway Express, Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. **DELIVERY:** Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, or damages of any kind arising out of delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fire, strikes, lockout, slow-downs, factory or labor conditions, errors in manufacture, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraphs, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product or part is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. **INSPECTION:** Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent.

8. **WARRANTY:** The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

9. **GENERAL:**
(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.
(b) The Seller represents that with respect to the production of articles and/or the performance of the services covered by this order, it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended.
(c) In no event shall either party be liable for consequential or special damages.
(d) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.
(e) Except to the extent provided in Paragraph 10, below, this order is not subject to cancellation or termination for convenience.

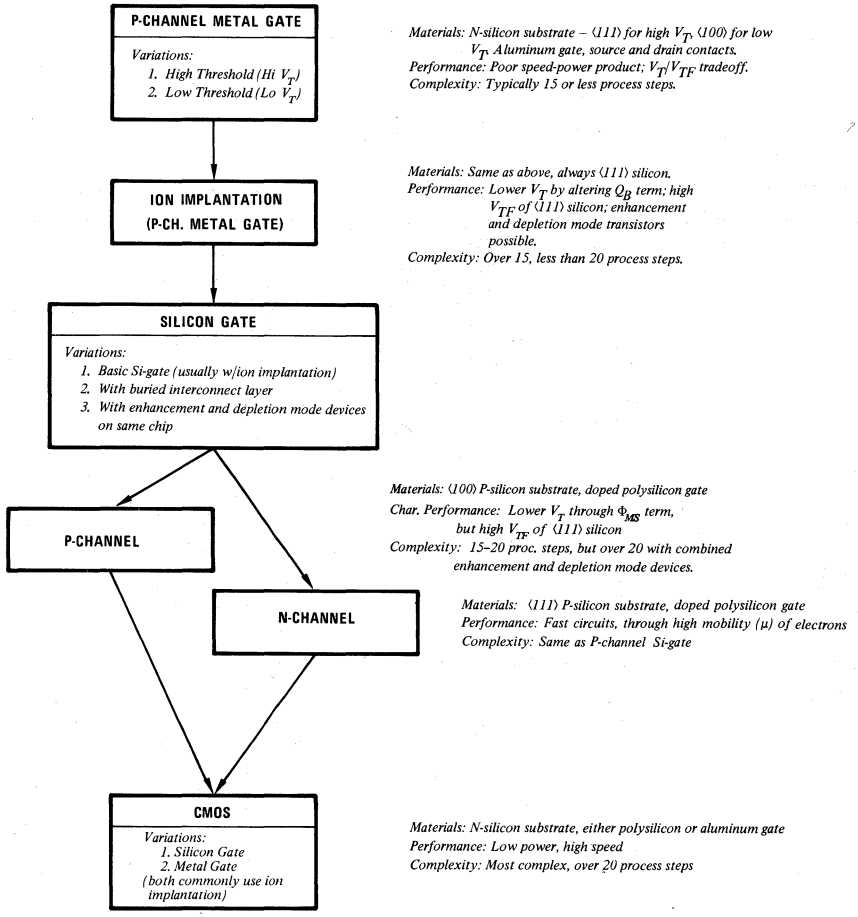
10. **GOVERNMENT CONTRACT PROVISIONS:** If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Armed Services Procurement Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be—i.e., "Contracting Officer" shall mean "Buyer"; "Contractor" shall mean "Seller"; and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.7, Payments; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Soviet Controlled Areas; 7-103.16, Contract Work Hours Standards Act—Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 8.706, Termination for Convenience of the Government (only to extent that Buyer's contract is terminated for the convenience of the Government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.14, Utilization of Small Business Concerns; 7-104.15, Examination of Records; 7-104.20, Utilization of Concerns in Labor Surplus Areas.

2

MOS Processes

Figure 2-1. The Family of Major MOS Processes.



Note: The Processes are grouped in the order of increasing complexity, which also corresponds, with the exception of CMOS, to their chronological evolution (see Figure 2-2).

MOS Processes

INTRODUCTION

From the first attempts, less than a dozen years ago, to manufacture MOS devices commercially, the MOS integrated circuit industry has grown to be one of the largest in electronics. Every major integrated circuit manufacturer today has some type of MOS product line, MOS/LSI has made possible the use of integrated circuits in entirely new areas of our environment*, and MOS is also likely to grow faster than any other electronics industry – both, by the expanding demand for existing products and through innovative expansion into new applications.

Manufacturing technologies in the MOS industry have evolved from a single early MOS process into several basic processes and many variations thereof, variously developed and used by different manufacturers. It is the purpose of this section to describe all the basic MOS processes and provide a comparative overview. This comparative description is preceded by a summary of the fundamental MOS theory, including a specific discussion of the parameters by which the comparisons are made.

EVOLUTION OF MOS

The earliest commercial MOS processes were developed by trial and error to the point where a manufacturer could produce a device that worked satisfactorily and would give a reasonable yield. It made sense for the manufacturer to stay with his process faithfully, for fear of disturbing a working combination of process steps and thus interrupting his entire production. This was the only practical and profitable manner of producing devices during the early years of MOS.

Out of this empirical heritage more understanding of the technology developed – both as a result of the accumulation of production experience, as well as from research into the processing steps and properties of materials. As a result, the MOS industry increased its facility to predictably vary processing steps, introduce entirely new processing techniques, and use new materials. An example of the alteration of process steps is the variation of oxide thickness; *ion implantation* is an entirely new processing technique; and the *silicon gate electrode* exemplifies the use of a new material.

The earliest MOS process was the *P-channel Metal Gate* (see Figure 2-2). Although there were prior unsuccessful attempts by various manufacturers to develop a process and become established in the MOS business, not until 1967, when American Microsystems Inc. began to manufacture and market its products, was it proven that MOS integrated circuits are an economically and technologically viable product. Thus, the P-channel Metal Gate process in a way became the basis for an entire MOS industry and stimulated the development of a multitude of other processes.

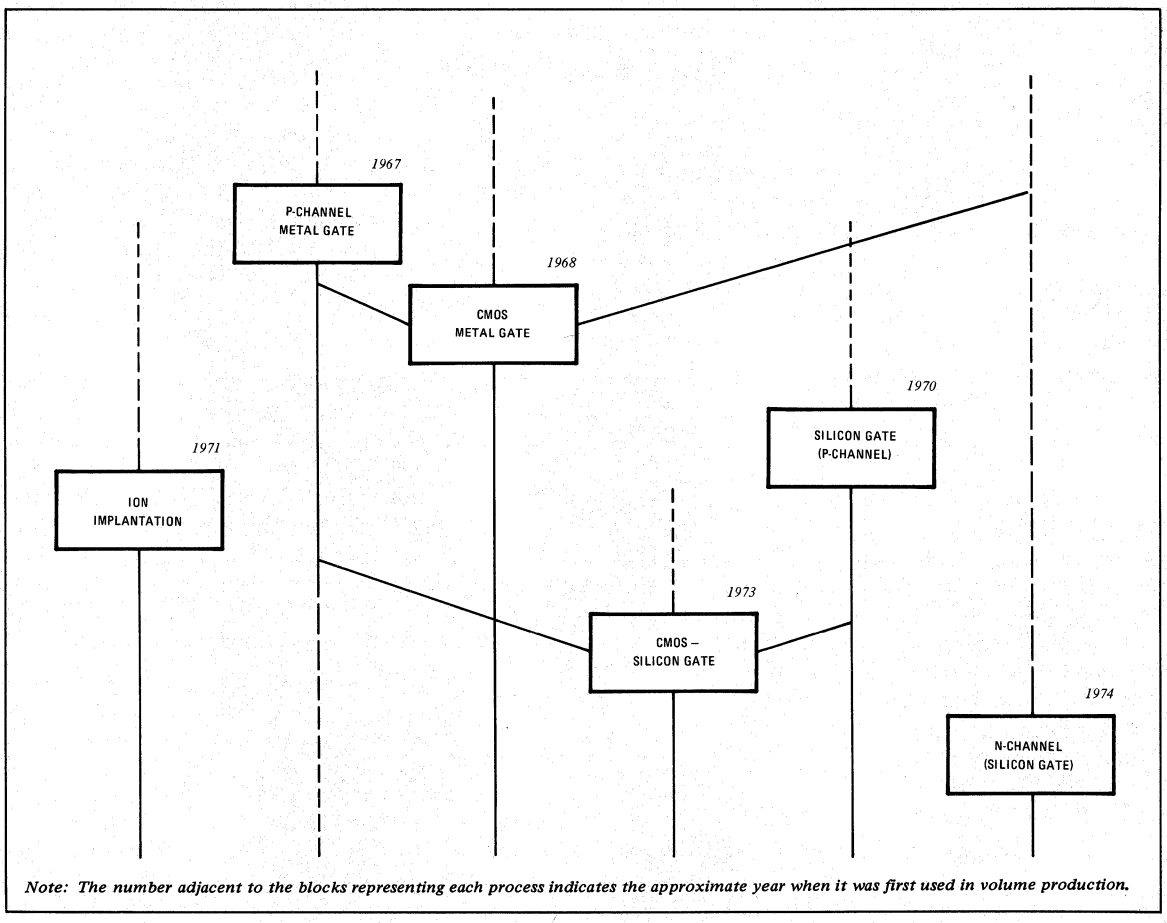
As the variations and innovations in MOS processes appeared, they naturally grouped into categories and were identified by different names. Each was favored for applications in specific products or types of circuits. Today, when the MOS industry has greatly matured, there exists a family of basic processes and a number of variations. To stay technologically current and competitive, a manufacturer, instead of using a single process, must make considered use of several processes for different products. However, to gain an overall understanding of the process, it is important to keep in sight their basic evolutionary interrelationship. It is in this context that the major MOS processes are described in this section.

THE MOS TRANSISTOR

All MOS integrated circuits are based on the MOS (metal-oxide-silicon) transistor, also called a MOSFET. These transistors are based on early research done by Sah, Ihantola and Moll, Hofstein and Heiman, Heil, as well as many others. Some of the work dates as far back as 1930. The following four pages contain a brief summary of the physiochemical and electronic theory of MOS transistors, followed by a discussion of some specific MOS transistor design considerations and the differences between processes.

*Some examples: large computer memories, automobile control systems, watches, clocks, home appliances, and entertainment systems. The most far reaching and dramatic effects, however, will almost certainly result from the introduction of the MOS/LSI microprocessor.

Figure 2-2. Chronological Evolution of Major MOS Processes.



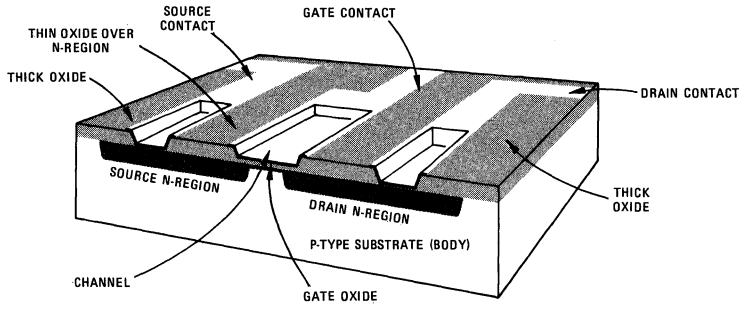
Note: The number adjacent to the blocks representing each process indicates the approximate year when it was first used in volume production.

TYPES OF TRANSISTORS

If an electrode is located near the surface of bulk semiconductor material, a voltage applied to the electrodes causes the conducting properties of the semiconductor surface to be altered. This is referred to as the *surface field effect* and is the fundamental phenomenon on which operation of the MOS transistor is based.

The bulk semiconductor material, or substrate, can be either P-type or N-type silicon. If P-type silicon is used, as shown in Figure 2-3, two N regions are diffused into the substrate. The electrode is positioned in the area between the two N regions and insulated from the substrate by a thin layer (1000 - 1500 Å) of a dielectric, such as silicon dioxide. Now, as long as the voltage on the electrode is slightly negative with respect to the substrate, it will cause the P-type silicon near the surface to become *accumulated* with positive charges, attracted by the negative electrical field of the electrode. As the electrode voltage is changed to be slightly positive with respect to the substrate, the surface will begin to be *depleted* of mobile positive charges and will cause a predominantly negative charge to appear. And if the voltage is increased still further, the surface becomes *inverted* and contains what may be thought of as a continuous layer of mobile negative charges – in the form of electrons. Thus, the surface essentially becomes N-type silicon. It is this latter state of *inversion* that is of prime interest, because it creates a conducting N channel between the two N regions, and thus allows current to flow.

Figure 2-3. Crossection of an N-Channel Transistor.

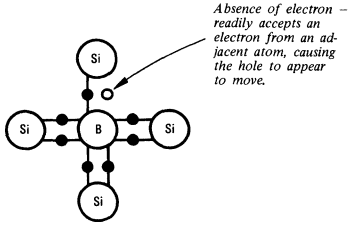


In an MOS transistor the two P regions are known as the *souree* and *drain*, whereas the electrode is referred to as the *gate*. (The lamination in the gate area gives rise to the name *metal-oxide-silicon,* or *MOS.*) The electrode voltage required to create the conducting channel is referred to as the *threshold voltage* V_T and is an important parameter in circuit design, because it represents that gate voltage required to turn the transistor on. Threshold voltage is discussed in more detail later.

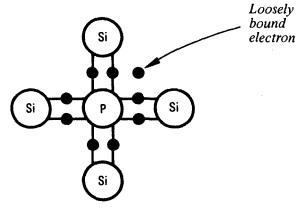
The above structure is that of an *N-channel* MOS transistor operating in the *enhancement mode.* That is, as the gate voltage is raised, it enhances the flow of current in the N channel between the source and drain. It is equally possible, however, to make a *P-channel enhancement mode* transistor, by diffusing two P regions in an N-type substrate and then increasing the gate voltage in a negative direction, to accumulate positive charge at the surface and thus create a P channel between the source and drain. Figure 2-4 shows a P-channel transistor.

P-type and N-type Silicon

P-type silicon is made by doping pure silicon, during its crystal growth stages, with impurity (dopant) atoms, commonly boron. The boron impurity causes the silicon to become a semiconductor, which conducts by virtue of mobile positive charges dispersed throughout its structure. The positive charges are the absence of an electron in the outermost shell of the silicon atoms, usually referred to as "holes". In a similar manner, N-type silicon is made by doping pure silicon with impurity atoms such as phosphorus, which leaves an "extra" loosely bound electron in the outermost shell of the silicon atoms. Thus, in N-type silicon conduction takes place by means of mobile negative charges.



(a) Boron doped (P-type) Silicon



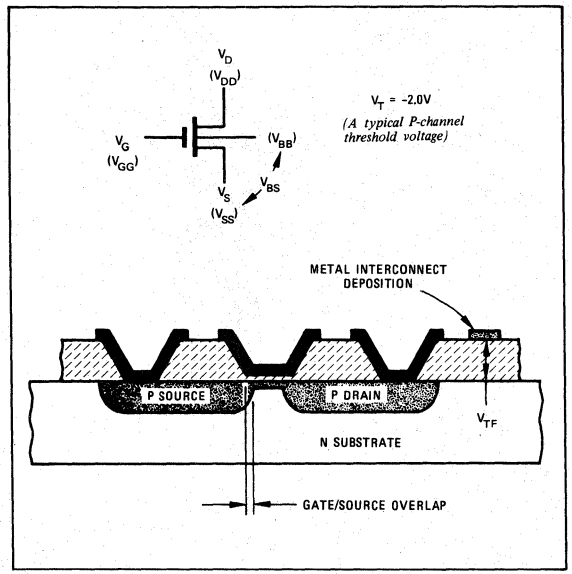
(b) Phosphorus doped (N-type) Silicon

In contrast to the enhancement mode transistor, there can also be a *depletion mode* transistor – which simply refers to the fact that the transistor is in a conducting state without any bias voltage on the gate; a bias must be applied to decrease the current flow.

There are two ways in which a depletion mode transistor can be made. First, it is actually more characteristic for an N-channel transistor device to operate in depletion mode, rather than in enhancement. A part of the reason is because the silicon dioxide insulating layer between the gate electrode and the substrate always has an internal positive charge, which acts toward the formation of an N channel, in much the same way as an applied positive gate bias does. Therefore, an N-channel transistor may intrinsically be a depletion mode device and special processing techniques are required to cause it to operate in enhancement mode.

Another way to make depletion mode transistor is by ion implantation. In the case of a P-channel transistor, the N-type substrate is bombarded with P-type (acceptor) impurity ions, to actually convert the surface of the substrate to P-type. Thus, a P channel is formed and will conduct current between the source and drain without any gate bias. Ion implantation is a special technique, described and illustrated in more detail later.

Figure 2-4. Crossection and Schematic Symbol of a P-channel Transistor.



VOLTAGE-CURRENT CHARACTERISTICS

The voltage-current relationships in an MOS transistor can be considered by using the P-channel transistor shown in Figure 2-4. If the gate voltage V_G becomes more negative than the threshold voltage V_T (-2.0 volts with respect to the substrate surface under the gate electrode), a channel is formed and hole current can flow between the source and the drain. The magnitude of the channel current depends on the drain voltage V_D. With the source at 0V, current will flow any time V_D is negative. There is a voltage drop along the channel (the channel acts as a resistive element) and because of this gradient, V_T is defined with respect to one point in the channel. This point is where the channel joins the source region, where the channel and source voltage is the same. Thus, V_T is actually defined with respect to the source and the common expression for it is:

$$V_T = V_G - V_S$$

when the channel starts to form.

As V_D is increased in the negative direction, current increases in a linear manner, until the transistor is saturated, at which time further increase in V_D does not materially increase the current. The point of saturation depends on the voltage applied to the gate, as shown by the series of drain current curves in Figure 2-5. The gate voltage can be used to raise the upper limit (saturation level) of current flow, and the maximum current is limited either by the dielectric breakdown between the gate electrode and the substrate, or by other factors described below. The gate voltage V_G is related to the drain voltage at saturation, $V_{D\,Sat}$, by the following equation:

$$V_{D\,Sat} = V_G - V_T$$

The saturation point often is also referred to as *pinch-off,* due to the fact that an inversion layer no longer exists adjacent to the drain (channel current, however, continues to flow).

When an MOS transistor is in a circuit, the drain may be connected to a drain supply voltage, designated V_{DD}, or the drain connection may serve as the output of the circuit. Both conditions are shown in the inverter circuit, Figure 2-6. The gate commonly serves as the input connection, or it may also be connected to a supply voltage, designated V_{GG}. The source serves as the reference against which V_T and all other voltages are measured. It is common to have the source tied to

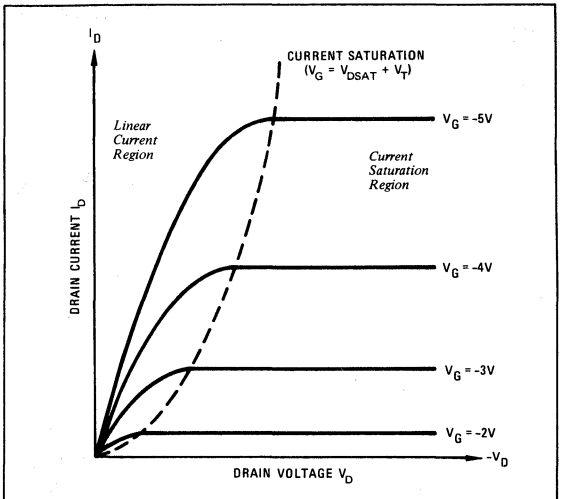
ground, but it may also be at a voltage other than ground. If the source is tied to a supply voltage, that voltage is designated V_{SS}.

The substrate, or body, is also commonly tied to ground, although back biasing the substrate is a specific technique for changing the effective V_T value. The influence of substrate back bias on V_T is referred to as the *body effect* and is, for example, used with N-channel devices to raise the V_T to an operationally more desirable value than the intrinsic V_T.

Considering the effects of both the source and substrate bias on the gate threshold voltage, and using the P-channel transistor in Figure 2-4 as an example, their relationships are as follows. The V_T is always -2V with respect to the source. That means that if V_{SS} is, for example, changed from 0 to +5V, V_G required to turn the transistor on will change from -2V to +3V – provided that the substrate voltage is also changed to +5V, so that there is no substrate-to-source bias. If the source now is returned to 0V, while the substrate remains at +5V, there is 5 volts back bias and this causes the body effect to shift V_T by an amount approximated by the formula:

$$\Delta V_T = -\gamma\sqrt{V_{BS}}$$

Figure 2-5. Drain Characteristic Curves of an MOS Transistor.

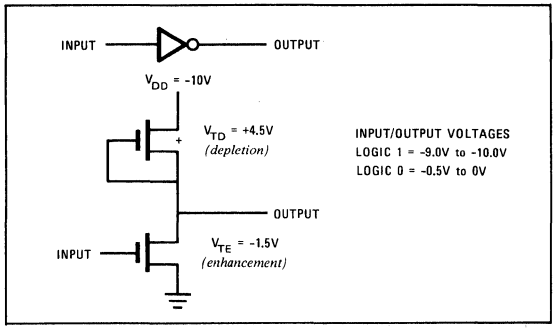


Channel Current Equation (nonsaturated):

$$I_C = \mu C_{OX} (W/\ell) \left[(V_G - V_T) V_D - \tfrac{1}{2}V_D^2\right]$$

μ	Mobility	V_G	Gate voltage
C_{OX}	Capacitance of gate oxide	V_T	Threshold voltage
W/ℓ	Width-to-length of channel	V_D	Drain voltage

Figure 2-6. Typical Inverter Using Both Depletion and Enhancement Mode Transistors.



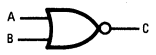
Where V_{BS} is the substrate-to-source back bias the γ is the *body effect* term (a constant that typically varies from 0.5 to 0.75, depending on the process and the doping concentrations). Thus, the effective V_T in this example is $-2 - (0.5\sqrt{5}) \approx -3.1$ volts (using $\gamma = 0.5$).

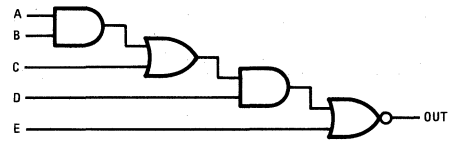
Note that there can never be any forward substrate-to-source bias (of 0.6 volts or more), because it would cause current flow between the substrate and the source, the same as in a forward biased diode. By the same token, if back bias is increased beyond the diode breakdown voltage, conduction will occur also. This is characteristically what happens when the drain voltage V_D is increased much beyond its value at channel current saturation. In this case the drain-to-substrate junction breaks down and avalanching of drain current takes place.

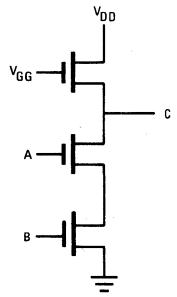
In summary, the operating range of an MOS transistor, is defined by the drain, source, substrate, or gate voltages. The drain, source, and substrate voltages can be between a forward bias condition of less than 0.6V and a back bias up to the diode breakdown voltage of the drain-substrate junction. Any time that the voltages are outside this range there is conduction between either the source or drain and the substrate, and the transistor is not performing its proper function. The gate voltage is limited by gate-to-substrate breakdown.

In addition, depending on the proximity of the drain and source regions (i.e., the length of the channel), another type of breakdown, known as *punch-through* can also occur and become the limiting factor. In punch-through the substrate in the area between the drain and source becomes depleted and current flow through it increases, until it is limited by the external circuit.

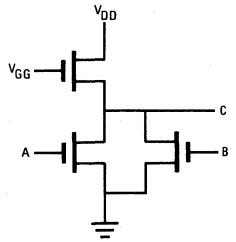
Implementing Logic With MOS Transistors



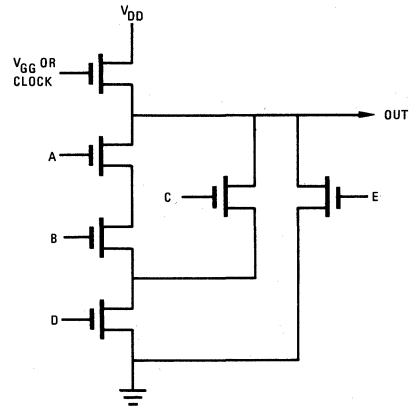




NAND Gate



NOR Gate



Multiple Logic Element

MOS DESIGN CONSIDERATIONS

In the design and manufacture of an MOS integrated circuit, there always are several main objectives of performance, cost, manufacturing feasibility, etc. Such objectives must be arranged in a priority and optimized. This approach is equally true for an MOS manufacturer who is planning a standard product, as for an end user considering the design of a custom circuit. Some of the essential objectives that must be considered are as follows:

- Speed – the slowest internal propagation delay possible in the circuit and the output signal rise and fall times.
- Power – the amount of power consumed during operation. It is related to junction temperature, power dissipation, and chip size.
- Type of Logic – is the circuit static or dynamic, does it consist of all random logic or of repetitive segments of logic, like in a shift register? These considerations determine the basic approaches to design and topological layout of the chip.
- Application – refers to factors that depend on the basic nature and environment of the equipment in which the circuit is to be used. Includes design considerations related to temperature, humidity, electrical noise, range of power consumption, and others.
- Power Supplies – the number of different voltages available to the circuit; their polarities and ranges.
- Clock Signals – the amplitude and frequency of necessary clock signals, as well as requirements to gate or otherwise process the signals. (The amplitudes and duration of clocking voltage levels are critical to the design of conduction ratios and coupler transistors.)
- Interface Requirements – the requirements to respond to certain voltage or current conditions at input or output.
- Packaging – the type of packages in which it is possible to mount the finished chip (depending on factors such as heat dissipation, size, etc.). Packages can be plastic, ceramic, Cer-DIP, or other types.
- Final Cost – the cost of the finished packaged and fully tested device. (Cost depends on the process, manufacturing yields, testing and packaging costs, etc.)

The MOS design engineer can begin to achieve some of these objectives during system design, partitioning, and circuit design stages, but in integrated circuits the fundamental decisions occur at the atomic structure level of materials and the microscopic dimensional level of individual circuit elements. Here the design engineer can fix performance characteristics of individual devices (transistors, resistors, etc.) and thereby structure the performance of the whole circuit. The specific device performance characteristics that the designer is concerned with are exemplified by those described on this and the following page, but to implement them he makes certain process and device dimension oriented decisions, listed below:

- Materials – the kind of substrate to be used, its doping concentrations, choice of silicon or aluminum for the gate electrode, etc.
- Process Techniques – the type of diffusion to be used; its duration; use of ion implantation for altering the threshold voltages; or the use of any other special steps or procedures.

  (Note: a particular combination of Materials and Process Techniques defines the MOS process.)
- Device Configuration – the size and dimensional proportions of the channel, drain, and source regions of each transistor; spacing between circuit elements and between interconnections; thickness of oxide and metal deposits *(most of these dimensions are incorporated into the final masks used in manufacturing).*

Therefore, to fully appreciate the difference between MOS processes, one must understand both the basic device characteristics and how a designer optimizes them with the choice of a particular material, process steps, and device dimensions.

THRESHOLD VOLTAGE V_T

One of the most basic device performance characteristics is the threshold voltage V_T. The concept of V_T and its role as a current determinant in an MOS transistor was described above, but it is important to consider the many different ways in which the V_T level can be altered in a transistor.

The level of V_T in an MOS transistor is very important because, in addition to affecting the amount of current, it affects the interface signal voltages, the level and polarity of power supply voltages needed in the circuit (thereby the power consumption), and indirectly also the speed of the transistor. Generally, in enhancement mode devices V_T must be sufficiently above or below 0V to provide a definite *on* and *off* biasing range, but not so much that it makes interfacing input signals difficult or causes high power consumption. A lower threshold is particularly important when a clock signal is used to turn the transistor *on* and *off.*

One fundamental determinant of V_T is the doping level of the substrate: the higher the dopant concentration in the substrate the higher the threshold voltage. Doping level of the substrate is always determined at the time when the crystal is grown, but can be altered by ion implantation. Ion implantation consists of bombarding the surface of the substrate with dopant ions to change the substrate characteristics in the surface layer, where it interacts with the electric field of the gate electrode.

Another determinant of V_T is the gate insulator –both its thickness and the material itself (commonly silicon dioxide). A decrease in thickness lowers V_T, but at the same time increases the risk of capacitive shorting between the gate electrode and the substrate or diffused regions. Different dielectric materials have been tried by various manufacturers to overcome the shorting.

An intrinsic determinant of V_T is the choice of gate electrode and substrate materials. This relates to the physics concept of *work function,* which represents the binding energy of an electron in a particular material. When polycrystalline doped silicon is used as a gate electrode instead of aluminum, the work function changes in such a way as to cause a lower V_T. This is the basic difference between *aluminum gate* and *silicon gate* processes.

In relation to substrate material, there are two basic crystalline structures that can be used in MOS transistors. One is known as ⟨111⟩ silicon and causes a relatively higher V_T, the other is ⟨100⟩ silicon and causes a lower V_T. There are, however, some tradeoffs between the two, relating to a parasitic field oxide threshold voltage V_{TF}, discussed later under the P-channel Metal Gate process.

W/ℓ RATIO

One of the very important dimension-related design parameters is the width-to-length ratio of the transistor channel. The W/ℓ ratio determines the total resistance of the channel, is one determinant of speed, and relates to the overall size of the transistor. Thus, it affects the final chip size, which, in turn, relates to the yield and thereby to final costs.

It is a typical procedure for a designer to start out with the basic speed requirements of a circuit, then calculate the inherent capacitance of all transistors that are used as loads in the circuit, and finally choose the W/ℓ of all driving transistors to provide the needed drive current, corresponding to the speed requirements. Figure 2-7 shows how the speed of a typical pair of inverters relates to the W/ℓ ratio of their transistors.

Another use of the W/ℓ ratio is in calculating the voltage drop across a transistor. In an inverter, as in Figure 2-6, where two transistors are connected in series, the relative voltage drop across each transistor is determined by choosing the two W/ℓ ratios, so that their resistances are in the corresponding proportion.

CAPACITANCE

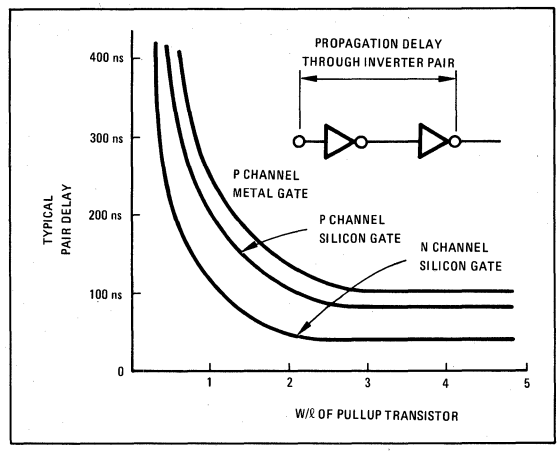
Another major concern in MOS transistor design is capacitance. Capacitance usually is considered in several parts. First, the gate electrode and the surface of the silicon substrate form a parallel plate capacitor, with the silicon oxide serving as the dielectric. Second, both the source and drain region junctions with the substrate constitute a capacitor, with the depletion region acting as the dielectric. Third, there is capacitance between the gate electrode and both the source and the drain.

This latter capacitance is particularly important in all transistors in which the gate electrode overlaps the source and drain regions and it does so in all except those manufactured by the *self-aligning gate* processes, see Figure 2-4. This overlap is necessary in manufacture, to allow for mask tolerances: the gate electrode metal deposit must always reach all the way from the source to the drain and the only way to assure this is to allow a positive (overlap) mask tolerance.

Capacitance, of course, affects the speed of a transistor and also its power consumption. The more capacitance loading a transistor presents to an input signal, the more time is required to turn the transistor on. Power consumption considerations become particularly important at high operating frequencies.

In addition to having undesireable effects on circuit performance, the intrinsic capacitances can also be used beneficially in MOS circuit design. In dynamic MOS circuits capacitance is very often used for temporary storage of charge representing a logic level. In a typical MOS shift register stage, Figure 2-8, the equivalent capacitances C1 and C2 are used to store data between clock pulses. Capacitance C1, for example, represents the sum of the drain-to-substrate capacitance of Q3, gate capacitance of Q4, and also the capacitance of the interconnect line between Q3 and Q4.

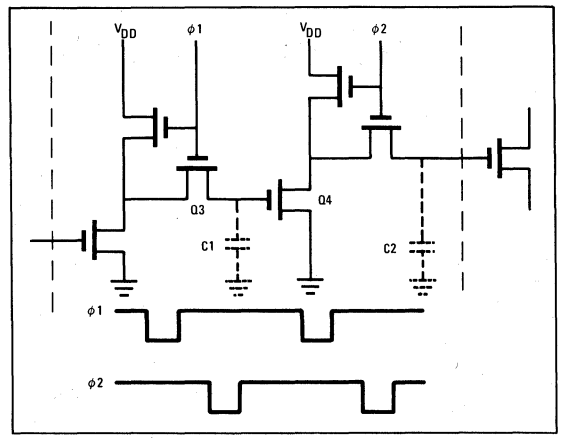
Figure 2-7. Typical Inverter Pair Delay vs. W/ℓ for Various MOS Processes.



MOBILITY

The term *mobility* (designated μ) refers to the intrinsic current carrying properties of N and P doped silicon. In N-doped silicon the majority current carriers are free electrons (see inset on page 2-5), whereas in P-doped silicon current is carried by means of holes. The mobility of electrons is approximately 2.5 times that of holes and therefore N-channel transistors are faster than P-channel. For the same channel size (or W/ℓ ratio) N-channel transistor can also carry more current.

Figure 2-8. Typical P-channel Shift Register Stage.



PROCESS DESCRIPTIONS

In the following pages each of the major processes is described individually. In the descriptions the basic process is described first, followed by an explanation of its advantages, applications, etc. In each case only the basic process is explained, without details of variations used by different manufacturers. Also, the less common processes, such as MNOS (Metal-Nitride Oxide-Silicon), or future processes, such as SOS (Silicon-on-Sapphire) are not described separately.

At the end of the descriptions comparative data on speed, power consumption, and cost is included.

P-CHANNEL METAL GATE PROCESS

Of all the basic MOS processes, P-channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds use today in some devices. Several versions of this process have evolved since its earliest days. A crossection of a P-channel metal gate MOS transistor is shown in Figure 2-4. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the supporting substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and the drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000 - 1500 Å) of silicon dioxide. The P-channel transistor is turned on by a negative gate voltage and conducts current between the source and the drain by means of holes as the majority carriers.

The basic P-channel metal gate process can be subdivided in two general categories: *high-threshold* and *low-threshold.* Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage V_T required to turn a transistor on. The high threshold V_T is typically -3 to -5 Volts and the low threshold V_T is typically -1.5 to -2.5 volts.

The most common manner in which the difference in threshold voltages is achieved is by the use of substrates with different crystalline structures. The high V_T process uses ⟨111⟩ silicon, whereas the low V_T process uses ⟨100⟩ silicon. The difference in the silicon structure causes the inherent potential (work function) across the interface between the substrate and the silicon dioxide gate dielectric to change in such a manner than it lowers the threshold voltage V_T.

One of the main advantages of lowering V_T is the ability to interface the device with TTL circuitry. However, the use of ⟨100⟩ silicon carries with it a distinct disadvantage also. Just as the surface layer of the ⟨100⟩ silicon can be inverted by a lower V_T, so it also can be inverted at other random locations – through the thick oxide layers – by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage V_{TF}, and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the low V_T process. A drop in V_{TF} between a high V_T and low V_T process may, for example, be from -28V to -17V.

The low V_T process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high V_T process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-channel metal gate processes yield devices slower in speed than those made by other MOS processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high V_T process, because it operates at a high threshold voltage, has excellent noise immunity.

ION IMPLANTATION (P-ch. MET. GATE) PROCESS

The P-channel Ion Implant process uses essentially the same geometrical structure and the same materials as the high V_T P-channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage V_T of the transistor, without influencing any other properties of the transistor.

Figure 2-9 shows the ion implantation step in a diagrammatic manner. It is performed in manufacture, after the gate oxide is deposited, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon

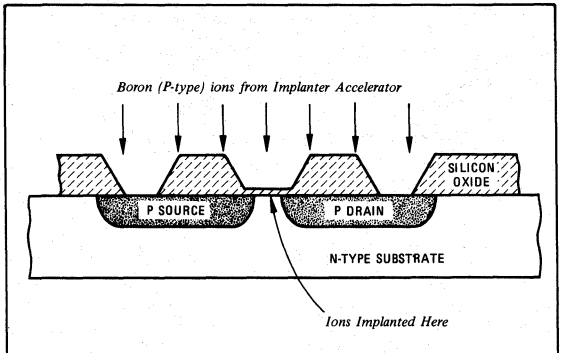
substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore, could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the V_T required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage V_{TF} (a problem with the low V_T P-channel Metal Gate process, described above). The ⟨111⟩ silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still remains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-implanted P-channel Metal Gate process is very much in use today. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Figure 2-9. Diagram of Ion Implantation Step.



Note: Implantation step is performed after gate oxidation.

Because of its low V_T, it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

P-CHANNEL SILICON GATE PROCESS

The Silicon Gate process is significantly different from the metal gate processes, in that it uses a polysilicon gate electrode material, rather than aluminum. Although the process is more complex than metal gate, several advantages arise from the basic change in materials, with the potential to add others.

Figure 2-10 shows the crossection of a typical silicon gate P-channel transistor. The materials are the same as for metal gate, except the gate electrode is doped polycrystalline silicon (in this instance P-doped), which is deposited over the silicon oxide gate dielectric in an epitaxial reactor.

The first advantage of a polysilicon gate electrode is that it reduces the threshold voltage V_T, (by acting through the *work function,* described previously). Thus, the silicon gate gives the same advantage as either ion implantation or the change of substrate in the low V_T process. A typical V_T of a silicon gate P-channel transistor is -1 to -2 volts.

Another aspect of the silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure 2-10.

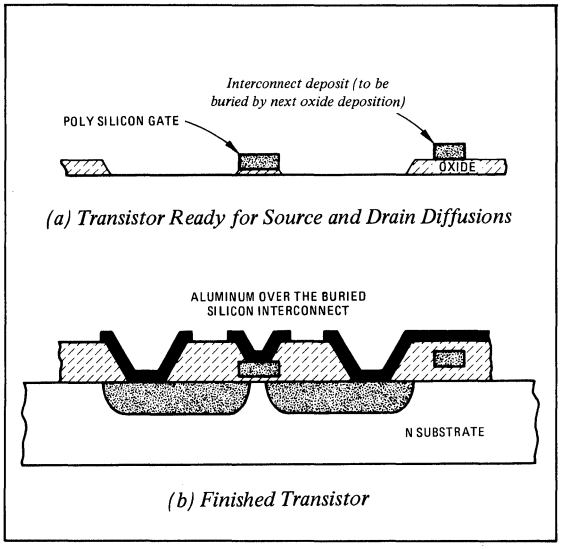
One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure 2-10] the interconnect lines cannot be located over these diffusion regions.

A third advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and thus improves speed, as well

as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure 2-10. Therefore, no planned overlap for manufacturing tolerance purposes need exist (as described under Capacitance, on page 2-10) and the gate is said to be *self-aligned.* The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

Figure 2-10. Crossection of a Silicon Gate MOS Transistor.



N-CHANNEL PROCESS

The N-channel process is the latest of the major MOS processes. It is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N channel is by means of electrons, rather than holes.

The main advantage of the N-channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-channel transistors are faster than P-channel. In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-channel transistors can be made smaller. The positive gate voltage allows an N-channel transistor to be completely compatible with TTL.

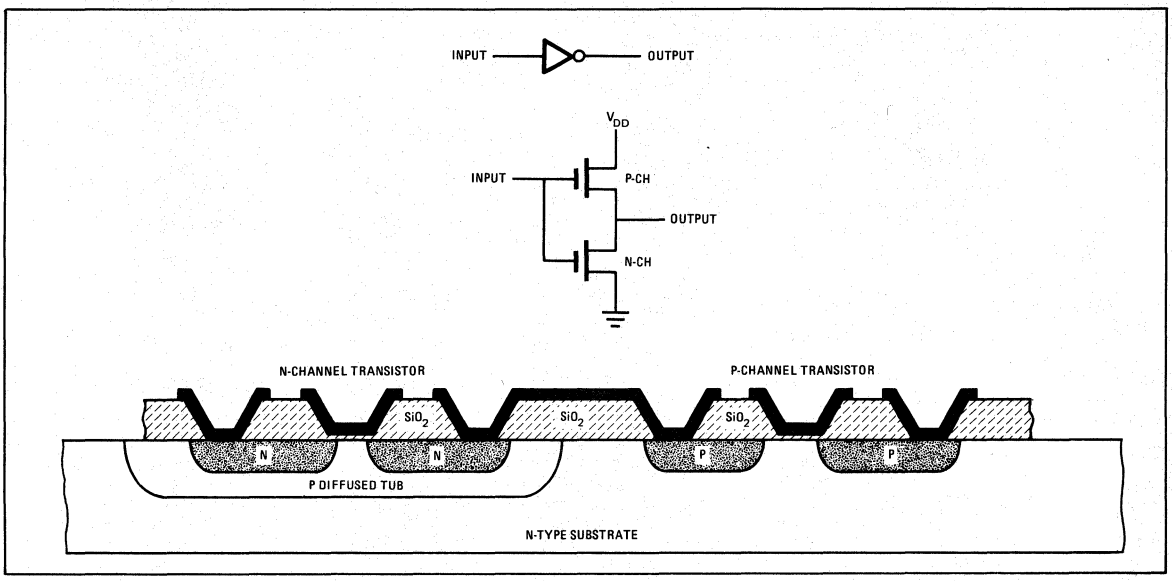
Figure 2-3 shows the crossection of an N-channel transistor. Because the N-channel process made its transition from the research laboratory into production after the evolution of silicon gate and ion implantation, most all N-channel devices use both, silicon gates and ion implantation.

Because N-channel is relatively new, however, many of its detailed production techniques still are undergoing development and evolutionary changes can be expected. In the future, the combination of high speed, TTL compatability, low power requirements, and compactness is likely to make N-channel the most widely used process. As manufacturing experience is gained, the potential cost of N-channel is low also.

Historically, N-channel process and its advantages were known well at the time when the first P-channel devices were successfully manufactured, however it was much more difficult to produce N-channel. One of the main reasons (described previously on page 2-6) was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a V_T of only a few tenths of a volt (positive). Thus, the transistor operated as a marginal depletion mode device, without a well defined *on/off* biasing range. Attempts to raise V_T by varying gate oxide thickness and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-channel became practical for high density circuits.

Presently, the N-channel process is used in large memory chips, microprocessors, and other devices in which the circuit compactness and higher speed are of importance. Most N-channel devices operate on a single +5V power supply and their threshold voltages range between +0.8 and +1.7. Higher voltages can be used to increase operating speed and a second supply voltage is required on devices that use substrate back bias.

Figure 2-11. Crossection and Schematic Diagram of a CMOS Inverter



CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors – one an N-channel, the other a P-channel, as shown in Figure 2-11. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure 2-11 is fabricated on an N-type silicon substrate in which a P "tub" is diffused to form the body for the N-channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is its extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-channel transistor is biased on, the P-channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-channel transistor on and the output is near the drain voltage $+V_{DD}$. In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Compared to other MOS processes, CMOS also is considerably faster. On the other hand, the use of two transistors in one device makes any circuit more complex and costly. It requires more chip size and, therefore, CMOS is not suitable for such devices as large (high number of bits) memories, microprocessors, or other complex circuits. Instead, watch circuits and other low power applications can benefit most from CMOS, and, in fact, would be impossible without CMOS. As a consequence, for MOS/LSI circuits CMOS is somewhat of a special purpose process, used in applications where the higher power consumption processes are not suitable.

The prime reason for the popularity of CMOS, however, is its use in manufacturing logic elements and building block circuits – logic gates, inverters, small shift registers, counters, etc. These CMOS devices constitute a logic family in the same way as TTL, ECL, and other bipolar circuits do. In the areas of very low power consumption, high noise immunity (when operated at any but the lowest power supply voltages), and simplicity of operation, CMOS compares favorably with any of the bipolar families and has become widely accepted by logic designers. In speed, however, CMOS (or any other MOS process) cannot compete with the fastest of bipolar.

CMOS circuits can be operated on a single power supply voltage, which can be varied from +3 to about +18 volts, with a higher voltage giving more speed and higher noise immunity.

Figure 2-12. Comparative Data on Major MOS Processes

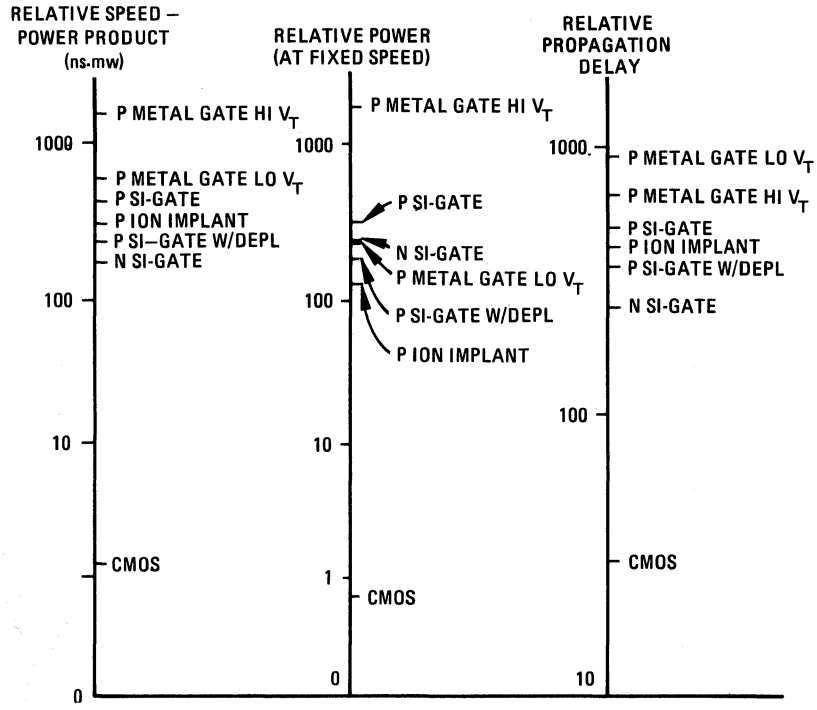
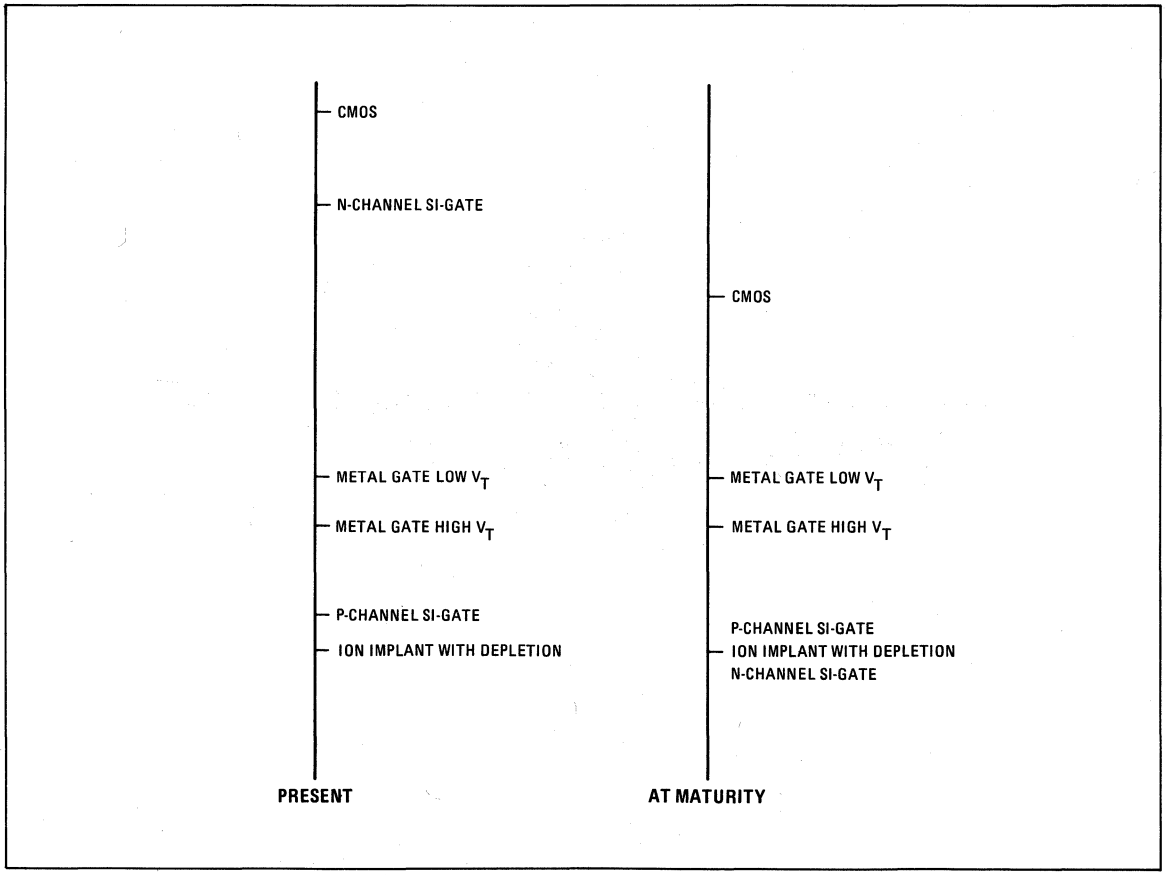


Figure 2-13. Relative Cost Per Logic Function



3

Custom Capabilities

Custom Capabilities

AMI – FIRST IN CUSTOM

AMI is the world's largest and most experienced custom MOS circuit manufacturer. Following its unique pioneering tradition in the MOS industry, AMI has continuously maintained a position of leadership – through evolution of superior circuit design engineering expertise, use of thoroughly proven reliable MOS manufacturing processes, and a solid research and development program. Today AMI has the largest design engineering staff in the world dedicated to applying the MOS technology to custom requirements, has the widest repertoire of MOS processes, and continues to expand vigorously, along with the increasing acceptance of MOS/LSI in worldwide markets.

Over 1,000 integrated circuits have been developed at AMI since the company implemented the first reliably reproducible MOS manufacturing process in 1967. Circuits for display, printing, business, scientific, and programmable calculators – circuits for household ovens and ranges, washers and dryers, audio entertainment systems, electronic organs – circuits for auto seat belt interlocks, tachometers, fuel injection, anti-skid braking, automatic transmissions – circuits for computer memories, minicomputers, data processors, microprocessors – circuits for point of sale networks, facsimile transceivers, line printers, modems, keyboard scanners, code converters, character generators, meter readers, credit card systems, multiplexers, computer terminals – circuits for timers, cash registers, coin changers, gambling machines, vending machines, DVMs, X-Y plotters, D/A converters – circuits for government communications links, satellite systems, lunar lander, and medical patient monitoring . . . all this just for starters.

The result is a track record no other company can match – both in custom and standard products. The extensive standard product line in this catalog is a tribute to the background, experience, engineering and manufacturing capability developed at AMI over years of working with custom MOS/LSI. This section explains what custom MOS is about, how you can decide if custom MOS applies to your need and the two methods of obtaining custom MOS/LSI circuits from AMI.

WHAT IS CUSTOM MOS/LSI

Custom MOS/LSI circuits are complex large scale integrated circuits designed specifically for a particular application. Any of several MOS processes can be used to manufacture such circuits, depending upon which best matches the circuit requirement. These circuits are designed from scratch – they are not modifications of existing geometries. Each component is selected and tailored for the most efficient performance of its function. Because of such attention to detail, custom MOS/LSI circuits can achieve the most function per unit of silicon area and result in the **lowest possible cost per function.** However, to obtain such optimization in all these areas requires expertise in system definition, logic and circuit design, topological layout, and manufacturing processes.

THE CUSTOM MOS/LSI DECISION

How do you know if custom MOS/LSI is right for you? Basically, there are three considerations involved when deciding whether or not a custom MOS/LSI is appropriate for a given application.

- Circuit Complexity
- Economy
- Digital Content

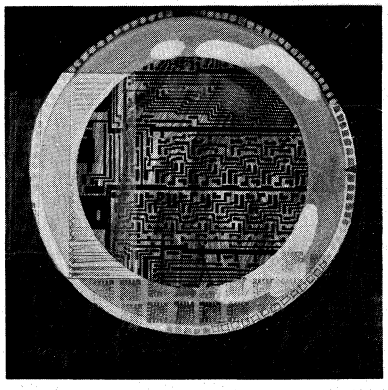
The first consideration in evaluating a custom MOS/LSI for an application is circuit complexity. An application suitable for custom circuitry is generally one requiring a complex circuit function – typically on the order of a minimum of 100 logic gates. This is because extensive engineering, design, and manufacturing effort is required for custom circuit development.

Moderately complex functions can be implemented economically with standard MSI and SSI components, but with increasing complexity problems of space, heat dissipation, power supply complexity, interconnections, and reliability usually develop. In such cases custom designed circuits can offer performance, cost, and reliability advantages.

Because of the extensive development costs necessary to achieve a good cost/performance ratio in a custom circuit, sufficient volume is required in order for a custom MOS/LSI circuit to be competitive with standard MSI and SSI circuits. An annual volume of 50,000

units is a typical rule of thumb for cost effectiveness. In cases where the user designs his own circuit and AMI manufactures it, much lower volumes become cost effective.

Of course, there always are additional important considerations affecting cost comparisons. One of the most obvious, with custom MOS/LSI, is to determine the total number of different components in a system that are eliminated by the substitution of a single custom circuit. The reduction of components has a significant effect on the number of interconnections, with an accompanying increase in reliability. This factor has a beneficial effect on product quality – it reduces troubleshooting problems at the board, subsystem, and system levels, minimizes field repairs, and usually reduces warranty problems. The reduction of components also decreases assembly and initial checkout costs. So, even though the use of 50,000 units annually is a good rule-of-thumb, as an application grows more complex, more influences become apparent, and custom MOS/LSI can become cost competitive and more reliable at much smaller volumes.



The last factor having an effect on the custom circuit decision is the amount of digital function in the circuit. There should be a preponderance of digital function for an MOS/LSI custom circuit to be appropriate. But, don't limit your thinking to traditional decisions between analog and digital activity. Many heretofore analog functions are increasingly being performed with digital MOS circuits.

THE CUSTOM MOS/LSI METHOD

Given that you have determined that you have the required circuit complexity, that your approach is economical, and that you have substantial digital function content, how do you go about obtaining the best custom MOS/LSI circuit for your application? The following steps are necessary:

- System Definition
- Electrical Feasibility Evaluation
- System Design and Partitioning
- Economic Analysis
- Parameter Specification
- Preliminary Logic Design and Stimulation
- Final Logic Design
- Chip Circuit Design
- Prototype Production
- Testing
- Production

There are two approaches available from AMI for custom MOS/LSI circuit development. The first is for AMI to do the design and also produce the part. The second approach is – "you design, we produce". Both involve AMI and the customer acting as a team.

Either way, you are going to experience a satisfying realization that your device has the advantage of the most appropriate MOS process, resulting in the highest performance, best reliability and lowest production cost possible. After all, you have formed a partnership with the company that has been committed to MOS/LSI exclusively for almost a decade.

In this partnership we will do our part by providing you with personalized engineering assistance, often resulting in a product with lower power dissipation, improved functional capability, greater flexibility, and reduced cost. You will also benefit from AMI's series of design checks for every step of the way in the program, with the result that quality assurance will be built-in. Checks and inspections will continue throughout the design and production cycles, instead of being an "add-on" at the end of the manufacturing process.

On your part, you can become involved, at almost any point during the development cycle, from system definition to wafer sort. Customer interface is a continuing and highly adaptable facet of AMI's custom circuit capability. This interface flexibility is required, because we at AMI realize that each device requires solu-

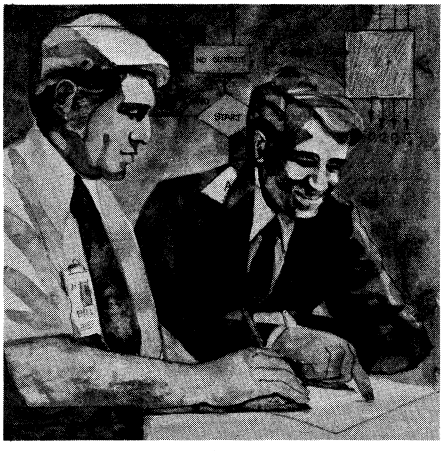
tions to different problems and may need working with the customer at different levels.

The "Let AMI Do Everything" Approach

AMI's total custom circuit capability encompasses the entire development sequence of a product. The services which AMI provides to the customer start with five conceptual planning steps:

- System Definition
- System Design and Partitioning
- Preliminary Logic Design and Simulation
- Final Logic Design
- Chip Circuit Design

First, system definition requires both full knowledge of the customer's requirements and MOS technological expertise. The right combination assures the best application of MOS/LSI. The user best knows system needs, the MOS designer best knows circuit capability. Working as a team, they can develop a final system which not only meets the needs, but optimizes performance and economy.

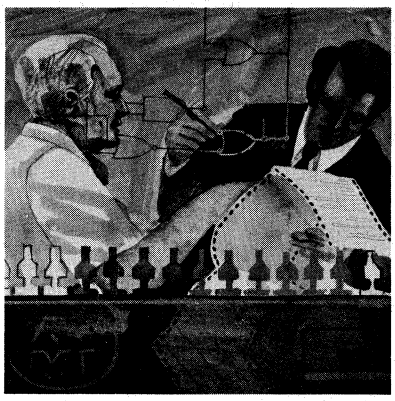


Step two, system partitioning, follows the joint development of the system definition. Partitioning involves the cataloging of functions into MOS subfunctions and then into chip functions. At this step of the program, the best MOS process for the application is selected. Usually, functional flow charts and timing diagrams are generated at this time, as a preliminary step in the logic design.

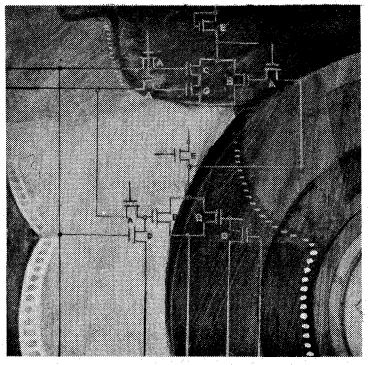
Once partitioning is accomplished, preliminary logic design and simulation can be done. The chip functions, as cataloged in step two, are translated into MOS logic diagrams. Traditional breadboarding techniques are quite often used to verify these logic designs. AMI also uses proprietary computerized simulation programs for verification. These programs check the design, functional capability, and efficiency of the design, as well as help reduce time and cost factors for design verification.

Final logic design is next. First, errors discovered through breadboarding or simulation are corrected. Earlier partitioning may be refined if the final logic

design indicates the need. During the final logic design step, all system design objectives are analyzed again. MOS logic diagrams are finalized, chip sizes are estimated, and testing procedures are generated.



And then – chip circuit design. The topological chip layout is a precise science. The exact dimensions and placement for each transistor and other functions must be determined. The list of factors affecting chip design is almost endless: the use of space, the economy of functions, the versatility of functions, the power requirements, the manufacturing processes, the interconnections, the packaging, the performance of the circuit, the reliability of the design. All these and more must be incorporated in the chip circuit design leading to final topological definition. Here again, AMI uses computerized circuit analysis programs to validate chip design and verify that the design meets the performance objectives determined during system definition. The computerized analysis not only substantiates the logic, it is an integral part of the on-going quality assurance program at AMI.



The "You Design, We Produce" Approach

This is an unique approach to custom MOS/LSI design, developed by AMI. You design the circuit and thus control the design budgets, the design schedules, the design changes prior to tooling, the logic and electrical requirements of the device, as well as the possibility of multiple sourcing the device. Another factor of great importance is that the MOS/LSI circuit can become cost effective in lower volume.

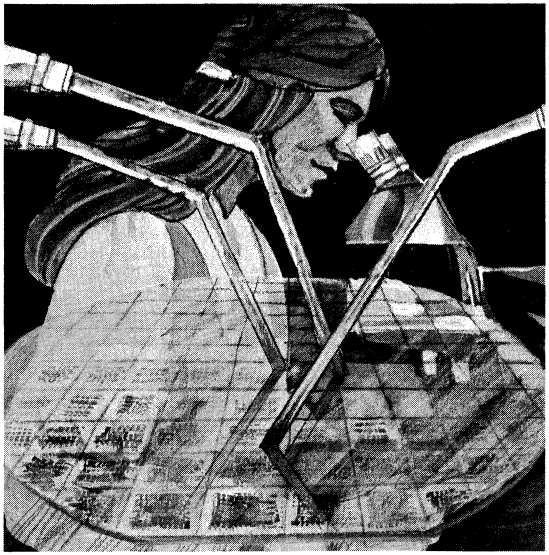
The actual device can be designed by you, or by your design consultant, who can implement your requirements into a compatible MOS/LSI design. Then, AMI will manufacture the device with the same high quality, high volume production processes used for AMI's own custom and standard circuits. (AMI can also assist you in locating a design consultant.)

Now, if you are going to investigate customer tooling (our name for producing your design), how do you go about it? Probably the best approach would be to become familiar with the AMI Four Step system. Four simple steps that work as follows:

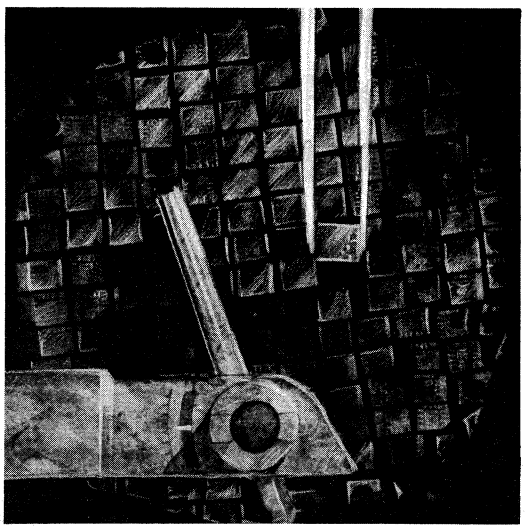
- Step One – Feasibility Study
- Step Two – Prototypes
- Step Three – Yield Evaluation
- Step Four – Production

Step One is simply an investigation and analysis of your requirements and their compatibility with our capability. There are many details to consider such as questions about process, design, packaging, testing, and tooling. AMI supplies a complete package of information to you or your design consultant containing all the necessary process parameters, design rules, packaging, testing, and tooling requirements to enable your design to be completely compatible with AMI's manufacturing standards. Upon completion of Step One, you are supplied on a no-charge basis a development plan, a firm quotation for prototypes and yield evaluation, and a budgetary estimate for production.

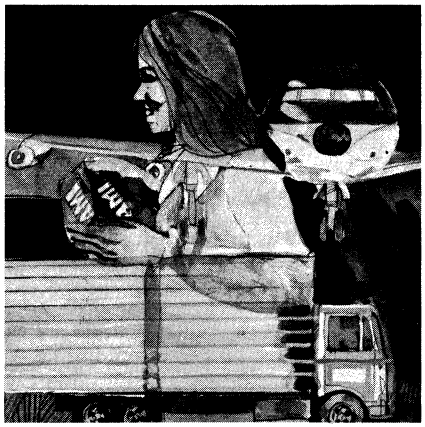
Step Two delivers to you sufficient optically inspected assembled parts to check the functionality of your design. Although the prototype devices are not functionally tested, they are guaranteed to be within the specified process parameters and of high quality and workmanship.



Once Step Two devices are approved, Step Three starts a multifaceted operation. Manufacturing documentation is generated, including test programs; wafer probe cards and program boards for the testing equipment are built; wafer reproducibility runs are made and then evaluated for yield factors. When it's all over, assembled tested devices are delivered to you for your evaluation. There is a charge for Step Three, based upon the complexity of the test program and the number of units delivered.



Step Four normally provides devices in production quantities within ten to twelve weeks after your approval of preproduction units delivered during Step Three.



Design Workshop

AMI offers still another service in the Customer Tooling area – a design workshop. Design workshops are offered to our customers on a continuing basis, for MOS logic and circuit designers who would like to become more familiar with the intricacies of AMI's requirements and manufacturing standards for custom MOS/LSI designs.

The design workshop is recommended for those customers planning to design circuits which will be manufactured by AMI. Generally a design workshop covers your requirements, as related to selected processes, suggested design ideas for the selected application, design rules, process parameters, possible tooling interfaces, and testing. Workshop programs are tailored to individual customer requirements in such a manner that the circuits which you design, as a result, can be processed, tested, and produced in quantity, using AMI's standard processes and manufacturing procedures.

AMI OFFERS MORE

When it comes to technologies, production facilities, quality assurance and testing, AMI offers more. As an MOS industry leader, the company is continuously investigating and researching new processes, production developments and other techniques to improve product capability, reliability, and cost effectiveness. Cur-

rently, a total of six MOS processes are used at AMI. Only those processes which prove reliably reproducible in a production environment are used.

P-channel, high voltage metal gate is the most widely used process in the industry. It is a relatively simple process, with the lowest wafer production costs. In addition to this cost advantage, P-channel metal gate MOS provides high noise immunity, ideal in applications involving mechanical equipment which can generate rf noise. Because of the high voltage, however, the circuits are a little more difficult to interface with bipolar circuits. They are also less efficient in chip area use, when compared to newer processes. As a result, chips are often larger, particularly for high speed circuits, and they are less cost effective.

P-channel, low voltage metal gate process is almost identical to the high voltage process with the significant difference being the use of a different silicon starting material. This provides a much lower threshold voltage and makes the interface with bipolar circuits much easier. This silicon material also reduces device breakdown voltages, somewhat reducing operating margins inside the chip. This process is quite suitable for low cost, moderate speed circuit applications.

Ion implantation (I^2) process adds one or two ion implantation steps to the high voltage P-channel metal gate process. The first step lowers the threshold voltage of all transistors by a specified amount. The addition of a second implantation step alters the threshold voltages of selected transistors causing them to operate in depletion mode. This provides several advantages: improved speed, lower power, improved noise margins, and easier bipolar interfaces. It also permits the use of unregulated power supplied and allows on-chip generation of full amplitude signals, using only one power supply. The full amplitude signal feature can be very useful for circuit simplification by converting logic into simpler forms, with a resulting decrease in chip area. In addition, the high breakdown voltages of the high voltage process are not disturbed. Therefore, I^2 metal gate processing is appropriate for chip applications where speed, noise immunity, and wide power supply tolerances are important.

The P-channel silicon gate, or SiGate, process offers two main features: a smaller transistor structure, resulting from a self-aligning fabrication technique eliminating some masking tolerance considerations, and the existence of a partial third layer of interconnect, which can reduce both cell area and cell interconnec-

Comparison of AMI's MOS Processes

Parameter	P Channel Hi V_T Metal Gate	P Channel Lo V_T Metal Gate	P Channel I^2 Metal Gate	P Channel Si Gate	N Channel Si Gate	Complementary MOS
Speed (per unit area)	5	6	3	4	2	1
Power Consumption (low speed)	6	4	2	5	2	1
Area (per logic function)	4	5	2	2	1	6
Noise Immunity	3	4	1	4	6	1
Logic Flexibility	3	3	1	3	3	2
On-Chip Clock Generation	4	3	2	5	5	1
Bipolar Compatibility	6	4	3	4	1	1
Power Supply Latitude	3	5	1	3	5	1
Process Simplicity	1	1	3	3	3	6
Process Maturity	1	1	3	3	6	5

Rankings are relative among the processes, with the lowest number being most desirable.

tions. The self-aligning gate structure lowers the effective gate capacitance, providing faster circuits than regular P-channel, although not as fast at ion implanted circuits. The lower gate capacitance, however, does make bootstrap techniques for generating full amplitude signals a little harder to implement.

The N-channel silicon gate process produces devices much faster than P-channel devices. N-channel SiGate gives high speed and high device density with easier bipolar compatibility, since the transistors are more comparable to NPN, as opposed to PNP. Devices made with N-channel SiGate process do tend to be more voltage sensitive and exhibit an associated reduction in noise immunity. At present, this process is used for high performance applications, but is expected to be cost effective for a wide variety of applications as it matures.

The most complex MOS process, which receives much attention, is **Complementary MOS or CMOS.** This process produces circuits which draw no static power – power dissipation occurs only when switching between logic states in process. As the operating frequency increases, though, power dissipation does approach that of other MOS technologies. The CMOS process can provide fast circuits with high noise immunity. Also, CMOS circuits can work over wide power supply tolerances and require a single voltage supply.

At present, chip area use per logic function is rather high with CMOS, but this can be expected to decrease as design experience is gained. Circuits using CMOS technology are used in extremely low power applications, such as in electronic watches, and in automotive applications. Most applications encountered thus far have been in battery-powered or telephone-line powered systems.

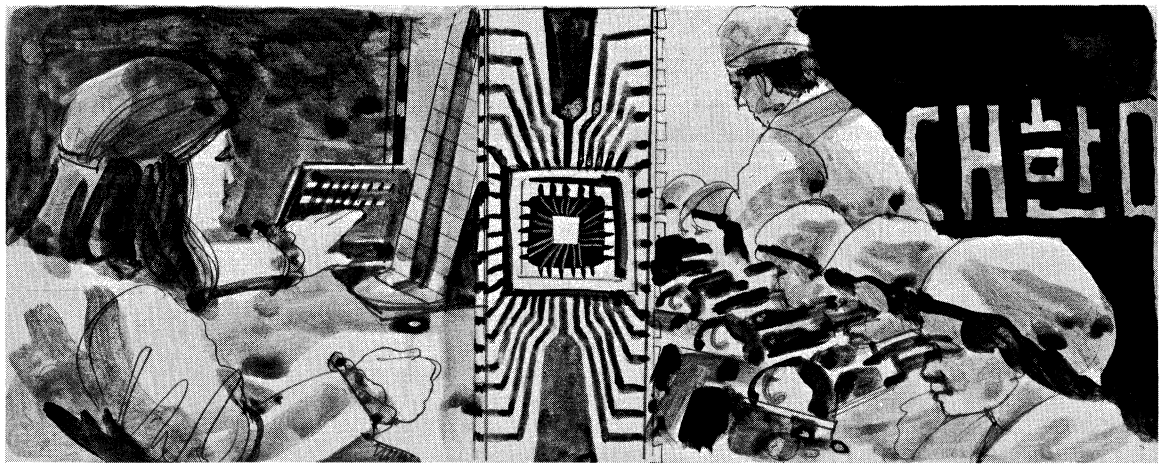
EQUIPMENT AND FACILITIES

All of the extensive automated equipment and the modern facilities at AMI's three main production locations are available for custom circuit production. Combined with the unmatched design experience of the largest MOS design engineering staff ever assembled, these facilities provide an unprecedented MOS/LSI circuit capability.

Advanced design tools at AMI include an on-site Burroughs 6700 computer with terminals located at the Santa Clara and Pocatello engineering facilities, two Computervision interactive graphics systems for on-line generation and editing of computerized composite data bases; high speed and high resolution Electromask pattern generators; high speed Calcomp plotting facilities; Fairchild Sentry 600 LSI testers; AMI proprietary PAFT and IMPACT testers; Macrodata MD-150 testers; and CAD software for logic and system simulation, circuit analysis, automated design fule checking, test pattern generation, and ROM masking. All these support AMI's engineering staff.

PRODUCTION

At the headquarters facility in Santa Clara, California, approximately 30% of the nearly 200,000 square foot production facility is clean room area. Each of the modular manufacturing units for wafer production is



dedicated to a single production process. There are four such modules at Santa Clara, two for full-scale production, one for engineering prototyping, and one for research and development. The two production modules can together produce in excess of one million devices per month. A significant factor in AMI's high volume production capability is that all wafer fabrication facilities produce 3-inch diameter wafers.

Automation plays an important role with use of automatic and semi-automatic equipment for spinning, baking, and photodeveloping. Automation also is used in testing and wafer handling equipment.

The Pocatello, Idaho plant at present encompasses almost 100,000 square feet and is also using the modular wafer fabrication concept. Four fabrication modules with a combined monthly capacity in excess of two million devices augment the Santa Clara production capacity.

In Korea, a wholly-owned subsidiary, Korean Microsystems, Inc., near Seoul, performs the majority of the assembly operations. Experienced personnel and new equipment, including the latest lead-bonding machines, provide KMI with an assembly capability of approximately three million devices per month, keeping pace with the wafer production capacity of Santa Clara and Pocatello. Over 1,200 employees work in the 84,000 square foot facility of KMI.

PACKAGING

A wide range of standard packages and packaging approaches is available, providing cost effective solutions for the majority of typical applications. Packages include TO cans, flat packs, and DIPs. All common lead configurations are available in ceramic, Cer-DIP, SLAM and plastic packages. (See Section 1 of this catalog.) LID and other special packages are also available.

TESTING

As mentioned earlier, the automated testing facilities available at AMI are extensive. A broad range of powerful testing units from Fairchild, Macrodata, and of AMI's own design, handle almost any testing requirement. For custom circuit devices it is preferable to supply test programs in formats suitable for one of the tester types used. However, test programs can be written, or rewritten, by AMI test group personnel. Information on all test equipment available at AMI is available on request. Detailed information on the Fairchild and Macrodata testers is available from the manufacturers.

QUALITY ASSURANCE

The AMI Quality Assurance program is an on-going process – a part of the design and manufacturing process. The following is a partial list of the quality control checkpoints in the creation of a custom circuit. These steps include meticulous checks of both design and workmanship.

- Final logic design (system objectives are reviewed)
- Chip circuit design (uses computerized circuit analysis to verify that performance meets objectives)
- Topological design
- Artwork generation
- Mask fabrication
- Wafer fabrication
- Wafer sort (functional requirements are checked)
- Scribe and break with 100% optical inspection
- Die attach
- Lead bonding followed by 100% pre-seal optical inspection
- Seal
- Final test
- Final electrical and environmental product assurance tests

Only after the checks at all these steps have been completed is a device considered fully manufacturable. It is then turned over to production with its yield history. The production facility continues its own quality control checks, starting from wafer fabrication on through final quality assurance tests.

CUSTOM MOS/LSI FROM AMI

The information in this section has been presented to show not only how and why custom can be used, but also to explain the types of custom services available at AMI, and the level of commitment at AMI to total custom circuit development and to customer tooling processing. If your application can benefit from high quality custom MOS/LSI circuits, AMI is the place to go for design, engineering, manufacturing, and testing capability. To get in contact with AMI Custom, just complete the inquiry card at the back of this catalog.

4

Random Access Memories
Shift Register Memories

Future Products

RAM – 256 x 4 bit Static, CMOS

RAM – 1024 x 1 bit Static, CMOS

RAM – 4096 x 1 bit Dynamic,
N-Channel, 16-pin Package

Selection Guide-RAMs and Shift Registers

Random Access Memory Standard Products

Part No.	Organization	Process	T_{Acc} (ns)	R/W T_{Cycle} (ns)	Operating Power (mW)	Standby Power (mW)	Supplies (V)	I/O	Clocks	Package	See Page
S2222	512 Static	CMOS	200	470	7.5	0.002	+10	MOS	0	2H, 1U	4-4
S2222A	512 Static	SiGate	400	940	7.5	0.01	+10	MOS	0	2H, 1U	4-4
S1103	1024 Dynamic	P-SiGate	310	580	450	–	+16, +19	MOS/Sense A	3	2P, 1P	4-8
S146	1024 Dynamic	P-SiGate	210	390	550	–	+19, +22	MOS/Sense A	3	2P, 1P	4-8
S1103-1	1024 Dynamic	P-SiGate	180	360	550	–	+19, +22	MOS/Sense A	3	2P, 1P	4-8
S1103X	1024 Dynamic	P-SiGate	120	270	550	–	+19, +22	MOS/Sense A	3	2P, 1P	4-8
S1103A	1024 Dynamic	P-SiGate	205	580	425	2.0	+16, +19	MOS/Sense A	3	2P, 1P	4-23
S1103A-1	1024 Dynamic	P-SiGate	145	340	660	0.2	+19, +22	MOS/Sense A	3	2P, 1P	4-23
S1103A-2	1024 Dynamic	P-SiGate	145	400	600	0.2	+19, +22	MOS/Sense A	3	2P, 1P	4-23
S4006	1024 Quasi-Static	P-I^2	400	650	450	50	–12, +5	TTL	0	2H, 4H	4-27
S4008	1024 Quasi-Static	P-I^2	500	900	450	50	–12, +5	TTL	0	2H, 4H	4-27
S4008-9	1024 Quasi-Static	P-I^2	800	1000	450	50	–12, +5	TTL	0	2H, 4H	4-27
S6605	4096 Dynamic	N-SiGate	210	490	335	4(1)	+12, ±5	TTL	1	2C,1C	4-32
S6605A	4096 Dynamic	N-SiGate	300	590	335	4(1)	+12, ±5	TTL	1	2C,1C	4-32
S6605B	4096 Dynamic	N-SiGate	600	880	335	4(1)	+12, ±5	TTL	1	2C,1C	4-32
S6810	1024 Static	N-SiGate	1000	1000	650	N/A	+5	TTL	0	2L,1W	4-40
S6810-1	1024 Static	N-SiGate	575	575	650	N/A	+5	TTL	0	2L,1W	4-40

Shift Register Memory Standard Products

Part No.	Organization	Max. Data Rate (MHz)	Power(2) (mW)	Supplies (V)	I/O	Clocks	Package	See Page
S1685	Dual 480 Dynamic	1	120	+5, –12	TTL/MOS	2	5F	*
S2181	Dual Var. 133 Static	1	400	+5, –12	TTL/MOS	1	2H	*
S2181A	Dual Var. 133 Static	2	400	+5, –12	TTL/MOS	1	2H	*
S2182	Quad 80 Static	1	565	+5, –12	TTL/MOS	1	4H	*
S2182A	Quad 80 Static	2	565	+5, –12	TTL/MOS	1	4H	*
S2183	Quad 81 Static	1	565	+5, –12	TTL/MOS	1	4H	*
S2183A	Quad 81 Static	2	565	+5, –12	TTL/MOS	1	4H	*
S2184	Quad 132 Static	1	565	+5, –12	TTL/MOS	1	4H	*
S2184A	Quad 132 Static	2	565	+5, –12	TTL/MOS	1	4H	*
S2185	Quad 133 Static	1	565	+5, –12	TTL/MOS	1	4H	*
S2185A	Quad 133 Static	2	565	+5, –12	TTL/MOS	1	4H	*

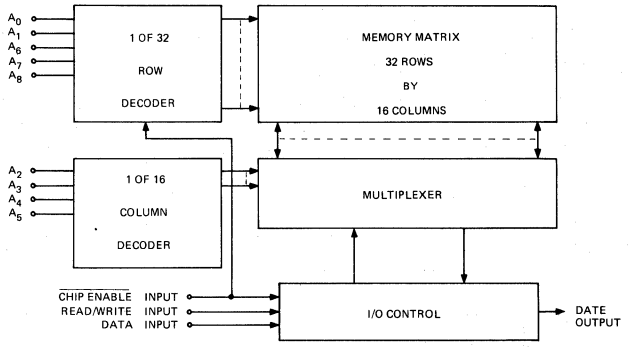
***Contact your nearest AMI Sales Office for additional data sheet information on this product (See Section 1)**

Notes: (1) With refresh
(2) Typical at 25°C ambient and maximum data rate.

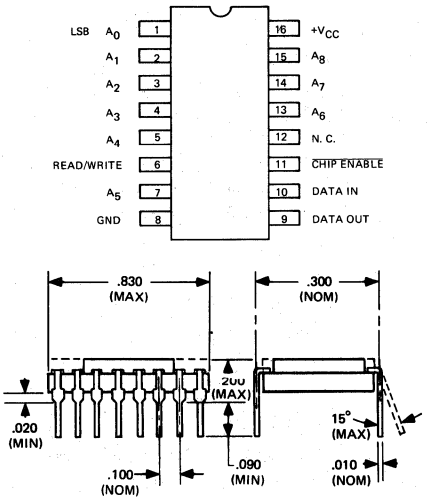
S2222
S2222A

512 X 1 STATIC CMOS
RANDOM ACCESS MEMORY

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2H, 1U - see Sec. 1)

FEATURES

- Low Standby Power – 4/20 nW/bit Typ.
- Fast Access Time – 200/400 nS Typ.
- Fast Cycle Time – 470/940 nS Min.
- Single Supply Voltage – +10 Volts
- Standby Supply for Non-volatility – 3.5 Volts Min.
- Static Memory – No Refresh
- Wide Temperature Range
  0° - 70°C (- 55°C to + 125°C soon)
- Single Read/Write Control Line
- Simple Memory Expansion – $\overline{\text{Chip Enable}}$
- Silicon Gate Technology
- 16 Dual In-line Package

FUNCTIONAL DESCRIPTION

The AMI S2222 series are 512 word by one-bit random access memory arrays, constructed with silicon gate CMOS devices, integrated on a monolithic array. With full decoding on the chip, this memory uses fully DC stable (static) storage elements and requires no refresh to operate. The memory matrix is organized as 32 rows by 16 columns. The S2222/A series devices have a unique circuit design which allows Chip enable to precharge the internal nodes resulting in minimum power dissipation.

High speed operation and nanowatt power dissipation features make this memory useful in applications where power must be conserved or where battery operation is required.

TYPICAL APPLICATIONS

- Terminals
- Low Power/High Speed Buffer
- Battery Operated Systems
- Portable Calculators
- Time Clocks
- Military Systems

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	- 55° to 125°C
Storage Temperature	- 65° to 150°C
Voltage on any pin with respect to the Ground Pin	- .3V to 12V
Voltage on any pin with respect to the V_{CC} Pin	.3V to - 12V

COMMENT:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. CHARACTERISTICS
T_A = 0°C - 70°C, V_{CC} = 10V±5% unless otherwise specified

SYMBOL	PARAMETER	S2222 LIMIT MIN	S2222 LIMIT TYP	S2222 LIMIT MAX	S2222A LIMIT MIN	S2222A LIMIT TYP	S2222A LIMIT MAX	UNITS	TEST CONDITIONS
I_{LI}	Input Load Currents (All Input Pins)	–	–	1	–	–	5	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Output Leakage Current	–	–	10	–	–	10	μA	$\overline{CE}$ = V_{CC}, V_{OUT} = 4V
I_{CC1}	Standby Power Supply Current	–	0.2	5	–	1.0	25	μA	All inputs = V_{CC}
I_{CC2}	Maximum Power Supply Current	–	2.5	–	–	2.5	–	mA	T_{CYCLE} = T_{WC} Min All inputs changing
V_{IL}	Input "Low" Voltage	0	–	+ 0.6	0	–	+ 0.6	V	
V_{IH}	Input "High" Voltage	V_{CC} - 0.6	–	V_{CC}	V_{CC}-0.6	–	V_{CC}	V	
I_{OL}	Output "Low" Current	1	2.5	–	1	2.5	–	mA	V_{OL} = 0.45V
I_{OH}	Output "High" Current	–	–	10	–	–	10	μA	V_{OH} = 4.0V
V_{SP}	Standby Supply Voltage for Retention (See Note 7)	3.5	–	10	3.5	–	10	V	$\overline{CE}$ = V_{SP} All other inputs at V_{SP} or 0V

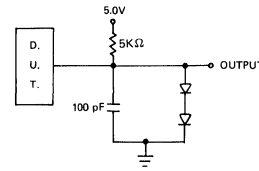
A. C. CHARACTERISTICS
T_A = 0°C - 70°C, V_{CC} = + 10V±5% unless otherwise specified

SYMBOL	PARAMETER	S2222 LIMIT MIN	S2222 LIMIT TYP	S2222 LIMIT MAX	S2222A LIMIT MIN	S2222A LIMIT TYP	S2222A LIMIT MAX	UNITS	TEST CONDITIONS
t_{ACC}	Access Time	–	200	350	–	400	700	nS	See Below
t_{RC}	Read Cycle Time	470	–	–	940	–	–	nS	See Below
t_{WC}	Write Cycle Time	470	–	–	940	–	–	nS	See Below
t_{CD}	$\overline{CHIP\ ENABLE}$ ($\overline{CE}$), Delay Time	40	–	–	80	–	–	nS	See Below
t_{CR}	$\overline{CE}$ Release Time	40	–	–	80	–	–	nS	See Below
t_{CH}	$\overline{CE}$ Hold Time	120	–	–	240	–	–	nS	See Below
t_{OD}	Output Release Time	–	30	70	–	60	140	nS	See Below
C_{IN}	Input Capacitance (A_{IN}, D_{IN}, $\overline{CE}$, R/W)	–	5*	10	–	5	10	pF	See Below

*A_{IN} and R/W Cap = 5 pF typ.
$\overline{CE}$ and D_{IN} = 8 pF typ.

(1) $t_r = t_f \leq 20$ nS
(2) Input Pulse Levels are 0.5V to V_{CC}
(3) Output Logic "0" < 0.7V
(4) Output Logic "1" > 0.7V
(5) $t_{CD} + t_{CR} = t_{CH}$ = 120 nS min.
(6) Test for 0.1V rise in output level
(7) t_{SP} (fall and rise time to $V_{SP} \geq 1$ Sec

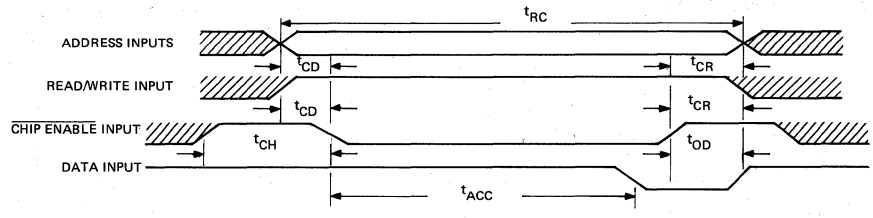
A. C. TEST CONDITIONS



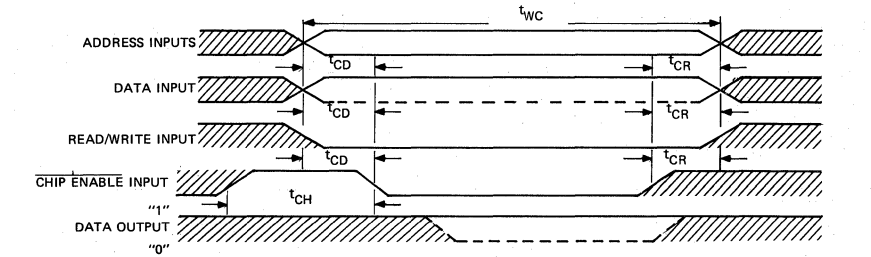
OPERATION

With the read/write input held at a logical "1" level, reading is accomplished by bringing the Chip Enable input to a logical "0" level. The address and read/write inputs must have been stable for at least 40 nS prior to the Chip Enable transition. Valid data will then occur at the output and remain for about 10 nS after the Chip Enable is returned to a logical "1" level. The output will sink current for a stored logical "0" (low) level and be disabled (floating) for a stored logical "1" (high).

With the read/write input at a logical "0", writing is accomplished by bringing the Chip Enable input to a logical "0". The address, data, and read/write inputs must have been stable for at least 40 nS prior to the Chip Enable transition and held for 40 nS after the completion of a write operation. During a write cycle the output will follow the input data.



READ CYCLE



WRITE CYCLE

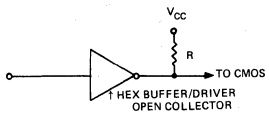
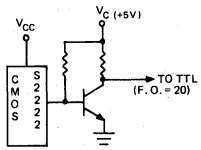


FIGURE 1 (a)
TTL TO CMOS INTERFACE



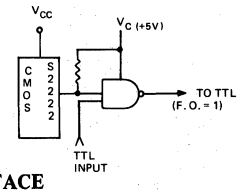


FIGURE 1 (b) CMOS TO TTL INTERFACE

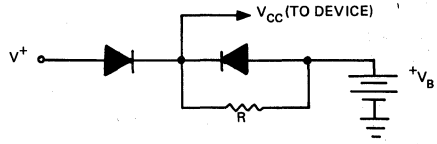


FIGURE 2 STANDBY BATTERY CIRCUIT

APPLICATIONS

Figure 3 shows a 2048 word by 8-bit static RAM memory system. The memory system is organized in an array of 4 rows by 8 columns. All data inputs and data outputs in a column are connected together to form a memory of 2048 words of 8-bit each. Additional bits are attained by paralleling the extra columns each made up of four, S2222/A. At the inputs to the CMOS memory, TTL devices can interface directly if an open-collector logic gate is used along with pull up resistor as shown in Figure 1 (a). Driver circuits are not required since the input capacitance is low (5.0 pF).

Figure 1 (b) shows methods of interfacing the memory outputs to TTL logic. With the + 10V V_{CC} supply voltage to a discrete transistor, or can fan out to a low power TTL gate as shown. The discrete transistor circuit provides higher speed and/or high fan-out.

Figure 2 shows an optional standby power supply circuit for making a CMOS memory "non-volatile". When the system power fails, a battery is used to sustain operation and maintain stored information. While the normal system power supply is present, the battery is trickle-charged through a resistor which sets the charging rate. Low-leakage diodes are recommended to conserve battery power. V_B is the sustaining voltage, and V^+ is the normal system power supply voltage.

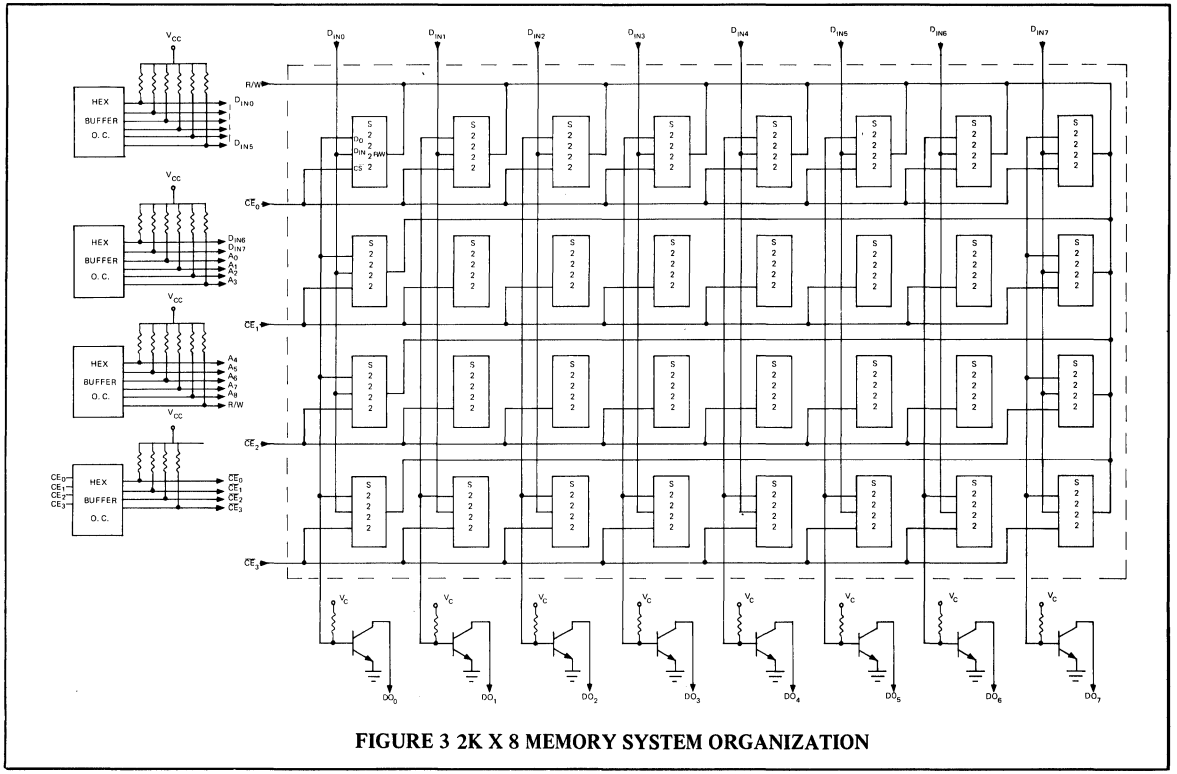
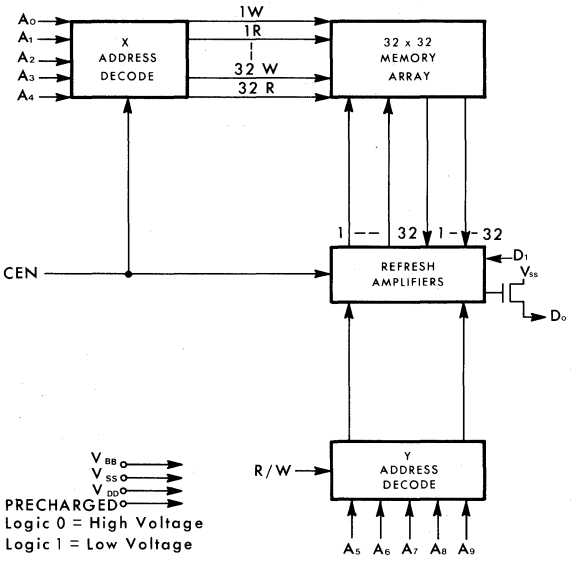


FIGURE 3 2K X 8 MEMORY SYSTEM ORGANIZATION

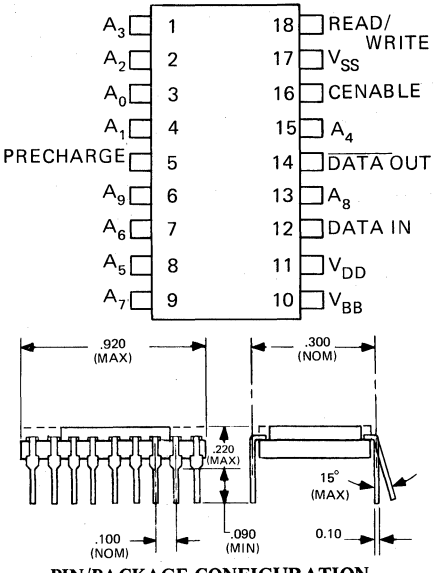
S1103
S146
S1103-1
S1103X

1024 x 1 RANDOM ACCESS MEMORY

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

(Available in Pkgs. 2P, 1P - see Sec. 1)

FEATURES

- Fast access time, 300/205/120ns
- Performance options subject to power supply levels
- Fast cycle time, 580/390/270ns
- Full internal decoding
- OR-tie capability
- Chip enable provides low power dissipation
- Simple memory expansion
- Inputs protected against static charge
- Refresh period, 2ms @ 0 to 70°C

FUNCTIONAL DESCRIPTION

The AMI S1103 family of random access memories are designed for applications where high performance, low cost and large bit storage are desired, such as main memories. It is a 1024 word by 1 bit array fabricated with low threshold, silicon gate technology. This high density process technology allows the design and production of extremely high performance memory devices.

The proven reliability of this process, and design, coupled with an extremely reliable plastic package, provide an exceptional solution for many memory systems cost and performance problems. The performance levels attainable are a function of the power supply levels used.

Some of the more important operational characteristics are discussed on the following page.

TYPICAL APPLICATIONS

Mainframe Memories, Add-On Memories, Cache Memories, Buffer Memories, Minicomputer Memories, Mass Memories, Terminals.

Operating Ambient Temperature	
S1103	0° to +70°C
S146/S1103–1/S1103X	0° to +55°C
Storage Temperature	– 65° to +150°C
All Input or Output Voltages with respect to the most Positive Supply, V_{BB}	– 25V to 0.3V
Supply Voltages V_{DD} and V_{SS}	– 25V to 0.3V
Power Dissipation.	varies with device

Stresses above maximum ratings may cause permanent device damage. This is a stress rating only; functional operation of the device at any other condition above that indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATION

The block diagram, schematic, and timing diagram, assist in the understanding of the operation of the S1103 family. Some important characteristics relative to system design are:

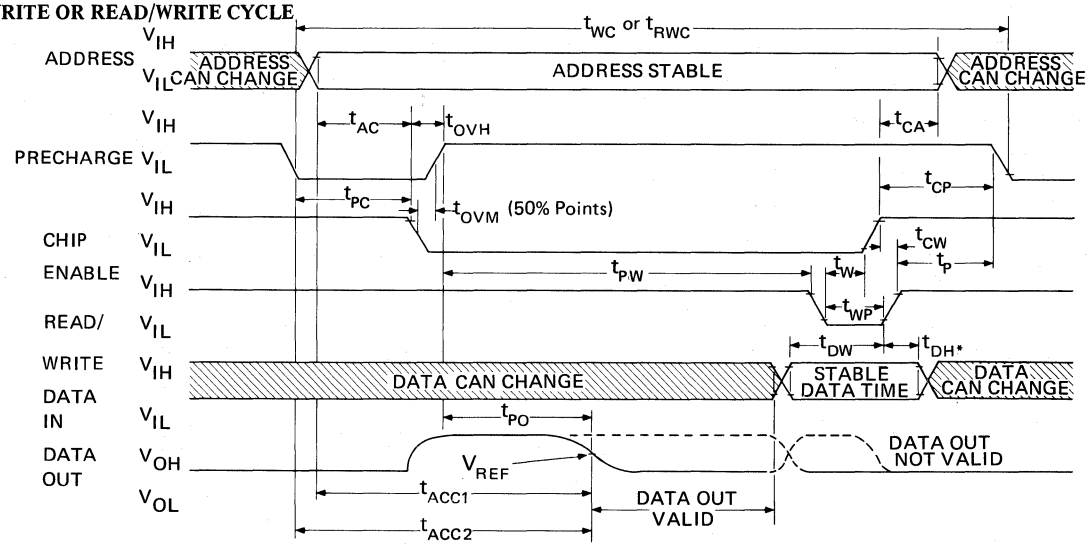
a) Periodic refreshing is required due to dynamic operation. The device must be cycled through the 32 addresses of the A0 – A4 inputs at least every 2 ms.

b) The memory precharge should be held positive on all but the enabled chips to reduce power dissipation. If the precharge input is negative and runs 30% duty cycle, at minimum cycle time, the dissipation is typically 350 mW for the S1103 and 550 mW for the S146, S1103–1 or S1103X.

c) Cell readout is non-destructive so the read/write cycle may be shortened for a read only or refresh only cycle, as the read/write pulse is only required for entry of new data. Thus a read only or refresh only cycle can be shorter than a read/write or a write only cycle.

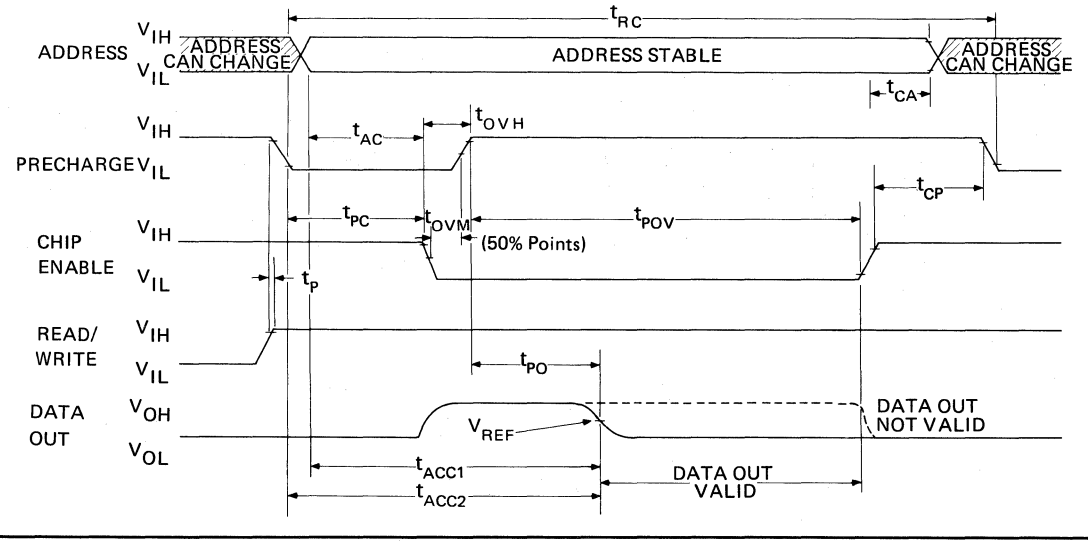
d) A high input (positive) is read as zero current out, and a low input written into the memory is read as current out.

WRITE OR READ/WRITE CYCLE

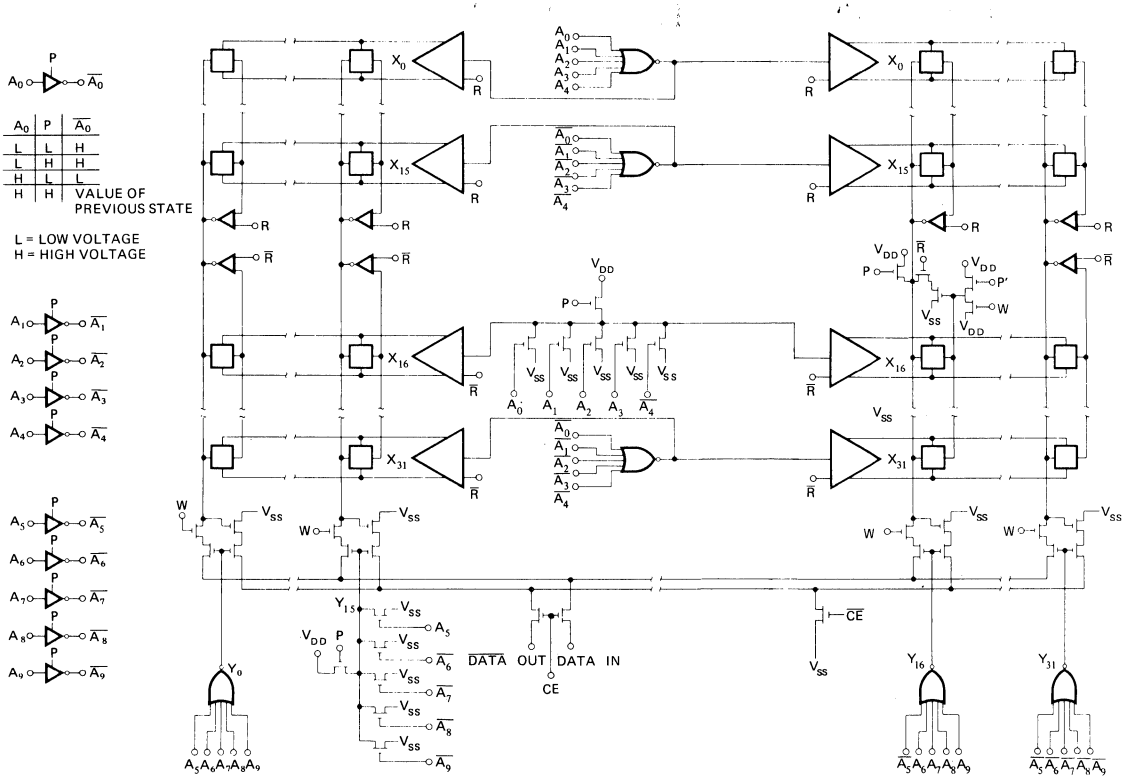


*t_{DW} and t_{DH} are referenced to the rising edge of Chip Enable or Read/Write, whichever occurs first.

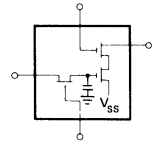
READ OR REFRESH CYCLE

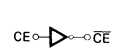


CIRCUIT DIAGRAM



BASIC MEMORY CELL





CE	P	P'
L	L	H
L	H	H
H	L	L
H	H	VALUE OF PREVIOUS STATE

P = PRECHARGE
CE = CENABLE
W = READ/WRITE
LOGIC 0 = HIGH VOLTAGE (H)
LOGIC 1 = LOW VOLTAGE (L)
V_{BB} = SUBSTRATE VOLTAGE

OPERATING, AC AND DC CHARACTERISTICS

OPERATING CHARACTERISTICS		S1103		S146		S1103–1		S1103X		UNITS
SYMBOL	TEST DESCRIPTION									
T_A	Ambient Temperature	0 to 70		0 to 55		0 to 55		0 to 55		°C
V_{DD}	Negative Supply	0		0		0		0		V
V_{SS}	Positive Supply (1)	16 ± 0.8		19 ± 1		19 ± 1		19 ± 1		V
$V_{BB} - V_{SS}$	Substrate Supply (2)	3.5 ± 0.5		3.5 to 0.5		3.5 ± 0.5		3.5 ± 0.5		V
C_L	Load Capacitance	100		100		50		50		pF
R_L	Load Resistance (3)	100		100		100		100		Ω
V_{REF}	Output Reference Voltage	40		80		80		80		mV
		S1103		**S146**		**S1103–1**		**S1103X**		**UNITS**
AC CHARACTERISTICS		**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	
	READ, WRITE AND READ/WRITE CYCLE									
t_{REF}	Time between Refresh Cycles		2		2		2		2	ms
t_{AC}	Address to Chip Enable Setup Time	115		65		30		30		ns
t_{CA}	Chip Enable to Address Hold Time	10		10		10		10		ns
t_{PC}	Precharge to Chip Enable Delay	125		70		60		35		ns
t_{OVM}	Precharge and Chip Enable Overlap	45	95	25	65	25	50	13	35	ns
t_{OVH}	Precharge and Chip Enable Overlap		140		85		85		85	ns
t_{CP}	Chip Enable to Precharge Delay	85		50		40		40		ns
	READ CYCLE									
t_{RC}	Read Cycle (4, 5)	480		330		300		238		ns
t_{POV}	Precharge to end of Chip Enable	165	500	130	500	115	500	114	500	ns
t_{PO}	Precharge to Output Delay		120		100		75		65	ns
t_{ACC1}	Address to Output Access (4, 6)		300		205		150		120	ns
t_{ACC2}	Precharge to Output Access (4, 7)		310		210		180		125	ns
	WRITE OR READ/ WRITE CYCLE	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNITS**
t_{WC}	Write Cycle (4, 8)	580		390		360		270		ns
t_{RWC}	Read/Write Cycle (4, 9)	580		390		360		270		ns
t_{PW}	Precharge to Write Delay	165	500	130	500	115	500	114	500	ns
t_{WP}	Write Pulse Width	50		40		40		20		ns
t_W	Write Setup Time	80		40		40		20		ns
t_{DW}	Data Setup Time (10)	105		40		40		25		ns
t_{DH}	Data Hold Time (11)	10		10		10		10		ns
t_{PO}	Precharge to Output Delay		120		100		75	60	65	ns
t_P	Time to Next Precharge	0		0		0		0		ns
t_{CW}	Chip Enable to Write		15		15		15		15	ns

AC CHARACTERISTICS (Cont'd)

		TYP.	MAX.	UNITS	CONDITIONS
	CAPACITANCE (12)				
C_{AD}	Address	5	7	pF	$V_{IN} = V_{SS}$
C_{PR}	Precharge	15	18	pF	$V_{IN} = V_{SS}$
C_{CE}	Chip Enable	15	18	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write	12	15	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input	5	7	pF	Enable = V_{DD}, $V_{IN} = V_{SS}$
C_{IN2}	Data Input	3	5	pF	Enable = V_{SS}, $V_{IN} = V_{SS}$
C_{OUT}	Data Output	3	4	pF	$V_{OUT} = V_{DD}$

All Unused Pins @ AC GND; f_0 = 1 MHz; V_{BB} = 3.0V

DC CHARACTERISTICS		S1103 MIN.	S1103 MAX.	S146/S1103-1/S1103X MIN.	S146/S1103-1/S1103X MAX.	UNITS	CONDITIONS
I_{LI}	Input Leakage Current		1		1	µA	$V_{IN}=V_{DD}$; All Unused
I_{LO}	Output Leakage Current		1		1	µA	$V_{OUT}=V_{DD}$;Pins at V_{SS}
I_{BB}	Substrate Supply Current		100		100	µA	
I_{DD1}	Supply Current During T_{PC}		56		75	mA	Address Prechg=V_{DD}; CE=V_{SS} T_A = 25°C
I_{DD2}	Supply Current During T_{OV}		59		80	mA	Address=Prechg=CE=V_{DD}; T_A = 25°C
I_{DD3}	Supply Current During T_{POV}		11		13	mA	Address=CE=V_{DD}; Prechg=R/W=V_{SS}; T_A = 25°C
I_{DD4}	Supply Current During T_{CP}		4.2		5	mA	Address=V_{DD}; Prechg=CE=R/W=V_{SS}; T_A = 25°C
I_{DDAVG}	Average Supply		25		33	mA	All Timing Parameters @ Min. Condition;T_A=25°C
I_{OH}	Output High Current	500	4000	850	5000	µA	Over Temperature Range
I_{OL}	Output Low Current		400		800	µA	Over Temperature Range
V_{IL1}	Input Low Voltage (14) (All Add/Data In)	V_{DD}	V_{DD}+1.8	V_{DD}	V_{DD}+1	V	Over Temperature Range
V_{IL2}	Input Low Voltage (Precharge, Ce, RW)	V_{DD}	V_{DD}+1.3	V_{DD}	V_{DD}+1	V	Over Temperature Range
V_{IH}	Input High Voltage	V_{SS}–1	V_{SS}+1	V_{SS}–1	V_{SS}+1	V	Over Temperature Range
V_{OH}	Output High Voltage	50	400	85	500	mV	Over Temperature Range
V_{OL}	Output Low Voltage		40		80	mV	Over Temperature Range

NOTES:

1. V_{SS} current drain is equal to (I_{DD} + I_{OH}) or (I_{DD} + I_{OL})
2. (V_{BB} – V_{SS}) supply should be applied before V_{SS}.
3. R_L of 100 Ω is chosen for convenience. In application,R_L may range from 100 to 1000 Ω.
4. t_T is defined as the time between the 10% and 90% point of any voltage transition (t_T = 20ns).
5. $t_{RC} = t_{PC} + t_{OVM} + t_{POV} + t_{CP} + 3t_T$
6. $t_{ACC1} = t_{AC} + t_{OVM} + t_{PO} + t_T$
7. $t_{ACC2} = t_{PC} + t_{OVM} + t_{PO} + t_T$
8. $t_{WC} = t_{PC} + t_{OVM} + t_{PW} + t_W + t_{CP} + 4t_T$
9. $t_{RWC} = t_{PC} + t_{OVM} + t_{PW} + t_W + t_{CP} + 4t_T$
10. t_{DW} is referenced to the 90% (negative) point of the rising edge of Chip Enable or Read/Write whichever occurs first.
11. t_{DH} is referenced to the 10% (positive) point of the rising edge of Chip Enable or Read/Write whichever occurs first.
12. All capacitances are periodically sampled and not 100% tested. Capacitance values are for either plastic or ceramic packages.
13. This parameter is periodically sampled and is not 100% tested.
14. V_{IL} Max. and V_{IH} Min. are a linear function of T_A between 0°C to 70°C. Interim values may be calculated accordingly.

S1103 SYSTEMS ORGANIZATION

Figure 1 shows a 4096 x 9 bit self contained asynchronous memory system. It communicates to the mainframe with three control signals.

Cycle Request is a signal which is generated by the mainframe demanding action by the memory.

Read/Write is also generated by the mainframe in association with the request signal and indicates whether a read or write operation is requested.

Ready is generated by the memory system in response to the request signal issued by the mainframe. The memory system goes busy (not ready) at the receipt of the request. At the conclusion of the memory cycle, the ready line again becomes true, and additional requests may be accepted. The cycle length for a read cycle may be made shorter than for a write cycle.

The mainframe also supplies addresses and data for writing and accepts data read from the memory.

The organization shown in Figure 1 uses common precharge and read/write drivers. By decoding precharge as well as cenable, the memory power consumption may be significantly reduced. For a 4096 word memory, full decoding of precharge can reduce DC power dissipation and clock driver losses by a factor of about 3. However, the extra level-shift circuits needed may offset some of these power savings. The decoding of precharge also reduces the noise coupled to the sense lines.

Dynamic MOS storage requires periodic refreshing of data. For the S1103, this refreshing may be accomplished by cycling through the 32 possible states of address lines A_0–A_4 in every 2 ms period.

To guarantee this condition for a random access memory, special refresh cycles may be executed by the controller. For a 600 ns cycle the refresh operation requires less than one percent of available memory cycles.

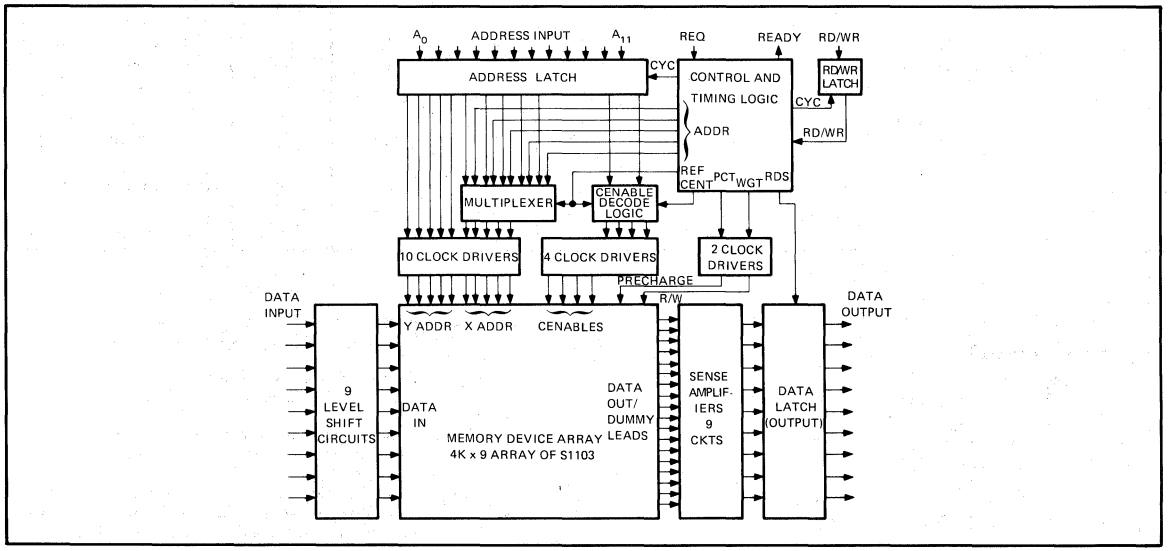
To permit a memory with S1103 to interface with TTL logic and provide this simple mode of operation, certain peripheral circuits are required. These circuits are shown as blocks in Figure 1.

Data Input Level-Shift. Converts data supplied for writing at TTL levels to MOS levels. These circuits need drive only the light capacitive load represented by four (for this memory) data input leads.

Sense Amplifiers and Latches. These circuits convert the currents read from the device to TTL levels and provide storage for subsequent use by the computer.

With a system such as shown in Figure 1 a certain amount of noise may be introduced by capacitive coupling of precharge,

S1103 MEMORY SYSTEM BLOCK DIAGRAM (4096, 9-BIT BYTES) - FIGURE 1



S1103 SYSTEMS ORGANIZATION (Cont'd)

and cenable signals to the sense lines. This noise may be reduced by running a dummy sense line in parallel and using a differential input sense amplifier. The transitions are then coupled equally into the sense line and the dummy line.

Address Latches and Clock Drivers. These circuits accept and store the address. Clock drivers convert the TTL levels to MOS levels, providing sufficient capability to drive the capacitance represented by the full array of devices.

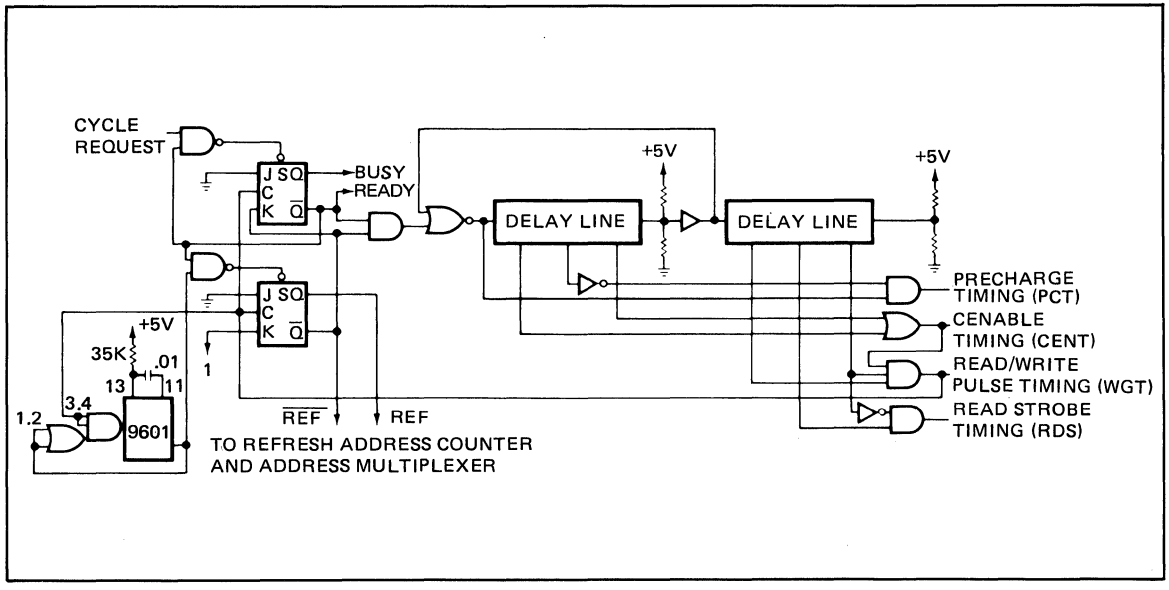
CONTROL CIRCUITS

The controller shown in Figure 2 is used to generate the timing and refresh control signals for an S1103 memory. The upper flip-flop (normal-cycle control flip-flop) acknowledges requests for memory cycles by entering the busy state (Q output a logic 1) the lower flip-flop (refresh cycle control flip-flop) and single shot (multivibrator) perform refresh cycle control. Any cycle executed with the lower flip-flop on is considered a refresh cycle.

The multivibrator requests a refresh cycle every 60μs. Refresh cycles can only be initiated when the normal cycle control flip-flop is in the ready state (Q output a logic 1). Execution of either type of cycle is accomplished by sending a signal down the delay line. The cycle timing signals are then derived from taps along the delay line. To maintain suitable delay to rise-time ratios, two delay lines with a buffer stage in between them have been used. The signal from the buffer stage which is fed back to the driving stage of the first delay line establishes the minimum cycle length. The read/write pulse timing signal is used to clear the flip-flops and allow the start of another cycle.

The circuit provides immediate acknowledgement of a normal cycle request. However, if the request occurs during execution of a refresh cycle, the normal cycle flip-flop goes on and remains on, thereby requesting a normal cycle immediately upon completion of the refresh cycle. In this way refresh cycles are invisible to the memory requestor except for the effective increase in cycle time. A five stage refresh address counter and a 5 bit wide multiplexer must be provided for refresh address generation and switching.

BASIC TIMING GENERATOR FOR S1103 MEMORY - FIGURE 2

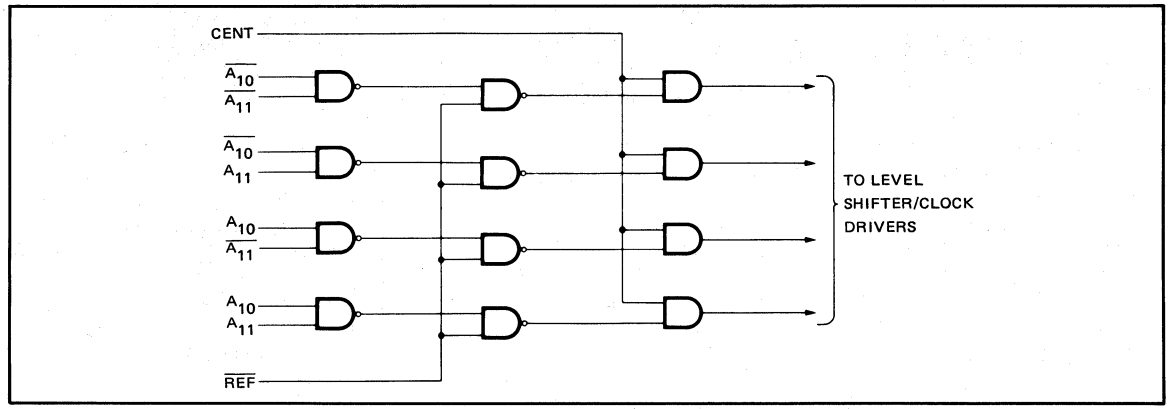


CENABLE DECODE CIRCUITS

Figure 3 shows a suggested circuit for controlling the cenable circuits. Address bits 10 and 11 are decoded by the left-most gates. This decoding is overridden when refresh is true (REF is low). The CENT input supplies timing for the array.

Similar decoders may also be used for decoding precharge and read/write.

CENABLE DECODE CIRCUIT - FIGURE 3



DRIVE AND SENSE CIRCUITS

Figure 4 shows a line receiver used as a sense amplifier with strobing included. The 75108 has an open collector output and hence is ideal for large systems where several modules are tied to a common data bus.

The sense line and the optional dummy line run parallel through the array with only the sense line connected to the device. This organization is used to minimize noise due to capacitative coupling to the sense line. The voltage divider consisting of a 200Ω and an 18K resistor is used to establish the logic 1/logic 0 detection level threshold.

BALANCED LINE SENSING - FIGURE 4

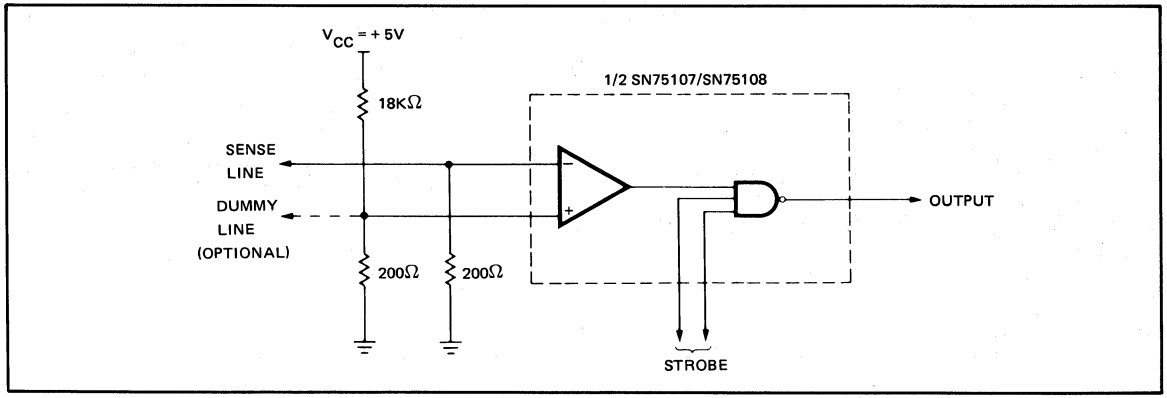
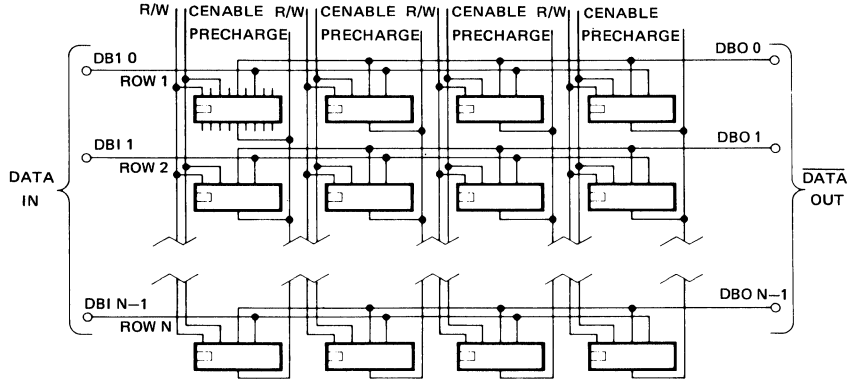


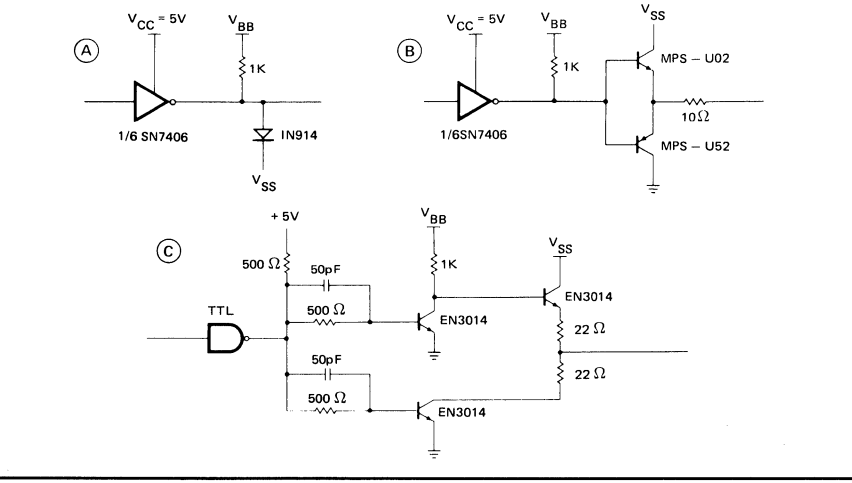
Figure 5 shows how the devices in the memory array are connected. For a 4K x 9 memory, the number of rows N is 9, and the number of columns is 5. In each row, data input leads are connected in common. Similarly, data output leads in each row are connected. In each column, cenable leads are connected. Unless precharge and read/write decoding is used, the remaining terminals are bussed so that corresponding pins of all packages are connected.

The circuits shown in Figure 6 are examples of drivers which can be used when interfacing TTL to S1103 levels. The driver shown in Figure 6A can be used to drive address and data lines. A more rugged driver is shown in Figure 6B and can be used to drive address and data lines in very large arrays. An inexpensive driver for precharge, cenable and read/write is shown in Figure 6C.

S1103 MEMORY EXPANSION - FIGURE 5



TTL TO S1103 INTERFACE CIRCUITS - FIGURE 6



INTERFACE CIRCUITS – TYPICAL OUTPUT CHARACTERISTICS (25°C)

	Driver Ⓐ	Driver Ⓑ	Driver Ⓒ
Low Voltage (V_{OL})			
No Load	0.25V	≈OV	0.04V
Sinking 3 - mA	–	+0.97V	0.14V
High Voltage (V_{OH})			
No load	V_{SS} + 0.65V	V_{SS} ± 0.01V	V_{SS} ± 0.01V
Source - 3 mA	–	V_{SS} – 0.05V	V_{SS} – 0.12V
Sink x 0.5 mA	–	V_{SS} + 0.01(1)	V_{SS} + 0.45(1)
Rise Time (t_R)(2)			
10pF	25 ns	25 ns	10 ns
50pF	90 ns	25 ns	15 ns
100pF	–	25 ns	20 ns
200pF	–	25 ns	25 ns
470pF	–	40 ns	50 ns
Fall Time (t_F)(2)			
10pF	12 ns	6 ns	6 ns
50pF	20 ns	8 ns	9 ns
100pF	–	10 ns	12 ns
200pF	–	14 ns	20 ns
470pF	–	24 ns	35 ns

NOTES:
1. This voltage level is a function of transistor reverse gain. A diode clamp to V_{SS} is recommended.
2. These values are measured between the 10% and 90% points.

The address bits in excess of the first ten are decoded and drive cenable for each column. This decoded cenable signal acts as a column select within the memory array. Block drivers are required for these signals also. The multiplexer permits substitution of the refresh address for the address in the latches during refresh cycles. Only five bits are required. The cenable decoding is also overridden during refresh cycles.

POWER DISSIPATION CONSIDERATIONS

To estimate power consumption of an S1103 memory, three sources of dissipation must be considered:

- **Memory DC Power.** Memory DC power is approximately given by the product of the number of packages selected at one time, times the sum of the power dissipated during each portion of the cycle, added to the power dissipated by the unselected packages. For a 4K x 9 memory with precharge decoding the DC memory power is as follows:

$$9 \text{ Devices} \times \underbrace{[0.056 \times 0.3}_{\text{Precharge } (t_{PC})} + \underbrace{0.059 \times 0.095}_{\text{Overlap } (t_{OVL})} + \underbrace{0.011 \times 0.385}_{\text{Cenable } (t_{POV})} + \underbrace{0.004 \times 0.22]}_{\text{Cenable to Next Precharge } (t_{CP})} \times \underbrace{16.8}_{V_{SS}} + \underbrace{27 \times 0.004 \times 16.8}_{\text{Unselected Devices}} \approx 6.0\text{W}$$

- **Clock Power.** Clock power is associated with current drawn from the power supplies to charge precharge, cenable, read/write, and address line capacitances. The worst case may be found by taking the product of memory frequency times total effective capacitance times the square of the clock drive voltage supply. For decoded precharge, read/write and cenable capacitances times the number of devices driven.

For a 4K x 9 memory with precharge decoding:

C_{eff} = 10 Address Lines x 7 pF x 36 Devices + ~ 60 pF x 9 Devices $\cong$ 3000 pF

Worst case power = $10^6 \times 3000 \times 10^{-12} \times 16.8^2 \cong 1.5\text{W}$

- **Level Shift Power.** Worst case is derived from the total number of level shifters times maximum dissipation per level shifter. For the level shifter shown with 470Ω load resistor and 17V supply, dissipation is approximately 0.6W. The 4K x 9 array required 31 circuits. Worst case power would be about 18.5W.

These power dissipation figures may be higher than actually observed for the following reasons:

- Not all level shifters will operate at maximum dissipation. The four used for precharge will typically dissipate only 40 – 60% of the maximum value. The four used for read/write have very low duty cycles. Address and data level shifters dissipate the maximum values only for certain conditions.

- Capacitive charging dissipation may also be less than the computed values if few address bits change.

- When level shifters are added for precharge decoding, the duty cycle is reduced in proportion to the number of drivers added.

Precharge duty cycle should be a minimum to reduce the power dissipation.

LOW POWER DATA RETENTION

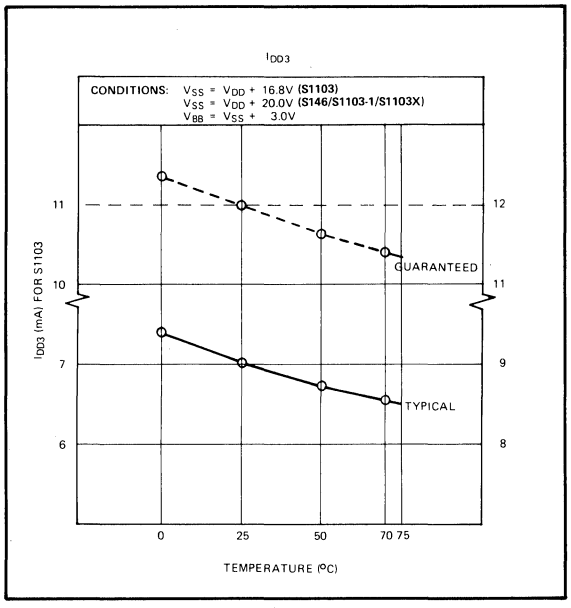
Low power data retention mode is an operating mode for a dynamic MOS memory in which power consumption is reduced to the minimum value possible while still maintaining data in the memory. For most dynamic MOS memories the power consumption level in this mode is in the range of from 1 to 10W per million bits. These low power levels make it possible to maintain the data within the memory with small battery packs. Many of the problems associated with the normal volatility of semiconductor memory systems can be eliminated using this mode of operation.

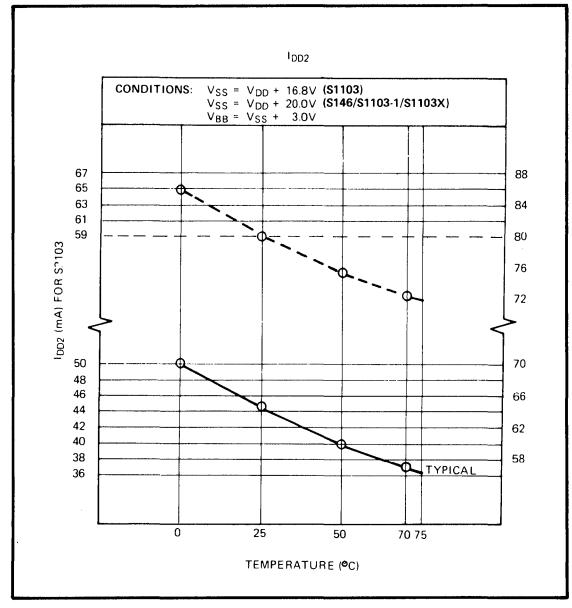
In the low power data retention mode of an S1103, the memory is operated such that only refresh cycles are executed. Power dissipation in the memory array is then reduced to a minimum value. To ensure low power dissipation elsewhere in the memory system, it is usually most desirable to execute the refresh cycles in bursts of 32 every 2 ms, which eliminates the need for retaining information about which locations were refreshed and which were not. The entire memory is refreshed every 2 ms.

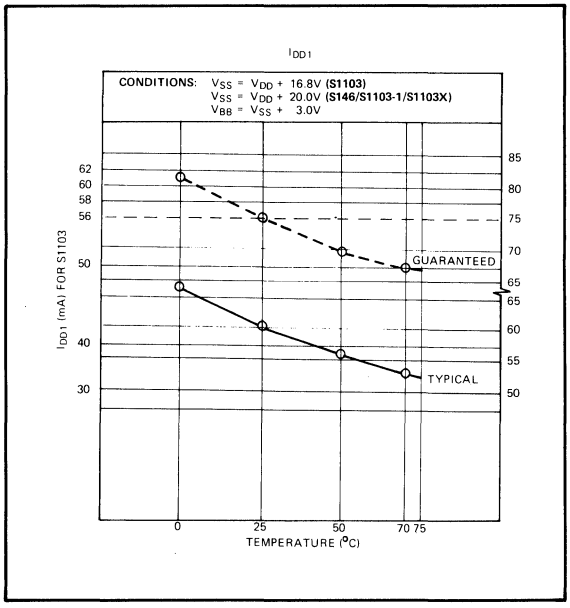
The S1103 has a potential current flow form V_{SS} to V_{DD} during the period between refresh bursts. However, this current can be minimized by ensuring that address line A_4 is low (V_{IL}) during the last cycle of the refresh burst, then returns high (V_{IH}) after the last cycle.

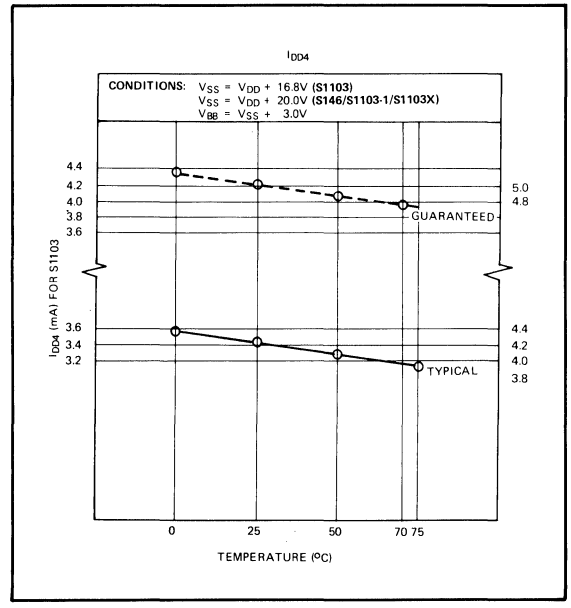
A typical implementation of low power data retention uses a time-out circuit which establishes when 2 ms have elapsed. Power is then switched on to the TTL controller and the memory is forced into burst (i.e., burst of 32 refresh cycles) refresh mode. Upon completion of the burst of refresh cycles, controller power is shut off and the time-out circuit reset. This sequence is repeated until main system power is applied. Then upon completion of the burst of refresh cycles, the memory switches to the normal operating mode. Three power supplies must always be present: V_{BB}, V_{SS} and a supply for use by the TTL logic in the controller. The TTL logic supply is switched on to the control logic only during the execution of refresh bursts or during normal operation. The V_{BB} and V_{SS} supplies must be maintained at the memory array at all times. The memory array draws significant current from the V_{SS} supply only during the execution of memory cycles. To minimize power consumption in the system, level shifters should be designed such that with the V_{SS} supply maintained on the level shifters, and the TTL controller supply off, the level shifter output is at + V_{SS} with no (or insignificant) power drawn from the V_{SS} or V_{BB} supplies.

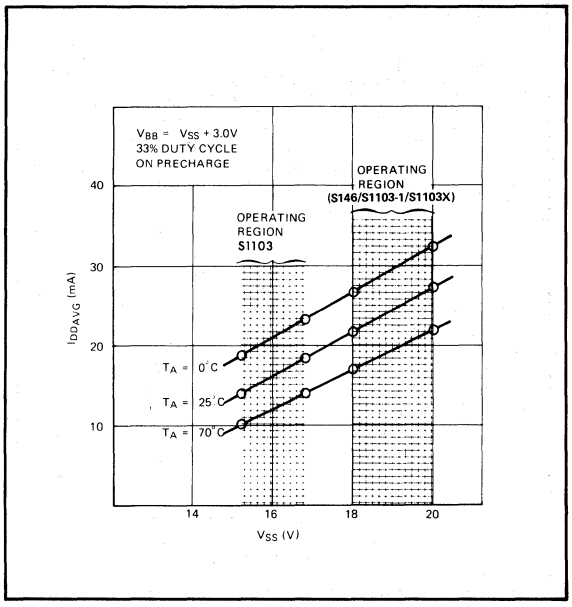
The power supplies for a memory with low power data retention mode are usually backed up by some form of storage battery. For the best results, the batteries are located on the unregulated side of the power supply regulators. During normal operation of the system, the batteries are trickle charged. Whenever the unregulated voltage falls below the battery voltage, the batteries deliver current. The voltages to the memory experience no switching transients, and proper regulation of all memory voltages is maintained.

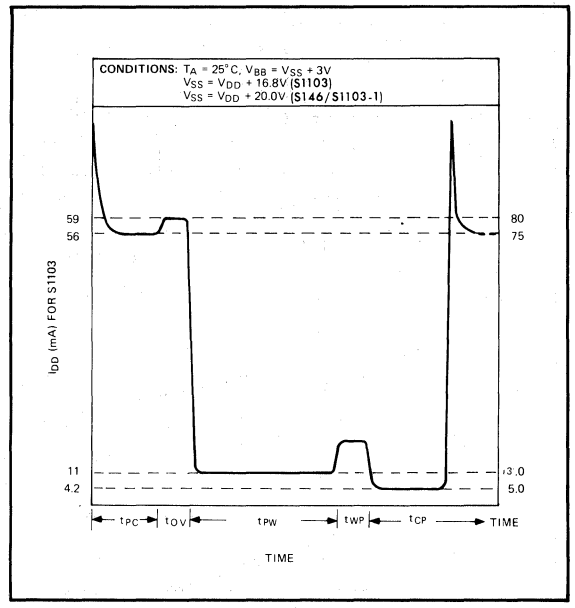

I_{DD3}
CONDITIONS: $V_{SS} = V_{DD} + 16.8V$ (S1103)
$V_{SS} = V_{DD} + 20.0V$ (S146/S1103-1/S1103X)
$V_{BB} = V_{SS} + 3.0V$
I_{DD3} (mA) FOR S1103
11
10
7
6
12
11
9
8
GUARANTEED
TYPICAL
0
25
50
70 75
TEMPERATURE (°C)

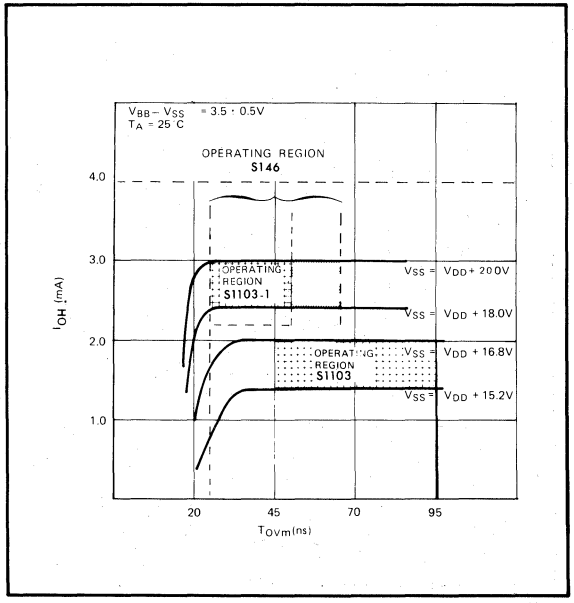

I_{DD2}
CONDITIONS: $V_{SS} = V_{DD} + 16.8V$ (S1103)
$V_{SS} = V_{DD} + 20.0V$ (S146/S1103-1/S1103X)
$V_{BB} = V_{SS} + 3.0V$
I_{DD2} (mA) FOR S1103
67
65
63
61
59
50
48
46
44
42
40
38
36
88
84
80
76
72
70
66
62
58
TYPICAL
0
25
50
70 75
TEMPERATURE (°C)

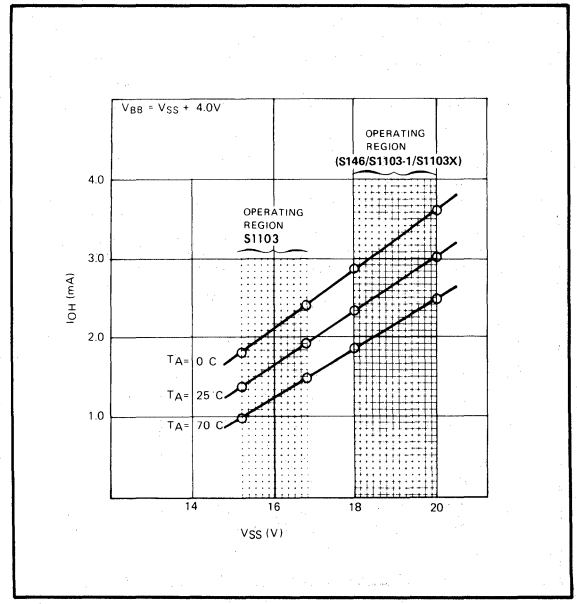

I_{DD1}
CONDITIONS: $V_{SS} = V_{DD} + 16.8V$ (S1103)
$V_{SS} = V_{DD} + 20.0V$ (S146/S1103-1/S1103X)
$V_{BB} = V_{SS} + 3.0V$
I_{DD1} (mA) FOR S1103
62
60
58
56
50
40
30
85
80
75
70
65
65
60
55
50
GUARANTEED
TYPICAL
0
25
50
70 75
TEMPERATURE (°C)


I_{DD4}
CONDITIONS: $V_{SS} = V_{DD} + 16.8V$ (S1103)
$V_{SS} = V_{DD} + 20.0V$ (S146/S1103-1/S1103X)
$V_{BB} = V_{SS} + 3.0V$
I_{DD4} (mA) FOR S1103
4.4
4.2
4.0
3.8
3.6
3.6
3.4
3.2
5.0
4.8
4.4
4.2
4.0
3.8
GUARANTEED
TYPICAL
0
25
50
70 75
TEMPERATURE (°C)


V_{BB} = V_{SS} + 3.0V
33% DUTY CYCLE
ON PRECHARGE
OPERATING REGION (S146/S1103-1/S1103X)
OPERATING REGION S1103
T_A = 0°C
T_A = 25°C
T_A = 70°C
I_{DDAVG} (mA)
V_{SS} (V)


CONDITIONS: T_A = 25°C, V_{BB} = V_{SS} + 3V
V_{SS} = V_{DD} + 16.8V (S1103)
V_{SS} = V_{DD} + 20.0V (S146/S1103-1)
I_{DD} (mA) FOR S1103
TIME


V_{BB} − V_{SS} = 3.5 - 0.5V
T_A = 25°C
OPERATING REGION S146
OPERATING REGION S1103-1
OPERATING REGION S1103
V_{SS} = V_{DD} + 20.0V
V_{SS} = V_{DD} + 18.0V
V_{SS} = V_{DD} + 16.8V
V_{SS} = V_{DD} + 15.2V
I_{OH} (mA)
T_{OVm}(ns)

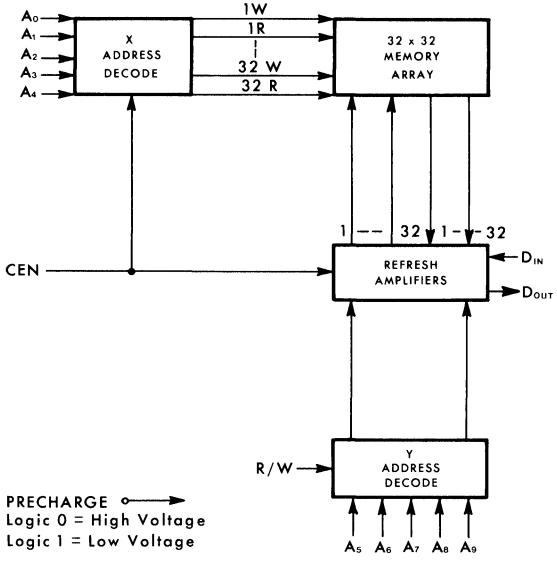

V_{BB} = V_{SS} + 4.0V
OPERATING REGION (S146/S1103-1/S1103X)
OPERATING REGION S1103
T_A = 0°C
T_A = 25°C
T_A = 70°C
I_{OH} (mA)
V_{SS} (V)

AMERICAN MICROSYSTEMS, INC.

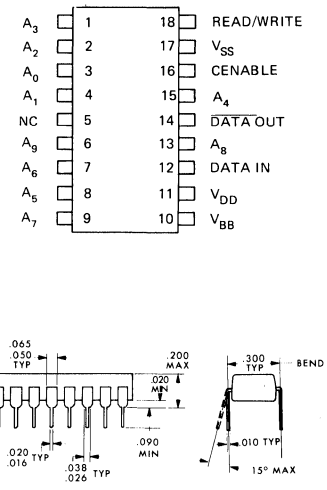
S1103A
S1103A-1
S1103A-2

1024×1 RANDOM ACCESS MEMORY

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2P, 1P - see Sec. 1)

FEATURES

- Fast access time, 205/145/145 ns
- Performance options subject to power supply levels
- Fast cycle time 580/340/400 ns
- No precharge required – critical precharge timing is eliminated
- Low standby power dissipation – 0.2 μW/bit typical
- Address registers incorporated on the chip
- Simple memory expansion – cenable input lead
- Inputs protected against static charge
- Refresh period, 2 ms @ 0 to 70°C

FUNCTIONAL DESCRIPTION

The AMI S1103A family of random access memories are designed for applications where high performance, low cost and large bit storage are desired, such as main memories. It is a 1024 word by 1 bit array fabricated with low threshold, silicon gate technology. This high density process technology allows the design and production of extremely high performance memory devices.

S1103A systems may be simplified due to the elimination of the precharge clock, its associated circuitry, and critical timing. Only one external clock, CENABLE, is required.

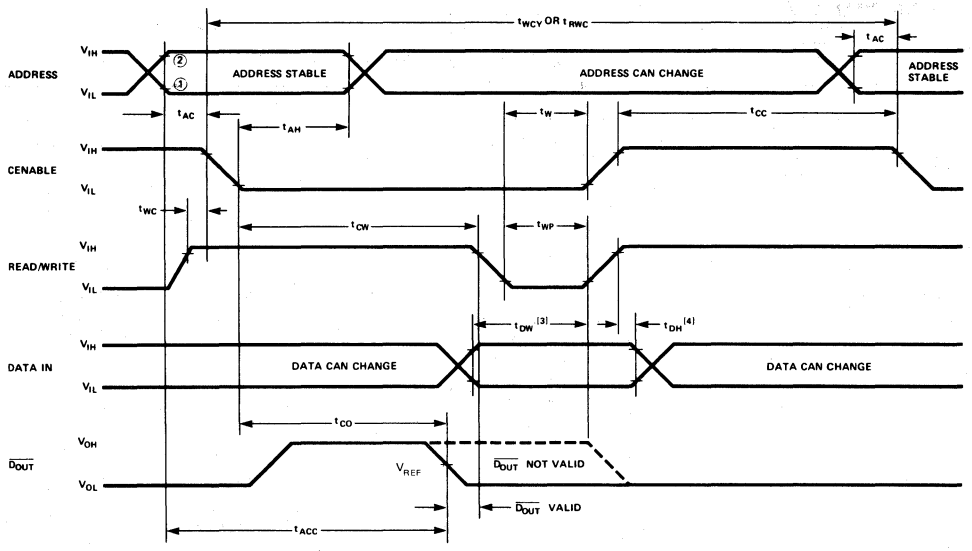
Information stored in the memory is non destructively read. Refreshing of all 1024 bits is accomplished in 32 read cycles (addressing A_0 to A_4) and is required every 2 milliseconds. The memory may be used in a low power standby mode by having cenable at V_{SS} potential.

TYPICAL APPLICATIONS

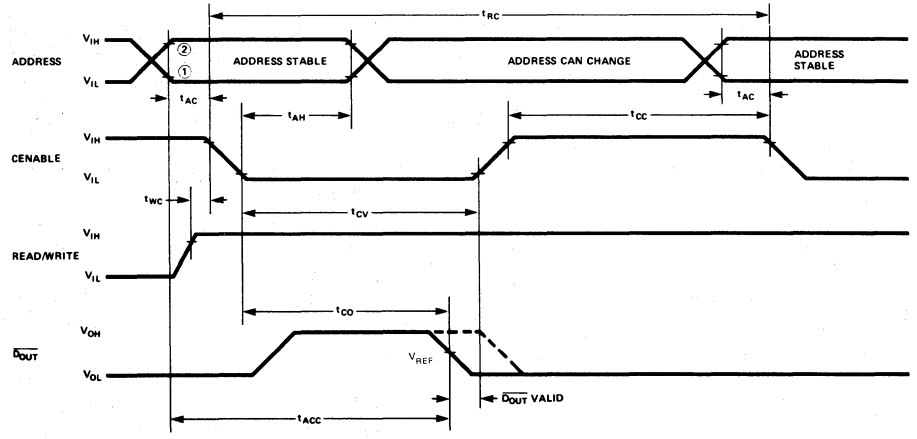
Mainframe Memories, Cache Memories, Buffer Memories, Minicomputer Memories, Mass Memories, Terminals.

WRITE CYCLE OR READ/WRITE CYCLE

Timing illustrated for minimum cycle.



READ CYCLE



NOTES:

1. 90% Point
2. 10% Point

t_T is defined as the transition between these two points

3. t_{DW} is referenced to point 1 of the rising edge of cenable or Read/Write, whichever occurs first.
4. t_{DH} is referenced to point 2 of the rising edge of cenable or Read/Write, whichever occurs first.

OPERATING, AC AND DC CHARACTERISTICS

OPERATING CHARACTERISTICS		S1103A		S1103A – 1		S1103A – 2		UNITS
SYMBOL	TEST DESCRIPTION							
T_A	Ambient Temperature	0 to 70		0 to 55		0 to 55		°C
V_{DD}	Negative Supply	0		0		0		V
V_{SS}	Positive Supply (8)	16 ± 0.8		19 ± 1		19 ± 1		V
$V_{BB} - V_{SS}$	Substrate Supply (9)	3.5 ± 0.5		3.5 ± 0.5		3.5 ± 0.5		V
C_L	Load Capacitance	100		50		50		pF
R_L	Load Resistance (10)	100		100		100		Ω
V_{REF}	Output Reference Voltage	40		80		80		mV
AC CHARACTERISTICS		**S1103A**		**S1103A – 1**		**S1103A – 2**		**UNITS**
		MIN	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
READ, WRITE AND READ/WRITE CYCLE								
t_{REF}	Time between Refresh Cycles		2		1		1	ms
t_{AC}	Address to Chip Enable Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		50		50		ns
t_{CC}	Cenable Off Time	230		120		180		ns
READ CYCLE								
t_{RC} (5)	Read Cycle	480		300		360		ns
t_{CV}	Cenable on time	210	500	140	500	140	500	ns
t_{CO}	Cenable Output Delay		185		125		125	ns
t_{ACC} (6)	Address to Output Access		205		145		145	ns
WRITE OR READ/WRITE CYCLE								
t_{WCY} (7)	Write Cycle	580		340		400		ns
t_{RWC} (7)	Read/Write Cycle	580		340		400		ns
t_{CW}	Cenable to Read/Write Delay	210	500	140	500	140	500	ns
t_{WP}	Read/Write Pulse Width	50		20		20		ns
t_W	Read/Write Setup Time	80		20		20		ns
t_{DW}	Data Setup Time	105		40		40		ns
t_{DH}	Data Hold Time	10		10		10		ns
t_{CO}	Output Delay		185		125		125	ns
t_{WC}	Read/Write to Cenable	0		0		0		

NOTES:

5. $t_{RC} = t_{CV} + t_{CC} + 2\,t_T$
6. $t_{ACC} = t_{AC} + t_{CO} + t_T$
7. $t_{WCY} = t_{RWC} = t_{CW} + t_W + t_{CC} + 3\,t_T$
8. V_{SS} current drain is equal to $(I_{DD} + I_{OH})$ or $(I_{DD} + I_{OL})$
9. $(V_{BB} - V_{SS})$ supply should be applied before V_{SS}.
10. R_L of 100 Ω is chosen for convenience. In application, R_L may range from 100 to 1000 Ω.

AC CHARACTERISTICS (Cont'd)

		PLASTIC TYP	PLASTIC MAX	CERAMIC MAX	UNIT	CONDITIONS
CAPACITANCE (12)						
C_{AD}	Address	5	7	12	pF	$V_{IN} = V_{SS}$
C_{CE}	Chip Enable	22	25	28	pF	$V_{IN} = V_{SS}$
C_{RW}	Read/Write	11	15	20	pF	$V_{IN} = V_{SS}$
C_{IN1}	Data Input	4	5	8	pF	Cenable = 0V, $V_{IN} = V_{SS}$
C_{IN2}	Data Input	2	4	7	pF	Cenable = V_{SS}, $V_{IN} = V_{SS}$
C_{OUT}	Data Output	2	3	7	pF	V_{OUT} = 0V

All Unused Pins @ AC GND; f_0 = 1 MHz; V_{BB} = 3.0V, T_A = 25°C

DC CHARACTERISTICS		S1103A MIN	S1103A MAX	S1103A – 1/–2 MIN	S1103A – 1/–2 MAX	UNIT	CONDITIONS
I_{LI}	Input Leakage Current (All Input Pins)		1		10	μA	V_{IN} = 0V
I_{LO}	Output Leakage Current		1		10	μA	V_{OUT} = 0V
I_{BB}	Substrate Supply Current		100		100	μA	
I_{DD1}	Supply Current During Cenable On		11		11	mA	Cenable = 0V, T_A = 25°C
I_{DD2}	Supply Current During Cenable Off		4		0.5	mA	Cenable = V_{SS}, T_A = 25°C
$I_{DD\ AVG}$	Average Supply Current		25		33	mA	Cycle Time = 580ns, T_A = 25°C
V_{IL}	Input Low Voltage	$V_{DD} - 1$	$V_{DD} + 1$	$V_{DD} - 1$	$V_{DD} + 1$	V	
V_{IH}	Input High Voltage	$V_{SS} - 1$	$V_{SS} + 1$	$V_{SS} - 1$	$V_{SS} + 1$	V	
I_{OH1}	Output High Current	600	4000	1150	7000	μA	T_A = 25°C
I_{OH2}	Output High Current	500	4000	900	7000	μA	T_A = Max Temp
I_{OL}*	Output Low Current	See Note 4		See Note 4			R_L (10) = 100Ω
V_{OH1}	Output High Voltage	60	400	115	700	mV	T_A = 25°C
V_{OH2}	Output High Voltage	50	400	90	700	mV	T_A = Max Temp
V_{OL}	Output Low Voltage	See Note 4		See Note 4			

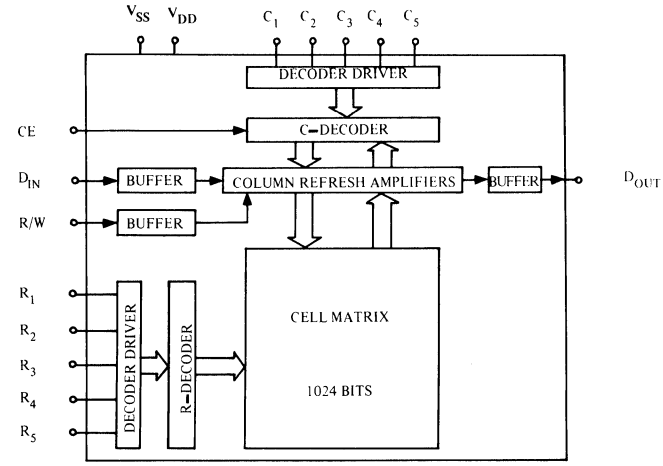
NOTES:

11. I_{OL} = leakage current of the 1103A plus external noise coupled with the output line from the clocks. $V_{OL} = I_{OL}$ across the load resistor.
12. All capacitances are periodically sampled at worst case operating conditions and are not 100% tested.

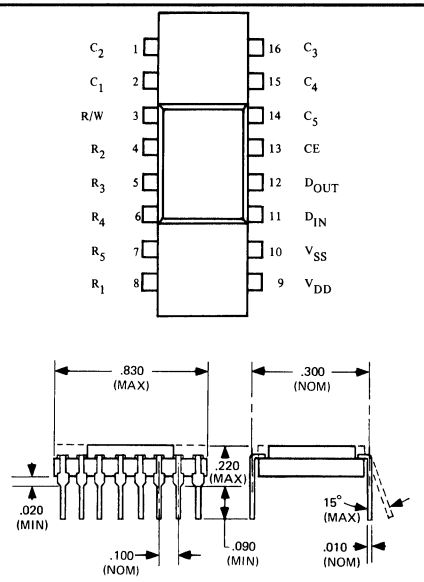
AMERICAN MICROSYSTEMS, INC.

S4006
S4008
S4008-9

1024X1 DYNAMIC
MOS RANDOM ACCESS MEMORY



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkg. 2H, 4H – see Sec. 1)

FEATURES

- Pin Compatible with 2102 Static 1K RAM
- Fast Access Time – 400/500/800 nsec. max.
- No Clocks Required
- Low Standby Power – 50 mw typ.
- Supply Voltage – + 5V and – 12V
- 16 Pin DIP – High Packing Density
- Static Internal Decoding and Sensing
- TTL Compatible Inputs
- Pin-for-Pin Replacement – Mostek's MK4006 Family

FUNCTIONAL DESCRIPTION

The S4006, S4008 and S4008-9 are a family of MOS dynamic 1024 x 1 random access memories designed to meet a wide variety of memory applications where performance, low cost, large bit storage, and simple interfacing are important design objectives. These memories are fully decoded internally. Information is read out nondestructively (NDRO) and has the same polarity as the input data.

All inputs are TTL compatible allowing the design of both small and large main-memory systems economically. No special interface circuitry is needed. The standard 16 pin dual-in-line package and low standby power dissipation make the S4006 family desirable for applications where packing density and low power consumption are critical.

Periodically the capacitor storage elements must be refreshed by cycling through all 32 Row addresses ($R_1 - R_5$) (TIMING CHARACTERISTICS). Since no other clocking is necessary, the S4006 family can be treated like a static RAM except during the refresh cycle. In use, all memory controlling, addressing and sensing functions are static. These devices produce negligible power supply current transients, therefore, standard TTL noise suppression techniques are sufficient. With input capacitances of less than 10 pF coupled with low input voltage swings, the need for high peak current driving circuitry is totally eliminated.

FUNCTIONAL DESCRIPTION (Con't.)

The memory provides a data output that is single-ended to minimize interface circuitry and simplify memory expansion. Output current is sourced from V_{SS} (+5V), and readily sensed by using available components. A low logic level output appears as an open circuit and a high logic level source current through a 5000 Ohm resistor to +5V.

Ion-implantation processing assures the performance of these devices. The AMI I^{2} TM process makes possible the low threshold voltages and in combination with P-channel metal gate processing allows both enhancement (normally OFF) and depletion (normally ON) MOS transistors to be combined on the same chip. By replacing conventional MOS load resistors with near constant current depletion load transistors, an I^2 memory can have faster access times, higher density and lower power dissipation than competitive non-I^2 memory devices.

TYPICAL APPLICATIONS

- 2102 Replacement at a Lower Cost
- Video Terminal Refresh Memories
- Peripheral Equipment Memory Storage
- Programmable Calculator Memories
- Data Entry Systems
- Buffer Memory

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} . . . . . + 0.3 to – 20V
Operating Temperature . . . . . 0°C to + 70°C
Storage Temperature . . . . . – 55°C to + 150°C

D. C. OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = + 5V ± 5%, V_{DD} = – 12V ± 5%

SYMBOL	PARAMETER	S4006 MIN	S4006 MAX	S4008 MIN	S4008 MAX	S4008-9 MIN	S4008-9 MAX	UNITS	TEST CONDITIONS
I_{SS} & I_{DD}	Supply Current At T_A = 0°C At T_A = 70°C		32 27		32 27		32 27	mA mA	Output Open
P_{SDBY}	Standby Power		50		50		—	mW	V_{DD} = + 0.95V Note 1
I_{IH}	Input Current, HIGH Level Any Input	–5	+5	–5	+5	–5	+5	μA	$V_{IN} = V_{SS} - 1.5V$
I_{IL}	Input Current LOW Level Any Input	–5	+5	–5	+5	–5	+5	μA	V_{IN} = 0.8V
I_{OH}	Output Current, HIGH Level	1.0		0.8		0.6		mA	Note 2
I_{OL}	Output Current, LOW Level		5		5		5	μA	Note 2
V_{IL}	Input Voltage LOW Level		+0.8		+0.8		+0.8	V	
V_{IH}	Input Voltage HIGH Level	V_{SS}-1.5		V_{SS}-1.5		V_{SS}-1.5		V	

A. C. OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{SS} = + 5V ± 5%, V_{DD} = −12V ± 5%

SYMBOL	PARAMETER	S4006 Min	S4006 Max	S4008 Min	S4008 Max	S4008-9 Min	S4008-9 Max	UNITS	TEST CONDITIONS
t_{ACC}	Access Time		400		500		800	ns	Note 4 and Figure 6
t_{RC}	Read Cycle Time	400		500		800		ns	
t_{WC}	Write Cycle Time	650		900		1000		ns	
t_{WP}	Write Pulse Width	250		400		450		ns	
t_{AW}	Address to Write Delay	400		500		550		ns	
t_{DLD}	Data to Write Set-Up Time	300		400		500		ns	
t_{DH}	Data to Write Hold Time	0		0		0		ns	
t_{RDLY}	Refresh Time		2		2		1	ms	Note 3
t_{CDPD}	Chip – Disable – to – Power–Down Delay	200		200				ns	
t_{CE}	Chip Enable Time		350		450		750	ns	Note 4
t_{CD}	Chip Disable Time		350		450		750	ns	
C_{IN}	Input Capacitance		5		5		5	pF	T_A = 25°C V_{IN} = V_{SS}
C_{OUT}	Output Capacitance		10		10		10	pF	T_A = 25° C V_{OUT} = V_{SS} − 5V
C_{DD}	V_{DD} Capacitance		75		75		75	pF	T_A = 25°C GND To −12V

NOTES:

(1) Applies to S4006L and S4008L only

(2) Steady state values with R_L = 200 Ω

(3) t_{RDLY} is the time between refresh cycles for a given row address

(4) See the access time measurement

TIMING CHARACTERISTICS

READ OPERATION

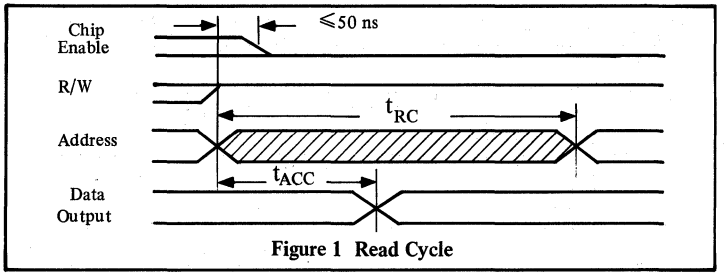


Figure 1 Read Cycle

With the Read/Write input HIGH and Chip Enable input LOW, the stored logic level appears at the output directly following the application of an address. The output data will remain valid until the next refresh operation. As soon as the output data is valid, the address can be changed. If periodically the memory is completely refreshed, any address can be applied repetitively without degrading the stored data.

WRITE OPERATION

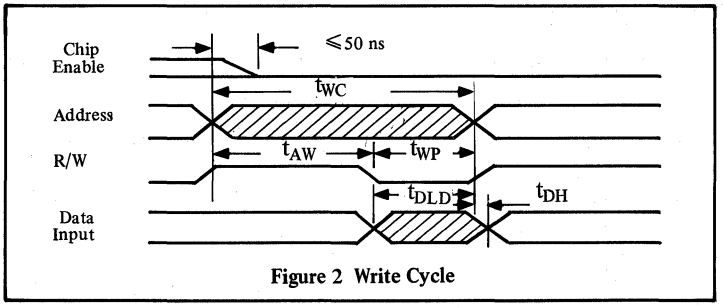


Figure 2 Write Cycle

With the Read/Write input LOW and the Chip Enable input LOW, data present at the data input will be stored in the addressed bit location. New addresses and data can be written following the return of the Read/Write input to a HIGH level. Valid data will appear at the data output within one read access time interval following the rising edge of the write pulse, if a read after write operation is desired. A read-modify-write operation is performed by delaying the write pulse until the address bit location has been read.

REFRESH OPERATION

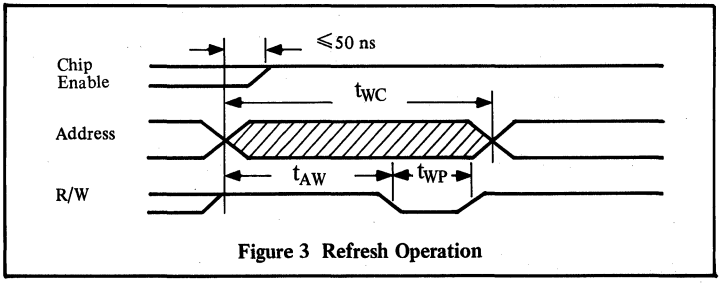


Figure 3 Refresh Operation

The capacitive storage cells of the S4006 family will not store data indefinitely. Periodically (see Refresh Time specification) the stored data must be written back into each storage cell. This refresh operation is done during both the Write and Refresh cycles. If all 32 Row addresses (R1 – R5) are continually addressed during normal write operations in less than the Refresh Time requirement, no refresh operation is necessary. However, if this normal write operation refresh does not occur, a separate refresh operation is also available.

The refresh and write operations are identical except that the Chip Enable is held HIGH disabling the chip while pulsing the Read/Write input and cycling through the 32 Row address.

Disabling the chip removes data from the output and prevents data at the data input from being written into the memory. The total time to entirely refresh the memory is 32 times the Write Cycle Time. This is 32μsec for the 4008–9.

TIMING CHARACTERISTICS (CONT.)

STANDBY MODE

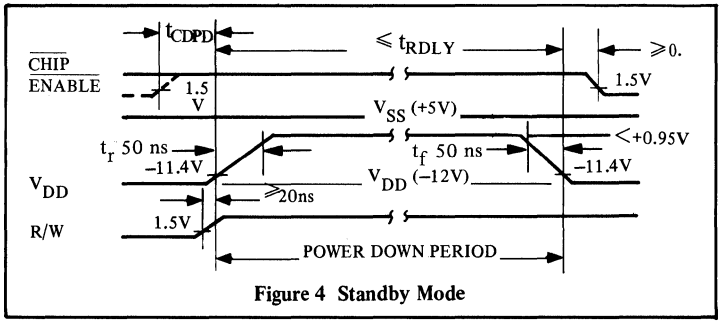


Figure 4 Standby Mode

By lowering the V_{DD} supply voltage to system ground (V_{SS} −5V), power dissipation can be reduced to about 50 mW without loss of stored data. The V_{DD} supply should be returned to −12V and a refresh operation initiated, if the standby mode is maintained as long as 2 ms. Following the return of V_{DD} to − 12V, read or write operations may commence. t_{ACC} and t_{AW} for the first bit after power up are 100 nsec longer than in normal operation. Add "L" to the model number when ordering this feature, i.e., S4006L, S4008L. Option not available in the S4008-9.

CHIP ENABLE

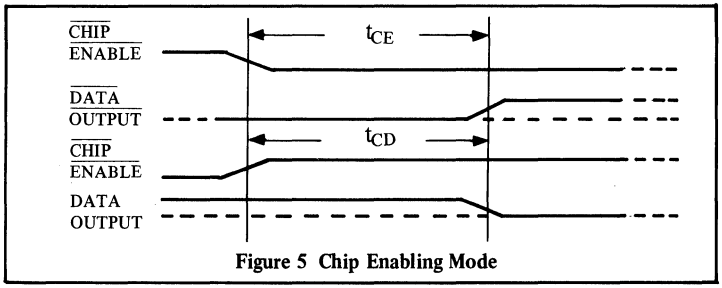


Figure 5 Chip Enabling Mode

A LOW logic level on the $\overline{CE}$ enables the chip. Output data becomes valid within t_{CE} time. Return of the $\overline{CE}$ input to logic HIGH disables the chip; data remains for t_{CD} time.

ACCESS TIME MEASUREMENT

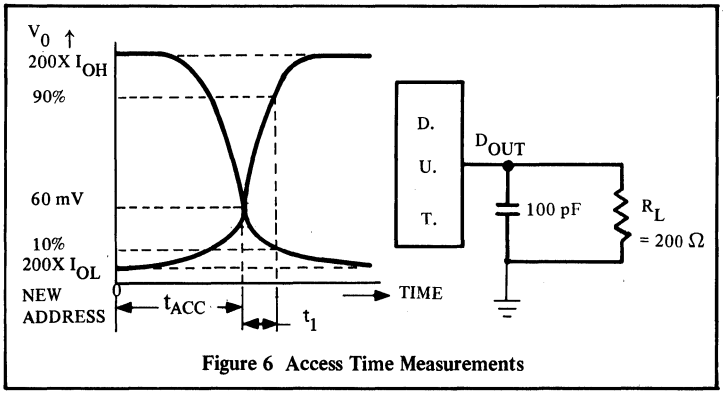


Figure 6 Access Time Measurements

(1) All Inputs −0.8V to V_{SS} − 1.

(2) $t_r = t_f \leqslant 20$ns

(3) All times are referenced to the 1.5V level at inputs and the 60 MV level at outputs

(4) t_1 = 200 ns

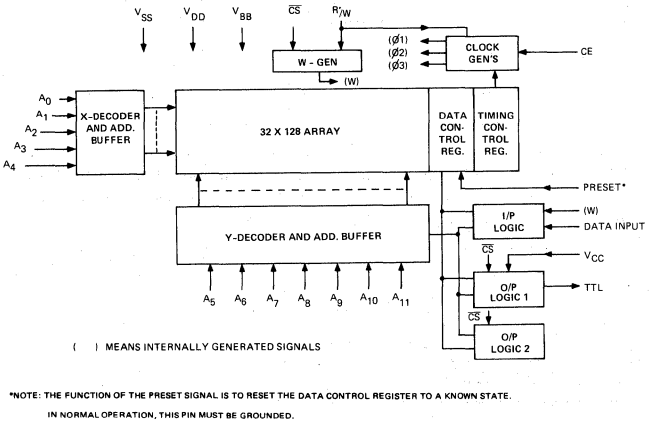
Figure 6 – Illustrates the measurement of access time after application of new address.

S6605
S6605A
S6605B

4096X1 RANDOM ACCESS MEMORY

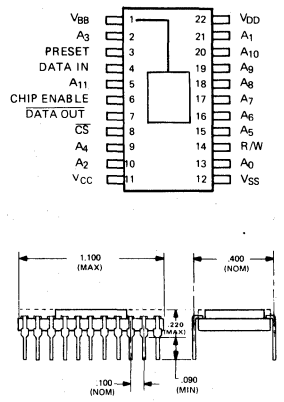
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



*NOTE: THE FUNCTION OF THE PRESET SIGNAL IS TO RESET THE DATA CONTROL REGISTER TO A KNOWN STATE. IN NORMAL OPERATION, THIS PIN MUST BE GROUNDED.

BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2C, 1C - see Sec. 1)

FEATURES

- Fast Access Time 210 – 300 – 600 ns
- Fast Read Cycle Time 370 – 470 – 900 ns
- Fast Read/Write Cycle Time – 490 – 590 – 1100 ns
- Low Power Dissipation
  - Active 335 mW Typ.
  - Standby with Refresh 4 mW Typ.
- Output – 3 State TTL
- Easy Refresh – Only 32 Cycles every 2.0 ms
- Address and data input latches on Chip
- TTL compatible Inputs except Chip Enable Clock
- Simple Memory Expansion – Chip Select
- 22 Pin Dual In-Line Package

FUNCTIONAL DESCRIPTION

The AMI S6605 series of dynamic read/write memories are designed for applications where high performance, low cost and large bit storage are desired in mainframe, add-on, and buffer memories and peripheral storage. The S6605 is a 4096 word by 1 bit array fabricated with selective oxidation N-Channel silicon gate technology. All decoding is done on the chip using ratioless techniques.

All addresses and control inputs are TTL/DTL compatible except for a single high voltage chip enable (CE) clock. The single + 12 volt CE clock lowers system cost. Low voltage swings result in a system with low noise and easy interface.

For standard interface, the S6605 provides a three state TTL output. The information read-out is nondestructive (NDRO). Refresh of the entire memory is accomplished by sequentially cycling each of the 32 row addresses (A_0 - A_4) every 2 ms.

TYPICAL APPLICATIONS

- Main Frame Memory
- Buffer Memory
- Add-on Memory
- Peripheral Storage
- Terminals, etc.

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to substrate:	- 0.3V to + 20V	Operating Temperature Range:	0°C to + 70°C
		Storage Temperature:	- 65° to + 150°C

COMMENT:

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D. C. AND OPERATING CHARACTERISTICS

T_A = 0° to 70°C, V_{DD} = + 12V ± 5%, V_{CC} = +5V ± 10%
V_{BB} = – 5V ± 5%, V_{SS} = 0V, unless otherwise noted.

SYMBOL	PARAMETERS	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	TEST CONDITIONS
V_{CEH}	Chip Enable, CE, High Level	V_{DD} - 1		V_{DD} + 1	V	
V_{CEL}	Chip Enable, CE, Low Level	- 1.0		0.8	V	
V_{IH}*	Addresses, $\overline{CS}$, R/W, Data Input and Preset High Levels	3.0		V_{DD} + 1.0	V	@ t_t = 20 ns
V_{IL}	Addresses, $\overline{CS}$, R/W, Data Input and Preset Low Levels	- 1.0		0.8	V	
V_{OH}	Output High Level	2.4		V_{CC}	V	At 100 μA Current Sourcing
V_{OL}	Output Low Level	V_{SS}		0.45	V	At 2.0 mA Current Sinking
I_L	Input to Substrate Leakage Current (All inputs except CE)		.01	10	μA	V_{IN} = 0V to V_{DD} + 1 Volt V_{DD} = 12.6 with respect to V_{SS}
I_{CEL}	CE Leakage Current		.01	20	μA	CE = V_{CEH}
I_{OL}	Output to Substrate Leakage Current		.01	10	μA	$\overline{CS}$ = V_{IH} V_{OUT} = 0.45V to V_{CC}
I_{DDL}	Leakage Current V_{DD} to V_{SS}, Inactive Mode		1	50	μA	CE = V_{CEL}

D. C. AND OPERATING CHARACTERISTICS (Cont'd)

SYMBOL	PARAMETERS	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	TEST CONDITIONS
I_{CCA}	Average V_{SS} current when $\overline{CS}$ is Low, Active Mode		0.1	1.0	mA	T_{CYC} = Min. R/W Cycle
I_{DDA}	Average V_{DD} to V_{SS} Current, Active Mode		28	36	mA	
I_{BBA}	V_{BB} Supply Current, Active Mode		1.0	100	μA	
I_{DDS}	V_{DD} Supply Current Flow to V_{SS} when CE is Low, Standby Mode with Refresh		1.0	500	μA	CE = V_{CEL}, $\overline{CS}$ = V_{IH}
I_{CCS}	V_{CC} to V_{SS} Current when either CE is Low or $\overline{CS}$ is High		.01	10	μA	
I_{BBS}	V_{BB} Supply Current, Standby Mode with Refresh		1.0	20	μA	

*NOTE: For S6605B V_{IH} = 3.5 MIN.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted.)

OPERATING MODES

MODE	CONTROL STATES R/W	CONTROL STATES $\overline{CS}$	OUTPUT
Active (CE = High)			
Read Only	H	L	Valid
Read/Write	H→L	L	Valid
Write Only	L	L	Valid
Read Refresh	H→L	L→H	Valid →Floating
Refresh Only	L	H	Floating
Chip Disabled (Unselected)	H	H	Floating
Standby (CE = Low)	X	X	Floating

X = Don't Care

AC AND OPERATING CHARACTERISTICS

$T_A = 0°$ to 70°C, $V_{DD} = +12V \pm 5\%$, $V_{CC} = 5V \pm 10\%$
$V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$, $V_{CEH} = V_{DD} \pm 1V$

SYMBOL	PARAMETERS		TTL OUTPUT VERSION DEVICES S6605	S6605A	S6605B	UNITS
T_{ACC}	ACCESS TIME		210	300	600	nsec
T_{CYCLE}	CYCLE TIMES	READ ONLY CYCLE	370	470	900	nsec
		READ/WRITE CYCLE	490	590	1100	nsec
		WRITE OR REFRESH CYCLE	490	590	1100	nsec
		READ REFRESH CYCLE	530	670	1200	nsec
T_{CE}	CHIP ENABLE PULSE WIDTH	READ ONLY CYCLE	210	310	610	nsec
		READ WRITE CYCLE	330	430	810	nsec
		WRITE OR REFRESH CYCLE	330	430	810	nsec
		READ REFRESH CYCLE	370	510	910	nsec
T_{CO}	CHIP ENABLE TO OUTPUT TIME		190	280	580	nsec
T_W	WRITE PULSE WIDTH		160	210	300	nsec
T_{SB}	CHIP ENABLE OFF TIME		120	120	250	nsec

NOTE: The numbers shown for Access Times are Maximum Values.
The numbers shown for Cycle Times, T_{CE}, T_{CO}, T_W and T_{SB} are Minimum values.
All timings with $t_T = 20$ nsec
Output Load = 1 TTL Gate and 50 pF (effective).

TABLE 2

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{AS}	Address Set Up Time	0	–	nsec
t_{AH}	Address Hold Time	60	–	nsec
t_T	CE Pulse Transition Time	20	100	nsec
t_{CSD}	Chip Select ($\overline{CS}$) Delay Time	–	70	nsec
t_{CSH}	$\overline{CS}$ Hold Time	0	–	nsec
t_{RWD}	Read Write (R/W) Delay Time	–	70	nsec
t_{RWH}	R/W Hold Time	0	–	nsec
t_{RWR}	R/W Release Time	Min t_{CE}	2000	nsec
t_{DS}	Data Set-Up Time	0	–	nsec
t_{DH}	Data Hold Time	0		nsec
t_{WD}	$\overline{CS}$ to Write Pulse Delay	0		nsec
t_{REF}	Time Between Refresh	–	2	msec
t_{RC}	R/W to Chip Enable Delay	0		nsec

CAPACITANCE

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance (A_n, D_{IN}, R/W, CS)	–	4.0	5.0	pF	Measured at $V_{BB} = -5V$
C_{CE}	Chip Enable Capacitance	–	25	30	pF	Note: These parmeters are periodically sampled and are not 100% tested. They are measured at worst case operating conditions.
C_{OUT}	Output Capacitance	–	4.0	5.0	pF	

OPERATION

Device operation can be understood by referring to logic diagram of Figure 1. The device has an internal timing generator which produces three pulses: $\phi 1$, $\phi 2$, and $\phi 3$. Pulse $\phi 1$ is for preconditioning the internal nodes; pulse $\phi 2$ is for reading data, and pulse $\phi 3$ initiates the refresh activity. Under the supervision of control signals $\overline{CS}$, and Read/Write, $\phi 3$ also triggers a write pulse (W) which enables the write operation.

The S6605 series of dynamic random access memories use the three-transistor memory cell. When chip enable (CE) is low, all dynamic nodes and bit lines (columns) are preconditioned. Input addresses must be stable before CE goes positive. At the positive going edge of CE, the addresses are sampled, and internally controlled delay is initiated. At the end of this delay, the selected address decoders are set up, and a read pulse is generated. The X-decoders select one of 32 rows, and the Y-decoders select one of 128 columns. If a "one" is stored in the memory cell, the associated bit line is discharged to a "Zero"; if a "Zero" is stored, the associated bit line remains charged at a "One". The stored information is therefore transferred from the cell to the bit line in inverted form, and will be sensed by the output buffer. When a write pulse occurs, the storage cell of the selected cell is forced to take the bit line voltage established by the input buffer. The state of the other bit lines are transferred to storage nodes of the selected row. Thus, the stored data is refreshed in inverted form. Thirty two control cells provide information as to whether the row is in non-inverted or inverted form.

A pin PRESET is provided for initialization of the control cells to a logic zero. One 200 nsec, 12V pulse will set all 32 cells to a logic zero. In system use, this good logic level will come naturally after the first few refresh cycles. For a system diagnosis Preset input signal provides a known state for the storage node. For normal operation, however, this pin must be held at a logic zero level.

The write pulse can be disabled by the read-write control (R/W) making the read-only cycle possible. The availability of the read-only cycle possible. The availability of the read-only cycle can improve system speed, because it requires a shorter cycle time.

The TTL output version provides data comparison and a three state output buffer on chip. Signals from both the data control cell and the selected memory cell are compared and provide correct data to the output buffer. The output is disabled (floating) when either CE is low or $\overline{CS}$ is high. Output data is inverted with respect to data input.

When CE is low, power dissipation of the device is minimized. In this condition, the device is said to be in standby mode. However standby mode cannot be maintained more than 2 ms; CE must be returned high for a refresh operation.

OPERATION MODES AND INTERNAL CIRCUIT ACTIVITIES

(Full Operating Voltage and Temperature Unless Otherwise Noted)

	MODE CONTROL SIGNAL		INTERNAL CIRCUIT ACTIVITIES
	@ $\phi 2$ – TIME	@ $\phi 3$ – TIME	
Read-Only	$\overline{CS}$ = '0' R/W: Don't Care	$\overline{CS}$ = '0' R/W = '1'	OUTPUT BUFFER ACTIVE. $\phi 3$ Inhibited.
Read-Refresh	$\overline{CS}$ = '0' R/W: Don't Care	$\overline{CS}$ = '1' R/W = '0'	OUTPUT VALID @ $\phi 2$-time. OUTPUT FLOAT @ $\phi 3$-time. $\phi 3$ exists. W inhibited.
Read-Modify-Write	$\overline{CS}$ = '0' R/W: Don't Care	$\overline{CS}$ = '0' R/W = '0'	OUTPUT VALID at $\phi 2$ and $\phi 3$-times. $\phi 3$ exists. W exists.
Write-Only	$\overline{CS}$ = '1' R/W: Don't Care	$\overline{CS}$ = '0' R/W = '0'	
Refresh-Only	$\overline{CS}$ = '1' R/W: Don't Care	$\overline{CS}$ = '1' R/W = '0'	OUTPUT FLOATS at $\phi 2$ and $\phi 3$ times. $\phi 3$ exists. W. inhibited.

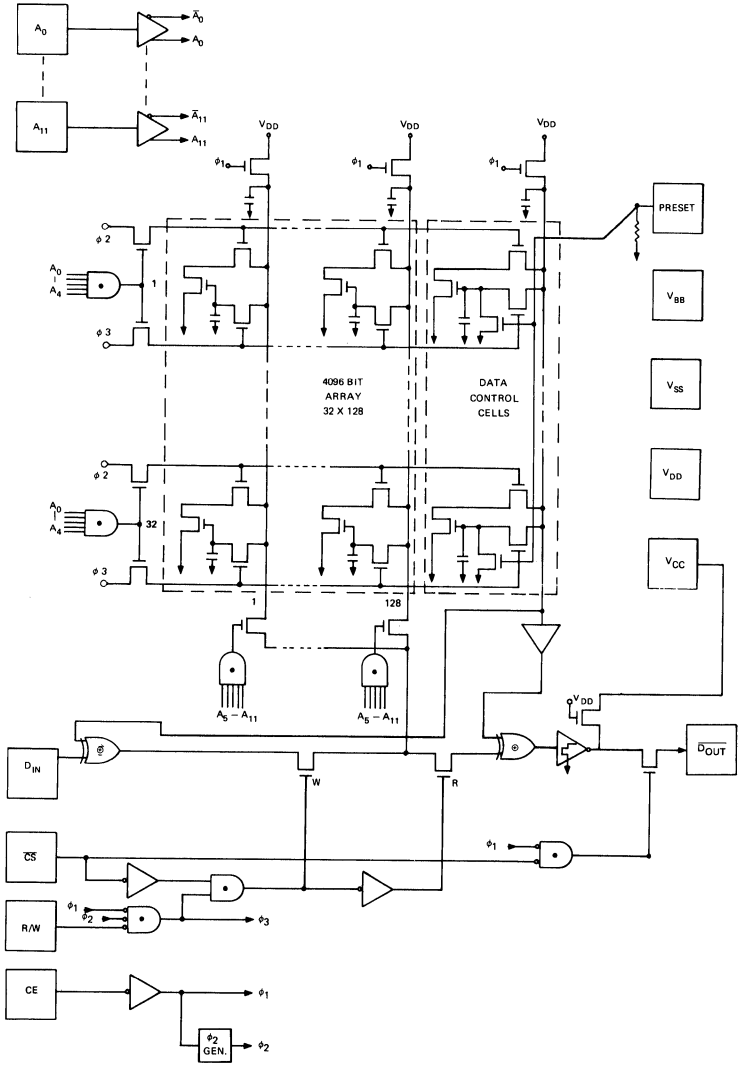
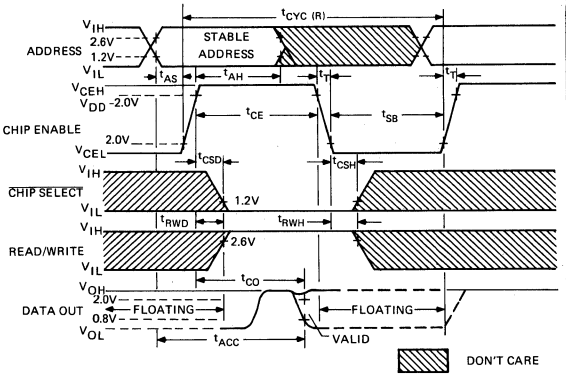
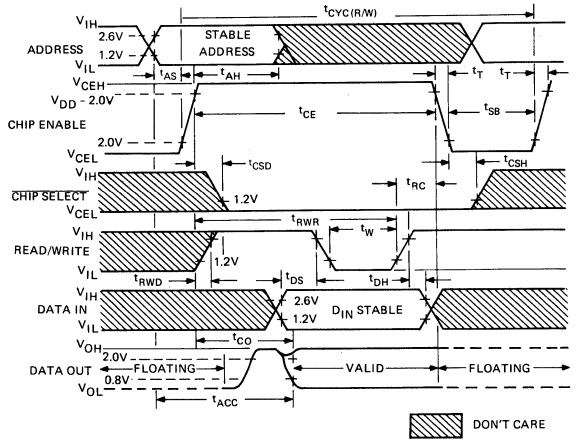


FIGURE 1 – LOGIC DIAGRAM OF 4096-BIT RAM

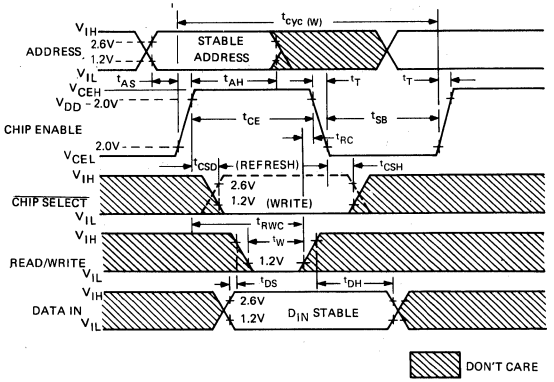
READ ONLY CYCLE TIMING



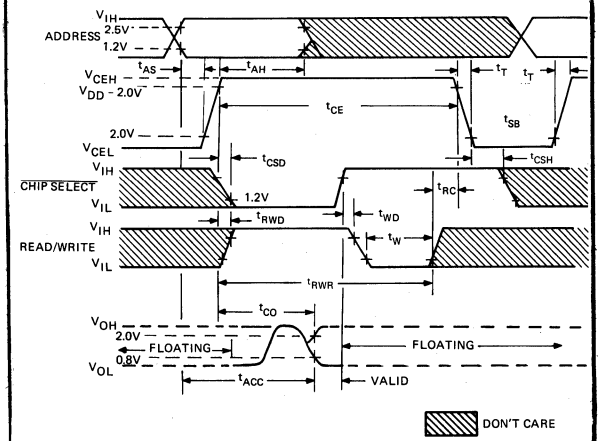
READ/WRITE CYCLE TIMING

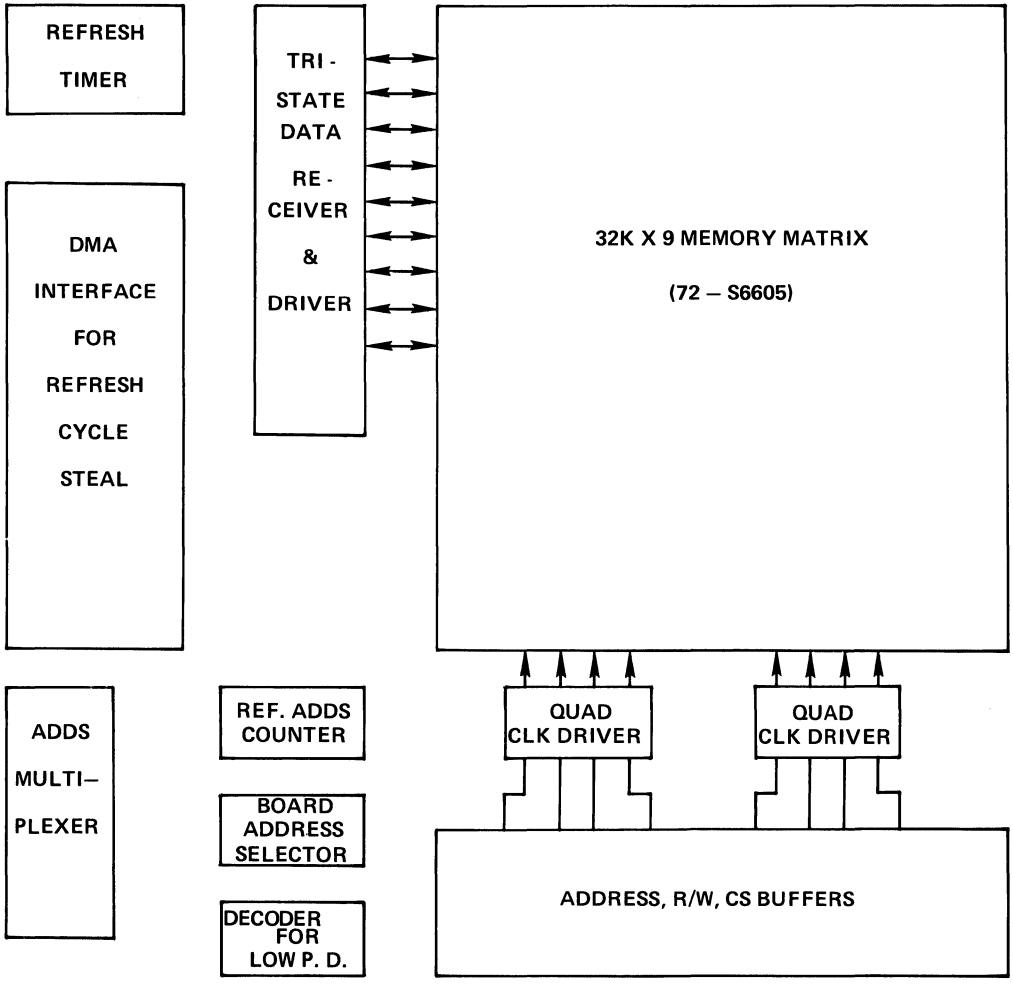


WRITE OR REFRESH CYCLE TIMING



READ REFRESH CYCLE TIMING





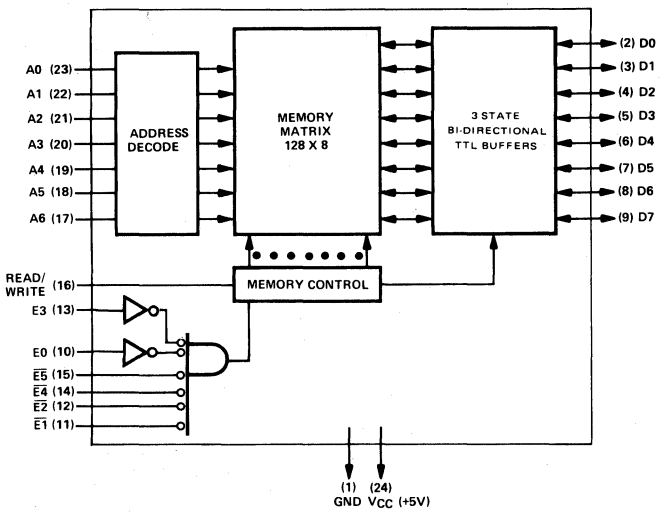
BLOCK DIAGRAM OF 32 × 9 MEMORY BOARD

S6810

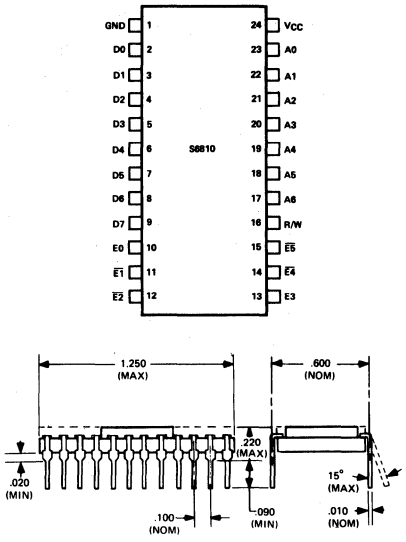
128 X 8 STATIC
READ/WRITE MEMORY

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W - see Sec. 1)

FEATURES

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Enable Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 1.0μs for S6810
  575 ns for S6810-1

FUNCTIONAL DESCRIPTION

The S6810 is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Microprocessor. Interfacing to the S6810 consists of an 8 Bit Bi-directional Data Bus, Seven Address Lines, a single Read/Write Control line, and six Chip Enable lines, four negative and two positive.

For ease of use, the S6810 is a totally static memory requiring no clocks or cell refresh. The S6810 is fabricated with N channel silicon gate technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

For a Complete Data Sheet See Page 6-34

5

Read Only Memories

Future Products

ROM – 2048 x 8 bit Static, 5V N-Channel,
TTL Compatible

ROM – 4096 x 4, 5V N-Channel,
TTL Compatible

PROM – 512 x 8 bit Erasable PROM

Selection Guide-ROMs

Part No.	Description	Organization	Max. Power Dissip. (mW)	Supplies (V)	Max. Access Time	Process	Package	See Page
S3514	4096 Bit Static ROM	512 x 8	500	+5, -12	1 μs	P-I^2	2L,1W	5-4
S5232	4096 Bit Static ROM	512 x 8 or 1024 x 4	500	+5, -12	1 μs	P-I^2	2L,1W	5-4
S8564	9 x 7 Charac. Gen./ROM	64 Word	1100	+5, -12	450 ns	P-I^2	2I,1Z	*
S8771	5120 Bit ROM	512 x 10	1000	+5, -12	450 ns	P-I^2	2I,1Z	*
S8773	2560 Bit ROM	256 x 10	625	+5, -12	450 ns	P-I^2	2I,1Z	*
S8865	8192 Bit ROM	2048 x 4	635	+5, -12	1.3 μs	P-I^2	2L,1W(24) 2I,1Z(28)	*
S8996	16,384 Bit ROM	4096 x 4	368	+5, -12	1.8 μs	P-I^2	2L,1W(24) 2I,1Z(28)	5-10
S9996	16,384 Bit ROM	2048 x 8	368	+5, -12	1.8 μs	P-I^2	2L,1W(24) 2I,1Z(28)	5-10
S6830	8192 Bit Static ROM	1024 x 8	683	+5	575 ns	N-SiGate	2L,1W	5-14
Character Generators								
S8564A	9 x 7 Horizontal Scan ASCII	64 Word	1100	+5, -12	450 ns	P-I^2	2I,1Z	*
S8564B	9 x 7 Horizontal Scan Katakana Alphabet	64 Word	1100	+5, -12	450 ns	P-I^2	2I,1Z	*
S8771D	9 x 7 Vertical Scan ASCII	64 Word	1100	+5, -12	450 ns	P-I^2	2I,1Z	*
S8773B	7 x 5 Horizontal Scan ASCII	64 Word	625	+5, -12	450 ns	P-I^2	2I,1Z	*
ROM Code Converters								
S8771A	Sine/Cosine Lookup Table	512 x 10	1100	+5, -12	450 ns	P-I^2	2I,1Z	*
S8771B	Arc Tangent Lookup Table	512 x 10	1100	+5, -12	450 ns	P-I^2	2I,1Z	*
S8771C	Sine/Cosine Lookup Table	512 x 8	1100	+5, -12	450 ns	P-I^2	2I,1Z	*
S8773A	Sine/Cosine Lookup Table	256 x 10	625	+5, -12	450 ns	P-I^2	2I,1Z	*

***Contact your nearest AMI Sales Office for additional data sheet information on this product (See Section 1)**

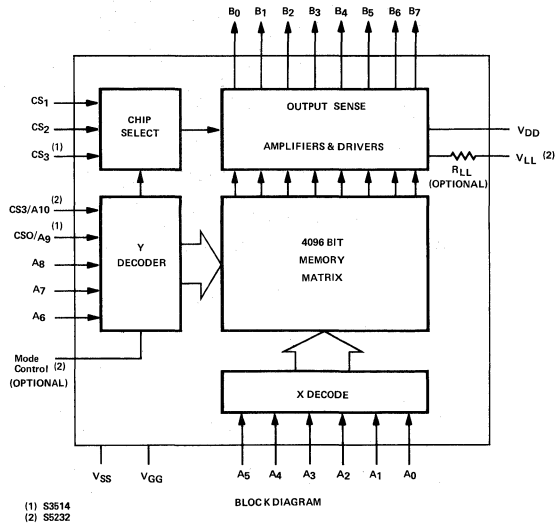
Notes: (1) All ROMs are mask-programmable for custom patterns to meet customer requirements.

S3514
S5232

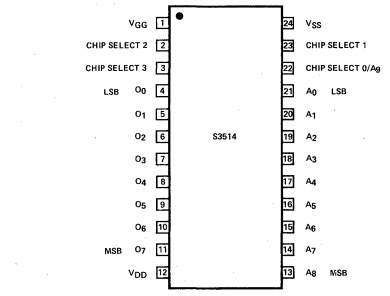
4096 BIT STATIC
MOS READ ONLY MEMORY

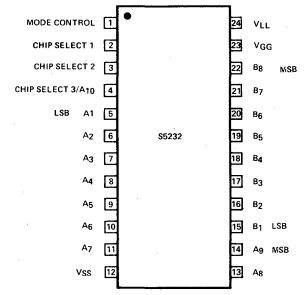
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



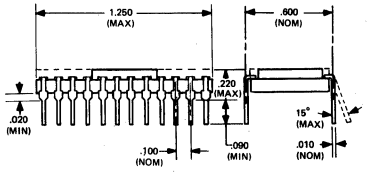
BLOCK DIAGRAM





FEATURES

- Static Operation – No Clocks Required
- High-speed –600 ns Typical Access Time
- Bus ORable Outputs – Three States
- Multiple ROM Control – 4 Chip Selects
- Standard Supplies – +5V, 0V, –12V
- S3514 Replaces FAIRCHILD 3514
- S5232 Replaces National MM 5232



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W - see Sec. 1)

FUNCTIONAL DESCRIPTION

The AMI S3514 and S5232 are TTL compatible MOS read-only memories (ROM) designed to store 4096 bits of information by programming one mask pattern. The word and bit organizations of these ROMs are either 512 x 8 or 1024 x 4. Both ROMs have push-pull outputs that can be in one of three states: HIGH, LOW or open (unselected state). This, plus the programmable Chip Selects, enables the use of several ROMs in parallel with no external components. Since the ROM is a static device, no clocks are required, making these ROMs both versatile and easy to use.

Low threshold-voltage processing, utilizing AMI's I^{2}TM is used with P-channel, depletion-mode MOS technology to provide direct output interfacing with TTL and DTL logic families. All inputs are protected to prevent damage from static charge accumulation.

TYPICAL APPLICATIONS

Code Conversion, Table Lookup, Microprogramming, Control Logic.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Terminal Relative to V_{SS} (except V_{GG})	+ 0.3V to –10V
Voltage on V_{GG} Terminal Relative to V_{SS}	+ 0.3V to –20V
Operating Temperature Range (Ambient)	0°C to + 70°C
Storage Temperature Range (Ambient)	–55°C to + 150°C

RECOMMENDED OPERATING CONDITIONS

($0°C \leqslant T_A \leqslant 70°C$)

	Parameter	Min.	Max.	Units	Notes (Page 5-8)
V_{SS}	Supply Voltage	+4.75	+5.25	V	
V_{DD}	Supply Voltage	0	0	V	Note 1
V_{GG}	Supply Voltage	–11.4	–12.6	V	
V_{LL}	Output Load Voltage	0	–12.6	V	Note 2, 7
V_{IL}	Input Voltage, LOW Level	0	V_{SS}–4.0		
V_{IH}	Input Voltage, HIGH Level	V_{SS}–1.5	V_{SS}	V	Note 3
V_{IH}	Input Voltage, HIGH Level	V_{SS}–2.0	V_{SS}	V	Note 4

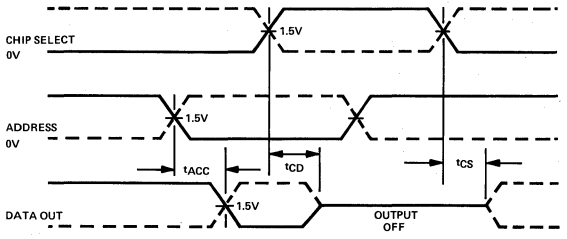
ELECTRICAL CHARACTERISTICS

(V_{SS} = +5.0V ± 5%; V_{DD} = 0V; V_{GG} = –12V ± 5%; V_{LL} = –12V ± 5%; $0°C \leqslant T_A \leqslant 70°C$ unless noted otherwise)

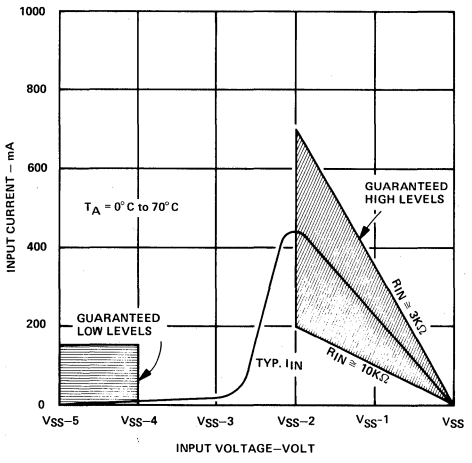
	Parameter	Min.	Max.	Units	Notes (Page 5-8)
I_{SS}	Supply Current, V_{SS}		28.0	mA	Note 5
I_{GG}	Supply Current, V_{GG}		28.0	mA	Note 5
R_{LL}	Output Load Resistor	500	2000	Ω	Note 7
$I_{I(L)}$	Input Leakage Current,		1.0	μA	$V_I = V_{SS}$ –6.0V. Note 3
I_{IL}	Input Current, LOW Level	0	–150	μA	$V_I = V_{SS}$ –4.0V. Note 4
I_{IH}	Input Current, HIGH Level	–200	–700	μA	$V_I = V_{SS}$ –2.0V. Note 4
V_{OL}	Output Voltage, LOW Level		0.4	V	I_{OL} = 1.6mA
V_{OH}	Output Voltage, HIGH Level	2.4		V	I_{OH} = –100μA
$I_{O(L)}$	Output Leakage Current		+10	μA	Outputs disabled ($V_O = V_{SS}$ –6V)
C_{IN}	Input Capacitance		10	pF	Note 6
C_O	Output Capacitance		10	pF	Note 6
t_{ACCESS}	Address to Output Access Time		1000	nsec	Note 8, See Timing
t_{CS}	Chip Select to Output Delay		800	nsec	
t_{CD}	Chip Deselect to Output Delay		800	nsec	

NOTES:
1. Not available on S5232
2. Not available on S3514
3. This parameter is for inputs without active pull-ups (programmable).
4. This parameter is for inputs with active pull-ups (programmable) for TTL interfaces. As the TTL driver goes to a HIGH level it must only provide $V_{SS}-2.0V$ (this voltage must not be clamped) and the input circuit pulls the output of the TTL device to V_{SS}. See Optional Input Pull-up Characteristics.
5. Inputs at V_{SS}, outputs unloaded. V_{DD} current comes only from the output loads.
6. $V_{Bias} - V_{SS} = 0V$; f = 1 MHz.
7. This option available only on S5232 with 1024 x 4 organization. For 512 x 8 organization, $V_{LL} = 0V$. For 1024 x 4 organization, $V_{LL} = 0V$ if R_{LL} is not programmed in; and $V_{LL} = -12V \pm 5\%$, if R_{LL} is programmed in. See output stage circuit options.
8. Outputs sinking 1.6mA or sourcing $-100\mu A$ and total load capacitance = 75pF.

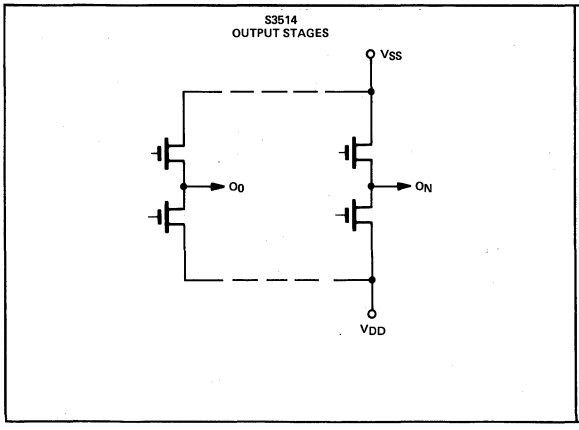
TIMING CHARACTERISTICS

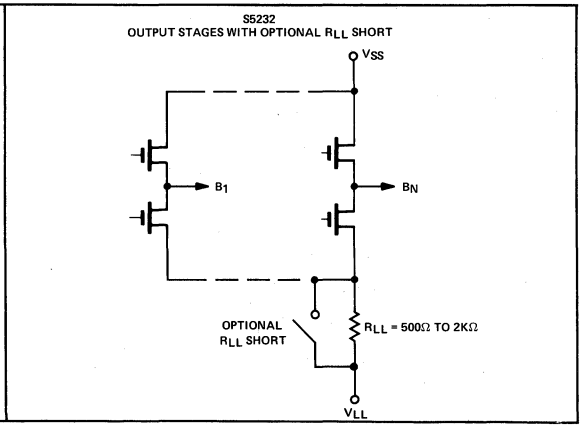


OPTIONAL INPUT PULL-UP CHARACTERISTICS

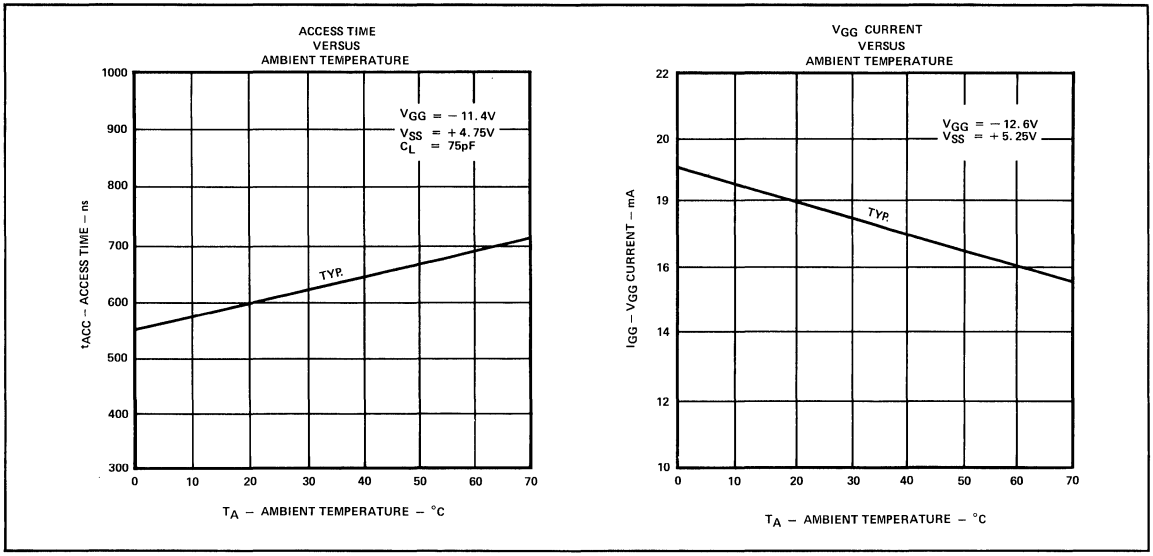


OUTPUT STAGE CIRCUIT OPTIONS





TYPICAL CHARACTERISTICS



OPERATING MODE

S3514

Function	512 x 8	1024 x 4
Chip Select 0/A9	1 or 0	A9
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3	1 or 0	1 or 0

1 = Most Positive = High Level Voltage

512 x 8: Chip Select 0/A9 operates as Chip Select 0.

1024 x 4: *A9 – Low enables odd outputs (O_1, O_3, O_5, O_7)
A9 – High enables even outputs (O_0, O_2, O_4, O_6)
*See note 9 on page 5-8.

Chip Selects: Four programmable chip selects provide control over 16-S3514 ROMS with no external decoding.

S5232

Function	512 x 8	1024 x 4
Mode Control	1	0
Chip Select 1	1 or 0	1 or 0
Chip Select 2	1 or 0	1 or 0
Chip Select 3/A10	1 or 0	address A10

1 = Most Positive = High Level Voltage

512 x 8: Mode Control – High
Chip Select 3/A10 operates as Chip Select 3.

1024 x 4. Mode Control – Low
*A10 – High enables even outputs (B_2, B_4, B_6, B_8)
A10 – Low enables odd outputs (B_1, B_3, B_5, B_7)
*See note 8 on page 5-8.

Chip Selects: Three programmable chip selects provide control over 8-S5232 ROMs with no external decoding.

AMI ROM PUNCHED–CARD CODING FORMAT[1]

S3514

First Card

Cols.	Information Field
1–30	Customer
31–50	Customer Part Number
60–72	AMI Part Number [2]

Second Card

1	Organization[3]
3	CS_0^4/A_9^8
5	CS3[4]
7	CS2[4]
9	CS1[4]
11	Active Pull-ups[5]

Data Cards/512 x 8 Organization

1–4	Decimal Address
6–13	Output O7 – O0 (MSB thru LSB)
15–17	Octal Equivalent of output data[7]

Data Cards/1024 x 4 Organization

1–4	Decimal Address (0–1022) even addresses
6–9	Output (MSB–LSB)
11–12	Octal Equivalent of output data[7]
50–53	Decimal Address (1–1023) odd addresses
55–58	Output (MSB–LSB)
60–61	Octal Equivalent of output data [7]

S5232

First Card

Cols.	Information Field
1–30	Customer
31–50	Customer Part Number
60–72	AMI Part Number [2]

Second Card

1	Organization[3]
3	CS_3^4/A_{10}^9
5	CS2[4]
7	CS1[4]
9	Active Pull-ups[5]
11	Series resistor to V_{LL}[6]

Data Cards/512 x 8 Organization

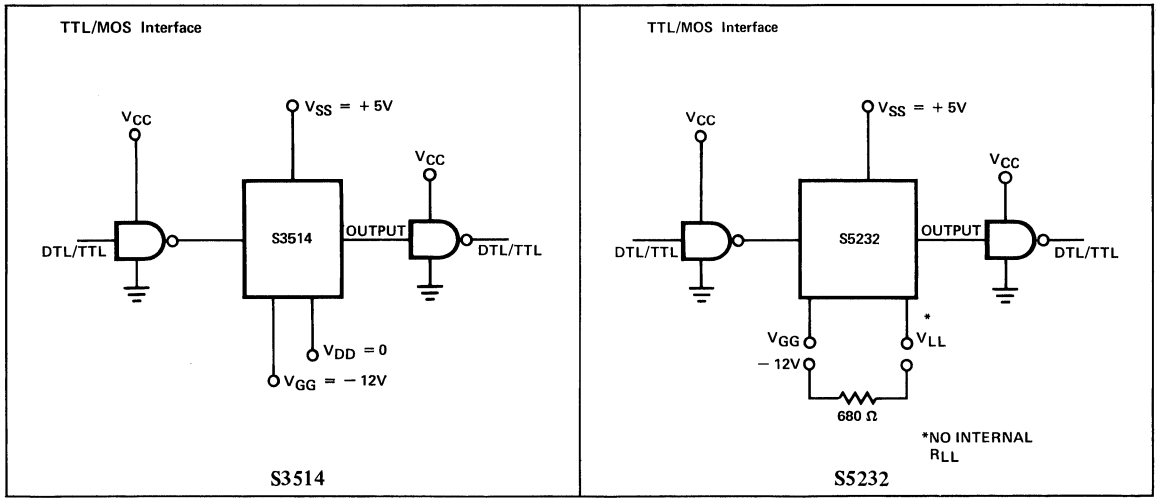
1–4	Decimal Address
6–13	Output B8–B1 (MSB thru LSB)
15–17	Octal Equivalent of output data[7]

Data Cards/1024 x 4 Organization

1–4	Decimal Address (0–1022) even addresses
6–9	Output (MSB–LSB)
11–12	Octal Equivalent of output data[7]
50–53	Decimal Address (1–1023) odd addresses
55–58	Output (MSB–LSB)
60–61	Octal Equivalent of output data[7]

NOTES:
1. Positive logic formats accepted only.
2. Assigned by Marketing Department; may be left blank.
3. A "0" indicates 512 x 8; a "1" indicates 1024 x 4.
4. A "0" indicates the chip is enabled by a logic 0, a "1" indicates it is enabled by a logic 1, and a "2" indicates a "Don't Care" condition.
5. A "1" indicates active pull-ups; a "0" indicates no pull-ups.
6. A "0" indicates an internal resistor, a "1" indicates no internal resistor. Available only with 1024 x 4 organization.
7. The octal parity check is created by breaking up the output word into groups of three from right to left and creating a base 8 (octal) number in place of these groups. For example the output word 10011110 would be separated into groups 10/011/110 and the resulting octal equivalent number is 236.
8. For 1024 x 4 organization, CSO/A9 input acts as A9 address. A9 LOW enables odd outputs; A9 HIGH enables even outputs. For this case, a "0" is required in this field. However, if it is required that A9 HIGH should enable odd outputs and A9 LOW should enable even outputs, a "1" may be punched in this field.
9. For 1024 x 4 organization, CS3/A10 acts as A10 address. A10 LOW enables odd outputs; and A10 HIGH enables even outputs. For this case, a "0" is required in this field. However, if it is required that A10 HIGH should enable odd outputs and A10 LOW should enable even outputs, a "1" may be punched in this field.

TYPICAL APPLICATION

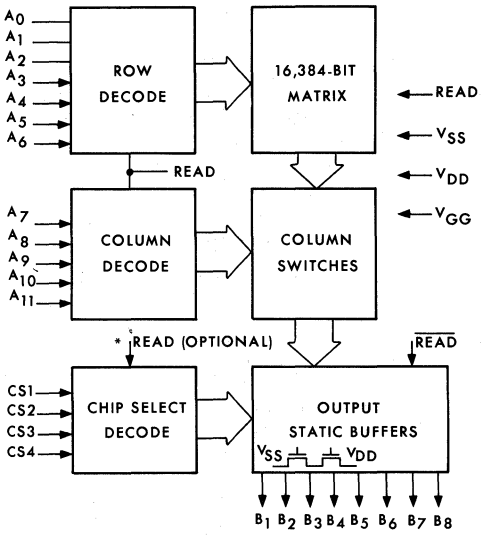


*For applications where V_{GG} is connected to V_{LL}, where low power dissipation is required on outputs and where a constant external resistance is preferred, the internal resistor can be programmed out and an external 680Ω resistor can be connected as shown.

S8996
S9996

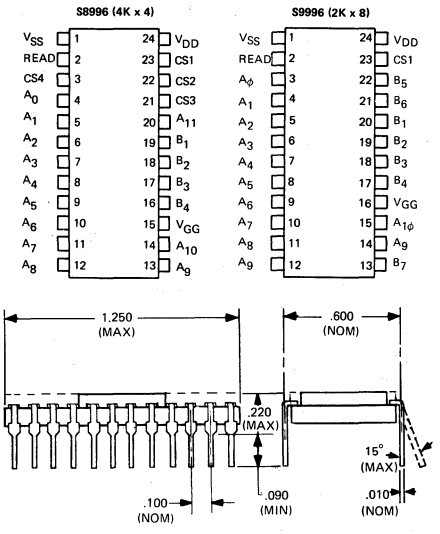
16, 384-BIT
READ-ONLY MEMORY

AMERICAN MICROSYSTEMS, INC.



*for synchronous Chip Select option only

BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W (24 pins) 2I, 1Z (28 pins) - see Sec. 1)

FEATURES

- Output holding registers
- Direct TTL (Tri-state) outputs
- Asynchronous Chip Select for memory expansion
- Synchronous Chip Select optional
- Static Operation
- Low power drain for battery operation
- +5V, − 12V power supplies
- 24-pin DIP package with 28-pin DIP option
- Alternate to AMI-S8865 & SIG-2580

FUNCTIONAL DESCRIPTION

The S8996 and S9996 are 16, 384-bit MOS read-only memories. The S8996 is organized as a 4096 x 4 ROM and the S9996 as a 2048 x 8 ROM respectively. A Read Input controls the entry of data from the ROM into the status output latches. Tri-state outputs allow OR-tying for implementation of larger memories. The outputs of the S8996 are enabled by a programmable 4-bit Chip Select code. The S9996 has one Chip Select in a 24-pin package and two Chip Selects available in a 28-pin package option.

The ROMs are fabricated with AMI'S I^{2TM} low V_T process. Custom patterns may be specified by sending a computer card deck containing the desired memory pattern to AMI. Card deck information is included in this data sheet.

TYPICAL APPLICATIONS:

Portable Low Power Equipment, Microprogramming, Look-up Tables, Random Logic Replacement.

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin	V_{SS} + 0.3V	Storage Chip Temperature	− 55°C to 150°C
Negative Voltage on any Pin	V_{SS} − 20V	Operating Ambient Temperature	0°C to + 70°C

OPERATING CHARACTERISTICS

T_A = 0° to +70°C, V_{SS} = + 5V ± 5%, V_{DD} = 0V, V_{GG} = − 12V ± 5%

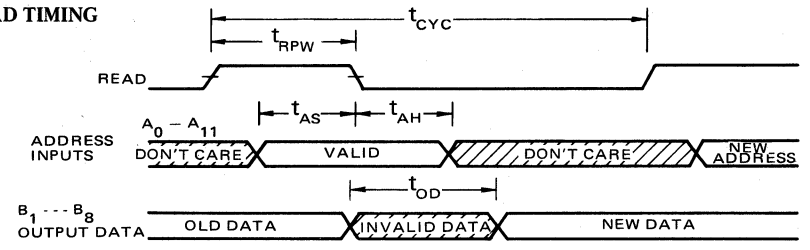
SYMBOL	PARAMETERS	MIN.	MAX.	UNITS	CONDITIONS
V_{IH}	Input High Level	V_{SS} − 1.0	V_{SS}	V	
V_{IL}	Input Low Level		V_{SS} − 4.1	V	
V_{OH}	Output High Level	V_{SS} − 1.0		V	I_L = 400μA Source
V_{OL}	Output Low Level		+ 0.6	V	I_L = 1.6mA Sink
t_{CYC}	Cycle Time	2.3		μs	Note 1
t_{RPW}	Read Pulse Width	500		ns	Test Conditions are
t_{AS}	Address Set Up Time	300		ns	t_r, $t_f \leqslant$25 ns on All
t_{AH}	Address Hold Time	200		ns	Inputs
t_{OD}	Output Propagation		1800	ns	Load=TTL Test Load
t_{CSS}	Chip Select Stable Time	100		ns	Note 2, TTL Test Load
t_{CSH}	Chip Select Hold Time	100		ns	Note 2, TTL Test Load
t_{CS}	Chip Select Output Delay		500	ns	Note 3, TTL Test Load
t_{DS}	Chip De-Select Output Delay		500	ns	Note 3, TTL Test Load
C_{IN}	Input Capacitance		7.5	pF	V_{IN} = V_{SS}, 25°C
C_{OUT}	Output Capacitance		10	pF	V_{OUT} = V_{SS}, 25°C Outputs disabled
I_{DD}	V_{DD} Supply Current		2	mA	Output Terminals Open
I_{GG}	V_{GG} Supply Current		20	mA	

NOTE 1: $t_{CYC\ Min.} = t_{RPW\ Min.} + t_{OD\ Max.}$

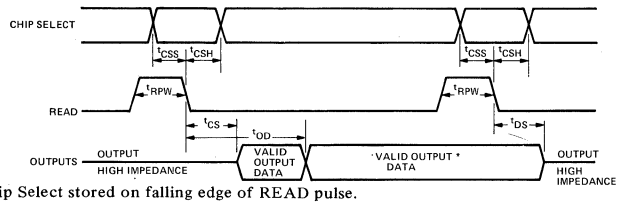
2: Applies only to synchronous Chip Select operation with the synchronous option.

3: Applies only to asynchronous Chip Select operation.

ADDRESS, READ TIMING

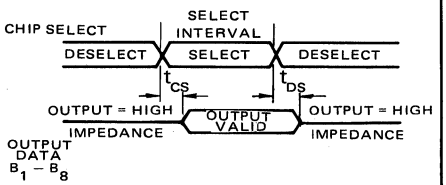


CHIP SELECT TIMING
SYNCHRONOUS OPTION OPERATION*



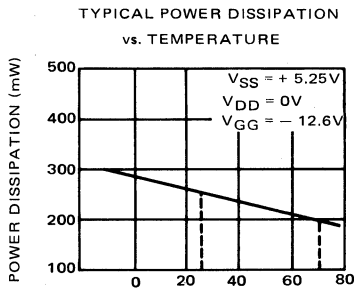
*Chip Select stored on falling edge of READ pulse.

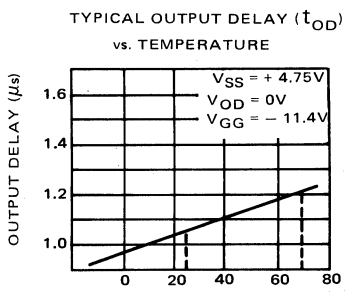
CHIP SELECT TIMING
ASYNCHRONOUS OPERATION*

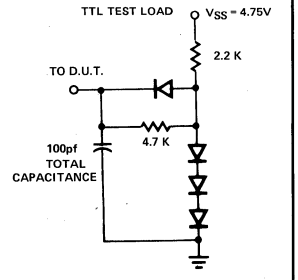


*Chip Select continuously operational

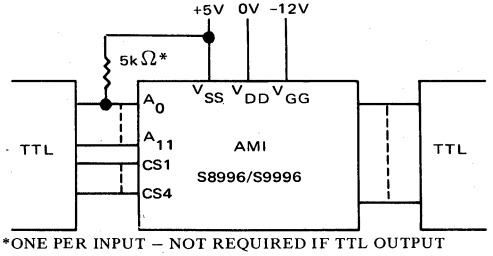
TYPICAL CHARACTERISTIC CURVES





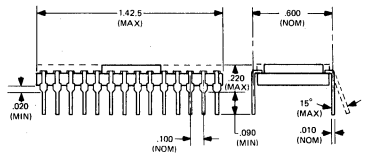


ELECTRICAL CONNECTION



*ONE PER INPUT – NOT REQUIRED IF TTL OUTPUT HIGH LEVEL IS GREATER THAN V_{SS} – 1.5V.

OPTIONAL 28 PIN CONFIGURATION (S9996 - 2K x 8)



V_{SS}	1	28	V_{DD}
READ	2	27	CS1
CS2	3	26	B_5
A_0	4	25	B_6
A_1	5	24	N/C
A_2	6	23	B_1
A_3	7	22	B_2
A_4	8	21	B_3
A_5	9	20	B_4
A_6	10	19	V_{GG}
A_7	11	18	A_{10}
A_8	12	17	A_9
N/C	13	16	B_7
N/C	14	15	B_8

CUSTOM PATTERN PROGRAMMING FORMAT (1)

DATA CARDS

S8996 (4-Bit Output)

FIRST CARD

COLS.	INFORMATION FIELD	
1	Output B_1	Corr
2	Output B_2	Corresponds
3	Output B_3	to Address 0
4	Output B_4	$A_2A_1A_0 = 000$
5	Blank	
6	Output B_1	
7	Output B_2	Corresponds to Address 1
8	Output B_3	$A_2A_1A_0 = 001$
9	Output B_4	
10	Blank	
.		
.		
.		Corresponds
39	Output B_4	to Address 7
.		$A_2A_1A_0 = 111$
40 - 72	Blank	
.		
73 - 76	Customer Part Number (4)	
77	Blank	
78 - 80	Card Reference No.	
	First Card – 001	

SECOND CARD THRU 512th CARD

Same as First Card for Addresses
8 thru 4095 in Sequential Order

513th CARD

1	CS1 (2)
2	CS1 (2)
3	CS3 (2)
4	CS4 (2)
15	Output Driver (5)
26	Chip Select Timing (6)
73 - 76	Customer Part Number

S9996 (8-Bit Output)

FIRST CARD

COLS.	INFORMATION FIELD	
1	Output B_1	
2	Output B_2	Corresponds
3	Output B_3	to Address 0
4	Output B_4	$A_2A_1A_0 = 000$
5	Output B_5	
6	Output B_6	
7	Output B_7	
8	Output B_8	
9	Blank	
10	Output B_1	Corresponds
.		to Address 1
.		$A_2A_1A_0 = 001$
.		Corresponds
36	Output B_8	to Address 3
.		$A_2A_1A_0 = 011$
37 - 72	Blank	
.		
73 - 76	Customer Part Number (4)	
77	Blank	
78 - 80	Card Reference No.	
	First Card – 001	

SECOND CARD THRU 512th CARD

Same as First Card for Addresses
4 thru 2047 in Sequential Order

513th CARD

1	CS1 (2, 3)
2	CS2 (2)
15	Output Driver (5)
26	Chip Select Timing (6)
73 - 76	Customer Part Number

NOTES:

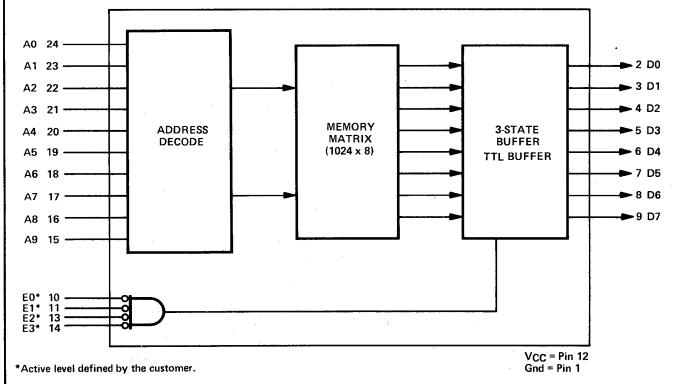
1. Only positive logic formats are accepted. 1 = V_{HIGH}, 0 = V_{LOW}
2. A Φ indicates the chip is enabled by a logic 0; A "1" indicates it is enabled by a logic 1; and a "2" indicates a Don't Care Condition. The outputs are held in the high resistance state for all other codes on these inputs.
3. Four Chip Selects (CS1 thru CS4) are available on the S8996. Two Chip Selects (CS1 and CS2) are available on the S9996 in 28-pin packages. One Chip Select (CS1) is available on the S9996 in 24-pin packages.
4. Assigned by AMI Marketing.
5. A "P" indicates Push-Pull Output; the letter O, not ϕ indicates Open Drain Output to V_{SS}.
6. An "A" indicates the Chip Select inputs are to be entered synchronously (see synchronous Chip Select timing, page 5-12); A "D" indicates asynchronous Chip Selects. (see asynchronous Chip Select timing, page 5-12).

S6830

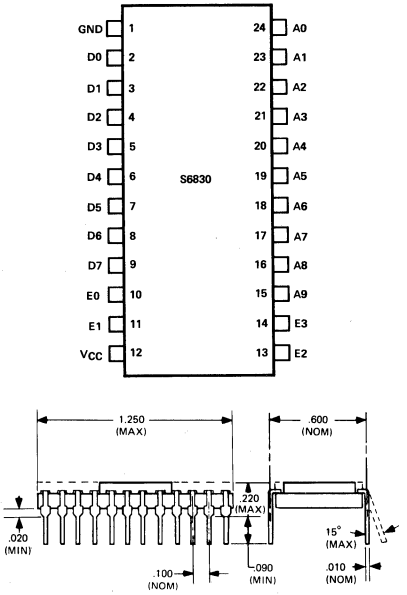
1024 X 8
READ ONLY MEMORY

AMERICAN MICROSYSTEMS, INC.

ADVANCE PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W - see Sec. 1)

FEATURES

- Organized as 1024-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Enable Inputs (Mask Programmable)
- Single 5-Volt Power Supply
- TTL Compatible Input/Output
- Maximum Access Time = 575 ns

FUNCTIONAL DESCRIPTION

The S6830 is a mask programmable read only memory organized 1024 words x 8 bits for application in byte organized systems. The S6830 is totally bus compatible with the S6800 microprocessor. Interfacing to the S6830 consists of an 8 bit three-state data bus, four mask programmable chip selects and ten address lines.

The S6830 is a totally static memory requiring no clocks. Access time is compatible with maximum data rates in a S6800 microprocessor system. The device operates from a single +5 volt power supply and is fabricated with N channel silicon gate technology.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

NOTE: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC (STATIC) CHARACTERISTICS
(V_{CC} = +5 Volt ± 5%; T_A = 0°C to +70°C)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (Norm. Op. Levels)	V_{IH}	2.4	5.25	Vdc
Input Low Voltage (Norm. Op. Levels)	V_{IL}	-0.3	0.4	Vdc
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	2.5	μAdc
Input High Threshold Voltage	V_{IHT}	2.0	–	Vdc
Input Low Threshold Voltage	V_{ILT}	–	0.65	Vdc
Output High Voltage (I_{OH} = -100 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.45	Vdc
Output Leakage Current (V_{OH} = 2.4 V, $\overline{E}$ = 0.4 V, E = 2.4 V)	I_{LOH}	–	10	μAdc
Output Leakage Current (V_{OH} = 0.4 V, $\overline{E}$ = 0.4 V, E = 2.4 V)	I_{LOL}	–	10	μAdc
Supply Current (V_{CC} = 5.25V, T_A = 0°C)	I_{CC}	–	130	mAdc

CAPACITANCE

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitance	C_{in}	–	–	7.5	pF	f = 1.0 MHz
Output Capacitance	C_{out}	–	–	15	pF	T_A = 25°C

AC (DYNAMIC) CHARACTERISTICS

V_{CC} = +5 Volt ± 5%; T_A = 0°C to +70°C

READ CYCLE (All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{cyc} (R)	575	–	ns
Output Enable Delay Time	t_{ED}	–	300	ns
Output Disable Delay Time	t_{DD}	10	150	ns
Read Access Time	t_{acc}	–	575	ns

READ CYCLE TIMING

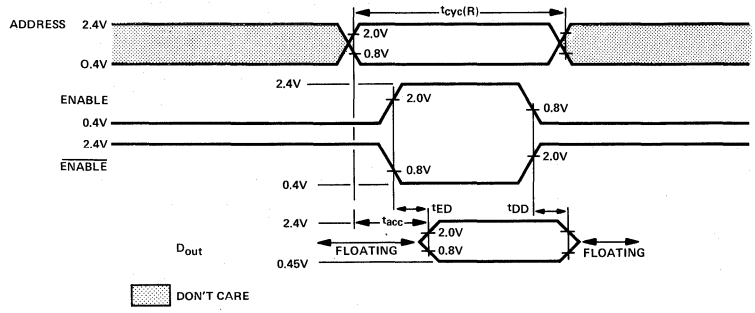
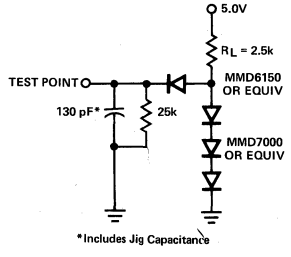


FIGURE 1 – AC TEST LOAD



6

Microprocessors

Selection Guide–Microprocessors

S6800 Microprocessing Family

Part No.	Description	Input/ Output	Power Supply (V)	Process	Package	See Page
S6800	Processor (8-bit)	TTL	+5V	N-SiGate	3M	6-16
S6810	RAM (128 x 8)	TTL	+5V	N-SiGate	2L,1W	6-34
S6830	ROM (1024 x 8)	TTL	+5V	N-SiGate	2L,1W	6-38
S6820	Peripheral Interface Adapter	TTL	+5V	N-SiGate	3M,1T	6-41
S6850	Asynchronous Communications Interface	TTL	+5V	N-SiGate	2L,1W	6-53
S2350	Synchronous Receiver/Transmitter	TTL	+5V	N-SiGate	3M,1T	6-63
S6605	RAM (4096 x 1)	TTL	±5V, +12V	N-SiGate	2C,1C	6-72

9209 Microprogrammable Display Processor

Part No.	Description	Input/ Output	Power Supply (V)	Process	Package	See Page
9209	Processor (4-bit)	MOS	-15V	P-SiGate	1T	6-73
S2299	Keyboard Buffer	Kbd/MOS	-15V	P-I^2	1T	6-80

Future Products

S6860 – a 0-600 baud Bell Series 100 Compatible modem that can connect directly to the S6850 ACIA. It is packaged in a 24-pin DIP.

Read Only Memory, 2048 x 8 – a mask programmable MOS memory, organized to be compatible with the S6800 MPU. The data, address, and control lines match those of the MPU, all signal levels are TTL compatible and it operates on a +5V power supply.

PROM – 512 x 8 bit Erasable PROM

S6800 Microprocessing Family

S6800 Microprocessor (MPU) – an 8-bit parallel processor, with the ability to address up to 65K bytes of memory, and execute instructions in 2 microseconds. It is manufactured using N-channel MOS technology and operates on a single +5V power supply. All inputs and outputs are TTL compatible. The MPU has six internal registers, four types of vectored interrupts and 72 basic instructions. The basic instructions can be used in different addressing modes to save instruction execution time and memory space.

S6810 Static Read/Write Memory, 128 x 8 – an N-channel MOS memory designed and organized to be compatible with the S6800 MPU. Its data, address and control line organization and functions match those of the MPU, all signal levels are TTL compatible and no clocks or refreshing are needed. There are two versions of this memory: S6810 with 1.0 μsec maximum access time, and S6810-1 with 575 nsec. maximum access time.

S6830 Read Only Memory, 1024 x 8 – an N-channel MOS mask programmable read only memory that is used for storing the S6800 MPU operating programs. Like the S6810 RAM, this ROM has data, address, and control line organization that is compatible with that of the MPU. Its signal levels are TTL compatible and it can be accessed in a maximum of 575 nsec.

S6820 Peripheral Interface Adapter (PIA) – a general purpose programmable interface circuit that provides the means for most any kind of peripheral device or circuit to communicate with the S6800 MPU. The PIA has two 8-bit input/output ports for communicating with the peripherals and the MPU can program either port to send or receive data. Each port has two control lines associated with it. These also can be programmed by the MPU to handle interrupt and handshake routines with the peripherals.

S6850 Asynchronous Communication Interface Adapter (ACIA) – a general purpose communications interface that allows an asynchronous serial communications device to transmit data to and receive data from a S6800 microcomputer system. The ACIA can be programmed for handling different word lengths at various data rates; it also has parity generation and checking capability. For interfacing with the S6860 modem, the ACIA provides three status and command lines.

S6800 SYSTEM COMPATIBLE COMPONENTS

S2350 Universal Synchronous Receiver/Transmitter (USRT) – a general purpose communications interface that allows a high speed synchronous communications device to transmit data to and receive data from a S6800 microcomputer system. It connects to the peripheral device via separate serial transmit and receive lines and to the S6800 system data and address bus through a S6820 PIA.

The USRT has separate internal receiver and transmitter sections, which can be clocked by two separate clocks. It has the capability to handle different word lengths, generate and check parity and other conditions, detect sync during receive, and send a fill character during transmit operation.

S6605 Random Access Memory, 4096 x 1 – an N-channel Si-gate dynamic RAM for large volume low cost read/write storage. This memory has TTL compatible inputs and outputs, that can be easily interfaced to the S6800 system bus, access times as low as 230 nsec, and it operates on a single clock/chip-enable signal.

S6800 Microcomputer Systems

LSI FAMILY

The AMI S6800 Microprocessing Family is a series of matched MOS large scale integrated circuits for building microcomputer systems. In the same way as individual logic elements and subsystem functions in SSI and MSI* families are building blocks for random logic circuits, so the AMI S6800 LSI circuits are a family of building blocks for microcomputer systems.

The LSI family, however, is also very different from SSI/MSI. With LSI, the hardware designer can deal with whole subsystems, instead of individual logic elements: his design task is much simpler and faster; the functional complexity of the final system can be greatly increased, while its physical size is reduced.

Another difference relates to applications. Because a microcomputer system can be programmed, whereas a random logic circuit generally cannot, the LSI family is primarily used for different applications than those of SSI/MSI. It certainly overlaps the SSI/MSI applications, because LSI microcomputers can be used advantageously in direct replacement of random logic circuits (they can be programmed to perform the same functions), but the most important applications of microcomputers are in the areas where random logic circuits cease to be practical. A microcomputer can typically perform tasks that would require extremely complex and space consuming random logic circuits, because programming gives the microcomputer a whole order of added capability.

AMI S6800

The AMI S6800 Microprocessing Family hardware includes a microprocessor, ROM and RAM memories, and data input/output circuits. These components may be assembled in a building block manner into a very simple microcomputer system, or into any of progressively more complex systems, which can be used in many general or special purpose applications. The important feature of the S6800 family is that within any system all components are directly compatible in signal functions, circuit performance characteristics, and logic levels. All operate on a single +5V power supply.

**SSI and MSI – small scale and medium scale integration.*

It remains to the user to integrate the microcomputer into his own large system and to program it for a specific task. The task may be either simple or complex and either general in purpose or highly specialized for one application.

To facilitate system design and programming, AMI will provide a comprehensive set of reference documents, design and programming aids, a program library, and other applications support. For example, AMI will make available a comprehensive hardware and software reference manual, a S6800 program assembler, and a simulator. Such design and programming support is a continuing and expanding effort at AMI.

BASIC S6800 MICROCOMPUTER SYSTEM

A basic system built with the S6800 components is shown in Figure 1. In this system the S6800 Microprocessor (MPU) is supported by over 1K bytes of memory and controls one input/output interface circuit. The 1024-byte ROM is used to store the operating program, the 128-byte RAM provides working storage for the MPU, and the Peripheral Interface Adapter (PIA) provides two independently programmable 8-bit input/output ports for communicating with two peripheral devices.

The S6800 system is bus oriented. Eight lines form the data bus and 16 more lines make up the address bus. The MPU controls the bus and all other devices – the memories and the PIA – attach to the busses and wait for instructions from the MPU to supply or receive data. In the basic system, Figure 1, the MPU uses address lines A2, A13, and A14 to select one of the three devices on the bus and the Read/Write and Valid Memory Address lines to instruct the devices to receive or send data to the MPU. When communicating with the PIA, address lines A0 and A1 are used to select among the two peripheral devices A and B; the CA1, CA2, CB1, and CB2 lines can be used to send out control signals to the peripherals, or receive interrupts.

The basic system is a complete microcomputer, which can be used for a large variety of applications. It is simple but versatile, because it can be easily reprogrammed by changing the ROM. The user must provide only the two-phase clock signal source, a power-up/restart circuit, and a single +5V power supply to complete the hardware.

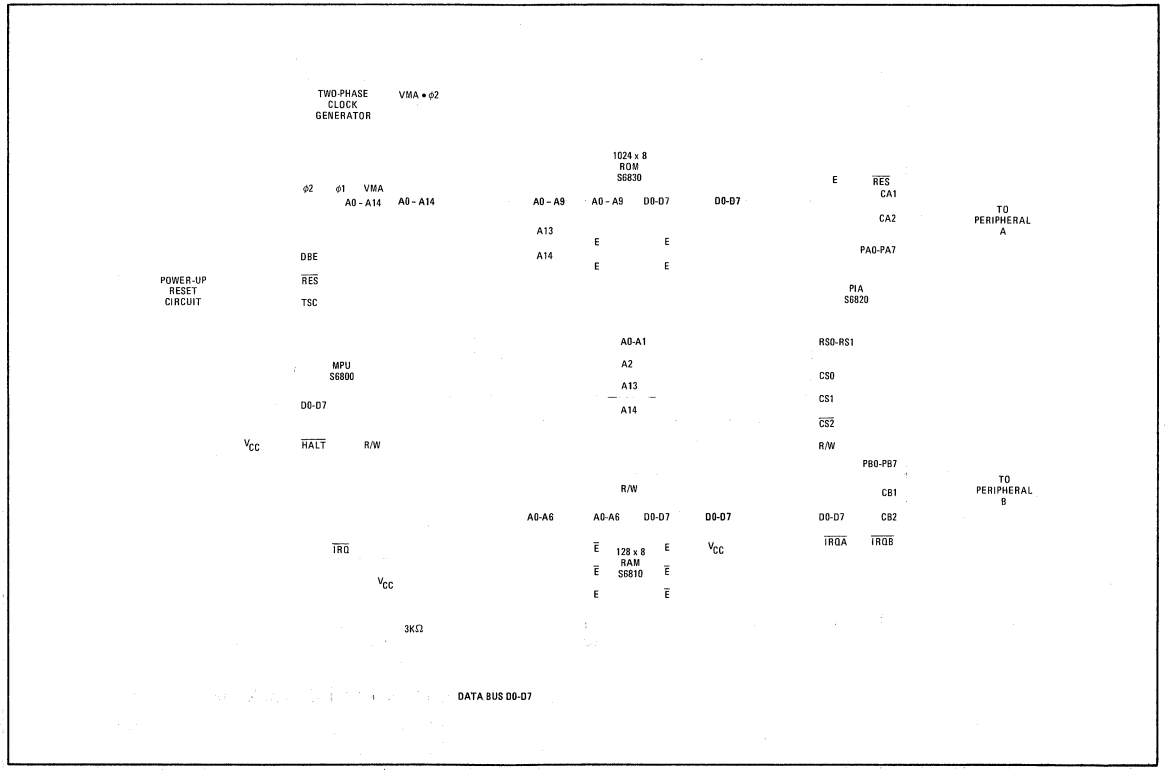
EXPANDING THE S6800 SYSTEM

The basic system can be altered or expanded in many different ways. For example, the S6850 Asynchronous Communication Interface Adapter (ACIA) can be substituted for the PIA, to enable the microcomputer to interface with a telecommunications modem. Or, additional memory can be added – either RAM or ROM – to expand the processing capability of the MPU. In general, the system can be expanded in a modular manner, by adding onto the bus as many as ten devices out of the S6800 family. These can be any combination of memory or input/output interface circuits. In this manner a system of nearly any complexity and configuration can be assembled. (Systems with more than ten devices on the bus require the addition of address and data bus buffers to operate at full speed.)

By building your microcomputer from the S6800 family of devices, you take advantage of the compatibility of the devices. They all conform to the bus discipline, all are compatible in load levels, and the entire system runs on a common system clock. In effect, you eliminate most all circuit design, save for the simple clock and power-up/restart circuits. Because you are dealing with only a small number of integrated circuits, circuit layout is simple and the entire microcomputer can be located on a single circuit card.

In some special purpose applications you may need to attach your own interface devices to the bus. As a result, more circuit design will be required, but you will find the S6800 MPU easy to work with. It has features that allow it to be used in many different systems. For example, by using the Halt, Three State Control, and Data Bus Enable lines you can easily design a direct memory access system, in which either the MPU or a peripheral device can read or write into the RAM and utilize the bus on a priority basis. You can also design a multiprocessor system, in which several MPUs can be attached to the same bus and share processing assignments, as well as memory space.

Figure 1 Basic S6800 Microcomputer System



S6800 INPUT/OUTPUT

One of the most important advantages that any S6800 system has to offer is its input/output versatility. In any computer system, large or small, the CPU internal functions are determined by the architecture of the computer and the user usually has little opportunity or need to alter them. On the other hand, the I/O configuration is almost always determined by the user and subject to change as peripherals are added or other system alterations are introduced. The I/O configuration is important to the user because it can affect the efficiency of the CPU itself, it determines the ease and speed with which peripherals can interact with the system, and determines the thruput rate of the system.

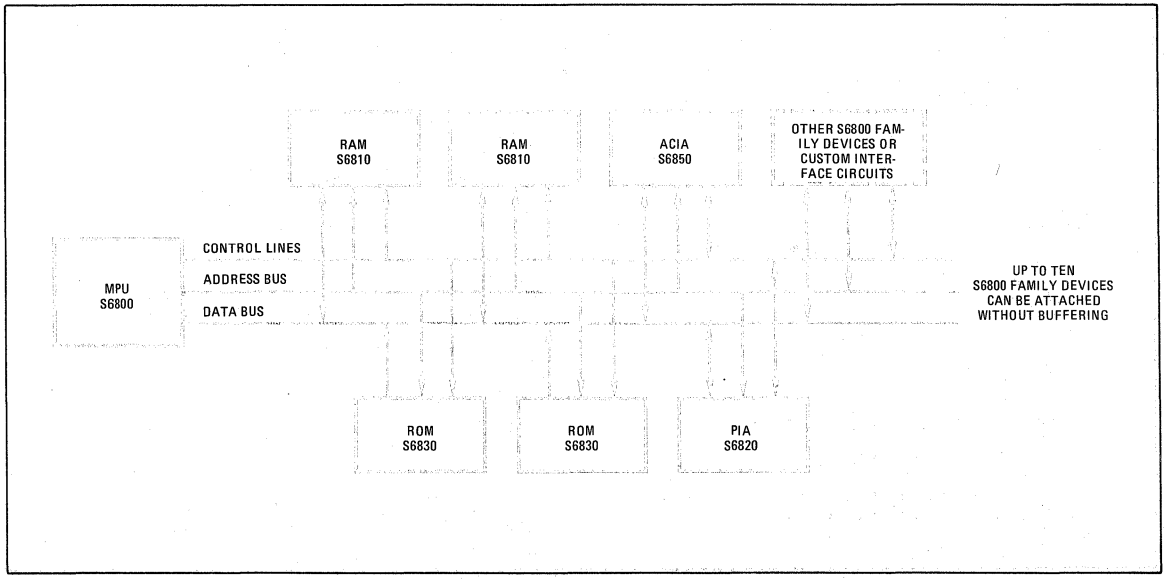
Therefore, the efficiency and versatility with which a CPU can handle its I/O – both in hardware and software – is an important criteria and is of particular concern to the user. It is in this area of I/O that the S6800 MPU excels.

- In a S6800 system, the MPU relegates most of the I/O control to such I/O interfaces as the PIA or ACIA. Each of these circuits is programmable and can interface with peripheral devices without directly involving the MPU. For example, the MPU can preprogram a PIA to either output data to the MPU or to receive it. Thereafter, the PIA circuits assume all functions of interfacing with the peripherals and the MPU never has to look at the interface until service is required. It must service interrupts from the PIA, but never needs to wait for input data to become available or for output data to be accepted. This relieves the MPU of its I/O functions, makes it more efficient in its primary task of data processing, and significantly increases system thruput.

- The I/O interfaces and memory are both located in the same address space within the S6800 system. The MPU can access any I/O device the same as a memory location – with address lines, instead of separate I/O control lines. Therefore, it can manipulate data in the I/O interface registers with the same programmed instructions as it uses for memory locations. This adds flexibility and increases system efficiency.

- The S6800 Instruction Set complements the above I/O addressing capability with specific instructions that can be used to access memory as well as I/O circuit registers and perform directly various manipulations on the data.

Figure 2 Expanding the S6800 System



S6800 INSTRUCTION SET

The S6800 MPU has a set of 72 basic instructions, listed in alphabetical order in Table 1. These include binary and decimal arithmetic functions, as well as logical, shift, rotate, load, store, branch, interrupt, and stack manipulation functions. Most of the instructions have several variations and most can be used with several memory addressing modes (see Table 2). Thus, the total complex of instructions available to the programmer actually is 197.

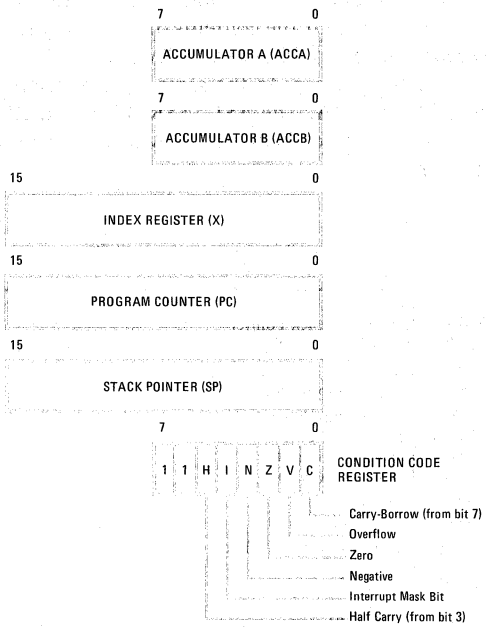
An instruction can be from one to three bytes long, depending on the addressing mode used with the instruction. The first byte always contains the operation code, which designates the kind of operation the MPU will perform. In single byte instructions no memory address is required, because the operation is performed on one of the internal MPU registers. In multiple byte instructions the second and third byte can be the operand, or a memory address for the operand. Formats for multiple byte instructions are shown in Table 2.

A noteworthy feature of the S6800 MPU is that some of the instructions can operate directly on any memory location. In other computer systems it is common that the processor fetches an operand from memory, stores it in the accumulator, then executes the operation in the ALU, and finally writes the result back into the memory. The S6800 is able to accomplish the same with only a single instruction, because it operates with any external location in the same manner as with an internal register. For example, it can directly increment or decrement the contents of a memory location. Because the MPU addresses I/O devices just like a memory location, it can do the same with registers inside the PIA or ACIA. The ASL, ASR, LSR, and ROL are other examples of instructions which operate in this manner.

Table 1 S6800 Microprocessor Instruction Set

ABA	Add Accumulators
ADC	Add with Carry
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
BCC	Branch if Carry Clear
BCS	Branch if Carry Set
BEQ	Branch if Equal to Zero
BGE	Branch if Greater or Equal Zero
BGT	Branch if Greater than Zero
BHI	Branch if Higher
BIT	Bit Test
BLE	Branch if Less or Equal
BLS	Branch if Lower or Same
BLT	Branch if Less than Zero
BMI	Branch if Minus
BNE	Branch if Not Equal to Zero
BPL	Branch if Plus
BRA	Branch Always
BSR	Branch to Subroutine
BVC	Branch if Overflow Clear
BVS	Branch if Overflow Set
CBA	Compare Accumulators
CLC	Clear Carry
CLI	Clear Interrupt Mask
CLR	Clear
CLV	Clear Overflow
CMP	Compare
COM	Complement
CPX	Compare Index Register
DAA	Decimal Adjust
DEC	Decrement
DES	Decrement Stack Pointer
DEX	Decrement Index Register
EOR	Exclusive OR
INC	Increment
INS	Increment Stack Pointer
INX	Increment Index Register
JMP	Jump
JSR	Jump to Subroutine
LDA	Load Accumulator
LDS	Load Stack Pointer
LDX	Load Index Register
LSR	Logical Shift Right
NEG	Negate
NOP	No Operation
ORA	Inclusive OR Accumulator
PSH	Push Data
PUL	Pull Data
ROL	Rotate Left
ROR	Rotate Right
RTI	Return from Interrupt
RTS	Return from Subroutine
SBA	Subtract Accumulators
SBC	Subtract with Carry
SEC	Set Carry
SEI	Set Interrupt Mask
SEV	Set Overflow
STA	Store Accumulator
STS	Store Stack Register
STX	Store Index Register
SUB	Subtract
SWI	Software Interrupt
TAB	Transfer Accumulators
TAP	Transfer Accumulators to Condition Code Reg.
TBA	Transfer Accumulators
TPA	Transfer Condition Code Reg. to Accumulator
TST	Test
TSX	Transfer Stack Pointer to Index Register
TXS	Transfer Index Register to Stack Pointer
WAI	Wait for Interrupt

Figure 3 Program Accessible Registers



MPU REGISTERS:

Accumulators A and B – Two separate 8-bit accumulators that are used to hold operands and results of operations in the ALU.

Index Register – A 16-bit register used for memory address storage in Indexed Addressing operations.

Program Counter – A 16-bit register that holds the current program instruction address. Once the initial program starting address is loaded into the program counter, it is incremented under control of the MPU hardware.

Stack Pointer – A 16-bit register used for storage of the next available location in an external push-down/pop-up stack.

Condition Code Register – An 8-bit register that stores certain results of operations in the ALU. These bits are used as testable conditions for the conditional branch instructions. In addition, one bit position stores the interrupt mask bit and the two high order bits are unused.

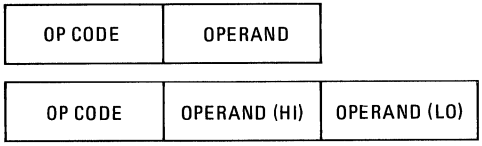
MEMORY REGISTER:

EXTERNAL STACK

The MPU uses a push-down/pop-up stack that can be located anywhere in RAM and be of any convenient size. It is accessed with the stack pointer address and has several uses. First, it always stores the MPU register contents following an interrupt and return addresses during subroutine execution. Second, it can also be used by the programmer to store data during program execution.

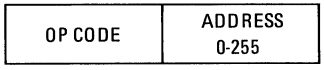
Table 2 Memory Reference Instruction Formats*

Immediate Addressing



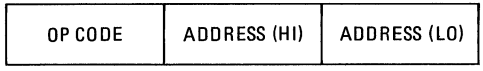
Instruction in which the operand immediately follows the op code. The operand is one byte for all accumulator operations and two bytes for index register or stack register operations.

Direct Addressing



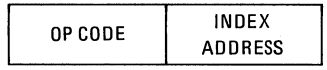
A two byte instruction in which the address of the operand is contained in the second byte of the instruction. This instruction allows direct addressing of operands within the first 256 memory locations (usually a RAM location).

Extended Addressing



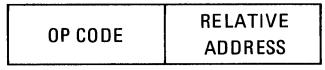
A three byte instruction in which the op code is followed by two bytes containing the full 16-bit memory address. This instruction can be used for addressing all 65,536 memory locations.

Indexed Addressing



A two byte instruction whose second byte is an unsigned number, which is added to the contents of the index register. The resulting 16-bit address is then used to address the memory. The contents of the index register remain unaltered after the addition.

Relative Addressing



A two byte instruction whose second byte is a signed 2's complement number which is added to the program counter. The resulting address is used to access the memory. This instruction allows the addressing of any memory location within a range of 129 bytes forward and 125 bytes back of the address contained in the program counter at the start of the instruction.

(Accumulator and Implied Addressing – These instructions operate directly on an MPU internal register and therefore are not concerned with memory addressing. They always are single byte instructions.)

** Instructions listed in Table 1 represent the operation codes only; in most cases they are followed by an operand or address, in the format shown in this table.*

S6800 MICROPROCESSOR

The S6800 Microprocessor (MPU) is an 8-bit parallel processor. It contains an 8-bit arithmetic unit (ALU), two 8-bit accumulators, one condition code register, and three 16-bit address storage registers, all of which are available for program use (see Figure 4). In addition, there are the following non-accessible registers: a 16-bit address incrementer/decrementer, an 8-bit temporary register and an 8-bit instruction register. There is also an instruction decode ROM and cycle control logic, interrupt and restart logic, bus control and halt logic, and a timing generator.

Within the MPU all data and address transfers between the registers, as well as to and from the ALU, are made across three internal 8-bit busses. The first is a data bus, the second is an address bus for the low order bits, and the third is an address bus for high order bits.

The MPU communicates with its external memory and all I/O devices across an 8-bit bidirectional data bus, D0 through D7, and 16 address lines, A0 through A15. The MPU can be disconnected from either bus by two control signals DBE and TSC.

MPU Operating Cycle. Instructions are executed within the MPU in incremental time periods (MPU cycles), each consisting of one $\phi 1$ clock period and one $\phi 2$ clock period. When the MPU is operating on a 1 MHz input clock, each MPU cycle is 1 microsecond long. It takes a minimum of two MPU cycles to execute an instruction.

During the $\phi 1$ period the MPU typically outputs a memory address to access (fetch) one 8-bit program instruction or data byte and then, during $\phi 2$, loads the byte into an internal register. During the next $\phi 1$ period the MPU executes the associated internal operation with the ALU and the registers. With this fetch-execute sequence an instruction may be completed in only two MPU cycles, or may require as many as 12. While the MPU is executing successive cycles, it is also common for it to overlap functions. For example, during any given clock period the MPU may be executing one instruction in the ALU or registers, while at the same time a fetch is being performed with the address in the program counter.

These internal operations of the MPU, as well as the output of address, data, and control signals, are all managed by the instruction decode and control logic. For example, to perform the execute part of any instruction, the control logic circuits generate signals that cause the ALU to perform addition, subtraction, or some Boolean logic function. These signals can also cause the contents of one register to be transferred into another, a register to be simply incremented or decremented, or some other similar function to occur. Such ALU and register operations are used to execute all of the S6800 instructions.

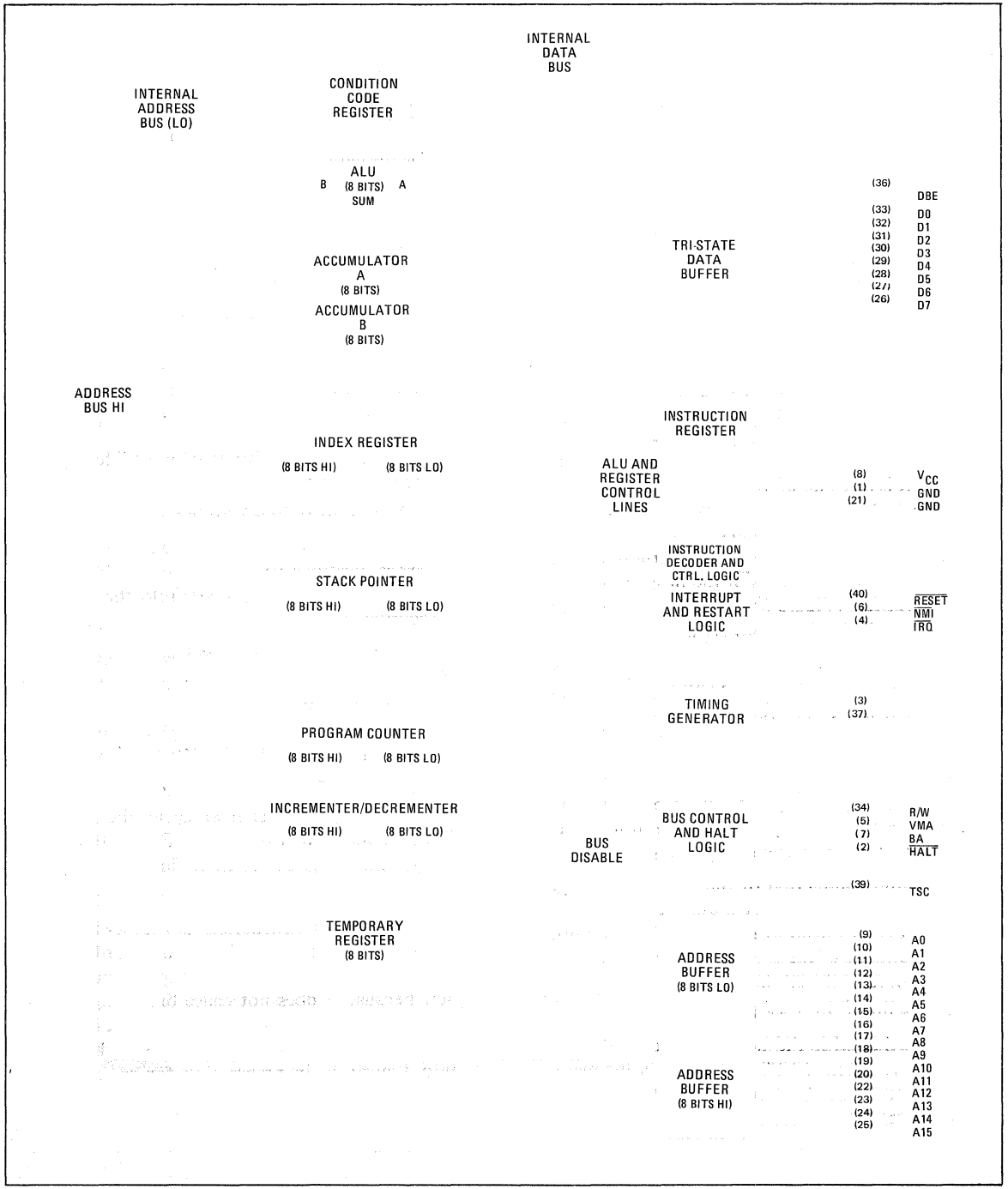
Memory Addressing Modes. During the fetch part of any MPU cycle a memory address is required in order to access a particular location in the external memory. This address is normally stored in the program counter. The program counter is 16 bits wide and therefore, can address any one of a maximum of 65,536 bytes.

At the beginning of a program sequence the MPU is initialized and the beginning address is loaded into the program counter. From there on the program counter is incremented automatically, so that at the end of any instruction cycle it stores the next instruction address. If the program contains an instruction to branch or jump to a different memory location, the op code must be followed by two bytes which load the new address into the program counter. There are, however, addressing techniques with which the jump can be accomplished by fetching only one new address byte out of the memory. These are related to the memory addressing instructions listed in Table 2.

Table 3 Hardware Registers (not accessible by program)

Instruction Register – 8-bit register used to receive and store all program instructions input into the MPU (via the data bus lines D0-D7).	**Incrementer** – 16-bit auxiliary address register, used by the MPU internal control logic, in conjunction with the program counter, to maintain and output the current program address.
Temporary Register – 8-bit register typically used to store the high order address bits prior to their output from the MPU onto the external address bus lines A8-A15.	

Figure 4 Block Diagram of S6800 Microprocessor



For example, if the destination of a branch is within 129 locations forward of 125 locations back of the current program counter contents, Relative Addressing can be used. In this mode only the op code and one signed 8-bit byte is fetched from the memory and is added to the program counter contents.

In Indexed Addressing, a single byte is added to the contents of the index register and the result is transferred into the program counter. Thus, the above addressing variations can be used to reduce the number of bytes that need be fetched to generate a new address. This reduces the number of MPU cycles and speeds up program execution.

The various addressing modes can also be used in a similar manner to generate the source or destination addresses for data.

Table 4 S6800 Interrupts

Nonmaskable Interrupt (NMI) – initiated by a low-going signal on the $\overline{NMI}$ line to the MPU; always interrupts the MPU – even while another interrupt is being processed and the interrupt mask bit is set. Therefore, NMI can be considered to the highest priority interrupt. It causes the following sequence of events:

1. At the completion of the instruction being executed, the contents of the program accessible registers (Figure 3) are stored in the stack.
2. The interrupt mask bit is set.
3. Starting with its next cycle, the MPU accesses locations FFFC and FFFD in the memory and loads the contents into the program counter.

Interrupt Request (IRQ) – initiated by a logic low signal on the $\overline{IRQ}$ line; interrupts the MPU as long as the interrupt mask bit is not set. It causes the following sequence of events:

1. At the completion of the instruction being executed, the interrupt mask bit is tested. If the bit is set the interrupt must wait; if it is not set, contents of the program accessible registers are stored in the stack.
2. The interrupt mask bit is set.
3. Starting with the next cycle, the MPU accesses locations FFF8 and FFF9 in the memory and loads the contents into the program counter.

Software Interrupt (SWI) – initiated by the SWI instruction and causes the following sequence of events:

1. Contents of the program accessible registers are stored in the stack.
2. The interrupt mask bit is set.
3. Starting with the next cycle, the MPU accesses locations FFFA and FFFB in the memory and loads the contents into the program counter.

Reset – initiated by a positive going edge on the $\overline{RESET}$ line to the MPU. It causes the following sequence of events:

1. All program accessible registers are cleared and other circuits in the MPU are initialized.
2. The interrupt mask bit is set.
3. Starting with the next cycle, the MPU accesses locations FFFE and FFFF in the memory and loads the contents into the program counter.

Wait (WAI) – an instruction that causes the MPU to stop all processing and wait for a hardware interrupt. This instruction is not an interrupt in itself because it does not cause branching to any memory address, however, it does cause contents of the program accessible registers to be stored into the stack, in preparation for an interrupt.

Interrupts. The S6800 MPU can be interrupted by any of several signals and program instructions, each of which initiates a different sequence in the MPU. Including the Reset signal, there are four interrupts – three hardware interrupts (signal lines connected to the MPU) and one software interrupt (SWI instruction). Each is described separately in Table 4.

All interrupts are vectored – they cause the MPU to automatically access a predetermined location in the memory and fetch a branch address of the routine or program to which the MPU is to go to service the interrupt. All interrupts except Reset also cause the contents of each program accessible MPU register (with the exception of the stack pointer) to be transferred to the external stack and thus be saved for later processing. The IRQ interrupt is also maskable – it cannot interrupt the MPU as long as bit 4 in the condition code register is set.

APPLICATIONS

The following five figures show various S6800 applications and system interconnections. Because the specific applications of microcomputers are so many and diverse, the figures are intended as general models for systems, in which the particular combination of devices, details of their interconnections, and control line utilization are left up to the user. Refer to the following data sheets for details about each device in the S6800 family.

Figure 5 Data Communications System

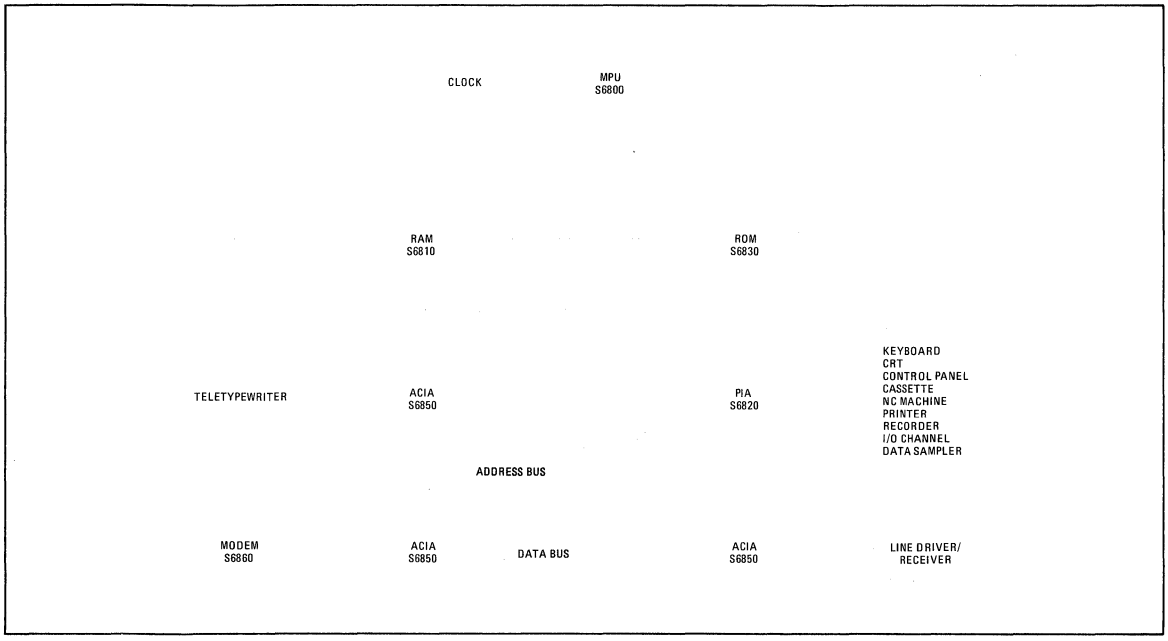


Figure 6 Data Acquisition System

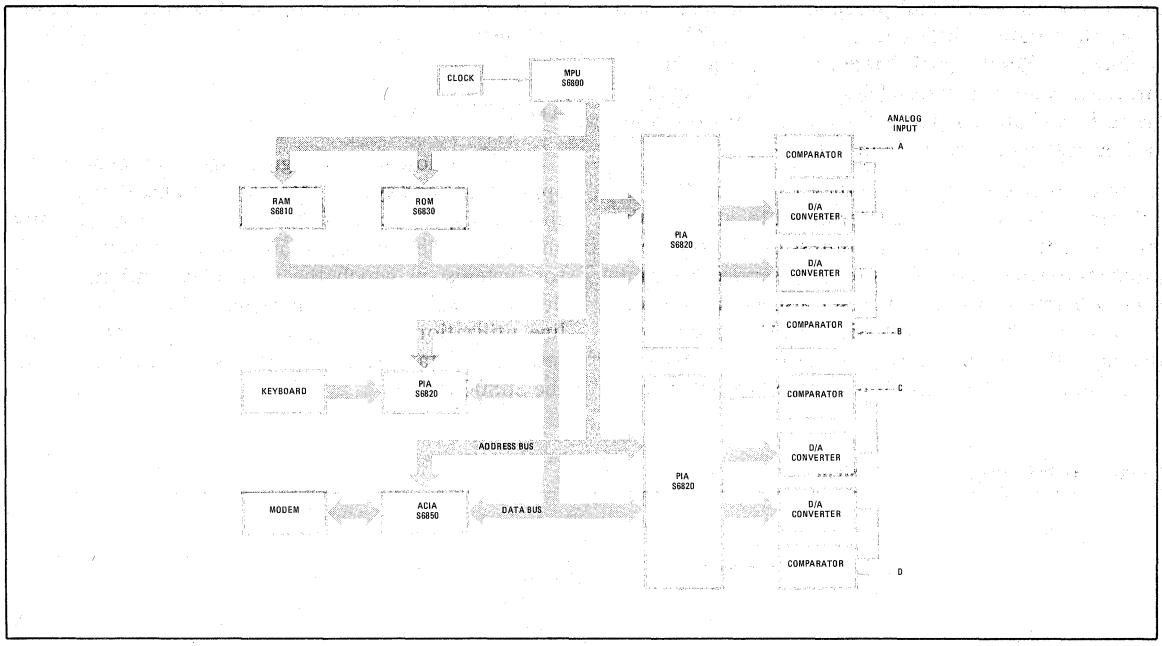


Figure 7 Traffic Control System

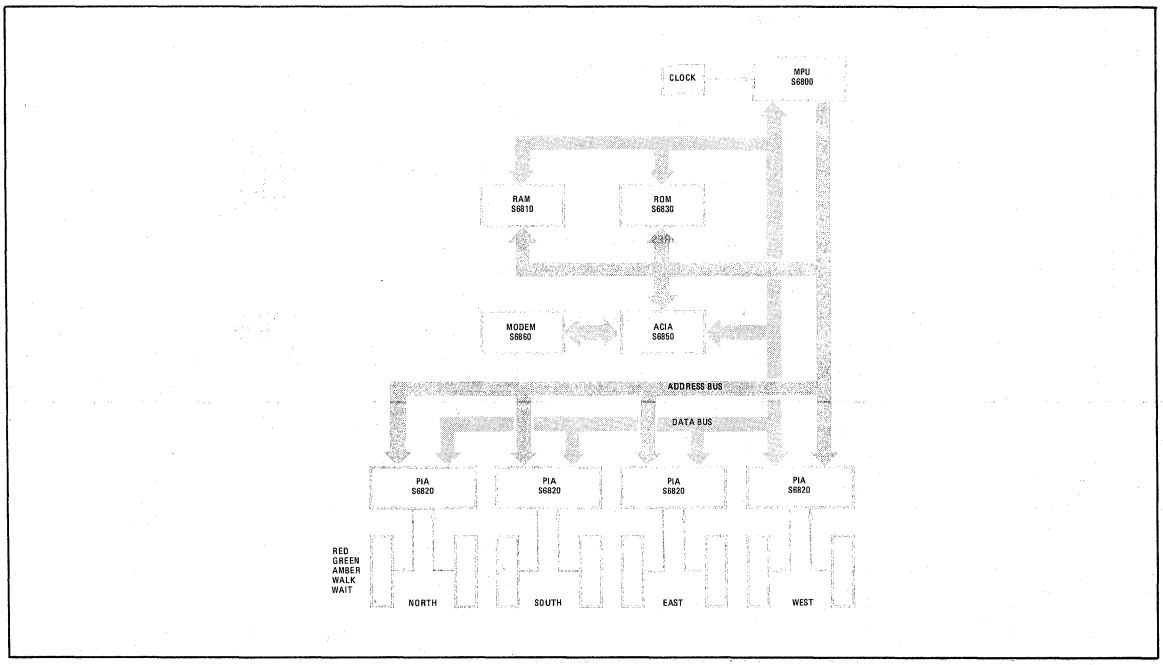


Figure 8 CRT Display System

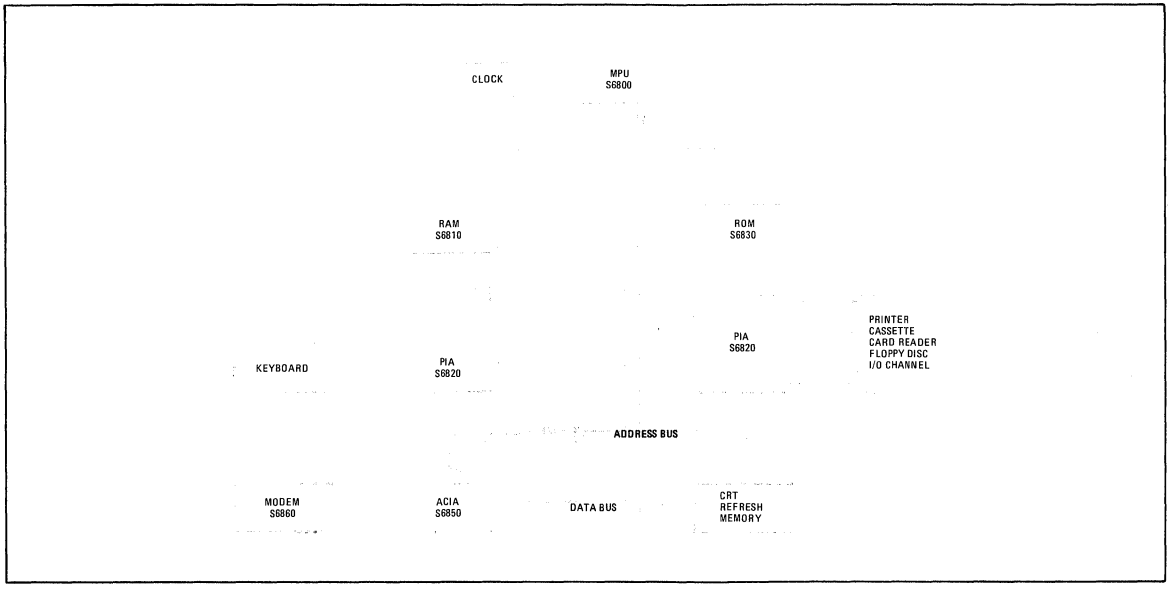
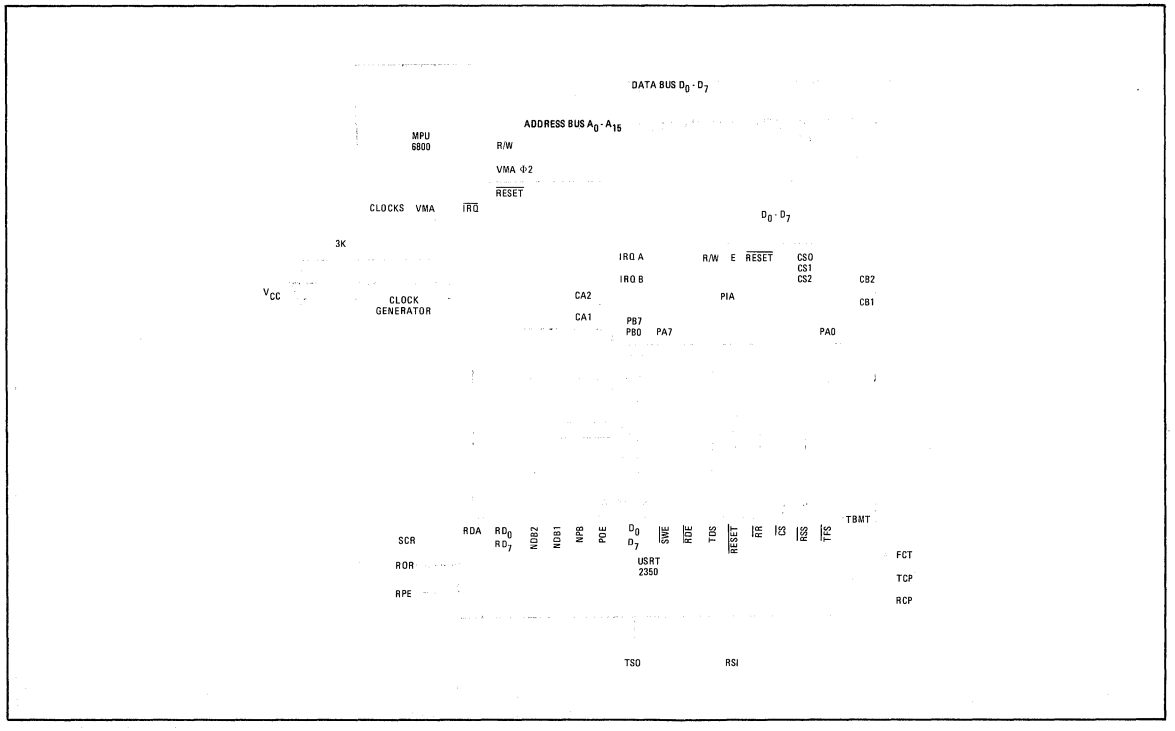


Figure 9 Schematic Diagram for Interconnecting S2350 USRT to the S6800 MPU

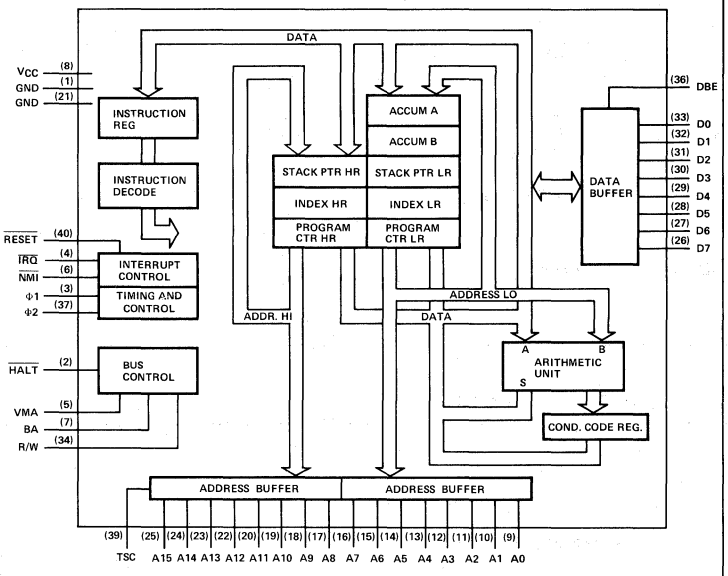


S6800

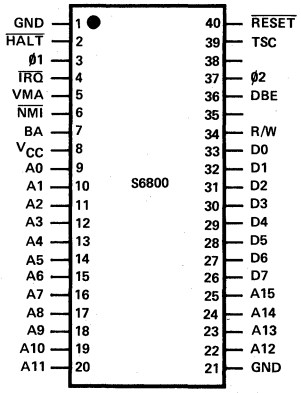
8-BIT
MICROPROCESSOR

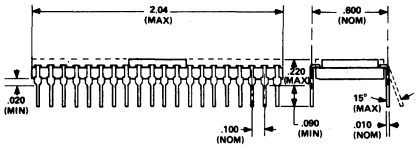
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM





PIN/PACKAGE CONFIGURATION
(Available in Pkg. 3M – see Sec. 1)

FEATURES

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65 k Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- 2 Microsecond Instruction Execution
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Access (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0 V ± 5% = 25°C unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}				Vdc
Logic		+ 2.4	–	V_{CC}	
$\phi1,\phi2$		V_{CC} -0.20	–	V_{CC} + 0.25	
Input Low Voltage (Normal Operating Levels)	V_{IL}				Vdc
Logic		-0.3	–	+ 0.4	
$\phi1,\phi2$		-0.3	–	+ 0.2	
Input High Threshold Voltage	V_{IHT}				Vdc
$\overline{Reset}$, $\overline{NMI}$, $\overline{Halt}$, $\overline{IRQ}$, Data		+ 2.0	–	–	
Input Low Threshold Voltage	V_{ILT}				Vdc
$\overline{Reset}$, $\overline{NMI}$, $\overline{Halt}$, $\overline{IRQ}$, Data		–	–	+ 0.8	
Input Leakage Current	I_{in}				μAdc
(V_{in} = 0 to 5.25 V, V_{CC} = 0) Logic*		–	–	2.5	
$\phi1,\phi2$		–	–	100	
Three-State (Off State) Input Current	I_{TSI}				μAdc
(V_{in} = 0.4 to 2.4 V, V_{CC} = max) Data		–	–	10	
A0-A15, R/W		–	–	100	
Output High Voltage	V_{OH}				Vdc
(I_{Load} = -100 μAdc, V_{CC} = min)		+ 2.4	–	–	
Output Low Voltage	V_{OL}				Vdc
(I_{Load} = 1.6 mAdc, V_{CC} = min)		–	–	+ 0.4	
Power Dissipation	P_D	–	0.600	1.2	W
Capacitance	C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz) Logic		–	–	10	
Data, TSC		–	–	15	
$\phi1,\phi2$		–	–	200	
A0-A15, R/W	C_{out}	–	–	12	pF

*Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3 kΩ pullup load resistors for wire-OR capability at optimum operation.

AC (DYNAMIC) CHARACTERISTICS

(V_{CC} = 5.0 volt ± 5%, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min.	Typ	Max.	Unit
Frequency of Operation	f	0.1	–	1.0	MHz
Clock Timing for 1-MHz Operation (Figure 1) (C_{clock} = 200 pF) Cycle Time	t_{cyc}	1.0	–	–	μs
Clock Pulse Width (Measured at V_{CC} –0.2 V) φ1	$PW_{\phi H}$	430	–	5000	ns
φ2		470	–	5000	
Rise and Fall Times φ1,φ2 (Measured between 0.2V and V_{CC} –0.2 V)	t_r, t_f	–	–	25	ns
Delay Time or Clock Overlap (Measured at 0.2 V)	t_d	0	–	1000	ns

READ/WRITE TIMING

Figures 2 and 3, f = 1.0 MHz, Loading = 130 pF and one TTL Load except VMA and BA Loading = 30 pF and one

Characteristic	Symbol	Min.	Typ	Max.	Unit
Read/Write Setup Time from MPU	T_{ASR}	–	100	300	ns
Address Setup Time from MPU	T_{ASC}	–	200	300	ns
Memory Read Access Time $t_{cyc} - (T_{ASC} + T_{DSU} + t_r)$	T_{ACC}	–	–	575	ns
Data Setup Time	T_{DSU}	100	–	–	ns
Address Setup Time from MPU for VMA	T_{VSC}	–	150	300	ns
Data Hold Time	T_H	10	30	–	ns
Enable High Time for DBE Input	T_{EH}	470	–	–	ns
Data Setup Time from MPU	T_{ASD}	–	150	200	ns

FIGURE 1 – CLOCK TIMING WAVEFORM

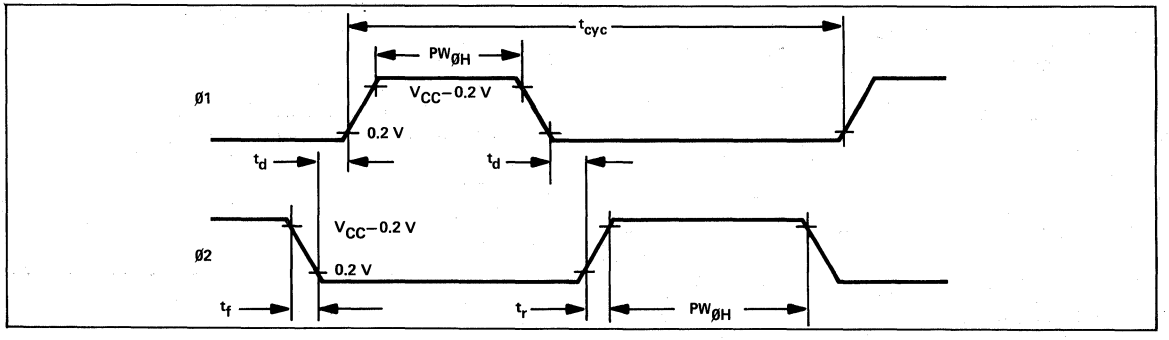


FIGURE 2 – READ DATA FROM MEMORY OR PERIPHERALS

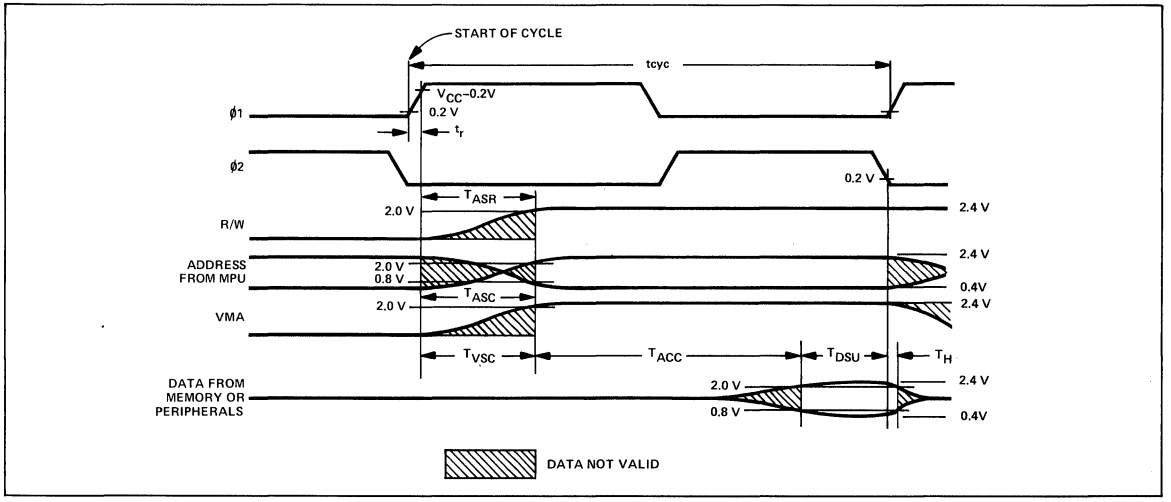
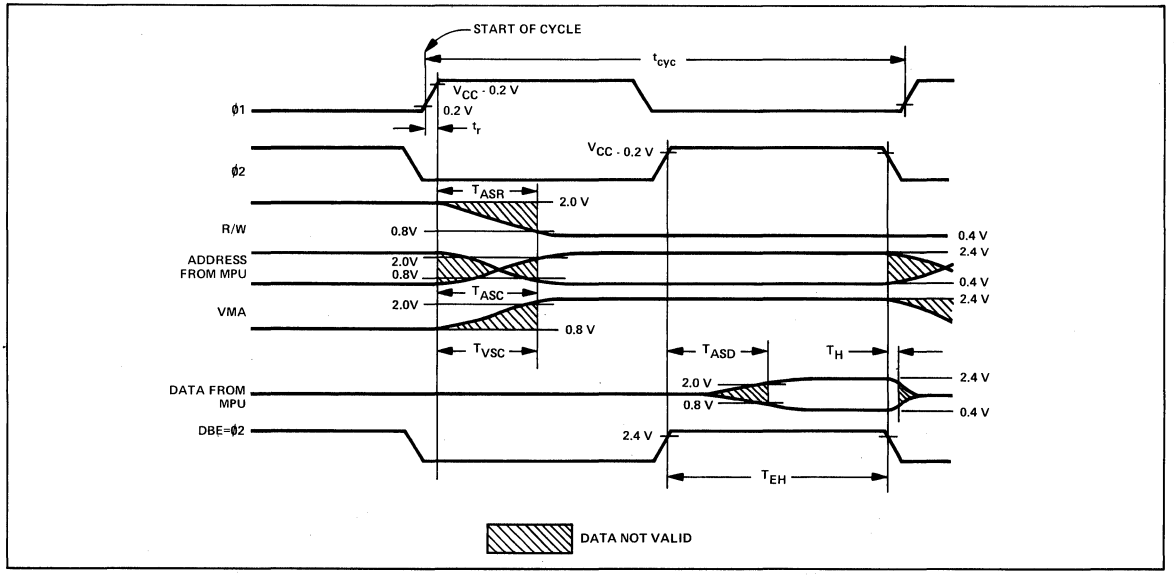


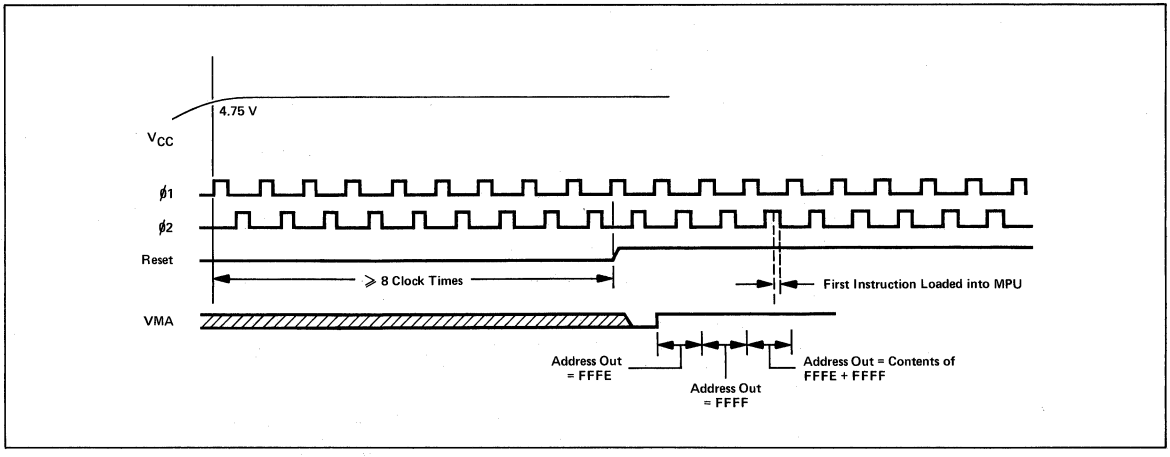
FIGURE 3 – WRITE DATA IN MEMORY OR PERIPHERALS



INTERFACE DESCRIPTION

Label	Pin	Function
$\phi 1$	(3)	**Clocks Phase One and Phase Two** – Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.
$\phi 2$	(37)	
$\overline{\text{RESET}}$	(40)	**$\overline{\text{Reset}}$** – This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts (Figure 4). If $\overline{\text{Reset}}$ goes high prior to the leading edge of $\phi 2$, on the next $\phi 1$ the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

FIGURE 4
INITIALIZATION OF MPU AFTER RESTART



VMA	(5)	**Valid Memory Address** – This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30 pF may be directly driven by this active high signal.

Label	Pin	Function
A0 • • • A15	(9) (25)	**Address Bus** – Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	**Three-State Control** – This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500 ns after TSC = 2.4 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The $\phi 1$ clock must be held in the high state and the $\phi 2$ in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 5.0 μs or destruction of data will occur in the MPU.
D0 • • D7	(33) (26)	**Data Bus** – Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130 pF.
DBE	(36)	**Data Bus Enable** – This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	**Read/Write** – This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three-State Control going high will turn Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130 pF.
$\overline{\text{HALT}}$	(2)	**$\overline{\text{Halt}}$** – When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode. Transition of the $\overline{\text{Halt}}$ line must not occur during the last 250 ns of phase one. To insure single instruction operation, the $\overline{\text{Halt}}$ line must go high for one Phase One Clock cycle.
BA	(7)	**Bus Available** – The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0)or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

Label	Pin	Function
$\overline{IRQ}$	(4)	**Interrupt Request** – This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory. The $\overline{Halt}$ line must be in the high state for interrupts to be recognized. The $\overline{IRQ}$ has a high impedance pullup device internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.
$\overline{NMI}$	(6)	**Non-Maskable Interrupt** – A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the $\overline{Interrupt\ Request}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{NMI}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{NMI}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory. $\overline{NMI}$ has a high impedance pullup resistor internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts. Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are acknowledged during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction.

INTERRUPTS – As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruction (SWI). The processor assumes the uppermost eight memory locations, FFF8 – FFFF, are assigned as interrupt vector addresses as defined in Figure 5.

After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{IRQ}$ or $\overline{NMI}$ inputs as shown by the simplified flow chart in Figure 6. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 7.

FIGURE 5 **MEMORY MAP FOR INTERRUPT VECTORS**

Vector		Description
MS	LS	
FFFE	FFFF	Restart
FFFC	FFFD	Non-maskable Interrupt
FFFA	FFFB	Software Interrupt
FFF?	FFF9	Interrupt Request

FIGURE 6 – MPU FLOW CHART

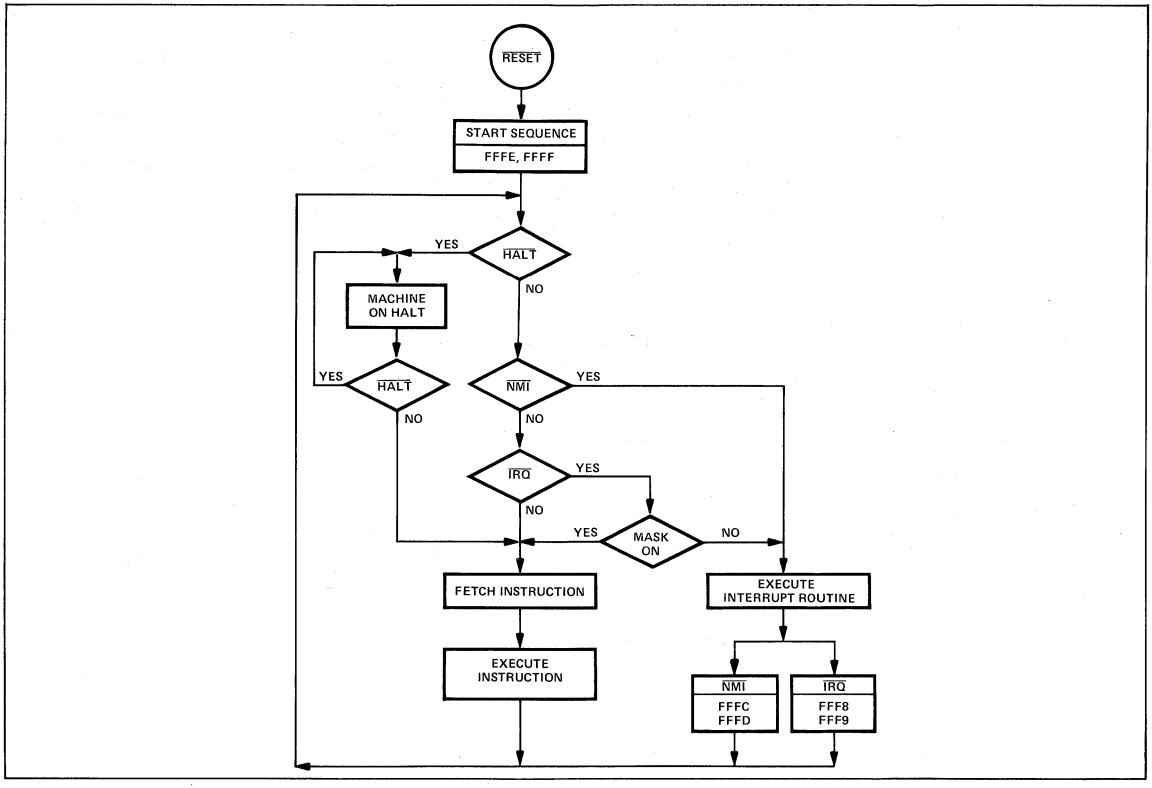
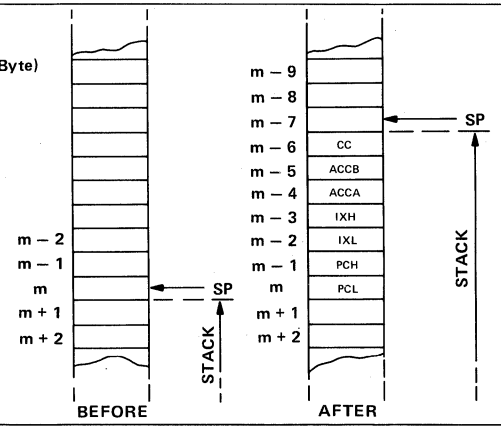


FIGURE 7 – SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits



MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer.

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

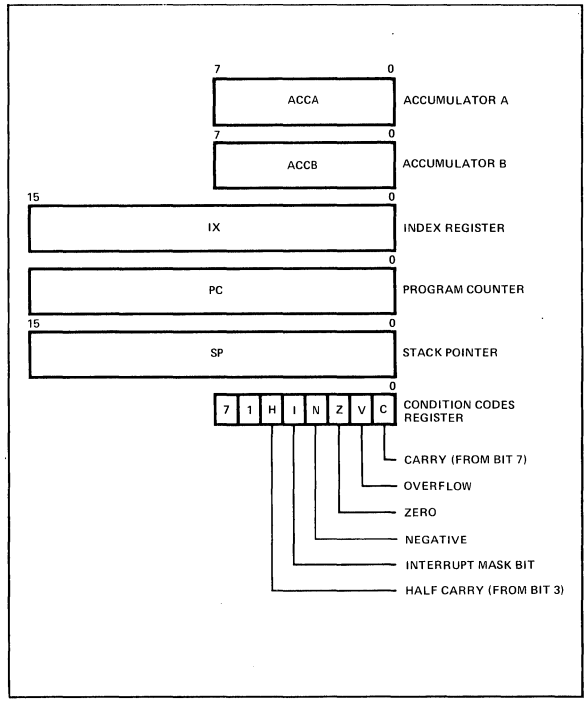
Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from the arithmetic logic unit (ALU).

Condition Code Register – The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

FIGURE 8 – PROGRAMMING MODEL OF THE MICROPROCESSOR



MPU ADDRESSING MODES

The S6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Figure 9 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

ACCUMULATOR ADDRESSING (ACCX)

OP CODE

A single byte instruction addressing operands only in accumulator A or accumulator B.

IMPLIED ADDRESSING

OP CODE

Single byte instruction where the operand address is implied by the instruction definition (i.e., Stack Pointer, Index Register or Condition Register).

IMMEDIATE ADDRESSING

OP CODE	IMMEDIATE OPERAND

OP CODE	IMMEDIATE OPERAND HIGHER	IMMEDIATE OPERAND LOWER

Two or three byte instructions with an eight or sixteen bit operand respectively. For accumulator operations the eight bit operand is contained in the second byte of a two byte instruction. For Index Register operations (e.g. LDX) sixteen bit operand is contained in the second and third byte of a three byte instruction.

DIRECT ADDRESSING

OP CODE	ADDRESS 0-255

Two byte instructions with the address of the operand contained in the second byte of the instruction. This format allows direct addressing of operands within the first 256 memory locations.

EXTENDED ADDRESSING

OP CODE	ADDRESS HIGHER	ADDRESS LOWER

Three byte instructions with the higher eight bits of the operand address contained in the second byte and the lower eight bits of address contained in the third byte of the instruction. This format allows direct addressing of all 65,536 memory locations.

INDEXED ADDRESSING

OP CODE	INDEX ADDRESS

Two byte instructions where the 8 bit unsigned address contained in the second byte of the instruction is added to the sixteen bit Index Register resulting in a sixteen bit effective address. The effective address is stored in a temporary register and the contents of the Index Register are unchanged.

RELATIVE ADDRESSING

OP CODE	RELATIVE ADDRESS

Two byte instructions where the relative address contained in the second byte of the instruction is added to the sixteen bit program counter plus two. The relative address is interpreted as a two's complement number allowing relative addressing within a range of −125 to +129 bytes of the present instruction.

FIGURE 9 – S6800 INSTRUCTION SET

		Addressing Mode							Condition Reg
		Implied	Immediate	Direct	Extended	Indexed	Relative	Boolean/Arith	5 4 3 2 1 0
Instruction	Mnemonic	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	Operation	H I N Z V C
Load accumulator	LDAA		86 2 2	96 3 2	B6 4 3	A6 5 2		M → A	• • ↕ ↕ R •
	LDAB		C6 2 2	D6 3 2	F6 4 3	E6 5 2		M → B	• • ↕ ↕ R •
Load stack pointer	LDS		8E 3 3	9E 4 2	BE 5 3	AE 6 2		$M \rightarrow SP_H$, $(M+1) \rightarrow SP_L$	• • 9 ↕ R •
Load index register	LDX		CE 3 3	DE 4 2	FE 5 3	EE 6 2		$M \rightarrow X_H$, $(M+1) \rightarrow X_L$	• • 9 ↕ R •
Store accumulator	STAA			97 4 2	B7 5 3	A7 6 2		A → M	• • ↕ ↕ R •
	STAB			D7 4 2	F7 5 3	E7 6 2		B → M	• • ↕ ↕ R •
Store stack pointer	STS			9F 5 2	BF 6 3	AF 7 2		$SP_H \rightarrow M$, $SP_L \rightarrow (M+1)$	• • 9 ↕ R •
Store index register	STX			DF 5 2	FF 6 3	EF 7 2		$X_H \rightarrow M$, $X_L \rightarrow (M+1)$	• • 9 ↕ R •
Transfer accumulators	TAB	16 2 1						A → B	• • ↕ ↕ R •
	TBA	17 2 1						B → A	• • ↕ ↕ R •
Transfer Acc. to cond. reg.	TAP	06 2 1						A → CCR	Note 12
Transfer cond. reg. to Acc.	TPA	07 2 1						CCR → A	• • • • • •
Transfer stck ptr to index	TSX	30 4 1						SP + 1 → X	• • • • • •
Transfer index to stck ptr	TXS	35 4 1						X − 1 → SP	• • • • • •
Pull data	PULA	32 4 1						SP + 1 → SP, M_{SP} → A	• • • • • •
	PULB	33 4 1						SP + 1 → SP, M_{SP} → B	• • • • • •
Push data	PSHA	36 4 1						A → M_{SP}, SP − 1 → SP	• • • • • •
	PSHB	37 4 1						B → M_{SP}, SP − 1 → SP	• • • • • •
Add accumulators	ABA	1B 2 1						A + B → A	↕ • ↕ ↕ ↕ ↕
Add	ADDA		8B 2 2	9B 3 2	BB 4 3	AB 5 2		A + M → A	↕ • ↕ ↕ ↕ ↕
	ADDB		CB 2 2	DB 3 2	FB 4 3	EB 5 2		B + M → B	↕ • ↕ ↕ ↕ ↕
Add with carry	ADCA		89 2 2	99 3 2	B9 4 3	A9 5 2		A + M + C → A	↕ • ↕ ↕ ↕ ↕
	ADCB		C9 2 2	D9 3 2	F9 4 3	E9 5 2		B + M + C → B	↕ • ↕ ↕ ↕ ↕
Subtract accumulators	SBA	10 2 1						A − B → A	• • ↕ ↕ ↕ ↕
Subtract	SUBA		80 2 2	90 3 2	B0 4 3	A0 5 2		A − M → A	• • ↕ ↕ ↕ ↕
	SUBB		C0 2 2	D0 3 2	F0 4 3	E0 5 2		B − M → B	• • ↕ ↕ ↕ ↕
Subtract with carry	SBCA		82 2 2	92 3 2	B2 4 3	A2 5 2		A − M − C → A	• • ↕ ↕ ↕ ↕
	SBCB		C2 2 2	D2 3 2	F2 4 3	E2 5 2		B − M − C → B	• • ↕ ↕ ↕ ↕
Increment	INCA	4C 2 1						A + 1 → A	• • ↕ ↕ 5 •
	INCB	5C 2 1						B + 1 → B	• • ↕ ↕ 5 •
	INC				7C 6 3	6C 7 2		M + 1 → M	• • ↕ ↕ 5 •
Increment stack pointer	INS	31 4 1						SP + 1 → SP	• • • • • •
Increment index reg.	INX	08 4 1						X + 1 → X	• • • ↕ • •
Decrement	DECA	4A 2 1						A − 1 → A	• • ↕ ↕ 4 •
	DECB	5A 2 1						B − 1 → B	• • ↕ ↕ 4 •
	DEC				7A 6 3	6A 7 2		M − 1 → M	• • ↕ ↕ 4 •
Decrement stack pointer	DES	34 4 1						SP − 1 → SP	• • • • • •
Decrement index register	DEX	09 4 1						X − 1 → X	• • • ↕ • •
Complement (1's)	COMA	43 2 1						$\overline{A} \rightarrow A$	• • ↕ ↕ R S
	COMB	53 2 1						$\overline{B} \rightarrow B$	• • ↕ ↕ R S
	COM				73 6 3	63 7 2		$\overline{M} \rightarrow M$	• • ↕ ↕ R S
Complement (2's)	NEGA	40 2 1						00 − A → A	• • ↕ ↕ 1 2
	NEGB	50 2 1						00 − B → B	• • ↕ ↕ 1 2
	NEG				70 6 3	60 7 2		00 − M → M	• • ↕ ↕ 1 2
Decimal adjust accumulator	DAA	19 2 1							• • ↕ ↕ ↕ 3

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

		Addressing Mode							Condition Reg
		Implied	Immediate	Direct	Extended	Indexed	Relative	Boolean/Arith	5 4 3 2 1 0
Instruction	Mnemonic	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	OP MC PB	Operation	H I N Z V C
Logical and	ANDA		84 2 2	94 3 2	B4 4 3	A4 5 2		A • M → A	• • ↕ ↕ R •
	ANDB		C4 2 2	D4 3 2	F4 4 3	E4 5 2		B • M → B	• • ↕ ↕ R •
Inclusive or	ORAA		8A 2 2	9A 3 2	BA 4 3	AA 5 2		A + M → A	• • ↕ ↕ R •
	ORAB		CA 2 2	DA 3 2	FA 4 3	EA 5 2		B + M → B	• • ↕ ↕ R •
Exclusive or	EORA		88 2 2	98 3 2	B8 4 3	A8 5 2		A ⊕ M → A	• • ↕ ↕ R •
	EORB		C8 2 2	D8 3 2	F8 4 3	E8 5 2		B ⊕ M → B	• • ↕ ↕ R •
Shift left arithmetic	ASLA	48 2 1						A, B, C, b7, b0	• • ↕ ↕ 6 ↕
	ASLB	58 2 1							• • ↕ ↕ 6 ↕
	ASL				78 6 3	68 7 2		M	• • ↕ ↕ 6 ↕
Shift right arithmetic	ASRA	47 2 1						A, B, b7, b0, C	• • ↕ ↕ 6 ↕
	ASRB	57 2 1							• • ↕ ↕ 6 ↕
	ASR				77 6 3	67 7 2		M	• • ↕ ↕ 6 ↕
Shift right logical	LSRA	44 2 1						A, B, 0, b7, b0, C	• • R ↕ 6 ↕
	LSRB	54 2 1							• • R ↕ 6 ↕
	LSR				74 6 3	64 7 2		M	• • R ↕ 6 ↕
Rotate left	ROLA	49 2 1						A, B, C, b7, b0	• • ↕ ↕ 6 ↕
	ROLB	59 2 1							• • ↕ ↕ 6 ↕
	ROL				79 6 3	69 7 2		M	• • ↕ ↕ 6 ↕
Rotate right	RORA	46 2 1						A, B, C, b7, b0	• • ↕ ↕ 6 ↕
	RORB	56 2 1							• • ↕ ↕ 6 ↕
	ROL				76 6 3	66 7 2		M	• • ↕ ↕ 6 ↕
Compare accumulators	CBA	11 2 1						A − B	• • ↕ ↕ ↕ ↕
Compare	CMPA		81 2 2	91 3 2	B1 4 3	A1 5 2		A − M	• • ↕ ↕ ↕ ↕
	CMPB		C1 2 2	D1 3 2	F1 4 3	E1 5 2		B − M	• • ↕ ↕ ↕ ↕
Compare index register	CPX		8C 3 3	9C 4 2	BC 5 3	AC 6 2		$X_H - M, X_L - (M+1)$	• • 8 ↕ 7 •
Test (zero or minus)	TSTA	4D 2 1						A − 00	• • ↕ ↕ R R
	TSTB	5D 2 1						B − 00	• • ↕ ↕ R R
	TST				7D 6 3	6D 7 2		M − 00	• • ↕ ↕ R R
Bit test	BITA		85 2 2	95 3 2	B5 4 3	A5 5 2		A • M	• • ↕ ↕ R •
	BITB		C5 2 2	D6 3 2	F5 4 3	E5 5 2		B • M	• • ↕ ↕ R •
								TEST	
Branch	BRA						20 4 2		• • • • • •
Branch if carry clear	BCC						24 4 2	C = 0	• • • • • •
Branch if carry set	BCS						25 4 2	C = 1	• • • • • •
Branch if overflow clear	BVC						28 4 2	V = 0	• • • • • •
Branch if overflow set	BVS						29 4 2	V = 1	• • • • • •
Branch if equal to zero	BEQ						27 4 2	Z = 1	• • • • • •
Branch if greater or equal to zero	BGE						2C 4 2	N ⊕ V = 0	• • • • • •
Branch if greater than zero	BGT						2E 4 2	Z + (N ⊕ V) = 0	• • • • • •
Branch if less than zero	BLT						2D 4 2	N ⊕ V = 1	• • • • • •
Branch if less than or equal to zero	BLE						2F 4 2	Z + (N ⊕ V) = 1	• • • • • •
Branch if not equal to zero	BNE						26 4 2	Z = 0	• • • • • •
Branch if minus	BMI						2B 4 2	N = 1	• • • • • •
Branch if plus	BPL						2A 4 2	N = 0	• • • • • •
Branch if higher	BHI						22 4 2	C + Z = 0	• • • • • •
Branch if lower or same	BLS						23 4 2	C + Z = 1	• • • • • •

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

Instruction	Mnemonic	Addressing Modes: Implied OP MC PB	Direct OP MC PB	Immediate OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	Condition Reg. 5 4 3 2 1 0 H I N Z V C
Branch to subroutine	BSR						8D 8 2	See Special Operations	• • • • • •
Jump to subroutine	JSR				BD 9 3	AD 8 2			• • • • • •
Jump	JMP				7E 3 3	6E 4 2			• • • • • •
Return from subroutine	RTS	39 5 1							• • • • • •
Return from interrupt	RTI	3B 10 1							Note 10
Software interrupt	SWI	3F 12 1							• S • • • •
Wait for interrupt	WAI	3E 9 1							• 11 • • • •
No operation	NOP	02 2 1						PC + 1 → PC	• • • • • •
Clear	CLRA	4F 2 1						00 → A	• • R S R R
	CLRB	5F 2 1						00 → B	• • R S R R
	CLR				7F 6 3	6F 7 2		00 → M	• • R S R R
Clear carry	CLC	0C 2 1						0 → C	• • • • • R
Clear interrupt mask	CLI	0E 2 1						0 → I	• R • • • •
Clear overflow	CLV	0A 2 1						0 → V	• • • • R •
Set carry	SEC	0D 2 1						1 → C	• • • • • S
Set interrupt mask	SEI	0F 2 1						1 → I	• S • • • •
Set overflow	SEV	0B 2 1						1 → V	• • • • S •

CONDITION CODE SYMBOLS:

- H Half-carry from bit 3;
- I Interrupt mask
- N Negative (sign bit)
- Z Zero (byte)
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- ↕ Test and set if true, cleared otherwise
- • Not Affected

LEGEND:

- OP Operation Code (Hexadecimal):
- MC Number of MPU Cycles;
- PB Number of Program Bytes;
- + Arithmetic Plus;
- − Arithmetic Minus;
- • Boolean AND;
- M_{SP} Contents of memory location pointed to by Stack Pointer;
- + Boolean Inclusive OR;
- ⊕ Boolean Exclusive OR;
- $\overline{M}$ Complement of M;
- → Transfer Into;
- 0 Bit = Zero;
- 00 Byte = Zero;

Note – Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

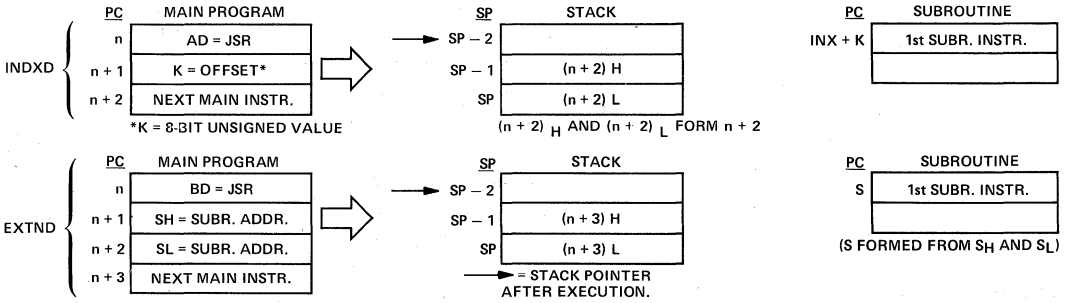
(Bit set if test is true and cleared otherwise)

1	(Bit V)	Test: Result = 10000000?
2	(Bit C)	Test: Result = 00000000?
3	(Bit C)	Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4	(Bit V)	Test: Operand = 10000000 prior to execution?
5	(Bit V)	Test: Operand = 01111111 prior to execution?
6	(Bit V)	Test: Set equal to result of N ⊕ C after shift has occurred.
7	(Bit N)	Test: Sign bit of most significant (MS) byte = 1?
8	(Bit V)	Test: 2's complement overflow from subtraction of MS bytes?
9	(Bit N)	Test: Result less than zero? (Bit 15 = 1)
10	(All)	Load Condition Code Register from Stack. (See Special Operations)
11	(Bit I)	Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
12	(ALL)	Set according to the contents of Accumulator A

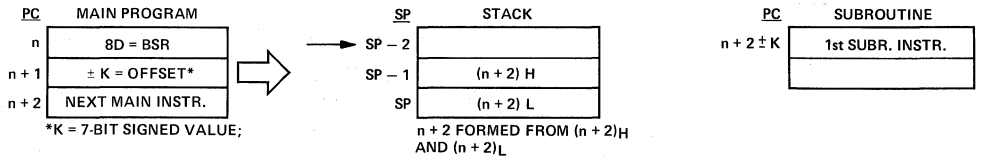
SPECIAL OPERATIONS

JMP, JUMP;

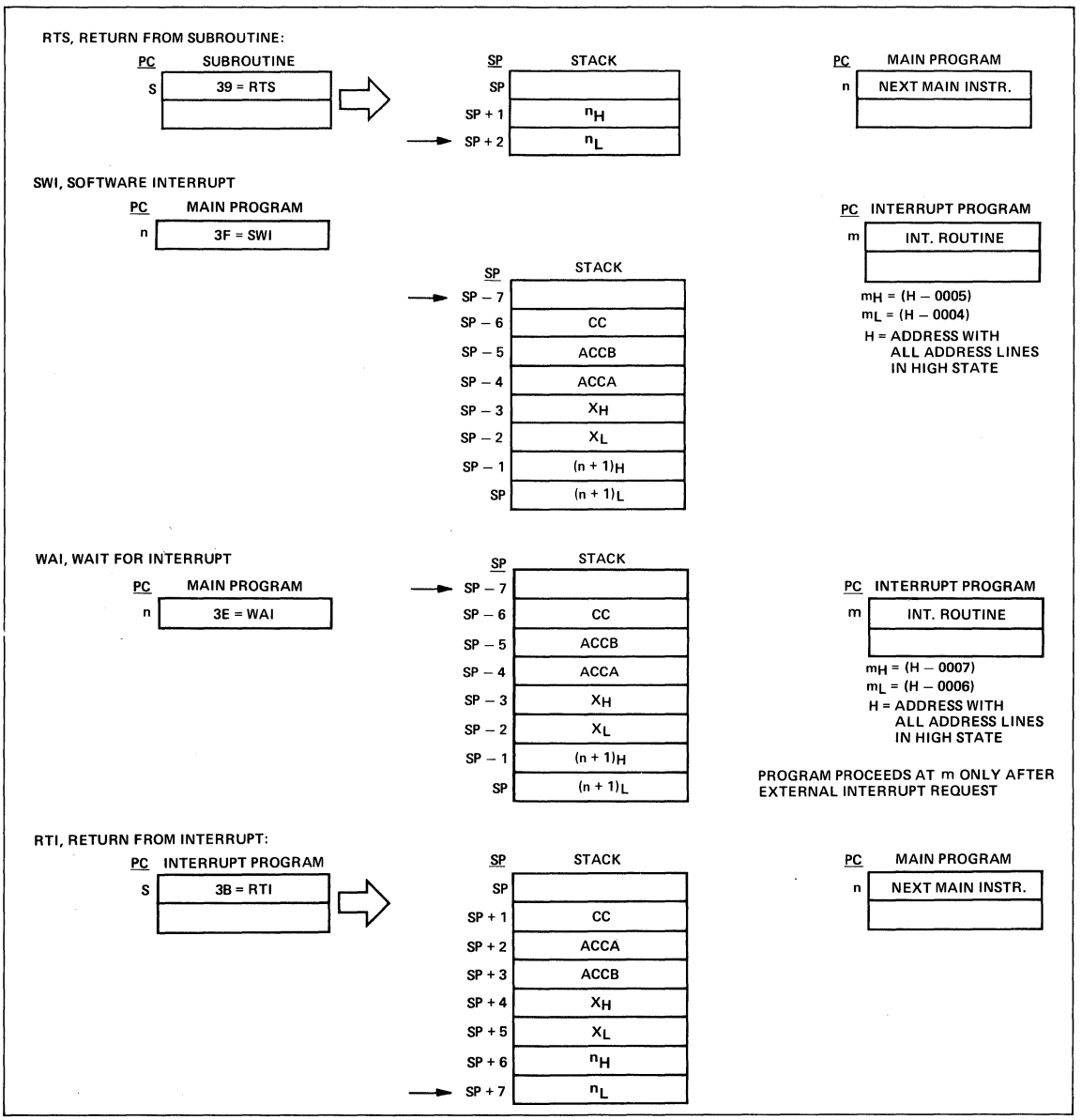
JSR, JUMP TO SUBROUTINE:



BSR, BRANCH TO SUBROUTINE:



SPECIAL OPERATIONS



SYSTEMS OPERATION

To demonstrate the great versatility of the functional building block concept, a typical system configuration is shown. This configuration will demonstrate how easily a basic system may be upgraded and expanded for a number of different applications.

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 10). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

TWO-PHASE CLOCK CIRCUITRY AND TIMING–The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1 MHz. In addition to the two phases, this circuit should also generate an enable signal E, and its complement $\overline{E}$, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing $\phi 2$ and VMA (Valid Memory Address).

CHIP SELECTION AND ADDRESSING–The minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 and A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000–007F
PIA	0	1	2004–2007 (Registers)
ROM	1	1	6000–63FF

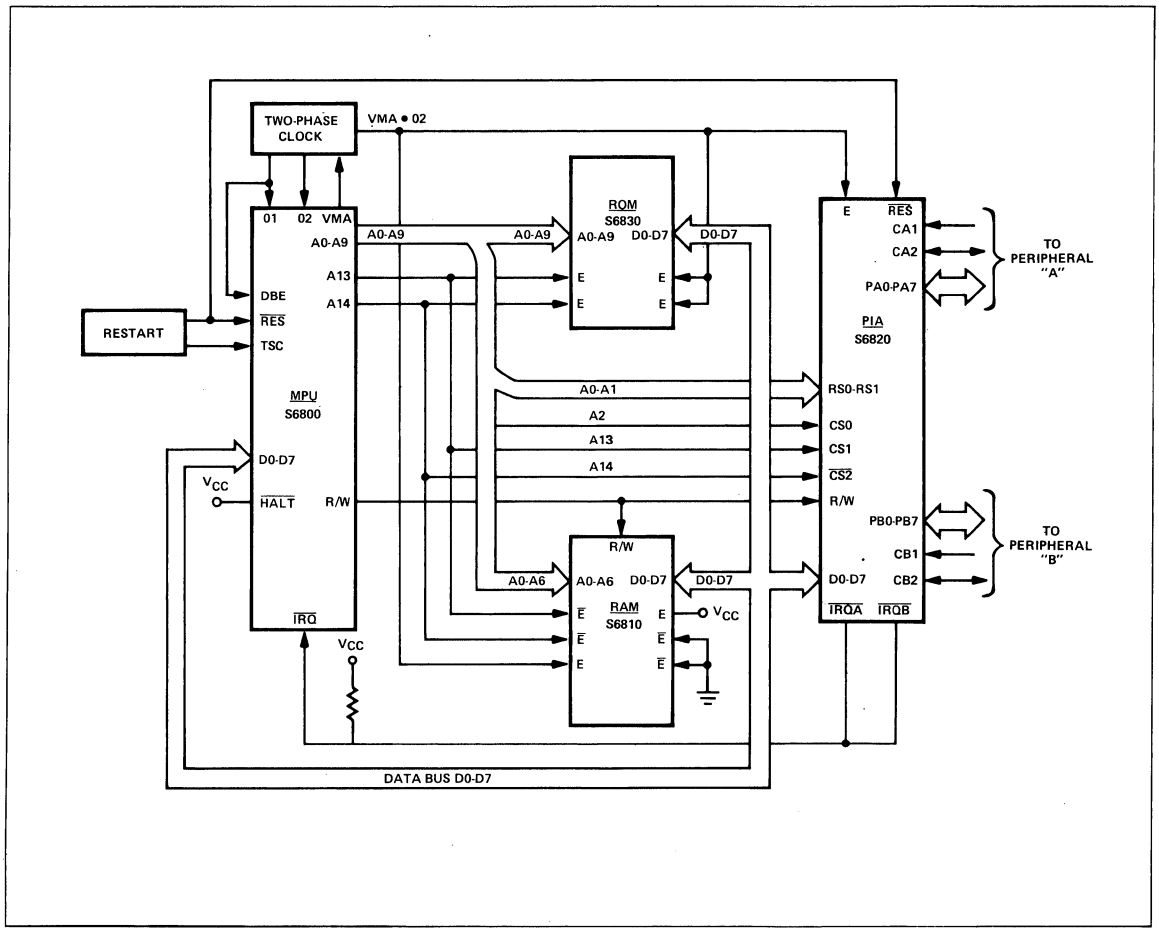
Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

PERIPHERAL CONTROL–All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

RESTART AND NON-MASKABLE INTERRUPT–Since this basic system does not have a nonvolatile RAM, special circuitry to handle loss of power using NMI is not required. Circuitry is, however, required to insure proper initialization of the MPU when power is turned on. This circuit should insure that the Restart signal is held low for eight $\phi 1$ clock cycles after the V_{CC} power supply reaches a voltage of approximately 4.75 volts DC. Also, in order to insure that a PIA or ACIA is not inadvertently selected during the power-on sequence, Three-State Control (TSC) should be held high until the positive transition of Restart.

$\overline{HALT}$–The $\overline{Halt}$ line is tied to V_{CC} and will automatically place the MPU in the run state when power is turned on. This signal may be used to halt the MPU if a switch is used to tie the line to ground for HALT and to V_{CC} for RUN.

FIGURE 10 – MINIMUM SYSTEM CONFIGURATION

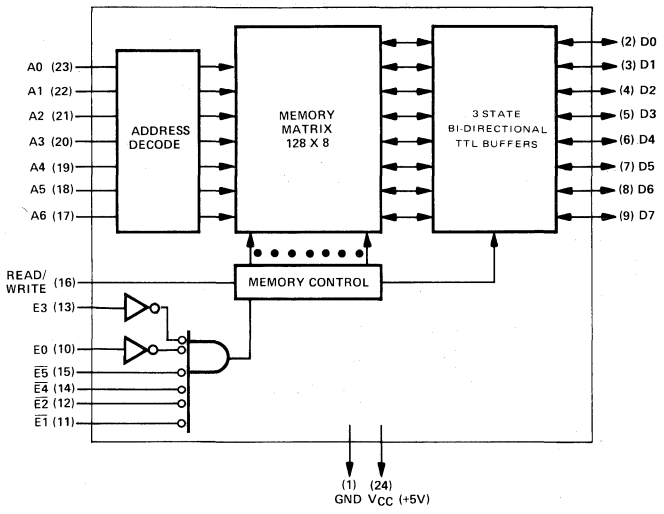


S6810

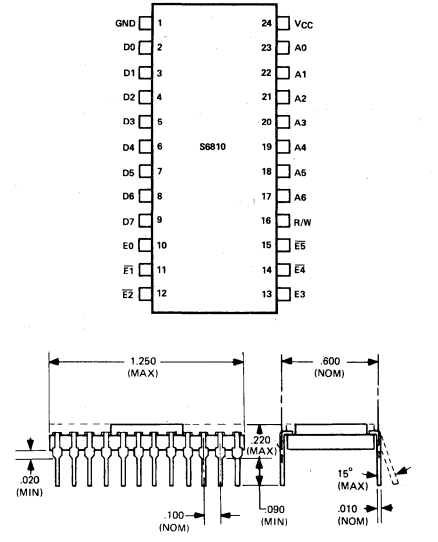
128 X 8 STATIC
READ/WRITE MEMORY

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W - see Sec. 1)

FEATURES

- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bi-Directional Three-State Data Input/Output
- Six Chip Enable Inputs (Four Active Low, Two Active High)
- Single 5-Volt Power Supply
- TTL Compatible
- Maximum Access Time = 1.0μs for S6810
  575 ns for S6810-1

FUNCTIONAL DESCRIPTION

The S6810 is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Microprocessor. Interfacing to the S6810 consists of an 8 Bit Bi-directional Data Bus, Seven Address Lines, a single Read/Write Control line, and six Chip Enable lines, four negative and two positive.

For ease of use, the S6810 is a totally static memory requiring no clocks or cell refresh. The S6810 is fabricated with N channel silicon gate technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0 Volt ± 5%; T_A = 0° C to +70° C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Condition
Input High Voltage(NormalOperatingLevels)	V_{IH}	2.4	–	5.25	V	
Input Low Voltage(NormalOperating Levels)	V_{IL}	-0.3	–	0.4	V	
Input Current (A_n, R/W, E_n, $\overline{E}_n$) (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μA	
Input High Threshold Voltage	V_{IHT}	2.0	–	–	V	
Input Low Threshold Voltage	V_{ILT}	–	–	0.8	V	
Output High Voltage (I_{OH} = -100 μA)	V_{OH}	2.4	–	–	V	
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	V	
Output Leakage Current (D0 – D7) (V_O = 2.4 V, E = 0.4 V, $\overline{E}$ = 2.4 V)	I_{LIH}	–	–	10	μA	
Output Leakage Current (D0 – D7) (V_O = 0.4 V, E = 0.4 V, $\overline{E}$ = 2.4 V)	I_{LOL}	–	–	10	μA	
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mA	
Input Capacitance	C_{IN}	–	–	7.5	pF	f = 1.0MHz, T_A = 25°C
Output Capacitance	C_{OUT}	–	–	15	pF	

AC (DYNAMIC) CHARACTERISTICS

(V_{CC} = 5.0 Volt ∓ 5%, T_A = 0°C to + 70°C)

Characteristic		Symbol	Min.	Max.	Unit
Address Setup Time		t_{AS}	30	–	ns
Address Hold Time		t_{AH}	0	–	ns
Chip Enable Pulse Width	S6810	t_{CS}	800	–	ns
	S6810-1		400		

READ CYCLE
(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic		Symbol	Min.	Max.	Unit
Read Cycle Time	S6810	$t_{cyc(R)}$	1000	–	ns
	S6810-1		575	–	ns
Output Enable Delay Time	S6810	t_{ED}	–	400	ns
	S6810-1		–	300	ns
Output Disable Delay Time	S6810	t_{DD}	10	200	ns
	S6810-1		10	150	ns
Read Access Time	S6810	t_{acc}	–	1000	ns
	S6810-1		–	575	ns

WRITE CYCLE
(All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic		Symbol	Min.	Max.	Unit
Write Cycle Time	S6810	$t_{cyc(W)}$	1000	–	ns
	S6810-1		500	–	ns
Write Pulse Width	S6810	t_{WP}	800	–	ns
	S6810-1		400	–	ns
Write Pulse Hold Time	S6810	t_{WH}	1000	–	ns
	S6810-1		500	–	ns
Data Setup Time	S6810	t_{DS}	500	–	ns
	S6810-1		300	–	ns
Data Hold Time	S6810	t_{DH}	0	–	ns
	S6810-1		0		

TIMING CHARACTERISTICS

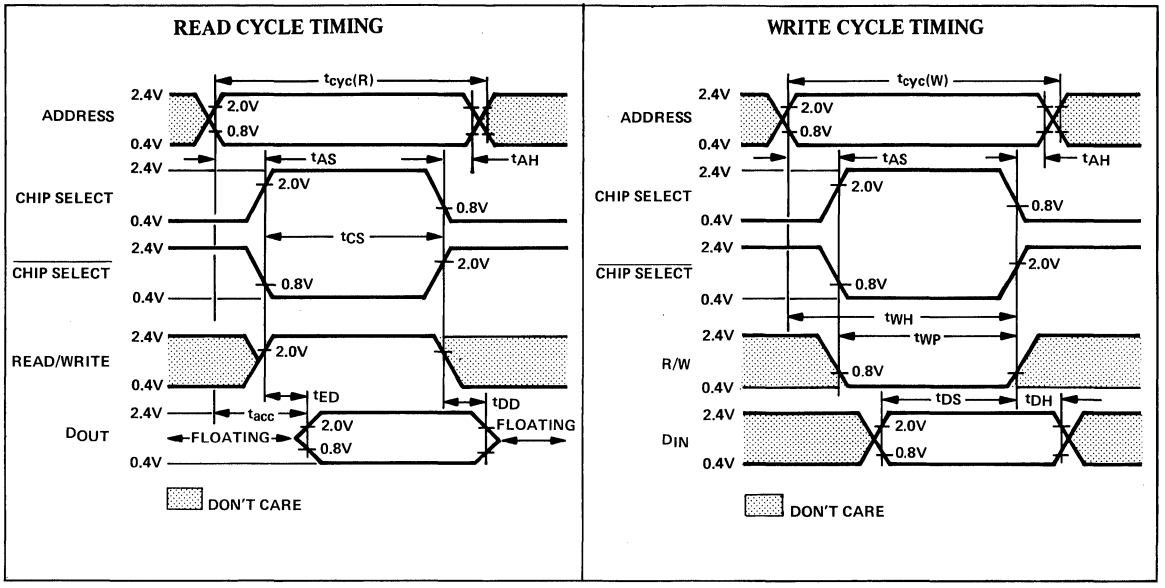
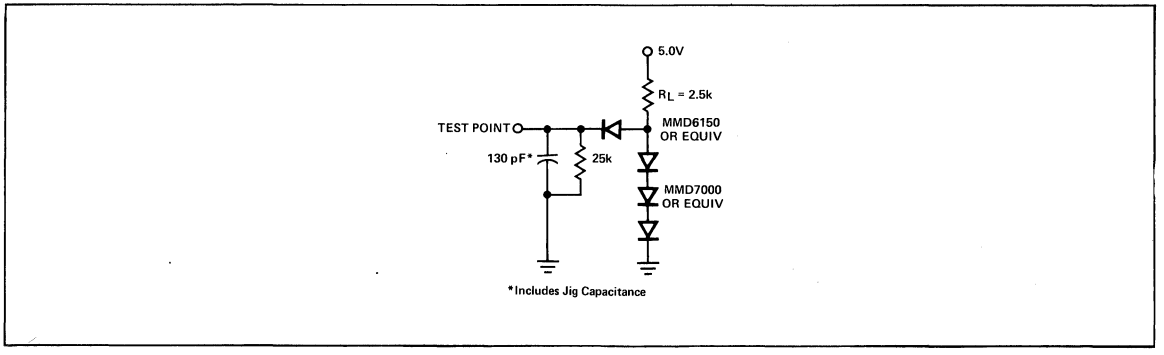


FIGURE 1 – AC TEST LOAD

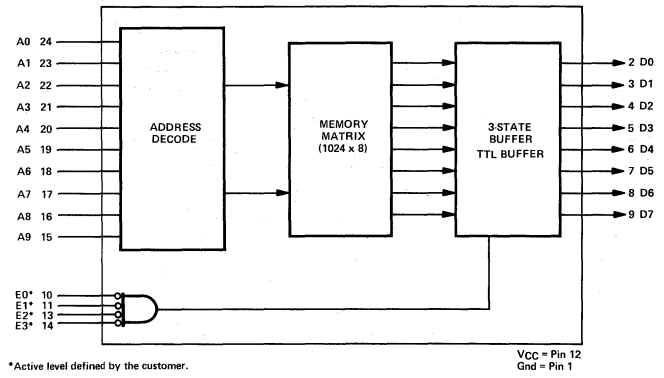


S6830

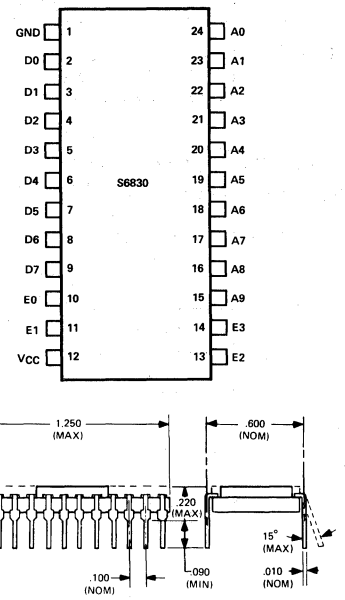
1024 X 8
READ ONLY MEMORY

AMERICAN MICROSYSTEMS, INC.

ADVANCE PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W - see Sec. 1)

FEATURES

- Organized as 1024-Bytes of 8 Bits
- Static Operation
- Three-State Data Output
- Four Chip Enable Inputs (Mask Programmable)
- Single 5-Volt Power Supply
- TTL Compatible Input/Output
- Maximum Access Time = 575 ns

FUNCTIONAL DESCRIPTION

The S6830 is a mask programmable read only memory organized 1024 words x 8 bits for application in byte organized systems. The S6830 is totally bus compatible with the S6800 microprocessor. Interfacing to the S6830 consists of an 8 bit three-state data bus, four mask programmable chip selects and ten address lines.

The S6830 is a totally static memory requiring no clocks. Access time is compatible with maximum data rates in a S6800 microprocessor system. The device operates from a single +5 volt power supply and is fabricated with N channel silicon gate technology.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{in}	−0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	−55 to +150°C

NOTE: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC (STATIC) CHARACTERISTICS
(V_{CC} = +5 Volt ± 5%; T_A = 0°C to +70°C)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage (Norm. Op. Levels)	V_{IH}	2.4	5.25	Vdc
Input Low Voltage (Norm. Op. Levels)	V_{IL}	−0.3	0.4	Vdc
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	2.5	μAdc
Input High Threshold Voltage	V_{IHT}	2.0	–	Vdc
Input Low Threshold Voltage	V_{ILT}	–	0.65	Vdc
Output High Voltage (I_{OH} = −100 μA)	V_{OH}	2.4	–	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	0.45	Vdc
Output Leakage Current (V_{OH} = 2.4 V, $\overline{E}$ = 0.4 V, E = 2.4 V)	I_{LOH}	–	10	μAdc
Output Leakage Current (V_{OH} = 0.4 V, $\overline{E}$ = 0.4 V, E = 2.4 V)	I_{LOL}	–	10	μAdc
Supply Current (V_{CC} = 5.25V, T_A = 0°C)	I_{CC}	–	130	mAdc

CAPACITANCE

Characteristic	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Capacitance	C_{in}	–	–	7.5	pF	f = 1.0 MHz
Output Capacitance	C_{out}	–	–	15	pF	T_A = 25°C

AC (DYNAMIC) CHARACTERISTICS

V_{CC} = +5 Volt ± 5%; T_A = 0°C to +70°C

READ CYCLE (All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	Min.	Max.	Unit
Read Cycle Time	t_{cyc} (R)	575	–	ns
Output Enable Delay Time	t_{ED}	–	300	ns
Output Disable Delay Time	t_{DD}	10	150	ns
Read Access Time	t_{acc}	–	575	ns

READ CYCLE TIMING

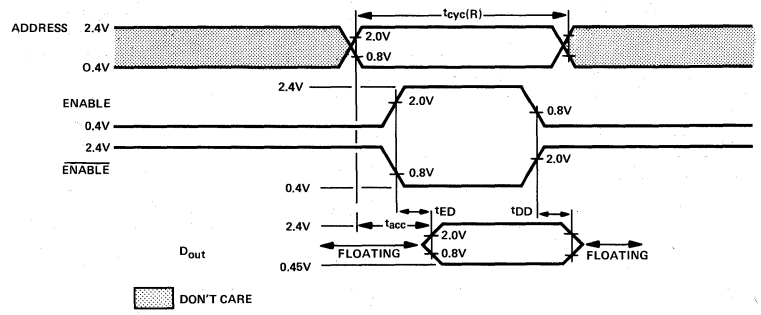
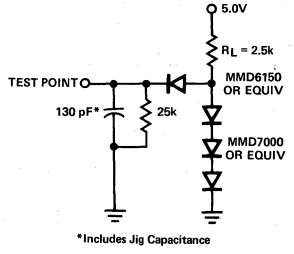


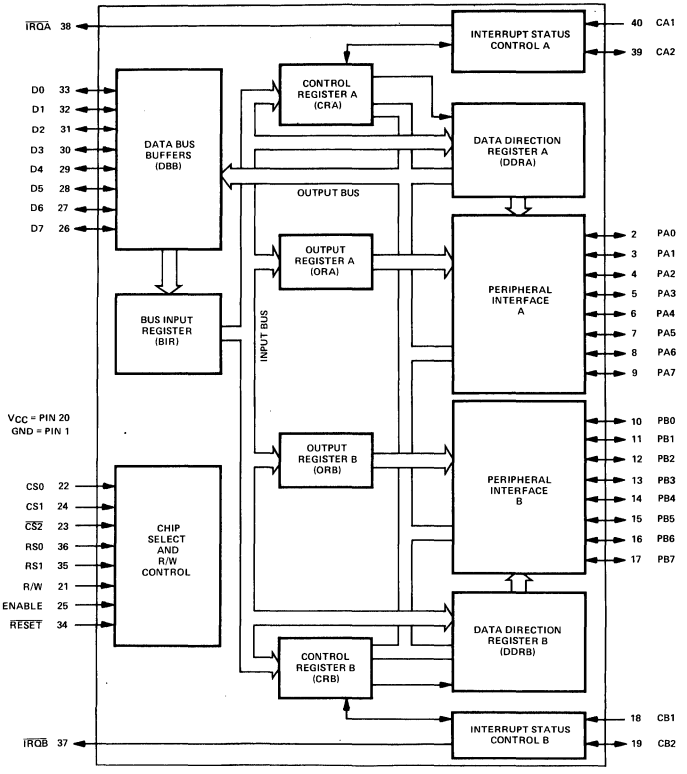
FIGURE 1 – AC TEST LOAD



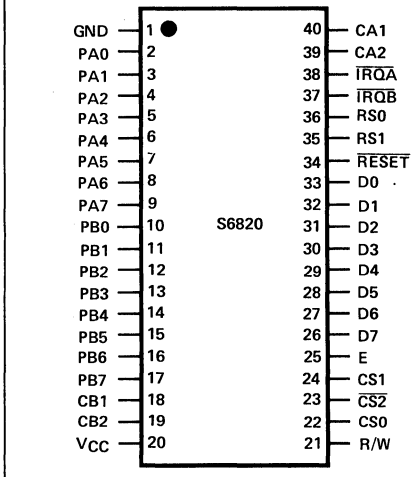
S6820

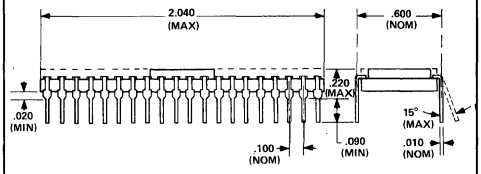
PERIPHERAL INTERFACE
ADAPTER (PIA)

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM





PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

FEATURES

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

FUNCTIONAL DESCRIPTION

The S6820 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the S6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

The PIA interfaces to the S6800 MPU with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S6800 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{in}	-0.3 to +7.0V
Operating Temperature Range T_A	0 to +70°C
Storage Temperature Range T_{stg}	-55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 25°C unless otherwise noted.)

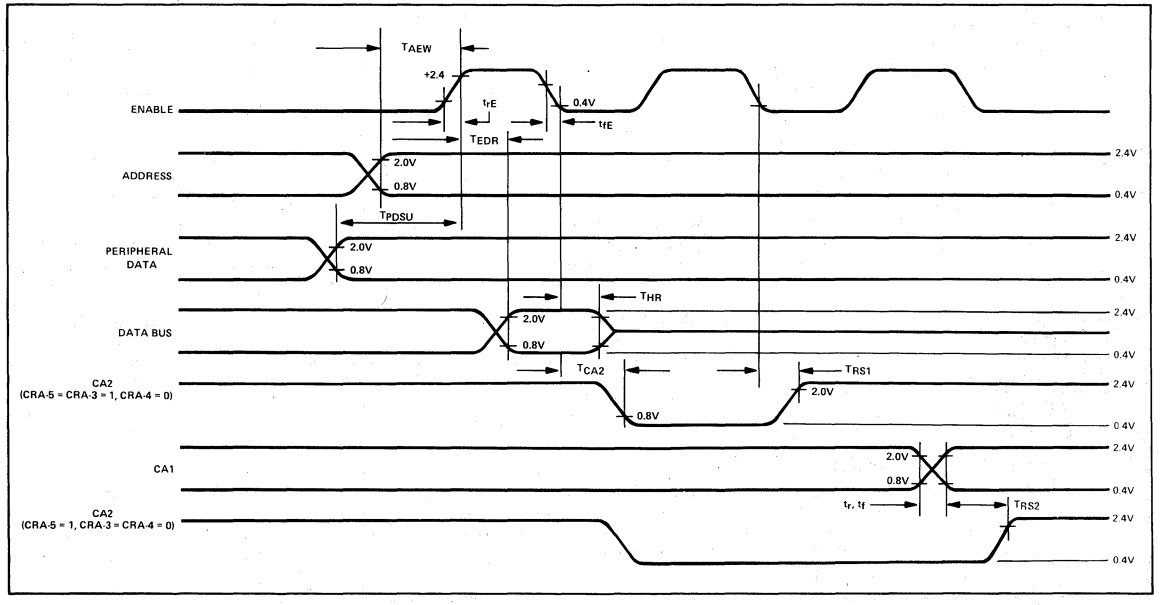
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.4	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	-0.3	–	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	V_{IHT}	+2.0	–	–	Vdc
Input Low Threshold Voltage All Inputs Except Enable	V_{ILT}	–	–	+0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.0 Vdc) R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, $\overline{\text{CS2}}$, CA1, CB1, Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7, PB0-PB7, CB2	I_{TSI}	–	2.0	10	μAdc
Input High Current PA0-PA7, CA2 (V_{IH} = 2.4 Vdc)	I_{IH}	100	250	–	μAdc
Input Low Current PA0-PA7, CA2 (V_{IL} = 0.4 Vdc)	I_{IL}	–	1.0	1.6	mAdc
Output High Voltage (V_{CC} = min, I_{Load} = -100 μAdc, Enable Pulse Width < 25 μs)	V_{OH}	+2.4	–	–	Vdc
Output Low Voltage (V_{CC} = min, I_{Load} = 1.6 mAdc)	V_{OL}	–	–	+0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 Vdc) (V_{OH} = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base) PB0-PB7, CB2	I_{OH}	 -100 -1.0	 -1000 -2.5	 – –	 μAdc mAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	I_{OL}	1.6	–	–	mAdc
Output Leakage Current (Off State) $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$	I_{off}	–	1.0	10	μAdc
Power Dissipation	P_D	–	300	600	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7, PA0-PA7, PB0-PB7, CA2, CB2 R/W, $\overline{\text{Reset}}$, RS0, RS1, CS0, CS1, $\overline{\text{CS2}}$, CA1, CB1 Enable	C_{in}	 – – –	 – – –	 10 7.0 20	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	10	pF

AC (DYNAMIC) CHARACTERISTICS Loading = 30 pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
= 130 pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$

READ TIMING CHARACTERISTICS (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Delay Time, Enable positive transition to Data valid on bus	T_{EDR}	–	–	395	ns
Peripheral Data Setup Time	T_{PDSU}	300	–	–	ns
Data Bus Hold Time	T_{HR}	10	–	–	ns
Delay Time, Enable negative transition to CA2 negative transition	T_{CA2}	–	–	1.0	μs
Delay Time, Enable negative transition to CA2 positive transition	T_{RS1}	–	–	1.0	μs
Rise and Fall Time for CA1 and CA2 input signals	t_r, t_f	–	–	1.0	μs
Delay Time from CA1 active transition to CA2 positive transition	T_{RS2}	–	–	2.0	μs
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	–	–	25	μs

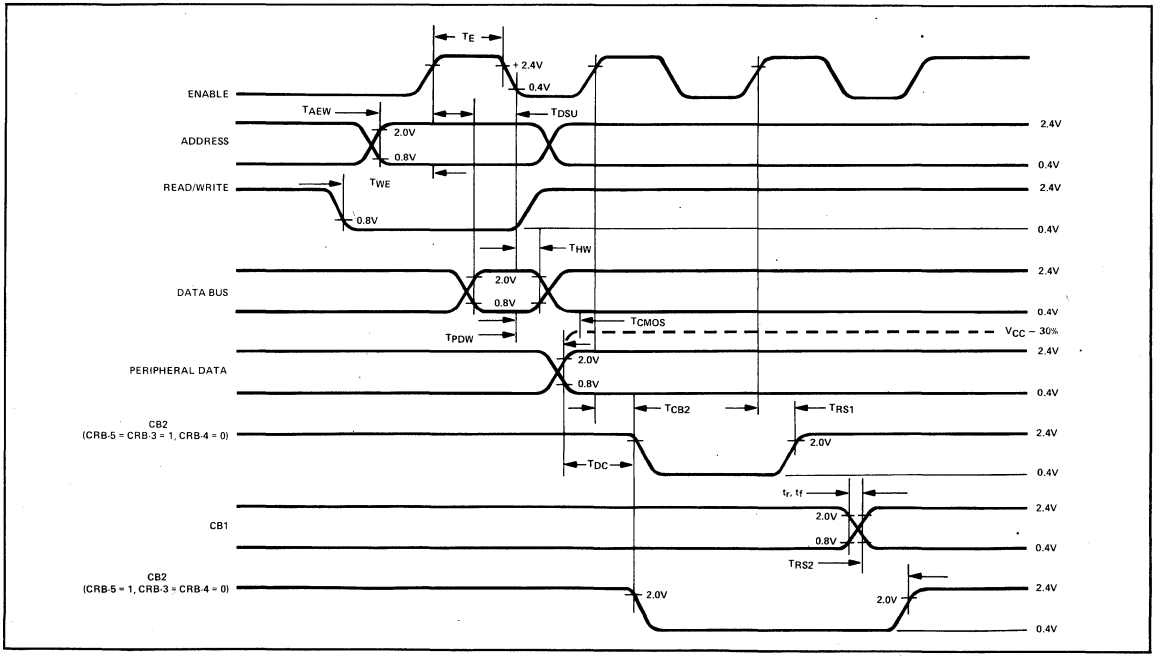
FIGURE 1 – READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	T_E	0.470	–	25	μs
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	–	–	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	–	–	ns
Data Bus Hold Time.	T_{HW}	10	–	–	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	–	–	1.0	μs
Delay Time, Enable negative transition to Peripheral Data valid, CMOS (V_{CC} – 30%) PA0-PA7, CA2	T_{CMOS}	–	–	2.0	μs
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	–	–	1.0	μs
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	–	1.5	μs
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	–	–	1.0	μs
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	–	–	1.0	μs
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	–	–	2.0	μs

FIGURE 2 – WRITE TIMING CHARACTERISTICS



INTERFACE DESCRIPTION

MPU/PIA INTERFACE

Pin	Label	Function
(33) (32) (31) (30) (29) (28) (27) (26)	D0 D1 D2 D3 D4 D5 D6 D7	**Bi-Directional Data** – The bi-directional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.
(25)	E	**Enable** – The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the S6800 $\phi 2$ Clock. The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1, and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.
(21)	R/W	**Read/Write** – This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.
(34)	$\overline{\text{RESET}}$	**$\overline{\text{Reset}}$** – The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.
(22) (24) (23)	CS0 CS1 $\overline{\text{CS2}}$	**Chip Select** – These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.
(36) (35)	RS0 RS1	**PIA Register Select** – The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read. The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.

(38) $\overline{IRQA}$
(37) $\overline{IRQB}$

Interrupt Request – The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open source" (no load device on the chip) and are capable of sinking a current of 1.6 mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU is accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.

PIA/PERIPHERAL INTERFACE

Pin	Label	Function
(2)	PA0	**Section A Peripheral Data** – Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.
(3)	PA1	
(4)	PA2	
(5)	PA3	
(6)	PA4	
(7)	PA5	
(8)	PA6	
(9)	PA7	The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low". Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.
(10)	PB0	**Section B Peripheral Data** – The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high". As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.
(11)	PB1	
(12)	PB2	
(13)	PB3	
(14)	PB4	
(15)	PB5	
(16)	PB6	
(17)	PB7	

Pin	Label	Function
(40) (18)	CA1 CB1	**Interrupt Input** – Peripheral Input lines CA1 and CB1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.
(39)	CA2	**Peripheral Control** – The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.
(19)	CB2	**Peripheral Control** – Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.
(1)	GND	**Ground**
(20)	V_{CC}	+5 Volts ± 5%

APPLICATION INFORMATION

INITIALIZATION

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

REGISTER ADDRESSING

There are six locations within the PIA accessible to the MPU data bus; two Peripheral Registers, two Data Direction Registers, and two Control Registers, Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

TABLE 1 – INTERNAL ADDRESSING

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

DATA DIRECTION REGISTERS (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. All Data Direction Register bits set at "0" configure the corresponding peripheral data line as an input; all "1s" result in an output.

CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1 and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

TABLE 2 – CONTROL WORD FORMAT

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Data Direction Access Control Bit (CRA-2 and CRB-2) – Bit 2 in each Control register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1) – The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

TABLE 3 – CONTROL OF INTERRUPT INPUTS CA1 AND CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled – $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled – $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

NOTES: 1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-0 (CRB-0).

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5) – Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

TABLE 4 – CONTROL OF CA2 AND CB2 AS INTERRUPT INPUTS
CRA5 (CRB5) is low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled – $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled – $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

NOTES: 1. ↑ indicates positive transition (low to high)
2. ↓ indicates negative transition (high to low)
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-3 (CRB-3).

TABLE 5 – CONTROL OF CA2 AS AN OUTPUT
CRA-5 is high

CRA-5	CRA-4	CRA-3	CA2	
			Cleared	Set
1	0	0	Low on negative transition of E after an MPU Read "A" Data operation.	High on an active transition of the CA1 signal
1	0	1	Low immediately after an MPU Read "A" Data operation.	High on the negative edge of the next "E" pulse.
1	1	0	Low when CRA-3 goes low as a result of an MPU Write in Control Register "A".	Always low as long as CRA-3 is low.
1	1	1	Always high as long as CRA-3 is high	High when CRA-3 goes high as a result of a Write in Control Register "A".

TABLE 6 – CONTROL OF CB2 AS AN OUTPUT
CRB-5 is high

CRB-5	CRB-4	CRB-3	CB2	
			Cleared	Set
1	0	0	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High when the interrupt flag bit CRB-7 is set by an active transition of the CB1 signal
1	0	1	Low on the positive transition of the first E pulse following an MPU Write "B" Data Register operation.	High on the positive transition of the next "E" pulse.
1	1	0	Low when CRB-3 goes low as a result of an MPU Write in Control Register "B".	Always low as long as CRB-3 is low. Will go high on an MPU Write in Control Register "B" that changes CRB-3 to "one".
1	1	1	Always high as long as CRB-3 is high. Will be cleared when an MPU Write Control Register "B" results in clearing CRB-3 to "zero".	High when CRB-3 goes high as a result of an MPU write into control register "B".

Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7) – The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Status lines when those lines are programmed to be interrupt inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

BASIC SYSTEM CONFIGURATION

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 3). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

TWO-PHASE CLOCK CIRCUITRY AND TIMING—The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1 MHz. In addition to the two phases, this circuit should also generate an enable Signal E, and its complement E, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing $\phi 2$ and VMA (Valid Memory Address).

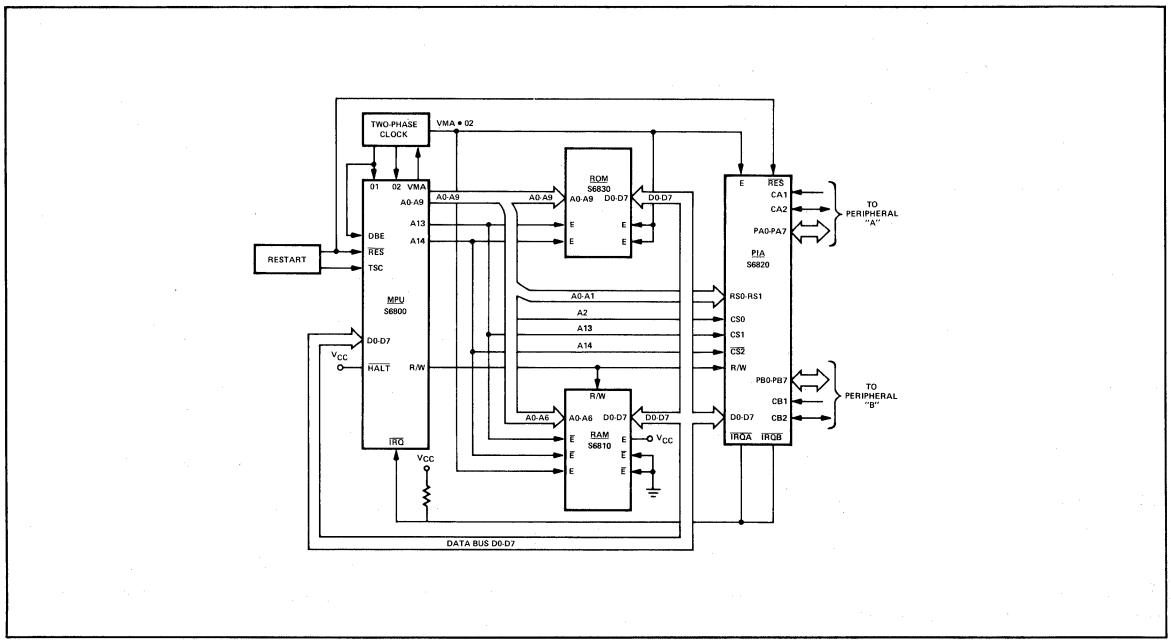
CHIP SELECTION AND ADDRESSING—The Minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000—007F
PIA	0	1	2004—2007 (Registers)
ROM	1	1	6000—63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

PERIPHERAL CONTROL—All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

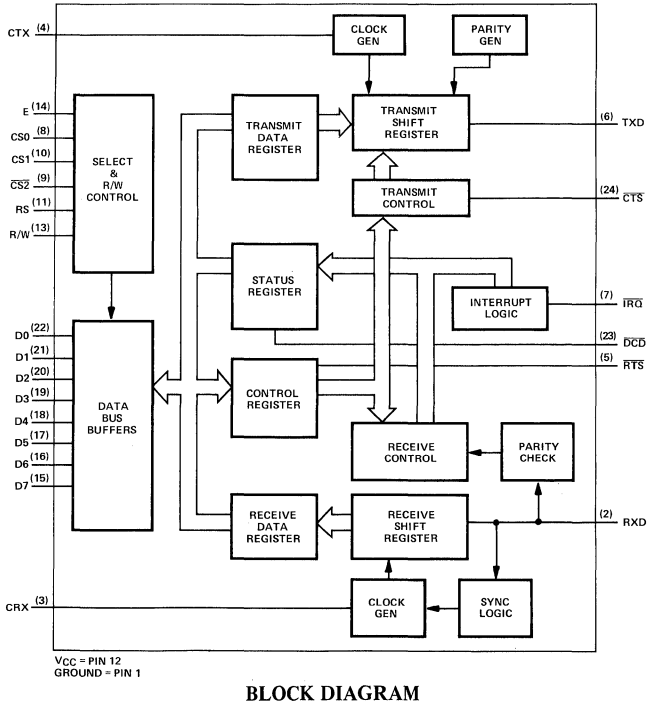
FIGURE 3. MINIMUM SYSTEM IMPLEMENTATION



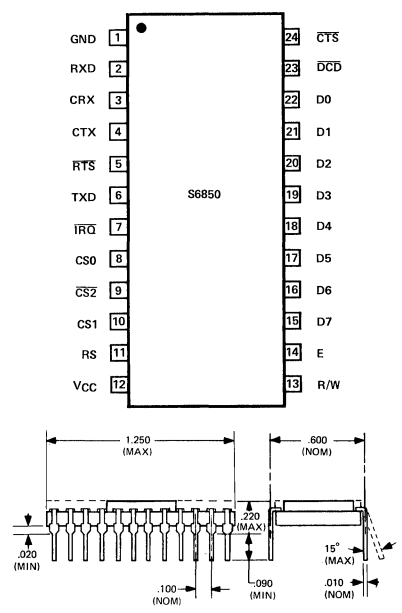
S6850

ASYNCHRONOUS COMMUNICATION
INTERFACE ADAPTER (ACIA)

ADVANCE PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

(Available in Pkgs. 2L, 1W - see Sec. 1)

FEATURES

- 8 Bit Bidirectional Data Bus for Communication with MPU.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered Receiver and Transmitter
- One or two stop bit operation.
- Eight and nine-bit transmission with optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional ÷1, ÷16, and ÷64 clock modes.
- Up to 500,000 bps transmission.

FUNCTIONAL DESCRIPTION

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	−0.3 to +7.0V	Operating Temperature Range T_A	0 to +70°C
Input Voltage V_{in}	−0.3 to +7.0V	Storage Temperature Range T_{stg}	−55 to +150°C

NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (STATIC) CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input High Voltage (Normal Operating Levels)	V_{IH}	+2.4	–	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)	V_{IL}	−0.3	–	+0.4	Vdc
Input High Threshold Voltage All Inputs Except Enable	V_{IHT}	+2.0	–	–	Vdc
Input Low Threshold Voltage All Inputs Except Enable	V_{ILT}	–	–	+0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.0 Vdc) R/W, RS, CS0, CS1, $\overline{CS2}$, Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max) D0-D7,	I_{TSI}	–	2.0	10	μAdc
Output High Voltage (I_{Load} = −100 μAdc, Enable Pulse Width < 25 μs)	V_{OH}	+2.4	–	–	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc) Enable Pulse Width < 25 μs	V_{OL}	–	–	+0.4	Vdc
Output Leakage Current (Off State) $\overline{IRQ}$	I_{LOH}	–	1.0	10	μAdc
Power Dissipation	P_D	–	300	525	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz) D0-D7, $\overline{CTS}$, $\overline{DCD}$ R/W, RS, CS0, CS1, $\overline{CS2}$, RXD Enable, CTX, CRX	C_{in}	 – – –	 – – –	 10 7.0 20	pF
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	10	pF

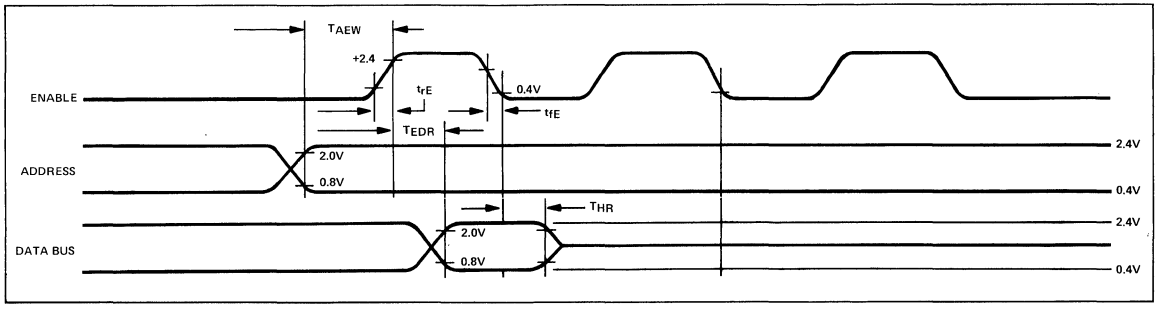
AC (DYNAMIC) CHARACTERISTICS

Loading = 130 pF and one TTL load for D0-D7 = 20pF and 1 TTL load for $\overline{RTS}$ and TXD = 100pF and 3KΩ to V_{CC} for $\overline{IRQ}$.

READ TIMING CHARACTERISTICS (Figure 1)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Setup Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Setup Time, Enable positive transition to Data valid on bus	T_{EDR}	–	–	395	ns
Data Bus Hold Time	T_{HR}	10	–	–	ns
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	–	–	25	μs

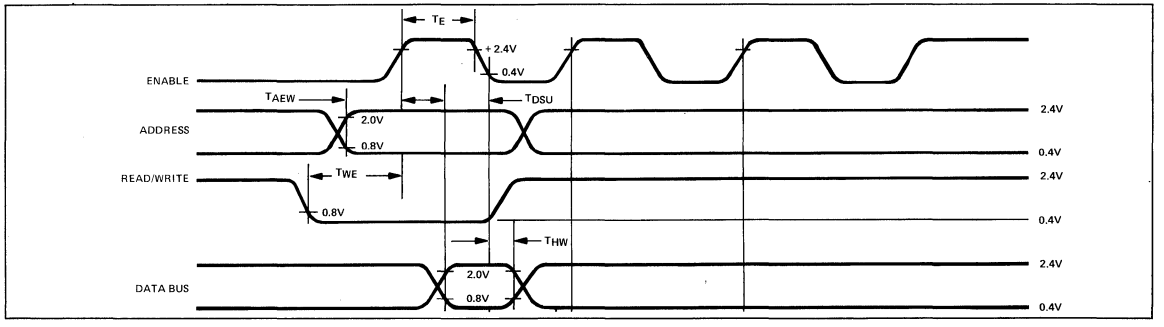
FIGURE 1 – READ TIMING CHARACTERISTICS



WRITE TIMING CHARACTERISTICS (Figure 2)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Enable Pulse Width	T_E	0.470	–	25	μs
Setup Time, Address valid to Enable positive transition	T_{AEW}	180	–	–	ns
Setup Time, Data valid to Enable netative transition	T_{DSU}	300	–	–	ns
Setup time, Read/Write negative transition to Enable positive transition	T_{WE}	130	–	–	ns
Data Bus Hold Time	T_{HW}	10	–	–	ns

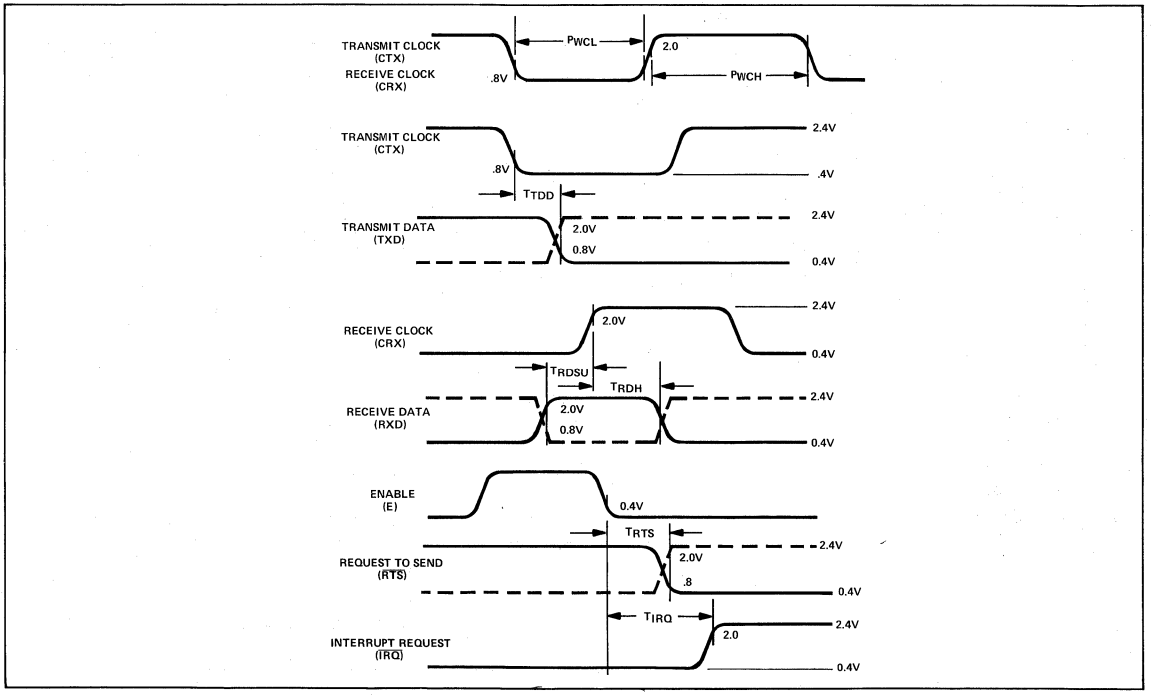
FIGURE 2 – WRITE TIMING CHARACTERISTICS



TRANSMIT/RECEIVE CHARACTERISTICS (Figure 3)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Clock Frequency ÷ 1 mode ÷ 16 mode ÷ 64 mode				 500 800 800	 KHz KHz KHz
Clock Pulse Width, Low State	PWCL	600			nsec
Clock Pulse Width, High State	PWCH	600			nsec
Delay Time, Transmit Clock to Data Out	T_{TDD}			1.0	μsec
Set up Time, Receive Data	T_{RDSU}	500			nsec
Hold Time, Receive Data	T_{RDH}	500			nsec
Delay Time, Enable to $\overline{IRQ}$ Reset	T_{IRQ}			1.2	μsec
Delay Time, Enable to $\overline{RTS}$	T_{RTS}			1.0	μsec

FIGURE 3 – TRANSMIT/RECEIVE TIMING



MPU/ACIA INTERFACE

Pin	Label	FUNCTION
(22) (21) (20) (19) (18) (17) (16) (15)	D0 D1 D2 D3 D4 D5 D6 D7	**ACIA BI-DIRECTIONAL DATA LINES**–The bi-directional data lines (D0-D7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is selected for a read operation.
(14)	E	**ACIA ENABLE SIGNAL**–The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 $\phi 2$ clock.
(13)	R/W	**READ/WRITE CONTROL SIGNAL**–The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read only or Write only registers within the ACIA.
(8) (10) (9)	CS0 CS1 $\overline{CS2}$	**CHIP SELECT SIGNALS**–These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write, and Register Select.
(11)	RS	**REGISTER SELECT SIGNAL**–The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{IRQ}$	**INTERRUPT REQUEST SIGNAL**–Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

ACIA/MODEM OR PERIPHERAL INTERFACE

Pin	Label	FUNCTION
(4)	CTX	**TRANSMIT CLOCK**–The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.

Pin	Label	FUNCTION
(3)	CRX	**RECEIVE CLOCK**–The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	**RECEIVED DATA**–The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRZ(Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500 Kbps when external synchronization is utilized.
(6)	TXD	**TRANSMIT DATA**–The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{CTS}$	**CLEAR-TO-SEND**–This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{RTS}$	**REQUEST-TO-SEND**–The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{DCD}$	**DATA CARRIER DETECTED**–This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	V_{CC}	**+5 volts ± 5%**
(1)	GND	**GROUND**

APPLICATION INFORMATION

INTERNAL REGISTERS–The ACIA has four internal registers utilized for status, control, receiving data, and transmitting data. The register addressing by the R/W and RS lines and the bit definitions for each register are shown in Figure 4.

FIGURE 4 – DEFINITION OF ACIA REGISTERS

	BUFFER ADDRESS			
	RS • $\overline{R/W}$	**RS • R/W**	**$\overline{RS}$ • $\overline{R/W}$**	**$\overline{RS}$ • R/W**
Data Bus Line Number	Transmit Data Register	Receiver Date Register	Control Register	Status Register
	(Write Only)	(Read Only)	(Write Only)	(Read Only)
0	Data Bit 0*	Data Bit 0*	Clk. Divide Sel. (CR0)	Rx Data Reg. Full (RDRF)
1	Data Bit 1	Data Bit 1	Clk. Divide Sel. (CR1)	Tx Data Reg. Empty (TDRE)
2	Data Bit 2	Data Bit 2	Word Sel. 1 (CR2)	Data Carrier Det. loss ($\overline{DCD}$)
3	Data Bit 3	Data Bit 3	Word Sel. 2 (CR3)	Clear-to-Send (CTS)
4	Data Bit 4	Data Bit 4	Word Sel. 3 (CR4)	Framing Error (FE)
5	Data Bit 5	Data Bit 5	Tx Control 1 (CR5)	Overrun (OVRN)
6	Data Bit 6	Data Bit 6	Tx Control 2 (CR6)	Parity Error (PE)
7	Data Bit 7***	Data Bit 7**	Rx Interrupt Enable (CR7)	Interrupt Request (IRQ)

Notes:
* Leading bit = LSB = Bit 0
** Unused data bits in received character will be "0's."
*** Unused data bits for transmission are "don't care's."

ACIA STATUS REGISTER–Information on the status of the ACIA is available to the MPU by reading the ACIA Status Register. This Read Only register is selected when RS is low and R/W is high. Information stored in this register indicates the status of: transmitting data register, the receiving data register and error status and the modem status inputs of the ACIA.

Receiver Data Register Full (RDRF) [Bit 0] – Receiver Data Register Full indicates that received data has been transferred to the Receiver Data Register. RDRF is cleared after an MPU read of the Receiver Data Register or by a Master Reset. The cleared or empty state indicates that the contents of the Receiver Data Register are not current. Data Carrier Detect being high also causes RDRF to indicate empty.

Transmit Data Register Empty (TDRE) [Bit 1]–The Transmit Data Register Empty bit being set high indicates that the Transmit Data Register contents have been transferred and that new data may be entered. The low state indicates that the register is full and that transmission of a new character has not begun since the last write data command.

Data Carrier Detect ($\overline{\text{DCD}}$) [Bit 2] – The Data Carrier Detect bit will be high when the $\overline{\text{DCD}}$ input from a modem has gone high to indicate that a carrier is not present. This bit going high causes an Interrupt Request to be generated if the Receiver Interrupt Enable (RIE) is set. It remains high until the interrupt is cleared by reading the Status Register and the data register or a Master Reset occurs. If the $\overline{\text{DCD}}$ input remains high after Read Status and Read Data or Master Reset have occurred, the $\overline{\text{DCD}}$ Status bit remains high and will follow the $\overline{\text{DCD}}$ input.

Clear-to-Send ($\overline{\text{CTS}}$) [Bit 3] – The Clear-to-Send bit indicates the state of the Clear-to-Send input from a modem. A low $\overline{\text{CTS}}$ indicates that there is a Clear-to-Send from the modem. In the high state, the Transmit Data Register Empty bit is inhibited and the Clear-to-Send status bit will be high. Master Reset does not affect the Clear-to-Send status bit.

Framing Error (FE) [Bit 4] – Framing error indicates that the received character is improperly framed by the start and stop bit and is detected by the absence of the 1st stop bit. This error indicates a synchronization error, faulty transmission, or a break condition. The framing error flag is set or reset during the receiver data transfer time. Therefore, this error indicator is present throughout the time that the associated character is available.

Receiver Overrun (OVRN) [Bit 5] – Overrun is an error flag that indicates that one or more characters in the data stream were lost. That is, a character or a number of characters were received but not read from the Receiver Data Register (RDR) prior to subsequent characters being received. The overrun condition begins at the midpoint of the last bit of the second character received in succession without a read of the RDR having occurred. The Overrun does not occur in the Status Register until the valid character prior to Overrun has been read. The RDRF bit remains set until Overrun is reset. Character synchronization is maintained during the Overrun condition. The overrun indication is reset after the reading of data from the Receive Data Register. Overrun is also reset by the Master Reset.

Parity Error (PE) [Bit 6]–The parity error flag indicates that the number of highs (ones) in the character does not agree with the preselected odd or even parity. Odd parity is defined to be when the total number of ones is odd. The parity error indication will be present as long as the data character is in the RDR. If no parity is selected, then both the transmitter parity generator output and the receiver parity check results are inhibited.

Interrupt Request ($\overline{\text{IRQ}}$) [Bit 7]–The IRQ bit indicates the state of the $\overline{\text{IRQ}}$ output. Any interrupt that is set and enabled will be indicated in the status register. Any time the $\overline{\text{IRQ}}$ output is low the IRQ bit will be high to indicate the interrupt or service request status.

CONTROL REGISTER–The ACIA control Register consists of eight bits of write only buffer that are selected when RS and R/W are low. This register controls the function of the receiver, transmitter, interrupt enables, and the Request-to-Send modem control output.

Counter Divide Select Bits (CR0 and CR1)–The Counter Divide Select Bits (CR0 and CR1) determine the divide ratios utilized in both the transmitter and receiver sections of the ACIA. Additionally, these bits are used to provide a Master Reset for the ACIA which clears the Status Register and initializes both the receiver and transmitter. Note that after a power-on or a power-fail restart, these bits must be set High to reset the ACIA. After resetting, the clock divide ratio may be selected. These counter select bits provide for the following clock divide ratios:

CR1	CR0	Function
0	0	÷ 1
0	1	÷16
1	0	÷64
1	1	Master Reset

Word Select Bits (CR2, CR3, and CR4)–The Word Select bits are used to select word length, parity, and the number of stop bits. The encoding format is as follows:

CR4	CR3	CR2	Function
0	0	0	7 Bits + Even Parity + 2 Stop Bits
0	0	1	7 Bits + Odd Parity + 2 Stop Bit
0	1	0	7 Bits + Even Parity + 1 Stop Bit
0	1	1	7 Bits + Odd Parity + 1 Stop Bit
1	0	0	8 Bits + 2 Stop Bits
1	0	1	8 Bits + 1 Stop Bit
1	1	0	8 Bits + Even Parity + 1 Stop Bit
1	1	1	8 Bits + Odd Parity + 1 Stop Bit

Word length, Parity Select, and Stop Bit changes are not double-buffered and therefore become effective immediately.

Transmitter Control Bits (CR5 and CR6)–Two Transmitter Control bits provide for the control of the Transmitter Buffer Empty interrupt output, the Request-to-Send output and the transmission of a BREAK level (space). The following encoding format is used:

CR6	CR5	Function
0	0	$\overline{RTS}$ = low, Transmitting Interrupt Disabled
0	1	$\overline{RTS}$ = low, Transmitting Interrupt Enabled
1	0	$\overline{RTS}$ = high, Transmitting Interrupt Disabled
1	1	$\overline{RTS}$ = low, Transmitting Interrupt Disabled and Transmits a BREAK level on the Transmit Data Output.

Receiver Interrupt Enable Bit (RIE) (CR7)–Interrupts will be enabled by a high level in bit position 7 of the Control Register (CR7). Interrupts caused by the Receiver Data Register Full being high or by a low to high transition on the Data Carrier Detect signal line are enabled or disabled by the Receiver Interrupt Enable Bit.

TRANSMIT DATA REGISTER (TDR)–Data is written in the Transmit Data Register *during* the peripheral enable time (E) when the ACIA has been addressed and RS • R/W is selected. Writing data into the register causes the Transmit Data Register Empty bit in the status register to go low. Data can then be transmitted. If the transmitter is idling and no character is being transmitted, then the transfer will take place within one bit time of the trailing edge of the Write command. If a character is being transmitted, the new data character will commence as soon as the previous character is complete. The transfer of data causes the Transmit Data Register Empty (TDRE) bit to indicate empty.

RECEIVE DATA REGISTER (RDR)–Data is automatically transferred to the empty Receive Data Register (RDR) from the receiver deserializer (a shift register) upon receiving a complete character. This event causes the Receiver Data Register Full bit (RDRF) (in the status buffer) to go high (full). Data may then be read through the bus by addressing the ACIA and selecting the Receiver Data Register with RS and R/W high when the ACIA is enabled. The non-destructive read cycle causes the RDRF bit to be cleared to empty although the data is retained in the RDR. The status is maintained by RDRF as to whether or not the data is current. When the Receiver Data Register is full, the automatic transfer of data from the Receiver Shift Register to the Data Register is inhibited and the RDR contents remain valid with its current status stored in the Status Register.

OPERATIONAL DESCRIPTION

From the MPU Bus interface the ACIA appears as two addressable RAM memory locations. Internally, there are four registers; two read-only and two write-only registers. The read-only registers are status and receive data, and the write only registers are control and transmit data. The serial interface consists of serial transmit and receive lines and three modem/peripheral control lines.

During a power-on sequence, the ACIA is internally latched in a reset condition to prevent erroneous output transitions. This power-on reset latch can only be released by the master reset function via the control register; bits b_0 and b_1 are set "high" for a master reset. After master resetting the ACIA, the programmable control register can be set for a number of options such as variable clock divider ratios, variable word length, one or two stop bits, parity (even, odd, or none) and etc.

TRANSMITTER–A typical transmitting sequence consists of reading the ACIA status register either as a result of an interrupt or in the ACIA's turn in a polling sequence. A character may be written into the Transmitter Data Register if the status read operation has indicated that the Transmit Data

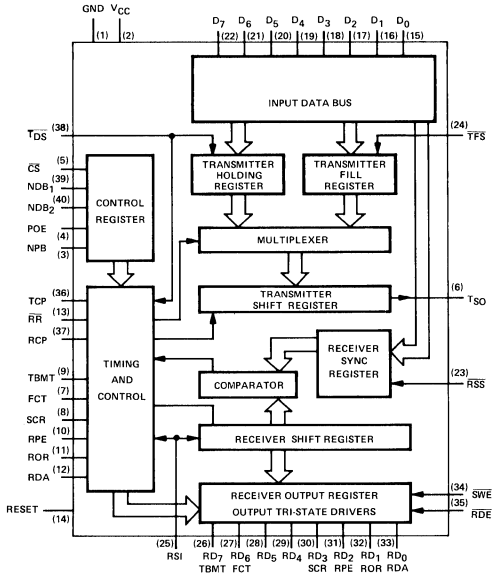
Register is empty. This character is transferred to a shift register where it is serialized and transmitted from the Tx Data output preceded by a start bit and followed by one or two stop bits. Internal parity (odd or even) can be optionally added to the character and will occur between the last data bit and the first stop bit. After the first character is written in the data register, the status register can be read again to check for a Transmit Data Register Empty condition and current peripheral status. If the register is empty, another character can be loaded for transmission even though the first character is in the process of being transmitted. This second character will be automatically transferred into the shift register when the first character transmission is completed. The above sequence continues until all the characters have been transmitted.

RECEIVER–Data is received from a peripheral by means of the Rx Data input. A divide by one clock ratio is provided for an externally synchronized clock (to its data) while the divide by 16 and 64 ratios are provided for internal synchronization. Bit synchronization in the divide by 16 and 64 modes is obtained by the detection of the leading mark-to-space transition of the start bit. False start bit deletion capability insures that a full half bit of a start bit has been received before the internal clock is synchronized to the bit time. As a character is being received, parity (odd or even) will be checked and the error indication will be available in the status register along with framing error, overrun error, and receiver data register full. In a typical receiving sequence, the status register is read to determine if a character has been received from a peripheral. If the receiver data register is full, the character is placed on the 8-bit ACIA bus when a Read Data command is received from the MPU. The status register can be read again to determine if another character is available in the receiver data register. The receiver is also double buffered so that a character can be read from the data register as another character is being received in the shift register. The above sequence continues until all characters have been received.

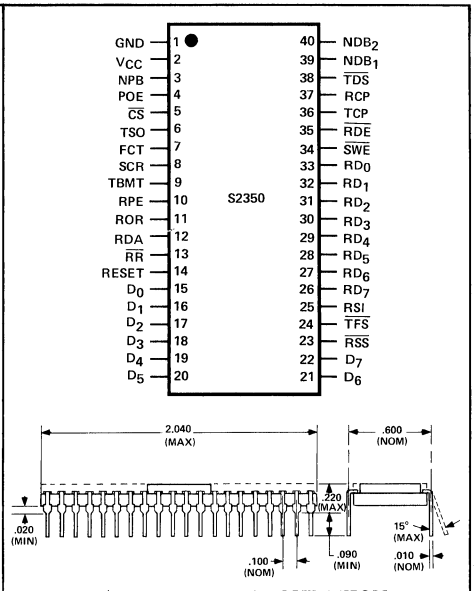
S2350

UNIVERSAL SYNCHRONOUS
RECEIVER/TRANSMITTER (USRT)

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5–8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character

received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- High Speed Terminals
- Time Division Multiplexing
- Industrial Data Transmission

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	−65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	−0.5 volt
Power dissipation	0.75 watt

DC (STATIC) CHARACTERISTICS*

$T_A = 0° - +70°C$. $V_{CC} = +5$ volts ±5%

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	V_{CC}	Volt	
V_{IL}	Input Low Voltage	- 0.5	+0.8	Volt	
I_{IL}	Input Leakage Current		10	μa	V_{IN} = OTO V_{CC} Volts
V_{OH}	Output High Voltage	2.4		Volts	$I_{OH} = -100\mu a$
V_{OL}	Output Low Voltage		+0.4	Volts	I_{OL} = 1.6ma
C_{IN}	Input Capacitance		10	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
C_{OUT}	Output Capacitance		12	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
I_{CC}	V_{CC} Supply Current		100	ma	No Load

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

AC (DYNAMIC) CHARACTERISTICS

$T_A = 0°C - +70°C, V_{CC} = +5$ volts ±5%

Symbol	Parameter	Min.	Max.	Unit	Condition
T_{CP}, R_{CP}	Clock Frequency	DC	500	KHz	

Input Pulse Widths

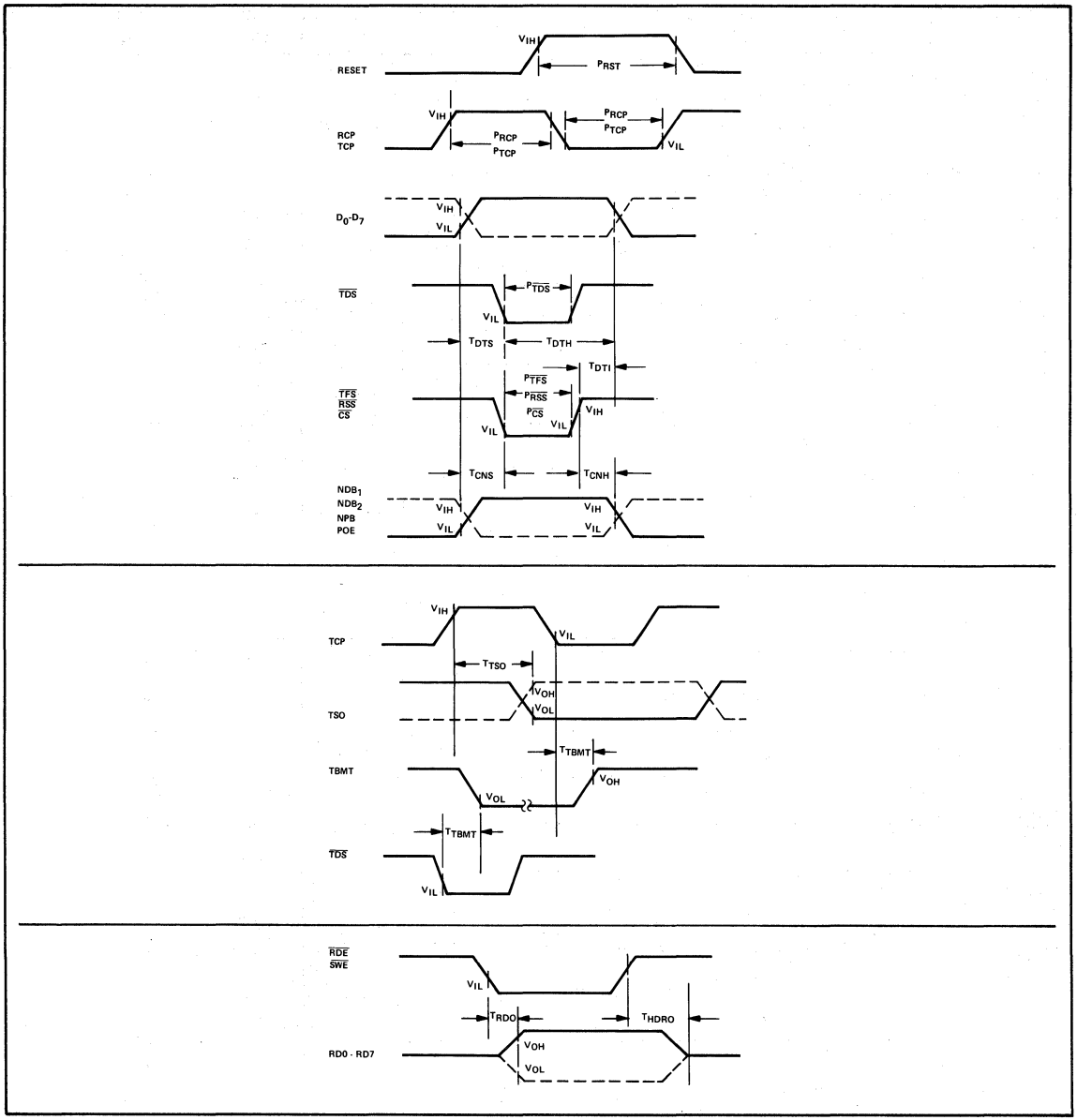
P_{TCP}	Transmit Clock	900		nsec	C_L = 20pf
P_{RCP}	Receive Clock	900		nsec	1TTL Load
P_{RST}	Reset	500		nsec	
$P_{\overline{TDS}}$	Transmit Data Strobe	200		nsec	
$P_{\overline{TFS}}$	Transmit Fill Strobe	200		nsec	
$P_{\overline{RSS}}$	Receive Sync Strobe	200		nsec	
$P_{\overline{CS}}$	Control Strobe	200		nsec	
$P_{\overline{RDE}}$	Receive Data Enable	400		nsec	Note 1
$P_{\overline{SWE}}$	Status Word Enable	400		nsec	Note 1
$P_{\overline{RR}}$	Receiver Restart	500		nsec	

Switching Characteristics

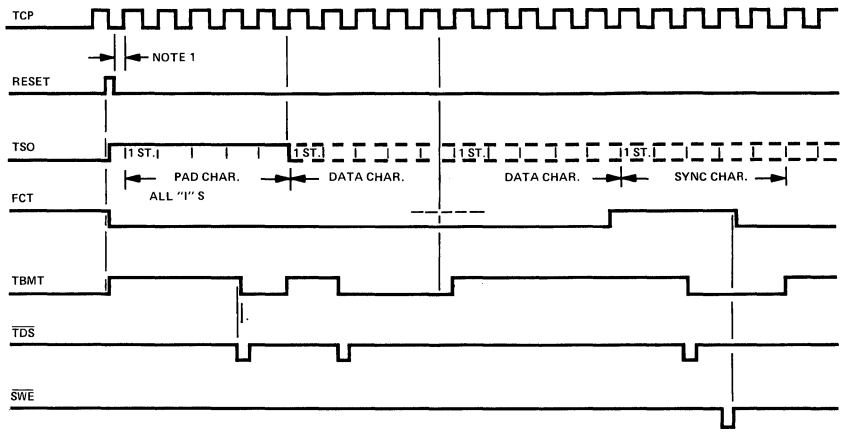
T_{TSO}	Delay, TCP Clock to Serial Data Out		700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output		1.4	μsec	
T_{TBMT}	Delay, $\overline{TDS}$ to TBMT		700	nsec	
T_{STS}	Delay, $\overline{SWE}$ to Status Reset		700	nsec	
T_{RDO}	Delay, $\overline{SWE}$, $\overline{RDE}$ to Data Outputs		400	nsec	1TTL Load
T_{HRDO}	Hold Time $\overline{SWE}$, $\overline{RDE}$ to Off State		400	nsec	C_L = 130 pf
T_{DTS}	Data Set Up Time $\overline{TDS}$, $\overline{TFS}$, $\overline{RSS}$, $\overline{CS}$	0		nsec	
T_{DTH}	Data Hold Time $\overline{TDS}$	700		nsec	
T_{DTI}	Data Hold Time $\overline{TFS}$, $\overline{RSS}$	200		nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0		nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200		nsec	
T_{RDA}	Delay $\overline{RDE}$ to $\overline{RDA}$ Output	700		nsec	

NOTE 1: Required to reset status and flags.

TIMING WAVEFORMS

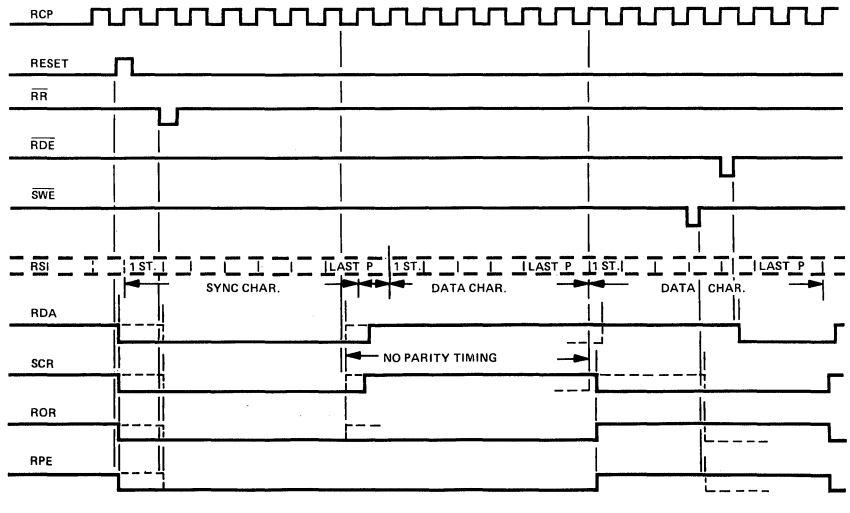


TRANSMITTER TIMING DIAGRAM



NOTE 1 DATA TRANSMISSION WILL START ON THE FIRST LOW TO HIGH TRANSITION OF TCP AFTER RESET IS LOW. THE INITIAL RESET PULSE SHOULD NOT OCCUR UNTIL 100 MICROSECONDS AFTER POWER IS APPLIED.

RECEIVER TIMING DIAGRAM



PIN DEFINITIONS

Pin	Label	Function
(1)	GND	Ground
(2)	V_{CC}	+5 VOLTS ±5%
(14)	RESET	MASTER RESET A V_{IH} initializes both the receiver and transmitter. The Transmitter Shift Register is set to output a character of all logic 1's. FCT is reset to V_{OL} and TBMT set to V_{OH} indicating the Transmitter Holding Register is empty. The receiver status is initialized to a V_{OL} on RPE, ROR, SCR, and RDA. The transmitter and receiver shift registers are reset to logic "0"s. The sync character detect logic is inhibited until a RR pulse is received.
(15)	D0	DATA INPUTS Data on the eight data lines is loaded into the Transmitter Holding Register by $\overline{TDS}$, the Transmitter Fill Register by $\overline{TFS}$, and the Receiver Sync Register by $\overline{RSS}$. Data is right jusitifed with the LSB at D0. For word lengths less than 8 bits, the unused inputs are ignored. Data is transmitted LSB first.
(16)	D1	
(17)	D2	
(18)	D3	
(19)	D4	
(20)	D5	
(21)	D6	
(22)	D7	
(38)	$\overline{TDS}$	TRANSMIT DATA STROBE A V_{IL} loads data on D0-D7 into the Transmitter Holding Register and resets TBMT to a V_{OL}.
(24)	$\overline{TFS}$	TRAMSMIT FILL STROBE A V_{IL} loads data on D0-D7 into the Transmitter Fill Register. The character in the Transmitter Fill Register is transmitted whenever a new character is not loaded in the allotted time after the TBMT is set to V_{OH}.
(23)	$\overline{RSS}$	RECEIVER SYNC STROBE A V_{IL} loads data on D0-D7 into the Receiver Sync Register. SCR is set to V_{OH} whenever data in the Receiver Shift Register compares with the character in the Receiver Sync Register.
(9)	TBMT	TRANSMIT BUFFER EMPTY A V_{OH} indicates the data in the Transmitter Holding Register has been transferred to the Transmitter Shift Register and new data may be loaded. TBMT is reset to V_{OL} by a V_{IL} on $\overline{TDS}$. A V_{IH} on RESET sets TBMT to a V_{OH}. TBMT is also multiplexed onto the RD7 output (26) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(6)	TSO	TRANSMITTER SERIAL OUTPUT Data entered on D0-D7 are transmitted serially, least significant bit first, on TSO at a rate equal to the Transmit Clock frequency, TCP. Source of the data to the transmitter shift register is the Transmitter Holding Register or Transmitter Fill Register.
(36)	TCP	TRANSMIT CLOCK Data is transmitted on TSO at the frequency of the TCP input in a NRZ format. A new data bit is started on each negative to positive transition (V_{IL} to V_{IH}) of TCP.

Pin	Label	Function
(26) (27) (28) (29) (30) (31) (32) (33)	RD7 RD6 RD5 RD4 RD3 RD2 RD1 RD0	RECEIVED DATA OUTPUTS RDO-RD7 contain data from the Receiver Output Register or selective status conditions depending on the state of $\overline{SWE}$ and $\overline{RDE}$ per the following table:

(34)	(35)	(33)	(32)	(31)	(30)	(39)	(28)	(27)	(26)
$\overline{SWE}$	$\overline{RDE}$	RD0	RD1	RD2	RD3	RD4	RD5	RD6	RD7
V_{IL}	V_{IL}	X	X	X	X	X	X	X	X
V_{IL}	V_{IH}	RDA	ROR	RPE	SCR	V_{OL}	V_{OL}	FCT	TBMT
V_{IH}	V_{IL}	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7
V_{IH}	V_{IH}	X	X	X	X	X	X	X	X

X Output is in the OFF or Tri-State condition
DB0 LSB of Receiver Output Register
DB7 MSB of Receiver Output Register
The two unused outputs are held at V_{OL} in the output status condition.

(35)	$\overline{RDE}$	RECEIVE DATA ENABLE A V_{IL} enables the data in the Receiver Output Register onto the output data lines RD0–RD7. The trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$ resets RDA to the V_{OL} condition.
(7)	FCT	FILL CHARACTER TRANSMITTED A V_{OH} on FCT indicates data from the Transmitter Fill Register has been transferred to the Transmitter Shift Register. FCT is reset to V_{OL} when data is transferred from the Transmitter Holding Register to the Transmitter Shift Register, or on the trailing edge (V_{IL} to V_{IH}) of the $\overline{SWE}$ pulse, or when RESET is V_{IH}. FCT is multiplexed onto the RD6 output (27) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(25)	RSI	RECEIVER SERIAL INPUT Serial data is clocked into the Receiver Shift Register, least significant bit first, on RSI at a rate equal to the Receive Clock frequency RCP.
(37)	RCP	RECEIVE CLOCK Data is transferred from RSI input to the Receiver Shift Register at the frequency of the RCP input. Each data bit is entered on the positive to negative transition (V_{IH} to V_{IL}) of RCP.

Pin	Label	Function
(12)	RDA	RECEIVED DATA AVAILABLE A V_{OH} indicates a character has been transferred from the Receiver Shift Register to the Receiver Output Register. RDA is reset to V_{OL} on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RDA is multiplexed onto the RD0 output (33) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(8)	SCR	SYNC CHARACTER RECEIVED A V_{OH} indicates the data in the Receiver Shift Register is identical to the data in the Receiver Sync Register. SCR is reset to a V_{OL} when the character in the Receiver Shift Register does not compare to the Receiver Sync Register, on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{SWE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. SCR is multiplexed onto the RD3 output (30) when $\overline{SWE}$ is a V_{IL} and $\overline{RDE}$ is V_{IH}.
(34)	$\overline{SWE}$	STATUS WORD ENABLE A V_{IL} enables the internal status conditions onto the output data lines RD0–RD7. The trailing edge of $\overline{SWE}$ pulse resets FCT, ROR, RPE, and SCR to V_{OL}.
(11)	ROR	RECEIVER OVERRUN A V_{OH} indicates data has been transferred from the Receiver Shift Register to the Receiver Output Register when RDA was still set to V_{OH}. The last data in the Output Register is lost. ROR is reset by a V_{IL} on $\overline{RDE}$ by the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. ROR is multiplexed onto the RD1 output (32) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(10)	RPE	RECEIVER PARITY ERROR A V_{OH} indicates the accumulated parity on the received character transferred to the Output Register does not agree with the parity selected by POE. RPE is reset with the next received character with correct parity, the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RPE is multiplexed onto the RD2 output (31) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(13)	$\overline{RR}$	RECEIVER RESTART A V_{IL} resets the receiver section by clearing the status RDA, SCR, ROR, and RPE to V_{OL}. The trailing edge of $\overline{RR}$ (V_{IL} to V_{IH}) also puts the receiver in a bit transparent mode to search for a comparison, each bit time, between the contents of the Receiver Shift Register and the Receiver Sync Register. The number of data bits per character for the comparison is set by NDB1 and NDB2. After a compare is made SCR is set to V_{OH}, the sync character is transferred to the Receiver Output Register, and the receiver enters a word synchronous mode framing an input character each word time. NOTE: Parity is not checked on the first sync character but is enabled for every succeeding character.

Pin	Label	Function
(39)	NDB1	NUMBER DATA BITS The number of Data Bits per character are determined by NDB1 and NDB2. The number of data bits does not include the parity bit.

NDB2	NDB1	CHARACTER LENGTH
V_{IL}	V_{IL}	5 Bits
V_{IL}	V_{IH}	6 Bits
V_{IH}	V_{IL}	7 Bits
V_{IH}	V_{IH}	8 Bits

For character lengths less than 8 bits, unused inputs are ignored and unused outputs are held to V_{OL}. Data is always right justified with D0 and RD0 being the least significant bits.

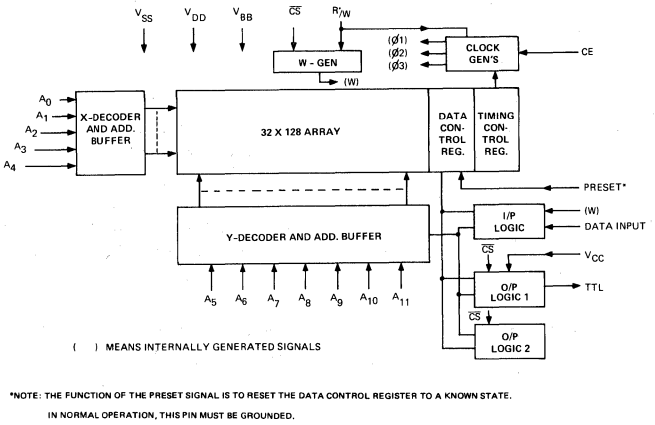
(3)	NPB	NO PARITY BIT A V_{IH} eliminates generation of a parity bit in the transmitter and checking of parity in the receiver. With parity disabled, the RPE status bit is held at V_{OL}.
(4)	POE	PARITY ODD/EVEN A V_{IH} directs both the transmitter and receiver to operate with even parity. A V_{IL} forces odd parity operation. NPB must be VIL for parity to be enabled.
(5)	$\overline{CS}$	CONTROL STROBE A V_{IL} loads the control inputs NDB1, NDB2, POE, and NPB into the Control Register. For static operation, $\overline{CS}$ can be tied directly to ground.

S6605
S6605A
S6605B

4096×1 RANDOM ACCESS MEMORY

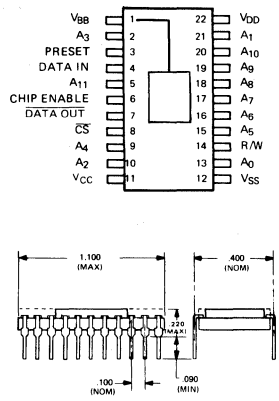
AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



*NOTE: THE FUNCTION OF THE PRESET SIGNAL IS TO RESET THE DATA CONTROL REGISTER TO A KNOWN STATE. IN NORMAL OPERATION, THIS PIN MUST BE GROUNDED.

BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2C, 1C - see Sec. 1)

FEATURES

- Fast Access Time 210 – 300 – 600 ns
- Fast Read Cycle Time 370 – 470 – 900 ns
- Fast Read/Write Cycle Time – 490 – 590 – 1100 ns
- Low Power Dissipation
  - Active 335 mW Typ.
  - Standby with Refresh 4 mW Typ.
- Output – 3 State TTL
- Easy Refresh – Only 32 Cycles every 2.0 ms
- Address and data input latches on Chip
- TTL compatible Inputs except Chip Enable Clock
- Simple Memory Expansion – Chip Select
- 22 Pin Dual In-Line Package

FUNCTIONAL DESCRIPTION

The AMI S6605 series of dynamic read/write memories are designed for applications where high performance, low cost and large bit storage are desired in mainframe, add-on, and buffer memories and peripheral storage. The S6605 is a 4096 word by 1 bit array fabricated with selective oxidation N-Channel silicon gate technology. All decoding is done on the chip using ratioless techniques.

All addresses and control inputs are TTL/DTL compatible except for a single high voltage chip enable (CE) clock. The single + 12 volt CE clock lowers system cost. Low voltage swings result in a system with low noise and easy interface.

For standard interface, the S6605 provides a three state TTL output. The information read-out is nondestructive (NDRO). Refresh of the entire memory is accomplished by sequentially cycling each of the 32 row addresses (A_0 - A_4) every 2 ms.

TYPICAL APPLICATIONS

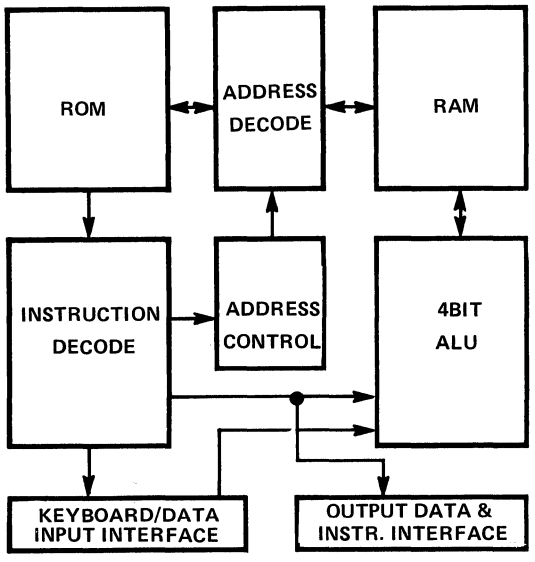
- Main Frame Memory
- Buffer Memory
- Add-on Memory
- Peripheral Storage
- Terminals, etc.

For a Complete Data Sheet See Page 4-32

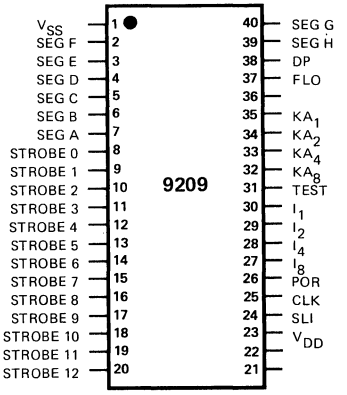
9209

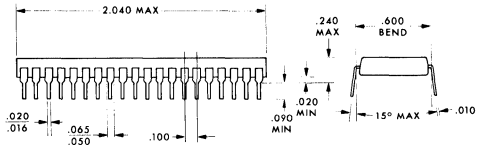
MICROPROGRAMMABLE
DISPLAY PROCESSOR

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM





PIN/PACKAGE CONFIGURATION
(Available in Pkg. 1T - see Sec. 1)

FEATURES

- 6048 bit internal ROM
- 256 bit internal RAM
- Two Accumulators
- Microinstruction decoding and control logic
- Clock generator integral to the chip
- Separate Input/Output Circuits
- Programmable keyboard matrix and debounce
- Programmable output
- Automatic power-on clear or initialization
- Outputs drive LED segments or flourescent displays directly

FUNCTIONAL DESCRIPTION

The 9209 Microprogrammable Display Processor (MDP) provides a flexible method of creating a variety of calculator and display-oriented microprocessor circuits. Designed to handle numeric input/output and display of up to 12 digits, the MDP contains all the essential elements of a microprocessor on one MOS chip (see block diagram).

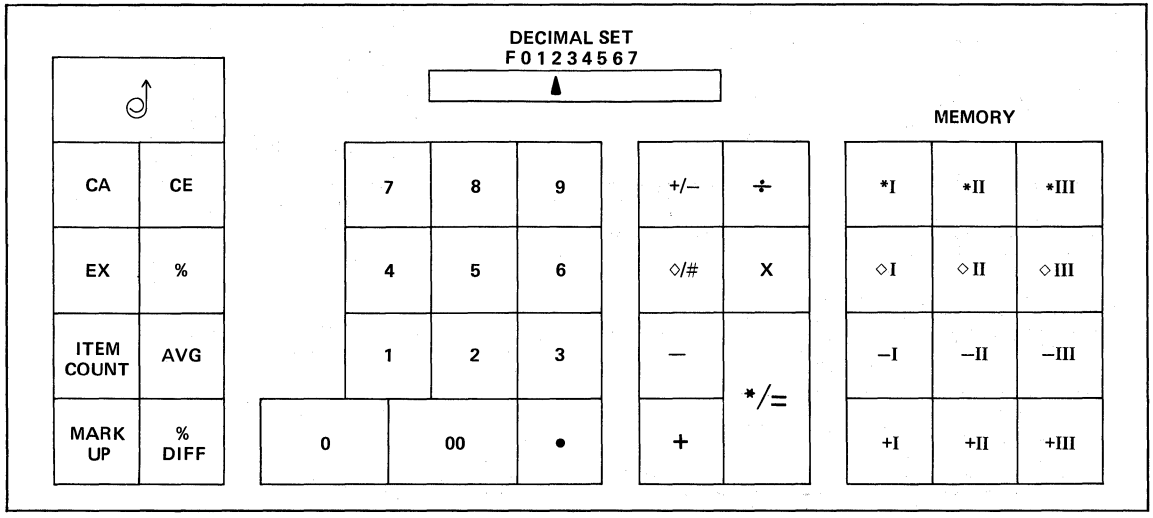
These elements—combined with an unusually versatile instruction set—allow the MDP to be used in a wide variety of calculator and non-calculator fixed program applications.

TYPICAL APPLICATIONS

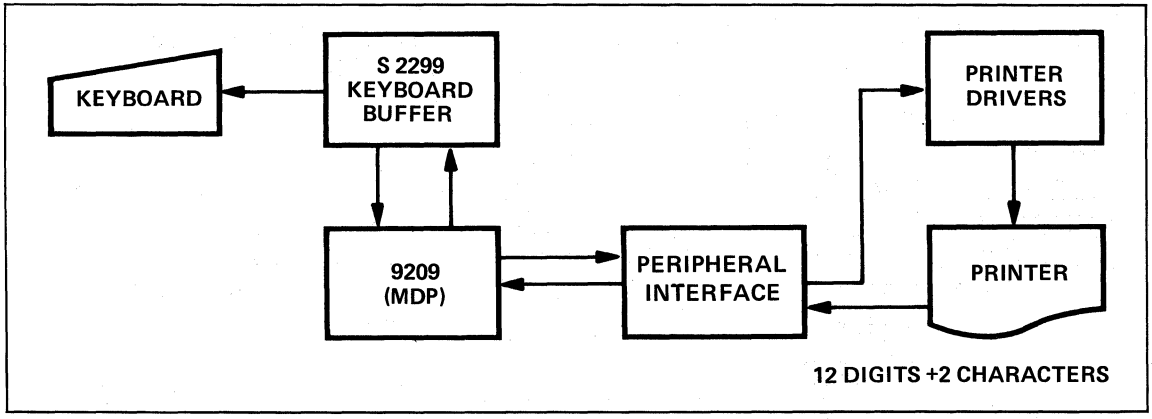
The relatively low cost of the MDP combined with its on-chip ROM and RAM functions permits its use in a wide variety of specialized systems requiring a nominal amount of data processing and data manipulation capability. Its area of application lies between special purpose (custom) LSI chips and standard high performance microprocessors.

The MDP can be used by itself or, with a small amount of external hardware, several may be connected in tandem for applications requiring increased capability. The figure below shows a typical multichip application for a high-end printing calculator using a 9209, a peripheral interface chip and a S2299 keyboard buffer chip.

TYPICAL KEYBOARD



BLOCK DIAGRAM OF A TYPICAL 12 DIGIT PRINTING CALCULATOR SYSTEM



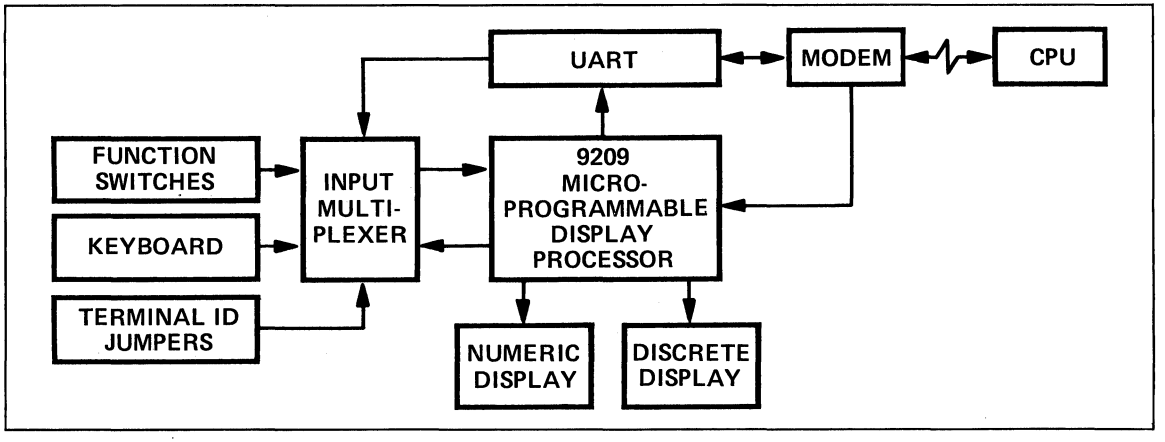
TYPICAL APPLICATIONS (Cont'd.)

The following figure shows the use of the 9209, a UART (Universal Asynchronous Receiver/Transmitter), and some TTL devices to implement a small terminal, used for the verification of credit sales and similar applications. All terminals in this network are periodically interrogated by the CPU and when a terminal receives its ID code (which is read in from the ID jumper matrix), it responds with "no transaction," or with the data which has been keyed in by the operator. In the latter case, the CPU responds with a discrete (OK, HOLD, WAIT, etc.) a credit limit, or other data such as a phone number to call, or a number sequence which must be given by the customer. Other applications include order entry and billing terminals.

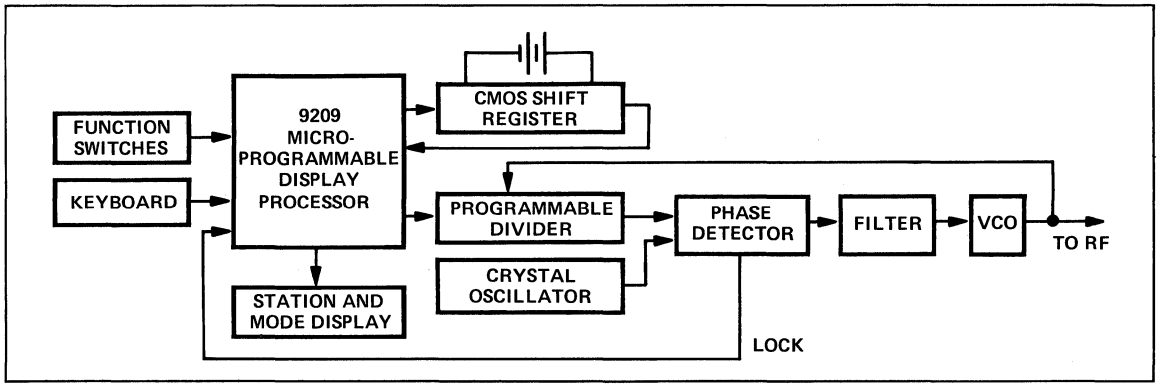
A third application shown is the use of the 9209 MDP as the controller for a digital FM tuner. The system is capable of storing ten station frequencies and includes automatic and manual search modes. Preselected stations are called up by depressing a single pushbutton.

As station entries are made, they are checked to assure that a valid frequency entry has been made. The preselected frequencies can be stored in the MDP's internal RAM, but normally are stored in a CMOS shift register with a separate battery supply to prevent loss of station data in the event of power failure.

CREDIT VERIFICATION TERMINAL APPLICATION



DIGITAL TUNER APPLICATION



TYPICAL APPLICATIONS (Cont'd.)

In addition to the preceding, the main use of the MDP is in single and multichip calculator and counting systems. AMI offers as standard products the following calculators which use the MDP-chip:

S9412 – 8 digit, five function display calculator with memory, metric/English conversions, square root, Pi, exchange, mark-up and percent change.

S9413 – 10 digit, five function display calculator with memory, square root and exchange.

S9414 – 12 digit, five function display calculator with memory, item count, average and mark-up.

S9651 – 10 digit, 7 function "slide-rule" with scientific notation and memory, square root and reciprocals.

Examples of two of these are shown below, as a guide to the functional complexity possible with this chip.

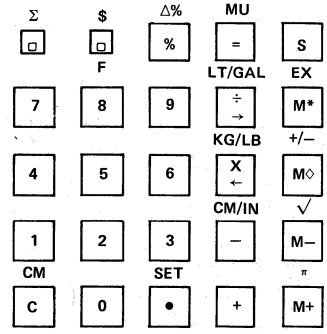
S9412 EIGHT DIGIT DISPLAY CALCULATOR

FEATURES

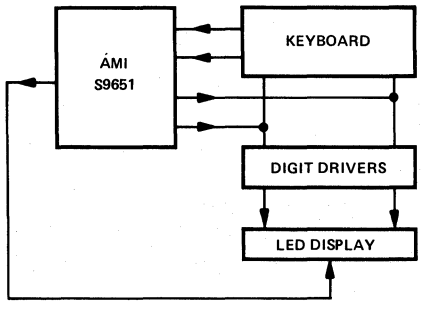
S9412

- Minimum external components.
- Low power.
- Five Function (+, –, x, ÷, %) eight digit display.
- Percent discount and percent add-on.
- Memory in-use indication.
- Algebraic keyboard with full-chaining.
- Automatic constant factor on five functions.
- Floating decimal mode.
- Add mode.
- Square root.
- π entry.
- Percentage mark-up.
- Percentage difference.
- Constant percentage mark-up and percentage difference.
- Register exchange.
- Change sign.
- Fixed decimal point with 5/4 rounding.
- Conversion of liters/gallons, kilograms/pounds, and centimeters/inches.
- Constant conversion modes.

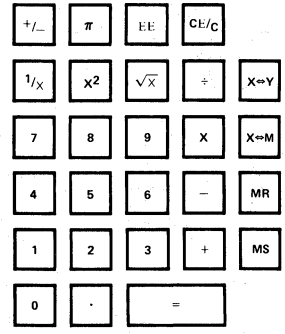
TYPICAL KEYBOARD



S9651 SLIDERULE CALCULATOR



BLOCK DIAGRAM



TYPICAL KEYBOARD

DETAILED FUNCTIONAL DESCRIPTION

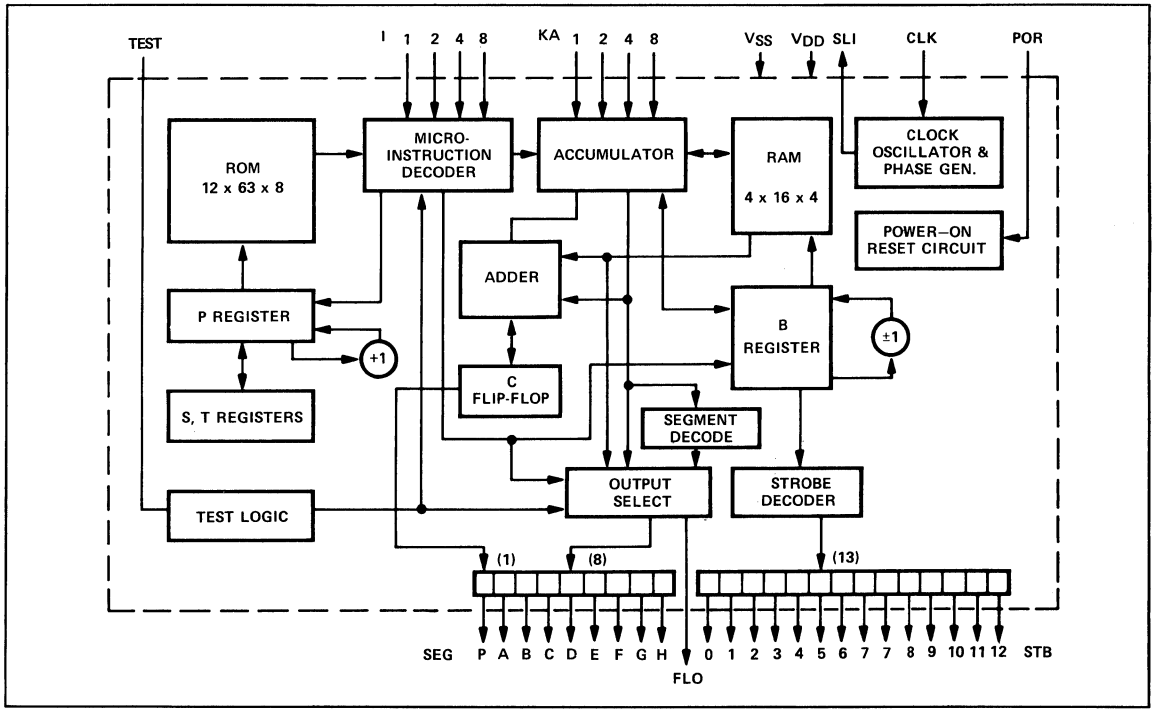
The detailed block diagram shows the major functional parts of the MDP. These are:

- A 6048-bit ROM containing microinstructions (12 x 63 x 8 organization).
- A 256-bit RAM memory for storing information (4 x 16 x 4 organization).
- A 4-bit parallel binary adder.
- Two 4-bit accumulators.
- A 6-bit RAM address register.
- A 10-bit ROM address register.
- Microinstruction decoding and control logic.
- A polynominal counter for incrementing the ROM address register.
- Two 10-bit address save registers.
- Input and output circuits.

The MDP is programmed by using microinstructions coded into the ROM. The ROM is organized into twelve "blocks" or "pages" each containing 63 words, which are addressed by the upper four bits of the address register. The lower 6 bits address the specific 8-bit word in each block.

The ROM addressing system consists of the P, S and T registers, each composed of an upper four bits and a lower six bits, a 6-bit polynomial counter, and two address control flip-flops. Normally, the polynomial counter is incremented once each instruction cycle and its contents transferred to the PL register to address the next ROM instruction. The counter can also be set to a specific starting address. The S and T registers form a stack used for storing return addresses when calling subroutines. The "pushing" and "popping" of the stack is controlled by the program.

9209 MDP DETAILED BLOCK DIAGRAM



DETAILED FUNCTIONAL DESCRIPTION (Cont'd.)

The RAM is used for storage of information in the processor. It is organized as four registers each containing sixteen 4-bit words. Data in the RAM can be loaded into the accumulator, exchanged with the accumulator, added to the accumulator or compared to the accumulator. Individual bits of the RAM can also be set, reset, and tested.

The adder is a parallel 4-bit binary adder having a carry input from the C flip-flop and two data inputs. The sum output is stored in the accumulator. The carry output can be stored in the C flip-flop and can be used by the control logic to skip microinstructions.

The main accumulator is a 4-bit register which can be loaded from the RAM, from the data input lines, from the ROM, from the adder or from the second accumulator. The latter is also a 4-bit register which can be loaded from the RAM.

The MDP also contains thirteen strobe outputs, which are under program timing and control. These outputs can be used for sampling a keyboard and/or driving a display. Segment data outputs for a display, four discrete data inputs, and an input for BCD data into the accumulator are also available. Optionally, data can be output in BCD, together with a data sampling pulse (FLO) for external use.

Also included are an internal oscillator, clock generators, and a power-on initializing circuit.

INSTRUCTION SET

The MDP operation is programmed by use of instructions stored in the ROM. The instruction set includes arithmetic, load, test and flag, addressing, and miscellaneous groups, and is summarized in the table below. The instructions operate on digits (4 bits) or individual bits of the data stored in the RAM. Register handling instructions can be implemented by the use of subroutines.

The nominal instruction cycle time is 15 usec. All instructions are executed in one cycle, with the exception of transfer and return instructions, which require two cycles.

There are also several mask programmed options which control the operation of hardware portions of the chip and which define parameters for the instructions. These include coding of the segment ROM and specifying the register length for register operations.

9209 INSTRUCTION SET SUMMARY

ARITHMETIC

ADD
ADD WITH CARRY
ADD IMMEDIATE
COMPLEMENT

LOAD A

LOAD IMMEDIATE
LOAD FROM RAM
EXCHANGE
EXCHANGE AND INCREMENT POINTER
EXCHANGE AND DECREMENT POINTER
LOAD FROM K INPUTS
LOAD FROM POINTER
LOAD FROM A2

TEST AND FLAG

SET, RESET, TEST C
SET, RESET, TEST BIT OF RAM
TEST A EQUAL RAM
TEST DISCRETE INPUTS
TEST KEY DOWN

ADDRESSING

JUMP
JUMP TO SUBROUTINE
JUMP TO MACROROUTINE
RETURN
RETURN AND SKIP
LOAD PAGE REGISTER

MISCELLANEOUS

SET POINTER
LOAD POINTER FROM A
LOAD STROBE OUTPUT
LOAD SEGMENT OUTPUTS FROM DECODE ROM
LOAD SEGMENT OUTPUTS FROM A AND RAM

PROGRAMMING SUPPORT

The following aids are available to assist in microprogram development for the MDP:

- Detailed hardware description and programming guide.
- Computer simulator running on AMI's internal timeshare network.
- Assembler.
- Hardware simulator.
- Sentry test program generator.

The hardware and software simulators both include diagnostic capabilities to assist the debugging of microprograms.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (All voltages measured with respect to V_{SS})

	Min.	Max.	Units
Storage Temperature	−55	+125	°C
Operating Temperature	0	+70	°C
Maximum Positive Voltage (any pin)		+0.3	V
Maximum Negative Voltage (any pin)		−30	V
Maximum Output Current (Segments)		11	mA
Maximum Output Current (Strobes)		5	mA

ELECTRICAL CHARACTERISTICS: V_{DD} = −15 ± 1V, T_A = 0 −55°C (All voltages measured with respect to V_{SS})

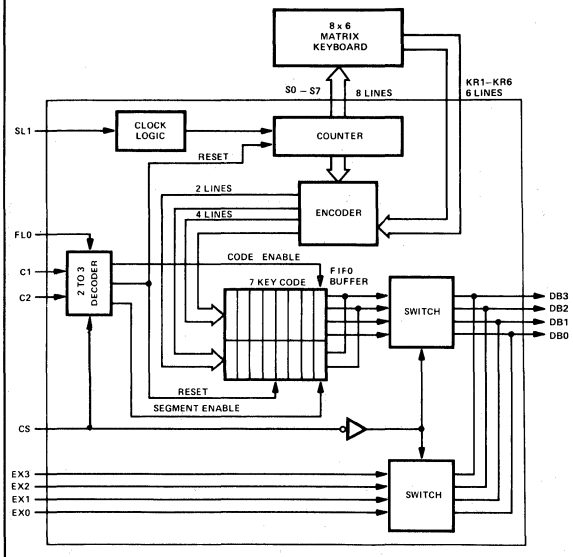
	Min.	Typ.	Max.	Units
Input High Level (Note 1)	−1.8		V_{SS}	V
Input Low Level (Note 1)	V_{DD}		−4.6V	V
Output High Level:				
Seg A - Seg H, DP; I = 6.5 mA	−3.0		V_{SS}	V
SO - S12, I - 2.8 mA; FLO, SL1, I = 1.0 mA	−1.5		V_{SS}	V
Output Low Current; V_O = −10V			25	μA
Supply Current		6.6	10.0	mA
Power Dissipation (Note 2)		100	160	MW
Power Reset Capacitor (Note 3)		100		pF
Oscillator Timing Resistor (Note 4)		24		KΩ
Oscillator Timing Capacitor (Note 5)		100		pF

NOTE 1. Inputs I1 − I8, KA_1 − KA_8. Each of these inputs has an internal resistor to V_{DD}. R_{MIN} = 125 KΩ.
NOTE 2. Does not include power dissipated in digit and segment drivers.
NOTE 3. Connected between POR pin and V_{SS}.
NOTE 4. Connected between CLK pin and V_{DD}.
NOTE 5. Connected between CLK pin and V_{SS}.

S2299

KEYBOARD BUFFER

AMERICAN MICROSYSTEMS, INC.



S2299 KEYBOARD BUFFER

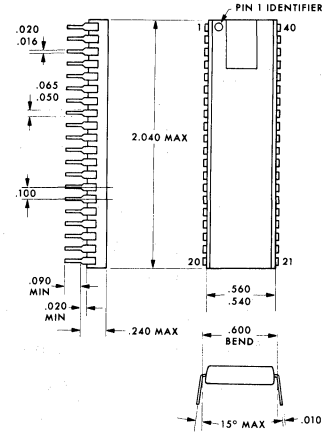
BLOCK DIAGRAM

PIN ASSIGNMENT

1. V_{SS}	40. FLO
2. *	39. C2
3. C1	38. TST
4. DB0	37. V_{DD}
5. *	36. *
6. *	35. *
7. EX0	34. KR6
8. DB1	33. KR5
9. EX1	32. KR4
10. MTEE	31. KR3
11. CS	30. KR2
12. EX2	29. KR1
13. DB2	28. SL1
14. EX3	27. S0
15. DB3	26. *
16. *	25. *
17. *	24. S1
18. S7	23. S2
19. S6	22. S3
20. S5	21. S4

* NO CONNECTION

All signals, except MTEE, are inverted.



PIN/PACKAGE CONFIGURATION

(Available in Pkg. 1T - see Sec. 1)

FEATURES

- 7 Key Buffer Storage
- 2 Key Rollover
- 48 Position Keyboard Matrix
- Key Bounce Protection
- 4 Line Data Bus

FUNCTIONAL DESCRIPTION

Interface Capabilities

The Keyboard Buffer chip interfaces with a keyboard matrix of up to 8 x 6 keys via a 4-bit parallel data bus. In addition, the chip provides a straight through data path from four separate input pins onto the data bus. All multiplexing control is compatible with a specially programmed 9209 chip.

Contact your AMI Sales Office or fill out the Business Reply Card in this Catalog for additional information on this Product.

7

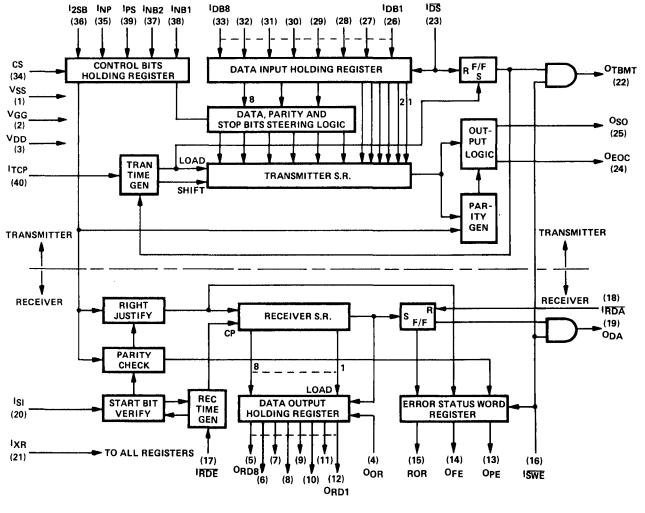
Communications Circuits

Selection Guide—Communications Circuits

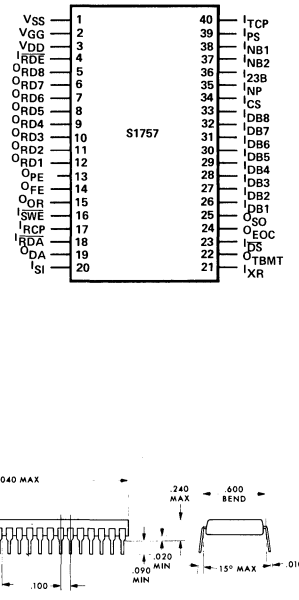
Part No.	Description	Word Length (Bits)	Max. Clock Freq. (KHz)	Input/ Output	Power Supply (V)	Process	Package	See Page
S1757	Asynchronous Receiver/Transmitter	5, 6, 7, 8	160	MOS	-12, ±5	P-I^2	3M,1T	7-3
S1883	Asynchronous Receiver/Transmitter	5, 6, 7, 8	200	TTL	-12, +5	P-I^2	3M,1T	7-9
S2350	Synchronous Receiver/Transmitter	5, 6, 7, 8	500	TTL	+5	N-SiGate	3M,1T	7-16
S6850	Asynchronous Receiver/Transmitter	7, 8	800	TTL	+5	N-SiGate	2L,1W	7-19
S9544	CRC Encoder/ Decoder	N/A	1000	TTL	-12, +5	P-I^2	4D,1D	7-20

S1757

UART™
UNIVERSAL ASYNCHRONOUS
RECEIVER/TRANSMITTER



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

FUNCTIONAL DESCRIPTION

UART – AMI's Universal Asynchronous Receiver/Transmitter – can simultaneously convert asynchronous serial binary characters to a parallel format and parallel binary characters to a serial asynchronous output with start and stop bits added.

General Description

The S1757 UART is a full duplex MOS digital data transmitter/receiver featuring TTL compatibility, asynchronous data transmission and a 10 kHz maximum baud rate. External controls select data word length, parity mode, and number of stop bits. The baud rate is established by the input clock frequency.

Packaged in a 40-pin dual inline package, the S1757 is a single TTL compatible LSI chip which functionally replaces approximately 25 TTL/MSI packages – including shift registers, latches and counters.

All UART characters contain a start bit, 5, 6, 7 or 8 data bits, an odd or even (or none at all) parity bit, and one or two stop bits.

Transmitting: The transmitting section is capable of operating in the dc to 10,000 baud range. Its unique front-end design includes TTL compatible clock inputs which eliminate the need for addition circuitry. In addition to the usual information bits the UART provides flag outputs that signal the end of transmission and that the buffer is empty.

Included in the transmitter section is an input holding register, a parallel to serial shift register, and the control logic necessary to convert parallel input data into a serial asynchronous communication format, adding start, stop and parity bits. The buffer register permits loading of the next character during the transmission of the present character.

Receiving: A unique start bit detection scheme in the receiver section of UART rejects input noise pulses and allows for errorless capture of data with up to 42% input distortion. Error-checking features include parity, framing and overrun checks, which provide flag outputs when an error is detected. Until the next character is received, the flag outputs and received data are stored internally. These outputs are wire-ORable and are provided with separate enable inputs for use in bus-organized system applications.

The receiver section contains a serial to parallel shift register, an output holding register, and the control logic necessary to receive an asynchronous serial data stream, check for parity and frame timing, and convert the data bits to a parallel format.

The S1757 array is fabricated with AMI's low V_T process. Inputs are directly TTL compatible – with an external resistor required to establish an adequate V_{IH} – and output interface is achieved with external pulldown resistors.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on Any Pin with Respect to V_{SS}	+.3 Volt
Negative Voltage on Any Pin with Respect to V_{SS}	−19.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS

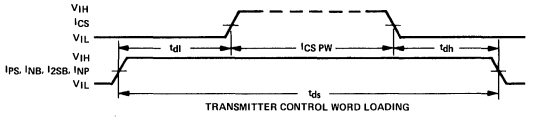
T_A = 0°C to +70°C; V_{SS} = +5 Volt ±5%; V_{GG} = −12 Volt ±5%; V_{DD} = −5 Volt ±5%

Symbol	Min	Typ	Max	Units	Conditions
V_{IH}	V_{SS} −1.0		V_{SS} +0.3	Volts	
V_{IL}	V_{GG}		+0.5	Volts	
V_{OH}	+2.5			Volts	Load = 20pF, 6.8KΩ to V_{GG} and 1 TTL input
V_{OL}			+0.4	Volts	Load = 20pF, 6.8KΩ to V_{GG} and 1 TTL input
C_{IN}			10	pF	$V_{IN} = V_{SS}$
C_{OUT}			10	pF	$V_{OUT} = V_{SS}$
I_{SS}			40	mA	$I_{\overline{SWE}} = I_{\overline{RDE}} = V_{IL}$
I_{DD}			10	mA	Load = 20pF, 6.8KΩ to V_{GG} and 1 TTL input
I_{GG}			10	mA	

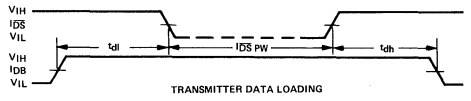
AC (DYNAMIC) CHARACTERISTICS

T_A = 0°C to +70°C; V_{SS} = +5 Volt ±5%; V_{GG} = −12 Volt ±5%; V_{DD} = −5 Volt ±5%

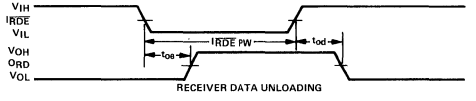
Symbol	Min	Typ	Max	Unit	Condition
Clock Frequency (I_{TCP}, I_{RCP})	DC		160	kHz	
P. W. (Clock)	3			μs	
P. W. (I_{CS})		500		ns	
P. W. ($I_{\overline{DS}}$)		250		ns	
P. W. (I_{XR})	2			μs	
P. W. ($I_{\overline{SWE}}$, $I_{\overline{RDA}}$, ($I_{\overline{RDE}}$)	1			μs	
t_{DL}	200			ns	Data lead time. The time before the I_{CS} ($I_{\overline{DS}}$) pulse during which the data must be valid.
t_{DH}	200			ns	The time after the I_{CS} ($I_{\overline{DS}}$) pulse during which the data must remain valid.
t_{OE}			2	μs	Output enable time. The time elapse between the leading edge of the $I_{\overline{SWE}}$ ($I_{\overline{RDE}}$) pulse and valid output data.
t_{OD}			2	μs	Output disable time. The time elapse between the trailing edge of the $I_{\overline{SWE}}$ ($I_{\overline{RDE}}$) pulse and the output becoming invalid.
t_{DS}					Data sample time. The time during which data must be valid to be properly sampled. t_{DS} = t_{DL} + I_{CS} ($I_{\overline{DS}}$)PW + t_{DH}.



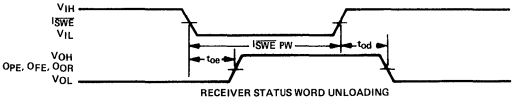
TRANSMITTER CONTROL WORD LOADING



TRANSMITTER DATA LOADING



RECEIVER DATA UNLOADING



RECEIVER STATUS WORD UNLOADING

APPLICATION DATA

Operational Description

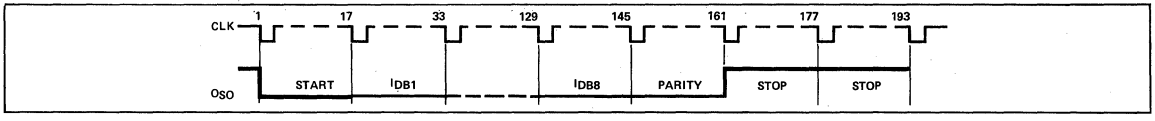
The UART block diagram is shown on the facing page. The UART transmitter asynchronously accepts 5 to 8 parallel data bits, which are temporarily stored in a holding register. The status of the transmitter is then checked to determine whether it is in the active or idle mode. If in idle (previously loaded character has been transmitted), the parallel data is transferred to a serial shift register together with start bit, parity, and stop bits in accordance with the settings of the control bit registers I_{NB2}, I_{NB1}, I_{2SB}, I_{PS} and I_{NP}. The data is then shifted out serially, start bit first, at rates up to 10K baud. Each bit transmitted is 16 I_{TCP} clock periods long. The transfer of data from the parallel register to the serial register is internally synchronized to eliminate possible variations of start pulse width due to asynchronous loading of input data. *If the input register is loaded during transmission of a character, the next start bit will immediately follow the last stop bit of the previous character. This feature eliminates the need for any precise external timing by allowing up to one full character time for the loading of the next character.*

The S1757 as a Data Receiver

UART functions as a data receiver by detecting a start bit on a serial input and shifting the data bits following into a serial register. The receiver detects a start bit by looking for a mark to space transition and sampling the input during the following 8 clock periods. *If the input line returns to mark (noise spike) during any of the 8 clock periods, the receiver returns to idle. If a valid start bit is received (V_L for 8 clock periods), the receiver enters the data entry mode.* The data word is shifted in by sampling the input at each succeeding 16th clock period after the 8 clock period start bit validation. After receiving the data bits, the control logic checks for parity and framing errors. During sampling of the first stop bit, the state of the data available register is checked. If the register has not been reset (indicating previous data has not been read out), an overrun error flag is generated. One clock period later, the data bits and transmission error flag signals are shifted in parallel to the output holding register and the data available (O_{DA}) register is set. The data and flags are held until receipt of the next character. *All outputs can be bussed with the outputs of other UARTs* with selection of data controlled by the $I_{\overline{SWE}}$ and $I_{\overline{RDE}}$ enable lines.

The S1757 Universal Asynchronous Receiver/Transmitter is now available from American Micro-Systems, Inc. The UART is ideally suited for a wide variety of data communication applications – including time division multiplexers, data concentrators, modems, communications processors, data terminals and various types of computer communications. UART's universal programming feature allows interfacing with the vast majority of communications devices, including Model 28, 32, 33, 37 and Inktronic Teletypes, IBM 2741, all popular CRT terminals, and many other peripherals.

Example: TRANSMISSION SEQUENCE
(8 BIT, PARITY, 2 STOP BITS MODE)



PIN DEFINITIONS

Pin	Label	Function
(1)	V_{SS}	+5 Volt ±5%.
(2)	V_{GG}	−12 Volt ±5%.
(3)	V_{DD}	−5 Volt ±5%.
(12) – (5)	O_{RD}	RECEIVED DATA OUTPUTS. LSB of data word appears on O_{RD1} regardless of data word length.

PIN DEFINITIONS (Continued)

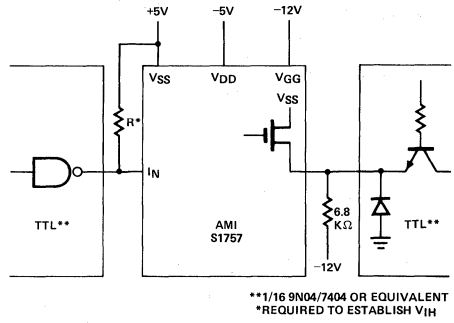
(4)	$I_{\overline{RDE}}$	RECEIVED DATA ENABLE. V_{IL} enables the received data output lines.
(13)	O_{PE}	RECEIVER PARITY ERROR. Goes to V_{OH} if received data word has a parity error.
(14)	O_{FE}	RECEIVER FRAMING ERROR. Goes to V_{OH} if stop bit (mark) is not detected.
(15)	O_{OR}	RECEIVER OVERRUN. Goes to V_{OH} if previously received character is not read out (O_{DA} not reset) before present character is ready to be transferred to output holding register.
(16)	$I_{\overline{SWE}}$	RECEIVER STATUS WORD ENABLE. V_{IL} enables the status word signals (O_{PE}, O_{DA}, O_{TBMT}, O_{FE}, O_{OR}).
(17)	I_{RCP}	RECEIVER CLOCK LINE. Frequency = 16 X baud rate.
(18)	$I_{\overline{RDA}}$	RESET DATA AVAILABLE. V_{IL} resets output O_{DA}.
(19)	O_{DA}	RECEIVED DATA AVAILABLE. V_{OH} indicates a character has been received and transferred to the output holding register.
(20)	I_{SI}	RECEIVER SERIAL INPUT. Accepts transmitted data. When data is not being transmitted, this line must be held high.
(21)	I_{XR}	EXTERNAL RESET. V_{IH} resets all registers and sets transmitter serial output to V_{OH}. Should be pulsed after power turn on.
(22)	O_{TBMT}	TRANSMITTER INPUT HOLDING REGISTER EMPTY. Goes to V_{OH} when a new data word may be loaded into transmitter.
(23)	$I_{\overline{DS}}$	TRANSMITTER DATA WORD INPUT STROBE. V_{IL} enters data into the input holding register. Transition to V_{IH} causes start bit on O_{SO} at next negative clock transition.
(24)	O_{EOC}	TRANSMITTER END OF CHARACTER FLAG. A V_{OL} to V_{OH} transition indicates transmission of a character and stop bits has been completed. V_{OH} is maintained until the mark to space transition of the start bit of a new character transmission.
(25)	O_{SO}	SERIAL TRANSMITTER OUTPUT. Character to be transmitted is shifted out serially on this output. Returns to V_{OH} during idle time.
(26) – (33)	I_{DB}	TRANSMITTER DATA INPUTS. V_{IH} causes mark to be transmitted. I_{DB1} is LSB regardless of length of data word.
(34)	I_{CS}	TRANSMITTER MODE CONTROL STROBE. V_{IH} enters I_{PS}, I_{NB1}, I_{NB2}, I_{2SB}, I_{NP} data into the control bits holding register. Can be strobed or hard wired to V_{IH}.
(35)	I_{NP}	TRANSMITTER/RECEIVER NO PARITY CONTROL. V_{IH} eliminates parity bit from transmitted data and disables the receiver parity check. Stop bits directly follow the data bits. V_{IH} forces O_{PE} to V_{IL}.
(36)	I_{2SB}	TRANSMITTER STOP BIT CONTROL. V_{IL} causes 1 stop bit to be transmitted. V_{IH} causes 2 stop bits to be transmitted.
(37) (38)	I_{NB2} I_{NB1}	TRANSMITTER/RECEIVER DATA BITS PER CHARACTER CONTROL. Selects character length per the following table.

I_{NB2}	I_{NB1}	BITS/CHARACTER
V_{IL}	V_{IL}	5
V_{IL}	V_{IH}	6
V_{IH}	V_{IL}	7
V_{IH}	V_{IH}	8

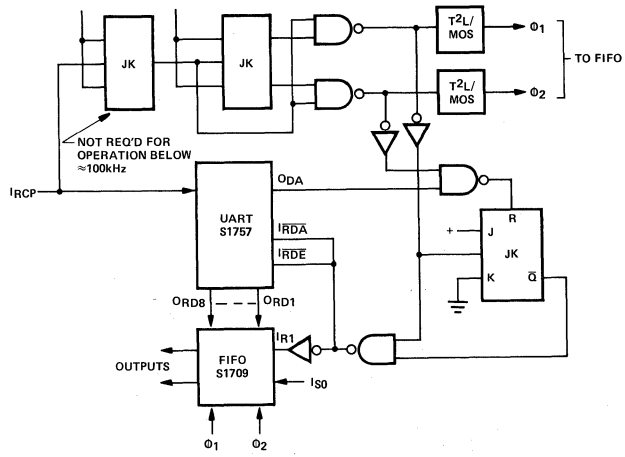
PIN DEFINITIONS (Continued)

(39) I_{PS} TRANSMITTER/RECEIVER PARITY SELECT. Determines transmitted parity and expected parity of receiver. Parity bit follows data bits in transmission. V_{IL} inserts and checks odd parity. V_{IH} inserts and checks even parity.

(40) I_{TCP} TRANSMITTER CLOCK LINE. Frequency = 16 X baud rate.



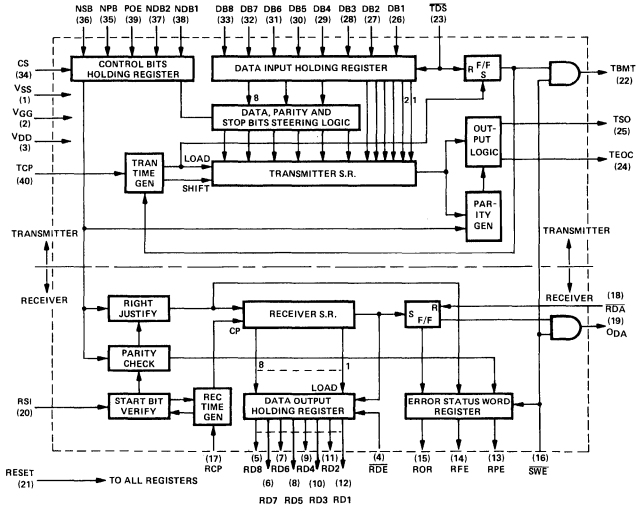
TTL CONNECTION



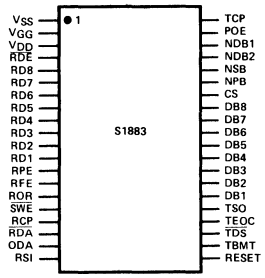
TYPICAL UART——►FIFO INTERFACE
TO BUFFER DATA OUTPUTS

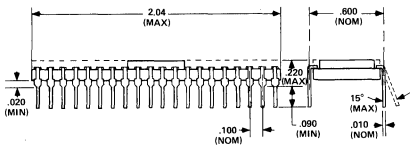
S1883

UART



S1883 BLOCK DIAGRAM





PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

FEATURES

- 12.5 Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission.

The parity bit is removed, checked and an error flag set if incorrectly received.

The data or baud rate at the receiver input and transmitter output are determined independently by external clock inputs. The clock inputs must be 16 times the data rate required at the serial input and output. The independent clocks allow for either half or full duplex operation.

The UART provides a buffer register in both the transmitter and receiver to allow a full character time for responding to a received data ready or transmit data request signal. The UART generates a MARK signal if the transmit register is not loaded with a data character and also indicates an overflow error if two characters are received without a RDA input.

TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- Industrial Data Transmission
- TTY Terminals
- Time Division Multiplexing

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on Any Pin with Respect to V_{SS}	+.3 Volt
Negative Voltage on Any Pin with Respect to V_{SS}	−20.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS

$T_A = 0° - +70°C$, $V_{SS} = +5$ Volt ±5%, $V_{GG} = -12$ Volt ±5%

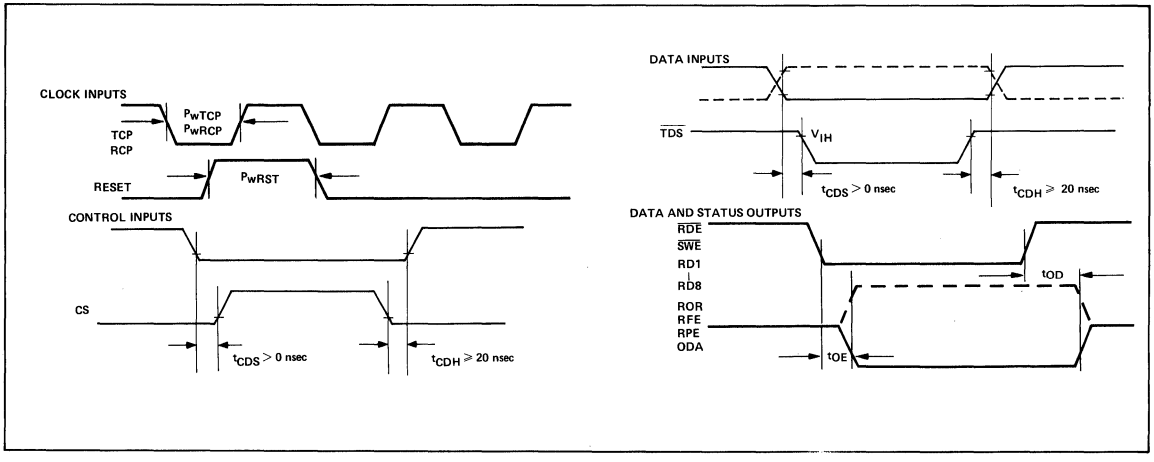
Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	V_{SS} -1.0	V_{SS} +0.3	Volt	Internal Pull-up
V_{IL}	Input Low Voltage	V_{GG}	0.8	Volt	Resistor Provided
I_{LI}	Input Load Current		-1.2	mamp	V_{IN} = 0 Volt
V_{OH}	Output High Voltage	2.4		Volt	I_{OH} = - 100 uamp
V_{OL}	Output Low Voltage		.4	Volt	I_{OL} = 1.6 mamp
C_{IN}	Input Capacitance		20	pf	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance		10	pf	$V_{OUT} = V_{SS}$
I_{SS}	V_{SS} Supply Current		30	mamp	$\overline{SWE} = \overline{RDE} = V_{IL}$
I_{GG}	V_{GG} Supply Current		40	mamp	ITTL Load

AC (DYNAMIC) CHARACTERISTICS

$T_A = 0°C - +70°C$; $V_{SS} = +5$ Volt ±5%; $V_{GG} = -12$ Volt ±5%

Symbol	Parameter	Min	Max	Unit	Condition
TCP, RCP	Clock Frequency	DC	200	KHz	
Input Pulse Widths					
PWTCP	Transmit Clock	2.5		usec	$C_L = 20pf$
PWRCP	Receive Clock	2.5		usec	1 TTL Load
PWCS	Control Strobe	250		nsec	
PWTDS	Transmit Data Strobe	250		nsec	
PWRST	RESET	1.0		μsec	
PWSWE	Status Word Enable	500		nsec	
PWRDA	Reset Data Available	500		nsec	
PWRDE	Receive Data Enable	250		nsec	
Switching Characteristics					
t_{CDS}	Control Set Up Time	0		nsec	Figure 1
t_{CDH}	Control Hold Time	20		nsec	Figure 1
t_{OE}	Output Enable Time		500	nsec	
t_{OD}	Output Disable Time		500	nsec	

TIMING WAVE FORMS (Figure 1)



PIN DEFINITIONS

Pin	Label	Function
(1)	V_{SS}	+5 Volt ± 5%
(2)	V_{GG}	−12 Volt ± 5%
(3)	V_{DD}	Ground
(21)	RESET	A $_{IH}$ resets all internal registers and counters. The transmitter status outputs TBMT and TEOC are set to V_{OH} indicating the input transmitter buffer register is empty. The TSO output generates V_{OH} or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the V_{OL} state.
(38)	NDB1	Number Data Bits/Character
(37)	NDB2	Number Data Bits/Character
(36)	NSB	Number Stop Bits The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs. The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.

NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS
V_{IL}	V_{IL}	V_{IL}	5	1
V_{IL}	V_{IL}	V_{IH}	6	1
V_{IL}	V_{IH}	V_{IL}	7	1
V_{IL}	V_{IH}	V_{IH}	8	1
V_{IH}	V_{IL}	V_{IL}	5	1.5
V_{IH}	V_{IL}	V_{IH}	6	2
V_{IH}	V_{IH}	V_{IL}	7	2
V_{IH}	V_{IH}	V_{IH}	8	2

(35)	NPB	NO PARITY BIT. A V_{IH} eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a V_{OL} condition.
(39)	POE	PARITY ODD/EVEN. If the NPB input is V_{IL}, the parity mode is ODD if POE is V_{IL} and EVEN if POE is V_{IH}. The parity mode is the same for both the transmitter and receiver.
(34)	CS	CONTROL STROBE. A V_{IH} loads POE, NDB1, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER. To load the control inputs for static operation CS can be hard-wired to V_{IH}.
(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT
(27)	DB2	HOLDING REGISTER by $\overline{TDS}$.
(28)	DB3	Input data is assumed right justified so DB1 is always the least significant bit and is the bit
(29)	DB4	
(30)	DB5	

(31) (32) (33)	DB6 DB7 DB8	transmitted following the START bit. For data words less than eight bits, the unused bits are don't care inputs.
(23)	$\overline{TDS}$	TRANSMITTER DATA STROBE. A V_{IL} enters data on the DB1-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at V_{OH}, the START bit will be generated on the first negative transition of the input clock TCP following the return of $\overline{TDS}$ to a V_{IH} state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is V_{OH} (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A V_{OH} indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT(S)) is available to load the next character. If a $\overline{TDS}$ is not generated within the time allotted, the TSO output will go into an idle state of V_{OH} or a MARK condition. TBMT will remain in the tri state mode unless $\overline{SWE}$ is a U_{ZL}.
(24)	TEOC	TRANSMITTER END OF CHARACTER. A V_{OL} to V_{OH} transition indicates the transmission of the character and stop bits have been completed. The V_{OH} is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSI.
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The V_{IH} to V_{IL} (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.
(12) (11) (10) (9) (8) (7) (6) (5)	RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are active only when $\overline{RDE}$ is a V_{IL}. The eight data outputs are in a tri-state mode if $\overline{RDE}$ is a V_{IH}. Data is presented at the outputs right justified with RDI the least significant bit. For data word lengths less than 8 bits the unused bits will appear as V_{OL}.
(4)	$\overline{RDE}$	RECEIVER DATA ENABLE. A V_{IL} enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD1-RD8 the RDE input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A V_{OH} indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

For contiguous data inputs on RSI data will remain in the holding register one character time before being lost.

(18) $\overline{RDA}$ RESET DATA AVAILABLE. A V_{IL} resets the ODA to a V_{OL}. If ODA is not reset by $\overline{RDA}$ the ROR will be set when the next complete character is received and transferred to the DATA OUTPUT HOLDING REGISTER.

(15) ROR RECEIVER OVERRUN. A V_{OH} indicates a second character has been received and transferred to the DATA OUTPUT HOLDING REGISTER without an intervening $\overline{RDA}$. If the previously received character has not been unloaded from the register the next character will be loaded and the first character lost. ROR will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

(14) RFE RECEIVER FRAMING ERROR. A V_{OH} indicates a correct STOP bit was not received following the START bit and correct number of data bits. RFE will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

(13) RPE RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character does not compare with the parity mode set by POE. RPE will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

(16) $\overline{SWE}$ STATUS WORD ENABLE. A V_{IL} enables the status outputs ODA, ROR, RFE, RPE and TBMT on the respective output lines. When $\overline{SWE}$ is V_{IH} all status outputs are in the tri-state mode.
For output configurations not requiring a tri-state condition for the status outputs, $\overline{SWE}$ may be tied directly to ground.

APPLICATION DATA

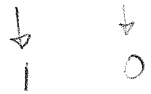
Asynchronous data communications is typified by low data rates, non-contiguous data messages, and a MARK condition on the line between characters. As a result, each data character must be framed for recognition by START and STOP bits. The S1883 UART provides all the logic required to provide a complete full-duplex (transmit and receive simultaneously) asynchronous communication channel for baud rates up to 9600 bps. Included in the S1883 capabilities are; automatic START and STOP bit generation and detection; PARITY generation and detection on variable length characters; tri-state outputs for data and status for data bus configurations, double buffering for less critical timing, and a receiver allowing acceptance of data with up to 42% distortion.

RECEIVER OPERATION

Asynchronous communication line discipline dictates that each character, regardless of width, must be preceded by a START bit. The receiver input logic detects the V_{IH} to V_{IL} (MARK to SPACE) transition on the RSI line that is the leading edge of the START bit. For one half bit time after the leading edge, RSI is sampled for a V_{IL} to insure a proper START bit was present. The following data bits are then clocked into the receiver in the center of each bit period. If RSI returns to the V_{IH} condition before the mid-point of the START bit, the receiver returns to a search for a MARK to SPACE transition.

If at the time of transfer ODA has not been reset by a $\overline{RDA}$, indicating the previous character has not been read, the ROR error flag is set to V_{OH}. The previous data character and status will be lost as the new character is loaded. One full character time is available, assuming contiguous data input at RSI, after ODA is set to read the output character. The data is available at the outputs RD1-RD8 right justified with RD1 the least significant bit. For character widths less than 8 bits the unused outputs are forced to V_{OL}.

For data bus configurations the output data and status are tri-state lines enabled by $\overline{RDE}$ and $\overline{SWE}$ respectively. For polled systems $\overline{SWE}$ can be strobed for detection of ODA and error conditions prior to reading data. For interrupt driven systems $\overline{SWE}$ can be tied directly to ground and ODA used as a data ready interrupt input. A minimum of one character time



is available to test the remaining error status bits and input the data character. Typically the same signal can be used for $\overline{RDE}$ and $\overline{RDA}$.

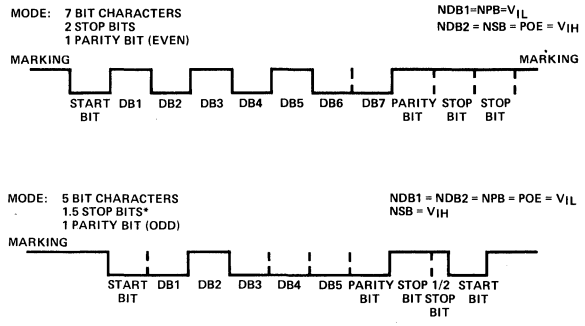
TRANSMITTER OPERATION

The transmit section of the S1883 is reset to a MARK condition with V_{OH} on TSO after receiving a pulse on RESET. Additionally, the transmitter is reset to a character request mode with TBMT and TEOC both at V_{OH}. If the character format is not static, the word length NDB1 and NDB2, parity mode NPB and POE, and number of stop bits NSB should be strobed into the UART with CS.

If both the DATA INPUT HOLDING REGISTER and the TRANSMITTER SHIFT REGISTER are empty the transmitter is in the idle state with TSO, TBMT and TEOC all at V_{OH}. The START bit for a data character loaded with a $\overline{TDS}$ pulse during the idle state is generated at the first negative transition of the TCP following the trailing edge of $\overline{TDS}$. TBMT goes to V_{OL} with the first $\overline{TDS}$. As soon as the character is transferred from the INPUT HOLDING REGISTER to the SHIFT REGISTER, TBMT returns to a V_{OH} and a second character can be loaded. Each character is transmitted with a START bit and 1, 1.5 or 2 stop bits controlled by the respective inputs.

The TEOC is set to V_{OH} after the generation of the last STOP bit indicating the complete character has been transmitted.

TYPICAL DATA FORMAT

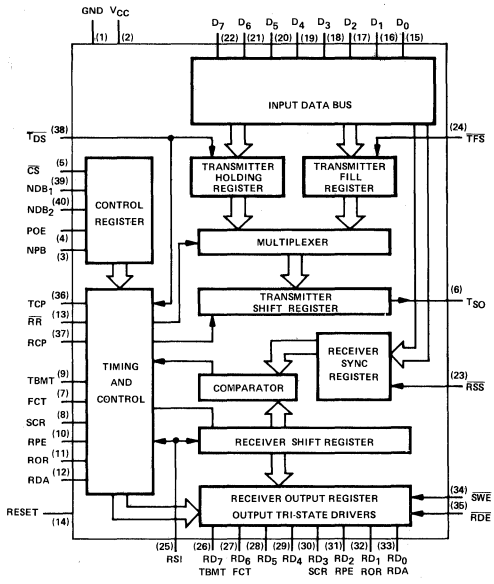


*1.5 stop bits generated only in the 5 bit/character mode.

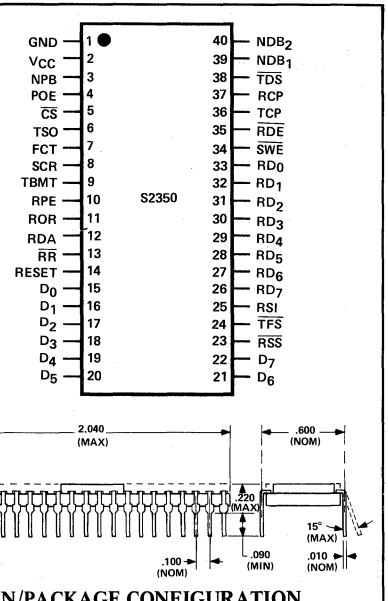
S2350

UNIVERSAL SYNCHRONOUS
RECEIVER/TRANSMITTER (USRT)

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 3M, 1T - see Sec. 1)

FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5–8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character

received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- High Speed Terminals
- Time Division Multiplexing
- Industrial Data Transmission

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	–65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	–0.5 volt
Power dissipation	0.75 watt

DC (STATIC) CHARACTERISTICS*

$T_A = 0° - +70°C$, $V_{CC} = +5$ volts ±5%

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	V_{CC}	Volt	
V_{IL}	Input Low Voltage	- 0.5	+0.8	Volt	
I_{IL}	Input Leakage Current		10	μa	V_{IN} = OTO V_{CC} Volts
V_{OH}	Output High Voltage	2.4		Volts	$I_{OH} = -100\mu a$
V_{OL}	Output Low Voltage		+0.4	Volts	I_{OL} = 1.6ma
C_{IN}	Input Capacitance		10	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
C_{OUT}	Output Capacitance		12	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
I_{CC}	V_{CC} Supply Current		100	ma	No Load

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

AC (DYNAMIC) CHARACTERISTICS

$T_A = 0°C - +70°C$, $V_{CC} = +5$ volts ±5%

Symbol	Parameter	Min.	Max.	Unit	Condition
T_{CP}, R_{CP}	Clock Frequency	DC	500	KHz	

Input Pulse Widths

P_{TCP}	Transmit Clock	900		nsec	C_L = 20pf
P_{RCP}	Receive Clock	900		nsec	1TTL Load
P_{RST}	Reset	500		nsec	
$P_{\overline{TDS}}$	Transmit Data Strobe	200		nsec	
$P_{\overline{TFS}}$	Transmit Fill Strobe	200		nsec	
$P_{\overline{RSS}}$	Receive Sync Strobe	200		nsec	
$P_{\overline{CS}}$	Control Strobe	200		nsec	
$P_{\overline{RDE}}$	Receive Data Enable	400		nsec	Note 1
$P_{\overline{SWE}}$	Status Word Enable	400		nsec	Note 1
$P_{\overline{RR}}$	Receiver Restart	500		nsec	

Switching Characteristics

T_{TSO}	Delay, TCP Clock to Serial Data Out		700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output		1.4	μsec	
T_{TBMT}	Delay, $\overline{TDS}$ to TBMT		700	nsec	
T_{STS}	Delay, $\overline{SWE}$ to Status Reset		700	nsec	
T_{RDO}	Delay, $\overline{SWE}$, $\overline{RDE}$ to Data Outputs		400	nsec	1TTL Load
T_{HRDO}	Hold Time $\overline{SWE}$, $\overline{RDE}$ to Off State		400	nsec	C_L = 130 pf
T_{DTS}	Data Set Up Time $\overline{TDS}$, $\overline{TFS}$, $\overline{RSS}$, $\overline{CS}$	0		nsec	
T_{DTH}	Data Hold Time $\overline{TDS}$	700		nsec	
T_{DTI}	Data Hold Time $\overline{TFS}$, $\overline{RSS}$	200		nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0		nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200		nsec	
T_{RDA}	Delay $\overline{RDE}$ to $\overline{RDA}$ Output	700		nsec	

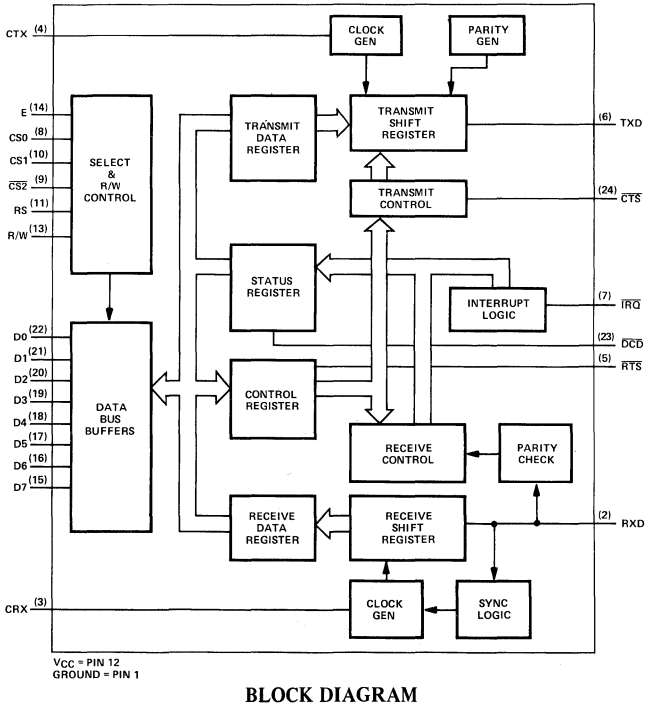
NOTE 1: Required to reset status and flags.

For a Complete Data Sheet See Page 6-63

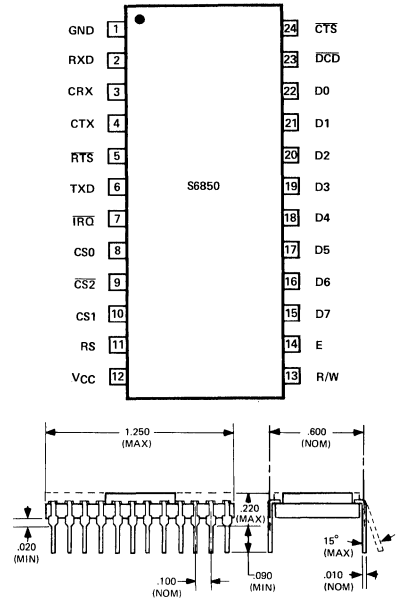
S6850

ASYNCHRONOUS COMMUNICATION
INTERFACE ADAPTER (ACIA)

ADVANCE PRODUCT DESCRIPTION



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkgs. 2L, 1W - see Sec. 1)

FEATURES

- 8 Bit Bidirectional Data Bus for Communication with MPU.
- False start bit deletion.
- Peripheral/modem control functions.
- Double buffered Receiver and Transmitter
- One or two stop bit operation.
- Eight and nine-bit transmission with optional even and odd parity.
- Parity, overrun and framing error checking.
- Programmable control register.
- Optional ÷1, ÷16, and ÷64 clock modes.
- Up to 500,000 bps transmission.

FUNCTIONAL DESCRIPTION

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

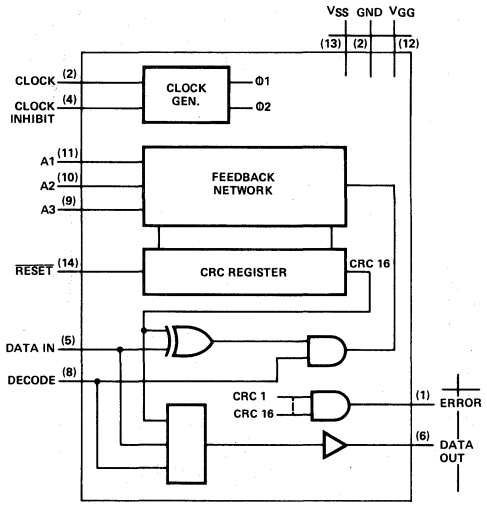
The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

For a Complete Data Sheet See Page 6-53

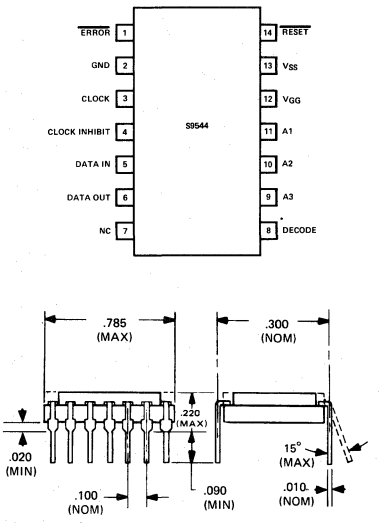
S9544

CRC ENCODER/DECODER

ADVANCED PRODUCT DESCRIPTION



S9544 BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

(Available in Pkgs. 4D, 1D – see Sec. 1)

FEATURES

- Encoder or Decoder
- Fast Data Rates – 1.0 MHz
- TTL Compatible – All Inputs and Outputs
- 14 Lead Dual In-Line Package
- Eight Generating Polynomials
  Including CRC 12, CRC 16, CCITT, SDLC, LRC, ISO

FUNCTIONAL DESCRIPTION

The S9544 can perform either Cyclic Redundancy Checking (CRC) or Longitudinal Redundancy Checking (LRC) for error detection with a selection of eight generating polynomials on serially transmitted digital data. The polynomial selection is accomplished with three programmable inputs. Operation as an encoder or decoder is selected by a single control input.

As an encoder, the S9544 divides the output data by the selected polynomial and transmits the remainder as the lower order bits of the message. As a decoder, the S9544 divides the serial data by the selected polynomial and indicates a zero remainder if no transmission error has occured.

The S9544 is fully TTL compatible at all inputs and outputs and will provide error detection at data rates to 1.0 MHz.

TYPICAL APPLICATIONS

- Tape Cassettes
- Floppy Discs
- Data Communications
  ASCII EBCDIC

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on Any Pin with Respect to V_{SS}	+.3 Volt
Negative Voltage on Any Pin with Respect to V_{SS}	−20.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS

V_{SS} = +5 Volt ±5%; V_{GG} = −12 volt ±5%; T_A = 0°C to +70°C

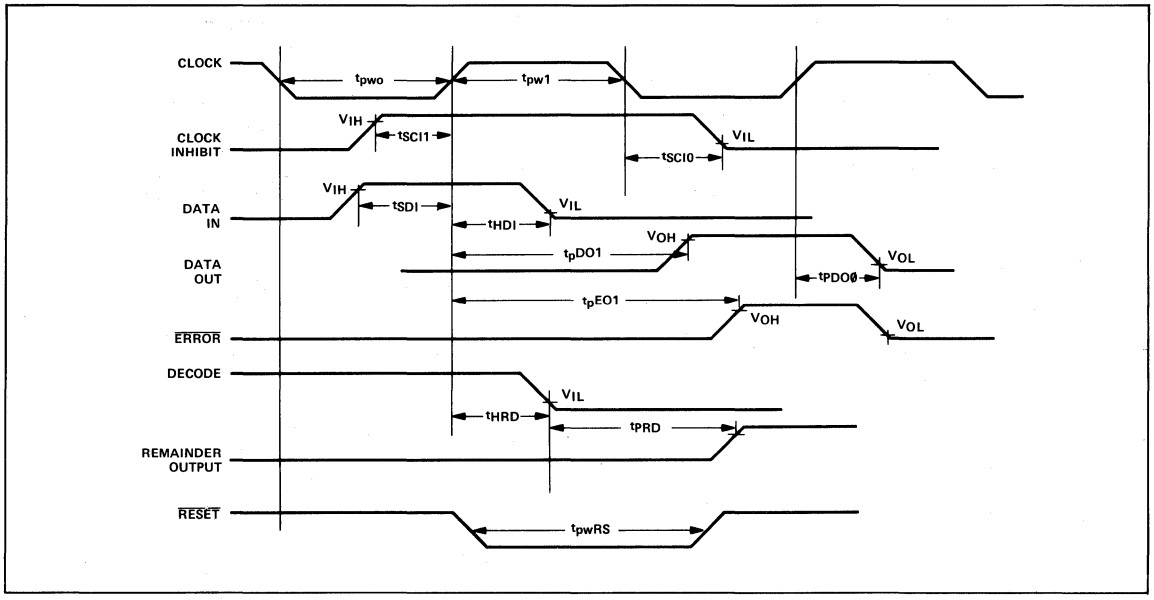
Symbol	Parameter	Min	Max	Unit	Condition
V_{IL}	Input Low Voltage	0	+.8	Volt	Internal Pull-up Resistor
V_{IH}	Input High Voltage	V_{SS} −1.0	V_{SS} +.3	Volt	Provided
I_{LI}	Input Load Current		−1.2	mA	V_{IL} = 0 Volt
V_{OL}	Output Low Voltage		.4	Volt	I_{OL} = 1.6ma
V_{OH}	Output High Voltage	2.4	–	Volt	I_{OH} = −40μa
I_{SS}	Power Supply Current		45	mA	Pin (3) (4) (14) @ V_{GG}. All other inputs @ V_{SS}.
I_{GG}	Power Supply Current		45	mA	V_{SS} = 5.25 Volt, V_{GG} = −12.6 Volt.

AC (DYNAMIC) CHARACTERISTICS

V_{SS} = +5.0V ± 5%; V_{GG} = −12.0 Volt ± 5%; T_A = 0°C to +70°C

Symbol	Parameter	Min	Max	Unit	Condition
$t_{pW}0$, $t_{pW}1$	Clock Pulse Width	500	DC	nsec	C_{LOAD} = 20pf
t_{SCI1}	Set Up Time for Clock Inhibit	200		nsec	and 1 TTL input.
t_{SC10}	Set Up Time for Clock Inhibit	200		nsec	
t_{SDI}	Set Up Time for Data Input	350		nsec	
t_{HDI}	Hold Time for Data Input	150		nsec	
$t_{p}DO0$	Propagation Delay Clock to Data Output	100	300	nsec	
$t_{p}DO1$	Propagation Delay Clock to Data Output		200	nsec	
t_{PEO1}	Propagation Delay Clock to Error Output		300	nsec	
t_{PWRS}	Reset Pulse Width	500		nsec	
t_{HRD}	Hold Time for Decode/Remainder	200		nsec	
t_{PRD}	Propagation Delay Remainder Output		600	nsec	

TIMING CHARACTERISTICS



APPLICATION DATA

Pin Number	Label	Function
(13)	V_{SS}	+5.0 ± 5% Volts
(2)	GND	Ground
(12)	V_{GG}	−12.0 ± 5% Volts
(3)	Clock	Input clock. Generates two phase non-overlapping internal clock. A V_{IL} generates Ø1; V_{IH} generates Ø2.
(4)	Clock Inhibit	A V_{IH} inhibits internal clock change regardless of CLOCK inputs. Input state is held in Ø1. A V_{IL} allows generation of internal clock.
(14)	$\overline{\text{Reset}}$	A V_{IL} causes the CRC register to reset to the all zero condition.
(1)	$\overline{\text{Error}}$	A V_{OL} is indicated if any stage of the CRC register is not a logic zero; e.g., a non-zero remainder as the result of a decode operation.
(8)	Decode	A V_{IH} causes the input data to be routed through the CRC register and divided by the selected generating polynomial in either the encode or decode mode. At the end of the message, a V_{IL} causes the CRC register feedback to be inhibited and the CRC register content, remainder, to be clocked out. After clocking the remainder out, the CRC is left in the reset state; i.e., all logic zero.

APPLICATION DATA (Cont.)

Pin Number	Label	Function
(11)	A1	The three address inputs allow selection of one of eight generating polynomials.
(10)	A2	
(9)	A3	

A1	A2	A3		
V_{IL}	V_{IL}	V_{IL}	$X^{16} + X^{15} + X^2 + 1$	CR16
V_{IL}	V_{IL}	V_{IH}	$X^{16} + X^{12} + X^5 + 1$	CCITT
V_{IL}	V_{IH}	V_{IL}	$X^{16} + X^{15} + X^{10} + X^6 + X^5 + 1$	CCITT
V_{IL}	V_{IH}	V_{IH}	$X^{16} + X^{15} + X^{13} + X^7 + X^4 + X^2 + X + 1$	
V_{IH}	V_{IL}	V_{IL}	$X^{14} + X^2 + X + 1$	ISO
V_{IH}	V_{IL}	V_{IH}	$X^8 + X^7 + X^2 + 1$	
V_{IH}	V_{IH}	V_{IL}	$X^{12} + X^{11} + X^3 + X^2 + X + 1$	CRI2
V_{IH}	V_{IH}	V_{IH}	$X^8 + 1$	BCC

OPERATION

To ensure reliable transmission of binary data over communication facilities or from magnetic storage media, it is necessary to transmit redundant checking information. The redundant check bits added at the transmission source are compared to similarly derived check bits at the receiving end to determine if errors have occured in the data storage transmission.

A binary sequence of data can be represented in polynomial form, e.g.

The binary sequence

1 0 1 1 0 0 1 1 1 0 1

could represent the polynomial

$$G(x) = 1 \cdot X^{10} + 0 \cdot X^9 + 1 \cdot X^8 + 1 \cdot X^7 + 0 \cdot X^6 + 0 \cdot X^5 + 1 \cdot X^4 + 1 \cdot X^3 + 1 \cdot X^2 + 0 \cdot X + 1$$
$$G(x) = X^{10} + X^8 + X^7 + X^4 + X^3 + X^2 + 1$$

The check bits added to the transmitted data are the coefficients of the remainder obtained when the binary transmitted data are divided, modulo 2, by the generating polynomial selected. The total message transmitted is again divided at the receiver by the same generating polynomial, a non-zero remainder at the receiver indicates a transmission error has occurred and retransmission of the data is required.

ENCODING OPERATION

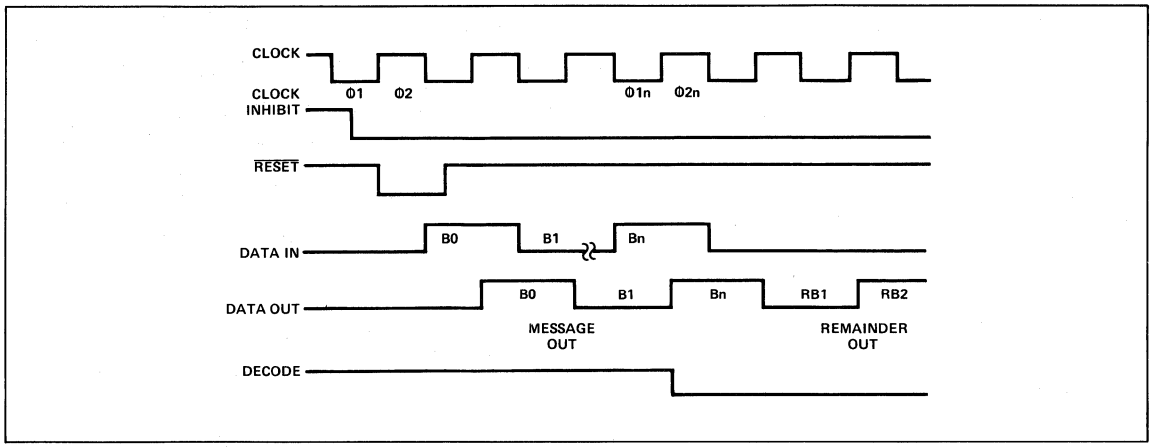
The S9544 with a V_{IH} applied to the DECODE input operates in an encoding mode by dividing the input data by the selected generating polynomial. The check character is transmitted as the remainder by bringing DECODE to V_{IL} at end of the message.

To initiate the correct data transmission, a V_{IL} is applied to CLOCK INHIBIT during the negative duration (internal $\phi 1$) of the clock. A V_{IL} is then applied to the $\overline{\text{RESET}}$ during the succeeding positive clock duration (internal $\phi 2$) to reset the CRC register to the all zeroes condition.

The first data bit is entered at DATA IN during the first negative clock ($\phi 1$) following the $\overline{\text{RESET}}$ pulse and appears at DATA OUT following the positive transition of the clock. Input data continue to be divided Modulo 2 by the selected generating polynomial and also presented at the output. When the last data bit has been entered the DECODE input should be lowered to transmit the accumulated remainder.

The V_{IL} is applied to the DECODE input during the positive clock ($\phi 2$) following the last data bit entry. After sixteen clock periods the CRC register will be in the all zeroes state and the 16 bit check character will have been transmitted.

TIMING DIAGRAM



DECODING OPERATION

The S9544 is used for error detection with the same control and timing as in the encoding mode. The serial data input is applied at DATA IN after bringing DECODE to V_{IH} and a $\overline{\text{RESET}}$ pulse to V_{IL}. After entering the last data bit in the message, the $\overline{\text{ERROR}}$ output will indicate a V_{OL} if any bit in the CRC register is non-zero. This is an indication that the received message is not evenly divisible by the selected polynomial and an error has occurred in the transmission of data.

8

Calculator Circuits

Selection Guide - Calculator Circuits

Part No.	Digits	Output	Memory	%	Const. Factor	Sq. Root	Add Mode	Kbd Type	Micro. Prog.	Int'l Clock	Process	Package	No.of Pkgs.	See Page
CK114	Up to 14	Disp./ Print.	Up to 13	Yes	Yes	Yes	Yes	Alg/Bus	Yes		HI VT	3H,3I,3M	6 to 13	*
CK114P	14	Print	1 or 2	Yes	Yes	Yes	No	Bus.	Yes		HI VT	3H,3I,3M	7	*
CK115P	12	Print	1 or 2	Yes	Yes	Yes	Yes	Bus.	Yes		HI VT	3H,3I,3M	7	*
S2144	8	Disp.	0	No	Yes	No	No	Alg/Bus	No		HI VT	1Z	1	*
S9411	8	Disp.	0	Yes	Yes	No	Yes	Alg.	Yes	Yes	P-SiGate	1Z	1	8-3
S9412A	8	Disp.	1	Yes	Yes	No	Yes	Alg.	Yes	Yes	P-SiGate	1T	1	8-14
S9412B(1)	8	Disp.	1	Yes	Yes	Yes	Yes	Alg.	Yes	Yes	P-SiGate	1T	1	8-14
S9412C(2)	8	Disp.	1	Yes	Yes	Yes	Yes	Alg.	Yes	Yes	P-SiGate	1T	1	8-14
S9413	10	Disp.	1	Yes	Yes	No	No	Alg.	Yes	Yes	P-SiGate	1T	1	*
S9414A	12	Disp.	1	Yes	Yes	No	Yes	Bus.	Yes	Yes	P-SiGate	1T	1	8-15
S9414B(3)	12	Disp.	1	Yes	Yes	No	Yes	Bus.	Yes	Yes	P-SiGate	1T	1	8-15
S9651(4)	10(5)	Disp.	1	No	Yes	Yes	No	Alg.	Yes	Yes	P-SiGate	1T	1	8-16
S2299(6)	N/A	BCD	0	NA	NA	NA	NA	Prog.	Yes	No	HIVT	1T	1	6-80
9209	8-12	Disp.	1	(7)	(7)	(7)	(7)	Prog.	Yes	Yes	P-SiGate	1T	1	6-73

***Contact your nearest AMI Sales Office for additional data sheet information on this product (See Section 1)**

Notes: *(1) Additional features – Mark-up, Percentage Difference, Exchange, Change sign, and Pi (π).*

(2) Additional features – All of S9412B, plus Metric Conversions.

(3) Additional features – Mark-up, Percentage Difference, Item count and average.

(4) Additional features – Pi (π), Change sign, Square root, Reciprocal, Square, Register exchange, Memory exchange – Scientific notation or floating input and output.

(5) Scientific notation – 8 Digit mantissa, 2 Digit exponent.

(6) Keyboard buffer – 7-key buffer for use with S9xxx devices above.

(7) Number of digits, features, and keyboard are all microprogrammable.

The following Application Notes are available from your nearest AMI Sales Office:

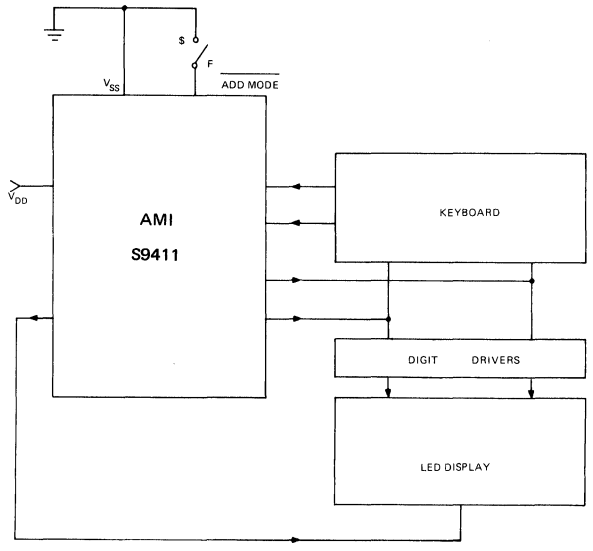
AP75-4A Eight-digit, 5-function Calculator, with LED Display, Using S9411.

AP74-5 Eight-digit Multifunction Calculator, with LED Display, Using S9412.

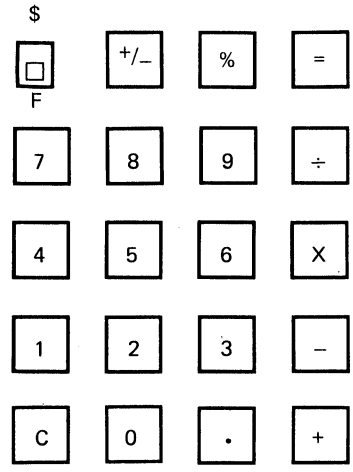
AP74-6 Eight-digit Multifunction Calculator, with Fluorescent Display, Using S9412.

S9411

CALCULATOR



BLOCK DIAGRAM



TYPICAL KEYBOARD

FEATURES

- Five function (+, –, x, ÷, %), 8 digit display.
- Percent discount and percent add-on.
- Automatic constant factor on all five functions.
- Algebraic keyboard with full chaining.
- Floating decimal mode.
- Add mode.
- Change sign key.
- Decimal wraparound on overflow.
- Automatic power-on clear.
- Leading zero suppression.
- True credit balance format.
- Outputs drive LED segments directly.
- Clock generator is integral to chip.
- Suitable for use with LED or fluorescent displays

FUNCTIONAL DESCRIPTION

The AMI S9411 Calculator chip is a five function eight digit display calculator constructed on a single MOS/LSI chip. Inputs to the S9411 are received from a 10 x 2 keyboard switch matrix with internal encoding and debouncing. The display outputs consist of seven segment outputs, decimal point, nine digit select signals.

KEYBOARD DESCRIPTION

Equals Key (=)

Perform previous operation and displays result.
Establishes constant factor mode with stored multiplicand, divisor, addend or subtrahend.
Performs constant factor operation if in constant factor mode.
Conditions calculator for new problem.

Multiplication Key (x)

Enters multiplicand.
Performs previous operation and displays result.
Conditions machine to multiply.

Division Key (÷)

Enters dividend.
Performs previous operation and displays result.
Conditions machine to divide.

Addition Key (+)

Performs previous operation and displays result.
Conditions machine for an addition.
If the "+" immediately follows a "%" (no digit entry in between), the stored multiplicand of the percent operation will be added to the result of the percent operation and the sum will be displayed. The machine is conditioned for a new problem.

Subtraction Key (–)

Performs previous operation and displays result.
Conditions machine for a subtraction.
If the "–" immediately follows a "%" (no digit entry in between), the result of the percent operation will be subtracted from the stored multiplicand and the difference will be displayed. The machine is conditioned for a new problem.

Percent Key (%)

If conditioned for multiplication, it will perform a percentage multiplication and condition the calculator for constant multiplication.
If conditioned for division, it will cause the quotient to be displayed as a percentage and it will condition the calculator for constant division.
If conditioned for addition or subtraction acts as an "=" key.

Change Sign Key (+/–)

During digit entry changes the sign of the entered factor.
After "=", changes the sign of the answer.

Clear Key (C)

If in the middle of a digit entry, clears the keyboard and the display.
If the error condition is on, clears the error condition only.
At any other time, it clears the keyboard, the display and all chain conditions.

Decimal Mode Switch (F or $)

When in the "F" position, all entries will be displayed as entered. All results will be displayed right justified and floating.

When in the "$" position (Add Mode), the decimal point will be automatically placed between the second and third digits of the display, counting from the right, at the time the first digit is entered. All results will be treated as if there was a decimal point control that was set to "2". Depression of the decimal point key will override the add mode on entry.

OPERATIONAL FEATURES

Automatic Constant

The first factor in a multiplication calculation or the second factor in a division, addition or subtraction calculation is retained as a constant when calculation is terminated by an "=" key or "%" key, except if it is followed by an add-on or discount calculation. Subsequent calculations using the stored constant are performed by following each entry with an"=" or "%" respectively. Repeat add or subtract calculations are performed by depressing "=" after the constant is established.

Power-on Clear

An internal power on clear circuit clears all registers and all constant conditions.

Overflow and Underflow

Overflow locks out all keys except C. Results which cannot be aligned to the decimal setting ($ mode) will cause the fixed decimal setting to be over-ridden and the decimal point will be positioned to accommodate the result (underflow). If the result exceeds the display capacity, the overflow indicator will be illuminated and the decimal point will be positioned to indicate the correct result when the display is multiplied by 10^8. Depression of the C key will extinguish the overflow symbol and allow the result to be used for further calculations.

Calculation Time

Maximum calculation time is 400 milliseconds (LED).

CALCULATION EXAMPLES

The following examples illustrate the operation of the S9411 chip.

PROBLEM	DP	KEY SEQUENCE	DISPLAY
ADDITION AND SUBTRACTION		1.23	1.23
+ 1.23	F	+	1.23
+ 2.5		2.5	2.5
− 1.2325		−	3.73
+ 123.456789		1.2325	1.2325
− 25		+	2.4975
+ 1.23		123.456789	123.45678
+ 102.184289		−	125.95428
		25	25.
		+	100.95428
		1.23	1.23
		=	102.18428
MULTIPLICATION		1.23	1.23
	F	X	1.23
(1.23)(0.456)(7) = 3.92616		.456	0.456
		X	0.56088
		7	7.
		=	3.92616
DIVISION		62.25	62.25
	F	÷	62.25
$\frac{62.25}{(6)(3)}$ = 3.4583333		6	6.
		÷	10.375
		3	3.
		=	3.4583333

PROBLEM	DP	KEY SEQUENCE	DISPLAY
CONSTANT MULTIPLICATION			
3 x 4 = 12	F	3	3.
3 x 7 = 21		X	3.
		4	4.
		=	12.
		7	7.
		=	21.
CONSTANT DIVISION			
12 ÷ 3 = 4	F	12	12.
15 ÷ 3 = 5		÷	12.
		3	3.
		=	4.
		15	15.
		=	5.
CONSTANT ADDITION			
2 + 3 = 5	F	2	2.
6 + 3 = 9		+	2.
8 + 3 + 3 + 3 = 17		3	3.
		=	5.
		6	6.
		=	9.
		8	8.
		=	11.
		=	14.
		=	17.
CONSTANT SUBTRACTION			
10 – 4 = 6	F	10	10.
16 – 4 = 12		–	10.
9 – 4 – 4 – 4 = –3		4	4.
		=	6.
		16	16.
		=	12.
		9	9.
		=	5.
		=	1.
		=	– 3.
CHANGE SIGN			
2 x (–12) = –24	F	2	2.
		X	2.
		12	12.
		+/–	– 12.
		=	– 24.

PROBLEM	DP	KEY SEQUENCE	DISPLAY
CHANGE SIGN $-(2 + 3) \times 4 = -20$	F	2 + 3 = +/– X 4 =	2. 2. 3. 5. – 5. – 5. 4. – 20.
POWER $(2)^4 = 16$	F	2 X = = =	2. 2. 4. 8. 16.
SQUARING $((3)^2)^2 = 81$	F	3 X = X =	3. 3. 9. 9. 81.
MIXED CALCULATION $\frac{(5.5 \times 3.25) + 10.7}{8.6} = 3.3226744$	F	5.5 X 3.25 + 10.7 ÷ 8.6 =	5.5 5.5 3.25 17.875 10.7 28.575 8.6 3.3226744
PERCENT 120 x 5% = 6.00 120 x 12% = 14.00	F	120 X 5 % 12 %	120. 120. 5. 6. 12. 14.4
ADD-ON 150 + 5.5% of 150 = 158.25	F	150 X 5.5 % +	150. 150. 5.5 8.25 158.25

PROBLEM	DP	KEY SEQUENCE	DISPLAY
DISCOUNT 150 – 5.5% of 150 = 141.75	F	150 X 5.5 % –	150. 150. 5.5 8.25 141.75
ADD MODE 1.25 3.65 .28 5.18	$	125 + 365 + 28 =	1.25 1.25 3.65 4.90 0.28 5.18
UNDERFLOW 123456.78 919191.91 1042648.69	$	12345678 + 91919191 =	123456.78 123456.78 919191.91 1042648.6
OVERFLOW 12345 x 10000 = 123450000	F	12345 X 10000 = C X 3 =	12345. 12345. 10000. ⊏ 1.2345000 1.2345000 1.2345000 3. 3.7035
OVERFLOW 12345678. 12.25 98769876 111115566.25	F	12345678 + 12.25 + 98769876 =	12345678. 12345678. 12.25 12345690. 98769876. ⊏ 1.1111556

ELECTRICAL PARAMETERS

NOTE: All voltages are measured with respect to V_{SS}

Absolute Maximum Ratings

	MIN	MAX	UNIT
Storage Temperature	−55	+125	°C
Operating Temperature	0	+ 55	°C
Maximum Positive Voltage (any pin)		+ 0.3	Volts
Maximum Negative Voltage (any pin)		− 30	Volts
Maximum allowable output current (any pin)		20	mA

Electrical Characteristics

V_{DD} = − 15.0 ± 1.5 V, T_A = 0° to 55°C

	MIN	TYP	MAX	UNIT
Input High Level				
$\overline{NUM}$, $\overline{FUN}$	−2.0		V_{SS}	Volts
ADD MODE	−0.8		V_{SS}	Volts
Input Low Level				
$\overline{NUM}$, $\overline{FUN}$	V_{DD}		−4.6	Volts
ADD MODE	V_{DD}		−8.0	Volts
Clock Input (LED Display)				
CAPACITOR		100		pF
RESISTOR		100		KΩ
Output High Level				
DIGITS (I_D = 2.8 mA)	−1.5		V_{SS}	Volts
SEGMENTS (I_S = 8.0 mA)	−2.0		V_{SS}	Volts
Supply Current		7	12.0	mA

KEYBOARD CHARACTERISTICS

Key contact resistance must be less than 1 KΩ.

Maximum allowable key bounce is 6 ms.

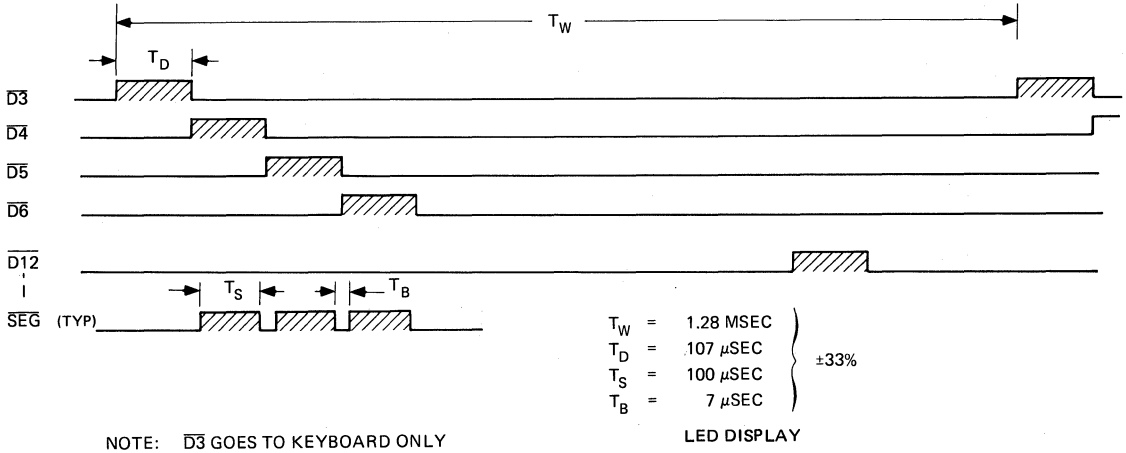
Maximum allowable load capacitance on the keyboard return lines $\overline{NUM}$, $\overline{FUN}$ is 75 pF.

DESCRIPTION OF OUTPUTS

The outputs of the S9411 are designed to drive a 7 segment display of 9 digit positions. This provides eight numeric digits and a ninth digit for display of minus (–), positive overflow (⊏) and negative overflow (E).

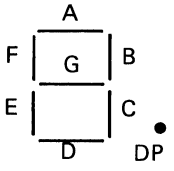
The segment outputs are designed to drive LED segments directly when using LED displays such as Litronix DL-95 or Hewlett-Packard 5082-7449.

The display outputs are in the V_{OH} state (low impedance to V_{SS}) to indicate an ON segment or ON digit.

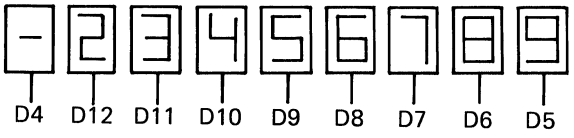


NOTE: $\overline{D3}$ GOES TO KEYBOARD ONLY
$\overline{D4}$ THRU $\overline{D12}$ GO TO KEYBOARD AND DISPLAY
FOR OTHER THAN LED DISPLAY, TIMING IS PROPORTIONAL TO THE VALUE OF THE OSCILLATOR TIMING CAPACITOR

TIMING DIAGRAM

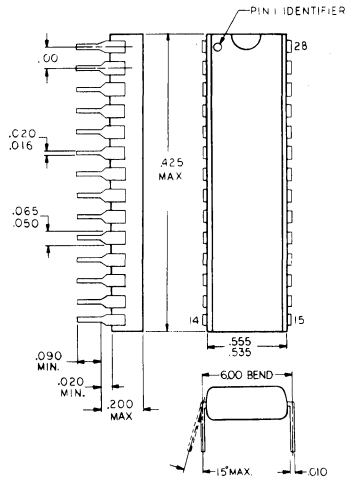


DISPLAY



DIGIT INTERFACE

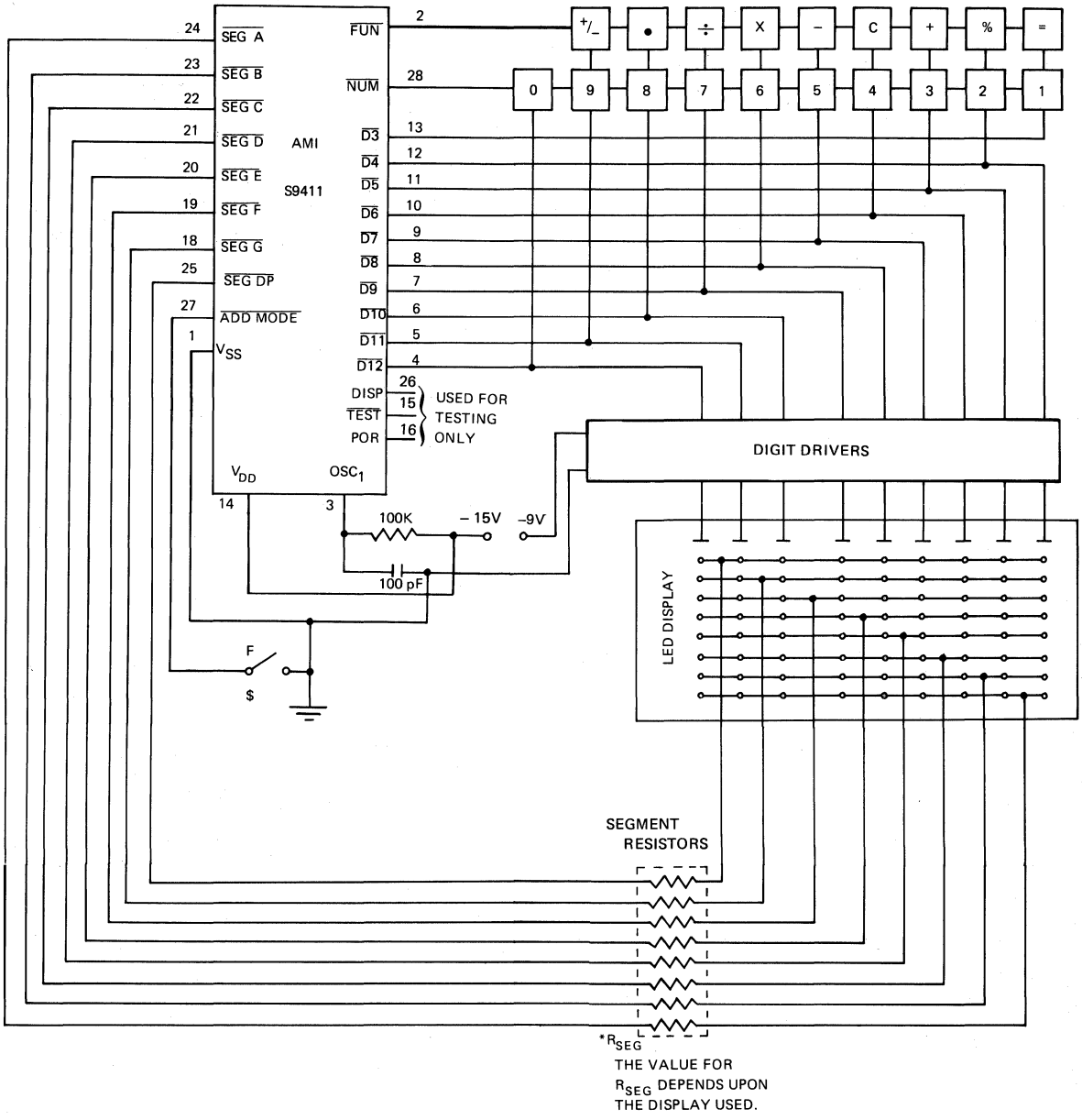
PIN	FUNCTION	PIN	FUNCTION
1	V_{SS}	28	$\overline{NUM}$
2	$\overline{FUN}$	27	$\overline{ADD\ MODE}$
3	OSC1	*26	DISP
4	$\overline{D12}$	25	$\overline{SEG\ DP}$
5	$\overline{D11}$	24	$\overline{SEG\ A}$
6	$\overline{D10}$	23	$\overline{SEG\ B}$
7	$\overline{D9}$	22	$\overline{SEG\ C}$
8	$\overline{D8}$	21	$\overline{SEG\ D}$
9	$\overline{D7}$	20	$\overline{SEG\ E}$
10	$\overline{D6}$	19	$\overline{SEG\ F}$
11	$\overline{D5}$	18	$\overline{SEG\ G}$
12	$\overline{D4}$	**17	N/C
13	$\overline{D3}$	*16	POR
14	V_{DD}	*15	$\overline{TEST}$



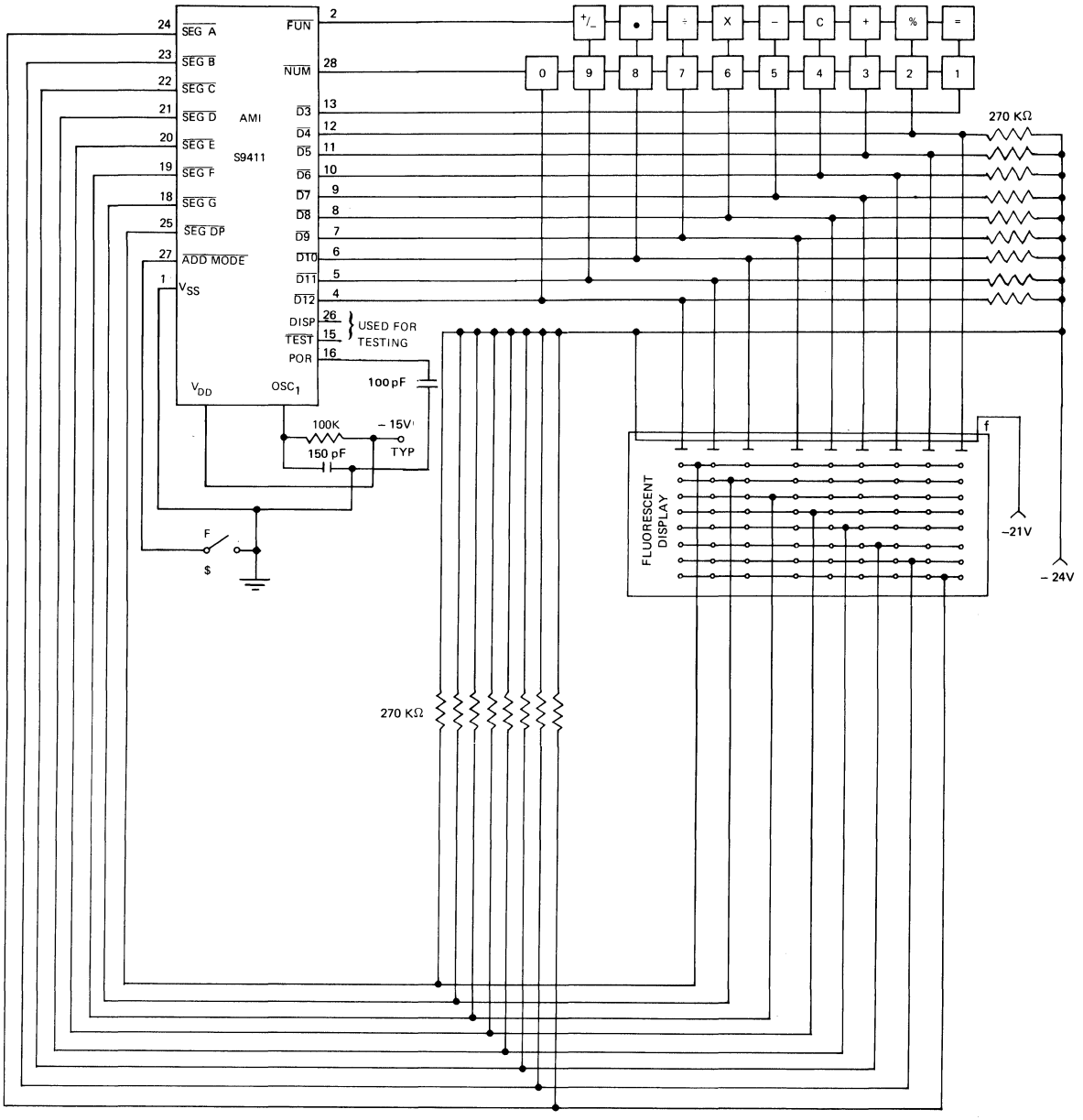
* No Connection – used for test only.

** No Connection

PIN/PACKAGE CONFIGURATION
(Available in Pkg. 1Z – see Sec. 1)



TYPICAL SCHEMATIC DIAGRAM W/LED DISPLAY

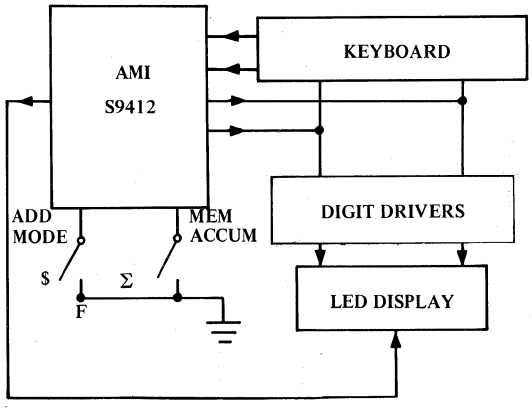


TYPICAL SCHEMATIC DIAGRAM W/FLUORESCENT DISPLAY

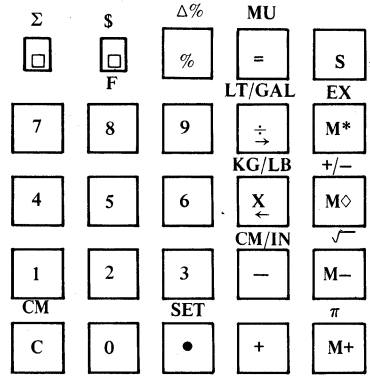
S9412A
S9412B
S9412C

CALCULATOR

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM



S9412C
TYPICAL KEYBOARD

FEATURES

S9412A

- Five function (+, –, X, ÷, %) eight digit display.
- Percent discount and percent add-on.
- Memory with automatic accumulation.
- Memory overflow protection.
- Memory in-use indication.
- Algebraic keyboard with full chaining.
- Automatic constant factor on five functions.
- Floating decimal mode.
- Add mode.
- Decimal wraparound on overflow.
- Leading zero suppression.
- Automatic power-on clear.
- Clock generator is integral to chip.
- Outputs drive LED segments directly.
- Suitable for use with LED, fluorescent or gas discharge displays.

S9412B

(Features in addition to those of the S9412A)

- Square root.
- π entry.
- Percentage mark-up.
- Percentage difference.
- Constant percentage mark-up and percentage difference.
- Register exchange.
- Change sign.
- Memory clear without disturbing display.
- Fixed decimal point with 5/4 rounding.

S9412C

(Features in addition to those of the S9412B)

- Conversion of liters/gallons, kilograms/pounds and centimeters/ inches.
- Constant conversion modes.

FUNCTIONAL DESCRIPTION

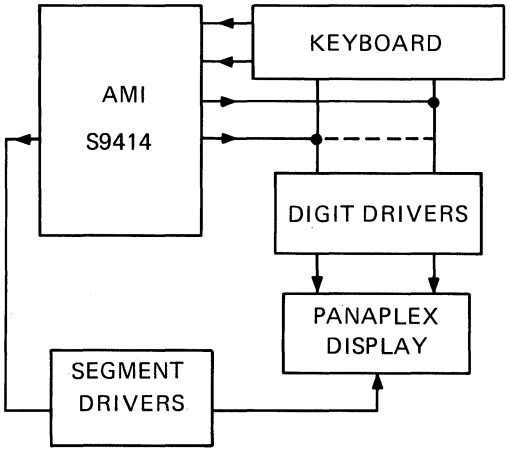
The AMI S9412 Calculator chip is a five function, one memory, eight digit display calculator constructed on a single MOS/LSI chip. Inputs to the S9412 are received from a 10 x 4 keyboard switch matrix with internal encoding and debouncing. The display outputs consist of eight segment outputs, decimal point, and nine digit select signals. Optional versions are available that include many extra functions and metric conversions. (S9412 B, S9412 C)

Contact your AMI Sales Office or fill out the Business Reply Card in this Catalog for additional information on this Product.

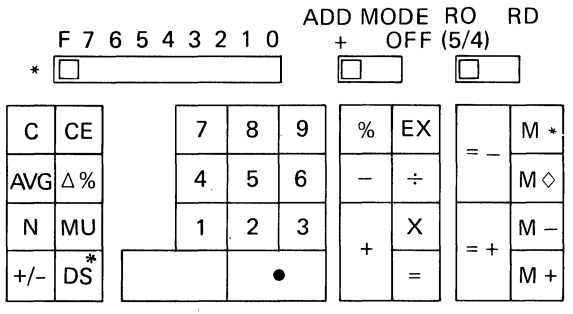
S9414A
S9414B

CALCULATOR

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



*CAN USE EITHER DECIMAL SET KEY, FOLLOWED BY A DIGIT KEY OR DECIMAL SELECTION SWITCH.

S9414B
TYPICAL KEYBOARD

FEATURES

S9414A

- Five function (+, −, X, ÷, %) 12 digit display.
- Percent discount and percent add-on.
- Memory.
- Memory overflow protection.
- Memory in-use indication.
- Arithmetic keyboard with chaining on X and ÷.
- Automatic constant factor on X, ÷, and %.
- Floating decimal input, floating or fixed out.
- Add mode on all decimal settings.
- Decimal wraparound on overflow.
- Leading zero suppression.
- Automatic power-on clear.
- Clock generator is integral to chip.
- Floating minus in display.
- Selectable round off.
- Decimal setting by key or switch.
- Change sign.
- Register exchange.
- Separate equals & accumulate keys.
- Output drives LED segments or fluorescent display directly.

S9414B

(Features in addition to those of the S9414A)

- Item count.
- Averaging.
- Percentage mark-up.
- Percentage difference.
- Constant percentage mark-up and percentage. difference.

FUNCTIONAL DESCRIPTION

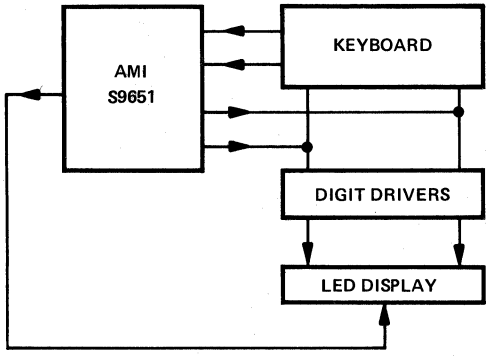
The AMI S9414 Calculator chip is a five function, one memory, 12 digit display calculator constructed on a single MOS/LSI chip. Inputs to the S9414 are received from a 10 x 4 keyboard switch matrix with internal encoding and debouncing.

The display outputs consist of seven segment outputs, decimal point, and 13 digit select signals. An optional version is available that includes many extra functions. (9414B)

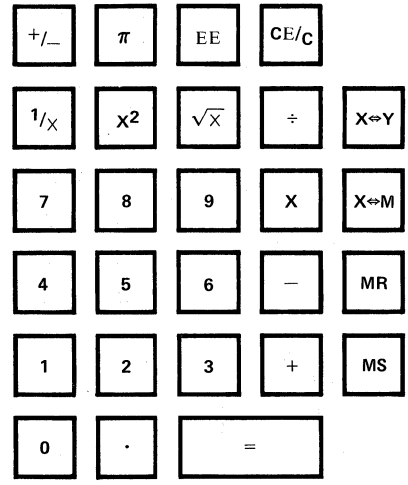
S9651

CALCULATOR

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM



TYPICAL KEYBOARD

FEATURES

- Seven function (+, –, X, ÷, X^2, $\sqrt{x}$, 1/x),12 digit display
- Scientific and floating notation
- Algebraic operation with full chaining
- Automatic four function constant factor
- Independent memory
- Leading zero suppression
- Automatic power-on clear
- Clock generator is integral to chip
- Outputs drive LED segments directly
- π
- Square root
- Square
- Reciprocal
- Memory and display exchange
- Register exchange
- Change sign
- Low battery indicator
- Display time out

FUNCTIONAL DESCRIPTION

The AMI S9651 Calculator chip is a multi-function, one memory, scientific notation (12 digit), display calculator constructed on a single MOS/LSI chip. Inputs to the S9651 are received from a 10 x 4 keyboard switch matrix with internal encoding and debouncing. The display outputs consist of seven segment outputs, decimal point, and 12 digit select signals.

Contact your AMI Sales Office or fill out the Business Reply Card in this Catalog for additional information on this Product.

9

Timing Circuits

(Watches/Clocks/Organs/DVMs)

Future Products

3 1/2 - digit Calendar LED Watch

4/6 - digit Line Clock

Single-chip Top Octave Synthesizer

Selection Guide-Timing Circuits

Part No.	Description	Power Supply (V)	I/O	Power Dis. (mW)	Data Rate (MHz)	Process	Package	See Page
Watch, Clock and DVM Circuits								
S1400	LCD Watch	+1.5	MOS	0.02	0.032	CMOS	(Special)	9-4
S1406	LCD Watch	+1.5	MOS	0.02	0.032	CMOS	Chip Car.	9-9
S1407	LCD Watch	+1.5	MOS	0.02	0.032	CMOS	PC Board	*
S1410	LCD Time/Date/Second Watch(1)	+1.5	MOS	0.01	0.032	CMOS	Chip Carrier	9-10
S1411	LCD Time/Date/Second Watch(1)	+1.5	MOS	0.01	0.032	CMOS	(Chip only)	9-10
S1412	LCD Time/Date/Second Watch	+1.5	MOS	0.02	0.032	CMOS	PC Board	*
S1420	LCD Time/Date/Second Watch(2)	+1.5	MOS	0.01	0.032	CMOS	Chip Carrier	9-14
S1421	LCD Time/Date/Second Watch(2)	+1.5	MOS	0.01	0.032	CMOS	(Chip only)	9-14
S1422	LCD Time/Date/Second Watch	+1.5	MOS	0.02	0.032	CMOS	PC Board	*
S1856	LED/LCD Auto Clk.	+6 to +16	MOS	70	0.256	P-I^2	1T	9-16
S1907A	DVM Counter/Displ.	+9, -9	MOS	50	0.5	P-I^2	1T	9-28
S1998	50/60 Hz Line Clk.	+8 to +29	MOS	300	50 x 10^{-3}	P-I^2	1T	9-21
Organ Circuits								
S2193	7 Stage Freq. Div.	-14, -28	MOS	300	0.1	P-I^2	1D	*
S2470	6 Stage Freq. Div.	-10, -27	MOS	350	0.1	HI V_T	1D	*
S2555	7 Out Freq. Synth.	-15, -27	MOS	400	2.1	HI V_T	1D	*
S2556	6 Out Freq. Synth.	-15, -27	MOS	400	2.1	HI V_T	1D	*
S2566	Rhythm Generator	-15, -27	MOS	300	0.1	HI V_T	1W	*
S2567	Rhythm Counter	-15, -27	MOS	400	0.1	HI V_T	1U	*
S8890	Rhythm Generator	+12	MOS	400		P-I^2	1T	*
S9660	Rhythm Generator	+12	MOS	400		P-I^2	1Z	*

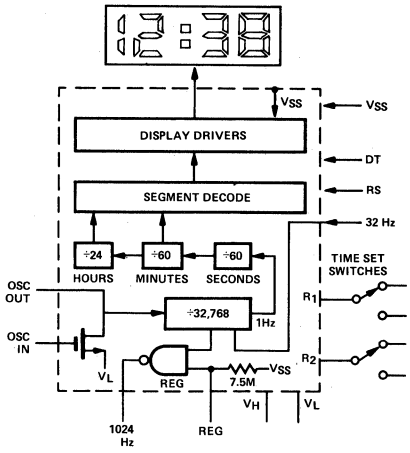
***Contact your nearest AMI Sales Office for additional data sheet information on this product (See Section 1)**

Notes: (1) Six-digit display
(2) Four-digit display

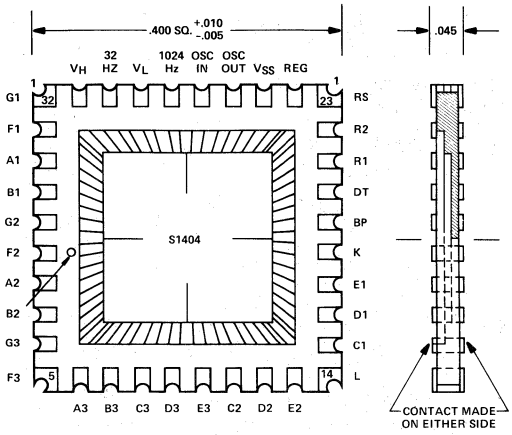
S1400
S1401
S1402
S1403
S1404

LCD WATCH DIVIDER/DRIVER

AMERICAN MICROSYSTEMS, IN



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Single Chip CMOS Construction
- 1024 Hz Upconverter Output
- Internal Voltage Regulator
- Up to 12 Volt Output
- Operates from 1.5V Cell
- 12 or 24 Hour Cycle
- Hours and Minutes Display
- Colon flashes at 1 Hz rate
- 32 Khz Oscillator

FUNCTIONAL DESCRIPTION

The S1400 is a single CMOS circuit that directly replaces currently available two chip systems. The S1400 generates drive signals to a 3½ digit liquid crystal display from a 1.5 volt battery. The circuit provides a 1024 Hz up-converter output and a 32 Hz display output. A flashing colon output is also provided with either a 24 hour or 12 hour display mode. Silicon gate ion implanted complementary MOS technology is used to obtain very low operating power and small circuit size. The display drivers operate from a voltage up to 12 volts generated from coil or transformer up-converter. The high voltage supply can be regulated by an external zener diode reference that gates the 1024 Hz output through the regulator input. Time set logic is provided to advance either the hours or minutes counters at 1 Hz rate. The circuit can be purchased in several standard packages or in a customer supplied special package.

FUNCTIONAL DESCRIPTION

V_{SS} – Positive power supply.

V_L – Negative power supply for dividers and segment decode. Normally at –1.5 Volts.

V_H – Negative segment driver supply. Normally at –7.5 volts.

1024 Hz – Up-converter driver output.

OSC IN – Gate of N channel oscillator device.

OSC OUT – Drain of N channel oscillator device.

AM/B – AM segment drive in 12 hour mode. Segment B drive of MSD in 24 hour mode.

PM/ADEG – PM segment drive in 12 hour mode. MSD segments A, D, E, and G drive in 24 hour mode.

12/24 HR – 12 or 24 hour select. Connection to V_{SS} selects 12 hour mode. Connection to V_L selects 24 hr. This input is wired internally in some package types. Display drive outputs are connected per the diagram below for 12 or 24 hour operation.

REG – May be deleted from circuit if tight voltage regulation not required.

RS – Reset Connection to V_{SS} resets all counters (normally held to V_L by internal resistor).

DT – Display test input. Connection to V_{SS} changes state of all segments (normally held by V_H by internal resistor).

BP – LCD back plane output.

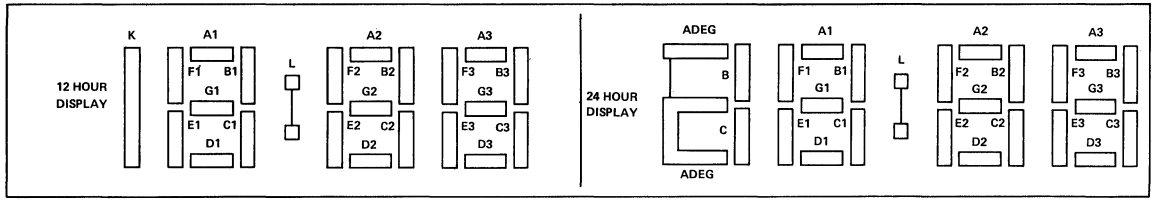
K/C – Most significant digit output in 12 hour mode. Segment C of most significant digit in 24 hour mode.

R1, R2 – Selects operating mode per the following table:

R1*	R2*	OPERATION
V_{SS}	V_{SS}	Normal Mode.
V_{SS}	V_H	Advance Hours only at 1 hour/second.
V_H	V_{SS}	Hold – Hrs. and Minutes. Also resets seconds to zero.
V_H	V_H	Advance Minutes/Hrs. at 1 min/second.

*R_1, R_2 inputs bounce protected by internal latches. Double throw switches are recommended on these inputs.

BP – BACK PLATE (DISPLAY COMMON)



ABSOLUTE MAXIMUM RATINGS

Storage temperature	–55°C to +150°C
Operating ambient temperature	–10°C to +70°C
Maximum supply voltages, V_L	–3V
V_H	–12V
Positive voltage on any pin	V_{SS} +0.3V
Negative voltage on RS, OSC OUT, 1024 Hz, 32 Hz, 12/24 HR	V_L –0.3V
Negative voltage on any other pin	V_H –0.3V

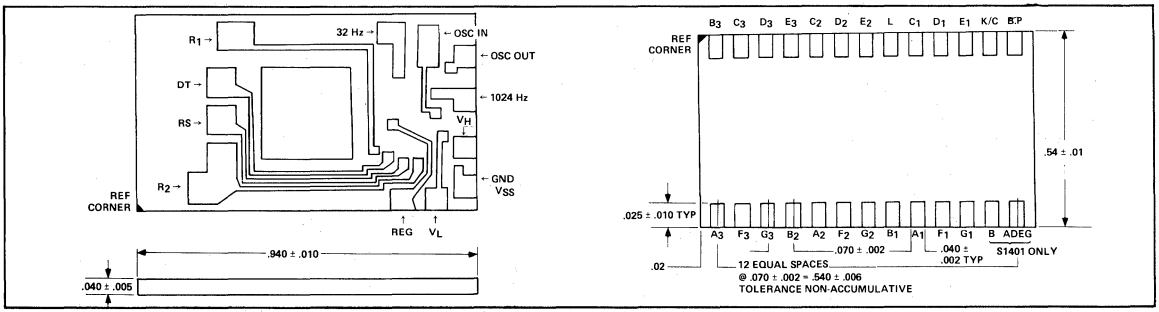
NOTE: Exceeding these voltages may forward bias some internal junctions. This is non-destructive if the current is limited to 0.1 mA.

PACKAGE OPTIONS

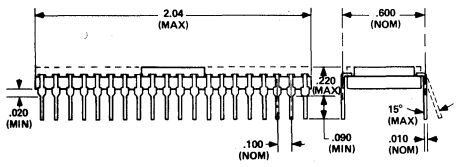
Available packages are listed by part number in the following table. The S1400 package is mechanically compatible with the S23560 LCD. Direct electrical contact between the S1400 and the S23560 is achieved with a suitable connector (see parts list). The S1404 package is particularly suited for modules using a CMOS attached to a PC board. The S1404 can be flow soldered to a board area less than 0.5 inches square with contact to the board made from either side. These features provide maximum module design flexibility.

S1400/S1400A/S1400B	Special Substrate Package 12 Hour Cycle
S1401	Special Substrate Package 24 Hour Cycle (Available by Special Order)
S1402	40 Pin Dip Package 12 or 24 Hour Cycles
S1403	Unpackaged (chip only) version of the S1400
S1404/S1404A/S1404B	36 Lead Chip Carrier

S1400, S1401 PACKAGE



S1402 PACKAGE



PIN	FUNCTION	PIN	FUNCTION
1	V_{SS}	40	F1
2	A1	39	G1
3	B1	38	AM/B*
4	G2	37	PM/ADEG*
5	F2	36	V_H
6	A2	35	32 Hz
7	B2	34	V_L
8	G3	33	12/24 HOUR (V_{SS} FOR 12 HR.)
9	F3	32	1024 Hz
10	A3	31	OSC IN
11	B3	30	OSC OUT
12	C3	29	REG
13	D3	28	RS
14	E3	27	R2
15	C2	26	R1
16	NO CONNECT	25	DT
17	D2	24	BP
18	E2	23	K/C*
19	L	22	E1
20	C1	21	D1

*12 HR. CYCLE CONNECTION/24 HR CYCLE CONNECTION

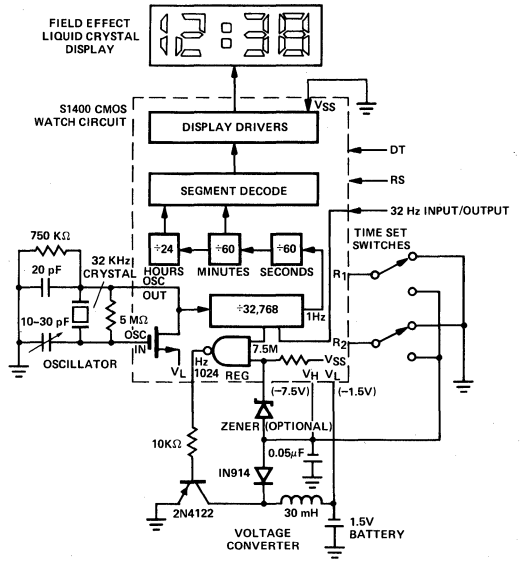
STATIC CHARACTERISTICS

$T_A = 25°C$, $V_L = -1.5V \pm 5\%$, $V_H = -7.5V \pm 10\%$, V_{SS} = Ground, 32768 Hz crystal

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_S	Minimum starting voltage	−1.4	−1.1		Volts	
V_{HIGH}	High logic level, all inputs		V_{SS}		Volts	
V_{LOW}	Low logic level:					
	RS, 1024 Hz, 32 Hz, 12/24		V_L		Volts	
	HR, DT, R1, R2		V_H		Volts	
	All display outputs		V_H		Volts	
V_{TH} (REG)	Regulator switching threshold	−0.5	−.75	−1.0	Volts	
R_O (SEG)	Segment output resistance, both states		20		Kohm	$I_O = 10\mu A$
R_O (BP)	Back plate output resistance, both states		6		Kohm	$I_O = 10\mu A$
R_O (1024)	1024 Hz pulse output resistance, both states		2	4	Kohm	$I_O = 10\mu A$
I_L	V_L supply current:					
	SXXXX		2.5	5.0	μA	Freq = 32768 Hz. Includes OSC bias current.
	SXXXXA			20.0		
	SXXXXB	20	50			
I_H	V_H supply current:					
	SXXXX		0.3	1.0	μA	Outputs open circuit.
	SXXXXA			2.5		
	SXXXXB	2.5	25			
I_{IN} (REG)	Voltage regulator input bias current		0.1		μA	$V_{IN} = -0.75V$
I_{OSC}	Oscillator transistor bias current		1.0		μA	
g_m OSC	Oscillator transistor transconductance		18		μmho	$I_{OSC} = 1\mu A$

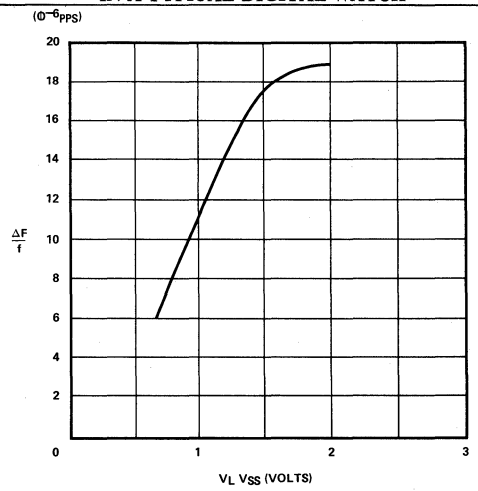
DYNAMIC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$F_{DISPLAY}$	Display switching frequency		32		Hz	
$F_{32\ Hz\ INPUT}$	Test Frequency			10.0	kHz	
PW (1024)	1024 Hz output pulse width	12	15	18	μs	

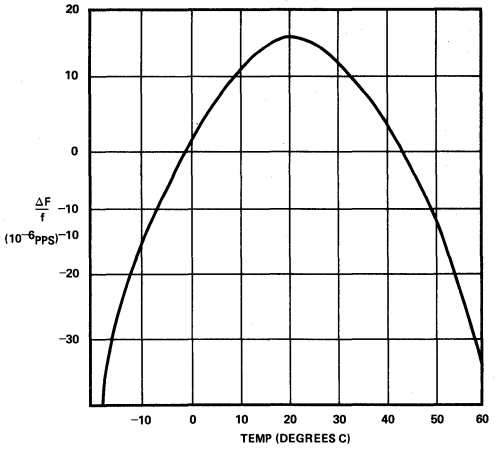


ELECTRICAL CONNECTIONS IN A TYPICAL DIGITAL WATCH

PARTS LIST	P/N	VENDOR
32 kHz Crystal	TPEY 014-5013-0	CTS Knights Reeves Hoffman
Display	S23560 6220 107	AMI ILIXCO Beckman
Display Connector		AMP Chromerics
Battery (Silver Oxide)	Eveready #301	ESB
Coil Pot Core	B65501 Y026	Siemens
Zener Diode	LVA Series	TRW CODI



TYPICAL OSCILLATOR CIRCUIT FREQUENCY VS V_L

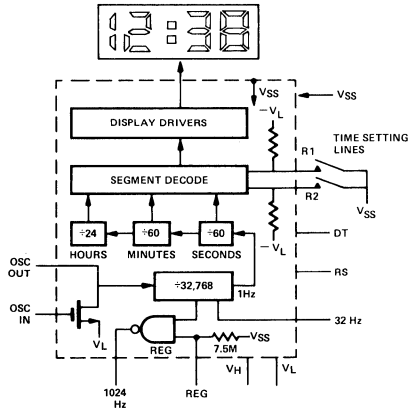


TYPICAL OSCILLATOR CIRCUIT FREQUENCY VS TEMPERATURE

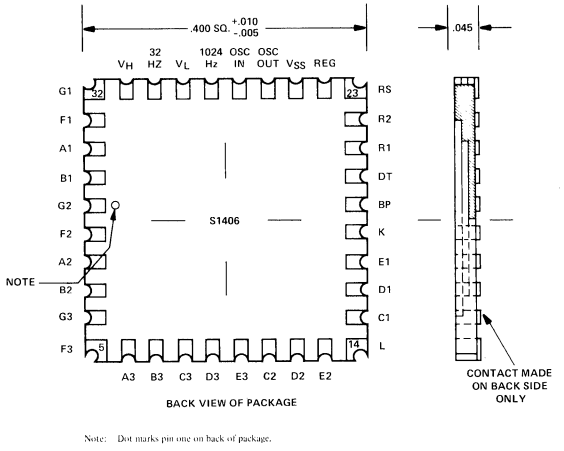
AMERICAN MICROSYSTEMS, INC.

S1406

LCD DIVIDER/DRIVER



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- Pinouts are a Mirror Image of S1404
- Single Chip CMOS Construction
- 1024 Hz Upconverter Output
- Internal Voltage Regulator
- Up to 12 Volt Output
- Uses Single-throw Setting Switches
- Internal Resistors on Inputs
- 12 or 24 Hour Cycle
- Hours and Minutes Display
- Colon flashes at 1 Hz rate
- 32 Khz Oscillator

(All other Features same as S1404)

FUNCTIONAL DESCRIPTION

The S1406 is a single CMOS circuit that directly replaces currently available two chip systems. The S1406 generates drive signals to a 3½ digit liquid crystal display from a 1.5 volt battery. The circuit provides a 1024 Hz up-converter output and a 32 Hz display output. A flashing colon output is also provided with either a 24 hour[1] or 12 hour display mode.

The S1406 is identical to the S1404, except its pinouts are a mirror image of those of the S1404, and internal resistors are used on the time setting lines. These resistors allow setting operations to be performed with single-throw push-button switches.

R1*	R2*	OPERATION
V_L	V_L	Normal Mode.
V_L	V_{SS}	Advance Hours only at 1 hour/second.
V_{SS}	V_L	Hold – Hrs. and Minutes. Also resets seconds to zero.
V_{SS}	V_{SS}	Advance Minutes/Hrs. at 1 min/second.

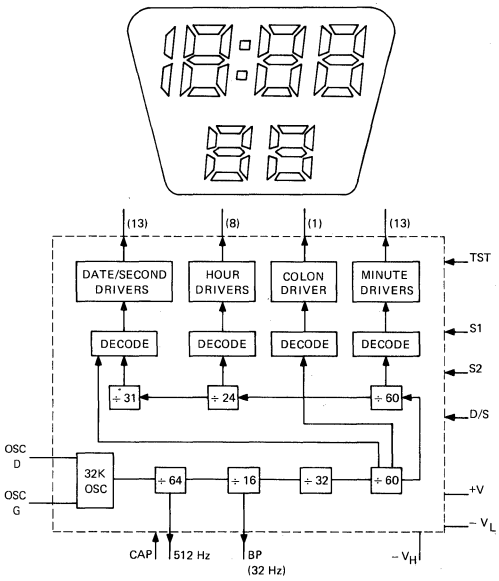
*R1, R2 normally held to V_L by internal resistor.

[1]Not available in S1406 package.

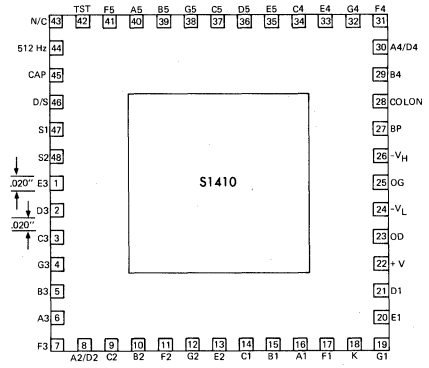
S1410
S1411

LCD TIME DATE SECOND
WATCH CIRCUIT

AMERICAN MICROSYSTEMS, INC.



TDS BLOCK DIAGRAM



S1410 PIN/PACKAGE CONFIGURATION
(S1411 – UNPACKAGED CHIP)

FEATURES

- Single Chip Construction
- Switch Inputs Filtered
- Internal Voltage Doubler
- Drives 5 - 1/2 Digit Display
- Utilizes a 1.5V Cell
- Date Sec Display
- Hours and Minutes Display
- 32 KHz Oscillator

FUNCTIONAL DESCRIPTION:

The AMI LCD TDS circuit is a single chip, silicon gate CMOS, watch circuit designed to drive a 5½ digit, field effect, liquid crystal display. When connected in a watch module, 3½ digits of the display show hours and minutes continuously. The remaining two digits continuously display seconds or date as selected by the user. Power for the circuit is furnished by a single 1.5V battery. The circuit provides a 512 Hz signal convenient for use in timing the oscillator. An internal voltage doubler furnishes voltage to drive a low voltage liquid crystal display. Only two external capacitors are required to operate the doubler. A 32 Hz output drives the display backplane. Time setting logic is provided to advance either hours, minutes, or date at a one Hz rate. The time base is a 32.768 KHz oscillator controlled by a quartz crystal.

LCD TDS CIRCUIT ELECTRICAL TEST SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Storage chip temperature		- 55°C to + 150°C	Positive voltage on any pin	V_{SS} + 0.3V
Operating ambient temperature		- 10°C to 70°C	Negative voltage on (OSC D, 512 Hz, 32 Hz)	V_L - 0.3V
Maximum Supply voltages	V_L	- 3V	Negative voltage on all other pins	V_H -0.3V
	V_H	- 12V		

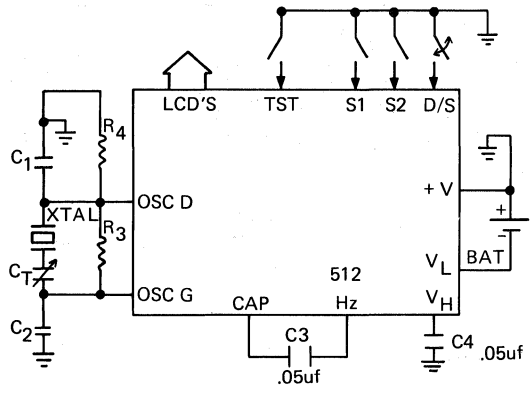
Note: Exceeding these voltages may forward bias some internal junctions. This is non-destructive if the current is limited to 0.1 mA.

SPECIFICATIONS

(T_A = 25°C, V_L = - 1.5V ± 5%, V_H =-3.2V ± 10%, V_{SS} = 0V, 32768 Hz Crystal)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_S	Starting voltage	– 1.4	– 1.1		Volts	
R_{OL} (SEG)	Segment low resistance		20		Kohm	I_0 = 10ua
R_{OH} (SEG)	Segment high resistance		20		Kohm	I_0 = 10ua
R_{OL} (BP)	Back plate low resistance		6		Kohm	I_0 = 10ua
R_{OH} (BP)	Back plate high resistance		6		Kohm	I_0 = 10ua
R_{OH} (512)	512 Hz HIGH resistance to V_{SS}		7		Kohm	I_0 = 1ua
R_{OL} (512)	512 Hz LOW resistance to V_L		7		Kohm	I_0 = 1ua
PW (512)	Pulse width		975		us	Freq = 32768 Hz
I_L	– V_L supply current		3.5	7.0	ua	includes OSC bias current
I_H	–V_H supply current		0.3	1.5	ua	Outputs open ckt
I_{OSC}	Oscillator transistor bias current		1.0		ua	
gm_{osc}	Oscillator transistor transconductance		18		umho	I = 1ua
V_H	Display Drive Voltage		2.8		Volts	I display = 1μA $C_3 = C_4$ = .05μf

ELECTRICAL CONNECTION



COMPONENT LIST

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
C_3	Doubler Capacitor		.05		uf
C_4	Doubler Capacitor		.05		uf
R_3	Oscillator bias resistor		5		Mohm
R_4	Oscillator load resistor		750		Kohm
C_1	Oscillator output capacitor		33		pf
C_2	Oscillator input capacitor		33		pf
C_T	Oscillator trimmer capacitor	5		50	pf
$-V_L$	Single cell battery		1.5		Volts
XTAL	32.768 KHz quartz crystal				

TST – Resets all counters when input level is held at V_{SS}

S1, S2 – Select function modes by Truth Table levels

D/S – Flips date or seconds mode by detecting positive (V_{SS}) input transition

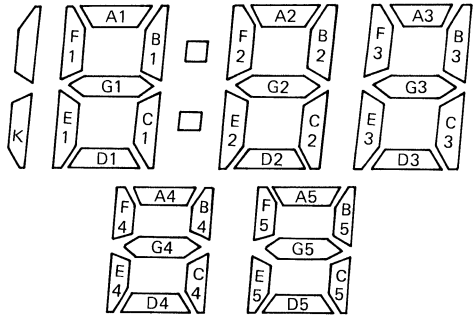
SETTING MODE TRUTH TABLE

S1	S2	FUNCTION*
		SEC DISPLAYED/DATE DISPLAYED
$-V_L$	$-V_L$	NORMAL / NORMAL
$-V_L$	$+V_{SS}$	ADV HRS / ADV DATE
$+V_{SS}$	$-V_L$	HOLD / NORMAL
$+V_{SS}$	$+V_{SS}$	ADV MIN / NORMAL

*S1, S2, D/S have internal resistors to $-V_L$

LCD DISPLAY ELECTRICAL CONNECTIONS

(Drawing not to scale nor representative of display font)



DISPLAY MODES:

HOURS SET While selected, Hours will advance at a 1 Hz rate from the digit indicated. Colon, Minutes and Seconds counters will continue normally. The Date counter is held at its current value. The Colon display will be "Flashing On" at a 1 Hz rate for "AM" indication and be held off for "PM" indication.

MINUTES SET – While selected, Minutes will advance at a 1 Hz rate from the digit indicated. Date, and Hours counters are held at their current value, the Seconds counter is reset to zero, and the Colon is held On.

DATE SET – While selected, Date will advance at a 1 Hz rate from the digit indicated. All other counters continue normally. No time setting is possible during this mode.

HOLD – While selected, the Seconds counter is reset to zero seconds, and the D/S digits are set to display zero seconds. Date, Colon, Hours and Minutes counters are automatically held at their current values. The Colon display will be held "On" independently of "AM" or "PM" conditions.

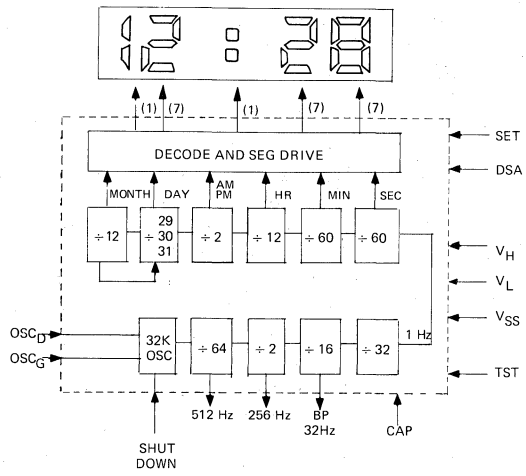
NORMAL – While selected, all counters will function normally. Date or Seconds will be displayed continuously as selected by the user.

S1420
S1421

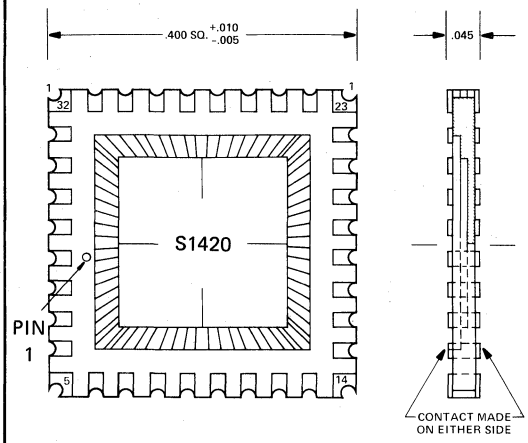
LCD CMOS WATCH CIRCUIT

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION



BLOCK DIAGRAM



S1420 PIN/PACKAGE CONFIGURATION
(S1421 – UNPACKAGED CHIP)

FEATURES

- 12 Month Calendar
- 512 Hz Oscillator Frequency Setting Output
- Voltage Doubler or Up Converter Options
- Drives Standard 3½ Digit Display
- Display and Setting with Two Push Buttons
- Uses Single 1.5V Battery
- Hours and Minutes Display
- Month and Date Display
- Seconds Display
- 32 kHz Oscillator
- Oscillator Shut Down Control

FUNCTIONAL DESCRIPTION

The AMI S1420 is a single chip, silicon gate CMOS watch circuit designed to drive a 3½ digit, field effect, liquid crystal display. Hour and minutes or seconds can be displayed continuously. Month and date are displayed on interrogation. Only two single pole single throw switches are required to accomplish all display and setting functions. The circuit provides a full calendar function which needs to be reset only once every four years.

FUNCTIONAL DESCRIPTION (Continued)

Power for the circuit is furnished by a single 1.5 volt battery. A 512 Hz output is provided for setting the oscillator frequency. An internal voltage doubler furnishes voltage to drive a low voltage liquid crystal display. Only two external capacitors are required to operate the doubler. Additionally, a 256 Hz, 15.6 μsec negative going pulse is available to drive an up-converter for high voltage liquid crystal display applications. a 32 Hz output drives the display backplane. The time base is a 32.768 kHz oscillator controlled by a quartz crystal.

The S1421 is a unpackaged version of the S1420.

OPERATION

The circuit may display hours and minutes continuously (S1A), month and date when interrogated (S1B) or seconds continuously (S1C) as shown in the table below:

STATE	NAME	DURATION	DISPLAY	COLON
S1A	HR MIN Display	Continuous	HH:MM	Flashing
S1B	MO DATE Display	Momentary	MO DD	Off
S1C	SEC Display	Continuous	SS	Off

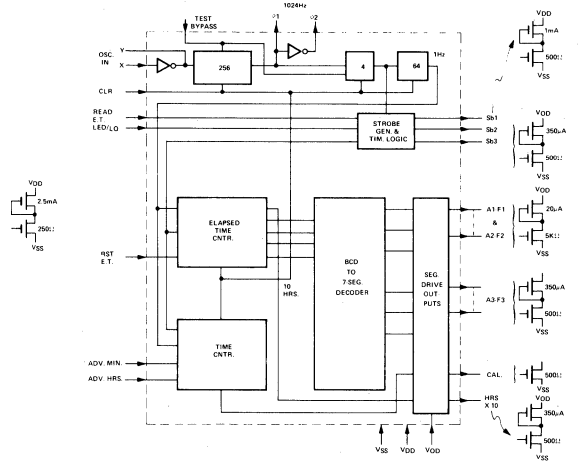
The absence of a colon distinguishes the month-date display from the hour-minute mode. The seconds mode is obvious as only the last two digits are used and the display is incrementing once per second.

All display and setting operations are controlled by two inputs, the DSA (Date, Second, Advance) input and the Set input. In Normal Operation only the DSA input is used. Both inputs have an internal pulldown to $-V_L$ so that a single pole, single throw contact may be used.

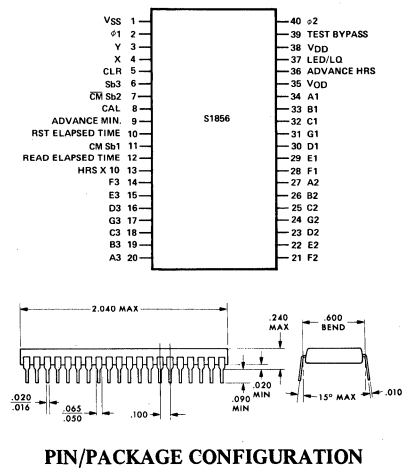
S1856

MOS DIGITAL CLOCK

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

(Available in Pkg. 1T - see Sec. 1)

FEATURES

- 262,144 External Quartz Crystal
- Has 20 Hr. Resettable Elapsed Time Counter
- Direct LCD Or Tung-sol DT1704 Tube Interface
- Electrically Selectable LED/MUX Output
- Minute and Hour SET Controls
- Separate Display Supply Allows Display Turn Off For Reduced Battery Current Drain
- 1024 Hz Outputs For Voltage Doubler
- Calendar Advancing or AM/PM Output

TYPICAL APPLICATIONS

- Automotive Clock
- Household Clock With Auxiliary Battery for Accurate Time Keeping During Power Interruptions
- Appliance Timers
- Industrial Timers
- Photographic Timers
- Avionics Timers
- Portable Clock

FUNCTIONAL DESCRIPTION

The S1856 Digital Clock provides the circuitry to implement a 4 digit time keeper with separate elapsed time counter. It is an MOS LSI circuit consisting of down counters, combinational logic, BCD to 7-segment decoder and output buffer transistors in a 40 pin DIP. The circuit has a separate output pin to drive each segment of a Liquid Crystal Display directly. However if the LED mode of operation is selected, only the HRS x 10 and F3 through A3 outputs are used to provide segment drive current. In this mode of operation segment drivers F3 through A3 are multiplexed at 25% duty cycle to provide MINUTES, 10's of MINUTES and HOURS information.

The ELAPSED TIME COUNTER can be reset and displayed separately without affecting the state of the time keeper. The ELAPSED TIME COUNTER has the added feature of displaying SECONDS, 10's of SECONDS and MINUTES automatically during the first 10 minutes after a reset has occurred. The counter will then display MINUTES, 10's of MINUTES, HOURS and 10's of HOURS for the remainder of its 20 hour capacity.

OPERATIONAL DESCRIPTION

The clock circuit block diagram is shown on the previous page. The input transistor of the circuit forms an oscillator circuit with an external quartz crystal and a few other components (see application drawings). The resultant 262.144 kHz signal is amplified and clipped in the input stage. A chain of binary down counters divides the square wave frequency by 256 to supply two complementary outputs, $\emptyset 1$ and $\emptyset 2$ at 1024 Hz. These low impedance outputs can drive an external voltage doubler as well as allow an accurate frequency tuning on the oscillator.

Next a divide by four stage produces a 64 Hz signal from which the three strobes Sb1, Sb2, and Sb3 are generated. The strobe generator also contains logic to synchronize the display outputs with the external strobes as well as control the segments for Liquid Crystal Display operation. The 64 Hz signal also inputs to a divide by 64 stage to produce a 1 Hz signal which inputs to both the TIME COUNTER and the ELAPSED TIME COUNTER.

The TIME COUNTER contains the binary stages and the decoding logic to generate the BCD code for MINUTES, HOURS and HRS x 10. This data is strobed into the BCD to 7-segment DECODER and loaded into the output buffers in synchronization with the appropriate strobe, Sb1, Sb2 or Sb3.

The ELAPSED TIME COUNTER functions similarly to the TIME COUNTER with the additional decoding of SECONDS and 10's of SECONDS to the display instead of HRS and HRS x 10 during the first 10 minutes after reset.

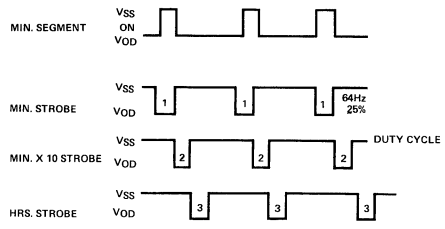
An internal connection to V_{DD} supply at pin 37 holds the clock in the liquid crystal mode and the outputs are interfaced directly with the LCD as shown in Figure 2 below.

To assure longevity of the LCD display, a 64 Hertz signal is applied to the individual segments. When the applied segment signal is in-phase with the 64 Hertz backplate (LCD common terminal) voltage, no visibility occurs. When the applied signal is 180° out of phase with the backplate voltage, visibility occurs. The waveforms shown in Figure 2 represent these conditions.

The backplate voltage is generated by buffering the signal which drives the timing counters. This assures that visibility of the display will not occur through synchronizing problems or rise and fall time differences.

The phase of the segment outputs is generated from the contents of data latches and buffer circuits. This provides an active pull-up or pull-down to both terminals of the segments at all times, thus eliminating the effect of capacitive coupling across the LCD segment. (See Figure 2)

When pin 37 is connected to V_{SS} the multiplexed mode of operation is selected. An ON segment in this mode is driven by a pull-down to V_{SS} which is true during its appropriate strobe time as shown in Figure 3 below.



A typical LED interface circuit is shown below in Figure 4. In this mode the HRS x 10 digit is a steady state DC output and can be used at any of the 3 strobe times.

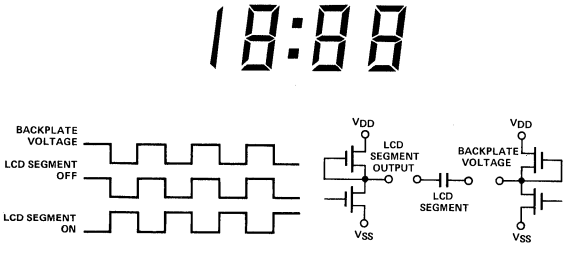


FIG. 2 LCD OUTPUT DRIVE

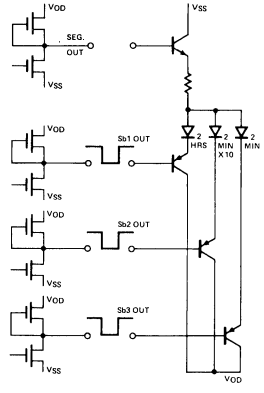


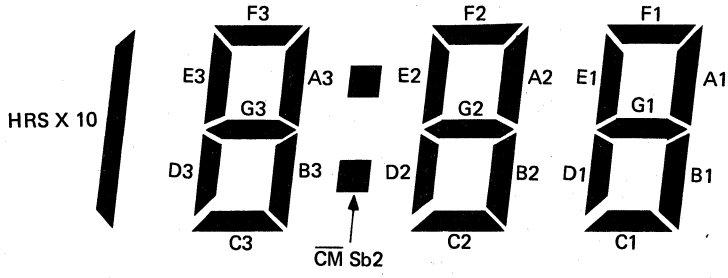
FIG. 4 MOS/LED INTERFACE

FUNCTIONAL DESCRIPTION OF INPUTS

V_{SS}	Positive voltage supply return line for circuit.
Y	Oscillator pull-up resistor connection. A 10K Ω resistor to V_{CC} from this pin serves as the 262.144 kHz oscillator load.
X	Oscillator input pin. Provides amplification at oscillation frequency of the output from the external crystal and RC network.
CLR	Master Clear. Resets all counters to zero when connected to V_{SS}.
ADV. MIN.	Sets MINUTES with carry to MINUTES x 10 at a one per second rate when connected to V_{SS}.
RST ET	Displays contents of ELAPSED TIME COUNTER when connected to V_{SS}, otherwise time of day is displayed.
V_{OD}	Negative power supply input for output buffers only. Allows display to be turned off while internal clock counters continue to operate.
ADV. HRS.	Sets HRS with carry to HRS x 10, at a one per second rate connected to V_{SS}.
LED/LQ	Mode select pin. When connected to V_{SS} the LED mode is selected. In this mode the three strobe outputs are used to multiplex outputs A3 through F3 to drive MINUTES, MINUTES x 10 and HRS x 10 digits. This occurs at 64 Hz 25% duty rate. In this mode outputs A1 through F1 and A2 through F2 remain off at negative supply level, V_{OD}.
V_{DD}	Negative power supply input for internal logic can be connected to V_{OD} for single supply operation.
TEST BYPASS	When connected to V_{SS} time counters advance at 1024 x normal rate. Used for automatic testing of the clock circuitry.

FUNCTIONAL DESCRIPTION OF OUTPUTS

$\phi 1$	Voltage doubler and frequency check output. This supplies a 1024 Hz square wave signal which swings between the V_{SS} and V_{DD} voltage levels.
$\phi 2$	Same as $\phi 1$ but 180° out of phase.
Sb3	Strobe signal for HRS digit. 64 Hz 25% duty cycle with voltage swing from V_{SS} to V_{OD}. Used only in LED mode.
$\overline{CM}$ Sb2	Drives colon in Liquid Crystal mode and serves as MIN x 10 digit strobe in LED mode. Voltage swing V_{SS} to V_{OD}.
CAL OUT	Calendar advance output. This pin has internal pulldown to V_{SS} only for stepping motor interface. An external 30 kΩ resistor may be connected to V_{OD} to drive an external latch for AM-PM display.
CM Sb1	Drives display back plan in LIQUID CRYSTAL mode and serves as MINUTES digit strobe in LED mode. Voltage swing V_{SS} to V_{OD}.



7 SEGMENT CALL OUT

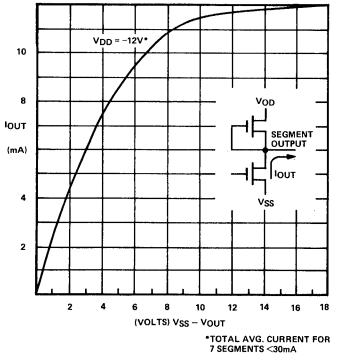
ABSOLUTE MAXIMUM RATINGS:

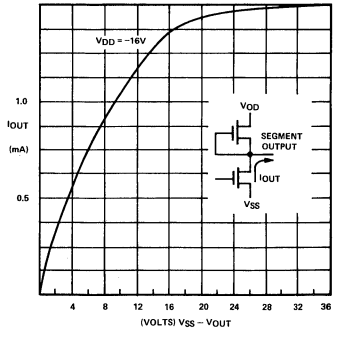
Positive Voltage on any Pin	V_{SS} +0.3V
Negative Voltage on any Pin	V_{SS} −28V
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +100°C

DYNAMIC CHARACTERISTICS
(T_A = −40°C to +70°C, V_{SS} = 0V, V_{DD} −6V to −16V, V_{OD} −5V to −28V)

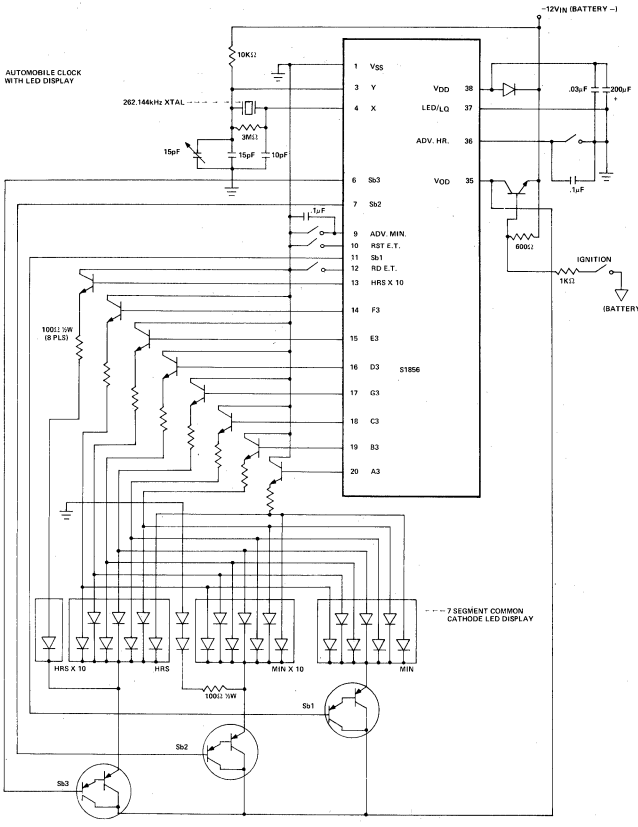
	Min.	Typ.	Max.	Units	Conditions
V_{IL} (OSC X)	V_{DD}		V_{SS} − 6	Volts	An internal
V_{IH}	V_{SS} − 1		V_{SS} + 0.3	Volts	resistor of
V_{IH} (Control)	V_{SS} − 0.5		V_{SS} + 0.3	Volts	700 KΩ (typical)
V_{IL}	V_{DD}		V_{SS} − 6	Volts	to V_{DD} is
					provided for all
					control inputs.
V_{OH} (Outputs)	V_{SS} − 1			Volts	Open circuit
V_{OL}			V_{DD}	Volts	Open circuit
I_{DD}		10	15	mA	V_{DD} − 14V
I_{DD}		10		mA	V_{DD} − 6V

TYPICAL PERFORMANCE CHARACTERISTICS

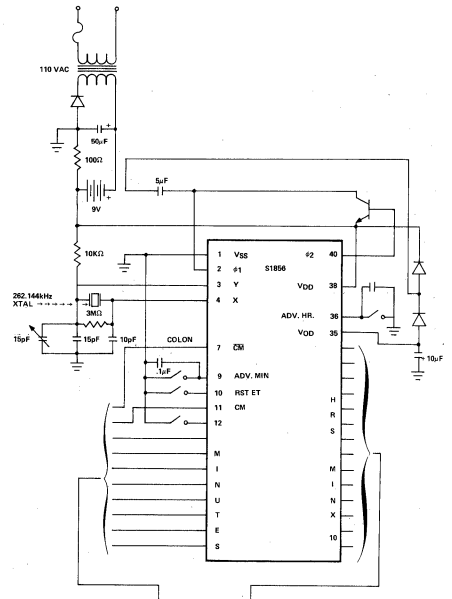


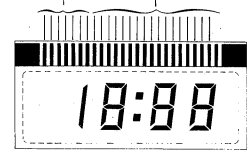


APPLICATION DATA



AUTOMOBILE CLOCK WITH LED DISPLAY



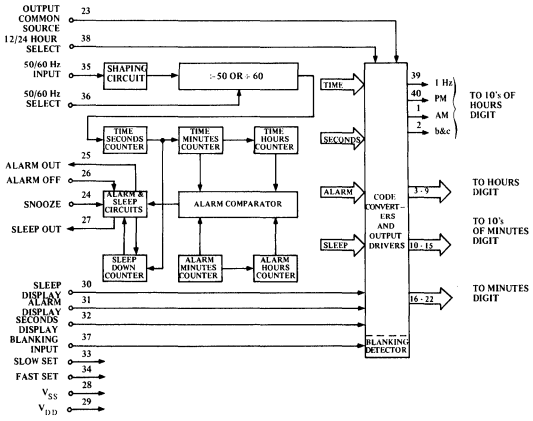


HOUSEHOLD CLOCK WITH AUXILLIARY BATTERY

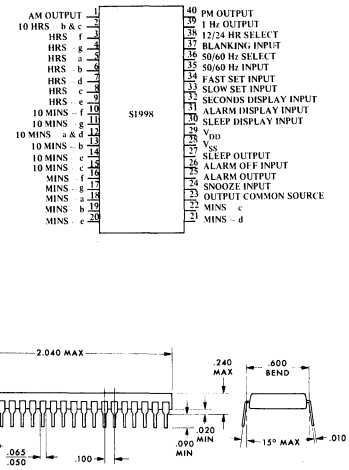
AMERICAN MICROSYSTEMS, INC.

S1998

DIGITAL ALARM CLOCK



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

(Available in Pkg. 1T - see Sec. 1)

FEATURES

- 50 or 60 Hz inputs
- Alarm with snooze
- Presettable 59 minute count-down timer
- Direct LCD/LED/Tube drive
- AM/PM or 24 hour outputs
- Power failure indicator
- Blanking/brightness control
- Alternate to MM 5316

FUNCTIONAL DESCRIPTION

The S1998 digital alarm clock is a monolithic MOS integrated circuit utilizing p-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. It provides all the logic required to build several types of clocks and timers. Four display modes (time, seconds, alarm and sleep) are provided to optimize circuit utility. The circuit interfaces directly with seven-segment fluorescent tubes or liquid crystal display, and requires only a single power supply. The time-keeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication or 24 hours.

Outputs consist of display drives, sleep (e. g., timed radio turn-off), and alarm enable. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The device operates over a power supply range of 8 to 29 volts and does not require a regulated supply. The S1998 is packaged in a 40-lead dual-in-line package.

TYPICAL APPLICATIONS

Alarm Clock, Clock Radio, Industrial Timer, Stop Watch, Photography Timers, Desk Clocks, Appliance Timers.

FUNCTIONAL DESCRIPTION

A block diagram of the S1998 digital alarm clock is shown on page 1. The various display modes provided by this clock are listed in Table 1. The functions of the setting controls are listed in Table 2. The following discussions are based on the Block Diagram.

50 or 60 Hz Input (pin 35): A shaping circuit is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 6V of hysteresis. A simple RC filter should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input (pin 38): A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1-pps time base. This counter is programmed to divide by 60 simply by leaving pin 38 unconnected; pull-down to V_{DD} is provided by an internal 2.5 MΩ resistor. Operation at 50 Hz is programmed by connecting pin 38 to V_{SS}.

Display Mode Select Inputs (pins 30 thru 32): In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal 2.5 MΩ pull-down resistors allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table 1. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in the Block Diagram the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs (pins 33 and 34): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table 2. Again, internal 2.5 MΩ pull-down resistors are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, in the 12-hour format (00:00:00 in the 24-hour format), by selecting seconds display and actuating both slow and fast set inputs.

Blanking Control Input (pin 37): Connecting this Schmitt trigger input to V_{DD} places all display drivers in a non-conducting, high-impedance state, thereby inhibiting the display. See Figure 4. Conversely, V_{SS} applied to this input enables the display.

Output Common Source Connection (pin 23): All display output drivers are open-drain devices with all sources common to pin 23 (Figure 4). When using fluorescent tube displays, V_{SS} or a display brightness control voltage is permanently connected to this pin. Since the brightness of a fluorescent tube display is dependent on the anode (segment) voltage, applying a variable voltage to pin 23 results in a display brightness control. This control is shown in Figure 7. However, when using liquid crystal displays, the lifetime of the display device is optimized when AC drive voltages are provided. The common source connection of the S1998 output drivers facilitates generating AC drive voltages. An interface circuit for driving liquid crystal display is shown in Figure 5.

When using low current LED displays the S1998 is connected as shown in Figure 3, to provide direct drive to the display. The 20V supply insures low output on resistance. The zener diode provides a 12V drop across output drivers which limits internal power dissipation to less than 60 MW per driver.

12 or 24 Hour Select Input (pin 36): By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal 2.5 MΩ pull-down resistor is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. Also, the output connections (pins 1, 2, 39 and 40) are different for each format. Figure 6 illustrates these differences. In addition to displaying 10's of hours, this digit provides an AM/PM indication.(12-hour format only) and the power failure indication. In the 12-hour format, AM indication is provided by segment "f"; PM indication by segment "e." The power failure indication consists of a flashing of the AM or PM indicator at a 1-Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal. In the 24-hour format, the power failure indication consists of flashing segments "c" and "f" for times less than 10 hours, and of a flashing segment "c" for times equal to or greater than 10 hours but less than 20 hours; and a flashing segment "g" for times equal to or greater than 20 hours.

FUNCTIONAL DESCRIPTION (Con't.)

Alarm Operation and Output (pin 25): The alarm comparator (Figure 1) senses coincidence between the alarm counter (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver (Figure 4), the S1998 output that is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input (pin 24) or reset by the alarm off input (pin 26).

Snooze Alarm Input (pin 24): Momentarily connecting pin 24 to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V_{DD} by an internal 2.5 MΩ resistor. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Alarm Off Input (pin 26): Momentarily connecting pin 26 to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal 2.5 MΩ resistor. The momentary alarm off input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm off input should remain at V_{SS}.

Sleep Timer and Output (pin 27): The sleep output at pin 27 can be used to turn off a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (Table 1) and setting the desired time interval (Table 2). This automatically results in a current-source output via pin 27, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. This turn-off may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the snooze input (pin 24). The output circuitry is the same as the other outputs (Figure 4).

TABLE 1. S1998 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE 2. S1998 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (12-hour format)
	Both	Time Resets to 00:00:00 (24-hour format)
Sleep	Slow	Subtracts Count at 2 Hz
	Fast	Subtracts Count at 60 Hz
	Both	Subtracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

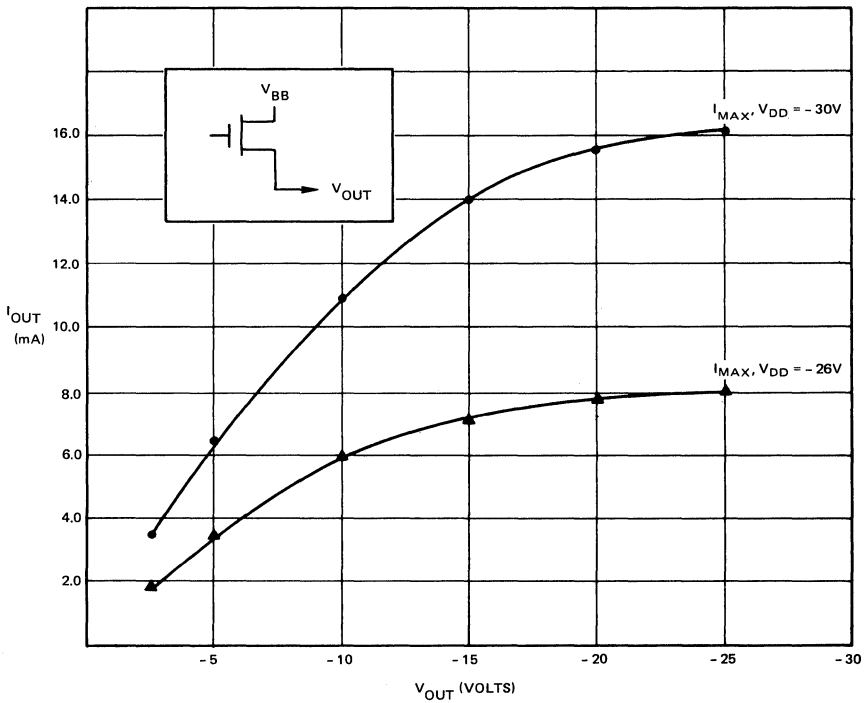
ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin	V_{SS} + 0.3V	Storage and Operating Chip Temperature	−55°C to + 150°C
Negative Voltage on any Pin	V_{SS} − 30V	Operating Ambient Temperature	0°C to + 70°C

STATIC CHARACTERISTICS

(T_A = 0° to + 70°C, V_{SS} = + 8V to + 29V, V_{DD} = GROUND

	Min.	Typ.	Max.	Units	Conditions
I_{SS} Power Supply Current:					no output loads
		2	5	mA	V_{SS} = + 8V
		3	15	mA	V_{SS} = + 29V
50/60 Hz Input:					
Frequency	DC	50 or 60	30k	Hz	
Voltage					
V_{IH} Logical High Level	V_{SS} −1		V_{SS}	V	Internal 2.5 MΩ on all inputs
V_{IL} Logical Low Level	V_{DD}		V_{DD} + 1	V	except CLOCK
Power Failure Detect Voltage:	+ 8.5		+ 13.5	V	(V_{SS} Voltage)
Output Currents:					V_{SS} = +21 to +29V, V_{DD}=0V
1 Hz Display					
I_{OH} Logical High Level	1500			μA	$V_{OH} = V_{SS} - 2V$
I_{OL} Logical Low Level			1	μA	$V_{OL} = V_{DD}$
10's of Hours (b &c), 10's of Minutes (a & d)					
I_{OH} Logical High Level	1000			μA	$V_{OH} = V_{SS} - 2V$
I_{OL} Logical Low Level			1	μA	$V_{OL} = V_{DD}$
All Other Display, Alarm and Sleep Outputs					
I_{OH} Logical High Level	500			μA	$V_{OH} = V_{SS} - 2V$
I_{OL} Logical Low Level			1	μA	$V_{OL} = V_{DD}$



S1998 DISPLAY DRIVER
OUTPUT VOLTAGE VS OUTPUT CURRENT
V_{BB} = V_{SS} = GROUND
(Pins 2, 40, 12 CURRENT = 2X I_{OUT})

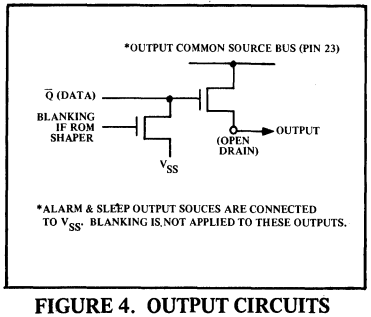
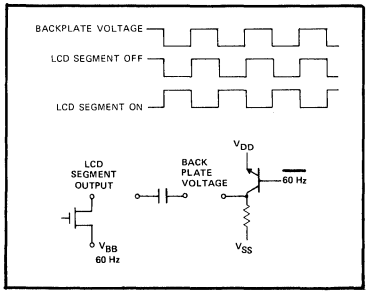


FIGURE 4. OUTPUT CIRCUITS



DISPLAY INTERFACE

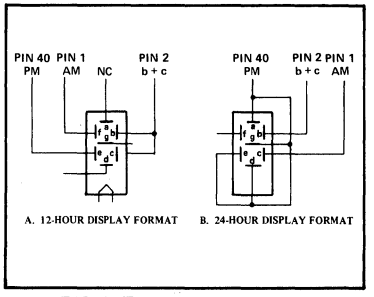


FIGURE 6. WIRING TEN'S-OF-HOURS DIGIT

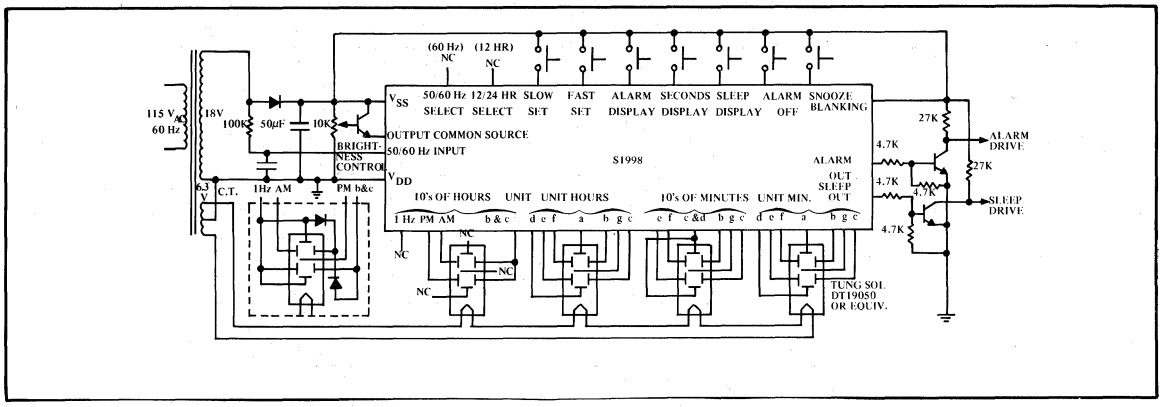


FIGURE 7. TUBE DISPLAY CLOCK

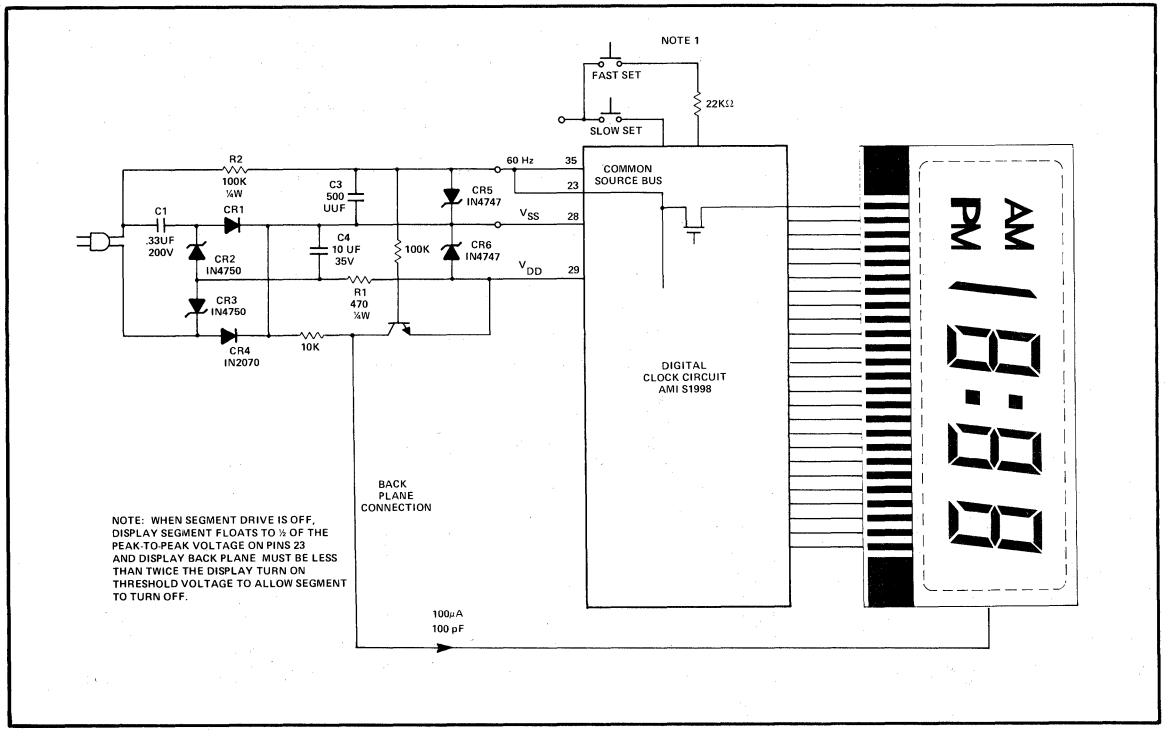


FIGURE 8 LCD DISPLAY CLOCK

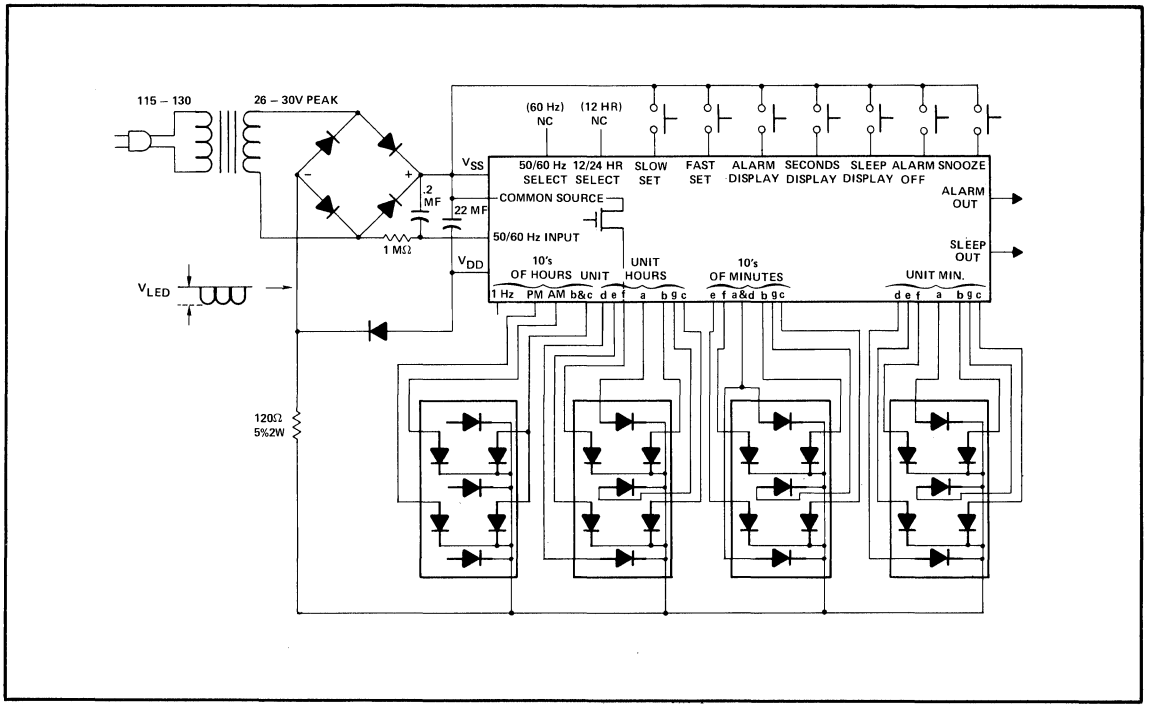


FIGURE 9 LED CLOCK

OPERATING CONDITIONS

Common Source (Pin 23) :	Connect to V_{SS} (Pin 28)
LED Voltage Supply:	Full Wave Rectified Sine Wave (Pulsating)
(V_{LED}) LED Power Supply Voltage Peak:	30 Volts Max.
LED Segment Voltage:	- 26 Volts DC Min. (2)
	- 30 Volts DC Max. (2)
Temperature:	40 Degrees C Max.
R LED: (1)	120 Ohms ± 5%, 2 Watt

DEVICE CHARACTERISTICS

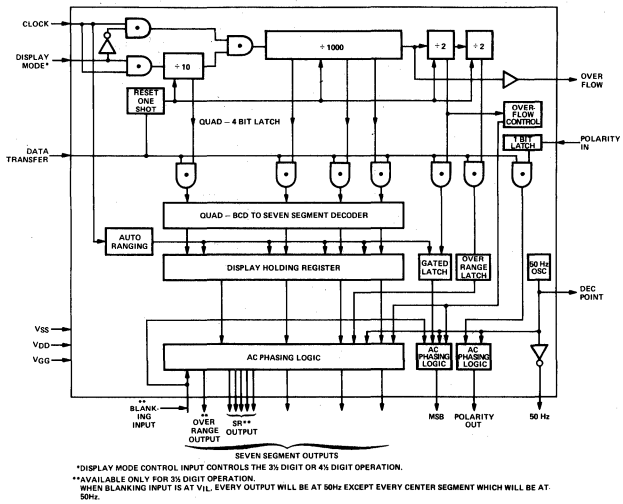
LED Segment Current:	(22 Segments on) 2.9 mA Min. at V_{LED} = 26 Volts
	(15 Segments on) 3.3 mA Min. at V_{LED} = 26 Volts(2)
	(15 Segments on) 4.5 mA Max. at V_{LED} = 30 Volts (2)
Power Dissipation:	700 Millivolts Max. @ 40°C and - 30V

NOTES:
1. (R_{LED}) resistor connected between LED cathodes and LED full wave rectified voltage supply. R_{LED} limits power on chip to 700 MW.
2. These peak voltages correspond to 115V to 130V RMS AC supply voltage.

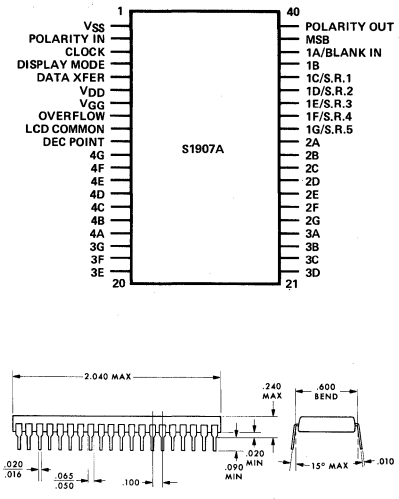
S1907A

DVM COUNTER/DISPLAY DRIVER

AMERICAN MICROSYSTEMS, INC.



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION
(Available in Pkg. 1T - see Sec. 1)

FEATURES

- Drives Liquid Crystal Display Directly
- Low Power Battery Operation
- Provides Autoranging Drive Capability
- Maximum Clock Frequency 500 kHz

TYPICAL APPLICATIONS

- Portable DMM
- Digital Voltmeter
- Event Counter
- Digital Panelmeter
- Digital Multimeter
- Power Supply Digital Readout
- Frequency Counter

FUNCTIONAL DESCRIPTION

The S1907 MOS Counter/Display provides the circuitry to implement a 4½ digit multimeter, an event counter, or a digital voltmeter. The S1907 can be used in any commercial or industrial application where event counting and display are required. The S1907 contains COUNTER – DECODER – DRIVER LOGIC and is driven by a burst of clock pulses from an external A/D converter circuit. The Counter/Display counts the incoming pulse train, decodes the count into a seven segment output and stores the output in a latch. Internal output buffers provide direct interfacing capability to a liquid crystal display.

A 3½ digit output option which includes an autorange function can be electrically selected.

Two or more S1907's can be cascaded to obtain display capability greater than 4½ digits. AMI's ion implanted low V_T process is used to achieve low power and high speed operation.

AUTO RANGING

This function is performed only in the 3½ digit mode. It is realized by shifting a one to the right, left, or by "store" in a five bit shift register. One of the above conditions is selected by underflow, overflow or neither. Underflow occurs when there are no ones in the last decade, MSB or overrange register. Overflow occurs when the overflow bit is a one. When the power supply approaches the operating level, the auto range shift register is initialized 1 0 0 0 0. In this condition, only a right shift, corresponding to underflow, may occur. When the register reaches the 0 0 0 0 1 state, only left shift may occur. Auto range may occur only once per transition from "0" to "1" of the data transfer line.
Each shift register output is brought out to a pin as described in the attached pin list. Each shift register output is capable of sinking 1.0 ma with the output at V_{SS} −1.0 volts (See Figure 6).

CLOCK INPUT

Clock input is used by the internal counter to count up to the number to be displayed. Counting occurs on the negative transition of the input clock signal.

DISPLAY MODE CONTROL INPUT

When the display mode control input is at V_{IL}, the chip functions in the 4½ digit mode and when the display mode control is at V_{IH}, the chip functions in 3½ digit mode.

DATA TRANSFER INPUT

This signal performs two control functions; transfer of data from the counters to the display holding registers and reset of the counters. The chip can be operated as an event timer or counter with the data transfer Input at V_{IL}. In this mode, the output buffers will be continuously updated as the counters are operating. Counting will occur with data transfer high or low. A V_{IL} to V_{IH} transition triggers a one shot with pulse width t_{cr} which resets the counter.

*A revision denotes change in connection of output buffers from V_{GG} to V_{DD} to eliminate DC component of output signal.

DIGIT SEGMENT OUTPUTS

This output signal can drive AMI's Liquid Crystal Display or TUNG-SOL DT-1704 display tubes (typical values only). Each segment is driven at approximately 50 Hz which is generated by an on-chip oscillator.

$\overline{50\ HZ}$ output

This is the common line to the Liquid Crystal Display input (GE Y1938).

OVERFLOW OUTPUT

This signal is not used to indicate an internal overflow condition, but is used to drive another DVM chip. When more than one DVM chip is used in a system, the overflow output of the first chip should be tied to the clock input of the second chip, and the data transfer signal should be tied to both chips.

BLANKING INPUT (3½ Digits Only)

When the blanking input signal is at V_{IL}, all LCD segment outputs except a center bar on digits are extinguished. The blanking input signal should be compatible with an over-range output signal.

OVERRANGE OUTPUT (3½ Digits Only)

The logic state of an overrange signal at V_{IL} indicates an overrange condition, and normally in a 3½ digit system, this output should be directly tied to the blanking input to indicate an overrange condition.

SR OUTPUTS 1 TO 5 (3½ Digits Only)

These outputs are used in conjunction with the autorange function. They can be used to drive external circuitry to provide control for the autorange function.

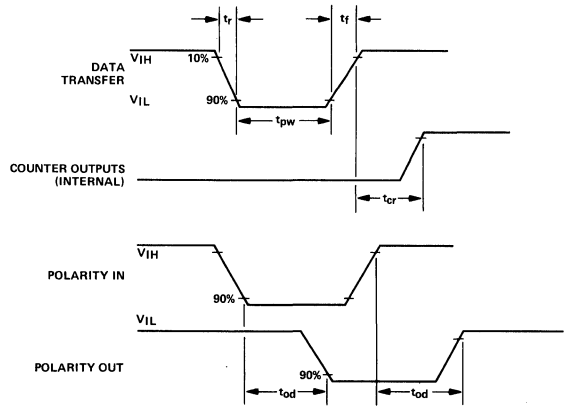
ABSOLUTE MAXIMUM RATINGS

Positive voltage on any pin	V_{SS} + 0.3V
Negative voltage on any pin	V_{SS} −30.0V
Storage and operating chip temperature	−25°C to +150°C
Operating ambient temperature	+0° to +70°C

SPECIFICATIONS
(T_A = 0° to +70°C, V_{DD} = −11 to −17V, V_{SS} = GRD, V_{GG} = −24 ± 1V)

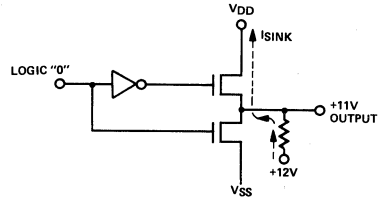
	Min.	Typ.	Max.	Units	Conditions
V_{IL} (Clock, logic)	V_{GG}		V_{SS} − 6.0	Volts	
V_{IH}	V_{SS} − 1.0		V_{SS}	Volts	
Clock Frequency	DC		500	KHz	
t_{pw} (Data transfer)	400			μs	
t_r, t_f (Data transfer)			500	nS	
t_{OD} (Output Delay)			5	μs	
t_{CR} (Counter Delay)			10	μs	
Input pull-up resistor to V_{SS} (all inputs)		100		kΩ	V_{IN} = V_{GG}
I_{OSD} (Segment Output Current)		2.0		mA	See Fig. 6
	10			μs	See Fig. 7
I_{OS} (50Hz Output Current)		3		mA	LOAD A
	50			μA	LOAD B
I_{OSOR} (Overrange Current)	1.0			mA	LOAD A
I_{OSAR} (Autorange Current)	1.0			mA	LOAD A
$I_{O\ DEC}$ (Decimal Current		2.0		mA	LOAD A
	25			μA	LOAD B
$I_{O\ MSB}$ (MSB Current)		0.6		mA	LOAD A
	10			μA	LOAD B
I_{OP} (Polarity Current		0.6		mA	LOAD A
	10			μA	LOAD B

TIMING DIAGRAM

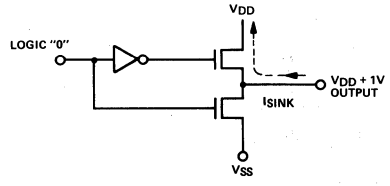


t_{pw} – Data Transfer Pulse Width
t_{cr} – Time to reset counters after data transfer makes a V_{IH} to V_{IL} transition.
t_{od} – Delay time from polarity input transition to polarity output transition.

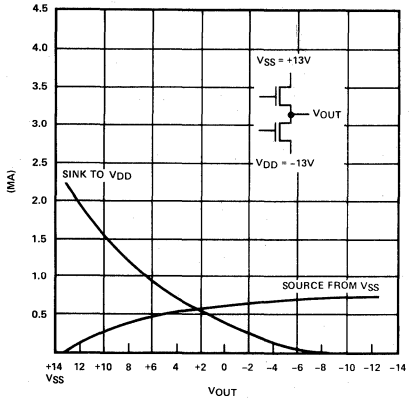
TEST INFORMATION



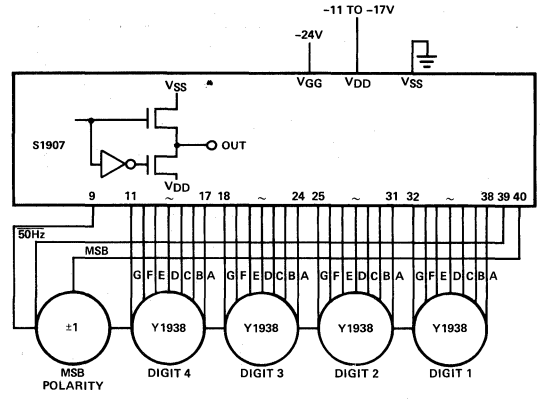
OUTPUT BUFFER LOADING CONDITION A



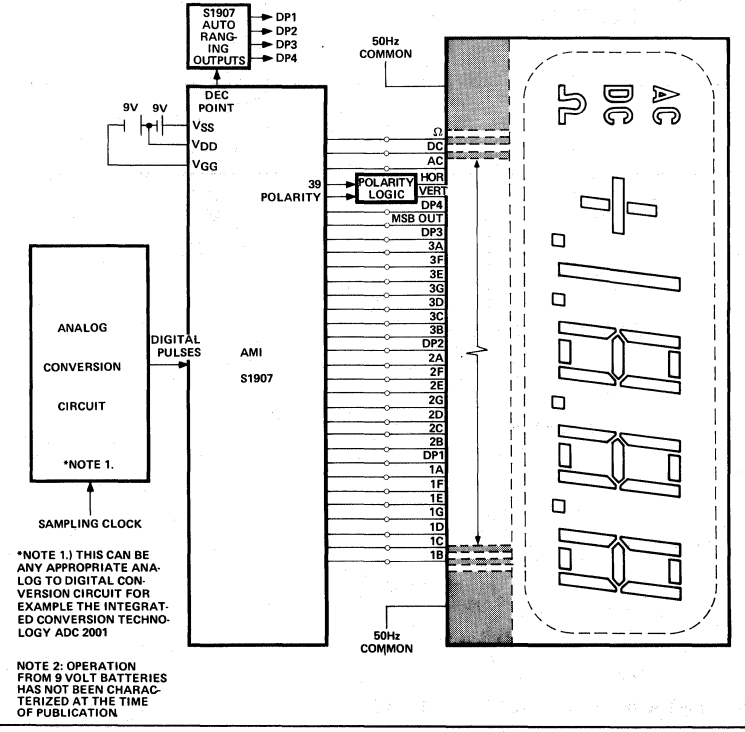
OUTPUT BUFFER LOADING CONDITION B



S1907 COUNTER/DISPLAY

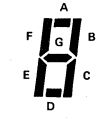


DISPLAY INTERFACE WITH TUBE DISPLAY



*NOTE 1.) THIS CAN BE ANY APPROPRIATE ANALOG TO DIGITAL CONVERSION CIRCUIT FOR EXAMPLE THE INTEGRATED CONVERSION TECHNOLOGY ADC 2001

NOTE 2: OPERATION FROM 9 VOLT BATTERIES HAS NOT BEEN CHARACTERIZED AT THE TIME OF PUBLICATION.



SEVEN SEGMENT OUTPUT DIAGRAM

10

Liquid Crystal Displays

Selection Guide–LCDs

Device No.	Description	Application	See Page
S23570	A 3½-digit, 3-volt display; most popular size and format for today's watches. Standard reflector is silver. Special-order options available: • Yellow/gold reflector • "Light-pack", for backlighting of display; allows clear viewing under all light conditions (with silver or yellow/gold reflector).	Men's Watch	10-7
S23590	Same as above except smaller in size.	Men's Watch	10-9
S23600	Microminiature 3-volt display with no compromise in readability. Single-ended connector configuration for flexibility in module design. Standard reflector is silver. Special-order option available: • Yellow/gold reflector	Ladies' Watch	10-11
S23610	A 6-digit, 3-volt display capable of presenting a continuous readout of either hours – minutes – seconds, or hours – minutes – date. Standard reflector is silver. Special-order options available: • Yellow/gold reflector • "Light-pack", for backlighting of display; allows clear viewing under all light conditions (with silver or yellow/gold reflector).	Time/Date/Second Watch	10-13
S23620	A 6-digit, 3-volt display capable of presenting a continuous readout of either hours – minutes – seconds (preceded by word "sec"), or hours – minutes – date (preceded by "date"). Standard reflector is silver. Special-order options available: • Yellow/gold reflector • "Light-pack", for backlighting of display; allows clear viewing under all light conditions (with silver or yellow/gold reflector).	Time/Date/Second Watch with Annunciators	10-15

Future Products

3½-digit Panel Meter Display Cell

12-hour Clock Display Cell

24-hour Clock Display Cell

AMI Liquid Crystal Displays

QUALITY BASED ON EXPERIENCE

Until a few years ago, liquid crystals were a laboratory curiosity with little commercial value. AMI was one of the first companies to work on a practical liquid crystal product, and in 1971 introduced LCD displays in their calculator product line. Today, the Company has grown to become one of the largest suppliers of field-effect type LCDs, manufacturing displays for a variety of OEM applications. AMI has full capability to design, produce original artwork, and manufacture field-effect liquid crystal displays of various configurations. This enables AMI to control each and every operation, thus reducing costs and establishing rigid quality assurance requirement standards, unsurpassed in the industry.

VARIETY OF PRODUCTS

Presently AMI delivers large numbers of LCDs to watch manufacturers throughout the world. These same displays are also being incorporated in complete watch modules assembled by the Company. In addition to watch products, further research and engineering is continuing in many process and product areas to meet ongoing commercial and industrial LCD needs for miniaturization, larger area displays, improved characteristics, extended life, and reduced operating voltages. Though AMI is production oriented, a major part of the Company's continuing success is its commitment to custom products.

AMI liquid crystal displays provide the high degree of readability needed in digital applications – and with only a fraction of the power required by other types of displays. Liquid crystals exhibit effective readability under almost all lighting conditions; diffused lighting does not adversely affect the display, thus no washing out occurs under direct sunlight.

BUILT-IN RELIABILITY

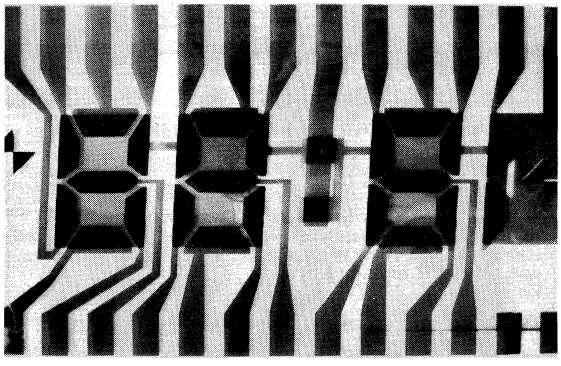
Each display is a plug-in type, able to interface directly with MOS watch circuits, including the AMI S1400 CMOS series.

AMI LCDs feature glass-to-glass construction, assuring mechanical durability and long life. In addition, the use of the twisted nematic field-effect technique for the LCDs (as opposed to dynamic scattering), allows compact designs and lowest operating voltages. All AMI watch displays are on at 3 volts and are completely turned off at 1 volt. During the off condition a display draws no power.

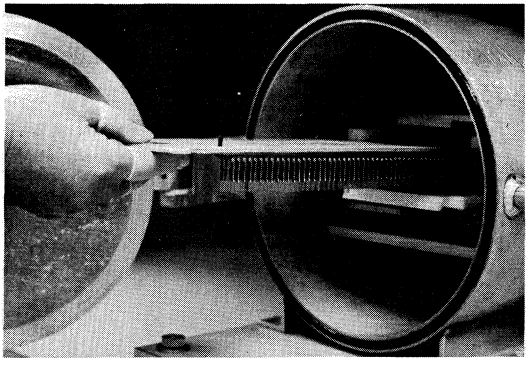
Other outstanding features of AMI liquid crystal displays include stable liquid crystal materials, excellent UV immunity, and extended life projections under recommended input signal conditions.

QUALITY CONTROL OF LCDs

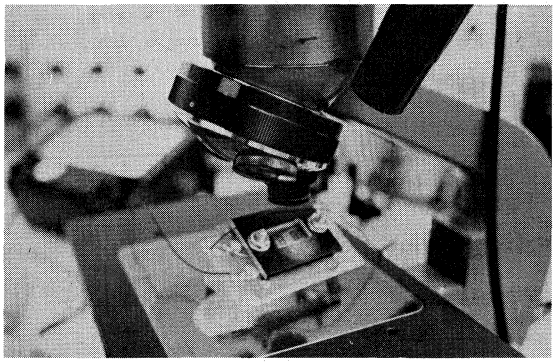
In order to ensure the highest degree of reliability of AMI liquid crystal displays, there are two significant test/failure programs conducted continuously in manufacturing: 1) Production Testing, and 2) Reliability Testing.



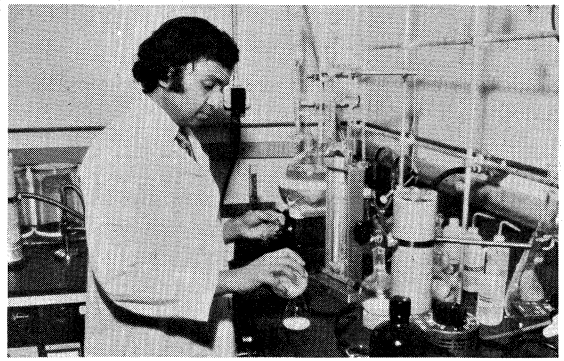
Artwork for a Typical Watch Display.



Display Cells Ready for Filling with Liquid Crystal Material.



The Viewing Angle is Checked on Display Cells with a Digital Photometer.



The Materials for AMI Displays are Made in Our Own Laboratories.

Production Testing

Every display at AMI is tested for speed, operating current, and given a thorough visual test for defects in the viewing surfaces and general readability of the display. Electromechanical tests consist of front-to-back shorts failure, open segment, and segment-to-segment shorts. Other tests include checking of each display for the integrity of the liquid crystal seal at the seal point, as well as the lifting or peeling of polarizer material in the viewing area. Contrast ratio, response time, and power consumption are also tested. In addition, each unit is inspected for seal contamination and liquid crystal molecular misalignment (haze or frost).

Reliability Testing

At AMI the manufacturing reliability programs for field-effect liquid crystal displays are continuous and are updated in ongoing weekly segments. All reliability tests are conducted in accordance with MIL-STD-883.

Note: A quarterly Liquid Crystal Reliability Brochure is available on request.

AMI RELIABILITY PROGRAM FOR LIQUID CRYSTALS

TEST	MIL-STD-883 METHOD	CONDITIONS
Accelerated Operating Life Test	1005	1000 hours. Every 4th lot 5000 hours; all displays are tested with 7 volts (rms) at 32 Hz, applied to all segments (TA = 50°C).
Temperature Cycle	1010	20 cycles between -20°C and 60°C. Dwell time 15 minutes at each extreme.
Humidity Cycling	1004	Initial conditioning not required. Two cycles, consisting of +50°C/90% RH to 25°C/90% RH for 15 hours, followed by 8 hours at +65°C.
Ultraviolet Test	Special	300 hours of UV exposure (Blak-Ray Lamp, 3660A) equivalent to normal sunlight.

LCDs Are Changing!

The rapidly increasing acceptance of Liquid Crystal Displays in watches and instruments, along with the emergence of a stable LCD industry, points to a promising future, both for the manufacturers who are able to deliver a quality product, and for the technology in general. However, to reach this favored status, the LCD industry has had to work for it.

When LCDs were first introduced in the early 1970s, they started out fast, but sometimes were backed up by very little technological knowhow. A large number of would-be manufacturers appeared on the scene and along with them came some inferior products – both in reliability and appearance. As a result, many large potential users pulled back and some misconceptions about LCDs arose. (For example, the old wives' tale that "LCDs dry out after a while" still can be heard from an occasional bystander.)

By now several years of experience have been accumulated and a few stable high quality LCD manufacturers have emerged as the industry leaders. Therefore, it is time to look at the technology and its products again. The development of LCDs is still advancing very rapidly, but trends in products and materials, as well as some user experience, are established. Now, a user needs to continuously update his information on specific characteristics of LCDs, follow new kinds of products, recognize the widening range of applications of LCDs, and be familiar with general trends in technology.

TYPES OF DISPLAYS

LCD operational modes are well known: excitation applied to the crystalline material inside the display changes its molecular orientation, thus modifying the light passing through. The more common twisted-nematic field-effect displays usually have a black or dark image on a clear or light colored background, however, the image may be reversed by rotating one of the two polarizers 90 degrees. The less common dynamic scattering displays have a white image on a clear or reflective mirrored background.

In field-effect displays, various color combinations of digits and backgrounds can be obtained by varying the tint or percent transmissiveness of the polarizers used. For example, a black image is usually obtained by using 42% transmissive polarizers. Changing to higher percentage transmissive polarizers (55%) gives blue digits. The 42% to 46% transmissive polarizers are most commonly used – mainly due to their wide availability, and because black digits are usually preferred (they yield a higher effective contrast ratio, when viewed on a light background). By changing the color of the rear reflector (reflective mode) some interesting color combinations are possible.

Both field-effect and dynamic-scattering displays can operate either in the reflective or transmissive mode. Since the LCDs emit no light of their own, a reflective mode LCD becomes less readable at very low light levels. Transmissive-mode displays, properly backlighted by an external source, can provide low-ambient performance equivalent to light-emitting displays, such as gas-discharge displays or LEDs. The trade-off is the increased power consumption of the light source, which partially negates the LCD low power advantage. The light source, of course, does not have to be operated continuously, and may be switched on only during low ambient conditions. It is important to note that an LCD is the *only* type of display available today that can have a provision for nighttime viewing and yet have increased readability in high ambient light.

Most liquid crystal displays are fabricated using screening or photo techniques, with Schiff Base, Esters, or Bi-phenyls as the liquid crystal material inside the cell. Field-effect LCDs have the liquid crystal material sandwiched between two glass sheets, separated by approximately one-half mil (12 microns), and sealed at the perimeters. As with semiconductors, yield is the most important factor in manufacturing. With small displays, the major constraint on yield is line resolution in the image displayed. Manufacturers using screening techniques have design rules which limit them to 5 - 7 mil lines and spaces, with reasonable yields, but photo techniques allow tighter tolerances, on the order of 2 to 4 mils.

OTHER ADVANTAGES

Liquid crystal displays have a number of distinct advantages that explain why a great deal of effort is going into the technology.

Low Power Consumption. The power requirements of LCDs are remarkably low. A twisted-nematic field-effect display, as used in a digital watch, typically requires less than one microwatt with all segments energized. In comparison, a four-digit LED watch display typically consumes 50 milliwatts, when operated at 3 to 4 volts! The low voltage, low current requirements of LCDs make them naturally compatible with CMOS circuits. (A dynamic-scattering type liquid crystal display, operating at 12 to 20 volt levels, dissipates approximately 40 to 50 microwatts.)

Alphanumerics/Pictures/Symbols. The ability to mix alphanumerics of any font, pictures, and symbols in a single envelope is another advantage of LCDs. In essence, any image that can be photographed can be presented as a liquid crystal display.

The advantages of LCDs are accompanied by some operational *trade-offs.* These trade-offs are relatively slow turn-on/turn-off times, and somewhat limited operational temperature ranges, as compared to other types of displays. However, advancements in materials, packaging, and the understanding of failure modes have resulted in continuous improvement of these parameters.

LCDs are noted for their faster response times above 25°C, while becoming slower as they approach 0°C. Response times (sometimes referred to as switching times) are dependent also on drive levels, the liquid crystal material, and the distance separating the front and back plates of the display cell. Tighter spacing of the plates results in faster switching times, but from a manufacturing yield standpoint, the tighter tolerances are more difficult to maintain, particularly in the larger instrumentation type displays.

It is important to understand the terms used to describe switching time. Some data sheets specify switching time excluding the trigger signal. This kind of specification "hides" the trigger transition, which can often involve an additional 50 - 100 ms! A realistic specification gives response times (200 ms turn-on, 350 ms turn-off are typical) from the trigger signal to within 10% of full change of image (or to 95% on).

A designer does have some opportunity to choose a trade-off for his particular application. For example, for a given display configuration tighter tolerances between the glass plates may be possible, a different mixture of LC material be used, or a higher drive voltage might be applied. The trade-off might involve some additional cost for the display, or display drive system. Here again, all manufacturers are gradually reducing the cost of LCDs, as better materials and methods develop.

Field-effect LCDs generally have an operating range of 0° to 50°C (32°F to 122°F), and a storage range of -40°C to 65°C (-40°F to 149°F). While other display technologies may have broader operating ranges, 0° to 50°C encompasses most of the range in which a device with a display might be viewed by an operator.

WHAT ABOUT LIFE PROJECTIONS?

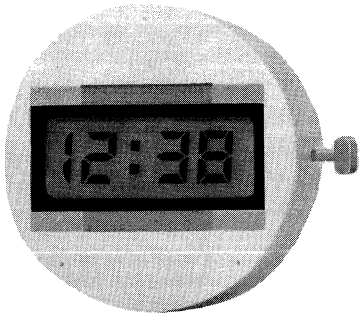
When choosing a supplier of LCDs, the buyer should not hesitate to request and review real-time life data. The buyer should be cautious, however, when claims for 20,000 or 30,000 plus hours of actual life are being presented. If an LCD manufacturer is keeping up with technology, he is continually implementing new or improved materials, life testing of these materials must be started over again, and consequently, it is impossible to have any large number of test hours accumulated. Instead, what is most important is to review the *trends* in life data – is the manufacturer improving?

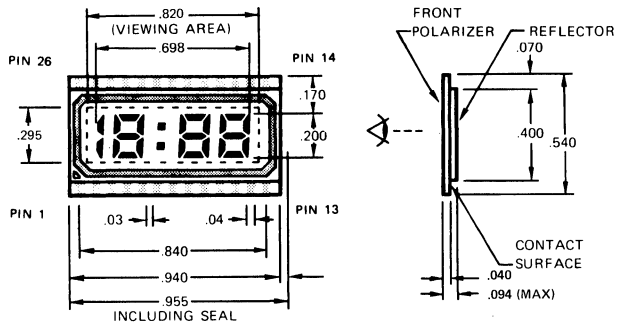
When dealing with a reputable manufacturer, you may find a standard "one year from date of shipment" warranty. *This is not unusual among component companies, and does not mean that the display is going to fail immediately after the one year.* Since valid life data takes time to accumulate, you should be more interested in the characteristics of the materials being used, and what trends, if any, are showing up in actual life testing. Also, you need to know *what the design goal is for projected life,* and *does the company have the data* to support advancements being made towards that design goal? AMI, for example, guarantees displays for one year from date of shipment, however, we have a 40,000 hour (5 years) design goal as a *minimum,* and data from real-life testing leads us to believe that projected life over 40,000 hours, when the display is properly driven, is certainly possible in the future.

AMERICAN MICROSYSTEMS, INC.

S23570

LOW VOLTAGE FIELD EFFECT
LIQUID CRYSTAL
DIGITAL WATCH DISPLAY





MINIMUM VIEWING AREA: .820" x .295"

FEATURES

- Low Voltage
- Field effect design
- Direct MOS compatibility
- Exceptionally low power
- Glass-to-glass seal
- High contrast ratio
- Wide viewing angle

FUNCTIONAL DESCRIPTION

The AMI S23570 Low Voltage Field Effect Liquid Crystal Digital Watch display is designed to interface directly with MOS watch circuits, including the AMI S-1400 CMOS series. It is a high contrast, very low power, three and a half digit display. The colon may be pulsed for seconds indication.

The display features glass-to-glass seal construction, assuring a high degree of mechanical durability and a long lifetime.

SPECIFICATIONS

Electrical @ 25°C, 3 VAC Sq. wave, 32 Hz unless otherwise specified.

Operating Voltage:	On 3 VAC Sq. Wave, 32 Hz Off 1 VAC Sq. Wave, 32 Hz
Current Drain:	≤150 nA @ 3 VAC Sq. Wave, 32 Hz
Capacitance:	≤400 pF @ 1 kHz, all segments operating
Frequency Range:	20 Hz to 1 kHz

Electro-Optical @ 25°C, 3 VAC Sq. Wave, 32 Hz unless otherwise specified.

Contrast Ratio:	The dark digit against a silver gray background presents a ratio of at least 10:1 in contrast when viewed at normal incidence. This represents visual saturation to the unaided eye.
Off Angle Viewing:	Contrast ratio is reduced less than 30% when viewed at 30° from the 6 o'clock position.
Response Time:	Room Temperature On Delay <300 ms to 90% on Off Delay <400 ms to 10% on The colon blink will be visible at 0°C when driven with a 32 Hz 0.5 sec on, 0.5 sec off signal.

Mechanical:

Dimensional:	See outline drawing. Character height: .200". Contact spacing: 26 equal contacts centered at .070, tolerances non-cumulative.

Environmental

Operating temperature:	0°C to 50°C
Storage temperature:	- 20°C to + 65°C
Humidity (including polarizer):	+ 50°C and 60% RH for moderate periods
(excluding polarizer):	+ 50°C and 90% RH for moderate periods

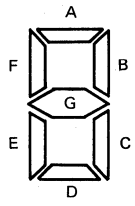
Lifetime

Continuous Operation: Minimum 10,000 hours under recommended CMOS signal conditions. Beyond the minimum lifetime it is expected that the devices will continue to operate indefinitely if not subjected to unusual mechanical, environmental or electrical stresses.

Workmanship

Quality:	The viewing area of the display will be free from inclusions, blemishes or non-uniformities in color visible to the unaided eye (<0.010"). The front polarized surface will have no scratches or blemishes that interfere with the legibility of the display when viewed at 10 inches under normal ambient light. The display will have no chips or scratches on the external contacts that interfere with the electrical operation.
Marking:	Marking will consist of the AMI logo, part number and manufacturing date code applied to the back surface. This mark will be sufficiently permanent to withstand normal handling.

CONTACT - SEGMENT IDENTIFICATION

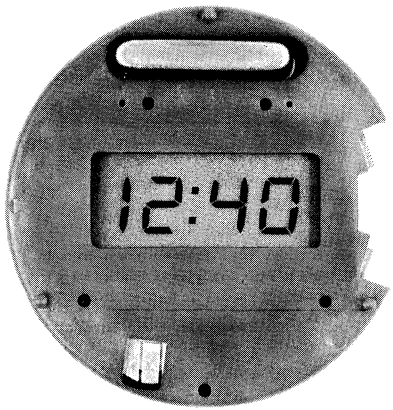


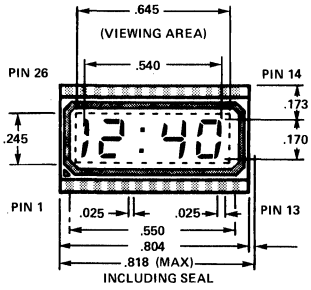
CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION
1	COMMON	10	MIN E	19	MIN x 10 F
2	HRS x 10	11	MIN D	20	MIN x 10 G
3	HRS E	12	MIN C	21	HRS B
4	HRS D	13	MIN B	22	HRS A
5	HRS C	14	MIN A	23	HRS F
6	COLON	15	MIN F	24	HRS G
7	MIN x 10 E	16	MIN G	25	SPARE
8	MIN x 10 D	17	MIN x 10 B	26	SPARE
9	MIN x 10 C	18	MIN x 10 A		

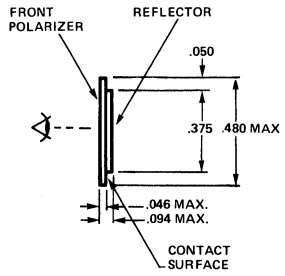
AMERICAN MICROSYSTEMS, INC.

S23590

LOW VOLTAGE FIELD EFFECT
LIQUID CRYSTAL
DIGITAL WATCH DISPLAY







MINIMUM VIEWING AREA: .645" x .245"

FEATURES

- Low Voltage
- Field Effect Design
- Direct MOS compatibility
- Exceptionally low power
- Glass-to-Glass Seal
- High Contrast Ratio
- Wide Viewing Angle

FUNCTIONAL DESCRIPTION

The AMI S23590 Low Voltage Field Effect Liquid Crystal Digital Watch display is designed to interface directly with MOS watch circuits, including the AMI S-1400 CMOS series. It is a high contrast, very low power, three and a half digit display. The colon may be pulsed for seconds indication.

The display features glass-to-glass seal construction, assuring a high degree of mechanical durability and a long lifetime.

SPECIFICATIONS

Electrical @ 25°C, 3 VAC sq. wave, 32 Hz unless otherwise specified.

Operating Voltage:	On 3 VAC Sq. Wave, 32 Hz Off 1 VAC Sq. Wave, 32 Hz
Current Drain:	⩽ 100 nA @ 3 VAC sq. Wave, 32 Hz
Capacitance:	⩽ 400 pF @ 1 kHz, all segments operating
Frequency Range:	20 Hz to 1 kHz

Electro-Optical @ 25°C, 3 VAC sq. Wave, 32 Hz – unless other wise specified.

Contrast Ratio:	The dark digit against a silver gray background presents a ratio of at least 10:1 in contrast when viewed at normal incidence. This represents visual saturation to the unaided eye.
Off Angle Viewing:	Contrast ratio is reduced less than 30% when viewed at 30° from the 6 o'clock position.
Response Time:	Room Temperature On Delay < 300 ms to 90% on Off Delay < 400 ms to 10% on The colon blink will be visible at 0°C when driven with a 32 Hz 0.5 sec on, 0.5 sec off signal.

Mechanical:

Dimensional:	See outline drawing. Character height: .170". Contact spacing: 26 equal contacts centered at .050 tolerances non-cumulative.

Environmental

Operating temperature:	0° to 50°C
Storage temperature:	- 20°C to 65°C
Humidity (including polarizer):	+50°C and 60% RH for moderate periods.
(excluding polarizer):	+ 50°C and 90% RH for moderate periods.

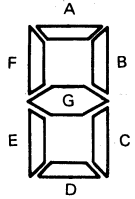
Lifetime

Continuous Operation: Minimum 10,000 hours under recommended CMOS signal conditions. Beyond the minimum lifetime it is expected that the devices will continue to operate indefinitely if not subjected to unusual mechanical, environmental or electrical stresses.

Workmanship

Quality: The viewing area of the display will be free from inclusions, blemishes or non-uniformities in color visible to the unaided eye (<0.010"). The front polarized surface will have no scratches or blemishes that interfere with the legibility of the display when viewed at 10 inches under normal ambient light. The display will have no chips or scratches on the external contacts that interfere with the electrical operation. Marking will consist of the AMI logo, part number and manufacturing date code applied to the back surface. This mark will be sufficiently permanent to withstand normal handling.

CONTACT - SEGMENT IDENTIFICATION

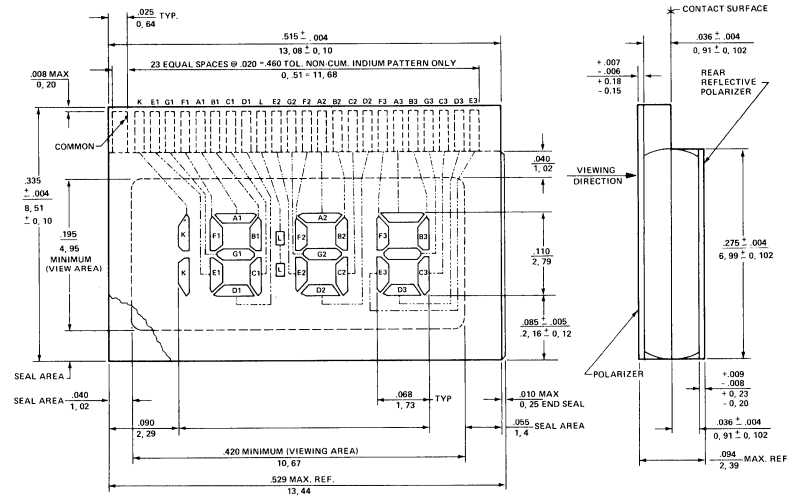


CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION
1	COMMON	10	MIN E	19	MIN x 10 F
2	HRS x 10	11	MIN D	20	MIN x 10 G
3	HRS E	12	MIN C	21	HRS B
4	HRS D	13	MIN B	22	HRS A
5	HRS C	14	MIN A	23	HRS F
6	COLON	15	MIN F	24	HRS G
7	MIN x 10 E	16	MIN G	25	SPARE
8	MIN x 10 D	17	MIN x 10 B	26	SPARE
9	MIN x 10 C	18	MIN x 10 A		

AMERICAN MICROSYSTEMS, INC.

S23600

LOW VOLTAGE FIELD EFFECT
LIQUID CRYSTAL
LADIES DIGITAL WATCH DISPLAY



MINIMUM VIEWING AREA: .420" x .195"

STANDARD FEATURES

- Microminiature Size
- Single-ended Connector Interface
- Low Voltage Drive
- Field Effect Design
- Direct MOS Compatibility
- Glass-to-Glass Seal
- High Stability LC Materials
- 'Silvered' Reflector
- Wide Viewing Angle
- Exceptionally Low Power Consumption

OPTIONAL (SPECIAL-ORDER) FEATURE AVAILABLE

- Yellow/Gold Reflector

FUNCTIONAL DESCRIPTION

The AMI S23600 Ladies Low Voltage Field Effect Liquid Crystal Digital Watch Display is designed to interface directly with MOS watch circuits, including the AMI S1400 CMOS series. It is a high contrast, very low power, 3-1/2 digit display.

The display features glass-to-glass seal construction, coupled with highly stable liquid crystal materials, to assure a high degree of mechanical durability and long lifetime.

SPECIFICATIONS

Electrical: @ 25°C, 3 VAC Sq. Wave, 32 Hz unless otherwise specified

Operating Voltage:	> 90% 'on' @ 3 VAC < 10% 'on' @ 1 VAC
Current Drain:	200nA typical, 400nA maximum
Capacitance:	200 pF typical, 300 pF maximum (all segments on)
Frequency Range:	20 Hz to 1 kHz

Electro-Optical: @ 25°C, 3 VAC Sq. Wave, 32 Hz unless otherwise specified

Contrast Ratio:	20:1 Minimum
Off-Angle Viewing:	Contrast ratio is reduced less than 30% when viewed at 30° from six o'clock position
Response Time:	From trigger signal to within 10% of full change (25°C)

	TYPICAL	MAXIMUM
On Delay	150 msec	250 msec
Off Delay	300 msec	500 msec

The colon blink will be visible @ 10°C

Mechanical:

Dimensional:	See outline drawing
Character Height:	.110"
Contact Spacing:	24 contacts total. 23 contacts, .010" wide (typ), centered at .020", tolerances non-cumulative. 'Common contact' is .020" wide (typ.)

Environmental

Operating Temperature:	0° to 50°C
Storage Temperature:	- 20°C to 65°C
Humidity (including polarizer):	+ 50°C and 60% RH for moderate periods
(excluding polarizer):	+ 50°C and 90% RH for moderate periods

Lifetime

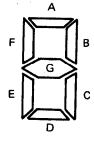
Continuous Operation: Minimum 10,000 hours under recommended CMOS signal conditions. Beyond the minimum lifetime it is expected that the devices will continue to operate indefinitely if not subjected to unusual mechanical, environmental or electrical stresses.

Workmanship

Quality: The viewing area of the display will be free from inclusions, blemishes or non-uniformities in color visible to the unaided eye (<0.010"). The front polarized surface will have no scratches or blemishes that interfere with the legibility of the display when viewed at 10 inches under normal ambient light. The display will have no chips or scratches on the external contacts that interfere with the electrical operation.

Marking: Marking will consist of the AMI logo, part number and manufacturing date code applied to the back surface. This mark will be sufficiently permanent to withstand normal handling.

CONTACT – SEGMENT IDENTIFICATION

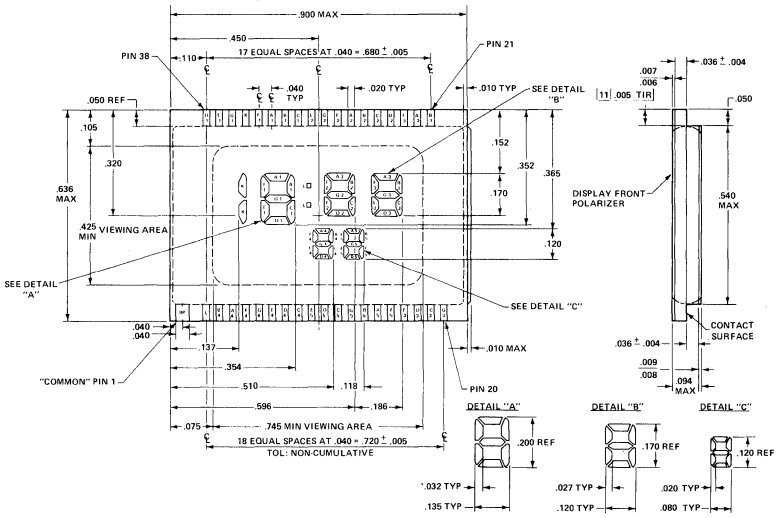


CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION
1	COMMON	13	MIN x 10 F
2	HRS x 10 K	14	MIN x 10 A
3	HRS x 1 UNIT E	15	MIN x 10 B
4	HRS x 1 UNIT G	16	MIN x 10 C
5	HRS x 1 UNIT F	17	MIN x 10 D
6	HRS x 1 UNIT A	18	MIN x 1 UNIT F
7	HRS x 1 UNIT B	19	MIN x 1 UNIT A
8	HRS x 1 UNIT C	20	MIN x 1 UNIT B
9	HRS x 1 UNIT D	21	MIN x 1 UNIT G
10	COLON L	22	MIN x 1 UNIT C
11	MIN x 10 E	23	MIN x 1 UNIT D
12	MIN x 10 G	24	MIN x 1 UNIT E

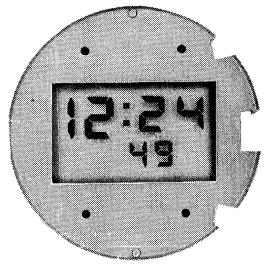
AMERICAN MICROSYSTEMS, INC.

S23610

LOW VOLTAGE FIELD EFFECT
SIX-DIGIT WATCH DISPLAY



MINIMUM VIEWING AREA: .745" x .425"



STANDARD FEATURES

- Low Voltage Drive
- Field Effect Design
- Direct MOS Compatibility
- Exceptionally Low Power Consumption
- High Stability LC Materials
- Glass-to-Glass Seal
- Wide Viewing Angle

OPTIONAL (SPECIAL-ORDER) FEATURES AVAILABLE

- Yellow/Gold Reflector
- Backlighting "Light-Pack"

FUNCTIONAL DESCRIPTION

The AMI S23610 Low Voltage Field-effect Liquid Crystal Six Digit Watch Display is designed to interface directly with MOS watch circuits, including the AMI S-1400 CMOS series. It is a high contrast, very low power, six digit display. This model provides for a continuous display of hours and minutes, and either seconds or date.

The display cell features glass-to-glass seal construction, coupled with highly stable liquid crystal materials, to assure a high degree of mechanical durability and long lifetime.

SPECIFICATIONS

Electrical: @ 25°C, 3 VAC Sq. Wave, 32 Hz, unless otherwise specified.

Operating Voltage:	> 90% 'on' @ 3 VAC < 10% 'on' @ 1 VAC
Current Drain:	250nA typical, 500nA maximum
Capacitance:	400pF typical, 600pF maximum
Frequency Range:	20 Hz to 1 kHz

Electro-Optical: @ 25°C, 3 VAC Sq. Wave, 32 Hz unless otherwise specified

Contrast Ratio:	20:1 Minimum
Off-Angle Viewing:	Contrast ratio is reduced less than 30% when viewed at 30° from the six o'clock position
Response Time:	From trigger signal to within 10% of full change (25°C)

	TYPICAL	MAXIMUM
On Delay	200 msec	300 msec
Off Delay	350 msec	550 msec

The colon blink will be visible @ 10°C

Mechanical:

Dimensional:	See outline drawing
Character Heights:	

Position:	Hours	Min	Sec/Date
	.200"	.170"	.120"

Contact Spacing:	38 contacts total. 37 contacts, .020" wide typ., centered at .040" –Tolerances non-cumulative. 'Common' contact is .040" wide (typ)

Environmental

Operating temperature:	0°C to 50°C
Storage temperature:	- 20°C to 65°C
Humidity (including polarizer):	+ 50°C and 60% RH for moderate periods.
(excluding polarizer):	+ 50°C and 90% RH for moderate periods.

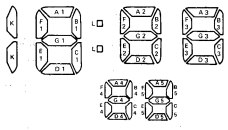
Lifetime

Continuous Operation: Minimum 10,000 hours under recommended CMOS signal conditions. Beyond the minimum lifetime it is expected that the devices will continue to operate indefinitely if not subjected to unusual mechanical, environmental or electrical stresses.

Workmanship

Quality: The viewing area of the display will be free from inclusions, blemishes or non-uniformities in color visible to the unaided eye (<0.010"). The front polarized surface will have no scratches or blemishes that interfere with the legibility of the display when viewed at 10 inches under normal ambient light. The display will have no chips or scratches on the external contacts that interfere with the electrical operation. Marking will consist of the AMI logo, part number and manufacturing date code applied to the back surface. This mark will be sufficiently permanent to withstand normal handling.

CONTACT - SEGMENT IDENTIFICATION



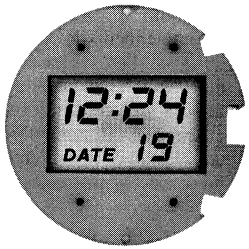
CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION
1	COMMON	14	B5	27	A2
2	COLON	15	A5	28	F2
3	B4	16	F5	29	G2
4	A4	17	E3	30	E2
5	F4	18	D3	31	C1
6	G4	19	C3	32	B1
7	E4	20	G3	33	A1
8	D4	21	B3	34	F1
9	C4	22	A3	35	K
10	E5	23	F3	36	G1
11	D5	24	D2	37	E1
12	C5	25	C2	38	D1
13	G5	26	B2		

AMERICAN MICROSYSTEMS, INC.

S23620

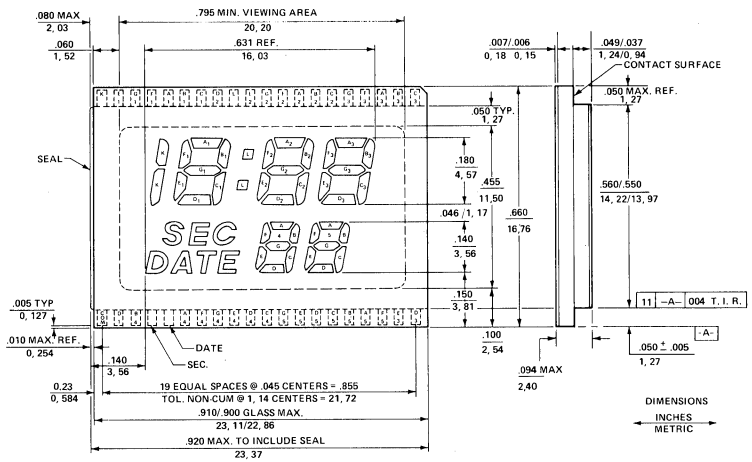
LOW VOLTAGE FIELD EFFECT
LIQUID CRYSTAL WATCH DISPLAY
SIX-DIGIT W/ANNUNCIATORS

ADVANCED PRODUCT DESCRIPTION



DATE MODE

SECONDS MODE



MINIMUM VIEWING AREA: .795" x .455"

STANDARD FEATURES

- Low Voltage Drive
- Field Effect Design
- Direct MOS Compatibility
- Exceptionally Low Power Consumption
- Glass-to-Glass Seal
- High-Stability L-C Materials
- 'Silvered' reflector
- Wide Viewing Angle

OPTIONAL (SPECIAL ORDER) FEATURES AVAILABLE

- Yellow/Gold Reflector
- Backlighting "Light-Pack"
- Thinner Glass Version (.028" ± .004" Glass, Front and Back Planes)

FUNCTIONAL DESCRIPTION

The AMI Model S23620 Watch Display is a Low Voltage Field-effect type, designed to interface directly with CMOS watch circuits. Unique to this six digit display, is the addition of annunciators for the words Seconds (Sec) and Date (Date). This model provides for a continuous display of hours and minutes, and either seconds or date. The annunciators for "Sec" or "Date" are energized for the appropriate function displayed.

The display cell features glass-to-glass seal construction, coupled with highly stable liquid crystal materials, to assure a high degree of mechanical durability and long lifetime.

SPECIFICATIONS

Electrical: @ 25°C, 3 VAC Sq. Wave, 32 Hz, unless otherwise specified.

Operating Voltage:	> 90% 'on' @ 3 VAC < 10% 'on' @ 1 VAC
Current Drain:	250nA typical, 500nA maximum
Capacitance:	400pF typical, 600pF maximum
Frequency Range:	20 Hz to 1 kHz

Electro-Optical: @ 25°C, 3 VAC Sq. Wave, 32 Hz unless otherwise specified

Contrast Ratio:	20:1 Minimum
Off-Angle Viewing:	Contrast ratio is reduced less than 30% when viewed at 30° from the six o'clock position
Response Time:	From trigger signal to within 10% of full change

	TYPICAL	MAXIMUM
On Delay	200 msec	300 msec
Off Delay	350 msec	550 msec

The colon blink will be visible @ 10°C

Mechanical:

Dimensional:	See outline drawing
Character Heights:	

Position:	Hours/Min	Sec/Date	Annunciators
	.180"	.140"	.060"

Contact Spacing:	40 equal contacts centered at .045 ± .004, tolerances non-cumulative.

Environmental

Operating temperature:	0°C to 50°C
Storage temperature:	- 20°C to 65°C
Humidity (including polarizer):	+ 50°C and 60% RH for moderate periods.
(excluding polarizer):	+ 50°C and 90% RH for moderate periods.

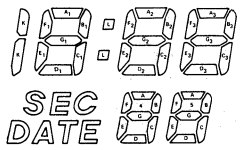
Lifetime

Continuous Operation: Minimum 10,000 hours under recommended CMOS signal conditions. Beyond the minimum lifetime it is expected that the devices will continue to operate indefinitely if not subjected to unusual mechanical, environmental or electrical stresses.

Workmanship

Quality: The viewing area of the display will be free from inclusions, blemishes or non-uniformities in color visible to the unaided eye (<0.010"). The front polarized surface will have no scratches or blemishes that interfere with the legibility of the display when viewed at 10 inches under normal ambient light. The display will have no chips or scratches on the external contacts that interfere with the electrical operation. Marking will consist of the AMI logo, part number and manufacturing date code applied to the back surface. This mark will be sufficiently permanent to withstand normal handling.

CONTACT - SEGMENT IDENTIFICATION



CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION	CONTACT NUMBER	DESIGNATION
1	COMMON	15	5 – C	28	2 – A
2	1 – D	16	5 – B	29	2 – F
3	4 – B	17	5 – A	30	2 – G
4	SEC	18	5 – F	31	2 – E
5	DATE	19	3 – E	32	COLON
6	4 – A	20	3 – D	33	2 – D
7	4 – F	21	3 – C	34	1 – C
8	4 – G	22	3 – B	35	1 – B
9	4 – E	23	3 – A	36	1 – A
10	4 – D	24	3 – F	37	1 – F
11	4 – C	25	3 – G	38	1 – G
12	5 – G	26	2 – C	39	1 – E
13	5 – E	27	2 – B	40	K
14	5 – D				

11

Watches and Watch Products

TDS-4 Time/date/seconds Watch with Backlighted LCD Display.

AMI's Light Emitting Diode Display Watch.

Watches and Watch Products

AMI is among the pioneers in the manufacture of mass marketable digital electronic watches. Even though the introduction of some forms of LED digital watches occurred as early as 1967, not until 1972 or 1973 did a digital type of watch turn from a high priced novelty item into a widely marketable accurate timepiece. At this time AMI took advantage of its MOS/LSI circuit manufacturing capability and its microelectronics product assembly and testing experience and introduced its first watch – the HMM.

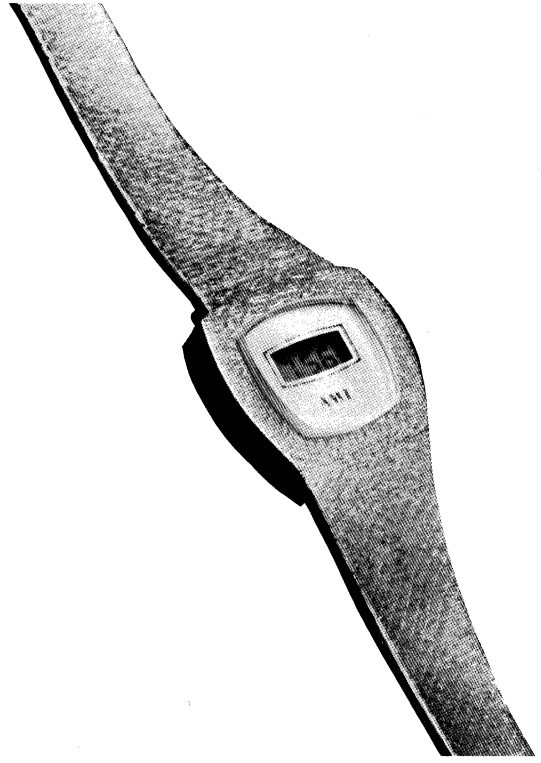
Since 1972 AMI has expanded all facets of its digital watch manufacturing activities and has become one of the largest suppliers of digital electronic watches and watch components in the world. Today AMI has a complete second-generation product line of men's and ladies' watches – using both LCDs and LEDs, and offering backlighted displays, time/date/seconds capabilities, and other sought after features.

A COMPLETE LINE OF WATCHES

The AMI product line consists of six basic models and a number of versions. Among men's watches, AMI manufactures one LED model and four basic LCD models – including 4 and 6-digit time/date/seconds display watches. All LCD time/date/seconds models have backlighted displays for easy nighttime reading.

One of the most notable watches introduced by AMI is the world's smallest digital electronic watch – the petite Amité for ladies. This watch is built around an extremely compact module, designated as the LWM. In the case shown below, the complete watch measures less than 1 in. in cross section (diameter) and less than 3/8 in. in height. As with all other AMI watches, the Amité is sold as a complete assembled watch, in a private label case, or the LWM module is available separately.

The World's Smallest – the Amité for Ladies.



A Ladies' Watch with Elegance – from AMI.

AMI MAKES ITS OWN

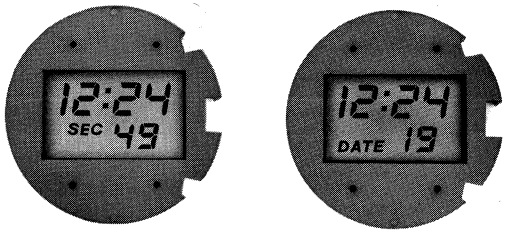
The three basic components of any quartz crystal digital electronic watch are: 1) the integrated circuit, 2) the display – either LCD or LED – and 3) the quartz crystal oscillator. These components are assembled into a watch module (also called a nest), along with a battery, and placed into a case to complete the watch. Because AMI manufactures all of the basic components as well as the modules and finished cased goods, the Company is in a unique position in the digital watch industry. It can offer to any customer a complete watch, mounted in a case of his choice, or any of a number of standard (or custom) watch modules, and also any of the basic components separately.

Other results of such vertically integrated structure are that AMI can be self-sufficient in its manufacturing and assembly activities – without depending on other major sources for critical components – and that AMI is able to closely control the quality of all parts of the watch.

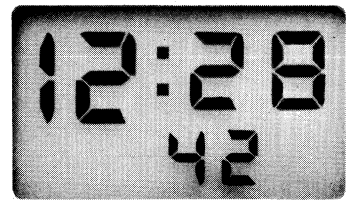
Manufacturing and marketing its products in this diversified manner, AMI keeps its volume up and can take advantage of mass economies in the production of all parts of a watch. This, in turn, allows the Company to maintain a position of leadership in the rapidly changing economic environment of the digital watch market and support the research and development needed in a rapidly advancing technology.

Integrated Circuits

It was the advent of CMOS/LSI integrated circuits, with their low power consumption feature, that brought digital electronic watches into existence. AMI manufactures a wide variety of CMOS and other types of watch and clock circuits, for use in their own watch modules and for direct sale to other manufacturers of timekeeping equipment. All watch circuits are complete on a single IC chip and are variously available unmounted, mounted in a chip carrier, or on a miniature circuit board, ready for insertion in men's and ladies' watch modules. Section 9 contains a complete description of the standard watch and clock circuits offered by AMI.



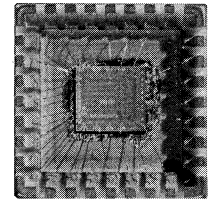
TDS-6 Watch Module.



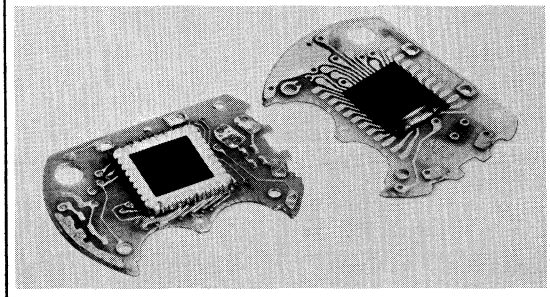
Liquid Crystal Display.

Watch Displays

AMI is also one of the largest and most experienced manufacturers of field-effect liquid crystal watch displays. As are the integrated circuits, so the liquid crystal displays are used both in AMI produced watches and sold to various other users. They are available in different sizes, with various color reflectors, and with



Watch Chip Mounted in Carrier.



PC Boards Ready for Insertion into Modules.

backlighting attachments. All displays operate on 3 volts, and require minute amounts of power, thus assuring maximum battery life in watches. See Section 10 for a description of LCD displays manufactured by AMI.

Quartz Crystal Oscillators

The quartz crystal oscillator, which vibrates 32,768 times per second, provides the basic frequency used by the watch circuit to keep time. Consequently, the accuracy and consistency of the crystal frequency over a long time period, and with variations in temperature and other conditions, determines the timekeeping accuracy of the watch. The quartz oscillators manufactured by AMI are designed specifically for watch circuits and allow AMI to guarantee accuracies typically around 5 seconds per month.

Watch Modules

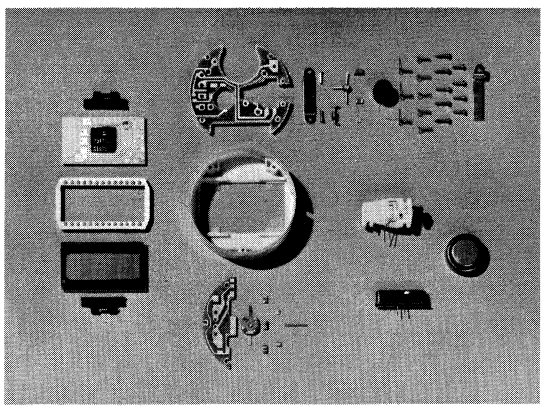
The design and manufacturing expertise that goes into the integrated circuits, displays, quartz crystals, and other components, is realized in the final assembly of the small presicion watch module. AMI builds a number of different modules, both for men's and ladies' watches, and with either LCD or LED type displays. Standard modules fit into a variety of different cases and AMI also designs and manufactures custom modules for individual watch manufacturers. To assure ruggedness and reliability, the modules are built to exacting standards and under rigid quality controls.

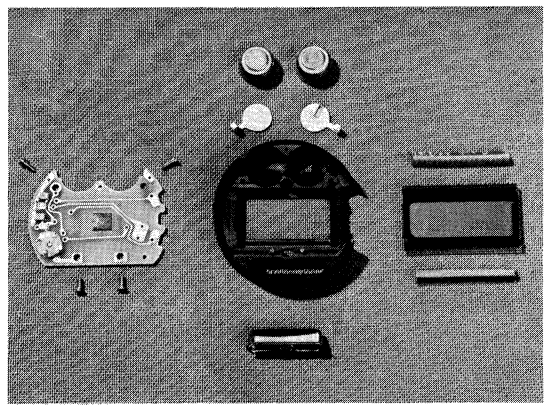
R & D KEEPS AMI AHEAD

One of the main reasons for the success of AMI in the digital electronic watch market is its research and development program. From the time when AMI began to manufacture watches, the Company has maintained a strong and independent research and development organization, primarily oriented toward basic research in technologies related to watch products.

With such orientation the R&D group has continuously provided a strong technological basis for innovations and new product development by design engineering. For example, AMI was the first to introduce low-voltage LCDs and the current second-generation men's watch product line is the most advanced in the industry. Strength in R&D also enabled AMI to introduce the remarkable ladies' Amité.

This R&D tradition provides assurance to the consumer of the continued excellence of AMI watch products in the future.





The above photo shows all parts that make up the HMM and CWM watch modules. It demonstrates the dramatic simplification of the second generation CWM (right) over the earlier HMM (left).

12

AMI Product Assurance Program

Product Assurance Program

INTRODUCTION

Quality is possibly one of the most used, least understood, and variously defined assets of the semiconductor industry. AMI learned early just how important effective quality assurance, quality control, and reliability monitoring can be in the ability of a manufacturer to deliver a repeatably reliable product. Particularly through the manufacture of custom MOS/LSI, much experience has been collected at AMI, indicating that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions: Quality Control, Quality Assurance, and Reliability. Each function has a different area of concern, but all share the responsibility for a reliable product.

The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program – Quality Control, Quality Assurance, and Reliability – have been developed as a result of many years of experience in MOS device design and manufacture. **Quality Assurance** establishes that the product meets, or fails to meet, product parameters – *QA checks results.* **Quality Control** establishes that every method meets, or fails to meet, processing or production standards – *QC checks methods.* **Reliability** establishes that QA and QC are effective – *Reliability checks device performance.*

As an indication that the AMI Product Assurance Program has been effective, NASA has endorsed AMI products for flight quality hardware since 1967, the Mars Landers and Lunar Landers all have incorporated AMI circuits, the Viking program utilizes AMI circuits, and many military airborne and reconnaissance hardware programs have depended on AMI devices.

QUALITY CONTROL

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of MOS devices and device production, from the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- Incoming Materials Control
- Microlithography Control
- Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are also performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences serve as examples of the thoroughness of AMI Quality Control.

- Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.

- Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage, or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are artwork generation, photoreduction, and the actual printing of the working plates.

Artwork, whether Rubylith, Gerber Plots, AMI generated or customer generated, is thoroughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must conform to stringent design rules, which have been developed over a period of years, as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For typical P-channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. In this sequence, a sliding sampling plan is used, determined by the type of product and process, complexity, and results experienced. The plates can be rejected first by manufacturing, when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program – the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to specifications. This involves checks on operators, equipment, and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

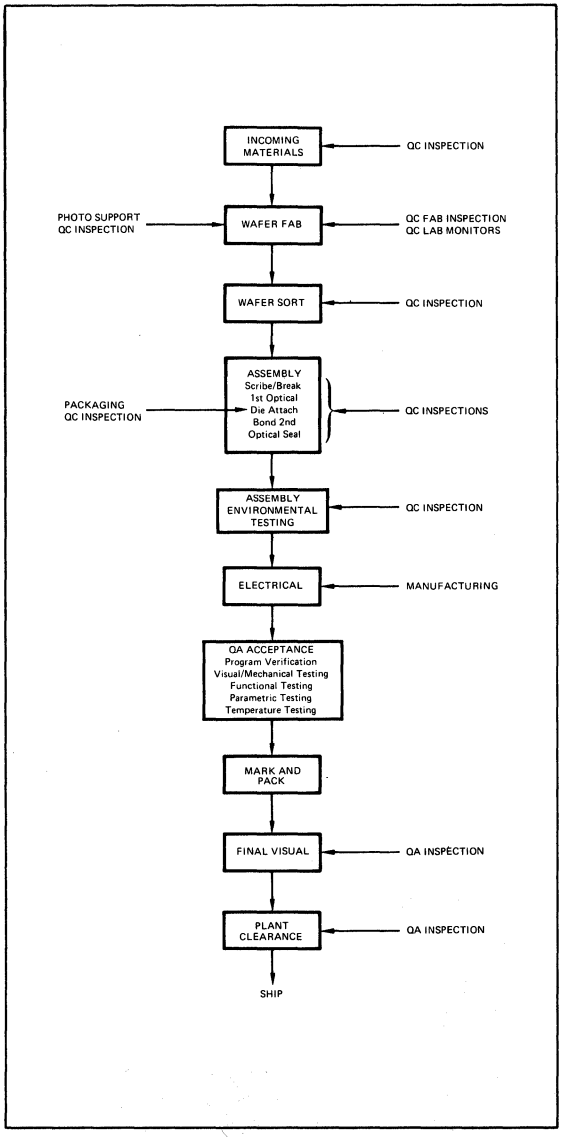
Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the QC Fabrication Group, a QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking, and evaporization are the most closely monitored steps.

Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows the corrective action taken.

Optical inspections are performed at several steps. For example, during wafer sort visual inspection for probe damage and alignment is performed; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

Figure 1. Flowchart of Product Assurance Program Implementation



QUALITY ASSURANCE

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintainance of AMI internal product specifications, to assure that they are always in conformance with customer specifications, or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing either with an LTPD of 10%, or less, if the specification requires tighter limits.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature levels. In addition, a number of other special temperature tests may be performed, if required by the specification. Generally, high temperature tests are at 125°C.

To perform the tests, QA uses AMI *PAFT* test systems, ROM test systems, Macrodata testers, Fairchild *Sentry* systems, Western Digital *Spartan* systems, *Impact* testers, and various bench test units. In special instances a part may also be tested in a real life environment, in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance, but it is identified as a *second-time* lot. If it fails again, it is discarded and corrective action in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run, to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts are sent from finished goods, they are again checked by the QA group to a 10% LTPD, with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA, to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) After QA evaluates all returns, they are sent to Reliability for failure analysis.

RELIABILITY

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification, and failure analysis. All are constantly monitored. To perform these functions AMI Reliability group is organized into two major areas:

- Reliability Laboratory
- Failure Analysis

Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions:

- New Process Qualification
- Process Change Qualification
- Process Monitoring
- New Device Qualification
- Device Change Qualification
- Device Monitoring
- New Package Qualification
- Package Change Qualification
- Package Monitoring
- High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package, or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective, the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of new processes. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what may be included on a typical rel chip:

- A discrete inverter and an MOS capacitor
- A large P-N junction covered by an MOS capacitor
- An additional MOS capacitor
- A large P-N junction area (identical to the junction area above, covered by the MOS capacitor)
- A long conductor, which crosses a significant number of etched cutouts
- Several conductors, which cross a deeply etched area

These parts of the rel chip each allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor crossing a number of etched cutouts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by increased currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for the manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts on-going process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

Package Qualification

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

SUMMARY

The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliable, with a very low reject level.

13

Application Notes

Application Notes Available

AP74-3	S2144 8-digit, 4-function Calculator
AP75-4A	S9411 8-digit, 5-function Calculator (LED)
AP74-5	S9412 8-digit Multifunction Calculator (LED)
AP74-6	S9412 8-digit Multifunction Calculator (Fluorescent Display)
AP75-8	Dynamic RAMs are Easy and Economical *(See page 13-3)*
AP75-9	Designing with 1103 Memories *(See page 13-17)*
AP75-10	MOS Circuits for Electronic Organs *(See page 13-23)*
AP75-11	Testing Dynamic RAMs *(See page 13-31)*
AP75-12	Digital Electronic Clock Circuits Using the S1998

AMERICAN MICROSYSTEMS, INC.

APPLICATION NOTE
AP75-8
MARCH, 1975

Dynamic RAMs are Easy and Economical

Les Brock

INTRODUCTION

Traditionally, dynamic read/write memories have been held with some disdain by system designers, who often undertake specific efforts to avoid using them. The reason, of course, is that a dynamic RAM must be periodically refreshed to maintain the information stored in its capacitive storage cells while a static RAM requires no refresh circuitry nor refresh time for the device to operate totally asynchronously. The reasoning runs along these lines: "Why should I design with a dynamic RAM since this requires that I cope with the additional cost and design of refresh circuitry as well as consider the time consumed by the refresh cycle when this isn't necessary in a static RAM?" The answer to such a question is simply this: dynamic RAMs cost much less than static RAMs, refresh circuitry is very simple and inexpensive, and the refresh cycle uses as little as 1% of the time a dynamic RAM is used in a system. The system designer who takes the time to analyze just how easy it is to use dynamic RAMs can realize significant cost and power advantages with little or no loss in system speed. With a little information, and a little work, a designer can cut memory system cost in half. And let's face it, total system cost must be the primary design consideration.

THE ECONOMICS OF DYNAMIC RAMs

Today, dynamic RAMs cost significantly less than comparable static RAMs. In a system using dynamic RAMs, the additional cost of refresh circuitry runs between $5 and $10, and this cost remains the same whether two dynamic RAMs are used or two hundred are required in a given system. For the sake of comparison, assume a cost of $8 for refresh circuitry and output sense amplifiers for a 1024-bit dynamic RAM, such as the AMI S4006. Now, in a small system using only two RAM circuits, this extra circuitry runs $4 per RAM, but in a system using 16 RAM devices, this circuitry costs only 50 cents per RAM. Remembering that dynamic RAMs can cost as little as half the cost of static RAMs, the cost advantages even in a 16-device memory system (2K-word x 8-bit) are significant.

Another important cost consideration involves developments in the RAM field in the foreseeable future. Present trends indicate that the 1024-bit static RAMs will not be cost competitive with 1024-bit dynamic RAMs for at least another year to year-and-a-half. Also, 4K dynamic RAMs are just entering the marketplace, and they will be competitive with 1024-bit dynamic RAMs almost immediately. Static RAMs, on a cost basis, will probably never be competitive with a 4K dynamic RAM. So, design with easy to use dynamic 1024-bit RAMs now, and be ready to work with the 4K dynamic RAMs with the confidence of experience.

THE SIMPLICITY OF REFRESH

Dynamic RAMs such as the S4006 cannot store data indefinitely unless the stored data is written back into the capacitive storage cells periodically. This writing back of stored data is called Refresh. The Refresh operation can be performed either during the Write operation, or during a separate Refresh cycle. In a 1024-bit memory such as the S4006, there are 32 Row and 32 Column addresses. If all Row addresses are continually addressed during normal Write operations in less time than the Refresh operation requires, no special Refresh cycle is necessary. When normal Write operations do not provide this automatic refresh, a separate Refresh cycle can be used. This Refresh cycle is very simple. The only difference between the Refresh and Write operations is that the Chip Enable input is disabled (held HIGH). Disabling the Chip Enable input removes data from the output and prevents any new data at the input from being stored. The time required for a separate Refresh

operation with a 1024-bit memory is 32 times the Write cycle time. A system providing transparent or invisible Refresh for a 2K-word by n-bit memory using S4006 family circuit is discussed in detail later in this paper.

There is an interesting comparison that can be made between the Read/Write/Refresh operations of an S4006 type dynamic RAM and the Read/Write operations of a static RAM such as the 2102. As far as the Address and Read functions are concerned, a 4006 dynamic RAM and 2102 static RAM are virtually identical. From the point of view of the Write function, however, a 4006 dynamic RAM performs either the Write function, or the Refresh operation, using only a single clock pulse. A static RAM such as the 2102, on the other hand, has a special requirement for a Write operation. The 2102 requires an advance notification of 50 ns before an address change so that the Write pulse can go from a LOW to a HIGH. No memory is capable of ESP, so the static RAM must always be returned HIGH immediately after a Write operation, waiting at least 50 ns for the next Write address. This requires another clock, or clock pulse, so the static RAM in effect requires one more clock pulse than the dynamic RAM. In other words, the S4006 requires only one clock to clock the Write pulse from a HIGH to a LOW, and the address change clocks the Write pulse back to a HIGH level. The 2102, however, not only requires the one clock to clock it from a HIGH to a LOW, but it must be clocked back HIGH again after the Write pulse to make sure that it is HIGH for at least 50 ns before the next address.

The dynamic S4006 RAM requires a single clock pulse while the static 2102 RAM requires two, and a memory such as an 1103 1K dynamic RAM requires three. And refreshing the S4006 only requires holding $\overline{CE}$ HIGH during the Write cycle for 32 Rows of address, or 32 times the Write cycle. Since the refresh circuitry can handle an almost unlimited number of S4006 RAMs and utilizes only standard, off-the-shelf TTL SSI and MSI components, obviously, the idea of refresh can't be that bad.

COMPATIBILITY

Dynamic RAMs are less expensive, consume less power, and are as fast as static RAMs. The S4006 RAM family also offers the added advantage of pin-for-pin compatibility with the 2102 1024-bit static RAM. This means that when 2102 prices become competitive with S4006, designers can convert from a dynamic RAM system to a static RAM system by merely leaving off the refresh circuitry.

A 2K-WORD X 8-BIT RAM USING THE S4006

The block diagram in Figure 1 shows the typical organization of a 2K-work by 8-bit memory using S4006 RAMs. This system incorporates input buffers and output sense amplifiers for total TTL compatibility. Also, an invisible refresh circuit, described in

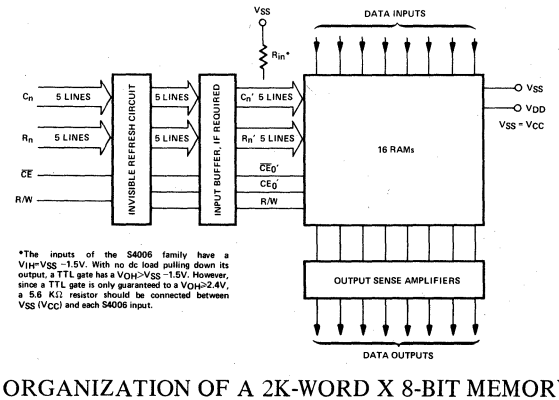


FIGURE 1. TYPICAL ORGANIZATION OF A 2K-WORD X 8-BIT MEMORY USING S4006 RAMS.

detail later, is included. Such a refresh circuit could be built on a separate printed circuit board in order to drive several S4006 RAM boards.

A memory system using S4006 devices can accept asynchronous address changes only when the R/W line to the chip is HIGH. Therefore, in a truly asynchronous addressing system, the Write pulse must be considered because the memory could be refreshing when it is not being addresses. An interesting feature of the Refresh circuitry, to be discussed next, is that after the first Read or Write cycle time (which for worst case includes one t_{WP} from the prior Refresh cycle) the entire memory can be accessed at the actual chip access time. If the time between two address changes is longer than $t_{WC} + t_{AW}$, memory Refresh occurs, and the R/W line will go LOW and not allow a new address to be entered until the end of t_{AW}. However, as long as new address changes occur within t_{AW}, they will be accepted and the memory cycle time will be equivalent to the actual cycle time of the RAM chip itself.

INVISIBLE REFRESH FOR A DYNAMIC RAM SYSTEM

The refresh circuit shown in Figure 2 can be used for a 2K-word by n-bit completely asynchronous read/write memory system using S4006 family RAMs. It is easily expandable to a 32K-word system

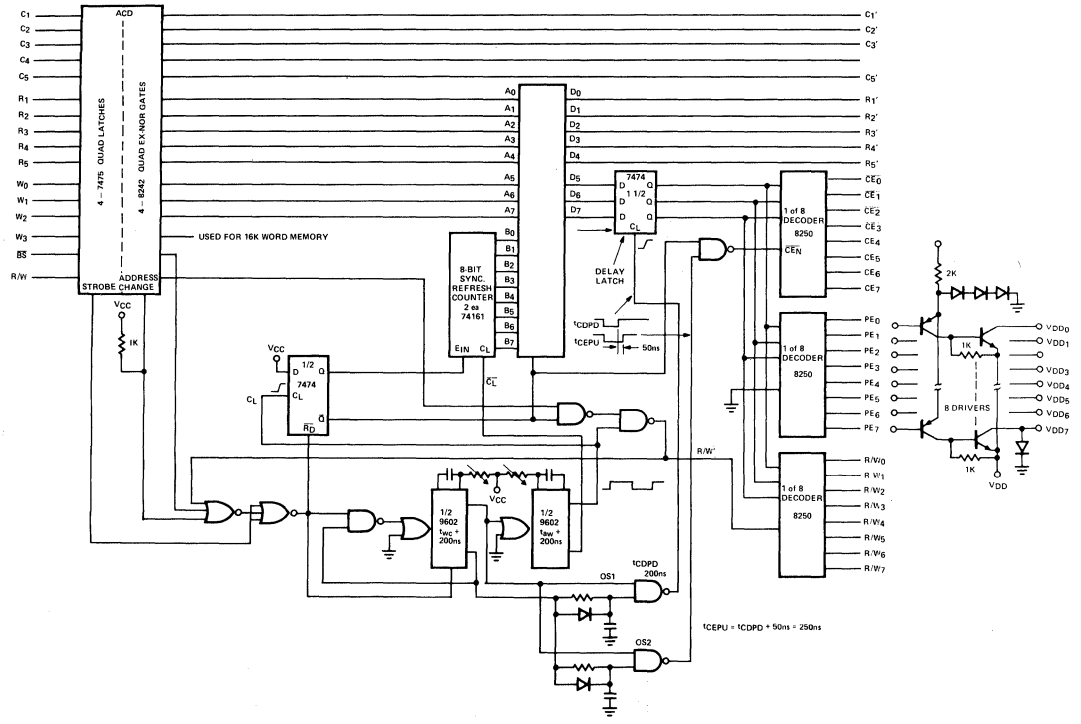


FIGURE 2. INVISIBLE REFRESH AND POWER DOWN FOR A 8K WORD X N BIT MEMORY USING THE 4006 FAMILY

with the addition of only three TTL devices. Because S4006 family device inputs are TTL compatible, standard SSI and MSI TTL components can be used producing the lowest cost high speed invisible refresh system. The S4006 family only requires a low power TTL gate or grounded emitter transistor for output sensing.

This refresh system consists of three basic functions; an Address Change Detector (ACD), a Multiplexer (MUX), and the Control Logic, Oscillator and Refresh Address Counter (CLORAC).

Address Change Detector (ACD)

The refresh system control logic requires indication of an address change which is the function of the ACD. The ACD uses three quad latches and three quad Exclusive NOR gates to detect an address change and asynchronously indicate this change to the CLORAC. The address stored in the latches is compared to any new address in the Exclusive NOR gates. If the addresses are different, the appropriate wired-OR Exclusive NOR gate output goes LOW pulling the Address Change (AC) line LOW. Given the condition that the Board Select input (BS) is LOW, and that none of the RAMs is recieving a write pulse, a new address can be strobed to the input latches. Once this occurs, the addresses being compared by the Exclusive NOR gates are the same, and all Exclusive NOR outputs return HIGH.

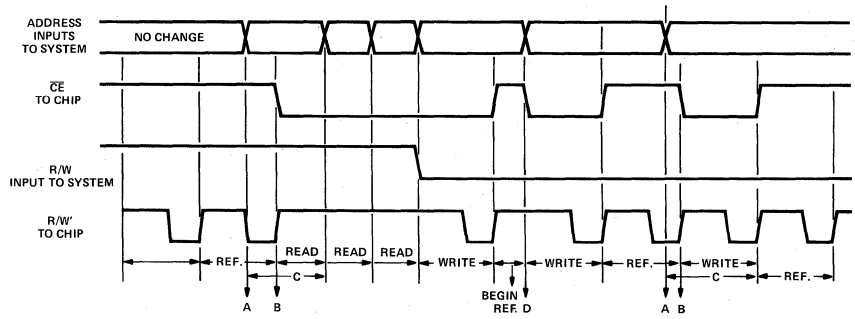
Multiplexer (MUX)

In this refresh system, two quad 2-input multiplexers simply function as an 8-pole double throw switch, multiplexing the Row Address, Chip Select and Read/Write terminals of the RAM system between the system inputs and the refresh inputs.

Control Logic, Oscillator and Refresh Address Counter (CLORAC)

All necessary control signals for the multiplexer and the address change detector are generated by the CLORAC. Any address change detected by the ACD is not accepted by the CLORAC unless the Board Select input is LOW and a write pulse is not being applied to the RAMs. If these conditions are met, the new address is accepted and stored, the oscillator is synchronized, and the refresh flip-flop is reset for memory Read or Write operation. Immediately, a full oscillator cycle is started ($t_{AW} + t_{WP}$).

In a Write operation, if a new address is not applied at the end of the Write Cycle ($t_{AW} + t_{WP}$), then the refresh flip-flop is automatically clocked into the refresh state (Q_{REF} = HIGH). This refresh operation continues until an address change is detected and applied. If no address change occurs during a time equal to 32 Write Cycle times, all RAM storage



A – New Address is Not Accepted During WRITE PULSE (twp).
B – New Address is Accepted at End of WRITE PULSE.
C – Worst Case Cycle Time Must Include Waiting For Completion of WRITE PULSE.
D – Refresh May Be Aborted if the Address Changes Before R/W Goes LOW.

FIGURE 3. WAVEFORMS GENERATED BY THE INVISIBLE REFRESH CIRCUITRY

elements are automatically refreshed. Refreshing is accomplished with the Chip Select input disabled (HIGH) while the synchronous binary refresh counter increments through all 32 Row addresses simultaneously with a write pulse being applied to the Read/Write input. If the RAM is not completely refreshed due to continuous Read cycles, every 2 ms (for the S4006 and S4008), address changes must be inhibited to allow completion of the refresh. Any time a refresh of a Row address is aborted due to the application of a new input address for reading or writing, the aborted refresh Row address will be re-applied to the RAM when refresh resumes.

INPUT/OUTPUT BUFFERING

Input Buffering

All inputs to the S4006 family devices are TTL compatible simply by using a pull up resistor. Some users prefer not to buffer the inputs at all. However, to provide input buffering, for example, for a 2K-word by 8-bit memory with each input at 5 pF, the address lines would present 80 pF (16 x 5 pF). This 80 pF capacitance can be easily buffered with a standard 7404 hex inverter. In larger memory systems, a high current driver such the Signetics 8T90 quad bus driver should be used to provide adequate buffering for the Address and Read/Write inputs.

Output Buffering

System access time is strongly influenced by the type of interface circuit used to convert the memory output signals to system logic levels. Several methods are in common use, ranging from a simple transistor/resistor combination to dual line receivers and 3-state output buffers. Sense amplifiers vary in performance specifications from very fast, high threshold types to slower, low threshold circuits. The output sense amplifier method selected depends on the particular memory applications, again with speed and cost the primary considerations.

The simplest output sense amplifier configuration is just a transistor (2N2639 or equivalent) and a resistor, Figure 4a. This current sourcing method provides higher speeds because the propagation delay through the output structure is minimal compared to

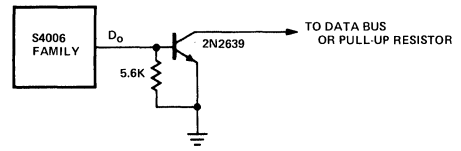


FIGURE 4a. SIMPLE SENSE AMP

other methods. It is also an inexpensive approach. A possible disadvantage of this sense amplifier is that since each column of the memory, regardless of the number of rows, requires two discrete components, this could represent substantial space on the printed circuit board.

Another method for converting small signal MOS outputs to TTL logic levels uses a dual line receiver such as the TI 75107 as the sense amplifier. This circuit switches its output to a TTL logic HIGH level when the 75107 non-inverting (or positive) input is 25 mV more positive than the inverting (or negative) input. Conversely, the 75107's output switches to a TTL logic LOW level when the non-inverting input reaches a level 25 mV below the inverting input reference voltage. This means there is only a 50 mV window where the 75107 output is undefined. This approach offers simplicity, economy and adequate speed. It does, however, require one IC package and two resistors for each column in the memory, Figure 4b.

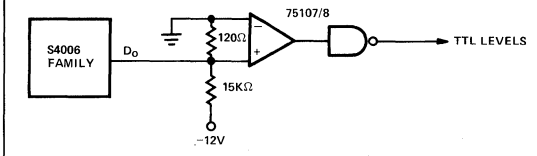


FIGURE 4b. 75107/8 DUAL SENSE AMP

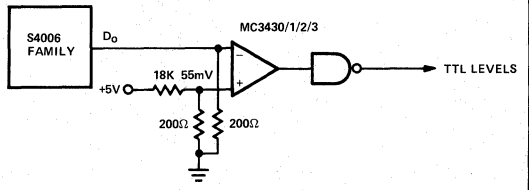


FIGURE 4c. MC3430/1/2/3 QUAD SENSE AMP

A third approach to output sense amplifiers for the S4006 family utilizes a quad differential voltage comparator such as the Motorola MC3403-33 devices. These devices are high speed comparators with a special specification called input Sensitivity, a parameter derived by combining the effects of input offset voltage, input offset current, voltage gain, temperature variations, and input common mode range. This parameter specifies the minimum differential input which guarantees a given logic level. One quad comparator operates as a single package sense amplifier for four columns of memory. Each column is tied to one of the inverting inputs of the comparator and to ground through a 200Ω resistor. The only other components necessary are in 18 kΩ resistor on the +5 V line, which feeds all the comparator non-inverting inputs and is also tied to ground with another 200Ω resistor. This approach provides outputs compatible with standard TTL loads (10 UL) with a propagation delay of 40 ns, all in a single IC package for 4-bit memories. A 16-bit memory system would only require four quad comparators, Figure 4c.

All of the output buffering approaches discussed for the S4006 family devices can be driven by a 2102 static RAM. Even though these devices are directly compatible, the fact that these output buffering circuits can be driven by a 2102 makes a dynamic RAM system designed for the S4006 family devices readily adaptable to using 2102 static RAMs.

POWER DOWN OPERATION

Significant reductions in power requirements and dissipation are possible by incorporating some power down capability in a memory using S4006 family devices. Typically, the powered down mode results in a device power dissipation figure of 25 mW, compared to 350 mW in the full power mode. Worst case figures run at 50 mW in power down operation versus 570 mW at full power.

As a practical example, a 16K-word x 8-bit memory (a total of 120 RAMs) dissipates 44.8 W (350 mW x 120). The same memory incorporating power down circuitry which powers up only 1K words at a time dissipates only 5.8W (2.8W for the powered up words, 3W total for all 15 other RAMs). This is a dissipation figure only 13% of that at full power. More startingly put, the full power up system dissipates 772% more power than the powered down mode.

There are a few considerations that the system designer must remember when adding a power down mode to an S4006 family system.

- All RAMs should not be powered up simultaneously
- R/W and $\overline{CE}$ must remain HIGH during the power down mode and until the system is powered up.
- R/W must be HIGH 20 ns prior and $\overline{CE}$ must be HIGH 200 ns prior to reaching 95% of V_{DD} full power when V_{DD} is being turned off.
- Rise and fall time of V_{DD} must be greater than 20 ns.

If all RAMs are powered up simultaneously, there are obvious problems with a large power spike and heat. The R/W line must remain HIGH (READ) during power down, otherwise the memory would try to write and there would be insufficient power to do so. The $\overline{CE}$ line must remain HIGH (DISABLED) during power down because the system would try a READ operation (R/W HIGH). In both cases, it would be possible for undetermined changes to occur in the memory, a very undesirable possiblity, Figure 5. By lowering the V_{DD} supply voltage to system ground (V_{SS} − 5 V), power dissipation can be reduced to about 50 mW without loss of stored data. The V_{DD} supply should be returned to −12V and a refresh operation initiated if the standby mode is

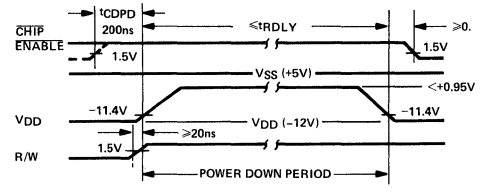


FIGURE 5. STANDBY MODE TIMING REQUIREMENTS

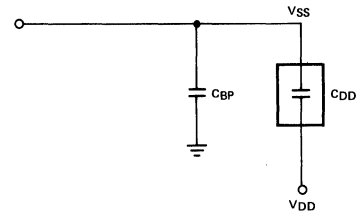


FIGURE 6. BYPASS CAPACITOR

maintained for 2 ms. Following the return of V_{DD} to −12V, Read or Write operations may commence. The rise and fall times of V_{DD} must be greater than 20 ns. t_{ACC} and t_{AW} for the first bit after power up are 100 ns longer than in normal operation.

Assuming a requirement that both R/W and $\overline{CE}$ be HIGH at least 200 ns (t_{CDPD}) prior to power down (V_{DD} at 95%) creates two possibilities.

- A t_{CDPD} of 200 ns plus 50 ns for power-up stabilization can be inserted between new addresses permitting only 1024 words to be powered up at a time. This adds 250 ns to the normal cycle time.
- An overlap of t_{CDPD} length when two 1024 words could be powered up simultaneously would allow addressing at the nominal cycle time of the memory. However, this simultaneous powering up of two 1024 words would create a power supply current spike 250 ns long.

Figure 2 illustrates the first possibility for an 8K-word by n-bit memory. When an address change is detected, D_5, and D_6, and D_7 (the Chip Select lines) are stored for 200 ns (t_{CDPD}) after the address change. During this t_{CDPD} period (OS. 1), $\overline{CE}_n$ and R/W_n are held HIGH. At the end of t_{CDPD}, PE_n changes to the new address, and $\overline{CE}_n$ is held HIGH for another 50 ns while the address is powered up. Thus, $\overline{CE}_n$ is held HIGH for a total of 250 ns, or $t_{CEPU} = t_{CDPD} + 50$ ns (OS. 2). The write cycle period, t_{WC}, is increased 250 ns to incorporate the t_{CEPU} period.

Power Bypass

There is another important aspect to power down operation. In a power down mode, if V_{DD} turns on and off quickly, significant transients could exist because the chip, from V_{DD} to V_{SS}, represents a capacitance of 75 pF. A bypass capacitor is requried to minimize V_{SS} line noise. This bypass capacitor (C_{BP}), in order to bypass a voltage transition on V_{DD}, must be equal to chip capacitance (C_{DD}) times the ratio of delta change in V_{DD} (ΔV_{DD}) and delta change in V_{SS} (ΔV_{SS}).

For a sample calculation, assume C_{DD} = 75 pF, ΔV_{DD} = 12V, and ΔV_{SS} = 0.5 V, thus

$$C_{BP} = 75\text{ pF}\ \frac{12\text{V}}{0.5\text{V}} = 1800\text{ pF}$$

A system using eight S4006 RAMs would require a bypass capacitor of approximately 0.019μF. For lower transitions (ΔV_{SS}), a .47 μF bypass capacitor would still provide a ΔV_{SS} of only 15 − 17 mV.

$$C_{BP} = 0.47\ \mu\text{F}$$

$$\Delta V_{SS} = \frac{75\text{ pF}}{0.47\ \mu\text{F}} \times 12\text{ V} \times 8\text{ RAMs} = 15\text{ mV}$$

CARE AND FEEDING OF THE S4006 FAMILY

As with any MOS circuit, there is a certain danger of input damage and electrostatic damage. In addition with dynamic logic, there can be noise problems such as ringing and crosstalk. These areas pose

no real problem, however, if some simple "preventive medicine" is practiced when designing with MOS circuits.

Ringing and Crosstalk

In any dynamic system, any parasitic inductance tends to cause ringing on the clock edges. Pull up resistors on all inputs sometimes help to avoid such ringing. However, the inputs should not be allowed to go more than 0.3V above V_{SS}. In fact, if the input diodes become forward biased, holes will be injected in the substrate causing random loss of bits of the memory. In effect, these holes cause a level change on the storage node, so a HIGH, for example, would change to a LOW, with resulting loss of information. One very effective approach to solving this problem is simply putting one diode drop below V_{SS} on the pull up resistors. This only requires tying all input resistors to one diode. This works quite well with S4006 devices because an input HIGH is guaranteed to be greater than $V_{SS} - 1.5$ V.

In a memory system using S4006 family devices, crosstalk occurs primarily because of distributed parasitic coupling capacitors. Parasitic coupling occurs throughout a system—in the clock driver, on the PC board, in the wiring, and in the MOS device itself. As a result, the clock signals react to each other: whenever one clock level changes, the other attempts to change.

As far as coupling capacitors in the device itself, only the selection of a circuit with minimized crossover capacitances can have any effect in reducing crosstalk. The S4006 family devices exhibit very low internal crossover capacitances. To avoid crosstalk caused by other system connection, two simple precautions should be taken. Use separate clock drivers for each phase in the system, and keep clock lines, on the boards or in the wiring, away from each other.

Electrostatic Damage

MOS inputs can be damaged by an accumulated static charge because they have a high dc impedance. Typically, manufacturers provide protection against such damage by incorporating an input structure to drain off any excess accumulated charge to the substrate before any damage is done to the gate of the input transistor. There are circumstances, however, which can still cause problems for the unwary. These include unterminated inputs, careless soldering methods, and handling the devices in a static charged environment.

Unterminated, or floating, MOS inputs are not necessarily HIGH or LOW. Assuming that they are at a logic HIGH level, as in the case for TTL inputs, can cause a non-catastrophic failure since a control input, for example, could switch the device to an unexpected operating mode. This happens when the static charge accumulation reaches the input switching threshold. The device may not be damaged, but there would be an apparent malfunction. MOS devices mounted on a PC board should be considered just as vulnerable, because an unterminated trace on the board is still an open line. All traces on the board connected to MOS inputs must therefore be terminated somehow prior to the traces leaving the board. A TTL buffer, a pull up resistor, or an MOS device output all provide very satisfactory terminations. Shipment and storage of MOS devices, alone and on boards, must consider such input termination. The device pins and board edge connectors for inputs require some kind of protection; conducting foam or tubes, or shunts.

Soldering MOS inputs requires grounded soldering equipment. The use of an unisolated solding iron can cause an excessive static charge.

When working with MOS devices, personnel should not wear clothing which picks up static electricity, such as silk or some of the nylon synthetics. Enough of a static charge can be generated to damage the MOS input transistors.

Obviously, a few simple precautions observed when handling MOS devices can eliminate device failure, operation malfunction, and a lot of troubleshooting headaches.

CONCLUSION

Dynamic RAMs are not as difficult to design with as is believed, and they offer significant cost

advantages over static RAMs. Presently, S4006 family devices are more cost effective than comparable 1024-bit static RAMs such as the 2102 family. Also, 4096-bit dynamic RAMS will be even more cost effective. As costs decline for 1024-bit static RAMs, they may become competitive with 1024-bit dynamic RAMs, but this is certainly not true of 4096-bit dynamic RAMs.

Refresh circuitry is not difficult and uses a negligible amount of time in a typical system (as little as 1%). The refresh circuit described is automatic and thus the term invisible. Except for the refresh activity, the S4006 family dynamic RAMs, for all practical systems considerations, functions exactly as a static RAM.

As a matter of convenience, it is a much easier design transition from work with S4006 family dynamic RAMs to systems which will be using the new 4096-bit dynamic RAMs. Also, by designing now with dynamic RAMs, the system engineer will have that much more experience and expertise when he is faced with the 4K RAM devices.

APPENDIX I – TESTING THE S4006 FAMILY

The testing of an MOS/LSI dynamic RAM includes several test methods which require some explanation. Considerations such as the time which would be required for all possible tests of a 1024-bit memory, for example, indicate that selected tests for worst cast conditions are desirable. Other factors, such as access time and refresh are also reasons why the testing of dynamic RAMs is somewhat different.

A dynamic RAM has a memory matrix, decoders, buffers, read/write circuits, and sense amplifiers, all possible sources of either functional or parametric failures. Effective test programs exercise these internal systems thoroughly to detect internal malfunction, usually by determining and using worst cast test conditions. This appendix discusses some of the factors concerning three areas of testing; pattern sensitivity, access time, and refresh.

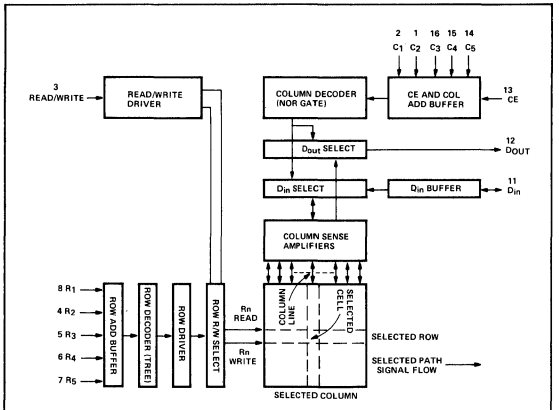


FIGURE 1. SIGNAL FLOW FOR SELECTED ROW/COLUMN

PATTERN SENSITIVITY TESTING

Pattern sensitivity tests can be divided into four categories.

- Bit/Decoder Testing
- Column Short Testing
- Row Short Testing
- Disturb Testing

An abbreviated listing of these tests and the test sequence for each is shown in Table I. Table II illustrates the relationship between the physical arrangement of the memory matrix and the external address inputs. Both Row and Column addresses correspond directly to the internal organization of the memory, with the binary 00000 corresponding to Row or Column 0, and 11111 corresponding to Row and Column 31.

Bit/Decoder Test

The proper function of the individual memory cells, as well as the row and column address decoders, can be checked by one simple test. Parity of the tester address bits determines the data pattern used, Table III. The binary locations shown correspond to the binary row and column locations listed in Table II.

TEST	SEQUENCE		DATA INPUT	COMPARISON
	OPERATION	CE		
BIT/DECODER*	WRITE	E	PARITY	
	READ	E		PARITY
COLUMN SHORTS,	WRITE	E	V BAR	
NO WRITE DURING	WRITE	D	$\overline{\text{V BAR}}$	
DISABLE	READ	E		V-Bar
ROW SHORTS,	WRITE	E	H-Bar	
NO READ DURING	READ	D	1	0
DISABLE, MAXIMUM	READ	E	0	H-Bar
POWER				
DISTURB	WRITE "ONES" INTO ROW	E	1	
	WRITE "ZEROES" INTO ADJACENT ROW	E	0	
	CONTINUE WRITE INTO SAME ROW	E	0	
	READ FIRST ROW "ONES"	E		1

*This test repeated with complemented data

TABLE I. PATTERN SENSITIVITY TESTING

							COL	0	1	2	3	4	27	28	29	30	31
							C_1	0	1	0	1	0	1	0	1	0	1
							C_2	0	0	1	1	0	1	0	0	1	1
							C_3	0	0	0	0	1	0	1	1	1	1
							C_5	0	0	0	0	0	1	1	1	1	1
							C_4	0	0	0	0	0	1	1	1	1	1
ROW	R_5	R_4	R_3	R_2	R_1															
0	0	0	0	0	0			1	3	5	7	9	55	57	59	61	63
1	0	0	0	0	1			65	67	69	71	73	119	121	123	125	127
2	0	0	0	1	0			129	131	133	135	137	183	185	187	189	191
3	0	0	0	1	1			193	195	197	199	201	247	249	251	253	255
4	0	0	1	0	0			257	259	261	263	265	311	313	315	317	319
27	1	1	0	1	1			320	318	316	314	312	266	264	262	260	258
28	1	1	1	0	0			256	254	252	250	248	202	200	198	196	194
29	1	1	1	0	1			192	190	188	186	184	138	136	134	132	130
30	1	1	1	1	0			128	126	124	122	120	74	72	70	68	66
31	1	1	1	1	1			64	62	60	58	56	10	8	6	4	2

TABLE II. Binary Location/Address Correspondence

Because the parity data pattern is not symmetrical, it can be used for detecting decoder problems. Also, this pattern is easy to generate and control. For example, if one bit of the row decoder is not functioning, only half of the 32 rows can be addressed. With a symmetrical data pattern, this could go undetected. Data would appear to be entering and leaving the memory at all 1024 locations, but actually may only be happening in 512 locations. The parity pattern identifies data as wrong if it comes from the wrong location. The error is detected by reading the memory and comparing the data to the input data pattern.

For example, using the data pattern shown in Table III and attempting to write into Row 00001 and Column 00101 means a 1 should be written into this location because the addresses are of different parity. If the least significant bit in the column decoder is inoperable and remains at a logic 0, the address accessed would actually be Row 00001 and Column 00100. The 1 would be written into this

	TESTER ROW ADDRESS	PARITY	TESTER COL. ADDRESS	PARITY	DATA EN-TERED
Row 0	00000	0	00000	0	0
	00000	0	00001	1	1
	00000	0	00010	1	1
	00000	0	00011	0	0
	00000	0	00100	1	1
	00000	0	00101	0	0
	00000	0	00110	0	0
	00000	0	00111	1	1
	00000	0	01000	1	1
Row 1	00001	1	00000	0	1
	00001	1	00001	0	1
	00001	1	00010	1	0
	00001	1	00011	0	1
	00001	1	00100	1	0
	00001	1	00101	0	1
	00001	1	00110	0	1
	00001	1	00111	1	0
	00001	1	01000	1	0

Note that changing the row address bit by one changes the data pattern entered.

TABLE III. Parity Data Pattern for Bit/Decoder Test

location, which should have received a logic 0. Read-out and comparison to the correct input data pattern detects this error. Any decoder bit in error thus has the effect of changing the address accessed by one bit and always causes erroneous data to be written into the accessed location.

This test is done twice, using complemented data on the second test, so that both a 1 and a 0 are written into every cell and read out of every cell. If a cell fails in any of the four functions, it will be detected in this test. However, shorts between columns or rows can go undetected, so separate checks must be made to check for row-to-row or column-to-column shorts.

Column Shorts

Writing alternate columns of 0 and 1 detects possible column-to-column shorts. Writing can not be performed during this test and it is necessary to prevent writing while the chip is disabled. For the full address sequence of 1024 addresses, a complementary $\overline{\text{V-Bar}}$ pattern is applied with the Write enabled and the chip disabled. Then the chip is enabled and the data is read and compared with the Vertical Bar pat-

TEST	SEQUENCE		DATA INPUT	COMPARISON
	OPERATION	CE		
ACCESS TIME *	WRITE	E	$\overline{\text{V – Bar}}$	
	WRITE	E	V – Bar	
	DELAY	D	0	
	READ	E		$\overline{\text{V – Bar}}$

***This test is repeated with complemented data**

TABLE IV. ACCESS TIME TESTING

tern. If any errors are detected, they are the result of column-to-column shorts or failure of the chip disable.

Row Shorts

Row shorts are detected by a similar test procedure, with alternate rows of 1 and 0 applied. So that read does not occur during chip disable, the chip is disabled, the read/write input is held HIGH (Read), and a read operation is performed, comparing output to input. The output should be 0 when the input is 1. This detects the read disable as well as input-to-output shorts. The outputs are then read with the chip enabled, and the outputs comparing to the Horizontal Bar pattern. Any error detected indicates a row short.

A maximum power state occurs when all inputs (Data, Read/Write, Chip Enable, Addresses) are at a logic 1 during row short testing, with the row being addressed containing a logic 1 in all cells.

Disturb Testing

Data can be disturbed or lost if the memory node capacitance is discharged, and this can be the result of adjacent write operations. This test checks for this possibility by writing a row of 1 and then writing a row of 0 in the adjacent row. After constantly refreshing the row of 0 for a period equal to maximum refresh delay, the original row of 1 is read to determine if any 1 has turned to a logic 0. This test is applied to all rows, and when Row 31 is reached, Row 30 is used for continuously wiring a row of 0.

ACCESS TIME TESTING

The source of worst case access times is the occurance of maximum delays in both the decoders and the matrix. Decoder delay depends on the number of address bits which change from one address to another. Matrix delay depends on the data being read, the previous operation, the location of the memory cell, and when a 1 is to be read, the elapsed time since the last refresh or write operation. These delays are also affected by temperature and supply voltage variations.

The address sequence shown in Table II provides worst case decoder delays. By using a vertical bar pattern, it also provides worst case matrix delays.

Table IV illustrates that this test uses several steps. The V-Bar pattern is first written into the matrix, then the $\overline{\text{V-Bar}}$ pattern is written. Because of

refresh during write, this creates maximum transitions on the column sense lines. Then the chip is disabled and the R/W input held HIGH (Read), for a refresh delay. During this period, addresses are continually cycled to generate maximum internal noise. After this delay, the data is sequentially read out using the same address sequence as for the write operation, and then compared to the last input. The cycle is then repeated using complemented data.

Several objectives are accomplished by this test. The ability of the matrix to maintain logic levels during refresh is checked. The pattern and sequence used assure worst cast access time. Charge leakage, which can be detrimental to access time, is also checked by reading a logic 1 in a cell after the maximum refresh delay. The repeat of the cycle with complemented data checks each cell for its ability to see both a logic 0 and logic 1, and also provides a worst cast test of write capability during a maximum write cycle rate.

REFRESH TESTING

Temperature has an effect on various testing activities, but this is particularly true of refresh testing, because attempts at extrapolation from room temperatures values generally yields inadequate results. Refresh testing should utilize worst case data sheet values at a test temperature of 70°C to obtain reliable results.

AMERICAN MICROSYSTEMS, INC.

APPLICATION NOTE
AP75-9
MARCH 1975

Designing with 1103 Memories

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The popularity of 1103 type memory devices has steadily increased as they have become readily available in large volume, at prices which make them competitive or even less expensive than core in computer memory systems. The information in this application note relates to parts made by AMI, as well as most other manufacturers who offer 1103 type devices. There are units available with worst-case access times ranging from 120 ns to as much as 1 μs, so it is wise to become familiar with a particular device's specifications.

Since the original 1103 memories became generally available, considerable experience has been gained in the testing of these devices and their application in memory systems. The information presented here is intended for the memory system designer and for the incoming inspection group.

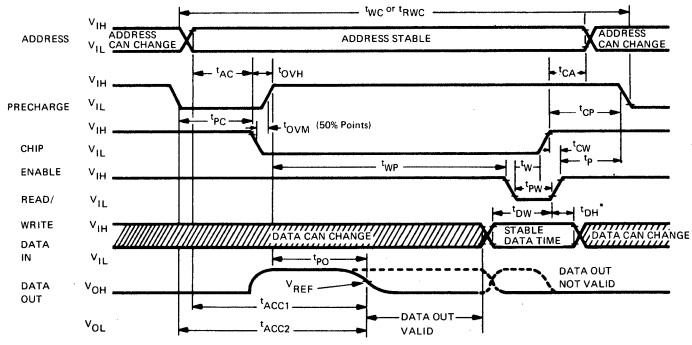
TIMING

When working with an 1103 type device, it is advisable to become familiar with the basic signal flow through the device for both a Read and a Write operation. Refer to the device schematic in Figure 1 and the timing waveforms in Figure 2.

Typical Read Cycle

In a normal Read cycle, the first thing that happens is a negative transition of the Precharge signal (PREC). As a result, all Data In and Data Out lines are precharged to the V_{DD} voltage (ON). Addresses can change prior to this precharge operation, but they must have changed and also settled early enough to satisfy the minimum access time interval (t_{AC}). Precharge provides the clock signal for two address func-

Figure 1. Timing Diagram of Write Cycle or Read/Write Cycle



* t_{DW} and t_{DH} are referenced to the rising edge of Chip Enable or Read/Write, whichever occurs first.

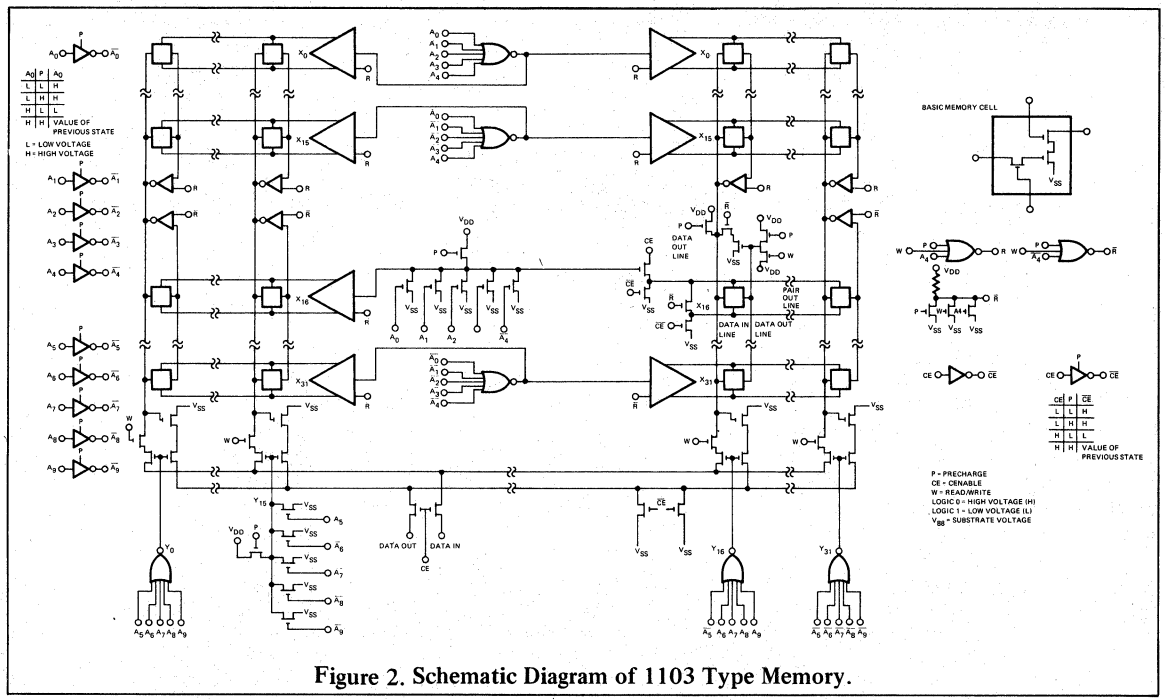


Figure 2. Schematic Diagram of 1103 Type Memory.

tions–one for the dynamic inversion of the address inverters and one for the dynamic decoding of the selected address decoders (both X and Y in the diagram).

The second step in a Read Cycle is the negative transition of the Chip Enable signal (CE). This turns on the output circuitry and allows current to flow, since the Data In line has already been precharged to the V_{DD} or "ON" voltage. The CE signal also enables the output transistors of all cells in the row selected by the X decoder. Depending on the information stored in each cell, its Data Out line is either discharged to V_{SS} or left at V_{DD}. This conditional discharge occurs during t_{OV}.

At the end of t_{OV}, the Precharge signal returns to the V_{SS} level turning on both the refresh signal (R) and the input transistors of all cells in the selected row. When R (or R, depending on the state of A_4) is turned on (changes from V_{SS} to V_{DD}), a conditional discharge of the Data In lines to V_{SS} occurs, based on the state of each Data Out line. When the input transistors in the selected row turn on, a refresh voltage is applied to each cell.

As the Data In line conditionally discharges to V_{SS} or "zero", output current of the selected column also falls from its previous level to "zero", The time required from the 90% point of the second Precharge transition to the point when the output current falls below a specified "zero" level is called t_{PO}. Total access time for the device (t_{ACC}) is determined by the combination of these various time intervals and is derived as follows:

$$t_{ACC} = t_{PC} + \tfrac{1}{2}t_F + t_{OV} + \tfrac{1}{2}t_R + t_{PO}$$

where T_F = CE negative transition time

t_R = Precharge positive transition time

Typical Write Cycle

A normal Write cycle always starts with the typical Read cycle described above. This is necessary for three reasons. First, the Y decoder must select the proper Data In line in order to write into a cell. Second, the input transistor of the cell must be on, accomplished by CE. Third, the CE signal at the same time also turns on all input transistors of all cells in the selected row, requiring that the proper information be present on each individual Data In line. The only assurance that these three conditions have been met is to start each Write cycle with a Read cycle.

Following the time interval (t_{PW}), data is written into the addressed cell by enabling the Write Enable input with a V_{DD} signal, while the data signal is applied to the Data In terminal. Under these conditions, the Data In connection offers a direct path to the addressed cell. Upon the transition of the CE signal to V_{SS}, all cells in the array are again isolated.

Minimum Overlap Time

There is a period of time when both the Precharge and Chip Enable lines are at the V_{DD} level; this is known as overlap time (t_{OV}). An 1103 type memory can enter a failure mode if minimum overlap time requirements are not met. What actually happens in such a failure mode is that the output signals tend to degrade from "ones" (current present) to "zeros" (current absent).

Early in a Read cycle, Data Out lines are precharged to V_{DD}. For a good solid "one" to appear on the Data Out line, the addressed cell must discharge the line to V_{SS} during the overlap time (t_{OV}). When t_{OV} is too short, the Data Out line remains partially on. This tends to cause the Data In line to discharge to V_{SS} through the refresh transistor in the sense amplifier. The Data In line should, however, remain at a solid V_{DD} potential. If it does not, it results in a weak current flow at Data Out, or a weak "one" level. Specifications for minimum overlap times in 1103 type devices consider this chain of events and guard against the occurrence of the condition.

Maximum Overlap Time

The reason for specifying a maximum overlap time (t_{OV} Max) is not necessarily as obvious as the need for t_{OV} Min. However, if the maximum overlap time is exceeded, the "zero" levels at Data Out elongate into "one" levels. The reason for this is that the "zero" levels stored in the cells are typically not perfect. These imperfect "zero" levels are generally the result of distributed stray capactiances throughout the device.

A perfect "zero" level is the actual V_{SS} voltage. A safety margin equal to one MOS threshold voltage (V_T) exists for each cell. If, however, the stored voltage at an addressed cell is more negative than $V_{SS} - V_T$, the cell's output transistor is partially on, instead of completely off. Consequently, the Data Out line discharges toward V_{SS} through this partially on transistor. Just how much the Data Out line discharges is a function of the conductivity of the output transistor and the duration of t_{OV}. If a long t_{OV} time is used, it is possible for the Data Out line to leak sufficient voltage for a "zero" with a long time constant (elongated) or even a "one" to appear at the Data Out terminal. This is because without a good V_{DD} level on the Data Out line, the Data In line cannot discharge quickly to V_{SS}.

t_{CW} Timing Restrictions

There is another important aspect of timing with most 1103 type devices. This is a parameter known as t_{CW} and is normally specified on data sheets as t_{CW} Max $\leqslant 0$ ns. The implication of this specification is that during a Write cycle, the positive-going edge of the CE signals must never occur prior to the positive-going edge of the WE signal. If it does, errors can occur in stored data and the refresh capability of the device can be adversely affected. If WE straddles the positive-going edge of CE, "ones" at the Data Out terminals can change to "zeros".

This type of failure is pattern dependent. That is, a problem can exist only if a particular sequence of events occurs in a particular order. Refer to the partial array schematic shown in Figure 2. During the first half of a Write cycle, the Data Out line for the column with a cell storing a "one" or V_{DD} discharges

to V_{SS} through that cell. With a WE pulse present the Data In line discharges to V_{SS}. This turns off the refresh amplifier path for the Data In line. This is the point at which any cell in the column storing a "one" faces a potential problem. The only separation between the stored "one" (V_{DD}) and V_{SS} on the Data In line is the input transistor. The voltage on the gate of this input transistor is also V_{SS} and it is only held off by the threshold voltage (V_T), typically 2.0 V. If the CE pulse makes a positive transition at this time, some of the positive voltage will be coupled from the gate of the CE control transistor to the Data In line. At this point in time, the Data In line is floating. When WE makes a positive transition, a relatively large positive voltage is coupled from the gate of the WE transistor to the floating Data In line. Such a "charge pumping" effect raises the voltage of the Data Input line above $V_{SS} + V_T$, turning on the input transistors of the cells. Turning these input transistors on causes the "one" levels to leak away.

VOLTAGE CONSIDERATIONS

Input Voltage HIGH

Transistor threshold voltages in MOS devices are referenced to the V_{SS} power supply. Typical voltage limit specifications for both clock and data input signals to an MOS array are based on and governed by the threshold voltage. With P-channel Si-gate devices such as the 1103, the threshold voltage is approximately 2.0 V. However, this threshold voltage increases with the application of positive substrate bias.

To be effective, a Clock or Data In line positive transition must reach and maintain a V_{IH} level at least as positive as $V_{SS} - V_T$. If not, the associated input transistors are not completely off. In order to provide some tolerance, most data sheet specifications list the minimum allowable limit for V_{IH} at 1.0 V more negative than V_{SS}.

Maximum V_{IH} limits are specified for reasons which are just a little more subtle. Typically, the V_{IH} Max limit is specified at $V_{SS} + 1.0$ V, but some 1103 designs have problems with this limit.

One reason for the V_{IH} Max limit is based on Data In circuit limitations imposed when a "zero" (or V_{SS}) is written into a cell. In a column with at least one cell storing a "one" (or V_{DD}), the storage nodes of the "one" cells are isolated from the Data In line only by input transistors. These input transistor gates have a V_{SS} potential through the $\overline{CE}$ transistors in the row decode circuits. If a "zero" is written into one of the cells in such a column, the positive voltage applied to the Data In terminal appears on the Data In line. This is a potentially dangerous situation for all cells in the column storing a "one". (V_{DD} is stored in the cell, V_{SS} is right outside on the Data In line. Also, V_{SS} is on the gate of the input transistor.) If the Data In voltage level is raised one threshold voltage level above V_{SS}, the input transistor is turned partially on and the charge flows off the storage node. Therefore, an input voltage HIGH which exceeds $V_{SS} + V_T$ simply forward biases the input transistors of all cells in that column. This causes the "ones" to leak toward "zeros", resulting in either a complete loss of the "ones" or a decrease in refresh capability.

Another reason behind the V_{IH} Max limit is that if the input voltage becomes more positive than V_{BB}, it forward biases the p-n junctions. The minority carriers which appear in the substrate quickly destroy "ones" stored in nearby cells, by drastically increasing their leakage current.

REFRESH CAPABILITY

As discussed earlier, a "one" (V_{DD} potential) in a storage cell is the unstable condition of 1103-type memories. Because a portion of the storage node is a p-type diffusion, inherent junction leakage tends to discharge the node to the substrate potential, V_{BB}. In order to accomplish a successful refresh cycle, the storage node must maintain sufficiently high voltage level over a specified period of leakage time, generally listed as 2.0 ms. The refresh capability of most 1103 devices determined by leakage alone at 70°C usually exceeds 40 ms. However, if electrical noise is present, the refresh capability can be reduced to several milliseconds. This noise has two possible origins; it can be externally applied through the power supplies, or it can originate within the chip itself.

Externally Applied Noise

In a situation with a "zero" having been read out of a cell, the Data In line is left floating at V_{SS}. At this point, all cells in this column with stored "ones" are susceptible to noise on both the V_{SS} and V_{BB} power supplies. The danger here is that the V_{DD} potential in these cells is only isolated from the V_{SS} potential, so the only voltage margin keeping these transistors in the off condition is the V_T, approximately 2.0 V. If a negative noise spike on V_{SS} occurs that is greater than V_T, these transistors turn on and charge is lost from their cells.

On the other hand, if a positive noise spike occurs on V_{BB}, it is capacitively coupled to the floating Data In line. If this noise spike exceeds V_T, the cell input transistors are turned on momentarily, again losing stored charge. The magnitudes of simultaneous positive and negative noise spikes is additive. Thus, the algebraic sum of the two spikes need only to exceed V_T for the problem to exist. The amount of charge lost in such noise spike situations is a function of the amplitude and duration of the noise.

Internally Generated Noise

A positive noise spike on a Data In line can cause loss of data and can be generated in several areas. One such source, capacitive coupling from the substrate (V_{BB}), was just discussed. Another source of positive noise is the R or $\overline{R}$ transistor in the refresh amplifier. A positive voltage transition on the gate of one of these transistors will be coupled to the Data In line. Because the A_4 and $\overline{A}_4$ addresses participate in deriving the R and $\overline{R}$ signals, toggling of the A_4 address causes a similar toggling of the refresh transistors. Thus, A_4 address changes are a positive noise source in the 1103.

A similar source of noise coupling is the WE transistor at the end of each Data In line. This is a large transistor, which compounds the problem. This problem was described in the section on t_{CW} timing restrictions. Many 1103 specifications neatly sidestep this problem area simply by requiring the positive edge of CE to occur last in a cycle ($t_{CW} \leqslant 0$). The AMI solution to the problem was a design change, which grounds Data In lines to V_{SS} at the end of each cycle. In this manner, any excess voltage is drained away.

CONCLUSION

A system designer can be quite comfortable when working with 1103 memory devices, and completely successful too, by considering a few important factors.

- Familiarity with basic signal flow for both Read and Write cycles.
- Awareness of the significance of various timing requirements.
- Consideration of the impact of power supply noise, refresh capability, and the adverse effects of both internally and externally generated noise.
- How the above factors can cause loss of data, erroneous data, or decreased refresh capability.
- The AMI 1103 device is far less susceptible to these problems than all the others.

By working closely with users of 1103 memory devices, AMI has gained an intimate knowledge of problems associated with utilizing 1103s in memory system manufacturing. Based on this experience and on extensive studies, AMI is able to ship an improved 1103 device, which greatly eases system application problems. The improvements can be translated directly into lower manufacturing costs and higher confidence in using these devices.

Improvements in AMI's 1103 have been accomplished by fine tuning of the layout and of circuit details to overcome the sensitivities described in this application note. The layout modifications have reduced stray capacitive coupling and minimized their effect on device operating margins, and resulted in a device which exhibits wider operating margins and less pattern sensitivity.

AMERICAN MICROSYSTEMS, INC.

APPLICATION NOTE
AP75-10
MARCH 1975

MOS Circuit for Electronic Organs

Ridge Cotton

INTRODUCTION

Music has always been a reflection of culture, and strangely enough, a rather accurate indication of the technological sophistication of a group, or period. Most of the earliest music depended almost entirely on rhythm, and it is not a coincidence that "primitive" music used simple rhythm instruments. These instruments were the only ones available.

With time, and accompanying sophistication, techniques for producing string, woodwind, and brass musical instruments developed and also with time, have been improved. It is only natural that electronic methods for the production of music would appear. The electronic organ is probably one of the most outstanding examples of electronically produced music, and the development of the electronic organ mirrors the developments that have occurred in electrical technology.

Early vacuum tube organs were replaced by solid state organs as transistors became available. Now, integrated circuits, specifically, MOS/LSI circuits, are a dominant factor in electronic music. One reason is the ability of MOS technology to produce circuits for accurate tone generation, eliminating the need for repeated tuning – and circuits for rhythm patterns, enhancing the sound of the organ by simulating drums and other basic percussion instruments.

At the present time, there are as many different approaches to the design of an electronic organ as there are organ manufacturers. However, there are certain elements basic to almost any electronic organ system.

TONE GENERATION

Musical tones occur in groups of twelve, called octaves. Since the frequency of any tone in an octave is exactly half the frequency of the corresponding tone in the adjacent, higher octave, typical modern electronic organs first generate the 12 frequencies in the top octave. The remaining tones are obtained easily with binary dividers. For example, an organ producing 96 tones requires the 12 top octave frequencies and 84 binary dividers. The block diagram of a typical electronic organ in Figure 1 exhibits this approach.

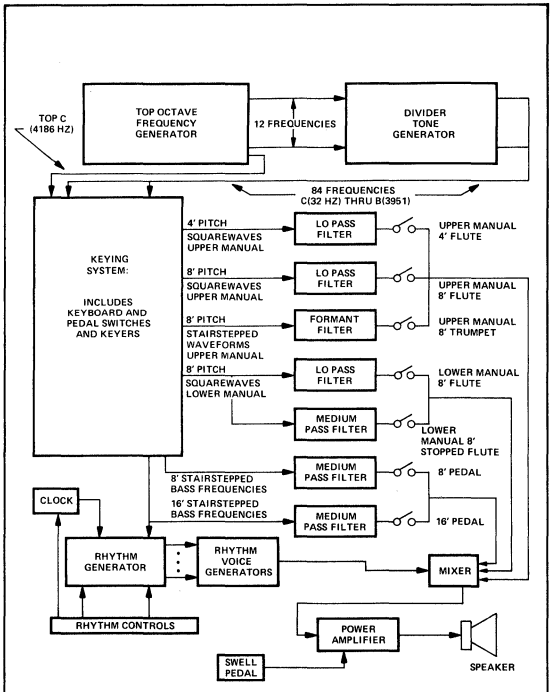


FIGURE 1. TYPICAL ORGAN BLOCK DIAGRAM

KEYING

Once the tones have been generated, some form of keying is required to switch the appropriate tones to the filters after the musician has selected the tone at the manuals or pedals. One of two basic keying approaches, ac or dc, is generally used.

FILTERING

Filters are used to shape the tone waveforms to simulate the various voices of the organ – flute, trumpet, etc. The signals are then mixed, amplified, and routed to the organ speaker. Volume is controlled by a swell pedal which attenuates the signals entering the amplifier.

RHYTHM

In addition to these areas electronic rhythm generators are becoming increasingly popular. Although not essential to an electronic organ, they now appear in varying degrees of complexity in most electronic organs being produced. Rhythm generators enhance the music by creating the illusion of a drum, and also help the organist maintain tempo.

TOP OCTAVE GENERATOR

Because all musical frequencies are exactly half of corresponding frequencies in the next highest octave, it is beneficial to generate the 12 frequencies of the highest, or top, octave. Generation of the top 12 frequencies in an electronic organ can be accomplished several different ways. The most obvious method uses 12 independent oscillators. The major disadvantage of this approach is high initial labor cost for tuning. In addition, the oscillators can change frequency with time, requiring further organ tuning at varying intervals. The AMI top octave generator (S2555 and S2556) eliminates both of these difficulties by dividing a single master frequency by 12 parallel divider chains; their outputs are the 12 top octave frequencies Figure 2. This approach generates the top octave with a high degree of accuracy (±1.1 cent error on all frequencies). In addition, an extra C note is provided by the S2555 generator. The advantage of this extra note will become obvious during discussion of tone dividers.

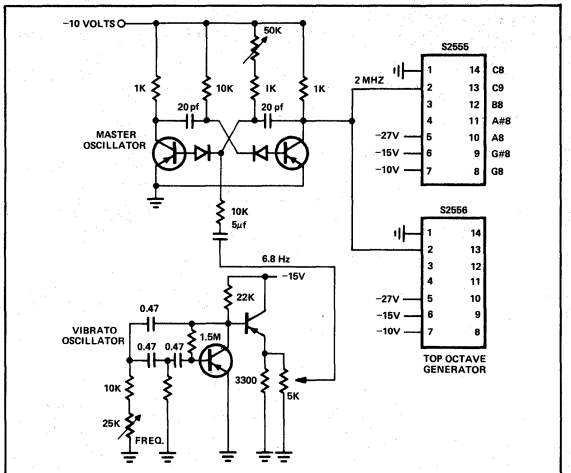


FIGURE 2. TOP OCTAVE GENERATOR (S2555/6) WITH MASTER OSCILLATOR AND VIBRATO GENERATOR

DIVIDER TONE GENERATOR

After the top octave frequencies have been generated, the remaining octave tones are obtained with binary dividers. Two AMI MOS divider circuits are available for this function; the S2470 with six dividers per package, and the S2193 with seven dividers per package.

A typical organ, Figure 1, requires the generation of seven octaves, or 84 frequencies, plus an extra C frequency. This is because most organs need a low C pedal and terminate the top octave with the highest C, requiring the generation of one additional tone beyond eight octaves. The organ shown in Figure 1 could use either 14 six-stage dividers (S2470) or 12 seven-stage dividers (S2193) with the extra C tone being provided by the S2555 top octave generator. It is also feasible to use the 12 top octave generator frequencies in place of the 12 highest frequency divider outputs. In this case, the organ could be built with only 12 six-stage dividers.

Another typical divider application is shown later in Figure 9. This three-octave "toy" organ uses S2193 dividers. It is relatively easy to build, requiring only a low-current (<100 mA) power supply, a power amplifier, and a speaker.

KEYING

With ac keying, Figure 3, frequencies from the tone generator pass directly through the keyboard switches to the bus outputs. As a result, annoying "key clicks" occur when the key switch is closed because the tone signal is applied instantly to the ac bus. Also, with ac keying, desirable "sustain" of musical notes cannot be obtained because the tone signal is removed instantly once the key switch is opened. In other words, musical notes "click" on when selected, and cannot linger unless the organist holds a finger or a foot on the selected key or pedal.

However, ac keying is often desirable because of lower costs. If the organ is a simpler, basic musical instrument, ac keying is tolerable from both cost and aesthetic viewpoints. As the organ develops sophistication, ac keying loses its advantage. Consider, for example, the organ in Figure 3. This organ requires more pitches, or "footages", because the upper manual supplies both 8′ and 4′ pitches. With ac keying, another set of contacts is required for each additional footage. if additional 16′, 2′, and 1′ pitch outputs were also desired, the total number of contacts per key would reach five. Obviously, the economic advantages of ac keying decrease under these circumstances.

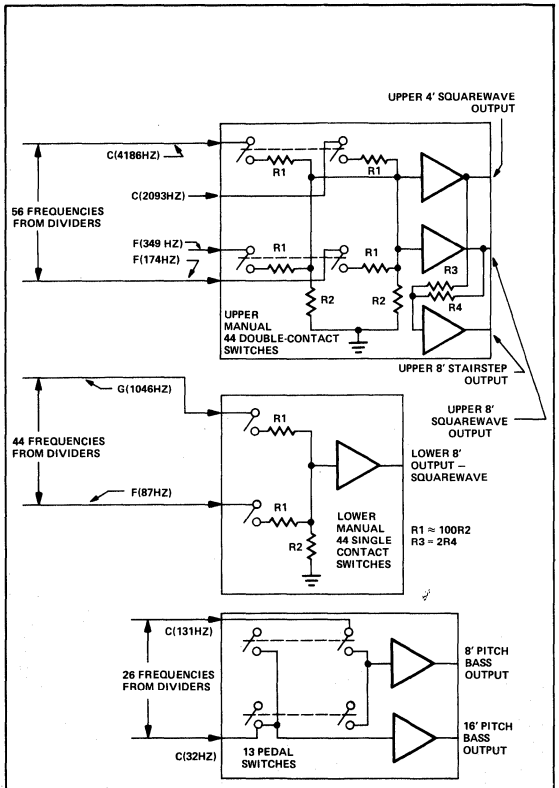


FIGURE 3. AC KEYING SYSTEM

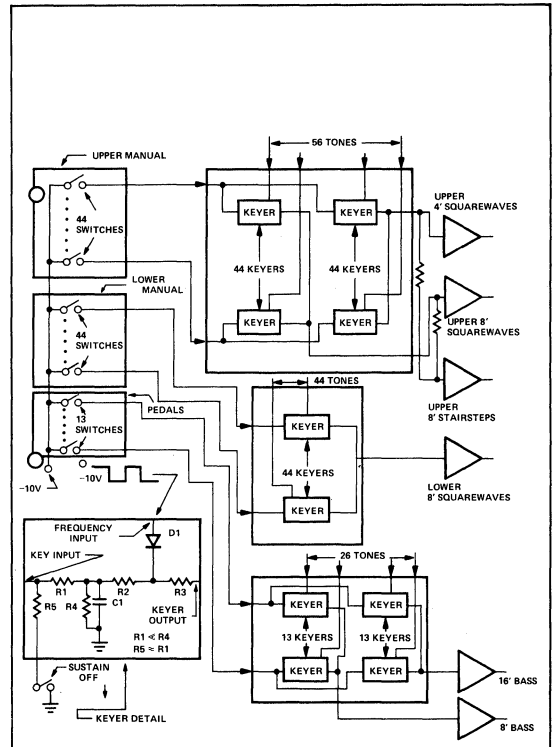


FIGURE 4. DC KEYING SYSTEM

With dc keying, a single contact key switch can control any number of output pitches. Also, "key click" is eliminated, and the desirable "sustain" feature is possible. Figure 4 shows a dc keying system. If you check the keyer detail exploded view, you will note that the appropriate frequency is applied constantly to diode D1, normally back-biased. When the key contact is closed, a negative potential is applied to the key input, causing C1 to charge up relatively fast. This forward biases D1 and applies the signal to the bus. The charging time constant of C1 + R1 eliminates "key click", and when the key is released, C1 discharges through R4. This causes the ac signal to decay slowly, obtaining "sustain". If R5 is grounded, C1 discharges much faster, eliminating long sustain.

Many of the disadvantages of ac keying are more than adequately eliminated by dc keying. However, the addition of "footages" or pitches requires an additional set of diode keyers for each pitch when using dc keying, much the same as ac keying requires additional sets of contacts. But, with dc keying, there is an attractive alternative. As shown in Figure 5, a large number of dc keyers can be included on one MOS/IC chip, significantly reducing the number of components required for additional pitches. In addition, MOS dividers can be incorporated on the same keyer chip, eliminating the need for separate divider packages.

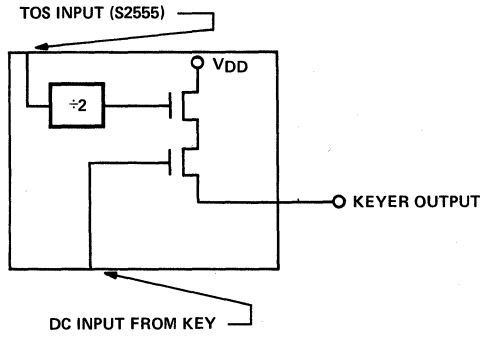


FIGURE 5. MOS KEYER

The result – an electronic organ keying system which works with only one top octave generator system, one key switch per key, and provides 16′, 8′, 4′, 2′, and 1′ pitch outputs. Thus, it may prove cost-effective in many electronic organ designs to replace standard IC divider packages and discrete diode keyer circuits with MOS/LSI systems. The high complexity of such MOS divider-keyer systems, combined with the widely varying musical requirements of the increasingly large number of organ models available, make the design of a standard MOS keyer product impractical. Such an attempt could result in a new "standard" product for each new organ model. The solution is to obtain a custom MOS/LSI circuit designed specifically for a particular organ model or line of models. AMI has the ability to design such custom MOS circuits to meet the exacting specifications required for musical keyer systems and the plant capacity to produce these circuits in high volume.

FILTERING

After an electronic organ generates the required frequencies and incorporates a keying system for selection of these tones, it must then offer a filtering mechanism to simulate the various classes of musical instrument sounds – strings, brass, flutes, etc. These are known as "voices" and are selected by activating switches called "stops". Three typical voice filters are illustrated in Figure 6. The component values are not listed because they depend on the specific voice to be simulated.

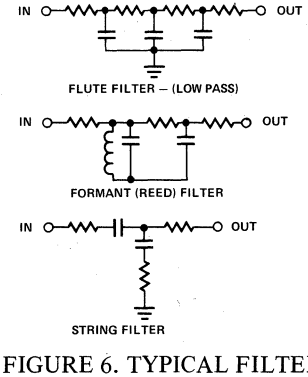


FIGURE 6. TYPICAL FILTERS

Of the many harmonics contained in the input waveforms, the filters must pass only those which are relevant to the voice desired, and certain waveforms are more suitable for filtering than others, depending on the voice to be imitated. A low pass flute filter, for example, attempts to pass only the fundamental sinewave. (Flutes actually possess more harmonics, but, generally, electronic organs tend to have flute voices made of sinewaves.) A squarewave is the best type of waveform input for this filter, because it contains no second harmonics, and the filter has only to suppress third harmonics and above to achieve the sine wave. The hollow sound produced by a square waveform, and its odd harmonics, make it useful for producing the clarinet voice, also.

Even though a squarewave is ideal for producing flute and clarinet voices, it is useless for reed voices, since these sounds require a full set of harmonics, even as well as odd. A square wave input to a reed filter produces an unpleasant, hollow musical result. Stairstepping approaches are often used to generate a waveform with all harmonics. Stairstepping is a process which adds octaves of square waves to approximate a sawtooth waveform. The sawtooth waveform approximation improves with the addition of more octaves. Referring back to Figures 3 and 4, a stairstepping method was used to add the 4′ and 8′ output busses to obtain an 8′ stairstep. An obvious advantage of this method is the very small number of components involved. The disadvantage lies in the musical result since the 8′ stairstepped output contains only two octaves, whereas three or even four would be musically superior. Further, the 4′ output is not stairstepped at all, and it would be impossible to obtain a stairstepped 4′ output without adding either an additional set of contacts in an ac keying system, or an additional set of diode keyers in a dc keying system.

There are, fortunately, other methods of obtaining stairstepped waveforms, and Figure 7 illustrates an approach which obtains these stairstepped waveforms at the tone generation stage, prior to the keyer stage. This method provides additional steps in the waveform and, hence improved sound quality. However, it may require additional dividers and a large resistor network.

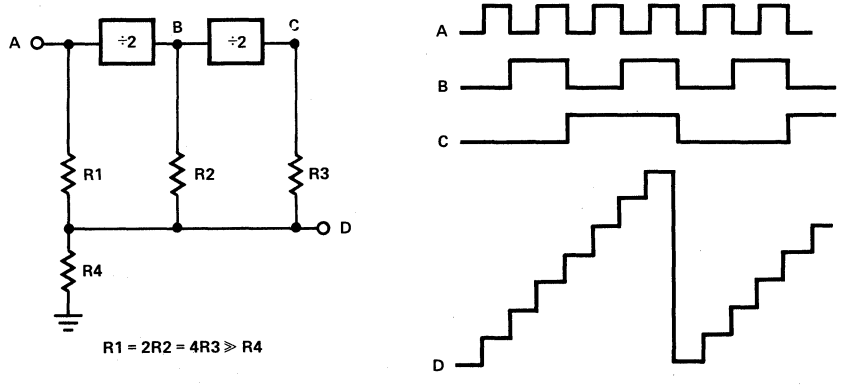


FIGURE 7. STAIRSTEPPING AT GENERATOR OUTPUT

RHYTHM

Rhythm generation adds to the music by simulating percussion instruments and by maintaining tempo for the organist. Relatively sophisticated rhythm systems have become practical in moderately priced organs because of the large storage capacity of a single MOS chip.

Basically, a rhythm system requires a rhythm generator device capable of producing several rhythm patterns for a given instrument and circuits which simulate the sounds of various rhythm instruments, see Figure 8. The production of rhythm patterns often requires a minimum sequence length of 32 bits. A sequence length of 64 bits provides almost all rhythm patterns desirable. Eight to ten outputs, each capable of producing a 32 to 64-bit sequence, can simulate most of the common rhythm patterns.

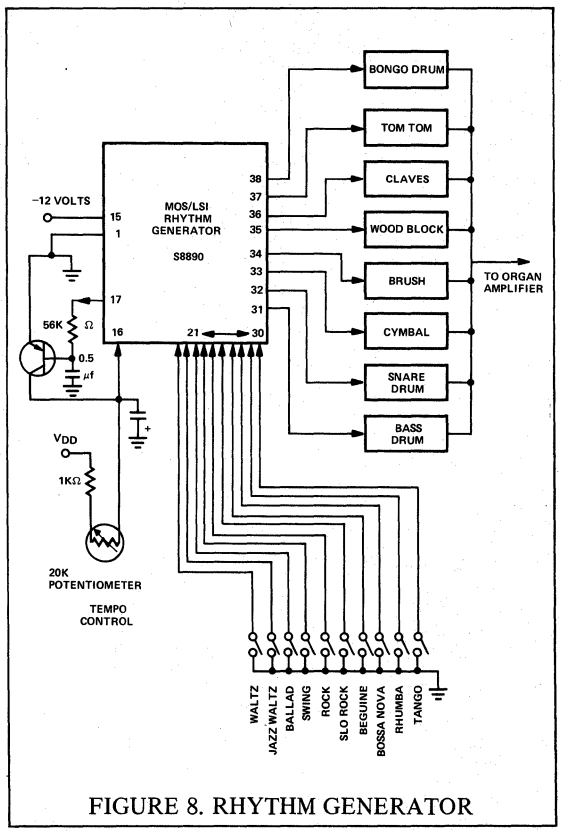


FIGURE 8. RHYTHM GENERATOR

Control terminals for altering the sequence at the outputs make it possible to program a read only memory in the generator, providing eight to ten rhythm patterns such as waltz, fox trot, tango, etc. If random access memory is used, other rhythm patterns could be selected from the organ keyboard. Detailed descriptions of rhythm generators are included on AMI rhythm generator data sheets for the S8890, S2566, and S2567. In addition, custom MOS/LSI rhythm generators can be developed to meet varying organ design requirements.

OTHER MUSICAL FEATURES

Many of the basic requirements of an electronic organ can be met by MOS/LSI circuits. Additionally, very complex musical systems can be built with standard read only and read/write MOS memories for complex synthesis and storage functions. For example, random access read/write memories (RAMs) can be used to store patterns of organ stop selections. Stop combinations could be made only once on the keyboard and stored in memory to be selected as desired by the organist. Memory circuits are also quite useful for storing musical chords, walking bass features, and other "complex" musical effects. Again, the system specifications for each application vary widely, often leading to a custom MOS/LSI circuit to accommodate a particular manufacturer's design.

CONCLUSION

Current electronic organs have gained much sophistication while remaining popularly priced, primarily due to developments in MOS/LSI circuits. Several AMI standard organ circuits provide the basic elements for an electronic organ. In addition, standard MOS/LSI memory circuits can be combined to provide quite sophisticated musical effects such as walking bass and chord production. Such effects have been impractical, if not impossible, to achieve in the past. When organ system designs require MOS circuits not available as standard products, AMI has the ability to design custom MOS circuits to meet a variety of specifications for electronic musical instruments.

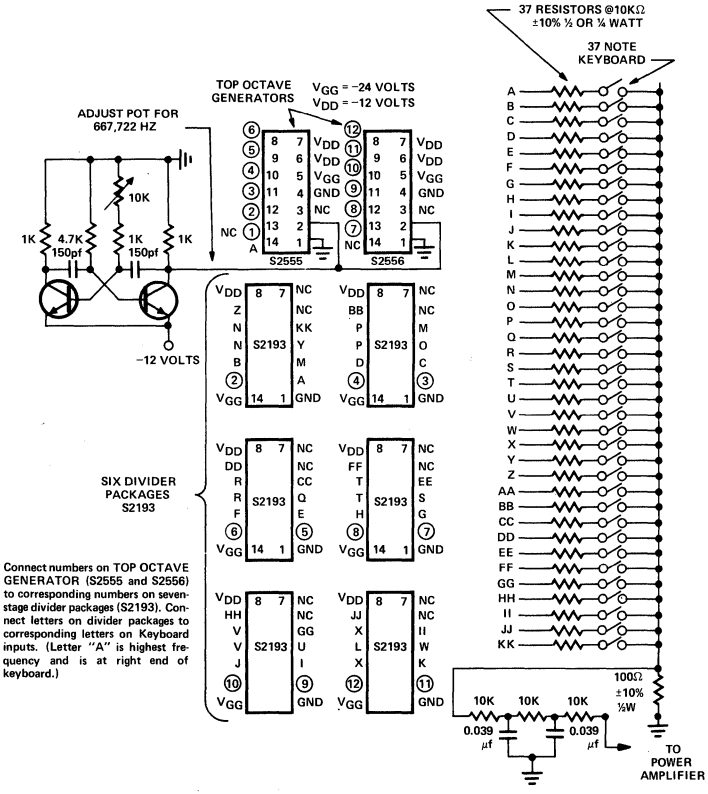


FIGURE 9. SCHEMATIC DIAGRAM FOR SINGLE-VOICE 37-NOTE KEYBOARD ELECTRONIC ORGAN

AMERICAN MICROSYSTEMS, INC.

APPLICATION NOTE
AP75-11
MARCH 1975

Testing Dynamic RAMs

Jim Dodson and Mike Mattson

INTRODUCTION

Successful testing of dynamic MOS RAMs requires knowledge of many factors which influence the performance of the memory. When dealing with dynamic devices, the slightest imperfection can affect the speed of the devices, so it becomes very important to adopt testing methods which can detect any such imperfections. On the other hand, these testing methods must lie within time constraints: too much time devoted to testing, runs head-on into the economic aspect. In the final analysis, economics is a primary consideration. This is true for both the manufacturer and the user.

There are several approaches to memory testing which have evolved based on time/cost considerations. One such approach is GALPAT, the well-known galloping pattern. This method requires time, based on the bit size of the memory, equivalent to $2n^2 + 2n$, where n = number of bits in the memory. For a 1024-bit memory, this is roughly 2×10^6 times the device cycle time. A 1024-bit memory with a 400 ns cycle time, for example, would require almost one full second for a single voltage test. A memory such as the 1103, which uses eight combinations of voltage and time for testing, requires almost 8 seconds of testing for only one test pattern.

If the memory being tested is pattern sensitive, more voltage/time combinations must be used in testing. It is conceivable to use as many as 12 combinations in a GALPAT test and this becomes quite costly.

Over the years AMI has learned much about dynamic RAM production and testing. The ability to produce a dynamic RAM with outstanding electrical performance and high reliability characteristics stems from a highly interactive combination of multiple factors, and testing is a predominant influence. These interactive factors are:

- Conservative Topological Design
- Production Process Control
- Thorough Test/Characterization
- Reliability Testing
- Effective Failure Analysis
- Accelerated Stress Testing

Rather than discuss testing in general terms, this note uses data accumulated for the AMI S1103 1024 x 1 silicon gate MOS dynamic RAM. Accelerated test data from a number of years is available for this part, and a cumulative summary of AMI test results is shown in Table I. It is evident from this data that the device is not only reproducible with good yield results, but also is highly stable with regard to performance.

Table 1. Cumulative Summary of Stress Test Data for the S1103 Dynamic RAM

TEST	JUNCTION TEMPERATURE Tj°C	NUMBER OF DEVICES	NUMBER OF UNIT HOURS	NUMBER OF FAILURES
Operating Life	140	706	1,913,000	9
Back Bias	125	1,131	1,547,000	8
Back Bias – 85°C/85% R. H.	85	721	1,267,000	6
Storage	150	588	1,556,000	0
Temperature Cycle	- 65 to + 150	461	69,200	1
Thermal Shock	- 65 to + 150	149	29,800	0
Thermal Intermittents	+ 25 to + 100	27,280	–	18

THE 1103 DYNAMIC READ/WRITE RAM

AMI S1103 devices are manufactured using a P-Channel low threshold silicon gate process developed by AMI. This process, combined with conservative topological design layout rules, produces a memory circuit with outstanding performance.

The S1103 RAM offers fast access and cycle times, internal decoding, and simple memory expansion. It is organized in 32 rows of 32 cells each, Figure 1. Five Address lines ($A_0 - A_4$) are provided for row selection. Signals on these address lines, once decoded, select a row of cells. The contents of the cells in the selected row are transferred to refresh amplifiers, and during the cycle, these data bits are rewritten into the selected row. Five additional address inputs ($A_5 - A_9$) are decoded into one refresh amplifier, to allow communication with the input and output lines. Three clocks are used: precharge, chip enable, and read/write.

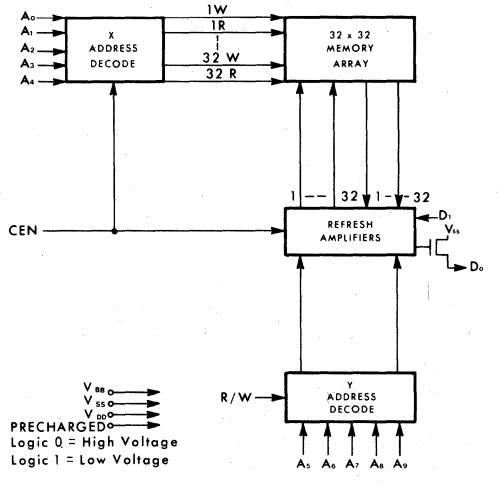


Figure 1. Block Diagram of the S1103 Dynamic RAM

TESTING THE 1103 DYNAMIC RAM

Testing procedures used at AMI for the 1103 RAM are designed to accomplish several objectives. First, the part must pass basic dc tests to prove that it performs well electrically. If it passes these tests, several levels of functional testing are used to further categorize the device. The first level functional tests are performed at approximately 3.2 MHz, and devices passing these tests meet the S1103X specifications. Because speed is the basis for the categorization of the S1103 device family, subsequent functional tests are performed at decreasing clock rate – first at 2.8 MHz, then at 2.5 MHz, and finally at 1.7 MHz. Devices which pass these functional tests are identified as S1103-1 at 2.8 MHz, S146 at 2.5 MHz, and S1103 at 1.7 MHz, Figure 2.

Parts which fail to pass the initial dc test are removed from the speed/functional test procedure and subjected to relaxed dc testing. If they pass the relaxed dc tests, they are functionally tested at the 1.7 MHz rate. All parts which fail to pass the 1.7 MHz functional test are rejected. The actual test procedures used are described below; all are performed under the same conditions, except for power supply differences and timing changes.

Wafer Sort

The first tests, performed on all devices, occur in the wafer stage. These tests are performed at room temperature and all failures are rejected prior to further processing. Tests performed include continuity, breakdown voltage, and function.

The continuity test is performed to check the contact between the probes on the probe card and pads on the chip Input breakdown voltage tests are performed with V_{BB} at 3V. Each input is checked for less than 10 μa leakage, when – 20V is applied and all other inputs are grounded.

A simple functional test is performed at the wafer stage, using a MARCH pattern, with the timing and voltage values listed in Table II. This test checks the ability of each cell to store a logic "one" or "zero". The MARCH pattern writes a test bit into every memory location. Then, the addresses are scanned from location 0 to 1023, the test bit is read at each

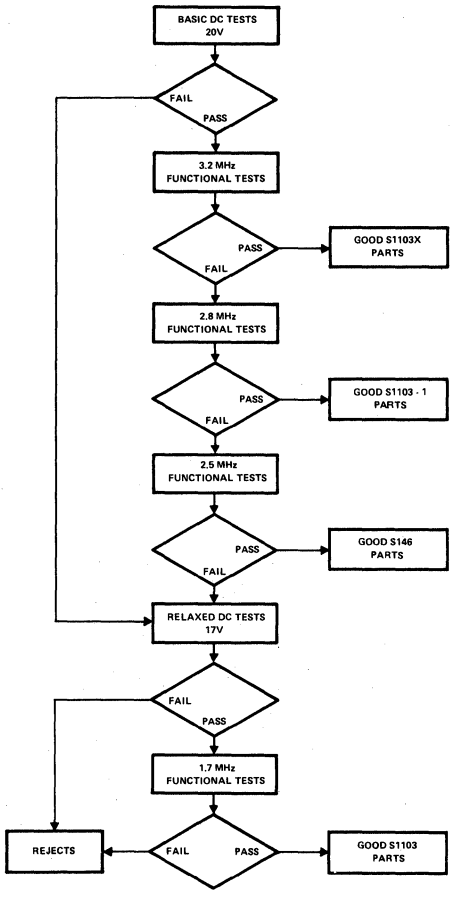


Figure 2. Qualification Test Sequence for the S1103 RAM

address, and the complement is written into the selected cell. Address scanning is then reversed, from cell 1023 to cell 0, and at each address the complement is read and the original test bit is written in again.

Final Test

Final test occurs after the tested wafer dice have been packaged. After assembly, the devices are subjected to a series of dc and functional tests at ambient and elevated temperature. The test includes a continuity test, dc and functional stress tests, and breakdown voltage and leakage tests on all inputs. I_{DD} power tests are also performed.

A continuity test is performed to check the contacts between the package and test head mechanism. The device is then subjected to high level dc voltages to identify weak locations. Breakdown voltage tests are made for all addresses, clocks and data input. Each input is checked for less than 10 μa leakage, when – 20V is applied and all other inputs are grounded. Also, four different power measurements are made under functional conditions (I_{DD1}, I_{DD2}, I_{DD3}, I_{DD4}), because with a dynamic circuit, power consumption varies.

All packaged devices which pass the continuity, dc stress, breakdown voltage/leakage, and supply power tests are subjected to functional testing. These functional tests use a variety of supply voltages, clock levels, and timing combinations, which include:

- HIGH clocks and inputs, HIGH V_{SS}
- HIGH clocks and inputs, LOW V_{SS}
- LOW clocks and inputs, HIGH V_{SS}
- LOW clocks and inputs, LOW V_{SS}

These four combinations are applied two times, first for minimum Precharge/Chip Enable overlap time (t_{OV}) and then for a maximum overlap time. All other timing values are held at minimum, Table II.

Several test patterns are used, including the MARCH pattern described above. Also, a CHECKERBOARD, COMPLEMENTARY ADDRESS, COLUMN BAR, and COLUMN DISTURB REFRESH patterns are used for each device. The complement of each pattern is also used. The CHECKERBOARD pattern is useful for checking the ability of each cell to hold a charge. The pattern writes a checkerboard data pattern into all 1024 locations in sequence from location 0 through location 1023, and then reads the data in the same order. The COMPLEMENTARY ADDRESS pattern also writes opposite data into alternate rows of memory, but does it "ping-pong" manner, writing first into location 0 and then into location 1023, then into location 1, then into location 1022, etc. Data is read in the same manner. See Figure 3.

Table II. S1103 Timing Characteristics

AC CHARACTERISTICS		S1103		S146		S1103-1		S1103X		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ, WRITE AND READ/WRITE CYCLE									
t_{REF}	Time between Refrésh Cycles		2		2		2		2	ms
t_{AC}	Address to Chip Enable Setup Time	115		65		30		30		ns
t_{CA}	Chip Enable to Address Hold Time	10		10		10		10		ns
t_{PC}	Precharge to Chip Enable Delay	125		70		60		35		ns
t_{OV}	Precharge and Chip Enable Overlap	45	95	25	65	25	50	13	35	ns
t_{OVH}	Precharge and Chip Enable Overlap		140		85		85		85	ns
t_{CP}	Chip Enable to Precharge Delay	85		50		40		40		ns
	READ CYCLE									
t_{RC}	Read Cycle (4, 5)	480		330		300		238		ns
t_{POV}	Precharge to end of Chip Enable	165	500	130	500	115	500	114	500	ns
t_{PO}	Precharge to Output Delay		120		100		75		65	ns
t_{ACC1}	Address to Output Access (4, 6)		300		205		150		120	ns
t_{ACC2}	Precharge to Output Access (4, 7)		310		210		180		125	ns
	WRITE OR READ/ WRITE CYCLE	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNITS
t_{WC}	Write Cycle (4, 8)	580		390		360		270		ns
t_{RWC}	Read/Write Cycle (4, 9)	580		390		360		270		ns
t_{PW}	Precharge to Write Delay	165	500	130	500	115	500	114	500	ns
t_{WP}	Write Pulse Width	50		40		40		20		ns
t_W	Write Setup Time	80		40		40		20		ns
t_{DW}	Data Setup Time (10)	105		40		40		25		ns
t_{DH}	Data Hold Time (11)	10		10		10		10		ns
t_{PO}	Precharge to Output Delay		120		100		75	60	65	ns
t_P	Time to Next Precharge	0		0		0		0		ns
t_{CW}	Chip Enable to Write		15		15		15		15	ns

V_{DD} = OV, $V_{BB} - V_{SS}$ = 3.4V, V_{SS} = 16V $\pm$ 5%, T_A = 0 - 70°C (S1103), 0 - 55°C (S146 and S1103-1)

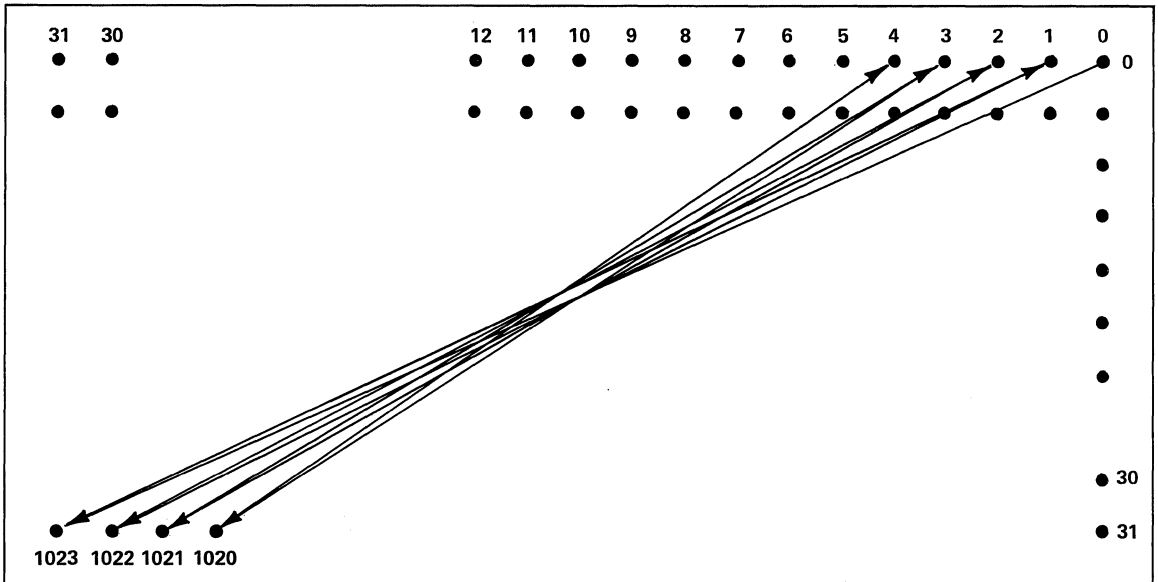


Figure 3. Representation of Complementary Addressing (Ping-Pong) Test

The COLUMN BAR test writes alternate data into adjacent columns in sequence from location 0 to location 1023 and reads the data in the same order. The COLUMN DISTURB REFRESH test is useful for checking refresh capability of the RAM. First "ones" are written into all cells of the selected column, then a "zero" is written into the first cell of that column for the refresh period, in this case, 2 ms. Then, a "one" is written into this first cell and all cells in the column are read for a "one" level. The procedure is repeated for all remaining 31 columns. Each test described is repeated with complemented logic levels to check every cell location for the ability to hold a level, in spite of adjacent disturbances, for the full specified refresh time.

RELIABILITY PROGRAMS

In the interest of reliability analysis, the performance range of 1103 devices as well as areas of potential failure are examined and checked by a variety of accelerated tests. These tests include the following areas.

- Operating Life
- Humidity
- High Temperature Storage
- Temperature Cycling
- Thermal Shock
- Solderability
- Thermal Intermittents

Operating Life

The operating life, or steady state life test is performed in accordance with MIL-STD-883, Method 1005. Test conditions used maximize stress conditions. For the S1103 device, functional burn in and back bias conditions are used with ambient temperature at 125°C. In an operating mode, the devices dissipate approximately 290 mW, with a junction

temperature approaching 140°C. Electrical performance of the devices is monitored at 0, 168, 500, and 1000 hours. Frequently, stress conditions are extended to 2000 hours. Extensive life testing has been performed over the past three years and Table III is a test summary for the S1103 device.

Table III. Life Test Data Summary for S1103 RAM

DATE	PACKAGE	TYPE OF BURN-IN	JUNCTION TEMPERATURE Tj°C	SAMPLE SIZE	NUMBER OF HOURS COMPLETED	NUMBER OF REJECTS DC	FUN
Dec 71	Cer	HTRB	125	30	2000	0	0
	Pl	HTRB	125	25	2000	0	0
Apr 72	Cer	HTRB	125	38	1000	0	0
May 72	Cer	Dynamic	140	38	2000	0	0
Aug 72	Cer	Dynamic	140	38	1000	1	0
Oct 72	Cer	Dynamic	140	25	4000	0	1
	Pl	Dynamic	140	100	4000	1	1
	Cer	Dynamic	140	25	4000	0	0
	Pl	Dynamic	140	75	4000	1	1
Nov 72	Cer	HTRB	125	25	3000	0	0
	Pl	HTRB	125	100	3000	0	1
	Cer	Dynamic	140	25	3000	0	0
	Pl	Dynamic	140	75	3000	0	0
	Cer	Dynamic	140	38	1000	0	0
Dec 72	Cer	HTRB	125	38	1000	0	0
Feb 73	Cer	HTRB	125	38	2000	0	0
April 73	Cer	Dynamic	140	92	1000	0	0
May 73	Cer	HTRB	125	38	1000	0	0
Oct 73	Cer	Dynamic	140	38	1000	0	0
Dec 73	Cer	Dynamic	140	39	1000	0	0
Jan 74	Cer	HTRB	125	162	1000	0	0
Jan 74	Cer	HTRB	125	73	2000	2	0
Feb 74	Cer	HTRB	125	114	1000	1	0
Mar 74	Cer	HTRB	125	250	1000	1	1
May 74	Cer	Dynamic	140	98	4000	2	1
July 74	Cer	HTRB	125	38	1000	0	0
July 74	Pl	HTRB	125	162	1000	1	1

In addition to S1103 device stress tests, extended life tests have been performed using a test vehicle, or "rel chip". This test vehicle includes a number of discrete devices for measuring individual device threshold, field threshold, and conduction factor, k'. In addition, the test vehicle also has a large p-n junction area, a large area gate oxide capacitor, a set of metal strips crossing deeply etched steps, continuity strings of polysilicon to P+, P+ to metal, and provisions for sheet resistance measurements. Table IV shows a life test data summary for the test vehicle.

Table IV. Test Vehicle Life Test Data Summary

DATE	PACKAGE	TYPE OF BURN-IN	JUNCTION TEMPERATURE Tj°C	SAMPLE	NUMBER OF HOURS COMPLETED	NUMBER REJECTS
Oct 71	Cer	Op-Life	125	10	1000	0
	Cer	Op-Life	125	15	1000	0
Nov 71	Cer	Op-Life	125	20	1000	0
Dec 71	Cer	Op-Life	125	56	2000	0
	Pl	Op-Life	125	75	2000	0
Feb 72	Cer	Op-Life	125	25	1000	0
May 72	Cer	Op-Life	125	20	1000	0
Aug 72	Cer	Op-Life	125	10	1000	1
Oct 72	Cer	Op-Life	125	18	4000	0
	Pl	Op-Life	125	45	4000	1
	Cer	Op-Life	125	18	4000	1
	Pl	Op-Life	125	45	4000	1
Nov 72	Cer	Op-Life	125	15	3000	1
	Pl	Op-Life	125	38	3000	0
	Cer	Op-Life	125	20	3000	0
	Pl	Op-Life	125	38	3000	1
Feb 73	Cer	Op-Life	125	20	1000	0
May 73	Cer	Op-Life	125	10	1000	0
Nov 73	Cer	Op-Life	125	12	1000	0
Jan 74	Cer	Op-Life	125	10	1000	0
May 74	Cer	Op-Life	125	10	1000	0

Humidity

Humidity tests include back bias in an 85°C, moisture resistance tests conducted in accordance with MIL-STD-883, Method 1004. Devices are also exposed to pressure at 125°C, at 100% relative humidity, with no bias. During three years of humidity tests, both dc and functional failures were almost non existent, and significantly, no evidence of moisture penetration in plastic packages was discovered. There was no occurrence of corrosion in either ceramic or plastic packages.

High Temperature Storage

Extensive test data has been gathered about temperature aging of both the S1103 devices and the test vehicle. The results have shown no deteriorating effects due to high temperature storage.

Temperature Cycling

Temperature cycling of parts is conducted according to MIL-STD-883, Method 1010, Condition C, for all S1103 types to evaluate bond and related failure modes. Thousands of device cycles over a three year period have resulted in only seven dc rejects. These tests included both ceramic and plastic packages.

Thermal Shock

Thermal shock data has been gathered according to MIL-STD-883, Method 1101, Condition C, for both 1103 devices and the test vehicle. The reject rate, again, has proven extremely low, often being zero for an entire year.

Solderability and Thermal Intermittent Tests

Periodic solderability tests are performed on S1103 devices, both in plastic and three layer ceramic packages. Plastic packages are subjected to thermal intermittent tests to monitor product quality. Cumulative test results on almost 28,000 devices has only shown 18 units showing opens, or only 0.07% defects as a result of bond lifts.

CONCLUSION

The abbreviated S1103 family testing results described here indicate the degree of reliability which has been achieved at AMI in the production of dynamic silicon gate RAMs. The combination of conservative topological design rules, several in-line process control inspections, thorough testing and characterization, regular reliability testing, and a strong failure analysis program results in a family of dynamic MOS RAMs exhibiting high reliability and outstanding performance. Detailed test descriptions results, and reliability figures, including failure analysis, are available from AMI for the S1103 family of memory devices, in the form of a fully documented engineering report.

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