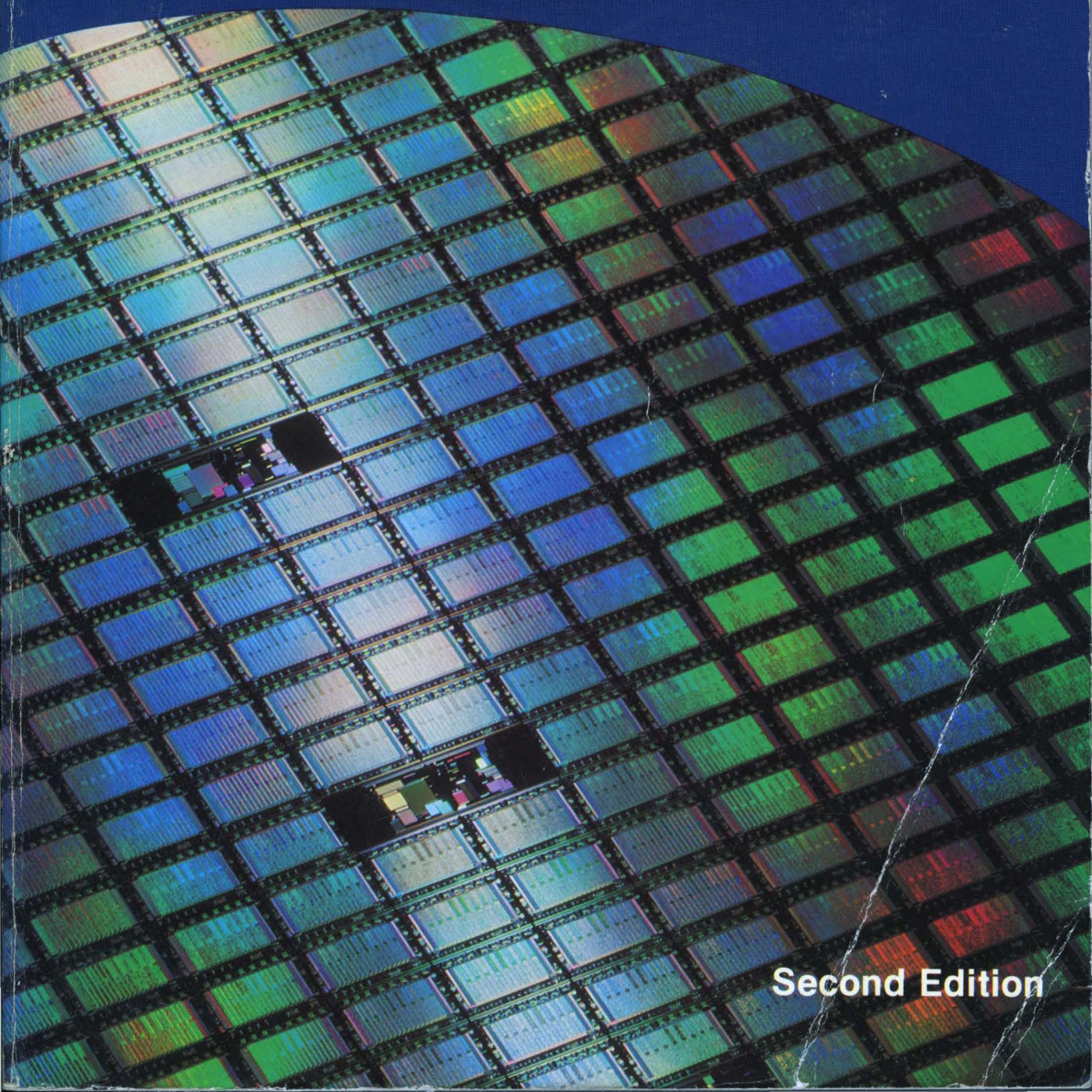
AMI

A Subsidiary of Gould Inc

1982 MOS Products Catalog



Second Edition

AMI

A Subsidiary
of Gould Inc.

1982
MOS Products Catalog

American Microsystems, Inc. (AMI) headquartered in Santa Clara, California is the semiconductor industry leader in the design and manufacture of custom MOS/VLSI (metal-oxide-silicon very-large-scale-integrated) circuits. It manufactures special circuits for the leading computer manufacturers, telecommunications companies, automobile manufacturers and consumer product companies worldwide. AMI is a wholly owned subsidiary of Gould, Inc.

Along with being the leading designer of custom VLSI, AMI is a major alternate source for the S6800 8-bit microprocessor family and the only alternate source for the S9900 16-bit family of microprocessors. The company provides the market with selected low power CMOS Static RAMs, and 8K, 16K, 32K, 64K and 128K ROMs for all JEDEC pinouts or as EPROM replacements.

The most experienced designer of systems-oriented MOS/VLSI communication circuits, AMI provides components for station equipment, PABX and Central Office Switching systems, data communications and advanced signal processing applications.

AMI is a leading innovator in combining digital and analog circuitry on a single silicon chip, and is a recognized leader in switched capacitor filter technology.

Processing technologies range from the mature PMOS metal gate, to silicon gate N-Channel to the advanced, small geometry, high performance silicon gate CMOS. Over 25 variations are available.

Headquartered in Santa Clara, California, AMI has design centers in Santa Clara; Pocatello, Idaho; and Swindon, England. Wafer fabricating plants are in Santa Clara and Pocatello, and assembly facilities are in Seoul, Korea and the Philippines. A joint venture company in Graz, Austria will include complete design and manufacturing facilities.

Field sales offices are located throughout the United States, in Europe and in the Far East. Their listing, plus those of domestic and international representatives and distributors appear on pages B.32 through B.35 of this publication.

AMI

Table of Contents

Indices

Numerical Index

Functional

Functional Index (Continued)

Communication Products

Cross Reference by Manufacturer

Manufacturer	Part Number	AMI Functional Equivalent Part
G.I.	SPR 128	3630
G.I.	ACF 7310,12,7410	3526
G.I.	ACF 7323C	3525
G.I.	ACF 7363C	3525
G.I.	ACF 7383C	3525
G.I.	AY5-9100	2560A
G.I.	AY5-9151	2560A
G.I.	AY5-9152	2560A
G.I.	AY5-9153	2560A
G.I.	AY5-9154	2560A
G.I.	AY5-9158	2560A
G.I.	AY5-9200	2562/2563
G.I.	AY3-9400	2559
G.I.	AY3-9401	2559
G.I.	AY3-9410	2559
G.I.	AY5-9800	3525
G.I.	AY3-9900	3501/3502
Hitachi	HD 44211	3507
Hitachi	HD 44231	3506
Intel	2364	3630
Intel	2910/2912	3501/2
Intel	2913	3507
Intel	2914	3507
Intersil	ICM 7206	2559
Mitel	MT 4320	3525
Mitel	ML 8204	2561A
Mitel	ML 8205	2561A
Mitel	MT 8865	3525
Mostek	MK 5087	2559
Mostek	MK 5089	25089
Mostek	MK 50981	2560A

Manufacturer	Part Number	AMI Functional Equivalent Part
Mostek	MK 50982	2560A
Mostek	MK 50991	2560A
Mostek	MK 50992	2560A
Mostek	MK 5116	3501/3502, 3507
Mostek	MK 5151	3501/3502, 3507
Mostek	MK 5156	3503/3504, 3506
Mostek	MK 5170	2562/2563
Mostek	MK 5175	25610
Mostek	MK 5387	2559
Mostek	MK 5389	25089
Motorola	MC 14400	3507
Motorola	MC 14401	3507
Motorola	MC 14402	3507
Motorola	MC 14406	3501/3502
Motorola	MC 14408	2560A
Motorola	MC 14409	2560A
National	MM 5393	2560A
National	MM 5395	2559
NEC	μPD 7720	2811
Nitron	NC 320	2560A
OKI	MSM 38128	3630
Phillips	TDA 1077	2559
RCA	CD 22859	2559
SSI	SSI 201	3525
Siliconix	DF 320	2560A
Siliconix	DF 321	2560A
Siliconix	DF 322	2560A
Siliconix	DF 341	3501/3502
Siliconix	DF 342	3501/3502
Supertex	CM 1310	3630

Communication Products

Cross Reference by Part Number

Part Number	Manufacturer	AMI Functional Equivalent Part
TDA 1077	Phillips	2559
SPR 128	G.I.	3630
CM 1310	Supertex	3630
MC 14400	Motorola	3507
MC 14401	Motorola	3507
MC 14402	Motorola	3507
MC 14406	Motorola	3501/3502
MC 14408	Motorola	2560A
MC 14409	Motorola	2560A
SSI 201	SSI	3525
CD 22859	RCA	2559
2364	Intel	3630
2910/2912	Intel	3501/2
2913	Intel	3507
2914	Intel	3507
DF 320	Siliconix	2560A
NC 320	Nitron	2560A
DF 321	Siliconix	2560A
DF 322	Siliconix	2560A
DF 328	Siliconix	2560A
DF 341	Siliconix	3501/3502
DF 342	Siliconix	3501/3502
MSM 38128	OKI	3630
MT 4320	Mitel	3525
HD 44211	Hitachi	3507
HD 44231	Hitachi	3506
MK 5087	Mostek	2559
MK 5089	Mostek	25089
MK 50981	Mostek	2560A
MK 50982	Mostek	2560A
MK 50991	Mostek	2560A

Part Number	Manufacturer	AMI Functional Equivalent Part
MK 50992	Mostek	2560A
MK 5116	Mostek	3501/3502, 3507
MK 5151	Mostek	3501/3502, 3507
MK 5156	Mostek	3503/3504, 3506
MK 5170	Mostek	2562/2563
MK 5175	Mostek	25610
MK 5387	Mostek	2559
MK 5389	Mostek	25089
MM 5393	National	2560A
MM 5395	National	2559
ICM 7206	Intersil	2559
ACF 7310,12,7410	G.I.	3526
ACF 7323C	G.I.	3525
ACF 7363C	G.I.	3525
ACF 7383C	G.I.	3525
μPD 7720	NEC	2811
ML 8204	Mitel	2561A
ML 8205	Mitel	2561A
MT 8865	Mitel	3525
AY5 9100	G.I.	2560A
AY5 9151	G.I.	2560A
AY5 9152	G.I.	2560A
AY5 9153	G.I.	2560A
AY5 9154	G.I.	2560A
AY5 9158	G.I.	2560A
AY5 9200	G.I.	2562/2563
AY3 9400	G.I.	2559
AY3 9401	G.I.	2559
AY3 9410	G.I.	2559
AY5 9800	G.I.	3525
AY3 9900	G.I.	3501/3502

Memory Products

CMOS RAMs

Vendor	256×4	1K×1	1K×4	4K×1
AMI	S5101	S6508	S6514*	S6504*
FUJITSU	—	—	6514/8414	8404
HARRIS	6561	6508	6514	6504
HITACHI	435101	—	4334	4315
INTERSIL	6551	6508	6514	6504
MOTOROLA	145101	146508	—	146504
NATIONAL	74C920	74C929	6514	6504
NEC	5101	6508	444/6514	—
OKI	573	574	5115	—
RCA	5101	1821	1825	5104
SSS	5101	5102	—	—
TOSHIBA	5101	5508	5514	5504

*To Be Announced

BYTE WIDE NMOS ROMs

Vendor	1K×8-24 Pin	2K×8-24 Pin	4K×8-24 Pin	*4K×8-24 Pin	8K×8-24 Pin	8K×8-28 Pin
AMI	S68308	S6831B	S68332	S2333	S68A364	S2364
AMD	AM9208	AM9216	AM9232	AM9233		
EA	EA8308	EA8316	EA8332	EA8333		
FAIRCHILD	F68B308	3516				
FUJITSU					MB8364	
GI			RO3-9332	RO3-9333	RO3-9364	
HITACHI	HN46830		HN462532			
INTEL	2608	2616		(2332)		(2364)
MARUMAN		MIC2316	MIC2332		MIC2364	
MITSUBISHI	M58730		M58333			
MOS		MPS2316	MPS2332		MPS2364	
MOSTEK		MK34000			MK36000	MK37000
MOTOROLA	MCM68308	MCM68316	MCM68332		MCM68364	
NATIONAL		MM52116	MM52132		MM52164	
NEC	PD2308	PD2316	PD2332		PD2364	
NITRON	NC6550					
OKI	MSM3770	MSM3870				
PANASONIC			MN2332			
ROCKWELL		RO3-9316				
SGS		M2316				
SIEMENS		SAB8316	SAB8332			
SIGNETICS	2608	2616	2632		2664	
SMC			ROM4732			
SYNERTEK		SY2316	SY2332	SY2333	SY2364	
TI			TMS4732		TMS4764	
TOSHIBA		TMM334	TMM333			TMM2364

*Pin compatible with 2732 EPROM

Source: IC Master 1980

S6800 Family

AMI	Fairchild	General Instruments	Hitachi	Motorola	National	Texas Instruments
S1602	—	AY-3-1014	—	—	MM5303N	TMS6011
S2350	—	—	—	—	—	—
S6800	F6800	—	HD46800	MC6800	—	—
S6801	—	—	—	MC6801	—	—
S6802	F6802	—	HD46802	MC6802	—	—
S6805	—	—	HD46805	MC6805	—	—
S6808	F6808	—	HD46808	MC6808	—	—
S6809	—	—	—	MC6809	—	—
S6810	F6810	—	HD46810	MC6810	—	—
S6821	F6821	—	HD46821	MC6821	—	—
S6840	F6840	—	HD46840	MC6840	—	—
S6846	F6846	—	HD46846	MC6846	—	—
S6850	F6850	—	HD46850	MC6850	—	—
S6852	F6852	—	HD46852	MC6852	—	—
S6854	F6854	—	HD46854	MC6854	—	—
S68488	F68488	—	HD468488	MC68488	—	—
S68045	—	—	—	—	—	—

S9900 Family

AMI	Texas Instruments
S9900	TMS9900
S9901	TMS9901
S9902	TMS9902
S9980	TMS9980
S9981	TMS9981

Alterable Microcomputer Family

Contact factory for complete data sheet.

AMI's all-CMOS Alterable Microcomputer Family contains four products: the AMU/PR, a prototyping device; the S99C91, a 16-bit CMOS microprocessor; the S99C923, a general-purpose I/O (GPIO) chip with 16 single-bit I/O ports; and the S99C922 containing all the functions of the GPIO in addition to a versatile counter/timer subsystem.

The S99C91, S99C922 and S99C923 have been topologically designed so that they can be integrated on a single chip, together with additional peripheral modules and memory, to form a customized CMOS 16-bit Alterable Microcomputer Unit (AMU). The Alterable Microcomputer thus offers volume users a low-cost upward migration path towards system implementations with minimal package count — a feature unmatched by any other microcomputer product family.

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

AMU/PR

CMOS 16-BIT MICROPROCESSOR ALTERABLE MICROCOMPUTER FAMILY

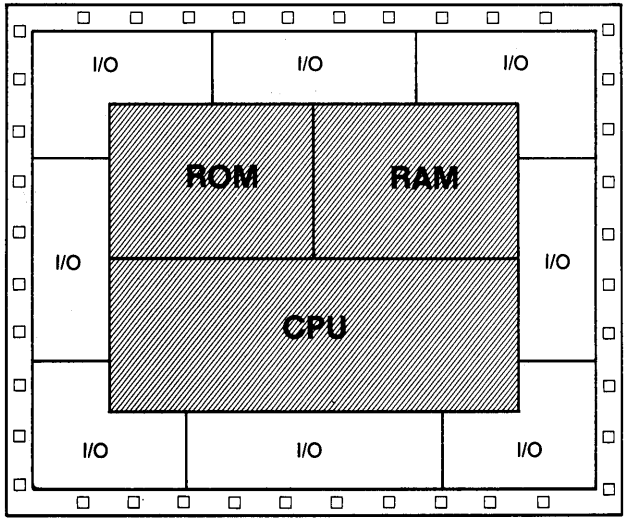
Features

- ☐ CMOS Silicon-Gate Technology
- ☐ 16-Bit Instruction Word
- ☐ 2K Bytes ROM, 128 Bytes RAM On Chip
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 64K Bytes of Addressable Memory
- ☐ 8-Bit Memory Data Bus
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O, and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 5 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ On-Chip Clock Generator
- ☐ Single 5V Supply
- ☐ 16 General Purpose Flags
- ☐ Power Down State (IDLE)
- ☐ Compatible With All S9900 Peripherals
- ☐ 48-Pin Package

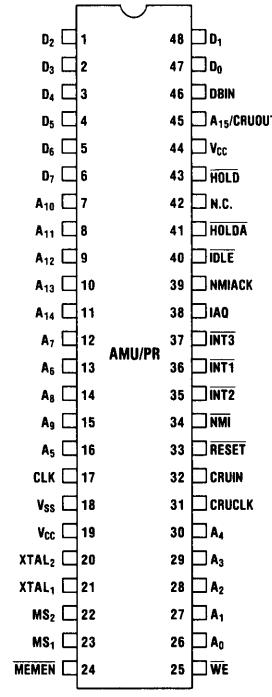
General Description

The AMU/PR is a single-chip 16-bit central processing unit (CPU) produced using an advanced dual-poly CMOS silicon-gate technology. The instruction set includes capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files (resident in memory) which allow faster response to interrupts and increase programming flexibility. Separate bus structures simplify the system design. AMI provides a compatible set of CMOS memory and support circuits to be used with the AMU/ PR system. The AMU/PR is the prototyping chip for the AMI Alterable Microcomputer Family. The Alterable Micomputer Family system is fully supported by software and hardware development systems.

Alterable Microcomputer Functional Block Diagram



Pin Configuration



CMOS 16-BIT MICROPROCESSOR ALTERABLE MICROCOMPUTER FAMILY

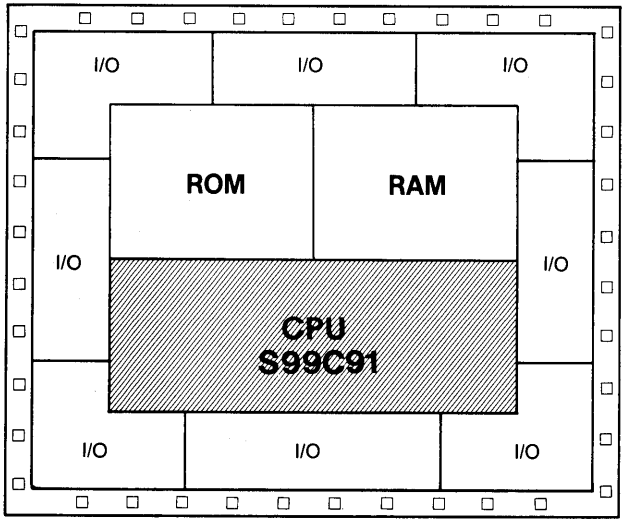
Features

- ☐ CMOS Silicon-Gate Technology
- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 64K Bytes of Addressable Memory
- ☐ 8-Bit Memory Data Bus
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O, and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 4 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ On-Chip Clock Generator
- ☐ Single 5V Supply
- ☐ 16 General Purpose Flags
- ☐ Power Down State (IDLE)
- ☐ Compatible With All S9900 Peripherals
- ☐ 40-Pin Package

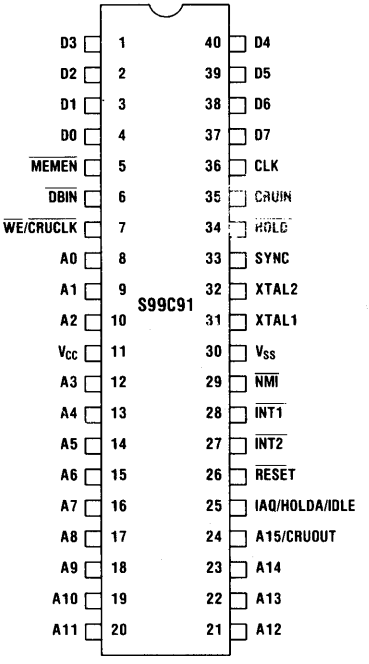
General Description

The S99C91 is a single-chip 16-bit central processing unit (CPU) produced using an advanced dual-poly CMOS silicon-gate technology. The instruction set includes capabilities offered by full minicomputers and is S9940 compatible. The unique memory-to-memory architecture features multiple register files (resident in memory) which allow faster response to interrupts and increase programming flexibility. The separate bus structure simplifies the system design. AMI provides a compatible set of CMOS memory and support circuits to be used with the S99C91 system. The S99C91 is a member of AMI's Alterable Microcomputer Family.

Alterable Microcomputer Functional Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S99C922

GENERAL PURPOSE INPUT/OUTPUT (GPIO) AND VERSATILE COUNTER MODULE ALTERABLE MICROCOMPUTER FAMILY

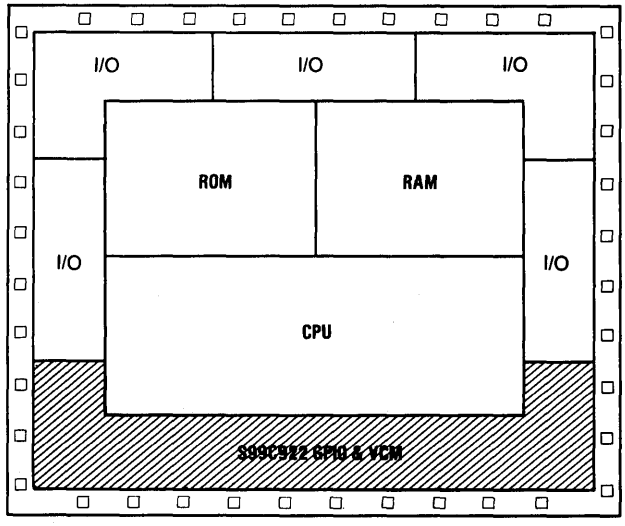
Features

- ☐ Advanced CMOS Technology
- ☐ AMI S99C91 and AMU/PR Family Compatible
- ☐ General-Purpose CRU Interface
- ☐ 16 Dedicated Single-Bit I/O Ports
- ☐ Ports Individually Software-Configurable as Input or Output
- ☐ Software Read of Input/Output Port Status
- ☐ 16 Bit Versatile Counter
- ☐ Two Modulus Registers
- ☐ Programmable Counter Output Pin
- ☐ Programmable Counter Interrupt Output
- ☐ Two Programmable External Gate/Count Inputs
- ☐ Single +5V Supply

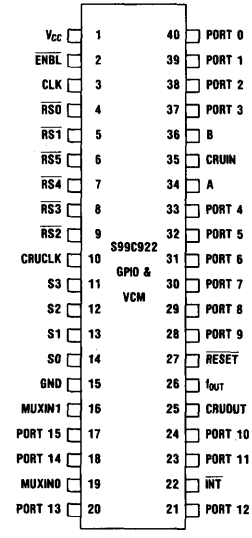
General Description

The S99C922 General Purpose I/O and Versatile Counter Module is designed to provide counter/timer functions and expandable I/O ports in an AMU or S9900 family microprocessor system. It is fabricated in dual polysilicon CMOS technology and is completely CMOS-compatible. The S99C922 is a member of AMI's Alterable Microcomputer family.

Alterable Microcomputer Functional Block Diagram



Pin Configuration



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S99C923

GENERAL PURPOSE INPUT/OUTPUT (GPIO) MODULE ALTERABLE MICROCOMPUTER FAMILY

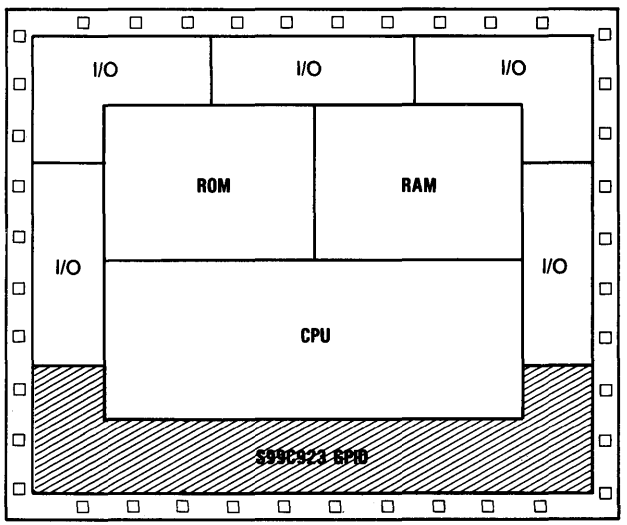
Features

- ☐ Advanced CMOS Technology
- ☐ AMI S99C91 and AMU/PR Family Compatible
- ☐ General-Purpose CRU Interface
- ☐ 16 Dedicated Single-Bit I/O Ports
- ☐ Ports Individually Software-Configurable as Input or Output
- ☐ Software Read of Input/Output Port Status
- ☐ Single +5V Supply

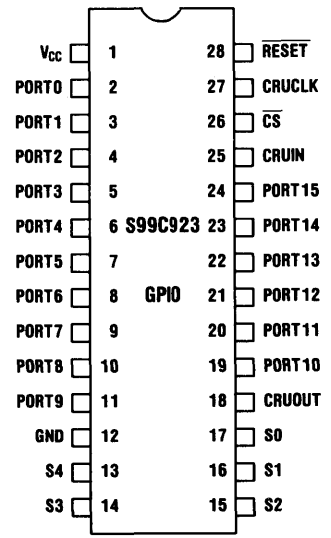
General Description

The S99C923 General Purpose I/O module is designed to provide expandable I/O ports in an AMU or S9900 family microprocessor system. It is fabricated in CMOS silicon-gate technology and is completely CMOS-compatible on all inputs. The S99C923 is a member of AMI's Alterable Microcomputer family.

Alterable Microcomputer Functional Block Diagram



Pin Configuration



No other company can match AMI's track record in developing state-of-the-art custom MOS products. With more than 1500 custom devices designed and manufactured since 1967, AMI has more experience than any other integrated circuit company in building a wide variety of custom microcircuits.

AMI not only has the experience, but the design engineering organization and the advanced production and testing facilities to produce the highest quality MOS/VLSI circuits. And because AMI also offers standard memory, microprocessor, telecommunication and consumer products and the widest variety of custom LSI processes in the industry, we're able to be objective in helping customers determine their most cost effective approach.

THE ADVANTAGES OF CUSTOM CIRCUITS

Since a single custom MOS/VLSI chip can replace expensive electromechanical devices, discrete logic components, or less efficient general purpose LSI circuits, it offers a number of benefits not available with standard logic.

Custom circuits save money. Grouping functions onto a single chip lowers production and inventory costs dramatically. That reduces your product manufacturing costs as well.

Custom circuits are more reliable. Putting a complete system on a chip trims component count, improving both product reliability and production yields. Rework, repair and replacements are minimized.

Custom circuits reduce space and power requirements. Fewer components means both space and power requirements are reduced.

Custom circuits offer superior performance. Since the circuit is designed to your requirements, features and functions can be incorporated which are not available in general purpose chips. Special tailoring reduces test requirements as well.

Custom circuits offer proprietary protection. Being tailored exactly to your requirements, a custom circuit cannot be easily duplicated. This can help put you ahead — and keep you ahead — of your competition.

THE SPECTRUM OF SOLUTIONS

The decision to use a custom circuit depends on your system design requirements — such things as complexity, features, size and power limitations. But no longer is your custom decision limited by low volume or short development time — not when you come to AMI.

AMI has a full spectrum of custom solutions to assure you get that solution which meets your system performance and time-to-market requirements at the lowest possible cost.

AMI's spectrum of solutions bridges the total span of volume, timing and interface needs of our customers. From semi-custom designs, to full custom design — somewhere on the spectrum, your development time and volume requirements can be met. For customers who already have their designs, AMI can provide custom fabrication for the customer's tooling. We will even teach custom design if that's what our customers need. And we can even go a step further and license the technology for a customer to set up his own fabrication capability. No other company offers such a spectrum of solutions. And no other company has more experience at helping you pick the best solution for your needs.

LOGIC ARRAYS

Our semi-custom logic arrays are the best solution for circuits of moderate complexity in low-to-medium volume applications.

AMI CMOS semi-custom logic arrays are standard logic layouts of everything except the final metal interconnect pattern. Since only the final pattern needs to be developed to customize your circuits, both development time spans and development costs are dramatically reduced. Because wafers containing arrays are preprocessed and inventoried, production lead times are short. Logic arrays are especially attractive for applications requiring circuit volumes from 1,000 to 50,000 units per year.

For more details on AMI's logic arrays, refer to the "Logic Array" section of this catalog.

STANDARD CELL CUSTOM

Standard cells are full custom circuits which are designed from computer stored modular cells. The computer assembles the cells into a collection of functional blocks to form a custom circuit. Since standard cells utilize predesigned cells, development time is reduced dramatically and development costs are cut 30 to 50 percent over conventional custom design. Circuit size is likely to be slightly larger than a conventional custom circuit, so they are most appropriate where rapid development is more important than minimal size. Standard cells are cost effective in volume levels beginning around 10,000 circuits.

For more details on AMI standard cells refer to page of this section.

CONVENTIONAL CUSTOM DESIGN

With conventional custom, circuit size is shrunk to the absolute minimum. Since less silicon is used, production costs are dramatically reduced. Where end product volume is high — beyond 50,000 units per year — or where special requirements for lowest power, minimal space or highest performance exist, the solution is likely to be conventional custom design.

Instrumental in the design of custom circuits is our Symbolic Interactive Design System (SIDS). The design is done primarily with SIDS where a layout designer works with symbols directly at a large screen alphanumeric color CRT. After the SIDS circuit design has been completed and verified, the symbols are converted to polygons and a 10X reticle tape is prepared.

SIDS uses on-line, real-time design rule checking capability to isolate design rule errors in the layout. This allows immediate correction which greatly reduces the development span time.

Also a nodal trace function permits a designer to trace and highlight a given electrical node. In this way, the designer can manually insure that the node is connected as specified in the master logic description.

Full background real-time design rule checking on windows, cells, and chips is supported, as is full background continuity checking against the master logic description. This eliminates the delay from digitizing and batch processed computer checking of circuits for accuracy.

With SIDS, error correction, circuit modification and area relocations take only minutes. That significantly reduces design cycle time and development costs.

Computer-aided hand-drawn layouts are used to reduce extremely complex circuits to the absolute smallest size. Development time and costs are higher, but in certain cases, size or complexity requirements may require the hand-drawn approach.

CUSTOMER DESIGNED SOLUTIONS

Many of our customers have their own circuit designs. In this case AMI can provide custom circuit fabrication for customer-owned tooling. We can accept a customer's fabrication job at any level: working plates, pattern generation tape or data base tapes accompanied with a developed test program and specification. Close cooperation between the customer and AMI simplifies circuit debug and facilitates manufacture at circuit completion. At the same time it gives the customer complete proprietary protection and control over design and production scheduling.

Through AMI's diversity of MOS process types, engineering support, test equipment and package options, we provide you a degree of flexibility no one else can offer. For more details on AMI's MOS processes, refer to the "General Information" section of this catalog.

JOINT DEVELOPMENT TEAMS

Through a Joint Development Team (JDT) we can teach a customer to design his own MOS/VLSI circuits. The JDT is a combination of technically skilled people from the partner company and AMI who function as a design group concentrating on the customer's products alone. The JDT partner brings his system design staff and AMI brings the MOS/VLSI staff and its design technology. The partner becomes part of an in-house AMI design group. The end result is a design capability for the partner company for circuits that AMI will fabricate.

If the customer wants to go beyond designing his own circuits to operating his own manufacturing/pilot line, AMI will license the necessary technology in those situations where a long-term business relationship can be established between the partner company and AMI.

AMI PROVIDES LEADING CAD TECHNOLOGY

At almost all levels of the spectrum, computer-aided design (CAD) software and hardware aids are employed

to assure correctness of design each step of the way and to shorten design spans reducing customer risk and lowering design cost. Highly efficient programs have been implemented to assist in logic design and simulation, layout planning, switched capacitor analysis routines and symbolic interactive design layout, to name just a few.

Hardware design aids include:

- On-site Burroughs 7760 computer with multiprocessing capability.
- Computer terminals built around a Prime computer and engineering design facilities which tie into the on-site 7760 and time-sharing services.
- Computervision interactive graphics system which provide on-line generation and editing of composite drawings; includes drafting surfaces and CRT displays.
- Calma graphics system for both production digitizing and on-line changes.
- Calma GDS-11 high speed electrostatic plotter.
- High speed, high resolution Electromask 9-track pattern generator.

Software design aids include:

Logic Design

- **Register Transfer Language (RTL) Simulation** — Provides a system behavior description to define instruction sets, optimize data paths, control hardware algorithm design and establish register designs.
- **Glide** — Permits user to design layout, simulate, generate patterns and develop test programs for logic arrays.
- **Path Analysis Program (PATH)** — Permits gross logic checks to be made before design, and final logic checks from the ultimate design.
- **Logic Simulator (SIMAD)** — (SIMulator with Assignable Delays) simulates logic network behavior for design verification and propagation delays.
- **Programmable Logic Array Designs Aids (PLAID)** — Uses state tables and Boolean equations to generate the optimum physical structure for random logic designs.
- **Block Oriented Logic Translator (BOLT))** — A logic description compiler that generates a common data base used by SIDS, SIMAD, LPA, continuity check, PATH and CIPAR.
- **Design Rule Checking (DRC)**
- **Trace and Continuity Checking**

Circuit Design

- **Circuit Simulator (ASPEC)** — Analyzes DC operation, DC transfer functions, time domain or transients and frequency domain or small signal AC characteristics.
- **Pole Zero Analysis (PZSLIC)** — Program analyzes the frequency domain of linear integrated circuits.
- **Switched Capacitor Analysis Routine (SCAR)** — Analyzes switched capacitor filter designs for telecommunications and other analog circuits.
- **Data Analysis Program (DAP)** — Analyzes data from circuit fabrication to maintain the parameters of circuit designs.

Mask Design

- **Layout Planning Aid (LPA)** — Lays out the chip plan and interconnection between functional blocks of an integrated circuit.
- **Symbolic Interactive Design System (SIDS)** — Permits a layout designer to work directly with a computer to lay out and check a circuit on a CRT screen, dramatically shortening layout time requirements.
- **Circuit Interactive Place and Route (CIPAR)** — Automatically creates error-free mask designs in extremely short time spans.

Test Generation

AMI utilizes numerous software programs to generate test programs for integrated circuits. All serve to reduce the time needed to develop test programs to meet customer specifications.

DIGITAL AND ANALOG COMBINATIONS

AMI is a leading innovator in combining digital and analog functions on a single chip. We can combine any of the functions below into an optimum circuit configuration to meet your needs. Unique combinations of these functions are already used in many applications in the communications, consumer, and industrial marketplace.

DIGITAL	ANALOG
PLA	OP AMP
ALU	Oscillator
Inverter	Comparator
RAM and ROM	Voltage Reference
Shift Register	A/D and D/A Converters
Interface Driver	Switched Capacitor Filters
Automatic Power Down	Programmable Power Down
	Phase Locked Loops

STATE OF THE ART PACKAGING

AMI's packaging capability spans a broad spectrum, beginning with plastic, ceramic and CERDIP and going on to chip carriers, die bonding to PC boards and, most recently, mini-flat packs. As well as being a leader in plastic packaging for the high volume, low cost consumer industry, AMI's high reliability plastic packages and chip carriers are accepted under the stringent requirements in the Telecom and Automotive industries. As many industry segments move toward space-saving packages, AMI remains in the forefront in packaging using chip carriers. AMI now is developing a family of mini-flat packs which are a plastic alternative to a chip carrier.

AMI DELIVERS QUALITY

AMI quality controls for in-process wafer inspection and final assembly and test are the best in the industry. Our care in fabrication, assembly and test mean that you get products that meet your specifications for reliability. Because over 70 percent of our total production is custom, we perform many checks routinely that would only be done on special orders and at additional cost by other manufacturers. In fact, our own in-house standards are tougher than most of our customers require. Most importantly, AMI is committed to making sure that everything we do is done right, every time we do it.

The Industry's Highest Standard

AMI has consistently pursued product excellence and has reached for higher quality levels in finished products shipped. Circuits are inspected to 0.1% AQL or your specifications, whichever is more stringent.

This 0.1% AQL can put you in a superior competitive position. Your incoming test and assembly costs come down since there is less reworking on the line. And your customers receive a more reliable product.

Quality Checks

Among the routine quality controls exercised over every product at AMI are:

- Full logic design checks against system specifications
- Circuit simulation to verify performance against objectives
- Working plates check on automatic checkers
- Automated mask fabrication checks
- In-process wafer fabrication checks
- Wafer sort tests
- 100% optical inspection at dicing
- 100% die attach checking
- 100% lead bonding inspection prior to package sealing
- Seal checks, fine and gross leak tests
- Final digital and analog tests
- Customer specified environmental tests

Meticulous in-process checks are performed on design and workmanship at every step, to ensure a fully manufacturable device. In manufacture, lot process and yield data are captured and examined as a matter of routine.

CUSTOM MOS/VLSI FROM AMI

The information in this section has been presented to show not only how and why custom can be used, but also to explain the types of commitment at AMI to total custom circuit development and to customer tooling processing. Whatever your requirements or questions about a custom or semicustom MOS/VLSI circuit, we can help you find the right solution. Because no other company offers you more services, experience and capability in a single place than AMI.

SUPPLEMENT — AMI'S STANDARD CELL PROGRAM

Program Description

The cells in the Standard Cell Program are basic logic elements such as gates, flip-flops, register counter bits and I/O devices. Each cell has been previously designed and analyzed for performance. Complex digital functions can be rapidly implemented by interconnecting the various cells. Most cells have a series 4000 CMOS equivalent and a 74LS TTL equivalent for ease of bread boarding.

The cells are initially designed on an interactive color graphics terminal — AMI's SIDS (Symbolic Interactive Design) system. The cell library is maintained within the SIDS data base. If other CAD (Computer-Aided Design) systems are used internally by a customer, the cell library can be digitized onto these systems.

Using the SIDS system, new cells or modifications of existing cells can be generated and added to the cell library rapidly, without any hand layout. Similarly, non-cell functions such as analog elements or memory arrays, RAM or ROM, can be designed using SIDS and merged with standard cells.

This ability to add special features efficiently, makes AMI's standard cell program far more flexible than other manufacturer's cell development systems.

PERFORMANCE

AMI's standard cell circuits can be successfully used in digital circuits with operating speeds up to 10MHz for NMOS (or CMOS at 10V V_{CC}) and 8MHz for CMOS (5V V_{CC}). It should be emphasized that if only a small portion of the circuit requires faster performance, this portion can be "customized" either by creating special cells or by designing circuitry outside of the cell structure. AMI will review customer logic without obligation to determine if a cell design is feasible.

NMOS Cells

The NMOS cells (Table I) are implemented using a 4 micron silicon gate process and can be used over the full military temperature range (−55°C to 125°C). Operating voltage is 5V±10%. The NMOS cells have been designed with three power/speed options. The fastest cells also have the highest power consumption and use the most area. Therefore, the fast cells should be used only where circuit performance requires high speed. Most circuits are optimized by using a combination of low power, standard and high speed cells.

CMOS Cells

The CMOS cells are designed using a 5 micron silicon gate oxide-isolated process. This process is well suited for analog circuitry and some analog cells will be added to the digital cells shown. CMOS cells (Table II) are characterized for 3V to 12V operation over the full military temperature range (−55°C to 125°C). CMOS cells are generally used where low power battery operation or backup are required. As in 4000 series CMOS, power for static operation is near zero. The typical power shown in Table II is for operation at 1MHz.

TOPOLOGY

Both CMOS and NMOS standard cells are fixed height (except I/O cells with width varying with cell complexity). Inputs and outputs to internal cells are available at both the top and bottom of cells. In addition, cells may be "flipped" from left to right when this orientation results in a shorter connection.

Most interconnection is accomplished by metal and polysilicon although diffusion can be used if required. At present, both NMOS and CMOS cells use single layer poly and metal. Input and output cells (for external pinouts) are arranged (no fixed spacing) around the cell periphery. These external cells generally are available in two different shapes. The long, narrow version is used where chip area is restricted by the number of pinouts. This version results in minimum bonding pad spacing. For designs that are not "pad-limited", the other version (approximately equal width and height) is used to minimize die size.

NMOS Cells

The cell height for the NMOS cells is 161.5 microns. V_{DD} and V_{SS} connections are metal lines across the cell. Two other metal lines cross the cell. These additional metal lines are used for clocks. The use of wide metal clock lines minimizes clock skew to maintain synchronous operation. Since the multiplexer cell does not require clocks, there is no connection to the cell itself and the clock lines are simply routed across the cell.

CMOS Cells

The CMOS cells have a cell height of 144 microns. In the CMOS cells, a 16 micron grid is used. All cell boundaries and cell input/output locations are located in 16 micron increments. This grid system increases cell area, but has several important advantages.

A relatively simple place and route software routine can be used for automatic circuit layout. Manual layout (primarily for user not having access to AMI CAD systems) is greatly simplified since any gridded paper can be used for rapid layout plan and trial interconnect. Computer assisted interconnect on SIDS (AMI Computer-Aided Design System) does not require the fixed grid.

DEVELOPING YOUR STANDARD CELL DESIGN

AMI offers three basic options for developing a standard cell custom circuit.

AMI Standard Development

The circuit user provides a completed logic diagram and a circuit specification. AMI performs all other design activity including MOS logic design, circuit design, layout, mask generation and fabrication of wafers. This development option is recommended for most users desiring to build a single LSI device and for multiple circuit users who do not wish to become directly involved in the MOS circuit development.

Shared Development

For those users who want to participate in the design of a standard cell circuit, a *Design Manual* is provided for either the NMOS or CMOS cell family. The Design Manual has complete performance data over temperature and voltage for all the cells. The manual contains information for calculating speed, power and die size. In addition, guidelines for logic design, breadboarding and developing test programs are provided. In a typical "shared" development, the user designs the logic using the available cells and performs preliminary power and speed calculations. The user may then identify or even lay out areas of the circuit requiring special attention to guarantee performance. The *Design Manual* is provided without obligation, but AMI does require the user to sign a "Non-Disclosure" agreement. A shared development is recommended for users who are considering multiple circuit developments, but who do not have an internal MOS design capability.

Customer Designed Input by Terminal

Users who wish to design their standard cell circuits, but do not want to invest in a CAD (Computer-Aided Design) system, can design their circuit on a low cost terminal. AMI's logic simulator SIMAD (SIMulator with Assignable Delays) is available for the users to simulate their desired logic on a time share terminal. The standard cells have been stored as logic MACROS. When the users are satisfied with the logic simulation they notify AMI, and AMI uses this data base to run the customer's software programs. A plot of the circuit is returned to the user for approval. After approval, AMI will deliver samples of the device in a short time period.

Customer Designed Circuits

For those users who wish to design custom circuits entirely within their own facility, AMI licenses the use of both (NMOS & CMOS) cell families. Standard cell tooling is provided in the form of a data base tape containing the topological information of the cells. AMI also licenses the use of several powerful CAD tools used in developing cell circuits. The user does the complete circuit design and develops a pattern generator tape which is used to make the wafer processing masks. Customer designed standard cell circuits require the user to have or be willing to develop a MOS design capability. However, a mask making or wafer fabrication facility is not required.

DEVELOPMENT SCHEDULE

One of the primary objectives of a cell program is to design a LSI circuit in a minimum time span. Circuit design is almost eliminated since both function and performance of the cells have been previously determined. Some effort is still required to verify that timing and power requirements are met. When cells are used, layout consists of arranging the cells in rows and making the required interconnections either on the computer assisted SIDS system or using a software place and route routine. In a conventional custom circuit layout, seven or eight mask layers must be carefully layed out and checked for possible layout errors. This layout simplicity greatly reduces the possibility of a layout error causing a time consuming second iteration of the design cycle.

DEVELOPMENT COST

Most AMI cell developments costs between $20,000 and $65,000. The factors that determine the cost of a standard cell circuit are:

Size

The number of cells required to implement the required function affects the development cost. Tables I and II show both the area of the cells and also the number of "2-input gate equivalents." This gate equivalent number is a short cut method of estimating size of a circuit without analysis of the logic. The yield of good die per wafer decreases rapidly as die size increases above 200 mils on a side. For most commercial applications, die size should be limited to less than 230 mils square. Figure 9 shows an approximation of die size vs. equivalent gate count.

Complexity

The following factors can affect circuit development costs: areas within the circuit that have critical timing require special layout attention; portions of the design that cannot be implemented with existing cells; special functions which must be added to a cell circuit.

Completeness of Design

The type of information provided by the circuit user is a major cost factor. For most circuits, AMI prefers to work from finished logic that has either been "breadboarded"

or analyzed by computer simulation. However, AMI will develop custom circuits (standard cell or conventional) from a detailed specification of the intended circuit.

Test Plan Development

Regardless of the design or layout method, production shipments of a custom device are dependent on a test program to test devices at wafer sort and after final assembly. A substantial portion (up to 20%) of the development cost is required for generating and "debugging" the test program. For users who are able to provide detailed test information, the development cost is reduced.

DEVELOPMENT OPTIONS	AMI Standard Development	Shared Development	Customer Development
Functional Specification	C	C	C
Logic Diagram	C	C	C
Breadboard (if built)	C	C	C
MOS Logic Diagram (Logic Using Cell Elements)	O	C	C
Logic Simulation	A	C	C
Circuit Design	A	O	C
Layout Plan (Cell Location)	A	O	O
Layout (Interconnection)	A	A	O
Pattern Generator Tape (Computer Tape of Layout)	A	A	O
Photo Masks	A	A	A
Wafer Fabrication	A	A	A
Assembly	A	A	A
Test Vectors	A	O	C
Complete Test Program	A	O	O

A = AMI Task
C = Customer Task
O = Optional - Customer or AMI Task

NMOS Standard Cells Summary

Table 1. Combinational Elements

CELL NAME	DESCRIPTION	CMOS EQUIV (1)	TTL EQUIV (1)	GATE EQUIV	AREA (2)	SPEED (3)	POWER (4)
ADDRL1	FULL ADDER	4008	74LS82	9.7	49.8	176	619
ADDRL3					58.1	48	2750
ADDRS5					58.1	58.1	7150
ANRIL1	AND-NOR-INV GATE	4019	74LS51	2.3	19.7	88	124
ANRIL3					18.5	24	550
ANRIS5					22.6	12	1788
INVRL1	INVERTER	4069	74LS04	0.7	7.6	57	124
INVRL3					8.4	15	550
INVRL5					11.7	5	1788
INVRL7					11.7	3	4675
MUX4L1	4 TO 1 MULTIPLEXER	4052	74LS153	6.3	35.9	83	495
MUX4L3					41.3	26	2200
MUX4S5					36.3	25	7150
NND2L1	2-INPUT NAND	4011	74LS00	1.0	10.0	54	124
NND2L3					10.0	16	550
NND2L5					14.5	6	1788
NND3L1	3-INPUT NAND	4023	74LS10	1.3	13.0	62	124
NND3L3					13.0	16	550
NND3L5					14.5	8	1788
NND4L1	4-INPUT NAND	4012	74LS20	1.7	15.4	65	124
NND4L3					15.0	25	550
NND4L5					19.7	12	1788
NOR2L1	2-INPUT NOR	4001	74LS02	1.0	9.6	67	124
NOR2L3					10.3	15	550
NOR2L5					11.7	6	1788
NOR2L7					17.1	4	4675
NOR3L1	3-INPUT NOR	4025	74LS27	1.3	12.3	92	124
NOR3L3					14.2	18	550
NOR3L5					17.1	7	1788
NOR2L7					22.6	5	4675
NOR4L1	4-INPUT NOR	4002		1.3	16.9	79	124
NOR4L3					17.7	18	550
NOR4L5					17.1	6	1788
NOR4L7					25.4	5	4675
XNR2S1	EXCLUSIVE NOR	4077	74LS266	2.3	15.0	86	248
XNR2S3					15.4	22	1100
XNR2S5					19.7	10	3575
XOR2S1	EXCLUSIVE OR	4070	74LS136	2.3	14.7	69	248
XOR2S3					15.0	19	1100
XOR2S5					17.1	9	3575

NMOS Standard Cells Summary

Table 2. I/O Elements

CELL NAME	DESCRIPTION	CMOS EQUIV (1)	TTL EQUIV (1)	GATE EQUIV	AREA (2)	SPEED (3)	POWER (4)
IPUPF0	TTL INPUT BUFFER W/PULL UP			2.7	95.6	51	663
IPUPF1					95.6	17	2172
IPUPF2					95.6	16	2172
IPUPT0					91.0	41	663
IPUPT1					91.0	12	2172
IPUPT2					91.0	11	2172
ISTRF0	SCHMITT TRIGGER INPUT BUFFER			2.7	79.2	47	248
ISTRF1					79.2	14	1100
ISTRT0					91.0	47	248
ISTRT1					91.0	14	1100
ITTLF0	TTL INPUT BUFFER			2.0	79.1	37	525
ITTLF1					79.1	15	2035
ITTLF2					79.1	12	2035
ITTLF3					88.8	10	5500
ITTLT0					87.6	34	525
ITTLT1					87.6	16	2035
ITTLT2					87.6	10	2035
ITTLT3					91.0	9	5500
OBAAF1	TTL OUTPUT BUFFER (6)	4050		2.0	91.0	86	550
OBAAF2					95.4	30	4152
OBAAF3					102.0	18	6875
OBAAT1					91.0	87	550
OBAAT2					95.5	29	4152
OBAAT3					100.0	17	6875
OB0DF1	OPEN DRAIN OUTPUT BUFFER (7)		74LS05	1.0	95.4	91	550
OB0DF2					95.4	30	1980
OB0DF3					95.4	17	4675
OB0DT1					89.3	92	550
OB0DT2					89.3	30	1980
OB0DT3					89.3	16	4675
OBTSF1	TTL TRI-STATE OUTPUT BUFFER (6)			2.0	124.8	74	550
OBTSF2				2.3	124.8	36	1980
OBTSF3				2.3	134.6	23	4675
OBTST1				2.0	113.4	76	550
OBTST2				2.3	117.9	33	1980
OBTST3				2.3	126.9	22	4675

NMOS Standard Cells Summary

Table 3. Flip Flops

CELL NAME	DESCRIPTION	CMOS EQUIV (1)	TTL EQUIV (1)	GATE EQUIV	AREA (2)	MAX FREQ (5)	POWER (4)
BBSRD1	DYNAMIC SERIAL SHIFT REGISTER	4015	74LS164	2.0	9.6	10.5	124
BBSRD3					11.9	16.7	550
BBSRD5					14.5	31.2	1980
BBSRD7					22.6	45.4	4675
CKDRL1	CLOCK DRIVER			2.7	13.0	3.8	248
CKDRL3				3.3	17.3	22.4	1100
CKDRL5				3.3	19.7	36.9	3575
CKDRL7				3.3	47.2	37.6	9350
DFFLS1	D-FLIP FLOP W/ASYN SET & RESET	4013	74LS74	6.0	31.6	7.7	371
DFFLS3				6.0	33.6	13.3	1650
DFFLS5				5.3	36.3	23.5	2998
DFSCS1	D-FLIP FLOP W/ASYN SET & RESET SINGLE CLOCK	4013	74LS74	6.7	30.6	3.2	371
DFSCS3					33.4	13.7	1650
DFSCS5					49.8	22.0	2998
JKFFS1	J-K--FLIP FLOP W/ASYN SET & RESET	4027	74LS112	9.7	41.7	5.1	743
JKFFS3				9.7	44.8	14.3	3300
JKFFS5				8.0	55.2	22.0	7535
LTCHS1	D-LATCH	4042	74LS75	2.7	13.4	8.3	248
LTCHS3					13.8	16.6	1100
LTCHS5					17.1	17.2	1980
RIFCS1	RIPPLE COUNTER BIT W/ASYN SET & RESET	4020	74LS93	6.0	24.7	5.7	371
RIFCS3					27.0	13.3	1650
RIFCS5					36.3	23.2	2998
SRPLS1	SHIFT REGISTER BIT W/SYNC PARALLEL LOAD + COMMON ASYN RESET	4035	74LS166	6.0	28.9	6.3	371
SRPLS3					28.9	11.8	1650
SRPLS5					38.9	20.6	4798

Table 4. Counters

CELL NAME	DESCRIPTION	CMOS EQUIV (1)	TTL EQUIV (1)	GATE EQUIV	AREA (2)	MAX FREQ (5)	POWER (4)
SNCAS1	SYNCHRONOUS COUNTER BIT; Cascadeable W/Asyn Reset	4518	74LS193	8.3	35.9	5.7	619
SNCAS3					40.7	10.5	2750
SNCBS1					33.8	5.0	619
SNCBS3					40.6	12.5	2750
SNCRS5				7.7	47.2	21.7	4978
UDCAS1	UP/DOWN COUNTER BIT; Cascadeable Alternating A & B Sync. Parallel Load, W/Asyn Reset	4518	74LS193	9.0	35.9	5.0	619
UDCAS3					40.6	11.1	2750
UDCBS1					37.8	5.7	619
UDCBS3					38.9	11.8	2750
UDCRS5				10.0	58.1	20.6	4978

NOTES:

(1) All Standard CMOS & TTL parts are NEAREST Equivalent
(2) 1E-6sq. in.
(3) tpd = 0.25 (tp1 + tp0) ns "typical" LOAD = 2 gates of same speed
(4) 1E-6W "typical"
(5) Pmax = 2/(twc + twc1 + 20) MHz "typical"
(6) CL = 15pF
(7) Falling Edge Delay, Cl = 15pF

CMOS Standard Cells Performance Data

Table 2. Combinational and I/O Elements

CELL NAME	DESCRIPTION	CMOS EQUIV	TTL EQUIV	2-IN GATE EQUIV	AREA $IN^2 \times 10^{-6}$	SPEED (TYP) nsec	POWER (TYP) @1MHz, μW
INV1	Inverter	4069	74LS04	.5	10.7	15	66
INV2	Inverting Driver	4049	74LS06	1.5	32.1	23	495
D1	Non-Inverting Driver	4050	74LS07	1.0	28.6	18	400
PD1	Non-Inverting Pad Driver W/Pad	4050	74LSO7	—	201.2	29	1850
PD1A	Non-Inverting Pad Driver W/Pad	4050	74LS07	—	233.3	29	1850
TD1	Non-Inverting 3-State Driver	40097	74LS125	2.5	42.9	26	390
TPD1	Non-Inverting 3-State Driver	40097	74LS125	2.7	227.0	41	1650
TPD1A	Non-Inverting 3-State Drive W/Pad	40097	74LS125	—	266.7	41	1650
ST1	Schmitt-Trigger CMOS Level W/Pad	40106	74LS14	—	139.3	24	150
INP1	Input Pad W/Protection Device and Inverter	4069	74LS04	—	113.5	10	150
TG2	Transfer Gate	—	—	—	14.3	32	57
ND21	2-Input NAND	4011	74LS00	1.0	14.3	19	70
ND31	3-Input NAND	4023	74LS10	1.5	25.0	19	48
ND41	4-Input NAND	4012	74LS20	2.0	21.4	31	39
ND51	5-Input NAND	4068	74LS30	2.5	28.6	31	40
NR21	2-Input NOR	4001	74LS02	1.0	14.3	23	99
NR31	3-Input NOR	4025	74LS27	1.5	17.9	28	69
NR41	4-Input NOR	4030	74LS86	2.5	28.6	32	33
ANR51	3 NAND-2 NOR	4073	74LS15				
	Combo	4025	74LS27	2.5	25.0	34	92
OND41	2 OR +	4071	74LS10				
	2 NAND Combo	4023	74L32	2.0	21.4	26	47
OND42	2-2 OR – NAND	4071	74LS00				
		4011	74LS32	2.0	21.4	26.	72
BUS1	Bus Pad W/3-State Non-Inverting Driver	4097 +	74LS125	—	263.1	13In	
	+ Input Inv	4069	74LS04	—	288.9	51Out	1650
BUS2	Bus Pad W/3-State Non-Inverting Driver	4097	74LS125		288.9	13In	
	+ Cell Aspect Ratio	4069	74LS04	—		51Out	1650
JKL2	JK Logic for D-FF	4027	74LS76	2.5	28.6	32	46
Storage Elements							
DR1	D-FF With Reset (Master-Slave)	4013	74LS74	6.0	71.4	15	486
DRS1	D-FF With Reset and Set	4013	74LS74	7.0	85.7	15	590
LSR1	D-Latch With Reset and Set	4042	74LS75	4.0	50.0	15	360
DR2	D-FF With Reset and Clock	4013	74LS74	6.0	75.0	15	460
DR3	D-FF With Reset and Clock	40174	74LS174	6.0	75.0	15	560
DRS2	D-FF With Reset, Set Clock	4013	74LS74	7.0	85.7	15	510
DFF1	D-FF With Clock	4013	74LS74	5.0	60.7	15	620

AMERICAN MICROSYSTEMS, INC.

Communication Products

For more information on those data sheets which are not included in their entirety refer to AMI's Telecom Design Manual or contact Telecom Marketing at (408) 554-2070.

AMERICAN MICROSYSTEMS, INC.

Communication Products Selection Guide

STATION PRODUCTS

Part No.	Description	Process	Power Supplies	Packages
S2559A/B	Digital Tone Generator	CMOS	3.5V to 13V	16 Pin
S2559C/D	Digital Tone Generator	CMOS	2.75V to 10V	16 Pin
S2559E/F/G/H	Digital Tone Generator	CMOS	2.5V to 10V	16 Pin
S2859	Digital Tone Generator	CMOS	3.0V to 10.0V	16 Pin
S2860	Digital Tone Generator	CMOS	3.5V	16 Pin
S2560A	Pulse Dialer	CMOS	1.5V to 3.5V	18 Pin
S2561, S2561C	Tone Ringer	CMOS	4.0V to 12.0V	18 Pin
S2561A	Tone Ringer	CMOS	4.0V to 12.0V	8 Pin
S2562	Repertory Dialer	CMOS	3.5V to 7.5V	40 Pin
S2563	Repertory Dialer, Line Powered	CMOS	2V to 5.5V	40 Pin
S25089	DTMF Generator	CMOS	2.5V to 10V	16 Pin
S25610	Repertory Dialer	CMOS	1.5V to 3.5V	18 Pin

PCM PRODUCTS

S3501/S3501A	μ-Law Encoder with Filter	CMOS	±5V	18 Pin
S3502/S3502A	μ-Law Decoder with Filter	CMOS	±5V	16 Pin
S3503	A-Law Encoder with Filter	CMOS	±5V	18 Pin
S3504	A-Law Decoder with Filter	CMOS	±5V	16 Pin
S3506	A-Law Combo Codec with Filters	CMOS	±5V	22 Pin
S3507/A	μ-Law Combo Codec with Filters	CMOS	±5V	22/28 Pin

SIGNAL PROCESSORS

RTDS2811	Real-Time Development System			
SSPP2811	Software Simulator Assembly Program Package			
S28211	Signal Processing Peripheral	NMOS	5V	28 Pin
S28214A	Fast Fourier Transformer	NMOS	5V	28 Pin
S28215	Digital Filter/Utility Peripheral	NMOS	5V	28 Pin
S28216	Echo Cancellor Processor	NMOS	5V	28 Pin

FILTER PRODUCTS

S3525A/B	DTMF Bandsplit Filter	CMOS	10.0V to 13.5V	18 Pin
S3526A/B	2600Hz Band-Pass/Notch Filter	CMOS	9V to 13.5V	14 Pin

SPEECH PRODUCTS

S3630A	128K ROM	NMOS	+5V	28 Pin
S3630B	128K ROM	NMOS	+5V	24 Pin
S3610	Speech Synthesizer	CMOS	+6V	24 Pin
S3620	Speech Synthesizer	CMOS	+6V	22 Pin

DTMF TONE GENERATOR

Features

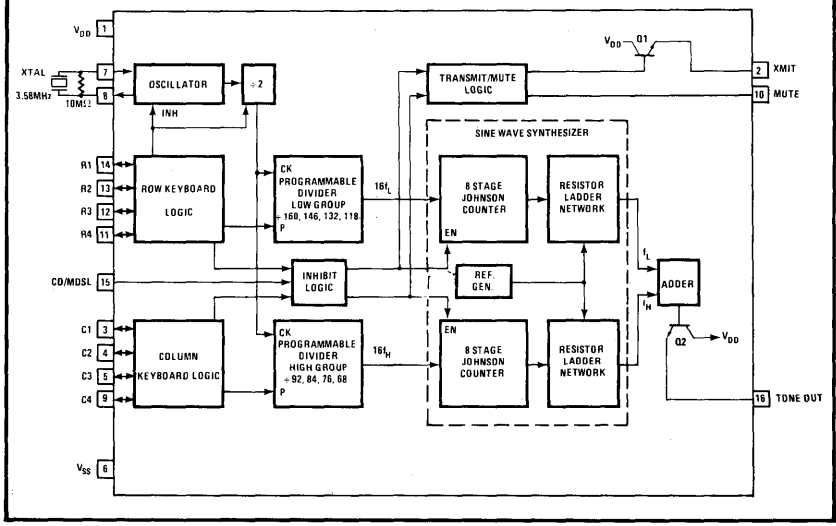
- ☐ **Wide Operating Supply Voltage Range: 3.5 to 13.0 Volts (A, B) 2.75 to 10 Volts (C, D)**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Mute Drivers On Chip**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range**
- ☐ **Dual Tone as Well as Single Tone Capability**
- ☐ **Four Options Available:**

  A:3.5 to 13.0V Mode Select
  B:3.5 to 13.0V Chip Disable
  C: 2.75 to 10V Mode Select
  D: 2.75 to 10V Chip Disable

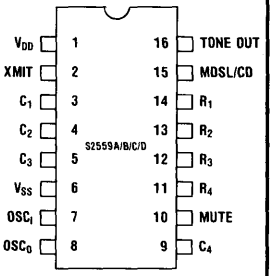
General Description

The S2559 DTMF Tone Genrator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinudsoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

DC Supply Voltage ($V_{DD}-V_{SS}$) S2559 A, B ..... +13.5V
DC Supply Voltage ($V_{DD}-V_{SS}$) S2559 C, D ..... +10.5V
Operating Temperature ..... −25°C to +70°C
Storage Temperature ..... −65°C to +140°C
Power Dissipation at 25°C 500mW
Input Voltage ..... $-0.6 \leq V_{IN} \leq V_{DD}+0.6$

S2559A & B Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			3.5		13.0	V
	Non Tone Out Mode (No Key Depressed)			3.0		13.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.5		0.4	40	μA
			13.0		1.5	130	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.5		0.95	2.9	mA
			13.0		11	33	mA
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	5.0	417	596	789	mVrms
		Row Tone, R_L=240Ω	12.0	378	551	725	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.5−13.0	1.75	2.54	3.75	dB
%DIS	Distortion*		3.5−13.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	(I_{OH}=15mA)	3.5	2.0	2.3		V
		(I_{OH}=50mA)	13.0	12.0	12.3		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		13.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		3.5		0	0.4	V
			13.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		3.5	3.0	3.5		V
			13.0	13.0	13.5		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.5	0.66	1.7		mA
			13.0	3.0	8.0		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.5	0.18	0.46		mA
		V_{OH}=9.5V	13.0	0.78	1.9		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current One Key Selected	V_{OL}=0.5V	3.5	0.26	0.65		mA
		V_{OL}=0.5V	13.0	1.2	3.1		mA
I_{OH}	Output Source Current One Key Selected	V_{OH}=2.5V	3.5	0.14	0.34		mA
		V_{OH}=9.5V	13.0	0.55	1.4		mA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

S2559A & B Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	V_{IL}=13.0V	13.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH}=0.0V	13.0			1.0	μA
I_{IL}	Sink Current	V_{IL}=0.5V	3.5	24	93		μA
	No Key Selected	V_{IL}=0.5V	13.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		3	6	mS
			13.0		0.8	1.6	mS
$C_{I/O}$	Input/Output Capacitance				12	16	pF
					10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL}=3.5V (Pull-down)	3.5	7	17		μA
		Sink Current V_{IL}=13.0V (Pull-down)	13.0	150	400		μA
I_{IH}		Source Current, V_{IH}=3.0V (Pull-up)	3.5	90	230		μA
		Source Current, V_{IH}=12.5V (Pull-up)	13.0	370	960		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH}=0.0V (Pull-up)	3.5	1.5	3.6		μA
		Source Current, V_{IH}=0.0V (Pull-up)	13.0	23	74		μA
I_{IL}	Chip Disable Input (S2559D)	Source Current, V_{IL}=3.5V (Pull-down)	3.5	4	10		μA
		Sink Current, V_{IL}=13.0V (Pull-down)	13.0	90	240		μA

S2559C & D Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.75		10.0	V
	Non Tone Out Mode (No Key Depressed)			2.5		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8	16.0	mA
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage		3.5	250	362	474	mVrms
		Row Tone, R_L=390Ω	5.0	367	546	739	mVrms
		Row Tone, R_L=240Ω	10.0	350	580	730	mVrms

S2559C & D Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
dB_{CR}	Ratio of Column to Row Tone		3.0−10.0	1.75	2.54	3.75	dB
%DIS	Distortion*		3.0−10.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High	(I_{OH}=15mA)	3.0	1.5	1.8		V
	(No Key Depressed)(Pin 2)	(I_{OH}=50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low,		2.75		0	0.5	V
	(No Key Depressed), No Load		10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High,		2.75	2.5	2.75		V
	(One Key Depressed) No Load		10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.0	0.17	0.41		mA
		V_{OH}=9.5V	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current	V_{OL}=0.5V	3.0	0.21	0.52		mA
	One Key Selected	V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current	V_{OH}=2.5V	3.0	0.13	0.31		mA
	One Key Selected	V_{OH}=9.5V	10.0	0.42	1.1		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	V_{IL}=10.0V	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH}=0.0V	10.0			1.0	μA
I_{IL}	Sink Current	V_{IL}=0.5V	3.0	24	93		μA
	No Key Selected	V_{IL}=0.5V	10.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		2	5	mS
			10.0		0.25	4	mS
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL}=3.0V (Pull-down)	3.0		16		μA
		Sink Current V_{IL}=10.0V (Pull-down)	10.0		24		μA
I_{IH}		Source Current, V_{IH}=2.5V (Pull-up)	3.0		210		μA
		Source Current, V_{IH}=9.5V (Pull-up)	10.0		740		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH}=0.0V (Pull-up)	3.0	1.4	3.3		μA
		Source Current, V_{IH}=3.0V (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559D)	Source Current, V_{IL}=3.0V (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, V_{IL}=10.0V (Pull-down)	10.0	55	143		μA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	−0.32
C3	1,477	1,471.9	−0.35
C4	1,633	1,645.0	+0.73

NOTE: % Error does not include oscillator drift.

Table 2. XMIT and MUTE Output Functional Relationship

OUTPUT	'DIGIT' KEY RELEASED	'DIGIT' KEY DEPRESSED	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

COMMUNICATIONS

Circuit Description

The S2559 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the DTMF Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2559 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2559 takes into account these considerations.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Keyboard Interface

The S2559 employs a calculator type scanning circuitry to determine key closures. When no key is depressed, active pull-down resistors are "on" on the row inputs and active pull-up resistors are "on" on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull-up or pull-down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The advantage of the scanning technique is that a keyboard arrangement of SPST switches are shown in Figure 2 without the need for a common line, can be used. Conventional telephone push button keyboards as shown in Figure 1 or X-Y keyboards with common can also be used. The common line of these keyboards can be left unconnected or wired "high".

Logic Interface

The S2559 can also interface with CMOS logic outputs directly. The S2559 requires active "High" logic levels. Since the active pull-up resistors present in the S2559 are fairly low value (500Ω typ), diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their "Low" state.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD} - V_{REF}$) of the stairstep function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones.

Figure 1. Standard Telephone Push Button Keyboard

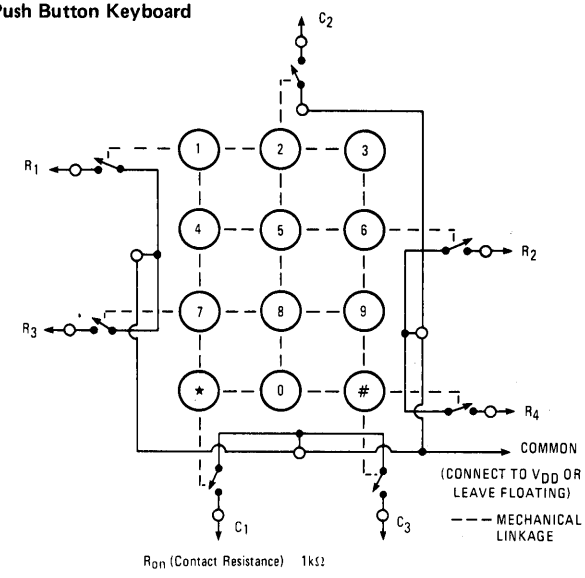


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format

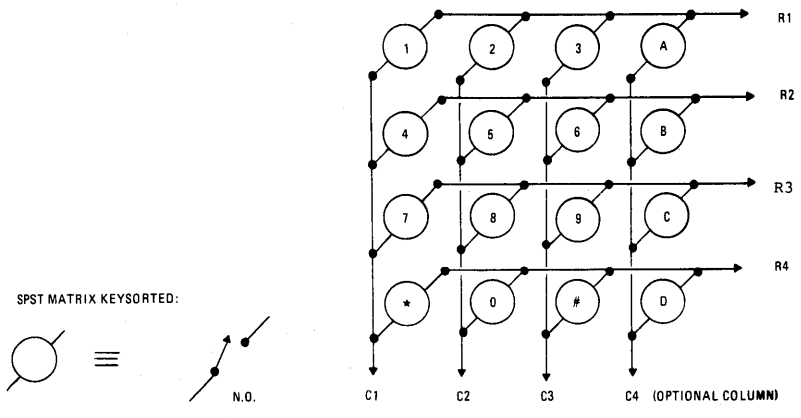
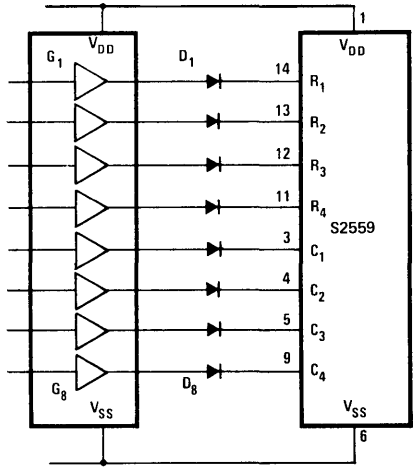
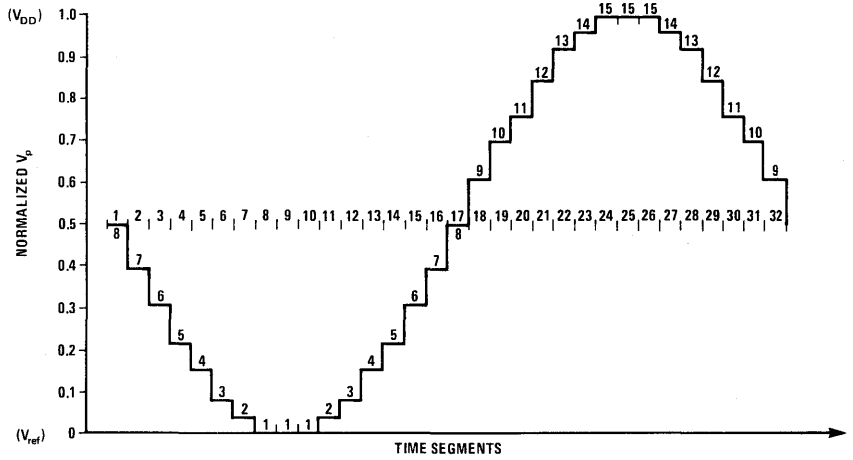


Figure 3. Logic Interface for Keyboard Inputs of the S2559



G1 THRU G8 ANY TYPE CMOS GATE
D1 THRU D8 DIODES TYPE IN914 (OPTIONAL)

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a bipolar NPN transistor connected as emitter follower to allow proper impedance transformation, at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by activating the appropriate row input or by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Mode Select

S2559A and S2559C have a Mode Select (MDSL) input (Pin 15). When MDSL is left floating (unconnected) or connected to V_{DD}, both the dual tone and single tone modes are available. If MDSL is connected to V_{SS}, the single tone mode is disabled and no output tone is produced if an attempt for single tone is made. The S2559B and S2559D do not have the Mode Select option.

Chip Disable

The S2559B and S2559D have a Chip Disable input at Pin 15 instead of the Mode Select input. The chip disable for the S2559B and S2559D is active "high." When the chip disable is active, the tone output goes to V_{SS}, the row, column inputs go into a high impedance state, the oscillator is inhibited and the MUTE and XMIT outputs go into active states. The effect is the device essentially disconnects from the keyboard. This allows one keyboard to be shared among several devices.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%
$R_S \leqslant 100\Omega$, L_M = 96MHY
C_M = 0.02pF C_h = 5pF

MUTE, XMIT Outputs

The S2559 A, B, C, D have a CMOS buffer for the MUTE output and a bipolar NPN transistor for the XMIT output. With no keys depressed, the MUTE output is "low" and the XMIT output is in the active state so that substantial current can be sourced to a load. When a key is depressed, the MUTE output goes high, while the XMIT output goes into a high impedance state. When Chip Disable is "high" the MUTE output is forced "low" and the XMIT output is in active state regardless of the state of the keyboard inputs.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the Digital Tone Generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the Tone Output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 5 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 5 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 5KΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3581A) and amplitudes at the selected frequencies can be noted. This measurment also permits verification of the preemphasis between the individual frequency tones.

Distortion is defined as "the ratio of the *total* power of all extraneous frequencies in the *voiceband* above 500Hz accompanying the signal to the power of the frequency *pair*." This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_n)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

where (V_1) ... (V_n) are extraneous frequency (i.e., intermodulation and harmonic) components in the 500Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$DIST_{dB} = 20 \log \frac{\sqrt{(V_1)^2+(V_2)^2+..(V_n)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\{\log[(V_1)^2+..(V_n)^2] - \log[(V_L)^2+(V_H)^2]\} \ldots (1)$$

An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from a S2559D device operating from a fixed supply of 4Vdc and R_L = 10kΩ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be −30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of -28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of −30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the 2559 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: *Bell System Communications Technical Reference, PUB 47001,* "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment," August 1976.

Figure 5. Test Circuit for Distortion Measurement

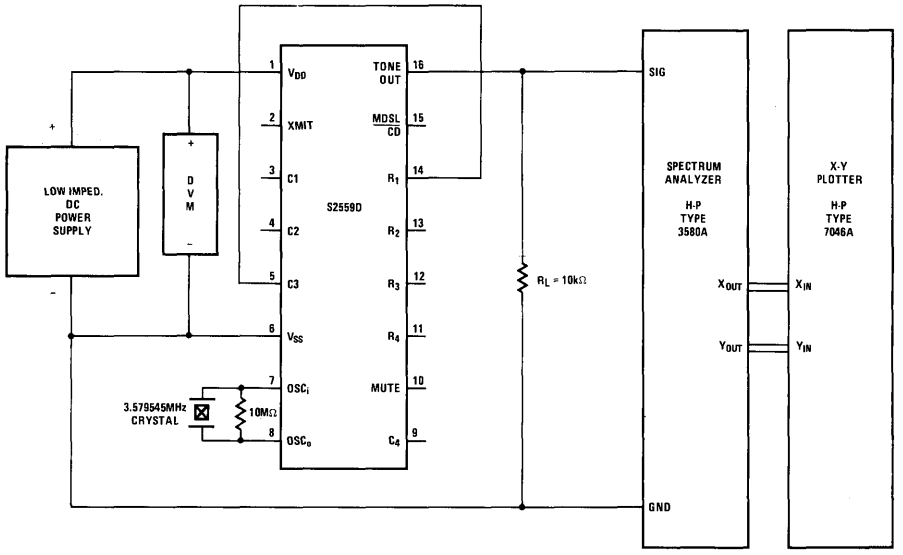
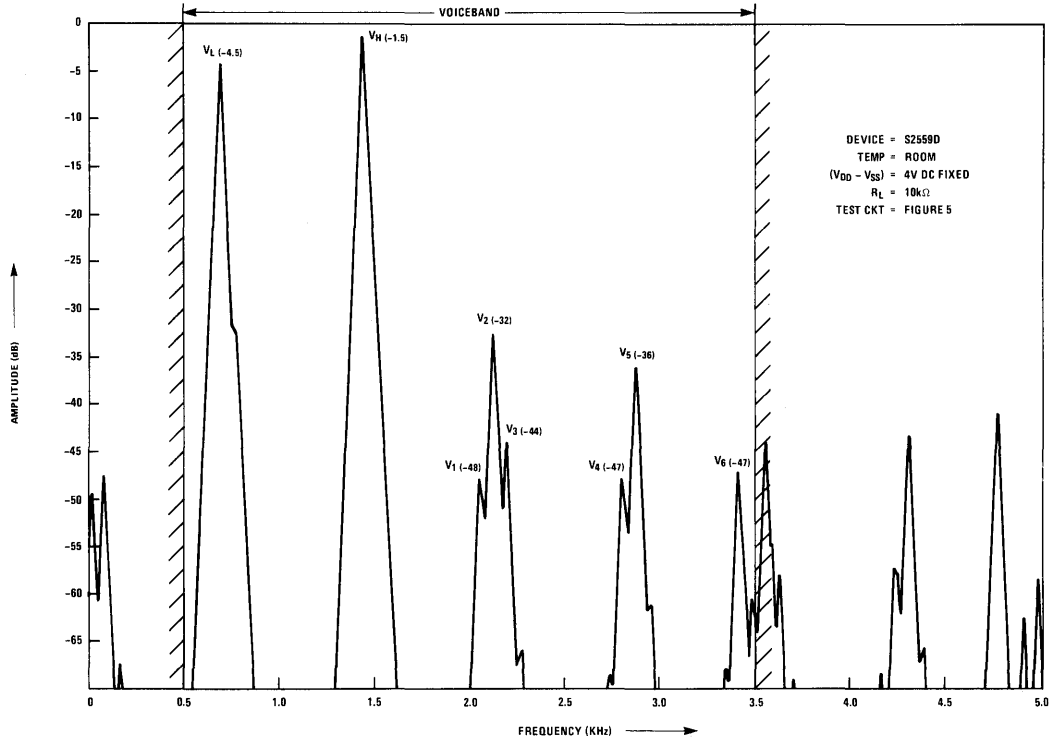


Figure 6. A Typical Spectrum Plot



DTMF TONE GENERATOR

Features

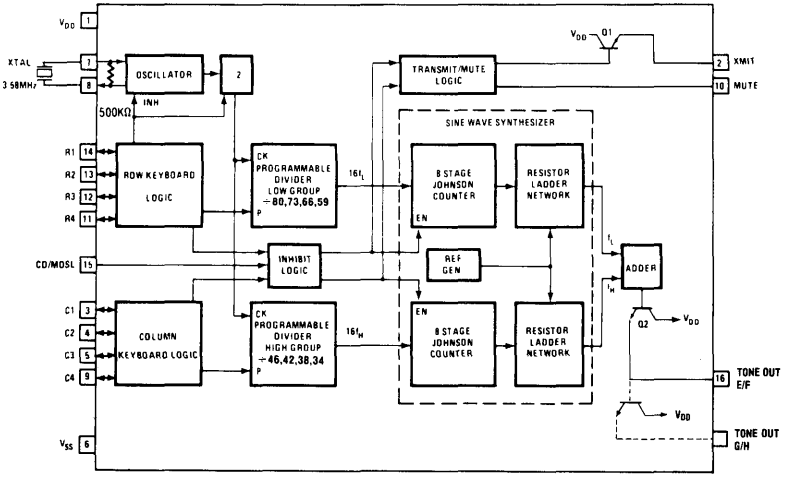
- ☐ Low Output Tone Distortion: 7%
- ☐ Wide Operating Supply Voltage Range: 2.5 to 10 Volts
- ☐ Oscillator Bias Resistor On-Chip
- ☐ Can be Powered Directly from Telephone Line or from Small Batteries
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ Four Options Available on Pin 15:
  - Bipolar Output
    - E: Mode Select
    - F: Chip Disable
  - Darlington Output
    - G: Mode Select
    - H: Chip Disable

General Description

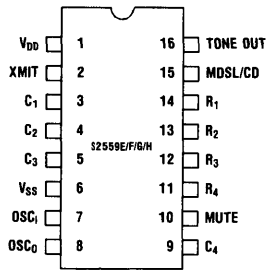
The S2559E, F, G and H are improved members of the S2559 Tone Generator Family. The new devices feature extended operating voltage range, lower tone distortion, and an on-chip oscillator bias resistor. The S2559E and F are pin and functionally compatible with the S2559C and D, respectively.

The S2559 G and H are identical to the E and F, except that there is a Darlington amplifier configuration on the tone out pin, rather than a single bipolar transistor as shown in the block diagram. In many applications this eliminates the need for a transistor in the telephone circuit. Tone distortion in the telephone is also likely to be lower.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

DC Supply Voltage (V_{DD}-V_{SS}) ..... +10.5V
Operating Temperature ..... −25°C to +70°C
Storage Temperature ..... −30°C to +125°C
Power Dissipation at 25°C 1000mW
Digital Input ..... $V_{SS}-0.3 \leq V_{IN} \leq V_{DD}+0.3$
Analog Input ..... $V_{SS}-0.3 \leq V_{IN} \leq V_{DD}+0.3$

S2559E, F, G and H Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.5		10.0	V
	Non Tone Out Mode (No Key Depressed)			1.6		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8	16.0	mA
	Tone Output						
S2559E/F V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	3.5	335	465	565	mVrms
			5.0	380	540	710	mVrms
		Row Tone, R_L=240Ω	10.0	380	550	735	mVrms
S2559G/H V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	3.5	110	315	495	mVrms
			5.0	340	540	675	mVrms
		Row Tone, R_L=240Ω	10.0	415	590	770	mVrms
dB_{CR}	Ratio of column to Row Tone (Dual Tone Mode)		3.5−10.0	1.0	2.0	3.0	dB
%DIS	Distortion*	2559E/F	3.5−10.0			7	%
		2559G/H	4.0−10.0			7	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	(I_{OH}=15mA)	3.0	1.5	1.8		V
		(I_{OH}=50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		2.75		0	0.5	V
			10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		2.75	2.5	2.75		V
			10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.0	0.17	0.41		mA
		V_{OH}=9.5V	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current One Key Selected	V_{OL}=0.5V	3.0	0.21	0.52		mA
		V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current One Key Selected	V_{OH}=2.5V	3.0	0.13	0.31		mA
		V_{OH}=9.5V	10.0	0.42	1.1		mA

**Distortion is defined as "the ratio of the total power of all extraneous frequencies, in the VOICE and above 500Hz, to the total power of the DTMF frequency pair".*

S2559E, F, G and H Electrical Characteristics (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Oscillator Input/Output						
I_{OL}	Output Sink Current	V_{OL}=0.5V	3.0	0.21	0.52		mA
	One Key Selected	V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current	V_{OH}=2.5V	3.0	0.13	0.31		mA
	One Key Selected	V_{OH}=9.5V	10.0	0.42	1.1		mA
t_{START}	Oscillator Startup Time		3.5		2	5	ms
			10.0		0.25	4	ms
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, VIL=3.0V (Pull-down)	3.0		16		μA
		Sink Current, VIL=10.0V (Pull-down)	10.0		24		μA
I_{IH}		Source Current, VIH=2.5V (Pull-up)	3.0		210		μA
		Source Current, VIH=9.5V (Pull-up)	10.0		740		μA
I_{IH}	Mode Select Input (S2559E,G)	Source Current, VIH=0.0V (Pull-up)	3.0	1.4	3.3		μA
		Source Current, VIH=3.0V (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559F,H)	Source Current, VIL=3.0V (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, VIL=10.0V (Pull-down)	10.0	55	143		μA

COMMUNICATIONS

DTMF TONE GENERATOR

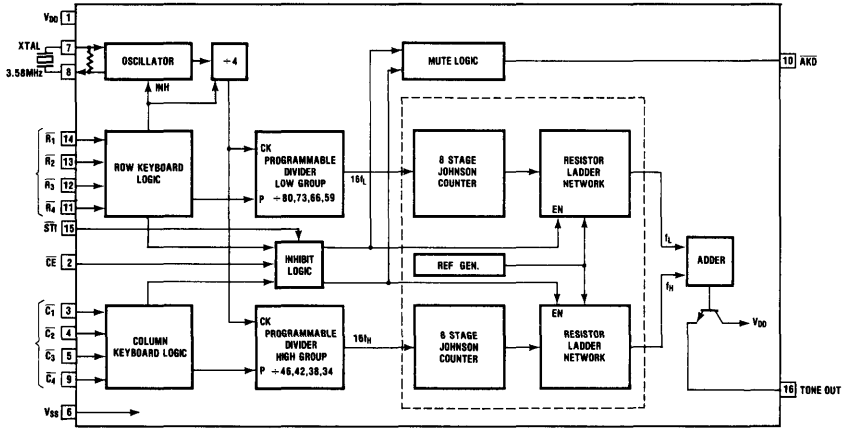
Features

- ☐ Wide Operating Voltage Range: 2.5 to 10 Volts
- ☐ Optimized for Constant Operating Supply Voltages, Typically 3.5V
- ☐ Tone Amplitude Stability is Within ±1.5dB of Nominal Over Operating Temperature Range
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly From the Telephone Lines or From Small Batteries
- ☐ Uses TV Crystal Standard (3.58MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability
- ☐ Specifically Designed for Electronic Telephone Applications
- ☐ Interfaces Directly to a Standard Telephone Push-Button Keyboard With Common Terminal
- ☐ Low Total Harmonic Distortion
- ☐ Dual Tone as Well as Single Tone Capability
- ☐ Direct Replacement for Mostek MK5089 Tone Generator

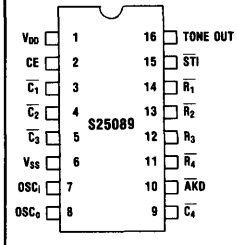
General Description

The S25089 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD}-V_{SS})	+10.5V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6 \le V_{IN} \le V_{DD}$ +0.6
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.5	—	10.0	V
	Non Tone Out Mode ($\overline{AKD}$ Outputs toggle with key depressed)			1.6	—	10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)		3.0 10.0	— —	1 5	20 100	μA μA
	Operating (One Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)		3.0 10.0	— —	.9 4.5	1.25 10.0	mA mA
	Tone Output						
V_{OR}	Dual Tone Mode Output	Row Tone	R_L=10kΩ R_L=100kΩ	3.0 3.5	−11.0 −10.0		−8.0 −7.0	dBm dBm
dB_{CR}	Ratio of Column to Row Tone			2.5-10.0	2.4	2.7	3.0	dB
%DIS	Distortion*			2.5-10.0	—	—	10	%
NKD	Tone Output—No Key Down						−80	dBm
	$\overline{AKD}$ Output							
I_{OL}	Output On Sink Current		V_{OL}=0.5V	3.0	0.5	1.0	—	mA
I_{OH}	Output Off Leakage Current			10.00		1	10	μA
	OSCILLATOR Input/Output							
I_{OL}	One Key Selected		V_{OL}=0.5V	3.0	0.21	0.52	—	mA
	Output Sink Current		V_{OL}=0.5V	10.0	0.80	2.1	—	mA
I_{OH}	Output Source Current		V_{OH}=2.5V	3.0	0.13	0.31	—	mA
	One Key Selected		V_{OH}=9.5V	10.0	0.42	1.1	—	mA

*Distortion measured in accordance with the specifications described in REF. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output (Continued)						
t_{START}	Oscillator Startup Time with Crystal as Specified		3.0-10.0	—	2	5	ms
$C_{I/O}$	Input/Output Capacitance		3.0 10.0	— —	12 10	16 14	pF pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		—	V_{SS}		.2(V_{DD} −V_{SS})	V
V_{IH}	Input Voltage, High		—	.8(V_{DD} −V_{SS})	—	V_{DD}	V
I_{IH}	Input Current	V_{IH}=0.0V	3.0	30	90	150	μA
	(Pull up)	V_{IH}=0.0V	10.0	100	300	500	μA

Oscillator

The S25089 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_0 terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 4 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%
R_S 100Ω, L_M=96mH
C_M=0.02pF C_H=5pF C_L=12pF

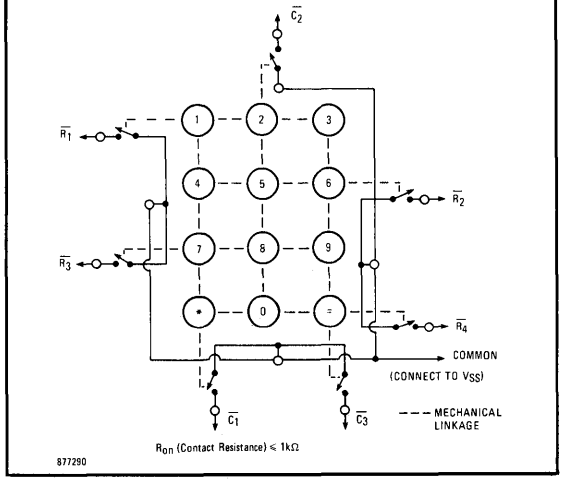
Keyboard Interface

The S25089 can interface with the standard telephone pushbutton keyboard (see Figure 1) with common. The common of the keyboard must be connected to V_{SS}.

Logic Interface

The S25089 can also interface with CMOS logic outputs directly (see Figure 2). The S25089 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 20kΩ -100kΩ.

Figure 1. Standard Telephone Push Button Keyboard



Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group

frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divided by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD}-V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected, dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys that are not either in the same row or in the same column are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Inhibiting Single Tones

The $\overline{STI}$ input (pin 15) is used to inhibit the generation of other than dual tones. It has an internal pull down to V_{SS} supply. When this input is left unconnected or connected to V_{SS}, single tone generation as described in the preceding paragraph (Single Tone Mode) is suppressed with all other functions operating normally. When this input is connected to V_{DD} supply, single or dual tones may be generated as previously described (Single Tone Mode, Dual Tone Mode).

Chip Enable Input (CE, Pin 2)

The chip enable input has an internal pull-up to V_{DD} supply. When this pin is left unconnected or connected to V_{DD} supply the chip operates normally. When connected to V_{SS} supply, tone generation is inhibited. All other chip functions operate normally.

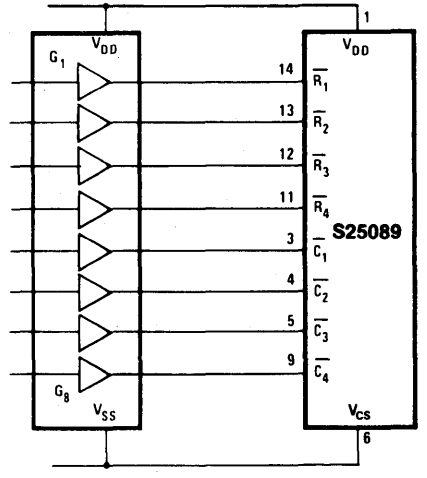
COMMUNICATIONS

Table 1. Comparison of Specified Vs. Actual Tone Frequencies Generated by S25089

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

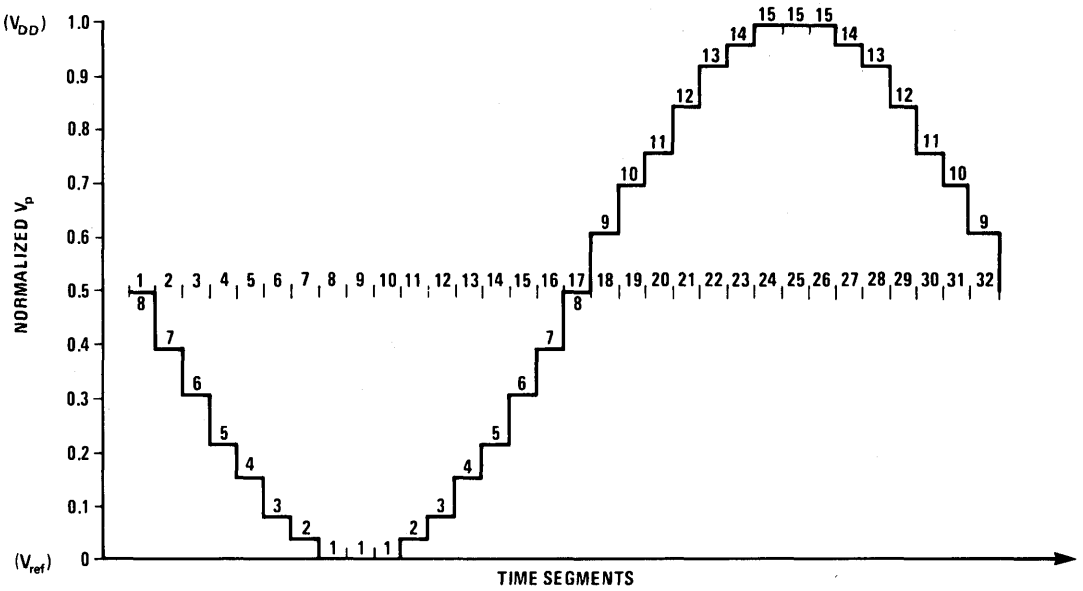
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S25089



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S25089 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of (V_{DD} - V_{REF}), increases with supply voltage (Figure 5).
b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ±1.0dB over nominal.
c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

$\overline{AKD}$ (Any Key Down or Mute) Output

The $\overline{AKD}$ output (pin 10) consists of an open drain N channel device (see Figure 6.) When no key is depressed the $\overline{AKD}$ output is open. When a key is depressed the $\overline{AKD}$ output goes to V_{SS}. The device is large enough to sink a minimum of 500μA with voltage drop of 0.2V at a supply voltage of 3.5V.

Figure 4. Structure of the Reference Voltage

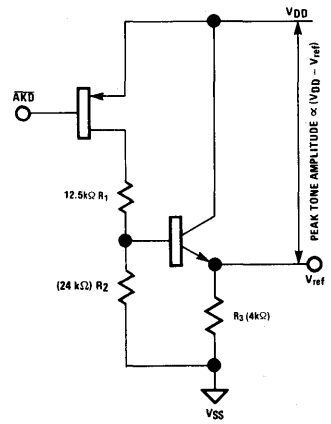


Figure 5. Typical Single Tone Output Amplitude Vs Supply Voltage (R_L =10k)

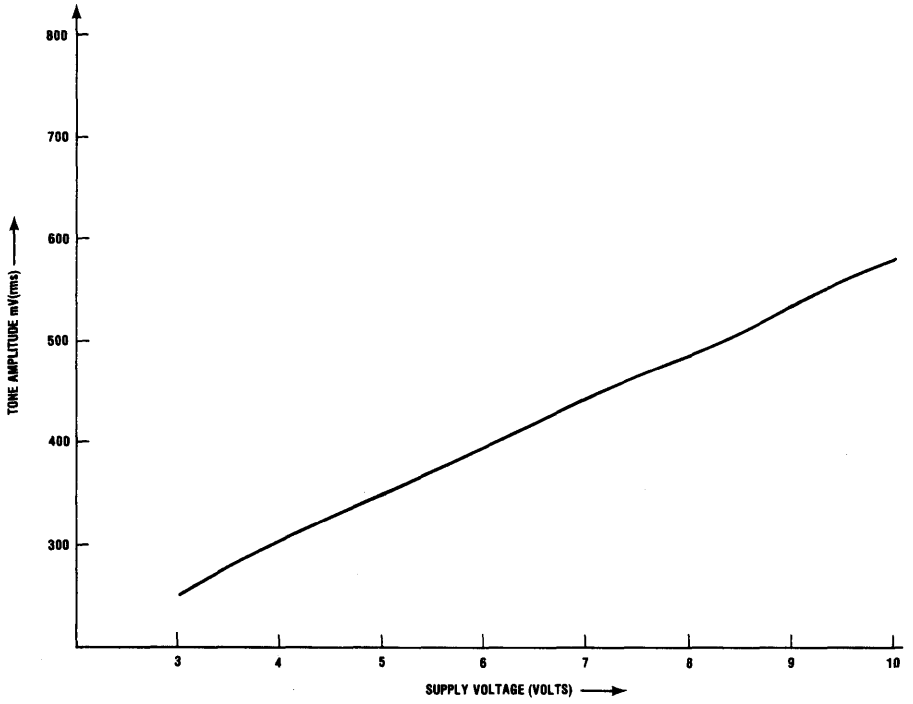
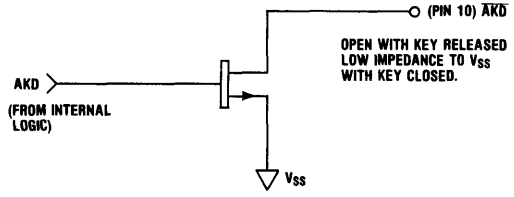


Figure 6. $\overline{AKD}$ Output Structure



AMERICAN MICROSYSTEMS, INC.

S2859

DTMF TONE GENERATOR

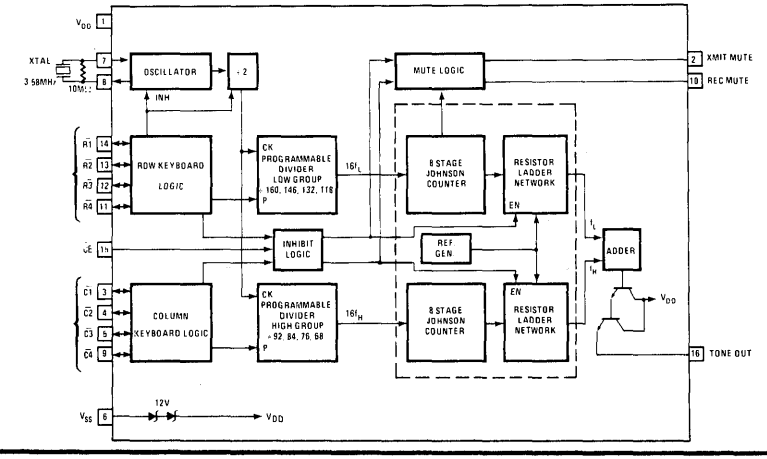
Features

- ☐ **Wide Operating Supply Voltage Range: 3.0 to 10 Volts**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Timing Sequence for XMIT, REC MUTE Outputs**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range**
- ☐ **Dual Tone as Well as Single Tone Capability**
- ☐ **Darlington Configuration Tone Output**

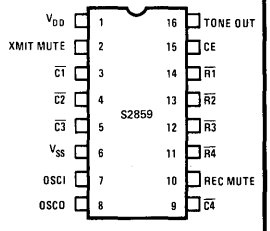
General Description

The S2859 DTMF Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2859 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, point-of-sale, and credit card verification terminals and process control.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD}-V_{SS}$)	+10.5V
Operating Temperature	−25 °C to +70 °C
Storage Temperature	−55 °C to +125 °C
Power Dissipation at 25 °C	500mW
Input Voltage	$-0.6 \leq V_{IN} \leq V_{DD}+0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −25 °C to 70 °C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				3.0	—	10.0	V
	Non Tone Out Mode (Mute Outputs Toggle With Key Depressed)				2.2	—	10.0	V
V_Z	Internal Zener Diode Voltage, I_Z = 5mA			—	—	12.0	—	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and Mute Outputs Unloaded)			3.0 10.0	— —	0.001 0.003	0.3 1.0	mA mA
	Operating (One Key Selected, Tone and Mute Outputs Unloaded)			3.0 10.0	— —	1.3 11	2.0 18	mA mA
	Tone Output							
V_{OR}	Single Tone	Row	R_L=100Ω	5.0	366	462	581	mVrms
	Mode Output Voltage	Tone	R_L=100Ω	10.0	370	482	661	mVrms
dB_{CR}	Ratio of Column to Row Tone			3.0−10.0	1.0	2.0	3.0	dB
%DIS	Distortion*			3.0−10.0	—	—	10	%
	REC, XMIT MUTE Outputs							
I_{OH}	Output Source Current		V_{OH}=1.2V	2.2	0.43	1.1	—	mA
			V_{OH}=2.5V	3.0	1.3	3.1	—	mA
			V_{OH}=9.5V	10.0	4.3	11	—	mA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

the MUTE outputs are open. When a key is depressed, the MUTE outputs go high. When chip enable is "Low" the MUTE outputs are forced in the "open" state regardless of the state of the keyboard.

Timing Sequence

Figure 4 illustrates the sequence in which the MUTE outputs operate when a key is depressed and released. When a valid key is depressed the REC MUTE output goes high first. The XMIT MUTE output goes high after a delay of about 1.6ms. This allows the receiver to be muted prior to the muting of the transmitter and generation of the dual tone. This prevents an undesirable click to be heard in the earpiece due to the momentary interruption of the direct current flowing through the network during the transition time when the transmitter is disconnected and dual tone applied. On release of the key the XMIT MUTE output goes open first, simultaneously the dual tone output is removed. The receiver at this time is still muted so that the click due to the momentary interruption of the direct current during the release of the key is not heard at the earpiece. The REC MUTE output goes open after a delay of about 1.7ms which reconnects the receiver to the network. The leading and trailing edge delays are guaranteed for supply voltages exceeding 3.0 volts. Below 3.0 volts the REC, XMIT MUTE outputs and tone output coincide with each other.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the digital tone generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the tone output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 4 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 4 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 1KΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3580A) and amplitudes at the selected frequencies can be noted. This measurement also permits verification of the pre-emphasis between the individual frequency tones.

Distortion is defined as "the ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the power of the frequency pair". This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_N)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

where $(V_1) \ldots (V_N)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500 Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$\text{DIST}_{dB} = 20 \log \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_N)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\{\log[(V_1{}^2+\ldots(V_N)^2] - \log[(V_L)^2+(V_H)^2]\} \ldots (1)$$

Table 2. Truth Table

INPUTS				OUTPUTS		
KEYS DEPRESSED	NUMBER OF COLUMNS LOW	NUMBER OF ROWS LOW	CHIP ENABLE	TONE	REC MUTE	XMIT MUTE
X	X	X	0	0	OPEN	OPEN
NONE	0	0	1	0	OPEN	OPEN
ONE	1	1	1	R+C	1	1
TWO OR MORE KEYS IN COLUMN	1	2 OR 3 OR 4	1	C	1	1
TWO OR MORE KEYS IN ROW	2 OR 3 OR 4	1	1	R	1	1
MULTI KEY	OTHER COMBINATIONS	OTHER COMBINATIONS	1	0	OPEN	OPEN
NOTE 1	4	3	1	R+C	A	B

X DON'T CARE A: 16 (ROW FREQ) B: 16 (COL FREQ)

NOTE 1: THIS MODE IS USED FOR TEST PURPOSES ONLY. IT IS INITIATED BY CONNECTING ALL COLUMN INPUTS AND THREE OUT OF FOUR ROW INPUTS TO V_{SS}. THE ROW INPUT THAT IS CONNECTED TO V_{DD} ROUTES THE CORRESPONDING 16 TIMES ROW FREQUENCY TO THE REC MUTE OUTPUT AND THE APPROPRIATE 16 TIMES COLUMN FREQUENCY (i.e., R_1 SELECTS C_1 etc.) TO THE XMIT MUTE OUTPUT.

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD} – V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output						
I_{OL}	One Key Selected	V_{OL} = 0.5V	3.0	0.21	0.52	–	mA
	Output Sink Current	V_{OL} = 0.5V	10.0	0.80	2.1	–	mA
I_{OH}	Output Source Current	V_{OH} = 2.5V	3.0	0.13	0.31	–	mA
	One Key Selected	V_{OH} = 9.5V	10.0	0.42	1.1	–	mA
I_{IL}	Input Current Leakage Sink Current One Key Selected	V_{IL} = 10.0V	10.0	–	–	1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH} = 0.0V	10.0	–	–	1.0	μA
I_{IL}	Sink Current	V_{IL} = 0.5V	3.0	24	58	–	μA
	No Key Selected	V_{IL} = 0.5V	10.0	27	66	–	μA
t_{START}	Oscillator Time		3.0 10.0	– –	2 0.25	5 0.75	ms ms
$C_{I/O}$	Input/Output Capacitance		3.0 10.0	– –	12 10	16 14	pF pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		3.0 10.0	– –	– –	0.75 3.0	V V
V_{IH}	Input Voltage, High		3.0 10.0	2.4 7.0		– –	V V
I_{IH}	Input Current	V_{IH} = 0.0V	3.0	20	60	100	μA
	(Pull up)	V_{IH} = 0.0V	10.0	66	200	336	μA

Circuit Description

The S2859 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the Digital Tone Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2859 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2859 takes into account these considerations.

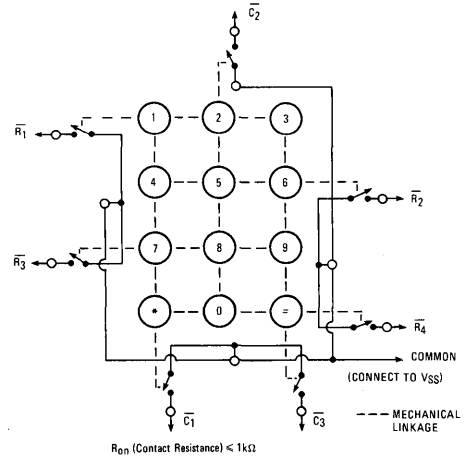
Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Keyboard Interface

The S2859 can interface with either the standard telephone pushbutton keyboard (see Figure 1) or an X-Y keyboard with common. The common of the keyboard must be connected to V_{SS}.

Figure 1. Standard Telephone Push Button Keyboard



Logic Interface

The S2859 can also interface with CMOS logic ouputs directly. (See Figure 2.) The S2859 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 33kΩ — 150kΩ.

Tone Generation

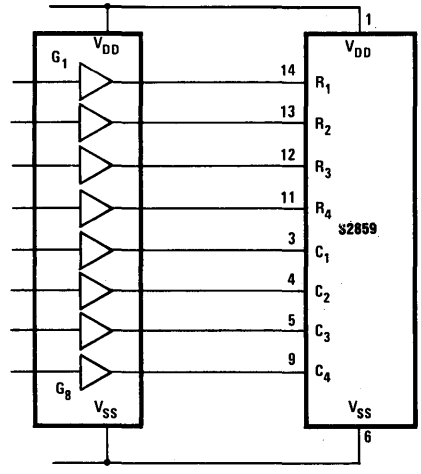
When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP ($V_{DD} - V_{REF}$) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

Table 1. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2859

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

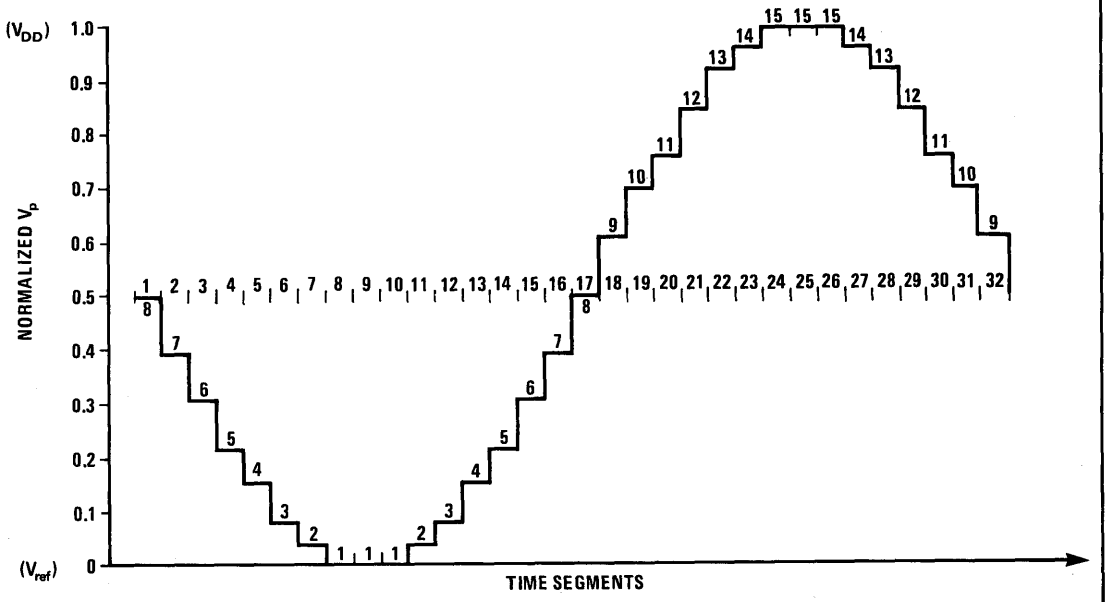
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S2859



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a Darlington NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Chip Enable

The S2859 has a chip enable input at pin 15. The chip enable for the S2859 is active "High". When the chip enable is "Low", the tone output goes to V_{SS}, the oscillator is inhibited and the MUTE outputs go into an open state.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3,579545MHz ±0.02%

R_S 100Ω, L_M=96MHy

C_M=0.02pF C_H=5pF C_L=12pF

MUTE Outputs

The S2859 has P-Channel buffers for the REC MUTE and XMIT MUTE outputs. With no keys depressed

Figure 4. Timing Diagram for (V_{DD}-V_{SS})≥3.5V

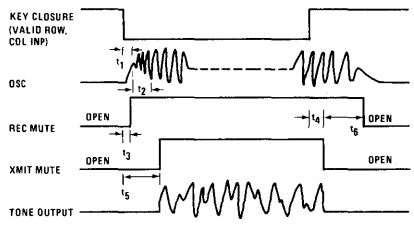
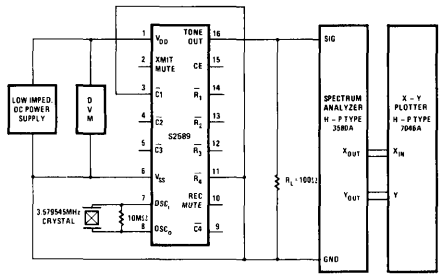


Figure 5. Test Circuit for Distortion Measurement



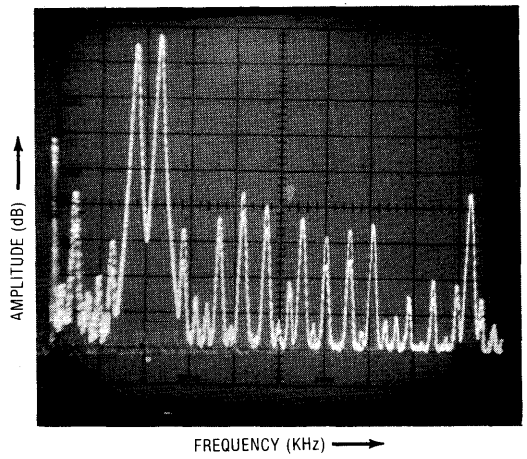
An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from S2859 device operating from a fixed supply of 4VDC and $R_L = 100\Omega$ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be −30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of −28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of −30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the S2859 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: Bell System Communications Technical Reference, PUB 47001, *"Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment,"* August 1976.

Figure 6. A Typical Spectrum Plot



DEVICE: S2859 $R_L = 100\Omega$
TEMP: ROOM TEST CKT: FIGURE 5
$(V_{DD} - V_{SS})$: 4V DC FIXED DUAL TONE: R_4, C_1
HORIZONTAL SCALE = 0.5KHz/DIV
VERTICAL SCALE = 10dB/DIV

DTMF TONE GENERATOR

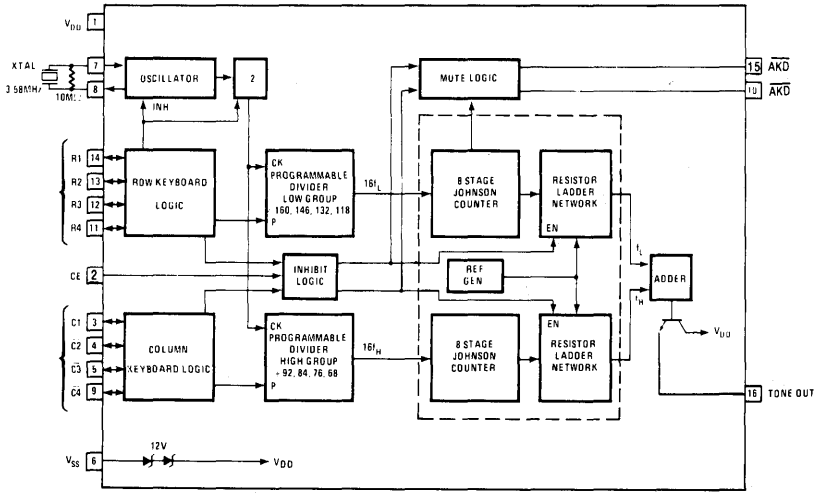
Features

- ☐ **Optimized for Constant Operating Supply Voltages, Typically 3.5V**
- ☐ **Tone Amplitude Stability is Within ±1.3 dB of Nominal Over Operating Temperature Range**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Specifically Designed for Electronic Telephone Applications**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **Dual Tone as Well as Single Tone Capability**

General Description

The S2860 Digital Tone Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration

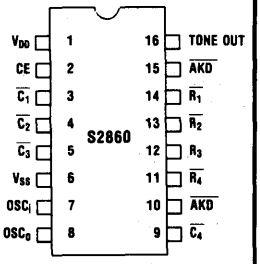
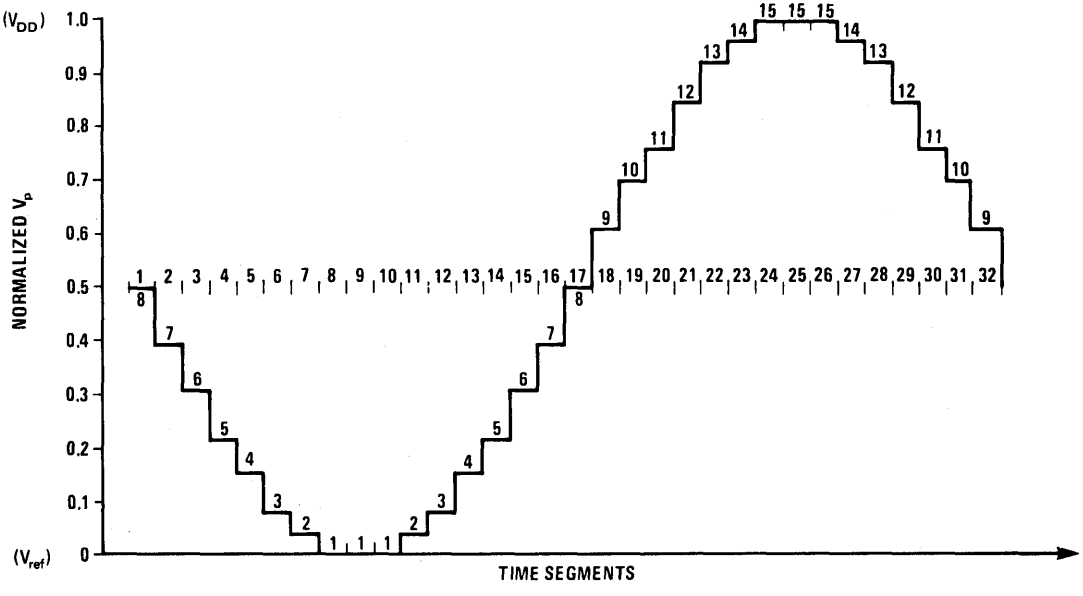


Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S2860 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of ($V_{DD} - V_{REF}$), increases with supply voltage (Figure 5)

b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ±1.3dB over nominal.

c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

AKD (Any Key Down or Mute) Outputs

The AKD outputs (pin 15 and pin 10) are identical and consist of open drain N channel devices (see Figure 6.)

When no key is depressed the AKD outputs are open. When a key is depressed the AKD outputs go to V_{SS}. The devices are large enough to sink a minimum of 100μA with voltage drop of 0.2V at a supply voltage of 3.5V.

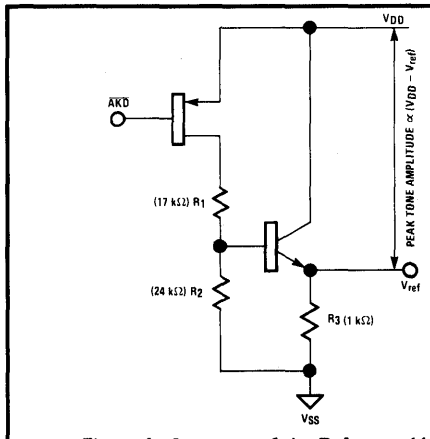


Figure 4. Structure of the Reference Voltage

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD} – V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output (Continued)						
t_{START}	Oscillator Time		3.0 10.0	– –	2 0.25	5 0.75	ms ms
$C_{I/O}$	Input/Output Capacitance		3.0 10.0	– –	12 10	16 14	pF pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		–	$V_{SS}-0.6$		$.2(V_{DD}-V_{SS})$	V
V_{IH}	Input Voltage, High		–	$.8(V_{DD}-V_{SS})$	–	$V_{DD}+0.6$	V
I_{IH}	Input Current	V_{IH} = 0.0V	3.0	20	60	100	μA
	(Pull up)	V_{IH} = 0.0V	10.0	66	200	336	μA

Oscillator

The S2860 contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

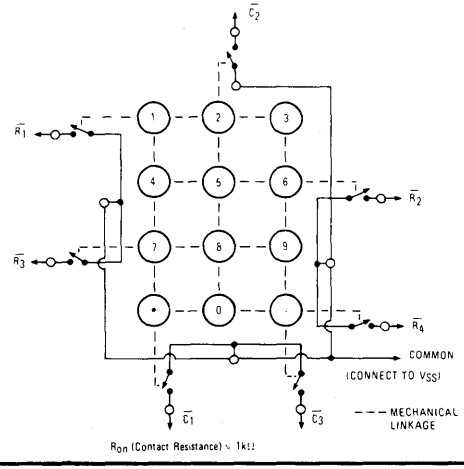
A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3,579545MHz ±0.02%
R_S 100Ω, L_M=96MHy
C_M=0.02pF C_H=5pF C_L=12pF

Keyboard Interface

The S2860 can interface with either the standard telephone pushbutton keyboard (see Figure 1) or an X-Y keyboard with common. The common of the keyboard must be connected to V_{SS}.

Figure 1. Standard Telephone Push Button Keyboard



Logic Interface

The S2860 can also interface with CMOS logic outputs directly. (See Figure 2.) The S2860 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 33kΩ – 150kΩ.

Tone Generation

When a valid key closure is detected, the keyboard logic

Tone Generation (Continued)

programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD} -V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

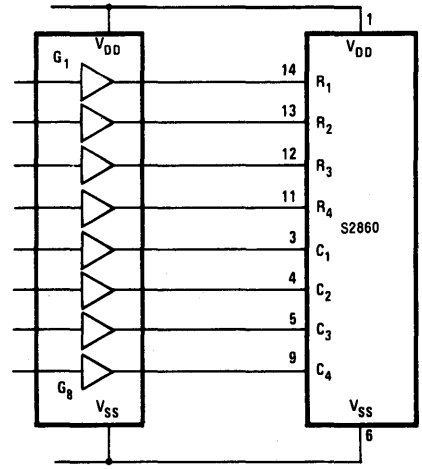
Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Table 1. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2859

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S2860



G1 THRU G8 ANY TYPE CMOS GATE

Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$)	+10.5V
Operating Temperature	−30°C to +70°C
Storage Temperature	−55°C to +125°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −30°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				3.0	–	10.0	V
	Non Tone Out Mode (AKD Outputs toggle with key depressed)				1.8	–		V
V_Z	Internal Zener Diode Voltage, I_Z = 5mA			–	–	12.0	–	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and AKD Outputs Unloaded)			3.5 10.0	– –	1 5	20 100	μA μA
	Operating (One Key Selected, Tone and AKD Outputs Unloaded)			3.5 10.0	– –	.9 3.6	1.25 5	mA mA
	Tone Output							
V_{OR}	Dual Tone	Row	R_L = 10k Ω	3.5	305	350	412	mVrms
	Mode Output	Tone	R_L = 1k Ω	3.5	272	350	412	mVrms
dB_{CR}	Ratio of Column to Row Tone			3.0 – 10.0	1.0	2.0	3.0	dB
%DIS	Distortion			3.0 – 10.0	–	–	10	%
	AKD Outputs							
I_{OH}	Output Sink Current		V_{OL}=.7V	3.5	0.1	1.0	–	mA
	OSCILLATOR Input/Output							
I_{OL}	One Key Selected		V_{OL} = 0.5V	3.0	0.21	0.52	–	mA
	Output Sink Current		V_{OL} = 0.5V	10.0	0.80	2.1	–	mA
I_{OH}	Output Source Current		V_{OH} = 2.5V	3.0	0.13	0.31	–	mA
	One Key Selected		V_{OH} = 9.5V	10.0	0.42	1.1	–	mA
I_{IL}	Input Current Leakage Sink Current One Key Selected		V_{IL} = 10.0V	10.0	–	–	1.0	μA
I_{IH}	Leakage Source Current One Key Selected		V_{IH} = 0.0V	10.0	–	–	1.0	μA
I_{IL}	Sink Current		V_{IL} = 0.5V	3.0	24	58	–	μA
	No Key Selected		V_{IL} = 0.5V	10.0	27	66	–	μA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

Figure 5. Typical Tone Output Amplitude Vs Supply Voltage ($R_L = 10k$)

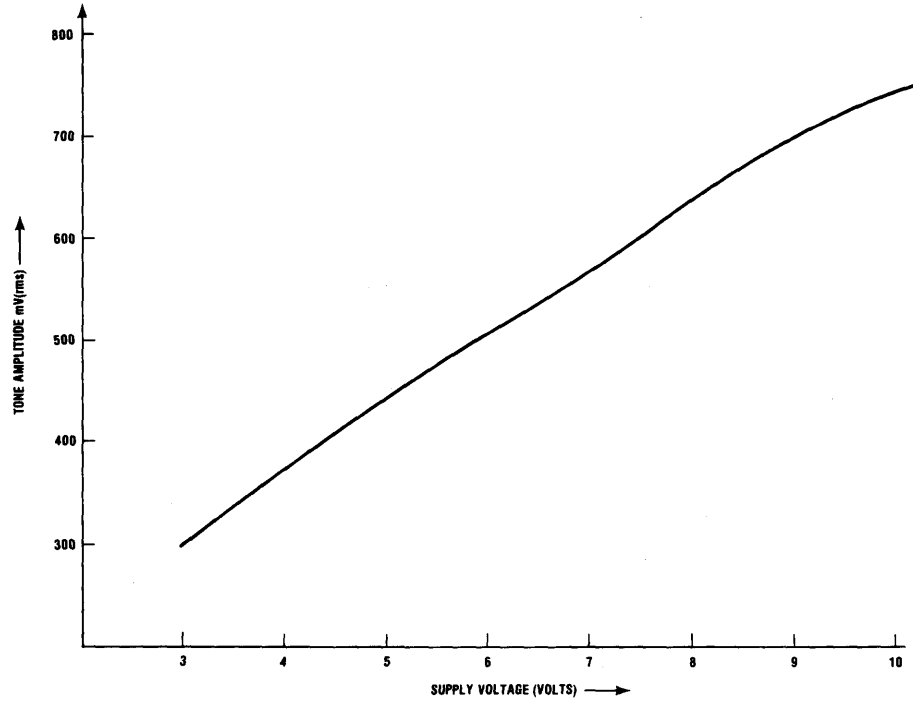
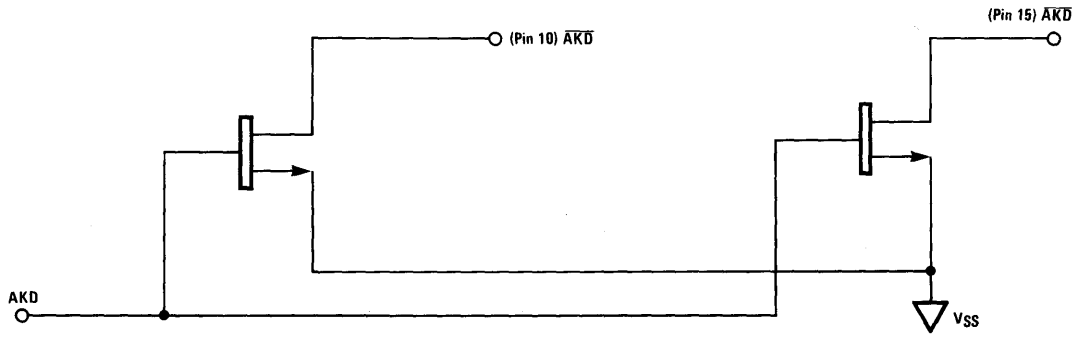


Figure 6. AKD Output Structure



AMERICAN MICROSYSTEMS, INC.

S2560A

PULSE DIALER

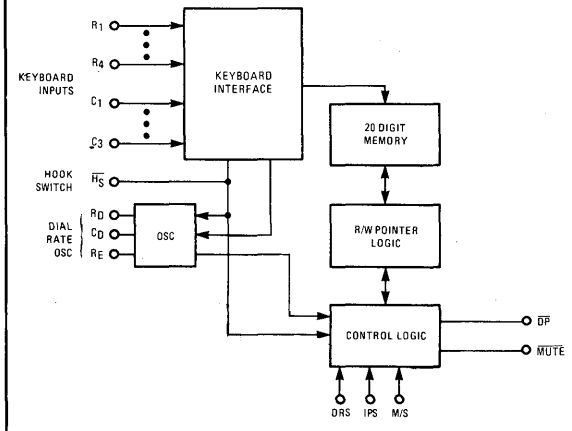
Features

- ☐ **Low Voltage CMOS Process for Direct Operation From Telephone Lines**
- ☐ **Inexpensive R-C Oscillator Design Provides Better than ±5% Accuracy Over Temperature and Unit to Unit Variations**
- ☐ **Dialing Rate Can Be Varied By Changing the Dial Rate Oscillator Frequency**
- ☐ **Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without Changing Oscillator Components**
- ☐ **Two Selections of Mark/Space Ratios (33-1/3/66-2/3 or 40/60)**
- ☐ **Twenty Digit Memory for Input Buffering and for Redial With Access Pause Capability**
- ☐ **Mute and Dial Pulse Drivers on Chip**
- ☐ **Accepts DPCT Keypad with Common Arranged in a 2 of 7 Format; Also Capable of Interface to SPST Switch Matrix**

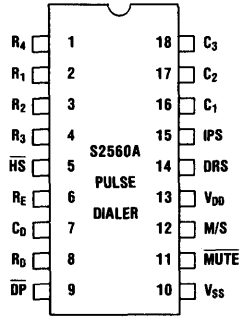
General Description

The S2560A Pulse Dialer is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered. IDP is scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD}$ to $V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	$V_{DD}-V_{SS}$ (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHDP}	$\overline{DP}$ Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	$\overline{MUTE}$ Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHM}	$\overline{MUTE}$ Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low Current (Sink)	1.5	20		µA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High Current (Source)	1.5	20		µA	V_{OUT} = 1V
V_{DR}	Data Retention Voltage		1.0		V	"On Hook" $\overline{HS}$ = V_{DD}. Keyboard open, all other input pins to V_{DD} or V_{SS}
I_{DD}	Quiescent Current	1.0		750	nA	
I_{DD}	Operating Current	1.5 3.5		100 500	µA µA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$ = V_{SS} ("Off Hook") Keyboard processing and dial pulsing at 10 pps at conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leq R_D \leq 750K\Omega$; $100pF \leq C_D^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD}-V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD}-V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded. When power is first applied to the device, the device should be in "On Hook" condition ($\overline{HS}$=1). This is necessary because there is no internal power or reset on chip and for proper operation all internal latches must come up in a known state. In applications where the device is hard wired in "Off Hook" ($\overline{HS}$=0) condition, a momentary "On Hook" condition can be presented to the device during power up by use of a capacitor resistor network as shown in Figure 6.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components: two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10 pps the oscillator should be adjusted to 2400 Hz. Typical values of external components for this are R_D and R_E=750kΩ and C_D=270 pF. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a ±10% tolerance of the dialing rate in the system.

Keyboard Interface (2560A)

The S2560A employs a scanning technique to determine a key closure. This permits interface to a DPCT keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2) and interface to a SPST switch matrix (Figure 7). A high level on the appropriate row and column inputs constitutes a key closure for logic interface. When using a SPST switch matrix, it is necessary to add small capacitors (30 pF) from the column inputs to V_{SS} to insure that the oscillator is shut off after a key is released or after the dialing is complete.

OFF Hook Operation: The device is continuously powered through a 150kΩ resistor during Off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during the pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

ON Hook Operation: The device is continuously powered through a 10—20MΩ resistor during the ON hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20 pps can be achieved. Dialing rates of 7 and 14 pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20 pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14 pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10 pps an IDP of 800ms is obtained and at 20 pps an IDP of 400ms is obtained.

The user can enter a number up to 20 digits long from a standard 3x4 double contact keypad with common (Figure 1). It is also possible to use a logic interface as shown in Figure 2 for number entry. Antibounce protection circuitry is provided on chip (min. 20ms.) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed twenty.

Auto Dialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

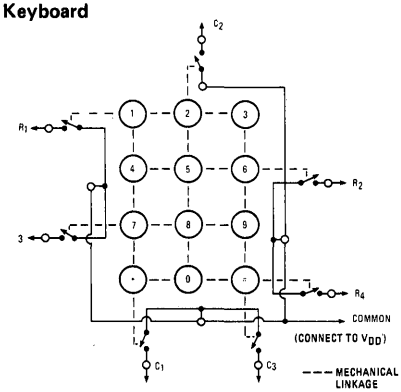
Table 1. S2560A Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 3. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IPS)	1	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceding the first dialed pulse is an inter-digit time equal to the selected IDP. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	1	A programmable line allows selection of two different output rates such as 7 or 14 pps, 10 or 20 pps, etc. See Tables 2 and 3.
Mark/Space (MS)	1	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{\text{MUTE}}$)	1	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.

Table 1. (Continued)

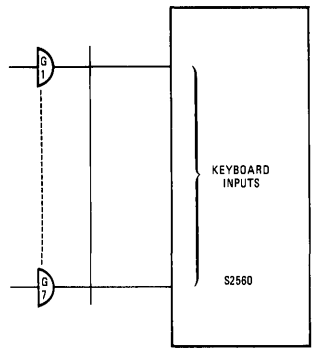
Pin	Number	Function
Dial Pulse Out ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator	3	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	1	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.
	18	

Figure 1. Standard Telephone Pushbutton Keyboard



R_{ON} (CONTACT RESISTANCE) < 1kΩ

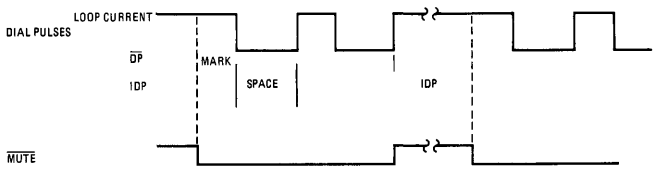
Figure 2. Logic Interface For the S2560



G1 through G7 any CMOS type logic gates

877292

Figure 3. Timing



877293

Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
(f_d/240)/ (f_d/120)	f_d				(f_d/240)	(f_d/120)	$\left(\frac{1920}{f_i} \times 10^3\right)$	$\left(\frac{960}{f_i} \times 10^3\right)$

Notes:

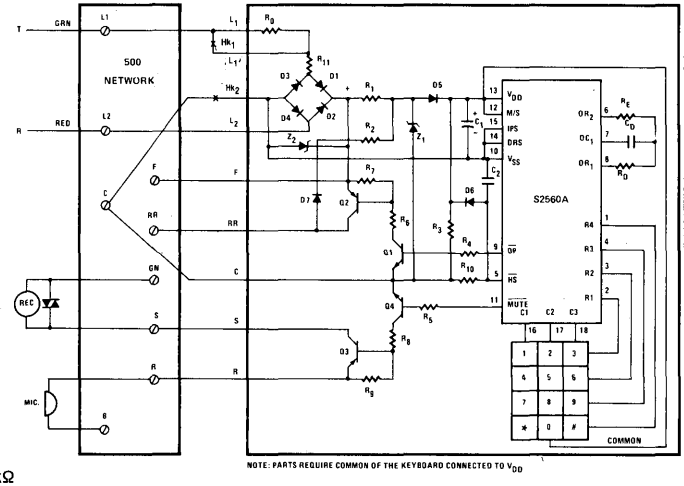
1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10 pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14 pps, and IDP of either 1142ms or 571ms can be selected.

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS	V_{SS} V_{DD}	(f/240) pps (f/120) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33-1/3/66-2/3 40/60
On Hook/Off Hook	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off Hook

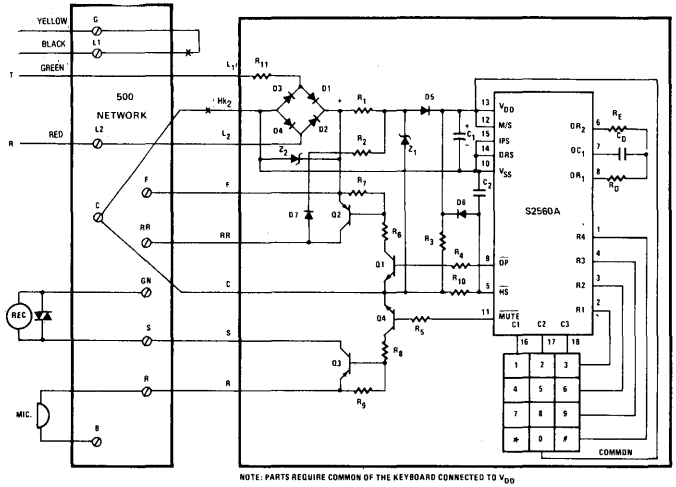
Note: f is the oscillator frequency and is determined as shown in Figure 5.

Figure 4. Pulse Dialer Circuit with Redial



R_0 = 10-20MΩ, R_1 = 150kΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ, R_{10} = 47kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004, D_5, D_6, D_7 = IN914, C_1 = 15μF
R_E = R_D = 750kΩ, C_D = 270pF, C_2 = 0.01μF
Q_1, Q_4 = 2N5550 TYPE Q_2, Q_3 = 2N5401 TYPE
Z_2 = IN5379 110V ZENER OR 2XIN4758

Figure 5. Pulse Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



R_1 = 10-20MΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ
R_{10} = 47kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, C_1 = 15μF
R_E, R_D = 750kΩ, C_D = 270pF
C_2 = 0.01μF, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

Figure 6. Circuit for Applying Momentary "On Hook" Condition During Power Up

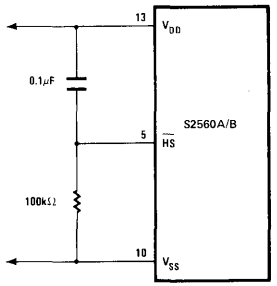
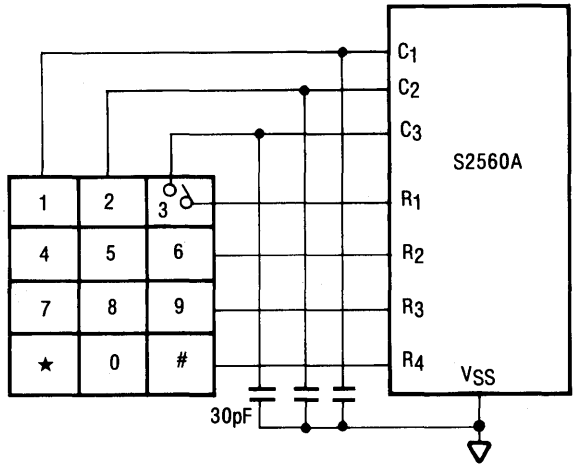


Figure 7. SPST Switch Matrix Interface

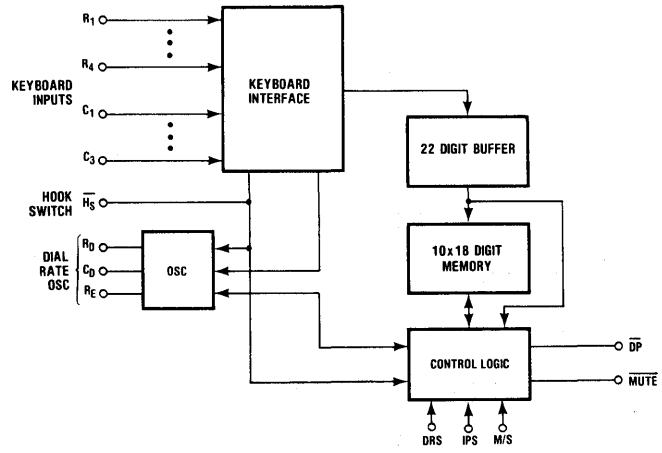


S25610 SINGLE CHIP REPERTORY DIALER

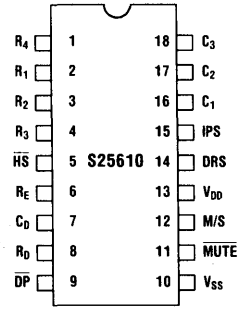
Features:

- ☐ Complete Pin Compatibility With S2560A Pulse Dialer Allowing Easy Upgrading of Existing Designs.
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓ - 66⅔/40-60), Interdigit Pause (400ms/800ms).
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD}$ to $V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	$V_{DD}-V_{SS}$ (Volts)	Min.	Max.	Units	Conditions
	Operating Voltage					
V_{DD}	Data Retention		1.0		V	On Hook, ($\overline{HS}=V_{DD}$)
V_{DD}	Non Dialing State		1.5	3.5	V	Off Hook, Oscillator Not Running
V_{DD}	Dialing State		2.0	3.5	V	Off Hook, Oscillator Running
	Operating Current					
I_{DD}	Data Retention	1.0		750	nA	On Hook, ($\overline{HS}=V_{DD}$)
I_{DD}	Non Dialing	1.5		10	μA	Off Hook ($\overline{HS}=V_{SS}$), Oscillator Not Running, Outputs Not Loaded.
I_{DD}	Dialing	2.0 3.5		100 500	μA μA	Off Hook, Oscillator Running, Outputs Not Loaded
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	$\overline{DP}$ Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	$\overline{MUTE}$ Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	$\overline{MUTE}$ Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	2.0 to 2.75 2.75 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leq R_D \leq 750K\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD}-V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD}-V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

Operating Characteristics

Normal Dialing

Off Hook, [D1] , ------- [Dn]

Dial pulsing to start as soon as first digit is entered (debounced and detected on chip). Pause may be entered in the dialing sequence by pressing the "#" key. Total number of digits entered not to exceed 22. Numbers exceeding 22 digits can be dialed but only after the first 22 digits have been completely dialed out. In this case redialing function is inhibited.

Storing of a Telephone Number(s)

Numbers can be stored as follows:

Off Hook, [*], [D1] ,---- [Dn] , [*], [LOC]

[*], [D1] , --- [Dn] , [*], [LOC]

etc.

Earpiece is muted in this operation to alert the user that a store operation is underway.

Repertory Dialing

Off Hook, [#], [LOC]

Numbers can be cascaded repeating [#], [LOC] sequence after completion of dialing of present sequence. If an access pause has been stored in "LOC", dialing will halt until the "#" key is pushed again.

Redialing

Last number dialed can be redialed as follows: Off Hook, [#] , [#] . Last number for this purpose is defined as the last number remaining in the buffer. Access pause is terminated by pushing the "#" key as usual.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components; two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D, $R_E = 750k\Omega$ and $C_D = 270pF$. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a $\pm 10\%$ tolerance of the dialing rate in the system.

Keyboard Interface (S25610)

The S25610 employs a scanning technique to determine a key closure. This permits interface to a DPCT (Double Pole Common Terminal) keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2),or a XY matrix. A high level on the appropriate row and column inputs constitutes a key closure for logic interface.

Off Hook Operations: The device is continuously powered through a 150kΩ resistor during off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during this pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

On Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the on hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed. DP and mute outputs are low in the on hook state.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10pps an IDP of 800ms is obtained and at 20pps an IDP of 400ms is obtained.

The user can enter a number up to 22 digits long from a standard 3×4 XY matrix keypad (Figure 1). It is also possible to use a logic interface or a keyboard with common (Figure 2) for number entry. Antibounce protection circuitry is provided on chip (min. 9ms) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed 22.

Redialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key twice. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

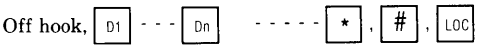
Repertory Dialing

Dialing of a number stored in memory is initiated by going OFF hook and pushing the # key followed by the single digit address. Numbers can be cascaded after dialing of the first number is completed.

Special Sequences

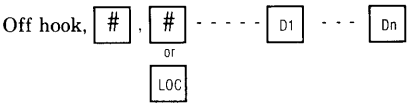
There are some special sequences that provide for mixed dialing or other features such as call disconnect, redial inhibit or memory clear as follows:

a. Normal dialing followed by repertory dialing



(wait for dialing to complete before pressing star key)

b. Normal dialing after repertory dialing or redialing



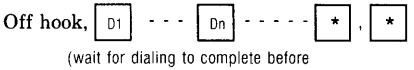
(wait for dialing to complete before pressing D1 key)

c. Disconnecting call

Off hook, - - - - -, * #

Pushing * and # keys simultaneously causes DP and mute outputs to go low and remain low until the keys are released. This causes a break in the line. If the keys are held down for a sufficiently long time (approx. 400ms), the call will be disconnected and new dial tone will be heard upon release of the keys. This feature is convenient when disconnecting calls by the normal method, i.e., hanging up the phone or depressing hookswitch is cumbersome.

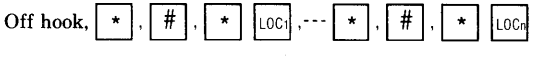
d. Inhibiting future redialing of a normally dialed number



(wait for dialing to complete before pressing star key)

Pushing * key twice after normal dialing is completed instructs the device to clear the redial buffer.

e. To clear a memory location(s)



Essentially this operation is equivalent to storing a pause in the memory location.

The various operating characteristics are summarized in Table 4.

Figure 1. SPST Matrix Keyboard Arranged in a Row, Column Format

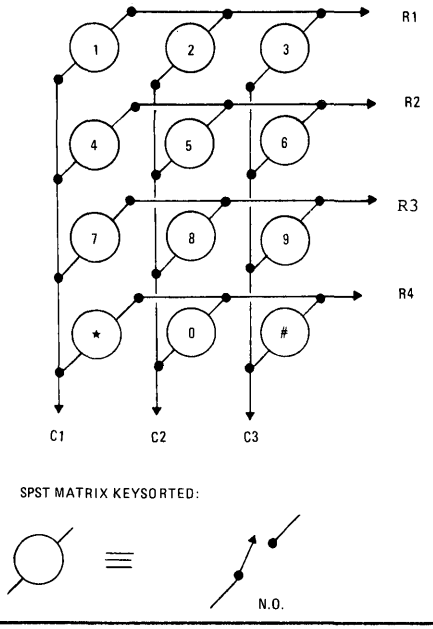


Figure 2. Standard Telephone Pushbutton Keyboard

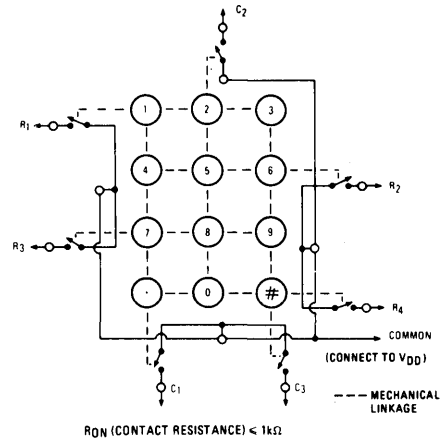


Figure 3. Timing (Off Hook)

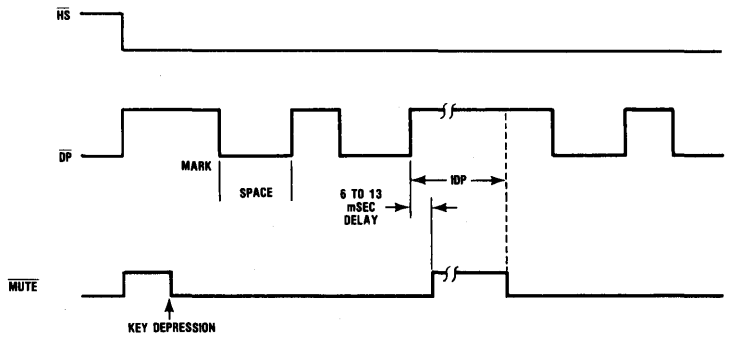


Table 1. S25610 Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 3. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IPS)	1	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	1	A programmable line allows selection of two different output rates such as 7 or 14pps, 10 or 20pps, etc. See Tables 2 and 3.
Mark/Space (MS)	1	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{\text{MUTE}}$)	1	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.
Dial Pulse Out ($\overline{\text{DP}}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator	3	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{\text{HS}}$)	1	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.

Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications.			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
(f_d/240)/ (f_d/120)	f_d				(f_d/240)	(f_d/120)	$\frac{1920}{f_i} \times 10^3$	$\frac{960}{f_i} \times 10^3$

Notes:

1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, an IDP of either 1142ms or 571ms can be selected.

Figure 4. Repertory Dialer Circuit with Redial

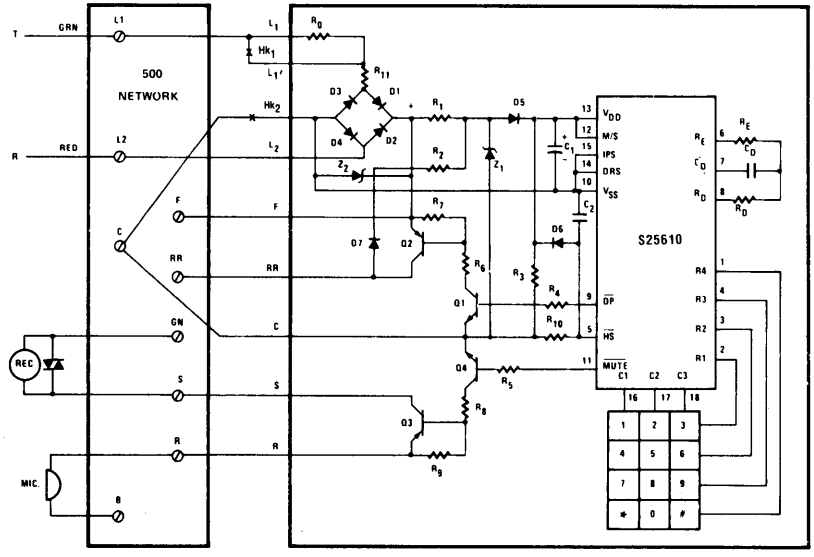
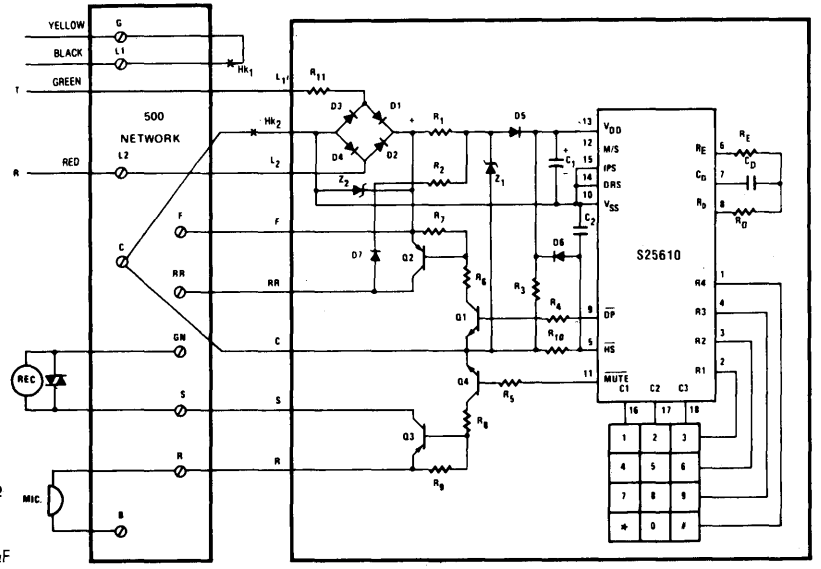


Table 3

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS}	(f/240) pps
		V_{DD}	(f/120) pps
Inter-Digit Pause Selection	IPS	V_{DD}	$\frac{960}{f}$ s
		V_{SS}	$\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS}	33-1/3/66-2/3
		V_{DD}	40/60
OnHook/Off Hook	$\overline{HS}$	V_{DD}	On Hook
		V_{SS}	Off hook

*Note: f is the oscillator frequency and is determined as shown in Figure 5.

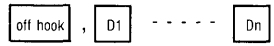
Figure 5. Repertory Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



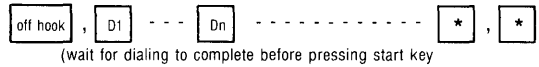
R_1 = 10-20MΩ, R_2 = 2kΩ
R_3 = 470kΩ, R_4, R_5 = 10kΩ
R_6, R_8 = 2kΩ, R_7, R_9 = 30kΩ
R_{10} = 47kΩ, R_{11} = 20Ω, 2W
Z_1 = 3.9V, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, C_1 = 15μF
R_E, R_D = 750kΩ, C_D = 270pF
C_2 = 0.01μF, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

Table 4. Summary of Operating Characteristics

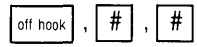
1) Normal Dialing:



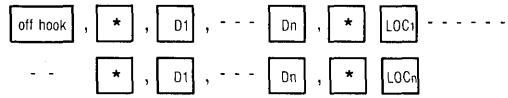
2) Inhibit Redialing:



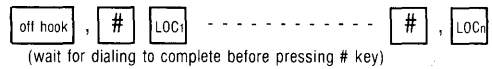
3) Redialing:



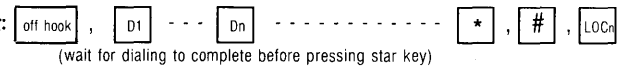
4) Storing of Number(s):



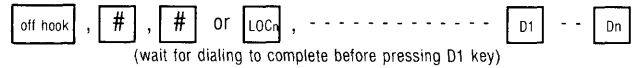
5) Repertory Dialing:



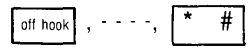
6) Normal Dialing + Repertory Dialing:



7) Recall + Normal Dialing:



8) Call Disconnect:



9) Clear Memory Location(s):

AMERICAN MICROSYSTEMS, INC.

S2561/S2561A/S2561C

TONE RINGER

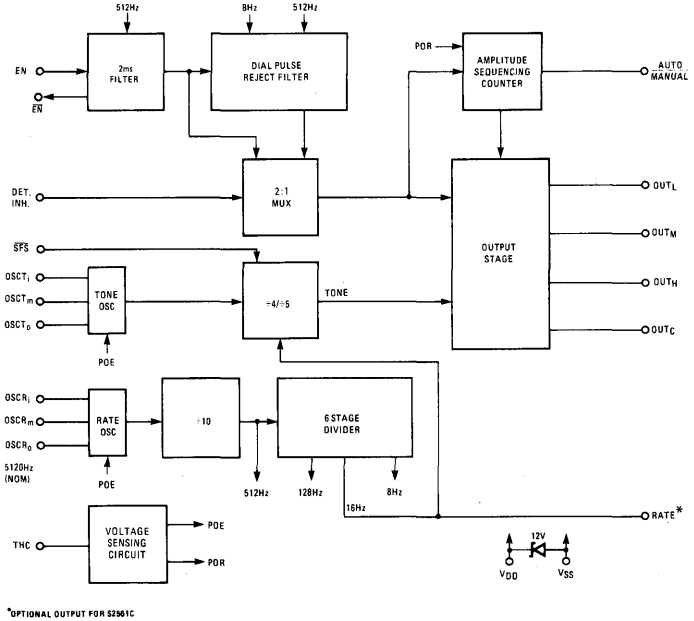
Features

- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 25mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

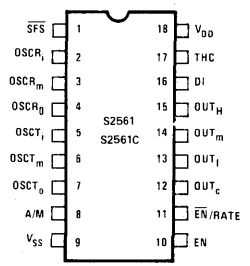
General Description

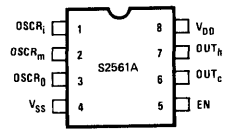
The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

Block Diagram



Pin Configuration





Absolute Maximum Ratings

Supply Voltage	+12.0V*
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

**This device incorporates a 12V internal zener diode across the VDD to VSS pins. Do NOT connect a low impedance power supply directly across the device unless the supply voltage can be maintained below 12V or current limited to <25mA.*

Electrical Characteristics

Specifications apply over the operating temperature and $3.5V \leq V_{DD}$ to $V_{SS} < 12.0V$ unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	12.0	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.0		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, V_{DD}=10V, THC pin open, DI pin open or V_{SS}
I_{OHC}	Output Drive Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD}=10V, V_{OUT}=0.75V
I_{OHM}	Output Source Current (Out_M output)	2		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD}=10V, V_{OUT}=0.75V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD}=10V, V_{OUT}=0.75V
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	V_{DD}+0.3	V	All inputs
V_{IL}	Input Logic "0" Level	V_{SS}−0.3	0.3 V_{DD}	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	0.9 V_{DD}		V	I_O=10μA (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	I_O=10μA (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 1	μA μA	V_{DD}=10V, V_{OUT}=0V V_{DD}=10V, V_{OUT}=10V
C_{IN}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	−5	+5	%	Fixed RC component values $1M\Omega \leq R_{ri}$, $R_{ti} \leq 5M\Omega$; $100k\Omega \leq R_{rm}$, $R_{tm} \leq 750k\Omega$; $150pF \leq C_{ro}$, $C_{to} \leq 3000pF$; 330pF recommended value of C_{ro} and C_{to}, supply voltage varied from 9V±2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range=300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, $V_{IN}=V_{DD}$ or V_{SS}		100	nA	Any input, except DI pin V_{DD}=10V
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	I_Z=5mA

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded

Functional Description

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies (512 and 640 Hz) with a frequency ratio of 5:4 at a 16 Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ±5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 1 for component and frequency selections. In the single frequency mode, activated by connecting the $\overline{SFS}$ input to V_{SS} only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: In the following description it is assumed that both the tone and rate oscillators are adjusted for a frequency of 5120 Hz. Ringing signal (nominally 42 to 105 VAC, 20 Hz, 2 sec on/4 sec off duty cycle) applied by the central office between the telephone line pair is capacitively coupled to the tone ringer circuitry as shown in Figure 2. Power for the device is derived from the ringing signal itself by rectification (diodes D1 thru D4) and zener diode clamping (Z_2). The signal is also applied to the EN input after limiting and clamping by a resistor (R_2) and internal diodes to V_{DD} and V_{SS} supplies. Internally the signal is first squared up and then processed thru a 2ms filter followed by a dial pulse reject filter. The 2ms filter is a two stage shift register clocked by a 512 Hz signal derived from the rate oscillator by a divide by 10 circuit. The squared ring signal (typically a square wave) is applied to the D input of the first stage and also to reset inputs of both stages. This provides for rejection of spurious noise spikes. Signals exceeding a duration of 2ms only can pass through the filter. The dial pulse reject filter is clocked at 8 Hz derived from the rate oscillator by a divide by 640 circuit. This circuit is designed to pass any signal that has at least two transitions in a given 125ms time period. This insures that signals below 8 Hz will be rejected with certainty. Signals over 16 Hz will be passed with certainty and between 8 Hz and 16 Hz there is a region of uncertainty. By adjusting the rate oscillator to a different frequency the break points in frequencies can be varied. For instance for break points of 10 Hz and 20 Hz the rate oscillator can be adjusted to 6400 Hz. Of course this also increases the tone shift rate to 20 Hz. The action of the dial pulse reject filter minimizes the dial pulse interference during dialing although it does not completely eliminate it due to the rather large region of uncertainty associated with this type of discrimination circuitry. The dial pulse filter also has the characteristic that an input signal is not detected unless its duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to V_{DD}. This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This produces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to V_{DD}. The internal threshold can also be reduced

Functional Description (Continued)

by connecting an external zener diode between the THC and V_{DD} pins.

Auto Mode: In the "auto" mode, activated by wiring the "auto/manual" input to V_{SS}, an amplitude sequencing of the output tone can be achieved. Resistors R_L and R_M are inserted in series with the Out_L and Out_M outputs, respectively, and paralleled with the Out_H output (Figure 1). Load is connected across Out_H and Out_C pins. R_L is chosen to be higher than R_M. In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.0 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltake will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.

Output Stage: The output stage is of push-pull type consisting of buffers L, M, H and C. The load is connected across pins Out_H and Out_C (Figure 2). During ringing, the Out_H and Out_C outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second ring and in the "high impedance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V_{DD} of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V_{DD} and V_{SS}.

Normal protection circuits are present on all inputs.

Table 1. S2561/S2561C Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}*, V_{SS}*)	2	These are the power supply pins. The device is designed to operate over the range of 3.5 to 12.0 volts. A range of 10 to 12 volts is recommended for the telephone application.
Ring Enable (EN*, $\overline{EN}$)	2	These pins are for the 20Hz ring enable input. They can also be used for DC level enabling by wiring the DI pin to V_{DD}. $\overline{EN}$ is available for the S2561 only.
Auto/Manual (A/M)	1	"Auto" mode for amplitude sequencing is implemented by wiring this pin to V_{SS}. "Manual" mode results when connected to V_{DD}. The amplitude sequencing counter is held in reset during the "manual" mode.
Outputs (Out_L, Out_M, Out_H^*, Out_C^*)	4	These are the push-pull outputs. Load is directly connected across Out_H and Out_C outputs. In the "auto" mode, resistors R_L and R_M can be inserted in series with the Out_L and Out_M outputs for amplitude sequencing (see Figure 1).
Oscillators Rate Oscillator ($OSCR_i^*$, $OSCR_m^*$ $OSCR_o^*$)	3	These pins are provided to connect external resistors RR_i, RR_m and capacitor CR_o to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.

Table 1 (Continued)

Pin	Number	Function
Tone Oscillator ($OSCT_i$, $OSCT_m$, $OSCT_o$)	3	These pins are provided to connect external resistors RT_i, RT_m and capacitor CT_o to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 5120Hz, a tone signal with frequencies of 512Hz and 640Hz results. See Table 2 for components selection.
Threshold Control (THC)	1	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It should be left open for telephone applications. For power supplies less than 9V connect to V_{DD}.
Rate	1	This is an optional output for the S2561C version which replaces the $\overline{EN}$ output. This is a 16Hz output that can be used by external logic as shown in Figure 3-A to produce a 2sec on/4sec off waveform.
Detector Inhibit (DI)	1	When this pin is connected to V_{DD}, the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to V_{SS} in normal telephone-type applications.
Single Frequency Select ($\overline{SFS}$)	1	When this pin is connected to V_{SS}, only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to V_{DD}.
	$\overline{18}$	

**Pinouts of 8 pin S2561A package.*

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)	Oscillator Components R_I (kΩ)	R_M (kΩ)	C_O (pF)	Rate (Hz)	Tone (Hz)
5120	1000	200	330	16	512/640
6400	Select components in the ranges indicated in the table of electrical charateristics			20	640/800
3200				10	320/400
8000				25	800/1000
fo				$\frac{fo}{320}$	$\frac{fo}{10}/\frac{fo}{8}$

Applications

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer circuit power is derived from the telephone lines by the network formed by capacitor C_1, resistor R_1, diode bridge D_1 through D_4, and filter capacitor C_2. C_2 is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of C_2 may be 47μF. C_1 and R_1 are chosen to satisfy the Ringer Equivalence Number (REN) spcification (REf. 1). For REN=1 the resistor should be a mini-mum of 8.2kΩ. It must be noted that the amount of power that can be delivered to the load depends upon the selection of C_1 and R_1.

The device is enabled by limiting the incoming ring signal through resistors R_2, R_3 and diodes d_5 and d_6. Zener diode Z_1 (typ. 9-27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 540 Hz with a shift rate of approximately 16 Hz and deliver at least 25mW to an 8Ω speaker through a 2000Ω:8Ω transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors R_L and R_M can be chosen to provide desired amplitude sequencing. Typically, signal power will be down $20 \log \left(\frac{R_{LOAD}}{R_L + R_{LOAD}} \right)$ dB during the first ring, and down $20 \log \left(\frac{R_{LOAD}}{R_M + R_{LOAD}} \right)$ dB during the second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to V_{DD}. Det. Inh pin must be connected to V_{DD} to allow DC level enabling of the ringer.

Non-Telephone Applications: The configuration shown in Figure 3-A may be used in non-telephone applications where it is desired to simulate the telephone bell. The internal threshold is bypassed by wiring THC to V_{DD}. The rate output (16Hz) is divided down by a 7 stage divider type 4024 to produce two signals: a 2 second on/2 second off signal and a 4 second on/4 second off signal. The first signal is connected to the EN pin and the second to the DI pin to produce a 2 second on/4 second off telephone-type ring signal. The ring sequence is initiated by removing the reset on the divider. If "auto" mode is used, a reset signal must be applied to the "amplitude sequencing" counter at the end of a ring sequence so that the circuit will respond correctly to a new ring sequence. This is done by temporarily connecting the "auto/manual" input to V_{SS}.

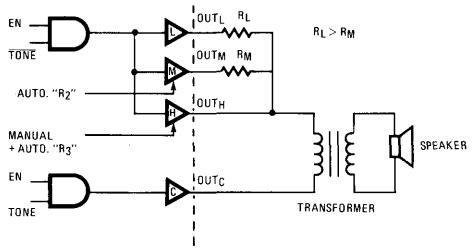
Figure 3-B shows a typical application for alarms, buzzers, etc. Single frequency mode is used by connecting the $\overline{SFS}$ input to V_{SS}. A suitable on/off rate can be determined by using the 7 stage divider circuit. If continuous tone is not desired, the 16Hz output can be used to gate the tone on and off by wiring it into the ENABLE input.

Many other configurations are possible depending upon the user's specific application.

Reference 1. Bell system communications technical reference:

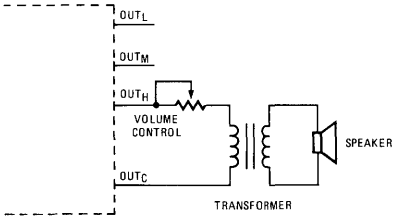
PUB 47001 of August 1976
"Electrical characteristics of Bell System Network Facilities at the interface with Voiceband Ancillary and Data Equipment" — Sections 2.6.1 and 2.6.3.

Figure 1-A. Output Stage Connected for Auto Mode Operation



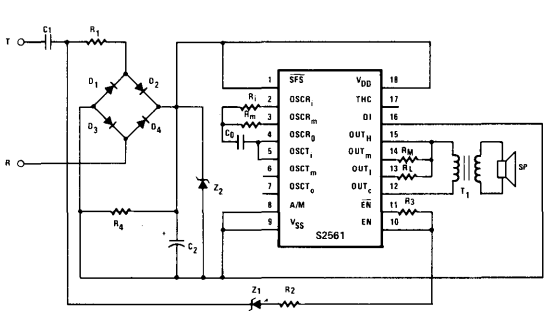
877276

Figure 1-B. Output Stage Connected for Manual Mode Operation.



877277

Figure 2. Typical Telephone Application of the S2561 and S2561A



C_1	.47μF/200V	R_1	2KΩ	R_i	1MΩ	R_L	18KΩ	SP	8ΩSPEAKER
C_2	47μF/25V	R_2	51KΩ	R_m	200KΩ	R_M	3.3KΩ	T_1	2000Ω/8ΩXFMR
D_1–D_4	IN4004	R_3	10MΩ	C_g	300pF	R_4	100KΩ	Z_1	9 TO 27V ZENER
Z_2	IN4742 12V ZENER								

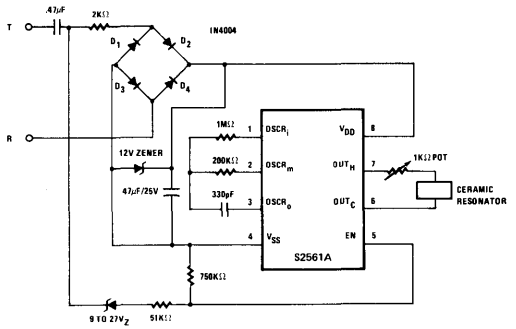


Figure 3-A. Simulation of the Telephone Bell in Non-Telephone Applications.

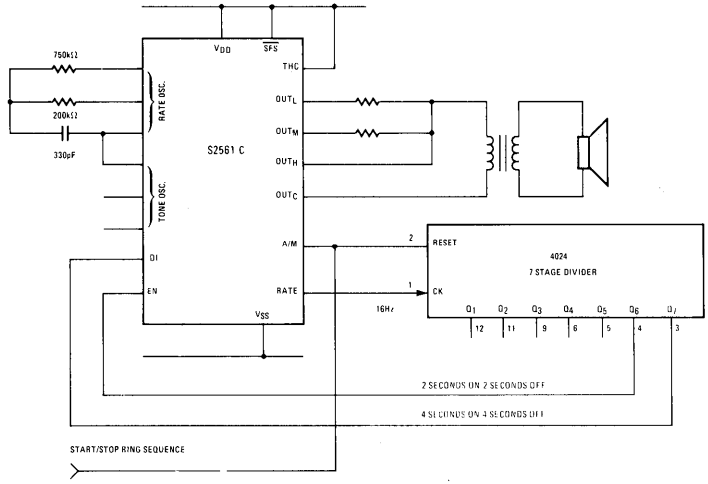
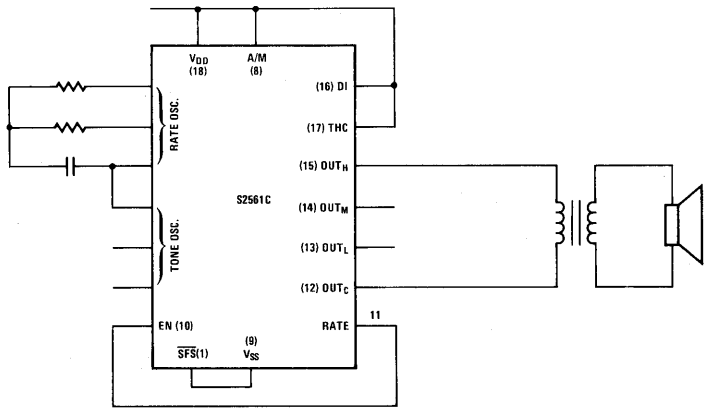


Figure 3-B. Single Frequency Tone Application in Alarms, Buzzers, Etc.



AMERICAN MICROSYSTEMS, INC.

S2562

REPERTORY DIALER

Features

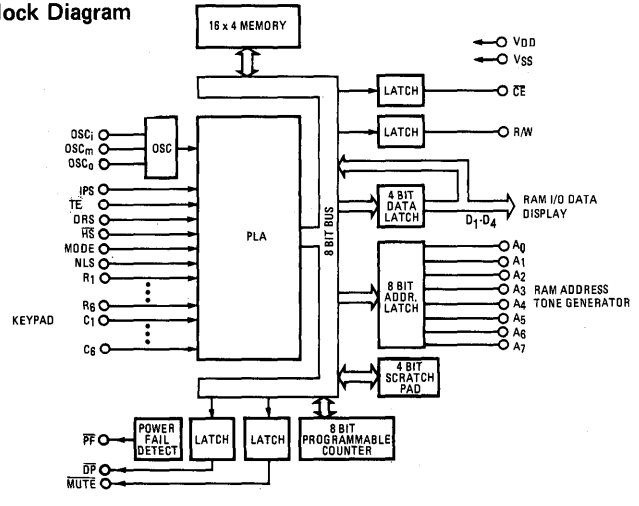
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing with Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Memory Storage of 32 8-Digit Numbers or 16 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries
- ☐ Inexpensive, but Accurate R-C Oscillator Design Provides Better Than ±3% Accuracy Over Supply Voltage, Temperature and Unit-Unit Variations and Allows Different Dialing Rates, IDP and Tone Drive Timing by Changing the Time Base
- ☐ Power Fail Detection
- ☐ BCD Output with Update for Number Display Applications

General Description

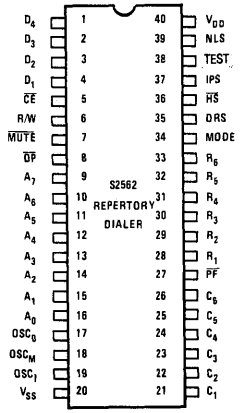
The S2562 Repertory Dialer is a CMOS integrated circuit that can perform storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101—256x4 RAM that functions as telephone number storage. With one S5101 up to 32 8-digit or 16 16-digit numbers can be stored. It can provide either dial pulses or DTMF tones with the addition of the AMI S2559 tone generator for either the dial or tone line applications.

Data subject to change at any time without notice. These sheets transferred for information only.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	13.5V
Operating Supply Voltage Range ($V_{DD}-V_{SS}$)	3.5V to 7.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	200°C

Electrical Characteristics:

Specifications apply over the operating temperature range and $4.5V \leq V_{DD}$ to $V_{SS} \leq 5.5V$ unless otherwise specified. Absolute values of measured parameters are specified.

Symbol	Characteristics	Min.	Max.	Units	Conditions
	Output Drive				
I_{OLDP}	$\overline{DP}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHDP}	$\overline{DP}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
I_{OLM}	$\overline{MUTE}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHM}	$\overline{MUTE}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
I_{OHPF}	$\overline{PF}$ Output Source Current	100		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
	CMOS to CMOS				
V_{IL}	Logic "0" Input Voltage		1.5	V	All inputs, $V_{DD}=5V$
V_{IH}	Logic "1" Input Voltage	3.5		V	All inputs, $V_{DD}=5V$
V_{OL}	Logic "0" Output Voltage		0.5	V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, $I_O=-10\mu A$, $V_{DD}=5V$
V_{OH}	Logic "1" Output Voltage	4.5		V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, $I_O=-10\mu A$, $V_{DD}=5V$
	Current Levels				
I_{DD}	Quiescent Current		25	μA	Standby, $V_{DD}=5V$
I_{DD}	Operating Current		500	μA	All valid input combinations, $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$ outputs open $V_{DD}=5V$
I_{IH}	Input Current Any Pin (keyboard inputs)	10	100	μA	$V_{IN}=V_{DD}$, $V_{DD}=5V$
I_{IL}, I_{IH}	Input Current All Other Pins		100	μA	$V_{IN}=V_{SS}$ or V_{DD}, $V_{DD}=5V$
I_{OZ}	Output Current in High Impedance State		1 1	μA μA	$V_{DD}=5V$, $V_{OUT}=0V$ data outputs (D1-D4) $V_{DD}=5V$, $V_{OUT}=5V$
fo	Oscillator Frequency	4	10	kHz	$V_{DD}=5V$ (min. duty cycle 30/70)
Δfo/fo	Frequency Deviation	−3	+3	%	$V_{DD}-V_{SS}$ from 4.5V to 5.5V. Fixed R-C oscillator components $50k\Omega \leq R_M \leq 750k\Omega$; $1M\Omega \leq R_I \leq 5M\Omega$; $150pF \leq C_O$ 3000pF; 330pF most desirable value for C_O, fo < 10kHz over the operating temperature and unit-unit variations
C_{IN}	Input Capacitance, Any Pin		7.5	pF	
V_{TRIP}	Supply Voltage at which $\overline{PF}$ Output Goes Low	2.5	4.5	V	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and posible damage of the input-protection diode when the device power supply is grounded. Power should be applied to the device in "on hook" condition.

Functional Description

The S2562 is a CMOS controller designed for storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101 256x4 RAM that functions as a telephone number storage. A single S5101 RAM will store up to 32 8-digit or 16 16-digit telephone numbers. The S2562 can be programmed to work with either 8-digit or 16-digit numbers by means of the Number Length Select (NLS) input.

The S2562 uses an inexpensive, but accurate R-C oscillator as a time base from which the dialing rate and inter-digit pause duration (IDP) are derived. Different dialing rates and IDP durations can be implemented by simply adjusting the oscillator frequency. The dialing rate and IDP can be further changed by a 2:1 factor by means of the dialing rate select (DRS) and inter-digit pause select (IPS) inputs. Thus, for the oscillator frequency of 8kHz, dialing rates of 10 and 20 pps and IDP's of 400 and 800ms can be achieved. The mark/space ratio is fixed independent of the time base at 40/60. Over supply voltage (5V±10%), operating temperature range and unit-unit variations, timing accuracy of ±3% can be achieved. A mute output is also available for muting of the receiver during dial pulsing. See Figure 5 for timing relationship.

The S2562 can be programmed by means of the MODE input for dual tone signaling applications as well. In this mode, it can interface directly with the AMI standard S2559 Tone Generator to produce the required DTMF signals. The tone on/off rate during an auto dial operation in this mode is derived from the time base. For the oscillator frequency of 8kHz, a tone drive rate of 50ms on, 50ms off is obtained. Different rates can be implemented by adjusting the time base as desired. See Tables 2 and 3 for the various combinations. In the tone mode, the mute output is used to gate the tone generator on and off. The 8 address lines that are normally used for addressing the RAM are also used to address the tone generator row, column inputs. Figure 6 shows a typical system application.

The S2562 can perform the following functions:

Normal Dialing

The user enters the desired number digits through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. Debouncing is provided on the keyboard entries to avoid false entries. The number entered is retained for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of digits (8 or 16).

An update pulse is generated to update the display digit as a new entry is made.

Redialing

The last number entered is retained in the internal memory and can be redialed by going "off hook" and depressing the "redial" (RDL) key. The RDL key is a unique 2 of 12 matrix location (R5, C3). The number being redialed out is displayed as it is dialed out.

In the tone mode, the redial tone drive rate depends upon the time base as discussed before.

Storing of a Normally Dialed or Redialed Number into the External Memory

After the normal dialing or redialing operation, the telephone number can be stored in the external memory for future repertory dialing use by going on hook and initiating the following key sequence.

1. Push "store" (ST) button.
2. Depress the single digit key corresponding to the desired address location.

Note that the "ST" key is a unique 2 of 12 matrix location (R_5, C_1).

Storing of a Telephone Number into the External Memory

This operation is performed "on hook" and no outdialing occurs. A telephone number can be stored in the desired address location by initiating the following key sequence.

1. Push the "*" key (This instructs the device to accept a new number for storage into the internal memory).
2. Enter the digits (including any access pauses) corresponding to the desired number. Digits will be displayed as they are entered.
3. Push the "ST" key.
4. Push the single digit key corresponding to the desired address location.

The entire sequence can be repeated to store as many numbers as desired. However, any memory locations not addressed with a telephone number "store" operation must be addressed with the following sequence.

1. Push the "*" key.
2. Push the "ST" key.
3. Push the single digit key corresponding to the first unused memory location.
4. Push the "ST" key.

5. Push the single digit key corresponding to the next unused memory location.

Steps 4. and 5. are repeated until all remaining memory locations have been addressed.

It should be noted that accessing all memory locations is required only for initial system set-up. This insures that no memory location will contain invalid data from memory power-up. If a memory location were to have invalid, power-up induced data and that location was addressed by the S2562, the S2562 would enter a "Halt" state and cease its normal program activities. To exit from this condition it is necessary to go "on hook" and perform a "store" operation.

Displaying of a Stored Telephone Number

This is an "on hook" operation Either the last dialed number or the number stored in the external memory can be displayed one digit at a time. The key sequence for displaying the last dialed number is as follows:

Push the "RDL" key.

The number in the external memory can be displayed as follows:

1. Push the "R" key.
2. Push the single digit key corresponding to the desired address location.

Note that the "R" key is a unique 2 of 12 matrix location (R_5, C_2).

The number is displayed one digit at a time at a rate determined by the time base. With a time base of 8kHz the display will be on 500ms, off 500ms. The display is updated by producing an update pulse. The update pulse must be decoded with external logic (one inverter and one 2-input gate) as shown in Figure 6.

The display is blanked by outputting an illegal (non BDC) code such as 1111. The 4511-type BCD to 7 segment decoder driver latch will blank the display when the illegal code is detected. When other driver circuits are employed, external logic must be used to detect the illegal code. Table 4 gives a list of display codes used by S2562.

Repertory Dialing

This is the most common mode of usage and allows the user to dial automatically any number stored in the memory. This mode is initiated by the following key sequence after going off hook.

1. Push the "*" key.
2. Push the single digit key corresponding to the desired address location.

The number is displayed as it is dialed out. In the tone mode, the tone driver rate is dependent on the time base as described earlier.

Pause

Note that the out dialing in the repertory or redial operation continues unless an access pause is detected. The outpulsing will stop and resume only when the user terminates the access pause by pushing the "*" key again.

Power Fail Detection

This output is normally high. When the supply voltage falls below a predetermined value, it goes low. The output can then drive a suitable latching device that will switch the memory to either the tip and ring or an auxiliary battery supply.

Memory Expansion

The memory can be expanded by paralleling additional S5101 RAM's. External logic must be used to enable the desired RAM corresponding to a desired address location. The S2562 can drive up to 2 RAM's without the need of buffering address and data lines.

Keybounce Protection

When a key closure is detected by the S2562, an internal timeout (4ms at fo=8kHz) is started. Any transitions that occur during this timeout will reset the timer to zero so that a key will only be accepted as valid after a noise free timeout period. The key must remain closed for an additional 16ms before released. Thus, the total make time of the key must be at least 20ms. The key must be released for at least 1ms before a new key is activated. Any transitions occurring when the key is released are ignored as long as the make time does not exceed 4ms.

Improper Operating Sequence

The S2562 will enter a "halt" state if a proper operating sequence is not followed. Examples of such sequences are:

1. Off hook, "ST", on hook
2. 2. Off hook, "*", on hook
3. Off hook, "*", unprogrammed loc.
4. On hook, "*", D_1, D_2 - - -, off hook without completing the store sequence
5. Off hook with supply voltage less than 3.5 volts

To clean the halt state press "ST" key followed by an unused "loc" key. This can be performed in either on hook or off hook condition. Figure 1 shows a scheme to clear the halt state electronically.

Table 1. Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 3.5V to 7.5V.
Keyboard (R_1-R_6, C_1-C_6)	12	These are 6 row and 6 column inputs from the keyboard contacts. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect to each other. Figure 2 depicts the standard telephone X-Y matrix keyboard arrangements that can be used. A logic, interface is also possible as shown in Figure 3. Debouncing is provided to avoid false entry. Key pad entry options are shown in Figure 4.
Number Length Select (NLS)	1	This input permits programming of the device to accept either 8-digit numbers or 16-digit numbers.
Mode Select (MODE)	1	This input allows the use of the device in either dial pulsing applications or tone drive applications.
Dial Rate Select (DRS)	1	This input allows selection of two different dialing rates such as 10 or 20 pps, 7 or 14 pps, etc. See Tables 2 and 3.
Inter-Digit Pause Select (IPS)	1	This allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceeding the first dialed digit is an inter-digit time equal to the selected IDP. Two pause durations, either 400ms or 800ms are available at dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Test Input (TEST)	1	This input is used for test purposes. For normal operation it must be tied to V_{DD}.
Mute Output ($\overline{MUTE}$)	1	A pulse is available that can provide drive to turn on an external transistor to mute the receiver during dial pulsing. See Figure 5 for mute and dial pulse output relationship. It is also used as a keyboard disable in the tone drive applications. See Figure 6.
Dial Pulse Output ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. This output will be normally high and go low during "space" or "break."
Display Memory I/O Data (D_1-D_4)	4	These are 4 bidirectional pins for inputting and outputting data to the external memory and display driver.

Table 1. (Continued)

Pin	Number	Function
Memory Enable ($\overline{CE}$)	1	This line controls the external memory operation.
Memory Read/Write (R/W)	1	This line controls the read or the write operation of the external memory. This output along with the $\overline{CE}$ output can be used to produce a pulse to update the external display. See Figure 6.
Tone Generator/Memory Address (A_0-A_7)	8	These are 8 output lines that carry the external memory address and tone generator row/column information.
Hook Switch ($\overline{HS}$)	1	This input conveys the state of the subset. "Off hook" corresponds to V_{SS} condition.
Power Fail Detect ($\overline{PF}$)	1	This output is normally high and goes low when the power supply falls below a certain predetermined value.
Oscillator (OSC_i, OSC_m, OSC_o)	3	These pins are provided to connect external resistors R_I, R_M and capacitor C_O to form an R-C oscillator that generates the time base for the repertory dialer. The output dialing rate, tone drive rate and IDP are derived from this time base.

Table 2. Table for Selection of Oscillator Component Values for Desired Dialing Rate, I_{DP} or Tone Drive Rate

Dial Rate Desired (PPS)	Osc. Freq. fo (Hz)	Oscillator Components R_M (kΩ)	Oscillator Components (R_I) (kΩ)	Oscillator Components C_O (pF)	Dial Rate (PPS) DRS=V_{SS}	Dial Rate (PPS) DRS=V_{DD}	IDP (ms) IPS=V_{SS}	IDP (ms) IPS=V_{DD}	Tone Drive On/Off Time (ms)
5.5/11	4400	TBD			5.5	11	1454	727	90/90
6/12	4800	220			6	12	1334	667	83.3/83.3
6.5/13	5200	190			6.5	13	1230	615	77/77
7/14	5600				7	14	1142	571	71/71
7.5/15	6000		1000	300	7.5	15	1066	533	66.7/66.7
8/16	6400				8	16	1000	500	62.5/62.5
8.5/17	6800	TBD			8.5	17	942	471	59/59
9/18	7200				9	18	888	444	55.5/55.5
9.5/19	7600				9.5	19	842	421	52.6/52.6
10/20	8000	110			10	20	800	400	50/50
(fo/800/ (fo/400)	fo				fo/800	fo/400	$\frac{6400 \times 10^3}{fo}$	$\frac{3200 \times 10^3}{fo}$	$\frac{400 \times 10^3}{fo}$/$\frac{400 \times 10^3}{fo}$

Figure 1. Logic to Eliminate Halt Condition Due to Improper Sequencing.

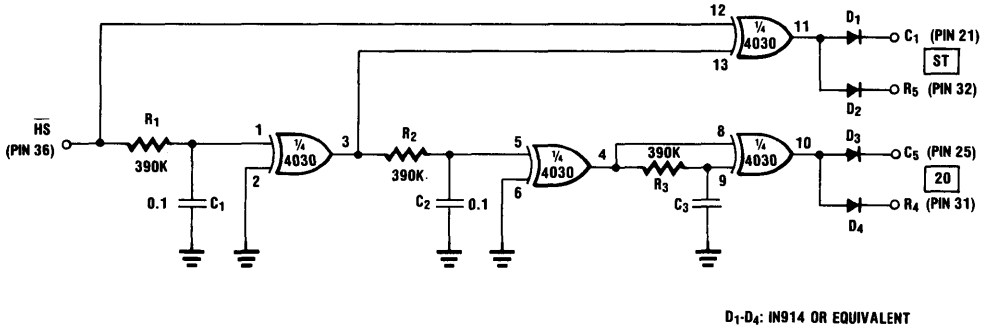
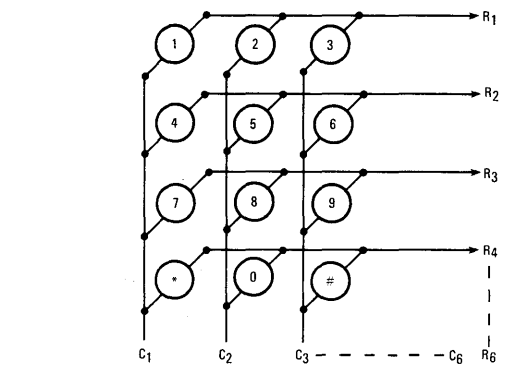
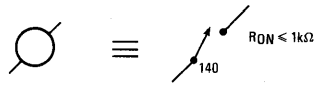


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 12 Row, Column Format

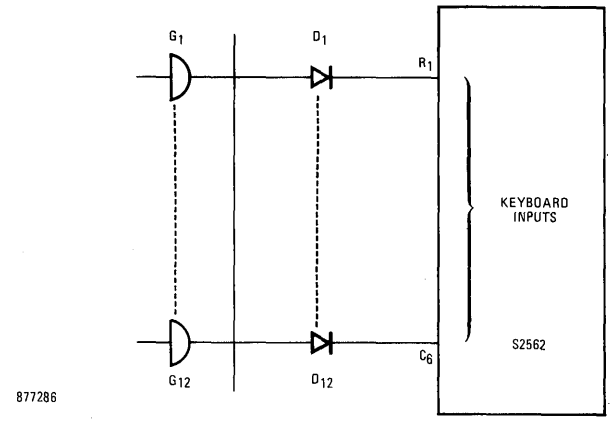


SPST MATRIX KEYBOARD:



877285

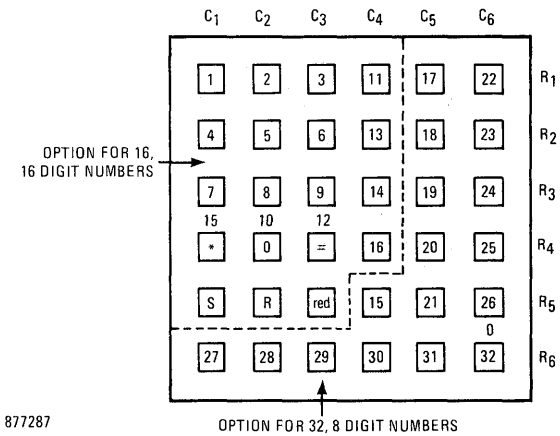
Figure 3. Logic Interface For the S2562



G_1 through G_{12} any CMOS type logic gates.
D_1 through D_{12} DIODES type 1N 914. (Optional)

A valid key closure corresponds to a logic high level on one row and one column

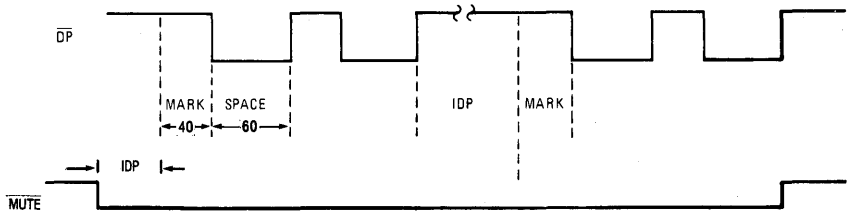
Figure 4. Example of Keypad Entry – Options



Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS} V_{DD}	(fo/800) pps (fo/400) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	(3200/fo) S (6400/fo) S
Test Input	TEST	V_{SS} V_{DD}	Test Mode Normal Mode
Hook Switch	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off hook
Mode Selection	MODE	V_{SS} V_{DD}	Dial pulse Tone Drive*
Number Length Selection	NLS	V_{SS} V_{DD}	8 digits 16 digits

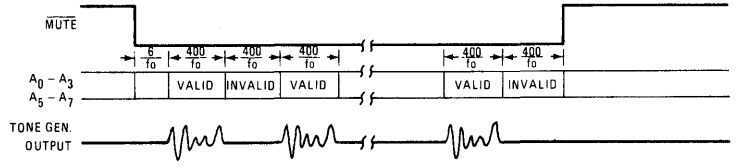
*For tone mode also set DRS=V_{SS}, IPS=V_{SS} and Test=V_{DD}.
Note: fo is the oscillator frequency and is determined as shown in Table 2.

Mute and Dial Pulse Output Timing Relationship



Mute will reset i) when the number of digits dialed out equals either the number of digits entered or the maximum selected (8 or 16) or ii) when an access pause is detected.

Figure 5B. Mute and Tone Output Timing Relationship



Mute output will reset i) when the number of digits dialed out equals the number of digits entered or equals the maximum selected (8 or 16) or ii) when an access pause is detected. In the normal dialing mode when digits are entered one at a time the mute output will reset between digits provided the time between entered digits exceeds $\frac{400}{fo}$. In both the normal dialing or automatic dialing mode tone will be output for a fixed duration of $\frac{400}{fo}$ (50msec for fo = 8kHz).

Figure 6. Typical Application of the S2562

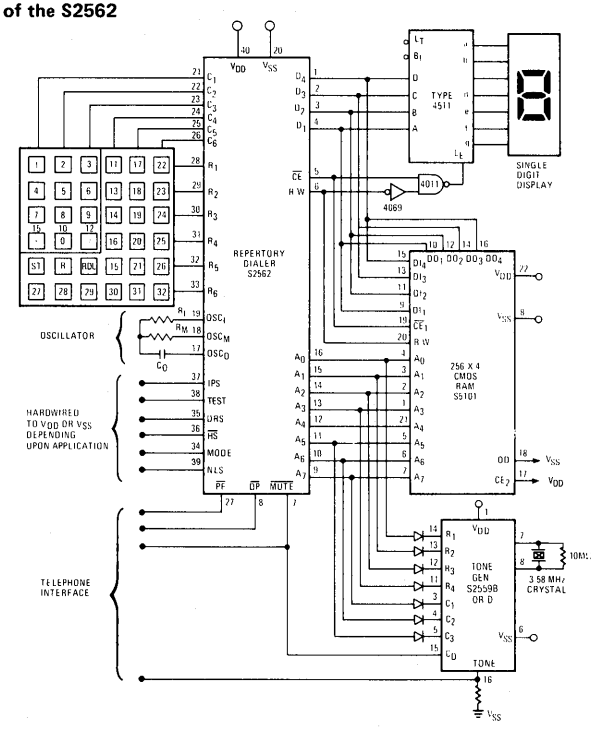


Table 4. Display Codes

D_4	D_3	D_2	D_1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Not Used
1	0	1	1	Not Used
1	1	0	0	# (Pause)
1	1	0	1	Not Used
1	1	1	0	Beginning of Number
1	1	1	1	Blank

AMERICAN MICROSYSTEMS, INC.

S2563

REPERTORY DIALER

COMMUNICATIONS

Features

- ☐ Specifically Designed for Telephone Line Powered Applications
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing With Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Two Selections of Mark/Space Ratio
- ☐ Memory Storage of 29 8-Digit Numbers or 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Can Use Standard 3×4 or 4×4 Keyboards
- ☐ Inexpensive, but Accurate R-C Oscillator Design
- ☐ BCD Output with Update for Single Digit Display

General Description

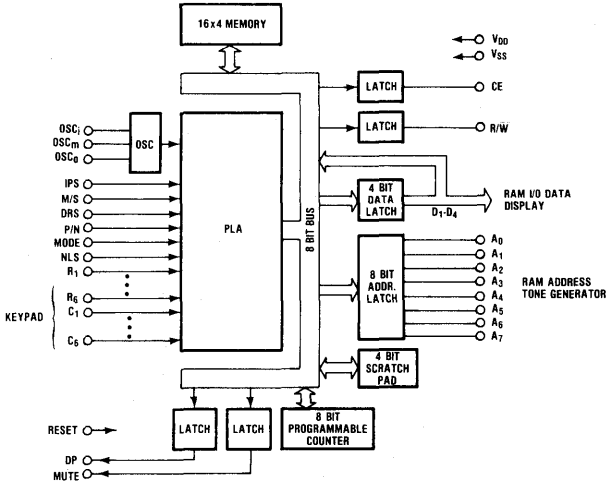
The S2563 is an improved version of the S2562 repertory dialer and can replace the S2562 in existing applications using local power. It is however specifically designed for applications that will only use telephone line power. To achieve this following changes were made to the S2562 design.

a. $\overline{PF}$ output was replaced by a level reset input which allows the device to be totally powered down in the on-hook state of the telephone.

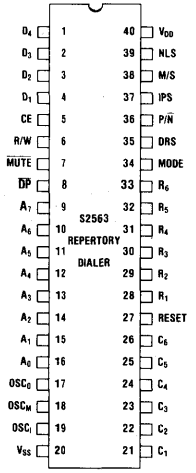
b. To reduce power consumption in the associated S5101 memory in the standby mode, the interface was changed so that its CE_2 input rather than the the $\overline{CE_1}$ input is controlled by the device.

c. Process was changed to a lower voltage CMOS process. Additionally a mark/space selection input (M/S) was added to allow selection of either 40/60 or 33/67 ratio. Provision was also made to allow the device to work with a standard 3×4 or 4×4 keyboard.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	6.0V
Operating Supply Voltage Range ($V_{DD}-V_{SS}$)	2.0V – 5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	200°C

Electrical Characteristics:
Specifications apply over the operating temperature range unless otherwise specified. Absolute values of measured parameters are specified.

Symbol	Characteristics	Min.	Max.	Units	Conditions
	Output Drive				
I_{OLDP}	$\overline{DP}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHDP}	$\overline{DP}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
I_{OLM}	$\overline{MUTE}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHM}	$\overline{MUTE}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
	CMOS to CMOS				
V_{IL}	Logic "0" Input Voltage		30%V_{DD}	V	All inputs
V_{IH}	Logic "1" Input Voltage	70%V_{DD}		V	All inputs
V_{OL}	Logic "0" Output Voltage		0.5	V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $I_O=10\mu A$, $V_{DD}=5V$
V_{OH}	Logic "1" Output Voltage	4.5		V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $I_O=-10\mu A$, $V_{DD}=5V$
	Current Levels				
I_{DD}	Quiescent Current		1.0	μA	Standby, $V_{DD}=1.5V$ (Data Retention)
I_{DD}	Operating Current		500	μA	All valid input combinations, $\overline{DP}$, $\overline{MUTE}$, outputs open $V_{DD}=5V$
I_{IH}	Input Current (keyboard inputs)	10	100	μA	$V_{IN}=V_{DD}$, $V_{DD}=5V$
I_{IL}, I_{IH}	Input Current All Other Pins		10	μA	$V_{IN}=V_{SS}$ or V_{DD}, $V_{DD}=5V$
I_{OZ}	Output Current in High Impedance State		10 10	μA μA	$V_{DD}=5V$, $V_{OUT}=0V$ data outputs (D1-D4) $V_{DD}=5V$, $V_{OUT}=5V$
fo	Oscillator Frequency	4	10	kHz	$V_{DD}=5V$ (min. duty cycle 30/70)
Δfo/fo	Frequency Deviation	−3	+3	%	$V_{DD}-V_{SS}$ from 4.5V to 5.5V. Fixed R-C oscillator components $50k\Omega \leq R_M \leq 750k\Omega$; $1M\Omega \leq R_I \leq 5M\Omega$; $150pF \leq C_O$ 3000pF; 330pF most desirable value for C_O, fo < 10kHz over the operating temperature and unit-unit variations
C_{IN}	Input Capacitance, Any Pin		7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and posible damage of the input-protection diode when the device power supply is grounded. Power should be applied to the device in "on hook" condition.

Functional Description

The S2563 is a CMOS controller designed for storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101 256×4 RAM that functions as a telephone number storage. A single S5101 RAM will store up to 29 8-digit or 16 16-digit telephone numbers. The S2563 can be programmed to work with either 8-digit or 16-digit numbers by means of the Number Length Select (NLS) input.

The S2563 uses an inexpensive, but accurate R-C oscillator as a time base from which the dialing rate and inter-digit pause duration (IDP) are derived. Different dialing rates and IDP durations can be implemented by simply adjusting the oscillator frequency. The dialing rate and IDP can be further changed by a 2:1 factor by means of the dialing rate select (DRS) and inter-digit pause select (IPS) inputs. Thus, for the oscillator frequency of 8kHz, dialing rates of 10 and 20 pps and IDP's of 400 and 800ms can be achieved.

The reset and P/$\overline{N}$ inputs are used to put the device in various operating modes. To store numbers in the memory P/$\overline{N}$ input must be made high. When low, normal operations such as dialing, redialing or memory dialing can be performed. When reset input is high, it overrides and forces the device in a power down mode. Connections of the two inputs depend upon the application—local power or telephone line power. See Table 4 for connection details.

The S2563 can also operate in the tone mode (MODE= V_{DD}). In this mode, it can interface with the AMI standard S2559 Tone Generator to produce the required DTMF signals. The tone on/off rate during an auto dial operation in this mode is derived from the time base. For the oscillator frequency of 8kHz, a tone drive rate of 50ms on, 50ms off is obtained. Different rates can be implemented by adjusting the time base as desired. See Tables 2 and 3 for the various combinations. In the tone mode, the mute output is used to gate the tone generator on and off. The 8 address lines that are normally used for addressing the RAM are also used to address the tone generator row, column inputs. Figure 6 shows a typical system application.

The S2563 operates in the following modes:

Normal Dialing

The user enters the desired number digits through the keyboard after entering the normal mode. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. Debouncing is provided on the keyboard entries to avoid false entries. The number entered is retained for future redial. Pauses may be entered when required in the dial sequence by pressing the "P" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of digits (8 or 16). An update pulse is generated to update the display digit as a new entry is made.

Redialing

The last number entered is retained in the internal memory and can be redialed by going in the normal mode and depressing the "redial" (RL) key. The RL keys are at locations (R_5, C_3) and (R_3, C_4). The number being redialed out is displayed as it is dialed out.

In the tone mode, the redial tone drive rate depends upon the time base as discussed before.

Storing of a Normally Dialed or Redialed Number into the External Memory

After the normal dialing or redialing operation, the telephone number can be stored in the external memory for future repertory dialing use by initiating the following key sequence.

1. Push "store" (ST) button.
2. Depress the single digit key corresponding to the desired address location.

Note that the "ST" keys are at locations (R_5, C_1) and (R_1, C_4).

Repertory Dialing

This is the most common mode of usage and allows the user to dial automatically any number stored in the memory. This mode is initiated by the following key sequence after entering the normal mode.

1. Push the "ML" key.
2. Push the single digit key corresponding to the desired address location.

The number is displayed as it is dialed out. In the tone mode, the tone driver rate is dependent on the time base as described earlier.

Pause

Note that the out dialing in the repertory or redial operation continues unless an access pause is detected. The outpulsing will stop and resume only when the user terminates the access pause by pushing the "ML" key again.

Program Modes (P/$\overline{N}$ = high, Reset = low)

Storing of a Telephone Number into the External Memory

During the store operation no out-dialing occurs. A telephone number can be stored in the desired address location by initiating the following key sequence.

1. Push the "ML" key (This instructs the device to accept a new number for storage into the internal memory.)
2. Enter the digits (including any access pauses) corresponding to the desired number. Digits will be displayed as they are entered.
3. Push the "ST" key.
4. Push the single digit key corresponding to the desired address location.

The entire sequence can be repeated to store as many numbers as desired. However, any memory locations not addressed with a telephone number "store" operation must be addressed with the following sequence.

1. Push the "ML" key.
2. Push the "ST" key.
3. Push the single digit key corresponding to the first unused memory location.
4. Push the "ST" key.
5. Push the single digit key corresponding to the next unused memory location.

Steps 4 and 5 are repeated until all remaining memory loccations have been addressed.

It should be noted that accessing all memory locations is required only for initial system set-up. This insures that no memory location will contain invalid data from memory power-up induced data and that location was addressed by the S2563, the S2563 would enter a "Halt" state and cease its normal program activities. To exit from this condition it is necessary to apply a momentary reset signal or toggle the P/$\overline{N}$ input.

Memory Expansion

The memory can be expanded by paralleling additional S5101 RAM's. External logic must be used to enable the desired RAM corresponding to a desired address location. The S2563 can drive up to 2 RAM's without the need of buffering address and data lines.

Keybounce Protection

When a key closure is detected by the S2563, an internal timeout (4ms at fo = 8kHz) is started. Any transitions that occur during this timeout will reset the timer to zero so that a key will only be accepted as valid after a noise free timeout period. The key must remain closed for an additional 16ms before released. Thus, the total make time of the key must be at least 20ms. The key must be released for at least 1ms before a new key is activated. Any transitions occurring when the key is released are ignored as long as the make time does not exceed 4ms.

Keyboard Entry Options

Figure 4 shows various options for arrangement of a keyboard for dialing of up to 29-8 digit or 15-16 digit numbers. A single S5101 memory is sufficient for number storage in the basic scheme.

Application Examples

Figures 6 and 8 respectively show the typical hookup schematics for the local power and telephone line power applications. Since power is available in the on-hook state of the telephone, store and display operations can be performed in this state for the local power application. In the telephone line power application, however, the device is put in the power-down mode to meet the on hook telephone leakage current specifications (5μA max). Store operation is performed in the off hook state by either storing the number after it is dialed out or by putting the device in the program mode by using a Prog/Norm switch. In this mode numbers can be stored without actually dialing them.

Table 1. Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 5.0V.
Keyboard (R_1-R_6, C_1-C_6)	12	These are 6 row and 6 column inputs from the keyboard contacts. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect to each other. Figures 1 and 2 depict the standard telephone DPCT and X-Y matrix keyboard arrangements that can be used. A logic, interface is also possible as shown in Figure 3. Debouncing is provided to avoid false entry. Key pad entry options are shown in Figure 4.
Number Length Select (NLS)	1	This permits programming of the device to accept either 8-digit numbers or 16-digit numbers.
Mode Select (MODE)	1	This input allows the use of the device in either dial pulsing applications or tone drive applications.
Dial Rate Select (DRS)	1	This input allows selection of two different dialing rates such as 10 or 20 pps, 7 or 14 pps, etc. See Tables 2 and 3.
Inter-Digit Pause Select (IPS)	1	This allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceeding the first dialed digit is an inter-digit time equal to the selected IDP. Two pause durations, either 400ms or 800ms are available at dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Mark/Space Ratio Select (M/S)	1	This input allows selection of two mark/space ratios. High (V_{DD}) level selects 40/60 and low (V_{SS}) level selects 33/67.
Mute Output ($\overline{MUTE}$)	1	A pulse is available that can provide drive to turn on an external transistor to mute the receiver during dial pulsing. See Figure 5 for mute and dial pulse output relationship. It is also used as a keyboard disable in the tone drive applications. See Figure 6.
Dial Pulse Output ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. This output will be normally high and go low during "space" or "break."
Display Memory I/O Data (D_1-D_4)	4	These are 4 bidirectional pins for inputting and outputting data to the external memory and display driver.
Memory Enable (CE)	1	This line controls the external memory read/write functions in power down mode. It should be connected to the CE_2 input of the S5101 memory.
Memory Read/Write (R/$\overline{W}$)	1	This line controls the read or the write operation of the external memory. This output along with the CE output can be used to produce a pulse to update the external display. See Figure 6.
Tone Generator/Memory Address (A_0-A_7)	8	These are 8 output lines that carry the external memory address and tone generator row/column information.
Program/Normal (P/$\overline{N}$)	1	This input selects the operating mode. When high (V_{DD}) it puts the device in the program mode and numbers can be stored into memory. When low (V_{SS}) it allows normal operations.
Reset	1	This is a level reset input. When high (V_{DD}) the chip is forced into a power down mode.
Oscillator (OSC_i, OSC_m, OSC_o)	3	These pins are provided to connect external resistors R_I, R_M and capacitor C_O to form an R-C oscillator that generates the time base for the repertory dialer. The output dialing rate, tone drive rate and IDP are derived from this time base.
	40	

Table 2. Table for Selection of Oscillator Component Values for Desired Dialing Rate, I_{DP} or Tone Drive Rate

Dial Rate Desired (PPS)	Osc. Freq. fo (Hz)	Oscillator Components			Dial Rate (PPS)		IDP (ms)		Tone Drive On/Off Time (ms)
		R_M (kΩ)	(R_I) (kΩ)	C_O (pF)	DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}	
5.5/11	4400	TBD	1000	300	5.5	11	1454	727	90/90
6/12	4800	220			6	12	1334	667	83.3/83.3
6.5/13	5200	190			6.5	13	1230	615	77/77
7/14	5600				7	14	1142	571	71/71
7.5/15	6000				7.5	15	1066	533	66.7/66.7
8/16	6400				8	16	1000	500	62.5/62.5
8.5/17	6800	TBD			8.5	17	942	471	59/59
9/18	7200				9	18	888	444	55.5/55.5
9.5/19	7600				9.5	19	842	421	52.6/52.6
10/20	8000	110			10	20	865	405	54/55.5
(fo/800/ (fo/400)	fo				fo/800	fo/400	$\frac{6400 \times 10^3}{fo}$	$\frac{3200 \times 10^3}{fo}$	$\frac{400 \times 10^3}{fo}$/$\frac{400 \times 10^3}{fo}$

Figure 1. Standard Telephone Pushbutton Keyboard

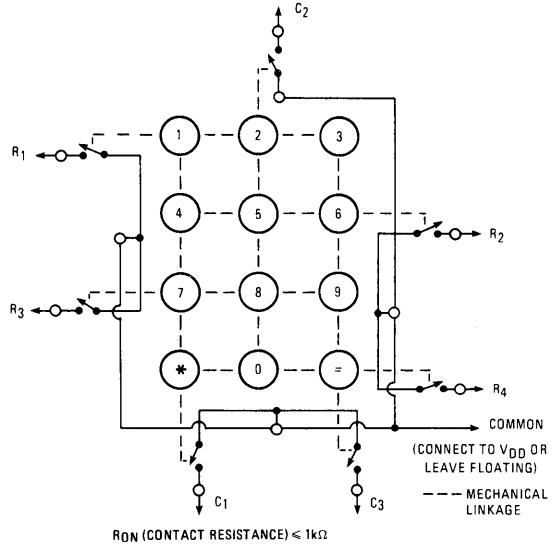
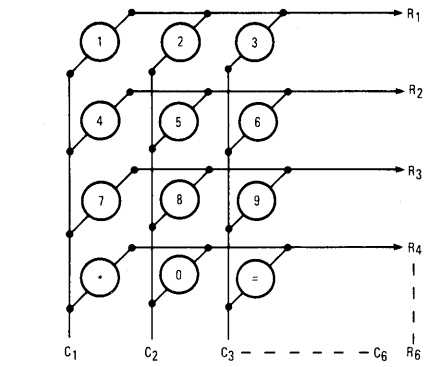


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 12 Row, Column Format



SPST MATRIX KEYBOARD:

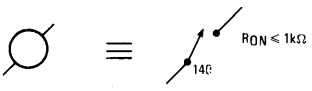
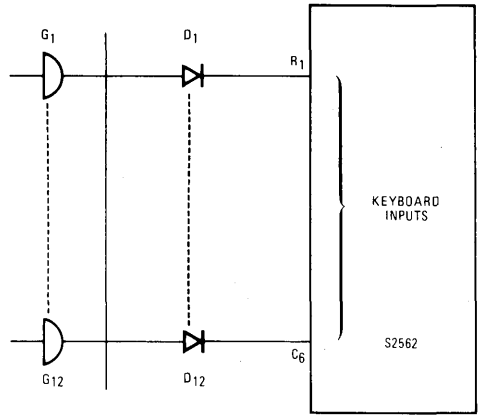


Figure 3. Logic Interface For The S2563



G_1 through G_{12} any CMOS type logic gates.
D_1 through D_{12} DIODES type 1N 914. (Optional)

A valid key closure corresponds to a logic high level on one row and one column

Figure 4. Example of Keypad Entry—Options
A. Using a Full Keyboard Provides Storage for 29-8 Digit Numbers

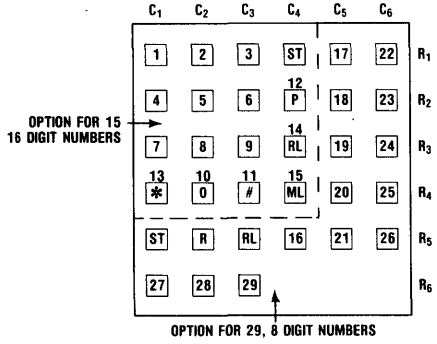


Figure 4B. Using a 4×4 Keyboard Provides Storage for 15-16 Digit Numbers

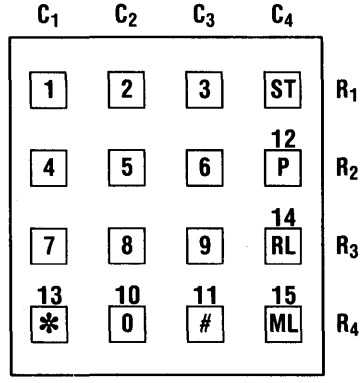


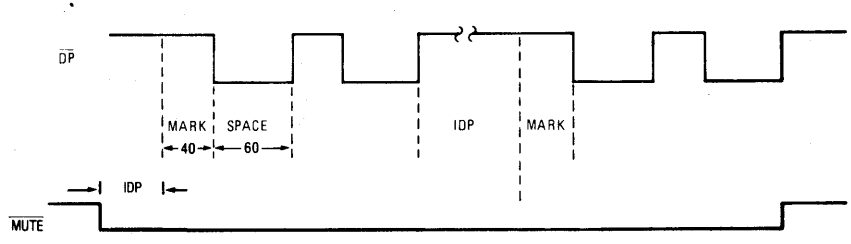
Table 3

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS} V_{DD}	(fo/800) pps (fo/400) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	(3200/fo) S (6400/fo) S
Mark/Space Ratio Selection	M/S	V_{SS} V_{DD}	33/67 40/60
Program/$\overline{\text{Normal}}$	P/$\overline{\text{N}}$	V_{DD} V_{SS}	Program Normal
Mode Selection	MODE	V_{SS} V_{DD}	Dial pulse Tone Drive*
Number Length Selection	NLS	V_{SS} V_{DD}	8 digits 16 digits
Reset	Reset	V_{SS} V_{DD}	Normal Operation Power Down

*For tone mode also set DRS = V_{SS}, IPS = V_{SS} and M/S = V_{DD}.

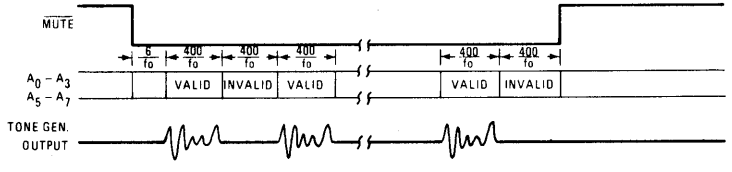
Note: fo is the oscillator frequency and is determined as shown in Table 2.

Figure 5A. Mute and Dial Pulse Output Timing Relationship



$\overline{\text{Mute}}$ will reset i) when the number of digits dialed out equals either the number of digits entered or the maximum selected (8 or 16) or ii) when an access pause is detected.

Figure 5B. Mute and Tone Output Timing Relationship



Mute output will reset i) when the number of digits dialed out equals the number of digits entered or equals the maximum selected (8 or 16) or ii) when an access pause is detected. In the normal dialing mode when digits are entered one at a time the mute output will reset between digits provided the time between entered digits exceeds $\frac{400}{fo}$. In both the normal dialing or automatic dialing mode tone will be output for a fixed duration of $\frac{400}{fo}$ (50msec for fo = 8kHz).

Table 4. Connection Table for Different Applications

Application	Pin	Connect to: (See figure below)
Telephone Line Power	P/N	Program/Normal Switch
	Reset	Hook Switch On Hook = V_{DD} Off Hook = V_{SS}
Local Power	P/N	Hook Switch On Hook = Program Mode (V_{DD}) Off Hook = Normal Mode (V_{SS})
	Reset	Hook Switch Power on reset circuit applying a momentary high level on power up or permanently connect to V_{SS}

Figure 6A. Local Power

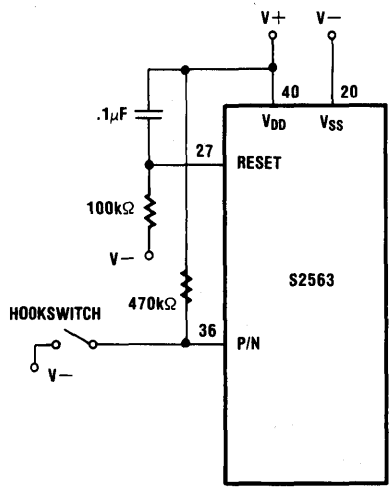


Figure 6B. Telephone Line Power

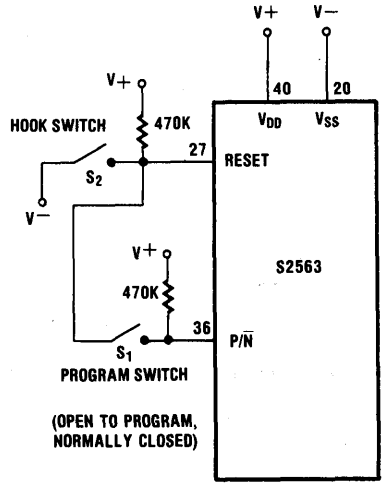


Figure 7. Typical Application of the S2563

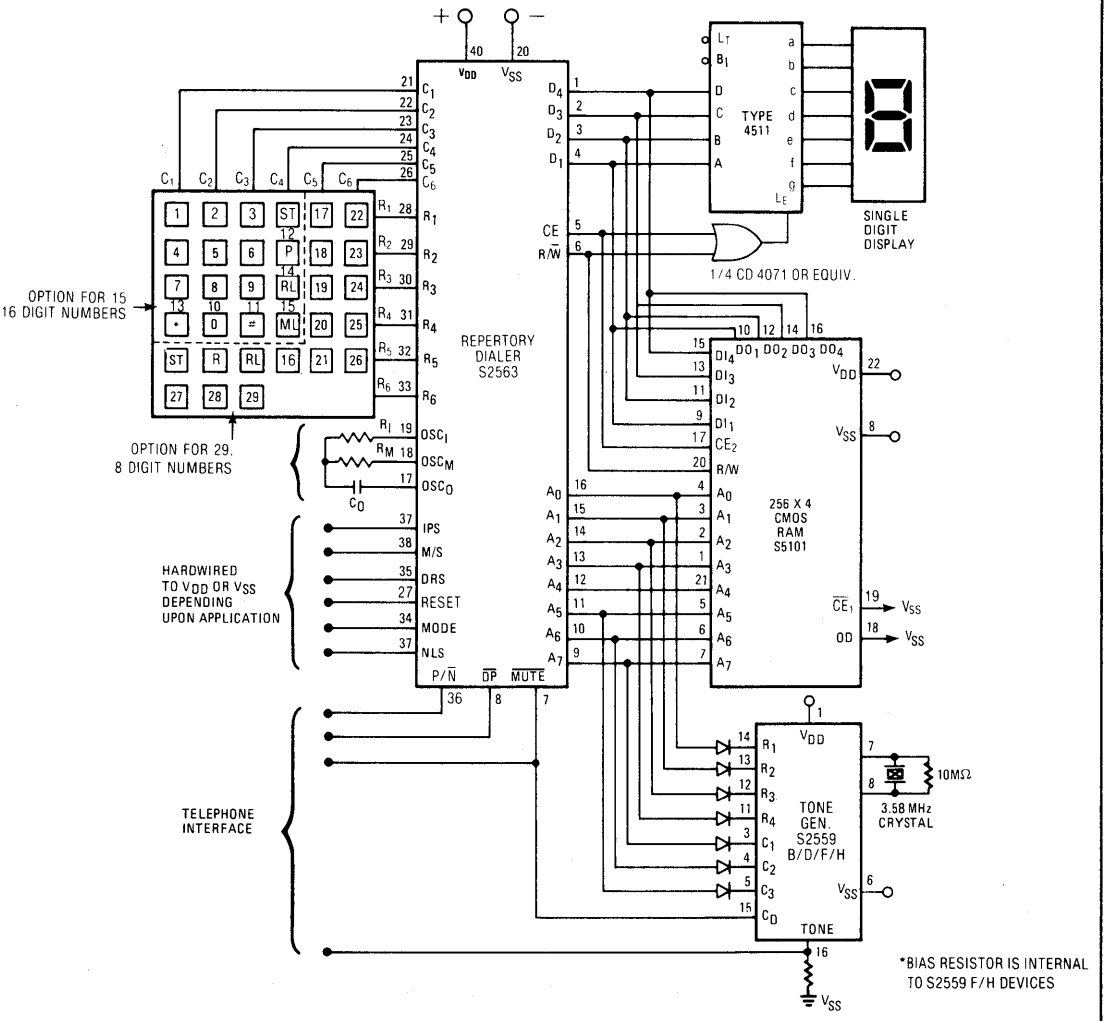


Table 5. Display Codes

Value Stored in Memory				Digit Value	Value Stored in Memory			
D_4	D_3	D_2	D_1		D_4	D_3	D_2	D_1
0	0	0	0	0	1	0	1	0
0	0	0	1	1	0	0	0	1
0	0	1	0	2	0	0	1	0
0	0	1	1	3	0	0	1	1
0	1	0	0	4	0	1	0	0
0	1	0	1	5	0	1	0	1
0	1	1	0	6	0	1	1	0
0	1	1	1	7	0	1	1	1
1	0	0	0	8	1	0	0	0
1	0	0	1	9	1	0	0	1
1	0	1	0	Not Used	0	0	0	0
1	0	1	1	Not Used	0	0	0	0
1	1	0	0	# (Pause)	1	1	0	0
1	1	0	1	Not Used	0	0	0	0
1	1	1	0	Beginning of Number	0	0	0	0
1	1	1	1	Blank	0	0	0	0

Table 6. Operating Sequences

1. **NORMAL DIALING**

   P/$\overline{N}$→NORM, [D_1], --- [D_n]

2. **ENTERING ACCESS PAUSE**

   ACCESS PAUSE ENTERED BY PUSHING [P] DURING NORMAL DIALING

3. **STORING OF A NUMBER AFTER DIALING**

   P/$\overline{N}$→NORM, [D_1] --- [D_n] —WAIT FOR DIALING TO COMPLETE— [ST], [LOC_n]

4. **REDIALING**

   P/$\overline{N}$→NORM, [RL]

5. **OVERRIDING ACCESS PAUSE**

   ACCESS PAUSE IS OVERRIDEN BY PUSHING [ML] TO CONTINUE FURTHER DIALING DURING A REPERTORY OR REDIALING SEQUENCE.

6. **REPERTORY DIALING**

   P/$\overline{N}$→NORM, [ML], [LOC_n]

7. **CASCADING NUMBERS IN REPERTORY DIALING**

   P/$\overline{N}$→NORM, [ML], [LOC_1] —WAIT FOR DIALING TO COMPLETE— [ML], [LOC_2] — etc.

8. **STORING OF NUMBERS IN MEMORY**

   P/$\overline{N}$→PROG, [ML], [D_1] --- [D_n], [ST], [LOC_1], [ML], [D_1] --- [D_n], [ST] [LOC_2] — etc.

NOTES: **1)** Function keys [ML], [RL], [P], [*] and [#] also designate memory locations 15, 14, 12, 13 and 11 respectively. Number can be stored in these locations by using the function keys as address keys in the appropriate sequence. To store a number in loc. 15 for example this sequence can be used P/$\overline{N}$→PROG, [ML], [D_1] --- [D_n], [ST], [ML]

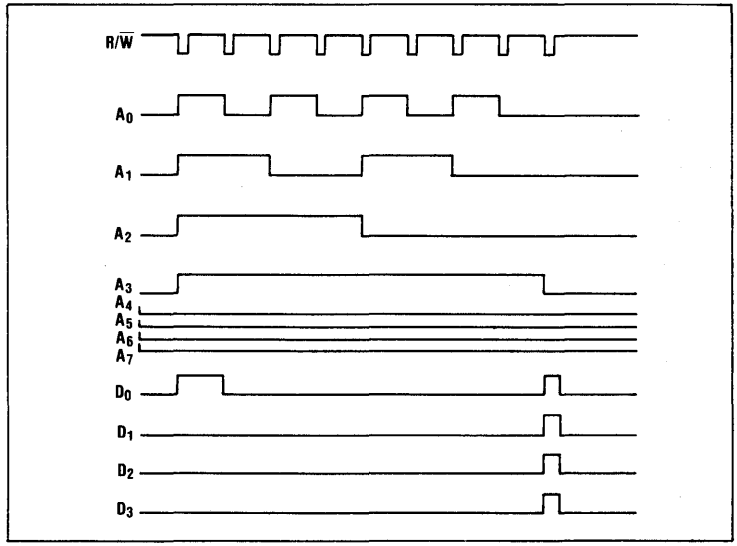
Similarly to dial a number stored in loc. 15 the following sequence can be used

P/$\overline{N}$→NORM, [ML], [ML]

Table 7. S2563 Memory Allocation

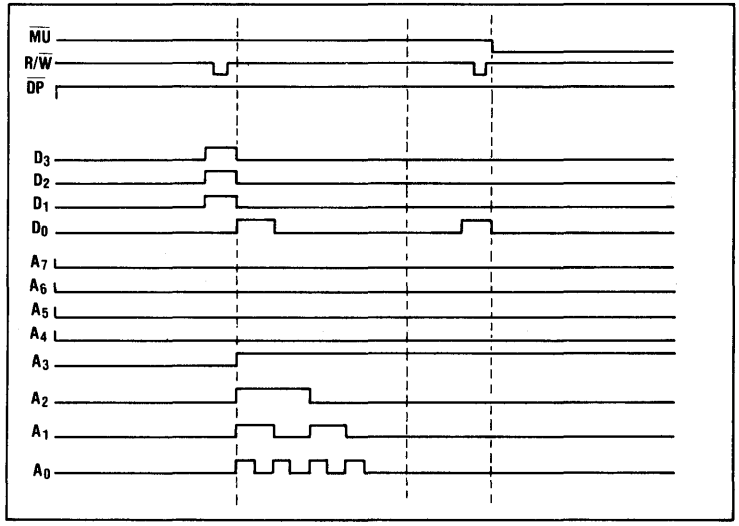
LOC.	ROW	COL.	8 DIGIT MODE MEM. ADDR. (HEX) D1 ..... D8		16 DIGIT MODE MEM. ADDR. (HEX) D1 ..... D16	
1	R1	C1	0F	08	1F	10
2	R1	C2	17	10	2F	20
3	R1	C3	1F	18	3F	30
4	R2	C1	27	20	4F	40
5	R2	C2	2F	28	5F	50
6	R2	C3	37	30	6F	60
7	R3	C1	3F	38	7F	70
8	R3	C2	47	40	8F	80
9	R3	C3	4F	48	9F	90
10	R4	C2	57	50	AF	A0
11	R4	C3	5F	58	BF	B0
12	R2	C4	67	60	CF	C0
13	R4	C1	6F	68	DF	D0
14	R3	C4	77	70	EF	E0
15	R4	C4	7F	77	FF	F0
16	R5	C4	87	80	0F	00
17	R1	C5	8F	88		
18	R2	C5	97	90		
19	R3	C5	9F	98		
20	R4	C5	A7	A0		
21	R5	C5	AF	A8		
22	R1	C6	B7	B0		
23	R2	C6	BF	B8		
24	R3	C6	C7	C0		
25	R4	C6	CF	C8		
26	R5	C6	D7	D0		
27	R6	C1	DF	D8		
28	R6	C2	E7	E0		
29	R6	C3	EF	E8		

Figure 8A.



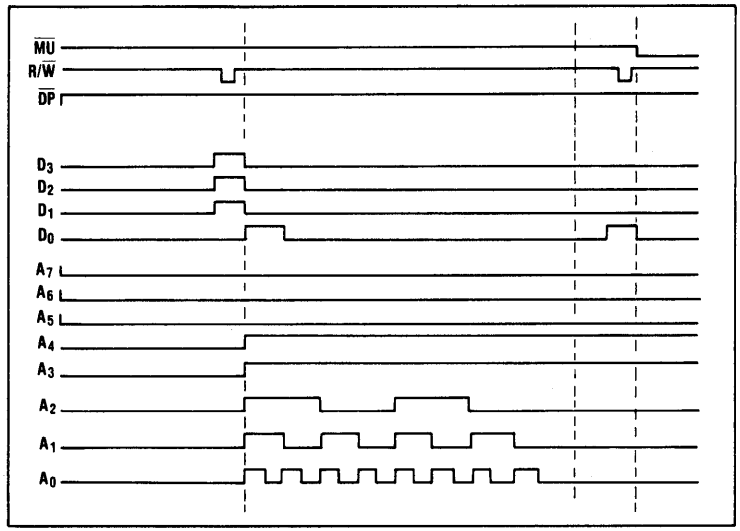
STORE INTO MEMORY
8 DIGIT MODE
LOCATION 1 DATA = 1

Figure 8B.



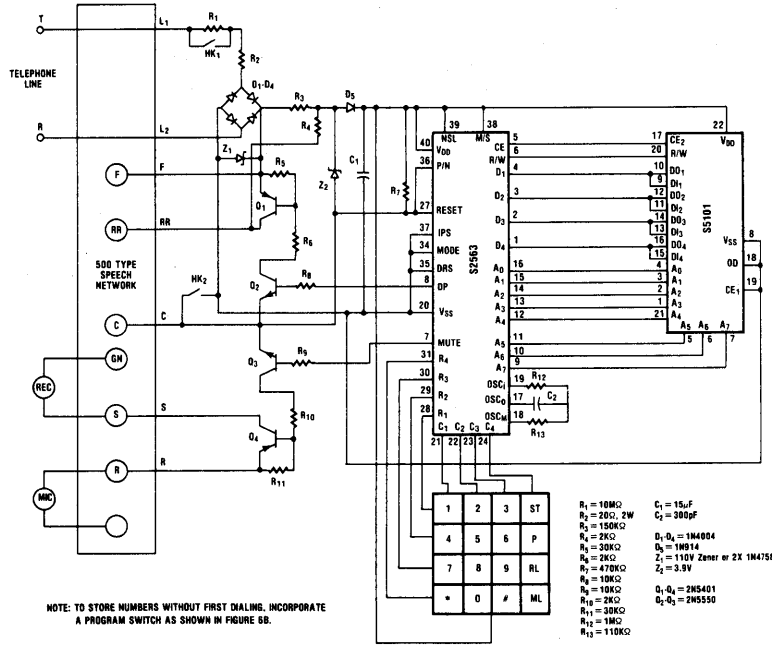
RECALL FROM MEMORY
8 DIGIT MODE
LOCATION 1

Figure 8C.



RECALL FROM MEMORY
16 DIGIT MODE
LOCATION 1

Figure 9. Typical Telephone Line Powered Repertory Dialer (Number Stored Offhook After Dialing is Completed)



NOTE: TO STORE NUMBERS WITHOUT FIRST DIALING, INCORPORATE A PROGRAM SWITCH AS SHOWN IN FIGURE 8B.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

RTDS2811

REAL-TIME DEVELOPMENT SYSTEM

Features

- ☐ **Provides Real-time (20MHz) Interactive Emulation for the AMI S2811 Signal Processing Peripheral**
- ☐ **Totally Self Contained (Internal Supply and Resident Software)**
- ☐ **Simple Interconnect Via RS232 to Port Users Terminal**
- ☐ **Full Software Capability Including Assembler and Editor**
- ☐ **In-Circuit Emulation Capability (Free Running with Breakpoints or Step-by-Step)**
- ☐ **Internal 6800 Based Microcomputer May be Used as Host Processor for S2811 Under Emulation**
- ☐ **Software Compatible with Software Simulator/ Assembler Program Package (SSPP2811)**

General Description

The RTDS2811 is a real-time in-circuit emulator for the AMI S2811 Signal Processing Peripheral (SPP). For information on the SPP chip please refer to the S2811 Advanced Product Description. The emulator is controlled from the user's terminal via the RS232 port at data rates up to 1200 bits/sec. The resident software package allows the user to load and assemble programs written in SPP Assembly language either from files or directly from the keyboard. The editor allows these programs to be modified by changing, inserting, or deleting instructions. The contents of the data memory may similarly be loaded from a file or created on-line and modified from the keyboard. Software switches control the interfaces to the emulator during emulation, allowing the system to be used as an in-circuit emulator in the user's prototype system, or to use the resident 6800 based microcomputer to operate as the host system. In the latter mode the system can be totally self-contained using file based I/O, eliminating the need to provide separate hardware for some phases of the emulation process. The system can be set to run continuously, conditionally, or step-by-step. In the conditional mode the system can be set to halt at breakpoints or on major flags (input, output, and overflow). The complete status of the system is displayed each time execution is halted, including in the step-by-step mode. Programs and memory maps created using the emulator can be used to generate the ROM mask for the S2811 by AMI.

Software generated by the RTDS2811 is totally compatible with the SSPP2811 Software Simulator/Assembler Program Package, allowing files to be transferred from one system to the other without modification.

SOFTWARE SIMULATOR/ASSEMBLER PROGRAM PACKAGE

Features

- ☐ **Provides Exact Simulation of Operation of AMI S2811 Signal Processing Peripheral**
- ☐ **Written in ANSI Fortran IV for Maximum Portability**
- ☐ **Runs on Any 16-Bit or Larger Computer With 28K Memory and Fortran IV Compiler**
- ☐ **Available Internationally on National CSS Time-sharing Service**
- ☐ **Allows Continuous or Step-by-Step Operation**
- ☐ **Allows Setting of Breakpoints on All Major Flags**
- ☐ **Trace Buffer Allows Storage and Display of Status of Previous 50 Instructions During Continuous Operation**
- ☐ **Software Compatible with Real-Time Development System (RTDS2811)**

General Description

The SSPP2811 is a software simulator for the AMI S2811 Signal Processing Peripheral (SPP). For information on the SPP chip please refer to the S2811 Advanced Product Description. The program is written in ANSI Standard Fortran for maximum portability. The machine specific software is reduced to a minimum and is available for several popular ranges of computers including Burroughs 7700, PRIME 400, and Amdahl 470 (IBM compatible). Experienced Fortran programmers will have no difficulty in writing these small routines for other machines. As well as being available in source code form on magnetic tape, the program is available already implanted on the National CSS, Inc. Timesharing Service. For information on the NCSS system please contact your local NCSS office.

The SSPP2811 package allows the user to simulate the operation of the S2811 chip either in a step mode or free running, with or without breakpoints. Data I/O for the simulation may be provided by means of files or directly from the terminal. An assembler allows the user to input the SPP program (in SPP Assembly Language) and the memory data either from a file or from the keyboard. The assembly listing may be dumped to file which can then be used to generate the ROM mask for the S2811 by AMI. During simulation a trace buffer may be used to store the last 50 (maximum) instructions executed. This greatly facilitates continuous simulation in conjunction with the breakpoints which may be set on (1) any individual instruction (2) the input flag (3) the output flag (4) overflow in the accumulator. The trace feature, either using the trace buffer or in the step-by-step mode, gives the user the complete status of the simulation, including the last instruction executed and the conditions of all internal registers, counters, latches, and busses.

Software generated by the SSPP2811 is totally compatible with the RTDS2811 Real-Time Development System, allowing files to be transferred from one system to the other without modification.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S28211A/B

SIGNAL PROCESSING PERIPHERAL

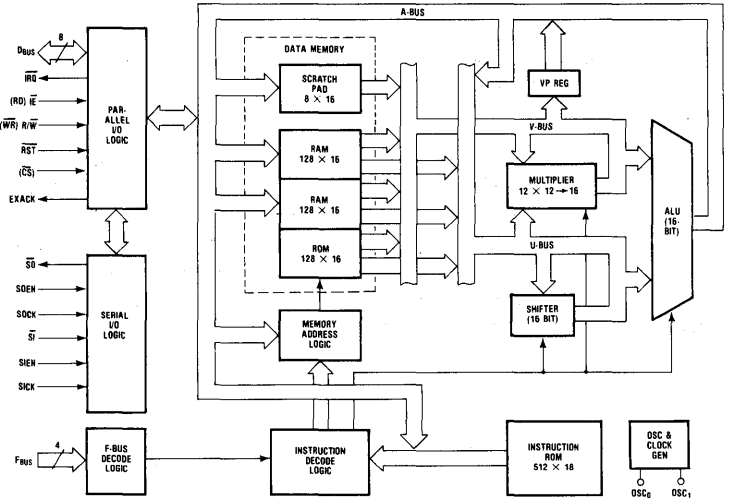
Features

- ☐ Single-Chip Programmable Digital Signal Processor
- ☐ May Be Customized (ROM Programmed) With Customer Generated Routines
- ☐ Self-Emulation Capability
- ☐ Standard Preprogrammed Processors Available
- ☐ Fetch/Multiply/Add/Store Cycle
- ☐ 512 Word × 18 Bit Instruction Memory
- ☐ Unique Three Port Data Memory 256 × 16 RAM/128 × 16 ROM
- ☐ 12 × 12 Pipelined Multiplier With 16 Bit Product
- ☐ 16 Bit Accumulator With Overflow Detect/Protect
- ☐ Double Buffered Asynchronous Serial I/O Port
- ☐ μP-Compatible I/O Port i.e. 6800 (A Version), 8080 (B Version), etc.

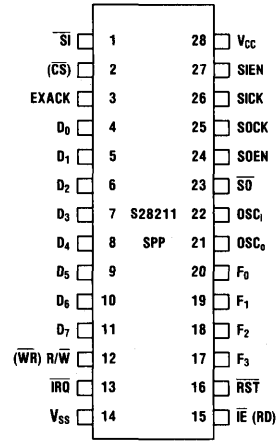
General Description

The S28211 is a single-chip microcomputer which has been optimized to execute digital signal processing algorithms commonly used in applications such as telecommunications speech processing, industrial process control instrumentation, etc. It may be used as a stand alone unit, or may be operated as a peripheral in a microprocessor based system. The latter configuration allows arrays of S28211s to be used together for increased processing throughput. The S28211's multi-bus, pipelined architecture and powerful multi-operation instructions make it possible to write very compact algorithms. This allows the available memory to be used efficiently and increases the execution speed of a given algorithm. The S28211 may be customized with user generated algorithms (Factory ROM Programmed). A selection of support tools

Simplified Block Diagram



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

(Assembler, Simulator, Real-time Emulator) are available for this task. In addition, a family of pre-programmed S28211s are available for standard applications.

Functional Description

The main functional elements of the S28211 (see Block Diagram) are:

1. a 512 × 18 ROM which contains the user program.
2. a 3-port 384 × 16 data memory (one input and two output ports) which allows simultaneous readout of two words.
3. a 12-bit × 12-bit high-speed parallel multiplier with 16-bit rounded product.
4. an Arithmetic/Logic Unit (ALU).
5. I/O and control circuits.

The S28211 is implemented in a combination of clocked and static logic which allows complete overlap of the multiply operation with the read, accumulate, and write operations. The basic instruction cycle is Read, Modify, Write, where the "Read" brings the operands from the data memory to the multiplier and/or the ALU, the "modify" operates on those operands and/or the product of the previous operands, and the "Write" stores the result of the "Modify." The cycle time for the instruction is 300 nanoseconds. This results in an arithmetic throughput of about 3.3 multiply and accumulate operations per microsecond.

The S28211 is intended to be used as a microprocessor peripheral. The S28211 control interface is directly compatible with the 6800 microprocessor bus (A version) or 8080/8085/Z80 microprocessor bus (B version), but can be adapted to other 8-bit microprocessors with the addition of a few MSI packages.

Operating in a microprocessor system, the S28211 can be viewed as a "hardware subroutine" module. The microprocessor can call up a "subroutine" by giving a command to the S28211. A powerful instruction set (including conditional branching and one level of subroutine) permits the S28211 to function independently of the microprocessor once the initial command is given. The S28211 will interrupt the microprocessor upon completion of its task. The microprocessor is free to perform other operations in the interim.

The S28211 contains a high-speed serial port for direct interface to an analog-to-digital (A/D) converter. In many applications, real-time processing of sampled analog data can be performed within the S28211 without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the S28211 processing.

Separate input and output registers exchange data with the S28211 data ports. Serial interface logic optionally converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

The S28211 is a memory-mapped peripheral, occupying 16 locations of the microprocessor memory space. Selecting the correct S28211 address will activate the corresponding control mode.

The control modes and the LIBL instruction enable real-time modification of the S28211 programs. This permits a single S28211 program to be used in several different applications. For example, an S28211 might be programmed as a "universal" digital filter, with cutoff frequency, filter order, and data source (serial or parallel port) selected at execution time by the control microprocessor.

AMERICAN MICROSYSTEMS, INC.

Please note: the S2814A has been replaced with the S28214 which is an NMOS direct pin for pin electrical and functional replacement for the S2814A.

S2814A

FAST FOURIER TRANSFORMER

Features

- ☐ Based on AMI's Signal Processing Peripheral Chip (S2811)
- ☐ Performs 32 Complex Point Forward or Inverse FFT in 1.3msec, Using Decimation in Frequency (DIF)
- ☐ Transform Expandable either by Using Multiple S2814As (for Minimum Processing Time) or by a Single S2814A (for Minimum Hardware)
- ☐ Operates with any 8 or 16 Bit Microprocessor, including S6800 and S9900. Optional DMA Controller Increases Speed
- ☐ All Data I/O Carried Out on Microprocessor Data Bus
- ☐ Basic Resolution of 57dB. Optional Conditional Array Scaling (CAS) Routine Increases Dynamic Range to 70dB
- ☐ Optional Windowing Routine Incorporated to Permit Use of Arbitrary Weighting Function
- ☐ Coefficient Generation On Chip, with Rotation Algorithm for Transform Expansion up to 512 Points
- ☐ Optional Power Spectrum Computation

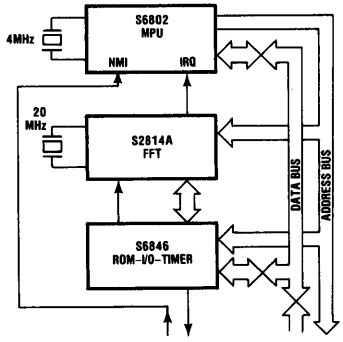
General Description

The AMI S2814A Fast Fourier Transformer is a preprogrammed version of the S2811 Signal Processing Peripheral. For further information on the internal operation of the S2811, please refer to the S2811 Advanced Product Description. It calculates FFTs and IFFTs using a decimation in frequency (DIF) technique for minimum distortion. The S2814A calculates a 32 complex point FFT using internally generated coefficients in a single pass. A coefficient rotation algorithm allows larger FFTs to be implemented (in blocks of 32 points). This implementation may be carried out by successive passes of the data through the two main routines in the S2814A, allowing larger transforms to be carried out with a single S2814A. Alternatively, an array of S2814As may be used to increase the transformation speed by parallel processing.

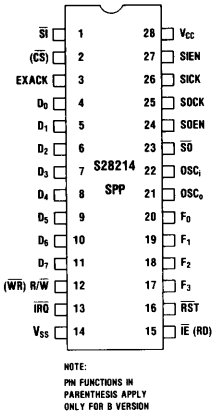
The word length used in the S2814A gives the transformed data a resolution of up to 57dB, but the total dynamic range can be increased up to 70dB by using the Conditional Array Scaling (CAS) routine incorporated.

The S2814A is intended to be used in a microprocessor system (see Block Diagram), using an 8 or 16 bit microprocessor, ROM, RAM and an optional DMA Controller or Address Generator. The S2814A is used as a

Block Diagram: Minimum System Configuration



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

memory mapped peripheral, and should be assigned a block of 16 addresses. It is used as a "hardware subroutine" function. The microprocessor controls the flow of data, including I/O, and calls the routines in the S2814A to cause the FFT to be executed. The S2814A responds to the microprocessor with the $\overline{IRQ}$ line when the processing of each routine is completed. In the case of a 32 point transform this signifies the completion of the transform, and in larger transforms it signifies that the microprocessor should unload the output data, load the next input data and call the next routine to be executed. The data is stored externally in RAM. Input data to be transformed is loaded into displacements 0 and 1 of the S2814A data memory. At the end of the FFT routine output data overwrites the input data. If power spectrum flag (PSF) is set, the S2814A computes the sum of the squares of the real and imaginary components of the output data and places the result in displacement 3 of the data memory. Both complex FFT data and power spectrum data are thus available. Windowing weights may be loaded into the S2814A prior to processing if the windowing routine is to be used. A 6800 compatible source listing of a suitable control program is available to the S2814A user at no charge. This control program will also be made available as a mask programmed ROM.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10sec.)	200°C

Electrical Specifications (V_{CC} = 5.0V ± 5%; V_{SS} = 0V, T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.0		V_{CC}+0.3	V	V_{CC} = 5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC} = 5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μA	V_{IN} = 0V to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD} = −100μA, V_{CC} = min, C_L = 30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD} = 1.6mA, V_{CC} = min, C_L = 30pF
f_{CLK} (max)	Maximum Clock Frequency				MHz	V_{CC} = 5.0V
	S2814A-10	10				
	S2814A-12	12				
	S2814A-15	15				
	S2814A	20				
P_D	Power Dissipation		1.2		W	V_{CC} = 5.0V

S2814A Pin Functions/Descriptions

Pin	Number	Function
D_0-D_7	4-11	(Input/Output) Bi-directional 8-bit data bus. Data is Two's Complement coded.
F_0-F_3	20-17	(Input) Control Function bus. Four Microprocessor address lines (typically A_0-A_3) are used to control the S2814A.
$\overline{IE}$	15	(Input) Interface Enable. A low level on this line enables data transfer on the data bus and control functions on the F-bus. Usually generated by microprocessor address decode logic.
R/$\overline{W}$	12	(Input) Read/write select. When HIGH, output data from the S2814A may be read, and when LOW data may be written into the S2814.
$\overline{IRQ}$	13	(Output) Interrupt Request. This open drain output goes low when the S2814A has completed the execution of a routine and output data is available.
$\overline{RST}$	16	(Input) When LOW all registers and counters will be cleared, including the program counter, and all control functions cleared.
OSC_i, OSC_0	22,21	Oscillator input and output. For normal operation a crystal is connected bet- ween these pins to generate the internal clock signals. Alternatively, an external square wave signal may be connected to OSC_0 pin with OSC_i pin left open. All timings shown in this Product Description assume a 20MHz clock frequency.
V_{CC}	28	Positive power supply connection.
V_{SS}	14	Negative power supply connection. Normally connected to ground.

In addition to the above, pins 23-27 and 1 are connected internally. They should all be tied to V_{SS} during normal operation. Do not make connections to pins 2 and 3.

Functional Description

The S2814A is a pre-programmed version of AMI's S2811 Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters. For more detailed information about the chip, please refer to the S2811 Advanced Product Description.

The S2814A Instruction ROM contains the various routines which make up the FFT package. The routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the coefficients required to execute the functions. 128 words of Data RAM are provided to hold the 32 point complex signal data during processing as well as the power spectrum of the output and various other parameters, including the total number of points in the desired transform. The memory is organized as a 32x4 matrix, with the data arranged in columns, as shown in Table 1B.

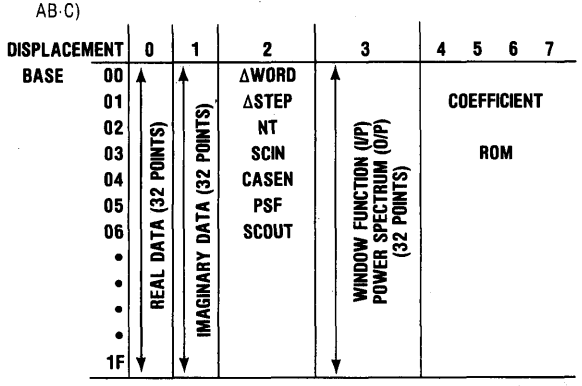
Table 1: Software Model of S2814A

A. Routine Locations in Instruction Memory

LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY PT. "INIT" ROUTINE
04	ENTRY PT. "FFT32" ROUTINE
D3	ENTRY PT. "COMPAS" ROUTINE
EA	ENTRY PT. "SCALE" ROUTINE
DC	ENTRY PT. "WINDOW" ROUTINE
E4	ENTRY PT. "CONJUG" ROUTINE

B. Data Memory Map

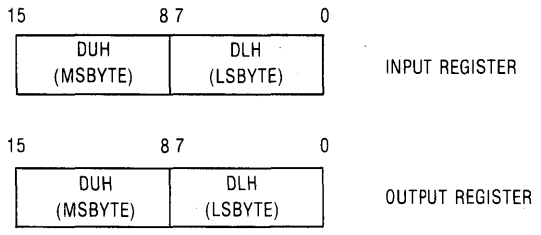
(Note: Address [Base AB, Displacement C] is written as AB·C)



C. Control Functions

F-BUS (HEX)	MNEMONIC	FUNCTION
1	RST	RESETS CHIP
2	DUH	SELECTS MSBYTE
3	DLH	SELECTS LSBYTE
4	XEQ	STARTS EXECUTION
9	BLK	SELECTS BLOCK MODE

D. Input and Output Registers



CODE IS TWO'S COMPLEMENT.

Initial Set-Up Procedure

After power up, the $\overline{RST}$ line should be held low for a minimum of 1 instruction cycle. If this line is connected to the reset line of the microprocessor this condition will be met easily. This will clear the Base and Index Registers, which are used for memory addressing, the Loop Counter and the Program Counter. Address zero in the Instruction ROM contains a Jump to Zero instruction, and thus the S2814A will remain in an idle state after being reset. Every routine in the memory is also terminated with a Jump to Zero instruction, and thus the S2814A will also remain in this same idle state after the the execution of each routine. The $\overline{IRQ}$ line will signal this condition each time, except after the initial reset and after execution of the INIT routine.

The Control Functions

The S2814A is controlled by the host microprocessor by means of the F-bus, Interface Enable ($\overline{IE}$) and the Read-Write (R/$\overline{W}$) lines. It should be connected to the host processor as a memory mapped peripheral as shown in Figure 1.

The 12 most significant address lines decode a group of 16 addresses to activate the $\overline{IE}$ line each time an address in the group is called, and the S2814A is controlled by reading to or writing from those addresses. Only 5 of these addresses are used as described in Table 2. Throughout this Product Description these addresses will be referred to as HHHX (X=0-F).

Figure 1. Connection of S2814A as a Memory Mapped Peripheral

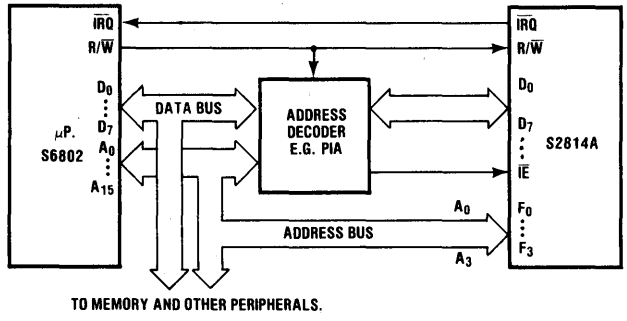


Table 2: S2814A Control Functions

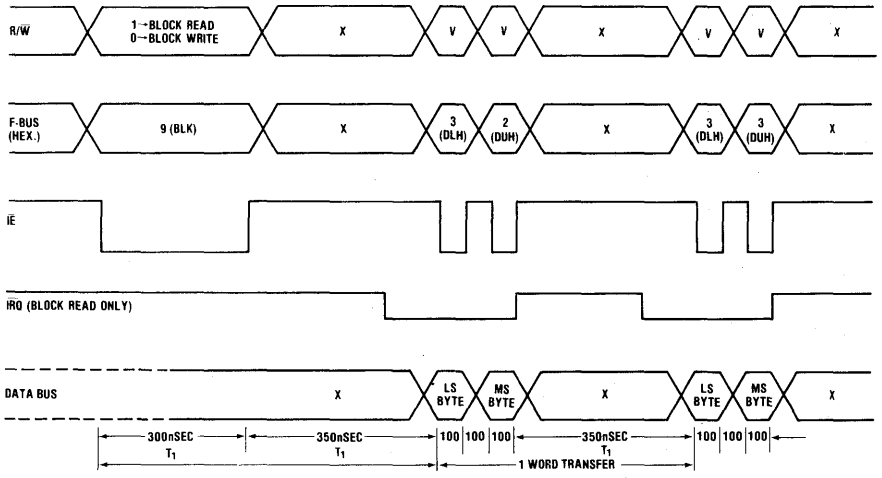
MNEMONIC	F-BUS HEX	DATA	TYPE OF OPERATION	FUNCTION
RST	1	XX	READ/ WRITE	CLEARS ALL REGISTERS. STARTS PROGRAM EXECUTION AT LOCATION 00. THIS IS THE IDLE STATE. THIS INSTRUCTION SHOULD PRECEDE BLOCK READ, BLOCK WRITE AND EXECUTE COMMANDS.
DUH	2	HH	READ/ WRITE	READS FROM OR WRITES INTO S2814A THE UPPER HALF OF THE DATA WORD. (SEE TABLE 1.D.)
DLH	3	HH	READ/ WRITE	READS FROM OR WRITES INTO S2814A THE LOWER HALF OF THE DATA WORD. (SEE TABLE 1.D)
XEQ	4	HH	WRITE	STARTS EXECUTION AT LOCATION HH
BLK	9	XX	READ/ WRITE	INITIATES A BLOCK READ OR BLOCK WRITE OPERATION. THE ENTIRE DATA RAM CAN BE ACCESSED SEQUENTIALLY BEGINNING WITH VALUES OF BASE AND DISPLACEMENT INITIALIZED USING "BLOCK TRANSFER SET UP" ROUTINE. IF A RESET OPERATION IS PERFORMED PRIOR TO BLOCK COMMAND THE DATA MEMORY ADDRESS IS INITIALIZED TO BASE 0, DISPLACEMENT 0. BLOCK READ OR WRITE OPERATION CAN BE TERMINATED ANY TIME BY PERFORMING A RESET OPERATION. THE INDEX REGISTER IS USED TO ADDRESS THE MEMORY DURING BLOCK TRANSFER AND INTERNAL ADDRESSING IS SEQUENCED AUTOMATICALLY.

NOTE: XX = Don't care
HH = 2 Hex characters (8-bit data)

The Block Transfer Operation

Block transfer is the mode used to load and unload the main data blocks into the S2814A at up to 4Mbytes/sec. In this mode the data memory is addressed by the Index Register, and after initialization the internal addressing is sequential and automatic. The sequence generated is that after each word transfer (16-bit words as 2 bytes, or 8-bit words as MSbyte (DUH) only) the base is incremented. After base 1F (31) has been reached, the base resets to 00 and the displacement increments. After base 1F displacement 3 has been reached (i.e., the highest address in the RAM, 1F.3), both base and displacement reset to zero. Note that when the BLK command is given the Read/Write line is latched internally, and remains latched until the RST command is given. The block transfer sequence and timing are shown in Figure 2. When using a microprocessor to execute the block read it will normally be advantageous to set the interrupt mask.

Figure 2. Block Transfer Sequence and Timing



NOTE 1: X = DON'T CARE, OR NOT VALID V = VALID

NOTE 2: ALL TIMES SHOWN ARE MINIMUM AND MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS AS FOLLOWS:

$$T_{1\,MIN} = \left[\frac{6000}{f_{CLK}} + 50\right] \text{ nsec}$$

In 6800 Assembly Language a Block Write would be executed with the following code:

```
LDX     OFFST   ;LOAD MEMORY START ADDRESS INTO INDEX REG.
STA   A BLK     ;WRITE DUMMY DATA TO ADDRESS $HHH9,BLOCK MODE.
LDA   A 0,X     ;READ FIRST BYTE FROM MEMORY.
STA   A DLH     ;WRITE INTO S2814A AS LSBYTE. ADDRESS $HHH3
LDA   A 1,X     ;READ SECOND BYTE FROM MEMORY.
STA   A DUH     ;WRITE INTO S2814A AS MSBYTE.ADDRESS $HHH2
LDA   A 2,X     ;SECOND WORD.
  .       .         .
  .       .         .
  .       .         .
LDA   A 62,X    ;32ND. WORD,LSBYTE.
STA   A DLH     ;
LDA   A 63,X    ;32ND. WORD,MSBYTE.
STA   A DUH     ;END OF TRANSFER.
STA   A RST     ;WRITE DUMMY DATA TO ADDRESS $HHH1.RESET.
```

Block Read would be executed by substituting LDA A for STA A, and vice versa.

where:

```
RST   EQU $HHH1
DLH   EQU $HHH3
DUH   EQU $HHH2
BLK   EQU $HHH9
```

The above code assumes that the block transfer is controlled by the host processor, not using DMA. Note that DLH must always precede DUH. 8-bit data may be transferred using DUH only, assuming that the significance of the data is correct.

The FFT Routines

Six individual routines are stored in the S2814A Instruction memory. Two or more of these are used in the computation of an FFT, depending on the transform size and the options selected. The starting addresses of the routines are shown in Table 3. All execution times quoted assume a 20MHz clock frequency.

Table 3. FFT Routines and Their Starting Addresses

LOCATION (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT FOR "INIT" ROUTINE
	(IR) = BASE, DISPLACEMENT
	$(BASE)_{4-0} \leftarrow (IR)_{15-11}, (DISP)_{1,0} \leftarrow (IR)_{9,8}$
	Returns to Idle state Exec. Time = 0.9μs
04	ENTRY POINT FOR "FFT32" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = SCIN, CASEN, PSF
	Perform 32 point FFT. Sets IRQ, Returns to Idle state. Exec. Time = 1.2 ms to 1.8ms.
	(OR) = SCOUT (DISP0) = Transformed Data (Real), (DISP1) = Transformed Data (Imag.) (DISP2) = SCOUT, (DISP3) = Power Spectrum Data if PSF = 1
D3	ENTRY POINT FOR "COMPAS" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = WORD, STEP, NT, SCIN, CASEN
	Perform COMPAS, Sets IRQ, Returns to Idle State Exec. Time = 233 to 374μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.) (DISP2) = SCOUT, (OR) = SCOUT
EA	ENTRY POINT FOR "SCALE" ROUTINE
	(IR) = SCLP, (DISP0) = Data (Real), (DISP1) = Data(Imag.)
	Performs scaling, Sets IRQ. Returns to Idle State Exec. Time = 51 to 250μsec.
	(DISP0) = Scaled Data (Real), (DISP1) = Scaled Data (Imag.)
DC	ENTRY POINT FOR "WINDOW" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP3) = Multiplying factors
	Performs multiplication, Sets IRQ, Returns to Idle State Exec. Time = 49μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.)
E4	ENTRY POINT FOR "CONJUG" ROUTINE
	No set-up required. Conjugates input data (negates imaginary components). Sets IRQ. Returns to Idle State. Exec. time = 30μsec.

1. Block Transfer Set-Up (INIT). Entry Address 01.

This routine presets the Index Register to allow block transfer to commence at any location other than 00.0 in the S2814A data RAM. An eight-bit word is loaded into the upper half of the input register and the routine executed as shown:

Figure 3A. Flowchart for Subroutine FT32IN

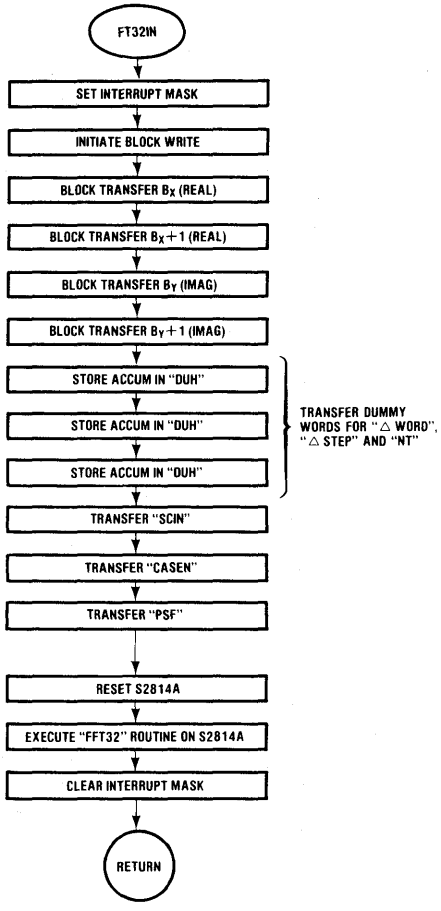
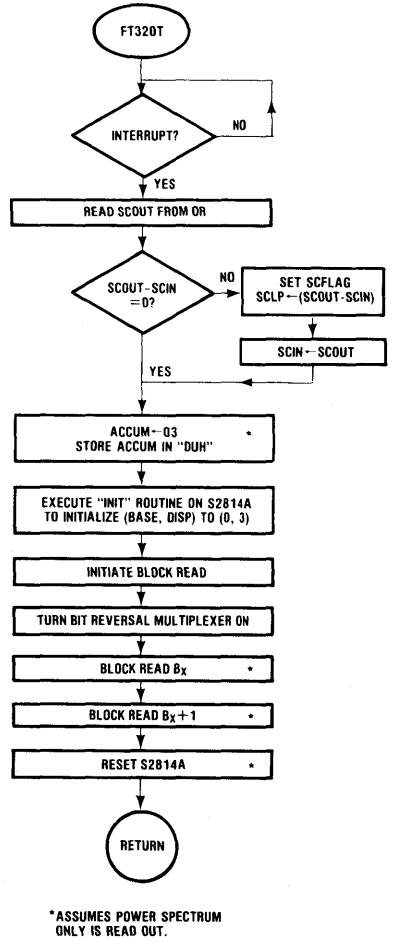


Figure 3B. Flowchart for Subroutine FT320T




```
DUH   EQU $HHH2
XEQ   EQU $HHH4


LDA   A #$XX
STA   A DUH
LDA   A #1
STA   A XEQ
```

where XX represents the start address for block transfer. (0.9μsec.) and the S2814A will return to the idle state. The routine will be executed in 3 instruction cycles Block transfer may then commence immediately.

2. FFT32. Entry Address = 04.

This is the basic 32 complex point FFT routine. For a 32 point FFT this routine is called once only and the output of the routine is the FFT. Larger FFTs are computed by decimating them into 32 point arrays before final processing of these arrays using FFT32 to obtain the final outputs. The following data is loaded into the S2814A, using block write starting at address 00.0, i.e., INIT is not used.

32 words of real input data (addresses 00.0 - 1F.0)

32 words of imaginary input data (addresses 00.1 -1F.1)

3 dummy words (to skip addresses) (addresses 00.2 -02.2)

SCIN (input scaling parameter) (address 03.2)

CASEN (CAS Enable) (address 04.2)

PSF (Power spectrum flag) (address 05.2)

Note that CASEN (Conditional array scaling enable) and PSF are not modified during processing, and need only be loaded once. CASEN should be positive to inhibit CAS (e.g. 0000) and negative to enable CAS (e.g. 8000). Note that SCIN is not needed if CAS is not enabled. PSF should be zero if the power spectrum output is not needed, any non-zero value (e.g. 0100) will cause the power spectrum to be computed. The block transfer should be terminated with the RST command, and the FFT32 routine called. Flow charts for loading and dumping the data are shown in Figure 3. The following sequence will cause the execution of the entire function:

```
CLR   B          ;CLEAR B ACC.
STA   A  RST     ;RESET S2814A REGISTERS.
SEI              ;SET INT. MASK.
STA   A  BLK     ;SET UP BLOCK WRITE.
JSR      BLKWT   ;WRITE 64 WORDS OF DATA.
STA   A  DUH     ;WRITE DUMMY DATA TO 00.0
STA   A  DUH     ;.....TO 00.1
STA   A  DUH     ;.....TO 00.2
LDA   A  SCIN    ;FETCH SCIN.
STA   A  DLH     ;WRITE TO ADDRESS 00.3
STA   B  DUH     ;COMPLETE WORD XFER.
LDA   A  CASEN   ;FETCH CAS ENABLE.
STA   A  DUH     ;WRITE TO ADDRESS 00.4
LDA   A  PSF     ;FETCH PS FLAG.
STA   A  DUH     ;WRITE TO ADDRESS 00.5
STA   A  RST     ;RESET S2814A.
LDA   A  #4      ;FFT32 START ADDRESS.
STA   A  XEQ     ;START EXECUTING.
CLI              ;CLEAR INT. MASK.
WAI              ;WAIT FOR ROUTINE END.
LDA   A  DLH     ;START OF INT. ROUTINE.
LDA   B  DUH     ;(DUMMY).READ SCOUT.
LDA   B  SCIN    ;FETCH SCIN.
STA   A  SCIN    ;SCOUT→SCIN
SBA              ;COMP.SCOUT WITH SCIN.
BEQ      READ    ;JUMP IF NO CHANGE.
STA   A  SCLP    ;(SCOUT-SCIN) → SCLP
LDA   A  PASSN   ;FETCH PASS #
CMP   A  #1      ;IS THIS 1ST.PASS?
BEQ      READ    ;IF SO, JUMP
JSR      SKOUT   ;SCALE PREVIOUS ARRAYS
LDA   A  #3      ;(ASSUME PSF SET
STA   A  DUH     ;PRESET TO ADDRESS 00.3
LDA   A  #1      ;
STA   A  XEQ     ;EXECUTE INIT.
STA   A  BRV     ;TURN ON BIT REV.MUX.
LDA   A  BLK     ;SET UP BLOCK READ.
JSR      BLKRD   ;READ DATA.
STA   A  RST     ;END
```

The routine execution time is variable, depending on whether CASEN and PSF are set. The times are:

1. CAS - OFF. PSF - OFF 3730 instruction cycles (1.119msec.)
2. CAS - OFF. PSF - ON 3862 instruction cycles (1.159msec.)
3. CAS - ON . PSF - OFF 5867max. instruction cycles (1.760msec.)
4. CAS - ON . PSF - ON 5999max. instruction cycles (1.800msec.)

When CAS is enabled, the time depends on the number of times overflow is corrected. At the end of the routine the complex output data will have overwritten the input data in the memory (addresses 00.0 to 1F.1) and the power spectrum data will be in displacement 3 (addresses 00.3 -1F.3). The output scaling factor (SCOUT) will be loaded in the output register, generating the $\overline{IRQ}$ to signify to the host processor that the routine has completed processing.

3. Combination Pass Routine, COMPAS. Entry Address = D3.

This is the decimation routine that breaks up larger transforms into a number of 32 point transforms to be executed by FFT32. The N data points are split into N/16 blocks of 16 points, and pairs of blocks are passed through COMPAS. The procedure is repeated one or more times if N is greater than 64, but for a 64 point FFT the resulting data is ready for processing using FFT32. The procedure is explained in greater detail in the section "Executing Larger Transforms". The following data is loaded into the S2814A before execution:

Figure 4A. Flowchart for Subroutine CSIN

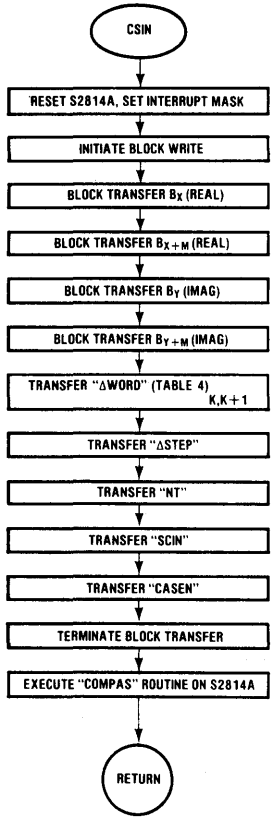
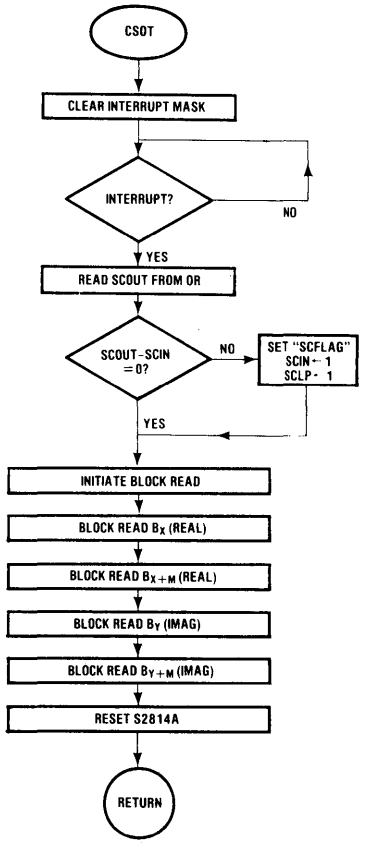


Figure 4B. Flowchart for Subroutine CSOT



32 words of real input data (addresses 00.0 - 1F.0)

32 words of imaginary input data (addresses 00.1 -1F.1)

Δ WORD (address 00.2)

Δ STEP Set up parameters (address 01.2)

NT (address 02.2)

SCIN (address 03.2)

CASEN (address 04.2)

^{D}SF (address 05.2)

The new parameters required, Δ WORD, Δ STEP and NT are dependent on the size of the transform and Δ WORD changes with each pass through the COMPAS routine. The values required are shown in the tables in sections "Executing 64 Point Transforms" and "Executing Larger Transforms". Flow charts for loading and dumping the data are shown in Figure 4. The routine execution time varies with transform size and depends on whether CAS is enabled or not, as shown:

TRANSFORM SIZE	64 POINT	128 POINT	256 POINT	512 POINT
Without CAS, Inst. cycles, (μsec.)	776 (233)	828 (248)	842 (253)	949 (255)
With CAS. (Max.) Inst. cycles (μsec.)	1172(352)	1224(367)	1238(371)	1245(374)

4. Data Point Scaling Routine, SCALE. Entry location = EA.

If CAS is enabled, then routines COMPAS, and FFT32 will scale all 32 data points being processed if an overflow occurs during that pass. The value of SCOUT allows the data during subsequent passes to be scaled automatically during the pass. However, data points which have already been processed must also be scaled, so that all the data is scaled by the same factor during each processing step. SCALE is a routine that allows this to be done at high speed. Each block to be scaled is block loaded into the S2814A, the routine SCALE executed, and the block dumped back into the original locations in memory.

Care must be taken to keep track of which blocks have already been processed during each step, so that blocks do not get missed or scaled twice. The execution time depends on the scaling factor (SCOUT), as shown below:

Scaling Factor (SCOUT)	1	2	3	4	5
Execution time. Inst. Cycles, (μsec.)	170(51)	336(101)	502(151)	668(200)	834(250)

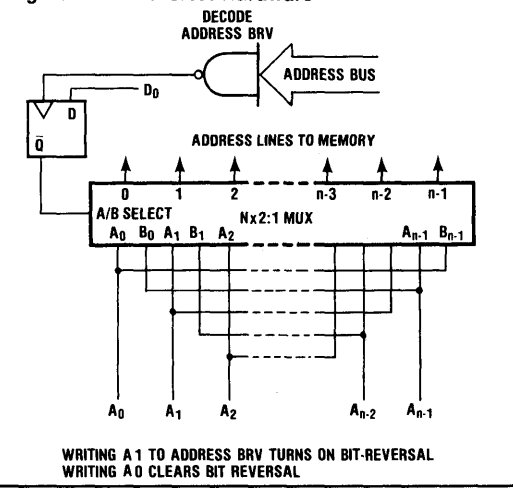
Windowing Routine, WINDOW. Entry Address = DC.

In order to allow the input data points to be windowed, a routine is provided to multiply the 32 real or complex points loaded in the S2814A by 32 window points. This is done on each block of 32 points prior to commencing the actual FFT processing. The input data required, in addition to the normal input data, are the 32 points of the window. They should be loaded into displacement 3 of the S2814A RAM and the routine WINDOW executed. The windowed data points will be returned to their original positions in the memory, so that COMPAS or FFT32 may then be executed immediately without further processing. The entire data can be loaded in a single block transfer operation by using INIT to preset the start address to 00.3. The 32 point window data is then loaded, followed by the signal data. This is possible because after loading the window the memory address will automatically reset to 00.0, the start address for the real data. The parameters are then loaded into displacement 2 addresses in the usual way. They will not be affected by the windowing operation. The total execution time is 163 instruction cycles, 49μsec.

Executing FFTs

Executing the FFTs consists of loading data blocks, executing routines in the S2814A and dumping the data. However, the sequence of the FFT output data is scrambled, and in order to use the results meaningfully, it must be unscrambled. This is done by reversing the order of the bits of the address lines for the final output data. Thus, for a 2^N point FFT the N address lines A_0, A_1, A_2 ..... A_{N-1} must be reversed to the sequence A_{N-1}, A_{N-2} ..... A_1, A_0 to address the output buffer memory. This is most conveniently done as the data points are being dumped out of the S2814A after the processing of the FFT32 routine(s). The bit reversal can be done either by software or hardware. The hardware realization is shown in Figure 5, and an example of software bit reversal is given in the section "Executing 32 Point FFTs."

Figure 5. Bit Reversal Hardware



Executing 32 Point Transforms

The basic 32 point transform is easily implemented with the S2814A since it simply requires the loading of the 32 real or complex data points and the 3 parameters SCIN, CASEN and PSF, executing FFT32 once only and dumping the data using bit reversal. The flowchart for this sequence is shown in Figure 6. It is assumed that the loading of data from the source into the input buffer and dumping of data from the output buffer to destination is carried out by the NMI (non-maskable interrupt) routine. The parameter SCIN should be set to zero, and the output data should be scaled (multiplied) by $2^{(SCOUT)}$ if absolute levels are wanted.

Figure 6. Flowchart for 32 Point FFT

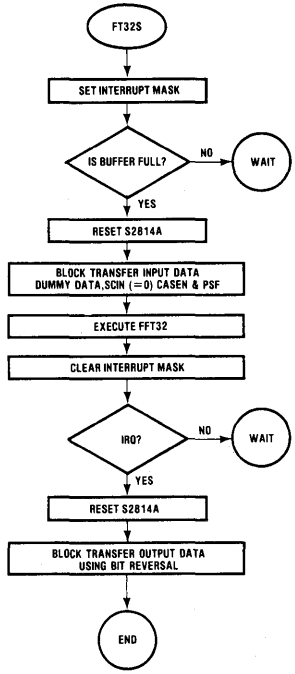
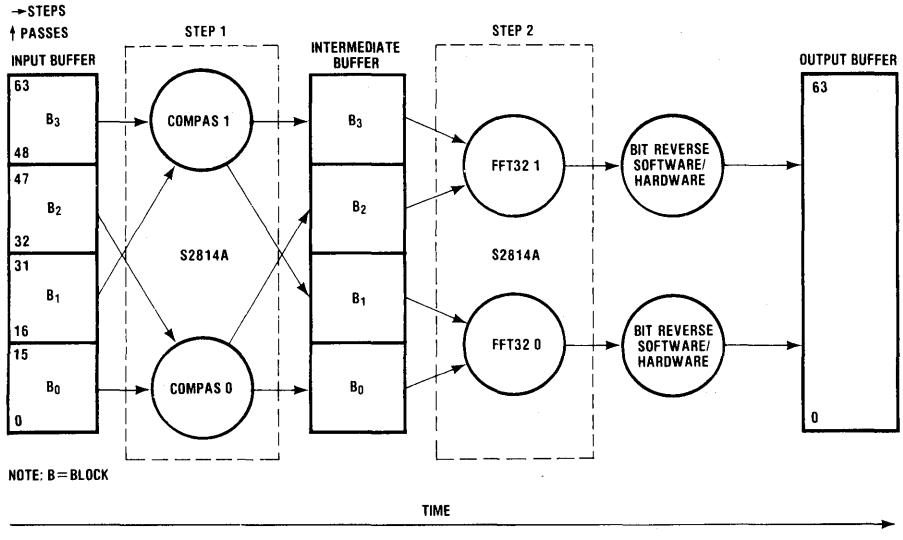


Figure 7. 64 Point FFT Flowgraph



Executing 64 Point Transforms

This is the simplest expansion of the FFT. The first step is to use COMPAS (twice) to decimate the data into two 32 point transforms, and then use FFT32 (twice) to produce the transforms. This is shown in the signal flow graph in Figure 7. The flow graph is independent of whether one or two S2814As are used, since the two passes through each of the 2 routines (COMPAS and FFT32) can be carried out sequentially or in parallel. The set up parameters for the 64 point FFT are:

For COMPAS 0: ΔWORD=8070
For COMPAS 1: ΔWORD=C070
} ΔSTEP=4000 NT=1

The treatment of SCIN and SCOUT is dealt with in the next section.

Executing Larger Transforms

The execution of larger transforms follows the same sequence as the 64 point transforms; namely the decimation of the data into a series of 32 point blocks that can be processed using FFT32. For a 2^N point FFT this involves N-5 steps of processing using COMPAS, and each step requires $2^{(N-5)}$ passes through the COMPAS routine. This is followed by $2^{(N-5)}$ passes through the FFT32 routine. Within each step, each pass may be carried out sequentially using a single S2814A, or in parallel using $2^{(N-5)}$ chips. There are also intermediate sequential + parallel combinations possible, of course, using fewer chips. A signal flow graph for 1 step is shown in Figure 8.

At the start of each step, SCIN should be set to zero. For the remaining passes in that step the value of SCOUT for the current pass should be used for SCIN for the next pass. The outputs of previously computed passes must be scaled using routine SCALE each time SCOUT increases during a pass. The maximum value of SCOUT after executing COMPAS is 1, and after executing FFT32 it is 5.

A flow chart for an N point transform control program is shown in Figure 9. The routine is called NFFT and uses the following subroutines.:

CSIN — procedure for loading S2814A with COMPAS input data (Figure 4A)
CSOT — procedure for dumping COMPAS output data (Figure 4B)
SCLPRV — procedure for scaling previously computed blocks of data in each step. See Figure 10.
FT32IN — procedure for loading S2814A with FFT32 input data (Figure 3a)
FT32OT — procedure for dumping FFT32 output data. (Figure 3b)

The values of ΔWORD, ΔSTEP and NT are shown in Tables 4 and 5.

Figure 8. N Point FFT Flowgraph

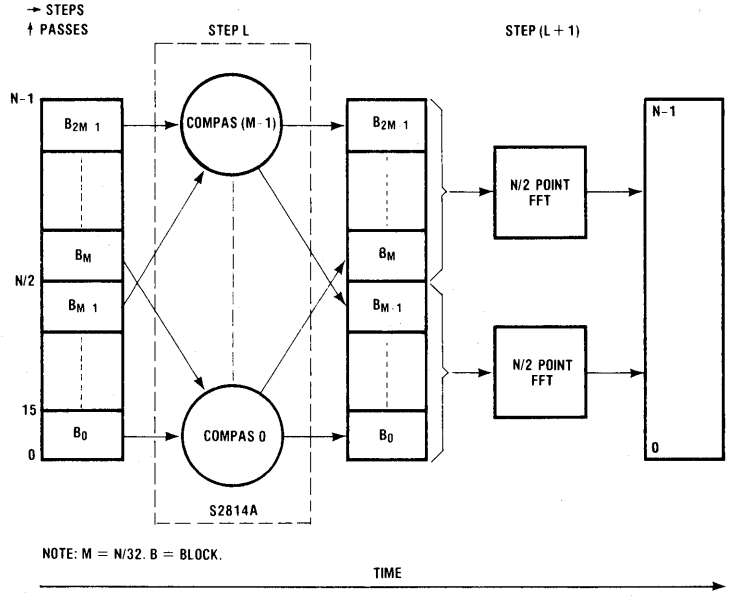
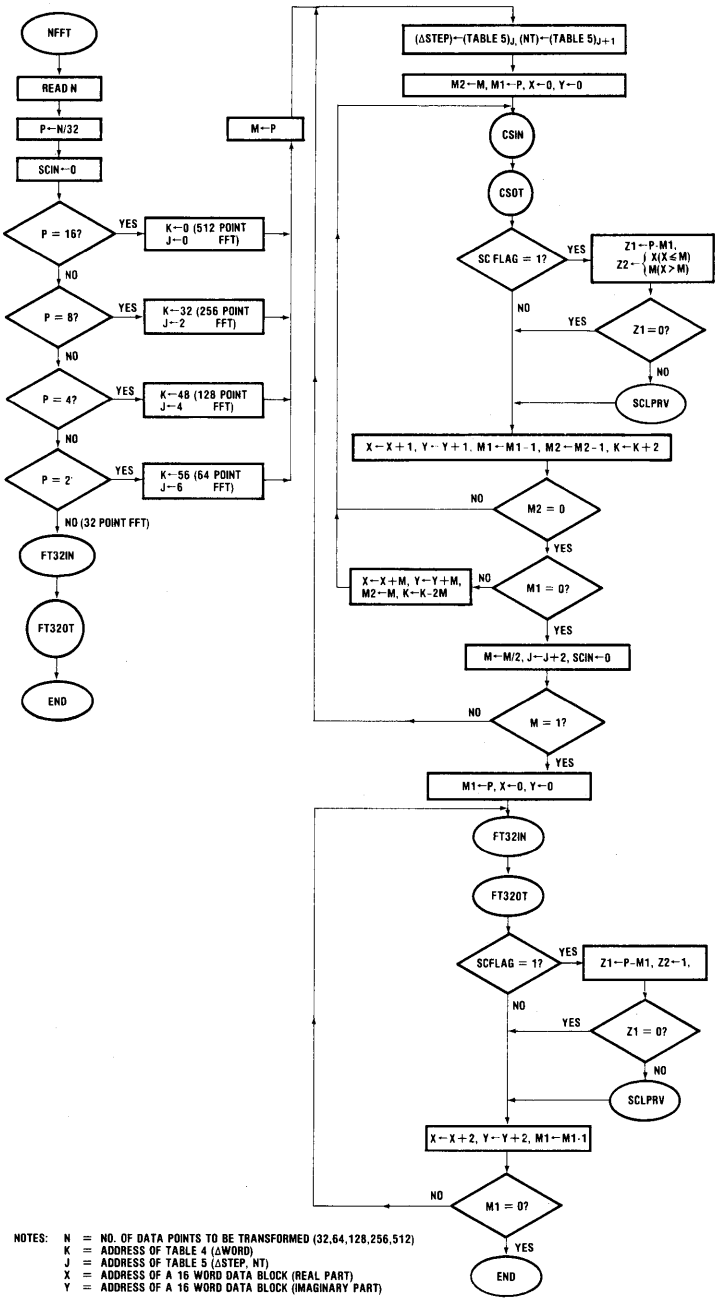


Figure 9. Flow Chart for N Point FFT, Routine "NFFT"



NOTES: N = NO. OF DATA POINTS TO BE TRANSFORMED (32,64,128,256,512)
K = ADDRESS OF TABLE 4 (ΔWORD)
J = ADDRESS OF TABLE 5 (ΔSTEP, NT)
X = ADDRESS OF A 16 WORD DATA BLOCK (REAL PART)
Y = ADDRESS OF A 16 WORD DATA BLOCK (IMAGINARY PART)

Figure 10. Flowchart for Subroutine "SCLPRV"

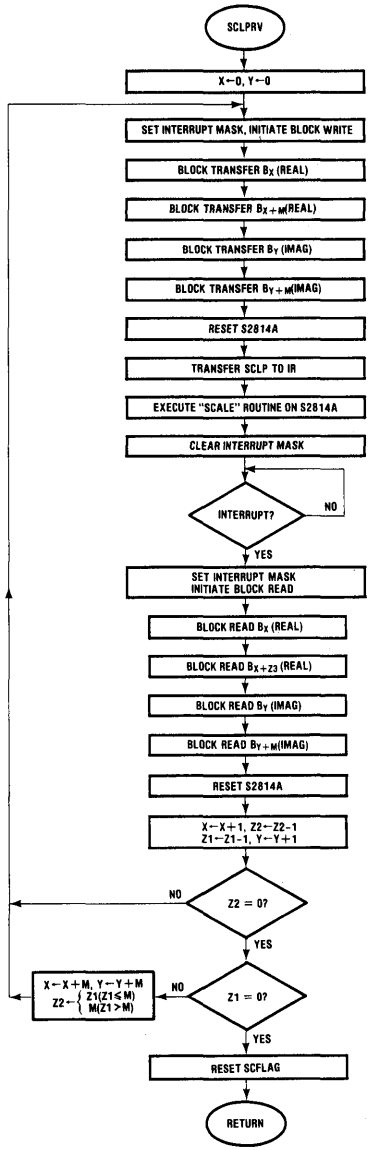


Table 4. (ΔWORD)

ENTRY PT for	K	VALUE	COMMENTS
512→	0	00	(ΔWORD L)
point	1	80	(ΔWORD H)
x'form	2	00	
	3	88	
	4	00	
	5	90	
	6	00	
	7	98	
	8	00	
	9	A0	
	10	00	
	11	A8	
	12	00	
	13	B0	
	14	00	
	15	B8	
	16	00	
	17	C0	
	18	00	
	19	C8	
	20	00	
	21	D0	
	22	00	
	23	D8	
	24	00	
	25	E0	
	26	00	
	27	E8	
	28	00	
	29	F0	
	30	00	
	31	F8	
256→	32	10	
point	33	80	
x'form	34	10	
	35	90	
	36	10	

Table 4 (continued)

ENTRY PT for	K	VALUE
	37	A0
	38	10
	39	B0
	40	10
	41	C0
	42	10
	43	D0
	44	10
	45	E0
	46	10
	47	F0
128 →	48	30
point	49	80
x'form	50	30
	51	A0
	52	30
	53	C0
	54	30
	55	E0
64 →	56	70
point	57	80
x form	58	70
	59	C0

Table 5. (ΔSTEP, NT)

ENTRY PT for	J	VALUE	COMMENTS
512 point	0	08	ΔSTEP(DUH)
x'form	1	0F	NT(DLH)
256	2	10	"
	3	07	"
128	4	20	"
	5	03	"
64	6	40	"
	7	01	"

Hardware.

The minimum hardware for a 32 point FFT is shown in Figure 11. All data transfer and control is handled by the S6802. The availability of the next input sample is signalled with the NMI line. A suitable analog interface is shown in Figure 12. The sampling clock is derived from the microprocessor clock, and the NMI signal is generated by the EOC (end of conversion) output of the A/D converter. This system may be expanded simply by adding more memory. The memory requirements are shown in Table 6. A word may be up to 16 bits long. In order to speed up the complete procedure it is necessary to use DMA for block transfer of data. The S2814A will transfer data at up to 4Mbytes/sec. A suitable DMA Address Generator is the Advanced Micro Devices AM 2940, but a 68B44 will accomplish the function more conveniently at a slightly lower speed (1.5Mbyte/sec).

Data Bus Interface.

Figure 13 shows how to interface the S2814A with a typical 6800 family microprocessor data bus. Note that the S2814A data bus must be isolated from the microprocessor system data bus by use of a PIA as in Figure 11 or a 74LS245 or 74LS645 type data transceiver as shown in Figure 13, since the S2814A drive capability is only one TTL load. The bus isolation may be omitted in some small systems.

Figure 11. 32/64 Point FFT Hardware

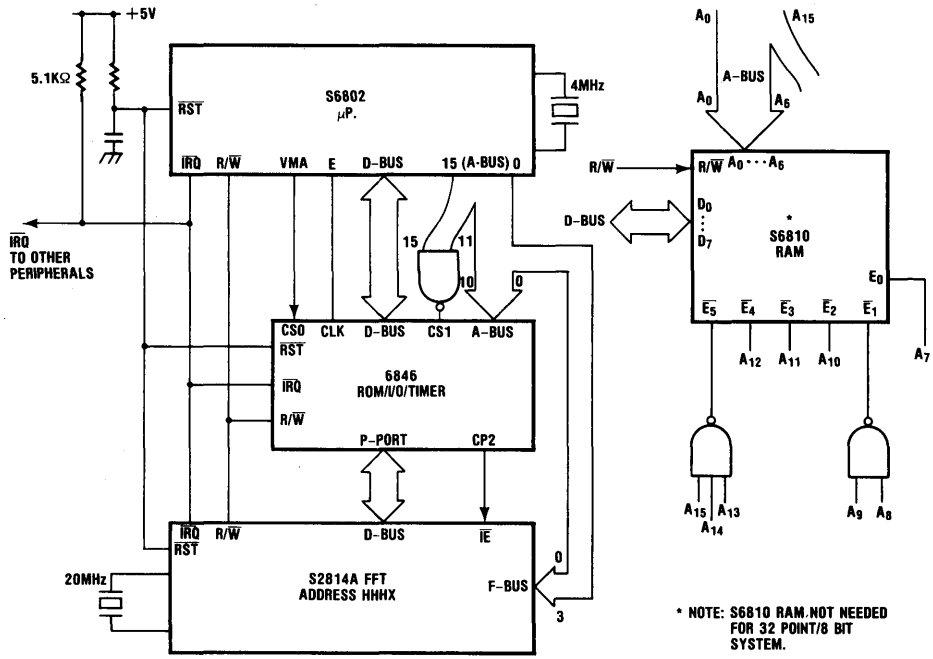


Figure 12. Analog Interface

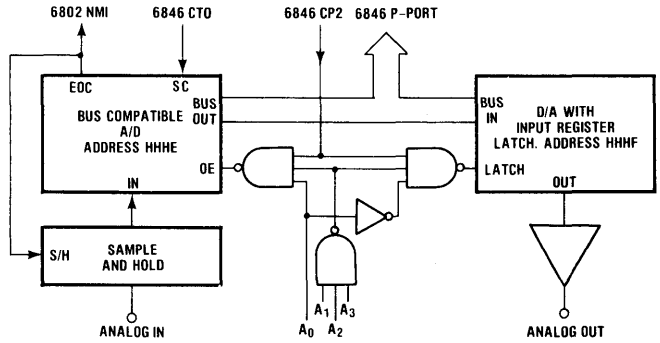


Figure 13. Interfacing the S2814A with a Microprocessor

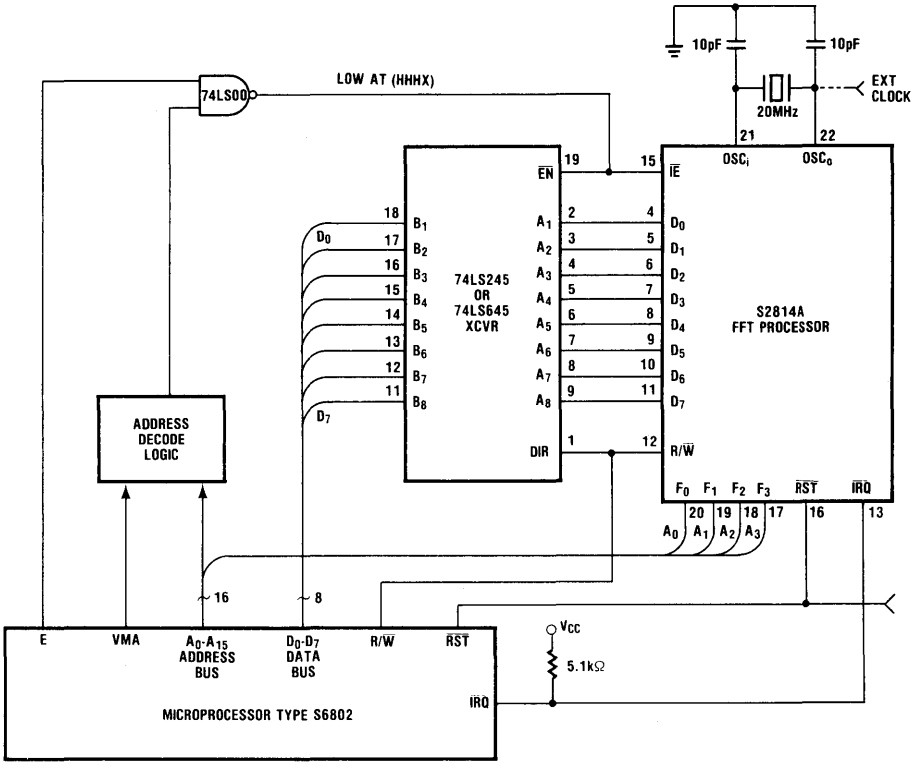


Table 6. Memory requirements for data point storage.

TRANSFORM SIZE (POINTS)	WORD LENGTH (BITS)	MEMORY REQUIREMENTS
32	8	64 bytes
	10/12	See Note 1
	16	128 bytes
64	8	128 bytes
	10/12	See Note 1
	16	256 bytes
128	8	256 bytes
	10/12	768 nibbles
	16	512 bytes
256	8	512 bytes
	10/12	1536 nibbles
	16	1024 bytes
512	8	1024 bytes
	10/12	3072 nibbles
	16	2048 bytes

Note 1: In practice the memory realization for these cases will be the same as for 16-bit systems.

Transform Execution Times.

The maximum execution times of transforms are shown in Table 7. The actual execution time when CAS is enabled will be between the times shown for CAS off and the maximum with CAS on. It will depend on the number of times that scaling has to be done.

FFT Resolution and Dynamic Range

The use of the Decimation in Frequency (DIF) algorithm in the S2814A ensures optimum signal to noise ratio, (SNR) for the architecture used. The use of the Conditional Array Scaling (CAS) gives a total dynamic range of approximately 70dB on all sizes of Transforms. The maximum resolution obtainable is approximately 57dB. CAS operates by detecting overflow in the butterfly computation routine. As soon as an overflow is detected the two points being combined in that butterfly are halved in magnitude (both the real and imaginary portions) and the butterfly recomputed. A flag is set, all previously computed butterfly outputs are then scaled, and all the inputs to subsequent butterflies are scaled before computation begins, so that at the end of the pass all points have been scaled equally. A scale factor is made available (SCOUT) so that the remaining data points in larger transforms, i.e., those other than the 32 in the S2814A when the overflow occurred, may also be scaled to keep them all in line. Thus, CAS operates as a discrete AGC, halving the signal levels each time an overflow is detected. By using SCOUT after executing the FFT the output may be expanded, so that the levels displayed in the spectrum will increase monotonically as the input increases.

Table 4. Total FFT execution times including block transfers. (msec.)

TRANSFORM SIZE	USING SINGLE S2814A BLOCK TRANSFER USING:				USING MULTIPLE S2814A ARRAY		
	A S6802 (22μsec/word)		B DMA 2MW/sec		# OF S2814As	C (USING DMA AT 2MW/sec)	
	MIN	MAX	MIN	MAX		MIN	MAX
32 pt.	4.0	4.6	1.3	1.9	1	1.3	1.9
64	14.2	15.7	3.2	4.6	2	1.6	2.3
128	40.7	44.0	7.6	11.0	4	1.9	2.8
256	106	114	17.8	25.4	8	2.3	3.2
512	262	280	40.7	57.9	16	2.6	3.7

Note: Minimum times assume that CAS and PSF are off. Maximum times assume that CAS and PSF are on, and that maximum overflow occurs during 1st pass. All times assume 20MHz clock frequency and must be increased proportionally for lower clock frequencies (except Column A).

AMERICAN MICROSYSTEMS, INC.

Please note: the S2815 has been replaced with the S28215 which is an NMOS direct pin for pin electrical and functional replacement for the S2815.

S2815

DIGITAL FILTER/UTILITY PERIPHERAL

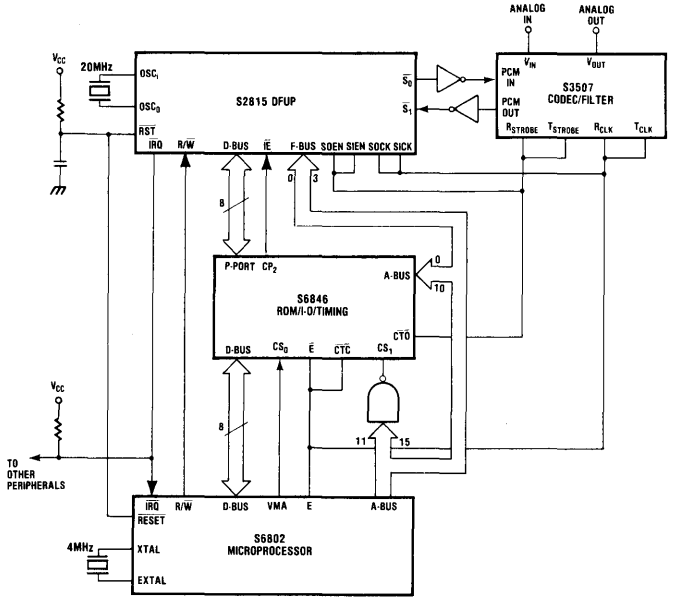
Features

- ☐ **S2811 Signal Processing Peripheral Programmed With Filter and Utility Routines**
- ☐ **Microprocessor Compatible Interface Plus Asynchronous Serial Interface**
- ☐ **Two Independent 30 Tap Transversal Filter Routines, Cascadable into a Single 60 Tap Filter**
- ☐ **Two Recursive (biquadratic) Filters Providing a Total of 16 Filter Sections**
- ☐ **Computation Functions: Two Integrating, Two Rectifying, Squaring, and Block Multiply Routines**
- ☐ **Conversion Functions: μ255 Law-to-Linear, Linear-to-μ255 Law, and Linear-to-dB Transformations**
- ☐ **Generator Functions: Sine and Pseudo-Random Noise Patterns**

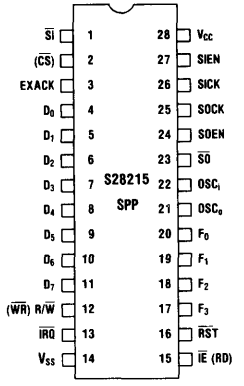
General Description

The AMI S2815 Digital Filter/Utility (DFUP) is a pre-programmed version of the S2811. Architectural and internal operating details of the S2811 may be found in the S2811 Advanced Product Description. The S2815 has been programmed with a collection of filter, computational, conversion, and generator routines which may be selected individually, or cascaded under control of the host processor. This arrangement allows a wide range of

Typical System Configuration



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

General Description (Continued)

signal processing functions frequently required in application areas such as telecommunications, test and instrumentation, industrial automation, process control, etc., to be satisfied by a single S2815 DFUP.

The I/O structure of the S2815 provides flexibility and easy interfacing in microprocessor based systems. Input and output data transfers may be accomplished serially, as shown in the block diagram, using a μ255-law Codec such as the S3507, or using linear A/D and D/A converters. Data may also be transferred in parallel under control of a host processor, such as the S6802. Routines may be executed individually, completely under control of the host processor, or internal transfer addresses may be set up by the host, allowing routines to be cascaded internally. The ability to cascade routines allows complicated functions to be completed without intervention by the host processor.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C

Electrical Specifications: (V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 0°C to +70°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Logic "1" Voltage	2.0		V_{CC}+0.3	V	V_{CC} = 5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC} = 5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μAdc	V_{IN} = 0V to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD} = −100μA, V_{CC} = min, C_L = 30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD} = 1.6mA, V_{CC} = min, C_L = 30pF
f_{CLK}	Clock Frequency	5.0	20		MHz	V_{CC} = 5.0V
P_D	Power Dissipation		1.2		W	V_{CC} = 5.0V
f_{CLK}(max)	Maximum Clock Frequency				MHz	V_{CC} = 5.0V
	S2815-10	10				
	S2815-12	12				
	S2815-15	15				
	S2815	20				

S2815 Function/Descriptions

Microprocessor Interface (16 pins)

D_0 through D_7 (Input/Output) Bi-directional 8-bit data bus.

F_0 through F_3 (Input) Control Mode/Operation Decode. Four microprocessor address leads are used for this purpose. See "CONTROL MODES AND OPERATIONS." (Table 2.)

$\overline{IE}$ (Input) Interface Enable. A low level on this pin enables the SPP microprocessor interface. Generated by microprocessor address decode logic.

$R/\overline{W}$ (Input) Read/Write Select. When HIGH, output data from the SPP is available on the data bus. When LOW, data can be written into SPP.

$\overline{IRQ}$ (Output) Interrupt Request. This open-drain output will go LOW when the SPP needs service from the microprocessor.

$\overline{RST}$ (Input) When LOW, clears all internal registers and counters, clears all modes and initiates program execution at location 00.

Serial Interface (6 pins)

SICK, SOCK (Input) Serial Input/Output Clocks. Used to shift data into/out of the serial port.

$\overline{SI}$ (Input) Serial Input. Serial data input port. Data is entered MSB first and is inverted.

SIEN (Input) Serial Input Enable. A HIGH on this input enables the serial input port. The length of the serial input word (16 bits maximum) is determined by the width of this strobe.

$\overline{SO}$ (Output) Serial Output. Three-state serial output port. Data is output MSB first and is inverted.

SOEN (Input) Serial Output Enable. A HIGH on this input enables the serial output port. The length of the serial output (16 bits maximum) is determined by the width of this strobe.

Miscellaneous

OSC_i, OSC_o An external 20MHz crystal with suitable capacitors to ground can be connected across these pins to form the time base for the SPP. An external clock can also be applied to OSC_o input if the crystal is not used.

V_{CC}, V_{SS} Power supply pins $V_{CC} = +5V$, $V_{SS} = 0$ volt (ground).

Functional Description

The S2815 is a pre-programmed version of AMI's S2811 Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters. For more detailed information about the chip, please refer to the S2811 Advanced Product Description.

The S2815 Instruction ROM contains the various routines which make up the DFUP package. The routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the parameters required to execute the functions. 128 words of Data RAM and an 8 word scratchpad are provided to hold the signal data and the jump addresses for cascading routines. The Data memory is arranged as a matrix of 32×8 words, as shown in Table 1B. The RAM utilization is routine dependent and is illustrated in the routine descriptions.

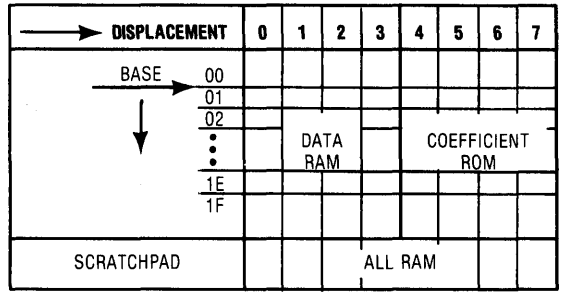
Table 1. Software Model of S2815

A. Routine Locations in Instruction Memory

(LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT "INIT" ROUTINE
04	ENTRY POINT "SETUP" ROUTINE
18 or 19*	ENTRY POINT "LINIP" ROUTINE
1B or 1C*	ENTRY POINT "MULIP" ROUTINE
34	ENTRY POINT "LINO1" ROUTINE
36	ENTRY POINT "LINO2" ROUTINE
38	ENTRY POINT "MULOP" ROUTINE
65	ENTRY POINT "DBOP" ROUTINE
80	ENTRY POINT "BMPY" ROUTINE
87	ENTRY POINT "IIR1" ROUTINE
96,97 or 98*	ENTRY POINT "IIR2" ROUTINE
A7	ENTRY POINT "FIR1" ROUTINE
AF, B0 or B1*	ENTRY POINT "FIR2" ROUTINE
BC	ENTRY POINT "RECT" ROUTINE
BF	ENTRY POINT "SQUAR" ROUTINE
C4	ENTRY POINT "FINT" ROUTINE
CA	ENTRY POINT "RINT" ROUTINE
CE	ENTRY POINT "SQUINT" ROUTINE
D6	ENTRY POINT "SINE" ROUTINE
E5	ENTRY POINT "NSET" ROUTINE
E9	ENTRY POINT "NOISE" ROUTINE

*See Routine descriptions for explanation of alternative entry points

B. Data Memory Map



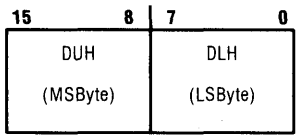
NOTE: Address [Base AB, Displacement C] is written as AB.C

C. Control Functions

F-Bus (HEX)	MNEMONIC
0	CLR
1	RST
2	DUH
3	DLH
4	XEQ
5	SRI
6	SRO
7	SMI
8	SMO
9	BLK
B	SOP
C	COP

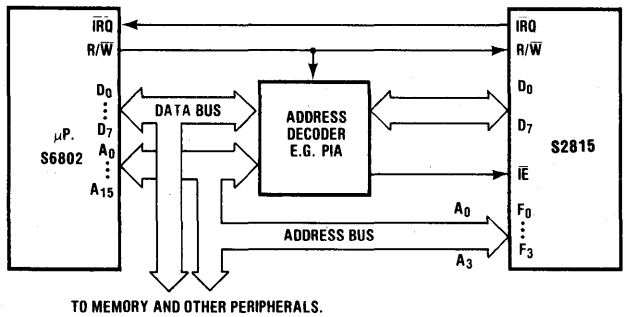
See Table 2 for descriptions

D. Input and Output Registers



Code is Two's Complement

Figure 1. Conection of S2815 as a Memory Mapped Peripheral



Initial Set-Up Procedure

After power up, the $\overline{RST}$ line should be held low for a minimum of 300nsec. If this line is connected to the reset line of the microprocessor, this condition will be met easily. This will clear the Base and Index Registers, which are used for memory addressing, the Loop Counter and the Program Counter. Address zero in the Instruction ROM contains a Jump to Zero instruction, and thus the S2815 will remain in an idle state after being reset.

The Control Functions

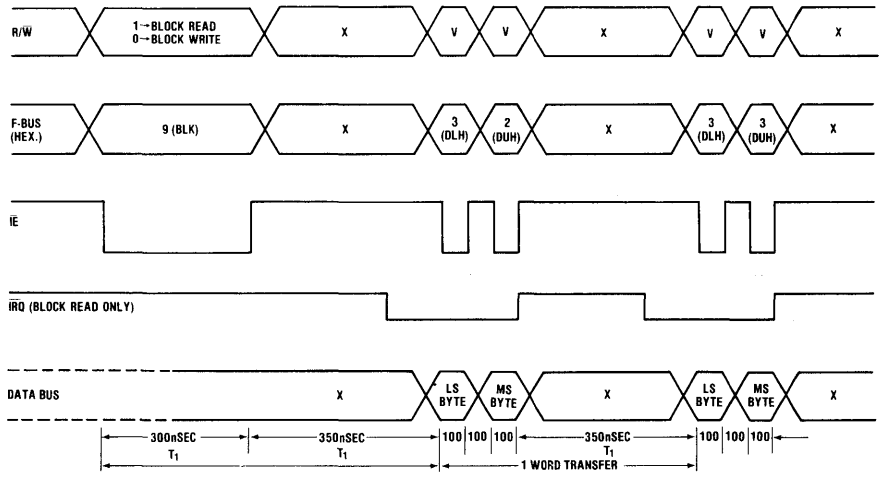
The S2815 is controlled by the host microprocessor by means of the F-bus, Interface Enable ($\overline{IE}$) and the Read-Write (R/$\overline{W}$) lines. It should be connected to the host processor as a memory mapped peripheral as shown in Figure 1.

The 12 most significant address lines decode a group of 16 addresses to activate the $\overline{IE}$ line each time an address in the group is called, and the S2815 is controlled by reading to or writing from those addresses. Only 12 of these addresses are used as described in Table 2. Throughout this Product Description these addresses will be referred to as HHHX (X=0-F).

The Block Transfer Operation

Block transfer is the mode used to load and unload the main data blocks into the S2815 at up to 4Mbytes/sec. In this mode the data memory is addressed by the Index Register, and after initialization the internal addressing is sequential and automatic. The sequence generated is that after each word transfer (16-bit words as 2 bytes, or 8-bit words as MSbyte (DUH) only) the base is incremented. After base 1F (31) has been reached, the base resets to 00 and the displacement increments. After base 1F displacement 3 has been reached (i.e., the highest address in the RAM, 1F.3), both base and displacement reset to zero. Note that when the BLK command is given the Read/Write line is latched internally, and remains latched until the RST command is given. The block transfer sequence and timing are shown in Figure 2.

Figure 2. Block Transfer Sequence and Timing



NOTE 1: X = DON'T CARE, OR NOT VALID V = VALID

NOTE 2: ALL TIMES SHOWN ARE MINIMUM AND MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS AS FOLLOWS:

$$T_{1\,MIN} = \left[\frac{6000}{f_{CLK}} + 50\right] \text{ nsec}$$

Table 2. S2815 Control Functions

MEMONIC	F-BUS HEX	DATA	TYPE OF OPERATION	FUNCTION
CLR	0	XX	XX	Clears all functions previously set. Sets SOP.
RST	1	XX	XX	Clears all registers. Starts program execution at location 00. This is the idle state. This instruction should precede block read, block write and execute commands.
DUH	2	HH	READ/WRITE	Reads from or writes into S2815 the upper half of the data word (See Table 1D). Must always follow DLH (Mandatory).
DLH	3	HH	READ/WRITE	Reads from or writes into S2815 the lower half of the data word (See Table 1D). Precedes DUH when used.
XEQ	4	HH	WRITE	Starts Execution at Location HH.
SRI	5	XX	XX	Enables Serial Input Port.
SRO	6	XX	XX	Enables Serial Output Port.
SMI	7	XX	XX	Converts sign + magnitude serial input data to two's complement.
SMO	8	XX	XX	Converts two's complement internal data to sign + magnitude serial output data.
BLK	9	XX	READ/WRITE	Initiates a block read or block write operation. The entire data RAM can be accessed sequentially beginning with values of base and displacement initialized using "Block Transfer Set Up" routine. If a reset operation is performed prior to block command, the data memory address is initialized to base 0, displacement 0. Block read or write operation can be terminated any time by performing a reset operation. The index register is used to address the memory during block transfer and internal addressing is sequenced automatically.
SOP	B	XX	XX	Set overflow protect. Normal mode of operation.
COP	C	XX	XX	Clear overflow protect.
	A,D-F			Do not use

Note: XX = Don't Care
HH = 2 Hex characters (8-bit data)

In 6800 Assembly Lanaguage a Block Write would be executed with the following code:

```
LDX   OFFST   ;LOAD MEMORY START ADDRESS INTO INDEX REG.
STA   A BLK   ;WRITE DUMMY DATA TO ADDRESS $HHH9.BLOCK MODE.
LDA   A 0,X   ;READ FIRST BYTE FROM MEMORY.
STA   A DLH   ;WRITE INTO S2815 AS LSBYTE.ADDRESS $HHH3
LDA   A 1,X   ;READ SECOND BYTE FROM MEMORY.
STA   A DUH   ;WRITE INTO S2815 AS MSBYTE.ADDRESS $HHH2
LDA   A 2,X   ;SECOND WORD.
  •     •       •
  •     •       •
  •     •       •
LDA   A 62,X  ;32ND. WORD,LSBYTE.
STA   A DLH   ;
LDA   A 63,X  ;32ND. WORD,MSBYTE.
STA   A DUH   ;END OF TRANSFER.
STA   A RST   ;WRITE DUMMY DATA TO ADDRESS $HHH1.RESET S2815
```

Block Read would be executed by substituting LDA A for STA A, and vice versa.

```
where:   RST   EQU   $HHH1
         DLH   EQU   $HHH3
         DUH   EQU   $HHH2
         BLK   EQU   $HHH9
```

The above code assumes that the block transfer is controlled by the host processor, not using DMA. Note that DLH must always precede DUH. 8-bit data may be transferred using DUH only, assuming that the significance of the data is correct.

Block transfer must be used for loading all filter coefficients (IIR1, IIR2, FIR1, FIR2, FINT, RINT and SQINT routines) and for loading and dumping the data for the BMPY routine.

The DFUP Routines

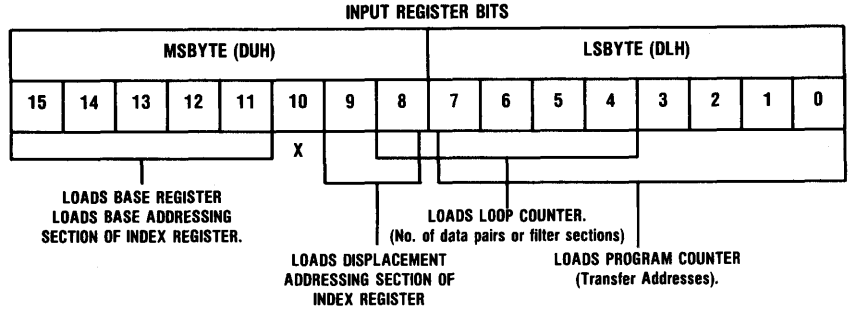
21 Individual routines are stored in the S2815 Instruction Memory. Routines INIT, SETUP, BMPY and NSET all return to the idle state after execution since they are not repetitive functions. All other routines are designed to be used repetitively with or without intervention from the control microprocessor by using loadable jump addresses to exit each routine. Thus, a number of routines may be strung together by setting the exit jump address of one to be the start address of the next. The entire function may be arranged as a closed loop, so that it will execute continuously after starting, or as an open ended string, so that it will execute once only after starting. This feature, together with the conditional synchronization feature incorporated in the 4 input routines, makes the S2815 extremely flexible as a digital filter/signal processor peripheral. The starting addresses, functions, parameters required and exit-jump (transfer) address locations are shown in Table 3.

Table 3. Parameters and Transfer Data Storage Locations:

ROUTINE	ENTRY POINT	STORAGE LOCATIONS FOR: (To be loaded using SETUP)	
		EXIT TRANSFER ADDRESS	FOR PARAMETERS
1. INIT	01	Returns to idle	None
2. SETUP	04	Returns to idle	None
3. LINIP	18 or 19*	Scratchpad 2	None
4. MULIP	1B or 1C	Scratchpad 2	None
5. LINO1	34	Scratchpad 3	None
6. LINO2	36	RAM $1E.2	None
7. MULOP	38	Scratchpad 3	None
8. DBOP	65	RAM $1E.2	None
9. BMPY	80	Returns to idle	Scratchpad 2
10. IIR1	87	Scratchpad 4	Scratchpad 7
11. IIR2	96, 97 or 98*	Scratchpad 5	Scratchpad 6
12. FIR1	A7	Scratchpad 5	Scratchpad 7
13. FIR2	AF, B0 or B1*	Scratchpad 4	Scratchpad 7
14. RECT	BC	RAM $1F.2	None
15. SQUAR	BF	RAM $1F.2	None
16. FINT	C4	RAM $1F.0	None
17. RINT	CA	RAM $1E.0	None
18. SQINT	CE	RAM $1E.0	None
19. SINE	D6	RAM $1E.0	None
20. NSET	E5	Returns to idle	None
21. NOISE	E9	RAM $1E.0	None

*See Routine Descriptions for explanation of alternative entry points

Figure 3. Input Data Significance for Register Loading



1. Block Transfer Set-up (INIT). Entry Address $01

This routine presets the Index Register to allow block transfer to commence at any location other than 00.0 in the S2815 data RAM. An eight-bit word is loaded into the upper half of the input register and the routine is executed as shown:

```
        LDA   A     #$XX
        STA   A     DUH
        LDA   A     #1
        STA   A     XEQ

where:  DUH   EQU   $HHH2
        XEQ   EQU   $HHH4
```

where XX represents the start address for block transfer. The bits used are shown in Figure 3. The routine will be executed in 3 instruction cycles (0.9μsec.) and the S2815 will return to the idle state. Block transfer may then commence immediately.

2. Parameter and Transfer Address Set-up (SETUP). Entry address $04

This routine allows the parameters and transfer addresses to be loaded into the appropriate memory locations prior to executing a function. The loading sequence is: Scratchpads 2 through 7, followed by main RAM locations $1E.0, $1E.2, $1F.0 and $1F.2. The input register bits loaded into the various internal registers are shown in Figure 3. Before executing the routine the input data for scratchpad 2 (S(2)) must be loaded into the input register. This may be omitted when not using the input routines LINIP or MULIP. While the routine is being executed the remaining input data must be loaded sequentially, allowing a minimum of 2 instruction cycles (0.6μsec.) between each word. An example of a 6800 language control program to execute SETUP is shown below:

```
SP    STA   A RST     ;RESETS S2815
      LDX     OFFST   ;LOAD MEMORY START ADDRESS INTO IX.REG.
      LDA   A 0,X     ;READ FIRST BYTE (DATA FOR S(2))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OR IR (DUMMY DATA)
      LDA   A #4      ;LOAD ACC. WITH "SETUP" START ADDRESS
      STA   A XEQ     ;START EXECUTION
      LDA   A 1,X     ;READ SECOND BYTE (DATA FOR S(3))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
      LDA   A 2,X     ;READ THIRD BYTE (DATA FOR S(4))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
      LDA   A 3,X     ;READ FOURTH BYTE (DATA FOR S(5))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
      LDA   A 4,X     ;READ FIFTH BYTE (LSBYTE FOR S(6))
      STA   A DUH     ;LOAD INTO LSBYTE OF IR
      LDA   A 5,X     ;READ SIXTH BYTE (MSBYTE FOR S(6))
      STA   A DUH     ;LOAD INTO MSBYTE OF IR
      LDA   A 6,X     ;READ SEVENTH BYTE (LS BYTE FOR S(7))
      STA   A DUH     ;LOAD INTO LSBYTE OF IR
```

```
LDA     A 7,X       ;READ EIGHTH BYTE (MSBYTE FOR S(7))
STA     A DUH       ;LOAD INTO MSBYTE OF IR
LDA     A 8,X       ;READ NINTH BYTE (DATA FOR RAM $1E.0)
STA     A DUH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
LDA     A 9,X       ;READ TENTH BYTE (DATA FOR RAM $1E.2)
STA     A DLH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
LDA     A A,X       ;READ ELEVENTH BYTE (DATA FOR RAM $1F.0)
STA     A DLH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
LDA     A B,X       READ TWELFTH BYTE (DATA FOR RAM $1F.2)
STA     A DLH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)

where:      RST   EQU   $HHH1
            DLH   EQU   $HHH3
            DUH   EQU   $HHH2
            XEQ   EQU   $HHH4
```

Note that the sequence may be aborted at any point with a STA A RST instruction. Since transfer addresses are stored in the LSByte of each 16-bit memory location, it is necessary to load dummy data into the MSByte (DUH) of the input register each time to terminate word transfer. Scratchpads 6 and 7 may hold valid data in both bytes, however. After the final data is loaded, the S2815 will return to the idle state after completion of the routine. This takes 3 instruction cycles (0.9μsec) maximum. If it is not necessary to load all the data (this is dependent on which routines are used), the routine may be aborted at any point by using the RST command, allowing a minimum of 2 instruction cycles (0.6μsec) after entering the last data required.

3. Linear Input Routine (LINIP). Entry address $18 or $19

The LINIP routine takes linearly coded (i.e., non-companded) input data from the input register and loads it into scratchpad 0 (S(0)) without modification, where it may be accessed by one of the other routines. Entering at address $18 will cause the S2815 to wait for new input data each time the routine executes. This allows the signal processing to be synchronized to the input sampling rate automatically, provided that the total execution time of all the routines cascaded to realize the overall function is less than the sampling period. If no new input data has been received when the S2815 executes line $18, then the $\overline{IRQ}$ line (interrupt request) will be set low. It will reset as soon as new data is loaded. This will occur only if the input port is in the parallel mode, i.e., the SRI mode is not set. The $\overline{IRQ}$ line is not activated in the serial mode. If the routine is entered at address $19, the processing will not wait for new input data each time, and will simply re-use the old data if none has been received. The execution time of the routine is 3 instruction cycles (0.9μsec) after receipt of new input data when entering at address $18, and 2 instruction cycles (0.6μsec) (independent of data receipt) when entering at address $19. Input data may be up to 16 bits wide. This routine exits to the transfer address stored in S(2).

4. Mu-Law Input Routine (MULIP). Entry address $1B or $1C

The MULIP routine takes μ-255 law companded data from the input register (MSByte, bits 15-8) and loads it into S(0) after linearization, i.e., decompanding. The conversion is exact. It is then suitable for linear processing and may be accessed by one of the other routines. Entering at address $1B will cause the S2815 to wait for new input data and set the $\overline{IRQ}$ line low each time the routine is executed, while entering at address $1C bypasses this feature. For details see LINIP routine description. The execution time is data dependent, being 18 instruction cycles (5.4μsec) after receipt of new input data (maximum) when entering at address $1B, and one cycle (0.3$\mu$sec) less when entering at address $1C, as for LINIP. This routine exits to the transfer address stored in S(2).

5. Linear Output Routine (LINO1). Entry address $34

The LINO1 routine takes the output data stored in S(0) and loads it into the output register without modification. This will set the $\overline{IRQ}$ line (interrupt request) low if the output port is in the parallel mode, i.e., the SRO mode is not

set. The $\overline{IRQ}$ line is not activated in the serial mode. The contents of the output register will be overwritten each time the LINO1 routine is executed. The execution time is 2 instruction cycles (0.6μsec). The routine exits to the transfer address stored in S(3).

6. Alternative Linear Output Routine (LINO2). Entry address $36

This routine is identical to LINO1, except that the exit transfer address is stored in RAM $1E.2.

7. Mu-Law Output Routine (MULOP). Entry address $38

The MULOP routine takes the output data stored in S(0) and loads it into the output register (MSByte, bits 15-8) after companding, i.e. compression according to the μ-255 law. The conversion is exact. The other features of this routine are as for LINO1. The execution time is data dependent, being 35 instruction cycles (10.5μsec) maximum. The routine exits to the transfer address stored in S(3).

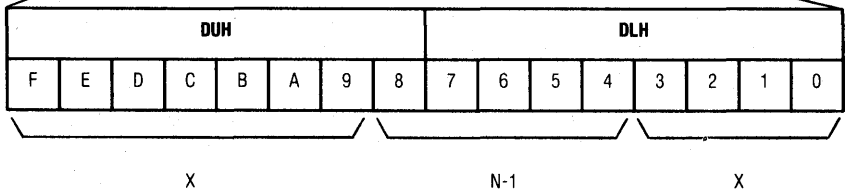
8. Decibel Output Routine (DBOP). Entry address $65

This routine takes the output data stored in S(0) and loads it into the output register after converting it to negative decibels, i.e., the result will be "dB below reference", or dBR without the sign. The integer portion of the output will be in the MSByte (bits 15-8) and the fractional part in the LSByte (bits 7-0), both as hexadecimal, positive numbers, making conversion to decimal (if required) by the control processor a simple task. All data is treated as fractional in the S2815, i.e., it lies in the range ±1. In 16 bit two's complement hex this is represented as $8000 (−1) to $7FFF ($+1 - 2^{-15}$), since +1 does not really exist in this code, being equal to −1 ($8000). The decibel reference (0dB) is taken to be +1, so that the result of decibel conversion is always negative in the DBOP routine. The output result, however, is expressed as a pure magnitude, without the minus sign, which is implicit. The conversion is accurate to ±0.01dB down to −20dB (0.1), ±0.02dB down to −40dB (0.01), and ±0.1dB down to −60dB (0.001). The conversion law used is "voltage" to dB, i.e., 20 $\log_{10}$(V), and the result must be divided by two if the result is a "power" measurement. The execution time is data dependent, being 132 instruction cycles (39.6μsec.) maximum. The routine exists to the transfer address stored in RAM $1E.2.

Table 4. Memory Map for BMPY Routine

DISPLACEMENT →		0	1	2	3	
BASE	00	A1	B1	X	P1	
	01	A2	B2	X	P2	
	02	A3	B3	X	P3	
	03	A4	B4	X	P4	
	1E	A31	B31	X	P31	
	1F	A32	B32	X	P32	
SCRATCHPAD		X	X	N-1	X	X

A,B=input data pair
P=product, AB
X=Don't care



9. Block Multiply Routine (BMPY). Entry address $80

This routine allows the user to multiply together an array of up to 32 pairs of data. The routine is not cascadable with any of the others since all data I/O must be done using the block transfer mode, and so the routine returns to the idle state after execution. The only parameter required for executing this routine is the number of data pairs to be multiplied N. The value of N-1 (i.e., the number of pairs minus one) is loaded into scratchpad 2, using the SETUP routine and then the data pairs are loaded into the RAM using the block transfer procedure. The memory map for the BMPY routine is shown in Table 4. After resetting the S2815 and setting it into the block write mode the A inputs are first loaded sequentially. If there are 32 of them, the B inputs may then be loaded sequentially without any break in the procedure (see "Block Transfer Operation").

If fewer than 32 pairs of data are involved, there are two ways of handling the procedure:

1) After loading the N values of A, load (32-N) dummy data inputs. Only the MSByte need be loaded (DUH). The internal addressing will then be set to accept the N values of B.

2) After loading the A inputs, reset the S2815 again and execute the INIT routine to set the index register to address $00.1. The input data will be $0100, although only the MSByte need be loaded (DUH = $01). Then set the S2815 into the block write mode again (without resetting) and continue loading the B inputs.

After the data pairs are loaded, the S2815 should be reset and the routine BMPY executed. The execution time is 4 + 3N instruction cycles, so that for 32 data pairs this will be 100 cycles (30μsec.). After execution the S2815 will return to the idle state and set the $\overline{IRQ}$ line low, to indicate completion. The final product (P_N) is available in the output register at this time and may be read without the use of the block transfer mode. This is useful when multiplying single data pairs. To read all the products it is necessary to first reset the S2815 and execute INIT to set the index register to address $00.3. The input data will be $0300 (DUH = $03). Setting the S2815 into the block read mode then allows the N products P to be read sequentially. Finally, the S2815 should be reset again to bring it out of the block transfer mode. The 6800 program shown below will execute the BMPY program to multiply together 2 data pairs. For simplicity, only 8 bit input data is used (DUH) and only the MSByte of the product is read, although products will be computed to 16 bits of precision for all data up to 12 bits wide.

```
BY    LDA    A #$10      ;1 = N – 1.(2 DATA PAIRS)
      STA    A DLH       ;LOAD INTO LSBYTE OF IR
      STA    A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
      LDA    A #4        ;4 = "SETUP" START ADDRESS
      STA    A XEQ       ;EXECUTE SETUP
      STA    A RST       ;RESET S2815
      STA    A BLK       ;PUT S2815 INTO BLK WRITE MODE
      LDX      OFFST     ;LOAD DATA START ADDRESS INTO IX.REG.
      LDA    A 0,X       ;READ FIRST A
      STA    A DUH       ;LOAD INTO MSBYTE OF IR
      LDA    A 1,X       ;READ SECOND A
      STA    A DUH       ;LOAD INTO MSBYTE OF IR
      STA    A RST       ;RESET S2815.EXIT BLK MODE
      LDA    A #1        ;1 = PRESET FOR S2815 IX,ALSO "INIT" START ADDRESS
      STA    A DUH       ;LOAD INTO MSBYTE OF IR
      STA    A XEQ       ;EXECUTE INIT
      STA    A BLK       ;PUT S2815 INTO BLK WRITE MODE
      LDA    A 2,X       ;READ FIRST B
      STA    A DUH       ;LOAD INTO MSBYTE OF IR
      LDA    A 3,X       ;READ SECOND B
      STA    A DUH       ;LOAD INTO MSBYTE OF IR
      STA    A RST       ;RESET S2815.EXIT BLK MODE
```

```
LDA     A #$80      ;$80 = "BMPY" START ADDRESS
STA     A XEQ       ;EXECUTE BMPY
WAI                 ;WAIT FOR INTERRUPT
STA     A RST       ;START OF INTERRUPT ROUTINE.RESET S2815
LDA     A #3        ;3 = PRESET FOR S2815 IX
STA     A DUH       ;LOAD INTO MSBYTE OF IR
LDA     A #1        ;1 = "INIT" START ADDRESS
STA     A XEQ       ;EXECUTE INIT
LDA     A BLK       ;PUT S2815 INTO BLK READ MODE
LDA     A DUH       ;READ FIRST PRODUCT
STA     A 4,X       ;STORE IN MEMORY
LDA     A DUH       ;READ SECOND PRODUCT
STA     A 5,X       ;STORE IN MEMORY
STA     A RST       ;RESET S2815.EXIT BLK MODE

where:      RST  EQU  $HHH1
            DLH  EQU  $HHH3
            DUH  EQU  1HHH2
            XEQ  EQU  $HHH4
            BLK  EQU  $HHH9
```

This program is intended to be instructional rather than practical, since the multiplication of such small arrays of 8 bit numbers can be done more effectively by other means, e.g., using a 6809 microprocessor. However, the extremely fast multiplication time of the S2815 makes this an effective way of dealing with large arrays.

10. Recursive (IIR) Digital Filter Routine IIR1. Entry address $87

This routine executes a number of biquadratic filter sections in cascade. The number of sections can be 1-16. The routine takes its input data from, and returns the output data to, Scratchpad 0. Each filter section occupies 2 bases of RAM in the data memory, with successive filter sections mapped into sequential base pairs as shown in Table 5. In order to be able to use this routine in conjunction with others, e.g., a transversal filter routine, it is possible to set the start base to any value, provided that enough space is left for the other filter sections, i.e., start base (Max.)= 32−2x (number of filter sections), e.g., for a 8th order filter (4 sections) start base (Max)=32 −8=24 ($18).

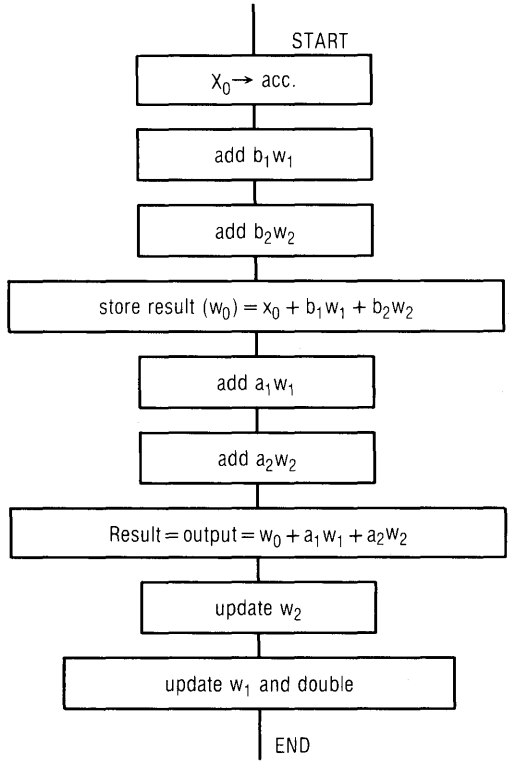
The data for the start base (bits 15-11) and (number of sections −1) (bits 8-4) is stored in S(7), and the exit transfer address is stored in S(4). These should be loaded using the SETUP routine, and the filter coefficients loaded using block transfer. Due to the algorithm used ALL FILTER COEFFICIENTS MUST BE HALVED BEFORE LOADING. This allows filter coefficients in the range ±2 to be used with purely fractional arithmetic.

Table 5. Memory Map and Flow Chart for IIR1 and IIR2 Routines

DISPLACEMENT ⟶		0	1	2	3
BASE	B	$-\frac{1}{2}b_2(1)$	$\frac{1}{2}a_2(1)$	$2w_2(1)$	X
↓	B+1	$-\frac{1}{2}b_1(1)$	$\frac{1}{2}a_1(1)$	$2w_1(1)$	X
	B+2	$-\frac{1}{2}b_2(2)$	$\frac{1}{2}a_2(2)$	$2w_2(2)$	X
	B+3	$-\frac{1}{2}b_1(2)$	$\frac{1}{2}a_1(2)$	$2w_1(2)$	X
	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮

NOTE: (1), (2) . . . . . means data for filter section 1, 2, etc.

Table 5. (Continued)



The algorithm. The basic algorithm used is the canonic form of biquadric difference equation:

$$w_0 = x_0 + b_1w_1 + b_2w_2$$

$$y_0 = w_0 + a_1w_1 + a_2w_2$$

where x_0 = the new input sample (Nth)

w_0 = the new intermediate output (Nth)

w_1 = the previous intermediate output (N-1th)

w_2 = The second previous intermediate output (N-2th)

y_0 = new section output (Nth)

Thus the transfer function is:

$$H(z) = \frac{1 + a_1z^{-1} + a_2a^{-2}}{1 - b_1z^{-1} - b_2z^{-2}}$$

Note the signs of the denominator co-efficients (b_1 and b_2).

Since coefficients a_1 and b_1 can lie in the range ± 2 it is necessary to perform some scaling to fit them into the fractional arithmetic of the S2815. The scheme used is: halve all coefficients and double all stored data, as shown in Table 5. Thus, all products of coefficients and data remain unchanged. This does, of course, have implications on the dynamic range of the system, since the signal levels throughout the system must be 6dB lower than would be possible

otherwise, in order to avoid overflow when the data is doubled. Note that the system normally operates with saturation arithmetic, since the SOP mode is automatically set. The user can change this by setting the COP mode from the control processor. However, instability may occur after overflow when operating in this mode. As with any digital filter, care must be taken with the gains that occur in most types of filters, especially in high Q sections. The optimum sequencing of both the numerators and the denominators of the transfer function polynomial is crucial to realize the maximum dynamic range of the system.

The use of this routine, including the host processor program, is illustrated in an applications example later in this Product Description. The execution time is 12 N+ 3 instruction cycles per sample (3.6N + 0.9μsec) for an N section filter.

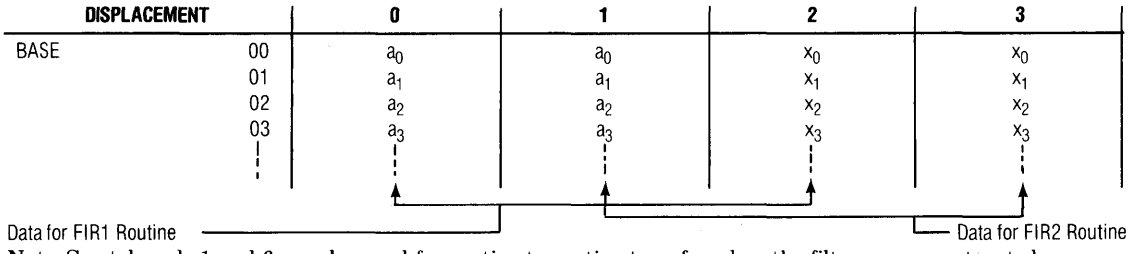
11. Recursive (IIR) Digital Filter Routine IIR2. Entry Address $96, $97 or $98

The function of this routine is similar to that of IIR1. The only differences are that a data input routine (equivalent to using LINIP) is available at the start, and the parameters and exit transfer address are stored in S(6) and S(5) respectively. Entering the routine at address $96 provides the "wait for new input" function, and entering at address $97 bypasses this feature (see description of LINIP routine). Entering at address $98 bypasses the input function altogether, and the input data will be taken from S(0), as with IIR1. The 2 recursive filter routines may be used together by mapping their data into different areas of the RAM, by using different start bases. The maximum total number of filter sections (shared between the 2 routines) remains at 16. By using the input function built into IIR2 and using LINIP to load data into IIR1, and by using separate output routines (LINO1 and LINO2), it is possible to process two completely independent signals simultaneously, as long as they have the same sampling frequency. A typical routine sequence (in a closed loop function) would be LINIP→IIR1→LINO1→IIR2→LINO2→back to LINIP. The execution time is 12N+3 instruction cycles per sample (3.6N+0.9μsec) for an N section filter (as for IIR1) when entering at address $98, and 2 or 1 instruction cycles longer when entering at address $96 or $97 respectively.

12. Transversal (FIR) Digital Filter Routine FIR1. Entry Address $A7

This routine executes a transversal (non-recursive, or FIR) filter function with 1-32 taps. The routine takes its input data from, and returns the output data to, scratchpad 0. The memory map for this routine (and for routine FIR2) is shown in Table 6. The data starts at base 0 at all times. The coefficients should be loaded using block transfer and the (number of taps −1) data is stored in S(7) (bits 8-4). The exit transfer address is stored in S(5). The two scratchpad locations should be loaded using the SETUP routine.

Table 6. Memory Map FIR1 and FIR2 Routines



Note: Scratch pads 1 and 6 are also used for routine to routine transfer when the filters are concatenated.

The algorithm. The algorithm used is straightforward. It computes the sum of products

$$y_0 = a_0x_0 + a_1x_1 + a_2x_2 \ldots . a_{N-1}x_{N-1}$$

where the x_i are input data samples in reverse chronological order, i.e., x_0 is the new input sample, x_{N-1} the oldest remaining in the storage register. The computation sequence is left to right, i.e., a_0x_0 first, then add a_1x_1, etc. Care must be taken to avoid overflow due to the system gain. The execution time for an N tap filter is N + 7 instruction cycles. (0.3N + 2.1μsec.) e.g. a 32 tap filter will be executed in 39 cycles, 11.7μsec.

13. Transversal (FIR) Digital Filter Routine FIR2. Entry Address $AF, $B0, or $B1

This routine is very similar to FIR1 except that a data input routine (equivalent to using LINIP) is available at the start; and the exit transfer address is stored in S(4). It is possible to operate both FIR filter routines concurrently, since they use mutually exclusive RAM locations for their signal and coefficient data, as shown in Table 6. However, since both routines use S(7) to store the data for the number of taps in the filters, they are constrained to be equal in length. This is not a problem in practice since one filter may easily be made shorter than the other by using coefficient values of zero for the unwanted taps. Note that if entry addresses $AF or $B0 are used for FIR2 then this routine executes an independent filter function, with separate input and output from FIR1, but if entry address $B1 is used then the routine is automatically appended to FIR1 to extend the length of the filter, up to a maximum of 64 taps. This occurs because the last tap data in FIR1 is loaded into the first tap position of FIR2 in the next sample period. However, the output data of the 2 routines are still treated separately. They must be read out with separate output routines (LINO1 and LINO2) and summed by the control processor to give the total sum of products for the whole filter. A typical routine sequence (In a closed loop function) for using FIR1 and FIR2 would be

LINIP→FIR1→LINO1→FIR2→LINO2→back to LINIP

If FIR2 is entered at addresses $AF or $B0 then this will execute 2 independent filters of the same length with separate I/O. If FIR2 is entered at $B1 then the function becomes a single double length filter with a single input and 2 outputs which must be summed externally.

The execution time of FIR2 is N+10 instruction cycles per sample (0.3N+3.0μsec) for an N tap filter when entering at address $B1, and 2 or 1 instruction cycles longer when entering at addresses $AF or $B0.

14. Rectifier Routine, RECT. Entry Address $BC

This routine gives the absolute value of the input data, so that in analog terms it acts as a perfect full wave rectifier. It will usually be used with the routine FINT. It takes its input from, and returns the output to S(0), and the exit transfer address is stored in RAM $1F.2 using the SETUP routine. The execution time is 3 instruction cycles (0.9μsec).

15. Squaring Routine, SQUAR. Entry Address $BF

This routine squares the input data, so that in analog terms the output is representative of the power level of the signal. When used with the FINT routine the result will be the mean square signal level. It takes its input from, and returns the output to, S(0), and the exit transfer address is stored in RAM $1F.2 using the SETUP routine. The execution time is 5 instruction cycles. (1.5μsec.)

16. First Order Integrator Routine, FINT. Entry Address $C4

This routine executes a first order recursive filter function, and although it is intended to be used as an integrator, it will equally act as a high or low pass filter. The function will be dependent on the coefficient b_1 used in the algorithm.

$$y_0 = x_0 + b_1 y_1$$

giving the transfer function

$$H(z) = \frac{1}{1 - b_1 z^{-1}}$$

When $b_1 = +1$ the system becomes a perfect, i.e., zero leakage, or infinite time constant, integrator. This is not quite attainable in practice since the maximum possible value of b_1 is $7FF0. (The last hexad is a zero not F, because the coefficient is truncated to 12 bits at the multiplier input.) This is equivalent to a decimal value of 0.9995. The coefficient b_1 is stored in RAM location $1F.1 using block transfer, and the exit transfer address is stored in RAM $1F.0 using the SETUP routine. The execution time is 6 instruction cycles (1.8μsec.).

17. Rectify and Integrate Routine, RINT. Entry address $CA

This routine is equivalent to a combination of RECT and FINT. The coefficient b_1 is stored in RAM location $1D.1 using block transfer, and the exit transfer address is stored in RAM $1E.0 using the SETUP routine. The execution time is 8 instruction cycles (2.4μsec.) making it 1 cycle faster than using RECT and FINT.

18. Square and Integrate Routine, SQINT. Entry Address $CE

This routine is equivalent to a combination of SQUAR and FINT. The coefficient b_1 is stored in RAM location $1D.1 using block transfer, and the exit transfer address is stored in RAM $1E.0 using the SETUP routine. The execution time is 8 instruction cycles (2.4μsec.) making it 3 cycles faster than using SQUAR and FINT.

19. Sine Generator Routine, SINE. Entry address $D6

This routine computes the sine of the input angle. The input data is required in the form of ω/π so that input data varying from -1 to $+1$ will represent angles from $-\pi$ to $+\pi$, covering a full cycle, or rotation. Cosines may be obtained by complementing the angle.

The algorithm. The 2 MSBs of the input angle (B_{15}-B_{14}) denote the quadrant in which angle lies. This information is first extracted and stored. The next 4 bits (B_{13}-B_{10}) are then used to address a 16 step sine/cosine lookup table, giving 64 values for the quantized angle in the 4 quadrants. The remaining bits are then used to interpolate between these 64 values, using the relationship:

$$\sin(A+\delta)=\sin A\cos\delta+\cos A\sin\delta$$

and the approximations $\cos\delta \rightarrow 1$ and $\sin\delta \rightarrow \delta$ } for small values of δ

giving $\sin(A+\delta)=\sin A+\delta\cos A$

Since $\delta < 6°$ (360/64) the maximum error in the approximation is 0.5% so that the result is correct to approximately 9 bits, including the sign. The routine takes its input from, and returns the output to, S(0), so that it may be used as data either for an output routine or as an input for one of the other computational routines. The execution time of the routine is 15 instruction cycles (4.5μsec.).

20. Noise Generator Setup Routine, NSET. Entry Address $E5

This routine sets up a non-zero starting value in the RAM location used as the register for the PRBS in the NOISE routine, and also allows the user to set a scaling factor for the output level of the noise. The peak level of the noise is equal to the scale factor used. A 6800 control program to execute this function is shown below:

```
LDA   A #SCALE     ;FETCH SCALE FACTOR
STA   A DUH        ;LOAD INTO IR (MSBYTE)
STA   A XEQ        ;EXECUTE NSET

where:    DUH   EQU   $HHH2
          XEQ   EQU   $HHH4
```

and SCALE is the desired scale factor in the range $00 to $7F. It is assumed that 8 bit precision is sufficient for the scale factor, but a 12 bit scale factor may be used if desired. The execution time of the routine is 4 instruction cycles (1.2μsec.) and the routine returns to the idle state after execution.

21. Noise Generator Routine, NOISE. Entry Address $E9

This routine generates a pseudo-random-binary-sequence of length 32767 cycles ($2^{15}-1$) using a 15 bit shift register with linear (exclusive - OR) feedback from the last 2 bits. The register is actually RAM location $1D.0, so that the result is that a pseudo-random number in the range $0001 to $7FFF is generated in this address. The value is then offset by $4000 to make the range symmetrical about zero (to eliminate the D.C. component) and doubled, making the new range $FFFE to $7FFE. It is then multiplied by the scaling factor loaded using the NSET routine, so that any peak value may be obtained. The output is loaded into S(0), so that it may be used as data either for an output routine or as an input for one of the other computational routines. The execution time of the routine randomly varies from 16 to 17 instruction cycles (4.8 - 5.1μsec.), with a mean time of 16.5 cycles over the entire sequence.

Cascading the Routines to Perform Functions

In order to perform a real function with the S2815 it is necessary to cascade a number of routines by setting up the appropriate exit transfer addresses to cause each routine to jump to the entry address of the next. The complete se-

quence may be open ended, jumping to the idle state after executing the final routine, or closed loop, jumping back to the entry address of the first routine after executing the last. A sequence will usually consist of an input/generation routine, followed by a chain of computational routines, ending in an output routine. This is explained in more detail in the examples.

Compatibility and Mutual Exclusivity of Routines

Since some routines share common storage locations for their exit transfer addresses, they are generally incompatible, or mutually exclusive, e.g., the two input routines LINIP and MULIP both use S(2) to store their exit transfer addresses, and consequently the function executed will be identical after exit from either of these two routines. In a closed loop situation, therefore, the function will always return to the same input routine after completion of the cycle, so that the other input routine becomes redundant. However, it is very unlikely that a situation would arise where both input routines would be required within the same closed loop program, so that this mutual exclusivity is very unlikely to be a problem.

The reason for using common exit transfer address storage locations is to reduce the memory requirement for this function, so as to make more memory available for the computational routines, such as the IIR and FIR routines. It will be found that in most cases no conflict will occur since the storage locations have been allocated in such a way as to minimize the mutual exclusivity of routines that are likely to be used together.

Another factor that can cause unwanted interaction between routines is common allocation of addresses for coefficients and/or data used internally in routines. In some cases this data is only stored temporarily in these locations and it is not necessary to preserve these data from one sample period to the next, however, in other cases this is not so. A good example is the use of scratchpads 1 and 6 in the FIR2 routine. These are always used (and overwritten) during the execution of this routine, but are only used for sample to sample data storage if this routine is used to extend the length of a filter with FIR1 i.e., by entering at address $B1. In the latter case the execution of the routine will be upset if another routine using these scratchpads (e.g., SINE, which uses S(1)) is incorporated in the program sequence. The memory maps for the BMPY, IIR1 & 2, and FIR1 & 2 routines are shown in Tables 4, 5, and 6. The address used in these routines are dynamically allocated according to the requirements e.g., the number of taps in the FIR filters, and care must be taken when using these routines in conjunction with others. A memory map for the locations used by the other routines is shown in Table 7.

Table 7. Memory Map for Routines (except BMPY, IIR and FIR)

SP	0	1	2	3
	I/O DATA (MOST ROUTINES)	T(4, 7, 8, 13, 19) D(13)*	E(3, 4)	E(5, 7)

SP	4	5	6	7
	E(10, 13)	E(11, 12)	P(11)	P(10, 12, 13)

	→DISPLACEMENT			
BASE↓	0	1	2	3
1C.		T(8)		T(8)
1D.	D(21)	T(21) C(17, 18)	C(21)	T(21) D(17, 18)
1E.	E(17, 18, 19, 21)	T(18)	E(6.8)	T(15)
1F.	E(16)	C(16)	E(14, 15)	D(16)

NOTES:

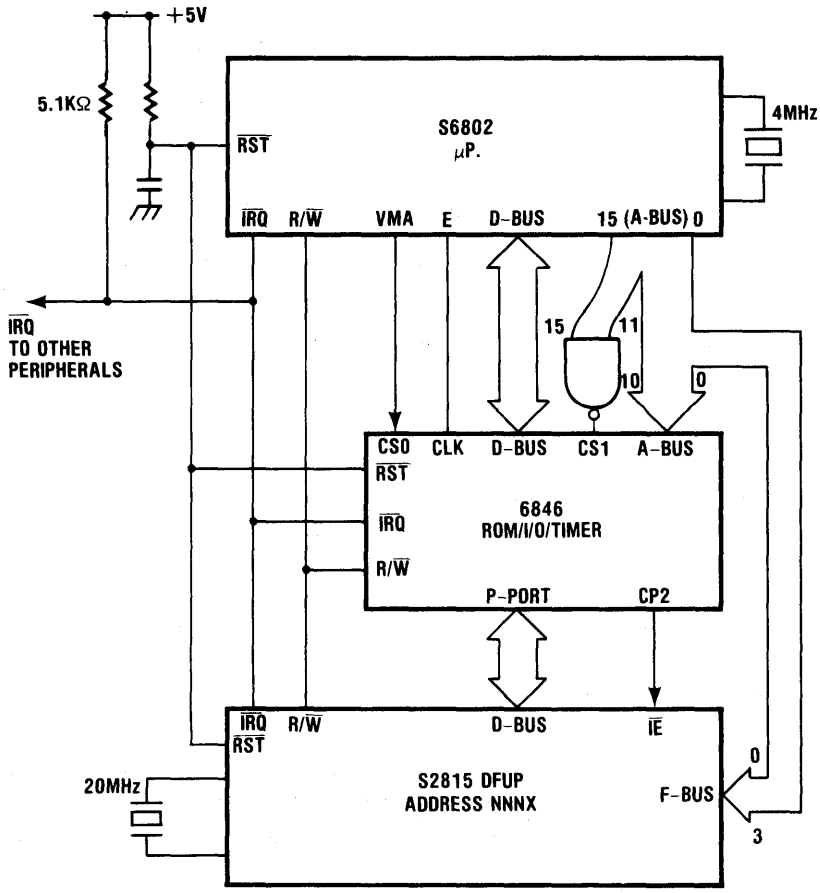
E = EXIT TRANSFER ADDRESS
P = PARAMETERS (BASE REGISTER AND LOOP COUNTER DATA)
C = COEFFICIENT
D = DATA (STORED FROM ONE SAMPLE PERIOD TO NEXT)
T = TEMPORARY DATA (USED ONLY DURING EXECUTION CYCLE)
(n) = ROUTINE NUMBER IN WHICH IT IS USED
(see Table 3 for cross-reference to routines)

*ONLY WHEN FIR2 ROUTINE IS ENTERED AT ADDRESS $B1 TO CONCATENATE FILTERS.

Hardware

The minimum hardware for the S2815 is shown in Figure 4. This does not include any provisions for analog interfacing, which is treated in the next section. The S6846 ROM/I/O/TIMER is used to store the S6802 control program and parameters, handle the parallel I/O from the S2815 and generate timing signals, e.g., sampling control. The microprocessor is synchronized to the sampling period by means of the NMI signal generated by the EOC (end of conversion) output of the A to D converter, if necessary. (This is unnecessary when using the serial port of the S2815 to handle the data from the A to D converter.)

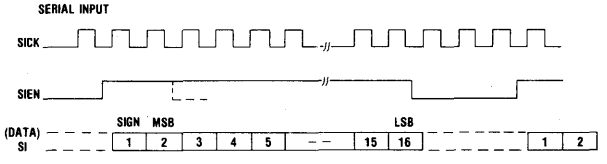
Figure 4. Minimum Hardware Configuration



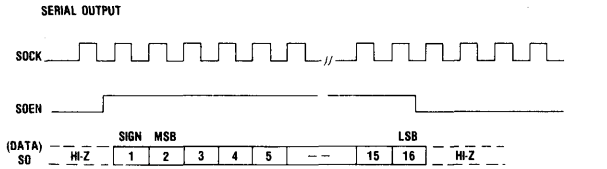
Interfacing to the Serial Port

The serial port allows bidirectional asynchronous interfacing between the S2815 and other devices such as successive approximation A/D converters and PCM Codecs or highways (using the MULIP and MULOP routines). Note that the data is inverted on both input and output. Data is clocked into and out of the S2815 with the serial clocks SICK and SOCK respectively, and gated with the enable lines SIEN and SOEN. The timing is shown in Figure 5.

Figure 5. S2815 Serial Interface Timing



1. SIEN MUST BE SYNCHRONIZED TO THE FALLING EDGE OF SICK SUCH THAT THE RISE AND FALL OF SIEN FOLLOW FALLING EDGE OF SICK.
2. DATA MAY CONTAIN 1 TO 16 BITS DEFINED BY WIDTH OF SIEN. SPP WILL LEFT JUSTIFY DATA WORDS 16 BITS.
3. DATA ARE SAMPLED ON THE TRAILING EDGE OF SICK.
4. MINIMUM 16 SICK PULSES + 64 CYCLES OF S2815 OSCILLATOR ARE REQUIRED BETWEEN SIEN RISING EDGES.
5. IF SERIAL INPUT BUFFER IS FULL, SPP WILL IGNORE NEW INPUT SAMPLES.
6. THE SERIAL DATA IS INVERTED AND MAY BE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.



1. RISE AND FALL OF SOEN MUST FOLLOW FALLING EDGE OF SOCK.
2. OUTPUT DATA WILL BE 1 TO 16 BITS DEFINED BY WIDTH OF SOEN.
3. DATA ARE VALID FROM RISING EDGE TO RISING EDGE OF SOCK SO THAT THE RECEIVING SYSTEM CAN SAMPLE DATA ON TRAILING EDGE.
4. MINIMUM 16 SOCK PULSES + 64 CYCLES OF S2815 OSCILLATOR ARE REQUIRED BETWEEN SOEN RISING EDGES.
5. IF THE SERIAL OUTPUT BUFFER IS EMPTY, ALL ONES WILL BE OUTPUT.
6. SO WILL BE IN A HIGH IMPEDANCE STATE WHEN NOT ENABLED BY SERIAL OUTPUT SEQUENCE.
7. THE SERIAL DATA IS INVERTED AND MAYBE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2816

ECHO CANCELLER PROCESSOR (ECP)

Please note: the S2816 has been replaced with the S28216 which is an NMOS direct pin for pin electrical and functional replacement for the S2816.

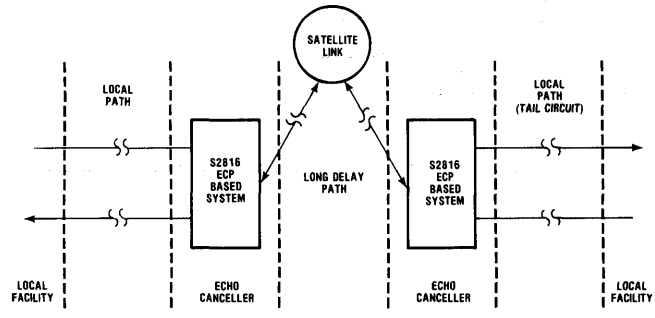
Features

- ☐ S2811 Based System With Echo Canceller Routines
- ☐ Especially Suited to Single-Hop or Double-Hop Satellite and Long Haul Terrestrial Circuits
- ☐ Eliminates Echo Without Signal Degradation
- ☐ Allows Full-Duplex Speech
- ☐ Accommodates Unlimited Long Haul Delays
- ☐ Operates With Local Loop Delays of Up to 25mSec. Expandable in 25mSec Increments Up to 100mSec
- ☐ Cancel Echoes With up to 6mSec Dispersion
- ☐ Convergence Time < 250mSec

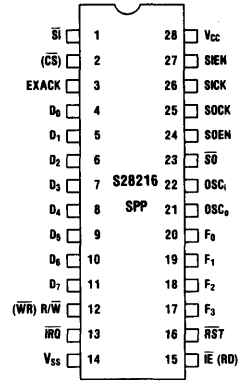
General Description

The AMI S2816 Echo Canceller Processor (ECP) is a pre-programmed version of the S2811 Signal Processing Peripheral. Architectural and internal operating details of the S2811 may be found in the S2811 Advanced Product Description. The S2816 is designed to provide the main echo canceller processing functions in a microprocessor based split-type echo canceller system. Programmed functions provided by the S2816 include μ255 law-to-linear and linear-to-μ255 law I/O conversion, local loop delay estimation, 48-tap auto-equalizing transversal filter, silence detection, and echo canceller performance estimation. This collection of routines allows the S2816 to dynamically eliminate echoes from long distance satellite undersea cable and terrestrial communication systems, employing either analog or digital links.

Typical System Application



Pin Configuration



NOTE:
PIN FUNCTIONS IN PARENTHESIS APPLY ONLY FOR B VERSION

Echo Canceller Routines

I/O Conversion

The input and output conversion routines are optional routines used when the echo canceller is placed in a PCM data stream, or when the echo canceller is placed in an analog data stream and a codec is used at the interface. The input conversion routine converts μ255 law PCM data to linear data. The output conversion routine converts linear data to μ255 law PCM data.

Local Loop Delay Estimator

The local loop delay estimator is used to determine the delay around the local loop. This information is supplied to the control processor which transfers the received data delayed by this estimate. The maximum local loop delay handling capability of the S2816 is 25.6mSec. May be expanded in 25mSec increments to 100mSec by adding additional memory storage.

Auto-Equalizing Transversal Filter

The auto-equalizing transversal filter is used to model the echo so that it may be subtracted from the signal presented on the long haul side. A 48-tap filter is used to accomplish this task. Echoes with up to 6mSec dispersion may be eliminated by this arrangement.

Silence Detector

The silence detector is used to control the learning rate of the auto-equalizing transversal filter; the silence detector routine calculates the running power average and makes a decision whether the incoming signal is speech or noise. If there is no signal to learn on, or there is a high level interfering signal, learning is suspended.

Echo Canceller Performance Estimator

The Echo Canceller performance estimate, like the silence detector, is used to set the learning rate of the echo canceller. The learning rate of the canceller is set at a level which is proportional to the estimated performance. Performance is based on the ratio of the running averages of the signal before and after cancellation. This ratio is used to control the learning rate of the auto-equalizing transversal filter. Convergence time, for 18dB echo cancellation with a 6dB Echo Return Loss (ERL), is less than 500mSec plus the local loop delay time.

System Application

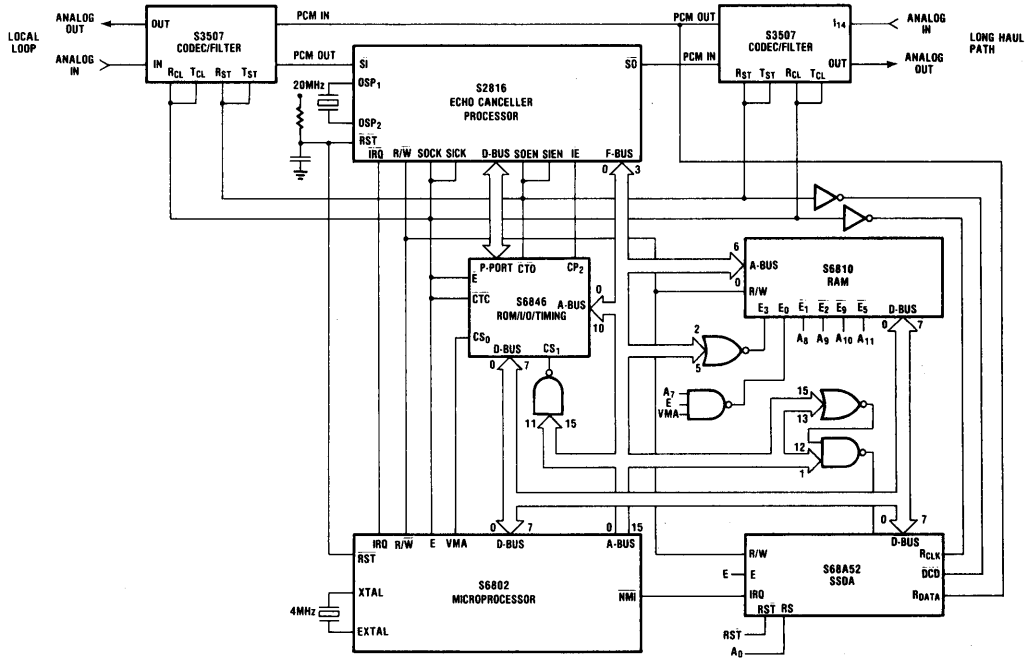
A proposed echo canceller system based on the S2816 is shown in Figure 2 together with the expected performance specifications. The S3507 codecs provide the required interfacing to the analog data stream. The S68A52 synchronous serial data adapter is used to convert the serial data stream into 8-bit words which can then be loaded into the S6810 RAM. The S6810 is used to store the receive data for a period of time equal to the local loop delay and then loaded into the S2816 for processing. The S6846 ROM-I/O-Timing is used to store the S6802 program, control the I/O between the S6802 and S2816, and provide timing signals required by the codec's. The S2816 performs the echo cancelling routines outlined above. Finally, the S6802 controls and monitors the entire operation.

Typical Echo System Specifications Using the S2816

☐ Echo Return Loss (ERL)	>6dB
☐ Residual Echo (Center Clipping Operating/Echo Suppression at High S/N Ratios)	<−60dBmo
☐ Convergence Time: ERL of 6dB and R_{in} of −10dBmo)	12dB < 250mSec 18dB < 500mSec
☐ Maximum Tail Circuit Delay	25.6mSec (1200 mi. nominal)
☐ Nominal Transmission Levels	+7dBm receive path −16dBm send path
☐ Insertion Loss	0 ±0.5dB, @1004Hz
☐ Frequency Response	±0.5dB, 300-3200Hz Ref. to 1KHz
☐ Harmonic Distortion	<1% for OdBmo test tone @1004Hz
☐ Idle Noise	≤16dBrnco
☐ Envelope Delay Distortion	≤100μSec, 500-3000Hz
☐ Dynamic Range	+3.5 to −60dBmo

COMMUNICATIONS

System Application



AMERICAN MICROSYSTEMS, INC.

S3501/S3501A, S3502/S3502A

SINGLE CHANNEL μ-LAW PCM CODEC/FILTER SET

Features

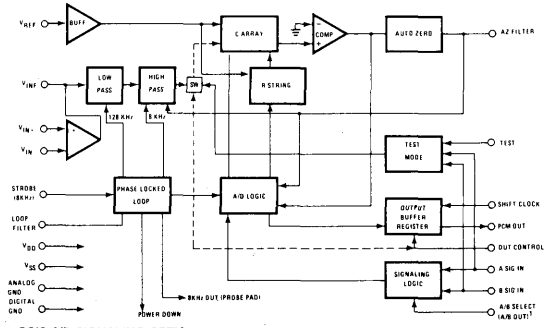
- ☐ CMOS Process for Low Power Dissipation
- ☐ Full Independent Encoder with Filter and Decoder with Filter Chip Set
- ☐ Meets or Exceeds AT&T D3 and CCITT G. 711 and G. 733 Specifications
- ☐ On-Chip Dual Bandwidth Phase-Lock Loop Derives All Timing and Provides Automatic Power Down
- ☐ Low Absolute Group and Relative Delay Distortion
- ☐ Single Negative Polarity Voltage Reference Input
- ☐ Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming
- ☐ Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate
- ☐ Programmable Gain Input/Output Amplifier Stages
- ☐ CCIS* Compatible A/B Signaling Option— S3501A/S3502A

General Description

The S3501 and S3502 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM Channel Bank and PBX systems requiring a μ-255 law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the μ-255 law transfer characteristic. Transmission and reception of 8-bit data words containing the analog information is typically performed at 1.544Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line.

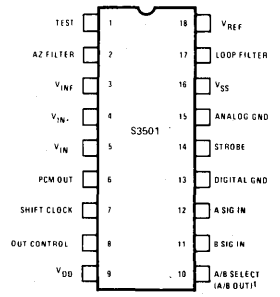
**Common Channel Interoffice Signaling*

S3501 Block Diagram Encoder with Filter



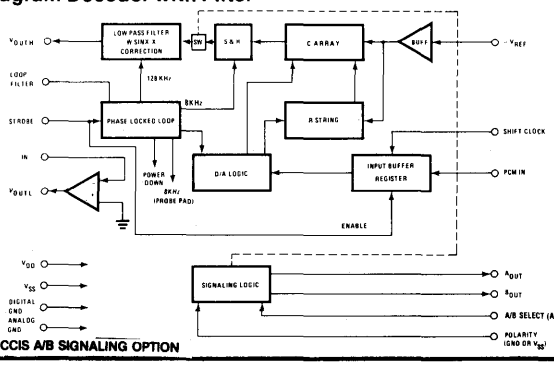
1 CCIS A/B SIGNALING OPTION

Pin Configuration



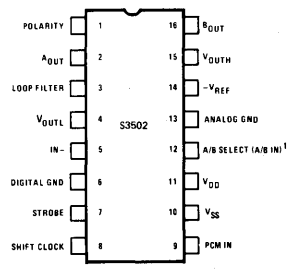
1 CCIS A/B SIGNALING OPTION-S3501A

S3502 Block Diagram Decoder with Filter



CCIS A/B SIGNALING OPTION

Pin Configuration



1 CCIS A/B SIGNALING OPTION-S3502A

S3501 Encoder with Filter Functional Description

S3501 Encoder with Filter chip consists of (1) a bandpass filter with D3 filter characteristic, (2) an analog to digital converter that uses a capacitor array, (3) a phaselock loop that generates all internal timing signals from the externally supplied strobe signal and (4) control logic that performs miscellaneous logic functions.

The band-limiting filter is a 5th order low pass elliptic filter followed by a third order Chebyshev high pass filter. The combined response characteristic (Figure 3) exceeds the D3 filter specifications. Note that the loss below 65Hz is at least 25dB which helps minimize the effect of power frequency induced noise.

The analog to digital converter utilizes a capacitor array based on charge redistribution technique (Ref. 1) to perform the analog to digital conversion with a μ-255 law transfer characteristic (see Figure 4).

The timing signals required for the band-pass filter (128kHz and 8kHz) and analog to digital converter (1.024MHz) are generated by a phase-lock loop comprising a VCO, a frequency divider, a loop filter and a lock detector. The loop locks to the externally supplied 8kHz strobe pulses. In the absence of the strobe pulses, the lock detector detects the unlocked condition and forces the device into a power-down mode thereby reducing power dissipation to a minimum. Thus power-down mode is easily implemented by simply gating the strobe pulses "off" when the channel is idle. The lock-up time, when strobe pulses are gated "on", is approximately 20ms. During this time the device outputs an idle code (all 1's) until lock-up is achieved. Note that signaling information is not transmitted during this time.

The control logic implements the loading of the output shift register, gating and shifting of the data word, signaling logic and other miscellaneous functions. A new analog sample is acquired on the rising edge of the strobe pulse. The data word representing the previous analog sample is loaded into the output shift register at this time and shifted out on the positive transitions of the shift clock during the strobe "on" time. (See Figure 1.) The signaling information is latched immediately after the A/B select input makes a transition. The "A" signaling input is selected after a positive transition and the "B" signaling input is selected after a negative transition. Signaling information is transmitted in the eighth bit position (LSB) of the next frame. (See Figures 1 and 2.) In the CCIS compatible A/B signaling option, the A bit is transmitted during the first data bit time. B bit is transmitted during the remaining 7-bit times. (See Figures 1 and 2.)

"All zero" code suppression is provided so that negative input signal values between the decision value numbers 127 and 128 are encoded as "00000010" after signalling insertion has been done.

S3501 Encoder with Filter Pin Function Descriptions

Strobe: (Refer to Figure 1 for timing diagram.) This TTL compatible input is typically driven by a pulse stream of 8kHz rate. Its active state is defined as a logic 1 level and should be active for a duration of 8 clock cycles of the shift clock. A logic "1" initiates the following functions: (1) instructs the device to acquire a new analog sample on the rising edge of the signal (logic 0 to logic 1 transition); (2) instructs the device to output the data word representing the previous analog sample onto the PCM-out pin serially at the shift clock rate during its active state; (3) forces the PCM-out buffer into an active state. A logic "0" forces the PCM-out buffer into a high impedance state if the Out Control pin is wired to V_{DD}. This input provides the sync information to the phase-lock loop from which all internal timing is developed. The absence of the strobe conveys power-down status to the device. (See functional description of the phase-lock loop for details.)

Shift Clock: This TTL compatible input is typically a square wave signal at 1.544MHz. The device can operate with clock rates from 56kHz (as in the single channel 7-bit PCM system) to 3.152MHz (as in the T1-C carrier system). Data is shifted out of the PCM-out buffer on the rising edges of the clock after a valid logic 0 to logic 1 transition of the strobe signal.

PCM-Out: This is an open drain buffer capable of driving one low power Schottky (74LS) TTL load with a suitable external pull-up resistor (1kΩ). This buffer is in active state (as controlled by the value of the data bit) whenever the strobe signal is a logic 1 and is in a high impedance state when the strobe input is a logic 0 and if the out control pin is wired to V_{DD} supply. When the out control is wired to V_{SS} the state of the output buffer is controlled by the value of the data bit being shifted out. For 56kHz and 64kHz PCM systems where output data is a continuous bit stream, the out control pin should be connected to V_{SS}.

A/B Select: (S3051 only) (Refer to Figure 2 for timing diagram.) This TTL compatible input is provided in order to select the path for the signaling information. It is a transition sensitive input. A positive transition on this input prior to the negative transition of the strobe input selects the "A" signaling input and is transmitted as the eighth bit in the subsequent frame. Similarly, a negative transition causes selection and transmission of informa-

tion on the "B" signaling input. Because it is a transition sensitive input, tying it to V_{DD} or V_{SS} disables A/B signaling.

A SIG IN, B SIG IN: These two TTL compatible inputs are provided to allow multiplexing of signaling information into the transmitted PCM data word in the eighth bit position in accordance with the timing diagram of Figure 2.

A/B Out: (S3501A only.) This is an open drain buffer capable of driving one low power Schottky (74LS) TTL load with a suitable external pull-up resistor 10kΩ). This is an optional output for implementing CCIS compatible A/B signaling. (See Figure 2b.) During data bit 1 time, A signaling bit is output. During remaining 7-bit times, B signaling bit is output. This output is in a high impedance state when strobe is not present.

Out Control: This is a CMOS compatible input and must be wired to either the V_{DD} or V_{SS} (except in 'test' mode). When connected to the V_{SS}, The PCM-out buffer is always in the active state. For continuous analog-to-PCM operation at 56 or 64kb/sec, Out Control should be tied to V_{SS}.

V_{IN-}, V_{IN+}, V_{INF}: These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. V_{IN-} and V_{IN+} are the inputs of a high input impedance op amp and V_{INF} is the output of this op amp. These three pins allow the user complete control over the input stage so that the input stage can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel and testing of the encoder in a stand alone situation. The input stage also allows the user to construct an anti-aliasing filter to provide sufficient suppression at 128kHz. (See Design Considerations on page 13.)

$-V_{REF}$: The input provides the conversion reference for the analog to digital conversion circuit. A value of −3volts is required. The reference must maintain 100ppM/°C regulation over the operating temperature range. A high input impedance buffer is provided on this input which facilitates bussing of the same reference voltage to several devices.

AZ Filter: A capacitor C_{AZ} (nominal .022μF) is required from this pin to analog ground for the functioning of the on-chip auto zero circuit. The most significant bit (sign bit) is filtered by the auto zero circuit and fed back to the input of the A/D converter to compensate for filter output offset variations. This technique insures that the long term average of the sign bit will be zero.

Analog Ground, Digital Ground: Two separate pins are provided for connection of analog signals referenced to analog ground and digital signals referenced to digital ground. This minimizes switching noise associated with the digital signals from affecting the analog signals.

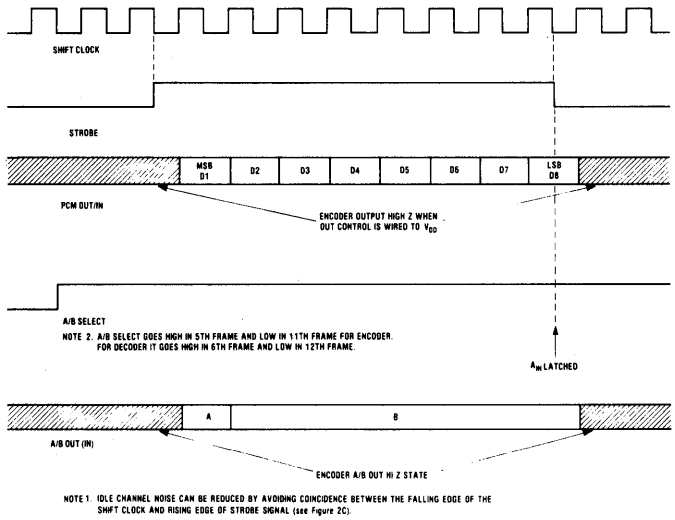
V_{DD}, V_{SS}: These are positive and negative supply pins.

Loop Filter: A capacitor C_{LOOP} (nominal .1μF) is required from this pin to digital ground to provide filtering of the phase comparator output.

Test: This pin is provided to allow for separate testing of the filter and encoder sections of the circuit. The circuit functions normally when this pin is connected to V_{SS}. When this pin is connected to V_{DD}, test mode results. In this mode when A SIG IN and B SIG IN inputs are connected to V_{SS} the filter output is disconnected from the encoder input. The encoder input is connected instead to the Out Control pin. For all other logical combinations of the A SIG IN and B SIG IN inputs the filter output is connected to the Out Control pin.

Ref. 1: *"A Two Chip PCM Voice CODEC with Filters,"* IEEE Journal of Solid State Circuits December 1979.

Figure 1-A. Typical Waveforms in a Time Multiplexed System



NOTE 1: IDLE CHANNEL NOISE CAN BE REDUCED BY AVOIDING COINCIDENCE BETWEEN THE FALLING EDGE OF THE SHIFT CLOCK AND RISING EDGE OF STROBE SIGNAL (see Figure 2C).

Figure 1-B. Waveform Detail

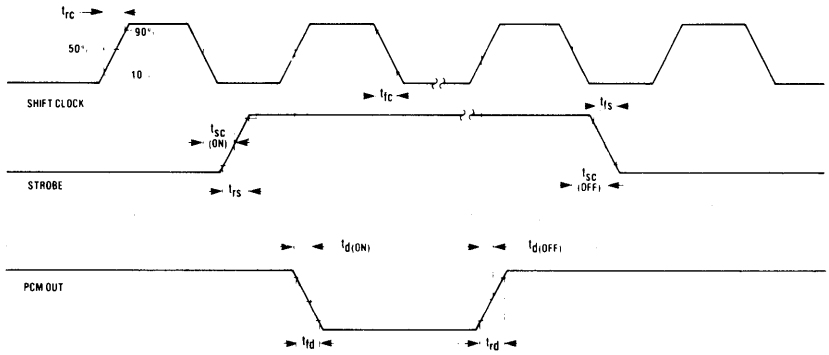
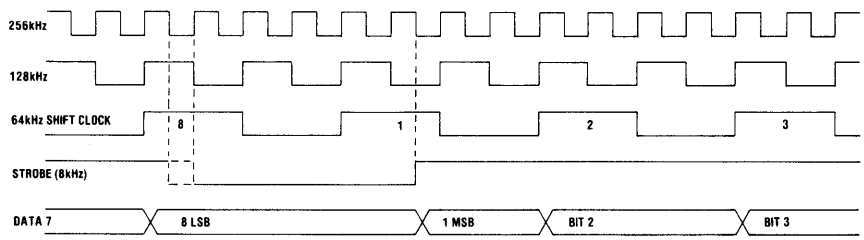


Figure 1-C. 64kHz Continuous Bit Stream Application



NOTES:
1. OUT CONTROL IS WIRED TO V_{SS} FOR CONTINUOUS BIT STREAM OPERATION.
2. THE NEGATIVE TIME OF THE STROBE SHOULD EXCEED ONE SHIFT CLOCK PERIOD.
3. THE CLOCK AND STROBE EDGES SHOULD BE SEPARATED BY AT LEAST 200ns.

Figure 2-A. Encoder A/B Signalling Waveforms

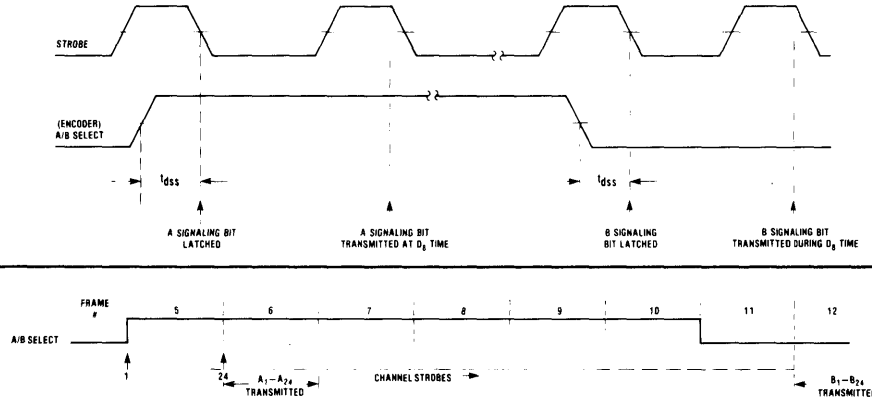


Figure 2-B. CODEC System Timing Diagram

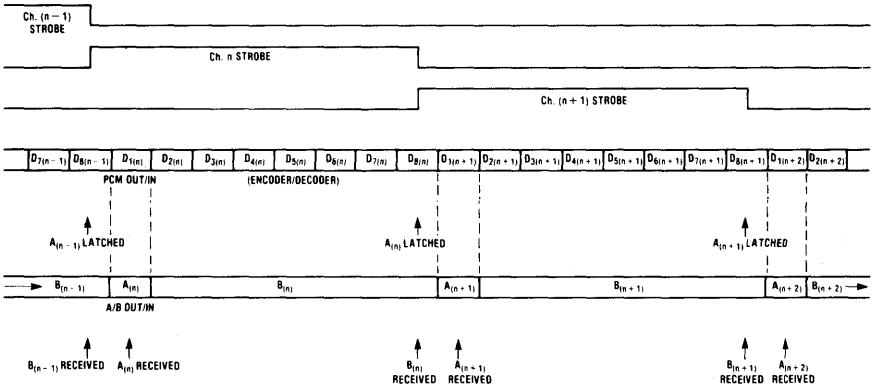
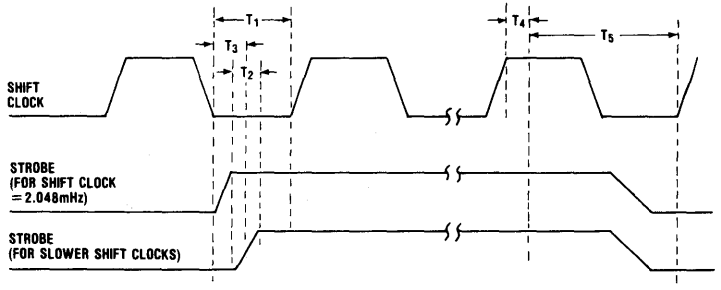


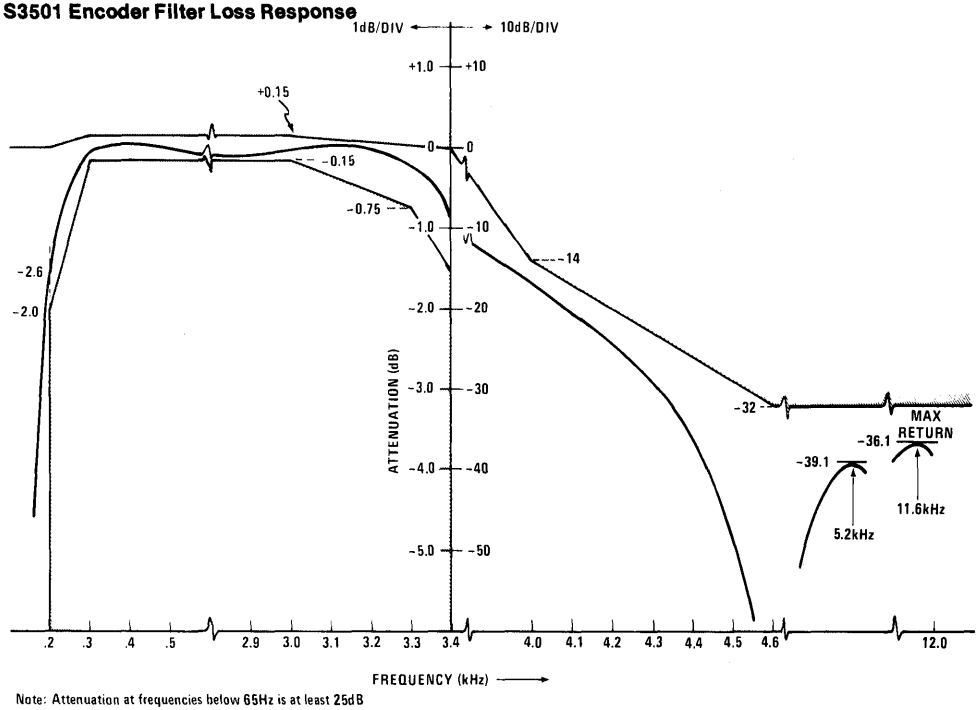
Figure 2-C.



NOTES:

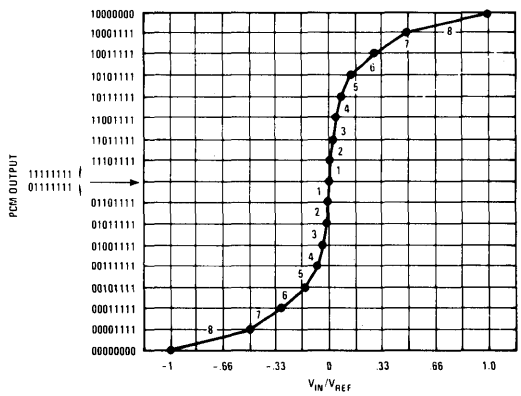
1. THE RISING EDGE OF THE STROBE MUST BE WITH IN T_1 AND THE FALLING EDGE WITHIN T_5. $T_4 = 200$ns (MIN).
2. FOR A 2.048mHz SHIFT CLOCK, IDLE CHANNEL NOISE WILL BE MINIMIZED IF THE RISING EDGE OF THE STROBE OCCURS IN T_3. $T_3 = 100$ns.
3. FOR SLOWER SHIFT CLOCK RATES, IDLE CHANNEL NOISE IS MINIMIZED IF THE RISING EDGE OCCURS IN T_2. FOR EXAMPLE, T_2 IS 125ns FOR A 1.544mHz SHIFT CLOCK.
4. ADJUSTING THE FALLING EDGE OF THE SHIFT CLOCK WILL NOT AFFECT IDLE CHANNEL NOISE.

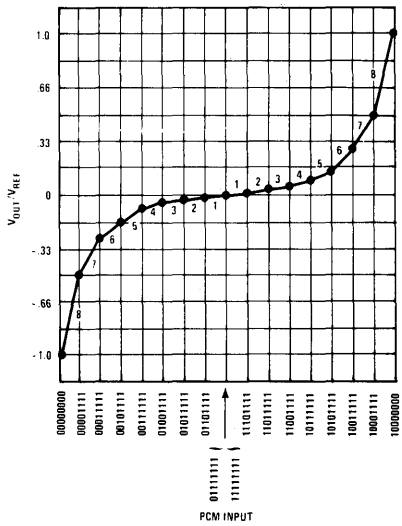
Figure 3. S3501 Encoder Filter Loss Response



Note: Attenuation at frequencies below 65Hz is at least 25dB

Figure 4. μ-255 Law Transfer Characteristics





S3501 Transfer Characteristics

S3502 Transfer Characteristics

S3501 Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	250mW
Digital Input	$-0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input	$-V_{REF} \leq V_{IN} \leq V_{REF}$
$-V_{REF}$	$V_{SS} \leq V_{REF} \leq 0$

S3501 Electrical Operating Characteristics ($T_A = 25°C$)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V+	Positive Supply	4.75	5.0	5.25	V	See Figure 7
V−	Negative Suppply	−4.75	−5.0	−5.25	V	
$-V_{REF}$	Negative Reference	−2.4	−3	−3.10	V	
P_{OPR}	Power Dissipation (Operating)		60	100	mW	
P_{STBY}	Power Dissipation (Standby)		15		mW	

S3501 AC Characteristics (Refer to Figures 1 and 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_d (On)	Shift Clock to PCM Out (On) Delay		140	170	ns	1kΩ, 50pF
t_d (Off)	Shift Clock to PCM Out (Off) Delay		140	170	ns	
t_{rd}	PCM Output Rise Time $C_L = 50pF$		100	125	ns	1kΩ Pull-Up on PCM Out selected for desired rise time
t_{fd}	PCM Output Fall Time $C_L = 50pF$		50	70	ns	
t_{dss}	A/B Select to Strobe Trailing Set Up Time	100			ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P−P Jitter of Strobe Rising Edge			5	μs	

S3501 Encoder DC Characteristics (5V Power Supply, $-V_{REF} = -3.0V$ see Figure 9.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance	10			MΩ	V_{IN-}, V_{IN+} Inputs
C_{IN}	Input Capacitance			10	pF	V_{IN-}, V_{IN+},V_{INF} Inputs
I_{INL}	Logic Input Low Current (Shift Clock, Strobe)			1	μA	$V_{IL} = 0.8V$
I_{INH}	Logic Input High Current			1	μA	$V_{IH} = 2.0V$
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.2			V	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.8	V	$I_{OL} = 5mA$
V_{OL}	Logic Output "Low" Voltage (A/B Out)			0.8	V	$I_{OL} = .1mA$
I_{OH}	PCM Output Off Leakage Current			1	μA	$V_O = 0$ to 5V

S3501 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input = (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	39		dB	−25
	35	38		dB	−30
	32	35		dB	−35
	29	32		dB	−40
	25	28		dB	−45
Gain Tracking		0±.02	±0.25	dB	−10
		0±0.02	±0.25	dB	−20
		0±0.03	±0.25	dB	−25
		0±0.03	±0.25	dB	−30
		−.02±0.04	±0.25	dB	−35
		−.02±0.06	±0.50	dB	−40
		−.02±0.09	±0.50	dB	−45
		−.02±0.13	±0.50	dB	−50
Idle Channel Noise		12.5	19	dBrncO	Analog Input to Analog GND
Transmission Level Point		5.4		dBm	

S3502 Decoder with Filter Functional Description

S3502 Decoder with Filter consists of (1) a digital to analog converter that uses a capacitor array; (2) a low pass filter with D3 filter characteristic; (3) a phase-lock loop that generates all internal timing signals from the externally supplied strobe signal and (4) control logic that performs miscellaneous logic functions.

The digital to analog converter uses a capacitor array based on charge redistribution technique (Ref. 1) to perform the D/A conversion with a μ-255 law transfer characteristic (See Figure 4).

The timing signals required for the low pass filter (128kHz) digital to analog converter (1.024MHz) are generated by a phase-lock loop comprised of a VCO, a frequency divider, a loop filter and a lock detector. The loop locks to the externally supplied 8kHz strobe pulses. In the absence of the strobe pulses, the lock detector detects the unlocked condition and forces the device into a power-down mode thereby reducing power dissipation to a minimum. Thus, power-down mode is easily implemented by simply gating the strobe pulses "off" when the channel is idle. During the power-down mode the output amplifier is forced to a high impedance state and the A, B outputs are forced to inactive state. The lock-up time, when strobe pulses are gated "on", is approximately 20ms. During this time the A/B outputs and the analog output stage are held in the idle state.

The control logic implements the loading of the input shift register, signaling logic and other miscellaneous functions. A new data word is shifted into the input register on a positive transition of the strobe signal at the shift clock rate. The received data is decoded by the D/A converter and applied to the sample and hold circuit. The output sample and hold circuit is filtered by a low pass filter. The low pass filter is a sixth order elliptic filter. The combined response of the sample and hold and the low pass filter is shown in Figure 5.

Signaling information is received and latched immediately after the A/B select input makes a positive or negative transition. On the positive transition of the A/B select input information received in the eighth bit of the data word is routed to the A_{OUT} pin and latched until updated again after the next positive transition of the A/B select input. Similarly "B" signaling information is routed and latched at the B_{OUT} pin after each negative transition of the A/B select input. The A and B outputs are designed such that either relay or TTL compatibility can be achieved (see detailed description under Pin/Function descriptions). In the CCIS compatible A/B signaling option "A" bit is latched during the data bit 1 time and "B" bit is latched during the data bit 8 time.

S3502 Decoder with Filter Pin/Functions Descriptions

Strobe: (Refer to Figure 1 for timing diagram.) This TTL compatible input is typically driven by a pulse stream of 8kHz rate. Its active state is defined as a logic 1 level and is normally active for a duration of 8 clock cycles of the shift clock. It initiates the following functions: (1) instructs the device to receive a PCM data word serially on PCM IN pin at the shift clock rate; (2) supplies sync information to the phase-lock loop from which all internal timing is generated; (3) conveys power-down mode to the device by its absence. (See functional description of the phase-lock loop for details.)

Shift Clock: This TTL compatible input is typically a square wave signal at 1.544MHz. The device can operate with clock rates from 56kHz (as in the single channel 7-bit PCM system) to 3.152MHz (as in the T1-C carrier system). Data is shifted in the PCM IN buffer on the falling edges of the clock after the strobe signal makes a logic 0 to logic 1 transition.

PCM IN: This is a TTL compatible input on which time multiplexed PCM data is received serially at the shift clock rate during the active state of the strobe signal.

A/B Select: (Refer to Figure 6 for timing diagram.) This TTL compatible input is provided in order to select the path for the signaling information. It is a transition sensitive input. A positive transition on this input routes the received signaling bit to the "A" output and a negative transition routes it to the "B" output.

A Out, B Out: These two open drain outputs are provided to output received signaling information. These outputs are designed in such a way that either LS TTL or relay drive compatibility can be achieved. With a suitable pull-up resistor (47KΩ) connected to the LS TTL logic supply, the output voltage will swing between digital ground and the LS TTL logic supply when the Polarity pin is connected to digital ground. (See Figure 6.) The output polarity is the same as the received signaling bit polarity. If the Polarity pin is connected to the V_{SS} supply, the output voltage will swing between V_{SS} and V_{DD} supplies with a suitable pull-up resistor. This facilitates driving a relay by a PNP emitter grounded transistor in −48V systems. The output polarities are inverted from the received signaling bit polarity to facilitate relay driving.

Polarity: This pin is provided for testing purposes and for controlling the A/B output polarities and TTL/relay drive

compatibilities. For TTL compatibility this pin is connected to digital ground. The A/B output polarities are then the same as the received signaling bit polarities. For relay drive capability this pin is connected to the V_{SS} supply. The A/B output polarities then are inverted from the received signaling bit polarities. Test mode results when this pin is connected to V_{DD}. In this mode the decoder output (S&H output) is connected to the B-Out pin while the filter input is connected to the A-Out pin.

$-V_{REF}$: The input provides the conversion reference for the digital to analog conversion circuit and the phase-lock loop. The reference must maintain 100ppM/°C regulation over the operating temperature range. A high input impedance buffer is provided on this input which facilitates bussing of the same reference voltage to several devices.

V_{OUTH}: This is the output of the low pass filter which represents the recreated voice signal from the received PCM data words. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance.

V_{OUTL}, IN−: These two pins are the output and input of the uncommitted output amplifier stage. Signal at the V_{OUTH} pin can be connected to this amplifier to realize a low output impedance with the unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel and testing of the decoder in a stand alone situation.

Analog Ground, Digital Ground: Two separate pins are provided for connection of analog signals referenced to analog ground and digital signals referenced to digital ground. This minimizes switching noise associated with the digital signals from affecting the analog signals.

V_{DD}, V_{SS}: These are the positive and negative power supply pins.

Loop Filter: A capacitor C_{LOOP} (nominal .1μF) is required from this pin to digital ground to provide filtering of the phase comparator output.

A/B IN: (S3502A only) This optional TTL compatible input is provided to implement CCIS compatible A/B signaling scheme.Time multiplexed A, B signaling information is applied at this input and recovered by the decoder as shown in Figure 2-b.

Figure 5. S3502 Decoder Filter with Sample & Hold Loss Response

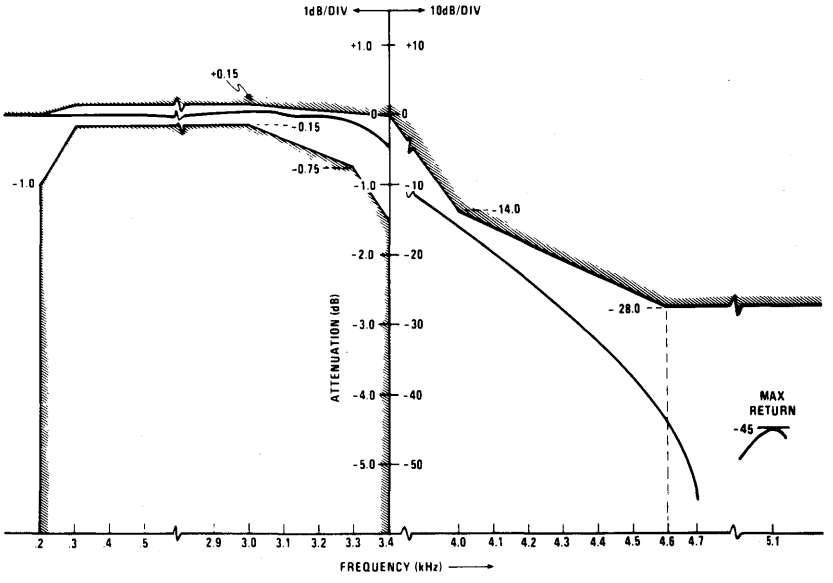


Figure 6-A. Waveform Detail

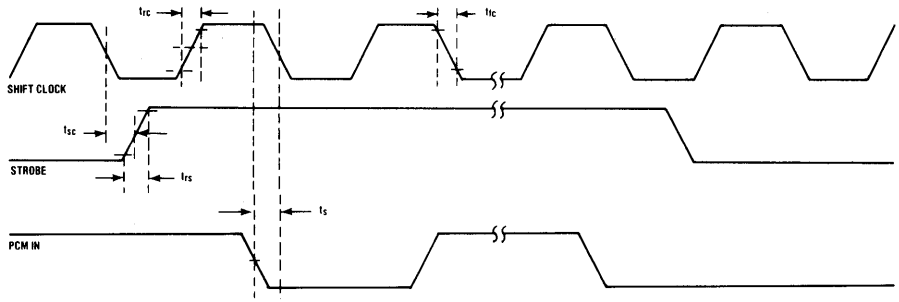
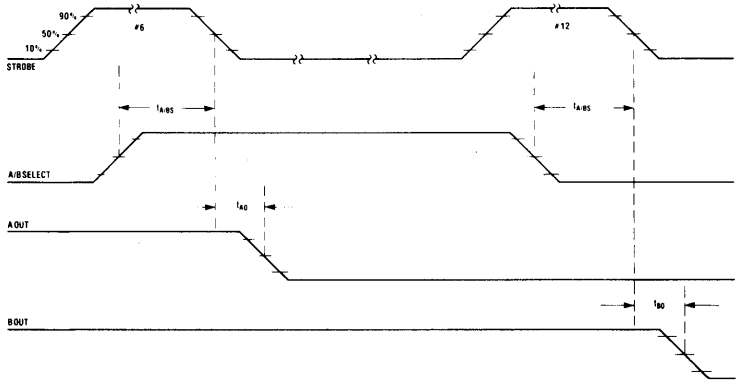


Figure 6-B. Decoder A/B Output Timing



S3502 Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	250mW
Digital Input	$-0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input	$-V_{REF} \leq V_{IN} \leq V_{REF}$
$-V_{REF}$	$V_{SS} \leq V_{REF} \leq 0$

S3502 Electrical Operating Characteristics ($T_A = 25°C$)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V+	Positive Supply	4.75	5.0	5.25	V	See Figure 11
V−	Negative Supply	−4.75	−5.0	−5.25	V	
$-V_{REF}$	Negative Reference	−2.4	−3	−3.1	V	
P_{OPR}	Power Dissipation (Operating)		60	100	mW	
P_{STBY}	Power Dissipation (Standby)		15		mW	

S3502 AC Characteristics (Refer to Figures 1 and 6)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{rd}	PCM Input Rise Time			100	ns	
t_{fd}	PCM Input Fall Time			100	ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P—P Jitter of Strobe Rising Edge			5	μs	
t_s	PCM Input Setup Time	100			ns	
$t_{A/BS}$	A/B Select Set Up Time to Strobe Trailing Edge	100			ns	
t_{AO}, t_{BO}	Strobe Falling Edge to A/B Out Delay			200	ns	

S3502 Decoder DC Characteristics 5V Power Supplies, $-V_{REF}=-3.0V$ (see Figure 11.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$R_L(V_{OUTL})$	Output Load Resistance	600			Ω	
R_{INA}(IN−)	Analog Input Resistance	10			MΩ	
C_{INA}(IN−)	Analog Input Capacitance			10	pF	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{IL}	Logic Input (Shift Clock, Strobe, PCM In) "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.2			V	
I_{INL}	Logic Input "Low" Current			1	μA	$V_{IL}=0.8V$
I_{INH}	Logic Input "High" Current			1	μA	$V_{IH}=2.0V$
V_{OL}	A, B Output "Low" Voltage			0.8	V	Polarity=Dig. Gnd, $I_{OL}=1mA$
V_{OL}	A, B Output "Low" Voltage			$V_{SS}+1.0$	V	Polarity=V_{SS}, $I_{OL}=1mA$

S3502 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input = (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	38.5		dB	−25
	35	39		dB	−30
	32	36.5		dB	−35
	29	33.5		dB	−40
	25	29		dB	−45
Gain Tracking		.02±.02	±0.25	dB	−10
		.04±.02	±0.25	dB	−20
		.04±.03	±0.25	dB	−25
		.03±.03	±0.25	dB	−30
		.04±.04	±0.25	dB	−35
		.04±.05	±0.50	dB	−40
		.1±.05	±0.50	dB	−45
		.15±.07	±0.50	dB	−50
Idle Channel Noise		9	13	dBrncO	PCM Input to Analog GND
0 Transmission Level Point (Digital Milliwatt Response)		4.9		dBm	−3V V_{REF} 600Ω Load

S3501/S3502 System Characteristics Typical Group Delay Characteristic

Device	Abs. Gr. Delay μs f = 1000Hz	Abs. Gr. Delay μs f = 2600Hz	Relative Gr. Delay Distortion (Over Band of 1000 Hz to 2600Hz wrt 1000Hz) μs
Encoder Low Pass	132	220	88
Encoder High Pass	104	22	−82
Encoder Total	236	242	6
Decoder Low Pass	153	250	97
Encoder + Decoder (Total)	389	492	103
End to End Group Delay (Encoder Analog Input to Decoder Analog Output)	639	742	103

Design Considerations

Because the Codec set is required to handle signals with a very large dynamic range, optimal analog performance requires careful attention to the layout of components:

The analog ground, digital ground, V_{DD} and V_{SS} busses should run independently to the power supply, or at least to the edge connector. They should be separate for each chip and should be kept as wide as possible on the printed circuit.

The connections should be as independent as possible. For example (see Figure 7), the 750Ω pull-up resistor to Pin 6 should join the V_{DD} supply at the edge connector and not at the device pin.

Decoupling capacitors should be as close as possible to the power supply pin and analog ground pin.

Digital signal lines should be kept away from analog signals, and separated by an analog ground line where possible for shielding.

3501/3501A Design Guidelines

A recommended S3501 schematic is shown in Figure 7. Parts of the circuit are discussed in more detail below.

Loop Filter Network—For shift clock rates above 512kHz the network in Figure 8 is recommended. For 512kHz or below a .1μF capacitor between pins 13 and 17 is sufficient.

Supply Decoupling—Figure 9 shows the recommended power supply decoupling circuits. The diodes are essential for ±5V power supplies.

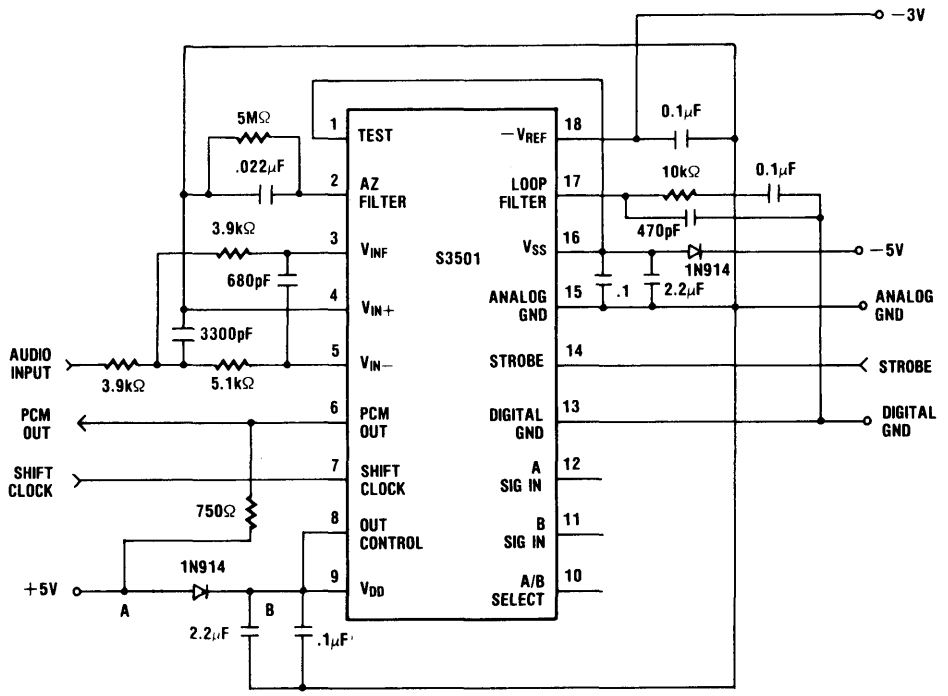
Reference Voltage—pin 18, requires a .1μF capacitor to analog ground. Pin 2, AZ filter, requires a .022μF capacitor to analog ground in parallel with 5MΩ resistor.

Anti-Aliasing

In applications where anti-aliasing pre-filtering is required, an on-chip op-amp may be configured into an active filter (Figure 10). Note that small changes in gain can be made by adjusting the resistor ratio R_1/R_2. Where anti-aliasing is not needed, a 3KΩ-4KΩ resistor can be connected between pins 3 and 5 (inverted gain configuration).

COMMUNICATIONS

Figure 7. Hookup Schematic for S3501 Using 1.544mHz Shift Clock Rate



NOTE: TEST PIN 1 MUST BE CONNECTED TO PIN 16 (NOT −5V) TO PREVENT FORWARD BIASING THE PIN.

Figure 8. Selection of Loop Filter Network

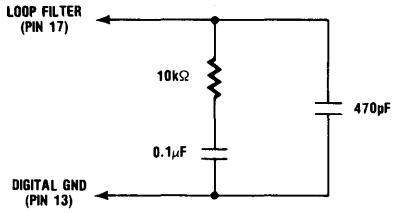


Figure 9-B.
Supply Decoupling for the V_{SS} Supply Pin

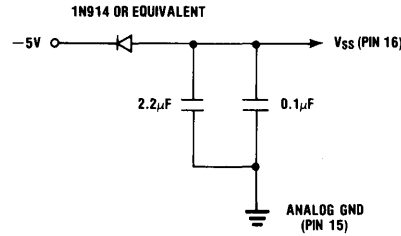


Figure 9-A.
Supply Decoupling for the V_{DD} Supply Pin

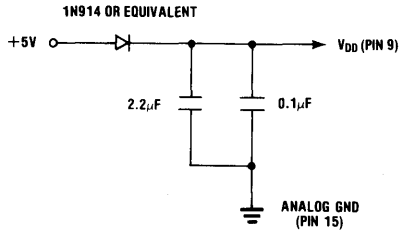
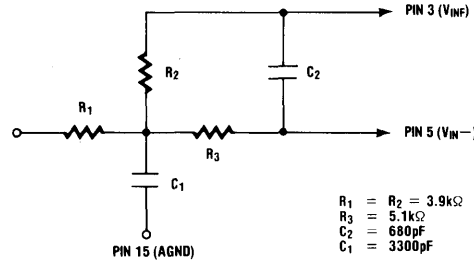


Figure 10. Anti-Aliasing Filter



S3502/S3502A Design Guidelines

Figure 11 depicts a recommended S3502 circuit. All of the following comments apply to Figure 11:

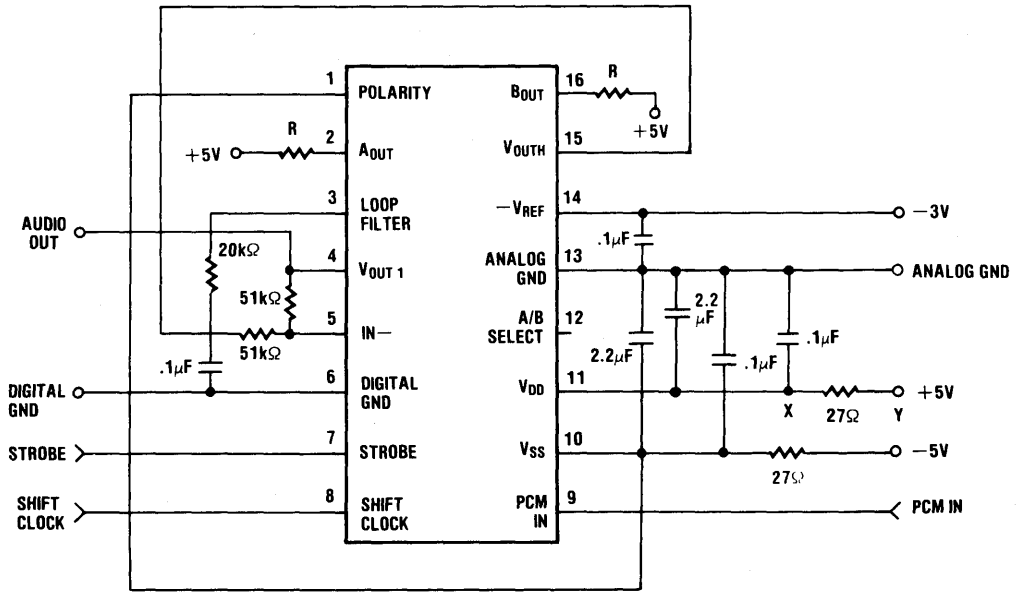
A_{OUT} and B_{OUT} are connected to V_{DD}. R should be larger than 10KΩ to reduce noise.

When pin 1 is connected to DGND (non-inverted signaling with T^2 output levels; not shown in Figure 11), R should be 47KΩ or greater.

Pin 1 should be connected to Pin 10, and not just to −5V, to avoid forward biasing the pin.

The 51KΩ output amplifier resistors should be carefully positioned away from the digital signals.

Figure 11. Hookup Schematic for S3502 Using 1.544mHz Shift Clock Rate



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3503/S3504

SINGLE CHANNEL A-LAW PCM CODEC/FILTER SET

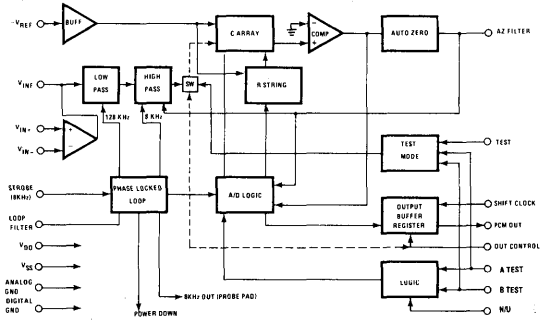
Features

- CMOS Process for Low Power Dissipation
- Full Independent Encoder with Filter and Decoder with Filter Chip Set
- Meets or Exceeds CCITT G.711, G.712 and G.733 Specifications
- On-Chip Dual Bandwidth Phase-Lock Loop Derives All Timing and Provides Automatic Power Down
- Low Absolute Group and Relative Delay Distortion
- Single Negative Polarity Voltage Reference Input
- Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming
- Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate
- Programmable Gain Input/Output Amplifier Stages

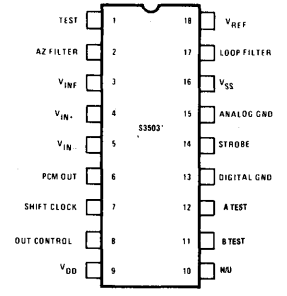
General Description

The S3503 and S3504 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM systems requiring an A-law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the A-law transfer characteristic. Typical transmission and reception of 8-bit data words containing the analog information is performed at 2.048Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line. These chips are pin-for-pin replacements for the S3501/S3502 chip set with the exception of the A-law transfer characteristic conforming to CCITT G.711 and the unused sigaling capability which remains available for special applications.

S3503 Block Diagram Encoder With Filter

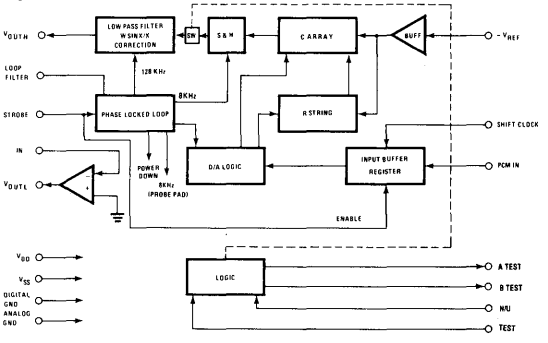


Pin Configuration

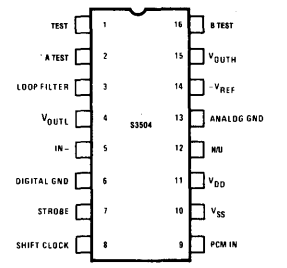


PIN 10, 11, 12 TO V_{DD} FOR NORMAL OPERATION, PIN 1 TO V_{SS}

S3504 Block Diagram Decoder with Filter



Pin Configuration



PIN 1 TO DIGITAL GROUND, PIN 2, 16 OPEN FOR NORMAL OPERATION

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S3506/S3507/S3507A

CMOS SINGLE CHIP μ-LAW/A-LAW COMBO CODECS WITH FILTERS

COMMUNICATIONS

Features

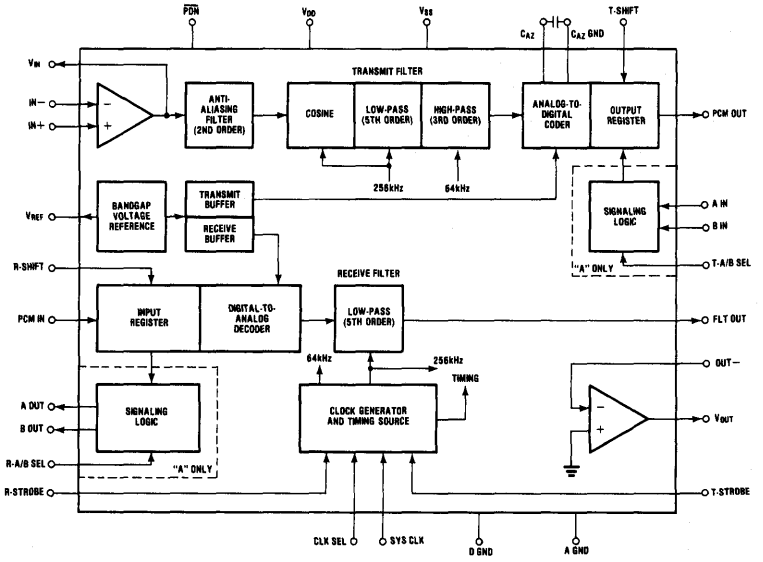
- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 8mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ±3.1V into a 1200Ω Load or Can Be Switched Off for Reduced Power (70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-Up
- ☐ Low Absolute Group Delay = 450μsec. @ 1kHz

General Description

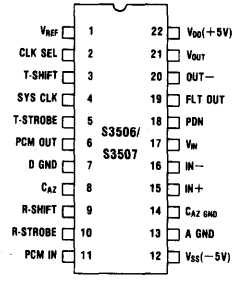
The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

These circuits provide the interface between the analog signals of the subscriber loop and the digital signals of the PCM highway in a digital telephone switching system.

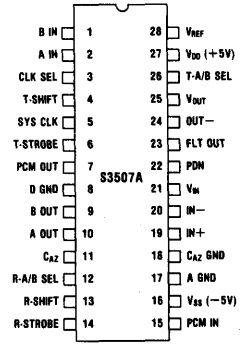
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)



General Description (Continued)

The devices operate from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or time-slot asynchronous operation.

In 22-pin cerdip or ceramic packages (.400″ centers) the S3506/S3507 are ideally suited for PCM applications: Exchange, PABX, Channel bank or Digital Telephone as well as fiber optic and other non-telephone uses. A 28-pin version, the S3507A, provides standard μ-Law A/B signaling capability. These devices are also available in a 28-pin chip carrier (see page 9). Extended temperature range versions can be supplied.

Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	−40°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	1000mW
Digital Input	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input	$V_{SS} - 0.3 \leq V_{IN} \leq V_{DD} + 0.3$

Electrical Operating Characteristics ($T_A = 0°$ to 70°C)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}	Positive Supply	4.75	5.0	5.25	V	
V_{SS}	Negative Supply	−4.75	−5.0	−5.25	V	
P_{OPR}	Power Dissipation (Operating)		80	110	mW	
P_{OPR}	Power Dissipation (Operating w/o Output Op Amp		70		mW	V_{DD} = 5.0V V_{SS} = −5.0V
P_{STBY}	Power Dissipation (Standby)		8	12	mW	

AC Characteristics (Refer to Figures 3A and 4A)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
D_{SYS}	System Clock Duty Cycle	40	50	60	%	
f_{SC}	Shift Clock Frequency	0.064		2.048	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}	Shift Clock to Strobe (On) Delay	−100	0	200	ns	
t_{sw}	Strobe Width	600ns		124.3μs	@2.048 MHz	700ns min @1.544MHz
t_{cd}	Shift Clock to PCM Out Delay		100	150	ns	100pF, 510Ω Load
t_{dc}	Shift Clock to PCM in Set-Up Time	60			ns	
t_{rd}	PCM Output Rise Time C_L=100pF		50	100	ns	to 3V; 510Ω to V_{DD}
t_{fd}	PCM Output Fall Time C_L=100pF		50	100	ns	to .4V; 510Ω to V_{DD}
t_{dss}	A/B Select to Strobe Trailing Edge Set-up Time	100			ns	

DC Characteristics (V_{DD} = +5V, V_{SS} = −5V)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance IN+, IN−	100			KΩ	
C_{IN}	Input Capacitance to Ground		7	15	pF	All Logic and Analog Inputs
	Shift Clock, PCM IN, System Clock, Strobe, $\overline{PDN}$					
I_{INL}	Logic Input Low Current			1	μA	V_{IL} =0.8V
I_{INH}	Logic Input High Current			1	μA	V_{IH} = 2.0V
	A/B Sel, A IN B IN					
I_{INL}	Logic Input Low Current			600	μA	V_{IL} = 0.8V
I_{INH}	Logic Input High Current			600	μA	V_{IH} = 2.0V
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.0			V	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.4	V	510Ω Pull-up to V_{DD} + 2 LSTTL
V_{OL}	Logic Output "Low" Voltage(A/B Out)			0.4	V	I_{OL} = 1.6mA
V_{OH}	Logic Output "High" Voltage	2.6			V	I_{OH} = 40μA
R_L	Output Load Resistance V_{OUT}	1200			Ω	

Transmission Delays

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Encoder		125		μs	From T_{STROBE} to the Start of Digital Transmitting
	Decoder	30	8T+25		μs	T=Period in μs of R_{SHIFT} CLOCK
	Transmit Section Filter			182	μs	@1kHz
	Receive Section Filter			110	μs	@1kHz

S3506 Single-Chip A-Law Filter/Codec Performance

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)		−85	−73	dBmOp	CCITT G.712 4.1
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)			−60	dBmO	CCITT G.712 4.2
ICN_R	Idle Channel Noise (Receive Section)			−78	dBmOp	CCITT G.712 4.3
	Spurious Out-of-Band Signals at Channel Output			−28	dBmO	CCITT G.712 6.1
IMD_{2F}	Intermodulation (2 Tone method)			−35	dBm	CCITT G.712 7.1
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)			−49	dBm	CCITT G.712 7.2
	Spurious In-Band Signals at the Channel Output Port			−40	dBmO	CCITT G.712 9
	Interchannel Crosstalk $V_{IN} - V_{OUT}$	75	80		dB	CCITT G.712 11
$V_{IN(Max)}$	Max Coding Analog Input Level		±3.1		V_{Opk}	
V_{OUT} (Max)	Max Coding Analog Output Level		±3.1		V_{Opk}	R_L=1.2KΩ

S3506 Single-Chip μ-Law Filter/Codec Performance (Continued)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ OdBmO
ED	Envelope Delay Distortion	500 to 600Hz		200	750	μsec	Relative to Minimum Delay Frequency
		600 to 1000Hz		120	375	μsec	
		1000Hz to 2600Hz		110	125	μsec	
		2600Hz to 2800Hz		160	750	μsec	
SD	Signal to Total Distortion	0 to −30dBmO	36	39		dB	Method 2 - Sine-wave Signal Used
		−40dBmO	29	31		dB	
		−45dBmO	24	26		dB	
GT	Gain Tracking with Input Level Variations (End-to-End. Each half channel is one half this value.)			±0.2 ±0.4 ±1.0	±0.5 ±1.0 ±3.0	dB dB dB	+3 to −40 dBmO −45 to −50 dBmO −55dBmO
ΔG	Gain Variation with Temperature and Power Supply Variation			±0.25		dB	
	Transmit Gain Repeatability			±0.1	±0.2	dB	
	Receive Gain Repeatability			±0.1	±0.2	dB	
$0TLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.51		VRMS	V_{OUT} Digital Milliwatt Response
$0TLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milliwatt Response at Decoder

S3507/S3507A Single-Chip μ-Law Filter/Codec Performance

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)		5	17	dBrncO	
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)			−60	dBmO	
ICN_R	Idle Channel Noise (Receive Section)			15	dBrncO	
	Spurious Out-of-Band Signals at the Channel Output			−28	dBmO	
IMD_{2F}	Intermodulation (2 Tone method)			−35	dBm	
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)			−49	dBm	
	Spurious In-Band Signals at the Channel Output Port			−40	dBmO	
	Interchannel Crosstalk $V_{IN}-V_{OUT}$	75	80		dB	
$V_{IN(Max)}$	Max Coding Analog Input Level		±3.1		V_{Opk}	
V_{OUT} (Max)	Max Coding Analog Output Level		±3.1		V_{Opk}	R_L 1.2KΩ
GT	Gain Tracking with Input Level Variations (End-to-End. Each half channel is one half of this value.)		±0.2 ±0.4 ±1.0	±0.5 ±1.0 ±3.0	dB dB dB	+3 to −40 dBmO −45 to −50 dBmO −55dBmO
ΔG	Gain Variation with Temperature and Power Supply Variation		±0.25		dB	
	Transmit Gain Repeatability		±0.1	±0.2	dB	
	Receive Gain Repeatability		±0.1	±0.2	dB	

S3507/S3507A Single-Chip μ-Law Filter/Codec Performance (Continued)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
$0TLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.51		VRMS	V_{OUT} Digital Milliwatt Response
$0TLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milliwatt Response at Decoder
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ OdBmO
ED	Envelope Delay Distortion	500 to 600Hz		200	750	μsec	Relative to Minimum Delay Frequency
		600 to 1000Hz		120	375	μsec	
		1000Hz to 2600Hz		110	125	μsec	
		2600Hz to 2800Hz		160	750	μsec	
SD	Signal to Total Distortion	0 to −30dBmO	36	39		dB	
		−40dBmO	29	31		dB	
		−45dBmO	24	26		dB	

COMMUNICATIONS

Pin/Function Descriptions

Pin	S3506/S3507	S3507A	Description
SYS CLK	4	5	**System Clock 256kHz**—This pin is a TTL compatible input for a 256kHz, 1.544MHz, 2048MHz, or 1.536MHz clock that is divided down to provide the filter clocks. The status of CLK SEL pin must correspond to the provided clock frequency.
T-SHIFT	3	4	**Transmit Shift Clock**—This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
R-SHIFT	9	13	**Receive Shift Clock**—This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
T-STROBE	5	6	**Transmit Strobe**—This TTL compatible pulse input (8kHz) is used for analog sampling and for initiating the PCM output from the coder. It must be synchronized with the T-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
R-STROBE	10	14	**Receive Strobe**—This TTL compatible pulse input (8kHz) initiates clocking of PCM input data into the decoder. It must be synchronized with the R-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
CLK SEL	2	3	**Clock Select**—This pin selects the proper divide ratios to utilize either 256kHz, 1.544MHz, 2.048MHz, or 1.536MHz as the system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz, to V_{SS} (−5V) for 1.544MHz or 1.536MHz operation, or to D GND for 256kHz operation.
PCM OUT	6	7	**PCM Output**—This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of T-SHIFT clock signal following a positive edge of the T-STROBE input. Data is clocked out by the positive edge of the T-SHIFT clock into one 510Ω pull-up per system plus 2 LS-TTL inputs.
PCM IN	11	15	**PCM Input**—This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of T-SHIFT clock.
C_{AZ} C_{AZ} GND	8 14	11 18	**Auto Zero**—A capacitor of 0.1μF ±20% should be connected between these pins for coder auto zero operation. Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
V_{REF}	1	28	**Voltage Reference**—Output of the internal band-gap reference voltage (≈−3.075V) generator is brought out to V_{REF} pin. Do not load this pin.
IN+ IN− V_{IN}	15 16 17	19 20 21	These pins are for analog input signals in the range of $-V_{REF}$ to $+V_{REF}$. IN− and IN+ are the inputs of a high input impedance op amp and V_{IN} is the output of this op amp. These three pins allow the user complete control over the input stage so that it can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel. V_{IN} should not be loaded by less than 47K ohms.
FLT OUT	19	23	**Filter Out**—This is the output of the low pass filter which represents the recreated analog signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 47K ohms, or the Digital MilliWatt response will fall off slightly.

Pin/Function Descriptions (Continued)

Pin	S3506/S3507	S3507A	Description
OUT− V_{OUT}	20 21	24 25	These two pins are the output and input of the uncommitted output amplifier stage. Signal at the FLT OUT pin can be connected to this amplifier to realize a low output impedance with unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel. The V_{OUT} pin has the capability of driving OdBm into a 600Ω load. (See Figure 1). If Out− is connected directly to V_{SS} the op amp will be powered down, reducing power consumption by 10mW, typically.
V_{DD} V_{SS}	22 12	27 16	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins, respectively (typ. +5V, −5V). The voltages should be applied simultaneously or V_{SS} should be applied first.
A GND D GND	13 7	17 8	Analog and digital ground pins are separate for minimizing crosstalk.
$\overline{PDN}$	18	22	**$\overline{\text{Power Down}}$**—This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high or low, but as long as they are static, the powered down mode is in effect.
A IN B IN T-A/B SEL		2 1 26	The transmit A/B select input selects the A signal input in a positive transition and the B signal input on the negative transition. These inputs are TTL compatible. The A/B signaling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronized to the T-STROBE input in each device.
A OUT B OUT R-A/B SEL		10 9 12	In the decoder the A/B signaling bits received in the PCM input word are latched to the respective outputs in the same frame in which the R-AB SEL input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.

COMMUNICATIONS

Functional Description

The simplified block diagram of the S3506/S3507 appears on page one. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A band-gap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analog signals first enter the chip at the uncommitted op amp terminals. This op amp allows gain trim to be used to set 0TLP in the system. From the V_{IN} pin the signal enters the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typ.) at 256kHz and 46dB (typ.) at 512Hz. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 256kHz, followed by a 3rd Order High-Pass Filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are >26dB (typ) from 0 to 60Hz and >35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analog-to-digital conversion process requires 9½ clock cycles, or about 72μs. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

The PCM data word is formatted according to the μ-law companding curve for the S3507 with the sign bit and the ones complement of the 7 magnitude bits according to the AT&T D3 specification. In the S3506 the PCM data word is formatted according to the A-Law companding curve with alternate mark inversion (AMI), meaning that the even bits are inverted per CCITT specifications.

Included in the circuitry of the S3507/S3507A is "All Zero" code suppression so that negative input signal values between decision value numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronization by T1 line clock recovery circuitry as there are never more than 15 consecutive zeros. The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz.

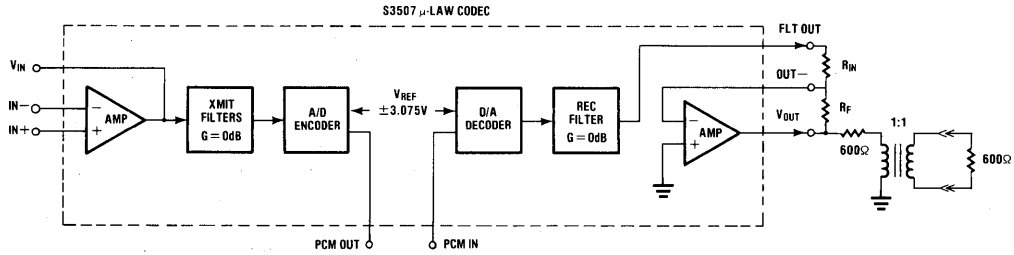
Idle Channel Noise Suppression

An additional feature of the CODEC is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of the chip is such that for 250msec. the only code words generated were +0, −0, +1, or −1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation, resetting the 250msec. timer. This feature is a form of Idle Channel Noise or Crosstalk Suppression. It is of particular importance in the S3506 A-Law version because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 47kΩ. When used in this fashion the low impedance output amp can be switched off for a savings in power consumption. When it is required to drive a 600Ω load the output is configured as shown in Figure 1 allowing gain trimming as well as impedance matching. With this configuration a transmission level of 0dBm can be delivered into the load with the +3.14dB or +3.17dB overload level being the maximum expected level.

Figure 1. S3507 Input/Output Reference Signal Levels



$$\text{IN VOLTS, } \emptyset TLP_{RMS} = .707\,(V_{REF} - 3.17dB)$$

$$= .707\left[3.075\left(10^{\frac{-3.17}{20}}\right)\right]$$

$$= 1.51 \text{ VRMS}$$

WHERE V_{REF} = 3.075 VDC AND THE OVERLOAD IS 3.17dB

$$\text{IN dBm, } \emptyset_{TLP} = 20 \text{ LOG } \frac{V_{\emptyset TLP}}{V_{\emptyset DBM}}$$

$$= 20 \text{ LOG } \frac{1.51}{.775}$$

$$= 5.8dBm$$

WHERE 0dBm = 1mW INTO 600Ω

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct is to drive the $\overline{PDN}$ pin to a low level. Stopping both the transmit strobe and the receive strobe will also put the chip into the stand-by mode. The strobes can be held high or low.

Voltage Reference Circuitry

A temperature compensated band-gap voltage generator (−3.075V) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed during assembly to ensure a minimum gain error of ±0.2dB due to all causes. The V_{REF} pin should not be connected to any load.

Power Supply and Clock Application

For proper operation V_{DD} and V_{SS} should be applied simultaneously. If not possible, then V_{SS} should be applied first. To avoid forward-biasing the device the clock voltages should not be applied before the power supply voltages are stable. When cards must be plugged into a "hot" system it may be necessary to install 1000Ω current-limiting resistors in series with the clock lines to prevent latch-up.

Timing Requirements

The internal design of the Single-Chip CODEC paid careful attention to the timing requirements of various systems. In North America, central office and channelbank designs follow the American Telephone and Telegraph Company's T1 Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Yet, in digital telephone designs, CODEC's may be used in a non-multiplexed form with a data rate as low as 64kb/s. The S3507 and S3507A fill these requirements.

In Europe, telephone exchange and channelbank designs follow the CCITT carrier PCM format to multiplex 30 voice channels at a data rate of 2.048Mb/s. The S3506 is designed for this market and will also handle PABX and digital telephone applications requiring the A-Law transfer characteristics.

The timing format chosen for the AMI Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kb/s to 2.048Mb/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, the S3506/S3507 does not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe, forcing the PCM output in a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and transmit/receive shift clocks are synchronized to it. Figure 2 shows the waveforms in typical multiplexed uses of the CODEC.

System Clock

The basic timing of the Codec is provided by the system clock. This 2.048MHz, 1.544MHz, or 256kHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. In most systems this clock will also be used as the shift clock to clock in and out the data. However, the shift clock can actually be any frequency between 64kHz and 2.048MHz as long as one of the two system clock frequencies is provided. Independent strobes and shift clocks allow asynchronous time slot operation of transmit and receive. The 3507 will also operate with a 1.536 system clock, as used in some PABX systems, with the CLK SEL pin in the 1.544 MHz Mode.

Signaling in μ-Law Systems

The S3506 and S3507 are compact 22-pin devices to meet the two worldwide PCM standards. In μ-Law systems there can be a requirement for signaling information to be carried in the bit stream with the coded analog data. This coding scheme is sometimes called 7-5/6 bit rather than 8 bit because the LSB of every 6th frame is replaced by a signaling bit. This is referred to as A/B Signaling and if a signaling frame carries the "A" bit, then 6 frames later the LSB will carry the "B" bit. To meet this requirement, the S3507A is available in a 28-pin dip package, or in a 28-pin dip carrier, as 6 more pins are required for the inputs and outputs of the A/B signaling.

Pin Configuration—S3507A 28-Lead Chip Carrier

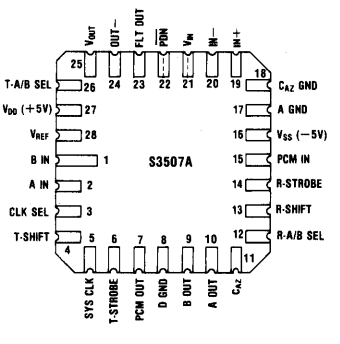
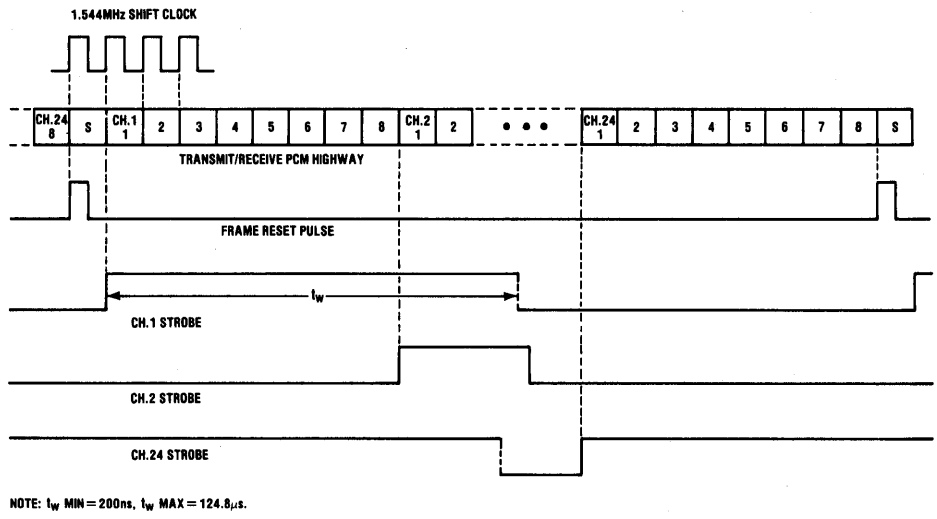
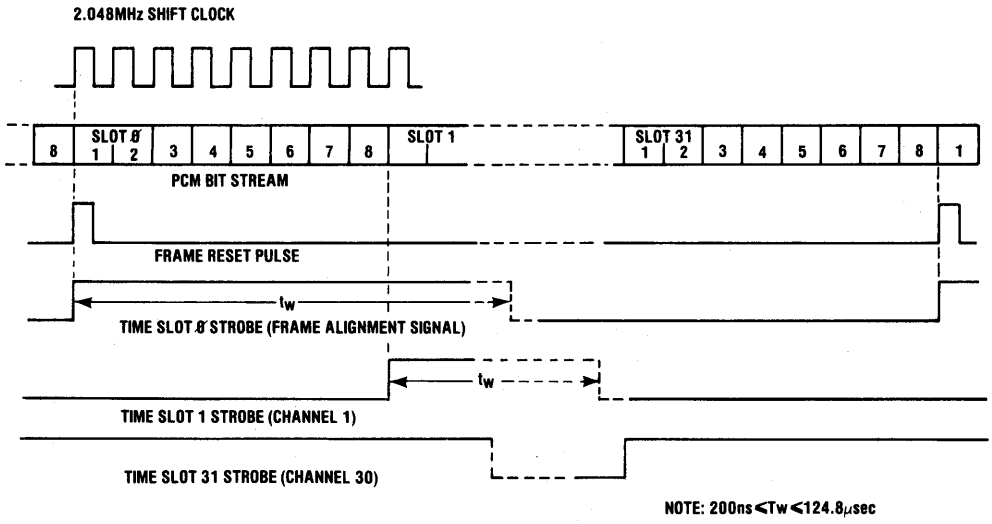


Figure 2A. Waveforms in a 24 Channel PCM System



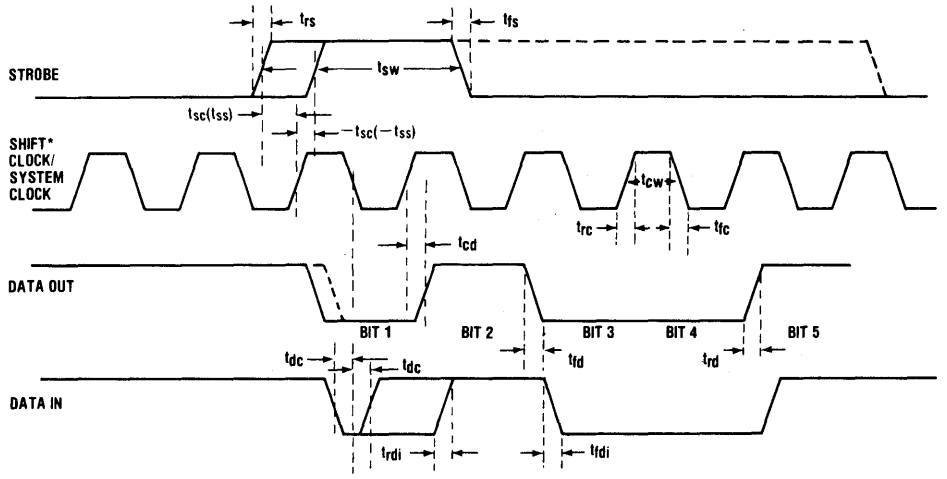
NOTE: t_W MIN = 200ns, t_W MAX = 124.8μs.

Figure 2B. Waveforms in 30 Channel PCM System



NOTE: 200ns $\leq$ Tw $\leq$ 124.8μsec

Figure 2C. Waveform Details



*In this example the shift clock is the system clock (1.544 or 2.048MHz). In systems where the data shift rate is not the same the relationship of each to the strobe remains the same. The system clock and shift clock need not have coincident edges, but must relate to the strobe within the t_{sc}, t_{ss} timing requirements.

The effect of the strobe occurring after the shift clock is to shorten the first (sign) bit at the data output.

The length of the strobe is not critical. It must be at a logic state longer than one system clock cycle. Therefore, the minimum would be >488ns at 2.048 and the maximum <124.3μsec at 1.544MHz.

	MIN	MAX
t_{cw}	195nsec.	9.38μsec.
t_{rs}		100ns
t_{fs}		100ns
t_{sc}	−100nsec.	200ns ‡
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	600ns*	124.3μsec.
t_{cd}	100nsec.	150ns
t_{dc}	60nsec.	
t_{rdi}		100ns
t_{fdi}		100ns

‡That is, the strobe can precede the shift clock by 200nsec, or follow it by as much as 100nsec.

*@2.048MHz 700ns @1.544MHz

Signaling Interface

In the AT&T T1 carrier PCM format an A/B signaling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground, etc., depending on the application. Two signaling conditions (A and B) per channel, giving four possible signaling states per channel are repeated every 12 frames (1.5 milliseconds). The A signaling condition is sent in bit 8 of all 24 channels in frame 6. The B signaling conditions is sent in frame 12. In each frame, bit 193 (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The S3507A in a 28-pin package is designed to simplify the signaling interface. For example, the A/B select input pins are transition sensitive. The transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronizes the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channelbank. The A and B signaling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore, A/B select input must go positive in the beginning of frame 5 and the negative in the beginning of frame 11 (see Figure 3).

Figure 3. Signaling Waveforms in a T1 Carrier System

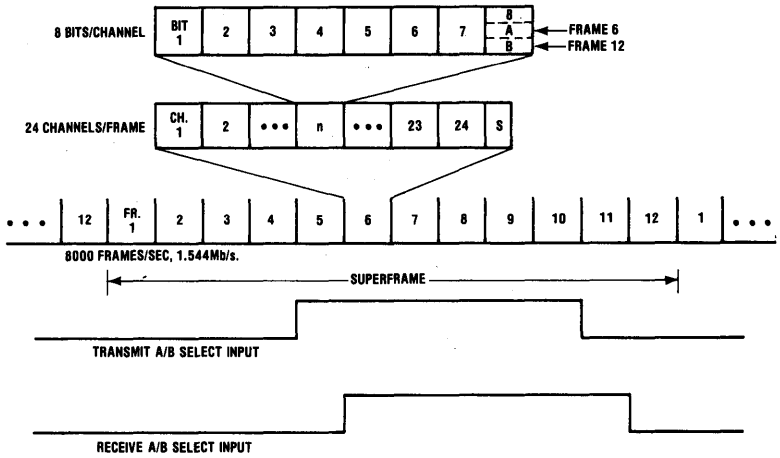
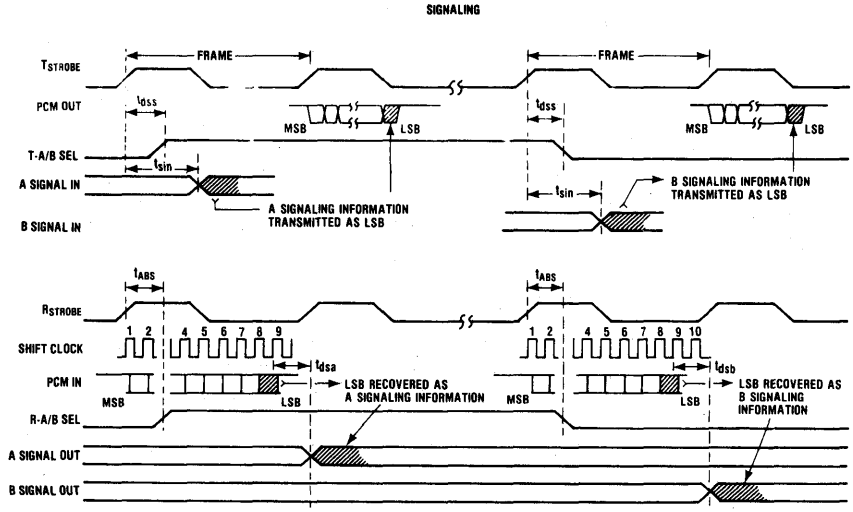
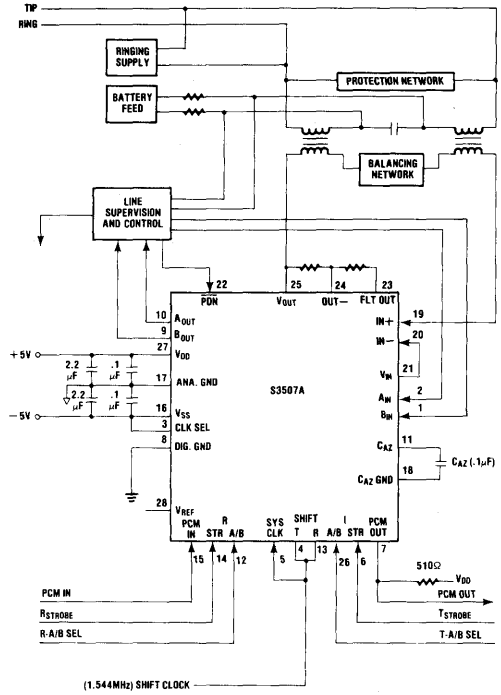


Figure 3A.. Signaling Waveform Details



	t_{dss}	t_{sin}	t_{ABS}	t_{dsa}	t_{dsb}
max	1.4μs	80μs	3μs	300ns	300ns

Figure 4. A Subscriber Line Interface Circuit



The decoder uses a similar scheme for receiving the A and B signaling bits, with one difference. They are latched to the respective outputs in the same frame in which the A/B select input makes a transition. Therefore, the receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

Applications Examples

There are two major categories of Codec applications. Central office, channel bank and PABX applications using a multiplex scheme, and digital telephone type dedicated applications. Minor applications are various A/D or D/A needs where the 8 bit word size is desirable for μP interface and fiber optic multiplex systems where non-standard data rates may be used.

A Subscriber Line Interface Circuit

Figure 4 shows a typical diagram of a subscriber line interface circuit using the S3507A. The major elements of such a circuit used in the central office or PABX are a two-to-four wire converter, PCM Codec with filters (S3507A) and circuitry for line supervision and control. The two-to-four wire converter—generally implemented by a transformer-resistor hybrid—provides the interface between the two-wire analog subscriber loop and the digital signals of the time-division-multiplexed PCM highways. It also supplies battery feed to the subscriber telephone. The line supervision and control circuitry provides off-hook and disconnect supervision, generates ringing and decodes rotary dial pulses. It supplies the A/B signaling bits to the coder for transmission within the PCM voice words. It receives A/B signaling outputs from the decoder and operates the A/B signaling relays.

In the T1 carrier system, 24 voice channels are multiplexed to form the transmit and receive highways, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mb/s.

Within the channelbank the transmit and receive channels of a Codec can occupy the same time slot for a synchronous operation or they can be independent of each other for time slot asynchronous operation. Asynchronous operation helps minimize switching delays through the system. Since the strobe or sync pulse for the coder and decoder sections is independent of each other in the S3507A, it can be operated in either manner.

In the CCITT carrier system, 30 voice channels and 2 framing and signaling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mb/s.

The line supervision and control circuitry within each subscriber line interface can generate all the timing signals for the associated Codec under control of a central processor. Alternatively, a common circuitry within the channelbank can generate the timing signals for all channels. Generation of the timing signals for the S3506 and S3507 is straightforward because of the simplified timing requirements (see Timing Requirements for details). Figures 5 and 5A show design schemes for generating these timing signals in a common circuitry. Note that only three signals: a shift clock, a frame reset pulse (coincident with the S bit) and a superframe reset pulse (coincident with the S bit in Frame 1) are needed. These signals are generated by clock recovery circuitry in the channelbank. Since the AMI Codec does not need channel strobes to be exactly 8-bit periods wide, extra decoding circuitry is not needed.

Figure 5. Generating Timing Signals in a T1 Carrier System

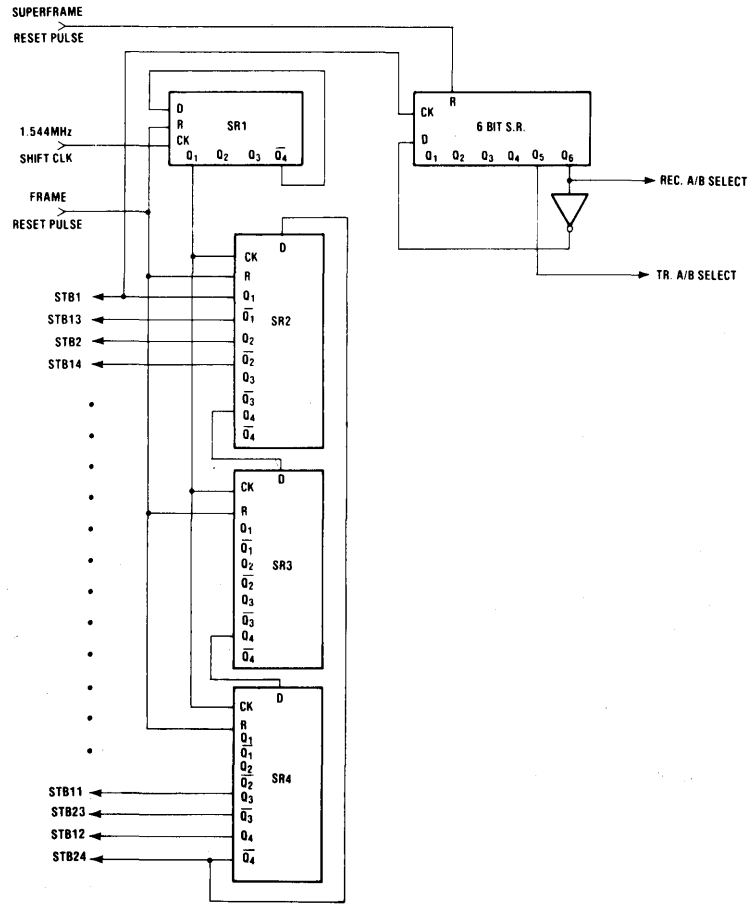
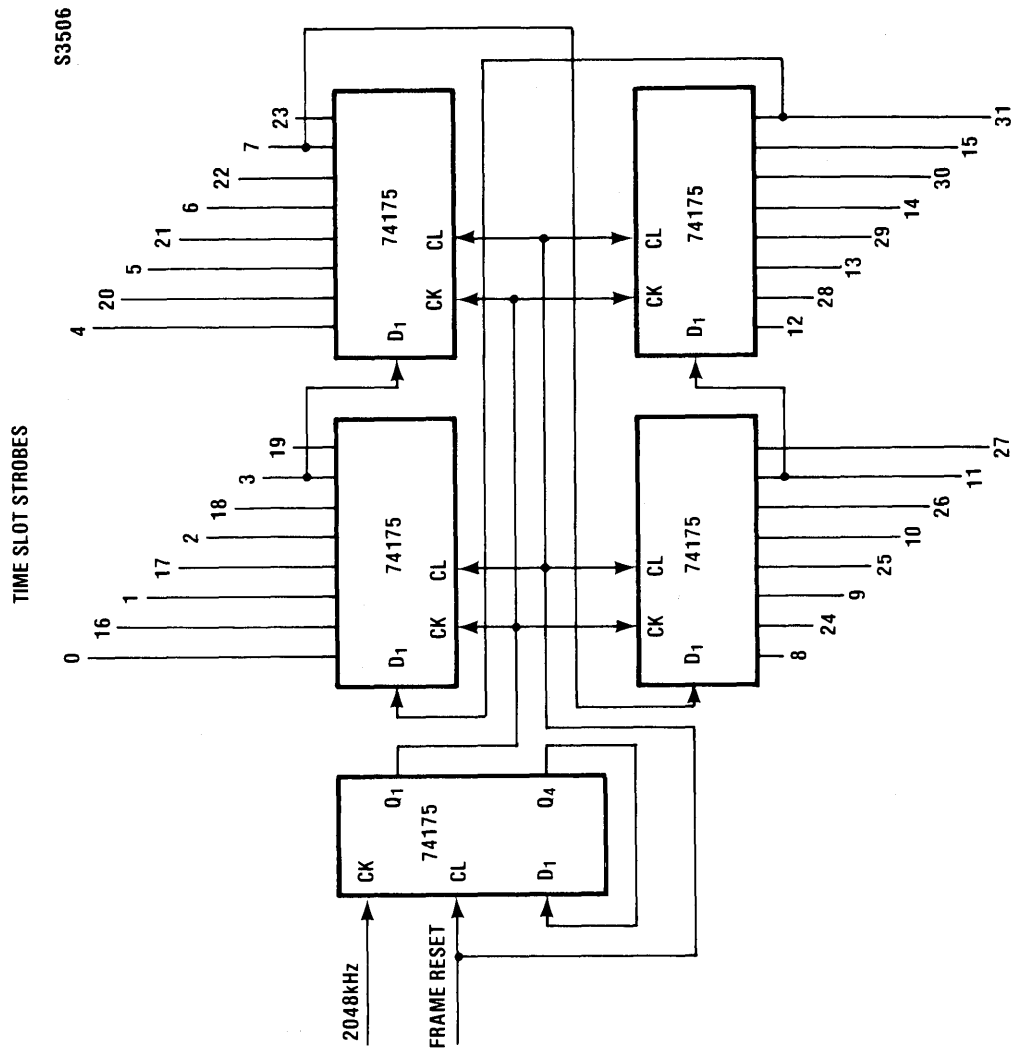


Figure 5A. Generating Timing Signals in a CCITT Carrier System (30+2 Channels)

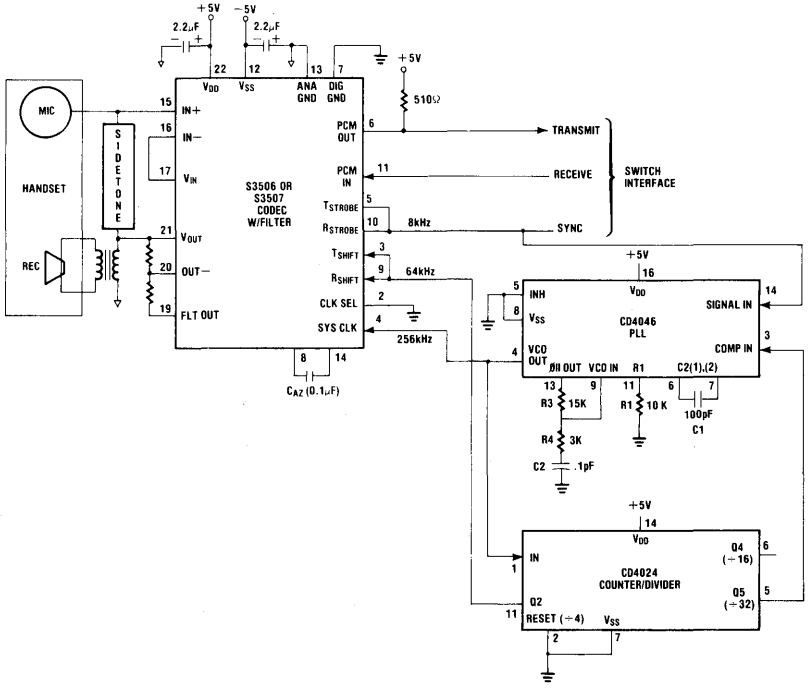


A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs to interface to the switch. Two pairs carry transmit and receive PCM voice data. One pair supplies an 8kHz synchronizing clock signal and the remaining pair supplies power to the telephone. More sophisticated designs reduce costs by time-division-multiplexing and superimposition techniques which minimize the number of wire pairs. The AMI Single-chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 6 shows a schematic for a typical digital telephone design.

Since asynchronous time slot operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 256kHz system clock and 64kHz shift clock from the 8kHz synchronizing signal received from the switch. The synchronizing signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output feeds directly into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

Figure 6. Voice Processing in a Digital Telephone Application



DTMF BANDSPLIT FILTER

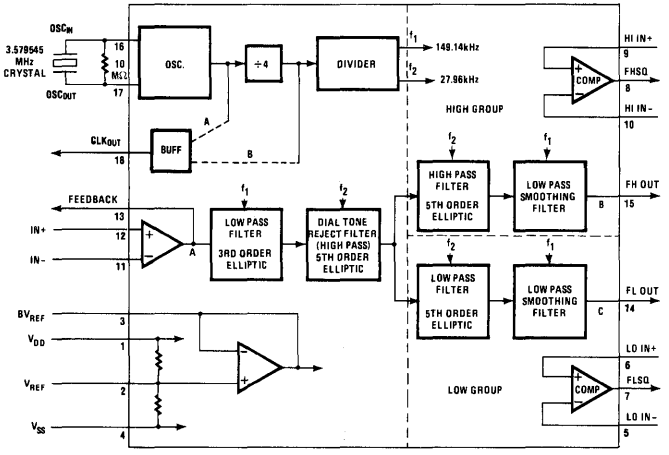
Features

- ☐ **CMOS Technology for Wide Operating Single Supply Voltage Range (7.0V to 13.5V). Dual Supplies (±3.5V to ±6.75V) Can Also Be Used.**
- ☐ **Uses Standard 3.58MHz Crystal as Time Base. Provides Buffered Clock to External Decoder Circuit.**
- ☐ **Ground Reference Internally Derived and Brought Out.**
- ☐ **Uncommitted Differential Input Amplifier Stage for Gain Adjustment**
- ☐ **Filter and Limiter Outputs Separately Available Providing Analog or Digital Outputs of Adjustable Sensitivity.**
- ☐ **Can be Used with Variety of Available Decoders to Build 2-Chip DTMF Receivers.**

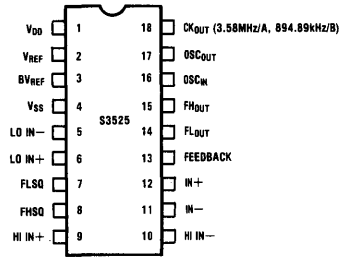
General Description

The S3525 DTMF Bandsplit Filter is an 18-pin monolithic CMOS integrated circuit designed to implement a high quality DTMF tone receiver system when used with a suitable decoder circuit. The device includes a dial tone filter, high group and low group separation filters and limiters for squaring of the filtered signals. An uncommitted input amplifier allows a programmable gain stage or anti-aliasing filter. An overall signal gain of 6dB is provided for the low group and high group signals in the circuit. The dial tone filter is designed to provide a rejection of at least 52dB in the frequency band of 300Hz to 500Hz. The difference between the S3525A and the S3525B is the frequency of output clock signal at the CKOUT pin. In the S3525B, it is a 894.89kHz square wave while in the S3525A, it is a 3.58MHz buffered oscillator signal. The S3525A can be used with digital DTMF decoder chips that need the TV crystal time base allowing use of only one crystal between the filter and decoder chips.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD} - V_{SS}) ..... +15.0V
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −55°C to +125°C
Analog Input ..... V_{SS} −0.3V ≤V_{IN}≤V_{DD} +0.3V

DC Electrical Operating Characteristics: T_A=0°C to +70°C

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref to V_{SS})		9.6	12.0	13.5	V
$V_{OL(CKOUT)}$	Logic Output "Low" Voltage I_{OL}=160μA			V_{SS}+0.4		V
$V_{OH(CKOUT)}$	Logic Output"High" Voltage I_{OH}=4μA			V_{DD}−1.0		V
$V_{OL(FH, FL)}$	Comparator Output Voltage Low	500pF Load			V_{SS}+0.5	V
		10kΩ Load			V_{SS}+2.0	V
$V_{OH(FH, FL)}$	Comparator Output Voltage High	500pF Load	V_{DD}−0.5			V
		10kΩ Load	V_{DD}−2.0			V
$R_{INA (IN-,IN+)}$	Analog Input Resistance		8			MΩ
$C_{INA (INA-, IN+)}$	Analog Input Capacitance				15	pF
V_{REF}	Reference Voltage Out		0.49 (V_{DD}−V_{SS})	0.50 (V_{DD}−V_{SS})	0.51 (V_{DD}−V_{SS})	V
V_{OR}=[BV_{REF}-V_{REF}]	Offset Reference Voltage				50	mV
P_D	Power Dissipation	V_{DD}=10V		170		mW
		V_{DD}=12.5V		400		mW
		V_{DD}=13.5V and 0°C			650	mW

AC System Specifications:

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
A_F	Pass Band Gain		5.5	6	6.5	dB
	Dial Tone Rejection					
	Dial Tone Rejection is measured at the output of each filter with respect to the passband					
DTR_L	Low Group Rejection	350Hz	55	59		dB wrt 700Hz
		440Hz	50	53		dB wrt 700Hz
DTR_H	High Group Rejection	Either Tone	55	68		dB wrt 1200Hz

AC System Specifications (Continued)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Attenuation Between Groups				
	Attenuation of the nearest frequency of the opposite group is measured at the output of each filter with respect to the passband				
GA_L	Attenuation of 1209Hz	50	>60		dB wrt 700Hz
GA_H	Attenuation of 941Hz	40	42		dB wrt 1200Hz
	Total Harmonic Distortion				
THD	Total Harmonic Distortion (dB). Dual tone of 770Hz and 1336 Hz sinewave applied at the input of the filter at a level of 3dBm each. Distortion measured at the output of each filter over the band of 300 Hz to 10kHz (V_{DD}=12V)			−40	dB
	Idle Channel Noise				
ICN	Idle Channel Noise measured at the output of each filter with C-message weighting. Input of the filter terminated to BV_{REF}			1	mV_{rms}
	Group Delay (Absolute)				
GD_L	Low Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms
GD_H	High Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms

Pin/Function Descriptions

OSC_{IN}, OSC_{OUT} — These pins are for connection of a standard 3.579545MHz TV crystal and a 10MΩ ±10% resistor for the oscillator from which all clocking is derived. Necessary capacitances are on-chip, eliminating the need for external capacitors.

CKOUT (S3525A) — Oscillator output of 3.58MHz is buffered and brought out at this pin. This output drives the oscillator input of a decoder chip that uses the TV crystal as time base. (Only one crystal between the filter and decoder chips is required.)

CKOUT (S3525B) — This is a divide by 4 output from the oscillator and is provided to supply a clock to decoder chips that use 895kHz as time base.

IN−, IN+, Feedback — These three pins provide access to the differential input operational amplifier on chip. The feedback pin in conjunction with the IN− and IN+ pins allows a programmable gain stage and implementation of an anti-aliasing filter if required.

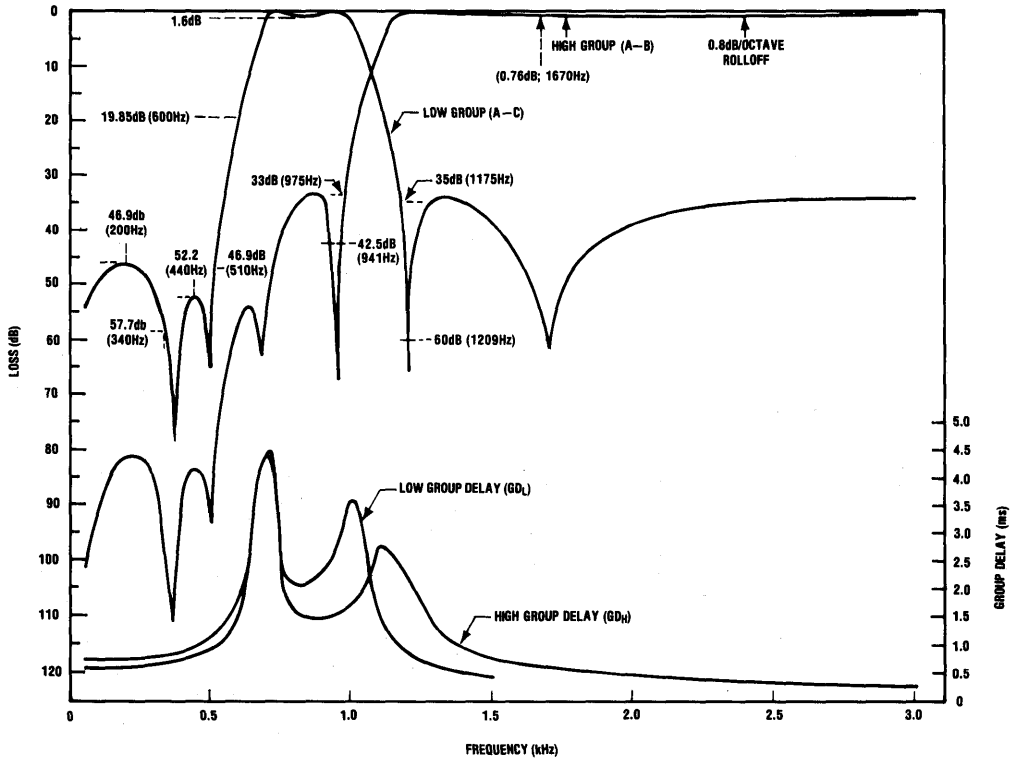
FH OUT, FL OUT — These are outputs from the high group and low group filters. These can be used as inputs to analog receiver circuits or to the on-chip limiters.

HI IN−, HI IN+
LO IN−, LO IN+ — These are inputs of the high group and low group limiters. These are used for squaring of the respective filter outputs. (See Figure 2.)

Pin/Function Descriptions (Continued)

FHSQ, FLSQ	These are respectively the high group and low group square wave outputs from the limiters. These are connected to the respective inputs of digital decoder circuits.
V_{DD}, V_{SS}	These are the power supply voltage pins. The device can operate over a range of $7V \leq (V_{DD} - V_{SS}) \leq 13.5V$.
V_{REF}	An internal ground reference is derived from the V_{DD} and V_{SS} supply pins and brought out to this pin. V_{REF} is $1/2(V_{DD} - V_{SS})$ above V_{SS}.
BV_{REF}	Buffered V_{REF} is brought out to this pin for use with the input and limiter stages.

Figure 1. Typical S3525 DTMF Bandsplit Filter Loss/Delay Characteristics



Input Configurations

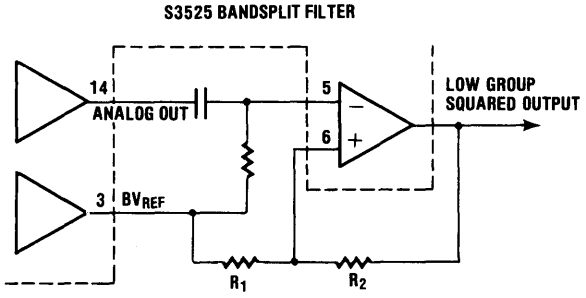
The applications circuits show some of the possible input configurations, including balanced differential and single ended inputs. Transformer coupling can be used if desired. The basic input circuit is a CMOS op amp which can be used for impedance matching, gain adjustment, and even filtering if desired. In the differential mode, the common mode rejection is used to reject power line-induced noise, but layout care must be taken to minimize capacitive feedback from pin 13 to pin 12 to maintain stability.

Since the filters have approximately 6dB gain, the inputs should be kept low to minimize clipping at the analog outputs (FL_{OUT} and FH_{OUT}).

Output Considerations

The S3525 has both analog and digital outputs available. Most integrated decoder circuits require digital inputs so the on-chip comparators are used with hysteresis to square the analog outputs. The sensitivity of the receiver system can be set by the ratio of R1 and R2, shown in Figure 2. The amount of hysteresis will set the basic sensitivity and eliminate noise response below that level.

Figure 2. Typical Squaring Circuit



ASSUMING $BV_{REF} = 0$ OR $\frac{1}{2}(V_{DD}-V_{SS})$ then

$$UTP = E_{O(SAT)} \frac{R_1}{R_1 + R_2}$$

$$LTP = -E_{O(SAT)} \frac{R_1}{R_1 + R_2}$$

Clock Considerations

The clock is provided by a standard 3.58MHz TV crystal in parallel with a 10MΩ resistor across pins 16 and 17. A buffered output at pin 18 is provided to drive the companion decoder at 3.58MHz (S3525A) or 895kHz (S3525B). It can be directly coupled or capacitively coupled depending on the decoder.

The circuits shown are not necessarily optimal but are intended to be good starting points from which an optimal design can be developed for each individual application.

Applications

Companion decoders to be used with the S3525 vary in performance and features. Teltone Corporation's TT6174, Rockwell Microelectronic's CRC8030 and MOSTEK's MK5102/03 are available units that can be used with the S3525.

Figure 3. AMI/Teltone 2 Chip DTMF Receiver

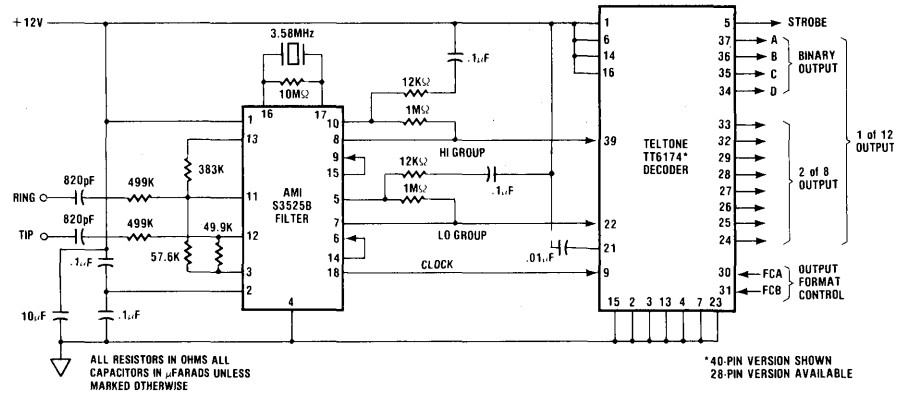


Figure 4. AMI/Mostek 2 Chip DTMF Receiver

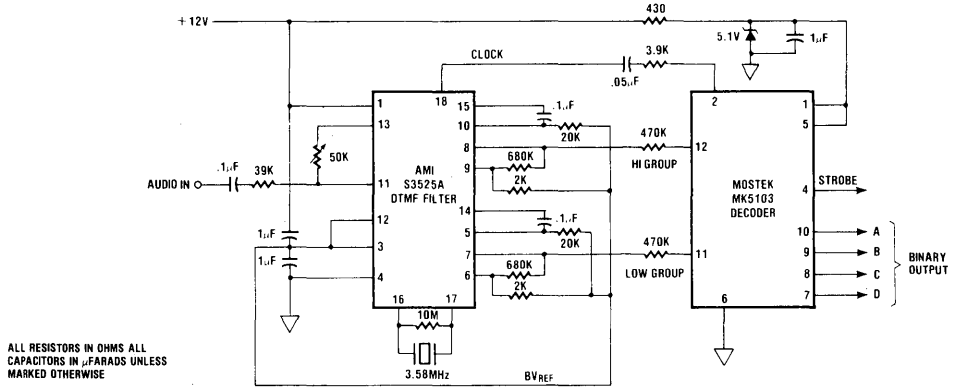
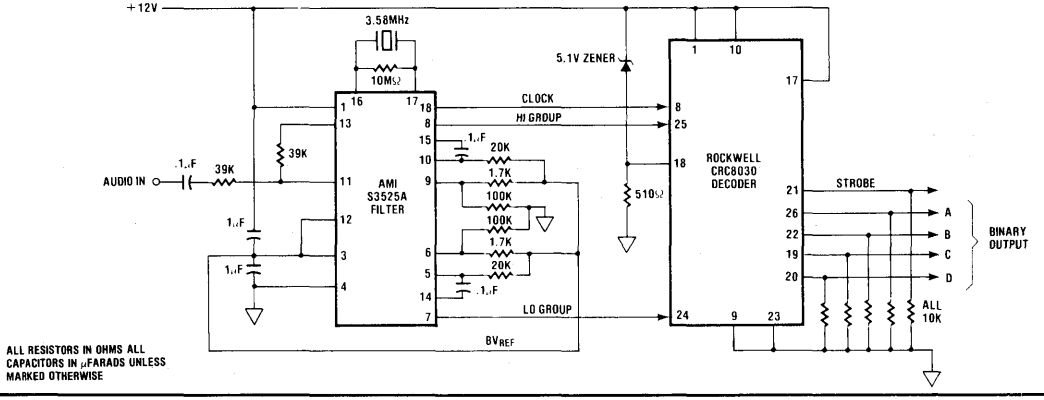


Figure 5. AMI/Rockwell 2 Chip DTMF Receiver



Additional information can be obtained from the S3525 Applications Note available on request from AMI, and from the suppliers of the decoder circuits.

TUNEABLE BANDPASS/NOTCH FILTER

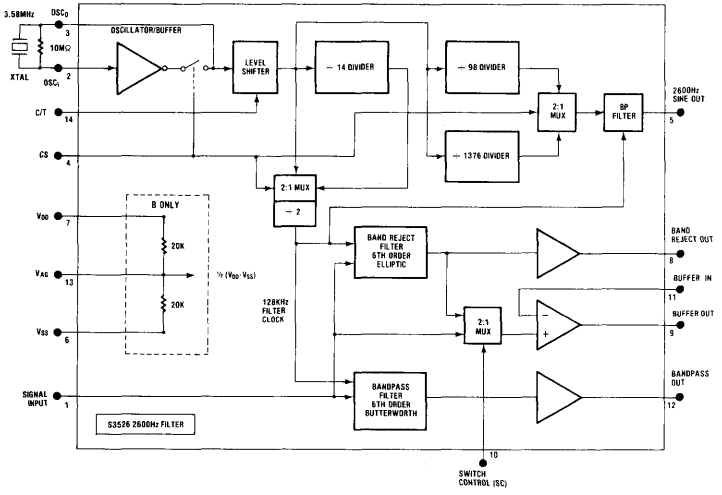
Features

- ☐ Provides Band Pass and Band Reject Outputs
- ☐ Uses 3.58MHz TV Crystal or 256KHz Clock as Timebase for 2600Hz Center Frequency
- ☐ Generates 2600Hz Sinewave
- ☐ Single or Dual Supply Operation
- ☐ Buffer Drives 600Ω Loads
- ☐ The bandpass/notch frequency can be shifted from 2600Hz by using other clock frequencies.

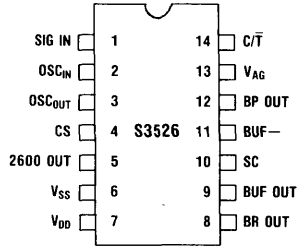
General Description

The S3526 Single Frequency (SF) Filter is a 14-pin monolithic CMOS circuit designed to implement a precision SF tone receiver. When used with an inexpensive 3.58 MHz TV crystal or a 256kHz clock input it provides sharp 2600 Hz bandpass and notch filters as well as a 2600Hz sine wave output. The 256kHz clock can be at CMOS or TTL levels. A change in the crystal (or clock) frequency from 3.58MHz (256kHz) will proportionately change the bandpass, notch and sine wave output frequencies. The S3526A is intended for dual +5V and −5V power supply operation, whereas the S3526B is intended for a single +10V supply.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V_{DD}-V_{SS})	+15.0V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Analog Input	V_{SS} −0.3V ≤ V_{IN} ≤ V_{DD} +0.3V

DC Electrical Operating Characteristics: T_A = 0°C to +70°C

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation V_{DD} = 10V		100		mW
V_{OT}	2600Hz Sine Wave Output Load = 10KΩ		±3.1		V (P-P)
V_{T_D}	2600Hz Output Distortion Load = 10KΩ (for 2600Hz center frequency)		−35		dB
R_{IN}	Input Resistances (Except SIG IN)	8			MΩ
C_{IN}	Input Capacitances			15.0	pF

Filter Performance Specifications

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain - All Paths	−0.5	0	0.5	dB
Z_{IN}	Input Impedance (SIG IN, Pin 1)		2.5		MOhms
	2600Hz Band Rejection Filter Attenuation (referenced from 1000Hz)				
	250Hz to 2200Hz	−0.5	0.1	0.5	dB
	2200Hz to 2400Hz	−0.5		5.0	dB
	2585Hz to 2615Hz	60	70		dB
	2800Hz to 3000Hz	−0.5		5.0	dB
	3000Hz to 3400Hz	−0.5	0.1	0.5	dB
	2600Hz Band Pass Filter Attenuation (referenced from 2600Hz)				
	DC to 1600Hz	70	80		dB
	2100Hz	50	63		dB
	2400Hz	30	37		dB
	2540Hz	3	5.8		dB
	2560Hz		.9	3	dB
	2640Hz		1.3	3	dB
	2660Hz	3	6.5		dB
	2800Hz	30	35		dB
	3100Hz	50	58		dB
	3600Hz	70	74		dB
	Ripple 2564Hz to 2632Hz			0.5	dB

Table 1: Control Pin Definitions

Pin No.	Name	Connection	Operation	Note
14	C/$\overline{T}$	V_{DD} to (V_{DD} − 0.5V)	CMOS Logic Levels	1
		(V_{DD} − 4V) to V_{SS}	TTL Logic Levels	
4	CS	V_{DD}	Ext. 256KHz Sq. Wave Clock at Pin 3	2
		V_{SS} or V_{AG}	3.58MHz Crystal Connected Between Pins 2 and 3 or 3.58 Clock to Pin 2	
10	SC	V_{DD}	Buffer Out = Input Signal	
		V_{SS}	Buffer Out = Band Reject Out	

Notes:

1) CMOS logic levels are same as V_{DD} and V_{SS} supply voltage levels. For TTL interface ground of TTL logic must be connected to V_{SS} supply pin.

2) For ext. 256KHz clock operation pin 2 must be connected to V_{DD}. For ext. 3.58 clock, drive pin 2, leave pin 3 open.

COMMUNICATIONS

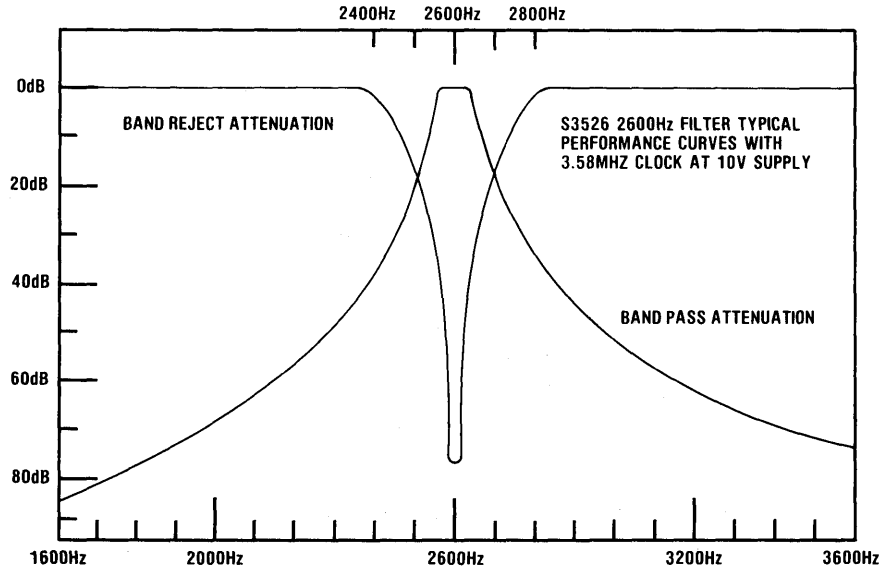
Pin Function Description

Pin	No.	Function
SIG IN	1	Signal In — This pin is the analog input to the filters and the buffer. It is a high impedance input (Z≈2.5MΩ).
OSC_{IN} OSC_{OUT}	2 3	These pins are the timing control for the entire chip. A 3.58MHz TV crystal is connected across these two pins in parallel with a 10MegOhm resistor. Another option is to provide a 256KHz signal at pin 3 and connect pin 2 to V_{DD}. It may be either TTL or CMOS levels, as determined by pin 14. Or, a CMOS level external 3.58MHz may be applied to pin 2 directly leaving pin 3 open.
CS	4	Clock Select - This pin when tied to V_{DD} configures the chip for 256KHz clock input operation. When tied to V_{AG} or V_{SS} the chip operates from a 3.58MHz crystal or clock input.
2600 OUT	5	This is an output pin providing a 2600Hz sine wave.
V_{SS}	6	Negative supply voltage pin.
V_{DD}	7	Positive supply voltage pin.
BR OUT	8	Band Reject Out - This is the output of the filter that notches out 2600Hz energy. It should drive a load $\geqslant$10KΩ.
BUF OUT	9	Buffer Out - This buffer can drive a 600Ω load and provides either the reproduced signal input without filtering, or provides the signal input with 2600Hz energy notched out.
SC	10	Switch Control - This pin controls which signal is presented at the Buffer Out. A logic high (V_{DD}) connects the input signal straight through. A logic low (V_{SS}) connects the output of the 2600Hz band reject filter to the Buffer Out.
BUF-	11	Buffer Negative - This is the inverting input to the buffer.
BP OUT	12	Band Pass Out - This is the output of the 2600Hz band pass filter which will pass any energy at 2600Hz present at the Signal In pin. It should drive a load $\geqslant$10KΩ.
V_{AG}	13	Analog Ground - This is the analog ground pin for audio inputs and outputs. When used with a single supply, this pin is 1/2 (V_{DD}-V_{SS}). When used with +5V supplies, this point is at ground. The S3526B has internal voltage divider resistors to V_{DD} and V_{SS} of ≅20KΩ. The S3525A does not.
C/$\overline{T}$	14	This pin determines whether CMOS or TTL levels will be accepted at pin 3 for a clock input. When tied to V_{DD}, the chip accepts CMOS logic levels; when tied to a point $\leqslant$(V_{DD}-4V), the chip accepts TTL levels.

Table 2: Analog Signal Parameters

Parameter	Min.	Typ.	Max.	Units
Input Signal Level			(V_{DD}-V_{SS})	Volts
Load Resistance (R_L) (BR OUT, BP OUT)		10		kΩ
Load Resistance (R_L) (BUFF OUT)		600		Ohms
Output Signal Level into R_L (Typ) BR OUT, BP OUT, BUFF OUT			+9	dBm

Figure 1. Typical Filter Performance Curves



AMERICAN MICROSYSTEMS, INC.

S3610

LPC-10 SPEECH SYNTHESIZER WITH ON-CHIP 20K SPEECH DATA ROM

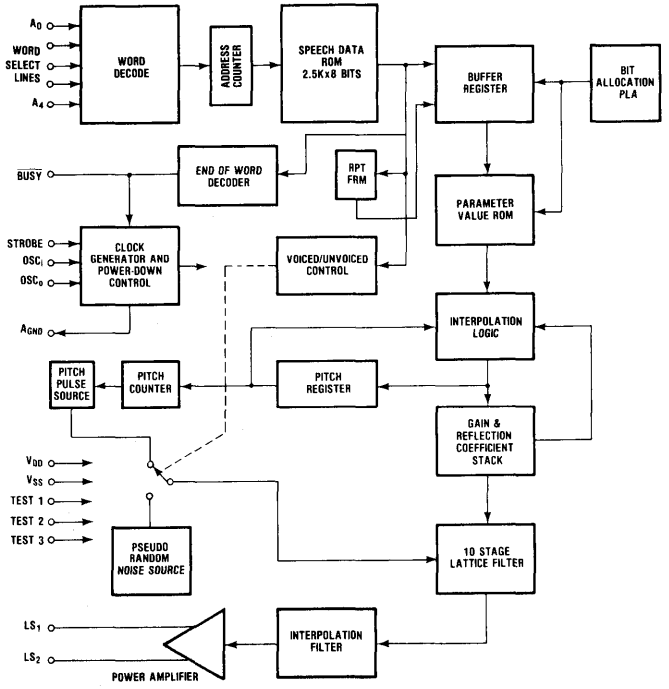
Features

- ☐ Simple Digital Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ 20K Bits Speech ROM
- ☐ Low Data Rate
- ☐ Up to 32 Word Vocabulary

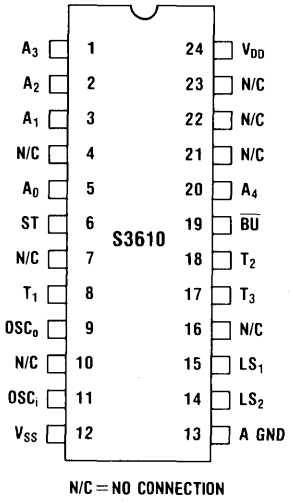
General Description

The S3610 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an internal 20K bit ROM. The simple digital interface consists of 5 word-select lines, a strobe input to load the address data and initiate operation, and a busy output signal. At the end of enunciation the chip automatically goes into the power-down mode until a new word select address is strobed in. The data rate from the speech ROM into the synthesizer is 2.0K bits/sec max. Typically the average data rate will be reduced to about 1.2K bits/sec. by means of the data rate reduction techniques used internally, giving about 17 seconds of speech from the ROM data. The 5 word-select lines allow a maximum vocabulary of 32 words.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

The synthesizer is realized using analog switched-capacitor filter technology and operates at 8K samples/sec. An output interpolating filter and bridge power amplifier give 30mW output power at 6 volts supply and allow the device to be connected directly to a 100Ω loudspeaker.

The S3610 also features an on-chip oscillator, requiring only a 640kHz ceramic resonator and a 120pF capacitor for normal operation.

AMI is able to provide a speech analysis service to generate the LPC parameters from customers' speech supplied on audio magnetic tape.

Absolute Maximum Ratings*

Supply Voltage	11 Volts DC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Voltage at any Pin	V_{SS} −0.3 to V_{SS} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications: (V_{DD}=6.0V ±10%, V_{SS}=0V, C_{AG}=0.047μF, T_A=0° to 70°C, unless otherwise specified)

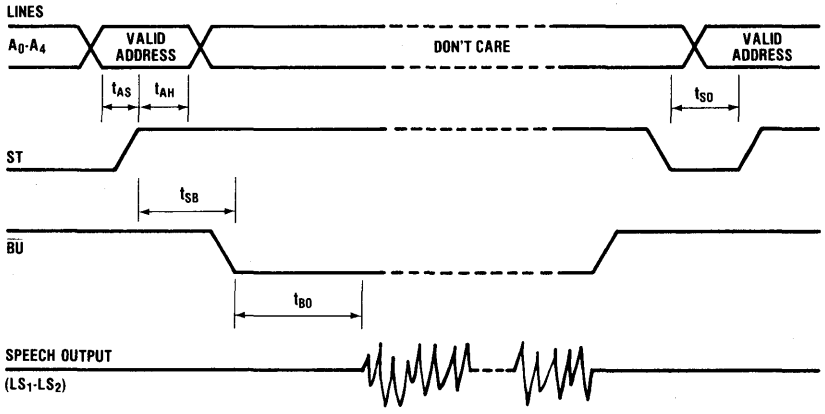
D.C. Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.4		V_{DD}	V	
V_{IL}	Input Low Logic "0" Voltage	−0.3		0.8	V	
I_{IN}	Input Leakage Current			10	μA	V_{IN}=0 to V_{DD}
V_{OL}	Output Low Voltage Busy Output			0.4	V	I_{OL}=1.6mA
ΔV_{OA}	Output DC Offset Voltage, Audio			200	mV	
V_{OA}	DC Output Voltage, Audio		½V_{DD}			R_{LOAD}=100Ω
I_{DD}	Supply Current, Operating		25		mA	
I_{DDL}	Supply Current, Powerdown		0.75		mA	

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
P_O	Audio Output Power		30		mW	R_{LOAD}=100Ω
t_{AS}	Address Set-up Time	200			nsec	See Figure 1
t_{AH}	Address Hold Time	10			nsec	See Figure 1
t_{SO}	Strobe Off Width	1			μsec	See Figure 1
t_{SB}	Strobe to Busy Delay		100	500	nsec	See Figure 1
t_{BO}	Busy to Speech Output Delay		19		msec	See Figure 1
F_{OSC}	Oscillator Resonator Frequency	−1%	640	+1%	KHz	
R_{LOAD}	Audio Output Load Impedance		100		Ω	
C_{INOSC}	Input Capacitance, Oscillator		100		pF	
C_{IN}	Input Capacitance, Digital Interface		7		pF	

Figure 1. Timing Requirements



Pin Function/Description

Digital Interface

A_0 through A_4 — **Word Select Inputs.** The 5-bit address data on these lines selects the word to be enunciated from the internal vocabulary.

ST — **Strobe Input.** A rising edge on this line strobes in the word select data and causes enunciation to commence. If this line is taken low prior to the end of enunciation (as indicated by the busy signal), enunciation stops immediately and the chip goes into power down mode.

$\overline{BU}$ — **Busy Output.** This open drain output signals that enunciation is in progress by going low.

Audio Interface

LS1 and 2 — **Loudspeaker Outputs.** These pins are used to connect the chip to the loudspeaker. They are D.C. coupled and have an offset of half the supply voltage. The audio output is balanced on the two outputs.

Misc.

OSC_i, OSC_o — **Oscillator Input and Output.** A 640KHz ceramic resonator (MuRata CSB640A or equivalent) should be connected between these pins for normal operation, or an external 640KHz signal may be fed into OSC_i. When a resonator is used, a 120pF capacitor should be connected between OSC_i input and ground.

T_1, T_2, T_3 — **Test Inputs.** These inputs should be left unconnected for normal operation.

V_{SS} — Most negative supply input. Normally connected to 0V.

V_{DD} — Most positive supply input.

A_{GND} — **Analog Ground.** An internally generated level approximately half way between V_{SS} and V_{DD}. A 0.047μF decoupling capacitor should be connected from this pin to V_{SS}. Do not connect this pin to a voltage supply.

Circuit Description

The main components of the S3610 LPC-10 Speech Synthesizer are shown in the block diagram.

Word Decode ROM—This ROM decodes the data presented on the word select lines into the start addresses of the speech words as stored in the Speech Data ROM. Up to 32 twelve bit start addresses may be programmed into this ROM. When the strobe line is taken high the start address selected is used to preset the Address Counter.

Address Counter—This binary counter is used to address the Speech Data ROM. After being preset to the desired start address it is incremented each time a new byte of data is required for the synthesizer.

Speech Data ROM—This ROM contains the 2.5K (2560) bytes of LPC-10 parameters encoded into a non-linearly quantized packed format. This format allows each frame of LPC parameters to be stored in only 5 bytes or less and is shown in Figure 2.

End of Word Decoder—This circuit detects the special code indicating that the last byte read from the Speech Data ROM denotes the end of the speech word data and initiates the power down routine after the previous frame has been enunciated.

Buffer Registers—The data from the Speech Data ROM is assembled into frames and then decimated into the 12 parameters required for LPC-10 synthesis: pitch, gain and the 10 lattice filter coefficients. The parameters are stored in an encoded format and the decoding is done in the Parameter Value ROM. The coefficient address registers are used to store the assembled frame data and address this ROM.

Bit Allocation PLA—A programmable logic array is used to control the allocation of bits in the Buffer Register to the 12 parameters. The allocation and permissible variations are shown in Figure 2.

Parameter Value ROM—This ROM is used as a look-up table to decode the stored parameters into the LPC coefficients.

Interpolation Logic—The coefficients for each frame of speech, normally 20msec. are interpolated four times per frame to generate smoother and more natural sounding speech. Hence, the interpolation period is one quarter of a frame period, normally 5msec. After interpolation, the coefficients are used to drive the pitch-pulse source, the lattice filter and the gain control. Interpolation is inhibited when a change from voiced to unvoiced speech, or vice versa, is made.

Pitch Register and Counter—This register stores the pitch parameter used to control the pitch counter.

Pitch-pulse Source—This is the signal source for voiced speech (vowel sounds). It is realized in switched-capacitor technology and generates symmetrical bipolar pulses at the rate specified by the pitch parameter and controlled by the pitch counter.

Pseudo-random Noise Source—This is the signal source for unvoiced speech (fricatives and sibilants) and consists of a 15-bit linear code generator giving a periodicity of 32767 sampling periods (4.096sec.). The output of this generator is scaled to a lower value and used as a random sign, constant amplitude signal.

Voiced/Unvoiced Speech Selector Switch—This switch determines whether the voiced or unvoiced signal source is used to drive the filter during a given frame.

LPC-10 Parameter Stack—This stack of 10 filter coefficients is used to control the lattice filter. The coefficients have an accuracy of 8-bits plus sign.

10 Stage Lattice Filter—The filter which simulates the effect of the vocal tract on the sound source (glottis) in the human speaker is realized here as a switched-capacitor (analog sampled data) 10 stage lattice filter. The filter parameters are determined dynamically by the time varying coefficients in the Parameter Stack and the filter operates at a sampling frequency of 8KHz (clock frequency/80).

Gain Controller—This controls the input signal level to the lattice filter to vary the sound level, and is an integral part of the lattice filter.

Interpolation Filter—The output signal from the lattice filter is sampled at 8KHz, and consequently its spectrum is rich in aliasing (foldover) distortion components above 4KHz (See Figure 3). The signal is cleaned up by passing it through a 4KHz low pass filter sampled at 160KHz. The spectrum of the output signal contains no aliasing distortion components below 156KHz, making the output suitable for feeding directly into a loudspeaker after amplification. This filter is also realized using switched-capacitor filter technology.

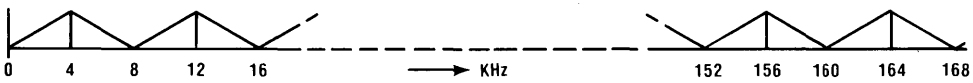
Power Amplifier—The amplifier brings up the level of the signal to give an output level of 30mW RMS into 100Ω load. The output is a balanced bridge configuration with anti-phase signals on the 2 output pins.

Figure 2. Packed Quantized Data Formats

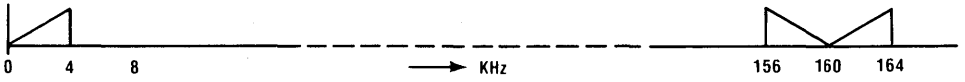
	BYTE 5								BYTE 4								BYTE 3								BYTE 2								BYTE 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VOICED	← PITCH →								← K10,K9,K8,K7,K6,K5 →								← K4,K3, K2, K1 →																V/UV	REPT	← GAIN →					
UNVOICED	← NOT USED →																← K4,K3, K2, K1 →																V/UV	REPT	← GAIN →					
REPEAT	← NOT USED →																																← PITCH →			GAIN				REPT*
END OF WORD	← NOT USED →																																0	0	0	0	0	0	0	0

*NOTE: 0 = SINGLE (OR LAST) REPEAT. 1 = MULTIPLE REPEAT

Figure 3.



(a) SPECTRUM OF SIGNAL OUTPUT OF LATTICE FILTER



(b) SPECTRUM OF SIGNAL AT OUTPUT OF INTERPOLATION FILTER.
NOTE: IN BOTH CASES A SIN x/x CHARACTERISTIC MODULATES THE SPECTRA. THIS IS OMITTED FOR SIMPLICITY.

Clock Generators and Power-down Control—This block contains the oscillator and timing circuits and also generates the analog ground reference voltage.

Speech Data Compression

The data rate of the synthesizer input is 5400 bits/sec before interpolation (21600 bits/sec after interpolation) consisting of 12 parameters of 9 bits each repeated every 20msec. This is reduced to less than 2000 bits/sec for storage by means of a non-linear quantization technique. Each of the 12 coefficients is constrained to have a fixed set of values in an optimized manner. The actual values are dependent on the speech data and generated automatically in the analysis process. The parameters used to

specify the coefficients are stored in the speech data ROM and used to address the coefficient look-up table ROM. The packing formats for the speech data are shown in Figure 2.

The speech data rate is further reduced by two other techniques shown in Figure 2. A substantial reduction is achieved by reducing the order of the lattice filter (the LPC order) to 4 during periods of unvoiced speech. This allows a 40% data reduction during these periods, which themselves typically account for 30-40% of speech (in the English language). A second reduction is obtained by detecting periods during which the filter parameters may be the same as those in the previous frame. Only the gain and pitch parameters are updated in such a frame, allowing an 80% data reduction. Note that in repeat frame only 3 bits are allocated to the gain parameter. The LSB is forced internally to zero.

Programming the S3610

The word decode ROM, the speech data ROM and the coefficient ROM are mask programmed with the customer's speech data. Interfacing with AMI to produce the ROM mask is possible at several levels, to suit the customer's requirements. AMI is able to provide a complete speech analysis service for this purpose. This allows accurate programming of the ROMs from a speech sample provided on audio magnetic tape with a fast turnaround. Customers who have LPC speech analysis facilities and wish to interface with AMI at a different level should contact the factory for further details about the quantization technique and formats acceptable.

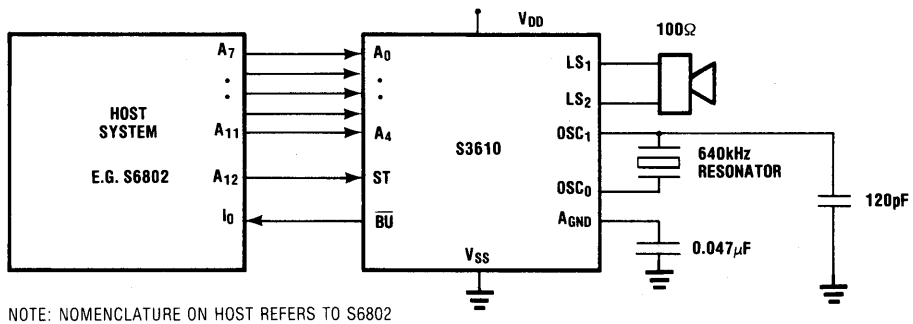
Interfacing

The S3610 is designed to be easily interfaced to a host controller. The interface timing requirements are shown in Figure 1. A valid 5-bit address should be presented on the word select lines and the strobe line taken to a logic 1 and held there until the end of enunciation, as indicated by the Busy output. A typical system configuration is shown in Figure 4. If it is not possible or inconvenient to monitor the Busy output or to maintain the strobe for the duration of the enunciation, these 2 lines may be combined as shown in Figure 5. The Busy output will automatically maintain the Strobe input once it is initiated. Note that an inverted strobe input is now required, and its duration should ensure that the Busy output goes low before it is removed. A minimum duration of 1μsec is recommended. A method of operating the synthesizer directly from a keyboard is shown in Figure 6. Using the 74C922 encoder limits the vocabulary to 16 words. This can be expanded to the maximum of 32 words by using 2 encoders. The R-C delay provides the address set-up time required before ST goes high.

Applications

Toys and Games
EDP
Instrumentation
Communications
Industrial Controls
Automotive
Appliances

Figure 4. Typical System Configuration



NOTE: NOMENCLATURE ON HOST REFERS TO S6802

Figure 5. Using Busy Output to Maintain Strobe

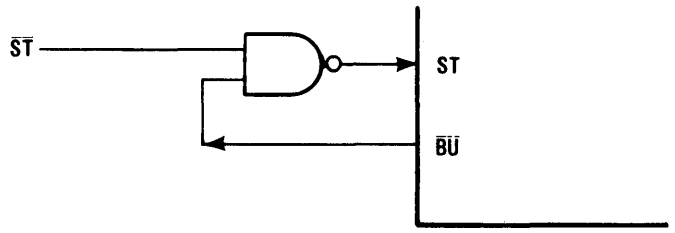
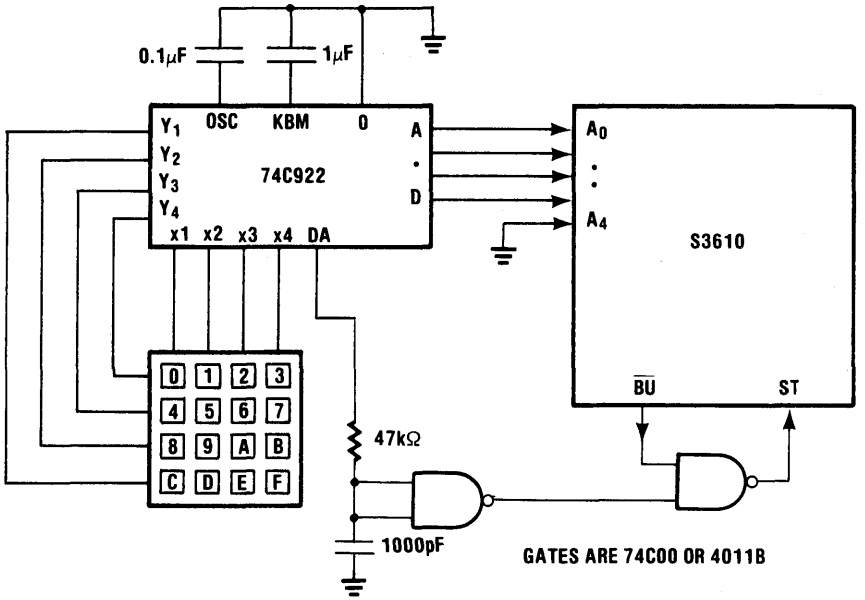


Figure 6. Direct Keyboard Operation



LPC-10 SPEECH SYNTHESIZER

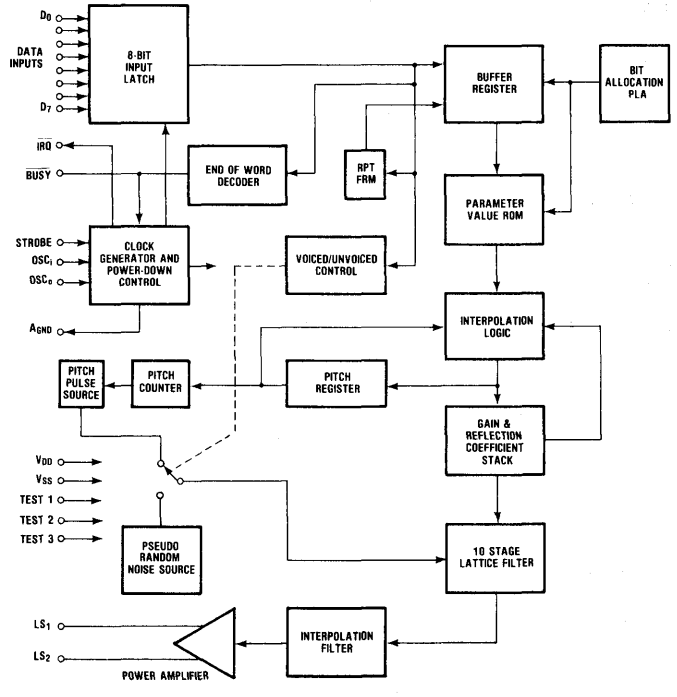
Features

- ☐ Simple Microprocessor Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ Low Data Rate

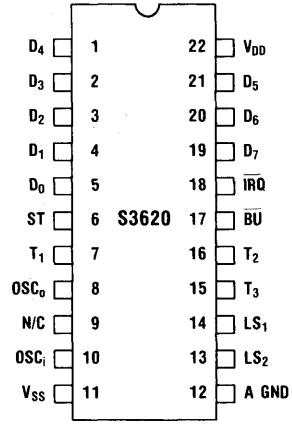
General Description

The S3620 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an external memory. The digital interface circuitry is fully microprocessor compatible and allows the processor to load the data with or without a DMA controller. The loading takes place on a handshake basis, and in the absence of a response from the processor the synthesizer automatically shuts down and goes into the powerdown mode. A busy signal allows the processor to sense the status of the synthesizer. The input data rate is 2.0K bits/sec. max., but typically the average data rate will be reduced to about 1.4K bits/sec. by means of the data rate reduction techniques used internally.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

The synthesizer is realized using analog switched-capacitor filter technology and operates at 8K samples/sec. An output interpolating filter and bridge power amplifier give 30mW output power at 6 volts supply and allow the device to be connected directly to a 100Ω loudspeaker.

The S3620 also features an on-chip oscillator, requiring only a 640kHz ceramic resonator and a 120pF capacitor for normal operation.

AMI is able to provide a speech analysis service to generate the LPC parameters from customers' speech supplied on audio magnetic tape.

Absolute Maximum Ratings*

Supply Voltage	11 Volts DC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Voltage at any Pin	V_{SS} −0.3 to V_{SS} +0.3V
Lead Temperature (Soldering, 10 sec.)	200°C
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications: (V_{DD}=6.0V ±10%, V_{SS}=0V, C_{AG}=0.047μF, T_A=0° to 70°C, unless otherwise specified)

D.C. Characteristics

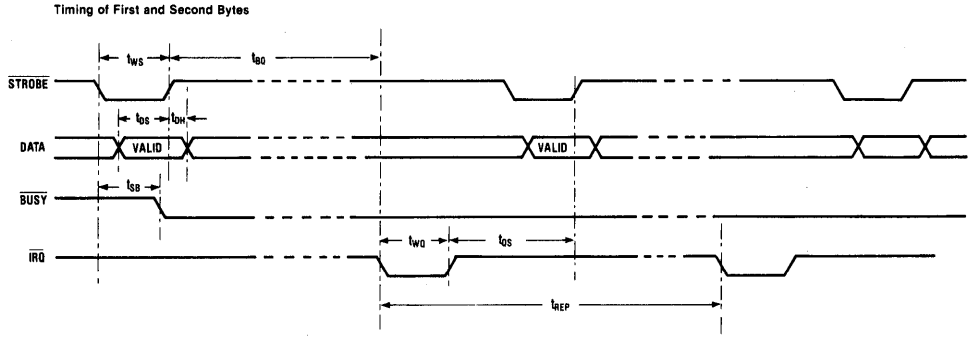
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.4		V_{DD}	V	
V_{IL}	Input Low Logic "0" Voltage	−0.3		0.8	V	
I_{IN}	Input Leakage Current			10	μA	V_{IN}=0 to V_{DD}
V_{OL}	Output Low Voltage Busy Output			0.4	V	I_{OL}=1.6mA
ΔV_{OA}	Output DC Offset Voltage, Audio			200	mV	
V_{OA}	DC Output Voltage, Audio		½V_{DD}			R_{LOAD}=100Ω
I_{DD}	Supply Current, Operating		25		mA	
I_{DDL}	Supply Current, Powerdown		0.75		mA	

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
P_O	Audio Output Power		30		mW	R_{LOAD}=100Ω
t_{DS}	Data Set-Up Time	100			nsec	See Figure 1
t_{DH}	Data Hold Time	10			nsec	See Figure 1
t_{WS}	Strobe Pulse Width	0.5		100	μsec	See Figure 1
t_{SB}	1st Strobe to Busy Delay		100	500	nsec	See Figure 1
t_{BQ}	1st Strobe to 1st IRQ Delay		19		msec	See Figure 1
t_{REP}	IRQ Repetition Rate		250		μsec	See Figure 1
t_{WQ}	IRQ Pulse Width	3		3.5	μsec	See Figure 1
t_{QS}	IRQ to Strobe Delay[See Note 1]			200	μsec	See Figure 1
F_{OSC}	Oscillator Resonator Frequency	−1%	640	+1%	KHz	See Figure 1
R_{LOAD}	Audio Output Load Impedance		100		Ω	
C_{INOSC}	Input Capacitance, Oscillator		100		pF	
C_{IN}	Input Capacitance, Digital Interface		7		pF	

NOTE 1: Failure to respond to an IRQ with a new strobe within the specified period results in the chip going into the power down mode.

Figure 1. Timing Requirements



Pin Function/Description

Digital Interface

D_0 through D_7	**Data Inputs.** The speech data (in quantized form) is loaded on these lines in 8 bit bytes.
ST	**Strobe Input.** A rising edge on this input strobes in the data bytes. Enunciation will commence after the first frame of data has been loaded. If no strobe is received by the chip in response to an IRQ output then enunciation stops immediately and the chip goes into the power-down mode.
$\overline{BU}$	**Busy Output.** This open drain output signals that enunciation is in progress by going low.
$\overline{IRQ}$	**Interrupt Request Output.** This open drain output signals that the chip is ready to receive the next byte of data. Failure to respond within the prescribed time results in the chip going into the power-down mode.

Audio Interface

LS1 and 2	**Loudspeaker Outputs.** These pins are used to connect the chip to the loudspeaker. They are D.C. coupled and have an offset of half the supply voltage. The audio output is balanced on the two outputs.

Misc.

OSC_i, OSC_o	**Oscillator Input and Output.** A 640KHz ceramic resonator (MuRata CSB640A or equivalent) should be connected between these pins for normal operation, or an external 640KHz signal may be fed into OSC_i. When a resonator is used, a 120pF capacitor should be connected between OSC_i input and ground.
T_1, T_2, T_3	**Test Inputs.** These inputs should be left unconnected for normal operation.
V_{SS}	Most negative supply input. Normally connected to 0V.
V_{DD}	Most positive supply input.
A_{GND}	**Analog Ground.** An internally generated level approximately half way between V_{SS} and V_{DD}. A 0.047μF decoupling capacitor should be connected from this pin to V_{SS}. Do not connect this pin to a voltage supply.

Circuit Description

The main components of the S3620 LPC-10 Speech Synthesizer are shown in the block diagram.

Input Latch—This 8-bit latch stores the input data after the strobe pulse and loads it into the Coefficient Address Registers.

End of Word Decoder—This circuit detects the special code indicating that the last byte loaded in the Input Latch denotes the end of the speech word data and initiates the power down routine after the previous frame has been enunciated.

Buffer Registers—The data from the Speech Data ROM is assembled into frames and then decimated into the 12 parameters required for LPC-10 synthesis: pitch, gain and the 10 lattice filter coefficients. The parameters are stored in an encoded format and the decoding is done in the parameter value ROM. The coefficient address registers are used to store the assembled frame data and address this ROM.

Bit Allocation PLA—A programmable logic array is used to control the allocation of bits in the Buffer Register to the 12 parameters. The allocation and permissible variations are shown in Figure 2.

Parameter Value ROM—This ROM is used as a look-up table to decode the stored parameters into the LPC coefficients.

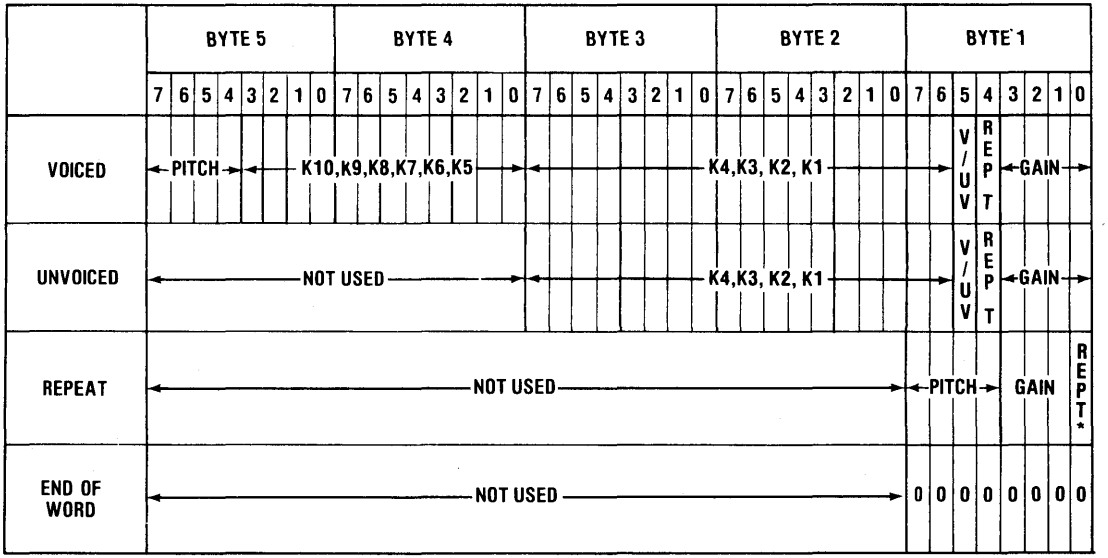
Interpolation Logic—The coefficients for each frame of speech, normally 20msec. are interpolated four times per frame to generate smoother and more natural sounding speech. Hence, the interpolation period is one quarter of a frame period, normally 5msec. After interpolation, the coefficients are used to drive the pitch-pulse source, the voiced/unvoiced switch, the lattice filter and the gain control. Interpolation is inhibited when a change from voiced to unvoiced speech, or vice versa, is made.

Pitch Register and Counter—This register stores the pitch parameter used to control the pitch counter.

Pitch-pulse Source—This is the signal source for voiced speech (vowel sounds). It is realized in switched-capacitor technology and generates symmetrical bipolar pulses at the rate specified by the pitch parameter and controlled by the pitch counter.

Pseudo-random Noise Source—This is the signal source for unvoiced speech (fricatives and sibilants) and consists of a 15-bit linear code generator giving a periodicity of 32767 sampling periods (4.096sec.). The output of this generator is scaled to a lower value and used as a random sign, constant amplitude signal.

Figure 2. Packed Quantized Data Formats



*NOTE: 0 = SINGLE (OR LAST) REPEAT. 1 = MULTIPLE REPEAT

Voiced/Unvoiced Speech Selector Switch—This switch determines whether the voiced or unvoiced signal source is used to drive the filter during a given frame.

LPC-10 Parameter Stack—This stack of 10 filter coefficients is used to control the lattice filter. The coefficients have an accuracy of 8-bits plus sign.

10 Stage Lattice Filter—The filter which simulates the effect of the vocal tract on the sound source (glottis) in the human speaker is realized here as a switched-capacitor (analog sampled data) 10 stage lattice filter. The filter parameters are determined dynamically by the time varying coefficients in the Parameter Stack and the filter operates at a sampling frequency of 8KHz (clock frequency/80).

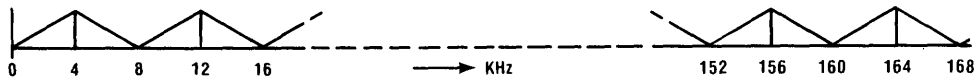
Gain Controller—This controls the input signal level to the lattice filter to vary the sound level, and is an integral part of the lattice filter.

Interpolation Filter—The output signal from the lattice filter is sampled at 8KHz, and consequently its spectrum is rich in aliasing (foldover) distortion components above 4KHz (See Figure 3). The signal is cleaned up by passing it through a 4KHz low pass filter sampled at 160KHz. The spectrum of the output signal contains no aliasing distortion components below 156KHz, making the output suitable for feeding directly into a loudspeaker after amplification. This filter is also realized using switched-capacitor filter technology.

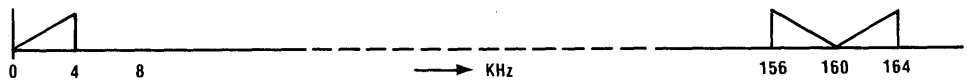
Power Amplifier—The amplifier brings up the level of the signal to give an output level of 30mW RMS into a 100Ω load. The output is a balanced bridge configuration with anti-phase signals on the 2 output pins.

Clock Generators and Power-down Control—This block contains the oscillator and timing circuits and also generates the analog ground reference voltage.

Figure 3.



(a) SPECTRUM OF SIGNAL OUTPUT OF LATTICE FILTER



(b) SPECTRUM OF SIGNAL AT OUTPUT OF INTERPOLATION FILTER.
NOTE: IN BOTH CASES A SIN x/x CHARACTERISTIC MODULATES THE SPECTRA. THIS IS OMITTED FOR SIMPLICITY.

Speech Data Compression

The data rate of the synthesizer input is 5400 bits/sec before interpolation (21600 bits/sec after interpolation) consisting of 12 parameters of 9 bits each repeated every 20msec. This is reduced to less than 2000 bits/sec for storage by means of a non-linear quantization technique. Each of the 12 coefficients is constrained to have a fixed set of values in an optimized manner. The actual values are dependent on the speech data and generated automatically in the analysis process. The parameters used to specify the coefficients are stored in the speech data ROM and used to address the coefficient look-up table ROM. The packing formats for the speech data are shown in Figure 2.

The speech data rate is further reduced by two other techniques shown in Figure 2. A substantial reduction is achieved by reducing the order of the lattice filter (the LPC order) to 4 during periods of unvoiced speech. This allows a 40% data reduction during these periods, which themselves typically account for 30-40% of speech (in the English language). A second reduction is obtained by detecting periods during which the filter parameters may be the same as those in the previous frame. Only the gain and pitch parameters are updated in such a frame, allowing an 80% data reduction.

Generation of Speech Data for the S3620

The speech data input to the S3620 is in a compressed format as explained in the previous section. AMI is able to provide a complete speech analysis service for this purpose and can supply the data on a diskette or programmed into EPROMs or mask programmed ROMs up to 128k bits. The speech sample should be provided to AMI on audio magnetic tape. Customers who have LPC speech analysis facilities and wish to generate their own data should contact AMI for further details of the quantization technique used and the availability of software to accomplish this.

Interfacing

The S3620 is designed to be easily interfaced to an 8-bit microprocessor system such as the S6800 as well as some 4-bit systems such as the S2000 family. The timing requirements are shown in Figure 1. A valid data byte should be present at the data input lines when the strobe line is taken to a logic 1 before the start of enunciation and in response to each $\overline{IRQ}$. The busy output may be used to identify the $\overline{IRQ}$ source during polling in a multiple interrupt system. A typical system configuration is shown in Figure 4. The S3620 occupies a single address in the microprocessor's memory space and data is loaded by writing it into that address after reading it from memory. The Address decode function may be realized using a PIA. An alternative interface technique is to write the data directly into the S3620 while reading it from the memory. This can be accomplished by mapping the S3620 into the entire address space of the speech data portion of the memory, so that the strobe is generated each time a byte of data is read from the speech memory. This can save hardware, as well as microprocessor instructions, since the loading of each byte is now accomplished in a single Read cycle instead of a Read cycle followed by a Write cycle. An example of this interfacing is shown in Figure 5, where the speech data occupies the memory addresses 0000 to 7FFF.

Applications

Toys and Games
EDP
Communications
Instrumentation
Industrial Controls
Automotive
Appliances

Figure 4.

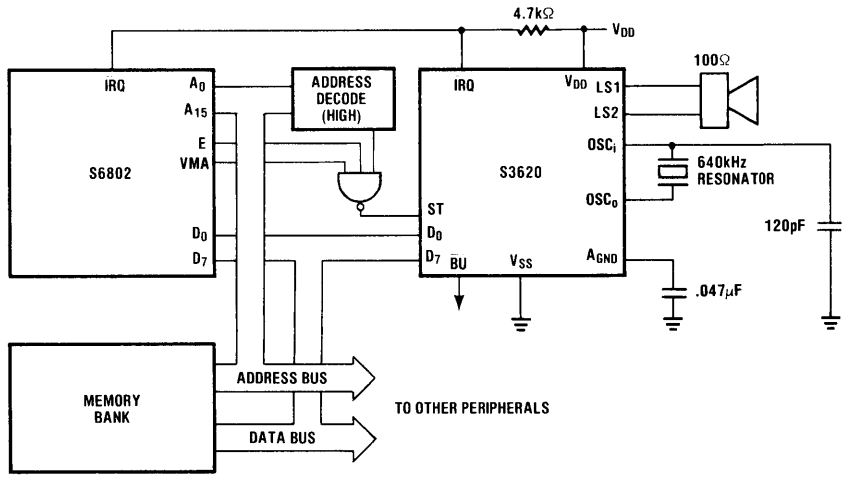
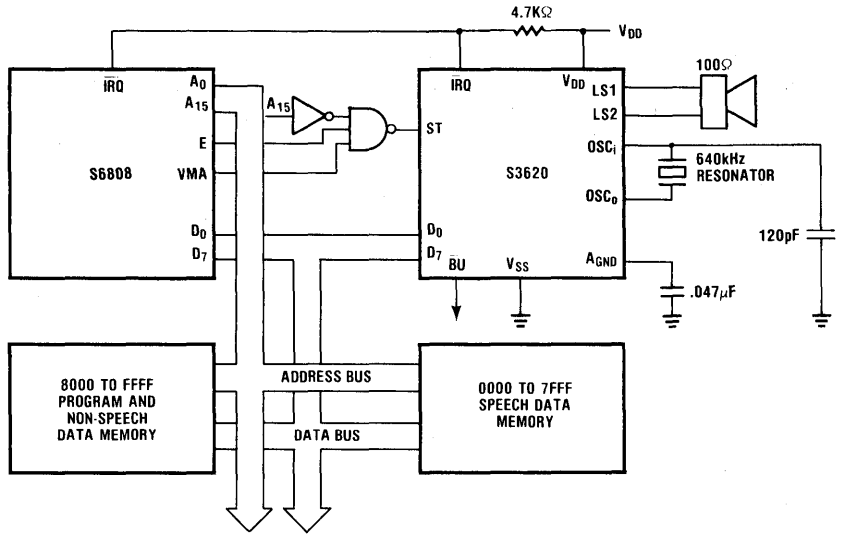


Figure 5.


4.7KΩ
VDD
100Ω
IRQ
A0
A15
E
S6808
VMA
D0
D7
A15
IRQ
VDD
LS1
LS2
ST
OSCi
S3620
640kHz
RESONATOR
OSCo
D0
D7
BU
VSS
AGND
120pF
.047μF
8000 TO FFFF
PROGRAM AND
NON-SPEECH
DATA MEMORY
ADDRESS BUS
DATA BUS
0000 TO 7FFF
SPEECH DATA
MEMORY

AMERICAN MICROSYSTEMS, INC.

S3630A/B

128K (16K×8) BIT NMOS ROM

COMMUNICATIONS

Features

- Single +5V Power Supply
- Directly TTL Compatible Inputs
- Directly TTL Compatible Outputs, Three State on S3630A
- Low Power: Supply Current-20mA Max.
- Power Down Capability (S3630A)

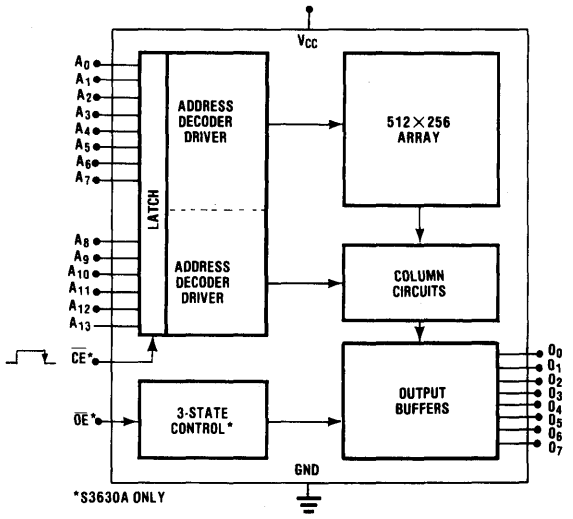
General Description

The S3630A/B is a high density 131072 bit NMOS mask programmable Read Only Memory. The device is fully TTL compatible and the organization as 16K×8 bits makes it very suitable for use in microprocessor systems. It is available in both 6μsec and 10μsec versions.

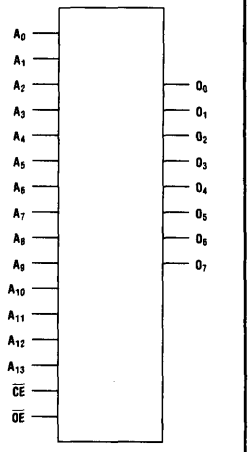
The S3630 is available in two pin configurations. The S3630A has the industry standard pinout (28-pin package). The S3630B has a minimum pin configuration, allowing it to be packaged in a 24-pin DIL pack, saving valuable board space where this configuration is usable, as well as reducing costs.

The S3630 is manufactured in a high density silicon gate, depletion load, N-channel process. Its high data capacity makes it extremely suitable for use in speech synthesis systems.

Block Diagram



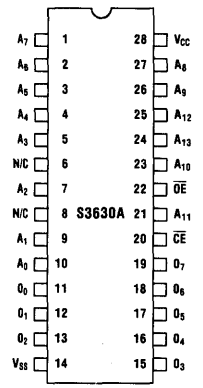
Logic Symbol



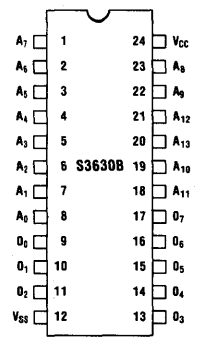
Pin Names

A_0-A_{13}	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

Pin Configuration



N.C. = NO CONNECTION



Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... −10°C to 80°C
Storage Temperature ..... −65°C to 150°C
Output or Supply Voltages ..... −0.5V to 7V
Input Voltages ..... −0.5V to 6.5V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: ($T_A = -10°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 1.6mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = 100\mu A$
V_{IL}	Input LOW Voltage	0		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		5.5	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to 5.5V
I_{LO}	Output Leakage Current			10	μA	$V_O = 0.4V$ to 5.5V, @V_{CC} 0.4V or OPEN
I_{CC}	Power Supply Current		10	20	mA	
I_{CC}	Standby			3	mA	3630A

Capacitance: ($T_A = 25°C$, f = 1MHz.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
C_{IN}	Input Capacitance			7	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: ($T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CEO}	Chip Enable Access Time S3630A S3630A-1			 6 10	 μsec μsec	See A.C. Conditions of Test and A.C. Test Load
t_{OE}	Output Enable Access Time S3630A and S3630A-1			350	nsec	
t_{OFF}	Output Deselect Time S3630A			350	nsec	
t_{AS}	Address Setup Time (S3630A)	0			nsec	
t_{AH}	Address Hold Time (S3630A)	1			μsec	
t_{CE}	$\overline{CE}$ Off Time (S3630A)	5			μsec	
t_{OV}	Access Time from V_{CC} On S3630B S3630B-1			 6 10	 μsec μsec	
t_{OFF}	Output Deselect Time S3630B			250	nsec	

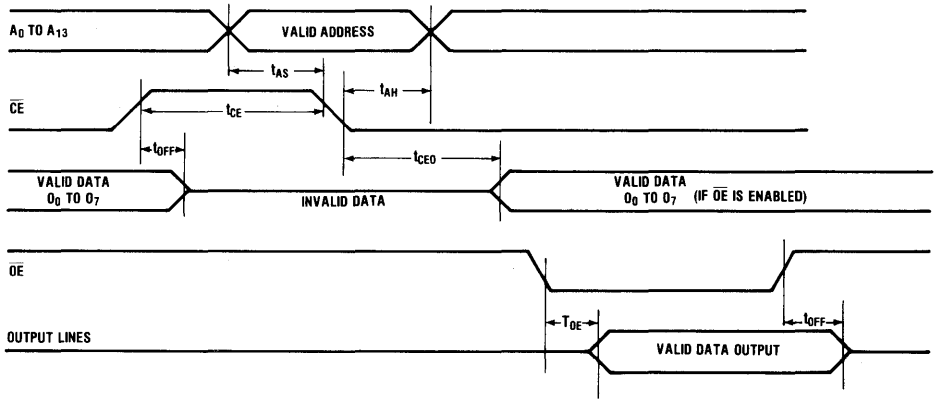
A.C. Characteristics: (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AS}	Address Set-Up Time S3630B			−200	nsec	
t_{AH}	Address Hold Time (S3630B)	2			μsec	
$V_{CC_{OFF}}$		100			nsec	

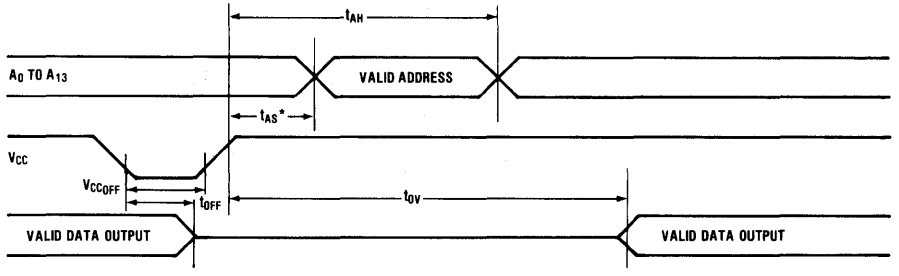
A.C. Test Conditions

Input Pulse Levels	0.8 to 2.0V
V_{CC} Levels	0 to 4.5V
Input/Output Timing Levels	1.5V
Output Load	1 TTL Load and 100pF

3630A Timing Diagram



3630B Timing Diagram



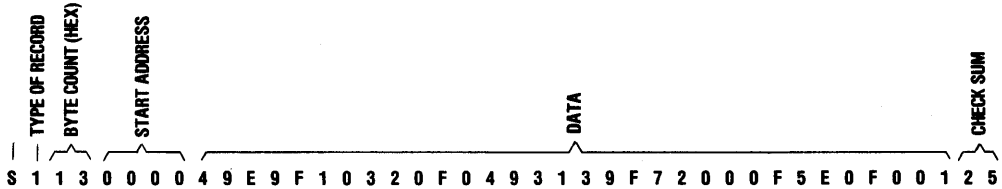
*t_{AS} MAY BE A NEGATIVE NUMBER SINCE THE ADDRESS DOES NOT HAVE TO BE VALID WHEN V_{CC} GOES ON BUT MAY OCCUR AFTERWARDS

Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI (see notes on page 4).

Position	Description
1	Start of record (Letter S)
2	Type of record 0—Header record (comments) 1—Data record 9—End of file record
3,4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5,6,7,8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9,...,N	Data Each data byte is represented by two hex characters. Most significant character first.
N+1,N+2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

EXAMPLE: S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C



NOTES:

Paper tape format is the same as the card format above except:

a. The record should be a maximum of 80 characters.
b. Carriage return and line feed after each record followed by another record.
c. There should NOT be any extra line feed between records at all.
d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMERICAN MICROSYSTEMS, INC.

Consumer Products

Contact factory for complete data sheet

REMOTE CONTROL CIRCUITS

Part No.	Description	Process	Power Supply	Commands	Packages
S2600	Remote Control Encoder	CMOS	+7V to 10V	31	16 Pin
S2601	Remote Control Decoder	PMOS	+10V to 18V	31	22 Pin
S2602	Remote Control Encoder	CMOS	+9V	18	16 Pin
S2603	Remote Control Decoder	PMOS	+9V	18	22 Pin
S2604	Remote Control Encoder	CMOS	+9V	18	16 Pin
S2605	Remote Control Decoder	CMOS	+9V	18	22 Pin
S2742	Remote Control Decoder	PMOS	+15V	512	18 Pin
S2743	Remote Control Encoder	PMOS	+9V	512	16 Pin
S2747	Remote Control Encoder	CMOS	+9V	512	16 Pin
S2748	Remote Control Decoder	CMOS	+12V	512	16 Pin

ORGAN CIRCUITS

Part No.	Description	Process	Packages
S10110	Analog Shift Register	PMOS	8 Pin
S10129	Six-Stage Frequency Divider	PMOS	14 Pin
S10130	Six-Stage Frequency Divider	PMOS	14 Pin
S10131	Six-Stage Frequency Divider	PMOS	14 Pin
S10430	Divider-Keyer	PMOS	40 Pin
S2567	Rhythm Counter	PMOS	16 Pin
S2688	Noise Generator	PMOS	8 Pin
S50240	Top Octave Synthesizer	PMOS	16 Pin
S50241	Top Octave Synthesizer	PMOS	16 Pin
S50242	Top Octave Synthesizer	PMOS	16 Pin
S50243	Top Octave Synthesizer	PMOS	16 Pin
S50244	Top Octave Synthesizer	PMOS	16 Pin
S50245	Top Octave Synthesizer	PMOS	16 Pin

CLOCK CIRCUITS

Part No.	Description	Process	Power Supply	Digits	Packages
S4003	Fluorescent Automotive Digital Clock (12 Hour+Date+Rally Timer)	PMOS	+12V	4	40 Pin

DRIVERS

Part No.	Description	Process	Power Supply	Outputs	Packages
S2809	Universal Driver	PMOS	+8V to +22V	32	40 Pin
S4535	32 Bit, High Voltage, Driver	CMOS	+5V	32	40 Pin
S4534	10 Bit, High Voltage, High Current Driver	CMOS	+5V	10	18 Pin
S4521	32 Bit Driver	CMOS	+5V	32	40 Pin

A/D CONVERTER AND DIGITAL SCALE CIRCUIT

Part No.	Description	Process	Power Supply	Digits	Packages
S4036	General Purpose A/D Converter and Digital Scale Circuit	CMOS	+9V	4	24 Pin

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2600/S2601

ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

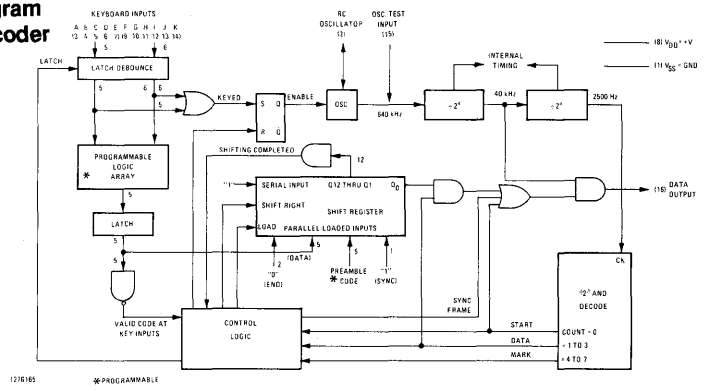
January 1982

CONSUMER

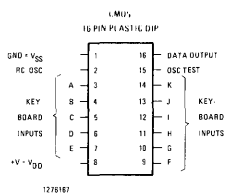
Features

- ☐ Small Parts Count — No Crystals Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hard-wire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 31 Commands — 5-bit Output Bus with Data Valid
- ☐ 3 Analog (LP Filterable PWM) Outputs
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Indexing Output — 2½ Hz Pulse Train
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

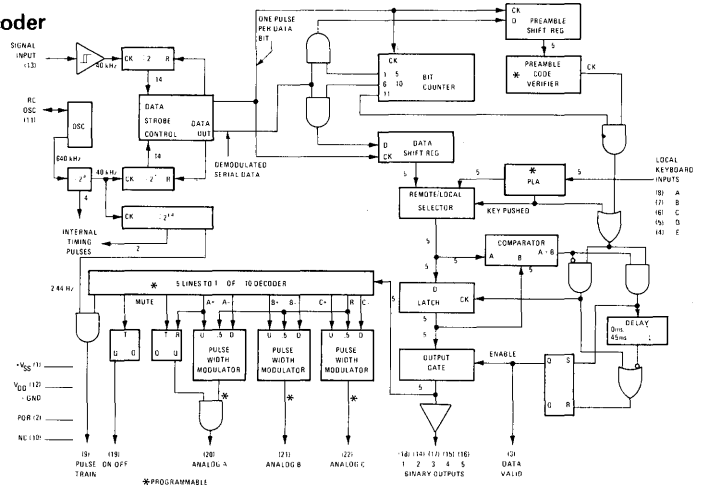
Block Diagram
S2600 Encoder



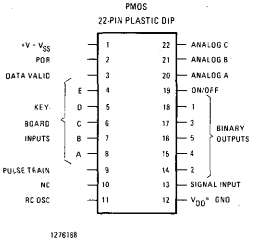
Pin Configuration
S2600



Block Diagram
S2601 Decoder



Pin Configuration
S2601



Functional Description

The S2600/S2601 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a synchronizing marker technique has eliminated the need for highly accurate frequencies generated by crystals. The S2600 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 thru 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 through 11 contain the command data. The S2601 Decoder produces an output only after two complete, consecutive, identical, 12-bit transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2600/S2601 system a very high immunity to noise, without a large number of discrete components.

S2600 Encoder

The S2600 is a CMOS device with an on-chip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator requires only an external resistor and capacitor, and to conserve power, *runs only during transmission.* Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group A through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2600/S2601 CODING," below. This code is loaded into a shift register in parallel with the sync, preamble, and end bits, to form the 12-bit message.

The transmitter output is a 40 kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in a 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The Test Input is used for functional testing of the device. A low level input will cause the oscillator frequency to be gated to the Data Output pin. This input has an internal pull-up resistor to V_{DD}.

S2601 Decoder

The S2601 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 11 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2601, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ±24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous pream-

ble codes or by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

The S2601 has five other outputs: Pulse Train, On/Off, Analog A, Analog B, and Analog C. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated. The Pulse Train output provides a 2.44Hz square wave (50% duty factor) whenever 11011 appears at the Binary Outputs, but otherwise it remains at a logic "0". This pulse train can be used for indexing, e.g., for stepping a TV channel selector.

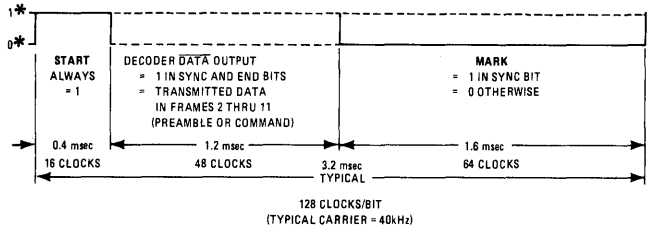
The On/Off ("mains") output changes state each time 01111 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

Analog Outputs A, B and C are 10kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code—6 codes in all. The entire range of 0% to 100% duty factor can be traversed in 6.5 seconds or at a rate of the oscillator frequency divided by 2^{12}. All three Analog Outputs are set to 50% duty factor whenever 01011 appears at the Binary Outputs. Analog A is mutable; 01100 sets it to 0% duty factor. If 01100 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2601 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Outputs to "0", sets the Analog Outputs at 50% duty factor, and insures that Analog A is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

CONSUMER

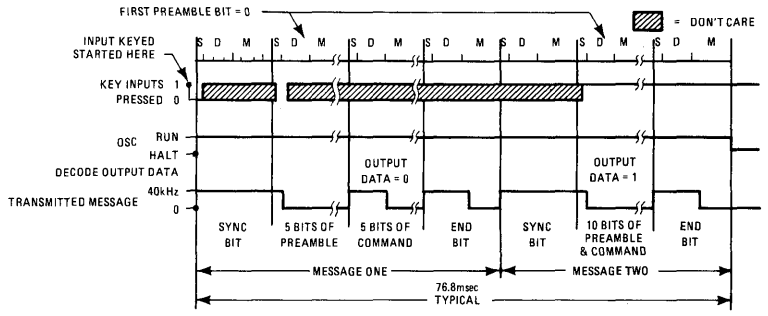
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

** IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

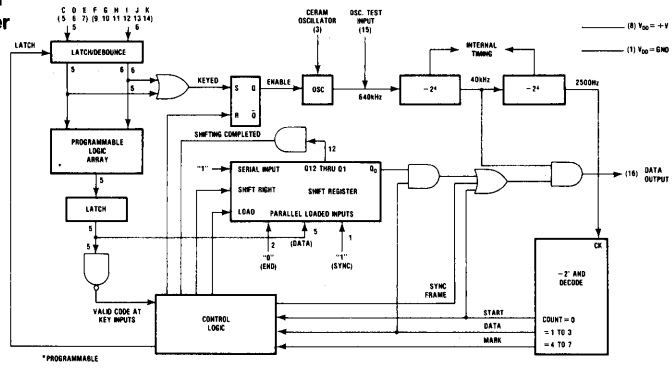
S2602/S2603

ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

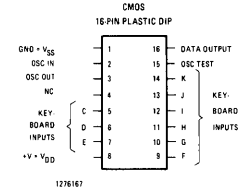
Features

- ☐ Accurate Data Transmission - No Frequency Trimming Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 18 Commands—5-bit Output Bus with Data Valid
- ☐ Analog (LP Filterable PWM) Output
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

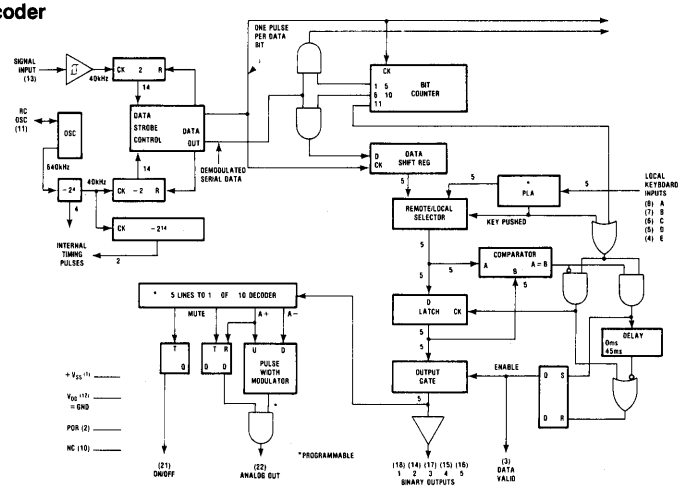
Block Diagram S2602 Encoder



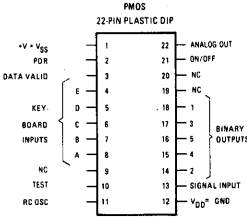
Pin Configuration S2602



Block Diagram S2603 Decoder



Pin Configuration S2603



Functional Description

The S2602/S2603 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a ceramic resonator with the S2602 Encoder eliminates the need to trim the S2603 decoder oscillator.

The S2602 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 through 6 are place-holder bits, and bits 7 through 11 contain the command data. The S2603 Decoder produces an output only after two complete, consecutive, identical transmissions. Marker pulses and redundant transmissions have given the S2602/S2603 system a very high immunity to noise, without a large number of discrete components.

S2602 Encoder

The S2602 is a CMOS device with an on-chip oscillator, 9 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator uses an external ceramic resonator, and to conserve power, *runs only during transmission.* Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group C through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2602/S2603 CODING," below. This code is loaded into a shift register in parallel with the sync and end bits to form the message.

The transmitter output is a 40kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark=1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The S2602 Encoder is silenced automatically by an on-chip duration limiter if a transmission persists for 6½ seconds (FOSC=320kHz). The absence of a keyboard closure will reset the duration limiter so that a new 6½ second internal starts with the next key closure.

S2603 Decoder

The S2603 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 8 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2603, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ±24% with respect to the receiver oscillator frequency.

The decoded place-holder bits from the next five-bit frames following the initial synchronizing frame are not used. However, the next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next transmission. In the case where 2 identical, proper transmissions are immediately followed by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

The S2603 has two other outputs: On/Off and Analog. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard

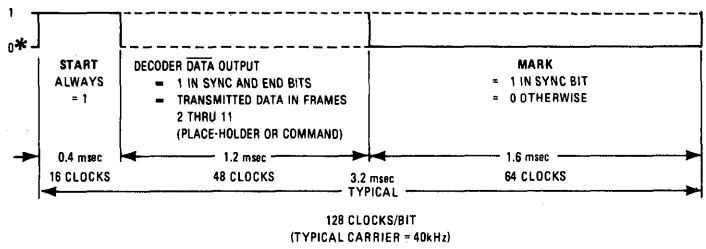
Inputs can cause to be generated.

The On/Off ("mains") output changes state each time 10011 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

The Analog Output is a 10kHz pulse train whose duty factor is digitally controllable. With a simple low-pass filter, this output can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. The Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code. The Analog Output is mutable; 11110 sets it to 0% duty factor. If 11110 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2603 has an on-chip power-on reset (POR) circuit which sets the On/Off Output to "0", sets the Analog Output at 50% duty factor, and insures that the Analog Output is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

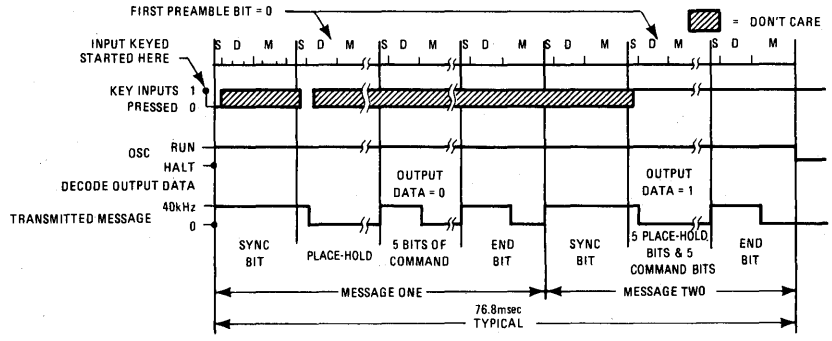
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2604/S2605

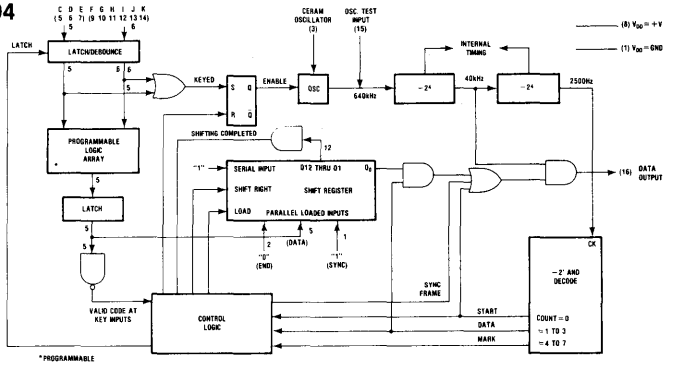
ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

CONSUMER

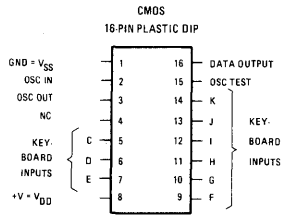
Features

- ☐ Accurate Data Transmission - No Frequency Trimming Required
- ☐ Easily Used in LED, Ultrasonic, RF, or Hardwire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 18 Commands—5-bit Output Bus with Data Valid
- ☐ Analog (LP Filterable PWM) Output
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

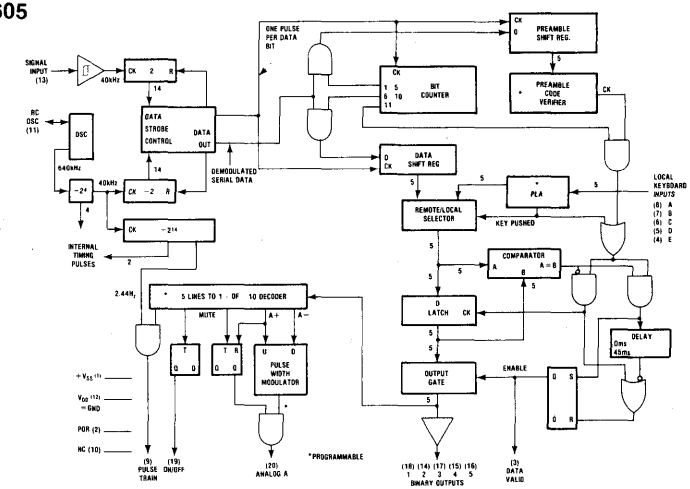
Block Diagram S2604



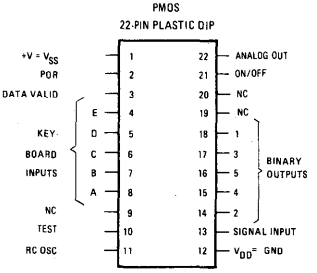
Pin Configuration S2604



Block Diagram S2605



Pin Configuration S2605



Functional Description

The S2604/S2605 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a ceramic resonator with the S2604 Encoder eliminates the need to trim the S2605 decoder oscillator.

The S2604 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 through 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 through 11 contain the command data. The S2605 Decoder produces an output only after two complete, consecutive, identical transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2604/S2605 system a very high immunity to noise, without a large number of discrete components.

S2604 Encoder

The S2604 is a CMOS device with an on-chip oscillator, 9 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator uses an external ceramic resonator, and to conserve power, *runs only during transmission.* Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group C through E is activated with one from the group F through K, the keyboard encoder generates a 5-bit code, as given in the table entitled "S2604/S2605 CODING," below. This code is loaded into a shift register in parallel with the sync and end bits to form the message.

The transmitter output is a 40kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark=1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of transmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The S2604 Encoder is, however, silenced automatically by an on-chip duration limiter if a transmission persists for 6½ seconds (FOSC=320kHz). The absence of a keyboard closure will reset the duration limiter so that a new 6½ second interval starts with the next key closure.

S2605 Decoder

The S2605 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40kHz signal input, and 8 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2605, overriding any 40kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40kHz signal from the local RC oscillator timing chain. A 40kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ±24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

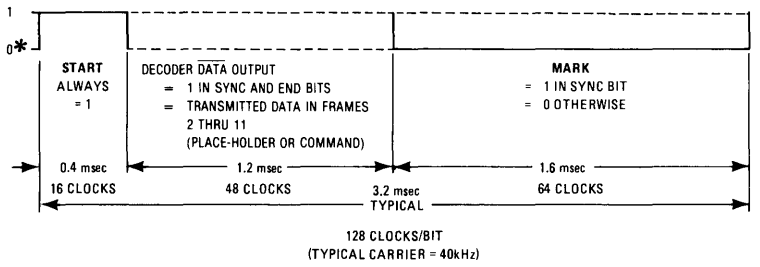
The S2605 has two other outputs: On/Off, and Analog. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated.

The On/Off ("mains") output changes state each time 10011 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

The Analog Output is a 10kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code. The Analog Output is mutable; 11110 sets it to 0% duty factor. If 11110 then disappears and reappears while the On/Off output is "On", the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2605 has an on-chip power-on reset (POR) circuit which sets the On/Off Outputs to "0", sets the Analog Outputs at 50% duty factor, and insures that Analog is not muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

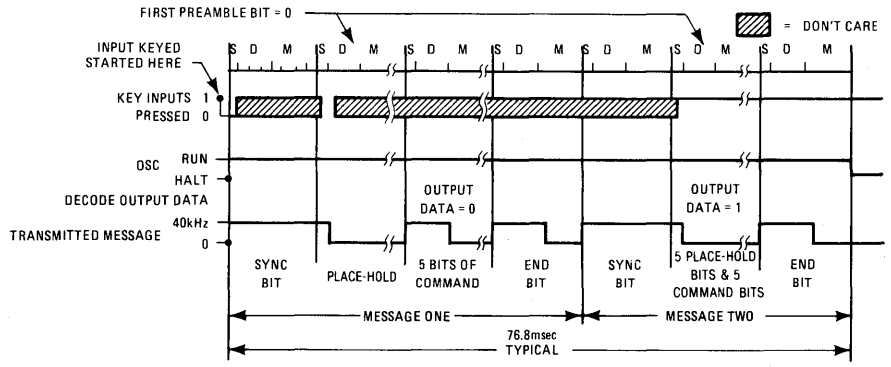
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



S2604/S2605 Coding

TRANSMITTER KEYBOARD INPUT PINS TIED TO V_{SS}	RECEIVER KEYBOARD INPUT PINS TIED TO V_{DD} (Note 1)	RESULTING RECEIVER BINARY OUTPUTS 1	2	3	4	5	RECEIVER DEDICATED FUNCTIONS
— (Note 2)		1	1	1	1	1	
DI		0	1	1	1	1	
CF		0	1	1	1	0	
DF		0	1	1	0	1	
EF		0	1	1	0	0	
CG		0	1	0	1	1	
DG		0	1	0	1	0	
EG		0	1	0	0	1	
CH		0	1	0	0	0	
DH		0	0	1	1	1	
EH		0	0	1	1	0	
EI	AE	1	0	1	0	0	
EJ	BE	1	1	0	0	0	
CI	A	1	1	1	0	0	INCREASE ANALOG (Note 5)
CJ	B	1	1	1	0	1	DECREASE ANALOG (Note 5)
CK	E	1	1	1	1	0	MUTE TOGGLE (Note 4)
EK	C	0	0	0	0	1	
DK	D	1	0	0	1	1	TOGGLE ON/OF OUTPUT
DJ	EC	0	0	0	0	0	
INVALID (Note 3)		1	1	1	1	1	(Note 3)
	AC	1	0	0	0	1	INCREASE ANALOG (Note 5)
	BC	1	0	0	1	0	DECREASE ANALOG (Note 5)

NOTES:

1. RECEIVER KEYBOARD INPUTS OVERRIDE ANY REMOTE SIGNAL.
2. REST STATE, "DATA VALID" OUTPUT **INACTIVE**
3. ANY SINGLE CLOSURE, INVALID COMBINATION OF 2 CLOSURES, OR COMBINATION OF 3 OR MORE CLOSURES OF S2604 TRANSMITTER INPUTS C, D, E, F,
4. THE MUTE TOGGLE WILL FUNCTION ONLY WHEN THE "ON/OFF" OUTPUT IS **ON.** HOWEVER MUTE IS **CLEARED** BY TURNING "ON/OFF" **OFF**, THEN **ON** AGAIN.
5. THE PULSEWIDTH OF THE ANALOG OUTPUT MAY BE CHANGED ONLY WHEN THE "ON/OFF" OUTPUT IS **ON.**

Electrical Specifications—2604 Encoder— All voltages measured with respect to V_{SS}

Absolute Maximum Ratings

Operating Ambient Temperature T_A	0 to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on any Pin	+14V
Negative Voltage on any Pin	−0.3V

Electrical Characteristics: Unless otherwise noted, $V_{DD}=8.5 \pm 1.5V$ and $T_A=0$ to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator Frequency	50	320	2000	kHz	
I_{DD}	Supply Current			2	mA	During Transmission, Data Output=1mA
	Standby			10	μ	No transmission (25°C)
V_{IH}	Input "1" Threshold	20			$\%V_{DD}$	
V_{IL}	Input "0" Threshold			80	$\%V_{DD}$	
I_{LL}	Input Source Current	50		300	μA	$V_I=OV$
I_{OH}	Output Source Current	1	1.5		mA	$V_0=V_{DD}-3V$
I_{OL}	Output Sink Current	−.2	−.5		mA	$V_0=+0.5V$

Note: Circuit operates with V_{DD} from 3.0V to 12.0V.

Electrical Specifications—2605 Decoder— All voltages measured with respect to V_{DD}

Absolute Maximum Ratings

Operating Ambient Temperature T_A ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
V_{SS} Power Supply Voltage ..... +31V
Positive Voltage on any Pin ..... V_{SS} +0.3V
Negative Voltage on any Pin ..... V_{SS} −31V

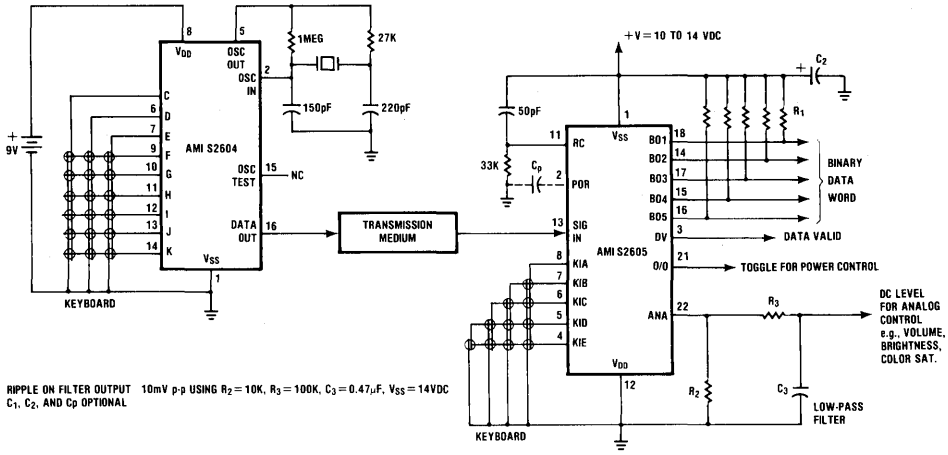
Electrical Characteristics: Unless otherwise noted, $V_{SS}=12 \pm 2V$ and $T_A=0$ to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator Frequency	512	640	768	kHz	
Δf0/f0	Frequency Deviation	−10		+10	%	Fixed R_{OSC}, C_{OSC}, V_{SS}
I_{SS}	Supply Current		34	50	mA	No Loads, $V_{DD}=14V$
			28		mA	$V_{DD}=10V$
Signal Input:						
V_{IH}	"1" Threshold			85	$\%V_{SS}$	
V_{IL}	"0" Threshold	30			$\%V_{SS}$	
V_{IH}-V_{IL}	Voltage Hysteresis	5		35	$\%V_{SS}$	
Keyboard and POR Inputs:						
V_{IH}	"1" Voltage	$V_{SS}-.5$	$V_{SS}-3.0$		V	
V_{IL}	"0" Voltage			$V_{SS}-5.5$	V	
I_{LL}	Source Current	50	150	300	μA	$V_I=V_{SS}-10V$
	Debounce Delay (Keyboard Inputs Only)	1.45		2.2	msec	
Binary Outputs (open source):						
I_{OL}	Sink Current	−0.7			mA	$V_0=V_{SS}-5.2V$, $V_{SS}=16V$
		−0.50	−0.60		mA	$V_0=V_{SS}-5.2V$, $V_{SS}=10V$
	Duration	34.9			msec	f0=704 kHz
Analog Output (open drain):						
ΔV_{step}	Step Voltage Change		$V_{SS}/64$		V	
I_{OH}	Source Current		1.04		mA	$V_0=V_{SS}-0.5V$, $V_{SS}=10V$
			1.15		mA	$V_0=V_{SS}-0.5V$, $V_{SS}=14V$
		1.0	1.2		mA	$V_0=V_{SS}-1V$
f_{step}	Analog Step Rate		10		kHz	(f0÷64)
Data Valid and On/Off Outputs:						
I_{OH}	Source Current	1	1.5		mA	$V_0=V_{SS}-2V$
I_{OL}	Sink Current	−30	−50		μA	$V_0=.7V$
t_r	Risetime (.1 V_{SS} to .9 V_{SS})			10	μsec	$R_L=\infty$, C_L 50pF
t_f	Falltime (.9 V_{SS} to .1 V_{SS})			10	μsec	$R_L=\infty$, C_L 50pF

Note: Circuit operates with V_{SS} from 7.0V to 30.0V

CONSUMER

Typical Bench Test Setup, Using a 320kHz Ceramic Resonator with S2604



AMERICAN MICROSYSTEMS, INC.

S2743/S2742

January 1981

ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

CONSUMER

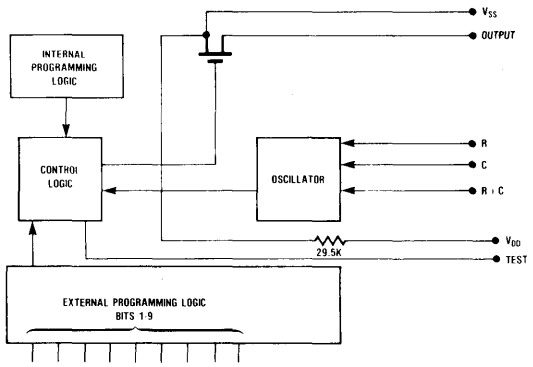
Features

- ☐ RC Oscillator Used—No Crystal Required
- ☐ Phase Locked Loop on Decoder for Reliable Operation
- ☐ 512 User Selectable Address Codes
- ☐ Encoder Operates on a Single Rail 9 Volt Supply—Suitable for Inexpensive and Convenient Battery Operation
- ☐ User can Determine the Type of Transmission Medium to Use

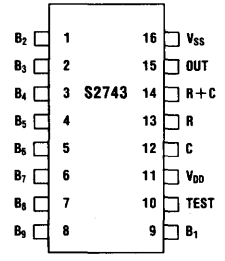
Applications

- ☐ Entry Access Systems
- ☐ Remote Engine Starting for Vehicles and Standby Generators
- ☐ Security Systems
- ☐ Traffic Control
- ☐ Paging Systems
- ☐ Remote Control of Domestic Appliances

Block Diagram 2743 Encoder

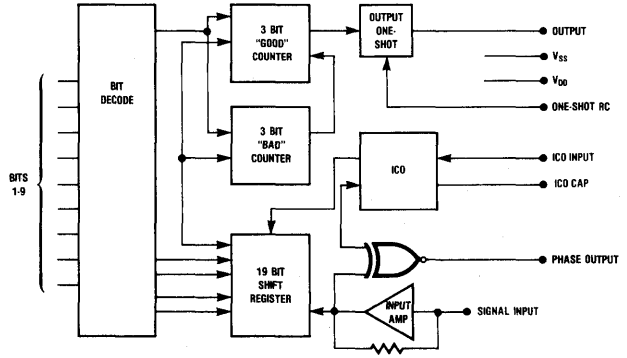


Pin Configuration 2743

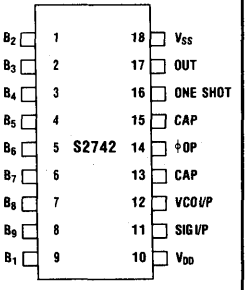


TOP VIEW

Block Diagram of 2742 Decoder



Pin Configuration 2742



TOP VIEW

General Description—Encoder/Decoder

This two-chip PMOS set includes a user-programmable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user addressable receiver. The user can select the transmission medium (RF, infrared, or hardwire). The externally selectable message allows up to 512 codes or addresses; this is done with the nine binary inputs on each device. An additional 3 bits of address can be programmed on chip as a fixed preamble.

The serial data encoder encodes by means of a frequency-shift-keyed trinary data pattern composed of 16 data bits. Each data bit will have a length equivalent to 32 cycles of high frequency clock (20kHz typical). Each trinary data pattern will be 512 cycles of 1/2 the oscillator frequency length. The encoder frequency oscillator reference is controlled with an external RC network. The encoder transmitter can be powered by a single 9 volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position there is no current flow.

The serial data decoder in conjunction with a receiver amplifier decodes the transmitted 16-bit coded signal. The on-chip phase-locked-loop locks in on the 20kHz signal even if the transmitted frequency differs from the receiver by up to ±15%. The coded signal input is compared with the externally selected code. The serial decoder looks at the transmitted signal a minimum of three times before validating a good message. A 3-bit "good" code counter or a 3-bit "bad" code counter ac cumulates the number of successive good and bad codes being received.

The decoder has an on-chip one-shot which is user programmed by an external RC combination. Whenever three complete good codes are received in the "good" counter a signal enables the one-shot which controls the signal valid output. If a series of three sequential bad codes enter the "bad" code counter the "bad" counter resets the "good" code counter and one-shot period and will not allow an active output until the end of the one-shot period. Any "good" code resets the "bad" code counter. If the "good" counter has accumulated three good codes and activated the output one shot, any occasional "good" code (occurring within the one-shot period) will maintain the output by retriggering the one-shot. The output appears like a single switch, on when "good" codes are received, off when not, with the minimum total period being determined by twice the one-shot period. The one-shot can be used to prevent the output from switching on and off to too rapidly due to system noise. The typical RC components shown in the block diagram give a period of about one second.

Functional Description—Serial Data Encoder

The AMI serial data encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically it will provide logical ones "1", logical zeroes "0", and synchronization pulses "S" and arrange them into a trinary data pattern composed of 16 data bits. Each data bit will be 32 cycles of the high frequency (HF-1/2 Oscillator Frequency) in length. Each trinary data pattern will be 512 cycles of 1/2 the Oscillator Frequency length.

A logical "1" is represented by 32 cycles of the high frequency.

A logical "0" is represented by 16 cycles of the high frequency followed directly by 8 cycles of the low frequency (LF = 1/2 HF).

A synchronization pulse "S" is represented by 16 cycles of the low frequency.

A 16-bit data pattern will be encoded in the device in such a manner as to have three (3) bits programmed internally and nine (9) bits programmed externally.

The Oscillator Frequency equals twice that of the High Frequency, and the High Frequency equals twice that of the Low Frequency.

The Oscillator circuit will require a maximum of three (3) external components (refer to Figure 2).

External programming inputs connected to the device $-V_{DD}$ supply will be considered as a logical "1". The bit programming current will not exceed 50μA. The programming resistance should not exceed 1kΩ. Unconnected external bit programming inputs will be considered at a logical "0".

A "1" ($-5V \leq$ "1" $\leq V_{DD}$) presented to the "Test" input sets the Internal counter and maintains the output of the device "On." The input impedance of the test input is greater than 5MΩ.

For portable operation a 9V transistor battery can be used for the DC voltage supply. Proper circuit polarity must be observed ($-V_{DD}$, $+V_{SS}$).

S2743 Absolute Maximum Ratings

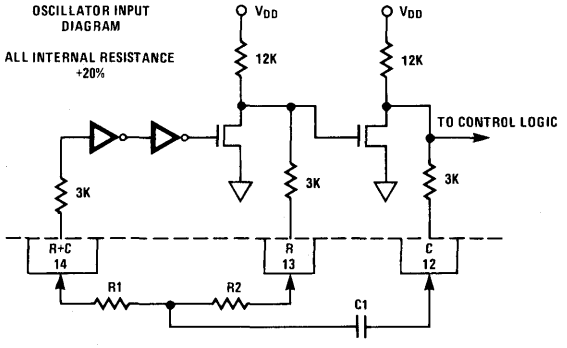
DC Supply Voltage	−15V
Input Voltage	V_{SS}+.3V to V_{SS} −15V
Operating Temperature Range	−40°C to +100°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (During Soldering)	300°C for Max. 10 sec.

S2743 Electrical Characteristics (25°C Air Temperature Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Operating Supply Voltage	−6.65	−9.5	−15	V	V_{DD}; V_{SS}=0V
	Operating Power Dissipation		27	40	MW	−8V, −5mA, Max
	Operating Frequency	2	40	60	kHz	Oscillator
	Programming Bits 1-9, Current			50	μA	Programming Input, R 1kΩ
	External Programming Resistance			1	kΩ	Bits 1-9
	(DC Bits 1-9) Program Logical "1"	V_{SS}−5V		V_{DD}	V	
	Input Levels Logical "0"	V_{SS}−1V		V_{SS}	V	
	Bits 1-9 Current		55		μA	Input R 9V>1.5M @ 5V
	Test and R+C Input Impedance	5		75	MΩ	
	(DC) Test Input Levels Test ON	V_{SS}−5V		V_{DD}	V	Maintains Output Device ON
	Test OFF (See Note 1)	V_{SS}−1V		V_{SS}	V	Permits Normal Operation
	R, C Resistance Logical "1"		12		kΩ	Resistance to V_{DD}, ±20%
	R,C Resistance Logical "0" (See Figure 1)		3		kΩ	Resistance to V_{SS} +20%−30%
	Output Current (See Note 2)	5			mA	Output Voltage=.8V W/V_{DD}=−7V

Notes: 1. Effect noted at Pin 15 to V_{SS}. 2. Output Voltage Pin 15 to V_{SS}. 3. All Voltages measured with respect to V_{SS}.

Figure 1. Serial Data Encoder



AMERICAN MICROSYSTEMS, INC.

S2747/S2748

December 1981

ENCODER/DECODER REMOTE CONTROL 2-CHIP SET

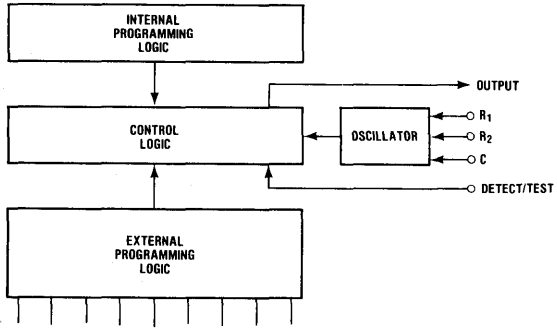
Features

- ☐ RC Oscillator Used—No Crystal Required
- ☐ 512 User Selectable Address Codes
- ☐ Low Power CMOS Encoder Operates on a Single Rail 9 Volt Supply
- ☐ Low Power CMOS Decoder Operates on a Single Rail 12 Volt Supply

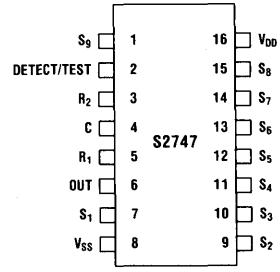
Applications

- ☐ Entry Access Systems
- ☐ Remote Engine Starting for Vehicles and Standby Generators
- ☐ Security Systems
- ☐ Traffic Control
- ☐ Paging Systems
- ☐ Remote Control of Domestic Appliances

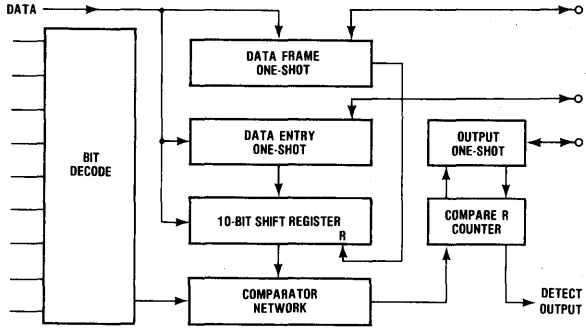
Block Diagram 2747 Encoder



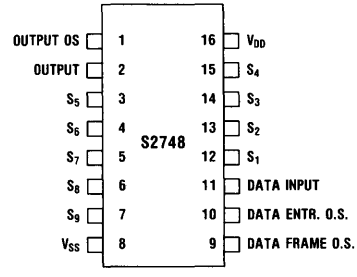
Pin Configuration 2747



Block Diagram 2748 Decoder



Pin Configuration 2748



General Description—Encoder/Decoder

This two-chip CMOS set includes a user-addressable serial data encoder for use in a simple low-power transmitter and a serial data decoder for use in a user-addressable low-power receiver. This chip set may be used with a variety of transmission media (RF, infrared, or hardwire). Up to 512 codes or addresses are externally selectable; this is done with the nine binary inputs on each device.

The serial data encoder outputs a train of ten pulses. The first pulse is a "marker" bit used to signal the decoder that a message is coming. The following nine pulses represent the encoded nine bits of binary information. The duration of the pulses output from the encoder is determined by a simple RC clock network. The encoder transmitter can be powered by a single 9-volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position, there is no current flow.

The serial data decoder, in conjunction with a receiver amplifier, decodes the transmitted signal. The coded signal input is compared with the decoder's externally selected address. The serial decoder looks at the transmitted signal a minimum of four times before validating a good message and turning the receiver's detection output on.

The decoder has an on-chip output one-shot which is user programmed by an external RC combination. This one-shot is used to prevent the detection output from switching on and off too rapidly due to system noise.

Functional Description—Serial Data Encoder

The Serial Data Encoder is comprised of three sections: Oscillator, Programming Logic, and Control Logic. Specifically, it will provide a marker pulse and nine data pulses. This 10-bit message will be output from the encoder, then a DC logic "0" pulse will be output for a time corresponding to the length of the 10-bit message.

The encoder will continue to cycle the message and the logic "0" silence period as long as power is applied to it.

Each bit of the 10-bit message is four RC oscillator periods wide. The format of each bit is the same. First, a Logic "1" is output for one oscillator period. Then, the data (or marker) value is output for the next two oscillator periods. Lastly, a logic "0" is output for one oscillator period. Thus, Logic "1" for one period, data for two periods, and Logic "0" for the last period. After a 10-bit message (40 oscillator periods) has elapsed, there will be an equivalent period of silence (Logic "0") output from the encoder, as mentioned previously.

The marker bit is equivalent to a data bit with a value of Logic "1".

The RC oscillator circuit requires a maximum of three external components (see Figure 1). To directly drive the oscillator, let encoder Pins 3 and 4 float, and apply the direct drive signal to encoder Pin 5.

The typical R_1, R_2, and C components shown in Figure 2 provide an oscillator frequently of about 1ms.

External programming inputs connected to the device will be considered as a Logic "0". Unconnected external bit programming inputs are pulled up by the chip to a Logic "1".

A Logic "1" applied to "test detect", Pin 2, resets the internal logic and forces the encoder output to a Logic "0". After the "test detect" pin is back at a Logic "0", the encoder output will be a Logic "0" for 40 RC oscillator clock periods, then the 10-bit message will begin.

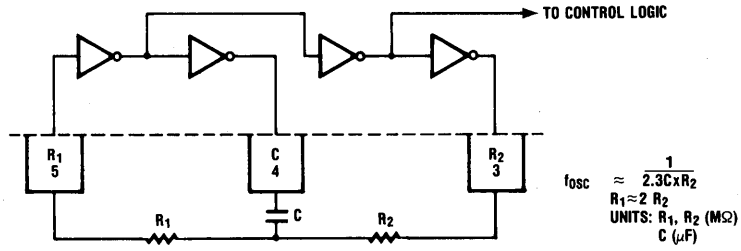
For portable operation, a 9V transistor battery with a 6V zener diode may be used for the DC voltage supply.

Functional Description—Serial Data Decoder

The Serial Data Decoder is comprised of four sections: Data Entry One-Shot, 9-Bit Digital Comparator, Good Detection Control Logic, and the Retriggerable Output One-Shot.

The Decoder is always on, looking for a "marker" pulse from the encoder. When a pulse is detected at the data input, the data entry one-shot clocks it into the first stage of a 10-bit shift register, after a user-selectable delay. As successive pulses are detected, they are similarly shifted into the shift register, with preceding shift register information shifted over one bit. As the marker bit is shifted into the tenth bit of the shift register, a comparison is made with the first nine bits of shift register information and the nine externally programmed address inputs. If a comparison is valid, a clock pulse is sent to the good detection counter logic. As mentioned in the Encoder Functional Description, a message lasts 40 encoder oscillator clock periods followed by 40 encoder oscillator clock periods of DC Logic "0". In the Decoder, it is necessary to clear the 10-bit shift register and associated logic after the message has been received and compared with the Decoder's external address bits. This is

Figure 1. Serial Data Encoder RC Oscillator



done using the data frame one-shot. The data frame one-shot provides a user-selectable delay from the end of a message until the shift register is reset. The typical RC components shown in Figure 2 provide data frame one-shot pulse width of about 10mS, while the components for the data entry one-shot will generate a 2ms pulse width clock delay during data entry.

The good detection counter circuit and the retriggerable output one-shot work together. Initially, as data begins to enter the Decoder, the output one-shot is refreshed to a Logic "1"; the detect output is off. As the output one-shot decays toward a Logic "0", the initial message is compared with the nine external address bits. If the comparison is true, a clock will increment the good detection control circuit. If four such comparisons occur, the detect output will turn on and the output one-shot will again be refreshed to a Logic "1". If less than four comparisons occur before the output one-shot decays to a Logic "0", the detect output will remain off, the output one-shot will not be refreshed to a Logic "1", and the good detection counter circuit will be reset. Once the detect output is turned on by four message detections in a single output one-shot period, it requires only one message detection per output one-shot period thereafter to keep the detect output continuously turned on. If no message detection occurs in a subsequent output one-shot period, the one-shot will decay to a Logic "0", turn off the detect output and reset the good detection counter circuit. The typical RC components shown in Figure 2 give an output one-shot period of about one second.

Also note that a logic inversion must take place external to the output of the Encoder before it is presented to the data input of the Decoder. Figure 2 shows a typical circuit to accomplish this.

S2747 Encoder Absolute Maximum Ratings

DC Supply Voltage	$V_{DD}=+9V$, $V_{SS}=0V$
Input Voltage	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Operating Temperature Range (Ambient)	−35°C to +85°C
Storage Temperature Range (Ambient)	−55°C to +150°C
Lead Temperature (During Soldering)	300°C for Max. 10 sec.

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S10110

ANALOG SHIFT REGISTER

CONSUMER

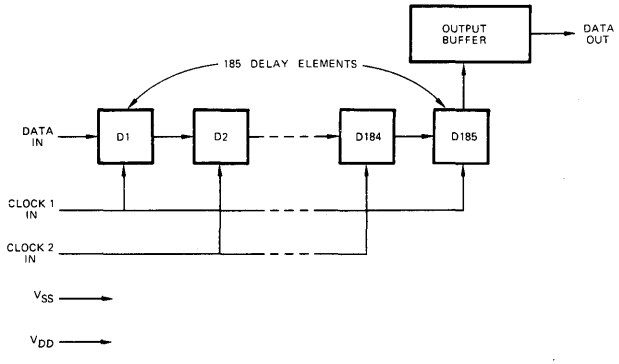
Features

- ☐ 185 Stage "Bucket Brigade" Delay Line
- ☐ Delays Audio Signals
- ☐ Accepts Clock Inputs up to 500 kHz
- ☐ Variable Delay
- ☐ Alternate to TCA 350

General Description

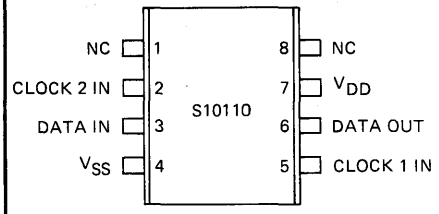
The S10110 analog shift register is a monolithic circuit fabricated with P-channel ion-implanted MOS technology. The part differs from a digital shift register, which is capable of only digital input and output information, in that an audio signal is typically supplied as the data input to the analog register, and the output is the same audio signal delayed in time. The amount of signal delay is dependent on the number of bits of delay (185) and the frequency of the two symmetrical clock inputs. Since each negative-going clock edge transfers data from one stage to the next, the analog signal delay equals 185 ÷ 2 × clock frequency.

Block Diagram

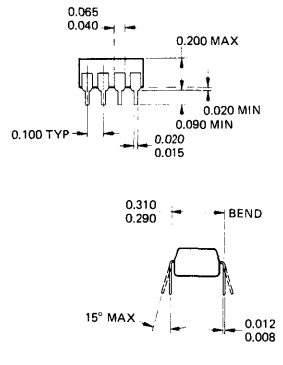


277181

Pin/Package Configuration



277182



57639

Operation

Device operation may be understood by referring to Figure 1. This is an actual schematic diagram of the analog shift register, or "bucket brigade," showing typical external bias techniques.

Data In Input:

The analog signal, or audio signal, to be delayed is applied to pin 3. This input must be biased to a negative voltage of approximately −8 volts, and two resistors may be used as a voltage divider to provide this bias. They must be chosen so that $(R_1) \pm (R_2) \div (R_1 + R_2)$ is less than 20 KΩ. The input signal applied to this input through series capacitor C_{IN} may be as high as 6 volts peak to peak.

Clock 1 and Clock 2 Inputs:

Applied respectively to pins 5 and 2, Clock 1 and Clock 2 are two symmetrical non-overlaping negative-going clocks used to transfer the analog data along the 185 bit delay line. Although these clocks may have a duty cycle as low as 25% (i.e.: each clock signal is at a negative level for 25% of its period), better output signals will be obtained with both clock duty cycles closer to 50%. It is important, however, that no overlap of the clock signals occurs at a level more negative than V_{SS}−0.8 volts.

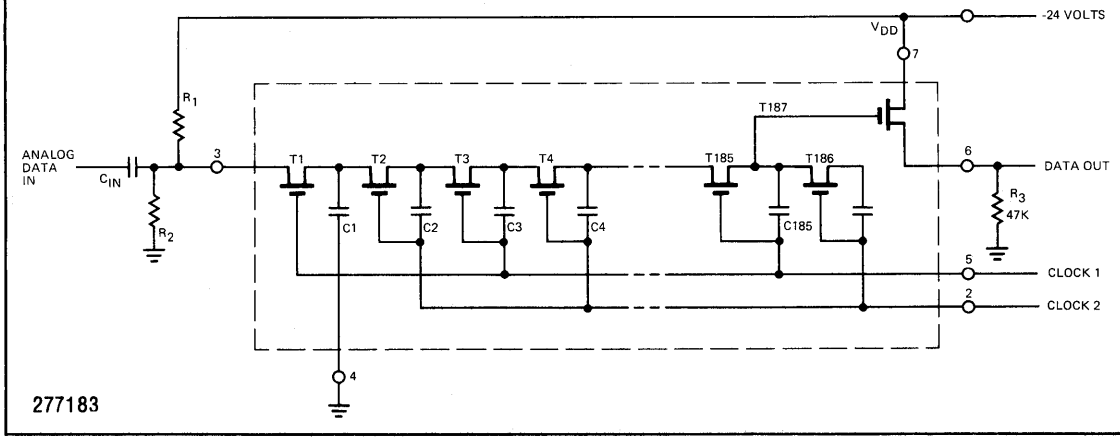
Referring again to Figure 1, it can be seen that when Clock 1 is negative, data is transferred from the data input to capacitor C1; likewise, data is transferred from each even-numbered capacitor to the capacitor to its right. When Clock 2 is negative, data is transferred from C1 to C2 and from each other odd-numbered capacitor to the capacitor to its right. In this manner, data is shifted from the input to C185 after a total of 185 negative clock pulses has occurred (i.e.: 93 periods of Clock 1 and 92 periods of Clock 2).

Data Out Output:

The output of the S10110 analog shift register is a single device, T187, with its drain at V_{DD} and its source connected to pin 6. If a 47K resistor to V_{SS} is supplied at this pin, T187 functions as a source follower.

Referring to Figure 3, it can be seen that the output potential during Clock 2 is a constant value near −10 volts. When Clock 1 switches on (negative), the output instantaneously drops to a level of approximately −30 volts; this is caused by the 20 volt swing of Clock 1 and C185. As Clock 1 remains on, device T185 transfers charge from C184 to C185, and the output voltage becomes more positive, depending on the charge previously stored on C184. It is during this part of Clock 1 that the output reflects the analog data stored on C1 185 bits earlier. Since the clock signal now appears on the output, it is necessary to apply the appropriate filtering to obtain the delayed analog signal.

Figure 1. Schematic Diagram and Pinouts of S10110



AMERICAN MICROSYSTEMS, INC.

S10129

SEVEN STAGE FREQUENCY DIVIDER

Features

- ☐ **Contains Seven Binary Dividers**
- ☐ **Triggers on Negative-Going Edge**
- ☐ **High Impedance Inputs**
- ☐ **Schmidt Trigger on Inputs**
- ☐ **No Minimum Input Rise or Fall Time Requirements**
- ☐ **Low Impedance Push-Pull Outputs**
- ☐ **Low Power Dissipation**
- ☐ **Resettable**

Applications

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

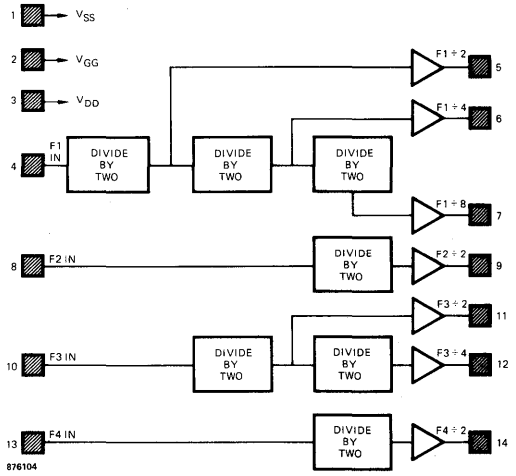
General Description

The S10129 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides seven stages of binary division in a 3-2-1-1 configuration; the S10129 is ideally suited for tone generation in electronic organs.

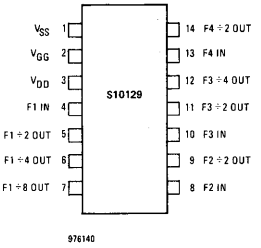
All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by V_{DD}. This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (V_{SS}) by momentarily applying a logic low level to the V_{GG} supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

Block Diagram



Pin Configuration



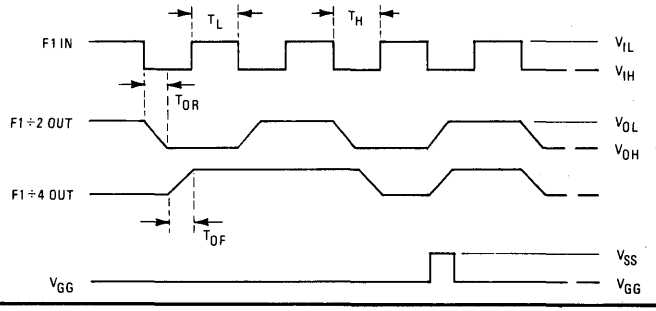
Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS} ..... +0.3V to −20V
Voltage on V_{GG} Relative to V_{SS} ..... +0.3V to −30V
Storage Temperature ..... −55°C to +150°C
Operating Temperature (ambient) ..... 0°C to +70°C

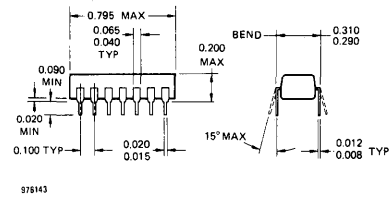
Electrical Characteristics ($0°C \le T_A \le 70°C$; $V_{DD} = -11V$ to $-16V$; $V_{GG} = -25V$ to $-29V$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Clock Low	$V_{SS}+0.3$		$V_{SS}-2.0$	V	
V_{IH}	Input Clock High	$V_{SS}-8$		V_{GG}	V	
f_{IN}	Input Clock Frequency	DC		250	kHz	
T_H, T_L	Input Clock On and Off Times	1.5			μs	
V_R	Voltage Applied to V_{GG} Input to Cause a Reset Condition	V_{SS}		$V_{SS}-0.5$	V	
T_R	Duration of V_R to Cause Reset	10			μs	50% to 50% point
V_{OH}	Output High Level	−11		V_{DD}	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{SS}
V_{OL}	Output Low Level	V_{SS}		−1	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{DD}
C_{IN}	Input Capacitance		5	10	pF	Applies to clock inputs
T_{OR}, T_{OF}	Output Rise and Fall Time		1	2	μs	40pF load applied
I_{GG}	V_{GG} Supply Current		2	3	mA	$V_{DD} = -12V$ $V_{GG} = -26V$ No load
I_{DD}	V_{DD} Supply Current		5	7	mA	$V_{DD} = -12V$ $V_{CC} = -26V$ No load

Timing Characteristics



Physical Dimensions



AMERICAN MICROSYSTEMS, INC.

S10130

SIX STAGE FREQUENCY DIVIDER

CONSUMER

Features

- ☐ **Contains Six Binary Dividers**
- ☐ **Triggers on Negative-Going Edge**
- ☐ **High Impedance Inputs**
- ☐ **Schmidt Trigger on Inputs**
- ☐ **No Minimum Input Rise or Fall Time Requirements**
- ☐ **Low Impedance Push-Pull Outputs**
- ☐ **Low Power Dissipation**
- ☐ **Resettable**

Applications

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

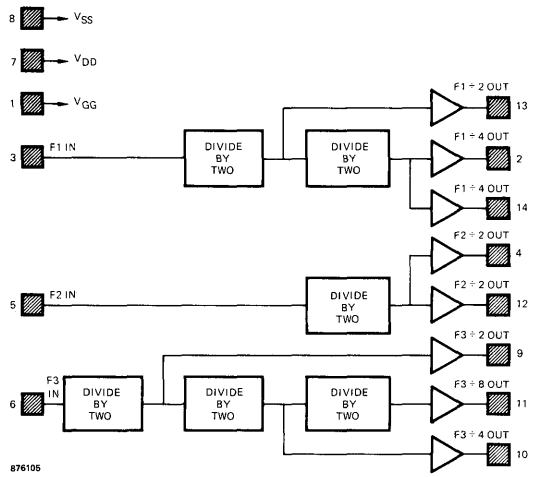
General Description

The S10130 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides six stages of binary division in a 3-2-1 configuration; the S10130 is ideally suited for tone generation in electronic organs.

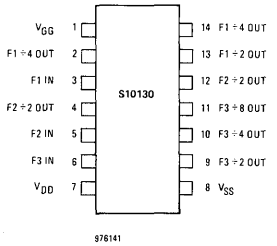
All inputs to the device are buffered to permit easy trig gering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by V_{DD}. This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (V_{SS}) by momentarily applying a logic low level to the V_{GG} supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

Block Diagram



Pin Configuration



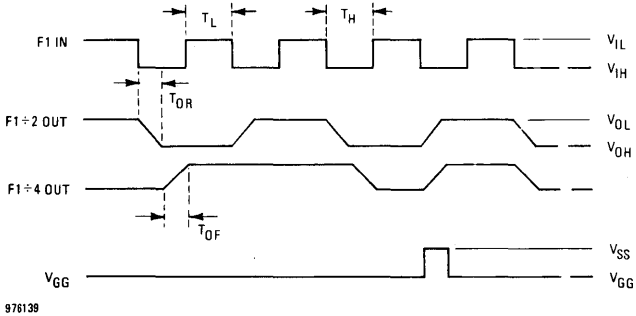
Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS} ..... + 0.3V to − 20V
Voltage on V_{GG} Relative to V_{SS} ..... + 0.3V to − 30V
Storage Temperature ..... − 55°C to + 150°C
Operating Temperature (ambient) ..... 0°C to + 70°C

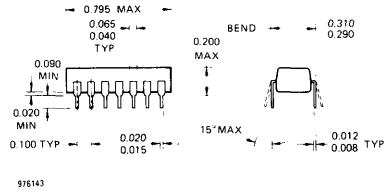
Electrical Characteristics ($0°C \leq T_A \leq 70°C$; V_{DD} = − 11V to − 16V; V_{GG} = − 25V to − 29V unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Clock Low	V_{SS} + 0.3		V_{SS} − 2.0	V	
V_{IH}	Input Clock High	V_{SS} − 8		V_{GG}	V	
f_{IN}	Input Clock Frequency	DC		250	kHz	
T_H, T_L	Input Clock On and Off Times	1.5			μs	
V_R	Voltage Applied to V_{GG} Input to Cause a Reset Condition	V_{SS}		V_{SS} − 0.5	V	
T_R	Duration of V_R to Cause Reset	10			μs	50% to 50% point
V_{OH}	Output High Level	− 11		V_{DD}	V	V_{DD} = − 12V V_{GG} = − 26V 5.5KΩ load to V_{SS}
V_{OL}	Output Low Level	V_{SS}		− 1	V	V_{DD} = − 12V V_{GG} = − 26V 5.5KΩ load to V_{DD}
C_{IN}	Input Capacitance		5	10	pF	Applies to clock inputs
T_{OR}, T_{OF}	Output Rise and Fall Time		1	2	μs	40pF load applied
I_{GG}	V_{GG} Supply Current		2	3	mA	V_{DD} = − 12V V_{GG} = − 26V No load
I_{DD}	V_{DD} Supply Current		5	7	mA	V_{DD} = − 12V V_{CC} = − 26V No load

Timing Characteristics



Physical Dimensions



AMERICAN MICROSYSTEMS, INC.

S10131

SIX STAGE FREQUENCY DIVIDER

December 1979

CONSUMER

Features

- ☐ **Contains Six Binary Dividers**
- ☐ **Triggers on Negative-Going Edge**
- ☐ **High Impedance Inputs**
- ☐ **Schmidt Trigger on Inputs**
- ☐ **No Minimum Input Rise or Fall Time Requirements**
- ☐ **Low Impedance Push-Pull Outputs**
- ☐ **Low Power Dissipation**
- ☐ **Resettable**

Applications

Electronic organ frequency generator, organ pedal frequency generator, electronic music synthesizers, N stage dividers, low frequency generation, binary counters.

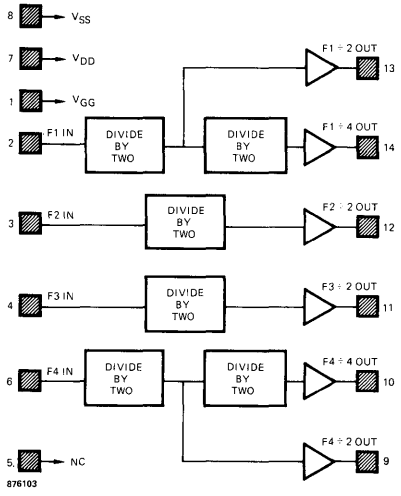
General Description

The S10131 is a monolithic frequency divider circuit fabricated with P-Channel ion-implanted MOS technology. The circuit provides six stages of binary division in a 2-2-1-1 configuration; the S10131 is ideally suited for tone generation in electronic organs.

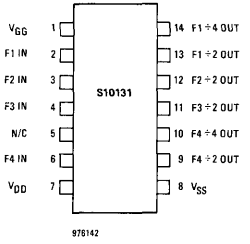
All inputs to the device are buffered to permit easy triggering of the divider stages. Outputs of each divider are buffered to provide low output impedance in both logic states to drive external circuitry as well as other dividers. The buffers have low standby current and are powered by V_{DD}. This voltage functions as a clamp voltage and thus sets the output amplitudes. Buffering the outputs also provides complete isolation between the dividers and the loads. If a buffer output is short-circuited, the divider will continue to function.

All divider outputs may be reset to a logic low level (V_{SS}) by momentarily applying a logic low level to the V_{GG} supply input. This is particularly desirable in some electronic organs in which phase relationships are important.

Block Diagram



Pin Configuration



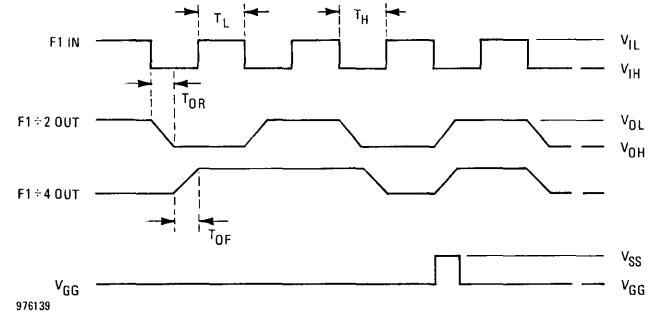
Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS} ..... +0.3V to −20V
Voltage on V_{GG} Relative to V_{SS} ..... +0.3V to −30V
Storage Temperature ..... −55°C to +150°C
Operating Temperature (ambient) ..... 0°C to +70°C

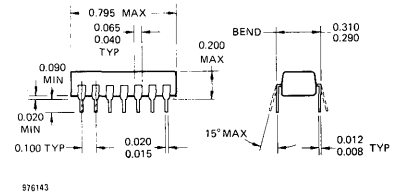
Electrical Characteristics ($0°C \le T_A \le 70°C$; $V_{DD} = -11V$ to $-16V$; $V_{GG} = -25V$ to $-29V$ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IL}	Input Clock Low	$V_{SS}+0.3$		$V_{SS}-2.0$	V	
V_{IH}	Input Clock High	$V_{SS}-8$		V_{GG}	V	
f_{IN}	Input Clock Frequency	DC		250	kHz	
T_H, T_L	Input Clock On and Off Times	1.5			μs	
V_R	Voltage Applied to V_{GG} Input to Cause a Reset Condition	V_{SS}		$V_{SS}-0.5$	V	
T_R	Duration of V_R to Cause Reset	10			μs	50% to 50% point
V_{OH}	Output High Level	−11		V_{DD}	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{SS}
V_{OL}	Output Low Level	V_{SS}		−1	V	$V_{DD} = -12V$ $V_{GG} = -26V$ 5.5KΩ load to V_{DD}
C_{IN}	Input Capacitance		5	10	pF	Applies to clock inputs
T_{OR}, T_{OF}	Output Rise and Fall Time		1	2	μs	40pF load applied
I_{GG}	V_{GG} Supply Current		2	3	mA	$V_{DD} = -12V$ $V_{GG} = -26V$ No load
I_{DD}	V_{DD} Supply Current		5	7	mA	$V_{DD} = -12V$ $V_{CC} = -26V$ No load

Timing Characteristics



Physical Dimensions



AMERICAN MICROSYSTEMS, INC.

S10430

DIVIDER-KEYER

CONSUMER

Features

- ☐ 22 Keyboard Inputs
- ☐ 88 DC Keyer Circuits
- ☐ 34 Binary Dividers
- ☐ Provides Four Pitch Outputs
- ☐ All Key Inputs Sustainable for Percussion
- ☐ All Dividers Resettable
- ☐ Provides "Any Key Down" Indication
- ☐ Eliminates Multiple-Contact Key Switches

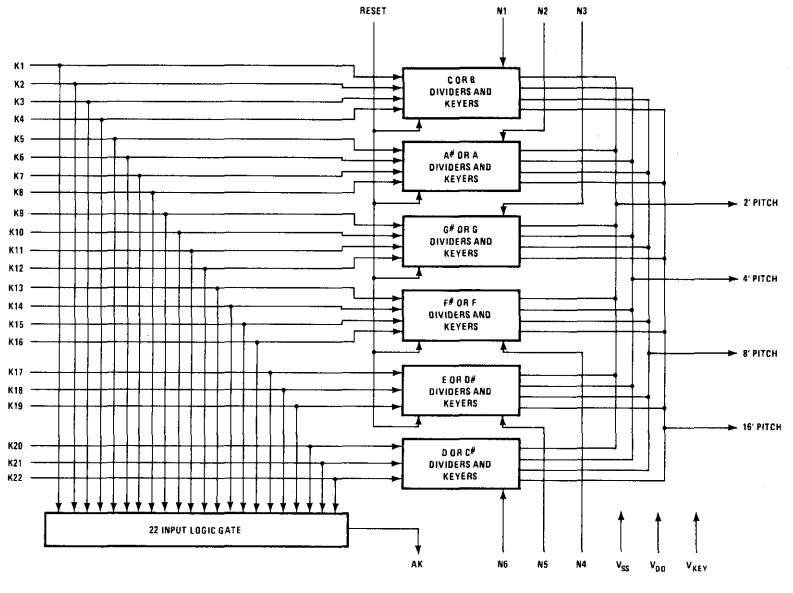
Typical Applications

- ☐ Generation and Keying of Musical Tones
- ☐ Standard Spinet Organ Keying (37 or 44 note keyboards)
- ☐ Keying of Sustained Tones
- ☐ Percussive Effects
- ☐ Generating Stair-stepped Waveforms
- ☐ Electronic Piano

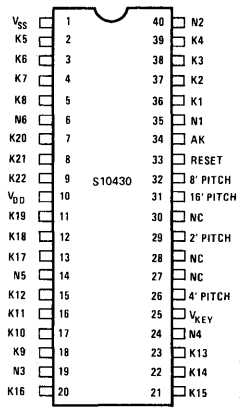
General Description

The S10430 divider-keyer is a monolithic integrated circuit fabricated with P-Channel ion-implanted MOS technology. It is intended for use in spinet organs or other electronic musical instruments having keyboards of up to 44 keys. This device has 22 key inputs, allowing all keying functions for a 44 note manual to be performed by two S10430 circuits. Each S10430 accepts six frequencies from a top octave synthesizer, such as an S50240, and provides squarewave outputs at 16 foot, 8 foot, 4 foot, and 2 foot pitches. For example, if a C key is depressed by itself a low C frequency appears at the 16 foot output, and a C frequency one octave higher appears at the 8 foot output; similarly, the 4 foot and 2 foot outputs provide C frequencies one and two octaves higher, respectively, than the C frequency of the 8 foot output. All appropriate frequency division is performed by the S10430, eliminating the need for external dividers.

Block Diagram



Pin Configuration



General Description (Continued)

The circuit also eliminates the need for multiple-contact key switches and discrete diode or transistor keyers. Because of the high input impedance of the MOS keyers used in this circuit, long sustain envelopes may be obtained by connecting low-value capacitors to the keying inputs.

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS} ..... +0.3V to -27.0V
Operating temperature (ambient) ..... 0°C to 70°C
Storage temperature ..... -65°C to 150°C

Electrical Characteristics

$0°C \leq T_A \leq 70°C$; $V_{SS} = 0V$; $V_{DD} = -12.6V$ to $-15.4V$; $V_{KEY} = -4.75V$ to $-5.25V$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IL}	Logic Low Level TOS and Reset Inputs	0.0		0.8	V	
V_{IH}	Logic High Level TOS and Reset Inputs	-4.2		V_{DD}	V	
t_r, t_f	Rise and Fall Times TOS Inputs			50	μsec	Measured between 10% and 90% points
V_{OL}	Logic Low Level AK Output		-0.5	-1.0	V	100KΩ load to V_{DD}
t_{fo}	Transition of AK Output to 10% of V_{DD}			10	μs	100pF and 100KΩ load to V_{DD}
F_T	Operating Frequency TOS Inputs	DC		50K	Hz	
D_O	Output Duty Factor	48		52	%	Measured between 10% and 90% points
I_{PA}	Peak Output Current Absolute (any pitch output with 1 keyer on)	350		650	μA	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -25V$ $T_A = 25°C$
I_P	Peak Output Current	85		115	$\%I_{AVE}$*	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -25V$ $T_A = 25°C$
I_P	Peak Output Current	50		75	$\%I_{AVE}$*	$V_{DD} = -14V$ $V_{KEY} = -5V$ $V_{EN} = -15V$ $T_A = 25°C$

*I_{AVE} is the average of all peak output current values within one circuit.

AMERICAN MICROSYSTEMS, INC.

S2567

RESETTABLE RHYTHM COUNTER

CONSUMER

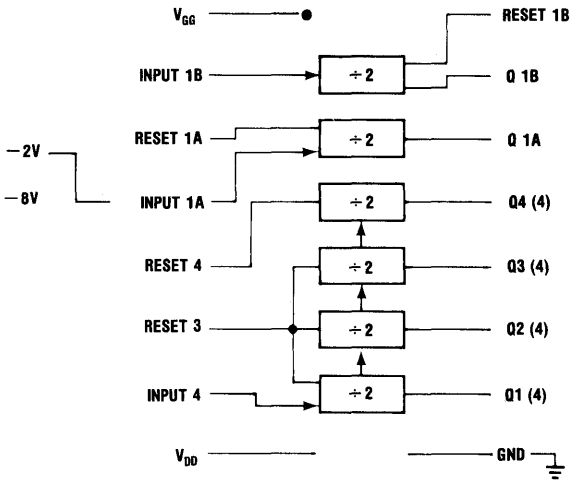
Features

- ☐ Pin for Pin Equivalent to GEM 567 and MC1181L
- ☐ Organ Rhythm Sections
- ☐ Portable Rhythm Sections
- ☐ Automatic Rhythm Organs

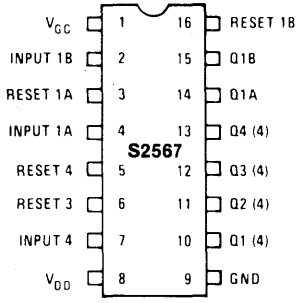
General Description

The S2567 Resettable Rhythm Counter is a six-stage asychronous binary counter designed for driving the count-address inputs of the S2566 Rhythm Generator. The internal partitioning and multiple-reset capability of the S2567 permit simultaneous generation of different meter rhythms. The S2567 Resettable Rhythm Counter is made by P-channel enhancement mode technology and is supplied in a 16-lead dual in-line package.

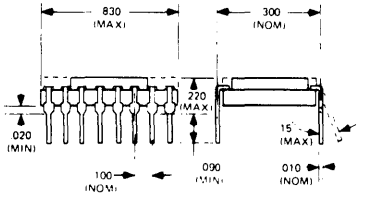
Block Diagram



Pin Configuration



Physical Dimensions



Absolute Maximum Ratings: @25°C, unless otherwise noted
Logic Supply Voltages:

V_{GG}	+0.3V to −33V
V_{DD}	+0.3V to −25V
V_I Trigger Voltage	+0.3V to −18V
P_D Power Dissipation	250mW
T_S Storage Temperature	−55°C to +100°C
T_A Operating Temperature	−0°C to +60°C

Dynamic Characteristics: $T_A = -25°C$
Operating Voltage Ranges:

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{GG}		−25	−27	−29	V
V_{DD}		−14	−15	−16	V
Inputs: (Pins 2 thru 7, and 16)					
f_I	Input Frequency	DC		100	kHz
V_{IH}	Logic "0" Level	+0.3		−2.0	V
V_{IL}	Logic "1" Level	−8.0		−18	V
t_r, t_f	Rise and Fall Times			25	μs
PW_I	Pulse Width	2			μs
I_{IL}	Leakage Current ($V_{ILT} = -18V$)			1	μA
Outputs: (Pins 10 thru 15, each loaded 20K to GND and 20K to V_{DD})					
V_{OH}	Logic "0" Level	0		−1.5	V
V_{OL}	Logic "1" Level	−9.0		V_{DD}	V
Reset Propagation Delay				2.0	μA
Supply Currents: (no output loads)					
I_{GG}			4	6	mA
I_{DD}				20	μA

AMERICAN MICROSYSTEMS, INC.

S2688

DIGITAL NOISE GENERATOR

June 1978

CONSUMER

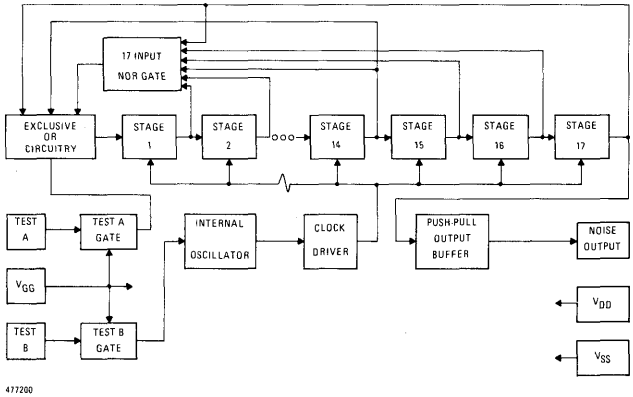
Features

- ☐ Internal Oscillator
- ☐ Consistent Noise Quality
- ☐ Consistent Noise Amplitude
- ☐ Zero State Lockup Prevention
- ☐ Zeros Can Be Externally Forced Into The Register
- ☐ Oscillator Can Be Driven Externally
- ☐ Operates With Single or Dual Power Supplies
- ☐ Eliminates Noise Preamps
- ☐ Alternate to MM5837

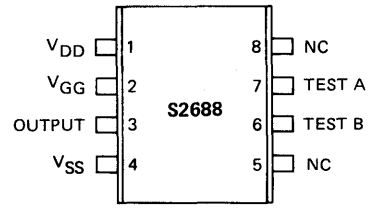
General Description

The S2688 noise generator circuit is fabricated in P-Channel ion implanted MOS technology and supplied in an eight-lead dual in-line plastic package. The device contains a 17-bit shift register which is continuously clocked by an internal oscillator. Exclusive OR feedback from the 14th and 17th stages causes the register to generate a pseudo-random noise pattern, and an internal gate is included to prevent the register from reaching an all zero lockup state. To facilitate testing, the device can be easily clocked by an external source.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Positive Voltage on any Pin	V_{SS} +0.3V
Negative Voltage on any pin except V_{GG}	V_{SS} - 28V
Negative Voltage on V_{GG} Supply Pin	V_{SS} - 33V
Storage Temperature	- 65°C to +150°C
Operating Ambient Temperature	0°C to +70°C

Electrical Specifications (0°C < T_A < 70°C; V_{SS} = 0 volts; V_{DD} = - 14.0V ± 1.0V; V_{GG} = 27.0V ± 2V; unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OH}	Output Logic 1 Level	V_{SS} - 1.5		V_{SS}	Volts	20KΩ load to V_{DD}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} +1.5	Volts	20KΩ load to V_{SS}
V_{OL}	Output Logic 0 Level	V_{DD}		V_{DD} +3.5	Volts	20KΩ load to V_{SS} V_{GG} = V_{DD} = - 14V ± 1.0V
Z_{IN}	Input Impedance (Test Inputs)		10		pF	
I_L	Leakage Current (Test Inputs)			500	nA	
f_o	Frequency of Internal Oscillator		100		kHz	
I_{DD}	V_{DD} Supply Current			4.0	mA	No output load
I_{GG}	V_{GG} Supply Current			500	μA	
f_{TEST}	Test Frequency	80		105	kHz	

Operation

The S2688 is a 17-bit digital shift register driven by an internal oscillator circuit. Outputs from the 14th and 17th stages are connected to an Exclusive OR circuit whose output provides the data input for the register. The 17th stage of the register is connected to a push-pull buffer, which is the circuit's output. This output provides continuous constant amplitude pseudo-random noise; that is, for any time slot, ones and zeroes have an almost equal probability of occurrence.

Typical Applications

- ☐ Percussion Instrument Voice Generators for Rhythm Units
- ☐ Electronic Music Synthesizers
- ☐ Simulated Pipe "Wind" Noise
- ☐ Acoustics Testing

Power Supplies

The S2688 noise generator may be operated with either one or two power supplies. In applications where a high output drive level is not critical, or where the output is loaded with a resistive load connected to V_{DD}, it is possible to operate the device from a single supply voltage; in this case, the V_{GG} supply pin is connected to the V_{DD} supply voltage. If a low impedance logic "0" level output is required, this can be achieved by connecting the V_{GG} supply pin to a more negative voltage.

Zero State Lockup Prevention

If the outputs of all 17 stages of the shift register were simultaneously to reach a "0" logic level, and no logic were provided to prevent this state from occuring, then the register would remain in the "all-zero" state.

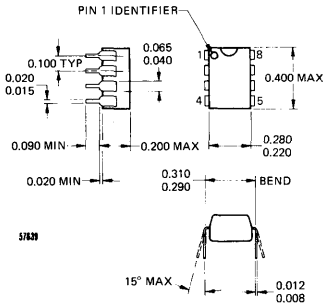
In this condition, the output would lockup and remain at a logic "0" level. This situation could occur when power is initially applied, or when triggered by noise spikes. To prevent this condition, a 17 input NOR gate is provided internally to decode the "all-zero" state and feed a logic "1" level into the register's data input.

Test Inputs

The S2688 has been designed to facilitate testing of the part. In the normal mode of operation, pins 6 and 7 are not used and appear to be open circuits. However, when the V_{GG} pin is connected to V_{SS}, these pins become test pins. Pin 7 (Test A) is used to force zeroes into the register, and pin 6 (Test B) becomes the clock input, driving the internal oscillator network. During the entire test period a 20KΩ load must be tied to V_{DD}.

Package Outline

8-Pin Plastic



CONSUMER

AMERICAN MICROSYSTEMS, INC.

S50240/S50241/S50242

TOP OCTAVE SYNTHESIZER

Features

- ☐ Single power supply
- ☐ Broad supply voltage operating range
- ☐ Low power dissipation
- ☐ High output drive capability
- ☐ S50240—50% output duty cycle
- ☐ S50241—30% output duty cycle
- ☐ S50242—50% output duty cycle

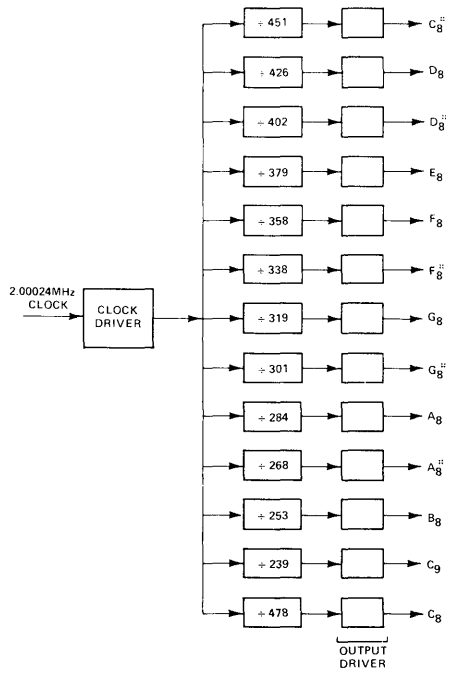
General Description

The S5024 is one of a family of ion-implanted, P-channel MOS, synchronous frequency dividers.

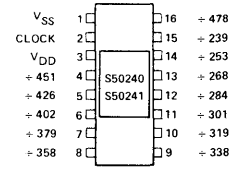
Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

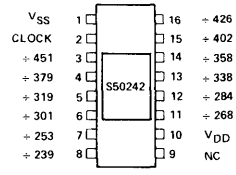
Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the S5024 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 360 mW of power. The circuits are packaged in 16 pin plastic dual-in-line packages.

Block Diagram



Pin Connections





RFI emination and feed-through are minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise time under no load conditions to reduce the R.F. harmonic content of each output signal.

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	+0.3V to −20V
Operating Temperature (Ambient)	0 °C to 50 °C
Storage Temperature (Ambient)	−65 °C to +150 °C

Recommended Operating Conditions

(0 °C ≤ T_A ≤ 50 °C)

Symbol	Parameter	Min	Typ	Max	Units	Figure
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−14.0	−16.0	V	

Electrical Characteristics

(0 °C ≤ T_A ≤ 50 °C; V_{DD} = −11 to −16V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Figure
V_{IL}	Input Clock, Low	0		−1.0	V	Figure 1
V_{IH}	Input Clock, High	−10.0		V_{DD}	V	Figure 1
f_I	Input Clock Frequency	100	2000.240	2250	kHz	
t_r, t_f	Input Clock Rise & Fall Times 10% to 90% @ 2.5MHz			50	nsec	Figure 1
t_{ON}, t_{OFF}	Input Clock On and Off Times @ 2.5MHz		200		nsec	Figure 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ 1.0mA	V_{DD} +1.5		V_{DD}	V	Figure 2
V_{OL}	Output, Low @ 1.0 mA	V_{SS} −1.0		V_{SS}	V	Figure 2
t_{ro}, t_{fo}	Output Rise & Fall Times, 500 pF Load 10% to 90%	250		2500	nsec	Figure 3
t_{ON}	Output Duty Cycle-S50240, S50242		50		%	
	S50241		30		%	
I_{DD}	Supply Current		14	22	mA	Outputs Unloaded

CONSUMER

Figure 1. Input Clock Waveform

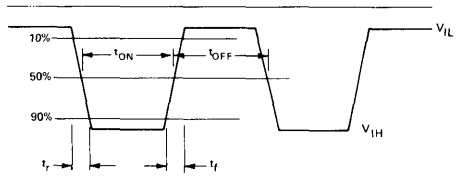


Figure 2. Output Signal DC Loading

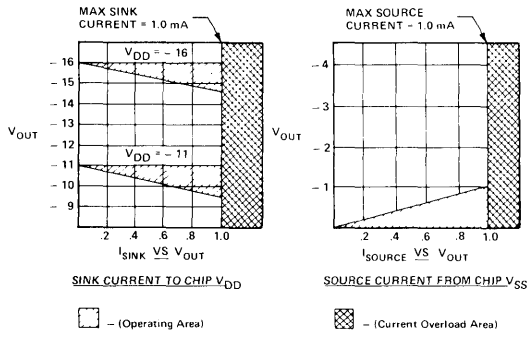
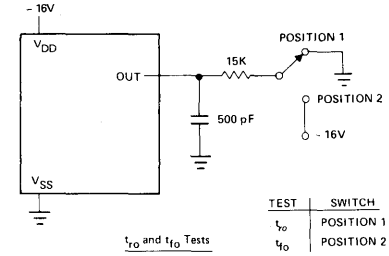
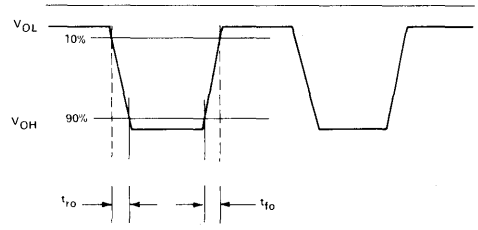


Figure 3. Output Rise and Fall Times





AMERICAN MICROSYSTEMS, INC.

S4003

July 1982

AUTO CLOCK

CONSUMER

Features

- ☐ **12 Hour, 4 Digit Auto Clock.**
- ☐ **Elapsed Time Counter (resettable, range to 99 hours).**
- ☐ **Calendar (4-year calendar with pin option for European date/month reversal).**
- ☐ **Ignition-Sensing Display Cut-off (to reduce battery drain when the auto is not operating).**
- ☐ **Crystal Input Accuracy (uses inexpensive 4.194 mHz crystal).**
- ☐ **Direct Display Drive (4-digit vacuum fluorescent displays, 24 Volts).**

Applications/Markets

- ☐ Automotive
- ☐ Avionics
- ☐ Marine
- ☐ Portable Clocks
- ☐ Industrial

General Description

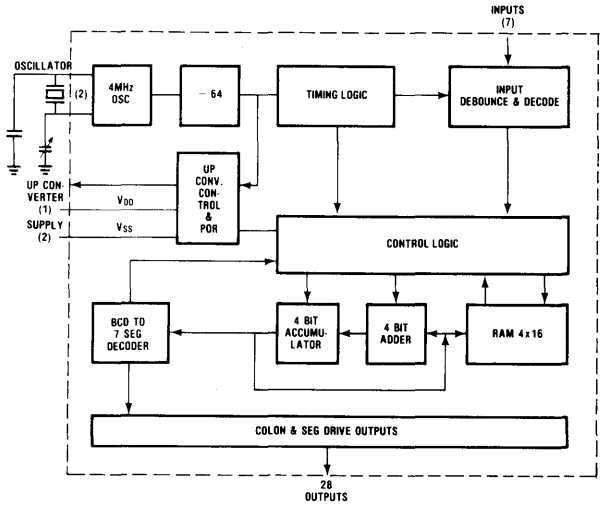
The S4003 Auto Clock is a PMOS integrated circuit which has found wide application in auto, avionic and marine applications as a portable or dashboard clock and as an industrial timer.

A functional description of the inputs/outputs and registers follows:

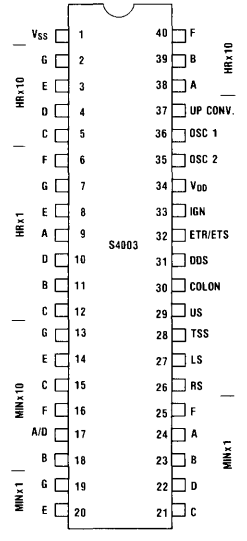
1. **Set Inputs**—Left digits set and right digits set will index the selected register at a 2Hz rate. Indexing either input will not upset the unselected digits.

2. **Time Set Select**—Enables set inputs to the timekeeping register. When updating hours, the minutes display will blank out and MX1 digit will display A or P. Minutes will update in a normal manner and reset seconds to zero. Seconds will restart on release of the time set select line. When deselected, the time will continue to be displayed for 5 seconds ±1 seconds. AM and PM indications will switch on the transfer from 11:59 to 12:00.

Block Diagram



Pin Configuration



3. **Elapsed Time Select**—Displays contents of elapsed time register while active. Left set will stop E.T. accumulation, right set or E.T. reset will restart accumulation of E.T.

4. **Elapsed Time Reset**—Displays, zeros, and restarts the elapsed time register.

5. **Date Select**—Displays the contents of the calendar register and enables set inputs. When deselected, the date will continue to be displayed for 5 ±1 seconds. If elapsed time select is true, the 5 seconds counter shall be inhibited.

6. **Ignition Off**—When ignition is off, all set inputs will be inactive and display outputs will be turned off. When ignition is turned on, the date will display for 5 seconds then revert to time.

7. **Time Register**—The time register is a 12 hour register. The time register shall be normally selected with no control inputs selected. When time set select and ignition sense are both true, the 5 seconds date counter shall be inhibited.

8. **Elapsed Time Register**—The elapsed time register shall be capable of accumulating time up to 99 hours and 59 minutes. The display shall be minutes and seconds to 59 minutes and 59 seconds then switch automatically to hours and minutes format. After 99 hours and 59 minutes, the elapsed time will reset to 00:00 and continue accumulation in minutes and seconds format as detailed above. All leading zeros shall be displayed.

9. **Date Register**—The date register will be a 4 year "smart" calendar. A month/date and date/month format will be pin selectable. The set inputs shall index the appropriate left or right digits regardless as to which format is selected. Date will advance on the transfer from PM to AM.

Date Setting—When date of month is set, the number will advance to the maximum allowed for the particular month being displayed. Further advance will reset the date to "01" and continue advancing as before. When the month is being set and the date is greater than that allowed for that month, (i.e., 02 30), the next timekeeping switch from PM to AM will advance the month and set the date to "01" (i.e., 03 01).

10. All registers are to be independent, i.e., setting time will not index calendar.

11. All registers will continue to accumulate while ignition is off.

12. Colons shall be non-flashing and displayed in the time display and elapsed time modes. Colons shall be extinguished in the date display mode.

13. On initial power up or in case of battery disconnect, the display shall read 0:00 on all functions until time is set. Voltage rise time to 10 volts will be greater than 10 mSeconds.

14. **Register Preference**—If more than one register for display is selected at one time, time will have preference over date, date will have preference over elapsed time.

15. **Illegal Conditions**—If either date, time, or E.T. reset inputs are true at the same time, the clock display shall blank. All set inputs will be disabled while the clock is in an illegal mode.

16. **Test Condition**—When date select, elapsed time select, time set select, and both right and left set inputs are true, the clock may enter a test mode.

17. **Switch Debounce Protection**—All setting inputs shall be protected against switch debounce for a period of 13 mSeconds min.

S4003 Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions
V_{SS} Supply Voltage Outputs Operational	9	20	24	Volts	V_{DD}=GND
V_{SS} Supply Voltage No Loss of Memory	7		24	Volts	V_{DD}=GND
V_{SS} Supply Voltage	7		24	Volts	Voltage to be ramped up from 0 volts (time constant 10ms from 0 to 10 volts)
I_{SS} Supply Current		5	6.5	mA	V_{SS}=12V 25°C
No Output Loads		10	15	mA	V_{SS}=20V
F0 Crystal Frequency		4.194304		MHz	
Fc Converter Frequency		65.536		KHz	
Converter Frequency Start w/Ignition Sense Off		8		Volts	V_{DD}=GND
Input Voltage					
V_{IH}	V_{SS}-1		V_{SS}	Volts	
V_{IL} (Except Ignition Sense)	V_{DD}		V_{DD}+1	Volts	
Ignition Sense (On)	+5.0			Volts	V_{SS}=9 to 20V
(Off)			+1.0	Volts	V_{DD}=GND
Output Currents					
Segment (Single) I_{OL}	0.5			mA	$V_{OH}=V_{SS}$-1
I_{OH}	1.0			μA	Leakage to V_{DD} (Output Off)
(A&D MX10) I_{OL}	1.0			mA	$V_{OH}=V_{SS}$-1
I_{OH}	1.0			μA	Leakage to V_{DD} (Output Off)
Converter I_{OH}	3.0			mA	V_{SS}-2, V_{SS}=18V
	1.0			mA	V_{SS}-2, V_{SS}=7V

Absolute Maximum Ratings:

1) Positive voltage on any pin: V_{SS} + 0.3V
2) Negative voltage on any pin: V_{SS} - 30.0V
3) Storage Temperature: -60°C to 150°C
4) Operating Temperature: −40°C to +85°C

CONSUMER

UNIVERSAL DRIVER

Features:

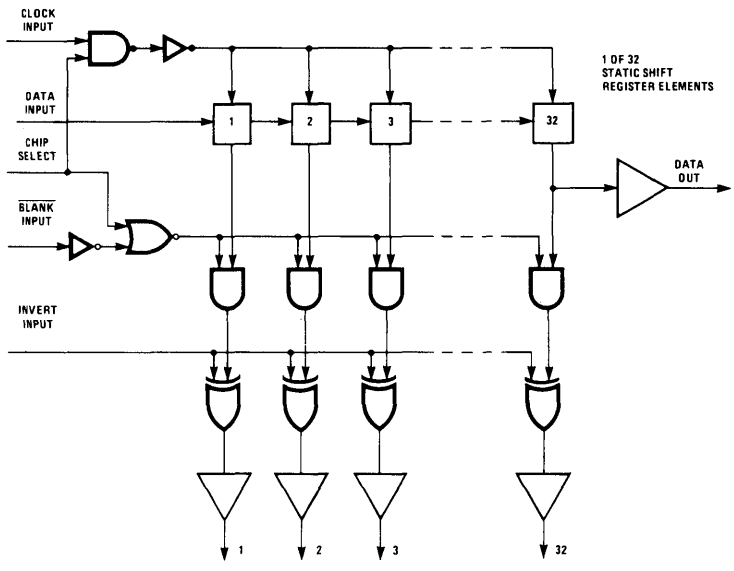
- ☐ 32 Bit Storage Register
- ☐ 32 Output Buffers
- ☐ Expansion Capability for More Bits
- ☐ Reduced RFI Emanation
- ☐ Wired OR Capability for Higher Current

General Description

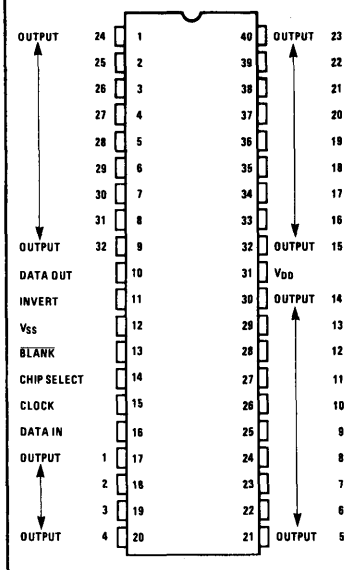
The S2809 Universal Driver is a P-Channel MOS integrated circuit. Data is clocked serially into a 32-bit master-slave static shift register. This provides static parallel drive to the output bits through drive buffers. To reduce RFI emanation, capacitors have been integrated on the circuit for reduction of output switching speeds. Serial interconnection of circuits is made possible by the Data Out Output, allowing additional bits to be driven.

Two or more outputs may be wired together for higher sourcing currents; useful in applications such as triac triggering or low voltage incandescent displays. The S2809 can also be used as a parallel output device for μC's such as AMI's S2000 series single chip microcomputer.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Operating Ambient Temperature T_A	10°C to +70°C
Storage Temperature	−65°C to +150°C
V_{SS} Supply Voltage	+25V
Positive Voltage on Any Pin	V_{SS} +0.3V

Electrical Characteristics (V_{DD}=0V, 8V < V_{SS} < 22V, T_A=10°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Logic 1 Level (Data, Clock, Invert, Chip Select Inputs)	V_{SS} −0.7		V_{SS} +0.3	V	
V_{IL}	Logic 0 Level (Data, Clock Invert, Chip Select Inputs)	V_{DD}		V_{SS} −7	V	
V_{BH}	Logic 1 Level ($\overline{\text{Blank}}$ Input)	V_{SS} −4.0		V_{SS} +0.3	V	
V_{BL}	Logic 0 Level ($\overline{\text{Blank}}$ Input)	V_{DD}		V_{SS} −7	V	
I_B	Current Sinked or Sourced by $\overline{\text{Blank}}$ Input			1.0	μA	Voltage applied to Blank Input between V_{DD} & V
C_B	Capacitance of $\overline{\text{Blank}}$ Input			12	pF	
I_{OH}	Output Source Current	9.0			mA	$V_{OUT}=V_{SS}$ −3
I_{OH}	Output Source Current	4.0			mA	$V_{OUT}=V_{SS}$ −1.5
I_{OS}	Sink Current Output Load Device			50	μA	Output voltage=V_{SS}
I_{OS}	Sink Current Output Load Device	10			μA	Output voltage=V_{DD} +3V
I_L	Output Leakage Current (Output Off)			10.0	μA	
I_{DD}	Supply Current			3.0	mA	Not including output source and sink current
I_{OM}	Maximum Total Output Loading			300	mA	All outputs on
f_c	Clock Frequency	DC		100K	Hz	
t_{ON}	Clock Input Logic I Level Duration	3.0			μs	
t_{OFF}	Clock Input Logic 0 Level Duration	6.5			μs	
t_{ro}, t_{fo}	Display Output Current Rise and Fall Times	10		150	μs	*Measured between 10% and 90% of output current V_{SS} +11V, I_{OH}=9ma

* **NOTE:** With supply voltages higher than 11 volts, delay exists before an output rise or fall. This delay will not exceed 100μs with a 22 volt supply.

CONSUMER

Functional Description

The 32-bit static shift register stores data to be used for driving 32 output buffers. Data is clocked serially into the register by the signal applied to the Clock Input whenever a logic 1 level is applied to the Chip Select Input; during this time, outputs are not driven by the shift register but will go to the logic level of the invert input. With a logic 0 level applied to the Chip Select Input, the 32 outputs are driven in parallel by the 32-bit register. It is possible to connect S2809 circuits in series to drive additional bits by use of the Data Output.

Clock Input

The Clock Input is used to clock data serially into the 32-bit shift register. The signal at the Clock Input may be continuous, since the shift register is clocked only when a logic 1 level is applied to the Chip Select Input. As indicated in Table 1, data is transferred from QN-1 to QN on the negative transition of the Clock Input.

Data Input

Whenever a logic 1 level is applied to the Chip Select Input, data present at the the Data Input is clocked into the 32-bit master-slave shift register. Data present at the input to the register is clocked into the master element during the logic 1 clock level and thus must be valid for the duration of the positive clock pulsewidth. This information is transferred to the slave section of each register bit during the clock logic 0 level.

Chip Select

The Chip Select Input is used to enable clocking of the shift register. When a logic 1 level is applied to this input, the register is clocked as described above. During this time, the output buffers are not driven by the register outputs, but will be driven to the logic level present at the Invert Input. With a logic 0 level at the Chip Select Input, clocking of the register is disabled, and the output buffers are driven by the 32 shift register elements.

Blank Input

This input may be used to control display intensity by varying the output duty cycles. With a logic 0 level at the Blank Input, all outputs will turn off (i.e., outputs will go to the logic level of the Invert Input). With a logic 1 level at the Blank Input, outputs are again driven in parallel by the 32 shift register elements (assuming the Chip Select Input is at logic 0).

The Blank Input has been designed with a high threshold to allow the use of a simple RC time constant to control the display intensity. This has been shown in Figure 1.

Invert Input

The Invert Input is used to invert the state of the outputs, if required. With a logic 0 level on this input, the logic level of the outputs is the same as the data clocked into the 32-bit shift register. A logic 1 level on the Invert Input causes all outputs to invert.

Data Output

The Data Out signal is a bufferered output driven by element 32 of the shift register. It is of the same polarity as this last register bit and may be used to drive the Data Input of another S2809. In this manner, S2809 circuits may be cascaded to drive additional bits.

Table 1. Logic Truth Table

DATA IN	CLOCK	CHIP SELECT	$\overline{\text{BLANK}}$	INVERT	Q1	QN	DRIVER OUTPUT
X	X	0	0	0			0
X	X	0	0	1		NO CHANGE	1
X	X	0	1	0			QN
X	X	0	1	1			$\overline{\text{QN}}$
0	⌐	1	X	0	0	QN−1→QN	0
1	⌐	1	X	0	1	QN−1→QN	0
0	⌐	1	X	1	0	QN−1→QN	1
1	⌐	1	X	1	1	QN−1→QN	1

Figure 1. Typical Display Intensity Control

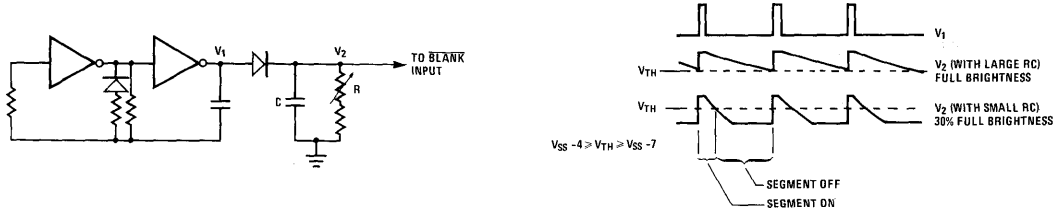


Figure 2. LED Drive — Series

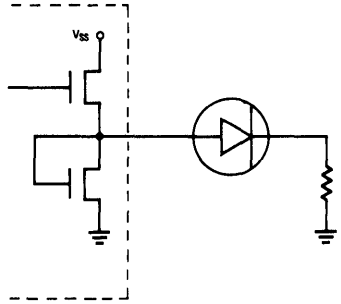


Figure 3. LED Drive — Shunt

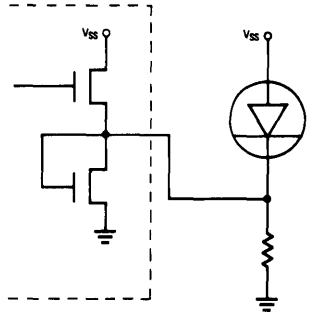


Figure 4. Vacuum Fluorescent Drive

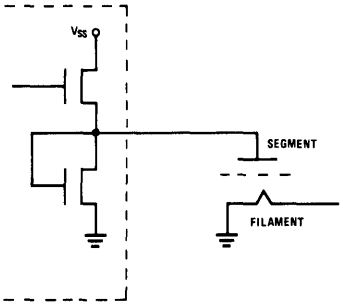


Figure 5. Liquid Crystal Drive

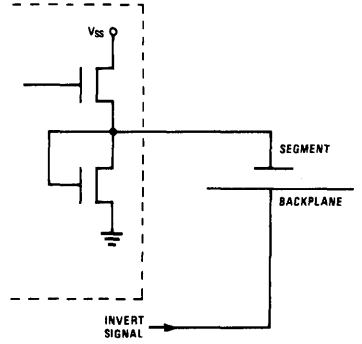
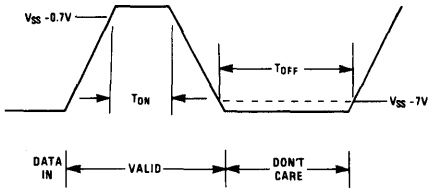
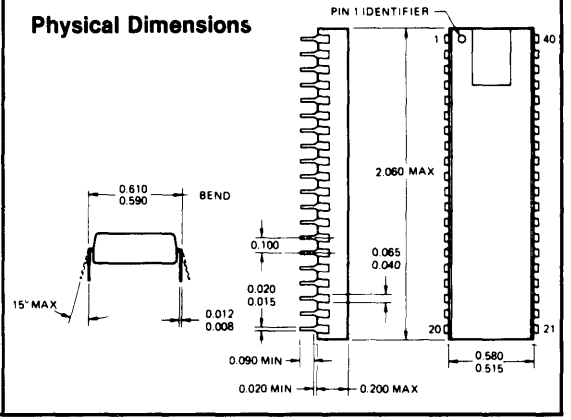


Figure 6. Clock Input Waveform



Physical Dimensions



32 BIT, HIGH VOLTAGE DRIVER

Features:

- ☐ High Voltage Outputs Capable of 60 Volt Swing
- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

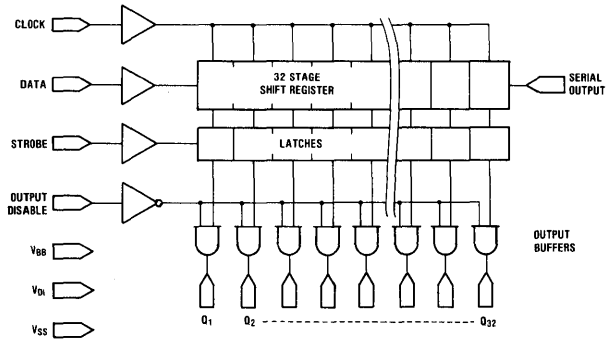
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

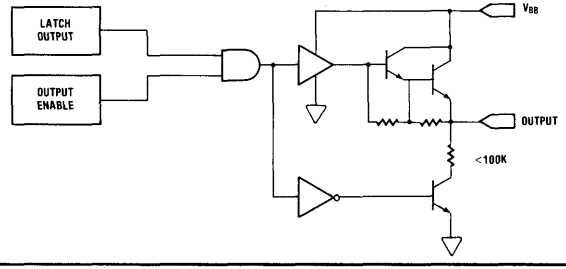
General Description

The AMI S4535 is a high voltage MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 25mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

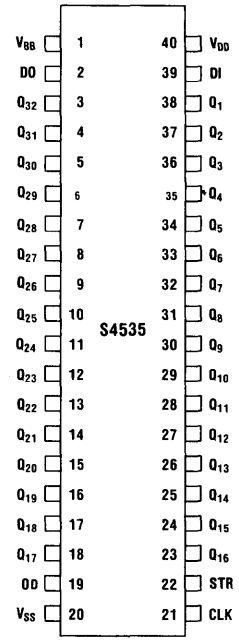
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	12V
V_{IN}	$V_{SS}-.3V$ to $V_{DD}+.3V$
V_{OUT} (Logic)	$V_{SS}-.3V$ to $V_{DD}+.3V$
V_{OUT} (Display)	$V_{SS}-.3V$ to $V_{BB}+.3V$
Power Dissipation	1.6W
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C

Operational Specification: $0°C \leq T_A \leq 70°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	−0.3	0.8	V	
V_{IH}	Input One Level	3.5	$V_{DD}+0.3$	V	
V_{SL}	Signal Out Zero Level	V_{SS}	0.5	V	$I_{SO}=-20\mu A$
V_{SH}	Signal Out One Level	$V_{DD}-0.5$	V_{DD}	V	$I_{SO}=20\mu A$
V_{DD}	Logic Voltage Supply	4.5	5.5	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		35	mA	No Loads, T=25°C
I_{BB}	Display Supply Current		10 168	mA mA	No Loads, T=25°C With Load
V_{OL}	Output Zero Level	V_{SS}	1.0	V	$I_O=-20\mu A$
V_{OH}	Output One Level	$V_{BB}-2.5$ $V_{BB}-3.2$	V_{BB} V_{BB}	V V	$I_O=5mA$ $I_O=25mA$, One Output
t_{SD}	Serial Out Prop. Delay		500	ns	$C_L=50pF$
t_{PD}	Parallel Out Prop. Delay		5	μs	$C_L=50pF$
t_W	Input Pulse Width	500		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	50		ns	

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

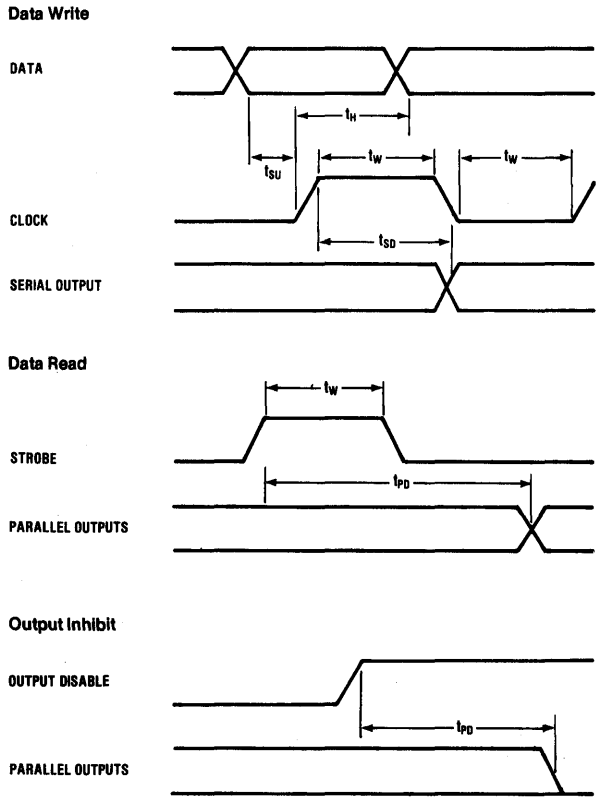
Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

Pin Description

Pin #	Name	Description
20	V_{SS}	Ground Connection
2	DO	Output of Shift Register—primarily used for cascading
19	OD	Output Disable
1	V_{BB}	Q Output Drive Voltage
21	CLK	System Clock Input
40	V_{DD}	Logic Supply Voltage
22	STR	Strobe to Latch Data from Registers
39	DI	Data Input to Shift Register
3-18 and 23-38	Q_1-Q_{32}	Direct Drive Outputs

Signal Timing Diagrams



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S4534

10 BIT, HIGH VOLTAGE, HIGH CURRENT DRIVER

CONSUMER

Features:

- ☐ Outputs Capable of 60 Volt Swings at 25mA
- ☐ Drives Up to 10 Devices
- ☐ Cascadable
- ☐ Requires Only 4 Control Lines

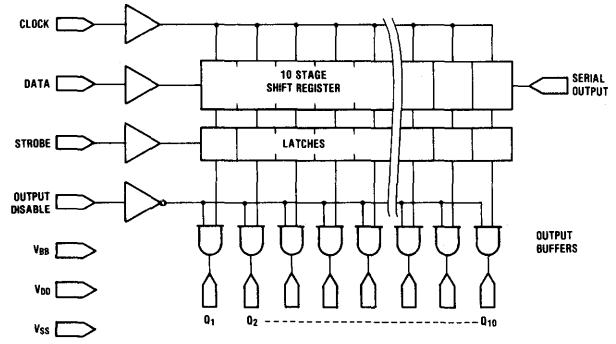
Applications:

- ☐ Vacuum Fluorescent Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

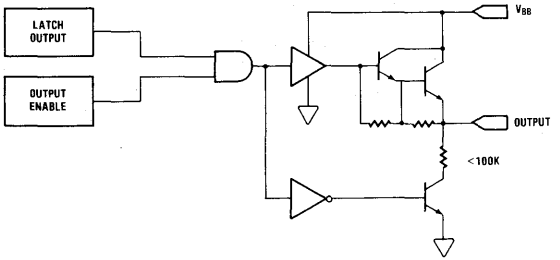
General Description

The AMI S4534 is a high voltage, high current MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control, by converting low level signals such as TTL, and CMOS to high voltage, high current drive signals. This device requires only four control lines due to its serial input construction. It latches the data to be output, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations of a 60 volt swing and up to 50mA per drive. It is especially well suited to drive vacuum fluorescent displays due to its high voltage output capability. One circuit will drive up to 10 devices and more can be driven by cascading several drivers together.

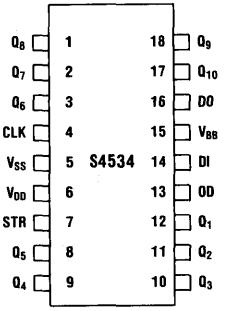
Functional Block Diagram



Output Buffer (Functional Diagram)



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{BB}	65V
V_{DD}	15V
V_{IN}	$V_{SS}-.3V$ to $V_{DD}+.3V$
V_{OUT} (Logic)	$V_{SS}-.3V$ to $V_{DD}+.3V$
V_{OUT} (Display)	$V_{SS}-.3V$ to $V_{BB}+.3V$
Power Dissipation	2W
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C

Operational Specification: $0°C \leqslant T_A \leqslant 70°C$ (unless otherwise noted)

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{IL}	Input Zero Level	−0.3	0.8	V	
V_{IH}	Input One Level	3.5	$V_{DD}+0.3$	V	
I_{IN}	Input Leakage Current		1.0	μA	$V_{DD}=5V$
V_{SL}	Signal Out Zero Level	V_{SS}	0.7	V	$I_{SO}=-20\mu A$
V_{SH}	Signal Out One Level	3.6	V_{DD}	V	$I_{SO}=20\mu A$
V_{DD}	Logic Voltage Supply	4.5	12	V	
V_{BB}	Display Voltage Supply	20	60	V	
I_{DD}	Logic Supply Current		20 30	mA mA	No Loads, $V_{DD}=5V$ No Loads, $V_{DD}=10V$
I_{BB}	Display Supply Current		6	mA	No Loads, T=25°C
V_{OL}	Output Zero Level	V_{SS}	1.0	V	$I_O=-20\mu A$
V_{OH}	Output One Level	$V_{BB}-2.5$	V_{BB}	V	$I_O=25mA$
t_{SD}	Serial Out Prop. Delay		375	ns	$C_L=50pF$
t_{PD}	Parallel Out Prop. Delay		5	μs	$C_L=50pF$
t_W	Input Pulse Width	375		ns	
t_{SU}	Data Set-Up Time	150		ns	
t_H	Data Hold Time	40		ns	

Functional Description

Serial data present at the input is transferred to the shift register on the Logic "0" to Logic "1" transition of the clock input signal. On succeeding clock pulses, the registers shift data information towards the serial data output. The input serial data must be presented prior to the rising edge of the clock input waveform.

Information present at any register is transferred to its respective latch when the strobe signal is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the strobe signal is held high.

When the output disable input is high, all of the high voltage buffers are disabled without affecting the information stored in the latches or shift register. With the output disable signal low, the high voltage outputs are controlled by the state of the latches.

Table 1.

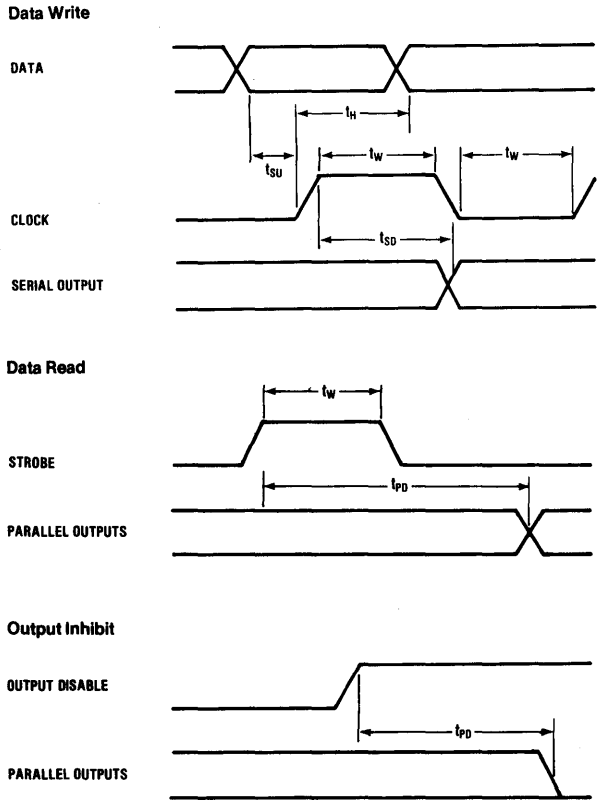
NUMBER OF OUTPUTS ON (I_{OUT} = 25mA)	MAX. ALLOWABLE DUTY CYCLE AT AMBIENT TEMPERATURE OF				
	25°C	40°C	50°C	60°C	70°C
10	100%	97%	85%	73%	62%
9		100%	94%	82%	69%
8			100%	92%	78%
7				100%	89%
6					100%
1	100%	100%	100%	100%	100%

Pin Description

Pin #	Name	Description
5	V_{SS}	Ground Connection
16	DO	Output of Shift Register—primarily used in cascading
13	OD	Output Disable
15	V_{BB}	Q Output Drive Voltage
4	CLK	System Clock Input
6	V_{DD}	Logic Supply Voltage
7	STR	Strobe to Latch Data from Registers
14	DI	Data Input to Shift Register
1-3, 8-12, 17-18	Q_1-Q_{10}	Direct Drive Outputs

CONSUMER

Signal Timing Diagrams



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S4521

32 BIT DRIVER

Features:

- ☐ Drives Up to 32 Devices
- ☐ Cascadable
- ☐ On Chip Oscillator
- ☐ Requires Only 3 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - High Noise Immunity
  - Wide Temperature Range

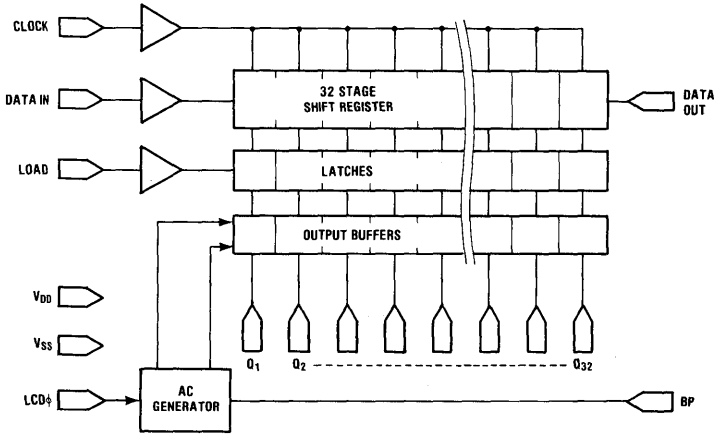
Applications:

- ☐ Liquid Crystal Displays
- ☐ LED and Incandescent Displays
- ☐ Solenoids
- ☐ Print Head Drives
- ☐ DC and Stepping Motors
- ☐ Relays

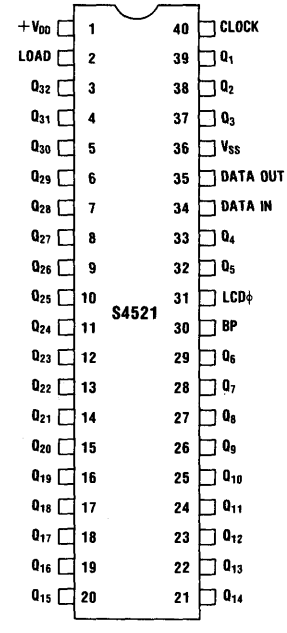
General Description

The AMI S4521 is a MOS/LSI circuit that drives a variety of output devices, usually under microprocessor control. This device requires only three control lines due to its serial input construction. It latches the data to be output, relieving the microprocessor from the task of generating the required waveform, or it may be used to bring data directly to the driver. The part acts as a versatile peripheral to drive displays, motors, relays and solenoids within its output limitations. It is especially well suited to drive liquid crystal displays as a backplane A.C. signal option is provided. The A.C. frequency of the backplane output can be user supplied or generated by attaching a capacitor to the LCDϕ input, which controls the frequency of the internal oscillator. One circuit will drive up to 32 devices and more can be driven by cascading several drivers together.

Functional Block Diagram



Pin Configuration



Absolute Maximum Ratings at 25°C

V_{DD}	−0.3 to +17V
Inputs (CLK, DATA IN, LOAD, LCDϕ)	V_{SS}−0.3 to V_{DD}+0.3V
Power Dissipation	250mW
Storage Temperature	−65 to +125°C
Operating Temperature	0°C to +70°C

Electrical Characteristics: V_{DD}=5V unless otherwise noted

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{DD}	Supply Voltage	3	15	V	
	Supply Current				
I_{DD1}	Operating		150	μA	f_{BP} = 120Hz, No Load
I_{DD2}	Quiescent		100	μA	LCDϕ High or Low, f_{BP}=0 Load @ Logic 0
	Inputs (CLK, DATA IN, LOAD)				
V_{IH}	High Level	0.5 V_{DD}	V_{DD}	V	
V_{IL}	Low Level	V_{SS}	0.2 V_{DD}	V	
I_L	Input Current		5	μA	
C_I	Input Capacitance		5	pF	
f_{CLK}	CLK Rate	DC	2	MHz	50% Duty Cycle
t_{DS}	Data Set-Up Time	100		ns	Data Change to CLK Falling Edge
t_{DH}	Data Hold Time	10		ns	
t_{PW}	Load Pulse Width	200		ns	
t_{PD}	Data Out Prop. Delay		220	ns	C_L=30pF, From Rising CLK Edge
t_{LC}	Load Pulse Set-Up	300		ns	Falling CLK Edge to Rising Load Pulse
t_{LCD}	Load Pulse Delay	0		ns	Falling Load Pulse to Falling CLK Edge
V_{OAVG}	DC Bias (Average) Any Q Output to Backplane		±25	mV	f_{BP} = 120Hz
V_{IH}	LCDϕ Input High Level	.9 V_{DD}	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{SS}	.1 V_{DD}	V	Externally Driven
	Capacitance Loads				
C_{LQ}	Q Output		50,000	pF	f_{BP} = 120Hz
C_{LBP}	Backplane		1.5	μF	f_{BP} = 120Hz, See Note 8
R_{ON}	Q Output Impedance		2.0	KΩ	I_L = 10μA
R_{ON}	Backplane Output Impedance		100	Ω	I_L=10μA
R_{ON}	Data Out Output Impedance		2.0	KΩ	I_L=10μA

CONSUMER

Operating Notes

1. The shift register loads and shifts on the falling edge of CLK. It outputs on the rising edge of the CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q10 was input 10 clock pulses earlier).
3. A logic 1 on Data In causes a Q output to be out of phase with the Backplane.
4. A logic 1 on Load causes a parallel load of the data in the shift register into the latches that control the Q output drivers.
5. To cascade units, (a) connect the Data Out of one chip to Data In of next chip, and (b) either connect Backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) or connect LCDϕ of all chips to a common driving signal. If the former is chosen, the Backplane that is tied to the LCDϕ inputs of the other chips should *not* also be connected to the Backplanes of those chips.
6. If LCDϕ is driven it is in phase with the Backplane output.
7. The LCDϕ pin can be used in two modes, driven or oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external resistor and capacitor. The Backplane frequency is a divide by 256 of the LCDϕ frequency in the oscillating mode.
8. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(mHz) = 0.2 \div C(in\ \mu F)$
9. If the total display capacitance is greater than 100,000 pF, a decoupling capacitor of 1μF is required across the power supply (pins 1 and 36).

Pin Description

Pin #	Name	Description
1	V_{DD}	Logic and Q Output Supply Voltage
2	LOAD	Signal to Latch Data from Registers
30	BP	Backplane Drive Output
31	LCDϕ	Backplane Drive Input
34	DATA IN	Data Input to Shift Register
35	DATA OUT	Data Output from Shift Register-primarily used in cascading
36	V_{SS}	Ground Connection
40	CLOCK	System Clock Input
3-29, 32-33, 37-39	Q_1-Q_{32}	Direct Drive Outputs

AMERICAN MICROSYSTEMS, INC.

S4036

GENERAL PURPOSE A/D CONVERTER AND DIGITAL SCALE CIRCUIT

Features:

- On-Chip Voltage Regulator
- On-Chip Low Supply Detection
- On-Chip LED Display Drivers
- Pin Selectable Sensitivity
- Linearity ± 5 LSB/3000 Bits
- Repeatability ± 3 LSB/3000 Bits

Applications:

- Low Cost ADC
- Digital Scale
- Digital Thermometer
- Digital Voltmeter
- Digital Light Meter

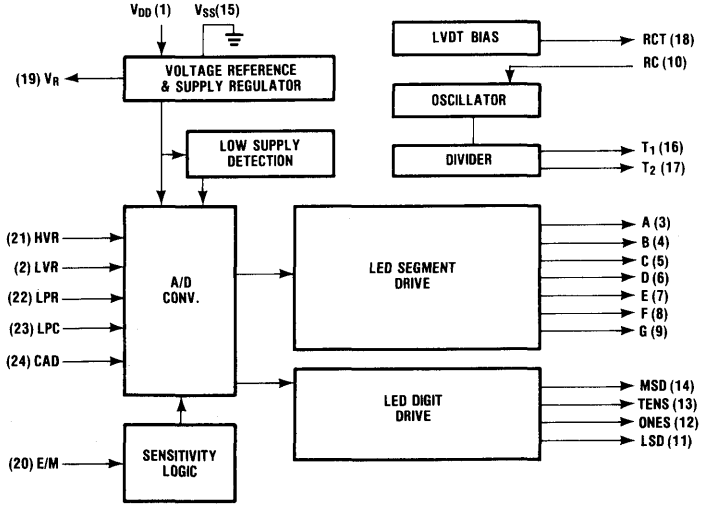
General Description

The S4036 General Purpose A/D Converter and Digital Scale Circuit provides a one chip solution to many Analog/Digital applications. Few external parts are needed as the S4036 provides an on-chip voltage reference, low supply detector, pin selectable sensitivity logic, and drivers for a multiplexed LED display.

The S4036 can begin to process analog data immediately upon presentation, or it can wait to sample the data after two seconds of settling time at user discretion.

In the sampled data mode of operation, a short pulse applied to the V_{DD} input signals the S4036 to start the sample interval counter. The display clears to "000," with the most significant digit blanked. After two seconds, approximately, the S4036 begins to process the analog input. The display "rolls-up" from "000" to the digital value of the analog input. This "roll-up" process takes one second. The value on the display at the end of the conversion is held fixed until the V_{DD} line is pulsed to restart the process.

Block Diagram



Pin Configuration

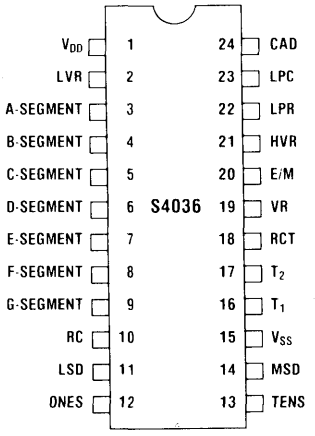


Figure 1. Typical ADC Application

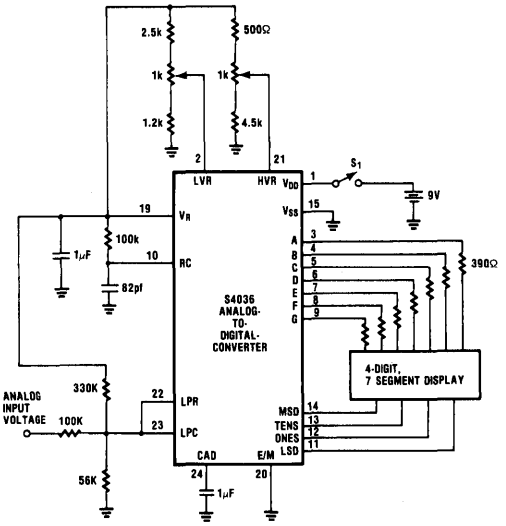
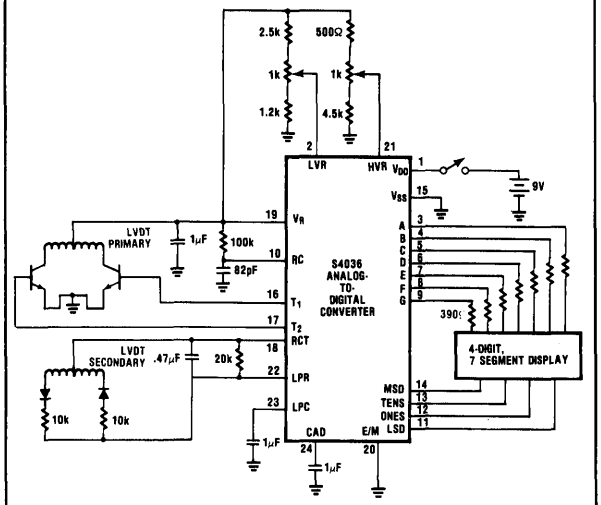


Figure 2. Typical Digital Scale Application



Here, a switch (S_1) pulses the V_{DD} input of the S4036 to begin the conversion process. When the analog voltage is more positive than the LVR voltage level, a non-zero reading will occur. If the analog voltage is more negative than the LVR level (underflow), a zero value reading will occur. If the analog voltage is more positive than the HVR voltage level (overflow), the S4036 will output a maximum value reading (2999 or 1360, depending on state of Pin 20). LVR is 1.5V to 2.5V, HVR is 4.5V to 5.5V.

The analog voltage is applied to Pins 22 and 23. Pins 16 (T_1), 17 (T_2), and 18 (RCT) are not connected. Notice the 390Ω resistors off Pins 3-9; these are used to limit the output current of the S4036.

A feature which can be user-programmed is the HVR and LVR voltages used by the ADC. The chip supplies a regulated voltage (Pin 19) which can be divided down and picked off via a potentiometer. Thus, the user can specify the lower reference ("0" value display point) and the upper reference (maximum value display point) merely by resistively dividing the regulated voltage output. This feature allows the S4036 to perform in many "non-standard" ADC situations.

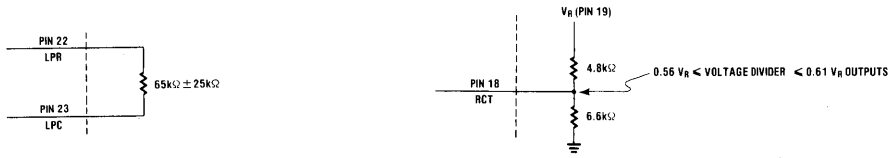
A capacitor is required on Pin 24 to implement the Analog-to-Digital Converter. For most applications, the value of this capacitor is nominally 1μF, but this value is not critical to the conversion process.

Here, a mechanical input from the scale pulses the V_{DD} input of the S4036 to begin the conversion process. The same mechanical input from the scale also displaces the core of the Linear Variable Differential Transformer (LVDT) proportional to the weight of the object being measured. The LVDT primary is driven by 2NPN transistors controlled by S4036 timing outputs T_1 and T_2, which are 180° out of phase at a 50% duty cycle. The output (RCT) is used to bias the center tap of the LVDT secondary. The LVDT secondary presents an output which varies linearly with core position. This voltage is rectified, filtered, and presented to the analog inputs (LPR and LPC). (See Figure 3 for internal connection of S4036 pins RCT, LPR, and LPC.)

The S4036 has two pin-selectable modes of sensitivity. A Logic "0" on Pin 20 allows 3000 possible readings (0 to 2999), while a Logic "1" on Pin 20 allows 1361 possible readings (0 to 1360). This feature allows the sensitivity of the S4036 to be adapted to meet a wide range of ADC applications. In most digital scale applications, the pin-selectable sensitivity of the S4036 can be used to provide pounds (3000 readings) or kilograms (1361 readings) by providing a Logic "0" or "1" on Pin 20, respectively.

The chip also contains an RC oscillator amplifier which interfaces with an external resistor and capacitor to provide the timing for the Analog-to Digital Converter and multiplexed LED display drivers.

Figure 3. Internal Connection of S4036 Pins RCT, LPR, & LPC



Absolute Maximum Ratings

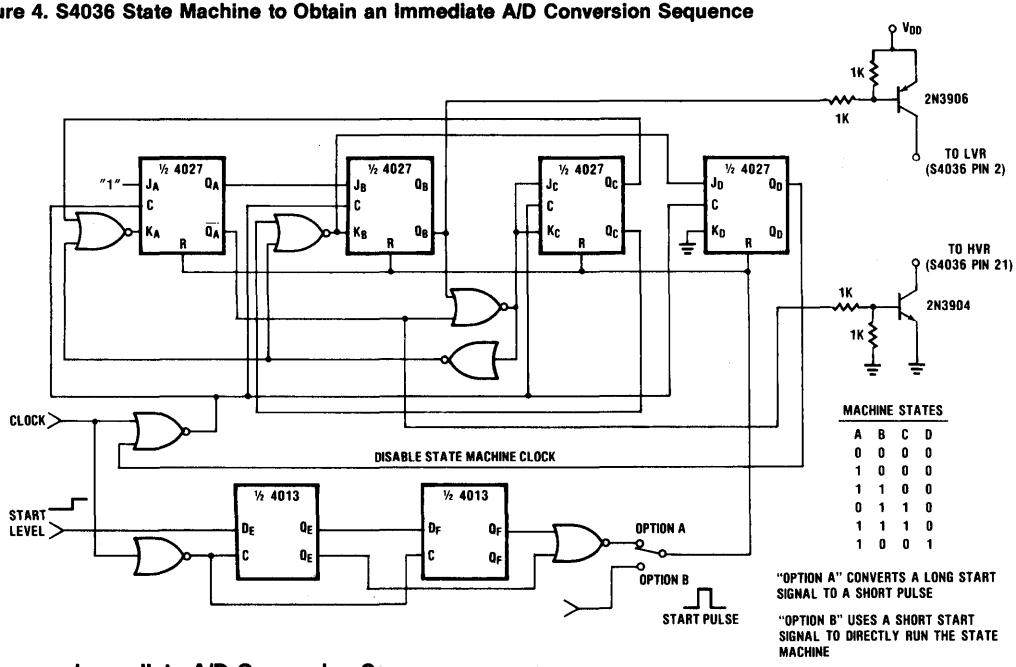
Voltage at Any Pin ..... V_{SS} −0.3V to V_{DD} +0.3V
Storage Temperature Range ..... −65°C to +150°C
DC Supply Voltage ..... 12 VDC
Power Dissipation (25°C) 1000mW
Safe Operation Temperature Range ..... 0°C to 50°C
Lead Temperature (During Soldering) ..... 300°C for Max. 10 Sec.

CONSUMER

Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
T_{ACC}	Accurate Operation Temperature Range	10	—	35	°C	
V_{DD}	Operating Supply Voltage	V_{LS}	—	9.50	VDC	
f_{OSC}	Oscillator Frequency	91	104	117	KHz	R=100K, C=82pF
I_{DD}	Operating Supply Current	—	—	12	mA	Outputs Unloaded
t_{SAM}	2 Sec Data Sample Time	2.24	2.52	2.88	Sec	
t_{ADC}	ADC Calculation Internal	0.82	0.92	1.05	Sec	
f_{DISP}	Display MUX Frequency	355	406	457	Hz	
% MUX	Each Digit Minimum MUX Duty Cycle	20			%	
V_R	Regulated Voltage	5.5	6.00	6.5	V	Into 242 Ohm
V_{SEG}	V_{OUT}, Segment Drivers	7.2	—	—	V	Into 720 Ohm
V_{DIGIT}	V_{OUT}, Digit Drivers	—	—	1.2	V	From 91 Ohm
V_{LS}	Low Supply Detection & A/D Shutdown	6.3	—	7.3	V	
LVR	Low Voltage Reference	1.5	—	2.5	V	
HVR	High Voltage Reference	4.5	—	5.5	V	
f_{LVDT}	T_1 and T_2 Freq.	11	13	15	KHz	
V_{LVDT}	T_1 and T_2 Output Voltages @ V_{DD}=8V	—	—	1	V	From 70K Ohm
		0.75	—	—	V	Into 1500 Ohm
	Linearity from Best Straight Line, V_{DD}=8V			±5	Bits	2.3V ≤ LPR ≤ 4.7V LVR=2V, HVR=5V
	Reading Change Over Range of V_{DD}			±5	Bits	7.3V ≤ V_{DD} ≤ 9.0V, LVR=2V, HVR=5V, LPR=3.5V
	Display Change Over Consecutive Readings			±3	Bits	V_{DD}=8V, LVR=2V, HVR=5V, LPR=3.5V

Figure 4. S4036 State Machine to Obtain an Immediate A/D Conversion Sequence



Immediate A/D Conversion Sequence

This sequence eliminates the analog data sample time, resets the S4036, and then proceeds directly with Analog-to-Digital conversion. This approach should be used for data which is steady when the S4036 is signaled to begin processing. It may be exercised by presenting the following logic series to LVR (Pin 2) and HVR (Pin 21):

Sequence Step	LVR	HVR
1	0	1
2	0	0
3	0	1
4	1	1
5	1	0
6	1	1
7	0	1

At the end of the signal sequence, the S4036 will sample the analog data input and "roll-up" the display to the digital value of the analog input. The sequence frequency should be greater than the oscillator frequency.

Logic "0": LVR $\leq$ 2.5V, HVR $\leq$ 1.0V

Logic "1": LVR $\geq V_{DD} - 1.0V$, HVR $\geq$ 4.5V

S4036 02 PRINTED IN USA 5M

CMOS GATE ARRAYS

Features

- ☐ **Arrays of Uncommitted CMOS Transistors Programmed by Metal Layer Interconnect to Implement Arbitrary Digital Logic Functions**
- ☐ **Multiple Developmental Interfaces: AMI or Customer Designed**
- ☐ **Two Array Families — 5-Micron and 3-Micron Versions**
- ☐ **Multiple Array Configurations—From 300 to 1260 Gates for 5-Micron Devices, and 500 to 5000 Gates for 3-Micron Devices**
- ☐ **Quick Turn Prototypes and Short Production Turn-On Time**
- ☐ **Economical Semi-Custom Approach for Low-to-Medium Production Volume Requirements**
- ☐ **Advanced Oxide-Isolated Silicon Gate CMOS Technology**
- ☐ **High Performance—2 to 3 ns Typical Gate Delay for 3-Micron Devices**
- ☐ **Broad Power Supply Range—3V to 12V (±10%)**
- ☐ **TTL or CMOS Compatible I/O**
- ☐ **Up to 134 I/O Connections**
- ☐ **Numerous Package Options**
- ☐ **Full Military Temperature Range (−55°C to 125°C) and MIL-STD-883 Class B Screening Available**

General Description

AMI's Gate Array products consist of arrays of CMOS devices whose interconnections are initially unspecified. By "programming" interconnect at the metal layer mask level, virtually arbitrary configurations of digital logic can be realized in an LSI implementation.

AMI gate array designs are based on topological cells—i.e., groups of uncommitted silicon-gate N-channel and P-channel transistors—that are placed at regular intervals along the X and Y axes of the chip with intervening polysilicon underpasses. Pads, input protection circuitry, and uncommitted output drivers are placed around the periphery.

Compared to SSI/MSI logic implementations, AMI's gate array approach offers lower system cost and, in addition, all the benefits of CMOS LSI. The lower system cost is due to significant reductions in component count, board area and power consumption. Product reliability, a strong function of component count, is thereby greatly enhanced. And compared to fully custom LSI circuits, the gate array offers several advantages: low development cost; shorter development time; shorter production turn-on time; and low unit costs for small to moderate production volumes.

AMI's CMOS gate arrays are offered in two families: the 5-micron UA series and the 3-micron GA series. The 5-micron UA series has been in production since 1980 and proven over hundreds of circuits. The 3-micron GA series is the high-speed high-density devices fabricated in AMI's state-of-the-art 3-micron CMOS processes.

Table 1. Five-Micron Gate Array Family

Circuit	Equivalent Two-Input Gates	Pads	LS Output Drivers	TTL Output Drivers
UA-1	300	40	17	20
UA-2	400	46	23	20
UA-3	540	52	25	24
UA-4	770	62	31	28
UA-5	1000	70	35	32
UA-6	1260	78	39	36

Five-Micron Gate Array Family

The family of 5-micron CMOS products is offered in six configurations, summarized in Table l, with circuit complexities equivalent to 300, 400, 540, 770, 1000, and 1260 two-input gates, respectively. All pads can be individually configured as inputs, outputs, or I/O's. Input switching characteristics can be programmed for either CMOS or TTL compatibility. LS buffer output drivers will support CMOS levels or two low power schottky TTL loads. TTL buffer outputs will also provide CMOS levels and are capable of driving up to six LS TTL loads. All output drivers can be programmed for tri-state or open drain (open collector) operation as required.

The CMOS technology used for these products is AMI's state-of-the-art 5-micron, oxide-isolated, silicon gate CMOS process. This process offers all the conventional advantages of CMOS—i.e., very low power consumption, broad power supply voltage range (3V to 12V ±10%), and high noise immunity—as well as dense circuits with high performance. Gate propagation delays are in the five to ten ns range for 5 volt operation at room temperature. AMI gate array products can be supplied in versions intended for operation over the standard commercial temperature range (0°C to +70°C), the industrial range (−40°C to +85°C), or the full military range (−55°C to +125°C). MIL-STD-883 Class B screening, including internal visual inspection and high temperature burn-in, is offered. Similarly, customer-specified high reliability screening is available for commercial and industrial applications.

The current AMI array family, 300 gates to 1260 gates, is run in a 3-12V CMOS process (internally coded CVA). AMI is currently optimizing this array family for 3V to 5V operation (internally coded as CVH process). This new family, tentatively called UA-300 through UA-1260, will be functionally identical to the existing UA-1 through UA-6. All design tools will be identical. In fact, all customer patterns for the two families will be interchangeable.

Customers who require 3V to 5V operation will be able to use the CVH family starting in early 1982. This optimized process will result in a 25-50% performance enhancement for 5V gate array designs. Customers who require operating voltages greater than 5V will continue to use the UA-1 to UA-6 CVA family.

In conjunction with these arrays, AMI has developed a set of "functional overlays." These are basic logic element building blocks—e.g. two input and larger gates of various types, flip-flops, and so forth—from which complete logic designs can be developed. Each functional overlay corresponds to a metal interconnect pattern that is superimposed on a set of uncommitted transistors (and polysilicon underpasses) in the array to implement the the logic element. Typical functional overlay logic elements and the number of two-input gate equivalents they utilize are shown in Table 2.

Table 2

Logic Element	2-Input Gate Equivalent
2-Input NOR	1
2-Input NAND	1
3-Input NOR	1.5
3-Input NAND	1.5
INVERTER	.5
D FLIP-FLOP W/RESET	5
D FLIP-FLOP W/SET-RESET	6
J-K FLIP-FLOP	8
CLOCKED LATCH	2.5
EXCLUSIVE OR	2.5
SCHMITT TRIGGER	2
4-BIT BCD CNTR W/RESET	27
TRANSMISSION GATE	.5

Three-Micron Gate Array Family

As part of AMI's long range semi-custom strategy in MOS/VLSI, AMI will continue to introduce new gate array products. These new products will offer performance and cost advantages not currently realizable. In conjunction with these new array products, AMI will introduce computer-aided design tools to automate the entire gate array design process.

The newest gate array family is the high-performance GA series which is based on AMI's 3-micron CMOS silicon gate process technology. With a 3-micron drawn geometry, it is equivalent to a 2-micron effective channel length which is the state-of-the-art.

The AMI GA series is designed for 5V operation over military temperature range (−55 to 125°C). Besides high speed (2 to 3 ns typical delay) and high density (up to 5K gates), it features total I/O flexibility in that each I/O pad can be one of any 13 options.

The GA series is available in two versions: single metal and double metal. The single metal version provides up to 2500 gates and the double metal version 5000 gates. See Table 3 for configurations.

In conjunction with these new array products, AMI will have a complete powerful set of design automation software to allow users complete design flexibility. Using a terminal tied to a central AMI owned or customer owned minicomputer or mainframe, the user will have access to a complete set of design automation software tools including:

- ☐ Schematic digitization and capture
- ☐ Logic simulation
- ☐ Circuit simulation
- ☐ Test vector generation
- ☐ Interactive or autoplace and route
- ☐ Auto continuity checking

These tools will allow the user to partially or fully automate the design task for maximum flexibility. In addition, AMI will introduce a complete 16-bit microprocessor based design automation system in conjunction with the double metal family. This product will utilize the identical software tools available on the timeshared mini or mainframe.

Table 3. Three-Micron Gate Array Family

Process	Product No.	Gates	Pads
Single Metal	GA-2500	2500	84
	GA-2000	2025	74
	GA-1500	1500	64
	GA-1000	1020	52
	GA-500	500	36
Double Metal	GA-5000D	5000	134
	GA-4000D	4000	120
	GA-3000D	3000	84
	GA-2000D	2000	74

Customer Interface

AMI can interface with a user at one of three input levels: logic, layout or PG tape. At the logic level, AMI will customize and develop the metal interconnect pattern from the user's logic diagram. This is known as the AMI-Designed interface.

For programs involving multiple gate array patterns from customers with suitable MOS design and layout experience, AMI will also support arrangements in which the customer designs the metal interconnect patterns and furnishes AMI with corresponding composite layout or metal mask PG tapes to AMI specification. This is known as the Customer-Designed Interface. To support this interface, AMI will provide the users with the CAD package plus training.

Packages

Pinout or lead count varies with die size and array complexity. The arrays are offered in standard plastic and ceramic dual-in-line packages with pin counts ranging from 16 to 64, and in JEDEC-Standard leadless chip carriers. AMI gate array products are also available in wafer or unpackaged die form.

5-Micron Gate Array Series

DC Characteristics—TTL Interface

Specified @ $V_{DD}=+5V \pm 10\%$; $V_{SS}=0$; Temperature $=-55°C$ to $+125°C$

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	0.0		0.8	V
V_{OH}	Output High Voltage (LS Buffer $I_{OH}=-700\mu A$) (T Buffer $I_{OH}=-1.5mA$)	2.7 2.4			V V
V_{OL}	Output Low Voltage (T Buffer $V_{OL}=2.4mA$) (LS Buffer $I_{OL}=0.8mA$)			0.4 0.4	V V
I_{OZ}	3-State Output Leakage $V_O=0$ or V_{DD}	−10	1	10	μA

DC Characteristics—CMOS Interface

Sym.	Parameter	V_{DD}	Limits							Units	Condition
			*T Low		25°C			*T High			
			Min	Max	Min	Typ	Max	Min	Max		
I_{DD}	Quiescent Device Current	5V 10V		0.1 0.2		.001 .002	0.1 0.2		1 2	μA/gate μA/gate	$V_{IN}=0$ or V_{DD}
V_{OL}	Low Level Output Voltage			0.05			0.05		0.05	V	$I_O=1\mu A$
V_{OH}	High Level Output Voltage	5V 10V	4.95 9.95		4.95 9.95			4.95 9.95		V V	$I_O=-1\mu A$
V_{IL}	Input Low Voltage	5V 10V	0.0 0.0	1.5 3.0	0.0 0.0		1.5 3.0	0.0 0.0	1.5 3.0	V V	
V_{IH}	Input High Voltage	5V 10V	3.5 7.0	5.0 10.0	3.5 7.0		5.0 10.0	3.5 7.0	5.0 10.0	V V	
I_{OL}	Output Low (Sink) Current T Buffer	5V 10V	3.2 6.0		3.2 6.0	4.8 9.0		2.4 4.0		mA mA	$V_O=0.4V$ $V_O=0.5V$
	LS Buffer	5V 10V	1.0 1.8		1.0 1.8	1.6 3.1		0.8 1.0		mA mA	$V_O=0.4V$ $V_O=0.5V$
I_{OH}	Output High (Source) Current T Buffer	5V 10V		−600 −1120			−600 −1120		−500 −940	μA μA	$V_O=4.6V$ $V_O=9.5V$
	LS Buffer	5V 10V		−300 −560			−300 −560		−250 −470	μA μA	$V_O=4.6V$ $V_O=9.5V$
I_{IN}	Input Leakage Current			1			1		1	μA	$V_{IN}=0$ or V_{DD}
I_{OZ}	3 State Output Leakage Current			±1			±1		±10	μA	$V_O=0$ or V_{DD}
C_I	Input Capacitance					5				pF	Any Input

*Military temperature range is −55°C to +125°C
Industrial temperature range is −40°C to +85°C
Commercial temperature range is 0°C to +70°C

AMERICAN MICROSYSTEMS, INC.

S6800

Microprocessor Component Family

Contact factory for complete data sheet

MICROPROCESSORS

S6800/S68A00/S68B00	8-Bit Microprocessor (1.0/1.5/2.0MHz Clock)
S6801/S6801E	Single Chip Microcomputer 2K ROM, 128×8 RAM, 31 I/O Lines, Enhanced Instruction Set (External [E] or Internal Clock)
S6802/A/B/S6808/A/B	Microprocessor with Clock and RAM (1.0/1.5/2.0MHz Clock) (S6808 Models—No RAM)
S6803/S6803N/R	S6801 Without ROM (N/R Model — No ROM and RAM)
S6805	Single Chip Microcomputer 1,152×8 ROM, 64×8 RAM, Timer, Pre-scaler, Bit Level Instructions.
S6809(E)/S68A09(E)/S68B09(E)	Pseudo 16-Bit Microprocessor (1.0/1.5/2.0MHz Clock) (E Models — External Clock Mode)

PERIPHERALS

S1602	Universal Asynchronous Receiver/Transmitter (UART)
S2350	Universal Synchronous Receiver/Transmitter (USRT)
S6551/S68051	UART With Baud Rate Generator
S6821/S68A21/S68B21	Peripheral Interface Adapter (PIA)(1.0/1.5/2.0MHz Clock)
S6840/S68A40/S68B40	Programmable Timer (1.0/1.5/2.0MHz)
S68045	CRT Controller (CRTC)
S6846	2K ROM, Parallel I/O, Programmable Timer
S6850/S68A50/S68B50	Asynchronous Communication Interface Adapter (ACIA)
S6852/S68A52/S68B52	Synchronous Serial Data Adapter (SSDA) (1.0/1.5/2.0MHz Clock)
S6854/S68A54/S68B54	Advanced Data Link Controller (ADLC) (1.0/1.5/2.0MHz Clock)
S68488	IEEE — 488 Bus Interface
S2811	Signal Processing Peripheral
S2814A	Fast Fourier Transformer
S2815	Digital Filter/Utility Peripheral
S2816	Echo Cancellor Processor

MEMORIES

S6810/S68A10/S68B10	128×8 Static RAM (450/360/250ns Access Time)

AMERICAN MICROSYSTEMS, INC.

S6800/S68A00/S68B00

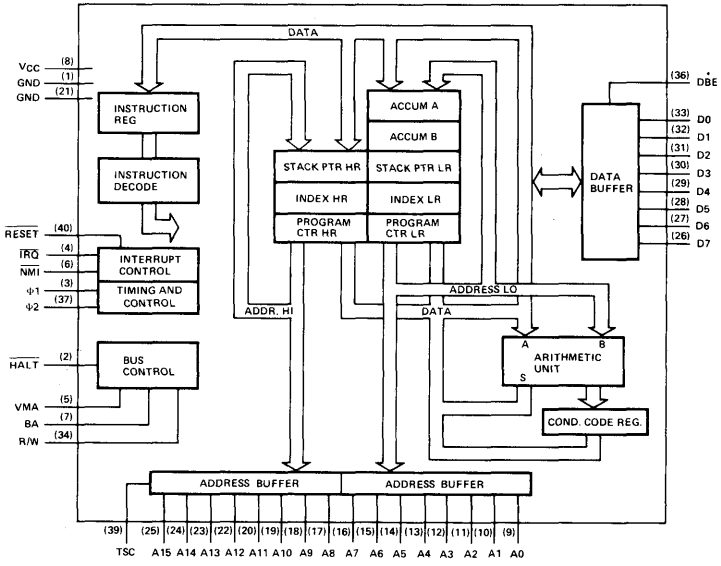
8-BIT MICROPROCESSOR

Features

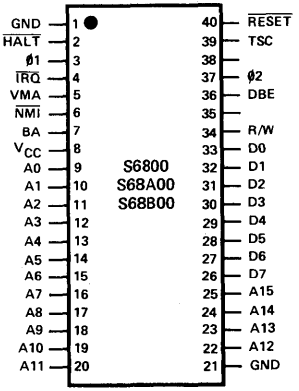
- ☐ Eight-Bit Parallel Processing
- ☐ Bi-Directional Data Bus
- ☐ Sixteen-Bit Address Bus — 65536 Bytes of Addressing
- ☐ 72 Instructions — Variable Length
- ☐ Seven Addressing Modes — Direct, Relative Immediate, Indexed, Extended, Implied and Accumulator
- ☐ Variable Length Stack
- ☐ Vectored Restart
- ☐ 2 Microsecond Instruction Execution
- ☐ Maskable Interrupt Vector
- ☐ Separate Non-Maskable Interrupt — Internal Registers Saved in Stack
- ☐ Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- ☐ Direct Memory Access (DMA) and Multiple Processor Capability
- ☐ Clock Rates — S6800 — 1.0MHz
  — S68A00 — 1.5MHz
  — S68B00 — 2.0MHz
- ☐ Simple Bus Interface Without TTL
- ☐ Halt and Single Instruction Execution Capability

S6800

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

Electrical Characteristics

(V_{CC} = 5.0V, ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Symbol	Characteristics		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage (Normal Operating Levels)	Logic	V_{SS} +2.0	—	V_{CC}	Vdc
V_{IHC}		$\phi1, \phi2$	V_{CC} −0.6	—	V_{CC} +0.3	
V_{IL}	Input Low Voltage (Normal Operating Levels)	Logic	V_{SS} −0.3	—	V_{SS} +0.8	Vdc
V_{ILC}		$\phi1, \phi2$	V_{SS} −0.3	—	V_{SS} +0.4	
I_{IN}	Input Leakage Current					μAdc
	(V_{IN} = 0 to 5.25V, V_{CC} = Max)	Logic*	—	1.0	2.5	
	(V_{IN} = 0 to 5.25V, V_{CC} = 0.0V)	$\phi1, \phi2$	—	—	100	
I_{TSI}	Three-State (Off State) Input Current	D0 — D7	—	2.0	10	μAdc
	V_{IN} = 0.4 to 2.4V, V_{CC} = Max	A0 — A15, R/W	—	—	100	
V_{OH}	Output High Voltage					Vdc
	(I_{LOAD} = 205μAdc, V_{CC} = Min)	D0 — D7	V_{SS} +2.4	—	—	
	(I_{LOAD} = 145μAdc, V_{CC} = Min)	A0 — A15, R/W, VMA	V_{SS} +2.4	—	—	
	(I_{LOAD} = −100μAdc, V_{CC} = Min)	BA	V_{SS} +2.4			
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = Min)		—	—	V_{SS} +0.4	Vdc
P_D	Power Dissipation		—	0.5	1.0	W
C_{IN}	Capacitance#					pF
	(V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	$\phi1$	—	—	35	
		$\phi2$	—	—	70	
		D0 — D7	—	10	12.5	
		Logic Inputs	—	6.5	10	
C_{OUT}		A0 — A15, R/W, VMA	—	—	12	pF
f	Frequency of Operation	S6800	0.1	—	1.0	MHz
		S68A00	0.1	—	1.5	
		S68B00	0.1	—	2.0	
	Clock Timing (Figure 1)	S6800	1.000	—	10	
t_{CYC}	Cycle Time	S68A00	0.666	—	10	μs
		S68B00	0.50	—	10	
	Clock Pulse Width	$\phi1, \phi2$ — S6800	400	—	9500	ns
$PW_{\phi H}$	Measured at V_{CC} −0.6V	$\phi1, \phi2$ — S68A00	230	—	9500	ns
		$\phi1, \phi2$ — S68B00	180	—	9500	
		S6800	900	—	—	ns
t_{UT}	Total $\phi1$ and $\phi2$ Up Time	S68A00	600	—	—	
		S68B00	440	—	—	
$t_{\phi r}, t_{\phi f}$	Measured between V_{SS} +0.4 and V_{CC} −0.6	Rise and Fall Times		—	100	ns
t_d	Measured at V_{OV} = V_{SS} +0.6V	Delay Time or Clock Separation	0	—	9100	ns

**Except $\overline{IRQ}$ and $\overline{NMI}$, Which require KΩ pullup load resistor for wire-OR capability at optimum operation.*
#Capacitances are periodically sampled rather than 100% tested.

Read/Write Timing

Symbol	Characteristics	S6800			S68A00			S68B00			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{AD}	Address Delay										ns
	C = 90pF	—	—	270	—	—	180	—	—	150	
	C = 30pF	—	—	250	—	—	165	—	—	135	
t_{ACC}	Periph. Read Access Time $t_{AC}=t_{UT}-(t_{AD}+t_{DSR})$	530	—		360	—		250	—		ns
t_{DSR}	Data Setup Time (Read)	100	—	—	60	—	—	40	—	—	ns
t_H	Input Data Hold Time	10	—	—	10	—	—	10	—	—	ns
t_H	Output Data Hold Time	10	25	—	10	25	—	10	25	—	ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	30	50	—	30	50	—	30	50	—	ns
t_{EH}	Enable High Time for DBE Input	450	—	—	280	—	—	220	—	—	ns
t_{DDW}	Date Delay Time (Write)	—	—	225	—	165	200	—	—	160	ns
	Processor Controls										
t_{PCS}	Proc. Control Setup Time	200	—	—	140	—	—	110	—	—	ns
t_{PC_r};t_{PC_f}	Processor Control Rise and Fall Time	—	—	100	—	—	100	—	—	100	ns
t_{BA}	Bus Available Delay	—	—	250	—	—	165	—	—	135	ns
t_{TSE}	Three-State Enable	—	—	40	—	—	40	—	—	40	ns
t_{TSD}	Three-State Delay	—	—	270	—	—	270	—	—	270	ns
$t_{\overline{DBE}}$	Data Bus Enable Down Time During $\phi 1$ Up Time	150	—	—	120	—	—	75	—	—	ns
t_{DBE_r}, t_{DBE_f}	Data Bus Enable Rise and Fall Times	—	—	25	—	—	25	—	—	25	ns

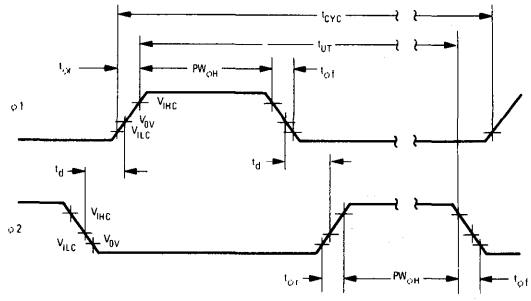


Figure 1. Clock Timing Waveform

Measurement point for $\phi 1$ and $\phi 2$ are shown below. Other measurements are the same as for MC6800.

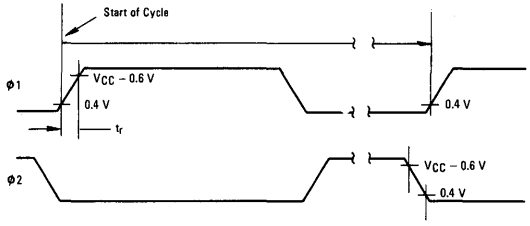


Figure 2. Read/Write Timing Waveform

Figure 3. Read Data From Memory or Peripherals

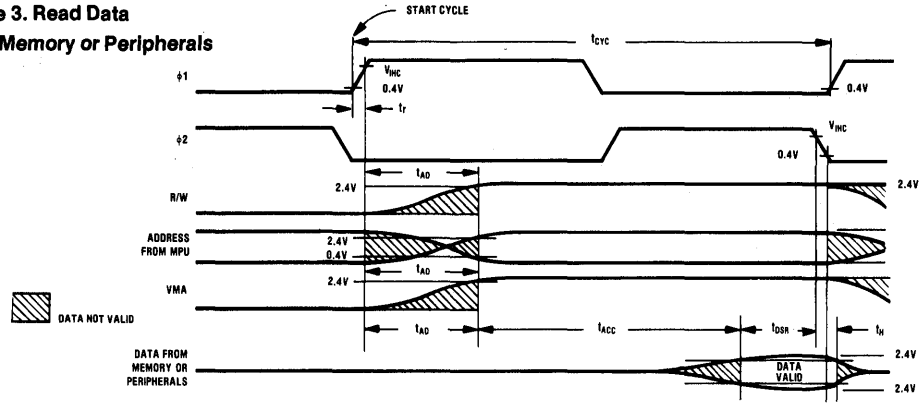
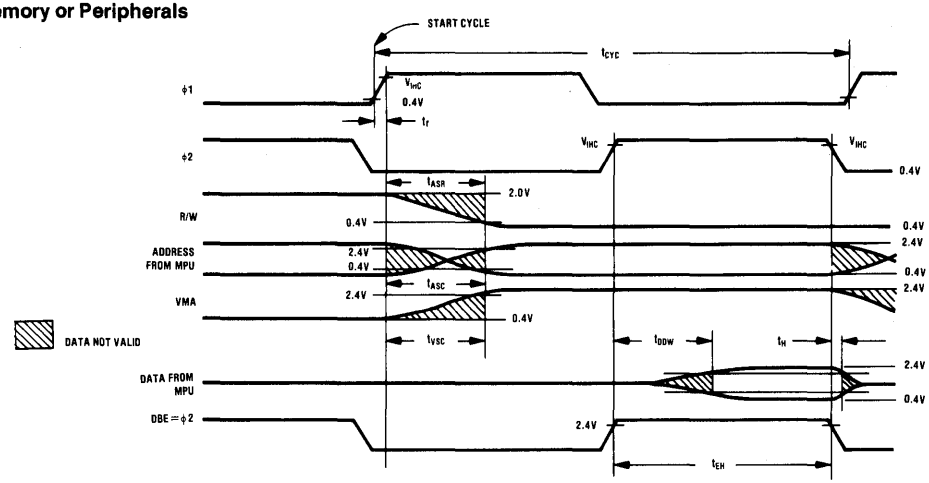


Figure 4. Write Data in Memory or Peripherals



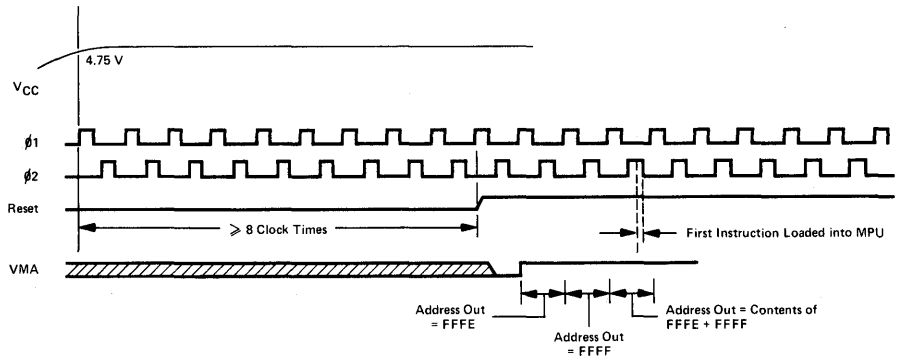


Figure 5. Initialization of MPU After Restart

Interface Description

Label	Pin	Function
ϕ1 ϕ2	(3) (37)	**Clocks Phase One and Phase Two** — Two pins are used for a two-phase non-overlapping clock that runs at the V_{CC} voltage level.
$\overline{\text{RESET}}$	(40)	**$\overline{\text{Reset}}$** — this input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. If a positive edge is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts (Figure 4). If $\overline{\text{Reset}}$ goes high prior to the leading edge of ϕ2, on the next ϕ1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.
VMA	(5)	**Valid Memory Address** — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 30pF may be directly driven by this active high signal.
A0 • • • A15	(9) (25)	**Address Bus** — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.
TSC	(39)	**Three-State Control** — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 500ns after TSC = 2.4V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The ϕ1 clock must be held in the high state and the ϕ2 in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 50μs or destruction of data will occur in the MPU.
D0 • • D7	(33) (26)	**Data Bus** — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load at 130pF.
DBE	(36)	**Data Bus Enable** — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however in normal operation, it can be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.
R/W	(34)	**Read/Write** — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this

signal is Read (high). Three-State Control going high will Read/Write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 130pF.

$\overline{HALT}$ (2) **$\overline{Halt}$** – When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction. Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three-state lines will be in the three-state mode.

Transition of the $\overline{Halt}$ line must not occur during the last 250ns of phase one. To insure single instruction operation, the $\overline{Halt}$ line must go high for one Phase One Clock cycle.

BA (7) **Bus Available** – The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{Halt}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30pF.

$\overline{IRQ}$ (4) **$\overline{Interrupt\ Request}$** – This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An adress loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{Halt}$ line must be in the high state for interrupts to be recognized.

The $\overline{IRQ}$ has a high impedance pullup device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{NMI}$ (6) **$\overline{Non\text{-}Maskable\ Interrupt}$**– A low-going edge on this input requests that a non-mask interrupt sequence be generated within the processor. As with the $\overline{Interrupt\ Request}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{NMI}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{NMI}$. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away in the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ has a high impedance pullup resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are acknowledged during $\phi 2$ and will start the interrupt routine on the $\phi 1$ following the completion of an instruction.

INTERRUPTS – As outlined in the interface description the S6800 requires a 16-bit vector address to indicate the location of routines for Restart, Non-maskable Interrupt, and Maskable Interrupt. Additionally an address is required for the Software Interrupt Instruc-

tion (SWI). The processor assumes the uppermost eight memory locations, FFF8 — FFFF, are assigned as interrupt vector addresses as defined in Figure 6.

After completing the current instruction execution the processor checks for an allowable interrupt request via the $\overline{IRQ}$ or $\overline{NMI}$ inputs as shown by the simplified flow chart in Figure 7. Recognition of either external interrupt request or a Wait for Interrupt (WAI) or Software Interrupt (SWI) instruction causes the contents of the Index Register, Program Counter, Accumulators and Condition Code Register to be transferred to the stack as shown in Figure 8.

VECTOR		DESCRIPTION
MS	LS	
FFFE	FFFF	RESTART
FFFC	FFFD	NON-MASKABLE INTERRUPT
FFFA	FFFB	SOFTWARE INTERRUPT
FFF8	FFF9	INTERRUPT REQUEST

Figure 6. Memory Map For Interrupt Vectors

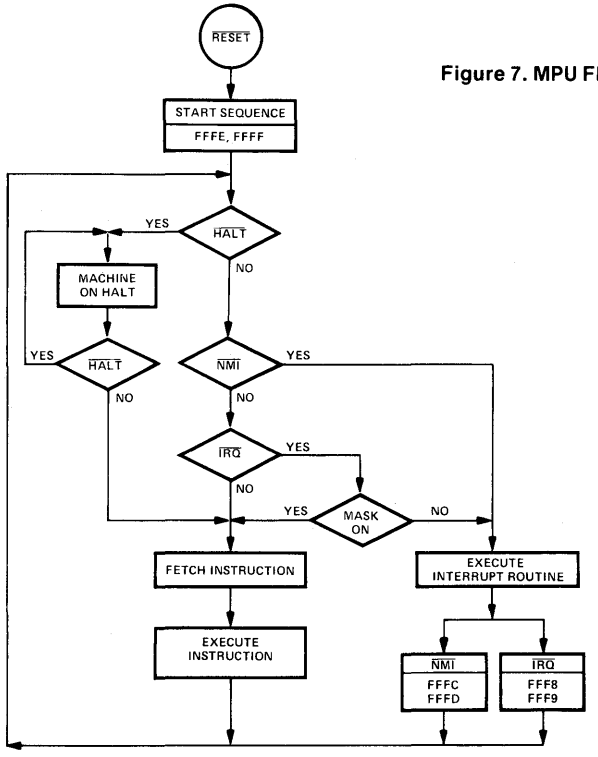


Figure 7. MPU Flow Chart

SP = Stack Pointer
CC = Condition Codes (Also called the Processor Status Byte)
ACCB = Accumulator B
ACCA = Accumulator A
IXH = Index Register, Higher Order 8 Bits
IXL = Index Register, Lower Order 8 Bits
PCH = Program Counter, Higher Order 8 Bits
PCL = Program Counter, Lower Order 8 Bits

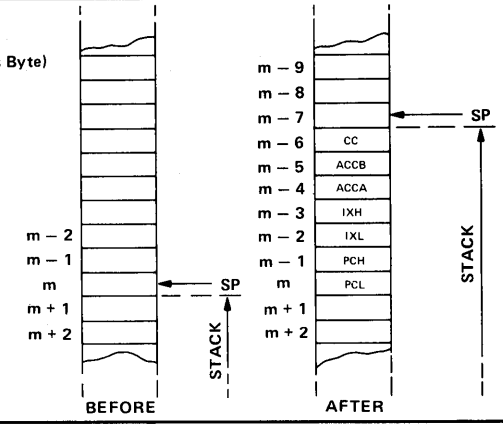


Figure 8. Saving The Status Of The Microprocessor In The Stack

MPU Registers

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer.

Program Counter – The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer – The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register – The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators – The MPU contains two 8-bit accumulators that are used to hold operands and results from the arithmetic logic unit (ALU).

Condition Code Register – The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (1). The unused bits of the Condition Code Register (b6 and b7) are ones.

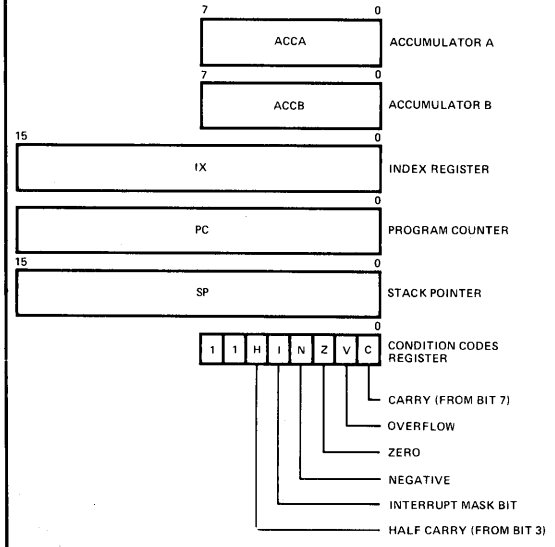
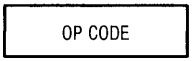


Figure 9. Programming Model of the Microprocessor

MPU Addressing Modes

The S6800 eight-bit microprocessing unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Figure 10 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

Accumulator Addressing (ACCX)



A single byte instruction addressing operands only in accumulator A or accumulator B.

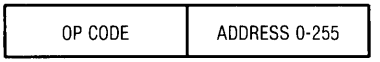
Implied Addressing

Single byte instruction where the operand address is implied by instruction definition (i.e., Stack Pointer, Index Register or Condition Register).

Immediate Addressing

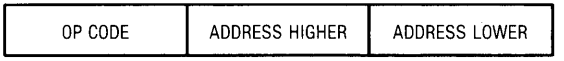
Two or three instructions with an eight or sixteen bit operand respectively. For accumulator operations the eight bit operand respectively. For accumulator operations the eight bit operand is contained in the second byte of a two byte instruction. For Index Register operations (e.g. LDX) sixteen bit operand is contained in the second and third byte of a three byte instruction.

Direct Addressing



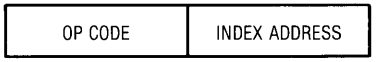
Two byte instructions with the address of the operand contained in the second byte of the instruction. This format allows direct addressing of operands within the first 256 memory locations.

Extended Addressing



Three byte instructions with the higher eight bits of the operand address contained in the second byte and the lower eight bits of address contained in the third byte of the instruction. This format allows direct addressing of all 65,536 memory locations.

Indexed Addressing



Two byte instructions where the 8-bit unsigned address contained in the second byte of the instruction is added to the sixteen bit Index Register resulting in a sixteen bit effective address. The effective address is stored in a temporary register and the contents of the Index Register are unchanged.

Relative Addressing

Two byte instructions where the relative address contained in the second byte of the instruction is added to the sixteen bit program counter plus two. The relative address is interpreted as a two's complement number allowing relative addressing within a range of −126 to +129 bytes of the present instruction.

Instruction	Mnemonic	Addressing Mode: Implied OP MC PB	Immediate OP MC PB	Direct OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	Condition Reg 5 4 3 2 1 0 / H I N Z V C
Load accumulator	LDAA		86 2 2	96 3 2	B6 4 3	A6 5 2		M → A	• • ↕ ↕ R •
	LDAB		C6 2 2	D6 3 2	F6 4 3	E6 5 2		M → B	• • ↕ ↕ R •
Load stack pointer	LDS		8E 3 3	9E 4 2	BE 5 3	AE 6 2		M → SP_H, (M + 1) → SP_L	• • 9 ↕ R •
Load index register	LDX		CE 3 3	DE 4 2	FE 5 3	EE 6 2		M → X_H, (M + 1) → X_L	• • 9 ↕ R •
Store accumulator	STAA			97 4 2	B7 5 3	A7 6 2		A → M	• • ↕ ↕ R •
	STAB			D7 4 2	F7 5 3	E7 6 2		B → M	• • ↕ ↕ R •
Store stack pointer	STS			9F 5 2	BF 6 3	AF 7 2		SP_H → M, SP_L → (M + 1)	• • 9 ↕ R •
Store index register	STX			DF 5 2	FF 6 3	EF 7 2		X_H → M, X_L → (M + 1)	• • 9 ↕ R •
Transfer accumulators	TAB	16 2 1						A → B	• • ↕ ↕ R •
	TBA	17 2 1						B → A	• • ↕ ↕ R •
Transfer Acc. to cond. reg.	TAP	06 2 1						A → CCR	Note 12
Transfer cond. reg. to Acc.	TPA	07 2 1						CCR → A	• • • • • •
Transfer stck ptr to index	TSX	30 4 1						SP + 1 → X	• • • • • •
Transfer index to stck ptr	TXS	35 4 1						X − 1 → SP	• • • • • •
Pull data	PULA	32 4 1						SP + 1 → SP, M_{SP} → A	• • • • • •
	PULB	33 4 1						SP + 1 → SP, M_{SP} → B	• • • • • •
Push data	PSHA	36 4 1						A → M_{SP}, SP − 1 → SP	• • • • • •
	PSHB	37 4 1						B → M_{SP}, SP − 1 → SP	• • • • • •
Add accumulators	ABA	1B 2 1						A + B → A	↕ • ↕ ↕ ↕ ↕
Add	ADDA		8B 2 2	9B 3 2	BB 4 3	AB 5 2		A + M → A	↕ • ↕ ↕ ↕ ↕
	ADDB		CB 2 2	DB 3 2	FB 4 3	EB 5 2		B + M → B	↕ • ↕ ↕ ↕ ↕
Add with carry	ADCA		89 2 2	99 3 2	B9 4 3	A9 5 2		A + M + C → A	↕ • ↕ ↕ ↕ ↕
	ADCB		C9 2 2	D9 3 2	F9 4 3	E9 5 2		B + M + C → B	↕ • ↕ ↕ ↕ ↕
Subtract accumulators	SBA	10 2 1						A − B → A	• • ↕ ↕ ↕ ↕
Subtract	SUBA		80 2 2	90 3 2	B0 4 3	A0 5 2		A − M → A	• • ↕ ↕ ↕ ↕
	SUBB		C0 2 2	D0 3 2	F0 4 3	E0 5 2		B − M → B	• • ↕ ↕ ↕ ↕
Subtract with carry	SBCA		82 2 2	92 3 2	B2 4 3	A2 5 2		A − M − C → A	• • ↕ ↕ ↕ ↕
	SBCB		C2 2 2	D2 3 2	F2 4 3	E2 5 2		B − M − C → B	• • ↕ ↕ ↕ ↕
Increment	INCA	4C 2 1						A + 1 → A	• • ↕ ↕ 5 •
	INCB	5C 2 1						B + 1 → B	• • ↕ ↕ 5 •
	INC				7C 6 3	6C 7 2		M + 1 → M	• • ↕ ↕ 5 •
Increment stack pointer	INS	31 4 1						SP + 1 → SP	• • • • • •
Increment index reg.	INX	08 4 1						X + 1 → X	• • • • ↕ •
Decrement	DECA	4A 2 1						A − 1 → A	• • ↕ ↕ 4 •
	DECB	5A 2 1						B − 1 → B	• • ↕ ↕ 4 •
	DEC				7A 6 3	6A 7 2		M − 1 → M	• • ↕ ↕ 4 •
Decrement stack pointer	DES	34 4 1						SP − 1 → SP	• • • • • •
Decrement index register	DEX	09 4 1						X − 1 → X	• • • ↕ • •
Complement (1's)	COMA	43 2 1						$\overline{A}$ → A	• • ↕ ↕ R S
	COMB	53 2 1						$\overline{B}$ → B	• • ↕ ↕ R S
	COM				73 6 3	63 7 2		$\overline{M}$ → M	• • ↕ ↕ R S
Complement (2's)	NEGA	40 2 1						00 − A → A	• • ↕ ↕ 1 2
	NEGB	50 2 1						00 − B → B	• • ↕ ↕ 1 2
	NEG				70 6 3	60 7 2		00 − M → M	• • ↕ ↕ 1 2
Decimal adjust accumulator	DAA	19 2 1							• • ↕ ↕ ↕ 3

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

Figure 10. S6800 Instruction Set

Instruction	Mnemonic	Addressing Mode: Implied OP MC PB	Immediate OP MC PB	Direct OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	Condition Reg 5 4 3 2 1 0 — H I N Z V C
Logical and	ANDA		84 2 2	94 3 2	B4 4 3	A4 5 2		A • M → A	• • ‡ ‡ R •
	ANDB		C4 2 2	D4 3 2	F4 4 3	E4 5 2		B • M → B	• • ‡ ‡ R •
Inclusive or	ORAA		8A 2 2	9A 3 2	BA 4 3	AA 5 2		A + M → A	• • ‡ ‡ R •
	ORAB		CA 2 2	DA 3 2	FA 4 3	EA 5 2		B + M → B	• • ‡ ‡ R •
Exclusive or	EORA		88 2 2	98 3 2	B8 4 3	A8 5 2		A ⊕ M → A	• • ‡ ‡ R •
	EORB		C8 2 2	D8 3 2	F8 4 3	E8 5 2		B ⊕ M → B	• • ‡ ‡ R •
Shift left arithmetic	ASLA	48 2 1						A, B: C ← b7 … b0 ← 0	• • ‡ ‡ 6 ‡
	ASLB	58 2 1							• • ‡ ‡ 6 ‡
	ASL				78 6 3	68 7 2		M: C ← b7 … b0 ← 0	• • ‡ ‡ 6 ‡
Shift right arithmetic	ASRA	47 2 1						A, B: b7 → … b0 → C	• • ‡ ‡ 6 ‡
	ASRB	57 2 1							• • ‡ ‡ 6 ‡
	ASR				77 6 3	67 7 2		M: b7 → … b0 → C	• • ‡ ‡ 6 ‡
Shift right logical	LSRA	44 2 1						A, B: 0 → b7 … b0 → C	• • R ‡ 6 ‡
	LSRB	54 2 1							• • R ‡ 6 ‡
	LSR				74 6 3	64 7 2		M: 0 → b7 … b0 → C	• • R ‡ 6 ‡
Rotate left	ROLA	49 2 1						A, B: C ← b7 … b0 ←	• • ‡ ‡ 6 ‡
	ROLB	59 2 1							• • ‡ ‡ 6 ‡
	ROL				79 6 3	69 7 2		M: C ← b7 … b0 ←	• • ‡ ‡ 6 ‡
Rotate right	RORA	46 2 1						A, B: → b7 … b0 → C	• • ‡ ‡ 6 ‡
	RORB	56 2 1							• • ‡ ‡ 6 ‡
	ROR				76 6 3	66 7 2		M: → b7 … b0 → C	• • ‡ ‡ 6 ‡
Compare accumulators	CBA	11 2 1						A − B	• • ‡ ‡ ‡ ‡
Compare	CMPA		81 2 2	91 3 2	B1 4 3	A1 5 2		A − M	• • ‡ ‡ ‡ ‡
	CMPB		C1 2 2	D1 3 2	F1 4 3	E1 5 2		B − M	• • ‡ ‡ ‡ ‡
Compare index register	CPX		8C 3 3	9C 4 2	BC 5 3	AC 6 2		$X_H - M, X_L - (M+1)$	• • 7 ‡ 8 •
Test (zero or minus)	TSTA	4D 2 1						A − 00	• • ‡ ‡ R R
	TSTB	5D 2 1						B − 00	• • ‡ ‡ R R
	TST				7D 6 3	6D 7 2		M − 00	• • ‡ ‡ R R
Bit test	BITA		85 2 2	95 3 2	B5 4 3	A5 5 2		A • M	• • ‡ ‡ R •
	BITB		C5 2 2	D5 3 2	F5 4 3	E5 5 2		B • M	• • ‡ ‡ R •
								TEST	
Branch	BRA						20 4 2		• • • • • •
Branch if carry clear	BCC						24 4 2	C = 0	• • • • • •
Branch if carry set	BCS						25 4 2	C = 1	• • • • • •
Branch if overflow clear	BVC						28 4 2	V = 0	• • • • • •
Branch if overflow set	BVS						29 4 2	V = 1	• • • • • •
Branch if equal to zero	BEQ						27 4 2	Z = 1	• • • • • •
Branch if greater or equal to zero	BGE						2C 4 2	N ⊕ V = 0	• • • • • •
Branch if greater than zero	BGT						2E 4 2	Z + (N ⊕ V) = 0	• • • • • •
Branch if less than zero	BLT						2D 4 2	N ⊕ V = 1	• • • • • •
Branch if less than or equal to zero	BLE						2F 4 2	Z + (N ⊕ V) = 1	• • • • • •
Branch if not equal to zero	BNE						26 4 2	Z = 0	• • • • • •
Branch if minus	BMI						2B 4 2	N = 1	• • • • • •
Branch if plus	BPL						2A 4 2	N = 0	• • • • • •
Branch if higher	BHI						22 4 2	C + Z = 0	• • • • • •
Branch if lower or same	BLS						23 4 2	C + Z = 1	• • • • • •

OP = Operation Code MC = Number of MPU Cycles PB = Number of Program Bytes

Figure 10. S6800 Instruction Set (Cont'd.)

Instruction	Mnemonic	Addressing Modes: Implied OP MC PB	Direct OP MC PB	Immediate OP MC PB	Extended OP MC PB	Indexed OP MC PB	Relative OP MC PB	Boolean/Arith Operation	Condition Reg. 5 4 3 2 1 0 H I N Z V C
Branch to subroutine	BSR						8D 8 2		• • • • • •
Jump to subroutine	JSR				BD 9 3	AD 8 2		See Special Operations	• • • • • •
Jump	JMP				7E 3 3	6E 4 2			• • • • • •
Return from subroutine	RTS	39 5 1							• • • • • •
Return from interrupt	RTI	3B 10 1							Note 10
Software interrupt	SWI	3F 12 1							• S • • • •
Wait for interrupt	WAI	3E 9 1							• 11 • • • •
No operation	NOP	01 2 1						PC + 1 → PC	• • • • • •
Clear	CLRA	4F 2 1						00 → A	• • R S R R
	CLRB	5F 2 1						00 → B	• • R S R R
	CLR				7F 6 3	6F 7 2		00 → M	• • R S R R
Clear carry	CLC	0C 2 1						0 → C	• • • • • R
Clear interrupt mask	CLI	0E 2 1						0 → I	• R • • • •
Clear overflow	CLV	0A 2 1						0 → V	• • • • R •
Set carry	SEC	0D 2 1						1 → C	• • • • • S
Set interrupt mask	SEI	0F 2 1						1 → I	• S • • • •
Set overflow	SEV	0B 2 1						1 → V	• • • • S •

Figure 10. S6800 Instruction Set (Cont'd.)

CONDITION CODE SYMBOLS:

H	Half-carry from bit 3;
I	Interrupt mask
N	Negative (sign bit)
Z	Zero (byte)
V	Overflow, 2's complement
C	Carry from bit 7
R	Reset Always
S	Set Always
↕	Test and set if true, cleared otherwise
•	Not Affected

LEGEND:

OP	Operation Code (Hexadecimal):
MC	Number of MPU Cycles;
PB	Number of Program Bytes;
+	Arithmetic Plus;
−	Arithmetic Minus;
•	Boolean AND;
MSP	Contents of memory location pointed to by Stack Pointer;
+	Boolean Inclusive OR;
⊕	Boolean Exclusive OR;
$\overline{M}$	Complement of M;
→	Transfer Into;
0	Bit = Zero;
00	Byte = Zero;

Note – Accumulator addressing mode instructions are included in the IMPLIED addressing.

CONDITION CODE REGISTER NOTES:

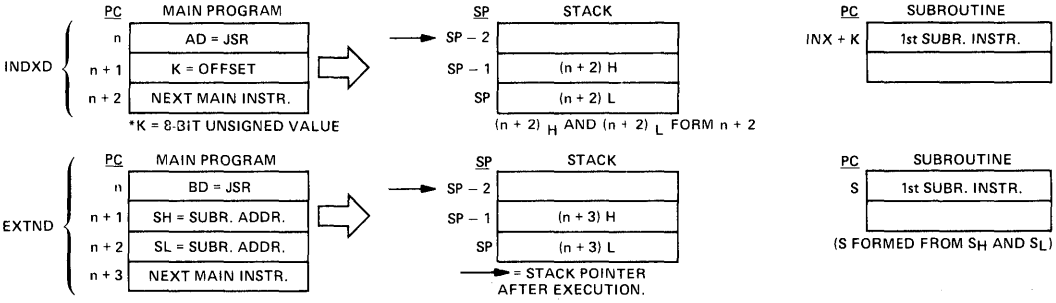
(Bit set if test is true and cleared otherwise)

1	(Bit V)	Test: Result = 10000000?
2	(Bit C)	Test: Result = 00000000?
3	(Bit C)	Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4	(Bit V)	Test: Operand = 10000000 prior to execution?
5	(Bit V)	Test: Operand = 01111111 prior to execution?
6	(Bit V)	Test: Set equal to result of N ⊕ C after shift has occurred.
7	(Bit N)	Test: Sign bit of most significant (MS) byte = 1?
8	(Bit V)	Test: 2's complement overflow from subtraction of MS bytes?
9	(Bit N)	Test: Result less than zero? (Bit 15 = 1)
10	(All)	Load Condition Code Register from Stack. (See Special Operations)
11	(Bit I)	Set when interrupt occurs, if previously set, a Non-Maskable Interrupt is required to exit the wait state.
12	(ALL)	Set according to the contents of Accumulator A

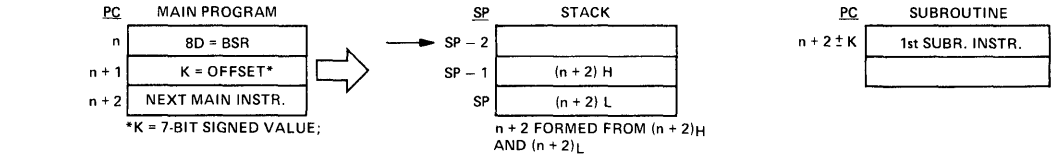
Special Operations

JMP, JUMP:

JSR, JUMP TO SUBROUTINE:

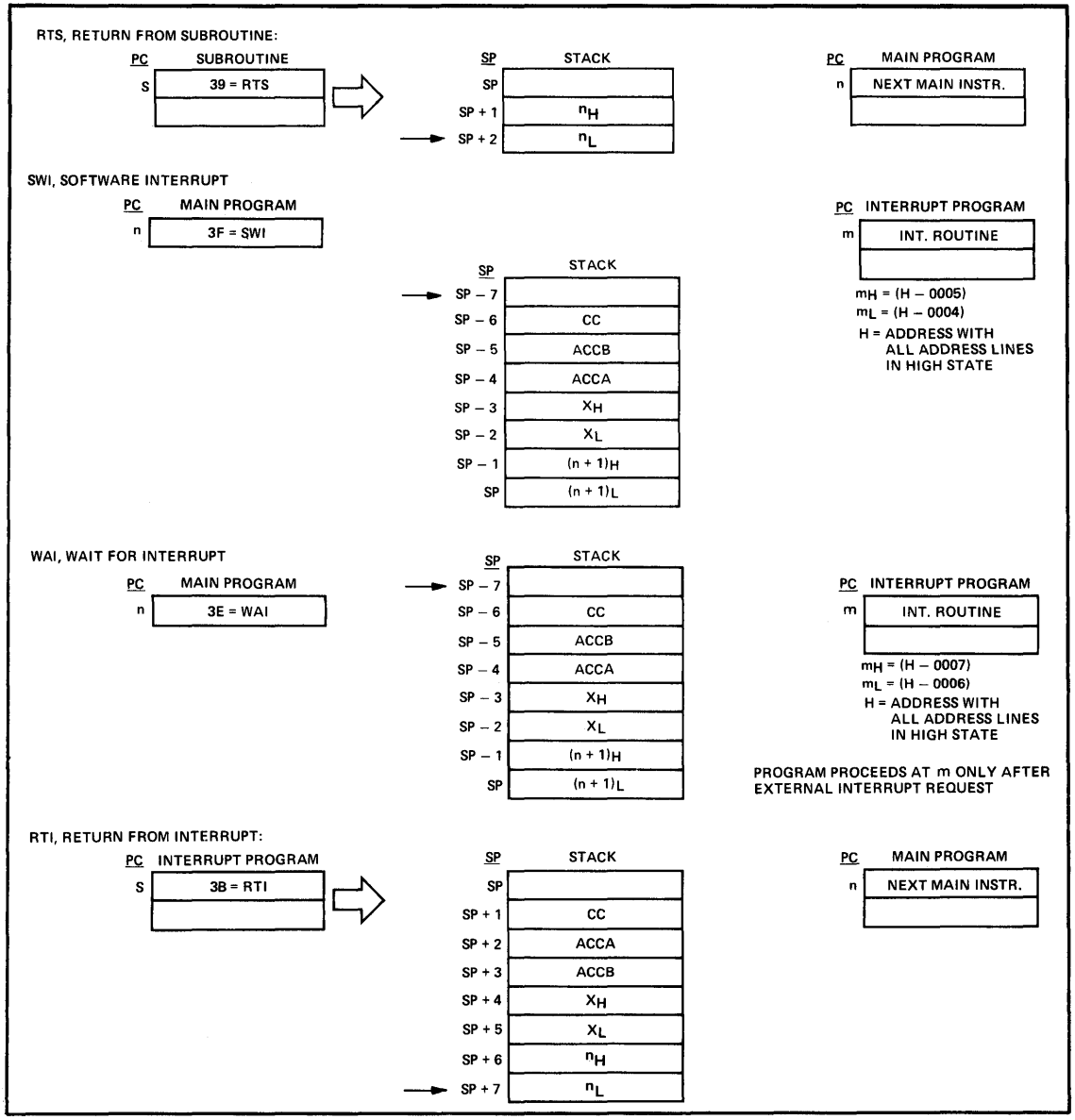


BSR, BRANCH TO SUBROUTINE:



S6800

Special Operations



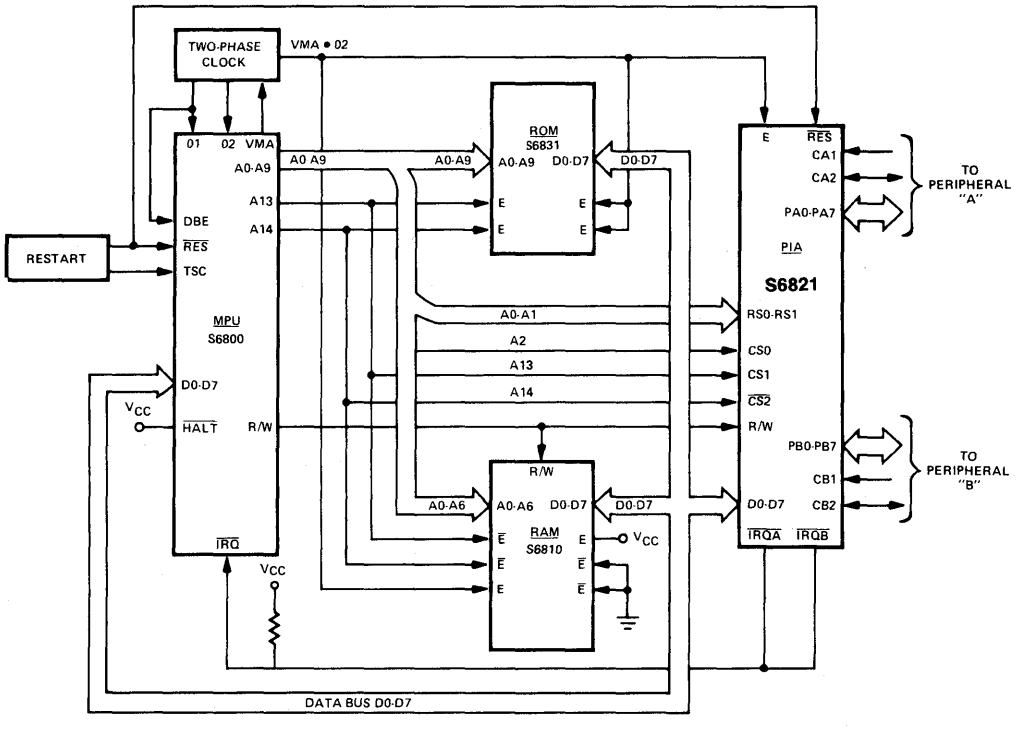


Figure 11. Minimum System Configuration

Systems Operation

To demonstrate the great versatility of the functional building block concept, a typical system configuration is shown. This configuration will demonstrate how easily a basic system may be upgraded and expanded for a number of different applications.

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 11). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

Two-Phase Clock Circuitry and Timing – The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1MHz. In addition to the two phases, this circuit should also generate an enable signal E, and its complement $\overline{E}$, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement is obtained by ANDing $\phi 2$ and VMA (Valid Memory Address).

Chip Selection and Addressing – The minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13 and A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000 – 007F
PIA	0	1	2004 – 2007 (Registers)
ROM	1	1	6000 – 63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

Peripheral Control – All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

Restart and Non-Maskable Interrupt – Since this basic system does not have a nonvolatile RAM, special circuitry to handle loss of power using NMI is not required. Circuitry is, however, required to insure proper initialization of the MPU when power is turned on. This circuit should insure that the Restart signal is held low for eight $\phi 1$ clock cycles after the V_{CC} power supply reaches a voltage of approximately 4.75 volts DC. Also, in order to insure that a PIA or ACIA is not inadvertently selected during the power-on sequence, Three-State Control (TSC) should be held high until the positive transition of Restart.

$\overline{\text{HALT}}$ – The $\overline{\text{Halt}}$ line is tied to V_{CC} and will automatically place the MPU in the run state when power is turned on. This signal may be used to halt the MPU if a switch is used to tie the line to ground for HALT and to V_{CC} for RUN.

AMERICAN MICROSYSTEMS, INC.

S6801/S6801E

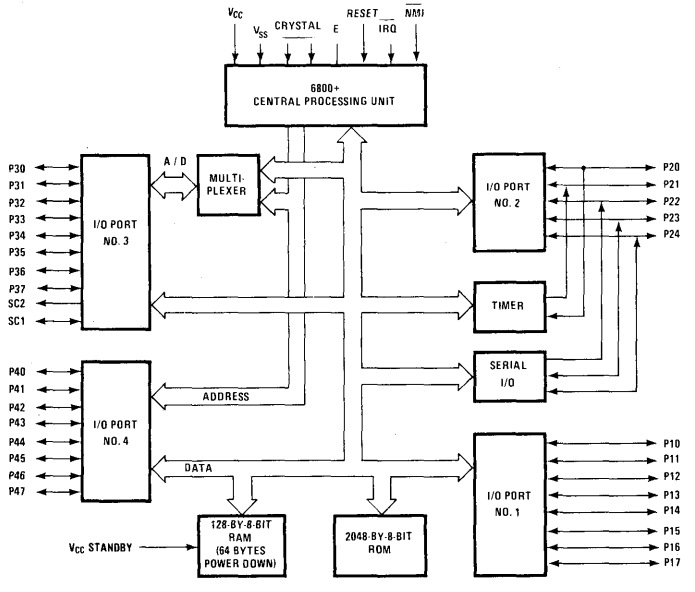
SINGLE CHIP MICROCOMPUTER

Features

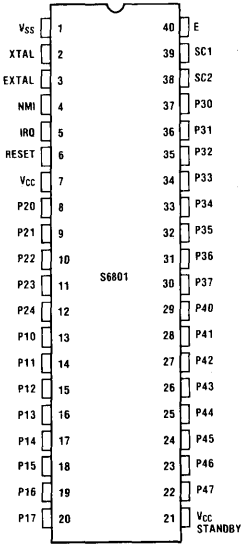
- ☐ Instruction and Addressing Compatible
- ☐ Object Code Compatible
- ☐ 16-Bit Programmable Timer
- ☐ Single Chip or Expandable to 65K Words
- ☐ On-Chip Serial Communications Interface (SCI)
  - — Simplex
  - — Half Duplex
    - — Mark/Space (NRZ)
    - — Biphase (FM)
  - — Port Expansion
    - — Full/Half Duplex
- ☐ Four Internal Baud Rates Available: $\phi 2 \div 16$, 128, 1024, 4096
- ☐ 2K Bytes of ROM
- ☐ 128 Bytes of RAM (64 Bytes Power Down Retainable)
- ☐ 31 Parallel I/O Lines
- ☐ Divide-by-Four Internal Clock
- ☐ Hardware 8×8 Multiply
- ☐ Three Operating Modes
  - — Single Chip
  - — Expanded Multiplex (up to 65K Addressing)
  - — Expanded Non-Multiplex
- ☐ S6801E Operating Modes
  - — Peripheral Controller
  - — Expanded Non-Multiplexed
  - — Expanded Multiplex
- ☐ Expanded Instruction Set
- ☐ Interrupt Capability
- ☐ Low Cost Versions
  - — S6803—No ROM Version
  - — S6803NR—No ROM or RAM
- ☐ TTL-Compatible with Single 5 Volt Supply

S6800

Block Diagram



Pin Configuration



General Description

The S6801 MCU is an 8-bit single-chip microcomputer system which is compatible with the S6800 family of parts. The S6801 is object code compatible with the S6800 instruction set.

The S6801 features improved execution times of key S6800 instructions including Jump to Subroutine (JSR) and all Conditioned Branches (BRA, etc.). In addition, several new 16-bit and 8-bit instructions have been added including Push/Pull to/from Stack, Hardware 8×8 Multiply, and store concatenated A and B accumulators (D accumulator).

The S6801 MCU can be operated in three modes: Single-Chip, Expanded Multiplex (up to 65K Byte Addressing), and Expanded Non-Multiplex. In addition, the S6801 is available with two mask options: an on-chip (÷4) Clock, or an external (÷1) Clock. The external mode is especially useful in Multiprocessor Applications. The S6801E can be configured as a peripheral by using the Read/Write (R/$\overline{W}$), Chip Select (CS), and Register Select (RS). The Read/Write line controls the direction of data on Port 3 and the Register Select (RS) allows for access to either Port 3 data register or control register.

The S6801 Serial Communications Interface (SCI) permits full serial communication using no external components in several operating modes—Full and/or Half Duplex operation—and two formats—Standard Mark/Space for typical Terminal/Modem interfaces and the Bi-Phase (FM, F2F, and Manchester) Format primarily for use between processors. Four software addressable registers are provided to configure the Serial Port; to provide status information; and as transmit/receive data buffers.

The S6801 includes a 16-bit timer with three effectively independent timing functions: (1) Variable pulse width measurement, (2) Variable pulse width generation, and (3) A Timer Overflow—Find Time Flag. This makes the S6801 ideal for applications such as Industrial Controls, Automotive Systems, A/D or D/A Converters, Modems, Real-Time Clocks, and Digital Voltage Controlled Oscillators (VCO).

The S6801 is fully TTL-compatible and requires only a single +5 volt supply.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature Range, T_A	0° to +70°C
Storage Temperature Range, T_{stg}	−55°C to +150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} (V_{IN} or V_{OUT}) V_{DD}.

Electrical Operating Characteristics $V_{CC}=5.0V\pm5\%$, $V_{SS}=0$, $T_A=0$ to +70°C, unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage $\overline{\text{Reset}}$	$V_{SS}+2.0$ $V_{SS}+4.0$		V_{CC} V_{CC}	Vdc
V_{IL}	Input Low Voltage	$V_{SS}-0.3$		$V_{SS}+0.8$	Vdc
I_{TSI} I_{TSI}	Three-State (Off State) Input Current P10-P17, P30-P37 (V_{IN}=0.4 to 2.4 Vdc) P20-P24		2.0 10.0	10 100	μAdc μAdc
V_{OH}	Output High Voltage All Outputs Except XTAL 1 and EXTAL 2 $I_{LOAD}=-200\mu$Adc	$V_{SS}+2.4$			Vdc
V_{OL}	Output Low Voltage All Outputs Except XTAL 1 and EXTAL 2 I_{LOAD}=1.6mAdc			$V_{SS}+0.4$	Vdc

Electric Characteristics (Continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
P_D	Power Dissipation			1200	mW
C_{IN}	Capacitance $V_{IN}=0$, $T_A=25°C$, f=1.0MHz P10-P17, P20-P24, P40-P47, P30-P37 Reset SC1, SC2, IRQ			 12.5 10 7.5	pF
t_{PDSU}	Peripheral Data Setup Time (Figure 3)	200			ns
t_{PDH}	Peripheral Data Hold Time (Figure 3)	0			ns
t_{OSD1}	Delay Time, Enable negative transition to OS3 Neg. Trans.			1.0	μs
t_{OSD2}	Delay Time, Enable neg. trans. to OS3 positive transition			1.0	μs
t_{PWD}	Delay Time, Enable negative transition to Peripheral Data Valid (Figure 4)			350	ns
t_{CMOS}	Delay Time, Enable negative transition to Peripheral Data Valid ($V_{SS}-30\%$ V_{CC}, P20-P24 (Figure 4)			2.0	μs
I_{OH}	Darlington Drive Current $V_O=1.5$Vdc — P10-P17	−1.0	−2.5	−10	mAdc
V_{SBB} V_{SB}	Standby Voltage (Not Operating) (Operating)	4.00 4.75		5.25 5.25	Vdc

NOTE: The above electricals satisfy Ports 1 and 2 always, and Ports 3 and 4 in the single chip mode only.

Bus Timing (Figure 7)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{CYC}	Cycle Time	1000		2000	ns
P_{WASH}	Address Strobe Pulse Width High	220			ns
t_{ASR}	Address Strobe Rise Time			50	ns
t_{ASF}	Address Strobe Fall Time			50	ns
t_{ASD}	Address Strobe Delay Time	60			ns
t_{ER}	Enable Rise Time			50	ns
t_{EF}	Enable Fall Time			50	ns
P_{WEH}	Enable Pulse Width High Time	450		1000	ns
P_{WEL}	Enable Pulse Width Low Time	430		1000	ns
t_{ASED}	Address Strobe to Enable Delay Time	60			ns
t_{AD}	Address Delay Time			270	ns
t_{DDW}	Data Delay Write Time			225	ns
t_{DSR}	Data Set-up Time	100			ns
t_{HR}	Hold Time Read	20		100	ns
t_{HW}	Hold Time Write	20			ns
t_{ADL}	Address Delay Time for Latch			200	ns
t_{AHL}	Address Hold Time for Latch	20			ns
PW_O	Pulse Width	370	370		ns
t_{AH}	Address Hold Time	20			ns
t_{UT}	Total Up Time	750			ns

MCU Signal Description

This section gives a description of the MCU signals for the various modes. General pin assignments for the signals are shown on page 1. SC1 and SC2 are signals which vary with the mode that the chip is in. Table 1 gives a summary of their function.

Table 1. Mode and Port Summary

MODE	PORT 1 EIGHT LINES	PORT 2 FIVE LINES	PORT 3 EIGHT LINES	PORT 4 EIGHT LINES	SC1	SC2
SINGLE CHIP	I/O	I/O	I/O	I/O	$\overline{IS3(I)}$	$\overline{OS3(O)}$
EXPANDED MUX	I/O	I/O	ADDRESS BUS (A0-A7) DATA BUS D0-D7	ADDRESS BUS* (A8-A15)	AS(O)	R/$\overline{W}$(O)
EXPANDED NON-MUX	I/O	I/O	DATA BUS D0-D7	ADDRESS BUS* (A0-A7)	$\overline{IOS}$(O)	R/$\overline{W}$(O)

*THESE LINES CAN BE SUBSTITUTED FOR I/O (INPUT ONLY) STARTING WITH THE MOST SIGNIFICANT ADDRESS LINE.

I = INPUT
O = OUTPUT
R/$\overline{W}$ = READ/$\overline{WRITE}$
IS = INPUT STROBE
OS = OUTPUT STROBE
IOS = I/O SELECT
SC = STROBE CONTROL
AS = ADDRESS STROBE

Read/Write Timing for Ports 3 and 4 (Figures 1-2)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{AD}	Address Delay			270	ns
t_{ACC}	Peripheral Read Access Time $t_{ACC}=t_{UT}-(t_{AD}+t_{DSR})$			530	ns
t_{DSR}	Data Setup Time (Read)	100			ns
t_{HR}	Input Data Hold Time	10			ns
t_{HW}	Output Data Hold Time	20			ns
t_{AH}	Address Hold Time (Address, R/W)	20			ns
t_{DDW}	Data Delay Time (Write)		165	225	ns
t_{PCS}	Processor Controls				
	Processor Control Setup Time	200			ns
t_{PCr}, t_{PCf}	Processor Control Rise and Fall Time (Measured between 0.8V and 2.0V)			100	ns

Port 3 Strobe Timing (Figures 5-6)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
t_{DSD1}	Output Strobe Delay 1			100	μs
t_{OSD2}	Output Strobe Delay 2			100	μs
PW_{IS}	Input Strobe Pulse Width	200			ns
t_{IH}	Input Data Hold Time	20			ns
t_{IS}	Input Data Setup Time	100			ns

Figure 1. Read Data From Memory or Peripherals Expanded Non-Multiplexed

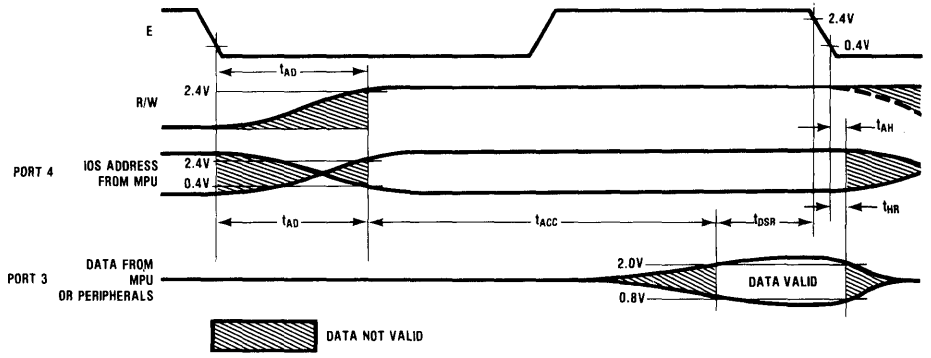
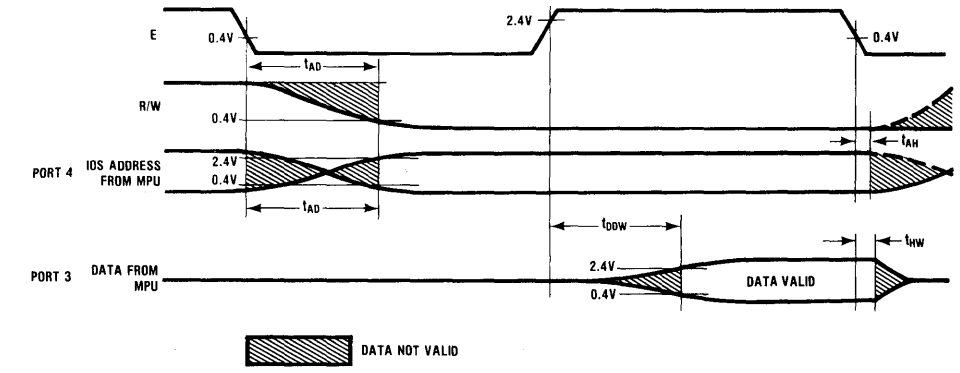


Figure 2. Write Data In Memory or Peripherals Expanded Non-Multiplexed



Ports 1 and 2, and Ports 3 and 4 in the Single Chip Mode

Figure 3. Peripheral Data Setup and Hold Times (Read Mode)

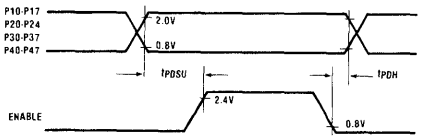


Figure 4. Peripheral CMOS Data Delay Times (Write Mode)

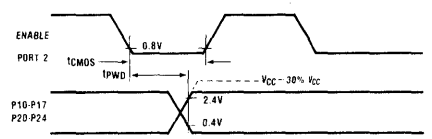


Figure 5. Output Strobe Timing — Single Chip Mode

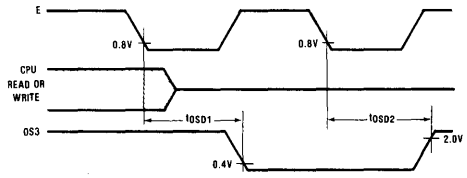


Figure 6. Input Strobe Timing — Single Chip Mode

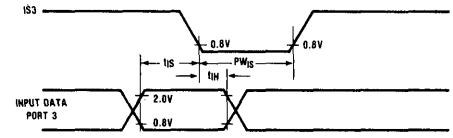


Figure 7. Multiplexed Bus Timing

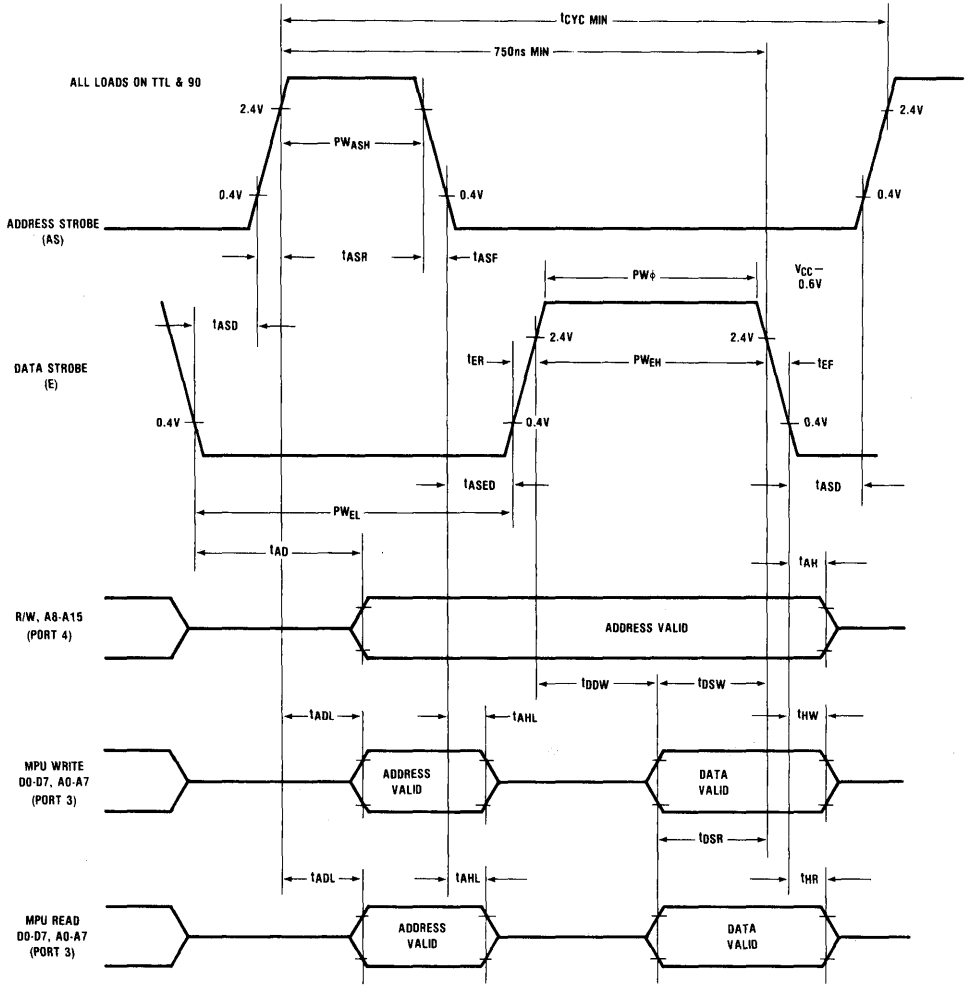


Figure 8. CMOS Load

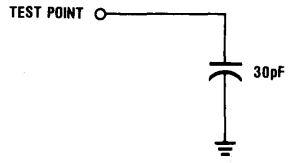
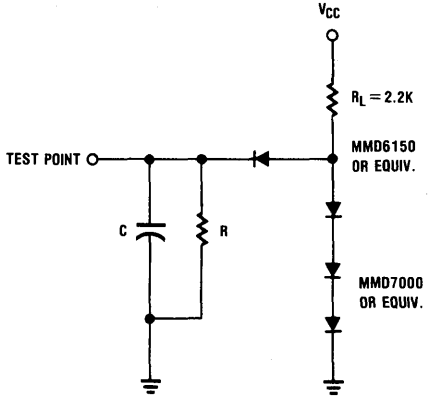
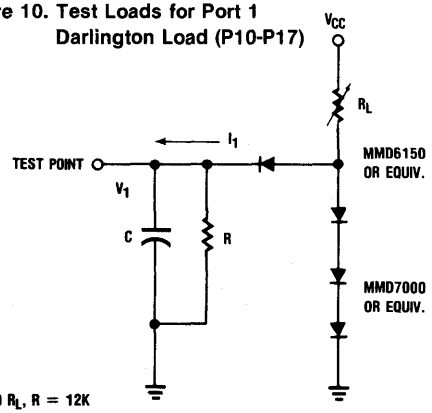


Figure 9. Bus Timing Test Load and Ports 1, 3 and 4 for Single Chip Mode



C = 90pF FOR P30-P37, P40-P47, E, SC1, SC2
R = 16.5KΩ FOR P30-P37, P40-P47, E, SC1, SC2

Figure 10. Test Loads for Port 1 Darlington Load (P10-P17)



C = 40 R_L, R = 12K
ADJUST R_L SO THAT I_1 = 3.2mA
WITH V_1 = 0.4V and V_{CC} = 5.25V

Figure 11. Typical Data Bus Output Delay versus Capacitive Loading

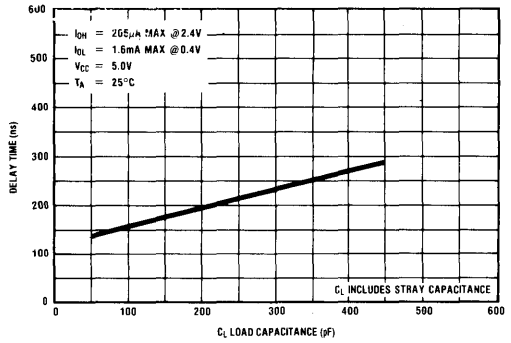
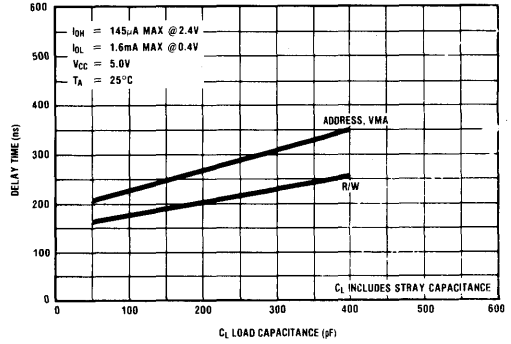


Figure12. Typical Read/Write, VMA, and Address Output Delay Versus Capacitive Loading



Signal Descriptions

V_{CC} and V_{SS}

These two pins are used to supply power and ground to the chip. The voltage supplied will be +5 volts±5%.

XTAL 1 and EXTAL 2

These connections are for a parallel resonant fundamental crystal, AT cut. Divide by 4 circuitry is included with the internal clock, so a 4 MHz crystal may be used to run the system at 1MHz. The divide by 4 circuitry allows for use of the inexpensive 3.56 MHz Color TV crystal for non-time critical applications. Two 27pF capacitors are needed from the two crystal pins to ground to insure reliable operation. EXTAL 2 may be driven by an external clock source at a 4 MHz rate to run at 1 MHz with a 40/60% duty cycle. It is not restricted to 4 MHz. XTAL 1

must be grounded if an external clock is used. The following are the recommended crystal parameters:

AT=Cut Parallel Resonance Crystal
C_o=7pF Max
FREQ=4.0 MHz @ C_L=24pF
R_S=50 ohms Max
Frequency Tolerance=±5% to ±0.02%
The best E output "Worst Case Design" tolerance is ±0.05% (500ppM) using a ±0.02% crystal.

V_{CC} Standby

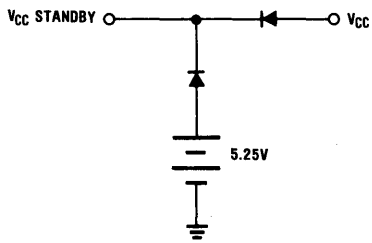
This pin will supply +5 volts ±5% to the standby RAM on the chip. The first 64 bytes of RAM will be maintained in the power down mode with 8 mA current max in the ROM version. The circuit of Figure 15 can be utilized to assure that V_{CC} Standby does not go below V_{SBB} during power down.

To retain information in the RAM during power down the following procedure is necessary:

1) Write "0" into the RAM enable bit, RAM E. RAM E is bit 6 of the RAM Control Register at location $0014. This disables the standby RAM, thereby protecting it at power down.

2) Keep V_{CC} Standby greater than V_{SBB}.

Figure 13. Battery Backup for V_{CC} Standby



Reset

This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial startup of the processor. On power up, the reset must be held low for at least 20 ms. During operation, $\overline{\text{Reset}}$, when brought low, must be held low at 3 clock cycles.

When a high level is detected, the MPU does the following:

a) All the higher order address lines will be forced high.

b) I/O Port 2 bits, 2, 1, and 0 are latched into programmed control bits PC2, PC1 and PC0.

c) The last two (FFFE, FFFF) locations in memory will be used to load the program addressed by the program counter.

d) The interrupt mask bit is set, must be cleared before the MPU can recognize maskable interrupts.

Enable (E)

This supplies the external clock for the rest of the system when the internal oscillator is used. It is a single phase, TTL compatible clock, and will be the divide by 4 result of the crystal frequency. It will drive one TTL load and 90pF.

Non-Maskable Interrupt ($\overline{\text{NMI}}$)

A low-going edge on this input requests that a non-maskable-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

In response to an $\overline{\text{NMI}}$ interrupt, the Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the stack. At the end of the sequence, a 16-bit address will be loaded that points to a vectoring address located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt service routine in memory.

A 3.3 KΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during E and will start the interrupt routine on the clock bar following the completion of an instruction.

Interrupt Request ($\overline{\text{IRQ}}$)

This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the

stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further maskable interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The IRQ requires a 3.3KΩ external resistor to V_{CC} which should be used for wire-OR and optimum control of interrupts. Internal Interrupts will use an internal interrupt line (IRQ2). This Interrupt will operate the same as IRQ except that it will use the vector address of FFF0 and FFF7. IRQ1 will have priority over IRQ2 if both occur at the same time. The Interrupt Mask Bit in the condition mode register masks both interrupts. (See Figure 23.)

The following pins are available in the Single Chip Mode, and are associated with Port 3 only.

Input Strobe ($\overline{IS3}$) (SC1)

This sets an interrupt for the processor when the IS3 Enable bit is set. As shown in Figure 6 Input Strobe Timing, IS3 will fall T_{IS} minimum after data is valid on Port 3. If IS3 Enable is set in the I/O Port Control/Status Register, an interrupt will occur. If the latch enable bit in the I/O Control Status Register is set, this strobe will latch the input data from another device when that device has indicated that it has valid data.

Output Strobe ($\overline{OS3}$) (SC2)

This signal is used by the processor to strobe an external device, indicating valid data is on the I/O pins. The timing for the Output Strobe is shown in Figure 5. I/O Port Control/Status Register is discussed in the following section.

The following pins are available in the Expanded Modes.

Read Write (R/W) (SC2)

This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or a Write (low) state. The normal standby state of this signal is Read (high). This output is capable of driving one TTL load and 90pF.

I/O Strobe ($\overline{IOS}$) (SC1)

In the expanded non-multiplexed mode of operation, $\overline{IOS}$ internally decodes A9 through A15 as zero's and A8 as a one. This allows external access of the 256 locations from $0100 to $01FF. The timing diagrams are shown as Figures 1 and 2.

Address Strobe (AS) (SC1)

In the expanded multiplexed mode of operation address strobe is output on this pin. This signal is used to latch the 8 LSB's of address which are multiplexed with data on Port 3. An 8-bit latch is utilized in conjunction with Address Strobe, as shown in Figure 27. Expanded Multiplexed Mode. Address Strobe signals the latch when it is time to latch the address lines so the lines can become data bus lines during the E pulse. The timing for this signal is shown in the MC6801 Bus Timing Figure 7. This signal is also used to disable the address from the multiplexed bus allowing a deselect time, T_{ASD} before the data is enabled to the bus.

S6801 Ports

There are four I/O ports on the S6801MCU; three 8-bit ports and one 5-bit port. There are two control lines associated with one of the 8-bit ports. Each port has an associated write only Data Direction Register which allows each I/O line to be programmed to act as an input or an output. *A "1" in the corresponding Data Direction Register bit will cause that I/O line to be an output A "0" in the corresponding Data Direction Register bit will cause the I/O line to be an input. There are four ports: Port 1, Port 2, Port 3, and Port 4. Their addresses and the addresses of their Data Direction registers are given in Table 2.

**The only exception is bit 1 of Port 2, which can either be data input or Timer output.*

Table 2. Port and Data Direction Register Addresses

Ports	Port Address	Data Direction Register Address
I/O Port 1	$0002	$0000
I/O Port 2	$0003	$0001
I/O Port 3	$0006	$0004
I/O Port 4	$0007	$0005

I/O Port 1

This is an 8-bit port whose individual bits may be defined as inputs or outputs by the corresponding bit in its data direction register. The 8 output buffers have three-state capability, allowing them to enter a high impedance state when the peripheral data lines are used as inputs. In

order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less than 0.6 volt for a logic "0". As outputs, these lines are TTL compatible and may also be used as a source of up to 1 mA at 1.5 volts to directly drive a Darlington base. After Reset, the I/O lines are configured as inputs. In all three modes, Port 1 is always parallel I/O.

I/O Port 2

This port has five lines that may be defined as inputs or outputs by its data direction register. The 5 output buffers have three-state capability, allowing them to enter a high impedance state when used as an input. In order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less than 0.8 volt for a logic "0". As outputs, this port has no internal pullup resistors but will drive TTL inputs directly. For driving CMOS inputs, external pullup resistors are required. After Reset, the I/O lines are configured as inputs. Three pins on Port 2 (pins 10, 9 and 8 of the chip) are used to program the mode of operation during reset. The values of these pins at reset are latched into the three MSB's (bits 7, 6, and 5) of Port 2 which are read only. This is explained in the Mode Selection Section.

In all three modes, Port 2 can be configured as I/O and provides access to the Serial Communications Interface and the Timer. Bit 1 is the only pin restricted to data input or Timer output.

I/O Port 3

This is an 8-bit port that can be configured as I/O, a data bus, or an address bus multiplexed with the data bus — depending on the mode of operation hardware programmed by the user at reset. As a data bus, Port 3 is bidirectional. As an input for peripherals, it must be supplied regular TTL levels, that is, greater than 2.0 volts for a logic "1" and less than 0.5 volt for a logic "0".

Its TTL compatible three-state output buffers are capable of driving one TTL load and 90pF. In the Expanded Modes, after reset, the data direction register is inhibited and data flow depends on the state of the R/W line. The input strobe (IS3) and the output strobe (OS3) used for handshaking are explained later.

In the three modes Port 3 assumes the following characteristics:

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register. There are two control lines associated with this port in this mode, an input strobe and an output strobe, that can be used for handshaking. They are controlled by the I/O Port Control/Status Register explained at the end of this section.

Expanded Non-Multiplexed Mode: In this mode Port 3 become the data bus (D7-D0).

Expanded Multiplexed Mode: In this mode Port 3 becomes both the data bus (D7-D0) and lower bits of the address bus (A7-A0). An address strobe output is true when the address is on the port.

I/O Port 3 Control/Status Register

	7	6	5	4	3	2	1	0
$000F	IS3 FLAG	IS3 ENABLE	X	OSS	LATCH ENABLE	X	X	X

Bit 0 Not used.
Bit 1 Not used.
Bit 2 Not used.
Bit 3 Latch Enable. This controls the input latch for I/O Port 3. If this bit is set high the input data will be latched with the falling edge of the Input Strobe, IS3. This bit is cleared by reset, or CPU Read Port 3.
Bit 4 (OSS) Output Strobe Select. This bit will select if the Output Strobe should be generated by a write to I/O Port 3 or a read of I/O Port 3. When this bit is cleared the strobe is generated by a read Port 3. When this bit is set the strobe is generated by a write Port 3.
Bit 5 Not used.
Bit 6. IS3 ENABLE. This bit will be the interrupt caused by IS3. When set to a low level the IS3 FLAG will be set by input strobe but the interrupt will not be generated. This bit is cleared by reset.
Bit 7 IS3 FLAG. This is a read only status bit that is set by the failing edge of the input strobe, IS3. It is cleared by a read of the Control/Status Register followed by a read or write of I/O Port 3. Reset will clear this bit.

I/O Port 4

This is an 8-bit port that can be configured as I/O or as address lines depending on the mode of operation. In order to be read properly, the voltage on the input lines must be greater than 2.0 volts for a logic "1" and less

than 0.8 volt for a logic "0". As outputs, each line is TTL compatible and can drive 1 TTL load and 90pF. After reset, the lines are configured as inputs. To use the pins as addresses, therefore, they should be programmed as outputs in the three modes. Port 4 assumes the following characteristics.

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register.

Expanded Non-Multiplexed Mode: In this mode Port 4 is configured as the lower order address lines (A7-A0) by writing one's to the data direction register. When all eight address lines are not needed, the remaining line starting with the most significant bit, may be used as I/O (inputs only).

Expanded Multiplexed Mode: In this mode Port 4 is configured as the high order address lines (A15-A8) by writing one's to the data direction register. When all eight address lines are not needed, the remaining line, starting with the most significant bit, may be used as I/O (inputs only).

Mode Selection

The mode of operation that 6801 will operate in after Reset is determined by hardware that the user must wire on pins 10, 9, and 8 of the chip. These pins are the three LSB's (I/O2, I/O1, and I/O0 respectively) of Port 2. They are latched into programmed control bits PC2, PC1, and PC0 when reset goes high. I/O Port 2 Register is shown below.

	7	6	5	4	3	2	1	0
$0003	PC2	PC1	PC0	I/O4	I/O3	I/O2	I/O1	I/O0

An example of external hardware that could be used in the Expanded Non-Multiplexed Mode is given in Figure 14. In the Expanded Non-Multiplexed Mode, pins 10, 9 and 8 are programmed Hi, Lo, Hi respectively as shown.

Couplers between the pins on Port 2 and the peripherals attached may be required. If the lines go to devices which require signals at power up differing from the signals needed to program the 6801's mode, couplers are necessary.

The 14066B can be used to provide this isolation between the peripheral device and the MCU during reset. Figure 15 shows the logic diagram and xxxxx? for the MC14066B. It is bidirectional and requires no external logic to determine the direction of the information flow.

The logic shown insures that the data on the peripheral will not change before it is latched into the MCU and the MCU has started the reset sequence.

Figure 14. Diode Configuration for the Expanded Non-Multiplexed Mode

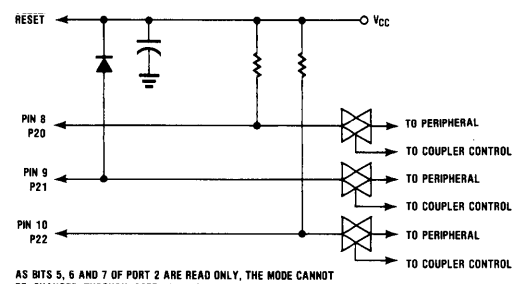
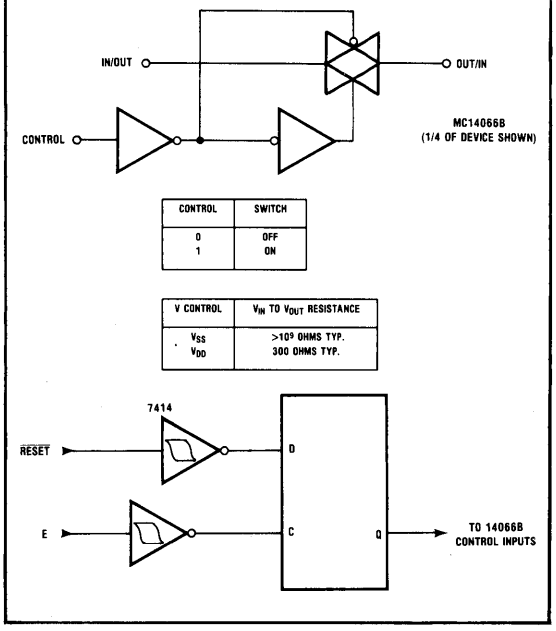


Figure 15. Quad Analog, Switch/Multiplexer In a Typical S6801 Circuit



S6800

S6801 Basic Modes

The S6801 is capable of operating n three basic modes, (1) Single Chip Mode, (2) Expanded Multiplexed Mode (compatible with S6800 peripheral family, (3) Expanded Non-Multiplexed Mode.

Single Chip Mode

Both mask options will operate in this mode. In the Single Chip Mode the parts are configured for I/O.

Internal Clock/Divide-by-Four (S6801)—This mask option is shown in Figure 16. In this mode, Port 3 has two associated control lines, an input strobe and an output strobe for handshaking data.

External Clock/Divide-by-One (S6801E)—This mask option is shown in Figure 16a. The Read/Write (R/W) line, Chip Select (CS), and Register Select (RS) are associated with Port 3 only. The Read/Write (R/W) line controls the direction of data on Port 3 and Chip Select (CS) enables Port 3. The Register Select (RS) allows for the access of Port 3 data register or Port 3 control register.

Figure 16. S6801 MCU Single Chip Mode

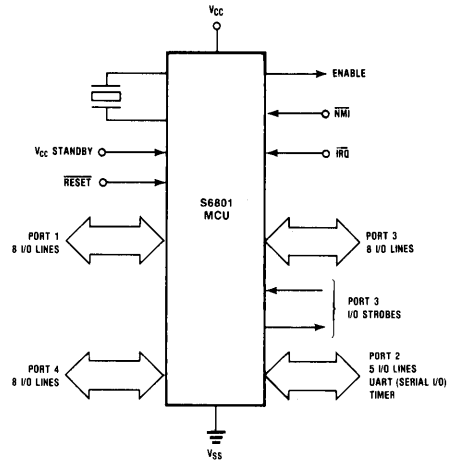
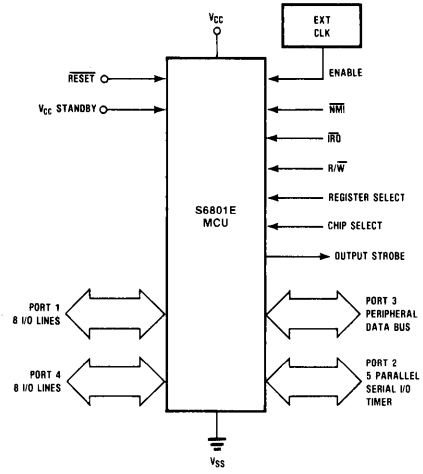


Figure 16a. S6801E MCU Single-Chip Mode



Expanded Non-Multiplexed Mode

In this mode the S6801 will directly address S6800 peripherals with no external logic. In this mode Port 3 becomes the data bus. Port 4 becomes the A7-A0 address bus or partial address and I/O (inputs only). Port 2 can be parallel I/O, serial only. In this mode the S6801 is expandable to 256 locations. The eight address lines associated with Port 4 may be substituted for I/O (inputs only) if a fewer number of address lines will satisfy the application.

Internal Clock/Divide-by-Four—This mask option is shown in Figure 17. The Internal Clock requires only the addition of a crystal for operation. This input will also accept an external TTL or CMOS input, but in either case, the clock frequency will be divided by four for this mask option.

External Clock/Divide-by-One—This mask option is shown in Figure 17a. The External Clock/Divide-by-One allows for an external clock to be applied to the Enable Pin. This is a divide-by-one input only.

Expanded Multiplexed Mode

In this mode Port 4 becomes higher order address lines with an alternative of substituting some of the address lines for I/O (inputs only). Port 3 is the data bus multiplexed with the lower order address lines differentiated by an output called Address Strobe. Port 2 is 5 lines of Parallel I/O, SC1, Timer, or any combination thereof. Port 1 is 8 Parallel I/O lines. In this mode it is expandable to 65K words.

Internal Clock/Divide-by-Four—This mask option is shown in Figure 18. Only an external crystal is required for operation.

External Clock/Divide-by-One—This mask option is shown in Figure 18a. This accepts an external clock input to the enable pin.

Figure 17. S6801 MCU Expanded Non-Multiplexed Mode

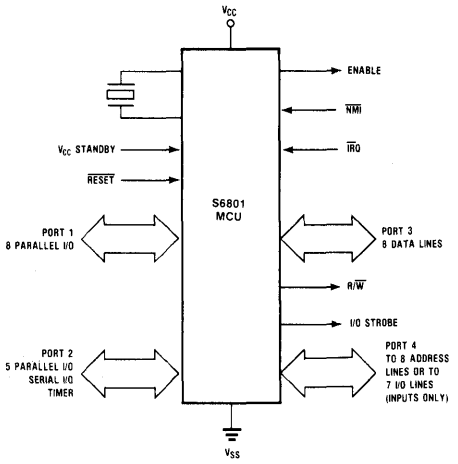


Figure 17a. S6801E MCU Expanded Non-Multiplexed-Mode

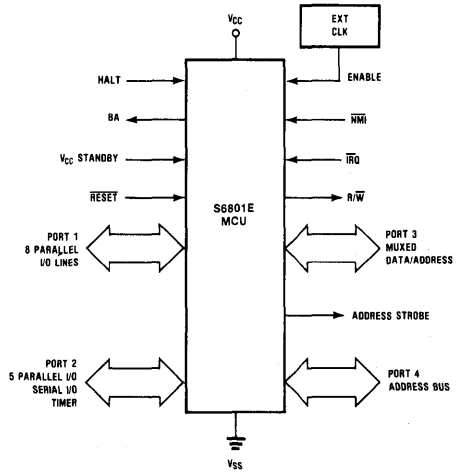


Figure 18. S6801 MCU Expanded Multiplexed Mode

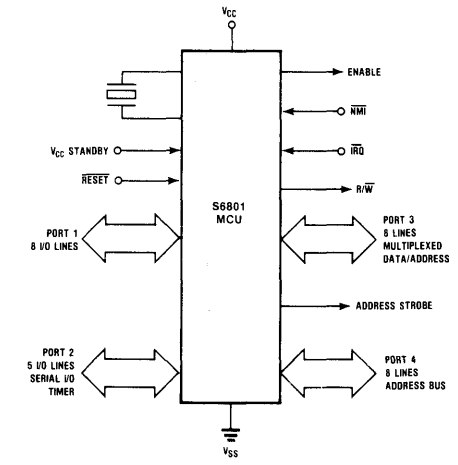


Figure 18a. S6801E MCU Expanded Multiplexed-Mode

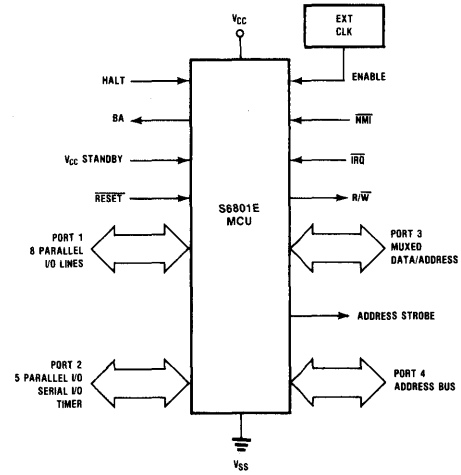


Table 3. Mode Selects

MODE		PROGRAM CONTROL			ROM	RAM	INTERRUPT VECTORS	BUS
7	Single Chip	Hi	Hi	Hi	I	I	I	I
6	Expanded Multiplexed	Hi	Hi	Lo	I	I	I	Ep/M
5	Expanded Non-Multiplexed	Hi	Lo	Hi	I	I	I	Ep
4	Single Chip Test	Hi	Lo	Lo	I(2)	I(1)	I	I
3	64K Address I/O	Lo	Hi	Hi	E	E	E	Ep/M
2	Ports 3 & 4 External	Lo	Hi	Lo	E	I	E	Ep/M
1		Lo	Lo	Hi	I	I	E	Ep/M
0	Test Data Outputted from ROM & ROM to I/O Port 3	Lo	Lo	Lo	I	I	I*	Ep/M

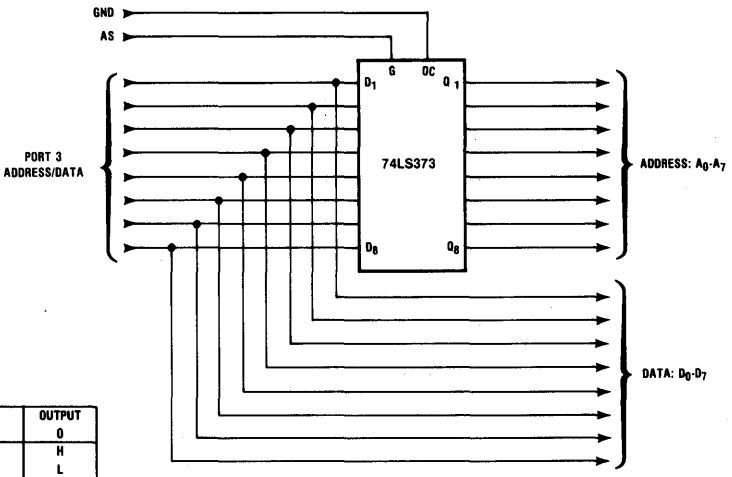
E—EXTERNAL all vectors are external
I—INTERNAL
Ep—EXPANDED MULTIPLEXED

*First two addresses read from external after reset
(1) Address for RAM XX80-XXFF
(2) ROM disabled

Lower Order Address Bus Latches

Since the data bus is multiplexed with the lower order address bus in Port 3, latches are required to latch those address bits. The SN74LS373 Transparent octal D-type latch can be used with the S6801 to latch the least significant address byte. Figure 19 shows how to connect the latch to the S6801. The output control to the LS373 may be connected to ground.

Figure 19. Latch Connection



FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	ENABLE D	OUTPUT Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

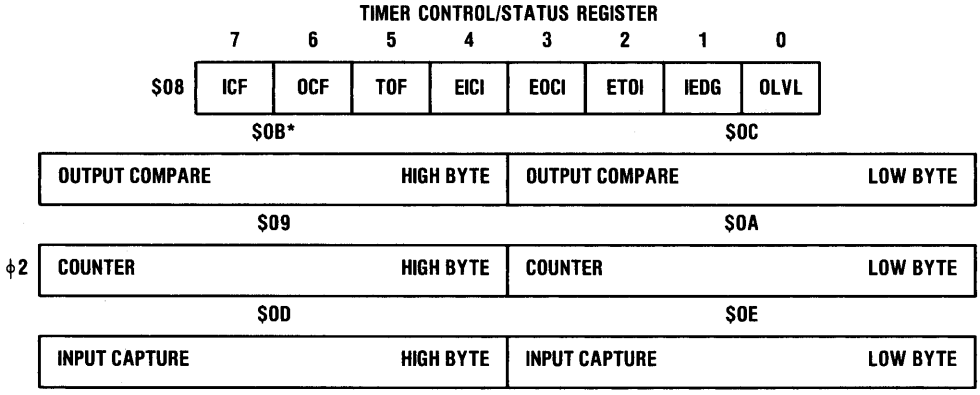
Programmable Timer

The S6801 contains an on-chip 16-bit programmable timer which may be used to perform measurements on an input waveform while independently generating an output waveform. Pulse widths for both input and output signals may vary from a few microseconds to many seconds. The timer hardware consists of

- an 8-bit control and status register
- a 16-bit free running counter
- a 16-bit output compare register, and
- a 16-bit input capture register

A block diagram of the timer registers is shown in Figure 20.

Figure 20. Block Diagram of Timer Registers



*THE CHARACTERS ABOVE THE REGISTERS REPRESENT THEIR ADDRESS IN HEX.

Free Running Counter ($0009:000A)

The key element in the programmable timer is a 16-bit free running counter which is driven to increasing values by the MPUϕ. The counter value may be read by the MPU software at any time. The counter is cleared to zero on RESET and may be considered a read-only register with one exception. Any MPU write to the counter's address ($09) will always result in a preset value of $FFF8 being loaded into the counter regardless of the value involved in the write. The preset feature is intended for testing operation of the part, but may be of value in some applications.

Output Compare Register ($000B:000C)

The Output Compare Register is a 16-bit read/write register which is used to control an output waveform. The contents of this register are constantly compared with the current value of the free running counter. When a match is found a flag is set (OCF) in the Timer Control and Status Register (TCSR) and the current value of the Output Level bit (OLVL) in the TCSR is clocked to the output level register. Providing the Data Direction Register for Port 2, Bit 1 contains a "1" (output), the output level register value will appear on the pin for Port 2 Bit 1. The values in the Output Compare Register and Output level bit may then be changed to control the output level on the next compare value. The Output Compare Register is set to $FFFF during RESET. The Compare function is inhibited for one cycle following a write to the high byte of the Output Compare Register to insure a valid 16-bit value is in the register before a compare is made.

Input Capture Register ($000D:000E)

The Input Capture Register is a 16-bit read-only register used to store the current value of the free running counter when the proper transition of an external input signal occurs. This input transition change required to trigger the counter transfer is controlled by the input Edge bit (EDG) in the TOSR. The Data Direction Register bit for Port 1 Bit 0 should *be clear (zero) in order to gate in the external input signal to the edge defect unit in the timer.

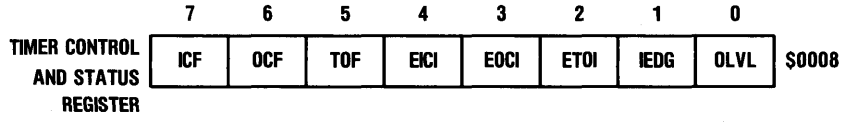
*With Port 2 Bit 0 configured as an output and set to "1". the external input will still be seen by the edge detect unit.

Timer Control and Status Register (TCSR) ($0008)

The Timer Control and Status Register consists of an 8-bit register of which all 8 bits are readable but only the low order 5 bits may be written. The upper three bits contain read-only timer status information and indicate that:

- a proper transition has taken place on the input pin with a subsequent transfer of the current counter value to the input capture register.
- a match has been found between the value in the free running counter and the output compare register, and
- when $0000 is in the free running counter.

Each of the flags may be enabled onto the S6801 internal bus (RO2) with an individual Enable bit in the tCSR. If the 1-bit in the S6801 Condition Code Register has been cleared, a priority vectored interrupt will occur corresponding to the flag bit(s) set. A description for each bit follows:



Bit 0 OLVL — **Output Level**—This value is clocked to the output level register on an output compare. If the DDR for Port 2 bit 1 is set, the value will appear on the output pin.

Bit 1 IEDG — **Input Edge**—This bit controls which transition of an input will trigger a transfer of the counter to the input capture register. The DDR for Port 2 Bit 0 must be clear for this function to operate.
IEDG=0 Transfer takes place on a negative (high-to-low transition).
IEDG=1 Transfer takes place on a positive edge (low-to-high transition).

Bit 2 ETOI — **Enable Timer Overflow Interrupt**—When *set*, this bit enables IRQ2 to occur on the internal bus for a TOF Interrupt; when *clear* the interrupt is inhibited.

Bit 3 EOCI — **Enable Output Compare Interrupt**—When *set*, this bit enables IRQ2 to appear on the internal bus for an input capture interrupt; when *clear* the interrupt is inhibited.

Bit 4 EICI — **Enable Input Capture Interrupt**—When *set*, this bit enables IRQ2 to occur on the internal bus for an input capture interrupt; when *clear* the interrupt is inhibited.

Bit 5 TOF — **Timer Overflow Flag**—This read-only bit is *set* when the counter contains $0000. It is *cleared* by a read of the TCSR (with TOF set) followed by an MPU read of the Counter ($09).

Bit 6 OCF — **Output Compare Flag**—This read-only bit is *set* when a match is found between the output compare register and the free running counter. It is *cleared* by a read of the TCSR (with ODF set) followed by an MPU write to the output compare register ($0B or $0C).

Bit 7 CF — **Input Capture Flag**—This read-only status bit is *set* by a proper transition on the input to the edge detect unit; it is *cleared* by a read of the TCSR (with ICF set) followed by an MPU read of the input Capture Register ($0D).

Serial Communications Interface

The S6801 contains a full-duplex asynchronous serial communications interface (SCI) on board. Two serial data formats (standard mark/space [NRZ] or Bi-phase) are provided at several different data rates. The controller comprises a transmitter and a receiver which operate independently or each other but in the same data format and at the same data rate. Both transmitter and receiver communicate with the MPU via the data bus and with the outside world via pins 2, 3, and 4 of Port 2. The hardware, software, and registers are explained in the following paragraphs.

Wake-up Feature

In a typical multi-processor application, the software protocol will usually contain a destination address in the initial byte(s) of the message. In order to permit non-

selected MPU's to ignore the remainder of the message, a wake-up feature is included whereby all further interrupt processing may be optionally inhibited until the beginning of the next message. When the next messge appears, the hardware re-enables (or "wakes-up") for the next message. The "wake-up" is automatically triggered by a string of ten consecutive 1's which indicates an idle transmit line. The software protocol must provide for the short idle period between any two consecutive messages.

Programmable Options

The following features of the S6801 serial I/O section have programmable:

- format—standard mark/space (NRZ) or Bi-phase
- clock—external or internal
- baud rate—one of 14 per given MPUϕ2 clock frequency or external clock X8 input
- wake-up feature—enabled or disabled
- interrupt requests—enabled or masked indivually for transmitter and receiver data registers
- clock output—internal clock enabled or disabled to Port 2 (Bit 2)
- Port 2 (bits 3 and 4)—dedicated or not dedicated to serial I/O individually for transmitter and receiver

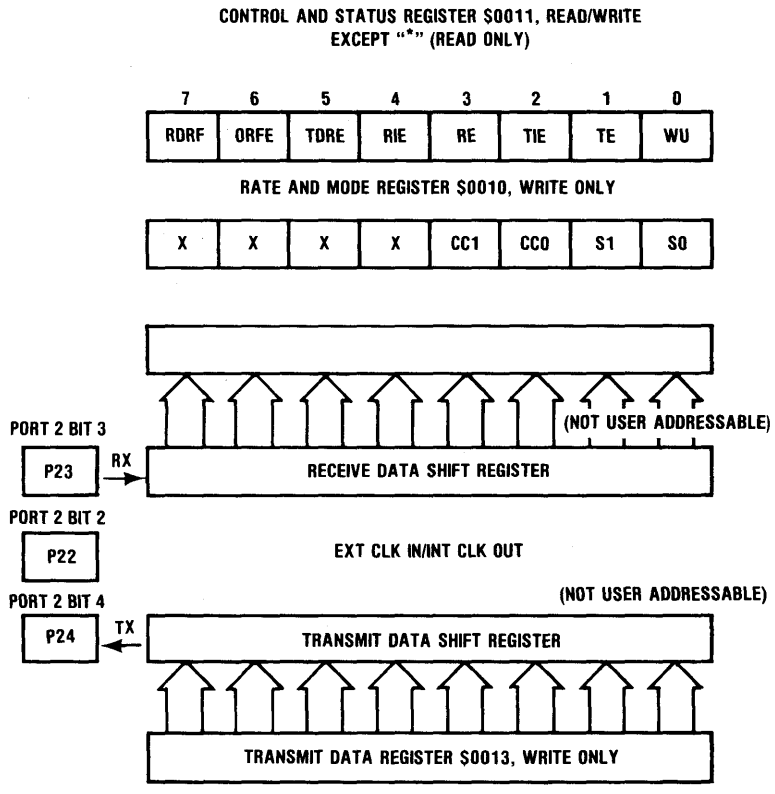
Serial Communications Hardware

The serial communications hardware is controlled by 4 registers as shown in Figure 21. The registers include:

- an 8-bit control and status register
- a 4-bit rate and mode control register (write only)
- an 8-bit read-only receive data register and
- an 8-bit write-only transmit data register

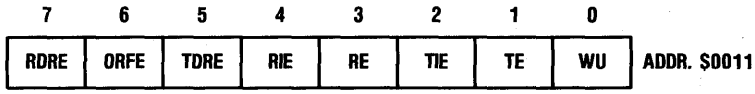
In addition to the four registers, the serial I/O section utilizes bit 3 (serial input) and bit 4 (serial output) or Port 2. Bit 2 of Port 2 is utilized if the internal-clock-out or external-clock-in options are selected.

Figure 21. Serial I/O Registers



Transmit/Receive Control and Status (TRCS) Register

The TRCS register consists of an 8-bit register of which all 8 bits may be read while only bits 0-4 may be written. The register is initialized to $20 on $\overline{\text{RESET}}$. The bits in the TRCS register are defined as follows:



Bit 0 WU — **"Wake-up on Next Message**—set by S6801 software cleared by hardware on receipt of ten consecutive 1's.

Bit 1 TE — **Transmit Enable**—set by S6801 to produce preamble of nine consecutive 1's and to enable gating of transmitter output to Port 2, bit 4 regardless of the DDR value corresponding to this bit; when clear, serial I/O has no effect on Port 2 bit 4.

Bit 2 TIE — **Transmit Interrupt Enable**—when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur when bit 5 (TDRE) is set; when clear, the TDRE value is masked from the bus.

Bit 3 RE — **Receiver Enable**—when set, gates Port 2 bit 3 to input of receiver regardless of DDR value for this bit; when clear, serial I/O has no effect on Port 2 bit 3.

Bit 4 RIE — **Receiver Interrupt Enable**—when set, will permit an $\overline{\text{IRQ2}}$ interrupt to occur when bit 7 (RDRF) or bit 6 (OR) is set; when clear, the interrupt is masked.

Bit 5 TDRE — **Transmit Data Register Empty**—set by hardware when a transfer is made from the transmit data register to the output shift register. The TDRE bit is cleared by reading the status register, then writing a new byte into the transmit data register, TDRE is initialized to 1 by $\overline{\text{RESET}}$.

Bit 6 ORFE — **Over-Run-Framing Error**—set by hardware when an overrun or framing error occurs (receive only). An overrun is defined as a new byte received with last byte still in Data Register/Buffer. A framing error has occured when the byte boundaries in bit stream are not synchronized to bit counter. The ORFE bit is cleared by reading the status register, then reading the Receive Data Register, or by $\overline{\text{RESET}}$.

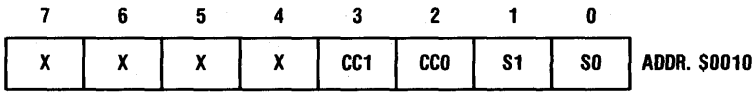
Bit 7 RDRF — **Receiver Data Register Full**—set by hardware when a transfer from the input shift register to the receiver data register is made. The RDRF bit is cleared by reading the status register, then reading the Receive Data Register, or by $\overline{\text{RESET}}$.

Rate and Mode Control Register

The Rate and Mode Control register controls the following serial I/O variables:

- Baud rate
- format
- Clocking source, and
- Port 2 bit 2 configuration

The register consists of 4 bits all of which are write-only and cleared on $\overline{\text{RESET}}$. The 4 bits in the register may be considered as a pair of 2-bit fields. The two low order bits control the bit rate for internal clocking and the remaining two bits control the format and clock select logic. The register definition is as follows:



Bit 0 S0
Bit 1 S1 — **Speed Select**—These bits select the Baud rate for the internal clock. The four rates which may be selected are a function of the MPU $\phi 2$ clock frequency. Table 4 lists the available Baud rate.

Bit 2 CC0
Bit 3 CC1 — **Clock Control and Format Select**—This 2-bit field controls the format and clock select logic. Table 5 defines the bit field.

Table 4. SCI Internal Baud Rates

S1, S0	XTAL	4.0MHz	4.9152MHz	2.5476MHz
	$\phi 2$	1.0MHz	1.2288MHz	0.6144MHz
00	$\phi 2 \div 16$	62.5K BITS/S	76.8K BITS/S	38.4K BITS/S
01	$\phi 2 \div 128$	7,812.5 BITS/S	9,600 BITS/S	4,800 BITS/S
10	$\phi 2 \div 1024$	976.6 BITS/S	1,200 BITS/S	600 BITS/S
11	$\phi 2 \div 4096$	244.1 BITS/S	300 BITS/S	150 BITS/S

Table 5. Bit Field

CC1, CC0	FORMAT	CLOCK SOURCE	PORT 2 BIT 2	PORT 2 BIT 3	PORT 2 BIT 4
00	BI-PHASE	INTERNAL	NOT USED	**	**
01	NRZ	INTERNAL	NOT USED	**	**
10	NRZ	INTERNAL	OUTPUT*	SERIAL INPUT	SERIAL OUTPUT
11	NRZ	EXTERNAL	INPUT	SERIAL INPUT	SERIAL OUTPUT

*CLOCK OUTPUT IS AVAILABLE REGARDLESS OF VALUES FOR BITS RE AND TE.
**BIT 3 IS USED FOR SERIAL INPUT IF RE = "1" IN TRCS; BIT 4 IS USED FOR SERIAL OUTPUT IF TE = "1" IN TRCS.

Internally Generated Clock

If the user wishes for the serial I/O to furnish a clock, the following requirements are applicable:

- the values of RE and TE are immaterial
- CC1, CC0 must be set to 10
- the maximum clock rate will be $\phi \div 16$
- the clock will be at 1× the bit rate and will have a rising edge at mid-bit

Externally Generated Clock

If the user wishes to provide an external clock for the serial I/O, the following requirements are applicable:

- the CC1, CC0, field in the Rate and Mode Control Register must be set to 11.
- the external clock must be set to 8 times (×8) the desired baud rate and
- the maximum external clock frequency is 1.2MHz.

Serial Operations

The Serial I/O hardware should be initialized by the S6801 software prior to operation. This sequence will normally consist of:

- writing the desired operation control bits to the Rate and Mode Control Register and
- writing the desired operational control bits in the Transmit/Receive Control and Status Register.

The Transmitter Enable (TE) and Receiver Enable (RE) bits may be left set for dedicated operations.

Transmit Operations

The transmit operation is enabled by the TE bit in the Transmit/Receive Control and Status Register. This bit when set, gates the output of the serial transmit shift register to Port 2 Bit 4 and takes unconditional control

over the Data Direction Register value for Port 2, Bit 4.

Following a $\overline{\text{RESET}}$, the user should configure both the Rate and Mode Control Register and the Transmit/Receiver Control and Status Register for desired operation. Setting the TE bit during this procedure initiates the serial output by first transmitting a ten-bit preamble of 1's. Following the preamble, internal synchronization is established and the transmitter section is ready for operation.

At this point one of two situations exist:

a) if the Transmit Data Register is empty (TDRE = 1), a continuous string of ones will be sent indicating an idle line, or
b) if data has been loaded into the Transmit Data Register (TDRE = 0), the word is transferred to the output shift register and transmission of the data word will begin.

During the transfer itself, the 0 start bit is first transmitted. Then the 8 data bits (beginning with bit 0) followed by the stop bit, are transmitted. When the Transmitter Data Register has been emptied, the hardware sets the TDRE flag bit.

If the S6801 fails to respond to the flag within the proper time, (TDRE is still set when the next normal transfer from the parallel data register to the serial output register should occur) then a 1 will be sent (instead of a 0) at "Start" bit time, followed by more 1's until more data is supplied to the data register. No 0's will be sent while TDRE remains a 1.

The Bi-phase mode operates as described above except that the serial output toggles each bit time, and on 1/2 bit times when a 1 is sent.

Receive Operation

The receive operation is enabled by the RE bit which gates in the serial input through Port 2 Bit 3. The receiver section operation is conditioned by the contents of the Transmit/Receive Control and Status Register and the Rate and Mode Control Register.

The receiver bit interval is divided into 8 sub-intervals for internal synchronization. In the standard, non-Bi-phase mode, the received bit stream is synchronized by the first 0 (space) encountered.

The approximate center of each bit time is strobed during the next 10 bits. If the tenth bit is not a 1 (stop bit) a framing error is assumed, and bit ORFE is set. If the tenth bit is 1, the data is transferred to the Receiver Data Register, and interrupt flag RDRF is set. If RDRF is still set at the next tenth bit time, ORFE will be set, indicating an over-run has occurred. When the S6801 responds to either flag (RDRF or ORFE) by reading the status register followed by reading the Data Register RDRF (or ORFE) will be cleared.

Ram Control Register

This register, which is addressed at $0014, gives status information about the standby RAM. A 0 in the RAM enable bit (RAM E) will disable the standby RAM, thereby protecting it at power down if V_{CC} is held greater than V_{SBB} volts, as explained previously in the signal description for V_{CC} Standby.

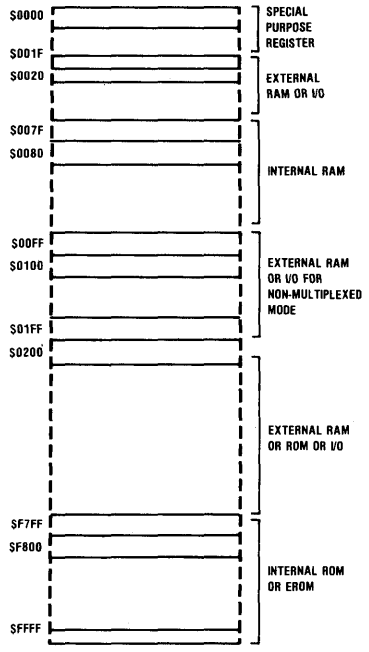
$0014	STAND-BY BIT	RAM E	X	X	X	X	X	X

Bit 1 Not used.
Bit 2 Not used.
Bit 3 Not used.
Bit 4 Not used.
Bit 5 Not used
Bit 6 The RAM ENABLE control bit allows the user the ability to disable the standby RAM. This bit is set to a logic "one" by reset which enables the standby RAM and can be written to or zero under program control. When the RAM is disabled, logic "zero", data is read from external memory.
Bit 7 The STANDBY BIT of the control register, $0014, is cleared when the standby voltage is removed. This bit is a read/write status flag that the user can read which indicates that the standby RAM voltage has been applied, and the data in the standby RAM is valid.

The S6801 provides up to 65K bytes of memory for program and/or data storage. The memory map is shown in Figure 22.

Locations $0020 through $007F access external RAM or I/O Internal RAM is accessed at $0080 through $00FF. The RAM may be alternately selected by mask programming at location $A000. However, if the user desires to access external RAM at those locations he may do so by clearing the RAM ENABLE control bit of the RAM Control Register. In this way an extra 126 bytes of external RAM are available. The first 64 bytes of the 128 bytes of on-chip RAM are provided with a separate power supply. This will maintain the 64 bytes of RAM in the power down mode as explained in the pin description for V_{CC} Standby.

Figure 22. Memory Map



Locations $0100 through $01FF are available in the Expanded Non-Multiplexed Mode. The eight address lines of Port 4 make this 256 word expandability possible. Those not needed for address lines can be used as input lines instead.

The full range of addresses available to the user is in the Expanded Multiplexed Mode. Locations $0200 through $F7FF can be used as external RAM, external ROM, or I/O. Any higher order bit not required for addressing can be used as I/O as in the Expanded Non-Multiplexed Mode.

The internal ROM is located at $F800 through $FFFF. The decoder for the ROM may be mask programmed on A12, and A13 as zeros or one's to provide for $C800, $D800, $E800 for the ROM address. A12 and A13 may also be don't care in this decoder. The primary address for the ROM will be $F800.

The first 32 bytes are for the special purpose registers as shown in Table 6.

Table 6. Special Registers

HEX ADDRESS	REGISTER
00	DATA DIRECTION 1
01	DATA DIRECTION 2
02	I/O PORT 1
03	I/O PORT 2
04	DATA DIRECTION 3
05	DATA DIRECTION 4
06	I/O PORT 3
07	I/O PORT 4
08	TCSR
09	COUNTER HIGH BYTE
0A	COUNTER LOW BYTE
0B	OUTPUT COMPARE HIGH BYTE
0C	OUTPUT COMPARE LOW BYTE
0D	INPUT CAPTURE HIGH BYTE
0E	INPUT CAPTURE LOW BYTE
0F	I/O PORT 3 C/S REGISTER
10	SERIAL RATE AND MODE REGISTER
11	SERIAL CONTROL AND STATUS REGISTER
12	SERIAL RECEIVER DATA REGISTER
13	SERIAL TRANSMIT DATA REGISTER
14	RAM/EROM CONTROL REGISTER
15-1F	RESERVED

Figure 23. Memory Map for Interrupt Vectors

	VECTOR MS	VECTOR LS	DESCRIPTION
Highest Priority	FFFE,	FFFF	Restart
	FFFC,	FFFD	Non-Maskable Interrupt
	FFFA,	FFFD	Software Interrupt
	FFF8,	FFF9	IRQ1/Interrupt Strobe S
	FFF6,	FFF7	IRQ2/Timer Input Capture
	FFF4,	FFF5	IRQ2/Timer Output Compare
	FFF2,	FFF3	IRQ2/Timer Overflow
Lowest Priority	FFF0,	FFF1	IRQ2/Serial I/O Interrupt

General Description of Instruction Set

The S6801 is upward object code compatible with the S6800 as it implements the full S6800 instruction set. The execution times of key instructions have been reduced to increase throughput. In addition, new instructions have been added; these include 16-bit operations and a hardware multiply.

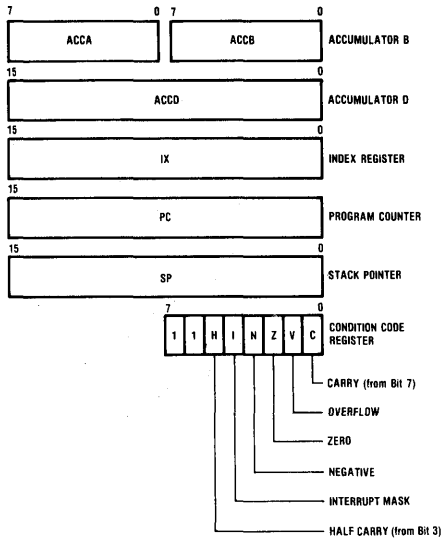
Included in the instruction set section are the following:

- MPU Programming Model (Figure 24)
- Addressing modes
- Accumulator and memory instructions—Table 7
- New instructions
- Index register and stack manipulations—Table 8
- Jump and branch instructions—Table 9
- Special operations—Figure 25
- Condition code register manipulation instructions—Table 10
- Instruction Execution times in machine cycles—Table 11
- Summary of cycle by cycle operation—Table 12

MPU Programming Model

The programming model for the S6801 is shown in Figure 24. The double (D) accumulator is physically the same as the A Accumulator concatenated with the B Accumulator so that any operation using accumulator D will destroy information in A and B.

Figure 24. MCU Programming Model



MPU Addressing Modes

The S6801 eight-bit microcomputer unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 11 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 4MHz, these times would be microseconds.

Accumulator (ACCX) Addressing—In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

Immediate Addressing—In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MCU addresses this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Direct Addressing—In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two-byte instructions.

Extended Addressing—In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight-bits of the address for the operand. This is an absolute address in memory. These are three-byte instructions.

Indexed Addressing—In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MCU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

Implied Addressing—In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one-byte instructions.

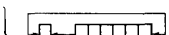
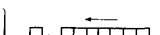
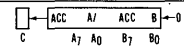
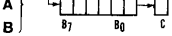
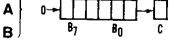
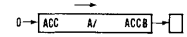
Relative Addressing—In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of −125 to +120 bytes of the present instruction. These are two-byte instructions.

Table 7. Accumulator & Memory Instructions

ACCUMULATOR AND MEMORY		ADDRESSING MODES																5	4	3	2	1	0
		IMMED.			DIRECT			INDEX			EXTEND			INHERENT									
Operations	**MNEMONIC**	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**OP**	~	#	**Boolean/Arithmetic Operation**	**H**	**I**	**N**	**Z**	**V**	**C**
ADD	ADDA	8B	2	2	9B	3	2	AB	4	2	BB	4	3				A + M→A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	4	2	FB	4	3				B + M→B	↕	•	↕	↕	↕	↕
ADD DOUBLE	ADDD	C3	4	3	D3	5	2	E3	6	2	F3	6	3				A:B + M:M + 1→A:B	•	•	↕	↕	↕	↕
ADD ACCUMULATORS	ABA													1B	2	1	A + B→A	↕	•	↕	↕	↕	↕
ADD WITH CARRY	ADCA	89	2	2	99	3	2	A9	4	2	B9	4	3				A + M + C→A		•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	4	2	F9	4	3				B + M + C→B		•	↕	↕	↕	↕
AND	ANDA	84	2	2	94	3	2	A4	4	2	B4	4	3				A M→A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	4	2	F4	4	3				B M→B	•	•	↕	↕	R	•
BIT TEST	BIT A	85	2	2	95	3	2	A5	4	2	B5	4	3				A M	•	•	↕	↕	R	•
	BIT B	C5	2	2	D5	3	2	E5	4	2	F5	4	3				B M	•	•	↕	↕	R	•
CLEAR	CLR							6F	6	2	7F	6	3				00 →M	•	•	R	S	R	R
	CLRA													4F	2	1	00 →A	•	•	R	S	R	R
	CLRB													5F	2	1	00 →B	•	•	R	S	R	R
COMPARE	CMPA	81	2	2	91	3	2	A1	4	2	B1	4	3				A − M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	4	2	F1	4	3				B − M	•	•	↕	↕	↕	↕
COMPARE ACCUMULATORS	CBA													11	2	1	A − B	•	•	↕	↕	↕	↕
COMPLEMENT, 1'S	COM							63	6	2	73	6	3				M→M	•	•	↕	↕	R	S
	COMA													43	2	1	A→A	•	•	↕	↕	R	S
	COMB													53	2	1	B→B	•	•	↕	↕	R	S
COMPLEMENT, 2'S	NEG							60	6	2	70	6	3				0C − M→M	•	•	↕	↕	①	②
(NEGATE)	NEGA													40	2	1	00 − A→A	•	•	↕	↕	①	②
NEGB														50	2	1	00 − B→B	•	•	↕	↕	①	②
DECIMAL ADJUST, A	DAA													19	2	1	Converts binary add of BCD characters into BCD format	•	•	↕	↕	↕	③
DECREMENT	DEC							6A	6	2	7A	6	3				M − 1→M	•	•	↕	↕	④	•
	DECA													4A	2	1	A − 1→A	•	•	↕	↕	④	•
	DECB													5A	2	1	B − 1→B	•	•	↕	↕	④	•
EXCLUSIVE OR	EORA	88	2	2	98	3	2	A8	4	2	B8	4	3				A⊕M→A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	4	2	F8	4	3				B⊕M→B	•	•	↕	↕	R	•
INCREMENT	INC							9C	6	2	7C	6	3				M + 1→M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1→A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1→B	•	•	↕	↕	⑤	•
LOAD ACCUMULATOR	LDAA	86	2	2	96	3	2	A6	4	2	B6	4	3				M→A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	4	2	F6	4	3				M→B	•	•	↕	↕	R	•
LOAD DOUBLE ACCUMULATOR	LDAD	CC	3	3	DC	4	2	EC	5	2	FC	5	3				M + A M + 1→B	•	•	↕	↕	R	•
MULTIPLY UNSIGNED	MUL													3D	10	1	A × B→AB	•	•	•	•	•	⑫
OR, INCLUSIVE	ORAA	8A	2	2	9A	3	2	AA	4	2	BA	4	3				A + M→A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	4	2	FA	4	3				B + M→B	•	•		↕	•	•

The Condition Code Register notes are listed after Table 10.

Table 7. Accumulator & Memory Instructions (Continued)

ACCUMULATOR AND MEMORY		ADDRESSING MODES																		
		IMMED.			DIRECT			INDEX			EXTEND			INHERENT			5	4	3	2	1	0
Operations	**MNEMONIC**	**OP**	**~**	**#**	**OP**	**~**	**#**	**OP**	**~**	**#**	**OP**	**~**	**#**	**OP**	**~**	**#**	**Boolean/Arithmetic Operation**	**H**	**I**	**N**	**Z**	**V**	**C**
PUSH DATA	PSHA													36	3	1	$A \rightarrow M_{SP}$ $SP-1 \rightarrow SP$	•	•	•	•	•	•
	PSHB													37	3	1	$B \rightarrow M_{SP}$ $SP-1 \rightarrow SP$	•	•	•	•	•	•
PULL DATA	PULA													33	4	1	$SP+1 \rightarrow SP$, $M_{SP} \rightarrow A$	•	•	•	•	•	•
	PULB													33	4	1	$SP+1 \rightarrow SP$, $M_{SP} \rightarrow B$	•	•	•	•	•	•
ROTATE LEFT	ROL							69	6	2	79	6	3				M	•	•	↕	↕	⑥	↕
	ROLA													49	2	1	A 	•	•	↕	↕	⑥	↕
	ROLB													59	2	1	B C b_7 b_0	•	•	↕	↕	⑥	↕
ROTATE RIGHT	ROR							66	6	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A 	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B C b_7 b_0	•	•	↕	↕	⑥	↕
SHIFT LEFT Arithmetic	ASL							66	6	2	78	6	3				M	•	•	↕	↕	⑥	↕
	ASLA													48	2	1	A 	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B C b_7 b_0 0	•	•	↕	↕	⑥	↕
DOUBLE SHIFT LEFT, Arithmetic	ASLD													05	3	1	 C A_7 A_0 B_7 B_0	•	•	↕	↕	⑥	•
SHIFT RIGHT Arithmetic	ASR							67	6	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A 	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B B_7 B_0 C	•	•	↕	↕	⑥	↕
SHIFT RIGHT, LOGICAL	LSR							64	6	2	74	6	3				M	•	•	↕	↕	⑥	↕
	LSRA													44	2	1	A 0 	•	•	↕	↕	⑥	↕
	LSRB													54	2	1	B B_7 B_0 C			↕	↕		↕
DOUBLE SHIFT RIGHT LOGICAL	LSRD													04	3	1	0 ACC A/ ACCB C  A7 A0 B7 B0	•	•	R	↕	⑤	↕
																		•	•	R	↕	6	↕
STORE ACCUMULATOR	STAA				97	3	2	A7	4	2	B7	4	3				A→M	•	•	↕	↕	R	•
	STAB				D7	3	2	E7	4	2	B7	4	3				B→M	•	•	↕	↕	R	•
STORE DOUBLE ACCUMULATOR	STAD				DD	4	2	ED	5	2	FD	5	3				A→M B→M+1	•	•	↕	↕	R	•
SUBTRACT	SUBA	80	2	2	90	3	2	A0	4	2	B0	4	3				A−M→A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	4	2	F0	4	3				B−M→B	•	•	↕	↕	↕	↕
DOUBLE SUBTRACT	SUBD	83	4	3	93	5	2	A3	6	2	B3	6	3				A:B−M:M+1→AB	•	•	↕	↕	↕	↕
SUBTRACT ACCUMULATORS	SBA													10	2	1	A−B→A	•	•	↕	↕	↕	↕
SUBTRACT WITH CARRY	SBCA	82	2	2	92	3	2	A2	4	2	B2	4	3				A−M−C→A	•	•	↕	↕	↕	↕
	SBCD	C2	2	2	D2	2	2	E2	4	2	F2	4	3				B−M−C→B	•	•	↕	↕	↕	↕
TRANSFER ACCUMULATORS	TAB													16	2	1	A→B	•	•	↕	↕	R	•
	TBA													16	2	1	A→B	•	•	↕	↕	R	•
TEST ZERO OR MINUS	TST							6D	6	2	7D	6	3				M−00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B−00	•	•	↕	↕	R	R

The Condition Code Register notes are listed after Table 10.

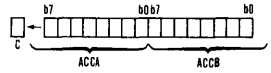
Added Instructions

In addition to the existing S6800 Instruction Set, the following new instructions are incorporated in the S6801 Microcomputer.

ABX Adds the 8-bit unsigned accumulator B to the 16-bit X-Register taking into account the possible carry out of the low order byte of the X-Register. IX←IX + ACCB

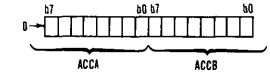
ADDD Adds the double precision ACCD* to the double precision value M:M+1 and places the results in ACCD. ACCD←(ACCD)+(M:M+1)

ASLD Shifts all bits of ACCAB one place to the left. Bit 0 is loaded with zero. The C bit is loaded from the most significant bit of ACCD.



LDD Loads the contents of double precision memory location into the double accumulator A:B. The condition codes are set according to the data. ACCD←(M:M+1)

LSRD Shifts all bits of ACCD one place to the right. Bit 15 is loaded with zero. The C bit is loaded from the least significant bit to ACCD.



MUL Multiplies the 8 bits in accumulator A with the 8 bits in accumulator B to obtain a 16-bit unsigned number in A:B. ACCA contains MSB of result. ACCD←ACCA *ACCB

PSHX The contents of the index register is pushed onto the stack at the address contained in the stack pointer. The stack pointer is decremented by 2. ↓(IXL), SP←(SP)−1
↓(IXH), SP←(SP)−1

PULX The index register is pulled from the stack beginning at the current address contained in the stack pointer +1. The stack pointer is incremented by 2 in total. SP←(SP)+1; IXH
SP←(SP)+1; IHL

STD Stores the contents of double accumulator A:B in memory. The contents of ACCD remain unchanged. M:M+1←(ACCD)

*ACCD is the 16-bit register (A:B) formed by concatenating the A and B accumulators. The A-accumulator is the most significant byte.

Table 8. Index Register and Stack Manipulation Instructions

POINTER OPERATIONS	MNEMONIC	IMMED. OP	IMMED. ~	IMMED. #	DIRECT OP	DIRECT ~	DIRECT #	INDEX OP	INDEX ~	INDEX #	EXTEND OP	EXTEND ~	EXTEND #	IMPLIED OP	IMPLIED ~	IMPLIED #	Boolean/Arithmetic Operation	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Compare Index Reg	CPX	8C	4	3	9C	5	2	AC	6	2	BC	6	3				$X_H - M, X_L - (M+1)$	•	•	⑦	‡	⑧	•
Decrement Index Reg	DEX													09	3	1	X − 1→X	•	•	•	‡	•	•
Decrement Stack Pointer	DES													34	3	1	SP − 1→SP	•	•	•	•	•	•
Increment Index Reg	INX													08	3	1	X + 1→X	•	•	•	‡	•	•
Increment Stack Pointer	INS													31	3	1	1SP + 1→SP	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	5	2	FE	5	3				$M→X_H, (M+1)→X_L$	•	•	⑨	‡	R	•
Load Stack Pointer	LDS	8E	3	3	9E	4	2	AE	5	2	BE	5	3				$M→SP_H, (M+1)→SP_L$	•	•	⑨	‡	R	•
Store Index Reg	STX				DF	4	2	EF	5	2	FF	5	3				$X_H→M, X_L→(M+1)$	•	•	⑨	‡	R	•
Store Stack Pointer	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H→M, SP_L→(M+1)$	•	•	⑨	‡	R	•
Index Reg→Stack Pointer	TXS													35	3	1	X − 1→SP	•	•	•	•	•	•
Stack Pointer→Index Reg	TSX													30	3	1	SP + 1→X	•	•	•	•	•	•
Add	ABX													3A	3	1	B + X→X	•	•	•	•	•	•
Push Data	PSHX													3C	3	1	$X_L→M_{SP}$, SP − 1→SP $X_H→H_{SP}$, SP − 1→SP	•	•	•	•	•	•
Pull Data	PULX													30	5	1	SP + 1→SP, $M_{SP}→X_H$ SP + 1→SP, $M_{SP}→X_L$	•	•	•	•	•	•

The Condition Code Register notes are listed after Table 10

Table 9. Jump and Branch Instructions

OPERATIONS	MNEMONIC	RELATIVE OP	RELATIVE ~	RELATIVE #	INDEX OP	INDEX ~	INDEX #	EXTND OP	EXTND ~	EXTND #	IMPLIED OP	IMPLIED ~	IMPLIED #	BRANCH TEST	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = 0	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										N⊕ V = 0	•	•	•	•	•	•
Branch If >Zero	BGT	2E	4	2										Z + (N⊕ V) = 0	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										C + Z = 0	•	•	•	•	•	•
Branch If≤Zero	BLE	2F	4	2										Z + (N ⊕ V) = 1	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										C + Z = 1	•	•	•	•	•	•
Branch If< Zero	BLT	2D	4	2										N ⊕ V = 1	•	•	•	•	•	•
Branch If Minus	BMI	28	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	20	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	8D	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		(10)					
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait For Interrupt*	WAI										3E	9	1		•	(11)	•	•	•	•

Table 10. Condition Code Register Manipulation Instructions

OPERATIONS	MNEMONIC	IMPLIED OP	IMPLIED ~	IMPLIED #	BOOLEAN OPERATION	COND. CODE REG. 5 H	4 I	3 N	2 Z	1 V	0 C
Clear Carry	CLC	0C	2	1	0→C	•	•	•	•	•	R
Clear Interrupt Mask	CLI	0E	2	1	0→1	•	R	•	•	•	•
Clear Overflow	CLV	0A	2	1	0→V	•	•	•	•	R	•
Set Carry	SEC	0D	2	1	1→C	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1	1→1	•	S	•	•	•	•
Set Overflow	SEV	0B	2	1	1→V	•	•	•	•	S	•
Accumulator A→CCR	TAP	06	2	1	A→CCR	(12)					
CCR→Accumulator A	TPA	07	2	1	CCR→A	•	•	•	•	•	•

CONDITION CODE REGISTER NOTES: (Bit set if test is true and cleared otherwise).

1 (Bit V) Test Result = 10000000?
2 (Bit C) Test Result = 00000000?
3 (Bit C) Test: Decimal value of most significant BCD Character greater than nine? (Not cleared if previously set.)
4 (Bit V) Test: Operand = 10000000 prior to execution?
5 (Bit V) Test: Operand = 01111111 prior to execution?
6 (Bit V) Test: Set equal to result of N⊕C after shift has occurred.
7 (Bit N) Test: Sign Bit of most significant (MS) byte = 1?
8 (Bit V) Test: 2's complement overflow from subtraction of MS bytes?
9 (Bit N) Test: Result less than zero? (Bit 15 = 1)
10 (All) Load Condition Code Register from Stack. (See Special Operations)
11 (Bit I) Set when interrupt occurs. If previously set, a Non-Maskable Interrupt as required to exit the wait state.
12 (All) Set according to the contents of Accumulator A.

Figure 25. Special Operations

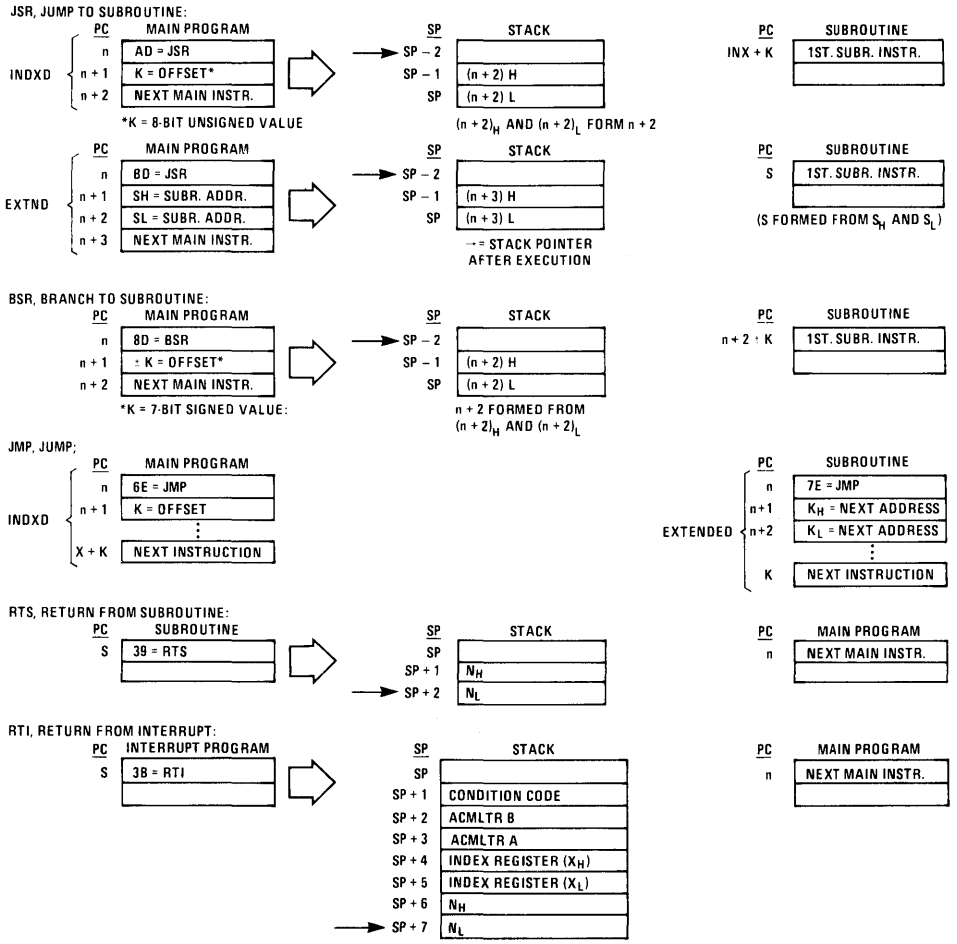


Table 11. Instruction Execution Times in Machine Cycle

	ACCX	IMMEDIATE	DIRECT	EXTENDED	INDEXED	INHERENT	RELATIVE		ACCX	IMMEDIATE	DIRECT	EXTENDED	INDEXED	INHERENT	RELATIVE
ABA	•	•	•	•	•	2	•	INX	•	•	•	•	•	3	•
ABX	•	•	•	•	•	3	•	JMP	•	•	•	3	3	•	•
ADC	•	2	3	4	4	•	•	JSR	•	•	5	6	6	•	•
ADD	•	2	3	4	4	•	•	LDA	•	2	3	4	4	•	•
ADDD	•	4	5	6	6	•	•	LDD	•	3	4	5	5	•	•
AND	•	2	3	4	4	•	•	LDS	•	3	4	5	5	•	•
ASL	2	•	•	6	6	•	•	LDX	•	3	4	5	5	•	•
ASLD	•	•	•	•	•	3	•	LSR	2	•	•	6	6	•	•
ASR	2	•	•	6	6	•	•	LSRD	•	•	•	•	•	3	•
BCC	•	•	•	•	•	•	3	MUL	•	•	•	•	•	10	•
BCS	•	•	•	•	•	•	3	NEG	2	•	•	6	6	•	•
BEQ	•	•	•	•	•	•	3	NOP	•	•	•	•	•	2	•
BGE	•	•	•	•	•	•	3	ORA	•	2	3	4	4	•	•
BGT	•	•	•	•	•	•	3	PSH	3	•	•	•	•	•	•
BHI	•	•	•	•	•	•	3	PSHX	•	•	•	•	•	4	•
BIT	•	2	3	4	4	•	•	PUL	4	•	•	•	□	•	•
BLE	•	•	•	•	•	•	3	PULX	•	•	•	•	•	5	•
BLS	•	•	•	•	•	•	3	ROL	2	•	•	6	6	•	•
BLT	•	•	•	•	•	•	3	ROR	2	•	•	6	6	•	•
BMI	•	•	•	•	•	•	3	RTI	•	•	•	•	•	10	•
BNE	•	•	•	•	•	•	3	RTS	•	•	•	•	•	6	•
BPL	•	•	•	•	•	•	3	SBA	•	•	•	•	•	2	•
BRA	•	•	•	•	•	•	3	SBC	•	2	3	4	4	•	•
BSR	•	•	•	•	•	•	6	SEC	•	•	•	•	•	2	•
BVC	•	•	•	•	•	•	3	SEI	•	•	•	•	•	2	•
BVS	•	•	•	•	•	•	3	SEV	•	•	•	•	•	2	•
CBA	•	•	•	•	•	2	•	STA	•	•	3	4	4	•	•
CLC	•	•	•	•	•	2	•	STD	•	•	4	5	5	•	•
CLI	•	•	•	•	•	2	•	STS	•	•	4	5	6	•	•
CLR	2	•	•	6	6	•	•	STX	•	•	4	5	5	•	•
CLV	•	•	•	•	•	2	•	SUB	•	4	5	6	6	•	•
CMP	•	2	3	4	4	•	•	SUBD	•	4	5	6	6	•	•
COM	2	•	•	6	6	•	•	SWI	•	•	•	•	•	12	•
CPX	•	4	5	6	6	•	•	TAB	•	•	•	•	•	2	•
DAA	•	•	•	•	•	2	•	TAP	•	•	•	•	•	2	•
DEC	2	•	•	6	6	•	•	TBA	•	•	•	•	•	2	•
DES	•	•	•	•	•	3	•	TPA	•	•	•	•	•	2	•
DEX	•	•	•	•	•	3	•	TST	•	•	•	6	6	•	•
EOR	•	2	3	4	4	•	•	TSX	•	•	•	•	•	2	•
INC	2	•	•	6	6	•	•	TXS	•	•	•	•	•	3	•
INS	•	•	•	•	•	3	•	WAI	•	•	•	•	•	9	•

S6802/A/B/S6808/A/B

MICROPROCESSOR WITH CLOCK AND RAM

Features

- ☐ On-Chip Clock Circuit
- ☐ 128x8-Bit On-Chip RAM (S6802)
- ☐ 32 Bytes of RAM Are Retainable (S6802)
- ☐ Software-Compatible With the S6800
- ☐ Expandable to 65K Words
- ☐ Standard TTL-Compatible Inputs and Outputs
- ☐ 8-Bit Word Size
- ☐ 16-Bit Memory Addressing
- ☐ Interrupt Capability
- ☐ Clock Rates:
  S6802/S6808—1.0MHz
  S68A02/S68A08—1.5MHz
  S68B02/S68B08—2.0MHz

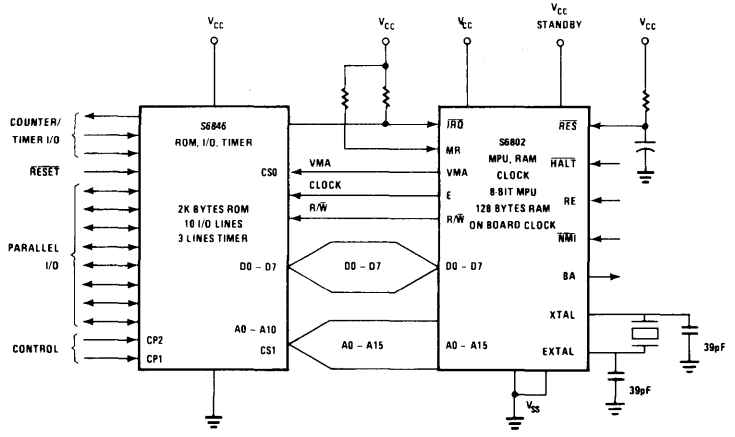
General Description

The S6802/S6808 are monolithic 8-bit microprocessors that contain all the registers and accumulators of the present S6800 plus an internal clock oscillator and driver on the same chip. In addition, the S6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007E. The first 32 bytes of RAM, at addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation. The S6808 is functionally identical to the S6802 except for the 128 bytes of RAM. The S6808 does not have any RAM.

The S6802/S6808 are completely software compatible with the S6800 as well as the entire S6800 family of parts. Hence, the S6802/S6808 are expandable to 65K words. When the S6802 is interfaced with the S6846 ROM-I/O-Timer chip, as shown in the Block Diagram below, a basic 2-chip microcomputer system is realized.

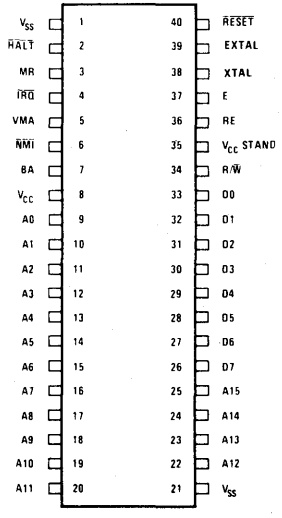
S6800

Typical Microcomputer Block Diagram



BLOCK DIAGRAM OF A TYPICAL COST EFFECTIVE MICROCOMPUTER. THE MPU IS THE CENTER OF THE MICROCOMPUTER SYSTEM AND IS SHOWN IN A MINIMUM SYSTEM INTERFACING WITH A ROM COMBINATION CHIP. IT IS NOT INTENDED THAT THIS SYSTEM BE LIMITED TO THIS FUNCTION BUT THAT IT BE EXPANDABLE WITH OTHER PARTS IN THE S6800 MICROCOMPUTER FAMILY.

Pin Configuration



Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature Range, T_A	0° to +70°C
Storage Temperature Range, T_{stg}	−55°C to +150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

D.C. Characteristics:

(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	Logic, EXtal	$V_{SS}+2.0$	—	V_{CC}	V
		$\overline{RESET}$	$V_{SS}+4.0$	—	V_{CC}	
V_{IL}	Input Low Voltage	Logic, EXtal, $\overline{RESET}$	$V_{SS}-0.3$	—	$V_{SS}+0.8$	V
I_{IN}	Input Leakage Current (V_{IN}=0 to 5.25V, V_{CC}=Max)	Logic*	—	1.0	2.5	μA
V_{OH}	Output High Voltage					V
	(I_{LOAD}=−205μA, V_{CC}=Min)	D0-D7	$V_{SS}+2.4$	—	—	V
	(I_{LOAD}=−145μA, V_{CC}=Min)	AO-A15, R/$\overline{W}$, VMA, E	$V_{SS}+2.4$	—	—	V
	(I_{LOAD}=−100μA, V_{CC}=Min)	BA	$V_{SS}+2.4$	—	—	V
V_{OL}	Output Low Voltage (I_{LOAD}=1.6mA, V_{CC}=Min)		—	—	$V_{SS}+0.4$	V
P_D	Power Dissipation	(Measured at T_A=0°C)	—	0.600	1.2	W
C_{IN}	Capacitance #					pF
	(V_{IN}=0, T_A=25°C, f=1.0MHz	D0-D7	—	10	12.5	
		Logic Inputs, EXtal	—	6.5	10	
C_{OUT}		A0-A15, R/$\overline{W}$, VMA	—	—	12	pF
V_{CC} Standby	V_{CC}		4.0	—	5.25	V
I_{DD} Standby	I_{DD} Standby		—	—	8.0	mA

Clock Timing (V_{CC}=5.0V±5%, V_{SS}=0, T_A=0°C to +70°C unless otherwise noted)

Symbol	Parameter	S6802/S6808 Min.	S6802/S6808 Typ.	S6802/S6808 Max.	S68A02/S68A08 Min.	S68A02/S68A08 Typ.	S68A02/S68A08 Max.	S68B02/S68B08 Min.	S68B02/S68B08 Typ.	S68B02/S68B08 Max.	Unit
	Frequency of Operation										
f	Input Clock÷4	0.1	—	1.0	0.1	—	1.5	.1	—	2	MHz
f_{Xtal}	Crystal Frequency	1.0	—	4.0	1.0	—	6.0	1.0	—	8	
t_{CYC}	Cycle Time	1.0	—	10	6.7	—	10	.50	—	10	μs
t_ϕ	Fall Time Measured between $V_{SS}+0.4V$ and $V_{SS}-2.4V$	—	—	25	—	—	25	—	—	25	ns

**Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3KΩ pull-up load resistors for wire-OR capability at optimum operation. Does not include Extal and Xtal,* which are crystal inputs.

#Capacitance are periodically sampled rather than 100% tested.

Read/Write Timing (Figures 1 through 5; Load Circuit of Figure 3.)
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	S6802/S6808			S68A02/S68A08			S68B02/S68B08			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AD}	Address Delay C=90pF C=30pF		100	270			180 165			150 135	ns
t_{ACC}	Peripheral Read Access Time	575			360			250			ns
t_{DSR}	Data Setup Time (Read)	100			70			60			ns
t_H	Input Data Hold Time	10	30		10			10			ns
t_{AH}	Address Hold Time (Address, R/W, VMA)	20			20			20			ns
t_{DDW}	Data Delay Time (Write) Processor Controls			225			170			160	ns
t_{PCS}	Processor Control Setup Time	200			140			110			ns
t_{PCr},t_{PCf}	Processor Control Rise and Fall Time			100			100			100	ns

Figure 1. Read Data From Memory or Peripherals

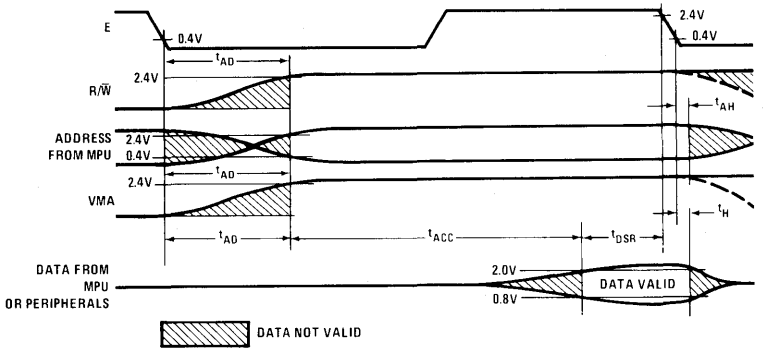


Figure 2. Write Data In Memory or Peripherals

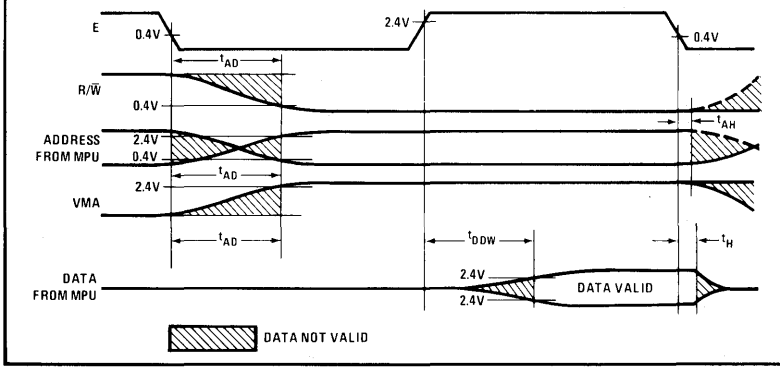
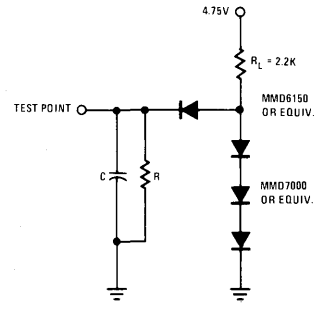


Figure 3. Bus Timing Test Load



C = 130pF FOR D0 – D7, E
= 90pF FOR A0 – A15, R/W, AND VMA
= 30pF FOR BA
R = 11.7 KΩ FOR D0 – D7, E
= 16.5KΩ FOR A0 – A15, R/W, AND VMA
= 24KΩ FOR BA

S6800

Figure 4. Typical Data Bus Output Delay Versus Capacitive Loading

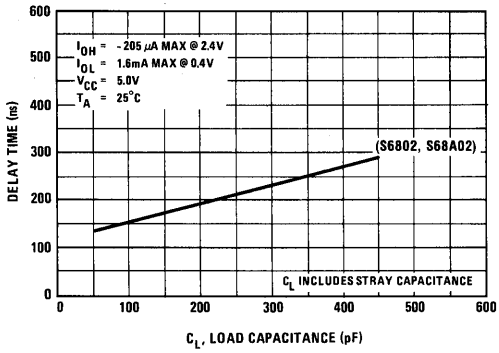


Figure 5. Typical Read/Write, VMA, and Address Output Delay Versus Capacitive Loading

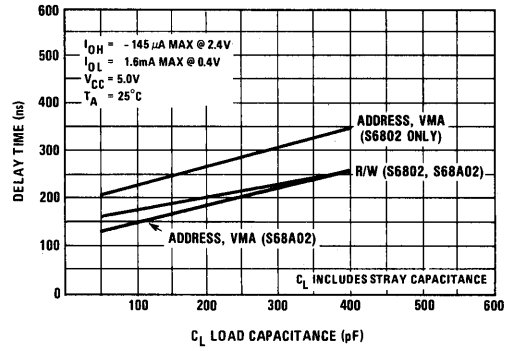
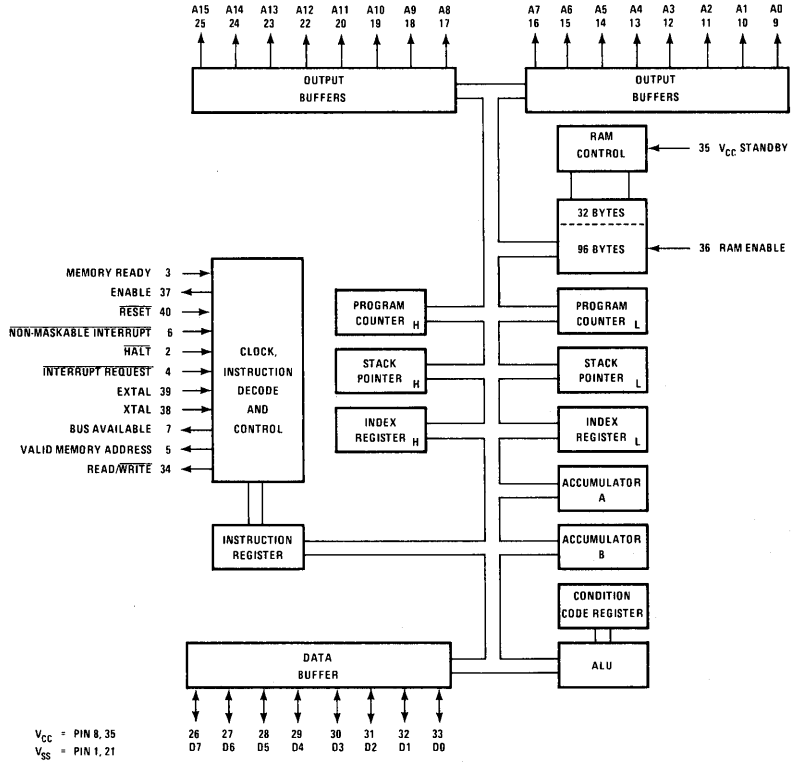


Figure 6. S6802 Expanded Block Diagram



Functional Description

MPU Registers

A general block diagram of the S6802 is shown in Figure 6. As shown, the number and configuration of the registers are the same as for the S6800. The 128x8 bit RAM has been added to the basic MPU. The first 32 bytes may be operated in a low power mode via a V_{CC} standby. These 32 bytes can be retained during power-up and power-down conditions via the RE signal.

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (Figure 7).

Program Counter—The program counter is a two byte (16 bits) register that points to the current program address.

Stack Pointer—The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register—The index register is a two byte register that is used to store data or a sixteen-bit memory address for the Indexed mode of memory addressing.

Accumulators—The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

Condition Code Register—The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and Half Carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The used bits of the Condition Code Register (b6 and b7) are ones.

Figure 8 shows the order of saving the microprocessor status within the stack.

Figure 7. Programming Model of the Microprocessing Unit

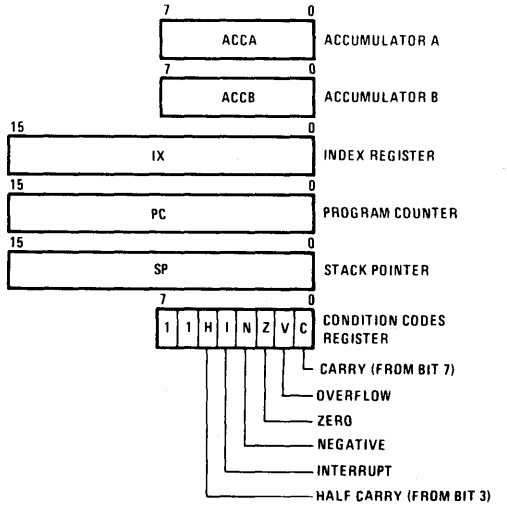
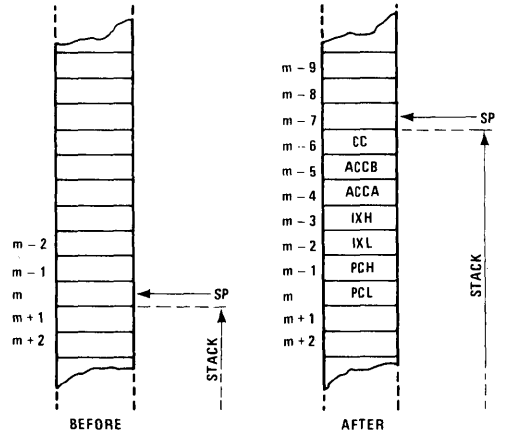


Figure 8. Saving the Status of the Microprocessor in the Stack



SP = STACK POINTER
CC = CONDITION CODES (ALSO CALLED THE PROCESSOR STATUS BYTE)
ACCB = ACCUMULATOR B
ACCA = ACCUMULATOR A
IXH = INDEX REGISTER, HIGHER ORDER 8 BITS
IXL = INDEX REGISTER, LOWER ORDER 8 BITS
PCH = PROGRAM COUNTER, HIGHER ORDER 8 BITS
PCL = PROGRAM COUNTER, LOWER ORDER 8 BITS

S6802/S6808 MPU Description

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor. These control and timing signals for the S6802/S6808 are identical to those of the S6800 except that TSC, DBE, $\phi 1$, $\phi 2$ input, and two unused pins have been eliminated, and the following signal and timing lines have been added:

RAM Enable (RE)
Crystal Connections EXtal and Xtal
Memory Ready (MR)
V_{CC} Standby
Enable $\phi 2$ Output (E)

The following is a summary of the S6802/S6808 MPU signals:

Address Bus (A0-A15)—Sixteen pins are used for the address bus. The outputs are capable of driving one standard TTL load and 130pF.

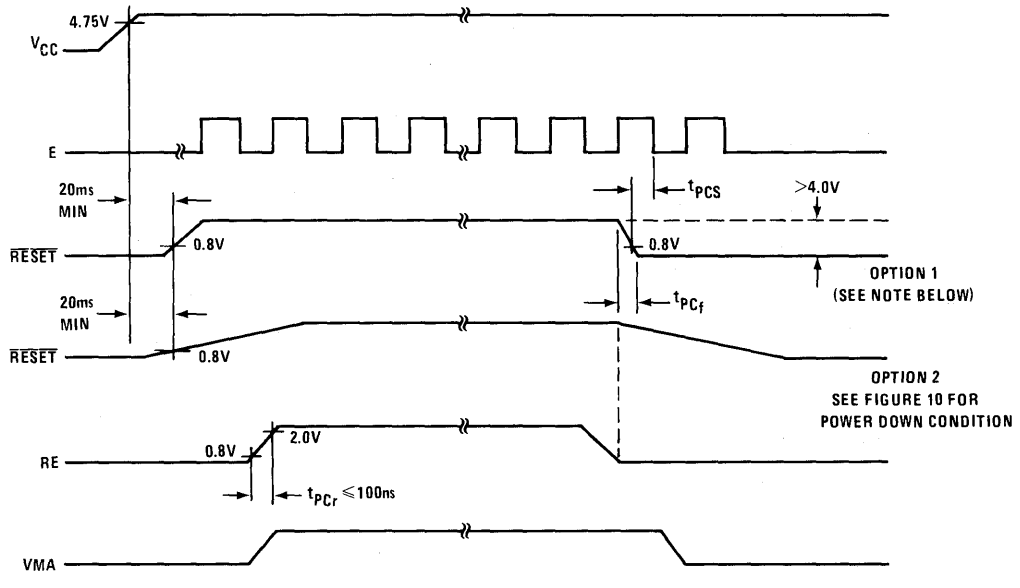
Data Bus (D0-D7)—Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state-output buffers capable of driving one standard TTL load and 130pF.

$\overline{\text{Halt}}$—When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction, Bus Available will be at a high state, Valid Memory Address will be at a low state, and all other three-state lines will be in the three-state mode. The address bus will display the address of the next instruction.

To insure single instruction operation, transition of the $\overline{\text{Halt}}$ line must not occur during the last 200ns of E and the Halt line must go high for one Clock cycle.

Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$)—This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high).

Figure 9. Power-up and Reset Timing



NOTE: IF OPTION 1 IS CHOSEN, $\overline{\text{RESET}}$ AND RE PINS CAN BE TIED TOGETHER.

When the processor is halted, it will be in the logical one state. This output is capable of driving one standard TTL load and 90pF.

Valid Memory Address (VMA)—This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90pF may be directly driven by this active high signal.

Bus Available (BA)—The Bus Available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the $\overline{\text{Halt}}$ line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit I = 0) or non-maskable interrupt. This output is capable of driving one standard TTL load and 30pF.

$\overline{\text{Interrupt Request}}$ ($\overline{\text{IRQ}}$)—This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The $\overline{\text{Halt}}$ line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while $\overline{\text{Halt}}$ is low.

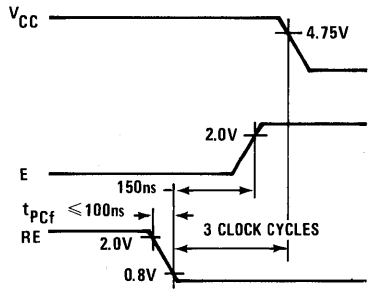
The $\overline{\text{IRQ}}$ has a high impedance pull-up device internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

$\overline{\text{Reset}}$—This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start-up of the processor. When this line is low, the MPU is inactive and the information in the registers will be lost. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFE, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine, the interrupt mask bit is set and must be reset before the MPU can be interrupted by $\overline{\text{IRQ}}$. Power-up and reset timing and power-down sequences are shown in Figures 9 and 10, respectively.

When $\overline{\text{RESET}}$ is released it must go through the low to high threshhold without bouncing, oscillating, or otherwise causing an erroneous $\overline{\text{RESET}}$ (less than 3 clock cycles). This may cause improper MPU operation.

$\overline{\text{Reset}}$, when brought low, must be held low at least 3 clock cycles. This allows the S6802/S6808 adequate time to respond internally to reset. This function is independent of the 20ms power up reset that is required.

Figure 10. Power-Down Sequence



Non-Maskable Interrupt (NMI)—A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the $\overline{\text{Interrupt Request}}$ signal, the processor will complete the current instruction that is being executed before it recognizes the $\overline{\text{NMI}}$ signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations caused the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$ has a high impedance pull-up resistor internal to the chip; however a 3kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{IRQ}$ and $\overline{NMI}$ are hardware interrupt lines that are sampled when E is high and will start the interrupt routine on a low E following the completion of an instruction.

Figure 12 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 2 gives the memory map for interrupt vectors.

RAM Enable (RE)—A TTL-compatible RAM enable input controls the on-chip RAM of the S6802. When placed in the high state, the on-chip memory is enabled to respond to the MPU controls. In the low state, RAM is disabled. This pin may also be utilized to disable reading and writing the on-chip RAM during power-down situation. RAM enable must be low three clock cycles before V_{CC} goes below 4.75V during power-down to retain the on board RAM contents during V_{CC} standby.

The Data Bus will be in the output mode when the internal RAM is accessed, which prohibits external data from entering the MPU. Note that the internal RAM is fully decoded from $0000 to $007F and these locations must be disabled when internal RAM is accessed.

Extal and Xtal—The S6802/S6808 has an internal oscillator that may be crystal controlled. These connections are for a parallel resonant fundamental crystal. (AT cut) A divide-by-four circuit has been added to the S6802 so that a 4MHz crystal may be used in lieu of a 1MHz crystal for a more cost effective system. Pin 39 of the S6802/S6808 may be driven externally by a TTL input signal if a separate clock is required. Pin 38 is to be left open in this mode. If the external clock is used it may not be halted for more than 4.5μs. The S6802/S6808 is a dynamic part except for internal RAM, and requires the external clock to retain information. Figure 11a shows the crystal parameters. In applications where other than a 4.0MHz crystal is used, Table 1 gives the designer the crystal parameters to be specified. The table contains the entire spectrum of usable crystals for the S6802/S6808. Crystal frequencies not shown (that lie between 1.0MHz and 4.0MHz) may be interpolated from the table. Figure 11b shows the crystal connection.

Table 1. Crystal Parameters

Y1 CRYSTAL FREQUENCY	C1 & C2	C LOAD	R1 (MAX)	C_0 (MAX)
4.0MHz	27pF	24pF	50 ohms	7.0pF
3.58MHz	27pF	20pF	50 ohms	7.0pF
3.0MHz	27pF	18pF	75 ohms	6.7pF
2.5MHz	27pF	18pF	74 ohms	6.0pF
2.0MHz	33pF	24pF	100 ohms	5.5pF
1.5MHz	39pF	27pF	200 ohms	4.5pF
1.0MHz	39pF	30pF	250 ohms	4.0pF

Memory Ready (MR)—MR is a TTL compatible input control signal which allows stretching of E. When MR is high, E will be in normal operation. When MR is low, it may be stretched integral multiples of half periods, thus allowing interface to slow memories. Memory Ready timing is shown in Figure 13.

Enable (E)—This pin supplies the clock for the MPU and the rest of the system. This is a single phase, TTL compatible clock. This clock may be conditioned by a Memory Ready Signal. This is equivalent to ϕ2 on the S6800.

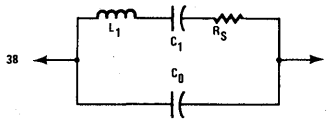
V_{CC} Standby—This pin supplies the dc voltage to the first 32 bytes of RAM as well as the RAM Enable (RE) control logic. Thus retention of data in this portion of the RAM on a power-up, power-down, or standby condition is guaranteed. Maximum current drain at 5.25V is 8mA.

Table 2. Memory Map for Interrupt Vectors

VECTOR		
MS	LS	DESCRIPTION
FFFE	FFFF	RESTART
FFFC	FFFD	NON-MASKABLE INTERRUPT
FFFA	FFFB	SOFTWARE INTERRUPT
FFF8	FFF9	INTERRUPT REQUEST

Note: Memory Read (MR), Halt, RAM Enable (RE) and Non-Maskable interrupt should always be tied to the correct high or low state if not used.

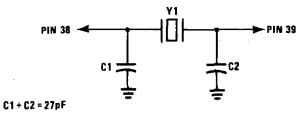
Figure 11a. Crystal Parameters



AT – Cut Parallel Resonance Crystal
C_0 = 7pF Max.
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 ohms Max.
Frequency Tolerance – ±5% to ±0.02%
The best E output "Worst Case Design" tolerance is ± 0.05% (500ppM) using A ±0.02 crystal.

Tolerance Note:
Critical timing loops may require a better tolerance than ±5%. Because of production deviations and the Temperature Coefficient of the S6802, the best "worst case design" tolerance is ±0.05%. (500 ppm) using a ±0.02% crystal. If the S6802 is not going to be used over its entire temperature range of 0°C to 70°C, a much tighter overall tolerance can be achieved.

Figure 11b. Crystal Connection



C1 + C2 = 27pF

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S6805

MICROCOMPUTER

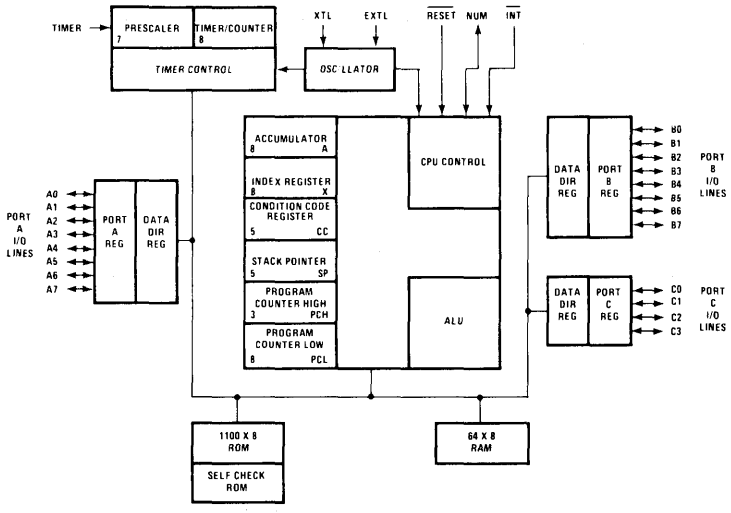
Features

☐ **Hardware**
- 8-Bit Architecture
- 64 Bytes RAM
- 1100 Bytes ROM
- 116 Bytes of Self Check ROM
- 28 Pin Package
- Memory Mapped I/O
- Internal 8-Bit Timer with 7-Bit Prescaler
- Vectored Interrupts — External, Timer, Software, Reset
- 20 TTL/CMOS Compatible I/O Line 8 Lines LED Compatible
- On-Chip Clock Circuit
- Self-Check Capability
- Low Voltage Inhibit
- 5 Vdc Single Supply

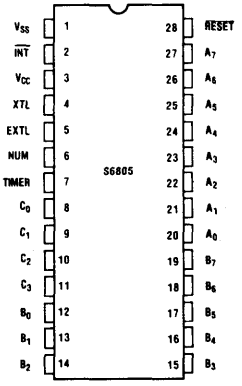
☐ **Software**
- Similar to 6800
- Byte Efficient Instruction Set
- Versatile Interrupt Handling
- True Bit Manipulation
- Bit Test and Branch Instruction
- Indexed Addressing for Tables
- Memory Usable as Registers/Flags
- 10 Addressing Modes
- Powerful Instruction Set
  - — All 6800 Arithmetic Instructions
  - — All 6800 Logical Instructions
  - — All 6800 Shift Instructions
  - — Single Instruction Memory Examine/Change
  - — Full Set of Conditional Branches

S6800

Block Diagram



Pin Configuration



General Description

The S6805 is an 8-bit single chip microcomputer. It is the first member of the growing microcomputer family that contains a CPU, on-chip clock, ROM, RAM, I/O and timer. A basic feature of the 6805 is an instruction set very similar to the S6800 family of microprocessors. Although the 6805 is not strictly source nor object code compatible, an experienced 6800 user can easily write 6805 code. Also a 6805 user will have no trouble moving up to the 6801 or 6809 for more complex tasks.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature Range, T_A	0° to +70°C
Storage Temperature Range, T_{stg}	−55°C to +150°C
Thermal Resistance, θ_{JA}	
Plastic	85°C/W
Ceramic	50°C/W
Cerdip	51°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to the range V_{SS} $(V_{IN}$ or $V_{OUT}) + V_{CC}$

Electrical Characteristics: $V_{CC} = +5.25$ Vdc ± 0.5Vdc, V_{SS} = GND, $T_A = 0° - 70°C$ unless otherwise noted

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	$\overline{RESET}$	4.0	—	V_{CC}	Vdc
V_{IH}		$\overline{INT}$	4.0		V_{CC}	Vdc
V_{IH}		All Other	$V_{SS}+2.0$	—	V_{CC}	Vdc
V_{IH}	Input High	Timer Mode	$V_{SS}+2.0$	—	V_{CC}	Vdc
V_{IH}	Voltage Timer	Self-Check Mode	—	9.0	15.0	Vdc
V_{IL}	Input Low Voltage	$\overline{RESET}$	$V_{SS}-0.3$	—	0.8	Vdc
V_{IL}		$\overline{INT}$	$V_{SS}-0.3$		1.5	Vdc
V_{IL}		All Other	$V_{SS}-0.3$	—	$V_{SS}+0.8$	Vdc
V_H	$\overline{INT}$ Hysteresis		—	100	—	mV_{CC}
P_D	Power Dissipation		—	350	—	mW
C_{IN}	Input Capacitance	EXTL	—	25	—	pF
C_{IN}		All Other	—	10	—	pF
LVR	Low Voltage Recover		—	—	4.75	Vdc
LVI	Low Voltage Inhibit		—	4.5	—	

Switching Characteristics: $V_{CC} = +5.25$ V ± 0.5 Vdc, V_{SS} = GND, $T_A = 0° - 70°C$ unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_{cl}	Clock Frequency	0.4	—	4.0	MHz
t_{CYC}	Cycle Time	1.0	—	10	μs
t_{IWL}	$\overline{INT}$ Pulse Width	$t_{CYC}+250$	—	—	ns
t_{RWL}	$\overline{RESET}$ Pulse Width	$t_{CYC}+250$	—	—	ns
t_{RHL}	Delay Time Reset (External Cap. = 0.47μF)	20	50	—	ms

Port Electrical Characteristics: $V_{CC}=+5.25$ Vdc± 0.5 Vdc, $V_{SS}=$GND, $T_A=0°-70°$C unless otherwise noted

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Condition
			Port A			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	$I_{LOAD}=1.6$mAdc
V_{OH}	Output High Voltage	2.4	—	—	Vdc	$I_{LOAD}=100\mu$Adc
V_{OH}	Output High Voltage	3.5	—	—	Vdc	$I_{LOAD}=-10\mu$Adc
V_{IH}	Input High Voltage	$V_{SS}+2.0$	—	V_{CC}	Vdc	$I_{LOAD}=-300\mu$Adc (max)
V_{IL}	Input Low Voltage	$V_{SS}-0.3$	—	$V_{SS}+0.8$	Vdc	$I_{LOAD}=-500\mu$Adc (max)
			Port B			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	$I_{LOAD}=3.2$mAdc
V_{OL}	Output Low Voltage	—	—	1.0	Vdc	$I_{LOAD}=10$mAdc(sink)
V_{OH}	Output High Voltage	2.4	—	—	Vdc	$I_{LOAD}=-200\mu$Adc
I_{OH}	Darlington Current Drive (Source)	−1.0	—	−10	mAdc	$V_O=1.5$Vdc
V_{IH}	Input High Voltage	$V_{SS}+2.0$	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	$V_{SS}-0.3$	—	$V_{SS}+0.8$	Vdc	
			Port C			
V_{OL}	Output Low Voltage	—	—	0.4	Vdc	$I_{LOAD}=1.6$mAdc
V_{OH}	Output High Voltage	2.4	—	—	Vdc	$I_{LOAD}=-100\ \mu$Adc
V_{IH}	Input High Voltage	$V_{SS}+2.0$	—	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	$V_{SS}-0.3$	—	$V_{SS}+0.8$	Vdc	
			Off-State Input Current			
I_{TSI}	Three-State Ports B & C	—	2	20	μAdc	
			Input Current			
I_{IN}	Timer at $V_{IN}=$(0.4 to 2.4 Vdc)	—	—	20	μAdc	

Figure 1. TTL Equiv. Test Load (Port B)

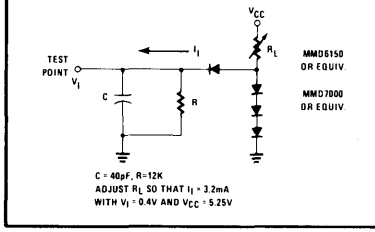


Figure 2. CMOS Equiv. Test Load (Port A)

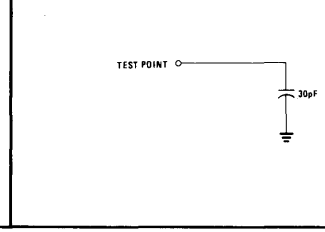
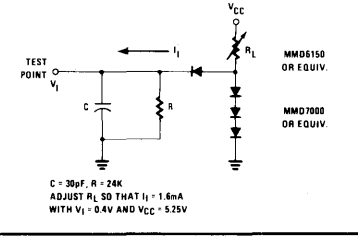


Figure 3. TTL Equiv. Test Load (Ports A and C)



Pin Description

Pin	Symbol	Description
1 and 3	V_{CC} and V_{SS}	Power is supplied to the MCU using these two pins. V_{CC} is 5.25V±.5V, and V_{SS} is the ground connection.
2	$\overline{INT}$	External Interrupt provides capability to apply an external interrupt to the MCU.
4 and 5	XTL and EXTL	Provide control input for the on-chip clock circuit. The use of crystal (at cut 4MHz maximum), a resistor or a wire jumper is sufficient to drive the internal oscillator with varying degrees of stability. (See Internal Oscillator Options for recommendations) An internal divide by 4 prescaler scales the frequency down to the appropriate $\phi 2$ clock rate (1MHz maximum).
6	NUM	This pin is not for user application and should be connected to ground.
7	TIMER	Allows an external input to be used to decrement the internal timer circuitry. See TIMER for detailed information about the timer circuitry.
8-11 12-19 20-27	C0-C3 B0-B7 A0-A7	Input/Output lines (A0-A7, B0-B7, C0-C3). The 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmed as either inputs or outputs under software control of the data direction registers. See Inputs/Outputs for additional information.
28	$\overline{RESET}$	This pin allows resetting of the MCU. A low voltage detect feature responds to a dip in voltage by forcing a RESET condition to clear all Data Direction Registers, so that all I/O pins are set as inputs.

Memory

The MCU memory is configured as shown in Figure 4. During the processing of an interrupt, the contents of the MCU registers are pushed onto the stack in the order shown in Figure 5. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first, then the high order three bits (PCH) are stacked first, then the high order three bits (PCH) are stacked. This ensures that the program counter is loaded correctly as the stack pointer increments when it pulls data from the stack. A subroutine call will cause only the program counter (PCH, PCL) contents to be pushed onto the stack.

Figure 4. MCU Memory Configuration

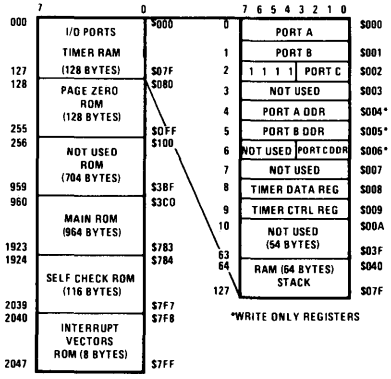


Figure 5. Interrupt Stacking Order

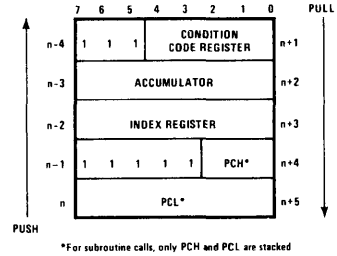
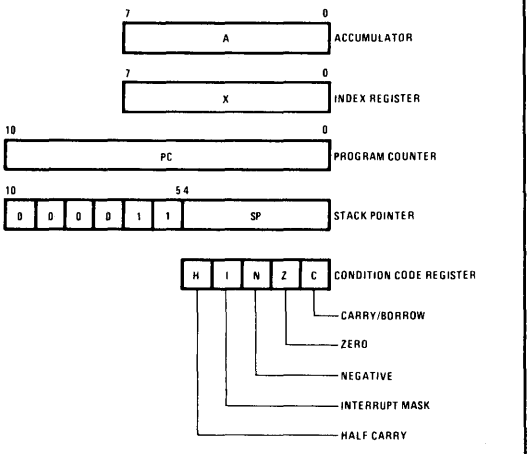


Figure 6. Programming Model



Registers

The S6805 MCU contains two 8-bit registers (A and X), one 11-bit register (PC), two 5-bit registers (SP and CC) that are visible to the programmer (see Figure 6).

Accumulator (A)

The A-register is an 8-bit general purpose accumulator used for arithmetic calculations and data manipulation.

Index Register (X)

This 8-bit register is used for the indexed addressing mode. It provides an 8-bit address that may be added to an offset to create an effective address. The index register can also be used for limited calculations and data manipulations when using the read/modify/write instructions. In code sequences not employing the index register it can be used as a temporary storage area.

Program Counter (PC)

This 11-bit register contains the address of the next instruction to be executed.

Stack Pointer (SP)

The stack pointer is an 11-bit register that contains the address of the next free location on the stack. Initially, the stack pointer is set to location $07F and is decremented as data is being pushed onto the stack and incremented as data is being pulled from the stack. The six most significant bits of the stack pointer are permanently set to 000011. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $07F. Subroutines and interrupts may be nested down to location $061 which allows the programmer to use up to 15 levels of subroutine calls. A 16th subroutine call would save the return address correctly, but the stack pointer would not remain pointing into the stack area and there would be no way to return from any of the subroutines.

Condition Code Register (CC)

The condition code register is a 5-bit register in which each bit is used to indicate or flag the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each individual condition code register bit is explained in the following paragraphs.

HALF CARRY (H)—Used during arithmetic operations (ADD and ADC) to indicate that a carry occurred between bits 3 and 4.

INTERRUPT (I)—This bit is set to mask the timer and external interrupt ($\overline{\text{INT}}$). If an interrupt occurs while this bit is set it is latched and will be processed as soon as the interrupt bit is reset.

NEGATIVE (N)—USED TO INDICATE that the result of the last arithmetic, logical or data manipulation was negative (bit 7 in result equal to a logical one).

ZERO (Z)—Used to indicate that the result of the last arithetic, logical or data manipulation was zero.

CARRY/BORROW (C)—Used to indicate that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, shifts and rotates.

Timer

The MCU timer circuitry is shown in Figure 7. The 8-bit counter is loaded under program control and counts down toward zero as soon as the clock input is applied. When the timer reaches zero the timer interrupt request bit (bit 7) in the timer control register is set. The MCU redsponds to this interrupt by saving the present MCU state in the stack, fetching the timer interrupt vector from locations $7F8 and $7F9 and executing the interrupt routine. The timer interrupt can be masked by setting the timer interrupt mask bit (bit 6) in the timer control register. The interupt bit (bit 1) in the condition code register will also prevent a timer interrupt from being processed.

The clock input to the timer can be from an external source applied to the TIMER input pin or it can be the internal $\phi 2$ signal. Note that when $\phi 2$ signal is used as the source it can be gated by an input applied to the TIMER

input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the options that has to be specified before manufacture of the MCU. A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before being applied to the counter. This prescaling option must also be specified before manufacturing begins. The timer continues to count past zero and its present count can be monitored at any time by monitoring the timer data register. This allows a program to determine the length of time since a timer interrupt has occurred and not disturb the counting process.

At power up or reset the prescaler and counter are initialized with all logical ones; the timer interrupt request bit (bit 7) is cleared and the timer request mask bit (bit 6) is set.

Self Check Mode:

The MCU includes a non-user mode pin that replaces the normal operating mode with one in which the internal data and address buses are available at the I/O ports. The ports are configured as follows in the test mode (some multiplexing of the address and data lines is necessary):

- The internal ROM and RAM are disabled and Port A becomes the input data bus on the $\phi 2$ of the clock and can be used to supply instructions of data to the MCU.
- Port B is also multiplexed. When $\phi 2$ is high, Port B is the output data bus, and when $\phi 2$ is low Port B is the address lines. The output data bus can be used to monitor the internal ROM or RAM.
- Port C becomes the last three address lines and a read/write control line.

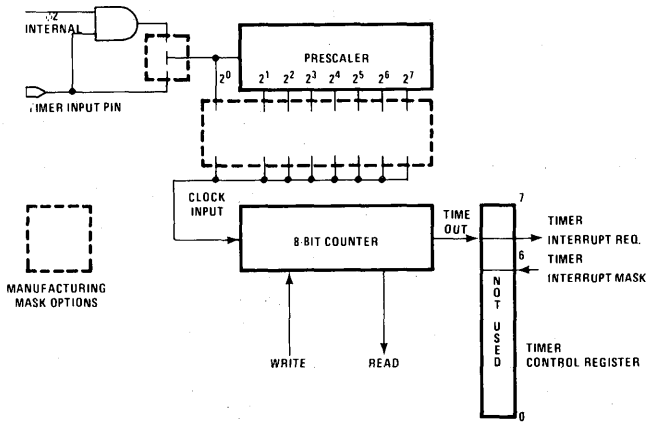
The MCU incorporates a self test program within a 116 byte non-user accessable test program and some control logic on-chip. These 116 bytes of ROM test every addressing mode and nearly every CPU instruction (95% of the total microprocessor capability) while only adding 1% to the total overall die size.

To perform the self test, the MCU output lines of Port A and B must be externally interconnected (Figure 7) and LED's are connected to Port C to provide both a pass/fail indication (3Hz square wave).

The flowchart for the self test program (Figure 8) runs four tests:

- **I/O TEST:** Tests for I/O lines that are stuck in high, low, shorted state, or are missing a connection. The I/O lines are all externally wired together so that the program can look for problems by testing for the correct operation of the lines as inputs and outputs and for shorts between two adjacent lines.
- **ROM ERROR:** (Checksum wrong). The checksum value of the user program must be masked into the self check ROM when the microcomputer is built. The self check program then tests the user ROM by computing the checksum value, which should be equal to the masked checksum if all the bits in the ROM are properly masked. Address and data lines that are stuck high, low or to each other are also detected by this test. An inoperable ROM will (in most cases) prevent the running of the self check program.

Figure 7. Timer Block Diagram



• **RAM Bits Non-Functional:** The RAM is tested by the use of a walking bit pattern that is written into memory and then verified. Every in RAM is set to one and then to zero by using 9 different patterns as shown in Figure 9.

Figure 8. Interconnected Ports for Self Check Mode. Port C Gives Go/No Go and Diagnostic Information.

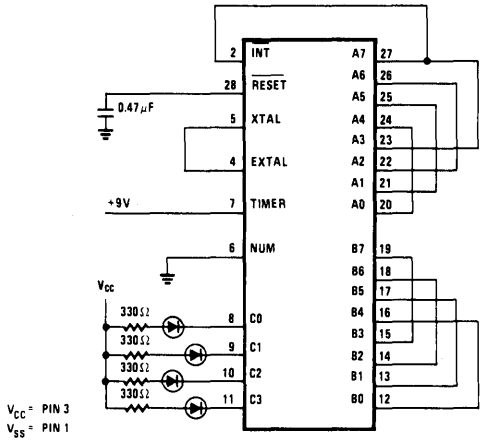
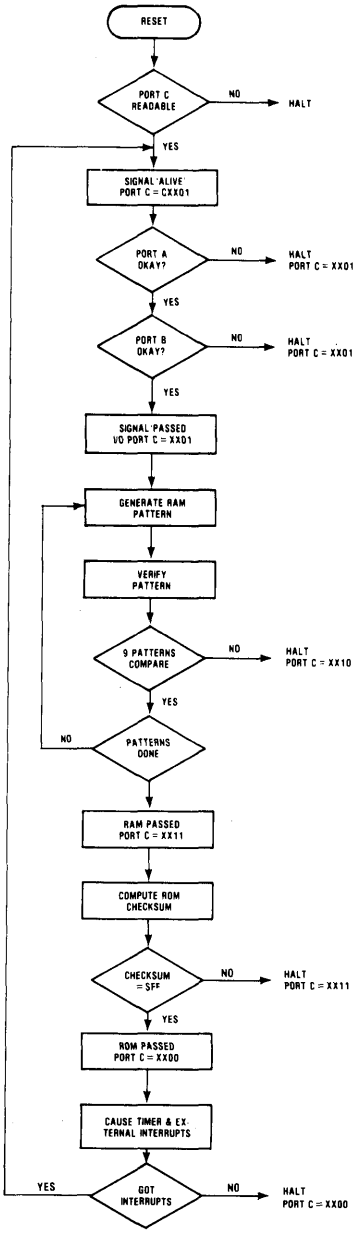


Figure 9. Flowchart of Self Test Routines



Self Test Routines

Program performs four main tests in the major loops and provides an output signal to indicate that the part is functional.

Interrupt Logic Failure: Using an I/O line the interrupt pin is toggled to create an interrupt. The main program runs long enough to allow the timer to underflow and causes the timer interrupt to be enabled.

If all of these tests are successful the program, then loops back to the beginning and starts testing again.

The self check program initially tries to get the MCU out of the reset state to indicate that the processor is at least working. The non-functional parts are thus immediately eliminated, and if the part fails at this first stage the program provides a means of determining the faulty section.

To place the MCU in the self check mode the voltage on the timer input (Figure 7) is raised to 8 volts which causes several operations to take place:

• The clocking source for the timer is shunted to the MCU internal clock to insure that the timer will run an underflow during the course of the program, no matter which clocking rate is masked.

• The address of the interrupt vectors (including the reset vector) are mapped into the self check ROM area. This allows the self check to test the interrupt structure.

The self check program is started by the reset signal instead of the normal program because the vectors (including the reset vector) have been overlaid. The self check program runs in an endless loop testing and retesting the processor as long as there are no errors. Signals on the I/O lines indicate that the test has passed, and if any test fails, the program stops by executing a branch to self instruction. The output lines then cease to toggle and two of the I/O lines will indicate the cause of failure.

RAM Test Pattern

"Walking bit" patterns test sequence sets and resets every bit in memory. (See Figure 10.)

Low Voltage Inhibit

As soon as the voltage at pin 3 (V_{CC}) falls to 4.5 volts, all I/O lines are put into a high impedance state. This prevents erroneous data from being given to an external device. When V_{CC} climbs back up to 4.6 volts a vectored reset is performed.

Table 1. Cause of Chip Failure as Shown in Bits 0 and 1 of I/O Port C

BIT 1	BIT 0	REASON FOR FAILURE
0	0	INTERRUPTS
0	1	I/O PORTS A OR B
1	0	RAM
1	1	ROM

Figure 10. RAM Test Pattern

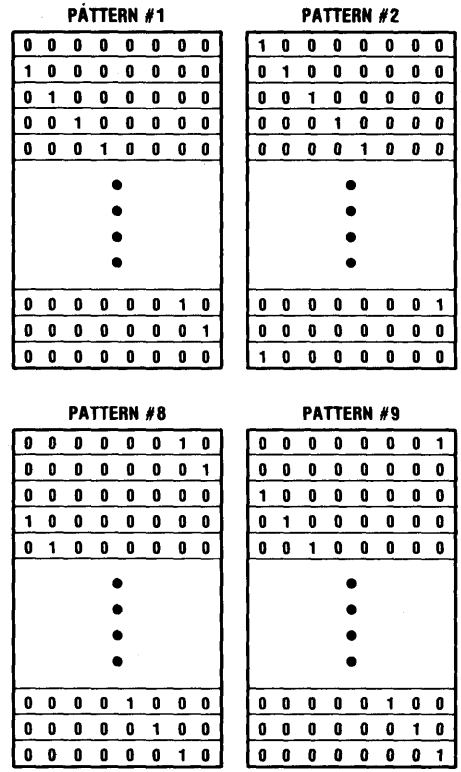
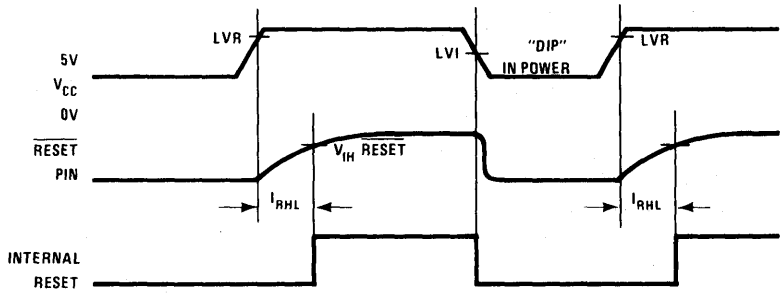


Figure 11. Power Up and Reset Timing

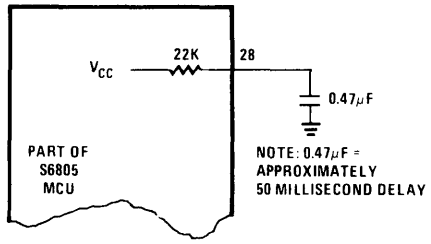


Resets

The MCU can be reset three ways; by the external reset input ($\overline{\text{RESET}}$), by the internal low voltage detect circuit already mentioned, and during the power up time. (See Figure 11.)

Upon power up, a minimum of 20 milliseconds is needed before allowing the reset input to go high. This time allows the internal oscillator to stabilize. Connecting a capacitor to the $\overline{\text{RESET}}$ input as shown in Figure 12 will provide sufficient delay.

Figure 12. Power Up Reset Delay Circuit



Internal Oscillator Options

The internal oscillator circuit has been designed to require a minimum of external components. The use of a crystal (AT cut, 4MHz max) or a resistor is sufficient to drive the internal oscillator with varying degrees of stability. A manufacturing mask option is available to provide better matching between the external components and the internal oscillator.

The different connection methods are shown in Figure 13. Crystal specifications are given in Figure 14. A resistor selection graph is given in Figure 15.

Figure 13. Internal Oscillator Options

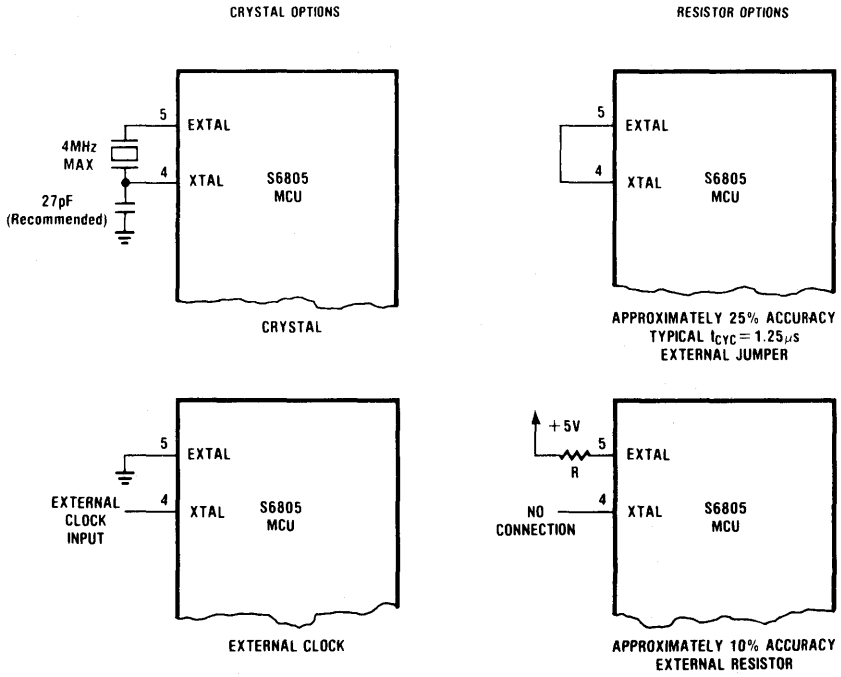
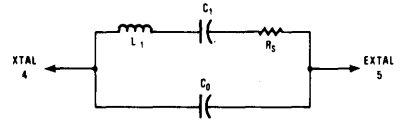
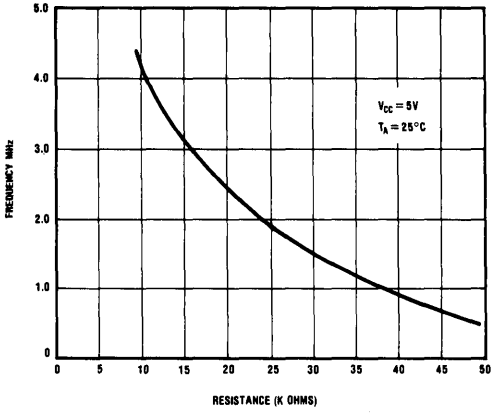


Figure 14. Crystal Parameters



AT-CUT PARALLEL RESONANCE CRYSTAL
C_0 = 7pF MAX
FREQ = 4.0MHz @ C_L = 24pF
R_S = 50 OHMS MAX

Figure 15. Typical Resistor Selection Graph



Interrupts

The MCU can be interrupted three different ways; through the external interrupt ($\overline{INT}$) input pin, the internal timer interrupt request, and a software interrupt instruction (SWI). When any interrupt occurs, processing is suspended, the present MCU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. The interrupt service routines normally end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt. Table 1 provides a listing of the interrupts, their priority, and the vector address that contain the starting address of the appropriate interrupt routine.

A sinusodial signal (1kHz maximum) can be used to generate an external interrupt ($\overline{INT}$) as shown in Figure 16.

A flowchart of the interrupt processing sequence is given in Figure 17.

Table 1. Interrupt Priorities

Interrupt	Priority	Vector Address
$\overline{RESET}$	1	$7FE AND $7FF
SWI	2	$7FC AND $7FD
$\overline{INT}$	3	$7FA AND $7FB
TIMER	4	$7F8 AND $7F9

Input/Output

There are 20 input/output pins. All pins are programmable as either inputs or outputs under software control of the data direction registers. When programmed as outputs, all I/O pins read latched output data regardless of the logic level at the output pin due to output loading (see Figure 18). When port B is programmed for outputs, it is capable of sinking 10 milliamperes on each pin (one volt maximum). All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs while Port B and C lines are CMOS compatible as inputs. Figure 19 provides some examples of port connections.

Figure 16. Typical Sinusodial Interrupt Circuits

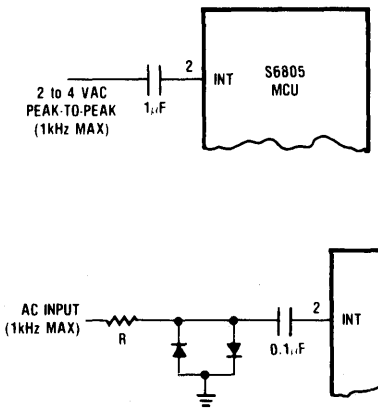


Figure 17. Interrupt Processing Flowchart

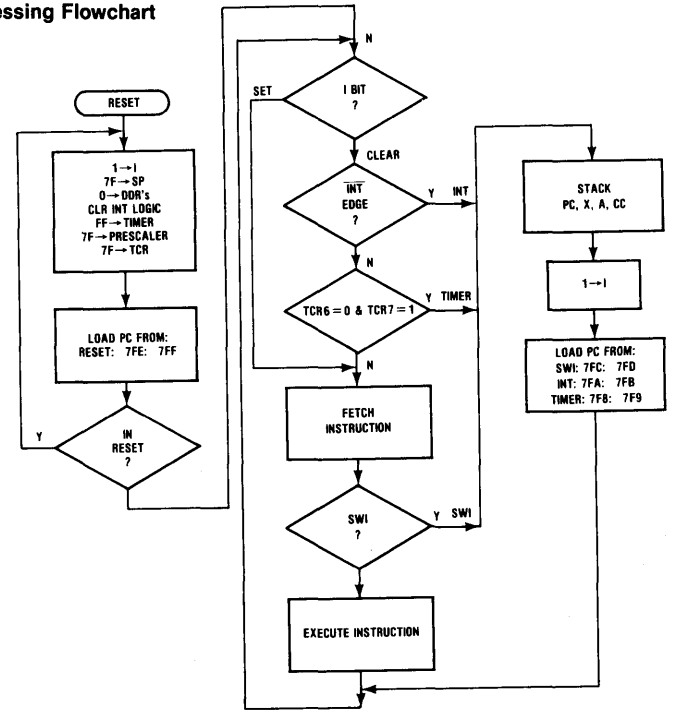
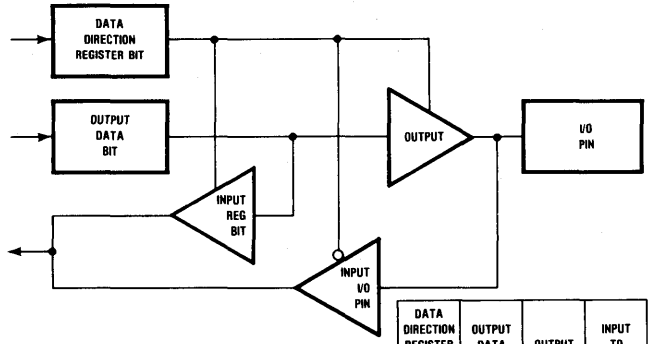
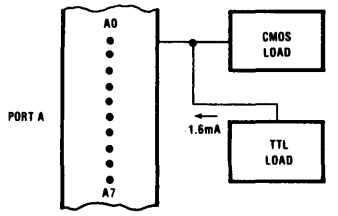


Figure 18. Typical Port I/O Circuitry

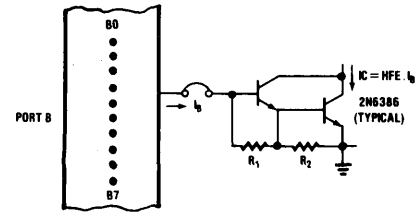


DATA DIRECTION REGISTER BIT	OUTPUT DATA BIT	OUTPUT STATE	INPUT TO MCU
1	0	0	0
1	1	1	1
0	X	3-STATE	PIN

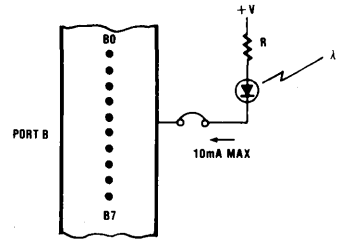
Figure 19. Typical Port Connections



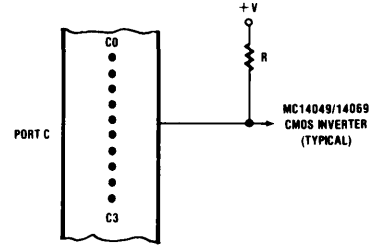
PORT A PROGRAMMED AS OUTPUT(S) DRIVING CMOS AND TTL LOAD DIRECTLY
(a)



PORT B PROGRAMMED AS OUTPUT(S) DRIVING DARLINGTON BASE DIRECTLY
(b)



PORT B PROGRAMMED AS OUTPUT(S) DRIVING LED(s) DIRECTLY
(c)



PORT C PROGRAMMED AS OUTPUT(S) DRIVING CMOS USING EXTERNAL PULL-UP RESISTORS
(D)

Bit Manipulation

The MCU has the ability to set or clear any single random access memory or input/output bit (except the data direction registers) with a single instruction (BSET, BCLR). Any bit in the page zero read only memory can be tested, using the BRSET and BRCLR instructions, and the program branches as a result of its state. This capability to work with any bit in RAM, ROM or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines. The example in Figure 20 illustrates the usefulness of the bit manipulation and test instructions. Assume that bit 0 of port A is connected to a zero crossing detector circuit and that bit 1 of port A is connected to the trigger of a TRIAC which powers the controlled hardware.

This program, which uses only seven ROM locations, provides turn-on of the TRIAC within 14 microseconds of the zero crossing. The timer could also be incorporated to provide turn-on at some later time which would permit pulse-width modulation of the controlled power.

Addressing Modes

The MCU has ten addressing modes available for use by the programmer. They are explained and illustrated briefly in the following paragraphs.

Figure 20. Bit Manipulation Example

```
        •
        •
        •
        •
        •
SELF 1  BRCLR 0, PORTA, SELF 1
        BSET 1, PORTA
        BCLR 1, PORTA
        •
        •
        •
        •
        •
```

Immediate—Refer to Figure 21. The immediate addressing mode accesses constants which do not change during program execution. Such instructions are two bytes long. The effective address (EA) is the PC and the operand is fetched from the byte following the opcode.

Direct—Refer to Figure 22 in direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in memory. All RAM space, I/O registers and 128 bytes of ROM are located in page zero to take advantage of this efficient memory addressing mode.

Extended—Refer to Figure 23. Extended addressing is used to reference any location in memory space. The EA is the contents of the two bytes following the opcode. Extended addressing instructions are three bytes long.

Relative—Refer to Figure 24. The relative addressing mode applies only to the branch instructions. In this mode the contents of the byte following the opcode is added to the program counter when the branch is taken. EA=(PC)+2+Rel. Rel is the contents of the location following the instruction opcode with bit 7 being the sign bit. If the branch is not tken Rel=0, when a branch takes place, the program goes to somewhere within the range of +129 bytes to −127 of the present instruction. These instructions are two bytes long.

Indexed (No Offset)—Refer to Figure 25. This mode of addressing accesses the lowest 256 bytes of memory. These instructions are one byte long and their EA is the contents of the index register.

Indexed (8-Bit Offset)—Refer to Figure 26. The EA is calculated by adding the contents of the byte following the opcode to the contents of the index register. In this mode, 511 low memory locations are accessable. These instructions occupy two bytes.

Indexed (16-Bit Offset)—Refer to Figure 27. This addressing mode calculates the EA by adding the contents of the two bytes following the opcode to the index register. Thus, the entire memory space may be accessed. Instructions which use this addressing mode are three bytes long.

Bit Set/Clear—Refer to Figure 28. This mode of addressing applies to instructions which can set or clear any bit on page zero. The lower three bits in the opcode specify the bit to be set or cleared while the byte following the opcode specifies the address in page zero

Bit Test and Branch—Refer to Figure 29. This mode of addressing applies to instructions which can test any bit in the first 256 locations ($00-$FF) and branch to any location relative to the PC. The byte to be tested is addressed by the byte following the opcode. The individual bit within that byte to be tested is addressed by the lower three bits of the opcode. The third byte is the relative address to be added to the program counter if the branch condition is met. These instructions are three bytes long. The value of the bit tested is written to the carry bit in the condition code register.

Inherent—Refer to Figure 30. The inherent mode of addressing has no EA. All the information necessary to execute an instruction is contained in the opcode. Direct operations on the accumulator and the index register are included in this mode of addressing. In addition, control instructions such as SWI. RTI belong to this group. All inherent addressing instructions are one byte long.

Figure 21. Immediate Addressing Example

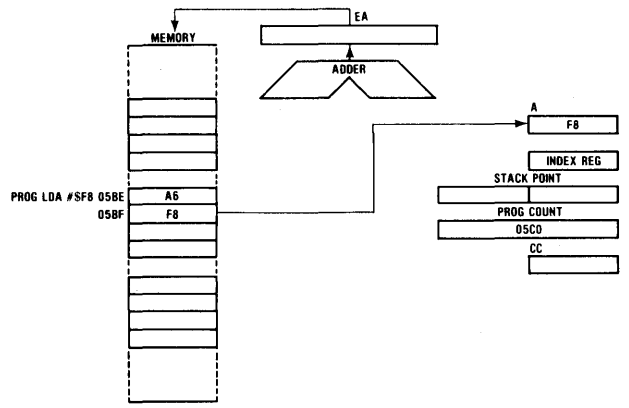


Figure 22. Direct Addressing Example

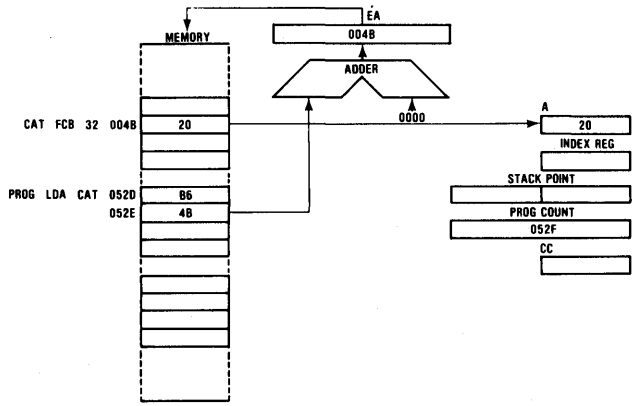


Figure 23. Extended Addressing Example

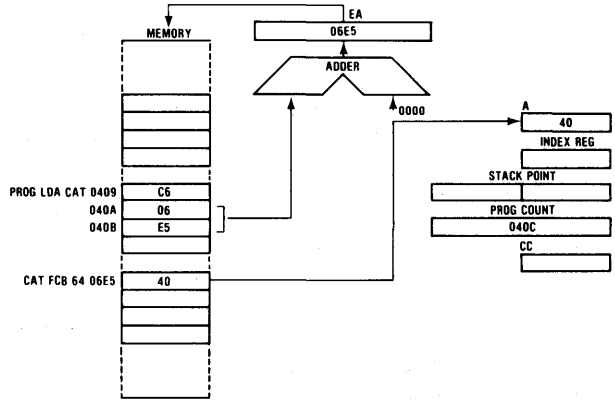


Figure 24. Relative Addressing Example

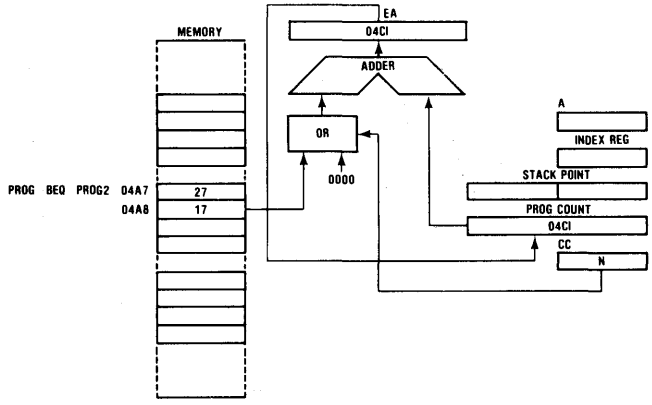


Figure 25. Indexed (No Offset) Addressing Example

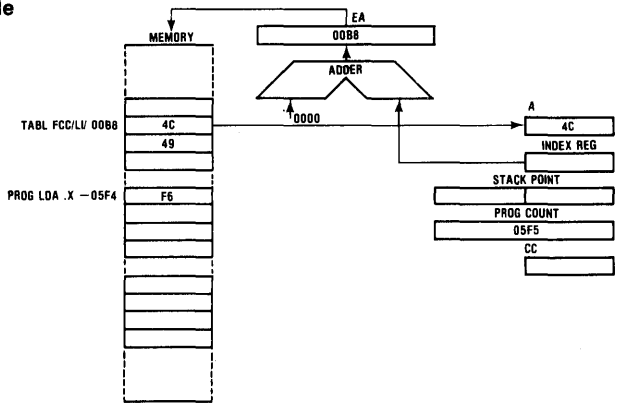


Figure 26. Indexed (8-Bit Offset) Addressing Example

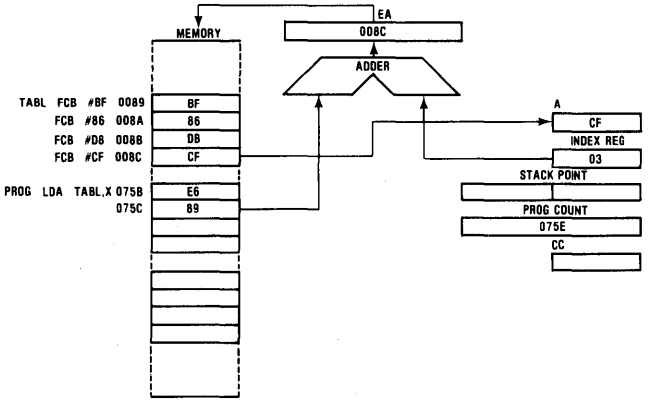


Figure 27. Indexed (16-Bit Offset) Addressing Example

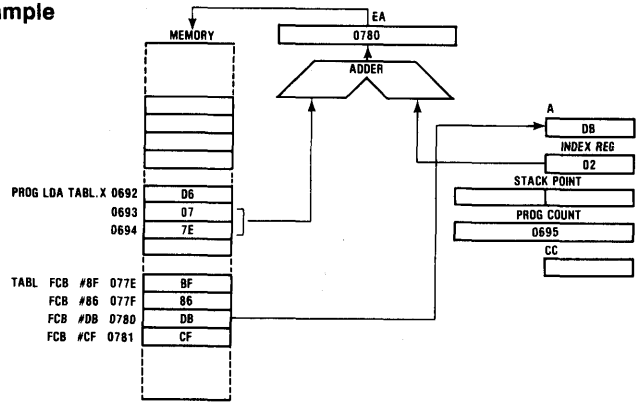


Figure 28. Bit Set/Clear Addressing Example

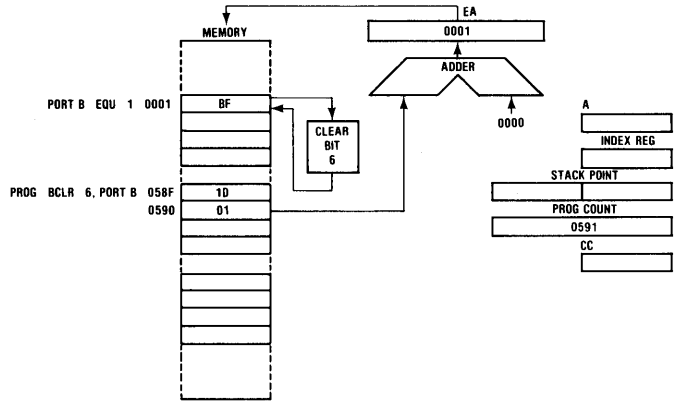


Figure 29. Bit Test and Branch Addressing Example

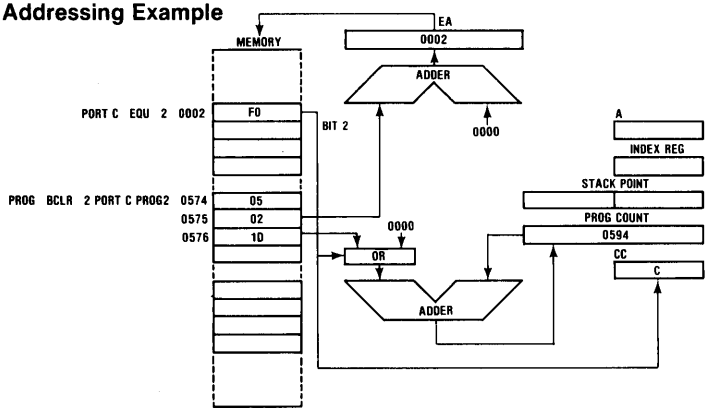
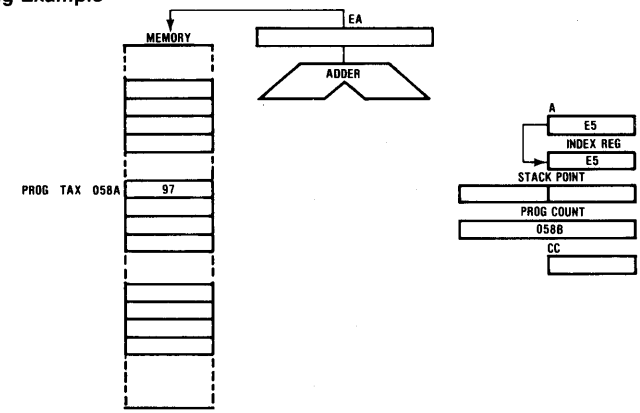


Figure 30. Inherent Addressing Example



Instruction Set

The MCU has a set of 59 basic instructions. They can be divided into five different types: register/memory, read/modify/write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

Register/Memory Instructions—Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to Table 2.

Read/Modify/Write Instructions—These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register. The test for negative or zero (TST) instruction is an exception to the read/modify/write instructions since it does not perform the write. Refer to Table 3.

Branch Instructions—The branch instructions cause a branch from the program when a certain condition is met. Refer to Table 4.

Bit Manipulation Instructions—These instructions are used on any bit in the first 256 bytes of the memory. One group either sets or clears. The other group performs the bit test and branch operations. Refer to Table 5.

Control Instructions—The control instructions control the MCU operations during program execution. Refer to Table 6.

Alphabetical Listing—The complete instruction set is given in alphabetical order in Table 7.

Opcode Map—Table 8 is an opcode map for the instructions used on the MCU.

Table 2. Register/Memory Instructions

		ADDRESSING MODES																	
		IMMEDIATE			DIRECT			EXTENDED			INDEXED (No Offset)			INDEXED (8-Bit Offset)			INDEXED 16-Bit Offset)		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
LOAD A FROM MEMORY	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
LOAD X FROM MEMORY	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
STORE A IN MEMORY	STA	—	—	—	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
STORE X IN MEMORY	STX	—	—	—	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
ADD MEMORY TO A	ADD	AE	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
ADD MEMORY AND CARRY TO A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
SUBTRACT MEMORY	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
SUBTRACT MEMORY FROM A WITH BORROW	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND MEMORY TO A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR MEMORY WITH A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
EXCLUSIVE OR MEMORY WITH A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
ARITHMETIC COMPARE A WITH MEMORY	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
ARITHMETIC COMPARE X WITH MEMORY	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
BIT TEST MEMORY WITH A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
JUMP UNCONDITIONAL	JMP	—	—	—	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
JUMP TO SUBROUTINE	JSR	—	—	—	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

Table 3. Read/Modify/Write Instructions

		ADDRESSING MODES														
		INHERENT (A)			INHERENT (X)			DIRECT			INDEXED (No Offset)			INDEXED (8-Bit Offset)		
Function	Mnemonic	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles	OP Code	# Bytes	OP Cycles	# Code	# Bytes	Cycles
INCREMENT	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
DECREMENT	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
CLEAR	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
COMPLEMENT	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
NEGATE (2's COMPLEMENT)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
ROTATE LEFT THRU CARRY	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
ROTATE RIGHT THRU CARRY	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
LOGICAL SHIFT LEFT	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
LOGICAL SHIFT RIGHT	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
ARITHMETIC SHIFT RIGHT	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
TEST FOR NEGATIVE OR ZERO	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

Table 4. Branch Instructions

		RELATIVE ADDRESSING MODE		
Function	Mnemonic	OP Code	# Bytes	# Cycles
BRANCH ALWAYS	BRA	20	2	4
BRANCH NEVER	BRN	21	2	4
BRANCH IFF HIGHER	BHI	22	2	4
BRANCH IFF LOWER OR SAME	BLS	23	2	4
BRANCH IFF CARRY CLEAR	BCC	24	2	4
(BRANCH IFF HIGHER OR SAME)	(BHS)	24	2	4
BRANCH IFF CARRY SET	BCS	25	2	4
(BRANCH IFF LOWER)	(BLO)	25	2	4
BRANCH IFF NOT EQUAL	BNE	26	2	4
BRANCH IFF EQUAL	BEQ	27	2	4
BRANCH IFF HALF CARRY CLEAR	BHCC	28	2	4
BRANCH IFF HALF CARRY SET	BHCS	29	2	4
BRANCH IFF PLUS	BPL	2A	2	4
BRANCH IFF MINUS	BMI	2B	2	4
BRANCH IFF INTERRUPT MASK BIT IS CLEAR	BMC	2C	2	4
BRANCH IFF INTERRUPT MASK BIT IS SET	BMS	2D	2	4
BRANCH IFF INTERRUPT LINE IS LOW	BIL	2E	2	4
BRANCH IFF INTERRUPT LINE IS HIGH	BIH	2F	2	4
BRANCH TO SUBROUTINE	BSR	AD	2	8

Table 5. Bit Manipulation Instructions

Function	Mnemonic	ADDRESSING MODES					
		OP Code	# Bytes	# Cycles	OP Code	# Bytes	# Cycles
BRANCH IFF BIT n IS SET	BRSET n(n = 0 . . . . . 7)	—	—	—	2•n	3	10
BRANCH IFF BIT n IS CLEAR	BRCLR n(n = 0 . . . . . 7)	—	—	—	01 + 2•n	3	10
SET BIT n	BSET n(n = 0 . . . . . 7)	10 + 2•n	2	7	—	—	—
CLEAR BIT n	BCLR n(n = 0 . . . . . 7)	11 + 2•n	2	7	—	—	—

Table 6. Control Instructions

Function	Mnemonic	INHERENT		
		OP Code	# Bytes	# Cycles
TRANSFER A TO X	TAX	97	1	2
TRANSFER X TO A	TXA	9F	1	2
SET CARRY BIT	SEC	99	1	2
CLEAR CARRY BIT	CLC	98	1	2
SET INTERRUPT MASK BIT	SEI	9B	1	2
CLEAR INTERRUPT MASK BIT	CLI	9A	1	2
SOFTWARE INTERRUPT	SWI	83	1	11
RETURN FROM SUBROUTINE	RTS	81	1	6
RETURN FROM INTERRUPT	RTI	80	1	9
RESET STACK POINTER	RSP	9C	1	2
NO OPERATION	NOP	9D	1	2

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S6809/S68A09/S68B09

8-BIT MICROPROCESSING UNIT

Features

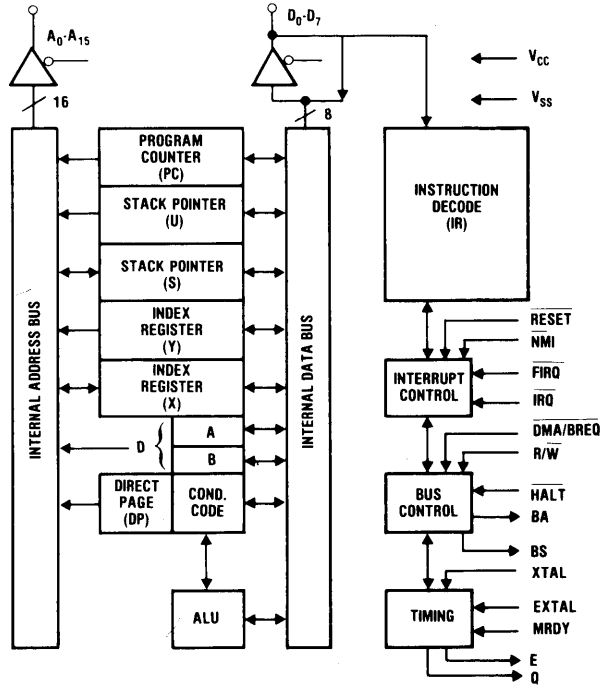
- Interfaces With All S6800 Peripherals
- Upward Compatible Instruction Set and Addressing Modes
- Upward Source Compatible Instruction Set and Addressing Modes
- Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator
- On-Chip Crystal Oscillator (4 times XTAL)

General Description

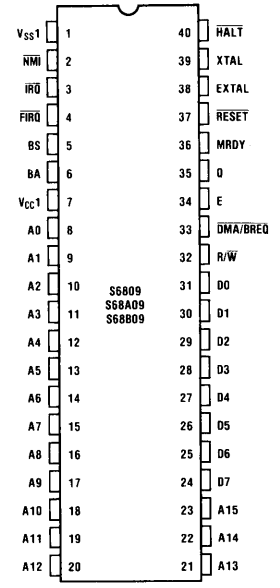
The S6809 is an advanced processor within the S6800 family offering greater throughput, improved byte efficiency, and increased adaptability to various software disciplines. These include position independence, reentrancy, recursion, block structuring, and high level language generation.

Because the S6809 generates *position-independent* code, software can be written in modular form for easy user expansion as system requirements increase. The S6809 is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809.

Block Diagram



Pin Configuration



S6809 Hardware Features

- ☐ **On-Chip Oscillator**
- ☐ **MRDY Input Extends Access Time**
- ☐ **$\overline{\text{DMA/BREQ}}$ for DMA and Memory Refresh**
- ☐ **Fast Interrupt Request Input: Stacks Only Program Counter and Condition Code**
- ☐ **Interrupt Acknowledge Output Allows Vectoring by Devices**
- ☐ **Three Vectored Priority Interrupt Levels**
- ☐ **SYNC Acknowledge Output Allows for Synchronization to External Event**
- ☐ **NMI Blocked after RESET until after First Load of Stack Pointer**
- ☐ **Early Address Valid Allows Use with Slow Memories**

S6809E Hardware Features

- ☐ **Last Instruction Cycle Output (LIC) for Identification Output Fetch**
- ☐ **Busy Output Eases Multiprocessor Design**

Instruction Set

- ☐ **Extended Range Branches**
- ☐ **Load Effective Address**
- ☐ **16-Bit Arithmetic**
- ☐ **8x8 Unsigned Multiply (Accumulator A*B)**
- ☐ **SYNC Instruction — Provides Software Sync with an External Hardware Process**
- ☐ **Push and Pull on 2 Stacks**
- ☐ **Push/Pull Any or All Registers**
- ☐ **Index Registers May Be Used as Stack Pointer**
- ☐ **Transfer/Exchange All Registers**

Addressing Modes

- ☐ **All 6800 Modes Plus PC Relative, Extended Indirect, Indexed Indirect, and PC Relative Indirect**
- ☐ **Direct Addressing Available Anywhere in Memory Map**
- ☐ **PC Relative Addressing: Byte Relative (± 32, 768 Bytes from PC)**
- ☐ **Complete Indexed Addressing Including Automatic Increment and Decrement, Register Offsets, and Four Indexable Registers (X, Y, U and S)**
- ☐ **Expanded Index Addressing**
  - **— 0, 5, 8, 16-Bit Constant Offset**
  - **— 8, 16-Bit Accumulator Offsets**

The S6809 gives the user 8 and 16-bit word capability with several hardware enhancements in the design such as the Fast Interrupt ($\overline{\text{FIRQ}}$), Memory Ready (MRDY), and Quadrature (Qout) and System Clock Outputs (Eout). With the Fast Interrupt Request ($\overline{\text{FIRQ}}$) the S6809 places *only* the Program Counter and Condition Code Register on the stack prior to accessing the $\overline{\text{FIRQ}}$ vector location. The Memory Ready ($\overline{\text{MRDY}}$) input allows extension of the data access time for use with slow memories. The System Clock (Eout) operates at the basic processor frequency and can be as the synchronization signal for the entire system. The Quadrature Output (Qout) provides additional system timing by signifying that address and data are stable.

The External Clock mode of the S6809E is particularly useful when synchronizing the processor to an externally generated signal. The Three-State Control input ($\overline{\text{TSC}}$) places the Address and R/$\overline{\text{W}}$ line in the high impedance state for DMA or Memory Refresh. The last Instruction Cycle (LIC) is activated during the last cycle of any instruction. This signifies that the next instruction cycle is the opcode fetch. The Processor Busy signal (BUSY) facilitates multiprocessor applications by allowing the designer to insure that flags being modified by one processor are not accessed by another simultaneously.

The S6809 features a family of addressing capabilities which can use any of the four index registers and stack pointers as a pointer to the operand (or the operand address). This pointer can have a fixed or variable signed offset that can be automatically incremented or decremented. The eight-bit direct page register permits a user to determine which page of memory is accessed by the instructions employing "page zero" addressing. This quick access to any page is especially useful in Multitasking Applications.

The S6809 has three vectored priority-interrupt levels, each of which automatically disables the lower priority interrupt while leaving the higher priority interrupt enabled.

The S6809 gives the system designer greater flexibility (through modular relocatable code) to enable the user to reduce system software costs while at the same time increasing software reliability and efficiency.

S6800

Absolute Maximum Ratings

Supply Voltage, V_{CC}	− 0.3V to + 7.0V
Input Voltage, V_{IN}	− 0.3V to + 7.0V
Operating Temperature Range, T_A	0°C to + 70°C
Storage Temperature Range, T_{stg}	− 55°C to + 150°C
Thermal Resistance, θ_{JA}	
Plastic	100°C/W
Ceramic	50°C/W

This device contains circuitry to protect the inputs against damage due to high static voltage or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%; V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage — Logic, EXtal	V_{SS} + 2.0		V_{DD}	Vdc	
	$\overline{RESET}$	V_{SS} + 4.0		V_{DD}		
V_{IL}	Input Low Voltage — Logic EXtal, $\overline{RESET}$	V_{SS} – 0.3		V_{SS} + 0.8	Vdc	
I_{in}	Input Leakage Current — Logic		1.0	2.5	μAdc	V_{in} = 0 to 5.25V, V_{CC} = max
V_{OH}	Output High Voltage — D0-D7	V_{SS} + 2.4			Vdc	I_{Load} = – 205μAdc, V_{CC} = min
	A0-A15, R/$\overline{W}$, Q, E	V_{SS} + 2.4				I_{Load} = – 145μAdc, V_{CC} = min
	BA, BS	V_{SS} + 2.4				I_{Load} = – 100μAdc, V_{CC} = min
V_{OL}	Output Low Voltage			V_{SS} + 0.5	Vdc	I_{Load} = 2.0mAdc, V_{CC} = min
P_D	Power Dissipation			1.0	W	
C_{in}	Capacitance # — D_0-D_7		10	15	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
	Logic Inputs, EXtal		7	10		
C_{out}	A_0-A_{15}, R/$\overline{W}$			12		
f	Frequency of Operation — S6809			4	MHz	
f_{XTAL}	S68A09			6		
f_{XTAL}	(Crystal or External Input) — S68B09			8		
I_{TSI}	Three-State (Off State) Input Current — D_0-D_7		2.0	10	μAdc	V_{in} = 0.4 to 2.4V, V_{CC} = max
	A_0-A_{15}, R/W			100		

Read/Write Timing (Reference Figures 1 and 2)

		S6809			S68A09			S68B09				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{CYC}	Cycle Time	1000			667			500			ns	
t_{UT}	Total Up Time	975			640			480			ns	$t_{ut} = t_{CYC} - t_{EF}$
t_{ACC}	Peripheral Read Access Time	695			440			320			ns	$t_{acc} = t_{ut} - t_{AD} - t_{DSR}$
t_{DSR}	Data Setup Time (Read)	80			60			40			ns	
t_{DHR}	Input Data Hold Time	10			10			10			ns	
t_{DHW}	Output Data Hold Time	30			30			30			ns	
t_{AH}	Address Hold Time (Address, R/$\overline{W}$)	20			20			20			ns	
t_{AD}	Address Delay			200			140			110	ns	
t_{DDW}	Data Delay Time (Write)			225			180			145	ns	
t_{AVS}	E_{low} to Q_{high} Time			250			165			125	ns	
t_{AQ}	Address Valid to Q_{high}	50			25			15			ns	
t_{PWEL}	Processor Clock Low	450			295			210			ns	
t_{PWEH}	Processor Clock High	450			280			220			ns	
t_{PCSR}	MRDY Set Up Time	125			125			125			ns	
t_{PCS}	Interrupts Set Up Time	200			140			110			ns	
t_{PCSH}	$\overline{HALT}$ Set Up Time	200			140			110			ns	
t_{PCSR}	$\overline{RESET}$ Set Up Time	200			140			110			ns	
t_{PCSD}	$\overline{DMA/BREQ}$ Set Up Time	125			125			125			ns	
t_{rc}	Crystal Osc Start Time	100			100			100			ms	
t_{ER}, t_{EF}	E Rise and Fall Time	5		25	5		25	5		20	ns	
t_{PCR}, t_{PLF}	Processor Control Rise/Fall			100			100			100	ns	
t_{QR}, t_{QF}	Q Rise and Fall Time	5		25	5		25	5		20	ns	
t_{PWQH}	Q Clock High	450			280			220			ns	

Figure 1. Read Data From Memory or Peripherals

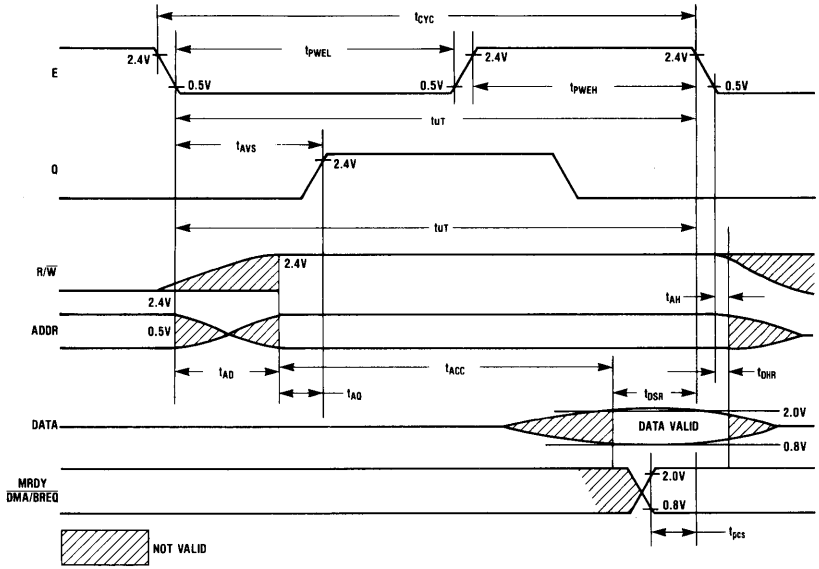
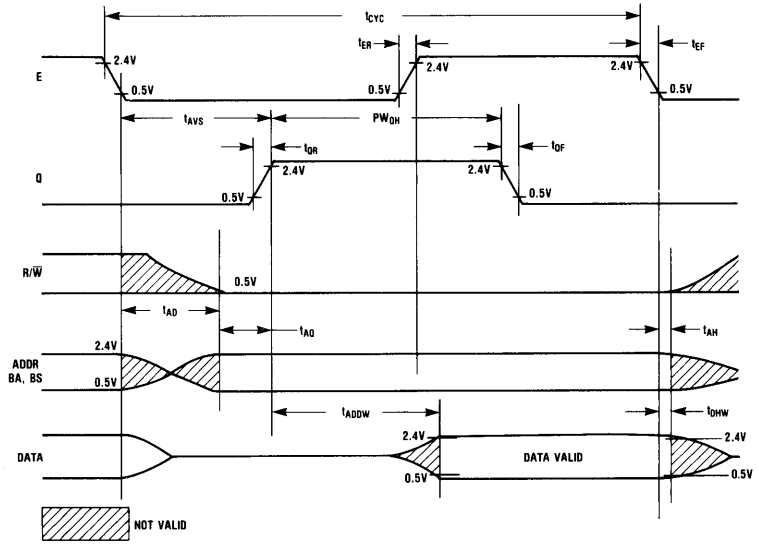
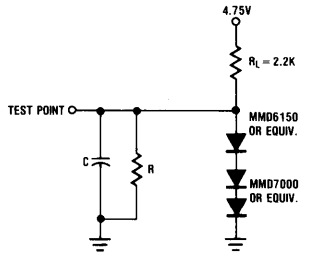


Figure 2. Write Data to Memory or Peripherals



S6800

Figure 3. Bus Timing Test Load



C = 30pF FOR BA, BS
130pF FOR D0-D7, E, Q
90pF FOR A0-A15, R/W

R = 11.7kΩ FOR D0-D7
16.5kΩ FOR A0-A15, E, Q
24kΩ FOR BA, BS

Programming Model

As shown in Figure 4, the S6809 adds three registers to the set available in the S6800. The added registers include a direct page register, the User Stack pointer and a second Index Register.

Accumulators (A, B, D)

The A and B registers are general purpose accumulators which are used for arithmetic calculations and manipulation of data.

Certain instructions concatenate the A and B registers to form a single 16-bit accumulator. This is referred to as the D register, and is formed with the A register as the most significant byte.

Direct Page Register (DP)

The Direct Page Register of the S6809 serves to enhance the Direct Addressing Mode. The content of this register appears at the higher address outputs (A_8-A_{15}) during direct Addressing Instruction execution. This

Figure 4. Programming Model of the Microprocessing Unit

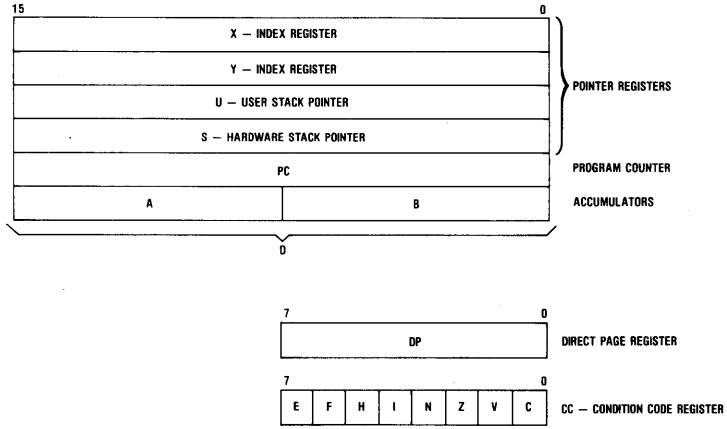
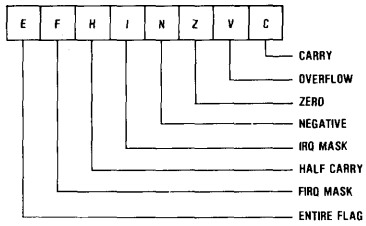


Figure 5. Condition Code Register Format



allows the direct mode to be used at any place in memory, under program control. To allow 6800 compatibility, all bits of this register are cleared during Processor Reset.

Index Registers (X, Y)

The Index Registers are used in indexed mode of addressing. The 16-bit address in this register takes part in the calculation of effective addresses. This address may be used to point to data directly or may be modified by an optional constant or register offset. During some indexed modes, the contents of the index register are incremented and decremented to point to the next item of tabular type data. All four pointer registers (X, Y, U, S) may be used as index registers.

Stack Pointers (U, S)

The Hardware Stack Pointer (S) is used automatically by the processor during subroutine calls and interrupts. The stack pointers of the S6809 point to the top of the stack, in contrast to the S6800 stack pointer which pointed to the next free location on the stack. The User Stack Pointer (U) is controlled exclusively by the programmer thus allowing arguments to be passed to and from subroutines with ease. Both Stack Pointers have the same indexed mode addressing capabilities as the X and Y registers, but also support **Push** and **Pull** instructions. This allows the S6809 to be used efficiently as a stack processor, greatly enhancing its ability to support higher level languages and modular programming.

Program Counter

The Program Counter is used by the processor to point to the address of the next instruction to be executed by the processor. Relative Addressing is provided allowing the Program Counter to be used like an index register in some situations.

Condition Code Register

The condition code register defines the State of the Processor at any given time, see Figure 5.

Bit 0 (C)

Bit 0 is the Carry Flag, and is usually the carry from the binary ALU. C is also used to represent a 'borrow' from subtract like instructions (CMP, NEG, SUB, SBC). Here the carry flag is the complement of the carry from the binary ALU.

Bit 1 (V)

Bit 1 is the overflow flag, and is set to a one by an operation which causes a signed two's complement arithmetic overflow. This overflow is detected in an operation in which the carry from the MSB in the ALU does not match the carry from the MSB-1.

Bit 2 (Z)

Bit 2 is the zero flag, and is set to a one if the result of the previous operation was identically zero.

Bit 3 (N)

Bit 3 is the negative flag, which contains exactly the value of the MSB of the result of the preceding operation. Thus, a negative two's-complement result will leave N set to a one.

Bit 4 (I)

Bit 4 is the $\overline{\text{IRQ}}$ mask bit. The processor will not recognize interrupts from the IRQ line if this bit is set to a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$, $\overline{\text{RESET}}$, and SWI all set I to a one; SWI2 and SWI3 do not affect I.

Bit 5 (H)

Bit 5 is the half-carry bit, and is used to indicate a carry from bit 3 in the ALU as a result of an 8-bit addition only (ADC or ADD). This bit is used by the DAA instruction to perform a BCD decimal add adjust operation. The state of this flag is undefined in all subtract-like instructions.

Bit 6 (F)

Bit 6 is the $\overline{\text{FIRQ}}$ mask bit. The processor will not recognize interrupts from the FIRQ line if this bit is a one. $\overline{\text{NMI}}$, $\overline{\text{FIRQ}}$, SWI, and $\overline{\text{RESET}}$ all set F to a one. $\overline{\text{IRQ}}$, SWI2 and SWI3 do not affect F.

Bit 7 (E)

Bit 7 is the entire flag, and when set to a one indicates that the complete machine state (all the registers) was stacked, as opposed to the subset state (PC and CC). The E bit of the *stacked* CC is used on a return from interrupt (RTI) to determine the extent of the unstacking. Therefore, the current E left in the Condition Code Register represents past action.

S6809 MPU Signal Description

Power (V_{SS}, V_{CC})

Two pins are used to supply power to the part: V_{SS} is ground or 0 volts, while V_{CC} is $+5.0V \pm 5\%$.

Address Bus (A_0-A_{15})

Sixteen pins are used to output address information from the MPU onto the Address Bus. When the processor does not require the bus for a data transfer, it will output address $FFFF_{16}$, R/$\overline{W}$ = 1, and BS = 0. Addresses are valid on the rising edge of Q (see Figures 1 and 2). All address bus drivers are made high-impedance when output Bus Available (BA) is high. Each pin will drive one Schottky TTL load and typically 90pF.

Data Bus (D_0-D_7)

These eight pins provide communication with the system bi-directional data bus. Each pin will drive one Schottky TTL load and typically 130pF.

Read/Write (R/$\overline{W}$)

This signal indicates the direction of the data transfer on the data bus. A low indicates that the MPU is writing data onto the data bus. R/$\overline{W}$ is made high impedance when BA is high. R/$\overline{W}$ is valid on the rising edge of Q, refer to Figures 1 and 2.

$\overline{\text{RESET}}$

A low level on this Schmitt-trigger input for greater than one bus cycle will reset the MPU as shown in Figure 6. The Reset vectors are fetched from locations $FFFE_{16}$ and $FFFF_{16}$ (Table 1) when Interrupt Acknowledge is true, (BA∧BS = 1). During initial power-on, the Reset line should be held low until the clock oscillator is fully operational; see Figure 7.

Because the S6809 Reset pin has a Schmitt-trigger input with a threshold voltage higher than that of standard peripherals, a simple R/C network may be used to reset the entire system. This higher threshold voltage insures that all peripherals are out of the reset state before the Processor.

$\overline{\text{HALT}}$

A low level on this input pin will cause the MPU to stop running at the end of the present instruction and remain halted indefinitely without loss of data. When Halted, the BA output is driven high indicating the buses are high-impedance. BS is also high which indicates the processor is in the Halt or Bus Grant state. While halted, the MPU will not respond to external real-time requests ($\overline{\text{FIRQ}}$, $\overline{\text{IRQ}}$) although $\overline{\text{DMA/BREQ}}$ will always be accepted, and $\overline{\text{NMI}}$ or $\overline{\text{RESET}}$ will be latched for later response. During the Halt state Q and E continue to run normally. If the MPU is not running ($\overline{\text{RESET}}$, $\overline{\text{DMA/BREQ}}$), a halted state (BA and BS = 1) can be achieved by pulling $\overline{\text{HALT}}$ low while $\overline{\text{RESET}}$ is still low. If $\overline{\text{DMA/BREQ}}$ and $\overline{\text{HALT}}$ are both pulled low, the processor will reach the last cycle of the instruction (by reverse cycle stealing) where the machine will then become halted. See Figure 8.

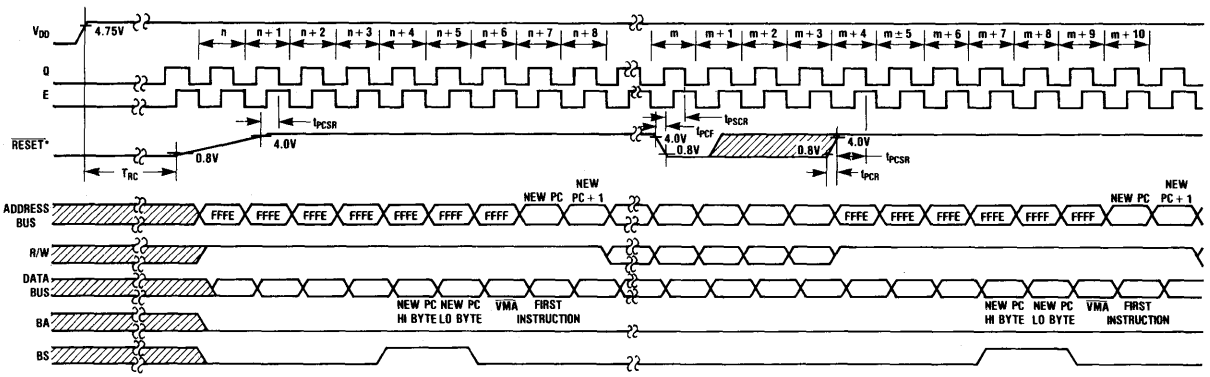
Bus Available, Bus Status (BA, BS)

The Bus Available output is an indication of an internal control signal which makes the MOS buses of the MPU high-impedance. This signal does not imply that the bus will be available for more than one cycle. When BA goes low, an additional dead cycle will elapse before the MPU acquires the bus.

The Bus Status output signal, when decoded with BA, represents the MPU state (valid with leading edge of Q):

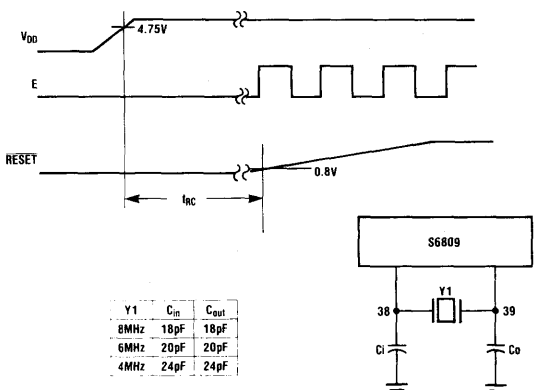
MPU State		
BA	BS	
0	0	Normal (Running)
0	1	Interrupt Acknowledge
1	0	SYNC Acknowledge
1	1	HALT or Bus Grant

Figure 6. $\overline{\text{RESET}}$ Timing



*NOTE: PARTS WITH DATE CODES PREFIXED BY 7F WILL COME OUT OF RESET ONE CYCLE SOONER THAN SHOWN

Figure 7. Crystal Connections and Oscillator Start Up



Y1	C_{in}	C_{out}
8MHz	18pF	18pF
6MHz	20pF	20pF
4MHz	24pF	24pF

6809 Crystal Parameters*

	3.58MHz	4.00MHz	6.0MHz	8.0MHz
RS	60Ω	50Ω	30-50Ω	20-40Ω
C_0	3.5pF	6.5pF	4-6pF	4-6pF
C_1	.015pF	.025pF	.01-.02pF	.01-.02pF
C_{in}-C_{out}	25pF	25pF	25pF	25pF
Q	40K	≅ 30K	≅ 20K	≅ 20K

All Parameters Are ± 10%.
*Note: These are representative AT-cut crystal parameters only. Crystals of other types of cut that work may also be used.

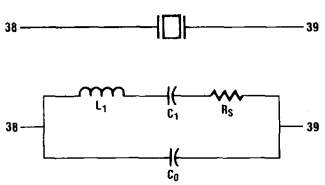
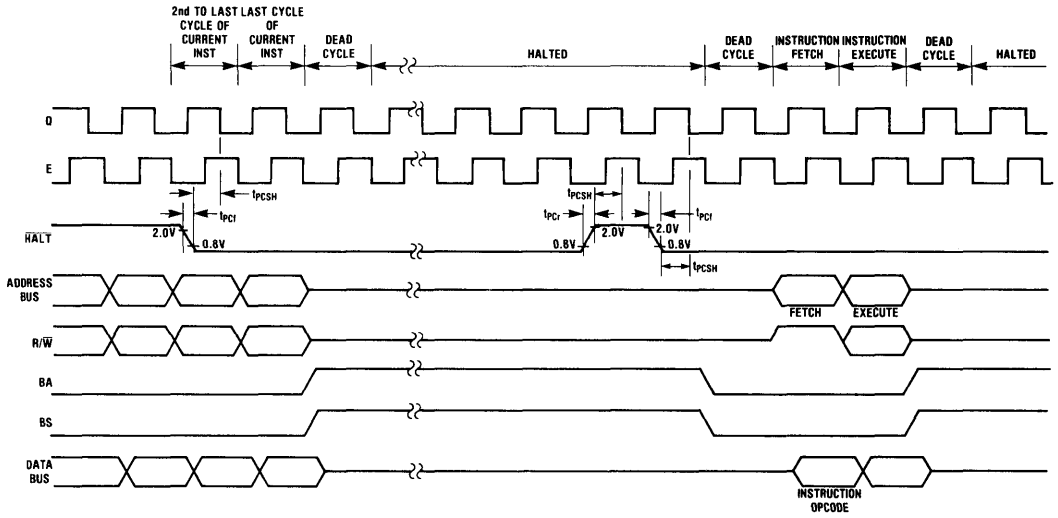


Figure 8. $\overline{HALT}$ and Single Instruction Execution for System Debug



Interrupt Acknowledge is indicated during both cycles of a hardware-vector-fetch ($\overline{RESET}$, $\overline{NMI}$, $\overline{FIRQ}$, $\overline{IRQ}$, SWI, SWI2, SWI3). This signal, plus decoding of the lower 4 address lines can provide the user with an indication of which interrupt level is being serviced and allow vectoring by device (see Table 1).

Sync Acknowledge is indicated while the MPU is waiting for external synchronization on an interrupt line.

Halt/Bus Grant is true when the S6809 is in a Halt or Bus Grant condition.

Table 1. Memory Map for Interrupt Vectors

Memory Map for Vector Location		Interrupt Vector Description
MS	LS	
FFFE	FFFF	$\overline{RESET}$
FFFC	FFFD	$\overline{NMI}$
FFFA	FFFB	SWI
FFF8	FFF9	$\overline{IRQ}$
FFF6	FFF7	$\overline{FIRQ}$
FFF4	FFF5	SWI2
FFF2	FFF3	SWI3
FFF0	FFF1	Reserved

*NOTE: $\overline{NMI}$, $\overline{FIRQ}$ and $\overline{IRQ}$ requests are latched by the falling edge of every Q except during cycle stealing operations (e.g., DMA) where only $\overline{NMI}$ is latched. From this point, a delay of at least one bus cycle will occur before the interrupt is serviced by the MPU.

Non-Maskable Interrupt ($\overline{NMI}$)

A negative edge on this input requests that a non-maskable interrupt sequence be generated. A non-maskable interrupt cannot be inhibited by the program, and also has a higher priority than $\overline{FIRQ}$, $\overline{IRQ}$ or software interrupts. During recognition of an $\overline{NMI}$, the entire machine state is saved on the hardware stack. After reset, an $\overline{NMI}$ will not be recognized until the first program load of the Hardware Stack Pointer (S). The pulse width of $\overline{NMI}$ low must be at least one E cycle. If the $\overline{NMI}$ input does not meet the minimum set up with respect to Q, the interrupt will not be recognized until the next cycle. See Figure 9.

Fast-Interrupt Request ($\overline{FIRQ}$)

A low level on this input pin will initiate a fast interrupt sequence, provided its mask bit (F) in the CC is clear. This sequence has priority over the standard Interrupt Request ($\overline{IRQ}$), and is fast in the sense that it stacks only the contents of the condition code register and the program counter. The interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 10.

Figure 9. $\overline{IRQ}$ and $\overline{NMI}$ Interrupt Timing

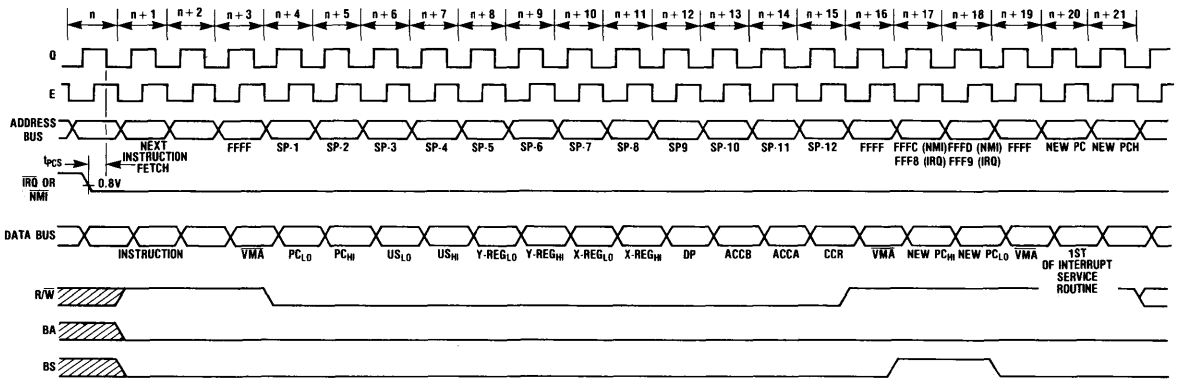
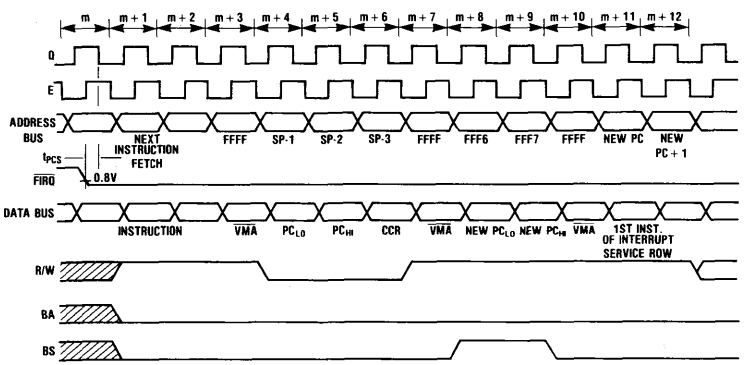


Figure 10. $\overline{FIRQ}$ Interrupt Timing



Interrupt Request ($\overline{IRQ}$)

A low level input on this pin will initiate an Interrupt Request sequence provided the mask bit (I) in the CC is clear. Since $\overline{IRQ}$ stacks the entire machine state it provides a slower response to interrupts than $\overline{FIRQ}$. $\overline{IRQ}$ also has a lower priority than $\overline{FIRQ}$. Again, the interrupt service routine should clear the source of the interrupt before doing an RTI. See Figure 9.

XTAL, EXTAL

These input pins are used to connect the on-chip oscillator to an external parallel-resonant crystal. Alternately, the pin EXTAL may be used as a TTL level input for external timing by grounding XTAL. The crystal or external frequency is 4 times the bus frequency, see Figure 7. Proper RF layout techniques should be observed in the layout of printed circuit boards.

E, Q

E is similar to the S6800 bus timing signal $\phi 2$; Q is a quadrature clock signal which leads E. Q has no parallel on the S6800. Addresses from the MPU will be valid with the leading edge of Q. Data is latched on the falling edge of E. Timing for E and Q is shown in Figure 11.

MRDY

This input control signal allows stretching of E to extend data-access time. When MRDY is high, E will be in normal operation. When MRDY is low, E may be stretched integral multiples of quarter (¼) bus cycles, thus allowing interface to slow memories as shown in Figure 12. A maximum stretch is 10 microseconds. During non-valid memory accesses ($\overline{VMA}$ cycles). MRDY has no effect on stretching E. This inhibits slowing the processor speed during "don't care" bus accesses.

$\overline{DMA/BREQ}$

The $\overline{DMA/BREQ}$ input provides a method of suspending execution and acquiring the MPU bus for another use as shown in Figure 13. Typical uses include DMA and dynamic memory refresh.

Transition of $\overline{DMA/BREQ}$ should occur during Q. A low level on this pin will stop instruction execution at the end of the current cycle. The MPU will acknowledge $\overline{DMA/BREQ}$ by setting BA and BS to a one. The requesting device will now have up to 15 bus cycles before the MPU retrieves the bus for self-refresh. Self-refresh requires one bus cycle with a leading and trailing dead cycle, see Figure 14.

Typically, the DMA controller will request to use the bus by asserting the $\overline{DMA/BREQ}$ pin low on the leading edge of E. When the MPU replies with BA = BS = 1, that cycle will be a dead cycle used to transfer control to the DMA controller.

False memory accesses should be prevented during any dead cycles. When BA is cleared (either as a result of

Figure 11. E/Q Relationship

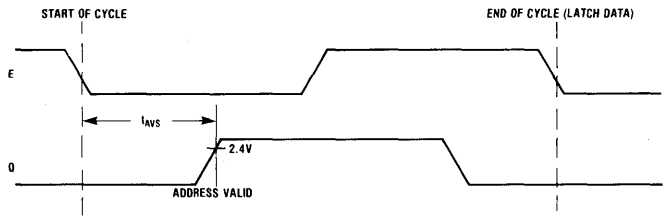


Figure 12. MRDY Timing

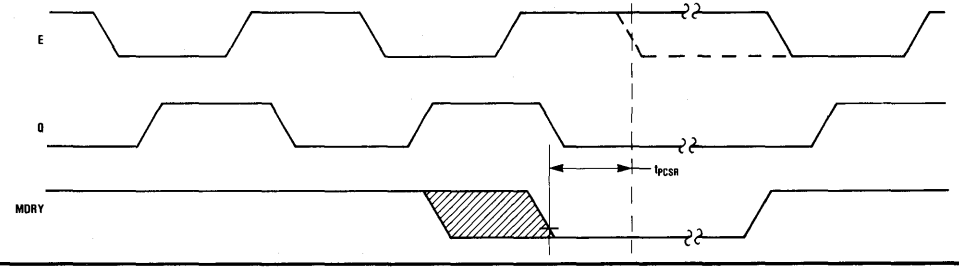


Figure 13. Typical DMA Timing (<14 Cycles)

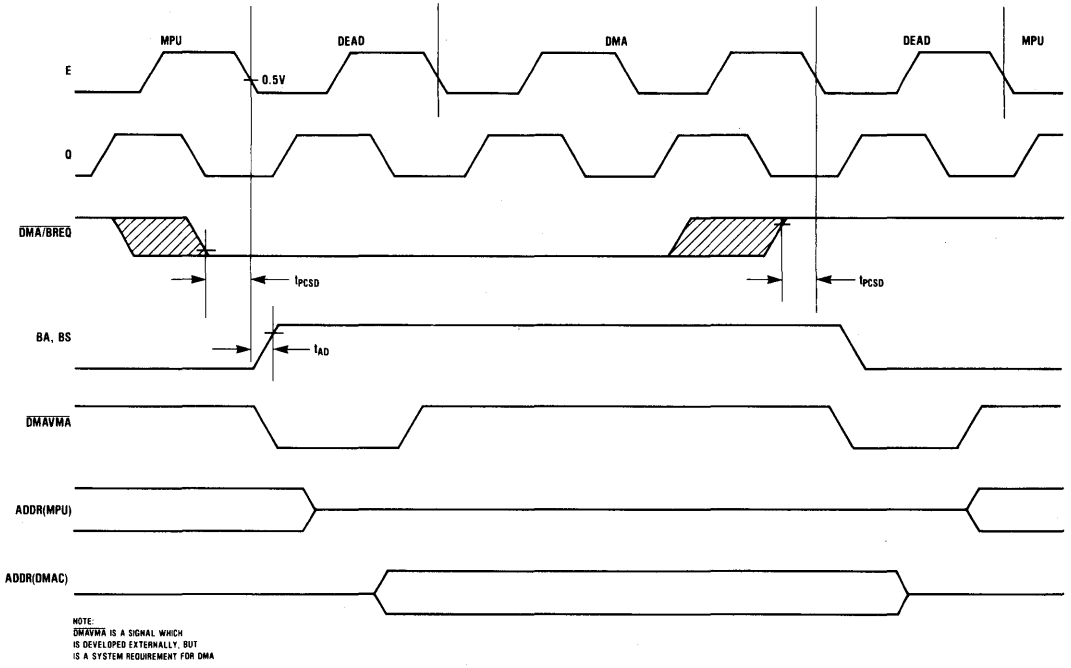
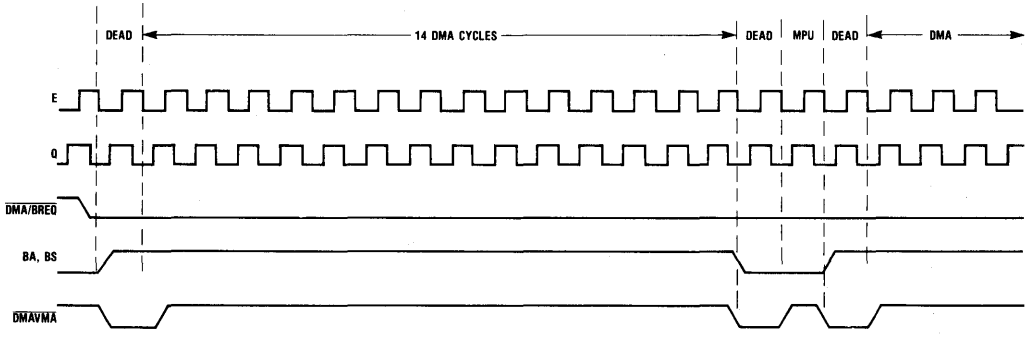


Figure 14. Auto-Refresh DMA Timing (<14 Cycles)



$\overline{DMA/BREQ}$ = HIGH or MPU self-refresh), the DMA device should be taken off the bus.

Another dead cycle will elapse before the MPU is allowed a memory access to transfer control without contention.

MPU Operation

During normal operation, the MPU fetches an instruction from memory and then executes the requested function. This sequence begins at $\overline{RESET}$ and is repeated indefinitely unless altered by a special instruction or hardware occurrence. Software instructions that alter normal MPU operation are: SWI, SWI2, SWI3, CWAI, RTI and SYNC. An interrupt, $\overline{HALT}$ or $\overline{DMA/BREQ}$ can also alter the normal execution of instructions. Figure 15 illustrates the flowchart for the S6809. The left-half of the flowchart represents normal operation; the right-half represents the flow when an interrupt when an interrupt or special instruction occurs.

Addressing Modes

The basic instructions of any computer are greatly enhanced by the presence of powerful addressing modes. The S6809 has the most complete set of addressing modes available on any microcomputer today. For example, the S6809 has 59 basic instructions, however it recognizes 1464 different variations of instructions and addressing modes. The new addressing modes support modern programming techniques. The following addressing modes are available on the S6809:

- Inherent (Includes Accumulator)
- Immediate
- Extended
  - Extended Indirect
- Direct
- Register
- Indexed
  - Zero-Offset
  - Constant Offset
  - Accumulator Offset
  - Auto Increment/Decrement
  - Indexed Indirect
- Relative
  - Short/Long Relative Branching
  - Program Counter Relative Addressing

Inherent (Includes Accumulator)

In this addressing mode, the opcode of the instruction contains all the address information necessary. Examples of Inherent Addressing are: ABX, DAA, SWI, ASRA, and CLRB.

Immediate Addressing

In Immediate Addressing, the effective addressing of the data is the location immediately following the opcode; the data to be used in the instruction immediately follows the opcode of the instruction. The S6809 uses both 8 and 16-bit immediate values depending on the size of argument specified by the opcode. Examples of instructions with Immediate Addressing are:

```
LDA #$20
LDX #$F000
LDY #CAT
```

Note: # signifies Immediate addressing, $ signifies hexadecimal value.

Extended Addressing

In Extended Addressing the contents of the two bytes immediately following the opcode fully specify the 16-bit effective address used by the instruction. Note that the address generated by an extended instruction defines an absolute address and is not position independent. Examples of Extended Addressing include:

```
LDA CAT
STX MOUSE
LDD $2000
```

Extended Indirect

As a special case of indexed addressing (discussed below), one level of indirection may be added to Extended Addressing. In Extended Indirect, the two bytes following the postbyte of an Indexed instruction contains the address of the address of the data.

```
LDA [CAT]
LDX [$FFFE]
STU [DOG]
```

Direct Addressing

Direct addressing is similar to extended addressing except that only one byte of address follows the opcode. This byte specifies the lower 8 bits of the address to be used. The upper 8 bits of the address are supplied by the direct page register. Since only one byte of address is required in direct addressing, this mode requires less memory and executes faster than extended addressing. Of course, only 256 locations (one page) can be accessed without redefining the contents of the DP register. Since the DP register is set to $00 on Reset, direct addressing on the S6809 is compatible with direct addressing on the S6800. Indirection is not allowed in direct addressing. Some examples of direct addressing are:

```
LDA    $30
SETDP  $10 (Assembler directive)
LDB    $1030
LDD    <CAT
```

Note: < is an assembler directive which forces direct addressing.

Register Addressing

Some opcodes are followed by a byte that defines a register or set of registers to be used by the instruction, this is called a POSTBYTE. Some examples of register addressing are:

TFR	X,Y	Transfers X into Y
EXG	A,B	Exchanges A with B
PSHS	A,B,X,Y	Push onto S Y,X,B, then A
PULU	X,Y,D	Pull from U D,X, then Y

Indexed Addressing

In all indexed addressing one of the pointer registers (X, Y, U, S, and sometimes PC) is used in a calculation of the effective address of the operand to be used by the instruction. Five basic types of indexing are available and are discussed below. The postbyte of an indexed instruction specifies the basic type and variation of the addressing mode as well as the pointer register to be used. Figure 16 lists the legal formats for the postbyte. Table 2 gives the assembler form and the number of cycles and bytes added to the basic values for indexed addressing for each variation.

Zero-Offset Indexed — In this mode, the selected pointer register contains the effective address of the data to be used by the instruction. This is the fastest indexing mode.

Examples are:

LDD 0,X
LDA 0,S

Constant Offset Indexed — In this mode a two's-complement offset and the contents of one of the pointer registers are added to form the effective address of the operand. The pointer register's initial content is unchanged by the addition.

Three sizes of offsets are available:

± 4-bit (– 16 to + 15)
± 7-bit (– 128 to + 127)
± 15-bit (– 32768 to + 32767)

The two's complement 5-bit offset is included in the postbyte and therefore is most efficient in use of bytes and cycles. The two's complement 8-bit offset is contained in a single byte following the postbyte. The two's complement 16-bit offset is in the two bytes following the postbyte. In most cases the programmer need not be concerned with the size of this offset since the assembler will select the optional size automatically.

Examples of constant-offset indexing are:

LDA 23,X
LDX -2,S
LDY 300,X
LDU CAT,Y

Figure 16. Indexed Addressing Postbyte Register Bit Assignments

POST—BYTE REGISTER BIT								INDEXED ADDRESSING MODE
7	6	5	4	3	2	1	0	
0	R	R	X	X	X	X	X	EA = ,R ± 4-BIT OFFSET
1	R	R	0	0	0	0	0	,R+
1	R	R	1	0	0	0	1	,R+ +
1	R	R	0	0	0	1	0	,–R
1	R	R	1	0	0	1	1	,– –R
1	R	R	1	0	1	0	0	EA = ,R ± 0 OFFSET
1	R	R	1	0	1	0	1	EA = ,R ± ACCB OFFSET
1	R	R	1	0	1	1	0	EA = ,R ± ACCA OFFSET
1	R	R	1	1	0	0	0	EA = ,R ± 7-BIT OFFSET
1	R	R	1	1	0	0	1	EA = ,R ± 15-BIT OFFSET
1	R	R	1	1	0	1	1	EA = ,R ± D OFFSET
1	X	X	1	1	1	0	0	EA = ,PC ± 7-BIT OFFSET
1	X	X	1	1	1	0	1	EA = ,PC ± 15-BIT OFFSET
1	R	R	1	1	1	1	1	EA = ,ADDRESS

ADDRESSING MODE FIELD
INDIRECT FIELD
SIGN BIT WHEN B7 = 0
REGISTER FIELD
00:R = X
01:R = Y
10:R = U
11:R = S
X = DON'T CARE

Accumulator-Offset Indexed — This mode is similar to constant offset indexed except that the two's complement value in one of the accumulators (A, B or D) and the content of one of the pointer registers are added to form the effective address of the operand. The contents of both the accumulator and the pointer register are unchanged by the addition. The postbyte specifies which accumulator to use as an offset and no additional bytes are required. The advantage of an accumulator offset is that the value of the offset can be calculated by a program at run-time.

Some examples are:

LDA B,Y
LDX D,Y
LEAX B,X

Auto Increment/Decrement Indexed — In the auto increment addressing mode, the pointer register contains the address of the operand. Then, after the pointer register is used it is incremented by one or two. This addressing mode is useful in stepping through tables, moving data, or for the creation of software stacks. In auto

Table 2. Indexed Addressing Modes

Type	Forms	Non Indirect				Indirect			
		Assembler Form	Postbyte OP Code	+ ~	+ #	Assembler Form	Postbyte OP Code	+ ~	+ #
Constant Offset From R (Signed Offsets)	No Offset	,R	1RR00100	0	0	[,R]	1RR10100	3	0
	5-Bit Offset	n, R	0RRnnnnn	1	0	defaults to 8-bit			
	8-Bit Offset	n, R	1RR01000	1	1	[n, R]	1RR11000	4	1
	16-Bit Offset	n, R	1RR01001	4	2	[n, R]	1RR11001	7	2
Accumulator Offset From R (Signed Offsets)	A — Register Offset	A, R	1RR00110	1	0	[A, R]	1RR10110	4	0
	B — Register Offset	B, R	1RR00101	1	0	[B, R]	1RR10101	4	0
	D — Register Offset	D, R	1RR01011	4	0	D, R]	1RR11011	7	0
Auto Increment/Decrement R	Increment By 1	,R+	1RR00000	2	0	not allowed			
	Increment By 2	,R++	1RR00001	3	0	[,R++]	1RR10001	6	0
	Decrement By 1	,−R	1RR00010	2	0	not allowed			
	Decrement By 2	,−−R	1RR00011	3	0	[,−−R]	1RR10011	6	0
Constant Offset From PC	8-Bit Offset	n, PCR	1XX01100	1	1	[n, PCR]	1XX11100	4	1
	16-Bit Offset	n, PCR	1XX01101	5	2	[n, PCR]	1XX11101	8	2
Extended Indirect	16-Bit Address	—	—	—	—	[n]	10011111	5	2

$^{+}_{\sim}$ and $^{+}_{\#}$ indicate the number of additional cycles and bytes for the particular variation.

R = X, Y, U or S X = 00 Y = 01
X = Don't Care U = 10 S = 11

decrement, the pointer register is decremented prior to use as the address of the data. The use of auto decrement is similar to that of auto increment but the tables, etc. are scanned from the high to low addresses. The size of the increment/decrement can be either one or two to allow for tables of either 8 or 16-bit data to be accessed and is selectable by the programmer. The predecrement, post-increment nature of these modes allow them to be used to create additional software stacks that behave identically to the U and S stacks.

Some examples of the auto increment/decrement addressing modes are:

```
LDA ,X+
STD ,Y++
LDBL ,-Y
LDX ,--S
```

Indexed Indirect

All of the indexing modes with the exception of auto increment/decrement by one, or a ± 4-bit offset may have an additional level of indirection specified. In Indirect addressing, the effective address is contained at the location specified by the content of the Index register plus any offset. In the example below, the A accumulator is loaded indirectly using an effective address calculated from the Index register and an offset.

```
                                  Before Execution
                              A = XX (don't care)
                                  X = $F000
$0100  LDA      [10,X]    EA is now $F010
$F010  $F1                F150 is now the new EA
$F011  $5Q
$F150  $AA
                                  After Execution
                              A = $AA Actual Data Loaded
```

All modes of indexed indirect are included except those which are meaningless (e.g., auto increment/decrement by 1 indirect). Some examples of indexed indirect are:

```
LDA  [,X]
LDD  [10,S]
LDA  [B,Y]
LDD  [,X++]
```

Relative Addressing

The byte(s) following the branch opcode is (are) treated as a signed offset which is added to the program counter. If the branch condition is true then the calculated address (PC + signed offset) is loaded into the program counter. Program execution continues at the new location as indicated by the PC; Short (1 byte offset) and long (2 bytes offset) relative addressing modes are available. All of memory can be reached in long relative addressing as an effective address is interpreted modulo 2^{16}. Some examples of relative addressing are:

```
        BEQ   CAT     (short)
        BGT   DOG     (short
CAT     LBEQ  RAT     (long)
DOG     LBGT  RABBIT  (long)
        .
        .
        .
RAT     NOP
RABBIT  NOP
```

Program Counter Relative

The PC can be used as the pointer register with 8 or 16-bit signed offsets. As in relative addressing the offset is added to the current PC to create the effective address. The effective address is then used as the address of the operand or data. Program Counter Relative Addressing is used for writing position independent programs. Tables related to a particular routine will maintain the same relationship after the routine is moved, if referenced relative to the Program Counter. Examples are:

```
LDA     CAT,PCR
LEAX    TABLE, PCR
```

Since program counter relative is a type of indexing, an additional level of indirection is available.

```
LDA     [CAT,PCR]
LDU     (DOG,PCR]
```

S6809 Instruction Set

The instruction set of the S6809 is similar to that of the S6800 and is upward compatible at the source code level. The number of opcodes has been reduced from 72 to 59, but because of the expanded architecture and additional addressing modes, the number of available opcodes (with different addressing modes) has risen from 197 to 1464.

Some of the new instructions and addressing modes are described in detail below:

PSHU/PSHS

The push instructions have the capability of pushing onto either the hardware stack (S) or user stack (U) any or all of the MPU registers with a single instruction.

PULU/PULS

The pull instructions have the same capability of the push instruction, in reverse order. The byte immediately following the push or pull opcode determines which register or registers are to be pushed or pulled. The actual PUSH/PULL sequence is fixed; each bit defines a unique register to push or pull as shown in Figure 17.

TFR/EXG

Within the S6809, any register may be transferred to or exchanged with another of like-size, i.e., 8-bit to 8-bit or 16-bit to 16-bit. Bits 4-7 of postbyte define the source register, while bits 0-3 represent the destination register. These are denoted as follows:

```
0000 – D     0101 – PC
0001 – X     1000 – A
0010 – Y     1001 – B
0011 – U     1010 – CC
0100 – S     1011 – DP
```

Note: All other combinations are undefined and INVALID.

Load Effective Address

The LEA works by calculating the effective address used in an indexed instruction and stores that address value, rather than the data at that address, in a pointer register. This makes all the features of the internal addressing hardware available to the programmer. Some of the implications of this instruction are illustrated in the following table of examples:

The LEA Instruction also allows the user to access data in a position independent manner. For example:

```
        LEAX  MSG1, PCR
        LBSR  PDATA (Print message routine)

MSG1 FCC  'MESSAGE'
```

Figure 17. Push/Pull Postbyte

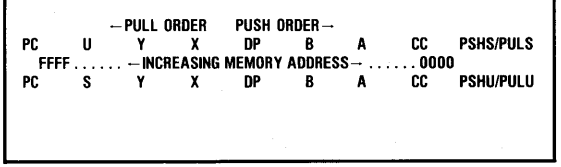


Table 3. LEA Examples

Instruction	Operation	Comment
LEAX 10, X	X+10 →X	Adds 5-bit constant 10 to X
LEAX 500, X	X+500 →X	Adds 6-bit constant 500 to X
LEAY A, Y	Y+A →Y	Adds 8-bit accumulator to Y
LEAY D, Y	Y+D →Y	Adds 16-bit D accumulator to Y
LEAU −10, U	U−10 →U	Subtracts 10 from U
LEAS −10, S	S−10 →S	Used to reserve area on stack
LEAS 10, S	S+10 →S	Used to 'clean up' stack
LEAX 5, S	S+5 →X	Transfers as well as adds

This sample program prints "message." By writing MSG1,PCR, the assembler computes the distance between the present address and MSG1. This result is placed as a constant into the LEAX instruction which will be indexed from the PC value at the time of execution. No matter where the code is located, when it is executed, the computed offset from the PC will put the absolute address of MSG1 into the X pointer register. This code is totally position independent.

MUL

Multiplies the unsigned binary numbers in the A and B accumulator and places the unsigned result into the 16-bit D accumulator. This unsigned multiply also allows multiple-precision multiplications.

Long and Short Relative Branches

The S6809 has the capability of program counter relative branching throughout the entire memory map. In this mode, if the branch is to be taken, the 8 or 16-bit signed offset is added to the value of the program counter to be used as the effective address. This allows the program to branch anywhere in the 64K memory map. Position independent code can be easily generated through the use of relative branching. Both short (8-bit) and long (16-bit) branches are available.

Sync

After encountering a Sync operation, the MPU enters a Sync state, stops processing instructions and waits for an interrupt. If the pending interrupt is non-maskable ($\overline{NMI}$) or maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) clear, the processor will clear the Sync state and perform the normal interrupt stacking and service routine. Since $\overline{FIRQ}$ and $\overline{IRQ}$ are not edge-triggered, a low level with a minimum duration of three cycles is required to assure that the interrupt will be taken. If the pending interrupt is maskable ($\overline{FIRQ}$, $\overline{IRQ}$) with its mask bit (F or I) set, the processor will clear the Sync state and continue processing in sequence. Figure 18 depicts Sync timing.

Software Interrupts

A Software Interrupt is an instruction which will cause an interrupt, and its associated vector fetch. These Software Interrupts are useful in operating system calls, software debugging, trace operations, memory mapping, and software development systems. Three levels of SWI are available on this S6809, and are prioritized in the following order: SWI, SWI2, SWI3.

16-Bit Operations

The S6809 has the capability of processing 16-bit data. These instructions include loads, stores, compares, adds, subtracts, transfers, exchanges, pushes and pulls.

Cycle-by-Cycle Operation

The address bus cycle-by-cycle performance chart illustrates the memory-access sequence corresponding to each possible instruction and addressing mode in the S6809. Each instruction begins with an opcode fetch. While that opcode is being internally decoded, the next program byte is always fetched. (Most instructions will use the next byte, so this technique considerably speeds throughput). Next, the operation of each opcode will follow the flowchart. $\overline{VMA}$ is an indication of $FFFF_{16}$ on the address bus, $R/\overline{W} = 1$ and $BS = 0$. The following examples illustrate the use of the chart; see Figure 19.

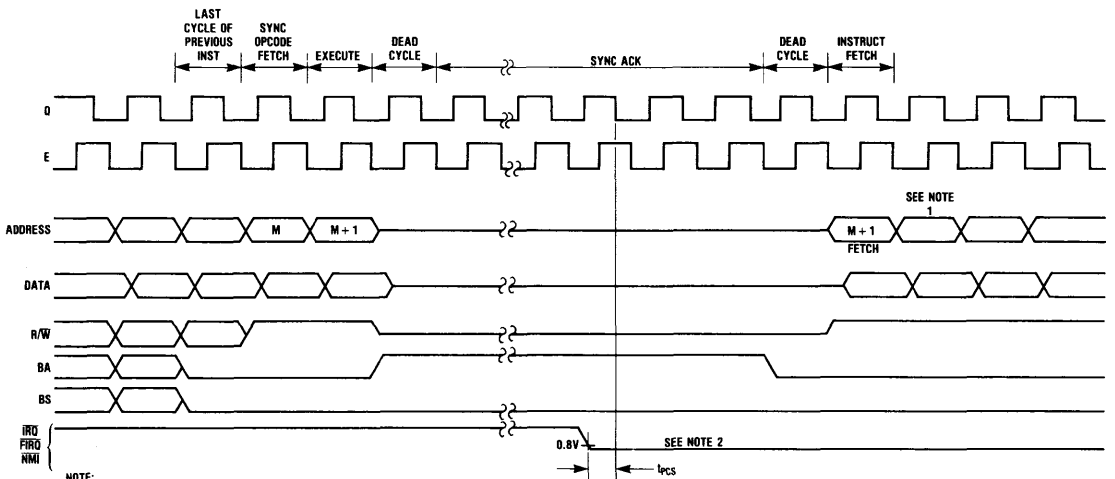
LBSR (Branch taken)

Cycle #	
1	opcode Fetch
2	opcode +
3	opcode +
4	$\overline{VMA}$
5	$\overline{VMA}$
6	ADDR
7	$\overline{VMA}$
8	STACK (write)
9	STACK (write)

DEC (Extended)

1	opcode Fetch
2	opcode +
3	opcode +
4	$\overline{VMA}$
5	ADDR (read)
6	$\overline{VMA}$
7	ADDR (write)

Figure 18. SYNC Timing



NOTE:

1. IF THE MASK BIT IS SET WHEN THE INTERRUPT IS REQUESTED PROCESSING WILL CONTINUE WITH INSTRUCTION EXECUTION FETCHED FROM PREVIOUS STEP. HOWEVER, IF AN $\overline{NMI}$ OR AN UNMASKED $\overline{FIRQ}$ OR $\overline{IRQ}$ CAUSED INTERRUPT, THE ADDRESS PLACED ON BUS FROM PREVIOUS CYCLE (M + 1) REMAINS ON BUS AND PROCESSING CONTINUES WITH THIS CYCLE AS (m + 1) OR (n + 1) OF INTERRUPT TIMING.
2. IF MASK BITS ARE CLEAR $\overline{IRQ}$ & $\overline{FIRQ}$ MUST BE HELD LOW FOR THREE CYCLES TO GUARANTEE INTERRUPT TO BE TAKEN, ALTHOUGH ONLY ONE CYCLE IS NECESSARY TO BRING THE PROCESSOR OUT OF SYNC.

S6809 Instruction Set Tables

The instructions of the S6809 have been broken down into six different categories. They are as follows:

8-Bit Operation (Table 4)
16-Bit Operation (Table 5)
Index Register/Stack Pointer Instructions (Table 6)
Relative Branches (Long and Short) (Table 7)
Miscellaneous Instructions (Table 8)
Hexadecimal Value Instructions (Table 9)

Table 4. 8-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADCA, ADCB	Add memory to accumulator with carry
ADDA, ADDB	Add memory to accumulator
ANDA, ANDB	And memory with accumulator
ASL, ASLA, ASLB	Arithmetic shift of accumulator or memory left
ASR, ASRA, ASRB	Arithmetic shift of accumulator or memory right
BITA, BITB	Bit test memory with accumulator
CLR, CLRA, CLRB	Clear accumulator or memory location
CMPA, CMPB	Compare memory from accumulator
COM, COMA, COMB	Complement accumulator or memory location
DAA	Decimal adjust A-accumulator
DEC, DECA, DECB	Decrement accumulator or memory location
EORA, EORB	Exclusive OR memory with accumulator
EXG R1, R2	Exchange R1 with R2 (R1, R2=A, B, CC, DP)
INC, INCA, INCB	Increment accumulator or memory location
LDA, LDB	Load accumulator from memory
LSL, LSLA, LSLB	Logical shift left accumulator or memory location
LSR, LSRA, LSRB	Logical shift right accumulator or memory location
MUL	Unsigned multiply (A x B→D)
NEG, NEGA, NEGB	Negate accumulator or memory
ORA, ORB	OR memory with accumulator
ROL, ROLA, ROLB	Rotate accumulator or memory left
ROR, RORA, RORB	Rotate accumulator or memory right
SBCA, SBCB	Subtract memory from accumulator with borrow
STA, STB	Store accumulator to memory
SUBA, SUBB	Subtract memory from accumulator
TST, TSTA, TSTB	Test accumulator or memory location
TFR, R1, R2	Transfer R1 to R2 (R1, R2=A, B, CC, DP)

NOTE: A, B, CC, or DP may be pushed to (pulled from) either stack with PSHS, PSHU, (PULS, PULU) instructions.

Table 5. 16-Bit Accumulator and Memory Instructions

Mnemonic(s)	Operation
ADDD	Add memory to D accumulator
CMPD	Compare memory from D accumulator
EXG D, R	Exchange D with X, Y, S, U or PC
LDD	Load D accumulator from memory
SEX	Sign Extend B accumulator into A accumulator
STD	Store D accumulator to memory
SUBD	Subtract memory from D accumulator
TFR D, R	Transfer D to X, Y, S, U or PC
TFR R, D	Transfer X, Y, S, U or PC to D

Table 6. Index Register/Stack Pointer Instructions

Mnemonic(s)	Operation
CMPS, CMPU	Compare memory from stack pointer
CMPX, CMPY	Compare memory from index register
EXG R1, R2	Exchange D, X, Y, S, U or PC with D, X, Y, S, U or PC
LEAS, LEAU	Load effective address into stack pointer
LEAX, LEAY	Load effective address into index register
LDS, LDU	Load stack pointer from memory
LDX, LDY	Load index register from memory
PSHS	Push any register(s) onto hardware stack (except S)
PSHU	Push any register(s) onto user stack (except U)
PULS	Pull any register(s) from hardware stack (except S)
PULU	Pull any register(s) from hardware stack (except U)
STS, STU	Store stack pointer to memory
STX, STY	Store index register to memory
TFR R1, R2	Transfer D, X, Y, S, U or PC to D, X, Y, S, U or PC
ABX	Add B accumulator to X (unsigned)

Table 7. Branch Instructions

Mnemonic(s)	Operation
BCC, LBCC	Branch if carry clear
BCS, LBCS	Branch if carry set
BEQ, LBEQ	Branch is equal
BGE, LBGE	Branch if greater than or equal (signed)
BGT, LBGT	Branch if greater (signed)
BHI, LBHI	Branch if higher (unsigned)
BHS, LBHS	Branch is higher or same (unsigned)
BLE, LBLE	Branch if less than or equal (signed)
BLO, LBLO	Branch if lower (unsigned)
BLS, LBLS	Branch if lower or same (unsigned)
BLT, LBLT	Branch if less than (signed)
BMI, LBMI	Branch if minus
BNE, LBNE	Branch if not equal
BPL, LBPL	Branch is plus
BRA, LBRA	Branch always
BRN, LBRN	Branch never
BSR, LBSR	Branch to subroutine
BVC, LBVC	Branch if overflow clear
BVS, LBVS	Branch if overflow set

Table 8. Miscellaneous Instructions

Mnemonic(s)	Operation
ANDCC	AND condition code register
CWAI	AND conditon code register, then wait for interrupt
NOP	No operation
ORCC	OR condition code register
JMP	Jump
JSR	Jump to subroutine
RTI	Return from interrupt
RTS	Return from subroutine
SWI, SWI2, SWI3	Software interrupt (absolute indirect)
SYNC	Synchronize with interrupt line

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S6809E/S68A09E/S68B09E

8-BIT MICROPROCESSING UNIT

Features

- ☐ Interfaces With All S6800 Peripherals
- ☐ Upward Compatible Instruction Set and Addressing Modes
- ☐ Upward Source Compatible Instruction Set and Addressing Modes
- ☐ Two 8-Bit Accumulators Can Be Concatenated Into One 16-Bit Accumulator
- ☐ External Clock Inputs, E and Q, Allow System Synchronization

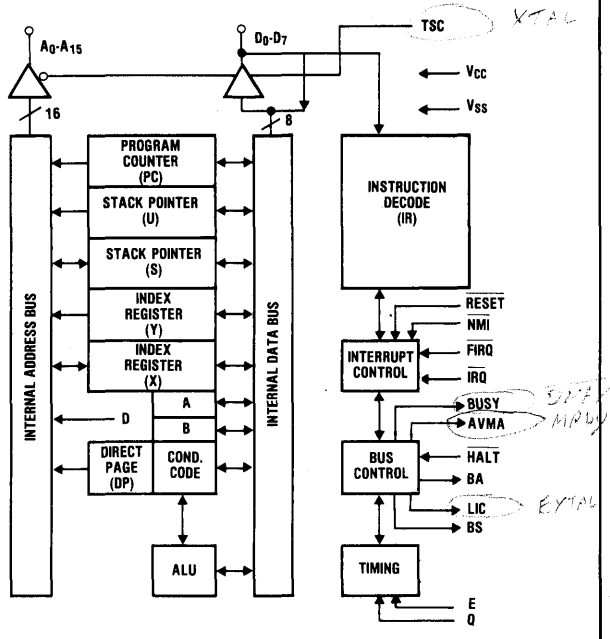
General Description

The S6809E is an advanced processor within the S6800 family offering greater throughput, improved byte efficiency, and increased adaptability to various software disciplines. These include position independence, reentrancy, recursion, block structuring, and high level language generation.

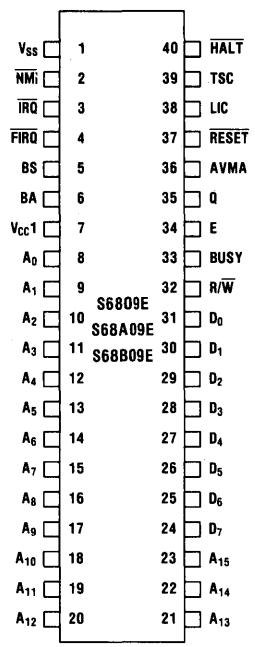
Because the S6809E supports *position-independent* code, software can be written in modular form for easy user expansion as system requirements increase. The S6809E is hardware compatible with all S6800 peripherals, and any assembly language code prepared for the S6800 can be passed through the S6809 assembler to produce code which will run on the S6809E.

S6800

Block Diagram



Pin Configuration



S6809E Hardware Features

- ☐ Fast Interrupt Request Input: Stacks Only Program Counter and Condition Code
- ☐ Interrupt Acknowledge Output Allows Vectoring by Devices
- ☐ Three Vectored Priority Interrupt Levels
- ☐ SYNC Acknowledge Output Allows for Synchronization to External Event
- ☐ NMI Blocked After RESET Until After First Load of Stack Pointer
- ☐ Early Address Valid Allows Use With Slow Memories
- ☐ Last Instruction Cycle Output (LIC) for Signalling Opcode Fetch
- ☐ Busy Output Eases Multiprocessor Design

Instruction Set

- ☐ Extended Range Branches
- ☐ Load Effective Address
- ☐ 16-Bit Arithmetic
- ☐ 8×8 Unsigned Multiply (AccumulatorA*B)
- ☐ SYNC Instruction—Provides Software Sync With an External Hardware Process
- ☐ Push and Pull on 2 Stacks
- ☐ Push/Pull Any or All Registers
- ☐ Index Registers May be Used as a Stack Pointer
- ☐ Transfer/Exchange all Registers

Addressing Modes

- ☐ All S6800 Modes Plus PC Relative Extended Indirect, Indexed Indirect, and PC Relative Indirect
- ☐ Direct Addressing Available Anywhere in Memory Map
- ☐ PC Relative Addressing: Byte Relative (±32,768 Bytes From PC)
- ☐ Complete Indexed Addressing Including Automatic Increment and Decrement, Register Offsets, and Four Indexable Register (X, Y, U and S)
- ☐ Expanded Index Addressing
  - ☐ 0, 5, 8, 16-Bit Constant Offset
  - ☐ 8, 16-Bit Accumulator Offsets

The S6809E gives the user 8- and 16-bit word capability with several hardware enhancements in the design such as the Fast Interrupt Request ($\overline{FIRQ}$), Memory Ready (MRDY), and Quadrature (Q_{OUT}) and System Clock Outputs (E_{OUT}). With the Fast Interrupt Request ($\overline{FIRQ}$) the S6809E places *only* the Program Counter and Condition Code Register on the stack prior to accessing the $\overline{FIRQ}$ vector location. The Memory Ready ($\overline{MRDY}$) input allows extension of the data access time for use with slow memories. The System Clock (E_{OUT}) operates at the basic processor frequency and can be as the synchronization signal for the entire system. The Quadrature Output (Q_{OUT}) provides additional system timing by signifying that address and data are stable.

The External Clock mode of the S6809E is particularly useful when synchronizing the processor to an externally generated signal. The Three-State Control input ($\overline{TSC}$) places the Address and R/$\overline{W}$ line in the high impedance state for DMA or Memory Refresh. The last Instruction Cycle (LIC) is activated during the last cycle of any instruction. This signifies that the next instruction cycle is the opcode fetch. The Processor Busy signal (BUSY) facilitates multiprocessor applications by allowing the designer to insure that flags being modified by one processor are not accessed by another simultaneously.

The S6809E features a family of addressing capabilities which can use any of the four index registers and stack pointers as a pointer to the operand (or the operand address). This pointer can have a fixed or variable signed offset that can be automatically incremented or decremented. The eight-bit direct page register permits a user to determine which page of memory is accessed by the instructions employing "page zero" addressing. This quick access to any page is especially useful in multitasking applications.

The S6809E has three vectored priority-interrupt levels, each of which automatically disables the lower priority interrupt while leaving the higher priority interrupt enabled.

The S6809E gives the system designer greater flexibility (through modular relocatable code) to enable the user to reduce system software costs while at the same time increasing software reliability and efficiency.

AMERICAN MICROSYSTEMS, INC.

S1602

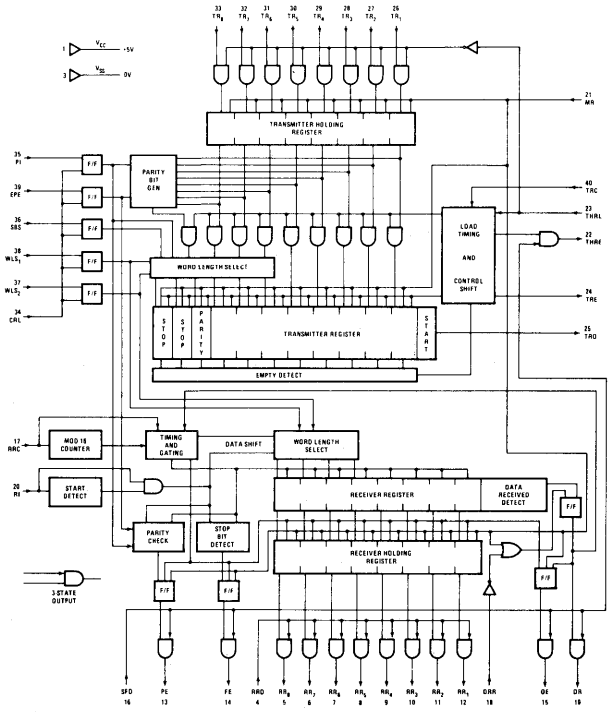
UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

Features

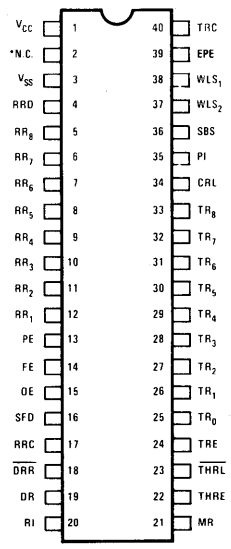
- ☐ Full or Half Duplex Operation — Can Receive and Transmit Simultaneously at Different Baud Rates.
- ☐ Completely Programmable — Data Word Length, Number of Stop Bits, Parity.
- ☐ Start Bit Generated Automatically
- ☐ Data and Clock Synchronization Performed Automatically
- ☐ Double Buffered—Eliminates Timing Difficulties
- ☐ Completely Static Circuitry
- ☐ Fully TTL Compatible.
- ☐ Three-state Output Capability
- ☐ Single Power Supply: +5V
- ☐ Standard 40-Pin Dual-in-Line Package
- ☐ Plug In Compatible with Western Digital TR1602A, TR1863, Fujitsu 8868A

S6800

Block Diagram



Pin Configuration



General Description

The AMI S1602 is a programmable Universal Asynchronous Receiver/Transmitter (UART) fabricated with N-Channel silicon gate MOS technology. All control pins, input pins and output pins are TTL compatible, and a single +5 volt power supply is used. The UART interfaces asynchronous serial data from terminals or other peripherals, to parallel data for a microprocessor, computer, or other terminal. Parallel data is converted by the transmitter section of the UART into a serial word consisting of the data as well as start, parity, and stop bit(s). Serial data is converted by the receiver section of the UART into parallel data. The receiver section verifies correct code transmission by parity checking and receipt of a valid stop bit. The UART can be programmed to accept word lengths of 5, 6, 7, or 8 bits. Even or odd parity can be set. Parity generation checking can be inhibited. The number of stop bits can be programmed for one, two, or one and one-half when transmitting a 5-bit code.

Absolute Maximum Ratings*

V_{CC} Pin Potential to V_{SS} Pin	−0.3V to +7.0V
Input Voltage	−0.3V to +7.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C

**Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheets. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Capacitance: $T_A = 25°$; f = 1MHz; $V_{IN} = 0V$

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance for all Inputs	10	—	pF

Guaranteed Operating Conditions (Referenced to V_{SS})

Symbol	Parameter	Operating Temperature	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	0°C to +70°C	4.75	5.0	5.25	V
V_{SS}			0.0	0.0	0.0	V
V_{IH}	Logic Input High Voltage	0°C to +70°C	2.2	—	V_{CC}	V
V_{IL}	Logic Input Low Voltage	0°C to +70°C	−0.3	—	+0.8	V

D.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{IL}	Input Leakage Current ($V_{IN} = 0$ to 5.25V, $V_{CC} = 5.25V$)	—	—	1.4	mA
I_{LZ}	Output Leakage Current for 3-State ($V_{OUT} = 0V$ to V_{CC}, SFD = RRD = V_{IH})	−20	—	+20	μA
V_{OL}	Output Low Voltage ($I_{OL} = 1.8mA$)	—	—	0.4	V
V_{OH}	Output High Voltage ($I_{OL} = -200\mu A$)	2.4	—	—	V
I_{CC}	V_{CC} Supply Current	—	70	—	mA

A.C. Characteristics (Guaranteed Operating Ranges Unless Otherwise Noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_C	Clock Frequency for RRC and TRC (Duty Cycle = 50%)	DC	—	800	kHz
t_{PWC}	CRL Pulse Width, High	200	—	—	ns
t_{PWT}	THRL Pulse Width, Low	180	—	—	ns
t_{PWR}	DRR Pulse Width, Low	180	—	—	ns
t_{PWM}	MR Pulse Width, High	150	—	—	ns
t_C	Coincidence Time (Figure 3 and Figure 8)	180	—	—	ns
t_{HOLD}	Hold Time (Figure 3 and Figure 8)	20	—	—	ns
t_{SET}	Setup Time (Figure 3 and Figure 8)	0	—	—	ns
t_{PD0}	Propagation Delay Time High to Low, Output (C_L = 130pF + 1TTL)	—	—	350	ns
t_{PD1}	Propagation Delay Time Low to High, Output (C_L = 130pF + 1TTL)	—	—	350	ns

Pin Description

Pin	Label	Function
1	V_{CC}	**Power Supply** — normally at +5V.
2	N.C.	**No connection.** On the S1602 this is an unconnected pin. On the TR1602A this is a −12V supply. −12V is not needed on the S1602 and thus the N.C. pin allows the S1602 to be compatible with the TR1602A.
3	V_{SS}	This is normally at 0V or ground.
4	RRD	**Receive Register Disconnect.** A high logic level, V_{IH}, on this pin disconnects the Receiver Holding Register outputs from the data outputs RR_8 — RR_1 on pin 5 — 12.
5 — 12	RR_8 — RR_1	**Receiver Holding Register Data.** These are the parallel outputs from the Receiver Holding Register if the RRD input is low (V_{IL}). Data is (LSB) right justified for character formats of less than eight bits, with RR_1 being the least significant bit. Unused MSBs are forced to a low logic output level, V_{OL}.
13	PE	**Parity Error.** This output pin goes to a high level if the received parity does not agree with that programmed by the Even Parity Enable input (pin 39). This output is updated as each character is transferred to the Receiver Holding Register. The Status Flag Disconnect input (pin 16) allows additional PE lines to be tied together by providing an output disconnect capability.
14	FE	**Framing Error.** This output pin goes high if the received character has no valid stop bit. Each time a character is transferred to the Receiver Holding Register, this output is updated. The Status Flag Disconnect input (pin 16) allows additional FE lines to be tied together by providing an output disconnect capability.
15	OE	**Overrun Error.** This output pin goes high if the Data Received Flag (pin 19) did not get reset before the next character was transferred to the Receive Holding Register. The Status Flag Disconnect input (pin 16) allows additional OE lines to be tied together providing an output disconnect capability.
16	SFD	**Status Flag Disconnect.** When this input is high, PE, FE, OE, DR and THRE outputs are forced to high impedance Three State allowing bus sharing capability.

Pin Description (Continued)

Pin	Label	Function
17	RRC	**Receive Register Clock.** This clock input is 16x the desired receiver shift rate.
18	$\overline{\text{DRR}}$	**Data Received Reset.** A low level input, V_{IL}, clears the Data Received (DR) line.
19	DR	**Data Received.** When a complete character has been received and transferred to the Receiver Holding Register, this output goes to the high level, V_{OH}.
20	RI	**Receiver Input.** Serial input data enters on this line. It is transfered to the Receiver Register as determined by the character length, parity and number of stop bits. When data is not being received, this input must remain high, V_{IH}.
21	MR	**Master Reset.** A high level pulse, V_{IH}, on this input clears the internal logic. The transmitter and Receive Registers, Receiver Holding Registers, FE, OE, PE, DRR are reset. In addition, the serial output line is set to a high level, V_{OH}.
22	THRE	**Transmitter Holding Register Empty.** This output will go high when the Transmitter Holding Register completes transfer of its contents to the Transmitter Register. The high level indicates a new character may be loaded into the Transmitter Holding Register.
23	$\overline{\text{THRL}}$	**Transmitter Holding Register Load.** When a low level, V_{IL}, is applied to this input, a character is loaded into the Transmitter Holding Register. The character is transferred to the Transmitter Register on a low to high level, V_{IH}, transition as long as the Transmitter Register is not currently in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until the transmission is completed. The new character is then transferred simultaneously with the start of the serial transmission of the new character.
24	TRE	**Transmitter Register Empty.** Goes high when the Transmitter Register has completed the serial transmission of a full character including the required number of stop bits. A high will be maintained until the start of transmission of the next character.
25	TRO	**Transmitter Register Output.** Transmits the Transmitter Register contents (Start bit, Data bits, Parity bit and Stop bit(s)) serially. Remains high, V_{OH}, when no data is being transmitted. Therefore, start of transmission is determined by transition of the Start bit from high to low level voltage, V_{OL}.
26—33	$TR_1 - TR_8$	**Transmitter Register Data Inputs.** The THRL strobe loads the character on these lines into the Transmitter Holding Register. If WLS_1 and WLS_2 have selected a character of less than 8 bits, the character is right justified to the least significant bit, TR_1 with the excess bits not used. A high input level, V_{IH}, will cause a high output level, V_{OH}, to be transmitted.
34	CRL	**Control Register Load.** The control bits, (WLS_1, WLS_2, EPE, PI, SBS), are loaded into the Control Register when the input is high. This input may be either strobed or hard wired to the high level.
35	PI	**Parity Inhibit.** Parity generation and verification circuitry are inhibited when this input is high. The PE output will be held low as well. When in the inhibit condition the Stop bit(s) will follow the last data bit on transmission.
36	SBS	**Stop Bit(s) Select.** A high level will select two Stop bits, and a low level selects one Stop bit. If 5-bit words are selected, a high level will generate one and one-half Stop bits.

Pin Description (Continued)

Pin	Label	Function
37, 38	WLS_2, WLS_1	**Word Length Select.** The state of these two (2) inputs determines the character length (exclusive of parity) as follows:

WLS_2	WLS_1	WORD LENGTH
LOW	LOW	5 bits
LOW	HIGH	6 bits
HIGH	LOW	7 bits
HIGH	HIGH	8 bits

Pin	Label	Function
39	EPE	**Even Parity Enable.** A high voltage level, V_{IH}, on this input will select even parity, while a low voltage level, V_{IL}, selects odd parity.
40	TRC	**Transmitter Register Clock.** The frequency of this clock input should be 16 times the desired baud rate.

Figure 1. Receiver Operating Timing

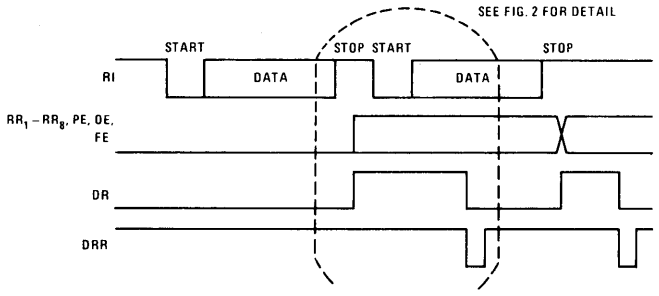
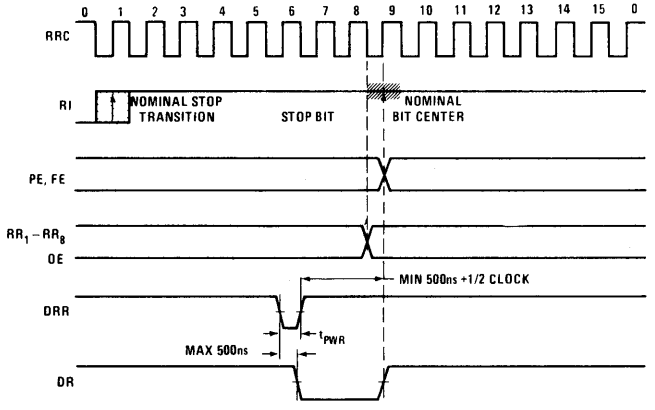


Figure 2. Timing for Status Flags, RR_1 thru RR_8 and DR



S6800

Figure 3. Transmitter Operating Timing

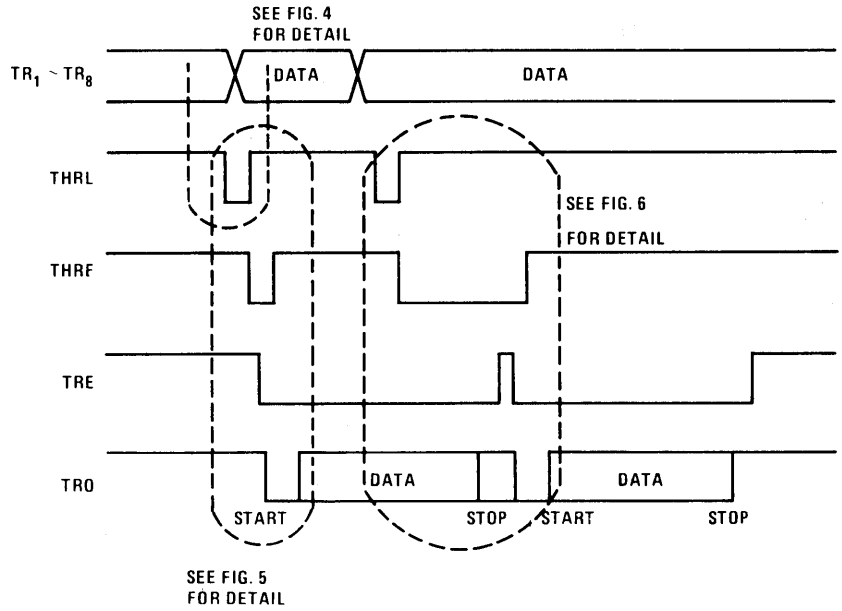


Figure 4. Data Input Load Cycle

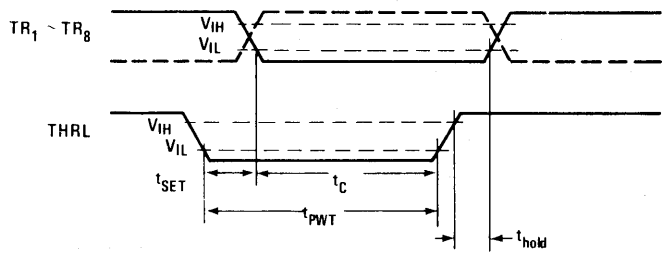
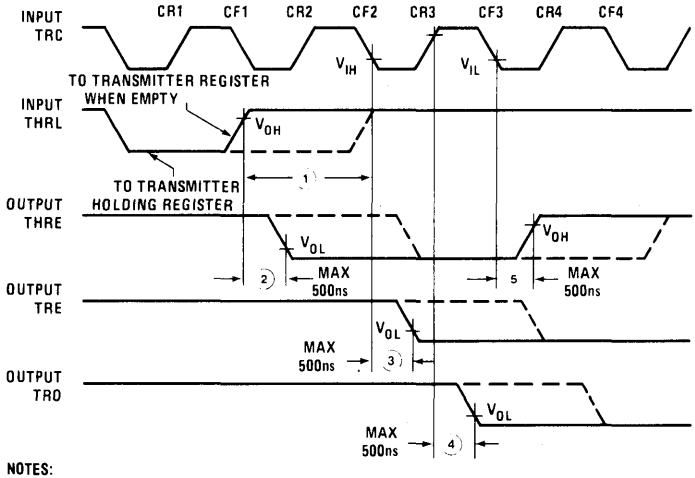


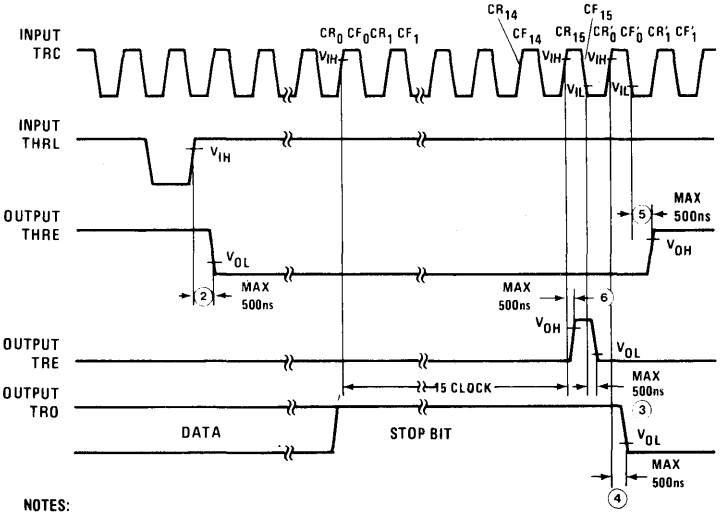
Figure 5. Transmitter Output Timing (1)



NOTES:

1. When the positive transition of THRL is 500ns or more before the falling edge of TRC (CF2 in the figure), TRE is enabled at CF2. But, when 500ns>(1)>0ns, TRE is invalid between CF2 and CF3.
2. THRE goes to low during 500ns Max. from the positive transition of THRL.
3. TRE goes to low during 500ns Max. from the first falling edge of TRC after THRE goes to low with TRE high.
4. TRO goes to low (START BIT) during 500ns Max. from the first rising edge of TRC after TRE goes to low.
5. THRE goes to high during 500ns Max. from the falling edge of TRC after START BIT is enabled.

Figure 6. Transmitter Output Timing (2)



NOTES:

2-5, refer to Figure 5.

6. TRANSMITTER REGISTER EMPTY goes to high during 500ns Max. from the 15th rising edge of TRC after STOP BIT is enables.

S6800

Figure 7. Input After Master Reset

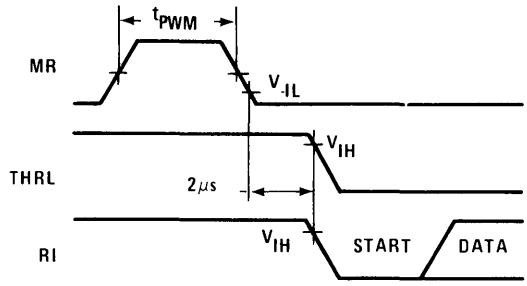


Figure 8. Control Register Load Cycle

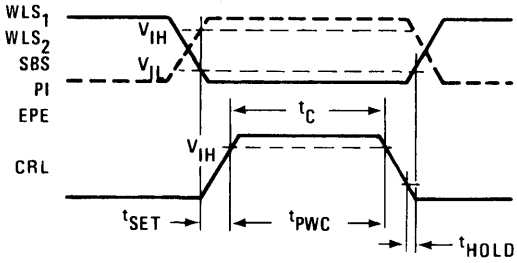


Figure 9. Status Flag Output

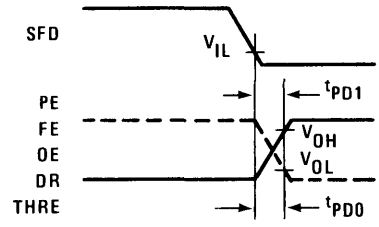
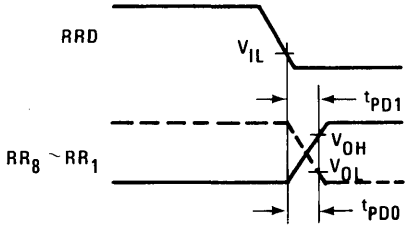


Figure 10. Data Output



AMERICAN MICROSYSTEMS, INC.

S2350

Universal Synchronous Receiver/Transmitter

Features

- ☐ **500kHz Data Rates**
- ☐ **Internal Sync Detection**
- ☐ **Fill Character Register**
- ☐ **Double Buffered Input/Output**
- ☐ **Bus Oriented Outputs**
- ☐ **5-8 Bit Characters**
- ☐ **Odd/Even or No Parity**
- ☐ **Error Status Flags**
- ☐ **Single Power Supply (+5V)**
- ☐ **Input/Output TTL-Compatible**

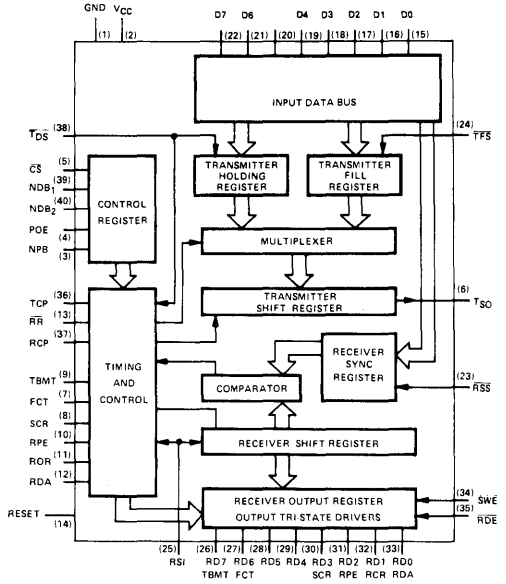
General Description

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial-to-parallel and parallel-to-serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

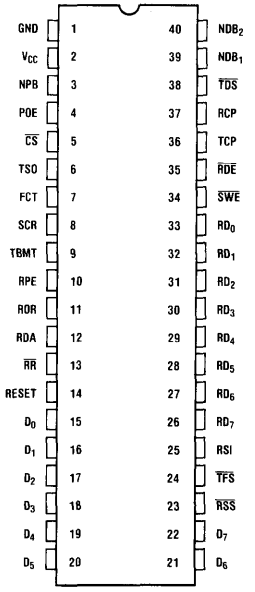
The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

S6800

Block Diagram



Pin Configuration



Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8-bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8-bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

Typical Applications

- ☐ Computer Peripherals
- ☐ Communication Concentrators
- ☐ Integrated Modems
- ☐ High Speed Terminals
- ☐ Time Division Multiplexing
- ☐ Industrial Data Transmission

Absolute Maximum Ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on any Pin with Respect to GROUND	+7V
Negative Voltage on any Pin with Respect to GROUND	−0.5V
Power Dissipation	0.75W

D.C. (Static) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		+0.8	V	
I_{IL}	Input Leakage Current			10	μA	V_{IN} = O_{TO} V_{CC} V
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
V_{OL}	Output Low Voltage			+0.4	V	I_{OL} = 1.6mA
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0V; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0V; f = 1.0MHz
I_{CC}	V_{CC} Supply Current			100	mA	No Load; V_{CC} = 5.25V

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

A.C. (Dynamic) Electrical Characteristics* (V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC		500	kHz	
Input Pulse Widths						
P_{TCP}	Transmit Clock	900			nsec	CL = 20pF
P_{RCP}	Receive Clock	900			nsec	1TTL Load
P_{RST}	Reset	500			nsec	
P_{TDS}	Transmit Data Strobe	200			nsec	
P_{TFS}	Transmit Fill Strobe	200			nsec	
P_{RSS}	Receive Sync Strobe	200			nsec	
P_{CS}	Control Strobe	200			nsec	
P_{RDE}	Receive Data Enable	400			nsec	Note 1
P_{SWE}	Status Word Enable	400			nsec	Note 1
P_{RR}	Receiver Restart	500			nsec	
Switching Characteristics						
T_{TSO}	Delay, TCP Clock to Serial Data Out			700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output			1.4	μsec	
T_{TBMT}	Delay, TDS to TBMT			700	nsec	
T_{STS}	Delay, SWE to Status Reset			700	nsec	
T_{RDO}	Delay, SWE, RDE to Data Outputs			400	nsec	1TTL Load
T_{HRDO}	Hold Time SWE, RDE to Off State			400	nsec	C_L = 130pF
T_{DTS}	Data Set Up Time TDS, TFS, RSS, CS	0			nsec	
T_{DTH}	Data Hold Time TDS	700			nsec	
T_{DTI}	Data Hold Time TFS, RSS	200			nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0			nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200			nsec	
T_{RDA}	Delay RDE to RDA Output	700			nsec	

NOTE 1: Required to reset status and flags.

Figure 1. Timing Waveform

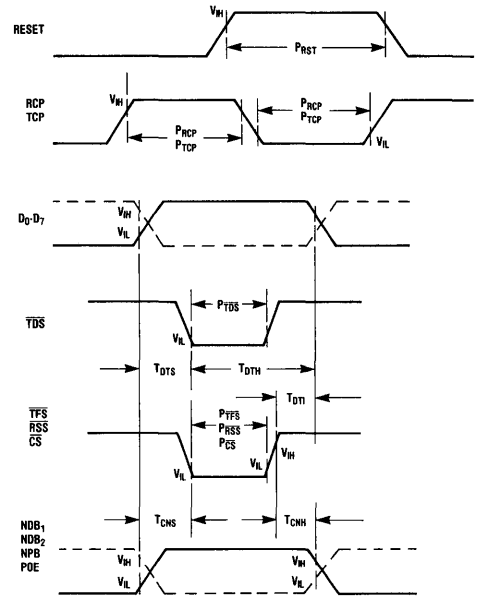


Figure 2. Timing Waveform

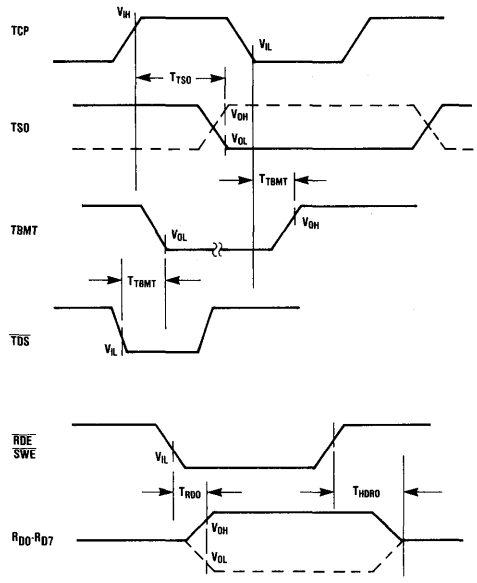
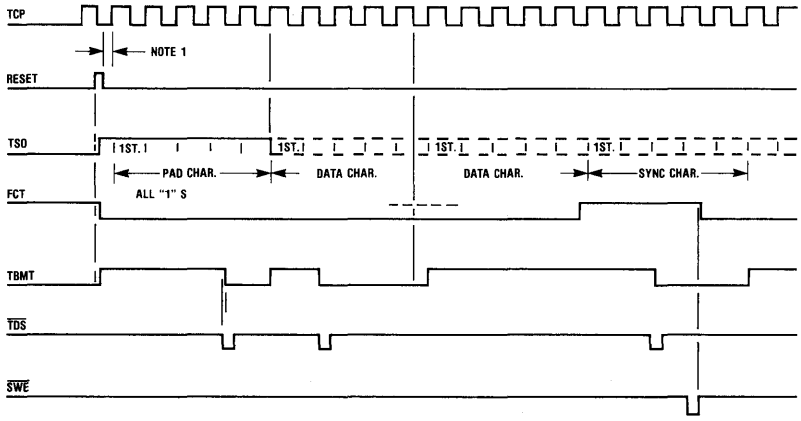


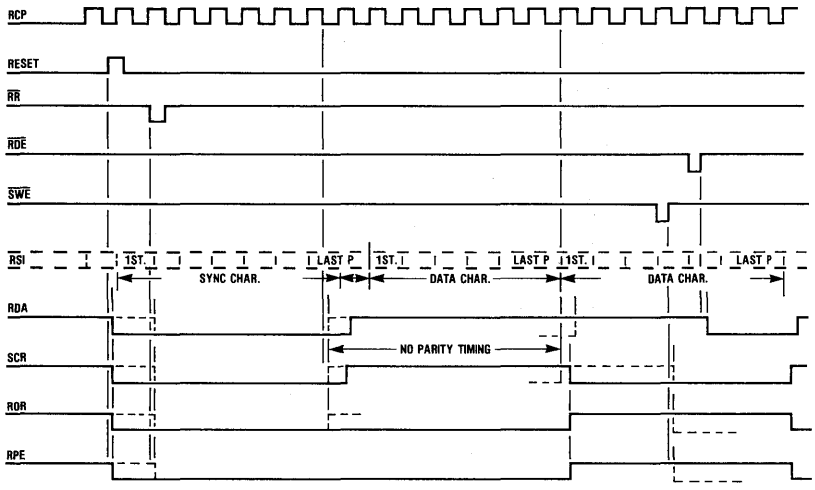
Figure 3. Transmitter Timing Diagram



NOTE 1 DATA TRANSMISSION WILL START ON THE FIRST LOW TO HIGH TRANSITION OF TCP AFTER RESET IS LOW. THE INITIAL RESET PULSE SHOULD NOT OCCUR UNTIL 100 MICROSECONDS AFTER POWER IS APPLIED.

S6800

Figure 4. Receiver Timing Diagram



Pin Definitions

Pin	Label	Function
(1)	GND	Ground
(2)	V_{CC}	+ 5 Volts ± 5%
(14)	RESET	MASTER RESET. A V_{IH} initializes both the receiver and transmitter. The Transmitter Shift Register is set to output a character of all logic 1's. FCT is reset to V_{OL} and TBMT set to V_{OH} indicating the Transmitter Holding Register is empty. The receiver status is initialized to a V_{OL} on RPE, SCR, and RDA. The sync character detect logic is inhibited until a RR pulse is received.
(15–22)	D0–D7	DATA INPUTS. Data on the eight data lines are loaded into the Transmitter Holding Register by $\overline{TDS}$, the Transmitter Fill Register by $\overline{TFS}$, and the Receiver Sync Register by $\overline{RSS}$. The character is right justified with the LSB at D0. For word lengths less than 8 bits, the unused inputs are ignored. Data transmission is LSB first.
(38)	$\overline{TDS}$	TRANSMIT DATA STROBE. A V_{IL} loads data on D0-D7 into the Transmitter Holding Register and resets TBMT to a V_{OL}.
(24)	$\overline{TFS}$	TRANSMIT FILL STROBE. A V_{IL} loads data on D0-D7 into the Transmitter Fill Register. The character in the Transmitter Fill Register is transmitted whenever a new character is not loaded in the allotted time.
(23)	$\overline{RSS}$	RECEIVER SYNC STROBE. A V_{IL} loads data on D0-D7 into the Receiver Sync Register. SCR is set to V_{OH} whenever data in the Receiver Shift Register compares with the character in the Receiver Sync Register.
(9)	TBMT	TRANSMIT BUFFER EMPTY. A V_{OH} indicates the data in the Transmitter Holding Register has been transferred to the Transmitter Shift Register and new data may be loaded. TBMT is reset to V_{OL} by a V_{IL} on $\overline{TDS}$. A V_{IH} on RESET sets TBMT to a V_{OH}. TBMT is also multiplexed onto the RD7 output (26) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(6)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on D0-D7 are transmitted serially, least significant bit first, on TSO at a rate equal to the Transmit Clock frequency, TCP. Source of the data to the transmitter shift register is the Transmitter Holding Register or Transmitter Fill Register.
(36)	TCP	TRANSMIT CLOCK. Data is transmitted on TSO at the frequency of the TCP input in a NRZ format. A new data bit is started on each negative to positive transition (V_{IL} to V_{IH}) of TCP.
(26–33)	RD7–RD0	RECEIVED DATA OUTPUTS RD0-RD7 contain data from the Receiver Output Register or selective status conditions depending on the state of $\overline{SWE}$ and $\overline{RDE}$ per the following table:

(34) $\overline{SWE}$	(35) $\overline{RDE}$	(33) RD0	(32) RD1	(31) RD2	(30) RD3	(39) RD4	(28) RD5	(27) RD6	(26) RD7
V_{IL}	V_{IL}	X	X	X	X	X	X	X	X
V_{IL}	V_{IH}	RDA	ROR	RPE	SCR	V_{OL}	V_{OL}	FCT	TBMT
V_{IH}	V_{IL}	DB0	BD1	DB2	DB3	DB4	DB5	DB6	DB7
V_{IH}	V_{IH}	X	X	X	X	X	X	X	X

X – Output is in the OFF or Tri-State condition
DB0 – LSB of Receiver Output Register
DB7 – MSB of Receiver Output Register
The two unused outputs are held at V_{OL} in the output status condition.

Pin Definitions (continued)

Pin	Label	Function
(35)	$\overline{RDE}$	RECEIVE DATA ENABLE. A V_{IL} enables the data in the Receiver Output Register onto the output data lines RD0–RD7. The trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$ resets RDA to the V_{OL} condition.
(7)	FCT	FILL CHARACTER TRANSMITTED. A V_{OH} on FCT indicates data from the Transmitter Fill Register has been transferred to the Transmitter Shift Register. FCT is reset to V_{OL} when data is transferred from the Transmitter Holding Register to the Transmitter Shift Register, or on the trailing edge (V_{IL} to V_{IH}) of the $\overline{SWE}$ pulse, or when RESET is V_{IH}. FCT is multiplexed onto the RD6 output (27) when $\overline{SWE}$ is at V_{IL} and $\overline{RDE}$ is at V_{IH}.
(25)	RSI	RECEIVER SERIAL INPUT. Serial data is clocked into the Receiver Shift Register, least significant bit first, on RSI at a rate equal to the Receive Clock frequency RCP.
(37)	RCP	RECEIVE CLOCK. Data is transferred from RSI input to the Receiver Shift Register at the frequency of the RCP input. Each data bit is entered on the positive to negative transition (V_{IH} to V_{IL}) of RCP.
(12)	RDA	RECEIVED DATA AVAILABLE. A V_{OH} indicates a character has been transferred from the Receiver Shift Register to the Receiver Output Register. RDA is reset to V_{OL} on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{RDE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RDA is multiplexed onto the RD0 output (33) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(8)	SCR	SYNC CHARACTER RECEIVED. A V_{OH} indicates the data in the Receiver Shift Register is identical to the data in the Receiver Sync Register. SCR is reset to a V_{OL} when the character in the Receiver Shift Register does not compare to the Receiver Sync Register, on the trailing edge (V_{IL} to V_{IH} transition) of $\overline{SWE}$, by a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. SCR is multiplexed onto the RD3 output (30) when $\overline{SWE}$ is a V_{IL} and $\overline{RDE}$ is V_{IH}.
(34)	$\overline{SWE}$	STATUS WORD ENABLE. A V_{IL} enables the internal status conditions onto the output data lines RD0–RD7. The trailing edge of $\overline{SWE}$ pulse resets FCT, ROR, RPE, and SCR to V_{OL}.
(11)	ROR	RECEIVER OVERRUN. A V_{OH} indicates data has been transferred from the Receiver Shift Register to the Receiver Output Register when RDA was still set to V_{OH}. The last data in the Output Register is lost. ROR is reset by the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$, a V_{IH} on RESET or a V_{OL} to V_{OH} transition of RDA. ROR is multiplexed onto the RD1 output (32) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.
(10)	RPE	RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character transferred to the Output Register does not agree with the parity selected by POE. RPE is reset with the next received character with correct parity, the trailing edge (V_{IL} to V_{IH}) of $\overline{SWE}$, a V_{IL} on $\overline{RR}$ or a V_{IH} on RESET. RPE is multiplexed onto the RD2 output (31) when $\overline{SWE}$ is V_{IL} and $\overline{RDE}$ is V_{IH}.

Pin Definitions (continued)

Pin	Label	Function
(13)	$\overline{RR}$	RECEIVER RESTART. A V_{IL} resets the receiver section by clearing the status RDA, SCR, ROR, and RPE to V_{OL}. The trailing edge of $\overline{RR}$ (V_{IL} to V_{IH}) also puts the receiver in a bit transparent mode to search for a comparison, each bit time, between the contents of the Receiver Shift Register and the Receiver Sync Register. The number of data bits per character for the comparison is set by NDB1 and NDB2. After a compare is made SCR is set to V_{OH}, the sync character is transferred to the Receiver Output Register, and the receiver enters a word synchronous mode framing an input character each word time. **NOTE:** Parity is not checked on the first sync character but is enabled for every succeeding character.
(39)	NDB1	NUMBER DATA BITS. The number of Data Bits per character are determined by NDB1 and NDB2. The number of data bits does not include the parity bit. NDB2 / NDB1 / CHARACTER LENGTH V_{IL} / V_{IL} / 5 Bits V_{IL} / V_{IH} / 6 Bits V_{IH} / V_{IL} / 7 Bits V_{IH} / V_{IH} / 8 Bits For character length less than 8 bits, unused inputs are ignored and unused outputs are held to V_{OL}. Data is always right justified with D0 and RD0 being the least significant bits.
(3)	NPB	NO PARITY BIT. A V_{IH} eliminates generation of a parity bit in the transmitter and checking of parity in the receiver. With parity disabled, the RPE status bit is held at V_{OL}.
(4)	POE	PARITY ODD/EVEN. A V_{IH} directs both the transmitter and receiver to operate with even parity. A V_{IL} forces parity operation. NPB must be V_{IL} for parity to be enabled.
(5)	$\overline{CS}$	CONTROL STROBE. A V_{IL} loads the control inputs NDB1, NDB2, POE, and NPB into the Control Register. For static operation, $\overline{CS}$ can be tied directly to ground.

AMERICAN MICROSYSTEMS, INC.

S6551/S68051

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER

Features

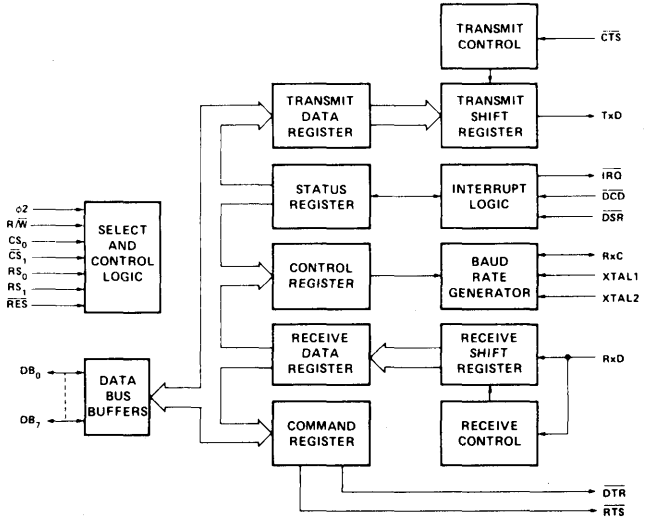
- ☐ On-Chip Baud Rate Generator: 15 Programmable Baud Rates Derived from a Standard 1.8432MHz External Crystal (50 to 19,200 Baud)
- ☐ Programmable Interrupt and Status Register to Simplify Software Design
- ☐ Single +5 Volt Power Supply
- ☐ Serial Echo Mode
- ☐ False Start Bit Detection
- ☐ 8-Bit Bi-Directional Data Bus for Direct Communication With the Microprocessor
- ☐ External 16× Clock Input for Non-Standard Baud Rates (Up to 125K Baud)
- ☐ Programmable: Word Lengths; Number of Stop Bits; and Parity Bit Generation and Detection
- ☐ Data Set and Modem Control Signals Provided
- ☐ Parity: (Odd, Even, None, Mark, Space)
- ☐ Full-Duplex or Half-Duplex Operation
- ☐ 5, 6, 7, 8 and 9-Bit Transmission

General Description

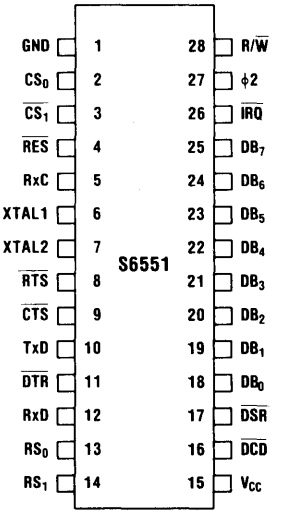
The S6551/S68051 is an Asynchronous Communication Adapter (ACIA) intended to provide for interfacing the 6500/6800 microprocessor families to serial communication data sets and modems. A unique feature is the inclusion of an on-chip programmable baud rate generator, with a crystal being the only external component required.

S6800

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3V to +7.0V
Input/Output Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

All inputs contain protection circuitry to prevent damage to high static charges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Operating Characteristics (V_{CC} = 5.0V ± 5, T_A = 0C to +70°C, unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0	—	V_{CC}	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
I_{IN}	Input Leakage Current: V_{IN} = 0 to 5V (φ2, R/$\overline{W}$, $\overline{RES}$, CS_0, $\overline{CS_1}$, RS_0, RS_1, $\overline{CTS}$, R×D, $\overline{DCD}$, $\overline{DSR}$)	—	±1.0	±2.5	μA
I_{TSI}	Input Leakage Current for High Impedance State (Three State)	—	±2.0	±10.0	μA
V_{OH}	Output High Voltage: I_{LOAD} = −100μA (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$)	2.4	—	—	V
V_{OL}	Output Low Voltage: I_{LOAD} = 1.6mA (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	—	—	0.4	V
I_{OH}	Output High Current (Sourcing): V_{OH} = 2.4V (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$)	−100	—	—	μA
I_{OL}	Output Low Current (Sinking): V_{OL} = 2.4V (DB_0-DB_7, T×D, R×C, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$)	1.6	—	—	mA
I_{OFF}	Output Leakage Current (Off State): V_{OUT} = 5V ($\overline{IRQ}$)	—	1.0	10.0	μA
C_{CLK}	Clock Capacitance (φ2)	—	—	20	pF
C_{IN}	Input Capacitance (Except XTAL1 and XTAL2)	—	—	10	pF
C_{OUT}	Output Capacitance	—	—	10	pF
P_D	Power Dissipation (See Graph) (T_A = 0°C)	—	170	300	mW

Write Cycle ($V_{CC}=5.0V\pm5$, $T_A=0C$ to $+70°C$, unless otherwise noted)

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	ϕ2 Pulse Width	400	—	200	—	ns
t_{ACW}	Address Set-Up Time	120	—	70	—	ns
t_{CAH}	Address Hold Time	0	—	0	—	ns
t_{WCW}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CWH}	R/$\overline{W}$ Hold Time	0	—	0	—	ns
t_{DCW}	Data Bus Set-Up Time	150	—	60	—	ns
t_{HW}	Data Bus Hold Time	20	—	20	—	ns

(t_r and t_f=10 to 30ns)

Figure 1. Power Dissipation vs Temperature

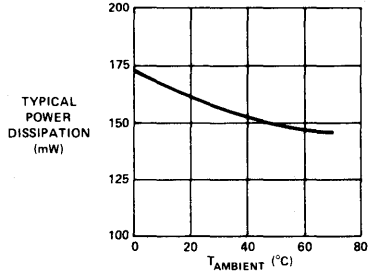
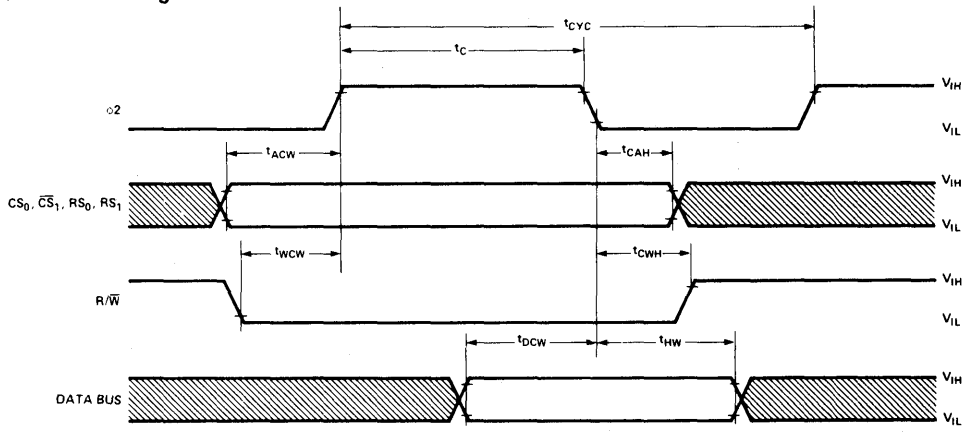


Figure 2. Write Timing Characteristics



S6800

Read Cycle (V_{CC} = 5.0V ± 5, T_A = 0C to +70°C, unless otherwise noted)

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Cycle Time	1.0	—	0.5	—	μs
t_C	ϕ2 Pulse Width	400	—	200	—	ns
t_{ACR}	Address Set-Up Time	120	—	70	—	ns
t_{CAR}	Address Hold Time	0	—	0	—	ns
t_{WCR}	R/$\overline{W}$ Set-Up Time	120	—	70	—	ns
t_{CDR}	Read Access Time (Valid Data)	—	200	—	150	ns
t_{HR}	Read Hold Time	20	—	20	—	ns
t_{CDA}	Bus Active Time (Invalid Data)	40	—	40	—	ns

Figure 3. Clock Generation

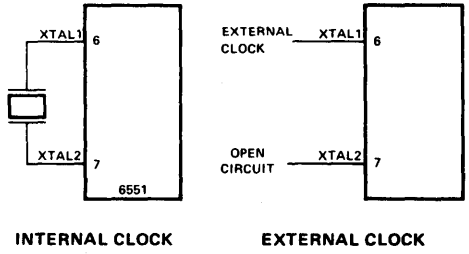


Figure 4. Read Timing Characteristics

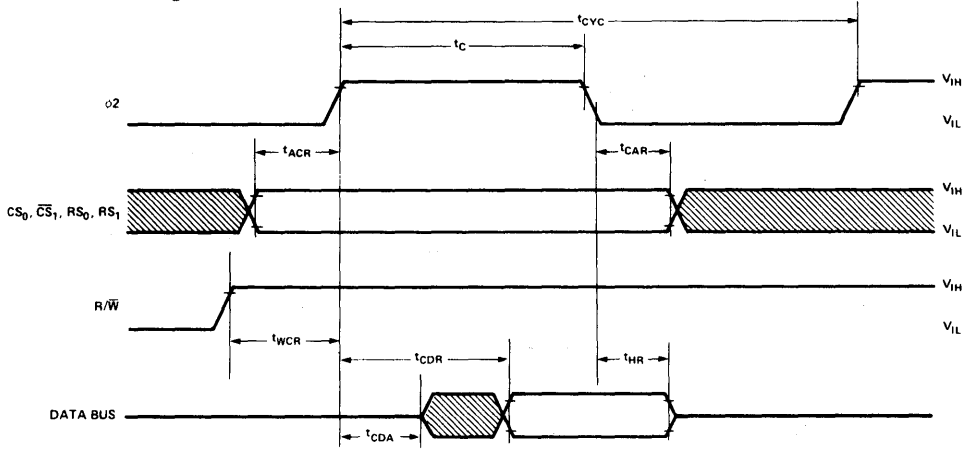


Figure 5. Test Load for Data Bus (DB_0-DB_7), $\overline{TxD}$, $\overline{DTR}$, RTS Outputs

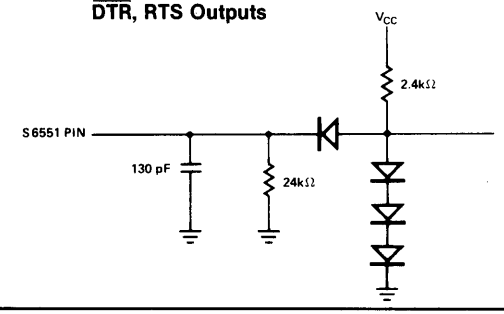


Figure 6a. Interrupt and Output Timing

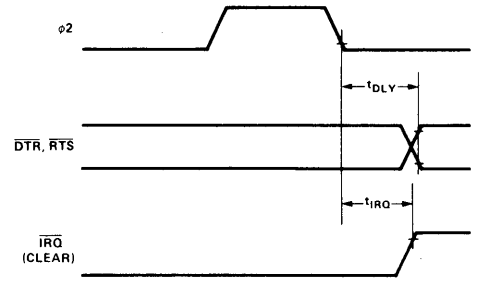


Figure 6b. Transmit Timing with External Clock

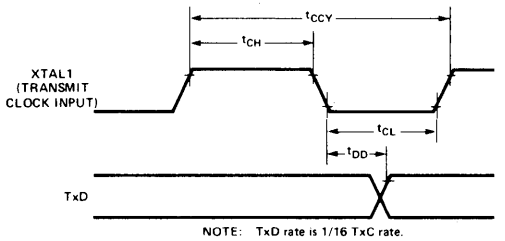
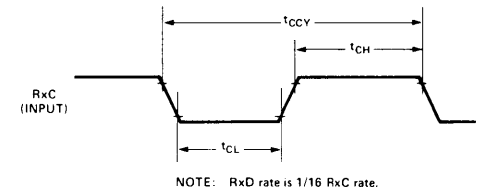


Figure 6c. Receive External Clock Timing



S6800

Transmit/Receive Characteristics

Symbol	Parameter	S6551		S6551A		Unit
		Min.	Max.	Min.	Max.	
t_{CCY}	Transmit/Receive Clock Rate	400*	—	400*	—	ns
t_{CH}	Transmit/Receive Clock High Time	175	—	175	—	ns
t_{CL}	Transmit/Receive Low Time	175	—	175	—	ns
t_{DD}	EXTAL1 to TxD Propagation Delay	—	500	—	500	ns
t_{DLY}	Propagation Delay ($\overline{RTS}$, DTR)	—	500	—	500	ns
t_{IRQ}	$\overline{IRQ}$ Propagation Delay (Clear)	—	500	—	500	ns

(t_r and t_f=10 to 30ns)

*The baud rate with external clocking is: Baud Rate = $\frac{1}{16 \times T_{CCY}}$

Pin Description

$\overline{RES}$ (Reset). During system initialization a low on the RES input will cause internal registers to be cleared.

φ2 Input Clock. The input clock is the system φ2 clock and is used to trigger all data transfers between the system microprocessor and the S6551.

R/$\overline{W}$ (Read/Write). The R/$\overline{W}$ is generated by the microprocessor and is used to control the direction of data transfers. A high on the R/$\overline{W}$ pin allows the processor to read the data supplied by the S6551. A low on the R/$\overline{W}$ pin allows a write to the S6551.

$\overline{IRQ}$ (Interrupt Request). The $\overline{IRQ}$ pin is an interrupt signal from the interrupt control logic. It is an open drain output, permitting several devices to be connected to the common $\overline{IRQ}$ microprocessor input. Normally a high level, $\overline{IRQ}$ goes low when an interrupt occurs.

DB_0-DB_7 (Data Bus). The DB_0-DB_7 pins are the eight data lines used for transfer of data between the processor and the S6551. These lines are bi-directional and are normally high-impedance except during Read cycles when selected.

CS_0-$\overline{CS_1}$ (Chip Selects). The two chip select inputs are normally connected to the processor address lines either directly or through decoders. The S6551 is selected when CS_0 is high and $\overline{CS_1}$ is low.

RS_0, RS_1 (Register Selects). The two register select lines are normally connected to the processor address lines to allow the processor to select the various S6551 internal registers. The following table indicates the internal register select coding:

Table 1

RS_1	RS_0	WRITE	READ
0	0	Transmit Data Register	Receiver Data Register
0	1	Programmed Reset (Data is "Don't Care")	Status Register
1	0	Command Register	
1	1	Control Register	

The table shows that only the Command and Control registers are read/write. The Programmed Reset operation does not cause any data transfer, but is used to clear the S6551 registers. The Programmed Reset is slightly different from the Hardware Reset ($\overline{RES}$) and these differences are described in the individual register definitions.

XTAL1, XTAL2 (Crystal Pins). These pins are normally directly connected to the external crystal (1.8432MHz) used to derive the various baud rates. Alternatively, an externally generated clock may be used to drive the XTAL1 pin, in which case the XTAL2 pin must float. The choice of crystal is not critical, but NYMPH PO18 (series resonant) is recommended.

T×D (Transmit Data). The T×D output line is used to transfer serial NRZ (non-return-to-zero) data to the modem. The LSB (least significant bit) of the Transmit Data Register is the first data bit transmitted and the rate of data transmission is determined by the baud rate selected.

R×D (Receive Data). The R×D input line is used to transfer serial NRZ data into the ACIA from the modem, LSB first. The receiver data rate is either the programmed baud rate or the rate of an externally generated receiver clock. This selection is made by programming the Control Register.

R×C (Receive Clock). The R×C is a bi-directional pin which serves as either the receiver 16×clock input or the receiver 16×clock output. The latter mode results if the internal baud rate generator is selected for receiver data clocking.

$\overline{RTS}$ (Request to Send). The $\overline{RTS}$ output pin is used to control the modem from the processor. The state of the $\overline{RTS}$ pin is determined by the contents of the Command Register.

$\overline{CTS}$ (Clear to Send). The $\overline{CTS}$ input pin is used to control the transmitter operation. The enable state is with $\overline{CTS}$ low. The transmitter is automatically disabled if $\overline{CTS}$ is high.

$\overline{DTR}$ (Data Terminal Ready). This output pin is used to to indicate the status of the S6551 to the modem. A low on $\overline{DTR}$ indicates the S6551 is enabled and a high indicates it is disabled. The processor controls this pin via bit 0 of the Command Register.

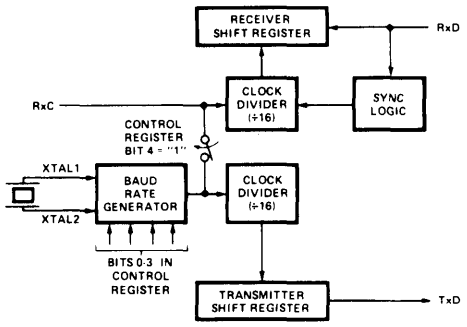
$\overline{DSR}$ (Data Set Ready). The $\overline{DSR}$ input pin is used to indicate to the S6551 the status of the modem. A low indicates the "ready" state and a high, "not-ready." $\overline{DSR}$ is a high-impedance input and must not be a no-connect. If unused, it should be driven high or low, but not switched.

$\overline{DCD}$ (Data Carrier Detect). The $\overline{DCD}$ input pin is used to indicate to the S6551 the status of the carrier-detect output of the modem. A low indicates that the modem carrier signal is present and a high, that it is not. $\overline{DCD}$, like $\overline{DSR}$, is a high-impedance input and must not be a no-connect.

Internal Organization

The Transmitter/Receiver sections of the S6551 are depicted by the block diagram in Figure 7.

Figure 7. Transmitter/Receiver Clock Circuits



Bits 0-3 of the Control Register select the divisor used to generate the baud rate for the Transmitter. If the Receiver clock is to use the same baud rate as the Transmitter, then R×C becomes an output pin and can be used to slave other circuits to the S6551.

Control Register

The Control Register is used to select the desired mode for the S6551. The word length, number of stop bits, and clock controls are all determined by the Control Register, which is depicted in Figure 8.

Command Register

The Command Register is used to control Specific Transmit/Receive functions and is shown in Figure 9.

Figure 8. Control Register Format

CONTROL REGISTER

7	6	5	4	3	2	1	0

STOP BITS

0 = 1 Stop Bit
1 = 2 Stop Bits
1 Stop Bit if Word Length = 8 Bits and Parity*
1½ Stop Bits if Word Length = 5 Bits and No Parity.

WORD LENGTH

BIT 6	BIT 5	DATA WORD LENGTH
0	0	8
0	1	7
1	0	6
1	1	5

RECEIVER CLOCK SOURCE

0 = External Receiver Clock
1 = Baud Rate Generator

*This allows for 9-bit transmission (8 data bits plus parity).

BAUD RATE GENERATOR

3	2	1	0	
0	0	0	0	16x EXTERNAL CLOCK
0	0	0	1	50 BAUD
0	0	1	0	75
0	0	1	1	109.92
0	1	0	0	134.58
0	1	0	1	150
0	1	1	0	300
0	1	1	1	600
1	0	0	0	1200
1	0	0	1	1800
1	0	1	0	2400
1	0	1	1	3600
1	1	0	0	4800
1	1	0	1	7200
1	1	1	0	9600
1	1	1	1	19,200

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	–	–	–	–	–

Figure 9. Command Register Format

COMMAND REGISTER

7	6	5	4	3	2	1	0

PARITY CHECK CONTROLS

BIT 7	BIT 6	BIT 5	OPERATION
–	–	0	Parity Disabled - No Parity Bit Generated - No Parity Bit Received
0	0	1	Odd Parity Receiver and Transmitter
0	1	1	Even Parity Receiver and Transmitter
1	0	1	Mark Parity Bit Transmitted, Parity Check Disabled
1	1	1	Space Parity Bit Transmitted, Parity Check Disabled

NORMAL/ECHO MODE FOR RECEIVER

0 = Normal
1 = Echo (Bits 2 and 3 must be "0")

DATA TERMINAL READY

0 = Disable Receiver and All Interrupts ($\overline{DTR}$ high)
1 = Enable Receiver and All Interrupts ($\overline{DTR}$ low)

RECEIVER INTERRUPT ENABLE

0 = $\overline{IRQ}$ Interrupt Enabled from Bit 3 of Status Register
1 = $\overline{IRQ}$ Interrupt Disabled

TRANSMITTER CONTROLS

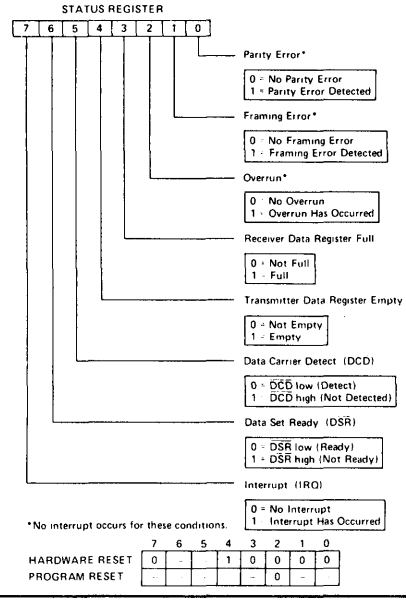
BIT 3	BIT 2	TRANSMIT INTERRUPT	$\overline{RTS}$ LEVEL	TRANSMITTER
0	0	Disabled	High	Off
0	1	Enabled	Low	On
;	0	Disabled	Low	On
1	1	Disabled	Low	Transmit BRK

	7	6	5	4	3	2	1	0
HARDWARE RESET	0	0	0	0	0	0	0	0
PROGRAM RESET	–	–	–	0	0	0	0	0

Status Register

The Status Register is used to indicate to the processor the status of various S6551 functions and is outlined in Figure 10.

Figure 10. Status Register Format



Transmit and Receive Data Registers

These registers are used as temporary data storage for the S6551 Transmit and Receive circuits. The Transmit Data Register is characterized as follows:

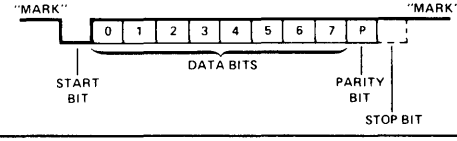
- ☐ Bit 0 is the leading bit to be transmitted.
- ☐ Unused data bits ae the high-order bits and are "don't care" for transmission.

The Receive Data Register is characterized in a similar fashion:

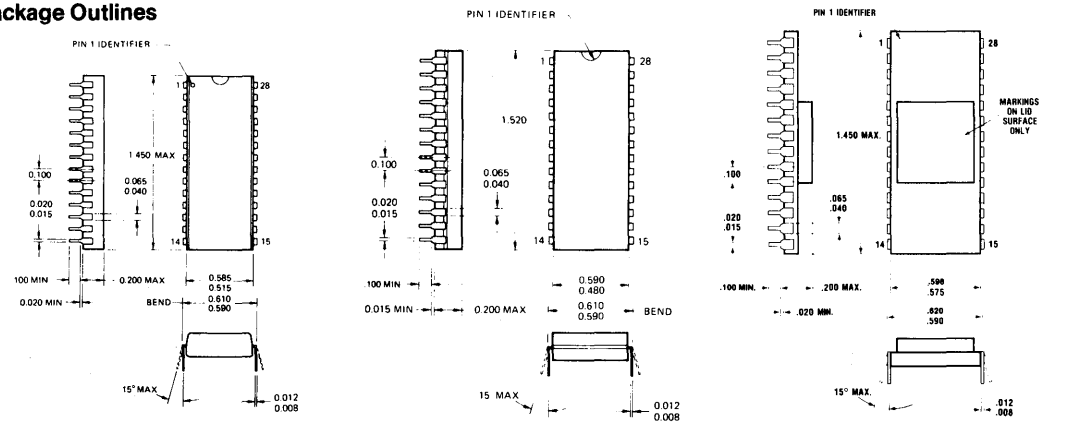
- ☐ Bit 0 is the leading bit received.
- ☐ Unused data bits are the high-order bits and are "0" for the receiver.
- ☐ Parity bits are not contained in the Receive Data Register, but are stripped-off after being used for external parity checking. Parity and all unused high-order bits are "0".

Figure 11 illustrates a single transmitted or received data word, for the example of 8 data bits, parity, and 1 stop bit.

Figure 11. Serial Data Stream Example



Package Outlines



28-Lead Plastic **28-Lead Cerdip** **28-Lead Ceramic**

AMERICAN MICROSYSTEMS, INC.

S6810/S68A10/S68B10

128 X 8 STATIC READ/WRITE MEMORY

Features

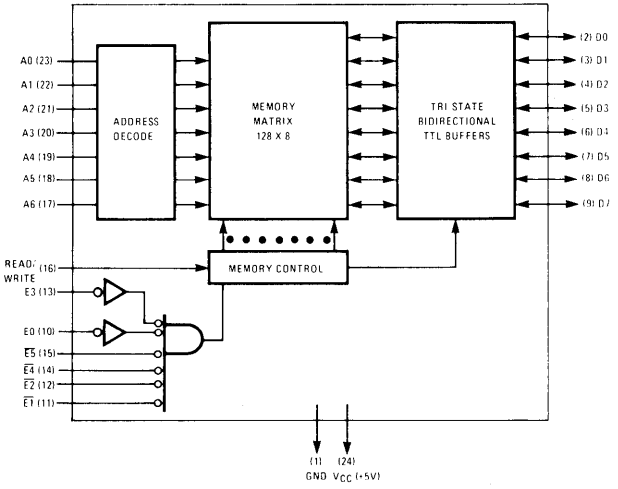
- ☐ **Organized as 128 Bytes of 8 Bits**
- ☐ **Static Operation**
- ☐ **Bidirectional Three-State Data Input/Output**
- ☐ **Six Chip Enable Inputs (Four Active Low, Two Active High**
- ☐ **Single 5 Volt Power Supply**
- ☐ **TTL Compatible**
- ☐ **Maximum Access Time**
  450ns for S6810
  360ns for S68A10
  250ns for S68B10

General Description

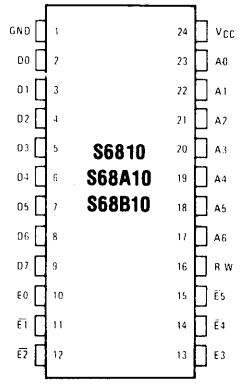
The S6810/S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S6800/S68A00 and S68B00 Microprocessors. Interfacing to the S6810/S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S6810/S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S6810/S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

Block Diagram



Pin Configuration



S6800

Absolute Maximum Ratings

Supply Voltage	−0.3V to +7.0V
Input Voltage	−0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

D.C. Characteristics:

(V_{CC} = +5.0V ± 5%, V_{SS} = 0, T_A=0°C to 70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{IN}	Input Current (A_n, R/W, CS_n, $\overline{CS_n}$)			2.5	μAdc	V_{IN} = 0V to 5.25V
V_{OH}	Output High Voltage	2.4			Vdc	I_{OH} = −205μA
V_{OL}	Output Low Voltage			0.4	Vdc	I_{OL} = 1.0mA
I_{LO}	Output Leakage Current (Three State)			10	μAdc	CS = 0.8V or $\overline{CS}$ = 2.0V, V_{OUT} = 0.4V to 2.4V
I_{CC}	Supply Current S6810 S68A10/S68B10			80 100	mAdc mAdc	V_{CC} = 5.25V, all other pins grounded, T_A = 0°C

A.C. Characteristics:

Read Cycle

(V_{CC} = +5.0V ± 5%, V_{SS} = 0,T_A=0°C to 70°C unless otherwise noted.)

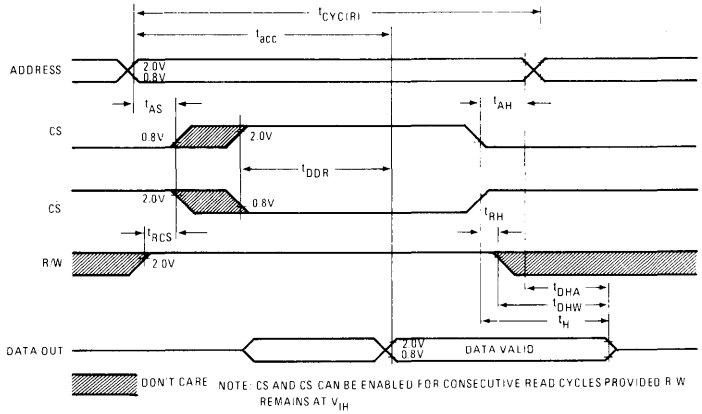
		S6810		S68A10		S68B10		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Units
$t_{cyc(R)}$	Read Cycle Time	450		360		250		ns
t_{acc}	Access Time		450		360		250	ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{DDR}	Data Delay Time (Read)		230		220		180	ns
t_{RCS}	Read to Select Delay Time	0		0		0		ns
t_{DHA}	Data Hold from Address	10		10		10		ns
t_H	Output Hold Time	10		10		10		ns
t_{DHW}	Data Hold from Write	10	80	10	60	10	60	ns
t_{RH}	Read Hold from Chip Select	0		0		0		ns

Write Cycle

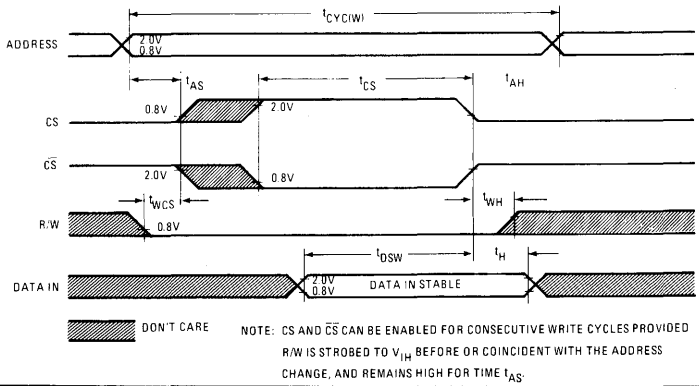
(V_{CC} = +5.0V ± 5%, V_{SS} = 0, T_A=0°C to 70°C unless otherwise noted.)

Symbol	Parameter	S6810		S68A10		S68B10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(W)}$	Write Cycle Time	450		360		250		ns
t_{AS}	Address Setup Time	20		20		20		ns
t_{AH}	Address Hold Time	0		0		0		ns
t_{CS}	Chip Select Pulse Width	300		250		210		ns
t_{WCS}	Write to Chip Select Delay Time	0		0		0		ns
t_{DSW}	Data Setup Time (Write)	190		80		60		ns
t_H	Input Hold Time	10		10		10		ns
t_{WH}	Write Hold Time from Chip Select	0		0		0		ns

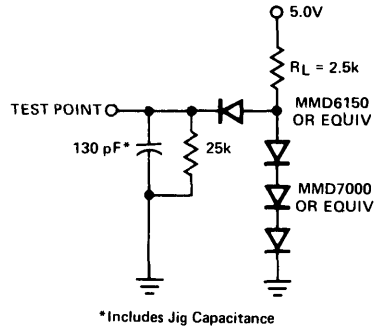
Read Cycle Timing



Write Cycle Timing



AC Test Load



*Includes Jig Capacitance

AMERICAN MICROSYSTEMS, INC.

S6821/S68A21/S68B21

PERIPHERAL INTERFACE ADAPTER (PIA)

Features

- ☐ 8-Bit Bidirectional Bus for Communication with the MPU
- ☐ Two Bidirectional 8-Bit Buses for Interface to Peripherals
- ☐ Two Programmable Control Registers
- ☐ Two Programmable Data Direction Registers
- ☐ Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- ☐ Handshake Control Logic for Input and Output Peripheral Operation
- ☐ High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- ☐ Program Controlled Interrupt and Interrupt Disable Capability
- ☐ CMOS Compatible Peripheral Lines
- ☐ Two TTL Drive Capability on all A and B Side Buffers
- ☐ TTL Compatible
- ☐ Static Operation

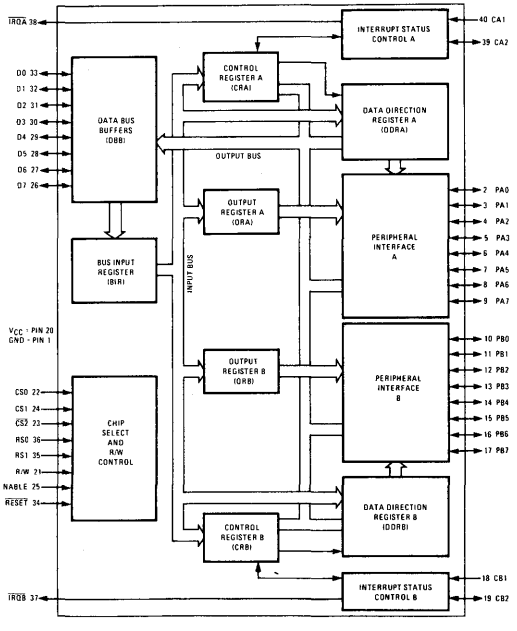
General Description

The S6821/S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S6800/S68A00/S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

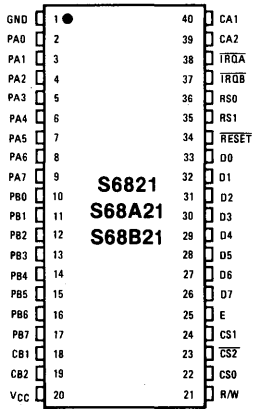
The functional configuration of the PIA is programmed by the MPU during system initialization Each of the peripheral data lines can be programmed to act as an

S6800

Block Diagram



Pin Configuration



General Description (Continued)

input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S6800/S68A00/S68B00 MPUs with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with S6800/S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

Absolute Maximum Ratings:

Symbol	Rating	Value	Unit
V_{CC}	Supply Voltage	−0.3 to +7.0	Vdc
V_{IN}	Input Voltage	−0.3 to +7.0	Vdc
T_A	Operating Temperature Range	0° to +70°	°C
T_{stg}	Storage Temperature Range	−55° to +150°	°C
θ_{ja}	Thermal Resistance	82.5	°C/W

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
Bus Control Inputs (R/$\overline{W}$, Enable, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$)						
V_{IH}	Input High Voltage	V_{SS}+2.0	–	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS}−0.3	–	V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current	–	1.0	2.5	μAdc	V_{IN}=0 to 5.25 Vdc
C_{IN}	Capacitance	–	–	7.5	pF	V_{IN}=0, T_A=25°C, f=1.0MHz
Interrupt Outputs ($\overline{IRQA}$, $\overline{IRQB}$)						
V_{OL}	Output Low Voltage	–	–	V_{SS}+0.4	Vdc	I_{LOAD}=3.2 mAdc
I_{LOH}	Output Leakage Current (Off State)	–	1.0	10	μAdc	V_{OH}=2.4 Vdc
C_{OUT}	Capacitance	–	–	5.0	pF	V_{IN}=0, T_A=25°C, f=1.0MHz
Data Bus (D0-D7)						
V_{IH}	Input High Voltage	V_{SS}+2.0	–	V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS}−0.3	–	V_{SS}+0.8	Vdc	
I_{TSI}	Three State (Off State) Input Current	–	2.0	10	μAdc	V_{IN}=0.4 to 2.4 Vdc
V_{OH}	Output High Voltage	V_{SS}+2.4	–	–	Vdc	I_{LOAD}=−205μAdc
V_{OL}	Output Low Voltage	–	–	V_{SS}+0.4	Vdc	I_{LOAD}=1.6mAdc
C_{IN}	Capacitance	–	–	12.5	pF	V_{IN}=0, T_A=25°C f=1.0MHz

Electrical Characteristics (Continued)

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Conditions
Peripheral Bus (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)						
I_{IN}	Input Leakage Current — R/$\overline{W}$, $\overline{Reset}$, RS0, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable		1.0	2.5	μAdc	V_{IN}=0 to 5.25 Vdc
I_{TSI}	Three-State (Off State) Input Current — PB0-PB7, CB2		2.0	10	μAdc	V_{IN}=0.4 to 2.4 Vdc
I_{IH}	Input High Current — PA0-PA7, CA2	−200	−400		μAdc	V_{IH}=2.4 Vdc
I_{OH}	Darlington Drive Current — PB0-PB7, CB2	−1.0		−10	mAdc	V_O=1.5 Vdc
I_{IL}	Input Low Current — PA0-PA7, CA2		−1.3	−2.4	mAdc	V_{IL}=0.4Vdc
V_{OH}	Output High Voltage — PA0-P7, PB0-PB7, CA2, CB2 PA0-PA7, CA2	V_{SS}+2.4 V_{CC}−1.0			Vdc	I_{LOAD}=−200μAdc I_{LOAD}=−10μAdc
V_{OL}	Output Low Voltage			V_{SS}+0.4	Vdc	I_{LOAD}=3.2mAdc
C_{IN}	Capacitance			10	pF	V_{IN}=0, T_A=25°C, f=1.0MHz
Power Requirements						
P_D	Power Dissipation			550	mW	

A.C. (Dynamic) Characteristics Loading=30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
=130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$
(V_{CC}=+5.0V±5%, T_A=0°C to +70°C unless otherwise noted)

Peripheral Timing Characteristics: V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.

Symbol	Parameter	S6821 Min.	S6821 Max.	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{PDSU}	Peripheral Data Setup Time	200		135		100		ns
t_{PDH}	Peripheral Data Hold Time	0		0		0		ns
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		1.0		0.670		0.5	μs
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		1.0		0.670		0.50	μs
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals		1.0		1.0		1.0	μs
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		2.0		1.35		1.0	μs
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	μs
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA0-PA7, CA2		2.0		1.35		1.0	μs

Peripheral Timing Characteristics (Continued)

Symbol	Parameter	S6821 Min.	S6821 Max.	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		1.0		0.670		0.5	μs
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	2.0		20		20		ns
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		1.0		0.670		0.5	μs
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		550		550		ns
t_r, t_f	Rise and Fall Times for CB1 and CB2 Input Signals		1.0		1.0		1.0	μs
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time, IRQA and IRQB		1.60		1.1		0.85	μs
t_{RS3}	Interrupt Response Time		1.0		1.0		1.0	μs
PW_I	Interrupt Input Pulse Width	500		500		500		ns
t_{RL}	Reset Low Time*	1.0		0.66		0.5		μs

*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

Figure 1. Enable Signal Characteristics

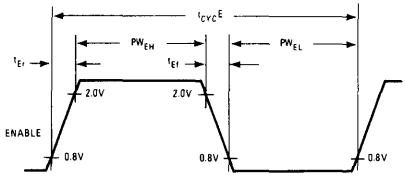


Figure 2. Bus Read Timing Characteristics (Read Information from PIA)

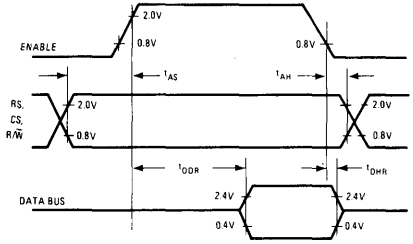


Figure 3. Bus Write Timing Characteristics (Write Information into PIA)

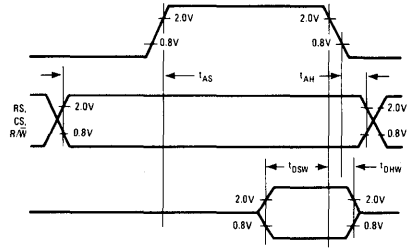
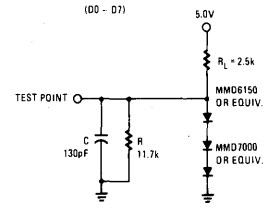


Figure 4. Bus Timing Test Loads



Bus Timing Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.

Symbol	Parameter	S6821		S68A21		S68B21		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er},t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Figure 5. TTL Equiv. Test Load

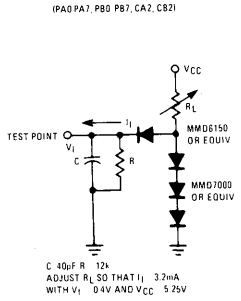


Figure 6. CMOS Equiv. Test Load

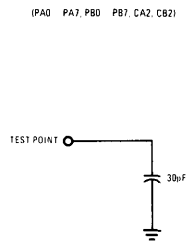


Figure 7. NMOS Equiv. Test Load

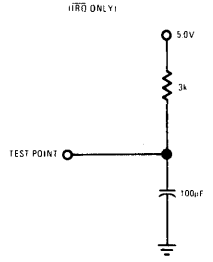


Figure 8. Peripheral Data Setup and Hold Times (Read Mode)

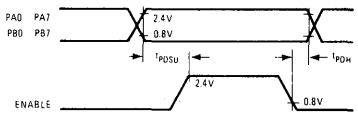
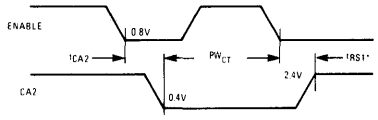


Figure 9. CA2 Delay Time (Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

Figure 10. CA2 Delay Time (Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

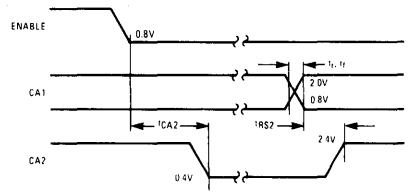


Figure 11. Peripheral CMOS Data Delay Times (Write Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)

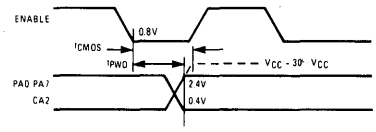
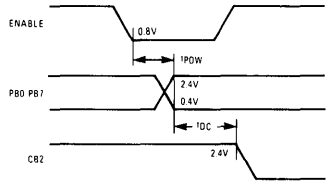


Figure 12. Peripheral Data and CB2 Delay Times (Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



CB2 Note:
CB2 goes low as a result of the positive transition of Enable.

Figure 13. CB2 Delay Time (Write Mode; CRB-5 = CRB-3 = 1. CRB-4 = 0)

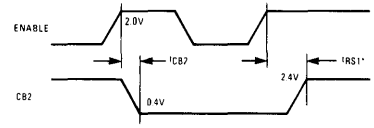
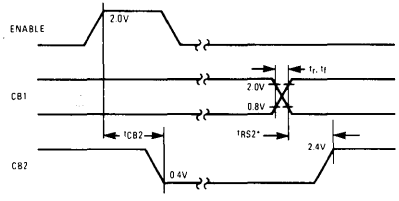
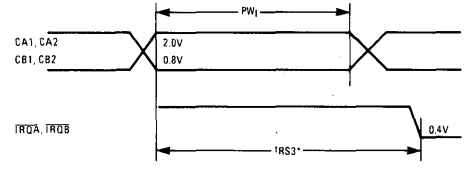


Figure 14. CB2 Delay Time (Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



*Assumes part was deselected during any previous E pulse.

Figure 15. Interrupt Pulse Width and $\overline{IRQ}$ Response



*Assumes Interrupt Enable Bits are set.

Figure 16. $\overline{IRQ}$ Release Time

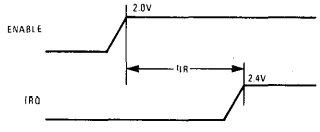
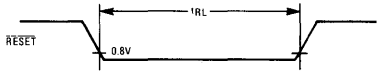
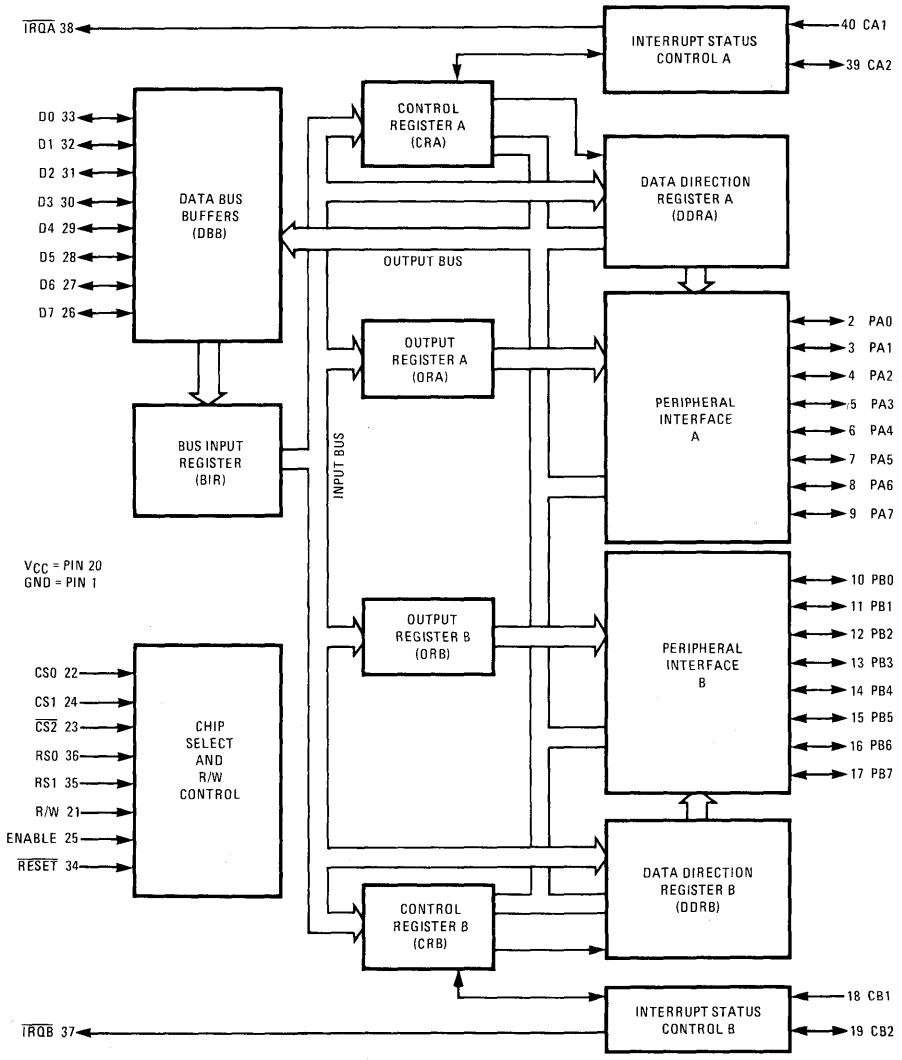


Figure 17. $\overline{Reset}$ Low Time.



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0μs before addressing the PIA.

Expanded Block Diagram



Interface Description

MPU/PIA Interface

Pin	Label	Function
(33) (32) (31) (30) (29) (28) (27) (26)	D0 D1 D2 D3 D4 D5 D6 D7	**Bidirectional Data** — The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The Read/Write line is in the Read (high) state when the PIA is selected for a Read operation.
(25)	E	**Enable** — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse. This signal will normally be a derivative of the S6800 $\phi 2$ Clock. The E pulse is used to condition the interrupt/control lines CA1, CA2, CB1 and CB2. At least one E pulse must occur from the inactive edge to the active edge of the input signal to set the interrupt flag, when the lines are used as inputs.
(21)	R/W	**Read/Write** — This signal is generated by the MPU to control the direction of data transfers on the Data Bus. A low state on the PIA Read/Write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the Read/Write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.
(34)	$\overline{\text{RESET}}$	$\overline{\text{Reset}}$ — The active low $\overline{\text{Reset}}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.
(22) (24) (23)	CS0 CS1 $\overline{\text{CS2}}$	**Chip Select** — These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{\text{CS2}}$ must be low for selection of the device. Data transfers are then performed under the control of the Enable and Read/Write signals. The chip select lines must be stable for the duration of the E pulse.
(36) (35)	RS0 RS1	**PIA Register Select** — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read. The Register select lines should be stable for the duration of the E pulse while in the read or write cycle.

(38)	$\overline{IRQA}$	**Interrupt Request** — The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open source" (no load device on the chip) and are capable of sinking a current of 1.6mA from an external source. This permits all interrupt request lines to be tied together in a wire-OR configuration.
(37)	$\overline{IRQB}$	

Each Interrupt Request line has two internal interrupt flag bits that will cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU is accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The Interrupt Flag is cleared (zeroed) as a result of an MPU Read Peripheral Data Operation.

PIA/Peripheral Interface

Pin	Label	Function
(2)	PA0	**Section A Peripheral Data** — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode the internal pullup resistor on these lines represents a maximum of one standard TTL load.
(3)	PA1	
(4)	PA2	
(5)	PA3	
(6)	PA4	
(7)	PA5	
(8)	PA6	
(9)	PA7	

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volts for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

(10)	PB0	**Section B Peripheral Data** — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. However, the output buffers driving these lines differ from those driving lines PA0-PA7. They have three-state capability, allowing them to enter a high impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high." As outputs, these lines are compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.
(11)	PB1	
(12)	PB2	
(13)	PB3	
(14)	PB4	
(15)	PB5	
(16)	PB6	
(17)	PB7	

(40) (18)	CA1 CB1	**Interrupt Input** — Peripheral Input lines CA1 and CB1 are input-only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.
(39)	CA2	**Peripheral Control** — The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents one standard TTL load. The function of this signal line is programmed with Control Register A.
(19)	CB2	**Peripheral Control** — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output, it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.
(1)	GND	**Ground**
(20)	V_{CC}	+5Volts ±5%

AMERICAN MICROSYSTEMS, INC.

S6840/S68A40/S68B40

PROGRAMMABLE TIMER

Features

- ☐ Operates from a Single 5 Volt Supply
- ☐ Fully TTL Compatible
- ☐ Single System Clock Required (Enable)
- ☐ Selectable Prescaler on Time 3 Capable of 4MHz for the S6840, 6MHz for the S68A40 and 8MHz for the S68B40
- ☐ Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- ☐ Readable Down Counter Indicates Counts to Go to Time-Out
- ☐ Selectable Gating for Frequency or Pulse-Width Comparison
- ☐ $\overline{RESET}$ Input
- ☐ Three Asynchronous External Clock and Gate/ Trigger Inputs Internally Synchronized
- ☐ Three Maskable Outputs

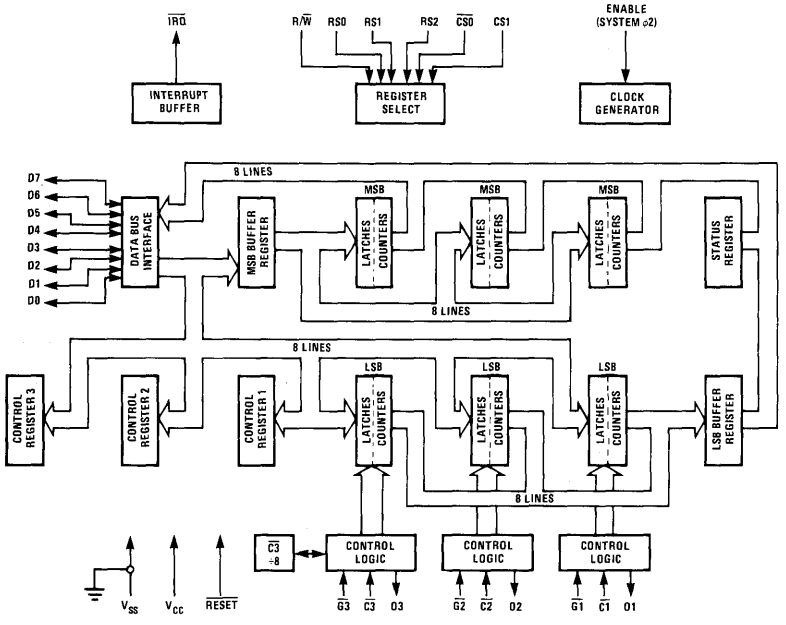
General Description

The S6840 is a programmable subsystem component of the S6800 family designed to provide variable system time intervals.

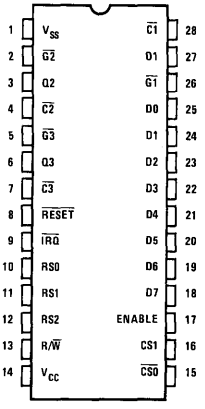
The S6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The S6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

S6800

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3 to +7.0V
Input Voltage V_{IN}	−0.3 to +7.0V
Operating Temperature Range T_A	0° to +70°C
Storage Temperature Range T_{stg}	−55° to +150°C
Thermal Resistance θ_{JA}	82.5°C/W

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics

V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	V_{SS}−0.3		V_{SS}+0.8	V	
I_{IN}	Input Leakage Current		1.0	2.5	μA	V_{IN}=0 to 5.25 V
I_{TSI}	Three State (Off State) Input Current D0-D7		2.0	10	μA	V_{IN}=0.4 to 2.4 V
V_{OH}	Output High Voltage D0-D7 Other Outputs	 V_{SS}+2.4 V_{SS}+2.4			 V V	 I_{LOAD}=−205μA I_{LOAD}=−200μA
V_{OL}	Output Low Voltage D0-D7 01—03, $\overline{IRQ}$			 V_{SS}+0.4 V_{SS}+0.4	 V V	 I_{LOAD}=1.6mA I_{LOAD}=3.2mA
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μA	V_{OH}=2.4V
P_D	Power Dissipation			550	mW	
C_{IN}	Capacitance D0-D7 All Others			 12.5 7.5	 pF	 V_{IN}=0, T_A=+25°C, f=1.0MHz
C_{OUT}	$\overline{IRQ}$ 01, 02, 03			 5.0 10	 pF	 V_{IN}=0, T_A=+25°C, f=1.0MHz

Bus Timing Characteristics

Read (See Figure 1)

		S6840		S68A40		S68B40		
Symbol	Characteristic	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Bus Timing Characteristics (Continued)

Read (See Figure 1)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCE}	Enable Cycle Time	1.0	10	0.666	10	0.5	10	μs
PW_{EH}	Enable Pulse Width, High	0.45	4.5	0.280	4.5	0.22	4.5	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

AC Operating Characteristics

(See Figures 3 and 7)

Symbol	Characteristic	S6840		S68A40		S68B40		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_r, t_f	Input Rise and Fall Times (Figures 4 and 5) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$		1.0		0.666*		0.500*	μs
PW_L	Input Pulse Width (Figure 4) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		ns
PW_H	Input Pulse Width (Figure 5) (Asynchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		$t_{CYCE}+t_{su}+t_{hd}$		ns
t_{su}	Input Setup Time (Figure 6) (Synchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	200		120		75		ns
t_{hd}	Input Hold Time (Figure 6) (Synchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	50		50		50		ns
PW_L, PW_H	Input Pulse Width (Synchronous Mode) $\overline{C3}$ (÷8 Prescaler Mode only)	125		84		62.5		ns
	Output Delay, O1-O3 (Figure 7)							
t_{co}	(V_{OH}=2.4V, Load B) TTL		700		460		340	ns
t_{cm}	(V_{OH}=2.4V, Load D) MOS		450		450		340	ns
t_{cmos}	(V_{OH}=0.7 V_{DD}, Load D) CMOS		2.0		1.35		1.0	μs
t_{IR}	Interrupt Release Time		1.2		0.9		0.7	μs

* t_r and $t_f \leq t_{CYCE}$

Figure 1. Bus Read Timing Characteristics (Read Information from PTM)

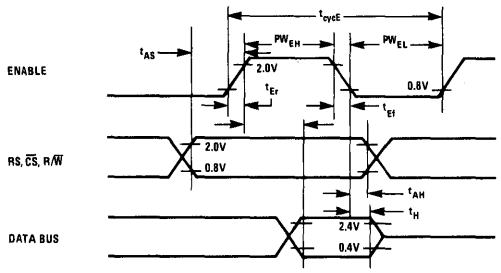


Figure 2. Bus Write Timing Characteristics (Write Information into PTM)

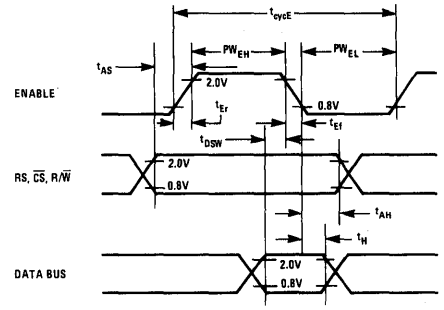


Figure 3. Input Pulse Width Low

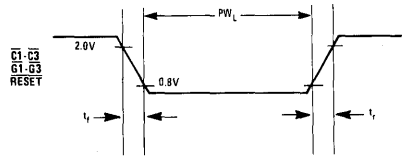


Figure 4. Input Pulse Width High

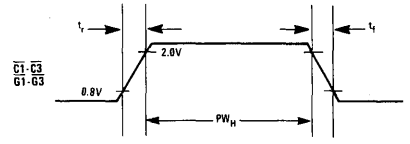


Figure 5. Input Setup and Hold Times

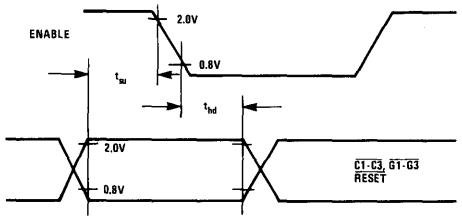


Figure 6. Output Delay

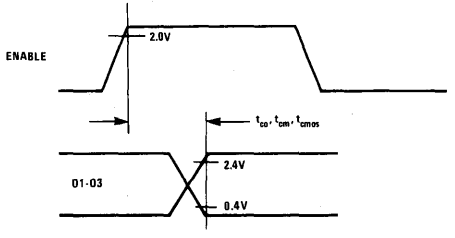


Figure 7. $\overline{IRQ}$ Release Time

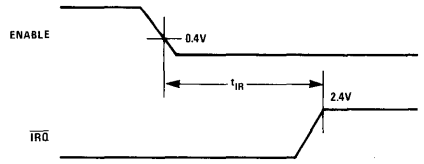
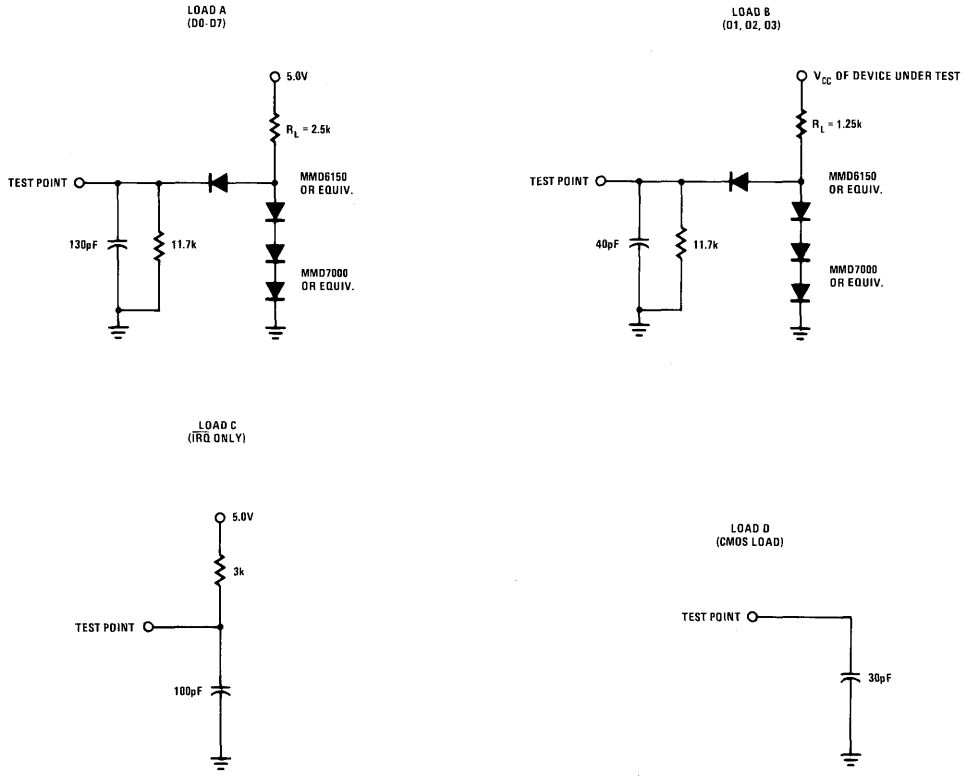


Figure 8. Bus Timing Test Loads



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

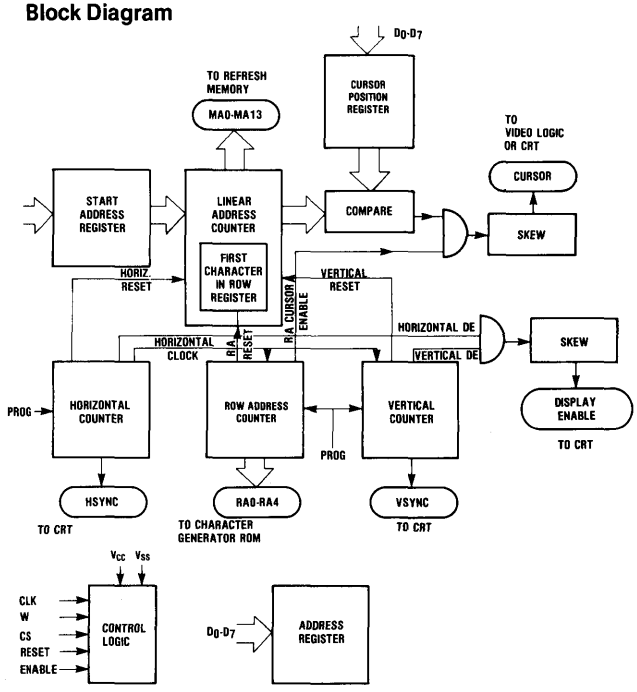
S68045/S68A045/S68B045

CRT CONTROLLER (CRTC)

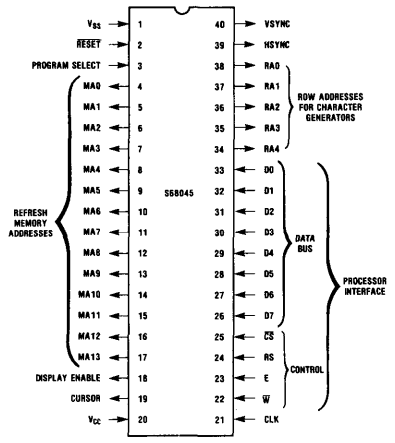
Features

- ☐ Generates Refresh Addresses and Row Selects
- ☐ Generates Video Monitor Inputs: Horizontal and Vertical Sync and Display Enable
- ☐ Low Cost; MC6845/SY6545 Pin Compatible
- ☐ Text Can Be Scrolled on a Character, Line or Page Basis
- ☐ Addresses 16K Bytes of Memory
- ☐ Screen Can Be Up to 128 Characters Tall By 256 Wide
- ☐ Character Font Can Be 32 Lines High With Any Width
- ☐ Two Complete ROM Programs
- ☐ Cursor and/or Display Can Be Delayed 0, 1 or 2 Clock Cycles
- ☐ Four Cursor Modes:
  - Non-Blink
  - Slow Blink
  - Fast Blink
  - Reverse Video With Addition of a Single TTL Gate
- ☐ Three Interlace Modes
  - Normal Sync
  - Interlace Sync
  - Interlace Sync and Video
- ☐ Full Hardware Scrolling
- ☐ NMOS Silicon Gate Technology
- ☐ TTL-Compatible, Single +5 Volt Supply

Block Diagram



Pin Configuration



General Description

The S68045 CRT Controller performs the complex interface between an S6800 Family microprocessor and a raster scan display CRT system. The S68045 is designed to be flexible yet low cost. It is configured to both simplify the development and reduce the cost of equipment such as intelligent terminals, word processing, and information display devices.

The CRT Controller consists of both horizontal and vertical counting circuits, a linear address counter, and control registers. The horizontal and vertical counting circuits generate the Display Enable, HSYNC, VSYNC, and RA0-RA4 signals. The RA0-RA4 lines are scan line count signals to the external character generator ROM. The number of characters per character row, scan lines per character row, character rows per screen, and the horizontal and vertical SYNC position and width are all mask programmable. The S68045 is capable of addressing 16K of memory for display. The CRT may be scrolled or paged through the entire display memory under MPU control. The cursor control register determines the cursor location on the screen, and the cursor format can be programmed for fast blink, slow-blink, or non-blink appearance, with programmable size. By adding a single TTL gate, the cursor can even be reversed video. The device features two complete, independent programs implemented in user-specified ROM. Either set of programmable variables (50/60Hz refresh rate, screen format, etc.) is available to the user at any time.

The S68045 is pin compatible with the MC6845, operates from a single 5-volt supply, and is designed using the latest in minimum-geometry NMOS technology.

Absolute Maximum Ratings

Supply Voltage V_{CC}	−0.3°C to +7.0°C
Input Voltage V_{IN}	−0.3V to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	−55°C to +150°C

Bus Timing Characteristics

Symbol	Parameter	S68045		S68A045		S68B045		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er},t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Electrical Characteristics

V_{CC}=5.0V±5%; V_{SS}=0, T_A=0°C to +70°C unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	−0.3		0.8	Vdc	
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	
V_{OH}	Output High Voltage	2.4			Vdc	I_{LOAD}=−100μA
V_{OL}	Ouput Low Voltage			0.4	Vdc	I_{LOAD}=1.6mA
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7 All Others			12.5 10	pF pF	
C_{OUT}	Output Capacitance All Outputs			10	pF	
P_{WCL}	Minimum Clock Pulse Width, Low	160			ns	
P_{WCH}	Clock Pulse Width, High	200		10,000	ns	
f_c	Clock Frequency			2.5	MHz	
t_{cr}, t_{cf}	Rise and Fall Time for Clock Input			20	ns	
t_{MAD}	Memory Address Delay Time			200	ns	
t_{RAD}	Raster Address Delay Time			200	ns	
t_{DTD}	Display Timing Delay Time			300	ns	
t_{HSD}	Horizontal Sync Delay Time			300	ns	
t_{VSD}	Vertical Sync Delay Time			300	ns	
t_{CDD}	Cursor Display Timing Delay Time			300	ns	

Systems Operation

The S68045 CRTC generates all of the signals needed for the proper operation of a CRT system including HSYNC, VSYNC, Display Enable, Cursor control signals (refer to Figure 1), the refresh memory addresses (MA0-MA13) and row addresses (RA0-RA4). The CRTC's timing is derived from the CLK input, which is divided down from the dot rate counter.

The CRTC, which is compatible with the 6800 family, communicates with the MPU by means of the standard 8-bit data bus. This primary data bus uses a buffered interface for writing information to the display refresh RAM by means of a separate secondary data bus. This arrangement allows the MPU to forget about the display except for those time periods when data is actually being changed on the screen. The address bus for the refresh RAM is continuously multiplexed between the MPU and the CRTC.

Since the MPU is allowed transparent read/write access to the display memory, the refresh RAM appears as just another RAM to the processor. This means that the refresh memory can also be used for program storage. Care should be taken by the system designer, however, to insure that the portion of memory being used for program storage is not actively displayed.

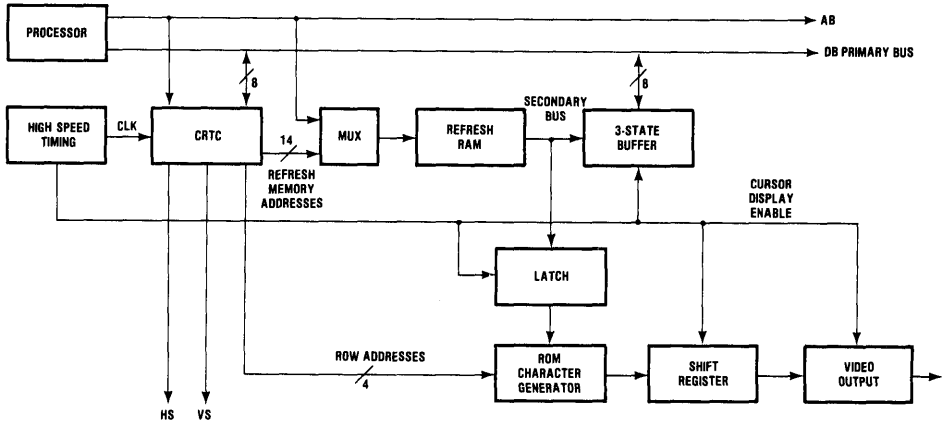
Displayed Data Control

Display Refresh Memory Addresses (MA0-MA13) — 14 bits of address provide the CRTC with access of up to 16K of memory for use in refreshing the screen.

Row Addresses (RA0-RA4) — 5 bits of data that provide the output from the CRTC to the character generator ROM. They allow up to 32 scan lines to be included in a character.

Cursor — This TTL compatible, active high output indicates to external logic that the cursor is being displayed.

Figure 1. Typical CRT Controller System



The character address of the cursor is held in a register, so the cursor's position is not lost even when scrolled off the screen.

CRT Control

All three CRT control signals are TTL compatible, active high outputs.

Display Enable — Indicates that valid data is being clocked to the CRT for the active display area.

Vertical Sync (VSYNC) — Makes certain the CRTC and the CRT's vertical timing are synchronized so the picture is vertically stable.

Horizontal Sync (HSYNC) — Makes certain the CRTC and the CRT's horizontal timing are synchronized so the picture is horizontally stable.

Processor Interface

All processor interface lines are three state, TTL/MOS compatible inputs.

Chip Select ($\overline{CS}$)—The $\overline{CS}$ line selects the CRTC when low to write to the internal Register File. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select — The RS line selects either the Address Register (RS="0") or one of the Data Registers (RS="1") of the internal Register File.

To address one of the software programmable registers (R12, R13, R14 or R15 in Table 2) first access the Address Register ($\overline{CS}$=0, RS=0) and write the number of the desired register. Then write into the actual register by addressing the data register section ($\overline{CS}$=0, RS=1) and enter the appropriate data.

Write ($\overline{W}$) — The $\overline{W}$ line allows a write to the internal Register File.

Data Bus (D0-D7) — The data bus lines (D0-D7) are write-only and allow data transfers to the CRTC internal register file.

Enable (E) — The Enable signal enables the data bus input buffers and clocks data to the CRTC. This signal is usually derived from the processor clock, and the high to low transition is the active edge.

S68045 Control Clock (CLK) — The clock signal is a high impedance, TTL/MOS compatible input which assures the CRTC is synchronized with the CRT itself. The CLK signal is divided down by external circuitry from the dot rate counter. The CLK frequency is equal to

the dot rate frequency divided by the width of a single character block (including framing) expressed in dots, CLK is equal to the character rate.

Program (PROG) — The voltage on this pin determines whether the screen format in ROM 0 (PROG LOW) or ROM 1 (PROG HIGH) is being used.

Reset ($\overline{RES}$) — The $\overline{RES}$ input resets the CRTC. An (active) low input on this line forces these actions:

a) MA0-MA13 are loaded with the contents of R12/R13 (the start address register).

b) The horizontal, vertical, and raster address counter are reset to the first raster line of the first displayed character in the first row.

c) All other outputs go low.

Note that none of the internal registers are affected by $\overline{RES}$.

$\overline{RES}$ on the CRTC differs from the reset for the rest of the 6800 family in the following aspects:

a) MA0-MA13 and RA0-RA4 go to the start addresses, instead of FFFF.

b) Display recommences immediately after $\overline{RES}$ goes high.

Internal Register Description — There is a bank of 15 control registers in the 68045, most of which are mask programmed. The exceptions are the Address Register, the two Start Address Registers (R12 & R13) and the Cursor Location Registers (R14 & R15). All software programmable registers are write only. The Address Register is 5 bits long. The software programmable registers are made available to the data lines whenever the chip select ($\overline{CS}$) goes low. When $\overline{CS}$ goes high, the data lines show a high impedance to the microprocessor.

Horizontal Total Register (R0) — The full horizontal period, expressed in character times, is masked in R0. (See Figure 2a.)

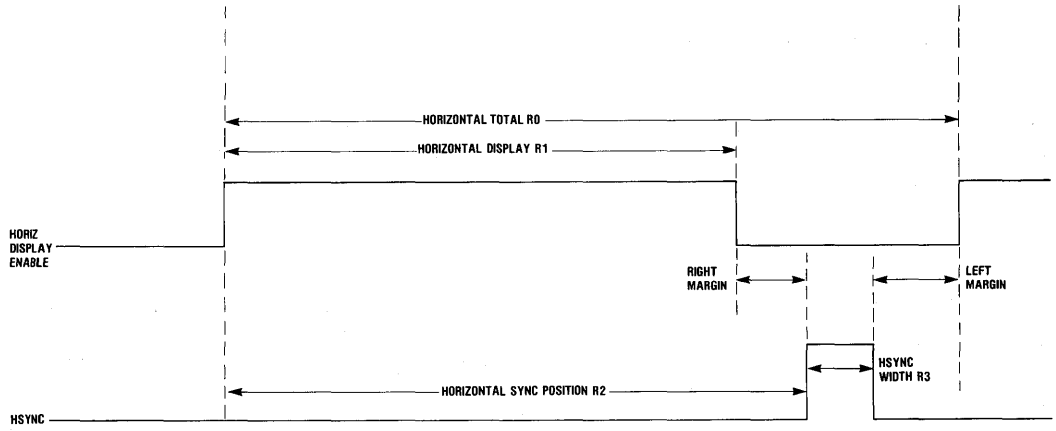
Horizontal Displayed Register (R1) — This register contains the number of characters to be actually displayed in a row. (See Figure 2a.)

Horizontal SYNC Position Register (R2) — The contents of R2 (also in character times) should be slightly larger than the value in R1 to allow for a non-displayed right border. (See Figure 2a.)

Sync Width Register (R3) — The width of the HSYNC pulse expressed in character times is masked into the lower four bits of R3. The width of the HSYNC pulse has to be non-zero.

The width of the VSYNC pulse is masked into the upper

Figure 2a. Approximate Timing Diagram



FOR MORE EXACT DIAGRAMS REFER TO THE BACK OF THE DATA SHEET. THE HORIZONTAL DISPLAY ENABLE IS ANDED WITH THE VERTICAL DISPLAY ENABLE TO PRODUCE THE DISPLAY ENABLE AT PIN 18. NOTE THE (a) FIGURE IS TIMED IN TERMS OF INDIVIDUAL CHARACTERS, WHEREAS THE (b) FIGURE IS TIMED IN TERMS OF CHARACTER ROWS.

four bits of R3 without any modification, with the exception that all zeroes will make VSYNC 16 characters wide.

Vertical Total Register (R4) — This register contains the total number of character rows — both displayed and non-displayed — per screen. This number is just the total number of scan lines used divided by the number of scan lines in a character row. If there is a remainder, it is placed in R5. (See Figure 2b).

Vertical Total Adjust Register (R5) — See description of R4. A fractional number of character row times is used to obtain a refresh rate which is exactly 50HZ, 60HZ, or some other desired frequency. (See Figure 2b).

Vertical Displayed Register (R6) — This register contains the total number of character rows that are actually displayed on the CRT screen. (See Figure 2b).

Vertical SYNC Position (R7) — R7 contains the position of the vertical SYNC pulse in character row times with respect to the top character row. Increasing the value shifts the data up. (See Figure 2b).

Interlace Mode Register (R8) — R8 controls which of the three available raster scan modes will be used (See Figure 3).

- Non-interlace or Normal sync mode
- Interlaced sync mode
- Interlaced sync and Video mode

The Cursor and Display Enable outputs can be delayed (skewed) 0, 1 or 2 clock cycles with respect to the refresh memory address outputs (MA0-MA13). The amount the cursor is delayed is independent of how much the Display Enable signal is delayed. This feature allows the system designer to account for memory address propagation delay through the RAM, ROM, etc.

Maximum Scan Line Register (R9) — Determines the number of scan lines per character row including top and bottom spacing.

Cursor Start Register (R10) — Contains the raster line where the cursor start (see Figure 4). The cursor start line can be anywhere from line 0 to line 31.

The cursor can be in one of the following formats.

- Non-blinking
- Slow blinking (1/16) the vertical refresh rate)
- Fast blinking (1/32 the vertical refresh rate)
- Reverse video (non-blinking, slow blinking, or fast blinking)

The reverse video cursor needs an external TTL XOR gate to be placed in the video circuit.

To implement the reverse video cursor, the cursor start line (R10) should be set to line 0 and the cursor end line (R11) should be set to whatever is in R9 so that the cursor covers the entire block. On the circuit level, the output from the Cursor pin (pin 19) should be taken through the XOR gate along with the output from the shift register. (See Figure 5.) With this setup the character whose memory address is in the cursor register (R14/R15) will have it's background high (because Cursor along is high) but the character itself will be off (because both cursor and the character are both high.

Figure 2b. Approximate Timing Diagram

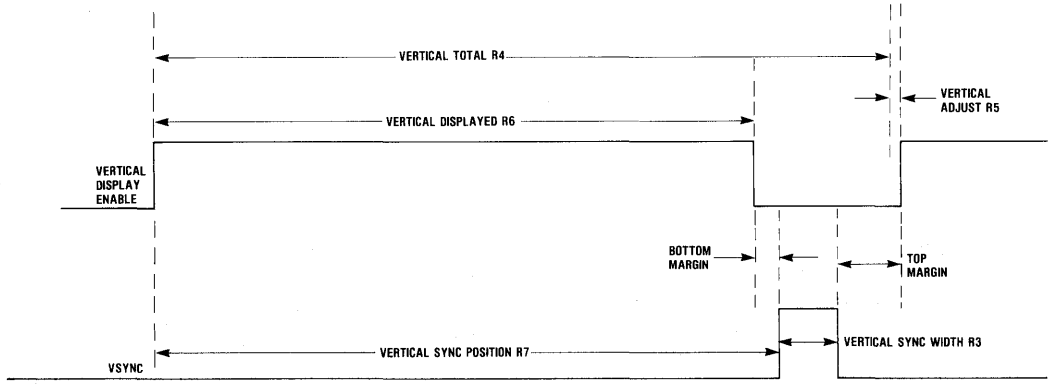


Figure 3. Interface Control

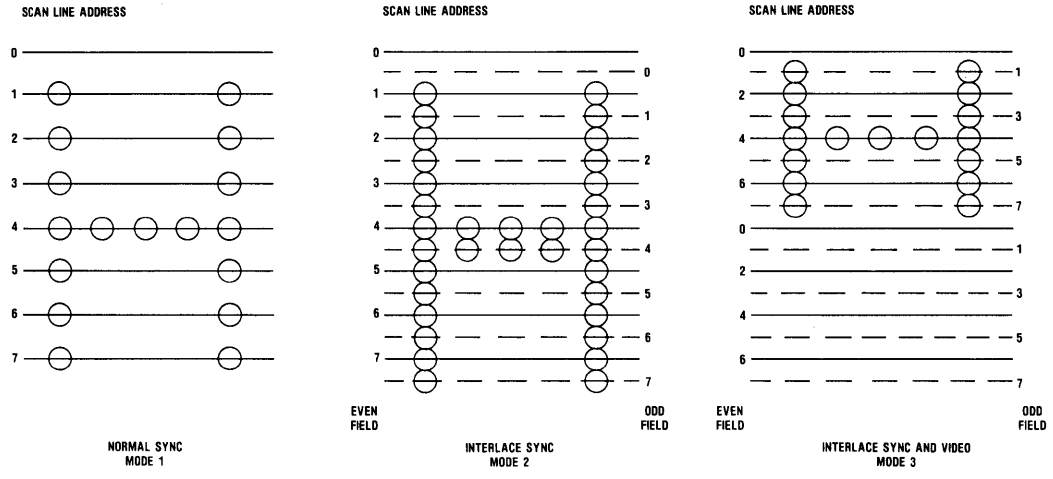
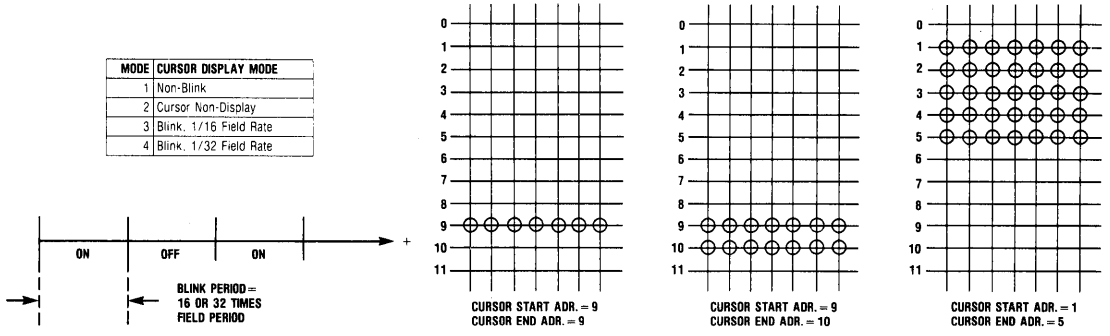


Figure 4. Cursor Control

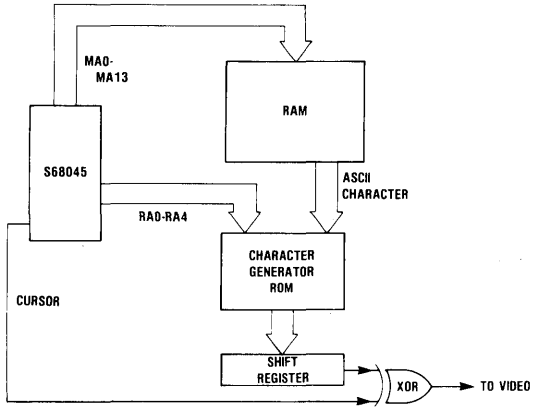
MODE	CURSOR DISPLAY MODE
1	Non-Blink
2	Cursor Non-Display
3	Blink, 1/16 Field Rate
4	Blink, 1/32 Field Rate



Memory Start Address Register (R12/R13) — These two software programmable, write-only registers taken together contain the memory address of the first character displayed on the screen. Register R12 contains the upper six bits of the fourteen refresh memory address bits, while R13 contains the lower eight bits. The Linear Address Generator begins counting from the address in R12/R13. By changing the starting address, the display can be scrolled up or down through the 16K memory block by character, line or page. If the value in R12/R13 is near the end of the 16K block the display will wrap around to the front.

Cursor Address Register (R14/R15) — These two software programmable, write-only registers, taken together, contain the address in memory of the cursor character.

Figure 5. Implementation of a Reversed Video Cursor



Register R14 contains the upper six bits and register R15 contains the lower eight bits of the character. Cursor position is associated with an address in memory rather than with a position on the screen. This way cursor position is not lost when the display is scrolled.

Address Register — The five bit address register is unique in that it does not store any CRT-related information, but is used as the address storage register in an indirect access of the other registers. When the Register Select pin (RS) is low, the address register is accessed by D0-D4. When RS is high, the register whose address is in the address register is accessed.

CRTC Internal Description

There are four counters which determine what the CRTC's output will be (see Block Diagram):

1) Horizontal Counter
2) Vertical Counter
3) Row Address Counter
4) Linear Address Counter

The first two counters, and to some extent the third, take care of the physical operation of the monitor. The Linear Address Counter, on the other hand, is responsible for the data that is displayed on the screen.

Surrounding these counters are the registers R0-R15. Coincidence logic continuously compares the contents of each counter with the contents of the register(s) associated with it. When a match is found, appropriate action is taken; the counter is reset to a fixed or dynamic value, or a flag (such as VSYNC) is set, or both.

Two sets of registers — The start Address Register (R12/R13) and the Cursor Position Register (R14/R15) — are programmable via the Data lines (D0-D7). The other registers are all mask programmed. There are two ROM programs available on each chip. Selection of which ROM program will be accessed is performed by the PROG pin.

Horizontal Counter

The Horizontal Counter produces four output flags: HSYNC, Horizontal Display Enable, Horizontal Reset to the Linear Address Counter, and the horizontal clock.

The Horizontal Counter is driven by the character rate clock, which was derived from the dot rate clock (see Table 1). Immediately after the valid display area is entered the Horizontal Counter is reset to zero but continues incrementing.

HSYNC is the only one of the four signals which is fed to an external device (the CRT). The Horizontal Counter is compared to registers R0, R2 and R3 to give an HSYNC of the desired frequency (R0), position (R2) and width (R3). (See Figure 2a.)

Horizontal Display Enable is an internal flag which, when ANDed with Vertical DE, is output at the Display Enable pin. The Horizontal Counter determines the proper frequency (R0), and width (R1).

The Horizontal Reset and the horizontal clock are actually identical signals: the only difference is the way they are used. Both are pulsed once for each scan line, so their frequency is equal to the character rate clock frequency divided by the entire horizontal period (display, non-display and retrace) expressed in character times

Table 1. Comparison of all CRTC Clocks

NAME	LOCATION OF CLOCK	DIVIDED BY:	CONTROLLING REGISTER	PRODUCES
DOT RATE CLOCK	EXTERNAL	TOTAL WIDTH OF A CHARACTER BLOCK IN DOTS	EXTERNAL	CHARACTER RATE CLOCK
CHARACTER RATE CLOCK	EXTERNAL INPUT	TOTAL NUMBER OF CHARACTERS IN A ROW	R0	HORIZONTAL CLOCK
HORIZONTAL CLOCK	INTERNAL	TOTAL NUMBER OF SCAN LINES IN A CHARACTER ROW	R9	ROW ADDRESS CLOCK
ROW ADDRESS CLOCK	INTERNAL	TOTAL NUMBER OF CHARACTER ROWS PER SCREEN	R4, R5	VERTICAL CLOCK

Table 2. CRTC Internal Register Assignment

REGISTER#	REGISTER FILE	BITS 7	6	5	4	3	2	1	0
R0	HORIZONTAL TOTAL	N_{ht}-1							
R1	HORIZONTAL DISPLAYED	N_{hd}							
R2	HORIZONTAL SYNC POSITION	N_{hsp}-1							
R3	HORIZONTAL SYNC WIDTH	N_{vsw}				N_{hsw}			
R4	VERTICAL TOTAL		N_{vt}-1						
R5	VERTICAL TOTAL ADJUST			N_{adj}					
R6	VERTICAL DISPLAYED		N_{vd}						
R7	VERTICAL SYNC POSITION		N_{vsp}-1						
R8	INTERLACE MODE	CURSOR SKEW		DIS. ENAB. SKEW				INTERLACE	
R9	MAX SCAN LINE ADDRESS			N_r-1*					
R10	CURSOR START		CURSOR BLINK		CURSOR START				
R11	CURSOR END				CURSOR END				
R12	START ADDRESS (H)	START ADDRESS (H)							
R13	START ADDRESS (L)	START ADDRESS (L)							
R14	CURSOR (H)	CURSOR (H)							
R15	CURSOR (L)	CURSOR (L)							

***For Interlace Sync and Video operation, R9 should contain N_r-2.**

NOT USED

CURSOR SKEW

BIT 7	BIT 6	RESULT
0	0	NO SKEW
0	1	1 CHARACTER SKEW
1	0	2 CHARACTER SKEW
1	1	ILLEGAL

DISPLAY ENABLE SKEW

BIT 5	BIT 4	RESULT
0	0	NO SKEW
0	1	1 CHARACTER SKEW
1	0	2 CHARACTER SKEW
1	1	ILLEGAL

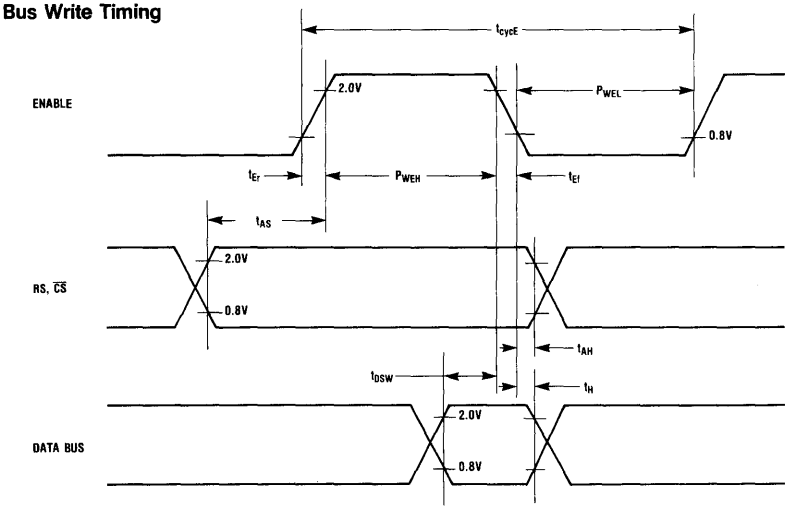
INTERLACE CONTROL

BIT 1	BIT 0	MODE
0	0	NON-INTERLACE
1	0	NON-INTERLACE
0	1	INTERLACE SYNC
1	1	INTERLACE SYNC & VIDEO

CURSOR CONTROL

MODE	BIT 6	BIT 5
NON-BLINK	0	0
CURSOR NON DISPLAY	0	1
BLINK @ 1/16 FIELD PERIOD	1	0
BLINK @ 1/32 FIELD PERIOD	1	1

Figure 6. Bus Write Timing



(which is stored in R0). The horizontal clock drives the Vertical and Row address Counters. The horizontal reset is discussed with the Linear Address Counter.

Vertical Counter

The Vertical Counter produces three output flags: VSYNC, Vertical Display Enable, and Vertical Reset to the Linear Address Counter. The Vertical Counter is driven by the horizontal clock. Immediately after vertical retrace the Vertical Counter is reset to zero but continues incrementing.

VSYNC is the only one of the three signals which is fed to an external device (the CRT). The Vertical Counter is compared to registers R3, R4, R5 and R7 to give a VSYNC of the desired frequency (R4, R5), position (R7) and width (R3). (See Figure 2b.)

Vertical Display Enable is an internal flag which, when ANDed with Horizontal DE, is output at the Display Enable pin. The Vertical Counter determines the proper frequency (R4, R5) and width (R6).

Vertical Reset is pulsed once for each screen. The frequency of Vertical Reset is equal to the horizontal clock frequency divided by the total number of scan lines in a screen (which is equal to (R4×R9)+R5). It will be discussed with the Linear Address Counter.

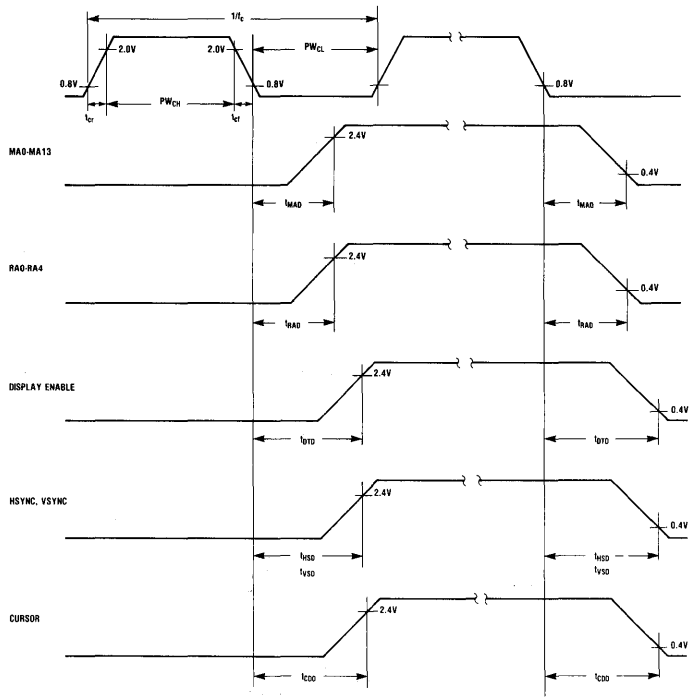
Row Address Counter

The Row Address Counter produces three sets of output: the five Row Address lines (RA0-RA4), the Row Address Cursor Enable flag and the Row Address Reset flag. The Row Address Counter is driven by the horizontal clock. Immediately after a full character row has been completed by the Row Address Counter is reset to zero but continues incrementing. Note that the Row Address Counter actually counts scan lines, which are different from character rows. A full character row consists of however many scan lines are in register R9.

The Row Address Lines, RA0-RA4, are the only data lines from the Row Address Counter that are fed to an external device (the character generator ROM). The Row Address lines just carry the count that is currently in the Row Address Counter. The counter is reset whenever the count equals the contents of the Maximum Scan Line Register (R9.)

Row Address Cursor Enable is a flag going to the Cursor output AND gate. The Row Address Cursor Enable flag goes high whenever the count in the Row Address Counter is greater than or equal to the Cursor Start Register (R10) but less than or equal to the Cursor End Register (R11). The other input to the Cursor output AND gate goes high whenever the address in the Linear

Figure 7. Bus Timing Character



Address Counter is equal to the address in the Cursor Position Reister (R14/R15).

Row Address Reset is pulsed whenever the Row Address Counter is reset. It will be discussed with the Linear Address Counter.

Linear Address Counter

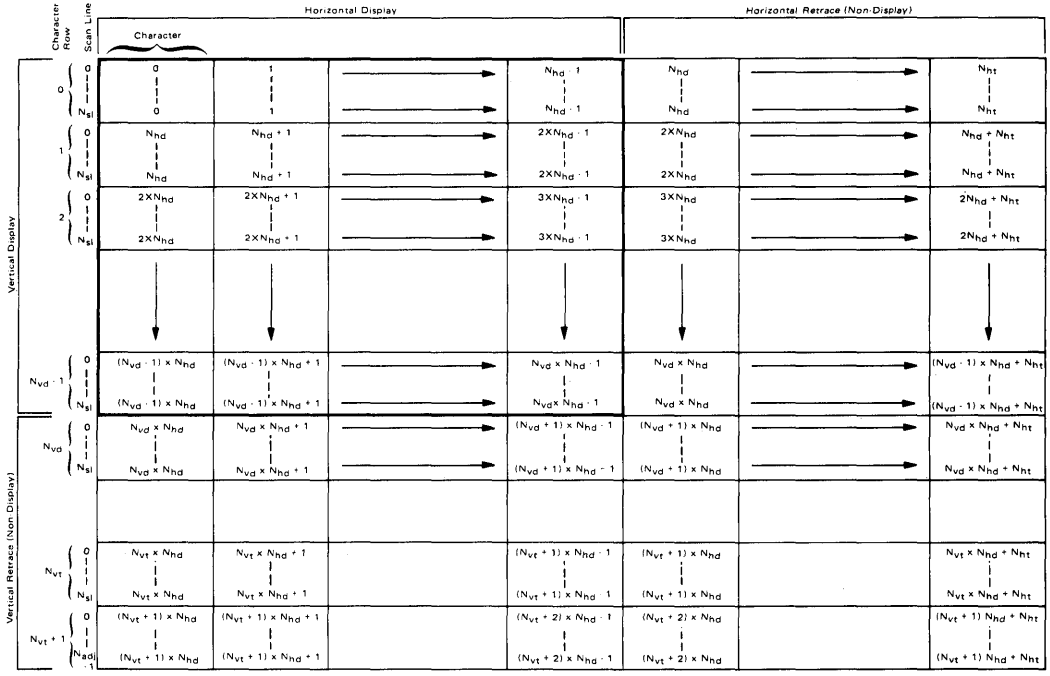
The Linear Address Counter (LAC) produces only one set of outputs: The Refresh Memory Address lines (MA0-MA13). These fourteen bits are fed externally to the Refresh RAM and internally to the Cursor Position coincidence circuit. The LAC is driven by the character rate clock and continuously increments during the display, non-display and retrace portions of the screen. It contains an internal read/write register which stores the memory address of the first displayed character in the current row.

When any of the three Reset flags already mentioned (Horizontal, Row Address and Vertical) is pulsed, the value in the internal register is loaded into the counter. If the reset is a Horizontal Reset the value in the internal register is not modified before the load. If the reset is a Row Address Reset, the value in the internal "first character" register is first increased by the number of characters displayed on a single character row (register R1). The new contents of the internal register are then loaded into the Linear Address Counter.

If the reset is a Vertical Reset, the value in Start Address Register (R12/R13) is first loaded into the internal register, and then into the Linear Address Counter.

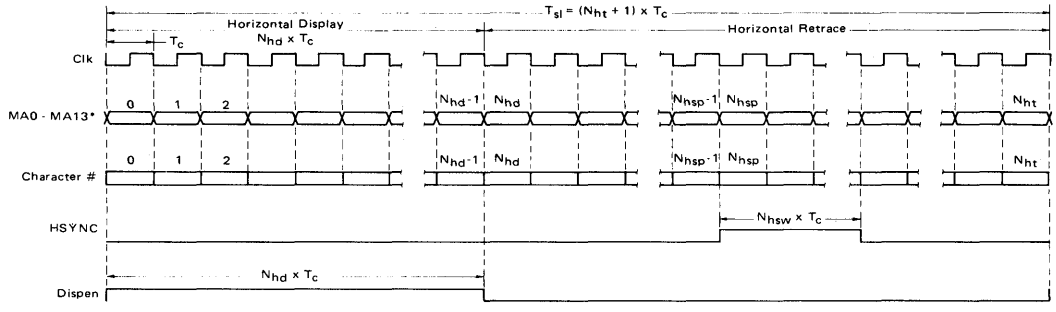
The fourteen output lines allow 16K of memory to be accessed. By incrementing or decrementing the number in the Start Address Register, the screen can be scrolled forward or backward through Display Refresh RAM on a character, line, or page basis.

Figure 8. Refresh Memory Addressing (MA0-MA13) State Chart



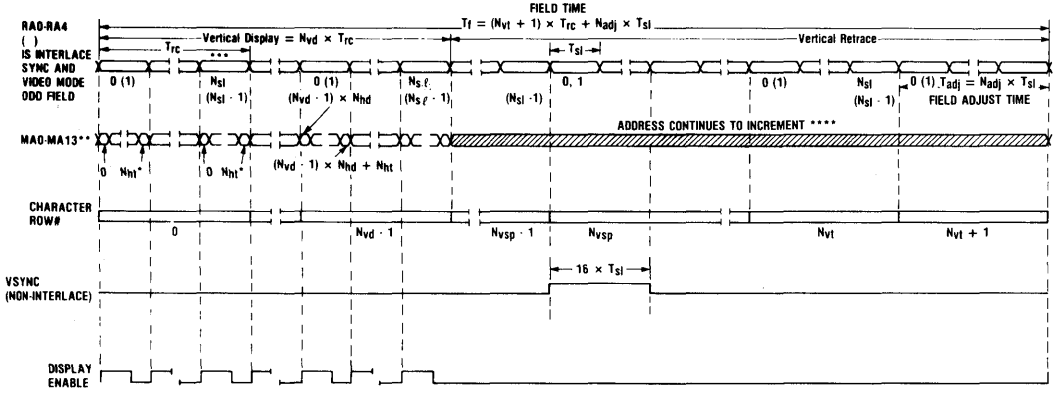
NOTE 1 The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0. Only Non-Interlace and Interlace Sync Modes are shown.

Figure 9. CRTC Horizontal Timing



*TIMING IS SHOWN FOR FIRST DISPLAYED SCAN ROW ONLY SEE CHART IN FIGURE 10 FOR OTHER ROWS. THE INTIAL MA IS DETERMINED BY THE CONTENTS OF START ADDRESS REGISTER, R12/R13. TIMING IS SHOWN FOR R12/R13 = 0.

Figure 10. CRTC Vertical Timing

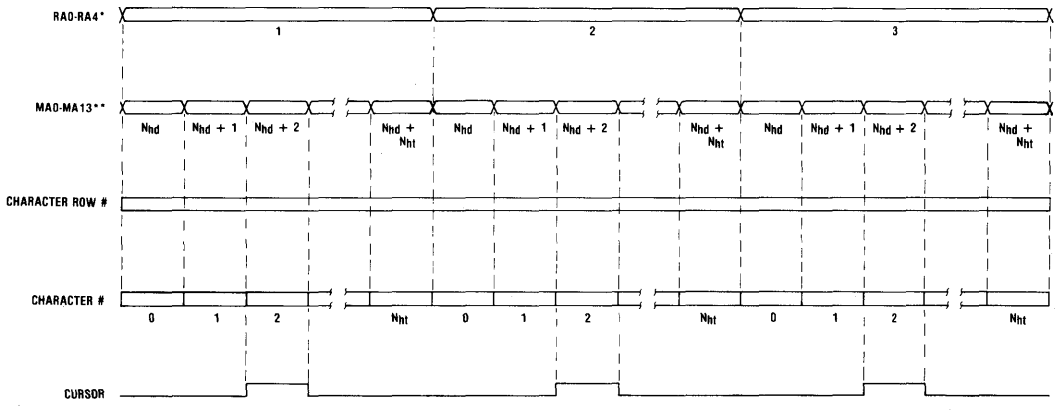


*N_{ht} THERE MUST BE AN EVEN NUMBER OF CHARACTER TIMES FOR BOTH INTERLACE MODES.

**INITIAL MA IS DETERMINED BY R12/R13 (START ADDRESS REGISTER), WHICH IS ZERO IN THIS TIMING EXAMPLE.

***N_{sl} MUST BE AN ODD NUMBER FOR INTERLACE SYNC AND VIDEO MODE.

Figure 11. Cursor Timing



* Timing is shown for non-interlace and interlace sync modes.
Example shown has cursor programmed as:
Cursor Register = N_{hd} + 2
Cursor Start = 1
Cursor End = 3

** The initial MA is determined by the contents of Start Address Register, R12/R13. Timing is shown for R12/R13 = 0.

AMERICAN MICROSYSTEMS, INC.

S6846

ROM-I/O-TIMER

Features

- 2048x8-Bit Bytes of Mask-Programmable ROM
- 8-Bit Bidirectional Data Port for Parallel Interface Plus Two Control Lines
- Programmable Interval Timer-Counter Functions
- Programmable I/O Peripheral Data, Control and Direction Registers
- Compatible with the Complete S6800 Microcomputer Product Family
- TTL-Compatible Data and Peripheral Lines
- Single 5 Volt Power Supply

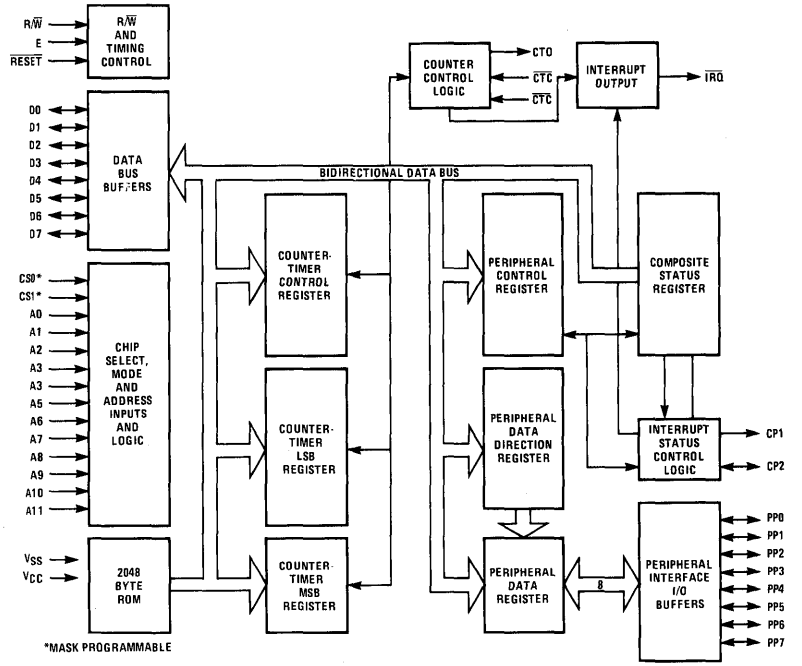
General Description

The S6846 combination chip provides the means, in conjunction with the S6802, to develop a basic 2-chip microcomputer system. The S6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

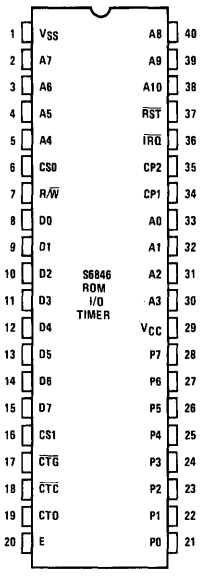
This device is capable of interfacing with the S6802 (basic S6800, clock and 128 bytes of RAM) as well as the S6800 if desired. No external logic is required to interface with most peripheral devices.

The S6846 combination chip may be partitioned into three functional operating sections: programmed storage, timer-counter functions, and a parallel I/O port.

Block Diagram



Pin Configuration



General Description (Continued)

Programmed Storage

The mask-programmable ROM section is similar to other AMI ROM products. The ROM is organized in a 2048 by 8-bit array to provide read only storage for a minimum microcomputer system. Two mask-programmable chip selects are available for user definition.

Address inputs A0-A10 allow any of the 2048 bytes of ROM to be uniquely addressed. Internal registers associated with the I/O functions may be selected with A0, A1 and A2. Bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the S6846.

Timer-Counter Functions

Under software control this 16-bit binary counter may be programmed to count events, measure frequencies and time intervals, or similar tasks. It may also be used for square wave generation, single pulses of controlled duration, and gated delayed signals. Interrupts may be generated from a number of conditions selectable by software programming.

The timer-counter control register allows control of the interrupt enables, output enables, and selection of an internal or external clock source. Input pin $\overline{CTC}$ (counter-timer clock) will accept an asynchronous pulse to be used as a clock to decrement the internal register for the counter-timer. If the divide-by-8 prescaler is used, the maximum clock rate can be four times the master clock frequency with a maximum of 4 MHz. Gate input ($\overline{CTG}$) accepts an asynchronous TTL-compatible signal which may be used as a trigger or gating function to the counter-timer. A counter-timer output ($\overline{CTO}$) is also available and is under software control via selected bits in the timer-counter control register. This mode of operation is dependent on the control register, the gate input, and the external clock.

Parallel I/O Port

The parallel bidirectional I/O port has functional operational characteristics similar to the B port on the S6821 PIA. This includes 8 bidirectional data lines and two handshake control signals. The control and operation of these lines are completely software programmable.

The interrupt input (CP1) will set the interrupt flags of the peripheral control register. The peripheral control (CP2) may be programmed to act as an interrupt input or as a peripheral control output.

S6800

Figure 1. Typical Microcomputer

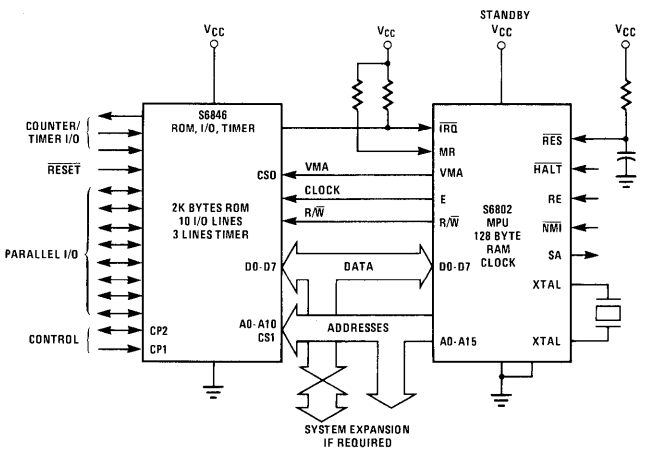


Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the S6800 Microcomputer family if desired.

Absolute Maximum Ratings

Supply Voltage	-0.3Vdc to +7.0Vdc
Input Voltage	-0.3Vdc to +7.0Vdc
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Thermal Resistance	70°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage — All Inputs	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage — All Inputs	V_{SS} -0.3		V_{SS} + 0.8	Vdc	
V_{OS}	Clock Overshoot/Undershoot — Input High Level — Input Low Level	V_{CC} -0.5 V_{SS} -0.5		V_{CC} + 0.5 V_{SS} + 0.5	Vdc	
I_{in}	Input Leakage Current — R/$\overline{W}$, $\overline{Reset}$, CS0, CS1 CP1, $\overline{CTG}$, $\overline{CTC}$, E, A0-A11		1.0	2.5 100	μAdc	V_{in} = 0 to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current — D0-D7 PP0-PP7, CR2		2.0	10 100	μAdc	V_{in} 0.4 to 2.4Vdc
V_{OH}	Output High Voltage D0-D7 CP2, PP0-PP7 Other Outputs	 V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4			Vdc Vdc	 I_{Load} = -205μAdc, I_{Load} = -145μAdc, I_{Load} = -100μAdc
V_{OL}	Output Low Voltage D0-D7 Other Outputs			 V_{SS} + 0.4 V_{SS} + 0.4	Vdc	 I_{Load} = 1.6mAdc I_{Load} = 3.2mAdc
I_{OH}	Output High Current (Sourcing) D0-D7 Other Outputs CP2, PP0-PP7	 -205 -200 -1.0		 -10	μAdc mADC	 V_{OH} = 2.4Vdc V_O = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{OL}	Output Low Current (Sinking) D0-D7 Other Outputs	 1.6 3.2			mAdc	 V_{OL} = 0.4Vdc
I_{LOH}	Output Leakage Current (Off State) — $\overline{IRQ}$			10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation			1000	mW	
C_{in}	Capacitance D0-D7 PP0-PP7, CP2 A0-A10, R/$\overline{W}$, $\overline{Reset}$, CS0, CS1, CP1, $\overline{CTC}$, $\overline{CTG}$ $\overline{IRQ}$			20 12.5 10 7.5	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
C_{out}	PP0-PP7, CP2, CTO			5.0 10	pF	
f	Frequency of Operation	0.1		1.0	MHz	
	Clock Timing					
t_{cycE}	Cycle Time	1.0			μs	
t_{RL}	Reset Low Time	2			μs	
t_{IR}	Interrupt Release			1.6	μs	

Read/Write Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
PW_{EL}	Enable Pulse Width, Low	430			ns	
PW_{EH}	Enable Pulse Width, High	430			ns	
t_{AS}	Set Up Time (Address CS0, CS1, R/W)	160			ns	
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Ef}, t_{Er}	Rise and Fall Time			25	ns	
t_{DSW}	Data Set Up Time	195			ns	

Bus Timing
Peripheral I/O Lines

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PDSU}	Peripheral Data Setup	200			ns	
t_{Pr}, t_{Pc}	Rise and Fall Times CP1, CP2			1.0	μs	
t_{CP2}	Delay Time E to CP2 Fall			1.0	μs	
t_{DC}	Delay Time I/O Data CP2 Fall	20			μs	
t_{RS1}	Delay Time E to CP2 Rise			1.0	μs	
t_{RS2}	Delay Time CP1 to CP2 Rise			2.0	μs	
t_{PDW}	Peripheral Data Delay			1.0	μs	

Timer-Counter Lines

t_{CR}, t_{CF}	Input Rise and Fall Time CTC and CTG			100	ns	
t_{PWH}	Input Pulse Width High (Asynchronous Mode)	t_{cyc} + 250			ns	
t_{PWL}	Input Pulse Width Low (Asynchronous Mode)	t_{cyc} + 250			ns	
t_{su}	Input Setup Time (Synchronous Mode)	200			ns	
t_{hd}	Input Hold Time (Synchronous Mode)	50			ns	
t_{CTO}	Output Delay			1.0	μs	

Figure 2. Bus Read Timing
(Read Information from S6846)

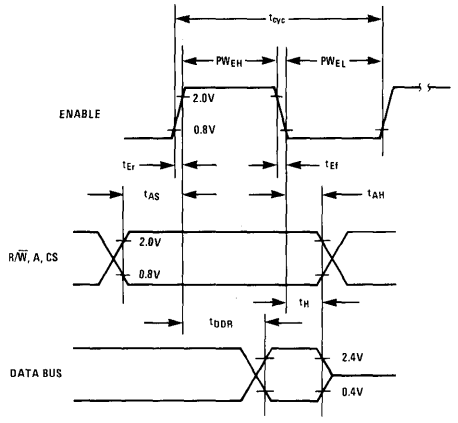


Figure 3. Bus Write Timing
(Write Information from MPU)

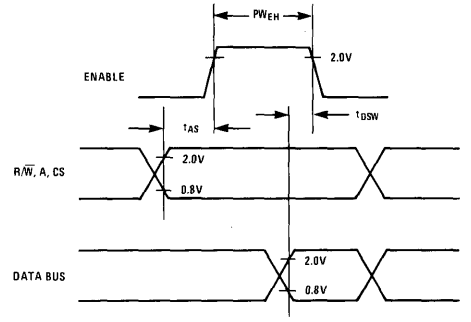


Figure 4. Peripheral Data and CP2 Delay
(Control Mode PCR5 = 1, PCR4 = 0, PCR3 = 1)

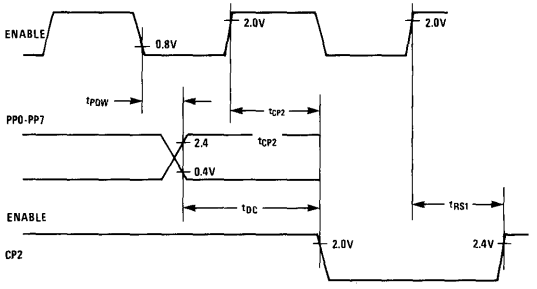


Figure 5. IRQ Release Time

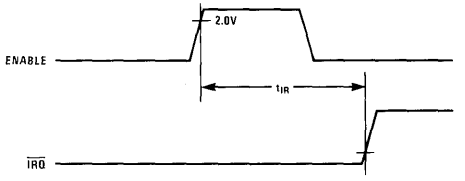


Figure 6. Peripheral Port Setup Time

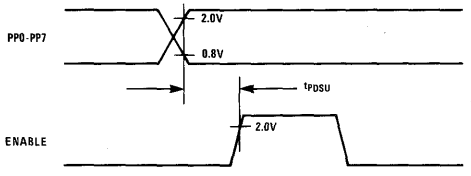


Figure 7. CP2 Delay Time
(PCR5 = 1, PCR4 = 0, PCR3 = 0)

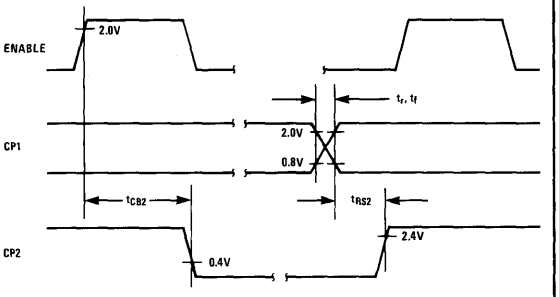


Figure 8. Input Pulse Widths

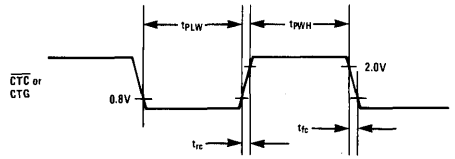
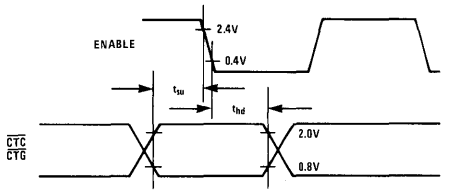


Figure 9. Input Setup and Hold Times



NOTE: This mode is valid only for synchronous operation.

Figure 10. Output Delay

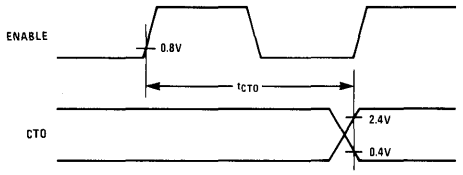
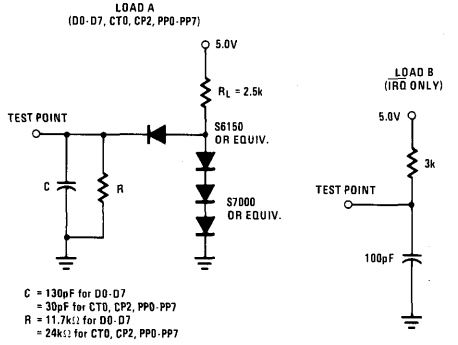


Figure 11. Bus Timing Test Loads



C = 130pF for D0-D7
= 30pF for CTO, CP2, PP0-PP7
R = 11.7kΩ for D0-D7
= 24kΩ for CTO, CP2, PP0-PP7

S6800

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S68488

GENERAL PURPOSE INTERFACE ADAPTER

Features

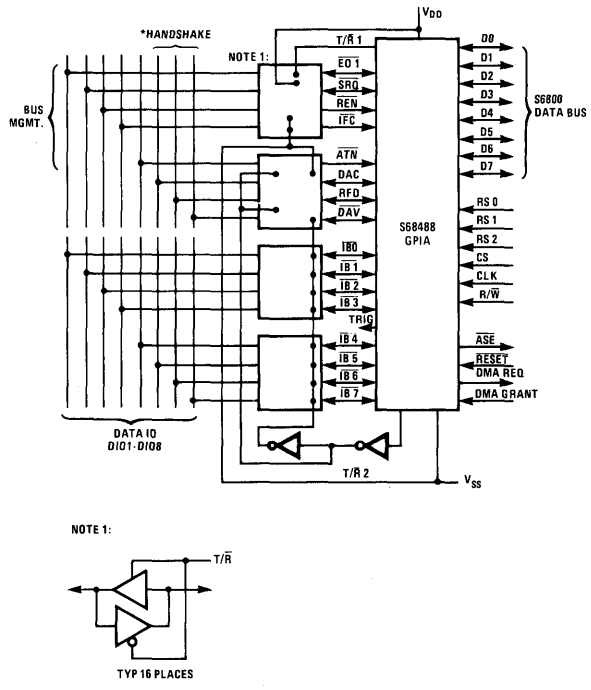
- ☐ Single or Dual Primary Address Recognition
- ☐ Secondary Address Capability
- ☐ Complete Source and Acceptor Handshakes
- ☐ Programmable Interrupts
- ☐ RFD Holdoff to Prevent Data Overrun
- ☐ Operates with DMA Controller
- ☐ Serial and Parallel Polling Capability
- ☐ Talk-Only or Listen-Only Capability
- ☐ Selectable Automatic Features to Minimize Software
- ☐ Synchronization Trigger Output
- ☐ S6800 Bus Compatible

General Description

The S68488 GPIA provides the means to interface between the IEEE488 standard instrument bus and the S6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

The S68488 will automatically handle all handshake protocol needed on the instrument bus.

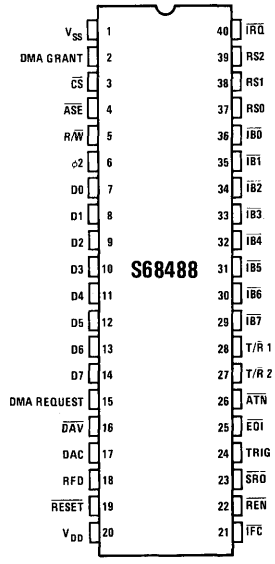
Block Diagram



NOTE 1:

*The 3-wire handshake described is the subject of patents owned by Hewlett-Packard Co.

Pin Configuration



Functional Description

The IEEE 488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communiation to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. A bus controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines; those devices which have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a PC board by a microprocessor as a part of the initialization sequence.

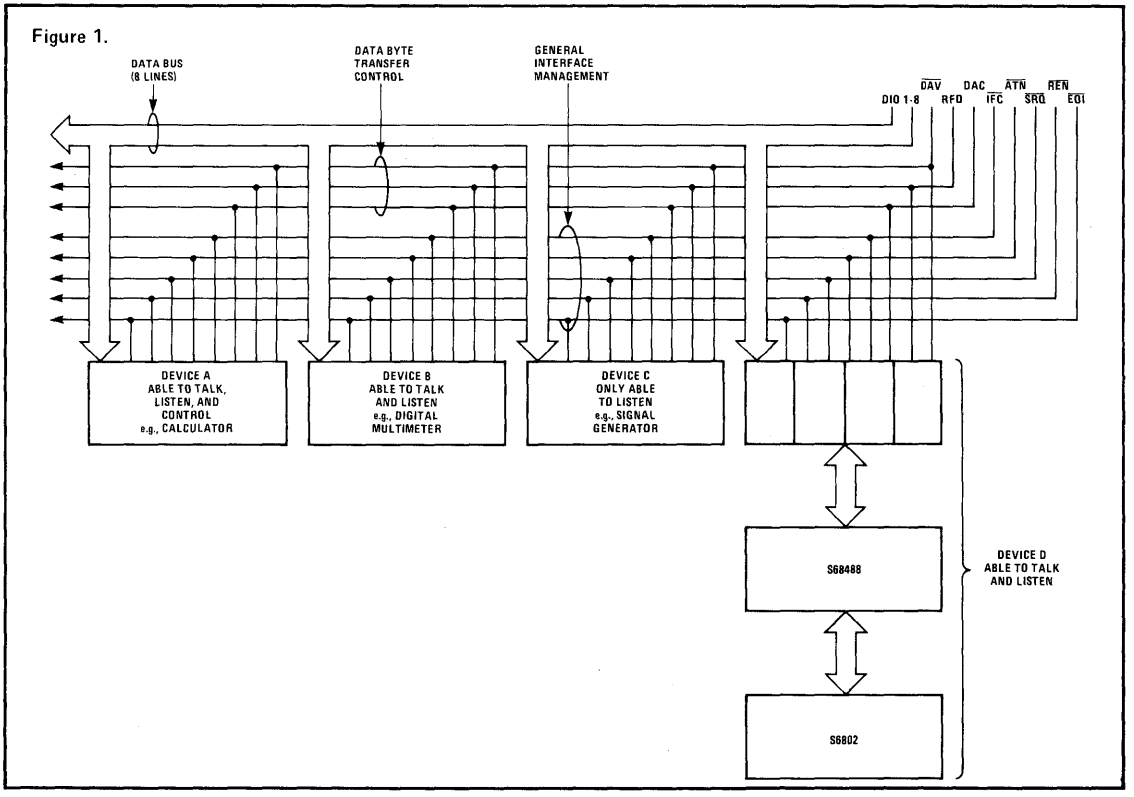
When the controller makes the attention line true, instrument bus commands may also be sent to single or multiple GPIAs.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive the same data concurrently.

The GPIA is designed to work with standard 488 bus driver Ics (S3448As) to meet the complete electrical specifications of the IEEE488 bus. Additionally, a powered-off instrument may be powered-on without disturbing the 488 bus. With some additional logic, the GPIA could be used with other microprocessors.

The S68488 GPIA has been designed to interface between the S6800 microprocessor and the complex protocol of the IEEE488 instrument bus. Many instrument bus protocol functions are handled automatically by the GPIA and require no additional MPU action. Other functions require minimum MPU response due to a large number of internal registers conveying information on the state of the GPIA and the instrument bus.

Figure 1.



Maximum Ratings

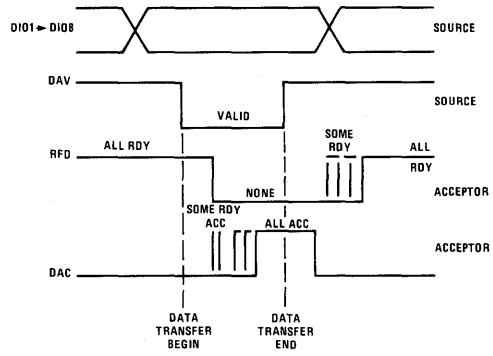
Supply Voltage	-0.3Vdc to +7.0Vdc
Input Voltage	-0.3Vdc to +7.0Vdc
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Thermal Resistance	+82.5°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} - 0.3		V_{SS} + 0.8		
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	V_{IN} = 0 to 5.25V
I_{TSI}	Three-State (Off State) Input Current D0-D7		2.0	10	μAdc	V_{IN} = 0.4 to 2.4V
V_{OH}	Output High Voltage D0-D7	V_{SS} + 2.4			Vdc	I_{load} = -205μA
V_{OL}	Output Low Voltage D0-D7 $\overline{IRQ}$			V_{SS} + 0.4 V_{SS} + 0.4	Vdc	I_{load} = 1.6mA I_{load} = 3.2mA
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7 All Others			12.5 7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz

Figure 2. Source and Acceptor Handshake



Bus Timing Characteristics

Read (See Figure 3)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	See Figure 3
PW_{EH}	Enable Pulse Width, High	0.45			μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160			ns	
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Write (See Figure 4)

t_{cycE}	Enable Cycle Time	1.0			μs	See Figure 4
PW_{EH}	Enable Pulse Width, High	0.45			μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160			ns	
t_{DSW}	Data Setup Time	195			ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Output (See Figure 5)

t_{HD}	Output Delay Time			400	ns	$\overline{DAV}$, DAC, RFD, $\overline{EOI}$, $\overline{ATN}$ valid
$t_{T/\overline{R}1, 2D}$				400	ns	T/$\overline{R}$1, T/$\overline{R}$2 valid

Figure 3. Bus Read Timing Characteristics (Read Information from GPIA)

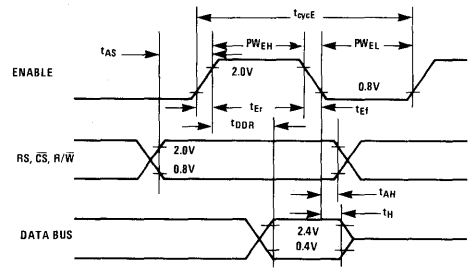


Figure 4. Bus Write Timing Characteristics (Write Information into GPIA)

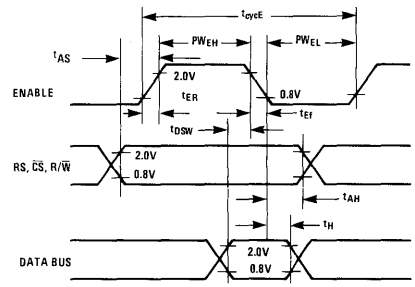
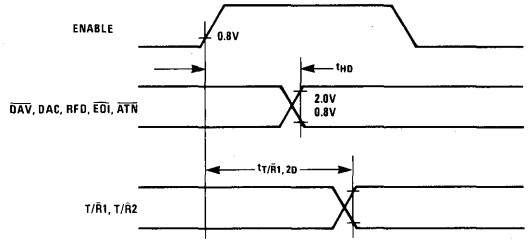


Figure 5. Output Bus Timing



A.C. Time Values

Symbol*	Parameter		Min.	Typ.	Max.	Unit	Conditions
T_1	Settling Time for Multiple Message	SH		≥2		μs**	
t_2	Response to $\overline{ATN}$	SH, AH, T, L		≤200		ns	
T_3	Interface Message Accept Time †	AH		>0		ϕ	
t_4	Response to $\overline{IFC}$ or $\overline{REN}$ False	T, TE, L, LE		<100		μs	
t_5	Response to $\overline{ATN} \bullet \overline{EOI}$	PP		≤200		ns	

* Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

** If three-state drivers are used on the $\overline{DIO}$ – $\overline{DAV}$ and $\overline{EOI}$ lines, T_1 may be:
(1) ≥1100ns
(2) Or ≥700ns if it is known that within the controller $\overline{ATN}$ is driven by a three-state driver.
(3) Or ≥500ns for all subsequent bytes following the first sent after each false transition of $\overline{ATN}$ [the first byte must be sent in accordance with (1) or (2)].

† Time required for interface functions to accept, not necessarily respond to interface messages.

ϕ Implementation dependent.

MPU bus clock rate – The current 6800 bus clock is ≤ 1MHz but part should operate at 1.5MHz (design goal), with appropriate settling times (T1).

ASYNCHRONOUS COMMUNICATION INTERFACE ADAPTER (ACIA)

Features

- ☐ 8-Bit Bi-directional Data Bus for Communication with MPU
- ☐ False Start Bit Deletion
- ☐ Peripheral/Modem Control Functions
- ☐ Double Buffered Receiver and Transmitter
- ☐ One or Two Stop Bit Operation
- ☐ Eight and Nine-Bit Transmission With Optional Even and Odd Parity
- ☐ Parity, Overrun and Framing Error Checking
- ☐ Programmable Control Register
- ☐ Optional ÷1, ÷16, and ÷64 Clock Modes
- ☐ Up to 500,000 bps Transmission

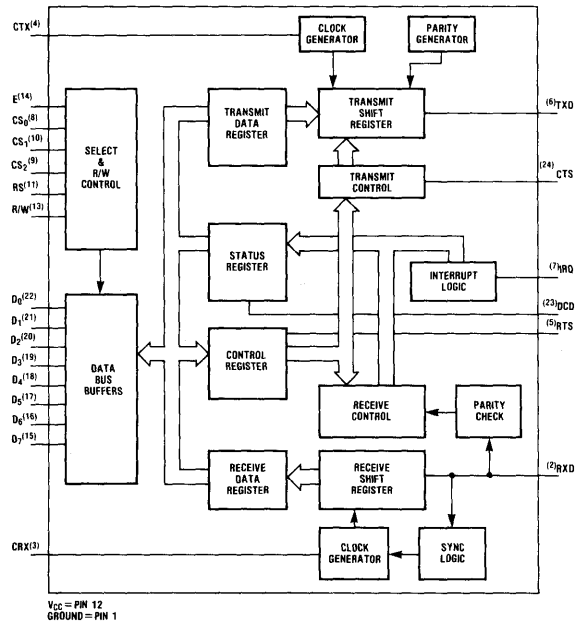
Functional Description

The S6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S6800 Microprocessing Unit.

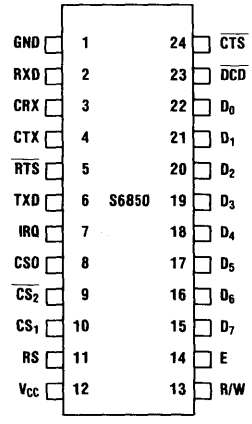
The S6850 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided. These lines allow the ACIA to interface directly with the S6860 0-600 bps digital modem.

S6800

Block Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage	−0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Input Voltage	−0.3V to +7.0V
Storage Temperature Range	−55°C to +150°C

*NOTE: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC (Static) Characteristics: (V_{CC} = 5.0V ±5%, T_A = 25°C, unless otherwise noted.)

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage (Normal Operating Levels)	+2.0	—	V_{CC}	Vdc
V_{IL}	Input Low Voltage (Normal Operating Levels)	−0.3	—	+0.4	Vdc
V_{IHT}	Input High Threshold Voltage All Inputs Except Enable	+2.0	—	—	Vdc
V_{ILT}	Input Low Threshold Voltage All Inputs Except Enable	—	—	+0.8	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.0 Vdc) R/W, RS, CS_0, CS_1, $\overline{CS_2}$, Enable	—	1.0	2.5	μAdc
I_{TSI}	Three-State (Off State) Input Current (V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = max) D_0, D_7	—	2.0	10	μAdc
V_{OH}	Output High Voltage (I_{LOAD} = 100μAdc, Enable Pulse Width 25μs) All Outputs Except $\overline{IRQ}$	+2.4	—	—	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc) Enable Pulse Width 25μs	—	—	+0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$				
P_D	Power Dissipation	—	300	525	mW
C_{IN}	Input Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)				pF
	D_0 - D_7		—	10	12.5
	R/W, RS, CS_0, CS_1, $\overline{CS_2}$, RXD, $\overline{CTD}$, $\overline{DCD}$, CTX, CRX		—	7.0	7.5
	Enable		—	7.0	7.5
C_{OUT}	Output Capacitance (V_{IN} = 0, T_A = 25°C, f = 1.0MHz)	—	—	10	pF

Figure 1. Enable Signal Characteristics

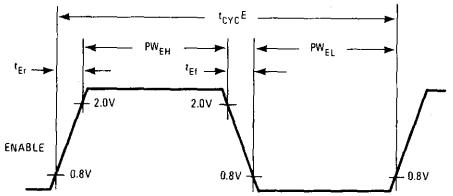
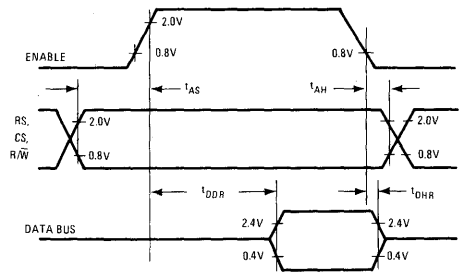


Figure 2. Bus Read Timing Characteristics



AC (Dynamic) Characteristics

Loading = 130pF and one TTL load for D_0-D_7 = 20pF and 1 TTL load for RTS and TXD = 100pF and 3KΩ to V_{CC} for $\overline{IRQ}$.

Symbol	Parameter	S6850 Min.	S6850 Max.	S68A50 Min.	S68A50 Max.	S68B50 Min.	S68B50 Max.	Units
$t_{cyc(E)}$	Enable Cycle Time	1000		666		500		ns
PW_{EH}	Enable Pulse Width, High	450		280		220		ns
PW_{EL}	Enable Pulse Width, Low	430		280		210		ns
t_{Er},t_{Ef}	Enable Pulse Rise and Fall Times		25		25		25	ns
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{DDR}	Data Delay Time, Read		320		220		180	ns
t_{DHR}	Data Hold Time, Read	10		10		10		ns
t_{DSW}	Data Setup Time, Write	195		80		60		ns
t_{DHW}	Data Hold Time, Write	10		10		10		ns

Transmit/Receive Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Unit
f_C					
	÷1 mode			500	KHz
	÷16 mode			800	KHz
	÷64 mode			800	KHz
PW_{CL}	Clock Pulse Width, Low State	600			nsec
PW_{CH}	Clock Pulse Width, High State	600			nsec
T_{TDD}	Delay Time, Transmit Clock to Data Out			1.0	μsec
T_{RDSU}	Set Up Time, Receive Data	500			nsec
T_{RDH}	Hold Time, Receive Data	500			nsec
T_{IRQ}	Delay Time, Enable to $\overline{IRQ}$ Reset			1.2	μsec
T_{RTS}	Delay Time, Enable to $\overline{RTS}$			1.0	μsec

Figure 3. Bus Write Timing Characteristics

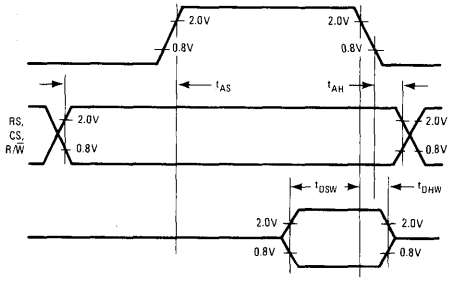


Figure 4. Bus Timing Test Loads

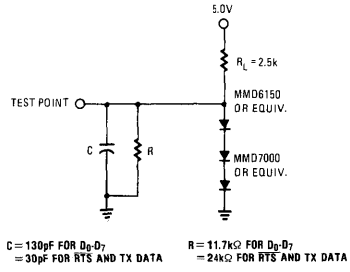
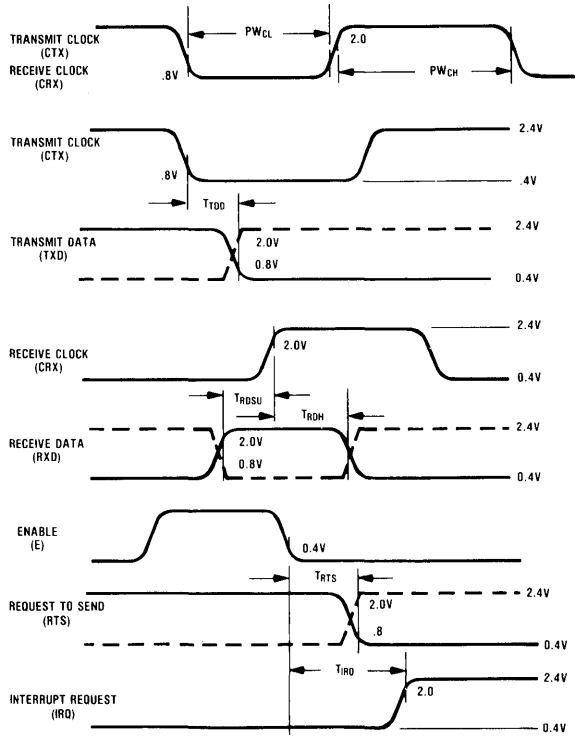


Figure 5. Transmit/Receive Timing



MPU/ACIA Interface

Pin	Label	Function
(22)	D_0	**ACIA Bi-directional Data Lines**—The bi-directional data lines (D_0-D_7) allow for data transfer between the ACIA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an ACIA read operation. The Read/Write line is in the read (high) state when the ACIA is selected for a read operation.
(21)	D_1	
(20)	D_2	
(19)	D_3	
(18)	D_4	
(17)	D_5	
(16)	D_6	
(15)	D_7	
(14)	E	**ACIA Enable Signal**—The Enable signal (E) is a high impedance TTL compatible input that enables the bus input/output data buffers and clocks data to and from the ACIA. This signal will normally be a derivative of the S6800 02 clock.
(13)	R/W	**Read/Write Control Signal**—The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the ACIA's input/output data bus interface. When Read/Write is high (MPU Read cycle), the ACIA output driver is turned on and a selected register is read. When it is low, the ACIA output driver is turned off and the MPU writes into a selected register. Thus, the Read/Write signal is used to select the Read Only or Write Only registers within the ACIA.

(8) (10) (9)	CS_0 $\overline{CS_1}$ $\overline{CS_2}$	**Chip Select Signals**—These three high impedance TTL compatible input lines are used to address an ACIA. A particular ACIA is selected when CS_0 and CS_1 are high and $\overline{CS_2}$ is low. Transfers of data to and from ACIA are then performed under the control of Enable, Read/Write, and Register Select.
(11)	RS	**Register Select Signal**—The Register Select line is a high impedance input that is TTL compatible and is used to select the Transmit/Receive Data or Control/Status registers in the ACIA. The Read/Write signal line is used in conjunction with Register Select to select the Read Only or Write Only register in each register pair.
(7)	$\overline{IRQ}$	**Interrupt Request Signal**—Interrupt request is a TTL compatible, open drain active low output that is used to interrupt the MPU. The Interrupt Request remains low as long as the cause of the interrupt is present and the appropriate interrupt enable within the ACIA is set.

ACIA/Modem or Peripheral Interface

Pin	Label	Function
(4)	CTX	**Transmit Clock**—The Transmit Clock is a high impedance TTL compatible input used for the clocking of transmitted data. The transmitter initiates data on the negative transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(3)	CRX	**Receive Clock**—The Receive Clock is a high impedance TTL compatible input used for synchronization of received data. (In the ÷ 1 mode, the clock and data must be synchronized externally.) The receiver strobes the data on the positive transition of the clock. Clock frequency of 1, 16, or 64 times the data rate may be selected.
(2)	RXD	**Received Data**—The Received Data line is a high impedance TTL compatible input through which data is received in a serial NRX (Non Return to Zero) format. Synchronization with a clock for detection of data is accomplished internally when clock rates of 16 or 64 times the bit rate are used. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.

Pin	Label	Function
(6)	TXD	**Transmit Data**—The Transmit Data output line transfers serial NRZ data to a modem or other peripheral device. Data rates are in the range of 0 to 500Kbps when external synchronization is utilized.
(24)	$\overline{CTS}$	**Clear-to-Send**—This high impedance TTL compatible input provides automatic control of the transmitting end of a communications link via the modem's "clear-to-send" active low output by inhibiting the Transmitter Data Register Empty status bit (TDRE).
(5)	$\overline{RTS}$	**Request-to-Send**—The Request-to-Send output enables the MPU to control a peripheral or modem via the data bus. The active state is low. The Request-to-Send output is controlled by the contents of the ACIA control register.
(23)	$\overline{DCD}$	**Data Carrier Detected**—This high impedance TTL compatible input provides automatic control of the receiving end of a communications link by means of the modem "Data-Carrier-Detect" or "Received-Line-Signal Detect" output. The $\overline{DCD}$ input inhibits and initializes the receiver section of the ACIA when high. A low to high transition of the Data Carrier Detect initiates an interrupt to the MPU to indicate the occurrence of a loss of carrier when the Receiver Interrupt Enable (RIE) is set.
(12)	V_{CC}	+5 volts ±5%
(1)	GND	Ground

AMERICAN MICROSYSTEMS, INC.

S6852/S68A52/S68B52

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

Features

- ☐ Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- ☐ Character Synchronization on One or Two Sync Codes
- ☐ External Synchronization Available for Parallel-Serial Operation
- ☐ Programmable Sync Code Register
- ☐ Up to 600kbps Transmission
- ☐ Peripheral/Modem Control Functions
- ☐ Three Bytes of FIFO Buffering on Both Transmit and Receive
- ☐ Seven, Eight, or Nine Bit Transmission
- ☐ Optional Even and Odd Parity
- ☐ Parity, Overrun, and Underflow Status
- ☐ **Clock Rates:**
  1.0MHz
  1.5MHz
  2.0MHz

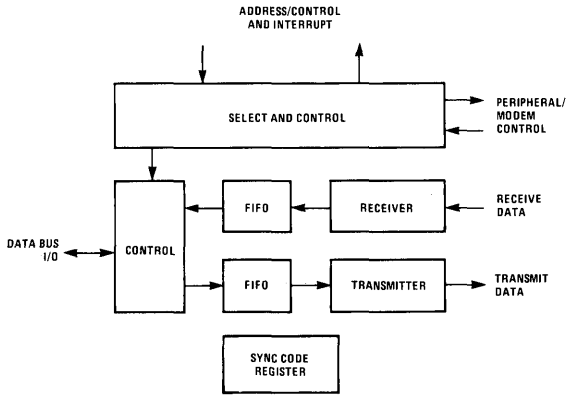
General Description

The S6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the S6800 Microprocessor systems.

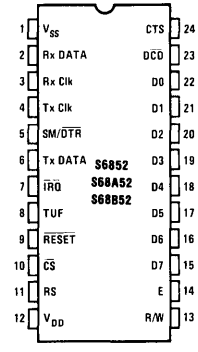
The bus interface of the S6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	−0.3 to +7.0
Input Voltage	−0.3 to +7.0V
Operating Temperature Range	0° to +70°C
Storage Temperature Range	−55° to +150°C
Thermal Resistance	+70°C/W

Note:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage		V_{SS}+2.0			Vdc
V_{IL}	Input Low Voltage				V_{SS}+0.8	Vdc
I_{IN}	Input Leakage Current (V_{IN}=0 to 5.25Vdc)	TxClk, Rx Clk, Rx Data, Enable Reset, RS, R/$\overline{W}$, $\overline{CS}$, $\overline{DCD}$, $\overline{CTS}$		1.0	2.5	μAdc
I_{TSI}	Three State (Off State) Input Current (V_{IN}=0.4 to 2.4Vdc, V_{CC}=5.25Vdc)	D0-D7		2.0	10	μAdc
V_{OH}	Output High Voltage I_{LOAD}=−205μAdc, Enable Pulse Width < 25μs I_{LOAD}=−100μAdc, Enable Pulse Width < 25μs	D0-D7 Tx Data, $\overline{DTR}$, TUF	 V_{SS}+2.4 V_{SS}+2.4			Vdc Vdc
V_{OL}	Output Low Voltage I_{LOAD}=1.6mAdc, Enable Pulse Width < 25μs				V_{SS}+0.4	Vdc
I_{LOH}	Output Leakage Current (Off State) V_{OH}=2.4Vdc	$\overline{IRQ}$		1.0	10	μAdc
P_D	Power Dissipation			300	525	mW
C_{IN}	Input Capacitance (V_{IN}=0, T_A=25°C, f=1.0MHz)	D0-D7 All Other Inputs			 12.5 7.5	pF
C_{OUT}	Output Capacitance (V_{IN}=0, T_A=25°C, f=1.0MHz)	Tx Data, SM/$\overline{DTR}$, TUF $\overline{IRQ}$			10 5.0	pF

Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C unless otherwise noted.)

		S6852		S68A52		S68B52		
Symbol	Characteristic	Min.	Max.	Min.	Max.	Min.	Max.	Unit
PW_{CL}	Minimum Clock Pulse Width, Low (Figure 1)	700		400		280		ns
PW_{CH}	Minimum Clock Pulse Width, High (Figure 2)	700		400		280		ns
f_C	Clock Frequency		600		1000		1500	kHz
t_{RDSU}	Receive Data Setup Time (Figure 3, 7)	350		200		160		ns
t_{RDH}	Receive Data Hold Time (Figure 3)	350		200		160		ns
t_{SM}	Sync Match Delay Time (Figure 3)		1.0		0.666		0.500	μs
t_{TDD}	Clock-to-Data Delay for Transmitter (Figure 4)		1.0		0.666		0.500	μs

*10μs or 10% of the pulse width, whichever is smaller.

Figure 1. Clock Pulse Width, Low-State

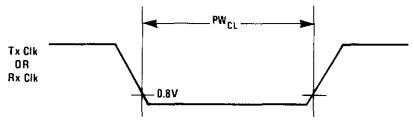
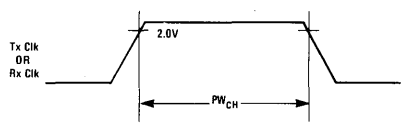


Figure 2. Clock Pulse Width, High-State



Electrical Characteristics-Continued (V_{CC} = 5.0V ± 5%, T_A = 0 to 70°C unless otherwise noted.)

Symbol	Characteristic	S6852 Min.	S6852 Max.	S68A52 Min.	S68A52 Max.	S68B52 Min.	S68B52 Max.	Unit
t_{TUF}	Transmitter Underflow (Figure 4, 6)		1.0		0.666		0.500	μs
t_{DTR}	$\overline{DTR}$ Delay Time (Figure 5)		1.0		0.666		0.500	μs
t_{IR}	$\overline{Interrupt\ Request}$ Release Time (Figure 5)		1.2		0.800		0.600	μs
t_{Res}	$\overline{Reset}$ Minimum Pulse Width	1.0		0.666		0.500		μs
t_{CTS}	$\overline{CTS}$ Setup Time (Figure 6)	200		150		120		ns
t_{DCD}	$\overline{DCD}$ Setup Time (Figure 7)	500		350		250		ns
t_r, t_f	Input Rise and Fall Times (except Enable) (0.8V to 2.0V)		1.0		1.0		1.0	μs

Bus Timing Characteristics

Symbol	Characteristic	S6852 Min.	S6852 Max.	S68A52 Min.	S68A52 Max.	S68B52 Min.	S68B52 Max.	Unit
Read								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		μs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns
Write								
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.5		μs
PW_{EH}	Enable Pulse Width, High	0.45	25	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Figure 3. Receive Data Setup and Hold Times and Sync Delay Time

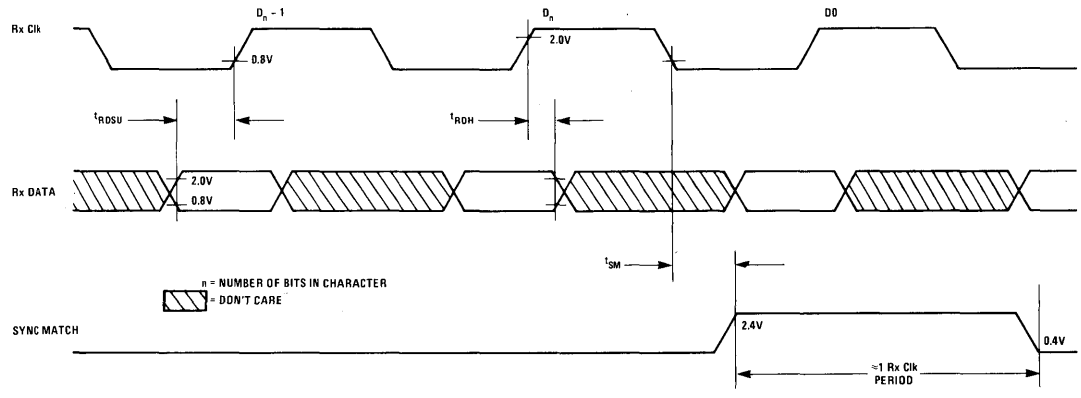


Figure 4. Transmit Data Output Delay and Transmitter Underflow Delay Time

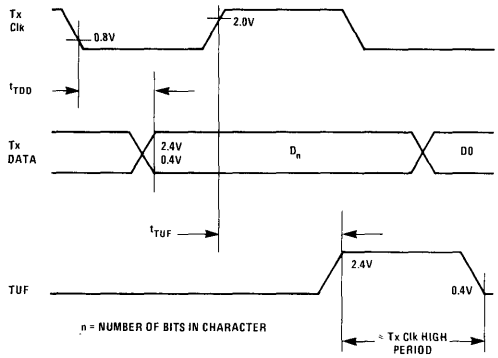


Figure 5. Data Terminal Ready and Interrupt Request Release Times

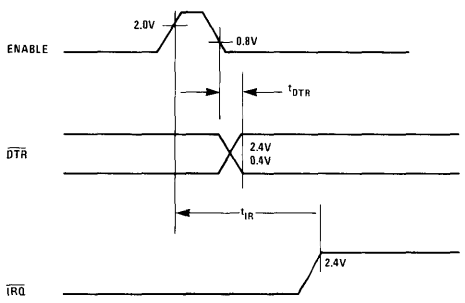


Figure 6. Clear-To-Send Setup Time

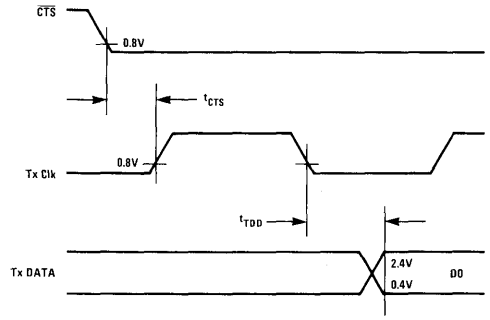


Figure 7. Data Carrier Detect Setup Time

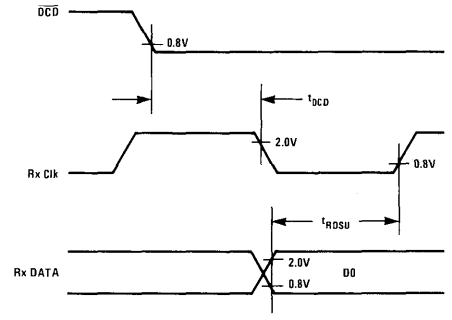


Figure 8. Bus Read Timing Characteristics (Read Information from SSDA)

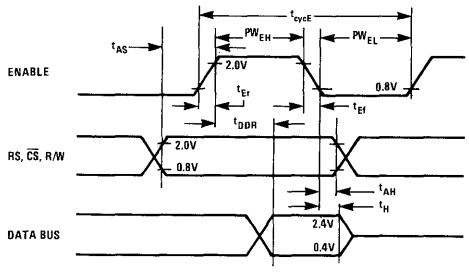
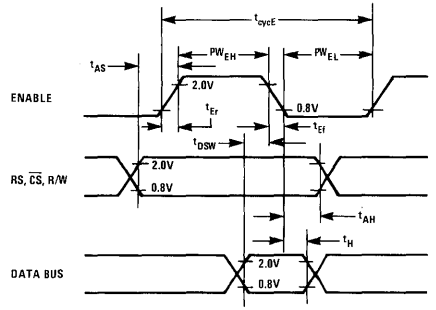
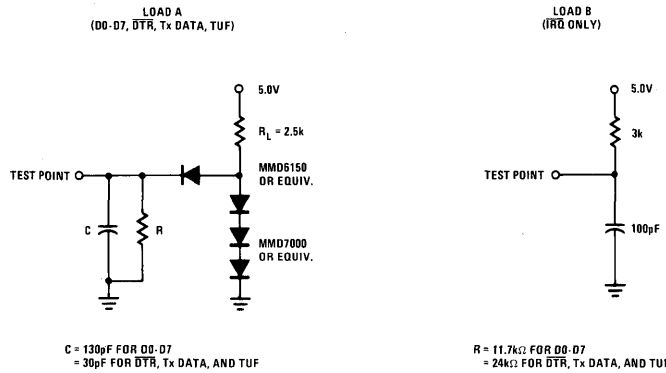


Figure 9. Bus Write Timing Characteristics (Write Information into SSDA)

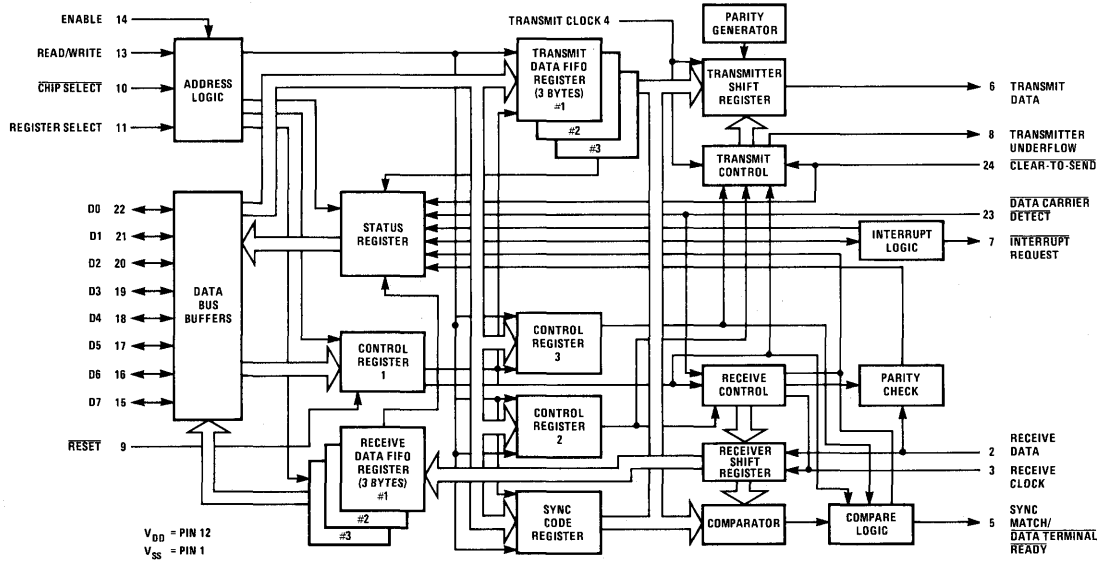


S6800

Figure 10. Bus Timing Test Loads



Expanded Block Diagram



Device Operation

At the bus interface, the SSDA appears as two addressable memory locations. Internally, there are seven registers: two read-only and five write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control 1, Control 2, Control 3, Sync Code and Transmit Data. The serial interface consists of serial input and output lines with independent clocks, and four peripheral/modem control lines.

Data to be transmitted is transferred directly into the 3-byte Transmit Data First-In First-Out (FIFO) Register from the data bus. Availability of the input to the FIFO is indicated by a bit in the Status Register; once data is entered, it moves through the FIFO to the last empty location. Data at the output of the FIFO is automatically transferred from the FIFO to the Transmitter Shift Register as the shift register becomes available to transmit the next character. If data is not available from the FIFO (underflow condition), the Transmitter Shift Register is automatically loaded with either a sync code or an all "1"s character. The transmit section may be programmed to append loaded with either a sync code or an all "1"s character. The transmit section may be programmed to append even, odd, or no parity to the transmitted word. An external control line ($\overline{\text{Clear-to-Send}}$) is provided to inhibit the transmitter without clearing the FIFO.

Serial data is accumulated in the receiver based on the synchronization mode selected. In the external sync mode, used for parallel-serial operation, the receiver is synchronized by the $\overline{\text{DCD}}$ ($\overline{\text{Data Carrier Detect}}$) input and transfers successive bytes of data to the input of the Receiver FIFO. The single-sync-character mode requires that a match occur between the Sync Code Register and one incoming character before data transfer to the FIFO begins. The two-sync-character mode requires that two sync codes be received in sequence to establish synchronization. Subsequent to synchronization in any mode, data is accumulated in the shift register, and parity is optionally checked. An indication of parity error is carried through the Receiver FIFO with each character to the last empty location. Availability of a word at the FIFO output is indicated by a bit in the Status Register, as is a parity error.

The SSDA and its internal registers are selected by the address bus, Read/Write (R/W) and Enable control lines. To configure the SSDA, Control Registers are selected and the appropriate bits set. The Status Register is addressable for reading status.

Other I/O lines, in addition to $\overline{\text{Clear-to-Send}}$ ($\overline{\text{CTS}}$) and $\overline{\text{Data Carrier Detect}}$ ($\overline{\text{DCD}}$), include SM/$\overline{\text{DTR}}$ (Sync Match/$\overline{\text{Data Terminal Ready}}$) and Transmitter Underflow (TUF). The transmitter and receiver each have individual clock inputs allowing simultaneous operation under separate clock control. Signals to the microprocessor are the Data bus and $\overline{\text{Interrupt}}$ Request ($\overline{\text{IRQ}}$).

Initialization

During a power-on sequence, the SSDA is reset via the $\overline{\text{Reset}}$ input and internally latched in a reset condition to prevent erroneous output transitions. The Sync Code Register, Control Register 2, and Control Register 3 should be programmed prior to the programmed release of the Transmitter and/or Receiver Reset bits; these bits in Control Register 1 should be cleared after the Reset line has gone high.

Transmitter Operation

Data is transferred to the transmitter section in parallel form by means of the data bus and Transmit Data FIFO. The Transmit Data FIFO is a 3-byte register whose status is indicated by the Transmitter Data Register Available status bit (TDRA) and its associated interrupt enable bit. Data is transferred through the FIFO on Enable (E) pulses. Two data transfer modes are provided in the SSDA. The 1-byte transfer mode provides for writing data to the transmitter section (and reading from the receiver section) one byte at a time. The 2-byte transfer mode provides for writing two data characters in succession.

Data will automatically transfer from the last register location in the Transmit Data FIFO (when it contains data) to the Transmitter Shift Register during the last half of the last bit of the previous character. A character is transferred into the Shift Register by the Transmitter Clock. Data is transmitted *LSB first*, and odd or even parity can be optionally appended. The unused bit positions in short word length characters from the data bus are "don't cares." (Note: The data bus inputs may be reversed for applications requiring the MSB to be transferred first, e.g., IBM format for floppy disks; however, care must be taken to properly program the control registers — Table 1 will have its bit positions reversed.)

When the Shift Register becomes empty and data is *not* available for transfer from the Transmit Data FIFO, an "underflow" occurs, and a character is inserted into the transmitter data stream to maintain

character synchronization. The character transmitted on underflow will be either a "Mark" (all "1"s) or the contents of the Sync Code Register, depending upon the state of the Transmit Sync Code on Underflow control bit. The underflow condition is indicated by a pulse (≈1 Tx Clk high period) on the Underflow output (when in Tx Sync on underflow mode). The Underflow output occurs coincident with the transfer of the last half of the last bit preceding the underflow character. The Underflow status bit is set until cleared by means of the Clear Underflow control bit. This output may be used in floppy disk systems to synchronize write operations and for appending CRCC.

Transmission is initiated by clearing the Transmitter Reset bit in Control Register 1. When the Transmitter Reset bit is cleared, the first *full* positive half-cycle of the Transmit Clock will initiate the transmit cycle, with the transmission of data or underflow characters beginning on the negative edge of the Transmit Clock pulse which started the cycle. If the Transmit Data FIFO was not loaded, an underflow character will be transmitted (see Figure 4).

The Clear-to-Send ($\overline{CTS}$) input provides for automatic control of the transmitter by means of external system hardware; e.g., the modem $\overline{CTS}$ output provides the control in a data communications system. The $\overline{CTS}$ input resets and inhibits the transmitter section when high, but does not reset the Transmit Data FIFO. The TDRA status bit is inhibited by $\overline{CTS}$ being high in either the one-sync-character or two-sync-character mode of operation. In the external sync mode, TDRA is unaffected by $\overline{CTS}$ in order to provide Transmit Data FIFO status for preloading and operating the transmitter under the control of the $\overline{CTS}$ input. When the Transmitter Reset bit (Tx Rx) is set, the Transmit Data FIFO becomes available for new data with TDRA inhibited.

Receiver Operation

Data and a presynchronized clock are provided to the SSDA receiver section by means of the Receive Data (Rx Data) and Receive Clock (Rx Clk) inputs. The data is a continuous stream of binary data bits without means for identifying character boundaries within the stream. It is, therefore, necessary to achieve character synchronization for the data at the *beginning* of the data block. Once synchronization is achieved, it is assumed to be retained for all successive characters within the block.

Data communications systems utilize the detection of sync codes during the initial portion of the preamble to establish character synchronization. This requires the detection of a single code or two successive sync codes. Floppy disk and cartridge tape units require sixteen bits of defined preamble and cassettes require eight bits of preamble to establish the reference for the start of record. All three are functionally equivalent to the detection of sync codes. Systems which do not utilize code detection techniques require custom logic external to the SSDA for character synchronization and use of the parallel-to-serial (external sync) mode. (Note: The Receiver Shift Register is set to ones when reset.)

Synchronization

The SSDA provides three operating modes with respect to character synchronization: one-sync-character mode, two-sync-character mode, and external sync mode. The external sync mode requires synchronization and control of the receiving section through the Data Carrier Detect ($\overline{DCD}$) input (see Figure 7). This external synchronization could consist of direct line control from the transmitting end of the serial data link or from external logic designed to detect the start of the message block. The one-sync-character mode searches on a bit-by-bit basis until a match is achieved between the data in the Shift Register and the Sync Code Register. The match indicates character synchronization is complete and will be retained for the message block. In the two-sync-character mode, the receiver searches for the first sync code match on a bit-by-bit basis and then looks for a second *successive* sync code character prior to establishing character synchronization. If the second sync code character is not received, the bit-by-bit search for the first sync code is resumed.

Sync codes received prior to the completion of synchronization (one or two character) are not transferred to the Receive Data FIFO. Redundant sync codes during the preamble or sync codes which occur as "fill characters" can automatically be stripped from the data, when the Strip Sync control bit is set, to minimize system loading. The character synchronization will be retained until cleared by means of the Clear Sync bit, which also inhibits synchronization search when set.

Receiving Data

Once synchronization has been achieved, subsequent characters are automatically transferred into the Receive Data FIFO and clocked through the FIFO to the last empty location by E pulses (MPU System $\phi 2$).

The Receiver Data Available status bit (RDA) indicates when data is available to be read from the last FIFO location (#3) when in the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate data is available when the last two FIFO register locations are full. Data being available in the Receive Data FIFO causes an interrupt request if the Receiver Interrupt Enable (RIE) bit is set. The MPU will then read the SSDA Status Register, which will indicate that data is available for the MPU read from the Receive Data FIFO register. The IRQ and RDA status bits are reset by a read from the FIFO. If more than one character has been received and is resident in the Receive Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA and IRQ status bits will again be set. The read data operation for the 2-byte transfer mode requires an intervening E clock between reads to allow the FIFO data to shift. Optional parity is automatically checked as data is received, and the parity status condition is maintained with each character until the data is read from the Receive Data FIFO. Parity errors will cause an interrupt request if the Error Interrupt Enable (EIE) has been set. The parity bit is not transferred to the data bus but must be checked in the Status Register. NOTE: In the 2-byte transfer mode, parity should be checked prior to reading the second byte, since a FIFO read clears the error bit.

Other status bits which pertain to the receiver section are Receiver Overrun and Data Carrier Detect ($\overline{DCD}$). The Overrun status bit is automatically set when a transfer of a character to the Receive Data FIFO occurs and the first register of the Receive Data FIFO is full. Overrun causes an interrupt if Error Interrupt Enable (EIE) has been set. The transfer of the overrunning character into the FIFO causes the previous character in the FIFO input register location to be lost The Overrun status bit is cleared by reading the Status Register (when the overrun condition is present), followed by a Receive Data FIFO Register read. Overrun cannot occur and be cleared without providing an opportunity to detect its occurrence via the Status Register.

A positive transition on the $\overline{DCD}$ input causes an interrupt if the EIE control bit has been set. The interrupt caused by $\overline{DCD}$ is cleared by reading the Status Register when the $\overline{DCD}$ status bit is high, followed by a Receive Data FIFO read. The $\overline{DCD}$ status bit will subsequently follow the state of the $\overline{DCD}$ input when it goes low.

Input/Output Functions

SSDA Interface Signals for MPU

The SSDA interfaces to the S6800 MPU with an 8-bit bi-directional data bus, a chip select line, a register select line, an interrupt request line, read/write line, an enable line, and a reset line. These signals, in conjunction with the S6800 VMA output, permit the MPU to have complete control over the SSDA.

SSDA Bi-Directional Data (D0-D7)—The bi-directional data lines (D0-D7) allow for data transfer between the SSDA and the MPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs an SSDA read operation.

SSDA Enable (E) — The Enable signal, E, is a high impedance TTL compatible input that enables the bus input/output data buffers, clocks data to and from the SSDA, and moves data through the FIFO Registers. This signal is normally the continuous S6800 System $\phi 2$ clock, so that incoming data characters are shifted through the FIFO.

Read/Write (R/W) — The Read/Write line is a high impedance input that is TTL compatible and is used to control the direction of data flow through the SSDA's input/output data bus interface. When Read/Write is high (MPU read cycle), SSDA output drivers are turned on if the chip is selected and a selected register is read. When it is low, the SSDA output drivers are turned off and the MPU writes into a selected register. The Read/Write signal is also used to select read-only or write-only registers within the SSDA.

Chip Select ($\overline{CS}$) — This high impedance TTL compatible input line is used to address the SSDA. The SSDA is selected when $\overline{CS}$ is low. VMA should be used in generating the $\overline{CS}$ input to insure that false selects will not occur. Transfers of data to and from the SSDA are then performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS) — The Register Select line is a high impedance input that is TTL compatible. A high level is used to select Control Registers C2 and C3, the Sync Code Register, and the Transmit/Receive Data Registers. A low level selects the Control 1 and Status Registers (see Table 1).

Table 1. SSDA Programming Model

REGISTER	CONTROL INPUTS		ADDRESS CONTROL		REGISTER CONTENT							
	RS	R/W	AC2	AC1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS (S)	0	1	X	X	INTERRUPT REQUEST (IRQ)	RECEIVER PARITY ERROR (PE)	RECEIVER OVERRUN (Rx Ovrn)	TRANS-MITTER UNDERFLOW (TUF)	CLEAR-TO-SEND ($\overline{CTS}$)	DATA CARRIER DETECT ($\overline{DCD}$)	TRANS-MITTER DATA REGISTER AVAILABLE (TDRA)	RECEIVER DATA AVAILABLE (RDA)
CONTROL 1 (C1)	0	0	X	X	ADDRESS CONTROL 2 (AC2)	ADDRESS CONTROL 1 (AC1)	RECEIVER INTERRUPT ENABLE (RIE)	TRANS-MITTER INTERRUPT ENABLE (TIE)	CLEAR SYNC	STRIP SYNC CHARACTERS (STRIP SYNC)	TRANS-MITTER RESET (Tx Rs)	RECEIVER RESET (Rx Rs)
RECEIVE DATA FIFO	1	1	X	X	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL 2 (C2)	1	0	0	0	ERROR INTERRUPT ENABLE (EIE)	TRANSMIT SYNC CODE ON UNDERFLOW (Tx Sync)	WORD LENGTH SELECT 3 (WS3)	WORD LENGTH SELECT 2 (WS2)	WORD LENGTH SELECT 1 (WS1)	1-BYTE/ 2-BYTE TRANSFER (1-BYTE/ 2-BYTE)	PERIPHERAL CONTROL 2 (PC2)	PERIPHERAL CONTROL 1 (PC1)
CONTROL 3 (C3)	1	0	0	1	NOT USED	NOT USED	NOT USED	NOT USED	CLEAR TRANS-MITTER UNDERFLOW STATUS (CTUF)	CLEAR $\overline{CTS}$ STATUS (CLEAR $\overline{CTS}$)	ONE-SYNC-CHARACTER/ TWO-SYNC-CHARACTER MODE CONTROL (1 Sync/ 2 Sync)	EXTERNAL/ INTERNAL SYNC MODE CONTROL (E/I Sync)
SYNC CODE	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
TRANSMIT DATA FIFO	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

X = DON'T CARE

Status Register

IRQ Bit 7 — The IRQ flag is cleared when the source of the IRQ is cleared. The source is determined by the enables in the Control Registers: TIE, RIE, EIE.

Bits 6-0 — indicate the SSDA status at a point in time, and can be *reset* as follows:

PE — Bit 6 — Read Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

Rx Ovrn — Bit 5 — Read Status and then Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

TUF — Bit 4 — A "1" into CTUF (C3 Bit 3) or into Tx Rs (C1 Bit 1).

$\overline{CTS}$ — Bit 3 — A "1" into Clear $\overline{CTS}$ (C3 Bit 2) or a "1" into Tx Rs (C1 Bit 1)

$\overline{DCD}$ — Bit 2 — Read Status and then Rx Data FIFO or a "1" into Rx Rs (C1 Bit 0)

TDRA — Bit 1 — Write into Tx Data FIFO.

RDA — Bit 0 — Read Rx Data FIFO.

Control Register 1

AC2, AC1 — Bits 7, 6 — Used to access other registers, as shown above.

RIE — Bit 5 — When "1", enables interrupt on RDA (S Bit 0).

TIE — Bit 4 — When "1", enables interrupt on TDRA (S Bit 1).

Clear Sync — Bit 3 — When "1", clears receiver character synchronization.

Strip Sync — Bit 2 — When "1", strips all sync codes from the received data stream.

Tx Rs — Bit 1 — When "1", resets and inhibits the transmitter section.

Rx Rs — Bit 0 — When "1", resets and inhibits the receiver section.

Control Register 3

CTUF — Bit 3 — When "1", clears TUF (S Bit 4), and IRQ if enabled.

Clear $\overline{CTS}$ — Bit 2 — When "1", clears $\overline{CTS}$ (S Bit 3), and IRQ if enabled.

1 Sync/2 Sync — Bit 1 — When "1", selects the one-sync-character mode; when "0", selects the two-sync-character mode.

E/I Sync — Bit 0 — When "1", selects the external sync mode; when "0", selects the internal sync mode.

Control Register 2

EIE — Bit 7 — When "1", enables the PE, Rx Ovrn, TUF, $\overline{CTS}$, and $\overline{DCD}$ interrupt flags (S Bits 6 through 2).

Tx Sync — Bit 6 — When "1", allows sync code contents to be transferred on underflow, and enables the TUF Status bit and output. When "0", an all mark character is transmitted on underflow.

WS3, 2, 1 — Bits 5-3 Word Length Select

BIT 5 WS3	BIT 4 WS2	BIT 3 WS1	WORD LENGTH
0	0	0	6 BITS + EVEN PARITY
0	0	1	6 BITS + ODD PARITY
0	1	0	7 BITS
0	1	1	8 BITS
1	0	0	7 BITS + EVEN PARITY
1	0	1	7 BITS + ODD PARITY
1	1	0	8 BITS + EVEN PARITY
1	1	1	8 BITS + ODD PARITY

1-Byte/2-Byte — Bit 2 — When "1", enables the TDRA and RDA bits to indicate when a 1-byte transfer can occur; when "0", the TDRA and RDA bits indicate when a 2-byte transfer can occur.

PC2, PC1 — Bits 1-0 — SM/$\overline{DTR}$ Output Control

BIT 1 PC2	BIT 0 PC1	SM/$\overline{DTR}$ OUTPUT AT PIN 5
0	0	1
0	1	PULSE ⎍ 1-BIT WIDE ON SM
1	0	0
1	1	SM INHIBITED, 0

Note: When the SSDA is used in applications requiring the MSB of data to be received and transmitted first, the data bus inputs to the SSDA may be reversed (D0 to D7, etc.) Caution must be used when this is done since the bit positions in this table will be reversed, and the parity should not be selected.

Interrupt Request ($\overline{IRQ}$) — $\overline{Interrupt\ Request}$ is a TTL compatible, open-drain (no internal pullup), active low output that is used to interrupt the MPU. The $\overline{Interrupt\ Request}$ remains low until cleared by the MPU.

$\overline{Reset}$ Input — The $\overline{Reset}$ input provides a means of resetting the SSDA from an external source. In the low state, the $\overline{Reset}$ input causes the following:

1. Receiver Reset (Rx Rs) and Transmitter Reset (Tx Rs) bits are set causing both the receiver and transmitter sections to be held in a reset condition.
2. Peripheral Control bits PC1 and PC2 are reset to zero, causing the SM/$\overline{DTR}$ output to be high.
3. The Error Interrupt Enable (EIE) bit is reset.
4. An internal synchronization mode is selected.
5. The Transmitter Data Register Available (TDRA) status bit is cleared and inhibited.

When $\overline{Reset}$ returns high (the inactive state), the transmitter and receiver sections will remain in the reset state until the Receiver Reset and Transmitter Reset bits are cleared via the bus under software control. The control Register bits affected by $\overline{Reset}$ (Rx Rs, Tx Rs, PC1, PC2, EIE, and E/I Sync) cannot be changed when $\overline{Reset}$ is low.

Clock Inputs

Separate high impedance TTL compatible inputs are provided for clocking of transmitted and received data.

Transmit Clock (Tx Clk) — The Transmit Clock input is used for the clocking of transmitted data. The transmitter shifts data on the negative transition of the clock.

Receive Clock (Rx Clk) — The Receive Clock input is used for clocking in received data. The clock and data must be synchronized externally. The receiver samples the data on the positive transition of the clock.

Serial Input/Output Lines

Receive Data (Rx Data) — The Receive Data line is a high impedance TTL compatible input through which data is received in a serial format. Data rates are from 0 to 600 kbps.

Transmit Data (Tx Data) — The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates are from 0 to 600 kbps.

Peripheral/Modem Control

The SSDA includes several functions that permit limited control of a peripheral or modem. The functions included are $\overline{Clear\text{-}to\text{-}Send}$, Sync Match/$\overline{Data}$

Terminal Ready, Data Carrier Detect, and Transmitter Underflow.

Clear-to-Send ($\overline{CTS}$) — The $\overline{CTS}$ input provides a real-time inhibit to the transmitter section (the Tx Data FIFO is not disturbed). A positive $\overline{CTS}$ transition resets the Tx Shift Register and inhibits the TDRA status bit and its associated interrupt in both the one-sync-character and two-sync-character modes of operation. TDRA is not affected by the $\overline{CTS}$ input in the external sync mode.

The positive transition of $\overline{CTS}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{CTS}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by writing a "1" in the Clear $\overline{CTS}$ bit in Control Register 3 or in the Transmitter Reset bit. The $\overline{CTS}$ status bit subsequently follows the $\overline{CTS}$ input when it goes low.

The $\overline{CTS}$ input provides character timing for transmitter data when in the external sync mode. Transmission is initiated on the negative transition of the first *full* positive clock pulse of the transmitter clock (Tx Clk) after the release of $\overline{CTS}$ (see Figure 6).

Data Carrier Detect ($\overline{DCD}$) — The $\overline{DCD}$ input provides a real-time inhibit to the receiver section (the Rx FIFO is not disturbed). A positive $\overline{DCD}$ transition resets and inhibits the receiver section except for the Receive FIFO and the RDRA status bit and its associated $\overline{IRQ}$.

The positive transition of $\overline{DCD}$ is stored within the SSDA to insure that its occurrence will be acknowledged by the system. The stored $\overline{DCD}$ information and its associated $\overline{IRQ}$ (if enabled) are cleared by reading the Status Register and then the Receiver FIFO, or by writing a "1" into the Receiver Reset bit. The $\overline{DCD}$ status bit subsequently follows the $\overline{DCD}$ input when it goes low. The $\overline{DCD}$ input provides character synchronization timing for the receiver during the external sync mode of operation. The receiver will be initialized and data will be sampled on the positive transition of the first *full* Receive Clock cycle after release of $\overline{DCD}$ (see Figure 7).

Sync Match/Data Terminal Ready (SM/$\overline{DTR}$) — The SM/DTR output provides four functions (see Table 1) depending on the state of the PC1 and PC2 control bits. When the Sync Match mode is selected (PC1 = "1", PC2 = "0"), the output provides a one-bit-wide pulse when a sync code is detected. The SM output is inhibited when PC2 = "1". The $\overline{DTR}$ mode (PC1 = "0") provides an output level corresponding to the complement of PC2 ($\overline{DTR}$ = "0" when PC2 = "1"). (See Table 1.)

Transmitter Underflow (TUF) — The Underflow output indicates the occurrence of a transfer of a "fill character" to the Transmitter Shift Register when the last location (#3) in the Transmit Data FIFO is empty. The Underflow output pulse is approximately a Tx Clk high period wide and occurs during the last half of the last bit of the character preceding the "Underflow" (see Figure 4). The Underflow output does not respond to underflow conditions when the Tx Sync bit is in the reset state.

ADVANCED DATA LINK CONTROLLER

Features

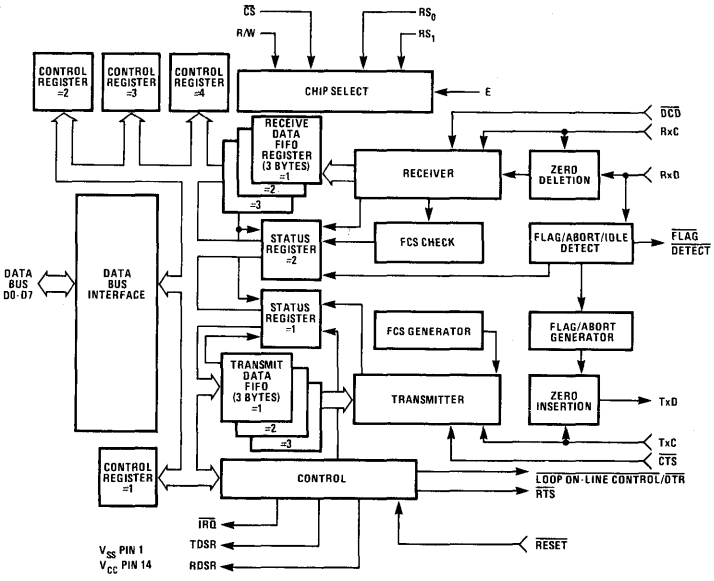
- ☐ S6800 Compatible
- ☐ Protocol Features
  - ☐ Automatic Flag Detection and Synchronization
  - ☐ Zero Insertion and Deletion
  - ☐ Extendable Address, Control and Logical Control Fields (Optional)
  - ☐ Variable Word Length Info Field — 5, 6, 7, or 8-bits
  - ☐ Automatic Frame Check Sequence Generation and Check
  - ☐ Abort Detection and Transmission
  - ☐ Idle Detection and Transmission
- ☐ Loop Mode Operation
- ☐ Loop Back Self-Test Mode
- ☐ NRZ/NRZI Modes
- ☐ Quad Data Buffers for Each Rx and Tx
- ☐ Prioritized Status Register (Optional)
- ☐ MODEM/DMA/Loop Interface

General Description

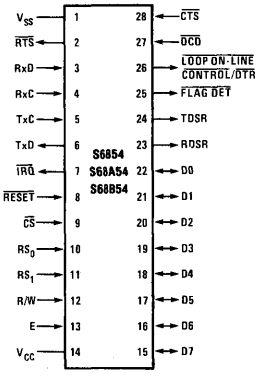
The S6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP), High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

S6800

Block Diagram



Pin Configuration



Absolute Maximum Ratings*

Supply Voltage	−0.3 to +7.0V
Input Voltage	−0.3 to +7.0V
Operating Temperature Range	0° to +70°C
Storage Temperature Range	−55° to +150°C
Thermal Resistance	70°C/W

*This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0		Vdc		
V_{IL}	Input Low Voltage			V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current All Inputs Except D0−D7		1.0	2.5	μAdc	V_{IN}=0 to 5.25 Vdc
I_{TSI}	Three State (Off State) Input Current D0−D7		2.0	10	μAdc	V_{IN}=0.4 to 2.4Vdc V_{CC}=5.25Vdc
V_{OH}	Output High Voltage D0-D7 All Others	 V_{SS}+2.4 V_{SS}+2.4			 Vdc Vdc	 I_{LOAD}=−205μAdc I_{LOAD}=−100μAdc
V_{OL}	Output Low Voltage			V_{SS}+0.4	Vdc	I_{LOAD}=1.6mAdc
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH}=2.4Vdc
P_D	Power Dissipation			850	mW	
C_{IN}	Capacitance D0-D7 All Other Inputs			12.5 7.5	pF pF	V_{IN}=0, T_A=+25°C, f=1.0MHz
C_{OUT}	$\overline{IRQ}$ All Others			5.0 10	pF pF	

Symbol	Characteristic	S6854 Min.	S6854 Max.	S68A54 Min.	S68A54 Max.	S68B54 Min.	S68B54 Max.	Unit
PW_{CL}	Minimum Clock Pulse Width, Low	700		450		280		ns
PW_{CH}	Minimum Clock Pulse Width, High	700		450		280		ns
f_C	Clock Frequency		0.66		1.0		1.5	MHz
t_{RDSU}	Receive Data Setup Time	250		200		120		ns
t_{RDH}	Receive Data Hold Time	120		100		60		ns
t_{RTS}	Request-to-Send Delay Time		680		460		340	ns
t_{TDD}	Clock-to-Data Delay for Transmitter		460		320		250	ns
t_{FD}	Flag Detect Delay Time		680		460		340	ns
t_{DTR}	DTR Delay Time		680		460		340	ns
t_{LOC}	Loop On-Line Control Delay Time		680		460		340	ns
t_{RDSR}	RDSR Delay Time		540		400		340	ns
t_{TDSR}	TDSR Delay Time		540		400		340	ns
t_{IR}	Interrupt Request Release Time		1.2		0.9		0.7	μs
t_{RES}	Reset Minimum Pulse Width	1.0		0.65		0.40		μs
t_r, t_f	Input Rise and Fall Times except Enable (0.8V to 2.0V)		1.0*		1.0*		1.0*	μs

*1.0μs or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Read

Symbol	Characteristic	S6854		S68A54		S68B54		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Write

Symbol	Characteristic	S6850		S68A50		S68B50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYCE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

Figure 1. Bus Timing Test Loads

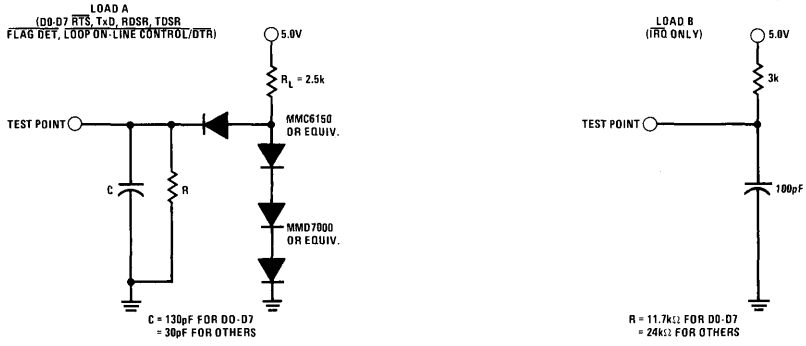


Figure 2. Receiver Data Setup/Hold, Flag Detect and Loop On-Line Control Delay Timing

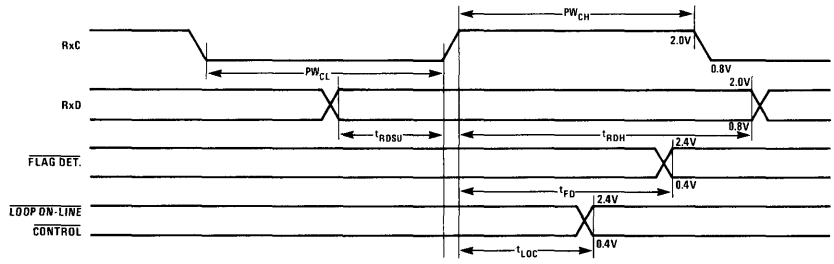


Figure 3. Transmit Data Output Delay and Request to Send Delay Timing

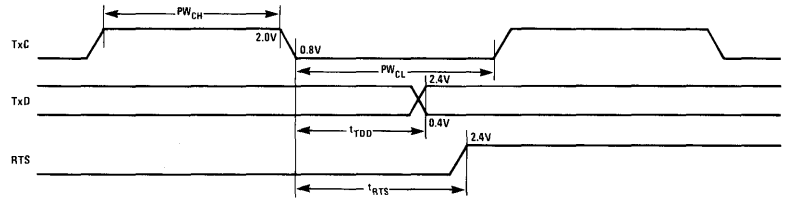


Figure 4. TDSR/RDSR Delays, IRQ Release Delay, RTS and DTR Delay Timing

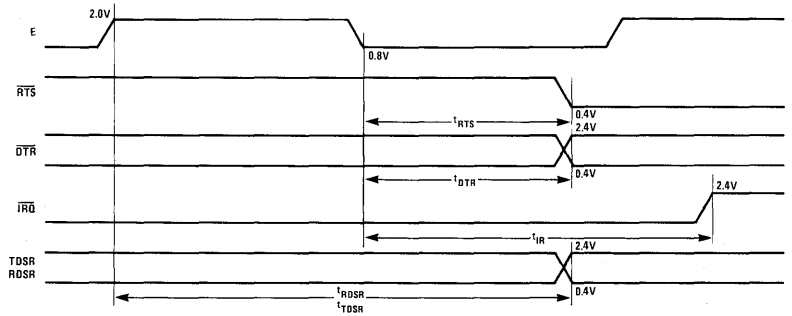
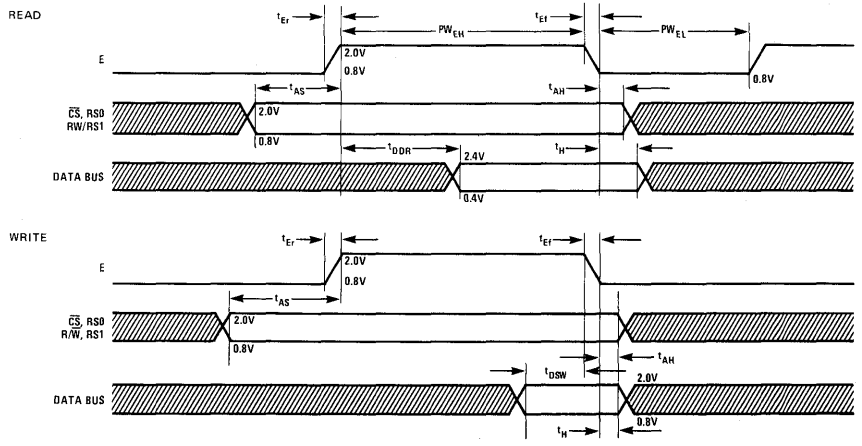


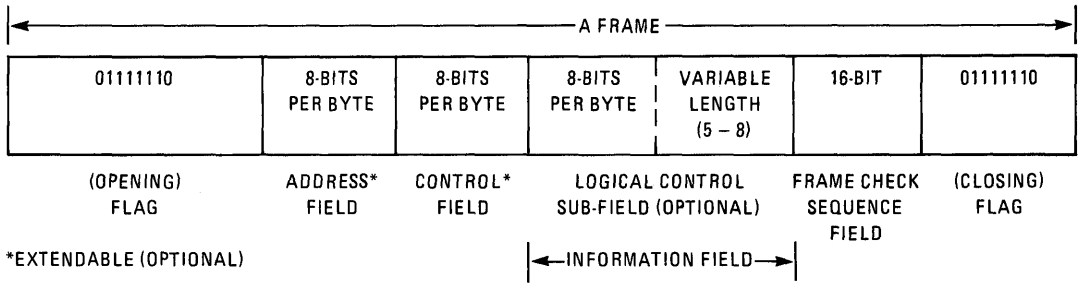
Figure 5. Bus Read/Write Timing Characteristics



Frame Format

The ADLC transmits and receives data (information or control) in a format called a frame. All frames start with an opening flag (F) and end with a closing flag (F). Between the opening flag and closing flag, a frame contains an address field, control field, information field, and frame check sequence field.

Figure 6. Data Format of a Frame



Flag (F) — The flag is the unique binary pattern (01111110). It provides the frame boundary and a reference for the position of each field of the frame.

The ADLC transmitter generates a flag pattern internally and the opening flag and closing flags are appended to a frame automatically. Two successive frames can share one flag for a closing flag of the first frame and for the opening flag of the next frame, if the "FF/F" control bit in the control register is reset.

The receiver searches for a flag on a bit by bit basis and recognizes a flag at any time. The receiver establishes the frame synchronization with every flag. The flags mark the frame boundary and reference for each field but they are not transferred to the Rx FIFO. The detection of a flag is indicated by the Flag Detect output and by a status bit in the status register.

Order of Bit Transmission — Address, control and information field bytes are transferred between the MPU and the ADLC in parallel by means of the data bus. The bit on D0 (data bus bit 0, pin 22) is serially transmitted first, and the first serially received bit is transferred to the MPU on D0. The FCS field is transmitted and receives MSB first.

Address (A) Field — The 8 bits following the opening flag are the address (A) field. The A-field can be extendable if the Auto-Address Extend Mode is selected in control register #3. In the Address Extend Mode, the first bit (bit 0) in every address octet becomes the extend control bit. When the bit is "0", the ADLC assumes another address octet will follow, and when the bit is "1", the address extension is terminated. A "null" address (all "0's") does not extend. In the receiver, the Address Present status bit distinguishes the address field from other fields. When an address byte is available to be read in the receive FIFO register, the Address Present status bit is set and causes an interrupt (if enabled). The Address Present bit is set for every address octet when the Address Extend Mode is used.

Control (C) Field — The 8 bits following the address field is the control (link control) field. When the Extended Control Field bit in control register #3 is selected, the C-field is extended to 16 bits.

Information (I) Field — The I-field follows the C-field and precedes the FCS field. The I-field contains "data" to be transferred but is not always necessarily contained in every frame. The word length of the I-field can be selected from 5 to 8 bits per byte by control bits in control register #4. The I-field will continue until it is terminated by the FCS and closing flag. The receiver has the capability to handle a "partial" last byte. The last information byte can be any word length between 1 and 8 bits. If the last byte in the I-field is less than the selected word length, the receiver will right justify the received bits, fill the remaining bits of the receiver shift register with zeros, and transfer a full byte to the Rx FIFO. Regardless of selected byte length, the ADLC will transfer 8 bits of data to the data bus. Unused bits for word lengths of 5, 6, and 7 will be zeroed.

Logical Control (LC) Field — When the Logical control Field Select bit in control register #3 is selected, the ADLC separates the I-field into two sub-fields. The first sub-field is the Logical Control field and the following sub-field is the "data" portion of the I-field. The logical control field is 8 bits and

follows the C-field, which is extendable by octets, if it is selected. The last bit (bit 7) is the extend control bit, and if it is a "1", the LC-field is extended one octet.

Note: Hereafter the word "Information Field" or "I-field" is used as the data portion of the information field, and excludes the logical control field. This is done in order to keep the consistency of the meaning of "Information Field" as specified in SDLC, HDLC, and ADCCP standards.

Frame Check Sequence (FCS) Field — The 16 bits preceding the closing flag is the FCS field. The FCS is the "cyclic redundancy check character (CRCC)". The poly-nomial $x^{16} + x^{12} + x^5 + 1$ is used both for the transmitter and receiver. Both the transmitter and receiver poly-nominal registers are initialized to all "1"s prior to calculation of the FCS. The transmitter calculates the FCS on all bits of the address, control, logical control (if selected), and information fields, and transmits the complement of the resulting remainder as FCS. The receiver performs the similar computation on all bits of the address, control, logical control (if selected), information, and received FCS fields and compares the result to F0B8 (Hexadecimal). When the result matches F0B8, the Frame Valid status bit is set in the status register. If the result does not match, the Error status bit is set. The FCS generation, transmission, and checking are performed automatically by the ADLC transmitter and receiver. The FCS field is not transferred to the Rx FIFO.

Invalid Frame — Any valid frames should have at least the A-field, C-field and FCS field between the opening flag and the closing flag. When invalid frames are received, the ADLC handles them as follows:

1) A short frame which has less than 25 bits between flags — The ADLC ignores the short frame and its reception is not reported to the MPU.
2) A frame less than 32 bits between the flags, or a frame 32 bits or more with an extended A-field or C-field that is not completed. — This frame is transferred into the Rx FIFO. The FCS/IF Error status bit indicates the reception of the invalid frame at the end of the frame.
3) Aborted Frame— The frame which is aborted by receiving an abort or DCD failure is also an invalid frame. Refer to "Abort" and "DCD status bit."

Zero Insertion and Zero Deletion — The Zero insertion and deletion, which allows the content of the frame to be transparent, are performed by the ADLC automatically. A binary 0 is inserted by the transmitter after any succession of 5 1's within a frame (A, C, LC, I, and FCS field). The receiver deletes a binary 0 that follows successive 5 continuous 1's within a frame.

Abort — The function of prematurely terminating a data link is called "abort". The transmitter aborts a frame by sending at least 8 consecutive 1's immediately after the Tx Abort control bit in control register #4 is set to a "1". (Tx FIFO is also cleared by the Tx Abort control bit at the same time.) The abort can be extended up to (at least) 16 consecutive 1's, if the Abort Extend control bit in the control register #4 is set when an abort is sent. This feature is useful to force mark idle transmission. Reception of 7 or more consecutive 1's is interpreted as an abort by the receiver. The receiver responds to a received abort as follows:

1) An abort in an "out of frame" condition — An abort during the idle or time fill has no meaning. The abort reception is indicated in the status register as long as the abort condition continues; but neither an interrupt nor a stored condition occurs. The abort indication is suppressed after 15 or more consecutive 1's are received (Received Idle status is set).
2) An abort "in frame" after less than 26 bits are received after an opening flag — Under this condition, any field of the aborted frame has not transferred to the MPU yet. The ADLC clears the aborted frame data in the FIFO and clears flag synchronization. Neither an interrupt nor a stored status occurs. The status indication is the same as (1) above.
3) An abort "in frame" after 26 bits or more are received after an opening flag — Under this condition, some fields of the aborted frame might have been transferred onto the data bus. The abort status is stored in the receiver status register and the data of the aborted frame in the ADLC is cleared. The synchronization is also cleared.

Idle and Time Fill — When the transmitter is in an "out of frame" condition (the transmitter is not transmitting a frame), it is in an idle state. Either a series of contiguous flags (time fill) or a mark idle

(consecutive 1's on a bit by bit basis) is selected for the transmission in an idle state by the Flag/Mark Idle control bit. When the receiver receives 15 or more consecutive 1's, the Receive Idle status bit is set and causes an interrupt. The flags and mark idle are not transferred to the Rx FIFO.

Operation

Initialization — During a power-on sequence, the ADLC is reset via the $\overline{\text{RESET}}$ input and internally latched in a reset condition to prevent erroneous output transitions. The four control registers must be programmed prior to the release of the reset condition. The release of the reset condition is performed via software by writing a "0" into the Rx RS control bit (receiver) and/or Tx RS control bit (transmitter). The release of the reset condition must be done after the $\overline{\text{RESET}}$ input has gone high.

At any time during operation, writing a "1" into the Rx RS control bit or TX RS control causes the reset condition of the receiver or the transmitter.

Transmitter Operation — The Tx FIFO register cannot be pre-loaded when the transmitter is in a reset state. After the reset release, the Flag/Mark Idle control bit selects either the mark idle state (inactive idle) or the Flag "time fill' (active idle) state.This active or inactive mark idle state will continue until data is loaded into the Tx FIFO.

The availability of the Tx FIFO is indicated by the TDRA status bit under the control of the 2-Byte/1-Byte control bit. TDRA status is inhibited by the Tx RS bit or $\overline{\text{CTS}}$ input being high. When the 1-Byte mode is selected, one byte of the FIFO is available for data transfer when TDRA goes high. When the 2-Byte mode is selected, two successive bytes can be transferred when TDRA goes high.

The first byte (Address field) should be written into the Tx FIFO at the "Frame Continue" address. Then the transmission of a frame automatically starts. If the transmitter is in a mark idle state, the transfer of an address causes an opening flag within two or three transmitter clock cycles. If the transmitter has been in a time fill state, the current time fill flag being transmitted is assumed as an opening flag and the address field will follow it.

A frame continues as long as data is written into the Tx FIFO at the "Frame Continue" address. The ADLC internally keeps track of the field sequence in the frame. The frame format is described in the "FRAME FORMAT" section.

The frame is terminated by one of two methods. The most efficient way to terminate the frames from a software standpoint is to write the last data character into the Transmit FIFO "Frame Terminate" address (RS1, RS0 = 11) rather than the Transmit FIFO "Frame Continue" address (RS1, RS0 = 10). An alternate method is to follow the last write of data in the Tx FIFO "Frame Continue" address with the setting of the Transmit Last Data control bit. Either method causes the last character to be transmitted and the FCS field to automatically be appended along with a closing flag. Data for a new frame can be loaded into the Tx FIFO immediately after the old frame data, if TDRA is high. The closing Flag can serve as the opening Flag of the next frame or separate opening and closing Flags may be transmitted. If a new frame is not ready to be transmitted, the ADLC will automatically transmit the Active (Flag) or Inactive (Mark) Idle condition.

If the Tx FIFO becomes empty at any time during frame transmission (the FIFO has no data to transfer into transmitter shift register during transmission of the last half of the next to last bit of a word), an underrun will occur and the transmitter automatically terminates the frame by transmitting an abort. The underrun state is indicated by the Tx Underrun status bit.

Any time the Tx ABORT Control bit is set, the transmitter immediately aborts the frame (transmits at least 8 consecutive 1's) and clears the Tx FIFO. If the abort Extend Control bit is set at the time, an idle (at least 16 consecutive 1's) is transmitted. An abort or idle in an "out of frame" condition can be useful to gain 8 or 16 bits of delay. (For an example, see "Programming Considerations.")

The $\overline{\text{CTS}}$ ($\overline{\text{Clear-To-Send}}$) input and $\overline{\text{RTS}}$ ($\overline{\text{Request-To-Send}}$) output are provided for a MODEM or other hardware interface.

The TDRA/FC status bit (when selected to be Frame Complete Status) can cause an interrupt upon frame completion (i.e., a flag or abort completion).

Details regarding the inputs and outputs, status bits, control bits, and FIFO operation are described in their respective sections.

Receiver Operation — Data and a pre-synchronized clock are provided to the ADLC receiver section by means of the Receive Data (RxD) and Receive Clock (RxC) inputs. The data is a continuous stream of binary bits with the characteristic that a maximum of five "1's" can occur in succession unless Abort, Flag,

Figure 7A. ADLC Transmitter State Diagram
C_1b_1 refers to control register bit

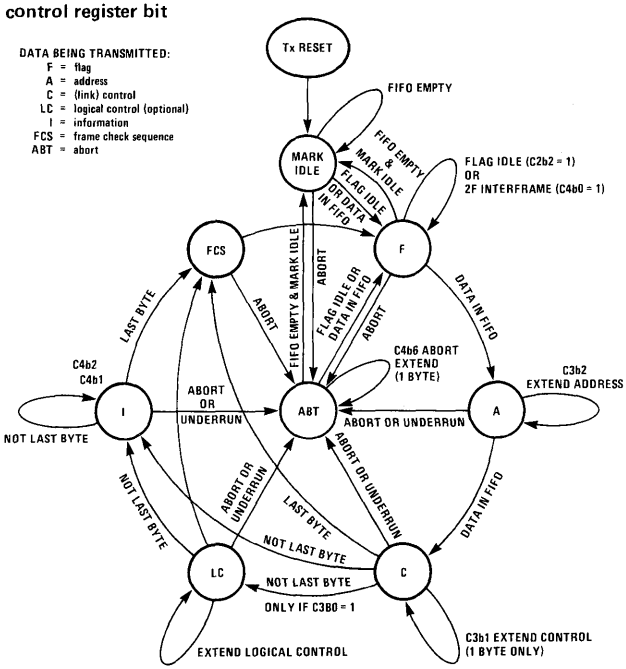
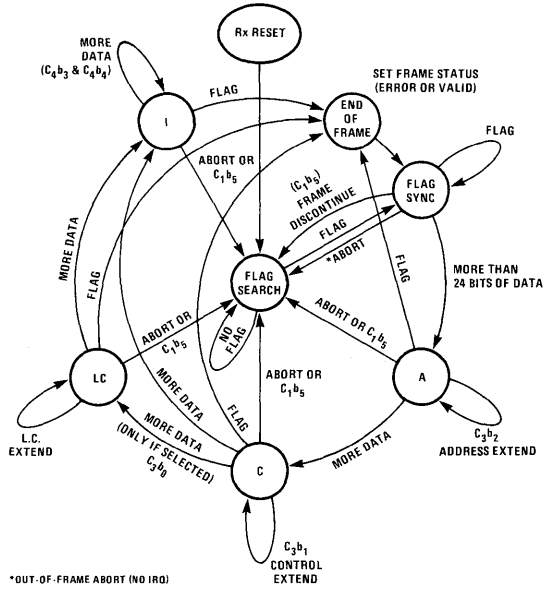


Figure 7B. ADLC Receiver State Diagram



Operation (Continued)

or Idling condition occurs. The receiver continuously (on a bit-by-bit basis) searches for Flags and Aborts.

When a flag is detected, the receiver establishes frame synchronization to the flag timing. If a series of flags is received, the receiver resynchronizes to each flag.

If the frame is terminated before the internal buffer time expires (the frame data is less than 25 bits after an opening flag), the frame is simply ignored. Noise on the data input (RxD) during time fill can cause this kind of invalid frame.

Once synchronization has been achieved and the internal buffer time (24 bit times) expires data will automatically transfer to the Rx Data FIFO. The Rx Data FIFO is clocked by E to cause received data to move through the FIFO to the last empty register location. The Receiver Data Available status bit (RDA) indicates when data is present in the last register (Reg. #3) for the 1 Byte Transfer Mode. The 2 Byte Transfer Mode causes the RDA status bit to indicate data is available when the last two FIFO register locations (Reg. #2 and #3) are full. If the data character present in the FIFO is an address octet the status register will exhibit an Address Present status condition. Data being available in the Rx Data FIFO causes an interrupt to be initiated (assuming the receiver interrupt is enabled, RIE = "1"). The MPU will read the ADLC Status Register as a result of the interrupt or in its turn in a polling sequence. RDA or Address Present will indicate that receiver data is available and the MPU should subsequently read the Rx Data FIFO register. The interrupt and status bit will then be reset automatically. If more than one character had been received and was resident in the Rx Data FIFO, subsequent E clocks will cause the FIFO to update and the RDA status bit and interrupt will again be SET. In the two byte transfer mode both data bytes may be read on consecutive E cycles. Address Present provides for 1 byte transfers only.

The sequence of each field in the received frame is automatically handled by the ADLC. The frame format is described in the "FRAME FORMAT" section.

When a closing flag is received, the frame is terminated. The 16 bits preceding the closing flag are regarded as the FCS and are not transferred to the MPU. Whatever data is present in the most significant byte portion of the receiver buffer register is right justified and transferred to the Rx FIFO. The frame boundary pointer, which is explained in the "Rx FIFO REGISTER" section, is set simultaneously in the Rx FIFO. The frame boundary pointer sets the Frame Valid status bit (when the frame was completed with no error) or the FCS/IF Error Status bit (when the frame was completed with error) when the last byte of the frame appears at the last location of the Rx FIFO. As long as the Frame Valid or FCS/IF Error status bit is set, the data transfer from the second location of the Rx FIFO to the last location of the Rx FIFO is inhibited.

Any time the Frame Discontinue control bit is set, the ADLC discards the current frame data in the ADLC without dropping flag synchronization. This feature can be used to ignore a frame which is addressed to another station.

The reception of an abort or idle is explained in the "FRAME FORMAT" section. The details regarding the inputs, outputs, status bits, control bits, and Rx FIFO operation are described in their respective sections.

Loop Mode Operation — The ADLC in the loop mode not only performs the transmission and receiving of data frames in the manner previously described but also has additional features for gaining and relinquishing loop control. In Figure 8a, a configuration is shown which depicts loop mode operation. The system configuration shows a primary station and several secondary stations. The loop is always under control of the primary station. When the primary wants to receive data, it transmits a Poll sequence and allows frame transmission to secondary stations on the loop. Each secondary is in series and adds one bit of delay to the loop. Secondary A in the figure receives data from the primary via its Rx Data Input, delays the data 1 bit, and transmits it to secondary B via its Tx Data Output. Secondaries B, C, and D operate in a similar manner. Therefore, data passes through each secondary and is received back by the primary controller.

Certain protocol rules must be followed in the manner by which the secondary station places itself on-loop (connects its transmitter output to the loop), goes active on the loop (starts transmitting its own stations' data on the loop), and goes off the loop (disconnects its transmitter output). Otherwise loop data to other stations down loop would be interfered. The data stream always flows the same way and the order in which secondary terminals are serviced is determined by the hardware configuration. The primary controller times the delay through the loop. Should it exceed n + 1 bit times, where n is the number of secondary terminals on the loop, it will indicate a loop failure. Control is transferred to a secondary by transmitting

Figure 8A. Typical Loop Configuration

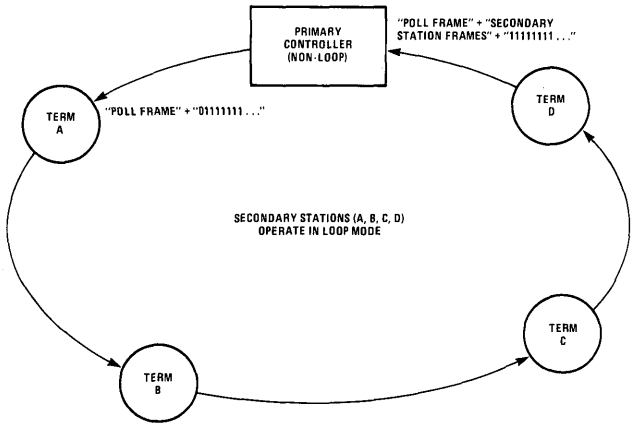
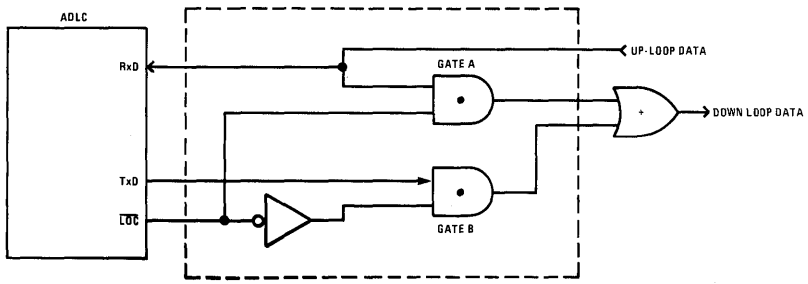


Figure 8B. Example of External Loop Logic



a "Go Ahead" signal following the closing Flag of a polling frame (request for a response from the secondary) from the primary station. The "Go Ahead" from the primary is a "0" and 7 "1's" followed by mark idling. The primary can abort its response request by interrupting its idle with flags. The secondary should immediately stop transmission and return control back to the primary. When the secondary completes its frame, a closing flag is transmitted followed by all "1"s. The primary detects the final 01111111 . . . ("Go Ahead" to the primary) and control is given back to the primary. Note that, if a down-loop secondary (e.g., station D) needs to insert information following an up-loop station (e.g., station A), the go ahead to station D is the last "0" of the closing flag from station A followed by "1's".

The ADLC in the primary station should operate in a non-loop, full duplex mode. The ADLC in the secondaries should operate in a loop mode, monitoring up-loop data on its receiver data input. The ADLC can recognize the necessary sequences in the data stream to automatically go on/off the loop and to insert its own station data. The procedure is the following and is summarized in Table 1.

Table 1. Summary of Loop Mode Operation

STATE	RX SECTION	TX SECTION	LOOP STATUS BIT
OFF-LOOP	Rx section receives data from loop and searches for 7 "1's" (when On-Loop Control bit set) to go ON-LOOP.	Inactive 1) NRZ MODE Tx data output is maintained "high" (mark). 2) NRZI MODE Tx data output reflects the Rx data input state delayed by one bit time. (Not normally connected to loop.) The NRZI data is internally decoded to provide error-free transitions to On-Loop mode.	"0"
ON-LOOP	1) When Go-Active on poll bit is set, Rx section searches for 01111111 pattern (the EOP or 'Go Ahead') to become the active terminal on the loop. 2) When On-Loop control bit is reset, Rx section searches of 8 "1's" to go OFF-LOOP.	Inactive 1) NRZ MODE Tx data output reflects Rx data input state delayed one bit time. 2) NRZI MODE Tx data output reflects Rx data input state delayed 2 bit times.	"1"
ACTIVE	Rx section searches for flag (an interrupt from the loop controller) at Rx data input. Received flag causes $\overline{FD}$ output to go low. IRQ is generated if $\overline{RIE}$ and FDSE control bits are set.	Tx data originates within ADLC until Go Active on Poll bit is reset and a flag or Abort is completed. Then returns to ON-LOOP state.	"0"

(1) Go On-loop — when the ADLC powers up, the terminal station will be off line. The first task is to become an active terminal on the loop. The ADLC must be connected to a Loop Link via an external switch as shown in Figure 8b. After hardware reset, the ADLC $\overline{LOC}/\overline{DTR}$ Output will be in the high state and the up-loop receive data repeated through gate A to the down Loop stations. Any Up-Loop transmission will be received by the ADLC. The Loop/Non-Loop Mode Control bit (bit 5 in Control Register 3) must be set to place the ADLC in the Loop Mode. The ADLC now monitors its Rx Data input for a string of seven consecutive "1's" which will allow a station to go on line. The Loop operation may be monitored by use of the Loop Status bit in Status Register 1. After power up and reset, this bit is a zero. When seven consecutive ones are received by the ADLC the $\overline{LOC}/\overline{DTR}$ output will go to a low level, disabling gate A (refer to Figure 8b), enabling gate B and connecting the ADLC Tx Data output to the down Loop stations. The up Loop data is now repeated to the down Loop stations via the ADLC. A one bit delay is inserted in the data (in NRZI mode, there will be a 2 bit delay) as it circulates through the ADLC. The ADLC is now on-line and the Loop Status bit in Status Register 1 will be at a one.

(2) Go Active after Poll — The receiver section will monitor the up link data for a general or addressed poll command and the Tx FIFO should be loaded with data so that when the go-ahead sequence of a zero followed by seven ones (01111111 ---) is detected, transmission can be initiated immediately. When the polling frame is detected, the Go-Active-On-Poll control bit must be set (bit 6 in Control Register 3). A minimum of seven bit times are available to set this control bit after the closing flag of the poll. When the Go-Ahead is detected by the receiver, the ADLC will automatically change the seventh one to a zero so that repeated sequence out gate B in Figure 8b is now opening flag sequence (01111110). Transmission now continues from the Tx FIFO with data (address, control, etc.) as previously described. When the ADLC has gone active-on-poll, the Loop Status bit in Status Register 1 will go to a zero. The receiver searches for a flag, which indicates that the primary station is interrupting the current operation.

(3) Go Inactive when On-Loop — The Go-Active-On Poll control bit may be RESET at any time during transmission. When the frame is complete (the closing Flag or abort is transmitted), the Loop is automatically released and the station reverts back to being

just a one bit delay in the Loop, repeating up link data. If the Go-Active-On-Poll control bit is not reset by software and the final frame is transmitted (Flag/Mark Idle bit = 0), then the transmitter will mark idle and will not release the loop to up-loop data. A Tx Abort command would have to be used in this case in order to go inactive when on the loop. Also, if the Tx FIFO was not preloaded with data (address, control, etc.) prior to changing the "Go Ahead Character" to a Flag, the ADLC will either transmit flags (active idle character) until data is loaded (when Flag/Mark Idle Control bit is high) or will go into an underrun condition and transmit an Abort (when Flag/Mark Idle control bit is low). When an abort is transmitted, the Go-Active-on-Poll control bit is reset automatically and the ADLC reverts to its repeating mode, (TxD = delayed RxD). When the ADLC transmitter lets go of the loop, the Loop Status bit will return to a "1", indicating normal on-loop retransmission of up-loop data.

4) Go Off-Loop — The ADLC can drop-off the Loop (go off-line) similar to the way it went on-line. When the Loop On-Line control bit is reset the ADLC receiver section looks for 8 successive "1's" before allowing the $\overline{LOC}/\overline{DTR}$ output to return high (the inactive state). Gate A in Figure 8b will be enabled and Gate B disabled allowing the loop to maintain continuity without disturbance. The Loop Status bit will show an off-line condition (logical zero).

Input/Output Functions

All inputs of ADLC are high impedance and TTL compatible level inputs. All outputs of the ADLC are compatible with standard TTL. Interrupt Request (IRQ), however, is an open drain output (no internal pull-up).

Interface for MPU

D0-D7

Bidirectional Data Bus — These data bus I/O ports allow the data transfer between ADLC and system bus. The data bus drivers are three-state devices that remain in the high impedance (off) state except when the MPU performs an ADLC read operation.

E

Enable Clock — E activates the address inputs ($\overline{CS}$, RS0 and RS1) and R/W input and enables the data transfer on the data bus. E also move data through the Tx FIFO and Rx FIFO. E should be a free running clock such as the S6800 MPU system clock.

$\overline{CS}$

Chip Select — An ADLC read or write operation is enabled only when the $\overline{CS}$ input is low and the E clock input is high. ($E \cdot \overline{CS}$).

RS0

RS1

Register Selects — When the Register Select inputs are enabled by ($E \cdot \overline{CS}$), they select internal registers in conjunction with the Read/Write input and Address Control bit (control register 1, bit 0). Register addressing is defined in Table 2.

R/W

Read/Write Control Line — The R/W input controls the direction of data flow on the data bus when it is enabled by ($E \cdot CS$). When R/W is high, the I/O Buffer acts as an output driver and as an input buffer when low. It also selects the Read Only and Write Only registers within the ADLC.

$\overline{RESET}$

Reset Input — The $\overline{RESET}$ Input provides a means of resetting the ADLC from a hardware source. In the "low state," the $\overline{RESET}$ Input causes the following:

- ☐ Rx Reset and Tx Reset are SET causing both the Receiver and Transmitter sections to be held in a reset condition.
- ☐ Resets the following control bits: Transmit Abort, RTS, Loop Mode, and Loop On-Line/DTR.
- ☐ Clears all stored status condition of the status registers.
- ☐ Outputs: $\overline{RTS}$ and $\overline{LOC}/\overline{DTR}$ go high. TxD goes to the mark state ("1's" are transmitted).

When $\overline{RESET}$ returns "high" (the inactive state) the transmitter and receiver sections will remain in the reset state until Tx Reset and Rx Reset are cleared via the data bus under software control. The Control Register bits affected by $\overline{RESET}$ cannot be changed when $\overline{RESET}$ is "low".

$\overline{IRQ}$

Interrupt Request Output — $\overline{IRQ}$ will be low if an interrupt situation exists and the appropriate interrupt enable has been set. The interrupt remains as long as the cause for the interrupt is present and the enable is set.

Clock and Data of Transmitter and Receiver

TxC

Transmitter Clock Input — The transmitter shifts data

on the negative transition of the TxC clock input. When the Loop Mode or Test Mode is selected, TxC should be the same frequency and phase as the RxC clock. The data rate of the transmitter should not exceed the E frequency.

RxC

Receiver Clock Input — The receiver samples the data on the positive transition of the TxC clock. RxC should be synchronized with receive data externally.

TxD

Transmit Data Output — The serial data from the transmitter is coded in NRZ or NRZI (Zero Complement) data format.

RxD

Receiver Data Input — The serial data to be received by the ADLC can be coded in NRZ or NRZI (Zero Complement) data format. The data rate of the receiver should not exceed the E frequency. If a partial byte reception is possible at the end of a frame, the maximum data rate of the receiver is indicated by the following relationship:

$$f_{RxC} \leq \frac{1}{2t_E + 300ns}$$

where t_E is the period of E.

Peripheral/Modem Control

$\overline{RTS}$

Request to Send Output — The Request-to-Send output is controlled by the Request-to-Send control bit in conjunction with the state of the transmitter section. When the RTS bit goes high, the $\overline{RTS}$ output is forced low. When the RTS bit returns low, the $\overline{RTS}$ output remains low until the end of the frame. The positive transition of $\overline{RTS}$ occurs after the completion of a Flag, an Abort, or when the RTS control bit is reset during a mark idling state. When the $\overline{RESET}$ input is low, the $\overline{RTS}$ output goes high.

$\overline{CTS}$

Clear to Send Input — The $\overline{CTS}$ input provides a real-time inhibit to the TDRA status bit and its associated interrupt. The positive transition of $\overline{CTS}$ is stored within the ADLC to insure its occurrence will be acknowledged by the system. The stored CTS information and its associated IRQ (if enabled) are cleared by writing a "1" in the Clear Tx Status bit or in the Transmitter Reset bit.

$\overline{DCD}$

Data Carrier Detect Input — The $\overline{DCD}$ input provides a real-time inhibit to the receiver section. A high level on the $\overline{DCD}$ input resets and inhibits the receiver register, but data in the Rx FIFO from a previous frame is not disturbed. The positive transition of $\overline{DCD}$ is stored within the ADLC to insure that its occurrence will be acknowledged by the system. The stored DCD information and its associated IRQ (if enabled) are cleared by means of the Clear Rx Status Control bit or by the Rx Reset bit.

$\overline{LOC}/\overline{DTR}$

Loop On Line Control/Data Terminal Ready output — The $\overline{LOC}/\overline{DTR}$ output serves as a $\overline{DTR}$ output in the non-loop mode or as a Loop Control output in the loop mode. When $\overline{LOC}/\overline{DTR}$ output performs the $\overline{DTR}$ function, it is turned on and off by means of the LOC/DTR control bit. When the Loc/DTR control bit is high the $\overline{DTR}$ output will be low. In the loop mode the $\overline{LOC}/\overline{DTR}$ output provides the means of controlling the external loop interface hardware to go On-line or Off-line. When the LOC/DTR control bit is SET and the loop has "idled" for 7 bit times or more (RxD) = 01111111 . . .), the $\overline{LOC}/\overline{DTR}$ output will go low (on-line). When the LOC/DTR control bit is low and the loop has "idled" for 8 bit times or more, the $\overline{LOC}/\overline{DTR}$ output will return high (off-line). The $\overline{RESET}$ input being low will cause the $\overline{LOC}/\overline{DTR}$ output to be high.

$\overline{FD}$

Flag Detect Output — An output to indicate the reception of a flag and initiate an external time-out counter for the loop mode operation. The $\overline{FD}$ output goes low for one bit time beginning at the last bit of the flag character, as sampled by the receiver clock (RxC).

DMA Interface

RDSR

Receiver Data Service Request Output — The RDSR Output is provided primarily for use in DMA Mode operation and indicates (when high) that the Rx FIFO requests service (RSDR output reflects the RDA status bit). If the prioritized Status Mode is selected, RDSR will be inhibited when any other receiver status conditions are present. RDSR goes low when the Rx FIFO is read.

TDSR

Transmitter Data Service Request Output — The TDSR Output is proivded for DMA mode operation and indicates (when high) that the Tx FIFO requests

service (TDSR reflects the TDRA status bit). TDSR goes low when the Tx FIFO is loaded. TDSR is inhibited by: The Tx Rs control bit being SET, $\overline{\text{RESET}}$ being low, or $\overline{\text{CTS}}$ being high. If the prioritized status mode is used, Tx underrun also inhibits TDSR.

ADLC Registers

Eight registers in the ADLC can be accessed by means of the MPU data and address buses. The registers are defined as read only or write only according to the direction of information flow. The addresses of these registers are defined in Table 2. The transmitter FIFO register can be accessed by two different addresses, the "Frame Terminate" address and the "Frame Continue" address. (The function of these addresses are discussed in the FIFO section.)

Table 2. Register Addressing

Register Selected	R/W	RS1	RS0	Address Control Bit (C_1b_0)
Write Control Register #1	0	0	0	X
Write Control Register #2	0	0	1	0
Write Control Register #3	0	0	1	1
Write Transmit FIFO (Frame Terminate)	0	1	1	0
Write Control Register #4	0	1	1	1
Read Status Register #1	1	0	0	X
Read Status Register #2	1	0	1	X
Read Receiver FIFO	1	1	X	X

Receiver Data First-In First-Out Register

Rx FIFO

The Rx FIFO consists of three 8-bit registers which are used for the buffer storage of received data. Data bytes are always transferred from a full register to an adjacent empty register; and both phases of the E input clock are used for the data transfer. Each register has pointer bits which point the frame boundary. When these pointers appear at the last FIFO location, they update the Address Present, Frame Valid or FCS/IF Error status bits.

The RDA status bit indicates the state of the Rx FIFO. When RDA status bit is "1", the Rx FIFO is ready to be read. The RDA status is controlled by the 2 Byte/1 Byte control bit. When overrun occurs, the data in the first byte of the Rx FIFO are no longer valid.

Both the Rx Reset bit and $\overline{\text{Reset}}$ input clear the Rx FIFO. Abort ("In Frame") and a high level on the $\overline{\text{DCD}}$ input also clears the Rx FIFO, but the last bytes of the previous frame, which are separated by the frame boundary pointer, are not disturbed.

Transmitter Data First-In First-Out Register

Tx FIFO

The Tx FIFO consists of three 8-bit registers which are used for buffer storage of data to be transmitted. Data is always transferred from a full register to an empty adjacent register; the transfer occurs on both phases of the E input clock. The Tx FIFO can be addressed by two different register addresses, the "Frame Continue" address and the "Frame Terminate" address. Each register has pointer bits which point to the frame boundary. When a data byte is written at the "Frame Continue" address, the pointer of the first FIFO register is set. When a data byte is written at the "Frame Terminate" address, the pointer of the first FIFO register is reset. RxRs control bit or Tx Abort control bit resets all pointers. The pointer will shift through the FIFO. When positive transition is detected at the third location of FIFO, the transmitter initiates a frame with an open flag. When the negative transition is detected at the third location of FIFO, the transmitter closes a frame, appending the FCS and closing Flag to the last byte.

The Tx last control bit can be used instead of using the "Frame Terminate" address. When the Tx last control bit is written by a "1", the logic searches the last byte location in the FIFO and resets the pointer in the FIFO register.

The status of Tx FIFO is indicated by the TDRA status bit. When TDRA is "1", the Tx FIFO is available for loading data. The TDRA status is controlled by the 2BYTE/1BYTE control bit. The Tx FIFO is reset by both Tx Reset and $\overline{\text{RESET}}$ input. During this reset condition or when $\overline{\text{CTS}}$ input is high, the TDRA status bit is suppressed and data loading is inhibited.

S28211	**Signal Processing Peripheral**
S28214A	**Fast Fourier Transformer**
S28215	**Digital Filter/Utility Peripheral**
S28216	**Echo Cancellor Processor**

Please refer to product data sheets in Communication Section on pages 3.88 to 3.128.

AMERICAN MICROSYSTEMS, INC.

S9900

High Performance Microprocessor Family

MICROPROCESSORS

S9900	16-Bit Microprocessor
S9980A/S9981	16-Bit Microprocessor 8-Bit Data Bus (S9981 has Internal Clock)

PERIPHERALS

S9901	Programmable Systems Interface (PSI)
S9902	UART/Asynchronous Communications Controller (USRT/ACC)

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S9900

16-BIT MICROPROCESSOR

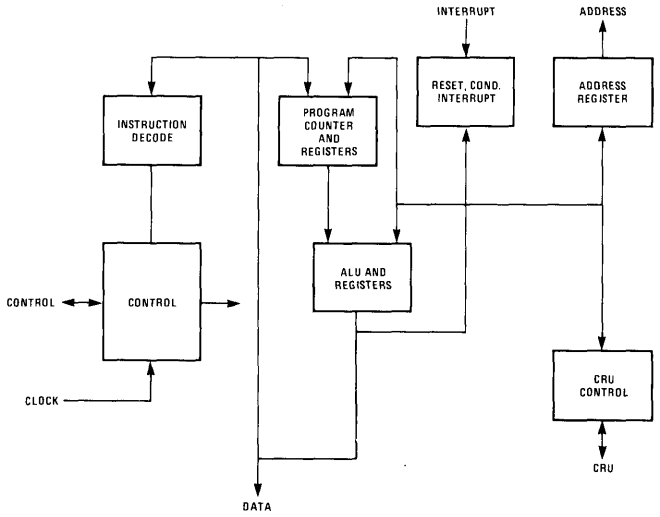
Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability including Multiply and Divide
- ☐ Up to 65,536 Bytes of Memory
- ☐ 3.3MHz Speed
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 16 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ N-Channel Silicon-Gate Technology

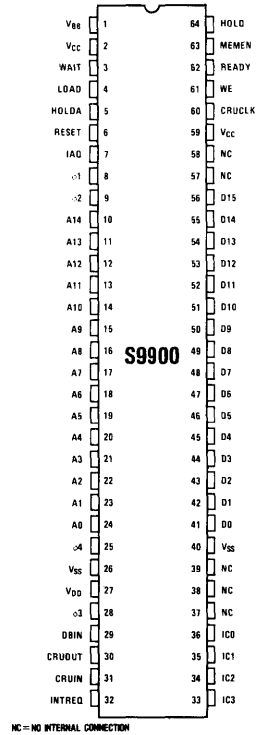
General Description

The S9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-channel silicon-gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and support circuits to be used with an S9900 system. The system is fully supported by software and complete prototyping systems.

Block Diagram



Pin Configuration



NC = NO INTERNAL CONNECTION

S9900 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1) ..... −0.3V to +20V
Supply Voltage, V_{DD} (See Note 1) ..... −0.3V to +20V
Supply Voltage, V_{SS} (See Note 1) ..... −0.3V to +20V
All Input Voltages (See Note 1) ..... −0.3V to +20V
Output Voltage (with Respect to V_{SS}) ..... −2V to +7V
Continuous Power Dissipation 1.2W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	-5.25	-5	-4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage (all inputs except clocks)	2.2	2.4	V_{CC}+1	V	
$V_{IH(\phi)}$	High-level clock input voltage	V_{DD}-2		V_{DD}	V	
V_{IL}	Low-level input voltage (all inputs except clocks)	-1	0.4	0.8	V	
$V_{IL(\phi)}$	Low-level clock input voltage	-0.3	0.3	0.6	V	
T_A	Operating free-air temperature	0		70	°C	

Timing Requirements Over Full Range of Recommended Operating Conditions (See Figures 1 and 2)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
$t_{c(\phi)}$	Clock cycle time	0.3	0.333	0.5	μs	
$t_{r(\phi)}$	Clock rise time	10	12		ns	
$t_{f(\phi)}$	Clock fall time	10	12		ns	
$t_{w(\phi)}$	Pulse width, any clock high	40	45	100	ns	
$t_{\phi 1L, \phi 2L}$	Delay time, clock 1 low to clock 2 low (time between clock pulses)	0	5		ns	
$t_{\phi 2L, \phi 3L}$	Delay time, clock 2 low to clock 3 low (time between clock pulses)	0	5		ns	
$t_{\phi 3L, \phi 4L}$	Delay time, clock 3 low to clock 4 low (time between clock pulses)	0	5		ns	
$t_{\phi 4L, \phi 1L}$	Delay time, clock 4 low to clock 1 low (time between clock pulses)	0	5		ns	
$t_{\phi 1H, \phi 2H}$	Delay time, clock 1 high to clock 2 high (time between leading edges)	73	83		ns	
$t_{\phi 2H, \phi 3H}$	Delay time, clock 2 high to clock 3 high (time between leading edges)	73	83		ns	
$t_{\phi 3H, \phi 4H}$	Delay time, clock 3 high to clock 4 high (time between leading edges)	73	83		ns	
$t_{\phi 4H, \phi 1H}$	Delay time, clock 4 high to clock 1 high (time between leading edges)	73	8		ns	
t_{su}	Data or control setup time before clock 1	30			ns	
t_h	Data hold time after clock 1	10			ns	

Electrical Characteristics Over Full Range of Recommended Operating Conditions (unless otherwise noted)

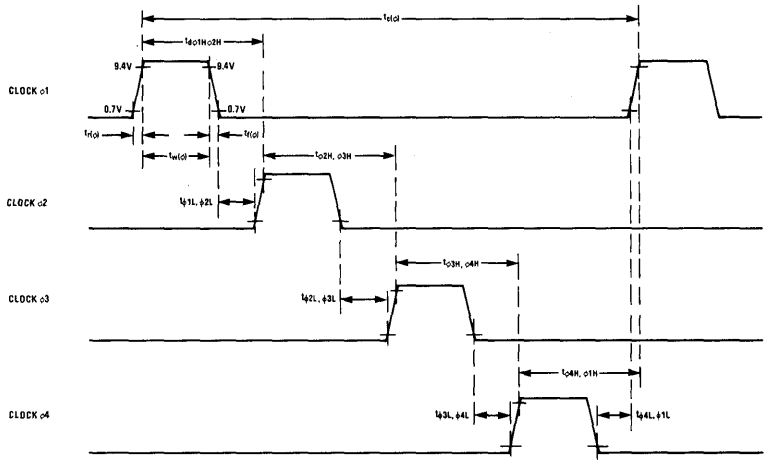
Symbol	Parameter		Min.	Typ.†	Max.	Unit	Conditions
I_I	Input current	Data Bus during DBIN		±50	±100	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, DBIN, Address bus, Data bus during HOLDA		±50	±100		$V_I = V_{SS}$ to V_{CC}
		Clock*		±25	±75		V_I = -0.3 to 12.6V
		Any other inputs		±1	±10		$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4		V_{CC}	V	I_O = -0.4mA
V_{OL}	Low-level output voltage				0.65 0.50	V	I_O = 32.mA I_O = 2mA
I_{BB}	Supply current from V_{BB}			0.1	1	mA	
I_{CC}	Supply current from V_{CC}			50	75	mA	
I_{DD}	Supply current from V_{DD}			25	45	mA	
C_i	Input capacitance (any inputs except clock and data bus)			10	15	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 1)}$	Clock-1 input capacitance			100	150	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 2)}$	Clock-2 input capacitance			150	200	pF	V_{BB} = -5, f = 1MHz unmeasured pins at V_{SS}
$C_{i(\phi 3)}$	Clock-3 input capacitance			100	150	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
$C_{i(\phi 4)}$	Clock-4 input capacitance			100	150	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			15	25	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}
C_o	Output capacitance (any output except data bus)			10	15	pF	V_{BB} = -5, f = 1MHz, unmeasured pins at V_{SS}

†All typical values are at $T_A = 25°C$ and nominal voltages.
*D.C. Component of Operating Clock.

Switching Characteristics Over Full Range of Recommended Operating Conditions (See Figure 2)

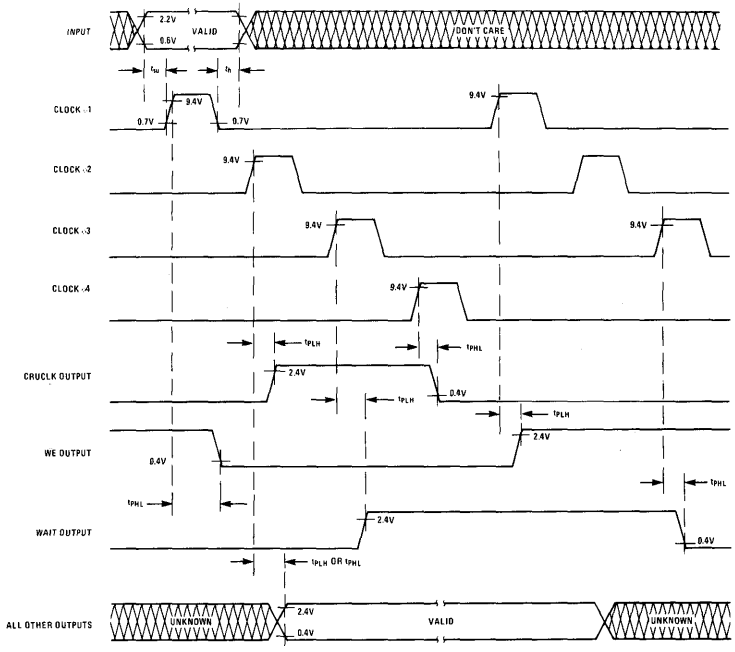
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{PLH} or t_{PHL}	Propagation delay time, clocks to outputs					C_L=200pF
	CRUCLK, WE, MEMEN, WAIT, DBIN			30	ns	
	All other outputs		20	40	ns	

Figure 1. Clock Timing



Note: All timing and voltage levels shown on ϕ1 apply to ϕ2, ϕ3, and ϕ4 in the same manner.

Figure 2. Signal Timing



†The number of cycles over which input/output data must/will remain valid can be determined from the number of wait states required for memory access. Note that in all cases data should not change during ϕ1.

Pin Description

Table 1 defines the S9900 pin assignments and describes the function of each pin.

Table 1. S9900 Pin Assignments and Functions

Signature	Pin	I/O	Description
			ADDRESS BUS
A0 (MSB)	24	OUT	A0 through A14 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when $\overline{\text{MEMEN}}$ is active and I/O-bit addresses and external-instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A1	23	OUT	
A2	22	OUT	
A3	21	OUT	
A4	20	OUT	
A5	19	OUT	
A6	18	OUT	
A7	17	OUT	
A8	16	OUT	
A9	15	OUT	
A10	14	OUT	
A11	13	OUT	
A12	12	OUT	
A13	11	OUT	
A14 (LSB)	10	OUT	
			DATA BUS
D0 (MSB)	41	I/O	D0 through D15 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. The data bus assumes the high-impedance state when HOLDA is active.
D1	42	I/O	
D2	43	I/O	
D3	44	I/O	
D4	45	I/O	
D5	46	I/O	
D6	47	I/O	
D7	48	I/O	
D8	49	I/O	
D9	50	I/O	
D10	51	I/O	
D11	52	I/O	
D12	53	I/O	
D13	54	I/O	
D14	55	I/O	
D15 (LSB)	56	I/O	
			POWER SUPPLIES
V_{BB}	1		Supply voltage (-5V NOM)
V_{CC}	2,59		Supply voltage (5V NOM). Pins 2 and 59 must be connected in parallel.
V_{DD}	27		Supply volage (12V NOM)
V_{SS}	26,40		Ground reference. Pins 26 and 40 must be connected in parallel.
			CLOCKS
$\phi 1$	8	IN	Phase-1 clock
$\phi 2$	9	IN	Phase-2 clock
$\phi 3$	28	IN	Phase-3 clock
$\phi 4$	25	IN	Phase-4 clock

Table 1. S9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
			BUS CONTROL
DBIN	29	OUT	Data bus in. When active (high), DBIN indicates that the S9900 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active.
$\overline{\text{MEMEN}}$	63	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address.
$\overline{\text{WE}}$	61	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9900 to be written into memory.
CRUCLK	60	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0 through A2.
CRUIN	31	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A3 through A14).
CRUOUT	30	OUT	CRU data out. Serial I/O data appears on the CRUOUT line when an LDCR, SBZ, or SBO instruction is executed. The data on CRUOUT should be sampled by external I/O interface logic when CRUCLK goes active (high).
			INTERRUPT CONTROL
$\overline{\text{INTREQ}}$	32	IN	Interrupt request. When active (low), $\overline{\text{INTREQ}}$ indicates that an external-interrupt is requested. If $\overline{\text{INTREQ}}$ is active, the processor loads the data on the interrupt-code-input lines IC0 through IC3 into the internal interrupt-code-storage register. The code is compared to the interrupt mask bits of the status register. If equal or higher priority than the enabled interrupt level (interrupt code equal or less than status register bits 12 through 15) the S9900 interrupt sequence is initiated. If the comparison fails, the processor ignores the request. $\overline{\text{INTREQ}}$ should remain active and the processor will continue to sample IC0 through IC3 until the program enables a sufficiently low priority to accept the request interrupt.
IC0 (MSB)	36	IN	Interrupt codes. IC0 is the MSB of the interrupt code, which is sampled when $\overline{\text{INTREQ}}$ is active. When IC0 through IC3 are LLLH, the highest external-priority interrupt is being requested and when HHHH, the lowest-priority interrupt is being requested.
IC1	35	IN	
IC2	34	IN	
IC3 (LSB)	33	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	64	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9900 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.

*If the cycle following the present memory cycle is also a memory cycle, it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

Table 1. S9900 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
HOLDA	5	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{WE}$, $\overline{MEMEN}$, and DBIN) are in the high-impedance state.
READY	62	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9900 enters a wait state and suspends internal operation until the memory systems indicate ready.
WAIT	3	OUT	Wait. When active (high), WAIT indicates that the S9900 has entered a wait state because of a not-ready condition from memory.
			TIMING AND CONTROL
IAQ	7	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9900 is acquiring an instruction. IAQ can be used to detect illegal op codes.
$\overline{LOAD}$	4	IN	Load. When active (low), $\overline{LOAD}$ causes the S9900 to execute a nonmaskable interrupt with memory address $FFFC_{16}$ containing the trap vector (WP and PC). The load sequence begins after the instruction being executed is completed. $\overline{LOAD}$ will also terminate an idle state. If $\overline{LOAD}$ is active during the time $\overline{RESET}$ is released, then the $\overline{LOAD}$ trap will occur after the $\overline{RESET}$ fuction is completed. $\overline{LOAD}$ should remain active for one instruction period. IAQ can be used to determine instruction boundaries. This signal can be used to implement cold-start ROM loaders. Additionally, front-panel routines can be implemented using CRU bits as front-panel-interface signals and software-control routines to control the panel operations.
$\overline{RESET}$	6	IN	Reset. When active (low), $\overline{RESET}$ causes the processor to be reset and inhibits $\overline{WE}$ and CRUCLK. When $\overline{RESET}$ is released, the S9900 then initiates a level-zero interrupt sequence that acquires WP and PC from locations 0000 and 0002, sets all status register bits to zero, and starts execution. $\overline{RESET}$ will also terminate an idle state. $\overline{RESET}$ must be held active for a minimum of three clock cycles.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before the S9900 enters the hold state. The maximum number of consecutive memory cycles is three.

Timing

Memory

A basic memory read and write cycle is shown in Figure 3. The read cycle is shown with no wait states and the write cycle is shown with one wait state.

$\overline{MEMEN}$ goes active (low) during each memory cycle. At the same time that $\overline{MEMEN}$ is active, the memory address appears on the address bus bits A0 through A14. If the cycle is a memory-read-only cycle, DBIN will go active (high) at the same time $\overline{MEMEN}$ and A0 through A14 become valid. The memory-write signal $\overline{WE}$ will remain inactive (high) during a read cycle. If the read cycle is also an instruction acquisition cycle, IAQ will go active (high) during the cycle.

The READY signal, which allows extended memory cycles, is shown high during $\phi 1$ of the second clock cycle of the read operation. This indicates to the S9900 that memory-read data will be valid during $\phi 1$ of the next clock cycle. If READY is low during $\phi 1$, then the S9900 enters a wait state suspending internal operation until a READY is sensed during a subsequent $\phi 1$. The memory read data is then sampled by the S9900 during the next $\phi 1$, which completes the memory-read cycle.

At the end of the read cycle, $\overline{MEMEN}$ and DBIN go inactive (high and low, respectively). The address bus may also change at this time; however, the data bus remains in the input mode for one clock cycle after the read cycle.

A write cycle is similar to the read cycle with the exception that $\overline{WE}$ goes active (low) as shown and valid write data appears on the data bus at the same time the address appears. The write cycle is shown as an example of a one-wait-state memory cycle. READY is low during $\phi 1$ resulting in the WAIT signal shown.

Hold

Other interfaces may utilize the S9900 memory bus by using the hold operation (illustrated in Figure 4) of the S9900. When $\overline{HOLD}$ is active (low), the S9900 enters the hold state at the next available non-memory cycle. Considering that there can be a maximum of three consecutive memory cycles, the maximum delay between $\overline{HOLD}$ going active to HOLDA going active (high) could be $t_{c(\phi)}$ (for setup) + (6 + 3W) $t_{c(\phi)}$ + $t_{c(\phi)}$ (delay for HOLDA), where W is the number of wait states per memory cycle and $t_{c(\phi)}$ is the clock cycle time. When the S9900 has entered the hold state, HOLDA goes active (high) and A0 through A15, D0 through D15 DBIN, $\overline{MEMEN}$, and $\overline{WE}$ go into a high-impedance state to allow other devices to use the memory buses. When $\overline{HOLD}$ goes inactive (high), the S9900 resumes processing as shown. If hold occurs during a CRU operation, the S9900 uses an extra clock cycle (after the removal of the $\overline{HOLD}$ signal) to reassert the CRU address providing the normal setup times for the CRU bit transfer that was interrupted.

CRU

CRU interface timing is shown in Figure 5. The timing for transferring two bits out and one bit in is shown. These transfers would occur during the execution of a CRU instruction. The other cycles of the instruction execution are not illustrated. To output a CRU bit, the CRU-bit address is placed on the address bus A0 through A14 and the actual bit data on CRUOUT. During the second clock cycle a CRU pulse is supplied by CRUCLK. This process is repeated until the number of bits specified by the instruction are completed.

The CRU input operation is similar in that the bit address appears on A0 through A14. During the subsequent cycle the S9900 accepts the bit input data as shown. No CRUCLK pulses occur during a CRU input operation.

Figure 3. S9900 Memory Bus Timing

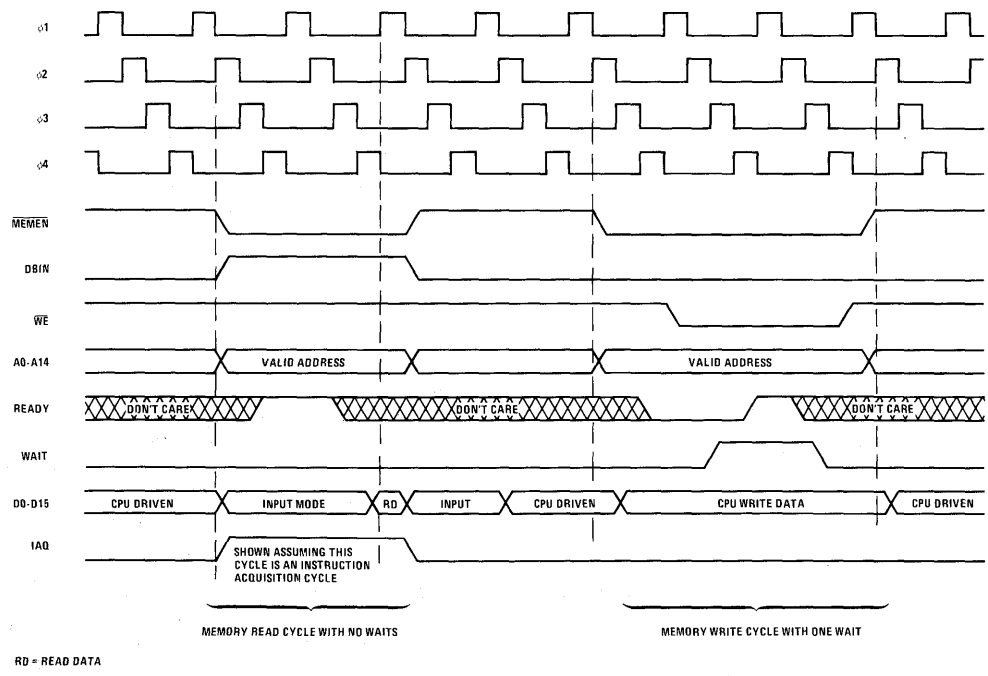


Figure 4. S9900 Hold Timing

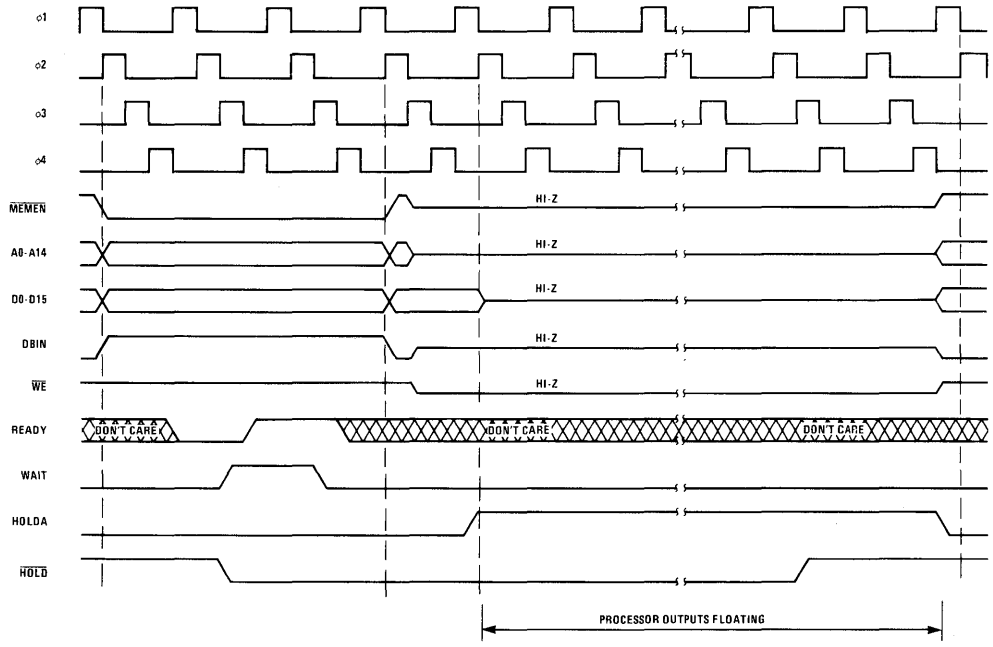
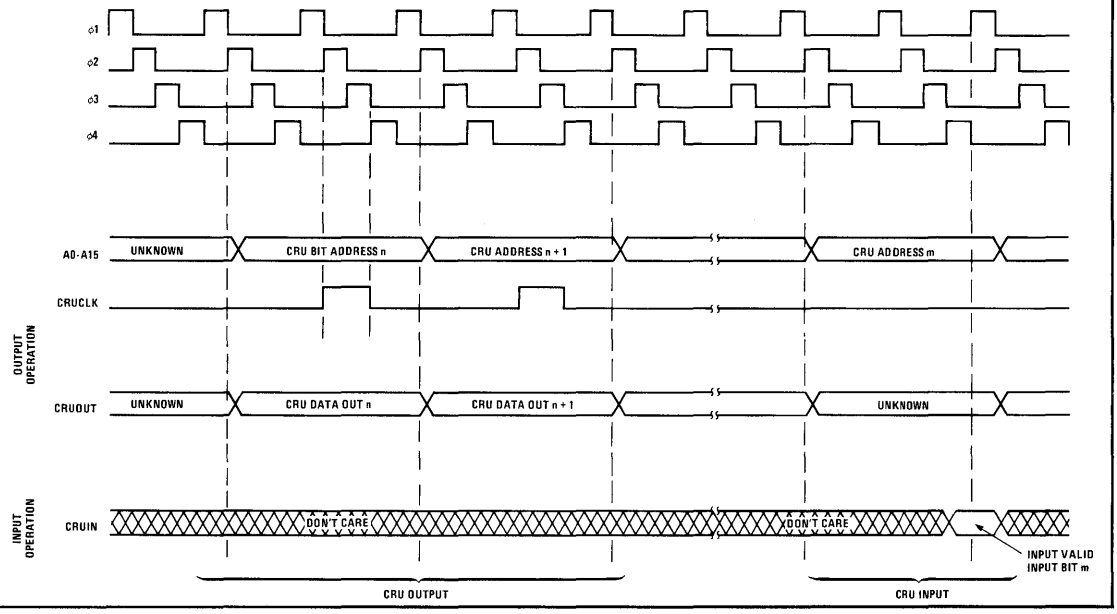


Figure 5. S9900 CRU Interface Timing



Architecture

The S9900 operation is shown in Figure 6 and its architecture illustrated by Figure 7.

Figure 6. S9900 CPU Flow Chart

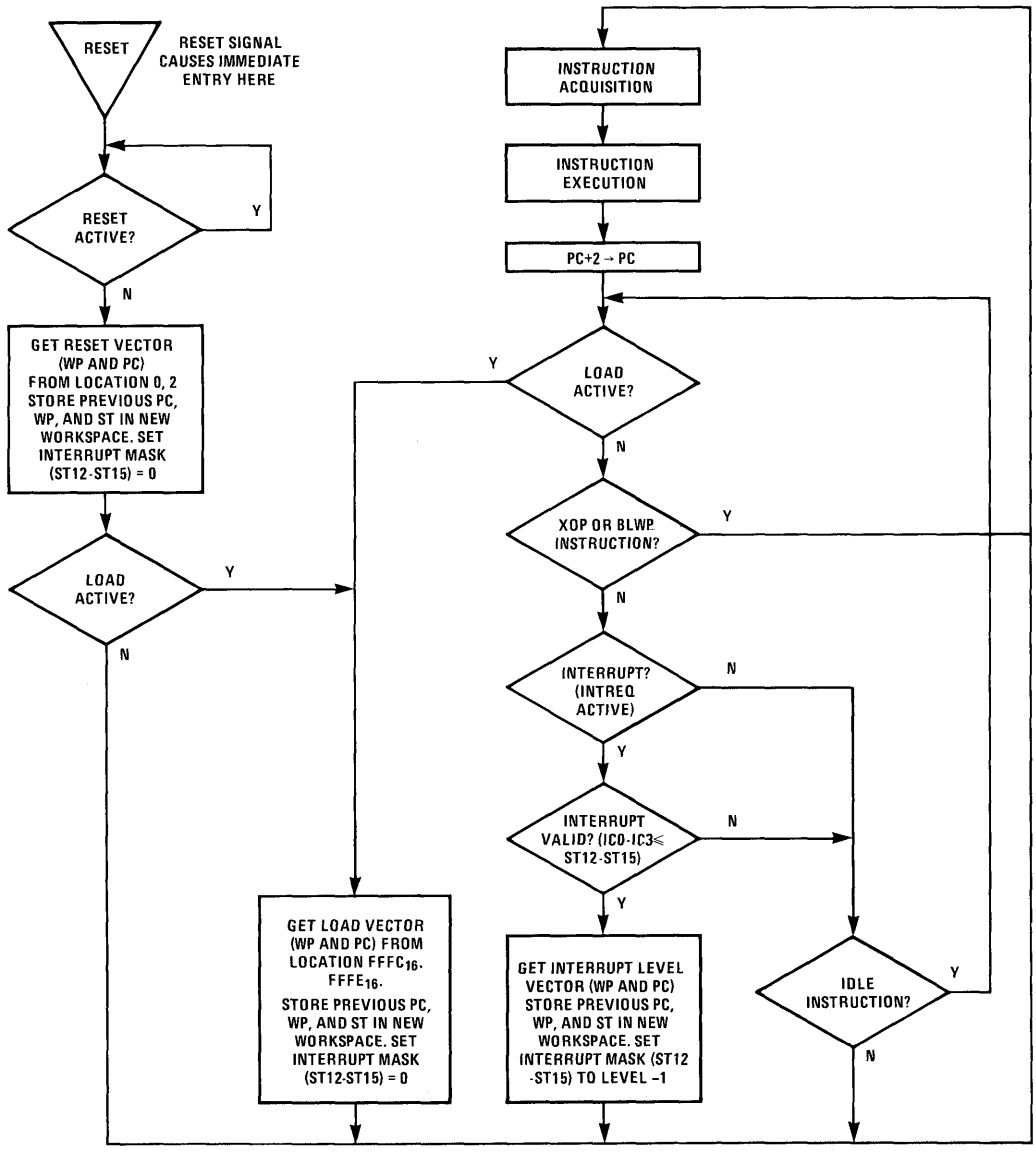
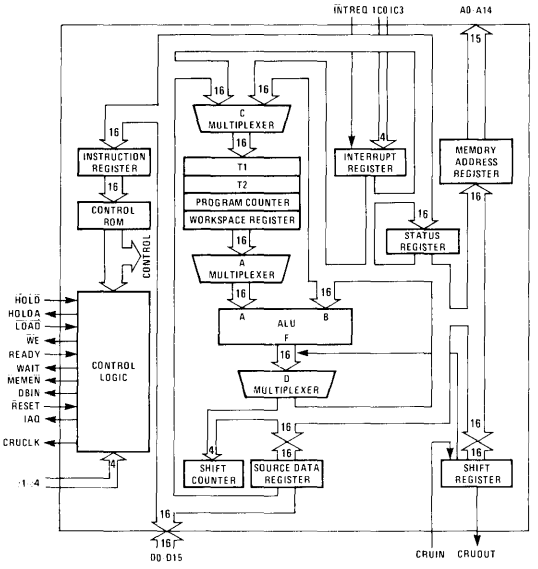
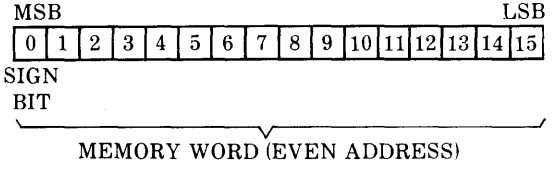


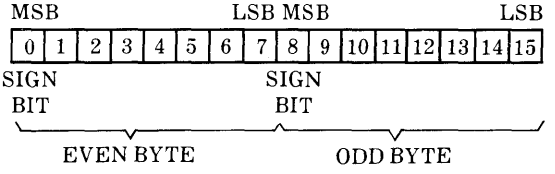
Figure 7. Architecture



Registers and Memory

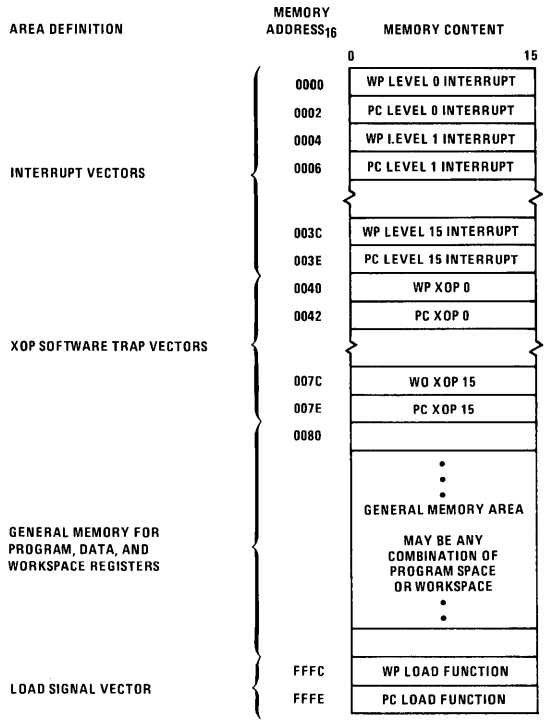
The S9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal-hardware registers with program-data registers. The memory word of the S9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the S9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte. The memory space is 65,536 bytes or 32,768 words. The word and byte formats are shown below.





The S9900 memory map is shown in Figure 8. The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

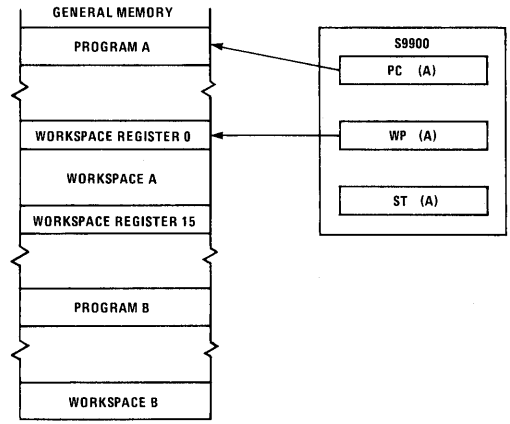
Figure 8. Memory Map



NOTE: 1 interrupt level 0 is reserved for RESET.

Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

A workspace-register file occupies 16 contiguous memory words in the general memory area (see Figure 2). Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer and initiating a memory request for the word. The relationship between the workspace pointer and its corresponding workspace is shown below.



The workspace concept is particularly valuable during operations that require a context switch, which is a change from one program environment to another (as in the case of an interrupt) or to a subroutine. Such an operation, using a conventional multi-register arrangement, requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the program counter, status register, and workspace pointer, the S9900 accomplishes a complete context switch with only three store cycles and three fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine. A corresponding time saving occurs when the original context is restored. Instructions in the S9900 that result in a context switch include:

1. Branch and Load Workspace Pointer (BLWP)
2. Return from Subroutine (RTWP)
3. Extended Operation (XOP).

Device interrupts, $\overline{\text{RESET}}$, and $\overline{\text{LOAD}}$ also cause a context switch by forcing the processor to trap to a service subroutine.

Interrupts

The S9900 employs 16 interrupt levels with the highest priority level 0 and lowest level 15. Level 0 is reserved for the $\overline{\text{RESET}}$ function and all other levels may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements.

The S9900 continuously compares the interrupt code (IC0 through IC3) with the interrupt mask contained in status-register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. The, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15, respectively, of the new workspace. The S9900 then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced, except for the level-zero interrupt, which loads zero into the mask. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed to preserve program linkage should a higher priority interrupt occur. All interrupt requests should remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete.

If a higher priority interrupt occurs, a second context switch occurs to service the higher priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower-priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters. The interrupt-vector locations, device assignment, enabling-mask value, and the interrupt code are shown in Table 2.

Input/Output

The S9900 utilizes a versatile direct command-driven I/O interface designated as the communications-register unit (CRU). The CRU provides up to 4096 directly addressable input bits and 4096 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The S9900 employs three dedicated I/O pins (CRUIN, CRUOUT, and CRUCLK) and 12 bits (A3 through A14) of the address bus to interface with the CRU system. The processor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move between memory and CRU data fields.

Single-Bit CRU Operations

The S9900 performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the S9900 develops a CRU-bit address and places it on the address bus, A3 to A14.

For the two output operations (SBO and SBZ), the processor also generates a CRUCLK pulse, indicating an output operation to the CRU device, and places bit 7 of the instruction word on the CRUOUT line to accomplish the specified operation (bit 7 is a one for SBO and a zero for SBZ). A test-bit instruction transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (EQUAL).

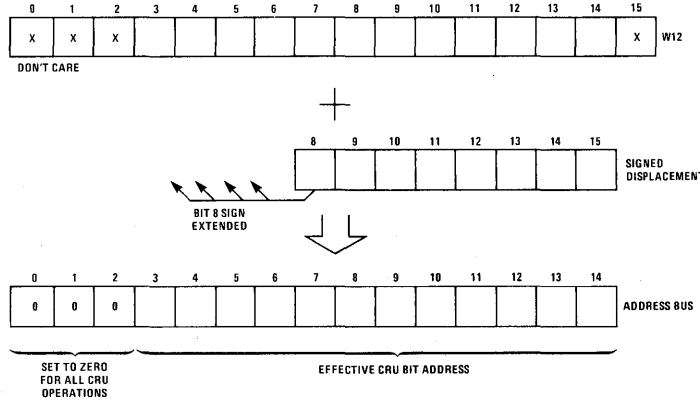
The S9900 develops a CRU-bit address for the single-bit operations from the CRU-base address contained in workspace register 12 and the signed displacement count contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded onto the address bus. Figure 9 illustrates the development of a single-bit CRU address.

Table 2. Interrupt Level Data

Interrupt Level		Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values to Enable Respective Interrupts (ST12 through ST15)	Interrupt Codes IC0 through IC3
(Highest priority)	0	00	Reset	0 through F*	0000
	1	04	External device	1 through F	0001
	2	08		2 through F	0010
	3	0C		3 through F	0011
	4	10		4 through F	0100
	5	14		5 through F	0101
	6	18		6 through F	0110
	7	1C		7 through F	0111
	8	20		8 through F	1000
	9	24		9 through F	1001
	10	28		A through F	1010
	11	2C		B through F	1011
	12	30		C through F	1100
	13	34		D through F	1101
	14	38		E and F	1110
(Lowest priority)	15	3C	External device	F only	1111

*Level 0 can not be disabled.

Figure 9. S9900 Single-Bit CRU Address Development



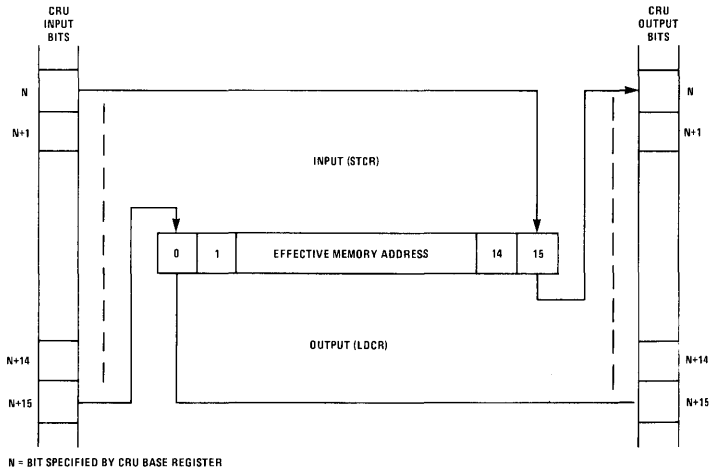
Multiple-Bit CRU Operations

The S9900 performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in Figure 10. Although the figure illustrates a full 16-bit transfer operation, any number of bits from 1 through 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, those bits come from the right-justified field within the addressed byte of the memory word. If the LDCR involves nine or more bits, those bits come from the right-justified field within the whole memory word. When transferred to the CRU interface, each successive bit receives an address that is sequentially greater than the address for the previous bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressd bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves from nine to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero.

When the input from CRU device is complete, the first bit from the CRU is the least-significant-bit position in the memory word or byte.

Figure 10. S9900 LDCR/STCR Data Transfers



S9900 Instruction Set

Definition

Each S9900 instruction performs one of the following operations:

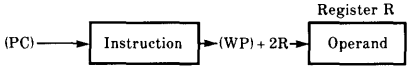
- ☐ Arithmetic, logical, comparison, or manipulation operations on data
- ☐ Loading or storage of internal registers (program counter, workspace pointer, or status)
- ☐ Data transfer between memory and external devices via the CRU
- ☐ Control functions.

Addressing Modes

S9900 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described later along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes [R, *R, *R+,@LABEL, or @TABLE (R)] are the general forms used by S9900 assemblers to select the addressing mode for register R.

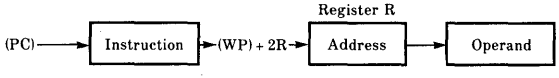
Workspace Register Addressing R

Workspace Register R contains the operand.



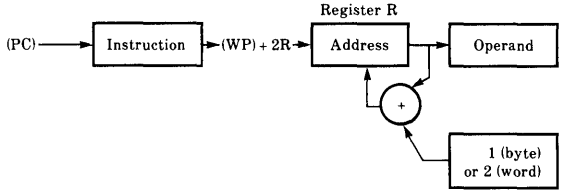
Workspace Register Indirect Addressing *R

Workspace Register R contains the address of the operand.



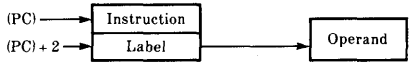
Workspace Register Indirect Auto Increment Addressing *R+

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace Register R are incremented.



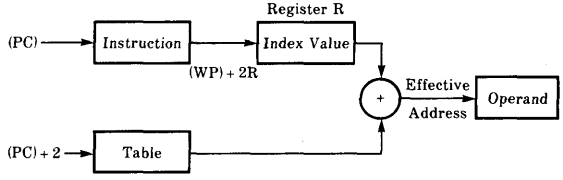
Symbolic (Direct) Addressing @LABEL

The word following the instruction contains the address of the operand.



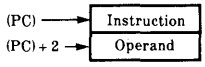
Indexed Addressing @TABLE (R)

The word following the instruction contains the base address. Workspace Register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



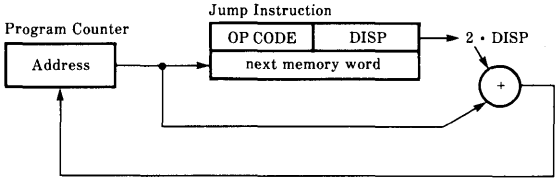
Immediate Addressing

The word following the instruction contains the operand.



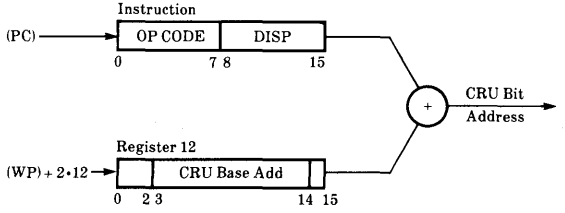
Program Counter Relative Addressing

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multiplied by 2 and added to the updated contents of the program counter. The result is placed in the PC.



CRU Relative Addressing

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace Register 12). The result is the CRU address of the selected CRU bit.



Terms and Definitions

The following terms are used in describing the instructions of the S9900:

TERM	DEFINITION
B	Byte indicator (1 = byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
W	Workspace register
WRn	Workspace register n
(n)	Contents of n
a→b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
$\overline{n}$	Logical complement of n

Status Register

The status register contains the interrupt mask level and information pertaining to the instruction operation.

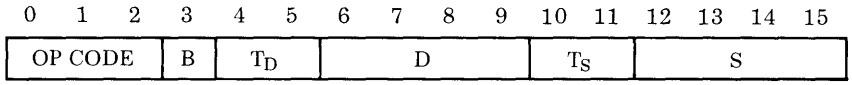
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ST0	ST1	ST2	ST3	ST4	ST5	ST6	not used (=0)					ST12	ST13	ST14	ST15
L>	A>	=	C	O	P	X						Interrupt Mask			

Bit	Name	Instruction	Condition to Set Bit to 1
ST0	LOGICAL GREATER THAN	C, CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 1 and MSB of IOP = 0, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C, CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 1
		CI	If MSB(W) = 0 and MSB of IOP = 1, or if MSB(W) = MSB of IOP and MSB of [IOP-(W)] = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0
ST2	EQUAL	C, CB	If (SA) = (DA)
		CI	If (W) = IOP
		COC	If (SA) and $(\overline{DA})$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All Others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(W) = MSB of IOP and MSB of result ≠ MSB(W)
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA)-(SA)] = 0
		ABS, NEG	If (SA) = 8000_{16}
ST5	PARITY	CB, MOVB LDCR, STCR	If (SA) has odd number of 1's If $1 \leq C \leq 8$ and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12-ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

Instructions

Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand

General format:



If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

The addressing mode for each operand is determined by the T field of that operand.

T_S or T_D	S or D	Addressing Mode	Notes
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

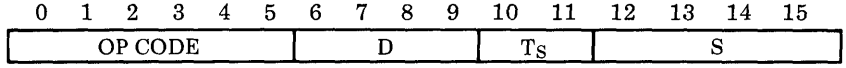
Notes:

1. *When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.*
2. *Workspace register 0 may not be used for indexing.*
3. *The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).*
4. *When $T_S = T_D = 10$, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.*

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	(SA)+(DA)→(DA)
AB	1 0 1	1	Add bytes	Yes	0-5	(SA)+(DA)→(DA)
C	1 0 0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	(DA) − (SA)→(DA)
SB	0 1 1	1	Subtract bytes	Yes	0-5	(DA) − (SA)→(DA)
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA)→(DA)
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA)→(DA)
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	(DA) AND $(\overline{SA})$→(DA)
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND $(\overline{SA})$→(DA)
MOV	1 1 0	0	Move	Yes	0-2	(SA)→(DA)
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	(SA)→(DA)

Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination

General format:



The addressing mode for the source operand is determined by the T_S field.

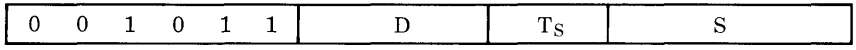
T_S	S	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	
10	1, 2, . . . 15	Indexed	1
11	0, 1, . . . 15	Workspace register indirect auto increment	2

NOTES: 1. Workspace register 0 may not be used for indexing.
2. The workspace register is incremented by 2.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeros corresponding	No	2	Test (D) to determined if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D)⊕(SA)→(D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D+1 (least significant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D+1) by unsigned (SA). Quotient → (D), remainder → (D+1). If D = 15, the next word in memory after WR15 will be used for the remainder.

Extended Operation (XOP) Instruction

General format:



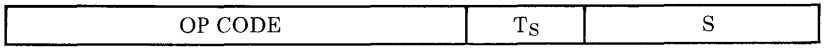
The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow$ (WP)
$(42_{16} + 4D) \rightarrow$ (PC)
SA → (new WR11)
(old WP) → (new WR13)
(old PC) → (new WR14)
(old ST) → (new WR15)

The S9900 does not test interrupt requests ($\overline{\text{INTREQ}}$) upon completion of the XOP instruction.

Single Operand Instructions

General format:



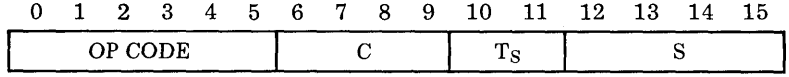
The T_S and S fields provide multiple mode addressing capability for the source operand.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	—	SA→(PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	—	(PC)→(WR11); SA→(PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	—	(SA)→(WP); (SA+2)→(PC); (old WP)→(new WR13); (old PC)→(new WR14); (old ST)→(new WR15); the interrupt input ($\overline{\text{INTREQ}}$) is not tested upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	—	0→(SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	—	$FFFF_{16}$→(SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	$(\overline{SA})$→(SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	−(SA)→(SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	|(SA)|→(SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	—	(SA), bits 9 thru 7→(SA), bits 8 thru 15; (SA), bits 8 thru 15 → (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA)+1→(SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA)+2→(SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA)−1→(SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA)−2→(SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	—	Execute the instruction at SA.

**Operand is compared to zero for status bit.*
†If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the S9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

CRU Multiple-Bit Instructions

General format:



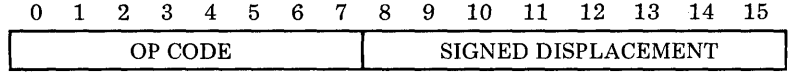
The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 3 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in teh workspace register indirect auto increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	0 0 1 1 0 0	Load communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†ST5 is affected only if $1 \leqslant C \leqslant 8$.

CRU Single-Bit Instructions

General format:

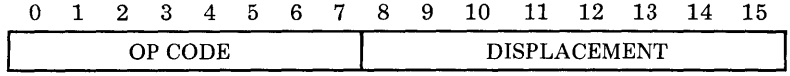


CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7	MEANING	STATUS BITS AFFECTED	DESCRIPTION
SBO	0 0 0 1 1 1 0 1	Set bit to one	—	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	—	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit=1, set ST2.

Jump Instructions

General format:

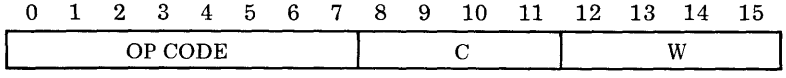


Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of −128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instruction.

MNEMONIC	OP CODE 0	1	2	3	4	5	6	7	MEANING	ST CONDITION TO LOAD PC
JEQ	0	0	0	1	0	0	1	1	Jump equal	ST2 = 1
JGT	0	0	0	1	0	1	0	1	Jump greater than	ST1 = 1
JH	0	0	0	1	1	0	1	1	Jump high	ST0 = 1 and ST2 = 0
JHE	0	0	0	1	0	1	0	0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0	0	0	1	1	0	1	0	Jump low	ST0 = 0 and ST2 = 0
JLE	0	0	0	1	0	0	1	0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0	0	0	1	0	0	0	1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0	0	0	1	0	0	0	0	Jump unconditional	unconditional
JNC	0	0	0	1	0	1	1	1	Jump no carry	ST3 = 0
JNE	0	0	0	1	0	1	1	0	Jump not equal	ST2 = 0
JNO	0	0	0	1	1	0	0	1	Jump no overflow	ST4 = 0
JOC	0	0	0	1	1	0	0	0	Jump on carry	ST3 = 1
JOP	0	0	0	1	1	1	0	0	Jump odd parity	ST5 = 1

Shift Instructions

General format:

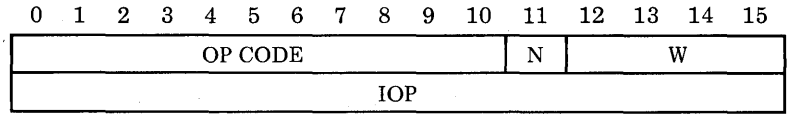


If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

MNEMONIC	OP CODE 0	1	2	3	4	5	6	7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0	0	0	0	1	0	1	0	Shift left arithmetic	Yes	0-4	Shift (W) left. Fill vacated bit positions with 0.
SRA	0	0	0	0	1	0	0	0	Shift right arithmetic	Yes	0-3	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	0	0	0	0	1	0	1	1	Shift right circular	Yes	0-3	Shift (W) right. Shift previous LSB into MSB.
SRL	0	0	0	0	1	0	0	1	Shift right logical	Yes	0-3	Shift (W) right. Fill vacated bit positions with 0's.

Immediate Register Instructions

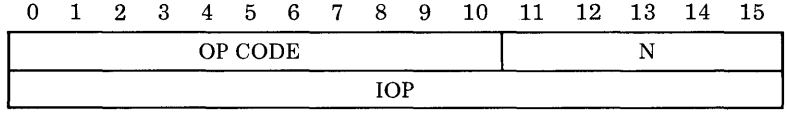
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(W)+IOP→(W)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(W) AND IOP→(W)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP→(W)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(W) OR IOP→(W)

Internal Register Load Immediate Instructions

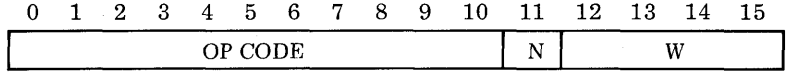
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP→(WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15→ST12 thru ST15

Internal Register Store Instructions

General format:



No ST bits are affected.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST)→(W)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP)→(W)

Return Workspace Pointer (RTWP) Instruction

General format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	1	1	1	0	0	N				

The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

External Instructions

General format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
OP CODE											N				

External instructions cause the three most-significant address lines (A0 through A2) to be set to the below described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS A0 A1 A2
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	—	Suspend S9900 instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L H L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12-15	0→ST12 through ST15	L H H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		—	H H L
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		—	H L H
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		—	H H H

S9900 Instruction Execution Times

Instruction execution times for the S9900 are a function of:

1) Clock cycle time, $t_{c(\phi)}$
2) Addressing mode used where operands have multiple addressing mode capability
3) Number of wait states required per memory access.

Table 3 lists the number of clock cycles and memory accesses required to execute each S9900 instruction. For instructions with multiple addressing modes for either or both operands, the table lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the

Table 3. Instruction Execution Times

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	DEST
A	14	4	A	A
AB	14	4	B	B
ABS (MSB = 0)	12	2	A	–
(MSB = 1)	14	4	A	–
AI	14	4	–	–
ANDI	14	4	–	–
B	8	2	A	–
BL	12	3	A	–
BLWP	26	6	A	–
C	14	3	A	A
CB	4	3	B	B
CI	14	3	–	–
CKOF	12	1	–	–
CKON	12	1	–	–
CLR	10	3	A	–
COC	14	3	A	–
CZC	14	3	A	–
DEC	10	3	A	–
DECT	10	3	A	–
DIV (ST4 is set)	16	3	A	–
DIV (ST4 is reset)*	92-124	6	A	–
IDLE	12	1	–	–
INC	10	3	A	–
INCT	10	3	A	–
INV	10	3	A	–
Jump (PC is changed)	10	1	–	–
(PC is not changed)	8	1	–	–
LDCR (C = 0)	52	3	A	–
(1≤C≤8)	20+2C	3	B	–
(9≤C≤15)	20+2C	3	A	–
LI	12	3	–	–
LIMI	16	2	–	–
LREX	12	1	–	–
$\overline{\text{RESET}}$ function	26	5	–	–
$\overline{\text{LOAD}}$ function	22	5	–	–
Interrupt context switch	22	5	–	–

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION† SOURCE	DEST
LWPI	10	2	–	–
MOV	14	4	A	A
MOVB	14	4	B	B
MPY	52	5	A	–
NEG	12	3	A	–
ORI	14	4	–	–
RSET	12	1	–	–
RTWP	14	4	–	–
S	14	4	A	A
SB	14	4	B	B
SBO	12	2	–	–
SBZ	12	2	–	–
SETO	10	3	A	–
Shift (C≠0)	12+2C	3	–	–
(C=0, Bits 12-15 of WR0=0)	52	4	–	–
(C=0, Bits 12-15 of WRP=N≠0)	20+2N	4	–	–
SOC	14	4	A	A
SOCB	14	4	B	B
STCR (C=0)	60	4	A	–
(1≤C≤7)	42	4	B	–
(C=8)	44	4	B	–
(9≤C≤15)	58	4	A	–
STST	8	2	–	–
STWP	8	2	–	–
SWPB	10	3	A	–
SZC	14	4	A	A
SZCB	14	4	B	B
TB	12	2	–	–
X**	8	2	A	–
XOP	36	8	A	–
XOR	14	4	A	–
Undefined op codes 0000-01FF, 0320-033F, 0C00-0FFF, 0780-07FF	6	1	–	–

*Execution time is dependent upon the partial quotient after each clock cycle during execution.

**Execution time is added to the execution time of the instruction located at the source address minus 4 clock cycles and 1 memory access time.

†The letters A and B refer to the respective tables that follow.

Table A Address Modification

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	8	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D≠0)	8	2

Table B Address Modification

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D =00)	0	0
WR indirect (T_S or T_D = 01)	4	1
WR indirect auto-increment (T_S or T_D = 11)	6	2
Symbolic (T_S or T_D = 10, S or D = 0)	8	1
Indexed (T_S or T_D = 10, S or D≠0)	8	2

appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$T = t_{c(\phi)} (C + W \cdot M)$

where:

- T = total instruction execution time;
- $t_{c(\phi)}$ = clock cycle time;
- C = number of clock cycles for instruction execution plus address modification;
- W = number of required wait states per memory access for instruction execution plus address modification — no wait states used unless accessing slow memory;
- M = number of memory accesses.

As an example, the instruction MOVB is used in a system with $t_{c(\phi)} = 0.333\ \mu s$ and no wait states are required to access memory. Both operands are addressed in the workspace register mode:

$T = t_{c(\phi)} (C + W \cdot M) = 0.333\ (14 + 0 \cdot 4)\ \mu s = 4.662 \mu s.$

If two wait states per memory access were required, the execution time is:

$$T = 0.333\ (14 + 2 \cdot 4)\ \mu s = 7.326 \mu s.$$

If the source operand was addressed in the symbolic mode and two wait states were required:

$T = t_{c(\phi)} (C + W \cdot M)$

$C = 14 + 8 = 22$

$M = 4 + 1 = 5$

$T = 0.333\ (22 + 2 \cdot 5)\ \mu s = 10.656 \mu s.$

System Design Examples

Figure 13 illustrates a typical minimum S9900 system. Eight bits of input and output interface are implemented. The memory system contains 1024x16 ROM and 1024x16 RAM memory blocks. The total package count for this system is 13 packages.

A maximum S9900 microprocessor system is illustrated in Figure 14. ROM and RAM are both shown for a total of 65,536 bytes of memory. The I/O interface supports 4096-output bits and 4096-input bits. Fifteen external interrupts are implemented in the interrupt interface. The clock generator and control section contains memory decode logic, synchronization logic, and the clock electronics. Bus buffers, required for this maximally configured system, are indicated on the system buses.

Figure 13. Minimum S9900 System

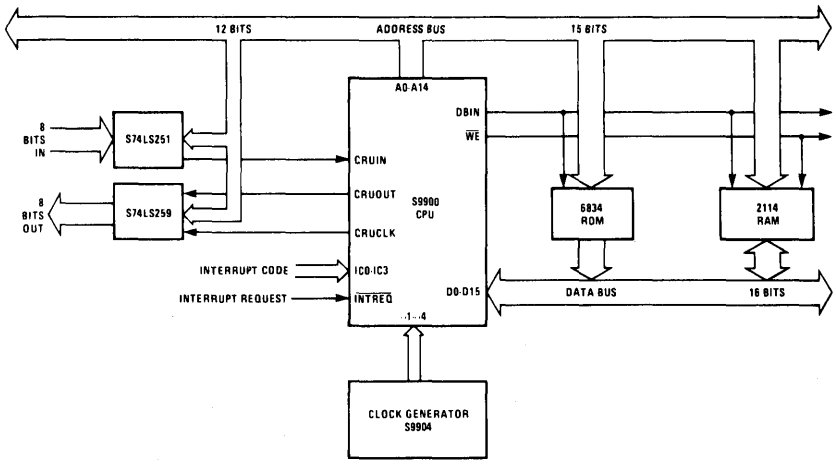
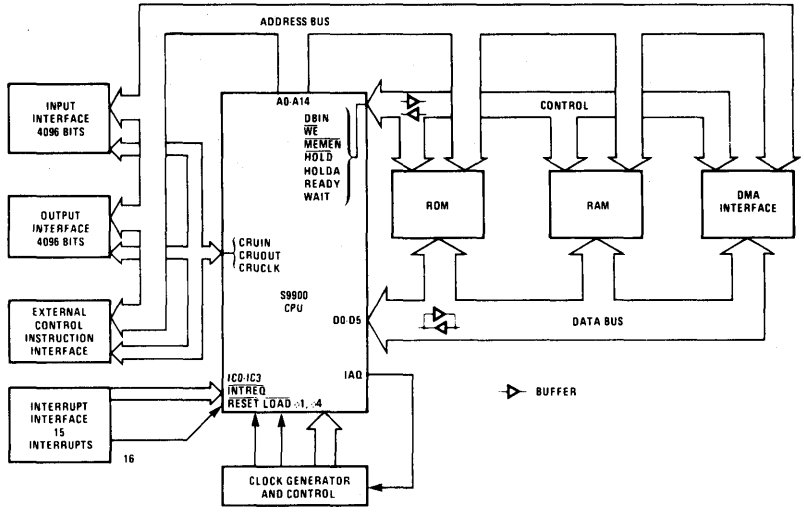


Figure 14. Maximum S9900 System



Instruction Summary

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
A	A000	1	Y	0-4	ADD(WORD)
AB	B000	1	Y	0-5	ADD(BYTE)
ABS	0740	6	Y	0-4	ABSOLUTE VALUE
AI	0220	8	Y	0-4	ADD IMMEDIATE
ANDI	0240	8	Y	0-2	AND IMMEDIATE
B	0440	6	N	–	BRANCH
BL	0680	6	N	–	BRANCH AND LINE (W11)
BLWP	0400	6	N	–	BRANCH LOAD WORKSPACE POINTER
C	8000	1	N	0-2	COMPARE (WORD)
CB	9000	1	N	0-2,5	COMPARE (BYTE)
CI	0280	8	N	0-2	COMPARE IMMEDIATE
CKOF	03C0	7	N	–	EXTERNAL CONTROL
CKON	03A0	7	N	–	EXTERNAL CONTROL
CLR	04C0	6	N	–	CLEAR OPERAND
COC	2000	3	N	2	COMPARE ONES CORRESPONDING
CZC	2400	3	N	2	COMPARE ZEROES CORRESPONDING
DEC	0600	6	Y	0-4	DECREMENT (BY ONE)
DECT	0640	6	Y	0-4	DECREMENT (BY TWO)
DIV	3C00	9	N	4	DIVIDE
IDLE	0340	7	N	–	COMPUTER IDLE
INC	0580	6	Y	0-4	INCREMENT (BY ONE)
INCT	05C0	6	Y	0-4	INCREMENT (BY TWO)
INV	0540	6	Y	0-2	INVERT (ONES COMPLEMENT)
JEQ	1300	2	N	–	JUMP EQUAL (ST2=1)
JGT	1500	2	N	–	JUMP GREATER THAN (ST1=1)
JH	1800	2	N	–	JUMP HIGH (ST0=1 AND ST2=0)
JHE	1400	2	N	–	JUMP HIGH OR EQUAL (ST0 OR ST2=1)
JL	1A00	2	N	–	JUMP LOW (ST0 AND ST2=0)
JLE	1200	2	N	–	JUMP LOW OR EQUAL (ST0=0 OR ST2=1)
JLT	1100	2	N	–	JUMP LESS THAN (ST1 AND ST2=0)
JMP	1000	2	N	–	JUMP UNCONDITIONAL
JNC	1700	2	N	–	JUMP NO CARRY (ST3=0)
JNE	1600	2	N	–	JUMP NOT EQUAL (ST2=0)
JNO	1900	2	N	–	JUMP NO OVERFLOW (ST4=0)
JOC	1800	2	N	–	JUMP ON CARRY (ST3=1)
JOP	1C00	2	N	–	JUMP ODD PARITY (ST5=1)
LDCR	3000	4	Y	0-2,5	LOAD CRU
LI	0200	8	N	0-2	LOAD IMMEDIATE
LIMI	0300	8	N	12-15	LOAD IMMEDIATE TO INTERRUPT MASK
LREX	03E0	7	N	12-15	EXTERNAL CONTROL
LWPI	02E0	8	N	–	LOAD IMMEDIATE TO WORKSPACE POINTER
MOV	C000	1	Y	0-2	MOVE (WORD)
MOVB	D000	1	Y	0-2,5	MOVE (BYTE)
MPY	3800	9	N	–	MULTIPLY

Instruction Summary (Continued)

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
NEG	0500	6	Y	0-4	NEGATE (TWO'S COMPLEMENT)
ORI	0260	8	Y	0-2	OR IMMEDIATE
RSET	0360	7	N	12-15	EXTERNAL CONTROL
RTWP	0380	7	N	0-6, 12-15	RETURN WORKSPACE POINTER
S	6000	1	Y	0-4	SUBTRACT (WORD)
SB	7000	1	Y	0-5	SUBTRACT (BYTE)
SBO	1D00	2	N	–	SET CRU BIT TO ONE
SBZ	1E00	2	N	–	SET CRU BIT TO ZERO
SETO	0700	6	N	–	SET ONES
SLA	0A00	5	Y	0-4	SHIFT LEFT (ZERO FILL)
SOC	E000	1	Y	0-2	SET ONES CORRESPONDING (WORD)
SOCB	F000	1	Y	0-2,5	SET ONES CORRESPONDING (BYTE)
SRA	0800	5	Y	0-3	SHIFT RIGHT (MSB EXTENDED)
SRC	0B00	5	Y	0-3	SHIFT RIGHT CIRCULAR
SRL	0900	5	Y	0-3	SHIFT RIGHT (LEADING ZERO FILL)
STCR	3400	4	Y	0-2,5	STORE FROM CRU
STST	02C0	8	N	–	STORE STATUS REGISTER
STWP	02A0	8	N	–	STORE WORKSPACE POINTER
SWPB	06C0	6	N	–	SWAP BYTES
SZC	4000	1	Y	0-2	SET ZEROES CORRESPONDING (WORD)
SZCB	5000	1	Y	0-2,5	SET ZEROES CORRESPONDING (BYTE)
TB	1F00	2	N	2	TEST CRU BIT
X	0480	6	N	–	EXECUTE
XOP	2C00	9	N	6	EXTENDED OPERATION
XOR	2800	3	Y	0-2	EXCLUSIVE OR

ILLEGAL OP CODES 0000-01FF, 0320-033F, 0780-07FF, 0C00-0FFF

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S9980A/S9981

16-BIT MICROPROCESSOR

Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 16,384 Bytes of Memory
- ☐ 8-Bit Memory Data Bus
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O, and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 4 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ On-Chip 4-Phase Clock Generator
- ☐ 40-Pin Package
- ☐ N-Channel Silicon-Gate Technology

The S9980A and the S9981 although very similar, have several differences which are:

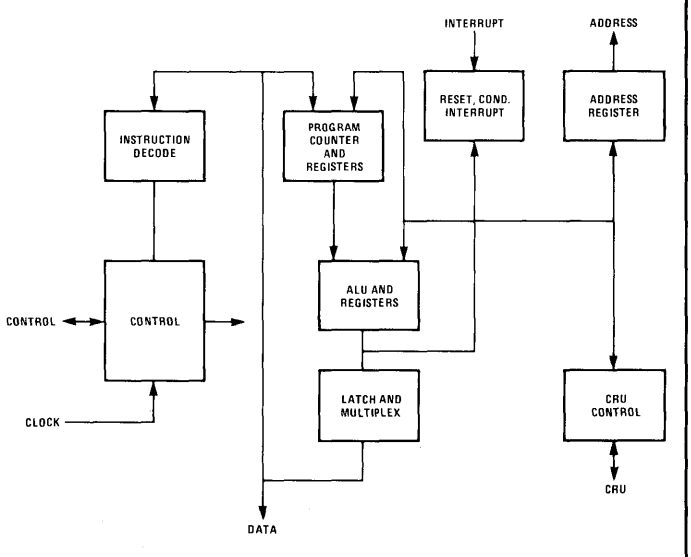
1. The S9980A requires a V_{BB} supply (pin 21) while the S9981 has an internal charge pump to generate V_{BB} from V_{CC} and V_{DD}.
2. The S9981 has an optional on-chip crystal oscillator in addition to the external clock mode of the S9980A.
3. The pin-outs are not compatible for D0-D7, INT0-INT2, and $\overline{\phi}3$.

Description

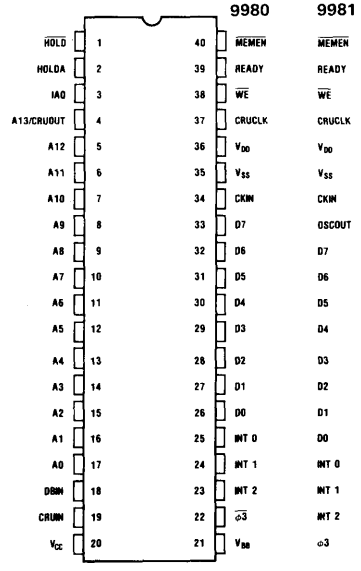
The S9980A/S9981 is a software-compatible member of AMI's 9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the S9980A/S9981 is a single-chip 16-bit central processing unit (CPU) which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package (see Figure 1). The instruction set of the S9980A/S9981 includes the capabilities offered by full minicomputers and is exactly the same as the 9900's. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort.

S9900

Block Diagram



Pin Configuration



S9980A/S9981 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) ..... −0.3V to 15V
Supply voltage, V_{DD} (see Note 1) ..... −0.3V to 15V
Supply voltage, V_{BB} (see Note 1) (9980A only) ..... −5.25V to 0V
All input voltages (see Note 1) ..... −0.3V to 15V
Output voltage (see Note 1) ..... −2V to 7V
Continuous power dissipation 1.4W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage (9980A only)	−5.25	−5	−4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage	2.2	2.4	$V_{CC}+1$	V	
V_{IL}	Low-level input voltage	−1	0.4	0.8	V	
T_A	Operating free-air temperature	0	20	70	°C	

Electrical Characteristics Over full Range of Recommended Operating Conditions (unless otherwise noted)

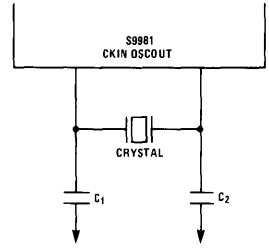
Symbol	Parameter		Min.	Typ.*	Max.	Unit	Conditions
I_I	Input current	Data bus during DBIN			±75	μA	$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, $\overline{DBIN}$ during HOLDA			±75	μA	$V_I = V_{SS}$ to V_{CC}
		Any other inputs			±10	μA	$V_I = V_{SS}$ to V_{CC}
V_{OH}	High-level output voltage		2.4			V	$I_O = -0.4$mA
V_{OL}	Low-level output voltage				0.5 0.65	V	$I_O = 2$mA $I_O = 3.2$mA
I_{BB}	Supply current from V_{BB} (9980A only)				1	mA	
I_{CC}	Supply current from V_{CC}			50 40	60 50	mA	0°C 70°C
I_{DD}	Supply current from V_{DD}			70 65	80 75	mA	0°C 70°C
C_I	Input capacitance (any inputs except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			25		pF	f = 1MHz, unmeasured pins at V_{SS}
C_O	Output capacitance (any output except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}

*All typical values are at T_A = 25°C and nominal voltages.

Clock Characteristics

The S9980A and S9981 have an internal 4-phase clock generator/driver. This is driven by an external TTL compatible signal to control the phase generation. In addition, the S9981 provides an output (OSCOUT) that in conjunction with CKIN forms an on-chip crystal oscillator. This oscillator requires an external crystal and two capacitors as shown in Figure 1. The external signal or crystal must be 4 times the desired system frequency.

Figure 1. Crystal Oscillator Circuit



Internal Crystal Oscillator (9981 Only)

The internal crystal oscillator is used as shown in Figure 1. The crystal should be a fundamental series resonant type. C_1 and C_2 represent the total capacitance on these pins including strays and parasitics.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	Crystal frequency	6		10	MHz	0°C-70°C
	C_1,C_2	10	15	25	pF	0°C-70°C

External Clock

The external clock on the S9980A and optional on the S9981, uses the CKIN pin. In this mode the OSCOUT pin of the S9981 must be left floating. The external clock source must conform to the following specifications.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{ext}	External source frequency*	6		10	MHz	
V_H	External source high level	2.2			V	
V_L	External source low level			0.8	V	
T_r/T_f	External source rise/fall time		10		ns	
T_{WH}	External source high level pulse width	40			ns	
T_{WL}	External source low level pulse width	40			ns	

*This allows a system speed of 1.5MHz to 2.5MHz

Switching Characteristics Over Full Range of Recommended Operating Conditions

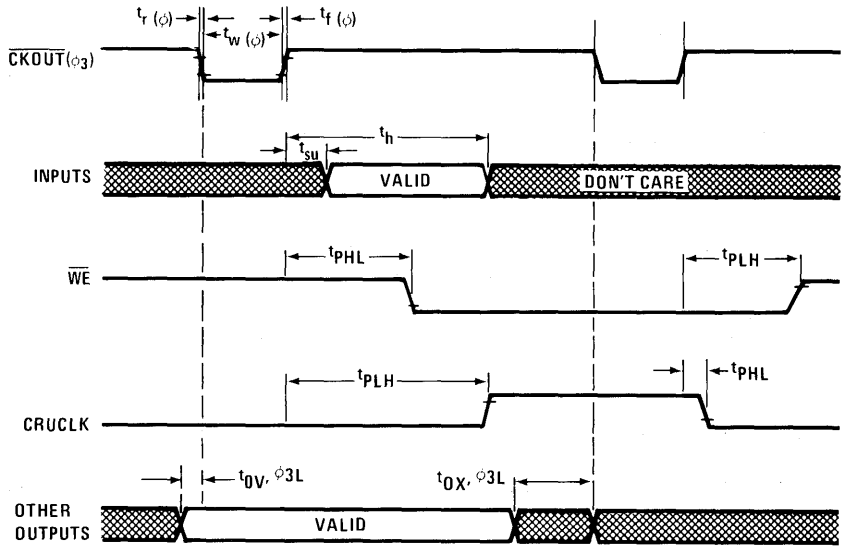
The timing of all the inputs and outputs is controlled by the internal 4 phase clock; thus all timings are based on the width of one phase of the internal clock. This is $1/f_{(CKIN)}$ (whether driven or from a crystal). This is also $\frac{1}{4} f_{system}$. In the following table this phase time is denoted t_w.

All external signals are with reference to $\phi 3$ (see Figure 2).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$t_r(\phi 3)$	Rise time of $\phi 3$	3	5	10	ns	
$t_f(\phi 3)$	Fall time of $\phi 3$	5	7.5	15	ns	
$t_w(\phi 3)$	Pulse width of $\phi 3$	$t_w - 15$	$t_w - 10$	$t_w + 10$	ns	
t_{su}	Data or control setup time*	$t_w - 30$			ns	
t_h	Data hold time*	$2t_{tw} + 10$			ns	
t_{PHL} ($\overline{WE}$)	Propagation delay time WE high to low	$t_w - 10$	t_w	$t_w + 20$	ns	tw = 1/f(CKIN) = ¼ f_{system}
t_{PLH} ($\overline{WE}$)	Propagation delay time WE low to high	t_w	$t_w + 10$	$t_w + 30$	ns	
t_{PHL} (CRUCLK)	Propagation delay time, CRUCLK high to low	− 20	− 10	+ 10	ns	C_L = 200pf
t_{PLH} (CRUCLK)	Propagation delay time, CRUCLK low to high	$2t_w - 10$	$2t_w$	$2t_w + 20$	ns	
t_{OV}	Delay time from output valid to $\phi 3$ low	$t_w - 50$	$t_w - 30$		ns	
t_{OX}	Delay time from output invalid to $\phi 3$ low		$t_w - 20$	t_w	ns	

*All inputs except IC0-IC2 must be synchronized to meet these requirements. IC0-IC2 may change asynchronously.

Figure 2. External Signal Timing Diagram



S9980A Pin Description

Table 1 defines the S9980A pin assignments and describes the function of each pin.

Table 1. S9980A Pin Assignments and Functions

Signature	Pin	I/O	Description
A0 (MSB)	17	OUT	**ADDRESS BUS**
A1	16	OUT	A0 through A13 comprise the address bus. This 3-state bus provides the memory-address
A2	15	OUT	vector to the external-memory system when MEMEN is active and I/O-bit addresses and
A3	14	OUT	external-instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus
A4	13	OUT	assumes the high-impedance state when HOLDA is active.
A5	12	OUT	
A6	11	OUT	
A7	10	OUT	
A8	9	OUT	
A9	8	OUT	
A10	7	OUT	
A11	6	OUT	
A12	5	OUT	
A13/CRUOUT	4	OUT	**CRUOUT**
			Serial I/O data appears on A13 when an LDCR, SBZ and SBO instruction is executed. This data should be sampled by the I/O interface logic when CRUCLK goes active (high). One bit of the external instruction code appears on A13 during external instruction execution.
D0 (MSB)	26	I/O	**DATA BUS**
D1	27	I/O	D0 through D7 comprise the bidirectional 3-state data bus. This bus transfers memory data
D2	28	I/O	to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is ac-
D3	29	I/O	tive. The data bus assumes the high-impedance state when HOLDA is active.
D4	30	I/O	
D5	31	I/O	
D6	32	I/O	
D7 (LSB)	33	I/O	
			POWER SUPPLIES
V_{BB}	21		Supply voltage (−5V NOM)
V_{CC}	20		Supply voltage (5V NOM)
V_{DD}	36		Supply voltage (12V NOM)
V_{SS}	35		Ground reference
CKIN	34	IN	**CLOCKS**
			Clock In. A TTL compatible input used to generate the internal 4-phase clock. CKIN frequency is 4 times the desired system frequency.
$\overline{\phi 3}$	22	OUT	Clock phase 3 ($\phi 3$) inverted; used as a timing reference.
DBIN	18	OUT	**BUS CONTROL**
			Data bus in. When active (high), DBIN indicates that the S9980A has disabled its output buffers to allow the memory to place memory-read data on the data bus during MEMEN. DBIN remains low in all other cases except when HOLDA is active at which time it is in the high-impedance state.

Table 1. S9980A Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
$\overline{\text{MEMEN}}$	40	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address. When HOLDA is active, $\overline{\text{MEMEN}}$ is in the high impedance state.
$\overline{\text{WE}}$	38	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9980 to be written into memory. When HOLDA is active, $\overline{\text{WE}}$ is in the high-impedance state.
CRUCLK	37	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0, A1, A13.
CRUIN	19	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A2 through A12).
INT2 INT1 INT0	23 24 25	IN IN IN	Interrupt code. Refer to interrupt discussion for detailed description.
			MEMORY CONTROL
$\overline{\text{HOLD}}$	1	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9980A enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	2	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	39	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9980A enters a wait state and suspends internal operation until the memory systems indicated ready.
			TIMING AND CONTROL
IAQ	3	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9980A is acquiring an instruction. IAQ can be used to detect illegal op codes. It may also be used to synchronize LOAD stimulus.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before S9980 enters hold state.

S9981 Pin Description

Table 2 defines the S9981 pin assignments and describes the function of each pin.

Table 2. S9981 Pin Assignments and Functions

Signature	Pin	I/O	Description
A0 (MSB)	17	OUT	**ADDRESS BUS**
A1	16	OUT	A0 through A13 comprise the address bus. This 3-state bus provides the memory-address vector to the external-memory system when MEMEN is active and I/O-bit addresses and external-instruction addresses to the I/O system when $\overline{\text{MEMEN}}$ is inactive. The address bus assumes the high-impedance state when HOLDA is active.
A2	15	OUT	
A3	14	OUT	
A4	13	OUT	
A5	12	OUT	
A6	11	OUT	
A7	10	OUT	
A8	9	OUT	
A9	8	OUT	
A10	7	OUT	
A11	6	OUT	
A12	5	OUT	
A13/CRUOUT	4	OUT	**CRUOUT**
			Serial I/O data appears on A13 when an LDCR, SBZ and SBO instruction is executed. This data should be sampled by the I/O interface logic when CRUCLK goes active (high). One bit of the external instruction code appears on A13 during external instruction execution.
D0 (MSB)	25	I/O	**DATA BUS**
D1	26	I/O	D0 through D7 comprise the bidirectional 3-state data bus. This bus transfers memory data to (when writing) and from (when reading) the external-memory system when $\overline{\text{MEMEN}}$ is active. The data bus assumes the high-impedance state when HOLDA is active.
D2	27	I/O	
D3	28	I/O	
D4	29	I/O	
D5	30	I/O	
D6	31	I/O	
D7 (LSB)	32	I/O	
			POWER SUPPLIES
V_{CC}	20		Supply voltage (5V NOM)
V_{DD}	36		Supply voltage (12V NOM)
V_{SS}	35		Ground reference
CKIN	34	IN	**CLOCKS**
OSCOUT	33	OUT	Clock In and Oscillator Out. These pins may be used in either of two modes to generate the internal 4-phase clock. In mode 1 a crystal of 4 times the desired system frequency is connected between CKIN and OSCOUT (see Figure 13). In mode 2 OSCOUT is left floating and CKIN is driven by a TTL compatible source whose frequency is 4 times the desired system frequency.
$\overline{\phi 3}$	21	OUT	Clock phase 3 ($\phi 3$) inverted; used as a timing reference.
DBIN	18	OUT	**BUS CONTROL**
			Data bus in. When active (high), DBIN indicates that the S9981 has disabled its output buffers to allow the memory to place memory-read data on the data bus during $\overline{\text{MEMEN}}$. DBIN remains low in all other cases except when HOLDA is active at which time it is in the high-impedance state.

Table 2. S9981 Pin Assignments and Functions (Continued)

Signature	Pin	I/O	Description
$\overline{\text{MEMEN}}$	40	OUT	Memory enable. When active (low), $\overline{\text{MEMEN}}$ indicates that the address bus contains a memory address. When HOLDA is active, $\overline{\text{MEMEN}}$ is in the high impedance state.
$\overline{\text{WE}}$	38	OUT	Write enable. When active (low), $\overline{\text{WE}}$ indicates that memory-write data is available from the S9981 to be written into memory. When HOLDA is active, $\overline{\text{WE}}$ is in the high-impedance state.
CRUCLK	37	OUT	CRU clock. When active (high), CRUCLK indicates that external interface logic should sample the output data on CRUOUT or should decode external instructions on A0, A1, A13.
CRUIN	19	IN	CRU data in. CRUIN, normally driven by 3-state or open-collector devices, receives input data from external interface logic. When the processor executes a STCR or TB instruction, it samples CRUIN for the level of the CRU input bit specified by the address bus (A2 through A12).
INT2	22	IN	Interrupt code. Refer to interrupt discussion for detailed description.
INT1	23	IN	
INT0	24	IN	
			MEMORY CONTROL
$\overline{\text{HOLD}}$	1	IN	Hold. When active (low), $\overline{\text{HOLD}}$ indicates to the processor that an external controller (e.g., DMA device) desires to utilize the address and data buses to transfer data to or from memory. The S9981 enters the hold state following a hold signal when it has completed its present memory cycle.* The processor then places the address and data buses in the high-impedance state (along with $\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) and responds with a hold-acknowledge signal (HOLDA). When $\overline{\text{HOLD}}$ is removed, the processor returns to normal operation.
HOLDA	2	OUT	Hold acknowledge. When active (high), HOLDA indicates that the processor is in the hold state and the address and data buses and memory control outputs ($\overline{\text{WE}}$, $\overline{\text{MEMEN}}$, and DBIN) are in the high-impedance state.
READY	39	IN	Ready. When active (high), READY indicates that memory will be ready to read or write during the next clock cycle. When not-ready is indicated during a memory operation, the S9981 enters a wait state and suspends internal operation until the memory systems indicated ready.
			TIMING AND CONTROL
IAQ	3	OUT	Instruction acquisition. IAQ is active (high) during any memory cycle when the S9981 is acquiring an instruction. IAQ can be used to detect illegal op codes. It may also be used to synchronize LOAD stimulus.

*If the cycle following the present memory cycle is also a memory cycle it, too, is completed before S9981 enters hold state.

Timing

Memory

Basic memory read and write cycles are shown in Figures 3a and 3b. Figure 3a shows a read and a write cycle with no wait states while Figure 3b shows a read and a write cycle for a memory requiring one wait state.

$\overline{\text{MEMEN}}$ goes active (low) during each memory cycle. At the same time that $\overline{\text{MEMEN}}$ is active, the memory address appears on the address bits A0 through A13. Since the S9980A/S9981 has an 8-bit data bus, every memory operation consists of two consecutive memory cycles. Address bit A13 is 0 for the first of the two cycles and goes to 1 for the second. If the cycle is a memory-read cycle, DBIN will go active (high) at the same time $\overline{\text{MEMEN}}$ and A0 through A13 become valid. The memory-write ($\overline{\text{WE}}$) signal remains inactive during a read cycle.

The READY signal allows extended memory cycle as shown in Figure 3b.

At the end of the read cycle, $\overline{\text{MEMEN}}$ and DBIN go inactive (high and low respectively). The address bus also changes at this time, however, the data bus remains in the input mode for one clock cycle after the read cycle.

A write cycle is similar to read cycle except that $\overline{\text{WE}}$ goes active (low) as shown and valid write data appears on the data bus at the same time the address appears.

Figure 3a. S9980A/S9981 Memory Bus Timing (No Wait States)

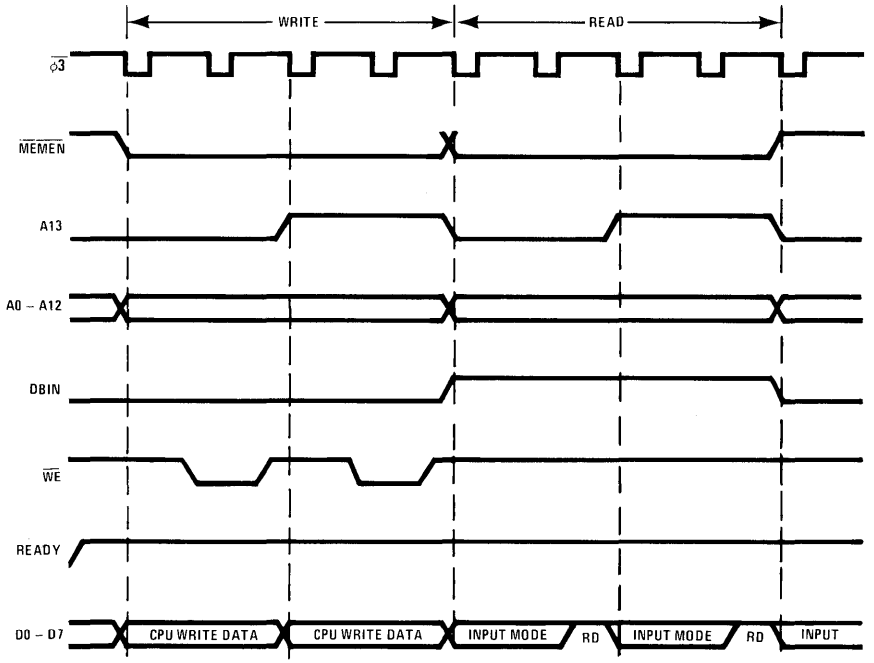
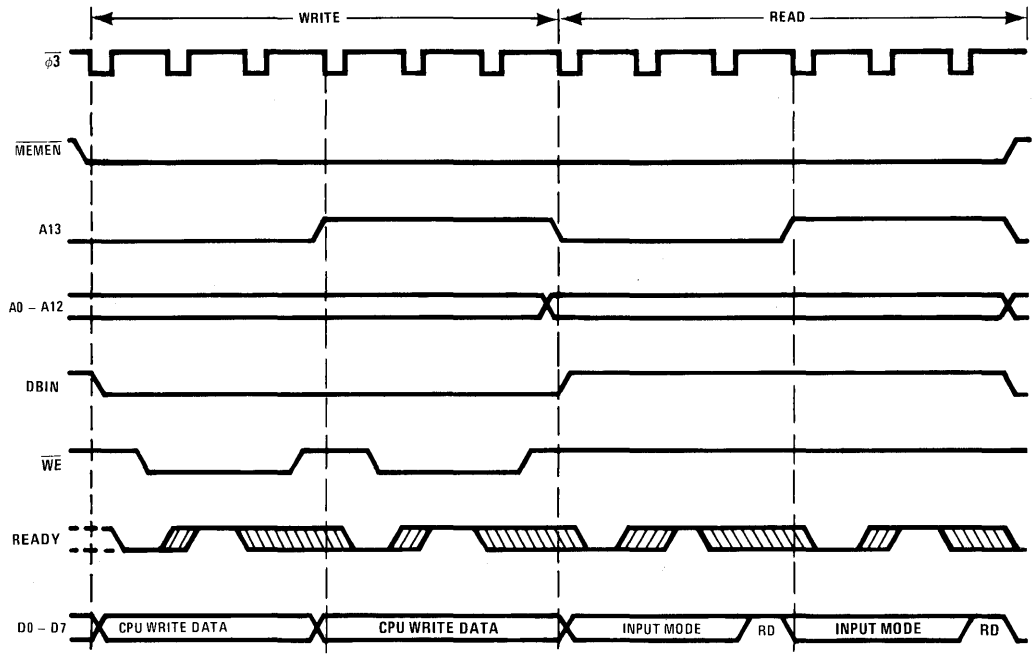


Figure 3b. S9980A/S9981 Memory Bus Timing (One Wait State)



HOLD

Other interfaces may utilize the S9980A/S9981 memory bus by using the hold operation (illustrated in Figure 4) of the S9980A/S9981. When HOLD is active (low), the S9980A/S9981 enters the hold state at the next available non-memory cycle clock period. When the S9980A/S9981 has entered the hold state HOLDA goes active (high), A0 through A13, D0 through D7, DBIN, MEMEN, and WE go into high-impedance state to allow other devices to use the memory buses. When HOLD goes inactive, S9980A/S9981 resumes processing as shown. Considering that there can be a maximum of 6 consecutive memory operations, the maximum delay between HOLD going active to HOLDA going active (high) could be $t_{c(\phi)}$ (for set up) + (12 + 6 W) $t_{c(\phi)}$ (delay for HOLDA), where W is the number of wait states per memory cycle and $t_{c(\phi)}$ is the clock cycle time. If hold occurs during a CRU operation, the S9980A/S9981 uses an extra clock cycle (after the removal of the HOLD signal) to reassert the CRU address providing the normal setup times for the CRU bit transfer that was interrupted.

CRU

CRU interface timing is shown in Figure 5. The timing for transferring two bits out and one bit in is shown. These transfers would occur during the execution of a CRU instruction. The other cycles of the instruction execution are not illustrated. To output a CRU bit, the CRU-bit address is placed on the address bus A2 through A12 and the actual bit data on A13. During the second clock cycle a CRU pulse is supplied by CRUCLK. This process is repeated until the number of bits specified by the instruction are completed.

The CRU input operation is similar in that the bit address appears on A2 through A12. During the subsequent cycle, the S9980A/S9981 accepts the bit input data as shown. No CRUCLK pulses occur during a CRU input operation.

Interrupt Code (IC0-IC2)

The S9980A/S9981 uses 4 phase clock (ϕ1, ϕ2, ϕ3, and ϕ4) for timing and control of the internal operations. IC0-IC2 are sampled during ϕ4 and then during ϕ2.

If these two successive samples are equal, the code is accepted and latched for internal use on the subsequent ϕ1. In systems with simple interrupt structures this allows the interrupt code to change asynchronously without the S9980A/S9981 accepting erroneous codes. When implementing multiple external interrupts, external synchronization of interrupt requests is required. See Figure 6 for a timing diagram. In systems with more than one external interrupt, the interrupts should be synchronized with the ϕ3 output of the S9980A/S9981 to avoid code transitions on successive sample cycles. This synchronization ensures that the S9980A/S9981 will service only the proper active interrupt level.

Figure 4. S9980A/S9981 Hold Timing

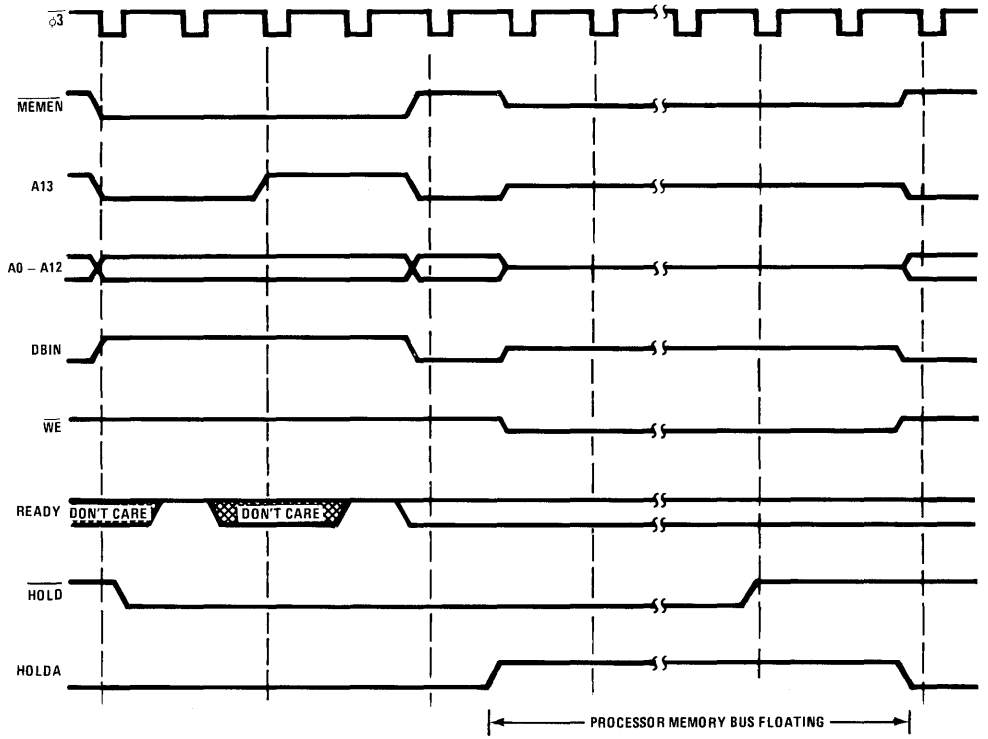


Figure 5. S9980A/S9981 CRU Interface Timing

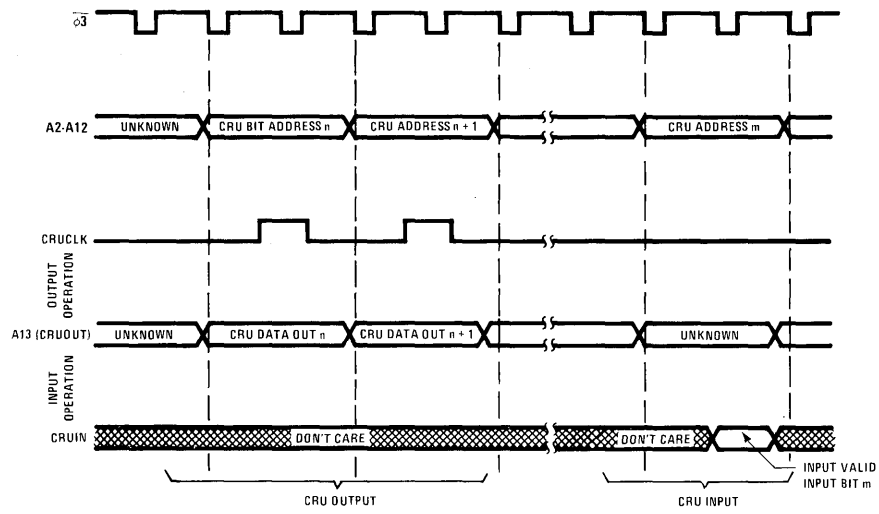
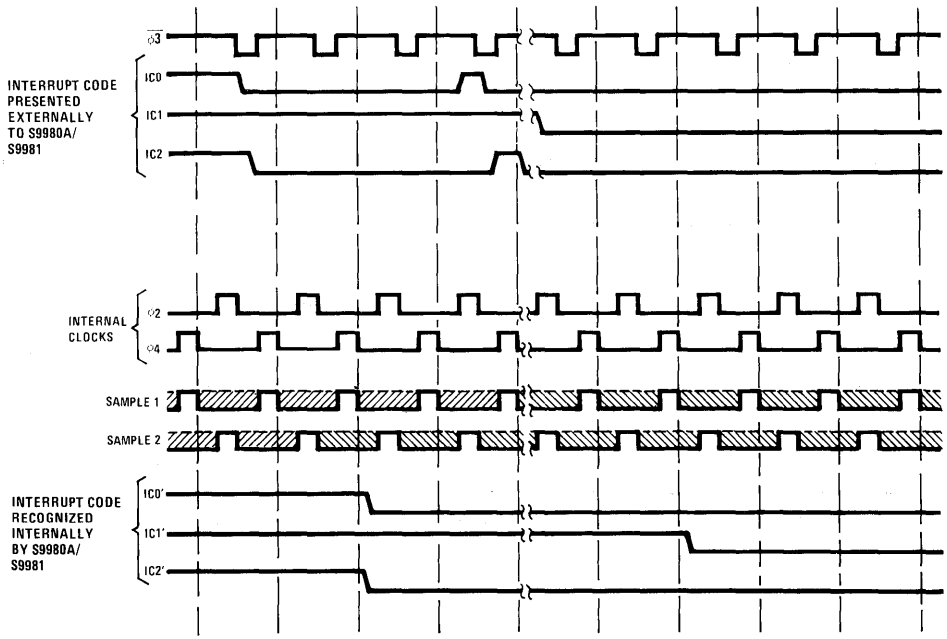


Figure 6. Interrupt Code Timing



Architecture

The S9980A/S9981 architecture is shown in Figure 7 and its operation illustrated by Figure 8.

Figure 7. Architecture

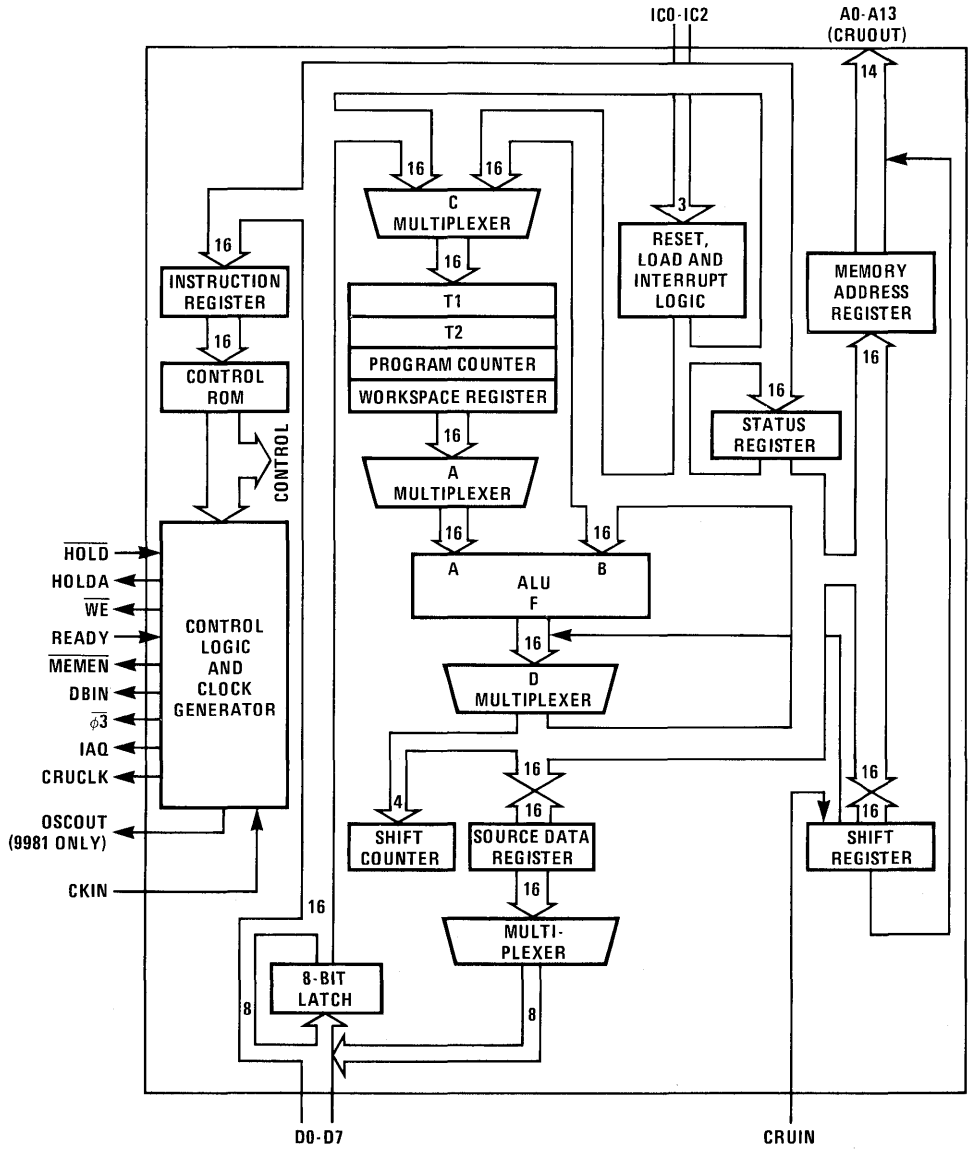
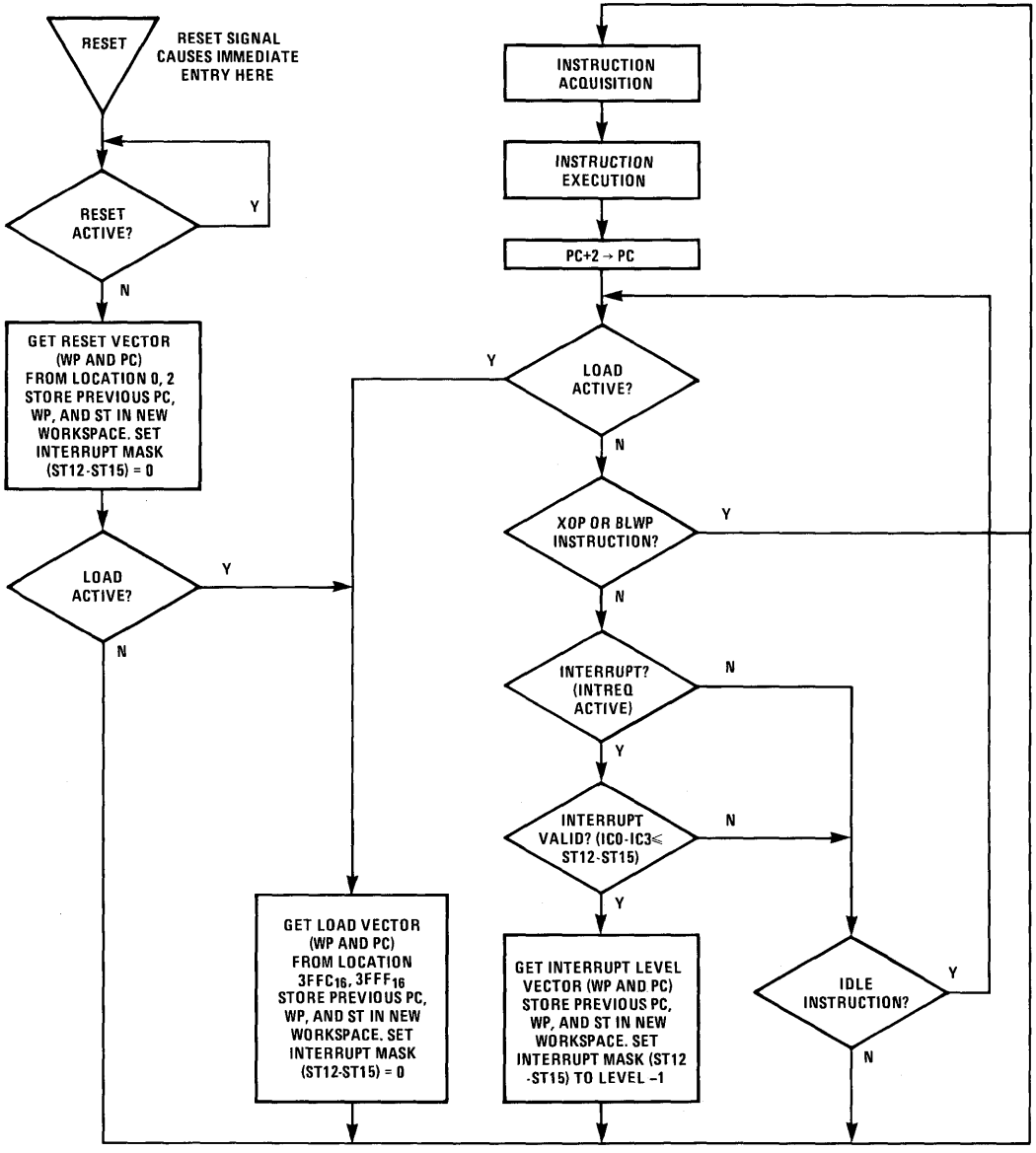
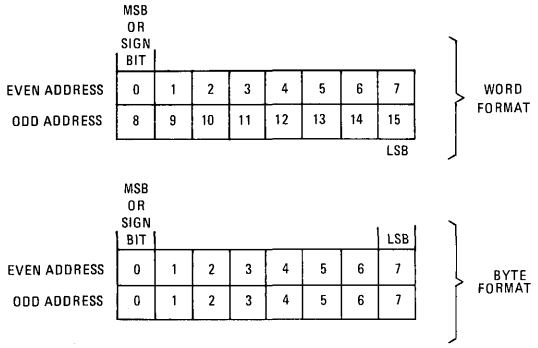


Figure 8. S9980A/S9981 CPU Flow Chart



The memory for the S9980A/S9981 is addressable in 8-bit bytes. A word is defined as 16 bits or 2 consecutive bytes in memory. The words are restricted to be on even address boundaries, i.e., the most-significant half (8 bits) resides at even address and the least-significant half resides at the subsequent odd address. A byte can reside at even or odd address. The word and byte formats are shown below.

Figure 9.



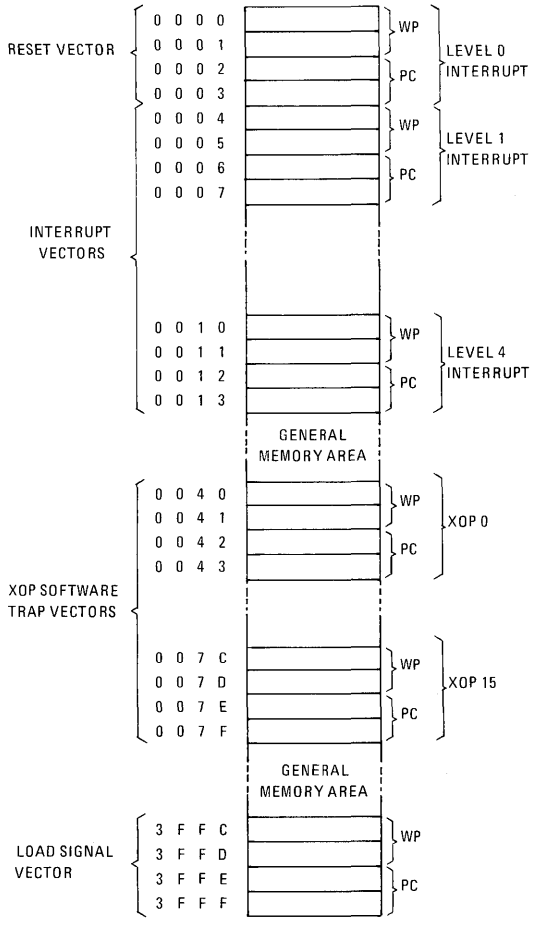
Registers and Memory

The S9980A/S9981 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal hardware registers with program-data registers. The S9980A/S9981 memory map is shown in Figure 10. The first two words (4 bytes) are used for RESET trap vector. Addresses 0004_{16} through 0013_{16} are used for interrupt vectors. Addresses 0040 through 007F are used for the extended operation (XOP) instruction trap vectors. The last four bytes at address $3FFC_{16}$ to 3FFF are used for trap vector for the LOAD function.

The remaining memory is available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

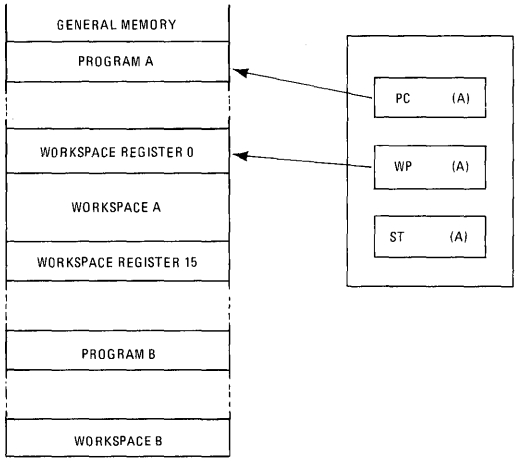
Three internal registers are accessible to the user. The program counter (PC) contains the address of the instruction following the current instruction being executed. This address is referenced by the processor to fetch the next instruction from memory and is then automatically incremented. The status register (ST) contains the present state of the processor. The workspace pointer (WP) contains the address of the first word in the currently active set of workspace registers.

Figure 10. Memory Map



NOTES: 1, INTERRUPT LEVEL 0 IS RESERVED FOR RESET.

A workspace-register file occupies 16 contiguous memory words in the general memory area. Each workspace register may hold data or addresses and function as operand registers, accumulators, address registers, or index registers. During instruction execution, the processor addresses any register in the workspace by adding the register number to the contents of the workspace pointer and initiating a memory request for the word. The relationship between the workspace pointer and its corresponding workspace is shown below.



The workspace concept is particularly valuable during operations that require a context switch, which is a change from one program environment to another (as in the case of an interrupt or call to a subroutine). Such an operation, using a conventional multi-register arrangement, requires that at least part of the contents of the register file be stored and reloaded. A memory cycle is required to store or fetch each word. By exchanging the program counter, status register, and workspace pointer, the S9980A/S9981 accomplishes a complete context switch with only six store cycles and six fetch cycles. After the switch the workspace pointer contains the starting address of a new 16-word workspace in memory for use in the new routine. A corresponding time saving occurs when the original context is restored. Instructions in the S9980A/S9981 that result in a context switch include:

1. Branch and Load Workspace Pointer (BLWP)
2. Return from Subroutine (RTWP)
3. Extended Operation (XOP)

Device interrupts, $\overline{\text{RESET}}$, and $\overline{\text{LOAD}}$ also cause a context switch by forcing the processor to trap to a service subroutine.

Interrupts

The architecture of the 9900 family allows vectoring of 16 interrupts. These interrupts are assigned levels from 0 to 15. The interrupt at level 0 has the highest priority and the interrupt at level 15 has the lowest priority. The S9900 implements all 16 interrupt levels. The S9980A/S9981 implements only 5 levels (level 0 and levels 1 through 4). Level 0 is reserved for $\overline{\text{RESET}}$ function.

Levels 1 through 4 may be used for external devices. The external levels may also be shared by several device interrupts, depending upon system requirements. The S9980A/S9981 continuously compares the interrupt code (IC0 through IC2) with the interrupt mask contained in status-register bits 12 through 15. When the level of the pending interrupt is less than or equal to the enabling mask level (higher or equal priority interrupt), the processor recognizes the interrupt and initiates a context switch following completion of the currently executing instruction. The processor fetches the new context WP and PC from the interrupt vector locations. Then, the previous context WP, PC, and ST are stored in workspace registers 13, 14, and 15, respectively, of the new workspace. The S9980A/S9981 then forces the interrupt mask to a value that is one less than the level of the interrupt being serviced. This allows only interrupts of higher priority to interrupt a service routine. The processor also inhibits interrupts until the first instruction of the service routine has been executed to allow modification of interrupt mask if needed (to mask out certain interrupts). All interrupt requests should remain active until recognized by the processor in the device-service routine. The individual service routines must reset the interrupt requests before the routine is complete. The interrupt code (IC0-IC2) may change asynchronously within the constraints specified in the timing requirements section.

If a higher priority interrupt occurs, a second context switch occurs to service the higher-priority interrupt. When that routine is complete, a return instruction (RTWP) restores the first service routine parameters to the processor to complete processing of the lower-priority interrupt. All interrupt subroutines should terminate with the return instruction to restore original program parameters. The interrupt-vector locations, device assignment, enabling mask value and the interrupt code are shown in Table 3.

Table 3. Interrupt Level Data

INTERRUPT CODE (IC0-IC2)	FUNCTION	VECTOR LOCATION (MEMORY ADDRESS IN HEX)	DEVICE ASSIGNMENT	INTERRUPT MASK VALUES TO ENABLE (ST12 THROUGH ST15)
1 1 0	Level 4	0 0 1 0	External Device	4 Through F
1 0 1	Level 3	0 0 0 C	External Device	3 Through F
1 0 0	Level 2	0 0 0 8	External Device	2 Through F
0 1 1	Level 1	0 0 0 4	External Device	1 Through F
0 0 1	Reset	0 0 0 0	Reset Stimulus	Don't Care
0 1 0	Load	3 F F C	Load Stimulus	Don't Care
0 0 0	Reset	0 0 0 0	Reset Stimulus	Don't Care
1 1 1	No-Op	—	—	—

Note that RESET and LOAD functions are also encoded on the interrupt code input lines.

Note that $\overline{\text{RESET}}$ and $\overline{\text{LOAD}}$ functions are also encoded on the interrupt code input lines.

Input/Output

The S9980A/S9981 utilizes a versatile direct command-driven I/O interface designated as the communications-register unit (CRU). The CRU provides up to 2,048 directly addressable output bits. Both input and output bits can be addressed individually or in fields of from 1 to 16 bits. The S9980A/S9981 employs CRUIN, CRUCLK, and A13 (for CRUOUT) and 11 bits (A2-A12) of the address bus to interface with the CRU system. The processor instructions that drive the CRU interface can set, reset, or test any bit in the CRU array or move between memory and CRU data fields.

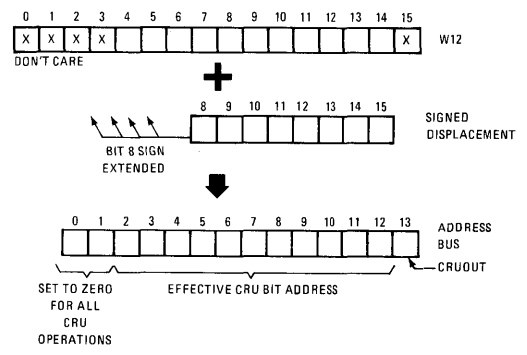
Single-Bit CRU Operations

The S9980A/S9981 performs three single-bit CRU functions: test bit (TB), set bit to one (SBO), and set bit to zero (SBZ). To identify the bit to be operated upon, the S9980A/S9981 develops a CRU-bit address and places it on the address bus, A2 to A12.

For the two output operations (SBO and SBZ), the processor also generates a CRUCLK pulse, indicating an output operation to the CRU device and places bit 7 of the instruction word on the A13 line to accomplish the specified operation (bit 7 is a one for SBO and a zero for SBZ). A test-bit instruction transfers the addressed CRU bit from the CRUIN input line to bit 2 of the status register (EQUAL).

The S9980A/S9981 develops a CRU-bit address for the single-bit operations from the CRU-base address contained in workspace register 12 and the signed displacement count contained in bits 8 through 15 of the instruction. The displacement allows two's complement addressing from base minus 128 bits through base plus 127 bits. The base address from W12 is added to the signed displacement specified in the instruction and the result is loaded into the address bus. Figure 11 illustrates the development of a single-bit CRU address.

Figure 11. A9980A/S9981 Single-Bit CRU Address Development



Multiple-Bit CRU Operations

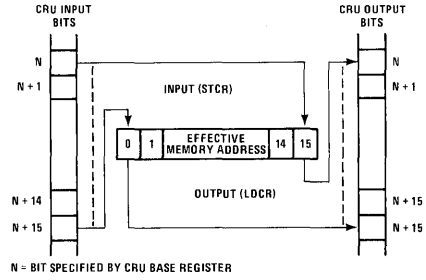
The S9980A/S9981 performs two multiple-bit CRU operations: store communications register (STCR) and load communications register (LDCR). Both operations perform a data transfer from the CRU-to-memory or from memory-to-CRU as illustrated in Figure 12. Although the figure illustrates a full 16-bit transfer operation, any number of bits from 1 through 16 may be involved. The LDCR instruction fetches a word from memory and right-shifts it to serially transfer it to CRU output bits. If the LDCR involves eight or fewer bits, those bits come from the right-justified

field within the addressed byte of the memory word. If the LDCR involves nine or more bits, those bits come from the right-justified field within the whole memory word. When transferred to the CRU interface, each successive bit receives an address that is sequentially greater than the address for the previous bit. This addressing mechanism results in an order reversal of the bits; that is, bit 15 of the memory word (or bit 7) becomes the lowest addressed bit in the CRU and bit 0 becomes the highest addressed bit in the CRU field.

An STCR instruction transfers data from the CRU to memory. If the operation involves a byte or less transfer, the transferred data will be stored right-justified in the memory byte with leading bits set to zero. If the operation involves from nine to 16 bits, the transferred data is stored right-justified in the memory word with leading bits set to zero.

When the input from the CRU device is complete, the first bit from the CRU is the least-significant-bit position in the memory word or byte.

Figure 12. S9980A/S9981 LDCR/STCR Data Transfers



External Instructions

The S9980A/S9981 has five external instructions that allow user-defined external functions to be initiated under program control. These instructions are CKON, CKOF, RSET, IDLE, and LREX. These mnemonics, except for IDLE, relate to functions implemented in the Texas Instrument 990 minicomputer and do not restrict use of the instructions to initiate various user-defined functions. IDLE also causes the S9980A/S9981 to enter the idle state and remain until an interrupt, RESET, or LOAD occurs. When any of these five instructions are executed by the S9980A/S9981, a unique 3-bit code appears on the address bus, bits A13, A0, and A1, along with a CRUCLK pulse. When the S9980A/S9981 is in an idle state, the 3-bit code and CRUCLK pulses occur repeatedly until the idle state is terminated. The codes are:

EXTERNAL INSTRUCTION	A13	A0	A1
LREX	H	H	H
CKOF	H	H	L
CKON	H	L	H
RSET	L	H	H
IDLE	L	H	L
CRU INSTRUCTIONS	H/L	L	L

Note that during external instructions bits (A2-A12) of the address bus may have any of the possible binary patterns. Since these bits (A2-A12) are used as CRU addresses, CRUCLK to the CRU must be gated with a decode of 0 on A0 and A1 to avoid erroneous strobe to CRU bits during external instruction execution.

Non-Maskable Interrupts

LOAD Function

The LOAD stimulus is an unmaskable interrupt that allows cold-start ROM loaders and front panels to be implemented for the S9980A/S9981. When the S9980A/S9981 decodes LOAD on IC0-IC2 lines, it initiates an interrupt sequence immediately following the instruction being executed. Memory location 3FFC is used to obtain the vector (WP and PC). The old PC, WP, and ST are loaded into the new workspace and the interrupt mask is set to 0000. Then the program execution resumes using the new PC and WP. Recognition of LOAD by the processor will also terminate the idle condition. External stimulus for LOAD must be held active (on IC0-IC2) for one instruction period by using IAQ signal.

RESET

When the S9980A/S9981 recognizes a RESET on IC0-IC2, it resets and inhibits $\overline{WE}$ and CRUCLK. Upon removal of the RESET code, the S9980A/S9981 initiates a level-zero interrupt sequence that acquires WP and PC from location 0000 and 0002, sets all status register bits to zero and starts execution. Recognition of RESET by the processor will also terminate an idle state. External stimulus for RESET must be held active for a minimum of three clock cycles.

S9980A/S9981 Instruction Set

Definition

The instruction set of the S9980A/S9981 is identical to that of S9900. Each instruction of this set performs one of the following operations:

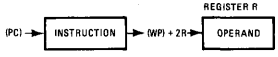
- Arithmetic, logical, comparison, or manipulation operations on data
- Loading or storage of internal registers (program counter, workspace pointer, or status)
- Data transfer between memory and external devices via the CRU
- Control functions.

Addressing Modes

S9980A/S9981 instructions contain a variety of available modes for addressing random-memory data (e.g., program parameters and flags), or formatted memory data (character strings, data lists, etc.). The following figures graphically describe the derivation of the effective address for each addressing mode. The applicability of addressing modes to particular instructions is described later along with the description of the operations performed by the instruction. The symbols following the names of the addressing modes [R, *R, *R+, @LABEL, or @TABLE (R)] are the general forms used by S9980A/S9981 assemblers to select the addressing mode for register R. Note that the S9980A/S9981 users use the same assembler and other software support packages as the ones used by S9900 users.

Workspace Register Addressing R

Workspace Register R contains the operand.

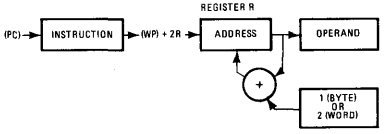


Workspace Register Indirect Addressing *R

Workspace Register R contains the address of the operand.

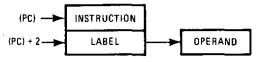
Workspace Register Indirect Auto Increment Addressing *R+

Workspace Register R contains the address of the operand. After acquiring the operand, the contents of workspace register R are incremented.



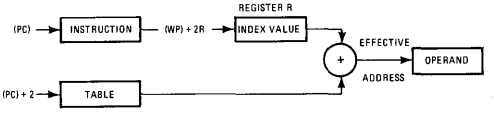
Symbolic (Direct) Addressing @LABEL

The word following the instruction contains the address of the operand.



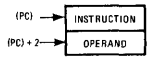
Indexed Addressing @TABLE (R)

The word following the instruction contains the base address: Workspace register R contains the index value. The sum of the base address and the index value results in the effective address of the operand.



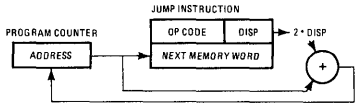
Immediate Addressing

The word following the instruction contains the operand.



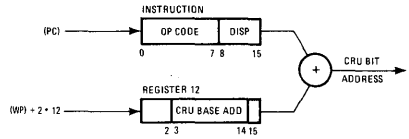
Program Counter Relative Addressing

The 8-bit signed displacement in the right byte (bits 8 through 15) of the instruction is multipled by 2 and added to the updated contents of the program counter. The result is placed in the PC.



CRU Relative Addressing

The 8-bit signed displacement in the right byte of the instruction is added to the CRU base address (bits 3 through 14 of the workspace register 12). The result is the CRU address of the selected CRU bit.



Terms and Definitions

The following terms are used in describing the instructions of the S9980A/S9981.

TERM	DEFINITION
B	Byte indicator (1 = byte, 0 = word)
C	Bit count
D	Destination address register
DA	Destination address
IOP	Immediate operand
LSB(n)	Least significant (right most) bit of (n)
MSB(n)	Most significant (left most) bit of (n)
N	Don't care
PC	Program counter
Result	Result of operation performed by instruction
S	Source address register
SA	Source address
ST	Status register
STn	Bit n of status register
T_D	Destination address modifier
T_S	Source address modifier
W	Workspace register
WRn	Workspace register n
(n)	Contents of n
a→b	a is transferred to b
|n|	Absolute value of n
+	Arithmetic addition
–	Arithmetic subtraction
AND	Logical AND
OR	Logical OR
⊕	Logical exclusive OR
n	Logical complement of n

Status Register

The status register contains the interrupt mask level and information pertaining to the instruction operation.

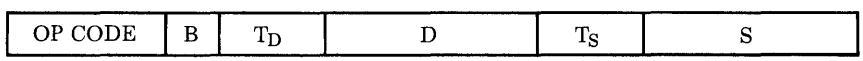
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
ST0	ST1	ST2	ST3	ST4	ST5	ST6	not used (=0)					ST12	ST13	ST14	ST15
L>	A>	=	C	O	P	X						Interrupt Mask			

BIT	NAME	INSTRUCTION	CONDITION TO SET BIT TO 1
ST0	LOGICAL GREATER THAN	C, CB	If MSB(SA) = 1 and MSB(DA) = 0, or if MSB (SA) = MSB(DA) and MSB of [(DA) – (SA)] = 1
		CI	If MSB(W) = 1 and MSB of IOP = 0, or if MSB(W) = MSB of IOP and MSB of [IOP – (W)] = 1
		ABS	If (SA) ≠ 0
		All Others	If result ≠ 0
ST1	ARITHMETIC GREATER THAN	C, CB	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA) – (SA)] = 1
		CI	If MSB(W) = 0 and MSB of IOP = 1, or if MSB(W) = MSB of IOP and MSB of [IOP – (W)] = 1
		ABS	If MSB(SA) = 0 and (SA) ≠ 0
		All Others	If MSB of result = 0 and result ≠ 0
ST2	EQUAL	C, CB	If (SA) = (DA)
		CI	If (W) = IOP
		COC	If (SA) and $(\overline{DA})$ = 0
		CZC	If (SA) and (DA) = 0
		TB	If CRUIN = 1
		ABS	If (SA) = 0
		All others	If result = 0
ST3	CARRY	A, AB, ABS, AI, DEC, DECT, INC, INCT, NEG, S, SB	If CARRY OUT = 1
		SLA, SRA, SRC, SRL	If last bit shifted out = 1
ST4	OVERFLOW	A, AB	If MSB(SA) = MSB(DA) and MSB of result ≠ MSB(DA)
		AI	If MSB(W) = MSB of IOP and MSB of result ≠ MSB(W)
		S, SB	If MSB(SA) ≠ MSB(DA) and MSB of result ≠ MSB(DA)
		DEC, DECT	If MSB(SA) = 1 and MSB of result = 0
		INC, INCT	If MSB(SA) = 0 and MSB of result = 1
		SLA	If MSB changes during shift
		DIV	If MSB(SA) = 0 and MSB(DA) = 1, or if MSB(SA) = MSB(DA) and MSB of [(DA) – (SA)] = 0
		ABS, NEG	If (SA) = 8000_{16}
ST5	PARITY	CB, MOVB	If (SA) has odd number of 1's
		LDCR, STCR	If 1 ≤ C ≤ 8 and (SA) has odd number of 1's
		AB, SB, SOCB, SZCB	If result has odd number of 1's
ST6	XOP	XOP	If XOP instruction is executed
ST12-ST15	INTERRUPT MASK	LIMI	If corresponding bit of IOP is 1
		RTWP	If corresponding bit of WR15 is 1

Instructions

Dual Operand Instructions with Multiple Addressing Modes for Source and Destination Operand

General format:



If B = 1 the operands are bytes and the operand addresses are byte addresses. If B = 0 the operands are words and the operand addresses are word addresses.

The addressing mode for each operand is determined by the T field of that operand.

T_S OR T_D	S OR D	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	1
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	4
10	1, 2, . . . 15	Indexed	2,4
11	0, 1, . . . 15	Workspace register indirect auto-increment	3

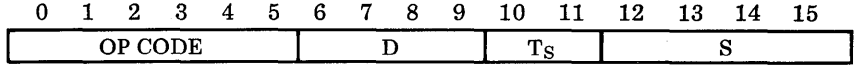
NOTES:

1. *When a workspace register is the operand of a byte instruction (bit 3 = 1), the left byte (bits 0 through 7) is the operand and the right byte (bits 8 through 15) is unchanged.*
2. *Workspace register 0 may not be used for indexing.*
3. *The workspace register is incremented by 1 for byte instructions (bit 3 = 1) and is incremented by 2 for word instructions (bit 3 = 0).*
4. *When T_S = T_D = 10, two words are required in addition to the instruction word. The first word is the source operand base address and the second word is the destination operand base address.*

MNEMONIC	OP CODE 0 1 2	B 3	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
A	1 0 1	0	Add	Yes	0-4	(SA) + (DA)→(DA)
AB	1 0 1	1	Add bytes	Yes	0-5	(SA) + (DA)→(DA)
C	1 0 0	0	Compare	No	0-2	Compare (SA) to (DA) and set appropriate status bits
CB	1 0 0	1	Compare bytes	No	0-2,5	Compare (SA) to (DA) and set appropriate status bits
S	0 1 1	0	Subtract	Yes	0-4	(DA) − (SA)→(DA)
SB	0 1 1	1	Subtract bytes	Yes	0-5	(DA) − (SA)→(DA)
SOC	1 1 1	0	Set ones corresponding	Yes	0-2	(DA) OR (SA)→(DA)
SOCB	1 1 1	1	Set ones corresponding bytes	Yes	0-2,5	(DA) OR (SA)→ (DA)
SZC	0 1 0	0	Set zeroes corresponding	Yes	0-2	(DA) AND ($\overline{SA}$)→(DA)
SZCB	0 1 0	1	Set zeroes corresponding bytes	Yes	0-2,5	(DA) AND ($\overline{SA}$)→(DA)
MOV	1 1 0	0	Move	Yes	0-2	(SA)→(DA)
MOVB	1 1 0	1	Move bytes	Yes	0-2,5	(SA)→(DA)

Dual Operand Instructions with Multiple Addressing Modes for the Source Operand and Workspace Register Addressing for the Destination.

General format:



The addressing mode for the source operand is determined by the T_S field.

T_S	S	ADDRESSING MODE	NOTES
00	0, 1, . . . 15	Workspace register	
01	0, 1, . . . 15	Workspace register indirect	
10	0	Symbolic	
10	1, 2, . . . 15	Indexed	1
11	0, 1, . . . 15	Workspace register indirect auto increment	2

NOTES:
1. *Workspace resgister 0 may not be used for indexing.*
2. *The workspace register is incremented by 2.*

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
COC	0 0 1 0 0 0	Compare ones corresponding	No	2	Test (D) to determine if 1's are in each bit position where 1's are in (SA). If so, set ST2.
CZC	0 0 1 0 0 1	Compare zeroes corresponding	No	2	Test (D) to determine if 0's are in each bit position where 1's are in (SA). If so, set ST2.
XOR	0 0 1 0 1 0	Exclusive OR	Yes	0-2	(D) ⊕ (SA)→(D)
MPY	0 0 1 1 1 0	Multiply	No		Multiply unsigned (D) by unsigned (SA) and place unsigned 32-bit product in D (most significant) and D + 1 (least sifnigicant). If WR15 is D, the next word in memory after WR15 will be used for the least significant half of the product.
DIV	0 0 1 1 1 1	Divide	No	4	If unsigned (SA) is less than or equal to unsigned (D), perform no operation and set ST4. Otherwise, divide unsigned (D) and (D + 1) by unsigned (SA). Quotient→(D), remainder→(D + 1). If D = 15, the next word in memory after WR15 will be used for the remainder.

S9900

Extended Operation (XOP) Instruction

General format:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	0	1	1	D				T_S		S			

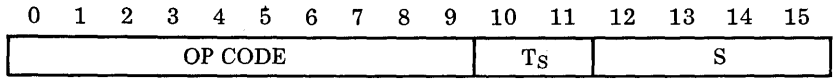
The T_S and S fields provide multiple mode addressing capability for the source operand. When the XOP is executed, ST6 is set and the following transfers occur:

$(40_{16} + 4D) \rightarrow (WP)$
$(42_{16} + 4D) \rightarrow (PC)$
SA → (new WR11)
(old WP) → (new WR13)
(old PC) → (new WR14)
(old ST) → (new WR15)

The S9980A/S9981 tests for reset and load but does not test for interrupt requests (INTREQ) upon completion of the XOP instruction.

Single Operand Instructions

General format:



The T_S and S fields provide multiple mode addressing capability for the source operand.

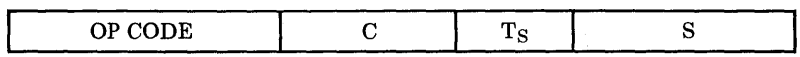
MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
B	0 0 0 0 0 1 0 0 0 1	Branch	No	–	SA→(PC)
BL	0 0 0 0 0 1 1 0 1 0	Branch and link	No	–	(PC)→(WR11); SA→(PC)
BLWP	0 0 0 0 0 1 0 0 0 0	Branch and load workspace pointer	No	–	(SA)→(WP); (SA + 2)→(PC); (old WP)→(new WR13); (old PC)→(new WR14); (old ST)→(new WR15); The S9980A/S9981 tests for reset and load, but does not test for interrupts upon completion of the BLWP instruction.
CLR	0 0 0 0 0 1 0 0 1 1	Clear operand	No	–	0→(SA)
SETO	0 0 0 0 0 1 1 1 0 0	Set to ones	No	–	$FFFF_{16}$→(SA)
INV	0 0 0 0 0 1 0 1 0 1	Invert	Yes	0-2	(SA)→(SA)
NEG	0 0 0 0 0 1 0 1 0 0	Negate	Yes	0-4	–(SA)→(SA)
ABS	0 0 0 0 0 1 1 1 0 1	Absolute value*	No	0-4	|(SA)|→(SA)
SWPB	0 0 0 0 0 1 1 0 1 1	Swap bytes	No	–	(SA), bits 0 thru 7→(SA), bits 8 thru 15; (SA), bits 8 thru 15→ (SA), bits 0 thru 7.
INC	0 0 0 0 0 1 0 1 1 0	Increment	Yes	0-4	(SA) + 1→(SA)
INCT	0 0 0 0 0 1 0 1 1 1	Increment by two	Yes	0-4	(SA) + 2→(SA)
DEC	0 0 0 0 0 1 1 0 0 0	Decrement	Yes	0-4	(SA) – 1→(SA)
DECT	0 0 0 0 0 1 1 0 0 1	Decrement by two	Yes	0-4	(SA) – 2→(SA)
X†	0 0 0 0 0 1 0 0 1 0	Execute	No	–	Execute the instruction at SA.

**Operand is compared to zero for status bit.*

†If additional memory words for the execute instruction are required to define the operands of the instruction located at SA, these words will be accessed from PC and the PC will be updated accordingly. The instruction acquisition signal (IAQ) will not be true when the S9900 accesses the instruction at SA. Status bits are affected in the normal manner for the instruction executed.

CRU Multiple-Bit Instructions

General format:



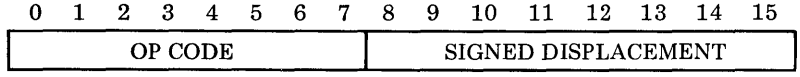
The C field specifies the number of bits to be transferred. If C = 0, 16 bits will be transferred. The CRU base register (WR12, bits 4 through 14) defines the starting CRU bit address. The bits are transferred serially and the CRU address is incremented with each bit transfer, although the contents of WR12 is not affected. T_S and S provide multiple mode addressing capability for the source operand. If 8 or fewer bits are transferred (C = 1 through 8), the source address is a byte address. If 9 or more bits are transferred (C = 0, 9 through 15), the source address is a word address. If the source is addressed in the workspace register indirect auto increment mode, the workspace register is incremented by 1 if C = 1 through 8, and is incremented by 2 otherwise.

MNEMONIC	OP CODE 0 1 2 3 4 5	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
LDCR	0 0 1 1 0 0	Load communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from (SA) to the CRU.
STCR	0 0 1 1 0 1	Store communication register	Yes	0-2,5†	Beginning with LSB of (SA), transfer the specified number of bits from the CRU to (SA). Load unfilled bit positions with 0.

†*ST5 is affected only if* $1 \leq C \leq B$.

CRU Single-Bit Instructions

General format:

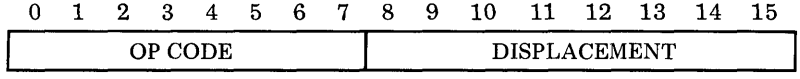


CRU relative addressing is used to address the selected CRU bit.

MNEMONIC	OP CODE 0 0 0 1 1 1 0 1	MEANING	STATUS BITS AFFECTED	DESCRIPTION
SBO	0 0 0 1 1 1 0 1	Set bit to one	—	Set the selected CRU output bit to 1.
SBZ	0 0 0 1 1 1 1 0	Set bit to zero	—	Set the selected CRU output bit to 0.
TB	0 0 0 1 1 1 1 1	Test bit	2	If the selected CRU input bit = 1, set ST2.

Jump Instructions

General format:

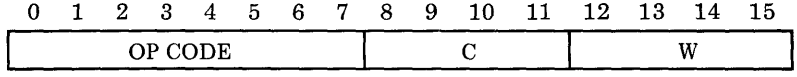


Jump instructions cause the PC to be loaded with the value selected by PC relative addressing if the bits of ST are at specified values. Otherwise, no operation occurs and the next instruction is executed since PC points to the next instruction. The displacement field is a word count to be added to PC. Thus, the jump instruction has a range of −128 to 127 words from memory-word address following the jump instruction. No ST bits are affected by jump instructions.

MNEMONIC	OP CODE 0	1	2	3	4	5	6	7	MEANING	ST CONDITION TO LOAD PC
JEQ	0	0	0	1	0	0	1	1	Jump equal	ST2 = 1
JGT	0	0	0	1	0	1	0	1	Jump greater than	ST1 = 1
JH	0	0	0	1	1	0	1	1	Jump high	ST0 = 1 and ST2 = 0
JHE	0	0	0	1	0	1	0	0	Jump high or equal	ST0 = 1 or ST2 = 1
JL	0	0	0	1	1	0	1	0	Jump low	ST0 = 0 and ST2 = 0
JLE	0	0	0	1	0	0	1	0	Jump low or equal	ST0 = 0 or ST2 = 1
JLT	0	0	0	1	0	0	0	1	Jump less than	ST1 = 0 and ST2 = 0
JMP	0	0	0	1	0	0	0	0	Jump unconditional	unconditional
JNC	0	0	0	1	0	1	1	1	Jump no carry	ST3 = 0
JNE	0	0	0	1	0	1	1	0	Jump not equal	ST2 = 0
JNO	0	0	0	1	1	0	0	1	Jump no overflow	ST4 = 0
JOC	0	0	0	1	1	0	0	0	Jump no carry	ST3 = 1
JOP	0	0	0	1	1	1	0	0	Jump odd parity	ST5 = 1

Shift Instructions

General format:

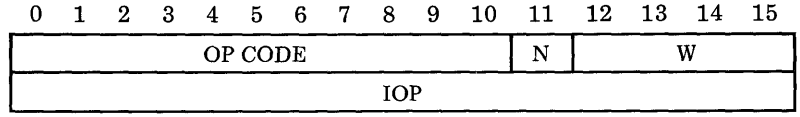


If C = 0, bits 12 through 15 of WR0 contain the shift count. If C = 0 and bits 12 through 15 of WR0 = 0, the shift count is 16.

MNEMONIC	OP CODE 0	1	2	3	4	5	6	7	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
SLA	0	0	0	0	1	0	1	0	Shift left arithmetic	Yes	0-4	Shift (W) left. Fill vacated bit positions with 0.
SRA	0	0	0	0	1	0	0	0	Shift right arithmetic	Yes	0-3	Shift (W) right. Fill vacated bit positions with original MSB of (W).
SRC	0	0	0	0	1	0	1	1	Shift right circular	Yes	0-3	Shift (W) right. Shift previous LSB into MSB.
SRL	0	0	0	0	1	0	0	1	Shift right logical	Yes	0-3	Shift (W) right. Fill vacated bit positions with 0's.

Immediate Register Instructions

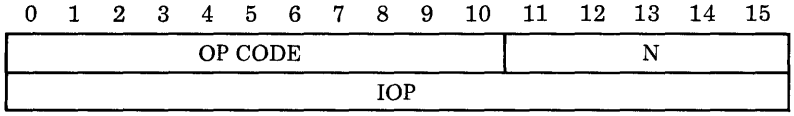
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	RESULT COMPARED TO 0	STATUS BITS AFFECTED	DESCRIPTION
AI	0 0 0 0 0 0 1 0 0 0 1	Add immediate	Yes	0-4	(W) + IOP → (W)
ANDI	0 0 0 0 0 0 1 0 0 1 0	AND immediate	Yes	0-2	(W) AND IOP → (W)
CI	0 0 0 0 0 0 1 0 1 0 0	Compare immediate	Yes	0-2	Compare (W) to IOP and set appropriate status bits
LI	0 0 0 0 0 0 1 0 0 0 0	Load immediate	Yes	0-2	IOP → (W)
ORI	0 0 0 0 0 0 1 0 0 1 1	OR immediate	Yes	0-2	(W) OR IOP → (W)

Internal Register Instruction

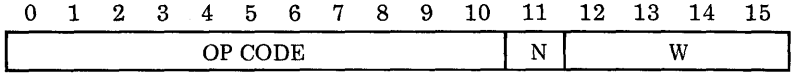
General format:



MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
LWPI	0 0 0 0 0 0 1 0 1 1 1	Load workspace pointer immediate	IOP → (WP), no ST bits affected
LIMI	0 0 0 0 0 0 1 1 0 0 0	Load interrupt mask	IOP, bits 12 thru 15 → ST12 thru ST15

Internal Register Store Instructions

General format:

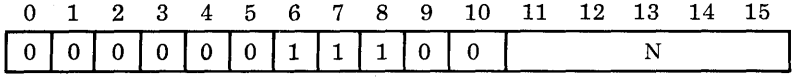


No ST bits are affected.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	DESCRIPTION
STST	0 0 0 0 0 0 1 0 1 1 0	Store status register	(ST) → (W)
STWP	0 0 0 0 0 0 1 0 1 0 1	Store workspace pointer	(WP) → (W)

Return Workspace Pointer (RTWP) Instruction

General format:

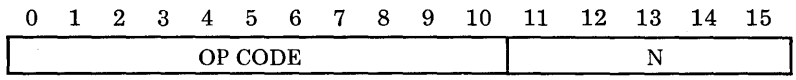


The RTWP instruction causes the following transfers to occur:

(WR15) → (ST)
(WR14) → (PC)
(WR13) → (WP)

External Instructions

General format:



External instructions cause the three address lines (A13; A0, A1) to be set to the below-described levels and the CRUCLK line to be pulsed, allowing external control functions to be initiated.

MNEMONIC	OP CODE 0 1 2 3 4 5 6 7 8 9 10	MEANING	STATUS BITS AFFECTED	DESCRIPTION	ADDRESS BUS A13 A0 A1
IDLE	0 0 0 0 0 0 1 1 0 1 0	Idle	—	Suspend S9980/S9981 instruction execution until an interrupt, $\overline{\text{LOAD}}$, or $\overline{\text{RESET}}$ occurs	L H L
RSET	0 0 0 0 0 0 1 1 0 1 1	Reset	12-15	0→ST12 thru ST15	L H H
CKOF	0 0 0 0 0 0 1 1 1 1 0	User defined		—	H H L
CKON	0 0 0 0 0 0 1 1 1 0 1	User defined		—	H L H
LREX	0 0 0 0 0 0 1 1 1 1 1	User defined		—	H H H

S9980A/S9981 Instruction Execution Times

Instruction execution times for the S9980A/S9981 are a function of:

1. Clock cycle time, $t_{c(\phi)}$.
2. Addressing mode used where operands have multiple addressing mode capability.
3. Number of wait states required per memory access.

Table 4 lists the number of clock cycles and memory accesses required to execute each S9980A/S9981 instruction. For instructions with multiple addressing modes for either or both operands, Table 4 lists the number of clock cycles and memory accesses with all operands addressed in the workspace-register mode. To determine the additional number of clock cycles and memory accesses required for modified addressing, add the appropriate values from the referenced tables. The total instruction-execution time for an instruction is:

$T = t_{c(\phi)} (C + W \cdot M)$

where:

T = total instruction time;
$t_{c(\phi)}$ = clock cycle time;
C = number of clock cycles for instruction execution plus address modification;
W = number of required wait states per memory access for instruction execution plus address modification;
M = number of memory accesses.

As an example, the instruction MOVB is used in a system with $t_{c(\phi)} = 0.400\mu s$ and no wait states are required to access memory. Both operands are addressed in the workspace register mode:

$T = t_{c(\phi)} (C + W \cdot M) = 0.400 (22 + 0 \cdot 8) = 8.8\mu s.$

If two wait states per memory access were required, the execution time is:

$T = 0.400 (22 + 2 \cdot 8)\ \mu s = 15.2\mu s.$

If the source operand was addressed in the symbolic mode and two wait states were required:

$T = t_{c(\phi)} (C + W \cdot M)$
$C = 22 + 10 = 32$
$M = 8 + 2 = 10$
$T = 0.400 (32 + 2 \cdot 10) = 20.8\mu s.$

Table 4. Instruction Execution Times

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION***	
			SOURCE	DESTINATION
A	22	8	A	A
AB	22	8	B	B
ABS (MSB = 0)	16	4	A	—
(MSB = 1)	20	6	A	—
AI	22	8	—	—
ANDI	22	8	—	—
B	12	4	A	—
BL	18	6	A	—
BLWP	38	12	A	—
C	20	6	A	A
CB	20	6	B	B
CI	20	6	—	—
CKOF	14	2	—	—
CKON	14	2	—	—
CLR	16	6	A	—
COC	20	6	A	—
CZC	20	6	A	—
DEC	16	6	A	—
DECT	16	6	A	—
DIV (ST4 is set)	22	6	A	—
DIV (ST4 is reset)*	104-136	12	A	—
IDLE	14	2	—	—
INC	16	6	A	—
INCT	16	6	A	—
INV	16	6	A	—
Jump (PC is changed)	12	2	—	—
(PC is not changed)	10	2	—	—
LDCR (C = 0)	58	6	A	—
(1<C<8)	26+2C	6	B	—
(9<C<15)	26+2C	6	A	—
LI	18	6	—	—
LIMI	22	6	—	—
LREX	14	2	—	—
LWPI	14	4	—	—
MOV	22	8	A	A
MOVB	22	8	B	B
MPY	62	10	A	—
NEG	18	6	A	—
ORI	22	8	—	—
RSET	14	2	—	—
RTWP	22	8	—	—
S	22	8	A	A
SB	22	8	B	B
SBO	16	4	—	—
SBZ	16	4	—	—
SETO	16	6	A	—

Table 4. Instruction Execution Times (Continued)

INSTRUCTION	CLOCK CYCLES C	MEMORY ACCESS M	ADDRESS MODIFICATION*** SOURCE	ADDRESS MODIFICATION*** DESTINATION
Shift (C ≠ 0)	18+2C	6	—	—
(C ≠ 0, Bits 12-15 of WR0 = 0)	60	8	—	—
(C = 0, Bits 12-15 of WRP = N ≠ 0)	28+2N	8	—	—
SOC	22	8	A	A
SOCB	22	8	B	B
STCR (C = 0)	68	8	A	—
(1≤C≤7)	50	8	B	—
(C = 8)	52	8	B	—
(9≤C≤15)	66	8	A	—
STST	12	4	—	—
STWP	12	4	—	—
SWPB	16	6	A	—
SZC	22	8	A	A
SZCB	22	8	B	B
TB	16	4	—	—
X**	12	4	A	—
XOP	52	16	A	—
XOR	22	8	A	—
RESET function	36	10	—	—
LOAD function	32	10	—	—
Interrupt context switch	32	10	—	—
Undefined op codes: 0000-01FF, 0320 033F, 0C00-0FFF, 0780-07FF	8	2	—	—

*Execution time is dependent upon the partial quotient after each clock cycle during execution.

**Execution time is added to the execution time of the instruction located at the source address.

***The letters A and B refer to the respective tables that follow.

Table A. Address Modification

ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	6	2
WR indirect auto-increment (T_S or T_D = 11)	12	4
Symbolic (T_S or T_D = 10, S or D = 0)	10	2
Indexed ($T_S T_D$ = 10, S or D ≠ 0)	12	4

Table B. Address Modification

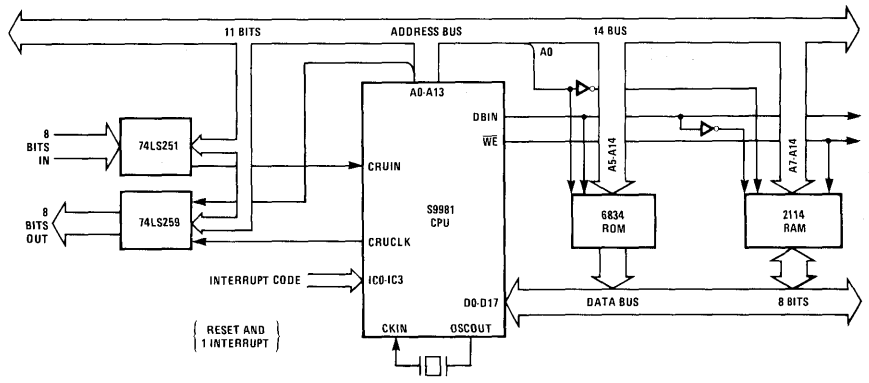
ADDRESSING MODE	CLOCK CYCLES C	MEMORY ACCESSES M
WR (T_S or T_D = 00)	0	0
WR indirect (T_S or T_D = 01)	6	2
WR indirect auto-increment (T_S or T_D = 11)	10	4
Symbolic (T_S or T_D = 10, S or D = 0)	10	2
Indexed (T_S or T_D = 10, S or D ≠ 0)	12	4

System Design Examples

Figure 15 illustrates a typical minimum S9981 system. Eight bits of input and output interface are implemented. No interface circuits are used for interrupt code thus providing for reset and one interrupt only. CKIN and OSCOUT are tied to a 10MHz crystal to use the on-chip crystal oscillator. The memory system contains 512x8 ROM and 1024x8 RAM. The package count for this system is 6 packages.

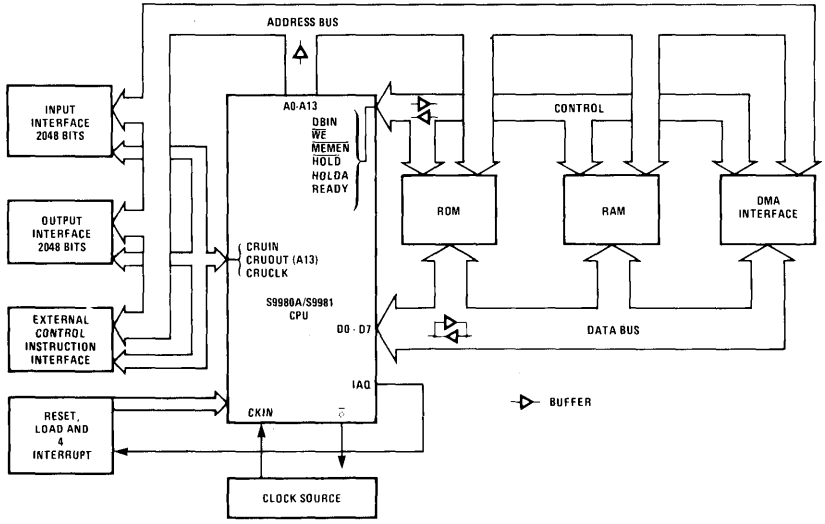
A maximum S9980A/S9981 system is illustrated in Figure 16. ROM and RAM are both shown for a total of 16,284 bytes of memory. The I/O interface support 2048 output bits and 2048 input bits. RESET, LOAD, and 4 interrupts are implemented on the interrupt interface lines. Optional external clock may be supplied on CKIN. Buss buffers, required for this maximally configured system, are indicated on the system buses.

Figure 15. Minimum S9980 System



S9900

Figure 16. Maximum S9980 System



Instructions Summary

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
A	A000	1	Y	0-4	ADD(WORD)
AB	B000	1	Y	0-5	ADD(BYTE)
ABS	0740	6	Y	0-4	ABSOLUTE VALUE
AI	0220	8	Y	0-4	ADD IMMEDIATE
ANDI	0240	8	Y	0-2	AND IMMEDIATE
B	0440	6	N	—	BRANCH
BL	0680	6	N	—	BRANCH AND LINK (W11)
BLWP	0400	6	N	—	BRANCH LOAD WORKSPACE POINTER
C	8000	1	N	0-2	COMPARE (WORD)
CB	9000	1	N	0-2,5	COMPARE (BYTE)
CI	0280	8	N	0-2	COMPARE IMMEDIATE
CKOF	03C0	7	N	—	EXTERNAL CONTROL
CKON	03A0	7	N	—	EXTERNAL CONTROL
CLR	04C0	6	N	—	CLEAR OPERAND
COC	2000	3	N	2	COMPARE ONES CORRESPONDING
CZC	2400	3	N	2	COMPARE ZEROES CORRESPONDING
DEC	0600	6	Y	0-4	DECREMENT (BY ONE)
DECT	0640	6	Y	0-4	DECREMENT (BY TWO)
DIV	3C00	9	N	4	DIVIDE
IDLE	0340	7	N	—	COMPUTER IDLE
INC	0580	6	Y	0-4	INCREMENT (BY ONE)
INCT	05C0	6	Y	0-4	INCREMENT (BY TWO)
INV	0540	6	Y	0-2	INVERT (ONES COMPLEMENT)
JEQ	1300	2	N	—	JUMP EQUAL (ST2-1)

Instructions Summary (Continued)

MNEMONIC	OP CODE	FORMAT	RESULT COMPARED TO ZERO	STATUS AFFECTED	INSTRUCTIONS
JGT	1500	2	N	—	JUMP GREATER THAN (ST1 = 1)
JH	1800	2	N	—	JUMP HIGH (ST0 = 1 AND ST2 = 0)
JHE	1400	2	N	—	JUMP HIGH OR EQUAL (ST0 OR ST2 = 1)
JL	1000	2	N	—	JUMP LOW (ST0 AND ST2 = 0)
JLE	1200	2	N	—	JUMP LOW OR EQUAL (ST0 = 0 OR ST2 = 1)
JLT	1100	2	N	—	JUMP LESS THAN (ST1 AND ST2 = 0)
JMP	1000	2	N	—	JUMP UNCONDITIONAL
JNC	1700	2	N	—	JUMP NO CARRY (ST3 = 0)
JNE	1600	2	N	—	JUMP NOT EQUAL (ST2 = 0)
JND	1900	2	N	—	JUMP NO OVERFLOW (ST4 = 0)
JOC	1800	2	N	—	JUMP ON CARRY (ST3 = 1)
JOP	1C00	2	N	—	JUMP ODD PARITY (ST5 = 1)
LDCR	3000	4	Y	0-2,5	LOAD CRU
LI	0200	8	N	0-2	LOAD IMMEDIATE
LIMI	0300	8	N	12-15	LOAD IMMEDIATE TO INTERRUPT MASK
LREX	03E0	7	N	12-15	EXTERNAL CONTROL
LWPI	02E0	8	N	—	LOAD IMMEDIATE TO WORKSPCE POINTER
MOV	C000	1	Y	0-2	MOVE (WORD)
MOVB	D000	1	Y	0-2,5	MOVE (BYTE)
MPY	3800	9	N	—	MULTIPLY
NEG	0500	6	Y	0-4	NEGATE (TWO'S COMPLEMENT)
ORI	0260	8	Y	0-2	OR IMMEDIATE
RSET	0360	7	N	12-15	EXTERNAL CONTROL
RTWP	0380	7	N	0-6, 12-15	RETURN WORKSPACE POINTER
S	6000	1	Y	0-4	SUBTRACT (WORD)
SB	7000	1	Y	0-5	SUBTRACT (BYTE)
SBO	1D00	2	N	—	SET CRU BIT TO ONE
SBZ	1E00	2	N	—	SET CRU BIT TO ZERO
SETO	0700	6	N	—	SET ONES
SLA	0A00	5	Y	0-4	SHIFT LEFT (ZERO FULL)
SOC	E000	1	Y	0-2	SET ONES CORRESPONDING (WORD)
SOCB	F000	1	Y	0-2,5	SET ONES CORRESPONDING (BYTE)
SRA	0800	5	Y	0-3	SHIFT RIGHT (MSB EXTENDED)
SRC	0800	5	Y	0-3	SHIFT RIGHT CIRCULAR
SRL	0900	5	Y	0-3	SHIFT RIGHT (LEADING ZERO FILL)
STCR	3400	4	Y	0-2,5	STORE FROM CRU
STST	02C0	8	N	—	STORE STATUS REGISTER
STWP	02A0	8	N	—	STORE WORKSPACE POINTER
SWPB	06C0	6	N	—	SWAP BYTES
SZC	4000	1	Y	0-2	SET ZEROES CORRESPONDING (WORD)
SZCB	5000	1	Y	0-2,5	SET ZEROES CORRESPONDING (BYTE)
TB	1F00	2	N	2	TEST CRU BIT
X	0480	6	N	—	EXECUTE
XOP	2C00	9	N	6	EXTENDED OPERATION
XOR	2800	3	Y	0-2	EXCLUSIVE OR

ILLEGAL OP CODES 0000-01FF;0320-033F;0780-07FF;0C00-0FFF

AMERICAN MICROSYSTEMS, INC.

S9901/S9901-4

Programmable Systems Interface Circuit

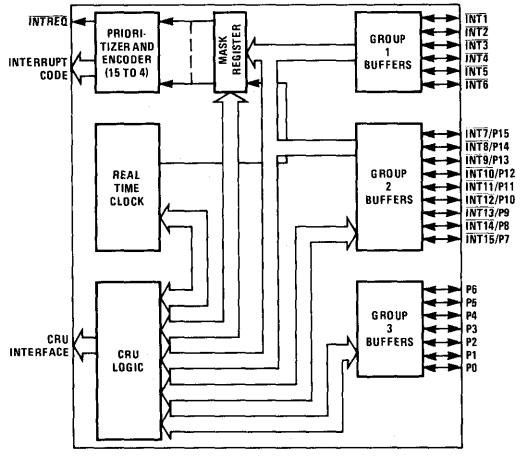
Features

- N-Channel Silicon-Gate Process
- 9900 Series CRU Peripheral
- Performs Interrupt and I/O Interface Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupts or I/O
- Easily Stacked for Interrupt and I/O Expansion
- Interval and Event Timer
- Single 5V Supply

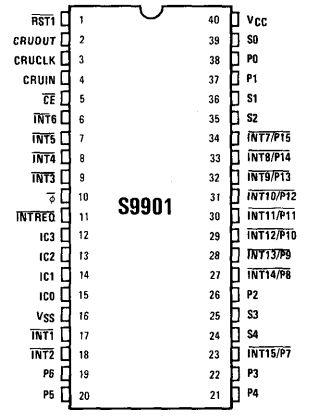
General Description

The S9901 Programmable Systems Interface is a multi-functioned component designed to provide low cost interrupts and I/O ports in a 9900/9980 microprocessor system. It is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs including the power supply (+5V) and single-phase clock. The Programmable Systems Interface provides a 9900/9980 system with interrupt control, I/O ports, and a real-time clock as shown on page 1.

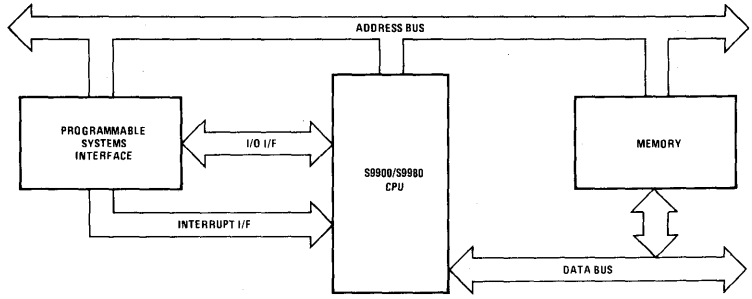
Block Diagram



S9901 Pin Configuration



9900/9980 System



S9901 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltages, V_{CC} and V_{SS}	−0.3V to +10V
All Input and Output Voltages	−0.3V to +10V
Continuous Power Dissipation	0.75W
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

**Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.*

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}		2		V
Low-Level Input Voltage, V_{IL}		0.8		V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics

Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)		±10		μA	V_I = 0V to V_{CC}
V_{OH}	High Level Output Voltage		2.4		V	I_{OH} = 100μA
			2		V	I_{OH} = −400μA
V_{OL}	Low Level Output Voltage		0.4		V	I_{OL} = 3.2mA
I_{CC}	Supply Current from V_{CC}		100		mA	
I_{SS}	Supply Current from V_{SS}		200		mA	
$I_{CC(av)}$	Average Supply Current from V_{CC}		60		mA	$t_{c(0)}$ = 333ns, T_A = 25°C
C_i	Capacitance, Any Input		10		pF	f = 1MHz,
C_o	Capacitance, Any Output		20		pF	All Other Pins at 0V

Timing Requirements

Over Full Range of Operating Conditions

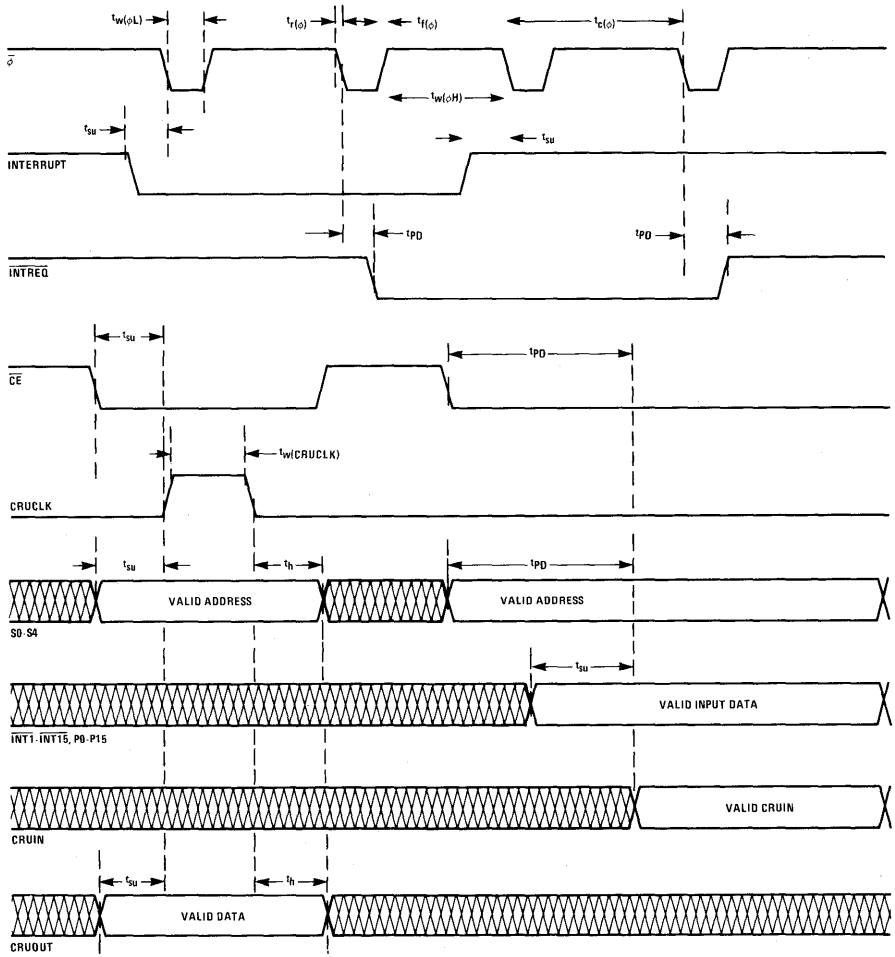
Symbol	Parameter	S9901			S9901-4			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
$t_{c(0)}$	Clock Cycle Time	300	333	2000	240	250	667	ns
$t_{r(0)}$	Clock Rise Time	5	10	40	5		40	ns
$t_{f(0)}$	Clock Fall Time	5	10	40	10		40	ns
$t_{w(0L)}$	Clock Pulse Low Width	45	55	300	40		300	ns
$t_{w(0H)}$	Clock Pulse High Width	225	240		180			ns
t_{su_1}	Setup Time for S_0-S_4, CE, or CRU_{OUT} Before CRU_{CLK}	100	200		80	80		ns
t_{su_3}	Setup Time, Input Before Valid CRU_{IN}	200	200		180	180		ns
t_{su_2}	Setup Time, Interrupt Before 0 Low	60	80		50	50		ns
$t_{w(CRUCLK)}$	CRU Clock Pulse Width	100			80			ns
t_h	Address Hold Time	60	80		50			ns

Switching Characteristics

Over Full Range of Recommended Operating Conditions

Symbol	Parameter	S9901 Min.	S9901 Typ.	S9901 Max.	S9901-4 Min.	S9901-4 Typ.	S9901-4 Max.	Unit	Test Conditions
t_{PD}	Propagation Delay, $\overline{0}$ Low to Valid $\overline{INTREQ}$, I_{C0}-I_{C3}		110	110		80	80	ns	C_L=100pF, 2 TTL Loads
t_{PD}	Propagation Delay, S_0-S_4 or $\overline{CE}$ to Valid CRU_{IN}		320	320		240	240	ns	C_L=100pF

Figure 1. Switching Characteristics



NOTE 1: ALL TIMING MEASUREMENTS ARE FROM 10% and 90% POINTS

Pin Definitions

Table 1 defines the S9901 pin assignments and describes the function of each pin.

Table 1. S9901 Pin Assignments and Functions

Signature	Pin	I/O	Description
$\overline{INTREQ}$	11	OUT	INTERRUPT Request. When active (low) $\overline{INTREQ}$ indicates that an enabled interrupt has been received. $\overline{INTREQ}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0-IC3 = (1,1,1,1).
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
$\overline{CE}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{CE}$ has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	36	IN	
S2	35	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{CE}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{CE}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{RST1}$	1	IN	Power Up Reset. When active (low) $\overline{RST1}$ resets all interrupt masks to "0", disables the clock, and programs all I/O ports to inputs. $\overline{RST1}$ has a Schmitt-Trigger input to allow implementation with an RC circuit as shown in Figure 6.
V_{CC}	40		Supply Voltage. +5V nominal.
V_{SS}	16		Ground Reference
$\overline{\phi}$	10		System clock ($\overline{\phi}3$ in S9900 system, $\overline{CKOUT}$ in S9980 system).
$\overline{INT1}$	17	IN	Group 1, interrupt inputs. When active.
$\overline{INT2}$	18	IN	(Low) the signal is ANDed with its corresponding mask bit and if enabled
$\overline{INT3}$	9	IN	sent to the interrupt control section. INT1 has highest priority.
$\overline{INT4}$	8	IN	
$\overline{INT5}$	7	IN	
$\overline{INT6}$	6	IN	
$\overline{INT7}$/P15	34	I/O	Group 2, Programmable interrupt (active low) or I/O pins (true logic).
$\overline{INT8}$/P14	33	I/O	Each pin is individually programmable as an interrupt, an input port, or an
$\overline{INT9}$/P13	32	I/O	output port.
$\overline{INT10}$/P12	31	I/O	
$\overline{INT11}$/P11	30	I/O	
$\overline{INT12}$/P10	29	I/O	
$\overline{INT13}$/P9	28	I/O	
$\overline{INT14}$/P8	27	I/O	
$\overline{INT15}$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as
P1	37	I/O	an input port or an output port.
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	

Functional Description

CPU Interface

The S9901 interfaces to the CPU through the Communications Register Unit (CRU) and the interrupt control lines as shown in Figure 1. The CRU interface consists of 5 address select lines (S0-S4), chip enable ($\overline{CE}$), and 3 CRU lines (CRUIN, CRUOUT, CRUCLK). When $\overline{CE}$ becomes active (low), the 5 select lines point to the CRU bit being accessed (see Table 2). In the case of a write, the datum is strobed off the CROUT line by the CRUCLK signal. For a read, the datum is sent to the CPU on the CRUIN line. The interrupt control lines consist of an interrupt request line ($\overline{INTREQ}$) and 4 code lines (IC0-IC3). The interrupt section of the S9901 prioritizes and encodes the highest priority active interrupt into the proper code to present to the CPU, and outputs this code on the IC0-IC3 code lines along with an active $\overline{INTREQ}$. Several S9901's can be used with the CPU by connecting all CRU and address lines in parallel and providing a unique chip select to each device.

System Interface

The system interface consists of 22 pins divided into 3 groups. The 6 pins in Group 1 ($\overline{INT1}$-$\overline{INT6}$) are normally dedicated to interrupt inputs (active low), but may also be used as input ports (true data in). Group 2 ($\overline{INT7}$/P15-$\overline{INT15}$/P7) consists of 9 pins which can be individually programmed as interrupt inputs (active low), input ports (true data in), or output ports (true data out). The remaining 7 pins which comprise Group 3 (P0-P6) are dedicated as individually programmable I/O ports (true data).

Interrupt Control

A block diagram of the interrupt control section is shown in Figure 4. The interrupt inputs (6 dedicated, 9 programmable) are sampled by $\bar{\phi}$ (active low) and are ANDED with their respective mask bits. If an interrupt input is active (low) and enabled (MASK=1), the signal is passed through to the priority encoder where the highest priority signal is encoded into a 4-bit binary code as shown in Table 3. The code along with the interrupt request is then output via the CPU interface on the leading edge of the next $\bar{\phi}$ to ensure proper synchronization to the processor.

The output signals will remain valid until the corresponding interrupt input is removed, the interrupt is disabled (MASK=0), or a higher priority enabled interrupt becomes active. When the highest priority enabled interrupt is removed, the code corresponding to the next highest priority enabled interrupt is output. If no enabled interrupt is active, all CPU interface lines ($\overline{INTREQ}$, IC0-IC3) are held high. $\overline{RST1}$ (power-up-reset) will force the output code to (0,0,0,0) with $\overline{INTREQ}$ held high and will reset all mask bits low (interrupts disabled). Individual interrupts can be subsequently enabled (disabled) by programming the appropriate command bits. Unused interrupt inputs may be used as datum inputs by disabling the interrupt (MASK=0).

Input/Output

A block diagram of the I/O section is shown in Figure 5. Up to 16 individually controlled I/O ports are available (7 dedicated, 9 programmable). $\overline{RST1}$ or $\overline{RST2}$ (a command bit) will program all ports to the input mode. Writing a datum to any port will program that port to the output mode and latch out the datum. The port will then remain in the output mode until either $\overline{RST1}$ or $\overline{RST2}$ is executed. Data present on the Group 2 pins can be read by either the Read Interrupt Commands or the Read Input Commands. Group 2 pins being used as input ports should have their respective Interrupt Mask values reset (low) to prevent false interrupts from occurring. In applications where Group 1 pins are not required as interrupt inputs, they may be used as input ports and read using the Read Input commands. As with Group 2 ports, any pins being used as input ports should have their respective Interrupt Masks disabled.

Table 2. CRU Bit Assignments

CRU Bit	S0	S1	S2	S3	S4	CRU Read Data	CRU Write Data
0	0	0	0	0	0	CONTROL BIT(1)	CONTROL BIT(1)
1	0	0	0	0	1	$\overline{INT}$1/CLK1(2)	Mask 1/CLK1(3)
2	0	0	0	1	0	$\overline{INT}$2/CLK2	Mask 2/CLK2
3	0	0	0	1	1	$\overline{INT}$3/CLK3	Mask 3/CLK3
4	0	0	1	0	0	$\overline{INT}$4/CLK4	Mask 4/CLK4
5	0	0	1	0	1	$\overline{INT}$5/CLK5	Mask 5/CLK5
6	0	0	1	1	0	$\overline{INT}$6/CLK6	Mask 6/CLK6
7	0	0	1	1	1	$\overline{INT}$7/CLK7	Mask 7/CLK7
8	0	1	0	0	0	$\overline{INT}$8/CLK8	Mask 8/CLK8
9	0	1	0	0	1	$\overline{INT}$9/CLK9	Mask 9/CLK9
10	0	1	0	1	0	$\overline{INT}$10/CLK10	Mask 10/CLK10
11	0	1	0	1	1	$\overline{INT}$11/CLK11	Mask 11/CLK11
12	0	1	1	0	0	$\overline{INT}$12/CLK12	Mask 12/CLK12
13	0	1	1	0	1	$\overline{INT}$13/CLK13	Mask 13/CLK13
14	0	1	1	1	0	$\overline{INT}$14/CLK14	Mask 14/CLK14
15	0	1	1	1	1	$\overline{INT}$15/$\overline{INTREQ}$	Mask 15/$\overline{RST}$2(4)
16	1	0	0	0	0	P0 INPUT(5)	P0 Output(6)
17	1	0	0	0	1	P1 Input	P1 Output
18	1	0	0	1	0	P2 Input	P2 Output
19	1	0	0	1	1	P3 Input	P3 Output
20	1	0	1	0	0	P4 Input	P4 Output
21	1	0	1	0	1	P5 Input	P5 Output
22	1	0	1	1	0	P6 Input	P6 Output
23	1	0	1	1	1	P7 Input	P7 Output
24	1	1	0	0	0	P8 Input	P8 Output
25	1	1	0	0	1	P9 Input	P9 Output
26	1	1	0	1	0	P10 Input	P10 Output
27	1	1	0	1	1	P11 Input	P11 Output
28	1	1	1	0	0	P12 Input	P12 Output
29	1	1	1	0	1	P13 Input	P13 Output
30	1	1	1	1	0	P14 Input	P14 Output
31	1	1	1	1	1	P15 Input	P15 Output

NOTES: (1) 0 = Interrupt Mode 1 = Clock Mode
(2) Data present on INT input pin (or clock value) will be read regardless of mask value.
(3) While in the Interrupt Mode (Control Bit = 0) writing a "1" into mask will enable interrupt; a "0" will disable.
(4) Writing a zero to bit 15 while in the clock mode (Control Bit = 1) executes a software reset of the I/O pins.
(5) Data present on the pin will be read. Output data can be read without affecting the data.
(6) Writing data to the port will program the port to the output mode and output the data.

Figure 4. Interrupt Control Logic

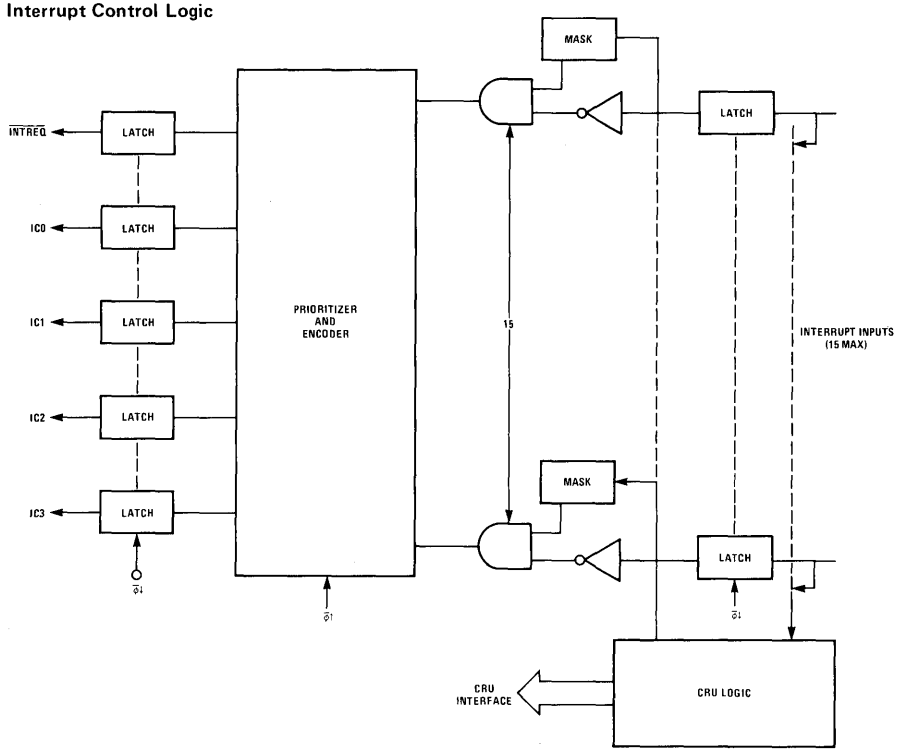


Table 3 Interrupt Code Generation

Interrupt/State	Priority	IC0	IC1	IC2	IC3	$\overline{\text{INTREQ}}$
$\overline{\text{INT}}$1	1 (HIGHEST)	0	0	0	1	0
$\overline{\text{INT}}$2	2	0	0	1	0	0
$\overline{\text{INT}}$3/CLOCK	3	0	0	1	1	0
$\overline{\text{INT}}$4	4	0	1	0	0	0
$\overline{\text{INT}}$5	5	0	1	0	1	0
$\overline{\text{INT}}$6	6	0	1	1	0	0
$\overline{\text{INT}}$7	7	0	1	1	1	0
$\overline{\text{INT}}$8	8	1	0	0	0	0
$\overline{\text{INT}}$9	9	1	0	0	1	0
$\overline{\text{INT}}$10	10	1	0	1	0	0
$\overline{\text{INT}}$11	11	1	0	1	1	0
$\overline{\text{INT}}$12	12	1	1	0	0	0
$\overline{\text{INT}}$13	13	1	1	0	1	0
$\overline{\text{INT}}$14	14	1	1	1	0	0
$\overline{\text{INT}}$15	15 (LOWEST)	1	1	1	1	0
NO INTERRRUPT	—	1	1	1	1	1

Programmable Real Time Clock

A block diagram of the programmable real time clock section is shown in Figure 6. The clock consists of a 14-bit counter that decrements at a rate of F(ϕ)/64 (at 3MHz this results in a maximum interval of 349ms with a resolution of 21.3μs) and can be used as either an interval timer or as an event timer.

The clock is accessed by writing a one into the control bit (address 0) to force CRU bits 1-15 to clock mode. (See Table 1.) Writing a nonzero value into the clock register then enables the clock and sets its frequency. During system set up this entire operation can be accomplished with one additional I/O instruction (LCDR) as shown in Table 4. The clock functions as an interval timer by decrementing to zero, issuing an interrupt, and restarting at the programmed start value. When the clock interrupt is active, the clock mask (mask bit 3) must be written into (with either a "1" or a "0") to clear the interrupt.

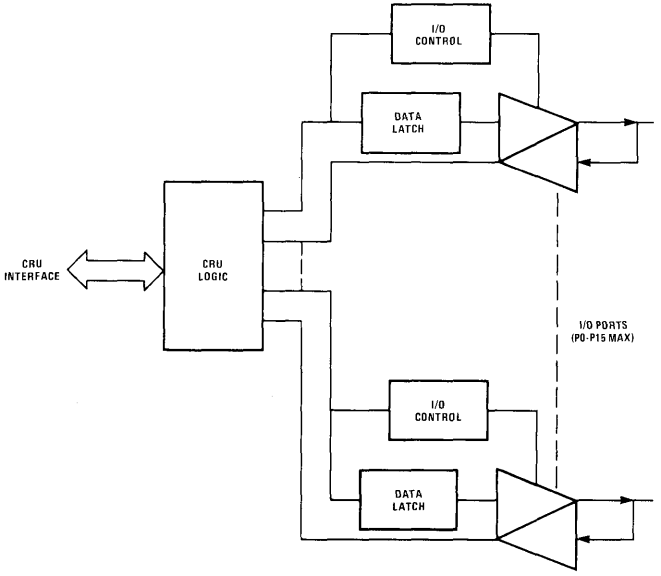
If a value other than that initially programmed is required, a new 14-bit clock start value is similarly programmed by executing a CRU write operation to the same locations. During programming the decrementer is restarted with the current start value after each start value bit is written. A timer restart can be easily implemented by writing a single bit to any of the clock bits.

The clock is disabled by $\overline{\text{RST1}}$ (power-up-clear) or by writing a zero value into the clock register. Enabling the clock programs the third priority interrupt ($\overline{\text{INT3}}$) as the clock interrupt and disables generation of interrupts from the $\overline{\text{INT3}}$ input pin. When accessing the clock all interrupts should be disabled to ensure that system integrity is maintained.

The clock can also function as an event timer since whenever the device is switched to the clock mode, by writing a one to the control bit, the current value of the clock is stored in the clock read register. Reading this value, and thus the elapsed event time, is accomplished by executing a 14-bit CRU read operation (addresses 1-14). The software example (Table 3) shows a read of the event timer.

The current status of the machine can always be obtained by reading the control (address zero) bit. A "0" indicates the machine is in an interrupt mode. Bits 1

Figure 5. I/O Interface



through 15 would normally be the interrupt input lines in this mode, but if any are not needed for interrupts they may also be read with a CRU input command and interpreted as normal data inputs. A "1" read on the control bit indicates that the 9901 is in the clock mode. Reading bits 1 through 14 completes the event timer operation as described above. Reading bit 15 indicates whether the interrupt request line is active.

A software reset $\overline{RST2}$ can be performed by writing a "1" to the control bit followed by writing a "1" to bit 15, which forces all I/O ports to the input mode.

Table 4 Software Examples

Assumptions

- System uses clock at maximum interval
- Total of 6 interrupts are used
- 8 bits are used as output port
- 8 bits are used as input port
- RST1 (power up reset) has already been applied

System Setup for Interrupt	LI	R12,PSIBAS	Setup CRU Base Address to point 9901
	LDCR	@X,0	Program Clock with maximum interval
	LDCR	@Y,7	Re-enter interrupt mode and enable top 6 interrupts
System Setup for Output Ports	LI	R12,PSIBAS+ 16	Move CRU Base to point I/O port
	LDCR	R1,8	Move most significant byte of R1 to output port
Read Programmed Inputs	LI	R12,PSIBAS+ 24	Move CRU Base to point to input ports
	STCR	R2,8	Move input port to most significant byte of R2

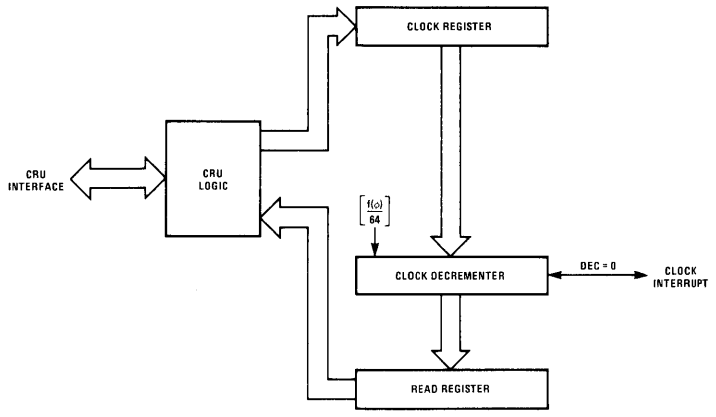
(X) ⟶ FFFF

(Y) ⟶ 7FXX

Don't cares

	BLWP	CLKVCT	Save Interrupt Mask
	•		
	•		
	•		
CLKPC	LIMI	0	Disable INTERRUPTS
	LI	R12,PSIBAS+ 1	Set up CRU Base
	SBO	-1	Set 9901 into Clock Mode, Latch Clock Value
	STCR	R4,14	Store Read Register Latch Value into R4
	SBZ	-1	Reenter Interrupt Mode and Restarting Clock
	RTWP		Restore Interrupt Mask
	○		
	•		
	•		
CLKVCT	DATA	CLKWP, CLKPC	

Figure 6. Real Time Clock



System Operation

During power up $\overline{RST1}$ must be activated (low) for a minimum of 2 clock cycles to force the S9901 into a known state. $\overline{RST1}$ will disable all interrupts, disable the clock, program all I/O ports to the mode, and force IC0-IC3 to (0,0,0,0) with $\overline{INTREQ}$ held high. System software must then enable the proper interrupts, program the clock (if used), and configure the I/O ports as required (see Table 4 for an example). After initial power up, the S9901 will be accessed only as needed to service the clock, enable (disable) interrupts, or read (write) data to the I/O ports. The I/O ports can be reconfigured by use of the $\overline{RST2}$ command bit.

Figure 7 illustrates the use of an S9901 with an S9900. The S9904 is used to generate $\overline{RST}$ to reset the 9900 and the 9901 (connected to $\overline{RST1}$). Figure 8 shows an S9980 system using the S9901. The reset function, load interrupt, and 4 maskable interrupts allowed in a 9980 are encoded as shown in Table 5. Connecting the system as shown ensures that the proper reset will be applied to the 9980.

Table 5 9980 Interrupt Level Data

Interrupt Code (IC0-IC2)	Function	Vector Location (Memory Address In Hex)	Device Assignment	Interrupt Mask Values To Enable (ST12 through ST15)
1 1 0	Level 4	0 0 1 0	External Device	4 Through F
1 0 1	Level 3	0 0 0 C	External Device	3 Through F
1 0 0	Level 2	0 0 0 8	External Device	2 Through F
0 1 1	Level 1	0 0 0 4	External Device	1 Through F
0 0 1	Reset	0 0 0 0	Reset Stimulus	Don't Care
0 1 0	Load	3 F F C	Load Stimulus	Don't Care
0 0 0	Reset	0 0 0 0	Reset Stimulus	Don't Care
1 1 1	No-Op	—	—	Don't Care

Figure 7. S9900-S9901 Interface

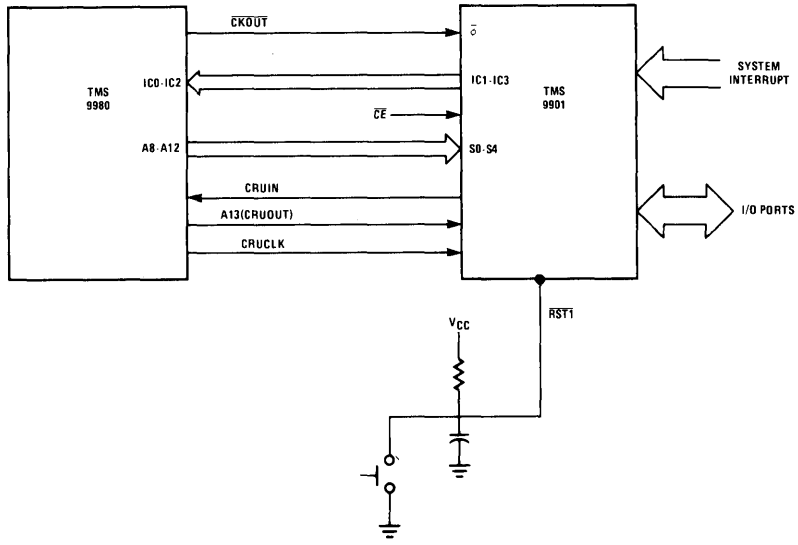
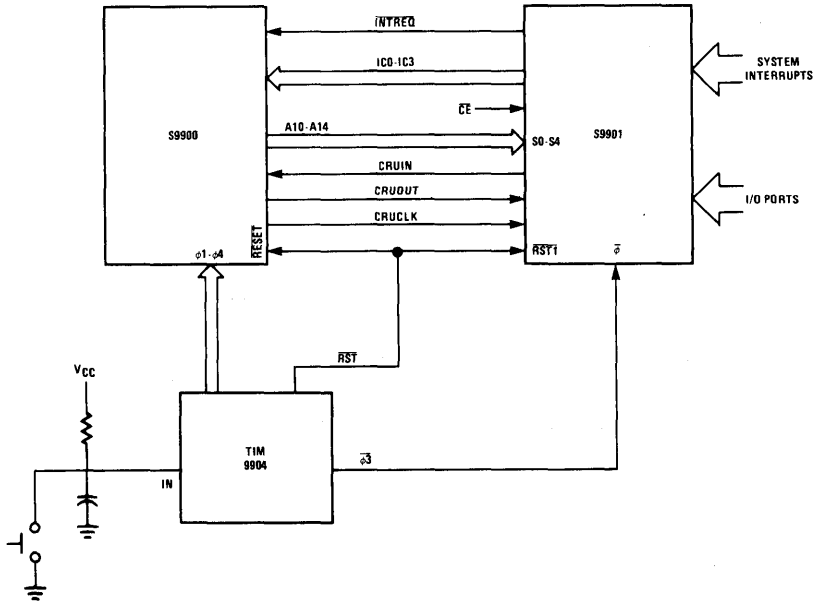


Figure 8. S9980-S9901 Interface



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S9902/S9902-4

Asynchronous Communications Controller (ACC)

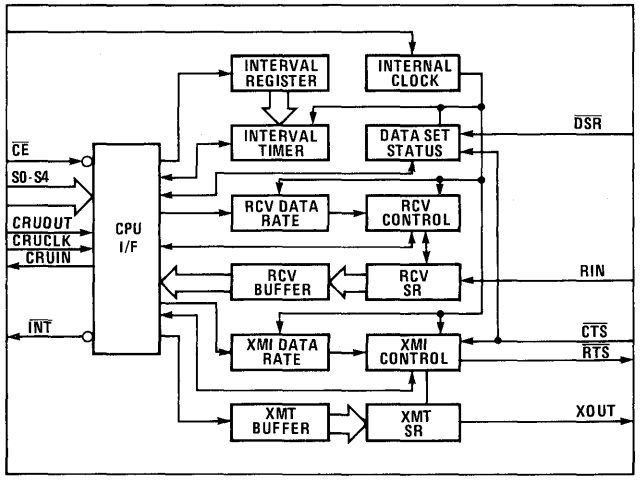
Features

- ☐ 5- to 8-Bit Character Length
- ☐ 1, 1½, or 2 Stop Bits
- ☐ Even, Odd, or No Parity
- ☐ Fully Programmable Data Rate Generation
- ☐ Interval Timer with Resolution from 64 to 16,320 μs
- ☐ Fully TTL Compatible, Including Single Power Supply

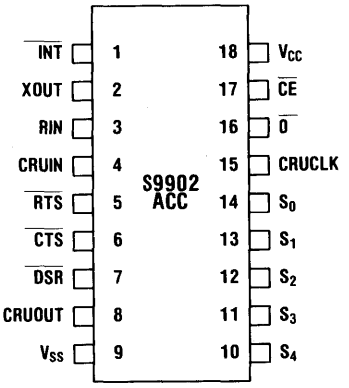
General Description

The S9902 Asynchronous Communication Controller (ACC) is a peripheral device for the S9900 family of microprocessors. The ACC provides an interface between the microprocessor and a serial asynchronous communication channel, performing the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor.

Block Diagram



S9902 Pin Configuration



S9900

S9902 Electrical Specifications

Absolute Maximum Ratings Over Operating Free Air Temperature Range (Unless Otherwise Noted)*

Supply Voltage, V_{CC}	−0.3V to +10V
All Input and Output Voltages	−0.3V to +10V
Continuous Power Dissipation	0.7W
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

**Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended period may affect device reliability.*

Recommended Operating Conditions

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5	5.25	V
Supply Voltage, V_{SS}		0		V
High-Level Input Voltage, V_{IH}	2.2	2.4	V_{CC}	V
Low-Level Input Voltage, V_{IL}		0.4	0.8	V
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics

Over Full Range of Recommended Operating Conditions (Unless Otherwise Noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_I	Input Current (Any Input)			±10	μA	V_I=0V to V_{CC}
V_{OH}	High Level Output Voltage	2.2	3.0		V	I_{OH}=100μA
		2.0	2.5			I_{OH}=−400μA
V_{OL}	Low Level Output Voltage		0.4	0.85	V	I_{OL}=3.2mA
$I_{CC(AV)}$	Average Supply Current from V_{CC}		2.5	100	mA	$t_{c(0)}$=250ns, T_A=25°C
C_i	Capacitance, Any Input		10		pF	f=1MHz,
C_o	Capacitance, Any Output		20			All other pins at 0V

Timing Requirements

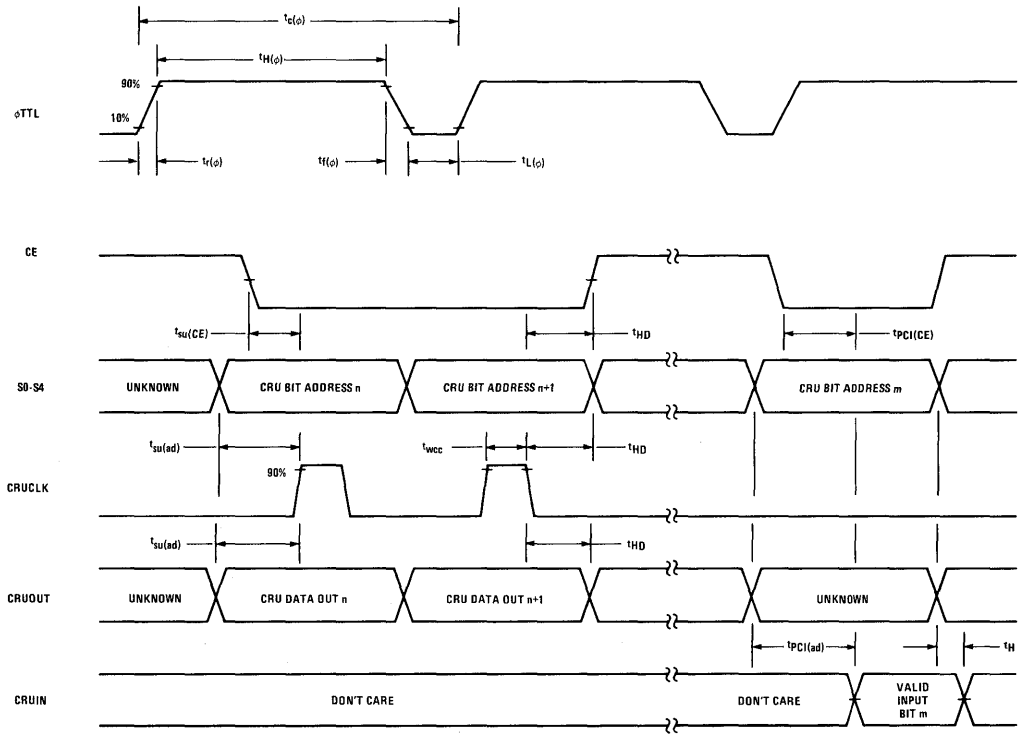
Over Full Range of Operating Conditions

Symbol	Parameter	S9902			S9902-4			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{c(0)}$	Clock Cycle Time	300	333	2000	240	250	667	ns
$t_{r(0)}$	Clock Rise Time	5	10	12	8		40	ns
$t_{f(0)}$	Clock Fall Time	225	10	12	10		40	ns
$t_{H(0)}$	Clock Pulse Low Width (High Level)		225	240	180			ns
$t_{L(0)}$	Clock Pulse Width (Low Level)	45	45	55	40			ns
$t_{su(ad)}$	Setup Time for Address and CRU_{OUT} Before CRU_{CLK}	180	220		150	150		ns
$t_{su(CE)}$	Setup Time for CE Before CRU_{CLK}	100	185		110	110		ns
t_{HD}	Hold Time for Address, CE and CRU_{OUT} After CRU_{CLK}	60	90		50	50		ns
t_{wcc}	CRU_{CLK} Pulse Width	100	120		80			ns

Switching Characteristics Over Full Range of Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
$T_{PCI(cd)}$	Propagation Delay, Address-to-Valid CRUIN			400	ns	C_L = 100pF
$T_{PCI(CE)}$	Propagation Delay, $\overline{CE}$-to-Valid CRUIN			400	ns	C_L = 100pF
t_H	CRUIN Hold Time After Address			20	ns	

Figure 3. Switching Characteristics



S9902 Pin Description

Table 1 defines the S9902 pin assignments and describes the function of each pin as shown in Figure 2.

Table 1

Signature	Pin	I/O	Description
$\overline{INT}$	1	O	Interrupt — when active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occured.
XOUT	2	O	Transmitter serial data output line — XOUT remains inactive (high) when S9902 is not transmitting.
RIN	3	I	Receiver serial data input line — RCV — must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receiver circuitry.
CRUIN	4	O	Serial data output pin from S9902 to CRUIN input pin of the CPU.
$\overline{RTS}$	5	O	Request-to-send output from S9902 to modem. This output is enabled by the CPU and remains active (low) during transmission from the S9902.
$\overline{CTS}$	6	I	Clear-to-send input from modem to S9902. When active (low), it enables the transmitter section of S9902.
$\overline{DSR}$	7	I	Data set ready input from modem to S9902. This input generates an interrupt when going On or Off.
CRUOUT	8	I	Serial data input line to S9902 from CRUOUT line of the CPU.
V_{SS}	9	I	Ground reference voltage.
S4 (LSB)	10	I	
S3	11	I	
S2	12	I	
S1	13	I	Address bus S0-S4 are the lines that are addressed by the CPU to select a particular S9902 function.
S0	14	I	
CRUCLK	15	I	CRU Clock. When active (high), S9902 from CRUOUT line of the CPU.
$\overline{\phi}$	16	I	TTL Clock.
$\overline{CE}$	17	I	Chip enable — when CE is inactive (high), the S9902 address decoding is inhibited which prevents execution of any S9902 command function. CRUIN remains at high-impedance when $\overline{CE}$ is inactive (high).
V_{CC}	18	I	Supply voltage (+5V nominal).

Device Interface

The relationship of the ACC to other components in the system is shown in Figures 4 and 5. The ACC is connected to the asychronous channel through level shifters which translate the TTL inputs and outputs to the appropriate levels (e.g., RS-232C, TTY current loop, etc.). The microprocessor transfers data to and from the ACC via the Communication Register Unit (CRU).

CPU Interface

The ACC interfaces to the CPU through the Communication Register Unit (CRU). The CRU interface consists of five address-select lines (S0-S4), chip enable ($\overline{CE}$), and three CRU control lines (CRUIN, CRUOUT, and CRUCLK). When $\overline{CE}$ becomes active (low), the five select lines address the CRU bit being accessed. When data is being transferred to the ACC from the CPU, CRUOUT contains the valid datum which is strobed by CRUCLK. When ACC data is being read, CRUIN is the datum output by the ACC.

Figure 4. S9902 ACC in an S9900 System

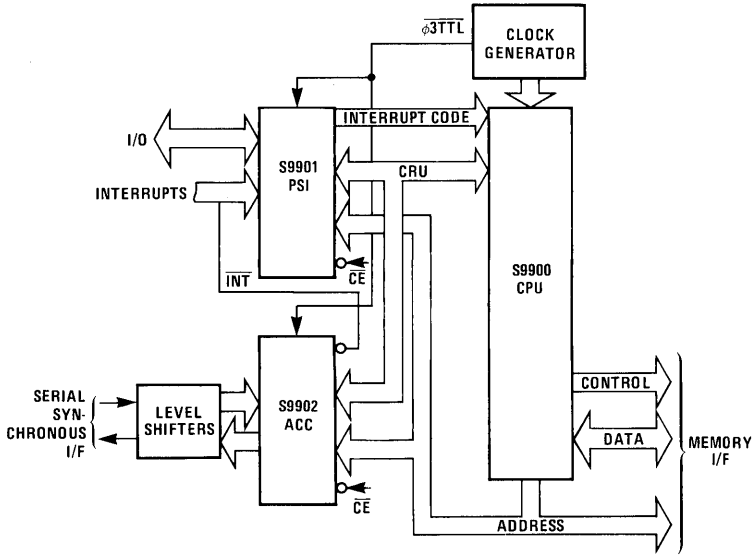
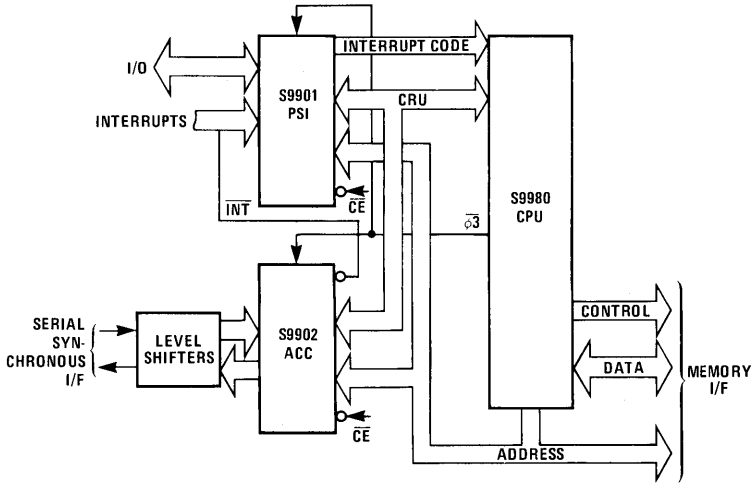


Figure 5. S9902 ACC in an S9980 System



Asynchronous Communication Channel Interface

The interface to the asynchronous communication channel consists of an output control line ($\overline{RTS}$), two input status lines ($\overline{DSR}$ and $\overline{CTS}$), and serial transmit (XOUT) and receive (RIN) data lines. The request-to-send line ($\overline{RTS}$) is active (low) whenever the transmitter is activated. However, before data transmission begins, the clear-to-send ($\overline{CTS}$) input must be active. The data set ready ($\overline{DSR}$) input does not affect the receiver or transmitter. When $\overline{DSR}$ or $\overline{CTS}$ changes level, an interrupt is generated.

Interrupt Output

The interrupt output ($\overline{INT}$) is active (low) when any of the following conditions occurs and the corresponding interrupt has been enabled by the CPU:

(1) $\overline{DSR}$ or $\overline{CTS}$ changes levels (DSCH = 1);

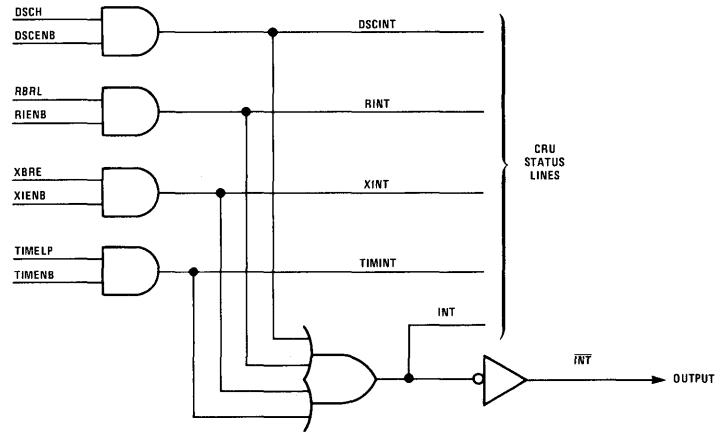
(2) a character has been received and stored in the Receiver Buffer Register (RBRL = 1);

(3) the Transmit Buffer Register is empty (XBRE = 1); or

(4) the selected time interval has elapsed (TIMELP = 1).

The logical relationship of the interrupt output is shown below.

$\overline{INT}$ Output Generation



Device Operation

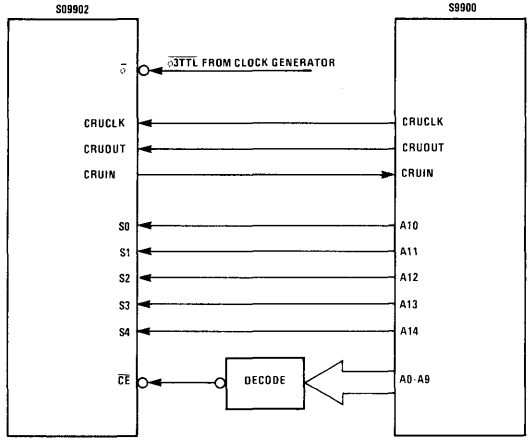
Clock Input

The clock input to the ACC ($\bar{\phi}$) is normally provided by the $\phi\bar{3}$ output of the clock generator (9900 systems) or the S9980 (9980 systems). This clock input is used to generate the internal device clock, which provides the time base for the transmitter, receiver, and interval timer of the ACC.

Control and Data Output

Data and control information is transferred to the ACC using $\overline{CE}$, S0-S4, CRUOUT, and CRUCLK. The diagrams below show the connection of the ACC to the S9900 and S9980 CPUs. The high-order CPU address lines are used to decode the $\overline{CE}$ signal when the device is being selected. The low-order address lines are connected to the five address-select lines (S0-S4). Table 2 describes the output bit address assignments for the ACC.

Connection of the ACC to the S9900



Connection of the ACC to the S9980 CPU's

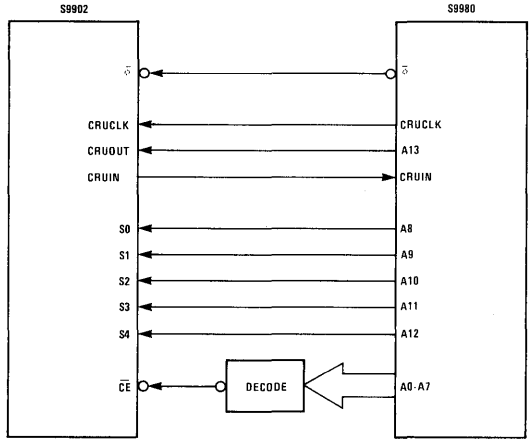


Table 2 S9902 ACC Output Bit Address Assignments

Address2 S0	S1	S2	S3	S4	Address10	Name	Description
1	1	1	1	1	31	RESET	Reset device.
					30-22		Not used.
1	0	1	0	1	21	DSCENB	Data Set Status Change Interrupt Enable.
1	0	1	0	0	20	TIMENB	Timer Interrupt Enable
1	0	0	1	1	19	XBIENB	Transmitter Interrupt Enable
1	0	0	1	0	18	RIENB	Receiver Interrupt Enable
1	0	0	0	1	17	BRKON	Break On
1	0	0	0	0	16	RTSON	Request to Send On
0	1	1	1	1	15	TSTMD	Test Mode
0	1	1	1	0	14	LDCTRL	Load Control Register
0	1	1	0	1	13	LDIR	Load Interval Register
0	1	1	0	0	12	LRDR	Load Receiver Data Rate Register
0	1	0	1	1	11	LXDR	Load Transmit Data Rate Register
					10-0		Control, Interval, Receive Data Rate, Transmit Data Rate, and Transmit Buffer Registers

Bit 31 (RESET) — Writing a one or zero to Bit 31 causes the device to be reset, disabling all interrupts, initializing the transmitter and receiver, setting $\overline{RTS}$ inactive (high), setting all register load control flags (LDCTRL, LDIR, LRDR, and LXDR) to a logic one level, and resetting the BREAK flag. No other input or output operations should be performed for $11\overline{\phi}$ clock cycles after issuing the RESET command.

Bit 30-Bit 22 — Not used.

Bit 21 (DSCENB) — Data Set Change Interrupt Enable. Writing a one to Bit 21 causes the $\overline{INT}$ output to be active (low) whenever DSCH (Data Set Status Change) is a logic one. Writing a zero to Bit 21 causes DSCH interrupts to be disabled. Writing either a one or zero to Bit 21 causes DSCH to be reset.

Bit 20 (TIMENB) — Timer Interrupt Enable. Writing a one to Bit 20 causes the $\overline{INT}$ output to be active whenever TIMELP (Timer Elapsed) is a logic one. Writing a zero to Bit 20 causes TIMELP interrupts to be disabled. Writing either a one or zero to Bit 20 causes TIMELP and TIMERR (Timer Error) to be reset.

Bit 19 (XBIENB) — Transmit Buffer Interrupt Enable. Writing a one to Bit 19 causes the $\overline{INT}$ output to be active whenever XBRE (Transmit Buffer Register Empty) is a logic one. Writing a zero to Bit 19 causes XBRE interrupts to be disabled. The state of XBRE is not affected by writing to Bit 19.

Bit 18 (RIENB) — Receiver Interrupt Enable. Writing a one to Bit 18 causes the $\overline{INT}$ output to be active whenever RBRL (Receiver Buffer Register Loaded) is a logic one. Writing a zero to Bit 18 disables RBRL interrupts. Writing either a one or zero to Bit 18 causes RBRL to be reset.

Bit 17 (BRKON) — Break On. Writing a one to Bit 17 causes the XOUT (Transmitter Serial Data Output) to go to a logic zero whenever the transmitter is active and the Transmit Buffer Register (XBR) and the Transmit Shift Register (XSR) are empty. While BRKON is set, loading of characters into the XBR is inhibited. Writing a zero to Bit 17 causes BRKON to be reset and the transmitter to resume normal operation.

Bit 16 (RTSON) — Request-to-Send On. Writing a one to Bit 16 causes the $\overline{RTS}$ output to be active (low). Writing a zero to Bit 16 causes $\overline{RTS}$ to go to a logic one after the XSR and XBR are empty, and BRKON is reset. Thus, the $\overline{RTS}$ output does not become inactive (high) until after character transmission has been completed.

Bit 15 (TSTMD) — Test Mode. Writing a one to Bit 15 causes $\overline{RTS}$ to be internally connected to $\overline{CTS}$, XOUT to be internally connected to RIN, $\overline{DSR}$ to be internally held low, and the Interval Timer to operate at 32 times its normal rate. Writing a zero to Bit 15 re-enables normal device operation.

Bits 14-11 — Register Load Control Flags. Output Bits 14-11 control which of the five registers will be loaded by writing to Bits 10-0. The flags are prioritized as shown in Table 3.

Table 3 S9902 ACC Register Load Selection

Register Load Control Flag Status				Register Enabled
LDCTRL	LDIR	LRDR	LXDR	
1	X	X	X	Control Register
0	1	X	X	Interval Register
0	0	1	X	Receive Data Rate Register
0	0	X	1	Transmit Data Rate Register
0	0	0	0	Transmit Buffer Register

Bit 14 (LDCTRL) — Load Control Register. Writing a one to Bit 14 causes LDCTRL to be set to a logic one. When LDCTRL = 1, any data written to bits 0-7 are directed to the Control Register. Note that LDCTRL is also set to a logic one when a one or zero is written to Bit 31 (RESET). Writing a zero to Bit 14 causes LDCTRL to be reset to a logic zero, disabling loading of the Control Register. LDCTRL is also automatically reset to a logic zero when a datum is written to Bit 7 of the Control Register which normally occurs as the last bit written when loading the Control Register with a LDCR instruction.

Bit 13 (LDIR) — Load Interval Register. Writing a one to Bit 13 causes LDIR to be set to a logic one. When LDIR = 1 and LDCTRL = 0, any data written to Bits 0-7 are directed to the Interval Register. Note that LDIR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Interval Register loading is not enabled until LDCTRL is set to a logic zero. Writing a zero to Bit 13 causes LDIR to be reset to logic zero, disabling loading of the Internal Register. LDIR is also automatically reset to logic zero when a datum is written to Bit 7 of the Interval Register, which normally occurs as the last bit written when loading the Interval Register with a LDCR instruction.

Bit 12 (LRDR) — Load Receive Data Rate Register. Writing a one to Bit 12 causes LRDR to be set to a logic one. When LRDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Receive Data Rate Register. Note that LRDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Receive Data Rate Register loading is not enabled until LDCTRL and LDIR have been set to a logic zero. Writing a zero to Bit 12 causes LRDR to be reset to a logic zero, disabling loading of the Receive Data Rate Register. LRDR is also automatically reset to logic zero when a datum is written to Bit 10 of the Receive Data Rate Register, which normally occurs as the last bit written when loading the Receive Data Rate Register with a LDCR instruction.

Bit 11 (LXDR) — Load Transmit Data Rate Register. Writing a one to Bit 11 causes LXDR to be set to a logic one. When LXDR = 1, LDIR = 0, and LDCTRL = 0, any data written to Bits 0-10 are directed to the Transmit Data Rate Register. Note that loading of both the Receive and Transmit Data Rate Registers is enabled when LDCTRL = 0, LDIR = 0, LRDR = 1, and LXDR = 1; thus these two registers may be loaded simultaneously when data are received and transmitted at the same rate. LXDR is also set to a logic one when a datum is written to Bit 31 (RESET); however, Transmit Data Rate Register loading is not enabled until LDCTRL and LDIR have been reset to logic zero. Writing a zero to Bit 11 causes LXDR to be reset to logic zero, disabling loading of the Transmit Data Rate Register. Since Bit 11 is the next bit addressed after loading the Transmit Data Rate Register, the register may be loaded and the LXDR flag reset with a single LDCR instruction where 12 bits (Bits 0-11) are written, with a zero written to Bit 11.

Control Register

The Control Register is loaded to select character length, device clock operation, parity, and the number of stop bits for the transmitter. Table 4 shows the bit address assignments for the Control Register.

Table 4 Control Register Bit Address Assignments

Address10	Name	Description
7	SBS1	← Stop Bit Select
6	SBS2	
5	PENB	Parity Enable
4	PODD	Odd Parity Select
3	CLK4M	ϕ Input Divide Select
2	—	Not Used
1	RCL1	← Character Length Select
0	RCL0	

7	6	5	4	3	2	1	0
SBS1	SBS2	PENB	PODD	CLK4M	NOT USED	RCL1	RCL0
MSB							LSB

Bits 7 and 6 (SBS1 and SBS2) — Stop Bit Selection. The number of stop bits to be appended to each transmitter character is selected by Bits 7 and 6 of the Control Register as shown below. The receiver only tests for a single stop bit, regardless of the status of Bits 7 and 6.

SBS1 Bit 7	SBS2 Bit 6	Number of Transmitted Stop Bits
0	0	1½
0	1	2
1	0	1
1	1	1

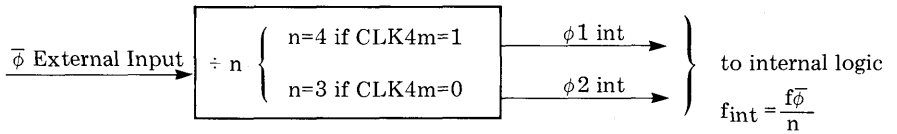
Stop Bit Selection

Bits 5 and 4
PENB and PODD) — Parity Selection. The type of parity to be generated for transmission and detected for reception is selected by Bits 5 and 4 of the Control Register as shown below. When parity is enabled (PENB = 1), the parity bit is transmitted and received in addition to the number of bits selected for the character length. Odd parity is such that the total number of ones in the character and parity bit, exclusive of stop bit(s), will be odd. For even parity, the total number of ones will be even.

PENB Bit 5	PODD Bit 4	PARITY
0	0	None
0	1	None
1	0	Even
1	1	Odd

Parity Selection

Bit 3 (CLK4M) — $\overline{\phi}$ Input Divide Select. The $\overline{\phi}$ input to the S9902 ACC is used to generate internal dynamic logic clocking and to establish the time base for the Interval Timer, Transmitter, and Receiver. The $\overline{\phi}$ input is internally divided by either 3 or 4 to generate the two-phase internal clocks required for MOS logic, and to establish the basic internal operating frequency (f_{int}) and internal clock period (t_{int}). When Bit 3 of the Control Register is set to a logic one (CLK4M = 1), $\overline{\phi}$ is internally divided by 4, and when CLK4M = 0, $\overline{\phi}$ is divided by 3. For example, when $f\overline{\phi}$ = 3 MHz, as in a standard 3 MHz S9900 system, and CLK4M = 0, $\overline{\phi}$ is internally divided by 3 to generate an internal clock period t_{int} of 1μs. The figure below shows the operation of the internal clock divider circuitry. The internal clock frequency should be no greater than 1. 1 MHz; thus, when $f\overline{\phi} > 3.3$ MHz, CLK4M should be set to a logic one.



Internal Clock Divider Circuitry

Bits 1 and 0
(RCL1 and RCL0) — Character Length Select. The number of data bits in each transmitted and received character is determined by Bits 1 and 0 of the Control Register as shown below.

RCL1 Bit 1	RCL0 Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Character Length Selection

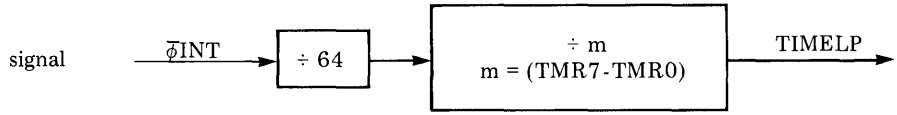
Interval Register

The Interval Register is enabled for loading whenever LDCTRL = 0 and LDIR = 1. The Interval Register is used for selecting the rate at which interrupts are generated by the Interval Timer of the ACC. The figure below shows the bit address assignments for the Interval Register when enabled for loading.

7	6	5	4	3	2	1	0
TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
MSB							LSB

Interval Register Bit Address Assignments

The figure below illustrates the establishment of the interval for the Interval Timer. As an example, if the Interval Register is loaded with a value of 80_{16} (128_{10}) the interval at which Timer Interrupts are generated is t_{ITVL} = t_{int} • 64 ◦ M = (1μs) (• 64) (• 128) = 8.192 ms. when t_{int} = 1μs.



frequency	fint	fint/64	fint/(64) (m)
time	tint	64 tint	64 m tint

Time Internal Selection

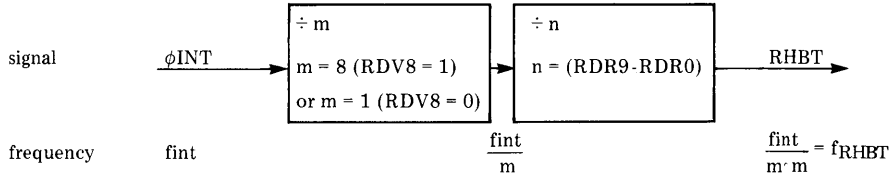
Receive Data Rate Register

The Receive Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LRDR = 1. The Receive Data Rate Register is used for selecting the bit rate at which data is received. The diagram shows the bit address assignments for the Receive Data Rate Register when enabled for loading.

10	9	8	7	6	5	4	3	2	1	0
RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0
MSB										LSB

Receive Data Rate Register Bit Address Assignments

The following diagram describes the manner in which the receive data rate is established. Basically, two programmable counters are used to determine the interval for one-half the bit period of receive data. The first counter either divides the internal system clock frequency (f_{int}) by either 8 (RDV8 = 1) or 1 (RDV8 = 0). The second counter has ten stages and may be programmed to divide its input signal by any value from 1 (RDR9-RDR0 = 0000000001) to 1023 (RDR8-RDR0 = 1111111111). The frequency of the output of the second counter (f_{RHBT}) is double the receive-data rate. Register is loaded with a value of 11000111000, RDV8 = 1, and RDR9-RDR0 = 1000111000 = 238_{16} = 568 10. Thus, for f_{int} = 1 MHz, the receive-data rate = 1 X 10^6 ÷ 8 ÷ 568 ÷ 2 = 110.04 bits per second.



Receive Data Rate Selection

Quantitatively, the receive-data rate f_{RCV} may be described by the following algebraic expression:

$$f_{RCV} = \frac{f_{RHBT}}{2} = \frac{f_{int}}{2mn} = \frac{f_{int}}{(2)\,(8^{RDV8})\,(RDR9\text{-}RDR0)}$$

Transmit Data Rate Register

The Transmit Data Rate Register is enabled for loading whenever LDCTRL = 0, LDIR = 0, and LXDR = 1. The Transmit Data Rate Register is used for selecting the data rate for the transmitter. The figure below shows the bit address assignments for the Transmit Data Rate Register.

10	9	8	7	6	5	4	3	2	1	0
XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0
MSB										LSB

Selection of transmit data rate is accomplished with the Transmit Data Rate Register in the same way that the receive data rate is selected when the Receive Data Rate Register. The algebraic expression for the Transmit Data Rate f_{XMT} is:

$$f_{XMT} = \frac{f_{XHBT}}{2} = \frac{f_{int}}{(2)\,(8^{XDV8})\,(XDR9\text{-}XDR0)}$$

For example, if the Transmit Data Rate Register is loaded with a value of 00110100001, XDV8 = 0, and XDR9-XDR0 = $1A1_{16}$ = 417, the transmit data rate = 1 X 10^6 ÷ 2 ÷ 1 ÷ 417 = 1199.04 bits per second.

Transmit Buffer Register

The Transmit Buffer Register is enabled for loading when LDCTRL = 0, LDIR = 0, LRDR = 0, LXDR = 0, and BRKON = 0. The Transmit Buffer Register is used for storage of the next character to be transmitted. When the transmitter is active, the contents of the Transmit Buffer Register are transferred to the Transmit Shift Register each time the previous character has been completely transmitted. The bit address assignments for the Transmit Buffer Register are shown below:

7	6	5	4	3	2	1	0
XBR7	XBR6	XBR5	XBR4	XBR3	XBR2	XBR1	XBR0
MSB							LSB

Transmit Buffer Register Bit Address Assignments

All 8 bits should be transferred into the register, regardless of the selected character length. The extraneous high-order bits will be ignored for transmission purposes; however, loading of bit 7 is internally detected to cause the Transmit Buffer Register Empty (XBRE) status flag to be reset.

Status and Data Input

Status and data information is read from the ACC using $\overline{CE}$, S0-S4, and CRUIN. The following figure illustrates the relationship of the signals used to access data from the ACC. Table 6 describes the input bit address assignments for the ACC.

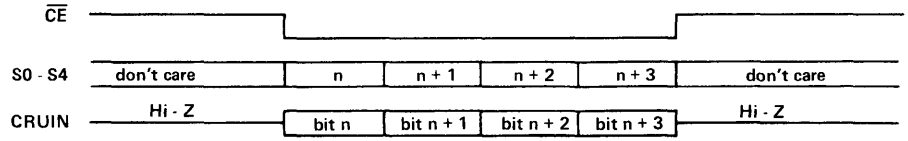


Table 5. CRU Output Bit Address Assignments

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESET	NOT USED									DSCENB	TIMENB	XBIENB	RIENB	BRKON	RTSON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSTMD	LDCTRL	LDIR	LRDR	LXDR	CONTROL, INTERVAL, RECEIVE DATA RATE, TRANSMIT DATA RATE, AND TRANSMIT BUFFER REGISTERS										

CONTROL REGISTER

1	X	X	X	SBS1	SBS2	PENB	PODD	CLK4M	–	RCL1	RCL0

Stop Bits: 00 1-1/2; 01 2; 1X 1

Party: 0X none; 10 even; 11 odd

fint = $f_{\phi}/(3+CLK4M)$

Character Length: 00 5; 01 6; 10 7; 11 8

INTERVAL REGISTER

0	1	X	X	TMR7	TMR 6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0

TMR

T_{ITVL} = tint X 64 X TMR

RECEIVE DATA RATE REGISTER

0	0	1	X	RDV8	RDR9	RDR8	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0

RDR

frcv = fint ÷ 8^{RDV8} ÷ RDR ÷ 2

TRANSMIT DATA RATE REGISTER

0	0	X	1	XDV8	XDR9	XDR8	XDR7	XDR6	XDR5	XDR4	XDR3	XDR2	XDR1	XDR0

XDR

fxmt = fint ÷ 8^{XDV8} ÷ XDR ÷ 2

TRANSMIT BUFFER REGISTER

0	0	0	0	XBR7	XBR6	XBR5	XBR4	XBR3	XBR2	XBR1	XBR0

NOTE 1: LOADING OF THE BIT INDICATED BY ☐ CAUSES THE LOAD CONTROL FLAG FOR THAT REGISTER TO BE AUTOMATICALLY RESET.

Table 6. S9902 ACC Input Bit Address Assignments

Address9 S0	S1	S2	S3	S4	Address10	Name	Description
1	1	1	1	1	31	INT	Interrupt
1	1	1	1	0	30	FLAG	Register Load Control Flag Set
1	1	1	0	1	29	DSCH	Data Set Status Change
1	1	1	0	0	28	CTS	Clear to Send
1	1	0	1	1	27	DSR	Data Set Ready
1	1	0	1	0	26	RTS	Request to Send
1	1	0	0	1	25	TIMELP	Timer Elapsed
1	1	0	0	0	24	TIMERR	Timer Error
1	0	1	1	1	23	XSRE	Transmit Shift Register Empty
1	0	1	1	0	22	XBRE	Transmit Buffer Register Empty
1	0	1	0	1	21	RBRL	Receive Buffer Register Loaded
1	0	1	0	0	20	DSCINT	Data Set Status Charge Interrupt (DSCH · DSCENB)
1	0	0	1	1	19	TIMINT	Timer Interrupt (TIMELP · TIMENB)
1	0	0	1	0	18	—	Not used (always = 0)
1	0	0	0	1	17	XBINT	Transmitter Interrupt (XBRE · XBIENB)
1	0	0	0	0	16	RBINT	Receiver Interrupt (RBRL · RIENB)
0	1	1	1	1	15	RIN	Receive Input
0	1	1	1	0	14	RSBD	Receive Start Bit Detect
0	1	1	0	1	13	RFBD	Receive Full Bit Detect
0	1	1	0	0	12	RFER	Receive Framing Error
0	1	0	1	1	11	ROVER	Receive Overrun Error
0	1	0	1	0	10	RPER	Receive Parity Error
0	1	0	0	1	9	RCVERR	Receive Error
0	1	0	0	0	8	—	Not used (always = 0)
					7-0	RBR7-RBR0	Receive Buffer Register (Received Data)

Bit 31 (INT) — INT = DSCINT + TIMINT + XBINT + RBINT. The interrupt output ($\overline{INT}$) is active when this status signal is a logic 1.

Bit 30 (FLAG) — FLAG = LDCTRL + LDIR + LRDR + LXDR + BRKON. When any of the register load control flags or BRKON is set, FLAG = 1.

Bit 29 (DSCH) — Data Set Status Change Enable. DSCH is set when the $\overline{DSR}$ or $\overline{CTS}$ input changes state. To ensure recognition of the state change, $\overline{DSR}$ or $\overline{CTS}$ must remain stable in its new state for a minimum of two internal clock cycles. DSCH is reset by an output to bit 21 (DSCENB).

Bit 28 (CTS) — Clear to Send. The CTS signal indicates the inverted status of the $\overline{CTS}$ device input.

Bit 27 (DSR) — Data Set Ready. The DSR signal indicates the inverted status of the $\overline{DSR}$ device input.

Bit 26 (RTS) — Request to Send. The RTS signal indicates the inverted status of the $\overline{RTS}$ device output.

Bit 25 (TIMELP) — Timer Elapsed. TIMELP is set each time the Interval Timer decrements to 0. TIMELP is reset by an output to bit 20 (TIMENB).

Bit 24 (TIMERR) — Timer Error. TIMERR is set whenever the Interval timer decrements to 0 and TIMELP is already set, indicating that the occurrence of TIMELP was not recognized and cleared by the CPU before subsequent intervals elapsed. TIMERR is reset by an output to bit 20 (TIMENB).

Bit 23 (XSRE) — Transmit Shift Register Empty. When XSRE = 1, no data is currently being transmitted and the XOUT output is at logic 1 unless BRKON is set. When XSRE = 0, transmission of data is in progress.

Bit 22 (XBRE) — Transmit Buffer Register Empty. When XBRE = 1, the transmit buffer register does not contain the next character to be transmitted. XBRE is set each time the contents of the transmit buffer register are transferred to the transmit shift register, XBRE is reset by an output to bit 7 of the transmit buffer register (XBR7), indicating that a character has been loaded.

Bit 21 (RBRL) — Receive Buffer Register Loaded. RBRL is set when a complete character has been assembled in the receive shift register and the character is transferred to the receive buffer register. RBRL is reset by an output to bit 18 (RIENB).

Bit 20 (DSCINT) — Data Set Status Change Interrupt. DSCINT = DSCH (input bit 29) · DSCENB (output bit 21). DSCINT indicates the presence of an enabled interrupt caused by the changing of state of $\overline{\text{DSR}}$ or $\overline{\text{CTS}}$.

Bit 19 (TIMINT) — Timer Interrupt. TIMINT = TIMELP (input bit 25) · TIMENB (output bit 20). TIMINT indicates the presence of an enabled interrupt caused by the interval timer.

Bit 17 (XBINT) — Transmitter Interrupt. XBINT = XBRE (input bit 22) · XBIENB (output bit 19). XBINT indicates the presence of an enabled interrupt caused by the transmitter.

Bit 16 (RBINT) — Receiver Interrupt. RBINT = RBRL (input bit 21) · RIENB (output bit 18). RBINT indicates the presence of an enabled interrupt caused by the receiver.

Bit 15 (RIN) — Receive Input. RIN indicates the status of the RIN input to the device.

Bit 14 (RSBD) — Receive Start Bit Detect. RSBD is set one-half bit time after the 1-to-0 transition of RIN indicating the start bit of a character. If RIN is not still 0 at this point in time, RSBD is reset. Otherwise, RSBD remains true until the complete character has been received. This bit is normally used for testing purposes.

Bit 13 (RFBD) — Receive Full Bit Detect. RFBD is set one bit time after RSBD is set to indicate the sample point for the first data bit of the received character. RSBD is reset when the character has been completely received. This bit is normally used for testing purposes.

Bit 12 (RFER) — Receive Framing Error. RFER is set when a character is received in which the stop bit, which should be a logic 1, is a logic 0. RFER should only be read when RBRL (input bit 21) is a 1. RFER is reset when a character with the correct stop bit is received.

Bit 11 (ROVER) — Receive Overrun Error. ROVER is set when a new character is received before the RBRL flag (input bit 21) is reset, indicating that the CPU failed to read the previous character and reset RBRL before the present character is completely received. ROVER is reset when a character is received and RBRL is 0 when the character is transferred to the receive buffer register.

Bit 10 (RPER) — Receive Parity Error. RPER is set when a character is received in which the parity is incorrect. RPER is reset when a character with correct parity is received.

Bit 9 (RCVERR) — Receive Error. RCVERR = RFER + ROVER + RPER. RCVERR indicates the presence of an error in the most recently received character.

Bit 7-Bit 0 (RBR7-RBR0) — Receive Buffer Register. The receive buffer register contains the most recently received character. For character lengths of fewer than 8 bits the character is right justified, with unused most significant bit(s) all zero(es). The presence of valid data in the receive buffer register is indicated when RBRL is a logic 1.

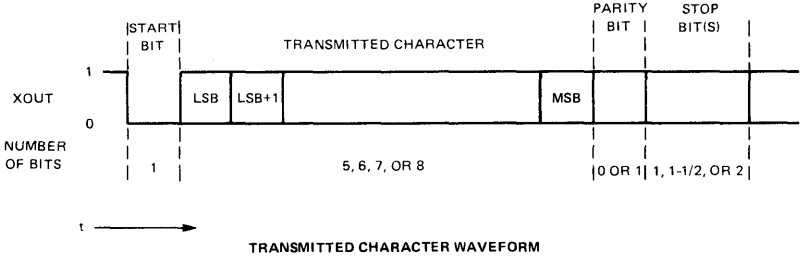
Transmitter Operation

Transmitter Initialization

The operation of the transmitter is described in the following flowchart. The transmitter is initialized by issuing the RESET command (output to bit 31), which causes the internal signals XSRE and XBRE to be set, and BRKON to be reset. Device outputs $\overline{RTS}$ and XOUT are set, placing the transmitter in its idle state. When RTSON is set by the CPU, the $\overline{RTS}$ output becomes active and the transmitter becomes active when $\overline{CTS}$ goes low.

Data Transmission

If the Transmit Buffer Register contains a character, transmission begins. The contents of the Transmit Buffer Register are transferred to the Transmit Shift Register, causing XSRE to be reset and XBRE to be set. The first bit transmitted (start bit) is always a logic 0. Subsequently, the character is shifted out, LSB first. Only the number of bits specified by RCL1 and RCL0 (character length select) of the Control Register are shifted. If parity is enabled, the correct parity bit is next transmitted. Finally the stop bit(s) selected by SBS1 and SBS0 of the Control Register are transmitted. Stop bits are always logic one. XSRE is set to indicate that no transmission is in progress, and the transmitter again tests XBRE to determine if the CPU has yet loaded the next character. The waveform for a transmitted character is shown below.



TRANSMITTED CHARACTER WAVEFORM

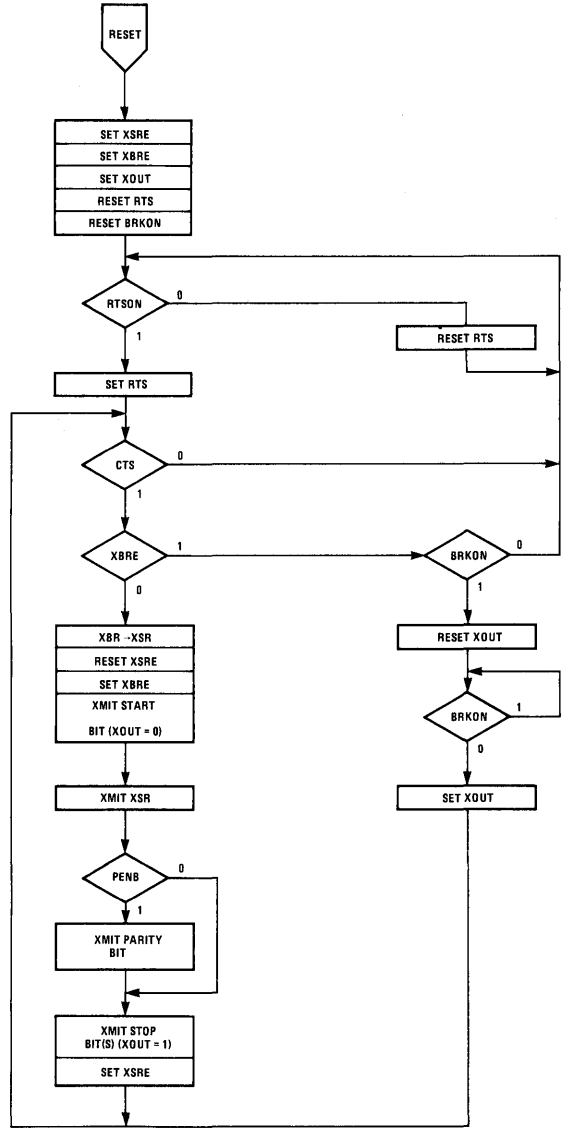
BREAK Transmission

The BREAK message is transmitted only if XBRE = 1, $\overline{CTS}$ = 9, and BRKON = 1. After transmission of the BREAK message begins, loading of the Transmit Buffer Register is inhibited and XOUT is reset. When BRKON is reset by the CPU, XOUT is set and normal operation continues. It is important to note that characters loaded into the Transmit Buffer Register are transmitted prior to the BREAK message regardless of whether the character has been loaded into the Transmit Shift Register before BRKON is set. Any character to be transmitted subsequent to transmission of the BREAK message may not be loaded into the Transmit Buffer Regiser until after BRKON is reset.

Transmission Termination

Whenever XSRE = 1 and BRKON = 0, the transmitter is idle, with XOUT set to one. If RTSON is reset at this time, the $\overline{RTS}$ device output will go inactive, disabling further data transmission until RTSON is again set. $\overline{RTS}$ will not go inactive, however, until any characters loaded into the Transmit Buffer Register prior to resetting RTSON are transmitted and BRKON = 0.

S9902 Transmitter Operation



Receiver Operation

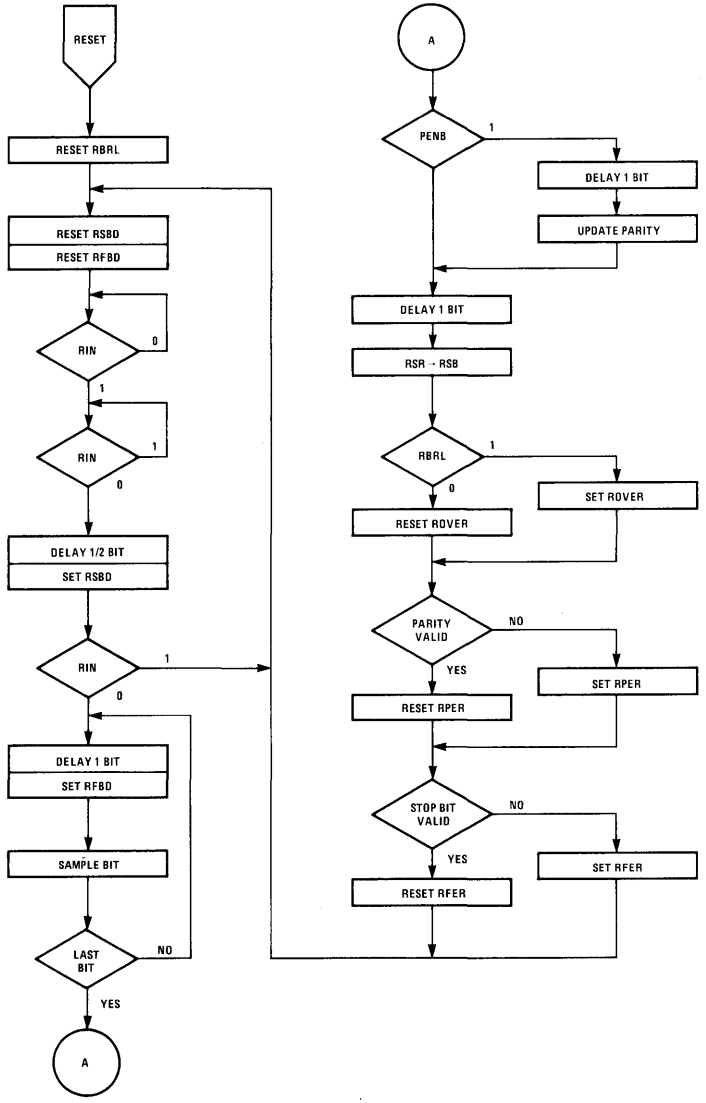
Receiver Initialization

Operation of the S9902 receiver is described in the following flowchart. The receiver is initialized any time the CPU issues the RESET command. The RBRL flag is reset to indicate that no character is currently in the Receive Buffer Register, and the RSBD and RFBD flags are reset. The receiver remains in the inactive state until a 1 to 0 transition is detected on the RIN device input.

Start Bit Detection

The receiver delays one-half bit time and again samples RIN to ensure that a valid start bit has been detected. If RIN = 0 after the half-bit delay, RSBD is set and data reception begins. If RIN = 1 no data reception occurs.

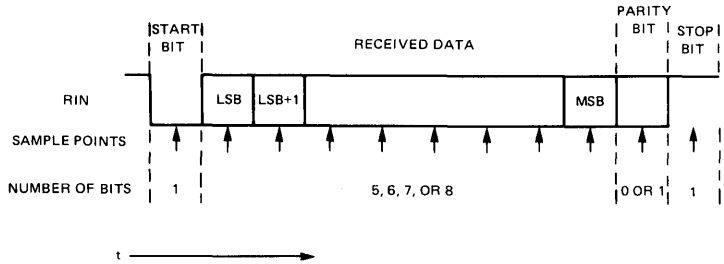
S9902 Receiver Operation



Data Reception

In addition to verifying the valid start bit, the half-bit delay after the 1-to-0 transition also establishes the sample point for all subsequent data bits in this character. Theoretically, the sample point is in the center of each bit cell, thus maximizing the limits of acceptable distortion of data cells. After the first full bit delay, the least significant data bit is received and RFBD is set. The receiver continues to delay one-bit intervals and sample RIN until the selected number of bits is received. If parity is enabled, one additional bit is read for parity. After an additional bit delay, the received character is transferred to the Receive Buffer Register, RBRL is set, ROVER and RPER are loaded with appropriate values, and RIN is tested for a valid stop bit. If RIN = 1, the stop bit is valid. RFER, RSBD, and RFBD are reset and the receiver waits for the next start bit to begin reception of the next character.

If RIN = 0 when the stop bit is sampled, RFER is set to indicate the occurrence of a framing error. RSBD and RFBD are reset but sampling for the start bit of the next character does not begin until RIN = 1.

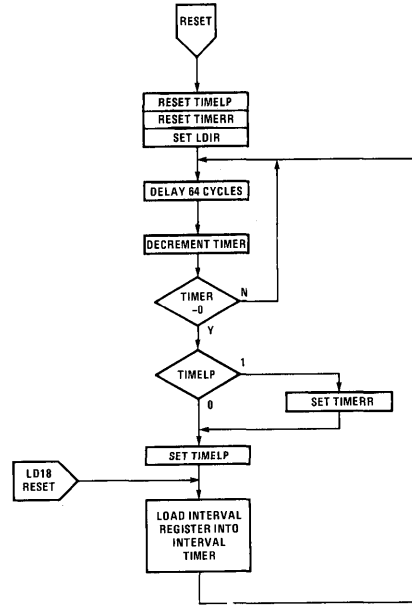


CHARACTER RECEPTION TIMING

Interval Timer Operation

A flowchart of the operation of the Interval Timer is shown below. Execution of the RESET command by the CPU causes TIMELP and TIMERR to be reset and LDIR to be set. Resetting LDIR causes the contents of the Interval Register to be loaded into the Interval Timer, thus beginning the selected time interval. The timer is decremented every 64 internal clock cycles (every 2 internal clock cycles when in Test Mode) until it reaches zero, at which time the Interval Timer is reloaded by the Interval Register and TIMELP is set. If TIMELP was already set, TIMERR is set to indicate that TIMELP was not cleared by the CPU before the next time period elapsed. Each time LDIR is reset the contents of the Interval Register are loaded into the Interval Timer, thus restarting the time.

Interval Timer Operation



Device Application

This section describes the software interface between the CPU and the S9902 ACC and discusses some of the design considerations in the use of this device in asynchronous communications applications.

Device Initialization

The ACC is initialized by the CPU issuing the RESET command, followed by loading the Control, Interval, Receive Data Rate, and Trasmit Data Rate registers. Assume that the value to be loaded into the CRU Base Register (register 12) in order to point to bit 0 is 0040_{16}. In this application, characters will have 7 bits of data plus even parity and one stop bit. The ϕ input to the ACC is a 3MHz signal. The ACC will divide this signal frequency by 3 to generate an internal clock frequency of 1MHz. An interrupt will be generated by the Interval Timer every 1.6 milliseconds when timer interrupts are enabled. The transmitter will operate at a data rate of 300 bits per second and the receiver will operate at 1200 bits per second. Had it been desired that both the transmitter and receiver operate at 300 bits per second, the "LDCR @RDR,11" instruction would have been deleted, and the "LDCR @XDR,12" instruction would have caused both data rate registers to be loaded and LRDR and LXDR to have been reset.

Initialization Program

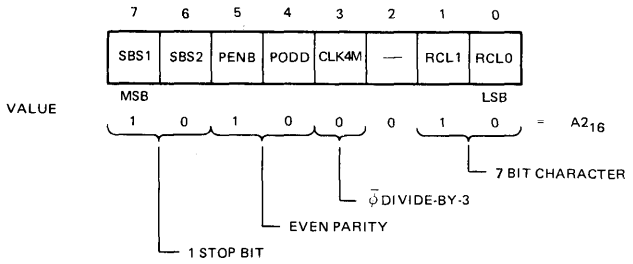
The initialization program for the configuration previously described is as shown below. The RESET command disables all interrupts, initializes all controllers, sets the four register load control flags (LDCTRL, LDIR, LRDR, and LXDR). Loading the last bits of each of the registers causes the load control flag to be automatically reset.

```
        LI      R12,>40         INITIALIZE CRU BASE
        SBO     31              RESET COMMAND
        LDCR    @CNTRL, 8       LOAD CONTROL AND RESET LDCTRL
        LDCR    @INTVL, 8       LOAD INTERVAL AND RESET LDIR
        LDCR    @RDR, 11        LOAD RDR AND RESET LRDR
        LDCR    @XDR, 12        LOAD XDR AND RESET LXDR
          •
          •
          •
CNTRL   BYTE    >A2
INTVL   BYTE    1600/64
RDR     DATA    >1A1
XDR     DATA    >4DO
```

The RESET command initializes all subcontrollers, disables interrupts, and sets LDCTRL, LDIR, LRDR, and LXDR, enabling loading of the control register.

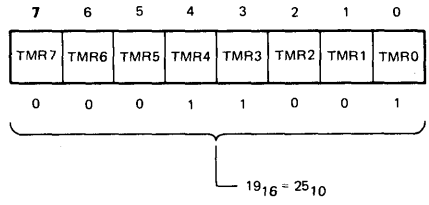
Control Register

The options described previously are selected by loading the value shown below.



Interval Register

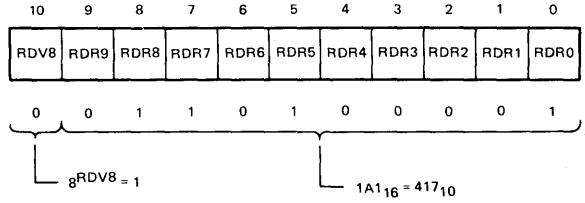
The interval register is to be set up to generate an interrupt every 1.6 milliseconds. The value loaded into the interval register specifies the number of 64 microsecond increments in the total interval.



25 X 64 MICROSECONDS = 1.6 MILLISECONDS

Receive Data Rate Register

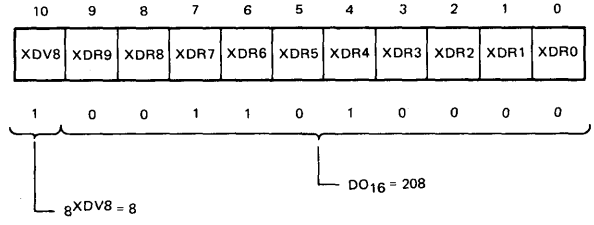
The data rate for the receiver is to be 1200 bits per second. The value to be loaded into the Receive Data Rate Register is as shown:



$10^6 \div 1 \div 417 \div 2 = 1199.04$ BITS PER SECOND

Transmit Data Rate Register

The data rate for the transmitter is to be 300 bits per second. The value to be loaded into the Transmit Data Rate Register is:



1 X $10^6 \div 8 \div 208 \div 2 = 300.48$ BITS PER SECOND

Data Transmission

The subroutine shown below demonstrates a simple loop for the transmitting of a block of data.

```
        LI      R0, LISTAD      INITIALIZE LIST POINTER
        LI      R1, COUNT       INITIALIZE BLOCK COUNT
        LI      R12, CRUBAS     INITIALIZE CRU BASE
        SBO     16              TURN OFF TRANSMITTER
XMTLP   TB      22              WAIT FOR XBRE = 1
        JNE     XMTLP
        LDCR    *R0+,8          LOAD CHARACTER INCREMENT POINTER RESET XBRE
        DEC     R1              DECREMENT COUNT
        JNE     XMTLP           LOOP IF NOT COMPLETE
        SBZ     16              TURN OFF TRANSMITTER
```

After initializing the list pointer, block count, and CRU base address. RTSON is set to cause the transmitter and the RTS output to become active. Data transmission does not begin, however, until the CTS input becomes active. After the final character is loaded into the transmit buffer register, RTSON is reset. The transmitter and the RTS output do not become inactive until the final character has been completely transmitted.

Data Reception

The software shown below will cause a block of data to be received and stored in memory.

```
CARRET  BYTE    >OD
RCVBLK  LI      R2, RCVLST      INITIALIZE LIST COUNT
        LI      R3, MXRCNT      INITIALIZE MAX COUNT
        LI      R4, CARRET      SET UP END OF BLOCK CHARACTER
RCVLP   TB      21              WAIT FOR RBRL = 1
        JNE     RCVLP
        STCR    *R2,8           STORE CHARACTER
        SBZ     18              RESET RBRL
        DEC     R3              DECREMENT COUNT
        JEQ     RCVEND          END IF COUNT = 0
        CB      *R2+, R4        COMPARE TO EOB CHARACTER, INCREMENT POINTER
        JNE     RCVLP           LOOP IF NOT COMPLETE
RCVEND  RT                      END OF SUBROUTINE
```

Register Loading After Initialization

The control, interval, and data rate registers may be reloaded after initialization. For example, it may be desirable to change the interval of the timer. Assume, for sample, that the interval is to be changed to 10.24 milliseconds. The instruction sequence is as follows:

```
        SB0     13              SET LOAD CONTROL FLAG
        LDCR    @INTVL2,8       LOAD REGISTER, RESET FLAG
          •
          •
          •
INTVL2  BYTE    10240/64
```

Caution should be exercised when transmitter interrupts are enabled to ensure that the transmitter interrupt does not occur while the load control flag is set. For example, if the transmitter interrupts between execution of the "SBO 13" and the next instruction, the transmit buffer is not enabled for loading when the transmitter interrupt service routine is entered because the LDIR flag is set. This situation may be avoided by the following sequence:

```
            BLWP    @INTVCHG        CALL SUBROUTINE
              •
              •
              •
ITV CPC     LI MI   0               MASK ALL INTERRUPTS
            MOV     @24(R13), RIZ   LOAD CRU BASE ADDRESS
            SB0     13              SET FLAG
            LDCR    @INTVL2,8       LOAD REGISTER AND RESET FLAG
            RTWP                    RESTORE MASK AND RETURN
              •
              •
              •
ITVCHG      DATA    ACCWP, ITVCPC
INTVL2      BYTE    10240/64
```

In this case all interrupts are masked, ensuring that all interrupts are disabled while the load control flag is set.

AMERICAN MICROSYSTEMS, INC.

Random Access Memories (RAMs)

AMERICAN MICROSYSTEMS, INC.

Memory Products Selection Guide

STATIC MOS RANDOM ACCESS MEMORIES

Part No.	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S68B10	128×8	NMOS	250	420	N/A	+5V	24 Pin
S68A10	128×8	NMOS	360	420	N/A	+5V	24 Pin
S6810	128×8	NMOS	450	400	N/A	+5V	24 Pin
S6810-1	128×8	NMOS	575	500	N/A	+5V	24 Pin

STATIC CMOS RANDOM ACCESS MEMORIES

Part No.	Organization	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S5101L-1	256×4	450	115	.055	+5V	22 Pin
S5101L	256×4	650	115	.055	+5V	22 Pin
S5101L-3	256×4	650	115	.735	+5V	22 Pin
S5101-8	256×4	800	115	2.7	+5V	22 Pin
S6501L-1	256×4	450	115	.055	+5V	22 Pin
S6501L	256×4	650	115	.055	+5V	22 Pin
S6501L-3	256×4	650	115	.735	+5V	22 Pin
S6501-8	256×4	800	115	2.7	+5V	22 Pin
S6504	4096×1	300	75	0.5	+5V	18 Pin
S6508-1	1024×1	300	13	.055	+5V	16 Pin
S6508	1024×1	460	13	.55	+5V	16 Pin
S6508A	1024×1	460/185[1]	12.5/50[1]	1.1	+4V to +11V	16 Pin
S6514	1024×4	300	75	0.25	+5V	18 Pin
S6516	2048×8	230	55MHz	5.5	+5V	24 Pin

MOS READ ONLY MEMORIES

Part No.	Description	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Power Supplies	Package
S68A316	16,384 Bit Static ROM	2048×8	NMOS	350	370	+5	24 Pin
S68B316	16,384 Bit Static ROM	2048×8	NMOS	250	275	+5	24 Pin
S68332	32,768 Bit Static ROM	4096×8	NMOS	450	370	+5	24 Pin
S68A332	32,768 Bit Static ROM	4096×8	NMOS	350	370	+5	24 Pin
S2333	32,768 Bit Static ROM	4096×8	NMOS	350	385	+5	24 Pin
S68116	16,384 Bit Static ROM	2048×8	NMOS	110	605	+5	24 Pin
S68132	32,768 Bit Static ROM	4096×8	NMOS	115	633	+5	24 Pin
S68164	65,536 Bit Static ROM	8192×8	NMOS	120	660	+5	24 Pin
S68A364	65,536 Bit Static ROM	8192×8	NMOS	350	385	+5	24 Pin
S68B364	65,536 Bit Static ROM	8192×8	NMOS	250	495	+5	24 Pin
S4264	65,536 Bit Static ROM	8192×8	NMOS	300	440	+5	24 Pin
S2364	65,536 Bit Static ROM	8192×8	NMOS	350	385	+5	28 Pin
S23128	131,072 Bit Static ROM	16384×8	NMOS	250	385	+5	28 Pin
S23256	262,144 Bit Static ROM	32768×8	NMOS	150	220	+5	28 Pin

AMERICAN MICROSYSTEMS, INC.

S5101

1024 BIT (256×4) STATIC CMOS RAM

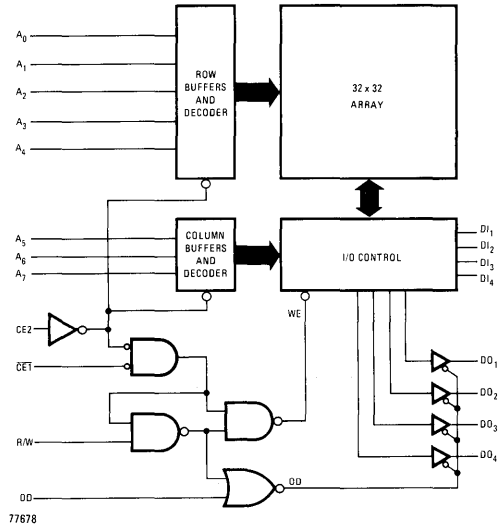
Features

- ☐ Ultra Low Standby Power
- ☐ Data Retention at 2V (L Version)
- ☐ Single +5V Power Supply
- ☐ Completely Static Operation
- ☐ Completely TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Available in Commercial, Industrial, and Military Temperature Range

General Description

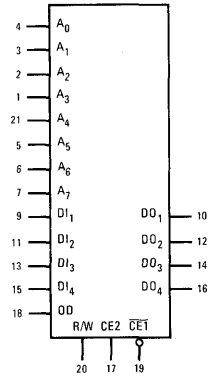
The AMI S5101 family of 256× 4-bit ultra low power CMOS RAMs offers fully static operation with a single +5 volt power supply. All inputs and outputs are directly TTL compatible. With data inputs and outputs on adjacent pins, either separate or common data I/O operations can easily be implemented for maximum design flexibility. The three-state outputs will drive one full TTL load and are disabled (high impedance state) by output disable (OD), either chip enable ($\overline{CE1}$ or CE2), or in a write cycle (R/W = LOW). This facilitates the control of common data I/O systems.

Block Diagram



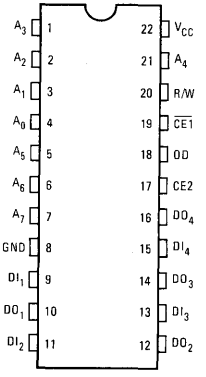
77678

Logic Symbol



877302

Pin Configuration



877301

Truth Table

$\overline{CE1}$	CE2	OD	R/W	DIN	Output	Mode
H	X	X	X	X	High Z	Not selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	*High Z	Write
L	H	L	H	X	Dout	Read

*Also available with D_{IN} on output during Write—consult AMI Sales Office

Pin Names

A_0 - A_7	Address Inputs	$\overline{CE1}$	Chip Enable
DI_1 - DI_4	Data Inputs	CE2	Chip Enable
DO_1 - DO_4	Data Outputs	R/W	Read/Write Input
OD	Output Disable	V_{CC}	+5 Volt Power Supply

RAMs

General Description (Continued)

The stored data is read out nondestructively and is the same polarity as the original input data. The S5101 is totally static, making clocks unnecessary for a new address to be accepted. The device has two chip enable inputs ($\overline{CE1}$ and CE2) allowing easy system expansion. CE2 disables the entire device but $\overline{CE1}$ does not disable the address buffers and decoders. Thus, minimum power dissipation is achieved when CE2 is low.

The L version of the S5101 has the additional feature of guaranteed data retention with the power supply as low as 2 volts. This makes the device an ideal choice when battery augmented non-volatile RAM storage is mandatory.

The S5101 is fabricated using a silicon gate CMOS process suitable for high volume production of ultra low power, high performance memories.

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
(Military temp part)	−55°C to +125°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage	8V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
I_{LI}	Input Leakage Current			1	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			1	μA	$\overline{CE1}$ = V_{IH} V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			22	mA	Outputs = Open, V_{IN} = V_{IL} to V_{CC}
I_{CCL}	Standby Supply Current	S5101L1, S5101L		10	μA	V_{IN} = 0V to V_{CC}
		S5101L3		140	μA	except
		S5101L8, S5101-8		500	μA	CE2 ⩽ 0.2V
V_{IL}	Input Low Voltage		-0.3	0.65	V	
V_{IH}	Input High Voltage		2.2	V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = -1 mA

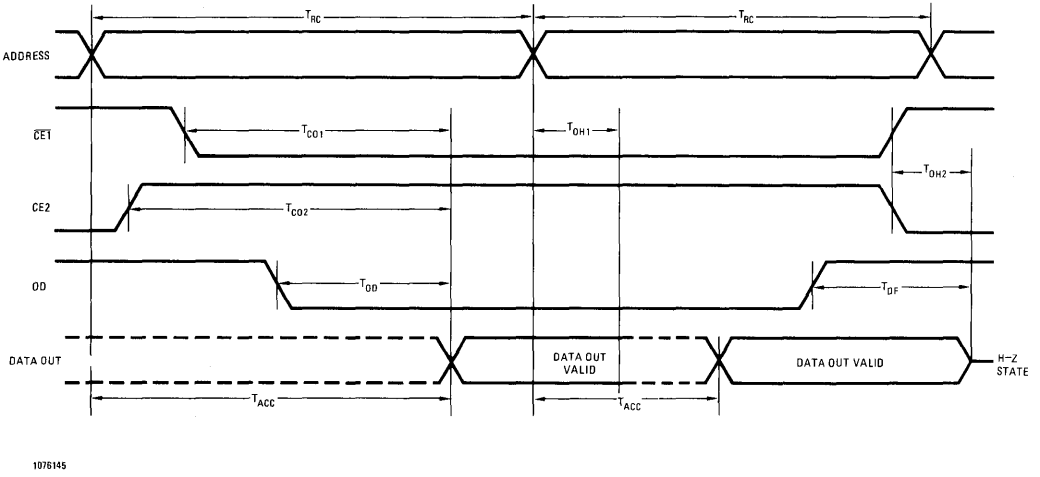
Capacitance

Symbol	Parameter	Limits Min.	Limits Max.	Units	Conditions
C_{IN}	Input Capacitance		8	pF	V_{IN} = 0V, on all Input Pins
C_O	Output Capacitance		12	pF	V_O = 0V

A.C. Characteristics for Read Cycle: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter	S5101L1 Limits		S5101L S5101L3 Limits		S5101L8 S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{RC}	Read Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{ACC}	Access Time		450		650		800	ns	
T_{CO1}	$\overline{CE1}$ to Output Delay		400		600		800	ns	
T_{CO2}	CE2 to Output Delay		500		700		850	ns	
T_{OD}	Output Disable to Enabled Output Delay		250		350		450	ns	
T_{DF}	Output Disable to Output H-Z State Delay	0	130	0	150	0	200	ns	
T_{OH1}	Output Data Valid Into Next Cycle with respect to Address	0		0		0		ns	
T_{OH2}	Output Data Valid Into Next Cycle with respect to Chip Enable	0		0		0		ns	

Read Cycle



1076145

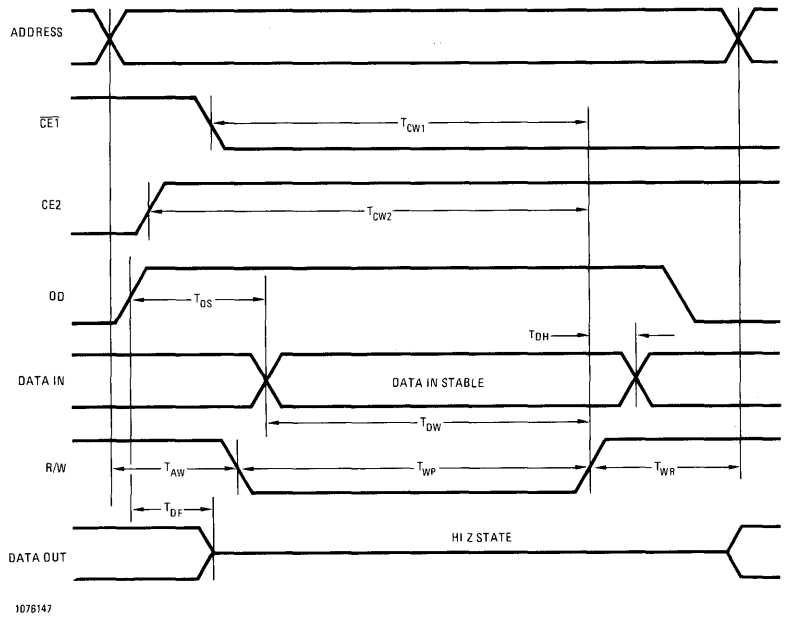
Note:
1. OD may be tied low for seaprate I/O information.
2. The output will go into a high impedance state if either CE1 is high, CE2 is low, OD is high or R/W is low.

RAMs

A.C. Characteristics for Write Cycle—Separate or Common Data I/O Using Output Disable: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter	S5101L1 Limits		S5101L S5101L3 Limits		S5101L8 S5101-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{WC}	Write Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{AW}	Address To Write Delay	130		150		200		ns	
T_{CW1}	CE1 to Write Delay	350		550		650		ns	
T_{CW2}	CE2 to Write Delay	350		550		650		ns	
T_{DW}	Data Set-Up to End of Write Time	250		400		450		ns	
T_{DH}	Data Hold After End of Write Time	50		100		100		ns	
T_{WP}	Write Pulse Width	250		400		450		ns	
T_{WR}	End of Write to New Address Recovery Time	50		50		100		ns	
T_{DS}	Output Disable to Data-In Set-Up Time	130		150		200		ns	

Write Cycle — For Separate or Common Data I/O

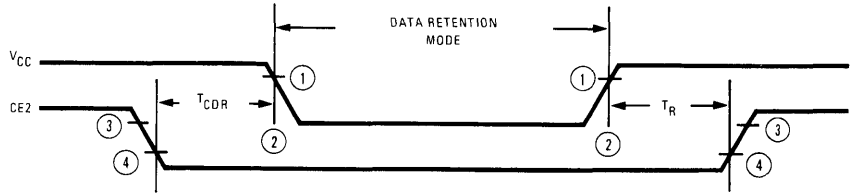


Low V_{CC} Data Retention Characteristics for S5101L, S5101L1, S5101L3 and S5101L8[1]: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	CE2≤0.2V
I_{CCDR}	Data Retention Supply Current	S5101L1, S5101L		10	µA	V_{CC} = V_{DR}
		S5101L3		140	µA	T_R = T_F = 20ns
		S5101L8		500	µA	CE2≤0.2V
T_{CRD}	Chip Deselect to Data Retention Time		0		ns	
T_R	Operation Recovery Time		T_{RC}[2]		ns	

Notes:
[1] For guaranteed low V_{CC} Data Retention @ 2.0V, order must specify S5101L, S5101L1, S5101L3 or S5101L8.
[2] T_{RC} = Read Cycle Time.

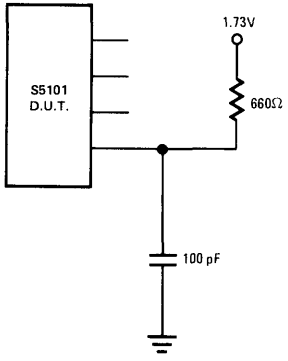
Low V_{CC} Data Retention Wave Form



1. 4.75V
2. V_{DR}
3. V_{IH}
4. 0.2V

477215

A.C. Test Load



1076146

A.C. Conditions of Test

Input Levels	0.65V to 2.2V
Input Rise and Fall Time	20ns
Timing Measurement Reference Level	1.5V

RAMs

S5101 Ordering Information

		0°C to +70°C	−40°C to +85°C	−55°C to −125°C
S5101L1	Plastic	S5101L1P	S5101L1PI	N/A
	Cerdip	S5101L1E	S5101L1EI	N/A
450ns; 10μA Standby	Ceramic	S5101L1C	S5101L1CI	S5101L1CM
S5101L	Plastic	S5101LP	N/A	N/A
	Cerdip	S5101LE	N/A	N/A
650ns; 10μA Standby	Ceramic	S5101LC	N/A	N/A
S5101L3	Plastic	S5101L3P	S5101L3PI	N/A
	Cerdip	S5101L3E	S5101L3EI	N/A
650ns; 140μA Standby	Ceramic	S5101L3C	S5101L3CI	S5101L3CM
S5101L8; S5101-8	Plastic	S5101L8P, S5101-8P	N/A	N/A
	Cerdip	S5101L8E, S5101-8E	N/A	N/A
800ns; 500μA Standby	Ceramic	S5101L8C, S5101-8C	N/A	N/A

N/A = Not Available

NOTE: Also available with MIL STD 883B processing. See Data Sheet for Military 5101L4

AMERICAN MICROSYSTEMS, INC.

S6501

1024 BIT (256 × 4) STATIC CMOS RAM

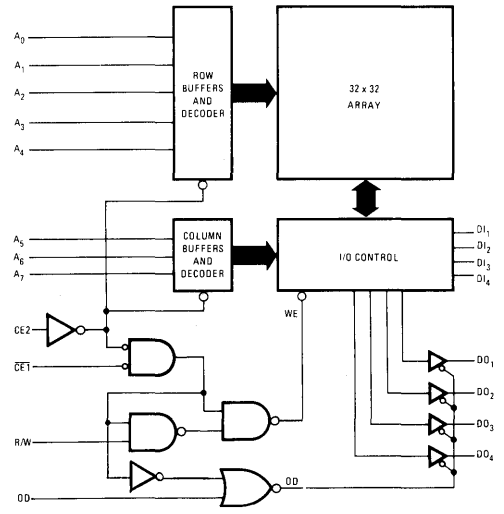
Features

- ☐ **Ultra Low Standby Power**
- ☐ **Data Retention at 2V (L Version)**
- ☐ **Single +5V Power Supply**
- ☐ **Completely Static Operation**
- ☐ **Completely TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**

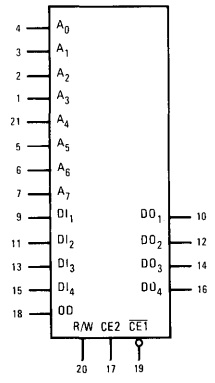
General Description

The AMI S6501 family of 256×4-bit ultra low power CMOS RAMs offers fully static operation with a single +5 volt power supply. All inputs and outputs are directly TTL compatible. With data inputs and outputs on adjacent pins, either separate or common data I/O operations can easily be implemented for maximum design flexibility. The three-state outputs will drive one full TTL load and are disabled (high impedance state) by output disable (OD), or by either chip enable ($\overline{CE1}$ or CE2). This facilitates the control of common data I/O systems.

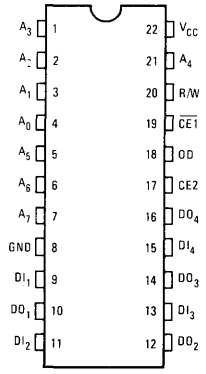
Block Diagram



Logic Symbol



Pin Configuration



Truth Table

$\overline{CE1}$	CE2	OD	R/W	DIN	Output	Mode
H	X	X	X	X	High Z	Not selected
X	L	X	X	X	High Z	Not Selected
X	X	H	L	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	Din	Write
L	H	L	H	X	Dout	Read

Pin Names

A_0-A_7	Address Inputs	$\overline{CE1}$	Chip Enable
DI_1-DI_4	Data Inputs	CE2	Chip Enable
DO_1-DO_4	Data Outputs	R/W	Read/Write Input
OD	Output Disable	V_{CC}	+5 Volt Power Supply

RAMS

General Description (Continued)

The stored data is read out nondestructively and is the same polarity as the original input data. The S6501 is totally static, making clocks unnecessary for a new address to be accepted. The device has two chip enable inputs ($\overline{CE1}$ and CE2) allowing easy system expansion. CE2 disables the entire device but $\overline{CE1}$ does not disable the address buffers and decoders. Thus, minimum power dissipation is achieved when CE2 is low.

The L version of the S6501 has the additional feature of guaranteed data retention with the power supply as low as 2 volts. This makes the device an ideal choice when battery augmented non-volatile RAM storage is mandatory.

The S6501 is fabricated using a silicon gate CMOS process suitable for high volume production of ultra low power, high performance memories.

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} +0.3V
Maximum Power Supply Voltage	8V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A=0°C to +70°C V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
I_{LI}	Input Leakage Current			1	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current			1	µA	$\overline{CE1}$ = V_{IH} V_{OUT} = 0V to V_{CC}
I_{CC}	Operating Supply Current			22	mA	Outputs = Open, V_{IN} = V_{IL} to V_{CC}
I_{CCL}	Standby Supply Current	S6501L1, S6501L		10	µA	V_{IN} = 0V to V_{CC}
		S6501L3		140	µA	except
		S6501L8, S6501-8		500	µA	CE2 ⩽ 0.2V
V_{IL}	Input Low Voltage		-0.3	0.65	V	
V_{IH}	Input High Voltage		2.2	V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage		2.4		V	I_{OH} = -1 mA

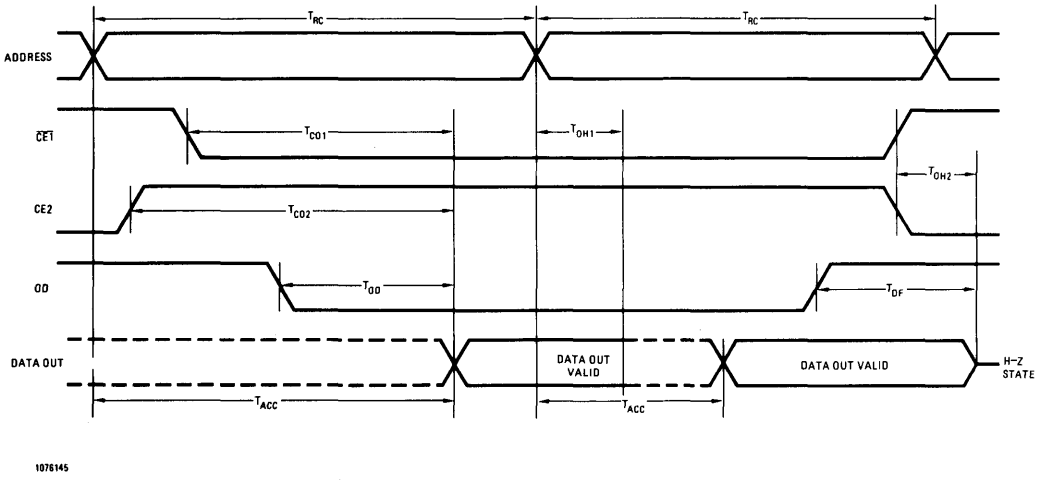
Capacitance

Symbol	Parameter	Limits Min.	Limits Max.	Units	Conditions
C_{IN}	Input Capacitance		8	pF	V_{IN} = 0V, on all Input Pins
C_O	Output Capacitance		12	pF	V_O = 0V

A.C. Characteristics for Read Cycle: $T_A=0°C$ to $+70°C$ $V_{CC}=5V\pm5\%$ (unless otherwise specified)

Symbol	Parameter	S6501L1 Limits		S6501L S6501L3 Limits		S6501L8 S6501-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{RC}	Read Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{ACC}	Access Time		450		650		800	ns	
T_{CO1}	$\overline{CE1}$ to Output Delay		400		600		800	ns	
T_{CO2}	CE2 to Output Delay		500		700		850	ns	
T_{OD}	Output Disable to Enabled Output Delay		250		350		450	ns	
T_{DF}	Output Disable to Output H-Z State Delay	0	130	0	150	0	200	ns	
T_{OH1}	Output Data Valid Into Next Cycle with respect to Address	0		0		0		ns	
T_{OH2}	Output Data Valid Into Next Cycle with respect to Chip Enable	0		0		0		ns	

Read Cycle



Note:
1. OD may be tied low for separate I/O information.
2. The output will go into a high impedance state if either CE1 is high, CE2 is low or OD is high.

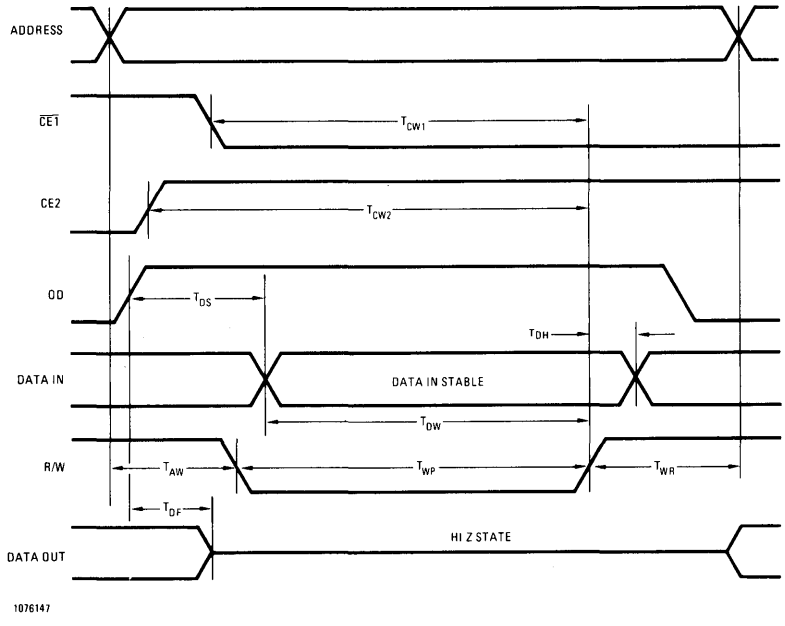
RAMs

A.C. Characteristics for Write Cycle—Separate or Common Data I/O Using Output Disable:

T_A=0°C to +70°C V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter	S6501L1 Limits		S6501L S6501L3 Limits		S6501L8 S6501-8 Limits		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
T_{WC}	Write Cycle Time	450		650		800		ns	See A.C. Conditions of Test and A.C. Test Load
T_{AW}	Address To Write Delay	130		150		200		ns	
T_{CW1}	CE1 to Write Delay	350		550		650		ns	
T_{CW2}	CE2 to Write Delay	350		550		650		ns	
T_{DW}	Data Set-Up to End of Write Time	250		400		450		ns	
T_{DH}	Data Hold After End of Write Time	50		100		100		ns	
T_{WP}	Write Pulse Width	250		400		450		ns	
T_{WR}	End of Write to New Address Recovery Time	50		50		100		ns	
T_{DS}	Output Disable to Data-In Set-Up Time	130		150		200		ns	

Write Cycle — For Separate or Common Data I/O



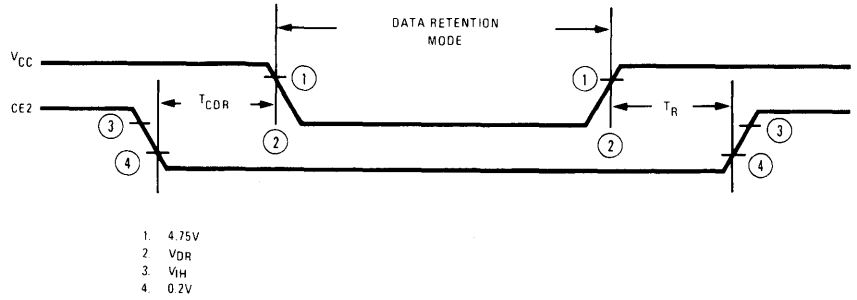
Low V_{CC} Data Retention Characteristics for S6501L, S6501L1, S6501L3 and S6501L8

$T_A = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$ (unless otherwise specified)

Symbol	Parameter		Limits Min.	Limits Max.	Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	CE2 ≤ 0.2V
I_{CCDR}	Data Retention Supply Current	S6501L1, S6501L		10	μA	$V_{CC} = V_{DR}$
		S6501L3		140	μA	$T_R = T_F = 20ns$
		S6501L8		500	μA	CE2 ≤ 0.2V
T_{CRD}	Chip Deselect to Data Retention Time		0		ns	
T_R	Operation Recovery Time		T_{RC}[1]		ns	

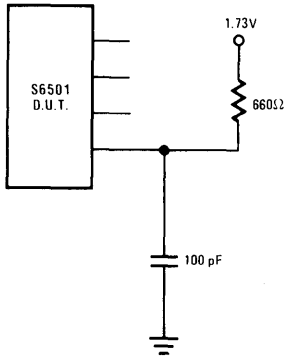
Notes:
[1] T_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Wave Form



477215

A.C. Test Load



1076146

A.C. Conditions of Test

Input Levels	0.65V to 2.2V
Input Rise and Fall Time	20ns
Timing Measurement Reference Level	1.5V

RAMs

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S6504

4096 BIT (4096×1) STATIC CMOS RAM

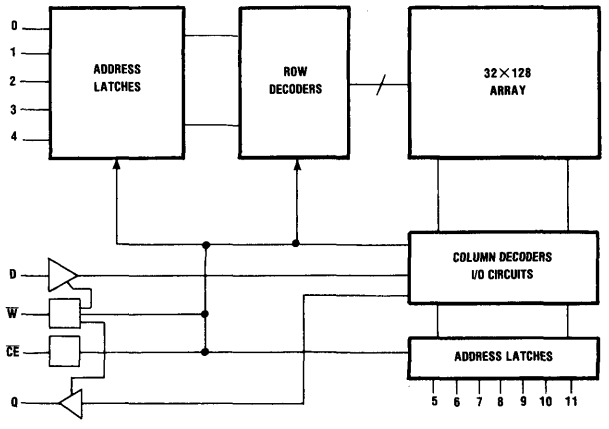
Features

- ☐ Low Standby Power—10μW Typ.
- ☐ Low Operating Power—20mW Typ.
- ☐ Low Voltage Data Retention —2.0V
- ☐ High Density Standard 18 Pin Package
- ☐ Fast Access Time 300ns
- ☐ On Chip Address Latches
- ☐ SiGate CMOS Technology

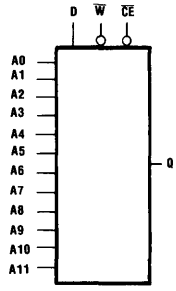
General Description

The AMI S6504 is a 4096×1 bit low power CMOS RAM offering static operation with a single +5V power supply. All inputs and outputs are fully TTL compatible. The addresses are buffered by on-chip address latches. These internal registers are latched by the HIGH to LOW transition of the $\overline{CE}$. The write enable and chip enable functions are designed such that either separate or common data 110 operations can be easily implemented for maximum design flexibility.

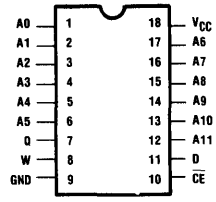
Block Diagram



Logic Symbol



Pin Configuration



Truth Table

Mode	$\overline{W}$	$\overline{CE}$	Data In	Data Out
Read	H	L	X	Data In
Write	L	L	X	Hi-Z
Not Selected	X	H	X	Hi-Z

Pin Names

A0—A11 ..... Address Inputs
Q ..... Output
D ..... Data In
$\overline{CE}$ ..... Chip Enable (Active LOW)
$\overline{W}$ ..... Write Enable (Active LOW)
V_{CC} ..... +5V Power Supply

AMERICAN MICROSYSTEMS, INC.

S6508/S6508A

1024 BIT (1024×1) STATIC CMOS RAM

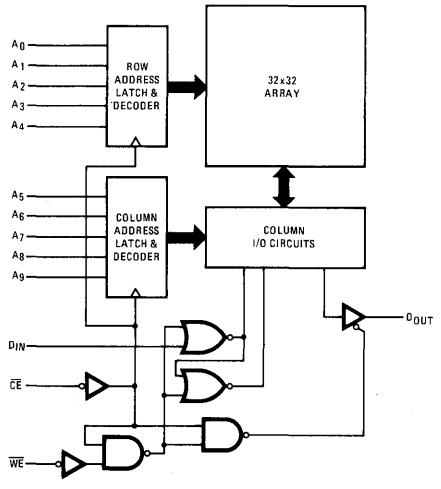
Features

- ☐ **Ultra Low Standby Power**
- ☐ **S6508 Completely TTL Compatible**
- ☐ **S6508A Completely CMOS Compatible**
- ☐ **4V to 11V Operation (S6508)**
- ☐ **Data Retention at 2V**
- ☐ **Three-State Output**
- ☐ **Low Operating Power: 10mW @1MHz (5V)**
- ☐ **Fast Access Time: 185ns @10V**
- ☐ **Available in Commercial, Industrial and Military Temperature Ranges**

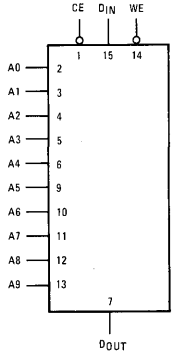
General Description

The AMI S6508 family of 1024×1 bit static CMOS RAMs offers ultra low power dissipation with a single power supply. The device is available in two versions. The basic part (S6508) operates on 5V and is directly TTL compatible on all inputs and the three-state output. The S6508 "A" operates from 4V to 11V and is fully CMOS compatible. The data is stored in ultra low power CMOS static RAM cells (six transistor). The stored data is read out nondestructively and is the same polarity as the original input data. The address is buffered by on-chip address registers. These internal registers are latched by the HIGH to LOW transition of chip enable ($\overline{CE}$). The write enable and chip enable functions are designed such that either separate or common data I/O operations can be easily implemented for maximum design flexibility.

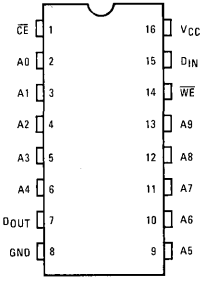
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0—A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply

RAMs

General Description (Continued)

The S6508 is fabricated using a silicon gate CMOS process suitable for high volume production of high performance, ultra low power memories. When deselected ($\overline{CE}$ = HIGH), the S6508-1 draws less than 10 microamps from the 5V supply. In addition, it offers guaranteed data retention with the power supply as low as 2 volts. This process makes the device an ideal choice where battery augmented nonvolatile RAM storage is mandatory.

CMOS to TTL—S6508/S6508-1
Absolute Maximum Ratings

Supply Voltage	8.0V
Input or Output Voltage Supplied	GND−0.5V to V_{CC}+0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range —T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
(Military temp part)	−55°C to +125°C

D.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0		V	
V_{IL}	Logical "0" Input Voltage			0.8	V	
I_{IL}	Input Leakage		−1.0	1.0	μA	0V V_{IN} V_{CC}
V_{OH2}	Logical "1" Output Voltage		V_{CC}−0.01		V	I_{OUT}=0
V_{OH1}	Logical "1" Output Voltage		2.4		V	I_{OH}=−0.2mA
V_{OL2}	Logical "0" Output Voltage			GND+0.01	V	I_{OUT}=0
V_{OL1}	Logical "0" Output Voltage			0.45	V	I_{OL}=2.0mA
I_O	Output Leakage		−1.0	1.0	μA	0V V_O V_{CC}, $\overline{CE}$=V_{IH}
I_{CCL}	Standby Supply Current	S6508		100	μA	V_{IN}=V_{CC}, $\overline{CE}$=V_{IH}
		S6508-1		10	μA	
I_{CC}	Supply Current S6508/S6508-1			2.0	mA	f=1MHz
C_{IN}	Input Capacitance			7.0	pF	
C_O	Output Capacitance			10.0	pF	

A.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

Symbol	Parameter	S6508-1		S6508		Units	Conditions
		Min.	Max.	Min.	Max.		
t_{ACC}	Access Time from $\overline{CE}$		300		460	ns	See A.C. conditions of test and A.C. test load
t_{EN}	Output Enable Time		180		285	ns	
t_{DIS}	Output Disable Time		180		285	ns	
t_{CEH}	$\overline{CE}$ HIGH	200		300		ns	
t_{CEL}	$\overline{CE}$ LOW	300		460		ns	
t_{WP}	Write Pulse Width (LOW)	200		300		ns	
t_{AS}	Address Setup Time	7		15		ns	
t_{AH}	Address Hold Time	90		130		ns	
t_{DS}	Data Setup Time	200		300		ns	
t_{DH}	Data Hold Time	20		20		ns	
t_{MOD}	Data Modify Time	0		0		ns	

CMOS to CMOS—S6508A
Absolute Maximum Ratings

Supply Voltage 12.0V
Input or Output Voltage Supplied ..... $-0.5V$ to $V_{CC}+0.5V$
Storage Temperature Range ..... $-65°C$ to $+150°C$
Operating Temperature Range —T_A (Standard Part) ..... $0°C$ to $+70°C$
(Industrial temp part) ..... $-40°C$ to $+85°C$
(Military temp part) ..... $-55°C$ to $+125°C$

D.C. Characteristics: $T_A=0°C$ to $+70°C$ (Standard part); $-40°C$ to $+85°C$ (Industrial temp part); $-55°C$ to $+125°C$ (Military temp part), $V_{CC}=5V\pm5\%$ (unless otherwise specified)

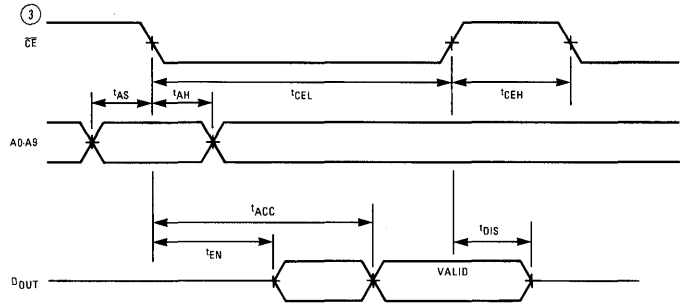
Symbol	Parameter	Min.	Max.	Units	Conditions
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	0V V_{IN} V_{CC}
V_{OH}	Logical "1" Output Voltage	$V_{CC}-0.01$		V	$I_{OUT}=0$
V_{OL}	Logical "0" Output Voltage		GND+0.01	V	$I_{OUT}=0$
I_O	Output Leakage	-1.0	1.0	μA	0V V_O V_{CC}, $\overline{CE}=V_{IH}$
I_{CCL}	Standby Supply Current		500	μA	$V_{IN}=V_{CC}$, $\overline{CE}=V_{IH}$
I_{CC}	Supply Current $V_{CC}=5V$		2.0	mA	f=1MHz
	Supply Current $V_{CC}=10V$		4.3	mA	f=1MHz
C_{IN}	Input Capacitance		7.0	pF	
C_O	Output Capacitance		10.0	pF	

A.C. Characteristics: $T_A=0°C$ to $+70°C$ (Standard part); $-40°C$ to $+85°C$ (Industrial temp part); $-55°C$ to $+125°C$ (Military temp part), $V_{CC}=5V\pm10\%$ (unless otherwise specified)

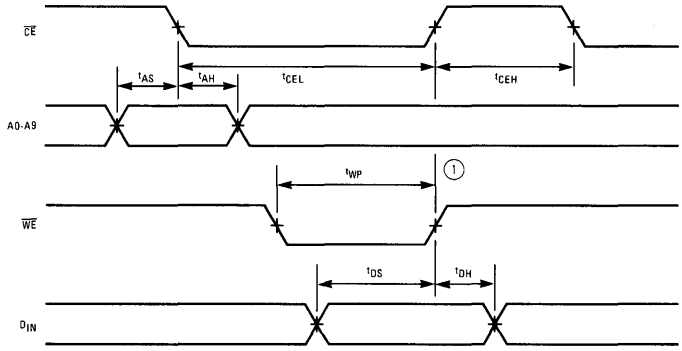
Symbol	Parameter	V_{CC}	Min.	Max.	Units	Conditions
t_{ACC}	Access Time from $\overline{CE}$	5V		460	ns	See A.C. conditions of test and A.C. test load
		10V		185	ns	
t_{EN}	Output Enable Time	5V		285	ns	
		10V		120	ns	
t_{DIS}	Output Disable Time	5V		285	ns	
		10V		120	ns	
t_{CEH}	$\overline{CE}$ HIGH	5V	300		ns	
		10V	125		ns	
t_{CEL}	$\overline{CE}$ LOW	5V	460		ns	
		10V	185		ns	
t_{WP}	Write Pulse Width (LOW)	5V	300		ns	
		10V	125		ns	
t_{AS}	Address Setup Time	5V	15		ns	
		10V	15		ns	
t_{AH}	Address Hold Time	5V	130		ns	
		10V	60		ns	
t_{DS}	Data Setup Time	5V	300		ns	
		10V	125		ns	
t_{DH}	Data Hold Time	5V	20		ns	
		10V	125		ns	
t_{MOD}	Data Modify Time	5V	0		ns	
		10V	0		ns	

RAMS

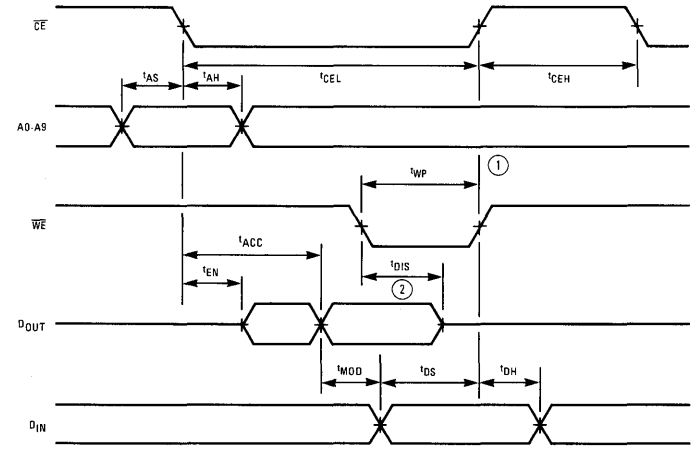
Read Cycle



Write Cycle



Read Modify Write Cycle



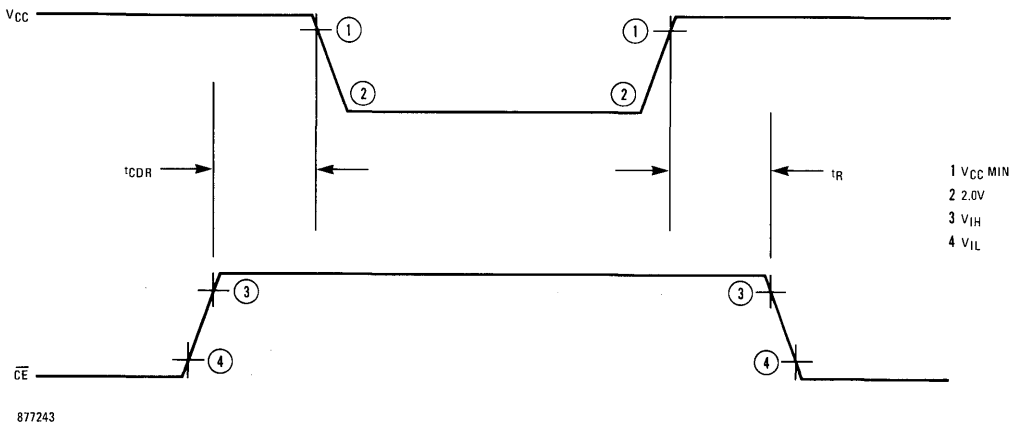
NOTES:

1. The write operation is terminated on any positive edge of Chip Enable ($\overline{CE}$) or Write Enable ($\overline{WE}$).
2. The data output will be in the high impedance state whenever $\overline{WE}$ is LOW.
3. $\overline{WE}$ is HIGH during a read operation.
4. Rise and fall times of V_{CC} equal 20ns.

D.C. Characteristics: T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part); −55°C to +125°C (Military temp part), V_{CC}=5V±5% (unless otherwise specified)

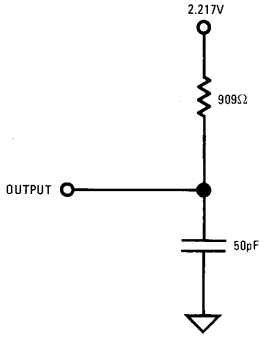
Symbol	Parameter		Min.	Max.	Units	Conditions
V_{DR}	V_{CC} for Data Retention		2.0		V	$\overline{CE}$ = 2.0V
I_{CCDR}	Data Retention	S6508,S6508A		10	μA	$V_{CC}=V_{DR}$ Min.
	Supply Current	S6508-1		1.0	μA	$t_r=t_f=20ns$
t_{CDR}	Deselect Setup Time		t_{CEH}		ns	
t_r	Recovery Time		t_{CEH}		ns	

Low V_{CC} Data Retention Waveform



877243

A.C.Test Load



877244

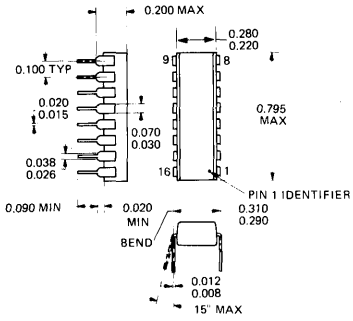
A.C. Test Conditions

Input Levels ..... V_{IL} to V_{IH}
Input Rise & Fall 20ns
Timing Measurement Reference Level
S6508/S6508-1 ..... 1.5V
S6508A ..... 50% V_{CC}

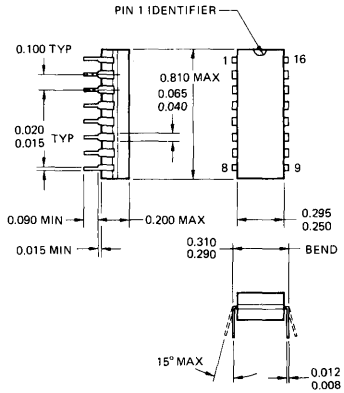
RAMs

Package Outlines

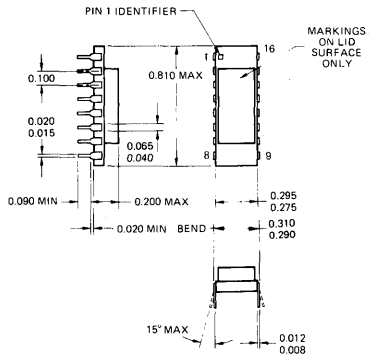
16-Pin Plastic



16-Pin Cer-DIP



16-Pin Ceramic



Ordering Information

Device	Access Time	Low V_{CC} Stby I_{CC}	Package	Order Number		
				0°C to +70°C	−40°C to +85°C	−55°C to +25°C
S6508	460	10μA	Plastic	S6508P	S6508PI	N/A
			Cerdip	S6508E	S6508EI	N/A
			Ceramic	S6508C	S6508CI	S6508CM
S6508-1	300	1μA	Plastic	S65081P	S65081PI	N/A
			Cerdip	S65081E	S65081EI	N/A
			Ceramic	S65081C	S65081CI	S65081CM
S6508A	185 @10V	10μA	Plastic	S6508AP	S6508API	N/A
			Cerdip	S6508AE	S6508AEI	N/A
			Ceramic	S6508AC	S6508ACI	S6508ACM

N/A = Not Available

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S6514

4096 BIT (1024 × 4) STATIC CMOS RAM

Features

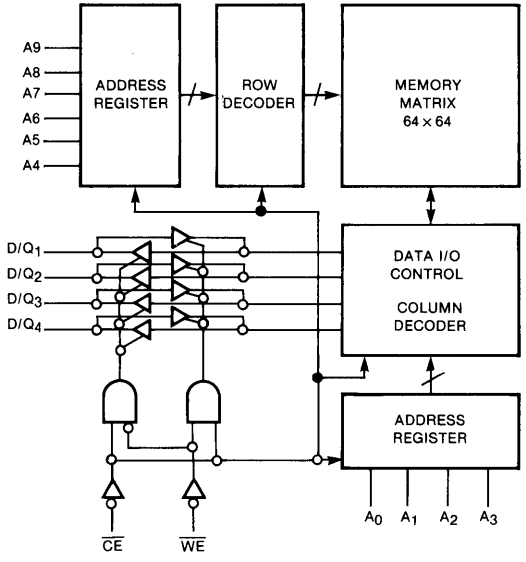
- ☐ **Low Power Standby—1mW MAX**
- ☐ **TTL Compatible Inputs/Outputs**
- ☐ **Three-State Outputs**
- ☐ **On-Chip Address Registers**
- ☐ **Data Retention @ 2V**
- ☐ **Standard 18 pin Package/Pinouts**

General Description

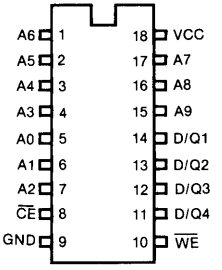
The AMI S6514 is a 1024x4 static CMOS RAM offering low power and static operation with a single +5 volt power supply. All inputs and outputs are TTL compatible. The common Data I/O pins allow direct interface with common bus systems.

Battery-backup design is simplified by use of $\overline{CE}$, which when HIGH, allows the other inputs to float.

Block Diagram



Pin Connections



Pin Names

A0-A9	Address Inputs
D/Q_1-D/Q_4	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable

Truth Table

Mode	$\overline{E}$	$\overline{W}$	Data Out
Read	L	H	Data In
Write	L	L	HI-Z
Disable	H	X	HI-Z

RAMs

Absolute Maximum Ratings

Supply Voltage $-V_{CC}$	$-0.3V$ to $+7.0V$
Input/Output Voltage Applied	$-0.3V$ to $V_{CC}+0.3V$
Storage Temperature $-T_{stg}$	$-65°C$ to $+150°C$

DC Electrical Characteristics: $T_A=0°C$ to $70°C$, $V_{CC}=+5V\pm10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current	-1		1	μA	$V_{IN}=GND$ to V_{CC}
I_{LO}	Output Leakage Current			1	μA	$V_{IN}=GND$ to V_{CC}
I_{SB}	Standby Supply Current			50	μA	$V_{IN}=GND$ or V_{CC}
I_{CC}	Operating Supply Current			7	mA	$V_{IN}=GND$ or V_{CC}, f=MHz
V_{IL}	Input Voltage LOW	-0.3		0.8	V	
V_{IH}	Input Voltage HIGH	2.4		$V_{CC}+0.3$	V	
V_{OL}	Output Voltage LOW			0.4	V	$I_{OL}=1.6mA$
V_{OH}	Output Voltage HIGH	2.4			V	$I_{OH}=-0.4mA$

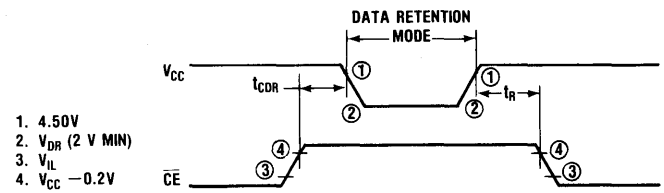
Capacitance: $T_A=25°C$, t=1MHz. Capacitance is sampled and guaranteed.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	GND to V_{CC}
C_{OUT}	Output Capacitance			10	pF	GND to V_{CC}

Low V_{CC} Data Retention Characteristics:

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CCDR}	I_{CC} for Data Retention			25	μA	$V_{IN}=GND$ to V_{CC}; $V_{CC}=3V$
V_{CCDR}	V_{CC} for Data Retention	2.0			V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	TELEL				

Low V_{CC} Data Retention Wave Form



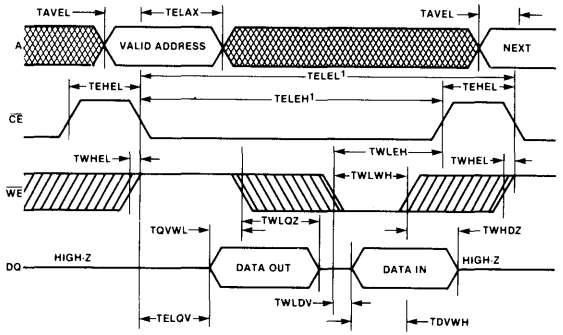
AC Test Conditions

t rise/t fall	20ns
Output Load	1 TTL Load & 50pF
All	Timing 1.5V

AC Electrical Characteristics: $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
TELQV	Chip Enable Access Time			300	ns	
TAVQV	Address Access Time			320	ns	
TWLQZ	Write Enable Output Disable Time			100	ns	
TEHQZ	Chip Enable Output Disable Time			100	ns	
TELEH	Chip Enable Pulse Negative Width	300			ns	
TEHEL	Chip Enable Pulse Positive Width	120			ns	
TAVEL	Address Setup Time	20			ns	
TELAX	Address Hold Time	50			ns	
TWLWH	Write Enable Pulse Width	300			ns	
TWLEH	Write Enable Pulse Setup Time	300			ns	
TELWH	Write Enable Pulse Hold Time	300			ns	
TDVWH	Data Setup Time	200			ns	
TWHDZ	Data Hold Time	0			ns	
TWHEL	Write Enable Read Setup Time	0			ns	
TQVWL	Output Data Valid to Write Time	0			ns	
TWLDV	Write Data Delay Time	100			ns	
TELWL	Early Output High-Z Time			0	ns	
TWHEH	Late Output High-Z Time			0	ns	
TELEL	Read or Write Cycle Time	420			ns	

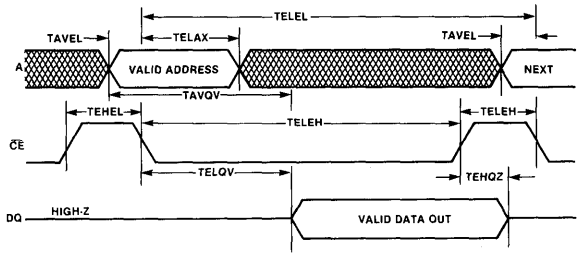
Read Modify Write Cycle



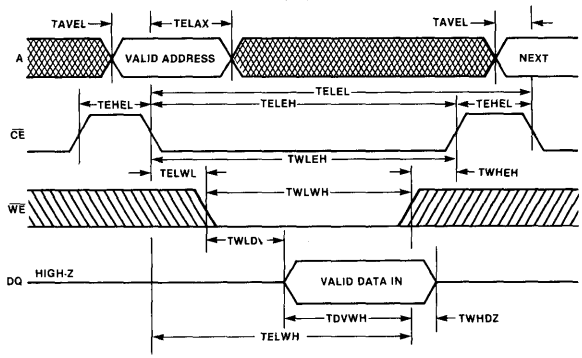
Note 1: TELEL & TELEH are longer than the minimum given for Read or Write cycle.

RAMs

Read Cycle: $\overline{WE}$ = HIGH

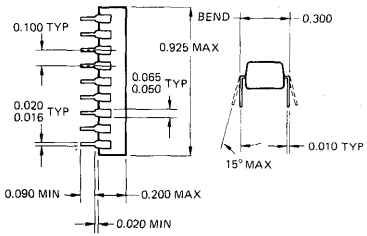


Write Cycle

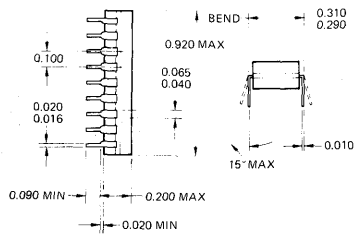


Package Outlines

18-Pin Plastic

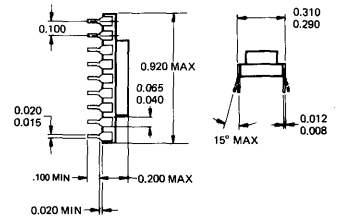


18-Pin Cer-DIP



2P

18-Pin Ceramic



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S6516

16,384 BIT (2048x8) STATIC CMOS RAM

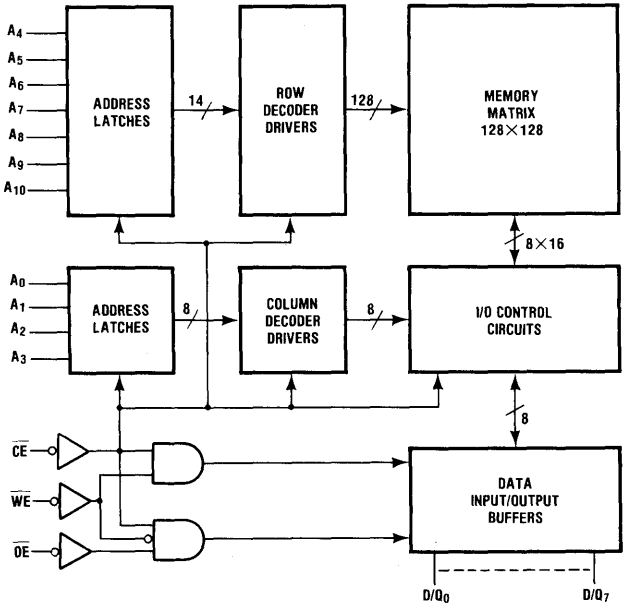
Features

- ☐ High Speed—150ns Maximum
- ☐ Low Power Standby—1mW Maximum
- ☐ Low Power Operation—55mW/MHz Maximum
- ☐ On-Chip Address Registers
- ☐ Fully TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Low Voltage Data Retention —2V
- ☐ Standard 24 Pin Package
- ☐ EPROM and ROM Compatible Pinouts

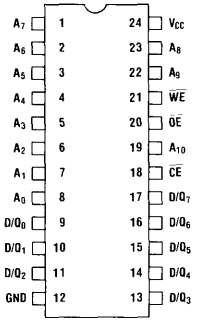
General Description

The AMI S6516 is a 16,384 bit static CMOS RAM organized as 2048 words by 8 bits. It offers low standby and operating power dissipation from a single +5V power supply. All inputs and outputs are TTL compatible. The common data I/O pins allow direct interface with common bus systems. The output enable function facilitates memory expansion by allowing the outputs to be OR-tied to other devices. The device operates synchronously with address registers provided on-chip. The data is latched into the registers during the high to low transition of the chip enable pulse.

Block Diagram



Pin Configuration



Pin Names

A_0-A_{10}	Address Inputs
$D/Q_0-D/Q_7$	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable

Truth Table

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Outputs
Read	L	H	L	Data Out
Write	L	L	H	High-Z
Chip Disable	H	X	X	High-Z
Output Disable	L	X	H	High-Z

RAMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage	−0.3V to 7V
Voltage on Any Pin with Respect to Ground	−0.3V to V_{CC} +0.3V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A = −40°C to +85°C, V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{LI}	Input Leakage Current	−1		1	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			1	μA	V_{IN} = GND to V_{CC}
I_{SB}	Standby Supply Current			50	μA	V_{IN} = GND or V_{CC}
I_{CC}	Operating Supply Current				mA	V_{IN} = GND or V_{CC}, f = MHz
V_{IL}	Input Voltage LOW	−0.3		0.8	V	
V_{IH}	Input Voltage HIGH	2.4		V_{CC} +0.3	V	
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6mA
V_{OH}	Output Voltage HIGH	2.4			V	I_{OH} = −0.4mA

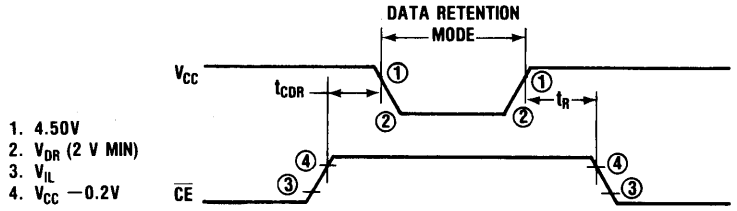
Capacitance: T_A = 25°C, t = 1MHz. Capacitance is sampled and guaranteed.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	GND to V_{CC}
C_{OUT}	Output Capacitance			10	pF	GND to V_{CC}

Low V_{CC} Data Retention Characteristics:

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{CCDR}	I_{CC} for Data Retention			25	μA	V_{IN} = GND to V_{CC}; V_{CC} = 3V
V_{CCDR}	V_{CC} for Data Retention	2.0			V	
t_{CDR}	Chip Deselect to Data Retention Time	0			ns	
t_R	Operation Recovery Time	TELEL				

Low V_{CC} Data Retention Wave Form



A.C. Test Conditions

Input Pulse Levels	0.8V and 2.2V
Input Rise and Fall Times	⩽20ns
Input Timing Level	0.8V and 2.2V
Output Timing Levels	0.6V and 2.2V
Output Load	1 TTL Load and 100pF

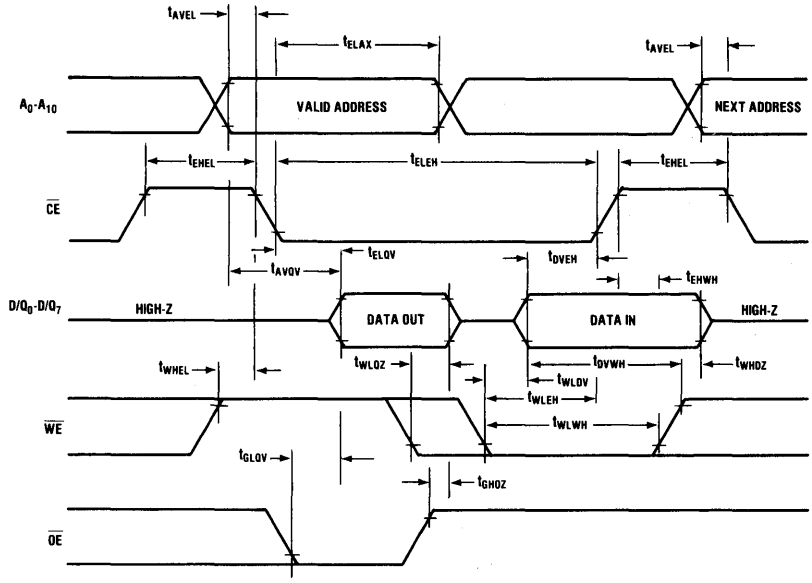
A.C. Electrical Characteristics: $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{ELQV}	Chip Enable Access Time			150	ns	
t_{AVQV}	Address Access Time			150	ns	
t_{WLQZ}	Write Enable Output Disable Time			50	ns	
t_{EHQZ}	Chip Enable Output Disable Time			50	ns	
t_{ELEH}	Chip Enable Pulse Negative Width	150			ns	
t_{EHEL}	Chip Enable Pulse Positive Width	60			ns	
t_{AVEL}	Address Setup Time	0			ns	
t_{ELAX}	Address Hold Time	25			ns	
t_{WLWH}	Write Enable Pulse Width	140			ns	
t_{WLEH}	Write Enable Pulse Setup Time	140			ns	
t_{ELWH}	Write Enable Pulse Hold Time	140			ns	
t_{DVWH}	Data Setup Time	90			ns	
t_{WHDZ}	Data Hold Time	−10			ns	
t_{WHEL}	Write Enable Read Setup Time	0			ns	
t_{QVWL}	Output Data Valid to Write Time	−10			ns	
t_{WLDV}	Write Data Delay Time	40			ns	
t_{ELWL}	Early Output High-Z Time	−10			ns	
t_{WHEH}	Late Output High-Z Time	10			ns	
t_{ELEL}	Read or Write Cycle time	230			ns	

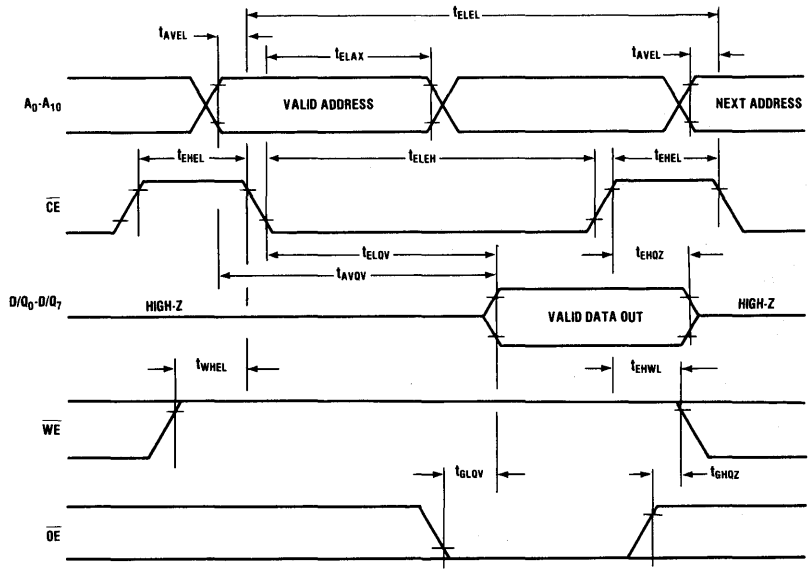
t_{EHWL}, Write Enable Read Hold Time ..... 0ns MIN. t_{GLQV}, Output Enable to Output Valid ..... 10ns MIN.
t_{DVEH}, Data Setup Time to Chip Enable ..... 140ns MIN. t_{GHQZ}, Output Enable to Output High-Z ..... 50ns MIN

RAMs

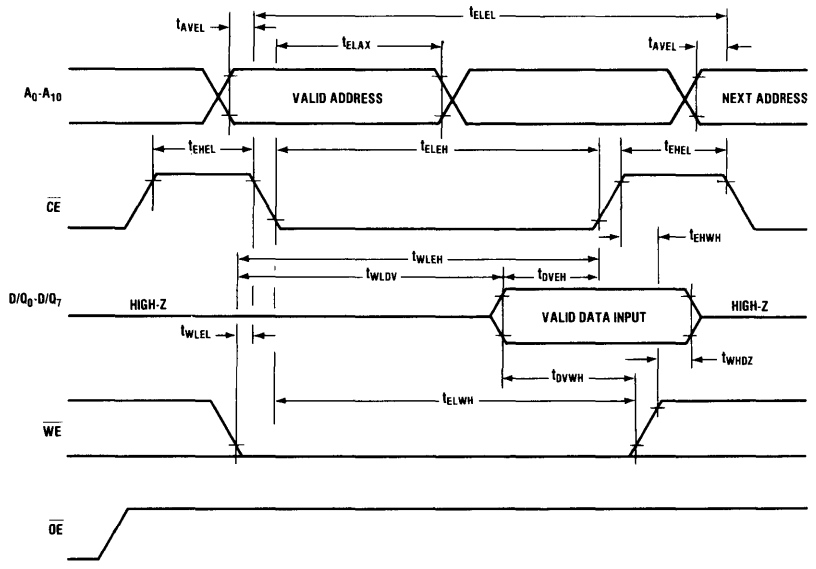
Read Modify Write Cycle



Read Cycle



Write Cycle


t_{ELEL}
t_{AVEL}
t_{ELAX}
t_{AVEL}
A_0-A_{10}
VALID ADDRESS
NEXT ADDRESS
t_{EHEL}
t_{ELEH}
t_{EHEL}
$\overline{CE}$
t_{EHWH}
t_{WLEH}
t_{WLDV}
t_{DVEH}
D/O_0-D/Q_7
HIGH-Z
VALID DATA INPUT
HIGH-Z
t_{WLEL}
t_{WHDZ}
t_{DVWH}
t_{ELWH}
$\overline{WE}$
$\overline{OE}$

Ordering Information

The following information should be included in the purchase order when ROM devices are being ordered.

- ☐ Part number
- ☐ Number of ROM patterns
- ☐ Quantity of prototypes for each pattern (if none, so state)
- ☐ Total quantity of each pattern
- ☐ Special marking (if required)
- ☐ *Method of ROM code entry (EPROM, punched paper tape, etc.)
- ☐ *Chip select definition —
- ☐ Pricing and delivery (pricing and delivery quotes can be obtained from any AMI Sales Office)

*If ordering a previously supplied pattern, the order should refer to the AMI C number (CXXXXX). This C number can be obtained from previous AMI billing or acknowledgement.

UNIT QUANTITY VARIANCE

AMI manufactures ROMS in a fully proven silicon gate N-channel process. However, as in any semi-conductor production, yield variations do occur. Because of these normal yield variations a policy has been established that requires the customer to accept a small variation from the nominal quantity ordered.

Unit Quantity Variance ±5% or 50 units (whichever is greater)

PART NUMBER

An AMI ROM part number consists of a device number followed by a single letter designating the package type.
P — designates plastic package
C — designates ceramic package (hermetic seal)

Device Numbers

S68308	1K×8	
S6831B/S68A316	2K×8	
S68A332/S68332	4K×8	Standard Pinout
S2333	4K×8	(Pin compatible with 2732 EPROM)
S68A364	8K×8	(24 Pin)
S2364	8K×8	(28 Pin-Compatible W/2764 EPROM)
*S23128	16K×8	(28 Pin)

*To Be Announced

ROM Sales Policy

MINIMUM ORDER QUANTITY

Capacity	Part No.	Architecture	Units/Pattern
8K	S68308	1K×8	1,000
16K	S6831B, S68A316	2K×8	1,000
32K	S68332, S68A332	4K×8	500
32K	S2333 (Alternate Pinout)	4K×8	500
64K	S68A364 (24-Pin)	8K×8	250
64K	S2364 (28-Pin)	8K×8	250
*128K	S23128 (28-Pin)	16K×8	100

*To Be Announced

Unless otherwise requested by the customer, approximately 5 units will be assembled in a ceramic package for verification of the ROM pattern by the customer. These 5 units will be considered as part of the total quantity ordered.

Mask Charges*

Most ROM suppliers charge a mask charge to cover the expense of generating tooling that is unique to each ROM pattern. Current AMI mask charges are as follows.

		Min. Qty/Mask Charges		
Part No.	Architecture	250 Pcs.	500 Pcs.	1000 Pcs.
S6831B, S68A316	2K×8	N/A	N/A	$ 500
S68332, S68A332, S2333	4K×8	N/A	$1000	$ 750
S68A364, S2364	8K×8	$2500	$2000	$1500

*Subject to Change

Reorder Policy

If a customer wishes to reorder the same ROM pattern, the following policy applies. If finished inventory exists, no minimum quantity limits will be imposed. However, if new wafer starts are required, the same minimum quantity as for a new pattern will apply. The 5 prototypes (supplied with new patterns) will not be supplied. No mask charge is applied to a reorder of a previously supplied ROM pattern.

DELIVERY

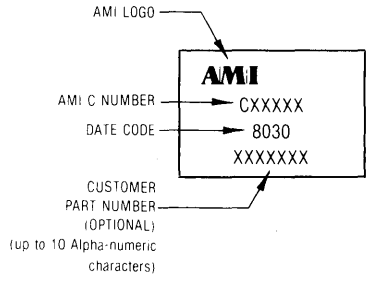
Exact delivery dates must be quoted by AMI Customer Service when the order is placed. The following general guidelines apply.

Prototypes	(5 Units)	5 wks.	(After Pattern Verification)
First Production	(250/500 Units)	7 wks.	(Or 4 wks. after prototype approval)
Quantity Production	(Any Quantity)	9-11 wks.	

ROM PACKAGE MARKING

Unless otherwise specified, AMI ROMs are marked with a C number (the letter C followed by a 5 digit number) and a date code. This C number identifies both the device type and the specific pattern. This C number will be used on all AMI documents concerning the ROM.

A ROM can also be marked with a number supplied by the customer. A single number of up to 10 alpha numeric characters can be marked on the device without extra charge. Other customer markings are possible, but must be approved before the order is entered.



ROM CODE DATA

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to diskette and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested, AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM requirements

The following EPROMs should be used for submitting ROM Code Data:

ROM		EPROM	
		PREFERRED	OPTIONAL
S68308	1KX8	2708	—
S6831B	2KX8	2716/2516	2-2708
S68332	4KX8	2532	2-2716/2516
S2333	4KX8	2732	2-2716/2516
S68A364	8KX8	68764	2-2532
S2364	8KX8	2764	2-2732

If two EPROM's are used to specify one ROM pattern, (i.e., 2 16K EPROMs for one 32K ROM) two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Example: Two 2716 EPROMs for S68332 ROM
Marking: EPROM # 1 000-7FF
EPROM # 2 800-FFF

PATTERN DATA FROM ROMs

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitor's ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

OPTIONAL METHOD OF SUPPLYING ROM CODE DATA

If an EPROM or ROM cannot be supplied, the following other methods are acceptable.

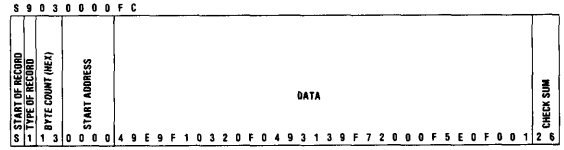
- 9 Track NRZ Magnetic Tape (2 each) odd parity, 800 BPI
- Paper Tape (AMI Hex format)
- Card Deck (AMI Hex format)

The AMI Hex format is described below. With its built-in address space mapping and error checking, this format is produced by the AMI Assembler.

Position	Description
1	Start of record (Letter S)
2	Type of record 0—Header record (comments) 1—Data record 9—End of file record
3, 4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9,..., N	Data Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S113000049E9F10320F04939F72000F5E0F00126
S9030000FC
```



Paper tape format is the same as the card format above except:

a. The record should be a maximum of 80 characters.
b. Carriage return and line feed after each record followed by another record.
c. There should NOT be any extra line feed between records at all.
d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S68A316/S68B316

16,384 BIT (2048x8) STATIC NMOS ROM

Features

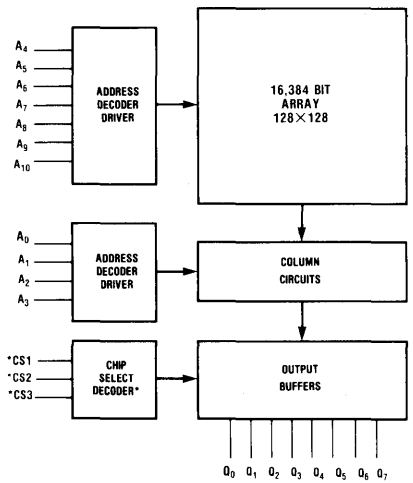
- ☐ **Fast Address Access Time:**
  S68A316 - 350ns Max.
  S68B316 - 250ns Max.
- ☐ **EPROM Pin Compatible**
- ☐ **Fully Static Operation**
- ☐ **Three Programmable Chip Selects**
- ☐ **TTL Compatible Inputs**
- ☐ **Three-State TTL Compatible Outputs**
- ☐ **Late Mask Programmable**

General Description

The AMI S68316 family of 16,384 bit mask programmable Read-Only-Memories organized as 2048 words by 8 bits offers fully static operation with a single +5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three chip selects are mask programmable, the active level is specified by the user. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

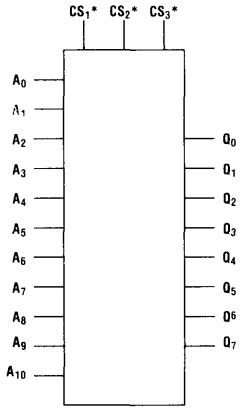
The devices are fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

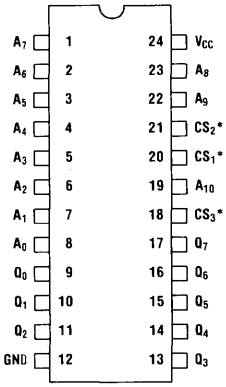


*USER DEFINED CHIP SELECTS
MAY BE DEFINED AS ACTIVE HIGH (CS) OR ACTIVE LOW (CS) OR NO CONNECTION (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{10}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_3$	Chip Select Inputs
V_{CC}	+5V Power Supply

ROMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to 80°C
Storage Temperature	65°C to 150°C
Output or Supply Voltage	0.5V to 7V
Input Voltage	0.5V to 5.5V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: $V_{CC} = +5V \pm 5\%$; $T_A = 0°C$ to $70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 3.2mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -220\mu A$
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to V_{CC}
I_{LO}	Output Leakage Current			10	μA	$V_{OUT} = 0.4V$ to V_{CC} Chip Deselected
I_{CC}	Power Supply Current S68A316			80	mA	
	S68B316			50		

Capacitance: $f = 1.0MHz$; $T_A = 25°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7.5	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $V_{CC} = +5V \pm 5\%$; $T_A = 0°C$ to $+70°C$

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A316			350	ns	See A.C. Test Conditions and Waveforms
		S68B316			250	ns	
t_{ACS}	Chip Select Access Time	S68A316			120	ns	
		S68B316			75	ns	
t_{OFF}	Chip Deselect Time	S68A316			120	ns	
		S68B316			60	ns	

NOTES:

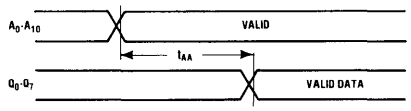
1. Only positive logic formats for $CS_1 - CS_3$ are accepted. $1 = V_{HIGH}$; $0 = V_{LOW}$
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.

A.C. Test Conditions

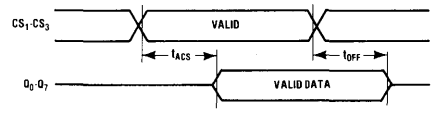
Input Pulse Levels	0.8V to 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms

Propagation From Addresses



Propagation From Chip Selects



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2716; Optional (2) 2708

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* *Consult AMI sales office for format.*

ROMs

AMERICAN MICROSYSTEMS, INC.

S68332/S68A332

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- Fast Access Time:
  S68332: 450ns Maximum
  S68A332: 350ns Maximum
- Fully Static Operation
- Single +5V ±5% Power Supply
- Directly TTL Compatible Inputs
- Three-State TTL Compatible Outputs
- Two Programmable Chip Selects
- EPROM Pin Compatible—2532
- Extended Temperature Range Available

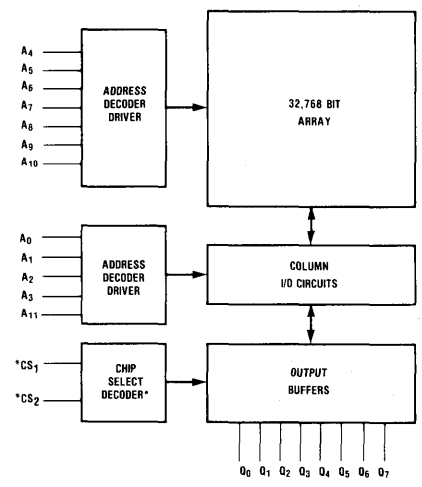
General Description

The AMI S68332 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68332 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

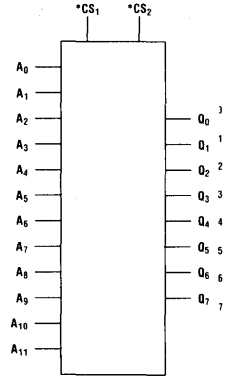
The S68332 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

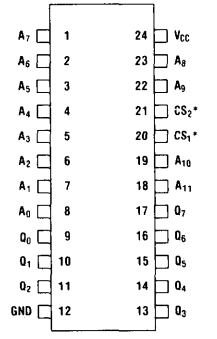


*PROGRAMMABLE CHIP SELECTS
MAY BE SPECIFIED AS ACTIVE LOW (CS) OR ACTIVE HIGH (CS) OR NO CONNECT (NC)

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{11}	Address Inputs
Q_0-Q_7	Data Outputs
CS_1-CS_2	Chip Select Inputs
V_{CC}	+5V Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_O=0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current			70	mA	

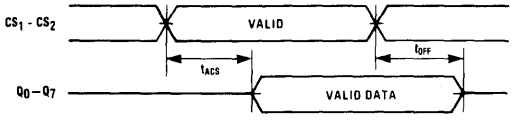
Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

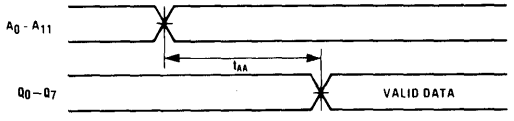
A.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to +70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68332			450	ns	See A.C. Test Conditions and Waveforms
		S68A332			350	ns	
t_{ACS}	Chip Select Access Time	S68332			150	ns	
		S68A332			150	ns	
t_{OFF}	Chip Deselect Time	S68332			150	ns	
		S68A332			150	ns	

Waveforms



Propagation From Chip Select



Propagation From Address

ROMs

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

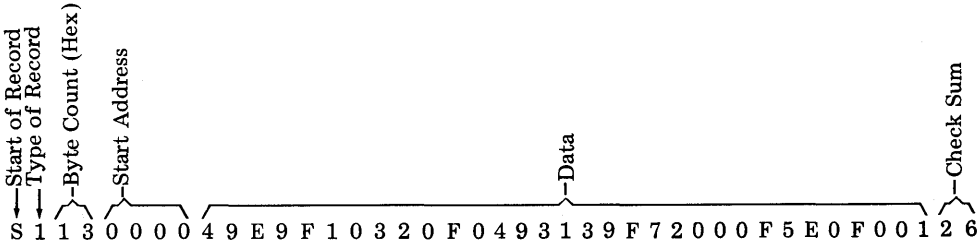
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



NOTES:
1. Only positive logic formats for CS_1 and CS_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S2333

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- Fast Access Time: 350ns Maximum
- Fully Static Operation
- Single +5V ±5% Power Supply
- Directly TTL Compatible Inputs
- Three-State TTL Compatible Outputs
- Two Programmable Chip Selects
- EPROM Pin Compatible (2732)
- Extended Temperature Range Available

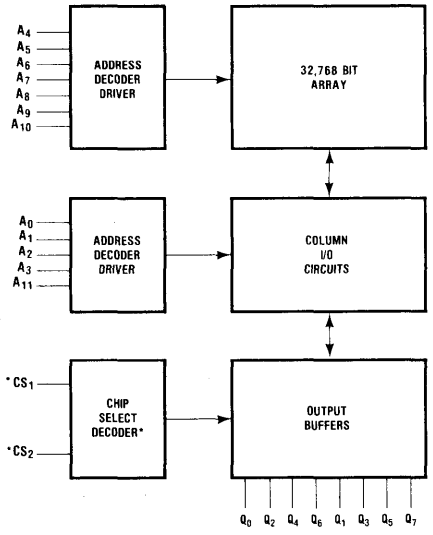
General Description

The AMI S2333 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2333 is pin compatible with UV EPROMs making system development much easier and more cost effective. The fully static S2333 requires no clocks for operation. The two chip selects are mask programmable with the active level for each being specified by the user.

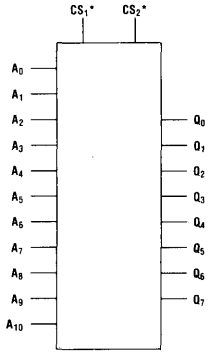
The S2333 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

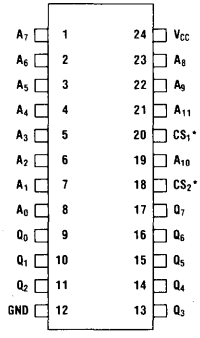


*PROGRAMMABLE CHIP SELECTS
MAY BE SPECIFIED AS ACTIVE LOW ($\overline{CS}$) OR ACTIVE HIGH (CS) OR NO CONNECT (NC)

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
$CS_1 - CS_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

ROMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias—T_A (Standard Part)	0°C to +70°C
(Industrial temp part)	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0V to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_O=0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current			70	mA	

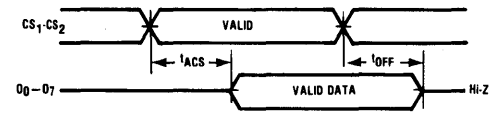
Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

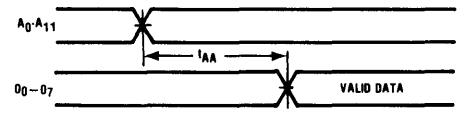
A.C. Characteristics: V_{CC} = +5V ± 5%, T_A=0°C to 70°C (Standard part); −40°C to +85°C (Industrial temp part)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			350	ns	See A.C. Test
t_{ACS}	Chip Select Access Time			120	ns	Conditions and
t_{OFF}	Chip Deselect Time			120	ns	Waveform

Waveforms



Propagation From Chip Select



Propagation From Address

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Rise and Fall Times	⩽ 20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-2732; Optional 2-2716

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

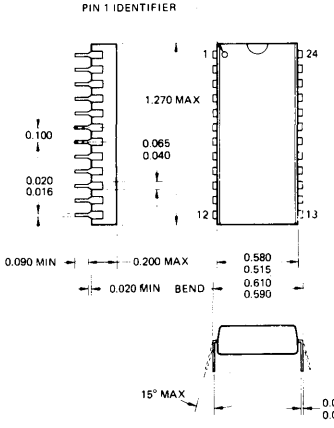
If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

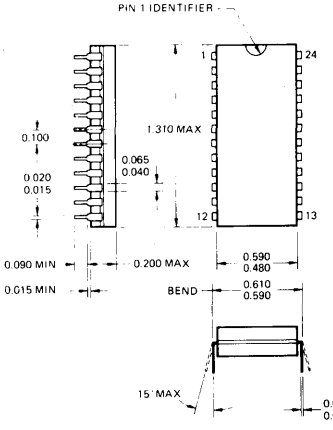
* *Consult AMI sales office for format.*

Package Outlines

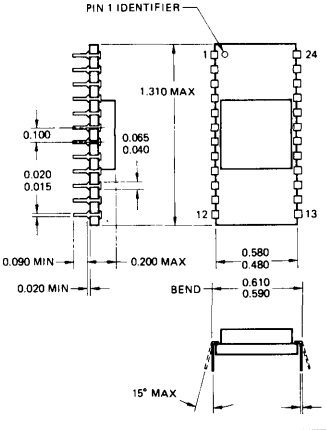
24-Pin Plastic



24-Pin Cer-DIP



24-Pin Ceramic



AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S68116/S68132/S68164

HIGH SPEED STATIC NMOS ROMS

Features

- ☐ Fast Access Time: S68116-110ns Maximum
  S68132-115ns Maximum
  S68164-120ns Maximum
- ☐ Low Standby Power Option
- ☐ Programmable Chip Select/Enable
- ☐ Fully Static Operation
- ☐ TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Standard JEDEC Pinouts
- ☐ EPROM Pin Compatible
- ☐ Late Mask Programmable

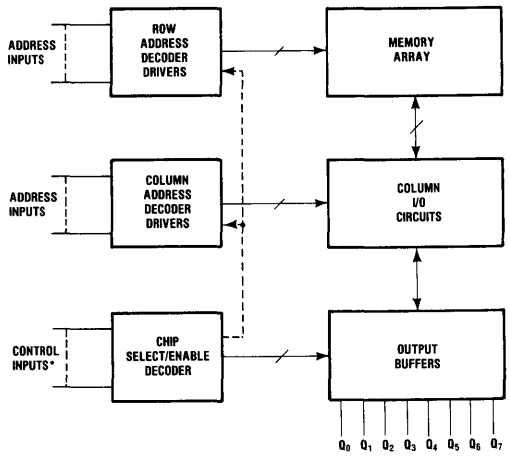
General Description

The AMI S681XX series of devices are fully static mask programmable NMOS ROMs organized as byte-wide devices. The devices are fully TTL compatible on all inputs and outputs and operate from a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The devices being fully static require no clocks for operation. The control lines are programmable as chip selects (CS) or chip enables (CE). The active levels also being specified by the user. When chip enables are specified and the device is not enabled, power supply current is reduced to 20mA maximum.

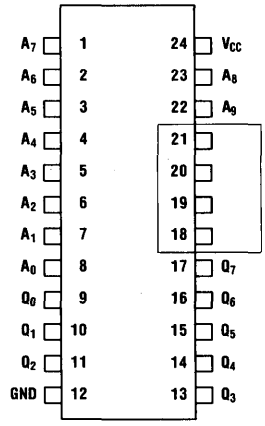
The S681XX series is fabricated using AMI's NMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram



*CONTROL FUNCTION AND ACTIVE LEVEL IS USER DEFINED

Pin Configuration



2kx8 S68116	4kx8 S68132	8kx8 S68164
CS/CE2	CS/CE2	A_{12}
CS/CE1	CS/CE1	CS/CE
A_{10}	A_{10}	A_{10}
CS/CE3	A_{11}	A_{11}

CONTROL FUNCTION AND ACTIVE LEVEL IS USER DEFINED

Pin Names

A_0-A_n	Address Inputs
Q_0-Q_7	Data Outputs
CS/CE	Programmable Chip Select/Enable
V_{CC}	5V;±10% Power Supply

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

Symbol	Parameter		Min.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage		2.4		V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage		−0.5	0.8	V	
V_{IH}	Input HIGH Voltage		2.0	V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN}=0V to 5.5V
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O=0.4V to 5.5V Chip Deselected
I_{SB}	Power Supply Current—Standby			20	mA	Chip Disabled
I_{CC}	Power Supply Current—Active	S68116		110	mA	Chip Enabled
		S68132		115	mA	
		S68164		120	mA	

Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

A.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

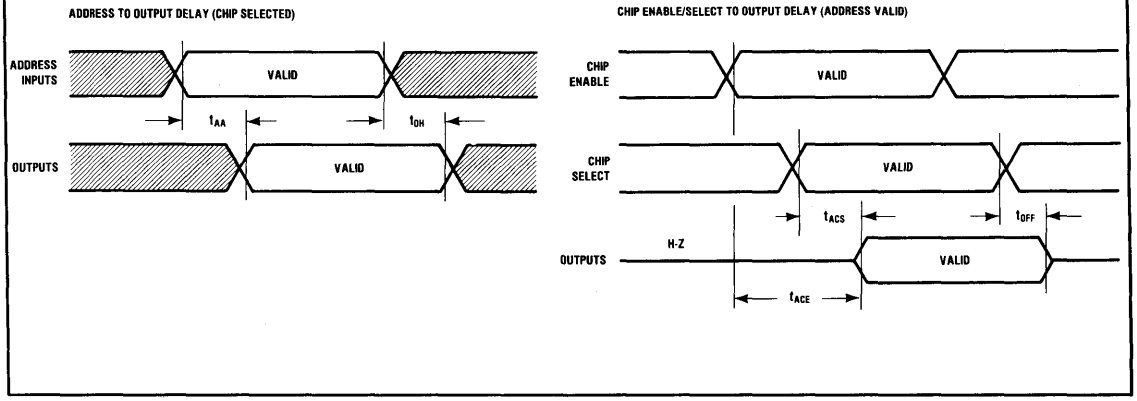
Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68116			110	ns	See A.C. Test Conditions and Waveforms
		S68132			115		
		S68164			120		
t_{ACE}	Chip Enable Access Time	S68116			110	ns	
		S68132			115		
		S68164			120		
t_{ACS}	Chip Select Access Time	S68116			50	ns	
		S68132			60		
		S68164			70		
t_{OFF}	Chip Deselect Time	S68116			50	ns	
		S68132			60		
		S68164			70		
t_{OH}	Output Hold Time	S68116	10			ns	
		S68132	15				
		S68164	20				

ROMs

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

S68116: 2716, S68132: 2532, S68164: 68764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

☐ 9 Track NRZ Magnetic Tape

☐ Paper Tape

☐ Card Deck

* *Consult AMI sales office for format.*

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S68A364/S68B364

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S68A364-350ns Maximum
  S58B364-250ns Maximum
- ☐ Low Standby Power: 85mW Maximum
- ☐ Late Mask Programmable
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Programmable Chip Enable

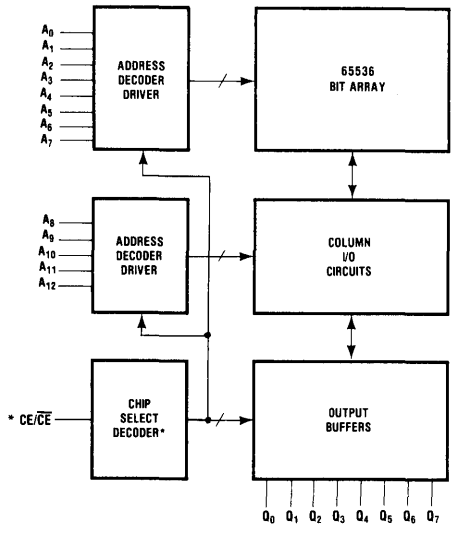
General Description

The AMI S68364 family are 65,536 bit static mask programmable NMOS ROMs organized as 8192 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and have a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The devices are fully static, requiring no clocks for operation. The chip enable is mask programmable, the active level being specified by the user. When not enabled, power supply current is reduced to a maximum of 15mA.

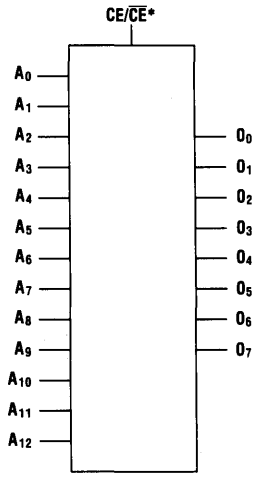
The S68364 family of devices are fabricated using AMI's NMOS ROM technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

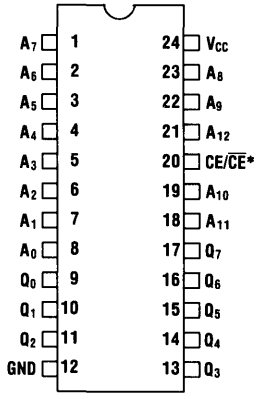


*USER DEFINED MASK PROGRAMMABLE CHIP ENABLE—MAY BE DEFINED AS ACTIVE HIGH, ACTIVE LOW, OR NO CONNECT.

Logic Symbol



Pin Configuration



Pin Names

A_0—A_{12}	Address Inputs
Q_0—Q_7	Data Outputs
CE/$\overline{CE}$	Programmable Chip Enable
V_{CC}	+5V Power Supply

ROMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN}=0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O=0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current S68A364			70	mA	
	S68B364			90	mA	
I_{SB}	Power Supply Current			15	mA	Chip Deselected

Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

A.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S68A364			350	ns	See A.C. Test Conditions and Waveforms
		S68B364			250	ns	
t_{ACE}	Chip Enable Access Time	S68A364			350	ns	
		S68B364			250		
t_{OFF}	Chip Deselect Time	S68A364			200	ns	
		S68B364			100	ns	

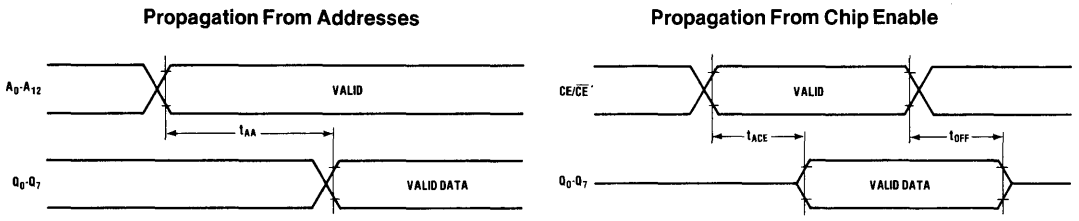
NOTES:

1. Only positive logic formats for CE/CE are accepted. 1=V_{HIGH}; 0=V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 68A764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* *Consult AMI sales office for format.*

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S4264

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- Single +5V±10% Power Supply
- High Performance:
  Maximum Access Time: 350ns
- EPROM Compatible for Cost Effective System Development
- Completely Static Operation:
- Directly TTL Compatible Inputs
- Three-State TTL Compatible Outputs

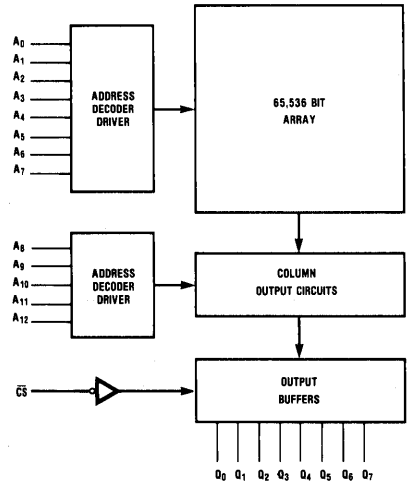
General Description

The AMI S4264 is a 65,536 bit fully static NMOS mask programmable ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

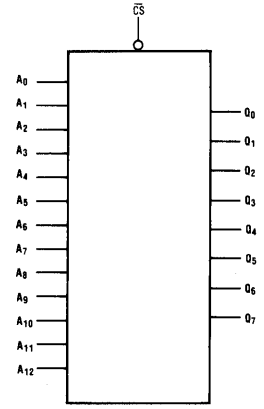
The S4264 is fully static requiring no clocks for operation. Data access is simple as no address setup times are required. The byte organization of the S4264 makes it ideal for microprocessor applications.

The S4264 is fabricated using AMI's proprietary NMOS technology. This process permits the manufacture of very high density, high performance mask programmable ROMs.

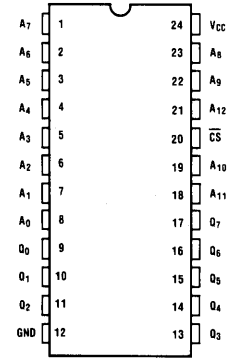
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0-A_{12}	Address Inputs
Q_0-Q_7	Data Outputs
$\overline{CS}$	Chip Select
V_{CC}	+5V Power Supply

Truth Table

Input	Outputs	Mode
$\overline{CS}$	Q_0-Q_7	
L	D_{OUT}	Read
H	Hi-Z	Deselected

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to 150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics:

$V_{CC} = +5V \pm 10\%, T_A = 0°C$ to $70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 3.2mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -220\mu A$
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current			10	μA	$\overline{CS} \geq 2.4V$, $V_O = 0.4V$ to V_{CC}

Capacitance: $T_A = 25°C$, $f = 1.0MHz$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

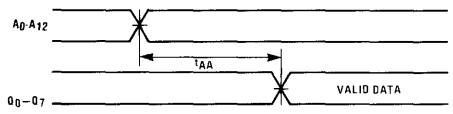
A.C. Characteristics:

$V_{CC} = +5V \pm 10\%, T_A = 0°C$ to $+70°C$

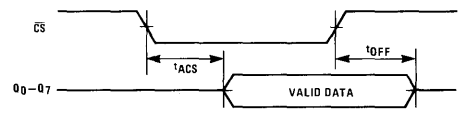
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			350	ns	See A.C. Test
t_{ACS}	Chip Enable Access Time			150	ns	Conditions and
t_{OFF}	Chip Deselect Time			80	ns	Waveforms

Wave Forms

Propagation Delay From Address



Propagation Delay From Chip Select



ROMs

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Rise and Fall Times	≤20ns
Input Timing Level	1.5V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2-2532

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* *Consult AMI sales office for format.*

AMERICAN MICROSYSTEMS, INC.

S2364/S2364A

65,536 BIT (8192x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: S2364 450ns Maximum
  S2364A 350ns Maximum
- ☐ Low Standby Power
  55mW Maximum
- ☐ Late Mask Programmable
- ☐ Fully Static Operation
- ☐ Single +5V ±10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Enables
- ☐ EPROM Pin Compatible (2764)

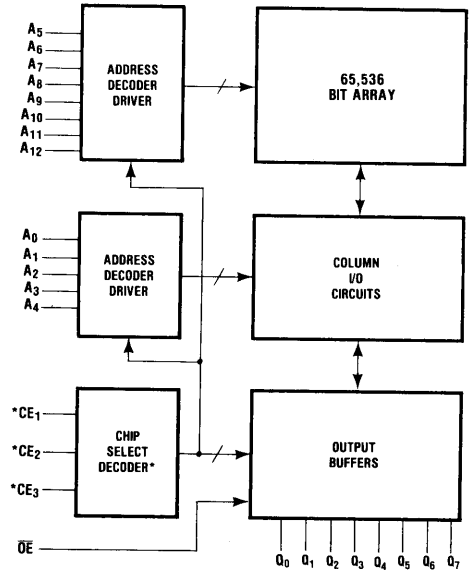
General Description

The AMI S2364 family are 65,536 bit static mask programmable NMOS ROMs organized as 8192 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and operate from a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S2364/S2364A are pin compatible with the 2764 UV EPROM making system development much easier and more cost effective. They are fully static, requiring no clocks for operation. The three chip enables are mask programmable; the active level for each being specified by the user. When the device is not enabled, the power supply current is reduced to a 10mA maximum.

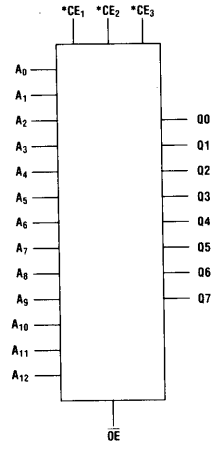
The S2364 family is fabricated using AMI's N-Channel NMOS ROM technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

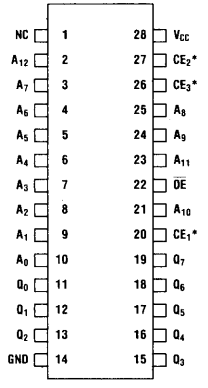


*USER DEFINED MASK PROGRAMMABLE CHIP ENABLE—MAY BE DEFINED AS ACTIVE HIGH, ACTIVE LOW, OR NO CONNECT.

Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{12}$	Address Inputs
$Q_0 - Q_7$	Data Outputs
CE_1, CE_2, CE_3	Chip Enables (User Defined)
$\overline{OE}$	Output Enable
V_{CC};GND;NC	5V;Ground;No Connect

ROMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage				0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage		−0.5		0.8	V	
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current				10	μA	V_{IN}=0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current				10	μA	V_O=0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current	S2364			70	mA	
		S2364A			70	mA	
I_{SB}	Power Supply Current	S2364			10	mA	
		S2364A			10	mA	

Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

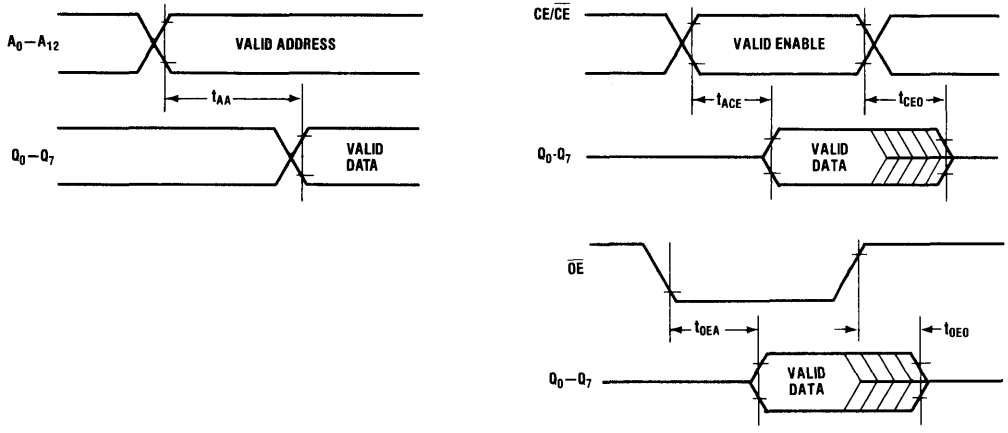
A.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time	S2364			450	ns	See A.C. Test Conditions and Waveforms
		S2364A			350	ns	
t_{ACE}	Chip Enable Access Time	S2364			450	ns	
		S2364A			350		
t_{CEO}	Disable Time From Chip Enable	S2364			250	ns	
		S2364A			200		
t_{OEA}	Output Enable Access Time	S2364			150	ns	
		S2364A			100		
t_{OEO}	Disable Time From $\overline{OE}$	S2364			150	ns	
		S2364A			100		

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-2764; Optional 2-2732

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

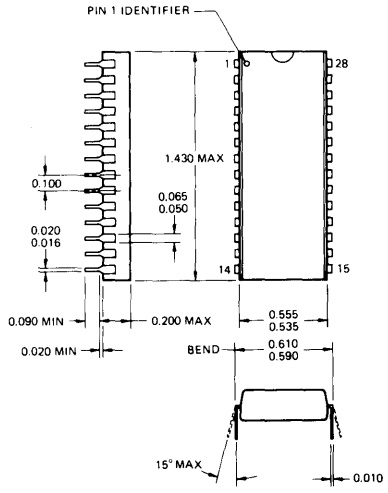
- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* *Consult AMI sales office for format.*

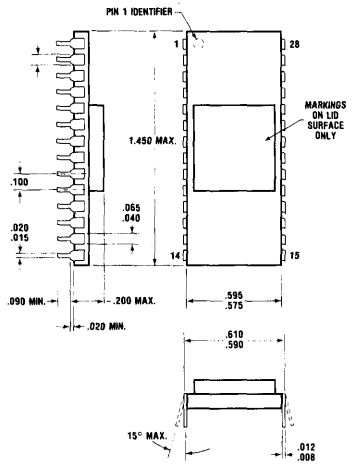
ROMs

Package Outlines

28-Pin Plastic



28-Pin Ceramic



Truth Table: CE_1, CE_2, & CE_3 are user defined; chip is enabled when CE_1, CE_2 & CE_3 inputs match the user defined logic states.

CE_1	CE_2	CE_3	$\overline{OE}$	Outputs	Power
$\overline{CE_1}$	X	X	X	Hi-Z	Stby
X	$\overline{CE_2}$	X	X	Hi-Z	Stby
X	X	$\overline{CE_3}$	X	Hi-Z	Stby
CE_1	CE_2	CE_3	H	Hi-Z	Active
CE_1	CE_2	CE_3	L	Data Out	Active

X=Don't Care Condition

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S23128

131,072 BIT (16384x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 250ns Max.
- ☐ Low Standby Power: 66mW Max.
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Outputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Enables/Selects
- ☐ EPROM Pin Compatible (27128)
- ☐ Late Mask Programmable
- ☐ Programmable Output/Chip Enable

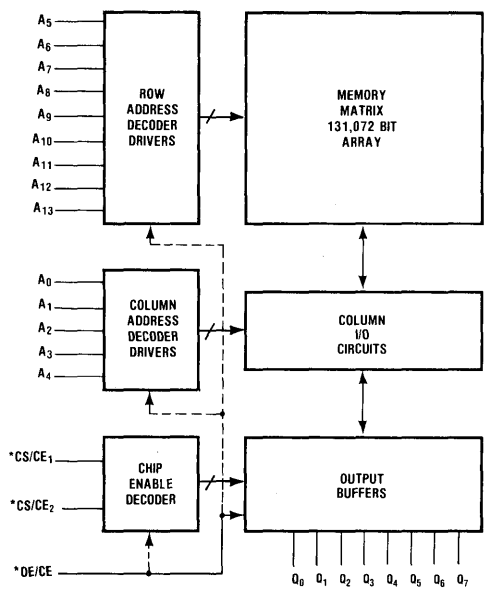
General Description

The AMI S23128 is a 131,072 bit static mask programmable NMOS ROM organized as 16,384 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23128 is pin compatible with the 27128 EPROM making system development easier and more cost effective. The fully static S23128 requires no clocks for operation. The three control pins are mask programmable with the active level and function being specified by the user. The pins can also be programmed as no connections. If CE functions are selected, automatic powerdown is available. The power supply current is reduced to 12mA when the chip is disabled.

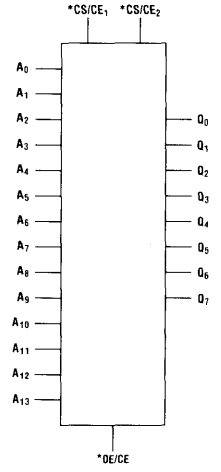
The S23128 is fabricated using AMI's NMOS technology. This permits the manufacture of high density, high performance ROMs.

Block Diagram

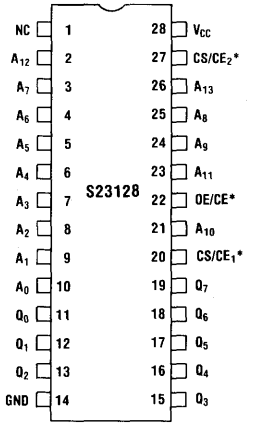


* THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE.

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{13}	Address Inputs
Q_0-Q_7	Data Outputs
CS/CE_1-CS/CE_2	Chip Selects/Enables
OE/CE	Output Enable/Chip Enable
V_{CC};GND;NC	5V;Ground; No Connect

ROMs

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin With Respect to Ground	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: $V_{CC} = +5V \pm 10\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 3.2mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -220\mu A$
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current	−10		10	μA	$V_{IN} = 0V$ to V_{CC}
I_{LO}	Output Leakage Current	−10		10	μA	$V_O = 0.4V$ to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			25	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			12	mA	Chip Disabled

Capacitance: $T_A = 25°C$, $f = 1.0MHz$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: $V_{CC} = +5V \pm 10\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			250	ns	See A.C.
t_{ACE}	Chip Enable Access Time			250	ns	Test Conditions
t_{OE}	Output Enable Access Time	0		80	ns	
t_{ACS}	Chip Select Access Time	0		80	ns	and
t_{CE0}	Disable Time From Chip Enable	0		80	ns	Waveforms
t_{OFF}	Chip Deselect Time	0		80	ns	
t_{OEO}	Disable Time From Output Enable	0		80	ns	
t_{OH}	Output Hold Time	0			ns	

Truth Table:

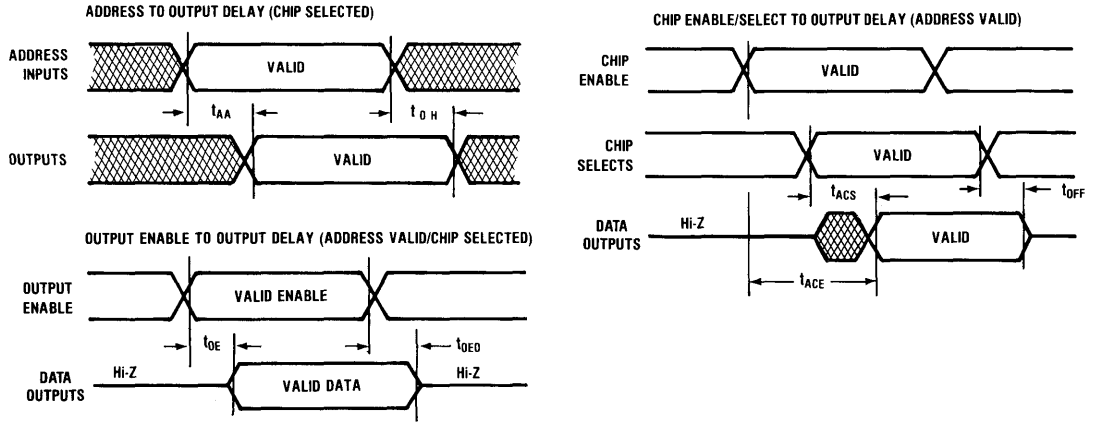
CS/CE1	CS/CE2	OE/CE	Outputs	Power
$\overline{CE1}$	X	X	Hi-Z	Standby
X	$\overline{CE2}$	X	Hi-Z	Standby
X	X	$\overline{CE}$	Hi-Z	Standby
$\overline{CS1}$	CS/CE2	OE/CE	Hi-Z	Active
CS/CE1	$\overline{CS2}$	OE/CE	Hi-Z	Active
CS/CE1	CS/CE2	$\overline{OE}$	Hi-Z	Active
CS/CE1	CS/CE2	OE/CE	Data Out	Active

The user decides between a CS/CE and OE/CE function and then defines the active level. The functions may also be defined as No Connections (NC). The chip is enabled when the inputs match the user defined states.

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 1-27128; Optional 2-2764

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* *Consult AMI sales office for format.*

ROMs

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY

S23256

262,144 BIT (32,768x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 150ns Maximum
- ☐ Low Power Dissipation
  Active Current: 40mA Maximum
  Standby Current: 10mA Maximum
- ☐ Fully Static Operation
- ☐ Two User-Defined and Programmable Control Lines
- ☐ EPROM Pin Compatible
- ☐ Late Mask Programmable

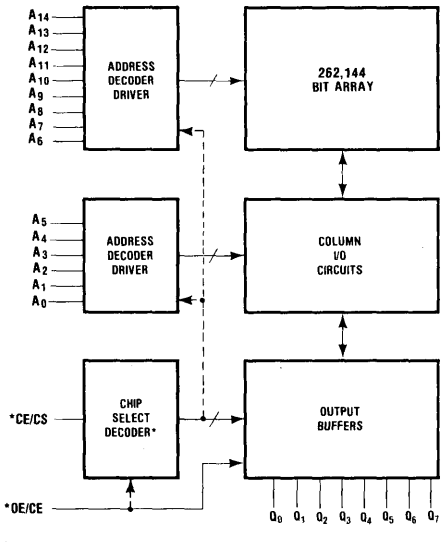
General Description

The AMI S23256 is a 262,144 bit static mask programmable NMOS ROM organized as 32,768 words by 8 bits. The devices are fully TTL compatible on all inputs and outputs and operate from a single +5V ±10% power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S23256 is pin compatible with the 27128 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation.

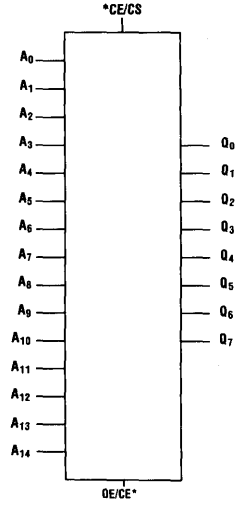
The S23256 is fabricated using AMI's N-Channel MOS ROM technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram

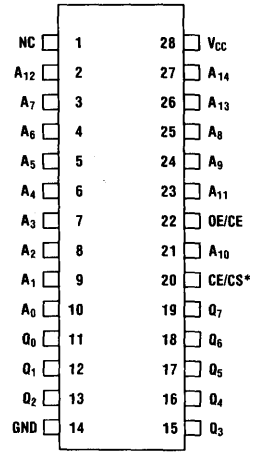


*THE USER DECIDES BETWEEN A CE OR CS AND OE OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL

Logic Symbol



Pin Configuration



Pin Names

A_0-A_{14}	Address Inputs
Q_0-Q_7	Data Outputs
CE/CS	Chip Enable/Chip Select
OE/CE	Output/Chip Enable
V_{CC};GND;NC	5V;Ground;No Connect

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Output or Supply Voltages	−0.5V to 7V
Input Voltages	−0.5V to 7V
Power Dissipation	1W

COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL}=3.2mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH}=−220μA
V_{IL}	Input LOW Voltage	−0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
$\|I_{LI}\|$	Input Leakage Current			10	μA	V_{IN}=0V to V_{CC}
$\|I_{LO}\|$	Output Leakage Current			10	μA	V_O=0.4V to V_{CC} Chip Deselected
I_{CC}	Power Supply Current—Active			40	mA	Chip Enabled
I_{SB}	Power Supply Current—Standby			10	mA	Chip Disabled

Capacitance: T_A=25°C, f=1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN}=0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT}=0V

A.C. Characteristics: V_{CC} = +5V ± 10%, T_A=0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AVQV}	Address Access Time			150	ns	See A.C. Test Conditions and Waveform
t_{AXQZ}	Output Hold/Address Change	10			ns	
t_{EVQV}	Chip Enable Access Time			150	ns	
t_{SVQV}	Chip Select Access Time			120	ns	
t_{GVQV}	Output Enable Access Time			120	ns	
t_{EXQZ}, t_{SXQZ}, t_{GXQZ}	Deselect Times			80	ns	

Truth Table

CE/CS	OE/CE	OUTPUTS	POWER
CE/CS	OE/CE	DATA OUT	ACTIVE
$\overline{CE}$	X	HIGH Z	STANDBY
$\overline{CS}$	X	HIGH Z	ACTIVE
X	$\overline{OE}$	HIGH Z	ACTIVE
X	$\overline{CE}$	HIGH Z	STANDBY

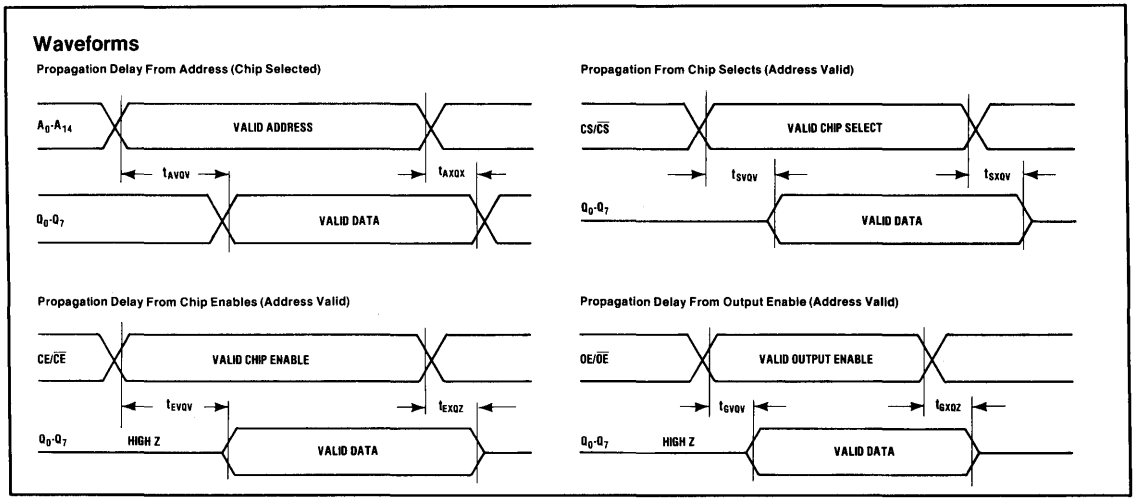
THE DEVICE IS ENABLED WHEN THE CONTROL LINES MATCH THE USER DEFINED STATES.

ROMs

A.C. Test Conditions

Input Pulse Levels	0.8V and 2.0V
Input Timing Level	0.8V and 2.0V
Output Timing Levels	0.4V and 2.4V
Output Load	1 TTL Load and 100pF

Waveforms



ROM Code Data

AMI's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. AMI will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the AMI computer system. The AMI programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested AMI will not proceed until the customer verifies the program in the returned EPROM.

EPROM Requirements

The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 2-27128

If two EPROMs are used to specify one ROM pattern, two blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the two EPROMs is for lower and upper address locations in the ROW. The preferred method is to mark the EPROM with the ROM address (in Hex) where the EPROM data is to be located.

Pattern Data from ROMS

If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the AMI device. The programmable chip selects must be defined. (NOTE: In some cases a competitors ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the AMI ROM, the required active logic level for this input must be specified.)

Optional Method of Supply ROM Data*

If an EPROM or ROM cannot be supplied the following, other methods are acceptable.

- ☐ 9 Track NRZ Magnetic Tape
- ☐ Paper Tape
- ☐ Card Deck

* *Consult AMI sales office for format.*

Communication Products

S25910	Ten Number 14 Digit DTMF Repertory Dialer With Last Number Redial
S3508	Asynchronous Version of the S3506 A-Law Codec
S3509	Asynchronous Version of the S3507 μ-Law Codec
S3527	16 Tap Analog Transversal Filter With 9-Bit Tap Control. Designed for Equalizing Band Signals
S3528	Programmable Low Pass Filter
S3530	300 Baud Single Chip Modem

ROMs

680XX	High Speed Family of NMOS ROMs Including 12K, 32K, 64K Bi-Polar PROM Pin-Outs

AMERICAN MICROSYSTEMS, INC.

Application Note Summary

Consumer Products

Useful Noise

The S2688 Noise Generator is useful in many applications where digital noise is required for audio effects.

MOS Music

MOS Music is a primer on the application of standard MOS/LSI circuits in creating electronic music. This note discusses the key elements of music production in an electronic organ.

Real Remote Control

A remote control system using the S2742 and S2743 with infrared transmission is shown. A simple but effective alignment technique is demonstrated which will ensure successful operation.

S6800 Family

A Minimal S6802/S6846 Systems Design

Details how to make an S6802/S6846 version of the EVK in a minimal systems application.

Microprocessor Crystal Specification

Aids the MPU system designer in specifying and ordering the crystal required for the S6802 microprocessor.

S68488 General Purpose Interface Adapter

Describes basic design information needed in using the S68488 GPIA.

S68045 Compared with Motorola MC 6845

Describes the fundamental differences between the two devices.

S9900 Family

S9900 Simplifies Design of Bi-Directional I/O Module

Illustrates use of the CPU. The design can be used for simple TTL logic testers. (Reprint from *Electronics)*

S9900 Minimum System Design with the S9900 16-Bit Microprocessor

This design uses just the CPU, a 1K ROM, a 2K RAM, a clock and six smaller IC's.

S9900 Controlled Dot Matrix Printer

S9900 shows how to control a 7040 series dot matrix printer in a minimal systems application.

S9900 Technical Article Reprints

A compilation of 6 technical articles covering: a comparison of the 9900, Z8000 and 8086; an 8-page description of the 9900; a real-time control software design using the 9900; a multiprocessor system design using the 9900; the bi-directional I/O module identical to the above application note; using the 9940 to implement the NBS data encryption standard.

At AMI we are continually searching for more effective methods of providing protection for MOS devices. Present configurations of protective devices are the result of years of research and review of field problems.

Although the oxide breakdown voltage may be far beyond the voltage levels encountered in normal operation, excessive voltages may cause permanent damage. Even though AMI has evolved the best designed protective device possible, we recognize that it is not 100% effective.

A large number of failed returns have been due to misapplication of biases. In particular, forward bias conditions cause excessive current through the protective devices, which in turn will vaporize metal lines to the inputs. *Careful inspection of the device data sheets and proper pin designation should help reduce this failure mode.*

Gate ruptures caused by static discharge also account for a large percentage of device failures in customers' manufacturing areas. *Precautions should be taken to minimize the possibility of static charges occurring during handling and assembly of MOS circuits.*

To assist our customers in reducing the hazards which may be detrimental to MOS circuits, the following guidelines for handling MOS are offered. *The precautions listed here are used at AMI.*

1. All benches used for assembly or test of MOS circuits are covered with conductive sheets. WARNING: Never expose an operator directly to a hard electrical ground. For safety reasons, the operator must have a resistance of at least 100K Ohms between himself and hard electrical ground.
2. All entrances to work areas have grounding plates on door and/or floor, which must be contacted by people entering the area.
3. Conductive straps are worn inside and outside of employees' shoes so that body charges are grounded when entering work area.
4. Anti-static neutralized smocks are worn to eliminate the possibility of static charges being generated by friction of normal wear. Two types are available; Dupont anti-static nylon and Dupont neutralized 65% polyester/35% cotton.
5. Cotton gloves are worn while handling parts. Nylon gloves and rubber finger cots are not allowed.
6. Humidity is controlled at a minimum of 35% to help reduce generation of static voltages.
7. All parts are transported in conductive trays. Use of plastic containers is forbidden. Axial leaded parts are stored in conductive foam, such as Velofoam#7611.
8. All equipment used in the assembly area must be thoroughly grounded. Attention should be given to equipment that may be inductively coupled and generate stray voltages. Soldering irons must have grounded tips. Grounding must also be provided for solder posts, reflow soldering equipment, etc.
9. During assembly of ICs to printed circuit boards, it is advisable to place a grounding clip across the fingers of the board to ground all leads and lines on the board.
10. Use of carpets should be discouraged in work areas, but in other areas may be treated with anti-static solution to reduce static generation.
11. MOS parts should be handled on conductive surfaces and the handler must touch the conductive surface *before* touching the parts.
12. In addition, no power should be applied to the socket or board while the MOS device is being inserted. This permits any static charge accumulated on the MOS device to be safely removed before power is applied.
13. MOS devices should not be handled by their leads unless absolutely necessary. If possible, MOS devices should be handled by their packages as opposed to their leads.
14. In general, materials prone to static charge accumulation should not come in contact with MOS devices.

These precautions should be observed even when an MOS device is suspected of being defective. The true cause of failure cannot be accurately determined if the device is damaged due to static charge build-up.

It should be remembered that even the most elaborate physical prevention techniques will not eliminate device failure if personnel are not fully trained in the proper handling of MOS.

This is a most important point and should not be overlooked.

More information can be obtained by contacting the Product Assurance Department.

American Microsystems, Inc.
3800 Homestead Road
Santa Clara, California 95051
Telephone (408) 246-0330
TWX 910-338-0024 or 910-338-0018

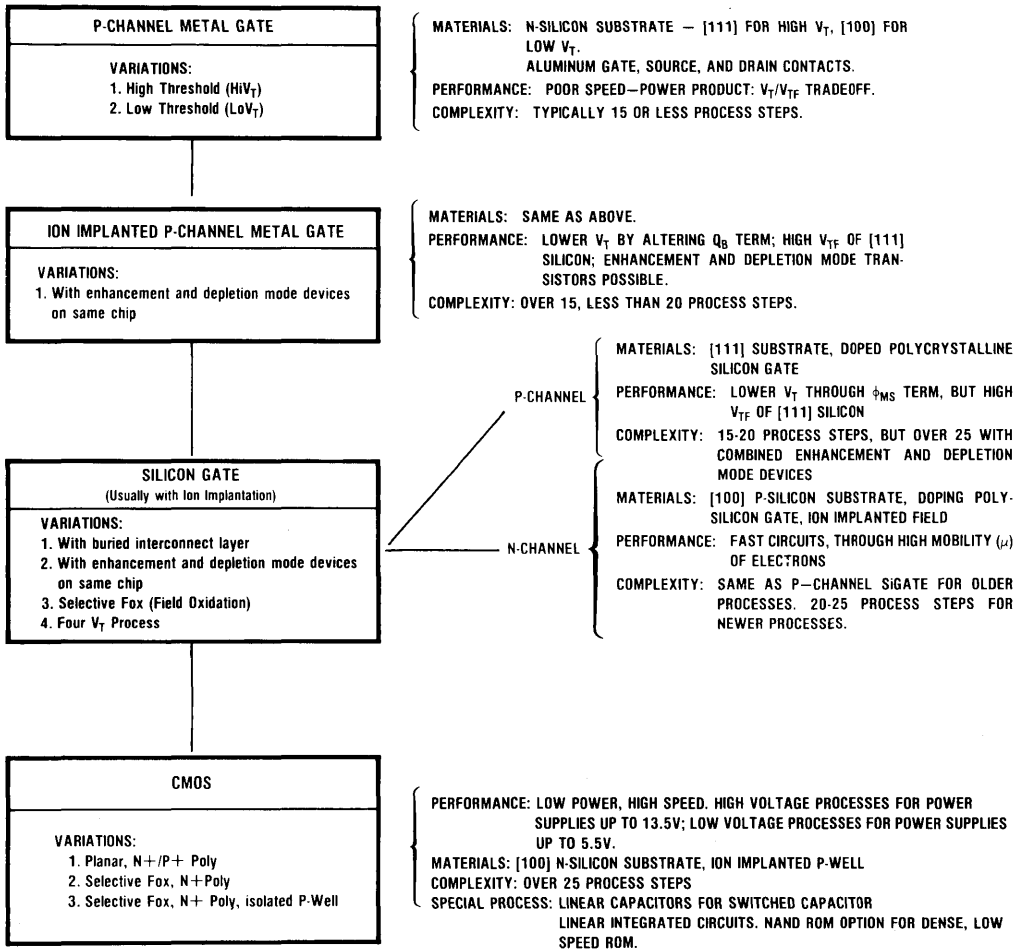
PROCESS DESCRIPTIONS

Each of the major MOS processes is described on the following pages. First, the established production proven processes are described, followed by those advanced processes, which are starting to go into volume production now. In each case, the basic processes is described first, followed by an explanation of its advantages, applications, etc.

P-CHANNEL METAL GATE PROCESS

Of all the basic MOS processes, P-Channel Metal Gate is the oldest and the most completely developed. It has served as the foundation for the MOS/LSI industry and still finds use today in some devices. Several versions of this process have evolved since its earliest days. A thin slice (8 to 10 mils) of lightly doped N-type silicon wafer serves as the substrate or body of the MOS transistor. Two closely spaced, heavily doped P-type regions, the source and drain, are formed within the substrate by selective diffusion of an impurity that provides holes as majority electrical carriers. A thin deposited layer of aluminum metal, the gate, covers the area between the source and drain regions, but is electrically insulated from the substrate by a thin layer (1000-15000Å) of silicon dioxide. The P-Channel transistor is turned on by a negative gate voltage and conducts current between

Figure B.1. Summary of MOS Process Characteristics



the source and the drain by means of holes as the majority carriers.

The basic P-Channel metal gate process can be subdivided into two general categories: *High-threshold and low-threshold.* Various manufacturers use different techniques (particularly so with the low threshold process) to achieve similar results, but the difference between them always rests in the threshold voltage V_T required to turn a transistor on. The high threshold V_T is typically -3 to -5 volts and the low threshold V_T is typically -1.5 to -2.5 volts.

The original technique used to achieve the difference in threshold voltages was by the use of substrates with different crystalline structures. The high V_T process used [111] silicon whereas, the low V_T process used [100] silicon. The difference in the silicon structure causes the surface charge between the substrate and the silicon dioxide to change in such a manner that it lowers the threshold voltages.

One of the main advantages of lowering V_T is the ability to interface the device with TTL circuitry. However, the use of [100] silicon carries with it a distinct disadvantage also. Just as the surface layer of the [100] silicon can be inverted by a lower V_T, so it also can be inverted at other random locations—through the thick oxide layers—by large voltages that may appear in the metal interconnections between circuit components. This is undesirable because it creates parasitic transistors, which interfere with circuit operation. The maximum voltage that can be carried in the interconnections is called the parasitic field oxide threshold voltage V_{TF}, and generally limits the overall voltage at which a circuit can operate. This, then, is the main factor that limits the use of the [100] low V_T process. A drop in V_{TF} between a high V_T and low V_T process may, for example, be from -28V to -17V.

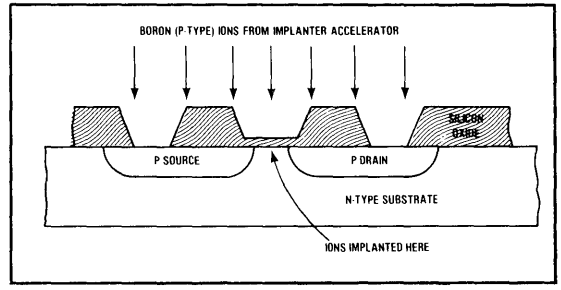
The low V_T process, because of its lower operating voltages, usually produces circuits with a lower operating speed than the high V_T process, but is easier to interface with other circuits, consumes less power, and therefore is more suitable for clocked circuits. Both P-Channel metal gate processes yield devices slower in speed than those made by other MOS processes, and have a relatively poor speed/power product. Both processes require two power supplies in most circuit designs, but the high V_T process, because it operates at a high threshold voltage, has excellent noise immunity.

Ion Implanted P-Channel Metal Gate Process

The P-Channel Ion Implanted process uses essentially the same geometrical structure and the same materials as the high V_T P-Channel process, but includes the ion implantation step. The purpose of ion implantation is to introduce P-type impurity ions into the substrate in the limited area under the gate electrode. By changing the characteristics of the substrate in the gate area, it is possible to lower the threshold voltage V_T of the transistor, without influencing any other of its properties.

Figure B.2. shows the ion implantation step in a diagrammatic manner. It is performed after the gate oxide is grown, but before the source, gate, and drain metallization deposition. The wafer is exposed to an ion beam which penetrates through the thin gate oxide layer and implants ions into the silicon substrate. Other areas of the substrate are protected both by the thicker oxide layer and sometimes also by other masking means. Ion implantation can be used with any process and, therefore could, except for the custom of the industry, be considered a special technique, rather than a process in itself.

Figure B.2. Diagram of Ion Implantation Step



The implantation of P-type ions into the substrate, in effect, reduces the effective concentration of N-type ions in the channel area and thus lowers the V_T required to turn the transistor on. At the same time, it does not alter the N-type ion concentration elsewhere in the substrate and therefore, does not reduce the parasitic field oxide threshold voltage V_{TF} (a problem with the low V_T P-Channel Metal Gate process, described above). The [111] silicon usually is used in ion-implanted transistors.

In fact, if the channel area is exposed to the ion beam long enough, the substrate in the area can be turned into P-type silicon (while the body of the substrate still re-

mains N-type) and the transistor becomes a depletion mode device. In any circuit some transistors can be made enhancement type, while others are depletion type, and the combination is a very useful circuit design tool.

The Ion-implanted P-Channel Metal Gate process is very much in use toady. Among all the processes, it represents a good optimization between cost and performance and thus is the logical choice for many common circuits, such as memory devices, data handling (communication) circuits, and others.

Because of its low V_T, it offers the designer a choice of using low power supply voltages to conserve power or increase supply voltages to get more driving power and thus increase speed. At low power levels it is more feasible to implement clock generating and gating circuits on the chip. In most circuit designs only a single power supply voltage is required.

N-CHANNEL PROCESS

Historically, N-Channel process and its advantages were known well at the time when the first P-Channel devices were successfully manufactured; however, it was much more difficult to produce N-Channel. One of the main reasons was that the polarity of intrinsic charges in the materials combined in such a way that a transistor was on at 0V and had a V_T of only a few tenths of a volt (*positive*). Thus, the transistor operated as a marginal depletion mode device without a well-defined *on/off* biasing range. Attempts to raise V_T by varying gate oxide thickness, increasing the substrate doping, and back biasing the substrate, created other objectionable results and it was not until research into materials, along with ion implantation, silicon gates, and other improvements came about that N-Channel became practical for high density circuits.

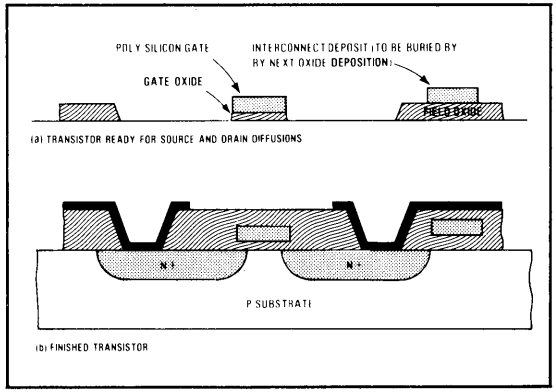
The N-Channel process gained its strength only after the P-Channel process, ion implantation, and silicon gate all were already well developed. N-Channel went into volume productions with advent of the 4K dynamic RAM and the microprocessor, both of which required speed and high density. Because P-Channel processes were nearing their limits in both of these respects, N-Channel became the logical answer.

The N-Channel process is structurally different from any of the processes described so far, in that the source, drain, and channel all are N-type silicon, whereas the body of the substrate is P-type. Conduction in the N-Channel is by means of electrons, rather than holes.

The main advantage of the N-Channel process is that the mobility of electrons is about three times greater than that of holes and, therefore, N-Channel transistors are faster than P-Channel . In addition, the increased mobility allows more current flow in a channel of any given size, and therefore N-Channel transistors can be made smaller. The positive gate voltage allows an N-Channel transistor to be completely compatible with TTL.

Although metal gate N-Channel processes have been used, the predominant N-Channel process is a silicon gate process. Among the advantages of silicon gate is the possibility of a buried layer of interconnect lines, in addition to the normal aluminum interconnections deposited on the surface of the chip. This gives the circuit designer more latitude in layout and often allows the reduction of the total chip size. Because the polysilicon gate electrode is deposited in a separate step, after the thick oxide layer is in place, the simultaneous deposition of additional polysilicon interconnect lines is only a matter of masking. These interconnect lines are buried by later steps, as shown in Figure B.3.

Figure B.3. Crosssection of an N-Channel Silicon Gate MOS Transistor



One minor limitation associated with the buried interconnect lines is their location. Because the source and drain diffusions are done after the polysilicon is deposited [see (a) of Figure B.3] the interconnect lines cannot be located over these diffusion regions.

A second advantage of a silicon gate is associated with the reduction of overlap between the gate and both the source and drain. This reduces the parasitic capacitance at each location and improves speed, as well as power consumption characteristics. Whereas in the metal gate process, the P region source and drain diffusion must be done prior to deposition of the gate electrode, in silicon gate process, the electrode is in place during diffusion, see (a) of Figure B.3. Therefore, no planned overlap for manufacturing tolerance purposes need exist and the gate is said to be *self-aligned.* The only overlap that occurs is due to the normal lateral extension of the source and drain regions during the diffusion process.

The silicon-gate process produces devices that are more compact than metal gate, and are slightly faster because of the reduced gate overlap capacitance. Because the basic silicon gate process is relatively simple, it is also economical. It is a versatile process that is used in memory devices and most any other circuit.

N-Channel development continues at a vigorous pace, resulting in all kinds of process variations, production techniques and applications. The combination of high speed, TTL compatibility, low power requirements, and compactness have already made N-Channel the most widely used process. The cost of N-Channel has been coming down also.

In addition to its use in large memory chips and microprocessors, N-Channel has become a good general purpose process for circuits in which compactness and high speed are important.

CMOS

The basic CMOS circuit is an inverter, which consists of two adjacent transistors—one an N-Channel, the other a P-Channel, as shown in Figure B.4. The two are fabricated on the same substrate, which can be either N or P type.

The CMOS inverter in Figure B.4 is fabricated on an N-type silicon substrate in which a P "tub" is diffused to form the body for the N-Channel transistor. All other steps, including the use of silicon gates and ion implantation, are much the same as for other processes.

The main advantage of CMOS is extremely low power consumption. When the common input to both gate electrodes is at a logic 1 (a positive voltage) the N-Channel transistor is biased on, the P-Channel is off, and the output is near ground potential. Conversely, when the input is at a logic 0 level, its negative voltage biases only the P-Channel transistor on and the output is near the drain voltage $+V_{DD}$. In either case, only one of the two transistors is on at a time and thus, there is virtually no current flow and no power consumption. Only during the transition from one logic level to the other are both transistors on and current flow increases momentarily.

Silicon Gate CMOS is also fast, approaching speeds of bipolar TTL circuits. On the other hand, the use of two transistors in every gate makes CMOS slightly more complex and costly, and requires more chip size. For these reasons, the original popularity of CMOS was in SSI logic elements and MSI circuits—logic gates, inverters, small shift registers, counters, etc. These CMOS devices consititute a logic family in the same way as TTL, ECL, and other bipolar circuits do; and in the areas of very low power consumption, high noise immunity, and simplicity of operation, are still widely accepted by discrete logic circuit designers.

Low power CMOS circuits made the watch circuit possible and also have been used in space exploration, battery operated consumer products, and automotive control devices. As experience was gained with CMOS, tighter design rules and reduced device sizes have been implemented and now LSI circuits, such as 1K RAM memories and microprocessors, are being manufactured in volume.

CMOS circuits can be operated on a single power supply voltage, which can be varied from +2.5 to about +13.5 volts with the high voltage processes, with a higher voltage giving more speed and higher noise immunity. Low voltage processes allow single power supply voltages from +1.5 to +5.5 volts.

The first implementation of an inverting gate is a process that uses both n+ to p+ polysilicon. The basic structure is a first-generation approach to which a selective field-oxidation process has been added.

Figure B.5 shows the plan and section views of the three-device gate portion. Because the P-Well in the top view spans both N-Channel devices, it is referred to as ubiquitous, and the process is called Ubiquitous P-Well.

In this planar process, p+ guard rings are used to reduce

surface leakage. Polysilicon cannot cross the rings, however, so that bridges must be built. Note the use of p+ polysilicon in the P-Channel areas. The plan view shows the construction of the bridges linking p+ to metal to n+. (Were the process to be used for a low-voltage, first-generation application like a watch circuit, the guard rings would not be necessary and polysilicon could directly connect N-Channel and P-Channel devices; however, to ensure good ohmic contact from one type of polysilicon to another, polysilicon-diode contacts must be capped with metal.)

This process provides a buried contact (n+ polysilicon to n+ diffusion) that can yield a circuit-density advantage. However, neither of the other two second-generation approaches provides buried contacts. Therefore, if a layout in this process is to be compatible with the others, the buried contact must be eliminated. Though there will be a penalty in real estate, the gain for custom applications is a great increase in the number of available CMOS vendors.

The n+-Only Polysilicon Aproach

Both of the second-generation CMOS processes that follow are variants of the n+-only, selective-field-oxide approach. One closely resembles the p+ n+ Ubiquitous-P-Well process, since it, too, has a Ubiquitous P-Well that is implanted before the field oxidation and thus runs under the field oxide. The other, called isolated P-Well, has separate wells for each N-Channel device that are implanted after field oxidation.

Figure B.6 shows the section and plan views of the n+-only Ubiquitous-P-Well approach used to build the gate of Figure B.4. This is the 5μm process recommended by AMI and others for new, high-performance CMOS designs. The layout is simpler than with the n+/p+ polysilicon Ubiquitous-Well approach (there are no buried contacts and no polysilicon-diode contacts), and it occupies less area for the same line widths. Also, since the process permits implanting in the field region, no guard rings are required. Polysilicon can thus cross directly from P- to N-Channel device areas without the need for bridges or polysilicon-dioxide contacts.

Figure B.4. Crossection and Schematic Diagram of a CMOS Inverter

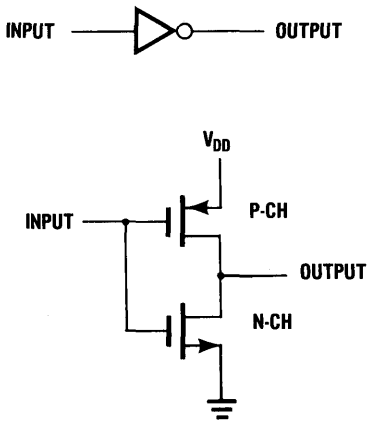
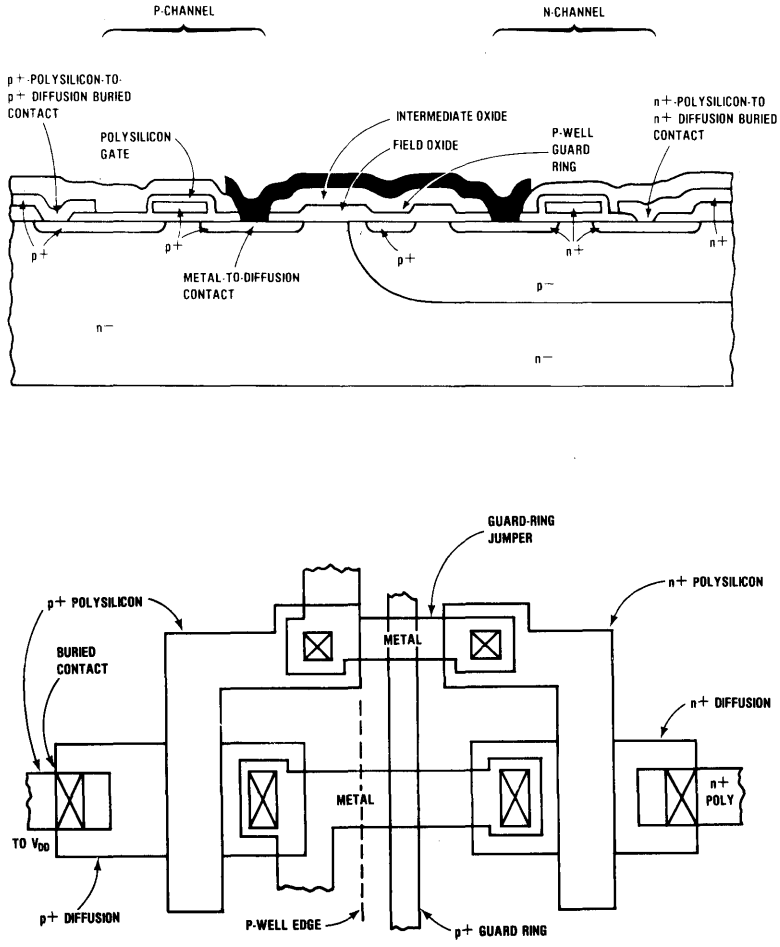
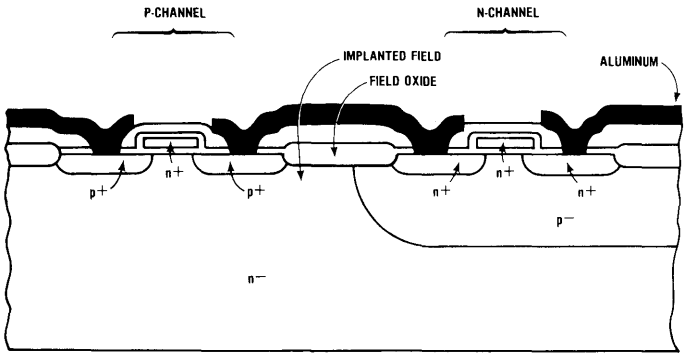


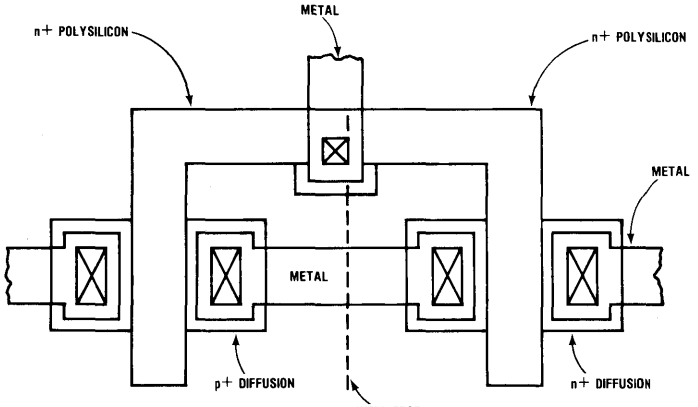
Figure B.5. n+/p+ Polysilicon Approach



THE FIRST HIGH-PERFORMANCE COMPLEMENTARY-MOS PLANAR PROCESS. ITS DRAWBACKS: TWO TYPES OF POLYSILICON ARE USED, AND THE UNAVAILABILITY OF FIELD IMPLANT DOPING TIES FIELD THRESHOLD TO DEVICE THRESHOLDS.

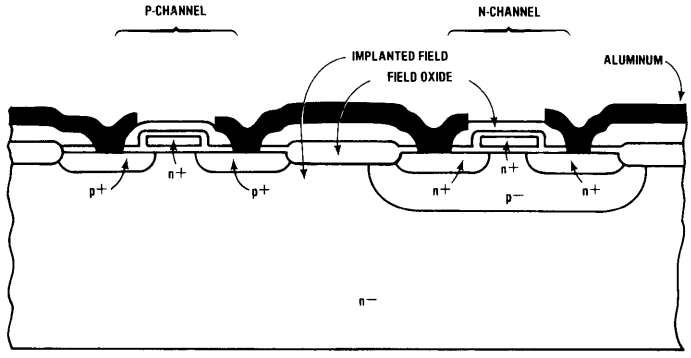
Figure B.6. n+-Only Polysilicon Approach

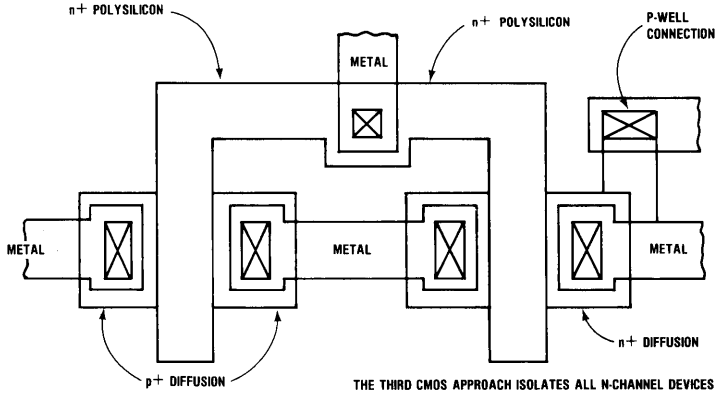




ALL NEW HIGH-PERFORMANCE CMOS CIRCUITS WILL USE ONE TYPE OF POLYSILICON. THIS VERSION HAS A UBIQUITOUS P-WELL: THAT IS, SERIES N-CHANNEL DEVICES SIT IN A COMMON P-WELL, WHICH, IMPLANTED REFORE FIELD OXIDATION, RUNS UNDER THE FIELD OXIDE. THIS IS AMI'S PREFERRED CMOS PROCESS FORMAT FOR ALL NEW DESIGNS.

Figure B.7. Isolated Wells.





THE THIRD CMOS APPROACH ISOLATES ALL N-CHANNEL DEVICES IN SEPARATE P-WELLS. SINCE THE ISOLATED WELLS MUST BE DOPED MUCH MORE HEAVILY THAN THOSE OF THE UBIQUITOUS-WELL APPROACH, n+-TO P-WELL CAPACITANCE IS GREATER AND SWITCHING SPEEDS LOWER. THIS IS AN n+-ONLY POLYSILICON PROCESS.

A variant of the all n+ (See Figure B.7) polysilicon process just discussed uses basically the selective field-oxide approach except that the P-Wells are not continuous under the field-oxide areas; they are instead bounded by field-oxide edges. Since the P-Wells are naturally isolated from one another, the process is called n+ poly-isolated P-Well. The isolated wells must all be connected to ground; if they are left floating, circuit malfunctions are bound to occur. The grounding is done either with p+ diffusions or with top-side metalization that covers a p+-to-P-Well contact diffusion.

In the Isolated-Well process, the P-Wells must be doped much more heavily than in the Ubiquitous-Well process. One result is a higher junction capacitance between the n+ areas and the wells that both slows switching speeds and raises the power dissipation of a device. Even though the speed loss could be compensated for by slightly shorter channel lengths, the operating power still remains high.

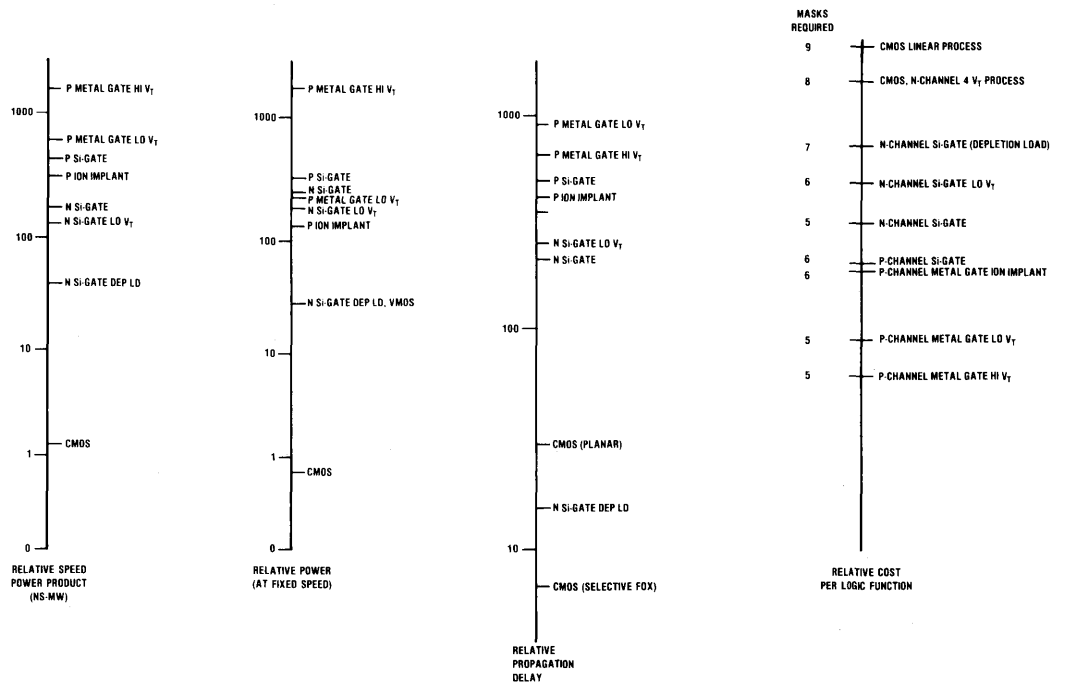
Although currently available from AMI and other manufacturers, the Isolated-Well process is in fact not recommended for new designs by AMI. Its layout takes up more area than does one using the Ubiquitous-Well approach, even though its P-Well to p+-area spacing is slightly less.

Table 1. Layout Compatibility Concerns for CMOS Processes

LAYOUT FEATURE	n+/p+ POLY-SILICON UBIQUITOUS P-WELL	n+-ONLY POLYSILICON UBIQUITOUS P-WELL	n+-ONLY POLY SILICON ISOLATED P-WELL
BURIED CONTACT	X	NO	NO
POLYSILICON DIODE CONTACT	YES	X	X
P-WELL ISOLATION WITH *DIFFUSION MASK*	NO	NO	YES
TIGHT P-WELL-TO-p+ SPACING	NO	NO	YES
LAYOUT CARE REQUIRED FOR P-WELL ELECTRICAL CONTACTS	NO	NO	YES

X = DOES NOT MATTER

Figure B.8. Comparative Data on Major MOS Processes



7.5 Micron CMOS Process Parameters

Parameter	Low V_T Min.	Low V_T Max.	High V_T Min.	High V_T Max.	Comments
V_{TN}	.55	.85	1.0	1.5	N-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TP}	−.4	−.95	−.8	−1.4	P-Channel Threshold at 1μA 50 x 7.5μ Device (Volts)
V_{TF}	8		15		Poly Field Threshold at 1μA 50 x 10μ Device (Volts)
B_{VDSS}	24	—	28	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	30	39	28	33	Diffusion Resistivity Ω/□
N+	9	15	9.1	12.6	Diffusion Resistivity Ω/□
R_{POLY} P+	118	172	80	140	Poly Resistivity Ω/□
N+	30	60	29	39	Poly Resistivity Ω/□
T_{OX}	1300		1200		Gate Oxide Thickness, In Angstroms
X_j P+	1.8*		1.8*		Junction Depth, In μ
N+	2.0*		2.0*		Junction Depth, In μ
Operating Voltage	—	5	5	12	In Volts
Max Rating	—	5.5	—	13.2	In Volts
Process Designator	CTA	CTA	CTE	CTE	

(*Typical)

CMOS I Process Parameters

	General Purpose				Double Poly				NAND ROM				
	High V		Low V		High V		Low V		High V		Low V		
Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Comments
V_{TN}	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	0.7	1.3	0.5	1.1	N-Channel Threshold 50 x 5μ Device (Volts)
V_{TP}	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	−0.7	−1.3	−0.5	−1.1	P-Channel Threshold 50 x 5μ Device (Volts)
V_{TF}	17	—	7	—	17	—	7	—	17	—	7	—	Poly Field Threshold (Volts)
B_{VDSS}	17	—	7	—	17	—	7	—	17	—	7	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	15	35	15	35	15	35	15	35	15	35	15	35	Diffusion Resistivity Ω/□
N+	35	80	35	80	35	80	35	80	35	80	35	80	Diffusion Resistivity Ω/□
R_{POLY}	15	45	15	45	15	45	15	45	15	45	15	45	Poly Resistivity Ω/□ (All poly is N+)
T_{OX}	750	850	750	850	750	850	750	850	750	850	750	850	Gate Oxide Thickness, In Angstroms
X_j P+	1.2*		1.2*		1.2*		1.2*		1.2*		1.2*		Junction Depth, In μ
N+	1.5*		1.5*		1.5*		1.5*		1.5*		1.5*		Junction Depth, In μ
Operating Voltage	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	2.2	13.2	1.5	5.5	In Volts
Max Rating	—	13.2	—	5.5	—	13.2	—	5.5	—	13.2	—	5.5	In Volts
Process Designator	CVA	CVA	CVH	CVH	CVB	CVB	CVE	CVE	CVD	CVD	CVC	CVC	

(*Typical)

CMOS II Process Parameters

Parameter	Single Metal Min.	Single Metal Max.	Double Metal Min.	Double Metal Max.	Comments
V_{TN}	0.6	1.0	0.6	1.0	N-Channel Threshold (Volts)
V_{TP}	−0.6	−1.0	−0.6	−1.0	P-Channel Threshold (Volts)
V_{TF}	10.0	—	10.0	—	Poly Field Threshold (Volts)
B_{VDSS}	10.0	—	10.0	—	Drain-Source Breakdown (Volts)
R_{DIFF} P+	35	80	35	80	Diffusion Resistivity Ω/□
N+	15	40	15	40	Diffusion Resistivity Ω/□
R_{POLY}	15	30	15	30	Poly Resistivity, Ω/□ (All Poly is N+)
T_{OX}	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j P+	0.3	0.5	0.3	0.5	Junction Depth, In μ
N+	0.3	0.5	0.3	0.5	Junction Depth, In μ
Operating Voltage	5.0	5.0	5.0	5.0	In Volts
Max Rating	—	5.5	—	5.5	In Volts
Process Designator	CCA	CCA	CCD	CCD	

6 & 5 Micron SiGate NMOS Process Parameters

	6 Micron						5 Micron		
	Low V_T		High V_T		16.67/Process Shrink				
Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Comments
V_{TE}	0.6	1.0	0.8	1.2	.75	1.25	0.6	1.0	Extrapolated Enhancement Threshold on a 50 x 6μ Transistor (Volts)
V_{TD}	−3.0	−4.0	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	Extrapolated Depletion Threshold on a 50 x 50μ Transistor (Volts)
V_{TN}	—	—	—	—	—	—	−.2	−.2	Intrinsic Device Threshold 50 x 6μ Transistor (Volts)
V_{TDD}	—	—	—	—	—	—	−4.35	−3.65	Deep Depletion Threshold (Volts)
V_{TF}	13	40	13	40	12	30	10	—	Poly Field Threshold (Volts)
B_{VDSS}	14	—	14	—	12	—	10	—	Drain-Source Breakdown on 50 x 50μ Transistor
R_{DIFF}	8	14	8	14	8	14	8	25	N+ Region Resistivity Ω/□
R_{POLY}	20	40	20	40	20	40	20	40	N+ Doped Poly Resistivity Ω/□
T_{OX}	1000	1150	1000	1150	750	850	750	850	Gate Oxide Thickness In Angstroms
X_j	1.2	1.6	1.2	1.6	0.8	1.2	0.8	1.2	Junction Depth, In μ
Operating Voltage	5	12	5	12	5	12	5	12	In Volts
Max Rating		13.2		13.2		13.2		13.2	In Volts
Process Designator	NVC	NVC	NVD	NVD	NVS	NVS	NEA/NEC		

NMOS I & NMOS II Process Parameters

	NMOS I				NMOS II				
	$4V_T$		Std.		$4V_T$		Std.		
Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Comments
V_{TE}	0.6	1.0	0.6	1.0	0.6	1.0	0.6	1.0	Extrapolated Enhancement Threshold Voltage on a 50 x 4μ Transistor (4μ Processes) or 50 x 3μ Transistor (3μ Processes) (Volts)
V_{TD}	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	−3.5	−2.5	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TN}	−0.15	+0.15	N/A	N/A	−0.15	+0.15	N/A	N/A	Extrapolated Threshold 50 x 6μ Device (Volts)
V_{TDD}	−4.35	−3.65	N/A	N/A	−4.85	−4.15	N/A	N/A	Extrapolated Threshold 50 x 50μ Device (Volts)
V_{TF}	7.5	—	7.5	—	7.5	—	7.5	—	Poly Field Threshold (Volts)
B_{VDSS}	7.5	—	7.5	—	7.5	—	7.5	—	Punch Through Voltage 50 x 4μ Device (4μ Processes) or 50 x 3μ Device (3μ Processes) (Volts)
R_{DIFF}	15	30	15	30	15	30	15	30	Diffusion Resistivity Ω/□
R_{POLY}	20	50	20	50	20	40	20	40	Poly Resistivity Ω/□
T_{OX}	650	750	650	750	450	550	450	550	Gate Oxide Thickness, In Angstroms
X_j	0.3	0.5	0.3	0.5	0.3	0.5	0.3	0.5	N+ Junction Depth, In μ
Operating Voltage	—	5/12	—	5/12	—	5	—	5	In Volts
Max Rating	—	5.5/13.2	—	5.5/13.2	—	5.5	—	5.5	In Volts
Process Designator	NDD	NDD	NDE	NDE	NCC	NCC	NCA	NCA	

7.5 Micron Metal Gate PMOS Process Parameters

	0 Implant						1 Implant		2 Implant		
	High V_T		Med V_T		Low V_T						
Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Comments
V_{TE}	−3.25	−4.95	−2.8	−4.2	−1.8	−2.5	−1.0	−1.8	−1.2	−2.0	$I_{DS} = 1\mu A$
V_{TD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	4.0	5.0	Depletion Measurement on a 50μ Transistor (Volts)
V_{TF}	30	—	25	—	17	—	25	—	25	—	Field Threshold (Volts)
B_{VDSS}	30	—	30	—	30	—	22	—	22	—	Drain-Source Breakdown (Volts)
R_{DIFF}	30	60	30	60	30	60	30	60	30	60	Sheet Resistivity Ω/□
I_{DS}/mA	1.25	2.55	0.8	2.2	0.8	2.0	2.8	4.0	2	4	Drain-Source Current (mA)
B_{VOXG}	120	—	80	—	100	—	90	—	90	—	Gate Oxide Breakdown (Volts)
X_j	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	1.7	1.9	Junction Depth, In μ
Process Designator	PMC	PMC	PMT	PMT	PMD	PMD	PNR	PNR	POG	POG	

INTRODUCTION

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions:

- ☐ Quality Control
- ☐ Quality Assurance
- ☐ Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program—Quality Control, Quality Assurance, and Reliability—have been developed as a result of many years of experience in MOS device design and manufacture.

Quality Control establishes that every method meets or fails to meet, processing or production standards—*QC checks methods.*

Quality Assurance establishes that every method meets, or fails to meet, product parameters—*QA checks results.*

Reliability establishes that QA and QC are effective—*Reliability checks device performance.*

One indication that the AMI Product Assurance Program has been effective is that NASA has endorsed AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated AMI circuits, and AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

QUALITY CONTROL

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- ☐ Incoming Materials Control
- ☐ Microlithography Control
- ☐ Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of AMI Quality Control:

- ☐ Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.
- ☐ Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photo-reduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, AMI generated or customer generated—the artwork is thoroughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must conform to stringent design rules, which have been developed over a period of years as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical N-Channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program—the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possibility of contamination or adverse effects due to temperature or humidity excesses.

Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the QC Fabrication Group, A QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking and evaporization are the most closely monitored steps.

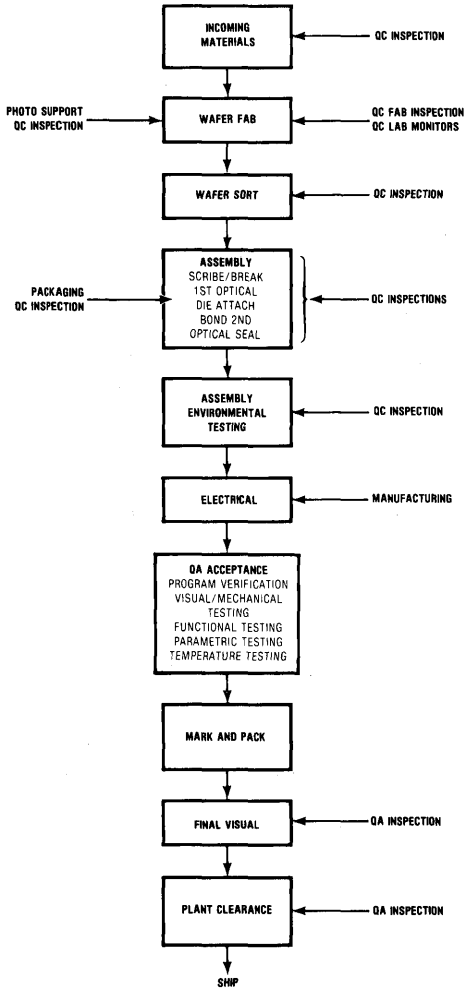
Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical Inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

QUALITY ASSURANCE

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA

Figure 1. Flowchart of Product Assurance Program Implementation



group also is responsible for calibration of all equipment, and for the maintenance of AMI internal product specifications, to assure that they are always in conformance with customer specifications or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing to a 0.1% AQL.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed if required by the specification.

To perform the tests, QA uses AMI PAFT test systems, ROM test systems, Macrodata testers, Fairchild *Sentry*, LTX *Sentinel*, *XINCOM* systems, Teradyne test systems, and various bench test units. In special instances a part may also be tested in a real life environment in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance but is identified as a resubmitted lot. If it fails again, corrective action in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts leave finished goods, they are again checked by the QA group to a 10% LTPD with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested by QA to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) Selected return samples are sent to Reliability for failure analysis.

RELIABILITY

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification and failure analysis. To perform these functions AMI Reliability group is organized into two major areas:

- ☐ Reliability Laboratory
- ☐ Failure Analysis

Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions.

- ☐ New Process Qualification
- ☐ Process Change Qualification
- ☐ Process Monitoring
- ☐ New Device Qualification
- ☐ Device Change Qualification
- ☐ New Package Qualification
- ☐ Device Monitoring
- ☐ Package Change Qualification
- ☐ Package Monitoring
- ☐ High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective, the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of a new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- ☐ A discrete inverter and an MOS capacitor
- ☐ A large P-N junction covered by an MOS capacitor.
- ☐ A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- ☐ A large area MOS capacitor over substrate
- ☐ Several long contact strings with different contact geometries
- ☐ Several long conductor geometries, which cross a series of eight deeply etched areas

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

Package Qualification

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

SUMMARY

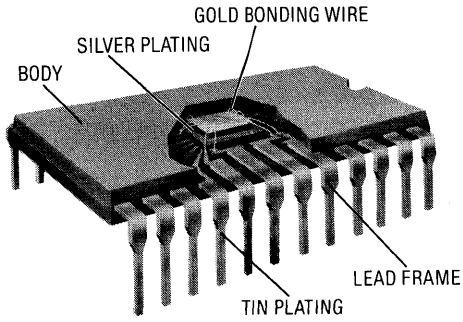
The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliable, with a very low reject level.

PLASTIC PACKAGE

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/LSI applications. The package consists of a plastic body, transfer-molded directly onto the assembled lead frame and die. The lead frame is Kovar or Alloy 42, with external pins tin plated. Internally, there is a 150μin. silver spot on the die attach pad and on each bonding fingertip. Gold bonding wire is attached with the thermosonic gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Available in: 8, 14, 16, 18, 22, 24, 28, 40 and 64 pin configurations.

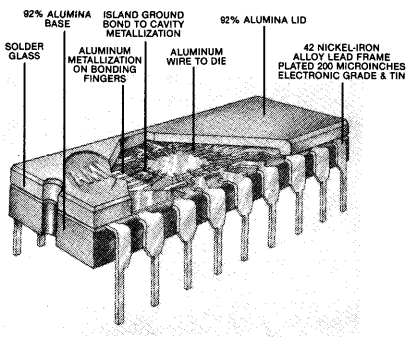


CERDIP PACKAGE

The Cerdip dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package yet is a cost-effective alternative. It is a military approved type package with excellent reliability characteristics.

The package consists of an Alumina (Al_2O_3 base and the same material lid, hermetically fused onto the base with low temperature solder glass.

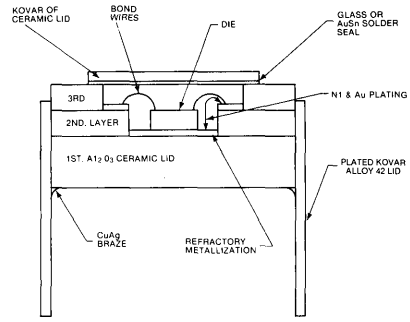
Available in 14, 16, 18, 20, 22, 24, 28 and 40 pin configurations.



CERAMIC PACKAGE

Industry standard high performance, high reliability package, made of three layers of AL_2O_3 ceramic and nickel-plated refractory metal. Either a low temperature glass sealed ceramic lid or a gold tin *eutectic* sealed Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold or tin plating for socket insertion or soldering.

Available in 14, 16, 18, 22, 24, 28 40 and 64 pin configurations.

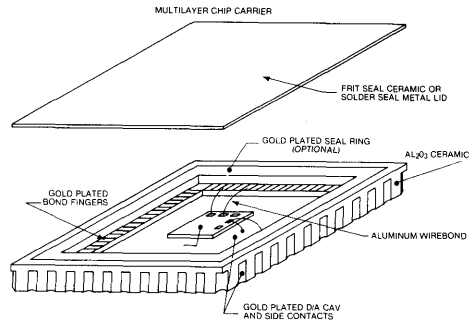


CHIP CARRIER PACKAGE

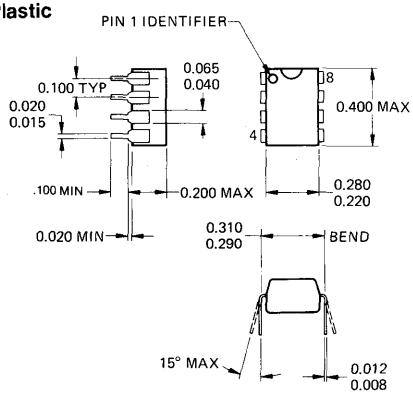
Chip carriers are the new industry standard in reducing package size. Built on the same concept as the highly reliable side-braze ceramic package, it is made of three layers of AL_2O_3 ceramic, refractory metallization and gold plating. The chip carrier also offers contact pads equally spaced on all four sides of the carrier resulting in increased package density, better electrical characteristics, and a more cost effective way of packaging IC devices.

The package comes with a gold tin *eutectic* sealed metal lid or the low cost glass sealed ceramic lid creating a standard hermetic cavity.

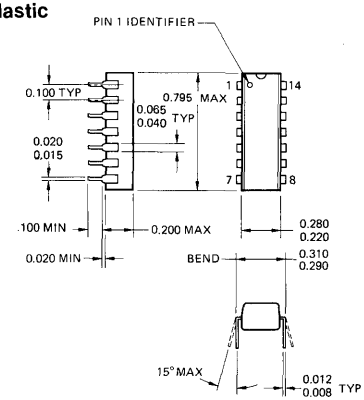
Available in 20, 24, 28, 40, 44, 68 and 84 LD standard 3-layer versions and 24, 28, 44 LD slam style on 50 mil center lines to the JEDEC standards.



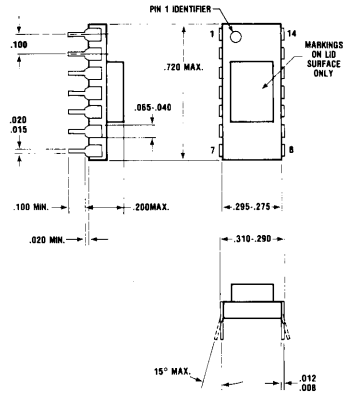
8-Pin Plastic



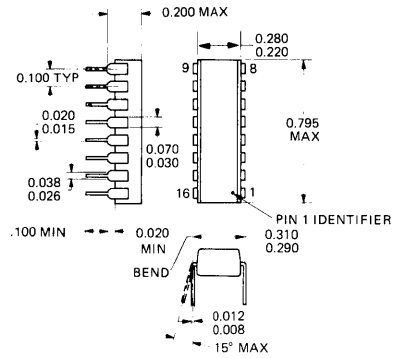
14-Pin Plastic



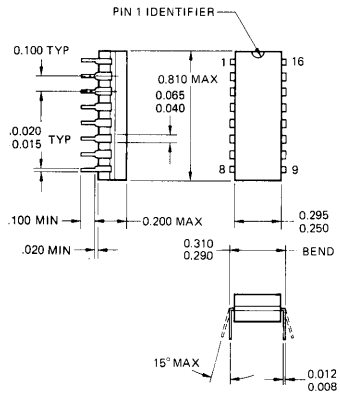
14-Pin Ceramic



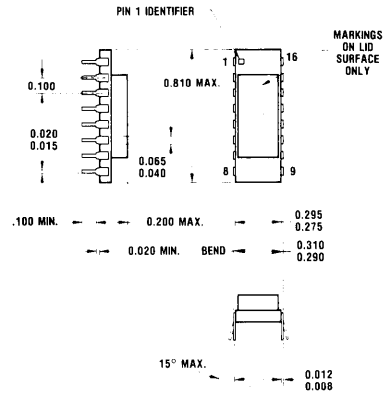
16-Pin Plastic



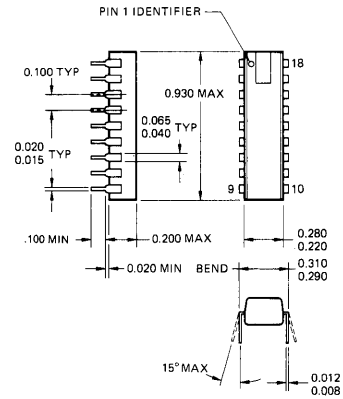
16-Pin Cerdip



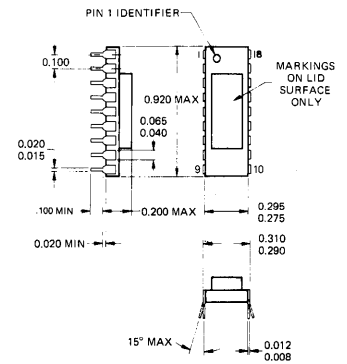
16-Pin Ceramic



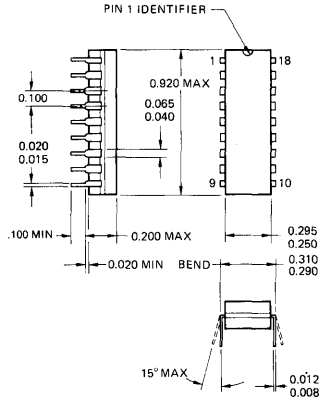
18-Pin Plastic



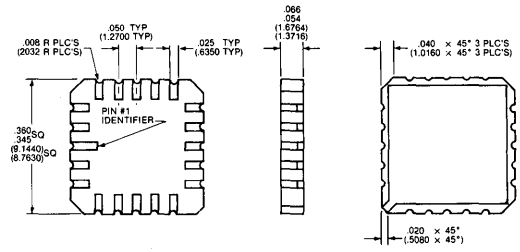
18-Pin Ceramic



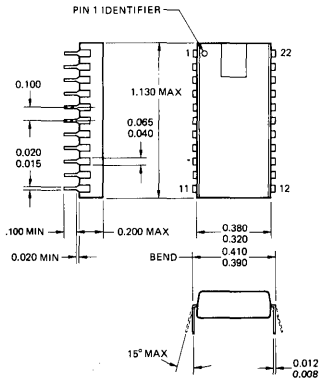
18-Pin Cerdip



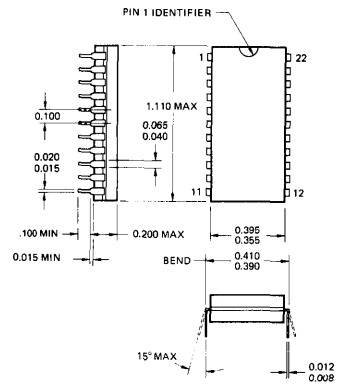
20-Lead Chip Carrier



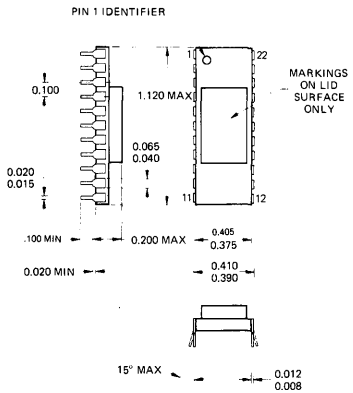
22-Pin Plastic



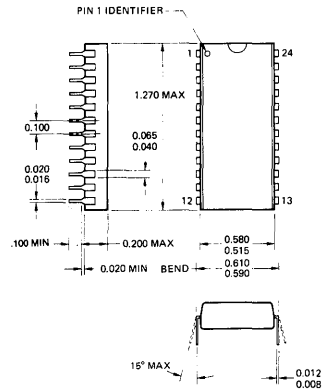
22-Pin Cerdip



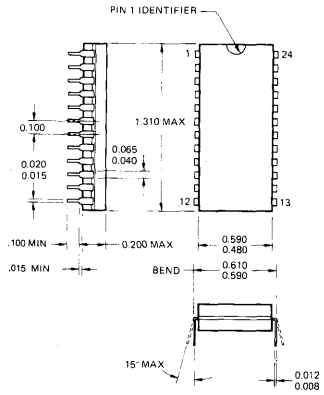
22-Pin Ceramic



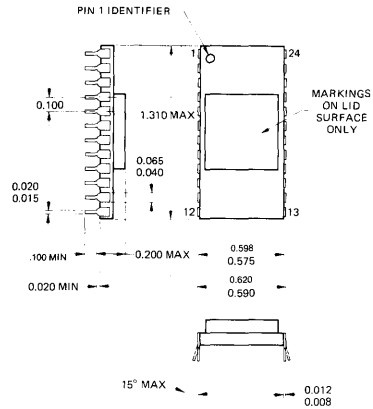
24-Pin Plastic



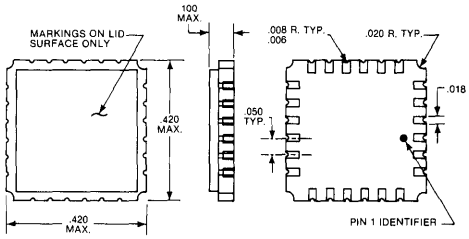
24-Pin Cerdip



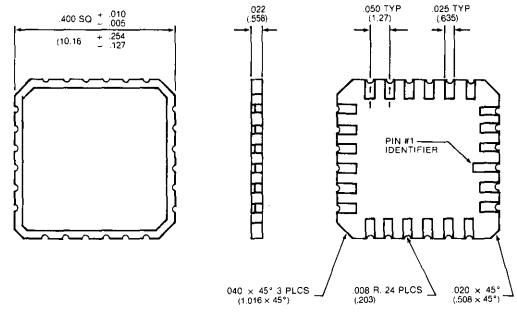
24-Pin Ceramic



24-Lead Chip Carrier

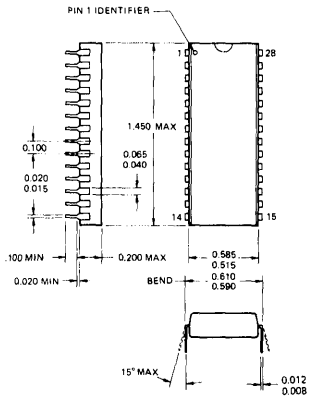


24-Lead Slam Chip Carrier

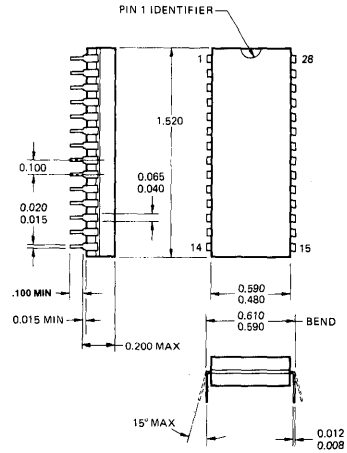


GENERAL INFORMATION

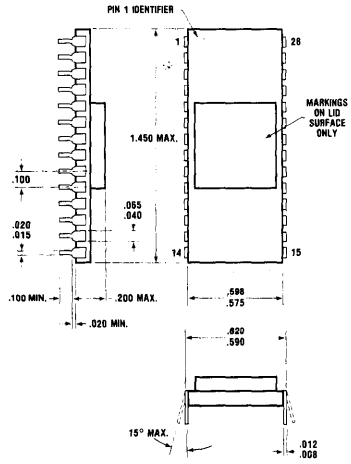
28-Pin Plastic



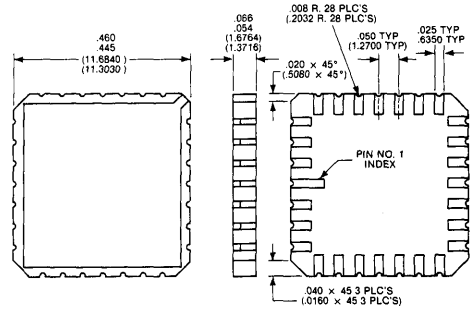
28-Pin Cerdip



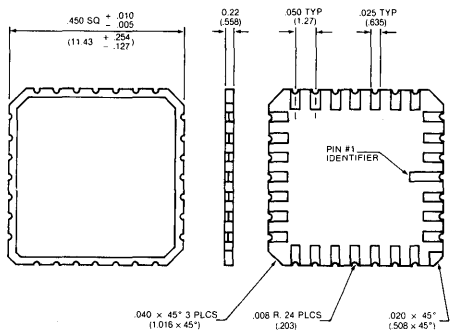
28-Pin Ceramic



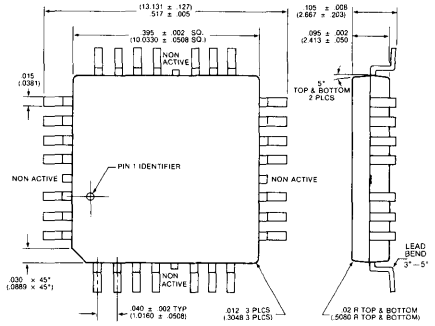
28-Lead Chip Carrier



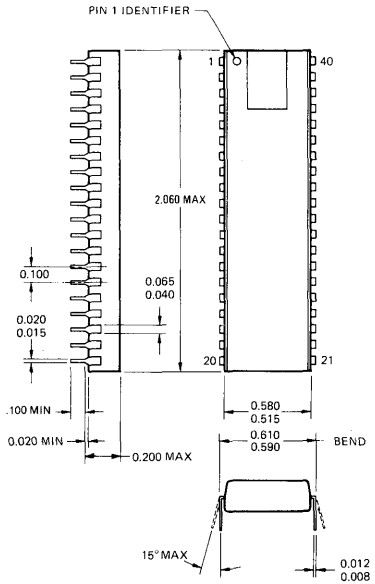
28-Lead Slam Chip Carrier



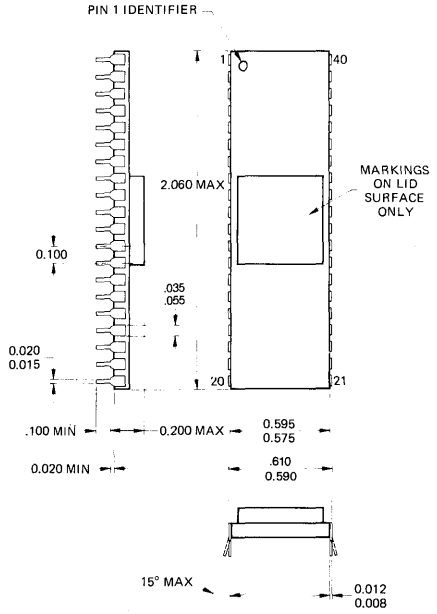
28 Lead Plastic Mini-Flat Package



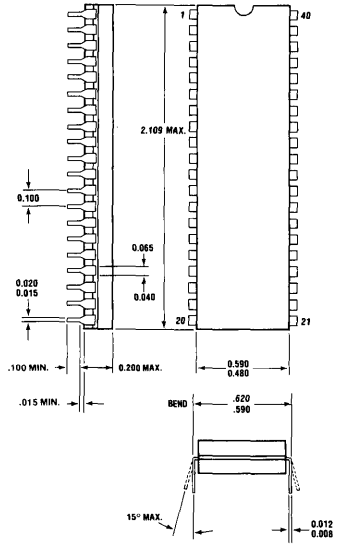
40-Pin Plastic



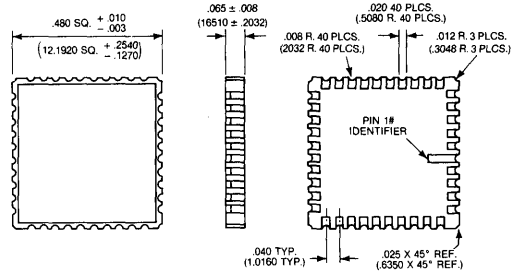
40-Pin Ceramic



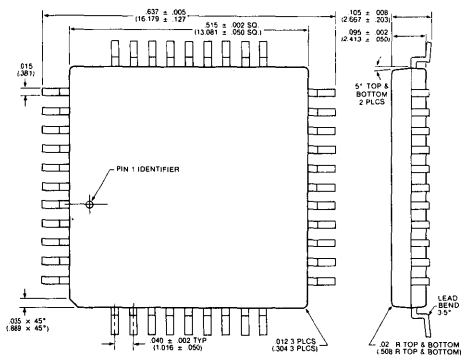
40-Pin Cerdip



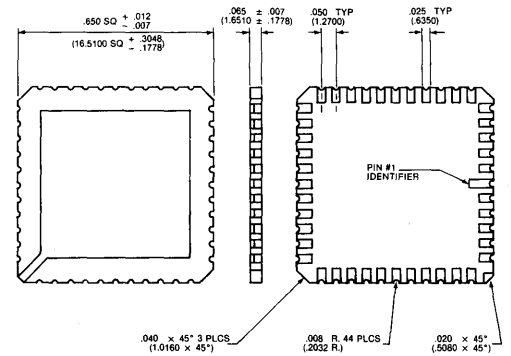
40-Lead Chip Carrier



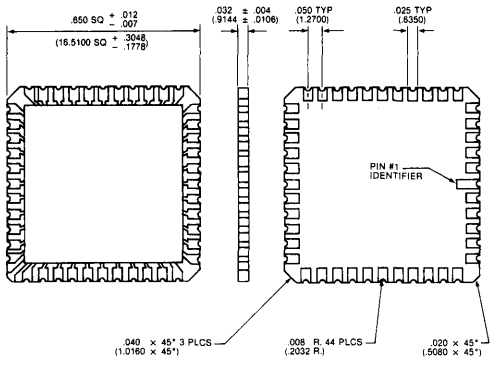
40 Lead Plastic Mini-Flat Package



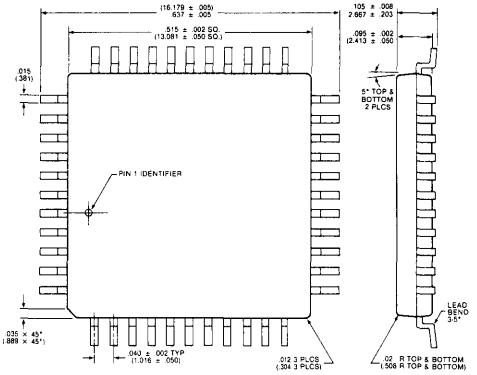
44-Lead Chip Carrier



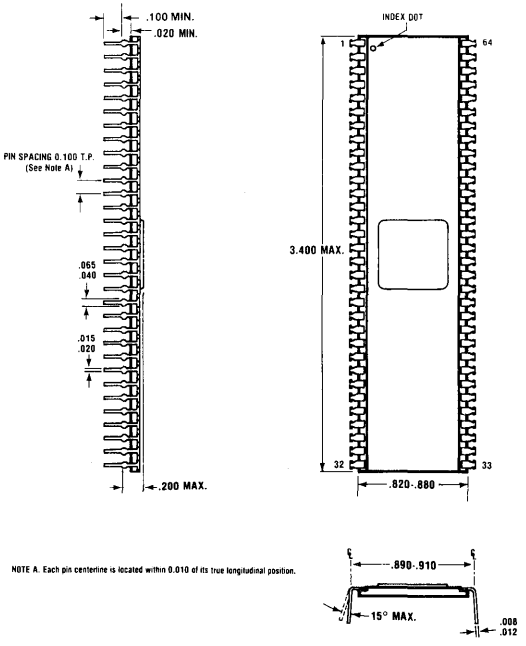
44-Lead Slam Chip Carrier



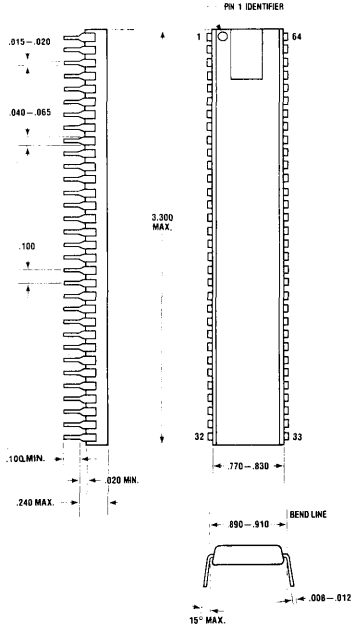
44 Lead Plastic Mini-Flat Package



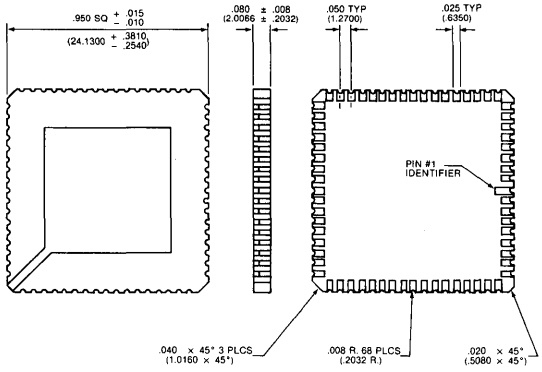
64-Pin Ceramic



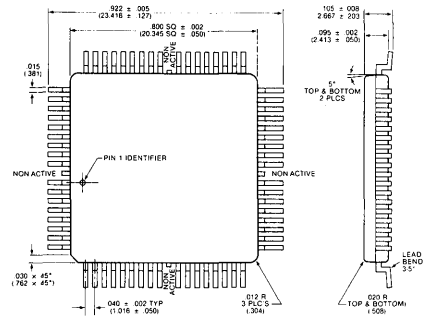
64-Pin Plastic



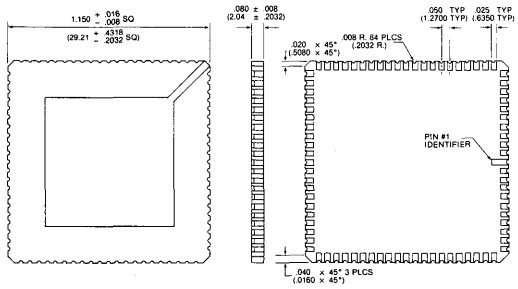
68-Lead Chip Carrier



68 Lead Plastic Mini-Flat Package



84-Lead Chip Carrier

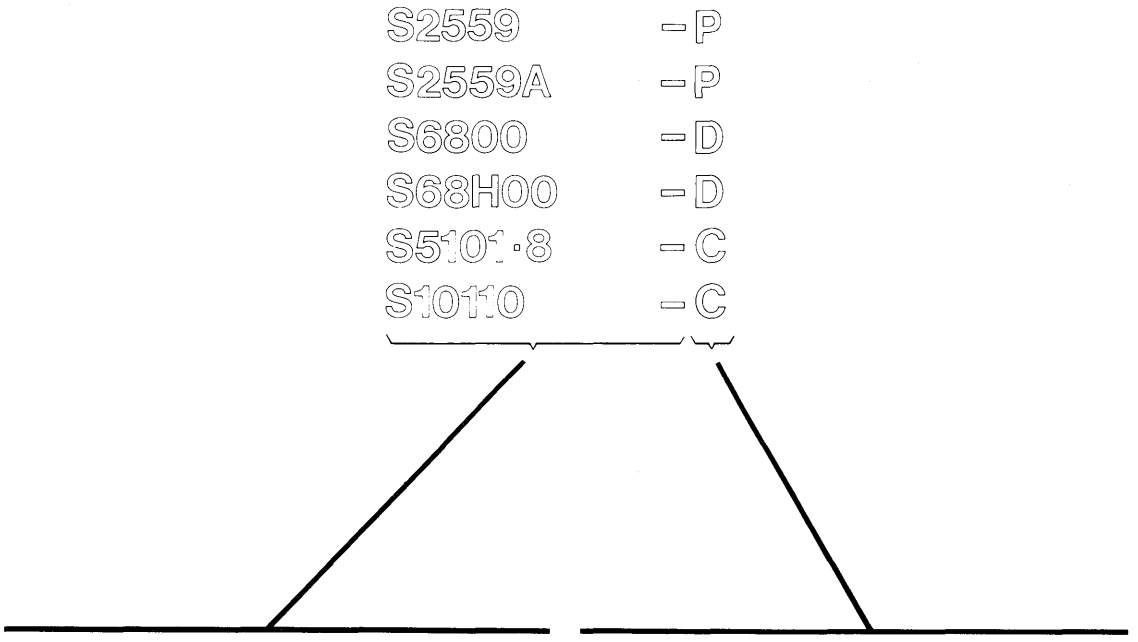


Standard Products:

Any product in this MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic carriers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.



Device Number — prefix S, followed by four (or five*) numeric digits that define the basic device type. Versions to the basic device are indicated by an additional alpha or numeric digit as shown in the above examples.

*Organ Circuits

Package Type — a single letter designation which identifies the basic package type. The letters are coded as follows:

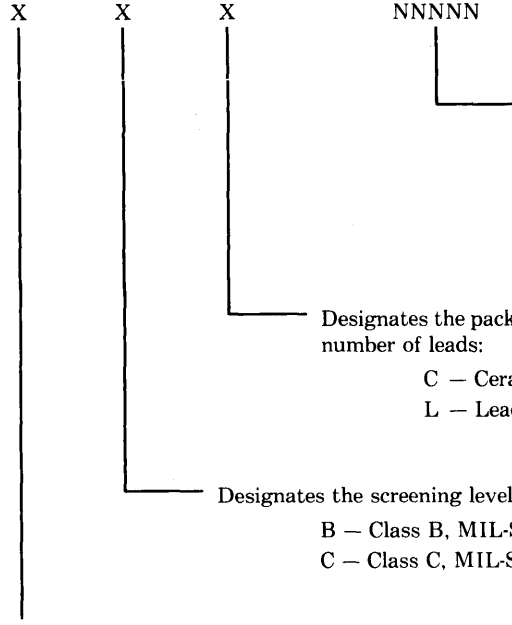
P — Plastic package

D — Cerdip package

C — Ceramic (three-layer) package

Military Products:

Parts Numbering Format



Examples
MBC 6802
LBC 68A00
MBL UA-3

Four to seven alpha numerics specifying the basic part number (die type) and including a power/speed selection as applicable. For example, 6802 indicates an 8-bit microprocessor with clock and RAM; 5101L-4 specifies a CMOS 256×4 static RAM with 0.055mW maximum standby power and 650ns maximum access time; and UA-3, a 540 gate CMOS uncommitted logic array.

Designates the package and utilizes one of the following letters regardless of the number of leads:

C — Ceramic dual in-line

L — Leadless chip carrier, ceramic, 50 mil pin spacing

Designates the screening level:

B — Class B, MIL-STD-883, Method 5004.5

C — Class C, MIL-STD-883, Method 5004.5

Designates the operating temperature range and utilizes one of the letters M or L. Definitions:

M — Full military temperature range, −55°C to +125°C

L — Limited military temperature range, −55°C to +85°C

Ordering Information

Please specify part numbers in accordance with the parts numbering format above.

TERMS OF SALE

OCTOBER 1982

1. ACCEPTANCE: THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. PAYMENT:

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. TAXES: Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. F.O.B. POINT: All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. DELIVERY: Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. PATENTS: The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. INSPECTION: Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. LIMITED WARRANTY: The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. PRODUCTS NOT WARRANTED BY SELLER: The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. PRICE ADJUSTMENTS: Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. VARIATION IN QUANTITY: If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. CONSEQUENTIAL DAMAGES: In no event shall Seller be liable for special, incidental or consequential damages.

13. GENERAL:

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder".

(h) Buyer, by accepting these products, certifies that he will not export or re-export the products furnished hereunder unless he complies fully with all laws and regulations of the United States relating to such export or re-export, including but not limited to the Export Administration Act of 1979 and the Export Administration Regulations of the U.S. Department of Commerce.

14. GOVERNMENT CONTRACT PROVISIONS: If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Defense Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

Worldwide Sales Offices

UNITED STATES

Northwest Region

HEADQUARTERS—3800 Homestead Road, Santa Clara, California 95051 ..... (408) 246-0330
TWX: 910-338-0018
or 910-338-0024
CALIFORNIA, 2960 Gordon Avenue, Santa Clara 95051 ..... (408) 738-4151
WASHINGTON, 20709 N.E. 232nd Avenue, Battle Ground 98604 ..... (206) 687-3101

Southwest Region

CALIFORNIA, 1451 Quail Street, Suite 208, Newport Beach 92660 ..... (714) 851-5931
ARIZONA, 5617 E. Waltann Lane, Scottsdale 85254 ..... (602) 996-5638

Central Region

ILLINOIS, 500 Higgins Road, Suite 210, Elk Grove Village 60007 ..... (312) 437-6496
MICHIGAN, 29200 Vassar Avenue, Suite 221, Livonia 48152 ..... (313) 478-4220
COLORADO, 7346A So. Alton Way, Englewood 80112 ..... (303) 694-0629

Southeastern Region

FLORIDA, 139 Whooping Loop, Altamonte Springs 32701 ..... (305) 830-8889
NORTH CAROLINA, 5711 Six Forks Road, Suite 210, Raleigh 27609 ..... (919) 847-9468
TEXAS, 725 South Central Expressway, Suite A-9, Richardson 75080 ..... (214) 231-5721
(214) 231-5285

Mid-Atlantic Area

PENNSYLVANIA, Axewood East, Butler & Skippack Pikes, Suite 230, Ambler 19002 ..... (215) 643-0217
INDIANA, 408 South 9th Street, Suite 201, Noblesville 46060 ..... (317) 773-6330
OHIO, 100 East Wilson Bridge Road, Suite 225, Worthington 43085 ..... (614) 436-0330

Northeastern Region

NEW YORK, 20F Robert Pitt Drive, Suite 208, Monsey 10952 ..... (914) 352-5333
MASSACHUSETTS, 24 Muzzey Street, Lexington 02173 ..... (617) 861-6530

INTERNATIONAL

ENGLAND, AMI Microsystems, Ltd., Princes House, Princes St., Swindon SN1 2HU ..... (0793) 37852
FRANCE, AMI Microsystems, S.A.R.L., 124 Avenue de Paris, 94300 Vincennes ..... (01) 374 00 90
WEST GERMANY, AMI Microsystems GmbH, Suite 237, Rosenheimer Strasse 30/32, 8000 Munich 80 ... (089) 483081
AUSTRIA, Austria Microsystems International GmbH, Schloss Premstätten
8141 Unterpremstätten, Graz, Vienna ..... (43) 3136/3666
ITALY, AMI Microsystems, S.p.A., Piazza Gobetti 12, Milano 20131 ..... (02) 293745
JAPAN, AMI Japan Ltd., 502 Nikko Sanno Building 2-5-3, Akasaka, Minato-ku, Tokyo 107 ..... (3) 586-8131

Domestic Representatives

ALABAMA, Huntsville	Rep, Inc.	(205) 881-9270
CANADA, Mississauga, Ontario	Vitel Electronics	(416) 245-8528
CANADA, Ottowa, Ontario	Vitel Electronics	(613) 836-1776
CANADA, Quebec, Quebec	Vitel Electronics	(514) 331-7393
GEORGIA, Tucker	Rep, Inc.	(404) 938-4358
ILLINOIS Elk Grove Village	Oasis Sales	(312) 640-1850
INDIANA, Fort Wayne	Giesting & Associates	(219) 486-1912
INDIANA, Indianapolis	Giesting & Associates	(317) 263-0005
IOWA, Cedar Rapids	Comstrand, Inc.	(319) 377-1575
KANSAS, Overland Park	Kebco, Inc.	(913) 649-1051
KANSAS, Wichita	Kebco, Inc.	(316) 733-1301
MARYLAND, Rockville	Mechtronics Sales	(301) 340-2130
MASSACHUSETTS, Burlington	Electronic Tech. Sales, Inc	(617) 272-5610
MICHIGAN, Coloma	Giesting & Associates	(616) 468-4200
MICHIGAN, Northville	Giesting & Associates	(313) 348-3811
MINNESOTA, Minneapolis	Comstrand, Inc.	(612) 788-9234
MISSOURI, Blue Springs	Kebco, Inc.	(816) 229-3370
MISSOURI, Maryland Heights	Kebco, Inc.	(314) 576-4111
NEW HAMPSHIRE, Nashua	Comp Tech, Inc.	(603) 883-9380
NEW YORK, Clinton	Advanced Components	(315) 853-6438
NEW YORK, Endicott	Advanced Components	(607) 785-3191
NEW YORK, North Syracuse	Advanced Components	(315) 699-2671
NEW YORK, Rochester	Advanced Components	(716) 544-7017
NEW YORK, Scottsville	Advanced Components	(716) 889-1429
NORTH CAROLINA, Raleigh	Rep, Inc.	(919) 851-3007
OHIO, Cincinnati	Giesting & Associates	(513) 521-8800
OHIO, Cleveland	Giesting & Associates	(216) 431-4241
OHIO, Dayton	Giesting & Associates	(513) 293-4044
OHIO, Galion	Giesting & Associates	(419) 468-3737
OKLAHOMA, Oklahoma City	Ammon & Rizos	(405) 942-2552
OREGON, Beaverton	SD-R^2	(503) 641-7377
PUERTO RICO, San Juan	Electronic Tech. Sales, Inc.	(809) 780-8259
TEXAS, Austin	Ammon & Rizos	(901) 874-1369
TEXAS, Dallas	Ammon & Rizos	(214) 233-5591
TEXAS, Houston	Ammon & Rizos	(713) 781-6240
TENNESSEE, Jefferson City	Rep, Inc.	(615) 475-4105
WASHINGTON, Bellevue	SD-R^2 Products & Sales	(206) 747-9424 (206) 624-2621
WISCONSIN, Brookfield	Oasis Sales	(414) 782-6660

Domestic Distributors

ARIZONA, Phoenix	Kierulff Electronics	(602) 243-4101
ARIZONA, Scottsdale	Western Microtechnology	(602) 948-4240
ARIZONA, Tempe	Anthem Electronics	(602) 244-0900
ARIZONA, Tucson	Kierulff Electronics	(602) 624-9986
CALIFORNIA, Canoga Park	Schweber Electronics	(213) 999-4702
CALIFORNIA, Chatsworth	Anthem Electronics	(213) 700-1000
CALIFORNIA, Chatsworth	Arrow Electronics	(213) 701-7500
CALIFORNIA, Cupertino	Western Microtechnology	(408) 725-1660
CALIFORNIA, Irvine	Schweber Electronics	(714) 556-3880
CALIFORNIA, Los Angeles	Kierulff Electronics	(213) 725-0325
CALIFORNIA, Newport Beach	Arrow Electronics	(714) 851-8961
CALIFORNIA, Palo Alto	Kierulff Electronics	(415) 968-6292
CALIFORNIA, San Diego	Anthem Electronics	(714) 279-5200
CALIFORNIA, San Diego	Arrow Electronics	(714) 565-4800
CALIFORNIA, San Diego	Kierulff Electronics	(714) 278-2112
CALIFORNIA, San Jose	Anthem Electronics	(408) 946-8000
CALIFORNIA, Santa Clara	Schweber Electronics	(408) 748-4700
CALIFORNIA, Sunnyvale	Arrow Electronics	(408) 745-6600
CALIFORNIA, Tustin	Anthem Electronics	(714) 730-8000
CALIFORNIA, Tustin	Kierulff Electronics	(714) 731-5711
CANADA, Alberta, Calgary	Future Electronics	(403) 259-6408
CANADA, British Columbia, Vancouver	Future Electronics, Inc.	(604) 438-5545
CANADA, Ontario, Downsview	Cesco Electronics, Ltd.	(416) 661-0220

Domestic Distributors (Continued)

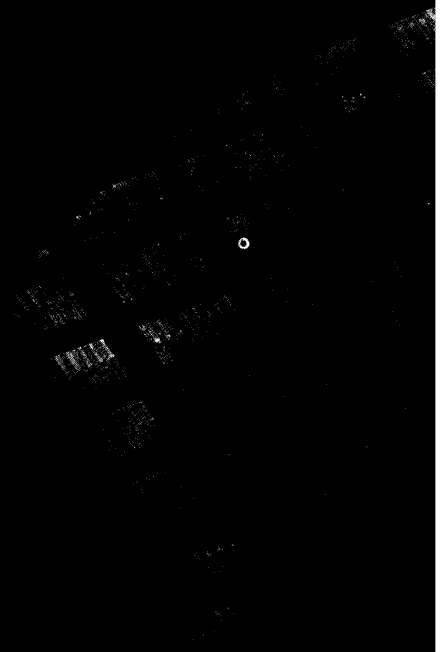
CANADA, Ontario, Downsview	Future Electronics, Inc.	(416) 663-5563
CANADA, Ottawa	Future Electronics, Inc.	(613) 820-8313
CANADA, Quebec, Montreal	Cesco Electronics, Ltd.	(514) 735-5511
CANADA, Quebec, Montreal	Future Electronics, Inc.	(514) 694-7710
CANADA, Quebec, Point Claire	Future Electronics, Inc.	(514) 694-7710
CANADA, Quebec	Cesco Electronics, Ltd.	(418) 687-4231
COLORADO, Denver	Arrow Electronics	(303) 758-2100
COLORADO, Denver	Kierulff Electronics	(303) 371-6500
CONNECTICUT, Danbury	Schweber Electronics	(203) 792-3742
CONNECTICUT, Wallingford	Arrow Electronics	(203) 265-7741
CONNECTICUT, Wallingford	Kierulff Electronics	(203) 265-1115
FLORIDA, Ft. Lauderdale	Arrow Electronics	(305) 776-7790
FLORIDA, Ft. Lauderdale	Kierulff Electronics	
FLORIDA, Hollywood	Schweber Electronics	(305) 927-0511
FLORIDA, Palm Bay	Arrow Electronics	(305) 725-1480
FLORIDA, St. Petersburg	Kierulff Electronics	(813) 576-1966
GEORGIA, Norcross	Arrow Electronics	(404) 449-8252
GEORGIA, Norcross	Kierulff Electronics	
GEORGIA, Norcross	Schweber Electronics	(404) 449-9170
ILLINOIS, Elk Grove Village	Kierulff Electronics	(312) 640-0200
ILLINOIS, Elk Grove Village	Schweber Electronics	(312) 364-3750
ILLINOIS, Schaumburg	Arrow Electronics	(312) 893-9420
INDIANA, Indianapolis	Arrow Electronics	(317) 243-9353
MARYLAND, Baltimore	Arrow Electronics	(301) 247-5200
MARYLAND, Baltimore	Kierulff Electronics	(301) 247-5020
MARYLAND, Gaithersburg	Schweber Electronics	(301) 840-5900
MASSACHUSETTS, Bedford	Schweber Electronics	(617) 275-5100
MASSACHUSETTS, Billerica	Kierulff Electronics	(617) 935-5134
MASSACHUSETTS, Woburn	Arrow Electronics	(617) 933-8130
MICHIGAN, Ann Arbor	Arrow Electronics	(313) 971-8220
MICHIGAN, Livonia	Schweber Electronics	(313) 525-8100
MINNESOTA, Eden Prairie	Schweber Electronics	(612) 941-5280
MINNESOTA, Edina	Arrow Electronics	(612) 830-1800
MINNESOTA, Edina	Kierulff Electronics	(612) 941-7500
MISSOURI, Earth City	Scheweber	(314) 739-0526
MISSOURI, Maryland Heights	Kierulff Electronics	(314) 739-0855
MISSOURI, St. Louis	Arrow Electronics	(314) 567-6888
LONG ISLAND, Westbury	Schweber Electronics	(516) 334-7474
NEW HAMPSHIRE, Manchester	Arrow Electronics	(603) 668-6968
NEW JERSEY, Fairfield	Arrow Electronics	(201) 575-5300
NEW JERSEY, Fairfield	Kierulff Electronics	(201) 575-6750
NEW JERSEY, Fairfield	Schweber Electronics	(201) 227-7880
NEW JERSEY, Moorestown	Arrow Electronics	(609) 235-1900
NEW MEXICO, Albuquerque	Arrow Electronics	(505) 243-4566
NEW YORK, Farmingdale	Arrow Electronics	(516) 293-6363
NEW YORK, Farmingdale	Arrow Electronics	(516) 694-6800
NEW YORK, Hauppauge	Arrow Electronics	(516) 231-1000
NEW YORK, Liverpool	Arrow Electronics	(315) 652-1000
NEW YORK, Rochester	Arrow Electronics	(716) 275-0300
NEW YORK, Rochester	Schweber Electronics	(716) 424-2222
NEW YORK, Westbury	Schweber Electronics	(516) 334-7474
NORTH CAROLINA, Greensboro	Kierulff Electronics	(919) 852-9440
NORTH CAROLINA, Raleigh	Schweber Electronics	
NORTH CAROLINA, Winston Salem	Arrow Electronics	(919) 725-8711
OHIO, Beachwood	Schweber Electronics	(216) 464-2970
OHIO, Centerville	Arrow Electronics	(513) 435-5563
OHIO, Cleveland	Kierulff Electronics	(216) 587-6558
OHIO, Columbus	Arrow Electronics	(614) 885-8362
OHIO, Solon	Arrow Electronics	(216) 248-3990
OKLAHOMA, Tulsa	Arrow Electronics	(918) 665-7700
OKLAHOMA, Tulsa	Kierulff Electronics	(918) 352-7537
OREGON, Portland	Kierulff Electronics	(503) 641-9150
PENNSYLVANIA, Horsham	Schweber Electronics	(215) 441-0600
PENNSYLVANIA, Monroeville	Arrow Electronics	(412) 856-7000

Domestic Distributors (Continued)

TEXAS, Austin	Kierulff Electronics	(512) 835-2090
TEXAS, Austin	Schweber Electronics	(512) 458-8253
TEXAS, Dallas	Arrow Electronics	(214) 386-7500
TEXAS, Dallas	Kierulff Electronics	(800) 442-1041
TEXAS, Dallas	Schweber Electronics	(214) 661-5010
TEXAS, Houston	Kierulff Electronics	(713) 530-7030
TEXAS, Houston	Schweber Electronics	(713) 784-3600
TEXAS, Stafford	Arrow Electronics	(713) 491-4100
UTAH, Salt Lake City	Kierulff Electronics	(801) 973-6913
WASHINGTON, Bellevue	Arrow Electronics	(206) 643-4800
WASHINGTON, Tukwila	Kierulff Electronics	(206) 575-4420
WISCONSIN, Madison	Arrow Electronics	(608) 273-4977
WISCONSIN, Oak Creek	Arrow Electronics	(414) 764-6600
WISCONSIN, Waukesha	Kierulff Electronics	(414) 784-8160

International Representatives and Distributors

ARGENTINA, Buenos Aires	YEL S.R.L.	46 2211
AUSTRIA, Vienna	PCS Handelsgesellschaft	(222) 627197
AUSTRALIA, New South Wales	Crosshouse	
AUSTRALIA, Preston, Victoria	Rifa Pty. Ltd.	(03) 480 1211
BELGIUM, Brussels	Betea Automation	(02) 7368050
BRAZIL, Sao Paulo	Datatronix Electronica Ltda.	11-826-0111
CHILI	Victronics Ltda.	36440-30237
ENGLAND, Derby	Quarndon Electronics Ltd.	(0332) 32651
ENGLAND, West Drayton Mtddx	Semiconductor Specialists	(08954) 46415/7
ENGLAND, Greater Manchester	Vako Electronics Ltd.	(061) 652-6316
ENGLAND, Harlow, Essex	VSI Electronics (UK) Ltd.	(0279) 2935477
FINLAND, Espoo	OY Atomica AB	(80) 423533
FRANCE, Montrouge	Produits Electronique	(01) 7353320
FRANCE, Sevres	Tekelec Airtronic	(01) 534-75-35
HONG KONG, Kowloon	Electrocon Products Ltd.	3-687214-6
INDIA	Semiconductor Complex Ltd.	87495
ISRAEL, Tel Aviv	Eldis Electronics, Ltd.	
ITALY, Milano	Mesa SpA	(02) 434333
ITALY, Roma	C.I.D. s.r.l.	(06) 63-83979
JAPAN, Tokyo	Kyobuto Boeki Kaisha, Ltd.	
JAPAN, Tokyo	Logic Systems International, Ltd.	
JAPAN, Tokyo	Logic House, Inc.	
JAPAN, Tokyo	Taiyo Electric Co.	(03) 379-2926
MEXICO	Dicopel S.A.	(905) 561-3211 (905) 687-1800
NETHERLANDS, Badhoevedere	Techmation Elec. NV	(02968) 6451
NETHERLANDS, Rotterdam	DMA Nederland, BV	010-361288
NEW ZEALAND, Auckland	David P. Reid (NZ) Ltd.	791-2612
SINGAPORE, Singapore	Dynamar Int'l. Ltd.	746 6188
SOUTH AFRICA, Transvaal	Radiokom Pty, Ltd.	(011) 485712
SOUTH KOREA, Seoul	Kortronics Enterprise	Seoul-634-5497
SPAIN, Barcelona	Interface S.A.	(03) 3017851
SWEDEN, Spanga	A.B. Rifa	(08) 7522500
SWITZERLAND, Zurich	W. Moor AG	(01) 8406644
TAIWAN, Taipai	Promotor Co., Ltd.	(02) 536-4057
WEST GERMANY, Berlin	Aktiv Elektronik GmbH	(030) 6845088
WEST GERMANY, Frankenthal	Gleichman	
WEST GERMANY, Hamburg	Microscan GmbH	
WEST GERMANY, Nettetal	Onmi-Ray GmbH	(02153) 7961
WEST GERMANY, Stuttgart	Ditronic GmbH	0711/724844
WEST GERMANY, Stuttgart	Mikrotec GmbH	(0711) 616036
WEST GERMANY, Viersen	Mostron Halbleitervertriebs	(0216) 17024
YUGOSLAVIA, Ljubljana	ISKRA/Standard/Iskra IEZE	(051) 551-353



AMI
American Microsystems, Inc.
A Subsidiary of Gould Inc.
3800 Homestead Rd., Santa Clara CA 95051
Telephone: (408) 246-0330
TWX: 910-338-0018