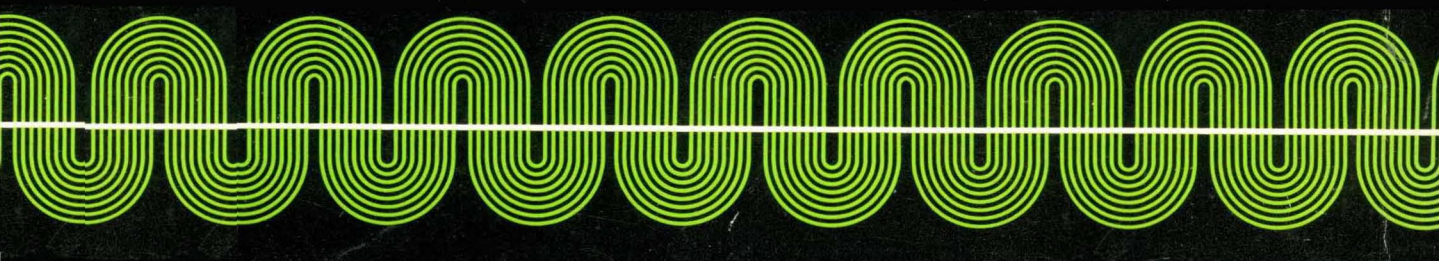
Telecommunications Design Manual

AMI

A Subsidiary of Gould Inc.

Telecommunications Design Manual



AMI

Telecommunications Design Manual

Telephone Products
Codecs
Signal Processors
Filter Products
Speech Synthesizers
Custom Circuit Design

AMERICAN MICROSYSTEMS, INC.
3800 HOMESTEAD ROAD, SANTA CLARA, CA 95051
PHONE: (408) 246-0330

Information furnished by AMI in this publication is believed to be accurate. Devices sold by AMI are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. AMI makes no warranty, express, statutory,implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. AMI makes no warranty of merchantability or fitness for any purposes. AMI reserves the right to discontinue production and change specifications and prices at any time and without notice.

Advanced Product Description means that this product has not been produced in volume, the specifications are preliminary and subject to change, and device characterization has not been done. Therefore, prior to programming or designing this product into a system, it is necessary to check with AMI for current information.

Preliminary means that this product is in limited production, the specifications are preliminary and subject to change. Therefore, prior to programming or designing this product into a system, it is necessary to check with AMI for current information.

This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically *not* recommended without additional processing by AMI for such application.

1st Revision - August 1982

AMERICAN MICROSYSTEMS, INC.

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AMERICAN MICROSYSTEMS, INC.

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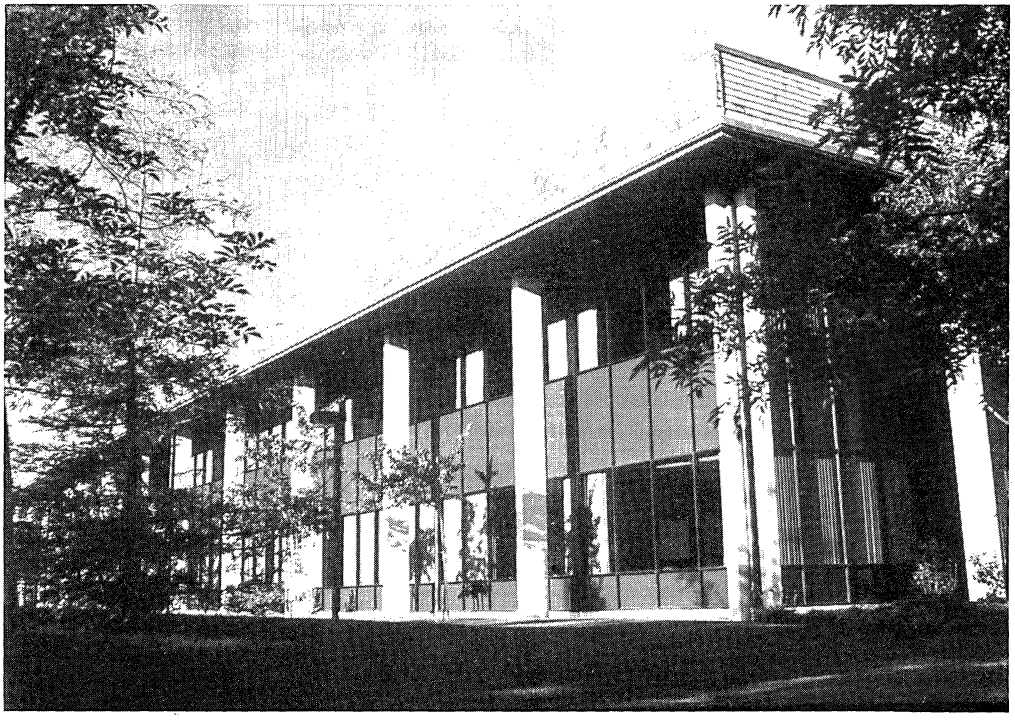
AMERICAN MICROSYSTEMS, INC.

Section 1.0

Introduction to AMI

The Company

Founded in 1966, AMI was the first commercial manufacturer of metal-oxide-silicon, large-scale-integrated (MOS/LSI) circuits. Today, AMI is an international company with design facilities in Santa Clara (California), Pocatello (Idaho) and Swindon (England), and sales offices throughout the United States, Europe and the Far East. The major manufacturing facility is in Pocatello and assembly is done at AMI facilities in Korea and the Philippines.



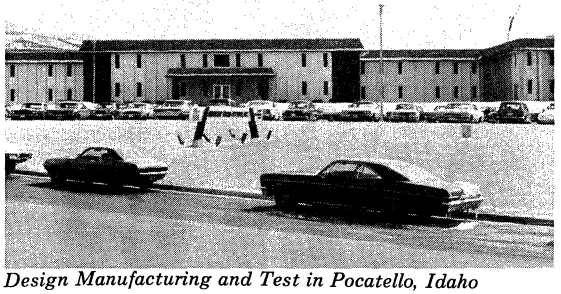
Headquarters in Santa Clara, California including Telecom Design, Manufacturing, Test, and Administration

The Capability

AMI, from its origination, has concentrated on the design of custom circuits that created new markets for MOS/LSI. This dedication has earned the company its position as the leader in custom MOS/LSI. AMI has designed more than 1500 LSI circuits for telecommunications, electronic data processing, consumer products and the automotive industry.

In addition, AMI has become a significant producer of custom-synergistic standard MOS circuits. These circuits fill select niches in the market where our experience as a custom house gives us market advantages. AMI standard products are concentrated in the areas of telecommunication circuits, ROM's, microcomputers, microprocessors and Uncommitted Logic Arrays (ULAs).

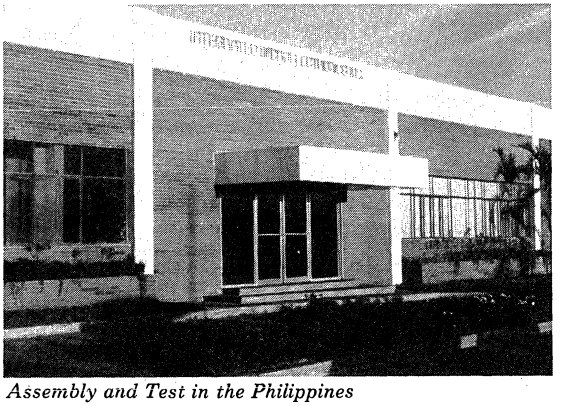
AMI catalog telecommunication products have been built on our custom experience with communication systems. The company produced the first monolithic CMOS single-chip Codec with filters, and were the first to design a two-chip Codec-with-filter set that eliminates any crosstalk. A full line of products for telephone sets, speech synthesis chips and signal processors complete the spectrum of communications circuits. The material in this design manual is intended to assist in designing with standard and custom telecommunications MOS/LSI circuits.



Design Manufacturing and Test in Pocatello, Idaho

Assembly and Test Facilities in Korea

Design Center in Swindon, England



Assembly and Test in the Philippines

Product Listing by Part Number

S25089	DTMF Generator
S2559A/B/.../G	DTMF Generator
S2560A	Telephone Pulse Dialer
S2561/A/C	Tone Ringer
S2562	Repertory Dialer
S25610	Repertory Dialer with On Chip Memory, Line Powered
S2563	Repertory Dialer, Line Powered
S2811	Signal Processing Peripheral
RTDS2811	Real-time Development System (Emulator)
SSPP2811	Software Simulator/Assembler Program Package
S2814A	Fast Fourier Transformer
S2815	Digital Filter/Utility Peripheral
S2816	Echo Canceller Processor
S2859	DTMF Generator
S2860	DTMF Generator
S3501/A	μ-law PCM Encoder with Filters
S3502/A	μ-law PCM Decoder with Filters
S3503	A-law PCM Encoder with Filters
S3504	A-law PCM Decoder with Filters
S3505/A	μ-law Codec with Filters
S3506	A-law Codec with Filters
S3507/A	μ-law Codec with Filters
S3525A/B	DTMF Bandsplit Filter
S3526A/B	2600Hz Band-pass, Band-reject Filter
S3610	Speech Synthesizer with On Chip Memory
S3620	Speech Synthesizer for Use with External Memory
S3630	128K ROM

Product Listing by Function

Telephone Products

DTMF or Touchtone®, Generators

S25089	Exact replacement for Mostek's MK5089
S2559A/B/C/D	Ideal for most telephone designs
S2559E/F	Improved versions of the 2559 family. Recommended for new designs.
S2559G/H	Like the E and F but with Darlington output configuration
S2859	Low enable keyboard input pins
S2860	For applications where supply voltage is constant
S2861	Re-numbered as 2559E and F

Other Telephone Station Products

S2560A/A-2	Generates dial pulses from pushbutton keyboard
S2561	Tone Ringer; Replacement for mechanical bells and buzzers - 18-pin package with variable rate
S2561A	8-pin package version of the 2561 with fixed rate
S2561C	Tone Ringer with logic control - 18-pin package
S25610	Single Chip Repertory Dialer with ten 18-number memory
S2562	Repertory Dialer
S2563	Telephone line powered Repertory Dialer

Codecs

S3501	μ-law PCM Encoder with filters. AT+T D3 compatible A/B signalling
S3501A	μ-law PCM Encoder with filters. CCIS compatible A/B signalling
S3502	μ-law PCM Decoder companion to S3501
S3502A	μ-law PCM Decoder companion to S3501A
S3503	A-law PCM Encoder with filters
S3504	A-law PCM Decoder with filters
S3505	μ-law Codec with filters (not recommended for new designs)
S3505A	S3505 with A/B signalling feature (not for new designs)
S3506	A-law Combo Codec
S3507	μ-law Combo Codec
S3507A	S3507 with A/B signalling

Product Listing by Function (continued)

Filters	
S3525A	DTMF Bandsplit Filter. 3.58MHz buffered output.
S3525B	DTMF Bandsplit Filter. 896KHz buffered output.
S3526A	2600Hz Band-pass, Band-reject Filter.
S3526B	3526A with on chip voltage divider for single supply operation

Speech Products	
S3610	Speech Synthesizer with on chip 20K ROM
S3620	Speech Synthesizer with external ROM interface
S3630	128K N-MOS ROM, 16K×8 organization

Signal Processing	
S2811	Signal Processing Peripheral
RTDS2811	Real-time Development System (Emulator)
SSPP2811	Software Simulator/Assembler Program
S2814A	Fast Fourier Transformer
S2815	Digital Filter/Utility Peripheral
S2816	Echo Canceller Processor

Cross Reference by Part Number

Part Number	Manufacturer	AMI Functional Equivalent Part
TDA 1077	Phillips	2559
SPR 128	G.I.	3630
CM 1310	Supertex	3630
MC 14400	Motorola	3507
MC 14401	Motorola	3507
MC 14402	Motorola	3507
MC 14406	Motorola	3501/3502
MC 14408	Motorola	2560A
MC 14409	Motorola	2560A
SSI 201	SSI	3525
CD 22859	RCA	2559
2364	Intel	3630
2910/2912	Intel	3501/2
2913	Intel	3507
2914	Intel	3507
DF 320	Siliconix	2560A
NC 320	Nitron	2560A
DF 321	Siliconix	2560A
DF 322	Siliconix	2560A
DF 328	Siliconix	2560A
DF 341	Siliconix	3501/3502
DF 342	Siliconix	3501/3502
MSM 38128	OKI	3630
MT 4320	Mitel	3525
HD 44211	Hitachi	3507
HD 44231	Hitachi	3506
MK 5087	Mostek	2559
MK 5089	Mostek	25089
MK 50981	Mostek	2560A
MK 50982	Mostek	2560A
MK 50991	Mostek	2560A

Part Number	Manufacturer	AMI Functional Equivalent Part
MK 50992	Mostek	2560A
MK 5116	Mostek	3501/3502, 3507
MK 5151	Mostek	3501/3502, 3507
MK 5156	Mostek	3503/3504, 3506
MK 5170	Mostek	2562/2563
MK 5175	Mostek	25610
MK 5387	Mostek	2559
MK 5389	Mostek	25089
MM 5393	National	2560A
MM 5395	National	2559
ICM 7206	Intersil	2559
ACF 7310,12,7410	G.I.	3526
ACF 7323C	G.I.	3525
ACF 7363C	G.I.	3525
ACF 7383C	G.I.	3525
μPD 7720	NEC	2811
ML 8204	Mitel	2561A
ML 8205	Mitel	2561A
MT 8865	Mitel	3525
AY5 9100	G.I.	2560A
AY5 9151	G.I.	2560A
AY5 9152	G.I.	2560A
AY5 9153	G.I.	2560A
AY5 9154	G.I.	2560A
AY5 9158	G.I.	2560A
AY5 9200	G.I.	2562/2563
AY3 9400	G.I.	2559
AY3 9401	G.I.	2559
AY3 9410	G.I.	2559
AY5 9800	G.I.	3525
AY3 9900	G.I.	3501/3502

Cross Reference by Manufacturer

Manufacturer	Part Number	AMI Functional Equivalent Part
G.I.	SPR 128	3630
G.I.	ACF 7310,12,7410	3526
G.I.	ACF 7323C	3525
G.I.	ACF 7363C	3525
G.I.	ACF 7383C	3525
G.I.	AY5-9100	2560A
G.I.	AY5-9151	2560A
G.I.	AY5-9152	2560A
G.I.	AY5-9153	2560A
G.I.	AY5-9154	2560A
G.I.	AY5-9158	2560A
G.I.	AY5-9200	2562/2563
G.I.	AY3-9400	2559
G.I.	AY3-9401	2559
G.I.	AY3-9410	2559
G.I.	AY5-9800	3525
G.I.	AY3-9900	3501/3502
Hitachi	HD 44211	3507
Hitachi	HD 44231	3506
Intel	2364	3630
Intel	2910/2912	3501/2
Intel	2913	3507
Intel	2914	3507
Intersil	ICM 7206	2559
Mitel	MT 4320	3525
Mitel	ML 8204	2561A
Mitel	ML 8205	2561A
Mitel	MT 8865	3525
Mostek	MK 5087	2559
Mostek	MK 5089	25089
Mostek	MK 50981	2560A

Manufacturer	Part Number	AMI Functional Equivalent Part
Mostek	MK 50982	2560A
Mostek	MK 50991	2560A
Mostek	MK 50992	2560A
Mostek	MK 5116	3501/3502, 3507
Mostek	MK 5151	3501/3502, 3507
Mostek	MK 5156	3503/3504, 3506
Mostek	MK 5170	2562/2563
Mostek	MK 5175	25610
Mostek	MK 5387	2559
Mostek	MK 5389	25089
Motorola	MC 14400	3507
Motorola	MC 14401	3507
Motorola	MC 14402	3507
Motorola	MC 14406	3501/3502
Motorola	MC 14408	2560A
Motorola	MC 14409	2560A
National	MM 5393	2560A
National	MM 5395	2559
NEC	μPD 7720	2811
Nitron	NC 320	2560A
OKI	MSM 38128	3630
Phillips	TDA 1077	2559
RCA	CD 22859	2559
SSI	SSI 201	3525
Siliconix	DF 320	2560A
Siliconix	DF 321	2560A
Siliconix	DF 322	2560A
Siliconix	DF 341	3501/3502
Siliconix	DF 342	3501/3502
Supertex	CM 1310	3630

AMERICAN MICROSYSTEMS, INC.

Section 4.0

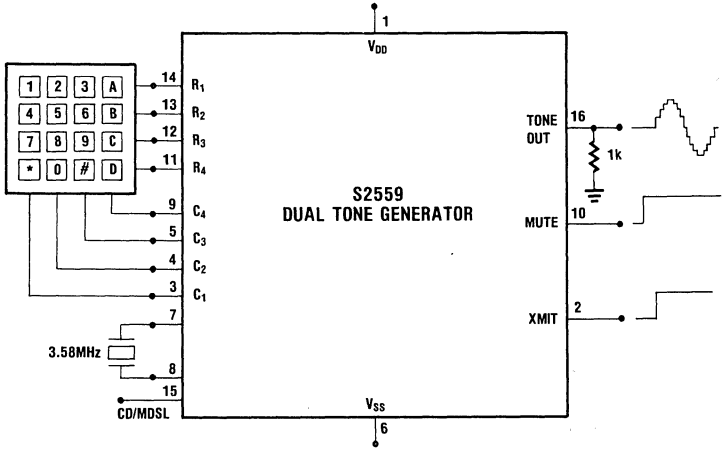
Brief Description of Telecom Products

- Telephone Products
- Codecs
- Signal Processors
- Filter Products
- Speech Synthesizers

DTMF Generators

S2559

- Line Powered Operation: 100μA Max Standby Current
- Wide Operating Voltage: E, F, G, H 2.5V to 10V; C and D, 2.75V to 10V; A and B, 3.5V to 13V
- Low Distortion (7% max for E & F) and Constant Output Amplitude
- Single or Dual Tone Output
- Uses Low Cost TV Crystal
- Uses X-Y or Standard Telephone Keyboard
- Darlington Output Configuration (G, H)



S2859

- Uses 2559 Pinout
- Wide Operating Voltage: 3.0V to 10V
- Line Powered Operation: 100μA Max Standby Current
- Inverted Keyboard Polarity for Direct Logic Control or Standard Telephone with Low Common
- Constant Output Amplitude with Varying Supply Voltage

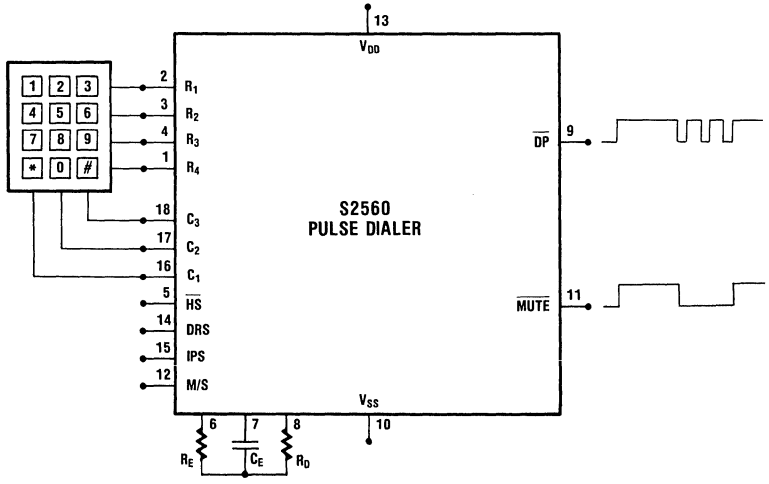
S2860

- Uses 2559 Pinout
- Optimized for 3.5V Operation
- Amplitude Proportional to Supply Voltage
- Highly Stable Output Amplitude Over Temperature: ±1.3dB
- Single or Dual Tone Output
- Has Keyboard Logic Polarity Inverted from 2559

S25089

- Exact Replacement for MOSTEK MK5089 DTMF Generator
- Similar to 2860

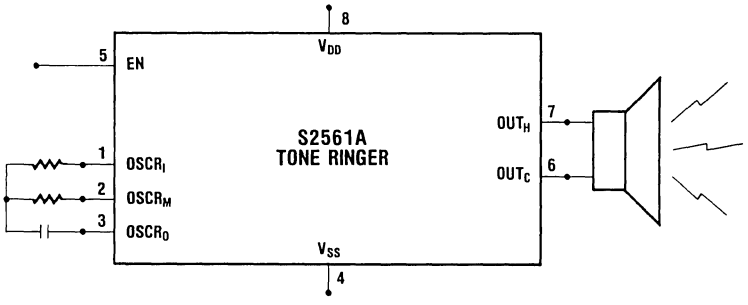
S2560A Pulse Dialer



- Line Powered Operation: 750nA Max Standby Current
- Low Operating Voltage: 1.5V to 3.5V
- Selectable Mark/Space Ratio, Inter-digit Pause Time and Dial Rate
- 20 Digit Memory for Last Number Redial (# Key)
- Very Stable Operation with RC Oscillator
- Uses X-Y or Standard Telephone Keyboard
- S2560A-2 Low Cost Version With Relaxed Specifications

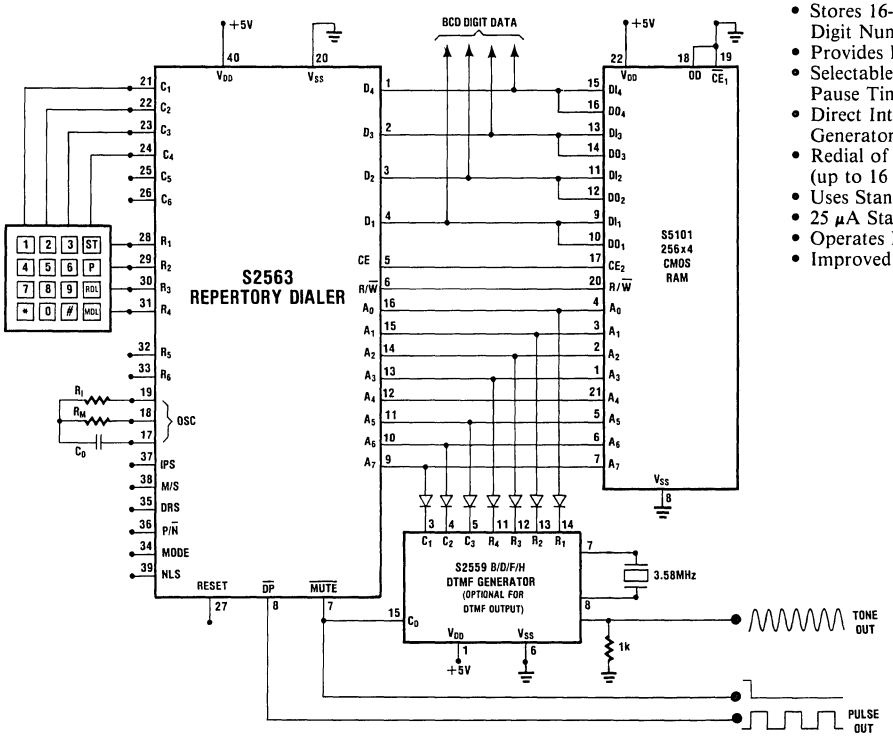
AMI

S2561A Tone Ringer



- Replacement for Bells and Buzzer
- Two Selectable Tones
- 8V to 12V Operating Range
- 5mA Push-Pull Output for Ceramic Resonators or Speakers with Impedance Transformers
- Selectable Rate on 2561 (18 Pin Package)
- Ringing Amplitude Sequencing Feature (18 Pin Package)

S2563 Repertory Dialer



- Stores 16-16 Digit Numbers or 29-8 Digit Numbers Using S5101 RAM
- Provides Dial Pulse Output.
- Selectable Pulse Rate and Interdigit Pause Time
- Direct Interface to S2559 DTMF Generator
- Redial of Last Number Dialed (up to 16 digits) With RDL Key
- Uses Standard X-Y Keyboard
- 25 μA Standby Current at 5V
- Operates Down to 2V
- Improved version of the S2562*

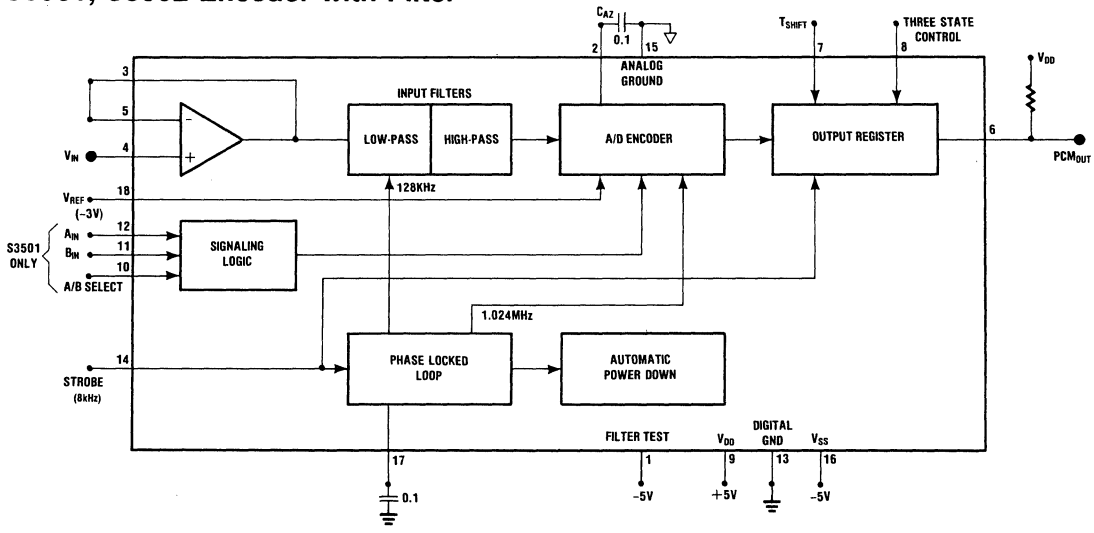
*NOTE: The S2562 is available, but not recommended for new designs.

AMI

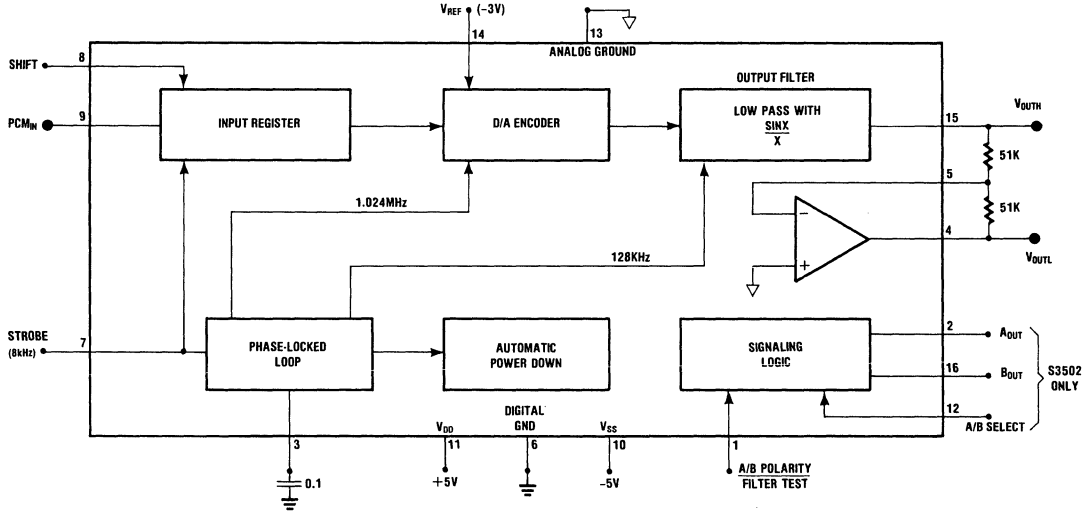
S3501, S3502, S3503, S3504 Encoder—Decoder with Filters

- Filter and Encoder or Decoder and Filter on the Same Chip: Ideal for Applications Which Require Encode or Decode Only
- On-board Phase-locked Loop Derives All Internal Timing Signals
- Automatic Power Down in Absence of 8kHz Strobe
- Auto Zero Circuit
- Low Idle Channel Noise: 14-17 dBrnCO
- Serial I/O Data Rates from 64K Bits/Sec to 3.152MBits/Sec
- Choice of μ-Law (3501, 3502) or A-Law (3503, 3504)

S3501, S3502 Encoder with Filter



S3502, S3504 Decoder with Filter



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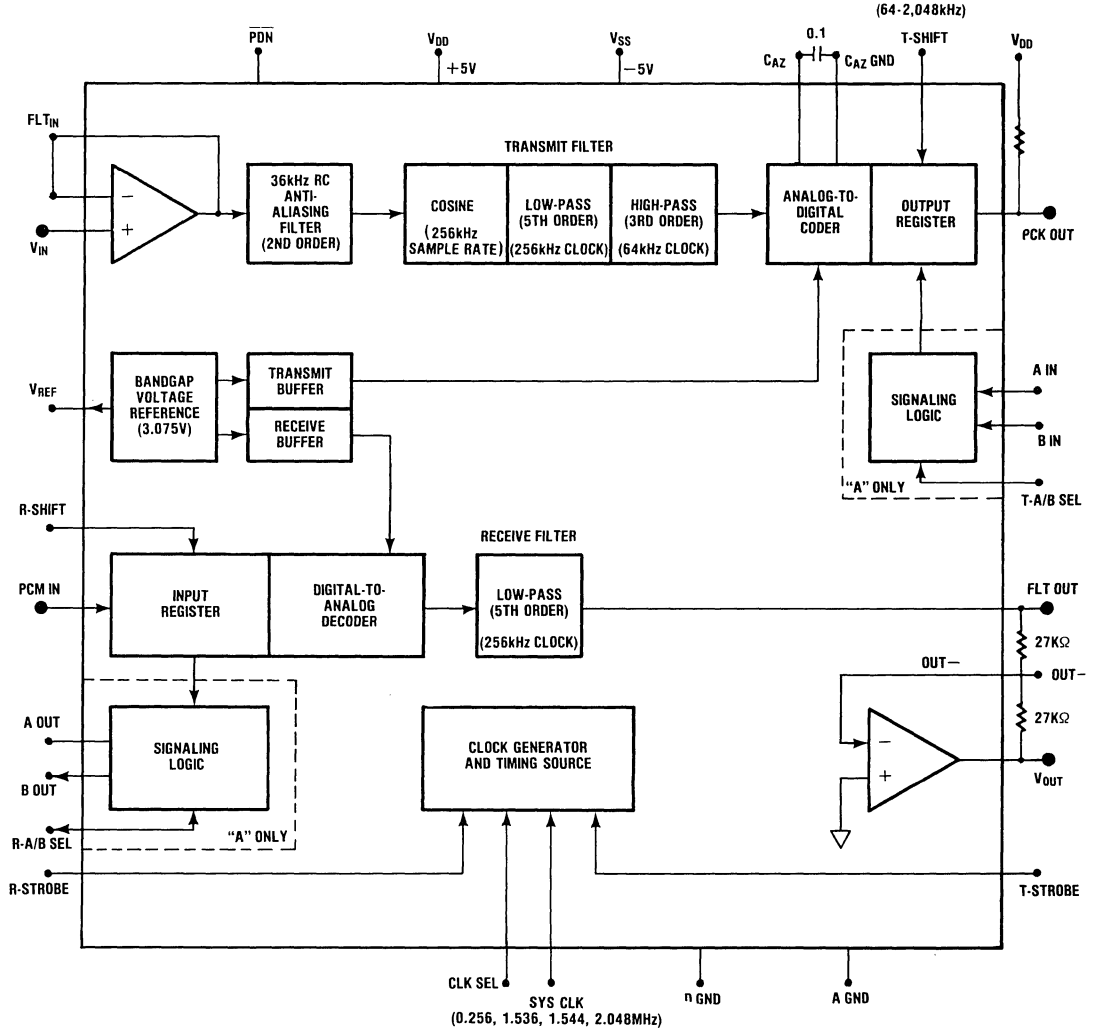
S3506, S3507, S3507A A-Law and μ-Law CMOS Codecs With Filters

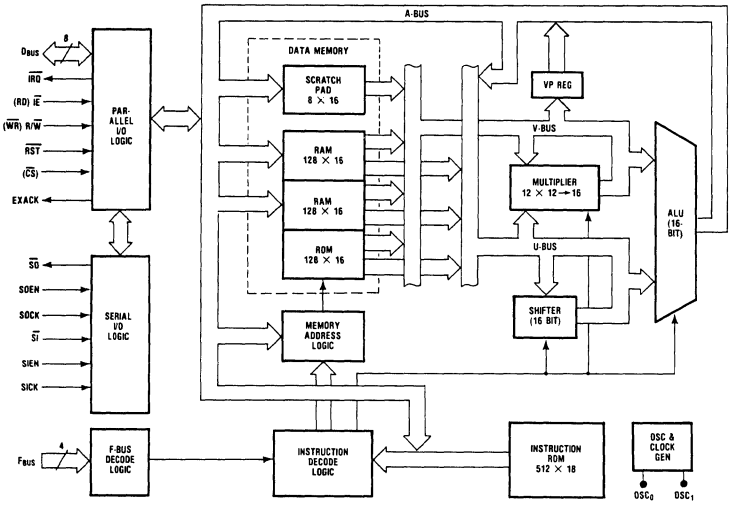
- Filters, Encoder and Decoder On One Chip
- Independent Operation of Encoder and Decoder Sections
- On Chip Precision Voltage Reference
- 22 Pin, 0.4″ Center Package (28 Pin With A/B Signalling)
- On Chip Second Order RC Anti-Aliasing Filter. 46dB rejection at 512kHz
- Maximum Power Consumption: 110mW Operating, 9mW Standby
- Serial I/O Data Rates From 64K-Bits/Sec to 2.1 Mega-Bits/Sec
- Programmable Input/Output Op-Amps
- Needs Only Two External Components



NOTE: The S3505 Codec with filters is available, but is not recommended for new designs.

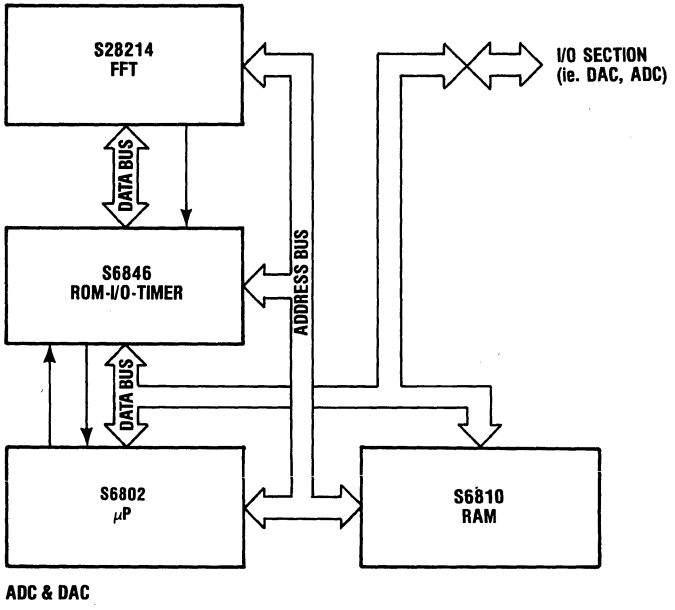
AMI

S28211 Programmable Real Time Digital Signal Processor



- Custom ROM Programmed
- 512 Word Instruction ROM
- Split Data Memory
  256 Words RAM, 128 Words ROM
- Self-Emulation Capability
- Realtime Processing of Signals to 100KHz
- Efficient Fetch/Multiply/Add/Store Instruction Cycle
- 300nSec Instruction Cycle Time
- Compatible With Any 8 or 16 Bit Microprocessor
- Direct Interface to 6800/8080/8085/Z80 Microprocessor Family

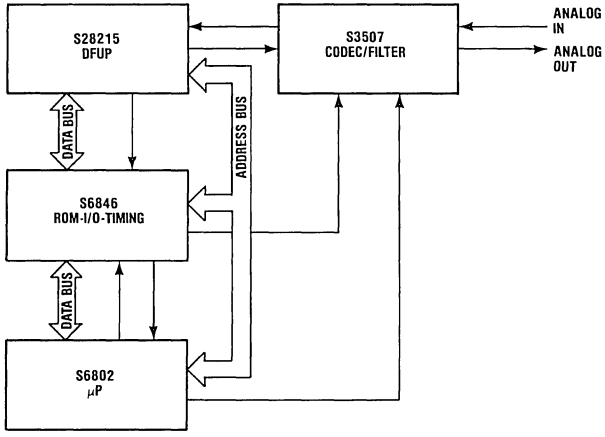
S28214 Fast Fourier Transformer



- Preprogrammed S28211
- Computes Real/Complex Point FFTs and IFFTs
- Computes Power Spectrums
- Real Time Spectrum Analysis of Signals to 10KHz
- Computes a 32 Complex Point FFT in 1.3mSec
- May be Used in Arrays to Increase Processing Bandwidth
- Handles Transform Sizes From 32 Points to 512 Points
- Larger Transforms Possible With Ext. Generated FFT COEF

AMI

S28215 Digital Filter/Utility Peripheral



- Preprogrammed S28211
- Two Independent 30 Tap Transversal Filters (Cascadable)
- Two 16 Section (Biquadratic) Recursive Filters
- Computational Functions: Integrations, Rectification, Squaring, and Block Multiply
- Conversion Functions: μ255 Law-to-Linear, Linear-to-μ255 Law, and Linear-to-dB
- Generator Functions: SINE and Pseudo-Random Noise
- Routines Cascadable to Form Complex Functions

S28216 Echo Canceller Processor

- Preprogrammed S28211
- Provides Main Echo Canceller Functions: Local Loop Delay, Estimation Echo, Modeling Performance Estimation, Silence & Double Talk Detection, & I/O Conversion
- Eliminates Echo Without Signal Degradation
- Allows Full Duplex Operation
- Accommodates Unlimited Long Haul Delays
- 6mSec Dispersion Handling Capability
- May be Inserted in Analog or Digital Data Paths
- Convergence Time <250mSec

SSPP 28211 Software Simulator/Assembler

The SSPP 28211 Software Simulator/Assembler is a Fortran IV program written to simulate the S28211 Signal Processing Peripheral. It is upwards compatible with the S28211 Real Time Emulator system.

The Software Simulator/Assembler is a low cost means of evaluating the performance of the S28211 Signal Processing Peripheral. As an assembler it may be used to produce the OP codes for mask programming of the S28211. The full simulator's prime function is to allow the users to debug and develop their signal processing routines, at low cost, and without the necessity to generate idealized signals that would be necessary when using the full speed emulator. This is particularly important in high speed applications where it is beneficial to be decoupled from practical difficulties while evaluating the signal processing algorithm.

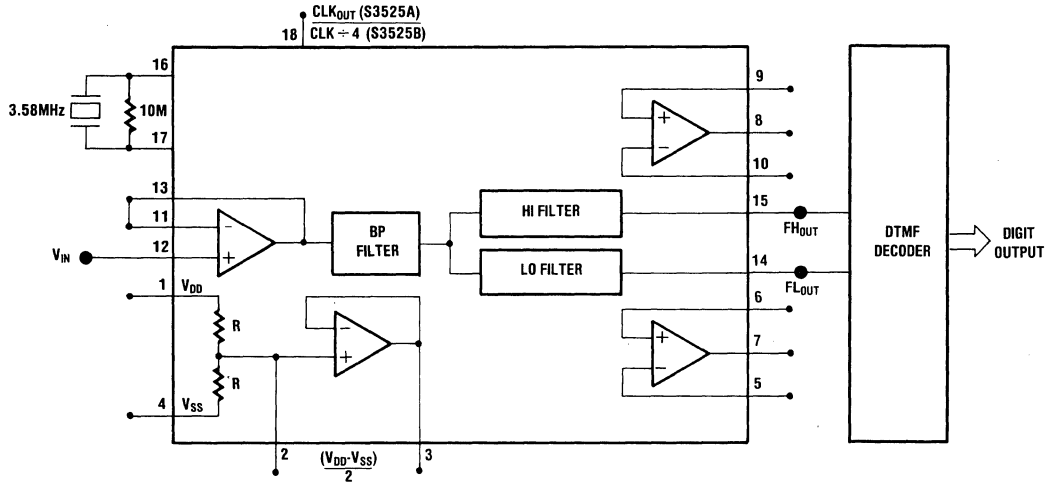
This software also allows the evaluation of the S28211 as to its capability to perform a specific function before totally committing to the complete project.

RTDS 28211 Real Time In-Circuit Emulator

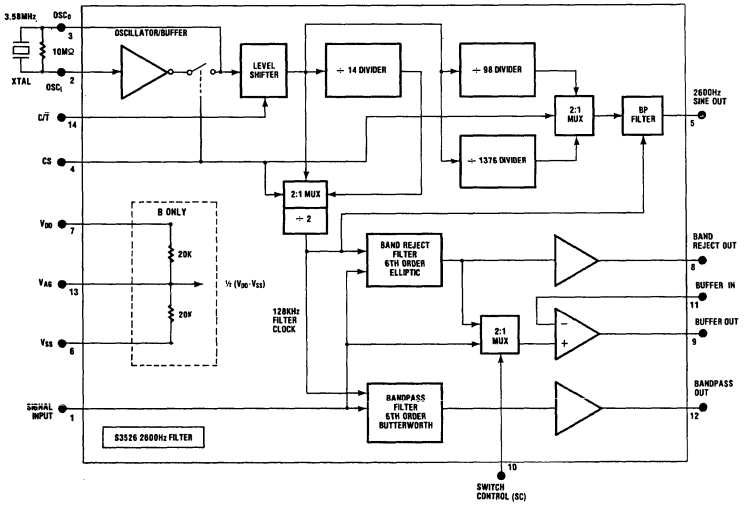
The RTDS 28211 Real-Time In-Circuit Emulator is a self-contained unit based on the 6800 microcomputer. The system has a full-feature software package with edit, assembly, trace, debug, etc., capabilities which is inter-compatible with the Software Simulator/Assembler. The system interfaces with microprocessor development systems via an RS-232C port and includes a remote emulator pod for direct insertion into the system (hardware under development.)

S3525 DTMF Bandsplit Filter

- Interface to Standard DTMF Decoders TT6174, MK 5102, MT 8860, 62, 63 and CRC 8030
- Buffered 1/2 (V_{DD}-V_{SS}) for Single Supply Operation
- Two Uncomitted OP Amps Available for Limiting and Squaring Outputs to the Decoder
- 10V to 13.5V Operating Range
- Buffered Input OP Amp for Gain Setting
- Uses Low Cost 3.58MHz TV Crystal



S3526 2600Hz Bandpass/Notch Filter

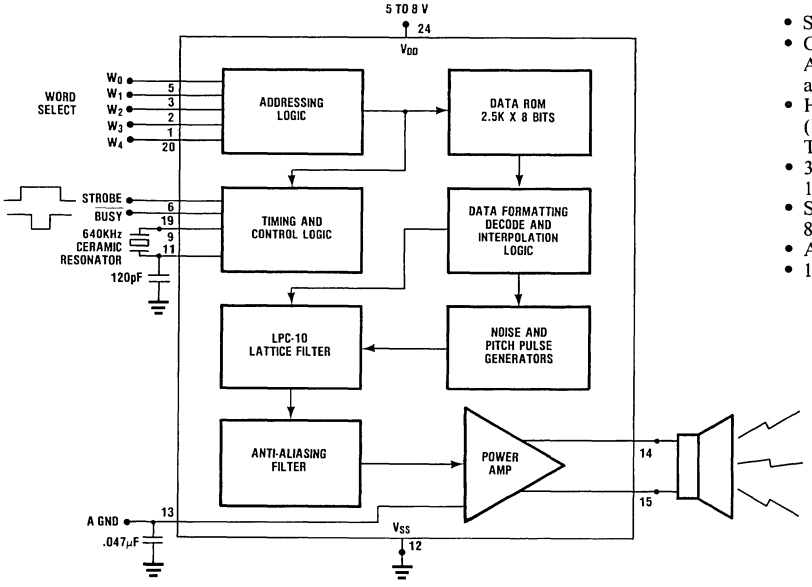


- Designed to Meet AT&T Telephone Interoffice Signalling Requirements
- Provides Bandpass and Band Reject Outputs
- Uses 3.58MHz TV Crystal Timebase
- Generates 2600Hz Signal
- Single 10V or Dual ±5V Supply Operation
- Bandpass/Notch Frequency can be Changed by Varying Crystal Frequency
- 80Hz Bandwidth (−3dB)
- Tuneable to Other Frequencies by Changing Oscillator Crystal or Drive

AMI

S3610 CMOS Speech Synthesizer

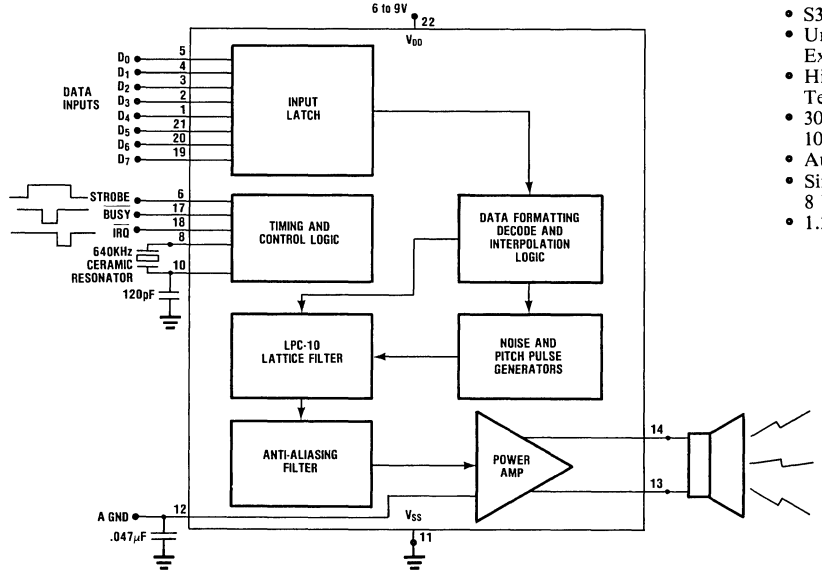
With 20K Internal ROM



- Single Chip CMOS Synthesizer
- On Chip 20K ROM Accommodates Approximately 17 Seconds of Speech and a 32 Word Maximum Vocabulary
- High Quality Speech Using LPC (Linear Preductive Cooling) Technology
- 30mw Audio Output. Directly Drives 100Ω Speaker
- Single Power Supply Operation: 5 to 8 Volts
- Automatic Powerdown: 6mw Max
- 1.2K to 2.0K Bits/Sec Data Rate

S3620 CMOS Speech Synthesizer

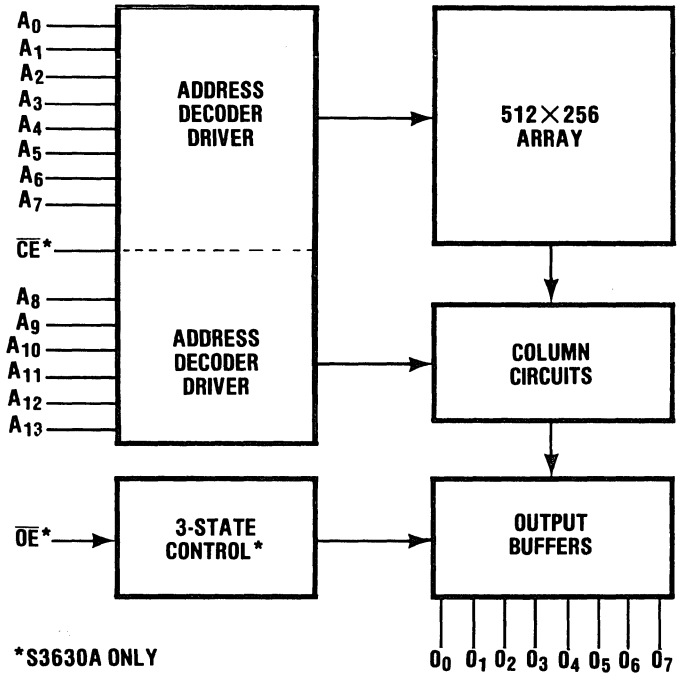
For Use With External ROM



- S3610 Without Internal ROM
- Unlimited Vocabulary by Use of External ROM(s)
- High Quality Speech Using LPC Technology
- 30mw Audio Output. Directly Drives 100Ω Speaker
- Automatic Powerdown: 6mw Max
- Single Power Supply Operation: 5 to 8 Volts
- 1.2K to 2.0K Bits/Sec Data Rate

AMI

S3630 128K (16KX8) Bit NMOS ROM



- Single +5V Power Supply
- Directly TTL Compatible Inputs
- Directly TTL Compatible Outputs, Three State on S3630A
- Low Power: 20mA Max Supply Current
- Power Down Capability (S3630A): 3mA Max.
- Two Pinouts Available:
  28 Pin/S3630A
  24 Pin/S3630B
- 6μs and 10μs Versions

AMERICAN MICROSYSTEMS, INC.

Section 5.0

Forthcoming New Products

S2550	Two to Four Wire Speech Network With Tone Ringer
S2569	DTMF Generator With 18 Digit Last Number Redial
S25910	Ten Number 14 Digit DTMF Repertory Dialer With Last Number Redial
S3508	Asynchronous Version of the S3506 A-Law Codec
S3509	Asynchronous Version of the S3507 μ-Law Codec
S3522	V22/Bell 212 Transmit/Receive Modem Filter With Group Delay Equalizers
S3527	16 Tap Analog Transversal Filter With 9-Bit Tap Control. Designed for Equalizing Voice Band Signals
S3528	Programmable Low Pass Filter
S3530	300 Baud Single Chip Modem

AMERICAN MICROSYSTEMS, INC.

Section 6.0

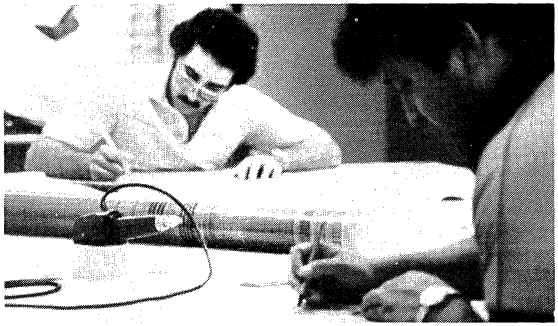
Custom MOS/VLSI Solutions For The Telecommunications Industry

- **Speech Synthesis and Recognition**
- **Modems**
- **Telephone/Communication Systems**
- **PABX**
- **Codecs**
- **Remote Data Control and Transmission**
- **Filters**

Whatever your needs for custom telecom circuits AMI has the experience and expertise to deliver the best solutions for you.

Custom Circuits For The Telecom Industry

In the telecommunications industry your demands on integrated circuits are extensive. You require economical circuits that have superior performance with increased reliability, and at the same time, use less power and board space. That's why more and more companies are turning to a custom MOS/VLSI (metal-oxide-silicon very large-scale integrated) solution as the best way to meet their telecommunications circuit requirements. Here are a few of the reasons why.



Computer-aided hand drawn circuits can be used to reduce circuit size to an absolute minimum.

Custom circuits save money

Grouping functions onto a single chip lowers production and inventory costs dramatically, reducing your product manufacturing costs as well.

Custom circuits are more reliable

Putting a complete system on a chip trims component count, improving both product reliability and production yields. Rework, repair and replacements are minimized.

Custom circuits reduce space and power requirements

Fewer components means both space and power requirements are reduced.

AMI's Custom Capability

As you can see, the advantages of custom circuits are quite extensive, but getting the best custom solution requires going to the right company.

AMI is the world's largest company dedicated to MOS/VLSI circuit design and manufacturing. AMI has a complete in-house manufacturing facility with the design and manufacturing expertise to take your product from conception to finished product.

AMI has worked with practically every type of MOS/VLSI circuit. AMI developed the first single chip microcomputer. AMI was the first to combine analog and digital on one chip. AMI developed the first single chip Combo Codec and is the recognized leader in the development of circuits utilizing switched capacitor filters for use in telecommunications applications. More than fifteen years of experience with 1500 different custom and customer-designed circuits has taught us a great deal about the special requirements of customers beyond custom design. Such things as efficient production controls for small lot manufacture, design security and product confidentiality, and custom-tailored quality assurance and reliability programs to assure all circuits meet your stringent requirements.

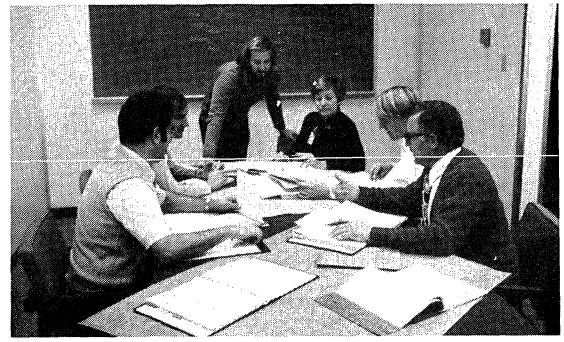
Confidentiality

In the highly competitive marketplace of telecommunications, confidentiality is a primary concern. Your market advantage is reduced if your competition can easily duplicate your custom circuit. AMI is extremely sensitive to this requirement and treats each circuit assignment as a highly proprietary project insuring complete security up to and through your product's manufacturing life.

Designing Your Custom Circuit At AMI

Fifteen years as the leader in custom MOS/VLSI circuit design means AMI has the experience and expertise to smoothly integrate your circuit needs.

The design process begins simply with either concepts/logic diagrams or prints/schematics. From these prints, the die size of the chip and the circuit development time span are estimated. Initial design specifications are then developed cooperatively between the customer and AMI. Circuit design is then started and, if needed, verified through breadboarding. After the design is complete, the circuit is ready for final layout and is drawn either on a computer console such as SIDS or is computer-aided hand drawn.



Routine AMI/customer meetings during design and fabrication assure that circuits meet the customers' specifications.

Computers speed design

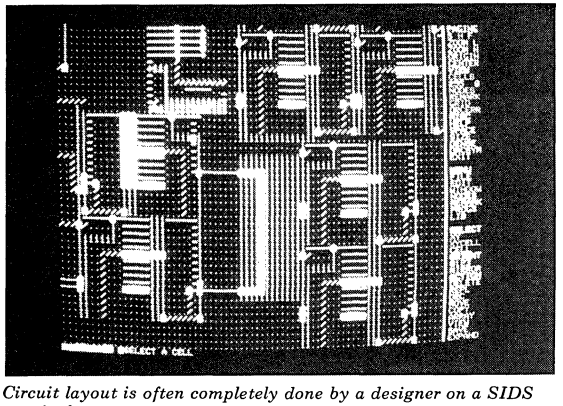
Instrumental in the design of AMI's Telecommunications custom circuits is our Symbolic Interactive Design System (SIDS).

Telecom circuit design is done primarily with the aid of SIDS. On SIDS, a layout designer works directly with symbols on a large screen alphanumeric color CRT. SIDS has on-line, real-time design rule checking capability to isolate design rule errors in the layout. This allows immediate correction of errors greatly reducing the development time span needed to develop a circuit.

A nodal trace function permits the designer to trace and highlight any given electrical node. In this way, the designer can manually assure that the node is properly connected as specified in the master logic description.

Full background real-time design rule checking on windows, cells, and chips is supported with SIDS, as is full background continuity checking against the master logic description. The use of the SIDS system eliminates the delay caused when digitizing and batch processed computer checking of circuits for accuracy is used.

Computer-Aided Design (CAD) systems cut development time and costs.



Circuit layout is often completely done by a designer on a SIDS terminal.

After the SIDS circuit design has been completed and verified, the symbols are converted to polygons and a 10X reticle tape is prepared.

With SIDS, error detection and correction, circuit modification and area relocations, take minutes, instead of weeks, significantly reducing design cycle time and development costs.

Leading CAD Technology

Computer Aided Design (CAD) software and hardware aids are employed to assure correctness of design each step of the way. Several highly efficient programs have been implemented to assist in logic design and simulation, layout planning, switched capacitor analysis routines and symbolic interactive design layout, to name just a few. Each of these programs have been fine tuned to closely model the actual process used at AMI.

Software design tools include:

Logic Design

Register Transfer Language (RTL) Simulation — provides a system behavior description to define instruction sets, optimize data paths, control hardware algorithm design and establish register designs.

GLIDE — permits user to design layout, simulate, generate patterns and develop test programs for logic arrays.

Path Analysis Program (PATH) — (Simulator with Assignment Delays) simulates logic network behavior for design verification and propagation delays.

Programmable Logic Array Designs Aids (PLAID) — uses state tables and Boolean equations to generate the optimum physical structure for random logic designs.

Digitizer enters hand drawn design elements into the computer.

Circuit Design

Circuit Simulator (ASPEC) — analyzes DC operation, DC transfer functions, time domain or transients and frequency domain or small AC characteristics.

Pole-Zero Analysis (PZSLIC) — program analyzes the frequency domain of linear integrated circuits.

Data Analysis Program (DAP) — analyzes data from circuit fabrication to maintain the parameters of circuit designs.

Switched Capacitor Analysis Routine (SCAR II) — analyzes switched capacitor filter designs used in telecommunication circuits. Two variations of the SCAR program are available to perform circuit sensitivity and noise analysis of switch capacitor filter circuits. This program is also used for scaling the switched capacitor ratios to optimize the final MOS design.

Layout Planning Aid (LPA) — lays out the chip plan and interconnection between functional blocks of an integrated circuit.

Symbolic Interactive Design System (SIDS) — permits a laying out and checking a circuit on a CRT screen, dramatically shortening layout time requirements.

Circuit Interactive Place and Route (CIPAR) — automatically creates error-free mask designs in extremely short time spans.

Computer controlled plotters are used to draw circuits.

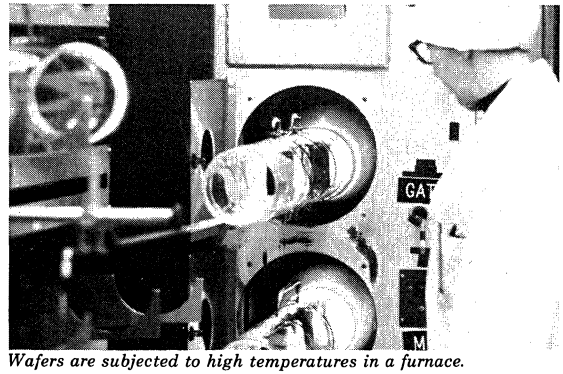
Manufacturing Quality Custom Circuits

Fabrication

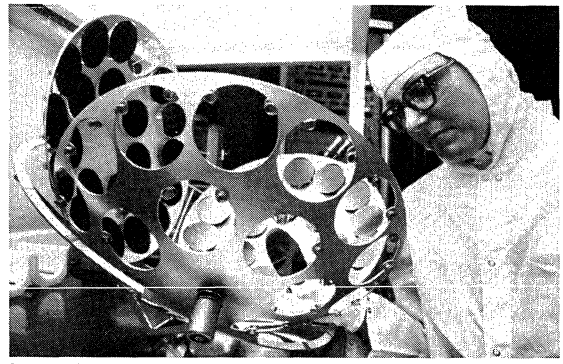
AMI's innovations extend beyond custom design to the fabrication of MOS/LSI circuits. The industry's most advanced fabrication equipment is used for processing wafers. Throughout the custom manufacturing process, control checks, optical and electrical inspections, fabrication data acquisition points, wafer probes and final test routines are performed. AMI utilizes these same tests and monitors on its standard telecom products to assure the highest quality product.

Quality assurance

AMI quality controls for in-process wafer inspection and final assembly and test are the best in the industry. Our care in fabrication, assembly and test mean that you get products that meet your specifications for reliability. Because over 70 percent of our total production is custom, we perform many checks routinely that would only be done on special orders and at additional cost by other manufacturers. In fact, our own in-house standard is tougher than required by most of our customers. Both our custom and standard products are screened to a 0.1% AQL level by our Q.A. Department before shipment. Most importantly, AMI is committed to making sure that everything we do is done right, every time we do it.



Wafers are subjected to high temperatures in a furnace.



During fabrication, silicon wafers are coated with aluminum in radio-frequency "sputtering" machines.

Quality checks

Among the routine quality controls exercised over every product at AMI are:

- Full logic design checks against system specifications
- Circuit simulation to verify performance against objectives
- Working plates check on automatic checkers
- Automated mask fabrication
- In-process wafer fabrication
- Wafer sort tests
- 100% optical inspection at dicing
- 100% die attach checking
- 100% lead bonding inspection prior to package sealing
- Seal checks, fine and gross leak tests
- 100% final digital and analog tests
- Customer specified environmental tests

Meticulous in-process checks are performed on design and workmanship at every step, to ensure a fully-manufacturable device. In manufacture, lot process and yield data are captured and examined as a matter of routine.

Test programs vary according to the requirements of the customer and the environment within which an integrated circuit must perform. The final testing to be performed on a circuit is normally decided on by AMI's and our customer's engineers. In addition, AMI provides special reliability programs for the stringent requirements of the telecommunications industry.

Please contact your AMI sales engineer to discuss your specific reliability or quality control requirements.

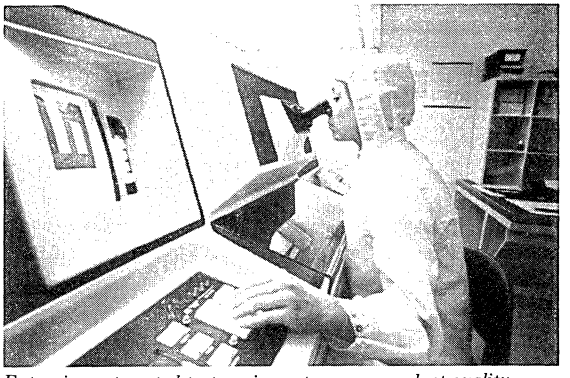
Automated mask inspection machine assures high quality photolithography.

Testing

AMI maintains extensive in-house test facilities to screen custom circuits to your specifications. State-of-the-art Fairchild Sentry 600, Sentry II and Sentry VII testers perform our digital testing requirements, while LTX testers test the combined analog/digital functions of telecommunications circuits.

AMI's extensive test equipment facility is backed up by test support software that includes a standard factor library allowing:

- Off-line, automatic creation of source factor programs
- Support of both functional and five types of DC parametric tests
- User control for the generation of different test programs



Extensive automated test equipment assures product quality.

Packaging

AMI's custom solutions do not stop with circuit design. Custom packaging is another reason AMI is the world's largest MOS/VLSI custom circuit manufacturer. AMI's packaging capability spans a broad spectrum besides the standard plastic, ceramic and cerdip packages. AMI's high-reliability plastic packages and chip carriers are accepted under the stringent requirements in the Telecom industry. As many industry segments move toward spacesaving packages, AMI remains in the forefront in packaging using chip carriers and is currently developing a family of mini-plastic-flat packages which are a low cost alternative to chip carriers.

Process Technologies

At AMI you get the widest selection of MOS alternatives and capabilities in the industry. Our core processing technologies range from mature PMOS metal gate, to silicon gate N-Channel, and to the advanced, small geometry, high-performance silicon gate CMOS.

A total of over 25 variations of core process in PMOS, NMOS, and CMOS are available. With so many variations of our basic core processes available, AMI can select the process which is right for your design. The charts which follow list the process parameters for some of our MOS processes.

CMOS Process Parameters

5 Micron

Process	Description	Pair Delay	V_{TH} & Min.	V_{TP} Max.	V_{TF} & BV Min.	Operating Voltage	Max. Rating
CVA	High Voltage - General Purpose	10nsec	0.7	1.3	7	2.2-13.2V	15V
CVB	High Voltage - 2 Poly Linear, Used In Telecom Applications	10nsec	0.7	1.3	17	2.2-12.2V	15V
CVC	Low Voltage - Nand ROM. Dense For Speech Processing Applications Where Slow Speed is ok	8nsec	0.5	1.1	7	1.5-5.5V	7V
CVD	CVB With Nand ROM. Good Linear With CVC Advantages	10nsec	0.7	1.3	17	2.2-13.2V	15V
CVE	Low Voltage - 2 Poly. Ideal For Logic With Lots Of Interconnect	8nsec	0.5	1.1	7	1.5-5.5V	7V
CVH	Low Voltage General Purpose - For Digital Applications With 1.7V-5V Power Supply	8nsec	0.5	1.1	7	1.5-5.5V	7V
CWA	High Voltage I_{SO} - P-Well General Logic	10nsec	0.7	1.3	17	3.0-13.2V	15V
7.5 Micron							
CTA	Low Voltage General Purpose Digital Process		0.4	1.0	7V	1.2-5V	5V
CTD	Intermediate Voltage General Purpose Digital Process		0.7	1.2	10V	2.0-10V	12V
CTE	High Voltage General Purpose Digital Process		0.9	1.5	15V	2.6-13.2V	15V

NMOS Process Parameters

6 Micron

Process	Description	VTE Min.	VTE Max.	VTF Min.	VTF Max	Operating Voltage	Max. Rating
NVC	High Voltage General Purpose	0.6	1.0	13	40	5-12	14
NVD	High Voltage Low Threshold	0.8	1.2	20	40	5-12	14
NVS	NVC With Circuit Shrink Polybias 5.4 Microns	0.75	1.25	20	40	5-10	12
5 Micron							
NEA/NEC	Fast Switching - 5 Volt Normal Operating	0.6	1.0	20	40	5-8	10

Telecommunications Expertise

Combined digital analog combinations

AMI is a leading innovator in combining digital and analog functions on a single chip. We can combine any of the functions listed and others into an optimum circuit configuration to meet your needs.

Unique combinations of these functions are already used in many applications in the communications, consumer and industrial marketplace including: thermostat controller, audio multiplexer, single chip microcomputer, single chip Codec, tone receiver, spectrum analyzer, echo canceller, speech synthesizer, modems, repertory dialer, touch-tone generator.

Digital	Analog
PLA	OP AMP
ALU	Oscillator
RAM and ROM	Bandgap-Voltage Reference
Shift Register	A/D and D/A Converters
Interface Driver	Switched Capacitor Filters
Automatic Power Down	Phase-locked Loops
Fuseable Link PROM's	Voltage Controller
	Attenuator Analog Switches

Using Switched Capacitors For Analog Circuitry

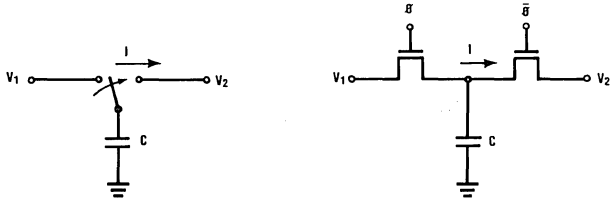
Switched capacitor technology is a very powerful tool in the design of analog circuitry. Typically, these capacitors are used in the input and/or feedback of Op Amps. When switched capacitors are used at the input, an equivalent RC product is generated which is actually just the ratio of two capacitors. When the feedback capacitor is also switched, then the gain of the Op Amp can be varied. By cascading these basic building blocks complex filters and circuits can be realized.

Since in MOS fabrication capacitors and, more importantly, capacitor ratios can be precisely manufactured and controlled, the resulting filters and precision gain elements built with this technology will have very high initial accuracy and excellent long term stability. So with switched capacitor technology, it is now possible to build analog circuitry which previously required inductors, large capacitors, precision components, and circuit fine tuning or laser trimming.

At AMI, our switched capacitor circuits are designed using double poly CMOS to provide totally floating capacitors and the obvious benefits of CMOS.

Simplified examples of a switched capacitor resistor, Op Amp, multiplying digital to analog converter, bandgap reference and ladder filter circuits are shown below to indicate both the simplicity and usefulness of such a powerful MOS/VLSI capability.

Figure 1. Switched Capacitor "Resistor"



A) SWITCHED CAPACITOR

$$Q = C(V_2 - V_1)$$

$$I = \frac{C(V_2 - V_1)}{T_C}$$

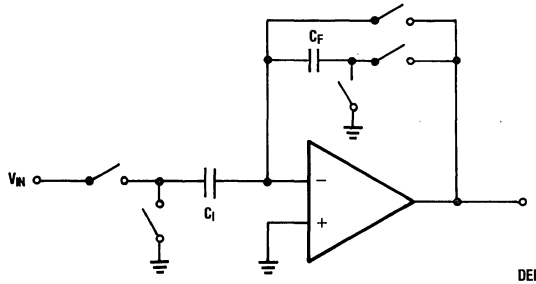
$$R = \frac{T_C}{C} = \frac{1}{Cf_C}$$

B) MOS REALIZATION

$f_C >> f_S$

f_C IS THE FREQUENCY OF CLOCK ϕ
ϕ AND $\bar{\phi}$ ARE NON OVERLAPPING CLOCKS

Figure 2. Offset Cancelled Gain Stage With Programmable Polarity



$$V_O = a \frac{C_I}{C_F} V_{IN}$$

a = +1 OR −1
DEPENDING ON SWITCHING SEQUENCE

Figure 3. Multiplying D/A Converter With Programmable Gain and Polarity With Auto Zero

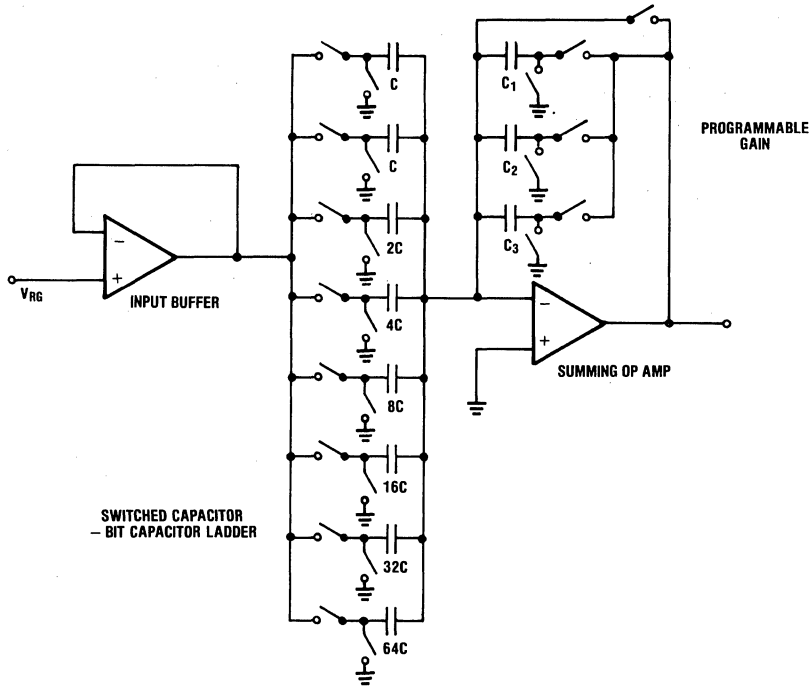


Figure 4. CMOS Band-Gap Reference and Trimming Buffer Using Polysilicon Fuses

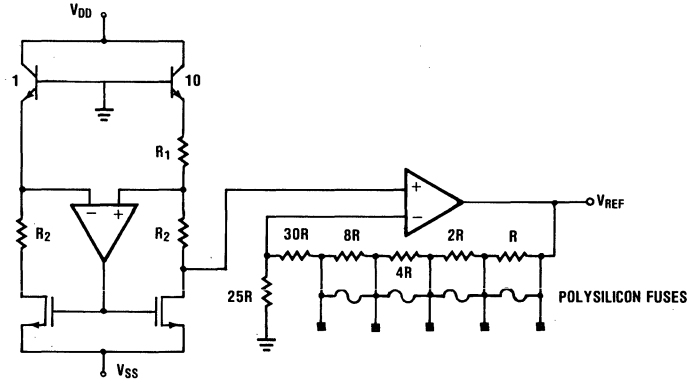
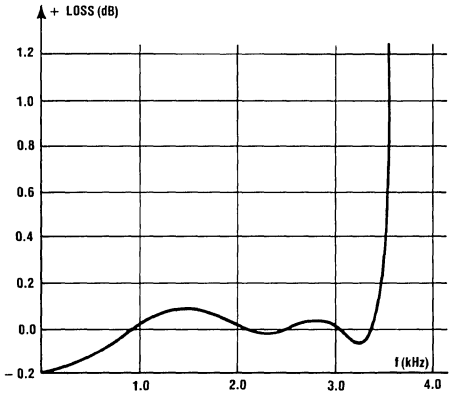
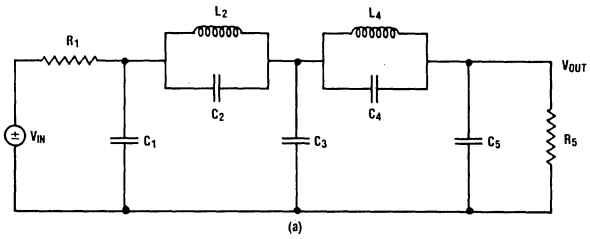


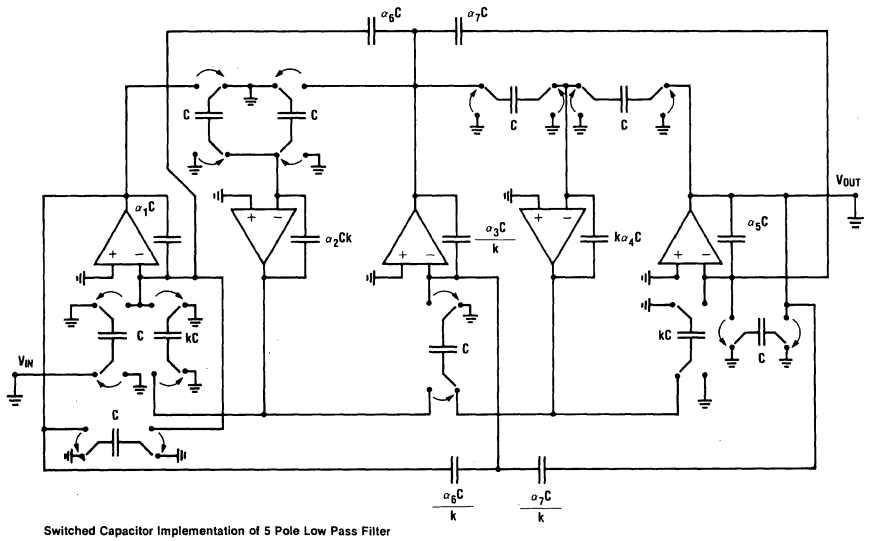
Figure 5. Five Pole Low Pass Filter



DESIRED FREQUENCY RESPONSE



ANALOG MODEL OF LOW PASS FILTER



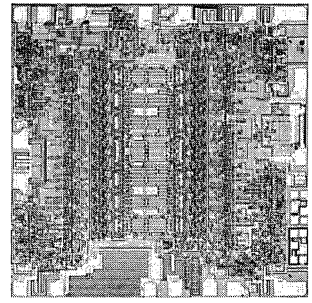
Switched Capacitor Implementation of 5 Pole Low Pass Filter

A History Of Successes

The following circuits are but a few examples of the many telecommunications circuits AMI has designed.

CMOS DTMF Generator

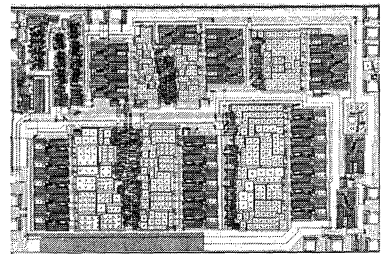
- Synthesizes Dual 700Hz to 1700Hz Sine Waves
- Telephone Line Powered
- Low Distortion Tone Generation Requires No External Filtering
- Operates Down To 2.5 Volts
- On Chip Voltage Reference



DIE SIZE: 115 × 116 MILS

DTMF Bandsplit Filter

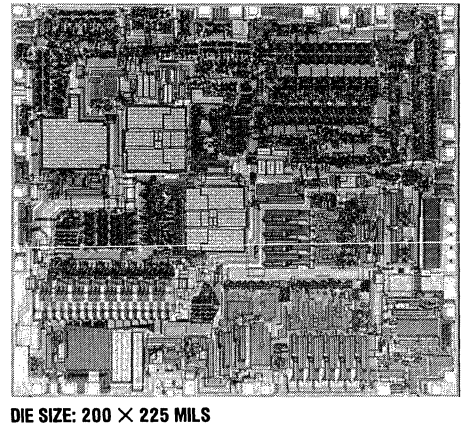
- Precision Filters Using Switched Capacitor Techniques
- On Board Voltage Divider For Single Supply Operation
- 3.58MHz TV Crystal Time Base For Very Stable Frequency Response
- Six Separate Filter Sections Including 5th Order Elliptic Hi Pass/Low Pass and Dial Tone Reject Filters



DIE SIZE: 127 × 190 MILS

World's First CMOS Combo Codec

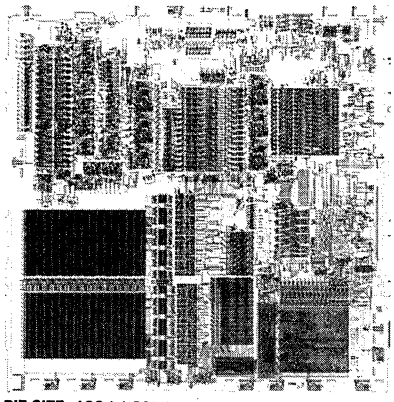
- Companding 8-Bit D/A and A/D Converters
- Trimmed Bandgap Voltage Reference
- Continuous 2 Pole 34KHz Anti-aliasing Low Pass Filter
- Switched Capacitor Voice Band Transmitting and Receiving Filters
- Input and Output Amplifiers
- On Board Clock & Timing Generators
- Two Speed Auto Zero Loop For Fast Acquisition After Power Up
- 60mw Power Consumption With 6mw in Standby Mode



DIE SIZE: 200 × 225 MILS

High Speed Signal Processor

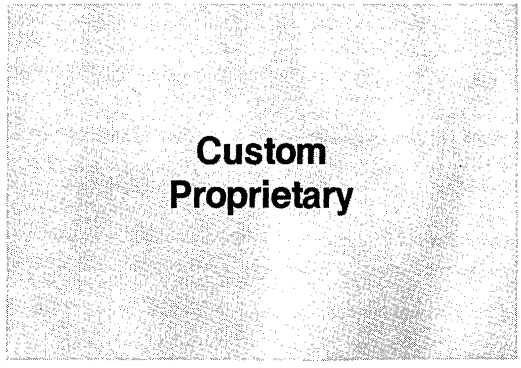
- 300ns Multiply + Add + Store Cycle Time
- 12 by 12 Pipeline Multiplier With 16-Bit Accumulator
- On Chip Oscillator
- 16-Bit Adder/Subtractor Unit
- 256 × 17 ROM
- 128 × 16 ROM
- 128 × 16 RAM



DIE SIZE: 198 × 205 MILS

CMOS Adaptive Delta Modulator For PABX Systems

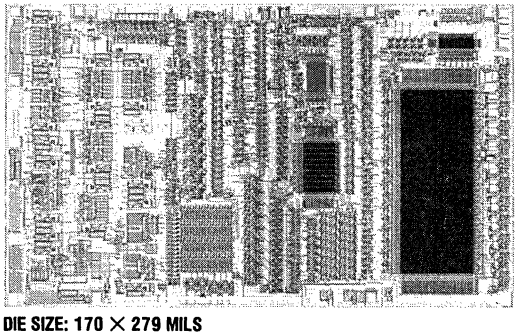
- DTMF Generator On Chip Accomplished By Square Wave Filtering
- On Board Phase Lock Loop
- Switched Capacitor Encode/Decode Audio Filters
- Low Impedance Output Drivers



DIE SIZE: 220×250 MILS

Single Chip CMOS Speech Synthesizer

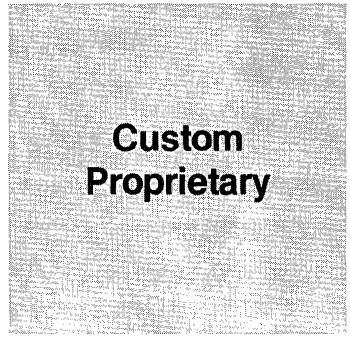
- 9-Bit Multiplying D/A Converter
- On Board 20K ROM and PLA
- Automatic Power Down
- 30mw Audio Output Amplifier
- 12 × 9 Bit Shift Register
- Switched Capacitor 3 Pole Low Pass Filter
- Voltage Divider On Chip For Single Power Supply Operation
- Time Base Oscillator Uses Either Crystal or Ceramic Resonator



DIE SIZE: 170 × 279 MILS

Receiver and Transmitter For 1200 Baud Modem

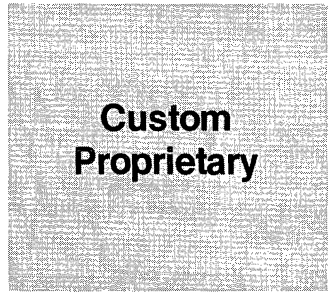
- Schmitt Trigger Inputs
- +5 Volt and −12 Volt Supplies
- Buss Drivers
- On Chip Shift Registers, Counters and Random Logic



DIE SIZE: 180×190 MILS

201/2400 Baud PSK Modem Transmitter

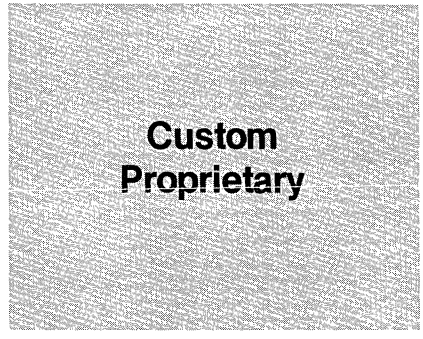
- Operates on +5 Volt and −12 Volt Supplies
- On Chip ROM
- Buss Drivers



DIE SIZE: 150×170 MILS

CMOS Serial Data Controller

- 5MHz Operating Frequency
- PLA Controlled Programming
- On Chip RAM
- Selects Messages Out Of PCM Data Stream
- Reinserts Modified Messages Into Data Stream



DIE SIZE: 185×230 MILS

S2559 A/B/C/D	DTMF Tone Generator
S2559 E/F/G/H	DTMF Tone Generator
S25089	DTMF Tone Generator
S2859	DTMF Tone Generator
S2860	DTMF Tone Generator
S2560A	Pulse Dialer
S25610	Single Chip Repertory Dialer
S2561	Tone Ringer
S2562	Repertory Dialer
S2563	Repertory Dialer
RTDS2811	Real-Time Development System
SSPP2811	Software Simulator/Assembler Program Package
S2811	Signal Processing Peripheral (SPP)
S2814	Fast Fourier Transformer (FFT)
S2815	Digital Filter/Utility Peripheral (DFUP)
S2816	Echo Canceller Processor (ECP)
S3501/A, S3502/A	Single Channel μLaw, PCM Codec Filter Set
S3503, S3504	Single Channel A-Law, PCM Codec/Filter Set
S3505/A	Single Chip μ-Law, PCM Codec with Filter
S3506, S3507/A	CMOS Single Chip μ-Law/A-Law Combo Codecs with Filters
S3525 A/B	DTMF Bandsplit Filter
S3526 A/B	2600Hz Bandpass/Notch Filter
S3610	LPC-10 Speech Synthesizer with On-Chip 20K Speech Data ROM
S3620	LPC-10 Speech Synthesizer
S3630	128K (16K$\times$8) Bit NMOS ROM

DTMF TONE GENERATOR

Features

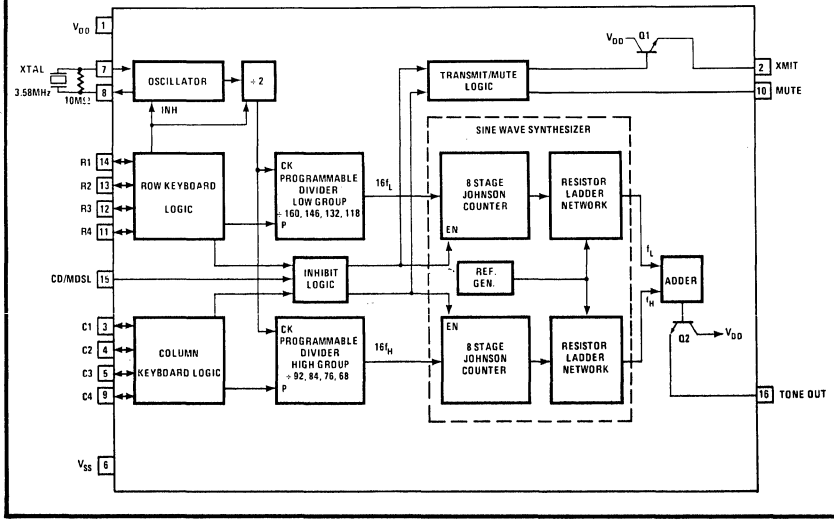
- ☐ **Wide Operating Supply Voltage Range: 3.5 to 13.0 Volts (A, B) 2.75 to 10 Volts (C, D)**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Mute Drivers On Chip**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range**
- ☐ **Dual Tone as Well as Single Tone Capability**
- ☐ **Four Options Available:**

  A:3.5 to 13.0V Mode Select
  B:3.5 to 13.0V Chip Disable
  C: 2.75 to 10V Mode Select
  D: 2.75 to 10V Chip Disable

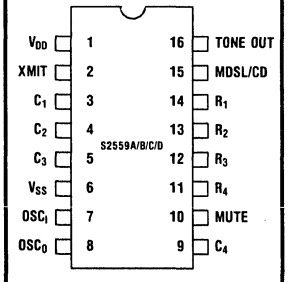
General Description

The S2559 DTMF Tone Genrator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinudsoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

DC Supply Voltage ($V_{DD}-V_{SS}$) S2559 A, B	+13.5V
DC Supply Voltage ($V_{DD}-V_{SS}$) S2559 C, D	+10.5V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +140°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6 \le V_{IN} \le V_{DD}+0.6$

S2559A & B Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			3.5		13.0	V
	Non Tone Out Mode (No Key Depressed)			3.0		13.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.5		0.4	40	μA
			13.0		1.5	130	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.5		0.95	2.9	mA
			13.0		11	33	mA
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	5.0	417	596	789	mVrms
		Row Tone, R_L=240Ω	12.0	378	551	725	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.5−13.0	1.75	2.54	3.75	dB
%DIS	Distortion*		3.5−13.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	(I_{OH}=15mA)	3.5	2.0	2.3		V
		(I_{OH}=50mA)	13.0	12.0	12.3		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		13.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		3.5		0	0.4	V
			13.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		3.5	3.0	3.5		V
			13.0	13.0	13.5		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.5	0.66	1.7		mA
			13.0	3.0	8.0		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.5	0.18	0.46		mA
		V_{OH}=9.5V	13.0	0.78	1.9		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current	V_{OL}=0.5V	3.5	0.26	0.65		mA
	One Key Selected	V_{OL}=0.5V	13.0	1.2	3.1		mA
I_{OH}	Output Source Current	V_{OH}=2.5V	3.5	0.14	0.34		mA
	One Key Selected	V_{OH}=9.5V	13.0	0.55	1.4		mA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

S2559A & B Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	V_{IL}=13.0V	13.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH}=0.0V	13.0			1.0	μA
I_{IL}	Sink Current	V_{IL}=0.5V	3.5	24	93		μA
	No Key Selected	V_{IL}=0.5V	13.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		3	6	mS
			13.0		0.8	1.6	mS
$C_{I/O}$	Input/Output Capacitance				12	16	pF
					10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL}=3.5V (Pull-down)	3.5	7	17		μA
		Sink Current V_{IL}= 13.0V (Pull-down)	13.0	150	400		μA
I_{IH}		Source Current, V_{IH}=3.0V (Pull-up)	3.5	90	230		μA
		Source Current, V_{IH}=12.5V (Pull-up)	13.0	370	960		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH}=0.0V (Pull-up)	3.5	1.5	3.6		μA
		Source Current, V_{IH}=0.0V (Pull-up)	13.0	23	74		μA
I_{IL}	Chip Disable Input (S2559D)	Source Current, V_{IL}=3.5V (Pull-down)	3.5	4	10		μA
		Sink Current, V_{IL}=13.0V (Pull-down)	13.0	90	240		μA

S2559C & D Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.75		10.0	V
	Non Tone Out Mode (No Key Depressed)			2.5		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8	16.0	mA
	Tone Output						
V_{OR}	Single Tone Mode Output Voltage		3.5	250	362	474	mVrms
		Row Tone, R_L=390Ω	5.0	367	546	739	mVrms
		Row Tone, R_L=240Ω	10.0	350	580	730	mVrms

S2559C & D Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
dB_{CR}	Ratio of Column to Row Tone		3.0−10.0	1.75	2.54	3.75	dB
%DIS	Distortion*		3.0−10.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	(I_{OH}=15mA)	3.0	1.5	1.8		V
		(I_{OH}=50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		2.75		0	0.5	V
			10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		2.75	2.5	2.75		V
			10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.0	0.17	0.41		mA
		V_{OH}=9.5V	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current One Key Selected	V_{OL}=0.5V	3.0	0.21	0.52		mA
		V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current One Key Selected	V_{OH}=2.5V	3.0	0.13	0.31		mA
		V_{OH}=9.5V	10.0	0.42	1.1		mA
	Input Current						
I_{IL}	Leakage Sink Current, One Key Selected	V_{IL}=10.0V	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH}=0.0V	10.0			1.0	μA
I_{IL}	Sink Current	V_{IL}=0.5V	3.0	24	93		μA
	No Key Selected	V_{IL}=0.5V	10.0	27	130		μA
t_{START}	Oscillator Startup Time		3.5		2	5	mS
			10.0		0.25	4	mS
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL}=3.0V (Pull-down)	3.0		16		μA
		Sink Current V_{IL}=10.0V (Pull-down)	10.0		24		μA
I_{IH}		Source Current, V_{IH}=2.5V (Pull-up)	3.0		210		μA
		Source Current, V_{IH}=9.5V (Pull-up)	10.0		740		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH}=0.0V (Pull-up)	3.0	1.4	3.3		μA
		Source Current, V_{IH}=3.0V (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559D)	Source Current, V_{IL}=3.0V (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, V_{IL}=10.0V (Pull-down)	10.0	55	143		μA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	−0.32
C3	1,477	1,471.9	−0.35
C4	1,633	1,645.0	+0.73

NOTE: % Error does not include oscillator drift.

Table 2. XMIT and MUTE Output Functional Relationship

OUTPUT	'DIGIT' KEY RELEASED	'DIGIT' KEY DEPRESSED	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

Circuit Description

The S2559 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the DTMF Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2559 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ±2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2559 takes into account these considerations.

Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Keyboard Interface

The S2559 employs a calculator type scanning circuitry to determine key closures. When no key is depressed, active pull-down resistors are "on" on the row inputs and active pull-up resistors are "on" on the column inputs. When a key is pushed a high level is seen on one of the row inputs, the oscillator starts and the keyboard scan logic turns on. The active pull-up or pull-down resistors are selectively switched on and off as the keyboard scan logic determines the row and the column inputs that are selected. The advantage of the scanning technique is that a keyboard arrangement of SPST switches are shown in Figure 2 without the need for a common line, can be used. Conventional telephone push button keyboards as shown in Figure 1 or X-Y keyboards with common can also be used. The common line of these keyboards can be left unconnected or wired "high".

Logic Interface

The S2559 can also interface with CMOS logic outputs directly. The S2559 requires active "High" logic levels. Since the active pull-up resistors present in the S2559 are fairly low value (500Ω typ), diodes can be used as shown in Figure 3 to eliminate excessive sink current flowing into the logic outputs in their "Low" state.

Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude V_P ($V_{DD} - V_{REF}$) of the stairstep function is fairly constant. V_{REF} is so chosen that V_P falls within the allowed range of the high group and low group tones.

Figure 1. Standard Telephone Push Button Keyboard

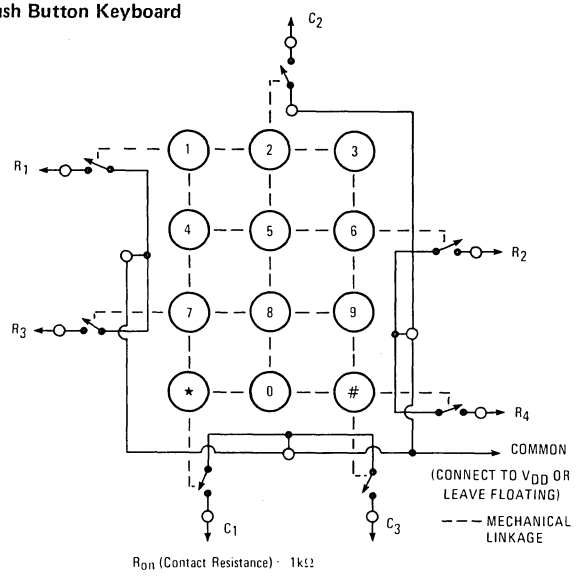


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 8 Row, Column Format

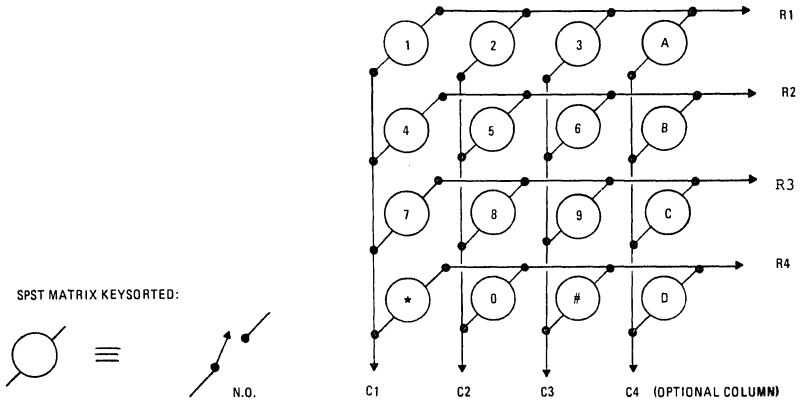
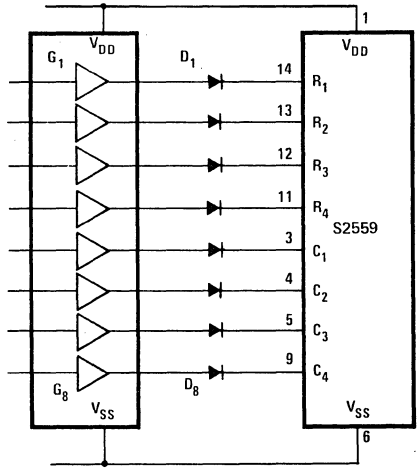
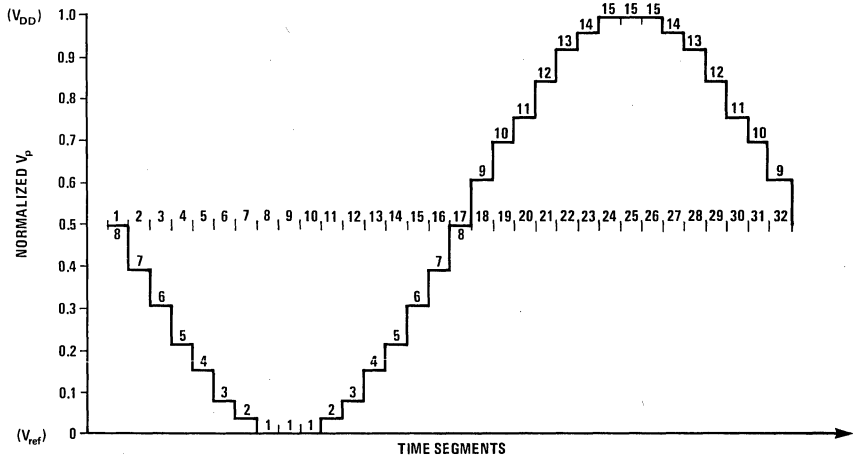


Figure 3. Logic Interface for Keyboard Inputs of the S2559



G1 THRU G8 ANY TYPE CMOS GATE
D1 THRU D8 DIODES TYPE IN914 (OPTIONAL)

Figure 4. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a bipolar NPN transistor connected as emitter follower to allow proper impedance transformation, at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by activating the appropriate row input or by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Mode Select

S2559A and S2559C have a Mode Select (MDSL) input (Pin 15). When MDSL is left floating (unconnected) or connected to V_{DD}, both the dual tone and single tone modes are available. If MDSL is connected to V_{SS}, the single tone mode is disabled and no output tone is produced if an attempt for single tone is made. The S2559B and S2559D do not have the Mode Select option.

Chip Disable

The S2559B and S2559D have a Chip Disable input at Pin 15 instead of the Mode Select input. The chip disable for the S2559B and S2559D is active "high." When the chip disable is active, the tone output goes to V_{SS}, the row, column inputs go into a high impedance state, the oscillator is inhibited and the MUTE and XMIT outputs go into active states. The effect is the device essentially disconnects from the keyboard. This allows one keyboard to be shared among several devices.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%
$R_S \leq 100\Omega$, L_M = 96MHY
C_M = 0.02pF C_h = 5pF

MUTE, XMIT Outputs

The S2559 A, B, C, D have a CMOS buffer for the MUTE output and a bipolar NPN transistor for the XMIT output. With no keys depressed, the MUTE output is "low" and the XMIT output is in the active state so that substantial current can be sourced to a load. When a key is depressed, the MUTE output goes high, while the XMIT output goes into a high impedance state. When Chip Disable is "high" the MUTE output is forced "low" and the XMIT output is in active state regardless of the state of the keyboard inputs.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the Digital Tone Generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the Tone Output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 5 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 5 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 5KΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3581A) and amplitudes at the selected frequencies can be noted. This measurment also permits verification of the preemphasis between the individual frequency tones.

Distortion is defined as "the ratio of the *total* power of all extraneous frequencies in the *voiceband* above 500Hz accompanying the signal to the power of the frequency *pair*." This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_n)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

where (V_1) ... (V_n) are extraneous frequency (i.e., intermodulation and harmonic) components in the 500Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$DIST_{dB} = 20 \log \frac{\sqrt{(V_1)^2+(V_2)^2+..(V_n)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\{\log[(V_1)^2+..(V_n)^2] - \log[(V_L)^2+(V_H)^2]\} \ldots (1)$$

An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from a S2559D device operating from a fixed supply of 4Vdc and R_L = 10kΩ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be −30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of -28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of −30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the 2559 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: *Bell System Communications Technical Reference, PUB 47001*, "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment," August 1976.

Figure 5. Test Circuit for Distortion Measurement

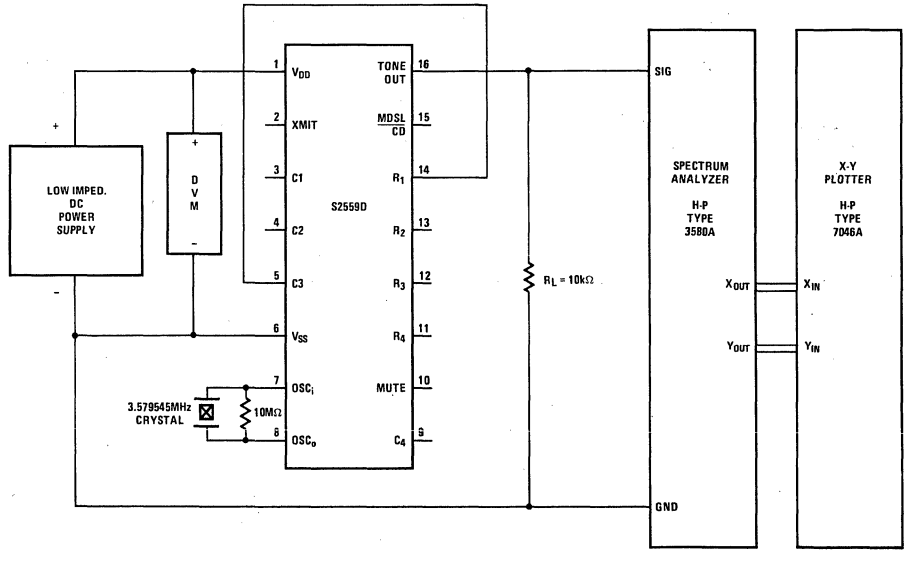
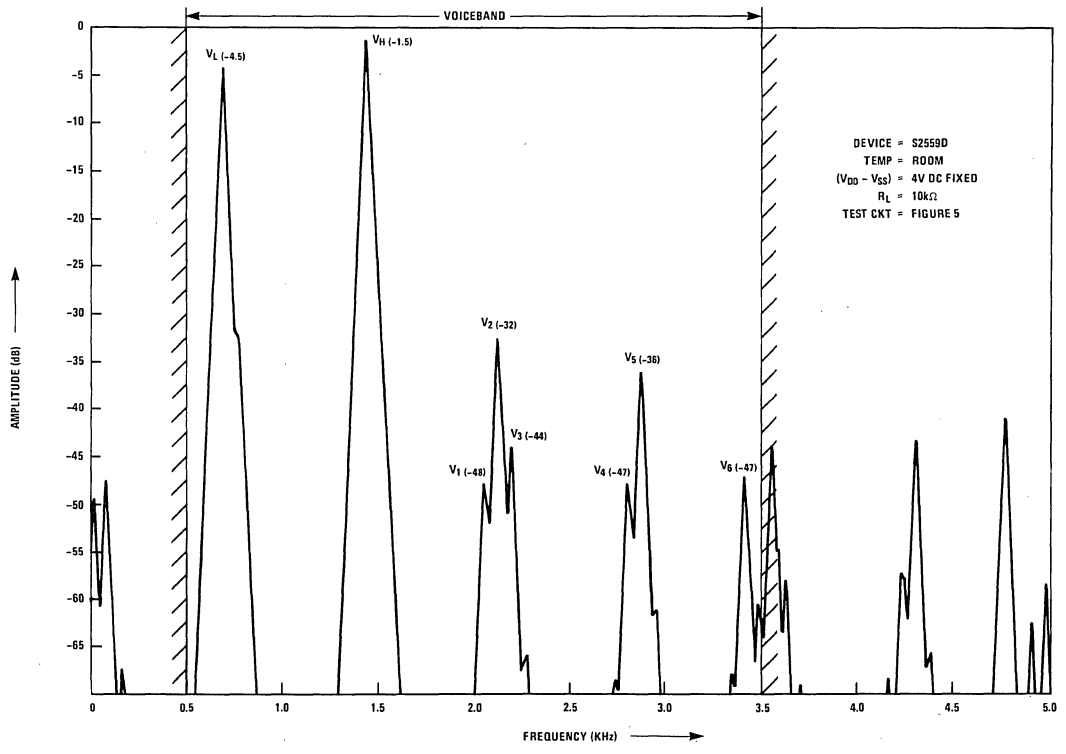


Figure 6. A Typical Spectrum Plot



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2559E/F/G/H

DTMF TONE GENERATOR

Features

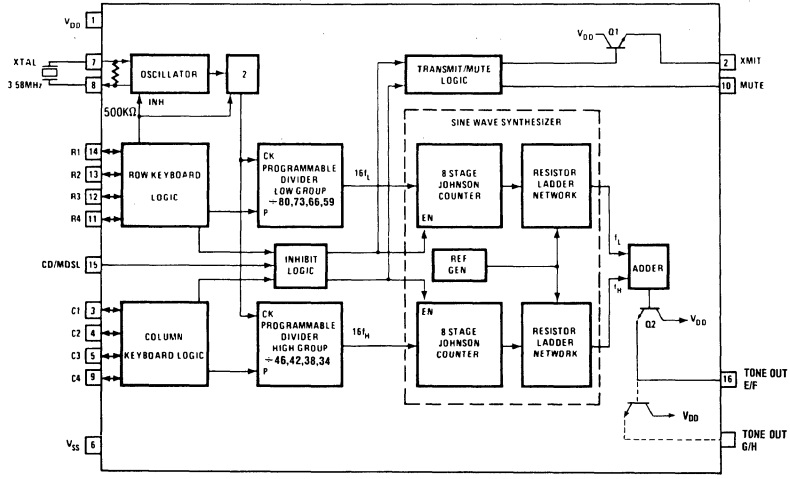
- ☐ Low Output Tone Distortion: 7%
- ☐ Wide Operating Supply Voltage Range: 2.5 to 10 Volts
- ☐ Oscillator Bias Resistor On-Chip
- ☐ Can be Powered Directly from Telephone Line or from Small Batteries
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ Four Options Available on Pin 15:
  - Bipolar Output
    - E: Mode Select
    - F: Chip Disable
  - Darlington Output
    - G: Mode Select
    - H: Chip Disable

General Description

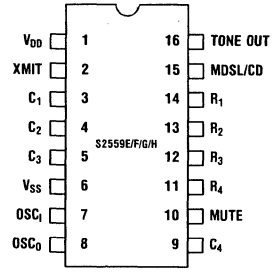
The S2559E, F, G and H are improved members of the S2559 Tone Generator Family. The new devices feature extended operating voltage range, lower tone distortion, and an on-chip oscillator bias resistor. The S2559E and F are pin and functionally compatible with the S2559C and D, respectively.

The S2559 G and H are identical to the E and F, except that there is a Darlington amplifier configuration on the tone out pin, rather than a single bipolar transistor as shown in the block diagram. In many applications this eliminates the need for a transistor in the telephone circuit. Tone distortion in the telephone is also likely to be lower.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

DC Supply Voltage (V_{DD}-V_{SS})	+10.5V
Operating Temperature	−25°C to +70°C
Storage Temperature	−30°C to +125°C
Power Dissipation at 25°C	1000mW
Digital Input	$V_{SS}-0.3 \leq V_{IN} \leq V_{DD}+0.3$
Analog Input	$V_{SS}-0.3 \leq V_{IN} \leq V_{DD}+0.3$

S2559E, F, G and H Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode (Valid Key Depressed)			2.5		10.0	V
	Non Tone Out Mode (No Key Depressed)			1.6		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8	16.0	mA
	Tone Output						
S2559E/F V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	3.5	335	465	565	mVrms
			5.0	380	540	710	mVrms
		Row Tone, R_L=240Ω	10.0	380	550	735	mVrms
S2559G/H V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L=390Ω	3.5	110	315	495	mVrms
			5.0	340	540	675	mVrms
		Row Tone, R_L=240Ω	10.0	415	590	770	mVrms
dB_{CR}	Ratio of column to Row Tone (Dual Tone Mode)		3.5−10.0	1.0	2.0	3.0	dB
%DIS	Distortion*	2559E/F	3.5−10.0			7	%
		2559G/H	4.0−10.0			7	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed)(Pin 2)	(I_{OH}=15mA)	3.0	1.5	1.8		V
		(I_{OH}=50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF}=0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		2.75		0	0.5	V
			10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed) No Load		2.75	2.5	2.75		V
			10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	V_{OL}=0.5V	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	V_{OH}=2.5V	3.0	0.17	0.41		mA
		V_{OH}=9.5V	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current	V_{OL}=0.5V	3.0	0.21	0.52		mA
	One Key Selected	V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current	V_{OH}=2.5V	3.0	0.13	0.31		mA
	One Key Selected	V_{OH}=9.5V	10.0	0.42	1.1		mA

**Distortion is defined as "the ratio of the total power of all extraneous frequencies, in the VOICE and above 500Hz, to the total power of the DTMF frequency pair".*

S2559E, F, G and H Electrical Characteristics (Continued)

Symbol	Parameter/Conditions		($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Oscillator Input/Output						
I_{OL}	Output Sink Current	V_{OL}=0.5V	3.0	0.21	0.52		mA
	One Key Selected	V_{OL}=0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current	V_{OH}=2.5V	3.0	0.13	0.31		mA
	One Key Selected	V_{OH}=9.5V	10.0	0.42	1.1		mA
t_{START}	Oscillator Startup Time		3.5		2	5	ms
			10.0		0.25	4	ms
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, VIL=3.0V (Pull-down)	3.0		16		μA
		Sink Current, VIL=10.0V (Pull-down)	10.0		24		μA
I_{IH}		Source Current, VIH=2.5V (Pull-up)	3.0		210		μA
		Source Current, VIH=9.5V (Pull-up)	10.0		740		μA
I_{IH}	Mode Select Input (S2559E,G)	Source Current, VIH=0.0V (Pull-up)	3.0	1.4	3.3		μA
		Source Current, VIH=3.0V (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559F,H)	Source Current, VIL=3.0V (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, VIL=10.0V (Pull-down)	10.0	55	143		μA

DTMF TONE GENERATOR

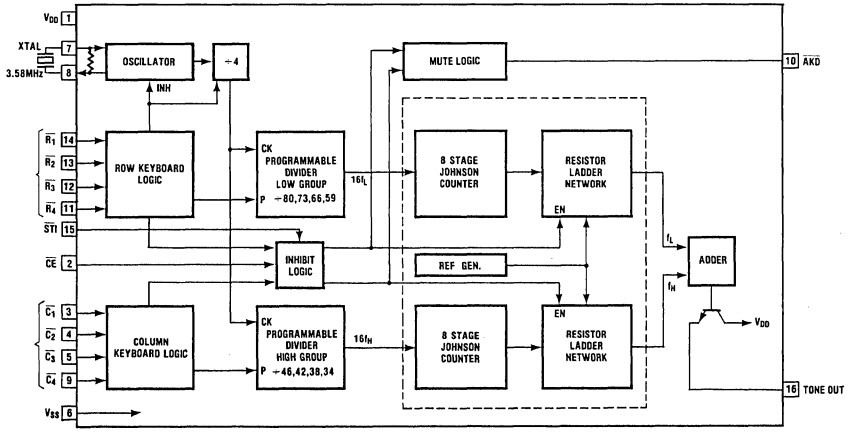
Features

- ☐ **Wide Operating Voltage Range: 2.5 to 10 Volts**
- ☐ **Optimized for Constant Operating Supply Voltages, Typically 3.5V**
- ☐ **Tone Amplitude Stability is Within ±1.5dB of Nominal Over Operating Temperature Range**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly From the Telephone Lines or From Small Batteries**
- ☐ **Uses TV Crystal Standard (3.58MHz) to Derive All Frequencies Thus Providing Very High Accuracy and Stability**
- ☐ **Specifically Designed for Electronic Telephone Applications**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button Keyboard With Common Terminal**
- ☐ **Low Total Harmonic Distortion**
- ☐ **Dual Tone as Well as Single Tone Capability**
- ☐ **Direct Replacement for Mostek MK5089 Tone Generator**

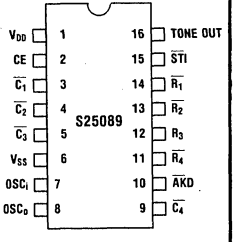
General Description

The S25089 DTMF Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD}-V_{SS})	+10.5V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	500mW
Input Voltage	$-0.6 \le V_{IN} \le V_{DD}$ +0.6
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −25°C to 70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				2.5	—	10.0	V
	Non Tone Out Mode ($\overline{AKD}$ Outputs toggle with key depressed)				1.6	—	10.0	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)			3.0 10.0	— —	1 5	20 100	μA μA
	Operating (One Key Selected, Tone and $\overline{AKD}$ Outputs Unloaded)			3.0 10.0	— —	.9 4.5	1.25 10.0	mA mA
	Tone Output							
V_{OR}	Dual Tone Mode Output	Row Tone	R_L=10kΩ R_L=100kΩ	3.0 3.5	−11.0 −10.0		−8.0 −7.0	dBm dBm
dB_{CR}	Ratio of Column to Row Tone			2.5-10.0	2.4	2.7	3.0	dB
%DIS	Distortion*			2.5-10.0	—	—	10	%
NKD	Tone Output—No Key Down						−80	dBm
	$\overline{AKD}$ Output							
I_{OL}	Output On Sink Current		V_{OL}=0.5V	3.0	0.5	1.0	—	mA
I_{OH}	Output Off Leakage Current			10.00		1	10	μA
	OSCILLATOR Input/Output							
I_{OL}	One Key Selected		V_{OL}=0.5V	3.0	0.21	0.52	—	mA
	Output Sink Current		V_{OL}=0.5V	10.0	0.80	2.1	—	mA
I_{OH}	Output Source Current		V_{OH}=2.5V	3.0	0.13	0.31	—	mA
	One Key Selected		V_{OH}=9.5V	10.0	0.42	1.1	—	mA

*Distortion measured in accordance with the specifications described in REF. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output (Continued)						
t_{START}	Oscillator Startup Time with Crystal as Specified		3.0-10.0	—	2	5	ms
$C_{I/O}$	Input/Output Capacitance		3.0	—	12	16	pF
			10.0	—	10	14	pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		—	V_{SS}		.2(V_{DD} −V_{SS})	V
V_{IH}	Input Voltage, High		—	.8(V_{DD} −V_{SS})	—	V_{DD}	V
I_{IH}	Input Current	V_{IH}=0.0V	3.0	30	90	150	μA
	(Pull up)	V_{IH}=0.0V	10.0	100	300	500	μA

Oscillator

The S25089 contains an oscillator circuit with the necessary parasitic capacitances and feedback resistor on chip so that it is only necessary to connect a standard 3.58MHz TV crystal across the OSC_i and OSC_0 terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 4 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3.579545MHz ±0.02%
R_S 100Ω, L_M=96mH
C_M=0.02pF C_H=5pF C_L=12pF

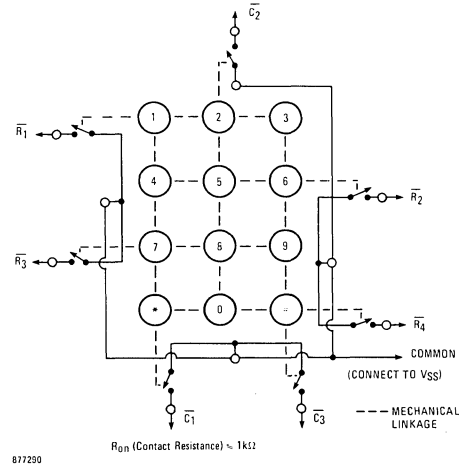
Keyboard Interface

The S25089 can interface with the standard telephone pushbutton keyboard (see Figure 1) with common. The common of the keyboard must be connected to V_{SS}.

Logic Interface

The S25089 can also interface with CMOS logic outputs directly (see Figure 2). The S25089 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 20kΩ -100kΩ.

Figure 1. Standard Telephone Push Button Keyboard



Tone Generation

When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group

frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divided by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD}-V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected, dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys that are not either in the same row or in the same column are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Inhibiting Single Tones

The $\overline{STI}$ input (pin 15) is used to inhibit the generation of other than dual tones. It has an internal pull down to V_{SS} supply. When this input is left unconnected or connected to V_{SS}, single tone generation as described in the preceding paragraph (Single Tone Mode) is suppressed with all other functions operating normally. When this input is connected to V_{DD} supply, single or dual tones may be generated as previously described (Single Tone Mode, Dual Tone Mode).

Chip Enable Input (CE, Pin 2)

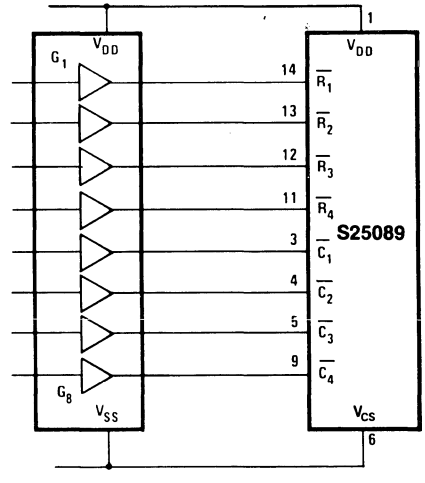
The chip enable input has an internal pull-up to V_{DD} supply. When this pin is left unconnected or connected to V_{DD} supply the chip operates normally. When connected to V_{SS} supply, tone generation is inhibited. All other chip functions operate normally.

Table 1. Comparison of Specified Vs. Actual Tone Frequencies Generated by S25089

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

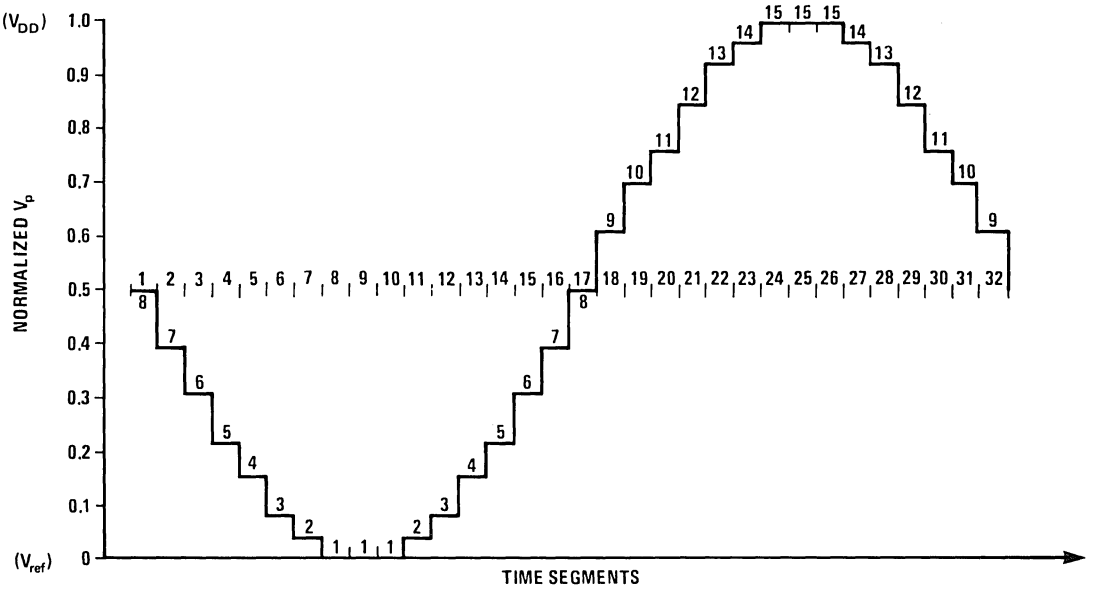
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S25089



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S25089 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of (V_{DD} - V_{REF}), increases with supply voltage (Figure 5).
b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ±1.0dB over nominal.
c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

$\overline{AKD}$ (Any Key Down or Mute) Output

The $\overline{AKD}$ output (pin 10) consists of an open drain N channel device (see Figure 6.) When no key is depressed the $\overline{AKD}$ output is open. When a key is depressed the $\overline{AKD}$ output goes to V_{SS}. The device is large enough to sink a minimum of 500μA with voltage drop of 0.2V at a supply voltage of 3.5V.

Figure 4. Structure of the Reference Voltage

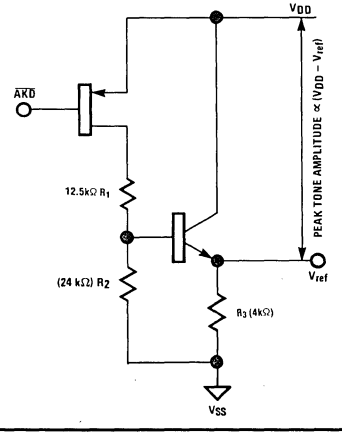


Figure 5. Typical Single Tone Output Amplitude Vs Supply Voltage (R_L = 10k)

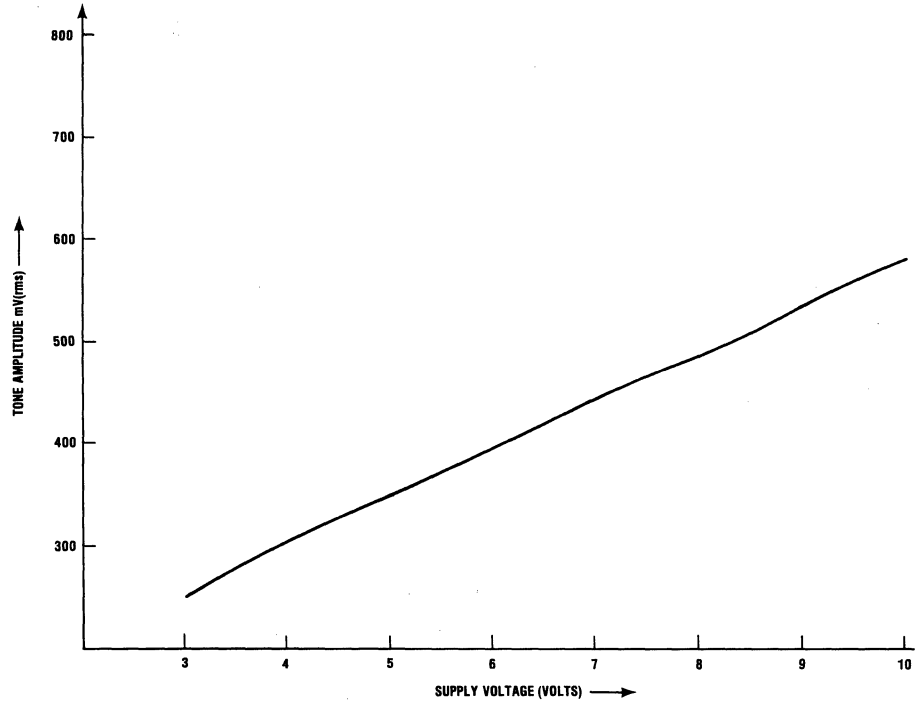
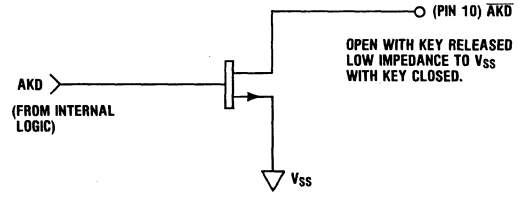


Figure 6. $\overline{AKD}$ Output Structure



AMERICAN MICROSYSTEMS, INC.

S2859

DTMF TONE GENERATOR

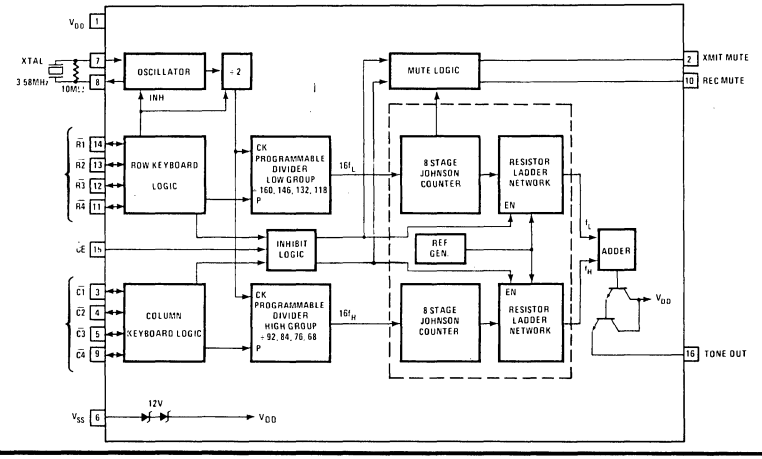
Features

- ☐ **Wide Operating Supply Voltage Range: 3.0 to 10 Volts**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Timing Sequence for XMIT, REC MUTE Outputs**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range**
- ☐ **Dual Tone as Well as Single Tone Capability**
- ☐ **Darlington Configuration Tone Output**

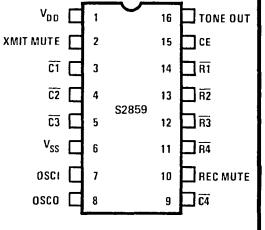
General Description

The S2859 DTMF Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2859 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, point-of-sale, and credit card verification terminals and process control.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD}-V_{SS}$)	+10.5V
Operating Temperature	−25 °C to +70 °C
Storage Temperature	−55 °C to +125 °C
Power Dissipation at 25 °C	500mW
Input Voltage	$-0.6 \leq V_{IN} \leq V_{DD}+0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −25 °C to 70 °C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			($V_{DD}-V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				3.0	—	10.0	V
	Non Tone Out Mode (Mute Outputs Toggle With Key Depressed)				2.2	—	10.0	V
V_Z	Internal Zener Diode Voltage, I_Z = 5mA			—	—	12.0	—	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and Mute Outputs Unloaded)			3.0	—	0.001	0.3	mA
				10.0	—	0.003	1.0	mA
	Operating (One Key Selected, Tone and Mute Outputs Unloaded)			3.0	—	1.3	2.0	mA
				10.0	—	11	18	mA
	Tone Output							
V_{OR}	Single Tone	Row	R_L=100Ω	5.0	366	462	581	mVrms
	Mode Output Voltage	Tone	R_L=100Ω	10.0	370	482	661	mVrms
dB_{CR}	Ratio of Column to Row Tone			3.0−10.0	1.0	2.0	3.0	dB
%DIS	Distortion*			3.0−10.0	—	—	10	%
	REC, XMIT MUTE Outputs							
I_{OH}	Output Source Current		V_{OH}=1.2V	2.2	0.43	1.1	—	mA
			V_{OH}=2.5V	3.0	1.3	3.1	—	mA
			V_{OH}=9.5V	10.0	4.3	11	—	mA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD} – V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output						
I_{OL}	One Key Selected	V_{OL} = 0.5V	3.0	0.21	0.52	–	mA
	Output Sink Current	V_{OL} = 0.5V	10.0	0.80	2.1	–	mA
I_{OH}	Output Source Current	V_{OH} = 2.5V	3.0	0.13	0.31	–	mA
	One Key Selected	V_{OH} = 9.5V	10.0	0.42	1.1	–	mA
I_{IL}	Input Current Leakage Sink Current One Key Selected	V_{IL} = 10.0V	10.0	–	–	1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH} = 0.0V	10.0	–	–	1.0	μA
I_{IL}	Sink Current	V_{IL} = 0.5V	3.0	24	58	–	μA
	No Key Selected	V_{IL} = 0.5V	10.0	27	66	–	μA
t_{START}	Oscillator Time		3.0 10.0	– –	2 0.25	5 0.75	ms ms
$C_{I/O}$	Input/Output Capacitance		3.0 10.0	– –	12 10	16 14	pF pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		3.0 10.0	– –	– –	0.75 3.0	V V
V_{IH}	Input Voltage, High		3.0 10.0	2.4 7.0		– –	V V
I_{IH}	Input Current	V_{IH} = 0.0V	3.0	20	60	100	μA
	(Pull up)	V_{IH} = 0.0V	10.0	66	200	336	μA

Circuit Description

The S2859 is designed so that it can be interfaced easily to the dual tone signaling telephone system and that it will more than adequately meet the recommended telephone industry specifications regarding the dual tone signaling scheme.

Design Objectives

The specifications that are important to the design of the Digital Tone Generator are summarized below: the dual tone signal consists of linear addition of two voice frequency signals. One of the two signals is selected from a group of frequencies called the "Low Group" and the other is selected from a group of frequencies called the "High Group". The low group consists of four frequencies 697, 770, 852 and 941 Hz. The high group consists of four frequencies 1209, 1336, 1477 and 1633 Hz. A keyboard arranged in a row, column format (4 rows x 3 or 4 columns) is used for number entry. When a push button corresponding to a digit (0 thru 9) is pushed, one appropriate row (R1 thru R4) and one appropriate column (C1 thru C4) is selected. The active row input selects one of the low group frequencies and the active column input selects one of the high group frequencies. In standard dual tone telephone systems, the highest high group frequency of 1633Hz (Col. 4) is not used. The frequency tolerance must be ±1.0%. However, the S2859 provides a better than .75% accuracy. The total harmonic and intermodulation distortion of the dual tone must be less than 10% as seen at the telephone terminals. (Ref. 1.) The high group to low group signal amplitude ratio should be 2.0 ± 2dB and the absolute amplitude of the low group and high group tones must be within the allowed range. (Ref. 1.) These requirements apply when the telephone is used over a short loop or long loop and over the operating temperature range. The design of the S2859 takes into account these considerations.

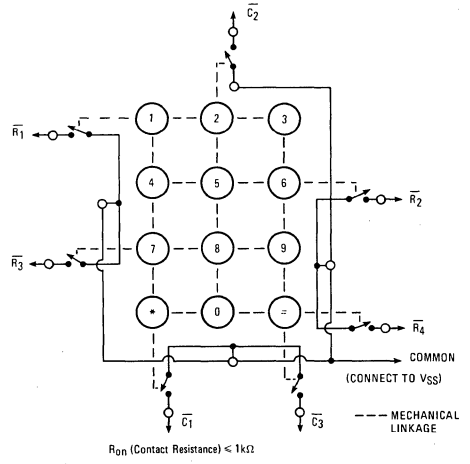
Oscillator

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Keyboard Interface

The S2859 can interface with either the standard telephone pushbutton keyboard (see Figure 1) or an X-Y keyboard with common. The common of the keyboard must be connected to V_{SS}.

Figure 1. Standard Telephone Push Button Keyboard



Logic Interface

The S2859 can also interface with CMOS logic ouputs directly. (See Figure 2.) The S2859 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 33kΩ—150kΩ.

Tone Generation

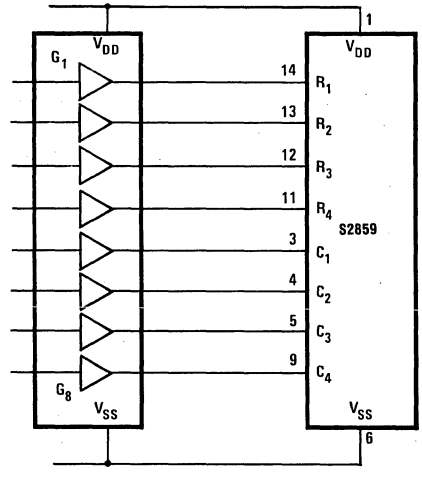
When a valid key closure is detected, the keyboard logic programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP ($V_{DD} - V_{REF}$) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

Table 1. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2859

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

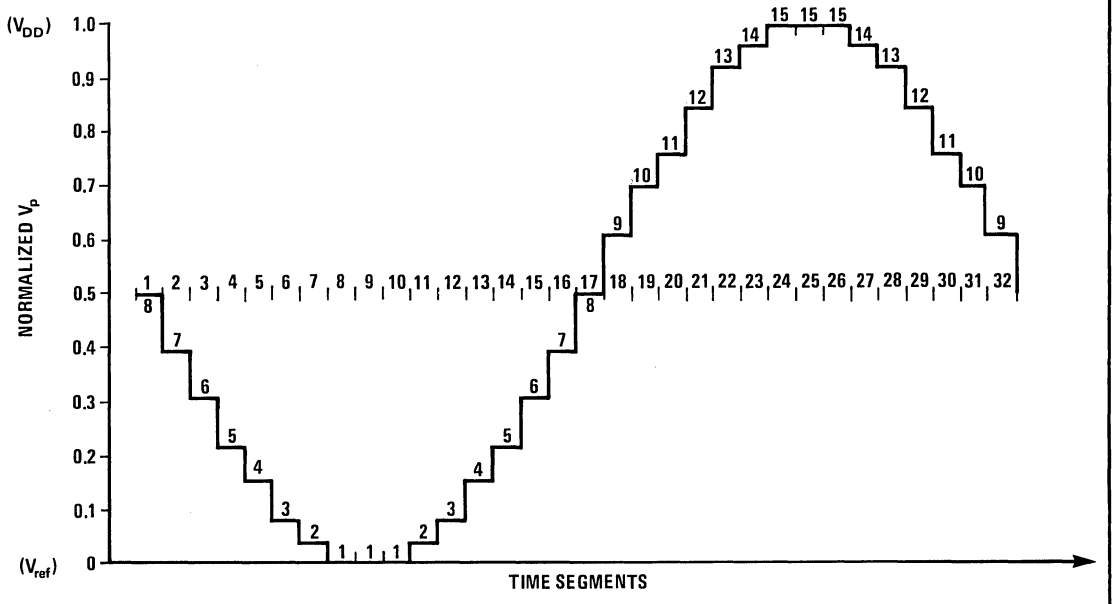
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S2859



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



The individual tones generated by the sinewave synthesizer are then linearly added and drive a Darlington NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Chip Enable

The S2859 has a chip enable input at pin 15. The chip enable for the S2859 is active "High". When the chip enable is "Low", the tone output goes to V_{SS}, the oscillator is inhibited and the MUTE outputs go into an open state.

Crystal Specification

A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3,579545MHz ±0.02%

R_S 100Ω, L_M=96MHY

C_M=0.02pF C_H=5pF C_L=12pF

MUTE Outputs

The S2859 has P-Channel buffers for the REC MUTE and XMIT MUTE outputs. With no keys depressed,

the MUTE outputs are open. When a key is depressed, the MUTE outputs go high. When chip enable is "Low" the MUTE outputs are forced in the "open" state regardless of the state of the keyboard.

Timing Sequence

Figure 4 illustrates the sequence in which the MUTE outputs operate when a key is depressed and released. When a valid key is depressed the REC MUTE output goes high first. The XMIT MUTE output goes high after a delay of about 1.6ms. This allows the receiver to be muted prior to the muting of the transmitter and generation of the dual tone. This prevents an undesirable click to be heard in the earpiece due to the momentary interruption of the direct current flowing through the network during the transition time when the transmitter is disconnected and dual tone applied. On release of the key the XMIT MUTE output goes open first, simultaneously the dual tone output is removed. The receiver at this time is still muted so that the click due to the momentary interruption of the direct current during the release of the key is not heard at the earpiece. The REC MUTE output goes open after a delay of about 1.7ms which reconnects the receiver to the network. The leading and trailing edge delays are guaranteed for supply voltages exceeding 3.0 volts. Below 3.0 volts the REC, XMIT MUTE outputs and tone output coincide with each other.

Amplitude/Distortion Measurements

Amplitude and distortion are two important parameters in all applications of the digital tone generator. Amplitude depends upon the operating supply voltage as well as the load resistance connected on the tone output pin. The on-chip reference circuit is fully operational when the supply voltage equals or exceeds 4 volts and as a consequence the tone amplitude is regulated in the supply voltage range above 4 volts. The load resistor value also controls the amplitude. If R_L is low the reflected impedance into the base of the output transistor is low and the tone output amplitude is lower. For R_L greater than 1KΩ the reflected impedance is sufficiently large and highest amplitude is produced. Individual tone amplitudes can be measured by applying the dual tone signal to a wave analyzer (H-P type 3580A) and amplitudes at the selected frequencies can be noted. This measurement also permits verification of the pre-emphasis between the individual frequency tones.

Distortion is defined as "the ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the power of the frequency pair". This ratio must be less than 10% or when expressed in dB must be lower than −20dB. (Ref. 1.) Voiceband is conventionally the frequency band of 300Hz to 3400Hz. Mathematically distortion can be expressed as:

$$\text{Dist.} = \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_N)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

where $(V_1) \ldots (V_N)$ are extraneous frequency (i.e., intermodulation and harmonic) components in the 500 Hz to 3400Hz band and V_L and V_H are the individual frequency components of the DTMF signal. The expression can be expressed in dB as:

$$\text{DIST}_{dB} = 20 \log \frac{\sqrt{(V_1)^2+(V_2)^2+\ldots+(V_N)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\{\log[(V_1{}^2+\ldots(V_N)^2] - \log[(V_L)^2+(V_H)^2]\} \ldots (1)$$

Table 2. Truth Table

INPUTS				OUTPUTS		
KEYS DEPRESSED	NUMBER OF COLUMNS LOW	NUMBER OF ROWS LOW	CHIP ENABLE	TONE	REC MUTE	XMIT MUTE
X	X	X	0	0	OPEN	OPEN
NONE	0	0	1	0	OPEN	OPEN
ONE	1	1	1	R+C	1	1
TWO OR MORE KEYS IN COLUMN	1	2 OR 3 OR 4	1	C	1	1
TWO OR MORE KEYS IN ROW	2 OR 3 OR 4	1	1	R	1	1
MULTI KEY	OTHER COMBINATIONS	OTHER COMBINATIONS	1	0	OPEN	OPEN
NOTE 1	4	3	1	R+C	A	B

X DON'T CARE A: 16 (ROW FREQ) B: 16 (COL FREQ)

NOTE 1: THIS MODE IS USED FOR TEST PURPOSES ONLY. IT IS INITIATED BY CONNECTING ALL COLUMN INPUTS AND THREE OUT OF FOUR ROW INPUTS TO V_{SS}. THE ROW INPUT THAT IS CONNECTED TO V_{DD} ROUTES THE CORRESPONDING 16 TIMES ROW FREQUENCY TO THE REC MUTE OUTPUT AND THE APPROPRIATE 16 TIMES COLUMN FREQUENCY (i.e., R_1 SELECTS C_1 etc.) TO THE XMIT MUTE OUTPUT.

Figure 4. Timing Diagram for (V_{DD}-V_{SS})≥3.5V

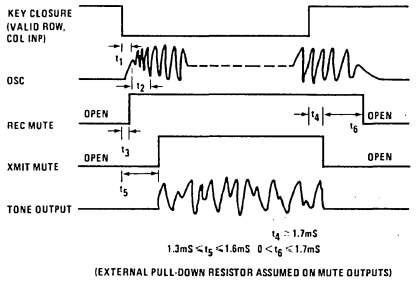
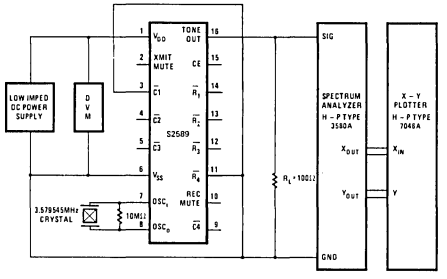


Figure 5. Test Circuit for Distortion Measurement



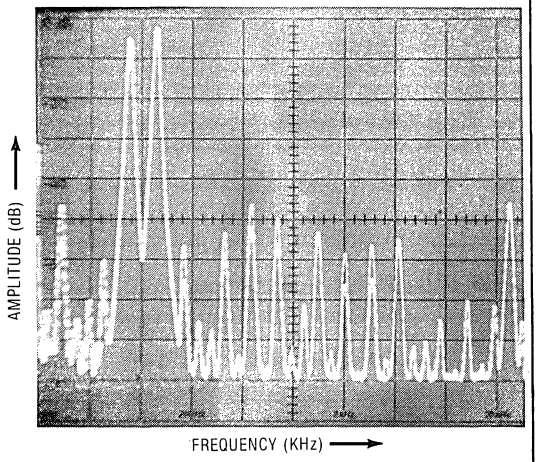
An accurate way of measuring distortion is to plot a spectrum of the signal by using a spectrum analyzer (H-P type 3580A) and an X-Y plotter (H-P type 7046A). Individual extraneous and signal frequency components are then noted and distortion is calculated by using the expression (1) above. Figure 6 shows a spectrum plot of a typical signal obtained from S2859 device operating from a fixed supply of 4VDC and $R_L = 100\Omega$ in the test circuit of Figure 5. Mathematical analysis of the spectrum shows distortion to be −30dB (3.2%). For quick estimate of distortion, a rule of thumb as outlined below can be used.

"As a first approximation distortion in dB equals the difference between the amplitude (dB) of the extraneous component that has the highest amplitude and the amplitude (dB) of the low frequency signal." This rule of thumb would give an estimate of −28dB as distortion for the spectrum plot of Figure 6 which is close to the computed result of −30dB.

In a telephone application amplitude and distortion are affected by several factors that are interdependent. For detailed discussion of the telephone application and other applications of the S2859 Tone Generator, refer to the applications note "Applications of Digital Tone Generator."

Ref. 1: Bell System Communications Technical Reference, PUB 47001, *"Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment,"* August 1976.

Figure 6. A Typical Spectrum Plot



DEVICE: S2859 — R_L = 100Ω
TEMP: ROOM — TEST CKT: FIGURE 5
(V_{DD} − V_{SS}): 4V DC FIXED — DUAL TONE: R_4, C_1
HORIZONTAL SCALE = 0.5KHz/DIV
VERTICAL SCALE = 10dB/DIV

DTMF TONE GENERATOR

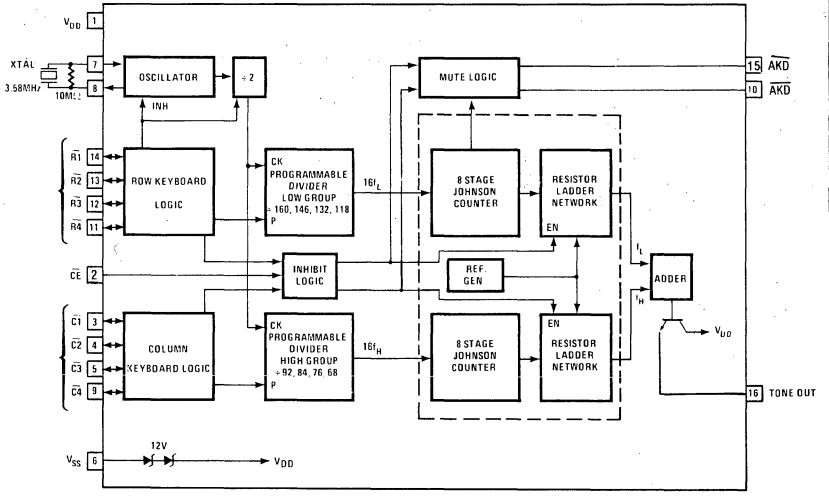
Features

- ☐ **Optimized for Constant Operating Supply Voltages, Typically 3.5V**
- ☐ **Tone Amplitude Stability is Within ±1.3 dB of Nominal Over Operating Temperature Range**
- ☐ **Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries**
- ☐ **Uses TV Crystal Standard (3.58 MHz) to Derive all Frequencies thus Providing Very High Accuracy and Stability**
- ☐ **Specifically Designed for Electronic Telephone Applications**
- ☐ **Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard with Common Terminal**
- ☐ **The Total Harmonic Distortion is Below Industry Specification**
- ☐ **Dual Tone as Well as Single Tone Capability**

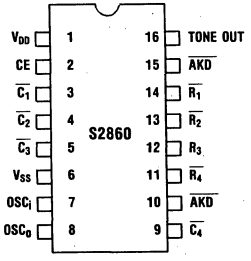
General Description

The S2860 Digital Tone Generator is specifically designed to implement a dual tone telephone dialing system in applications requiring fixed supply operation and high stability tone output level, making it well suited for electronic telephone applications. The device can interface directly to a standard pushbutton telephone keyboard or X-Y keyboard with common terminal connected to V_{SS} and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is very stable over the operating temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage ($V_{DD} - V_{SS}$)	+10.5V
Operating Temperature	−30 °C to +70 °C
Storage Temperature	−55 °C to +125 °C
Power Dissipation at 25 °C	500mW
Input Voltage	$-0.6 \leq V_{IN} \leq V_{DD} + 0.6$
Input/Output Current (except tone output)	15mA
Tone Output Current	50mA

Electrical Characteristics:

(Specifications apply over the operating temperature range of −30 °C to 70 °C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions			($V_{DD} - V_{SS}$) Volts	Min.	Typ.	Max.	Units
	Supply Voltage							
V_{DD}	Tone Out Mode (Valid Key Depressed)				3.0	–	10.0	V
	Non Tone Out Mode (AKD Outputs toggle with key depressed)				1.8	–		V
V_Z	Internal Zener Diode Voltage, I_Z = 5mA			–	–	12.0	–	V
	Supply Current							
I_{DD}	Standby (No Key Selected, Tone and AKD Outputs Unloaded)			3.5 10.0	– –	1 5	20 100	μA μA
	Operating (One Key Selected, Tone and AKD Outputs Unloaded)			3.5 10.0	– –	.9 3.6	1.25 5	mA mA
	Tone Output							
V_{OR}	Dual Tone	Row	R_L = 10k Ω	3.5	305	350	412	mVrms
	Mode Output	Tone	R_L = 1k Ω	3.5	272	350	412	mVrms
dB_{CR}	Ratio of Column to Row Tone			3.0 – 10.0	1.0	2.0	3.0	dB
%DIS	Distortion			3.0 – 10.0	–	–	10	%
	AKD Outputs							
I_{OH}	Output Sink Current		V_{OL}=.7V	3.5	0.1	1.0	–	mA
	OSCILLATOR Input/Output							
I_{OL}	One Key Selected		V_{OL} = 0.5V	3.0	0.21	0.52	–	mA
	Output Sink Current		V_{OL} = 0.5V	10.0	0.80	2.1	–	mA
I_{OH}	Output Source Current		V_{OH} = 2.5V	3.0	0.13	0.31	–	mA
	One Key Selected		V_{OH} = 9.5V	10.0	0.42	1.1	–	mA
I_{IL}	Input Current Leakage Sink Current One Key Selected		V_{IL} = 10.0V	10.0	–	–	1.0	μA
I_{IH}	Leakage Source Current One Key Selected		V_{IH} = 0.0V	10.0	–	–	1.0	μA
I_{IL}	Sink Current		V_{IL} = 0.5V	3.0	24	58	–	μA
	No Key Selected		V_{IL} = 0.5V	10.0	27	66	–	μA

**Distortion measured in accordance with the specifications described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair".*

Electrical Characteristics: (Continued)

Symbol	Parameter/Conditions		(V_{DD} – V_{SS}) Volts	Min.	Typ.	Max.	Units
	OSCILLATOR Input/Output (Continued)						
t_{START}	Oscillator Time		3.0 10.0	– –	2 0.25	5 0.75	ms ms
$C_{I/O}$	Input/Output Capacitance		3.0 10.0	– –	12 10	16 14	pF pF
	Row, Column and Chip Enable Inputs						
V_{IL}	Input Voltage, Low		–	V_{SS}–0.6		.2(V_{DD} –V_{SS})	V
V_{IH}	Input Voltage, High		–	.8(V_{DD} –V_{SS})	–	V_{DD}+0.6	V
I_{IH}	Input Current	V_{IH} = 0.0V	3.0	20	60	100	μA
	(Pull up)	V_{IH} = 0.0V	10.0	66	200	336	μA

Oscillator

The S2860 contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect a 10MΩ feedback resistor and the standard 3.58MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row input is activated. The reference frequency is divided by 2 and then drives two sets of programmable dividers, the high group and the low group.

Crystal Specification

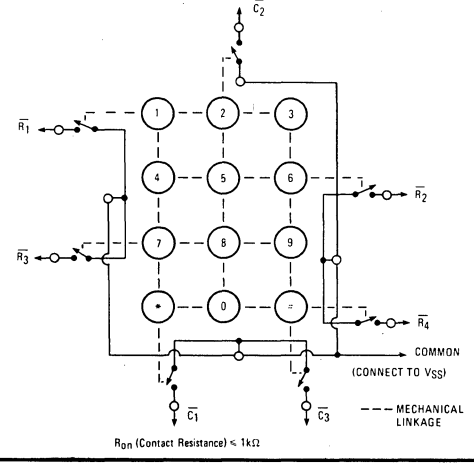
A standard television color burst crystal is specified to have much tighter tolerance than necessary for tone generation application. By relaxing the tolerance specification the cost of the crystal can be reduced. The recommended crystal specification is as follows:

Frequency: 3,579545MHz ±0.02%
R_S 100Ω, L_M=96MHy
C_M=0.02pF C_H=5pF C_L=12pF

Keyboard Interface

The S2860 can interface with either the standard telephone pushbutton keyboard (see Figure 1) or an X-Y keyboard with common. The common of the keyboard must be connected to V_{SS}.

Figure 1. Standard Telephone Push Button Keyboard



Logic Interface

The S2860 can also interface with CMOS logic outputs directly. (See Figure 2.) The S2860 requires active "Low" logic levels. Low levels on a row and a column input corresponds to a key closure. The pull-up resistors present on the row and column inputs are in the range of 33kΩ —150kΩ.

Tone Generation

When a valid key closure is detected, the keyboard logic

Tone Generation (Continued)

programs the high and low group dividers with appropriate divider ratios so that the output of these dividers cycle at 16 times the desired high group and low group frequencies. The outputs of the programmable dividers drive two 8-stage Johnson counters. The symmetry of the clock input to the two divide by 16 Johnson counters allows 32 equal time segments to be generated within each output cycle. The 32 segments are used to digitally synthesize a stair-step waveform to approximate the sinewave function (see Figure 3). This is done by connecting a weighted resistor ladder network between the outputs of the Johnson counter, V_{DD} and V_{REF}. V_{REF} closely tracks V_{DD} over the operating voltage and temperature range and therefore the peak-to-peak amplitude VP (V_{DD} -V_{REF}) of the stair-step function is fairly constant. V_{REF} is so chosen that VP falls within the allowed range of the high group and low group tones.

The individual tones generated by the sinewave synthesizer are then linearly added and drive an NPN transistor connected as an emitter follower to allow proper impedance transformation at the same time preserving signal level. This allows the device to drive varying resistive loads without significant variation in tone amplitude. For example, a load resistor change from 10kΩ to 1kΩ causes a decrease in tone amplitude of less than 1dB.

Dual Tone Mode

When one row and one column is selected dual tone output consisting of an appropriate low group and high group tone is generated. If two digit keys, that are not either in the same row or in the same column, are depressed, the dual tone mode is disabled and no output is provided.

Single Tone Mode

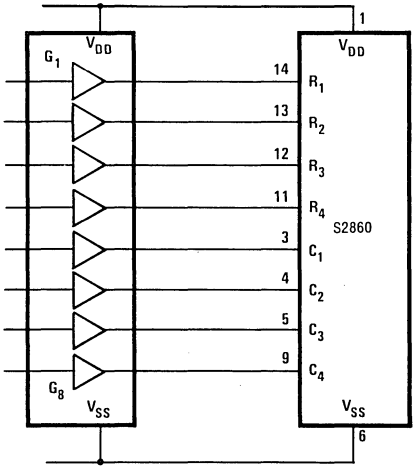
Single tones either in the low group or the high group can be generated as follows. A low group tone can be generated by depressing two digit keys in the appropriate row. A high group tone can be generated by depressing two digit keys in the appropriate column, i.e., selecting the appropriate column input and two row inputs in that column.

Table 1. Comparisons of Specified Vs. Actual Tone Frequencies Generated by S2859

ACTIVE INPUT	OUTPUT FREQUENCY Hz		%ERROR
	SPECIFIED	ACTUAL	SEE NOTE
R1	697	699.1	+0.30
R2	770	766.2	−0.49
R3	852	847.4	−0.54
R4	941	948.0	+0.74
C1	1209	1215.9	+0.57
C2	1336	1331.7	−0.32
C3	1477	1471.9	−0.35
C4	1633	1645.0	+0.73

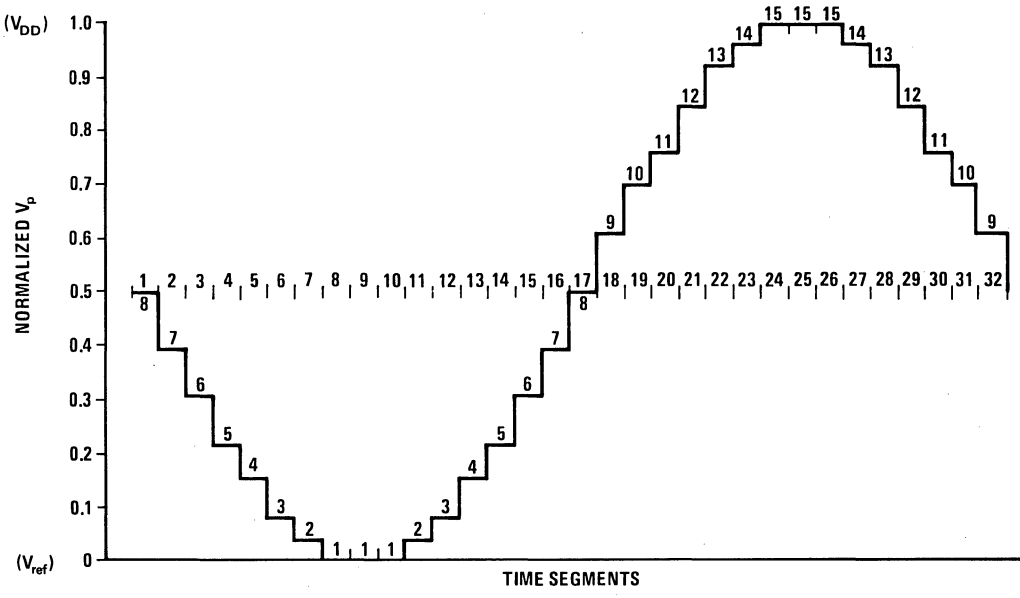
NOTE: %ERROR DOES NOT INCLUDE OSCILLATOR DRIFT

Figure 2. Logic Interface for Keyboard Inputs of the S2860



G1 THRU G8 ANY TYPE CMOS GATE

Figure 3. Stairstep Waveform of the Digitally Synthesized Sinewave



Reference Voltage

The structure of the reference voltage employed in the S2860 is shown in Figure 4. It has the following characteristics:

a) V_{REF} is proportional to the supply voltage. Output tone amplitude, which is a function of ($V_{DD} - V_{REF}$), increases with supply voltage (Figure 5)

b) The temperature coefficient of V_{REF} is low due to a single V_{BE} drop. Use of a resistive divider also provides an accuracy of better than 1%. As a result, tone amplitude variations over temperature and unit to unit are held to less than ±1.3dB over nominal.

c) Resistor values in the divider network are so chosen that V_{REF} is above the V_{BE} drop of the tone output transistor even at the low end of the supply voltage range. The tone output clipping at low supply voltages is thus eliminated, which improves distortion performance.

AKD (Any Key Down or Mute) Outputs

The AKD outputs (pin 15 and pin 10) are identical and consist of open drain N channel devices (see Figure 6.)

When no key is depressed the AKD outputs are open. When a key is depressed the AKD outputs go to V_{SS}. The devices are large enough to sink a minimum of 100μA with voltage drop of 0.2V at a supply voltage of 3.5V.

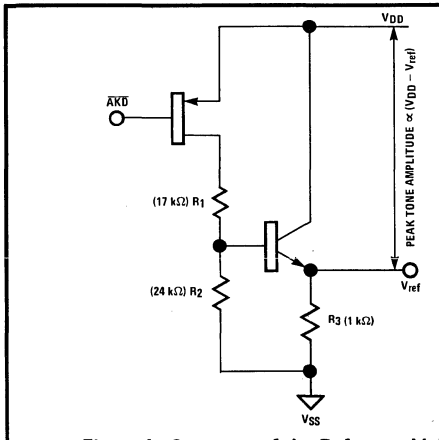


Figure 4. Structure of the Reference Voltage

Figure 5. Typical Tone Output Amplitude Vs Supply Voltage ($R_L = 10k$)

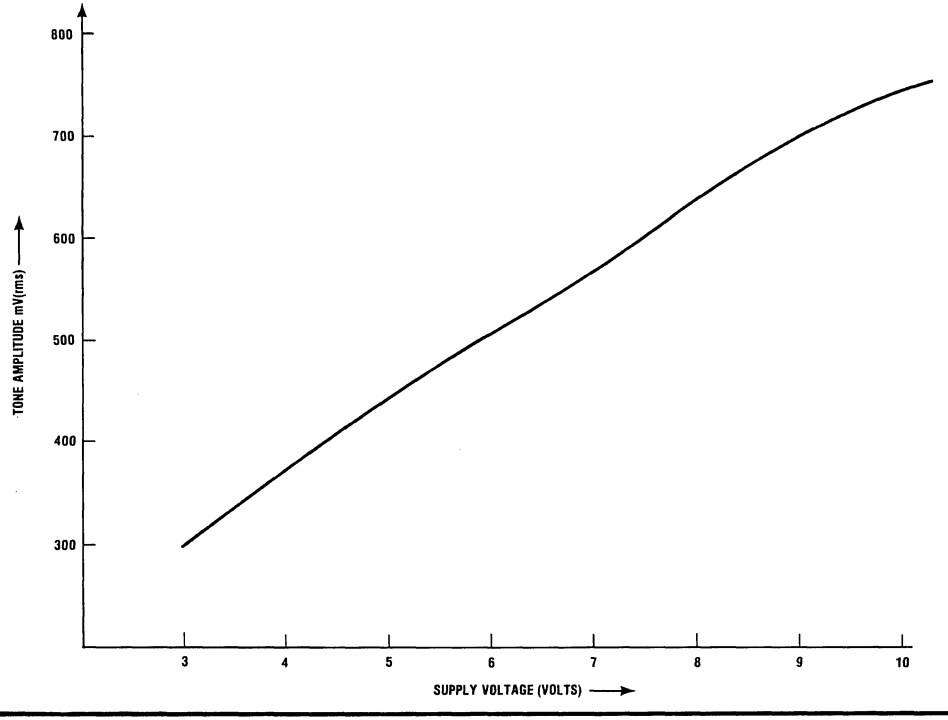
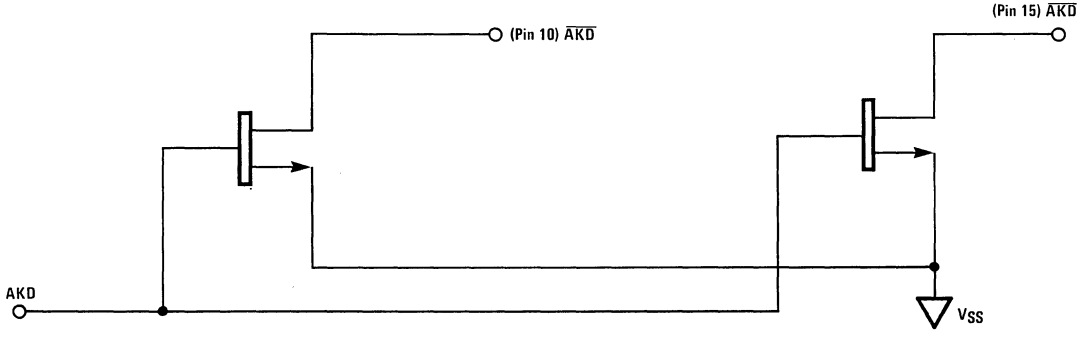


Figure 6. AKD Output Structure



AMERICAN MICROSYSTEMS, INC.

S2560A

PULSE DIALER

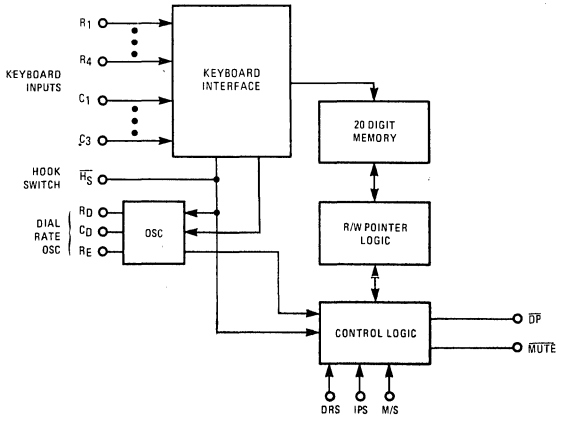
Features

- ☐ **Low Voltage CMOS Process for Direct Operation From Telephone Lines**
- ☐ **Inexpensive R-C Oscillator Design Provides Better than ±5% Accuracy Over Temperature and Unit to Unit Variations**
- ☐ **Dialing Rate Can Be Varied By Changing the Dial Rate Oscillator Frequency**
- ☐ **Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without Changing Oscillator Components**
- ☐ **Two Selections of Mark/Space Ratios (33-1/3/66-2/3 or 40/60)**
- ☐ **Twenty Digit Memory for Input Buffering and for Redial With Access Pause Capability**
- ☐ **Mute and Dial Pulse Drivers on Chip**
- ☐ **Accepts DPCT Keypad with Common Arranged in a 2 of 7 Format; Also Capable of Interface to SPST Switch Matrix**

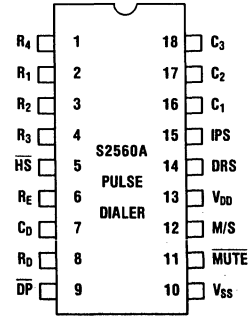
General Description

The S2560A Pulse Dialer is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered. IDP is scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD}$ to $V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	$V_{DD}-V_{SS}$ (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHDP}	$\overline{DP}$ Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	$\overline{MUTE}$ Output Low Current (Sink)	3.5	125		µA	V_{OUT} = 0.4V
I_{OHM}	$\overline{MUTE}$ Output High Current (Source)	1.5 3.5	20 125		µA µA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low Current (Sink)	1.5	20		µA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High Current (Source)	1.5	20		µA	V_{OUT} = 1V
V_{DR}	Data Retention Voltage		1.0		V	"On Hook" $\overline{HS}$ = V_{DD}. Keyboard open, all other input pins to V_{DD} or V_{SS}
I_{DD}	Quiescent Current	1.0		750	nA	
I_{DD}	Operating Current	1.5 3.5		100 500	µA µA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$ = V_{SS} ("Off Hook") Keyboard processing and dial pulsing at 10 pps at conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leq R_D \leq 750K\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD}-V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD}-V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded. When power is first applied to the device, the device should be in "On Hook" condition ($\overline{HS}$=1). This is necessary because there is no internal power or reset on chip and for proper operation all internal latches must come up in a known state. In applications where the device is hard wired in "Off Hook" ($\overline{HS}$)=0) condition, a momentary "On Hook" condition can be presented to the device during power up by use of a capacitor resistor network as shown in Figure 6.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components: two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10 pps the oscillator should be adjusted to 2400 Hz. Typical values of external components for this are R_D and R_E=750kΩ and C_D=270 pF. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a ±10% tolerance of the dialing rate in the system.

Keyboard Interface (2560A)

The S2560A employs a scanning technique to determine a key closure. This permits interface to a DPCT keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2) and interface to a SPST switch matrix (Figure 7). A high level on the appropriate row and column inputs constitutes a key closure for logic interface. When using a SPST switch matrix, it is necessary to add small capacitors (30 pF) from the column inputs to V_{SS} to insure that the oscillator is shut off after a key is released or after the dialing is complete.

OFF Hook Operation: The device is continuously powered through a 150kΩ resistor during Off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during the pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

ON Hook Operation: The device is continuously powered through a 10—20MΩ resistor during the ON hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20 pps can be achieved. Dialing rates of 7 and 14 pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20 pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14 pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10 pps an IDP of 800ms is obtained and at 20 pps an IDP of 400ms is obtained.

The user can enter a number up to 20 digits long from a standard 3x4 double contact keypad with common (Figure 1). It is also possible to use a logic interface as shown in Figure 2 for number entry. Antibounce protection circuitry is provided on chip (min. 20ms.) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed twenty.

Auto Dialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

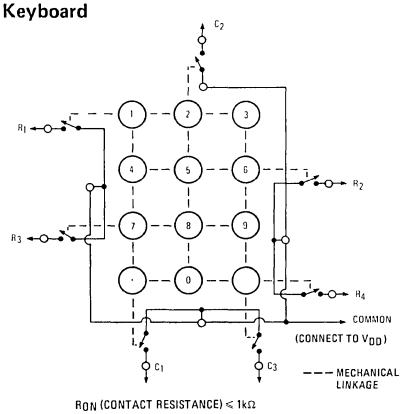
Table 1. S2560A Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 3. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IPS)	1	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceding the first dialed pulse is an inter-digit time equal to the selected IDP. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	1	A programmable line allows selection of two different output rates such as 7 or 14 pps, 10 or 20 pps, etc. See Tables 2 and 3.
Mark/Space (MS)	1	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{\text{MUTE}}$)	1	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.

Table 1. (Continued)

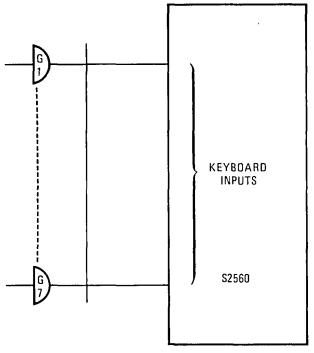
Pin	Number	Function
Dial Pulse Out ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator	3	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{HS}$)	1	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.
	18	

Figure 1. Standard Telephone Pushbutton Keyboard



R_{ON} (CONTACT RESISTANCE) $\leq 1k\Omega$

Figure 2. Logic Interface For the S2560



G1 through G7 any CMOS type logic gates

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Figure 3. Timing

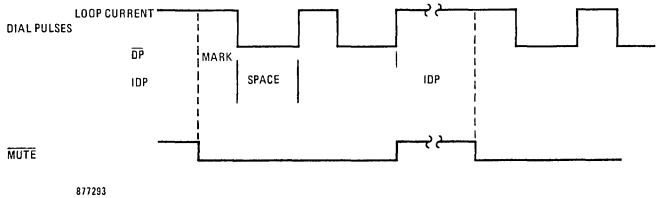

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Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
(f_d/240)/ (f_d/120)	f_d				(f_d/240)	(f_d/120)	$\left(\frac{1920}{f_i} \times 10^3\right)$	$\left(\frac{960}{f_i} \times 10^3\right)$

Notes:

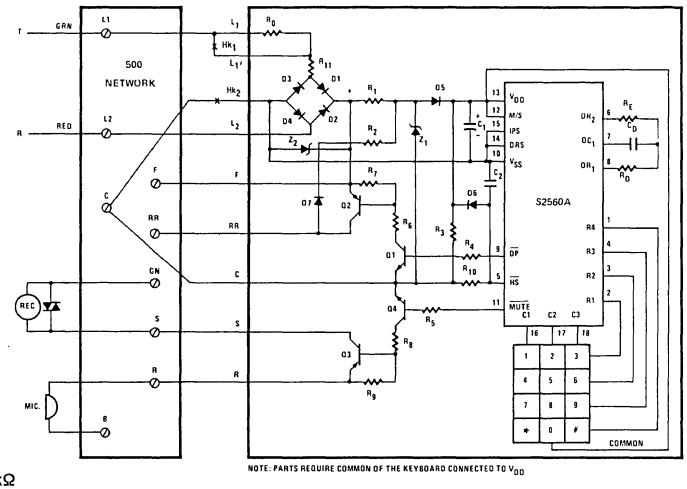
1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10 pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14 pps, and IDP of either 1142ms or 571ms can be selected.

Table 3.

Function	Pin Designation	Input Logic Level	Selection
Dial Pulse Rate Selection	DRS	V_{SS} V_{DD}	(f/240) pps (f/120) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	$\frac{960}{f}$ s $\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS} V_{DD}	33-1/3/66-2/3 40/60
On Hook/Off Hook	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off Hook

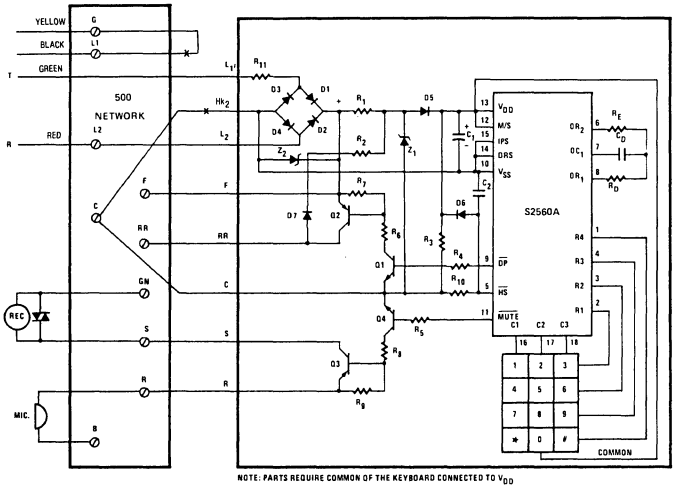
Note: f is the oscillator frequency and is determined as shown in Figure 5.

Figure 4. Pulse Dialer Circuit with Redial



$R_0 = 10\text{-}20M\Omega$, $R_1 = 150k\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$, $R_{10} = 47k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$, $R_{11} = 20\Omega$, .2W
$Z_1 = 3.9V$, D_1—$D_4 = IN4004$, D_5, D_6, $D_7 = IN914$, $C_1 = 15\mu F$
$R_E = R_D = 750k\Omega$, $C_D = 270pF$, $C_2 = 0.01\mu F$
Q_1, $Q_4 = 2N5550$ TYPE Q_2, $Q_3 = 2N5401$ TYPE
$Z_2 = IN5379$ 110V ZENER OR 2XIN4758

Figure 5. Pulse Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



$R_1 = 10\text{-}20M\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$
$R_{10} = 47k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—$D_4 = IN4004$
D_5, D_6, $D_7 = IN914$, $C_1 = 15\mu F$
R_E, $R_D = 750k\Omega$, $C_D = 270pF$
$C_2 = 0.01\mu F$, Q_1, $Q_4 = 2N5550$
Q_2, $Q_3 = 2N5401$
$Z_2 = 150V$ ZENER OR VARISTOR TYPE GE MOV150

Figure 6. Circuit for Applying Momentary "On Hook" Condition During Power Up

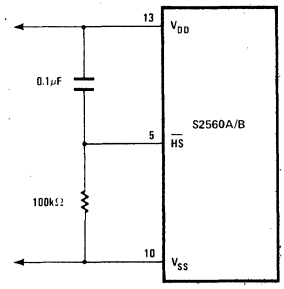
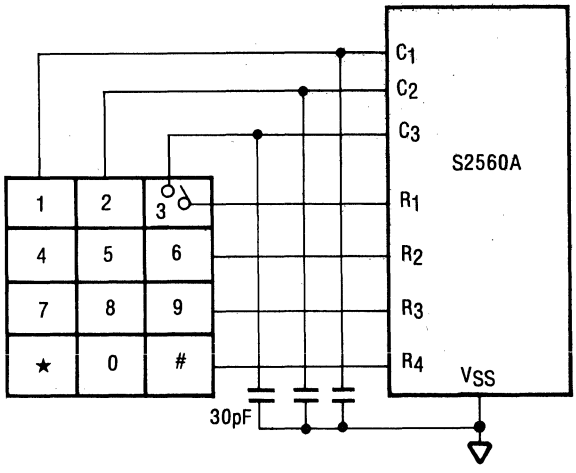


Figure 7. SPST Switch Matrix Interface

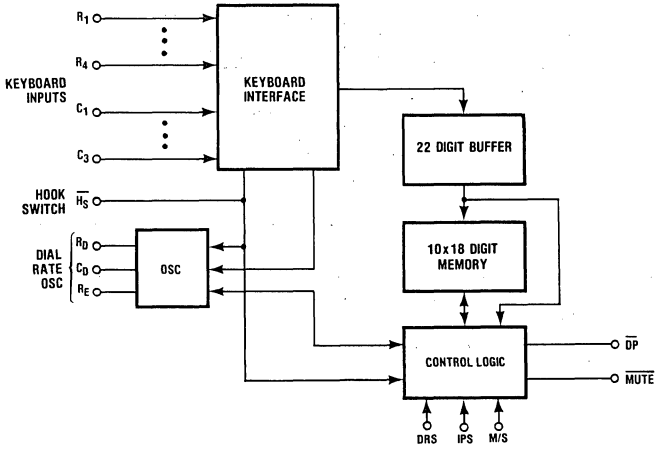


S25610 SINGLE CHIP REPERTORY DIALER

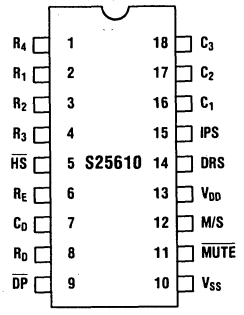
Features:

- ☐ Complete Pin Compatibility With S2560A Pulse Dialer Allowing Easy Upgrading of Existing Designs.
- ☐ Ten 18-Digit Number Memories Plus Last Number Redial (22 Digit) Memory On Chip.
- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines.
- ☐ Inexpensive R-C Oscillator Design With Accuracy Better Than ±5% Over Temperature and Unit-Unit Variations.
- ☐ Independent Select Inputs for Variation of Dialing Rates (10pps/20pps), Mark/Space Ratio (33⅓ - 66⅔/40-60), Interdigit Pause (400ms/800ms).
- ☐ Can Interface With Inexpensive XY Matrix or Standard 2 of 7 Keyboard With Common. Also Capable of Logic Interface (Active High).
- ☐ Mute and Pulse Drivers On Chip.
- ☐ Call Disconnect by Pushing * and # Keys Simultaneously.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	+5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics:

Specifications apply over the operating temperature and $1.5V \leq V_{DD}$ to $V_{SS} \leq 3.5V$ unless otherwise specified.

Symbol	Parameter	$V_{DD}-V_{SS}$ (Volts)	Min.	Max.	Units	Conditions
	Operating Voltage					
V_{DD}	Data Retention		1.0		V	On Hook, ($\overline{HS}=V_{DD}$)
V_{DD}	Non Dialing State		1.5	3.5	V	Off Hook, Oscillator Not Running
V_{DD}	Dialing State		2.0	3.5	V	Off Hook, Oscillator Running
	Operating Current					
I_{DD}	Data Retention	1.0		750	nA	On Hook, ($\overline{HS}=V_{DD}$)
I_{DD}	Non Dialing	1.5		10	μA	Off Hook ($\overline{HS}=V_{DD}$), Oscillator Not Running, Outputs Not Loaded.
I_{DD}	Dialing	2.0 3.5		100 500	μA μA	Off Hook, Oscillator Running, Outputs Not Loaded
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	$\overline{DP}$ Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	$\overline{MUTE}$ Output Low Current (Sink)	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	$\overline{MUTE}$ Output High Current (Source)	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	2.0 to 2.75 2.75 to 3.5	−3 −3	+3 +3	% %	Fixed R-C oscillator components $50K\Omega \leq R_D \leq 750K\Omega$; $100pF \leq C_D{}^* \leq 1000pF$; $750k\Omega \leq R_E \leq 5M\Omega$ *300pF most desirable value for C_D
	Input Voltage Levels					
V_{IH}	Logical "1"		80% of ($V_{DD}-V_{SS}$)	V_{DD} +0.3	V	
V_{IL}	Logical "0"		V_{SS} −0.3	20% of ($V_{DD}-V_{SS}$)	V	
C_{IN}	Input Capacitance Any Pin			7.5	pF	

Operating Characteristics

Normal Dialing

Off Hook, [D1] , ------- [Dn]

Dial pulsing to start as soon as first digit is entered (debounced and detected on chip). Pause may be entered in the dialing sequence by pressing the "#" key. Total number of digits entered not to exceed 22. Numbers exceeding 22 digits can be dialed but only after the first 22 digits have been completely dialed out. In this case redialing function is inhibited.

Storing of a Telephone Number(s)

Numbers can be stored as follows:

Off Hook, [*], [D1] ,---- [Dn] , [*], [LOC]

[*], [D1] , --- [Dn] , [*], [LOC]

etc.

Earpiece is muted in this operation to alert the user that a store operation is underway.

Repertory Dialing

Off Hook, [#], [LOC]

Numbers can be cascaded repeating [#], [LOC] sequence after completion of dialing of present sequence. If an access pause has been stored in "LOC", dialing will halt until the "#" key is pushed again.

Redialing

Last number dialed can be redialed as follows: Off Hook, [#] , [#] . Last number for this purpose is defined as the last number remaining in the buffer. Access pause is terminated by pushing the "#" key as usual.

Functional Description

The pin function designations are outlined in Table 1.

Oscillator

The device contains an oscillator circuit that requires three external components; two resistors (R_D and R_E) and one capacitor (C_D). All internal timing is derived from this master time base. To eliminate clock interference in the talk state, the oscillator is only enabled during key closures and during the dialing state. It is disabled at all other times including the "on hook" condition. For a dialing rate of 10pps the oscillator should be adjusted to 2400Hz. Typical values of external components for this are R_D, $R_E = 750k\Omega$ and $C_D = 270pF$. It is recommended that the tolerance of resistors to be 5% and capacitor to be 1% to insure a ±10% tolerance of the dialing rate in the system.

Keyboard Interface (S25610)

The S25610 employs a scanning technique to determine a key closure. This permits interface to a DPCT (Double Pole Common Terminal) keyboard with common connected to V_{DD} (Figure 1), logic interface (Figure 2),or a XY matrix. A high level on the appropriate row and column inputs constitutes a key closure for logic interface.

Off Hook Operations: The device is continuously powered through a 150kΩ resistor during off hook operation. The DP output is normally high and sources base drive to transistor Q_1 to turn ON transistor Q_2. Transistor Q_2 replaces the mechanical dial contact used in the rotary dial phones. Dial pulsing begins when the user enters a number through the keyboard. The $\overline{DP}$ output goes low shutting the base drive to Q_1 OFF causing Q_2 to open during this pulse break. The $\overline{MUTE}$ output also goes low during dial pulsing allowing muting of the receiver through transistors Q_3 and Q_4. The relationship of dial pulse and mute outputs are shown in Figure 3.

On Hook Operation: The device is continuously powered through a 10-20MΩ resistor during the on hook operation. This resistor allows enough current from the tip and ring lines to the device to allow the internal memory to hold and thereby providing storage of the last number dialed. DP and mute outputs are low in the on hook state.

The dialing rate is derived by dividing down the dial rate oscillator frequency. Table 2 shows the relationship of the dialing rate with the oscillator frequency and the dial rate select input. Different dialing rates can be derived by simply changing the external resistor value. The dial rate select input allows changing of the dialing rate by a factor of 2 without the necessity of changing the external component values. Thus, with the oscillator adjusted to 2400Hz, dialing rates of 10 or 20pps can be achieved. Dialing rates of 7 and 14pps similarly can be achieved by changing the oscillator frequency to 1680Hz.

The Inter-Digit Pause (IDP) time is also derived from the oscillator frequency and can be changed by a factor of 2 by the IDP select input. With IDP select pin wired to V_{SS}, an IDP of 800ms is obtained for dial rates of 10 and 20pps. IDP can be reduced to 400ms by wiring the IDP select pin to V_{DD}. At dialing rates of 7 and 14pps, IDP's of 1143ms and 572ms can be similarly obtained. If the IDP select pin is connected to the dial rate select pin, the IDP is scaled to the dial rate such that at 10pps an IDP of 800ms is obtained and at 20pps an IDP of 400ms is obtained.

The user can enter a number up to 22 digits long from a standard 3×4 XY matrix keypad (Figure 1). It is also possible to use a logic interface or a keyboard with common (Figure 2) for number entry. Antibounce protection circuitry is provided on chip (min. 9ms) to prevent false entry.

Any key depressions during the on-hook condition are ignored and the oscillator is inhibited. This insures that the current drain in the on-hook condition is very low and used to retain the memory.

Normal Dialing

The user enters the desired numbers through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20pps. The number entered is retained in the memory for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed 22.

Redialing

The last number dialed is retained in the memory and therefore can be redialed out by going off hook and pressing the "#" key twice. Dial pulsing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. In such a case, the dial pulsing will stop and will resume again only after the user pushes the "#" key.

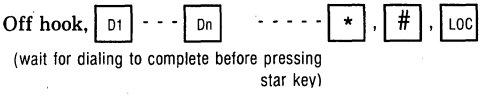
Repertory Dialing

Dialing of a number stored in memory is initiated by going OFF hook and pushing the # key followed by the single digit address. Numbers can be cascaded after dialing of the first number is completed.

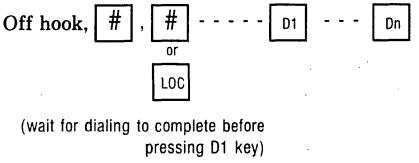
Special Sequences

There are some special sequences that provide for mixed dialing or other features such as call disconnect, redial inhibit or memory clear as follows:

a. Normal dialing followed by repertory dialing



b. Normal dialing after repertory dialing or redialing

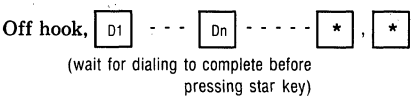


c. Disconnecting call

Off hook,- - - - -, * #

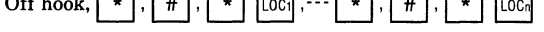
Pushing * and # keys simultaneously causes DP and mute outputs to go low and remain low until the keys are released. This causes a break in the line. If the keys are held down for a sufficiently long time (approx. 400ms), the call will be disconnected and new dial tone will be heard upon release of the keys. This feature is convenient when disconnecting calls by the normal method, i.e., hanging up the phone or depressing hookswitch is cumbersome.

d. Inhibiting future redialing of a normally dialed number



Pushing * key twice after normal dialing is completed instructs the device to clear the redial buffer.

e. To clear a memory location(s)



Essentially this operation is equivalent to storing a pause in the memory location.

The various operating characteristics are summarized in Table 4.

Figure 1. SPST Matrix Keyboard Arranged in a Row, Column Format

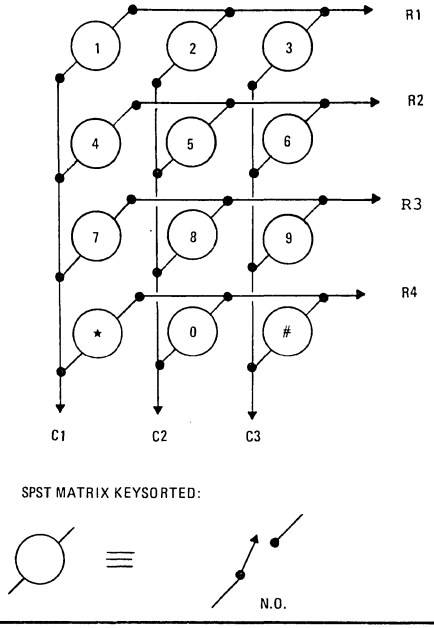


Figure 2. Standard Telephone Pushbutton Keyboard

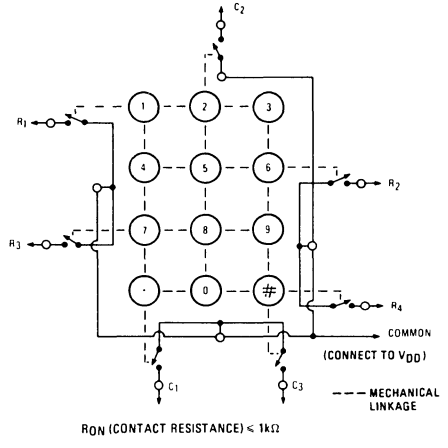


Figure 3. Timing (Off Hook)

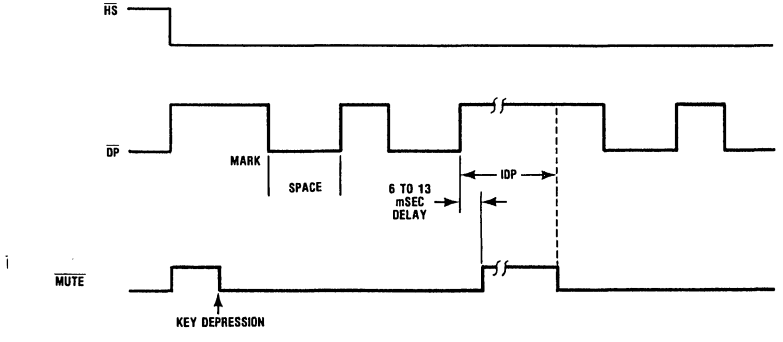


Table 1. S25610 Pin/Function Descriptions

Pin	Number	Function
Keyboard (R_1, R_2, R_3, R_4, C_1, C_2, C_3)	7	These are 4 row and 3 column inputs from the keyboard contacts. These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect with each other. A logic interface is also possible as shown in Figure 3. Active pull up and pull down networks are present on these inputs when the device begins keyboard scan. The keyboard scan begins when a key is pressed and starts the oscillator. Debouncing is provided to avoid false entry (typ. 20ms).
Inter-Digit Pause Select (IPS)	1	One programmable line is available that allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Two pauses either 400ms or 800ms are available for dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Dial Rate Select (DRS)	1	A programmable line allows selection of two different output rates such as 7 or 14pps, 10 or 20pps, etc. See Tables 2 and 3.
Mark/Space (MS)	1	This input allows selection of the mark/space ratio, as per Table 3.
Mute Out ($\overline{\text{MUTE}}$)	1	A pulse is available that can provide a drive to turn on an external transistor to mute the receiver during the dial pulsing.
Dial Pulse Out ($\overline{\text{DP}}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space" and "high" otherwise.
Dial Rate Oscillator	3	These pins are provided to connect external resistors R_D, R_E and capacitor C_D to form an R-C oscillator that generates the time base for the Key Pulser. The output dialing rate and IDP are derived from this time base.
Hook Switch ($\overline{\text{HS}}$)	1	This input detects the state of the hook switch contact; "off hook" corresponds to V_{SS} condition.
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 3.5V.

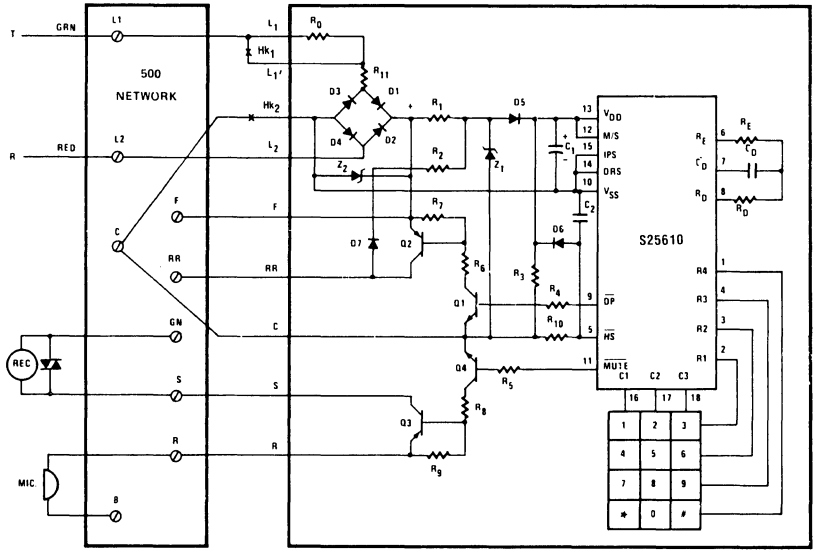
Table 2. Table for Selecting Oscillator Component Values for Desired Dialing Rates and Inter-Digit Pauses

Dial Rate Desired	Osc. Freq. (Hz)	R_D (kΩ)	R_E (kΩ)	C_D (pF)	Dial Rate (pps)		IDP (ms)	
					$DRS=V_{SS}$	$DRS=V_{DD}$	$IPS=V_{SS}$	$IPS=V_{DD}$
5.5/11	1320	Select components in the ranges indicated in table of electrical specifications.			5.5	11	1454	727
6/12	1440				6	12	1334	667
6.5/13	1560				6.5	13	1230	615
7/14	1680				7	14	1142	571
7.5/15	1800				7.5	15	1066	533
8/16	1920				8	16	1000	500
8.5/17	2040				8.5	17	942	471
9/18	2160				9	18	888	444
9.5/19	2280				9.5	19	842	421
10/20	2400	750	750	270	10	20	800	400
$(f_d/240)/(f_d/120)$	f_d				$(f_d/240)$	$(f_d/120)$	$\frac{1920}{f_i} \times 10^3$	$\frac{960}{f_i} \times 10^3$

Notes:

1. IDP is dependent on the dialing rate selected. For example, for a dialing rate of 10pps, an IDP of either 800ms or 400ms can be selected. For a dialing rate of 14pps, an IDP of either 1142ms or 571ms can be selected.

Figure 4. Repertory Dialer Circuit with Redial



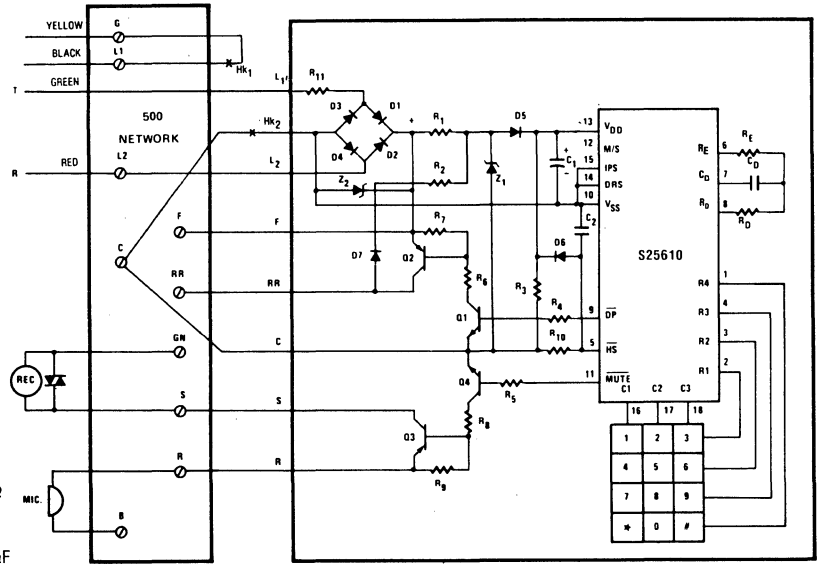
$R_0 = 10\text{-}20M\Omega$, $R_1 = 150k\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$, $R_{10} = 47k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—$D_4 = IN4004$, D_5, D_6, $D_7 = IN914$, $C_1 = 15\mu F$
$R_E = R_D = 750k\Omega$, $C_D = 270pF$, $C_2 = 0.01\mu F$
Q_1, $Q_4 = 2N5550$ TYPE Q_2, $Q_3 = 2N5401$ TYPE
$Z_2 = IN5379$ 110V ZENER OR 2XIN4758

Table 3

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS}	(f/240) pps
		V_{DD}	(f/120) pps
Inter-Digit Pause Selection	IPS	V_{DD}	$\frac{960}{f}$ s
		V_{SS}	$\frac{1920}{f}$ s
Mark/Space Ratio	M/S	V_{SS}	33-1/3/66-2/3
		V_{DD}	40/60
OnHook/Off Hook	$\overline{HS}$	V_{DD}	On Hook
		V_{SS}	Off hook

*Note: f is the oscillator frequency and is determined as shown in Figure 5.

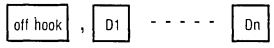
Figure 5. Repertory Dialer Circuit with Redial (Single Hook Switch Contact Application for PABX)



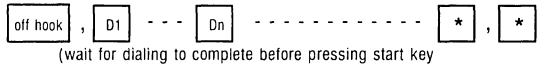
$R_1 = 10\text{-}20M\Omega$, $R_2 = 2k\Omega$
$R_3 = 470k\Omega$, R_4, $R_5 = 10k\Omega$
R_6, $R_8 = 2k\Omega$, R_7, $R_9 = 30k\Omega$
$R_{10} = 47k\Omega$, $R_{11} = 20\Omega$, 2W
$Z_1 = 3.9V$, D_1—D_4 = IN4004
D_5, D_6, D_7 = IN914, $C_1 = 15\mu F$
R_E, $R_D = 750k\Omega$, $C_D = 270pF$
$C_2 = 0.01\mu F$, Q_1, Q_4 = 2N5550
Q_2, Q_3 = 2N5401
Z_2 = 150V ZENER OR VARISTOR TYPE GE MOV150

Table 4. Summary of Operating Characteristics

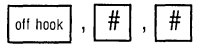
1) Normal Dialing:



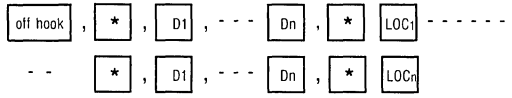
2) Inhibit Redialing:



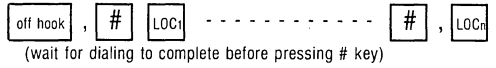
3) Redialing:



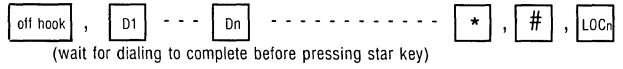
4) Storing of Number(s):



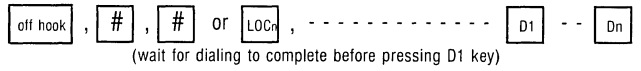
5) Repertory Dialing:



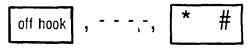
6) Normal Dialing + Repertory Dialing:



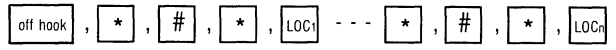
7) Recall + Normal Dialing:



8) Call Disconnect:



9) Clear Memory Location(s):



AMERICAN MICROSYSTEMS, INC.

S2561/S2561A/S2561C

TONE RINGER

Features

- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 25mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

General Description

The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

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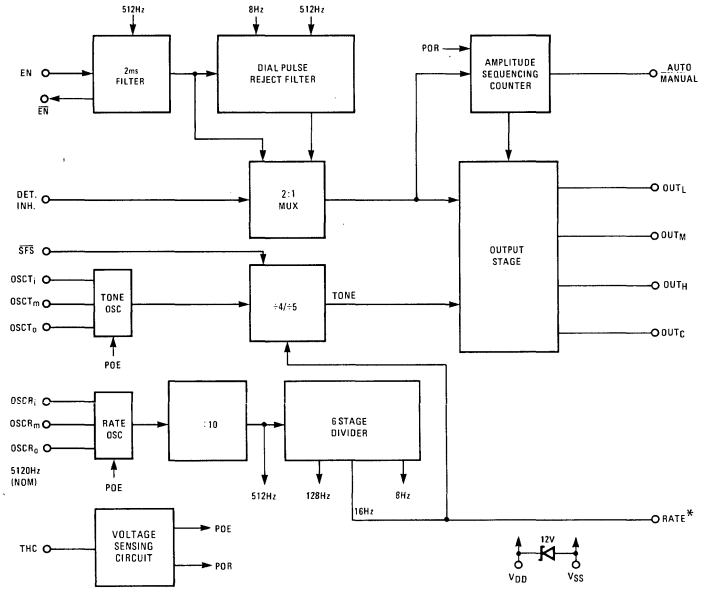
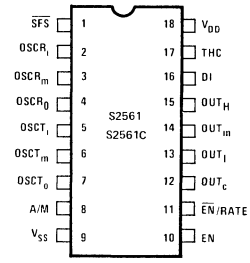
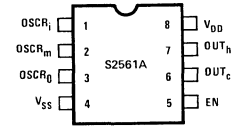
Block Diagram



Pin Configuration





Absolute Maximum Ratings

Supply Voltage	+12.0V*
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	300°C

**This device incorporates a 12V internal zener diode across the VDD to VSS pins. Do NOT connect a low impedance power supply directly across the device unless the supply voltage can be maintained below 12V or current limited to <25mA.*

Electrical Characteristics

Specifications apply over the operating temperature and 3.5V≤V_{DD} to V_{SS}<12.0V unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	12.0	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.0		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, V_{DD}=10V, THC pin open, DI pin open or V_{SS}
I_{OHC}	Output Drive Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD}=10V, V_{OUT}=0.75V
I_{OHM}	Output Source Current (Out_M output)	2		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD}=10V, V_{OUT}=0.75V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD}=10V, V_{OUT}=8.75V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD}=10V, V_{OUT}=0.75V
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	V_{DD}+0.3	V	All inputs
V_{IL}	Input Logic "0" Level	V_{SS}−0.3	0.3 V_{DD}	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	0.9 V_{DD}		V	I_O=10μA (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	I_O=10μA (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 1	μA μA	V_{DD}=10V, V_{OUT}=0V V_{DD}=10V, V_{OUT}=10V
C_{IN}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	−5	+5	%	Fixed RC component values 1MΩ ≤ R_{ri}, R_{ti}≤5MΩ; 100kΩ≤ R_{rm}, R_{tm}≤750kΩ; 150pF≤ C_{ro}, C_{to}≤3000pF; 330pF recommended value of C_{ro} and C_{to}, supply voltage varied from 9V±2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range=300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, V_{IN}=V_{DD} or V_{SS}		100	nA	Any input, except DI pin V_{DD}=10V
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	I_Z=5mA

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off (V_{SS} ≤ V_I ≤ V_{DD} as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded

Functional Description

The S2561 is a CMOS device capable of simulating the effects of the telephone bell. This is achieved by producing a tone that shifts between two predetermined frequencies (512 and 640 Hz) with a frequency ratio of 5:4 at a 16 Hz rate.

Tone Generation: The output tone is derived from a tone oscillator that uses a 3 pin R-C oscillator design consisting of one capacitor and two resistors. The oscillator frequency is divided alternately by 4 or 5 at the shift rate. Thus, with the oscillator adjusted for 5120Hz, a tone signal is produced that alternates between 512Hz and 640Hz at the shift rate. The shift rate is derived from another 3 pin R-C oscillator which is adjusted for a nominal frequency of 5120Hz. It is divided down to 16Hz which is used to produce the shift in the tone frequency. It should be noted that in the special case where both oscillators are adjusted for 5120Hz, it is only necessary to have one external R-C network for one oscillator with the other oscillator driven from it. The oscillators are designed such that for fixed R-C component values an accuracy of ±5% can be obtained over the operating supply voltage, temperature and unit-unit variations. See Table 1 for component and frequency selections. In the single frequency mode, activated by connecting the $\overline{SFS}$ input to V_{SS} only the higher frequency continuous tone is produced by using a fixed divider ratio of 4 and by disabling the shift operation.

Ring Signal Detection: In the following description it is assumed that both the tone and rate oscillators are adjusted for a frequency of 5120 Hz. Ringing signal (nominally 42 to 105 VAC, 20 Hz, 2 sec on/4 sec off duty cycle) applied by the central office between the telephone line pair is capacitively coupled to the tone ringer circuitry as shown in Figure 2. Power for the device is derived from the ringing signal itself by rectification (diodes D1 thru D4) and zener diode clamping (Z_2). The signal is also applied to the EN input after limiting and clamping by a resistor (R_2) and internal diodes to V_{DD} and V_{SS} supplies. Internally the signal is first squared up and then processed thru a 2ms filter followed by a dial pulse reject filter. The 2ms filter is a two stage shift register clocked by a 512 Hz signal derived from the rate oscillator by a divide by 10 circuit. The squared ring signal (typically a square wave) is applied to the D input of the first stage and also to reset inputs of both stages. This provides for rejection of spurious noise spikes. Signals exceeding a duration of 2ms only can pass through the filter. The dial pulse reject filter is clocked at 8 Hz derived from the rate oscillator by a divide by 640 circuit. This circuit is designed to pass any signal that has at least two transitions in a given 125ms time period. This insures that signals below 8 Hz will be rejected with certainty. Signals over 16 Hz will be passed with certainty and between 8 Hz and 16 Hz there is a region of uncertainty. By adjusting the rate oscillator to a different frequency the break points in frequencies can be varied. For instance for break points of 10 Hz and 20 Hz the rate oscillator can be adjusted to 6400 Hz. Of course this also increases the tone shift rate to 20 Hz. The action of the dial pulse reject filter minimizes the dial pulse interference during dialing although it does not completely eliminate it due to the rather large region of uncertainty associated with this type of discrimination circuitry. The dial pulse filter also has the characteristic that an input signal is not detected unless its duration exceeds 125ms. This insures that the tone ringer will not respond to momentary bursts of ringing less than 125 milliseconds in duration (Ref 1).

In logic interface applications, the 2ms filter and the dial pulse reject filter can be inhibited by wiring the Det. INHIBIT pin to V_{DD}. This allows the tone ringer to be enabled by a logic '1' level applied at the "ENABLE" input without the necessity of a 20Hz ring signal.

Voltage Sensing: The S2561 contains a voltage sensing circuit that enables the output stage and the rate and tone oscillators, only when the supply voltage exceeds a predetermined value. Typical value of this threshold is 7.3 volts. This produces two benefits. First, it insures that the audible intensity of the output tone is fairly constant throughout the ringing period; and secondly, it insures proper circuit operation during the "auto" mode operation by reducing the power consumption to a minimum when the supply voltage drops below 7.3 volts. This extends the supply voltage decay time beyond 4 seconds (off period of the ring signal) with an adequate filter capacitor and insures the proper functioning of the "amplitude sequencing" counter. It is important to note that the operating supply voltage should be well above the threshold value during the ringing period and that the filter capacitor should be large enough so that the ripple on the supply voltage does not fall below the threshold value. A supply voltage of 10 to 12 volts is recommended.

In applications where the tone ringer is continuously powered and below the threshold level, the internal threshold can be bypassed by connecting the THC pin to V_{DD}. The internal threshold can also be reduced

Functional Description (Continued)

by connecting an external zener diode between the THC and V_{DD} pins.

Auto Mode: In the "auto" mode, activated by wiring the "auto/manual" input to V_{SS}, an amplitude sequencing of the output tone can be achieved. Resistors R_L and R_M are inserted in series with the Out_L and Out_M outputs, respectively, and paralleled with the Out_H output (Figure 1). Load is connected across Out_H and Out_C pins. R_L is chosen to be higher than R_M. In this manner the first ring is of the lowest amplitude, second ring is of medium amplitude and the third and consecutive rings thereafter are at maximum amplitude. For the proper functioning of the "amplitude sequencing" counter the device must have at least 4.0 volts across it throughout the ring sequence. The filter capacitor is so chosen that the supply voltake will not drop below 4.0 volts during the off period. At the end of a ring sequence when the off period substantially exceeds the 4 second duration, the counter will be reset. This will insure that the amplitude sequencing will start correctly beginning a new ring sequence. The counter is held in reset during the "manual" mode operation. This produces a maximum ring amplitude at all times.

Output Stage: The output stage is of push-pull type consisting of buffers L, M, H and C. The load is connected across pins Out_H and Out_C (Figure 2). During ringing, the Out_H and Out_C outputs are out of phase with each other and pulse at the tone rate. During a non-ringing state, all outputs are forced to a known level such as ground which insures that there is no DC component in the load. Thus, direct coupling can be used for driving the load. The major benefit of the push-pull arrangement is increased power output. Four times as much power can be delivered to the load for the same operating voltage. Buffers M and H are three-state. In the "auto" mode buffer M is active only during the second ring and in the "high impedance" state at all other times. Buffer H is active beginning the third ring. In the "manual" mode buffers H, L and C are active at all times while buffer M is in a high impedance state. The output buffers are so designed that they can source or sink 5mA at a V_{DD} of 10 volts without appreciable voltage drop. Care has been taken to make them symmetrical in both source and sink configurations. Diode clamping is provided on all outputs to limit the voltage spikes associated with transformer drive in both directions V_{DD} and V_{SS}.

Normal protection circuits are present on all inputs.

Table 1. S2561/S2561C Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}*, V_{SS}*)	2	These are the power supply pins. The device is designed to operate over the range of 3.5 to 12.0 volts. A range of 10 to 12 volts is recommended for the telephone application.
Ring Enable (EN*, $\overline{EN}$)	2	These pins are for the 20Hz ring enable input. They can also be used for DC level enabling by wiring the DI pin to V_{DD}. $\overline{EN}$ is available for the S2561 only.
Auto/Manual (A/M)	1	"Auto" mode for amplitude sequencing is implemented by wiring this pin to V_{SS}. "Manual" mode results when connected to V_{DD}. The amplitude sequencing counter is held in reset during the "manual" mode.
Outputs (Out_L, Out_M, Out_H^*, Out_C^*)	4	These are the push-pull outputs. Load is directly connected across Out_H and Out_C outputs. In the "auto" mode, resistors R_L and R_M can be inserted in series with the Out_L and Out_M outputs for amplitude sequencing (see Figure 1).
Oscillators Rate Oscillator ($OSCR_i^*$, $OSCR_m^*$ $OSCR_o^*$)	3	These pins are provided to connect external resistors RR_i, RR_m and capacitor CR_o to form an R-C oscillator with a nominal frequency of 5120Hz. See Table 2 for components selection.

Table 1 (Continued)

Pin	Number	Function
Tone Oscillator ($OSCT_i$, $OSCT_m$, $OSCT_o$)	3	These pins are provided to connect external resistors RT_i, RT_m and capacitor CT_o to form an R-C oscillator from which the tone signal is derived. With the oscillator adjusted to 5120Hz, a tone signal with frequencies of 512Hz and 640Hz results. See Table 2 for components selection.
Threshold Control (THC)	1	The internal threshold voltage is brought out to this pin for modification in non-telephone applications. It should be left open for telephone applications. For power supplies less than 9V connect to V_{DD}.
Rate	1	This is an optional output for the S2561C version which replaces the $\overline{EN}$ output. This is a 16Hz output that can be used by external logic as shown in Figure 3-A to produce a 2sec on/4sec off waveform.
Detector Inhibit (DI)	1	When this pin is connected to V_{DD}, the dial pulse reject filter is disabled to allow DC level enabling of the tone ringer. This pin should be hardwired to V_{SS} in normal telephone-type applications.
Single Frequency Select ($\overline{SFS}$)	1	When this pin is connected to V_{SS}, only a single frequency continuous tone is produced as long as the tone ringer is enabled. In normal applications this pin should be hardwired to V_{DD}.
	$\overline{18}$	

**Pinouts of 8 pin S2561A package.*

Table 2. Selection Chart for Oscillator Components and Output Frequencies

Tone/Rate Oscillator Frequency (Hz)	Oscillator Components R_I (kΩ)	R_M (kΩ)	C_O (pF)	Rate (Hz)	Tone (Hz)
5120	1000	200	330	16	512/640
6400	Select components in the ranges indicated in the table of electrical charateristics			20	640/800
3200				10	320/400
8000				25	800/1000
fo				$\frac{fo}{320}$	$\frac{fo}{10}/\frac{fo}{8}$

Applications

Typical Telephone Application: Figure 2 shows the schematic diagram of a typical telephone application for the S2561 tone ringer circuit power is derived from the telephone lines by the network formed by capacitor C_1, resistor R_1, diode bridge D_1 through D_4, and filter capacitor C_2. C_2 is chosen to be large enough so as to insure that the power supply ripple during ringing does not fall below the internal threshold level (typ. 7.3 volts) and to provide large enough decay time during the off period. A typical value of C_2 may be 47μF. C_1 and R_1 are chosen to satisfy the Ringer Equivalence Number (REN) spcification (REf. 1). For REN=1 the resistor should be a mini-mum of 8.2kΩ. It must be noted that the amount of power that can be delivered to the load depends upon the selection of C_1 and R_1.

The device is enabled by limiting the incoming ring signal through resistors R_2, R_3 and diodes d_5 and d_6. Zener diode Z_1 (typ. 9-27 volts) may be required in certain applications where large voltage transients may occur on the line during dial pulsing. The internal 2ms filter and the dial pulse reject filter will suppress any undesirable components of the signal and will only respond to the normal 20Hz ring signal. Ring signals with frequencies above 16Hz will be detected.

The configuration shown will produce a tone with frequency components of 512Hz and 540 Hz with a shift rate of approximately 16 Hz and deliver at least 25mW to an 8Ω speaker through a 2000Ω:8Ω transformer. If "manual" mode is used, a potentiometer may be inserted in series with the transformer primary to provide volume control. If "automatic" mode is used, resistors R_L and R_M can be chosen to provide desired amplitude sequencing. Typically, signal power will be down $20 \log \left(\frac{R_{LOAD}}{R_L + R_{LOAD}} \right)$ dB during the first ring, and down $20 \log \left(\frac{R_{LOAD}}{R_M + R_{LOAD}} \right)$ dB during the second ring with maximum power delivered to the load beginning the third and consecutive rings.

In applications where dial pulse rejection is not necessary, such as in DTMF telephone systems, the ENABLE pin may be connected directly to V_{DD}. Det. Inh pin must be connected to V_{DD} to allow DC level enabling of the ringer.

Non-Telephone Applications: The configuration shown in Figure 3-A may be used in non-telephone applications where it is desired to simulate the telephone bell. The internal threshold is bypassed by wiring THC to V_{DD}. The rate output (16Hz) is divided down by a 7 stage divider type 4024 to produce two signals: a 2 second on/2 second off signal and a 4 second on/4 second off signal. The first signal is connected to the EN pin and the second to the DI pin to produce a 2 second on/4 second off telephone-type ring signal. The ring sequence is initiated by removing the reset on the divider. If "auto" mode is used, a reset signal must be applied to the "amplitude sequencing" counter at the end of a ring sequence so that the circuit will respond correctly to a new ring sequence. This is done by temporarily connecting the "auto/manual" input to V_{SS}.

Figure 3-B shows a typical application for alarms, buzzers, etc. Single frequency mode is used by connecting the $\overline{SFS}$ input to V_{SS}. A suitable on/off rate can be determined by using the 7 stage divider circuit. If continuous tone is not desired, the 16Hz output can be used to gate the tone on and off by wiring it into the ENABLE input.

Many other configurations are possible depending upon the user's specific application.

Reference 1. Bell system communications technical reference:

PUB 47001 of August 1976
"Electrical characteristics of Bell System Network Facilities at the interface with Voiceband Ancillary and Data Equipment" — Sections 2.6.1 and 2.6.3.

Figure 1-A. Output Stage Connected for Auto Mode Operation

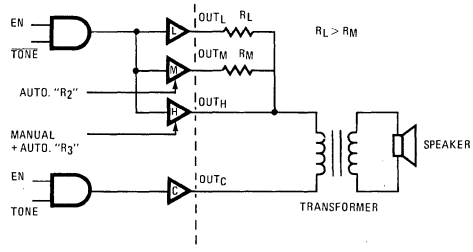


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Figure 1-B. Output Stage Connected for Manual Mode Operation.

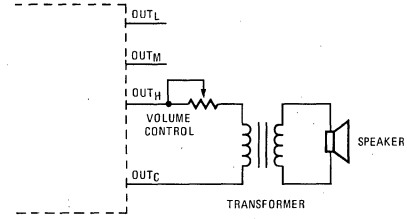

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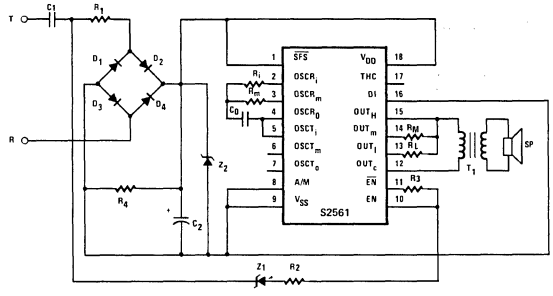
Figure 2. Typical Telephone Application of the S2561 and S2561A



C_1	.47μF/200V	R_1	2KΩ	R_i	1MΩ	R_L	18KΩ	SP	8ΩSPEAKER
C_2	47μF/25V	R_2	51KΩ	R_m	200KΩ	R_M	3.3KΩ	T_1	2000Ω/8ΩXFMR
D_1–D_4	IN4004	R_3	10MΩ	C_0	300pF	R_4	100KΩ	Z_1	9 TO 27V ZENER
Z_2	IN4742 12V ZENER								

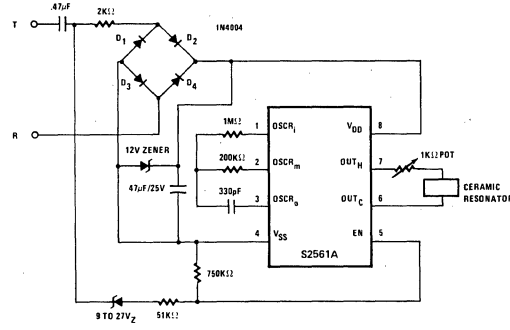


Figure 3-A. Simulation of the Telephone Bell in Non-Telephone Applications.

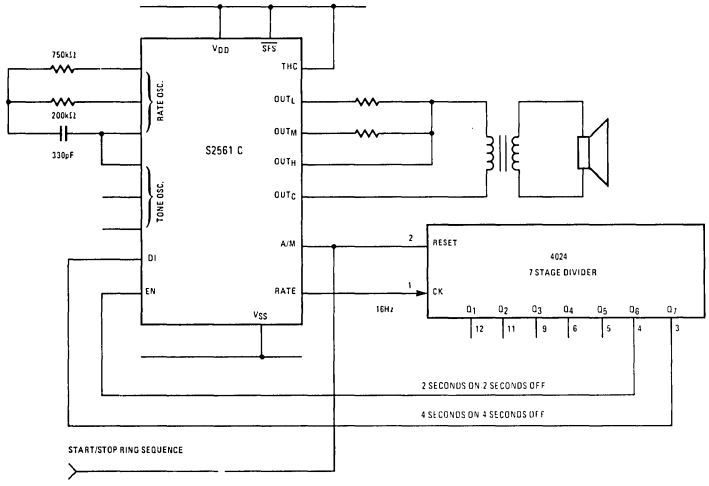
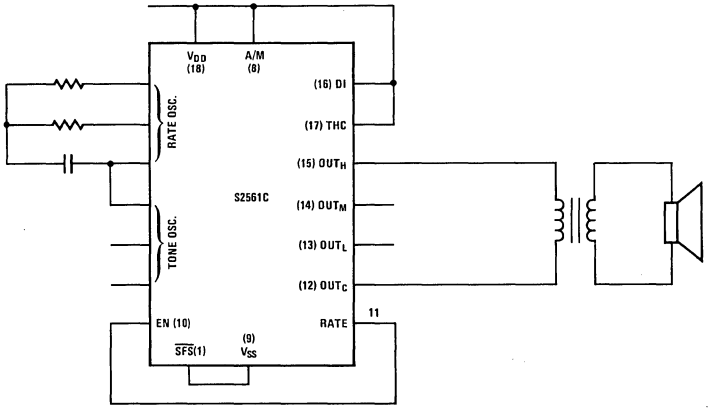


Figure 3-B. Single Frequency Tone Application in Alarms, Buzzers, Etc.



AMERICAN MICROSYSTEMS, INC.

S2562

REPERTORY DIALER

Features

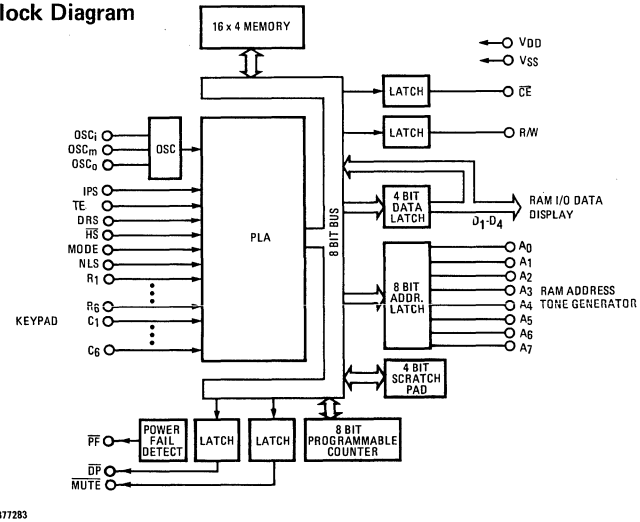
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing with Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Memory Storage of 32 8-Digit Numbers or 16 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries
- ☐ Inexpensive, but Accurate R-C Oscillator Design Provides Better Than ± 3% Accuracy Over Supply Voltage, Temperature and Unit-Unit Variations and Allows Different Dialing Rates, IDP and Tone Drive Timing by Changing the Time Base
- ☐ Power Fail Detection
- ☐ BCD Output with Update for Number Display Applications

General Description

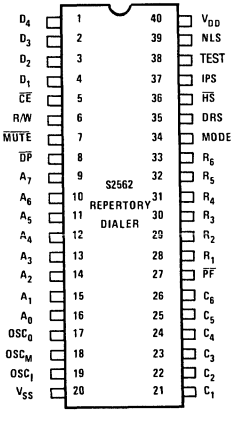
The S2562 Repertory Dialer is a CMOS integrated circuit that can perform storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101—256x4 RAM that functions as telephone number storage. With one S5101 up to 32 8-digit or 16 16-digit numbers can be stored. It can provide either dial pulses or DTMF tones with the addition of the AMI S2559 tone generator for either the dial or tone line applications.

Data subject to change at any time without notice. These sheets transferred for information only.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	13.5V
Operating Supply Voltage Range ($V_{DD}-V_{SS}$)	3.5V to 7.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	200°C

Electrical Characteristics:

Specifications apply over the operating temperature range and 4.5V ≤ V_{DD} to V_{SS} ≤ 5.5V unless otherwise specified. Absolute values of measured parameters are specified.

Symbol	Characteristics	Min.	Max.	Units	Conditions
	Output Drive				
I_{OLDP}	$\overline{DP}$ Output Sink Current	400		μA	V_{OUT}=0.4V, V_{DD}=5V
I_{OHDP}	$\overline{DP}$ Output Source Current	400		μA	V_{OUT}=3.6V, V_{DD}=5V
I_{OLM}	$\overline{MUTE}$ Output Sink Current	400		μA	V_{OUT}=0.4V, V_{DD}=5V
I_{OHM}	$\overline{MUTE}$ Output Source Current	400		μA	V_{OUT}=3.6V, V_{DD}=5V
I_{OHPF}	$\overline{PF}$ Output Source Current	100		μA	V_{OUT}=3.6V, V_{DD}=5V
	CMOS to CMOS				
V_{IL}	Logic "0" Input Voltage		1.5	V	All inputs, V_{DD}=5V
V_{IH}	Logic "1" Input Voltage	3.5		V	All inputs, V_{DD}=5V
V_{OL}	Logic "0" Output Voltage		0.5	V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, I_O=−10μA, V_{DD}=5V
V_{OH}	Logic "1" Output Voltage	4.5		V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, I_O=−10μA, V_{DD}=5V
	Current Levels				
I_{DD}	Quiescent Current		25	μA	Standby, V_{DD}=5V
I_{DD}	Operating Current		500	μA	All valid input combinations, $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$ outputs open V_{DD}=5V
I_{IH}	Input Current Any Pin (keyboard inputs)	10	100	μA	$V_{IN}=V_{DD}$, V_{DD}=5V
I_{IL}, I_{IH}	Input Current All Other Pins		100	μA	$V_{IN}=V_{SS}$ or V_{DD}, V_{DD}=5V
I_{OZ}	Output Current in High Impedance State		1 1	μA μA	V_{DD}=5V, V_{OUT}=0V data outputs (D1-D4) V_{DD}=5V, V_{OUT}=5V
fo	Oscillator Frequency	4	10	kHz	V_{DD}=5V (min. duty cycle 30/70)
Δfo/fo	Frequency Deviation	−3	+3	%	$V_{DD}-V_{SS}$ from 4.5V to 5.5V. Fixed R-C oscillator components 50kΩ≤ R_M ≤ 750kΩ; 1MΩ ≤ R_I ≤ 5MΩ; 150pF ≤ C_O 3000pF; 330pF most desirable value for C_O, fo < 10kHz over the operating temperature and unit-unit variations
C_{IN}	Input Capacitance, Any Pin		7.5	pF	
V_{TRIP}	Supply Voltage at which $\overline{PF}$ Output Goes Low	2.5	4.5	V	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and posible damage of the input-protection diode when the device power supply is grounded. Power should be applied to the device in "on hook" condition.

Functional Description

The S2562 is a CMOS controller designed for storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101 256x4 RAM that functions as a telephone number storage. A single S5101 RAM will store up to 32 8-digit or 16 16-digit telephone numbers. The S2562 can be programmed to work with either 8-digit or 16-digit numbers by means of the Number Length Select (NLS) input.

The S2562 uses an inexpensive, but accurate R-C oscillator as a time base from which the dialing rate and inter-digit pause duration (IDP) are derived. Different dialing rates and IDP durations can be implemented by simply adjusting the oscillator frequency. The dialing rate and IDP can be further changed by a 2:1 factor by means of the dialing rate select (DRS) and inter-digit pause select (IPS) inputs. Thus, for the oscillator frequency of 8kHz, dialing rates of 10 and 20 pps and IDP's of 400 and 800ms can be achieved. The mark/space ratio is fixed independent of the time base at 40/60. Over supply voltage (5V±10%), operating temperature range and unit-unit variations, timing accuracy of ±3% can be achieved. A mute output is also available for muting of the receiver during dial pulsing. See Figure 5 for timing relationship.

The S2562 can be programmed by means of the MODE input for dual tone signaling applications as well. In this mode, it can interface directly with the AMI standard S2559 Tone Generator to produce the required DTMF signals. The tone on/off rate during an auto dial operation in this mode is derived from the time base. For the oscillator frequency of 8kHz, a tone drive rate of 50ms on, 50ms off is obtained. Different rates can be implemented by adjusting the time base as desired. See Tables 2 and 3 for the various combinations. In the tone mode, the mute output is used to gate the tone generator on and off. The 8 address lines that are normally used for addressing the RAM are also used to address the tone generator row, column inputs. Figure 6 shows a typical system application.

The S2562 can perform the following functions:

Normal Dialing

The user enters the desired number digits through the keyboard after going off hook. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. Debouncing is provided on the keyboard entries to avoid false entries. The number entered is retained for future redial. Pauses may be entered when required in the dial sequence by pressing the "#" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of digits (8 or 16).

An update pulse is generated to update the display digit as a new entry is made.

Redialing

The last number entered is retained in the internal memory and can be redialed by going "off hook" and depressing the "redial" (RDL) key. The RDL key is a unique 2 of 12 matrix location (R5, C3). The number being redialed out is displayed as it is dialed out.

In the tone mode, the redial tone drive rate depends upon the time base as discussed before.

Storing of a Normally Dialed or Redialed Number into the External Memory

After the normal dialing or redialing operation, the telephone number can be stored in the external memory for future repertory dialing use by going on hook and initiating the following key sequence.

1. Push "store" (ST) button.
2. Depress the single digit key corresponding to the desired address location.

Note that the "ST" key is a unique 2 of 12 matrix location (R_5, C_1).

Storing of a Telephone Number into the External Memory

This operation is performed "on hook" and no outdialing occurs. A telephone number can be stored in the desired address location by initiating the following key sequence.

1. Push the "*" key (This instructs the device to accept a new number for storage into the internal memory).
2. Enter the digits (including any access pauses) corresponding to the desired number. Digits will be displayed as they are entered.
3. Push the "ST" key.
4. Push the single digit key corresponding to the desired address location.

The entire sequence can be repeated to store as many numbers as desired. However, any memory locations not addressed with a telephone number "store" operation must be addressed with the following sequence.

1. Push the "*" key.
2. Push the "ST" key.
3. Push the single digit key corresponding to the first unused memory location.
4. Push the "ST" key.

5. Push the single digit key corresponding to the next unused memory location.

Steps 4. and 5. are repeated until all remaining memory locations have been addressed.

It should be noted that accessing all memory locations is required only for initial system set-up. This insures that no memory location will contain invalid data from memory power-up. If a memory location were to have invalid, power-up induced data and that location was addressed by the S2562, the S2562 would enter a "Halt" state and cease its normal program activities. To exit from this condition it is necessary to go "on hook" and perform a "store" operation.

Displaying of a Stored Telephone Number

This is an "on hook" operation Either the last dialed number or the number stored in the external memory can be displayed one digit at a time. The key sequence for displaying the last dialed number is as follows:

Push the "RDL" key.

The number in the external memory can be displayed as follows:

1. Push the "R" key.
2. Push the single digit key corresponding to the desired address location.

Note that the "R" key is a unique 2 of 12 matrix location (R_5, C_2).

The number is displayed one digit at a time at a rate determined by the time base. With a time base of 8kHz the display will be on 500ms, off 500ms. The display is updated by producing an update pulse. The update pulse must be decoded with external logic (one inverter and one 2-input gate) as shown in Figure 6.

The display is blanked by outputting an illegal (non BDC) code such as 1111. The 4511-type BCD to 7 segment decoder driver latch will blank the display when the illegal code is detected. When other driver circuits are employed, external logic must be used to detect the illegal code. Table 4 gives a list of display codes used by S2562.

Repertory Dialing

This is the most common mode of usage and allows the user to dial automatically any number stored in the memory. This mode is initiated by the following key sequence after going off hook.

1. Push the "*" key.
2. Push the single digit key corresponding to the desired address location.

The number is displayed as it is dialed out. In the tone mode, the tone driver rate is dependent on the time base as described earlier.

Pause

Note that the out dialing in the repertory or redial operation continues unless an access pause is detected. The outpulsing will stop and resume only when the user terminates the access pause by pushing the "*" key again.

Power Fail Detection

This output is normally high. When the supply voltage falls below a predetermined value, it goes low. The output can then drive a suitable latching device that will switch the memory to either the tip and ring or an auxiliary battery supply.

Memory Expansion

The memory can be expanded by paralleling additional S5101 RAM's. External logic must be used to enable the desired RAM corresponding to a desired address location. The S2562 can drive up to 2 RAM's without the need of buffering address and data lines.

Keybounce Protection

When a key closure is detected by the S2562, an internal timeout (4ms at fo=8kHz) is started. Any transitions that occur during this timeout will reset the timer to zero so that a key will only be accepted as valid after a noise free timeout period. The key must remain closed for an additional 16ms before released. Thus, the total make time of the key must be at least 20ms. The key must be released for at least 1ms before a new key is activated. Any transitions occurring when the key is released are ignored as long as the make time does not exceed 4ms.

Improper Operating Sequence

The S2562 will enter a "halt" state if a proper operating sequence is not followed. Examples of such sequences are:

1. Off hook, "ST", on hook
2. 2. Off hook, "*", on hook
3. Off hook, "*", unprogrammed loc.
4. On hook, "*", D_1, D_2 - - -, off hook without completing the store sequence
5. Off hook with supply voltage less than 3.5 volts

To clean the halt state press "ST" key followed by an unused "loc" key. This can be performed in either on hook or off hook condition. Figure 1 shows a scheme to clear the halt state electronically.

Table 1. Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 3.5V to 7.5V.
Keyboard (R_1-R_6, C_1-C_6)	12	These are 6 row and 6 column inputs from the keyboard contacts. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect to each other. Figure 2 depicts the standard telephone X-Y matrix keyboard arrangements that can be used. A logic, interface is also possible as shown in Figure 3. Debouncing is provided to avoid false entry. Key pad entry options are shown in Figure 4.
Number Length Select (NLS)	1	This input permits programming of the device to accept either 8-digit numbers or 16-digit numbers.
Mode Select (MODE)	1	This input allows the use of the device in either dial pulsing applications or tone drive applications.
Dial Rate Select (DRS)	1	This input allows selection of two different dialing rates such as 10 or 20 pps, 7 or 14 pps, etc. See Tables 2 and 3.
Inter-Digit Pause Select (IPS)	1	This allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceeding the first dialed digit is an inter- digit time equal to the selected IDP. Two pause durations, either 400ms or 800ms are available at dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Test Input (TEST)	1	This input is used for test purposes. For normal operation it must be tied to V_{DD}.
Mute Output ($\overline{MUTE}$)	1	A pulse is available that can provide drive to turn on an external transistor to mute the receiver during dial pulsing. See Figure 5 for mute and dial pulse output relationship. It is also used as a keyboard disable in the tone drive applications. See Figure 6.
Dial Pulse Output ($\overline{DP}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. This output will be normally high and go low during "space" or "break."
Display Memory I/O Data (D_1-D_4)	4	These are 4 bidirectional pins for inputting and outputting data to the external memory and display driver.

Table 1. (Continued)

Pin	Number	Function
Memory Enable ($\overline{CE}$)	1	This line controls the external memory operation.
Memory Read/Write (R/W)	1	This line controls the read or the write operation of the external memory. This output along with the $\overline{CE}$ output can be used to produce a pulse to update the external display. See Figure 6.
Tone Generator/Memory Address (A_0-A_7)	8	These are 8 output lines that carry the external memory address and tone generator row/column information.
Hook Switch ($\overline{HS}$)	1	This input conveys the state of the subset. "Off hook" corresponds to V_{SS} condition.
Power Fail Detect ($\overline{PF}$)	1	This output is normally high and goes low when the power supply falls below a certain predetermined value.
Oscillator (OSC_i, OSC_m, OSC_o)	3	These pins are provided to connect external resistors R_I, R_M and capacitor C_O to form an R-C oscillator that generates the time base for the repertory dialer. The output dialing rate, tone drive rate and IDP are derived from this time base.
	40	

Table 2. Table for Selection of Oscillator Component Values for Desired Dialing Rate, I_{DP} or Tone Drive Rate

Dial Rate Desired (PPS)	Osc. Freq. fo (Hz)	Oscillator Components R_M (kΩ)	(R_I) (kΩ)	C_O (pF)	Dial Rate (PPS) DRS=V_{SS}	Dial Rate (PPS) DRS=V_{DD}	IDP (ms) IPS=V_{SS}	IDP (ms) IPS=V_{DD}	Tone Drive On/Off Time (ms)
5.5/11	4400	TBD			5.5	11	1454	727	90/90
6/12	4800	220			6	12	1334	667	83.3/83.3
6.5/13	5200	190			6.5	13	1230	615	77/77
7/14	5600				7	14	1142	571	71/71
7.5/15	6000		1000	300	7.5	15	1066	533	66.7/66.7
8/16	6400				8	16	1000	500	62.5/62.5
8.5/17	6800	TBD			8.5	17	942	471	59/59
9/18	7200				9	18	888	444	55.5/55.5
9.5/19	7600				9.5	19	842	421	52.6/52.6
10/20	8000	110			10	20	800	400	50/50
(fo/800/ (fo/400)	fo				fo/800	fo/400	$\frac{6400 \times 10^3}{fo}$	$\frac{3200 \times 10^3}{fo}$	$\frac{400 \times 10^3}{fo}$/$\frac{400 \times 10^3}{fo}$

Figure 1. Logic to Eliminate Halt Condition Due to Improper Sequencing.

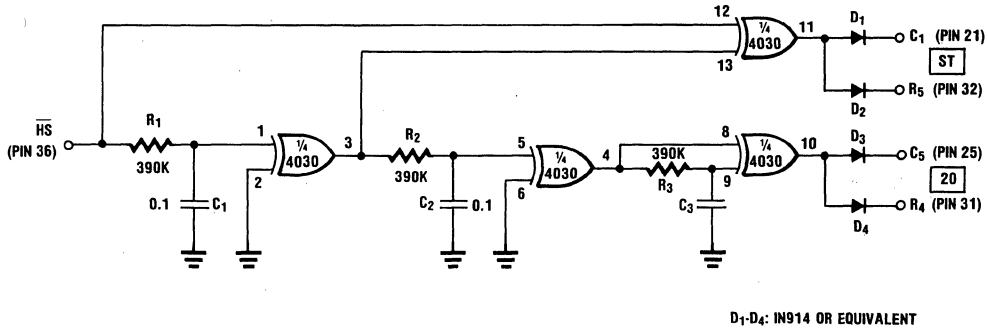


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 12 Row, Column Format

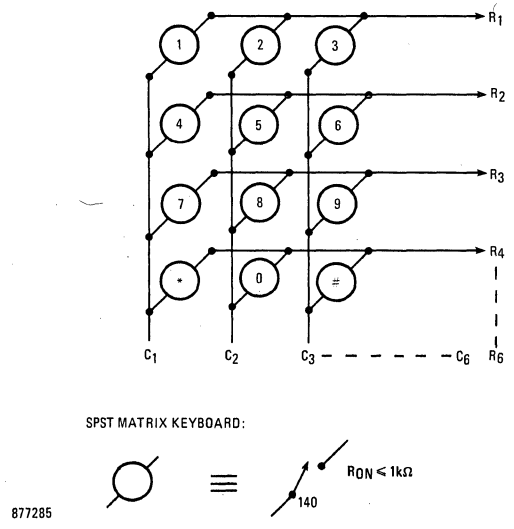
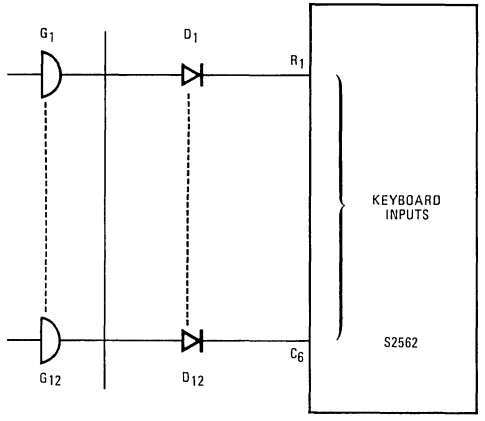


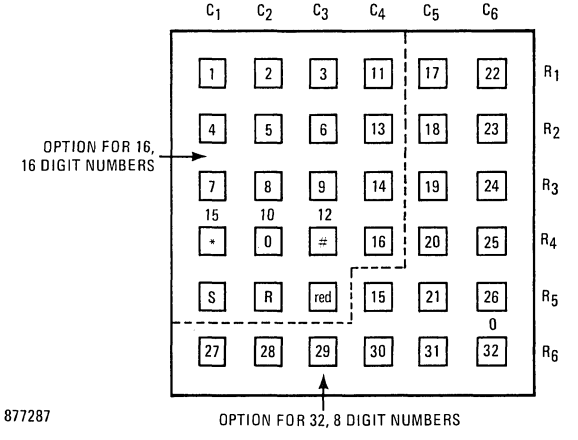
Figure 3. Logic Interface For the S2562



G_1 through G_{12} any CMOS type logic gates.
D_1 through D_{12} DIODES type 1N 914. (Optional)

A valid key closure corresponds to a logic high level on one row and one column

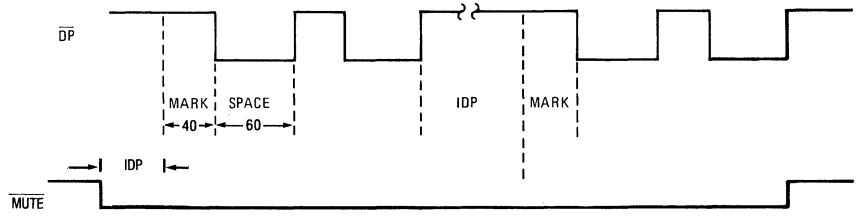
Figure 4. Example of Keypad Entry – Options



Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS} V_{DD}	(fo/800) pps (fo/400) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	(3200/fo) S (6400/fo) S
Test Input	TEST	V_{SS} V_{DD}	Test Mode Normal Mode
Hook Switch	$\overline{HS}$	V_{DD} V_{SS}	On Hook Off hook
Mode Selection	MODE	V_{SS} V_{DD}	Dial pulse Tone Drive*
Number Length Selection	NLS	V_{SS} V_{DD}	8 digits 16 digits

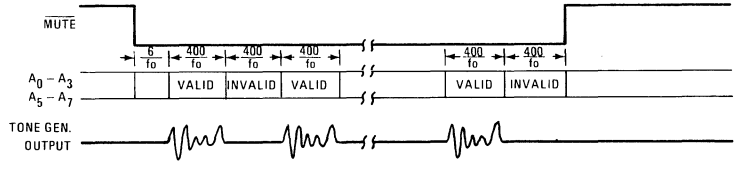
*For tone mode also set DRS=V_{SS}, IPS=V_{SS} and Test=V_{DD}.
Note: fo is the oscillator frequency and is determined as shown in Table 2.

Mute and Dial Pulse Output Timing Relationship



$\overline{Mute}$ will reset i) when the number of digits dialed out equals either the number of digits entered or the maximum selected (8 or 16) or ii) when an access pause is detected.

Figure 5B. Mute and Tone Output Timing Relationship



Mute output will reset i) when the number of digits dialed out equals the number of digits entered or equals the maximum selected (8 or 16) or ii) when an access pause is detected. In the normal dialing mode when digits are entered one at a time the mute output will reset between digits provided the time between entered digits exceeds $\frac{400}{fo}$. In both the normal dialing or automatic dialing mode tone will be output for a fixed duration of $\frac{400}{fo}$ (50msec for fo = 8kHz).

Figure 6. Typical Application of the S2562

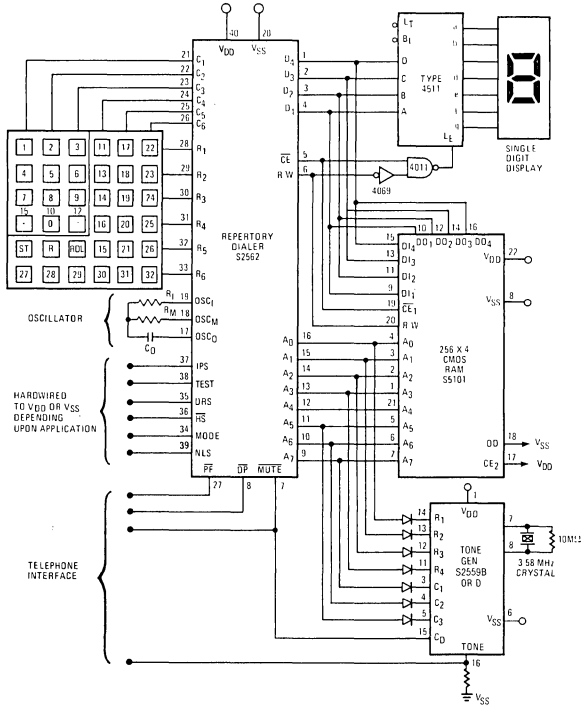


Table 4. Display Codes

D_4	D_3	D_2	D_1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Not Used
1	0	1	1	Not Used
1	1	0	0	# (Pause)
1	1	0	1	Not Used
1	1	1	0	Beginning of Number
1	1	1	1	Blank

AMERICAN MICROSYSTEMS, INC.

S2563

REPERTORY DIALER

Features

- ☐ Specifically Designed for Telephone Line Powered Applications
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing With Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Two Selections of Mark/Space Ratio
- ☐ Memory Storage of 29 8-Digit Numbers or 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Can Use Standard 3×4 or 4×4 Keyboards
- ☐ Inexpensive, but Accurate R-C Oscillator Design
- ☐ BCD Output with Update for Single Digit Display

General Description

The S2563 is an improved version of the S2562 repertory dialer and can replace the S2562 in existing applications using local power. It is however specifically designed for applications that will only use telephone line power. To achieve this following changes were made to the S2562 design.

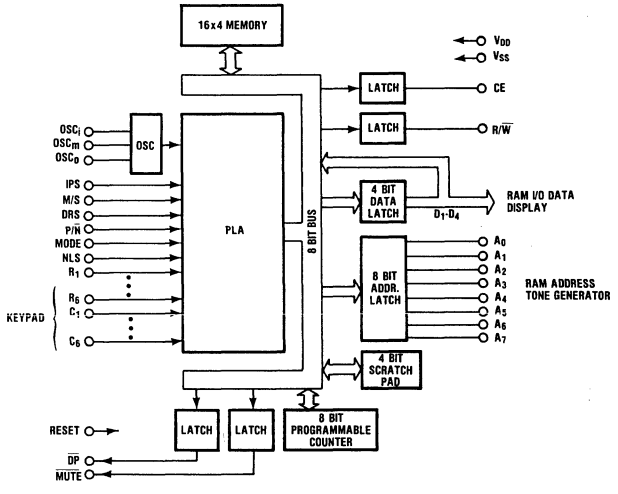
a. $\overline{PF}$ output was replaced by a level reset input which allows the device to be totally powered down in the on-hook state of the telephone.

b. To reduce power consumption in the associated S5101 memory in the standby mode, the interface was changed so that its CE_2 input rather than the the $\overline{CE_1}$ input is controlled by the device.

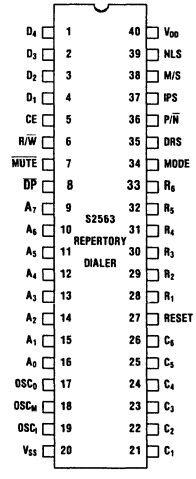
c. Process was changed to a lower voltage CMOS process. Additionally a mark/space selection input (M/S) was added to allow selection of either 40/60 or 33/67 ratio. Provision was also made to allow the device to work with a standard 3×4 or 4×4 keyboard.

Data subject to change at any time without notice. These sheets transferred for information only.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

Supply Voltage	6.0V
Operating Supply Voltage Range ($V_{DD}-V_{SS}$)	2.0V – 5.5V
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−40°C to +125°C
Voltage at any Pin	V_{SS} −0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10sec)	200°C

Electrical Characteristics:

Specifications apply over the operating temperature range unless otherwise specified. Absolute values of measured parameters are specified.

Symbol	Characteristics	Min.	Max.	Units	Conditions
	Output Drive				
I_{OLDP}	$\overline{DP}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHDP}	$\overline{DP}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
I_{OLM}	$\overline{MUTE}$ Output Sink Current	400		μA	$V_{OUT}=0.4V$, $V_{DD}=5V$
I_{OHM}	$\overline{MUTE}$ Output Source Current	400		μA	$V_{OUT}=3.6V$, $V_{DD}=5V$
	CMOS to CMOS				
V_{IL}	Logic "0" Input Voltage		30%V_{DD}	V	All inputs
V_{IH}	Logic "1" Input Voltage	70%V_{DD}		V	All inputs
V_{OL}	Logic "0" Output Voltage		0.5	V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $I_O=10\mu A$, $V_{DD}=5V$
V_{OH}	Logic "1" Output Voltage	4.5		V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $I_O=-10\mu A$, $V_{DD}=5V$
	Current Levels				
I_{DD}	Quiescent Current		1.0	μA	Standby, $V_{DD}=1.5V$ (Data Retention)
I_{DD}	Operating Current		500	μA	All valid input combinations, $\overline{DP}$, $\overline{MUTE}$, outputs open $V_{DD}=5V$
I_{IH}	Input Current (keyboard inputs)	10	100	μA	$V_{IN}=V_{DD}$, $V_{DD}=5V$
I_{IL}, I_{IH}	Input Current All Other Pins		10	μA	$V_{IN}=V_{SS}$ or V_{DD}, $V_{DD}=5V$
I_{OZ}	Output Current in High Impedance State		10 10	μA μA	$V_{DD}=5V$, $V_{OUT}=0V$ data outputs (D1-D4) $V_{DD}=5V$, $V_{OUT}=5V$
fo	Oscillator Frequency	4	10	kHz	$V_{DD}=5V$ (min. duty cycle 30/70)
Δfo/fo	Frequency Deviation	−3	+3	%	$V_{DD}-V_{SS}$ from 4.5V to 5.5V. Fixed R-C oscillator components $50k\Omega \leq R_M \leq 750k\Omega$; $1M\Omega \leq R_I \leq 5M\Omega$; $150pF \leq C_O$ 3000pF; 330pF most desirable value for C_O, fo < 10kHz over the operating temperature and unit-unit variations
C_{IN}	Input Capacitance, Any Pin		7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leq V_I \leq V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and posible damage of the input-protection diode when the device power supply is grounded. Power should be applied to the device in "on hook" condition.

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The S2563 is a CMOS controller designed for storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101 256×4 RAM that functions as a telephone number storage. A single S5101 RAM will store up to 29 8-digit or 16 16-digit telephone numbers. The S2563 can be programmed to work with either 8-digit or 16-digit numbers by means of the Number Length Select (NLS) input.

The S2563 uses an inexpensive, but accurate R-C oscillator as a time base from which the dialing rate and inter-digit pause duration (IDP) are derived. Different dialing rates and IDP durations can be implemented by simply adjusting the oscillator frequency. The dialing rate and IDP can be further changed by a 2:1 factor by means of the dialing rate select (DRS) and inter-digit pause select (IPS) inputs. Thus, for the oscillator frequency of 8kHz, dialing rates of 10 and 20 pps and IDP's of 400 and 800ms can be achieved.

The reset and P/$\overline{N}$ inputs are used to put the device in various operating modes. To store numbers in the memory P/$\overline{N}$ input must be made high. When low, normal operations such as dialing, redialing or memory dialing can be performed. When reset input is high, it overrides and forces the device in a power down mode. Connections of the two inputs depend upon the application—local power or telephone line power. See Table 4 for connection details.

The S2563 can also operate in the tone mode (MODE= V_{DD}). In this mode, it can interface with the AMI standard S2559 Tone Generator to produce the required DTMF signals. The tone on/off rate during an auto dial operation in this mode is derived from the time base. For the oscillator frequency of 8kHz, a tone drive rate of 50ms on, 50ms off is obtained. Different rates can be implemented by adjusting the time base as desired. See Tables 2 and 3 for the various combinations. In the tone mode, the mute output is used to gate the tone generator on and off. The 8 address lines that are normally used for addressing the RAM are also used to address the tone generator row, column inputs. Figure 6 shows a typical system application.

The S2563 operates in the following modes:

Normal Dialing

The user enters the desired number digits through the keyboard after entering the normal mode. Dial pulsing starts as soon as the first digit is entered. The entered digits are stored sequentially in the internal memory. Since the device is designed in a FIFO arrangement, digits can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 50ms while the dialing rate may vary from 7 to 20 pps. Debouncing is provided on the keyboard entries to avoid false entries. The number entered is retained for future redial. Pauses may be entered when required in the dial sequence by pressing the "P" key, which provides access pauses for future redial. Any number of access pauses may be entered as long as the total entries do not exceed the total number of digits (8 or 16). An update pulse is generated to update the display digit as a new entry is made.

Redialing

The last number entered is retained in the internal memory and can be redialed by going in the normal mode and depressing the "redial" (RL) key. The RL keys are at locations (R_5, C_3) and (R_3, C_4). The number being redialed out is displayed as it is dialed out.

In the tone mode, the redial tone drive rate depends upon the time base as discussed before.

Storing of a Normally Dialed or Redialed Number into the External Memory

After the normal dialing or redialing operation, the telephone number can be stored in the external memory for future repertory dialing use by initiating the following key sequence.

1. Push "store" (ST) button.
2. Depress the single digit key corresponding to the desired address location.

Note that the "ST" keys are at locations (R_5, C_1) and (R_1, C_4).

Repertory Dialing

This is the most common mode of usage and allows the user to dial automatically any number stored in the memory. This mode is initiated by the following key sequence after entering the normal mode.

1. Push the "ML" key.
2. Push the single digit key corresponding to the desired address location.

The number is displayed as it is dialed out. In the tone mode, the tone driver rate is dependent on the time base as described earlier.

Pause

Note that the out dialing in the repertory or redial operation continues unless an access pause is detected. The outpulsing will stop and resume only when the user terminates the access pause by pushing the "ML" key again.

Program Modes (P/$\overline{N}$ = high, Reset = low)

Storing of a Telephone Number into the External Memory

During the store operation no out-dialing occurs. A telephone number can be stored in the desired address location by initiating the following key sequence.

1. Push the "ML" key (This instructs the device to accept a new number for storage into the internal memory.)
2. Enter the digits (including any access pauses) corresponding to the desired number. Digits will be displayed as they are entered.
3. Push the "ST" key.
4. Push the single digit key corresponding to the desired address location.

The entire sequence can be repeated to store as many numbers as desired. However, any memory locations not addressed with a telephone number "store" operation must be addressed with the following sequence.

1. Push the "ML" key.
2. Push the "ST" key.
3. Push the single digit key corresponding to the first unused memory location.
4. Push the "ST" key.
5. Push the single digit key corresponding to the next unused memory location.

Steps 4 and 5 are repeated until all remaining memory loccations have been addressed.

It should be noted that accessing all memory locations is required only for initial system set-up. This insures that no memory location will contain invalid data from memory power-up induced data and that location was addressed by the S2563, the S2563 would enter a "Halt" state and cease its normal program activities. To exit from this condition it is necessary to apply a momentary reset signal or toggle the P/$\overline{N}$ input.

Memory Expansion

The memory can be expanded by paralleling additional S5101 RAM's. External logic must be used to enable the desired RAM corresponding to a desired address location. The S2563 can drive up to 2 RAM's without the need of buffering address and data lines.

Keybounce Protection

When a key closure is detected by the S2563, an internal timeout (4ms at fo = 8kHz) is started. Any transitions that occur during this timeout will reset the timer to zero so that a key will only be accepted as valid after a noise free timeout period. The key must remain closed for an additional 16ms before released. Thus, the total make time of the key must be at least 20ms. The key must be released for at least 1ms before a new key is activated. Any transitions occurring when the key is released are ignored as long as the make time does not exceed 4ms.

Keyboard Entry Options

Figure 4 shows various options for arrangement of a keyboard for dialing of up to 29-8 digit or 15-16 digit numbers. A single S5101 memory is sufficient for number storage in the basic scheme.

Application Examples

Figures 6 and 8 respectively show the typical hookup schematics for the local power and telephone line power applications. Since power is available in the on-hook state of the telephone, store and display operations can be performed in this state for the local power application. In the telephone line power application, however, the device is put in the power-down mode to meet the on hook telephone leakage current specifications (5μA max). Store operation is performed in the off hook state by either storing the number after it is dialed out or by putting the device in the program mode by using a Prog/Norm switch. In this mode numbers can be stored without actually dialing them.

Table 1. Pin/Function Descriptions

Pin	Number	Function
Power (V_{DD}, V_{SS})	2	These are the power supply inputs. The device is designed to operate from 1.5V to 5.0V.
Keyboard (R_1-R_6, C_1-C_6)	12	These are 6 row and 6 column inputs from the keyboard contacts. When a key is pushed, an appropriate row and column input must go to V_{DD} or connect to each other. Figures 1 and 2 depict the standard telephone DPCT and X-Y matrix keyboard arrangements that can be used. A logic, interface is also possible as shown in Figure 3. Debouncing is provided to avoid false entry. Key pad entry options are shown in Figure 4.
Number Length Select (NLS)	1	This permits programming of the device to accept either 8-digit numbers or 16-digit numbers.
Mode Select (MODE)	1	This input allows the use of the device in either dial pulsing applications or tone drive applications.
Dial Rate Select (DRS)	1	This input allows selection of two different dialing rates such as 10 or 20 pps, 7 or 14 pps, etc. See Tables 2 and 3.
Inter-Digit Pause Select (IPS)	1	This allows selection of the pause duration that exists between dialed digits. It is programmed according to the truth table shown in Table 3. Note that preceeding the first dialed digit is an inter-digit time equal to the selected IDP. Two pause durations, either 400ms or 800ms are available at dialing rates of 10 and 20 pps. IDP's corresponding to other dialing rates can be determined from Tables 2 and 3.
Mark/Space Ratio Select (M/S)	1	This input allows selection of two mark/space ratios. High (V_{DD}) level selects 40/60 and low (V_{SS}) level selects 33/67.
Mute Output ($\overline{\text{MUTE}}$)	1	A pulse is available that can provide drive to turn on an external transistor to mute the receiver during dial pulsing. See Figure 5 for mute and dial pulse output relationship. It is also used as a keyboard disable in the tone drive applications. See Figure 6.
Dial Pulse Output ($\overline{\text{DP}}$)	1	Output drive is provided to turn on a transistor at the dial pulse rate. This output will be normally high and go low during "space" or "break."
Display Memory I/O Data (D_1-D_4)	4	These are 4 bidirectional pins for inputting and outputting data to the external memory and display driver.
Memory Enable (CE)	1	This line controls the external memory read/write functions in power down mode. It should be connected to the CE_2 input of the S5101 memory.
Memory Read/Write (R/$\overline{\text{W}}$)	1	This line controls the read or the write operation of the external memory. This output along with the CE output can be used to produce a pulse to update the external display. See Figure 6.
Tone Generator/Memory Address (A_0-A_7)	8	These are 8 output lines that carry the external memory address and tone generator row/column information.
Program/Normal (P/$\overline{\text{N}}$)	1	This input selects the operating mode. When high (V_{DD}) it puts the device in the program mode and numbers can be stored into memory. When low (V_{SS}) it allows normal operations.
Reset	1	This is a level reset input. When high (V_{DD}) the chip is forced into a power down mode.
Oscillator (OSC_i, OSC_m, OSC_0)	3	These pins are provided to connect external resistors R_I, R_M and capacitor C_O to form an R-C oscillator that generates the time base for the repertory dialer. The output dialing rate, tone drive rate and IDP are derived from this time base.
	40	

Table 2. Table for Selection of Oscillator Component Values for Desired Dialing Rate, I_{DP} or Tone Drive Rate

Dial Rate Desired (PPS)	Osc. Freq. fo (Hz)	Oscillator Components			Dial Rate (PPS)		IDP (ms)		Tone Drive On/Off Time (ms)
		R_M (kΩ)	(R_1) (kΩ)	C_O (pF)	DRS=V_{SS}	DRS=V_{DD}	IPS=V_{SS}	IPS=V_{DD}	
5.5/11	4400	TBD			5.5	11	1454	727	90/90
6/12	4800	220			6	12	1334	667	83.3/83.3
6.5/13	5200	190			6.5	13	1230	615	77/77
7/14	5600				7	14	1142	571	71/71
7.5/15	6000		1000	300	7.5	15	1066	533	66.7/66.7
8/16	6400				8	16	1000	500	62.5/62.5
8.5/17	6800	TBD			8.5	17	942	471	59/59
9/18	7200				9	18	888	444	55.5/55.5
9.5/19	7600				9.5	19	842	421	52.6/52.6
10/20	8000	110			10	20	865	405	54/55.5
(fo/800/ (fo/400)	fo				fo/800	fo/400	$\frac{6400 \times 10^3}{fo}$	$\frac{3200 \times 10^3}{fo}$	$\frac{400 \times 10^3}{fo}/\frac{400 \times 10^3}{fo}$

Figure 1. Standard Telephone Pushbutton Keyboard

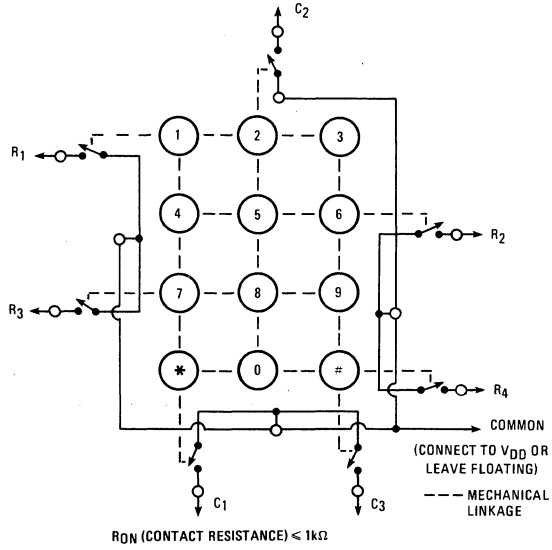
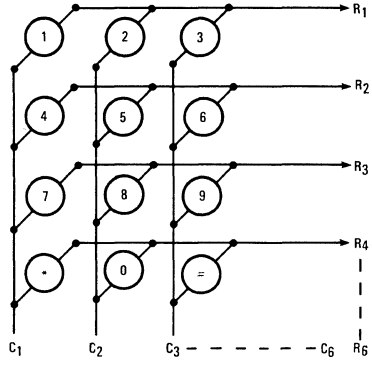


Figure 2. SPST Matrix Keyboard Arranged in the 2 of 12 Row, Column Format



SPST MATRIX KEYBOARD:

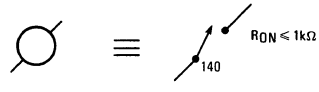
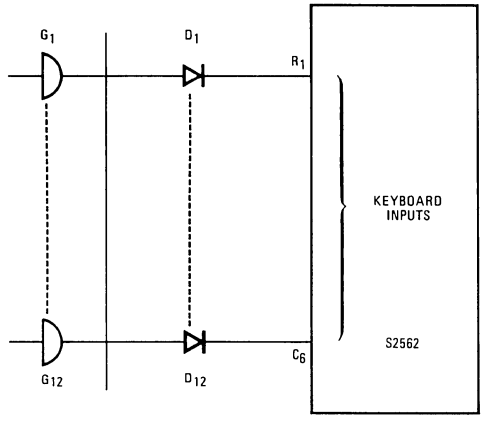


Figure 3. Logic Interface For The S2563



G_1 through G_{12} any CMOS type logic gates.
D_1 through D_{12} DIODES type 1N 914. (Optional)

A valid key closure corresponds to a logic high level on one row and one column

Figure 4. Example of Keypad Entry—Options
A. Using a Full Keyboard Provides Storage for 29-8 Digit Numbers

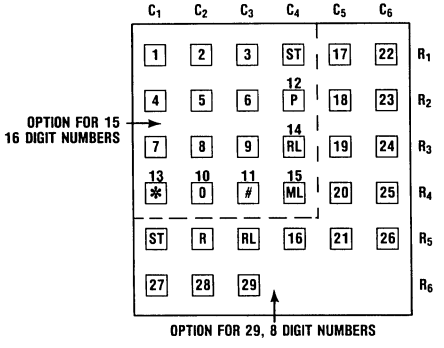


Figure 4B. Using a 4×4 Keyboard Provides Storage for 15-16 Digit Numbers

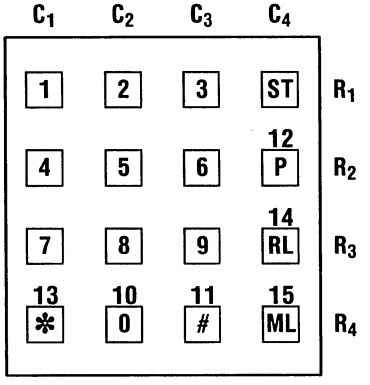


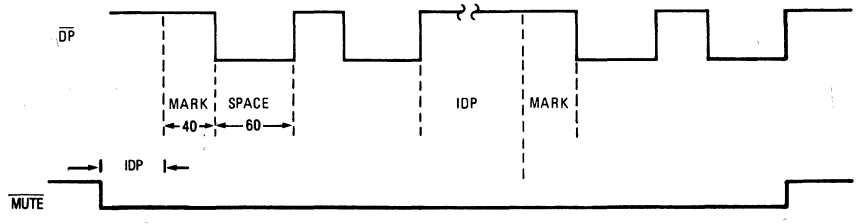
Table 3

Function	Pin Designation	Input Logic Level	Selection
Dial Rate Selection	DRS	V_{SS} V_{DD}	(fo/800) pps (fo/400) pps
Inter-Digit Pause Selection	IPS	V_{DD} V_{SS}	(3200/fo) S (6400/fo) S
Mark/Space Ratio Selection	M/S	V_{SS} V_{DD}	33/67 40/60
Program/$\overline{\text{Normal}}$	P/$\overline{\text{N}}$	V_{DD} V_{SS}	Program Normal
Mode Selection	MODE	V_{SS} V_{DD}	Dial pulse Tone Drive*
Number Length Selection	NLS	V_{SS} V_{DD}	8 digits 16 digits
Reset	Reset	V_{SS} V_{DD}	Normal Operation Power Down

*For tone mode also set DRS = V_{SS}, IPS = V_{SS} and M/S = V_{DD}.

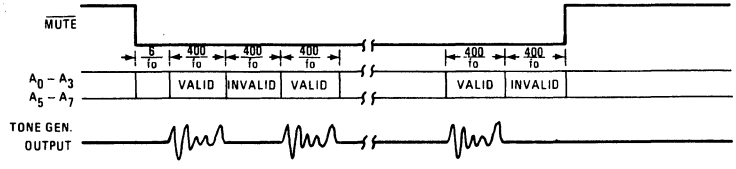
Note: fo is the oscillator frequency and is determined as shown in Table 2.

Figure 5A. Mute and Dial Pulse Output Timing Relationship



$\overline{\text{Mute}}$ will reset i) when the number of digits dialed out equals either the number of digits entered or the maximum selected (8 or 16) or ii) when an access pause is detected.

Figure 5B. Mute and Tone Output Timing Relationship



Mute output will reset i) when the number of digits dialed out equals the number of digits entered or equals the maximum selected (8 or 16) or ii) when an access pause is detected. In the normal dialing mode when digits are entered one at a time the mute output will reset between digits provided the time between entered digits exceeds $\frac{400}{fo}$. In both the normal dialing or automatic dialing mode tone will be output for a fixed duration of $\frac{400}{fo}$ (50msec for fo = 8kHz).

Table 4. Connection Table for Different Applications

Application	Pin	Connect to: (See figure below)
Telephone Line Power	P/N	Program/Normal Switch
	Reset	Hook Switch On Hook = V_{DD} Off Hook = V_{SS}
Local Power	P/N	Hook Switch On Hook = Program Mode (V_{DD}) Off Hook = Normal Mode (V_{SS})
	Reset	Hook Switch Power on reset circuit applying a momentary high level on power up or permanently connect to V_{SS}

Figure 6A. Local Power

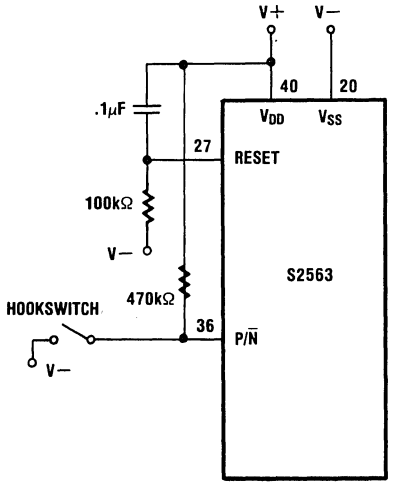


Figure 6B. Telephone Line Power

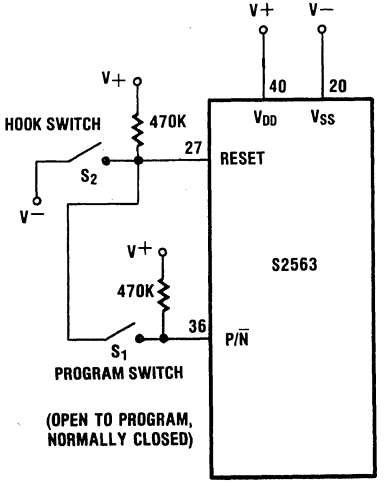


Figure 7. Typical Application of the S2563

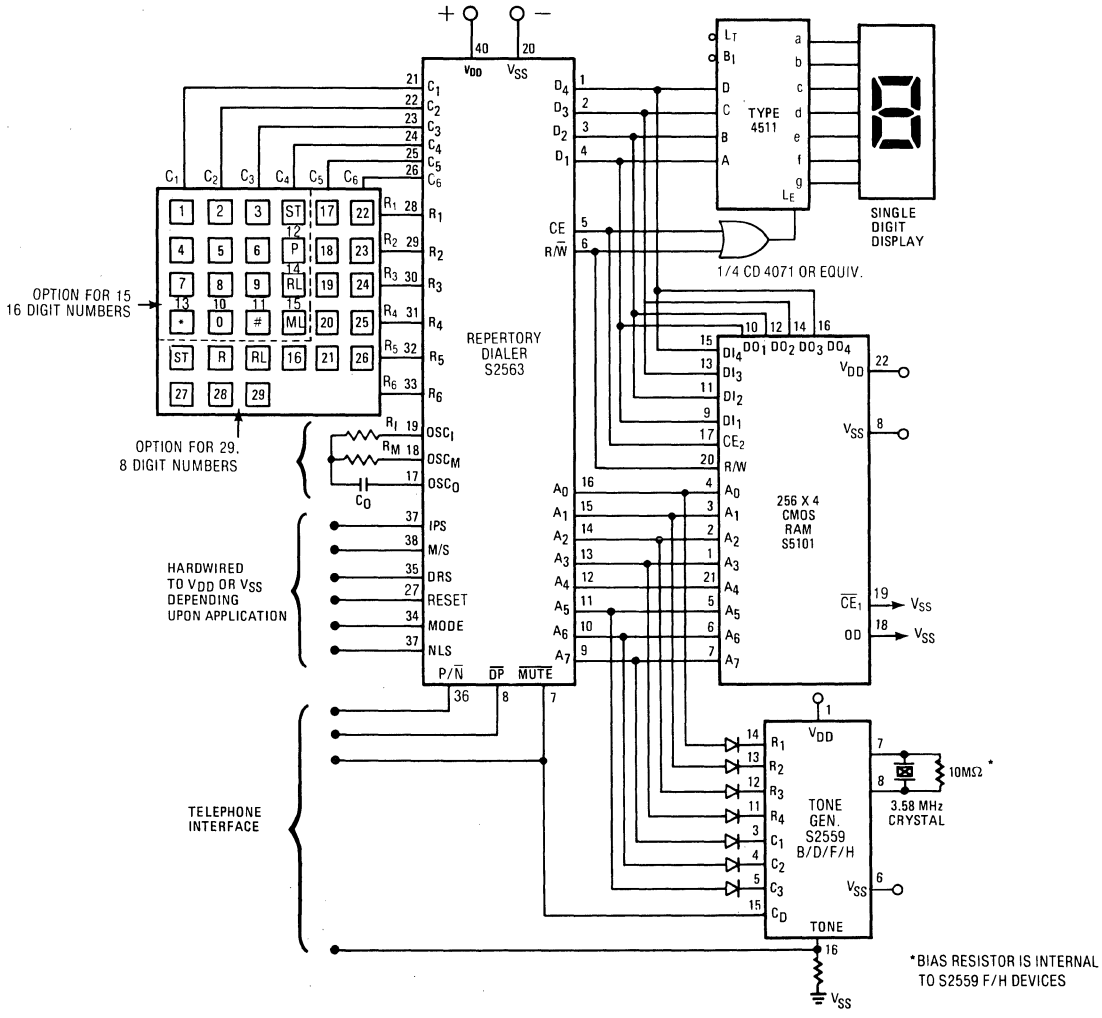


Table 5. Display Codes

Value Stored in Memory				Digit Value	Value Stored in Memory			
D_4	D_3	D_2	D_1		D_4	D_3	D_2	D_1
0	0	0	0	0	1	0	1	0
0	0	0	1	1	0	0	0	1
0	0	1	0	2	0	0	1	0
0	0	1	1	3	0	0	1	1
0	1	0	0	4	0	1	0	0
0	1	0	1	5	0	1	0	1
0	1	1	0	6	0	1	1	0
0	1	1	1	7	0	1	1	1
1	0	0	0	8	1	0	0	0
1	0	0	1	9	1	0	0	1
1	0	1	0	Not Used	0	0	0	0
1	0	1	1	Not Used	0	0	0	0
1	1	0	0	# (Pause)	1	1	0	0
1	1	0	1	Not Used	0	0	0	0
1	1	1	0	Beginning of Number	0	0	0	0
1	1	1	1	Blank	0	0	0	0

Table 6. Operating Sequences

1. **NORMAL DIALING**

   P/$\overline{N}$→NORM, [D_1], --- [D_n]

2. **ENTERING ACCESS PAUSE**

   ACCESS PAUSE ENTERED BY PUSHING [P] DURING NORMAL DIALING

3. **STORING OF A NUMBER AFTER DIALING**

   P/$\overline{N}$→NORM, [D_1] --- [D_n] —WAIT FOR DIALING TO COMPLETE— [ST], [LOC_n]

4. **REDIALING**

   P/$\overline{N}$→NORM, [RL]

5. **OVERRIDING ACCESS PAUSE**

   ACCESS PAUSE IS OVERRIDEN BY PUSHING [ML] TO CONTINUE FURTHER DIALING DURING A REPERTORY OR REDIALING SEQUENCE.

6. **REPERTORY DIALING**

   P/$\overline{N}$→NORM, [ML], [LOC_n]

7. **CASCADING NUMBERS IN REPERTORY DIALING**

   P/$\overline{N}$→NORM, [ML], [LOC_1] —WAIT FOR DIALING TO COMPLETE— [ML], [LOC_2] — etc.

8. **STORING OF NUMBERS IN MEMORY**

   P/$\overline{N}$→PROG, [ML], [D_1] --- [D_n], [ST], [LOC_1], [ML], [D_1] --- [D_n], [ST] [LOC_2] — etc.

NOTES: **1)** Function keys [ML], [RL], [P], [*] and [#] also designate memory locations 15, 14, 12, 13 and 11 respectively. Number can be stored in these locations by using the function keys as address keys in the appropriate sequence. To store a number in loc. 15 for example this sequence can be used P/$\overline{N}$→PROG, [ML], [D_1] --- [D_n], [ST], [ML]

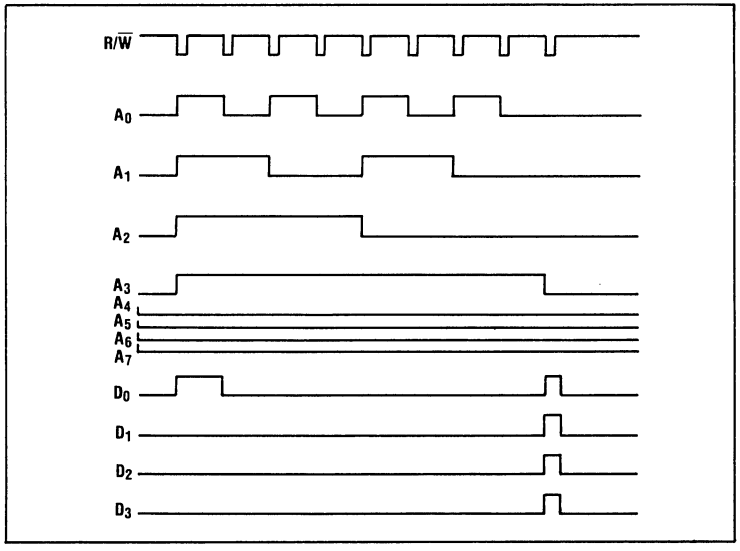
Similarly to dial a number stored in loc. 15 the following sequence can be used

P/$\overline{N}$→NORM, [ML], [ML]

Table 7. S2563 Memory Allocation

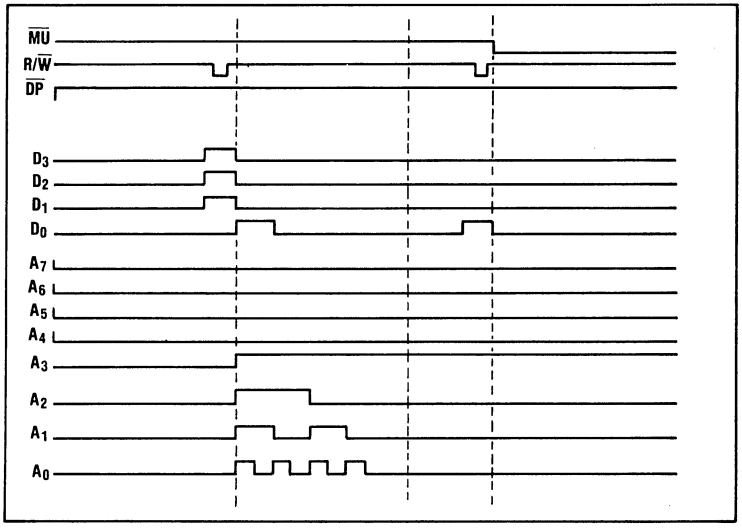
LOC.	ROW	COL.	8 DIGIT MODE MEM. ADDR. (HEX) D1 ..... D8	16 DIGIT MODE MEM. ADDR. (HEX) D1 ..... D16
1	R1	C1	0F 08	1F 10
2	R1	C2	17 10	2F 20
3	R1	C3	1F 18	3F 30
4	R2	C1	27 20	4F 40
5	R2	C2	2F 28	5F 50
6	R2	C3	37 30	6F 60
7	R3	C1	3F 38	7F 70
8	R3	C2	47 40	8F 80
9	R3	C3	4F 48	9F 90
10	R4	C2	57 50	AF A0
11	R4	C3	5F 58	BF B0
12	R2	C4	67 60	CF C0
13	R4	C1	6F 68	DF D0
14	R3	C4	77 70	EF E0
15	R4	C4	7F 77	FF F0
16	R5	C4	87 80	0F 00
17	R1	C5	8F 88	
18	R2	C5	97 90	
19	R3	C5	9F 98	
20	R4	C5	A7 ..... A0	
21	R5	C5	AF A8	
22	R1	C6	B7 ..... B0	
23	R2	C6	BF B8	
24	R3	C6	C7 ..... C0	
25	R4	C6	CF C8	
26	R5	C6	D7 ..... D0	
27	R6	C1	DF D8	
28	R6	C2	E7 ..... E0	
29	R6	C3	EF E8	

Figure 8A.



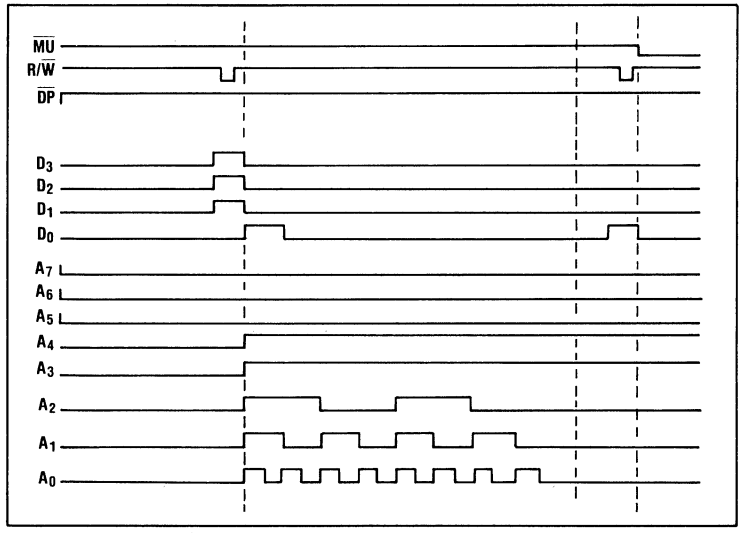
STORE INTO MEMORY
8 DIGIT MODE
LOCATION 1 DATA = 1

Figure 8B.



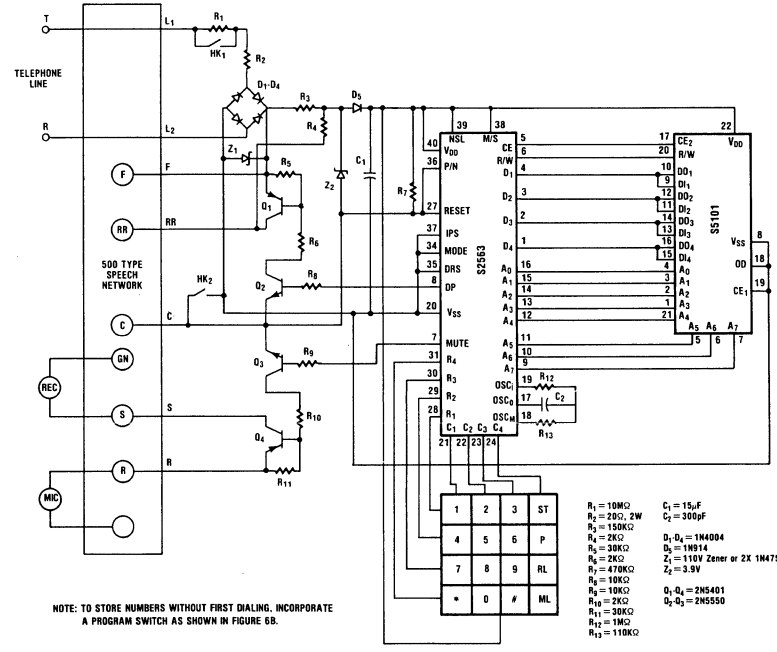
RECALL FROM MEMORY
8 DIGIT MODE
LOCATION 1

Figure 8C.



RECALL FROM MEMORY
16 DIGIT MODE
LOCATION 1

Figure 9. Typical Telephone Line Powered Repertory Dialer (Number Stored Offhook After Dialing is Completed)



NOTE: TO STORE NUMBERS WITHOUT FIRST DIALING, INCORPORATE A PROGRAM SWITCH AS SHOWN IN FIGURE 6B.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

RTDS2811

REAL-TIME DEVELOPMENT SYSTEM

Features

- ☐ **Provides Real-time (20MHz) Interactive Emulation for the AMI S2811 Signal Processing Peripheral**
- ☐ **Totally Self Contained (Internal Supply and Resident Software)**
- ☐ **Simple Interconnect Via RS232 to Port Users Terminal**
- ☐ **Full Software Capability Including Assembler and Editor**
- ☐ **In-Circuit Emulation Capability (Free Running with Breakpoints or Step-by-Step)**
- ☐ **Internal 6800 Based Microcomputer May be Used as Host Processor for S2811 Under Emulation**
- ☐ **Software Compatible with Software Simulator/ Assembler Program Package (SSPP2811)**

General Description

The RTDS2811 is a real-time in-circuit emulator for the AMI S2811 Signal Processing Peripheral (SPP). For information on the SPP chip please refer to the S2811 Advanced Product Description. The emulator is controlled from the user's terminal via the RS232 port at data rates up to 1200 bits/sec. The resident software package allows the user to load and assemble programs written in SPP Assembly language either from files or directly from the keyboard. The editor allows these programs to be modified by changing, inserting, or deleting instructions. The contents of the data memory may similarly be loaded from a file or created on-line and modified from the keyboard. Software switches control the interfaces to the emulator during emulation, allowing the system to be used as an in-circuit emulator in the user's prototype system, or to use the resident 6800 based microcomputer to operate as the host system. In the latter mode the system can be totally self-contained using file based I/O, eliminating the need to provide separate hardware for some phases of the emulation process. The system can be set to run continuously, conditionally, or step-by-step. In the conditional mode the system can be set to halt at breakpoints or on major flags (input, output, and overflow). The complete status of the system is displayed each time execution is halted, including in the step-by-step mode. Programs and memory maps created using the emulator can be used to generate the ROM mask for the S2811 by AMI.

Software generated by the RTDS2811 is totally compatible with the SSPP2811 Software Simulator/Assembler Program Package, allowing files to be transferred from one system to the other without modification.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

SSPP2811

SOFTWARE SIMULATOR/ASSEMBLER PROGRAM PACKAGE

Features

- ☐ **Provides Exact Simulation of Operation of AMI S2811 Signal Processing Peripheral**
- ☐ **Written in ANSI Fortran IV for Maximum Portability**
- ☐ **Runs on Any 16-Bit or Larger Computer With 28K Memory and Fortran IV Compiler**
- ☐ **Available Internationally on National CSS Time-sharing Service**
- ☐ **Allows Continuous or Step-by-Step Operation**
- ☐ **Allows Setting of Breakpoints on All Major Flags**
- ☐ **Trace Buffer Allows Storage and Display of Status of Previous 50 Instructions During Continuous Operation**
- ☐ **Software Compatible with Real-Time Development System (RTDS2811)**

General Description

The SSPP2811 is a software simulator for the AMI S2811 Signal Processing Peripheral (SPP). For information on the SPP chip please refer to the S2811 Advanced Product Description. The program is written in ANSI Standard Fortran for maximum portability. The machine specific software is reduced to a minimum and is available for several popular ranges of computers including Burroughs 7700, PRIME 400, and Amdahl 470 (IBM compatible). Experienced Fortran programmers will have no difficulty in writing these small routines for other machines. As well as being available in source code form on magnetic tape, the program is available already implanted on the National CSS, Inc. Timesharing Service. For information on the NCSS system please contact your local NCSS office.

The SSPP2811 package allows the user to simulate the operation of the S2811 chip either in a step mode or free running, with or without breakpoints. Data I/O for the simulation may be provided by means of files or directly from the terminal. An assembler allows the user to input the SPP program (in SPP Assembly Language) and the memory data either from a file or from the keyboard. The assembly listing may be dumped to file which can then be used to generate the ROM mask for the S2811 by AMI. During simulation a trace buffer may be used to store the last 50 (maximum) instructions executed. This greatly facilitates continuous simulation in conjunction with the breakpoints which may be set on (1) any individual instruction (2) the input flag (3) the output flag (4) overflow in the accumulator. The trace feature, either using the trace buffer or in the step-by-step mode, gives the user the complete status of the simulation, including the last instruction executed and the conditions of all internal registers, counters, latches, and busses.

Software generated by the SSPP2811 is totally compatible with the RTDS2811 Real-Time Development System, allowing files to be transferred from one system to the other without modification.

AMERICAN MICROSYSTEMS, INC.

S2811

SIGNAL PROCESSING PERIPHERAL

Features

- ☐ Programmable for Digital Processing of Signals in Voice-Grade Communications Systems and Other Applications with Signals in the Audio Frequency Range
- ☐ On-Chip 12-Bit Parallel Multiplier (One Cycle Multiplication Time)
- ☐ Built-in Program ROM (256x17)*, 3-Port Data Memory (256x16) and Add/Subtract Unit (ASU)
- ☐ Pipeline Structure for High Speed Instruction Execution (300ns Cycle Time)
- ☐ Bus-Oriented Parallel I/O for Easy Microprocessor Interface
- ☐ Additional Double Buffered I/O for Ease of Asynchronous Serial Interface
- ☐ On-Chip Crystal Oscillator (20MHz) Circuit
- ☐ Pre-Programmed Standard Parts Available

General Description

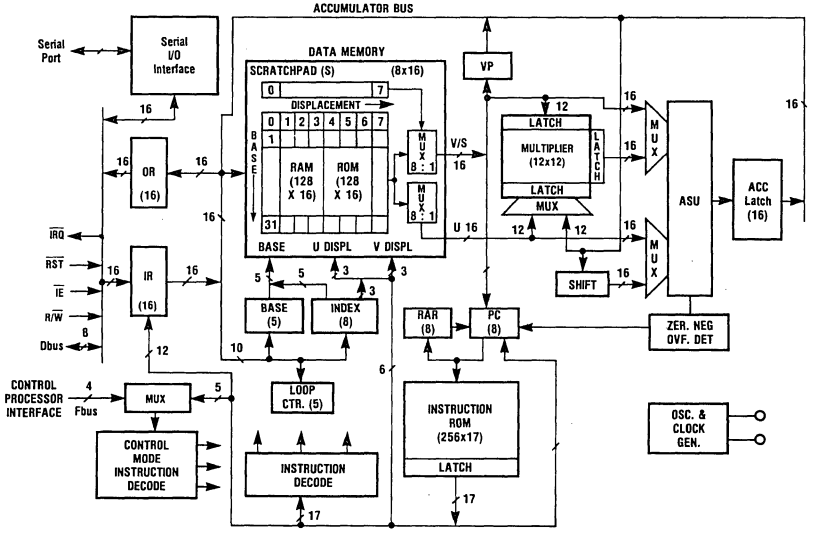
The S2811 Signal Processing Peripheral (SPP) is a high speed special purpose arithmetic processor with on-chip ROM, RAM, multiplier, adder/subtractor, accumulator and I/O organized in a pipeline structure to achieve an effective operation of one multiply, add and store of up to 12-bit numbers in 300 nanoseconds.

User Support

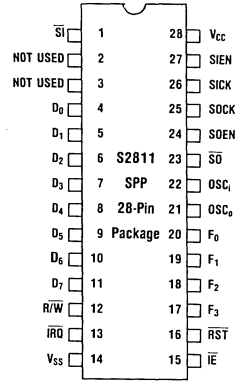
A real time in circuit emulator, the RTDS2811 is available. This is a fully compatible hardware emulator with software assembler/disassembler and editor for rapid program development and debugging. An S2811 assembler and software simulator program package SSPP2811 is also available.

*Out of the 256 instruction locations of the ROM, 250 are usable by the user program. Six instruction locations are reserved for in-house testing.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C

Electrical Specifications: (V_{CC}=5.0V ±5%, V_{SS}=0V, T_A=0°C to +70°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Logic "1" Voltage	2.0		V_{CC}+0.3	V	V_{CC}=5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC}=5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μAdc	V_{IN}=0V to 5.25V
C_I	Input Capicitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD}=−100μA, V_{CC}=min, C_L=30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD}=1.6mA, V_{CC}=min, C_L=30pF
f_{CLK}	Clock Frequency	5.0	20		MHz	V_{CC}=5.0V
P_D	Power Dissipation		1.2		W	V_{CC}=5.0V
f_{CLK}(max)	Maximum Clock Frequency				MHz	V_{CC}=5.0V
	S2811-10	10				
	S2811-12	12				
	S2811-15	15				
	S2811	20				

SPP Pin Function/Descriptions

Microprocessor Interface (16 pins)

D_0 through D_7 (Input/Output) Bi-directional 8-bit data bus. Maximum load 1 TTL (See above).

F_0 through F_3 (Input) Control Mode/Operation Decode. Four microprocessor address leads are used for this purpose. See "SPP CONTROL MODES AND OPERATIONS." (Table 1)

$\overline{IE}$ (Input) Interface Enable. A low level on this pin enables the SPP microprocessor interface. Generated by microprocessor address decode logic.

R/$\overline{W}$ (Input) Read/Write Select. When HIGH, output data from the SPP is available on the data bus. When LOW, data can be written into SPP.

$\overline{IRQ}$ (Output) Interrupt Request. This open-drain output will go LOW when the SPP needs service from the microprocessor.

$\overline{RST}$ (Input) When LOW, clears all internal registers and counters, clears all modes and initiates program execution at location 00.

Serial Interface (6 pins)

SICK, SOCK	Serial Input/Output Clocks. Used to shift data into/out of the serial port.
$\overline{SI}$	(Input) Serial Input. Serial data input port. Data is entered MSB first and is inverted.
SIEN	(Input) Serial Input Enable. A HIGH on this input enables the serial input port. The length of the serial input word (16 bits maximum) is determined by the width of this strobe.
$\overline{SO}$	(Output) Serial Output. Three-state serial output port. Data is output MSB first and is inverted.
SOEN	(Input) Serial Output Enable. A HIGH on this input enables the serial output port. The length of the serial output (16 bits maximum) is determined by the width of this strobe.

Miscellaneous

OSC_i, OSC_o	An external crystal with suitable capacitors to ground can be connected across these pins to form the time base for the SPP. An external clock can also be applied to OSC_i input if the crystal is not used. All timings shown in this Product Description assume a 20MHz clock frequency.
V_{CC}, V_{SS}	Power supply pins $V_{CC}=+5V$, $V_{SS}=0$ volt (ground).

Note: Do not make connections to pins 2 and 3.

Functional Description

The main functional elements of the SPP (see Block Diagram) are:

1. a 256x17 ROM which contains the user program,
2. a 3-port 256x16 data memory (one input and two output ports) which allows simultaneous readout of two words,
3. a 12-bit high-speed parallel multiplier,
4. an Add/Subtract unit (ASU),
5. an accumulator register, and,
6. I/O and control circuits.

The SPP is implemented in a combination of clocked and static logic which allows complete overlap of the multiply operation with the read, accumulate, and write operations. The basic instruction cycle is "Read, Modify, Write" where the "Read" brings the operands from the RAM to the multiplier and/or the product of the previous operands, and the "Write" stores the result of the "Modify." The cycle time for the instruction is 300 nanoseconds. This results in an arithmetic throughput of about 3.3 multiply and accumulate operations per microsecond. Figure 1 illustrates the SPP Instruction Formats. The OP1 and OP2 instructions are listed in Tables 2 and 3 and Figure 2 illustrates the basic instruction timing.

The SPP is intended to be used as a microprocessor peripheral. The SPP control interface is directly compatible with the 6800 microprocessor bus, but can be adapted to other 8-bit microprocessors with the addition of a few MSI packages.

The high-speed number crunching capability of the SPP gives a standard microprocessor system the necessary computational speed to implement complex digital algorithms in real time.

Operating in a microprocessor system, the SPP can be viewed as a "hardware subroutine" module. The microprocessor can call up a "subroutine" by giving a command to the SPP. A powerful instruction set (including conditional branching and one level of subroutine) permits the SPP to function independently of the microprocessor once the initial command is given. The SPP will interrupt the microprocessor upon completion of its task. The microprocessor is free to perform other operations in the interim.

The SPP contains a high-speed serial port for direct interface to an analog-to-digital (A/D) converter. In many applications, real-time processing of sampled analog data can be performed within the SPP without tying up the main microprocessor. Data transfer to the microprocessor occurs upon completion of the SPP processing. The SPP interface environment is summarized in Figure 3.

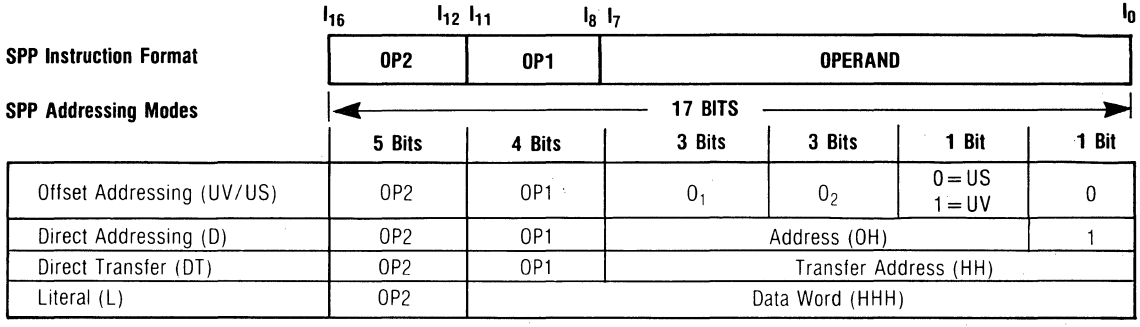
Separate input and output registers exchange data with the SPP data ports. Serial interface logic converts the parallel 2's complement data to serial 2's complement or sign + magnitude format. Data format and source (serial or parallel port) is software selectable.

Table 1 summarizes direct commands given to the SPP from the control processor. These control modes are specified via four address lines brought to the SPP.

The SPP is a memory-mapped peripheral, occupying 16 locations of the microprocessor memory space. Providing the proper SPP address will activate the corresponding control mode.

The control modes and the LIBL command enable real-time modification of the SPP programs. This permits a single SPP program to be used in several different applications. For example, an SPP might be programmed as a "universal" digital filter, with cutoff frequency, filter order, and data source (serial or parallel port) selected at execution time by the control microprocessor.

Figure 1. S2811 Object Code Instruction Formats.



Addressing Mode	Effective Address U	Effective Address V/S	Multiplier Operands
UV	(BAS)+O_1	V=(BAS)+O_2	P=U•V
US	(BAS)+O_1	S=O_2	P=U•S
D	—	OH	P=A•V

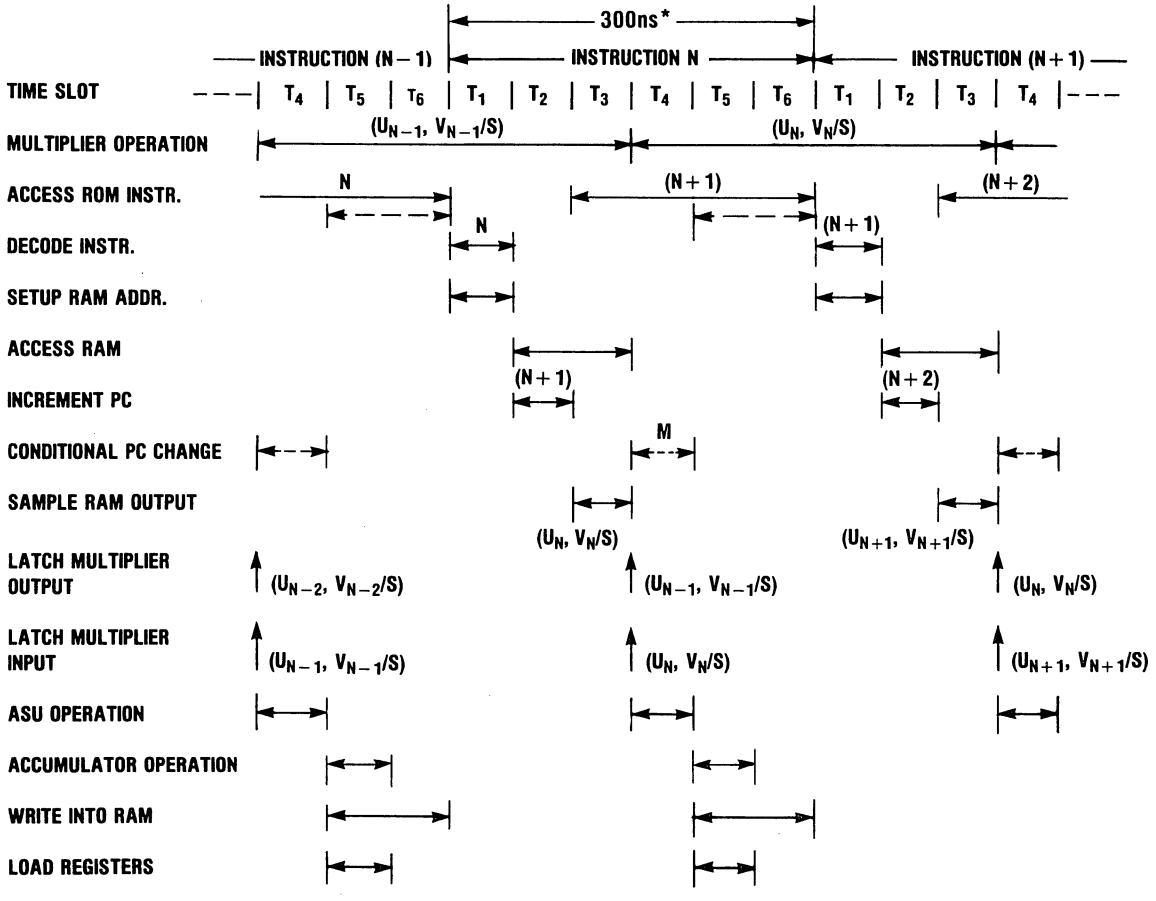
NOTE: O indicates an octal digit (3 bits) and H indicates a hexadecimal digit (4 bits)

Table 1. SPP Control Modes and Operations

Input leads F_0-F_3 define several control modes and operations to facilitate the interface between the SPP and a control processor. In general, these inputs are derived from the control processor address leads. The SPP will therefore occupy 16 memory locations, being a memory mapped peripheral.

F-Bus (F_3-F_0) Hex Value	Mnemonic	Control Modes and Operations: Operation/Function
0	CLR (Clear)	Resets control modes to normal operation.
1	RST (Reset)	Software master reset. Clears all SPP registers and starts execution at location 00. Also resets control modes to normal operation.
2	DUH (Data U/H)	Specifies MSByte of data word. DUH terminates data word transfer.
3	DLH (Data L/H)	Specifies LSBs of data word.
4	XEQ (Execute)	Starts execution at location specified on data lines (HH).
5	SRI (Ser. Inp.)	Enables serial input port.
6	SRO (Ser. Out.)	Enables serial output port.
7	SMI (S/M Inp.)	Converts sign-magnitude serial input data to 2's complement form.
8	SMO (S/M Out.)	Converts 2's complement internal data to sign-magnitude serial output.
9	BLK (Block)	Enables block data transfer.
A	XRM (Ext. ROM)	Permits control of SPP using external instruction ROM. A special mode used primarily for testing.
B	SOP	Set Overflow Protect (Normal mode of operation).
C	COP	Clear Overflow Protect.
D,E,F		Do not use.

Figure 2. SPP Instruction Timing Diagram



*ASSUMES 20MHz CLOCK FREQUENCY

EACH TIME SLOT = 50ns*

Figure 3. SPP Interface Environment

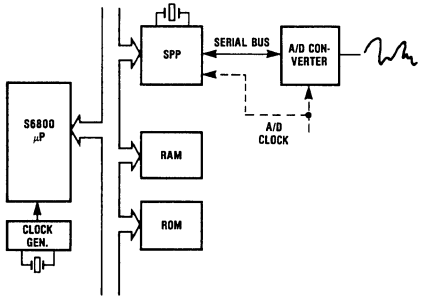


Figure 4. Loading BASE and INDEX Registers and LOOP and PROGRAM Counters

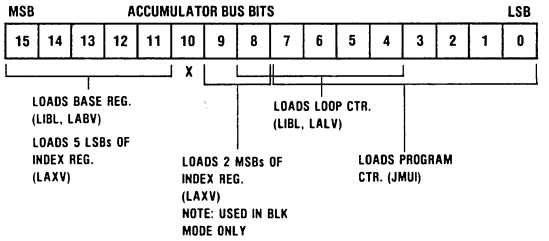


Figure 5A. SPP to 6800 Interface

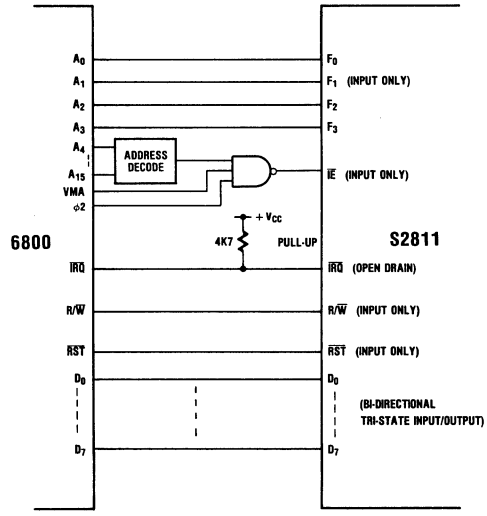
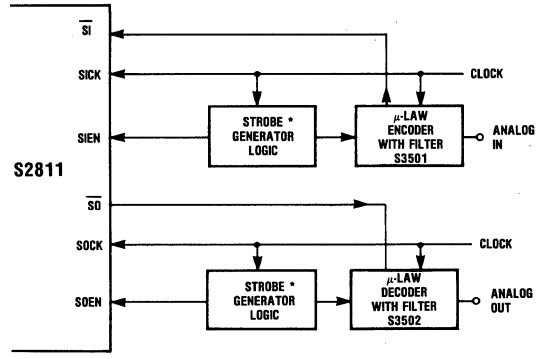


Figure 5B.



Note 1. μlaw↔linear conversion is performed by the SPP software.

*Note 2. The input and output clocks and strobe generators may be realized with two (2) CMOS packages.

Figure 5C. SPP Serial Port to PCM BUS Interface

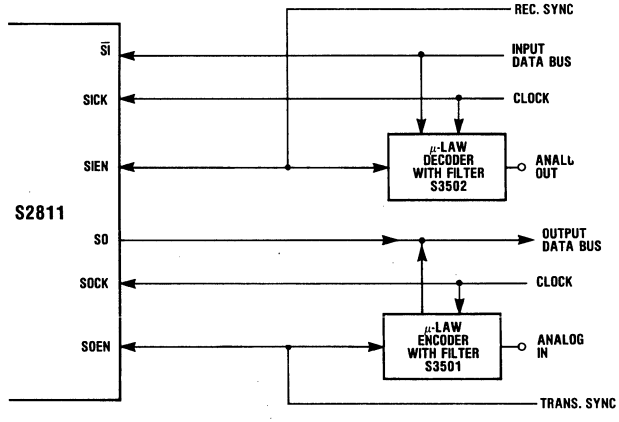
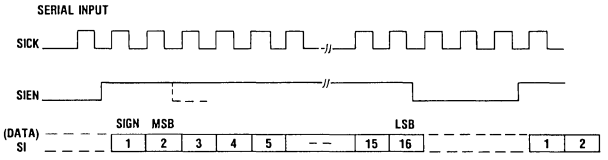
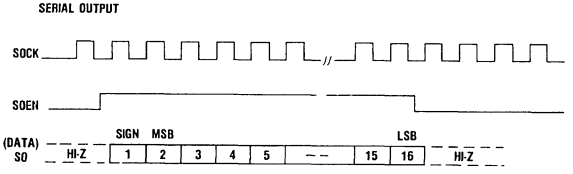


Figure 5D. SPP Serial Interface Timing

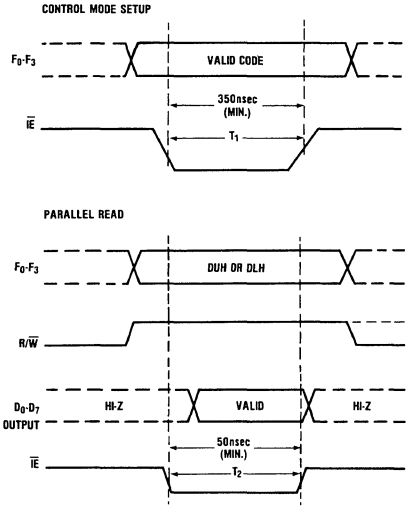


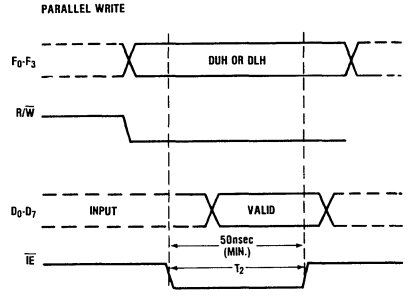
1. SIEN MUST BE SYNCHRONIZED TO THE FALLING EDGE OF SICK SUCH THAT THE RISE AND FALL OF SIEN FOLLOW FALLING EDGE OF SICK.
2. DATA MAY CONTAIN 1 TO 16 BITS DEFINED BY WIDTH OF SIEN. SPP WILL LEFT JUSTIFY DATA WORDS 16 BITS.
3. DATA ARE SAMPLED ON THE TRAILING EDGE OF SICK.
4. MINIMUM 16 SICK PULSES + 64 CYCLES OF S2815 OSCILLATOR ARE REQUIRED BETWEEN SIEN RISING EDGES.
5. IF SERIAL INPUT BUFFER IS FULL, SPP WILL IGNORE NEW INPUT SAMPLES.
6. THE SERIAL DATA IS INVERTED AND MAY BE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.



1. RISE AND FALL OF SOEN MUST FOLLOW FALLING EDGE OF SOCK.
2. OUTPUT DATA WILL BE 1 TO 16 BITS DEFINED BY WIDTH OF SOEN.
3. DATA ARE VALID FROM RISING EDGE TO RISING EDGE OF SOCK SO THAT THE RECEIVING SYSTEM CAN SAMPLE DATA ON TRAILING EDGE.
4. MINIMUM 16 SOCK PULSES + 64 CYCLES OF S2815 OSCILLATOR ARE REQUIRED BETWEEN SOEN RISING EDGES.
5. IF THE SERIAL OUTPUT BUFFER IS EMPTY, ALL ONES WILL BE OUTPUT.
6. SO WILL BE IN A HIGH IMPEDANCE STATE WHEN NOT ENABLED BY SERIAL OUTPUT SEQUENCE.
7. THE SERIAL DATA IS INVERTED AND MAYBE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.

Figure 5E. SPP Parallel Interface Timing





NOTE: ALL TIMES SHOWN ARE MINIMUM AND MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS AS FOLLOWS:

$T_{1\ MIN} = \left[\frac{6000}{f_{CLK}}\right] + 50$ nsec

$T_{2\ MIN} = \frac{1000}{f_{CLK}}$ nsec

WHERE f_{CLK} IS IN MHz

Table 2. SPP Instruction Set

OP1 Instructions

Type	Mnemonic	Hex Code I11-18	Address Modes	Operations	Description
No Operation	**NOP**	0	- - -	None	**No OP**eration
Accumulator Operations	**ASB**	C	- - -	ABS (A)→A	**ASB**olute value of accumulator is placed in accumulator.
	NEG	D	- - -	—(A)→A	**NEG**ate accumulator contents (two's complement) and replace in accumulator.
	SHR	E	- - -	(A)/2→A	**SH**ift **R**ight accumulator contents 1-bit position. Equivalent to dividing contents by two.
	SGV	F	UV/US, D	(A)→A, if sign (A) = sign V/S −(A)→A, if sign (A)≠sign V/S	**Sg**n of RAM output **V** is the sign of accumulator contents. Accumulator contents are negated (two's complement) if different sign from V. Useful in implementing hard limiter function.
Addition Operations	**AUZ**	2	UV/US	(U) + 0→A	**A**dd **U** and **Z**ero. Loads RAM output U into the accumulator.
	AVZ	1	UV/US, D	(V/S) + 0→A	**A**dd **V**/S and **Z**ero. Loads RAM output V/S into the accumulator.
	AVA	8	UV/US, D	(V/S) + (A)→A	**A**dd **V**/S and **A**ccumulator contents. Sum is placed back into accumulator.
	AUV	4	UV/US	(U) + (V/S)→A	**A**dd RAM outputs **U** and **V**/S and place sum in accumulator.
Subtraction	**SVA**	9	UV/US, D	(V/S)—(A)→A	**S**ubtract **V**/S and **A**ccumulator contents. The difference (V—A) is placed in the accumulator.
	SVU	5	UV/US	(V/S)—(U)→A	**S**ubtract RAM outputs **V** and **U** and place difference (V—U) in the accumulator.
Multiply/ Add Operations	**APZ**	3	- - - (current inst.) UV/US, D (prec. instr)	(P) + 0→A	**A**dd **P**roduct and **Z**ero. Loads multiplier product into the accumulator. The multiplier inputs were set up in the preceding instruction by addressing mode.
	APA	A	- - - (current inst.) UV/US, D (prec. instr)	(P) + (A)→A	**A**dd **P**roduct and **A**ccumulator contents. Result is placed in the accumulator. The multiplier inputs were set up in the preceding instructions by addressing mode.
	APU	6	UV (current instr) UV/US, D (prec. instr)	(P) + (U)→A	**A**dd **P**roduct and RAM output **U**. Sum is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.
Multiply/ Subtract Operations	**SPA**	B	- - - (current instr) UV/US, D (prec. instr)	(P)—(A)→A	**S**ubtract **P**roduct and **A**ccumulator contents. Difference (P—A) is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.
	SPU	7	UV/US (current instr) UV/US, D (prec. instr)	(P)—(U)→A	**S**ubtract **P**roduct and RAM output **U**. Difference (P—U) is placed in accumulator. The multiplier inputs were set up in preceding instruction by addressing mode.

Table 3. SPP Instruction Set
OP2 Instructions

Type	Mnemonic	Hex Code I16-I12	Address Modes	Operations	Description
Load Instructions	**LLTI**	1E	Literal	HHH→IR	**L**oad **LiT**eral in **I**nput register. A 12-bit (3 hex digits) literal is transferred to the input register. This instruction cannot be used with an OP1 instruction or with a specified addressing mode. Literal is left justified to occupy bits 4-15 in register.
	LIBL	07	- - -	(IR)→BAS (IR)→LC	**L**oad **I**nput contents to **B**ase register and **L**oop counter. See Figure 4. Clears input flag (LOW).
	LACO	02	- - -	(A)→OR	**L**oad **AC**cumulator contents into the **O**utput Register. This is the basic data output instruction. Sets output flag (HIGH). The IRQ line will be set low if the SRO mode is not set.
	LAXV	05	UV/US, D	(A)→IX, V/S (A)→A	**L**oad **A**ccumulator contents into index register and RAM location **V**/S. Accumulator is truncated to 5 most significant bits after the operation. See Figure 4.
	LALV	04	UV/US, D	(A)→LC, V/S	**L**oad **A**ccumulator to **L**oop counter and RAM location **V**/S. See Figure 4.
	LABV	03	UV/US, D	(A)→BAS, V/S (A)→A	**L**oad **A**ccumulator to **B**ase and RAM location **V**/S. Truncate accumulator contents to most significant 5 bits after the operation. See Figure 4.
Data Transfer Instructions	**TACU**	0B	UV/US	(A)→U	**T**ransfer **A**ccumulator **C**ontents into RAM location **U**.
	TACV	0C	UV/US, D	(A)→V/S	**T**ransfer **A**ccumulator **C**ontents into RAM location **V**/S.
	TIRV	08	UV/US, D	(IR)→V/S	**T**ransfer **I**nput **R**egister Contents to RAM location **V**/S. This is the basic data input instruction. Clears input flag (LOW).
	TVPV	09	UV/US, D	VP→V/S	**T**ransfer contents of **VP** register (equals previous value of output V) to RAM location **V**/S.
	TAUI	10	UV/US	(A)→U	**T**ransfer **A**ccumulator contents into RAM location **U** using **I**ndex register as base.
Accumulator Operations	**CLAC**	01	- - -	0→A	**CL**ear the **AC**cumulator. Forces SWAP mode to normal operation and clears overflow flag.
Register Manipulation Instruction	**INIX**	0D	- - -	(IX) + 1→IX	**IN**crement the **IndeX** register.
	DECB	0E	- - -	(BAS)—1→BAS	**DEC**rement the **B**ase register.
	INCB	0F	- - -	(BAS) + 1→BAS	**INC**rement the **B**ase register.
	SWAP	06	- - -	BAS↔IX	**SWAP** the roles of Base and Index registers.
Unconditional Branch Instruction	**JMUD**	15	DT	HH→PC	**Ju**M**p** **U**nconditionally **D**irect to location indicated by 8-bit (two hex digits) literal HH. Cannot be used with an OP1 instruction requiring specific addr. mode.
	JMUI	11	UV/US, D	[(IX)]→PC	**Ju**M**p** **U**nconditionally **I**ndirect to location indicated by contents of RAM address pointed to by index and displacement indicated by V/S. $[V/S)_{0\text{-}7}]$→PC.
Conditional Branch Instructions	**JMCD**	16	DT	HH→PC, if LC≠0 (LC)—→LC	**Ju**M**p** **C**onditionally **D**irect to location indicated by 8-bit (two hex digits) literal HH, if loop counter is not zero. Loop Counter is decremented after the test.
	JMPZ	19	DT	HH→PC if (A) = 0	**Ju**M**P** to location specified if accumulator contents are **Z**ero as a result of previous instruction.
	JMPN	1A	DT	HH→PC if (A) :	**Ju**M**P** to location specified if accumulator contents are **N**egative as a result of previous instruction.
	JMPO	1B	DT	HH→PC if (A) Overflows	**Ju**M**P** to location specified if accumulator **O**verflows as a result of previous instruction. Clears overflow flag.
	JMIF	1C	DT	HH→PC if IF = 0	**Ju**M**p** if **I**nput **F**lag is low to location specified (Note 4). IRQ line will be set low if the SRI mode is not set.
	JMOF	1D	DT	HH→PC if OF = 1	**Ju**M**p** if **O**utput **F**lag is high to location specified (Note 4).
Subroutine Instruction	**JMSR**	14	DT	(PC) + 1→RAR, HH→PC	**Ju**M**p** to **SubR**outine. Execution jumps unconditionally to location indicated by 8-bit (two hex digits) literal HH. Return address is stored in RAR. Cannot be used with an OP1 instruction requiring specified address mode.
	RETN	13	- - -	(RAR)→PC	**RET**ur**N** from subroutine. Execution continues at instruction following the JMSR instruction.

Table 3. SPP Instruction Set
OP2 Instructions (Continued)

Type	Mnemonic	Hex Code I16-I12	Address Modes	Operations	Description
Complex Instructions	**JCDT**	18	DT	HH→PC if LC≠0, (LC)—1→LC (BAS) + 1 →BAS, (IX) + 1→IX	**J**ump **C**onditionally **D**irect Dual **T**racking. Increment base and Index registers. Loop Counter is decremented after test.
	JCDI	17	DT	HH→PC if LC ≠0, (BAS) + 1→BAS (LC)—1→LC	**J**ump **C**onditionally **D**irect and **I**ncrement base register. Loop Counter is decremented after test.
	TVIB	0A	UV/US	(VP)→V/S, (BAS) + 1→BAS	**T**ransfer contents of VP register to RAM location **V**/S and **I**ncrement **B**ase register.
	MODE	1F	- - -	Control mode replaces OP1	OP1 code in this instruction can select any one of the several control **MODE**s/operations specified in Table 1.
	REPT	12	- - -	PC inhibited if LC≠0 (next instruction) (LC)—1→LC (each iteration of next instruction.)	**REP**eat next instruction until LC = 0. Increment PC to access next instruction, then suppresses increment of PC if LC≠0. Loop Counter is decremented when REPT is executed, so that number of repeats is equal to original value of LC.

NOTES:
1. Whenever the Index register is selected by an instruction OP2 it controls the entire line of code.
2. Loop Counter cannot underflow.
3. S refers to scratchpad.
4. Input flag is low if SPP has not received a new input word.
5. (A) represents truncation of the accumulator to 5 most significant bits (sign and 4 MSB).
6. Multiplier input latches and the VP register are not updated when either the DT or L addressing modes are used in conjunction with an OP2 instruction.
7. - - - indicates don't care address mode.
8. When D address mode is used, accumulator contents as a result of previous instruction replace U input to multiplier.

SPP Addressing Modes

The SPP provides four methods of data access (see Figure 1). In the direct mode, the full address of the data is specified. Due to limitations in the instruction word size, only one data word at a time may be accessed in this manner, and only even displacement addresses.

In the relative (to base) mode the base register is set up using a LLTI/LIBL sequence, or LABV, and two data words are accessed simultaneously by specifying U and V displacements in the instruction word.

Data may be stored/retrieved from the scratchpad memory by specifying the scratchpad mode and providing scratchpad and U port displacements. The U port data is accessed relative to the base register. The scratchpad data is treated exactly the same as data accessed via the U and V RAM ports, except the 8-word scratchpad block is substituted for the V data block.

The fourth addressing mode is dual-tracking base addressing. This mode greatly increases throughput in matrix operations.

The JMIF and JMOF instructions provide the capability to synchronize the SPP when operating in synchronous sampled data systems. When executed these commands cause the SPP to set the $\overline{IRQ}$ output low, thus requesting service from the microprocessor. The SPP can be put in a wait loop until a new data sample is available at the IR or has been read from the OR, as appropriate. The TIRV and LIBL commands facilitate transfer of input data from the IR to data memory or the base register and loop counter respectively. LACO command provides for data transfer to the OR.

Block Data Transfer (BLK Mode)

The contents of the RAM portion of the data memory may be loaded or dumped via the parallel interface by use of the Block Transfer mode. This mode is ideally suited for transfer using a DMA Controller. The sequence and timing are shown in Figure 6. Eight bit words may be transferred using the DUH mode only. The memory is addressed by the index register in this mode, and the register is automatically incremented after each word transfer. The displacement is addressed by the 2 most significant bits of this register (see Figure 4) so that the addressing is done base-by-base, then next displacement, i.e., columnwise. The starting address is selected by pre-

setting the Index Register (using the LAXV instruction) before setting the SPP into the BLK mode. The last address will depend on the number of word transfers executed. Note that the address following Base 31, Displacement 3 is Base 0, Displacement 0. This allows the continuous transfer of any number of words to be executed, starting at any address. The status of the R/$\overline{W}$ line is latched into the chip when the BLK mode is set up, eliminating the need to control this line when the block transfer is being done under the direct control of the host processor. When using a microprocessor to execute the block read it will normally be advantageous to set the interrupt mask.

Figure 6A. Block Read Sequence/Timing

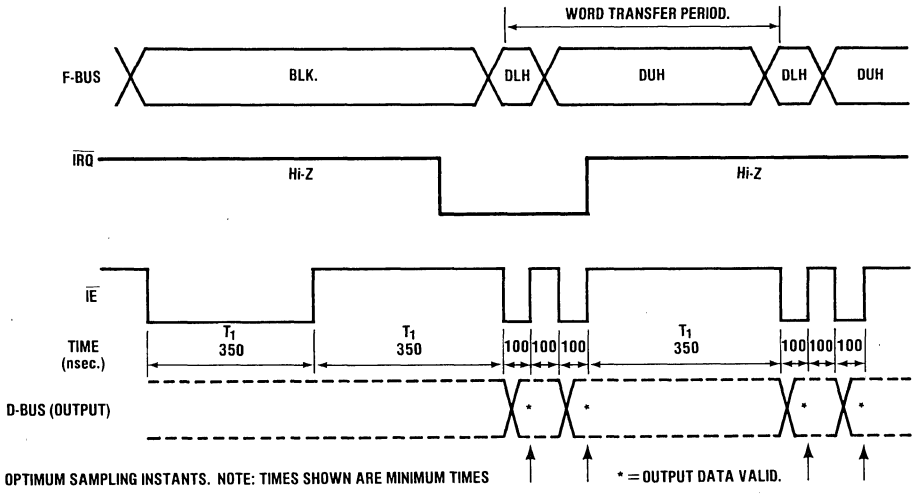
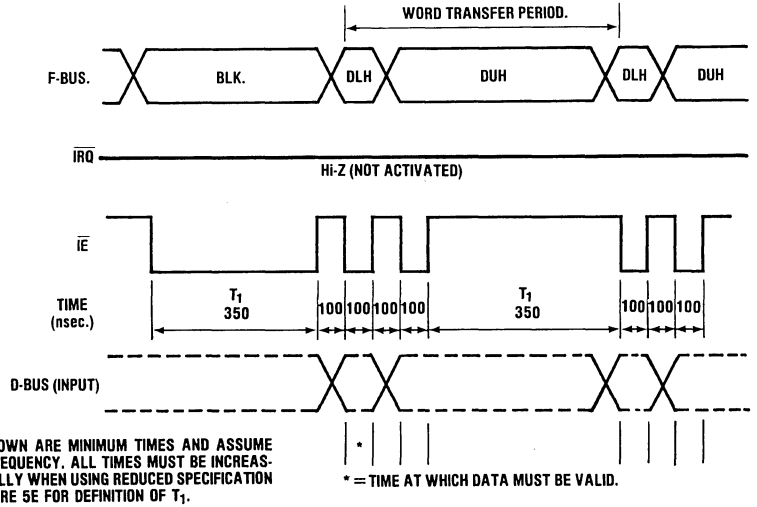


Figure 6B. Block Write Sequence/Timing



NOTE: TIMES SHOWN ARE MINIMUM TIMES AND ASSUME 20MHz CLOCK FREQUENCY. ALL TIMES MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS. SEE FIGURE 5E FOR DEFINITION OF T_1.

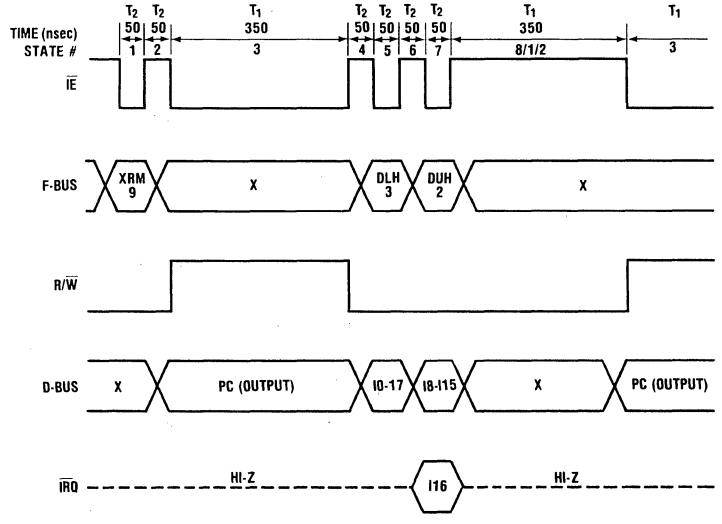
External Instruction Operation (XRM Mode)

The XRM mode is primarily intended for testing the SPP independently of the contents of the Instruction ROM. However, it can be used in program development and certain low speed applications using an external memory to store the program. Note that only the Instruction ROM is substituted in this mode, it is not possible to substitute the contents of the Data ROM (Displacements 4-7).

In this mode the SPP operates as a state machine. Selecting the XRM mode initializes the state machine to the idle state (State 1), as shown in Figure 7-A. When the $\overline{IE}$ line returns high the state machine advances to the ready state (State 2). In State 3 the program counter is output on the Data Bus (D_0-D_7), provided the R/$\overline{W}$ line is high at that time. The next rising edge of $\overline{IE}$ takes the state machine into State 4, and may be used to latch the PC into an external register. By using this to address the external instruction memory it is possible to make full use of the conditional branching instructions without any separate computation. The next cycle of the $\overline{IE}$ line takes the state machine through States 4 and 5 during which time the lower 8 bits of the next instruction to be executed (I0-I7) are read in on the Data Bus, and latched in on the rising edge of $\overline{IE}$ which takes the state machine into State 6. The next cycle takes the state machine through States 6 and 7 when the next 8 bits of the next instruction (I18-I15) are read in on the Data Bus, and the MSB (I16) is read in on the $\overline{IRQ}$ line. The $\overline{IRQ}$ line will always be floating at this time, even if it was previously set low. The next rising edge of the $\overline{IE}$ latches in these instruction bits and advances the state machine into State 8, the execute state. The next low state of the $\overline{IE}$ line advances the state machine into the idle state, State 1, once again, if this occurs within 250nsec of the start of state 8. If the $\overline{IE}$ line is allowed to remain high beyond the end of the execution cycle (as shown in Figure 7A) then states 1 and 2 will be skipped internally and the first falling edge of $\overline{IE}$ will take the state machine directly into state 3 as shown. It is important that the SPP be allowed to complete its execution cycle (300nsec) before the next rising edge of $\overline{IE}$, otherwise the cycle may be corrupted.

No restrictions on serial I/O exist in the XRM mode, but there are constraints on the handling of parallel I/O due to the use of the $\overline{IE}$ line, the F-bus and the D-bus for instruction loading. When the SPP is waiting for input data (caused by the execution of a JMIF operator) or has output data ready (caused by the exe-

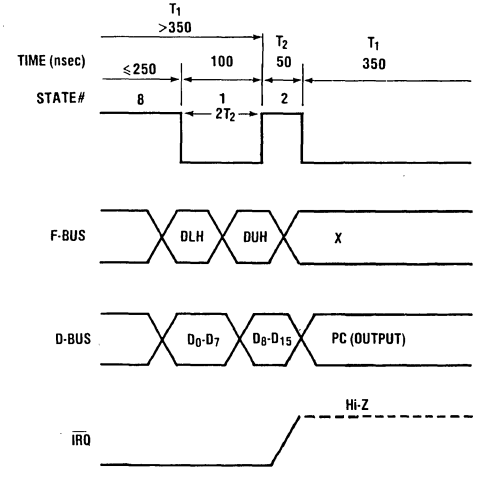
Figure 7A. Block Transfer Timing/Sequence



NOTES: X = DON'T CARE
CODE XRM NEED ONLY APPEAR ON THE F-BUS IN THE FIRST CYCLE
THE FIRST PC OUTPUT WILL NOT NECESSARILY BE VALID
TIMES SHOWN ARE MINIMUM TIMES AND ASSUME 20MHz CLOCK FREQUENCY. ALL TIMES MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS
USE CLR OR RST TO STOP XRM OPERATION. SEE FIGURE 5E FOR DEFINITION OF T_1 AND T_2

cution of a LACO operator) the $\overline{IRQ}$ line will go low during the T5 period (see Figure 2) of the execution cycle. Several methods of dealing with the data transfer exist, but the simplest is to cause the state machine to go into state 1 by taking the $\overline{IE}$ line low within 250nsec of the start of state 8 in the next cycle as shown in Figure 7B. If the F-bus is set to code DLH (hex 3) during the first part of this period the LSbyte of the data may be read, (in the case of an output) or written (in the case of an input). If the F-bus is then set to code DUH (hex 2) without taking $\overline{IE}$ high, the data will change to the MSbyte (in the case of an output), and in the case of an input the LSbyte will be latched in at the F-bus transition, allowing the MSbyte to be written and latched in at the rising edge of $\overline{IE}$ taking the state machine into State 2.

Figure 7B. Data Transfer During XRM Operation



NOTE: TIMES SHOWN ARE MINIMUM TIMES AND ASSUME 20MHz CLOCK FREQUENCY. THEY MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS. SEE FIGURE 5E FOR DEFINITIONS OF T_1 AND T_2

Circuit Description

Instruction ROM—The SPP program is stored in a 256x17 bit ROM. The 17-bit wide instruction word (See Figure 1) facilitates multiple operations per instruction. Addresses 250-255 are reserved for chip testing.

Data Memory—The 256x16 bit data memory is organized to provide two operands (U, V) in a single fetch cycle. The 256 data words are structured in a 32-'base' by 8-'displacement' word matrix. Memory is further partitioned such that each base group contains 4 words of RAM (displacements 0 through 3) and 4 words of ROM (displacements 4 through 7). Only the base information is fed to the RAM/ROM core. All eight displacement words associated with that base are accessed in parallel. Two independent displacement multiplexers select the two operands (U, V) from the eight output words. Within an 8-word base, therefore, the memory appears to have three ports.

Scratchpad Memory—An 8-word scratchpad memory (all RAM) is provided so that common data may be accessed with the full efficiency of data contained within an 8-word base. An additional multiplexer on the "V" memory port accesses the scratchpad data instead of data from the main memory core. Since this is independent of the base group, the scratchpad contents may be considered as a "floating" base group. This feature doubles the efficiency of equalizer tap update and similar programs.

VP Register—The VP register provides a one-instruction delay of data accessed from the memory "V" port. The memory read cycle precedes the write cycle (see Figure 2). The VP register consists of two portions. Data from the n-th read cycle first enters the master portion. During the next cycle, data from instruction n+1 enters the master portion while the instruction n data shifts to the slave portion. The data in the slave portion may be returned to the memory during the instruction n+1 write cycle by use of the commands TVPV or TVIB. Thus digital filter z^{-1} delays are implemented with minimal software overhead.

RAR—A return address register allows one level of subroutine nesting. This facilitates repeated use of universal subroutines such as a second order digital filter routine, SIN/COS routine, etc., thus minimizing the program size.

Loop Counter—A loop counter is provided to handle iteration loops up to 32 iterations. Special jump instructions conditional on this loop counter to be zero, provide the iteration test without adding program steps. The loop counter can be loaded from the Input Register as well as the Accumulator.

Base Register—The base register is 5 bits wide and is used to set up the base in memory in the offset addressing (UV/US) modes. Its function may be taken over by the Index Register by means of the SWAP and TAUI instructions, and also during Block Transfer.

Table 4. OP1, OP2 Code Cross-Compatibility Table

Notes: X indicates the OP1, OP2 combination cannot be used
1. index register provides "base" information
2. CLAC overrides OP2 instruction
3. OP1 bits provide function code—see Table 1
4. address is not used with MODE and is available for setting up multiplier and VP register

	OP1→ / OP2↓	Accumulator Operations					Addition Operations				Subtraction Operations			Multiply/Add Operations			Multiply/Sub. Operations			
		NOP	ABS	NEG	SHR	SGV	AUZ	AVZ	AVA	AUV	S V A	SVU	APZ	APA	APU	SPA	SPU	MULTIPLIER SETUP	
No Operation Instruction	NOOP																		
Load Instructions	LLTI	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
	LIBL																		
	LACO																		
	LAXV																		
	LALV																		
	LABV																		
Data Transfer Instructions	TACU																		
	TACV																		
	TIRV																		
	TVPV																		
	TVIB																		
	TAUI						1	1	1	1	1	1			1		1	1	
Accumulator Instructions	CLAC	See note 2																	
Register Manipulation Instructions	INIX																		
	DECB																		
	INCB																		
	SWAP																		
Unconditional Branch Instructions	JMUD					X	X	X	X	X	X	X			X		X	X	
	JMUI					1	1	1	1	1	1	1			1		1	1	
Conditional Branch Instructions	JMCD					X	X	X	X	X	X	X			X		X	X	
	JMPZ					X	X	X	X	X	X	X			X		X	X	
	JMPN					X	X	X	X	X	X	X			X		X	X	
	JMPO					X	X	X	X	X	X	X			X		X	X	
	JMIF					X	X	X	X	X	X	X			X		X	X	
	JMOF					X	X	X	X	X	X	X			X		X	X	
Subroutine Instructions	JMSR					X	X	X	X	X	X	X			X		X	X	
	RETN																		
Complex Instructions	JCDT					X	X	X	X	X	X	X			X		X	X	
	JCDI					X	X	X	X	X	X	X			X		X	X	
	MODE	See note 3																4	
	REPT																		

Index Register—The index register is 5 bits wide and is used to access lookup tables. This register can be incremented by a software command. Lookup table instructions cause the index contents to be used as the data memory base. Table contents may be used either as data or as jump addresses for computed GO-TO operations. Special instructions allow the base and the index register to work together, providing a dual base addressing scheme. The index is also used to step through the data memory during block transfer operations. In this mode two additional MSBs are added to this register.

ASU—The heart of the SPP is a 16-bit adder/subtractor unit (ASU). The ASU operates with two's complement arithmetic, and is provided with zero, negative and overflow detect circuits. The basic adder cell includes look-ahead carry logic to improve speed. The ASU will deliver a 16-bit sum in 40 nanoseconds. An accumulator latch follows the ASU. A shifter is available to shift the accumulator contents 1 bit to the right, providing a precision divide-by-two.

Multiplier—The SPP incorporates a parallel modified Booth's algorithm multiplier. The multiplier inputs are truncated to 12 bits and the multiplier output is rounded to 16 bits. These truncations produce a product with a resolution of 15 bits. The 16 MSBs of the product are retained. This implies that all numbers in the SPP are represented as fractions less than one in magnitude. The imaginary binary point is to the left of the MSB (B14). This fractional representation and the fixed-point arithmetic requires proper scaling of equations to realize the full accuracy of the SPP. A benefit of fractional representation of numbers is that the multiplier cannot overflow. The propagation delay through the multiplier is 300 nanoseconds. A 300-nanosecond SPP instruction cycle is achieved by pipelining the multiplier. Data entered into the multiplier during instruction n will result in a product available during instruction n+1 (see Figure 2). The one instruction delay removes the multiplier propagation delay from the overall instruction cycle.

Multiplication is automatically set up by the address mode (see Figure 1). The multiplier is always active. Products are utilized by specifying one of the multiplier OP1 operators (APZ, APA, APU, SPA, SPU). The multiplier latches are updated wherever the instruction operand is a D or UV/S address. They are not updated if the operand is a Literal or DT, and the product of the previous set-up is retained until one of the multiplier OP1 operators is used to read it out.

Programming Examples

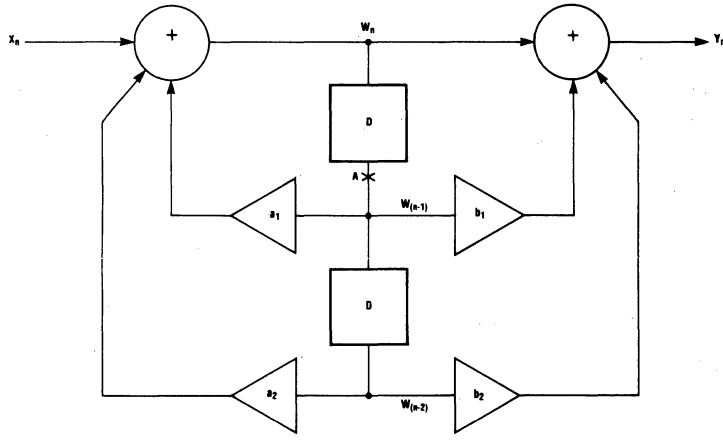
In this section two programming examples are provided to illustrate the use of some of the instructions and the power of the instruction set. The first example is that of a second order digital filter section. This can be implemented as a subroutine in the SPP such that the main program can access it repeatedly to implement higher order filter sections. The second example is that of a SINCOS subroutine that computes the values of sin ω and cos ω using an approximation formula. This routine was chosen as it illustrates the use of some of the complex instructions and because it is useful in applications that require carrier generation.

1. A second Order IIR Digital Filter Section; Figure 8 shows a block diagram, filter equations and the computational process involved in the implementation of this filter. It is clear that storage must be provided for the fixed coefficients a_1, a_2, b_1 and b_2 and previous two intermediate results W_{n-1} and W_{n-2}. Figure 10 illustrates the memory configuration at the beginning of the subrouine. Fixed coefficients are conveniently stored in the ROM portion of the data memory in displacements 4 through 7 while displacements 0 and 1 are used for storage of past values. It is assumed that the present input sample X_n is loaded in the accumulator by the main program prior to accessing the subroutine. At the end of the subroutine output Yn is left in the accummulator while W_{n-1}, and W_{n-2} are replaced by W_n and W_{n-1} so that the next input sample X_{n+1} can be processed. Note that only one base value is used by the filter for the storage and main program must load this value in the base register prior to execution.

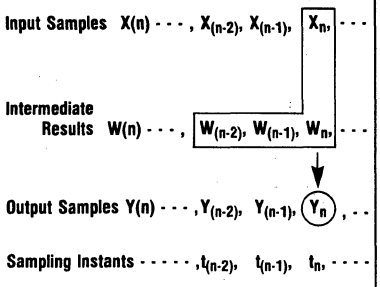
Figure 9 illustrates the instruction sequence of the subroutine. Only five instructions are needed to completely process the section. This corresponds to a processing time of 1.5 microseconds. Figure 10 illustrates how the memory map gets modified during the execution. A higher order filter is implemented by cascading of the second order sections. The main program can increment the base register and decrement the loop counter after each iteration until the required number of iterations of this subroutine take place. Since the accumulator holds the output of the filter after each iteration, no storage is required in memory. Figure 11 illustrates the program and memory allotment for implementation of a sixth order filter.

Figure 8. Digital Filter Example

A. Second Order Recursive IIR Digital Filter Section



B. Computation Process



C. Digital Filter Equations

$$W_n = X_n + a_1 W_{(n-1)} + a_2 W_{(n-2)}$$

$$Y_n = W_n + b_1 W_{(n-1)} + b_2 W_{(n-2)}$$

Figure 9. Digital Filter Subroutine

LINE#	LABEL	OP1	OP2	OPERAND		COMMENTS
0	DF	NOP	NOOP	UV 4,0	;	a_1, $W_{n-1} \rightarrow$MULT. ACC$=X_n$
1		APA	NOOP	UV 5,1	;	a_2, $W_{n-2} \rightarrow$MULT. $X_n + a_1 \rightarrow$ACC
2		APA	TACV	UV 6,0	;	b_1, $W_{n-1} \rightarrow$MULT. $W_n = X_n + a_1$, $W_{n-1} + a_2 W_{n-2} \rightarrow$ACC ACC$\rightarrow$V 0 replace W_{n-1} $W_{n-1} \rightarrow$VP
3		APA	TVPV	UV 7,1	;	b_2, $W_{n-2} \rightarrow$MULT. $W_n + b\ W_{n-1} \rightarrow$ACC $W_{n-1} \rightarrow$V 1 replaces W_{n-2}
4		APA	RETN	—	;	$Y_n = W_n + b_1\ W_n + b_2\ W_{n-2} \rightarrow$ACC Return to main program

Figure 10. Memory Maps for the Digital Filter

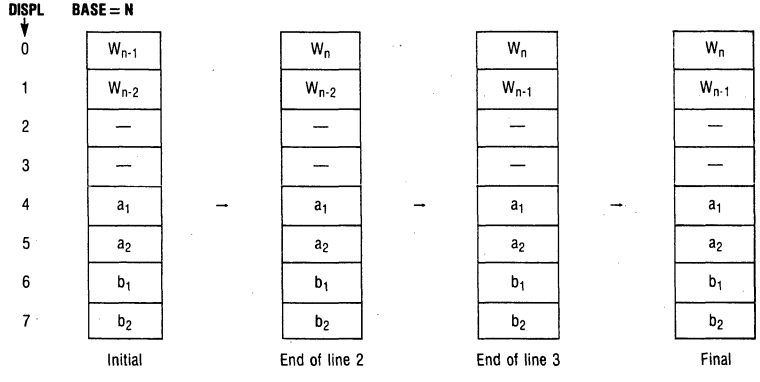


Figure 11A. Main Program Instructions for a Sixth Order Filter

LABEL	OP1	OP2	OPERAND	COMMENTS
		•		
		•		
		•		
	NOP	LLTI	L002	; (IR) = 002
	NOP	LIBL	—	; 0→BAS, 2→LC
				Initialize base register and loop counter
L1	—	JMSR	DF	; Jump to DF subroutine
	—	JCDI	L1	; Increment base, Test if LC = 0
		•		If non zero go to L1
		•		Decrement LC after test
		•		Output of the filter is in accumulator at the end of iterations.

Figure 11B. Memory Map for the Sixth Order Filter

Base → / DISPL ↓	0	1	2	—
0	$W_{0(n-1)}$	$W_{1(n-1)}$	$W_{2(n-1)}$	
1	$W_{0(n-2)}$	$W_{1(n-2)}$	$W_{2(n-2)}$	
2	—			
3	—			
4	a_{01}	a_{11}	a_{21}	
5	a_{02}	a_{12}	a_{22}	
6	b_{01}	b_{11}	b_{21}	
7	b_{02}	b_{12}	b_{22}	

Implementation of Second Order Digital Filter with Coefficients >1 in the S2811

In order to be able to implement a digital filter with coefficients in the range of −2 to +2 it is necessary to scale the coefficients by a factor of 2 to bring them into the permissible range of −1 and +1. However, in order to restore the "loop gain" of the recursive section of the filter it is necessary to correct for this in the signal flow network. The easiest way to do this is to double the signal level at the point A in Figure 8. The modified second order filter subroutine is shown below, together with the basic subroutine. Note that in the modified subroutine all the coefficients must be halved.

Basic Subroutine (|coefficients|<1)

```
0 NOP   NOOP  UV4,0 ; a1, Wn-1→MULT.
                     ACC=Xn
1 APA   NOOP  UV5,1 ; a2, Wn-2→ACC
2 APA   TACV  UV6,0 ; b1, Wn-1→MULT.
                     Wn=Xn+a1 Wn-1+a2
                     Wn-2→ACC
                     ACC→V0 (replace Wn-1)
                     Wn-1→(VP)
3 APA   TVPV  UV7,1 ; b2, Wn-2→MULT.
                     Wn+b1 Wn-1→ACC
                     Wn-1→V(1) (replaces Wn-2)
4 APA   RETN        ; Yn=Wn+b1 Wn-1+b2
                     Wn-2→ACC
                     Return to main program
```

Modified Subroutine (|coefficients|<2)

```
0 NOP   NOOP  UV4,0 ;
1 APA   NOOP  UV5,1 ; as above
2 APA   TACV  UV6,0 ;
3 APA   TVPV  UV7,1 ;
4 APA   TACV  US−0  ; Yn=Wn+b1 Wn-1+b2
                     Wn-2→ACC→S0
5 AUV   TACV  UV0,0 ; U0+V0→ACC→V0=2Wn-1
6 AVZ   RETN  US−0  ; S0→ACC=Yn
```

2. **SINCOS:** SINCOS is a subroutine that provides the sinω values for values of ω satisfying the condition $-\pi \leq \omega < \pi$. Since all numbers in the SPP are represented as fractions less than 1 it is first necessary to scale by a factor π such that $-1 \leq \frac{\omega}{\pi} < 1$. The value $\omega' = \frac{\omega}{\pi}$ is assumed to be in the accumulator at the beginning of the subroutine. In a practical application the control processor can enter ω′ into the SPP before the computation begins

If the control processor does not have scaled values of ω available, an alternative method can be used. In this method the control processor can enter $\frac{\omega}{4}$ into the SPP. $\frac{\omega}{4}$ can be easily obtained by a 2-bit right shift operation. The SPP can then convert $\frac{\omega}{4}$ to $\frac{\omega}{\pi}$ by first multiplying $\frac{\omega}{4}$ by $\frac{2}{\pi}$ and then adding the result to itself. In any event it is assumed that $\omega' = \frac{\omega}{\pi}$ is available in the accumulator when the subroutine is accessed. When the control is returned to the main program $\sin\omega$ is available in S(0) and $\cos\omega$ is available in S(1) while ω' remains in the accumulator as well as S(2). The subroutine computes the $\sin\omega$ and $\cos\omega$ values by use of the following approximation:

For small values of $\Delta\omega$.

$\sin\Delta\omega \cong \Delta\omega$

$\cos\Delta\omega \cong 1$

$$\sin\omega = \sin(\hat{\omega}+\Delta\omega) = \sin\hat{\omega}\cos\Delta\omega + \cos\hat{\omega}\sin\Delta\omega \cong \sin\omega + \Delta\omega\cos\omega$$

$$\cos\omega = \cos(\hat{\omega}+\Delta\omega) = \cos\hat{\omega}\cos\Delta\omega - \sin\hat{\omega}\sin\Delta\omega \cong \cos\hat{\omega} - \Delta\omega\sin\hat{\omega}$$

ω represents the nearest quantized value to ω. In the subroutine the quantized value is obtained by truncating $2|\omega'| = (\frac{2}{\pi}|\omega|)$. The truncation results in five most significant bits including the sign bit. Since absolute value is truncated, sign bit is zero. The four most significant magnitude bits provide sixteen quantized angles $2|\hat{\omega}'| = \omega_q$. ω_q is loaded in the index register. Use of SWAP command allows the index register to access the appropriate block of data memory corresponding to ω_q. $\sin\hat{\omega}$ and $\cos\hat{\omega}$ values corresponding to ω_q are stored in displacements 4 and 5 (ROM portion) of the appropriate block addressed by ω_q. Figure 13A illustrates the organization of the lookup table.

Figure 12 shows a detailed sequence of instructions for the SINCOS routine. The routine is nineteen instructions long and takes 5.7 microseconds to execute. As seen from Figure 12, the first objective of the program is to transform the input angle to the first quadrant. This transformation process is graphically illustrated in Figure 13B. The input angle ω' is stored in S(0) and a number $[\frac{1}{2} - |\omega'|]$ is stored in S(1). The signs of these numbers are used to assign the sign to the magnitudes of $\sin\omega$ and $\cos\omega$ computed by the approximation formulae. Table 13C illustrates how the sign of $\sin\omega$ can be taken from the sign of the angle ω' and sign of $\cos\omega$ can be taken from the sign of the number $[\frac{1}{2} - |\omega'|]$. The signs are assigned by use of the SGV instruction at the end of the subroutine. The quantized angle ω_q is computed by the truncation of the number $2|\omega'|$. The truncated value (five most significant bits including sign bit) are loaded in the index register by the LAXV instruction and allows direct access of the $\sin\hat{\omega}$ and $\cos\hat{\omega}$ values from the appropriate block. $\Delta\omega$ is computed simply as a difference between the input and the quantized angle. The $\sin\omega$ and $\cos\omega$ values are stored in S(0) and S(1) respectively while the angle ω' is retained in the accumulator as well as S(2) when the program exits.

The SINCOS subroutine illustrates the following operations:

- —Scaling
- —Table Lookup
- —Use of SWAP command
- —Use of SCRATCHPAD
- —All Data Addressing Modes
- —Use of SGV command
- —Use of TVPV command
- —Truncation of the accumulator using LAXV command.

Figure 12. SINCOS Subroutine

SINCOS Routine

LINE#	LABEL	OP1	OP2	OPERAND		COMMENTS
0	SC	NOP	TACV	US−,0	;	$\omega' = \frac{\omega}{\pi} \rightarrow$ S0, ACC
1		ABS	SWAP	- -	;	$\lvert\omega'\rvert \rightarrow$ACC, SWAP roles of base and index
2		SVA	NOOP	D00.6	;	½-$\lvert\omega'\rvert \rightarrow$ACC
3		NOP	TACV	US-,1	;	½-$\lvert\omega'\rvert \rightarrow$ACC
4		AVA	NOOP	US-,1	;	S(1) + ACC $\rightarrow$ACC = (1-2$\lvert\omega'\rvert$)
5		ABS	NOOP	- -	;	$\lvert$1-2$\lvert\omega'\rvert\rvert \rightarrow$ACC
6		SVA	NOOP	D01.6	;	2$\lvert\omega'\rvert \rightarrow$ACC
7		NOP	LAXV	US-,2	;	2$\lvert\omega'\rvert \rightarrow$S(2). $\hat{\omega}' \rightarrow$ACC, IX. $\hat{\omega}'$ = quantized value corresponding to ω
8		SVA	TACV	US-,2	;	2$\lvert\omega'\rvert - \hat{\omega}' = 2\Delta\omega' \rightarrow$ACC, S(2)
9		AVA	NOOP	US-,2	;	S(2) + ACC = $\rightarrow$ACC($4\Delta\omega'$)
10		NOP	NOOP	D02.6	;	$\frac{\pi}{4}$, $4\Delta\omega' \rightarrow$MULT.
11		APZ	TACV	US-,2	;	$\pi\Delta\omega' \rightarrow$ACC, S(2) ($\pi\Delta\omega' = \Delta\omega$)
12		NOP	NOOP	US(4,2)	;	sin$\hat{\omega}$, $\Delta\omega \rightarrow$MULT. Index register contents $\hat{\omega}'$ point to sin$\hat{\omega}$ in displacement 4 of the appropriate block.
13		SPU	TACV	US(5,2)	;	$\Delta\omega\sin\hat{\omega} - \cos\hat{\omega} = \cos\omega \rightarrow$ACC, S(2). $\Delta\omega$, cos$\hat{\omega} \rightarrow$MULT.
14		APU	SWAP	US(4,2)	;	sin$\hat{\omega} + \Delta\omega\cos\hat{\omega} = \sin\omega \rightarrow$ACC. Transfer control back to base register
15		SGV	TACV	US-,0	;	Assign the sign of ω' to (sinω) and store result in S(0). sin$\omega \rightarrow$S(0), $\omega' \rightarrow$(VP)
16		AVZ	TVPV	US-,2	;	$-\cos\omega \rightarrow$ACC. (VP) = ωS(2). Refer to the description of the VP register for explanation of TVPV instruction.
17		SGV	TACV	US-,1	;	Assign the sign of [½-$\lvert\omega'\rvert$] to cosω and store result in S(1). cos$\omega \rightarrow$S(1)
18		AVZ	RETN	US-,2	;	$\omega' = \frac{\omega}{\pi} \rightarrow$ACC. Return to main program.

Figure 13A. Organization of the Lookup Table for SINCOS Routine

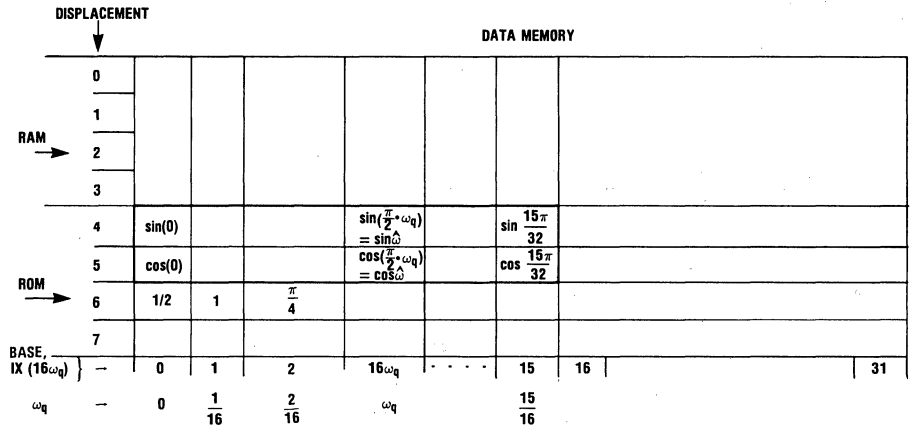


Figure 13B. Graphical Angle Transformation Process

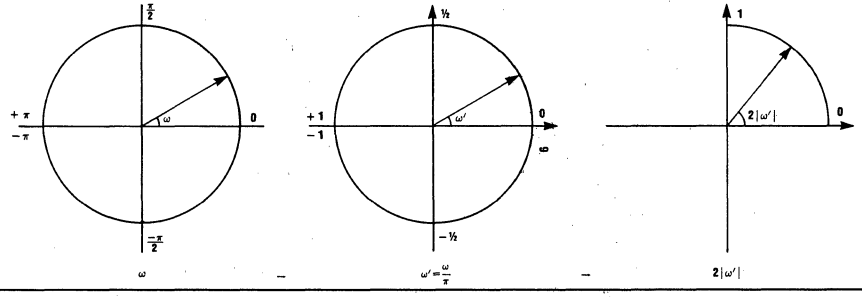


Figure 13C. Table for Computing Sign of sinω, cosω

	QUADRANTS			
	1	2	3	4
Range of ω	$0 \rightarrow \pi/2$	$\pi/2 \rightarrow \pi$	$-\pi \rightarrow -\pi/2$	$-\pi/2 \rightarrow 0$
Range of ω′	$0 \rightarrow 1/2$	$1/2 \rightarrow 1$	$-1 \rightarrow -1/2$	$-1/2 \rightarrow 0$
Range of $[1/2 - \lvert\omega'\rvert]$	$1/2 \rightarrow 0$	$0 \rightarrow -1/2$	$-1/2 \rightarrow 0$	$0 \rightarrow 1/2$
Sign of ω′	+	+	−	−
Sign of sinω	+	+	−	−
Sign of $[1/2 - \lvert\omega'\rvert]$	+	−	−	+
Sign of cos ω	+	−	−	+

AMERICAN MICROSYSTEMS, INC.

S2814A

FAST FOURIER TRANSFORMER

Features

- Based on AMI's Signal Processing Peripheral Chip (S2811)
- Performs 32 Complex Point Forward or Inverse FFT in 1.3msec, Using Decimation in Frequency (DIF)
- Transform Expandable either by Using Multiple S2814As (for Minimum Processing Time) or by a Single S2814A (for Minimum Hardware)
- Operates with any 8 or 16 Bit Microprocessor, including S6800 and S9900. Optional DMA Controller Increases Speed
- All Data I/O Carried Out on Microprocessor Data Bus
- Basic Resolution of 57dB. Optional Conditional Array Scaling (CAS) Routine Increases Dynamic Range to 70dB
- Optional Windowing Routine Incorporated to Permit Use of Arbitrary Weighting Function
- Coefficient Generation On Chip, with Rotation Algorithm for Transform Expansion up to 512 Points
- Optional Power Spectrum Computation

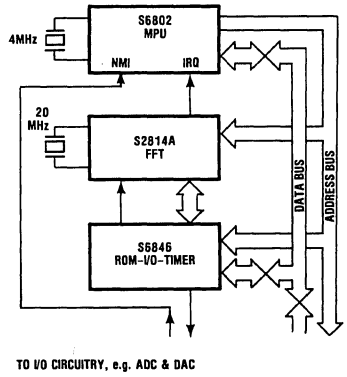
General Description

The AMI S2814A Fast Fourier Transformer is a pre-programmed version of the S2811 Signal Processing Peripheral. For further information on the internal operation of the S2811, please refer to the S2811 Advanced Product Description. It calculates FFTs and IFFTs using a decimation in frequency (DIF) technique for minimum distortion. The S2814A calculates a 32 complex point FFT using internally generated coefficients in a single pass. A coefficient rotation algorithm allows larger FFTs to be implemented (in blocks of 32 points). This implementation may be carried out by successive passes of the data through the two main routines in the S2814A, allowing larger transforms to be carried out with a single S2814A. Alternatively, an array of S2814As may be used to increase the transformation speed by parallel processing.

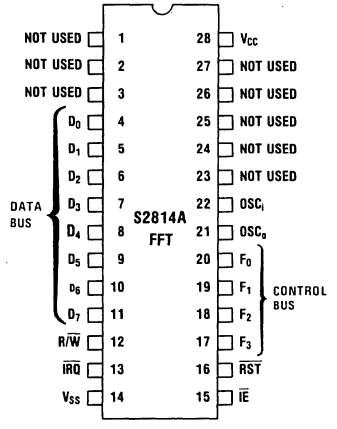
The word length used in the S2814A gives the transformed data a resolution of up to 57dB, but the total dynamic range can be increased up to 70dB by using the Conditional Array Scaling (CAS) routine incorporated.

The S2814A is intended to be used in a microprocessor system (see Block Diagram), using an 8 or 16 bit microprocessor, ROM, RAM and an optional DMA Controller or Address Generator. The S2814A is used as a

Block Diagram: Minimum System Configuration



Pin Configuration



memory mapped peripheral, and should be assigned a block of 16 addresses. It is used as a "hardware subroutine" function. The microprocessor controls the flow of data, including I/O, and calls the routines in the S2814A to cause the FFT to be executed. The S2814A responds to the microprocessor with the $\overline{IRQ}$ line when the processing of each routine is completed. In the case of a 32 point transform this signifies the completion of the transform, and in larger transforms it signifies that the microprocessor should unload the output data, load the next input data and call the next routine to be executed. The data is stored externally in RAM. Input data to be transformed is loaded into displacements 0 and 1 of the S2814A data memory. At the end of the FFT routine output data overwrites the input data. If power spectrum flag (PSF) is set, the S2814A computes the sum of the squares of the real and imaginary components of the output data and places the result in displacement 3 of the data memory. Both complex FFT data and power spectrum data are thus available. Windowing weights may be loaded into the S2814A prior to processing if the windowing routine is to be used. A 6800 compatible source listing of a suitable control program is available to the S2814A user at no charge. This control program will also be made available as a mask programmed ROM.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10sec.)	200°C

Electrical Specifications (V_{CC} = 5.0V ± 5%; V_{SS} = 0V, T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.0		V_{CC}+0.3	V	V_{CC} = 5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC} = 5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μA	V_{IN} = 0V to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD} = −100μA, V_{CC} = min, C_L = 30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD} = 1.6mA, V_{CC} = min, C_L = 30pF
f_{CLK} (max)	Maximum Clock Frequency				MHz	V_{CC} = 5.0V
	S2814A-10	10				
	S2814A-12	12				
	S2814A-15	15				
	S2814A	20				
P_D	Power Dissipation		1.2		W	V_{CC} = 5.0V

S2814A Pin Functions/Descriptions

Pin	Number	Function
D_0-D_7	4-11	(Input/Output) Bi-directional 8-bit data bus. Data is Two's Complement coded.
F_0-F_3	20-17	(Input) Control Function bus. Four Microprocessor address lines (typically A_0-A_3) are used to control the S2814A.
$\overline{IE}$	15	(Input) Interface Enable. A low level on this line enables data transfer on the data bus and control functions on the F-bus. Usually generated by microprocessor address decode logic.
R/$\overline{W}$	12	(Input) Read/write select. When HIGH, output data from the S2814A may be read, and when LOW data may be written into the S2814.
$\overline{IRQ}$	13	(Output) Interrupt Request. This open drain output goes low when the S2814A has completed the execution of a routine and output data is available.
$\overline{RST}$	16	(Input) When LOW all registers and counters will be cleared, including the program counter, and all control functions cleared.
OSC_i, OSC_0	22,21	Oscillator input and output. For normal operation a crystal is connected bet- ween these pins to generate the internal clock signals. Alternatively, an external square wave signal may be connected to OSC_0 pin with OSC_i pin left open. All timings shown in this Product Description assume a 20MHz clock frequency.
V_{CC}	28	Positive power supply connection.
V_{SS}	14	Negative power supply connection. Normally connected to ground.

In addition to the above, pins 23-27 and 1 are connected internally. They should all be tied to V_{SS} during normal operation. Do not make connections to pins 2 and 3.

Functional Description

The S2814A is a pre-programmed version of AMI's S2811 Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters. For more detailed information about the chip, please refer to the S2811 Advanced Product Description.

The S2814A Instruction ROM contains the various routines which make up the FFT package. The routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the coefficients required to execute the functions. 128 words of Data RAM are provided to hold the 32 point complex signal data during processing as well as the power spectrum of the output and various other parameters, including the total number of points in the desired transform. The memory is organized as a 32x4 matrix, with the data arranged in columns, as shown in Table 1B.

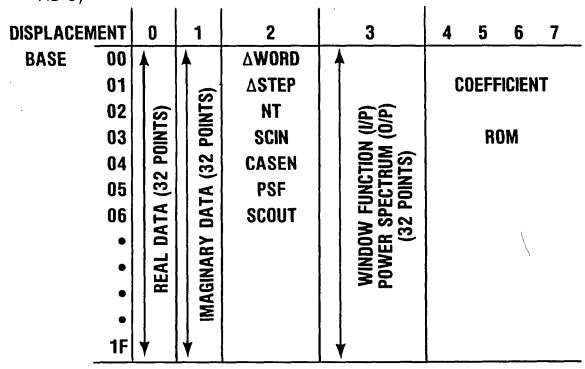
Table 1: Software Model of S2814A

A. Routine Locations in Instruction Memory

LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY PT. "INIT" ROUTINE
04	ENTRY PT. "FFT32" ROUTINE
D3	ENTRY PT. "COMPAS" ROUTINE
EA	ENTRY PT. "SCALE" ROUTINE
DC	ENTRY PT. "WINDOW" ROUTINE
E4	ENTRY PT. "CONJUG" ROUTINE

B. Data Memory Map

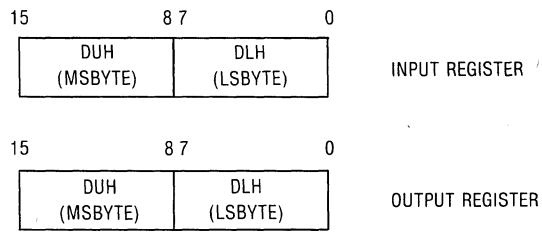
(Note: Address [Base AB, Displacement C] is written as AB·C)



C. Control Functions

F-BUS (HEX)	MNEMONIC	FUNCTION
1	RST	RESETS CHIP
2	DUH	SELECTS MSBYTE
3	DLH	SELECTS LSBYTE
4	XEQ	STARTS EXECUTION
9	BLK	SELECTS BLOCK MODE

D. Input and Output Registers



CODE IS TWO'S COMPLEMENT.

Initial Set-Up Procedure

After power up, the $\overline{RST}$ line should be held low for a minimum of 1 instruction cycle. If this line is connected to the reset line of the microprocessor this condition will be met easily. This will clear the Base and Index Registers, which are used for memory addressing, the Loop Counter and the Program Counter. Address zero in the Instruction ROM contains a Jump to Zero instruction, and thus the S2814A will remain in an idle state after being reset. Every routine in the memory is also terminated with a Jump to Zero instruction, and thus the S2814A will also remain in this same idle state after the the execution of each routine. The $\overline{IRQ}$ line will signal this condition each time, except after the initial reset and after execution of the INIT routine.

The Control Functions

The S2814A is controlled by the host microprocessor by means of the F-bus, Interface Enable ($\overline{IE}$) and the Read-Write (R/$\overline{W}$) lines. It should be connected to the host processor as a memory mapped peripheral as shown in Figure 1.

The 12 most significant address lines decode a group of 16 addresses to activate the $\overline{IE}$ line each time an address in the group is called, and the S2814A is controlled by reading to or writing from those addresses. Only 5 of these addresses are used as described in Table 2. Throughout this Product Description these addresses will be referred to as HHHX (X=0-F).

Figure 1. Connection of S2814A as a Memory Mapped Peripheral

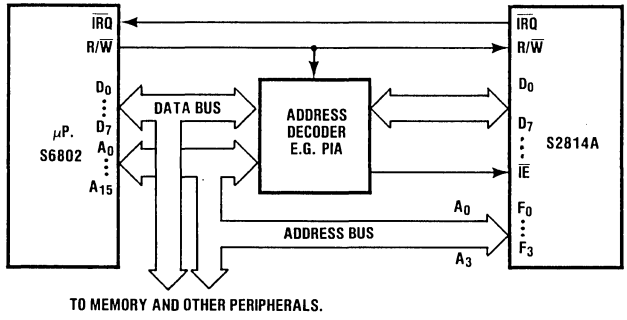


Table 2: S2814A Control Functions

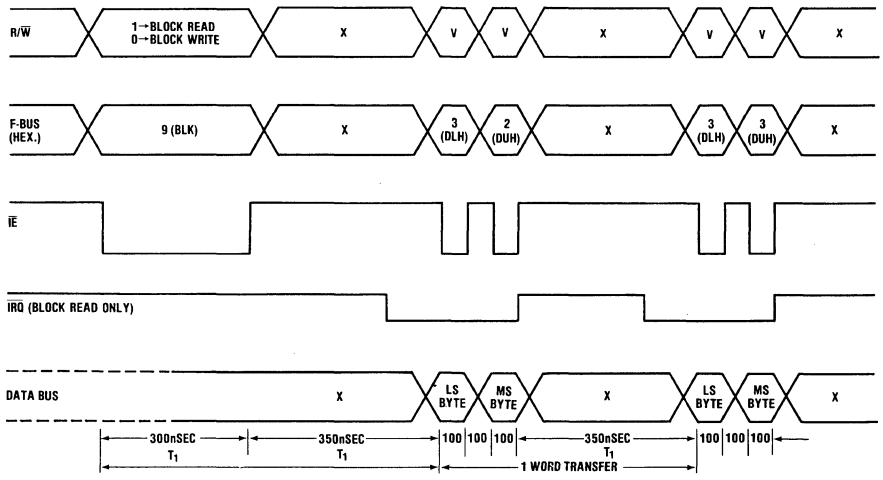
MNEMONIC	F-BUS HEX	DATA	TYPE OF OPERATION	FUNCTION
RST	1	XX	READ/ WRITE	CLEARS ALL REGISTERS. STARTS PROGRAM EXECUTION AT LOCATION 00. THIS IS THE IDLE STATE. THIS INSTRUCTION SHOULD PRECEDE BLOCK READ, BLOCK WRITE AND EXECUTE COMMANDS.
DUH	2	HH	READ/ WRITE	READS FROM OR WRITES INTO S2814A THE UPPER HALF OF THE DATA WORD. (SEE TABLE 1.D.)
DLH	3	HH	READ/ WRITE	READS FROM OR WRITES INTO S2814A THE LOWER HALF OF THE DATA WORD. (SEE TABLE 1.D)
XEQ	4	HH	WRITE	STARTS EXECUTION AT LOCATION HH
BLK	9	XX	READ/ WRITE	INITIATES A BLOCK READ OR BLOCK WRITE OPERATION. THE ENTIRE DATA RAM CAN BE ACCESSED SEQUENTIALLY BEGINNING WITH VALUES OF BASE AND DISPLACEMENT INITIALIZED USING "BLOCK TRANSFER SET UP" ROUTINE. IF A RESET OPERATION IS PERFORMED PRIOR TO BLOCK COMMAND THE DATA MEMORY ADDRESS IS INITIALIZED TO BASE 0, DISPLACEMENT 0. BLOCK READ OR WRITE OPERATION CAN BE TERMINATED ANY TIME BY PERFORMING A RESET OPERATION. THE INDEX REGISTER IS USED TO ADDRESS THE MEMORY DURING BLOCK TRANSFER AND INTERNAL ADDRESSING IS SEQUENCED AUTOMATICALLY.

NOTE: XX = Don't care
HH = 2 Hex characters (8-bit data)

The Block Transfer Operation

Block transfer is the mode used to load and unload the main data blocks into the S2814A at up to 4Mbytes/sec. In this mode the data memory is addressed by the Index Register, and after initialization the internal addressing is sequential and automatic. The sequence generated is that after each word transfer (16-bit words as 2 bytes, or 8-bit words as MSbyte (DUH) only) the base is incremented. After base 1F (31) has been reached, the base resets to 00 and the displacement increments. After base 1F displacement 3 has been reached (i.e., the highest address in the RAM, 1F.3), both base and displacement reset to zero. Note that when the BLK command is given the Read/Write line is latched internally, and remains latched until the RST command is given. The block transfer sequence and timing are shown in Figure 2. When using a microprocessor to execute the block read it will normally be advantageous to set the interrupt mask.

Figure 2. Block Transfer Sequence and Timing



NOTE 1: X = DON'T CARE, OR NOT VALID V = VALID

NOTE 2: ALL TIMES SHOWN ARE MINIMUM AND MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS AS FOLLOWS:

$$T_{1\ MIN} = \left[\frac{6000}{f_{CLK}} + 50\right] \text{ nsec}$$

In 6800 Assembly Language a Block Write would be executed with the following code:

```
LDX     OFFST   ;LOAD MEMORY START ADDRESS INTO INDEX REG.
STA  A  BLK     ;WRITE DUMMY DATA TO ADDRESS $HHH9,BLOCK MODE.
LDA  A  0,X     ;READ FIRST BYTE FROM MEMORY.
STA  A  DLH     ;WRITE INTO S2814A AS LSBYTE. ADDRESS $HHH3
LDA  A  1,X     ;READ SECOND BYTE FROM MEMORY.
STA  A  DUH     ;WRITE INTO S2814A AS MSBYTE.ADDRESS $HHH2
LDA  A  2,X     ;SECOND WORD.
  .       .       .
  .       .       .
  .       .       .
LDA  A  62,X    ;32ND. WORD.LSBYTE.
STA  A  DLH     ;
LDA  A  63,X    ;32ND. WORD,MSBYTE.
STA  A  DUH     ;END OF TRANSFER.
STA  A  RST     ;WRITE DUMMY DATA TO ADDRESS $HHH1.RESET.
```

Block Read would be executed by substituting LDA A for STA A, and vice versa.

where:

```
RST   EQU $HHH1
DLH   EQU $HHH3
DUH   EQU $HHH2
BLK   EQU $HHH9
```

The above code assumes that the block transfer is controlled by the host processor, not using DMA. Note that DLH must always precede DUH. 8-bit data may be transferred using DUH only, assuming that the significance of the data is correct.

The FFT Routines

Six individual routines are stored in the S2814A Instruction memory. Two or more of these are used in the computation of an FFT, depending on the transform size and the options selected. The starting addresses of the routines are shown in Table 3. All execution times quoted assume a 20MHz clock frequency.

Table 3. FFT Routines and Their Starting Addresses

LOCATION (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT FOR "INIT" ROUTINE
	(IR) = BASE, DISPLACEMENT
	$(BASE)_{4\text{-}0} \leftarrow (IR)_{15\text{-}11}, (DISP)_{1,0} \leftarrow (IR)_{9,8}$
	Returns to Idle state Exec. Time = 0.9μs
04	ENTRY POINT FOR "FFT32" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = SCIN, CASEN, PSF
	Perform 32 point FFT. Sets IRQ, Returns to Idle state. Exec. Time = 1.2 ms to 1.8ms.
	(OR) = SCOUT (DISP0) = Transformed Data (Real), (DISP1) = Transformed Data (Imag.) (DISP2) = SCOUT, (DISP3) = Power Spectrum Data if PSF = 1
D3	ENTRY POINT FOR "COMPAS" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP2) = WORD, STEP, NT, SCIN, CASEN
	Perform COMPAS, Sets IRQ, Returns to Idle State Exec. Time = 233 to 374μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.) (DISP2) = SCOUT, (OR) = SCOUT
EA	ENTRY POINT FOR "SCALE" ROUTINE
	(IR) = SCLP, (DISP0) = Data (Real), (DISP1) = Data(Imag.)
	Performs scaling, Sets IRQ. Returns to Idle State Exec. Time = 51 to 250μsec.
	(DISP0) = Scaled Data (Real), (DISP1) = Scaled Data (Imag.)
DC	ENTRY POINT FOR "WINDOW" ROUTINE
	(DISP0) = Input Data (Real), (DISP1) = Input Data (Imag.) (DISP3) = Multiplying factors
	Performs multiplication, Sets IRQ, Returns to Idle State Exec. Time = 49μsec.
	(DISP0) = Output Data (Real), (DISP1) = Output Data (Imag.)
E4	ENTRY POINT FOR "CONJUG" ROUTINE
	No set-up required. Conjugates input data (negates imaginary components). Sets IRQ. Returns to Idle State. Exec. time = 30μsec.

1. Block Transfer Set-Up (INIT). Entry Address 01.

This routine presets the Index Register to allow block transfer to commence at any location other than 00.0 in the S2814A data RAM. An eight-bit word is loaded into the upper half of the input register and the routine executed as shown:

Figure 3A. Flowchart for Subroutine FT32IN

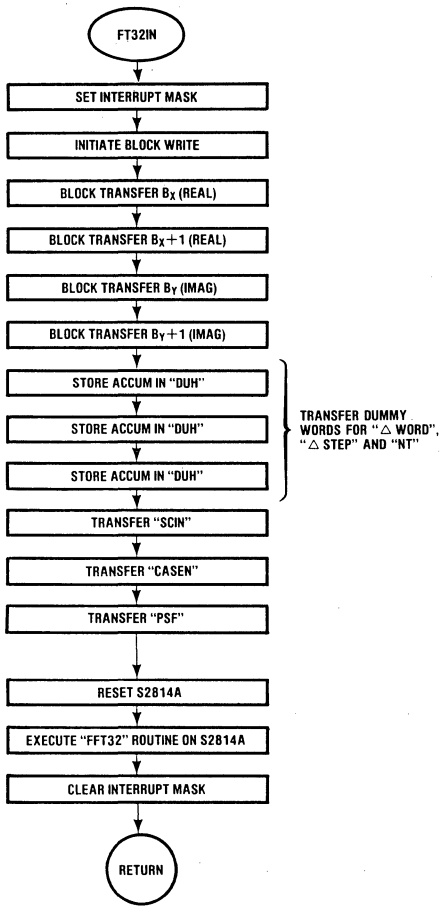
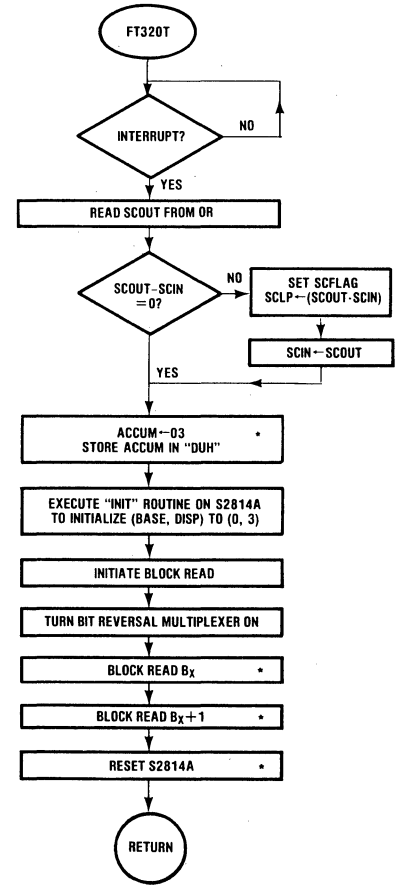


Figure 3B. Flowchart for Subroutine FT320T



*ASSUMES POWER SPECTRUM ONLY IS READ OUT.

```
DUH   EQU $HHH2
XEQ   EQU $HHH4


LDA   A #$XX
STA   A DUH
LDA   A #1
STA   A XEQ
```

where XX represents the start address for block transfer. The routine will be executed in 3 instruction cycles (0.9μsec.) and the S2814A will return to the idle state. Block transfer may then commence immediately.

2. FFT32. Entry Address = 04.

This is the basic 32 complex point FFT routine. For a 32 point FFT this routine is called once only and the output of the routine is the FFT. Larger FFTs are computed by decimating them into 32 point arrays before final processing of these arrays using FFT32 to obtain the final outputs. The following data is loaded into the S2814A, using block write starting at address 00.0, i.e., INIT is not used.

32 words of real input data (addresses 00.0 - 1F.0)

32 words of imaginary input data (addresses 00.1 -1F.1)

3 dummy words (to skip addresses) (addresses 00.2 -02.2)

SCIN (input scaling parameter) (address 03.2)

CASEN (CAS Enable) (address 04.2)

PSF (Power spectrum flag) (address 05.2)

Note that CASEN (Conditional array scaling enable) and PSF are not modified during processing, and need only be loaded once. CASEN should be positive to inhibit CAS (e.g. 0000) and negative to enable CAS (e.g. 8000). Note that SCIN is not needed if CAS is not enabled. PSF should be zero if the power spectrum output is not needed, any non-zero value (e.g. 0100) will cause the power spectrum to be computed. The block transfer should be terminated with the RST command, and the FFT32 routine called. Flow charts for loading and dumping the data are shown in Figure 3. The following sequence will cause the execution of the entire function:

```
CLR   B          ;CLEAR B ACC.
STA   A RST      ;RESET S2814A REGISTERS.
SEI              ;SET INT. MASK.
STA   A BLK      ;SET UP BLOCK WRITE.
JSR     BLKWT    ;WRITE 64 WORDS OF DATA.
STA   A DUH      ;WRITE DUMMY DATA TO 00.0
STA   A DUH      ;.....TO 00.1
STA   A DUH      ;.....TO 00.2
LDA   A SCIN     ;FETCH SCIN.
STA   A DLH      ;WRITE TO ADDRESS 00.3
STA   B DUH      ;COMPLETE WORD XFER.
LDA   A CASEN    ;FETCH CAS ENABLE.
STA   A DUH      ;WRITE TO ADDRESS 00.4
LDA   A PSF      ;FETCH PS FLAG.
STA   A DUH      ;WRITE TO ADDRESS 00.5
STA   A RST      ;RESET S2814A.
LDA   A #4       ;FFT32 START ADDRESS.
STA   A XEQ      ;START EXECUTING.
CLI              ;CLEAR INT. MASK.
WAI              ;WAIT FOR ROUTINE END.
LDA   A DLH      ;START OF INT. ROUTINE.
LDA   B DUH      ;(DUMMY).READ SCOUT.
LDA   B SCIN     ;FETCH SCIN.
STA   A SCIN     ;SCOUT→SCIN
SBA              ;COMP.SCOUT WITH SCIN.
BEQ     READ     ;JUMP IF NO CHANGE.
STA   A SCLP     ;(SCOUT-SCIN) → SCLP
LDA   A PASSN    ;FETCH PASS #
CMP   A #1       ;IS THIS 1ST.PASS?
BEQ     READ     ;IF SO, JUMP
JSR     SKOUT    ;SCALE PREVIOUS ARRAYS
LDA   A #3       ;(ASSUME PSF SET
STA   A DUH      ;PRESET TO ADDRESS 00.3
LDA   A #1       ;
STA   A XEQ      ;EXECUTE INIT.
STA   A BRV      ;TURN ON BIT REV.MUX.
LDA   A BLK      ;SET UP BLOCK READ.
JSR     BLKRD    ;READ DATA.
STA   A RST      ;END
```

The routine execution time is variable, depending on whether CASEN and PSF are set. The times are:

1. CAS - OFF. PSF - OFF 3730 instruction cycles (1.119msec.)
2. CAS - OFF. PSF - ON 3862 instruction cycles (1.159msec.)
3. CAS - ON . PSF - OFF 5867max. instruction cycles (1.760msec.)
4. CAS - ON . PSF - ON 5999max. instruction cycles (1.800msec.)

When CAS is enabled, the time depends on the number of times overflow is corrected. At the end of the routine the complex output data will have overwritten the input data in the memory (addresses 00.0 to 1F.1) and the power spectrum data will be in displacement 3 (addresses 00.3 -1F.3). The output scaling factor (SCOUT) will be loaded in the output register, generating the $\overline{IRQ}$ to signify to the host processor that the routine has completed processing.

3. Combination Pass Routine, COMPAS. Entry Address = D3.

This is the decimation routine that breaks up larger transforms into a number of 32 point transforms to be executed by FFT32. The N data points are split into N/16 blocks of 16 points, and pairs of blocks are passed through COMPAS. The procedure is repeated one or more times if N is greater than 64, but for a 64 point FFT the resulting data is ready for processing using FFT32. The procedure is explained in greater detail in the section "Executing Larger Transforms". The following data is loaded into the S2814A before execution:

Figure 4A. Flowchart for Subroutine CSIN

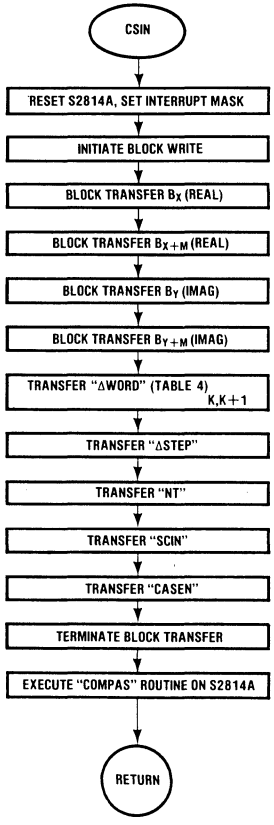
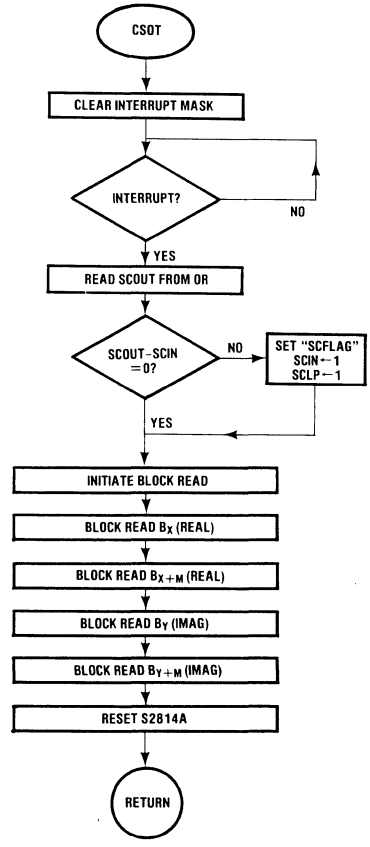


Figure 4B. Flowchart for Subroutine CSOT



32 words of real input data (addresses 00.0 - 1F.0)

32 words of imaginary input data (addresses 00.1 -1F.1)

Δ WORD (address 00.2)

Δ STEP Set up parameters (address 01.2)

NT (address 02.2)

SCIN (address 03.2)

CASEN (address 04.2)

PSF (address 05.2)

The new parameters required, Δ WORD, Δ STEP and NT are dependent on the size of the transform and Δ WORD changes with each pass through the COMPAS routine. The values required are shown in the tables in sections "Executing 64 Point Transforms" and "Executing Larger Transforms". Flow charts for loading and dumping the data are shown in Figure 4. The routine execution time varies with transform size and depends on whether CAS is enabled or not, as shown:

TRANSFORM SIZE	64 POINT	128 POINT	256 POINT	512 POINT
Without CAS, Inst. cycles, (μsec.)	776 (233)	828 (248)	842 (253)	949 (255)
With CAS. (Max.) Inst. cycles (μsec.)	1172(352)	1224(367)	1238(371)	1245(374)

4. Data Point Scaling Routine, SCALE. Entry location = EA.

If CAS is enabled, then routines COMPAS, and FFT32 will scale all 32 data points being processed if an overflow occurs during that pass. The value of SCOUT allows the data during subsequent passes to be scaled automatically during the pass. However, data points which have already been processed must also be scaled, so that all the data is scaled by the same factor during each processing step. SCALE is a routine that allows this to be done at high speed. Each block to be scaled is block loaded into the S2814A, the routine SCALE executed, and the block dumped back into the original locations in memory.

Care must be taken to keep track of which blocks have already been processed during each step, so that blocks do not get missed or scaled twice. The execution time depends on the scaling factor (SCOUT), as shown below:

Scaling Factor (SCOUT)	1	2	3	4	5
Execution time. Inst. Cycles, (μsec.)	170(51)	336(101)	502(151)	668(200)	834(250)

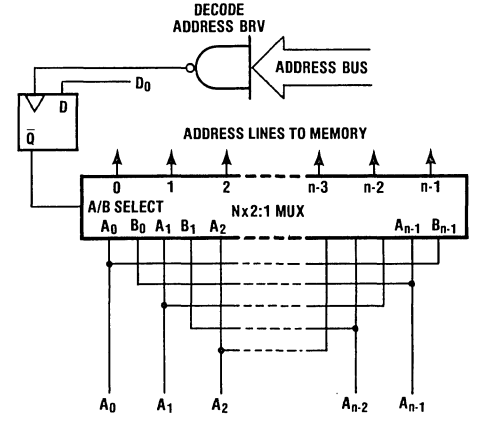
Windowing Routine, WINDOW. Entry Address = DC.

In order to allow the input data points to be windowed, a routine is provided to multiply the 32 real or complex points loaded in the S2814A by 32 window points. This is done on each block of 32 points prior to commencing the actual FFT processing. The input data required, in addition to the normal input data, are the 32 points of the window. They should be loaded into displacement 3 of the S2814A RAM and the routine WINDOW executed. The windowed data points will be returned to their original positions in the memory, so that COMPAS or FFT32 may then be executed immediately without further processing. The entire data can be loaded in a single block transfer operation by using INIT to preset the start address to 00.3. The 32 point window data is then loaded, followed by the signal data. This is possible because after loading the window the memory address will automatically reset to 00.0, the start address for the real data. The parameters are then loaded into displacement 2 addresses in the usual way. They will not be affected by the windowing operation. The total execution time is 163 instruction cycles, 49μsec.

Executing FFTs

Executing the FFTs consists of loading data blocks, executing routines in the S2814A and dumping the data. However, the sequence of the FFT output data is scrambled, and in order to use the results meaningfully, it must be unscrambled. This is done by reversing the order of the bits of the address lines for the final output data. Thus, for a 2^N point FFT the N address lines A_0, A_1, A_2 ..... A_{N-1} must be reversed to the sequence A_{N-1}, A_{N-2} ..... A_1, A_0 to address the output buffer memory. This is most conveniently done as the data points are being dumped out of the S2814A after the processing of the FFT32 routine(s). The bit reversal can be done either by software or hardware. The hardware realization is shown in Figure 5, and an example of software bit reversal is given in the section "Executing 32 Point FFTs."

Figure 5. Bit Reversal Hardware



Executing 32 Point Transforms

The basic 32 point transform is easily implemented with the S2814A since it simply requires the loading of the 32 real or complex data points and the 3 parameters SCIN, CASEN and PSF, executing FFT32 once only and dumping the data using bit reversal. The flowchart for this sequence is shown in Figure 6. It is assumed that the loading of data from the source into the input buffer and dumping of data from the output buffer to destination is carried out by the NMI (non-maskable interrupt) routine. The parameter SCIN should be set to zero, and the output data should be scaled (multiplied) by $2^{(SCOUT)}$ if absolute levels are wanted.

Figure 6. Flowchart for 32 Point FFT

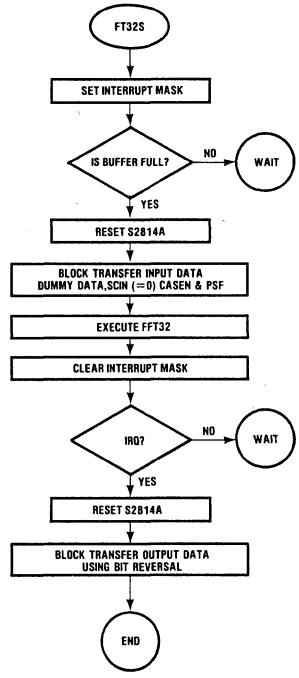
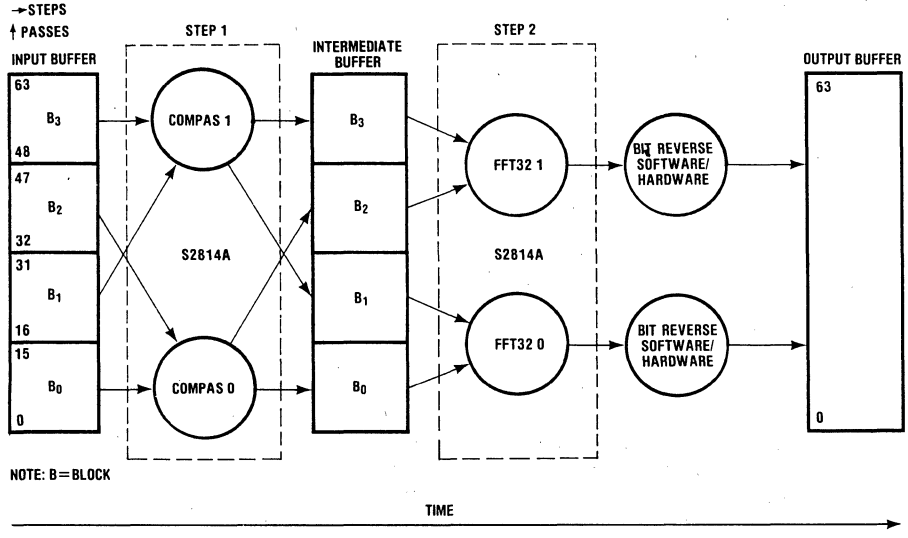


Figure 7. 64 Point FFT Flowgraph



Executing 64 Point Transforms

This is the simplest expansion of the FFT. The first step is to use COMPAS (twice) to decimate the data into two 32 point transforms, and then use FFT32 (twice) to produce the transforms. This is shown in the signal flow graph in Figure 7. The flow graph is independent of whether one or two S2814As are used, since the two passes through each of the 2 routines (COMPAS and FFT32) can be carried out sequentially or in parallel. The set up parameters for the 64 point FFT are:

For COMPAS 0: ΔWORD=8070
For COMPAS 1: ΔWORD=C070
} ΔSTEP=4000 NT=1

The treatment of SCIN and SCOUT is dealt with in the next section.

Executing Larger Transforms

The execution of larger transforms follows the same sequence as the 64 point transforms; namely the decimation of the data into a series of 32 point blocks that can be processed using FFT32. For a 2^N point FFT this involves N-5 steps of processing using COMPAS, and each step requires $2^{(N-5)}$ passes through the COMPAS routine. This is followed by $2^{(N-5)}$ passes through the FFT32 routine. Within each step, each pass may be carried out sequentially using a single S2814A, or in parallel using $2^{(N-5)}$ chips. There are also intermediate sequential + parallel combinations possible, of course, using fewer chips. A signal flow graph for 1 step is shown in Figure 8.

At the start of each step, SCIN should be set to zero. For the remaining passes in that step the value of SCOUT for the current pass should be used for SCIN for the next pass. The outputs of previously computed passes must be scaled using routine SCALE each time SCOUT increases during a pass. The maximum value of SCOUT after executing COMPAS is 1, and after executing FFT32 it is 5.

A flow chart for an N point transform control program is shown in Figure 9. The routine is called NFFT and uses the following subroutines.:

CSIN — procedure for loading S2814A with COMPAS input data (Figure 4A)
CSOT — procedure for dumping COMPAS output data (Figure 4B)
SCLPRV — procedure for scaling previously computed blocks of data in each step. See Figure 10.
FT32IN — procedure for loading S2814A with FFT32 input data (Figure 3a)
FT32OT — procedure for dumping FFT32 output data. (Figure 3b)

The values of ΔWORD, ΔSTEP and NT are shown in Tables 4 and 5.

Figure 8. N Point FFT Flowgraph

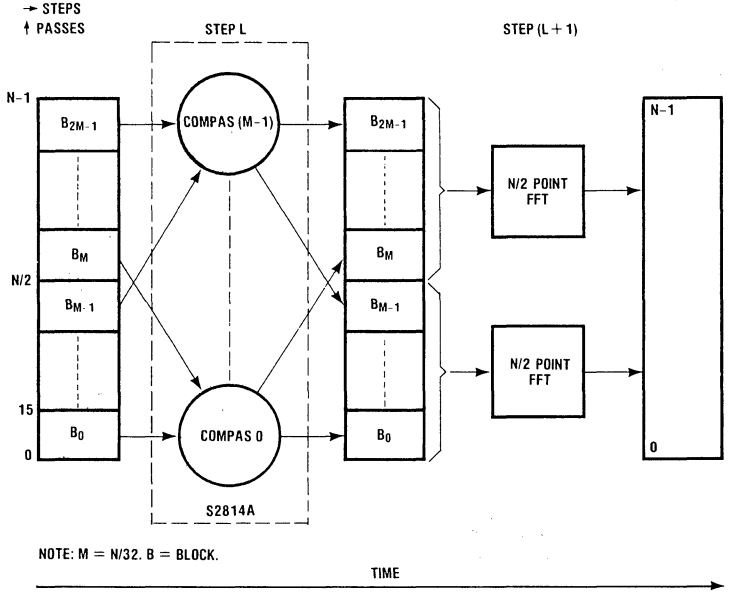
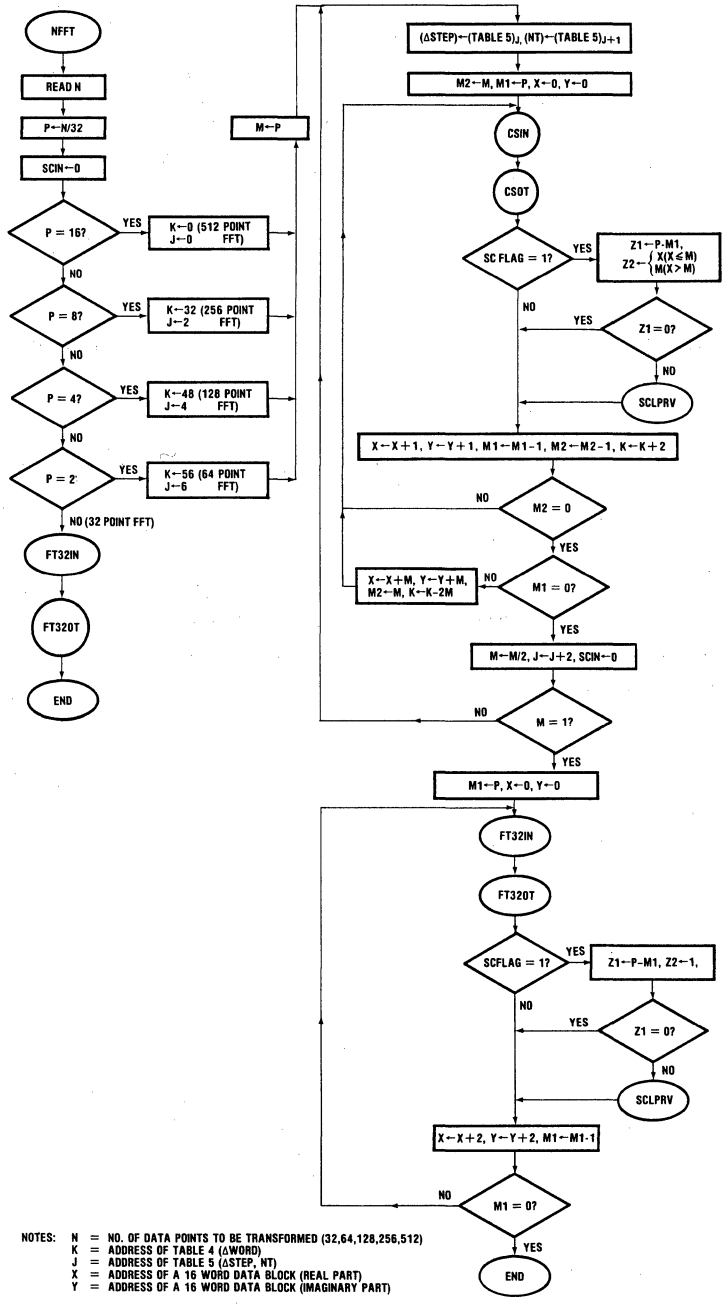


Figure 9. Flow Chart for N Point FFT, Routine "NFFT"



NOTES: N = NO. OF DATA POINTS TO BE TRANSFORMED (32,64,128,256,512)
K = ADDRESS OF TABLE 4 (ΔWORD)
J = ADDRESS OF TABLE 5 (ΔSTEP, NT)
X = ADDRESS OF A 16 WORD DATA BLOCK (REAL PART)
Y = ADDRESS OF A 16 WORD DATA BLOCK (IMAGINARY PART)

Figure 10. Flowchart for Subroutine "SCLPRV"

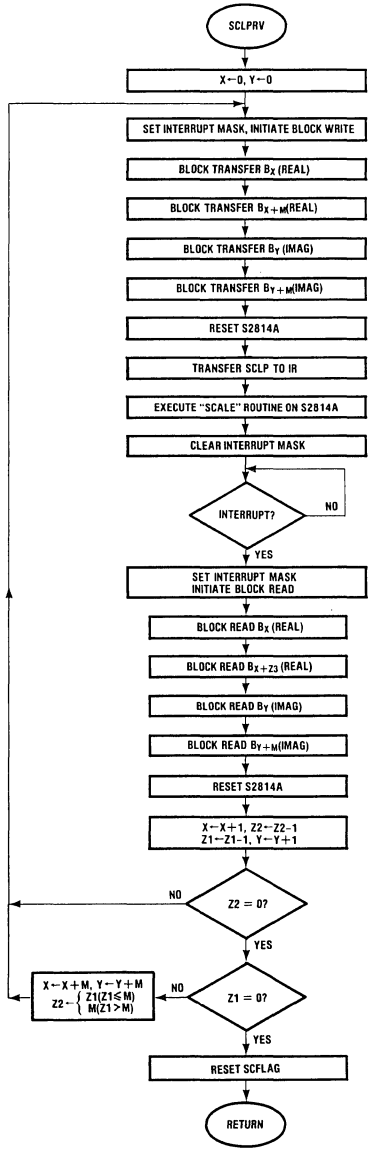


Table 4. (ΔWORD)

ENTRY PT for	K	VALUE	COMMENTS
512→	0	00	(ΔWORD L)
point	1	80	(ΔWORD H)
x'form	2	00	
	3	88	
	4	00	
	5	90	
	6	00	
	7	98	
	8	00	
	9	A0	
	10	00	
	11	A8	
	12	00	
	13	B0	
	14	00	
	15	B8	
	16	00	
	17	C0	
	18	00	
	19	C8	
	20	00	
	21	D0	
	22	00	
	23	D8	
	24	00	
	25	E0	
	26	00	
	27	E8	
	28	00	
	29	F0	
	30	00	
	31	F8	
256→	32	10	
point	33	80	
x'form	34	10	
	35	90	
	36	10	

Table 4 (continued)

ENTRY PT for	K	VALUE
	37	A0
	38	10
	39	B0
	40	10
	41	C0
	42	10
	43	D0
	44	10
	45	E0
	46	10
	47	F0
128 →	48	30
point	49	80
x'form	50	30
	51	A0
	52	30
	53	C0
	54	30
	55	E0
64 →	56	70
point	57	80
x form	58	70
	59	C0

Table 5. (ΔSTEP, NT)

ENTRY PT for	J	VALUE	COMMENTS
512 point	0	08	ΔSTEP(DUH)
x'form	1	0F	NT(DLH)
256	2	10	''
	3	07	''
128	4	20	''
	5	03	''
64	6	40	''
	7	01	''

Hardware.

The minimum hardware for a 32 point FFT is shown in Figure 11. All data transfer and control is handled by the S6802. The availability of the next input sample is signalled with the NMI line. A suitable analog interface is shown in Figure 12. The sampling clock is derived from the microprocessor clock, and the NMI signal is generated by the EOC (end of conversion) output of the A/D converter. This system may be expanded simply by adding more memory. The memory requirements are shown in Table 6. A word may be up to 16 bits long. In order to speed up the complete procedure it is necessary to use DMA for block transfer of data. The S2814A will transfer data at up to 4Mbytes/sec. A suitable DMA Address Generator is the Advanced Micro Devices AM 2940, but a 68B44 will accomplish the function more conveniently at a slightly lower speed (1.5Mbyte/sec).

Data Bus Interface.

Figure 13 shows how to interface the S2814A with a typical 6800 family microprocessor data bus. Note that the S2814A data bus must be isolated from the microprocessor system data bus by use of a PIA as in Figure 11 or a 74LS245 or 74LS645 type data transceiver as shown in Figure 13, since the S2814A drive capability is only one TTL load. The bus isolation may be omitted in some small systems.

Figure 11. 32/64 Point FFT Hardware

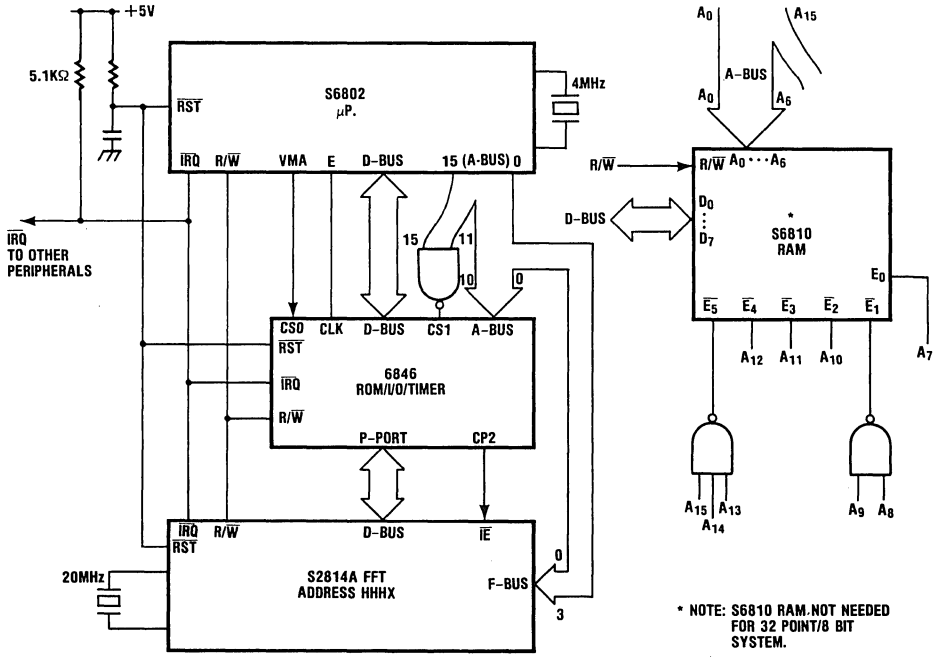


Figure 12. Analog Interface

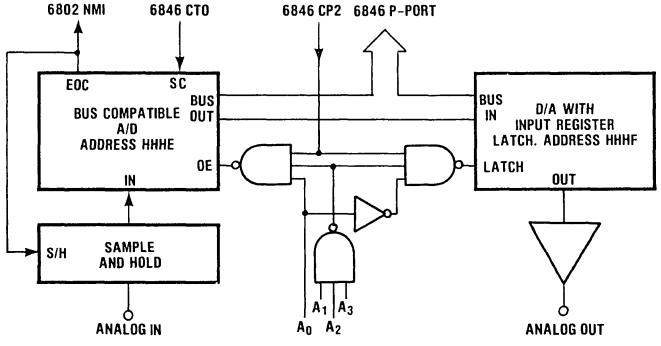


Figure 13. Interfacing the S2814A with a Microprocessor

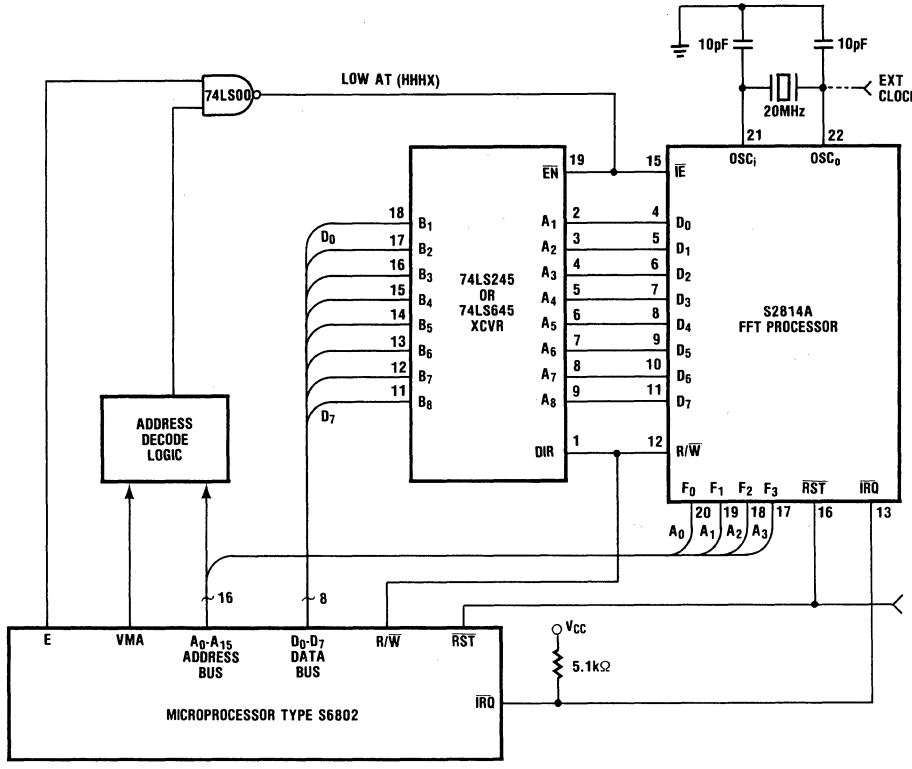


Table 6. Memory requirements for data point storage.

TRANSFORM SIZE (POINTS)	WORD LENGTH (BITS)	MEMORY REQUIREMENTS
32	8	64 bytes
	10/12	See Note 1
	16	128 bytes
64	8	128 bytes
	10/12	See Note 1
	16	256 bytes
128	8	256 bytes
	10/12	768 nibbles
	16	512 bytes
256	8	512 bytes
	10/12	1536 nibbles
	16	1024 bytes
512	8	1024 bytes
	10/12	3072 nibbles
	16	2048 bytes

Note 1: In practice the memory realization for these cases will be the same as for 16-bit systems.

Transform Execution Times.

The maximum execution times of transforms are shown in Table 7. The actual execution time when CAS is enabled will be between the times shown for CAS off and the maximum with CAS on. It will depend on the number of times that scaling has to be done.

FFT Resolution and Dynamic Range

The use of the Decimation in Frequency (DIF) algorithm in the S2814A ensures optimum signal to noise ratio, (SNR) for the architecture used. The use of the Conditional Array Scaling (CAS) gives a total dynamic range of approximately 70dB on all sizes of Transforms. The maximum resolution obtainable is approximately 57dB. CAS operates by detecting overflow in the butterfly computation routine. As soon as an overflow is detected the two points being combined in that butterfly are halved in magnitude (both the real and imaginary portions) and the butterfly recomputed. A flag is set, all previously computed butterfly outputs are then scaled, and all the inputs to subsequent butterflies are scaled before computation begins, so that at the end of the pass all points have been scaled equally. A scale factor is made available (SCOUT) so that the remaining data points in larger transforms, i.e., those other than the 32 in the S2814A when the overflow occurred, may also be scaled to keep them all in line. Thus, CAS operates as a discrete AGC, halving the signal levels each time an overflow is detected. By using SCOUT after executing the FFT the output may be expanded, so that the levels displayed in the spectrum will increase monotonically as the input increases.

Table 4. Total FFT execution times including block transfers. (msec.)

TRANSFORM SIZE	USING SINGLE S2814A BLOCK TRANSFER USING:				USING MULTIPLE S2814A ARRAY		
	A S6802 (22μsec/word)		B DMA 2MW/sec		# OF S2814As	C (USING DMA AT 2MW/sec)	
	MIN	MAX	MIN	MAX		MIN	MAX
32 pt.	4.0	4.6	1.3	1.9	1	1.3	1.9
64	14.2	15.7	3.2	4.6	2	1.6	2.3
128	40.7	44.0	7.6	11.0	4	1.9	2.8
256	106	114	17.8	25.4	8	2.3	3.2
512	262	280	40.7	57.9	16	2.6	3.7

Note: Minimum times assume that CAS and PSF are off. Maximum times assume that CAS and PSF are on, and that maximum overflow occurs during 1st pass. All times assume 20MHz clock frequency and must be increased proportionally for lower clock frequencies (except Column A).

DIGITAL FILTER/UTILITY PERIPHERAL

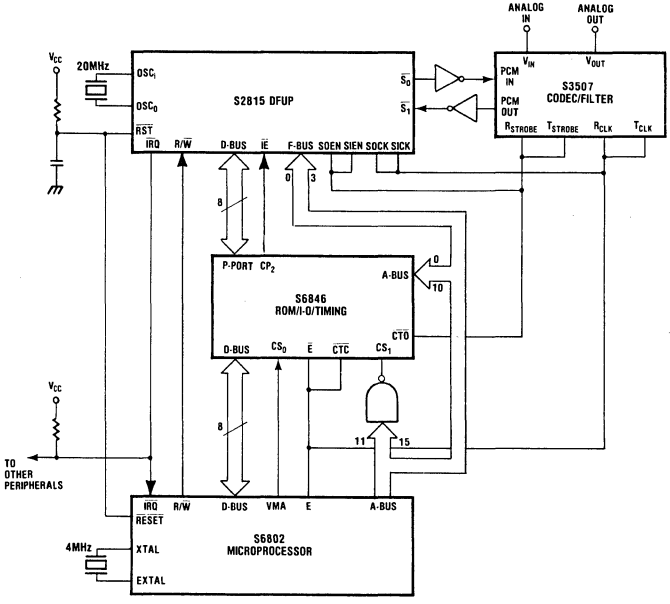
Features

- ☐ S2811 Signal Processing Peripheral Programmed With Filter and Utility Routines
- ☐ Microprocessor Compatible Interface Plus Asynchronous Serial Interface
- ☐ Two Independent 30 Tap Transversal Filter Routines, Cascadable into a Single 60 Tap Filter
- ☐ Two Recursive (biquadratic) Filters Providing a Total of 16 Filter Sections
- ☐ Computation Functions: Two Integrating, Two Rectifying, Squaring, and Block Multiply Routines
- ☐ Conversion Functions: μ255 Law-to-Linear, Linear-to-μ255 Law, and Linear-to-dB Transformations
- ☐ Generator Functions: Sine and Pseudo-Random Noise Patterns

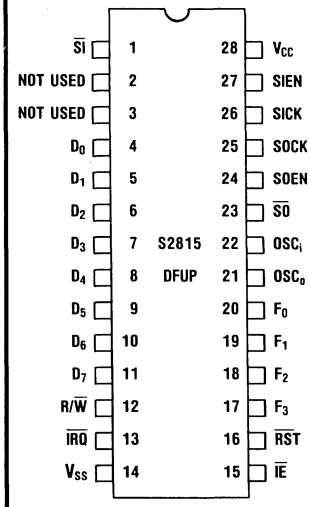
General Description

The AMI S2815 Digital Filter/Utility (DFUP) is a pre-programmed version of the S2811. Architectural and internal operating details of the S2811 may be found in the S2811 Advanced Product Description. The S2815 has been programmed with a collection of filter, computational, conversion, and generator routines which may be selected individually, or cascaded under control of the host processor. This arrangement allows a wide range of

Typical System Configuration



Pin Configuration



General Description (Continued)

signal processing functions frequently required in application areas such as telecommunications, test and instrumentation, industrial automation, process control, etc., to be satisfied by a single S2815 DFUP.

The I/O structure of the S2815 provides flexibility and easy interfacing in microprocessor based systems. Input and output data transfers may be accomplished serially, as shown in the block diagram, using a μ255-law Codec such as the S3507, or using linear A/D and D/A converters. Data may also be transferred in parallel under control of a host processor, such as the S6802. Routines may be executed individually, completely under control of the host processor, or internal transfer addresses may be set up by the host, allowing routines to be cascaded internally. The ability to cascade routines allows complicated functions to be completed without intervention by the host processor.

Absolute Maximum Ratings

Supply Voltage	7.0VDC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Voltage at any Pin	V_{SS} −0.3 to V_{CC} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C

Electrical Specifications: (V_{CC}=5.0V ±5%, V_{SS}=0V, T_A=0°C to +70°C, unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input HIGH Logic "1" Voltage	2.0		V_{CC}+0.3	V	V_{CC}=5.0V
V_{IL}	Input LOW Logic "0" Voltage	−0.3		0.8	V	V_{CC}=5.0V
I_{IN}	Input Logic Leakage Current		1.0	2.5	μAdc	V_{IN}=0V to 5.25V
C_I	Input Capacitance			7.5	pF	
V_{OH}	Output HIGH Voltage	2.4			V	I_{LOAD}=−100μA, V_{CC}=min, C_L=30pF
V_{OL}	Output LOW Voltage			0.4	V	I_{LOAD}=1.6mA, V_{CC}=min, C_L=30pF
f_{CLK}	Clock Frequency	5.0	20		MHz	V_{CC}=5.0V
P_D	Power Dissipation		1.2		W	V_{CC}=5.0V
f_{CLK}(max)	Maximum Clock Frequency				MHz	V_{CC}=5.0V
	S2815-10	10				
	S2815-12	12				
	S2815-15	15				
	S2815	20				

S2815 Function/Descriptions

Microprocessor Interface (16 pins)

D_0 through D_7	(Input/Output) Bi-directional 8-bit data bus.
F_0 through F_3	(Input) Control Mode/Operation Decode. Four microprocessor address leads are used for this purpose. See "CONTROL MODES AND OPERATIONS." (Table 2.)
$\overline{IE}$	(Input) Interface Enable. A low level on this pin enables the SPP microprocessor interface. Generated by microprocessor address decode logic.
$R/\overline{W}$	(Input) Read/Write Select. When HIGH, output data from the SPP is available on the data bus. When LOW, data can be written into SPP.
$\overline{IRQ}$	(Output) Interrupt Request. This open-drain output will go LOW when the SPP needs service from the microprocessor.
$\overline{RST}$	(Input) When LOW, clears all internal registers and counters, clears all modes and initiates program execution at location 00.

Serial Interface (6 pins)

SICK, SOCK	(Input) Serial Input/Output Clocks. Used to shift data into/out of the serial port.
$\overline{SI}$	(Input) Serial Input. Serial data input port. Data is entered MSB first and is inverted.
SIEN	(Input) Serial Input Enable. A HIGH on this input enables the serial input port. The length of the serial input word (16 bits maximum) is determined by the width of this strobe.
$\overline{SO}$	(Output) Serial Output. Three-state serial output port. Data is output MSB first and is inverted.
SOEN	(Input) Serial Output Enable. A HIGH on this input enables the serial output port. The length of the serial output (16 bits maximum) is determined by the width of this strobe.

Miscellaneous

OSC_i, OSC_o	An external 20MHz crystal with suitable capacitors to ground can be connected across these pins to form the time base for the SPP. An external clock can also be applied to OSC_o input if the crystal is not used.
V_{CC}, V_{SS}	Power supply pins $V_{CC} = +5V$, $V_{SS} = 0$ volt (ground).

Functional Description

The S2815 is a pre-programmed version of AMI's S2811 Signal Processing Peripheral. This is a high speed microcomputer organized for efficient signal processing and contains a data memory, instruction memory, an arithmetic unit incorporating a 12-bit parallel multiplier, as well as control registers and counters. For more detailed information about the chip, please refer to the S2811 Advanced Product Description.

The S2815 Instruction ROM contains the various routines which make up the DFUP package. The routines together with their starting addresses in the Instruction ROM, are shown in Table 1A.

The Data ROM contains the parameters required to execute the functions. 128 words of Data RAM and an 8 word scratchpad are provided to hold the signal data and the jump addresses for cascading routines. The Data memory is arranged as a matrix of 32×8 words, as shown in Table 1B. The RAM utilization is routine dependent and is illustrated in the routine descriptions.

Table 1. Software Model of S2815

A. Routine Locations in Instruction Memory

(LOC (HEX)	FUNCTION
00	IDLE STATE
01	ENTRY POINT "INIT" ROUTINE
04	ENTRY POINT "SETUP" ROUTINE
18 or 19*	ENTRY POINT "LINIP" ROUTINE
1B or 1C*	ENTRY POINT "MULIP" ROUTINE
34	ENTRY POINT "LINO1" ROUTINE
36	ENTRY POINT "LINO2" ROUTINE
38	ENTRY POINT "MULOP" ROUTINE
65	ENTRY POINT "DBOP" ROUTINE
80	ENTRY POINT "BMPY" ROUTINE
87	ENTRY POINT "IIR1" ROUTINE
96,97 or 98*	ENTRY POINT "IIR2" ROUTINE
A7	ENTRY POINT "FIR1" ROUTINE
AF, B0 or B1*	ENTRY POINT "FIR2" ROUTINE
BC	ENTRY POINT "RECT" ROUTINE
BF	ENTRY POINT "SQUAR" ROUTINE
C4	ENTRY POINT "FINT" ROUTINE
CA	ENTRY POINT "RINT" ROUTINE
CE	ENTRY POINT "SQUINT" ROUTINE
D6	ENTRY POINT "SINE" ROUTINE
E5	ENTRY POINT "NSET" ROUTINE
E9	ENTRY POINT "NOISE" ROUTINE

*See Routine descriptions for explanation of alternative entry points

B. Data Memory Map

DISPLACEMENT →	0	1	2	3	4	5	6	7
BASE ↓ 00								
01								
02								
⋮		DATA RAM			COEFFICIENT ROM			
1E								
1F								
SCRATCHPAD			ALL RAM					

NOTE: Address [Base AB, Displacement C] is written as AB.C

C. Control Functions

F-Bus (HEX)	MNEMONIC
0	CLR
1	RST
2	DUH
3	DLH
4	XEQ
5	SRI
6	SRO
7	SMI
8	SMO
9	BLK
B	SOP
C	COP

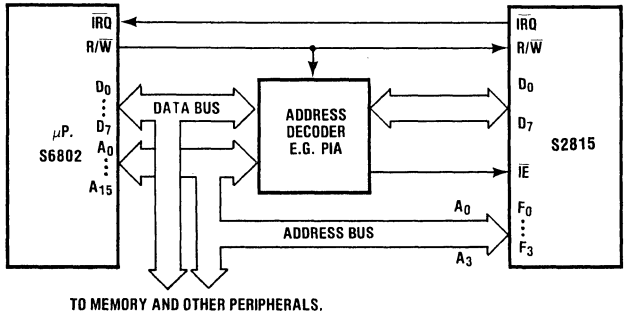
See Table 2 for descriptions

D. Input and Output Registers

15 — 8	7 — 0
DUH (MSByte)	DLH (LSByte)

Code is Two's Complement

Figure 1. Conection of S2815 as a Memory Mapped Peripheral



Initial Set-Up Procedure

After power up, the $\overline{RST}$ line should be held low for a minimum of 300nsec. If this line is connected to the reset line of the microprocessor, this condition will be met easily. This will clear the Base and Index Registers, which are used for memory addressing, the Loop Counter and the Program Counter. Address zero in the Instruction ROM contains a Jump to Zero instruction, and thus the S2815 will remain in an idle state after being reset.

The Control Functions

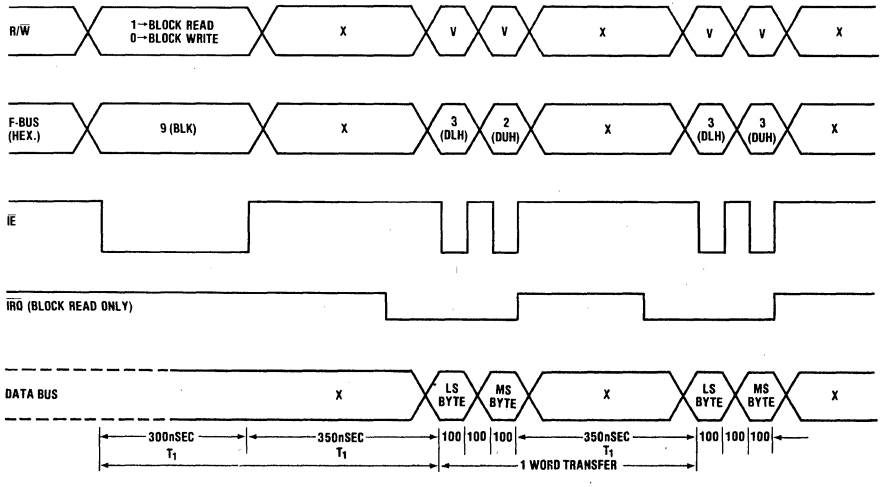
The S2815 is controlled by the host microprocessor by means of the F-bus, Interface Enable ($\overline{IE}$) and the Read-Write (R/$\overline{W}$) lines. It should be connected to the host processor as a memory mapped peripheral as shown in Figure 1.

The 12 most significant address lines decode a group of 16 addresses to activate the $\overline{IE}$ line each time an address in the group is called, and the S2815 is controlled by reading to or writing from those addresses. Only 12 of these addresses are used as described in Table 2. Throughout this Product Description these addresses will be referred to as HHHX (X=0-F).

The Block Transfer Operation

Block transfer is the mode used to load and unload the main data blocks into the S2815 at up to 4Mbytes/sec. In this mode the data memory is addressed by the Index Register, and after initialization the internal addressing is sequential and automatic. The sequence generated is that after each word transfer (16-bit words as 2 bytes, or 8-bit words as MSbyte (DUH) only) the base is incremented. After base 1F (31) has been reached, the base resets to 00 and the displacement increments. After base 1F displacement 3 has been reached (i.e., the highest address in the RAM, 1F.3), both base and displacement reset to zero. Note that when the BLK command is given the Read/Write line is latched internally, and remains latched until the RST command is given. The block transfer sequence and timing are shown in Figure 2.

Figure 2. Block Transfer Sequence and Timing



NOTE 1: X=DON'T CARE, OR NOT VALID V=VALID

NOTE 2: ALL TIMES SHOWN ARE MINIMUM AND MUST BE INCREASED PROPORTIONALLY WHEN USING REDUCED SPECIFICATION PARTS AS FOLLOWS:

$$T_{1\,MIN} = \left\lceil \frac{6000}{f_{CLK}} + 50 \right\rceil \text{ nsec}$$

Table 2. S2815 Control Functions

MEMONIC	F-BUS HEX	DATA	TYPE OF OPERATION	FUNCTION
CLR	0	XX	XX	Clears all functions previously set. Sets SOP.
RST	1	XX	XX	Clears all registers. Starts program execution at location 00. This is the idle state. This instruction should precede block read, block write and execute commands.
DUH	2	HH	READ/WRITE	Reads from or writes into S2815 the upper half of the data word (See Table 1D). Must always follow DLH (Mandatory).
DLH	3	HH	READ/WRITE	Reads from or writes into S2815 the lower half of the data word (See Table 1D). Precedes DUH when used.
XEQ	4	HH	WRITE	Starts Execution at Location HH.
SRI	5	XX	XX	Enables Serial Input Port.
SRO	6	XX	XX	Enables Serial Output Port.
SMI	7	XX	XX	Converts sign + magnitude serial input data to two's complement.
SMO	8	XX	XX	Converts two's complement internal data to sign + magnitude serial output data.
BLK	9	XX	READ/WRITE	Initiates a block read or block write operation. The entire data RAM can be accessed sequentially beginning with values of base and displacement initialized using "Block Transfer Set Up" routine. If a reset operation is performed prior to block command, the data memory address is initialized to base 0, displacement 0. Block read or write operation can be terminated any time by performing a reset operation. The index register is used to address the memory during block transfer and internal addressing is sequenced automatically.
SOP	B	XX	XX	Set overflow protect. Normal mode of operation.
COP	C	XX	XX	Clear overflow protect.
	A,D-F			Do not use

Note: XX = Don't Care
HH = 2 Hex characters (8-bit data)

In 6800 Assembly Lanaguage a Block Write would be executed with the following code:

```
LDX   OFFST   ;LOAD MEMORY START ADDRESS INTO INDEX REG.
STA   A BLK   ;WRITE DUMMY DATA TO ADDRESS $HHH9.BLOCK MODE.
LDA   A 0,X   ;READ FIRST BYTE FROM MEMORY.
STA   A DLH   ;WRITE INTO S2815 AS LSBYTE.ADDRESS $HHH3
LDA   A 1,X   ;READ SECOND BYTE FROM MEMORY.
STA   A DUH   ;WRITE INTO S2815 AS MSBYTE.ADDRESS $HHH2
LDA   A 2,X   ;SECOND WORD.
  •     •       •
  •     •       •
  •     •       •
LDA   A 62,X  ;32ND. WORD,LSBYTE.
STA   A DLH   ;
LDA   A 63,X  ;32ND. WORD,MSBYTE.
STA   A DUH   ;END OF TRANSFER.
STA   A RST   ;WRITE DUMMY DATA TO ADDRESS $HHH1.RESET S2815
```

Block Read would be executed by substituting LDA A for STA A, and vice versa.

```
where:   RST   EQU   $HHH1
         DLH   EQU   $HHH3
         DUH   EQU   $HHH2
         BLK   EQU   $HHH9
```

The above code assumes that the block transfer is controlled by the host processor, not using DMA. Note that DLH must always precede DUH. 8-bit data may be transferred using DUH only, assuming that the significance of the data is correct.

Block transfer must be used for loading all filter coefficients (IIR1, IIR2, FIR1, FIR2, FINT, RINT and SQINT routines) and for loading and dumping the data for the BMPY routine.

The DFUP Routines

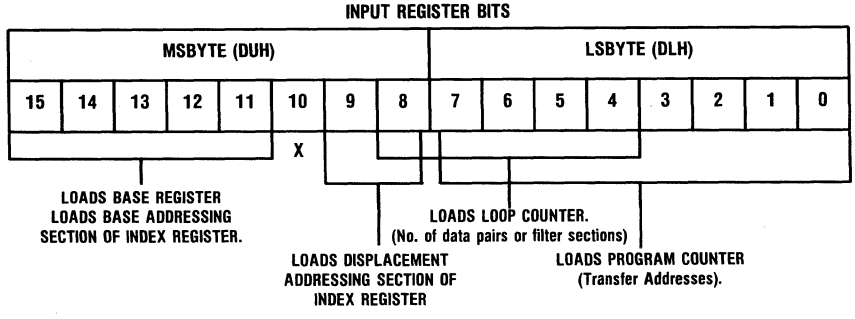
21 Individual routines are stored in the S2815 Instruction Memory. Routines INIT, SETUP, BMPY and NSET all return to the idle state after execution since they are not repetitive functions. All other routines are designed to be used repetitively with or without intervention from the control microprocessor by using loadable jump addresses to exit each routine. Thus, a number of routines may be strung together by setting the exit jump address of one to be the start address of the next. The entire function may be arranged as a closed loop, so that it will execute continuously after starting, or as an open ended string, so that it will execute once only after starting. This feature, together with the conditional synchronization feature incorporated in the 4 input routines, makes the S2815 extremely flexible as a digital filter/signal processor peripheral. The starting addresses, functions, parameters required and exit-jump (transfer) address locations are shown in Table 3.

Table 3. Parameters and Transfer Data Storage Locations:

ROUTINE	ENTRY POINT	STORAGE LOCATIONS FOR: (To be loaded using SETUP)	
		EXIT TRANSFER ADDRESS	FOR PARAMETERS
1. INIT	01	Returns to idle	None
2. SETUP	04	Returns to idle	None
3. LINIP	18 or 19*	Scratchpad 2	None
4. MULIP	1B or 1C	Scratchpad 2	None
5. LINO1	34	Scratchpad 3	None
6. LINO2	36	RAM $1E.2	None
7. MULOP	38	Scratchpad 3	None
8. DBOP	65	RAM $1E.2	None
9. BMPY	80	Returns to idle	Scratchpad 2
10. IIR1	87	Scratchpad 4	Scratchpad 7
11. IIR2	96, 97 or 98*	Scratchpad 5	Scratchpad 6
12. FIR1	A7	Scratchpad 5	Scratchpad 7
13. FIR2	AF, B0 or B1*	Scratchpad 4	Scratchpad 7
14. RECT	BC	RAM $1F.2	None
15. SQUAR	BF	RAM $1F.2	None
16. FINT	C4	RAM $1F.0	None
17. RINT	CA	RAM $1E.0	None
18. SQINT	CE	RAM $1E.0	None
19. SINE	D6	RAM $1E.0	None
20. NSET	E5	Returns to idle	None
21. NOISE	E9	RAM $1E.0	None

*See Routine Descriptions for explanation of alternative entry points

Figure 3. Input Data Significance for Register Loading



1. Block Transfer Set-up (INIT). Entry Address $01

This routine presets the Index Register to allow block transfer to commence at any location other than 00.0 in the S2815 data RAM. An eight-bit word is loaded into the upper half of the input register and the routine is executed as shown:

```
            LDA   A     #$XX
            STA   A     DUH
            LDA   A     #1
            STA   A     XEQ

where:      DUH   EQU   $HHH2
            XEQ   EQU   $HHH4
```

where XX represents the start address for block transfer. The bits used are shown in Figure 3. The routine will be executed in 3 instruction cycles (0.9μsec.) and the S2815 will return to the idle state. Block transfer may then commence immediately.

2. Parameter and Transfer Address Set-up (SETUP). Entry address $04

This routine allows the parameters and transfer addresses to be loaded into the appropriate memory locations prior to executing a function. The loading sequence is: Scratchpads 2 through 7, followed by main RAM locations $1E.0, $1E.2, $1F.0 and $1F.2. The input register bits loaded into the various internal registers are shown in Figure 3. Before executing the routine the input data for scratchpad 2 (S(2)) must be loaded into the input register. This may be omitted when not using the input routines LINIP or MULIP. While the routine is being executed the remaining input data must be loaded sequentially, allowing a minimum of 2 instruction cycles (0.6μsec.) between each word. An example of a 6800 language control program to execute SETUP is shown below:

```
SP    STA   A RST     ;RESETS S2815
      LDX     OFFST   ;LOAD MEMORY START ADDRESS INTO IX.REG.
      LDA   A 0,X     ;READ FIRST BYTE (DATA FOR S(2))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OR IR (DUMMY DATA)
      LDA   A #4      ;LOAD ACC. WITH "SETUP" START ADDRESS
      STA   A XEQ     ;START EXECUTION
      LDA   A 1,X     ;READ SECOND BYTE (DATA FOR S(3))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
      LDA   A 2,X     ;READ THIRD BYTE (DATA FOR S(4))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
      LDA   A 3,X     ;READ FOURTH BYTE (DATA FOR S(5))
      STA   A DLH     ;LOAD INTO LSBYTE OF IR
      STA   A DUH     ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
      LDA   A 4,X     ;READ FIFTH BYTE (LSBYTE FOR S(6))
      STA   A DUH     ;LOAD INTO LSBYTE OF IR
      LDA   A 5,X     ;READ SIXTH BYTE (MSBYTE FOR S(6))
      STA   A DUH     ;LOAD INTO MSBYTE OF IR
      LDA   A 6,X     ;READ SEVENTH BYTE (LS BYTE FOR S(7))
      STA   A DUH     ;LOAD INTO LSBYTE OF IR
```

```
LDA     A 7,X       ;READ EIGHTH BYTE (MSBYTE FOR S(7))
STA     A DUH       ;LOAD INTO MSBYTE OF IR
LDA     A 8,X       ;READ NINTH BYTE (DATA FOR RAM $1E.0)
STA     A DUH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
LDA     A 9,X       ;READ TENTH BYTE (DATA FOR RAM $1E.2)
STA     A DLH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
LDA     A A,X       ;READ ELEVENTH BYTE (DATA FOR RAM $1F.0)
STA     A DLH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
LDA     A B,X       READ TWELFTH BYTE (DATA FOR RAM $1F.2)
STA     A DLH       ;LOAD INTO LSBYTE OF IR
STA     A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)

where:      RST   EQU   $HHH1
            DLH   EQU   $HHH3
            DUH   EQU   $HHH2
            XEQ   EQU   $HHH4
```

Note that the sequence may be aborted at any point with a STA A RST instruction. Since transfer addresses are stored in the LSByte of each 16-bit memory location, it is necessary to load dummy data into the MSByte (DUH) of the input register each time to terminate word transfer. Scratchpads 6 and 7 may hold valid data in both bytes, however. After the final data is loaded, the S2815 will return to the idle state after completion of the routine. This takes 3 instruction cycles (0.9μsec) maximum. If it is not necessary to load all the data (this is dependent on which routines are used), the routine may be aborted at any point by using the RST command, allowing a minimum of 2 instruction cycles (0.6μsec) after entering the last data required.

3. Linear Input Routine (LINIP). Entry address $18 or $19

The LINIP routine takes linearly coded (i.e., non-companded) input data from the input register and loads it into scratchpad 0 (S(0)) without modification, where it may be accessed by one of the other routines. Entering at address $18 will cause the S2815 to wait for new input data each time the routine executes. This allows the signal processing to be synchronized to the input sampling rate automatically, provided that the total execution time of all the routines cascaded to realize the overall function is less than the sampling period. If no new input data has been received when the S2815 executes line $18, then the $\overline{IRQ}$ line (interrupt request) will be set low. It will reset as soon as new data is loaded. This will occur only if the input port is in the parallel mode, i.e., the SRI mode is not set. The $\overline{IRQ}$ line is not activated in the serial mode. If the routine is entered at address $19, the processing will not wait for new input data each time, and will simply re-use the old data if none has been received. The execution time of the routine is 3 instruction cycles (0.9μsec) after receipt of new input data when entering at address $18, and 2 instruction cycles (0.6μsec) (independent of data receipt) when entering at address $19. Input data may be up to 16 bits wide. This routine exits to the transfer address stored in S(2).

4. Mu-Law Input Routine (MULIP). Entry address $1B or $1C

The MULIP routine takes μ-255 law companded data from the input register (MSByte, bits 15-8) and loads it into S(0) after linearization, i.e., decompanding. The conversion is exact. It is then suitable for linear processing and may be accessed by one of the other routines. Entering at address $1B will cause the S2815 to wait for new input data and set the $\overline{IRQ}$ line low each time the routine is executed, while entering at address $1C bypasses this feature. For details see LINIP routine description. The execution time is data dependent, being 18 instruction cycles (5.4μsec) after receipt of new input data (maximum) when entering at address $1B, and one cycle (0.3μsec) less when entering at address $1C, as for LINIP. This routine exits to the transfer address stored in S(2).

5. Linear Output Routine (LINO1). Entry address $34

The LINO1 routine takes the output data stored in S(0) and loads it into the output register without modification. This will set the $\overline{IRQ}$ line (interrupt request) low if the output port is in the parallel mode, i.e., the SRO mode is not

set. The $\overline{IRQ}$ line is not activated in the serial mode. The contents of the output register will be overwritten each time the LINO1 routine is executed. The execution time is 2 instruction cycles (0.6μsec). The routine exits to the transfer address stored in S(3).

6. Alternative Linear Output Routine (LINO2). Entry address $36

This routine is identical to LINO1, except that the exit transfer address is stored in RAM $1E.2.

7. Mu-Law Output Routine (MULOP). Entry address $38

The MULOP routine takes the output data stored in S(0) and loads it into the output register (MSByte, bits 15-8) after companding, i.e. compression according to the μ-255 law. The conversion is exact. The other features of this routine are as for LINO1. The execution time is data dependent, being 35 instruction cycles (10.5μsec) maximum. The routine exits to the transfer address stored in S(3).

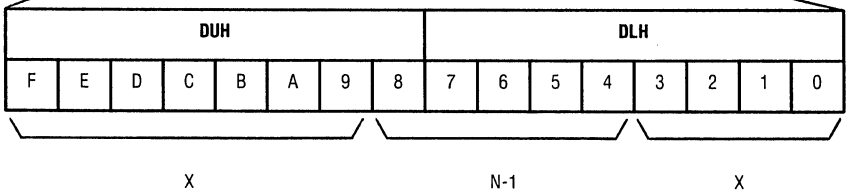
8. Decibel Output Routine (DBOP). Entry address $65

This routine takes the output data stored in S(0) and loads it into the output register after converting it to negative decibels, i.e., the result will be "dB below reference", or dBR without the sign. The integer portion of the output will be in the MSByte (bits 15-8) and the fractional part in the LSByte (bits 7-0), both as hexadecimal, positive numbers, making conversion to decimal (if required) by the control processor a simple task. All data is treated as fractional in the S2815, i.e., it lies in the range ±1. In 16 bit two's complement hex this is represented as $8000 (−1) to $7FFF ($+1 - 2^{-15}$), since +1 does not really exist in this code, being equal to −1 ($8000). The decibel reference (0dB) is taken to be +1, so that the result of decibel conversion is always negative in the DBOP routine. The output result, however, is expressed as a pure magnitude, without the minus sign, which is implicit. The conversion is accurate to ±0.01dB down to −20dB (0.1), ±0.02dB down to −40dB (0.01), and ±0.1dB down to −60dB (0.001). The conversion law used is "voltage" to dB, i.e., 20 $\log_{10}$(V), and the result must be divided by two if the result is a "power" measurement. The execution time is data dependent, being 132 instruction cycles (39.6μsec.) maximum. The routine exists to the transfer address stored in RAM $1E.2.

Table 4. Memory Map for BMPY Routine

DISPLACEMENT →		0	1	2	3	
BASE ↓	00	A1	B1	X	P1	
	01	A2	B2	X	P2	
	02	A3	B3	X	P3	
	03	A4	B4	X	P4	
	1E	A31	B31	X	P31	
	1F	A32	B32	X	P32	
SCRATCHPAD		X	X	N-1	X	X

A,B=input data pair
P=product, AB
X=Don't care



9. Block Multiply Routine (BMPY). Entry address $80

This routine allows the user to multiply together an array of up to 32 pairs of data. The routine is not cascadable with any of the others since all data I/O must be done using the block transfer mode, and so the routine returns to the idle state after execution. The only parameter required for executing this routine is the number of data pairs to be multiplied N. The value of N-1 (i.e., the number of pairs minus one) is loaded into scratchpad 2, using the SETUP routine and then the data pairs are loaded into the RAM using the block transfer procedure. The memory map for the BMPY routine is shown in Table 4. After resetting the S2815 and setting it into the block write mode the A inputs are first loaded sequentially. If there are 32 of them, the B inputs may then be loaded sequentially without any break in the procedure (see "Block Transfer Operation").

If fewer than 32 pairs of data are involved, there are two ways of handling the procedure:

1) After loading the N values of A, load (32-N) dummy data inputs. Only the MSByte need be loaded (DUH). The internal addressing will then be set to accept the N values of B.

2) After loading the A inputs, reset the S2815 again and execute the INIT routine to set the index register to address $00.1. The input data will be $0100, although only the MSByte need be loaded (DUH = $01). Then set the S2815 into the block write mode again (without resetting) and continue loading the B inputs.

After the data pairs are loaded, the S2815 should be reset and the routine BMPY executed. The execution time is 4 + 3N instruction cycles, so that for 32 data pairs this will be 100 cycles (30μsec.). After execution the S2815 will return to the idle state and set the $\overline{IRQ}$ line low, to indicate completion. The final product (P_N) is available in the output register at this time and may be read without the use of the block transfer mode. This is useful when multiplying single data pairs. To read all the products it is necessary to first reset the S2815 and execute INIT to set the index register to address $00.3. The input data will be $0300 (DUH = $03). Setting the S2815 into the block read mode then allows the N products P to be read sequentially. Finally, the S2815 should be reset again to bring it out of the block transfer mode. The 6800 program shown below will execute the BMPY program to multiply together 2 data pairs. For simplicity, only 8 bit input data is used (DUH) and only the MSByte of the product is read, although products will be computed to 16 bits of precision for all data up to 12 bits wide.

```
BY   LDA   A #$10      ;1 = N – 1.(2 DATA PAIRS)
     STA   A DLH       ;LOAD INTO LSBYTE OF IR
     STA   A DUH       ;LOAD INTO MSBYTE OF IR (DUMMY DATA)
     LDA   A #4        ;4 = "SETUP" START ADDRESS
     STA   A XEQ       ;EXECUTE SETUP
     STA   A RST       ;RESET S2815
     STA   A BLK       ;PUT S2815 INTO BLK WRITE MODE
     LDX     OFFST     ;LOAD DATA START ADDRESS INTO IX.REG.
     LDA   A 0,X       ;READ FIRST A
     STA   A DUH       ;LOAD INTO MSBYTE OF IR
     LDA   A 1,X       ;READ SECOND A
     STA   A DUH       ;LOAD INTO MSBYTE OF IR
     STA   A RST       ;RESET S2815.EXIT BLK MODE
     LDA   A #1        ;1 = PRESET FOR S2815 IX,ALSO "INIT" START ADDRESS
     STA   A DUH       ;LOAD INTO MSBYTE OF IR
     STA   A XEQ       ;EXECUTE INIT
     STA   A BLK       ;PUT S2815 INTO BLK WRITE MODE
     LDA   A 2,X       ;READ FIRST B
     STA   A DUH       ;LOAD INTO MSBYTE OF IR
     LDA   A 3,X       ;READ SECOND B
     STA   A DUH       ;LOAD INTO MSBYTE OF IR
     STA   A RST       ;RESET S2815.EXIT BLK MODE
```

```
LDA    A #$80      ;$80 = "BMPY" START ADDRESS
STA    A XEQ       ;EXECUTE BMPY
WAI                ;WAIT FOR INTERRUPT
STA    A RST       ;START OF INTERRUPT ROUTINE.RESET S2815
LDA    A #3        ;3 = PRESET FOR S2815 IX
STA    A DUH       ;LOAD INTO MSBYTE OF IR
LDA    A #1        ;1 = "INIT" START ADDRESS
STA    A XEQ       ;EXECUTE INIT
LDA    A BLK       ;PUT S2815 INTO BLK READ MODE
LDA    A DUH       ;READ FIRST PRODUCT
STA    A 4,X       ;STORE IN MEMORY
LDA    A DUH       ;READ SECOND PRODUCT
STA    A 5,X       ;STORE IN MEMORY
STA    A RST       ;RESET S2815.EXIT BLK MODE

where:     RST  EQU  $HHH1
           DLH  EQU  $HHH3
           DUH  EQU  1HHH2
           XEQ  EQU  $HHH4
           BLK  EQU  $HHH9
```

This program is intended to be instructional rather than practical, since the multiplication of such small arrays of 8 bit numbers can be done more effectively by other means, e.g., using a 6809 microprocessor. However, the extremely fast multiplication time of the S2815 makes this an effective way of dealing with large arrays.

10. Recursive (IIR) Digital Filter Routine IIR1. Entry address $87

This routine executes a number of biquadratic filter sections in cascade. The number of sections can be 1-16. The routine takes its input data from, and returns the output data to, Scratchpad 0. Each filter section occupies 2 bases of RAM in the data memory, with successive filter sections mapped into sequential base pairs as shown in Table 5. In order to be able to use this routine in conjunction with others, e.g., a transversal filter routine, it is possible to set the start base to any value, provided that enough space is left for the other filter sections, i.e., start base (Max.)= 32−2x (number of filter sections), e.g., for a 8th order filter (4 sections) start base (Max)=32 −8=24 ($18).

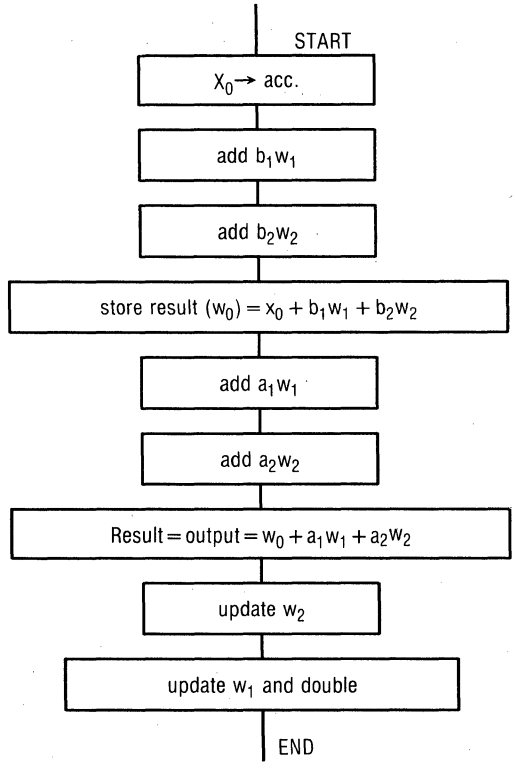
The data for the start base (bits 15-11) and (number of sections −1) (bits 8-4) is stored in S(7), and the exit transfer address is stored in S(4). These should be loaded using the SETUP routine, and the filter coefficients loaded using block transfer. Due to the algorithm used ALL FILTER COEFFICIENTS MUST BE HALVED BEFORE LOADING. This allows filter coefficients in the range ±2 to be used with purely fractional arithmetic.

Table 5. Memory Map and Flow Chart for IIR1 and IIR2 Routines

DISPLACEMENT →		0	1	2	3
BASE	B	$-\frac{1}{2}b_2(1)$	$\frac{1}{2}a_2(1)$	$2w_2(1)$	X
↓	B+1	$-\frac{1}{2}b_1(1)$	$\frac{1}{2}a_1(1)$	$2w_1(1)$	X
	B+2	$-\frac{1}{2}b_2(2)$	$\frac{1}{2}a_2(2)$	$2w_2(2)$	X
	B+3	$-\frac{1}{2}b_1(2)$	$\frac{1}{2}a_1(2)$	$2w_1(2)$	X
	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮
	⋮	⋮	⋮	⋮	⋮

NOTE: (1), (2) . . . . . means data for filter section 1, 2, etc.

Table 5. (Continued)



The algorithm. The basic algorithm used is the canonic form of biquadric difference equation:

$$w_0 = x_0 + b_1w_1 + b_2w_2$$

$$y_0 = w_0 + a_1w_1 + a_2w_2$$

where x_0 = the new input sample (Nth)

w_0 = the new intermediate output (Nth)

w_1 = the previous intermediate output (N-1th)

w_2 = The second previous intermediate output (N-2th)

y_0 = new section output (Nth)

Thus the transfer function is:

$$H(z) = \frac{1 + a_1z^{-1} + a_2a^{-2}}{1 - b_1z^{-1} - b_2z^{-2}}$$

Note the signs of the denominator co-efficients (b_1 and b_2).

Since coefficients a_1 and b_1 can lie in the range ± 2 it is necessary to perform some scaling to fit them into the fractional arithmetic of the S2815. The scheme used is: halve all coefficients and double all stored data, as shown in Table 5. Thus, all products of coefficients and data remain unchanged. This does, of course, have implications on the dynamic range of the system, since the signal levels throughout the system must be 6dB lower than would be possible

otherwise, in order to avoid overflow when the data is doubled. Note that the system normally operates with saturation arithmetic, since the SOP mode is automatically set. The user can change this by setting the COP mode from the control processor. However, instability may occur after overflow when operating in this mode. As with any digital filter, care must be taken with the gains that occur in most types of filters, especially in high Q sections. The optimum sequencing of both the numerators and the denominators of the transfer function polynomial is crucial to realize the maximum dynamic range of the system.

The use of this routine, including the host processor program, is illustrated in an applications example later in this Product Description. The execution time is 12 N+ 3 instruction cycles per sample (3.6N + 0.9μsec) for an N section filter.

11. Recursive (IIR) Digital Filter Routine IIR2. Entry Address $96, $97 or $98

The function of this routine is similar to that of IIR1. The only differences are that a data input routine (equivalent to using LINIP) is available at the start, and the parameters and exit transfer address are stored in S(6) and S(5) respectively. Entering the routine at address $96 provides the "wait for new input" function, and entering at address $97 bypasses this feature (see description of LINIP routine). Entering at address $98 bypasses the input function altogether, and the input data will be taken from S(0), as with IIR1. The 2 recursive filter routines may be used together by mapping their data into different areas of the RAM, by using different start bases. The maximum total number of filter sections (shared between the 2 routines) remains at 16. By using the input function built into IIR2 and using LINIP to load data into IIR1, and by using separate output routines (LINO1 and LINO2), it is possible to process two completely independent signals simultaneously, as long as they have the same sampling frequency. A typical routine sequence (in a closed loop function) would be LINIP→IIR1→LINO1→IIR2→LINO2→back to LINIP. The execution time is 12N+3 instruction cycles per sample (3.6N+0.9μsec) for an N section filter (as for IIR1) when entering at address $98, and 2 or 1 instruction cycles longer when entering at address $96 or $97 respectively.

12. Transversal (FIR) Digital Filter Routine FIR1. Entry Address $A7

This routine executes a transversal (non-recursive, or FIR) filter function with 1-32 taps. The routine takes its input data from, and returns the output data to, scratchpad 0. The memory map for this routine (and for routine FIR2) is shown in Table 6. The data starts at base 0 at all times. The coefficients should be loaded using block transfer and the (number of taps −1) data is stored in S(7) (bits 8-4). The exit transfer address is stored in S(5). The two scratchpad locations should be loaded using the SETUP routine.

Table 6. Memory Map FIR1 and FIR2 Routines

DISPLACEMENT		0	1	2	3
BASE	00	a_0	a_0	x_0	x_0
	01	a_1	a_1	x_1	x_1
	02	a_2	a_2	x_2	x_2
	03	a_3	a_3	x_3	x_3
	⋮	⋮	⋮	⋮	⋮

Data for FIR1 Routine — Data for FIR2 Routine

Note: Scratch pads 1 and 6 are also used for routine to routine transfer when the filters are concatenated.

The algorithm. The algorithm used is straightforward. It computes the sum of products

$$y_0 = a_0x_0 + a_1x_1 + a_2x_2 \ldots\ldots a_{N-1}x_{N-1}$$

where the x_i are input data samples in reverse chronological order, i.e., x_0 is the new input sample, x_{N-1} the oldest remaining in the storage register. The computation sequence is left to right, i.e., a_0x_0 first, then add a_1x_1, etc. Care must be taken to avoid overflow due to the system gain. The execution time for an N tap filter is N + 7 instruction cycles. (0.3N + 2.1μsec.) e.g. a 32 tap filter will be executed in 39 cycles, 11.7μsec.

13. Transversal (FIR) Digital Filter Routine FIR2. Entry Address $AF, $B0, or $B1

This routine is very similar to FIR1 except that a data input routine (equivalent to using LINIP) is available at the start; and the exit transfer address is stored in S(4). It is possible to operate both FIR filter routines concurrently, since they use mutually exclusive RAM locations for their signal and coefficient data, as shown in Table 6. However, since both routines use S(7) to store the data for the number of taps in the filters, they are constrained to be equal in length. This is not a problem in practice since one filter may easily be made shorter than the other by using coefficient values of zero for the unwanted taps. Note that if entry addresses $AF or $B0 are used for FIR2 then this routine executes an independent filter function, with separate input and output from FIR1, but if entry address $B1 is used then the routine is automatically appended to FIR1 to extend the length of the filter, up to a maximum of 64 taps. This occurs because the last tap data in FIR1 is loaded into the first tap position of FIR2 in the next sample period. However, the output data of the 2 routines are still treated separately. They must be read out with separate output routines (LINO1 and LINO2) and summed by the control processor to give the total sum of products for the whole filter. A typical routine sequence (In a closed loop function) for using FIR1 and FIR2 would be

LINIP→FIR1→LINO1→FIR2→LINO2→back to LINIP

If FIR2 is entered at addresses $AF or $B0 then this will execute 2 independent filters of the same length with separate I/O. If FIR2 is entered at $B1 then the function becomes a single double length filter with a single input and 2 outputs which must be summed externally.

The execution time of FIR2 is N+10 instruction cycles per sample (0.3N+3.0μsec) for an N tap filter when entering at address $B1, and 2 or 1 instruction cycles longer when entering at addresses $AF or $B0.

14. Rectifier Routine, RECT. Entry Address $BC

This routine gives the absolute value of the input data, so that in analog terms it acts as a perfect full wave rectifier. It will usually be used with the routine FINT. It takes its input from, and returns the output to S(0), and the exit transfer address is stored in RAM $1F.2 using the SETUP routine. The execution time is 3 instruction cycles (0.9μsec).

15. Squaring Routine, SQUAR. Entry Address $BF

This routine squares the input data, so that in analog terms the output is representative of the power level of the signal. When used with the FINT routine the result will be the mean square signal level. It takes its input from, and returns the output to, S(0), and the exit transfer address is stored in RAM $1F.2 using the SETUP routine. The execution time is 5 instruction cycles. (1.5μsec.)

16. First Order Integrator Routine, FINT. Entry Address $C4

This routine executes a first order recursive filter function, and although it is intended to be used as an integrator, it will equally act as a high or low pass filter. The function will be dependent on the coefficient b_1 used in the algorithm.

$$y_0 = x_0 + b_1 y_1$$

giving the transfer function

$$H(z) = \frac{1}{1 - b_1 z^{-1}}$$

When $b_1 = +1$ the system becomes a perfect, i.e., zero leakage, or infinite time constant, integrator. This is not quite attainable in practice since the maximum possible value of b_1 is $7FF0. (The last hexad is a zero not F, because the coefficient is truncated to 12 bits at the multiplier input.) This is equivalent to a decimal value of 0.9995. The coefficient b_1 is stored in RAM location $1F.1 using block transfer, and the exit transfer address is stored in RAM $1F.0 using the SETUP routine. The execution time is 6 instruction cycles (1.8μsec.).

17. Rectify and Integrate Routine, RINT. Entry address $CA

This routine is equivalent to a combination of RECT and FINT. The coefficient b_1 is stored in RAM location $1D.1 using block transfer, and the exit transfer address is stored in RAM $1E.0 using the SETUP routine. The execution time is 8 instruction cycles (2.4μsec.) making it 1 cycle faster than using RECT and FINT.

18. Square and Integrate Routine, SQINT. Entry Address $CE

This routine is equivalent to a combination of SQUAR and FINT. The coefficient b_1 is stored in RAM location $1D.1 using block transfer, and the exit transfer address is stored in RAM $1E.0 using the SETUP routine. The execution time is 8 instruction cycles (2.4μsec.) making it 3 cycles faster than using SQUAR and FINT.

19. Sine Generator Routine, SINE. Entry address $D6

This routine computes the sine of the input angle. The input data is required in the form of ω/π so that input data varying from −1 to +1 will represent angles from $-\pi$ to $+\pi$, covering a full cycle, or rotation. Cosines may be obtained by complementing the angle.

The algorithm. The 2 MSBs of the input angle (B_{15}-B_{14}) denote the quadrant in which angle lies. This information is first extracted and stored. The next 4 bits (B_{13}-B_{10}) are then used to address a 16 step sine/cosine lookup table, giving 64 values for the quantized angle in the 4 quadrants. The remaining bits are then used to interpolate between these 64 values, using the relationship:

$$\sin(A+\delta)=\sin A\cos\delta+\cos A\sin\delta$$

and the approximations $\cos\delta \rightarrow 1$ and $\sin\delta \rightarrow \delta$ } for small values of δ

giving $\sin(A+\delta)=\sin A+\delta\cos A$

Since $\delta < 6°$ (360/64) the maximum error in the approximation is 0.5% so that the result is correct to approximately 9 bits, including the sign. The routine takes its input from, and returns the output to, S(0), so that it may be used as data either for an output routine or as an input for one of the other computational routines. The execution time of the routine is 15 instruction cycles (4.5μsec.).

20. Noise Generator Setup Routine, NSET. Entry Address $E5

This routine sets up a non-zero starting value in the RAM location used as the register for the PRBS in the NOISE routine, and also allows the user to set a scaling factor for the output level of the noise. The peak level of the noise is equal to the scale factor used. A 6800 control program to execute this function is shown below:

```
LDA   A #SCALE    ;FETCH SCALE FACTOR
STA   A DUH       ;LOAD INTO IR (MSBYTE)
STA   A XEQ       ;EXECUTE NSET

where:    DUH   EQU   $HHH2
          XEQ   EQU   $HHH4
```

and SCALE is the desired scale factor in the range $00 to $7F. It is assumed that 8 bit precision is sufficient for the scale factor, but a 12 bit scale factor may be used if desired. The execution time of the routine is 4 instruction cycles (1.2μsec.) and the routine returns to the idle state after execution.

21. Noise Generator Routine, NOISE. Entry Address $E9

This routine generates a pseudo-random-binary-sequence of length 32767 cycles ($2^{15}-1$) using a 15 bit shift register with linear (exclusive - OR) feedback from the last 2 bits. The register is actually RAM location $1D.0, so that the result is that a pseudo-random number in the range $0001 to $7FFF is generated in this address. The value is then offset by $4000 to make the range symmetrical about zero (to eliminate the D.C. component) and doubled, making the new range $FFFE to $7FFE. It is then multiplied by the scaling factor loaded using the NSET routine, so that any peak value may be obtained. The output is loaded into S(0), so that it may be used as data either for an output routine or as an input for one of the other computational routines. The execution time of the routine randomly varies from 16 to 17 instruction cycles (4.8 - 5.1μsec.), with a mean time of 16.5 cycles over the entire sequence.

Cascading the Routines to Perform Functions

In order to perform a real function with the S2815 it is necessary to cascade a number of routines by setting up the appropriate exit transfer addresses to cause each routine to jump to the entry address of the next. The complete se-

quence may be open ended, jumping to the idle state after executing the final routine, or closed loop, jumping back to the entry address of the first routine after executing the last. A sequence will usually consist of an input/generation routine, followed by a chain of computational routines, ending in an output routine. This is explained in more detail in the examples.

Compatibility and Mutual Exclusivity of Routines

Since some routines share common storage locations for their exit transfer addresses, they are generally incompatible, or mutually exclusive, e.g., the two input routines LINIP and MULIP both use S(2) to store their exit transfer addresses, and consequently the function executed will be identical after exit from either of these two routines. In a closed loop situation, therefore, the function will always return to the same input routine after completion of the cycle, so that the other input routine becomes redundant. However, it is very unlikely that a situation would arise where both input routines would be required within the same closed loop program, so that this mutual exclusivity is very unlikely to be a problem.

The reason for using common exit transfer address storage locations is to reduce the memory requirement for this function, so as to make more memory available for the computational routines, such as the IIR and FIR routines. It will be found that in most cases no conflict will occur since the storage locations have been allocated in such a way as to minimize the mutual exclusivity of routines that are likely to be used together.

Another factor that can cause unwanted interaction between routines is common allocation of addresses for coefficients and/or data used internally in routines. In some cases this data is only stored temporarily in these locations and it is not necessary to preserve these data from one sample period to the next, however, in other cases this is not so. A good example is the use of scratchpads 1 and 6 in the FIR2 routine. These are always used (and overwritten) during the execution of this routine, but are only used for sample to sample data storage if this routine is used to extend the length of a filter with FIR1 i.e., by entering at address $B1. In the latter case the execution of the routine will be upset if another routine using these scratchpads (e.g., SINE, which uses S(1)) is incorporated in the program sequence. The memory maps for the BMPY, IIR1 & 2, and FIR1 & 2 routines are shown in Tables 4, 5, and 6. The address used in these routines are dynamically allocated according to the requirements e.g., the number of taps in the FIR filters, and care must be taken when using these routines in conjunction with others. A memory map for the locations used by the other routines is shown in Table 7.

Table 7. Memory Map for Routines (except BMPY, IIR and FIR)

SP	0	1	2	3
	I/O DATA (MOST ROUTINES)	T(4, 7, 8, 13, 19) D(13)*	E(3, 4)	E(5, 7)

SP	4	5	6	7
	E(10, 13)	E(11, 12)	P(11)	P(10, 12, 13)

	→DISPLACEMENT			
BASE↓	0	1	2	3
1C.		T(8)		T(8)
1D.	D(21)	T(21) C(17, 18)	C(21)	T(21) D(17, 18)
1E.	E(17, 18, 19, 21)	T(18)	E(6.8)	T(15)
1F.	E(16)	C(16)	E(14, 15)	D(16)

NOTES:

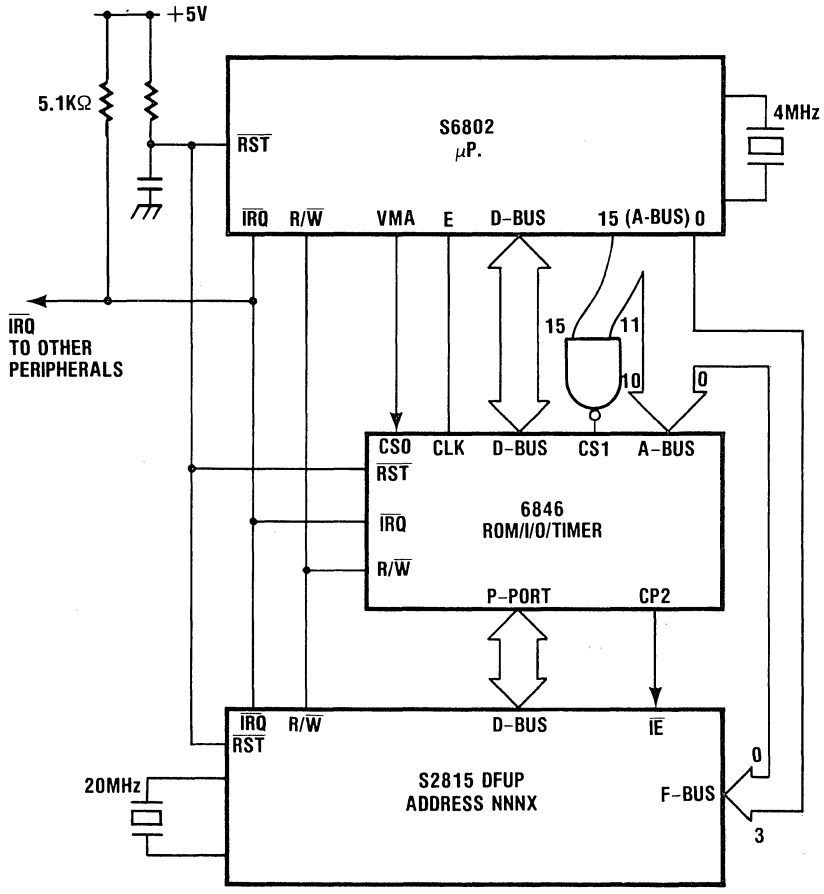
E = EXIT TRANSFER ADDRESS
P = PARAMETERS (BASE REGISTER AND LOOP COUNTER DATA)
C = COEFFICIENT
D = DATA (STORED FROM ONE SAMPLE PERIOD TO NEXT)
T = TEMPORARY DATA (USED ONLY DURING EXECUTION CYCLE)
(n) = ROUTINE NUMBER IN WHICH IT IS USED (see Table 3 for cross-reference to routines)

*ONLY WHEN FIR2 ROUTINE IS ENTERED AT ADDRESS $B1 TO CONCATENATE FILTERS.

Hardware

The minimum hardware for the S2815 is shown in Figure 4. This does not include any provisions for analog interfacing, which is treated in the next section. The S6846 ROM/I/O/TIMER is used to store the S6802 control program and parameters, handle the parallel I/O from the S2815 and generate timing signals, e.g., sampling control. The microprocessor is synchronized to the sampling period by means of the NMI signal generated by the EOC (end of conversion) output of the A to D converter, if necessary. (This is unnecessary when using the serial port of the S2815 to handle the data from the A to D converter.)

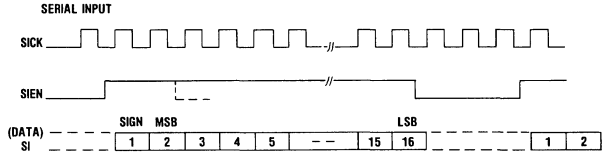
Figure 4. Minimum Hardware Configuration



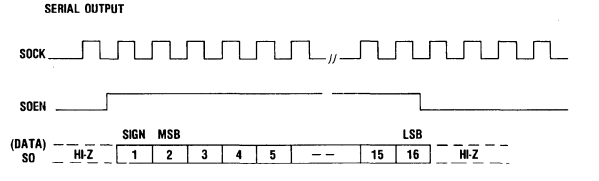
Interfacing to the Serial Port

The serial port allows bidirectional asynchronous interfacing between the S2815 and other devices such as successive approximation A/D converters and PCM Codecs or highways (using the MULIP and MULOP routines). Note that the data is inverted on both input and output. Data is clocked into and out of the S2815 with the serial clocks SICK and SOCK respectively, and gated with the enable lines SIEN and SOEN. The timing is shown in Figure 5.

Figure 5. S2815 Serial Interface Timing



1. SIEN MUST BE SYNCHRONIZED TO THE FALLING EDGE OF SICK SUCH THAT THE RISE AND FALL OF SIEN FOLLOW FALLING EDGE OF SICK.
2. DATA MAY CONTAIN 1 TO 16 BITS DEFINED BY WIDTH OF SIEN. SPP WILL LEFT JUSTIFY DATA WORDS 16 BITS.
3. DATA ARE SAMPLED ON THE TRAILING EDGE OF SICK.
4. MINIMUM 16 SICK PULSES + 64 CYCLES OF S2815 OSCILLATOR ARE REQUIRED BETWEEN SIEN RISING EDGES.
5. IF SERIAL INPUT BUFFER IS FULL, SPP WILL IGNORE NEW INPUT SAMPLES.
6. THE SERIAL DATA IS INVERTED AND MAY BE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.



1. RISE AND FALL OF SOEN MUST FOLLOW FALLING EDGE OF SOCK.
2. OUTPUT DATA WILL BE 1 TO 16 BITS DEFINED BY WIDTH OF SOEN.
3. DATA ARE VALID FROM RISING EDGE TO RISING EDGE OF SOCK SO THAT THE RECEIVING SYSTEM CAN SAMPLE DATA ON TRAILING EDGE.
4. MINIMUM 16 SOCK PULSES + 64 CYCLES OF S2815 OSCILLATOR ARE REQUIRED BETWEEN SOEN RISING EDGES.
5. IF THE SERIAL OUTPUT BUFFER IS EMPTY, ALL ONES WILL BE OUTPUT.
6. SO WILL BE IN A HIGH IMPEDANCE STATE WHEN NOT ENABLED BY SERIAL OUTPUT SEQUENCE.
7. THE SERIAL DATA IS INVERTED AND MAYBE EITHER IN SIGN + MAGNITUDE OR TWO'S COMPLEMENT CODE.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S2816

ECHO CANCELLER PROCESSOR (ECP)

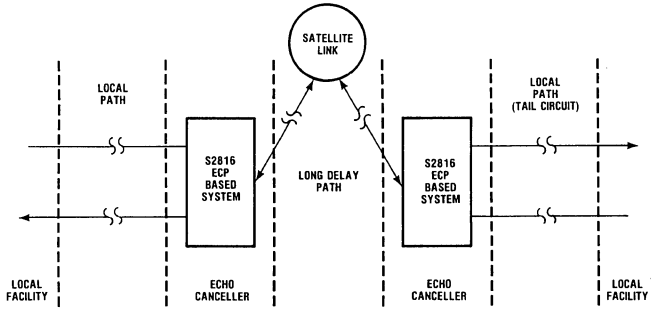
Features

- ☐ S2811 Based System With Echo Canceller Routines
- ☐ Especially Suited to Single-Hop or Double-Hop Satellite and Long Haul Terrestrial Circuits
- ☐ Eliminates Echo Without Signal Degradation
- ☐ Allows Full-Duplex Speech
- ☐ Accommodates Unlimited Long Haul Delays
- ☐ Operates With Local Loop Delays of Up to 25mSec. Expandable in 25mSec Increments Up to 100mSec
- ☐ Cancel Echoes With up to 6mSec Dispersion
- ☐ Convergence Time $<$ 250mSec

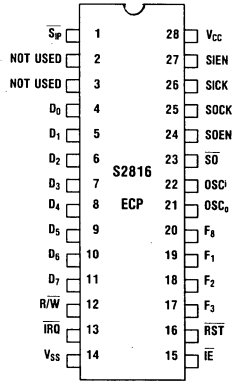
General Description

The AMI S2816 Echo Canceller Processor (ECP) is a pre-programmed version of the S2811 Signal Processing Peripheral. Architectural and internal operating details of the S2811 may be found in the S2811 Advanced Product Description. The S2816 is designed to provide the main echo canceller processing functions in a microprocessor based split-type echo canceller system. Programmed functions provided by the S2816 include μ255 law-to-linear and linear-to-μ255 law I/O conversion, local loop delay estimation, 48-tap auto-equalizing transversal filter, silence detection, and echo canceller performance estimation. This collection of routines allows the S2816 to dynamically eliminate echoes from long distance satellite undersea cable and terrestrial communication systems, employing either analog or digital links.

Typical System Application



Pin Configuration



Echo Canceller Routines

I/O Conversion

The input and output conversion routines are optional routines used when the echo canceller is placed in a PCM data stream, or when the echo canceller is placed in an analog data stream and a codec is used at the interface. The input conversion routine converts μ255 law PCM data to linear data. The output conversion routine converts linear data to μ255 law PCM data.

Local Loop Delay Estimator

The local loop delay estimator is used to determine the delay around the local loop. This information is supplied to the control processor which transfers the received data delayed by this estimate. The maximum local loop delay handling capability of the S2816 is 25.6mSec. May be expanded in 25mSec increments to 100mSec by adding additional memory storage.

Auto-Equalizing Transversal Filter

The auto-equalizing transversal filter is used to model the echo so that it may be subtracted from the signal presented on the long haul side. A 48-tap filter is used to accomplish this task. Echoes with up to 6mSec dispersion may be eliminated by this arrangement.

Silence Detector

The silence detector is used to control the learning rate of the auto-equalizing transversal filter; the silence detector routine calculates the running power average and makes a decision whether the incoming signal is speech or noise. If there is no signal to learn on, or there is a high level interfering signal, learning is suspended.

Echo Canceller Performance Estimator

The Echo Canceller performance estimate, like the silence detector, is used to set the learning rate of the echo canceller. The learning rate of the canceller is set at a level which is proportional to the estimated performance. Performance is based on the ratio of the running averages of the signal before and after cancellation. This ratio is used to control the learning rate of the auto-equalizing transversal filter. Convergence time, for 18dB echo cancellation with a 6dB Echo Return Loss (ERL), is less than 500mSec plus the local loop delay time.

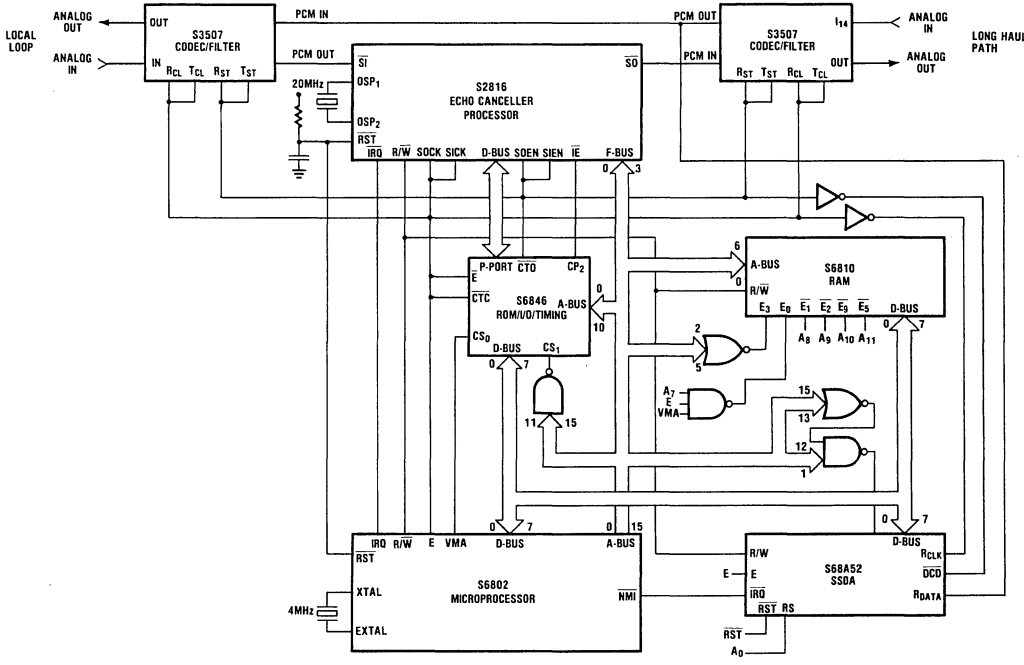
System Application

A proposed echo canceller system based on the S2816 is shown in Figure 2 together with the expected performance specifications. The S3507 codecs provide the required interfacing to the analog data stream. The S68A52 synchronous serial data adapter is used to convert the serial data stream into 8-bit words which can then be loaded into the S6810 RAM. The S6810 is used to store the receive data for a period of time equal to the local loop delay and then loaded into the S2816 for processing. The S6846 ROM-I/O-Timing is used to store the S6802 program, control the I/O between the S6802 and S2816, and provide timing signals required by the codec's. The S2816 performs the echo cancelling routines outlined above. Finally, the S6802 controls and monitors the entire operation.

Typical Echo System Specifications Using the S2816

☐ Echo Return Loss (ERL)	>6dB
☐ Residual Echo (Center Clipping Operating/Echo Suppression at High S/N Ratios)	<−60dBmo
☐ Convergence Time: ERL of 6dB and R_{in} of −10dBmo)	12dB < 250mSec 18dB < 500mSec
☐ Maximum Tail Circuit Delay	25.6mSec (1200 mi. nominal)
☐ Nominal Transmission Levels	+7dBm receive path −16dBm send path
☐ Insertion Loss	0 ±0.5dB, @1004Hz
☐ Frequency Response	±0.5dB, 300-3200Hz Ref. to 1KHz
☐ Harmonic Distortion	<1% for OdBmo test tone @1004Hz
☐ Idle Noise	≤16dBrnco
☐ Envelope Delay Distortion	≤100μSec, 500-3000Hz
☐ Dynamic Range	+3.5 to −60dBmo

System Application



AMERICAN MICROSYSTEMS, INC.

S3501/S3501A, S3502/S3502A

SINGLE CHANNEL μ-LAW PCM CODEC/FILTER SET

Features

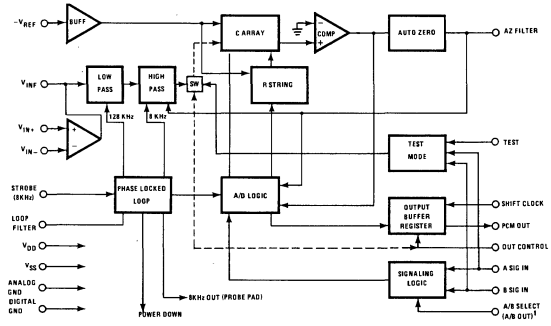
- CMOS Process for Low Power Dissipation
- Full Independent Encoder with Filter and Decoder with Filter Chip Set
- Meets or Exceeds AT&T D3 and CCITT G. 711 and G. 733 Specifications
- On-Chip Dual Bandwidth Phase-Lock Loop Derives All Timing and Provides Automatic Power Down
- Low Absolute Group and Relative Delay Distortion
- Single Negative Polarity Voltage Reference Input
- Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming
- Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate
- Programmable Gain Input/Output Amplifier Stages
- CCIS* Compatible A/B Signaling Option—S3501A/S3502A

General Description

The S3501 and S3502 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM Channel Bank and PBX systems requiring a μ-255 law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the μ-255 law transfer characteristic. Transmission and reception of 8-bit data words containing the analog information is typically performed at 1.544Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line.

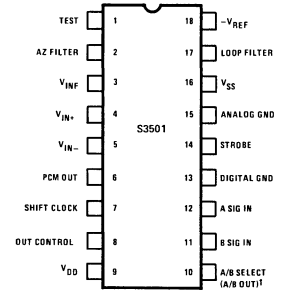
**Common Channel Interoffice Signaling*

S3501 Block Diagram Encoder with Filter



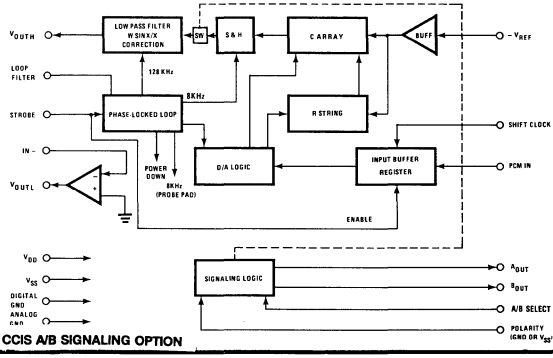
1 CCIS A/B SIGNALING OPTION

Pin Configuration



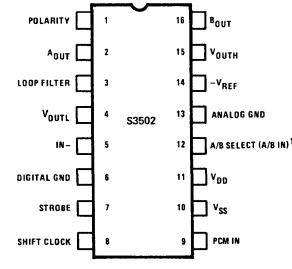
1 CCIS A/B SIGNALING OPTION-S3501A

S3502 Block Diagram Decoder with Filter



CCIS A/B SIGNALING OPTION

Pin Configuration



1 CCIS A/B SIGNALING OPTION-S3502A

S3501 Encoder with Filter Functional Description

S3501 Encoder with Filter chip consists of (1) a bandpass filter with D3 filter characteristic, (2) an analog to digital converter that uses a capacitor array, (3) a phaselock loop that generates all internal timing signals from the externally supplied strobe signal and (4) control logic that performs miscellaneous logic functions.

The band-limiting filter is a 5th order low pass elliptic filter followed by a third order Chebyshev high pass filter. The combined response characteristic (Figure 3) exceeds the D3 filter specifications. Note that the loss below 65Hz is at least 25dB which helps minimize the effect of power frequency induced noise.

The analog to digital converter utilizes a capacitor array based on charge redistribution technique (Ref. 1) to perform the analog to digital conversion with a μ-255 law transfer characteristic (see Figure 4).

The timing signals required for the band-pass filter (128kHz and 8kHz) and analog to digital converter (1.024MHz) are generated by a phase-lock loop comprising a VCO, a frequency divider, a loop filter and a lock detector. The loop locks to the externally supplied 8kHz strobe pulses. In the absence of the strobe pulses, the lock detector detects the unlocked condition and forces the device into a power-down mode thereby reducing power dissipation to a minimum. Thus power-down mode is easily implemented by simply gating the strobe pulses "off" when the channel is idle. The lock-up time, when strobe pulses are gated "on", is approximately 20ms. During this time the device outputs an idle code (all 1's) until lock-up is achieved. Note that signaling information is not transmitted during this time.

The control logic implements the loading of the output shift register, gating and shifting of the data word, signaling logic and other miscellaneous functions. A new analog sample is acquired on the rising edge of the strobe pulse. The data word representing the previous analog sample is loaded into the output shift register at this time and shifted out on the positive transitions of the shift clock during the strobe "on" time. (See Figure 1.) The signaling information is latched immediately after the A/B select input makes a transition. The "A" signaling input is selected after a positive transition and the "B"signaling input is selected after a negative transition. Signaling information is transmitted in the eighth bit position (LSB) of the next frame. (See Figures 1 and 2.) In the CCIS compatible A/B signaling option, the A bit is transmitted during the first data bit time. B bit is transmitted during the remaining 7-bit times. (See Figures 1 and 2.)

"All zero" code suppression is provided so that negative input signal values between the decision value numbers 127 and 128 are encoded as "00000010" after signalling insertion has been done.

S3501 Encoder with Filter Pin Function Descriptions

Strobe: (Refer to Figure 1 for timing diagram.) This TTL compatible input is typically driven by a pulse stream of 8kHz rate. Its active state is defined as a logic 1 level and should be active for a duration of 8 clock cycles of the shift clock. A logic "1" initiates the following functions: (1) instructs the device to acquire a new analog sample on the rising edge of the signal (logic 0 to logic 1 transition); (2) instructs the device to output the data word representing the previous analog sample onto the PCM-out pin serially at the shift clock rate during its active state; (3) forces the PCM-out buffer into an active state. A logic "0" forces the PCM-out buffer into a high impedance state if the Out Control pin is wired to V_{DD}. This input provides the sync information to the phase-lock loop from which all internal timing is developed. The absence of the strobe conveys power-down status to the device. (See functional description of the phase-lock loop for details.)

Shift Clock: This TTL compatible input is typically a square wave signal at 1.544MHz. The device can operate with clock rates from 56kHz (as in the single channel 7-bit PCM system) to 3.152MHz (as in the T1-C carrier system). Data is shifted out of the PCM-out buffer on the rising edges of the clock after a valid logic 0 to logic 1 transition of the strobe signal.

PCM-Out: This is an open drain buffer capable of driving one low power Schottky (74LS) TTL load with a suitable external pull-up resistor (1kΩ). This buffer is in active state (as controlled by the value of the data bit) whenever the strobe signal is a logic 1 and is in a high impedance state when the strobe input is a logic 0 and if the out control pin is wired to V_{DD} supply. When the out control is wired to V_{SS} the state of the output buffer is controlled by the value of the data bit being shifted out. For 56kHz and 64kHz PCM systems where output data is a continuous bit stream, the out control pin should be connected to V_{SS}.

A/B Select: (S3051 only) (Refer to Figure 2 for timing diagram.) This TTL compatible input is provided in order to select the path for the signaling information. It is a transition sensitive input. A positive transition on this input prior to the negative transition of the strobe input selects the "A" signaling input and is transmitted as the eighth bit in the subsequent frame. Similarly, a negative transition causes selection and transmission of informa-

tion on the "B" signaling input. Because it is a transition sensitive input, tying it to V_{DD} or V_{SS} disables A/B signaling.

A SIG IN, B SIG IN: These two TTL compatible inputs are provided to allow multiplexing of signaling information into the transmitted PCM data word in the eighth bit position in accordance with the timing diagram of Figure 2.

A/B Out: (S3501A only.) This is an open drain buffer capable of driving one low power Schottky (74LS) TTL load with a suitable external pull-up resistor 10kΩ). This is an optional output for implementing CCIS compatible A/B signaling. (See Figure 2b.) During data bit 1 time, A signaling bit is output. During remaining 7-bit times, B signaling bit is output. This output is in a high impedance state when strobe is not present.

Out Control: This is a CMOS compatible input and must be wired to either the V_{DD} or V_{SS} (except in 'test' mode). When connected to the V_{SS}, The PCM-out buffer is always in the active state. For continuous analog-to-PCM operation at 56 or 64kb/sec, Out Control should be tied to V_{SS}.

V_{IN-}, V_{IN+}, V_{INF}: These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. V_{IN-} and V_{IN+} are the inputs of a high input impedance op amp and V_{INF} is the output of this op amp. These three pins allow the user complete control over the input stage so that the input stage can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel and testing of the encoder in a stand alone situation. The input stage also allows the user to construct an anti-aliasing filter to provide sufficient suppression at 128kHz. (See Design Considerations on page 13.)

$-V_{REF}$: The input provides the conversion reference for the analog to digital conversion circuit. A value of −3volts is required. The reference must maintain 100ppM/°C regulation over the operating temperature range. A high input impedance buffer is provided on this input which facilitates bussing of the same reference voltage to several devices.

AZ Filter: A capacitor C_{AZ} (nominal .022μF) is required from this pin to analog ground for the functioning of the on-chip auto zero circuit. The most significant bit (sign bit) is filtered by the auto zero circuit and fed back to the input of the A/D converter to compensate for filter output offset variations. This technique insures that the long term average of the sign bit will be zero.

Analog Ground, Digital Ground: Two separate pins are provided for connection of analog signals referenced to analog ground and digital signals referenced to digital ground. This minimizes switching noise associated with the digital signals from affecting the analog signals.

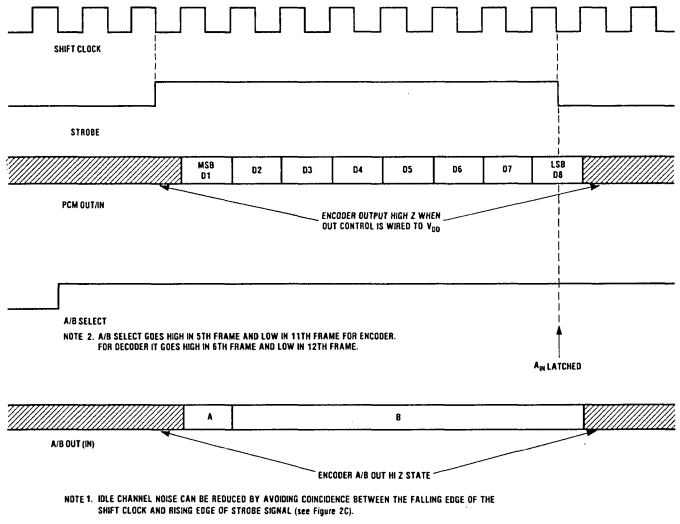
V_{DD}, V_{SS}: These are positive and negative supply pins.

Loop Filter: A capacitor C_{LOOP} (nominal .1μF) is required from this pin to digital ground to provide filtering of the phase comparator output.

Test: This pin is provided to allow for separate testing of the filter and encoder sections of the circuit. The circuit functions normally when this pin is connected to V_{SS}. When this pin is connected to V_{DD}, test mode results. In this mode when A SIG IN and B SIG IN inputs are connected to V_{SS} the filter output is disconnected from the encoder input. The encoder input is connected instead to the Out Control pin. For all other logical combinations of the A SIG IN and B SIG IN inputs the filter output is connected to the Out Control pin.

Ref. 1: *"A Two Chip PCM Voice CODEC with Filters,"* IEEE Journal of Solid State Circuits December 1979.

Figure 1-A. Typical Waveforms in a Time Multiplexed System



NOTE 1. IDLE CHANNEL NOISE CAN BE REDUCED BY AVOIDING COINCIDENCE BETWEEN THE FALLING EDGE OF THE SHIFT CLOCK AND RISING EDGE OF STROBE SIGNAL (see Figure 2C).

Figure 1-B. Waveform Detail

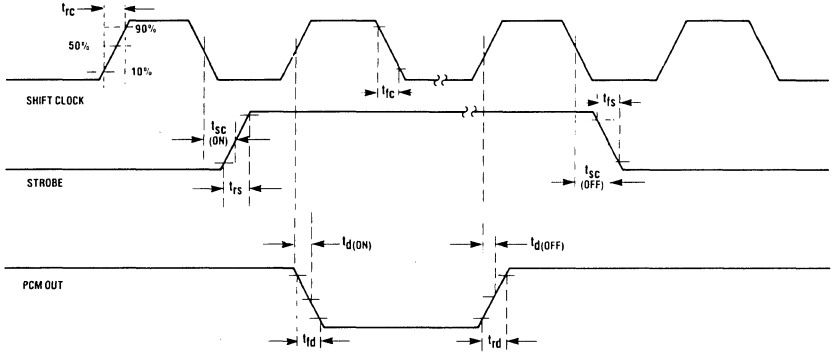
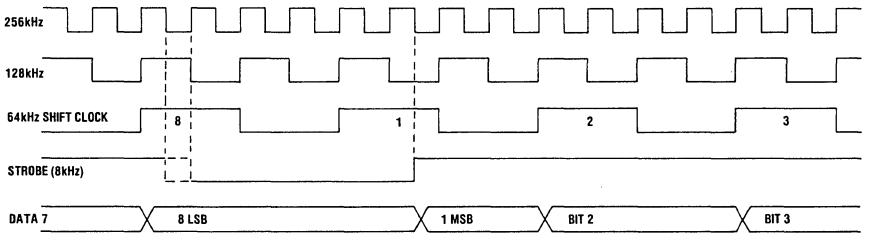


Figure 1-C. 64kHz Continuous Bit Stream Application



NOTES:
1. OUT CONTROL IS WIRED TO V_{SS} FOR CONTINUOUS BIT STREAM OPERATION.
2. THE NEGATIVE TIME OF THE STROBE SHOULD EXCEED ONE SHIFT CLOCK PERIOD.
3. THE CLOCK AND STROBE EDGES SHOULD BE SEPARATED BY AT LEAST 200ns.

Figure 2-A. Encoder A/B Signalling Waveforms

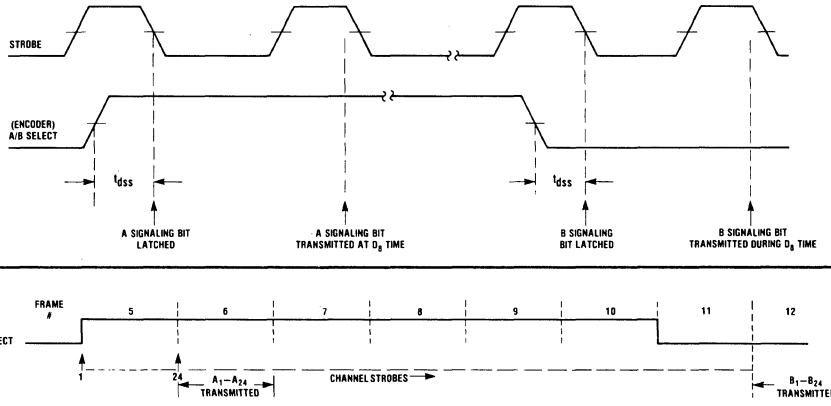


Figure 2-B. CODEC System Timing Diagram

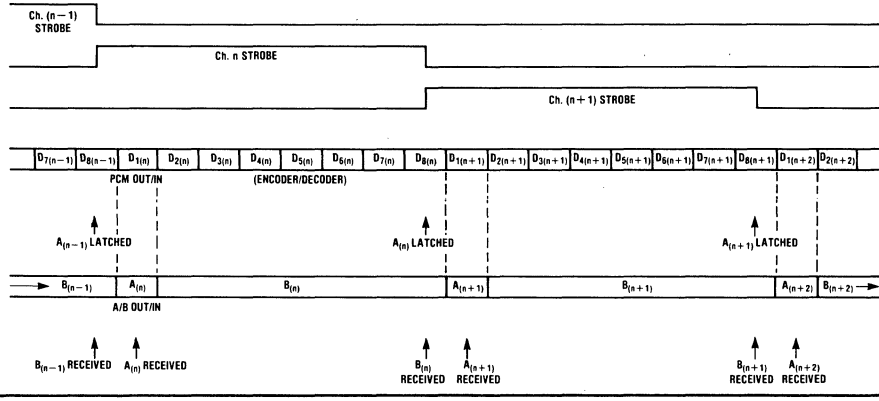
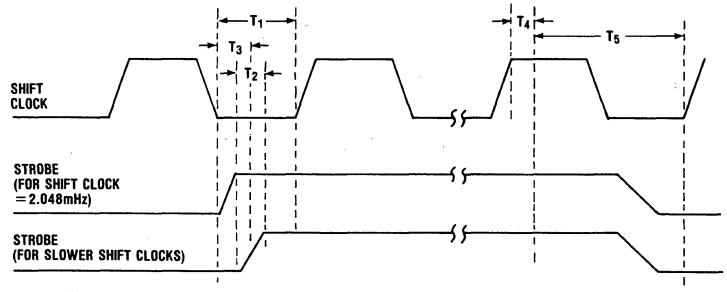


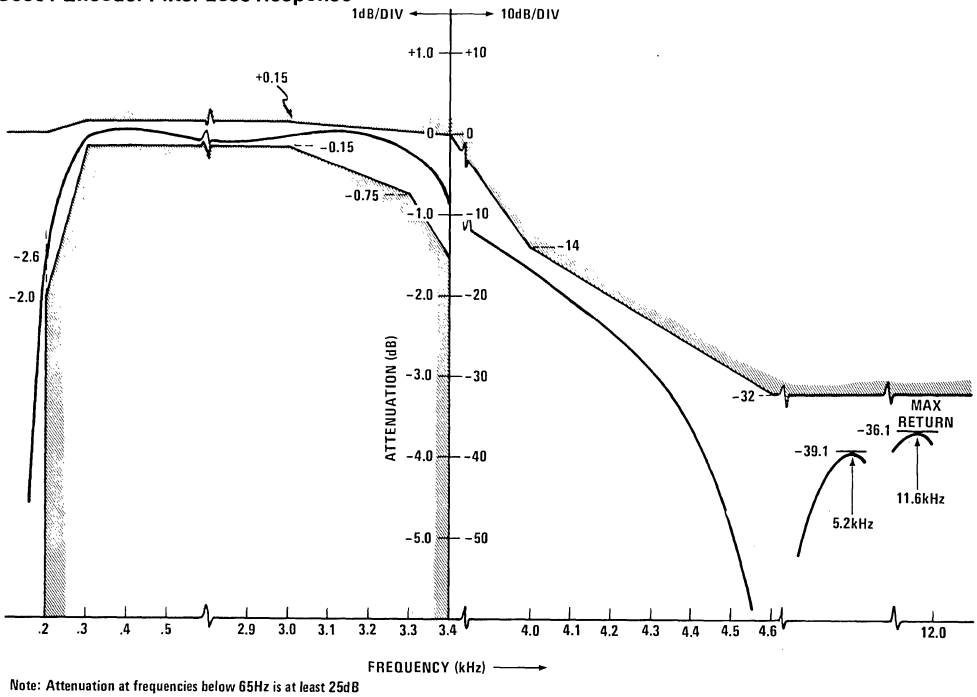
Figure 2-C.



NOTES:

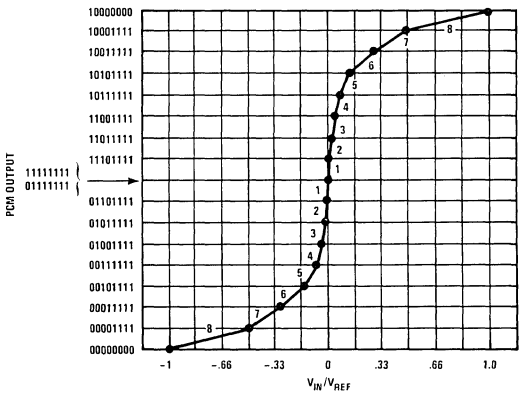
1. THE RISING EDGE OF THE STROBE MUST BE WITH IN T_1 AND THE FALLING EDGE WITHIN T_5. $T_4 = 200ns$ (MIN). FOR A 2.048mHz SHIFT CLOCK, IDLE CHANNEL NOISE WILL BE MINIMIZED IF THE RISING EDGE OF THE STROBE OCCURS IN T_3. $T_3 = 100ns$.
3. FOR SLOWER SHIFT CLOCK RATES, IDLE CHANNEL NOISE IS MINIMIZED IF THE RISING EDGE OCCURS IN T_2. FOR EXAMPLE, T_2 IS 125ns FOR A 1.544mHz SHIFT CLOCK.
4. ADJUSTING THE FALLING EDGE OF THE SHIFT CLOCK WILL NOT AFFECT IDLE CHANNEL NOISE.

Figure 3. S3501 Encoder Filter Loss Response

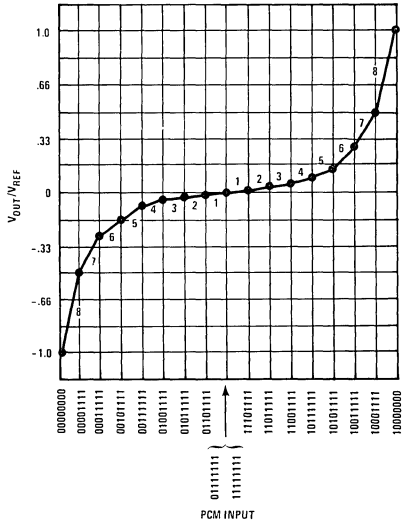


Note: Attenuation at frequencies below 65Hz is at least 25dB

Figure 4. μ-255 Law Transfer Characteristics



S3501 Transfer Characteristics



S3502 Transfer Characteristics

S3501 Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	250mW
Digital Input	$-0.3 \le V_{IN} \le V_{DD} + 0.3$
Analog Input	$-V_{REF} \le V_{IN} \le V_{REF}$
$-V_{REF}$	$V_{SS} \le V_{REF} \le 0$

S3501 Electrical Operating Characteristics ($T_A = 25°C$)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V+	Positive Supply	4.75	5.0	5.25	V	See Figure 7
V−	Negative Suppply	−4.75	−5.0	−5.25	V	
$-V_{REF}$	Negative Reference	−2.4	−3	−3.10	V	
P_{OPR}	Power Dissipation (Operating)		60	100	mW	
P_{STBY}	Power Dissipation (Standby)		15		mW	

S3501 AC Characteristics (Refer to Figures 1 and 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_d (On)	Shift Clock to PCM Out (On) Delay		140	170	ns	1kΩ, 50pF
t_d (Off)	Shift Clock to PCM Out (Off) Delay		140	170	ns	
t_{rd}	PCM Output Rise Time $C_L = 50pF$		100	125	ns	1kΩ Pull-Up on PCM Out selected for desired rise time
t_{fd}	PCM Output Fall Time $C_L = 50pF$		50	70	ns	
t_{dss}	A/B Select to Strobe Trailing Set Up Time	100			ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P−P Jitter of Strobe Rising Edge			5	μs	

S3501 Encoder DC Characteristics (5V Power Supply, $-V_{REF}=-3.0V$ see Figure 9.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance	10			MΩ	V_{IN-}, V_{IN+} Inputs
C_{IN}	Input Capacitance			10	pF	V_{IN-}, V_{IN+},V_{INF} Inputs
I_{INL}	Logic Input Low Current (Shift Clock, Strobe)			1	μA	$V_{IL}=0.8V$
I_{INH}	Logic Input High Current			1	μA	$V_{IH}=2.0V$
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.2			V	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.8	V	$I_{OL}=5mA$
V_{OL}	Logic Output "Low" Voltage (A/B Out)			0.8	V	$I_{OL}=.1mA$
I_{OH}	PCM Output Off Leakage Current			1	μA	$V_O=0$ to 5V

S3501 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input= (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	39		dB	−25
	35	38		dB	−30
	32	35		dB	−35
	29	32		dB	−40
	25	28		dB	−45
Gain Tracking		0±.02	±0.25	dB	−10
		0±0.02	±0.25	dB	−20
		0±0.03	±0.25	dB	−25
		0±0.03	±0.25	dB	−30
		−.02±0.04	±0.25	dB	−35
		−.02±0.06	±0.50	dB	−40
		−.02±0.09	±0.50	dB	−45
		−.02±0.13	±0.50	dB	−50
Idle Channel Noise		12.5	19	dBrncO	Analog Input to Analog GND
Transmission Level Point		5.4		dBm	

S3502 Decoder with Filter Functional Description

S3502 Decoder with Filter consists of (1) a digital to analog converter that uses a capacitor array; (2) a low pass filter with D3 filter characteristic; (3) a phase-lock loop that generates all internal timing signals from the externally supplied strobe signal and (4) control logic that performs miscellaneous logic functions.

The digital to analog converter uses a capacitor array based on charge redistribution technique (Ref. 1) to perform the D/A conversion with a μ-255 law transfer characteristic (See Figure 4).

The timing signals required for the low pass filter (128kHz) digital to analog converter (1.024MHz) are generated by a phase-lock loop comprised of a VCO, a frequency divider, a loop filter and a lock detector. The loop locks to the externally supplied 8kHz strobe pulses. In the absence of the strobe pulses, the lock detector detects the unlocked condition and forces the device into a power-down mode thereby reducing power dissipation to a minimum. Thus, power-down mode is easily implemented by simply gating the strobe pulses "off" when the channel is idle. During the power-down mode the output amplifier is forced to a high impedance state and the A, B outputs are forced to inactive state. The lock-up time, when strobe pulses are gated "on", is approximately 20ms. During this time the A/B outputs and the analog output stage are held in the idle state.

The control logic implements the loading of the input shift register, signaling logic and other miscellaneous functions. A new data word is shifted into the input register on a positive transition of the strobe signal at the shift clock rate. The received data is decoded by the D/A converter and applied to the sample and hold circuit. The output sample and hold circuit is filtered by a low pass filter. The low pass filter is a sixth order elliptic filter. The combined response of the sample and hold and the low pass filter is shown in Figure 5.

Signaling information is received and latched immediately after the A/B select input makes a positive or negative transition. On the positive transition of the A/B select input information received in the eighth bit of the data word is routed to the A_{OUT} pin and latched until updated again after the next positive transition of the A/B select input. Similarly "B" signaling information is routed and latched at the B_{OUT} pin after each negative transition of the A/B select input. The A and B outputs are designed such that either relay or TTL compatibility can be achieved (see detailed description under Pin/Function descriptions). In the CCIS compatible A/B signaling option "A" bit is latched during the data bit 1 time and "B" bit is latched during the data bit 8 time.

S3502 Decoder with Filter Pin/Functions Descriptions

Strobe: (Refer to Figure 1 for timing diagram.) This TTL compatible input is typically driven by a pulse stream of 8kHz rate. Its active state is defined as a logic 1 level and is normally active for a duration of 8 clock cycles of the shift clock. It initiates the following functions: (1) instructs the device to receive a PCM data word serially on PCM IN pin at the shift clock rate; (2) supplies sync information to the phase-lock loop from which all internal timing is generated; (3) conveys power-down mode to the device by its absence. (See functional description of the phase-lock loop for details.)

Shift Clock: This TTL compatible input is typically a square wave signal at 1.544MHz. The device can operate with clock rates from 56kHz (as in the single channel 7-bit PCM system) to 3.152MHz (as in the T1-C carrier system). Data is shifted in the PCM IN buffer on the falling edges of the clock after the strobe signal makes a logic 0 to logic 1 transition.

PCM IN: This is a TTL compatible input on which time multiplexed PCM data is received serially at the shift clock rate during the active state of the strobe signal.

A/B Select: (Refer to Figure 6 for timing diagram.) This TTL compatible input is provided in order to select the path for the signaling information. It is a transition sensitive input. A positive transition on this input routes the received signaling bit to the "A" output and a negative transition routes it to the "B" output.

A Out, B Out: These two open drain outputs are provided to output received signaling information. These outputs are designed in such a way that either LS TTL or relay drive compatibility can be achieved. With a suitable pull-up resistor (47KΩ) connected to the LS TTL logic supply, the output voltage will swing between digital ground and the LS TTL logic supply when the Polarity pin is connected to digital ground. (See Figure 6.) The output polarity is the same as the received signaling bit polarity. If the Polarity pin is connected to the V_{SS} supply, the output voltage will swing between V_{SS} and V_{DD} supplies with a suitable pull-up resistor. This facilitates driving a relay by a PNP emitter grounded transistor in -48V systems. The output polarities are inverted from the received signaling bit polarity to facilitate relay driving.

Polarity: This pin is provided for testing purposes and for controlling the A/B output polarities and TTL/relay drive

compatibilities. For TTL compatibility this pin is connected to digital ground. The A/B output polarities are then the same as the received signaling bit polarities. For relay drive capability this pin is connected to the V_{SS} supply. The A/B output polarities then are inverted from the received signaling bit polarities. Test mode results when this pin is connected to V_{DD}. In this mode the decoder output (S&H output) is connected to the B-Out pin while the filter input is connected to the A-Out pin.

$-V_{REF}$: The input provides the conversion reference for the digital to analog conversion circuit and the phase-lock loop. The reference must maintain 100ppM/°C regulation over the operating temperature range. A high input impedance buffer is provided on this input which facilitates bussing of the same reference voltage to several devices.

V_{OUTH}: This is the output of the low pass filter which represents the recreated voice signal from the received PCM data words. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance.

V_{OUTL}, IN−: These two pins are the output and input of the uncommitted output amplifier stage. Signal at the V_{OUTH} pin can be connected to this amplifier to realize a low output impedance with the unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel and testing of the decoder in a stand alone situation.

Analog Ground, Digital Ground: Two separate pins are provided for connection of analog signals referenced to analog ground and digital signals referenced to digital ground. This minimizes switching noise associated with the digital signals from affecting the analog signals.

V_{DD}, V_{SS}: These are the positive and negative power supply pins.

Loop Filter: A capacitor C_{LOOP} (nominal .1μF) is required from this pin to digital ground to provide filtering of the phase comparator output.

A/B IN: (S3502A only) This optional TTL compatible input is provided to implement CCIS compatible A/B signaling scheme.Time multiplexed A, B signaling information is applied at this input and recovered by the decoder as shown in Figure 2-b.

Figure 5. S3502 Decoder Filter with Sample & Hold Loss Response

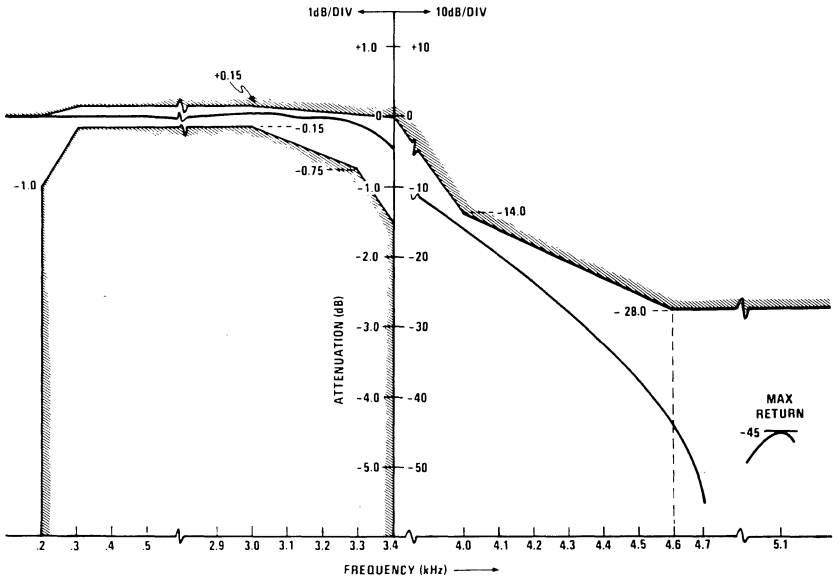


Figure 6-A. Waveform Detail

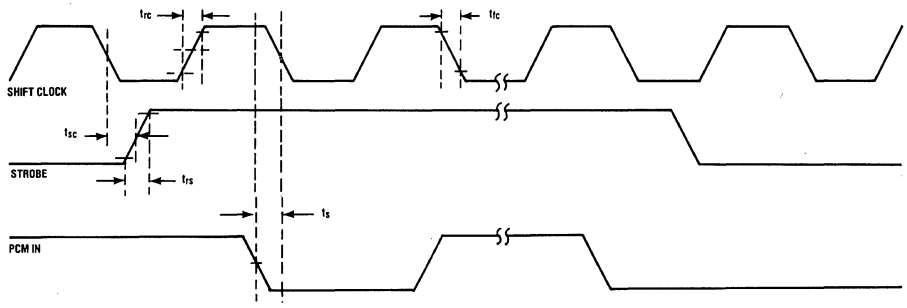
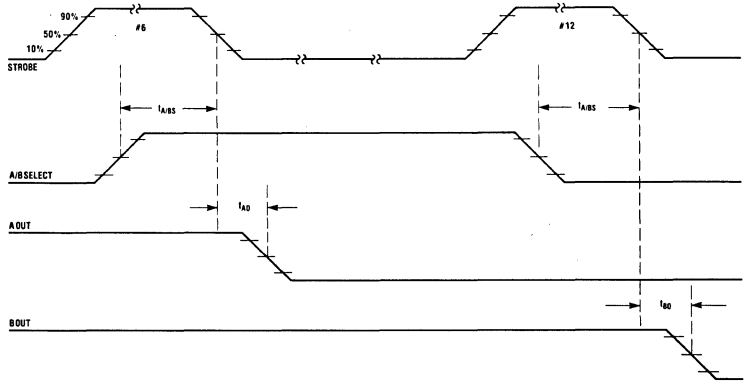


Figure 6-B. Decoder A/B Output Timing



S3502 Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	250mW
Digital Input	$-0.3 \leq V_{IN} \leq V_{DD} + 0.3$
Analog Input	$-V_{REF} \leq V_{IN} \leq V_{REF}$
$-V_{REF}$	$V_{SS} \leq V_{REF} \leq 0$

S3502 Electrical Operating Characteristics ($T_A = 25°C$)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V+	Positive Supply	4.75	5.0	5.25	V	See Figure 11
V−	Negative Supply	−4.75	−5.0	−5.25	V	
$-V_{REF}$	Negative Reference	−2.4	−3	−3.1	V	
P_{OPR}	Power Dissipation (Operating)		60	100	mW	
P_{STBY}	Power Dissipation (Standby)		15		mW	

S3502 AC Characteristics (Refer to Figures 1 and 6)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{SC}	Shift Clock Frequency	0.056	1.544	3.152	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}(On)	Shift Clock to Strobe (On) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{sc} (Off)	Shift Clock to Strobe (Off) Delay	0+		(1/2 CP)−	Shift Clock Period	
t_{rd}	PCM Input Rise Time			100	ns	
t_{fd}	PCM Input Fall Time			100	ns	
t_L	Phase-Lock Loop Lock Up Time		20	90	ms	
t_j	P—P Jitter of Strobe Rising Edge			5	μs	
t_s	PCM Input Setup Time	100			ns	
$t_{A/BS}$	A/B Select Set Up Time to Strobe Trailing Edge	100			ns	
t_{AO}, t_{BO}	Strobe Falling Edge to A/B Out Delay			200	ns	

S3502 Decoder DC Characteristics 5V Power Supplies, $-V_{REF}=-3.0V$ (see Figure 11.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$R_L(V_{OUTL})$	Output Load Resistance	600			Ω	
R_{INA}(IN−)	Analog Input Resistance	10			MΩ	
C_{INA}(IN−)	Analog Input Capacitance			10	pF	
I_{REF-}	Negative Reference Current		150	300	nA	
R_{REF-}	Negative Reference Input Resistance	10			MΩ	
V_{IL}	Logic Input (Shift Clock, Strobe, PCM In) "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.2			V	
I_{INL}	Logic Input "Low" Current			1	μA	$V_{IL}=0.8V$
I_{INH}	Logic Input "High" Current			1	μA	$V_{IH}=2.0V$
V_{OL}	A, B Output "Low" Voltage			0.8	V	Polarity=Dig. Gnd, $I_{OL}=1mA$
V_{OL}	A, B Output "Low" Voltage			$V_{SS}+1.0$	V	Polarity=V_{SS}, $I_{OL}=1mA$

S3502 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit	Condition Analog Input= (dBmO)
Signal to Distortion	35	40		dB	0
	35	40		dB	−20
	35	38.5		dB	−25
	35	39		dB	−30
	32	36.5		dB	−35
	29	33.5		dB	−40
	25	29		dB	−45
Gain Tracking		.02±.02	±0.25	dB	−10
		.04±.02	±0.25	dB	−20
		.04±.03	±0.25	dB	−25
		.03±.03	±0.25	dB	−30
		.04±.04	±0.25	dB	−35
		.04±.05	±0.50	dB	−40
		.1±.05	±0.50	dB	−45
		.15±.07	±0.50	dB	−50
Idle Channel Noise		9	13	dBrncO	PCM Input to Analog GND
0 Transmission Level Point (Digital Milliwatt Response)		4.9		dBm	−3V V_{REF} 600Ω Load

S3501/S3502 System Characteristics Typical Group Delay Characteristic

Device	Abs. Gr. Delay μs f = 1000Hz	Abs. Gr. Delay μs f = 2600Hz	Relative Gr. Delay Distortion (Over Band of 1000 Hz to 2600Hz wrt 1000Hz) μs
Encoder Low Pass	132	220	88
Encoder High Pass	104	22	−82
Encoder Total	236	242	6
Decoder Low Pass	153	250	97
Encoder + Decoder (Total)	389	492	103
End to End Group Delay (Encoder Analog Input to Decoder Analog Output)	639	742	103

Design Considerations

Because the Codec set is required to handle signals with a very large dynamic range, optimal analog performance requires careful attention to the layout of components:

The analog ground, digital ground, V_{DD} and V_{SS} busses should run independently to the power supply, or at least to the edge connector. They should be separate for each chip and should be kept as wide as possible on the printed circuit.

The connections should be as independent as possible. For example (see Figure 7), the 750Ω pull-up resistor to Pin 6 should join the V_{DD} supply at the edge connector and not at the device pin.

Decoupling capacitors should be as close as possible to the power supply pin and analog ground pin.

Digital signal lines should be kept away from analog signals, and separated by an analog ground line where possible for shielding.

3501/3501A Design Guidelines

A recommended S3501 schematic is shown in Figure 7. Parts of the circuit are discussed in more detail below.

Loop Filter Network—For shift clock rates above 512kHz the network in Figure 8 is recommended. For 512kHz or below a .1μF capacitor between pins 13 and 17 is sufficient.

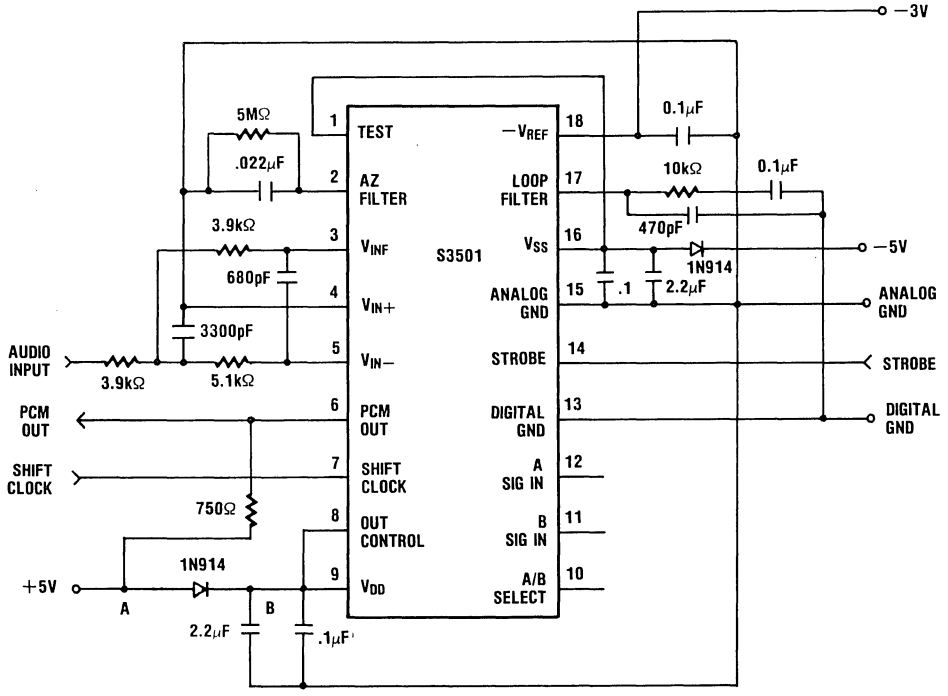
Supply Decoupling—Figure 9 shows the recommended power supply decoupling circuits. The diodes are essential for ±5V power supplies.

Reference Voltage—pin 18, requires a .1μF capacitor to analog ground. Pin 2, AZ filter, requires a .022μF capacitor to analog ground in parallel with 5MΩ resistor.

Anti-Aliasing

In applications where anti-aliasing pre-filtering is required, an on-chip op-amp may be configured into an active filter (Figure 10). Note that small changes in gain can be made by adjusting the resistor ratio R_1/R_2. Where anti-aliasing is not needed, a 3KΩ-4KΩ resistor can be connected between pins 3 and 5 (inverted gain configuration).

Figure 7. Hookup Schematic for S3501 Using 1.544mHz Shift Clock Rate



NOTE: TEST PIN 1 MUST BE CONNECTED TO PIN 16 (NOT −5V) TO PREVENT FORWARD BIASING THE PIN.

Figure 8. Selection of Loop Filter Network

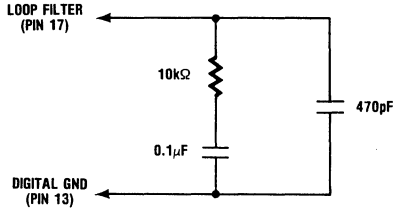


Figure 9-B.
Supply Decoupling for the V_{SS} Supply Pin

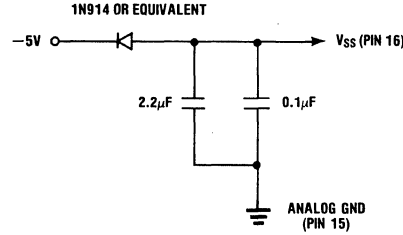


Figure 9-A.
Supply Decoupling for the V_{DD} Supply Pin

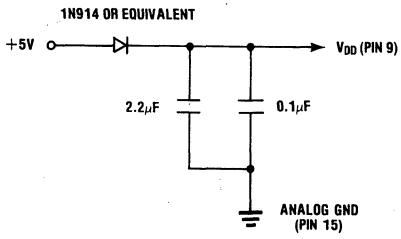
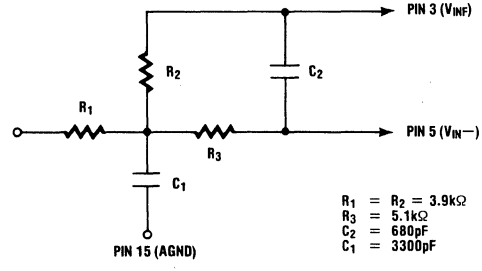


Figure 10. Anti-Aliasing Filter



S3502/S3502A Design Guidelines

Figure 11 depicts a recommended S3502 circuit. All of the following comments apply to Figure 11:

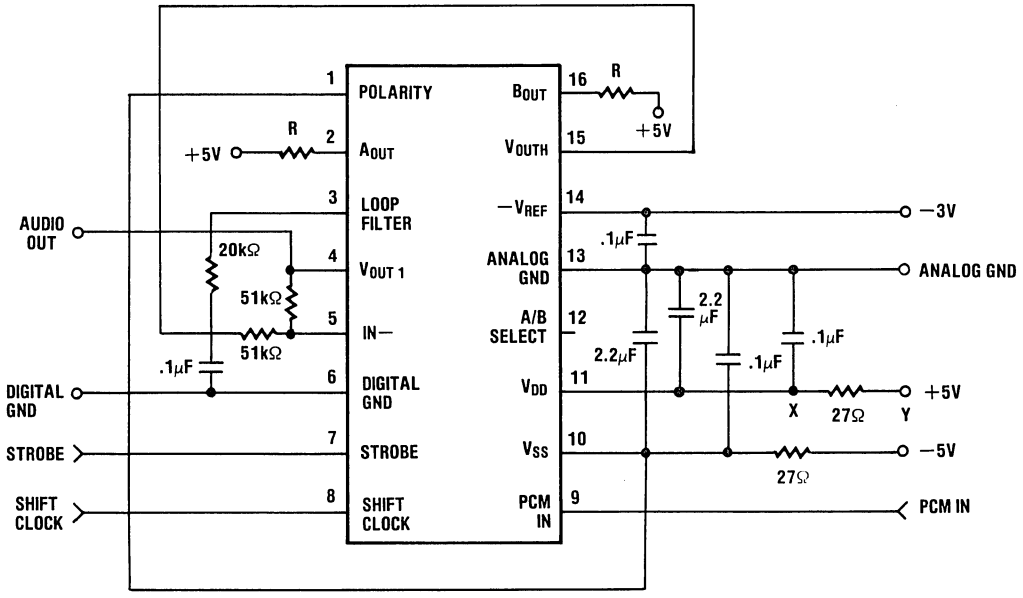
A_{OUT} and B_{OUT} are connected to V_{DD}. R should be larger than 10KΩ to reduce noise.

When pin 1 is connected to DGND (non-inverted signaling with T^2 output levels; not shown in Figure 11), R should be 47KΩ or greater.

Pin 1 should be connected to Pin 10, and not just to −5V, to avoid forward biasing the pin.

The 51KΩ output amplifier resistors should be carefully positioned away from the digital signals.

Figure 11. Hookup Schematic for S3502 Using 1.544mHz Shift Clock Rate



AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3503/S3504

SINGLE CHANNEL A-LAW PCM CODEC/FILTER SET

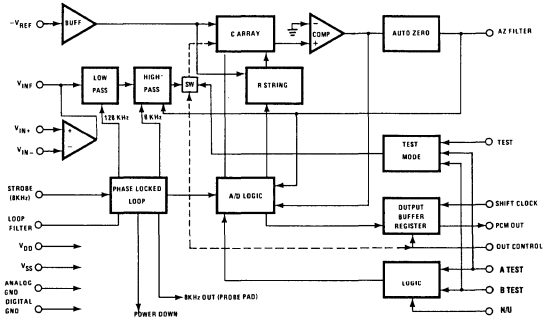
Features

- ☐ CMOS Process for Low Power Dissipation
- ☐ Full Independent Encoder with Filter and Decoder with Filter Chip Set
- ☐ Meets or Exceeds CCITT G.711, G.712 and G.733 Specifications
- ☐ On-Chip Dual Bandwidth Phase-Lock Loop Derives All Timing and Provides Automatic Power Down
- ☐ Low Absolute Group and Relative Delay Distortion
- ☐ Single Negative Polarity Voltage Reference Input
- ☐ Encoder with Filter Chip Has Built-In Dual Speed Auto Zero Circuit with Rapid Acquisition During Power Up that Eliminates Long Term Drift Errors and Need for Trimming
- ☐ Serial Data Rates from 56kb/s to 3.152Mb/s at 8kHz Nominal Sampling Rate
- ☐ Programmable Gain Input/Output Amplifier Stages

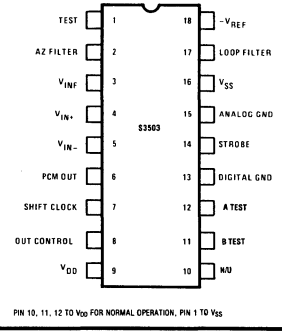
General Description

The S3503 and S3504 form a monolithic CMOS Companding Encoder/Decoder chip set designed to implement the per channel voice frequency CODECS used in PCM systems requiring an A-law transfer characteristic. Each chip contains two sections: (1) a band-limiting filter, and (2) an analog ↔ digital conversion circuit that conforms to the A-law transfer characteristic. Typical transmission and reception of 8-bit data words containing the analog information is performed at 2.048Mb/s rate with analog sampling occurring at 8kHz rate. A strobe input is provided for synchronizing the transmission and reception of time multiplexed PCM information of several channels over a single transmission line. These chips are pin-for-pin replacements for the S3501/S3502 chip set with the exception of the A-law transfer characteristic conforming to CCITT G.711 and the unused sigaling capability which remains available for special applications.

S3503 Block Diagram Encoder With Filter

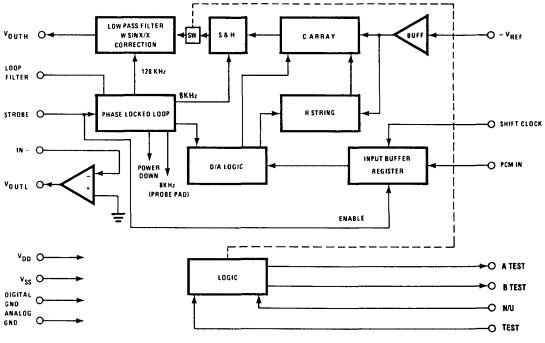


Pin Configuration

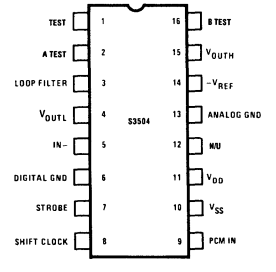


PIN 10, 11, 12 TO V_{DD} FOR NORMAL OPERATION. PIN 1 TO V_{SS}

S3504 Block Diagram Decoder with Filter



Pin Configuration



PIN 1 TO DIGITAL GROUND, PIN 2, 16 OPEN FOR NORMAL OPERATION

AMERICAN MICROSYSTEMS, INC.

PRELIMINARY DATA SHEET

S3506/S3507/S3507A

CMOS SINGLE CHIP μ-LAW/A-LAW COMBO CODECS WITH FILTERS

Features

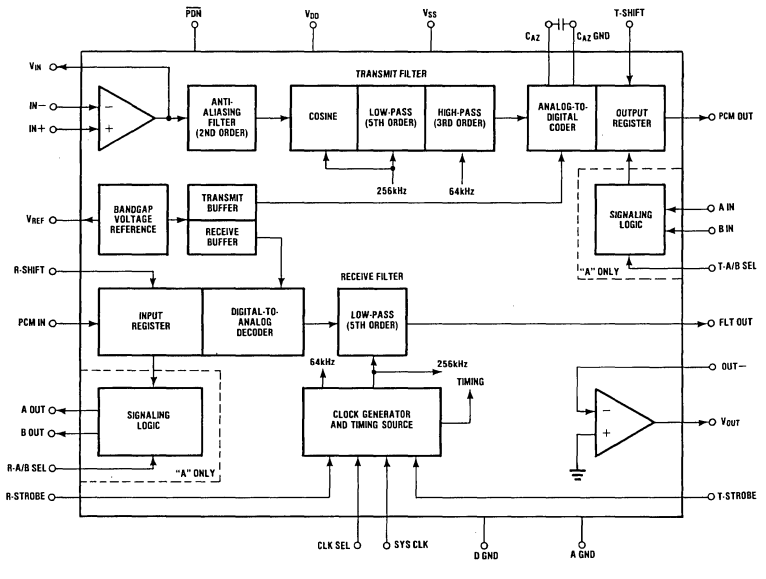
- ☐ Independent Transmit and Receive Sections With 75dB Isolation
- ☐ Low Power CMOS 80mW (Operating) 8mW (Standby)
- ☐ Stable Voltage Reference On-Chip
- ☐ Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- ☐ Input Analog Filter Eliminates Need for External Anti-Aliasing Prefilter
- ☐ Input/Output Op Amps for Programming Gain
- ☐ Output Op Amp Provides ±3.1V into a 1200Ω Load or Can Be Switched Off for Reduced Power (70mW)
- ☐ Special Idle Channel Noise Reduction Circuitry for Crosstalk Suppression
- ☐ Encoder has Dual-Speed Auto-Zero Loop for Fast Acquisition on Power-Up
- ☐ Low Absolute Group Delay = 450μsec. @ 1kHz

General Description

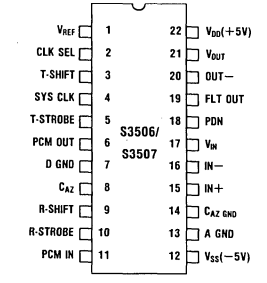
The S3506 and S3507 are monolithic silicon gate CMOS Companding Encoder/Decoder chips designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analog↔digital conversion circuits that conform to the desired transfer characteristic. The S3506 provides the European A-Law companding and the S3507 provides the North American μ-Law companding characteristic.

These circuits provide the interface between the analog signals of the subscriber loop and the digital signals of the PCM highway in a digital telephone switching system.

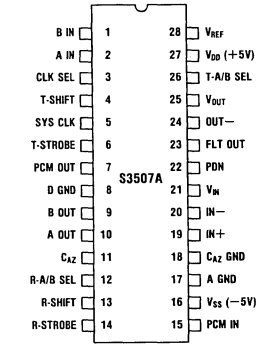
Block Diagram



Pin Configuration (22 Pin)



Pin Configuration (28 Pin)



General Description (Continued)

The devices operate from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or time-slot asynchronous operation.

In 22-pin cerdip or ceramic packages (.400″ centers) the S3506/S3507 are ideally suited for PCM applications: Exchange, PABX, Channel bank or Digital Telephone as well as fiber optic and other non-telephone uses. A 28-pin version, the S3507A, provides standard μ-Law A/B signaling capability. These devices are also available in a 28-pin chip carrier (see page 9). Extended temperature range versions can be supplied.

Absolute Maximum Ratings

DC Supply Voltage V_{DD}	+6.0V
DC Supply Voltage V_{SS}	−6.0V
Operating Temperature	−40°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation at 25°C	1000mW
Digital Input	V_{SS} −0.3≤V_{IN}≤V_{DD} +0.3
Analog Input	V_{SS} −0.3≤V_{IN}≤V_{DD} +0.3

Electrical Operating Characteristics (T_A = 0° to 70°C)

Power Supply Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{DD}	Positive Supply	4.75	5.0	5.25	V	
V_{SS}	Negative Supply	−4.75	−5.0	−5.25	V	
P_{OPR}	Power Dissipation (Operating)		80	110	mW	
P_{OPR}	Power Dissipation (Operating w/o Output Op Amp		70		mW	V_{DD} = 5.0V V_{SS} = −5.0V
P_{STBY}	Power Dissipation (Standby)		8	12	mW	

AC Characteristics (Refer to Figures 3A and 4A)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
D_{SYS}	System Clock Duty Cycle	40	50	60	%	
f_{SC}	Shift Clock Frequency	0.064		2.048	MHz	
D_{SC}	Shift Clock Duty Cycle	40	50	60	%	
t_{rc}	Shift Clock Rise Time			100	ns	
t_{fc}	Shift Clock Fall Time			100	ns	
t_{rs}	Strobe Rise Time			100	ns	
t_{fs}	Strobe Fall Time			100	ns	
t_{sc}	Shift Clock to Strobe (On) Delay	−100	0	200	ns	
t_{sw}	Strobe Width	600ns		124.3μs	@2.048 MHz	700ns min @1.544MHz
t_{cd}	Shift Clock to PCM Out Delay		100	150	ns	100pF, 510Ω Load
t_{dc}	Shift Clock to PCM in Set-Up Time	60			ns	
t_{rd}	PCM Output Rise Time C_L=100pF		50	100	ns	to 3V; 510Ω to V_{DD}
t_{fd}	PCM Output Fall Time C_L=100pF		50	100	ns	to .4V; 510Ω to V_{DD}
t_{dss}	A/B Select to Strobe Trailing Edge Set-up Time	100			ns	

DC Characteristics (V_{DD} = +5V, V_{SS} = −5V)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
R_{INA}	Analog Input Resistance IN+, IN−	100			KΩ	
C_{IN}	Input Capacitance to Ground		7	15	pF	All Logic and Analog Inputs
	Shift Clock, PCM IN, System Clock, Strobe, PDN					
I_{INL}	Logic Input Low Current			1	μA	V_{IL} =0.8V
I_{INH}	Logic Input High Current			1	μA	V_{IH} = 2.0V
	A/B Sel, A IN B IN					
I_{INL}	Logic Input Low Current			600	μA	V_{IL} = 0.8V
I_{INH}	Logic Input High Current			600	μA	V_{IH} = 2.0V
V_{IL}	Logic Input "Low" Voltage			0.8	V	
V_{IH}	Logic Input "High" Voltage	2.0			V	
V_{OL}	Logic Output "Low" Voltage (PCM Out)			0.4	V	510Ω Pull-up to V_{DD} + 2 LSTTL
V_{OL}	Logic Output "Low" Voltage (A/B Out)			0.4	V	I_{OL} = 1.6mA
V_{OH}	Logic Output "High" Voltage	2.6			V	I_{OH} = 40μA
R_L	Output Load Resistance V_{OUT}	1200			Ω	

Transmission Delays

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
	Encoder		125		μs	From T_{STROBE} to the Start of Digital Transmitting
	Decoder	30	8T+25		μs	T=Period in μs of R_{SHIFT} CLOCK
	Transmit Section Filter			182	μs	@1kHz
	Receive Section Filter			110	μs	@1kHz

S3506 Single-Chip A-Law Filter/Codec Performance

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)		−85	−73	dBmOp	CCITT G.712 4.1
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)			−60	dBmO	CCITT G.712 4.2
ICN_R	Idle Channel Noise (Receive Section)			−78	dBmOp	CCITT G.712 4.3
	Spurious Out-of-Band Signals at Channel Output			−28	dBmO	CCITT G.712 6.1
IMD_{2F}	Intermodulation (2 Tone method)			−35	dBm	CCITT G.712 7.1
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)			−49	dBm	CCITT G.712 7.2
	Spurious In-Band Signals at the Channel Output Port			−40	dBmO	CCITT G.712 9
	Interchannel Crosstalk $V_{IN} - V_{OUT}$	75	80		dB	CCITT G.712 11
$V_{IN(Max)}$	Max Coding Analog Input Level		±3.1		V_{Opk}	
V_{OUT} (Max)	Max Coding Analog Output Level		±3.1		V_{Opk}	R_L = 1.2KΩ

S3506 Single-Chip μ-Law Filter/Codec Performance (Continued)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ OdBmO
ED	Envelope	500 to 600Hz		200	750	μsec	Relative to Mini-
	Delay	600 to 1000Hz		120	375	μsec	mum Delay
	Distortion	1000Hz to 2600Hz		110	125	μsec	Frequency
		2600Hz to 2800Hz		160	750	μsec	
SD	Signal to	0 to −30dBmO	36	39		dB	Method 2 - Sine-
	Total	−40dBmO	29	31		dB	wave Signal Used
	Distortion	−45dBmO	24	26		dB	
GT	Gain Tracking with Input Level Variations (End-to-End. Each half channel is one half this value.)			±0.2 ±0.4 ±1.0	±0.5 ±1.0 ±3.0	dB dB dB	+3 to −40 dBmO −45 to −50 dBmO −55dBmO
ΔG	Gain Variation with Temperature and Power Supply Variation			±0.25		dB	
	Transmit Gain Repeatability			±0.1	±0.2	dB	
	Receive Gain Repeatability			±0.1	±0.2	dB	
$0TLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.51		VRMS	V_{OUT} Digital Milli- watt Response
$0TLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milli- watt Response at Decoder

S3507/S3507A Single-Chip μ-Law Filter/Codec Performance

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
ICN_W	Idle Channel Noise (Weighted Noise)		5	17	dBrncO	
ICN_{SF}	Idle Channel Noise (Single Frequency Noise)			−60	dBmO	
ICN_R	Idle Channel Noise (Receive Section)			15	dBrncO	
	Spurious Out-of-Band Signals at the Channel Output			−28	dBmO	
IMD_{2F}	Intermodulation (2 Tone method)			−35	dBm	
IMD_{PF}	Intermodulation (1 Tone + Power Frequency)			−49	dBm	
	Spurious In-Band Signals at the Channel Output Port			−40	dBmO	
	Interchannel Crosstalk $V_{IN}-V_{OUT}$	75	80		dB	
$V_{IN(Max)}$	Max Coding Analog Input Level		±3.1		V_{Opk}	
V_{OUT} (Max)	Max Coding Analog Output Level		±3.1		V_{Opk}	R_L 1.2KΩ
GT	Gain Tracking with Input Level Variations (End-to-End. Each half channel is one half of this value.)		±0.2 ±0.4 ±1.0	±0.5 ±1.0 ±3.0	dB dB dB	+3 to −40 dBmO −45 to −50 dBmO −55dBmO
ΔG	Gain Variation with Temperature and Power Supply Variation		±0.25		dB	
	Transmit Gain Repeatability		±0.1	±0.2	dB	
	Receive Gain Repeatability		±0.1	±0.2	dB	

S3507/S3507A Single-Chip μ-Law Filter/Codec Performance (Continued)

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
$0TLP_R$	Zero Transmission Level Point (Decoder See Figure 1)			1.51		VRMS	V_{OUT} Digital Milliwatt Response
$0TLP_T$	Zero Transmission Level Point (Encoder See Figure 1)			1.51		VRMS	V_{IN} to Yield Same as Digital Milliwatt Response at Decoder
AD	Absolute Delay End-to-End @ 1KHz			450	500	μsec	@ OdBmO
ED	Envelope Delay Distortion	500 to 600Hz		200	750	μsec	Relative to Minimum Delay Frequency
		600 to 1000Hz		120	375	μsec	
		1000Hz to 2600Hz		110	125	μsec	
		2600Hz to 2800Hz		160	750	μsec	
SD	Signal to Total Distortion	0 to −30dBmO	36	39		dB	
		−40dBmO	29	31		dB	
		−45dBmO	24	26		dB	

Pin/Function Descriptions

Pin	S3506/S3507	S3507A	Description
SYS CLK	4	5	**System Clock 256kHz**—This pin is a TTL compatible input for a 256kHz, 1.544MHz, 2048MHz, or 1.536MHz clock that is divided down to provide the filter clocks. The status of CLK SEL pin must correspond to the provided clock frequency.
T-SHIFT	3	4	**Transmit Shift Clock**—This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
R-SHIFT	9	13	**Receive Shift Clock**—This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
T-STROBE	5	6	**Transmit Strobe**—This TTL compatible pulse input (8kHz) is used for analog sampling and for initiating the PCM output from the coder. It must be synchronized with the T-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
R-STROBE	10	14	**Receive Strobe**—This TTL compatible pulse input (8kHz) initiates clocking of PCM input data into the decoder. It must be synchronized with the R-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
CLK SEL	2	3	**Clock Select**—This pin selects the proper divide ratios to utilize either 256kHz, 1.544MHz, 2.048MHz, or 1.536MHz as the system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz, to V_{SS} (−5V) for 1.544MHz or 1.536MHz operation, or to D GND for 256kHz operation.
PCM OUT	6	7	**PCM Output**—This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of T-SHIFT clock signal following a positive edge of the T-STROBE input. Data is clocked out by the positive edge of the T-SHIFT clock into one 510Ω pull-up per system plus 2 LS-TTL inputs.
PCM IN	11	15	**PCM Input**—This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of T-SHIFT clock.
C_{AZ}	8	11	**Auto Zero**—A capacitor of 0.1μF ±20% should be connected between these pins for coder auto zero operation. Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
C_{AZ} GND	14	18	
V_{REF}	1	28	**Voltage Reference**—Output of the internal band-gap reference voltage (≈−3.075V) generator is brought out to V_{REF} pin. Do not load this pin.
IN+	15	19	These pins are for analog input signals in the range of $-V_{REF}$ to $+V_{REF}$. IN− and IN+ are the inputs of a high input impedance op amp and V_{IN} is the output of this op amp. These three pins allow the user complete control over the input stage so that it can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain or as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel. V_{IN} should not be loaded by less than 47K ohms.
IN−	16	20	
V_{IN}	17	21	
FLT OUT	19	23	**Filter Out**—This is the output of the low pass filter which represents the recreated analog signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 47K ohms, or the Digital MilliWatt response will fall off slightly.

Pin/Function Descriptions (Continued)

Pin	S3506/S3507	S3507A	Description
OUT−	20	24	These two pins are the output and input of the uncommitted output amplifier stage. Signal at the FLT OUT pin can be connected to this amplifier to realize a low output impedance with unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel. The V_{OUT} pin has the capability of driving OdBm into a 600Ω load. (See Figure 1). If Out− is connected directly to V_{SS} the op amp will be powered down, reducing power consumption by 10mW, typically.
V_{OUT}	21	25	
V_{DD}	22	27	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins, respectively (typ. +5V, −5V). The voltages should be applied simultaneously or V_{SS} should be applied first.
V_{SS}	12	16	
A GND	13	17	Analog and digital ground pins are separate for minimizing crosstalk.
D GND	7	8	
$\overline{PDN}$	18	22	**$\overline{Power\ Down}$**—This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high or low, but as long as they are static, the powered down mode is in effect.
A IN		2	The transmit A/B select input selects the A signal input in a positive transition and the B signal input on the negative transition. These inputs are TTL compatible. The A/B signaling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronized to the T-STROBE input in each device.
B IN		1	
T-A/B SEL		26	
A OUT		10	In the decoder the A/B signaling bits received in the PCM input word are latched to the respective outputs in the same frame in which the R-AB SEL input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.
B OUT		9	
R-A/B SEL		12	

Functional Description

The simplified block diagram of the S3506/S3507 appears on page one. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A band-gap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analog signals first enter the chip at the uncommitted op amp terminals. This op amp allows gain trim to be used to set 0TLP in the system. From the V_{IN} pin the signal enters the 2nd order analog anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typ.) at 256kHz and 46dB (typ.) at 512Hz. From the Cosine Filter the signal enters a 5th Order Low-Pass Filter clocked at 256kHz, followed by a 3rd Order High-Pass Filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are >26dB (typ) from 0 to 60Hz and >35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analog-to-digital conversion process requires 9½ clock cycles, or about 72μs. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

The PCM data word is formatted according to the μ-law companding curve for the S3507 with the sign bit and the ones complement of the 7 magnitude bits according to the AT&T D3 specification. In the S3506 the PCM data word is formatted according to the A-Law companding curve with alternate mark inversion (AMI), meaning that the even bits are inverted per CCITT specifications.

Included in the circuitry of the S3507/S3507A is "All Zero" code suppression so that negative input signal values between decision value numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronization by T1 line clock recovery circuitry as there are never more than 15 consecutive zeros. The 8-bit PCM data is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz.

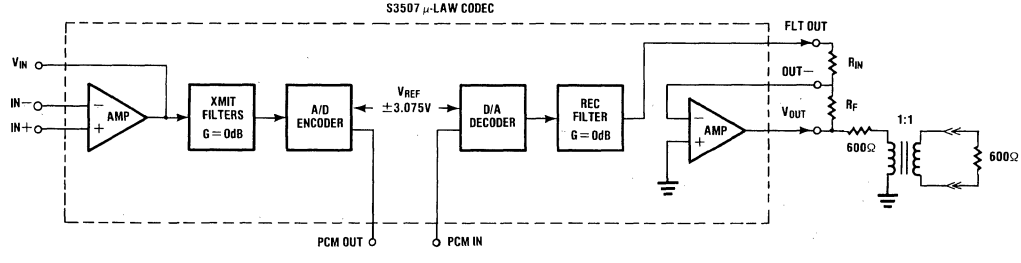
Idle Channel Noise Suppression

An additional feature of the CODEC is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of the chip is such that for 250msec. the only code words generated were +0, −0, +1, or −1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation, resetting the 250msec. timer. This feature is a form of Idle Channel Noise or Crosstalk Suppression. It is of particular importance in the S3506 A-Law version because the A-Law transfer characteristic has "mid-riser" bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialized to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order Low-Pass Filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalization to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 47kΩ. When used in this fashion the low impedance output amp can be switched off for a savings in power consumption. When it is required to drive a 600Ω load the output is configured as shown in Figure 1 allowing gain trimming as well as impedance matching. With this configuration a transmission level of 0dBm can be delivered into the load with the +3.14dB or +3.17dB overload level being the maximum expected level.

Figure 1. S3507 Input/Output Reference Signal Levels



IN VOLTS, $\emptyset TLP_{RMS}$ = .707 (V_{REF} −3.17dB)
= .707 [3.075 (10 $\frac{-3.17}{20}$)]
= 1.51 VRMS
WHERE V_{REF} = 3.075 VDC AND THE OVERLOAD IS 3.17dB

IN dBm, $\emptyset_{TLP}$ = 20 LOG $\frac{V_{\emptyset TLP}}{V_{\emptyset DBM}}$
= 20 LOG $\frac{1.51}{.775}$
= 5.8dBm
WHERE 0dBm = 1mW INTO 600Ω

Power Down Logic

Powering down the CODEC can be done in several ways. The most direct is to drive the $\overline{PDN}$ pin to a low level. Stopping both the transmit strobe and the receive strobe will also put the chip into the stand-by mode. The strobes can be held high or low.

Voltage Reference Circuitry

A temperature compensated band-gap voltage generator (−3.075V) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimize crosstalk. This reference voltage is trimmed during assembly to ensure a minimum gain error of ±0.2dB due to all causes. The V_{REF} pin should not be connected to any load.

Power Supply and Clock Application

For proper operation V_{DD} and V_{SS} should be applied simultaneously. If not possible, then V_{SS} should be applied first. To avoid forward-biasing the device the clock voltages should not be applied before the power supply voltages are stable. When cards must be plugged into a "hot" system it may be necessary to install 1000Ω current-limiting resistors in series with the clock lines to prevent latch-up.

Timing Requirements

The internal design of the Single-Chip CODEC paid careful attention to the timing requirements of various systems. In North America, central office and channelbank designs follow the American Telephone and Telegraph Company's T1 Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Yet, in digital telephone designs, CODEC's may be used in a non-multiplexed form with a data rate as low as 64kb/s. The S3507 and S3507A fill these requirements.

In Europe, telephone exchange and channelbank designs follow the CCITT carrier PCM format to multiplex 30 voice channels at a data rate of 2.048Mb/s. The S3506 is designed for this market and will also handle PABX and digital telephone applications requiring the A-Law transfer characteristics.

The timing format chosen for the AMI Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kb/s to 2.048Mb/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, the S3506/S3507 does not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+) edges of the strobe, forcing the PCM output in a high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and transmit/receive shift clocks are synchronized to it. Figure 2 shows the waveforms in typical multiplexed uses of the CODEC.

System Clock

The basic timing of the Codec is provided by the system clock. This 2.048MHz, 1.544MHz, or 256kHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. In most systems this clock will also be used as the shift clock to clock in and out the data. However, the shift clock can actually be any frequency between 64kHz and 2.048MHz as long as one of the two system clock frequencies is provided. Independent strobes and shift clocks allow asynchronous time slot operation of transmit and receive. The 3507 will also operate with a 1.536 system clock, as used in some PABX systems, with the CLK SEL pin in the 1.544 MHz Mode.

Signaling in μ-Law Systems

The S3506 and S3507 are compact 22-pin devices to meet the two worldwide PCM standards. In μ-Law systems there can be a requirement for signaling information to be carried in the bit stream with the coded analog data. This coding scheme is sometimes called 7-5/6 bit rather than 8 bit because the LSB of every 6th frame is replaced by a signaling bit. This is referred to as A/B Signaling and if a signaling frame carries the "A" bit, then 6 frames later the LSB will carry the "B" bit. To meet this requirement, the S3507A is available in a 28-pin dip package, or in a 28-pin dip carrier, as 6 more pins are required for the inputs and outputs of the A/B signaling.

Pin Configuration—S3507A 28-Lead Chip Carrier

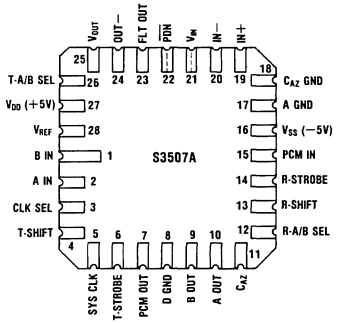
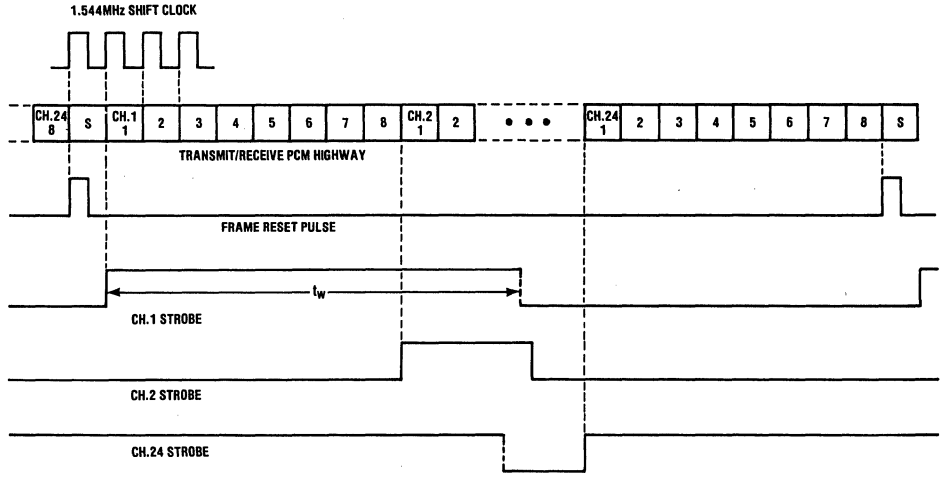
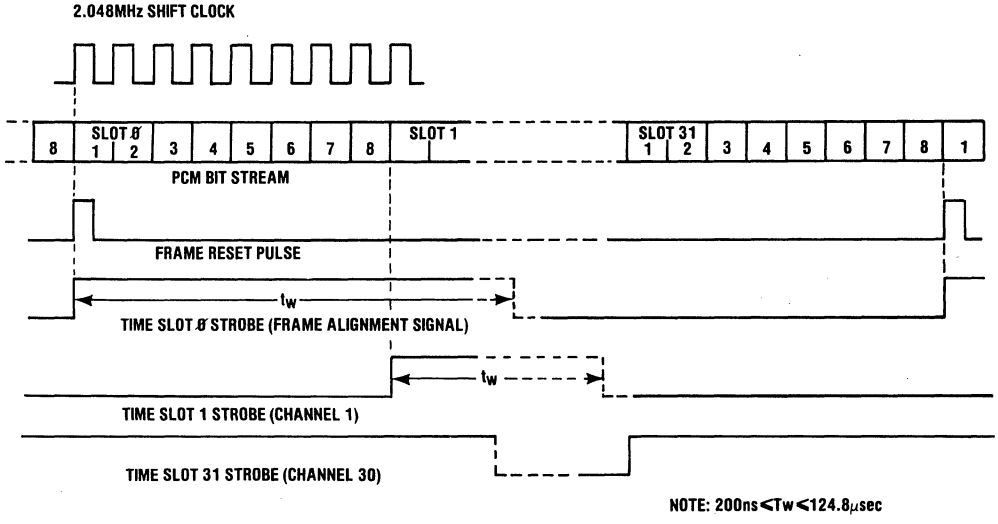


Figure 2A. Waveforms in a 24 Channel PCM System



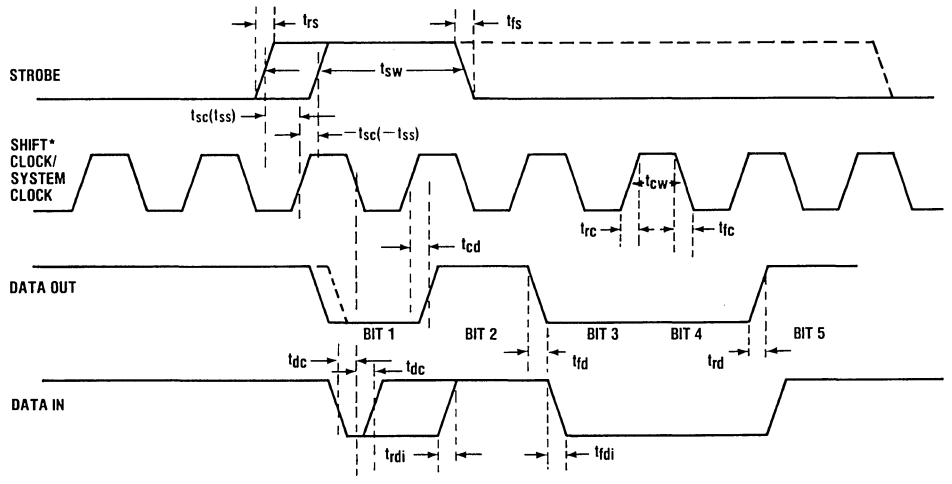
NOTE: t_W MIN = 200ns, t_W MAX = 124.8μs.

Figure 2B. Waveforms in 30 Channel PCM System



NOTE: 200ns$\leq$Tw$\leq$124.8μsec

Figure 2C. Waveform Details



*In this example the shift clock is the system clock (1.544 or 2.048MHz). In systems where the data shift rate is not the same the relationship of each to the strobe remains the same. The system clock and shift clock need not have coincident edges, but must relate to the strobe within the t_{sc}, t_{ss} timing requirements.

The effect of the strobe occurring after the shift clock is to shorten the first (sign) bit at the data output.

The length of the strobe is not critical. It must be at a logic state longer than one system clock cycle. Therefore, the minimum would be >488ns at 2.048 and the maximum <124.3μsec at 1.544MHz.

	MIN	MAX
t_{cw}	195nsec.	9.38μsec.
t_{rs}		100ns
t_{fs}		100ns
t_{sc}	−100nsec.	200ns ‡
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	600ns*	124.3μsec.
t_{cd}	100nsec.	150ns
t_{dc}	60nsec.	
t_{rdi}		100ns
t_{fdi}		100ns

‡That is, the strobe can precede the shift clock by 200nsec, or follow it by as much as 100nsec.

*@2.048MHz 700ns @1.544MHz

Signaling Interface

In the AT&T T1 carrier PCM format an A/B signaling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground, etc., depending on the application. Two signaling conditions (A and B) per channel, giving four possible signaling states per channel are repeated every 12 frames (1.5 milliseconds). The A signaling condition is sent in bit 8 of all 24 channels in frame 6. The B signaling conditions is sent in frame 12. In each frame, bit 193 (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The S3507A in a 28-pin package is designed to simplify the signaling interface. For example, the A/B select input pins are transition sensitive. The transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronizes the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channelbank. The A and B signaling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore, A/B select input must go positive in the beginning of frame 5 and the negative in the beginning of frame 11 (see Figure 3).

Figure 3. Signaling Waveforms in a T1 Carrier System

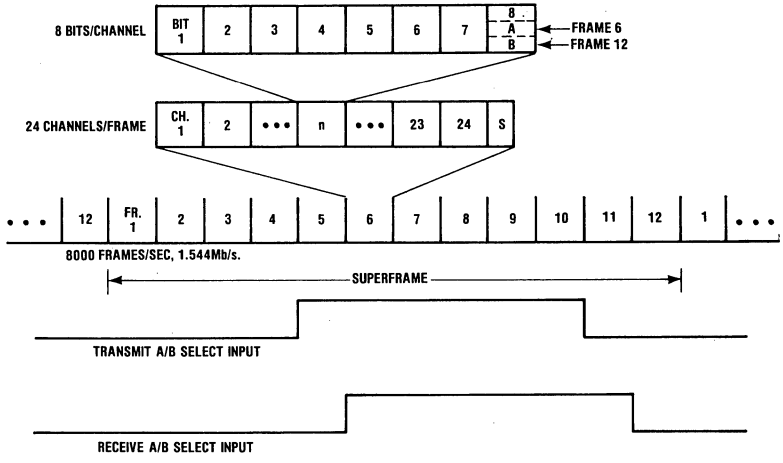
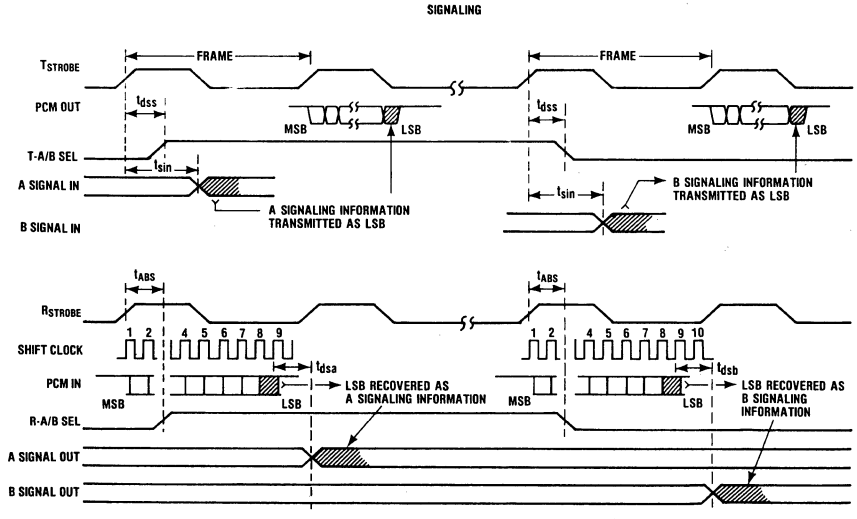
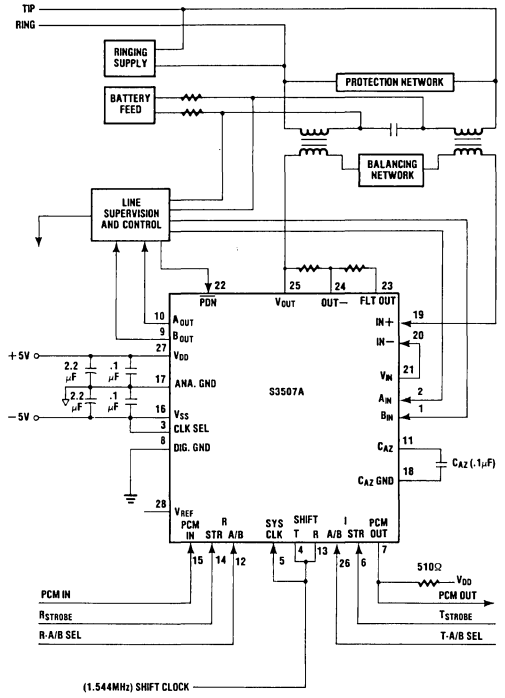


Figure 3A.. Signaling Waveform Details



	t_{dss}	t_{sin}	t_{ABS}	t_{dsa}	t_{dsb}
max	1.4μs	80μs	3μs	300ns	300ns

Figure 4. A Subscriber Line Interface Circuit



The decoder uses a similar scheme for receiving the A and B signaling bits, with one difference. They are latched to the respective outputs in the same frame in which the A/B select input makes a transition. Therefore, the receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

Applications Examples

There are two major categories of Codec applications. Central office, channel bank and PABX applications using a multiplex scheme, and digital telephone type dedicated applications. Minor applications are various A/D or D/A needs where the 8 bit word size is desirable for μP interface and fiber optic multiplex systems where non-standard data rates may be used.

A Subscriber Line Interface Circuit

Figure 4 shows a typical diagram of a subscriber line interface circuit using the S3507A. The major elements of such a circuit used in the central office or PABX are a two-to-four wire converter, PCM Codec with filters (S3507A) and circuitry for line supervision and control. The two-to-four wire converter—generally implemented by a transformer-resistor hybrid—provides the interface between the two-wire analog subscriber loop and the digital signals of the time-division-multiplexed PCM highways. It also supplies battery feed to the subscriber telephone. The line supervision and control circuitry provides off-hook and disconnect supervision, generates ringing and decodes rotary dial pulses. It supplies the A/B signaling bits to the coder for transmission within the PCM voice words. It receives A/B signaling outputs from the decoder and operates the A/B signaling relays.

In the T1 carrier system, 24 voice channels are multiplexed to form the transmit and receive highways, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mb/s.

Within the channelbank the transmit and receive channels of a Codec can occupy the same time slot for a synchronous operation or they can be independent of each other for time slot asynchronous operation. Asynchronous operation helps minimize switching delays through the system. Since the strobe or sync pulse for the coder and decoder sections is independent of each other in the S3507A, it can be operated in either manner.

In the CCITT carrier system, 30 voice channels and 2 framing and signaling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mb/s.

The line supervision and control circuitry within each subscriber line interface can generate all the timing signals for the associated Codec under control of a central processor. Alternatively, a common circuitry within the channelbank can generate the timing signals for all channels. Generation of the timing signals for the S3506 and S3507 is straightforward because of the simplified timing requirements (see Timing Requirements for details). Figures 5 and 5A show design schemes for generating these timing signals in a common circuitry. Note that only three signals: a shift clock, a frame reset pulse (coincident with the S bit) and a superframe reset pulse (coincident with the S bit in Frame 1) are needed. These signals are generated by clock recovery circuitry in the channelbank. Since the AMI Codec does not need channel strobes to be exactly 8-bit periods wide, extra decoding circuitry is not needed.

Figure 5. Generating Timing Signals in a T1 Carrier System

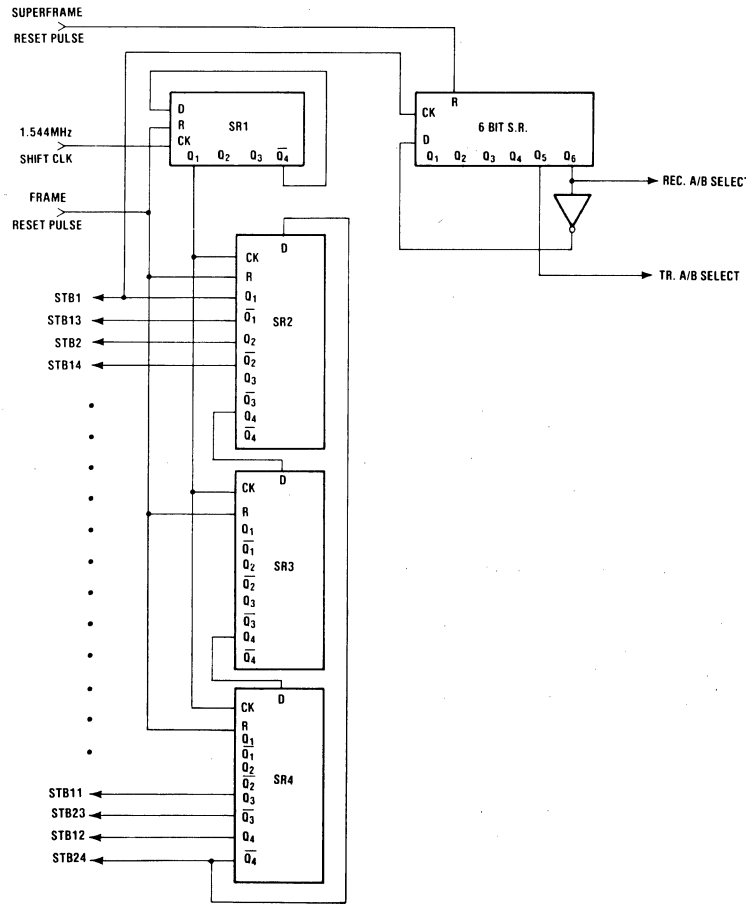
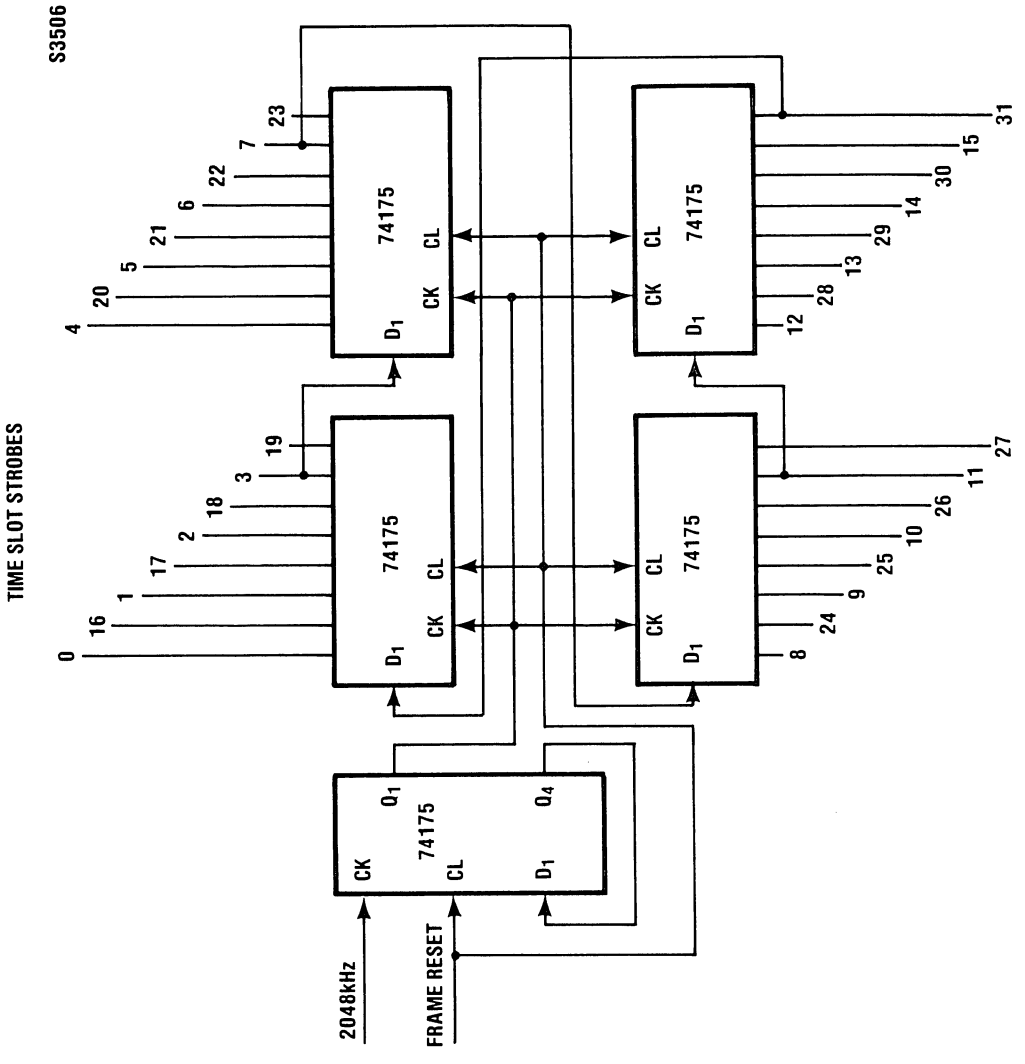


Figure 5A. Generating Timing Signals in a CCITT Carrier System (30+2 Channels)

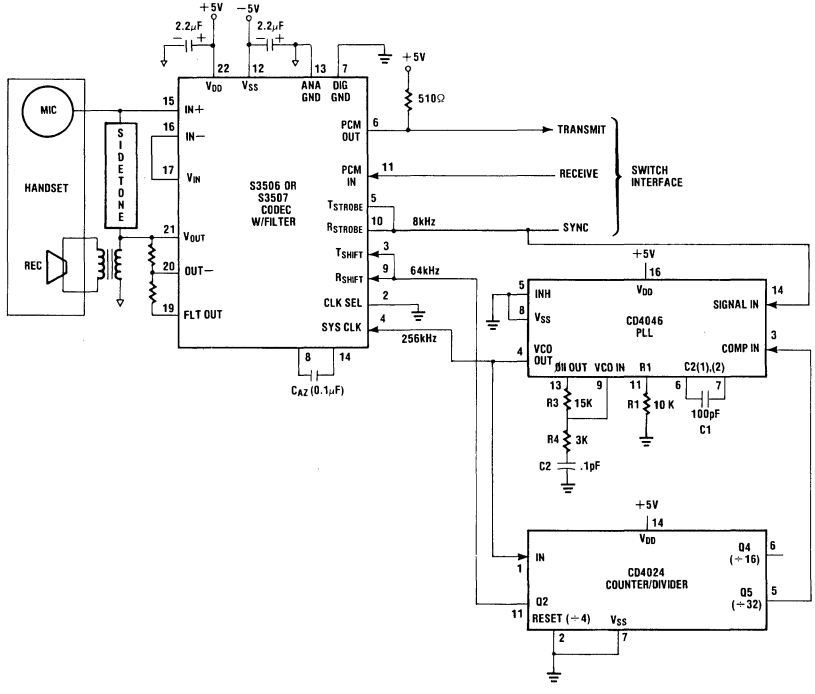


A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs to interface to the switch. Two pairs carry transmit and receive PCM voice data. One pair supplies an 8kHz synchronizing clock signal and the remaining pair supplies power to the telephone. More sophisticated designs reduce costs by time-division-multiplexing and superimposition techniques which minimize the number of wire pairs. The AMI Single-chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 6 shows a schematic for a typical digital telephone design.

Since asynchronous time slot operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 256kHz system clock and 64kHz shift clock from the 8kHz synchronizing signal received from the switch. The synchronizing signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output feeds directly into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

Figure 6. Voice Processing in a Digital Telephone Application



AMERICAN MICROSYSTEMS, INC.

S3525A/S3525B

DTMF BANDSPLIT FILTER

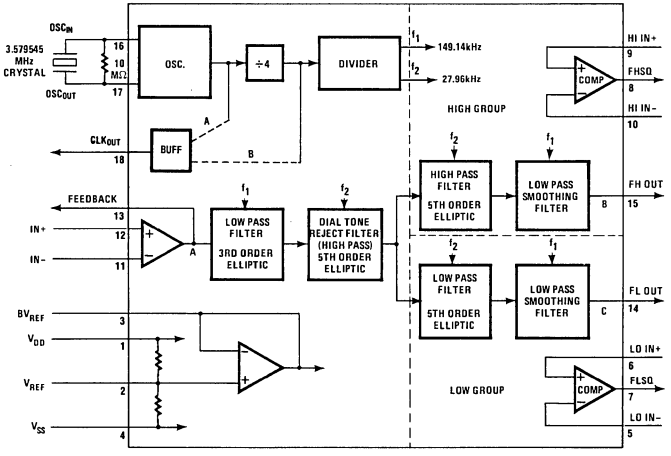
Features

- ☐ **CMOS Technology for Wide Operating Single Supply Voltage Range (7.0V to 13.5V). Dual Supplies (±3.5V to ±6.75V) Can Also Be Used.**
- ☐ **Uses Standard 3.58MHz Crystal as Time Base. Provides Buffered Clock to External Decoder Circuit.**
- ☐ **Ground Reference Internally Derived and Brought Out.**
- ☐ **Uncommitted Differential Input Amplifier Stage for Gain Adjustment**
- ☐ **Filter and Limiter Outputs Separately Available Providing Analog or Digital Outputs of Adjustable Sensitivity.**
- ☐ **Can be Used with Variety of Available Decoders to Build 2-Chip DTMF Receivers.**

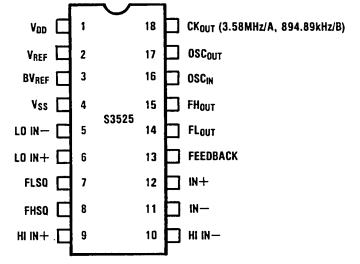
General Description

The S3525 DTMF Bandsplit Filter is an 18-pin monolithic CMOS integrated circuit designed to implement a high quality DTMF tone receiver system when used with a suitable decoder circuit. The device includes a dial tone filter, high group and low group separation filters and limiters for squaring of the filtered signals. An uncommitted input amplifier allows a programmable gain stage or anti-aliasing filter. An overall signal gain of 6dB is provided for the low group and high group signals in the circuit. The dial tone filter is designed to provide a rejection of at least 52dB in the frequency band of 300Hz to 500Hz. The difference between the S3525A and the S3525B is the frequency of output clock signal at the CKOUT pin. In the S3525B, it is a 894.89kHz square wave while in the S3525A, it is a 3.58MHz buffered oscillator signal. The S3525A can be used with digital DTMF decoder chips that need the TV crystal time base allowing use of only one crystal between the filter and decoder chips.

Block Diagram



Pin Configuration



Absolute Maximum Ratings:

DC Supply Voltage (V_{DD} - V_{SS})	+15.0V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +125°C
Analog Input	V_{SS} −0.3V ≤V_{IN}≤V_{DD} +0.3V

DC Electrical Operating Characteristics: T_A=0°C to +70°C

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref to V_{SS})		9.6	12.0	13.5	V
$V_{OL(CKOUT)}$	Logic Output "Low" Voltage I_{OL}=160μA			V_{SS}+0.4		V
$V_{OH(CKOUT)}$	Logic Output"High" Voltage I_{OH}=4μA			V_{DD}−1.0		V
$V_{OL(FH, FL)}$	Comparator Output Voltage Low	500pF Load			V_{SS}+0.5	V
		10kΩ Load			V_{SS}+2.0	V
$V_{OH(FH, FL)}$	Comparator Output Voltage High	500pF Load	V_{DD}−0.5			V
		10kΩ Load	V_{DD}−2.0			V
$R_{INA\ (IN-,IN+)}$	Analog Input Resistance		8			MΩ
$C_{INA\ (INA-,\ IN+)}$	Analog Input Capacitance				15	pF
V_{REF}	Reference Voltage Out		0.49 (V_{DD}−V_{SS})	0.50 (V_{DD}−V_{SS})	0.51 (V_{DD}−V_{SS})	V
V_{OR}=[BV_{REF}-V_{REF}]	Offset Reference Voltage				50	mV
P_D	Power Dissipation	V_{DD}=10V		170		mW
		V_{DD}=12.5V		400		mW
		V_{DD}=13.5V and 0°C			650	mW

AC System Specifications:

Symbol	Parameter/Conditions		Min.	Typ.	Max.	Units
A_F	Pass Band Gain		5.5	6	6.5	dB
	Dial Tone Rejection					
	Dial Tone Rejection is measured at the output of each filter with respect to the passband					
DTR_L	Low Group Rejection	350Hz	55	59		dB wrt 700Hz
		440Hz	50	53		dB wrt 700Hz
DTR_H	High Group Rejection	Either Tone	55	68		dB wrt 1200Hz

AC System Specifications (Continued)

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
	Attenuation Between Groups				
	Attenuation of the nearest frequency of the opposite group is measured at the output of each filter with respect to the passband				
GA_L	Attenuation of 1209Hz	50	>60		dB wrt 700Hz
GA_H	Attenuation of 941Hz	40	42		dB wrt 1200Hz
	Total Harmonic Distortion				
THD	Total Harmonic Distortion (dB). Dual tone of 770Hz and 1336 Hz sinewave applied at the input of the filter at a level of 3dBm each. Distortion measured at the output of each filter over the band of 300 Hz to 10kHz ($V_{DD}=12V$)			−40	dB
	Idle Channel Noise				
ICN	Idle Channel Noise measured at the output of each filter with C-message weighting. Input of the filter terminated to BV_{REF}			1	mV_{rms}
	Group Delay (Absolute)				
GD_L	Low Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms
GD_H	High Group Filter Delay over the band of 50Hz to 3kHz		4.5	6.0	ms

Pin/Function Descriptions

OSC_{IN}, OSC_{OUT} — These pins are for connection of a standard 3.579545MHz TV crystal and a 10MΩ ±10% resistor for the oscillator from which all clocking is derived. Necessary capacitances are on-chip, eliminating the need for external capacitors.

CKOUT (S3525A) — Oscillator output of 3.58MHz is buffered and brought out at this pin. This output drives the oscillator input of a decoder chip that uses the TV crystal as time base. (Only one crystal between the filter and decoder chips is required.)

CKOUT (S3525B) — This is a divide by 4 output from the oscillator and is provided to supply a clock to decoder chips that use 895kHz as time base.

IN−, IN+, Feedback — These three pins provide access to the differential input operational amplifier on chip. The feedback pin in conjunction with the IN− and IN+ pins allows a programmable gain stage and implementation of an anti-aliasing filter if required.

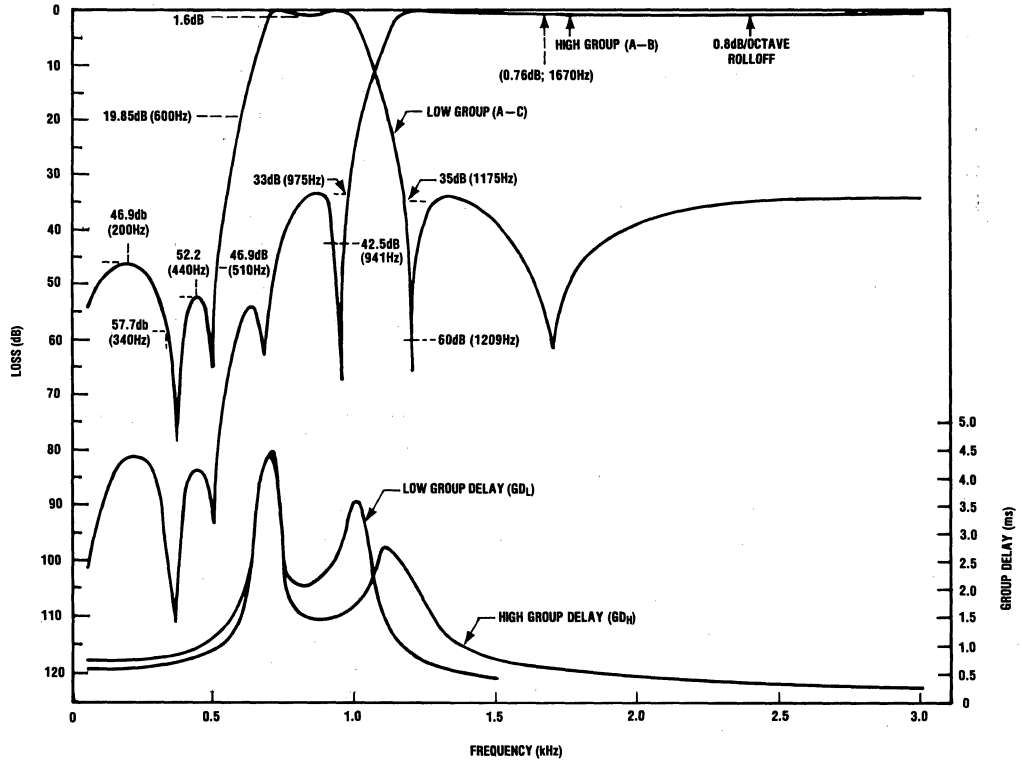
FH OUT, FL OUT — These are outputs from the high group and low group filters. These can be used as inputs to analog receiver circuits or to the on-chip limiters.

HI IN−, HI IN+
LO IN−, LO IN+ — These are inputs of the high group and low group limiters. These are used for squaring of the respective filter outputs. (See Figure 2.)

Pin/Function Descriptions (Continued)

FHSQ, FLSQ	These are respectively the high group and low group square wave outputs from the limiters. These are connected to the respective inputs of digital decoder circuits.
V_{DD}, V_{SS}	These are the power supply voltage pins. The device can operate over a range of $7V \leq (V_{DD} - V_{SS}) \leq 13.5V$.
V_{REF}	An internal ground reference is derived from the V_{DD} and V_{SS} supply pins and brought out to this pin. V_{REF} is $1/2(V_{DD} - V_{SS})$ above V_{SS}.
BV_{REF}	Buffered V_{REF} is brought out to this pin for use with the input and limiter stages.

Figure 1. Typical S3525 DTMF Bandsplit Filter Loss/Delay Characteristics



Input Configurations

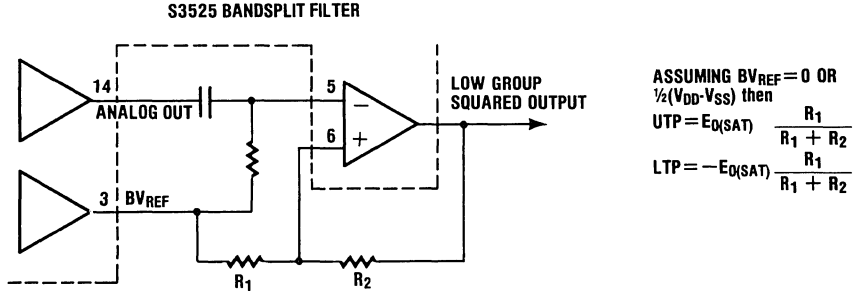
The applications circuits show some of the possible input configurations, including balanced differential and single ended inputs. Transformer coupling can be used if desired. The basic input circuit is a CMOS op amp which can be used for impedance matching, gain adjustment, and even filtering if desired. In the differential mode, the common mode rejection is used to reject power line-induced noise, but layout care must be taken to minimize capacitive feedback from pin 13 to pin 12 to maintain stability.

Since the filters have approximately 6dB gain, the inputs should be kept low to minimize clipping at the analog outputs (FL_{OUT} and FH_{OUT}).

Output Considerations

The S3525 has both analog and digital outputs available. Most integrated decoder circuits require digital inputs so the on-chip comparators are used with hysteresis to square the analog outputs. The sensitivity of the receiver system can be set by the ratio of R1 and R2, shown in Figure 2. The amount of hysteresis will set the basic sensitivity and eliminate noise response below that level.

Figure 2. Typical Squaring Circuit



Clock Considerations

The clock is provided by a standard 3.58MHz TV crystal in parallel with a 10MΩ resistor across pins 16 and 17. A buffered output at pin 18 is provided to drive the companion decoder at 3.58MHz (S3525A) or 895kHz (S3525B). It can be directly coupled or capacitively coupled depending on the decoder.

The circuits shown are not necessarily optimal but are intended to be good starting points from which an optimal design can be developed for each individual application.

Applications

Companion decoders to be used with the S3525 vary in performance and features. Teltone Corporation's TT6174, Rockwell Microelectronic's CRC8030 and MOSTEK's MK5102/03 are available units that can be used with the S3525.

Figure 3. AMI/Teltone 2 Chip DTMF Receiver

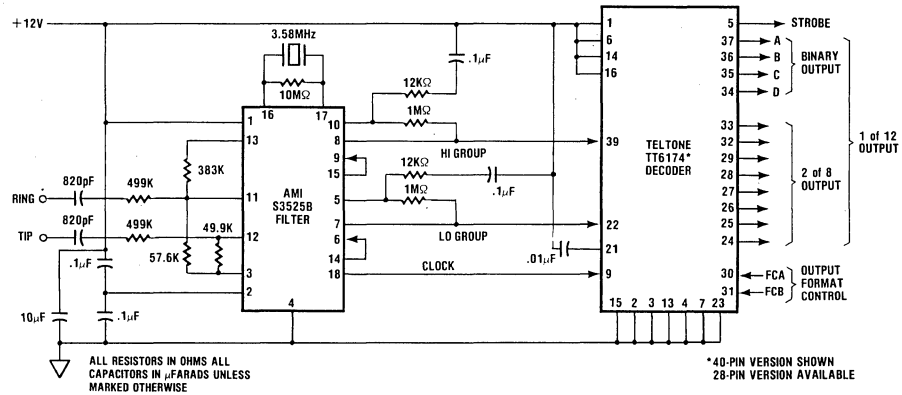


Figure 4. AMI/Mostek 2 Chip DTMF Receiver

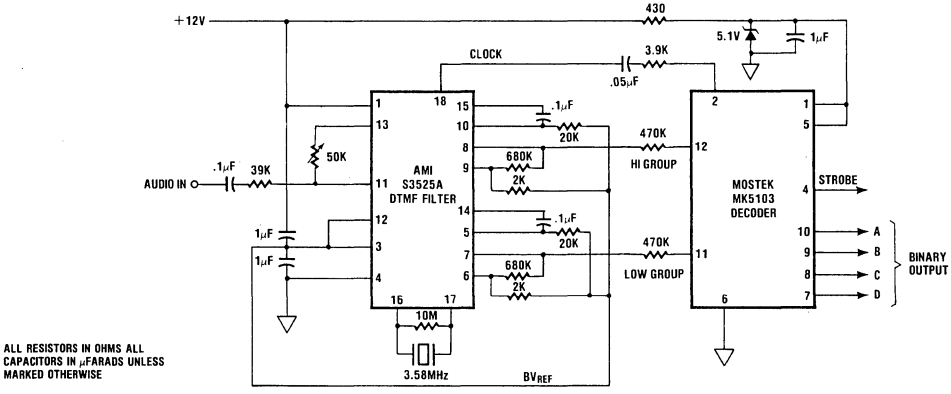
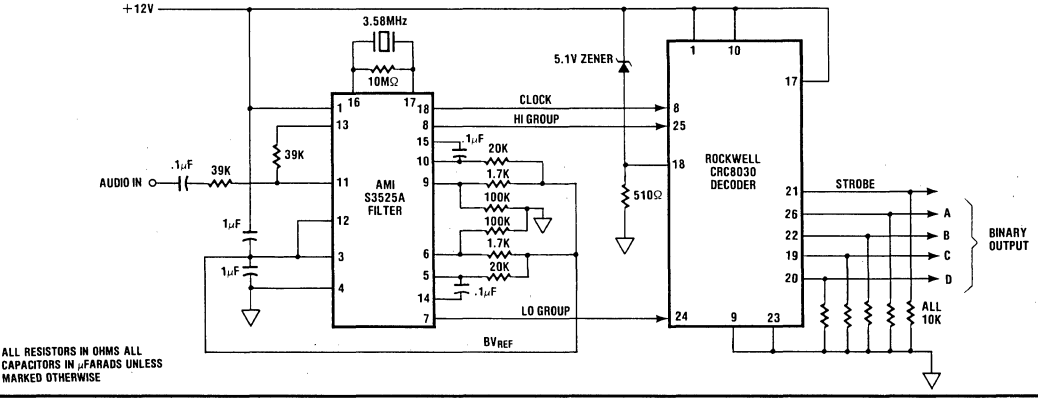


Figure 5. AMI/Rockwell 2 Chip DTMF Receiver



Additional information can be obtained from the S3525 Applications Note available on request from AMI, and from the suppliers of the decoder circuits.

AMERICAN MICROSYSTEMS, INC.

ADVANCED PRODUCT DESCRIPTION

S3526A/S3526B

2600Hz Bandpass/Notch Filter

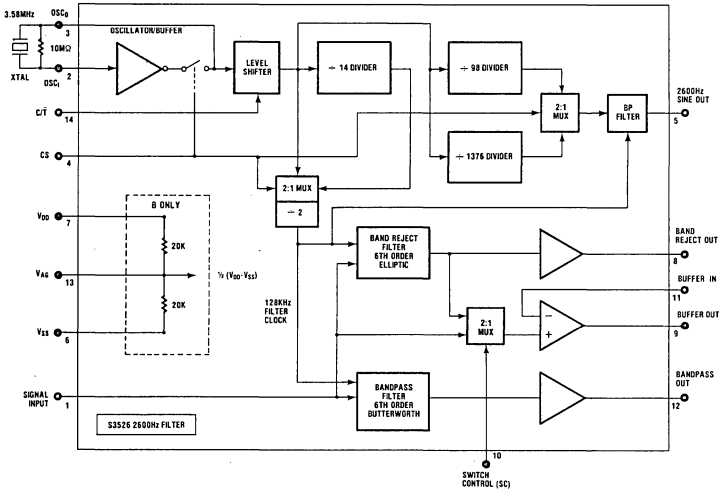
Features

- ☐ **Provides Band Pass and Band Reject Outputs**
- ☐ **Uses 3.58MHz TV Crystal or 256KHz Clock as Timebase for 2600Hz Center Frequency**
- ☐ **Generates 2600Hz Sinewave**
- ☐ **Single or Dual Supply Operation**
- ☐ **Buffer Drives 600Ω Loads**
- ☐ **The bandpass/notch frequency can be shifted from 2600Hz by using other clock frequencies.**

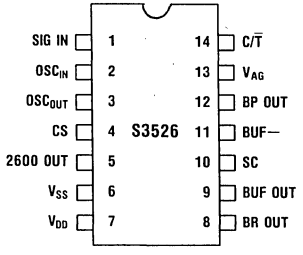
General Description

The S3526 Single Frequency (SF) Filter is a 14-pin monolithic CMOS circuit designed to implement a precision SF tone receiver. When used with an inexpensive 3.58 MHz TV crystal or a 256kHz clock input it provides sharp 2600 Hz bandpass and notch filters as well as a 2600Hz sine wave output. The 256kHz clock can be at CMOS or TTL levels. A change in the crystal (or clock) frequency from 3.58MHz (256kHz) will proportionately change the bandpass, notch and sine wave output frequencies. The S3526A is intended for dual +5V and −5V power supply operation, whereas the S3526B is intended for a single +10V supply.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage (V_{DD}-V_{SS})	+15.0V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Analog Input	V_{SS} −0.3V ≤ V_{IN} ≤ V_{DD} +0.3V

DC Electrical Operating Characteristics: T_A = 0°C to +70°C

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
V_{DD}	Positive Supply (Ref. to V_{SS})	9.0	10	13.5	V
P_D	Power Dissipation V_{DD} = 10V		100		mW
V_{OT}	2600Hz Sine Wave Output Load = 10KΩ		±3.1		V (P-P)
V_{T_D}	2600Hz Output Distortion Load = 10KΩ (for 2600Hz center frequency)		−35		dB
R_{IN}	Input Resistances (Except SIG IN)	8			MΩ
C_{IN}	Input Capacitances			15.0	pF

Filter Performance Specifications

Symbol	Parameter/Conditions	Min.	Typ.	Max.	Units
A_F	Pass Band Gain - All Paths	−0.5	0	0.5	dB
Z_{IN}	Input Impedance (SIG IN, Pin 1)		2.5		MOhms
	2600Hz Band Rejection Filter Attenuation (referenced from 1000Hz)				
	250Hz to 2200Hz	−0.5	0.1	0.5	dB
	2200Hz to 2400Hz	−0.5		5.0	dB
	2585Hz to 2615Hz	60	70		dB
	2800Hz to 3000Hz	−0.5		5.0	dB
	3000Hz to 3400Hz	−0.5	0.1	0.5	dB
	2600Hz Band Pass Filter Attenuation (referenced from 2600Hz)				
	DC to 1600Hz	70	80		dB
	2100Hz	50	63		dB
	2400Hz	30	37		dB
	2540Hz	3	5.8		dB
	2560Hz		.9	3	dB
	2640Hz		1.3	3	dB
	2660Hz	3	6.5		dB
	2800Hz	30	35		dB
	3100Hz	50	58		dB
	3600Hz	70	74		dB
	Ripple 2564Hz to 2632Hz			0.5	dB

Table 1: Control Pin Definitions

Pin No.	Name	Connection	Operation	Note
14	C/$\overline{T}$	V_{DD} to (V_{DD} − 0.5V)	CMOS Logic Levels	1
		(V_{DD} − 4V) to V_{SS}	TTL Logic Levels	
4	CS	V_{DD}	Ext. 256KHz Sq. Wave Clock at Pin 3	2
		V_{SS} or V_{AG}	3.58MHz Crystal Connected Between Pins 2 and 3 or 3.58 Clock to Pin 2	
10	SC	V_{DD}	Buffer Out = Input Signal	
		V_{SS}	Buffer Out = Band Reject Out	

Notes:

1) CMOS logic levels are same as V_{DD} and V_{SS} supply voltage levels. For TTL interface ground of TTL logic must be connected to V_{SS} supply pin.

2) For ext. 256KHz clock operation pin 2 must be connected to V_{DD}. For ext. 3.58 clock, drive pin 2, leave pin 3 open.

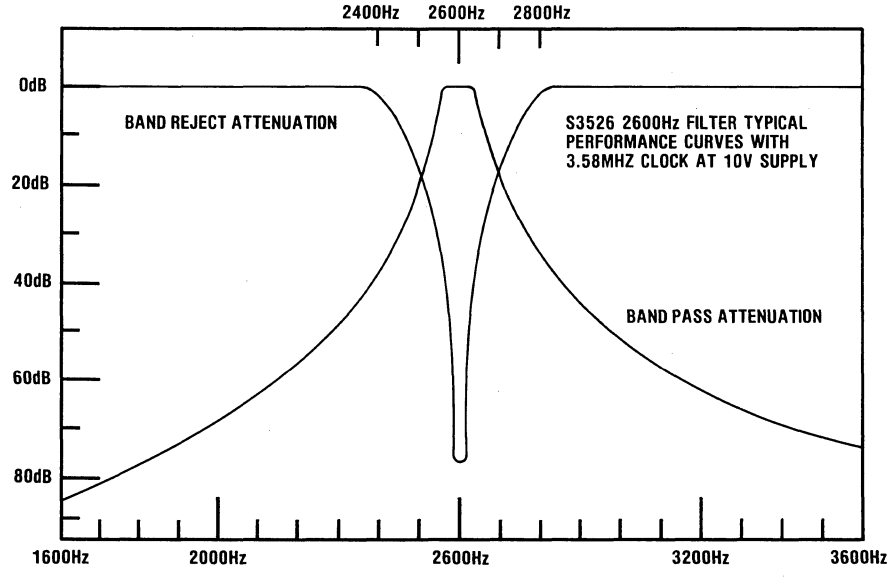
Pin Function Description

Pin	No.	Function
SIG IN	1	Signal In — This pin is the analog input to the filters and the buffer. It is a high impedance input (Z≈2.5MΩ).
OSC_{IN} OSC_{OUT}	2 3	These pins are the timing control for the entire chip. A 3.58MHz TV crystal is connected across these two pins in parallel with a 10MegOhm resistor. Another option is to provide a 256KHz signal at pin 3 and connect pin 2 to V_{DD}. It may be either TTL or CMOS levels, as determined by pin 14. Or, a CMOS level external 3.58MHz may be applied to pin 2 directly leaving pin 3 open.
CS	4	Clock Select - This pin when tied to V_{DD} configures the chip for 256KHz clock input operation. When tied to V_{AG} or V_{SS} the chip operates from a 3.58MHz crystal or clock input.
2600 OUT	5	This is an output pin providing a 2600Hz sine wave.
V_{SS}	6	Negative supply voltage pin.
V_{DD}	7	Positive supply voltage pin.
BR OUT	8	Band Reject Out - This is the output of the filter that notches out 2600Hz energy. It should drive a load ⩾10KΩ.
BUF OUT	9	Buffer Out - This buffer can drive a 600Ω load and provides either the reproduced signal input without filtering, or provides the signal input with 2600Hz energy notched out.
SC	10	Switch Control - This pin controls which signal is presented at the Buffer Out. A logic high (V_{DD}) connects the input signal straight through. A logic low (V_{SS}) connects the output of the 2600Hz band reject filter to the Buffer Out.
BUF-	11	Buffer Negative - This is the inverting input to the buffer.
BP OUT	12	Band Pass Out - This is the output of the 2600Hz band pass filter which will pass any energy at 2600Hz present at the Signal In pin. It should drive a load ⩾ 10KΩ.
V_{AG}	13	Analog Ground - This is the analog ground pin for audio inputs and outputs. When used with a single supply, this pin is 1/2 (V_{DD}-V_{SS}). When used with +5V supplies, this point is at ground. The S3526B has internal voltage divider resistors to V_{DD} and V_{SS} of ≅20KΩ. The S3525A does not.
C/$\overline{T}$	14	This pin determines whether CMOS or TTL levels will be accepted at pin 3 for a clock input. When tied to V_{DD}, the chip accepts CMOS logic levels; when tied to a point ⩽(V_{DD}-4V), the chip accepts TTL levels.

Table 2: Analog Signal Parameters

Parameter	Min.	Typ.	Max.	Units
Input Signal Level			(V_{DD}-V_{SS})	Volts
Load Resistance (R_L) (BR OUT, BP OUT)		10		kΩ
Load Resistance (R_L) (BUFF OUT)		600		Ohms
Output Signal Level into R_L (Typ) BR OUT, BP OUT, BUFF OUT			+9	dBm

Figure 1. Typical Filter Performance Curves



AMERICAN MICROSYSTEMS, INC.

S3610

LPC-10 SPEECH SYNTHESIZER WITH ON-CHIP 20K SPEECH DATA ROM

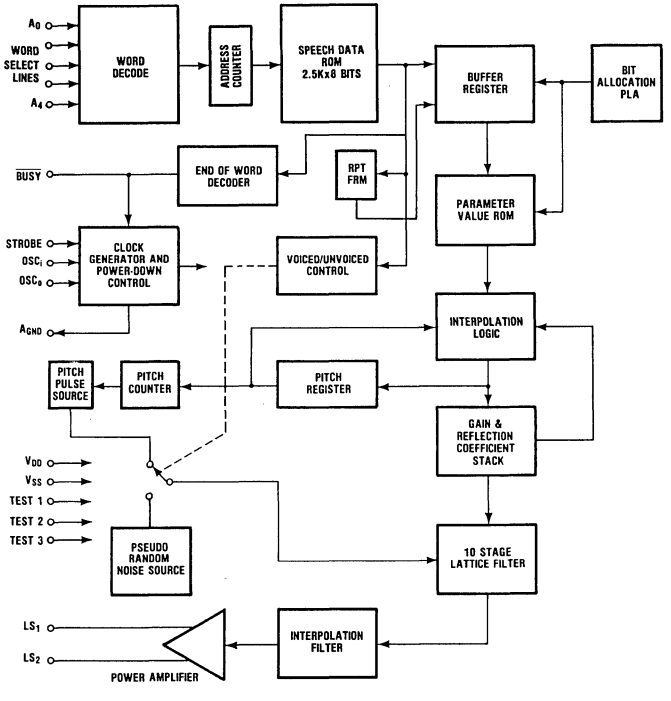
Features

- ☐ Simple Digital Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Power Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ 20K Bits Speech ROM
- ☐ Low Data Rate
- ☐ Up to 32 Word Vocabulary

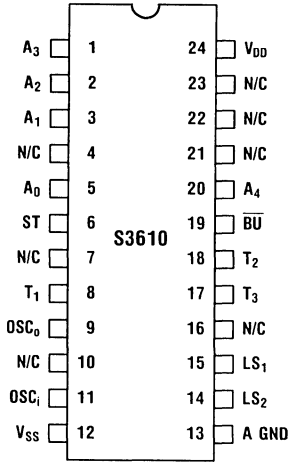
General Description

The S3610 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an internal 20K bit ROM. The simple digital interface consists of 5 word-select lines, a strobe input to load the address data and initiate operation, and a busy output signal. At the end of enunciation the chip automatically goes into the power-down mode until a new word select address is strobed in. The data rate from the speech ROM into the synthesizer is 2.0K bits/sec max. Typically the average data rate will be reduced to about 1.2K bits/sec. by means of the data rate reduction techniques used internally, giving about 17 seconds of speech from the ROM data. The 5 word-select lines allow a maximum vocabulary of 32 words.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

The synthesizer is realized using analog switched-capacitor filter technology and operates at 8K samples/sec. An output interpolating filter and bridge power amplifier give 30mW output power at 6 volts supply and allow the device to be connected directly to a 100Ω loudspeaker.

The S3610 also features an on-chip oscillator, requiring only a 640kHz ceramic resonator and a 120pF capacitor for normal operation.

AMI is able to provide a speech analysis service to generate the LPC parameters from customers' speech supplied on audio magnetic tape.

Absolute Maximum Ratings*

Supply Voltage	11 Volts DC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Voltage at any Pin	V_{SS} −0.3 to V_{SS} +0.3V
Lead Temperature (soldering, 10 sec.)	200°C
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications: (V_{DD}=6.0V ±10%, V_{SS}=0V, C_{AG}=0.047μF, T_A=0° to 70°C, unless otherwise specified)

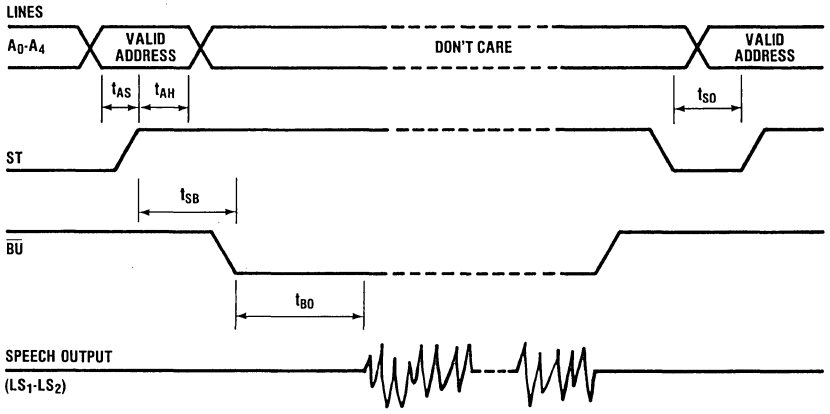
D.C. Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.4		V_{DD}	V	
V_{IL}	Input Low Logic "0" Voltage	−0.3		0.8	V	
I_{IN}	Input Leakage Current			10	μA	V_{IN}=0 to V_{DD}
V_{OL}	Output Low Voltage Busy Output			0.4	V	I_{OL}=1.6mA
ΔV_{OA}	Output DC Offset Voltage, Audio			200	mV	
V_{OA}	DC Output Voltage, Audio		½V_{DD}			R_{LOAD}=100Ω
I_{DD}	Supply Current, Operating		25		mA	
I_{DDL}	Supply Current, Powerdown		0.75		mA	

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
P_O	Audio Output Power		30		mW	R_{LOAD}=100Ω
t_{AS}	Address Set-up Time	200			nsec	See Figure 1
t_{AH}	Address Hold Time	10			nsec	See Figure 1
t_{SO}	Strobe Off Width	1			μsec	See Figure 1
t_{SB}	Strobe to Busy Delay		100	500	nsec	See Figure 1
t_{BO}	Busy to Speech Output Delay		19		msec	See Figure 1
F_{OSC}	Oscillator Resonator Frequency	−1%	640	+1%	KHz	
R_{LOAD}	Audio Output Load Impedance		100		Ω	
C_{INOSC}	Input Capacitance, Oscillator		100		pF	
C_{IN}	Input Capacitance, Digital Interface		7		pF	

Figure 1. Timing Requirements



Pin Function/Description

Digital Interface

A_0 through A_4	**Word Select Inputs.** The 5-bit address data on these lines selects the word to be enunciated from the internal vocabulary.
ST	**Strobe Input.** A rising edge on this line strobes in the word select data and causes enunciation to commence. If this line is taken low prior to the end of enunciation (as indicated by the busy signal), enunciation stops immediately and the chip goes into power down mode.
$\overline{BU}$	**Busy Output.** This open drain output signals that enunciation is in progress by going low.

Audio Interface

LS1 and 2	**Loudspeaker Outputs.** These pins are used to connect the chip to the loudspeaker. They are D.C. coupled and have an offset of half the supply voltage. The audio output is balanced on the two outputs.

Misc.

OSC_i, OSC_o	**Oscillator Input and Output.** A 640KHz ceramic resonator (MuRata CSB640A or equivalent) should be connected between these pins for normal operation, or an external 640KHz signal may be fed into OSC_i. When a resonator is used, a 120pF capacitor should be connected between OSC_i input and ground.
T_1, T_2, T_3	**Test Inputs.** These inputs should be left unconnected for normal operation.
V_{SS}	Most negative supply input. Normally connected to 0V.
V_{DD}	Most positive supply input.
A_{GND}	**Analog Ground.** An internally generated level approximately half way between V_{SS} and V_{DD}. A 0.047μF decoupling capacitor should be connected from this pin to V_{SS}. Do not connect this pin to a voltage supply.

Circuit Description

The main components of the S3610 LPC-10 Speech Synthesizer are shown in the block diagram.

Word Decode ROM—This ROM decodes the data presented on the word select lines into the start addresses of the speech words as stored in the Speech Data ROM. Up to 32 twelve bit start addresses may be programmed into this ROM. When the strobe line is taken high the start address selected is used to preset the Address Counter.

Address Counter—This binary counter is used to address the Speech Data ROM. After being preset to the desired start address it is incremented each time a new byte of data is required for the synthesizer.

Speech Data ROM—This ROM contains the 2.5K (2560) bytes of LPC-10 parameters encoded into a non-linearly quantized packed format. This format allows each frame of LPC parameters to be stored in only 5 bytes or less and is shown in Figure 2.

End of Word Decoder—This circuit detects the special code indicating that the last byte read from the Speech Data ROM denotes the end of the speech word data and initiates the power down routine after the previous frame has been enunciated.

Buffer Registers—The data from the Speech Data ROM is assembled into frames and then decimated into the 12 parameters required for LPC-10 synthesis: pitch, gain and the 10 lattice filter coefficients. The parameters are stored in an encoded format and the decoding is done in the Parameter Value ROM. The coefficient address registers are used to store the assembled frame data and address this ROM.

Bit Allocation PLA—A programmable logic array is used to control the allocation of bits in the Buffer Register to the 12 parameters. The allocation and permissible variations are shown in Figure 2.

Parameter Value ROM—This ROM is used as a look-up table to decode the stored parameters into the LPC coefficients.

Interpolation Logic—The coefficients for each frame of speech, normally 20msec. are interpolated four times per frame to generate smoother and more natural sounding speech. Hence, the interpolation period is one quarter of a frame period, normally 5msec. After interpolation, the coefficients are used to drive the pitch-pulse source, the lattice filter and the gain control. Interpolation is inhibited when a change from voiced to unvoiced speech, or vice versa, is made.

Pitch Register and Counter—This register stores the pitch parameter used to control the pitch counter.

Pitch-pulse Source—This is the signal source for voiced speech (vowel sounds). It is realized in switched-capacitor technology and generates symmetrical bipolar pulses at the rate specified by the pitch parameter and controlled by the pitch counter.

Pseudo-random Noise Source—This is the signal source for unvoiced speech (fricatives and sibilants) and consists of a 15-bit linear code generator giving a periodicity of 32767 sampling periods (4.096sec.). The output of this generator is scaled to a lower value and used as a random sign, constant amplitude signal.

Voiced/Unvoiced Speech Selector Switch—This switch determines whether the voiced or unvoiced signal source is used to drive the filter during a given frame.

LPC-10 Parameter Stack—This stack of 10 filter coefficients is used to control the lattice filter. The coefficients have an accuracy of 8-bits plus sign.

10 Stage Lattice Filter—The filter which simulates the effect of the vocal tract on the sound source (glottis) in the human speaker is realized here as a switched-capacitor (analog sampled data) 10 stage lattice filter. The filter parameters are determined dynamically by the time varying coefficients in the Parameter Stack and the filter operates at a sampling frequency of 8KHz (clock frequency/80).

Gain Controller—This controls the input signal level to the lattice filter to vary the sound level, and is an integral part of the lattice filter.

Interpolation Filter—The output signal from the lattice filter is sampled at 8KHz, and consequently its spectrum is rich in aliasing (foldover) distortion components above 4KHz (See Figure 3). The signal is cleaned up by passing it through a 4KHz low pass filter sampled at 160KHz. The spectrum of the output signal contains no aliasing distortion components below 156KHz, making the output suitable for feeding directly into a loudspeaker after amplification. This filter is also realized using switched-capacitor filter technology.

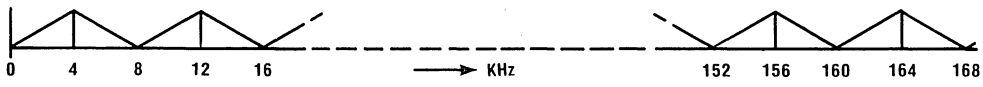
Power Amplifier—The amplifier brings up the level of the signal to give an output level of 30mW RMS into 100Ω load. The output is a balanced bridge configuration with anti-phase signals on the 2 output pins.

Figure 2. Packed Quantized Data Formats

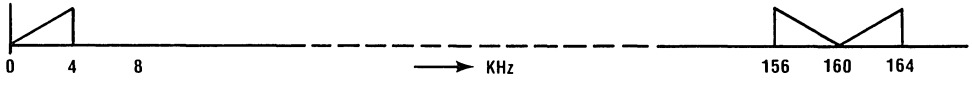
	BYTE 5								BYTE 4								BYTE 3								BYTE 2								BYTE 1							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
VOICED	← PITCH →								← K10,K9,K8,K7,K6,K5 →								← K4,K3, K2, K1 →																→	V/UV	REPT	← GAIN →				
UNVOICED	← NOT USED →																← K4,K3, K2, K1 →																→	V/UV	REPT	← GAIN →				
REPEAT	← NOT USED →																																← PITCH →			GAIN				REPT*
END OF WORD	← NOT USED →																																0	0	0	0	0	0	0	0

*NOTE: 0 = SINGLE (OR LAST) REPEAT. 1 = MULTIPLE REPEAT

Figure 3.



(a) SPECTRUM OF SIGNAL OUTPUT OF LATTICE FILTER



(b) SPECTRUM OF SIGNAL AT OUTPUT OF INTERPOLATION FILTER.
NOTE: IN BOTH CASES A SIN x/x CHARACTERISTIC MODULATES THE SPECTRA. THIS IS OMITTED FOR SIMPLICITY.

Clock Generators and Power-down Control—This block contains the oscillator and timing circuits and also generates the analog ground reference voltage.

Speech Data Compression

The data rate of the synthesizer input is 5400 bits/sec before interpolation (21600 bits/sec after interpolation) consisting of 12 parameters of 9 bits each repeated every 20msec. This is reduced to less than 2000 bits/sec for storage by means of a non-linear quantization technique. Each of the 12 coefficients is constrained to have a fixed set of values in an optimized manner. The actual values are dependent on the speech data and generated automatically in the analysis process. The parameters used to

specify the coefficients are stored in the speech data ROM and used to address the coefficient look-up table ROM. The packing formats for the speech data are shown in Figure 2.

The speech data rate is further reduced by two other techniques shown in Figure 2. A substantial reduction is achieved by reducing the order of the lattice filter (the LPC order) to 4 during periods of unvoiced speech. This allows a 40% data reduction during these periods, which themselves typically account for 30-40% of speech (in the English language). A second reduction is obtained by detecting periods during which the filter parameters may be the same as those in the previous frame. Only the gain and pitch parameters are updated in such a frame, allowing an 80% data reduction. Note that in repeat frame only 3 bits are allocated to the gain parameter. The LSB is forced internally to zero.

Programming the S3610

The word decode ROM, the speech data ROM and the coefficient ROM are mask programmed with the customer's speech data. Interfacing with AMI to produce the ROM mask is possible at several levels, to suit the customer's requirements. AMI is able to provide a complete speech analysis service for this purpose. This allows accurate programming of the ROMs from a speech sample provided on audio magnetic tape with a fast turnaround. Customers who have LPC speech analysis facilities and wish to interface with AMI at a different level should contact the factory for further details about the quantization technique and formats acceptable.

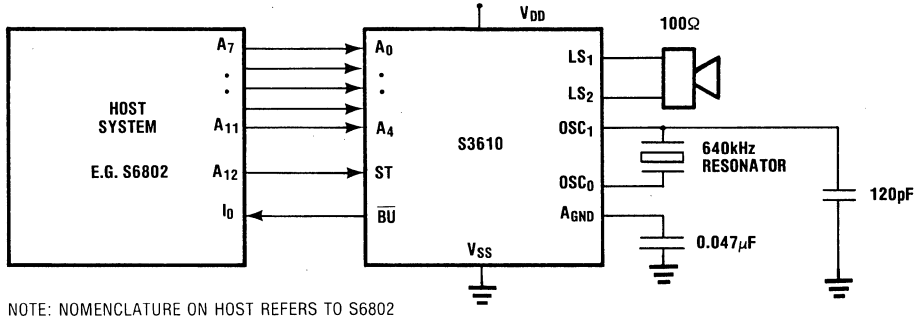
Interfacing

The S3610 is designed to be easily interfaced to a host controller. The interface timing requirements are shown in Figure 1. A valid 5-bit address should be presented on the word select lines and the strobe line taken to a logic 1 and held there until the end of enunciation, as indicated by the Busy output. A typical system configuration is shown in Figure 4. If it is not possible or inconvenient to monitor the Busy output or to maintain the strobe for the duration of the enunciation, these 2 lines may be combined as shown in Figure 5. The Busy output will automatically maintain the Strobe input once it is initiated. Note that an inverted strobe input is now required, and its duration should ensure that the Busy output goes low before it is removed. A minimum duration of 1μsec is recommended. A method of operating the synthesizer directly from a keyboard is shown in Figure 6. Using the 74C922 encoder limits the vocabulary to 16 words. This can be expanded to the maximum of 32 words by using 2 encoders. The R-C delay provides the address set-up time required before ST goes high.

Applications

Toys and Games
EDP
Instrumentation
Communications
Industrial Controls
Automotive
Appliances

Figure 4. Typical System Configuration



NOTE: NOMENCLATURE ON HOST REFERS TO S6802

Figure 5. Using Busy Output to Maintain Strobe

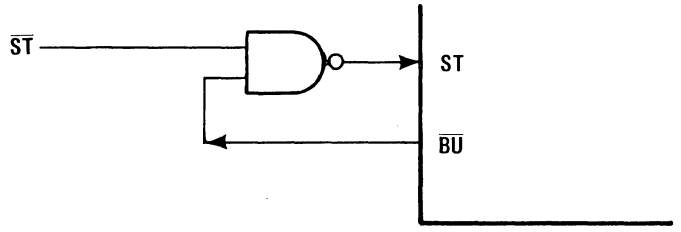
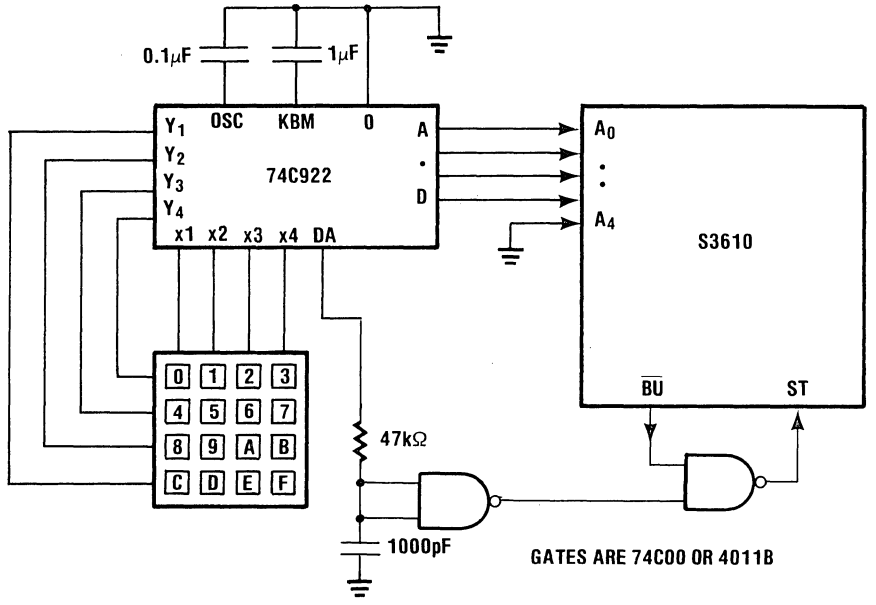


Figure 6. Direct Keyboard Operation



LPC-10 SPEECH SYNTHESIZER

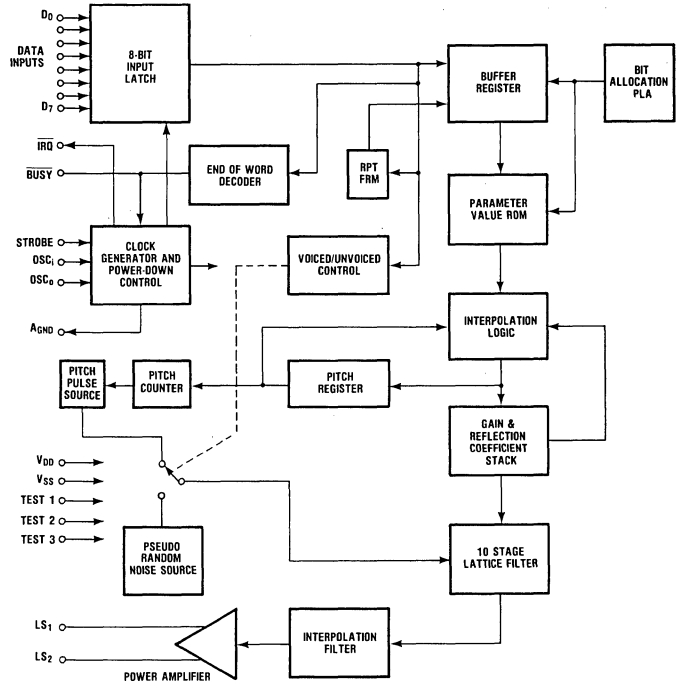
Features

- ☐ Simple Microprocessor Interface
- ☐ CMOS Switched-Capacitor Filter Technology
- ☐ Automatic Powerdown
- ☐ 5-8 Volts Single Supply Operation
- ☐ Direct Loudspeaker Drive
- ☐ 30mW Audio Output
- ☐ Low Data Rate

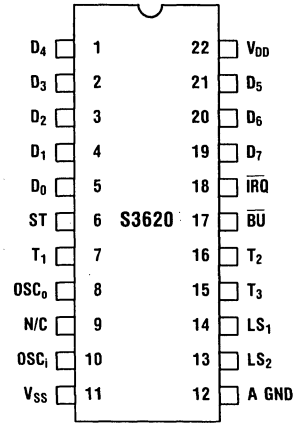
General Description

The S3620 LPC-10 Speech Synthesizer generates speech of high quality and intelligibility from LPC (Linear Predictive Coding) data stored in an external memory. The digital interface circuitry is fully microprocessor compatible and allows the processor to load the data with or without a DMA controller. The loading takes place on a handshake basis, and in the absence of a response from the processor the synthesizer automatically shuts down and goes into the powerdown mode. A busy signal allows the processor to sense the status of the synthesizer. The input data rate is 2.0K bits/sec. max., but typically the average data rate will be reduced to about 1.4K bits/sec. by means of the data rate reduction techniques used internally.

Block Diagram



Pin Configuration



N/C = NO CONNECTION

The synthesizer is realized using analog switched-capacitor filter technology and operates at 8K samples/sec. An output interpolating filter and bridge power amplifier give 30mW output power at 6 volts supply and allow the device to be connected directly to a 100Ω loudspeaker.

The S3620 also features an on-chip oscillator, requiring only a 640kHz ceramic resonator and a 120pF capacitor for normal operation.

AMI is able to provide a speech analysis service to generate the LPC parameters from customers' speech supplied on audio magnetic tape.

Absolute Maximum Ratings*

Supply Voltage	11 Volts DC
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Voltage at any Pin	V_{SS} −0.3 to V_{SS} +0.3V
Lead Temperature (Soldering, 10 sec.)	200°C
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications: (V_{DD}=6.0V ±10%, V_{SS}=0V, C_{AG}=0.047μF, T_A=0° to 70°C, unless otherwise specified)

D.C. Characteristics

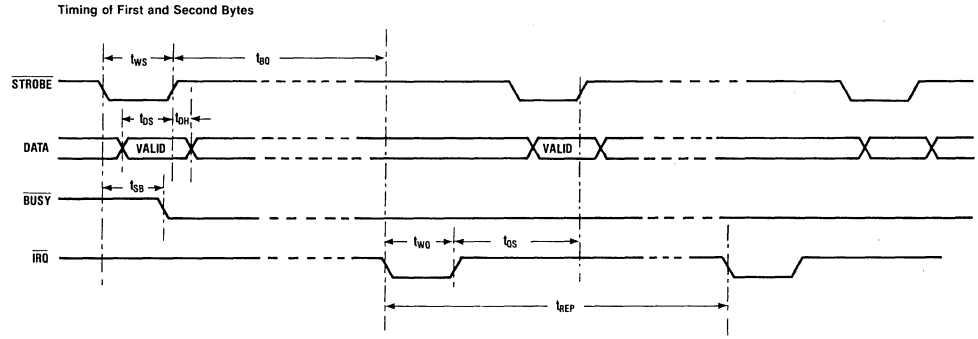
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Logic "1" Voltage	2.4		V_{DD}	V	
V_{IL}	Input Low Logic "0" Voltage	−0.3		0.8	V	
I_{IN}	Input Leakage Current			10	μA	V_{IN}=0 to V_{DD}
V_{OL}	Output Low Voltage Busy Output			0.4	V	I_{OL}=1.6mA
ΔV_{OA}	Output DC Offset Voltage, Audio			200	mV	
V_{OA}	DC Output Voltage, Audio		½V_{DD}			R_{LOAD}=100Ω
I_{DD}	Supply Current, Operating		25		mA	
I_{DDL}	Supply Current, Powerdown		0.75		mA	

AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
P_O	Audio Output Power		30		mW	R_{LOAD}=100Ω
t_{DS}	Data Set-Up Time	100			nsec	See Figure 1
t_{DH}	Data Hold Time	10			nsec	See Figure 1
t_{WS}	Strobe Pulse Width	0.5		100	μsec	See Figure 1
t_{SB}	1st Strobe to Busy Delay		100	500	nsec	See Figure 1
t_{BQ}	1st Strobe to 1st IRQ Delay		19		msec	See Figure 1
t_{REP}	IRQ Repetition Rate		250		μsec	See Figure 1
t_{WQ}	IRQ Pulse Width	3		3.5	μsec	See Figure 1
t_{QS}	IRQ to Strobe Delay[See Note 1]			200	μsec	See Figure 1
F_{OSC}	Oscillator Resonator Frequency	−1%	640	+1%	KHz	See Figure 1
R_{LOAD}	Audio Output Load Impedance		100		Ω	
C_{INOSC}	Input Capacitance, Oscillator		100		pF	
C_{IN}	Input Capacitance, Digital Interface		7		pF	

NOTE 1: Failure to respond to an IRQ with a new strobe within the specified period results in the chip going into the power down mode.

Figure 1. Timing Requirements



Pin Function/Description

Digital Interface

D_0 through D_7	**Data Inputs.** The speech data (in quantized form) is loaded on these lines in 8 bit bytes.
ST	**Strobe Input.** A rising edge on this input strobes in the data bytes. Enunciation will commence after the first frame of data has been loaded. If no strobe is received by the chip in response to an IRQ output then enunciation stops immediately and the chip goes into the power-down mode.
$\overline{BU}$	**Busy Output.** This open drain output signals that enunciation is in progress by going low.
$\overline{IRQ}$	**Interrupt Request Output.** This open drain output signals that the chip is ready to receive the next byte of data. Failure to respond within the prescribed time results in the chip going into the power-down mode.

Audio Interface

LS1 and 2	**Loudspeaker Outputs.** These pins are used to connect the chip to the loudspeaker. They are D.C. coupled and have an offset of half the supply voltage. The audio output is balanced on the two outputs.

Misc.

OSC_i, OSC_o	**Oscillator Input and Output.** A 640KHz ceramic resonator (MuRata CSB640A or equivalent) should be connected between these pins for normal operation, or an external 640KHz signal may be fed into OSC_i. When a resonator is used, a 120pF capacitor should be connected between OSC_i input and ground.
T_1, T_2, T_3	**Test Inputs.** These inputs should be left unconnected for normal operation.
V_{SS}	Most negative supply input. Normally connected to 0V.
V_{DD}	Most positive supply input.
A_{GND}	**Analog Ground.** An internally generated level approximately half way between V_{SS} and V_{DD}. A 0.047μF decoupling capacitor should be connected from this pin to V_{SS}. Do not connect this pin to a voltage supply.

Circuit Description

The main components of the S3620 LPC-10 Speech Synthesizer are shown in the block diagram.

Input Latch—This 8-bit latch stores the input data after the strobe pulse and loads it into the Coefficient Address Registers.

End of Word Decoder—This circuit detects the special code indicating that the last byte loaded in the Input Latch denotes the end of the speech word data and initiates the power down routine after the previous frame has been enunciated.

Buffer Registers—The data from the Speech Data ROM is assembled into frames and then decimated into the 12 parameters required for LPC-10 synthesis: pitch, gain and the 10 lattice filter coefficients. The parameters are stored in an encoded format and the decoding is done in the parameter value ROM. The coefficient address registers are used to store the assembled frame data and address this ROM.

Bit Allocation PLA—A programmable logic array is used to control the allocation of bits in the Buffer Register to the 12 parameters. The allocation and permissible variations are shown in Figure 2.

Parameter Value ROM—This ROM is used as a look-up table to decode the stored parameters into the LPC coefficients.

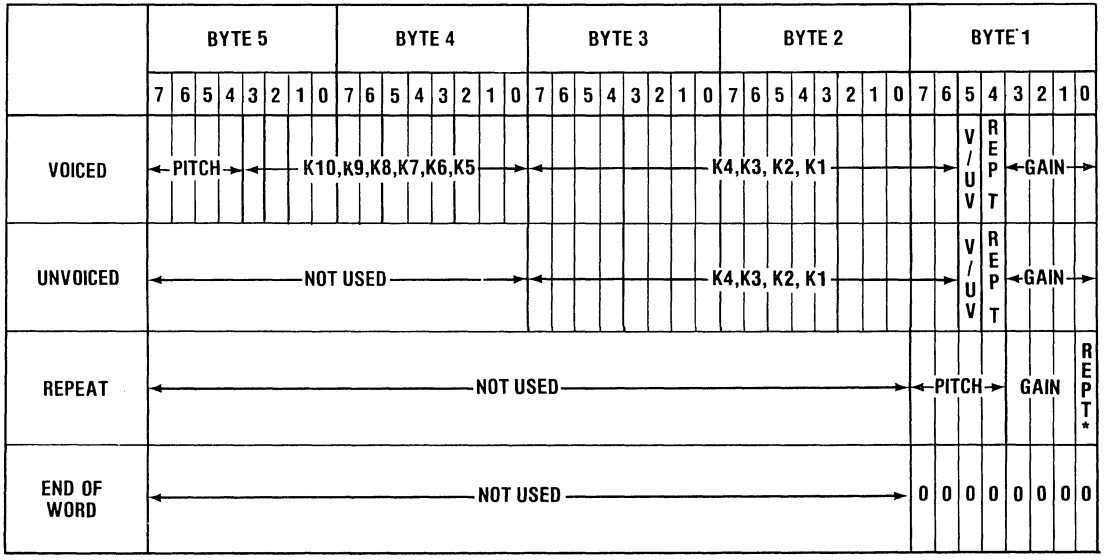
Interpolation Logic—The coefficients for each frame of speech, normally 20msec. are interpolated four times per frame to generate smoother and more natural sounding speech. Hence, the interpolation period is one quarter of a frame period, normally 5msec. After interpolation, the coefficients are used to drive the pitch-pulse source, the voiced/unvoiced switch, the lattice filter and the gain control. Interpolation is inhibited when a change from voiced to unvoiced speech, or vice versa, is made.

Pitch Register and Counter—This register stores the pitch parameter used to control the pitch counter.

Pitch-pulse Source—This is the signal source for voiced speech (vowel sounds). It is realized in switched-capacitor technology and generates symmetrical bipolar pulses at the rate specified by the pitch parameter and controlled by the pitch counter.

Pseudo-random Noise Source—This is the signal source for unvoiced speech (fricatives and sibilants) and consists of a 15-bit linear code generator giving a periodicity of 32767 sampling periods (4.096sec.). The output of this generator is scaled to a lower value and used as a random sign, constant amplitude signal.

Figure 2. Packed Quantized Data Formats



*NOTE: 0 = SINGLE (OR LAST) REPEAT. 1 = MULTIPLE REPEAT

Voiced/Unvoiced Speech Selector Switch—This switch determines whether the voiced or unvoiced signal source is used to drive the filter during a given frame.

LPC-10 Parameter Stack—This stack of 10 filter coefficients is used to control the lattice filter. The coefficients have an accuracy of 8-bits plus sign.

10 Stage Lattice Filter—The filter which simulates the effect of the vocal tract on the sound source (glottis) in the human speaker is realized here as a switched-capacitor (analog sampled data) 10 stage lattice filter. The filter parameters are determined dynamically by the time varying coefficients in the Parameter Stack and the filter operates at a sampling frequency of 8KHz (clock frequency/80).

Gain Controller—This controls the input signal level to the lattice filter to vary the sound level, and is an integral part of the lattice filter.

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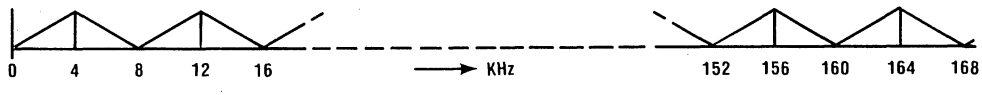
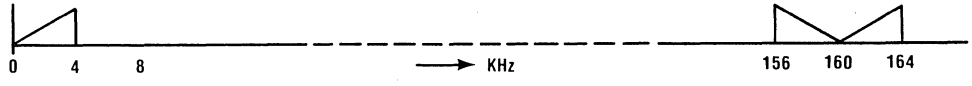
Power Amplifier—The amplifier brings up the level of the signal to give an output level of 30mW RMS into a 100Ω load. The output is a balanced bridge configuration with anti-phase signals on the 2 output pins.

Clock Generators and Power-down Control—This block contains the oscillator and timing circuits and also generates the analog ground reference voltage.

Figure 3.



(a) SPECTRUM OF SIGNAL OUTPUT OF LATTICE FILTER



(b) SPECTRUM OF SIGNAL AT OUTPUT OF INTERPOLATION FILTER.
NOTE: IN BOTH CASES A SIN x/x CHARACTERISTIC MODULATES THE SPECTRA. THIS IS OMITTED FOR SIMPLICITY.

Speech Data Compression

The data rate of the synthesizer input is 5400 bits/sec before interpolation (21600 bits/sec after interpolation) consisting of 12 parameters of 9 bits each repeated every 20msec. This is reduced to less than 2000 bits/sec for storage by means of a non-linear quantization technique. Each of the 12 coefficients is constrained to have a fixed set of values in an optimized manner. The actual values are dependent on the speech data and generated automatically in the analysis process. The parameters used to specify the coefficients are stored in the speech data ROM and used to address the coefficient look-up table ROM. The packing formats for the speech data are shown in Figure 2.

The speech data rate is further reduced by two other techniques shown in Figure 2. A substantial reduction is achieved by reducing the order of the lattice filter (the LPC order) to 4 during periods of unvoiced speech. This allows a 40% data reduction during these periods, which themselves typically account for 30-40% of speech (in the English language). A second reduction is obtained by detecting periods during which the filter parameters may be the same as those in the previous frame. Only the gain and pitch parameters are updated in such a frame, allowing an 80% data reduction.

Generation of Speech Data for the S3620

The speech data input to the S3620 is in a compressed format as explained in the previous section. AMI is able to provide a complete speech analysis service for this purpose and can supply the data on a diskette or programmed into EPROMs or mask programmed ROMs up to 128k bits. The speech sample should be provided to AMI on audio magnetic tape. Customers who have LPC speech analysis facilities and wish to generate their own data should contact AMI for further details of the quantization technique used and the availability of software to accomplish this.

Interfacing

The S3620 is designed to be easily interfaced to an 8-bit microprocessor system such as the S6800 as well as some 4-bit systems such as the S2000 family. The timing requirements are shown in Figure 1. A valid data byte should be present at the data input lines when the strobe line is taken to a logic 1 before the start of enunciation and in response to each $\overline{IRQ}$. The busy output may be used to identify the $\overline{IRQ}$ source during polling in a multiple interrupt system. A typical system configuration is shown in Figure 4. The S3620 occupies a single address in the microprocessor's memory space and data is loaded by writing it into that address after reading it from memory. The Address decode function may be realized using a PIA. An alternative interface technique is to write the data directly into the S3620 while reading it from the memory. This can be accomplished by mapping the S3620 into the entire address space of the speech data portion of the memory, so that the strobe is generated each time a byte of data is read from the speech memory. This can save hardware, as well as microprocessor instructions, since the loading of each byte is now accomplished in a single Read cycle instead of a Read cycle followed by a Write cycle. An example of this interfacing is shown in Figure 5, where the speech data occupies the memory addresses 0000 to 7FFF.

Applications

Toys and Games
EDP
Communications
Instrumentation
Industrial Controls
Automotive
Appliances

Figure 4.

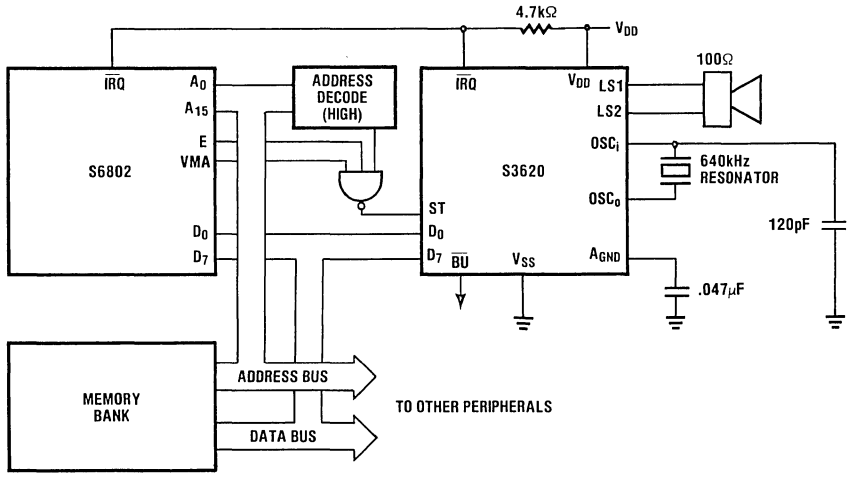
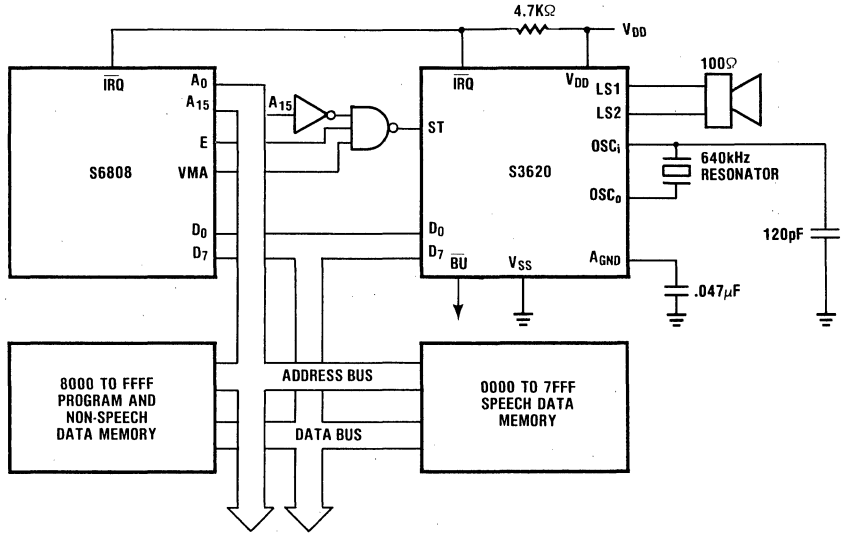


Figure 5.


4.7KΩ
VDD
100Ω
IRQ
A0
A15
E
S6808
VMA
D0
D7
A15
IRQ
VDD
LS1
LS2
ST
OSCi
S3620
640kHz
RESONATOR
OSCo
D0
D7
BU
VSS
AGND
120pF
.047μF
8000 TO FFFF
PROGRAM AND
NON-SPEECH
DATA MEMORY
ADDRESS BUS
DATA BUS
0000 TO 7FFF
SPEECH DATA
MEMORY

AMERICAN MICROSYSTEMS, INC.

S3630A/B

128K (16K×8) BIT NMOS ROM

Features

- ☐ Single +5V Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Directly TTL Compatible Outputs, Three State on S3630A
- ☐ Low Power: Supply Current-20mA Max.
- ☐ Power Down Capability (S3630A)

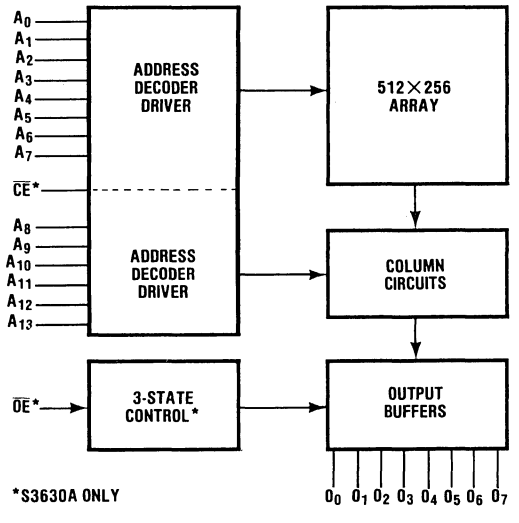
General Description

The S3630A/B is a high density 131072 bit NMOS mask programmable Read Only Memory. The device is fully TTL compatible and the organization as 16K×8 bits makes it very suitable for use in microprocessor systems. It is available in both 6μsec and 10μsec versions.

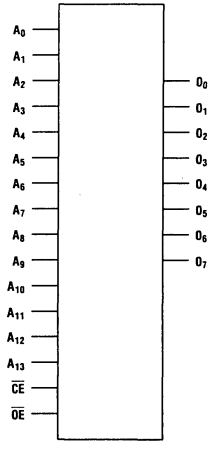
The S3630 is available in two pin configurations. The S3630A has the industry standard pinout (28-pin package). The S3630B has a minimum pin configuration, allowing it to be packaged in a 24-pin DIL pack, saving valuable board space where this configuration is usable, as well as reducing costs.

The S3630 is manufactured in a high density silicon gate, depletion load, N-channel process. Its high data capacity makes it extremely suitable for use in speech synthesis systems.

Block Diagram



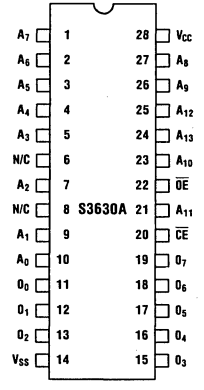
Logic Symbol



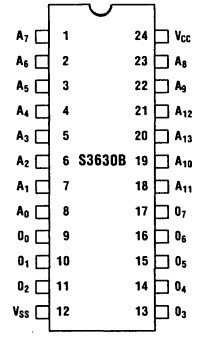
Pin Names

A_0-A_{13}	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable

Pin Configuration



N.C. = NO CONNECTION



Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... −10°C to 80°C
Storage Temperature ..... −65°C to 150°C
Output or Supply Voltages ..... −0.5V to 7V
Input Voltages ..... −0.5V to 6.5V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: ($T_A = -10°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 1.6mA$
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = 100\mu A$
V_{IL}	Input LOW Voltage	0		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		5.5	V	
I_{LI}	Input Leakage Current			10	μA	$V_{IN} = 0$ to 5.5V
I_{LO}	Output Leakage Current			10	μA	$V_O = 0.4V$ to 5.5V, @V_{CC} 0.4V or OPEN
I_{CC}	Power Supply Current		10	20	mA	
I_{CC}	Standby			3	mA	3630A

Capacitance: ($T_A = 25°C$, f = 1MHz.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
C_{IN}	Input Capacitance			7	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance			10	pF	$V_{OUT} = 0V$

A.C. Characteristics: ($T_A = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CEO}	Chip Enable Access Time S3630A S3630A-1			 6 10	 μsec μsec	See A.C. Conditions of Test and A.C. Test Load
t_{OE}	Output Enable Access Time S3630A and S3630A-1			350	nsec	
t_{OFF}	Output Deselect Time S3630A			350	nsec	
t_{AS}	Address Setup Time (S3630A)	0			nsec	
t_{AH}	Address Hold Time (S3630A)	1			μsec	
t_{CE}	$\overline{CE}$ Off Time (S3630A)	5			μsec	
t_{OV}	Access Time from V_{CC} On S3630B S3630B-1			 6 10	 μsec μsec	
t_{OFF}	Output Deselect Time S3630B			250	nsec	

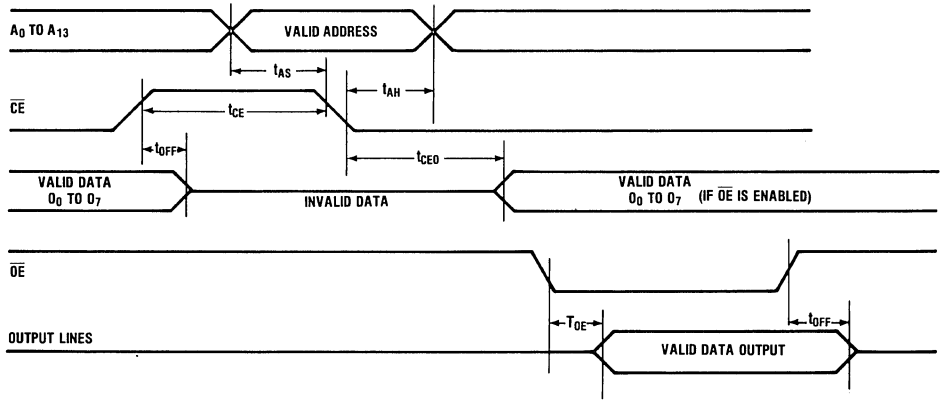
A.C. Characteristics: (Continued)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AS}	Address Set-Up Time S3630B			−200	nsec	
t_{AH}	Address Hold Time (S3630B)	2			μsec	
$V_{CC_{OFF}}$		100			nsec	

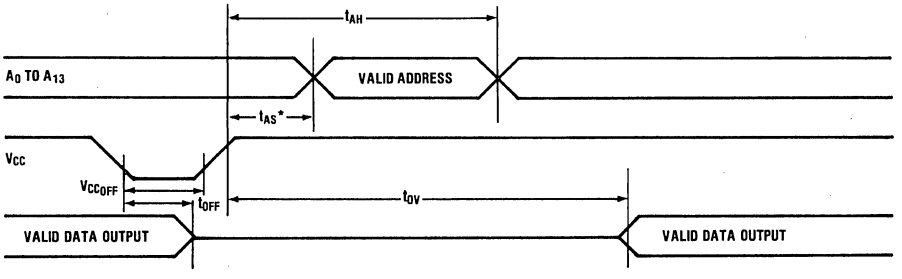
A.C. Test Conditions

Input Pulse Levels ..... 0.8 to 2.0V
V_{CC} Levels ..... 0 to 4.5V
Input/Output Timing Levels 1.5V
Output Load ..... 1 TTL Load and 100pF

3630A Timing Diagram



3630B Timing Diagram



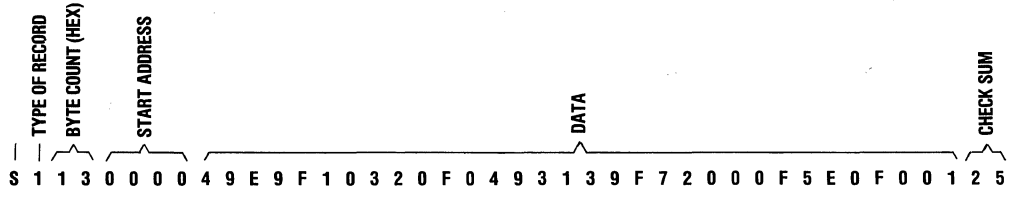
*t_{AS} MAY BE A NEGATIVE NUMBER SINCE THE ADDRESS DOES NOT HAVE TO BE VALID WHEN V_{CC} GOES ON BUT MAY OCCUR AFTERWARDS

Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI (see notes on page 4).

Position	Description
1	Start of record (Letter S)
2	Type of record 0—Header record (comments) 1—Data record 9—End of file record
3,4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5,6,7,8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9,...,N	Data Each data byte is represented by two hex characters. Most significant character first.
N+1,N+2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

EXAMPLE: S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C



NOTES:

Paper tape format is the same as the card format above except:

a. The record should be a maximum of 80 characters.
b. Carriage return and line feed after each record followed by another record.
c. There should NOT be any extra line feed between records at all.
d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

AMERICAN MICROSYSTEMS, INC.

Section 8.0

Application Notes

S2559 DTMF TONE GENERATOR

Applications of the S2559 DTMF Tone Generator

The S2559 Series DTMF Tone Generators were designed specifically for use in the implementation of the DTMF tone dialing push-button telephones. Other applications of the device include radio and mobile telephones, Remote Control, Point of Sale and Credit Card Verification Terminals, Alarm Reporting Devices, Automatic Dialers, etc. This application note describes design considerations, test methods and results obtained using the S2559 Tone Generator in these applications. For detailed specifications of the device refer to the S2559 Data Sheet.

Push-Button Dual Tone Telephone

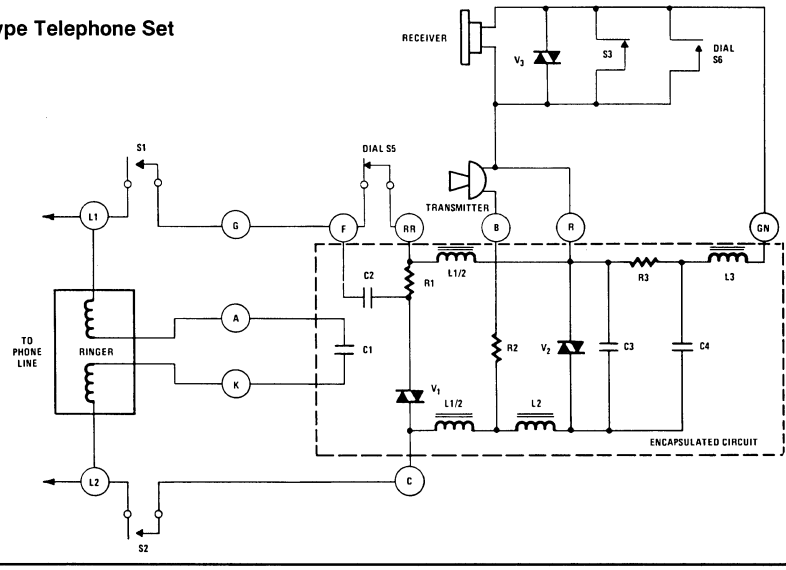
The primary application of the DTMF Tone Generator is in the design of a push-button dual tone telephone. To help explain how it can be used in a modified standard telephone, a description of the standard telephone is presented first.

Figure 1 shows the circuit diagram of a 500 type telephone set, an industry standard. Although there are various manufacturers of the 500 type telephone set, the internal circuitry is similar. Some manufacturers encapsulate all the active circuits with access provided at terminals only. The nomenclature of these terminals and their number may vary, depending upon the telephone model and its manufacturer.

The telephone set is composed of a transmitter, a receiver, an electrical network for equalization and associated circuitry to control sidetone and to connect power and signaling. The transmission circuitry of the telephone set is designed to separate the transmitter and receiver circuits to limit the amount of the talker's signal appearing in his own receiver (sidetone) and to block the direct current in the transmitter from the receiver. A controlled amount of sidetone is necessary for maintaining a natural conversation.

In the diagram of Figure 1, L1, L2 and L3 form a 3 winding transformer and V2, C3, R3, C4 form the sidetone balancing network. With the phone on-hook, hookswitch contacts S1, S2 are open and S3 is closed to protect the transmitter and receiver from ringing current from the central office to pass through the transmitter. When the phone is off the hook, contacts S1, S2 close, S3 opens and direct current flows in the transmitter. Capacitors in the

Figure 1. 500 Type Telephone Set



sidetone balance network prevent the direct current flowing in the transmitter from appearing in the receiver. During dialing, contact S6 across the receiver is closed to eliminate undesirable clicks and contact S5 interrupts the direct current at the dial pulse rate. Capacitor C2 forms a dial pulse filter to suppress high frequency interference into radio sets. Varistor V_3 suppresses clicks in the receiver. Varistors V_1 and V_2 are part of the equalizing network to reduce transmitting and receiving efficiency on short loops.

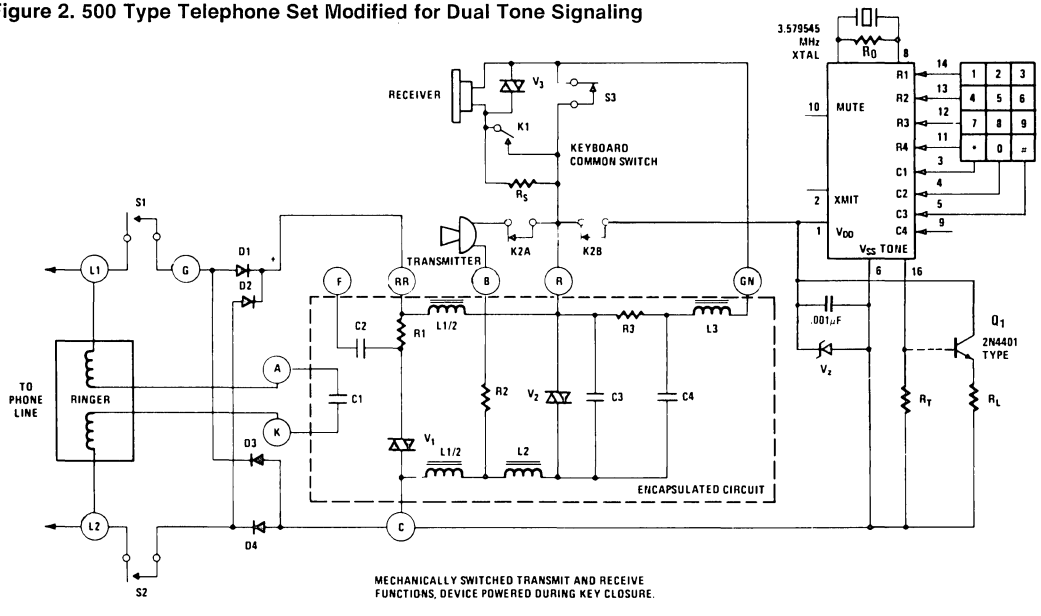
The varistors have a property of decreasing in resistance with increasing currents. On long loops the direct current from the central office battery is low; the varistor impedances are therefore high and the maximum telephone set efficiency is obtained. On short loops the high direct current results in low varistor impedances which shunt the speech currents and reduce the set efficiency. The overall effect is to make speech volumes at the central office and at the subscriber receivers less dependent on loop length.

The voltage developed in the local transmitter is divided in the windings L1 and L2 so that the voltages induced in the winding L3 are opposing. The voltage across the sidetone network resistance R3 arising from current flowing in winding L2 is arranged to oppose the resultant of voltages induced in L3. The overall effect of this balance is that the current in the receiver as a result of voltages developed in the transmitter is small and thus produces a low sidetone level. On the other hand, speech currents received from the loop pass through windings L1 and L2 and produce additive voltages in winding L3 which is connected to the receiver. These additive voltages are opposed by an approximately equal voltage 180° out of phase which results from the receiving current in winding L2. As a result there is little voltage drop across R3 and maximum receiving levels are obtained without appreciable power loss in resistor R3.

Implementation Using Mechanical Switching

Figure 2 shows how the circuit of Figure 1 can be modified to incorporate the DTMF Tone Generator eliminating the dial, adding a push-button keyboard to achieve a push-button dual tone telephone. It is seen that the device in-

Figure 2. 500 Type Telephone Set Modified for Dual Tone Signaling



MECHANICALLY SWITCHED TRANSMIT AND RECEIVE FUNCTIONS, DEVICE POWERED DURING KEY CLOSURE.

NOTES: i) RESISTOR R_0 NOT NEEDED FOR S2559 E, F, G OR H
ii) EMITTER FOLLOWER Q_1 IS BUILT IN ON S2559 G AND H

terfaces directly with the encapsulated circuitry without modification of it. Diodes D1 through D4 are inserted to insure that the polarity of the direct voltage across the device is the same even if connections to the phone terminals are reversed.

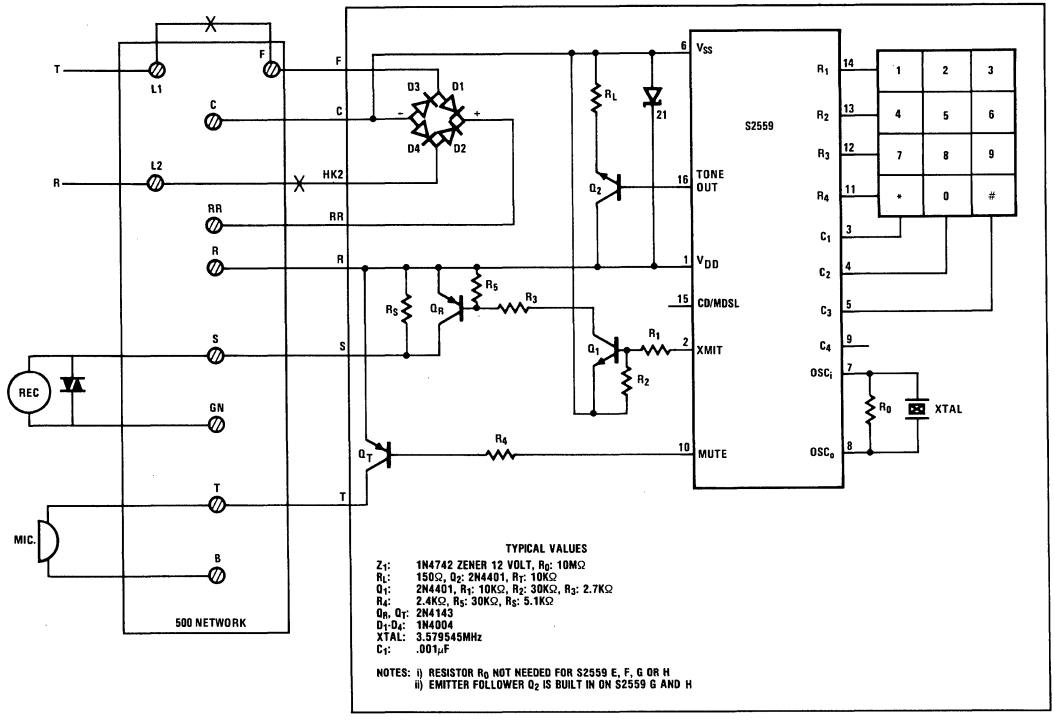
When the phone goes off-hook and a digit key is pushed, the device is powered up by the closure of common switch contact K2B. Zener V_Z insures that the voltage across the device will not exceed the maximum operating voltage. The recommended value for V_Z is 12 volts. Common switch K2A opens, removing the drive to the transmitter. The common switch K1 opens, which leaves the receiver connected through resistor Rs. Resistor Rs determines the amount of digit sidetone heard in the receiver. Typical value of Rs is 5.1KΩ.

The tone output of the device can be connected directly to the phone line through resistor R_T. To obtain tone amplitudes in the acceptable range, typically a resistor in the range of 100 ohms to 200 ohms is required. Lower resistor values produce higher amplitudes at the phone terminals but at increased distortion. An alternate way to produce higher amplitudes at the same time keeping distortion low is to use an emitter follower transistor, as shown in Figure 2. R_T is now increased to 10KΩ while R_L is chosen in the range of 100 to 200 ohms to produce the desired amplitude. Lower values of R_L tend to increase amplitude seen at the phone terminals as before.

Implementation Using Electronic Switching

Electronic switching using transistors can be employed to control the transmit and receive functions of the telephone as shown in Figure 3, which depicts an interface cir-

Figure 3. Tone Generator Interface Circuit

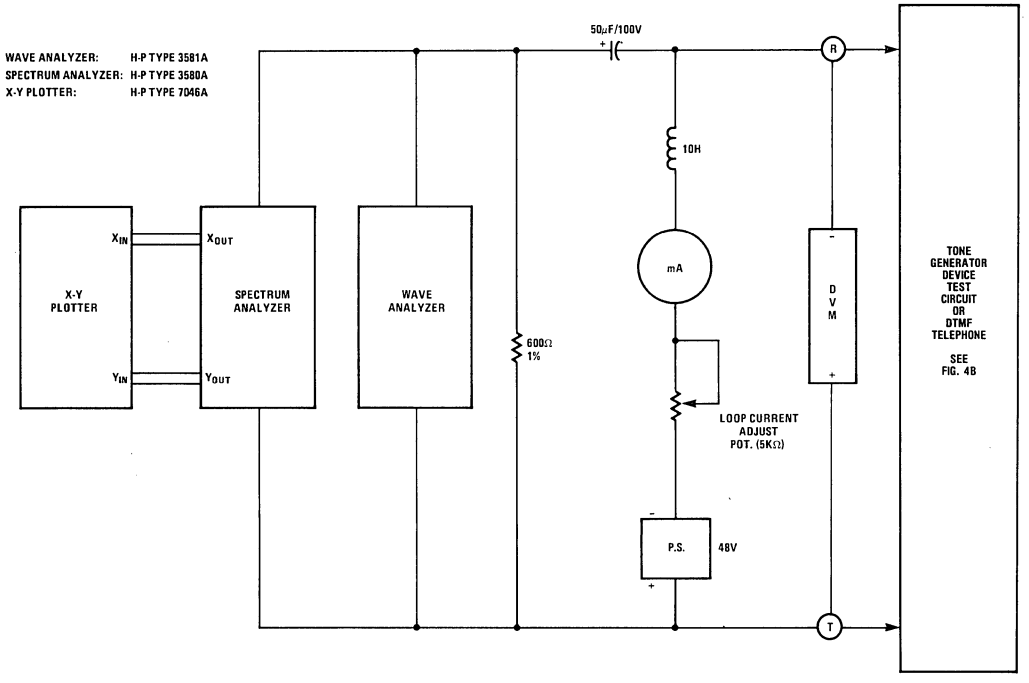


cuit for the 2500 type network. PNP transistors Q_T and Q_R are used as series contacts with the microphone and the receiver. In the tone dialing mode, transistors Q_T and Q_R are turned off, while in the voice mode they are turned "on". There is a slight loss in the transmission efficiency due to the finite "on" impedances of the transistors and due to base drive currents required by the two transistors for "hard switching".

Printed Circuit Board

An example of a PC layout for the tone generator is shown in the artwork section (Section II) of this Design Manual. See AW101.

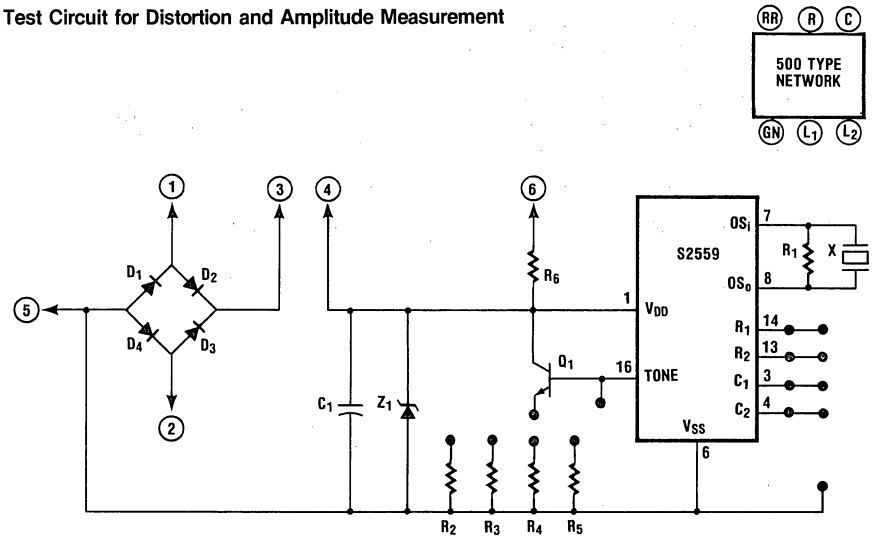
Figure 4A. Bench Method for Measurement of Amplitude and Distortion Performance



Performance Evaluation

The two major criteria in the evaluation of the DTMF Tone Generator in the telephone application are 1) the Amplitude/Loop Current characteristic, and 2) Distortion. Figures 4A and 4B show test circuits suitable for these measurements. Note that the circuit of Figure 4A allows simulation of DC Loop Conditions only. With this circuit, loop current can be varied over the range of 20mA to 80mA.

Figure 4B. Test Circuit for Distortion and Amplitude Measurement



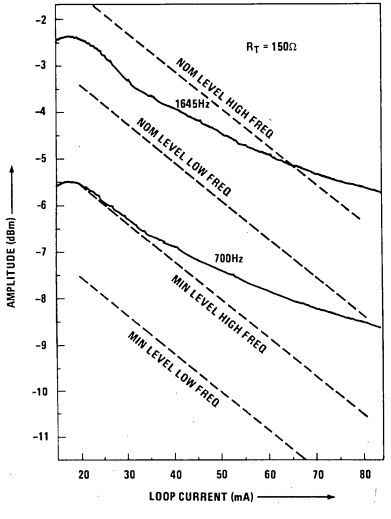
PARTS LIST

D_1-D_4	=	1N4004	R_4	=	130Ω
Z_1	=	1N4742	R_5	=	120Ω
C_1	=	.001μF	R_6	=	5.1k
R_1	=	10MΩ	Q_1	=	2N5550
R_2	=	180Ω	X	=	3.579545MHz CRYSTAL
R_3	=	170Ω			

WIRING CONNECTIONS

FROM	TO
1	L_1
2	L_2
3	RR
4	R
5	C

Figure 5. Typical Amplitude/Loop Current Plot for Circuit of Figure 2



Amplitude/Loop Current

Figure 5 shows a typical plot of amplitude vs loop current superimposed on the recommended AT&T specification (ref. 1) obtained using the circuit of Figure 2 with $R_T = 150\Omega$ (external emitter follower stage disconnected) in the test configuration of Figure 4. The absolute amplitude can be increased or decreased in a variety of ways. One way is to vary R_L. R_L typically will be in the range of 100 to 200Ω. Increasing R_L tends to decrease amplitude but improve distortion. Another alternative for increased amplitude is to use a bypass capacitor across R_L. This, however, tends to increase distortion. An emitter-follower transistor can be connected on the tone output. This allows increased amplitude and reduced distortion at the same time. These alternatives are shown in Figure 6. Use of the extra emitter-follower stage, however, decreases the amplitude slope characteristic. In general, a trade-off between amplitude, amplitude slope and distortion is necessary.

Distortion

The AT&T specification (ref. 1) reads "The total power of

Figure 6. Alternatives for Increasing Amplitude

all extraneous frequencies in the voiceband above 500Hz accompanying the signal should be at least 20dB below the level of the frequency pair." The key words here are the total power, voiceband and level of frequency pair. The voiceband is normally defined to be 300Hz to 3400Hz. Therefore, the total power of all extraneous components in the 500Hz to 3400Hz is of interest. The measurement of total power is not easy. To measure it precisely, first the total power of the DTMF signal with extraneous components in the 500Hz to 3400Hz band should be measured. The DTMF signal then should be removed by use of two notch filters centered around the appropriate low group and high group frequencies and the total power measured again. The ratio of the two readings gives a measure of distortion. An alternative is to plot a spectrum of the dual tone waveform and compute distortion using the following formula.

$$\text{Dist. (dB)} = 20 \log \frac{\sqrt{\sum_{i=1}^{n} (V_i)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\left\{\log\left[\sum_{i=1}^{n} (V_i)^2\right] - \log\left[(V_L)^2+(V_H)^2\right]\right\} \qquad (1)$$

Where V_L and V_H correspond to the rms voltage levels of the low group and high group signal components in the dual tone signal and V_i is the ith extraneous (either intermodulation or harmonic) component in the voiceband (500Hz to 3400 Hz). Individual component amplitudes in dB can be readily read off from the spectrum plot, converted to (rmsv)^2 by the use of the conversion chart shown in Table 1. Distortion is then calculated by use of equation (1), above.

Figures 7 and 8 show typical spectrum plots obtained in the test circuit of Figure 4 on a S2559D device in the circuit of Figure 3. Detailed distortion calculations on these spectrum plots are shown in Tables 2 and 3. The results show the distortion at 20mA loop current to be −24.9dB and at 30mA loop current −36.3dB. It is evident that distortion decreases rapidly as the supply voltage increases and as the modulation of the supply voltage decreases.

A rule of thumb for quick estimate of distortion is: As a first approximation, distortion in dB equals the difference between the levels in dB of the extraneous component with the highest amplitude and the low group signal component: or

Table 1. dB to (rmsV) and (rmsV)^2 Conversion Chart

dB	(rmsV)	(rmsV)^2	dB	(rmsV)	(rmsV)^2	dB	(rmsV)	(rmsV)^2	dB	(rmsV)	(rmsV)^2
−1.0	0.8913	0.79433	−20	0.1	0.0100000	−33	0.02238	0.0005012	−46	0.005011	0.0000251
−1.5	0.8414	0.70795	−21	0.089	0.0079433	−34	0.01995	0.0003981	−47	0.00446	0.0000199
−2.0	0.7943	0.63096	−22	0.07943	0.0063096	−35	0.01778	0.0003162	−48	0.00398	0.0000158
−2.5	0.7498	0.56234	−23	0.0707	0.0050119	−36	0.01584	0.0002512	−49	0.00354	0.0000126
−3.0	0.7079	0.50119	−24	0.063	0.0039811	−37	0.014125	0.0001995	−50	0.00316	0.0000100
−3.5	0.6683	0.44668	−25	0.0562	0.0031623	−38	0.01259	0.0001585	−51	0.002818	0.0000079
−4.0	0.6309	0.39811	−26	0.050118	0.0025119	−39	0.01122	0.0001259	−52	0.00251	0.0000063
−4.5	0.5957	0.35481	−27	0.0446	0.0019953				−53	0.00223	0.0000050
−5.0	0.5623	0.31623	−28	0.0398	0.0015849	−40	0.01	0.0001000	−54	0.00199	0.0000040
−5.5	0.53088	0.28184	−29	0.03548	0.0012589	−41	0.0089	0.0000794	−55	0.00177	0.0000032
−6.0	0.5012	0.25119				−42	0.00794	0.0000631	−56	0.00158	0.0000025
−6.5	0.4732	0.22387	−30	0.03162	0.0010000	−43	0.00707	0.0000501	−57	0.0014125	0.0000020
−7.0	0.4467	0.19953	−31	0.02818	0.0007943	−44	0.0063	0.0000398	−58	0.001259	0.0000016
−7.5	0.4217	0.17783	−32	0.0251	0.0006310	−45	0.00562	0.0000316	−59	0.001122	0.0000013

$$\text{Dist. (dB)} = V_{ih(dB)} - V_{L(dB)} \quad (2)$$

Using this rule of thumb gives estimates of −25dB and −37dB respectively for the loop currents of 20 and 30mA which are close to the computed values of −24.9dB and −36.3dB.

Figure 9 shows a plot of distortion vs loop current for various tone generators. It is seen that the S2559E and G have lower distortion than A and C devices and are recommended for new designs.

Figure 7. Typical Spectrum Plot of a S2559D Device in Circuit of Figure 3 with Test CKT of Figure 4

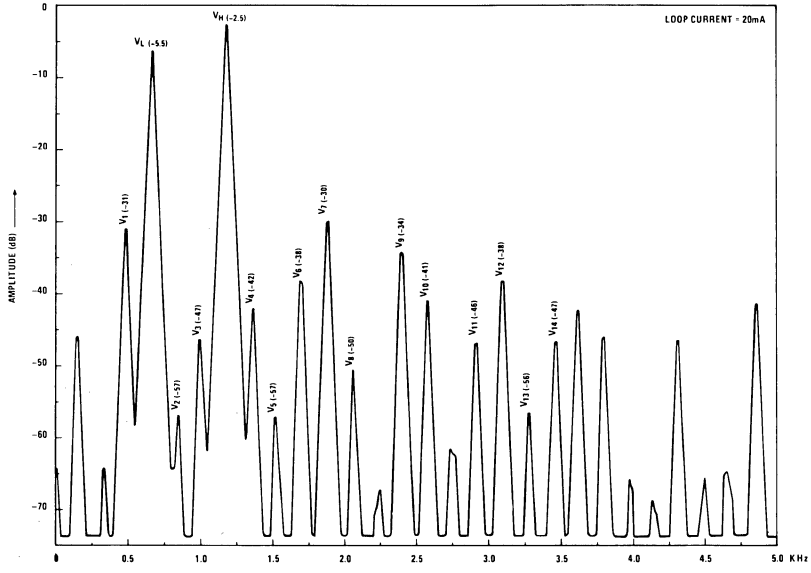


Figure 8. Typical Spectrum Plot of a S2559D in Circuit of Figure 3 with Test CKT of Figure 4

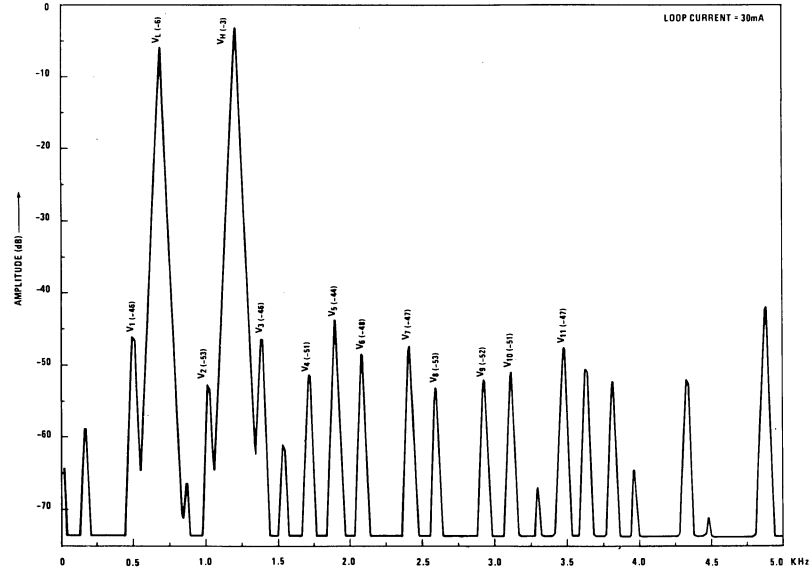


Table 2. Distortion Calculations for Spectrum of Figure 7 Device: S2559D in Circuit of Figure 3, Test Circuit Figure 4, 20mA Loop Current

Component	Measured (dB)	rmsV INV log $\frac{dB}{20}$	$(rmsV)^2$
V_L	−5.5		.2818434
V_H	−2.5		.5623434
V_1	−31		.0000794331
V_2	−57		.0000001995
V_3	−47		.0000019953
V_4	−42		.0000063314
V_5	−57		.0000001995
V_6	−38		.0001584585
V_7	−30		.0010000000
V_8	−50		.0000010000
V_9	−34		.0003981071
V_{10}	−41		.0000794714
V_{11}	−46		.0000025119
V_{12}	−38		.0001584585
V_{13}	−56		.0000002512
V_{14}	−47		.0000199539
V_{15}			.
$\sum_{i=1}^{n}(V_i)^2$			.0027333
$(V_L)^2+(V_H)^2$			.8441834

$$DIST = 20 \log \frac{\sqrt{\sum_{i=1}^{n}(V_i)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\left\{\log\left[\sum_{i=1}^{n}(V_i)^2\right] - \log\left[(V_L)^2+(V_H)^2\right]\right\}$$

$$= 10\left\{-2.56-(-0.074)\right\}$$

$$= -24.9dB\ (5.7\%)$$

Table 3. Distortion Calculations for Spectrum of Figure 8 Device: S2559D in Circuit of Figure 3, Test Circuit Figure 4, 30mA Loop Current

Component	Measured (dB)	rmsV INV log $\frac{dB}{20}$	$(rmsV)^2$
V_L	−6.0		.2511834
V_H	−3.0		.5011834
V_1	−46		.0000251189
V_2	−53		.0000050119
V_3	−46		.0000251189
V_4	−51		.0000079433
V_5	−44		.0000398398
V_6	−48		.0000158489
V_7	−47		.0000199539
V_8	−53		.0000050119
V_9	−52		.0000063314
V_{10}	−51		.0000079433
V_{11}	−47		.0000199539
V_{12}			.
V_{13}			.
V_{14}			.
V_{15}			.
$\sum_{i=1}^{n}(V_i)^2$			.0011771779
$(V_L)^2+(V_H)^2$			.7523636

$$DIST = 20 \log \frac{\sqrt{\sum_{i=1}^{n}(V_i)^2}}{\sqrt{(V_L)^2+(V_H)^2}}$$

$$= 10\left\{\log\left[\sum_{i=1}^{n}(V_i)^2\right] - \log\left[(V_L)^2+(V_H)^2\right]\right\}$$

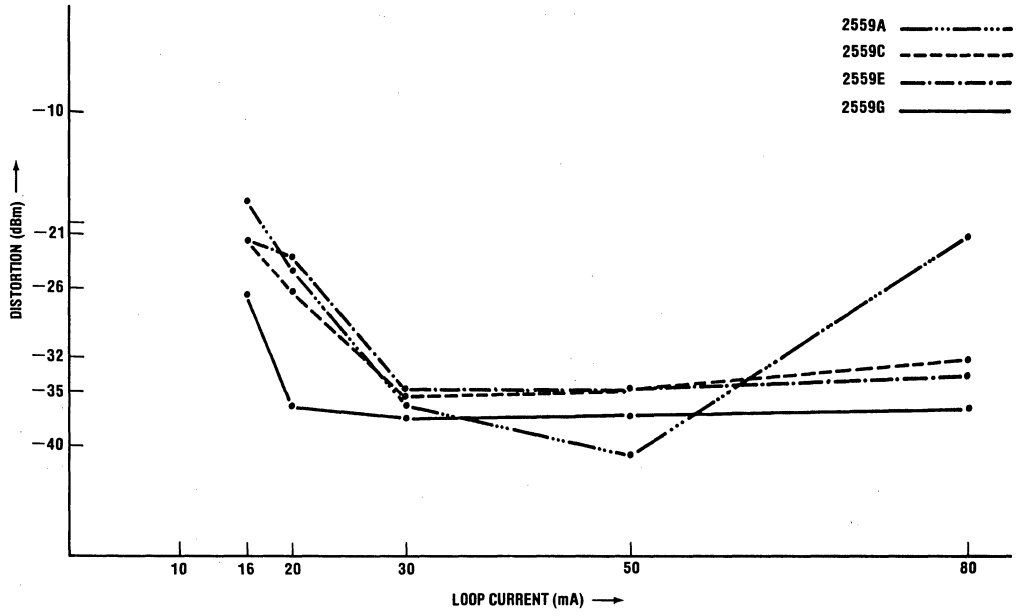
$$= 10\left\{-3.75-(-0.124)\right\}$$

$$= -36.3dB\ (1.5\%)$$

Other Considerations

The supply voltage available to the Tone Generator is a function of the DC loop current flowing through the telephone network and the DC impedance presented by the network. The insertion of the diode bridge and voltage drop in the transformer winding further reduce the available voltage. Typically, the DC voltage available to the device is 1.7 volts less than that measured at the TIP and RING terminals. The instantaneous minimum voltage as seen by the device is even smaller because of the DTMF signal riding on the DC component. The instantaneous minimum voltage can be expressed as $V_{min} = V_{dc} - V_{ac}$ (peak). Because the signal amplitude is larger at lower loop currents, i.e., at lower DC voltages, the instantaneous minimum voltage is significantly less than the average voltage measured across the device. This causes higher distortion at lower loop currents.

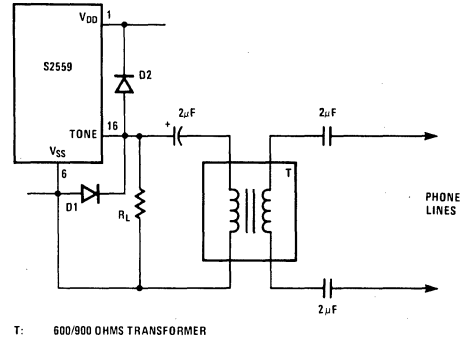
Figure 9. Distortion Vs. Loop Current



The DC voltage across the device is under the designer's control during DTMF dialing. The AT&T specification (ref. 1) recommends a minimum DC voltage of 6 volts (4 volts preferred) across the TIP and RING during voice and initial off-hook condition at a loop current of 20mA. However, during DTMF dialing, the DC voltage is permitted to increase to 8 volts (6 volts preferred). The designer can take advantage of this specification to insure adequate voltage across the device at low loop currents. Even with a preferred 6 volt specification, allowing for 1.7 volts drop in the bridge and transformer winding, the average voltage across the device will be at least 4.3 volts. The instantaneous minimum voltage will not drop significantly below 3.6 volts, assuring good distortion performance down to lower loop currents. The voltage across the device can be increased by allowing the telephone DC impedance to increase during DTMF signaling. Since the microphone is switched out during signaling, this is direc tly a function of the DC current drawn by the device. Since the DC current required by the device is low, it is primarily a function of the load R_L. Increasing R_L will increase the DC impedance and thereby increase the average supply voltage, thus reducing distortion. Increasing R_L, however, reduces signal amplitude so a trade off has to be made between amplitude and distortion.

Consideration should also be given to insure adequate base drive to the external transmit and mute transistors when operating at low loop currents if electronic switching is used.

Figure 10. Transformer Coupled Phone Interface



T: 600/900 OHMS TRANSFORMER
D1, D2: 1N914 TYPE DIODES
R_L: 1K Ω TYP.

Transient Voltage Protection

An important consideration in the design of electronic equipment to be connected to the telephone network is that adequate transient voltage protection circuitry must be incorporated such that the equipment can withstand lightning surges without causing harm to the telephone network. In particular, all equipment must meet the metallic and longitudinal surge voltage specifications outlined in the FCC part 68 (ref. 2).

When applied to tone generator interface circuits, such as those in Figures 2 and 3, transient voltage protection requires proper selection of components for the diode bridge and the zener diode. It is necessary that the diode bridge utilize high voltage breakdown and high current capacity diodes. 1N4004 type diodes may be adequate but higher rated diodes might be required.

Selection of the zener diode depends upon its transient response characteristic. A slow zener diode will not clamp voltage to its rated value. However, it should be noted that the S2559 Tone Generator can withstand pulse voltages that exceed the absolute maximum continuous DC voltage ratings (10.0V for S2559C, D; 13.5V for S2559A, B). Typically, the S2559 devices can withstand up to 20 volts of pulse voltages for durations of less than 1ms. It should also be noted that the zener diode and the device are behind the network transformer winding and not directly across the telephone terminals. These considerations allow selection of a wide range of zener diodes as protection elements. A zener diode of the type 1N4742 may be adequate in most cases.

Ancillary Interface to Phone Lines

The DTMF Tone Generator can be used in ancillary station apparatus (such as alarm reporting devices, automatic dialers, data terminals, etc.) for tone dialing or low speed data transmission applications. A transformer interface, such as that shown in Figure 10, can be used. Consideration must be given to the device latch up possibility due to induced voltage spikes in the transformer winding connected to the tone output. Latch up can be prevented by diode clamping the tone output to V_{DD} and V_{SS}.

Call Progress Tone Generation

The DTMF Tone Generator can be used in other single or multitone applications by selecting a crystal of appropriate frequency. The precise dial tone is defined to be a multifrequency tone consisting of 350Hz and 440Hz. By selecting a crystal of 1.307112MHz, a dial tone of 346Hz and 444Hz can be obtained by activating the R4, C1 inputs of the device. Other call progress tones such as busy and ringback tones can be similarly generated as shown in Table 4.

Table 4. Call Progress Tone Generation Using S2559

TYPE OF TONE	DESIRED FREQUENCY (Hz)	CRYSTAL NEEDED (MHz)	ROW-COLUMN CONNECTION	ACTUAL FREQUENCY (Hz)
DIAL	350 + 440	1.307112	R_4, C_1	346 + 444
BUSY/REORDER	480 + 620	1.820891	R_4, C_1	482 + 618
RINGBACK*	440 + 480	1.307112	R_1, R_2, C_1 R_1, R_2, C_2	444 + 486
*TWO S2559s EACH OPERATING IN SINGLE TONE MODE ARE NEEDED				

References

Ref. 1: Bell System Communications Technical Reference (PUB 47001). *Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment.* August 1976.

Ref. 2: Rules and Regulations, FCC part 68. *Connection of Terminal Equipment to the Telephone Network.* July 1977.

S3501/S3502, S3503/S3504

SINGLE CHANNEL A-LAW & μ-LAW PCM CODEC/FILTER SETS

System Design Guidelines

The Codec Chip sets are required to handle signals with a very large dynamic range. The smallest signals that the devices have to resolve are thousands of times smaller than TTL and other digital signal amplitudes. Therefore, to achieve optimal analog performance requires careful attention to positioning and layout of components.

The following general guidelines should be followed:

1) The analog ground, digital ground, V_{DD} and V_{SS} busses should be independent to the power supply (or at least up to the edge connector).

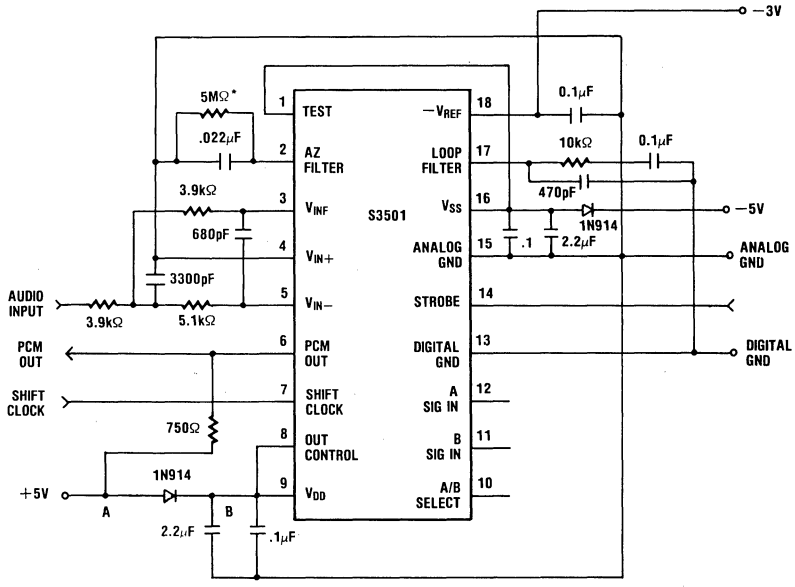
2) These busses should be separate for each chip (and should be kept as wide as possible on a printed circuit).

3) The connections should be as independent as possible. For example (see Figure 1): the 750Ω pull-up resistor to pin 6 should join the V_{DD} supply at the edge connector (and not at the device pin). To reduce current drain at slower clock rates the pull-up resistor value can be increased.

4) Decoupling capacitors (specially for V_{DD}) should be as close to the power supply pin and analog ground pin as possible. (0.1μF capacitor to be closest). Suitable decoupling is also required at the edge connector of power supply.

5) Digital signal lines should be kept away from analog signals and separated by an analog ground line for shielding where possible.

Figure 1. Hookup Schematic for S3501 Using 1.544mHz Shift Clock Rate



S3501/S3503 Design Guidelines

A recommended encoder schematic is shown in Figure 1. Parts of the circuit are discussed in more detail below.

Loop Filter Network—For shift clock rates above 512kHz the network in Figure 2 is recommended. For 512kHz or below a .1μF capacitor between pins 13 and 17 is sufficient.

Supply Decoupling—Figure 3 shows the recommended power supply decoupling circuits. The diodes are essential for ±5V power supplies if maximum performance is desired.

Reference Voltage—Pin 18 requires a .1μF capacitor to analog ground. Pin 2, AZ filter, requires a .022μF capacitor to analog ground in parallel with 5MΩ resistor (250k on 53503).

Anti-Aliasing

In applications where anti-aliasing pre-filtering is required, an on-chip op-amp may be configured into an active filter (Figure 4). Note that small changes in gain can be made by adjusting the resistor ratio R_1/R_2. Where anti-aliasing is not needed, a 3KΩ-4KΩ resistor can be connected between pins 3 and 5 (inverted gain configuration).

S3502/S3504 Design Guidelines

Figure 5 depicts a recommended decoder circuit. All of the following comments apply to Figure 5: A_{OUT} and B_{OUT} are connected to V_{DD} through pull-up resistors. R should be larger than 10KΩ to reduce noise.

When pin 1 is connected to DGND (non-inverted signalling with T²L output levels; not shown in Figure 5), R >47KΩ.

Pin 1 should be connected to pin 10 to avoid forward biasing the pin.

The 512KΩ output amplifier resistors should be carefully positioned away from the digital signals.

Test Mode Operation

When in TEST mode, the internal autozero is disabled since the feedback between the encoder and filter is interrupted. When testing the encoder, an external autozero loop is required to cancel its offset. When testing the filter alone, the AZ FILTER pin should be tied to AGND. This nulls out the open loop voltage on the autozero capacitor.

The filter output should be sampled by a narrow strobe occurring 15μs after the rising edge of the strobe input on pin 14.

Loading on pin 15 V_{OUTH} (S3502/S3504)

Resistive load on pin 15 should be 39kΩ or greater.

Figure 2. Selection of Loop Filter Network

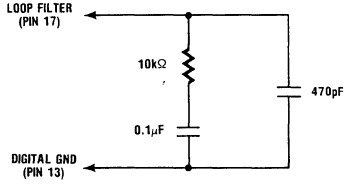


Figure 3-B. Supply Decoupling for the V_{SS} Supply Pin

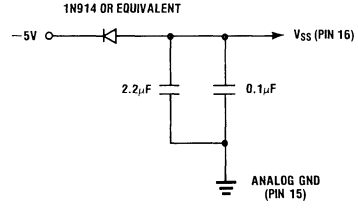


Figure 3-A. Supply Decoupling for the V_{DD} Supply Pin

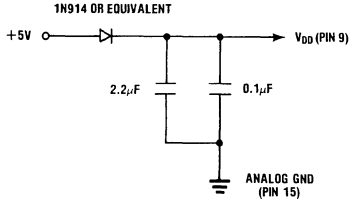


Figure 4. Anti-Aliasing Filter

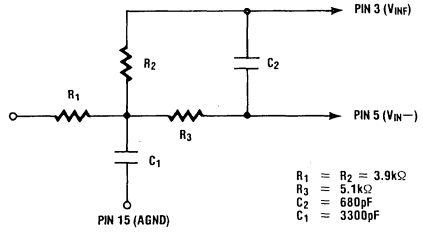
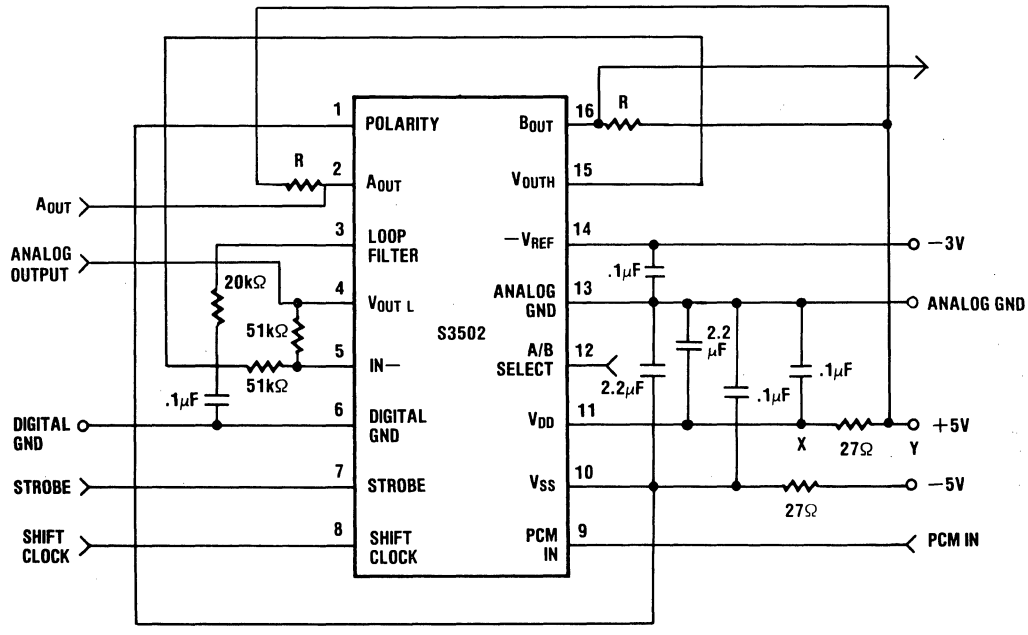


Figure 5. Hookup Schematic for S3502 Using 1.544mHz Shift Clock Rate



Performance Evaluation

The key parameters in the evaluation of the Codec set are: gain tracking, idle channel noise, quantization distortion ratio and frequency response. All these parameters can be measured in an end to end test by comparing the input audio signal to the Encoder with the output audio signal from the Decoder. In this test PCM output of the Encoder is connected to the PCM input of the Decoder. A typical test set up using the HP3779B Primary Multiplex Analyzer is shown in Figure 6. Note that a unity gain buffer amplifier using a low noise Op Amp should be inserted in series with the Decoder output to eliminate capacitive loading effects of the measuring instrument and long coaxial cable.

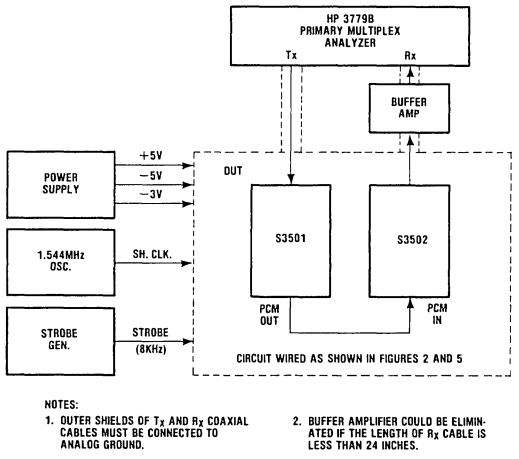
With V_{REF}= −3.0V, the S3502 decoder output at V_{OUTH} pin for a "digital milliwatt" signal applied at the PCM IN pin is about +4.9dBm. Thus $OTLP_{OUT}$ for the Codec set is +4.9dBm. For component values shown in Figures 1 and 5, the thru gain in the end to end test is a little less than unity. Therefore, OdBmO at the input will be about +5.4dBm. Exact level should be determined for the unit under test using the digital milliwatt method. Care should be taken to set up the measuring instrument to take into account the OTLP for the Codec set.

HP3779B System Parameters are:

	dBr IN	dBr OUT	Single Channel Interface
S3501/S3502	5.4	4.9	1.544MHz Clock rate
S3503/S3504	5.4	4.9	2.048MHz Clock rate

Typical results using the test set up of Figure 6 are shown in Table 1.

Figure 6. Test Setup for Codec Evaluation (End-to-End)



NOTES:

1. OUTER SHIELDS OF T_X AND R_X COAXIAL CABLES MUST BE CONNECTED TO ANALOG GROUND.
2. BUFFER AMPLIFIER COULD BE ELIMINATED IF THE LENGTH OF R_X CABLE IS LESS THAN 24 INCHES.

Table 1. Typical Results with Test Set up of Figure 6.

GAIN v LEVEL -tone		A-A 1/ 1
FREQUENCY	(kHz):	1.02
REF LEVEL	(dBm0):	−10.0

CHAN	LEVEL (dBm0)	LIMITS (dB) LOWER	UPPER	MEASUREMENT RESULTS		*IF FAIL
1	−55.0	−3.00	3.00	RESULT (dB):	0.13	
	−50.0	−1.00	1.00	RESULT (dB):	0.08	
	−45.0	−1.00	1.00	RESULT (dB):	−0.07	
	−40.0	−0.50	0.50	RESULT (dB):	−0.09	
	−35.0	−0.50	0.50	RESULT (dB):	−0.12	
	−30.0	−0.50	0.50	RESULT (dB):	−0.08	
	−25.0	−0.50	0.50	RESULT (dB):	−0.04	
	−20.0	−0.50	0.50	RESULT (dB):	−0.02	
	−15.0	−0.50	0.50	RESULT (dB):	0.01	
	−10.0	−0.50	0.50	RESULT (dB):	−0.01	
	−5.0	−0.50	0.50	RESULT (dB):	0.03	
	0.0	−0.50	0.50	RESULT (dB):	0.11	
	3.0	−0.50	0.50	RESULT (dB):	−0.10	

GAIN		A-A 1/ 2
FREQUENCY	(kHz):	1.02
LEVEL	(dBm0):	0.0
LOWER LIMIT	(dB):	−0.50
UPPER LIMIT	(dB):	0.50

CHAN	MEASUREMENT RESULTS		*IF FAIL
1	RESULT (dB):	−0.03	

Table 1. Typical Results with Test Set up of Figure 6. (Continued)

IDLE CHAN NOISE C-MES A-A 1/ 4

UPPER LIMIT (DBrnC0): 23.0

CHAN	MEASUREMENT RESULTS		*IF FAIL
1	RESULT:	14.7	
2	RESULT:	14.6	

QUANT DIST -tone A-A 1/ 5

FREQUENCY (kHz): 1.02

CHAN	LEVEL (dBm0)	LOWER LIMIT (dB)	MEASUREMENT RESULTS		*IF FAIL
1	−45.0	22.0	RESULT (dB):	27.4	
	−40.0	27.0	RESULT (dB):	30.4	
	−35.0	30.0	RESULT (dB):	34.1	
	−30.0	33.0	RESULT (dB):	35.4	
	−25.0	33.0	RESULT (dB):	35.7	
	−20.0	33.0	RESULT (dB):	39.1	
	−15.0	33.0	RESULT (dB):	38.3	
	−10.0	33.0	RESULT (dB):	37.8	
	−5.0	33.0	RESULT (dB):	38.5	
	0.0	33.0	RESULT (dB):	38.3	

GAIN v FREQUENCY A-A 1/ 6

REF FREQ (kHz): 1.02

LEVEL (dBm0): 0.0

CHAN	FREQ (kHz)	LIMITS (dB) LOWER	UPPER	MEASUREMENT RESULTS		*IF FAIL
1	0.21	*****	0.50	RESULT (dB):	−0.89	
	0.31	−0.50	0.50	RESULT (dB):	0.11	
	0.61	−0.50	0.50	RESULT (dB):	0.10	
	0.91	−0.50	0.50	RESULT (dB):	0.03	
	1.21	−0.50	0.50	RESULT (dB):	−0.04	
	1.51	−0.50	0.50	RESULT (dB):	−0.05	
	1.81	−0.50	0.50	RESULT (dB):	−0.01	
	2.11	−0.50	0.50	RESULT (dB):	0.05	
	2.41	−0.50	0.50	RESULT (dB):	0.04	
	2.71	−0.50	0.50	RESULT (dB):	−0.04	
	2.99	−0.50	0.50	RESULT (dB):	−0.03	
	3.39	−1.80	0.50	RESULT (dB):	−1.37	
	3.59	*****	0.50	RESULT (dB):	−7.84	

AMI CODEC PERFORMANCE EVALUATOR

CODEC Performance Evaluator Operation

The CODEC Performance Evaluator box provides an opportunity to check CODEC performance. It eliminates the difficulties and noise inherent in a wire-wrap breadboard.

The basic PCM timing signals are all provided by a self-contained logic card. The shift rate is either 1.544MHz or 2.048MHz, depending on the box. The CODEC chip plugs into a clean, well designed PC board, minimizing noise. This card is keyed so it cannot be inserted the wrong way into the socket of the Evaluator.

The box has a self-contained power supply. Banana jacks are provided for measuring current consumption or using external power supplies. BNC jacks are available to monitor Strobe, Shift Clock, and A/B Select with a scope.

For end-to-end testing, an audio signal is applied to the Analog In Jack and measured at the Analog Out Jack provided the PCM In and Out jacks are looped together. If A to D or D to A is desired, the PCM is available and external test equipment may be synchronized to the signals available at the BNC Jacks (Strobe, Clock).

The standard A/B signaling format is available in simple format. When the A/B Select switch is in the "ON" position, the 8th bit of the signaling frames carry whatever is set in the A IN and B IN switches. In this fashion Idle Channel Noise and Quantizing Distortion can be compared under both signaling and no signaling conditions.

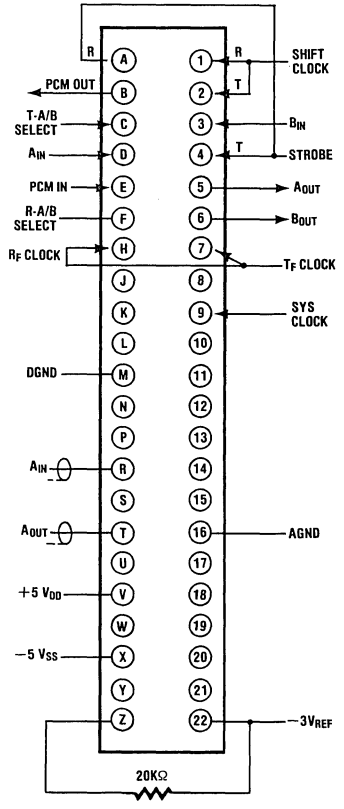
The Reset Button is to reset the Evaluator's internal logic card in the event of a power-up problem. It is not related to the CODEC chips but only the logic card providing the PCM shift clock and strobe timing.

The Strobe Switch allows the 8KHz strobe to the device to be switched off, putting the CODEC into the power down mode. The operating vs. standby current can be measured at the power supply banana jacks by turning the strobe on and off.

In making measurements of the various CODEC's performance it must be remembered that 0TLP is different for different versions. The exact 0TLP should be determined from the proper data sheet and then used to correct the readings (Example: A 21dBrncO idle channel noise measurement may actually be 21-4.9=16.1dBrncO).

The CODEC demonstration boards are illustrated in the Artwork section (Sec. 11) of this manual showing the parts layouts and valves. See AW 201, 202, 203.

CODEC DEMO BOX EDGE CONNECTOR



THIS PRINT IS FOR ALL VERSIONS OF CODEC PERFORMANCE CARDS. NO ONE CARD USES ALL THESE CONNECTIONS. SEE THE SPECIFIC CARD SCHEMATIC FOR EXACT REQUIREMENTS (AW201, 202, 203).

USING THE S3525A/B DTMF BANDSPLIT FILTER

Introduction

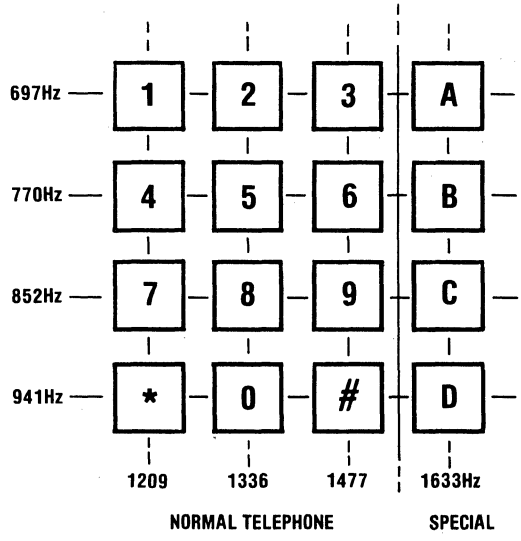
DTMF (Dual-Tone, Multi-Frequency) or Touch-Tone®, is widely used for controlling and signaling. Bell System originally designed this signaling method to provide customers with a more rapid, convenient means of transmitting digits of the called party phone to the central office. Now, it is used in many other applications.

Pushing a button produces 2 tones simultaneously. It is this particular set of tones that the DTMF Receiver at the telephone central office (or exchange) uses to determine which button was pushed (see Figure 1). By analyzing the series of tones sent, the receiver determines what number was dialed and the switching equipment then acts accordingly.

The requirements for accuracy and reliability in the telephone network have been well defined. As a result a DTMF Receiver for a central office must have high quality and reliability.

The performance of DTMF in the telephone network is well appreciated by designers of other systems evidenced by the familiar Touch-Tone® pad present on radios, remote credit card terminals, electronic bank tellers, etc. These applications take advantage of the end-to-end capability inherent in the DTMF method. The tones, like voice, go from the originating end to the receiving end without significant degradation.

Figure 1. DTMF Keyboard



Using the S3525

Crystal Oscillator

The S3525 crystal oscillator circuit requires a 10 Meg ohm resistor in parallel with a standard 3.58MHz television colorburst crystal. For this application, however, crystals with relaxed tolerances can be used. Specifications can be as follows:

Frequency	3.579545 ±.02%
RS≤180Ω	L_M~96MH
C_L=18pF	C_h=7pF

Alternate Clock Configurations

If 3.58MHz is already available in the system it can be applied directly as a logic level to the OSC_{IN} (pin 16). [Max. zero~30% V_{DD}, min. one~70% V_{DD}]. Waveforms not satisfying these logic levels can be capacitively coupled to OSC_{IN} as long as the 10 Meg ohm feedback resistor is installed as shown in Figure 2.

The S3525A provides a buffered 3.58MHz signal from the on-chip oscillator to external decoders or other devices requiring 3.58MHz. The S3525B provides a buffered ÷4 output at 895kHz to drive certain tone decoders and microprocessors. If both frequencies are required in a system, the 3.58MHz can be capacitively coupled as shown in Figure 2A or 2B.

Figure 2A. S3525B Driving MK5103

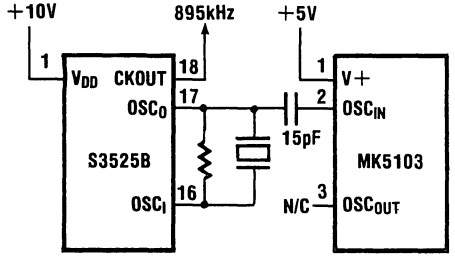
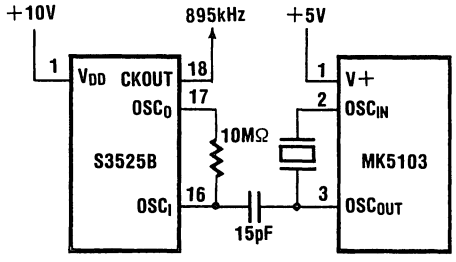


Figure 2B. MK5103 Driving S3525B Supply Pin



Input Configurations

The S3525 operates either from a single or dual power supply. It has a differential input Op Amp. Therefore, the input configuration depends on the power supply and the signal source characteristics. Figures 3 and 4 give some configurations for both balanced and unbalanced signal sources. An on-chip voltage divider provides a reference voltage at 1/2 (V_{DD}-V_{SS}) to the internal circuitry. It is also provided at pin 3.

Since the filter has about 6dB of gain, to keep the filter outputs (pins 14, 15) out of clipping for maximum linearity, the level at pin 13 should be kept to 3/8 (V_{DD}-V_{SS})≤V_{PP} ≤5/8 (V_{DD}-V_{SS}). This will keep distortion at a minimum. However, since these analog outputs typically drive comparators to do the squaring function, exceeding these limits will still give good performance.

Figure 3 shows an input configuration for either balanced or unbalanced, high impedance or terminated connection. When used with a 600Ω balanced line, the input is at point (A) and the terminating 600Ω is installed. When used with an unbalanced line, the input is at point (B(and the transformer is deleted. The terminating resistor may or may not be used depending on the desired load to be presented to the line. The feedback resistor R_f is selected to maintain the proper value at pin 13 for the maximum signal level received from the line.

Figure 4 illustrates an input configuration for a 600Ω balanced line terminated at the DTMF receiver. This eliminates the capacitor of Figure 3.

Figure 5 provides a method of bridging a balanced line without a transformer to provide a high impedance input with common mode rejection of 60Hz or other noise on the line. The values given are commonly available EIA values. Better precision or balance can be obtained with 1% resistor values if required.

Figure 3.

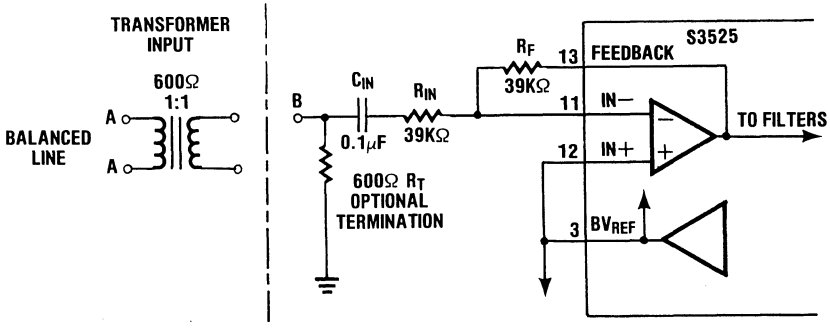


Figure 4.

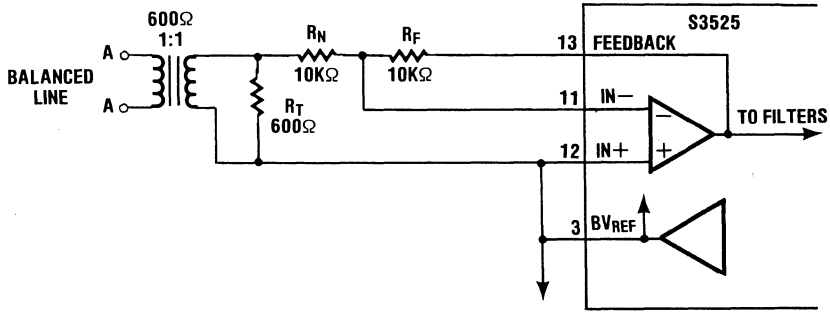
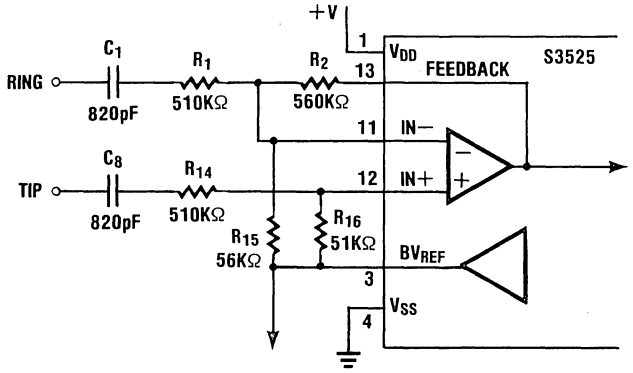


Figure 5.



Output Configurations

The S3525 has analog outputs for low group and high group tones available for circuits requiring analog or sinusoidal waveforms for detection.

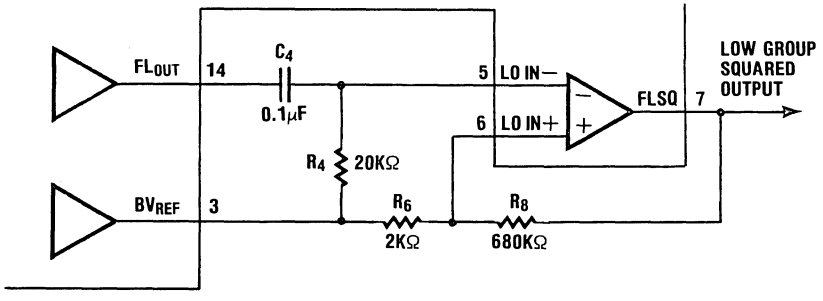
However, the majority of the current receivers on the market require square wave inputs and these should be as close to the 50% duty cycle as possible.

The two uncommitted op amps on the S3525 can buffer analog signals or, more typically, be configured as comparators to provide the squaring function. This squaring function is important because much of the performance of the completed DTMF Receiver is determined here.

In the squaring circuit of Figure 6 the capacitor C_4 acts as a high pass filter to prevent any DC offset from the analog output being coupled into the comparator. This is important in assuring the 50% duty cycle of the output waveform driving most decoder chips. R_4 provides bias of the input pin.

The trip point of the comparator, or the basic sensitivity of the receiver, is determined by adjusting the ratio of R_6 to R_8. For central office systems one might need sensitivity to −26dBm but for an intercom or tone-control system, one may not want or need that much sensitivity. The fact that the sensitivity can be adjusted off-chip increases the flexibility of the S3525 for various applications.

Figure 6. S3525 Bandsplit Filter



Receiver Applications Circuits

This application note describes three different DTMF receiver circuits with the S3525 DTMF Bandsplit Filter IC and available digital DTMF Decoder IC's. These circuits use only two IC packages and a few external components.

Receiver A uses the TELTONE TT6174 Digital Tone Receiver, Receiver B the MOSTEK MK5102 or 5103, and Receiver C the ROCKWELL CRC 8030. These are 3 very compact DTMF Receiver systems. Receiver B, for example, was built on a single-sided board in a 2½ by 3½ inch area.

The benefits of the S3525 are significant compared to a conventional Op Amp filter or Hybrid Filter network. A simple 2-IC DTMF Receiver reduces parts costs, assembly labor, and PC board size.

All of these receiver circuits have been constructed and evaluated in the lab. However, they do not necessarily represent optimized circuit values and are offered only as starting points for development of DTMF Receivers to meet each user's particular application.

Figure 7. Evaluation Decoder and Display Block Diagram

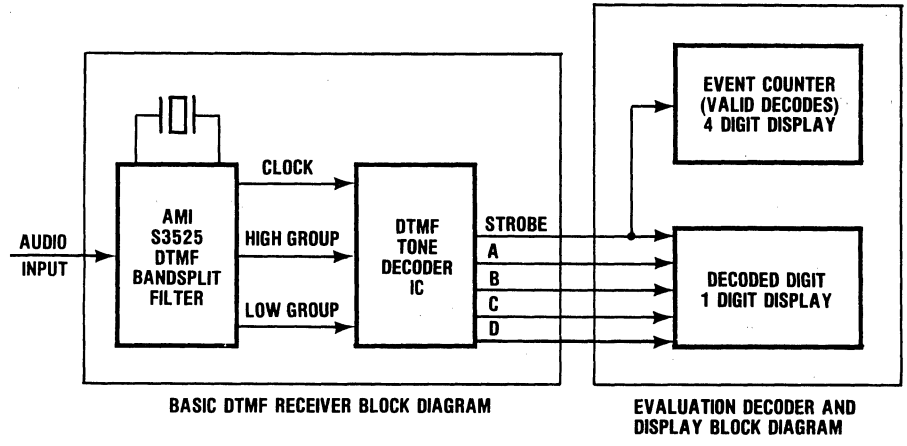
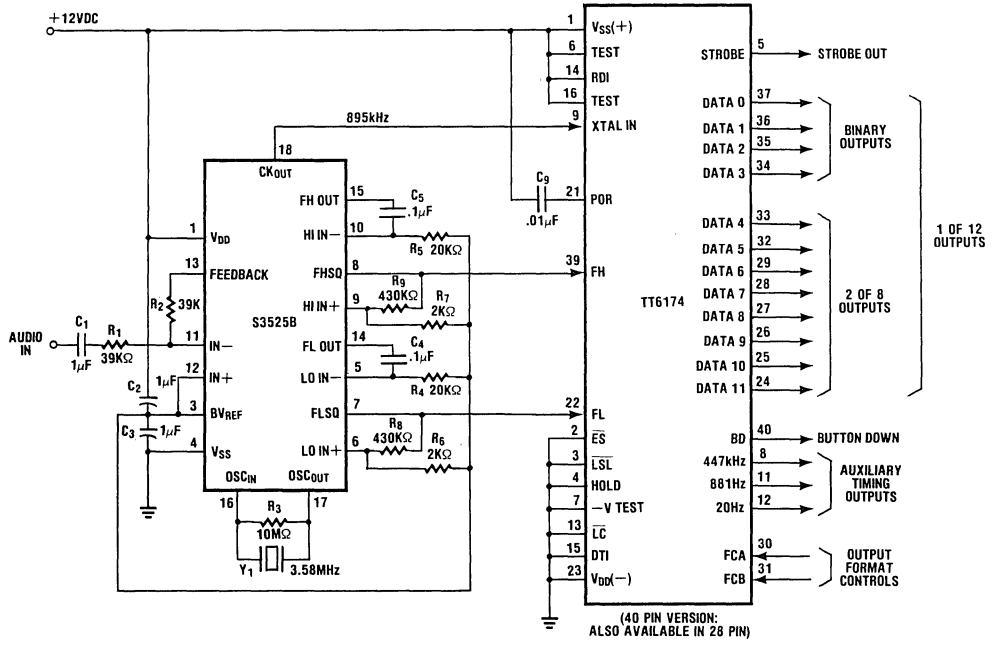


Figure 8A. AMI/TELTONE DTMF Receiver



DTMF Receiver A

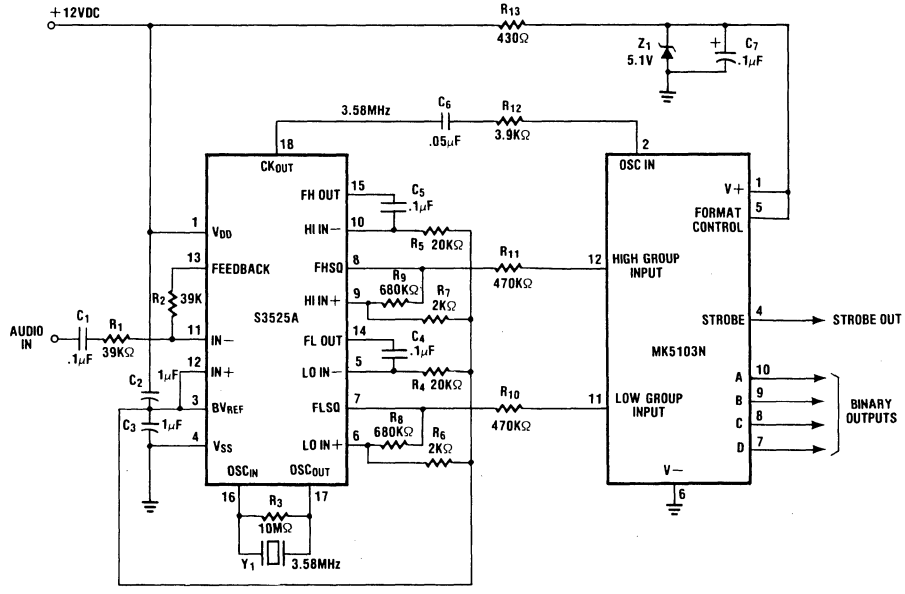
Figure 8A illustrates a two-chip DTMF Receiver circuit with the AMI S3525B Bandsplit Filter and a Teltone TT6174 Digital Tone Receiver chip. This receiver operates from 11 to 13.5 Volts DC and, with an additional loop current detector, can even detect Dial Pulses as well as the 16 DTMF digits. Depending on the format control, the receiver can deliver binary, 1 of 12 or 2 of 8 and binary simultaneously. This flexibility makes the receiver valuable for many different applications without needing external logic for data format conversion. A standard 3.58MHz TV crystal provides the clocking for both chips, with the buffered divide-by-four output of the S3525B driving TT6174 at 895kHz.

The input circuitry is a single-ended input for general applications but could be a differential design for high-impedance bridging across a telephone line.

This decoder chip has many other features that are not shown in this schematic and for a complete description Teltone should be contacted.

For PC layout and parts list see AW-301 in Section 11 of this Design Manual.

Figure 8B. AMI/MOSTEK DTMF Receiver



DTMF Receiver B

Figure 8B illustrates a two-chip DTMF Receiver circuit with the AMI S3525A Bandsplit Filter and a MOSTEK MK5103N Tone Decoder. This receiver operates from a single power supply in the 10 to 13.5V range or from a ±5V supply. The S3525A crystal oscillator circuit buffered output drives the MK5103 clock input through a coupling capacitor and resistor.

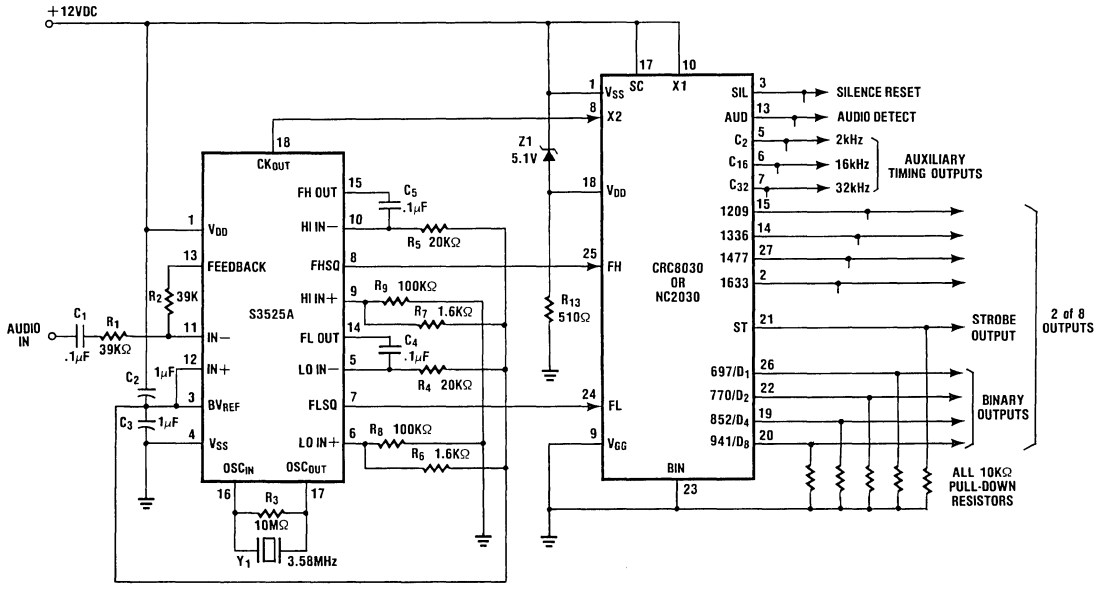
The input potentiometer adjusts the input level for maximum dynamic range depending on the signal source. The sensitivity of the receiver is then determined by the ratio of the 680kΩ resistor to the 2kΩ resistor as described in the paragraph on output configurations.

The 470kΩ resistors provide signal attenuation since the S3525 outputs are close to 12V and the MK5103 is at 5V. These would be required, of course, even if the ±5V supplies were used and the 5.1V zener was deleted.

The 1μF capacitors bypassing pin 3 are important to minimize noise on the BV_{REF} line both inside the chip and where it is used for the comparators to set the sensitivity.

For PC layout and parts list see AW-302 in Section 11 of this Design Manual.

Figure 8C. AMI/Rockwell DTMF Receiver



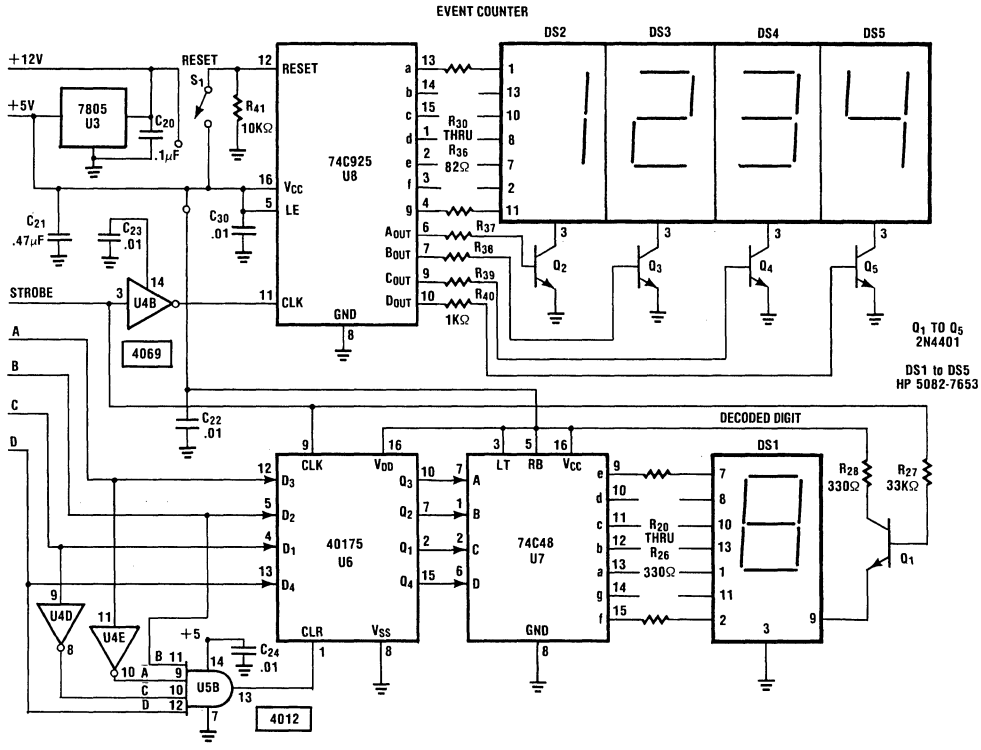
DTMF Receiver C

Figure 8C illustrates a two-chip DTMF Receiver circuit with the AMI S3525A Bandsplit Filter and a Rockwell CRC 8030 DTMF Detector. This receiver operates from a single power supply in the 10 to 13.5V range and delivers binary outputs from incoming DTMF tones. The common 3.58MHz TV crystal is connected across the oscillator terminals of the S3525A. The buffered output of the oscillator is applied to the CRC 8030 oscillator input directly.

The input circuitry to the S3525 is the same as previous circuits or can be varied to suit the application. The input is a differential op amp and can be used accordingly. Be sure BV_{REF} (pin 3) is adequately bypassed as it provides the reference voltage for the squaring circuits and the internal op amps.

The CRC 8030 requires the high and low inputs (FL, FH) to be low (negative) when no signal is present. Therefore, the squaring circuits of Figure 8B cannot be used as they can be either high or low when no signal is present. The positive input of the squaring op amp is biased slightly negative by the 1.6kΩ and 100kΩ resistors insuring that the output is negative when no signal is present.

Figure 9. Display and Counting Circuitry



Display and Counting Circuitry

Evaluation of the DTMF circuits requires the ability to detect valid digit decodes and which digit is decoded. For the purpose of verifying the described receivers a simple approach was taken.

The valid-digit or event counter consists of four 7-segment LED displays driven by a 1-chip, 4-digit counter with multiplexed 7-segment output drivers. This and 1/6 of a hex inverter are all that is required to count the decodes.

It takes a bit more to display the decoded digit, particularly to convert that old confusion factor of the "0" button actually being a 10. With the circuit in Figure 9, it takes 1 LED display and 4 chips to do the job, although the special characters appear a little unusual on the 7-segment display.

For displaying the decoded digit only (on Receiver A), the Event Counter and the 7805 could be eliminated. Then the resistors R_{20} through R_{26}, R_{28} should be raised from 300Ω to 1500Ω to control the LED current from 12V rather than 5V.

The Decoded Digit Display shows the decoded digit until the next strobe pulse so the last digit remains displayed. The transistor Q_1 drives the decimal point of the LED showing when a valid digit (strobe) is actually present.

For PC layout of this circuit see AW301, 302 in Section 11 of this Design Manual.

Evaluation of Circuits

A simple evaluation of the circuits can be conducted using the Mitel CM7291 Tone Receiver Test Cassette. A cassette player, a frequency counter, and a voltmeter will allow a user to check receiver parameters: receiver detection bandwidth, maximum acceptable amplitude ratio (twist), receiver guard time, dynamic range, acceptable signal-to-noise ratio, and receiver falsing or "talk-off".

The results of the tests can be used for a basic evaluation of a DTMF receiver. However, showing good results on the test tape does not prove Central Office quality. Additional testing must be done to prove compliance to various standards. Depending on the particular telephone administration different tests may be required. Figure 10 illustrates the CEPT (European) requirement for single frequency tone protection. In Table I the performance of the 3 receivers on the tests from the tape are summarized.

Figure 10. Signal Condition Requirements

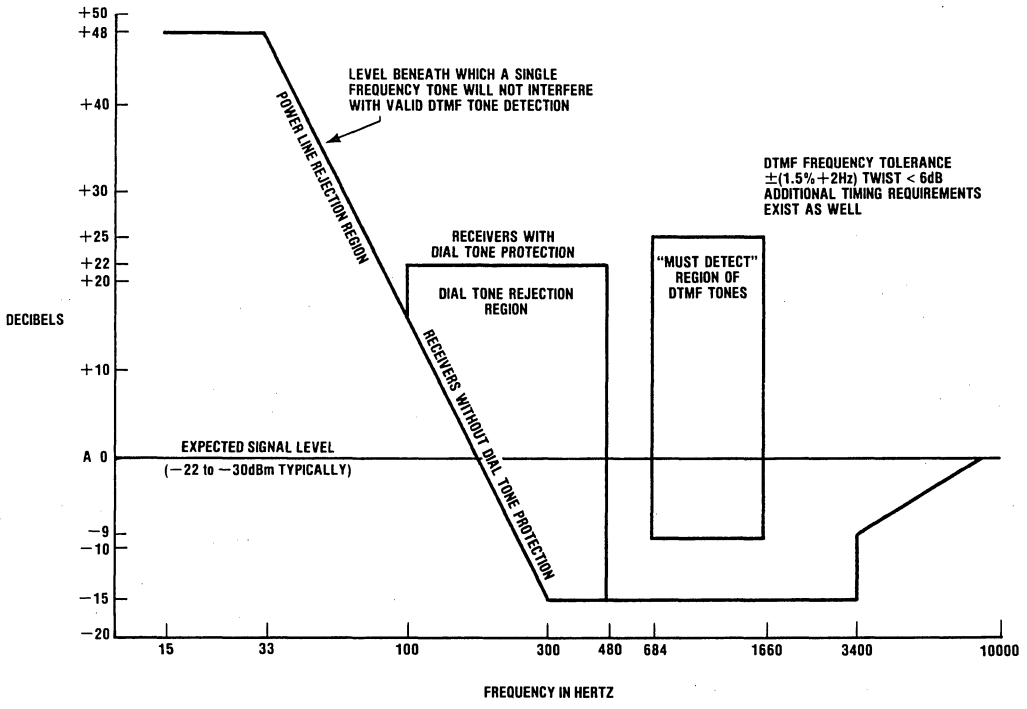


Table I: Performance of Receiver Circuits (Tested Using Mitel CM7291 Tape)

Test	Receiver	AMI/Teltone	AMI/Mostek	AMI/Rockwell	Comments
Valid Decodes		160/160	159/160	160/160	Note 1
Bandwidth		3.8 to 5.2%	4.8 to 5.2%	4.7 to 5.5%	
Center Frequency		0.0 to 0.5%	0.0 to 0.25%	−0.05 to −0.45%	
Twist		±20dB	+16.0dB −19.7dB	+11.9dB −16.5dB	
Dynamic Range		35dB	31dB	27dB	Note 2
Decode Time		31.1msec	33.3msec	16.8msec	Note 2
Signal to Noise Performance					
24dB		1000	993	1000	Notes 2, 3
18dB		1000	997	1000	
12dB		1000	991	1000	
Talk-off		4 hits	1 hit	2 hits	

Notes:
1. This test is 10 pulses of each digit.
2. Performed only with digit 1.
3. This test performed with 20dB attenuator in front of receiver to realistically simulate telephone conditions such as Bell Systems PBX spec. in Publication 48002. Mitel tape level is too high. Results are number of valid decodes from 1000 pulses provided.

Summary of Receiver Circuits

Three different DTMF receivers have been outlined using the S3525 DTMF Bandsplit Filter. These circuits have been constructed and evaluated in the lab using the described test tape. These circuits have not been subjected to analysis for temperature variation, component tolerance variations, or many of the other considerations that a production design should include. They are intended only to illustrate the various ways the S3525 can be used to reduce cost and improve performance of DTMF Receivers. Should any additional applications information be required, please contact AMI or the decoder manufacturer.

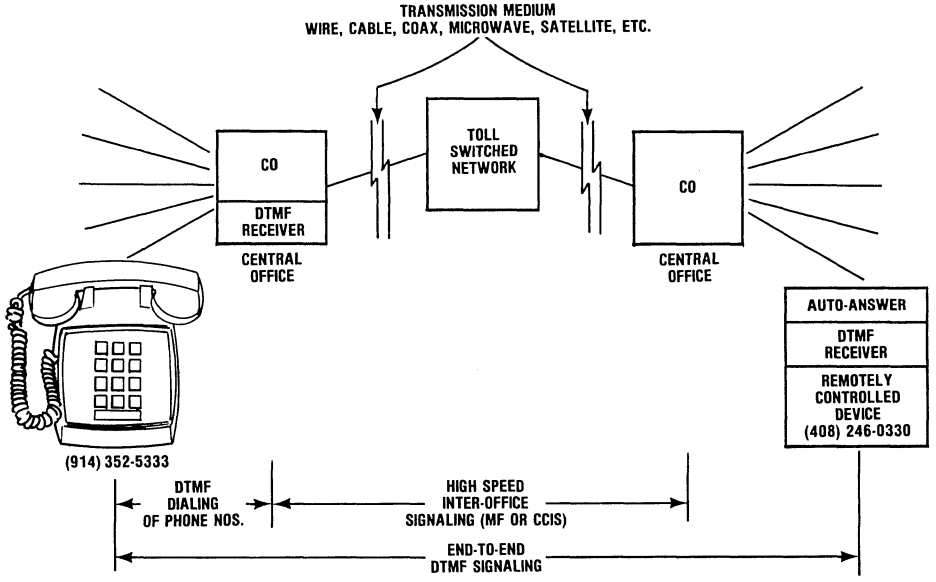
Applications

Most DTMF decoder chips have additional output formats other than the 4-bit binary used in these application circuits. The MOSTEK MK5102N-5 (MK5013N-5) will produce either the 4-bit binary or a dual 2-bit Row/Column code that, with the addition of 1 more chip, will produce the familiar 2-of-8 or 1-of-16 formats.

The TELTONE TT6174 can produce 3 different output formats directly; a binary, 2-of-8 or 1-of-12.

Specific applications require different output formats. The basic application is the DTMF Receiver for a PABX or Central Office to decode dialing. Other applications include radio systems, remote control systems, remote alarm and security systems, mobile telephones, remote computer entry, point-of-sale systems, DTMF-to-rotary dial-pulse converters, dial intercom systems, toll restrictors, etc.

Figure 11. DTMF End-to-End Signaling Using the Telephone Network



Remote Control

In some systems, the telephone set is used to do the remote controlling. A remote device to be signalled is interconnected to the telephone network with its own number (see Figure 11). When that number is dialed, the connection is established. The calling party continues to push the buttons on his telephone, sending command codes.* The DTMF Receiver at the central office is disconnected once the line connection is established, so no problem arises in the telephone network. Now the DTMF Receiver in the answering device is detecting and responding to the dialed digits, performing the control functions.

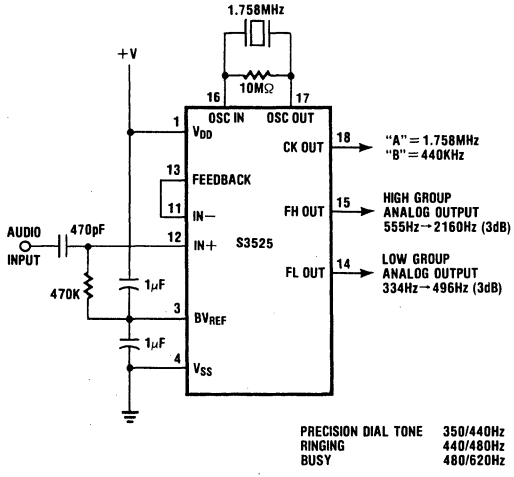
Dial Tone Detector

Since the frequency response of switched capacitor filters can be varied directly by varying the clock frequency, the S3525 can be used for other Telecommunications applications.

One application is a dial tone detector for telephone accessory equipment to determine the presence or absence of dial tone. Precision dial tone is a combination of 350 and 440Hz. By using a crystal of 1.758MHz the 3dB points of the low group filter output will be 334 to 496Hz. Thus, all the energy from precision dial tone will be available at the low group output. Any energy present at the high group

*Need "Polarity Guard" or non-reversing central office so encoder stays enabled.

Figure 12. Dial Tone Detect



Dial Tone Detector (continued)

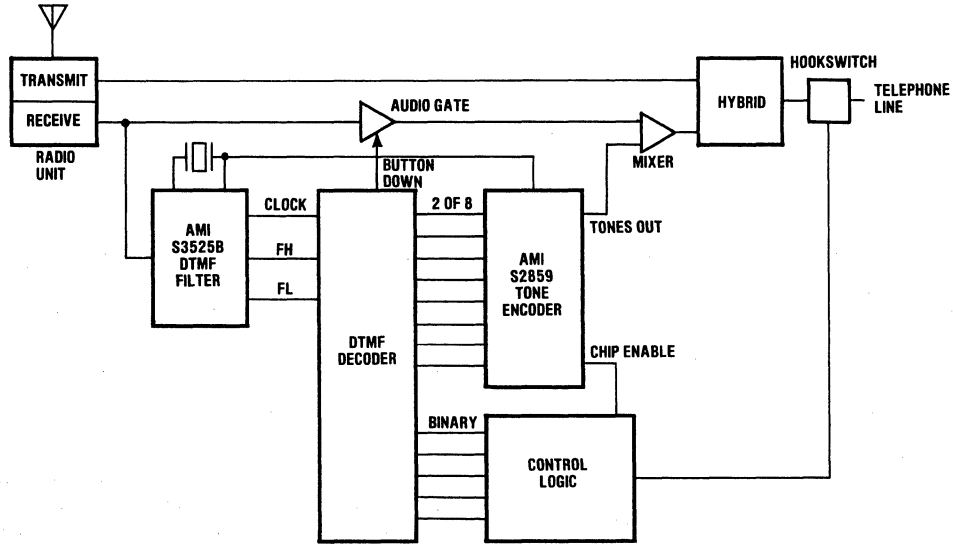
output (now 555 to 2160Hz) will indicate the presence of something other than dial tone.

The choice of 1.758MHz as the oscillator crystal allows both precision dial tone and ringing to be passed through the low group filter as well as the low half of the busy signal, while the upper half of the busy signal will be present in the high group output.

This technique can be demonstrated with an off-the-shelf microprocessor crystal at 1.8432MHz (most crystal vendors stock it) while ordering the 1.758MHz to fit the pass-band more exactly. The pass-band will be 350 to 520Hz instead of 334 to 496Hz but will allow circuit design and evaluation to proceed.

This application shows that modern switched-capacitor filter devices are not limited to a specific design bandwidth, but can sometimes be used for other applications by varying clock rates, a benefit not provided by the now out-moded hybrid filters.

Figure 13. Radio-Telephone Interconnect



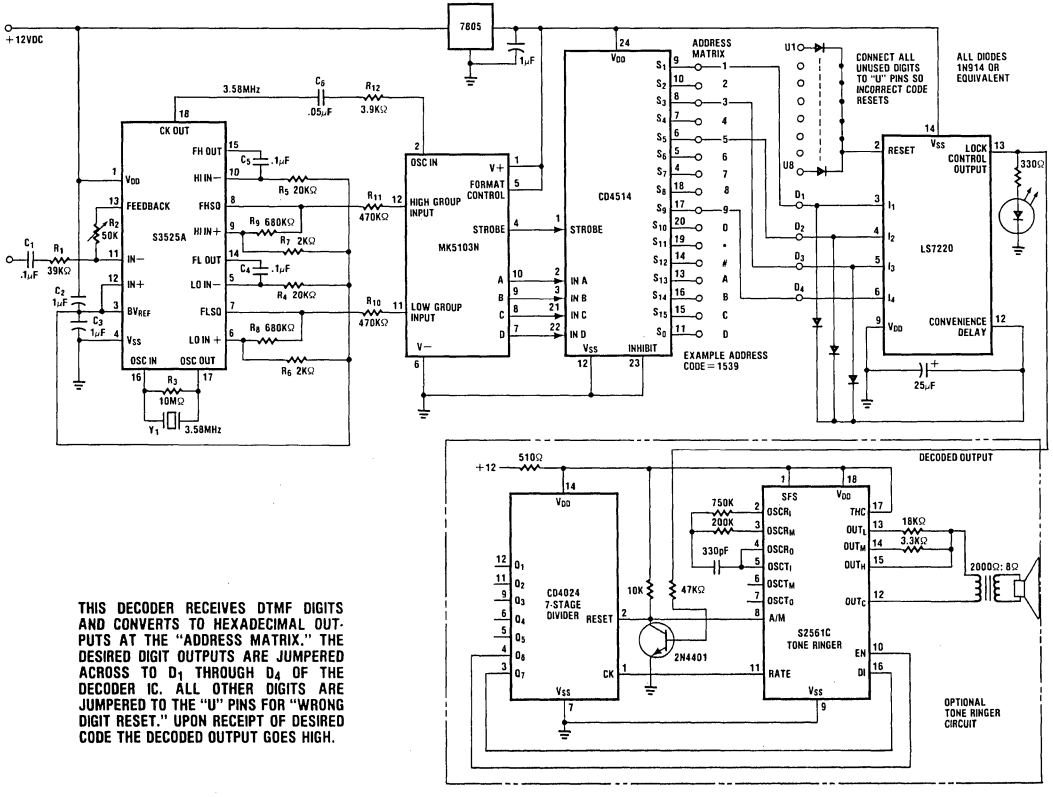
Mobile Radio

The S3525 can be used to improve the reliability of radio-to-telephone interconnections. The noisy, twisted DTMF signals from the radio network can be regenerated into accurate, constant level, low noise tones to the telephone line. The 2-of-8 output of the decoder drives a DTMF encoder chip (S2859) to repeat the received tones, or where Touch-Tone^{R} service is not available, drives a Pulse Dialer chip (S2560) to translate the radio tones to dial pulses (see Figure 13).

In a telephone network the central office connects and rings an individual telephone after decoding the number dialed by the calling party. In a radio network or intercom over a single pair of lines, however, all stations hear the dialed address digits. Therefore, an address decoder must be located at each station and programmed to ring or open a loudspeaker circuit only when its specific address is dialed.

Figure 14 shows a 6 IC circuit that will decode a 4-digit address code and ring like a telephone and light an LED when the correct address is detected. This circuit could be modified to simply turn on a loudspeaker, eliminating two ICs, or to initiate remote control function

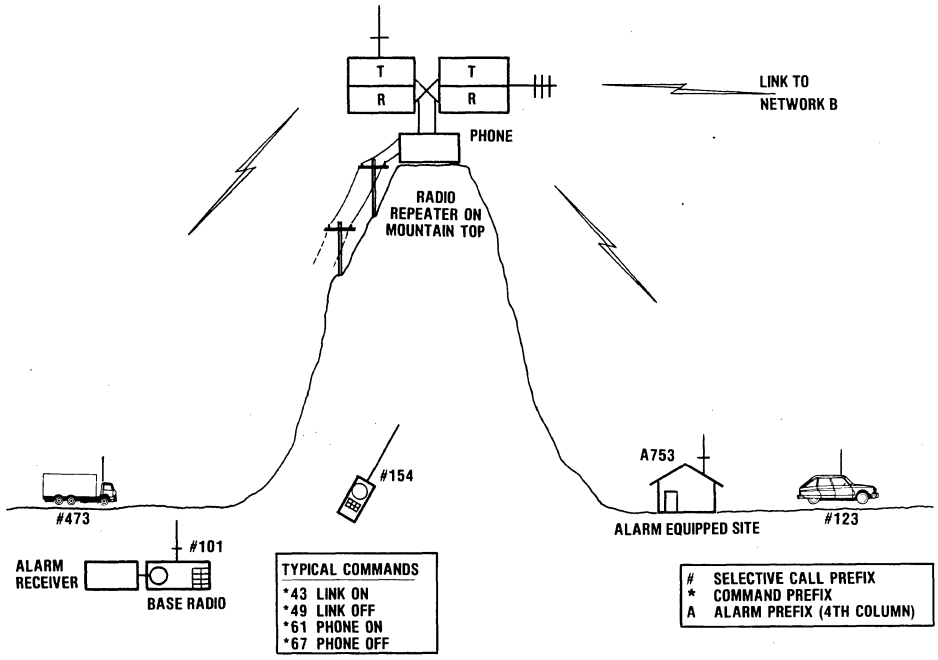
Figure 14. DTMF Address Decoder Circuit



THIS DECODER RECEIVES DTMF DIGITS AND CONVERTS TO HEXADECIMAL OUTPUTS AT THE "ADDRESS MATRIX." THE DESIRED DIGIT OUTPUTS ARE JUMPERED ACROSS TO D_1 THROUGH D_4 OF THE DECODER IC. ALL OTHER DIGITS ARE JUMPERED TO THE "U" PINS FOR "WRONG DIGIT RESET." UPON RECEIPT OF DESIRED CODE THE DECODED OUTPUT GOES HIGH.

The following illustration shows a complex radio and telephone network using DTMF signaling for a variety of functions: selective calling, telephone interconnect, alarms, and remote control. This system is based on the DTMF circuits described earlier in this application note, each station having encode and decode capability.

Figure 15. Complex Radio Network Using DTMF Signaling



Examples of how such a system can be used:

—**Local network radio calls.** Unit 154 calls the van by dialing #473. The decoder in the van can be set to honk the horn if the driver is a short distance from his vehicle. Similarly, dialing #101 alerts the dispatcher. The range of this local network is extended by locating the radio repeater on a high point.

—**Calls to distant networks.** A command signal, such as *43, turns on the radio link to the distant network allowing a user to signal stations in the other network as if they were local. A second command, *49, disconnects the two networks.

—**Radio to telephone interconnect.** Dialing *61 connects the repeater to a telephone line. The radio user can then dial the telephone number of any point he needs to call. Dialing *67 hangs up the phone. A telephone caller might be able to dial into the system, reversing the procedure, and dial #154 to talk to that unit.

—**Security alarms.** When no phone lines are available alarms can be sent by radio. In this example the dynamite shack on the road construction project has a burglar alarm that sends A753 if tripped. The dispatcher's alarm receiver sounds an alert and appropriate action is taken. At night the alarm could be received by the supervisor's radio pager, in his pocket, wherever he was.

—**Remote Control.** Although not illustrated, access gates to construction sites, security lights, pumps, etc. can all be controlled by radio with DTMF.

This list could go on, but the conclusion is that DTMF signaling is the method of choice for many systems and the AMI S3525 Bandsplit Filter, with the decoder chips currently on the market, plus AMI's set of DTMF and Pulse Dialer chips, provide the tools to use this effectively and at low cost.

References

Teltone TT6174 Digital Tone Receiver Data Sheet Issue 2, 12/6/78

Teltone M-900 DTMF Filter and Decoder Set Data Sheet Issue 1, 9/1/80

Mostek MK5103(N)-5V Preliminary Data Sheet, August 1978

Mostek MK5102N-5 Application Note, August 1978

Mitel CM7290, CM7291 Tone Receiver Test Cassette, Copyright 1973, 1980

Rockwell CRC8030 DTMF Detector Data Sheet, May 1978

Rockwell CRC8030 DTMF Receiver Application Note, May 1978

LSI Computer Systems LS7220 Keyless Lock Circuit Data Sheet, February 1980

Addresses

Teltone Corporation
P.O. Box 657
10801-120th Ave. N.E.
Kirkland, WA 98033

Mostek Corporation
1215 W. Crosby Road
Carrollton, TX 75006

Rockwell International Corp.
Microelectronic Devices
P.O. Box 3669
Anaheim, CA 92803

LSI Computer Systems, Inc.
1235 Walt Whitman Road
Melville, N.Y. 11747

Mitel, Inc.
1735 Jefferson Davis Highway
Arlington, VA 22202

AN SPP-MICROPROCESSOR INTERFACE

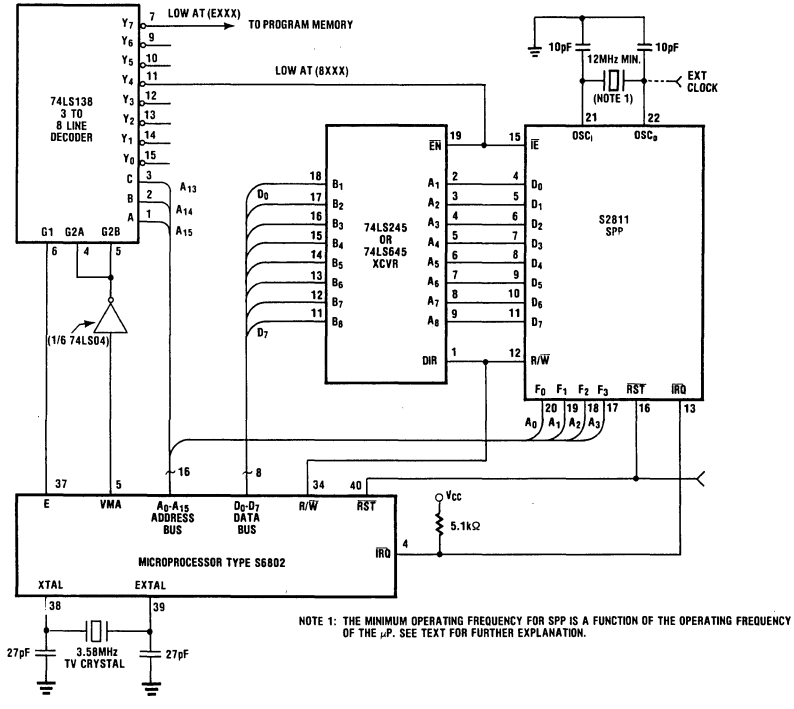
Designed as a memory mapped peripheral, the SPP (S2811 and other S2811 based devices) occupies a block of 16 addresses in the microprocessor memory space. Communicating with the SPP, therefore, is as simple as reading from or writing to a 16 byte random access memory. 13 of the 16 addresses are assigned a specific function. To make the SPP perform that function the microprocessor must read from or write to the corresponding memory location.

Table 1 shows the various control functions and their corresponding addresses. Note that the most significant hex digits (XYZ) of the addresses are left to the programmer's choice. In this application note a block of addresses from 8000 to 800F is assigned to the SPP for the sake of convenience. Thus, to initiate a block write operation a dummy data byte is written to memory address 8009. This is accomplished by an assembly language instruction "STA A BLK" in the 6800 family of microprocessors. Mnemonic BLK is equated to address 8009 by an assembler directive "BLK EQU 8009" in the beginning of the program.

Hardware Interface

Figure 1 shows a typical logic diagram for interfacing the SPP with a 6802 microprocessor. An address decoder generates the interface enable ($\overline{IE}$) pulse for block of addresses 8XXX. E signal output from the 6802 enables

Figure 1. Interfacing the SPP with a Microprocessor



the decoder during its positive cycle. Since the E signal is derived by dividing the oscillator frequency by 4, the width of $\overline{IE}$ pulse equals 2 times the oscillator clock cycle. For example, operating the 6802 at 4MHz will produce the $\overline{IE}$ pulse width of about 500nsec. When operating with a 20MHz crystal the SPP requires a minimum pulse width of 350nsec on the $\overline{IE}$ input. Thus the minimum clock frequency for the SPP is 14MHz when the 6802 operates at 4MHz. To operate the SPP at lower speeds the microprocessor clock must also be slowed down accordingly. It is recommended that a data transceiver be used with the SPP to isolate it from the data bus. To obtain maximum speed the SPP data outputs should drive only one LS TTL load and capacitive load should be minimized.

Software Interface

Once suitable addresses have been assigned to control functions and assembler directives given to equate these addresses to suitable mnemonics, software generation is straightforward. In general, the types of operations performed under microprocessor control include block read and write, execute a specific routine, read from OR (output register) and write to IR (input register), read from or write to a specific data memory location, etc. These commonly used operations and corresponding software source listings are summarized in Tables 2, 3 and 4.

Careful attention should be paid to conditions that can cause interrupts to occur from the SPP. SPP instructions such as LACO and JMIF cause interrupts. These are essential for proper sequencing of microprocessor programs. However, interrupts can also occur during block read operation. During a block read operation, the interrupt request line goes low to signal the availability of a data word. When the upper half (DUH) of the data word is read by the microprocessor, the interrupt request line returns high. It goes back low again one instruction cycle later to signal the availability of the next data word. To avoid these unnecessary interrupts from causing erroneous execution of an interrupt program, interrupt mask should be set prior to block read operation. In general, it is the best practice to leave the interrupt mask set until the microprocessor initiates an operation that will cause a valid interrupt request from SPP.

Applications that are heavily data transfer oriented such as FFT processing, performing data transfer using software, may be too slow. For example, to complete the transfer of one data word using software may take about 20μsec. The SPP itself is capable of handling data transfer rates to 2MW/sec. To obtain maximum utilization of the SPP or to process a task in the shortest possible time, data transfer should be carried out using DMA techniques rather than software alone.

Table 1: SPP Control Functions and Corresponding Addresses

Control	Function	Address
CLR	Clear Modes	XYZ0
RST	Master Reset	XYZ1
DUH	MS Byte of Data Word; Terminates Word Transfer	XYZ2
DLH	LS Byte of Data Word	XYZ3
XEQ	Execute from Location Specified by Data	XYZ4
SRI	Enable Serial Input Port	XYZ5
SRO	Enable Serial Output Port	XYZ6
SMI	Convert Serial S/M Input to 2's Complement	XYZ7
SMO	Convert 2's Complement Data to Serial S/M Output	XYZ8
BLK	Initiate Block Data Transfer	XYZ9
XRM	Enable External ROM Operation	XYZA
SOP	Set Overflow Protect	XYZB
COP	Clear Overflow Protect	XYZC
— —	Not Used	XYZD--XYZF

Table 2. Commonly Used Operations

Operation	6800 μP Instructions
Block Read	
Read Sequentially from SPP Memory Starting With Loc. (00.0)	STA A RST ; Reset SPP LDA A BLK ; Initiate Block Read LDA A DLH ; Read LS Byte from (00.0) - - - - - - - - - - - LDA A DUH ; Read MS Byte from (00.0) - - - - - - - - - - - LDA A DLH ; Read LS Byte from (01.0) • • • STA A RST ; Terminate Block Read
Block Write	
Write Sequentially Into SPP Memory Starting With Loc. (00.0)	Similar to Sequence Above, Except Replace LDA A Instruction With STA A
Execute a Specific Routine	
	STA A RST ; Reset SPP LDA A #$XX ; Load Starting Addr (XX) of Routine STA A XEQ ; Execute Routine WAI ; Wait for SPP to Finish • •

Table 3. Reading or Writing to a Specific Memory Location

To read or write to a specific memory location an initialization (IN) routine should be placed in the SPP instruction ROM as follows:

	Loc.	Instruction					Comments
Z0	00	NOP	JMUD	DT	Z0	;	Idle State
IN	01	NOP	TIRV	US	7,0	;	Load (IR) Into (S0)
	02	AVZ	LAXV	US	7,0	;	Preset Index Reg. $(IR)_{15\text{-}11} \rightarrow (Base)_{4\text{-}0}$; $(IR)_{9,8} \rightarrow (DISP)_{1,0}$
	03	NOP	JMUD	DT	Z0	;	Return to Idle State

With this routine Block Read or Write operation can be started from any RAM location

Example	6800 μP Instructions			
Write to RAM (1D.1)	STA	A	RST	; Reset SPP
	LDA	A	#$E9	; Load RAM Addr (1D.1) = E9
	STA	A	DUH	; Load IR
	LDA	A	#$01	; Load Address of IN Routine
	STA	A	XEQ	; Execute IN Routine
	STA	A	BLK	; Initiate Block Write
	LDA	A	LS	; Load LS Byte Into Accum
	STA	A	DLH	; Write LS Byte Into (1D.1)
	LDA	A	MS	; Load MS Byte Into Accum
	STA	A	DUH	; Write MS Byte Into (1D.1)
	•			
	•			Etc.
	•			

Table 4. Table for Translating RAM Address for Use With Initialization Routine

SPP RAM Addr	Load IR With	SPP RAM Addr	Load IR With
00.0--00.3	00XX--03XX	10.0--10.3	80XX--83XX
01.0--01.3	08XX--0BXX	11.0--11.3	88XX--8BXX
02.0--02.3	10XX--13XX	12.0--12.3	90XX--93XX
03.0--03.3	18XX--1BXX	13.0--13.3	98XX--9BXX
04.0--04.3	20XX--23XX	14.0--14.3	A0XX--A3XX
05.0--05.3	28XX--2BXX	15.0--15.3	A8XX--ABXX
06.0--06.3	30XX--33XX	16.0--16.3	B0XX--B3XX
07.0--07.3	38XX--3BXX	17.0--17.3	B8XX--BBXX
08.0--08.3	40XX--43XX	18.0--18.3	C0XX--C3XX
09.0--09.3	48XX--4BXX	19.0--19.3	C8XX--CBXX
0A.0--0A.3	50XX--53XX	1A.0--1A.3	D0XX--D3XX
0B.0--0B.3	58XX--5BXX	1B.0--1B.3	D8XX--DBXX
0C.0--0C.3	60XX--63XX	1C.0--1C.3	E0XX--E3XX
0D.0--0D.3	68XX--6BXX	1D.0--1D.3	E8XX--EBXX
0E.0--0E.3	70XX--73XX	1E.0--1E.3	F0XX--F3XX
0F.0--0F.3	78XX--7BXX	1F.0--1F.3	F8XX--FBXX

Examples: 1D.1 = E9XX
17.2 = BAXX
09.3 = 4BXX

AMERICAN MICROSYSTEMS, INC.

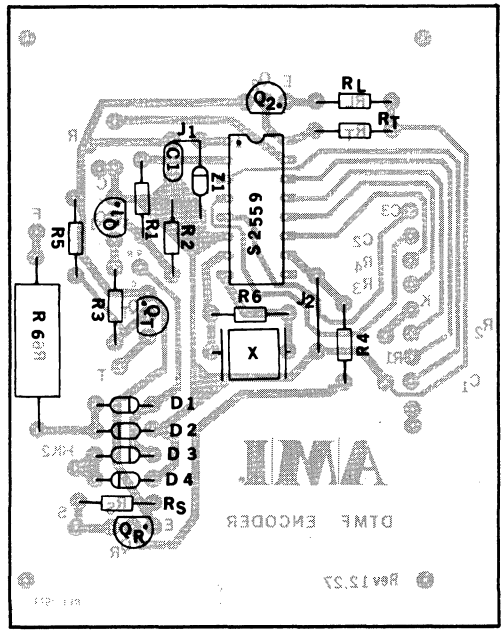
Section 9.0

Demonstration PC Boards

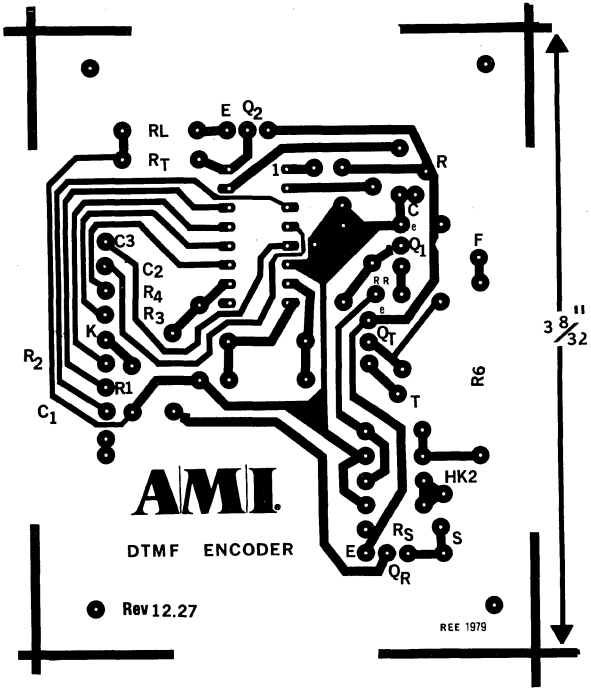
AW-101	DTMF Encoder-S2559
AW-102	Pulse Dialer-S2560A
AW-103	Repertory Dialer-S2562
AW-104	Tone Ringer-S2561
AW-201	Codec Demo Card-S3501/02/03/04
AW-202	Codec Demo Card-S3506/3507
AW-203	Codec Demo Card-S3507A
AW-301	DTMF Receiver-S3525B/TT6174
AW-302	DTMF Receiver-S3525A/MK5102

The circuits and boards shown in this section are offered only as starting points for further development and not as finished products. Each circuit has been constructed and tested as described in the Application Notes. However, they have *not* been subjected to analysis for temperature variation, component tolerance variations, or many of the other considerations required for a production design. It is expected that the circuits will be modified or changed to fit each particular application.

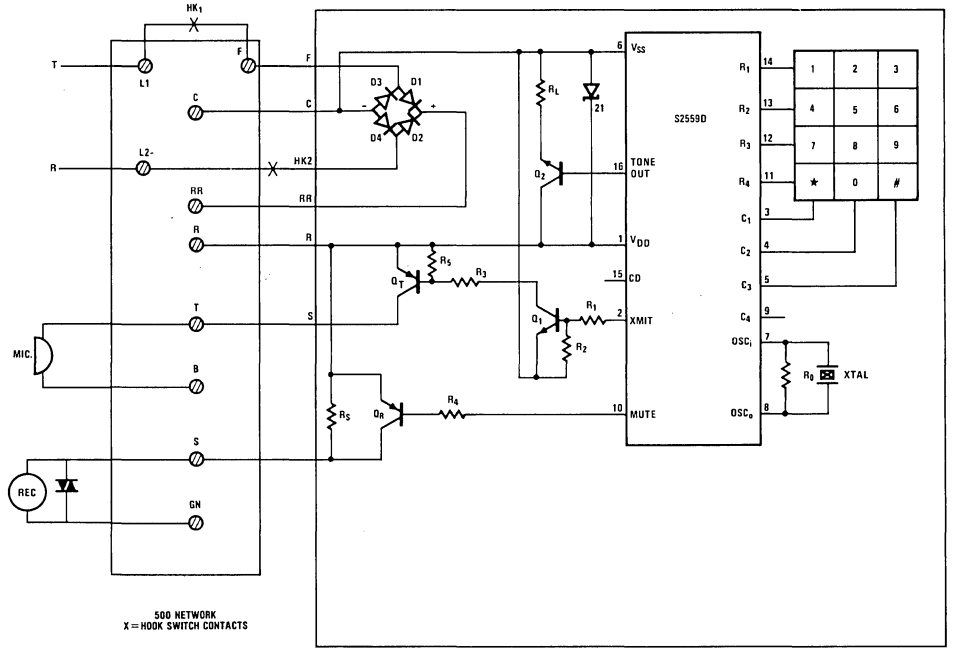
Assembly Information



Back Side Metal Pattern



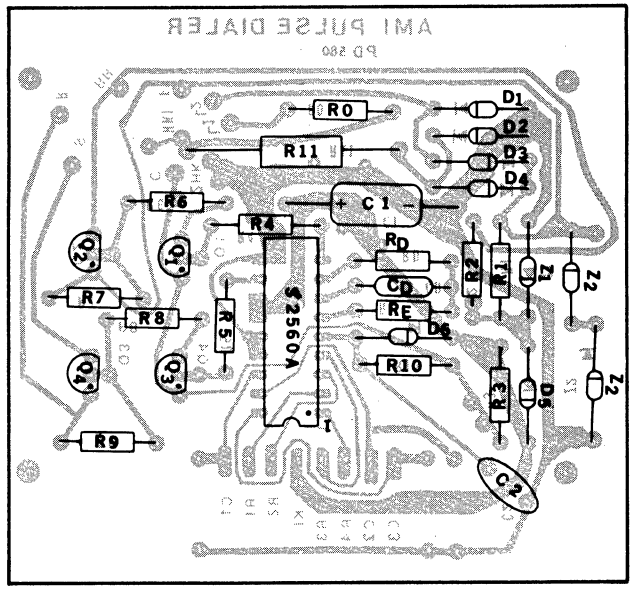
Schematic Diagram



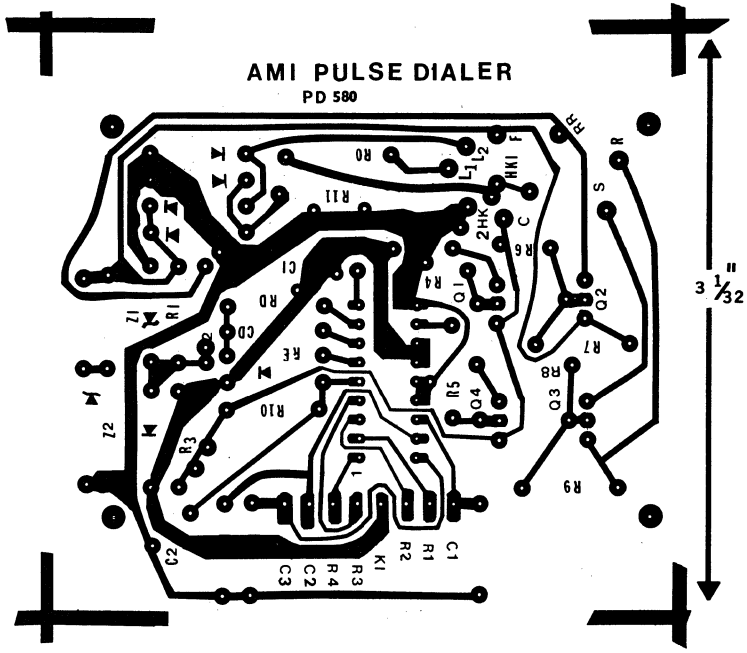
Parts List

Ref. #	Part #/Value	Description
R_0	10MΩ	Resistors
R_1	10KΩ	Resistors
R_2	30KΩ	Resistors
R_3	2.7KΩ	Resistors
R_4	2.4KΩ	Resistors
R_5	30KΩ	Resistors
R_L	150Ω	Resistors
R_S	5.1KΩ	Resistors
R_T	10KΩ	Resistors
C_1	.001μF	Capacitor
D_1-D_4	IN4004	Diode
Z_1	IN4742 Zener 12V	Zener Diode
Q_1	2N4401	Transistor
Q_2	2N4401	Transistor
Q_R, Q_T	2N4143	Transistor
XTAL	3.579545MHz	Crystal

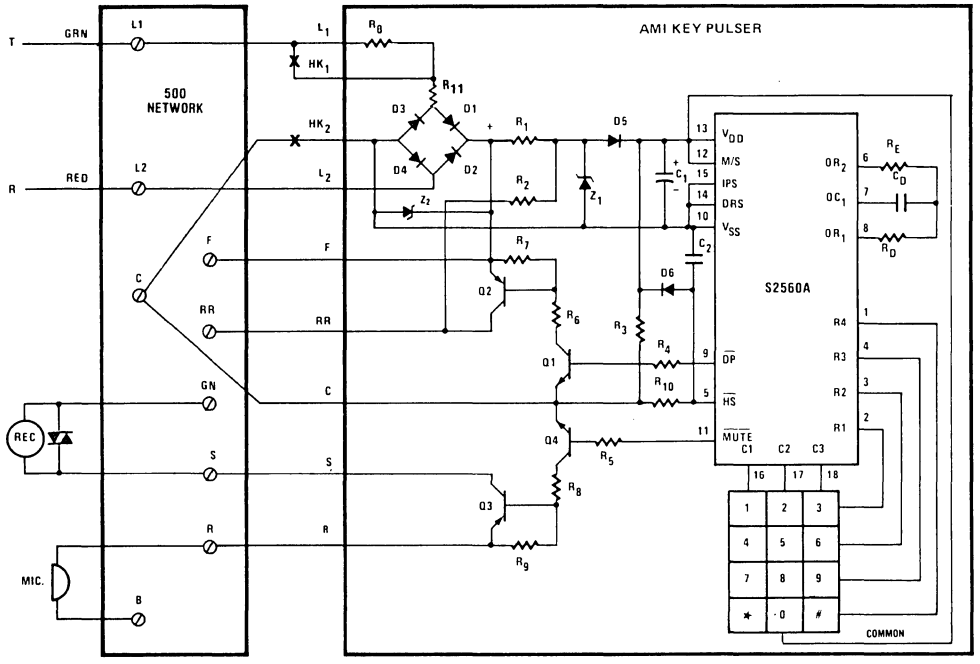
Assembly Information



Back Side Metal Pattern



Schematic Diagram

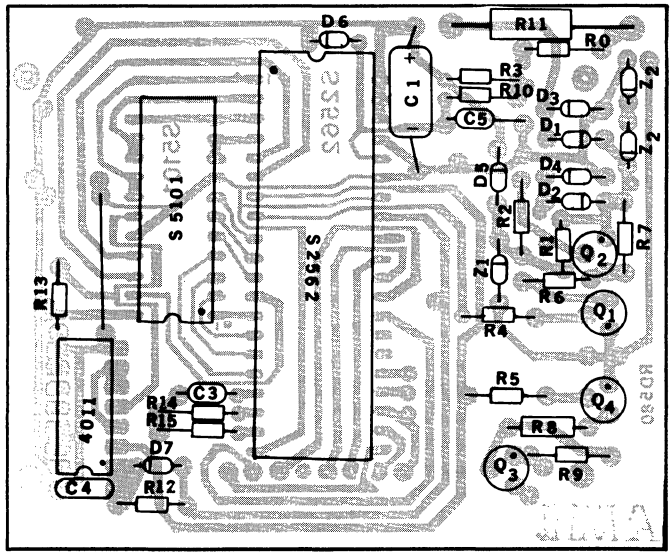


NOTE: PARTS REQUIRE COMMON OF THE KEYBOARD CONNECTED TO V_{DD}

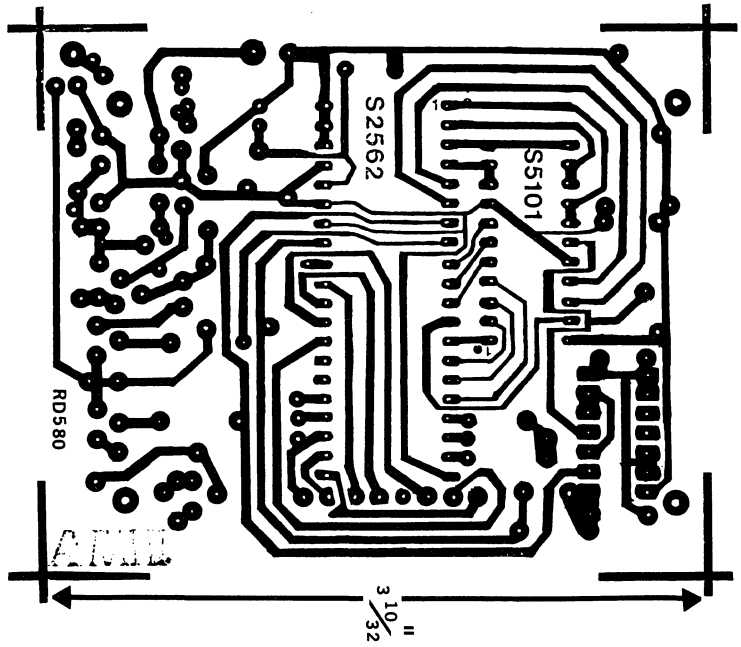
Parts List

Ref. #	Part #/Value	Description
R_0	10MΩ to 50MΩ	Resistor
R_1	150KΩ	Resistor
R_2	2KΩ	Resistor
R_3	470KΩ	Resistor
R_5	10KΩ	Resistor
R_6, R_8	2KΩ	Resistor
R_7, R_9	30KΩ	Resistor
R_{10}	47KΩ	Resistor
R_{11}	20Ω, 2W	Resistor
R_E, R_D	750KΩ	Resistor
C_1	15μF	Capacitor
C_2	0.01μF	Capacitor
C_D	270pF	Capacitor
D_1-D_4	IN4004	Diode
D_5, D_6	IN914	Diode
Q_1, Q_4	2N5550	Transistor
Q_2, Q_3	2N5401	Transistor
Z_1	IN4730	3.9V Zener
Z_2	IN5479	110V Zener

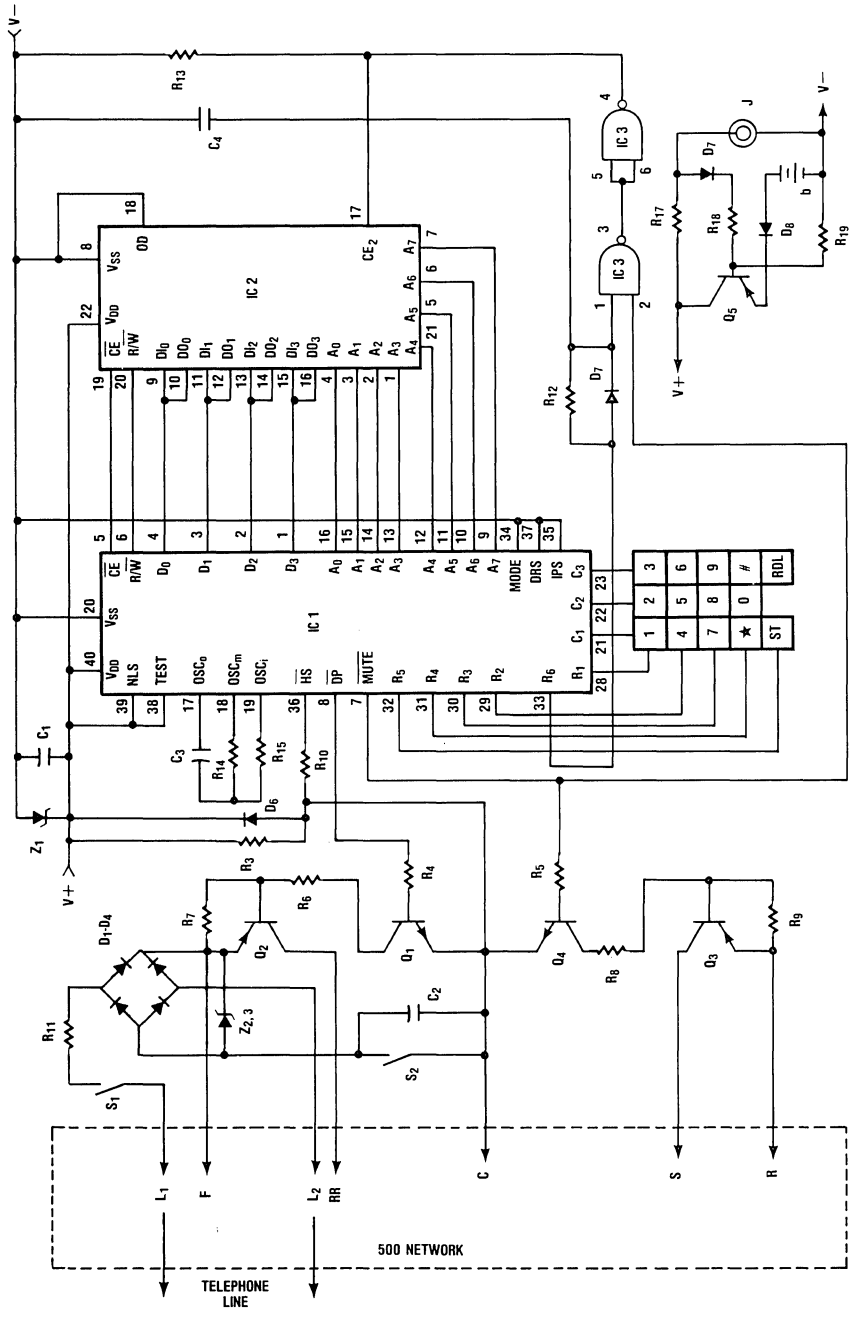
Assembly Information



Back Side Metal Pattern



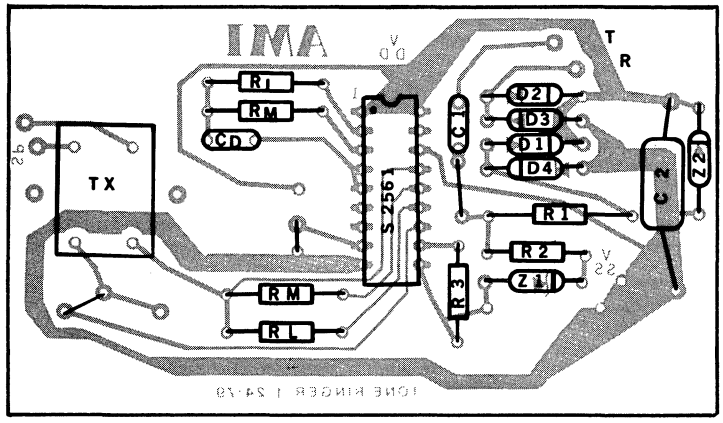
Schematic Diagram



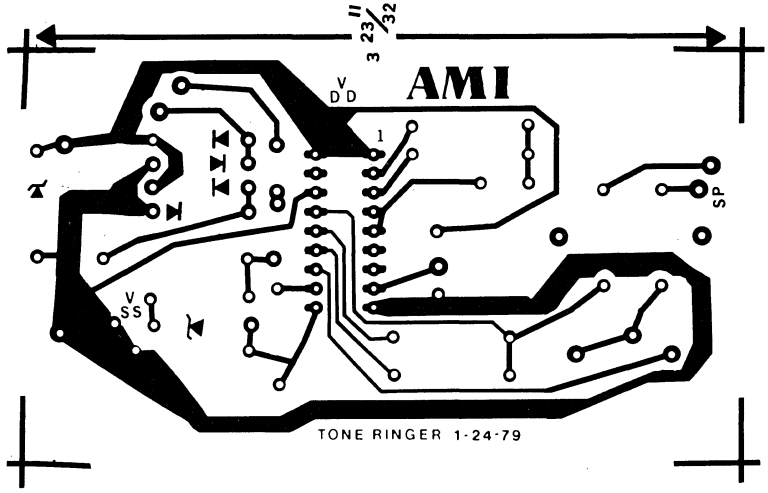
Parts List

Ref. #	Part #/Value	Description	Comments
R_3	750KΩ	Resistor	
R_4	18KΩ	Resistor	
R_5	18KΩ	Resistor	
R_6	2KΩ	Resistor	
R_7	30KΩ	Resistor	
R_8	2KΩ	Resistor	
R_9	30KΩ	Resistor	
R_{11}	20Ω 1W	Resistor	
R_{12}	10MΩ	Resistor	
R_{13}	470KΩ	Resistor	
R_{14}	110KΩ	Resistor	
R_{15}	1MΩ	Resistor	
R_{17}	100Ω	Resistor	
R_{18}	10KΩ	Resistor	
R_{19}	47KΩ	Resistor	
Q_5	ECG 288	Transistor	
Z_1	IN4733A	5.1V Zener	
Z_2/Z_3	IN5379	110V Zener Diode	(2 IN4758 diodes replaced with 1)
D_1-D_4	IN4004	Diode	
D_5-D_8	IN914	Diode	
Q_1	2N5550 or ECG 194	Transistor	
Q_4	2N5550 or ECG 194	Transistor	
Q_2	2N5401 or ECG 288	Transistor	
Q_3	2N5401 or ECG 288	Transistor	
C_1	100 MFD 25V	Capacitor	
C_2	.01 MFD	Capacitor	
C_3	330 PFD	Capacitor	
C_4	1000 PFD	Capacitor	
S_1		Hook Switch 1	
S_2		Hook Switch 2	
Battery	(3) AA 1.5 Vol		
IC3	CD4011	Integrated Circuit	
IC2	S5101	Integrated Circuit	
IC1	S2562	Integrated Circuit	
Key Board	Chromerics Type LT 23296		

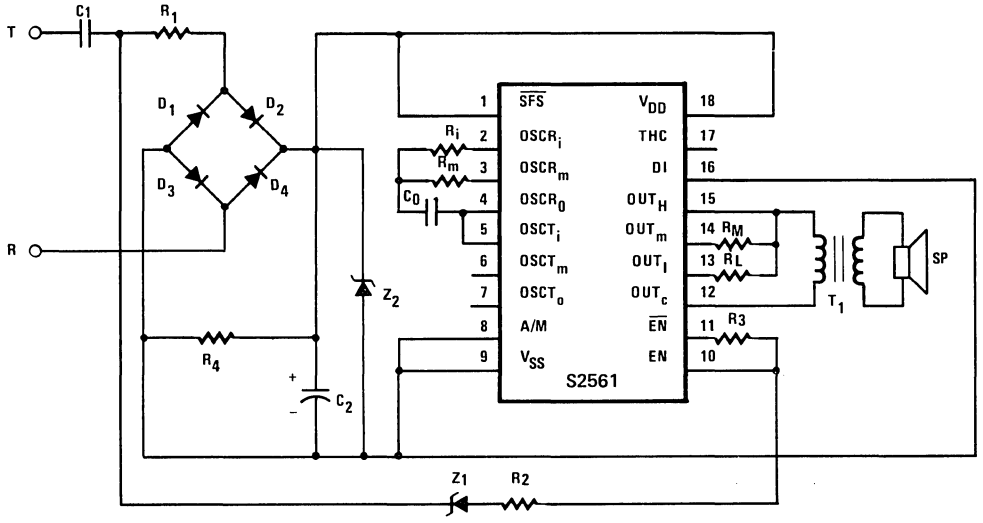
Assembly Information



Back Side Metal Pattern



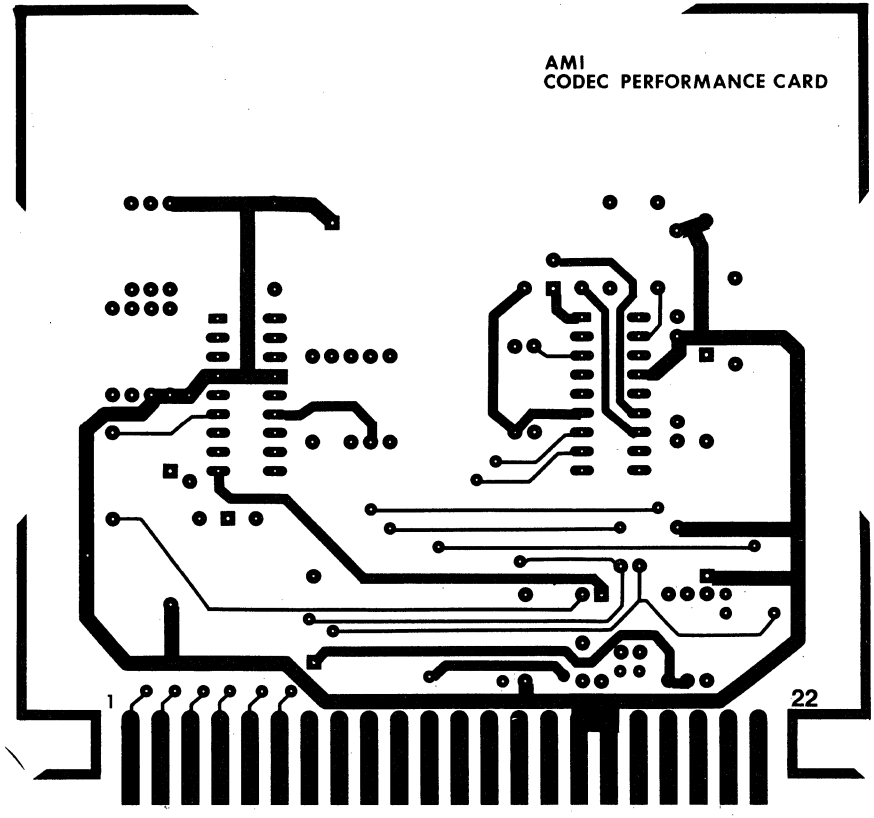
Schematic Diagram



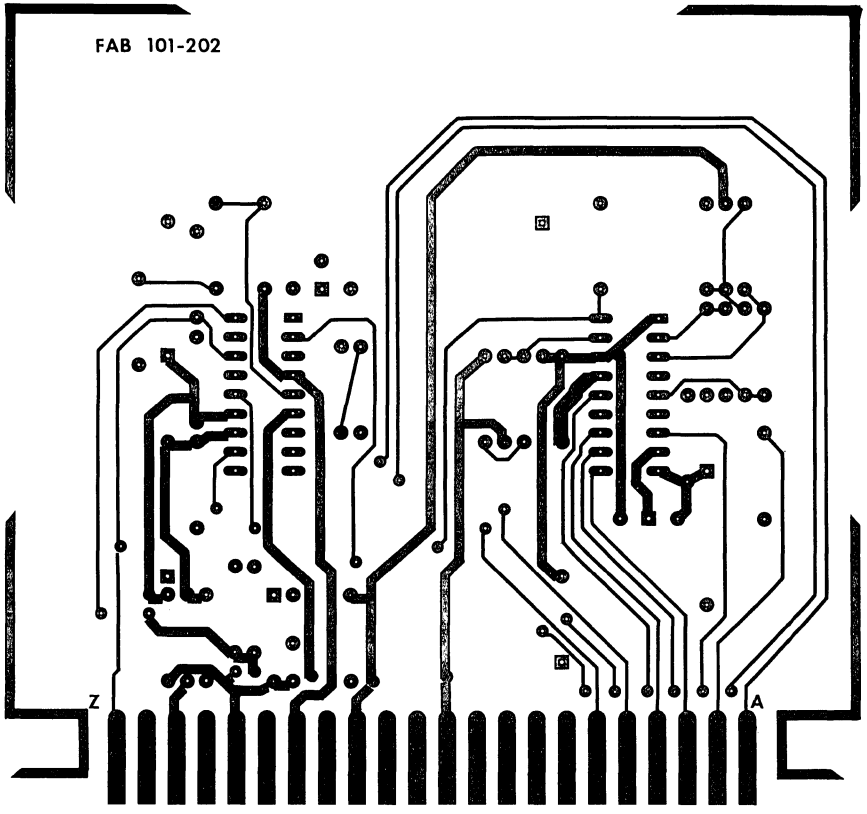
Parts List

Ref. #	Part #/Value	Description
C_1	1μF	Capacitor
C_2	47μF	Capacitor
D_1-D_4	IN4004	Diode
Z_2	IN4742	12V Zener Diode
C_D	300pF	Capacitor
Z_1	9 to 27V	Zener Diode
SP	8Ω	Speaker
T_1	2000Ω to 8Ω	Transformer
R_1	2KΩ	Resistor
R_2	51KΩ	Resistor
R_3	10MΩ	Resistor
R_i	1MΩ	Resistor
R_m	200KΩ	Resistor
R_L	18KΩ	Resistor
R_M	3.3KΩ	Resistor
R_4	100KΩ	Resistor

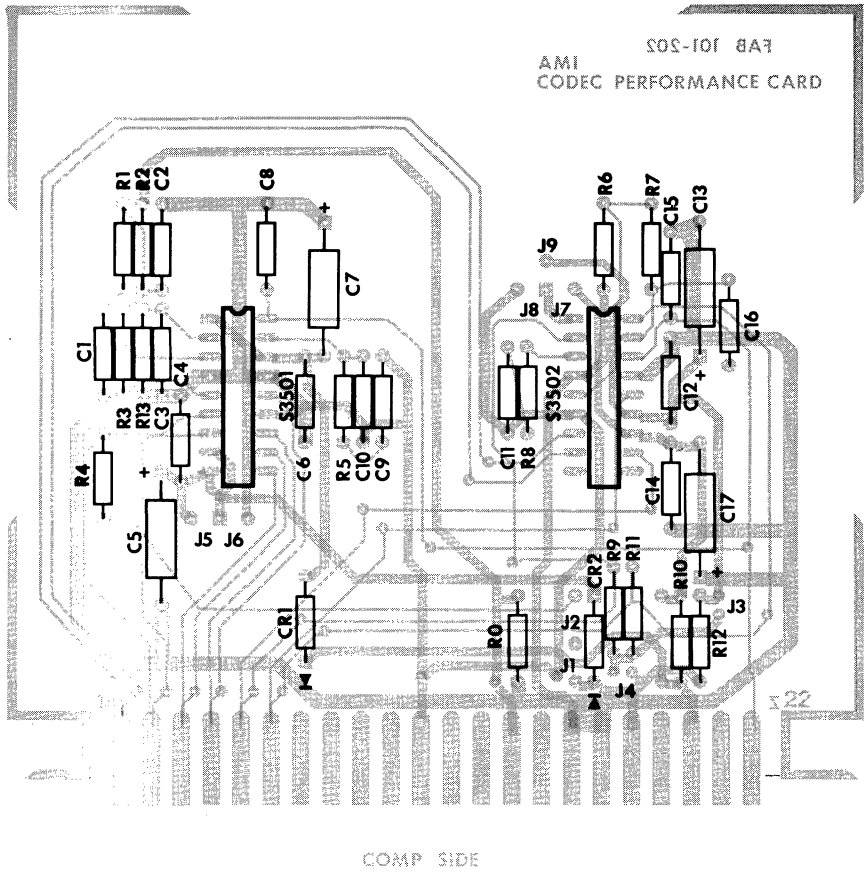
Component Side Metal Pattern



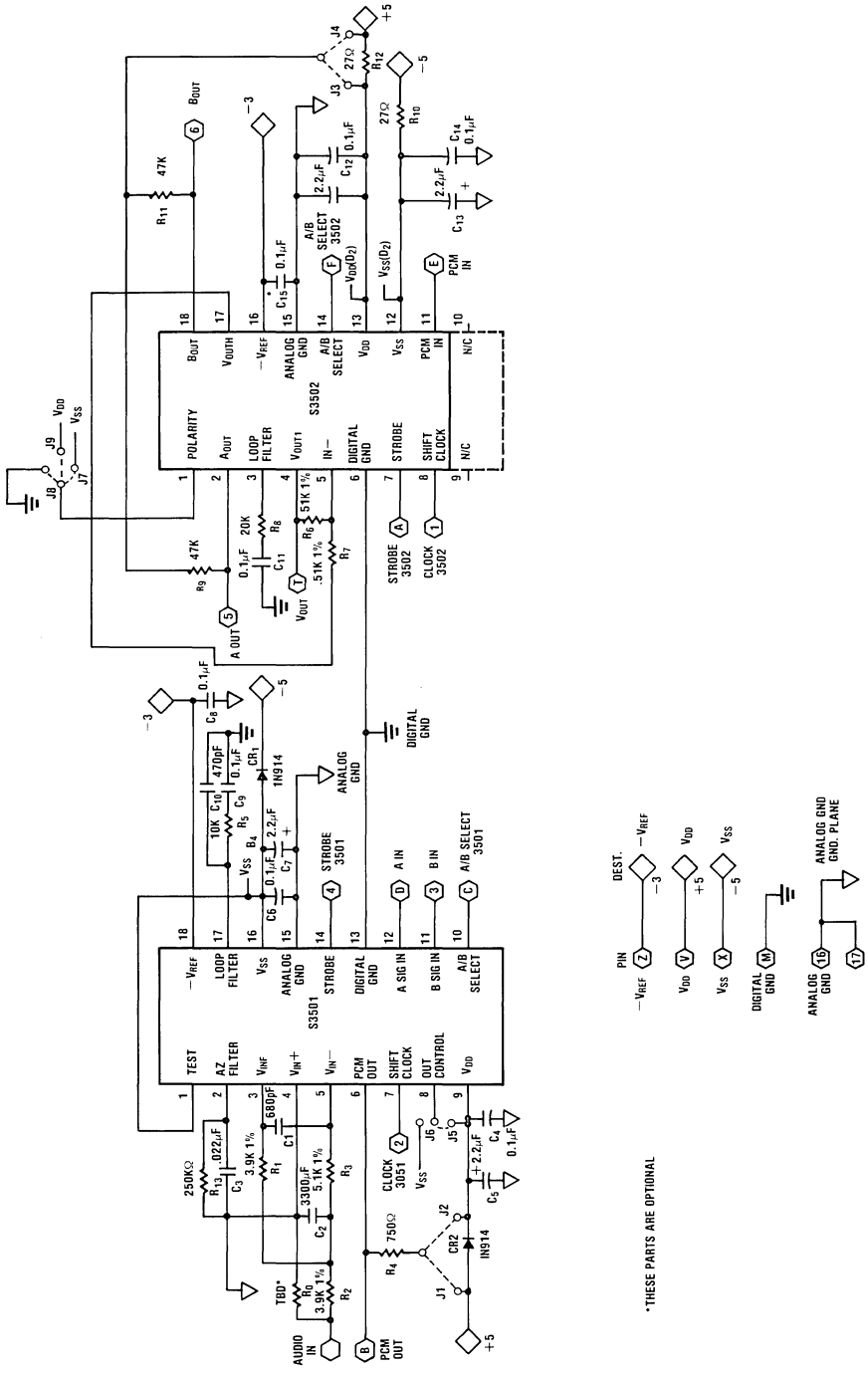
Back Side Metal Pattern



Assembly Information



Schematic Diagram



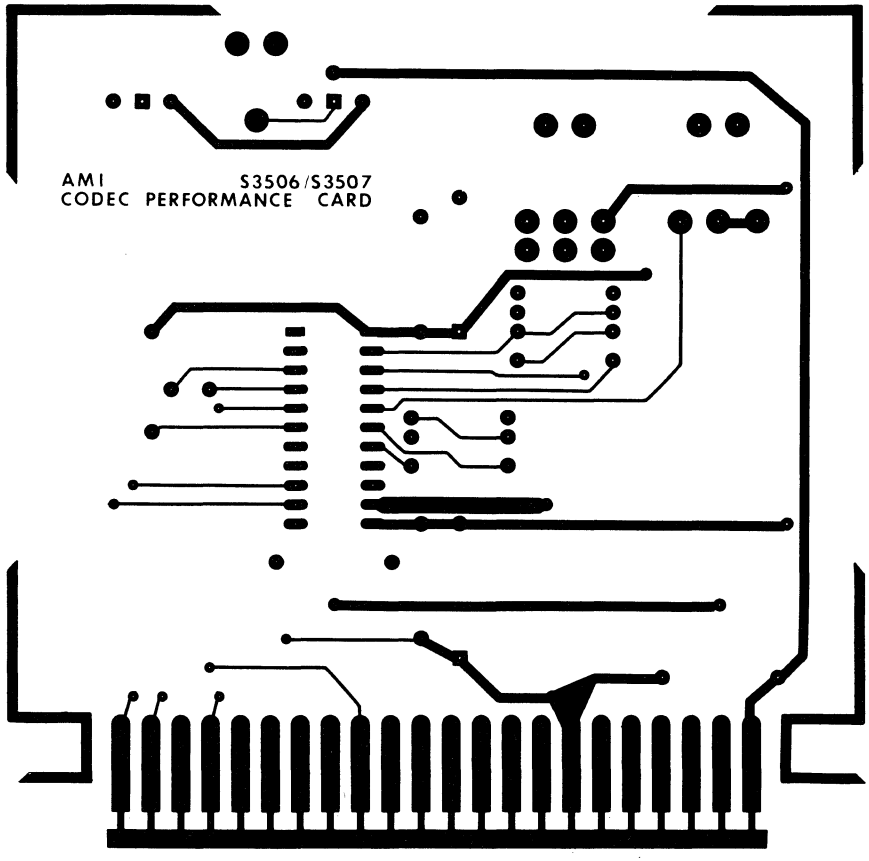
Parts List

Ref. #	Part #/Value	Description	Comments
CR_1, CR_2	IN914	Diode	
R_0	600Ω	Resistor ¼W	Termination if desired
R_1, R_2	3.9KΩ 1%	Resistor ¼W	Metal-film
R_3	5.1KΩ 1%	Resistor ¼W	Metal-film
R_4	750Ω 5%	Resistor ¼W	Metal-film
R_5	10KΩ 5%	Resistor ¼W	Metal-film
R_6, R_7	51KΩ 1%	Resistor ¼W	Metal-film
R_8	20KΩ 5%	Resistor ¼W	Metal-film
R_9, R_{11}	47KΩ 5%	Resistor ¼W	Metal-film
R_{10}, R_{12}	27Ω 5%	Resistor ¼W	Metal-film
R_{13} (S3501/02)	250KΩ 5%	Resistor ¼W	Metal-film
R_{13} (S3503/04)	5MΩ 5%	Resistor ¼W	Metal-film
C_1	680pF 50V	Capacitor, UP125B681K	Taiyo Yuden*
C_2	3300pF 50V	Capacitor, UP125X332N	Taiyo Yuden*
C_3	.022μF 16V	Capacitor, EP125Y223N	Taiyo Yuden*
C_{10}	470pF 50V	Capacitor, UP125B471K	Taiyo Yuden*
C_4,C_6,C_8,C_9 C_{11},C_{12},C_{14}	.1μF 50V	Capacitor, C43C104MNP	Corning
C_5,C_7, C_{13},C_{17}	2.2μF	Tantalum Capacitor 150D225X9020A2	Sprague

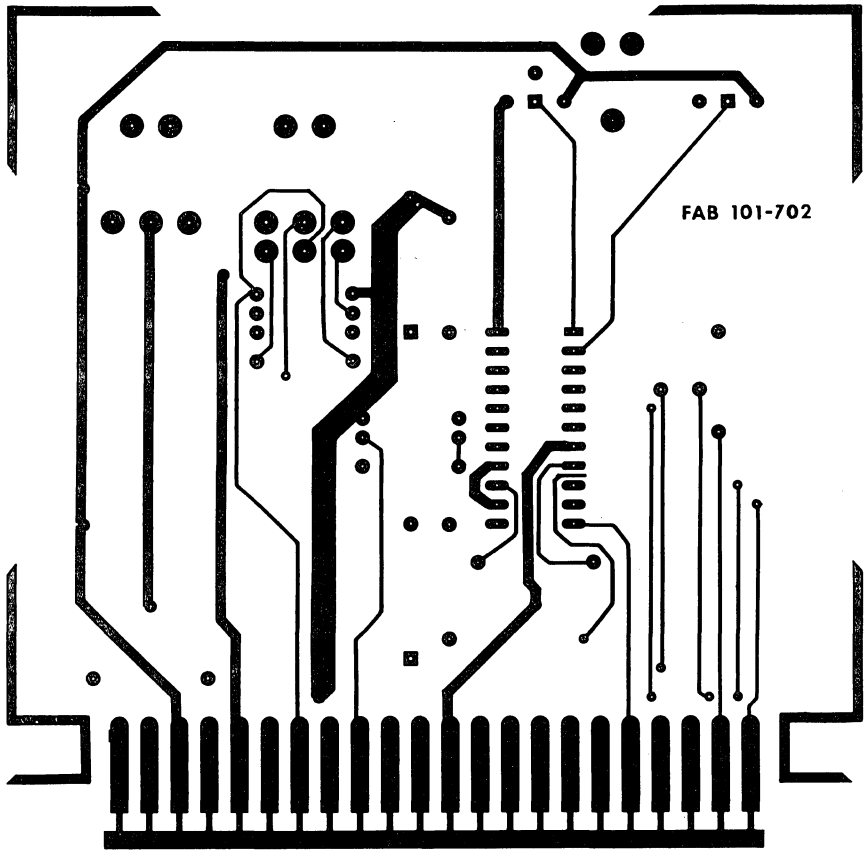
The capacitor part numbers are compact capacitor for PC mounting.

*Taiyo Yuden is available through SaRonix in Palo Alto, California.

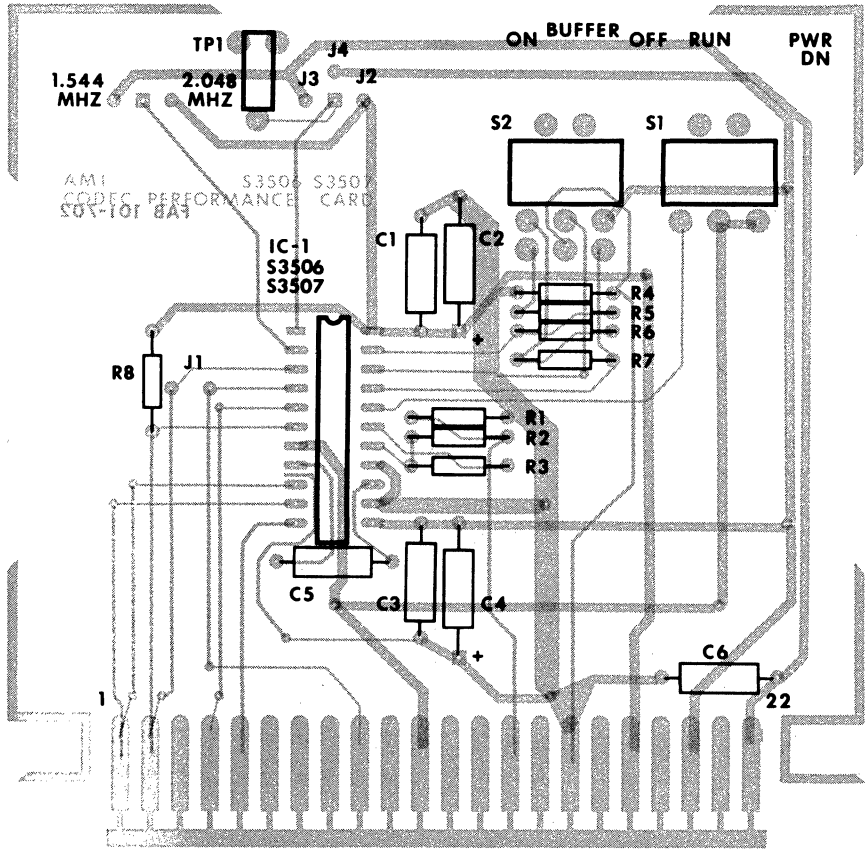
Component Side Metal Pattern



Back Side Metal Pattern



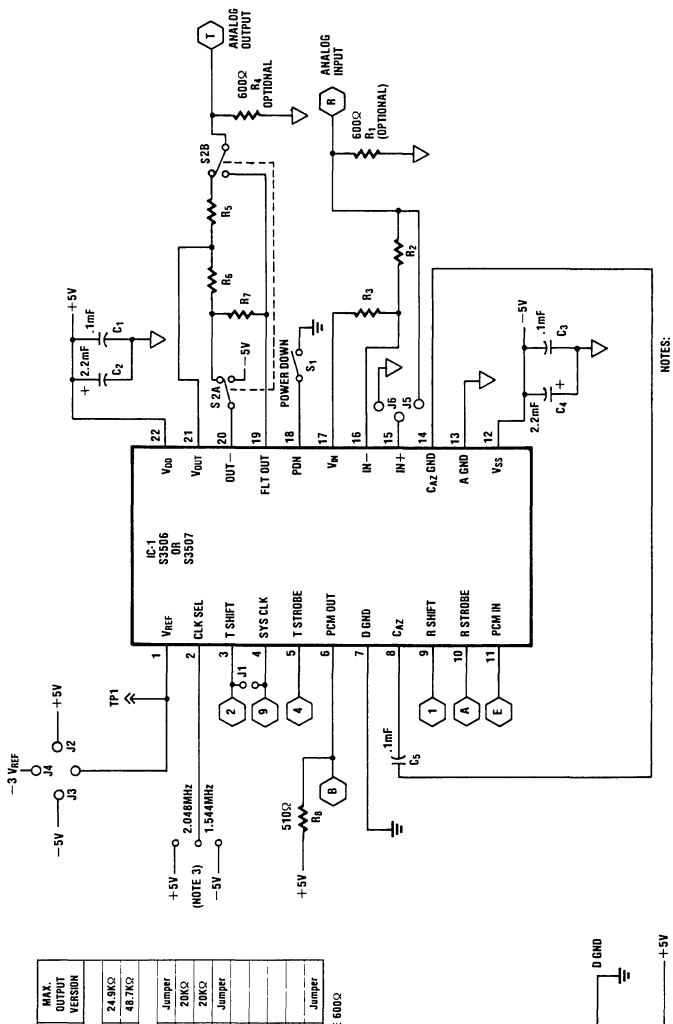
Assembly Information



Parts List

Ref. #	Part #/Value	Description
S_1	MTM-106D-RA	Switch SPDT Alco
S_2	MTM-206N-R	Switch DPDT Alco
TP_1	450-3888-01-04-00	Cambion
	506-4488-01-00-14	Cambion
C_2, C_4	2.2mfd	Capacitor Tant.
C_1,C_3,C_5	.1mfd	Capacitor Ceramic
R_8	510Ω 5% ¼W	Resistor

Schematic Diagram



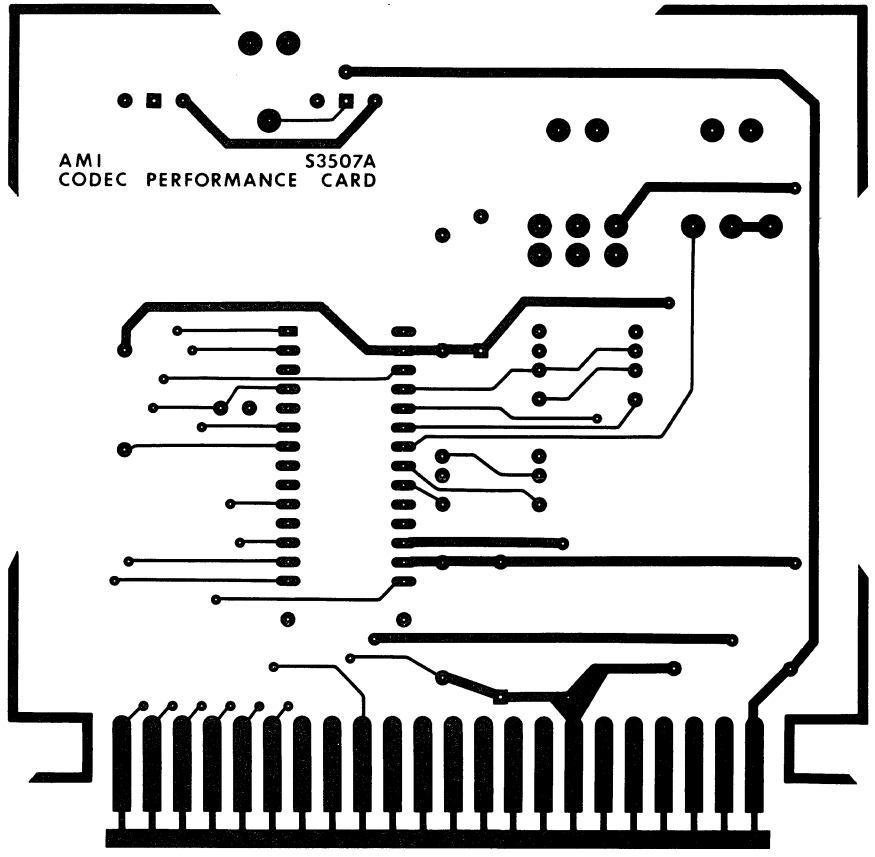
NOTES:
1. TERMINATION RESISTORS R_1 AND R_4 OPTIONAL.
2. RESISTORS R_2 THRU R_7 VALUES ARE DEFINED IN APP. NOTES.
3. JUMPER MUST BE USED IN EITHER 2.048MHz OR 1.544MHz (1.536MHz) TO DEMOTE SYSTEM CLOCK FREQUENCY.

RESISTOR/JUMPER SELECTION

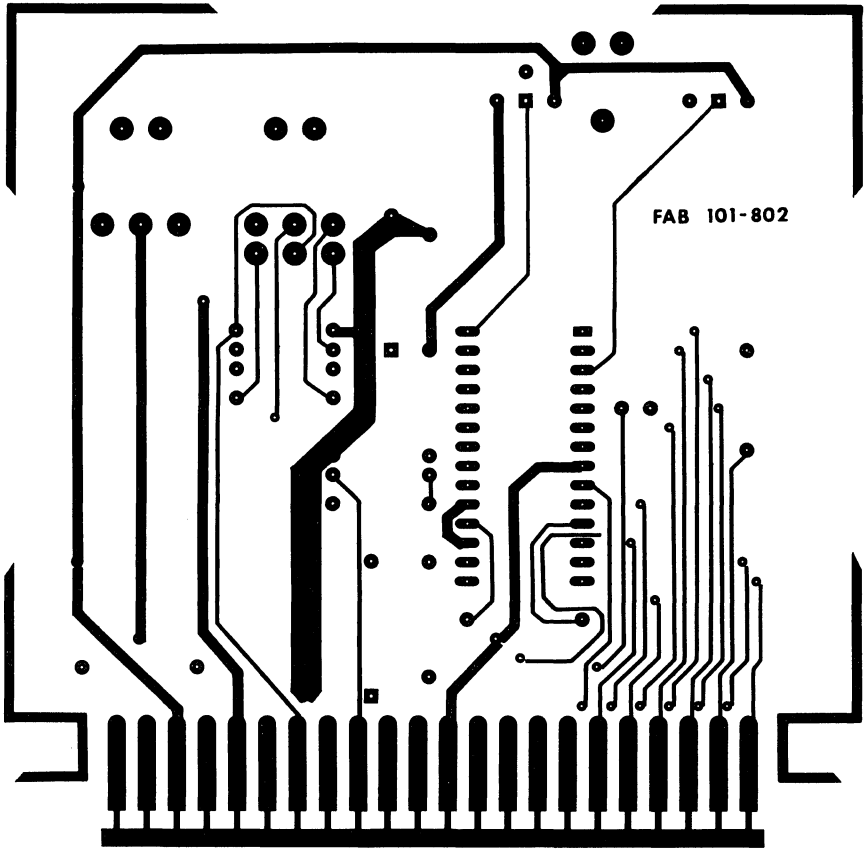
	MINIMUM PART VERSION	1 = 1 VERSION	0dBm/ OTLP(1200)	0dBm/ OTLP(600)	MAX. OUTPUT VERSION
R_1	NU	(NOTE 1)			
R_2	NU	20KΩ	24.9KΩ	24.9KΩ	24.9KΩ
R_3	Jumper	20KΩ	48.7KΩ	48.7KΩ	48.7KΩ
R_4	NU	(NOTE 1)			
R_5	Jumper	600Ω	600Ω	Jumper	Jumper
R_6	20KΩ	20KΩ	20.5KΩ	24.9KΩ	20KΩ
R_7	20KΩ	20KΩ	20.0KΩ	48.7KΩ	20KΩ
J_1	Jumper	Jumper	Jumper	Jumper	Jumper
J_2					
J_3					
J_4					
J_5	Jumper				
J_6		Jumper	Jumper	Jumper	Jumper

NOTE: IF TERMINATED INPUTS & OUTPUTS ARE DESIRED USE 600Ω RESISTOR.

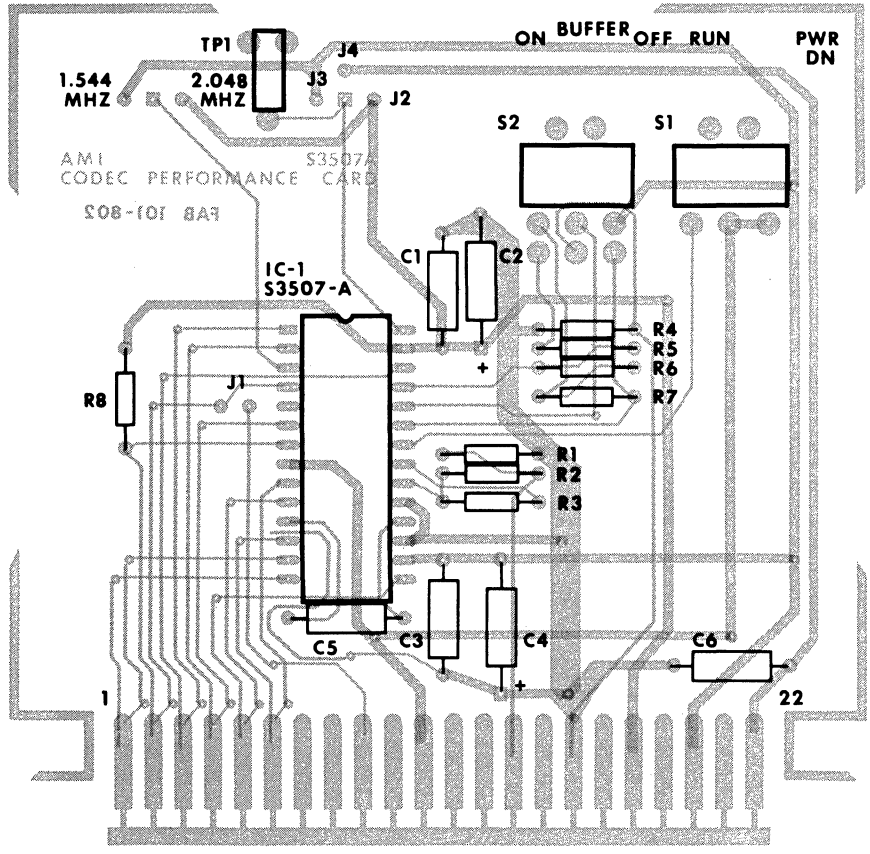
Component Side Metal Pattern



Back Side Metal Pattern



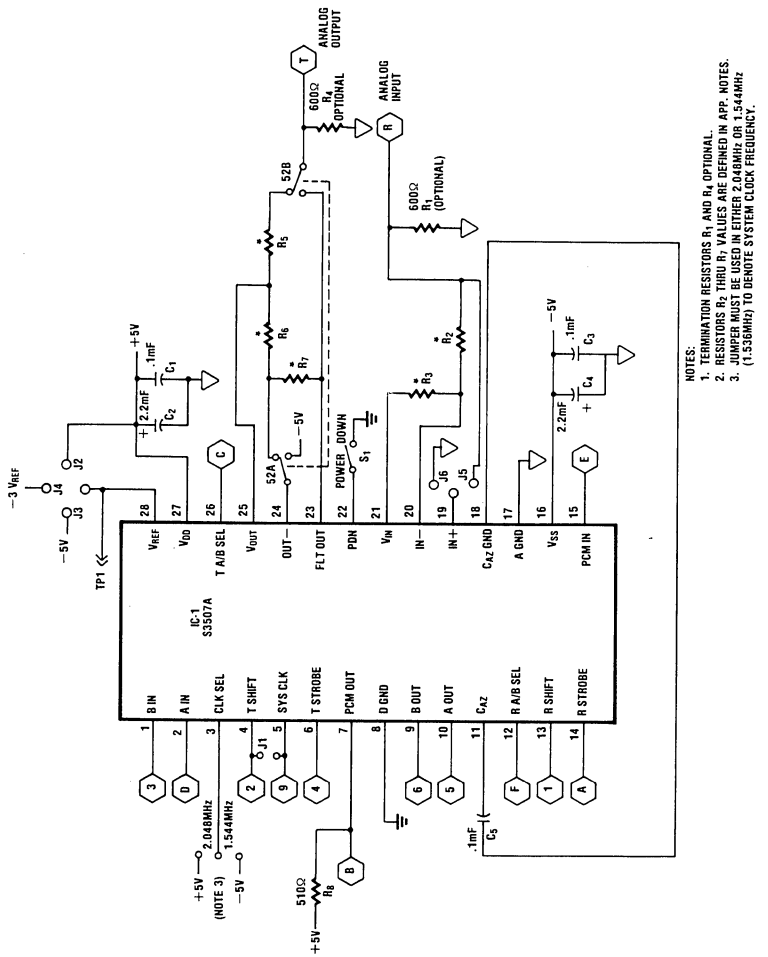
Assembly Information



Parts List

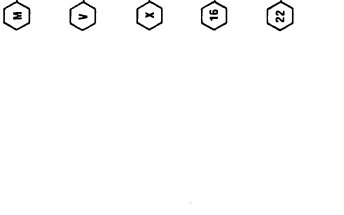
Ref. #	Part #/Value	Description
S_1	MTM-106D-RA	Switch SPDT Alco
S_2	MTM-206N-R	Switch DPDT Alco
TP_1	450-3888-01-04-00	Cambion
	506-4488-01-00-14	Cambion
C_2, C_4	2.2mfd	Capacitor Tant.
C_1,C_3,C_5	.1mfd	Capacitor Ceramic
R_8	510Ω 5% ¼W	Resistor

Schematic Diagram

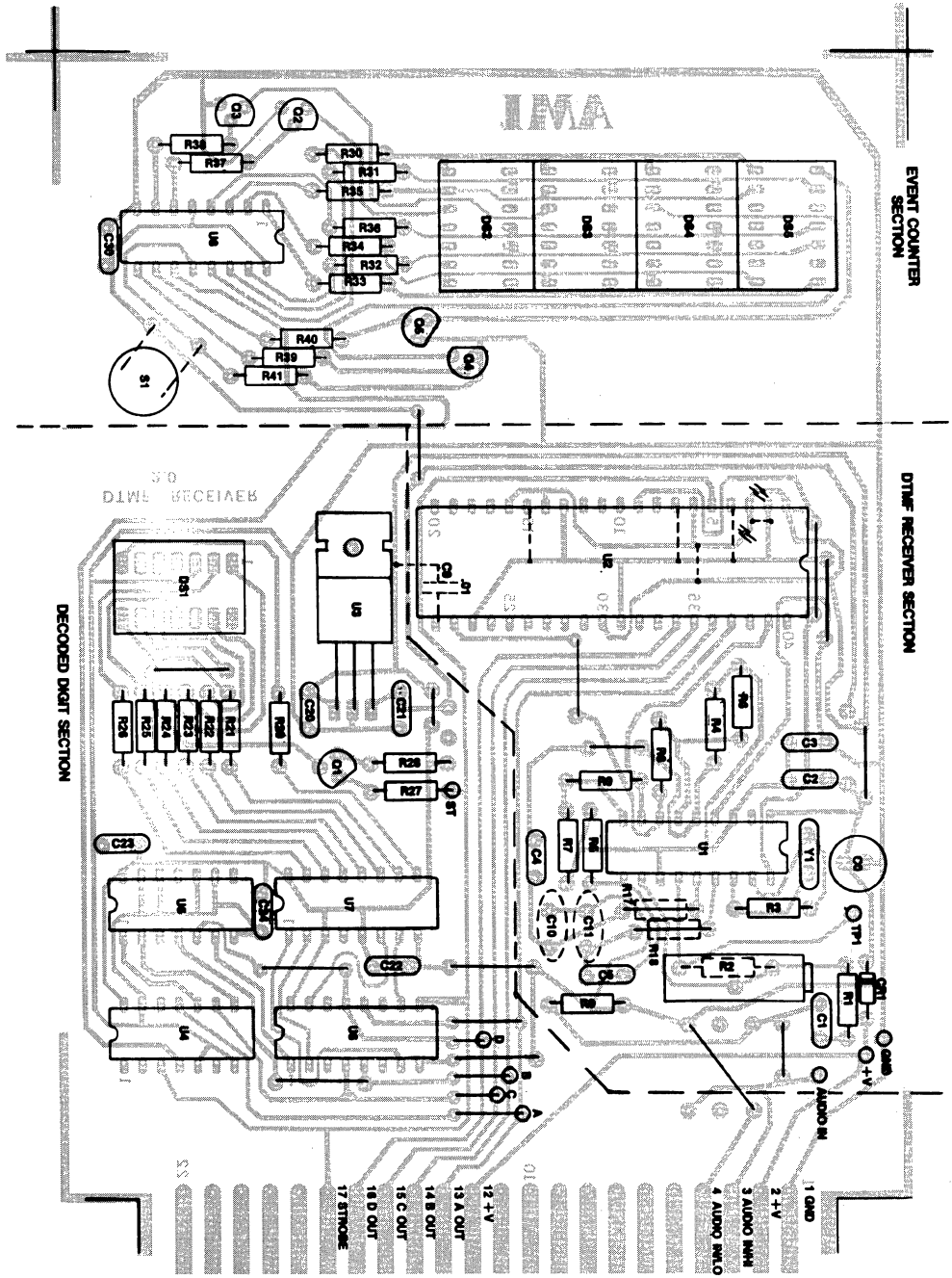


	MINIMUM PART VERSION	1=1 VERSION	0dBm/ DTLP(1200)	0dBm/ DTLP(600)	MAX. OUTPUT VERSION
R_1	NU		(NOTE 1)		
R_2	NU	20KΩ	24.9KΩ	24.9KΩ	24.9KΩ
R_3	Jumper	20KΩ	48.7KΩ	48.7KΩ	48.7KΩ
R_4	NU		(NOTE 1)		
R_5	Jumper	600Ω	600Ω	Jumper	Jumper
R_6	20KΩ	20KΩ	20.5KΩ	24.9KΩ	20KΩ
R_7	20KΩ	20KΩ	20.0KΩ	48.7KΩ	20KΩ
J_1	Jumper	Jumper	Jumper	Jumper	Jumper
J_2					
J_3					
J_4					
J_5	Jumper				
J_6		Jumper	Jumper	Jumper	Jumper

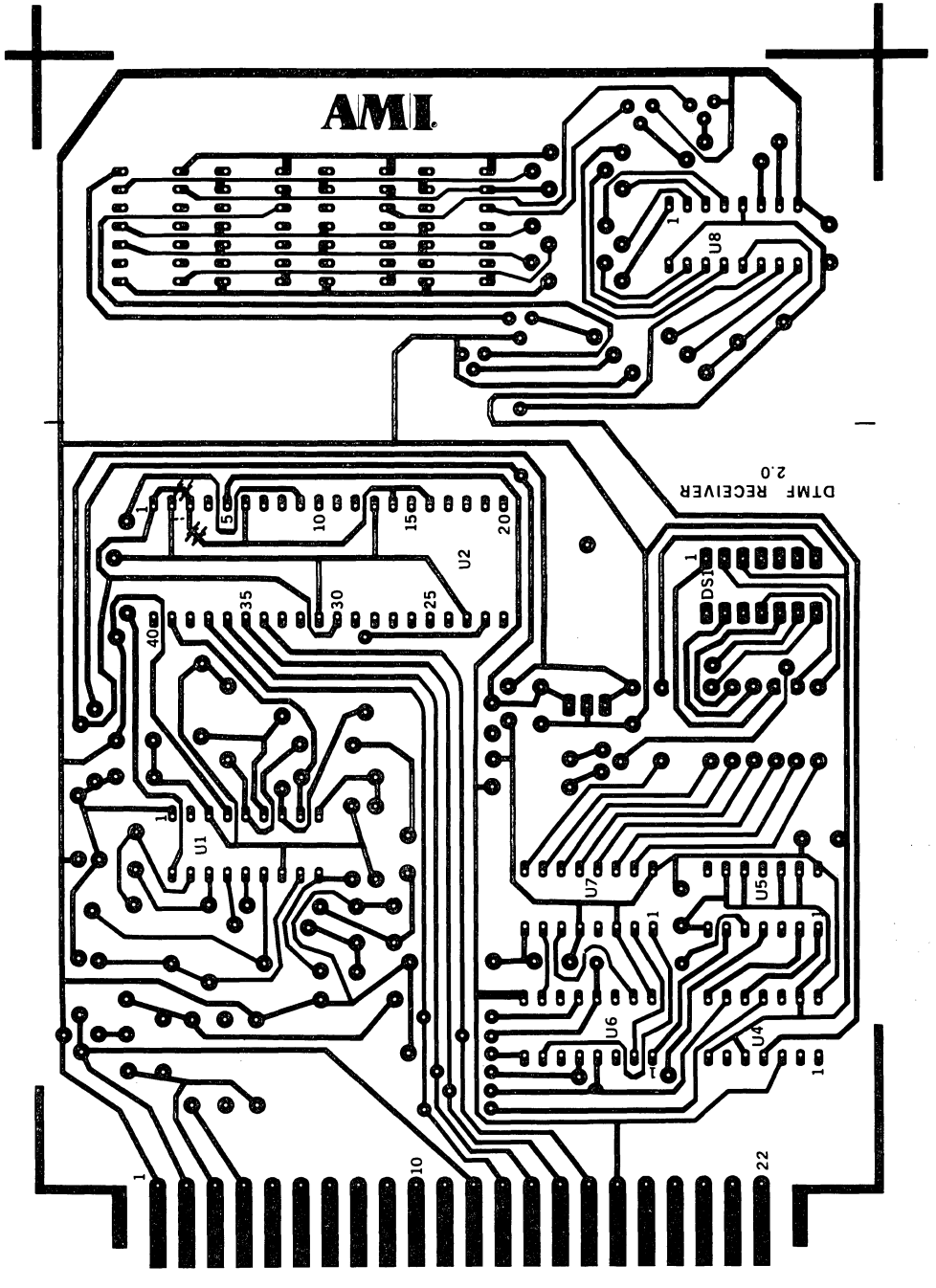
NOTE 1: IF TERMINATED INPUTS & OUTPUTS ARE DESIRED USE 600Ω RESISTOR.



Assembly Information



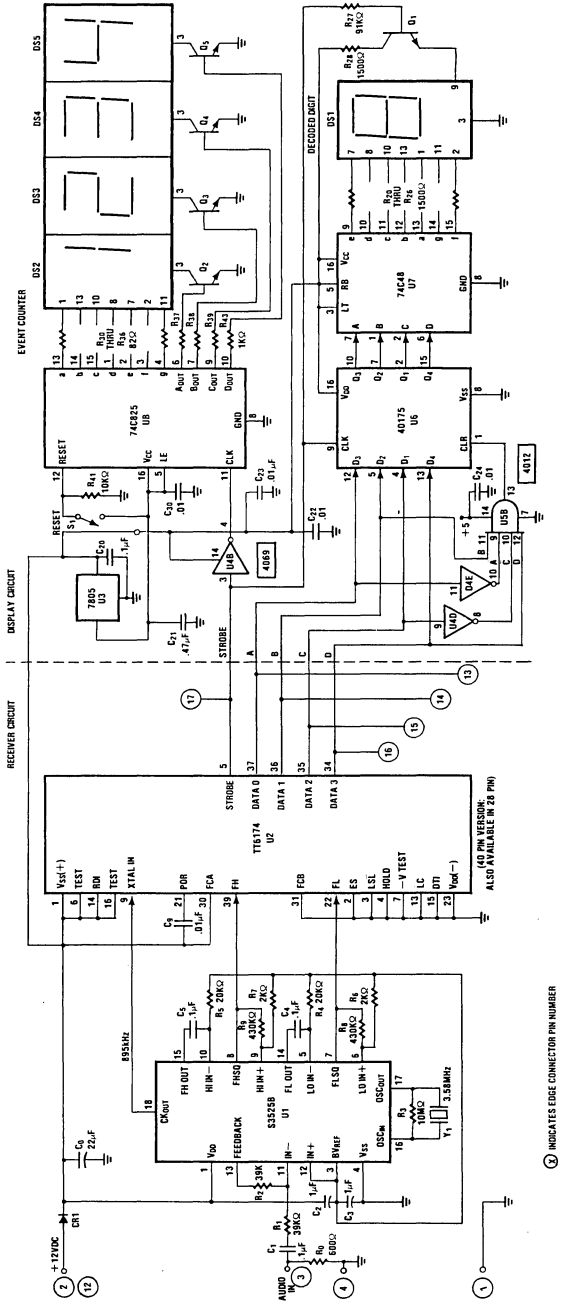
Back Side Metal Pattern



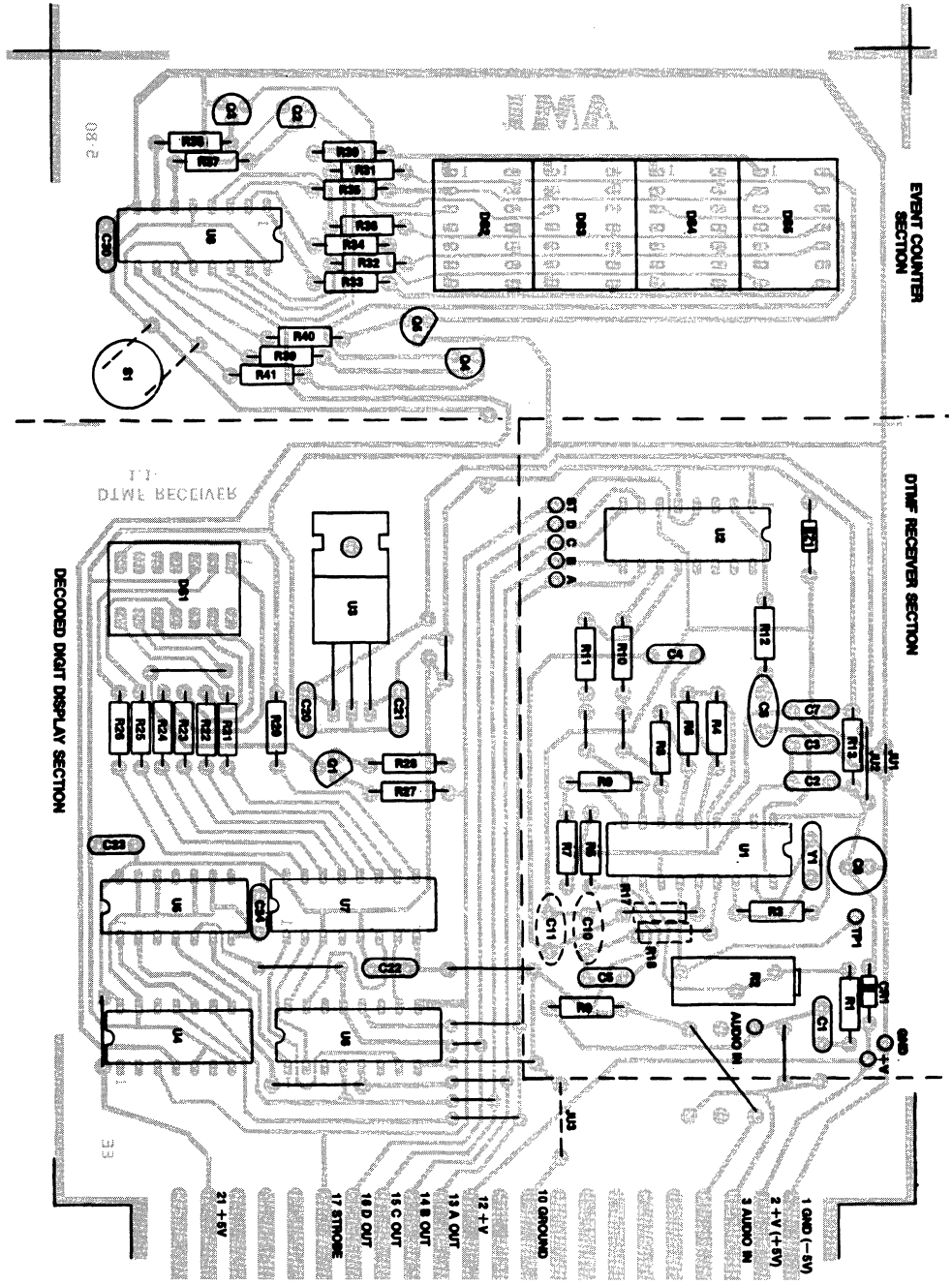
Parts List Board Version 2.0

Ref. #	Part #/Value	Description	Comments
R_0	600Ω	Resistor ¼W	Optional termination
R_1	39KΩ	Resistor ¼W	
R_2	39KΩ	Resistor ¼W	or 50K potentiometer (Bourns 3006P)
R_3	10MΩ	Resistor ¼W	
$R_{4,5}$	20KΩ	Resistor ¼W	
$R_{6,7}$	2KΩ	Resistor ¼W	
$R_{8,9}$	430KΩ	Resistor ¼W	
R_{10} to R_{16}	Not Used	Resistor ¼W	
$R_{17,18}$	1KΩ	Resistor ¼W	Optional-jumper out normally
C_0	22μF	Capacitor	
$C_{1,4,5}$	.1μF	Capacitor	
$C_{2,3}$	1μF	Capacitor	
$C_{6,7,8}$	N/U	Capacitor	
C_9	.01μF	Capacitor	
$C_{10,11}$	470pF 50V	Capacitor	Optional - leave open normally
U_1	S3525B	Integrated Circuit	AMI Bandsplit Filter
U_2	TT6174	Integrated Circuit	Teltone Digital Tone Decoder
CR_1	IN4004	Diode, Zener Diode	Optional - Polarity protection
Y_1	3.58MHz	Crystal	Saronix NYPO35A or equivalent
		Display Section	
R_{20} to $R_{26,28}$	1500Ω	Resistor ¼W	
R_{27}	91KΩ	Resistor ¼W	
R_{30} to R_{36}	82Ω	Resistor ¼W	
R_{37} to R_{40}	1KΩ	Resistor ¼W	
R_{41}	10KΩ	Resistor ¼W	
$C_{20,30}$	.1μF	Capacitor	
C_{21}	.47μF	Capacitor	
$C_{22,23,24}$	.01μF	Capacitor	
Q_1 to Q_5	2N4401	Transistor	
U_3	7805	5V Regulator	
U_4	4069	Hex Inverter	
U_5	74C20	Dual 4-Input NAND Gate	
U_6	40175	Quad D Flip-Flop	
U_7	74C48	BCD-to-7 Segment Decoder	(CD4511B Substitute)
U_8	74C925	4-Digit Counter/Display Driver	
DS_1 to DS_5	HP5082-7653	LED Displays	

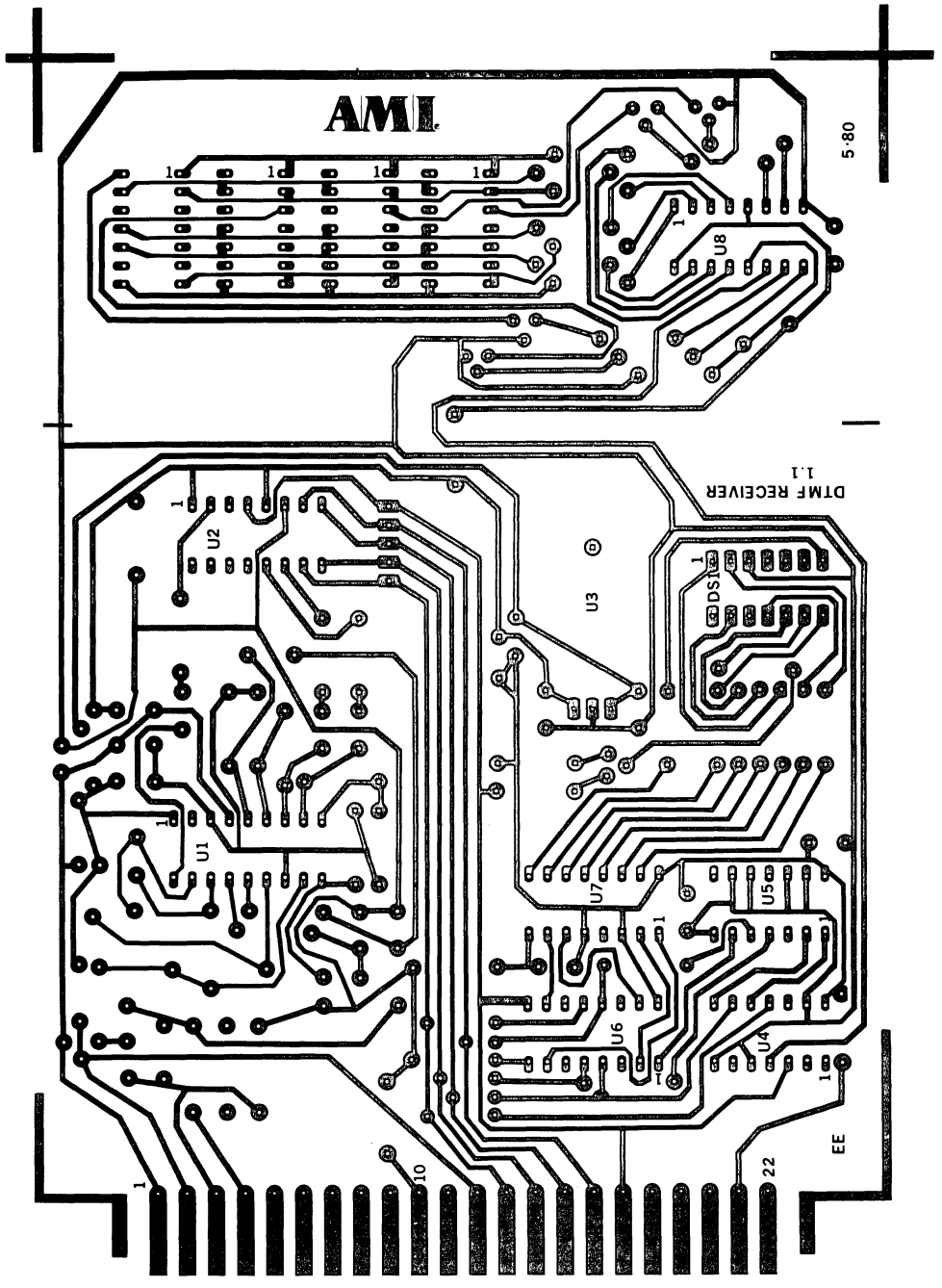
Schematic Diagram (Version 2.0)



Assembly Information



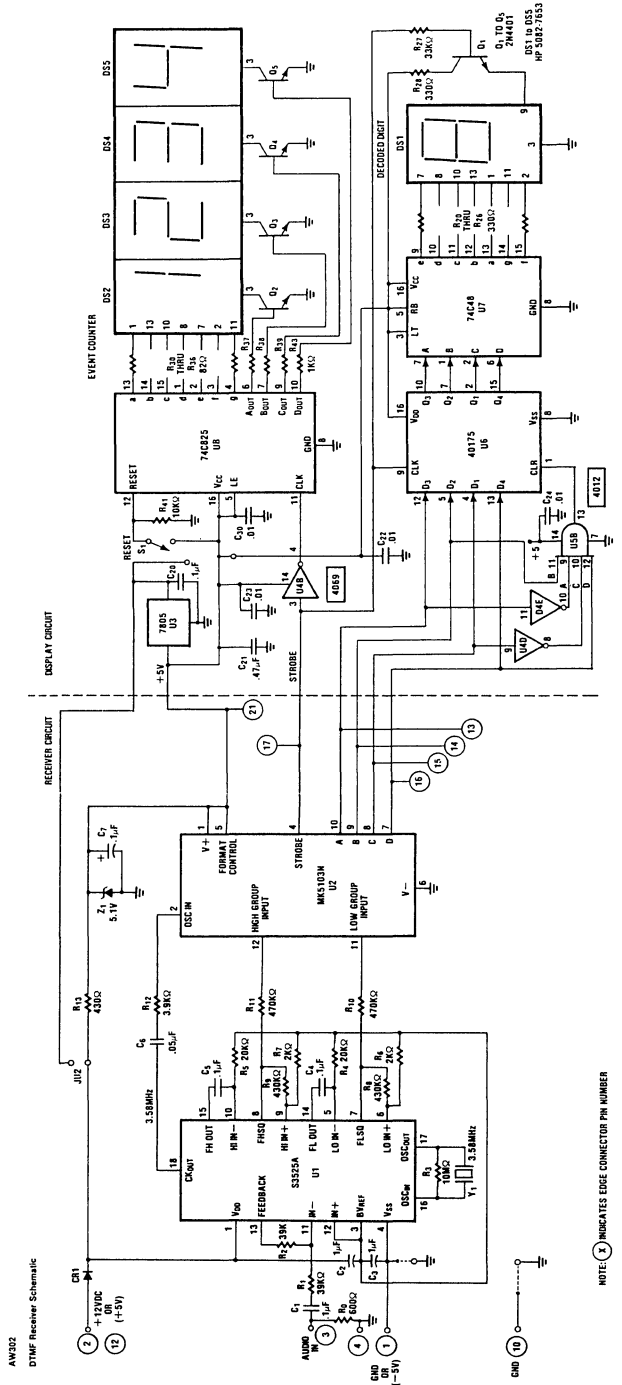
Back Side Metal Pattern



Parts List Version 1.1

Ref. #	Part #/Value	Description	Comments
R_0	600Ω	Resistor ¼W	Optional termination
R_1	39KΩ	Resistor ¼W	
R_2	50KΩ	Potentiometer	Bourns 3006P
R_3	10MΩ	Resistor	
$R_{4,5}$	20KΩ	Resistor	
$R_{6,7}$	2KΩ	Resistor	
$R_{8,9}$	680KΩ	Resistor	
$R_{10,11}$	470KΩ	Resistor	
R_{12}	3.9KΩ	Resistor	
R_{13}	430Ω	Resistor	Used with Z_1
$R_{14,15,16}$	N/U		
$R_{17,18}$	1KΩ	Resistor	Optional-jumper out normally
C_0	25μF	Capacitor	
$C_{1,4,5,7}$	.1μF	Capacitor	C_7 used only with Z_1
$C_{2,3}$	1μF	Capacitor	
C_6	.05μF	Capacitor	
$C_{8,9}$	N/U	Capacitor	
$C_{10,11}$	470pF 50V	Capacitor	Optional - leave open normally
U_1	S3525A	Integrated Circuit	AMI Bandsplit Filter
U_2	MK5102,03	Integrated Circuit	Mostek DTMF Decoder
CR_1	IN4004	Diode	Optional - Polarity protection
Y_1	3.58MHz	Crystal	Saronix NYPO35A or equivalent
Z_1	IN4733A	5.1V Zener Diode	Used if display section deleted
		Display Section	
U_3	7805	5V Regulator	
U_4	4069	Hex Inverter	
U_5	74C20	Dual 4-Input NAND Gate	
U_6	40175	Quad D Flip-Flop	
U_7	74C48	BCD-to-7 Segment Decoder	CD4511B substitute
U_8	74C925	4-Digit Counter/Display Driver	
Q_1 to Q_5	2N4401	Transistor	
DS_1 to DS_5	HP5082-7653	LED Displays	
S_1	SPST	N/O Pushbutton Switch	
R_{20} to $R_{26,28}$	330Ω	Resistor	
R_{27}	33KΩ	Resistor	
R_{30} to R_{36}	82Ω	Resistor	
R_{37} to R_{40}	1KΩ	Resistor	
R_{41}	10KΩ	Resistor	
C_{20}	.1μF	Capacitor	
C_{21}	.47μF	Capacitor	
$C_{22,23,24}$	.01μF	Capacitor	
C_{30}	1μF	Capacitor	

Schematic Diagram (Version 1.1)



Articles

Semiconductors provide new features

by Victor Godbole

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Semiconductors provide new features

While telephone equipment has been produced providing new features, most of these phones need auxiliary power sources. The challenge is to provide these features on line-powered telephones

Victor Godbole

SINCE THE Federal Communications Commission (FCC) changed the rules to provide for direct connection of registered privately manufactured telephone equipment to the telephone network, quite an array of independent add-on equipment has appeared on the market.

The equipment offers features and styles not previously available in phones, including automatic dailing and redialing, hands free dialing, call monitoring, built-in calculators, call timers, numeric displays, electronic tone ringers, and multifeature speaker phones. Most such consumer phones, however, require auxiliary power sources either from ac lines or off-line batteries for their operation. Interface to the network is relatively straightforward and could be standardized.

The electronics in such equipment are not constrained by network characteristics or the limited telephone system power. Using non-system power, any function that is feasible and marketable is practical. The new equipment can, therefore, choose from a wide range of technologies and components.

The real challenge is to provide features *within* conventional telephones powered from the tip and ring alone. Major telephone manufacturers in the U.S. have taken on this challenge as they begin to replace many electromechanical elements of the conventional 500 type telephones with semiconductors.

VICTOR GODBOLE is Manager of Telecommunications Applications for American Microsystems, Inc., Santa Clara, Cal.

Telephone and semiconductor manufacturers have found that task is tricky to say the least. Semiconductors have to meet three stiff requirements: the harsh telephone environment, low cost criteria and performance as good as existing equipment. To be widely accepted, integrated circuits must offer significant advantages in cost or performance over the electromechanical alternative.

The telephone environment

The telephone represents a far from ideal environment for electronic circuits. The power supply is unregulated, has a high source impedance and the amount of power available is limited. This is because power is supplied to the telephone by the central office (CO) battery system over a copper wire loop. The effective resistance of the loop, which increases in proportion to the distance between the telephone and the CO, can vary from a few hundred ohms to over 2400 ohms. The total direct current available to the phone, therefore, can vary over a range from 80mA down to 20mA while the direct voltage across the phone terminals can vary from 10 volts down to 3 volts.

Since signaling and speech transmission is done over the same pair of wires that carries power to the telephone, this presents additional problems to the electronic circuits. Circuits that perform the tone signaling function in effect modulate their own power supply while those used for pulse dialing must continue to operate from a very high impedance source (over 100k ohms) during the "break" state of the dialing sequence. In the normal voice mode these circuits must also present a high impedance to the speech signals. Additionally, the electronic circuits must be protected from the possibility of large induced surge voltages due to lightning.

It is not difficult to identify the major functional electromechanical elements of a 500 type telephone open to replacement by solid state circuits. The signaling functions of tone dialing and pulse dialing, the alerting function of the bell ringer and the speech function of the speech network form conceptually simple blocks suitable for solid state integration. These major functions could be implemented by four large scale integration (LSI) circuits.

The signaling functions require low power and wide operating voltage range, therefore, low power complimentary metal semiconductors (CMOS) must be used for them. The tone ringing function could be implemented either with CMOS or bipolar technology. Due to very low operating voltage requirements, at present, only bipolar technology can be considered for the solid state speech network. Several off the shelf (mostly CMOS) LSI circuits are already available for the signaling and alerting functions (see Table 1). There is no standard circuit available for the speech network, but the semiconductor manufacturers as well as the telephone manufacturers are developing a solid state alternative.

Tone dialing circuits

Off the shelf solid state tone dialing integrated circuits (IC) have gained acceptance among telephone manufacturers such as International Telephone & Telegraph Corp. (ITT), Stromberg-Carlson, American Telecommunications and General Telephone & Electronics Corp. (GTE) for replacement of conventional electromechanical dual tone multifrequency (DTMF) tone dials, despite several major problems in the integration of these devices in the telephone environment. The key factors influencing this trend are: the potential for significant cost reduction in the keyboard mechanics, improved frequency accuracy and stability of these devices and facility in adding new features.

Table 1

Semiconductors for line-powered telephone sets—LSI devices

Function	Operating requirements	How is function typically performed?	Benefits of solid state approach	Problems faced by semiconductors	Devices now in use or in design at major North American telephone manufacturers	Comments
Tone Dialing	Supply voltage during tone dialing: 2.75V-10V. During voice mode: 1.7V-10V. Outputs for electronic muting of transmitter and receiver.	CMOS LSI circuit in conjunction with a crystal time base and few discrete components including FET or transistor switches for transmitter, receiver muting.	Reduction in cost of keyboard mechanics. Improved frequency accuracy and stability.	Meeting the amplitude and distortion specifications over the range of loop currents and temperature. Maintaining transmitter and receiver efficiencies at the same levels as obtained with mechanical contacts.	AMI S2559, S2859 Family, MOSTEK MK 5087 Family	AMI S2859 features sequenced outputs for transmitter, receiver muting, to eliminate receiver "clicks" during push and release of buttons. The first phase of solid state tone dialing phones manufactured use mechanically switched muting.
Pulse Dialing	Supply voltage range 1.5V-5.5V low operating current (<200 μA). Low memory retention current (<1 μA).	CMOS LSI circuit in conjunction with a RC oscillator and several discrete components including FET or transistor switches for dial pulsing and receiver muting.	Provides keyboard convenience and fast number entry for rotary dialing. Last number redial capability.	Relatively high cost of electronics to implement the function.	AMI S2560 A, MOSTEK MK 5098, 5099, National MM 5393, Siliconix DF320 other custom circuits	
Tone Ringing	Operate from ringing voltages in the range of 42-105 VAC, Draw less than 5 mA, provide at least 80 dB sound pressure thru a suitable transducer.	Bipolar or CMOS circuit with the output stage designed to drive a speaker thru a transformer or for direct driving of a ceramic transducer or high impedance speaker.	Cost reduction in the future is expected. Desirable features such as 3 level sequenced ringing is available.	Simulating the sound of the conventional telephone bell, providing desired level of audio output. Providing high impedance to non-ringing frequencies.	Custom bipolar circuit (GTE). AMI S2561, Mitel ML8204	Solid state tone ringing is not widely accepted by public and telephone manufacturers.
Speech Network	1.7V-10V	Bipolar LSI circuit in conjunction with dynamic transducers for microphone and earphone elements.	Lower cost, built in loop length compensation, better equalization.	Operate when two telephones in parallel at the low end of the loop current range.	Custom bipolar LSI circuit (Northern Telecom) discrete bipolar circuitry.	Work in experimental and prototype stage. Not marketed in U.S.

Conventional electromechanical keyboard arrangements require dual contact keys with multiple common contacts for energizing the individual loading coil (LC) oscillators and for muting of the microphone and receiver elements. The solid state ICs permit use of a simpler keyboard with a single contact per key. On-chip transmit and mute drivers now permit muting via external field-effect transistor (FET) or transistor switches.

For better accuracy and stability a low cost TV crystal serves as the master time base from which digital countdown circuitry derives individual frequencies. Temperature sensitivity and long term drift are almost completely eliminated by this technique. Other solid state ICs easily can be added around the tone dialing ICs to provide features that were either simply not possible or were impractical with the conventional electromechanical approach.

The major problems confronting all electronic tone dialing schemes in 500 type telephones sets have been (1) transient voltage protection of electronics; (2) need for polarity guard diode bridges; (3) re-

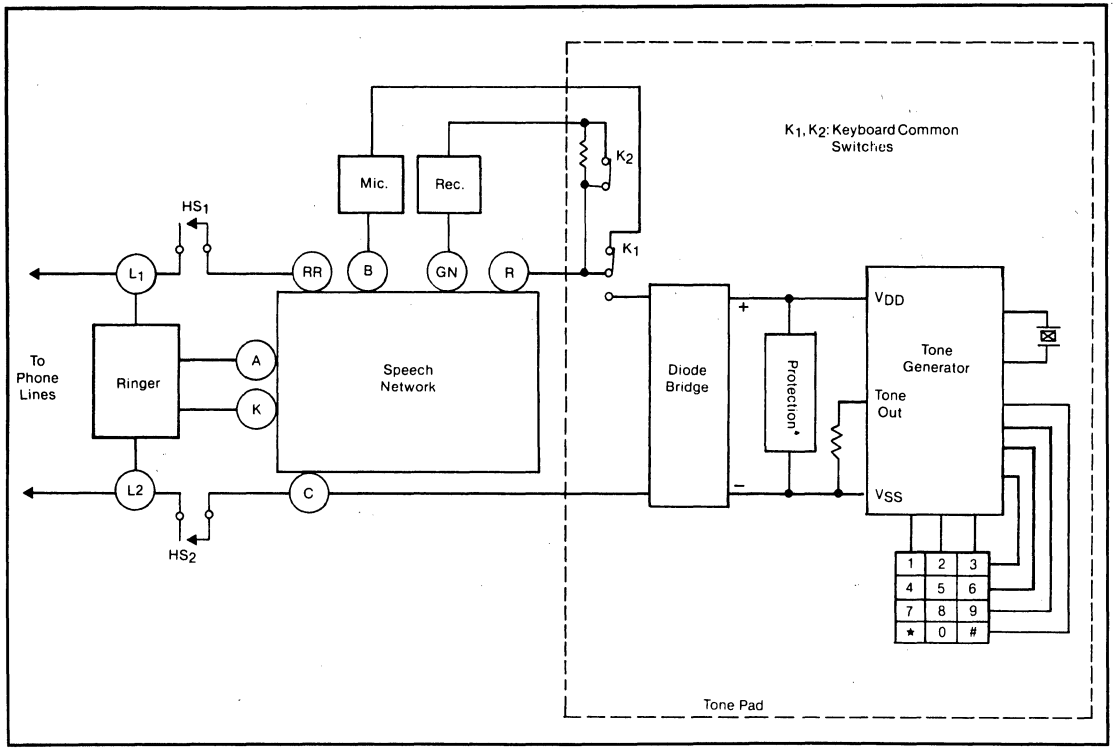


FIG. 1 *Compromise adaptation of solid state tone dialing in a 500 type telephone.*

duction in transmission efficiency due to insertion of the diode bridge in series with the transmission path; (4) reduction in transmission efficiency due to insertion of the "imperfect" solid state switches in series with the transmission path; and (5) degradation of performance (specifically distortion) at lower loop currents (that is, when operating over long loops, where the instantaneous voltages across the tone dialing ICs are very low because the signal rides on the supply voltage itself). The additional voltage drop (about 1.4 volts) contributed by the diode bridge makes matters worse. Finally, there are two more problems: (6) lower amplitude levels are usual with the solid state approach and (7) objectionable "clicks" are heard in the earpiece during the push and release of the key.

Table 2

Semiconductors for line-powered phone sets—discrete components

Function	How is function typically performed?	Typical components
Polarity guard	A diode bridge formed with four silicon high voltage breakdown, high current capacity diodes.	1N 4004 or equivalent
Protection network	A current limiting resistor (high wattage low ohmic value) in conjunction with a varistor or zener diode with a breakdown voltage in excess of 110V.	20Ω 2W carbon composition resistor, Varistor GE MOV-150 type or zener diode 1N 5379 equivalent
Dial pulsing contact	High voltage breakdown PNP or NPN transistor or FET switch.	2N 5401, 2N 5550

Most major telephone manufacturers have adopted the compromise solution shown in Fig. 1 as the first phase for integration of the tone dialing ICs in the telephone.

In the compromise solution, the dual contact, multiple-common-terminal keyboard is retained, which eliminates problems 4 and 7 above. The diode bridge is moved so that it is in the transmission path only during tone dialing, and this eliminates problem 3. Since all electronics are now behind the primary winding of the speech network, transient voltage protection is simplified. Note that the electronics are powered during the closure of a key and otherwise disconnected. A 5-watt zener diode with a breakdown in the 12 to 15 volt range is adequate for protection, thus solv-

ing problems 1 and 3. Only problems 2, 5 and 6 remain at this point. Newer versions of tone dialing ICs are specifically designed to operate at a lower voltage (2.5V) to alleviate the problems somewhat. In general, all industry objectives are met; although some with only a minimum margin.

Even though a major cost savings does not result with the compromise solution, it has provided a starting point for integration of solid state devices in the telephone. The experience gained by both the telephone manufacturers and semiconductor manufacturers in the integration of these devices has led to a better understanding of their mutual problem areas.

The all electronic tone dialing scheme is feasible and will become practical soon with the availability of lower cost FET switches for performing the transmitter and receiving muting. Design for this second phase of integration of tone dialers is underway at present at most of these telephone manufacturers.

The major motivation for replacing the rotary dial with a solid state circuit is certainly not cost savings. In fact, the reverse is true. The major benefits of the solid state approach are that it provides push-button convenience for rapid entry of the dialed number, and that a user can redial the last dialed number at the touch of a button.

With the use of low voltage CMOS integrated circuits, it is possible to design the pulse dialers with sub-microamp current requirements for memory retention. This allows the circuit to be powered through a very large resistance (10-50M Ω) during the on hook state.

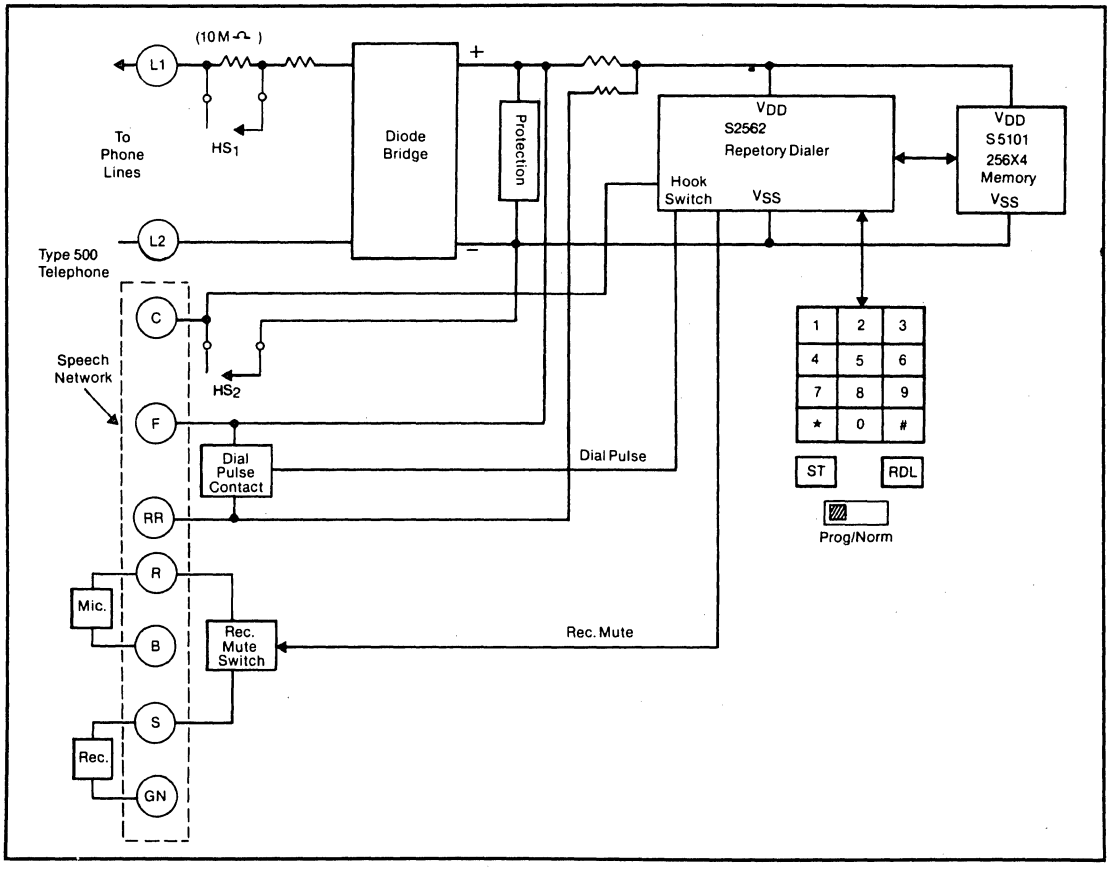
Most of the sample problems outlined for the tone dialing circuits also confront semiconductor pulse dialing. However, a compromise solution, where the electronics are only powered during the key closure, cannot be adapted here since the circuits must be powered continuously. High voltage transistors or FETs must be used for the dial pulse contact and receiver meeting. This contributes to increased cost. The increase in cost is also due to the necessity for a several digit buffer memory (up to 20 digits) in the pulse dialer IC to allow rapid number entry and redialing of the last dialed number.

It is possible that some years from now, the cost of the solid state approach could come down to the level of the rotary dial, since all solid circuit costs tend to decrease with higher volume production.

Tone ringing circuits

The electronic alternative to the bell typically consists of a tone ringer IC, a few discrete components such as a diode bridge to rectify the ac ringing signal and a filter capacitor and an audio output

FIG. 2 *A line-powered repertory dialer.*



device (either a speaker or a transducer). The electronic ringer has been used in some key telephone and private automatic branch exchange (PABX) systems. Recently, it has found a place in such consumer products as the GTE FlipPhone.

There are many reasons why the electronic alternative has not yet been widely accepted for the conventional 500 type telephones. Some of these reasons are:

- The electronic sound differs considerably from a bell. It is generally a tone that shifts between two audio frequencies, for example, 512 and 640 Hz, at a low frequency rate, about 16 Hz, to create a warble effect to simulate the bell. Consumer acceptance of such a sound may be slow in coming.
- The electronic sound is not as a loud as the bell owing to the limited power that can be drawn from the ringing signal. The speaker or transducer is not as efficient an audio output device as the bell.
- The impedance presented by the bell to non-ringing frequencies is quite high due to its resonant characteristic. On the other hand, the electronic ringer presents an impedance determined by the coupling capacitance and series resistance. Therefore, at low frequencies such as 10 Hz the impedance is not much higher than at ringing frequencies of 20 Hz. The low impedance at 10 Hz causes dial pulse distortion. The toner ringer circuit must be designed to present a high impedance to non-ringing frequencies.

Most presently available tone ringer ICs do not have this characteristic.

- The mounting of the speaker or transducer in the telephone is an important factor in the intensity of sound produced. With existing phone design the speaker must be mounted facing down against the base. With most desk telephones this mounting arrangement reduces sound output. Thus, the mechanical design of the phone may have to be changed to adapt to the electronic ringers.
- The cost of the electronic alternative at present is at best equal to the mechanical bell. There is no clear cost advantage to allow trade-offs in the performance area.

The electronic ringer offers some unique features and advantages, however. Weight and space savings are considerable. The sound can be personalized to distinguish one phone from another, which could be helpful in office situations.

Some of the tone ringer ICs offer the interesting feature of amplitude sequencing. The first "ring" is at the lowest level. The second "ring" increases to a medium level and the third and consecutive "rings" are at the maximum level. This is highly desirable when there are several telephones in a small area, as in office situations. In homes, this could be a useful feature especially for phone calls received at night, to prevent rudely awakening the called person.

Most of the problems mentioned above are solvable. Transducer manufacturers like Goulton and Murata are working on lowering the resonant frequency to make the sound more acceptable. The impedance at resonance is also being increased to allow direct interface to the ringer ICs.

Speech network

The speech network in the telephone performs the equalization (equalizing speech levels to compensate for variations in loop currents) and sidetone balancing (limiting the amount of the talker's signal appearing in his own receiver) functions.

The conventional speech network is a passive circuit comprising a three winding transformer which separates the transmission and receiving paths, carbon transmitter, magnetic receiver, two varistors for equalization and a resistance-capacitance (RC) network for sidetone balance.

The major disadvantage of the conventional speech network is that it is bulky and expensive to produce. The carbon microphone is both noisy and relatively unreliable and the efficiency of its output varies considerably with the loop current. An active speech network using bipolar technology and dynamic transducers to replace the carbon microphone and magnetic receiver forms the electronic alternative to the conventional passive network. At least two bipolar LSI circuits have been developed recently—one by Northern Telecom for their electronic telephone for Bell Canada and another by SGS-ATES.

Basically, the LSI speech network consists of a regulator, transmit/receive amplifiers and a bridge circuit for balancing. Additionally, it may consist of a power supply for the tone generator. Gain of the amplifier is automatically adjusted in proportion to the variation in loop current. The electronic speech network provides better equalization performance than conventional speech networks. The drawback of the present LSI circuits is that they only operate down to 3v dc. When two telephones are in parallel over a long loop (20 mA) the dc voltage across the network can go down to as low as 1.7 volts. For this reason, electronic telephones using the LSI speech network have not been marketed in the U.S.

The recently developed low voltage bipolar op-amps could be redesigned to work on lower voltage levels. Work is also going on at semiconductor manufacturers such as American Microsystems on a low voltage CMOS op-amp. With CMOS it will be possible to combine the speech network with either pulse dialing or tone dialing to make a single super LSI circuit.

A look at the future

The acceptance of solid state tone and pulse dialing devices within the conventional telephones has opened the door for incorporation of novel features that were simply not feasible with the electromechanical approach. The availability of the two spare keys facilitates implementation of such features. The features are implemented by adding circuitry around the tone generator or pulse dialer IC. The design of the additional circuitry is simplified due to the chip enable/disable facility provided on these ICs.

Hold and monitor

These are the easiest and most convenient functions that can be added to the telephone by adding two latches and a solid state switch to the tone or pulse dialing circuitry. A "hold" capacity permits the initiating party to carry on conversations or consultations without the listening party hearing them. A monitor capacity allows one to listen in (from an extension) to a phone conversation on the line without loading the line. The hold latch and the monitor latch are the essential elements. The latch is set

by depressing the associated key. To reset the latch and to revert to the normal operation one need only depress the appropriate key again. The hold latch operates the transmit mute switch so that the microphone is disconnected at the same time it operates a shunt switch such that a resistor (typically 200 ohms) is placed across the microphone. This ensures that the dc loop current will continue to flow and maintain the connection.

The latch also disables the tone generator so that the dual tone corresponding to the hold key is not generated. The receiver mute switch is not operated so that the initiating party continues to hear the other end. The monitor latch performs similar functions with the exception that the microphone shunt switch is not operated. The result is that the extension phone in the monitor mode does not draw significant dc current and conversations can thus be monitored without causing voice degradation.

Fixed number dialing

Another feature that can be added is the capability to dial a number simply by pushing a spare key. The number can be hardwired into the tone dial assembly. The advantage of this scheme is that the memory is non-volatile and thus does not require local power either from ac lines or batteries for retention. Further, the number is not easily modified. It cannot be changed from the keyboard.

The feature allows emergency number dialing or access to a specific service where the user does not know the access number. For emergency dialing either a three-digit code such as 911 or a local seven-digit number can be programed into the assembly.

A counter sequentially closes solid state switches connected between appropriate row and column inputs to simulate dialing the desired digits. A low frequency RC oscillator is gated on to sequence the counter through the states. A chip disable function available in the tone generator IC facilitates gating off the tone during the interdigit time. The oscillator frequency is adjusted so that the digit on/off time is about 50mS. Dialing of a seven-digit local number thus can be completed in less than a second.

Repertory dialing systems that allow automatic dialing of a large number of calls at the touch of a button have been available for quite some time. These are available either as ancillary devices or as an add-on to telephones. In either case these devices require local ac power or batteries for their operation.

The recent availability of low power, low voltage CMOS LSI circuits either in the form of general purpose microprocessors or specific devices, for the first time, make the prospect of a line powered repertory dialing telephone feasible. One such device, the AMI S2562, with a companion S5101 CMOS RAM (random access memory) can be used for pulse dialing or with the addition of a tone generator IC such as the S2559 can be used for tone dialing as well.

The key feature of both the S2562 and the S5101 is the low leakage (submicroamp) current requirements for data retention. This allows the devices to be powered from the tip and ring in the on hook condition without exceeding the on hook power limitations imposed by the telephone companies. Programing of numbers is done on the off hook condition. Since no dialing takes place during programing, numbers for future use can be stored conveniently. A block diagram of such a repertory dialer is shown in Fig. 2.

The electronic phone

The major hurdle in the design of all electronic phones—making the electronic speech network function satisfactorily over all conditions—is likely to be overcome in a short time thanks to the recent advance in fabrication of the low voltage operational amplifier. It is within reach of existing technology to fabricate a monolithic LSI circuit that can combine the speech network as well as the pulse or tone dialing function on the same die. Incorporation of low power CMOS microprocessors and low current LCD displays should follow, completing the transformation of the dumb electromechanical instrument, which the century old telephone is, into an intelligent, modern multifeature terminal of the future. □

AMERICAN MICROSYSTEMS, INC.

AA 201

Encoder-decoder chip pair eliminates system crosstalk

by Yusef Haque and Victor Godbole

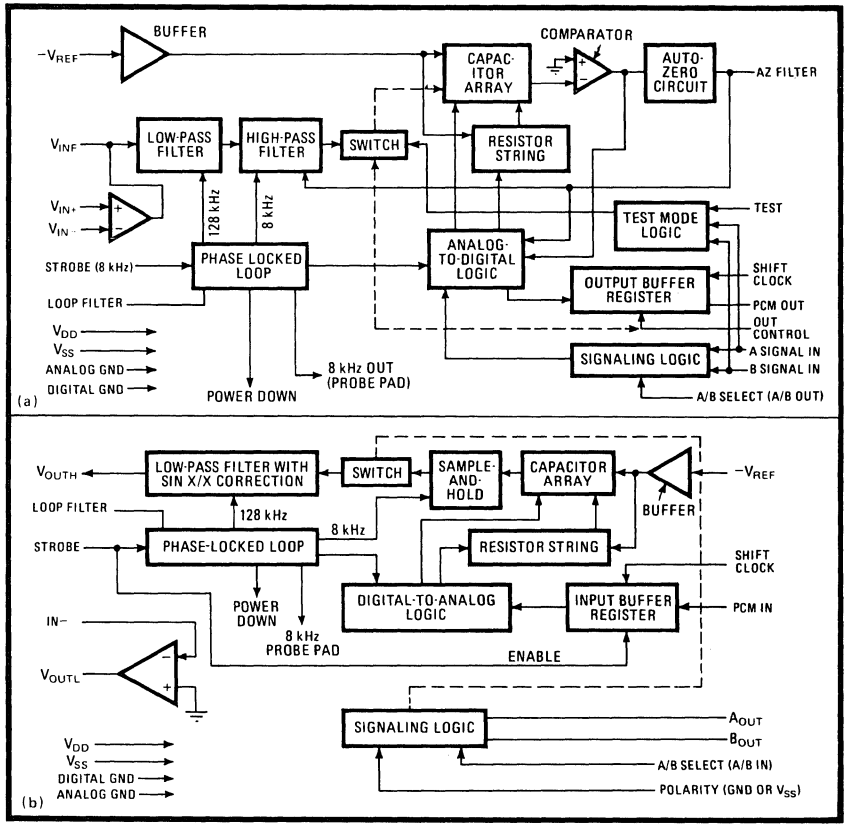
Encoder-decoder chip pair eliminates system crosstalk

C-MOS logic anticipates future telephone signaling schemes; partitioning gives codec more design flexibility

by Yusef Haque and Victor Godbole, *American Microsystems Inc., Santa Clara, Calif.*

☐ Codecs with a variety of architectures are now available for use in communications equipment. In looking for optimal, cost-effective solutions to high-level integration of telephony functions, a number of "best answers" have been claimed. Putting the entire codec on one chip has obvious face-value attraction, but there are strong arguments—notably design flexibility and zero crosstalk—for a two-chip implementation with receiving (decoding) and transmitting (encoding) functions on separate chips.

Like other codecs, the complementary-MOS S3501 encoder and S3502 decoder together form a subsystem for encoding analog signals into a pulse-code modulated (PCM) digital data stream and for decoding received PCM data, returning it to analog form [*Electronics*, May 22, 1980, p. 202]. Each chip carries filtering circuitry for its associated (transmitting or receiving) channel. The two chips can be used in a central telephone office to allow more efficient digital signal-switching to be used (see "A complete central office system," p. 117); they can be used in a telephone to put the signal in digital form before it goes out on the transmission line; and they



1. Partitioned. In the AMI codec pair, both the encoder (a) and the decoder (b) have on-board filters. The chips are packaged separately to eliminate system crosstalk and to allow the user to purchase only what is necessary for a particular application.

A complete central office system

The major elements of a typical line-interface circuit used in a private branch exchange or central office are a two-to-four-wire converter, transmit and receive filters, analog-to-digital and digital-to-analog converters, and circuitry for line supervision and control. The two-to-four-wire converter—generally implemented by a transformer-resistor hybrid—provides an interface between the two-wire subscriber termination and the transmit and receive paths of the time-division-multiplexed pulse-code-modulated data highway. It also supplies the battery feed to the subscriber telephone.

The transmit filter performs the band-limiting function needed for the 8-kHz-sampling system and the a-d converter encodes the band-limited analog signal into 8-bit PCM data words at the 8-kHz sampling rate. Typically, data words from 24 channels are multiplexed to form a PCM transmit highway.

On the incoming signal side, the d-a converter decodes the 8-bit PCM data words from the PCM receive highway into analog samples at the 8-kHz rate. Then the low-pass receive filter smoothes these samples to reconstruct the original analog signal. The line-supervision and control circuitry provides off-hook and disconnect supervision and ringing and rotary-dial pulse decoding, as well as supplying signaling bits to the a-d converter for transmission within the PCM data words.

The S3501 and S3502 provide both the a-d and d-a conversion with its associated filtering. Programmable attenuator blocks in the transmit and receive portion are needed to provide attentuation—typically in increments of 0.1 decibels over the range from 0 to 6.3 dB. This is required to overcome variations in losses in office wiring. The codec filters have zero gain, but further gain adjustments can be implemented at the input of the encoder amplifier stage or at the output of the decoder output-amplifier stage.

can be used in private branch exchanges to bring the benefits of digital switching into the office.

Partitioning the codec function into independent transmitting and receiving sections eliminates any possibility of channel crosstalk due to either sharing of the conversion circuitry or leakage between on-chip components. It also means that the two chips can be operated either synchronously or asynchronously.

When half is enough

In applications that require either analog-to-digital or digital-to-analog conversion but not both, such as digital signal processing or tone receiving, this partitioning lowers costs because only the equivalent of half a codec need be purchased and because certain auxiliary chips that may be needed to make a full codec perform are made unnecessary. Two-chip partitioning also permits the use of 16- or 18-pin packages, which are machine-insertable.

The choice of C-MOS was dictated by the desire to keep power consumption low—always a consideration in central telephone offices where many thousands of codecs are used at once. The C-MOS pair typically dissipates but 125 milliwatts in the active mode.

The choice of C-MOS also means that only two noncritical and non-tracking power supplies (+5 and −5 volts typical) are needed. The third supply (+12 V) needed for some circuits made in n-channel MOS is also eliminated.

For a given supply voltage, C-MOS gives more dynamic range than n-MOS in the codec's linear circuit elements, such as its operational amplifiers. Since these amplifiers use complimentary symmetry in their output structure, typical design voltage swings close to the maximum +5- and −5-V power supply levels are obtained in typical designs, making useful the maximum possible dynamic range of codec input signals.

C-MOS technology has one further advantage. Since a vertical npn transistor is available, the output amplifier in the decoder filter can directly drive the 600-ohm transformer in the subscriber-loop interface circuit connected to the codec. Up to +9 dBm of power is furnished for this task, plenty for all applications.

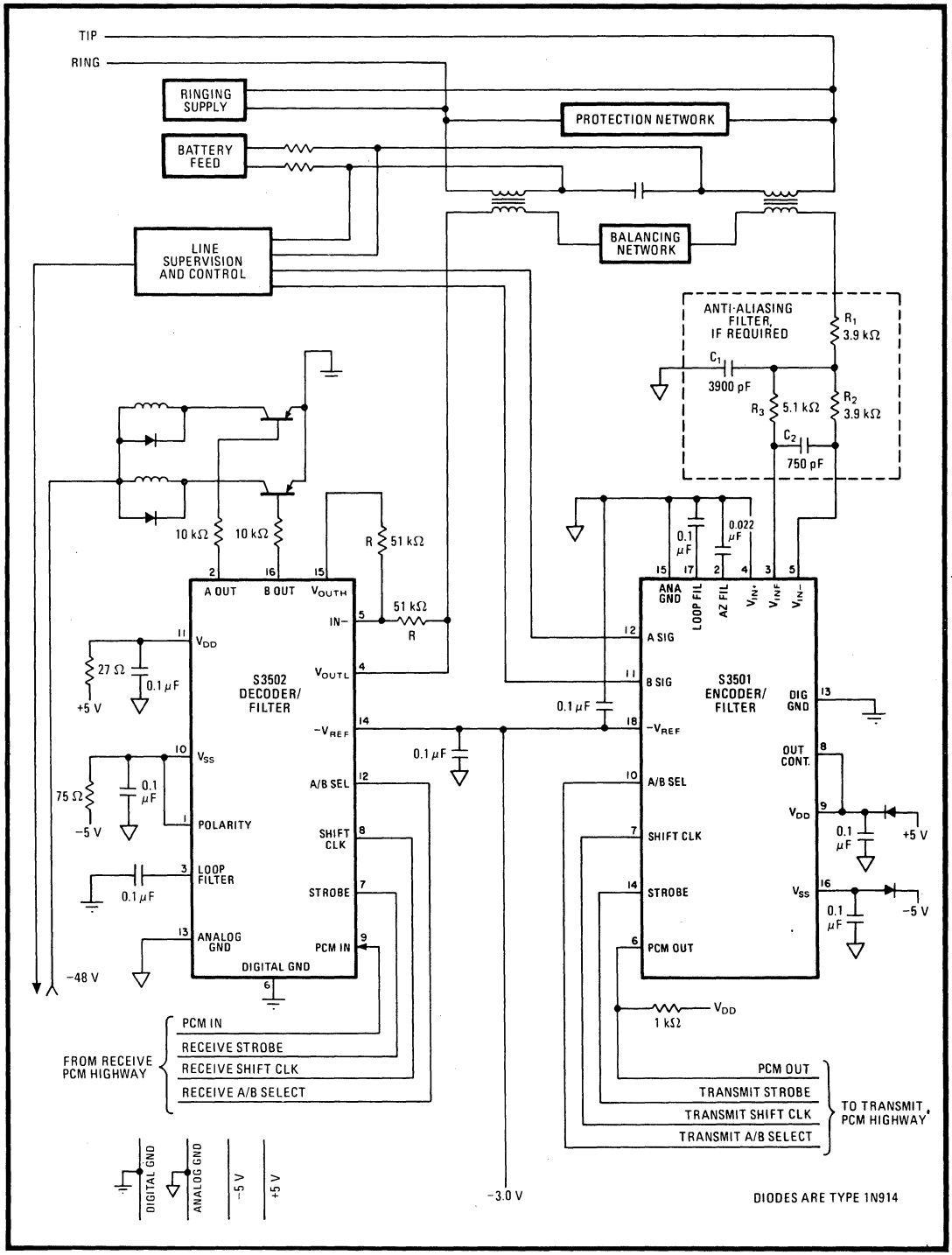
Both the S3501 and S3502 require an externally supplied −3-V reference voltage for the a-d and d-a conversion circuitry. This shortcoming is not as bad as it seems at first glance. Due to the high input impedance presented at the reference input, input current is only 100 nanoamperes, and multiple-chip sets can be supplied by one voltage reference. In fact, all codec sets in a standard 24-channel PCM system can easily share a single reference source. Commercial low-cost bipolar references with the required long-term stability and temperature coefficient (better than 100 parts per million/°C) are readily available and the cost per 24 channels for this shared reference is negligible.

On-board filters

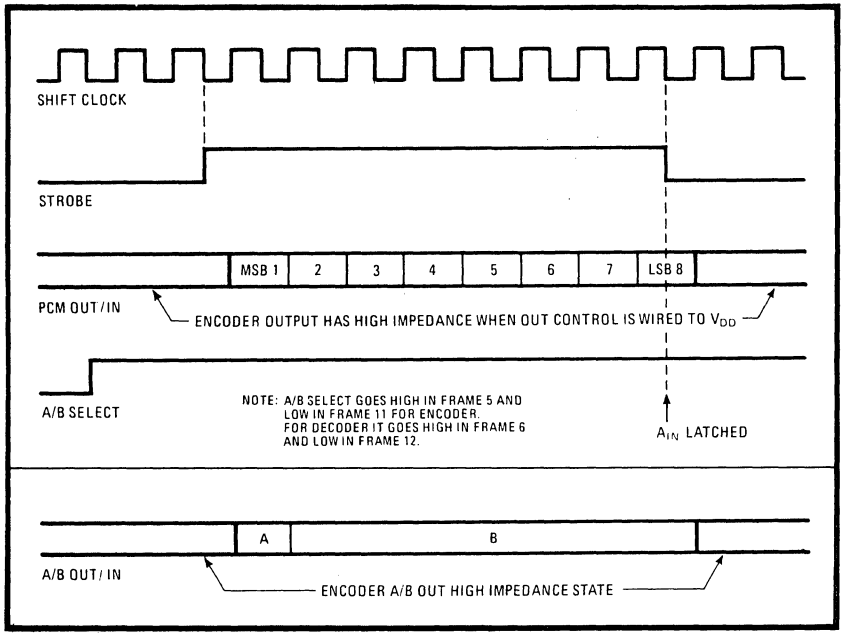
The filters that codecs require for the transmitting and receiving channels have traditionally been implemented by active circuitry using either discrete components or hybrids. These filters require component trimming to achieve their frequency-response characteristic. Recent design advances in monolithic switched-capacitor filters have made possible monolithic realizations of these filter functions with no external components or frequency-response adjustments. Many manufacturers have made monolithic filters available, but few have done so on the same chip as the d-a or a-d converter. AMI and others have integrated the encoder and its filter on one chip and the decoder and its filter on another because the approach has considerable advantages in addition to the reduction of system chip count.

With an integrated filter, a phase-locked loop can be used to generate all timing signals for the filter and conversion circuitry from the system's 8-kilohertz sampling strobe signal. If this is done, the filter clocks and the a-d and d-a conversion clocks have an exact harmonic relationship with the 8-kHz strobe signal. This eliminates the need for a smoothing filter between the transmit filter and the a-d converter.

Furthermore, since such a timing scheme means the sample-and-hold function in the encoder can be elimi-



2. Central office. The S3501 encoder and S3502 decoder are connected in a central telephone office much as are one-chip codecs; antialiasing filter is needed if 128-kHz noise is present. Both present and anticipated A/B signaling formats are taken into account.



3. Waveforms. In a typical pulse-code-modulation multiplexed telephone system, the codec's TTL-compatible strobe input is driven by an 8-kHz signal. When a logic 1 level appears on the strobe line, 8 PCM bits are encoded or decoded at the data highway's shift-clock rate—between limits of 56 kHz and 3.2 MHz for the S3501/S3502.

nated, its contribution to the codec group delay is eliminated, improving an important system specification. It is also important to remember that with this approach the a-d and d-a conversion rate is based on the 8-kHz strobe only and is independent of the PCM data rate. So any arbitrary data rate from 56-kHz to 3.2 megahertz may be used. This increases the codec's range of applications.

The use of a phase-locked loop to derive all timing signals has one more advantage. A simplified power-down scheme can be implemented by simply gating off the 8-kHz strobe signal when the channel is idle. The phase-locked loop then detects the unlocked condition and powers down all the active circuitry. Total power dissipation is reduced to less than 25 milliwatts in this mode of operation.

Other system design improvements have been incorporated in the chip architecture. They can be immediately used in a typical central-office telephony application (Fig. 2). For example, to minimize the noise induced in the codec circuitry by nearby power lines, the low-pass filter in the encoder is followed by a third-order Chebyshev high-pass filter. This filter provides attenuation of at least 25 decibels below 65 hertz. And, for further noise immunity in the codec, its operational amplifiers and comparators have 75- to 85-dB rejection of power-supply noise. Because of the codec's good noise rejection, 0.1-microfarad bypass capacitors are sufficient for power-supply decoupling in most applications. Idle-channel noise of 14 dBrnC or better has been obtained for the full channel using the S3501 and S3502.

There is yet another source of noise that is of concern since the switched-capacitor filters are sampled-data filters. Any extraneous signal or noise components at the input of the transmit filter in the vicinity of the filter sampling frequency (128 kHz) fold back into the filter passband. In most cases these components are negligibly small so that no external filtering at the input is necessary. However, if extraneous signal or noise in the vicinity of 128 kHz is significant, an external two-pole RC filter (formed by R_1, R_2, R_3, C_1, and C_2 in Fig. 2) should be added. This is used in conjunction with the uncommitted on-chip input amplifier to provide sufficient attenuation for these undesired-frequency components. This second-order filter can readily be designed to have negligible impact on the codec passband characteristics. Transmit-channel gain adjustment can also be accomplished by changing the gain of this filter.

A similar antialiasing filter is not necessary at the output of the decoder since the transformer has band-limiting characteristics and the received signal is sent to the subscriber connection of the system.

Simplified timing

The internal design of the codec chip set allows for a simple solution to an ambiguity problem in codec system timing. Unless the codec is timed with the proper edges of the clock signal, the user cannot be sure that the eighth data bit is not shortened or the first data bit is not lengthened. To ensure that this timing is accomplished properly, data is shifted out of the encoder on the positive edges of the shift clock.

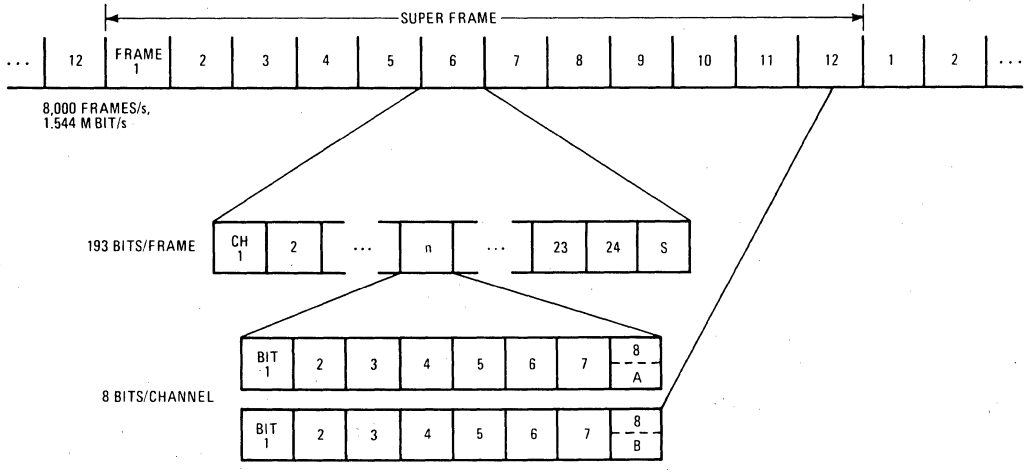
At the same time the 8-kHz sampling strobe is synchronized to the negative edges of the shift clock. In the absence of the strobe signal, the encoder output goes into a high-impedance state, in coincidence with the positive edge of the shift clock. With this timing approach, all 8 data bits on the PCM highway must occupy equal time. This permits the logic to sample data bits (synchronized with the negative edge of the shift clock) at the center of the bit "on" time, avoiding any chance of ambiguity

Sending the signal

In American Telephone & Telegraph Co.'s T1 Carrier PCM format, A/B signaling is used to convey channel signaling information. This information varies with the service requirements and according to whether the application is subscriber, direct, toll-connecting, tandem, or intertoll. It might include the on- or off-hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, or ring ground.

Usually, provision is made to send two signaling conditions—A and B—per channel, giving four possible signaling states per channel repeated every 12 frames. This requires a sampling period of 1.5 milliseconds per signaling condition. The A signaling condition is sent in bit 8 of all 24 channels in frame 6. The B signaling condition is sent in frame 12. In each frame, bit 193 (called the S bit) performs the terminal framing function and serves to identify frames 6 and 12 (see figures).

Use of the bit 8 in the PCM channel word for signaling causes a slight degradation in the signal-to-quantizing-distortion ratio and increases idle-channel noise. The D2, D3, and D4 channel bank formats allow for future use of common-channel interoffice signaling (CCIS), which multiplexes signaling for all 24 voice channels onto a separate signaling highway. The S3501A/S3502A codec set is designed to accommodate a separate A/B signaling highway and facilitate the CCIS scheme.



(Fig. 3). The decoder uses a similar scheme for reception of PCM data.

The S3501 and S3502 are designed to simplify the signaling interfaces (see "Sending the signal," p. 120). For example, the A/B-select input pin is transition-sensitive: it selects the A signal input on a positive transition and the B signal input on a negative transition. A common A/B-select signal can thus be used for all 24 transmit channels in a channel bank instead of two separate select signals.

Encoding signaling data

The A/B-select input is internally synchronized with the strobe input and thus each individual encoder in such a bank is able to derive its own A/B-select input in the proper time slot. The A/B-select input must go high at the beginning of frame 5 and low at the beginning of frame 11. The encoder logic then puts out the A signaling bit at the time slot of bit 8 in frame 6 and the B signaling bit similarly in frame 12.

A similar scheme is used for receiving the A and B signaling bits in the decoder. There is, however, one difference. The A and B signaling bits are latched to the output in the same frame where the A/B-select input makes a transition. With this approach, the A/B-select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

The received A/B signaling bits are usually used to control A and B signaling relays. It is common practice to use 48-V relays that operate from the −48-V supply available in the central office. The decoder's signaling-output logic was designed to facilitate this relay driving with a pnp transistor interface. In this approach the decoder logic latches the received A and B signaling bits and performs a level translation that provides an output voltage swing from −5 to +5 V dc for the signaling-bit change from logic 1 to logic 0.

Thus, with the received signaling bit equal to a logic 1, the signaling output is −5 V dc. This supplies sufficient base drive to the pnp transistor to turn the relay on. At the same time, when the signaling bit is a logic 0, the output voltage changes to +5 V dc. This allows reliable shutdown of the grounded-emitter transistor and turns the relay off. For relay drive capability, the polarity pin on the decoder is connected to the V_{ss}, or power-supply, pin. TTL compatibility at the signaling outputs can be achieved by connecting the polarity pin to digital ground. In this connection there is no inversion of the signaling output level with respect to the received bit polarity. □

V-MOS chip joins microprocessor to handle signals in real time

by Richard W. Blasco

V-MOS chip joins microprocessor to handle signals in real time

By performing millions of operations a second, this device enables a standard microprocessor to rival bit-slice systems

by Richard W. Blasco, *American Microsystems Inc., Santa Clara, Calif.*

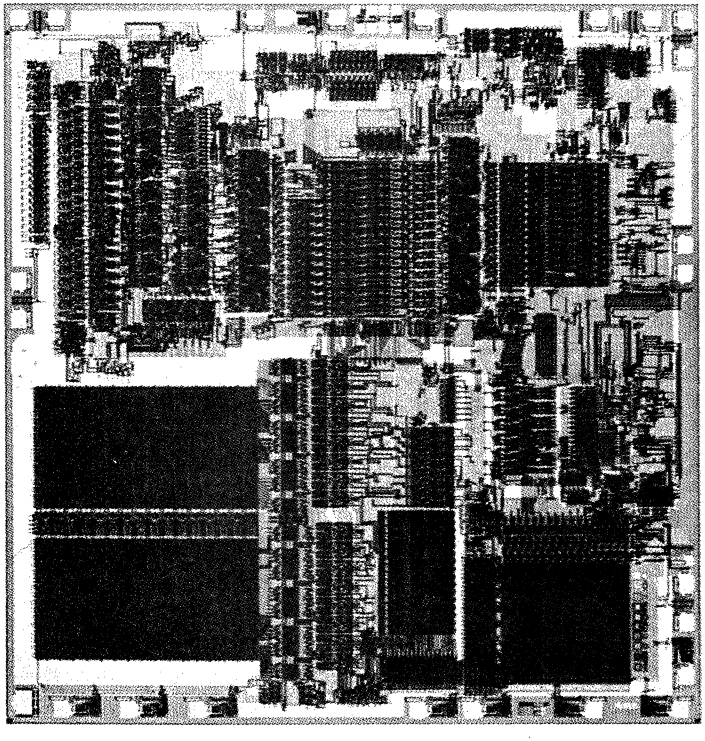
☐ Versatility, easy programming, and low cost make standard microprocessors heavy hitters in many leagues. But they do tend to strike out when it comes to real-time signal processing, with its number-crunching throughputs of several million arithmetic operations each second, its need for external synchronization at minimal software overhead, and so on. However, help is at hand.

A powerful microcomputer

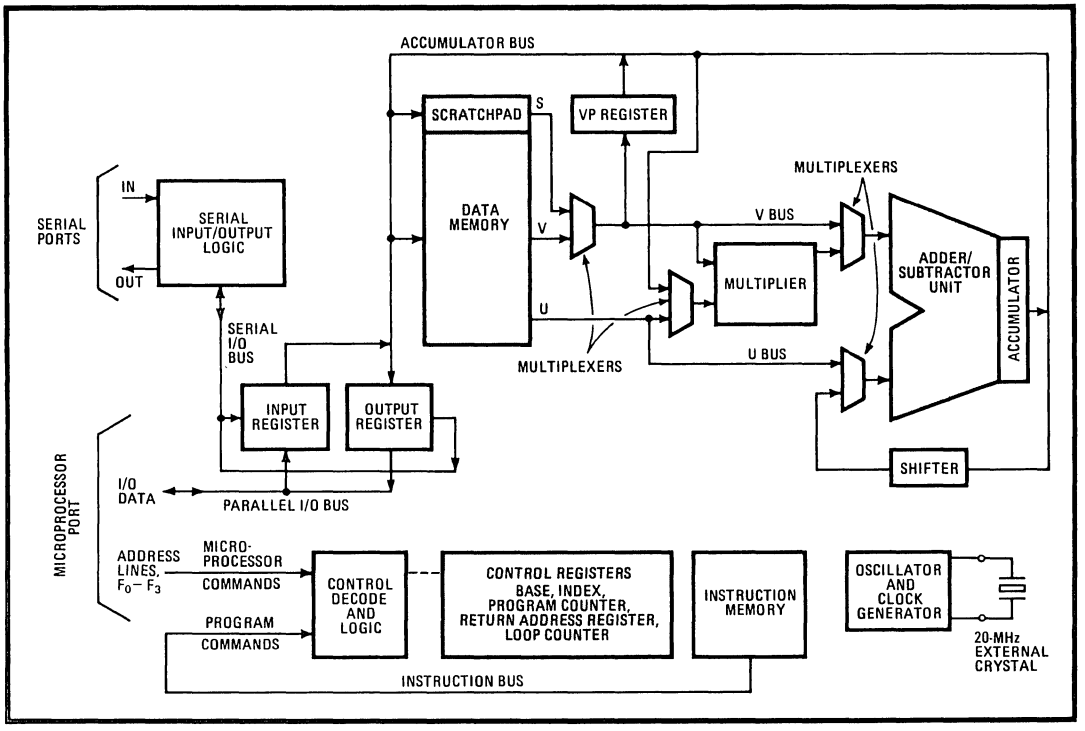
A new large-scale integrated chip gives a microprocessor system the processing clout required to handle real-time signals. Dubbed the S2811 signal-processing peripheral (SPP), this powerful chip gives the system a signal-processing capability rivaling the capability of bipolar bit slices and dedicated multipliers—at considerably lower chip count, cost, and power consumption.

The SPP is actually a powerful microcomputer in its own right, packing 30,500 devices on a die measuring only 198 by 205 mils. This density was achieved with the proprietary V-MOS process, in which vertical devices are fabricated by etching a V groove through an epitaxial layer. Like a microcomputer, the part is programmable for digital processing of signals in voice-grade communications systems and other audio-frequency applications. The architecture is optimized for the processing of audio signals (Fig. 1).

Linking instruction memory, data memory, a hardware multiplier, and an adder/subtractor unit with a parallel multiple-bus structure, the SPP can fetch two operands, multiply them, and accumulate and store the



Signal processor. Actually a 16-bit microcomputer, this peripheral chip uses V-MOS technology to achieve the density necessary for handling voice communications digitally in real time.



1. Built for speed. Architecture of the S2811 signal-processing peripheral device features multiple buses and special-purpose registers to provide processing throughput that is comparable to that of bipolar bit slices; yet the new device is a single chip.

TABLE 1: S2811 SIGNAL-PROCESSING PERIPHERAL CHIP BENCHMARKS

Operation	Number of instructions	Execution time
Biquad filter section	7	2.1 μs
Dual-tone multifrequency decoder	51	54 μs/sample
μ-law/linear conversion	15	6.6 μs
Sine and cosine of angle	19	5.7 μs
Fixed to floating-point conversion	18	15.9 μs
Floating-point to fixed conversion	3	5.1 μs
V.27 (4,800-bit/s) modem	248	497.7 μs/baud
32-point complex fast Fourier transform (expandable)	190	1.5 ms/32 points
Audio-spectrum analyzer	34	21.7 μs/sample

result in a single 300-nanosecond instruction cycle. Its architecture also includes several special-purpose registers to facilitate throughput.

The result is processing capability equivalent to some 35 bipolar bit-slice devices packed into a 28-pin dual in-line package. Clocking is provided by connecting a 20-megahertz series-resonant crystal across two pins. Power dissipation of the device is less than 1 watt from a single 5-volt supply.

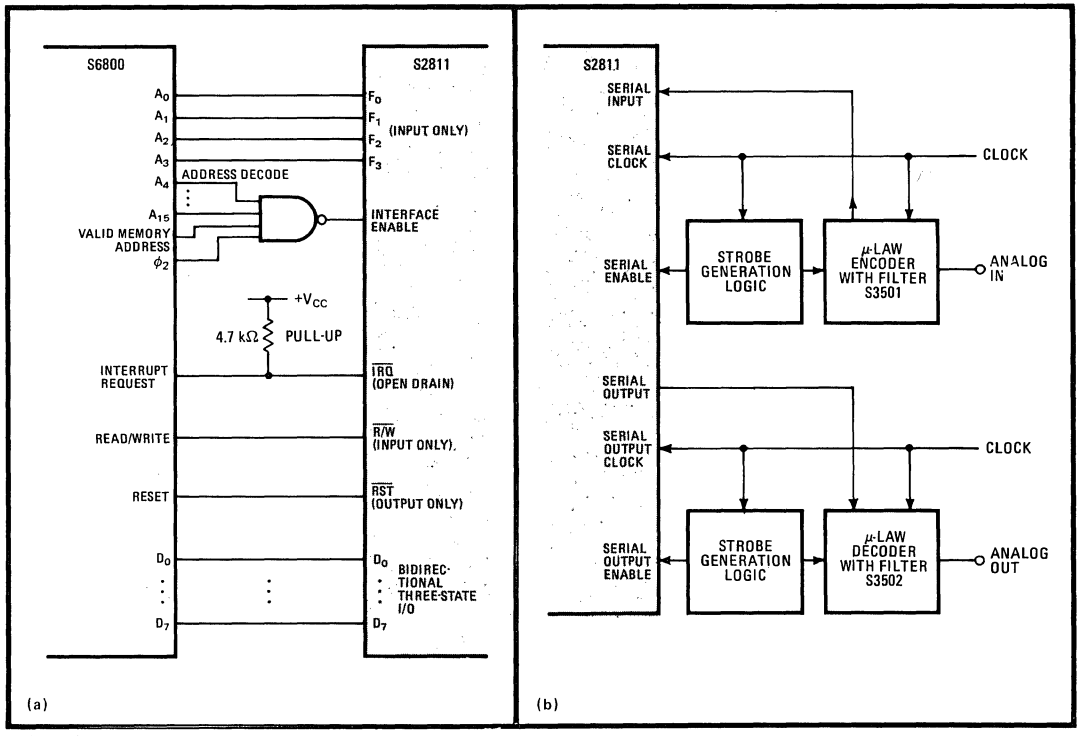
The S2811's processing capability should make it a practical solution in many applications, as the benchmarks in Table 1 suggest. The part was designed for telecommunications applications, but prospective users also have proposed it for radar image processing, speech compression and recognition, process control, and pattern classification. The small size and low power dissipation of SPP-based systems are particularly advantageous in mobile applications. For complex tasks a number of the chips may be linked together in an array; for specialized jobs, several standard, factory-programmed parts will be available.

Control by microprocessor

The SPP teams with a microprocessor to provide a flexible and powerful signal-processing arrangement. It is coded using an internal mask-programmable read-only memory. The coding results in a collection of processing sequences, or "hardware subroutines," called up by the microprocessor to process signals. By providing parametric data during the callup or by changing the sequence of routine calls, the processor can modify program flow.

For example, a universal filter routine may be coded in the SPP, with key filter parameters (order of filter, pole and zero locations, and so on) supplied by the control processor at execution time. So the same mask pattern is usable for several different applications. Similarly, a single mask pattern can provide both forward and inverse Fourier transform operations, depending on the sequence of calls from the control processor.

The SPP may be coded to provide an interrupt upon completion of its task, freeing the control processor to perform other tasks until then. The instruction set is



2. Straightforward. Microprocessor port (a) and serial ports (b) provide straightforward and simple interfacing. The serial input and output ports are independent, and each can interface up to 10 coders/decoders thanks to the time-division-multiplexed format.

powerful enough to permit operation for several hundred microseconds between microprocessor calls. This permits use of any standard processor to control the part.

While capable of operating without a control processor (see "It stands alone for simple jobs," p. 134), the SPP is intended to fit into a microprocessor environment. Its interface was designed to be both simple and flexible, with two input/output ports: one to the microprocessor, and a serial port to the outside world.

Data may be routed via the microprocessor or serial port under software control. The multiple-bus architecture permits a serial input and output, either a parallel input or output, and internal number crunching all to take place simultaneously. All necessary control logic is handled by hardware in the S2811, minimizing software overhead. This sophistication makes the interface as simple and straightforward as possible (Fig. 2).

The microprocessor port, for device control and data I/O, is directly compatible with the 6800 and 9900 bus format. Addition of a few medium-scale integrated devices provides compatibility with any of the popular microprocessors.

The serial port, for signal I/O, is directly compatible with the interfaces of the American Microsystems S3501/S3502 coder/decoder. Low-cost codecs may be used for analog-to-digital and d-a access because the S2811 software can be written to include conversion from companded to noncompressed code and vice versa.

The serial port may be directly connected to a standard telecommunications highway for processing of pulse-code-modulated signals without leaving the digital domain. It will handle word lengths from 1 to 16 bits at a shift rate up to 5 MHz. The part can service as many as 10 transmit and 10 receive PCM channels simultaneously at a 2.048-MHz shift rate. The transmit and receive channels are asynchronous and independent.

Synchronization of data

Input and output flags, along with double buffering of the serial port, permit the SPP to operate in synchronous sampled-data systems with a minimum of software overhead. Signal processing usually involves sampling the input signal at regular intervals and passing these samples to the processor. The sampling must occur at precise intervals, with essentially no phase jitter on the sampling strobe. The signal processor must acquire the samples at precise points in the program execution cycle for proper operation. Some means of synchronization is therefore required.

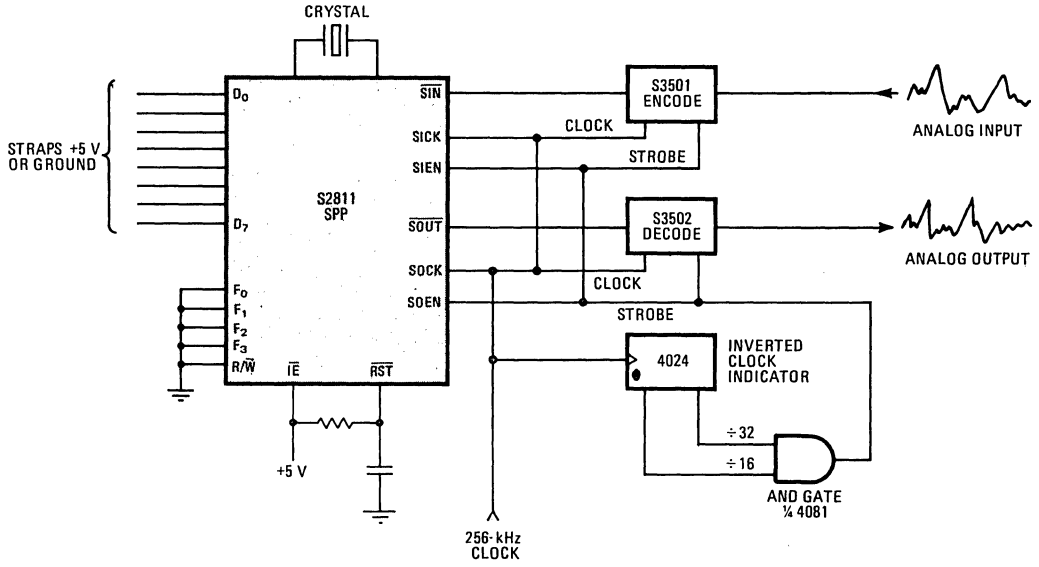
Synchronization can be achieved in two ways. Sampling strobes may be generated by the processor by fixing the program length and providing special sampling instructions. Alternatively, the processor may be synchronized to an external sampling strobe by somehow adjusting the program length to equal the sample period. Both methods are to be found implemented in signal-processing chips.

The first method requires minimal hardware, since no

It stands alone for simple jobs

For simple tasks like Touch-Tone decoding, the S2811 can operate without a control processor, as shown above. The resistor and capacitor on the RST input generate a start pulse to initialize the part and begin execution at location 00. Use of jump tables and the special MODE instruction allows the part to provide its own program control and setup information.

Generating a strobe for the codecs and SPP requires only the 4024 seven-stage ripple counter and a quarter of a 4081 AND gate. The S3501/2 codec chips contain the aliasing filters required by the sampling arrangement. The unused S2811 parallel inputs may be connected to switches to provide program options or with a transistor-transistor-logic patch to provide more outputs.



adjustments for program length are needed. However, strobe accuracy requirements are now imposed on the processor clock. Program jumps and loops are all but excluded, since they would make maintaining a constant program length excessively difficult. The limitations of this approach become unacceptable as the processing algorithm gains complexity.

The S2811 uses the second, more common approach. The fixed program length is slightly less than the sampling interval, and wait loops extend the length to equal the sample period. One or more buffer registers provide elastic storage with samples remaining there for a period equaling the difference between the sampling period and the instantaneous program length. Elastic storage permits synchronization to be maintained despite small variations in program length, so long as the average program length is no longer than the sample period.

Hardware resources

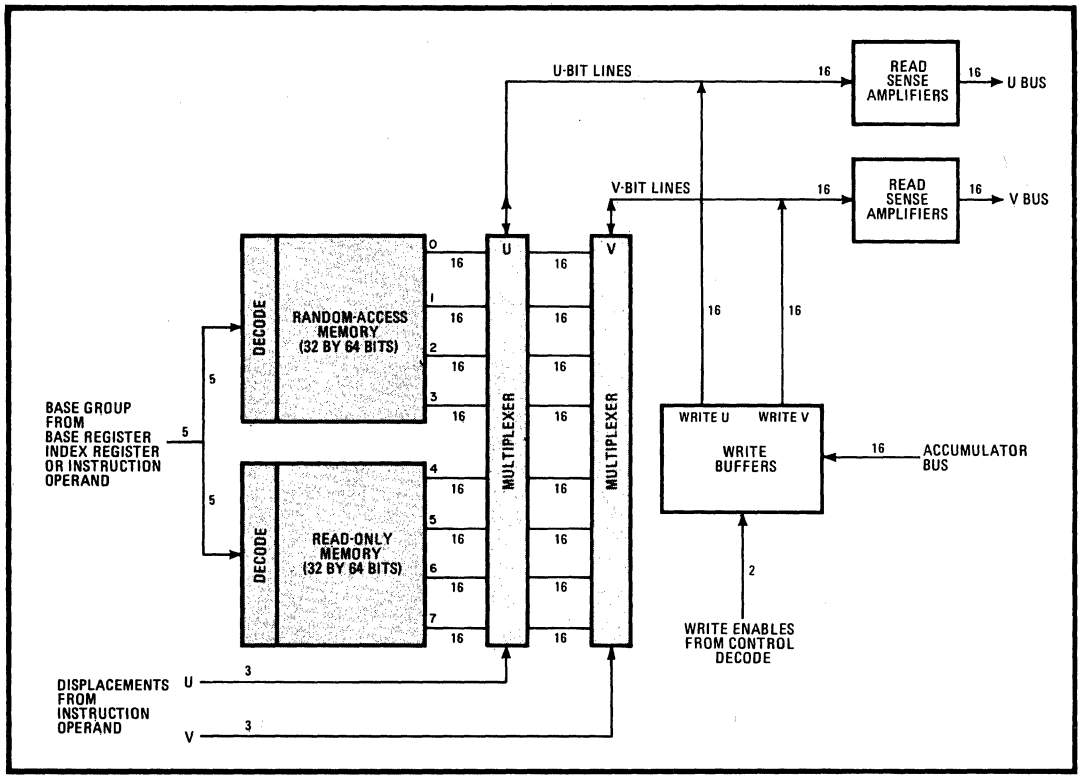
As the signal-processing element in a microprocessor-based system, the SPP is designed to be flexible and easy to use for most audio-signal tasks. The architecture will look familiar to those who assemble signal-processing units from medium- or small-scale integrated circuits; on a single chip are the hardware features of the typical bipolar bit-slice solution.

The user's code is stored in a 256-by-17-bit ROM. Six of the 17-bit instruction words are reserved for production-line testing; the remaining 250 words are available to the user. The limited size of the instruction memory is not as much of a constraint as it might seem, because of the power of the instruction set itself (as later discussion of the set will make clear). Experience suggests that available processing time is exhausted slightly before code space is depleted in most applications.

The data memory stores 256 16-bit data words. The arrangement of Fig. 3 permits simultaneous access of two operands with a single fetch command. The memory is organized as 32 "base" groups of eight "displacement" words each. All eight displacement words are accessed in parallel, over lines 0–7, and the two displacement multiplexers select two of the words for processing. For convenience of reference, one multiplexer and the associated lines are identified as the U circuit, the other multiplexer and lines as the V circuit.

To conserve die area, the data memory is split between a random-access memory and a ROM. In most applications this partitioning is ideal, since coefficients, lookup tables, and other fixed data conveniently reside in the four ROM displacements—and there is no need to load coefficients into the SPP upon power-up. Those applications requiring additional RAM may utilize the block-transfer mode to expand the apparent memory size.

An eight-word scratchpad can replace the V output.



3. Two for the price of one. The base-displacement organization of the 256-word data memory coupled with the output multiplexers, provides two memory words with a single fetch. One word comes on the U-bit lines, and the other on the V-bit lines.

All in RAM, the scratchpad data is available independently of the base-group selection (each base consists of four words in RAM and four in ROM). It stores the constants and parameters common to several groups of data and also is handy for temporary storage of intermediate results.

A fully parallel modified Booth algorithm multiplier forms the product of two 12-bit inputs and rounds off the result to 16 bits. The round-off scheme used is accurate to 15¾ bits and has zero mean error.

Multiply time is 300 ns and overlaps the 300-ns instruction cycle so that the product of two operands fetched during instruction N is available during instruction N+1. This pipelining maximizes throughput and is fairly easy to handle when programming the SPP.

The adder/subtractor unit (ASU) calculates the sum or difference of two 16-bit members. Circuitry is provided to detect zero, negative, and overflow outputs, with special jump instructions providing program branching on these conditions. Overflow protect circuitry provides the saturation arithmetic already discussed. A 1-bit arithmetic shifter scales numbers in the ASU by a factor of two.

Digital filtering algorithms require implementation of a delay of one sample period (Z^{-1}). The VP register makes the V operand accessed during instruction N available during instruction N+1 for storage. This simplifies filtering routines (see "Filters are easy," p. 136) by eliminating the overhead otherwise required to implement the Z^{-1} delays.

Control logic interprets the commands from the the control microprocessor or from the internal instruction memory and sets up data paths in the SPP. (Several macroinstructions are provided to minimize code for commonly used routines.) Programmable logic arrays implement all decoding, making it relatively easy to modify the basic instruction set.

Several counters and registers assist in controlling the SPP. These are:

- The base register, which is a 5-bit presettable up/down counter providing base-group address information to the data memory.
- The index register, an 8-bit presettable up counter providing addressing during the block-transfer mode and serving as an alternative base register (using only 5 bits) for table-lookup and dual-base addressing operations.
- The program counter, an 8-bit presettable up counter providing the instruction memory address. Extensive jump instructions allow program branches and loops.
- The return address register, an 8-bit register storing the program return address when a subroutine is called. One level of subroutine nesting is available.
- The loop counter, a presettable 5-bit down counter controlling iteration loops. Several jump instructions are

Filters are easy

The S2811 architecture is optimized for implementation of digital filters. Consequently, implementation of filters is both straightforward and efficient. For example, the finite impulse response transversal filter is implemented with the following equation:

$$Y_n = \sum_{i=0}^{N} W_i X_{(n-1)}$$

where

$Y_{(n)}$ = the output
$X_{(n)}$ = the input
N = the number of stages
i = the stage number
W_i = the weight associated with stage i
$X_{(n-1)}$ = the present input sample delayed by i samples.

Data samples are shifted following each $Y_{(n)}$ calculation. The following six-instruction routine implements this filter, including setup of required control registers. The new sample $X_{(n)}$ is placed into location 00.0.

Use of the REPT command provides high efficiency, since each additional tap requires only 300 nanoseconds to process. The power of the S2811 instruction set is illustrated in line 54, where an accumulation, VP-register-to-RAM transfer, base-register increment, multiplier setup, loop-counter decrement, and loop-counter test are all implemented in a single 300-ns macroinstruction, including all necessary overhead.

Adaptive transversal filters are implemented using similar routines, with coefficients stored in random-access memory. Tap update routines modify the coefficients to make the filter adaptive.

LINE	OP1	OP2	OPERAND	COMMENTS
50	NOP	CLAC	–	Clears accumulator
51	–	LLTI	L(09F)	Loads base, loop counter set up to input register
52	AVZ	LIBL	D(00.4)	Sets base = 1, loop ctr = 31, loads W0 in accumulator, and starts multiply of W0 x (ASU) = 0
53	APZ	REPT	D(00.0)	Sets up first multiply, loads zero product into accumulator (next line to be repeated 31 times)
54	APA	TVIB	UV(4,0)	Accumulates product from previous tap, starts multiply for new tap, and shifts data using VP register, incrementing base register
55	APA	TACV	D(0E.2)	Accumulates last term and stores Y sample in address 0E.2

TABLE 2: S2811 SIGNAL-PROCESSING PERIPHERAL CHIP'S OP1 (ASU) INSTRUCTIONS

Type	Mnemonic	Operation
No operation	NOP	No operation
Accumulator operations	ABS	Absolute value
	NEG	Negate ASU contents
	SHR	Arithmetic shift right
	SGV	Negate ASU contents if different polarity from RAM-V contents
Addition operations	AUZ	Load RAM-U contents in ASU
	AVZ	Load RAM-V contents in ASU
	AVA	Add RAM-V and ASU contents
	AUV	Add RAM-U and RAM-V contents
Subtraction operations	SVA	Subtract ASU from RAM-V contents
	SVU	Subtract RAM-U from RAM-V contents
Multiply/add operations	APZ	Load product in ASU
	APA	Add product to ASU contents
	APU	Add product and RAM-U contents
Multiply/subtract operations	SPA	Subtract ASU contents from product
	SPU	Subtract RAM-U contents from product

conditioned on this counter, which is automatically decremented each time it is tested. Gating logic is provided to prevent underflow when the loop counter counts down to zero.

Control codes

The microprocessor controls the SPP over the four address lines designated F_0–F_3 in Fig. 2. When the interface-enable ($\overline{IE}$) line is brought low, the command is transmitted over these lines to set a latch in the chip. The user maps his processing codes into 16 contiguous addresses of the microprocessor's memory space by assigning the F lines to the four least significant address lines. Then reading or writing to the appropriate memory address will activate the desired SPP command.

The DUH/DLH commands (data–upper half byte and data–lower half byte) will transfer 16-bit data into or out of the SPP. Since DUH terminates a word transfer, the most significant bits are always transferred last. Using the DUH command alone is enough to transfer 8-bit data at full efficiency.

The basic routine call from the microprocessor is XEQ: start execution at location D_0–D_7. Execution will start at the SPP code location corresponding to the D_0–D_7 data inputs. In addition, either hardware or software reset will start execution at location 00, providing boot-strap start-up when a control processor is not used.

The remaining control codes set latches to provide special modes of operation. These special modes are set

up by first clearing the control latches using the CLR command and then calling out the desired modes with the appropriate commands.

In addition, these control latches can be set with a special operating instruction (MODE) to provide its own control commands. At the time he is developing his program, the user is free to specify which of the control commands are to be fixed in the code and which of them will be selected by the control processor later on, at the execution time.

Control options for flexibility

The remaining eight commands in the control code provide I/O format and source options to maximize flexibility. The S2811 usually operates with all data transferred via the parallel microprocessor port, one byte at a time. The SRI and SRO commands (enable serial input or output) will route data samples via the serial input and output ports, respectively. With the serial port selected, data may be presented in sign-magnitude form rather than the normal 2's complement format. The SMI and SMO commands (sign-magnitude serial input or output) enable the appropriate conversion logic.

Blocks of data may be moved using the BLK mode. Repeated DLH/DUH access commands will transfer data words while automatically incrementing the index register to access the next word. With an appropriate direct-memory-access controller, data may be transferred into and out of the SPP at a 4-megabyte-per-second rate. Thus the block-transfer capability permits virtual techniques to expand the apparent memory size of the chip.

An external ROM mode (XRM) permits control of the SPP from an external code source. It was included primarily for testing of the part, allowing a standard test pattern to exercise the chip independently of the user's code. With 10 MSI packages, however, users may run the chip from an external programmable ROM, but it operates at half speed (600-ns cycle) in this mode.

The external ROM mode may be used for program development or to provide patches or additions to existing code. The limitations of this mode militate against its use for general program development, where tight timing constraints probably will exist.

The SOP and COP commands determine whether saturation arithmetic (SOP) or overflow arithmetic (COP) is performed in the adder/subtractor unit. With overflow protection enabled, the ASU output will saturate to the maximum positive or negative value, corresponding to the direction of the overflow.

Expandable options

The block-transfer capabilities, microprocessor control, and dual I/O ports provide SPP-based systems with degrees of expandability. Using the block-transfer mode, a single chip may be used to process several sets of data on a time-sharing basis. Under direction of the microprocessor, higher throughput may be achieved by dividing the processing tasks among several parts.

Using the serial ports, two SPPs can pass data directly to each other. Array processor architectures are easily implemented in this manner. The time-division-multiplexed format of the serial ports permits selective inter-

TABLE 3: S2811 SIGNAL-PROCESSING PERIPHERAL CHIP'S OP2 (TRANSFER/CONTROL) INSTRUCTIONS

Type	Mnemonic	Operation
No operation	NOOP	No operation
Load instructions	LLTI	Load literal in input register
	LIBL	Load input register contents into base and loop counters
	LACO	Load ASU contents in output register (sets interrupt request)
	LAXV	Load ASU contents in index register and RAM-V
	LALV	Load ASU contents in loop counter and RAM-V
	LABV	Load ASU contents in base register and RAM-V
Data transfer instructions	TACU	Transfer ASU contents to RAM-U
	TACV	Transfer ASU contents to RAM-V
	TIRV	Transfer input register contents to RAM-V
	TVPV	Transfer VP register contents to RAM-V
	TAUI	Transfer ASU contents to RAM-U using index contents as base
Adder/subtractor unit operations	CLAC	Clear ASU and overflow, SWAP latches
Register manipulation instructions	INIX	Increment index register
	INCB	Increment base register
	DECB	Decrement base register
	SWAP	Interchange roles of base, index registers
Unconditional jump instructions	JMUD	Jump unconditionally direct
	JMUI	Jump unconditionally indirect (index points to jump table)
Conditional jump instructions	JMCD	Jump direct, conditioned on loop counter (jumps if LC $\neq$ 0, LC auto-decrements)
	JMPZ	Jump direct if ASU contents = 0
	JMPN	Jump direct if ASU contents are negative
	JMPO	Jump direct if ASU overflow latch is set (resets overflow latch)
	JMIF	Jump direct if input flag is low (input register empty)
	JMOF	Jump direct if output flag is high (output register full)
Subroutine instructions	JMSR	Jump to subroutine
	RETN	Return to main program
Macro-instructions	JCDT	Jump conditionally dual-tracking (increments base and index registers)
	JCDI	Jump conditionally direct and increment base register
	TVIB	Transfer VP contents to RAM-V and increment base register
	REPT	Repeat next instruction until LC = 0 (LC decrements with each iteration)
	MODE	Force OP1 to NOP and use OP1 bits to provide control code (Table 1)

TABLE 4: S2811 SIGNAL-PROCESSING PERIPHERAL CHIP'S ADDRESS MODES/MULTIPLIER SETUP

Mode	Description	Multiplier inputs
UV	Offset addressing using base and two displacements provided in operand; data located in RAM-U and RAM-V	RAM-U X RAM-V
US	Offset addressing; data located in RAM-U and scratchpad	RAM-U X scratchpad
DA	Direct addressing using address provided in operand; data is RAM-V only	ASU X RAM-V
LT	Literal; data located in operand	None – previous inputs are held
DT	Direct transfer; jump address provided in operand	None – previous inputs are held

connection of the array elements by generating input and output strobes during the appropriate time slots.

To harness the processing power of this architecture, a potent instruction set comes with it. The 17-bit instruction word, partitioned into two op codes and an operand, are stored in the SPP's ROM. They are the vehicle by which the user customizes the chip's functions for his application. In general, this code is independent of the control microprocessor's program. The two are linked via the F lines.

Instruction set details

The 4-bit OP_1 code controls the ASU, while the 5-bit OP_2 commands set up data transfer and program flow. The 8-bit operand provides literal data or address information (3 bits each for displacement selection as shown bottom left of Fig. 3).

The 16 OP_1 instructions (Table 2) and 32 OP_2 instructions (Table 3) provide 388 valid instruction combinations. Benchmarks indicate that this arrangement permits the user to command an average of 3.3 operations per line of code executed.

The large number of instruction possibilities, coupled with the branching and looping capabilities of the SPP, maximize program efficiency. Also, subroutines allow code to be used several times in a program. This ability allows the chip to operate with minimal direction from the control microprocessor and makes the maximum 250 lines of code more than adequate for the majority of applications.

The last 2 bits of the operand identify the addressing mode. Data may be directly addressed, offset addressed, or indirectly addressed. Direct addressing allows access of data in displacements 2, 4, or 6 of Fig. 3, independent of the base register and the index registers. It allows access of only a single word at a time.

Offset addressing makes use of either the base or the index register to point to the base group, while the U and V displacements are specified by the operand. It permits the simultaneous access of two words, one of which may be a scratchpad word.

An offset variant

Dual-base addressing is a variation of offset addressing in which the base and index registers alternately supply the base-group information, under the direction of the swap command. JCDT (jump conditionally, dual tracking) increments the base and index together, providing a tracking arrangement. This address mode is useful in computing kernel functions in which data becomes separated in memory by a fixed offset, as in the fast Fourier transform. It allows the base and index registers to be set up to accommodate this offset with negligible loss of program efficiency.

Indirect addressing allows use of lookup and jump tables stored in the data memory. The index register points to the base group whose contents may be loaded into the ASU for table lookup or into the program counter for jump-table implememtation.

Specifying an address automatically sets up the SPP multiplier, as detailed in Table 4. The last two modes in the table serve to inhibit the update of the multiplier inputs, causing a product to be held while executing jump or literal instructions.

The multiplier runs constantly. Access to a product takes only specification of the proper OP_1 code to load it into the accumulator. Products not used are simply overwritten by new products.

Programming support

The assembly-language format has been defined to make SPP code readable, and users may submit their programs in this format to the manufacturer. A low-cost in-circuit emulator that is designed to run at a reduced speed will be available soon, and a software simulator and a real-time in-circuit emulator will be available somewhat later on a limited basis.

Moreover, several SPP-based standard products, programmed for specific tasks, will be introduced. The first such product is the S2814 fast Fourier transformer. Users of these parts need only be concerned with proper interface to the SPP.

A bright future

Technology in the area of signal processing is developing rapidly, and the SPP approach is not the only possible approach. Other chips will be coming for microprocessor-based systems. Also, further development of bipolar bit slices, switched-capacitor analog technology, and even analog microprocessors will provide many options for signal-processing systems.

Products like the SPP make the message clear: signal-processing technology is in the midst of a revolution. Techniques previously thought impractical are easily implemented with newly available integrated components. Whichever technologies emerge, the outcome will be easier, more flexible, faster signal processing. □

AMERICAN MICROSYSTEMS, INC.

AA 402

Programmable signal-processor LSI rivals analog-circuit filters

by Dr. Gwyn P. Edwards

Programmable signal-processor LSI rivals analog-circuit filters

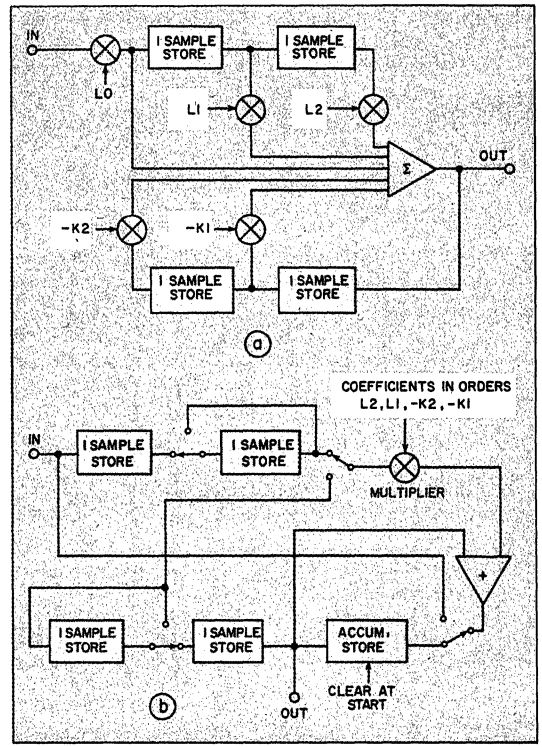
With special-purpose hardware now available, digital filtering can carry out functions previously realizable only by analog techniques. Switching from analog to digital filters reaps several technical advantages, including flexibility—almost any analog-filter characteristic can be programmed—and high stability and reliability at increasingly competitive costs.

Digital filters can be implemented with a general-purpose microprocessor system, with a bit-slice assembly or with a specialized programmable signal-processing LSI chip (such as the AMI S2811; see "Signal-Processor Architecture").

At low speeds—to a few hundred kHz for seismological, medical and biological data—the general-purpose microprocessor can be very effective. Low-order filters, in particular, can be realized quite readily with a single-chip, general-purpose microprocessor, such as AMI's S6801. However, a bank of complex filters would need the more powerful capabilities of a faster 16-bit machine (such as AMI's S9900), together with several associated memory and peripheral-control chips.

At intermediate sampling speeds—to about 100 kHz—the AMI S2811 signal-processing peripheral (SPP) is available for customer programming, and will soon be available preprogrammed for a wide variety of standard filter configurations. Dedicated custom-designed LSIs also are possible, but they are restricted to high-volume production or where high single-unit costs can be tolerated. Several companies (including AMI) offer cell, or universal-logic-array (ULA) type, custom-design facilities for producing such LSIs, as an intermediate stage to a full custom design.

For high sampling frequencies—above about 100 kHz—special-purpose LSI chips, at present, are not fast enough: Systems assembled with fast ICs, MSIs and discrete components become necessary. Before the introduction of the new special-purpose signal-processing chips, like the AMI S2811, this approach was the only way available, even at low speeds. Microprocessor systems made up with n-bit-slice chips are particularly suitable for high-speed processing. They provide a great boost to the capabilities of TTL circuits, while reducing the parts count. The n-bit-slice circuits can be microprogrammed to execute digital-filter algorithms efficiently. However, to achieve the maximum speed capability of the n-bit slice, ECL would be required.



1. Digitally implementing a filter involves multiplying data by constant coefficients (L_0, L_1, L_2, K_1, etc.), storing the data samples and summing the results. All the operations can be done in parallel (a) or, to save hardware, the complex multiplier can be multiplexed (b) and the operation performed serially.

Once the general technology is selected, the configuration of the processor's arithmetic unit is the next item that most affects throughput speed: At high speed, parallel arithmetic becomes almost mandatory; at low speeds serial arithmetic is simpler, and hardware can be saved by multiplexing the processor.

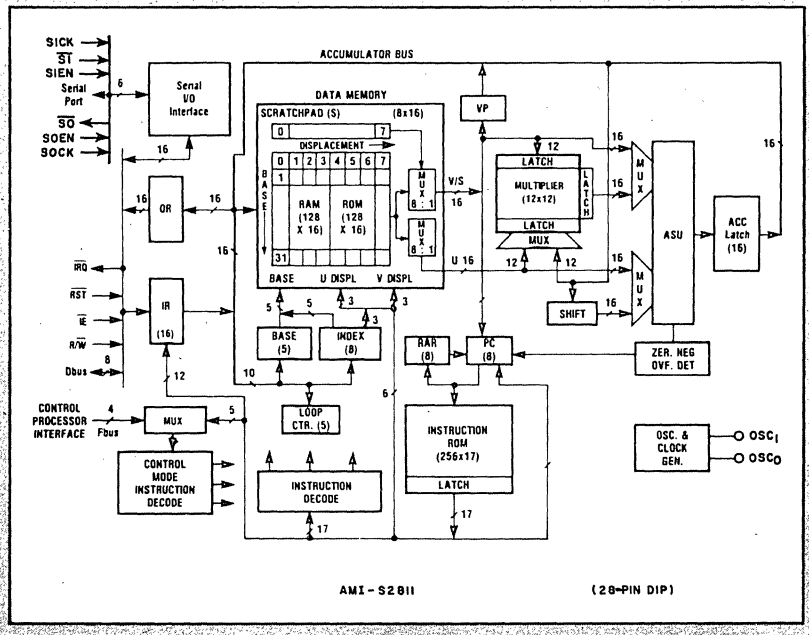
No matter what hardware and architecture are

Dr. Gwyn P. Edwards, Telecommunications Applications Engineer, American Microsystems, Inc., 3800 Homestead Rd., Santa Clara, CA 95051.

employed, multiplication is the most complex function in implementing digital filters. Therefore, multiplexing a single multiplier to perform all multiplications could save substantial hardware.

As Fig. 1a shows, four multiplications are needed to implement a second-order filter section. However, not only can the simplified multiplexing arrangement of Fig. 1b perform all multiplications with one multiplier, but the adder now can be easily implemented in the serial system as a single-input, clearable accumulator, using a two-input adder for addition, storage and feedback. As a result, the whole arithmetic unit—multiplier and accumulator—is multiplexed (Fig. 2), with data and coefficients stored in memories and sequentially supplied in proper order to the unit. Even with such a low level of multiplexing,

Signal-processor architecture



This special-purpose arithmetic processor—with on-chip ROM, RAM, multiplier, adder/subtractor, accumulator and I/O—is organized in a pipeline structure. The multiplier can multiply, add and store two 12-bit numbers in about 300 ns.

Pinout nomenclature

Microprocessor interface (16 pins)

D_0-D_7 — (*Input/Output*) Bidirectional 8-bit data bus.

F_0-F_3 — (*Input*) Control-mode/operation decode.

$\overline{IE}$ — (*Input*) Interface Enable.

R/$\overline{W}$ — (*Input*) Read/Write select. When high, SPP output data are available on the data bus.

$\overline{IRQ}$ — (*Output*) Interrupt Request. An open-drain output that goes low when SPP needs service.

$\overline{RST}$ — (*Input*) Reset. When low, it clears all internal registers, counters and modes, and initiates program execution at location 00.

Serial interface (6 pins)

SICK, SOCK — (*Input*) Serial Clocks. Shifts data into or out of the serial port.

$\overline{SI}$ — (*Input*) Serial Input. Data enter MSB first and are inverted.

SIEN — (*Input*) Serial Input Enable. Length of input word (16 bits maximum) determined by enable width.

SO — (*Output*) Serial Output. Three-state; output MSB first and inverted.

SOEN — (*Input*) Serial Output Enable. Length of output (16 bits maximum) determined by enable width.

Miscellaneous

OSC_I, OSC_O — External 20-MHz crystal (with suitable capacitors to ground) across these pins provide the time base. Or, an external clock can be applied to the OSC_I input.

V_{CC}, V_{SS} — V_{CC} = +5 V, V_{SS} = 0 V (ground).

flexible, complicated universal filter sections can be readily realized.

Many multiplying techniques are possible, with methods classed as all-parallel, all-serial and serial-parallel.

Serial/binary multiplication is simplest

Serial, binary multiplication requires the least amount of hardware (Fig. 3a). But it is also the slowest way to go, and generally cannot be used for digital-filter implementation, especially in high-speed, real-time applications. A complete operation takes M(M+N+1) clock cycles, where M and N are the number of bits in the multiplied numbers.

Parallel-serial techniques (Fig. 3b), often called "pipelining," are substantially faster, since they require just (M+N) clock cycles—far fewer than the all-serial method. But more hardware is needed.

The fastest method is parallel addressing a look-up table. All 2^{M+N} possible products of an M × N-bit multiplication are stored in a fast ROM. Addressing the memory with the M and N bits in parallel gives the product in one quick step. But a 16 × 16-bit multiplication would require a huge memory capacity of over 4-billion 32-bit words.

The solution? Break each word into four 4-bit nibbles, and a more reasonably sized 4 × 4 ROM with 256 address locations can be used sequentially. The partial products, after being properly shifted to preserve significance, can be summed to get the final product. Although this multiplexing saves hardware, speed is sacrificed. Four-separate look-up tables operating in parallel with the partial products summed simultaneously, of course, would produce a quicker result.

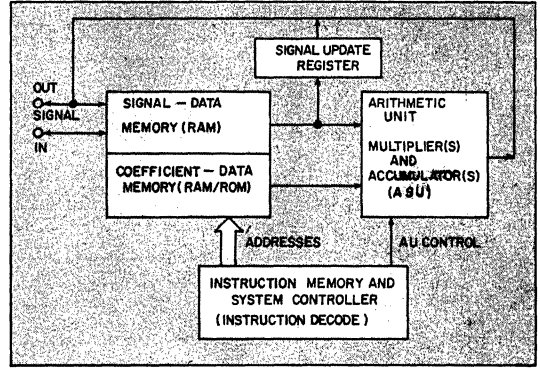
On the other hand, a direct shift-and-add process such as Booth's algorithm can do the multiplication. Like the look-up-table system, a Booth's-algorithm multiplier can be simplified by splitting the input data into nibbles and then summing the partial products. The AMI S2811 employs Booth's technique by working with three bits at a time (Fig. 4).

The algorithm operates on binary numbers in the two's-complement fractional form, where the most-significant bit in front of the decimal represents the sign of the number (see "Booth's Multiplication"). In the algorithm, a number, Y, with m+1 bits can be represented as the sum of two (or more) adjacent bits at a time:

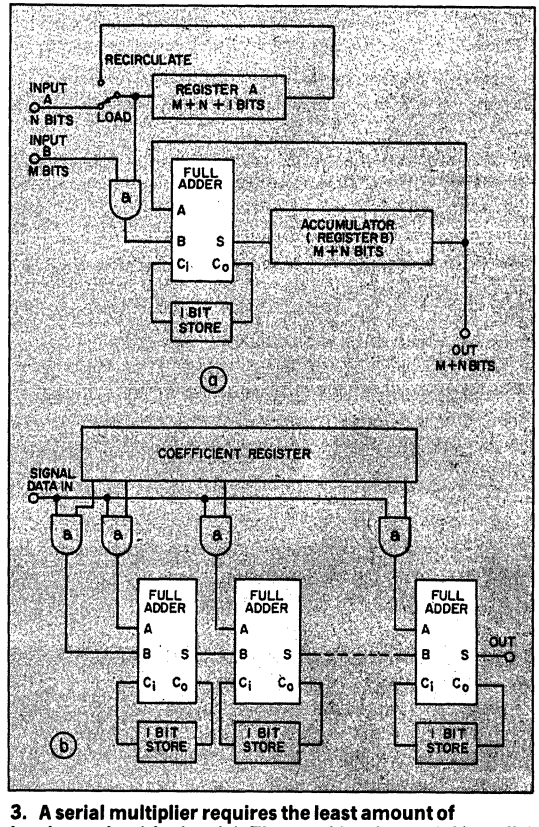
$$Y = \sum_{i=0}^{m} 2^{-m+i} (y^{i-1} - y^{i}),$$

where $(y^{i-1} - y^{i})$ represents the adjacent-bit pairs.

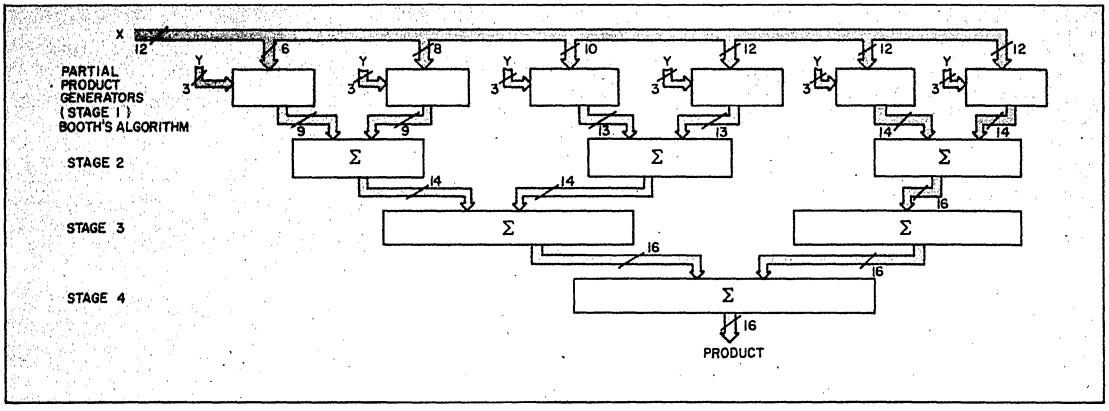
Each pair can assume four different binary configurations, or values (F_i). Starting with the least-significant pair, and multiplying each value of F_i by a number, X, produces four partial products, P_i. Then, by shifting Y one bit at a time, successive Y bit-pairs can be similarly multiplied by X. The total product



2. The multiplier and accumulator can be multiplexed and RAMs used to store (and thus provide delays) for the data, as in this generalized block diagram of a signal processor. ROMs and RAMs provide storage for coefficients and instructions.



3. A serial multiplier requires the least amount of hardware, but it's slow (a). The combination serial/parallel approach, called pipelining (b), is much faster.



4. Employing Booth's algorithm to perform the multiplication, the S2811 operates with three bits at a time and sums the partial products.

is obtained when all the partial products are summed:

$$XY = \sum_{i=0}^{m} 2^{-m+i} P_i.$$

Booth's algorithm is not limited to working with bit pairs. (Using pairs merely helps simplify the explanation of the algorithm.) Operating with three successive bits and then shifting twice per 3-bit group, as is done in the SPP, doubles the speed. In this way, the SPP multiplies two 12-bit two's-complement numbers in just 300 ns to get a 24-bit output. The numbers are separated into six substrings of 3 bits each, and each string executes Booth's algorithm individually. The partial products generated by the algorithm are then summed into a final 24-bit product.

Because the SPP operates primarily with 16-bit numbers (except at the multiplier input), the 24-bit product is not actually produced, but a minimum-logic circuit provides an accurately rounded-off 16-bit output.

Because the 16-bit words represent fixed-point, two's-complement fractional numbers in the SPP, the numbers require proper scaling to realize full accuracy. However, this procedure has the advantage that the multiplier cannot overflow.

On the other hand, the adder/subtractor can overflow. Arithmetic overflow causes highly undesirable behavior, especially when implementing recursive filters: The nonlinear overflow characteristics can cause oscillations because of the overflow's cyclic properties. To prevent such problems, the S2811 provides programmable overflow protection in its adder/subtractor unit. When an overflow is detected, the circuit substitutes a "saturation" value for the actual value, thus preventing oscillations.

Word length determines the maximum point of overflow and thereby establishes not only a digital filter's dynamic range but also its signal-to-noise ratio. However, as a practical matter, the word length is usually fixed by the microprocessor that implements the filter. The 16-bit word used in the S2811 has been found to be adequate for most ordinary purposes.■■

Booth's algorithm for multiplication

For multiplying an (m+1) bit word, Y, by X,

$$X \cdot Y = X\left[-(y^m) + \frac{y^{m-1}}{2} + \frac{y^{m-2}}{4} + \frac{y^{m-3}}{8} + \ldots \frac{y^0}{2^m}\right],$$

when the y terms are in two's complement notation. If the y terms are taken two at a time, the product becomes

$$X \cdot Y = X \sum_{i=0}^{m} 2^{-m+i}\,(y^{i-1} - y^i)\,.$$

The y numbers can have the value of a one or zero only, and the most-significant bit, $-(y^m)$, represents the number's sign. When it equals one, the number is negative; when it's zero, the number is positive. The second bit, $y^{m-1}/2$, has the weight of 1/2, and $(y^{m-2}/4)$ has 1/4, etc. (Negative exponents of y are dropped.) Thus, the two's-complement number 1.0011, in ordinary binary, is −0.1101, or −13/16.

Taking two's-complement bits, two at a time, provides four possible combinations for each pair as shown in the following table, where $F_i = y^{i-1} - y^i$ and P_i is a partial product:

y^{i-1}	y^i	F_i	P_i
0	0	0	0
1	1	0	0
0	1	−1	−X
1	0	1	X

The partial product of each pair is shifted one bit to the left successively for increasing values of i and all are summed to yield the total product.

Partitioning of system tasks simplifies digital signal processing

by Victor Godbole

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PARTITIONING OF SYSTEM TASKS SIMPLIFIES DIGITAL SIGNAL PROCESSING

By utilizing a conventional microprocessor for data handling, I/O, and decision making, an intelligent peripheral device is freed to handle complex signal processing tasks in real time

Victor Godbole American Microsystems, Incorporated
3800 Homestead Rd, Santa Clara, CA 95051

The complexity of signal processing in voiceband data communications varies with the nature of the application. Low speed modems using frequency shift keying techniques can perform entirely in the analog domain. On the other hand, in higher speed modems the use of multilevel data encoding schemes results in a significantly higher level of complexity. It is difficult to achieve high precision and stability when using analog techniques to implement the large amounts of filtering and adaptive equalization schemes employed in high speed modems.

By contrast, digital signal processing techniques are better suited to high speed modem applications and offer several distinct advantages. Performance is stable and repeatable from unit to unit. High precision can be achieved and is limited only by the number of bits that the signal processor can handle. Greater flexibility is also obtainable because it is easier to modify response by simply varying the proper arithmetical coefficients. Moreover, major building blocks of the arithmetic unit (adder and subtracter, multiplier, etc), can be timeshared, allowing complex tasks to be broken down into several repeatable fundamental tasks.

Suitable hardware in large scale integration (LSI) form is now becoming available to reduce component count and the cost of hardware implementation in applications that require digital signal processing techniques. Conventional microprocessors, since they lack needed arithmetic power and speed, are not well suited to the requirements of complex digital signal processing. Algorithms used in such processing are highly multiplication intensive. Even for only a single, second order, digital filter section, the processor must perform four multiplications, four additions, and two store operations. Conventional microprocessors cannot perform 8- or 16-bit manipulations fast enough to process a significant number of these filter sections within the typical 125-μs sampling interval corresponding to the 8-kHz sampling rate used in voiceband data communications systems.

The necessary ingredients of a digital signal processor are a specialized architecture and an instruction set tailored to provide computational efficiency. A specialized digital signal processor, configured as an intelligent peripheral to operate in conjunction with a conventional microprocessor, allows efficient partitioning

of system tasks. The microprocessor then becomes a controller for managing data flow, including input/output (I/O), and for calling out the application-specific routines stored in the signal processing peripheral. In turn, the peripheral actually performs the hard work associated with a specific signal processing task.

Architectural Functions

For optimum architecture, the general requirements of digital signal processing algorithms, as well as specific application details, must be considered. Filtering is a basic requirement in most voiceband communications systems. Both recursive (filters using feedback) and nonrecursive (transversal filters) are widely used. Because they provide minimum delay distortion, transversal filters are most suitable when a linear phase characteristic is required. Recursive filters are generally used when a steep filter response is desired with minimum computation. However, recursive filters exhibit a nonlinear phase characteristic that results in higher delay distortion.

A basic second order filter section can be used as a building block for higher order filters. In the equation for a second order recursive filter section

$$W_n = X_n + a_1 W_{(n-1)} + a_2 W_{(n-2)}$$

$$Y_n = W_n + b_1 W_{(n-1)} + b_2 W_{(n-2)}$$

a_1, a_2, b_1, and b_2 are fixed coefficients.[1] X_n and Y_n represent input and output samples respectively, and W_n, $W_{(n-1)}$ and $W_{(n-2)}$ are intermediate computed results for present and past sampling instants. Clearly, some provision must be made for storing signal and coefficient data. Examination of the equations points out that half the data memory in a system can be read only memory (ROM) while the other half must be random access memory (RAM) holding variable signal data. This half ROM, half RAM division of data memory should achieve a considerable reduction in the overall size of data memory. To improve throughput, one must also make provision for accessing the coefficient data word simultaneously with the signal data word for multiplication. This calls for a dual output port memory structure. Use of a pipelined multiplier achieves still further improvement in throughput.

When the multiplier delay equals one instruction cycle, a product becomes available from the multiplier during the instruction immediately following the instruction in which data were entered into the multiplier. An instruction structure can then be realized to read two words from data memory, perform an arithmetic operation on them, and store the result back into data memory, all in only one cycle. This sort of dual operator instruction format for simultaneous arithmetic and data transfer operation is vital for realizing computational efficiency. The equations also show that digital signal processing algorithms, such as recursive filter algorithms, operate extensively on delayed samples. A register must temporarily hold a value that was read from a location in data memory during one instruction until it is transferred to another data memory location during the next instruction. This implements digital filter Z^{-1} delays with minimal software overhead.

To provide sufficient dynamic range, an appropriate word length should be chosen to represent signal and coefficient values. In most applications, a 70-dB dynamic range is adequate, indicating that a 12-bit word is acceptable. Also, as pointed out earlier, higher order filters can be implemented by using a second order filter section as a building block. When permitting higher order computations to use the same set of instructions or subroutines designed for the basic second order filter, some facility must be provided for multiple iterations and iteration testing.

Instruction Repertory Promotes Efficiency

Special instructions implemented by the S2811 demonstrate the impact of instruction set design on digital signal processing efficiency.[5,6] For example, signal processing algorithms such as that for the second order recursive filter operate extensively on delayed samples. By using a special instruction that transfers the V-port input register content to RAM (TVPV), the previous value read from the V-port passes directly to a memory location designated in the current instruction, implementing digital filter Z^{-1} delays with minimum software overhead.

A set overload protect (SOP) control mode allows the accumulator output to saturate to the maximum or minimum signed value, depending on the direction of overflow, whenever an overflow occurs. This feature is invaluable for implementing recursive filters, where oscillations might be caused by feedback after accumulator overflow.

First level loop nesting normally involves a great deal of software overhead. To avoid this, the S2811 includes a hardware loop counter allowing up to 32 iterations. Jump instructions such as jump conditional direct (JMCD) and jump conditional direct and increment (JCDI) test the loop counter for a zero condition before performing the program step, providing iteration test and loop control without adding program instructions.

Efficiency increases in digital signal processing when several tasks are performed in parallel. Complex (multifunction) instructions simplify parallel task implementation. Some signal processing tasks must fetch data words that are separated by a fixed offset in memory. An instruction that interchanges the roles of the base and index registers (SWAP) allows the base and index registers to work together and achieves a dual base addressing scheme. For example, the jump conditionally dual tracking (JCDT) instruction increments the base and index registers. It then tests to determine whether the loop counter is zero, and, if it is not zero, branches to the specified address. The loop counter is decremented after the test.

This approach saves several steps when programming iteration loops that fetch and process data words separated by fixed memory offsets, thereby reducing execution time in, for example, Fast Fourier Transform processing.

These and other considerations suggest an architecture that is specialized toward efficient implementation of digital signal processing algorithms. Once the basic building blocks are identified, the next task places a quantitative judgment on the sizes of the various blocks. How much data memory is required? How large an instruction ROM? How many different instructions? A careful study of various applications, cost vs size tradeoffs, and the level of design complexity provided answers to these questions.

Application Examples

The specialized architecture selected for use in the AMI S2811 signal processing peripheral (SPP) is shown in Fig 1. Although specialized for voiceband data communications requirements, this architecture also supports any algorithms or numerical computations that are multiplication intensive, that use delay elements, and that are suitable for easy implementation of in-place computations. Filtering is one of the basic signal processing tasks encountered in voiceband data communications systems. Among these tasks are to limit bandwidth, smooth a demodulated signal, smooth a rectified waveform for averaging, and provide equalization. Both recursive and transversal filter types are widely used.

Transversal Filter

A typical application for a transversal filter is in the modem's receiving circuit, where it is used to remove the high frequency components from the demodulated signal. The equation for an N-stage (N-tap) transversal filter (Fig 2) can be written as

$$X(k) = C_0x(k) + \sum_{n=1}^{N} C_nx(k-n)$$

Here C_1 to C_n are respective tap weights and x(k) and X(k) represent, respectively, the input and output sample values at the kth sampling instant. The equation shows that computation of X(k) involves a "sum of products" type operation. It is convenient to carry out the computation sequentially.

Operations to be performed at any given tap can be summarized as follows: accumulate product from previous tap; start multiplication for current tap; update the signal value associated with the current tap by shifting in the signal sample from the previous tap; and decrement the iteration counter. If the iteration count is zero, accumulate a final product, store it in the memory location designated for the output sample, and

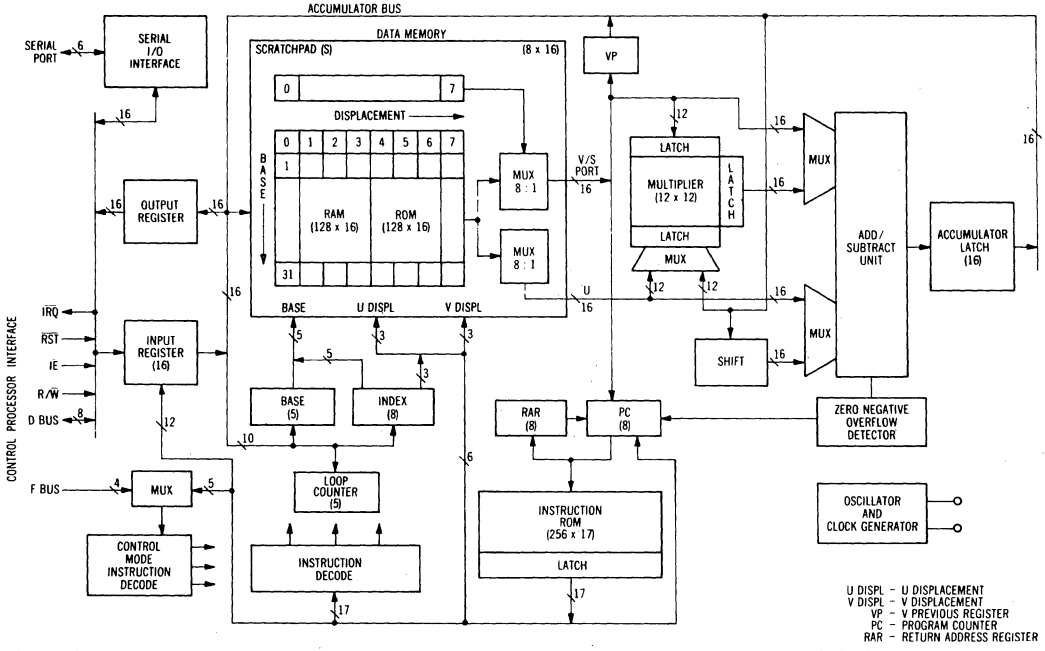

Fig 1 Specialized signal processing architecture. Arithmetic unit consists of high speed parallel multiplier and addition/subtraction unit (ASU). Dual port data memory is organized as half RAM, half ROM, for storing signal and coefficient data, respectively. Instruction ROM holds signal processing routines. Serial and parallel I/O ports provide signal and control interface

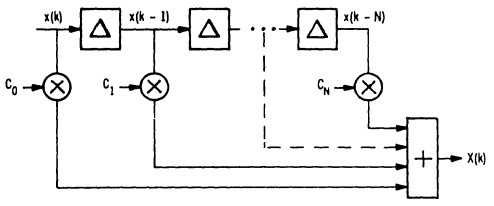

Fig 2 Transversal filter. Output X(k) at a given sampling instant is a function of present and past values of input x(k) only. No recursion of output occurs. Signal value at each tap is multiplied by its tap weight. Products from all taps are accumulated to produce output

terminate the computation sequence. If the iteration count is nonzero, proceed to the next tap.

Implementing the Filter

An SPP can implement the filter by storing a sequence of instructions in the form of a program or subroutine within the instruction ROM and by creating a memory map for accessing signal and coefficient data. Fig 3 shows the computational sequence in the SPP when implementing a filter of this type. In a typical transversal filter routine designed to run on the SPP, the base register and the loop counter are first initialized to proper values. The entire series of steps for a given tap calculation is achieved by a single instruction such as

APA TVIB UV(4,0)

Preceding this instruction, a complex (multifunction) command extends the computation sequence through all taps until the loop counter reaches zero. To end the routine, an instruction accumulates the final product and transfers it to a memory location designated to hold the output sample.

Availability of complex (multifunction) instructions coupled with parallel processing minimizes software overhead. To implement an N-tap transversal filter, for example, six source statements, six machine instructions, and a total processing time of N + 5 instruction cycles are required. With a 300-ns instruction cycle time, this corresponds to an execution time of about 5 μs for a 12-tap filter. The typical 8-kHz sampling rate in voiceband data communications systems allows 125 μs for all the different signal processing tasks that must be performed, so it is important to minimize individual task computation times. This permits one signal processing device to perform all of the tasks that most applications require.

Equalization

Voiceband data communications channels are nothing more than voice grade telephone lines, and these introduce both amplitude and delay distortion into the transmitted signal. Amplitude distortion is caused by variations in gain as a function of frequency within the passband. Delay distortion is caused by the nonlinear relationship between the signal's phase shift and its frequency characteristic. Both types of distortion result from channel characteristics. Delay distortion causes interference between adjacent transmitted information samples; it is also known as intersymbol interference (ISI).

As the data transmission rate increases, so does the need for equalization. To avoid this need, various grades of conditioned lines with prescribed distortion limits are available from telephone companies; however, these must be leased as private lines. On the other hand, modems can incorporate equalization to allow the use of ordinary dial-up lines and at the same time attain a higher data rate. Equalization can be fixed to match average line conditions, or it can be manually or automatically adjustable. High performance modems use automatic and adaptive equalization techniques. With the SPP, algorithms for such equalization techniques can be easily implemented.

The most commonly used form of easily adjustable equalizer is a transversal filter similar to the one used in baseband filtering. Each tap on the (2N + 1)-tap

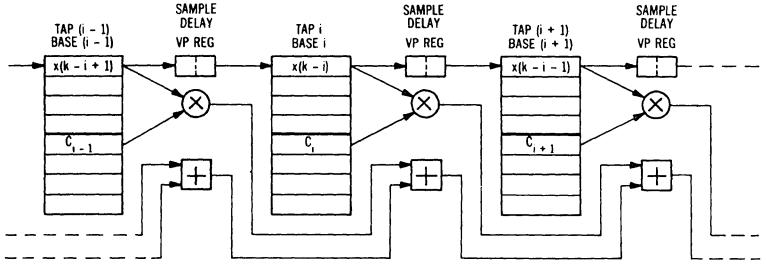

Fig 3 Filter implementation. A group of memory words (base) is associated with each tap. In each base, signal value is stored in RAM location and coefficient value is stored in ROM location. Taps are processed in sequence. Adder, multiplier, and delay register blocks are used repeatedly, under program control, until all taps have been processed

transversal equalizer is connected to a summing amplifier through a variable gain device. The equation for the equalizer can be written as

$$X(k) = \sum_{n=-N}^{N} C_n x[k - (N + n)]$$

where x(k) are input samples to the equalizer and X(k) are equalizer outputs.

Consider first the use of an equalizer in a baseband pulse amplitude modulation (PAM) system where the equalizing filter is inserted between the receiving filter and an analog to digital converter (ADC).[2] Ideally, if the received pulse has a peak at t = 0 and ISI on both sides, one would like to have

$$X(k) = \begin{cases} 1, \text{ for } k = 0 \\ 0, \text{ for } k = \pm 1, \pm 2, \ldots, \pm N \end{cases}$$

This condition cannot always be realized because there are only 2N + 1 tap gains available. For example, a 3-tap equalizer can be designed for zero ISI in the equalized pulse on either side of t = 0, but with a small ISI at points further out from t = 0 where the unequalized pulse had zero ISI (Fig 4).

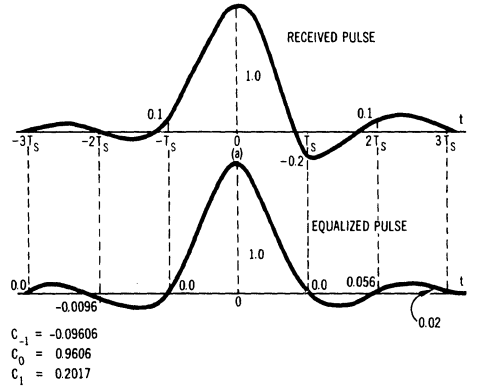

Fig 4 Three-tap equalizer input/output. Received pulse has peak at t = 0 and ISI on both sides of t = 0. Three-tap equalizer can be designed for zero ISI on either side of t = 0, but with small ISI at points well removed from t = 0 where received pulse may have had zero ISI

Complex Valued Adaptive Equalizer

Equalizers used in high performance modems extend the basic transversal equalizer just described. In a typical configuration for a 4800-bit/s modem conforming to CCITT V.27 specifications[3], the equalizer is inserted between the baseband filter and the quadrature phase shift keying (QPSK) detector. The baseband filter actually consists of two transversal filters that smooth the inphase and quadrature phase components of the demodulated signal. The inphase and quadrature phase components can be considered as forming a complex number x + jy as input to the equalizer. For an adaptive equalizer, the tap gains given by complex value $a_n + jb_n$ are updated from computations performed on error signals e_x and e_y supplied by the QPSK detector.

In a typical application, the baseband filters are sampled at 8 kHz, and the equalizer is sampled at 1.6 kHz or at the baud rate. It is necessary to sample baseband filters at the higher sampling rate in order to remove higher frequencies contained in the signal after demodulation. Thus, four out of five filter samples are simply discarded, and the equalizer processes one out of every five samples supplied by the filters. Equalizer output is a complex number that is processed to decode the received symbol. An error signal can be computed on the basis of the actual received symbol and the equalizer output. Equalizer tap gains are updated at a baud rate based on this error signal.

Typically, the equalizer may consist of 8 to 16 taps. Fig 5 shows the signal flow graph for a 16-tap equalizer.

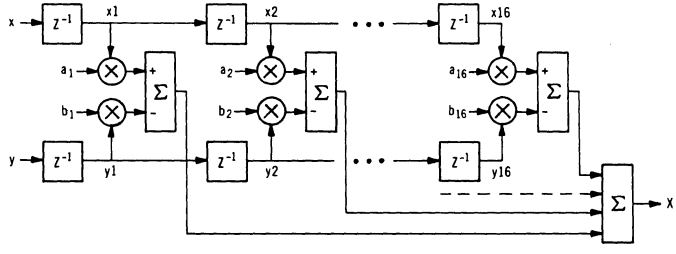

Fig 5 Equalizer implementation. Inphase and quadrature phase components are multiplied by their respective tap weights. Resulting quadrature phase data is subtracted from inphase data. Results from all taps are summed to produce real (inphase) component of equalizer output. Imaginary (quadrature phase) component of output is produced separately in similar manner

The equations for the 16-tap complex valued equalizer can be written as

$$X = \sum_{n=1}^{16} a_n x_n - b_n y_n$$

$$Y = \sum_{n=1}^{16} b_n x_n + a_n y_n$$

$$x_{n+1} = Z^{-1} x_n$$

$$y_{n+1} = Z^{-1} y_n$$

These equations are derived from the result of multiplying two complex numbers as follows:

$$(x_n + jy_n)(a_n + jb_n) = (a_n x_n - b_n y_n) + j(b_n x_n + a_n y_n)$$

Here, X and Y represent, respectively, the real and imaginary (inphase and quadrature phase) components of the equalizer output.

The complex valued equalizer can be implemented in a manner similar to that of a transversal filter on the SPP. However, there are some important differences. Coefficient values are not fixed; therefore, they must be stored in RAM. Equalizer computation involves complex numbers; hence, both x and y input data values are stored in adjacent RAM locations. Equalizer output also is a complex number whose real and imaginary components are computed in separate passes.

Other common signal processing tasks such as carrier generation, modulation and demodulation, and averaging can be handled in much the same fashion after programming appropriate algorithms for their implementation.

Once the SPP has been programmed with application-specific routines, its use in the system proceeds completely under microprocessor software control. Hardware interfacing of the SPP is straightforward because it is handled like any other memory mapped peripheral. In a general purpose signal processing system configuration (Fig 6), serial I/O ports are used directly with ADCs and digital to analog converters (DACs) to provide a signal interface. A parallel port implements the control interface to the microprocessor.

To prevent aliasing of out-of-band signal and noise frequency components caused by the sampling process, the input analog signal must be bandwidth limited before it can be digitized and processed in the SPP. For providing bandwidth limiting to 3.4 kHz, standard D3 channelbank[4] filters commonly used in pulse code modulation (PCM) telecommunications are ideally suited to perform the antialiasing filter function in the signal processing system. D3 channelbank filters are now available as monolithic integrated circuits, further simplifying system design. On the output side, a similar low pass smoothing filter should be used after the DAC, limiting the signal spectrum to around 3.4 kHz as required in voice grade telephone channels.

In a system, the microprocessor typically sets up the initial conditions and parameters, then begins execution of a signal processing task by calling out an application-specific routine stored in the SPP. Depending on the application, processing may continue until the SPP is interrupted by the microprocessor, perhaps to select a different algorithm or for periodic updating of adaptive algorithm coefficients. Or, the SPP may interrupt the processor for intermediate I/O conditions or to signal the end of a processing task. Thus, either an open ended or an interactive mode of signal processing can be selected for maximum flexibility.

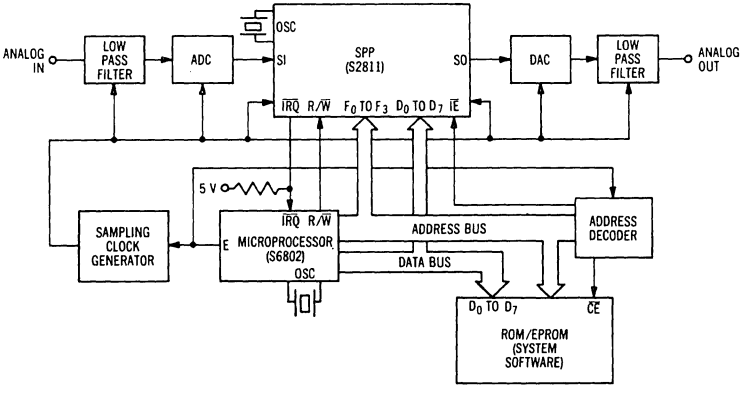

Fig 6 Signal processing system block diagram. Analog input signal is bandwidth limited by low pass filter, digitized by ADC, and processed by SPP under microprocessor control. SPP output is converted to analog form by DAC and smoothed by low pass filter to produce analog output signal

Conclusion

Designers of high performance voiceband data communications systems can simplify most commonly encountered digital signal processing tasks by selecting devices with architectures optimized for signal processing. Such devices use parallel processing to implement highly multiplication intensive sum-of-products type algorithms most efficiently. Careful consideration must be given to partitioning of system tasks. It is best to have normal data handling, I/O, and decision making tasks handled by a conventional microprocessor, while leaving the complex tasks of signal processing to a specialized device organized as an intelligent peripheral that operates in parallel with the microprocessor.

Acknowledgments

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Victor Godbole, department manager for communications applications engineering at American Microsystems, Inc, holds an MSEE from Oklahoma State University and has published several technical papers. He has been principal engineer for switching systems design at North Electric Co and design engineer at Cleveland Electronics, Inc.

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AA 601

An introduction to linear CMOS capabilities

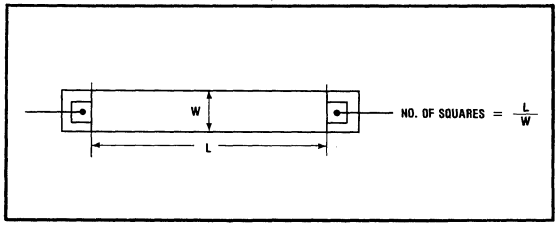
An Introduction to Linear CMOS Capabilities

The Linear Elements

It is well know that CMOS is a very nice process for implementing digital logic functions because of these characteristics: low power dissipation, high noise immunity, wide operating supply voltage range and medium to high speed capability. Various digital circuits from simple watch to sophisticated microprocessor circuits with a variety of CMOS processes have been fabricated to suit a given application. It is not well known that CMOS is also a very nice process for implementing analog functions such as filters, A/D and D/A converters, phase lock loops, voltage references, waveform synthesis, etc. In the past few years AMI has developed, primarily due to the extensive work on the codec chips, unique design and fabrication capabilities in this area. It is the intent of this article to take an overview of these capabilities in as non-technical a manner as possible.

To implement most analog functions one needs to be able to fabricate these discrete elements: resistors, capacitors, transistors, switches, diodes, zener diodes, operational amplifiers, comparators, current mirrors, buffer amplifiers, etc.

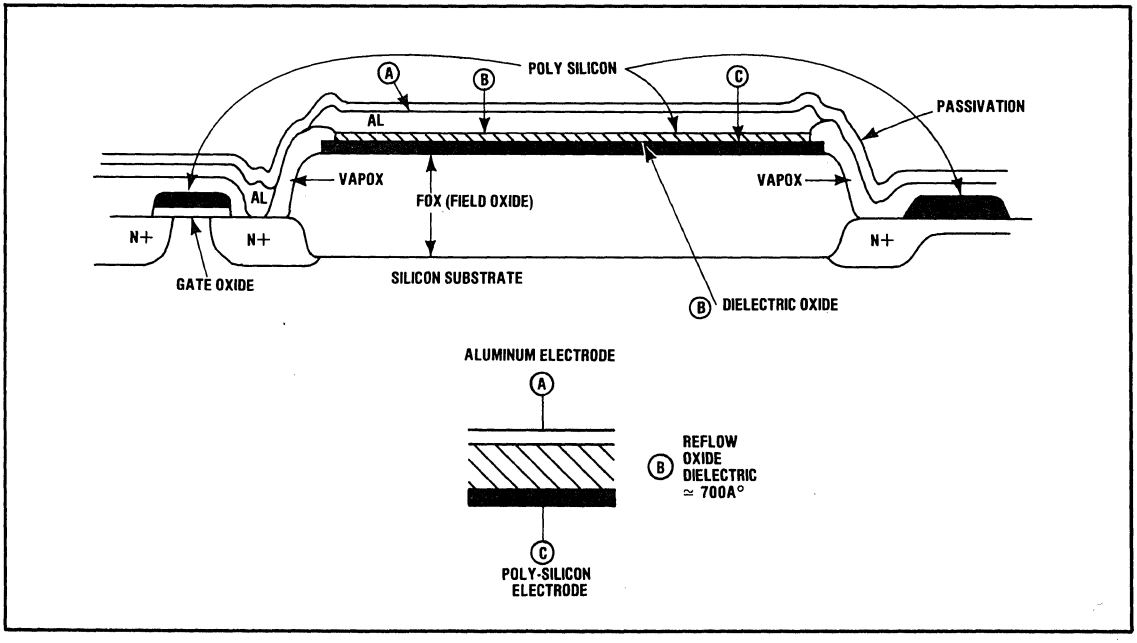
Resistors: There are at least four methods of fabricating a resistor. P Well, Diffused, Poly and Active device. Basically a resistor is formed by long and narrow lines of a high resistive material between two contacts.



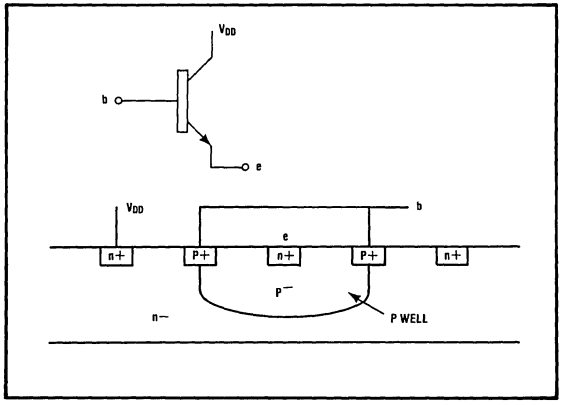
The resistance is proportional to the number of squares contained in the material. The width used is usually minimum, such as 0.3 mil giving 3.3 squares per mil of the length. The amount of resistance per square depends upon the method of fabrication. It varies from a low 20Ω/sq for n+ diffused resistors to a high 5kΩ/square for P well resistors. No matter what method is used, it is possible to make precision resistors. The absolute accuracy varies from 3 to 1 to 5 to 1 over process parameters, operating voltage and temperature. Therefore, absolute resistors are only used in non-critical applications such as pull up or pull down, bias resistors for oscillators and zener dioes, current limiting resistors for LED drivers, for interconnection between elements on chip. Poly resistors are least voltage dependent, have low temperature coefficient and less variation. They are used in ladder networks for A/D or D/A converters where a high accuracy of resistor ratios is required. A ratio accuracy of better than 1% is feasible.

Capacitors: In our silicon gate CMOS processes, small capacitors can be easily formed between two layers with metal as one plate and either poly-silicon or source drain diffusion as the second plate. Oxide regrowth which occurs during the processing sequence serves as the dielectric of the capacitor.

The CMOS capacitors are voltage invarient and have a very low temp. coefficient. Since the value of the capacitance depends upon the area, the ratio of two adjacent capacitors can be controlled very accurately. Typically an accuracy of better than 0.1% is attainable. This is of great significance in filter and A/D, D/A converter designs. Typically a capacitance of 0.37pF/mil^2 is achieved limiting the useful range of capacitances from less than a pF to hundreds of pF.

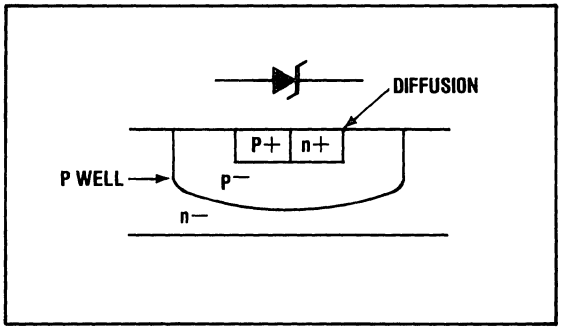


Transistors: It is only possible to make NPN transistors with the collector connected to the substrate (V_{DD}) using our CMOS pro-



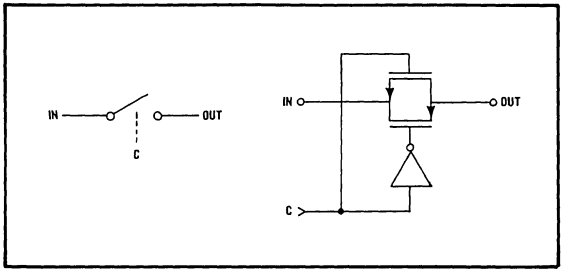
cesses. It has a vertical structure meaning it is not formed on the surface of the chip, but it is as deep as a P well. Typically these transistors have a DC gain (β) of 300 to 500, reverse collector emitter breakdown voltage (BV_{CEO}) of 50V bandwidth (f_T) of 40 to 50MHz. The current carrying capability depends upon the area of the device. In the S2559 tone generator we have an output transistor capable of sourcing 100mA with a voltage drop of less than 1.5V at a supply voltage of 10V. These transistors are used for low impedance drives in buffer amplifiers, high output source current capability, etc.

Zener Diodes: These could be fabricated one of two ways, Poly or diffused. Poly is impure silicon, so these zeners do not have a sharp breakdown. A sharp breakdown characteristic can be obtained with an extremely heavily doped P-N junction.



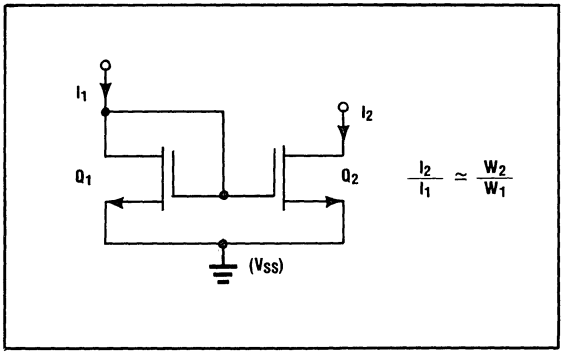
A typical on-chip zener diode has a breakdown voltage of 6 volts. The current carrying capacity depends upon the area of the device. Higher voltages can be obtained by cascading.

Switches: Switches are simply implemented by a pair of devices formed as a transmission gate. Switches are important in analog functions. They are used for sampling of analog signals, for multiplexing or demultiplexing of several signals, for switching of time constants, for sample and hold, or for simply an on/off control of signals.



In our CMOS processes we can realize an on resistance of less than 1000 ohms, an off resistance of billions of ohms. In analog processing the capacitance of the switches, the on as well as off impedances, plays an important role.

Current Mirrors



A current mirror is an element which produces a mirroring current I_2 as a function of both input current I_1 and a ratio of the device widths. Inserting a switch (transmission gate), an on-off control of current I_2 can be implemented $I_2 = \frac{W_2}{W_1} C I_1$

The control signal bit C can have values 0 or 1. By binary weighting of several mirroring devices a D/A converter can be implemented. Because of ratio design, accurate current mirrors can be produced. Therefore, this is a very valuable technique in D/A converter designs, waveform synthesis, current sensing and amplification, etc.

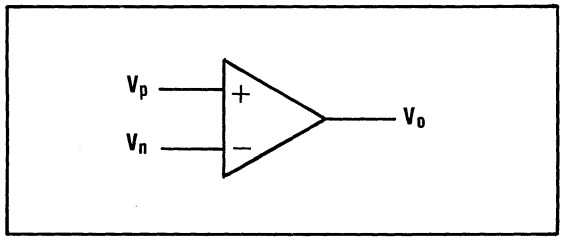
Operational Amplifiers: Operational amplifier is the most important linear element. To implement any kind of sophisticated analog function, this is a must.

The Op Amp

The most important of all linear elements is the operational amplifier or what is commonly known as the Op Amp.

What is an Op Amp?

An Op Amp is a direct coupled high gain amplifier whose performance can be controlled by use of feedback. Externally, it is represented by the following symbol.



Internally, it consists of several series connected transistor stages. Figure I shows a typical CMOS Op Amp. Functionally, if a positive voltage is applied to the positive (+) input, the Op Amp output will go positive. Likewise, a positive voltage on the negative (−) input will cause the output to go negative. The Op Amp has a very high voltage gain for differential input signals effective between the two inputs. The Op Amp also has a very low voltage gain for signals applied to both inputs simultaneously. This is called the common mode rejection capability of the Op Amp. By using discrete elements such as resistors and/or capacitors in conjunction with the Op Amp we can construct many useful circuits such as non-inverting or inverting amplifier, differential amplifier, summing amplifier, integrator, differentiator, voltage to current, current to voltage or current to current converter, low-pass, high-pass, bandpass or bandstop filter, comparator, etc. These all represent important building blocks for analog-circuit designs

Ideal vs Practical Op Amp

None of the ideal parameters listed below are achieved or ever achievable by practical Op Amps.

1. Differential Voltage Gain = ∞
2. Common-mode Voltage Gain = 0
3. Bandwidth = ∞
4. Input Impedance = ∞
5. Output Impedance = 0
6. Output Voltage = 0 when input voltage = 0
7. Output Noise = 0
8. Drift with Temperature = 0

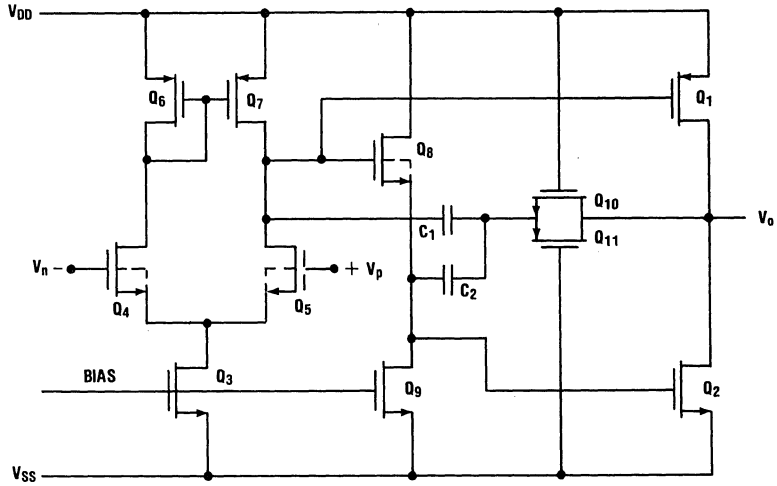
Parameters of a practical CMOS Op Amp are listed in Table 1. These non-ideal characteristics place a top limit on the performance of the building blocks mentioned above.

Inside the CMOS Op Amp

To those who are familiar with transistor circuits, a brief description of the circuitry inside the Op Amp might be enlightening. Those who are not interested may safely skip this section. In passing, those interested in real estate may note that our CMOS Op Amp occupies very little space—172 sq. mils to be exact!

As shown in Figure 1, the Op Amp consists of an input differential amplifier (Q_4, Q_5) a current source (Q_3), a current mirror (Q_6, Q_7), a level shifter (Q_8, Q_9), an output stage (Q_1, Q_2) and internal compensation network (Q_{10}, Q_{11}, C_1, C_2).

Figure 1. CMOS Operational Amplifier Schematic



The current source is required so that the circuit will have a large common-mode rejection. The input differential amplifier stage determines the ultimate gain stability, bias drift, input impedance, slewing rate, bandwidth, noise and common-mode rejection of the Op Amp. Subsequent stages have little effect on these parameters. The level shifting amplifier provides a DC level shift such that the output voltage of the Op Amp is close to zero when the input differential voltage is zero. The output stage is like a digital inverter except the gates of the output devices are not connected to each other. They are connected to the input and output of the level shifter. The output stage is designed to provide low output impedance and high current drive capability. Without compensation Op Amp circuits that use negative feedback will oscillate because the Op Amp has a voltage gain much higher than unity at a phase shift of 180°. To reduce the gain below unity at 180° phase shift, a compensation network is included. The compensation network places a pole at a low frequency (10Hz) to reduce gain below unity at 180° phase shift. Comparators do not use negative feedback. Internal compensation is therefore not required for comparator circuits. This results in lower area for comparators.

Table I. CMOS Operational Amplifier Specs

Low Frequency Gain	90dB
Unity Gain Bandwidth	2.5MHz
Offset Voltage	
—Standard Deviation	10mV
—Mean	+0.4mV
CMRR	73dB
PSRR	70dB (DC) to V_{SS} 68dB (DC) to V_{DD} (measured)
Slew Rate	2V/μsec
Power Dissipation	1.6mW
Noise	26μV rms[1]
Area	172 mil^2

NOTE: 1. integrated over a band 10Hz-1MHz.

Summary

An Op Amp is a very versatile building block available to designers of analog circuits. Though far from ideal, the CMOS Op Amp is at least as good as the popular bipolar 741 Op Amp in performance at the same time with a power consumption that is much lower. In design of precision A/D, D/A converters, switched capacitor filters and other analog circuits, a good Op Amp is essential. Our CMOS linear capabilities represent the state-of-the-art in the design of the Op Amp.

Switched Capacitor Filters

Combinations of the linear elements discussed before allow us to implement complex linear functions such as active filters, A/D and D/A converters, Reference Voltage Sources, Sample and Hold Circuits, Phase-Lock Loops, Auto Zero Loops, etc. Now we will look at the switched capacitor filters—our design capabilities, characteristics and constraints as they apply to this linear function and some of the applications of this function.

What is a Switched Capacitor Filter?

A "switched capacitor" filter is similar to an active filter built around RC networks except where all resistors are replaced by small capacitors switched at a high rate. The principle behind this technique is illustrated in Figure 1. In discrete RC active filters the accuracy of absolute RC products is the controlling factor in achieving a desired performance. In switched capacitor filters the RC products are replaced by capacitor ratios and sampling frequency. Earlier we saw that capacitor ratios can be controlled to better than 0.1% accuracy on a CMOS chip. The sampling frequency can be controlled to any accuracy desired; usually this is externally supplied by the user. The consequence is that active filters can be implemented monolithically with great precision and without the need of external discrete components or need for trimming.

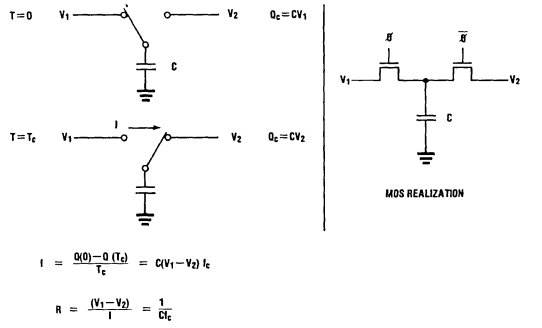
We have successfully fabricated a sixth order elliptic low pass and a third order elliptic high pass filter as part of the Codec chip set (S3501/02). We have also made a DTMF bandsplit filter (S3525). In addition, these techniques are also used in our many custom circuits.

Advantage of Switched Capacitor Filters

- The parameters of a switched capacitor filter—Gain, Q, center frequency, bandwidth, etc. are accurrately controlled
- Stability with time and temperature is excellent
- No external precision components required
- Component trimming is eliminated
- Reduced cost of filter function plus fewer leads, less board space, less assembly
- Low power
- Can be combined with **other** analog and digital function to form a complete **subsystem** on a **single** chip

Due to the upper limit on the sampling frequency of 200kHz and capacitor ratio of 50, the SCF's at present are useful in the audio frequency range. Even so, there are numerous applications where they can be used as summarized below.

Figure 1. Switched Capacitor Resistor



Applications of SCF's

Applications that require fixed precision filters without trimming or special processing and that are slated for high volume production are best candidates for monolithic switched capacitor filters. Examples are:

Communications

Voice frequency transmit and receive filters in PCM systems
DTMF bandsplit, MF and SF filters for tone receivers
Transmit and receive filters for data modems
Precision programmable attenuator for office wiring loss compensation

Music

Voicing filters for organs
Filters for rhythm sections

Signal Processing

Signal analysis and synthesis
Synthesizing speech using formant filters

"Switched Capacitor" A/D Converters

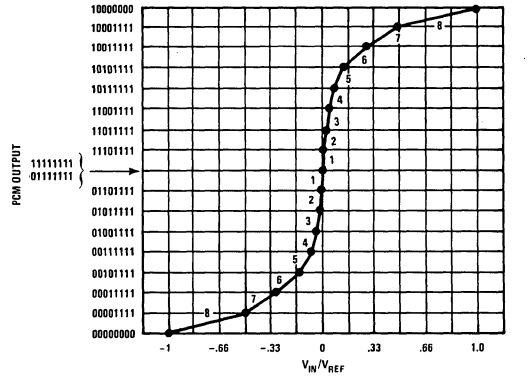
Analog to digital and digital to analog conversion techniques have become important as well as abundant due to the increasing use of electronic computers to analyze or construct analog signals. Since computers are getting faster every day, the need for precision high speed analog to digital converters is growing. Our linear capabilities, especially those in CMOS, allow us to implement high speed and accurate A/D and D/A converters. Resolution of 12 bits with a conversion speed of under 50μs is feasible with our techniques. What is our most favored technique? "Switched Capacitor", of course! The technique works on the principle of successive approximation and charge redistribution.

The accompanying diagrams illustrate a three step procedure for implementing the A/D converter used in our codec. Since a non-linear (logarithmic) transfer function is required (Figure 1), the capacitors in the ladder are binary weighted.

The first step is to sample the input voltage V_{IN} (Figure 2-A) by momentarily closing the switch S_V. At this point the bottom plates of all capacitors are connected to ground. The result is that the top plate is charged to $Q_C = 255C\ V_{IN}$. The voltage on the top plate V_T equals V_{IN}.

The second step is to determine in which segment the voltage V_{IN} lies by using successive approximation. First, bottom plate of capacitor C_1 is connected to a negative reference voltage V_{REF}. Since charge is conserved, V_T changes to $V_T = V_{IN} - \frac{V_{REF}}{255}$. This is compared with ground in the comparator. Since in the chosen example, V_{IN} lies in the fourth segment, V_T after the first try will exceed ground. The process is continued as shown in the diagram

Figure 1. μ-255 Law Transfer Characteristics



(Figure 2-B) until V_T is brought down just below ground. This occurs when the bottom plates of the first four capacitors is connected to the negative reference voltage. The appropriate segment is thus identified.

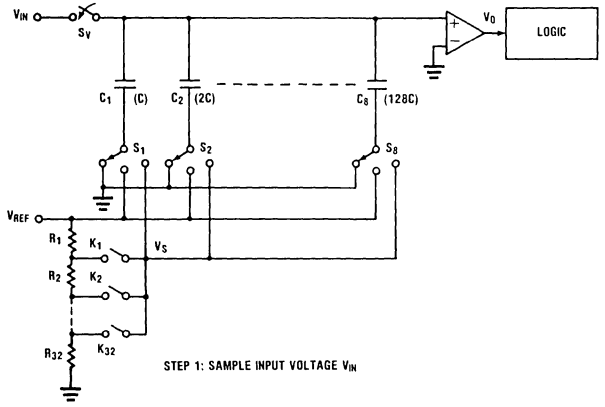
The third step is quantization within the identified segment. To do this the bottom plate of the identified segment capacitor (C_4 in the example) is connected to a voltage source V_S which is a fraction of V_{REF} (Diagram 2-C). Once again successive approximation is used to find the correct fraction. In the codec, sixteen equal levels (called steps) are used per segment. Thus, the end result is to identify one of eight segments (3-bit code) and one of sixteen levels (4-bit code). A sign bit is added to indicate whether the input voltage is positive or negative. The final results is an 8-bit digital word representing the input V_{IN}.

Note that 8 clock periods are required for segment identification while 4 clock periods are required for step identification. Thus, the total conversion time is 12 clock periods. Each of the cycles can be accomplished in as little as 4μs, giving under 50μs as the conversion time. It is important to note that either a linear or non linear transfer function can be easily implemented.

The process of successive approximation is well suited for microprocessor control. A precision high speed A/D converter can be incorporated into a single chip microcomputer with the basic architecture shown in the diagrams. What is most interesting is that depending upon the algorithm chosen in the software, a linear or non-linear (logarithmic) transfer function can be implemented. Resolution desired can also be software controlled.

Switched capacitor filters and switched capacitor A/D, D/A converters are the two most important tools in our arsenal and are being successfully used in both standard and custom circuit designs.

Figure 2-A. Successive Approximation Switched Capacitor Companding A/D Converter



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An introduction to digital filters

by Dr. Gwyn P. Edwards

An Introduction to Digital Filters

By Dr. Gwyn P. Edwards
Senior Applications Engineer

Introduction

The digital filter is a sampled data filter made purely of digital hardware. It performs operations on the sampled digital signal in the same manner as the analog filter performs operations on a continuous analog signal. The analog continuous filter is the physical realization of a differential equation, and the output of the filter is the solution of that differential equation when it is excited by the input signal. The discrete (or sampled) equivalent of the continuous differential equation is known as the difference equation, and the digital filter is the solution of this when excited by the input signal.

The analog continuous filter is composed of resistive and reactive elements, which give rise to the differential equation which is its transfer function. Consider the example shown in Figure 1 (a). We have:

$$V_o = V_I - RCdV_o/dt. \quad (1)$$

V_o is the solution of this equation when a signal V_I is applied.

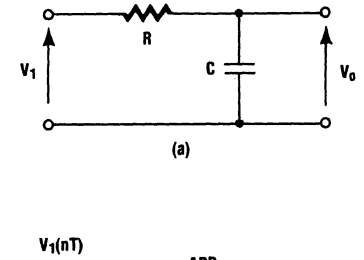
The digital sampled data filter is composed of delay units (shift registers), multipliers (which perform attentuation or amplification), and summers. These units give rise to the difference equation which is the transfer function. Consider the example shown in Figure 1 (b). We have:

$$V_o(nT) = V_I(nT) - a.V_o((n-1)T) \quad (2)$$

where nT represents the time during the nth sample period. Thus (n-1)T represents the time during the (n-1)th sample period, so that V((n-1)T) is V(nT) delayed by a time T.

V_o is the solution of this equation when a signal V_I is applied. The terminology V(nT) is used to represent a sampled signal, which has a constant value for a period T between two sampling instants. n represents the sample number, and is an arbitrary integer.

Figure 1.



In both cases it is easy to see that it is not possible to write the equations in such a form that give the output directly, since in one case the output depends on its own derivative, and in the other the output depends on previous values of itself. A transformation technique is required to rewrite the equations in a more useful form. In the analog case the well known Laplace transform is used, and in the other case the Z transform is used.

The Z Transform

The Laplace transform, although invaluable in conventional circuit theory, is of little or no use in such cases as sampled data filters, e.g. transversal filters. Such filters are based mainly on the summation of present and past values of signals, and so a transform operator based on time delay or advance is more useful than the Laplace transform operator S. Such a transform is the Z transform. Although this may be used to analyze linear continuous circuits in some cases, we shall only consider discrete-time, or sampled, circuits here.

The Z transform V(z) of a sampled, time varying, quantity V(nT) is defined by:

$$V(z) = \sum_{n=0}^{\infty} V(nT).\, z^{-n} \quad (3)$$

where V(nT) = 0 for n < 0.

Thus if we have a quantity V '(nT), equal to V(nT) but delayed by m sampling periods, then:

$$V' = V((n-m)T) \quad (4)$$

The Z transform of V '(nT) is:

$$V'(z) = \sum_{n=0}^{\infty} V'(nT).\, z^{-n} \quad (5)$$

$$= \sum_{n=0}^{\infty} V((n-m)T).\, z^{-n}$$

$$= z^{-m} \sum_{n=0}^{\infty} V((n-m)T).\, z^{-(n-m)}$$

Putting $l = n - m$ we get:

$$V'(Z) = z^{-m} \sum_{l=-m}^{\infty} V(lt).z^{-l}$$

$$= z^{-m} \sum_{l=0}^{\infty} V(lt).z^{-l} \quad (6)$$

since V(lt) = 0 for $l < 0$.

$$\therefore V'(z) = z^{-m}V(z) \quad (7)$$

from the definition of the Z transform (3).

This relationship between the past and present values of the sampled quantity is of primary importance in digital filter theory.

If $V'(Z) = z^{-1}(z)$
it follows that $V(z) = zV'(z)$
and $V(nT) = V'((n+1)T)$

Thus multiplication by z in the Z domain represents advancing by a time T in the time domain, and Z is consequently known as the "unit advance operator". From the Laplace transform theory we know that advancing by a time T is equivalent to multiplying by e^{sT} in the complex frequency domain, and thus we can say:

$$z = e^{sT} \tag{8}$$

This is a very important relationship connecting the complex frequency and Z domains, since it enables us to correlate points on the Z-plane with points on the S-plane, and vice versa. This immediately gives us a method of designing digital filters in the frequency domain. The unique relationship between the S and Z-planes can be evolved quite easily.

1. Since e^{sT} is periodic, with period T, for the imaginary part of s, it follows that the whole of the Z-plane can be mapped onto that part of the S-plane lying between the bounds $-j\pi/T < s < +j\pi/T$. The mapping then repeats itself continuously, with period $2\pi T$, beyond these bounds. This is shown in Figure 2.

2. If s is purely imaginary, then we have

$$Z = e^{sT} \rightarrow e^{j\omega T} = \cos(\omega T) + j\sin(\omega T) \tag{9}$$

As ω varies, z maps itself onto the unit circle in the Z plane, since $\cos(\omega T) + j \sin(\omega T)$ is the equation of a circle of unit radius.

By substitution we can find that when $T = O$, then $z = 1 + jO$. When $T = \pi$, then $z = -1 + jO$, and when $T = \pm\pi/2$, then $z = O \pm j1$. This is also shown in Figure 2.

3. If s is real, then we have

$$z = e^{sT} \rightarrow e^{\alpha T} \text{ where } \alpha \text{ is real}$$

When $\alpha = O$ $\quad z = +1$
When $\alpha = -\infty$ $\quad z = O$
When $\alpha > O$ $\quad z > 1$

Thus the pole on the Z-plane will lie on the real axis in the right hand half of the plane. For stability ($\alpha < O$) the pole will lie inside the unit circle.

4. Generally, we have

$$z = e^{sT} = e^{(\alpha + j\omega)T} = e^{\alpha T}\cos(\omega T) + je^{\alpha T}\sin(\omega T) \tag{10}$$

As ωvaries, z maps onto the Z-plane in circles of radius $e^{\alpha T}$. Thus the left hand half of the S-plane ($\alpha < O$) maps itself into the inside of the unit circle ($e^{\alpha T} < 1$) in the Z-plane, and vice versa.

Application of the Z-Transform to Sampled Data Systems

Since the Z transform gives us a relationship between the past and present values of a sampled quantity, just as the Laplace transform gives us a relationship between a continuous signal and its derivatives, we may process the input/output relationships given previously into more convenient forms.

$$V_o = V_I - RCdV_o/dt \tag{1}$$
$$\text{and } V_o(nT) = V_I(nT) - aV_o(n-1)T \tag{2}$$

Applying the Laplace transform to (1) and the Z transform to (2), we obtain:

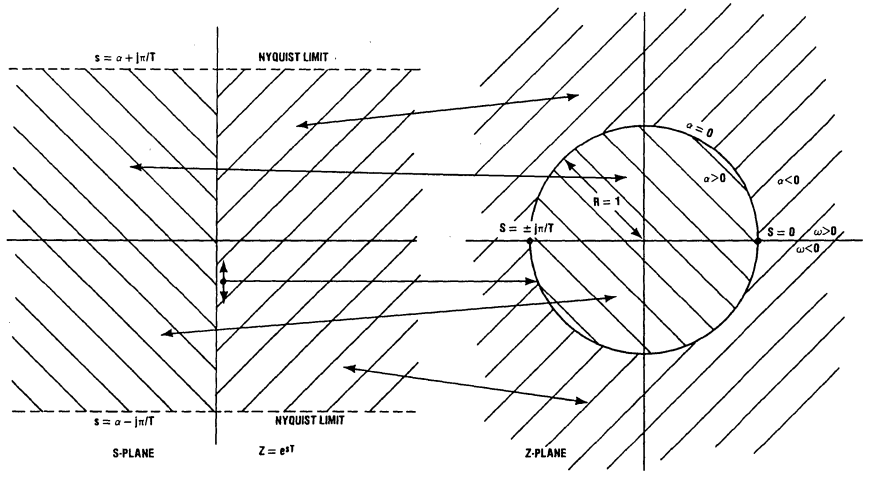
$$V_o(s) = V_I(s) - RCsV_o(s) \tag{11}$$
$$\text{and } V_o = V_I - az^{-1}V_o(z) \tag{12}$$

so that the appropriate transfer function may easily be obtained in both cases.

$$H(s) = \frac{V_o(s)}{V_I(s)} = \frac{1}{1 + RCs} \tag{13}$$

$$\text{and } H(z) = \frac{V_o(z)}{V_I(z)} = \frac{1}{1 + az^{-1}} \tag{14}$$

Figure 2.

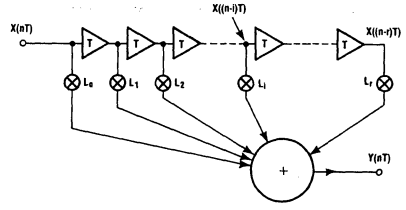


Realization of Digital Filters

The digital filter is made entirely of digital hardware. This may be special purpose hardware, wired to perform the filter function exclusively, or else it may be a general purpose digital processor programmed to perform the filter function.

The simplest form of digital filter is the transversal, or non-recursive, filter shown in Figure 3. In this filter the output is purely a function of past and present values of the input signal. No recursion of the output occurs. The filter consists of delay units (shift registers), multipliers, and summers. Theoretically the arithmetic would have an infinite word length, but in practice a word length of between 6 and 40 bits would be used.

Figure 3.



Consider the situation where all the shift registers contain zeros, and a single "1", i.e. a unit impulse, of unit amplitude and one clock period duration, is introduced at the input. The output level immediately becomes L_0, since the inputs to all the other multipliers are still zero. After the first shift pulse, the "1" moves to the output of the first shift stage, the input returns to zero, and the output level becomes L_1. It is easy to see that after consecutive shift pulses the output level becomes L_2, L_3, L_4 . . . . . L_r, and then returns to zero. Since the impulse response becomes zero after this finite period of time, non-recursive filters are also known as Finite Impulse Response (FIR) filters. This is illustrated (in an analog form) in Figure 4. The output of the filter for any input sequence is given by

$$Y(nT) = \sum_{i=0}^{r} L_i.X((n-i)T) \qquad (15.)$$

Applying the Z transform by multiplying each term by Z^{-n} and summing over n, we get

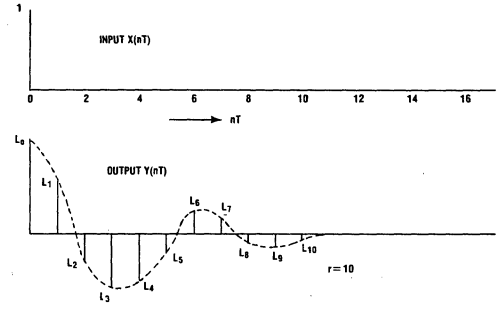
$$\sum_{n=0}^{\infty} Y(nT).z^{-n} = \sum_{n=0}^{\infty} \sum_{i=0}^{r} L_i.X((n-i)T).z^{-n}$$

$$\therefore \quad Y(z) = \sum_{i=0}^{r} L_i X(z) z^{-i} \qquad (16.)$$

$$\therefore \quad H(z) = \frac{Y(z)}{X(z)} = \sum_{i=0}^{r} L_i z^{-i}$$

which is the Z transfer function of the filter.

Figure 4.



If the output of this filter with the unit impulse input (after digital-to-analog conversion) is passed through a low-pass filter with a cutoff frequency of $\frac{1}{2}f_S$ (or 1/2T), the output waveform would be as shown in the dotted line in Figure 4. Since this output represents the response of the filter to an input impulse, H(z) is sometimes called the "impulse transfer function". Designing the filter by choosing the coefficients to give a certain time response is described in the section on design methods.

The non-recursive filter has only zeros in the Z-plane, and no poles, since it has no denominator polynomial. This greatly limits its performance since the length of its impulse response is determined exactly by the number of coefficients used, and a very large number is required to give the impulse response of most generally used filters, e.g. a filter with a Tchebycheff response. This limitation can be overcome by recursion of the output, as shown in Figure 5. The output of this filter is dependent on past values of the output, as well as past and present values of the input. The output is given by the following difference equation:

$$Y(nT) = \sum_{i=0}^{r} L_i.X((n-i)T) - \sum_{i=1}^{m} K_i.((n-i)T) \qquad (17.)$$

Summing over n, and applying the Z transform, we get:

$$\sum_{n=0}^{\infty} Y(nT)z^{-n} = \sum_{n=0}^{\infty} \left\{ \sum_{i=0}^{r} L_i.X((n-i)T)z^{-n} - \sum_{i=1}^{m} K_i.Y((n-i)T)z^{-n} \right\}$$

$$\therefore \quad Y(z) = \sum_{i=0}^{r} L_i.X(z).z^{-i} - \sum_{i=1}^{m} K_i Y(z).z^{-i}$$

$$\therefore \quad Y(z) \left\{ 1 + \sum_{i=1}^{m} K_i z^{-i} \right\} = X(z) \sum_{i=0}^{r} L_i z^{-i}$$

$$\therefore \quad H(z) = \frac{Y(z)}{X(z)} = \frac{\sum_{i=0}^{r} L_i z^{-i}}{1 + \sum_{i=1}^{m} K_i z^{-i}}$$

Figure 5.

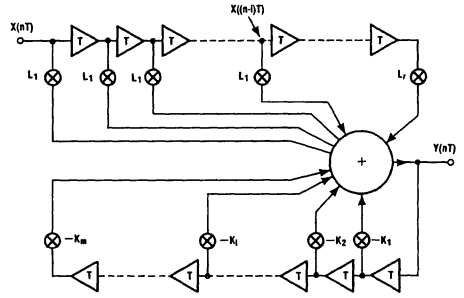
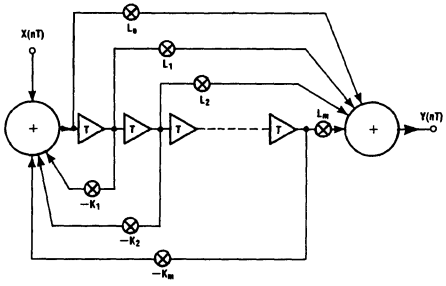


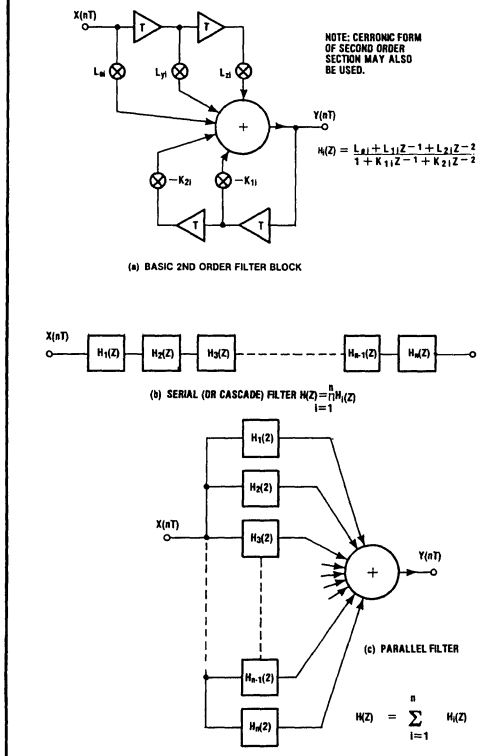
Figure 6.



This polynomial has both poles and zeros in the Z-plane, and thus is a general purpose function. Because of the recursion of the output, the filter theoretically has an infinitely long impulse response, and consequently recursive filters are also known as Infinite Impulse Response (IIR) filters. In practice it will be of finite duration, the length depending on the word length of the arithmetic.

The form of the filter shown in Figure 5 is the basic form. This can be reduced to the canonic form shown in Figure 6, with a great reduction in the number of delay elements required. This reduction will be maximum when the numerator and denominator have the same number of coefficients, when every delay unit will be used twice. The canonic and basic (or direct) forms of the filter are not often used. Since it is possible to factorize the transfer function into either quadratic factors or partial fractions, it is possible to realize the digital filter in the serial (or cascade) and

Figure 7.

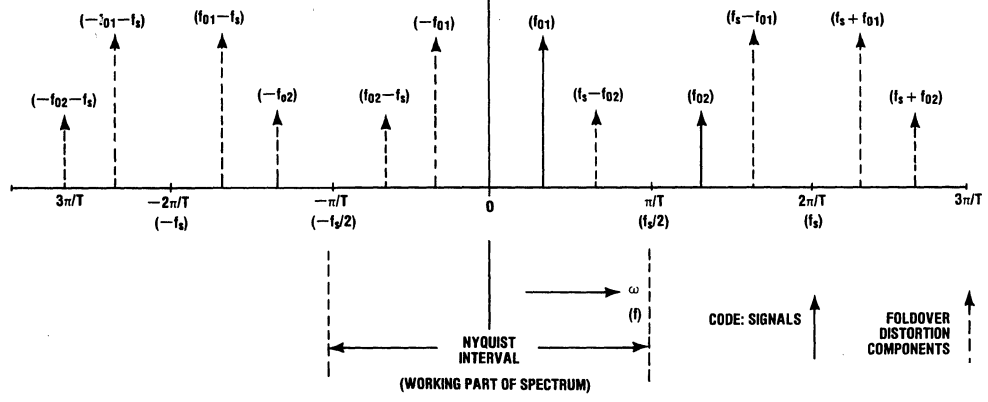


parallel forms respectively. These are shown in Figure 7. It has been shown by many workers (5) in the field that the serial and parallel forms offer far greater accuracy and lower noise levels than the direct and canonic forms, the improvements gained being a monotonic function of the order of the filter. Thus the serial and parallel forms can be realized with shorter word lengths than the direct and canonic forms, and still maintain the same performance. This results in a great saving in the hardware required for realization.

Limitations of Digital Filters

Since digital filters are sampled, or discrete time, networks, the input signals must obey the Nyquist criterion, i.e. the highest frequency present must not exceed half the sampling frequency. Failure to observe this fact will result in foldover distortion of the output signal. This is a consequence of the fact that when a signal at frequency f_0 is sampled at a frequency f_s, then the resultant signal contains components at the frequencies $(nf_s \pm f_0)$ for all real values of n, both negative and positive. The most significant component, apart from the one corresponding to $n = 0$, is f_s-f_0. It is clear that if $f_0 > \frac{1}{2}f_s$ then $(f_s\text{-}f_0) < \frac{1}{2}f_s$, so that the distortion component may enter into the working part of the spectrum of the system. This is illustrated in Figure 8.

Figure 8.



The Gain of a digital filter. The generalized form of the Z transfer function

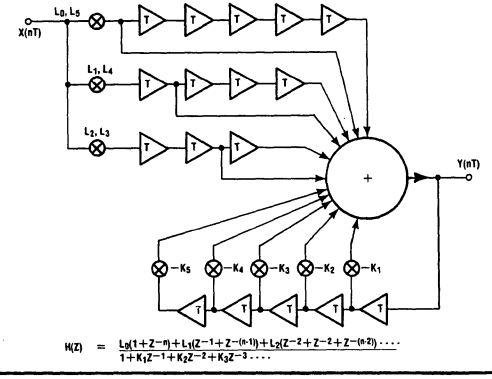
$$H(Z) = \frac{\sum_{i=0}^{r} L_i z^{-i}}{1 + \sum_{i=1}^{m} K_i z^{-i}} \qquad (18.)$$

will have an in-band gain that may well differ from unity, just as in the case of the analog filter. The gain of the filter may be varied at will by altering the numerator coefficients proportionally. It is important that the denominator coefficients are not altered, however, since K_0 must be unity if no recursion of the now value of the output is to be used. If the gain of the filter is not critical, the numerator coefficients may be normalized by dividing them all by L_o. The transfer function then becomes

$$H(Z) = \frac{1 + \sum_{i=1}^{r} L_i z^{-i}}{1 + \sum_{i=1}^{m} K_i z^{-i}} \qquad (19.)$$

The gain of the generalized filter will be L_0 times the gain of the normalized one. Normalization has the advantage that one multiplier may be eliminated. In the case of serial and parallel filters this means one per block, so that in a 2Nth order filter, N multipliers are eliminated. However, care must be taken to ensure that overflow of the arithmetic does not occur, by proper scaling of the signal between sections.

Figure 9. Alternative Arrangement for Mirror-Image Numerator Polynomial



Special cases. Two special cases are worthy of mention here.

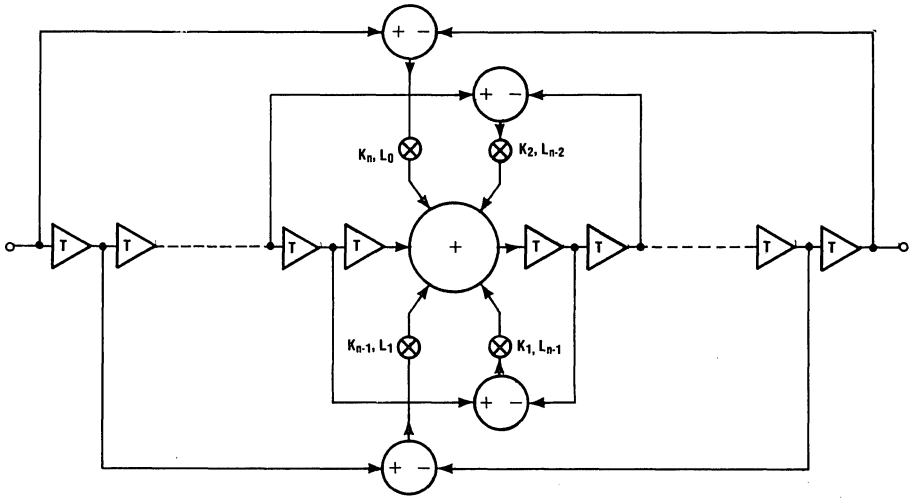
1. Mirror image polynomials. Certain classes of filters, including elliptic filters, will yield mirror image numerator polynomials. This enables the number of numerator multipliers needed to be reduced by half by using the method shown in Figure 9. If the filter is made of serial or parallel second order blocks which have normalized numerator coefficients ($L_0 = 1$), then since $L_2 = L_0$, only 3 multipliers are needed to realize a second order block, instead of the usual five.

2. All-pass structures. Phase shift correction networks of an all-pass nature are characterized by the relationship

$$L_i = K_{N-i} \qquad (20.)$$

where N is the order of the filter. The numerator polynomial will always be of the same order as the denominator polynomial in this class of filters. This relationship enables the number of multipliers required to be halved by using the method shown in Figure 10.

Figure 10. Alternative Arrangement for All-Pass Network



$$H(Z) = \frac{L_0+L_1Z^{-1}+L_2Z^{-2}\cdots+Z^{-n}}{1+L_{n-1}Z^{-1}+L_{n-2}Z^{-2}\cdots L_0Z^{-n}}$$

Overflow Oscillations

It has been shown that under certain circumstances, digital filters are unstable due to the nonlinear overflow characteristics of the arithmetic unit. The characteristic of two's complement arithmetic is shown in Figure 11 (a). It has been shown that the criterion for unconditional stability for a filter made with such an arithmetic unit is

$$|K_1| + |K_2| < 1$$

which is rather restrictive on the locations of the poles of the filter. An alternative, and more satisfactory, method of preventing overflow oscillations is to cause the arithmetic to "saturate" in the overflow condition. Perfect saturation is illustrated in Figure 11 (b), but it has been shown that any saturation characteristic which lies in the shaded area will give unconditional stability. Note that it is not necessary (nor desirable) to cause every part of the summer block to saturate on overflow, since overflow capability of the intermediate summations is desirable with two's complement arithmetic. The only point at which overflow saturation is necessary is after the final summation.

Design Methods for Digital Filters

There are several methods available for designing digital filters. Briefly, they are as follows.

1. **Impulse invariance.** The Z transfer function of a digital filter is also known as the "impulse transfer function". Thus, if the impulse response of the digital filter is made to be equal to the sampled impulse response of the desired filter, then the digital filter will be the one required. However, it must be emphasized that foldover distortion of the characteristic occurs at the Nyquist frequency. It is therefore necessary to choose a response which has a negligible magnitude above the Nyquist frequency so that the distortion will also be negligible. Clearly this technique is very easily applied to transversal filters, but techniques are also available for designing recursive filters by this method.

2. **Direct synthesis from the squared magnitude function.** Analog filters are designed by choosing a suitable squared magnitude function, e.g. a Butterworth characteristic is based on the function

$$|H(j\omega)|^2 = \frac{1}{1+(\omega/\omega_c)^{2n}} \qquad (21.)$$

Suitable functions can also be found for the simple synthesis of digital filters. Such a function is

$$\left|H(z)\right|^2_{z=e^{j\omega T}} = \frac{1}{1+\dfrac{\tan^{2n}(\omega T/2)}{\tan^{2n}(\omega_c T/2)}} \qquad (22.)$$

This function is similar to the Butterworth function and transforms into a function of z very simply.

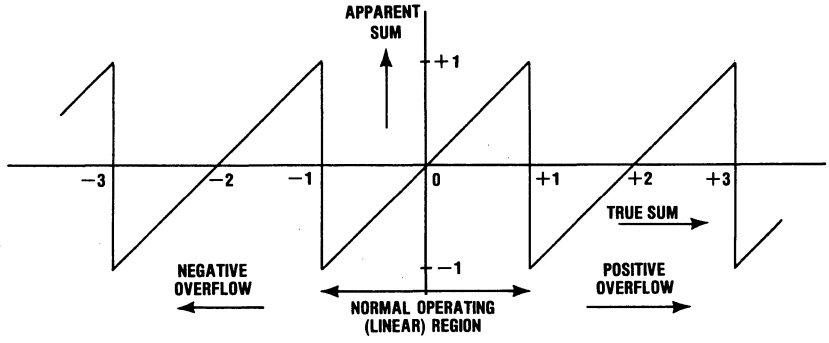
If other squared magnitude functions are desired, such as Tchebycheff or Elliptic functions, then the simplicity of transformation is lost. A technique is available, however, for designing Tchebycheff and Elliptic filters when the order is 2^N (for integer values of N). This technique is based on a telescoping process, starting with the relatively simple second order function and relating higher order functions to this by the relationship[6], [7].

$$P_{2(r+1)}(\omega) = P_2\{P_2(\omega, \gamma_r, \tau_r), \gamma_{r+1}, \tau_{r+1}\} \qquad (21.)$$

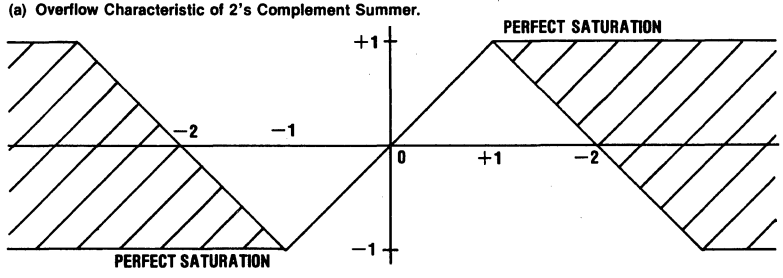
where $P_2(\omega, \gamma_2, \tau_2)$ is a 2nd order Elliptic function, the Tchebycheff function being a special case of this.

In all other cases the complexity of the problem is such that it is easier to use other methods, such as method 3.

Figure 11.



(a) Overflow Characteristic of 2's Complement Summer.



(b) Perfect Saturation Characteristic and Stable Overflow Region (Shaded)

3. **Indirect synthesis by the bilinear transformation of a continuous filter function.** Since continuous (analog) filter design techniques have been developed to a very high degree of sophistication, it seems sensible to use these techniques to design the required filter in the s-plane, and then transform this into the z-plane. Apart from the fact that the transformation $z = e^{sT}$ is difficult to apply, it was noted earlier that foldover distortion of the response occurs if the characteristic has a significant magnitude above the Nyquist frequency. Both these problems may be overcome if another transformation is used. This transformation should map the entire $j\omega$ axis of the s-plane onto the unit circle in the z-plane, thus eliminating the foldover distortion. Such a transformation is the "bilinear transformation":[4]

$$s = \frac{2}{T} \frac{(1 - z^{-1})}{(1 + z^{-1})} \tag{22.}$$

together with its inverse form

$$z^{-1} = \frac{(1 - sT/2)}{(1 + sT/2)} \tag{23.}$$

This transformation is very easy to apply, and always results in a function in which the order of the numerator polynomial is the same as the order of the denominator polynomial. It is important to realize that since this transformation warps the characteristic of the filter along the ω axis, the desired characteristic should be prewarped in the reverse order to compensate for this. The warping is a tangential function

$$\omega = \frac{2}{T} \tan \left\{ \frac{(\omega T)}{2} \right\} \tag{24.}$$

where ω is a point on the real frequency scale, and ω_1 is the corresponding point on the warped frequency scale. This is illustrated in Figure 12.

The prewarping is achieved by replacing all points ω by ω_1, according to the relationship:

$$\omega_1 = \frac{2}{T} \arctan \left\{ \frac{(\omega T)}{2} \right\} \tag{25.}$$

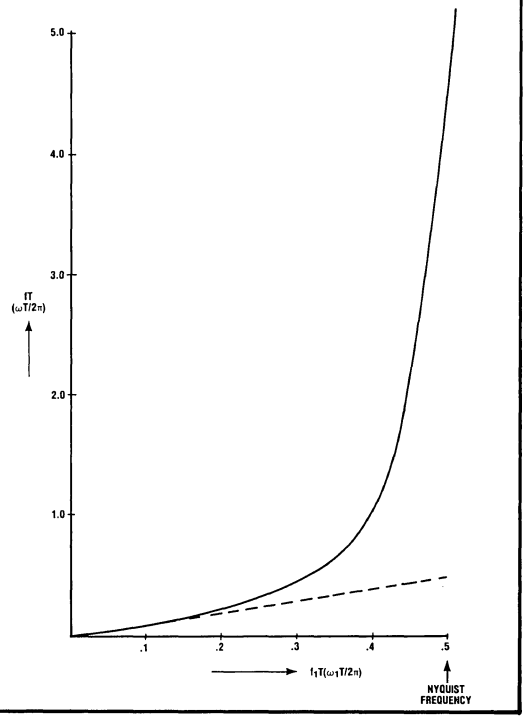
The analog filter is then designed using these values of ω_1, and the correct digital filter will be obtained by using the bilinear transformation on the S transfer function.

In the simple cases of high-pass or low-pass filters where there is only one critical frequency, e.g. the cutoff frequency, the prewarping of the characteristic may be avoided by the use of the prewarped bilinear transformation[8].

$$s = \Omega_c . \cot \frac{(\omega_c T)}{2} \cdot \frac{(1 - z^{-1})}{(1 + z^{-1})} \tag{26.}$$

where Ω_c is the cutoff frequency of the linear filter (often normalized), ω_c is the desired cutoff frequency of the digital filter and T is the sampling period.

Figure 12.



This transformation will automatically put the one critical point (taken here to be the cutoff frequency) at the correct frequency, but it is very important to realize that, except for zero frequency, no other point on the frequency scale of the digital filter characteristic will correspond to the equivalent point on the analog filter characteristic. From this it follows that the transition ratio of the digital filter will be less than that of the original analog filter, i.e. the cutoff will be sharper. This is a bonus obtained at the expense of the warping of the frequency scale whenever the bilinear transformation is used. Further, the improvement of the transition ratio will increase with the cutoff frequency, the transition ratio reducing to zero when the cutoff frequency is equal to the Nyquist frequency. The variation of the transition ratio with the cutoff frequency follows the law:[9]

$$\tau = \frac{T\,\omega_c}{2 \arctan \left\{ \tan\left[\frac{\pi}{4\,\tau_o}\right] \cdot \tan\left[\frac{\omega_c T}{2}\right] \right\}} \qquad (27.)$$

where ω_c is the cutoff frequency

- T is the sampling period
- τ is the transition ratio
- τ_o is the transition ratio when the cutoff frequency is half the Nyquist frequency.

4. Design of arbitrary filter characteristics by optimization. Numerous techniques exist for the direct synthesis of digital filters by optimization. For example, FIR filters may be designed very quickly by the Parks and McClellan technique[11], using the Remez exchange algorithm. Similar techniques have also been developed for IIR filters[12]. In most cases the process can be speeded up by using a suitable model, or approximation, to the desired characteristic as a starting point for the optimization program.

Summary

There are four methods available for designing digital filters.

1. Impulse invariance. Limited to responses which have a negligible magnitude above the Nyquist frequency, sometimes difficult to apply.
2. Direct synthesis. Can be used successfully if a suitable squared magnitude function is available. Otherwise only really applicable when the order of the filter is 2^N.
3. Indirect synthesis. Probably the most useful general technique available.
4. Frequency sampling. Rather limited in the frequency responses that can be generated.

The four methods have been described very briefly here, this serving mainly to enable the user to choose the most suitable method for the problem in hand. A more detailed description can be found in the appropriate papers, and also in Chapter 3 of "Digital Processing of Signals" (Gold and Rader).

Appendix I. Internal Overflow in Digital Filters.

It is quite possible for internal overflow to occur in a digital filter arithmetic unit even though the input level is such that the output should be within the working range of the unit. This is completely analogous to the case of L-C filters, where the voltages across individual components often exceed the input and output voltages by very large amounts. Overflow is permissible in the partial sums of the summing unit when a code such as two's complement arithmetic is used, but overflow before or in the multipliers will have disasterous results on the output signal. Consider the second order filter block shown in Figure A1. Its transfer function is:

$$H(z) = \frac{L_0 + L_1 z^{-1} + L_2 z^{-2}}{1 + K_1 z^{-1} + K_2 z^{-2}}$$

since K_0 has been normalized. The filter will have a gain factor, which may be greater or less than unity, but the worst case for overflow is when the gain is unity. In that case let us assume that both the input and output levels are N bits peak amplitude (referred to the quantization level). Thus we may say that the peak signal levels at points A, B, C, D, E and F in the system will also be N bits. The signal levels at the other points in the system will be dependent on the multiplier coefficients, and can be specified in certain special cases.

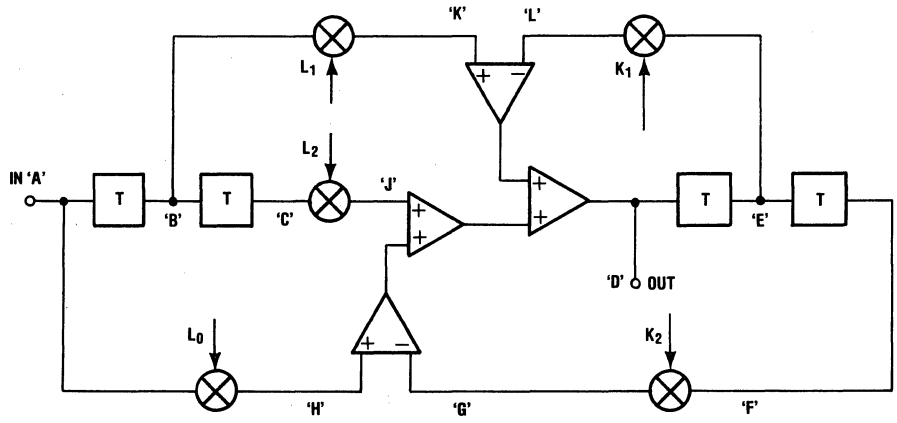
(a) Normalized Mirror Image Polynomial Filters.

Filters having purely imaginary zeroes in the S-plane (or zeroes lying on the unit circle in the Z-plane) have mirror image polynomial (M.I.P.) numerators. Thus if we normalize the numerator coefficients in Figure A1, so as to make $L_0 = 1$, then we have $L_2 = 1$ also, so that:

$$H(Z) = \frac{1 + L_1 z^{-1} + z^{-2}}{1 + K_1 z^{-1} + K_2 z^{-2}}$$

In this case it can be shown that $|L_1| \leq 2$, $|K_1| < 2$, and $|K_2| < 1$. Thus at points G, H and J the peak signal levels will be N bits, and at points K and L the peak signal levels will be N + 1 bits. At the partial summation nodes the peak signal level will exceed this, but since overflow is permissible at these points it is of no consequence. Therefore, in order to be able to handle input or

Figure A1.



output levels (whichever is the greater) of N bits peak, the internal arithmetic must be able to process a level of N + 1 bits.

(b) **Normalized All-Pass Networks**

In the case of normalized all-pass networks having unity gain, it can be shown that the numerator coefficients (starting at L_0) are equal to the denominator coefficients in reverse order (starting at K_n, in an nth order section).

$$\text{i.e. } L_i = K_{n-i}$$

Thus in Figure A1 we can say that

$$L_0 = K_2,\ L_1 = K_1, \text{ and } L_2 = K_0 = 1$$

We may also state that $|K_1| < 2$ and $|K_2| < 1$, so that $|L_1| < 2$ and $|L_0| < 1$.

Thus at points G, H and J the peak signal levels will be N bits, and at points K and L the peak signal levels will be N + 1 bits, so that the same conditions hold as in the M.I.P. filters.

(c) **General Case**

Let L be the greatest in absolute magnitude of L_0, L_1, L_2
Let K be the greatest in absolute magnitude of K_1, K_2
Let A be the maximum gain of the filter.
Let x and y be such that:

$$2^{x-1} \leqslant L < 2^x \text{ and } . \ 2^{y-1} \leqslant K \ . \ A < 2^y$$

Referring to Figure A1, we may state that the greatest peak signal level at points H, J, and K (but only necessarily at one of them) will be N + x bits, and at points G and L (but only necessarily at one of them) the greatest peak signal level will be N + y bits. Thus in order to be able to handle these signals, the arithmetic must be able to process N + x or N + y bits, whichever is the greater.

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AMERICAN MICROSYSTEMS, INC.

AA 603

SCAR II, switched-capacitor filter analysis and optimization software

SCAR II

Switched-Capacitor Filter Analysis and Optimization Software

AMI Communications Engineering possesses a very sophisticated method of analyzing and optimizing switched-capacitor filter circuits. It is called the Switched-Capacitor Analysis Routine II, more commonly called SCAR II.

The SCAR II program expands on the offerings of an earlier program called SCAR I, jointly developed by AMI and UCLA. An important difference is that SCAR II not only analyzes a circuit for given component values, but also **optimizes** a design by changing the element values in the direction of the frequency response specified.

SCAR evolved from the need for a tool capable of aiding in switched-capacitor filter designs, a new MOS filter technique. In Telecommunications, most circuits use a filter. To understand the relationship between SCAR and filters, here is a brief description of filters and their switched-capacitor equivalents.

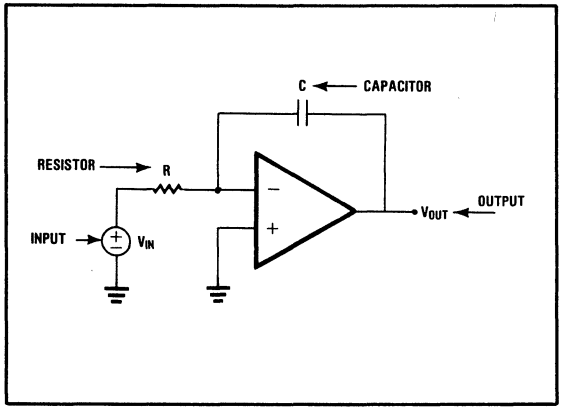
What is a Filter

An electrical signal going into a circuit consists of an infinite number of frequency components. A filter selects the desired portion of frequency content from a signal meeting the specified requirements and rejects the rest. For example, when you tune your radio, what you are basically doing is changing the filter to find the frequency. Once the frequency is found, all other channels are rejected.

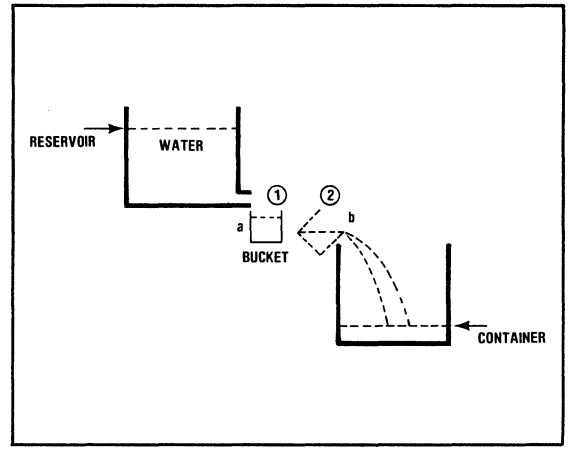
Older filters consisted of capacitors, inductors and resistors. However, the absolute value of resistors and capacitors on silicon cannot be accurately controlled. To remedy this problem, three years ago AMI designed an MOS switched-capacitor filter made of op amps, capacitors and switches. To achieve the required accuracy in value, we used ratioed capacitors. The ratio of two capacitors is accurately controllable because the size of two capacitors remains proportionate in individual IC's. The net effect of putting a signal into a switched-capacitor filter is the same as putting the signal through a filter built from capacitors, inductors and resistors, with the advantage that the filter can be fabricated complete on silicon.

The following is an illustrated comparison between the older filter and the switched-capacitor filter.

A Simple R-C Active First Order Filter

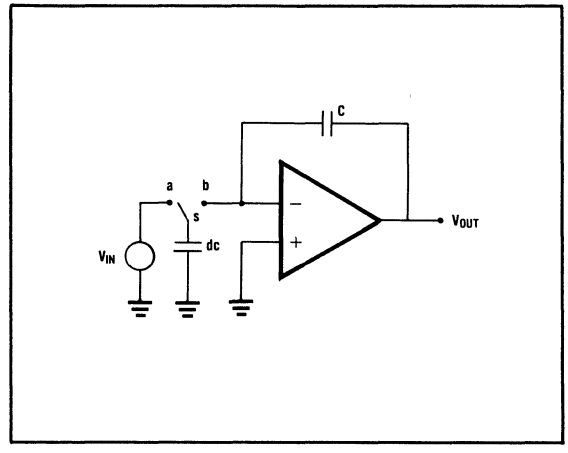


The capacitor C is charged by the input voltage source through R. The input voltage source can be considered as a water reservoir that fills an empty container (Capacitor C) through a valve (Resistor R) that controls the water flow (see below).



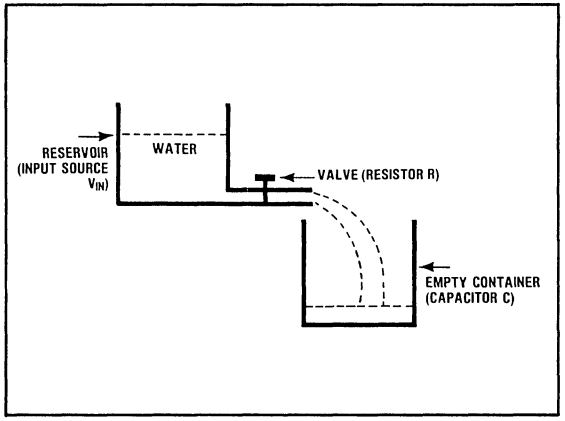
Switched Capacitor Filter

The figure below depicts the switched-capacitor version of the above circuit.



A two-phase clock periodically controls circuit operation. In the first-**half** period the switch "S" is thrown to point "A" and capacitor C is charged to the input voltage. In the **second**-half period switch "S" is connected to point "B" and the charge on capacitor dc is transferred to capacitor "C". This process repeats periodically. Once again, the input source can be assumed as a reservoir and the capacitor "C" as an empty container (see

below). The hose and valve, however, are replaced by a bucket. First the bucket fills with water from the reservoir, then empties into the container.



If this process is repeated periodically at a fast rate, in time it can be assumed there is a continuous flow of water into the container. The water level in the container, however, changes discretely as opposed to the continuous flow in the simple filter.

A designer needs to know how to design a required filter. How does one combine the op amps, capacitors and switches? How does one determine the capacitor ratios to achieve the required frequency response? Finding the answers to these basic questions and the right switched-capacitor filter component values requires using SCAR II.

SCAR II's Capabilities

SCAR II analyzes and optimizes characteristics of a filter, but it also performs noise analysis. Noise (static) is an undesirable source within a circuit other than the signal source causing the output to change. This noise arises from circuit elements inside the chip. In a given system, the output noise level is specified, and the circuit should not create more noise than it is allowed. SCAR II is capable of telling the engineer how much noise will appear at the output.

SCAR II also performs a sensitivity analysis, i.e., if a given component is varied by so many percents, SCAR tells how much the frequency response varies and whether the filter will meet the specifications.

Using SCAR II makes a circuit perform better from the very beginning so tweaking does not have to be done at design end. It gives a very solid prediction of how the circuit will behave and lets the engineer know that when the circuit reaches completion, it will work to specification.

AMERICAN MICROSYSTEMS, INC.

AA 701

Rationale for custom integrated circuits

by D. Schare

Rationale for custom integrated circuits

***D. Schare* looks at custom designed and manufactured integrated circuits**

Products tailor-made to our personal requirements have become so expensive, it seems, that they are a thing of the past in most spheres of our lives. However, a stable and significant portion of the semiconductor industry thrives by designing and manufacturing custom integrated circuits. Such circuits constantly push the state of the art for functional density, speed/power ratios, and other parameters; yet they remain economically competitive with standard, mass-produced devices.

Custom metal oxide semiconductor/large-scale integrated (MOS/LSI) circuits are rarely adaptations of existing designs. Instead they arise as unique engineering solutions to control, digital processing, data manipulation, sensor interpretation, input-output and other design problems. With catalogues from semiconductor manufacturers listing pages of standard, off-the-shelf ICs, the question remains: Why is it necessary or desirable to custom-design an integrated circuit?

Application of custom IC

A custom IC made the handheld calculator feasible. From that custom genesis, the pocket calculator has grown into a ubiquity. Another common item is the smoke detector. Large and expensive smoke detectors existed earlier; custom circuits reduced their size, power requirements and price dramatically, and made them common. The same is true for digital watches. Had they been made with standard small-scale integrated (SSI) or medium-scale integrated (MSI) microcircuits, they would have emerged the size of a clock. MOS/LSI made them as small as their mechanical counterparts and as accurate as a ship's chronometer.

Custom circuits have permitted design of somewhat exotic but highly useful products. Datotek, a small firm in Dallas, has designed probably the most compact, sophisticated cryptographic device ever made, through use of a custom IC. The custom chip incorporates the electronics of three printed circuit boards. Combined with a microprocessor, the circuit creates a pocket calculator-sized device that generates 10^{52} different codes, assuring secure communications. Travelling executives use Datotek's machine for encoding and decoding messages requiring privacy of the correspondence with their headquarters.

Analogous to the arithmetic unit in a computer, the custom chip performs the key code-generation function. It produces a "semi-infinite" pseudo-random key stream 10^{65} bits long when commanded to by the microprocessor.

Datotek considered at least two other approaches before settling on the custom development program. A wholly microprocessor-based design could have performed the key generation function in software, but would not have been as secure. Moreover, the complexity of the custom coding hardware could not have been achieved. A hybrid approach with 100 MSI chips divided into 10 packages of 10 circuits each, all bonded on the substrate, was also considered. The company's engineers determined that it would have been cost prohibitive and resulted in much poorer reliability.

Ability to compete in an existing market establishes another reason to go custom. Courier Terminal Systems, Inc., headquartered in Tempe, Arizona, engages in manufacturing and selling IBM-compatible terminals, one of the most fiercely competitive areas in the EDP market. Courier employs custom circuits as a means to compete. Expanding beyond off-the-shelf electronics helps the firm keep the performance of its products equal to those of much larger vendors with much greater resources. The latest version of its Courier 270 Information Display System uses two new custom circuits. One, an I/O device, replaced an 18-chip TTL (transistor-transistor logic) arrangement of MSI and SSI. This substitution led to higher reliability and lower power consumption, and decreased sparing, maintenance and assembly costs. Board space opened up to add features, though hardware costs remained about the same. The custom circuits produced an unsought benefit in the final design — the smaller power supply size had a smaller magnetic field and required no costly shielding.

Both chips are 40-pin, NMOS, silicon gate, depletion load chips. The I/O device, essentially a specialised UART (Universal Asynchronous Receiver-Transmitter), handles the receipt of formatted data and the transmission of raw data to the appropriate portion of the system — terminal, controller, or printer — as dictated by the systems microprocessor. Both chips are used in several systems manufactured by Courier, to provide intrasystem compatibility.

In car chip

Ford Motor Company is another firm that has gone the custom route to achieve size reductions, greater reliability and smaller costs. For its Lincoln Continental Mark IV the company designed a PMOS chip measuring 221-mils square and containing approximately 3600 transistors. The device forms the primary system component in the car's "miles-to-empty" feature which estimates how many miles can be driven before running out of gas. It also tells the miles per gallon usage rate. The central reason for custom was to minimise size. The MTE had to fit inside the instrument cluster. Building the same module with standard ICs would have required about 100 circuits. Microprocessors could not be used because they require peripheral circuits that would have made the system design more expensive and less reliable.

Some users of custom circuits find themselves having absolutely no alternative. A pacemaker manufacturer, for instance. Though low volume (where other custom using products tend to be high-volume), the pacemaker must be both compact as possible and extraordinarily reliable. Custom LSI is virtually the

The author is with American Microsystems Inc, California

only possible solution for these design necessities.

In general, there are three major market areas for custom microcircuits: 1) electronic data processing and control systems, including business equipment, calculators, terminals, word processors, and computers with moderate production volumes and long life; 2) consumer products such as entertainment and music systems, security devices, automotive electronics, appliances and games (products made in high volumes over shorter lifetimes than the first category) and 3) telecommunications products, such as codecs, switches and signal processors for central offices and PBXs (with long design cycles and long lives).

Reasons for custom

The chief reason is clearly economic. By incorporating many functions onto one silicon chip, custom circuits reduce part counts. Reduced part count lowers costs of test, assembly, handling and labour. Reliability increases with fewer parts and interconnections. Space is saved, and materials for the product itself are reduced. Power dissipation diminishes and with it the size of the power supply subsystem. Heating problems and cooling requirements may be eliminated; and finally, the cost to troubleshoot or maintain a system comes down.

A system designed by GTE Automatic Electric Inc., the equipment arm of General Telephone, provides an example. By using a 132 by 129 mil, CMOS-technology custom chip mounted in an 18-pin package, the company reduced the number of printed circuit cards in its coin-operated telephones from three to one. The simpler system made for easier, faster installation of the phones by giving more convenient access to mounting bolts. Performance advantages, such as ability to change base rates by throwing tiny toggle switches, made it possible to ship phones fully assembled, in smaller boxes, and at a saving in shipping costs.

The very existence of some products demonstrates the space advantages from the incredible "shrinking" capability of custom MOS/LSI circuits.

Cost of a custom program

Since the point of custom integrated circuit use is to reduce product costs while retaining or enhancing product performance, circuit cost is extremely important. Semiconductor manufacturers base MOS/LSI circuit prices on development program costs, design complexity, chip size, fabrication technology, package type and testing requirements. Prices are generally negotiated individually by circuit or circuit set.

Since the costs of circuit development must be pro-rated over the production volume and contract life, generally volumes of about 20,000 circuits are the smallest feasible for custom circuits, where the manufacturer both designs and fabricates the chips. There is an important exception which will be discussed later.

Whether the semiconductor manufacturer can afford to invest the engineering resources in the program for a given volume will determine a custom program's feasibility. For a simple circuit, the required engineering may be relatively little and straightforward; for a complex circuit, the needed manpower may be great, the engineers highly skilled and the time long. Circuit complexity impacts other cost factors significantly — chip size, production yield, testing demands and packaging.

Circuit complexity and benefits from it are constantly increasing. In 1970, AMI designed chips with a maximum of 350 transistors. By 1980, there will be 30,000 or more transistors on custom circuits. More transistors means more functions in a single package, greater reliability in a finished product and lower costs for assembly, power supply, cases, shipping and related items. But greater complexity also means that higher custom circuit development, checkout and testing costs must be amortised in production.

For standard integrated circuits such costs are distributed among all customers for a circuit. For custom circuits, one company bears the full burden — except where the circuit has a general use and the company allows the semiconductor manufacturer to market the device as a standard product. (This is sometimes done, with the customer company forbidding sale to producers of a competing end product.)

The exception to the volume-versus-development-cost tradeoff arises where the customer company performs its own design work. Some companies have developed this kind of in-house expertise or they hire third-party designers to do the work for them. Such an approach to custom requires the designer to know the semiconductor manufacturer's fabrication technologies and design rules, but it is not uncommon for some companies to use this means of developing circuits. One company that makes aircraft electronics regularly engineers its own circuits in order to make manufacture in relatively low volumes (usually about 5000 each) attractive to semiconductor companies. The company delivers "tooling tapes", magnetic tapes with the complete circuit in digital data form, to AMI for conversion into the photolithographic masks used to make the silicon wafers that each contain up to several hundred of the complete circuits. Singer, the sewing machine manufacturer, also uses this approach as a way of protecting design secrecy. As product design sophistication increases, work of this kind (called "customer tooling" at AMI) has become sufficiently important for AMI to establish a special Customer Tooling Department. This department advises users on our technologies, design rules and special requirements, arranges conversion of tapes from non-compatible formats and manages the customer's circuit production.

Chip size

After production volume, chip size becomes the important consideration. Yield — i.e., the number of finished circuits on a silicon wafer that pass all the electrical tests — emerges statistically as inversely proportional to the size of the chip. The larger the circuit, the fewer there are on a wafer. Random defects that can ruin a circuit occur in a fixed number per square inch. The bigger the circuit, the higher the probability that a randomly distributed defect will occur in it. Those factors — fewer chips per wafer, higher probability of defects in big chips — lower the yield and make circuit size extremely important.

Costs turn out to be proportional to the cube of die or chip area — a die with twice the size of another will cost eight times as much to manufacture. As a result, circuit designers pay extraordinary attention to achieving high circuit densities, narrow line and element spacings and small final circuit sizes. Most of the work must be done by hand; however, AMI also uses a very sophisticated Interactive Design System which permits engineers to lay circuits out using a colour CRT termi-

nal and a computer. The IDS shortens the time required to design circuits, checks them for accuracy and function immediately and reduces the overall design time and cost.

Packaging also plays an important role in cost calculation. Plastic and ceramic dual in-line packages are the most common. Plastic is the lowest cost, but it does not provide the environmental protection of ceramic. Ceramic packages cost up to $2.00 each for a 40-pin size, and represent a substantial part of the integrated circuit's final cost. For this reason, rigorous tests must cull out bad circuits before they are ever packaged.

In summary on costs, to get a reliable estimate, a custom circuit user must provide the semiconductor manufacturer the system and electrical specifications of the end product, a logic diagram of the circuit (if possible) and should indicate all power supplies, inputs, outputs, speed requirements and special circuits, critical paths or conditions. These should be accompanied by planned production volume information and packaging needs. If you need help, contact a custom manufacturer early for assistance in preparing your request.

Microprocessor against custom logic

Microprocessors provide the flexibility of software alteration that custom chips often cannot or are not intended to have. Many manufacturers design products with microprocessors, to prove product concepts, establish market position or develop a market, and then switch to custom circuits for economical volume production. Often, the microprocessor overkills the design requirements, wasting power and cost.

Once a design is successful and performance and program criteria become fixed, available cost savings justify a custom development program.

Courier, mentioned earlier, often introduces a new product with a standard circuit, discovers any problems and buys valuable learning time, before allocating the engineering resources to the task of developing a custom circuit.

A substantial degree of flexibility can be incorporated in a custom chip as well as with microprocessors. It is harder to copy a hardware design than it is a software one, a factor which protects a custom product's head start in the market. To achieve that custom flexibility, a portion of the chip may be dedicated to an erasable/programmable ROM memory, which can be reprogrammed at a later time. Or, the on-chip ROM can contain many different programs or patterns. One computer terminal maker includes scores of fonts and formats in its keyboard encoder, but implements only special ones for each product.

Upgrade features that are planned and included can be accessed by selective pin connections. Tel-Tone Corp., a supplier of electronic and tone oriented communications equipment, designed one set of custom chips for several products. The company added "downbond" options permitting selection of 40 out of 42 internal connections to IC package leads. Different pin combinations enable alternative product applications.

Judicious combination of functions in a custom circuit can extend its production life. Dacom, Inc., a facsimile equipment manufacturer, has used the same set of custom circuits, to perform essential data compression and reconstruction functions in its products since 1973; yet their product line has expanded from one product to several and all are state of the art units. The company has added some interface circuits to its products over the years, but the original custom circuits continue to sustain ever higher performance levels.

Risks in custom development

Developing a custom chip involves risks similar to those encountered in the development of any new, complex product. Schedules sometimes slip, for a variety of reasons. Although most of the chips produced work correctly the first time, many do not. Even wrong ones often have enough functions working correctly to allow the customer to debug his system. The correction sequence usually requires six to eight weeks. Problems do occur in designs entailing thousands of lines placed in a small area. Human errors creep in similar to typographical errors that evade an army of proof readers. Sophisticated methods are used to screen them out. Computerised logic, design rule and adjacency checking, for example. Still, if the designer corrects the only four ways a problem can occur, Murphy's law says, a fifth way often arises.

As a further guard against error, a breadboard is generally desirable for all new designs. Two types of breadboards are used — chip emulators and functional emulators. Chip emulators more closely approximate a gate-for-gate equivalent of the chip. They show whether the final logic is correct and actually plug into the chip socket for system debugging. An emulator can be used to fully check chip features before committing the design to silicon.

Custom development program

A program to develop a custom circuit involves four major phases and several steps in a sequence that can take from 20 to 40 weeks. The four phases include: 1) system definition and logic design; 2) chip circuit design, simulation, and test program generation; 3) mask fabrication, wafer fab, prototypes, and customer approval; and finally, 4) production.

System definition requires the user to supply the circuit designer an electrical specification and circuit description. The circuit designer develops a logic design. Using customer-supplied logic-exercise vectors, a computer program simulates the logic. A customer must approve the logic simulation before circuit design begins.

The first step in design is preparation of a composite plan at a scale of 100:1 for customer review of the chip pinouts. Once approved, the layout is digitised to convert geometrical patterns to digital data, which are processed to provide a "pattern generation tape". Once the customer provides the final test vectors, working photolithographic masks are made from the tapes, and wafer fabrication commences. The manufacturer performs tests to evaluate wafers, die and packaged chips and any reliability steps are taken, prior to shipment to the customers.

Future uses of custom

Custom circuits will continue to play an important part in systems design, alongside microprocessors and standard parts.

The reason for continued growth in customs is that users receive many more functions per unit cost from each advance in technology.

Microprocessors often require custom interface chips. The constant emergence of previously infeasible or unimagined products open new custom possibilities. □

CMOS switched-capacitor filters for a PCM voice CODEC

by Roubik Gregorian, Member, IEEE, and William E. Nicholson, Jr., Member, IEEE

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CMOS Switched-Capacitor Filters for a PCM Voice CODEC

ROUBIK GREGORIAN, MEMBER, IEEE, AND WILLIAM E. NICHOLSON, JR., MEMBER, IEEE

Abstract—Three switched-capacitor circuits are described which perform all filtering functions in a PCM voice CODEC. They use novel integrators and/or state-variable sections, which desensitize the overall response against stray-capacitance effects.[1] All filters are fully integrated on a CMOS test chip. The basic design considerations and the measured performance are discussed.[2]

I. Introduction

In a pulse-code-modulation (PCM) telephone system, the analog voice signal in each channel is band-limited to approximately 3400 Hz by a transmit filter. It is then converted into a pulse-amplitude-modulated (PAM) signal by a sampling switch, operated at an 8 kHz rate. Next, the PAM signals from all channels are encoded into a PCM signal, and the resulting binary bit stream is transmitted.

At the receiver, the incoming PCM signal is sequentially decoded and reconverted into PAM form. This signal is then applied to a sample-and-hold (S/H) stage, followed by the receive filter. The latter is a low-pass filter which smooths the S/H output by removing its high-frequency components. It also compensates for the $\sin(\omega T/2)/(\omega T/2)$ amplitude distortion due to the S/H stage.

Earlier versions of the transmit and receive filters were active-*RC* filters, realized using thin-film technology. The recently developed concept of switched-capacitor filters [1]-[3] makes it possible to obtain high-quality filters in fully integrated form. This has advantages in terms of size and cost, and it also avoids the need for tuning or trimming of the fabricated filter.

The purpose of this work is to describe the monolithic (CMOS) realizations of the transmit and receive filters, designed for a PCM coder-decoder (CODEC) system.

II. The Transmit Filter

A. General Considerations

The main function of the transmit filter is to limit the frequency content of the analog voice signal to the 0-3.4 kHz band. This then permits sampling at an 8 kHz rate without aliasing. In addition, some bandreject or high-pass filtering is also necessary, to prevent power-line-frequency signals (50 Hz and 60 Hz) from being transmitted. The block diagram of the filter is shown in Fig. 1(a); the timing diagram in Fig. 1(b). As the block diagram shows, the filter contains a low-pass and a high-pass filter, connected in cascade. The low-pass filter performs the bandlimiting to 3.4 kHz. Its clock rate is 128 kHz; this is high enough to minimize the error due to the imperfections of the terminating stages (discussed in Appendix II), yet not so high as to cause excessive spread in element values of the filter. The high-pass filter removes the 50 Hz and 60 Hz signals; it allows signals above 300 Hz to pass. A high clock rate would result in wide element-value spread for this filter, and hence the lowest possible rate, 8 kHz, was chosen. As explained below, this also permits operation without a separate input S/H stage.

The clock signals for the two filters are obtained from an on-chip phase-locked loop [Fig. 1(a)]. It runs at 1024 kHz, and locks to an external 8 kHz strobe signal.

Next, a detailed description of the transmit low-pass and high-pass filters will be given.

B. The Transmit Low-Pass Filter

The transmit low-pass filter operated at 128 kHz was designed to meet the International Telephone and Telegraph Consultative Committee (CCITT) attenuation/frequency recommendations. The theoretical design was carried out by computer-aided methods, such that, the composite response of the high-pass-low-pass combination was equal ripple in the passband. However, due to an error in the composite drawing of one capacitor, the actual frequency response of the low-pass filter deviated from the theoretical design. The switched-capacitor circuit with the wrong capacitor value was simulated by SCAR,[3] and the resulting frequency response is shown as the solid curve in Fig. 2. From now on, this frequency response will be assumed as the theoretical design, and the experimental measurement results will be compared to it.

The design approach chosen was based on the simulation of a doubly-terminated reactance ladder filter [3], [7]. The model circuit was a fifth-order elliptic filter [Fig. 3(a)]. The choice of this approach was motivated by the low-sensitivity properties of the resulting filter [9], [10].

Using the design technique of [3] and [7], the circuit of Fig. 2(b) resulted. In the circuit, the clock phases used in adjacent integrator stages must alternate, in order to achieve the "lossless" mapping $s = (z^{1/2} - z^{-1/2})/T$ between the complex frequency variables of the analog model and derived switched-capacitor filter.

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The authors are with American Microsystems Inc., Santa Clara, CA 95051.

[1]The circuit techniques to be described are in the process of being patented.

[2]The experimental results given here are measurements taken from a CMOS test chip containing filters.

[3]Switched-capacitor analysis routine (SCAR) is a computer-aided analysis program jointly developed by AMI and UCLA.

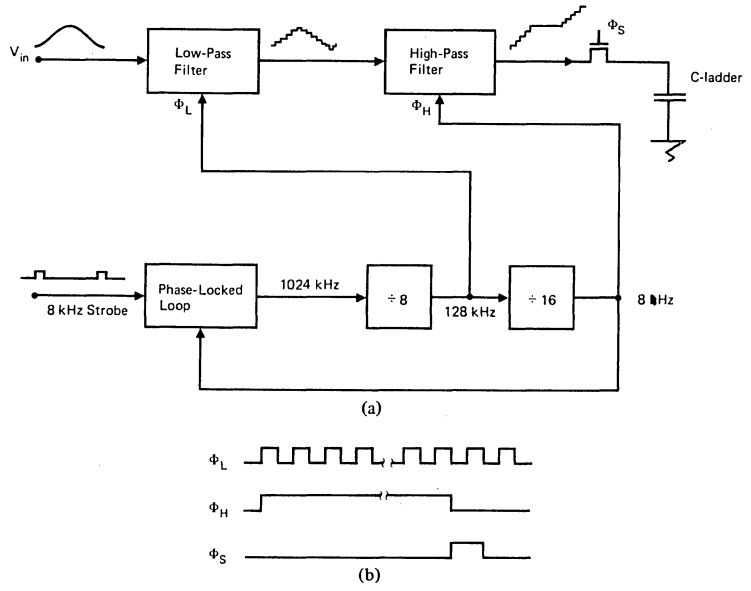


Fig. 1. (a) Block diagram of the transmit filter. (b) Timing diagram.

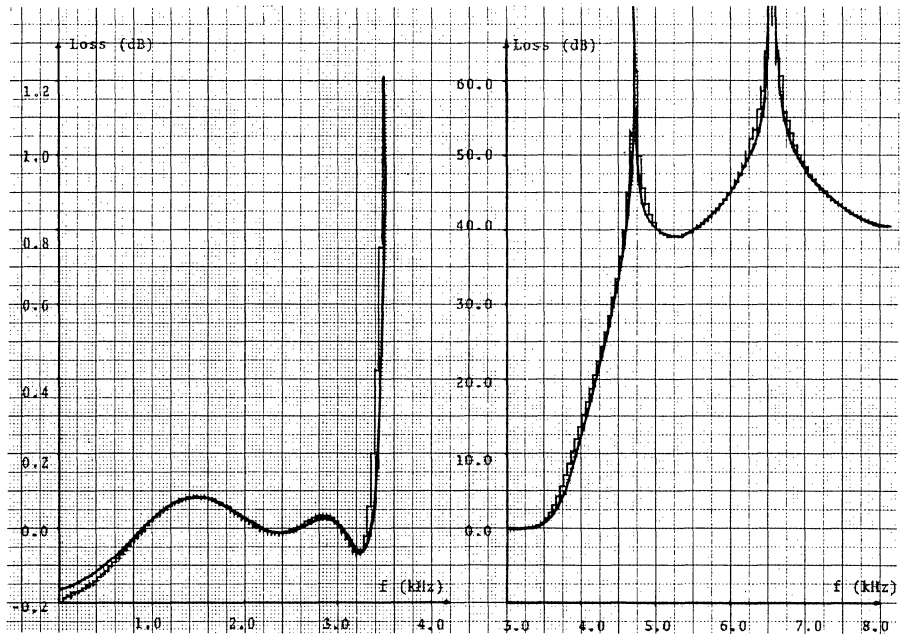


Fig. 2. Transmit-filter loss response.

It is shown in Appendix I that the integrator stages used in the circuit of Fig. 3(b) are somewhat sensitive to stray-capacitance effects. Hence, modified integrators (also described in Appendix I) have actually been used in the final circuit. The resulting filter is shown in Fig. 3(c).

The internal stages of the circuits in both Fig. 3(b) and (c) satisfy the lossless $s \leftrightarrow z$ mapping, previously given. The terminating stages, however, do not. This results in some loss distortion in the passband, having the largest effect near the passband limit. The effect is analyzed in Appendix II, where

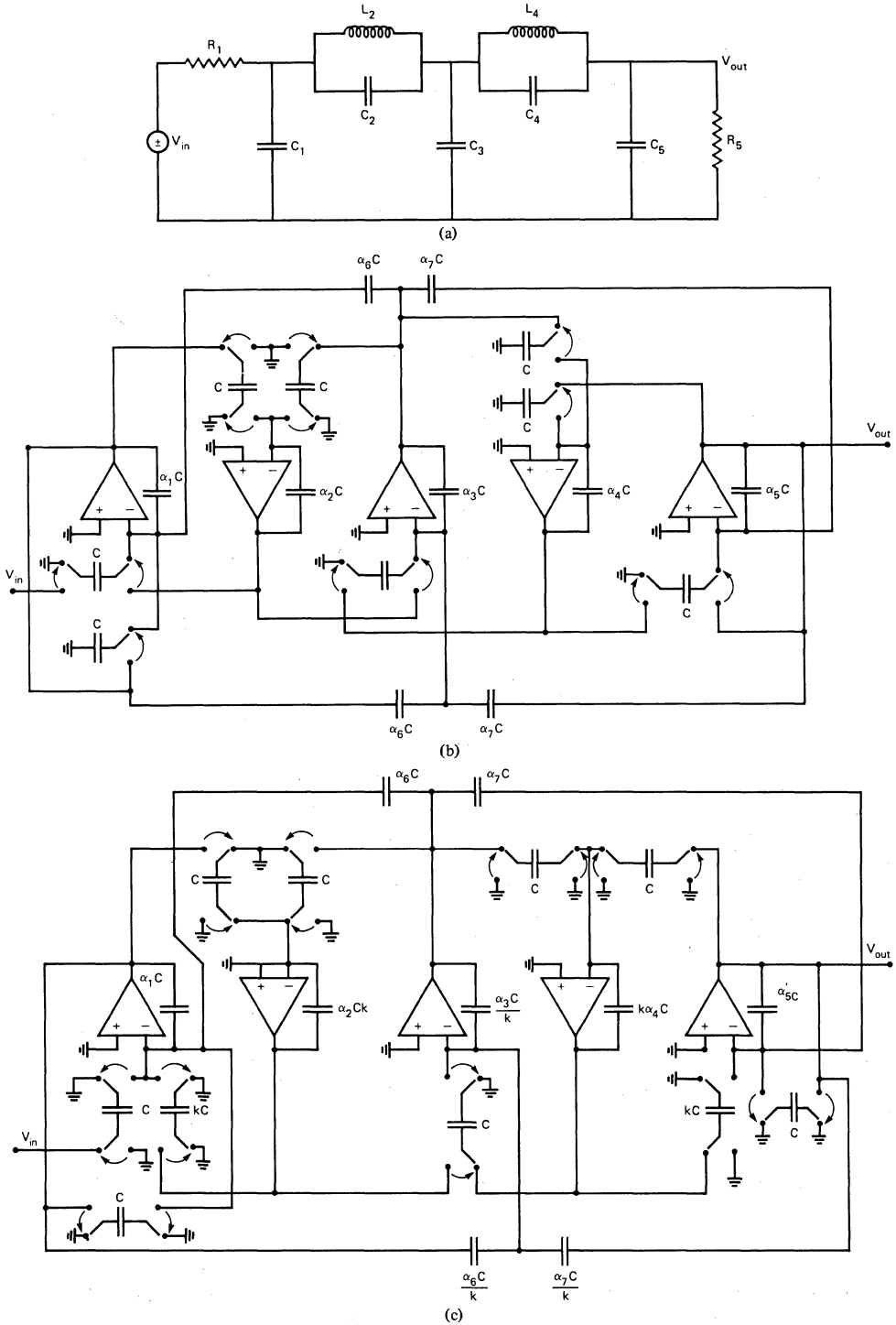


Fig. 3. (a) Analog model for the transmit low-pass filter. (b) Active switched-capacitor ladder filter. (c) Modified circuit of the ladder filter. $\alpha_1 = (C_1 + C_2)f_c$; $\alpha_2 = L_2 f_c$; $\alpha_3 = (C_2 + C_3 + C_4)f_c$; $\alpha_4 = L_4 f_c$; $\alpha_5 = (C_4 + C_5)f_c$; $\alpha_6 = C_2 f_c$; $\alpha_7 = C_4 f_c$.

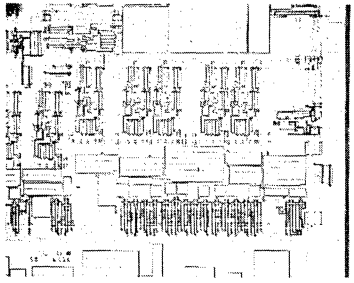


Fig. 4. Photomicrograph of the transmit low-pass filter.

it is shown that this distortion becomes negligible provided $\pi f_p T \ll 1$, where f_p is the upper frequency limit of the passband, and $T = 1/f_c$ the clock period. For the 128 kHz clock frequency and the 3.4 kHz passband limit, this condition is marginally satisfied. As a result, the loss distortion is less than 0.1 dB.

The output voltages of the integrators in Fig. 3(b) are scaled replicas of the inductor currents and capacitor voltages of the analog model. For sharply selective filters, such as the one discussed, the frequency responses of the inductor currents exhibit large resonant peaks near the passband limit; hence, the corresponding integrators may be driven into saturation. This was avoided for the filter of Fig. 3(c) by reducing the gains of the second and fourth integrators, which were subject to this effect, and increasing the gains of the following stages by corresponding amounts. Thus, a different scale factor was used in each stage. The magnitudes of these factors were chosen so as to maximize the dynamic range of the overall filter. Also, the largest capacitor of the circuit was found to be the feedback capacitor of the third operational amplifier. The scaling scheme used also reduced the value of this capacitor, and hence the capacitance spread of the filter, without scaling, was about 18:1; with scaling, 11.3:1. Since (as sensitivity analysis shows) the performance is most sensitive to the capacitance ratio of the third integrator, having more favorable values for this stage reduces the already low sensitivity even further.

The performance of the filter is affected by a number of nonideal phenomena. These are briefly discussed in Appendix III.

As the prototype of Fig. 3(a) illustrates, for $R_1 = R_2$ there is a flat loss of 6 dB between V_{out} and V_{in}. This can be avoided (or reduced) only at the cost of increasing the sensitivity of the filter [9], [10]. Hence, it was decided to accept this loss and to make up for it by a corresponding 6 dB gain in the high-pass transmit filter.

The die area for the low-pass filter was 2100 mil^2. It was fabricated using a 5 μm minimum-line-width CMOS process. The microphotograph of the chip is shown in Fig. 4. The measured frequency response as obtained from a frequency synthesizer and x-y plotter is shown as the staircased curve superimposed on the theoretical design in Fig. 2. The plot in Fig. 2 shows the excellent match between theoretical design and experimental results. The small error at low frequencies is primarily due to the large deviation of the loss from 0 dB.

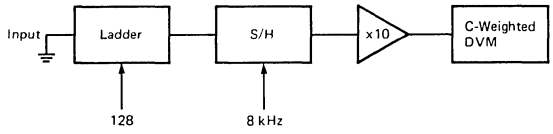


Fig. 5. Noise measurement setup for transmit low-pass filter.

This causes higher sensitivities of the frequency response to element value variations at these frequencies. The filter used ±5 V supply voltages. With a 6 V peak-to-peak sine-wave signal at 900 Hz applied to the input of the filter, the second harmonic was measured 68 dB below the fundamental component. The dc offset voltage at the output was measured to be 5 mV.

Noise measurement was performed with the setup shown in Fig. 5. The 8 kHz sample-and-hold was used to alias the high-frequency noise components into the baseband and effectively measure the wide-band noise. The measured noise was 55 μV_{rms}.

C. The Transmit High-Pass Filter.

The theoretical design of the high-pass filter clocked at 8 kHz is shown as the solid curve in Fig. 7(b).

The transfer function used was a third-order Chebyshev filter characteristic. The circuit configuration chosen is shown in Fig. 6(a); the timing diagram in Fig. 6(b). A detailed analysis of a state-variable circuit (similar to that of Fig. 6) was given in [4]. Using similar analysis techniques, the z-domain transfer function of the filter is readily found to be

$$H(z) = \frac{V_0(z)}{V_{in}(z)} = \frac{\alpha_1 \alpha_3 (z-1)^3}{[(1+\alpha_4)z - 1]\,[(1+\alpha_1)z^2 - (2+\alpha_1 - \alpha_1'\alpha_2)z + 1]}. \tag{1}$$

Using the bilinear $s \leftrightarrow z$ transformation

$$S = \frac{2}{T}\frac{z-1}{z+1} \tag{2}$$

$H(z)$ transforms into the form

$$H(s) = \frac{s^3}{a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{3}$$

which is suitable for a third-order all-pole analog transfer function. Hence, choosing the a_i in (3) so as to obtain the desired Chebyshev characteristic, then transforming the resulting $\hat{H}(s)$ using (2) into the z-domain, and finally equating the coefficients of z^k to those in (1), the element values α_i in Fig. 6(a) can readily be obtained.

Inspection of the circuit of Fig. 6(a) reveals that during the $\phi_H = 1$ half-cycle a direct path exists from the input terminal to the output. Hence, unless the input signal is a sampled-and-held waveform, there is a signal leak-through which affects the frequency response of the filter. Fortunately, as the block diagram of Fig. 1(a) shows, the high-pass filter is followed by a S/H stage operated at 8 kHz. By choosing the phase ϕ_s of the sampling switch to be complementary to ϕ_H [Fig. 1(b)] the leakthrough is eliminated.

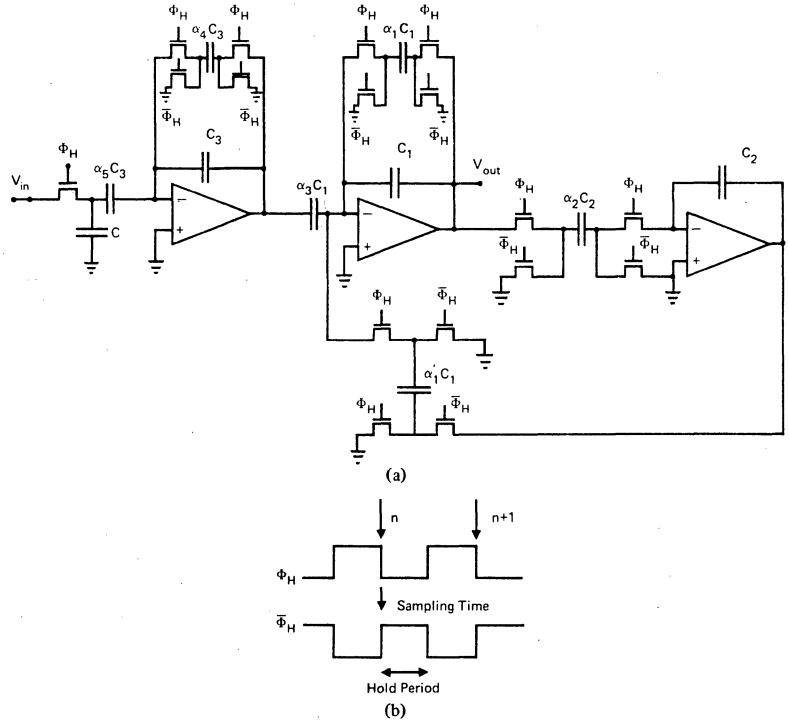


Fig. 6. (a) Circuit diagram of the transmit high-pass filter. (b) Timing diagram.

The die area of the high-pass filter was 2300 mil^2. It was fabricated on the same chip as the low-pass filter and the phase-locked loop, using a 5 μm minimum-linewidth CMOS process. Its photomicrograph is shown in Fig. 7(a).

The frequency response is shown as the staircased curve in Fig. 7(b). Narrow pulse sampling was used in the measurements to avoid the $\sin x/x$ rolloff due to the 8 kHz sample-and-hold effects. The dc offset output voltage was -0.5 mV. The noise was measured with the setup shown in Fig. 7(c). The measured noise was 35 μV_{rms} *C*-message weighted.

The largest capacitance ratio in the circuit was 7:1; note that the capacitance ratio would have been 106:1 if a 128 kHz clock rate had been used.

III. The Receive Filter

The receive filter performs two functions. It smoothes the sampled-and-held signal coming from the 8 kHz S/H stage following the decoder, by removing frequencies above 4 kHz. It also incorporates the loss equalization necessary to compensate for the loss distortion caused by the S/H operation. The specifications are thus in the form

Passband: $0 \leqslant f \leqslant f_p$ (passband edge);

$$\text{loss} = 20 \log \left| \frac{\sin \pi f T}{\pi f T} \right| \pm \alpha_p .$$

Stopband: f_s (stopband edge) $\leqslant f \leqslant \infty$; loss = ∞.

Clock frequency: 128 kHz.

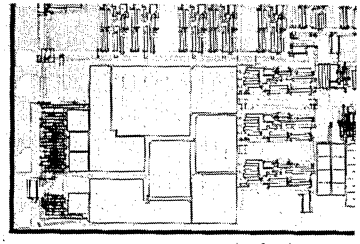
The theoretical design is shown as the solid curve in Fig. 8. The response shown belongs to a S/H followed by the receive filter.

Due to the shaped passband response, the low-sensitivity design approach used for the transmit low-pass filter is not feasible for the receive filter. Hence a two-stage state-variable configuration was chosen for the circuit. Each stage was a third-order filter section, containing the low-sensitivity configurations discussed in Appendix I. Fig. 9(a) shows the basic circuit; Fig. 9(b) the clock signals. For a single stage, the operation of the circuit is described by the charge-conservation equations

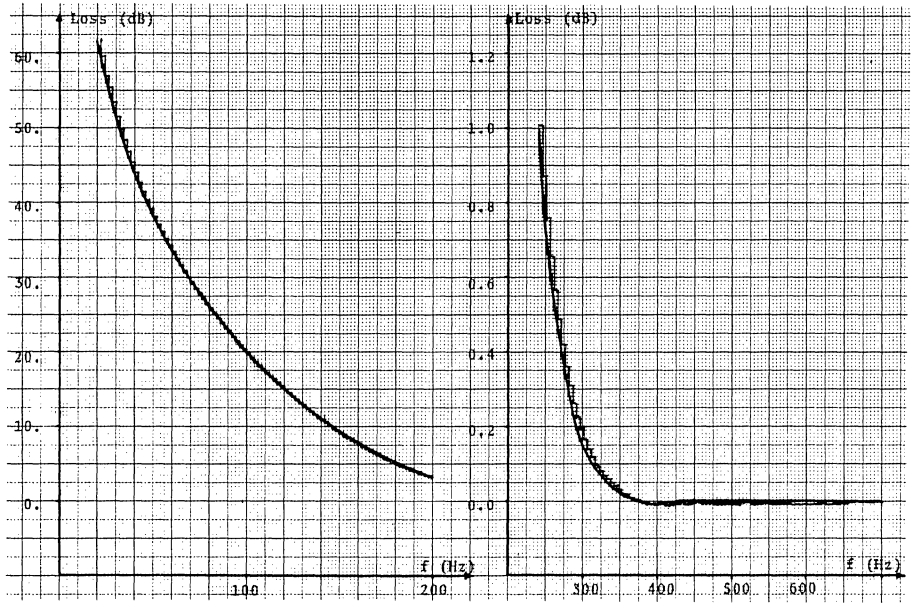
$$\begin{aligned} C_1 V_1(n) - C_1 V_1(n-1) &= -\alpha_1 V_1(n) - \alpha_1' V_2(n) + \alpha_3 V_{in}(n-1) \\ C_2 V_2(n) - C_2 V_2(n-1) &= \alpha_2 V_1(n-1) \\ C_3 V_3(n) - C_3 V_3(n-1) &= -\alpha_6 C_3 V_3(n-1) - \alpha_5 C_3 V_2(n) \\ &\quad - \alpha_4 C_3 [V_1(n) - V_1(n-1)]. \end{aligned} \tag{4}$$

In the z-domain, these equations lead to the transfer function

$$\begin{aligned} H(z) &\triangleq \frac{V_0(z)}{V_{in}(z)} \\ &= -\frac{\alpha_3 \alpha_4 \left[z^2 - \left(2 - \frac{\alpha_2 \alpha_5}{\alpha_4} \right) z + 1 \right]}{[(1+\alpha_6) z - 1](1+\alpha_1) z^2 - (2 + \alpha_1 - \alpha_1' \alpha_2') z + 1]}. \end{aligned} \tag{5}$$



(a)



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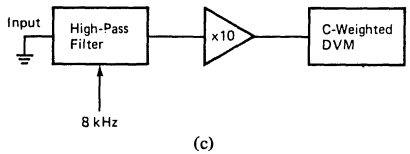


(c)

Fig. 7. (a) Photomicrograph of the transmitt high-pass filter. (b) Frequency response of the transmit high-pass filter. (c) Noise measurement setup for transmit high-pass filter.

$H(z)$ represents a third-order characteristic with three poles (one real, two normally forming a complex conjugate pair) and two conjugate complex transmission zeros on the unit circle. Cascading two such sections, therefore, a sixth-order filter response resembling a "Type A" elliptic characteristic can be obtained.

The element values α_i of the filter were found using computer-aided optimization. This was performed by minimizing a power of the error between the desired and the actual responses, integrated over the frequency range of interest. In the passband, the desired gain was the $(\omega T/2)/\sin(\omega T/2)$ response; in the stopband, an equiripple (Chebyshev) behavior.

The design was carried out directly in the z-domain, in two steps. First, the critical frequencies (zeros and poles) were found using the least pth optimization strategy [10], by matching $|H[\exp(j\omega T)]|$ to the desired amplitude response. Next, the poles and zeros of the transfer function were paired in an optimum manner, and the element values found using coefficient matching. In assigning the poles to zeros, the objective was to minimize the in-band loss of the overall filter, and to maximize its dynamic range.

It should be noted that the two capacitors $\alpha_3 C_1$ and $\alpha_1' C_1$ could be replaced by a single "differencing" capacitor, connected between V_{in} and ground during the $\phi = 1$ half-cycle, and to V_2 and the input of the first operational amplifier during the $\phi = 0$ half-cycle. The actual circuit uses two capac-

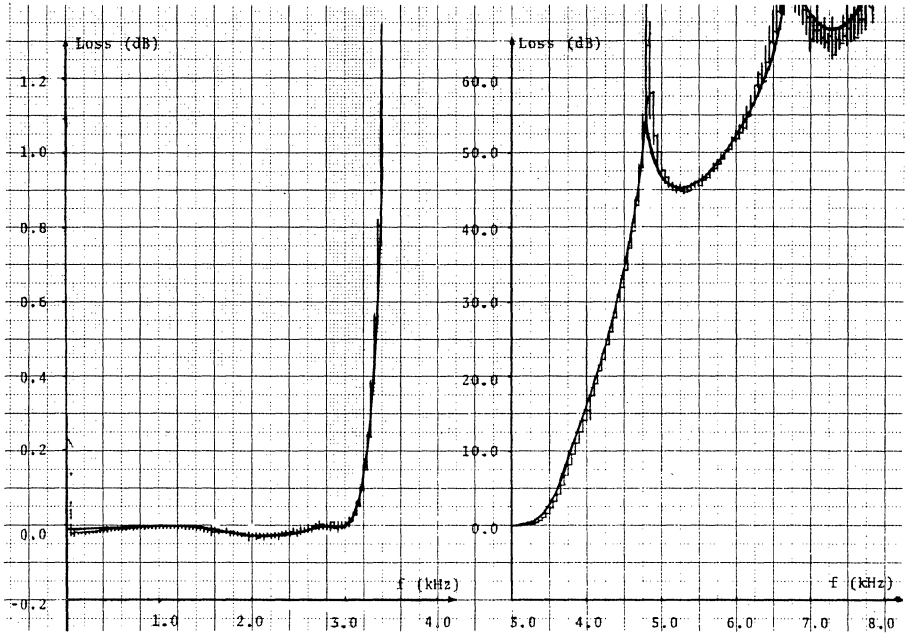


Fig. 8. Frequency response of receive filter.

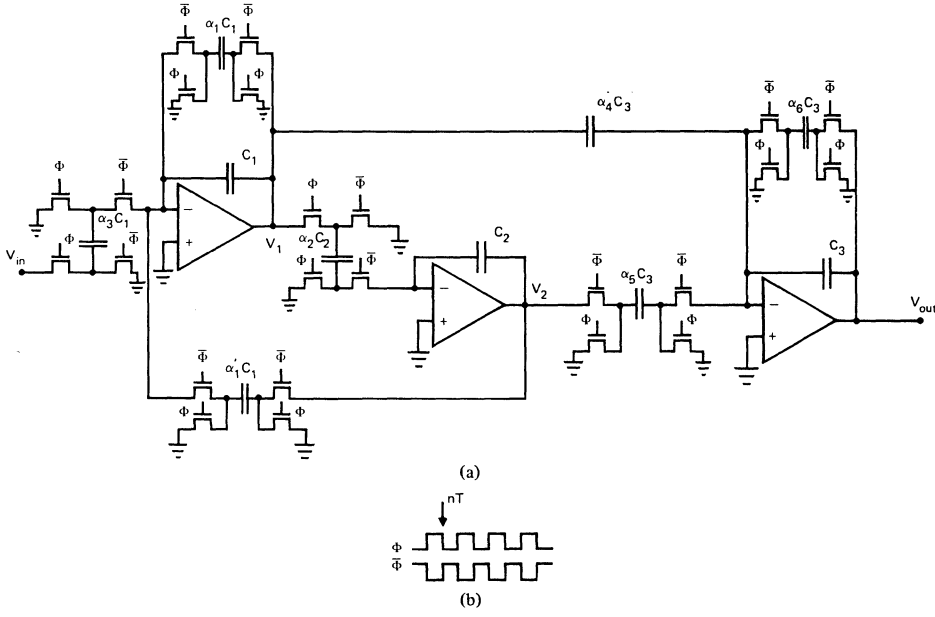
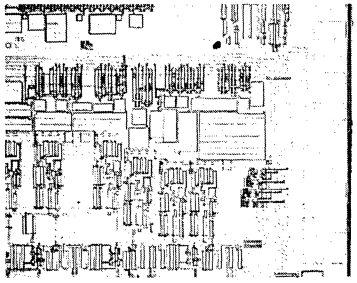


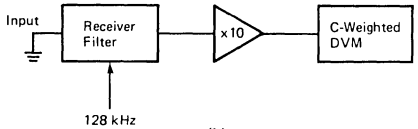
Fig. 9. (a) Circuit diagram of the receive filter stages. (b) Timing diagram.

itors, thereby providing an extra free parameter. The latter was used to scale the gain of each stage such that the maximum gain values were the same for all six amplifiers.

The total die area of the six amplifiers and 20 capacitors contained in the filter was 2500 mil^2. It was processed in CMOS, with thin-oxide polysilicon-to-metal capacitors. The photomicrograph of the filter is shown in Fig. 10(a). The measured frequency response is shown as the staircased curve in Fig. 8. The response belongs to a S/H, followed by the receive filter. The circuit uses ±5 V supply voltages and 128 kHz



(a)



(b)

Fig. 10. (a) Photomicrograph of the receive filter. (b) Noise measurement setup for receive filter.

clock. The measured output dc offset voltage was 6 mV. Noise was measured with the setup of Fig. 10(b) as 85 μV_{rms} C-message weighted.

IV. The Sensitivity of the State-Variable Filter Sections

The simulated-ladder configuration used for the transmit low-pass filter is known [3], [7] to exhibit the same low-sensitivity properties as the model analog filter. However, the cascaded-section structures used in the other two filters do not have such inherently low sensitivities, and hence their behaviors for inaccurate element values need to be examined.

Element-value variations affect the transfer functions given in (1) and (5) primarily by changing the natural modes (poles) of the circuits. [Note that the zeros of $H(z)$ in (1) are not affected by the α_i; also, the zeros in (5) remain on the unit circle for all α_i values.] Hence, first the behavior of the natural-mode polynomial will be examined. Let

$$P(s) = s^2 + (\omega_0/Q)s + \omega_0^2 \tag{6}$$

be the analog equivalent of the quadratic factor of the natural-mode polynomial, obtained by using the bilinear transformation (2). Equating coefficients in (1) and (5) and normalizing time and frequency so that $T = 1$, we obtain

$$\omega_0 = 2\left[\frac{\alpha_1'\alpha_2}{4 + 2\alpha_1 - \alpha_1'\alpha_2}\right]^{1/2} \tag{7}$$

$$Q = \frac{[\alpha_1'\alpha_2(4 + 2\alpha_1 - \alpha_1'\alpha_2)]^{1/2}}{2\alpha_1}. \tag{8}$$

Defining the usual way logarithmic sensitivities

$$S_x^y = (x/y)\,\partial y/\partial x,$$

we get the sensitivities of ω_0 and Q:

$$S_{\omega_0}^{\alpha_1} = -\frac{\omega_0^2\alpha_1}{4\alpha_1'\alpha_2}$$

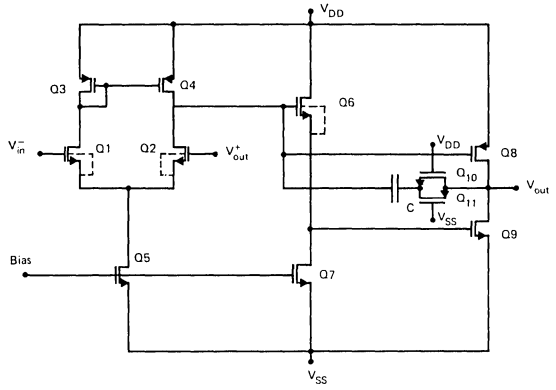


Fig. 11. CMOS operational amplifier.

$$S_{\omega_0}^{\alpha_1'} = S_{\omega_0}^{\alpha_2} = \omega_0^2\frac{2 + \alpha_1}{4\alpha_1'\alpha_2}$$

$$S_Q^{\alpha_1} = \alpha_1'\alpha_2\frac{\alpha_1'\alpha_2 - \alpha_1 - 4}{4\alpha_1^2 Q^2}$$

$$S_Q^{\alpha_1'} = S_Q^{\alpha_2} = \alpha_1'\alpha_2\frac{2 + \alpha_1 - \alpha_1'\alpha_2}{4\alpha_1^2 Q^2}. \tag{9}$$

The sensitivity effects are worst for high-Q sections. For the state-variable section with the highest Q (contained in the receive filter), $Q \cong 5.5$ and $\omega_0 \cong 0.175$. Using the corresponding α_i in (9), the sensitivities turn out to be

$$S_{\omega_0}^{\alpha_1} = 0.008$$
$$S_{\omega_0}^{\alpha_1'} = S_{\omega_0}^{\alpha_2} = 0.5$$
$$S_Q^{\alpha_1} = -0.9$$
$$S_Q^{\alpha_1'} = S_Q^{\alpha_2} = 0.49.$$

Thus, all-relative sensitivities are less than unity.

Turning now to the sensitivities of the transmission zero θ_0 of the receive filter stage of Fig. 9, the logarithmic sensitivities can be found from (5):

$$S_{\theta_0}^{\alpha_2} = -S_{\theta_0}^{\alpha_4} = S_{\theta_0}^{\alpha_5} = \frac{\alpha_2\alpha_5}{2\alpha_4\theta_0\sin\theta_0}. \tag{10}$$

For the high-Q section of the receive filter, $\theta_0 \simeq 0.315$, and (10) gives $S_{\theta_0}^{\alpha_2} = -S_{\theta_0}^{\alpha_4} = S_{\theta_0}^{\alpha_5} = 0.5$.

For the transmit high-pass filter, we have $\omega_0 \simeq 0.145$, $Q \simeq 1.14$ and the corresponding sensitivities are

$$S_{\omega_0}^{\alpha_1} \cong 0.03 \qquad S_{\omega_0}^{\alpha_1'} = S_{\omega_0}^{\alpha_2} \cong 0.5$$
$$S_Q^{\alpha_1} \cong -0.96 \qquad S_Q^{\alpha_1'} = S_Q^{\alpha_2} = 0.5.$$

The above results show that all sensitivities of the state-variable sections are within practically acceptable limits.

V. Switched-Capacitor Filter Components

The circuit diagram of the CMOS operational amplifier used in the filters is shown in Fig. 11. In the input stage, Q_1, Q_2, Q_3, and Q_4 form a differential-input-single-ended-output

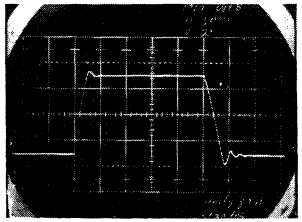


Fig. 12. Square-wave response of the operational amplifier; horizontal scale 1 μs/div, vertical scale 2 V/div.

voltage amplifier. This is followed by a dc level shifter consisting of Q_6 and Q_7, which drives Q_9 in the output stage. Transistors Q_8 and Q_9 provide the output buffer and gain stage. Frequency compensation is accomplished by using the on-chip Miller capacitor $C(\approx 5$ pF).

The circuit design ensures that the performance is essentially unaffected by threshold-voltage variations. The device geometries were selected so as to keep all transistors in saturation, even for large output voltage swings and large common-mode signals.

Fig. 12 shows the time response of the amplifier, connected as a unity-gain voltage follower, when a ±3 V square-wave input voltage was applied.

The measured performance of the amplifier is summarized in the following table:

Open-loop dc gain	86 dB
Power dissipation (for $V_{DD} = -V_{SS} = 5$ V)	5 mW
Slew rate	+13 V/μs
(for 6V input step)	− 9 V/μs
0.1 percent settling time (for 15 pF load)	< 1.5 μs
Equivalent input noise voltage (10 kHz BW)	14 μV_{rms}
Common-mode rejection ratio (for $V_{DD} = -V_{SS} = 5$V, and -4.6 V < V_{cm} < 3.9 V)	70 dB

The total die area of the amplifier (fabricated using 5 μm minimum-linewidth rule) was 170 mil^2.

The capacitors used in the filters were formed by metal and polysilicon electrodes, with thin-silicon-dioxide dielectric. The thin oxide is created by the oxide regrowth occurring automatically during the processing sequence used. It results in 0.37 pF/mil^2 capacitance without the need for any extra processing steps.

VI. Conclusions

Monolithic (CMOS) realization of transmit and receive filters designed for a PCM voice coder-decoder (CODEC) system has been described. The design of the transmit low-pass was based on the simulation of a doubly-terminated reactance ladder filter. This choice was motivated by the low-sensitivity properties of the resulting filters. The state-variable structure was chosen for the transmit high-pass and receive low-pass filters. Special integrator schemes made the filter frequency responses insensitive to parasitic elements. Novel state-variable structures were presented that placed the transmission zeros inherently on the unit circle independent of capacitor ratios. Direct z-domain design was carried out which eliminated $s \leftrightarrow z$ transformation effects. Results were presented for the transmit and receive filters. The transmit circuit implemented a fifth-order elliptic ladder filter. This was followed by a third-order Chebyshev all-pole high-pass circuit. Sampling rates of 128 kHz and 8 kHz were used for the low-pass and high-pass, respectively. The achieved dynamic range for the transmit section was 91 dB. The receive filter was realized by a two-stage state-variable configuration. Each stage was a third-order elliptic filter section. In the passband the receiver filter approximated an $x/\sin(x)$ response. Sampling rate of 128 kHz was also used for the receive filter and the achieved dynamic range was 89 dB. The filters used CMOS operational amplifiers with measured open-loop gain of 86 dB. Second harmonic distortion with 6 V peak-to-peak single frequency input signal and ±5 V supply voltage was 68-70 dB below the fundamental component for all three filters.

Termination inaccuracy effects in simulated ladder filters and nonideal effects in switched-capacitor filters were briefly discussed.

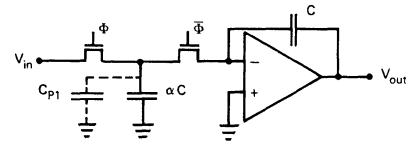


Fig. 13. Basic switched-capacitor integrator stage.

Appendix I
Low-Sensitivity Integrators[4]

Fig. 13 shows the basic integrator used in simulated ladder filters. Its transfer function (for $C_{p1} = 0$) is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha}{z - 1}. \tag{11}$$

This section is insensitive to most stray-capacitance effects, since the impedances from almost all nodes to ground are very low. However, the stray capacitance C_{p1} from the upper plate of αC to ground is in parallel with αC, and hence changes the value of α to $\alpha + C_{p1}/C$ in (11). This establishes a lower limit on αC and hence on the total die area occupied by the stage. Furthermore, C_{p1} includes nonlinear p-n junction capacitance, and hence contributes to the harmonic distortion of the filter.

In order to avoid the inaccuracy and nonlinearity caused by C_{p1}, two alternative integrator stages have been developed which are immune to the effects of C_{p1}. The first circuit is shown by Fig. 14(a) [11]-[13]. Except for the absence of the negative sign, this stage has the same transfer function as that shown in Fig. 13. However, now none of the stray capacitances affect the operation. In fact, C_{p1} only absorbs and discharges to ground from the input voltage source. C_{p2} ac-

[4]The circuits described here have been developed independently by the authors and several other people.

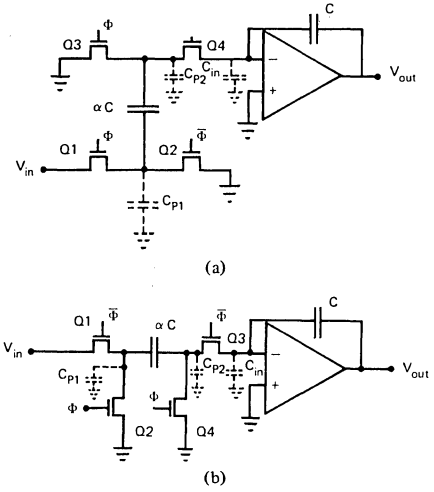


Fig. 14. (a) Low-sensitivity noninverting integrator stage. (b) Low-sensitivity inverting integrator stage.

quires some charge from αC temporarily (when $Q3$ turns off), but then loses it to the capacitor C after $Q4$ turns on. Hence, except for this brief transient, it does not contribute to the operation of the stage.

A different circuit is shown in Fig. 14(b). It is an inverting integrator which uses a series (rather than shunt) switched capacitor. The operation of the circuit is as follows. When $\phi = 1$, Q_2 and Q_4 discharge αC, C_{p1}, and C_{p2}. When ϕ turns zero, αC and C_{p1} are charged to V_{in} through Q_1 and Q_3, while C_{p2} and C_{in} are held at virtual ground. Hence, again only C_{p1} absorbs charge from the input voltage source, but the total charge integrated by C is supplied by αC and the stray capacitors do not participate in the operation of the circuit.

The circuits of Fig. 14 were used in the ladder-simulation filter shown in Fig. 3(c) and discussed in Section II-B. A different application of the principles illustrated in Fig. 14 was used in the state-variable sections of Figs. 6 and 9.

Appendix II
Termination Inaccuracy Effects in Simulated-Ladder Filters

As mentioned in Section II-B, the terminating stages of the circuits [of Fig. 3(b) and 3(c)] do not satisfy the lossless $s \leftrightarrow z$ transformation valid for the internal stages. As a result, the terminations R_1 and R_2 of the model analog filter are equal to $R \exp(-j\omega T/2)$ for Fig. 3(b) and $R \exp(j\omega T/2)$ for Fig. 3(c) rather than R. Thus, for Fig. 3(c) both terminations are changed by an amount

$$\Delta R_1 = \Delta R_2 = +R\,[1 - \exp(j\omega T/2)]. \tag{12}$$

It is known [9] that a first-order approximation for the corresponding change in the loss α (in nepers) is given by:

$$\Delta\alpha \cong \frac{1}{2}\,\mathrm{Re}\left[\rho_1 \frac{\Delta R_1}{R} + \rho_2 \frac{\Delta R_2}{R}\right] \tag{13}$$

where ρ_1 and ρ_2 are the input and output reflection factors, respectively. From [12] and [13], for $\omega T/2 \ll 1$

$$\Delta\alpha = \frac{1}{2}\,\mathrm{Re}\,[(\rho_1 + \rho_2)(1 - \exp(j\omega T/2)] \cong -\frac{\omega T}{4}\,\mathrm{Im}(\rho_1 + \rho_2). \tag{14}$$

For the doubly-terminated reactance-two-port model filter used,

$$|\rho_1|^2 = |\rho_2|^2 = 1 - \exp(-2\alpha) \cong 2\alpha. \tag{15}$$

For the circuit of Fig. 3(b) a similar expression as (14) holds with the negative sign omitted. Hence, for both circuits, an upper bound can be given for $|\Delta\alpha|$:

$$|\Delta\alpha| \leqslant \frac{\omega T}{2}\,|\rho_1| \cong \omega T\sqrt{\alpha/2}. \tag{16}$$

For the transmit low-pass filter we have $F_c = 1/T = 128$ kHz; the passband limit is $f_p = 3.4$ kHz, and $\alpha \leqq 0.1$ dB $\simeq 0.0115$ Np in the passband. Hence, (16) gives $|\Delta\alpha| < 0.103$ dB for the additional passband loss distortion.

Appendix III
Nonideal Effects in Switched-Capicitor Filters

In this Appendix, some nonideal effects will be analyzed. Consider the basic integrator stage shown in Fig. 13. Assume that $C_{p1} = 0$, and that in the frequency range of interest $A(\omega) = A(0) < \infty$. Then the input voltage of the operational amplifier is $-V_{out}/A$, and the charge-conversation relation is

$$C\left[V_{out}(n) + \frac{V_{out}(n)}{A(0)}\right] - C\left[V_{out}(n-1) + \frac{V_{out}(n-1)}{A(0)}\right]$$
$$= -\alpha C\left[\frac{V_{out}(n)}{A(0)} + V_{in}(n-1)\right]. \tag{17}$$

Using z-transformation

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha_1'}{z - (1 - \epsilon)} \tag{18}$$

results, where

$$\alpha' \triangleq \frac{\alpha A(0)}{A(0) + \alpha + 1}, \qquad \epsilon \triangleq \frac{\alpha}{A(0) + \alpha + 1}. \tag{19}$$

For $|\alpha| < 1$ and $A(0) > 10^4$ (which was valid for our filters), $|\Delta\alpha/\alpha| < 2 \times 10^{-4}$ and $|\epsilon| < 10^{-4}$. Hence, the effect of the finite gain is negligible.

Another parasitic effect which affects the performance is the nonzero "on" resistance R_{on} of the MOS switching transistors. As a result, at high switching rates the time constant of R_{on} and the capacitors charged or discharged by it may become comparable to the clock half-period. The effect is a capacitor ratio error that causes distortion of the frequency response. This effect can be decreased by increasing the width-to-length ratios of the channels of the switching transistors. This will, however, also increase the clock feedthrough and leakage in the switch.

Finally, the dc offset of the filters will be briefly discussed. The major contributing factors to the dc offset are the offset

of the operational amplifier, junction leakages, and clock feedthrough. The amplifier offset can cause latchup, unless there is a switched capacitor removing the accumulated charge from the input terminals or it is in a negative feedback loop. The leakage current through the p-n junction of the switching transistor at the amplifier input causes a sawtooth component in the output voltage, when input is zero. The overlap capacitance between the gate and the source of the switching MOSFET causes clock feedthrough, which takes the form of sharp impulses in the output. Both leakage and clock feedthrough cause error voltages which are periodic and occur at the clock rate. Due to the sampling in the subsequent stagers, this error will appear aliased as a dc offset voltage.

In the filters designed and fabricated by the authors, self-aligned-gate technology was used. This minimized the gate-overlap capacitance of the switching transistors, and hence the clock feedthrough. Also, CMOS transfer gates were used as switches. Hence, the positive rising and negative falling edges causing clock feedthrough were nearly matched, and almost exactly canceled.

ACKNOWLEDGMENT

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Roubik Gregorian (S'76–M'77), for a photograph and biography, see this issue, p. 969.

William E. Nicholson, Jr. (M'77), for a photograph and biography, see this issue, p. 969.

Switched-capacitor filter design using cascaded sections

by Roubik Gregorian, Member, IEEE

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Switched-Capacitor Filter Design Using Cascaded Sections

ROUBIK GREGORIAN, MEMBER, IEEE

Abstract—**This paper describes a number of simple (first-, second-, or third-order) switched-capacitor circuits. These can be used as simple self-contained filters, or as filter sections in the cascade realization of a higher order transfer function. All these sections are free from parasitic effects, and all can be designed directly in the sampled-signal domain. Low-pass, high-pass, bandpass, and all-pass circuits are discussed, with and without finite nonzero transmission zeros.**

I. Introduction

THE PURPOSE of this paper is to describe first-, second-, and third-order switched-capacitor filter sections. These sections can be cascaded to realize higher order sharply selective filters. They share the following advantages.

1) They can be designed directly in the sampled-data (z-variable) domain. No approximation requiring $f \ll f_c$ is implied or necessary.

2) Transmission zeros at finite nonzero frequencies can be realized.

3) The circuit response is unaffected by parasitic capacitances.

No attempt was made to develop a general-purpose filter section, since design experience suggests that a set of specialized sections, each suited to a particular purpose, is preferable.

II. Basic Structures

The basic building block of the sections to be described is the switched-capacitor integrator. Its usual form is shown in Fig. 1(a); however, the performance of this circuit is sensitive to the parasitic capacitance C_{p1} between the upper plate of the grounded capacitor αC and ground. To avoid the inaccuracies and nonlinear effects due to C_{p1}, two improved integrator circuits have been developed [1]–[3]. These are shown in Fig. 1(b) and (c); they are the ones used in the sections discussed below.

Another simple circuit, which realizes a first-order high-pass transfer function, is shown in Fig. 2. In the figure, it was assumed that a separate sample-and-hold (S/H) stage is used at the input. Usually, however, the first-order circuit forms a section of a higher order filter and v_{in} is, therefore, already a sampled-and-held signal. Then, of course, the S/H stage can be omitted. The

Manuscript received October 26, 1979; revised January 21, 1980.
The author is with American Microsystems, Inc., Santa Clara, CA 95051.

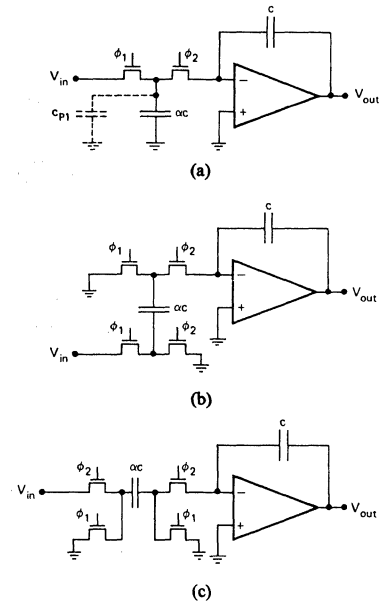

Fig. 1. Basic switched-capacitor integrator state. (b) Parasitic insensitive noninverting integrator stage. (c) Parasitic insensitive inverting integrator stage.

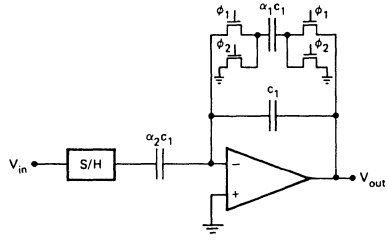

Fig. 2. First-order high-pass filter stage.

transfer function of the section is

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{\alpha_2}{1+\alpha_1} \cdot \frac{z-1}{z-(1+\alpha_1)^{-1}}. \quad (1)$$

The operation of this circuit is again independent of the effects of all stray capacitances.

Fig. 3 illustrates a second-order filter section, based on the improved integrators shown in Fig. 1(b) and (c). Its

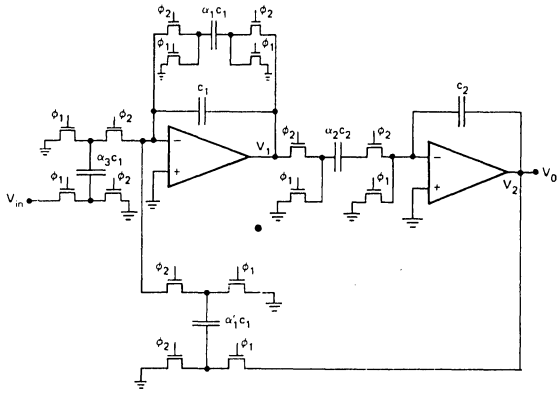

Fig. 3. Second-order parasitic-free filter section.

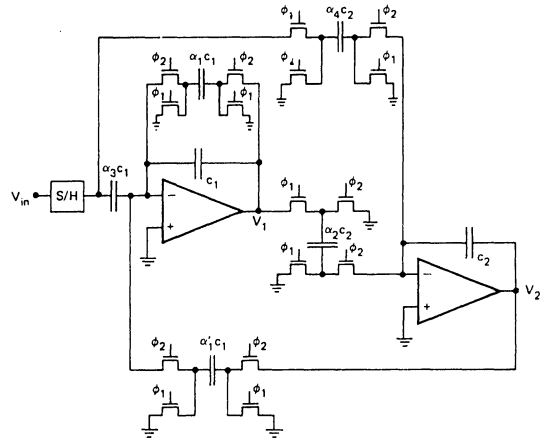

Fig. 4. Second-order notch filter.

transfer function is

$$H(z)=\frac{-\dfrac{\alpha_2\alpha_3}{1+\alpha_1}z}{z^2-\dfrac{2'+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z+\dfrac{1}{1+\alpha_1}} \tag{2}$$

which contains no finite transmission zeros. In this circuit, if desired, capacitors $\alpha_1 C_1$ and $\alpha_3 C_1$ can be replaced by a single capacitor connected between v_{in} and ground during the $\phi_1=1$ half cycle, and between V_0 and the input of the first operational amplifier when $\phi_2=1$. By using two capacitors as shown, a free parameter is introduced which can be used to scale the voltage gain of the section. Thus the dynamic range of the filter can be maximized.

III. Notch Filter Sections

The circuit shown in Fig. 4 can be used as a second-order notch filter section. It is again constructed from the parasitic-immune building blocks of Section II. From charge conservation, the relations

$$\begin{aligned}C_1v_1(nT)&=C_1v_1(nT-T)-\alpha_1C_1v_1(nT)-\alpha_1'C_1v_2(nT)\\&\quad-\alpha_3C_1[v_{in}(nT)-v_{in}(nT-T)]\\C_2v_2(nT)&=C_2v_2(nT-T)+\alpha_2C_2v_1(nT-T)\\&\quad+\alpha_4C_2v_{in}(nT-T)\end{aligned} \tag{3}$$

can be obtained. From (3), the transfer function from the input v_{in} to the output v_1 of the first amplifier can be found:

$$H(z)=\frac{V_1(z)}{V_{in}(z)}=-\frac{\alpha_3}{1+\alpha_1}\cdot\frac{z^2-\left(2-\dfrac{\alpha_1'\alpha_4}{\alpha_3}\right)z+1}{z^2-\dfrac{2+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z+\dfrac{1}{1+\alpha_1}}. \tag{4}$$

In addition to two (normally complex-conjugate) poles, there are now two complex-conjugate transmission zeros located on the unit circle. Hence, this circuit can be used as a self-contained notch filter, or as one of the sections in an elliptic filter. As an illustration, Fig. 5 shows a third-order elliptic low-pass filter, obtained by combining the first-order section with the notch filter section. The transfer function of this circuit is given by

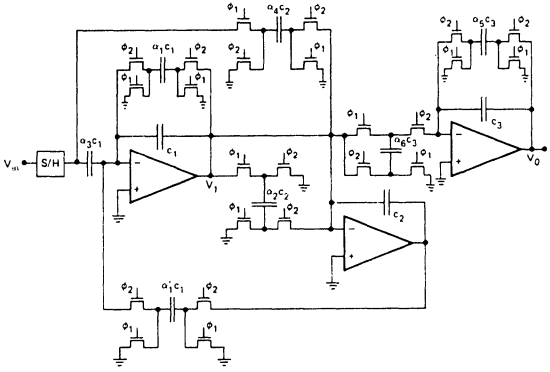

Fig. 5. Third-order elliptic low-pass filter.

$$H(z)=\frac{V_0(z)}{V_{in}(z)}=\frac{\alpha_3\alpha_6}{(1+\alpha_1)(1+\alpha_5)}\cdot\frac{(z+1)\left[z^2-\left(2-\dfrac{\alpha_1'\alpha_4}{\alpha_3}\right)z+1\right]}{\left(z-\dfrac{1}{1+\alpha_5}\right)\left(z^2-\dfrac{2+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z+\dfrac{1}{1+\alpha_1}\right)}.$$

The coefficients of the transfer function (and from these, the element values) can be obtained by applying the familiar bilinear s-to-z transformation

$$S=\frac{2}{T}\frac{z-1}{z+1} \tag{5}$$

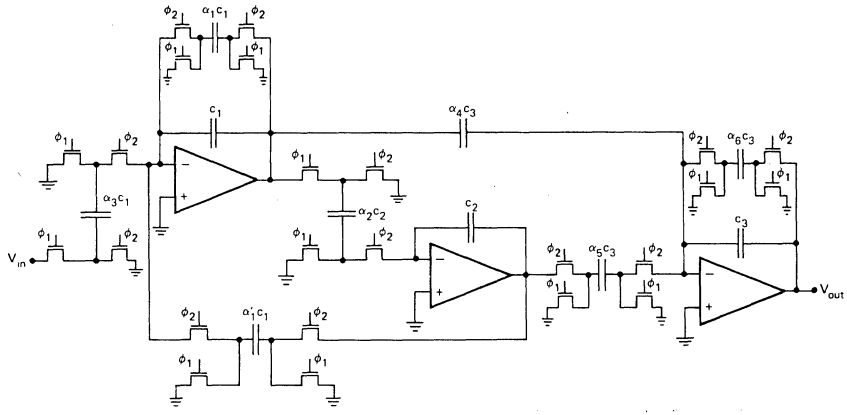

Fig. 6. Alternative form of third-order low-pass filter.

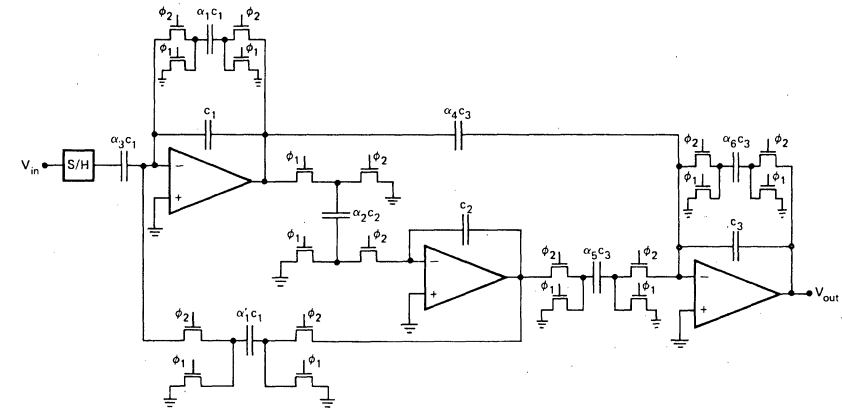

Fig. 7. Third-order elliptic high-pass filter.

to the transfer function of an analog elliptic filter designed with appropriately predistorted specifications [4].

An alternative realization of a third-order low-pass filter section [1] is shown in Fig. 6. Its transfer function is

$$H(z) = -\frac{\alpha_3\alpha_4}{(1+\alpha_1)(1+\alpha_6)} \cdot \frac{z^2 - \left(2 - \dfrac{\alpha_2\alpha_5}{\alpha_4}\right)z + 1}{\left(z - \dfrac{1}{1+\alpha_6}\right)\left(z^2 - \dfrac{2+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z + \dfrac{1}{1+\alpha_1}\right)}. \quad (6)$$

Strictly speaking, (6) does not represent an elliptic transfer function, since there is no transmission zero at $z=-1$ (corresponding to $s\to\infty$). However, if f_c is much larger than the passband frequency f_p, the effect of the missing zero on the passband response will be small. For example, if $f_c/f_p = 40$, the passband distortion is less than 0.03 dB.

The circuit of Fig. 6 needs no S/H stage at its input, since the capacitor $\alpha_3 C_1$ acts as a S/H device.

IV. High-Pass Notch Filter

Replacing the input capacitor $\alpha_3 C_1$ in the circuit of Fig. 6 with an unswitched capacitor, and adding a S/H section, the third-order high-pass circuit of Fig. 7 results. Its transfer function is given by

$$H(z) = \frac{-\alpha_3\alpha_4}{(1+\alpha_1)(1+\alpha_6)} \cdot \frac{(z-1)\left[z^2 - \left(2 - \dfrac{\alpha_2\alpha_5}{\alpha_4}\right)z + 1\right]}{\left(z - \dfrac{1}{1+\alpha_6}\right)\left(z^2 - \dfrac{2+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z + \dfrac{1}{1+\alpha_1}\right)}. \quad (7)$$

This function contains one zero at dc (i.e., $z=1$) and two conjugate-complex zeros on the unit circle, as well as three poles. It is thus suitable for a third-order elliptic high-pass

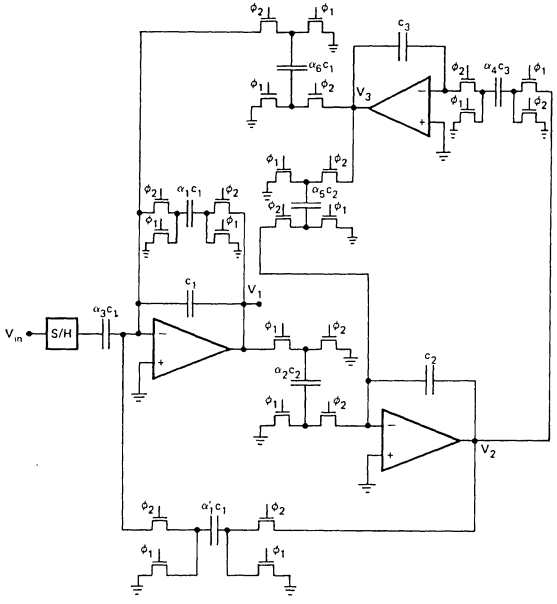

Fig. 8. Third-order elliptic high-pass filter with improved capacitor-ratio spread.

filter. If $\alpha_5 \to 0$, then $H(z)$ will have three zeros at dc, and hence can be used as the transfer function of an all-pole high-pass filter.

If the pole-Q's are very high and/or f_c/f_c very large, the natural modes of the circuit of Fig. 7 will be very close to the unit circle. This will result in a large spread of capacitor values in the circuit. Specifically, as (7) shows, the capacitance ratio α_1 is related to the magnitude r of the conjugate-complex pole-pair by the formula

$$\alpha_1 = r^{-2} - 1. \tag{8}$$

If $r \simeq 1$, then $\alpha_1 \simeq 0$ and the element values vary widely, making the circuit impractical.

To eliminate this undesirable effect, the circuit of Fig. 8 may instead be employed. Analysis shows that the transfer function is now

$$H(z) = \frac{V_1(z)}{V_{in}(z)} = \frac{-[\alpha_3/(1+\alpha_1)](z-1)[z^2-(2-\alpha_4\alpha_5)z+1]}{z^3 - z^2\left[2-\alpha_4\alpha_5+\frac{1-\alpha_1'\alpha_2}{1+\alpha_1}\right]+z\left[1+\frac{2-\alpha_4\alpha_5+\alpha_2\alpha_4\alpha_6-\alpha_1'\alpha_2}{1+\alpha_1}\right]-\frac{1}{1+\alpha_1}}. \tag{9}$$

Comparing the denominator of $H(z)$ with the natural-mode polynomial:

$$(z-\beta)(z-re^{j\theta})(z-re^{-j\theta}) = z^3-(2r\cos\theta+\beta)z^2 + (2r\beta\cos\theta+r^2)z-\beta r^2 \tag{10}$$

reveals that now (8) is replaced by

$$\alpha_1 = \frac{1}{\beta r^2} - 1. \tag{11}$$

Normally, $\beta < r$ and hence, even for $r \simeq 1$, α_1 will not be excessively small. Hence, this circuit will have a much smaller capacitance-value spread than that of Fig. 7.

V. Bandpass and All-Pass Sections

A second-order section which is suitable for bandpass filtering is shown in Fig. 9. Analysis gives for its transfer function

$$H(z) = \frac{-\alpha_3}{1+\alpha_1}\cdot\frac{(z-1)(z+1)}{z^2+\frac{2+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z+\frac{1}{1+\alpha_1}}. \tag{12}$$

(In the circuit $\alpha_4 = \alpha_3/\alpha_1'$ is assumed, and hence α_4 does not enter the transfer function.) Clearly, there are transmission zeros at $z = \pm 1$ which by (5) correspond to $s = 0$ and ∞. Hence, the circuit can perform as a bandpass filter.

The circuit of Fig. 10, with some restrictions on its element values, can be used as an all-pass section. Its transfer function is given by

$$H(z) = \frac{-\alpha_3}{1+\alpha_1}\cdot\frac{z^2-\left(2-\frac{\alpha_1'\alpha_4-\alpha_5}{\alpha_3}\right)+\left(1+\frac{\alpha_5}{\alpha_3}\right)}{z^2-\frac{2+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z+\frac{1}{1+\alpha_1}}. \tag{13}$$

The condition which $H(z)$ must satisfy in order to have a constant magnitude on the unit circle is that for each pole z_p there be a corresponding zero at $(z_p^*)^{-1}$. Then, each factor $[\exp(j\omega T)-(z_p^*)^{-1}]/[\exp(j\omega T)-z_p]$ of $H(z)$ has a constant magnitude $1/|z_p|$ and hence the transfer function has the all-pass property. For the function given in (13), this condition results in the relations

$$\frac{\alpha_5}{\alpha_3} = \alpha_1, \quad \frac{\alpha_4}{\alpha_3} = \alpha_2. \tag{14}$$

Substitution in (13) then gives

$$H(z) = \frac{-\alpha_3}{1+\alpha_1}\cdot\frac{z^2-(1+\alpha_1)(2+\alpha_1-\alpha_1'\alpha_2)z+1+\alpha_1}{z^2-\frac{2+\alpha_1-\alpha_1'\alpha_2}{1+\alpha_1}z+\frac{1}{1+\alpha_1}}. \tag{15}$$

It can easily be verified that (15) describes an all-pass circuit. This makes the z-domain design of switched-capacitor phase correctors or delay lines possible.

VI. Sensitivities

Element-value variations affect the transfer functions of the described filter sections primarily by changing the values of the natural modes. A useful measure of these sensitivities can, therefore, be obtained by transforming the natural-mode (denominator) polynomial of $H(z)$ into that of an analog transfer function, using the bilinear s-to-z transformation given in (5). For a second-order

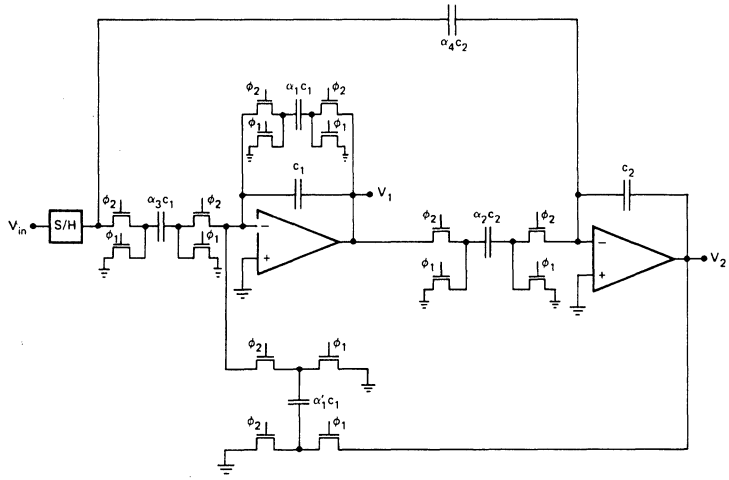

Fig. 9. Second-order bandpass filter.

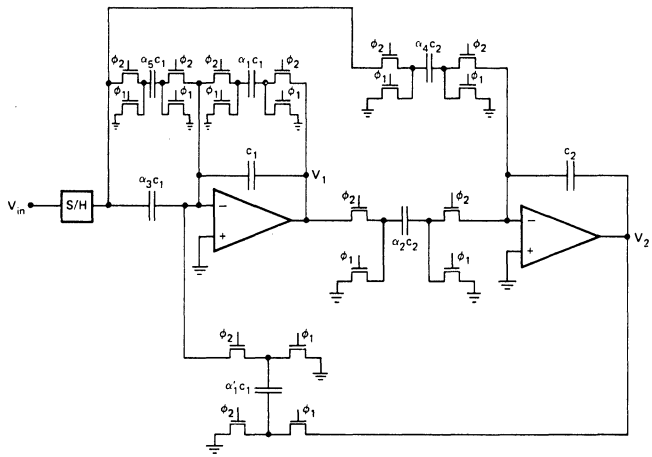

Fig. 10. Second-order all-pass filter.

section, this process gives an s-domain polynomial

$$P(s)=s^2+\frac{\omega_0}{Q}s+\omega_0^2. \tag{16}$$

Then, the logarithmic sensitivities

$$S_{\alpha_i}^{\omega_0}\triangleq\frac{\alpha_i}{\omega_0}\cdot\frac{\partial\omega_0}{\partial\alpha_i}$$

$$S_{\alpha_i}^{Q}\triangleq\frac{\alpha_i}{Q}\cdot\frac{\partial Q}{\partial\alpha_i} \tag{17}$$

will provide meaningful information on the effect of element value tolerances on the response. An inspection of (2), (4), (6), (12), (13), and (15) shows that the common form of most of the natural-mode polynomials of the described sections is

$$Q(z)=(1+\alpha_1)z^2-(2+\alpha_1-\alpha_1'\alpha_2)z+1. \tag{18}$$

Using (5) to transform $Q(z)$ into $p(s)$, and normalizing time and frequency so that $T=1$, we obtain

$$\omega_0=2\left[\frac{\alpha_1'\alpha_2}{4+2\alpha_1-\alpha_1'\alpha_2}\right]^{1/2}$$

$$Q=\frac{[\alpha_1'\alpha_2(4+2\alpha_1-\alpha_1'\alpha_2)]^{1/2}}{2\alpha_1}. \tag{19}$$

Differentiating ω_0 and Q, gives the logarithmic sensitivities

$$S_{\alpha_1}^{\omega_0}=-\frac{\omega_0^2}{4}\cdot\frac{\alpha_1}{\alpha_1'\alpha_2}\qquad S_{\alpha_1'}^{\omega_0}=S_{\alpha_2}^{\omega_0}=\frac{\omega_0^2}{4}\cdot\frac{2+\alpha_1}{\alpha_1'\alpha_2}$$

$$S_{\alpha_1}^{Q}=\frac{1}{4Q^2}\cdot\frac{\alpha_1'\alpha_2(\alpha_1'\alpha_2-\alpha_1-4)}{\alpha_1^2}$$

$$S_{\alpha_1'}^{Q}=S_{\alpha_2}^{Q}=\frac{1}{4Q^2}\cdot\frac{\alpha_1'\alpha_2(2+\alpha_1-\alpha_1'\alpha_2)}{\alpha_1^2}. \tag{20}$$

We turn now to the sensitivities of the finite nonzero transmission zeros. Inspection of (4), (6), (7), and (9) shows that the common form of the numerator polynomial $N(z)$ is

$$N(z)=z^2-\left(2-\frac{\alpha\beta}{\gamma}\right)z+1 \tag{21}$$

where, α, β, and γ are capacitor ratios. It can be seen that the magnitude of the zeros are not affected by α_i, and they remain on the unit circle for all α_i values. The transmission-zero phase-angle, θ_0, however, is affected by the element value tolerances and its logarithmic sensitivities can be found as

$$S_\alpha^{\theta_0}=S_\beta^{\theta_0}=-S_\gamma^{\theta_0}=\frac{1-\cos\theta_0}{\theta_0\sin\theta_0}. \tag{22}$$

Next, the limiting values of the sensitivities when pole-Q's are very high and/or f_c/f_p very large will be investigated. From (19) it can be seen that if the pole-Q is very high, then $\alpha_1\simeq 0$. The $\alpha_1 Q$ product, however, will have a finite value given by

$$\lim(\alpha_1 Q)|_{Q\to\infty}\to\frac{[\alpha_1'\alpha_2(4-\alpha_1'\alpha_2)]^{1/2}}{2}. \tag{23}$$

From (20) and (23), the maximum sensitivities for high-Q poles can be obtained as

$$S_{\alpha_1\max}^{Q}=-1 \qquad S_{\alpha_1'\max}^{Q}=S_{\alpha_2\max}^{Q}=0.5.$$

For cases when f_c/f_p is very large, ω_0 is very close to zero and as (19) suggests, $\alpha_1'\alpha_2\simeq 0$. From (19), $\omega_0/\alpha_1'\alpha_2$ has a finite value given as

$$\lim\left(\frac{\omega_0^2}{\alpha_1'\alpha_2}\right)\Bigg|_{\omega_0\to 0}\to\frac{2}{2+\alpha_1}. \tag{24}$$

Combining (20) and (24) gives the maximum ω_0 sensitivities as

$$S_{\alpha_1(\max)}^{\omega_0}=-0.5$$
$$S_{\alpha_1'\max}^{\omega_0}=S_{\alpha_2\max}^{\omega_0}=0.5.$$

The above results show that all sensitivities of the state-variable sections are within practically acceptable limits.

VII. Design Examples

The design of notch, low-pass, and high-pass filters will be described next, as an illustration.

Consider first the design of a switched-capacitor notch filter with the following specifications:

notch frequency: 60 Hz
3-dB bandwidth: 58 Hz
sampling frequency: 8 kHz.

The z-domain transfer function of the notch filter, obtained from applying (5) to an analog prototype, designed to meet the prewarped specifications is given by

$$H(z)=0.9777\frac{z^2-1.9978z+1}{z^2-1.9533z+0.9554}.$$

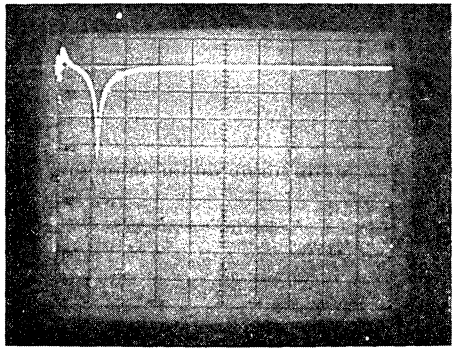

Fig. 11. Measured response of notch filter. Horizontal scale 50 Hz/div.; vertical scale 10 dB/div.

The capacitor ratios, α_i's, obtained from (4) are

$$\alpha_1=0.04668$$
$$\alpha_1'=\alpha_2=0.04688$$
$$\alpha_3=1.0233$$
$$\alpha_4=0.04802. \tag{25}$$

Using the corresponding α_i's in (20), the sensitivities turn out to be

$$S_{\alpha_1}^{\omega_0}=-0.01 \qquad S_{\alpha_1'}^{\omega_0}=S_{\alpha_2}^{\omega_0}\approx 0.5$$
$$S_{\alpha_1}^{Q}=-0.99$$
$$S_{\alpha_1'}^{Q}=S_{\alpha_2}^{Q}\approx 0.5$$
$$S_{\alpha_1'}^{\theta_0}=S_{\alpha_4}^{\theta_0}=-S_{\alpha_3}^{\theta_0}=0.5.$$

A discrete prototype of a circuit shown in Fig. 4 with the corresponding capacitor ratios given in (25) was constructed, and the corresponding measured frequency response is shown in Fig. 11.

Next, let it be required to design a switch-capacitor low-pass filter that meets the following specifications:

passband:	$0<f<3.3$ kHz	equiripple with 0.1-dB maximum deviation
stopband:	4.5 kHz $<f<\infty$	minimum stopband loss = 37 dB

clock frequency = 128 kHz.

A two stage state-variable configuration was chosen for the circuit. One stage was the second-order circuit shown in Fig. 4 and the other, was the third-order filter section shown in Fig. 6. By cascading the two sections, a fifth-order elliptic filter was obtained. The complete circuit was then fabricated as a CMOS integrated circuit. Fig. 12 illustrates the measured loss response of the filter.

Finally, the design of a high-pass filter with the following specifications will be considered:

passband:	$680<f<\infty$	equal ripple 1.2-dB maximum deviation
stopband:	$0<f<450$	minimum loss = 45 dB

clock frequency = 28 kHz.

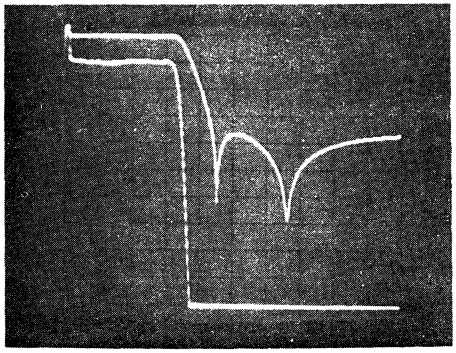

Fig. 12. Measured response of fifth-order elliptic low-pass filter. Horizontal scale 1 kHz/div.; vertical scale, top trace 10 dB/div.; bottom trace 1 dB/div.

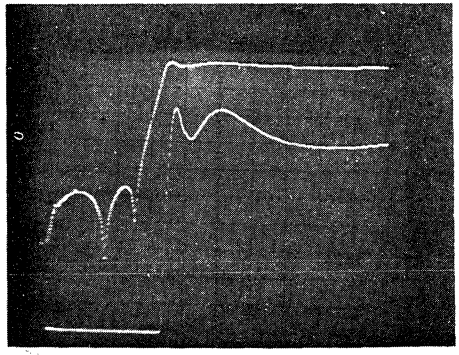

Fig. 13. Measured response of fifth-order elliptic high-pass filter. Horizontal scale 200 Hz/div.; vertical scale, top trace 10 dB/div.; bottom trace 1 dB/div.

A fifth-order elliptic transfer function was used to realize the filter. It consisted of two state-variable stages, one, a second-order circuit, as shown in Fig. 4, and the other a third-order filter stage shown in Fig. 8. The design was carried out in two steps. First, the critical frequencies (zeros and poles) were found using the bilinear z-transform. Next, the poles and zeros of the transfer function were paired in an optimum maner. In assigning the poles to zeros, the objective was to minimize the in-band loss of the overall filter, and to maximize its dynamic range. The free parameters in the transfer function were used to scale the gain of each stage such that the maximum gain values were the same for all five op amps.

The natural mode polynomial for the third-order section which had the highest Q ($Q \sim 10$) is given by

$$Q(z) = (z - 0.6284)(z^2 - 1.9608z + 0.984).$$

For the circuit of Fig. 7 the value of α_1 given by 8 is, $\alpha_1 = 0.0163$, resulting in a capacitor-value spread of 62:1. To eliminate this undesirable effect, the circuit of Fig. 8 was employed instead. The value of α_1 for this circuit is, $\alpha_1 = 0.62$. The largest capacitor-value spread was 15.5:1, which is a factor of 4 improvement over the circuit of Fig. 7. This circuit was processed as a CMOS integrated circuit. Its measured frequency response as obtained from a spectrum analyzer is shown in Fig. 13.

VIII. Conclusions

The filter sections described in this paper provide an easy technique for designing switched-capacitor filters in a cascade form. All filters employ the state-space structure, and use modified integrators which are unaffected by parasitic capacitances.

The filters obtained using the discussed sections are moderately insensitive to element-value variations but not as insensitive as those designed by simulating doubly terminated reactance filters. They are simpler in design and structure, however, adequate for many (if not most) practical applications.

Acknowledgment

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Roubik Gregorian (S'76–M'77), for photograph and biography see page 512 of this Transactions.

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AP 401

Realtime spectrum analysis using a microprocessor peripheral

by Victor Godbole and Zaheer Ali

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REALTIME SPECTRUM ANALYSIS USING A MICROPROCESSOR PERIPHERAL

Victor Godbole

American Microsystems, Inc.
Santa Clara, California

Zaheer Ali

Commercial Telecommunications Corp.
Santa Maria, California

ABSTRACT

The realization of a fast-Fourier transform (FFT) processor for realtime spectrum analysis of voice-band signals using a single chip signal processing peripheral is described. The chip processes FFT algorithms to compute the discrete Fourier transform (DFT) of an N-point sequence by decomposing the sequence into shorter sequence DFT's.

The chip is a 16 bit microcomputer with architecture and instruction set optimized for digital signal processing. It features a 12 X 12 bit parallel multiplier pipelined to operate in a single instruction cycle of 300nsec. Designed as a microprocessor peripheral it allows efficient partitioning of system tasks in performing a variety of signal processing functions.

INTRODUCTION

Spectrum analysis is an important technique for analyzing voice-band signals in the field of telecommunications encompassing both voice and data transmissions. It is also widely used in measurement, bio-medical and faultfinding equipment. There are two basic approaches to spectrum analysis. In the swept frequency approach the input signal is mixed with a swept local oscillator in the input mixer. This mixing product passes through the IF bandpass filters and amplifiers. The detected output is displayed on the vertical axis of the CRT. The shape and bandwidth of the bandpass filters determine both the resolution of the spectrum analyzer and measurement bandwidth for noise measurement. In this approach the analysis is done in a serial manner, therefore, it is slow. On the other hand it is the most economical but generally used only in measurement. The second approach - the parallel analysis approach - is one where all frequency bands of interest are analyzed simultaneously. It is most suitable for realtime analysis. Obviously its implementation is much more complex. However, continuing advances in LSI techniques are making its use practical in areas where previously it was uneconomical.

Recent availability of single chip signal processors with architectures optimized for implementing multiplication intensive algorithms makes computations of DFT's to handle voice-band signals in realtime a practicality. The digital technique can replace the filter banks required in the parallel spectrum analyzer in many applications.

The hardware realization of an FFT processor for realtime spectrum analysis depends upon system considerations such as signal bandwidth and frequency resolution. The sampling rate Fs must be at least twice the bandwidth of the input signal according to the Nyquist criteria while frequency resolution is given by f = Fs/N where N is the transform size. For most voice-band signal processing a sampling rate of 8kHz is common with a frequency resolution of 20Hz considered adequate. To be an integer power of 2, N must then equal 512. The FFT processor must be able to execute the function within the time T = N/Fs or 64 msec. for the case of N = 512 and Fs = 8kHz. This time includes the FFT processing time as well as the time required for transfer of data between the FFT processor and the Input/Output memories.

Conventional microprocessors lack the needed arithmetic power and speed to handle all of the system tasks involved in realtime spectrum analysis. An efficient organization is one where the microprocessor controls data collection and flow of data to and from a specialized FFT processor. The FFT processor in turn must have an architecture optimized for efficient implementation of the highly multiplication intensive FFT algorithm. The signal processing peripheral described in this paper has the necessary architecture to implement a 512 point complex FFT processor for voice-band signals in realtime in conjunction with a conventional microprocessor.

THE SIGNAL PROCESSING PERIHPERAL (SPP)

The SPP has previously been described in detail in references (1) through (3). The device consists of a 12 X 12 bit parallel pipelined multiplier, a 256 word X 16 bit data memory, a 256 word X 17 bit instruction ROM, ASU and microprocessor interface port. The data memory is novel in that it is partitioned equally in half RAM, half ROM. This is particularly useful for storing of variable signal data in the RAM portion and fixed coefficients in the ROM portion. The instruction format is dual operand with many multifunction instructions available. The basic operation of reading two values from the data memory, multiplying them, performing an airthmetic operation on the product and storing the result into the data memory can be done in one instruction cycle time of 300nsec. This is vital in providing computational efficiency in the implementation of FFT algorithms. It is obvious that the SPP does not have enough data memory to store 512 complex data points simultaneously. It was

necessary to develop a technique to break down the larger transform into smaller transforms such as a 32 point transform at a time. It was necessary to select the right kind of FFT algorithm to achieve efficiency and to maximize dynamic range and signal to noise ratio for the given architecture.

SELECTING THE FFT ALGORITHM

To calculate an N-point DFT, $(N-1)^2$ complex multiplications and N(N-1) complex additions must be performed. This follows from the equation

$$X(n) = \sum_{k=0}^{N-1} X_0(k)e^{-j2\pi nk/N}, n = 0, ---, N-1$$

$$= \sum_{k=0}^{N-1} X_0(k)W_N^{nk}, \text{ where } W_N = e^{-j2\pi/N} \quad (1)$$

observe that $W_N^0 = 1$, reducing the actual number of complex multiplications required to $(N-1)^2$ rather than N^2.

The FFT algorithm takes advantage of the property of the DFT when N is an integer power of 2 to reduce the number of complex multiplications to $\frac{N}{2}[\log_2 N]$ and the number of complex additions to $N \log_2 N$. It achieves this by successively decomposing the N point DFT in shorter sequences of DFTs until the length of the decomposed sequence is 2. The fundamental 2 point transform is called a butterfly. To compute an N point DFT, $\frac{N}{2}[\log_2 N]$ butterfly operations must be performed. The DFT can be decomposed with either a decimation-in-time (DIT) or decimation-in-frequency (DIF) algorithm to obtain the values. The DIT butterfly combines the two complex input points A and B to deliver two complex output points X and Y in accordance with the following equations

$$X = A + WB \qquad Y = A - WB \quad (2)$$

while the DIF butterfly takes the following form:

$$X = A + B \qquad Y = (A - B)\,W \quad (3)$$

W represents the complex coefficients.
Observe that in the DIF algorithm the complex multiplication is performed after the arithmetic operation.

Within the SPP the multiplier output is truncated to 16 bits. Better precision is obtained when using the DIF algorithm rather than the DIT algorithm. For this reason the DIF algorithm was selected. The basic form of equation (3) can be implemented to store each output in memory locations formerly occupied by its input data. An alternative to this "in place" geometry stores the results in a separate set of memory locations. This constant geometry algorithm has the advantages of a simpler indexing routine and a retention of the original data but has the disadvantage of requiring double the data memory (RAM). The size of the RAM is a major contributing factor to the overall chip size in a device like the SPP. The "in place" algorithm was selected to maximize the use of the RAM.

IMPLEMENTING THE ALGORITHM

Fig. 1 shows the data memory map for implementing a 32 point complex FFT within the SPP. The 32 X 4 addresses of the RAM section are used to store the 32 complex input data points, various control parameters, variable coefficients needed for FFT computations and the 32 complex and power spectrum output data points. The ROM portion holds the fixed coefficients from which variable coefficients needed for a particular computation sequence are generated. These include the sine and cosine values for the basic 32 point FFT as well as the sine and cosine values of 16 incremental angles which allow generation of coefficients for transform sizes to 512 points. Since the SPP can only operate on 32 data points at a time, the larger transforms are decomposed into shorter 32 point sequences. The signal flow graph for the N point FFT is shown in Fig. 2.

The SPP instruction ROM holds various routines to compute FFTs of any size from 32 to 512 points. The FFT32 routine is the basic routine which computes the complex FFT of 32 points. For a 32 point transform this is executed once. For larger size transforms this routine is executed on the final decomposed 32 point arrays. The COMPAS routine is the decomposition routine that breaks up larger arrays into a number of 32 point arrays to be executed by FFT32. The N data points are split into N/16 blocks of 16 points and pairs of blocks are executed by COMPAS according to the signal flow graph of Fig. 2. For an N point FFT the COMPAS routine is executed MN/32 times where $M = [\log_2 N - 5]$. This is followed by N/32 passes through the FFT32 routine on the final decomposed arrays.

There are additional routines such as WINDOW and SCALE, etc. for enhancing system performance. For instance the WINDOW routine permits use of an arbitrary weighing function on the input data points. The SCALE routine is used in conjunction with the conditional array scaling (CAS) feature provided on the chip.

Without the use of CAS the maximum resolution obtainable is approximately 57dB. CAS operates by detecting overflow in the butterfly computation routine. As soon as an overflow is detected the two points being combined in that butterfly are halved in magnitude and the butterfly recomputed. A flag is set, all previously computed butterfly outputs are scaled and all the inputs to subsequent butterflies are scaled before computation begins, so that at the end of the pass all points have been scaled equally. A scale factor (SCOUT) is made available so that the remaining data points in larger transforms may also be scaled equally. Thus, CAS operates as a discrete AGC and improves the dynamic range to about 70dB.

HARDWARE REALIZATION

The SPP is designed to interface with a conventional 8 bit or 16 bit microprocessor. It appears to the host processor as a memory mapped peripheral occupying a block of 16 addresses. Since all the necessary routines to compute FFTs of any

size from 32 to 512 points are in the SPP the host processor only needs to control data I/O and calling of specific routines in the necessary sequence. A typical system configuration is shown in Fig. 3.

Signal to be analyzed is first bandwidth limited by a low pass filter and then digitized by an A/D converter at the desired sampling rate. Data is collected by the microprocessor and stored in the input memory. The input memory consists of two sections. One section collects data corresponding to N sample points while the data previously collected in the second section is sent to the SPP for FFT processing. At the end of each cycle (T=N/Fs) the memories exchange roles. Similarly, on the output side a two section memory is used. Output data from the SPP is transferred to one memory section while the data in the other section is supplied to the D/A converter at the sampling rate. This pipelining of input and output memories makes continuous processing of signals in realtime possible. Another low pass filter is used to smooth the D/A converter output before it is displayed on the vertical axis of the CRT.

It is to be noted that the FFT computations produce results that are scrambled. To unscramble the data the order of the address bits must be reversed. This bit reversing can be done in hardware by use of multiplexers. A hardware bit reverser is essential for high speed. Bit reversing is performed only on the final outputs produced by FFT32 routines.

It is also obvious that the larger the transform size the larger the number of block transfers necessary between the host processor and the SPP. For an N point FFT the number of block transfers is given by $n = [(\log_2 N)-4]N/16$. The basic execution time within the SPP then becomes negligible compared with the time needed for data transfer. For highest possible speed a Direct Memory Access (DMA) technique can be used. Alternatively a multiple SPP array can be used to process the 32 point blocks within the N point sequence in parallel. There are also intermediate sequential & parallel combinations possible using fewer chips.

The control software required for an N point FFT is minimum and can be entirely contained within a standard 2k byte EPROM or ROM. The basic functions of the software are to load input data points and control parameters into the SPP, initiate execution of either the COMPAS or FFT32 routine and wait for interrupt. The SPP requests interrupt service on the IRQ line after completion of each routine. The output data points are then unloaded and passed to the output memory using the bit reversal hardware if the output is the final sequence produced by FFT32 routines. Additional functions such as CAS and windowing can be included to enhance system performance.

PERFORMANCE

The maximum execution times for various transform sizes along with signal bandwidth possible are shown in Table 1. The actual execution time when CAS is enabled will be between the times shown for CAS off and the maximum with CAS on. It will depend on the number of times that scaling has to be done. The execution times are shown for direct data transfer using an S6802 microprocessor with a 4MHz crystal (1μsec cycle time) and also when using DMA to transfer data at 4M bytes/sec.

Results show that without using a DMA technique to speed up data transfer a transform size of only 32 points can be handled for realtime voice-band signal processing. With the DMA, however, maximum frequency resolution with a 512 point transform can be obtained over the entire voice-band.

Use of CAS gives a total dynamic range of about 70dB. The maximum resolution obtainable is about 57dB.

SUMMARY

A programmable signal processing peripheral coupled with a conventional microprocessor is able to perform realtime spectrum analysis of voice-band signals with economy and efficiency due to its specialized architecture and partitioning of system tasks. The microprocessor handles data collection and the flow of data to and from the signal processor while the signal processor executes an FFT algorithm to compute the DFT of an N point sequence.

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TRANSFORM SIZE	BLOCK TRANSFER USING S6802 (22μsec/word) EXECUTION TIME (msec) MIN	MAX	MAXIMUM SIGNAL BW (kHz)	BLOCK TRANSFER USING DMA (2nM/sec) EXECUTION TIME (msec) MIN	MAX	MAXIMUM SIGNAL BW (kHz)
32pt	4.0	4.6	3.4	1.3	1.9	8.4
64	14.2	15.7	2.0	3.2	4.6	6.9
128	40.7	44.0	1.4	7.6	11.0	5.8
256	106	114	1.1	17.8	25.4	5.0
512	262	280	0.9	40.7	57.9	4.4

Table 1 Tranform Size vs. Execution Times and Signal Bandwidth

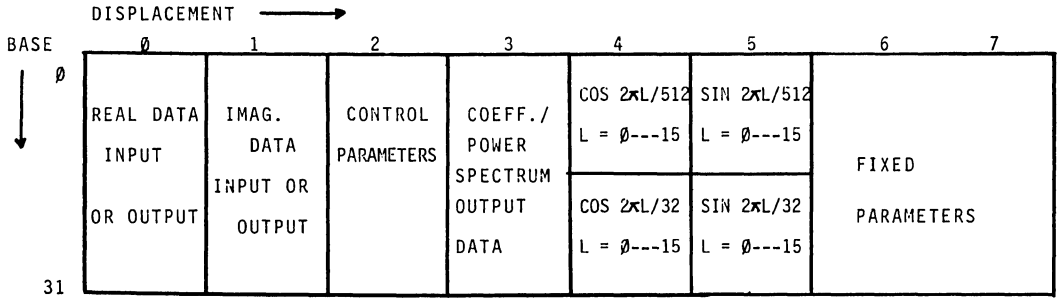

Fig. 1 Data Memory Map of SPP for FFT Processing

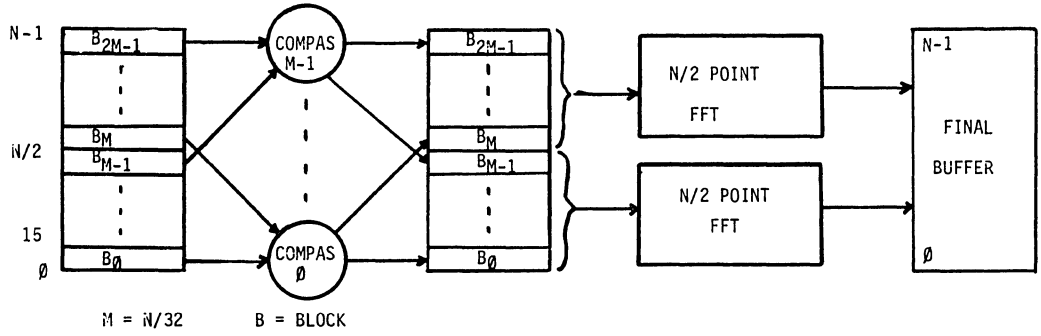

Fig. 2 Signal Flow Graph for N Point FFT

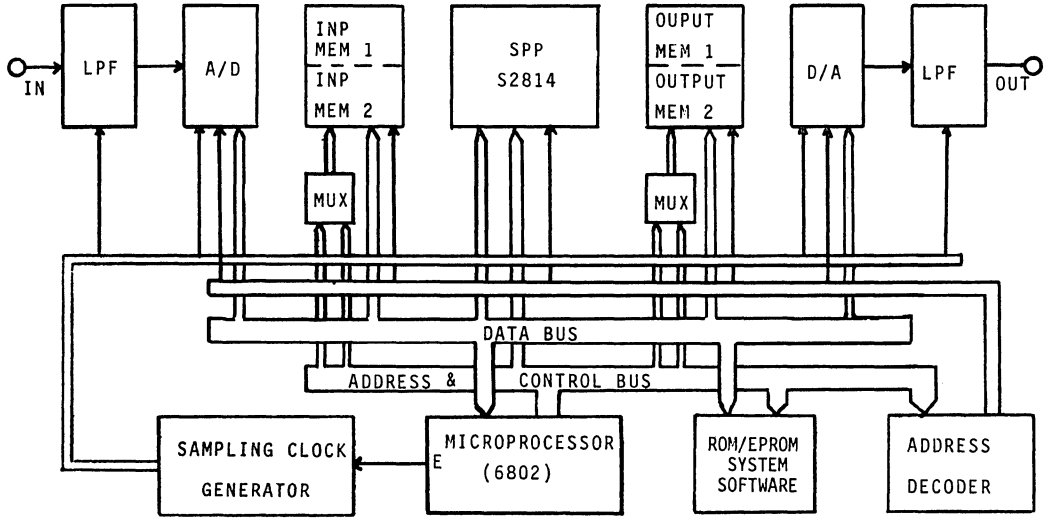

Fig. 3 A Typical System Configuration

A speech/speaker recognition and response system

by Gwyn P. Edwards

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A SPEECH/SPEAKER RECOGNITION AND RESPONSE SYSTEM

Dr. Gwyn P. Edwards

American Microsystems, Inc.
Santa Clara, California

ABSTRACT

The realization of a speech analyzer plus an LPC synthesizer in a single chip signal processing microprocessor is described. The chip is able to process both algorithms in real time to create an interactive voice analyzer/response system operating under the control of a microprocessor and with the LPC speech data stored in a ROM.

The chip is a 16 bit microprocessor specially architectured for signal processing. It features all single cycle instructions with a 300nsec cycle time, and a 12 x 12 bit parallel multiplier pipelined to operate in a single cycle. It can be programmed to perform a wide variety of signal processing functions including speech processing.

Introduction

The combination of speech processing research and present semiconductor technology have at last made it possible to realize all the signal processing functions of a speech/speaker recognition plus voice response system on a single IC chip, the AMI S2811 Signal Processing Peripheral. Further, that chip is a programmable non-dedicated function, the signal processing equivalent of a microprocessor. The addition of a program plus a control processor with additional memory and analog interface circuitry turns this device into a powerful but extremely compact speech analyzer and synthesizer. In addition, the availability of a real time in-circuit-emulator, the RTDS2811, allows experimental work, and program development to be carried out in the laboratory with the minimum effort. This is invaluable in speech processing, where results are so subjective and indefinitive.

The Signal Processing Peripheral

The SPP has previously been described in detail (1), (2), (3), but a brief description of the essential features and architecture is given here. The architecture is shown in Fig. 1. The microprocessor-like structure will be immediately apparent. The device has a memory to memory instruction cycle of 300nsec. The interface circuitry consists of a parallel port utilizing an 8 bit bidirectional data bus, for ease of connection to the host microprocessor system, and also a completely asynchronous serial port. Serial data flow is controlled entirely by the external system, making interfacing to existing systems possible with minimum changes. Since the serial and parallel ports share the same Input and Output Registers, simultaneous use of the two I/O modes must be carried out on a time-shared basis.

From the Input and Output Registers the data path leads to the Accumulator Bus which interfaces the accumulator to the data memory and the I/O registers. Data flow on this bus is software controlled.

The data memory itself is interesting for two reasons. 1. It is split into equal quantities (128 words) of RAM and ROM. This is quite different from conventional microprocessor practice, and reflects the differences between data processing and signal processing. The ROM portion is used as a look-up table for coefficients, e.g. for digital filters, sine and cosine tables, etc. 2. The memory has two output ports, U and V. In the base plus displacement address modes (UV and US), which are equivalent to Indexed addressing in microprocessors, two data words may be accessed in one instruction cycle, one from each port. There is an addressing constraint that words to be accessed together must lie in the same base (block) of 8 words in the memory. Each base contains 4 words of RAM and 4 of ROM. In practice, the memory management needed to keep pairs of words in the same base will not be found difficult because of the flexible addressing modes available and by using the scratchpad, which is an 8 word all RAM addition to the memory, always accessible to the V port in lieu of main memory.

The Adder/Subtractor unit (ASU) is a 16 bit arithmetic unit using two's complement code. Multiplexers on its inputs are controlled by the software to provide flexibility. Its output is fed into the 16 Accumulator latches.

A special feature of the chip is the parallel multiplier. This is a two's complement multiplier (using Booth's algorithm) forming a rounded 16 bit product from two 12 bit inputs in 300nsec. Since the multiplier is loaded in one instruction cycle and the product loaded into the accumulator

in the next, this multiplication time is actually transparent to the user and adds very little overhead to the processing time of most algorithms.

The machine operates under the control of programs stored in the Instruction ROM. Since each instruction is a full read-modify write cycle, the 256 instructions are capable of executing programs that would take several times as many instructions in a conventional microprocessor and at a much higher speed, since each instruction is executed in just one 300nsec cycle. The power and flexibility of the instruction set is greatly enhanced by having separate operator sets for arithmetic functions and data manipulation. Both operators are executed in each cycle.

The power of the SPP is clearly shown in the fact that the biquadratic filter algorithm can be executed in 5 instruction cycles (1.5μsec) and a 32 complex point FFT can be executed in 1.5msec.

Speech/Speaker Recognition

The applications of the recognition of human speech by machine are as varied as the means of executing the function. Basically speech analysis may be split into two main categories. 1. Complete analysis of random continuous speech so as to permit regeneration of the speech by synthesis e.g. LPC, Formant, from the resulting parameters. 2. Partial analysis of either isolated words or continuous speech so as to permit feature identification by means of pattern recognition techniques. The requirements of the two systems are quite different, the latter typically attempting to "classify" the speech input with nearly an order of magnitude fewer bits than would be used for synthesis.

Analysis for recognition can itself be categorized into two sub-classes as already noted, namely the analysis of isolated words or utterances, and the far more complex analysis of continuous speech. In the latter case it is mainly the task of pattern recognition which becomes complicated, but this complication can be greatly reduced by improved analysis techniques. The scope of the remainder of this section will be limited to the subject of the analysis of isolated words, since this work is currently at an early stage. Again, this subject may be divided into two categories - speech (word) and speaker recognition, according to the application requirements. This division is a minor one, however, since the techniques involved are largely similar, and one system could be used for both purposes. However, a system to be dedicated to the former task could be optimized for that task by placing different emphasis on some of the analysis parameters relative to those in a system optimized to the latter task.

One of the big advantages of having a software definable system is being able to experiment with the system (using a real time emulator, in this case) and try out the various combinations of speech analysis parameters so as to yield an effective system that will operate within the constraints of the hardware. These constraints will include processing speed and memory limitations. The constraints will obviously pose limitations on the analysis techniques that may be implemented, since some of them e.g. LPC analysis, are very complex. Nevertheless, let us look at the parameters that should be considered. According to a survey carried out by Lea and Shoup (4) the best parameters, listed in order of preference, are:

- Formant frequencies, F_1, F_2, F_3
- Fundamental frequency, F_0
- LPC analysis
- Energy contours
- Poles of LPC spectrum
- Formant amplitudes
- Total spectrum
- Zero crossing counts
- Time domain analyses
- Formant Bandwidths

The order or preference shown is that for speech recognition, and might be changed slightly for speaker recognition. To attempt to analyze all of these parameters would not only be a formidable task for any system but also excessive, since many parameters duplicate some features of others, and in any case the consequent information (bit rate) would unnecessarily complicate the pattern recognition task to follow. Indeed, the entire problem balances delicately on being able to provide enough good analysis information to ensure reliable rejection of mismatches without making the matching problem so difficult that an unacceptably high rejection rate of matches occurs. The objective of the experimental work is to try to find this balance whilst simultaneously obeying the constraints of the system.

The ongoing work at AMI is pursuing these many techniques. In some cases novel approaches to the problem are being investigated, these being methods that exploit the capabilities of the S2811, notably its high speed execution of signal processing algorithms including the FFT. Since this work is still at a very early stage of development no results are available for presentation at this time.

Speech Synthesis

Unlike the techniques for speech analysis, those for synthesis are well documented (5), (6). The techniques most suited to low bit-rate synthesis are LPC and Formant synthesis. Given that the available data rate is of the order of 2Kb/sec it is generally agreed that LPC produces the more natural sounding and better quality speech in this range. Also, at such a data rate it is also well documented that the optimum LPC order is 10

and that the sampling rate should be in the region of 6 to 8 KHz. Reducing the sampling rate below 6KHz will obviously reduce the speech bandwidth excessively, producing dull, flat sounding speech, and increasing it above 8KHz results in too large a range for the distribution of the filter poles, resulting in a reduction of quality. Having set these parameters the remaining uncertainties in this area are the optimum techniques for reducing the data rate without significantly reducing the speech quality. These include frame repetition for extended sounds and the reduction of the LPC order to 4 during unvoiced speech.

The task of LPC synthesis is ideally suited to an SPP system since it requires the control processor to access, decode and format the LPC parameters at a relatively slow speed (once during each 20msec. frame). The SPP itself then computes the speech samples, a highly arithmetically oriented task, at the much higher rate of 6 to 8K samples/sec. The parameters are loaded into the SPP using the block transfer mode, and parameter interpolation is carried out within the SPP at four times the frame rate. The actual effective input data rate to the synthesizer itself is 9.6Kb/sec. The compacting of data from this rate to 2Kb/sec. is carried out by non-linear quantization of the parameters (7). This is a technique that allows the LPC parameters themselves to be specified by a smaller amount of data using a ROM look-up table. This function is carried out by the control microprocessor.

The System

It has not been the purpose of this paper to present new ideas in speech processing techniques, but rather to show how existing techniques can be married to newly available hardware to realize a speech/speaker recognition and voice response system at much lower cost than previously possible. The resulting system is shown in block form in Fig. 2. Incoming data from the A to D converter is stored in the buffer memory prior to analysis. The memory is split into two blocks of 256 bytes each, and one is loaded while the contents of the other are being processed. If the total analysis time does not exceed 32msec. per block then the processing is effectively carried out in real time, assuming a sampling rate of 8KHz. After feature extraction has been carried out the resulting data is matched against the reference patterns held in memory. Non-linear time warping is used to assist in this task. This is carried out in the control processor. The voice response to speech input is then synthesized using LPC from parameters held in memory, and the resulting output samples fed into the D to A converter.

The realization of the system is shown in Fig. 3. The signal processing (analysis and synthesis) is carried out in the S2811 Signal Processing Peripheral. The device can be switched to execute either the analysis routines or synthesis routine by the S6805 microcomputer. It is not possible to execute both functions simultaneously because of the limitations of the internal read/write memory of the SPP but this is not generally required if the device is to operate in a conversational (half duplex) mode. The synthesizer is only switched in to give a response and then switched out again. During response time the system is deaf, but this avoids the problem of acoustic feedback. All data processing, including overall control, timing and comparison is carried out by the microcomputer.

A novel approach to the interfacing is the use of a μ-law codec pair for A to D and D to A conversion. This gives 3 advantages, at the expense of requiring μ-law to linear and linear to μ-law conversion, but this is easily carried out in the SPP.

1. It gives the input a large dynamic range while restricting the data to be stored in the buffer memory to 8 bit words.

2. It allows direct PCM input/output where this can be used.

3. The Codec chip pair is inexpensive and incorporates anti-aliasing filters.

The memory block for storing the reference patterns and LPC parameters is deliberately unspecified because it is application dependent. It can be realized as RAM, ROM or EPROM as required, and the size will depend on the amount of storage required for both reference patterns and LPC parameters.

Summary

The system presented is able to perform the function of speech/speaker recognition with voice response at lower cost and in a smaller space than previously possible due to the capabilities of the S2811 Signal Processing Peripheral. Since this chip is a non-dedicated processor it finds possible applications in a wide range of signal processing areas. It signals the arrival of a new breed of hardware that promises to revolutionize signal processing in the same way that the microprocessor is now revolutionizing data processing.

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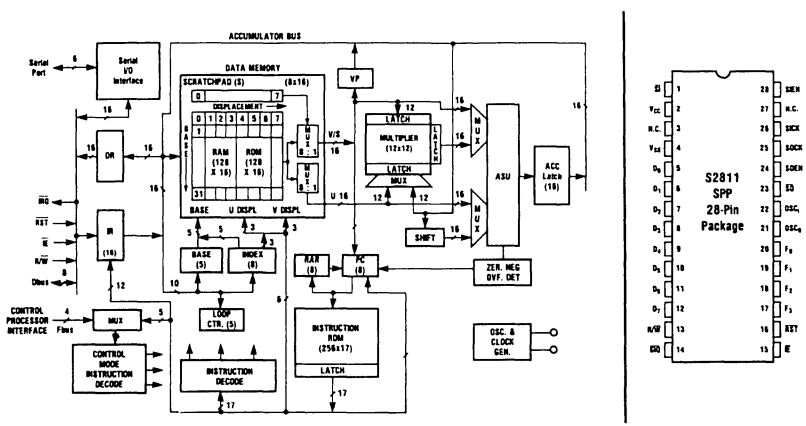

FIG. 1. ARCHITECTURE AND PINOUT OF SIGNAL PROCESSING PERIPHERAL

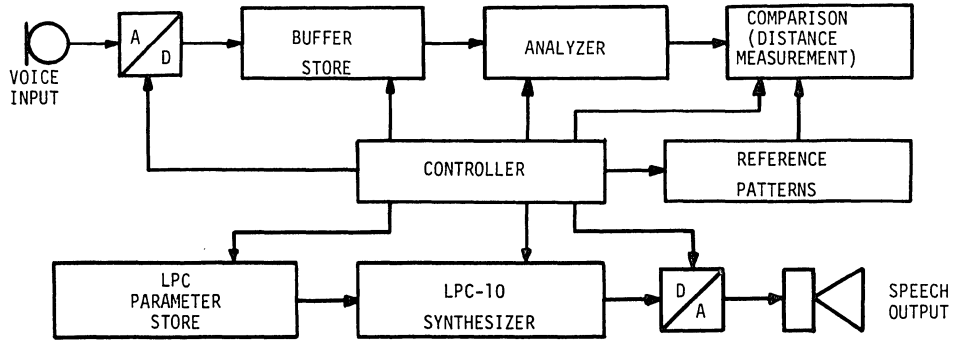

FIG. 2. BLOCK DIAGRAM OF SPEECH/SPEAKER RECOGNITION AND RESPONSE SYSTEM

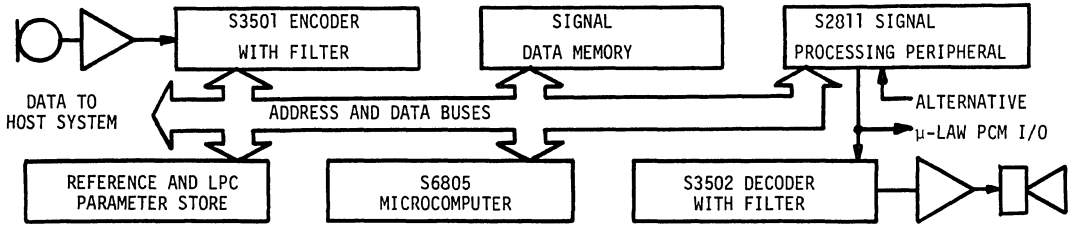

FIG. 3. REALIZATION OF SYSTEM, USING SIGNAL PROCESSING PERIPHERAL

The implementation of a speech synthesis algorithm

by Gideon Amir, Roubik Gregorian, and Gwyn Edwards,

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THE IMPLEMENTATION OF A SPEECH SYNTHESIS ALGORITHM

Gideon Amir, Roubik Gregorian, Gwyn Edwards

American Microsystems, Inc.
Santa Clara, CA 95051

ABSTRACT

The application of integrated circuit technology to Speech Synthesis and Recognition represents an important development in the field. This paper describes a complete Speech Synthesis System on a single chip. The considerations involved in the choice of a compatible algorithm, machine word length and coefficient accuracy are discussed. The device contains a 32 word vocabulary and an innovative implementation of the LPC lattice structure. It operates at a variable bit rate to provide high quality speech with low bit storage requirements. The software supporting the Speech Synthesis System is also described.

INTRODUCTION

The implementation of Speech Synthesis algorithms in integrated circuits has been one of the most important developments in the field of speech processing. The purpose of this paper is to illustrate the impact of LSI and the demands that it makes on this field. The development of the S3610 Speech Synthesizer and the considerations taken in the design, will be described here to demonstrate this interaction between LSI and Speech Processing Theory.

Choosing an Algorithm

Several Integrated Circuits now on the market demonstrate the difficulty involved in choosing an optimum algorithm. While some manufacturers chose LPC (1) or its PARCOR relative (2), one Semiconductor company has invented its own algorithm based on a new method of waveform coding (3) and another used the formant approach. Clearly, each manufacturer arriving at a different algorithm indicates the difficulty involved in choosing the best one for the application. The S3610 is using LPC for several reasons:

1) Software Support: Linear prediction theory and application to speech processing was found to be highly advanced (4) with substantial studies to support analysis of speech and quantization of parameters with minimal human intervention in the process.

2) High quality of speech vs. bit rate: When compared with other methods LPC was found to have low bit storage requirement for the desired speech quality when a wide range of speakers was considered (including foreign languages, female and child voices as well as non-human sounds). Admittedly, this aspect of algorithm selection warrants additional research.

3) Complexity of Circuit Design: All approaches can be implemented using a digital solution (with D/A conversion for voice output). The use of Analog filters for Formant Synthesis or an Analog D/A multiplier as in the S3610 described below offers some interesting advantages.

4) Compatibility of Analysis Method to LSI: The S3610 Speech Synthesizer chip was assumed to be part of a system that in the future will offer integrated analysis functions as well. The algorithm chosen, therefore, had to be compatible to LSI in both Synthesis and Analysis. While the formant approach represents some serious problems in that regard, the Waveform Coding would seem the simplest. Unfortunately, the compression techniques required here to produce low enough bit rate involve high level of computational power which cannot be easily integrated. The LPC algorithm again, seemed to be most promising and was, therefore, adopted for the S3610.

The Application

The application of the LSI Speech Synthesizer bears heavily on the design approach to be selected. While some applications require minimum vocabulary with natural sounding speech (toys, appliances, etc) others are aimed at open end vocabularies and/or economy of storage. A certain measurement of flexibility seems to be necessary for most applications where higher quality can be achieved by sacrificing storage space. The operating environment is also of importance determining design objectives such as power supply range, operating and standby currents and package size. The LSI designer will essentially have to meet three main objectives:

1) Economy: The final cost to manufacture the product which is primarily governed by the die size, the process, the testing and the packaging of the chip.

2) The quality of speech desired.

3) The operating environment - which in turn impacts the process selected and the economy.

In the design of the S3610 a high quality of speech acceptable to the consumer, automotive and professional applications was desired. A battery operated environment with wide range of power supply and low stand-by current was assumed which motivated the choice of a CMOS process. To meet

the economy requirement with the relatively expensive CMOS process and on chip storage capability of up to 32 words, an innovative circuit design approach to the LPC lattice structure was adopted.

SPEECH SYNTHESIS ON A SINGLE CHIP

The S3610 Speech Synthesizer block diagram is shown in Figure 1. The chip is divided into 3 main parts: The Front End block includes the input logic and timing, the Speech ROM containing 20,5kbs of speech data, the coefficient dequantization PLA and the interpolation logic.

The LPC Filter block contains the multiplier and lattice delay circuits and the voiced and unvoiced excitation sources. Finally, the Back End block includes a three pole smoothing filter and a balanced output audio amplifier.

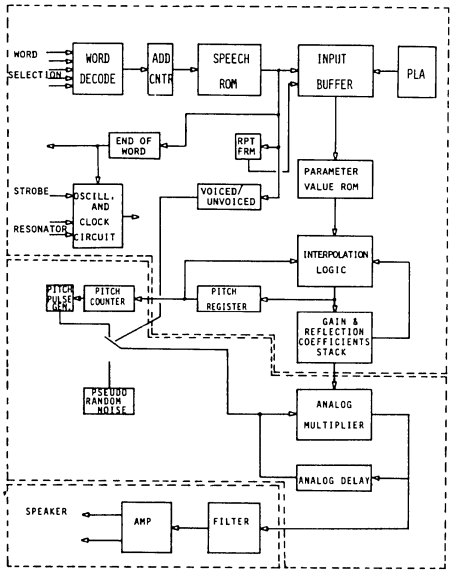

Fig. 1 Speech Synthesis System on a Single-Chip - Block Diagram

On-Chip ROM

As mentioned before the S3610 was designed to include a vocabulary of up to 32 words or utterances. This was accomplished by an on chip, very dense, mask programmable Read Only Memory (ROM) capable of storing 20408 bits organized in 2560 bytes. The byte organization rather than serial output was preferred to enable direct interface with external ROM's with the standard "by-eight" organization. This, however, placed some restrictions on the frame size, having to be a multiple of 8.

Choosing Frame Size

The frame update rate was chosen to be 50Hz which combines with four linear interpolation cycles to provide a sufficiently high update rate of 200Hz. The normal frame rate of 10ms was thus cut in half without sacrificing quality. With the 50Hz frame rate a maximum frame size of 40 bits was chosen yielding a bit rate of 2000bps. This bit rate was found to be sufficient for high quality speech with room for further bit-rate reduction in special cases as will be described below. A larger frame of 48 bits would have resulted in too high a bit rate for a marginally improved speech quality.

Parameter Quantization

The order of the LPC filter now had to be determined. With the 40 bit frame size providing for Pitch, Gain and Reflection Coefficients information, a filter size of more than 10 poles is redundant. Even so too few bits were available to directly quantify the parameters. A further complication is the fact that optimum quantization is nonlinear (5). To solve these problems a parameter ROM is included on the chip containing quantized values of each of the 10 Reflection Coefficients as well as the Pitch and Gain Parameters. The Parameter ROM word length was set to 9 bits since higher accuracy did not result in a perceptible improvement of speech quality. The machine uses fixed point arithmetic and all numbers are stored in 2's compliment format and are less than 1 in magnitude.

The Bit allocation within a frame is derived at the same time as the coefficient quantization values and is programmed in the PLA controlling the input buffer and parameter ROM addressing.

Bit Rate Reduction

At 2000 bits/second, a fixed frame length format still wastes a great deal of information. During unvoiced frames a filter order of 4 was found quite adequate, furthermore the pitch information is obviously unnecessary. The byte oriented frame can, therefore, be shortened from 5 to 3 bytes as shown in Figure 2. The frequent redundancy in the speech itself is also taken advantage of by repeating the reflection coefficients of frames with spectral distance (6) of 2db or less. This reduces the frame length of repeat frames to a single byte containing only gain and pitch information. The single byte repeat frames can be repeated as many times as necessary enabling the system to operate at a minimum bit rate approaching 400b/s. This feature is very useful when using the synthesizer to generate tones. Finally, a single null

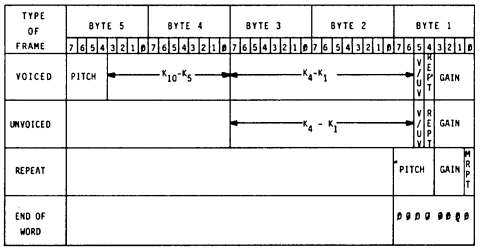

Fig. 2 Frame Format in the S3610

byte signals the end of word and provides for automatic shut down of the system. With the variable frame length system the average bit rate produced by the chip is 1200b/s. With 20.5kb of ROM on chip the average bit rate produced by the chip is 1200b/s. With 20.5kb of ROM on chip the average vocabulary will last about 17 seconds.

The LPC Filter

There are several ways to implement the LPC lattice filter on a chip. Using an all digital design the TI pipeline Booth's algorithm implementation (1) requires a very large portion of the chip area while providing 14 bit accuracy. A serial multiplier approach can be used in a two multiplier structure with much reduced chip area. The speed of operation, however, would go up requiring a much higher frequency clock. In addition, a digital approach still requires a D/A converter at the end. The S3610 design uses neither of these techniques. Instead, a high resolution analog switched capacitor multiplier is used as shown in Figure 3a. The two stage multiplier performs multiplication and addition simultaneously 20 times each sampling period with the intermediate results (B's) stored in 10 sample and hold circuits. The principl of operation of this multiplier has been discussed earlier (1) and will not be detailed here. It should be mentioned, however, that the whole structure requires much less area in CMOS than the Booth's algorithm multiplier uses in PMOS.

The accuracy of the Switched Capacitor multiplier is only limited by the analog circuit noise and leakage and computer simulations show it to be better than an equivalent digital multiplier of 11 bits. In order to improve the accuracy and Signal to Noise ratio some properties of the LPC lattice structure are used to advantage. It was found, for example, that $b_i \leq b_i/2$ for all $i \neq 1$, when b_i is the intermediate result as shown in Figure 3b. By multiplying the bi's by 2 before storing them in the sample and hold circuits and then dividing by 2 again when they are fetched by the multiplier an improvement of the signal to noise ratio of 6db is obtained. An extremely simple two's complement to sign magnitude conversion of reflection coefficients is also provided by the analog multiplier since a simultaneous addition of the LSB is easily done by simply adding one unit capacitor at the first multiplier stage. Another significant advantage of this multiplier is obviously the fact that its output, being analog, can be used to drive the output circuitry directly where the digital multipliers lose some of their accuracy driving a lower resolution D/A converter.

Excitation Sources

Several studies were made on the subject of the pitch pulse in LPC synthesizers. Even though no conclusive proof to the advantage of one pulse shape over another (as far as speech quality is concerned) was found, the S3610 was equipped with the Hilbert pulse pitch source shown in Figure 4. This pulse provides proper energy distribution and yet allows pitch frequencies as high as 800Hz without creating a DC offset. The Hilbert pulse, as well as the

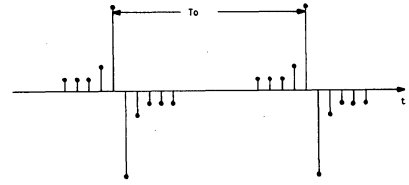

Fig. 4 Hilbert Pulse Excitation Used in the Pitch Source of the S3610.

unvoiced source amplitude are generated by a simple switched capacitor circuit and present the analog input Ui to the multiplier. Since the source's amplitude is referenced to the power supply, a proper tracking of input voltage with the dynamic range of the multiplier is obtained. The source amplitude can be programmed concurrently with the speech ROM and further optimization of Signal to Noise ratio can result. The unvoiced source sign is controlled by a pseudo-random shift register with a period of several hundred milliseconds to prevent correlation distortion in the output signal.

Output Filter and Amplifier

Taking advantage of the Switched Capacitor process used a smoothing filter was added at the output of the LPC filter. The three pole elliptic filter smooths the 8kHz sampled and held signal and adds Sin(x)/x compensation. The smoothed voice signal is brought out through a balanced, push-pull amplifier which is capable of providing 100mW to a 100Ω speaker and ceramic resonator to operate.

The complete chip was laid out using standard 5μ CMOS double poly process. A heavy depletion non-critical step was added for ROM programming. The total area of the chip came out to 30.6sq. millimeters.

SOFTWARE SUPPORT

Figure 5 shows the flow diagram of the analysis procedure which provides the ROM program for the S3610. The digitized speech data is first analyzed for the LPC Reflection Coefficients (using the Autocorrelation method) Pitch and Gain parameters. The analysis data is then used to drive a Speech Synthesis Program that simulates the LSI Synthesizer to a great detail including word length, dynamic range and even parasitic leakage effects. The results of this synthesis are listened to and analysis data edit procedure is followed until satisfactory speech quality is obtained. This edit cycle is optional and is intended to derive the best possible quality out of the hardware. The edited analysis data is then run through a bit rate reduction process which eliminates redundant information by repeating frames with spectral distance within the specified threshold. The quantization program then sets the final average bit rate of the speech sample. This bit rate is checked against the available bit storage space. If a mismatch occurs another

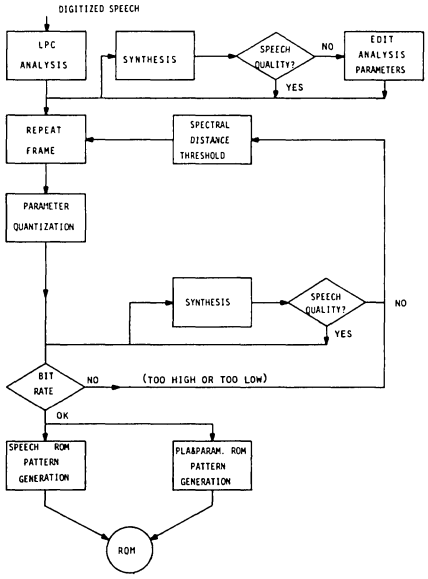

Fig. 5 ROM Pattern Generation Flow Chart

iteration through the bit rate reduction procedure is initiated by adjusting the distance threshold as required. The final analysis file is used to generate the ROM patterns for the speech ROM, the PLA and the Parameter ROM. In many cases, particularly when the same speaker is involved, new vocabularies can be generated without changing the parameter ROM. In these cases an external ROM may be used to expand the vocabulary beyond 32 words. The external ROM version of the synthesizer, the S3620, is identical to the S3610 except for the interface provided for an external byte oriented ROM.

CONCLUSION

The speech synthesis system on a single chip described in this paper demonstrates the interaction between speech processing research and semiconductor technology. As expected, some modifications and compromises are required to be able to integrate speech synthesis algorithms on silicon but the results are very encouraging and point toward further development and cooperation between the Semiconductor and Speech and Signal Processing Communities.

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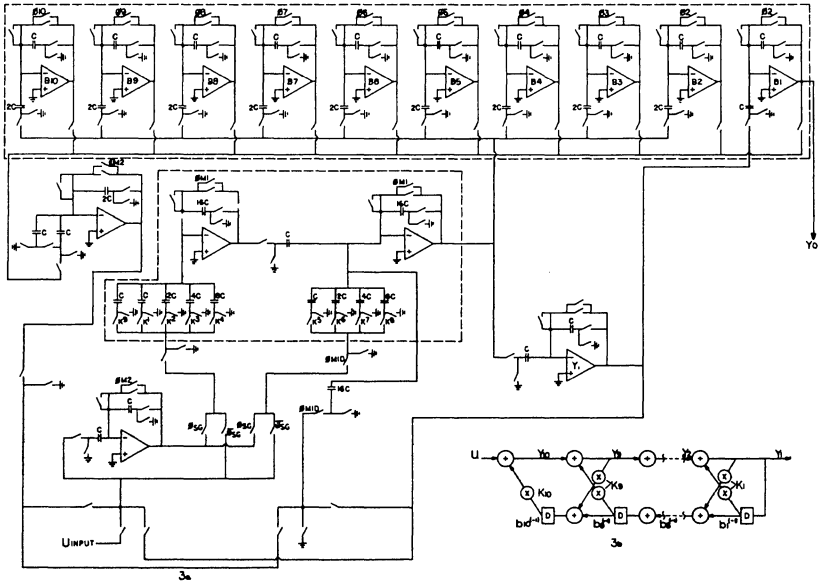

Fig. 3 Analog Implementation of a 10 pole LPC Filter (3a) and Equivalent Lattice Structure (3b)

AMERICAN MICROSYSTEMS, INC.

AP 601

NMOS and CMOS A/D LSI performance/cost trade offs

by Roger Mao, Yusuf Haque, Richard Nedbal, Bill Nicholson and Roubik Gregorian

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NMOS and CMOS A/D LSI Performance/Cost Trade Offs

Roger Mao, Yusuf Haque, Richard Nedbal
Bill Nicholson and Roubik Gregorian

American Microsystems, Inc.
3800 Homestead Road
Santa Clara, CA 95051

Introduction

MOS Technology is showing itself to be a viable competitor in satisfying the LSI digital/analog market. Either NMOS or CMOS can be selected to satisfy the I.C. design, but each has its own unique performance/cost tradeoffs. It is important to choose the proper boundaries between the analog and digital functions (e.g., filter implementation), and to select the appropriate converter or interface technique (e.g., dual slope integration vs. capacitor charge distribution). Two devices, a CMOS CODEC and an NMOS D/A-A/D microprocessor, have been chosen as examples of today's MOS LSI digital/analog capabilities.

Viability of MOS Digital/Analog LSI

MOS Technology has proven itself to be the leader in innovative LSI digital technology and the forerunner of ever increasing chip density. Cases in point are memory and microprocessor devices. Quantitatively, a recent survey of 115 microprocessors (including generic devices) revealed that 89% of the available devices were fabricated in MOS Technology and with the remaining 11% fabricated in BJT (bipolar) technology. Of this 89%, 38% were processed in PMOS, 41% in NMOS, and 10% in CMOS. Today, MOS is penetrating the frontiers of the analog domain and is proving itself to be a strong contender in many application areas previously served by BJT analog technology. The application areas of greatest interest are those involving a mixture of both MOS high density digital and analog circuitry, and products of this type are proving themselves to be very cost and performance competitive with BJT I^2L devices. Greater diversification in function is now being accommodated by MOS, and perhaps one reason is the greater effort required in designing and simulating LSI BJT circuitry. In certain high performance circuits BJT analog Technology has and will continue to have an edge over MOS. This is due to its inherent higher speed and drive capabilities as well as its lower noise and offset characteristics. However, MOS technology will have an advantage in chip density. Ironically enough, bulk CMOS Technology uses verti-NPN BJT devices previously considered as unwanted parasitics to increase its versatility in implementing important analog functions, so that the apparent odds between the MOS and BJT camps become blurred. In any given process and design situation, the inherent and sometimes unwanted components of that process may be used to satisfy the design requirement.

Selecting the Best Boundaries Between D & A

In the development of an LSI digital/analog chip, the precise partitioning of the digital and analog functions are dictated by the requirements of the application, the die area, testing, and the ultimate cost. Certain functions are purely digital, for example, manual data entry into a keyboard with the resulting information displayed on some readout system. Other functions are best implemented in the pure analog domain, such as the modulation of audio information for AM transmission. For functions involving analog or digital signals that are to be processed in a particular manner, the processing could be performed in either the analog or digital domain. In the initial stages of the developmental design cycle, it is necessary to weigh the trade offs relative to which portion of the circuitry will be implemented in the analog and digital domains. For example, if an analog signal requires conversion to the digital domain, and requires some prefiltering processing, the prefiltering could be implemented by switched-capacitor techniques before the conversion process. The other solution is to digitize the signal and perform digital filtering on the coded signal.

Choosing CMOS or NMOS for the Job

Another consideration, especially true at AMI, is the selection of the proper MOS process to fulfill the design requirements. The selection can be PMOS, NMOS, CMOS or VMOS. For this discussion PMOS and VMOS will be excluded, since PMOS has certain similar aspects to NMOS (although slower and less expensive), and since VMOS's analog capabilities have not been totally investigated. This leaves CMOS and NMOS polysilicon gate technologies for consideration. For a given critical dimension feature set (i.e., channel length, or metal line spacing), the NMOS process provides a digital density improvement over CMOS by a factor of 1.5. NMOS also has the advantage over CMOS in that the current production processing requires fewer masks and steps, and this results in a cost advantage by a factor of 1.2 for a given amount silicon. Newer CMOS processes are reducing this advantage. This density and process cost advantage becomes even less significant, as the packaging and testing costs become more dominant for a given function. Advantages of CMOS over NMOS in the digital domain are lower power by a factor of 20 (using microprocessors as comparison), wider voltage variations, and lower susceptibility to power supply noise. In the analog domain CMOS has the advantage of providing more easily implemented analog functions for a smaller size, and providing additional components not found in NMOS processes (i.e., vertical NPN BJT Transistors, and Zener diodes). For example, CMOS has a lead over NMOS in differential operational amplifiers, in that CMOS has greater output voltage range, and greater tolerance to supply variations. Many papers have been published to date on CMOS and NMOS amplifiers [1] [2] [3] [4]. Table 1 shows some measured parameters of AMI's proprietary CMOS and NMOS amplifiers.

Fundamental Digital and Analog Techniques

Just as logic gates and flip-flops are fundamental in developing more sophisticated logic blocks in the digital MOS domain (e.g., shift registers, counters, RAMs, ROMs, PLAs and ALUs), the MOS analog domain has developed in its arsenal amplifiers, comparators, switching capacitors, and converter capacitor/resistor/MOS arrays which comprise the basic building blocks for D/A converters, A/D converters, and filters. Table 2 lists the types of converters that have been implemented thus far in MOS, their possible resolution (without trimming), their conversion rates, and reference numbers for more detail on the techniques. In addition, techniques have appeared that utilize a mixture of array structures to achieve high resolution and accuracies [11] [15]. One of the most important contributions to the MOS analog domain was the development of switched-capacitor filters [16] [17]. This technique uses MOS transmission gates and thin oxide capacitors to form elements that behave like resistors. Using classical filter design associated with active RC filter implementations, the resistors are replaced with the switched-capacitors in those filters.

Since the equivalent resistors track with their capacitor counterparts, the filters achieve high accuracy and stability, nearly independent of process variations. Some of the inherent problems of MOS amplifiers (offset and noise) have been significantly reduced by clever circuit techniques. Voltage offset of an amplifier can be reduced by nearly a factor of 1000 by storing the offset with the voltage of interest on a capacitor, and feeding the resulting value through the amplifier so as to cancel the offset. Other techniques such as auto-zero loops and commutating autozero (CAZ) loops [18] have also reduced offset. Noise (mostly low frequency 1/f) can be reduced by using CAZ or chopping techniques. Voltage references have been developed using the NPN BJT and Zener components in CMOS devices [19]. In addition, references were fabricated using MOS devices in an enhancement-depletion differential pair configuration [20], and by using the MOS subthreshold region [21].

Codec and A/D-D/A Microprocessors as Examples

Many LSI D/A type of devices have been built at AMI in the past. Included are organ chips containing sophisticated digital circuitry and tone shaping circuits, video I.C.'s for generating color graphics on Television consoles, and tone generators that replace the LC oscillator in touch tone® telephone subsets. Today, AMI has entered into even higher degrees of complexities with a CMOS PCM CODEC pair (the S3501 and S3502) [22], and an NMOS 4 bit microprocessor with 8 bit A/D converter (the S2200). CODEC's are one of the glamour devices tailored for the needs of the telephone industry. The S3501 encoder is a logarithmic A/D converter that contains filters to bandlimit the input signal and reduce the 60Hz hum inherent on the telephone line. The voice signal, which has a nominal amplitude range of approximately 48dB and a frequency range of approximately 0.3 to 3.0 KHz is converted by means of a μ-255 companding A/D converter to 8 bits of coded information (PCM). The PCM signal is transmitted at a rate of 1.544MHz over T1 Type Telephone lines, and due to its digital nature, PCM can be reconstructed faithfully by repeating stations without the introduction of noise and distortion. The PCM signal is received by the S3502 decoder that converts this coded information back into the voice signal. This signal is further processed by an on-chip filter before being sent to the telephone subset. Both parts contain digital circuits, such as a SAR, signaling logic, and a phase-lock loop network, to generate the chip clocks synchronized to the 8KHz strobe found on the system. The S3501, as the more complex of the two parts, has for its analog components ten amplifiers, a comparator, an auto-zero loop, an 8 bit capacitor array, and a 4 bit string resistor array within an area of 31,300 mil^2.

The S2200 is a 4-bit microcomputer with A/D and D/A converter capabilities of 8 bits implemented in NMOS. Due to the general nature of this microcomputer, it fits application areas such as automotive instrumentation, household appliances, electronic scales, toys and games, point of sale devices, and remote monitors. The S2200 has an on-chip 2048 word 8-bit ROM, and if necessary, an additional program memory can be added up to a maximum of 8192 words. A scratchpad RAM can hold the temporary values of 64 4-bit data words. Four registers are on-board (BU, BL, E, and ACC), of which BU and BL registers are used to access RAM words, the E register can be used as either a general purpose or an index register for controlling RAM access, and the ACC register serves as an accumulator or temporary storage register. The ALU uses a 4-bit parallel adder and carry register to perform addition, complementation, comparison, and Boolean operations. Sixty-four instructions are available. A program counter acts as a pointer to the next instruction to be executed, and a subroutine stack holds the return address during the execution of subroutines. Up to 5 levels of subroutines are possible. The I/O inputs consist of 3 inputs and 3 outputs for control, eight bidirectional "K" inputs/outputs for software decision making and data entry (including analog-digital information), and eight bi-directional three-state "D" lines for general purpose data signals. In addition, thirteen "A" output lines are used for addressing or external device control. Either an A/D or D/A conversion can be performed. The converter consists of an 8-bit resistor string array which requires no trimming and a high speed clocked comparator. The analog signal to be converted can be applied to any K type input. The start of the analog conversion is initiated by the operation SANG. The resulting word is split and sent to the accumulator and current RAM word location by the RANG instruction. To perform a D/A conversion, the LANG instruction is used. The analog register is loaded from the accumulator and current RAM location, and the resulting analog value appears on K output number five. The chip is expected to be 48,400 mil^2 in area and contains approximately 25,000 devices. Also, a CMOS version is being designed which will be known as the S2210 for low current applications.

Table 1: CMOS and NMOS Differential Pair Amplifier Performance for Supply Voltages of + Volts at 25°C

Parameter	CMOS	NMOS	Units
Differential Gain	88.0	68.0	dB
CMRR	75.0	85.0	dB
PSRR	70.0	44.0	dB
Input Common Mode Range	−4.0, +4.0	−4.9,3.7	V
Output Range	−5.0, +5.0	−4.2,3.8	V
Offset (μ, o)	+1.0, ±13	+38, ±24	mV
Gain-Bandwidth Product	1.3	1.3	MHz
Phase Margin	58.0	60.0	deg.
Slew Rate Rise	6.8	5.0	V/μs
Slew Rate Fall	1.9	2.5	V/μs
Noise (10Hz to 1MHz)	28.0	36.0	μVRMS
Power	1.2	9.0	mW
Size	320.0	500.0	mil^2
Number of Devices	13.0	24.0	--

Table 2: Types of D/A and A/D Converter Techniques Applicable to MOS Fabricated Devices

Type	Resolution	Conversion Rate D/A	Conversion Rate A/D
Integrating [1] [2] [5] [6]	12-16	--	20-500ms
Pulse Modulation [7]	12	--	100ms
R-2R, Binary Weighted R	6-8	6μs	48μs
String Resistor [8] [9]	8-10	3μs	36μs(60ns[1])
Capacitor Array [10] [11]	12-14	3μs	36μs
Charge Swap [12]	6-8	100μs	100μs
Current Steering(MOS) [13] [14]	8-10	0.5-2μs	5-20μs

1. Flash Converter [9]

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AMERICAN MICROSYSTEMS, INC.

AP 602

Specialized signal processing chips simplify telecommunications equipment design

by Dr. Gwyn P. Edwards

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SPECIALIZED SIGNAL PROCESSING CHIPS SIMPLIFY TELECOMMUNICATIONS EQUIPMENT DESIGN

Dr. Gwyn P. Edwards
American Microsystems, Inc.
3800 Homestead Road
Santa Clara, CA 95051

1. INTRODUCTION

Recent advances in silicon technology have in turn made possible great advances in sampled data signal processing, both digital and analog. Digital signal processing has been a classical example of a technique waiting for a technology. Signal processing is much more process intensive than data processing, so while data processing made great advances with the advent of the microprocessor, real-time digital signal processing remained a useful tool only to those whose needs justified the enormous resources required, such as NASA and the military. However, at last the Semiconductor Industry has come to the rescue with VLSI technology that allows chips like the AMI S2811 Signal Processing Peripheral to be realized. We will see that in the same way as the 70's was the Decade of the Microprocessor, the 80's will be the Decade of the "Micro-Signalprocessor". Devices like the S2811 have applications all over the field of Telecommunications, from speech coding for low bit-rate digital systems through high-speed data modems to Telecommunication test equipment such as PCM system analyzers.

On the analog front, other improvements in technology have made possible capacitors with accurate ratios. This, combined with Switched-capacitor circuit theory has made possible truly monolithic filters - the dream of engineers for over a decade. These, and Switched-capacitor codecs will be changing the face of telephone office equipment in the very near future.

2. THE S2811 THE PROGRAMMABLE SIGNAL PROCESSOR CONCEPT

A quick look at the basic requirements of signal processing instantly reveals why a conventional microprocessor falls far short of meeting these requirements. Basically, the whole problem is based on the poor throughput rate of a microprocessor, but this is attributable to, and curable by several factors:

2.1 Bus Conflict

Since a conventional microprocessor shares its data bus between instructions and true data, there is always a bottleneck at this point. An architecture which separates the instruction and data buses (and their associated memories) bring a speed improvement by virtue of increasing the parallelism of the system. Ultimately, this can allow all instructions to be executed in a single cycle.

2.2 Instruction Level

A machine which only has basic level instructions, e.g., Read data, Write data, takes several instructions to execute a simple function, such as read 2 words, perform an arithmetic combination and store the result. This kind of function is fundamental in signal processing, and an architecture that can execute it all in a single instruction not only brings a tremendous improvement in processing power, but also raises the level of the assembly language. This in turn simplifies the programming task by relegating most of the detail to the microprogramming used internally to implement the higher level language.

2.3 Arithmetic power

Signal processing is highly arithmetically orientated. It follows that the throughput of a signal processor will be very dependent on the capabilities of its arithmetic unit. Flexible add/subtract and multiply capabilities are essential and pipelining the multiplier to allow single cycle multiply and accumulate also brings benefits.

2.4 Interfacing

The bus interface of a microprocessor whilst well-suited to data transfer within the microprocessor subsystem, is generally ill-suited to other

interfacing needs, hence the plethora of microprocessor interface chips, PIA's, ACIA's etc., needed to operate microprocessors in the real world. Of great importance also is the need to be able to interface asynchronously and without interfering with the signal processing task itself, so that separate registers for these tasks must be provided.

These features, and many more, were all incorporated into the architecture of the S2811 from the outset, and the result is a single chip processor that is capable of executing signal processing algorithms very efficiently. The architecture is shown in Fig. 1.

Two kinds of interface are provided- an 8 bit bi-directional bus interface (the microprocessor port) which allows the 16 bit data to be transferred as 2 bytes. Together with the Interface Enable, Read/Write and Function lines this allows the device to fit into microprocessor systems as a memory mapped peripheral. By connecting the 4 function bus (F-bus) lines to the 4 least significant address lines and decoding a block of 16 addresses to operate the Interface Enable line the device can be set up into any of its operating modes by reading or writing to those addresses. 13 of them are used (Ø-C) to control the device operation as detailed in Table 1.

Separate input and output registers allow data I/O to take place without interrupting the internal processing. An interrupt request $\overline{IRQ}$ line signals to the control processor whenever I/O service is needed. The other interface is a 6 line asynchronous serial port. Separate inputs and outputs together with their own clocks and enables (all externally initiated) allow the device to be directly connected to a variety of systems including PCM highways. The use of separate buffers between the serial port and the input and output registers mean that this port is double buffered, providing great flexibility when working with variable length algorithms.

The serial port provides an additional degree of flexibility: It allows the device to operate in a stand-alone mode when executing closed loop programs. A simple refinement of this operating mode even allows the device to execute a number of selectable functions.

CONTROL MODE FUNCTIONS

F-BUS VALUE	MNEMONIC	FUNCTION
0	CLR (Clear)	Clears control modes to normal operation.
1	RST (Reset)	Software reset. Clears all SPP registers.
2	DUH (Data U/H)	Specifies MSByte of data word. DUH terminates data word transfer.
3	DLH (Data L/H)	Specifies LSBs of data word.
4	XEQ (Execute)	Starts execution at location specified on data lines.
5	SRI (Ser.Inp)	Enables serial input port.
6	SRO (Ser.Out)	Enables serial output port.
7	SMI (S/M Inp.)	Converts sign + magnitude serial input data to 2's complement form.
8	SMO (S/M Out)	Converts 2's complement internal data to sign+ magnitude serial output.
9	BLK (Block)	Enables block data transfer.
A	XRM (Ext.ROM)	Permits control of SPP using external instruction ROM.
B	SOP	Set Overflow Protect.
C	COP	Clear Overflow Protect.
D,E,F		Not Used.

TABLE 1

The separate internal data and instruction buses connect to the data and instruction memories. The instruction memory is mask programmed ROM (for minimum production costs) and contains 256 seventeen bit words. It is conventional and addressed by the program counter (PC). In the XRM mode of operation this is bypassed and instructions loaded from the data bus are executed one at a time in a load-execute manner. The data memory contains 256 sixteen bit words and has a very unconventional organization in 2 respects:

a) It is organized as a 32 X 8 matrix and has 2 output ports. This allows the reading of 2 words from any selected group of 8 to be read simultaneously, simplifying the requirement, detailed in Section 2.2, of 2 reads in a single cycle.

b) It is arranged as 128 words of RAM (for signal data) and 128 words of ROM (for coefficient data). The RAM/ROM split is made in such a way as to make available 4 words of

each in each group of 8. This is optimum for many applications.

The adder/subtractor unit (ASU) is a 16 bit unit with an accumulator latch. Its output feeds directly back onto the main data bus, and it is equipped with zero, negative and overflow detectors which allow flexible conditional branching to be executed. A useful feature is the saturation circuit which allows the accumulator output to be saturated whenever overflow occurs. This is invaluable in feedback circuits such as recursive filters, where continuous oscillation can otherwise occur after overflow.

Flexible addressing of the memory is provided by the Base and Index registers, whose functions can be interchanged by the SWAP instruction. The Block Transfer mode of operation uses the Index Register for subroutining, and an automatically decremented loop counter provides for simple high speed looping. A data transfer register (the VP register) allows high speed data updating in filter algorithms and an 8 word scratchpad memory augments the main memory or acts as additional accumulator registers. The entire system fits in a 28 pin package.

In each 300nsec. instruction cycle two operators are executed. The first is the arithmetic function, OP1 (read-modify), and the second is the data transfer function, OP2, (write to memory or register). The resulting complete read-modify-write cycle gives each instruction executed high power in terms of both processing speed and program efficiency. The instruction set consists of 16 OP1s and 32 OP2s. There are 388 valid combinations of these (the remaining 124 are incompatible) making the set very powerful, but with only 48 mnemonics to remember, also very easy to use. More detailed information about the chip may be found in the data sheet and references (1) and (2).

3. A SIGNAL PROCESSING APPLICATION A 4800 bps MODEM

The modem industry has been in the forefront in adopting new technology and for several years now the vast majority of the modems on the market have included LSI parts, in many cases custom designed. It is very interesting to note how many modem manufacturers have adopted microprocessors in the data processing sections of their products. This has enabled them to incorporate flexibility and versatility into their products without hardware changes, thereby allowinto them to market a whole range of options at very little cost. Attempts to incorporate microprocessors into the signal processing sections of modems, however, have only served to prove the inability of the conventional microprocessor to accomplish such tasks. The S2811 fills this gap nicely.

Although it can be shown that the S2811 is technically applicable to any modem configuration up to 9600 bits/sec. its sheer capability and consequent cost make it economically unattractive in most applications below 4800 bits/sec., although there are exceptions at 1200 and 2400 bits/sec. The 4800 bits/sec. (CCITT V.27 and Bell 208) and 9600 bits/sec. (CCITT V.29) are the two modems in which the S2811 shows greatest potential, with the 4800 bits/sec one being especially interesting since one S2811 can accomplish all the signal processing in this device. The V.27 modem is shown in block form in Fig. 2. The signal processing all takes place in the S2811 and the data processing and miscellaneous housekeeping takes place in the S6801MCU. Minimal external circuitry is required to make up a flexible modem system without the development costs associated with custom design, as shown in Fig. 3.

4. SWITCHED CAPACITOR FILTER TECHNOLOGY

A major recent innovation in semiconductor technology has been the ability to realize floating capacitors with closely controlled ratios. This technology was initially developed in UC Berkeley to realize switched capacitor filters, which were just a lab curiosity without a suitable technology. The potential of this powerful combination of a momolithic technology and a circuit design technique was such that it moved out of the research laboratory into full scale production at a remarkable rate, and several manufacturers are now offering switched-capacitor filters. The technology itself has been used to realize more than just filters, as the close tolerance capacitor ratios lend themselves well to digital to analog conversion techniques too. Thus, armed with a powerful new weapon, the MOS industry has made inroads into fields which were hitherto the exclusive domain of bipolar and hybrid technologies.

The basic technology for realizing the floating capacitor is shown in Fig. 4. The process is identical to a conventional silicon gate NMOS (or CMOS) process up to the stage where the oxide layer is grown on top of the polysilicon

pattern. This is the stage shown in Fig. 4(a), and at this point in the normal process, all that remains to be done is to etch contact holes and deposit the aluminum pattern. In the floating capacitor process a modified contact mask is used to strip the Vapox layer from both the normal contact holes and the capacitor areas, as shown in Fig. 4(b). It is this mask that determines the capacitor areas. A thin layer of clean oxide is then thermally grown on the freshly exposed silicon areas, as shown in Fig. 4(c). The thickness of this oxide is typically 600 Å. This will determine the absolute values of the capacitors, but it will be shown later that only the ratios of capacitor values are of concern, and so the important factor at this stage is the uniformity of the oxide thickness over relatively small areas of the wafer. This can be made constant to within 0.1%. After the oxide growth it is necessary to recut the contact holes, using the regular contact mask, and deposit the aluminum pattern as shown in Fig. 4(d). Note that the resulting floating capacitor has a significant parasitic capacitance from its lower plate to substrate (ground), and circuit design must take this into account. In conclusion, the floating capacitor process involves only one additional masking stage and one additional oxide growing stage over the regular NMOS or CMOS processes, both of which can easily be accomodated into the wafer fabrication line.

Before proceeding to the application of this technology it is necessary to understand the basic property of switched capacitor filters which makes the absolute values of the capacitors unimportant. This is completely in contrast to other filter design techniques, where parameter products are involved, making them unsuitable for realization with monolithic technologies, where close tolerance absolute values are not possible This basic property may be explained with the aid of Fig. 5. If switch S moves from position B to position A, then the voltage on capacitor C will change from V2 to V1. The charge in the capacitor will thus change (ΔQ) by C(V1-V2). If the switch now moves repeatedly between positions A and B, this amount of charge will be picked up from node A and dumped into node B in each cycle of the switch, and thus a net current will flow from node A to node B. This current is the rate of charge transfer, and is equal to the product of the charge transfer per cycle and the frequency of the switch cycling, f_c:

$$I = \Delta Q f_c = C(V1-V2)f_c$$

So far we have assumed that both V2 and V1 are constant, so that the current is also constant, but it is easy to visualize (and can be proved) that the analysis remains good for varying values, as long as the variation during one cycle of switch closure is negligible, i.e., $f_s << f_c$ where f_s is the signal (V1 and V2) frequency. A complete analysis shows that there is also a predictable dependence on f_s when this is not true.

If we now use the circuit in Fig. 5 to represent the resistance in an R-C integrator, as shown in Fig. 6, then the system has a transfer function:

$$G(j\omega) = \frac{1}{1+j\omega RC_2} = \frac{1}{1+j\omega C_2/C_1 f_c}$$

as long as $\omega << 2\pi f_c$, which is dependent only on the ratio C2/C1, since f_c can be externally controlled.

Much more complex filter structures can be realized using the same techniques and in all cases it can be shown that the same principle of dependence on capacitor ratios only still applies. However, it is essential to use the correct sampled data analysis or synthesis techniques (Z transform theory) to design structures that will operate correctly over wider bandwidth. A summary of AMI's switched capacitor filter capabilities is shown in Table 2.

SUMMARY OF AMI'S SWITCHED CAPACITOR FILTER DESIGN CAPABILITIES

* All types of filters (HP,LP,BP, etc) possible.
* Several computer aided design techniques available to provide optimum design in all cases.
* Gain/shape variation typically less than 0.1%.
* Temperature stability typically 20ppm/^{o}C.
* Sampling frequencies up to 250KHz.
* Q factors up to 50.
* Operational amplifier gains typically 80dB.
* Dynamic range typically 80dB

TABLE 2

5. A FILTER APPLICATION
DTMF BANDSPLIT FILTER, S3525

The DTMF (Touch Tone®) receiver has been a problem child to telecommunication engineers ever since the specification was written. The specification is not an easy one to meet at any cost - but at a realistic cost it becomes extremely difficult. Generally the receiver has been realized using digital techniques of period measurement, but this still leaves the dial-tone rejection and tone group separation (bandsplitting) to be done using conventional analog techniques. The filter requirements are complex but not stringent, and are summarized in the masks shown in Fig. 7. A realization of the overall function, the S3525 is shown in the block diagram in Fig. 8. The addition of low-pass filters at the input and outputs seems superfluous at first sight, but will be explained.

One characteristic of sampled data filters is that all parameters are a function of the sampling frequency. When pole frequencies become very small fractions of the sampling frequency the filter parameters become small, resulting in the capacitor ratios required becoming very large. In turn, larger capacitor ratios become increasingly innacurate so that best results will always be obtained if the sampling frequency can be made no more than about ten times the working signal bandwidth. The actual frequency (f_2) used in the S3525 is obtained by dividing the frequency of the ubiquitous (and cheap!) 3.58MHz colorburst crystal by 128, giving 28KHz. (approximately). This makes the design of the main filters straightforward, but introduces 2 problems:

5.1 Since the Nyquist frequency of the system is now only 14KHz, stray signals at the telephone office can create aliasing distortion problems. In the S3525, this problem is eliminated by preceeding the main filters with a 3KHz low pass filter sampling at a much higher rate.

5.2 Since the output of the bandsplitting filters are sampled at 28KHz, the period counting circuits in the following detector can resolve the zero crossings to only 35.7μsec, which is inadequate. This problem is solved by following the bandsplitting filters with interpolating filters, which are low-pass filters running at a higher sampling rate.

In both cases the sampling frequency used (f1) is obtained by dividing the crystal frequency by 24, giving a frequency of 150KHz (approximately). This results in the system having an input Nyquist frequency of 75KHz, and an output resolution of 6.7μsec, both of which adequately meet requirements.

More detailed information on the design of the filters themselves may be obtained in (4). The S3525 provides on chip comparators for squaring the outputs, and these are left unconnected internally to allow the filter outputs to be filtered with a simple R-C circuit to further improve the time resolution. In addition, hysteresis may be used to provide added noise immunity. These features are all incorporated into the system shown in Fig 9, where the S3525 is used in conjunction with a Mostek MK5102 DTMF decoder chip to realize a 2 chip DTMF receiver.

6. CONCLUSION

Two new signal processing chips have been presented, one digital and one analog. Both are the result of some of the latest improvements in semi-conductor technology, and both simplify the design of telecommunication equipment. Both allow products to be realized with fewer components and fewer production line adjustment than previously possible. These features allow products to be made more cost effective, thereby increasing their market penetration.

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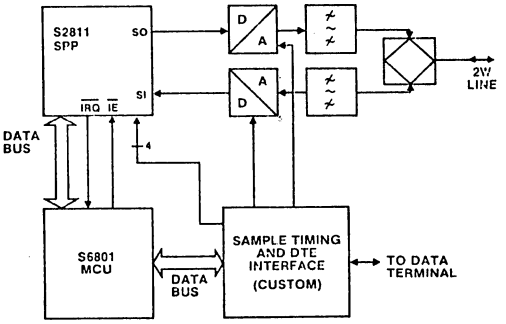


Fig. 3 (above) V27 Modem Using S2811 and S6801

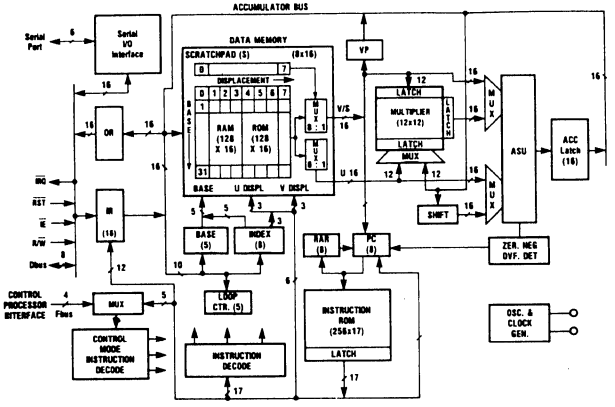


Fig. 1 S2811 Architecture

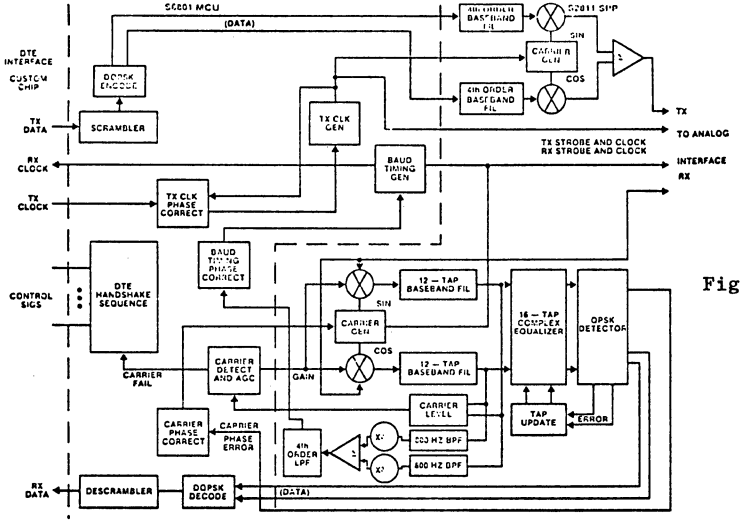


Fig. 2 CCITT V27 Modem Functions.

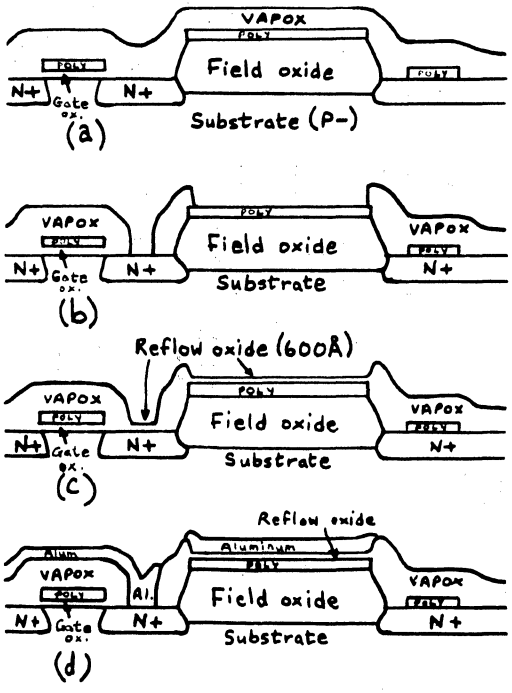


Fig. 4 Floating Capacitor Technology

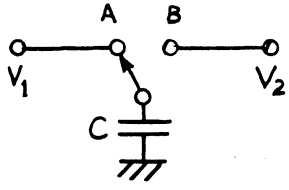


Fig.6 Switched Capacitor Principle

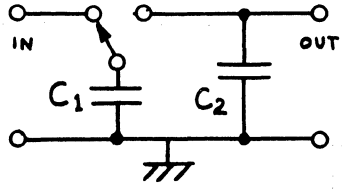


Fig.6 Switched Capacitor Lowpass Filter

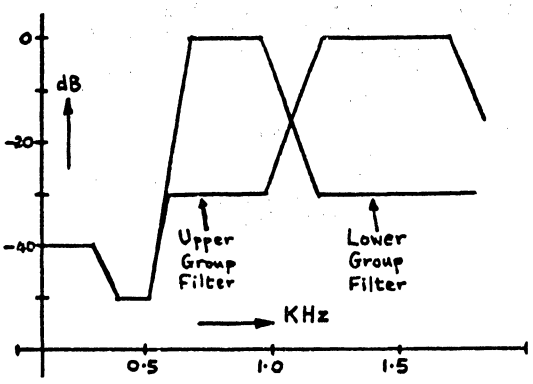


Fig.7 DTMF Filter Masks

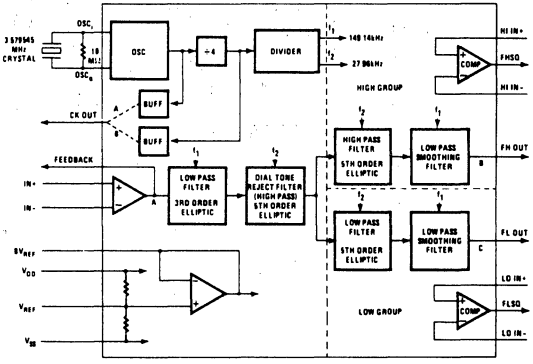


Fig.8 S3525 Block Diagram

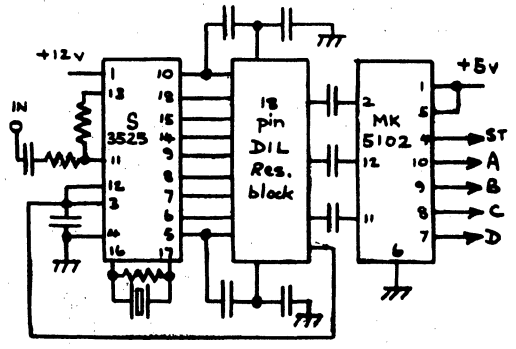
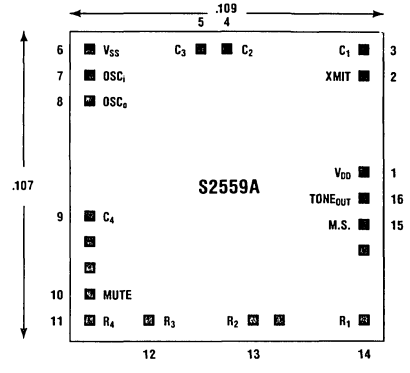
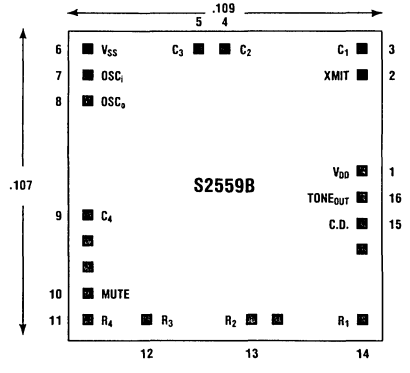


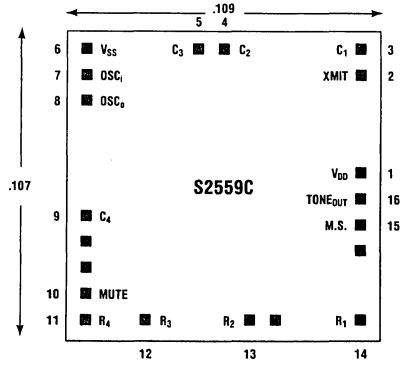
Fig.9 DTMF Receiver Using S3525 & MK5102

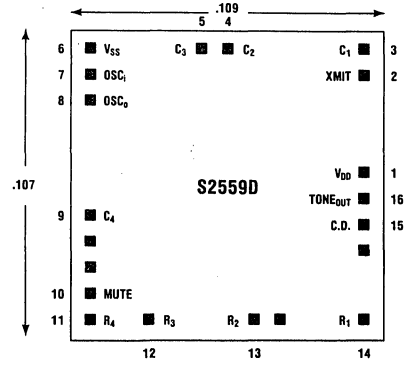
Dice and Bonding Diagrams

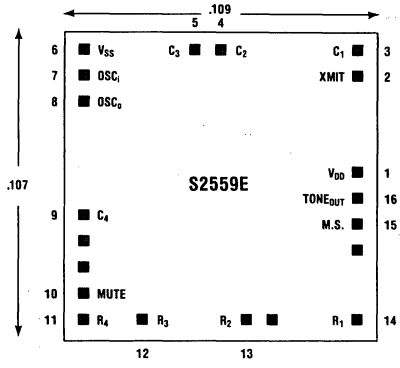
NOTE: These devices are available in dice form. All dimensions in inches.







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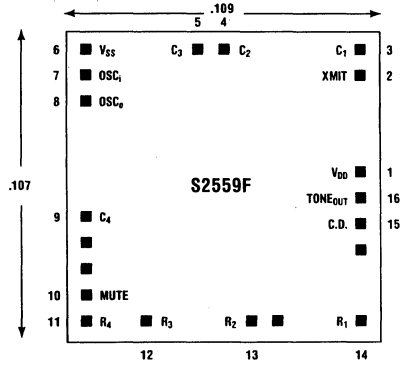
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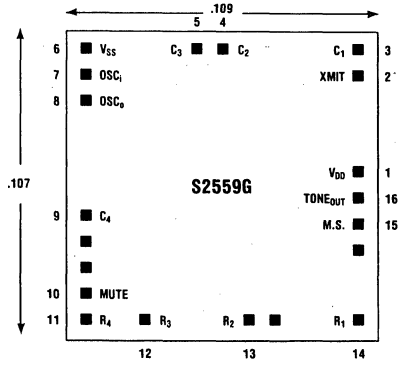
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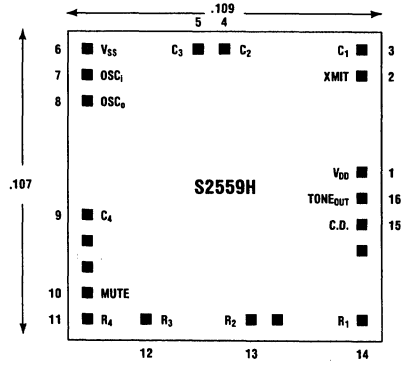
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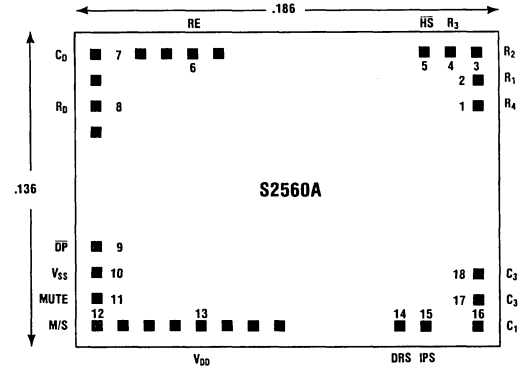
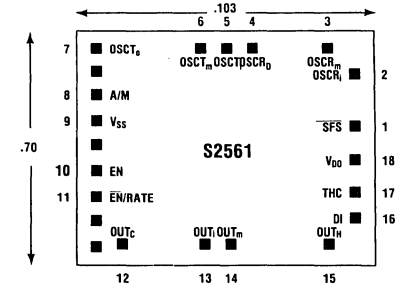
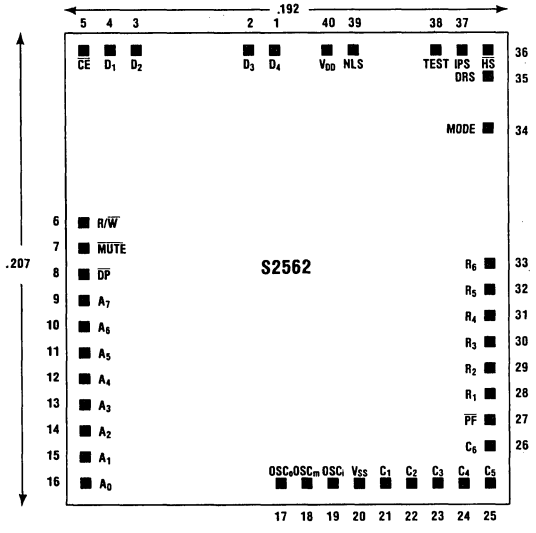
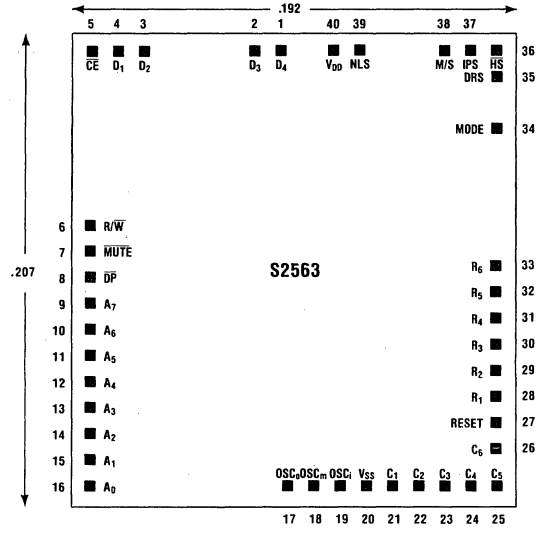
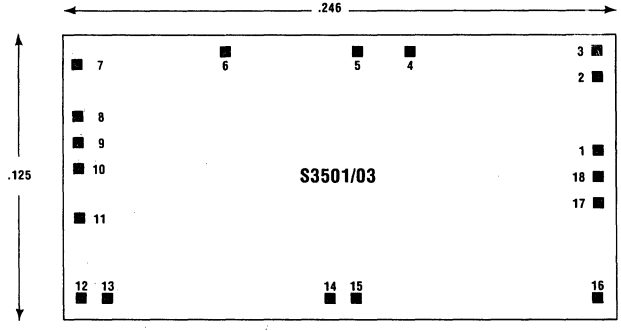
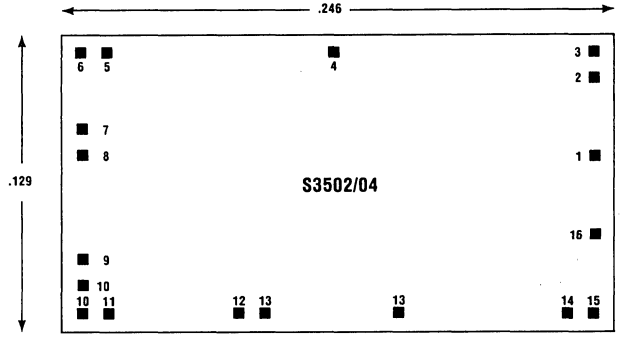

.186
RE
HS R3
CD
RD
DP
VSS
MUTE
M/S
R2
R1
R4
C3
C3
C1
S2560A
VDD
DRS IPS

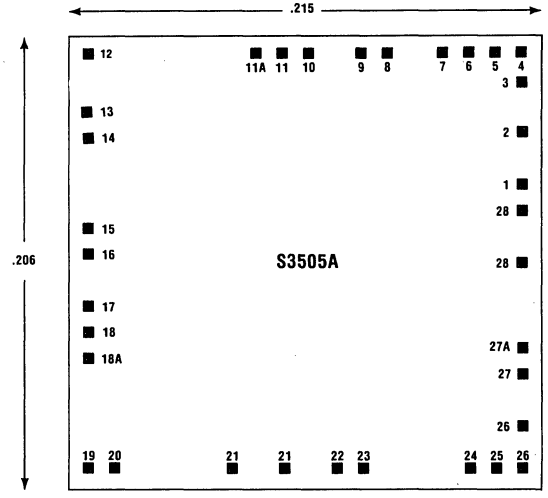

.103
.70
OSCTe
A/M
VSS
EN
EN/RATE
OUTC
OSCTm OSCTI OSCRD
OUTI OUTm
OSCRm
OSCRI
SFS
VDD
THC
DI
OUTH
S2561

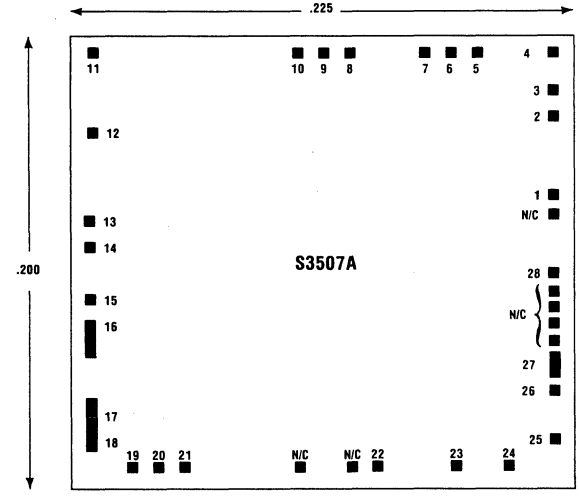

.192
.207
CE D1 D2
D3 D4
VDD NLS
TEST IPS HS
DRS
MODE
R/W
MUTE
DP
A7
A6
A5
A4
A3
A2
A1
A0
R6
R5
R4
R3
R2
R1
PF
C6
OSCe OSCm OSCI VSS C1 C2 C3 C4 C5
S2562

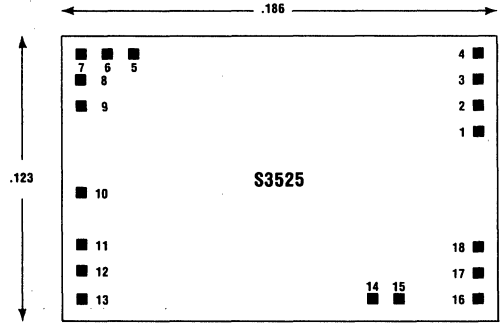

.192
.207
S2563
5 4 3 2 1 40 39 38 37
CE D1 D2 D3 D4 VDD NLS M/S IPS HS
DRS
MODE
R/W
MUTE
DP
A7
A6
A5
A4
A3
A2
A1
A0
R6 R5 R4 R3 R2 R1
RESET
C6
OSCo OSCm OSCi VSS C1 C2 C3 C4 C5
6 7 8 9 10 11 12 13 14 15 16
17 18 19 20 21 22 23 24 25
26 27 28 29 30 31 32 33 34 35 36

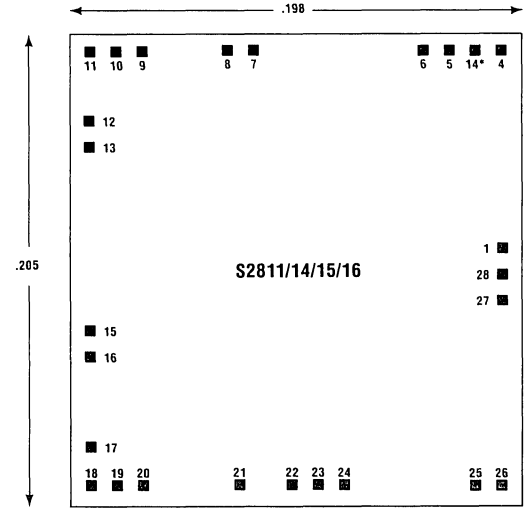

.246
.125
S3501/03
7 6 5 4 3 2 1 18 17
8 9 10 11
12 13 14 15 16


.246
.129
6
5
4
3
2
7
8
1
S3502/04
16
9
10
10
11
12
13
13
14
15

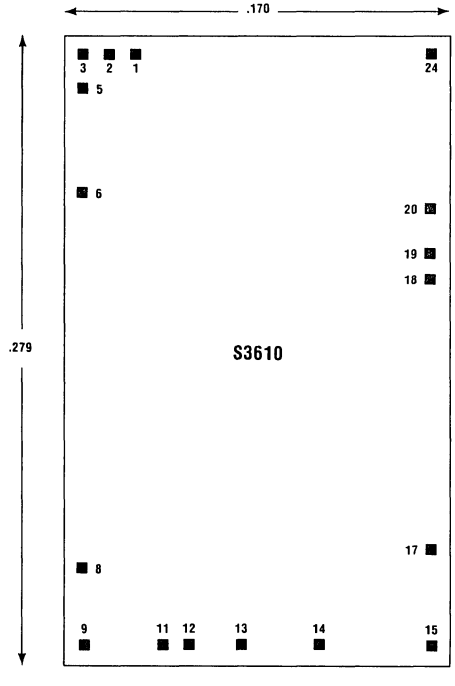

.215
.206
12
11A
11
10
9
8
7
6
5
4
3
13
14
2
1
28
15
16
S3505A
28
17
18
18A
27A
27
26
19
20
21
21
22
23
24
25
26

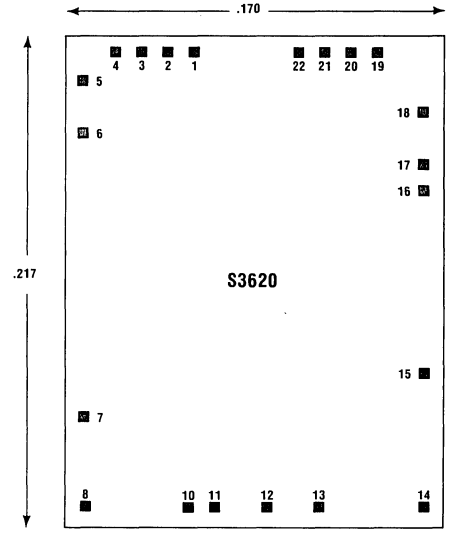

.225
.200
11
10
9
8
7
6
5
4
3
2
12
1
N/C
13
14
S3507A
28
15
N/C
16
27
26
17
18
25
19
20
21
N/C
N/C
22
23
24

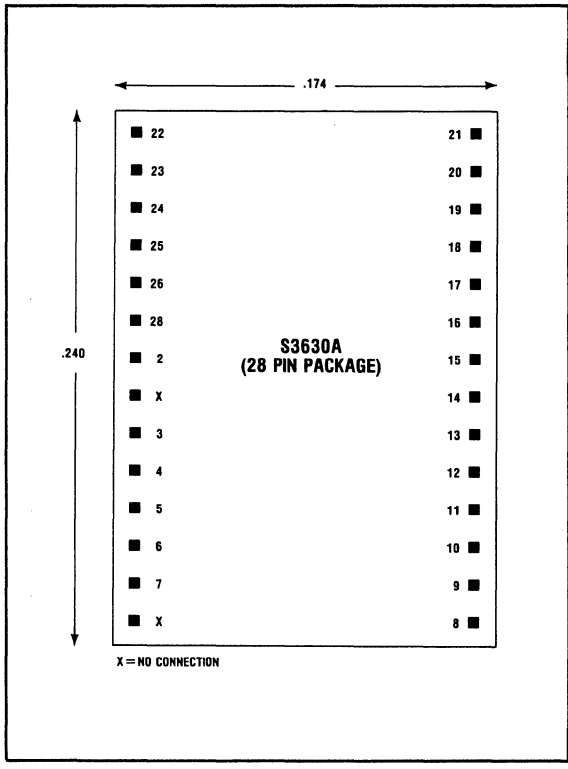

.186
.123
7
6
5
4
8
3
9
2
1
S3525
10
11
18
12
17
14
15
13
16

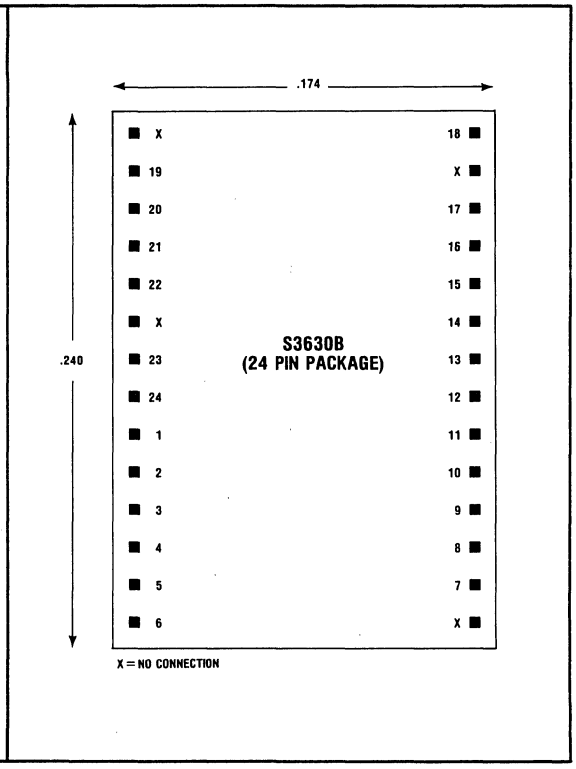


*THIS PAD IS BONDED TO WELL (GND)



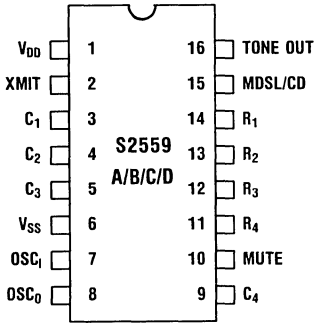


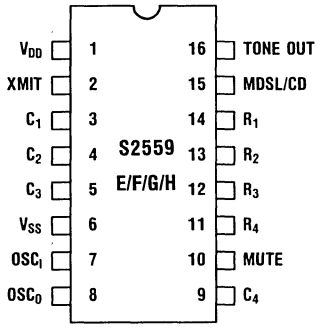

.174
.240
22
23
24
25
26
28
2
X
3
4
5
6
7
X
21
20
19
18
17
16
15
14
13
12
11
10
9
8
S3630A
(28 PIN PACKAGE)
X = NO CONNECTION

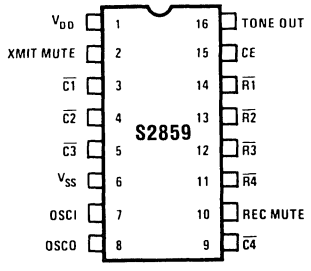

.174
.240
X
19
20
21
22
X
23
24
1
2
3
4
5
6
18
X
17
16
15
14
13
12
11
10
9
8
7
X
S3630B
(24 PIN PACKAGE)
X = NO CONNECTION

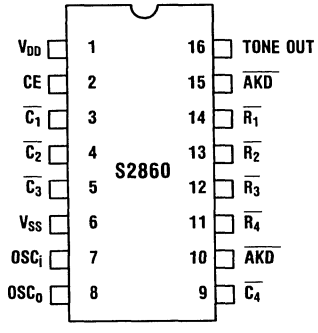
Product Pin-Out Designations

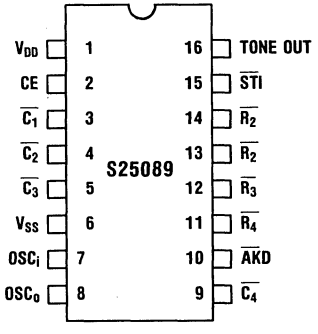
NOTES: ALL FIGURES ARE TOP VIEW, N/C = NO CONNECTION; N/U = NOT USED

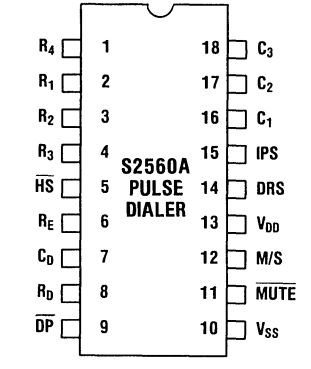


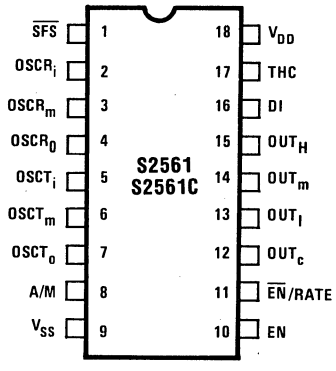


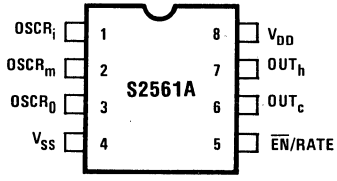


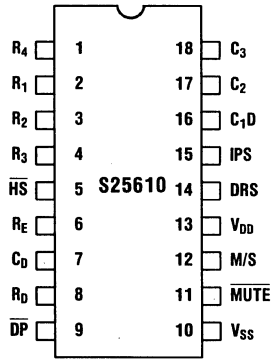


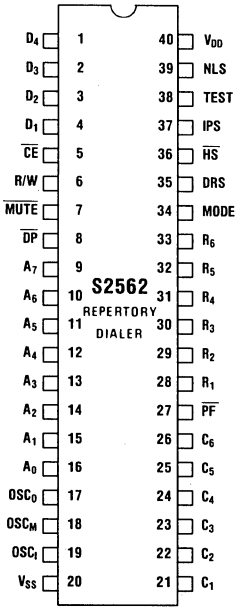


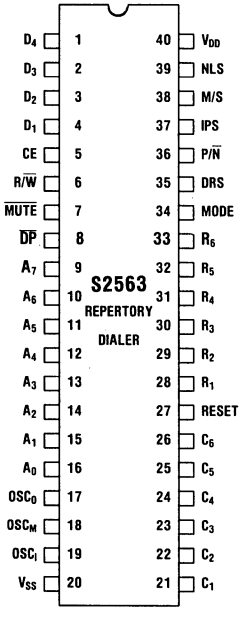


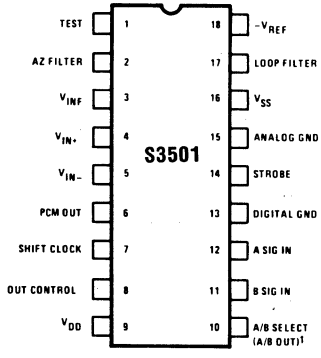

S2561
S2561C
1 SFS
2 OSCRi
3 OSCRm
4 OSCRO
5 OSCTi
6 OSCTm
7 OSCTO
8 A/M
9 VSS
18 VDD
17 THC
16 DI
15 OUTH
14 OUTm
13 OUTl
12 OUTc
11 EN/RATE
10 EN

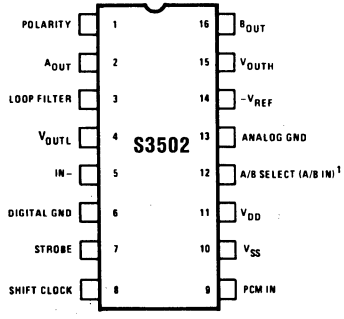

S2561A
1 OSCRi
2 OSCRm
3 OSCRO
4 VSS
8 VDD
7 OUTh
6 OUTc
5 EN/RATE

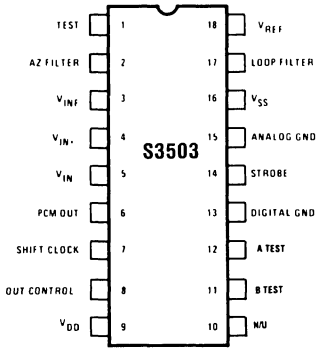

S25610
1 R4
2 R1
3 R2
4 R3
5 HS
6 RE
7 CD
8 RD
9 DP
18 C3
17 C2
16 C1D
15 IPS
14 DRS
13 VDD
12 M/S
11 MUTE
10 VSS

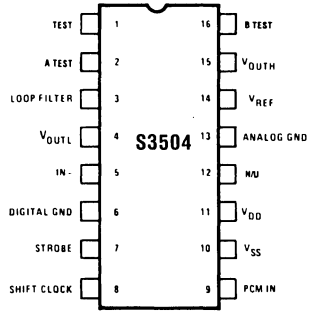

S2562
REPERTORY
DIALER
1 D4
2 D3
3 D2
4 D1
5 CE
6 R/W
7 MUTE
8 DP
9 A7
10 A6
11 A5
12 A4
13 A3
14 A2
15 A1
16 A0
17 OSC0
18 OSCM
19 OSCI
20 VSS
40 VDD
39 NLS
38 TEST
37 IPS
36 HS
35 DRS
34 MODE
33 R6
32 R5
31 R4
30 R3
29 R2
28 R1
27 PF
26 C6
25 C5
24 C4
23 C3
22 C2
21 C1

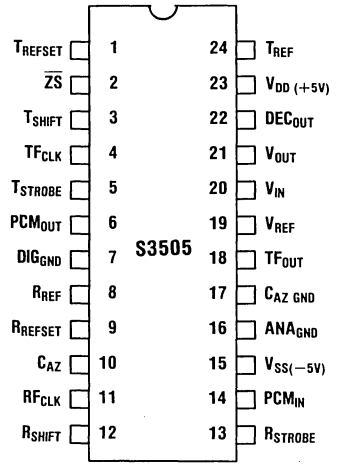

S2563
REPERTORY
DIALER
1 D4
2 D3
3 D2
4 D1
5 CE
6 R/W
7 MUTE
8 DP
9 A7
10 A6
11 A5
12 A4
13 A3
14 A2
15 A1
16 A0
17 OSC0
18 OSCM
19 OSCI
20 VSS
40 VDD
39 NLS
38 M/S
37 IPS
36 P/N
35 DRS
34 MODE
33 R6
32 R5
31 R4
30 R3
29 R2
28 R1
27 RESET
26 C6
25 C5
24 C4
23 C3
22 C2
21 C1

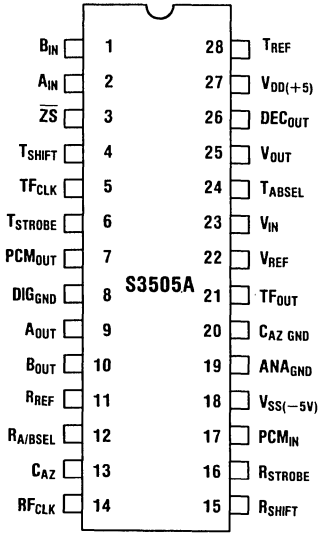

S3501
1 TEST
2 AZ FILTER
3 VINF
4 VIN+
5 VIN-
6 PCM OUT
7 SHIFT CLOCK
8 OUT CONTROL
9 VDD
18 -VREF
17 LOOP FILTER
16 VSS
15 ANALOG GND
14 STROBE
13 DIGITAL GND
12 A SIG IN
11 B SIG IN
10 A/B SELECT (A/B OUT)1

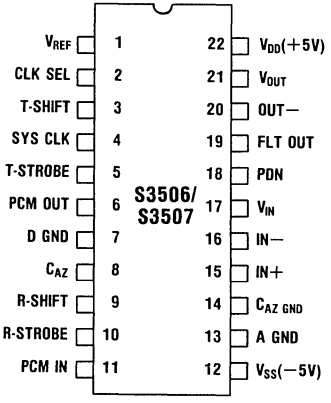

S3502
1 POLARITY
2 AOUT
3 LOOP FILTER
4 VOUTL
5 IN-
6 DIGITAL GND
7 STROBE
8 SHIFT CLOCK
16 BOUT
15 VOUTH
14 -VREF
13 ANALOG GND
12 A/B SELECT (A/B IN)1
11 VDD
10 VSS
9 PCM IN

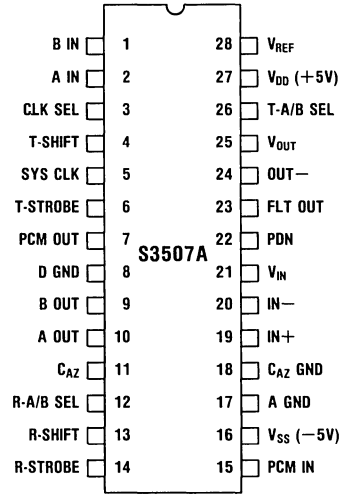

S3503
TEST 1
AZ FILTER 2
V_{INF} 3
V_{IN-} 4
V_{IN} 5
PCM OUT 6
SHIFT CLOCK 7
OUT CONTROL 8
V_{DD} 9
18 V_{REF}
17 LOOP FILTER
16 V_{SS}
15 ANALOG GND
14 STROBE
13 DIGITAL GND
12 A TEST
11 B TEST
10 N/U

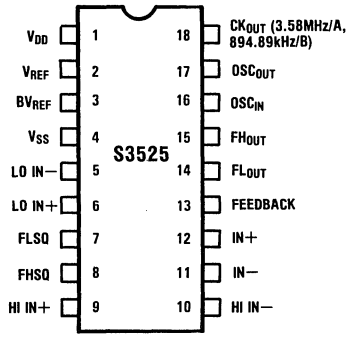

S3504
TEST 1
A TEST 2
LOOP FILTER 3
V_{OUTL} 4
IN- 5
DIGITAL GND 6
STROBE 7
SHIFT CLOCK 8
16 B TEST
15 V_{OUTH}
14 V_{REF}
13 ANALOG GND
12 N/U
11 V_{DD}
10 V_{SS}
9 PCM IN

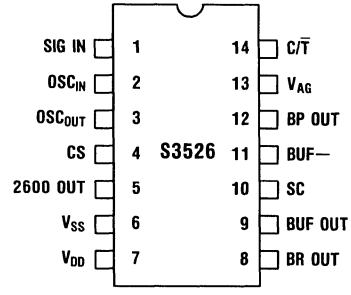

S3505
T_{REFSET} 1
$\overline{ZS}$ 2
T_{SHIFT} 3
TF_{CLK} 4
T_{STROBE} 5
PCM_{OUT} 6
DIG_{GND} 7
R_{REF} 8
R_{REFSET} 9
C_{AZ} 10
RF_{CLK} 11
R_{SHIFT} 12
24 T_{REF}
23 V_{DD} (+5V)
22 DEC_{OUT}
21 V_{OUT}
20 V_{IN}
19 V_{REF}
18 TF_{OUT}
17 C_{AZ} GND
16 ANA_{GND}
15 V_{SS}(−5V)
14 PCM_{IN}
13 R_{STROBE}

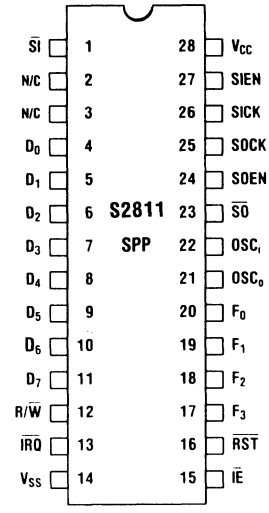

S3505A
B_{IN} 1
A_{IN} 2
$\overline{ZS}$ 3
T_{SHIFT} 4
TF_{CLK} 5
T_{STROBE} 6
PCM_{OUT} 7
DIG_{GND} 8
A_{OUT} 9
B_{OUT} 10
R_{REF} 11
$R_{A/BSEL}$ 12
C_{AZ} 13
RF_{CLK} 14
28 T_{REF}
27 V_{DD}(+5)
26 DEC_{OUT}
25 V_{OUT}
24 T_{ABSEL}
23 V_{IN}
22 V_{REF}
21 TF_{OUT}
20 C_{AZ} GND
19 ANA_{GND}
18 V_{SS}(−5V)
17 PCM_{IN}
16 R_{STROBE}
15 R_{SHIFT}

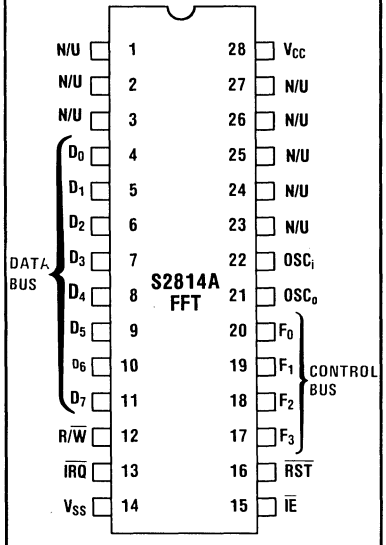

S3506/
S3507
V_{REF} 1
CLK SEL 2
T-SHIFT 3
SYS CLK 4
T-STROBE 5
PCM OUT 6
D GND 7
C_{AZ} 8
R-SHIFT 9
R-STROBE 10
PCM IN 11
22 V_{DD}(+5V)
21 V_{OUT}
20 OUT−
19 FLT OUT
18 PDN
17 V_{IN}
16 IN−
15 IN+
14 C_{AZ} GND
13 A GND
12 V_{SS}(−5V)

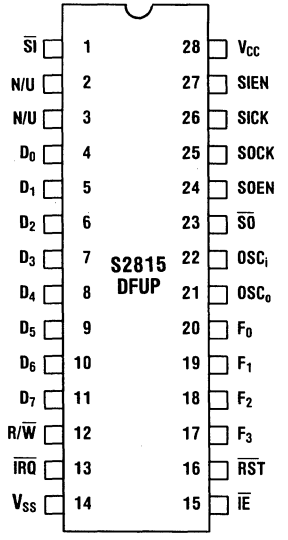

S3507A
B IN 1
A IN 2
CLK SEL 3
T-SHIFT 4
SYS CLK 5
T-STROBE 6
PCM OUT 7
D GND 8
B OUT 9
A OUT 10
C_{AZ} 11
R-A/B SEL 12
R-SHIFT 13
R-STROBE 14
28 V_{REF}
27 V_{DD} (+5V)
26 T-A/B SEL
25 V_{OUT}
24 OUT−
23 FLT OUT
22 PDN
21 V_{IN}
20 IN−
19 IN+
18 C_{AZ} GND
17 A GND
16 V_{SS} (−5V)
15 PCM IN

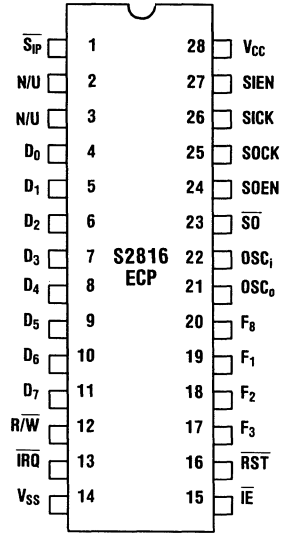

S3525
VDD 1
VREF 2
BVREF 3
VSS 4
LO IN− 5
LO IN+ 6
FLSQ 7
FHSQ 8
HI IN+ 9
18 CKOUT (3.58MHz/A, 894.89kHz/B)
17 OSCOUT
16 OSCIN
15 FHOUT
14 FLOUT
13 FEEDBACK
12 IN+
11 IN−
10 HI IN−

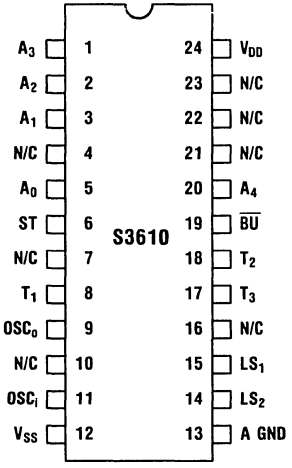

S3526
SIG IN 1
OSCIN 2
OSCOUT 3
CS 4
2600 OUT 5
VSS 6
VDD 7
14 C/T
13 VAG
12 BP OUT
11 BUF−
10 SC
9 BUF OUT
8 BR OUT

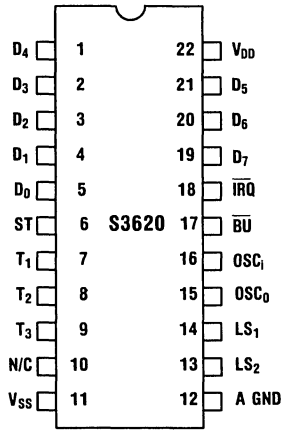

S2811
SPP
SI 1
N/C 2
N/C 3
D0 4
D1 5
D2 6
D3 7
D4 8
D5 9
D6 10
D7 11
R/W 12
IRQ 13
VSS 14
28 VCC
27 SIEN
26 SICK
25 SOCK
24 SOEN
23 SO
22 OSCi
21 OSCo
20 F0
19 F1
18 F2
17 F3
16 RST
15 IE

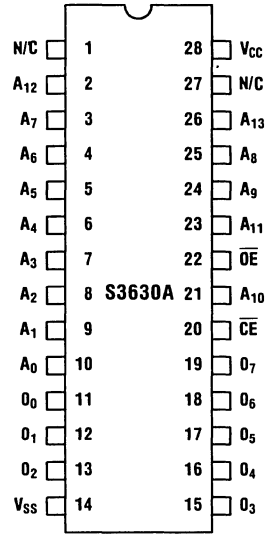

S2814A
FFT
N/U 1
N/U 2
N/U 3
D0 4
D1 5
D2 6
D3 7
D4 8
D5 9
D6 10
D7 11
R/W 12
IRQ 13
VSS 14
28 VCC
27 N/U
26 N/U
25 N/U
24 N/U
23 N/U
22 OSCi
21 OSCo
20 F0
19 F1
18 F2
17 F3
16 RST
15 IE
DATA BUS
CONTROL BUS

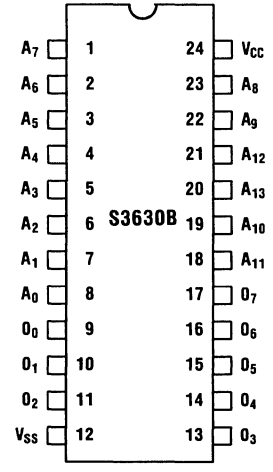

S2815
DFUP
SI 1
N/U 2
N/U 3
D0 4
D1 5
D2 6
D3 7
D4 8
D5 9
D6 10
D7 11
R/W 12
IRQ 13
VSS 14
28 VCC
27 SIEN
26 SICK
25 SOCK
24 SOEN
23 SO
22 OSCi
21 OSCo
20 F0
19 F1
18 F2
17 F3
16 RST
15 IE


S2816
ECP
SIP 1
N/U 2
N/U 3
D0 4
D1 5
D2 6
D3 7
D4 8
D5 9
D6 10
D7 11
R/W 12
IRQ 13
VSS 14
28 VCC
27 SIEN
26 SICK
25 SOCK
24 SOEN
23 SO
22 OSCi
21 OSCo
20 F8
19 F1
18 F2
17 F3
16 RST
15 IE









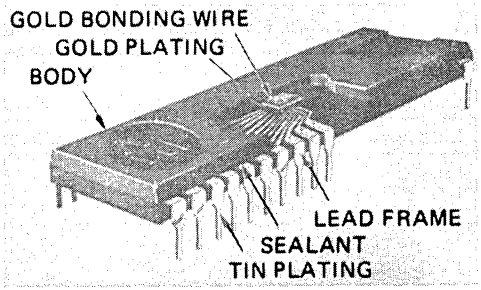
N.C. = NO CONNECTION

PLASTIC PACKAGE

The AMI plastic dual-in-line package is the equivalent of the widely accepted industry standard, refined by AMI for MOS/LSI applications. The package consists of a plastic body, transfer-molded directly onto the assembled lead frame and die. The lead frame is Kovar or Alloy 42, with external pins tin plated. Internally, there is a 150μin. silver spot on the die attach pad and on each bonding fingertip. Gold bonding wire is attached with the thermosonic gold ball bonding technique.

Materials of the lead frame, the package body, and the die attach are all closely matched in thermal expansion coefficients, to provide optimum response to various thermal conditions. During manufacture every step of the process is rigorously monitored to assure maximum quality of the AMI plastic package.

Available in: 8, 14, 16, 18, 22, 24, 28, 40 and 64 pin configurations.

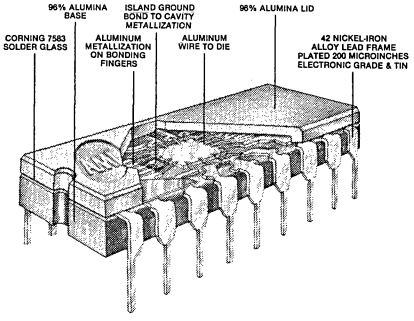


Cerdip PACKAGE

The Cerdip dual-in-line package has the same high performance characteristics as the standard three-layer ceramic package yet is a cost-effective alternative. It is a military approved type package with excellent reliability characteristics.

The package consists of an Alumina (Al_2O_3 base and the same material lid, hermetically fused onto the base with low temperature solder glass.

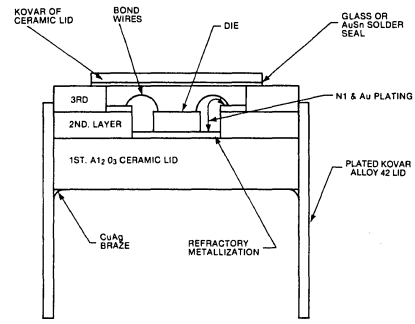
Available in 14, 16, 18, 20, 22, 24, 28 and 40 pin configurations.



CERAMIC PACKAGE

Industry standard high performance, high reliability package, made of three layers of AL_2O_3 ceramic and nickel-plated refractory metal. Either a low temperature glass sealed ceramic lid or a gold tin *eutectic* sealer Kovar lid is used to form the hermetic cavity of this package. Package leads are available with gold or tin plating for socket insertion or soldering.

Available in 14, 16, 18, 22, 24, 28 40 and 64 pin configurations.

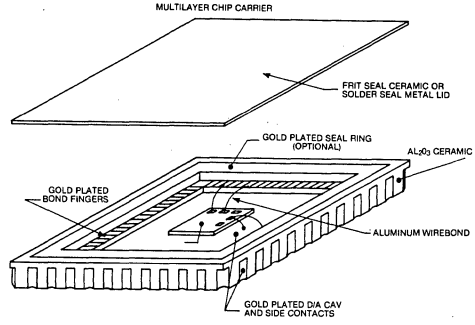


CHIP CARRIER PACKAGE

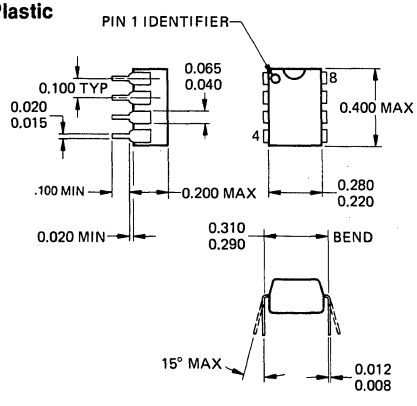
Chip carriers are the new industry standard in reducing package size. Build on the same concept as the highly reliable side-braze ceramic package, it is made of three layers of AL_2O_3 ceramic, refractory metallization and gold plating. The chip carrier also offers contact pads equally spaced on all four sides of the carrier resulting in increased package density, better electrical characteristics, and a more cost effective way of packaging IC devices.

The package comes with a gold tin *eutectic* sealed metal lid or the low cost glass sealed ceramic lid creating a standard hemetic cavity.

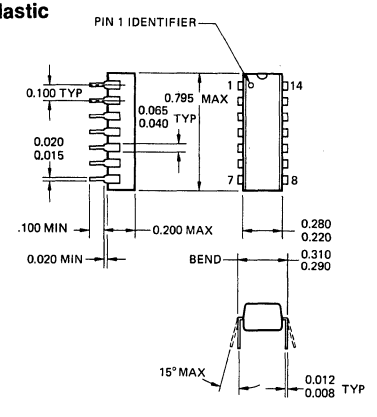
Available in 20, 24, 28, 40, 44, 68 and 84 LD standard 3-layer versions and 24, 28, 44 LD slam style on 50 mil center lines to the JEDEC standards.



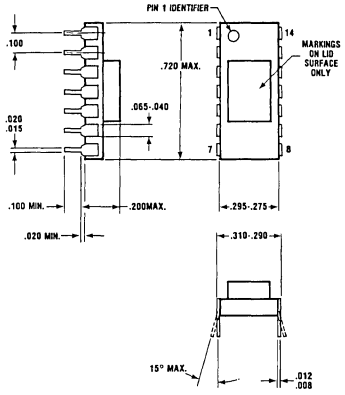
8-Pin Plastic



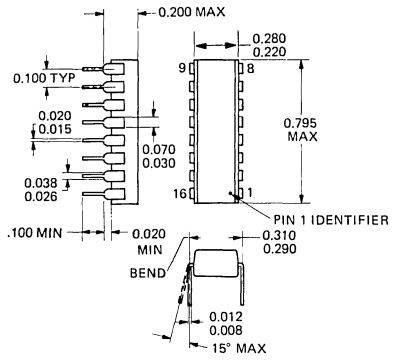
14-Pin Plastic



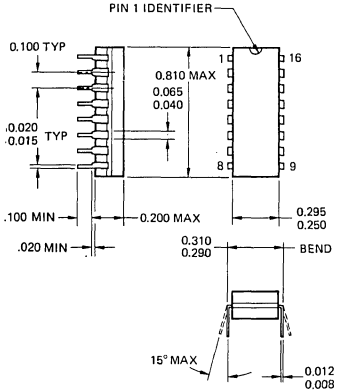
14-Pin Ceramic



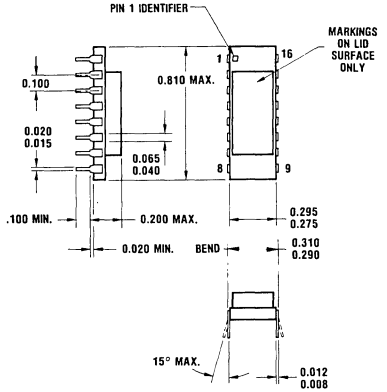
16-Pin Plastic



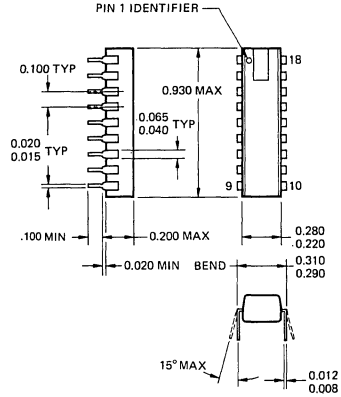
16-Pin Cerdip



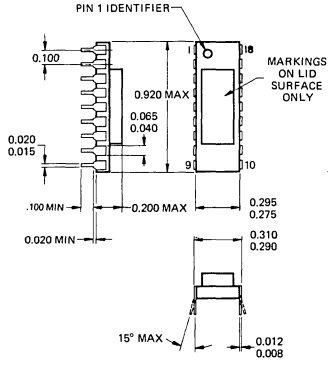
16-Pin Ceramic



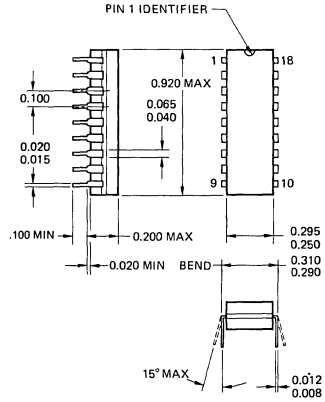
18-Pin Plastic



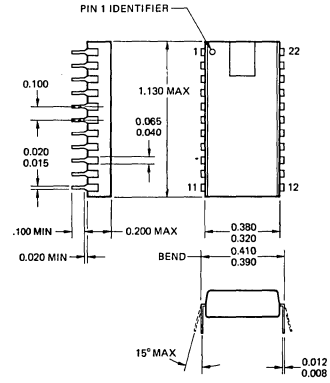
18-Pin Ceramic



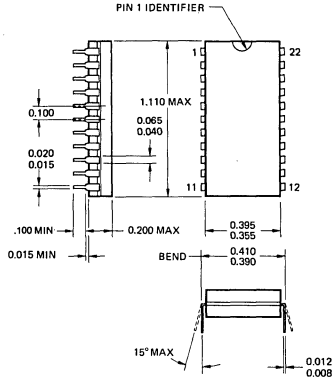
18-Pin Cerdip



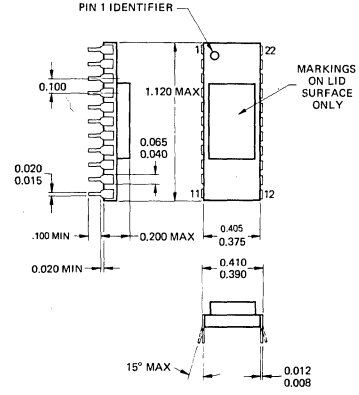
22-Pin Plastic



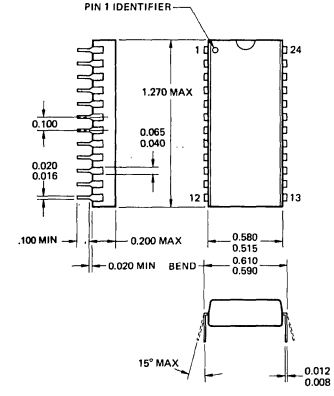
22-Pin Cerdip



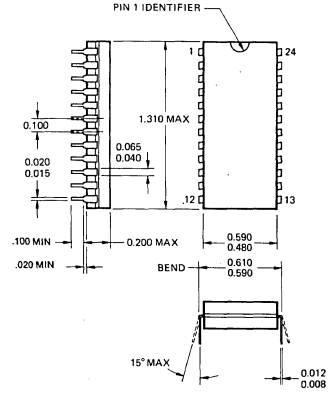
22-Pin Ceramic



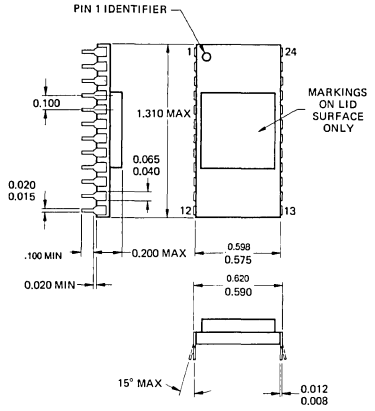
24-Pin Plastic



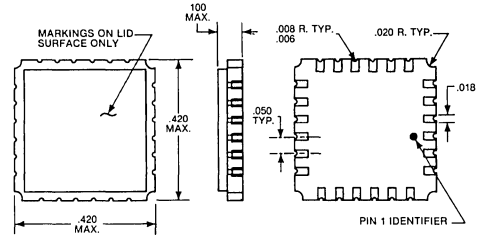
24-Pin Cerdip



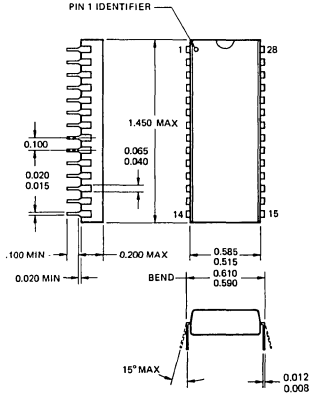
24-Pin Ceramic



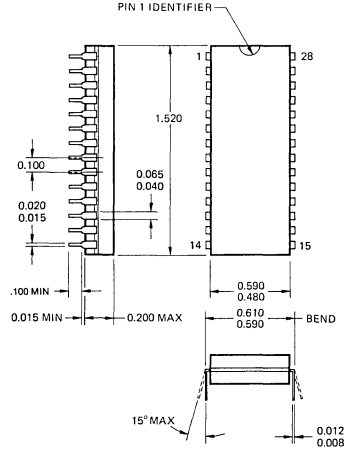
24-Lead Chip Carrier



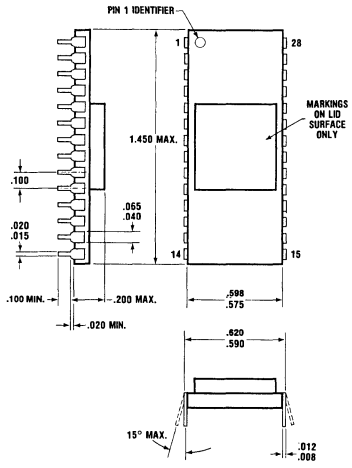
28-Pin Plastic



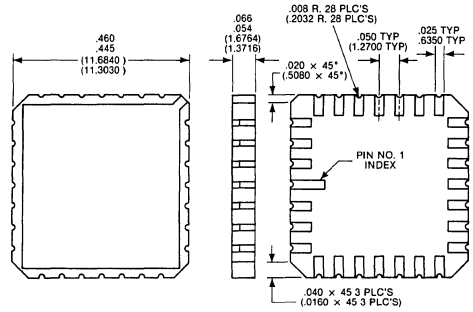
28-Pin Cerdip



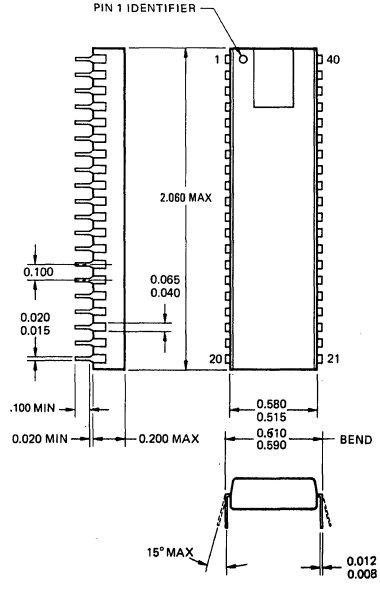
28-Pin Ceramic



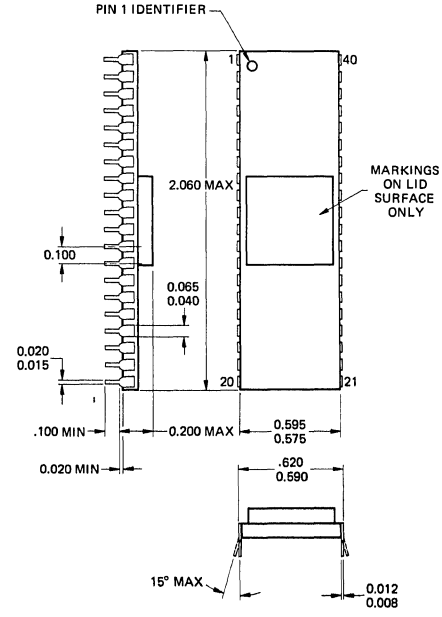
28-Lead Chip Carrier



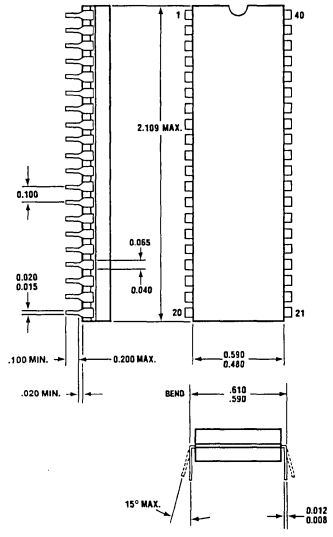
40-Pin Plastic



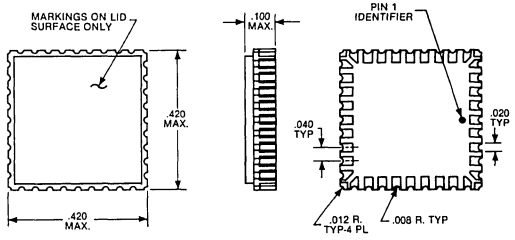
40-Pin Ceramic



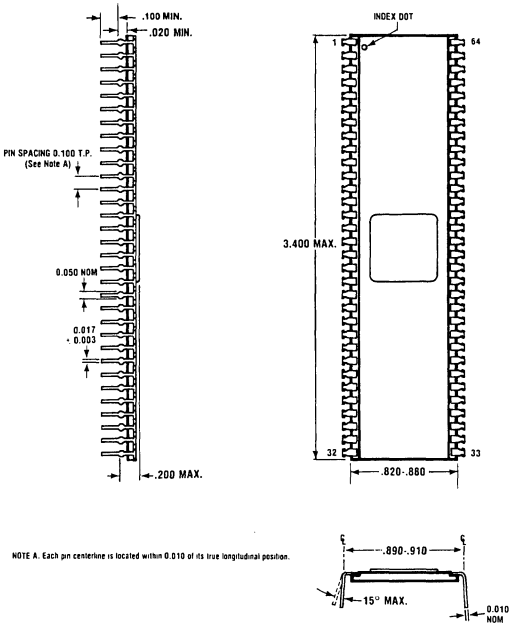
40-Pin Cerdip



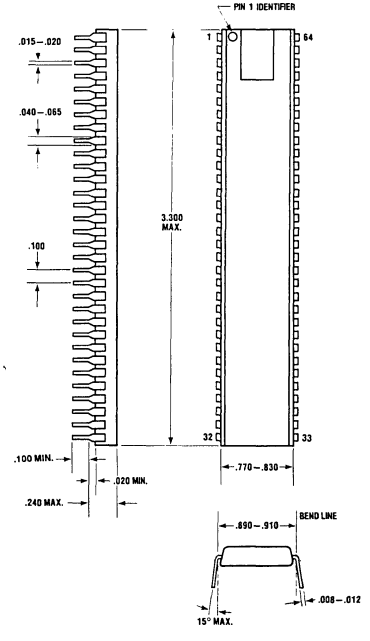
40-Lead Chip Carrier



64-Pin Ceramic



64-Pin Plastic



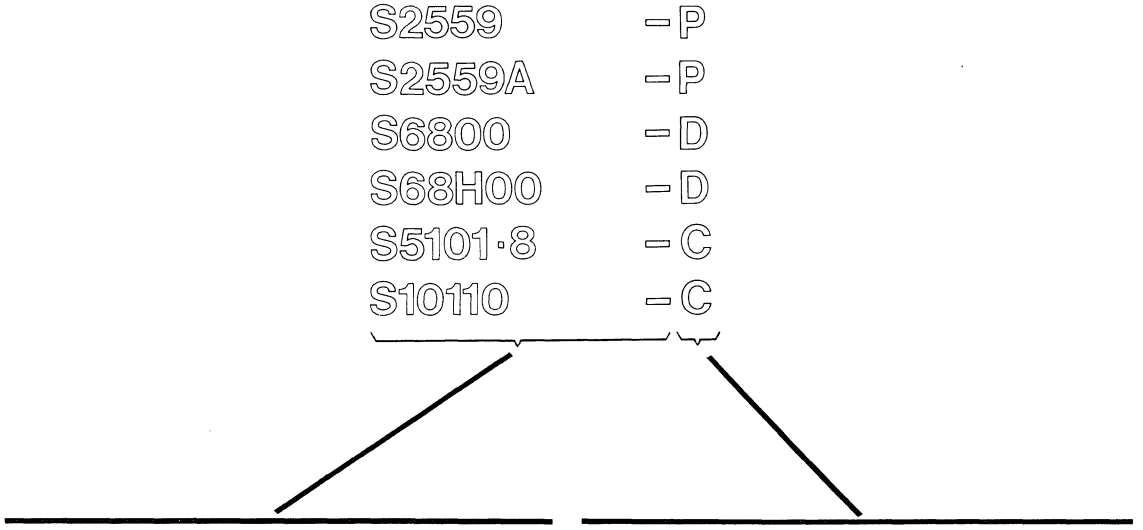
Ordering Information

Standard Products:

Any product in this MOS Products Catalog can be ordered using the simple system described below. With this system it is possible to completely specify any standard device in this catalog in a manner that is compatible with AMI's order processing methods. The example below shows how this ordering system works and will help you to order your parts in a manner that can be expedited rapidly and accurately.

All orders (except those in sample quantities) are normally shipped in plastic carriers or aluminum tube containers, which protect the devices from static electricity damage under all normal handling conditions. Either container is compatible with standard automatic IC handling equipment.

Any device described in this catalog is an AMI Standard Product. However, ROM devices that require mask preparation or programming to the requirements of a particular user, devices that must be tested to other than AMI Quality Assurance standard procedures, or other devices requiring special masks are sold on a negotiated price basis.



Device Number — prefix S, followed by four (or five*) numeric digits that define the basic device type. Versions to the basic device are indicated by an additional alpha or numeric digit as shown in the above examples.

*Organ Circuits

Package Type — a single letter designation which identifies the basic package type. The letters are coded as follows:

P — Plastic package

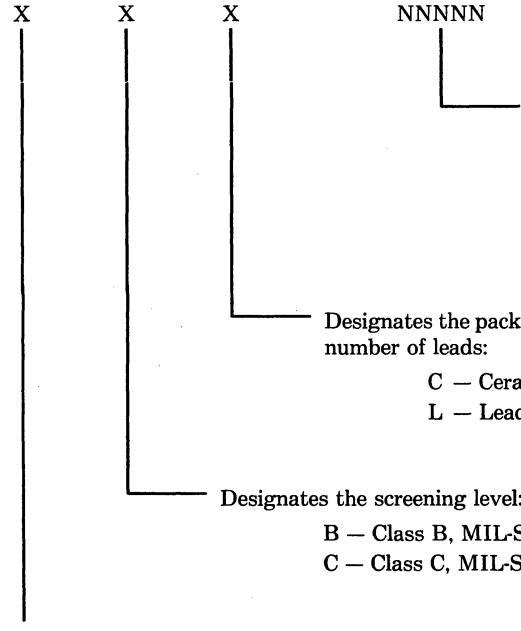
D — Cerdip package

C — Ceramic (three-layer) package

Military Products:

Parts Numbering Format

Examples
MBC 6802
LBC 68A00
MBL UA-3



Four to seven alpha numerics specifying the basic part number (die type) and including a power/speed selection as applicable. For example, 6802 indicates an 8-bit microprocessor with clock and RAM; 5101L-4 specifies a CMOS 256×4 static RAM with 0.055mW maximum standby power and 650ns maximum access time; and UA-3, a 540 gate CMOS uncommitted logic array.

Designates the package and utilizes one of the following letters regardless of the number of leads:

C — Ceramic dual in-line
L — Leadless chip carrier, ceramic, 50 mil pin spacing

Designates the screening level:

B — Class B, MIL-STD-883, Method 5004.5
C — Class C, MIL-STD-883, Method 5004.5

Designates the operating temperature range and utilizes one of the letters M or L. Definitions:

M—Full military temperature range, −55°C to +125°C
L —Limited military temperature range, −55°C to +85°C

Ordering Information

Please specify part numbers in accordance with the parts numbering format above.

TERMS OF SALE

OCTOBER 1981

1. **ACCEPTANCE:** THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold or sold hereunder. Prices for the items called for hereby are not subject to audit.

2. **PAYMENT:**

(a) Unless otherwise agreed, all invoices are due and payable thirty (30) days from date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and conditions or security satisfactory to such department.

(b) If, in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.

(c) Each shipment shall be considered a separate and independent transaction, and payment therefor shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.

3. **TAXES:** Unless otherwise provided herein, the amount of any present or future sales, revenue, excise or other taxes, fees, or other charges of any nature, imposed by any public authority, (national, state, local or other) applicable to the products covered by this order, or the manufacture or sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof, the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authority.

4. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer, and Seller's liability as to delivery ceases upon making delivery of material purchased hereunder to carrier at shipping point, the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Shipments will normally be made by Parcel Post, United Parcel Service (UPS), Air Express, or Air Freight. Unless specific instructions from Buyer specify which of the foregoing methods of shipment is to be used, the Seller will exercise his own discretion.

5. **DELIVERY:** Shipping dates are approximate and are based upon prompt receipt from Buyer of all necessary information. In no event will Seller be liable for any re-procurement costs, nor for delay or non-delivery, due to causes beyond its reasonable control including, but not limited to, acts of God, acts of civil or military authority, priorities, fires, strikes, lockouts, slow-downs, shortages, factory or labor conditions, yield problems, and inability due to causes beyond the Seller's reasonable control to obtain necessary labor, materials, or manufacturing facilities. In the event of any such delay, the date of delivery shall, at the request of the Seller, be deferred for a period equal to the time lost by reason of the delay.

In the event Seller's production is curtailed for any of the above reasons so that Seller cannot deliver the full amount released hereunder, Seller may allocate production deliveries among its various customers then under contract for similar goods. The allocation will be made in a commercially fair and reasonable manner. When allocation has been made, Buyer will be notified of the estimated quota made available.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents, trademarks, or unfair competition arising from compliance with Buyer's designs, specifications, or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements.

Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer, so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information, and assistance (at the Seller's expense) for defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is, in such suit, held to constitute infringement of patent, and the use of said product is enjoined, the Seller shall, at its own expense, either procure for the Buyer the right to continue using said product or part, replace same with non-infringing product, modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. In no event shall Seller's total liability to the Buyer under or as a result of compliance with the provisions of this paragraph exceed the aggregate sum paid by the Buyer for the allegedly infringing product. The foregoing states the entire liability of the Seller for patent infringement by the said products or any part thereof. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.

7. **INSPECTION:** Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the material. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.

8. **LIMITED WARRANTY:** The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED, STATUTORY, OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not finished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as is where is.

9. **PRODUCTS NOT WARRANTED BY SELLER:** The second paragraph of Paragraph 6, Patents, and Paragraph 8, Limited Warranty, above apply only to integrated circuits of Seller's own manufacture. IN THE CASE OF PRODUCTS OTHER THAN INTEGRATED CIRCUITS OF SELLER'S OWN MANUFACTURE, SELLER MAKES NO WARRANTIES EXPRESSED, STATUTORY OR IMPLIED INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY, FREEDOM FROM PATENT INDEMNITY AND FITNESS FOR A PARTICULAR PURPOSE. Such products may be warranted by the original manufacturer of such products. For further information regarding the possible warranty of such products contact Seller.

10. **PRICE ADJUSTMENTS:** Seller's unit prices are based on certain material costs. These materials include, among other things, gold packages and silicon. Adjustments shall be as follows:

(a) Gold. The price at the time of shipment shall be adjusted for increases in the cost of gold in accordance with Seller's current Gold Price Adjustment List. This adjustment will be shown as a separate line item on each invoice.

(b) Other Materials. In the event of significant increases in other materials, Seller reserves the right to renegotiate the unit prices. If the parties cannot agree on such increase, then neither party shall have any further obligations with regard to the delivery or purchase of any units not then scheduled for production.

11. **VARIATION IN QUANTITY:** If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent (5%) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity order.

12. **CONSEQUENTIAL DAMAGES:** In no event shall Seller be liable for special, incidental or consequential damages.

13. **GENERAL:**

(a) The validity, performance and construction of these terms and all sales hereunder shall be governed by the laws of the State of California.

(b) The Seller represents that with respect to the production of articles and/or performance of the services covered by this order it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended, Williams-Steiger Occupational Safety and Health Act of 1970, Executive Orders 11375 and 11246, Section 202 and 204.

(c) The Buyer may not unilaterally make changes in the drawings, designs or specifications for the items to be furnished hereunder without Seller's prior consent.

(d) Except to the extent provided in Paragraph 14, below, this order is not subject to cancellation or termination for convenience.

(e) If Buyer is in breach of its obligations under this order, Buyer shall remain liable for all unpaid charges and sums due to Seller and will reimburse Seller for all damages suffered or incurred by Seller as a result of Buyer's breach. The remedies provided herein shall be in addition to all other legal means and remedies available to Seller.

(f) Buyer acknowledges that all or part of the products purchased hereunder may be manufactured and/or assembled at any of Seller's facilities domestic or foreign.

(g) Unless otherwise agreed in a writing signed by both Buyer and Seller, Seller shall retain title to and possession of all tooling of any kind (including but not limited to masks and pattern generator tapes) used in the production of products furnished hereunder".

14. **GOVERNMENT CONTRACT PROVISIONS:** If Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Defense Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be - i.e., "Contracting Officer" shall mean "Buyer", "Contractor" shall mean "Seller", and the term "Contract" shall mean this order:

7-103.1, Definitions; 7-103.3, Extras; 7-103.4, Variation in Quantity; 7-103.8, Assignment of Claims; 7-103.9, Additional Bond Security; 7-103.13, Renegotiation; 7-103.15, Rhodesia and Certain Communist Areas; 7-103.16, Contract Work Hours and Safety Standards Act - Overtime Compensation; 7-103.17, Walsh-Healey Public Contracts Act; 7-103.18, Equal Opportunity Clause; 7-103.19, Officials Not to Benefit; 7-103.20, Covenant Against Contingent Fees; 7-103.21, Termination for Convenience of the Government (only to the extent that Buyer's contract is terminated for the convenience of the government); 7-103.22, Authorization and Consent; 7-103.23, Notice and Assistance Regarding Patent Infringement; 7-103.24, Responsibility for Inspection; 7-103.25, Commercial Bills of Lading Covering Shipments Under FOB Origin Contracts; 7-103.27, Listing of Employment Openings; 7-104.4, Notice to the Government of Labor Disputes; 7-104.11, Excess Profit; 7-104.15, Examination of Records by Comptroller General; 7-104.20, Utilization of Labor Surplus Area Concerns.

Product Assurance Program

INTRODUCTION

Quality is one of the most used, least understood, and variously defined assets of the semiconductor industry. At AMI we have always known just how important effective quality assurance, quality control, and reliability monitoring are in the ability to deliver a repeatably reliable product. Particularly, through the manufacture of custom MOS/LSI, experience has proved that one of the most important tasks of quality assurance is the effective control and monitoring of manufacturing processes. Such control and monitoring has a twofold purpose: to assure a consistently good product, and to assure that the product can be manufactured at a later date with the same degree of reliability.

To effectively achieve these objectives, AMI has developed a Product Assurance Program consisting of three major functions:

- ☐ Quality Control
- ☐ Quality Assurance
- ☐ Reliability

Each function has a different area of concern, but all share the responsibility for a reliable product.

The AMI Product Assurance Program

The program is based on MIL-STD-883, MIL-M-38510, and MIL-Q-9858A methods. Under this program, AMI manufactures highest quality MOS devices for all segments of the commercial and industrial market and, under special adaptations of the basic program, also manufactures high reliability devices to full military specifications for specific customers.

The three aspects of the AMI Product Assurance Program—Quality Control, Quality Assurance, and Reliability— have been developed as a result of many years of experience in MOS device design and manufacture.

Quality Control establishes that every method meets or fails to meet, processing or production standards—*QC checks methods.*

Quality Assurance establishes that every method meets, or fails to meet, product parameters—*QA checks results.*

Reliability establishes that QA and QC are effective—*Reliability checks device performance.*

One indication that the AMI Product Assurance Program has been effective is that NASA has endorsed AMI products for flight quality hardware since 1967. The Lunar Landers and Mars Landers all have incorporated AMI circuits, and AMI circuits have also been utilized in the Viking and Vinson programs, as well as many other military airborne and reconnaissance hardware programs.

QUALITY CONTROL

The Quality Control function in AMI's Product Assurance Program involves constant monitoring of all aspects of materials and production, starting with the raw materials purchased, through all processing steps, to device shipment. There are three major areas of Quality Control:

- ☐ Incoming Materials Control
- ☐ Microlithography Control
- ☐ Process/Assembly Control

Incoming Materials Control

All purchased materials, including raw silicon, are checked carefully to various test and sampling plans. The purpose of incoming materials inspection is to ensure that all items required for the production of AMI MOS circuits meet such standards as are required for the production of high quality, high reliability devices.

Incoming inspection is performed to specifications agreed to by suppliers of all materials. The Quality Control group continuously analyzes supplier performance, performs comparative analysis of different suppliers, and qualifies the suppliers.

Tests are performed on all direct material, including packages, wire, lids, eutectics, and lead frames. These tests are performed using a basic sampling plan in accordance with MIL-S-19500, generally to a Lot Tolerance Percent Defective (LTPD) level of 10%. The AQL must be below 1% overall.

Two incoming material inspection sequences illustrate the thoroughness of AMI Quality Control:

- ☐ Purchased packages are first inspected visually. Then, dimensional inspections are performed, followed by a full functional inspection, which subjects

the packages to an entire production run simulation. Finally, a full electrical evaluation is made, including checks of the insulation, resistance, and lead-to-lead isolation. A package lot which passes these tests to an acceptable LTPD level is accepted.

- ☐ Raw silicon must also pass visual and dimensional checks. In addition, a preferential etch quality inspection is performed. For this inspection, the underlayers of bulk silicon are examined for potential anomalies such as dislocation, slippage or etch pits. Resistivity of the silicon is also tested.

Microlithography Control

Microlithography involves the processes which result in finished working plates, used for the fabrication of wafers. These processes are pattern or artwork generation, photo-reduction, and the actual printing of the working plates.

Pattern generation now is the most common practice at AMI. The circuit layout is digitized and stored on a tape, which then is read into an automated pattern generator which prints a highly accurate 10x reticle directly.

In cases where the more traditional method of artwork generation is used whether Rubylith, Gerber Plots, AMI generated or customer generated—the artwork is throughly inspected. It is checked for level-to-level registration and dimensional tolerances. Also, a close visual inspection of the workmanship is made. AMI artwork is usually produced at 200x magnification and must conform to stringent design rules, which have been developed over a period of years as part of the process control requirements.

Acceptable artwork is photographically reduced to a 20x magnification, and then further to a 10x magnification. The resulting 10x reticles are then used for producing 1x masters. The masters undergo severe registration comparisons to a registration master and all dimensions are checked to insure that reductions have been precise. During this step, image and geometry are scrutinized for missing or faded portions and other possible photographic omissions.

For a typical N-Channel silicon gate device, master sets are checked at all six geometry levels in various combinations against each other and against a proven master set. Allowable deviations within the die are limited to 0.5 micron, deviations within a plate are limited to 1 micron, and all plate deviations are considered cumulatively.

Upon successful completion of a device master set, it is released to manufacturing where the 1x plates are printed. A sample inspection is performed by manufacturing on each 30-plate lot and the entire lot is returned to Quality Control for final acceptance. Quality Control performs audits on each manufacturing inspector daily, by sample inspection techniques.

The plates can be rejected first by manufacturing, when the 30-plate lots are inspected, or by Quality Control when the lots are submitted for final acceptance. If either group rejects the plates, they are rescreened and then undergo the same inspection sequence. In the rescreening process, the plates undergo registration checks; visual checks for pin holes, protrusions, and faded or missing images, as well as all critical dimension checks.

Process Control

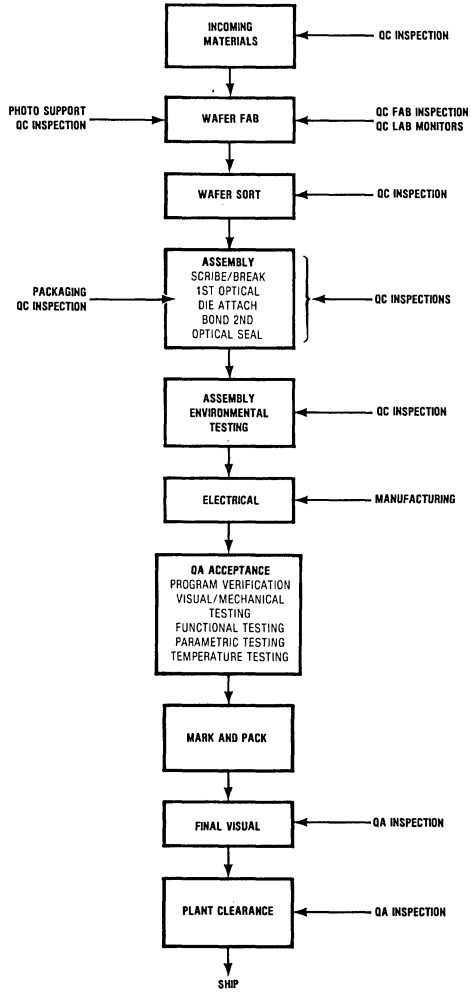
Once device production has started in manufacturing, AMI Quality Control becomes involved in one of the most important aspects of the Product Assurance Program—the analysis and monitoring of virtually all production processes, equipment, and devices.

Process controls are performed in the fabrication area, by the Quality Control Fabrication Group, to assure adherence to specifications. This involves checks on operators, equipment and environment. Operators are tested for familiarity with equipment and adherence to procedure. Equipment is closely checked both through calibration and maintenance audits. Environmental control involves close monitoring of temperature, relative humidity, water resistivity and bacteria content, as well as particle content in ambient air. All parameters are accurately controlled to minimize the possiblity of contamination or adverse effects due to temperature or humidity excesses.

Experience has proven that such close control of the operators, equipment, and environment is highly effective towards improved quality and increased yields.

In addition to the specification adherence activities of the QC Fabrication Group, a QC Laboratory performs constant process monitoring of virtually every step of all processes. Specimens are taken from all production steps and critically evaluated. Sampling frequency varies, depending on the process, but generally, oxidation, diffusion, masking, and evaporization are the most closely monitored steps.

Figure 1. Flowchart of Product Assurance Program Implementation



Results are supplied both to manufacturing and engineering. When evidence of a problem occurs, QC provides recommendations for corrections and follows up the corrective action taken.

Optical Inspections are performed at several steps; quality control limits are based on a 10% LTPD. The chart in Figure 1 shows process steps and process control points.

QUALITY ASSURANCE

The Quality Assurance function in the Product Assurance Program involves checking the ability of manufactured parts to meet specifications. In addition, the QA group also is responsible for calibration of all equipment, and for the maintenance of AMI internal product specifications, to assure that they are always in conformance with customer specifications or other AMI specifications.

After devices undergo 100% testing in manufacturing, they are sent to Quality Assurance for acceptance. Lots are defined, and using the product specifications, sample sizes are determined, along with the types of tests to be performed and the test equipment to be used. Lots must pass QA testing a 0.1% AQL.

Three types of tests are performed on the samples: visual/mechanical, parametric, and functional. All tests are performed both at room temperature and at elevated temperature. In addition, a number of other special temperature tests may be performed if required by the specification.

To perform the tests, QA uses AMI PAFT test systems, ROM test systems, Macrodata testers, Fairchild *Sentry*, LTX *Sentinel*, *XINCOM* systems, Teradyne test systems, and various bench test units. In special instances a part may also be tested in a real life environment in the equipment which is to finally utilize it.

If a lot is rejected during QA testing, it is returned to the production source for an electrical rescreening. It is then returned to QA for acceptance but is identified as a resubmitted lot. If it fails again, corrective action in engineering is initiated. As evidence of the problem is detected, the parts may also be traced all the way back to the wafer run to analyze the cause.

When a lot is acceptable, it is sent to packaging and then to finished goods. When parts leave finished goods, they are again checked by the QA group to a 10% LTPD with visual/mechanical tests. Also, all supporting documentation for the parts is verified, including QA acceptance, special customer specifications, certificates of compliance, etc. Only after this last check are devices considered ready for plant clearance.

If there are customer returns, they are first sample tested

by QA to determine the cause of the return. (Many times an invalid customer test will incorrectly cause returns.) Selected return samples are sent to Reliability for failure analysis.

RELIABILITY

The Reliability function in the Product Assurance Program involves process qualification, device qualification, package qualification, reliability program qualification and failure analysis. To perform these functions AMI Reliability group is organized into two major areas:

- ☐ Reliability Laboratory
- ☐ Failure Analysis

Reliability Laboratory

AMI Reliability Laboratory is responsible for the following functions.

- ☐ New Process Qualification
- ☐ Process Change Qualification
- ☐ Process Monitoring
- ☐ New Device Qualification
- ☐ Device Change Qualification
- ☐ New Package Qualification
- ☐ Device Monitoring
- ☐ Package Change Qualification
- ☐ Package Monitoring
- ☐ High Reliability Programs

There are various closely interrelated and interactive phases involved in the development of a new process, device, package or reliability program. A process change may affect device performance, a device change may affect process repeatability, and a package change may affect both device performance and process repeatability. To be effective. the Reliability Laboratory must monitor and analyze all aspects of new or changed processes, devices, and packages. It must be determined what the final effect is on product reliability, and then evaluate the merits of the innovation or change.

Process Qualification

For example, AMI Research and Development group recommends a new process or process alteration when it feels that the change can result in product improvement. The Reliability Laboratory then performs appropriate environmental and electrical evaluations of a new process. Typically, a special test vehicle, or "rel chip", generated by R&D during process development, is used to qualify the recommended new process or process change.

The rel chip is composed of circuit elements similar to those that may be required under worst-case circuit design conditions. The rel chip elements are standard for any given process, and thus allow precise comparisons between diffusion runs. The following is an example of what is included on a typical rel chip:

- ☐ A discrete inverter and an MOS capacitor
- ☐ A large P-N junction covered by an MOS capacitor.
- ☐ A large P-N junction area (identical to the junction area above, but without the MOS capacitor)
- ☐ A large area MOS capacitor over substrate
- ☐ Several long contact strings with different contact geometries
- ☐ Several long conductor geometries, which cross a series of eight deeply etched areas

Each circuit element of a rel chip allows a specific test to be performed. As an example, the discrete inverter and MOS load device accommodate power life tests. As a consequence, any type of parameter drift can be observed. The MOS capacitor, covering the large P-N junction, can serve to indicate the presence of contamination in the oxide, under the oxide, or in the bulk silicon. If unusual drift is evidenced, the location of contamination can be determined through analysis of the additional MOS capacitor and the large P-N junction area. The metal conductor interconnecting contacts is useful for life testing under relatively high current conditions. It facilitates the detection of metal separation when moisture or other contaminants are present.

The conductors crossing deeply etched areas allow the checking of process control. Rather than depending upon optical inspection of metal quality, burned out areas caused by high currents are readily identified and provide a quantitative measure of metal quality.

If the Reliability Laboratory determines that a recommended new process or process change is viable for manufacturing purposes, further analysis is necessary to determine that production devices can be manufactured in high volume, in a repeatable and reliable manner.

Process Monitoring

In addition to process qualification, the Reliability group also conducts ongoing process monitoring programs. Once every 90 days each major production process is evaluated using rel chips as test vehicles. The resulting test data is analyzed for parameter limits and process stability. In this manner AMI can help assure repeatability and high product quality.

Package Qualification

New packages are also qualified before they are adopted. To analyze packages, a qualification matrix is designed, according to which the new package and an established package (used for control) are tested concurrently. The test matrix consists of a full spectrum of electrical and environmental stress tests, in accordance with MIL-STD-883.

Failure Analysis

Another important function of the Reliability group is failure analysis. Scanning electron microscopes, high power optical microscopes, diagnostic probe stations, and other equipment is used in failure analysis of devices submitted from various sources. It is the function of the Reliability group to determine the cause of failure and recommend corrective action.

The Reliability group provides a failure analysis service for the previously mentioned in-house programs and for the evaluation of customer returns. All AMI customers are provided a failure analysis service for any part that fails within one year from date of purchase and the results of the analysis are returned in the form of a written report.

SUMMARY

The Product Assurance Program at AMI is oriented towards process control and monitoring, and the evaluation of devices. The Program consists of three major functions: Quality Control, Quality Assurance, and Reliability. Constant monitoring of all phases of production, with information feedback at all levels, allows fast and efficient detection of problems, evaluation and analysis, correction, and verification of the correction. The overall result is a line of products which are highly repeatable and reliabile, with a very low reject level.

Terms and Definitions

At one time each discipline had its own set of specific terms and definitions, and although the basic electrical terms were common, the rest usually were not.

As time goes on, however, the various disciplines meet and merge because of their need to communicate. As a result, the basic terms of the telephone network need to be understood by the computer data communications people, and those who used to send information by a twisted pair of wires may find the new path over microwave radio, fiber optics, or a light beam through the air.

This glossary will be seen as a modest attempt to collect those various terms together in one place, not just to highlight the specific products elsewhere in the book, but to provide a little light on each of several disciplines.

A/B signaling—A special case of 8th-bit signaling to allow 4 logic states to be multiplexed in with the voice on PCM channels in the μlaw system.

ACD (automatic call distributor)—A switching system that automatically distributes incoming calls to a centralized group of receivers in the sequence in which the calls are received. It holds calls until a receiver is available. ACD can be incorporated into, or be separate from, a PBX/PABX system.

AC signaling—Using AC signals or tones to transmit data and/or control signals.

Acoustic coupler—A sound transducer connected to a modem that permits use of a telephone handset as a connection to the telephone-company network for data-transmission purposes.

ACU (automatic calling unit)—A device that automatically places a telephone call upon receiving information from a data-processing device.

A/D (analog to digital converter)—Converts an analog signal sample to a digital representation suitable for digital processing and switching.

AIOD (automatically identified outward dialing)—A means for identifying stations within the system placing long distance toll calls. AIOD provides a station-by-station itemization of long distance charges.

A Law—A CCITT-suggested standard for companding, using the equations:

$$F(x) = \operatorname{sgn}(x)\ \frac{1+\ln(A\,|\,x\,|)}{1+\ln(A)} \qquad \frac{1}{A} \leq x \leq 1$$

$$F(x) = \operatorname{sgn}(x)\ \frac{A\,|\,x\,|}{1+\ln A} \qquad 0 \leq x \leq \frac{1}{A}$$

where A is set equal to 87.6.

Aliasing noise—A distortion component which will be created when frequencies present in a sampled signal are greater than ½ the sample rate.

Anti-aliasing filter—A filter (normally low pass) which band limits the input signal BEFORE sampling to avoid aliasing noise.

Algorithm—A prescribed set of well-defined rules or processes for finding a problem's solution.

Alphanumeric—Consisting of letters and numbers

Alternate route—A secondary communication path used to reach a destination when the primary one is unavailable.

AM (amplitude modulation)—Transmission of information on a communication link by varying the voltage level (amplitude).

AMA—Automatic message accounting.

Ambient noise—Interference present in a communication line at all times.

Amplitude variation (ripple)—Unwanted signal-voltage variations at different frequencies on a communication line.

ANI (automatic number identification)—Identifies stations placing toll calls for accounting purposes. Also referred to as IOD (identified outward dialing) or AIOD (automatically identified outward dialing).

Answer back—A signal from a receiving data processing device in response to a transmitting one's request indicating that the receiver is ready to accept or has received data.

Answer from any station—Enables a station to divert a non-answered call at another station to his own telephone by dialing 1 or 2 digits (Call Pick-Up).

ARQ (automatic retransmission request)—An error-detection and -correction technique that attempts a retry upon detecting an error.

ASCII (American Standard Code for Information Interchange)—A data communication code set.

ASR—Automatic send/receive.

Asynchronous—Not synchronized by a clocking signal; in code sets, character codes containing start and stop bits.

ATB (all trunks busy)—A mathematical analysis based on calling volumes, duration, distribution of calls, and total number of sequentially switched lines available to handle the calling traffic. Also referred to as Erlang's Lost Call Formula, because an arriving call encountering an ATB condition is lost to the network, i.e., the caller is forced to hang up and redial.

ATC (automated technical control)—A computer system used to maintain control of a data communication network.

AT&T—American Telephone & Telegraph Company.

Attendant conference—Allows the attendant to connect central office (CO) trunks with internal stations speaking to the inside/outside parties privately in turn.

Attenuation—Loss of communication-signal energy.

Automatic dialer—A device that automatically dials telephone numbers on a network.

Automatic supervision—This feature permits the PABX attendant to extend incoming trunk calls without announcement to the called party. In this mode the PABX/PBX supervises the connection and automatically returns the call to the attendant's console if the called station does not answer within a prescribed time.

AWG (American Wire Gauge)—Wire-size standard.

Backup—The hardware and software resources available to recover after a degradation or failure of one or more system components.

Balanced circuit—A circuit terminated by a network whose impedance balances that of the line, resulting in negligible return losses.

Balancing network—Electronic circuitry used to match 2-wire to 4-wire facilities, sometimes called a hybrid. The balancing is necessary to maximize power transfer and minimize echo.

Bandwidth—The information-carrying capability of a communication line or channel.

Baseband—The frequency band that information-bearing signals occupy before they combine with a carrier in the modulation process.

Base group—Twelve communication-set paths capable of carrying the human voice on a telephone set; a unit of frequency-division-multiplexing systems' bandwidth allocation.

Battery (telephone)—48 volt battery (or supply) used to power the telephone set from the central office or PABX.

Baud—A data-communication-rate unit used similarly to bits per second (bps) for low-speed data; the number of signal-level changes per second (regardless of the information the signals contain).

Baudot—A 5-level code set; its formal name is the International Telegraph Alphabet (ITA) #2.

BCH—An error-detecting and -correcting technique used by communication receivers.

Bit rate—The rate at which data bits are transmitted over a communication path, normally expressed in bits per second (bps); not to be confused with the data signaling rate (baud), which measures the rate of signal changes transmitted.

Bit stream—A continuous series of bits transmitted on a link.

Blank—A "no-information" condition in a data-recording medium or storage location. This vacancy can be represented by all spaces or all ZEROs, depending on the medium.

Block—A set of contiguous bits and/or bytes that make up a definable quantity of information.

Blocking—Describes a condition in a switching system in which no paths or circuits are available to complete a call, resulting in a busy tone returned to the calling party. This is because there are more telephones than through connection paths, so dynamic channel allocation is on a demand basis. If all channels are busy, new calls are blocked from completion or are delayed until a channel becomes available.

Non-blocking system—Each telephone has a guaranteed through connection when needed. This may be in the form of a dedicated channel (fixed channel assignment) which guarantees any phone the same communication channel at any time.

Block-multiplexer channel—A computer-peripheral multiplexer channel that interleaves blocks of data. (See byte-multiplexer channel; contrast with selector channel.)

Bridge—Equipment and techniques used to match circuits to each other, ensuring minimum transmission impairment. Bridging is normally required on multi-point data channels where several local loops or channels interconnect.

Broadband—Refers to transmission facilities whose bandwidth is greater than that available on voice-grade facilities. Also called wide band.

Broadcast—To send messages or communicate simultaneously with many or all points in a circuit.

BSC (bisync)—An IBM-developed data-link-control procedure using character synchronization.

BSP—Bell System Practices.

Buffer—A storage area for a data block.

Burst—A group of events occurring together in time.

Burst error—A series of consecutive errors in data transmission.

Bus—A connective link between multiple processing sites (co-located only), where any of the processing sites can transmit to any other, but only one way at a time.

Busy lamp field—The busy lamp field provides a console attendant with a visual indication of the busy/free status of internal PABX/PBX stations.

Busy override—This feature permits the attendant entry into a call in progress to announce important calls. Typically, a warning tone indicates the attendant's entry to the line.

Byte—A set of contiguous bits constituting a discrete item of information. Most common bytes are six or eight bits long.

Byte-multiplexer channel—A channel that interleaves bytes of data from different sources. (Contrast with selector channel.)

Cache memory—A high-speed computer memory that contains the instruction or sequence of instructions most likely to be executed next.

Callback—Allows the station user encountering an internal busy signal to dial a single digit and hang up. When the called party becomes free, both stations are automatically rung and connected (Camp-on).

Call blocking—Permits the attendant to prevent any station(s) from receiving any calls. When this feature is activated, calls to the restricted stations are automatically rerouted to the attendant or to a recorded announcement.

Call forwarding—Typically with electronic PABX/PBX systems, the call forwarding feature permits the user to dial a special 1- or 2-digit code, and then dial the extension to which all calls are to be automatically transferred.

In many PABX/PBX installations, call forwarding is used to classify that feature which reroutes incoming trunk (or station) to the attendant's console when the called station is busy or does not answer within a prescribed number of rings.

Call-setup time—The overall length of time required to establish a switched call between terminal equipment.

Call splitting—Enables the attendant to speak privately with either the outside or local party.

Call waiting—This feature employs a tone which notifies the called party that an additional call was directed to his number. In many systems the user can then "flash the system" (momentarily depress the hook switch, which places the original connection on hold and connects the new call). Successive flashes then can be used to alternate connections between the station and the 2 calls.

Camp-on—Provides the means for extending incoming central office trunk calls to busy PABX/PBX stations. When the busy station becomes idle, ringing to that station is applied automatically. If the camp-on condition is extended beyond a certain time, the attendant is automatically alerted; camp-on may continue unless cancelled by the attendant. See call waiting.

CANTAT—Canadian Transatlantic Telephone underseas cables.

Carrier—An analog signal at a fixed amplitude and frequency that combines with an information-bearing signal in the modulation process to produce an output signal suitable for transmission.

Carrier system—A method of obtaining several channels from one communication path by combining them at the originating end, transmitting a wide-band or high-speed signal and recovering the original information at the receiving end.

CC—Common control.

CCIS—Common channel interoffice signaling.

CCITT (Consultative Committee for International Telephone and Telegraph)—An international standards group of the European International Telecommunications Union.

CCS—Hundred (C) calling seconds. A unit of telephone traffic, each call lasting 100 seconds equals one CCS.

CCSA—Common control switching arrangement.

CCU—Common control unit.

CDF—Common distribution frame.

CDO—Community dial office.

Central office (C.O.)—Main telephone office usually located within a few miles of the subscriber that houses switching gear. Most central offices have the capability of handling approximately 10,000 subscribers.

Centrex—An improved Bell System PBX system that allows direct inward dialing (DID).

CEPT—Conference of European Postal Telecommunications Administrations.

CERT (character error-rate testing)—Checking a data line with test characters.

CFE—Customer furnished equipment or CPE for customer provided equipment.

Chain—A series of processing locations through which information must pass on a store-and-forward basis to reach a subsequent location.

Channel—A communication path.

Channel bank—Communication equipment typically used for multiplexing voice-grade channels into a digital transmission signal. Typically 24 channels in the U.S. and 30 channels in Europe.

Character—A language unit coded in bits.

Character parity—Adding an overhead bit to a character code to provide error-checking capability.

Circuit switching—A communication method in which an electrical connection between calling and called stations is established on demand for exclusive circuit use until the connection is released.

Classmarks—Service marks, or classmarks, are used to designate various restrictions that may be applied to individual PABX/PBX stations. Typically these range from unrestricted to fully restricted classes.

Classmarks range between 2 and 20 assignable restriction features depending on the type and manufacture of the PABX/PBX system, and are used to inhibit telephones from accessing outside lines, tie lines, WATS lines, toll call lines, etc.

Clocking—Time-synchronizing communication information.

Cluster—A group of user terminals co-located and connected to one controller, through which each terminal accesses a communication line.

C-message weighting—A curve or filter response that approximates the human ear's response to different frequencies. This curve is used in noise measurements and was developed after experiments with many listeners. An example from the curve illustrates that a tone at 200Hz is 25dB less disturbing than a 1000Hz tone of the same power.

CO—Central Office.

COAM (customer owned and maintained)—Equipment that the customer has purchased and for which the telephone company is not responsible.

Coaxial cable—2-conductor wire whose longitudinal axes are coincident; cable with a noise shield around a signal-carrying conductor.

Codec—Coder/decoder; an A/D/A converter that digitally codes and decodes analog signals, usually by companding, in the voice-frequency range.

Code call—This feature provides a means (typically coded audible signals) to alert a person who is away from his telephone station. Code calls can be answered from any station by dialing a code-call answer number; this completes a talking path between the calling and called parties, and releases the code-call circuit to process other traffic.

Common mode rejection—The ability of a device having a balanced input to reject a voltage applied simultaneously to both differential input terminals.

Communication-line controller—A hardware unit that performs line-control functions with a modem.

Companding—A nonlinear technique of compressing and expanding analog information to amplify weak signals and attenuate strong ones. It achieves an enhanced signal-to-distortion ratio over the 40-dB or greater input range encountered in telephony.

Compression—Reduction of a signal's dynamic range in such a way that small signal characteristics are maintained. Usually a logarithmic type conversion is used.

Concentrator—An electronic device that interfaces in a store-and-forward mode with multiple low-speed communication lines at a message level and then retransmits those messages to a processing site via one or more high-speed communication lines.

Conditioning—Applying electronic filter elements to a communication line to improve its ability to support higher transmission data rates. (See equalization.)

Conference trunk—A predetermined number of lines available for setting up conference calls. In a meet-me type of conference circuit, individual conferees are con-

tacted, or scheduled. Each dials the same trunk number which interconnects the several users simultaneously. Outside callers can be added to the conference circuit by the attendant.

Connecting block—A cable-termination block where access to circuit connections is available.

Consultation, trunk-to-trunk—This feature permits a PABX station connected to an outside trunk to access a second trunk line by placing the outside party on hold. It is nominally available for consultation, but not for conferencing.

Contention—Competition for use of the same communication facilities; a line-control method in which terminals request or bid to transmit.

Control-line timing—Clock signals between a modem and a communication-line controller unit.

COS—Class of service.

CPFH—Call party/forced hold.

CPFR—Called party/forced release.

CPS (characters per second)—A data-rate unit.

CPU (central processing unit)—The computer control logic used to execute programs.

CR—Call register.

CRC (cyclic redundancy check)—An error-checking control technique utilizing a binary prime divisor that produces a unique remainder.

Crossbar—A type of widely used control-switching system using a crossbar or coordinate switch. Crossbar switching systems suit data switching because they have low-noise characteristics and can handle Touch-Tone dialing.

Crosspoint—The operating contacts or otherwise low impedance path connection over which conversations are routed.

Crosstalk—The unwanted noise in an information channel resulting from cross coupling from another information channel or other noise.

CTS (clear to send)—A control signal between a modem and a controller used to initiate data transmission over a communication line.

CTX—Centrex.

Cursor—A lighted area on a CRT screen used to indicate the next character location to be accessed.

CXR (carrier)—A communication signal used to indicate the intention to transmit data on a line.

D3—The D3 channel bank is a specific generation of AT&T's 24-channel PCM terminal which multiplexes 24 voice channels into a 1.544MHz digital bit stream. Its specifications are essential for any PCM devices to meet.

D/A (digital to analog converter)—Converts a digital word to an analog value. If the digital words are periodic, the output will appear like the output of an S&H.

DAA (data access arrangement)—A telephone-switching-system protective device used to attach uncertified nontelephone-company-manufactured equipment to the network.

Data base—A collection of electronically stored data records.

Data compression—A technique that provides for the transmission of fewer data bits than originally required without information loss. The receiving location expands the received data bits into the original bit sequence.

Data set—See modem.

Data switcher—A system used to connect network lines to a specific data-processing computer port.

dB (decibel)—Power-and-voltage-level-measurement unit.

dBm—Power-level-measurement unit in the telephone industry based on 600Ω impedance and 1004Hz frequency. 0dBm is 1mW at 1004Hz terminated by 600Ω impedance.

dBmO—Power level (in dBm) referred to the zero-transmission-level point (OTLP); dBm is the absolute power level referenced to 1mW, while OTLP is the system point of zero relative to transmission.

dBmOp—Circuit noise in dBmO measured on a line with a noise measuring set having psophometric weighting.

dBr—dB relative to point of zero transmission level.

dBrn (decibels above reference noise)—Weighted circuit noise power in dB referred to 1 picowatt (−90 dBm) which is defined as OdBrn. Type of weighting is indicated by next letter (see dBrnc).

dBrnc—Weighted circuit noise power in dBrn, measured on a line by a noise measuring set with C message weighting.

dBrncO—Noise measured in dBrnc referred to zero transmission level point.

DCE (data communication equipment)—Equipment (such as a modem) installed at a user's premises that provides all the functions required to establish, maintain and terminate a connection and signal conversion and coding

between the data terminal equipment and common carrier's line.

DDD (direct distance dial)—The North American telephone dial system that allows subscribers to direct distance dial through the intertoll networks without operator assistance.

DDS—Digital Data Service.

Dedicated line—A communication line that isn't dialed, also termed a leased or private line.

Delay distortion—Distortion that occurs on communication lines due to signals' different propagation speeds at different frequencies. Measured in microseconds of delay relative to the delay at 1700Hz. This type of distortion doesn't affect voice communication, but can seriously impair data transmissions.

Delta modulation—A simple digital coding technique that produces a serial bit stream describing changes in analog input levels; usually utilized in devices employing continuously variable-slope delta (CVSD) modulation.

Demodulator—A functional section of a modem that converts received analog line signals to digital form.

Dial transfer—Permits the called station to automatically transfer an incoming call to another station without attendant intervention.

Dial up—The use of a rotary-dial or Touch-Tone® phone to initiate a station-to-station call.

Dictation access—Dictation services at a central dictation machine facility which is accessed by dialing an assigned number. Subsequent control of the dictation machine is performed by dialing single digit codes (e.g., 1=record, 2=advance, 3=stop, etc.).

DID (direct inward dialing)—Permits internal PBX/PABX stations to be accessed directly through the dialup network without local attendant intervention.

DOD (direct outward dialing)—Permits PABX/PBX stations to access central office trunks without attendant intervention.

Distortion—Failure to reproduce the original signal. Distortion has many forms, including amplitude, phase, delay, etc.

DTMF—Dual tone, multi-frequency dialing. See tone dialing.

DMA—Direct memory access from I/O and peripheral controllers without going through the arithmetic processing unit.

DPS—Dial pulse sender.

DQM (data-quality monitor)—A device used to measure data bias distortion above or below a threshold.

DSS—Direct station selection.

DTE (data-termination equipment)—Equipment that constitutes the data source and/or data sink and provides for the communication control function protocol; it includes any piece of equipment at which a communication path begins or ends.

EBCDIC (extended binary coded decimal interchange code)—An 8-level code set used frequently in data communication.

Echo distortion—A telephone-line impairment caused by electrical reflections at distant points where line impedances are dissimilar.

EIA (Electronic Industries Association) RS-232—The standard interface between a modem and line controller for voice-grade communication lines.

Eighth-bit signaling—During a signaling frame, signaling information is inserted into the eighth (LSB) bit position of each PCM word of each channel in the frame. Also called A/B signaling.

Electronic switching system (ESS)—A type of telephone switching system that uses a special-purpose digital computer to direct and control the switching operation. ESS permits custom-calling services such as speed dialing, call transfer and 3-way calling.

Encryption—The technique of modifying a known bit stream on a transmission line to make it appear like a random sequence of bits to an unauthorized observer.

Envelope delay—An analog line impairment where a variation of signal delay with frequency occurs across the data-channel bandwidth. (See delay distortion.)

EO—End Office (Class V, Serving, or Central Office).

Equalization—A technique used to compensate for distortions present on a communication channel. Equalizers add loss or delay to signals in inverse proportion to the channel characteristics. The signal response curve is then relatively "flat" and can be amplified to regain its original form. (See distortion.)

ESS—Electronic switching systems.

ESSS—Electronic subscriber switching system.

Executive right-of-way—Provides the capability of overriding a busy line condition. A typical application is when a busy signal is received from a station within the PABX/PBX system, EROW can be accomplished by dialing a single additional digit within 8 to 10 seconds.

This causes a warning tone to sound, alerting both talking parties that their connection is being entered.

Expansion—Expansion of a compressed signal back to its original dynamic range.

F1F2—A type of modem that operates over a half-duplex line (2-wire) to produce two subchannels at two different frequencies for low-speed full-duplex operation. (See reverse channel.)

Facility—A transmission path between two or more locations without terminating or signaling equipment. Adding terminating equipment would produce either a channel, a central-office line or a trunk.

FASN—Free access to selected numbers.

FDM (frequency-division multiplexing)—A technique in which a data line's bandwidth is divided into different frequency subchannels. It permits several terminals to share the same line.

FE (format effectuation)—Characters of a code set used to format information to be sent for processing.

FEC (forward error correcting)—Used to describe equipment that corrects transmission errors at a receiver. The technique provides for transmission of additional information with the original bit stream so that if an error is detected, the receiver can recreate the correct information without a retransmission.

FEX (Foreign Exchange Service)—The extension of a trunk line beyond its normal (local) central office to a more distant (foreign) central office.

Fiber optics—A technology employing plastic or glass fibers that carry light representing information.

Filter—Electronic circuitry that blocks some signal components while allowing other components to pass through uniformly.

Firmware—A set of software instructions placed permanently or temporarily in a read-only memory (ROM).

Flag—A delimiting bit field used to separate portions of data.

Flexible disk (floppy disk)—A magnetic storage medium constructed of thin plastic.

FM (frequency modulation)—A method of transmitting digital information on an analog link by varying the carrier frequency.

Format—A message or data structure that allows identification of specific control codes or data by their position during processing.

Frame—Time-division multiplexing on Bell System T1 PCM lines combines 24 digitally encoded voice channels (formatted in 8-bit words) into a 192-bit block plus one framing bit to form a 193-bit frame. By international agreement, frames are produced at an 8kHz sampling rate (once every 125μsec); for T1 systems this figure translates to 1.544M bps. Systems conforming to CCITT specifications produce 32 8-bit-long time slots per frame. Utilizing the same sampling rate as Bell, but with 256 bits per frame, the European data rate equals 2.048M bps. Framing bits are unnecessary with this method because the convention reserves two slots per frame for framing and signaling information.

Frequency offset—Analog-line frequency change, or translation; an impairment encountered on a communication line.

Frequency shift keying (FSK)—A form of frequency modulation in which the carrier frequency is made to vary or change in frequency precisely when a change in the state of a transmitted signal occurs.

Frequency stacking—Another name for FDM that describes how the multiplexing is performed.

Front end—An auxiliary computer system that performs network control operations, releasing the host computer system to process data.

Full duplex (FDX)—A 4-wire circuit or protocol that provides for simultaneous transmission in both directions between two points.

Full/full duplex—A protocol for a multidrop line that permits transmission from a master location to a slave site; the master location can also simultaneously receive a transmission from another slave site on that line.

FX—Foreign Exchange. See FEX.

Gain—The degree to which a signal's amplitude is increased. The amount of amplification realized when a signal passes through an amplifier or repeater, normally measured in decibels.

Gain tracking error—A measurement of the dependence of gain on signal level. The output signal is compared to the input signal (assuming unity gain) over a range of input signals. The variation of gain from a constant gain (determined at 0dBm input level) is the gain tracking error.

Gaussian noise—Noise whose amplitude is characterized by the Gaussian distribution (e.g., white noise, ambient noise, hiss).

Group channel—A unit or method of organization on telephone carrier (multiplex) systems. A full group is a channel equivalent to 12 voice-grade channels (48kHz). A half group has the equivalent bandwidth of six voice-grade channels (24kHz). When not subdivided into voice facilities, group channels can furnish high-speed data communication.

Guard frequency—Describes the frequencies between subchannels in FDM systems used to guard against subchannel interference.

Half duplex—A communication line consisting of two wires or employing a protocol capable of transmitting in only one direction at a time.

Hamming code—An FEC technique named for its inventor. It corrects single-bit errors.

Handshaking—Line termination interplay to establish a data communication path.

Harmonics—Frequencies that are multiples of a fundamental value.

Harmonic distortion—A data communication line impairment caused by erroneous frequency generation along the line.

HDLC (High level data link control)—A CCITT standard data communication line protocol.

Hit on the line—Describes errors caused by external interference, such as impulse noise resulting from lightning or man-made interference.

Hold—Consultation or dial inquiry. Permits a station to call another station while placing the original incoming/outgoing call on hold.

Hold-Music/message—Provides background music or recorded announcements to an incoming caller placed on hold.

House cables—Conductors inside a building used to connect communication equipment to outside lines.

HRC (horizontal redundancy checking)—A validity-checking technique used on data transmission blocks in which redundant information is included with the information to be checked.

Hunting, consecutive, or group—Provides for the automatic selection of an idle line from a group of extensions. When the dialed extension is busy, a free line from the group is connected without additional dialing.

Non-consecutive—Typically on a "skip from/skip to" basis; the line that is skipped-to can be in a different number group from the number originally dialed.

Hybrid—See balancing network.

Idle channel noise (ICN)—The total signal energy measured at the output of the device or channel under test when the input of the device or channel is grounded. It can be a wideband noise measurement, using a C-message weighting filter to bandlimit the output noise.

Impulse noise—A type of communication line interference characterized by high amplitude and short duration.

Incoming call identification—Used to indicate to the PABX/PBX attendant, by means of an indicator on the console, the type of call (FEX, WATS, local trunk, tie line) that is being processed at the console so the attendant can answer each call with an appropriate response.

Insertion loss—Signal power loss resulting from connecting communication equipment with dissimilar impedance values, or with attenuation.

Intercept—Permits calls to changed or vacant numbers to be rerouted to either the attendant's (or operator's) console or to a recorded announcement device.

Intercom—A subsidiary station-to-station dialing system that is typically employed with key telephone units (KTU) to provide short-range, limited access between various users for internal communication purposes.

IO—Intermediate office.

IOD—Identified outward dialing. See AIOD.

Interference—Refers to unwanted occurrences on communication channels that result from natural or man-made noises and signals.

Intermodulation distortion—An analog line impairment where two frequencies interact to create an erroneous frequency, which in turn distorts the data signal representation.

ITDM (intelligent time division multiplexer)—A multiplexer that assigns time slots on demand rather than on a fixed subchannel-scanning basis. Also termed a statistical multiplexer.

Jitter—Type of analog communication line distortion caused by a signal's variation from its reference timing position, which can cause data transmission errors, particularly at high speeds. This variation can be in amplitude, time, frequency or phase.

Jumbo group—The highest FDM carrier system multiplexing level; it contains 3600 voice frequency (VF) or telephone channels (six master groups).

Key system—A miniature EPABX that accepts 4 to 10 telephone lines and can direct them to as many as 30 telephone sets.

KTS—Key telephone set.

KTU—Key telephone unit.

Leased line (private line, dedicated line)—A communication line for voice and/or data rented from a communication carrier.

Line protocol—A control program used to perform data communication functions over network lines. Consists of both handshaking and line control functions that move the data between transmit and receive locations.

Local loop—The access line from either a user terminal or a computer port to the first telephone office along the line path.

Lockout—Denies the PABX/PBX attendant the ability to reenter previously completed incoming CO trunk calls, unless recalled by the called station.

Lockout, line—Permits the switching equipment to go on lockout, and allows the switching path(s) to be disengaged if a station experiences line trouble, or if the equipment is left in an "off hook" condition without originating dialing pulses within a specified length of time.

Logging—Recording data, such as error events or transactions, for future reference.

Longitudinal balance—Common-mode rejection of a telephone circuit.

Long line—A communication line spanning a long distance relative to the local loop.

Loop—The closed loop circuit formed by the subscriber telephone set or equipment and the cable pair and other conductors that connect it to the central office switching equipment.

Loop current—The current flowing in the loop circuit.

Loopback—Directing signals back toward the source at some point along a communication path.

Loop disconnect dialing—The type of dialing done with the rotary dial telephone in which the loop or circuit from a central office is pulsed open or disconnected at a specific rate to indicate digits dialed. The same opening of the circuit can be done with pushbuttons that drive a loop disconnect or pulse dialer circuit. This method is gradually being replaced with tone dialing during which the loop is always closed during calling and the digits are indicated by sending audio tones to the central office. (See tone dialing).

LSB—Least significant bit.

LTS (line test set)—Analog line test unit.

Main distribution frame (MDF)—The cable rack on which all distribution and trunk cables leading into a central office are terminated.

MCC—Miscellaneous common carrier.

Message switching—Routing messages between locations by store and forward techniques in a computer.

Message unit register—See register.

Message waiting—Typically a glow lamp installed on the telephone set that alerts a hotel/motel guest when a message is being held. The message waiting feature is controlled by the attendant. Activation of the message waiting lamp does not prevent the station from originating or receiving calls.

Metering—A means of gathering traffic statistics using registers. Register actuations are referred to as "peg count" (PC), and can be employed to determine all circuits busy conditions relating to trunks, junctors, etc. Metering, measurement, and analysis techniques may vary from simple to quite sophisticated. Path fault peg counting may also be incorporated into the design of a PABX with each PC indicating a continuity check failure. These, and other features can be used to provide early warnings of service degradation within the PABX system.

MFP—Multi-frequency pulsing (tone dialing).

MG (master group)—An FDM carrier-multiplexing level containing 600 voice-frequency channels.

Microcode—A set of software instructions that execute a macro instruction.

MIL-188—A military interface between a modem and line controller equivalent to RS-232.

Modem (data set)—An acronym for a unit that modulates and demodulates digital information from a terminal or computer port to an analog carrier signal for passage over an analog line.

MSB—Most significant bit.

Multifrequency tones (dual tone MF)—Signaling code utilizing a pair of frequencies in the 700-1700Hz range to represent one of 16 possible codes, e.g., digits from 0 to 9 and control characters.

μ-Law—Bell System specified companding technique accepted as the North American standard; its governing equation is:

$$F(x) = \text{sgn}(x) \frac{\ln(1+\mu|x|)}{\ln(1+\mu)} \quad -1 \leq x \leq 1$$

where modern usage sets $\mu = 255$.

Multiplexed line—A data communication line equipped with multiplexers at each end.

Multipoint line—A communication line with several subsidiary controllers sharing time on the line under a central site's control.

NPD—Network protective device.

Night answer—Universal: Enables incoming trunk calls to be answered from any non-restricted station by dialing a 1- or 2-digit number.

Predetermined: Enables preselected stations to intercept incoming CO trunk calls when the attendant is not on duty.

Noise—Any signal different from the intended signal being transmitted.

Numbering plan—In PABX/PBX systems featuring flexible numbering plan assignments, the actual appearance of a station's line at the switching equipment need not correspond directly with the number assigned to that station. Numbers can be assigned without respect to such factors as (1) calling volume, (2) actual physical location of the telephone station, or (3) actual appearance at the switching equipment. Flexible arrangements permit personnel to retain their listed numbers regardless of relocations within the facility.

Older systems, especially step-by-step, or cross-bar with limited common control facilities do not provide this flexibility. Number assignments are determined by actual connection points and traffic load balancing considerations.

Octathorpe—One of the keys in the standard pushbutton telephone designated with the # sign. Commonly referred to as the "pound" or "number" sign.

Off hook—Circuit condition caused when the handset is lifted from the switchhook of the telephone set, i.e., a low DC impedance is placed across the line causing a relay at the central office to be seized when it recognizes the request for service by the loop current flowing.

On hook—Circuit condition caused when the handset is replaced on its cradle, i.e., approximately an open circuit.

On line—A direct connection between a remote terminal and a central processing site.

Open wire—Communication lines that aren't insulated and formed into cables, but are instead mounted on aerial crossarms on utility poles.

OPX—Off premise extension.

OR—Originating register.

PABX—Private Automatic Branch Exchange. The (almost) standard acronym for customer owned, switchable telephone systems providing internal and/or external station-to-station dialing.

Packet mode terminal—Data terminal equipment that can control and format packets and transmit and receive them.

Packet switching—The transfer of data by means of addressed packets whereby interim point-to-point channels are available only during the transmission of one packet. The channel then becomes available for the transfer of packets from the same or other messages. Contrast with circuit switching, where the data network determines the end-to-end routing before the entire message transfer.

PAD (packet assembler/disassembler)—Equipment providing packet assembly and disassembly facilities.

Paging—Permits the attendant and/or individual station users to have automatic access to voice paging systems.

PAM (pulse amplitude modulation)—The representation of an analog signal by pulses at a specific rate. The amplitude of the pulses represent the amplitude of the analog signal at the sample times.

Parity error—An error occurring when the results of the parity calculations at the transmit and receive ends of a system don't agree.

Passband filters—Filters used in modem design to allow only the frequencies within the communication channel to pass while rejecting all frequencies outside the channel.

PBX (Private Branch Exchange)—A class of service in standard Bell System terminology that typically provides for the same service as PABX.

PC (phase corrector)—A part of synchronous modems that adjusts the local data clocking signal to match the incoming receive data sent by the remote clocking signal.

PCM (pulse code modulation)—A method of transmitting data where the signals are sampled and then converted to digital words. These digital words (PCM) are then transmitted serially, typically as 8-bit words.

Phase jitter—An analog line impairment caused by power and communication equipment along the line that shifts the signal phase relationship back and forth.

PM (phase modulation)—Variation of an analog signal's phase in direct relationship to digital input information.

Point-to-point—A communication link connected directly from one site to another.

Polling—A control message sent from a master site to a slave site that serves as an invitation to transmit data to the master site.

Pre-emphasis/de-emphasis—Pre-emphasis is the emphasis or boosting of the frequencies at the high end of the speech spectrum to compensate for their natural roll off. This allows a modulator to maintain a higher average level than with flat response and when de-emphasis is done at the other end of the circuit to restore the original waveforms, high frequency noise is decreased. The result is better signal to noise performance.

Primary center—A Class 3 telephone switching office at the next level above toll center.

Privacy—The techniques used for limiting and/or preventing access to specific system information from otherwise authorized system users.

Propagation delay—The time necessary for a signal to travel from one point in a circuit to another.

Protocol—A formal set of conventions governing the format and control of inputs and outputs between two communicating processes, including handshaking and line discipline.

Psophometric weighting—CCITT standard filter response for simulating the non-linear response of the human ear and the telephone ear piece (see C-Message weighting).

Pulse modulation—Modulating the characteristics of a pulse series in one of several ways to create an information bearing signal. Typical methods involve modifying the pulses' amplitude (PAM), width or duration (PDM), or position (PPM). The most common pulse modulation technique employed in telephone communications is pulse code modulation (PCM), in which the system samples the information signals at regular intervals and transmits a series of pulses in coded form, representing the amplitude of the information signal at the sampling time.

Quadrature distortion—Analog signal distortion frequently found in phase modulation modems.

Quantization distortion—The distortion or noise introduced when a continuous analog signal is converted to discrete digital codes. This varies with step size and is minimized by non-linear companding to attempt to maintain a constant SNR over varying signal levels.

RCC—Radio common carrier.

Reactance—Frequency sensitive communication line impairment causing loss of power and phase shifting.

Receiver—The device in the telephone handset that converts electrical energy to speech, or the device that captures or accepts the signal from the transmission medium, such as a microwave receiver or fiber optic receiver.

Recovery—The actions required to bring a system to a predefined level of operation after a degradation or failure.

Regional center—A Class 1 telephone switching office, the top level in the DDD system.

Register-message—In hotel/motel service, a metering device to tally calls placed from the individual guest rooms.

Register-message unit—At central offices, a metering device used to accumulate message unit charges from trunk lines extending from the associated PABX/PBX facility.

Response time—The time measured from the depression of a terminal's Enter key to the display of the first character of the response at that terminal site.

Reverse channel—An optional feature on some modems that provides simultaneous communication from the receiver to the transmitter on a 2-wire channel. It can be used for message transmission, circuit assurance or breaking and to facilitate certain forms of error control and network diagnostics. Also termed backward channel.

Ringing voltage—20Hz (approximately) of AC at a voltage of 75-105 volts supplied by the central office to ring the subscriber's bell.

RTS (request to send)—An RS-232 control signal between a modem and user's digital equipment that initiates the data transmission sequence on a communication line.

S&H (sample and hold)—A circuit which samples a signal and holds the sampled value until the next sample is taken.

Sampled data system—A system that operates on samples of input analog signals (can be either analog or digital processing or both).

Sampling rate—The frequency at which an analog signal's amplitude is gated into a coder circuit. The Nyquist sampling theorem states that if a band limited signal is sampled at regular intervals and at a rate equal to or greater than twice the highest frequency of interest, the sample contains all the information of the original signal. In telephony, the frequency band of interest ranges from 300 to 3400Hz, so a sampling rate of 8kH provides dc to 4000Hz reproduction.

SCC—Specialized common carriers.

SDLC (synchronous data link control)—An IBM data communication message protocol.

Sectional center—A Class 2 telephone switching office between a regional and a primary center.

Selector channel—A channel designed to operate with only one I/O device at a time. Once the I/O device is selected, a complete record transfers one byte at a time. (Contrast with block multiplexer channel.)

Series calling—This feature automatically returns completed incoming trunk line calls to the attendant as the called station hangs up.

Service codes—Typically single digit codes to access frequently called PABX/PBX stations. (For example; 0=Assistance, 9=Outside Line, 1=Front Desk, etc., etc.). "Routing" may be applied to service codes so that all stations which dial 1 will reach the front desk; however, some stations which dial 2 for room service will reach a kitchen that is different from other stations dialing 2.

Signaling—The transmission of control, or status information between switching systems in the form of dedicated bits or channels of information inserted on trunks with voice data.

Signal to distortion ratio (S/D)—The ratio between the input signal level, and the level of all components that are present when the input signal (usually a 1.020kHz sinusoid) is eliminated from the output signal (by filtering, for example).

Slicing level—A voltage or current level of a digital signal at which a ONE or ZERO can be determined.

Slot—A unit of time in a TDM frame during which a subchannel bit or character is carried to the other end of the circuit and extracted by the receiving TDM unit. (See time slot.)

Smoothing (reconstruction) filter—Restores the desired analog signal at the S&H or D/A output.

S/N (signal-to-noise)—The relative power levels of a signal and noise on a communication line, expressed in decibels.

SPC (stored program control)—A method of controlling the functions and features of a switching system by computer. The computer is controlled by a fixed software program which defines the capabilities and operation of the switching system.

SRC (spiral redundancy checking)—A validity checking technique for transmission blocks where the redundant information sent with the block for receiver checking is accumulated in a spiral bit position fashion.

SRCTS—Special reverse charge toll service.

Station apparatus—The telephone equipment that terminates the voice channels at the subscribers location. Telephone sets, call directors, multi-button phones, repertory dialers and key systems are examples of station apparatus.

Step dialing—When a called station is found busy, step dialing permits a single additional digit to be dialed to seek out another station within the called group.

Store and forward—A data communication technique that accepts messages or transactions, stores them until they are validated and complete and then forwards them to the next location as addressed in the message or transaction header.

Streaming—A modem's condition when it is sending a carrier signal on a multidrop communication line and hasn't been polled.

Subset—The subscribers telephone set.

Super group—The assembly of five 12-channel groups, for simultaneous modulation and demodulation, occupying adjacent bands in the spectrum. Can be used as 60 voice-grade or wide-band channels or combinations of both.

Switching register—See register.

SXS—Step by step (switching system).

SYN (SYNC)—A bit or character used to synchronize a time frame in a time division multiplexer. Also, a sequence used by synchronous modems to perform bit synchronization and by the line controller for character synchronization.

Synchronous modem—A line termination unit that uses a derived clocking signal to perform bit synchronization with incoming data.

T1 carrier—A PCM system operating at a 1.544MHz rate carrying 24 individual VF channels.

Tandem trunk—See trunk.

TAT—Transatlantic Telephone (underseas cables 1 through 6).

TASI—Time assignment speech interpolation.

TDM (time division multiplexing)—A data communication technique for combining several lower speed channels into one facility or transmission path at a higher speed in which each low-speed channel is allotted a specific position or time slot in the signal stream based upon time. Thus, the information on the low-speed input channels is interleaved at higher speed on the multiplexed channel. At the receiver, the signals are separated to reconstruct the individual low-speed channels.

Telemetry—Transmission and collection of data obtained by sensing conditions in a real-time environment.

Tenant service—Permits one PABX system to serve more than one organization. Each tenant (i.e., co-user) can be provided his own trunk lines, attendants, consoles, internal switching links, etc.

Text—The part of a message or transaction between the control information of the header and that of the trace section or tail that constitutes the information to be processed or delivered to the addressed location.

Thermal noise—A type of electromagnetic noise produced in conductors or in electronic circuitry that is proportional to temperature. (See Gaussian noise.)

Three-way calling—Permits the setting up of a conference call between the user's station and 2 outside parties.

Time sharing—A processing technique that permits multiple users to share resources simultaneously.

Time slot—A specific position in a multiplexed data stream. The bits in this position are those of one channel of information.

Toll center—A Class 4 telephone switching office up one level from the end or service office, named for the call billing apparatus found there.

Toll ticketing—A method of providing printout of all toll calls by station. More complex systems provide full billing information, time, and charges.

Tone dialing—Referred to as Dual Tone, Multi-Frequency (DTMF) dialing or calling. Tone systems are more rapid than rotary dial mechanisms. When used within a PABX/PBX system, the tone can require translation to emulate rotary dial pulses for trunk or WATS calls if the local CO is not prepared to accept tone codes.

T/P (transaction processing)—A processing technique using on-line control programs and a remote terminal network so that inquiries and applications against a data base can be performed at any processing site where the data is stored. Routing is performed based on the content of the message that also contains the information to be processed.

T&R (tip and ring)—The two conductors of the cable pair used to carry audio and signaling information to and from the central office and the subscriber.

Transmitter—The carbon device in the telephone handset used to convert speech to electrical energy, or the device that enters the signal into the transmission medium, such as a microwave transmitter or fiber optic transmitter.

Trunk—A telephone circuit or channel between two central offices or switching equipment.

Attendant: Used to permit a PABX/PBX station to call the attendant to call a station. Sometimes referred to an "intercom trunk" or "attendant's line." In some arrangements, internal calls to the attendant cannot be internally extended; that is, they cannot be passed on to another inside station. They may, however, be extendable to an outside (CO) trunk line.

Information: When provided with call completion features, the information trunk(s) can be used to permit the attendant to extend an internally originated call to another internal station or to a central office trunk.

Tandem: Service in which incoming trunks are fed into outgoing trunks.

Tie: Used for interconnecting 2 PABX systems with access through specific code digits or through the assistance of the attendant.

TSAC (time slot assigner circuit)—A circuit that determines when a CODEC will put its 8 bits of data on the PCM bit stream. To multiplex 24 or 30 channels together requires each channel to have a time slot assigned. This is assigned permanently by hardware or dynamically by software instructions to the TSAC. A complex circuit, the TSAC has been reduced to a single integrated circuit in some systems.

Turnaround time—The time required for a modem to reverse the direction of transmission on a half-duplex line.

Twist—The amplitude ratio of a pair of DTMF tones. Because of transmission and equipment variations, a pair of tones that originated equal in amplitude may arrive with a considerable difference in amplitude.

Uncontrolled terminal—A user terminal that is on line all the time and does not contain line control logic for polling and calling.

USOC—Uniform service offering code.

VCA—Voice coupling arrangement.

VF (voice frequency)—Describes a telephone channel designed to carry the human voice or data in the 300 to 3000Hz range (approximately).

V&H—Vertical & horizontal. Coordinate system used in computing mileage between any two points for tariff applications.

VRC (vertical redundancy checking)—A method of character parity checking.

WECO—Western Electric Company.

Weighting filters—Different filters are used to represent the transmission passband characteristics of different communication networks. The two most frequently used are C-message and psophometric weighting filters. C-message weighting is used as a standard in North America while psophometric weighting is often used in Europe.

White noise—See Gaussian noise and thermal noise.

Wide band—Implies data speeds requiring the equivalent of more than one VF channel for operation; broadband.

AMERICAN MICROSYSTEMS, INC.

Section 18.0

Other AMI Standard Products

- Memory
- Microprocessor
- Microcomputer
- Microprocessor Peripherals
- Remote Control Circuits
- Organ Circuits
- Clock Circuits
- Display Drivers
- Scale Circuits
- Uncommitted Logic Arrays

Memory Products

STATIC MOS RANDOM ACCESS MEMORIES

Part No.	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S68B10	128×8	NMOS	250	420	N/A	+5V	24 Pin
S68A10	128×8	NMOS	360	420	N/A	+5V	24 Pin
S6810	128×8	NMOS	450	400	N/A	+5V	24 Pin
S6810-1	128×8	NMOS	575	500	N/A	+5V	24 Pin

STATIC CMOS RANDOM ACCESS MEMORIES

Part No.	Organization	Max. Access Time(ns)	Max. Active Power(mW)	Max. Standby Power(mW)	Power Supplies	Package
S5101L-1	256×4	450	115	.055	+5V	22 Pin
S5101L	256×4	650	115	.055	+5V	22 Pin
S5101L-3	256×4	650	115	.735	+5V	22 Pin
S5101-8	256×4	800	115	2.7	+5V	22 Pin
S6501L-1	256×4	450	115	.055	+5V	22 Pin
S6501L	256×4	650	115	.055	+5V	22 Pin
S6501L-3	256×4	650	115	.735	+5V	22 Pin
S6501-8	256×4	800	115	2.7	+5V	22 Pin
S6504[2]	4096×1	300	75	0.5	+5V	18 Pin
S6508-1	1024×1	300	13	.055	+5V	16 Pin
S6508	1024×1	460	13	.55	+5V	16 Pin
S6508A	1024×1	460/185[2]	12.5/50[2]	1.1	+4V to +11V	16 Pin
S6514[2]	1024×4	300	75	0.25	+5V	18 Pin
S6516[2]	2048×8	230	55MHz	5.5	+5V	24 Pin

MOS READ ONLY MEMORIES

Part No.	Description	Organization	Process	Max. Access Time(ns)	Max. Active Power(mW)	Power Supplies	Package
S6831B	16,384 Bit Static ROM	2048×8	NMOS	450	370	+5	24 Pin
S68A316	16,384 Bit Static ROM	2048×8	NMOS	350	370	+5	24 Pin
S68332	32,768 Bit Static ROM	4096×8	NMOS	450	370	+5	24 Pin
S68A332	32,768 Bit Static ROM	4096×8	NMOS	350	370	+5	24 Pin
S2333	32,768 Bit Static ROM	4096×8	NMOS	350	385	+5	24 Pin
S68A364	65,536 Bit Static ROM	8192×8	NMOS	350	385	+5	24 Pin
S68B364	65,536 Bit Static ROM	8192×8	NMOS	250	495	+5	24 Pin
S4264	65,536 Bit Static ROM	8192×8	NMOS	300	440	+5	24 Pin
S2364	65,536 Bit Static ROM	8192×8	NMOS	350	385	+5	28 Pin
S23128[2]	131,072 Bit Static ROM	16,384×8	NMOS	250	385	+5	28 Pin

[1] Not recommended for new designs

[2] To be announced

Microprocessor Products

The AMI S6800 Microcomputer Systems Family

MICROPROCESSORS

S6800/S68A00/S68B00	8-Bit Microprocessor (1.0/1.5/2.0MHz XTAL)
S68H00	High Speed S6800 (2MHz Clock)
S6801/S6801E	Single Chip Microcomputer 2K ROM, 128×8 RAM, 31 I/O Lines, Enhanced Instruction Set (External [E] or Internal Clock)
S6802/S68A02	Microprocessor with Clock and RAM (1.0/1.5MHz Clock)
S6803/S6803N/R	S6801 Without ROM (N/R Model — No ROM and/or RAM)
S6805	Single Chip Microcomputer 1,152×8 ROM, 64×8 RAM, Clock, Pre-scaler, Bit Level Instructions.
S6808/S68A08	S6800 with Clock (1.0/1.5MHz Clock)
S6809(E)/S68A09(E)/S68B09(E)	Pseudo 16-Bit Microprocessor (1.0/1.5/2.0MHz Clock) (E Models — External Clock Mode)

PERIPHERALS

S1602	Universal Asynchronous Receiver/Transmitter (UART)
S2350	Universal Synchronous Receiver/Transmitter (USRT)
S6821/S68A21/S68B21	Peripheral Interface Adapter (PIA)(1.0/1.5/2.0MHz Clock)
S68H21	High Speed Peripheral Interface Adapter (PIA) (2.5MHz Clock)
S6840/S68A40/S68B40	Programmable Timer (1.0/1.5/2.0MHz)
S68045	CRT Controller (CRTC)
S6846	2K ROM, Parallel I/O, Programmable Timer
S68047	Video Display Generator (VDG)
S6850/S68A50/S68B50	Asynchronous Communication Interface Adapter 800 Bus Compatible
S6852/S68A52/S68B52	Asynchronous Communication Interface (1.0/1.5/2.0MHz Clock) (ACIA)
S6854/S68A54/S68B54	Advanced Data Link Controller (ADLC) (1.0/1.5/2.0MHz Clock)
S68488	IEEE — 488 Bus Interface
S6894	Data Encryption Unit (DEU)

MEMORIES

S6810/S68A10/S68B10	128×8 Static RAM (450/360/250ns Access Time)
S6810-1	Low Cost S6810 (575ns Access Time)

THE AMI S9900 MICROCOMPUTER SYSTEMS FAMILY

MICROPROCESSORS

S9900	16-Bit Microprocessor
S9980A/S9981	16-Bit Microprocessor 8-Bit Data Bus (S9981 has Internal Clock)

PERIPHERALS

S9901	Programmable Systems Interface (PSI)
S9902	UART/Asynchronous Communications Controller (USRT/ACC)

Consumer and Interface Products

REMOTE CONTROL CIRCUITS

Part No.	Description	Process	Power Supply	Commands	Packages
S2600	Remote Control Encoder	CMOS	+7V to 10V	31	16 Pin
S2601	Remote Control Decoder	PMOS	+10V to 18V	31	22 Pin
S2602	Remote Control Encoder	CMOS	+9V	18	16 Pin
S2603	Remote Control Decoder	PMOS	+9V	18	22 Pin
S2742	Remote Control Decoder	PMOS	+15V	512	18 Pin
S2743	Remote Control Encoder	PMOS	+9V	512	16 Pin
S2747	Remote Control Encoder	CMOS	+9V	512	16 Pin
S2748	Remote Control Decoder	CMOS	+12V	512	16 Pin

ORGAN CIRCUITS

Part No.	Description	Process	Packages
S10110	Analog Shift Register	PMOS	8 Pin
S10129	Six-Stage Frequency Divider	PMOS	14 Pin
S10130	Six-Stage Frequency Divider	PMOS	14 Pin
S10131	Six-Stage Frequency Divider	PMOS	14 Pin
S10430	Divider-Keyer	PMOS	40 Pin
S2567	Rhythm Counter	PMOS	16 Pin
S2688	Noise Generator	PMOS	8 Pin
S50240	Top Octave Synthesizer	PMOS	16 Pin
S50241	Top Octave Synthesizer	PMOS	16 Pin
S50242	Top Octave Synthesizer	PMOS	16 Pin
S50243	Top Octave Synthesizer	PMOS	16 Pin
S50244	Top Octave Synthesizer	PMOS	16 Pin
S50245	Top Octave Synthesizer	PMOS	16 Pin

CLOCK CIRCUITS

Part No.	Description	Process	Power Supply	Digits	Packages
S2709	Fluorescent Automotive Digital Clock (12 Hour)	PMOS	+12V	4	22 Pin
S4003	Fluorescent Automotive Digital Clock (12 Hour+Date+Rally Timer)	PMOS	+12V	4	40 Pin

DRIVERS

Part No.	Description	Process	Power Supply	Outputs	Packages
S2809	Universal Driver	PMOS	+8V to +22V	32	40 Pin
S4535	32 Bit, High Voltage, Driver	CMOS	+5V	32	40 Pin
S4534	10 Bit, High Voltage, Driver	CMOS	+5V	10	18 Pin
S4521	32 Bit Driver	CMOS	+5V	32	40 Pin

A/D CONVERTER AND DIGITAL SCALE CIRCUIT

Part No.	Description	Process	Power Supply	Digits	Packages
S4036	General Purpose A/D Converter and Digital Scale Circuit	CMOS	+9V	4	24 Pin

UNCOMMITTED LOGIC ARRAYS

Features

- ☐ Arrays of Uncommitted CMOS Transistors Programmed by Metal Layer Interconnect to Implement Arbitrary Digital Logic Functions
- ☐ Multiple Developmental Interfaces: AMI or Customer Designed
- ☐ Six Array Configurations—From 300 to 1260 Gates
- ☐ Quick Turn Prototypes and Short Production Turn-On Time
- ☐ Economical Semi-Custom Approach for Low-to-Medium Production Volume Requirements
- ☐ Advanced Oxide-Isolated Silicon Gate CMOS Technology
- ☐ High Performance—5 to 10 ns Typical Gate Delay
- ☐ Broad Power Supply Range—3V to 10V (±10%)
- ☐ TTL or CMOS Compatible I/O
- ☐ Up to 76 I/O Connections
- ☐ Numerous Package Options
- ☐ Full Military Temperature Range (−55°C to 125°C) and MIL-STD-883 Class B Screening Available

General Description

AMI's Uncommitted Logic Array (ULA) products consist of arrays of CMOS devices whose interconnections are initially unspecified. By "programming" interconnect at the metal layer mask level, virtually arbitrary configurations of digital logic can be realized in an LSI implementation.

AMI ULA designs are based on topological cells—i.e., groups of uncommitted silicon-gate N-channel and P-channel transistors—that are placed at regular intervals along the X and Y axes of the chip with intervening polysilicon underpasses. Pads, input protection circuitry, and uncommitted output drivers are placed around the periphery.

A family of CMOS ULA products is offered in six configurations, summarized in Table l, with circuit complexities equivalent to 300, 400, 540, 770, 1000, and 1260 two-input gates, respectively. All pads (except the two preassigned power supply connections) can be individually configured as inputs, outputs, or I/O's. Input switching characteristics can be programmed for either CMOS or TTL compatibility. LS buffer output drivers will support CMOS levels or two low power schottky TTL loads. TTL buffer outputs will also provide CMOS levels and are capable of driving up to six LS TTL loads. All output drivers can be programmed for tri-state or open drain (open collector) operation as required. One input-only pad is also provided.

Table 1

Circuit	Equivalent Two-Input Gates	Pads	LS Output Drivers	TTL Output Drivers	Input Only
UA-1	300	40	17	20	1
UA-2	400	46	23	20	1
UA-3	540	52	25	24	1
UA-4	770	62	31	28	1
UA-5	1000	70	35	32	1
UA-6	1260	78	39	36	1

Pinout or lead count varies with die size and array complexity as shown in Table 1. The arrays are offered in standard plastic and ceramic dual-in-line packages with pin counts ranging from 16 to 64, and in JEDEC-Standard leadless chip carriers. AMI ULA products are also available in wafer or unpackaged die form.

The CMOS technology used for these products is AMI's state-of-the-art 5-micron, oxide-isolated, silicon gate CMOS process. This process offers all the conventional advantages of CMOS—i.e., very low power consumption, broad power supply voltage range (3V to 10V ±10%), and high noise immunity—as well as dense circuits with high performance. Gate propagation delays are in the five to ten ns range for 5 volt operation at room temperature. AMI ULA products can be supplied in versions intended for operation over the standard commercial temperature range (0°C to +70°C), the industrial range (−40°C to +85°C), or the full military range (−55°C to +125°C). MIL-STD-883 Class B screening, including internal visual inspection and high temperature burn-in, is offered. Similarly, customer-specified high reliability screening is available for commercial and industrial applications.

Compared to SSI/MSI logic implementations, AMI's ULA approach offers lower system cost and, in addition, all the benefits of CMOS LSI. The lower system cost is due to significant reductions in component count, board area and power consumption. Product reliability, a strong function of component count, is thereby greatly enhanced. And compared to fully custom LSI circuits, the ULA offers several advantages: low development cost; shorter development time; shorter production turn-on time; and low unit costs for small to moderate production volumes.

In conjunction with these arrays, AMI has developed a set of "functional overlays." These are basic logic element building blocks—e.g. two input and larger gates of various types, flip-flops, and so forth—from which complete logic designs can be developed. Each functional overlay corresponds to a metal interconnect pattern that is superimposed on a set of uncommitted transistors (and polysilicon underpasses) in the array to implement the logic element. Typical functional overlay logic elements and the number of two-input gate equivalents they utilize are shown in Table 2.

AMI will convert customer designed logic to metal interconnect patterns using functional overlays and its proprietary Symbolic Interactive Design System (SIDS). SIDS is a computer aided design tool for layout using on-line color graphics terminals. Interested customers should submit logic diagrams for evaluation and a quotation.

For programs involving multiple ULA patterns from customers with suitable MOS design and layout experience, AMI will also support arrangements in which the customer designs the ULA metal interconnect patterns and furnishes AMI with corresponding metal mask PG tapes to AMI specification.

Table 2

Logic Element	2-Input Gate Equivalent
2-Input NOR	1
2-Input NAND	1
3-Input NOR	1.5
3-Input NAND	1.5
INVERTER	.5
D FLIP-FLOP W/RESET	5
D FLIP-FLOP W/SET-RESET	6
J-K FLIP-FLOP	8
CLOCKED LATCH	2.5
EXCLUSIVE OR	2.5
SCHMITT TRIGGER	2
4-BIT BCD CNTR W/RESET	27
TRANSMISSION GATE	.5

DC Characteristics—TTL Interface

Specified @ $V_{DD}=+5V \pm 10\%$; $V_{SS}=0$; Temperature $=-55°C$ to $+125°C$

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	2.0		V_{DD}	V
V_{IL}	Input Low Voltage	0.0		0.8	V
V_{OH}	Output High Voltage (LS Buffer $I_{OH}=-700\mu A$) (T Buffer $I_{OH}=-1.5mA$)	2.7 2.4			V V
V_{OL}	Output Low Voltage (T Buffer $V_{OL}=2.4mA$) (LS Buffer $I_{OL}=0.8mA$)			0.4 0.4	V V
I_{OZ}	3-State Output Leakage $V_O=0$ or V_{DD}	−10	0.001	10	μA

DC Characteristics—CMOS Interface

Sym.	Parameter	V_{DD}	Limits *T Low Min	Limits *T Low Max	Limits 25°C Min	Limits 25°C Typ	Limits 25°C Max	Limits *T High Min	Limits *T High Max	Units	Condition
I_{DD}	Quiescent Device Current	5V 10V		0.1 0.2		.001 .002	0.1 0.2		1 2	μA/gate μA/gate	$V_{IN}=0$ or V_{DD}
V_{OL}	Low Level Output Voltage			0.05			0.05		0.05	V	$I_O=1\mu A$
V_{OH}	High Level Output Voltage	5V 10V	4.95 9.95		4.95 9.95			4.95 9.95		V V	$I_O=-1\mu A$
V_{IL}	Input Low Voltage	5V 10V	0.0 0.0	1.5 3.0	0.0 0.0		1.5 3.0	0.0 0.0	1.5 3.0	V V	
V_{IH}	Input High Voltage	5V 10V	3.5 7.0	5.0 10.0	3.5 7.0		5.0 10.0	3.5 7.0	5.0 10.0	V V	
I_{OL}	Output Low (Sink) Current T Buffer	5V 10V	3.2 6.0		3.2 6.0	4.8 9.0		2.4 4.0		mA mA	$V_O=0.4V$ $V_O=0.5V$
	LS Buffer	5V 10V	1.0 1.8		1.0 1.8	1.6 3.1		0.8 1.0		mA mA	$V_O=0.4V$ $V_O=0.5V$
I_{OH}	Output High (Source) Current T Buffer	5V 10V		−600 −1120			−600 −1120		−500 −940	μA μA	$V_O=4.6V$ $V_O=9.5V$
	LS Buffer	5V 10V		−300 −560			−300 −560		−250 −470	μA μA	$V_O=4.6V$ $V_O=9.5V$
I_{IN}	Input Leakage Current			1			1		1	μA	$V_{IN}=0$ or V_{DD}
I_{OZ}	3 State Output Leakage Current			±1			±1		±10	μA	$V_O=0$ or V_{DD}
C_I	Input Capacitance					5				pF	Any Input

*Military temperature range is −55°C to +125°C
Industrial temperature range is −40°C to +85°C
Commercial temperature range is 0°C to +70°C

Worldwide Sales Offices

UNITED STATES

Northwest Region

HEADQUARTERS—3800 Homestead Road, Santa Clara, California 95051 ..... (408) 246-0330, TWX: 910-338-0018
CALIFORNIA, 2960 Gordon Avenue, Santa Clara 95051 ..... (408) 738-4151
WASHINGTON, 20709 N.E. 232nd Avenue, Battle Ground 98604 ..... (206) 687-3101

Southwest Region

CALIFORNIA, 1451 Quail Street, Suite 208, Newport Beach 92660 ..... (714) 851-5931

Central Region

ILLINOIS, 500 Higgins Road, Suite 210, Elk Grove Village 60007 ..... (312) 437-6496
MICHIGAN, 29200 Vassar Avenue, Suite 221, Livonia 48152 ..... (313) 478-4220
COLORADO, 7346A So. Alton Way, Englewood 80112 ..... (303) 694-0629

Southeastern Region

FLORIDA, 139 Whooping Loop, Altamonte Springs 32701 ..... (305) 830-8889
NORTH CAROLINA, 7000 Six Forks Road, Suite 114, Raleigh 27609 .....
TEXAS, 725 South Central Expressway, Suite A-9, Richardson 75080 ..... (214) 231-5721
(214) 231-5285

Mid-Atlantic Area

PENNSYLVANIA, Axewood East, Butler & Skippack Pikes, Suite 230, Ambler 19002 ..... (215) 643-0217
INDIANA, 408 South 9th Street, Suite 201, Noblesville 46060 ..... (317) 773-6330
OHIO, 100 East Wilson Bridge Road, Suite 200, Worthington 43085 ..... (614) 436-0330

Northeastern Region

NEW YORK, 20F Robert Pitt Drive, Suite 208, Monsey 10952 ..... (914) 352-5333
MASSACHUSETTS, 24 Muzzey Street, Lexington 02173 ..... (617) 861-6530

EUROPE

ENGLAND, AMI Microsystems, Ltd., Princes House, Princes St., Swindon SN1 2HU ..... (0793) 37852
FRANCE, AMI Microsystems, S.A.R.L., 124 Avenue de Paris, 94300 Vincennes ..... (01) 374 00 90
WEST GERMANY, AMI Microsystems GmbH, Rosenheimer Strasse 30/32, 8000 Munich 80 ..... (089) 483081
AUSTRIA, Austrian Microsystems International GmbH, Floragasse 7, 1040 Vienna ..... (222) 65 47 11
ITALY, AMI Microsystems, S.p.A., Piazza Gobetti 12, Milano 20131 ..... (02) 293745
JAPAN, AMI Japan Ltd., 502 Nikko Sanno Building 2-5-3, Akasaka, Minato-ku, Tokyo 107 ..... (813) 586-8131

Domestic Representatives

ALABAMA, Huntsville	Rep, Inc.	(205) 881-9270
CALIFORNIA, Los Angeles	Ed Landa Co.	(213) 879-0770
CALIFORNIA, San Diego	Hadden Associates	(714) 565-9445
CANADA, Ottowa, Ontario	Vitel Electronics	(613) 596-0400
CANADA, Rexdale, Ontario	Vitel Electronics	(416) 245-8528
CANADA, Quebec, Quebec	Vitel Electronics	(514) 331-7393
CANADA, Vancouver, B.C.	Vitel Electronics	(604) 438-6121
GEORGIA, Tucker	Rep, Inc.	(404) 938-4358
ILLINOIS, Elk Grove Village	Oasis Sales	(312) 640-1850
IOWA, Cedar Rapids	Comstrand, Inc.	(319) 377-1575
KANSAS, Overland Park	Kepco, Inc.	(913) 649-1051
MINNESOTA, Minneapolis	Comstrand, Inc.	(612) 788-9234
MISSOURI, Maryland Heights	Kepco, Inc.	(314) 576-4111
NEW HAMPSHIRE, Nashua	Enjay Electronics	(603) 883-9380
NEW YORK, Clinton	Advanced Components	(315) 853-6438
NEW YORK, Endicott	Advanced Components	(607) 785-3191
NEW YORK, North Syracuse	Advanced Components	(315) 699-2671
NEW YORK, Rochester	Advanced Components	(716) 554-7017
NEW YORK, Scottsville	Advanced Components	(716) 889-1429
NEW YORK, W. Babylon	Astrorep	(516) 422-2500 (201) 624-4408 (203) 324-4208
NORTH CAROLINA, Raleigh	Rep, Inc.	(919) 851-3007
OHIO, Cincinnati	Giesting & Associates	(513) 521-8800
OHIO, Dayton	Giesting & Associates	(513) 293-4044
OHIO, Galion	Giesting & Associates	(419) 468-3737
OKLAHOMA, Oklahoma City	Ammon & Rizos	(405) 942-2552
PENNSYLVANIA, Hopwood	Giesting & Associates	(412) 433-2336
TEXAS, Austin	Ammon & Rizos	(901) 874-1369
TEXAS, Dallas	Ammon & Rizos	(214) 233-5591
TEXAS, Houston	Ammon & Rizos	(713) 781-6240
TENNESSEE, Jefferson City	Rep, Inc.	(615) 475-4105
WASHINGTON, Bellevue	SD-R^2 Products & Sales	(206) 747-9424 (206) 624-2621
WISCONSIN, Brookfield	Oasis Sales	(414) 782-6660

Domestic Distributors

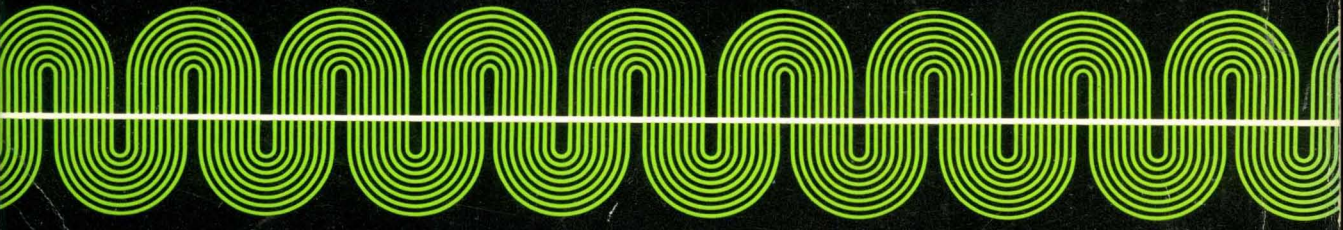
ARIZONA, Phoenix	Kierulff Electronics	(602) 243-4101
ARIZONA, Tucson	Kierulff Electronics	(602) 624-9986
CALIFORNIA, Canoga Park	Schweber Electronics	(213) 999-4702
CALIFORNIA, Cupertino	Western Microtechnology	(408) 725-1660
CALIFORNIA, Irvine	Schweber Electronics	(714) 556-3880
CALIFORNIA, Los Angeles	Kierulff Electronics	(213) 725-0325
CALIFORNIA, Palo Alto	Kierulff Electronics	(415) 968-6292
CALIFORNIA, San Diego	Anthem Electronics	(714) 279-5200
CALIFORNIA, San Diego	Arrow Electronics	(714) 565-4800
CALIFORNIA, San Diego	Kierulff Electronics	(714) 278-2112
CALIFORNIA, San Jose	Anthem Electronics	(408) 946-8000
CALIFORNIA, Santa Clara	Schweber Electronics	(408) 496-0200
CALIFORNIA, Sunnyvale	Arrow Electronics	(408) 745-6600
CALIFORNIA, Tustin	Anthem Electronics	(213) 582-2122
CALIFORNIA, Tustin	Kierulff Electronics	(714) 731-5711
CANADA, British Columbia, Vancouver	Future Electronics, Inc.	(604) 438-5545
CANADA, Ontario, Downsview	Cesco Electronics, Ltd.	(416) 661-0220
CANADA, Ontario, Downsview	Future Electronics, Inc.	(416) 663-5563

Domestic Distributors (continued)

CANADA, Ottawa	Future Electronics, Inc.	(613) 820-8313
CANADA, Quebec, Montreal	Cesco Electronics, Ltd.	(514) 735-5511
CANADA, Quebec, Montreal	Future Electronics, Inc.	(514) 731-7441
CANADA, Quebec	Cesco Electronics, Ltd.	(418) 687-4231
COLORADO, Denver	Arrow Electronics	(303) 758-2100
COLORADO, Denver	Kierulff Electronics	(303) 371-6500
COLORADO, Wheatridge	Bell Electronics	(303) 424-1985
CONNECTICUT, Danbury	Schweber Electronics	(203) 792-3500
CONNECTICUT, Wallingford	Arrow Electronics	(203) 265-7741
FLORIDA, Ft. Lauderdale	Arrow Electronics	(305) 776-7790
FLORIDA, Hollywood	Schweber Electronics	(305) 927-0511
FLORIDA, Palm Bay	Arrow Electronics	(305) 725-1480
FLORIDA, St. Petersburg	Kierulff Electronics	(813) 576-1966
GEORGIA, Norcross	Arrow Electronics	(404) 449-8252
GEORGIA, Norcross	Schweber Electronics	(404) 449-9170
ILLINOIS, Elk Grove Village	Kierulff Electronics	(312) 640-0200
ILLINOIS, Elk Grove Village	Schweber Electronics	(312) 364-3750
ILLINOIS, Lombard	R/M Electronics	(312) 932-5150
ILLINOIS, Schaumburg	Arrow Electronics	(312) 893-9420
INDIANA, Indianapolis	Arrow Electronics	(317) 243-9353
INDIANA, Indianapolis	R/M Electronics	(317) 247-9701
MARYLAND, Baltimore	Arrow Electronics	(301) 247-5200
MARYLAND, Gaithersburg	Schweber Electronics	(301) 840-5900
MASSACHUSETTS, Bedford	Schweber Electronics	(617) 275-5100
MASSACHUSETTS, Billerica	Kierulff Electronics	(617) 667-8331
MASSACHUSETTS, Woburn	Arrow Electronics	(617) 933-8130
MICHIGAN, Ann Arbor	Arrow Electronics	(313) 971-8220
MICHIGAN, Livonia	Schweber Electronics	(313) 525-8100
MICHIGAN, Wyoming	R/M Electronics	(616) 531-9300
MINNESOTA, Eden Prairie	Schweber Electronics	(612) 941-5280
MINNESOTA, Edina	Arrow Electronics	(612) 830-1800
MISSOURI, St. Louis	Arrow Electronics	(314) 567-6888
NEW HAMPSHIRE, Manchester	Arrow Electronics	(603) 668-6968
NEW JERSEY, Fairfield	Schweber Electronics	(201) 227-7880
NEW JERSEY, Moorestown	Arrow Electronics	(215) 928-1800
NEW JERSEY, Saddlebrook	Arrow Electronics	(201) 797-5800
NEW MEXICO, Albuquerque	Arrow Electronics	(505) 243-4566
NEW MEXICO, Albuquerque	Bell Electronics	(505) 292-2700
NEW YORK, Farmingdale	Arrow Electronics	(516) 694-6800
NEW YORK, Hauppauge	Arrow Electronics	(516) 231-1000
NEW YORK, Liverpool	Arrow Electronics	(315) 652-1000
NEW YORK, Rochester	Schweber Electronics	(716) 424-2222
NEW YORK, Westbury	Schweber Electronics	(516) 334-7474
NORTH CAROLINA, Winston Salem	Arrow Electronics	(919) 725-8711
OHIO, Beechwood	Schweber Electronics	(216) 464-2970
OHIO, Centerville	Arrow Electronics	(513) 435-5563
OHIO, Solon	Arrow Electronics	(216) 248-3990
OREGON, Portland	Kierulff Electronics	(503) 641-9150
PENNSYLVANIA, Monroeville	Arrow Electronics	(412) 856-7000
TEXAS, Dallas	Arrow Electronics	(214) 386-7500
TEXAS, Dallas	R.M. Electronics	(214) 263-8361
TEXAS, Dallas	Schweber Electronics	(214) 661-5010
TEXAS, Houston	Schweber Electronics	(713) 784-3600
TEXAS, Stafford	Arrow Electronics	(713) 491-4100
UTAH, Salt Lake City	Bell Electronics	(801) 972-6969
UTAH, Salt Lake City	Kierulff Electronics	(801) 973-6913
WASHINGTON, Bellevue	Arrow Electronics	(206) 643-4800
WASHINGTON, Tukwila	Kierulff Electronics	(206) 575-4420
WISCONSIN, Oak Creek	Arrow Electronics	(414) 764-6600
WISCONSIN, Waukesha	Kierulff Electronics	(414) 784-8160

International Representatives and Distributors

ARGENTINA, Buenos Aires	YEL S.R.L.	46 2211
AUSTRALIA, New South Wales	Crosshouse	
AUSTRALIA, Preston, Victoria	Rifa Pty. Ltd.	(03) 480 1211
BELGIUM, Brussels	Betea Automation	(02) 7368050
BRAZIL, Sao Paulo	Datatronix Electronica Ltda.	11-826-0111
CHILI	Victronics Ltda.	36440-30237
DENMARK, Clostrup	Ditz Schweitzer A/S	(02) 453044
ENGLAND, Derby	Quarndon Electronics Ltd.	(0332) 32651
ENGLAND, West Drayton Mtddx	Semiconductor Specialists	(08954) 46415/7
ENGLAND, Greater Manchester	Vako Electronics Ltd.	(061) 652-6316
ENGLAND, Harlow, Essex	VSI Electronics (UK) Ltd.	(0279) 2935477
FINLAND, Espoo	OY Atomica AB	(080) 423533
FRANCE, Montrouge	Produits Electronique	(01) 7353320
FRANCE, Sevres	Tekelec Airtronic	(01) 534-75-35
HONG KONG, Kowloon	Electrocon Products Ltd.	3-687214-6
INDIA	Semiconductor Complex Ltd.	87495
ITALY, Milano	Mesa SpA	(02) 434333
ITALY, Roma	C.I.D. s.r.l.	(06) 63-83979
JAPAN, Osaka	Matsushita Elec. Trading Co.	(06) 204-5510
JAPAN, Tokyo	Logic House, Inc.	
JAPAN, Tokyo	Taiyo Electric Co.	(03) 379-2926
MEXICO	Dicopel S.A.	(905) 543-1984 (905) 687-1800
NETHERLANDS, Rotterdam	DMA Holdings, BV	010-361188
NEW ZEALAND, Auckland	David P. Reid (NZ) Ltd.	492-189
NORWAY, Oslo	Sevrre Hoyeh A/S	(02) 413755
SINGAPORE, Singapore	Dynamar Int'l. Ltd.	235-1139
SOUTH AFRICA, Transvaal	Radiokom Pty, Ltd.	(011) 485712
SOUTH KOREA, Seoul	Kortronics Enterprise	Seoul-634-5497
SPAIN, Barcelona	Interface S.A.	(03) 3017851
SWEDEN, Spanga	A.B. Rifa	(08) 7522500
SWITZERLAND, Zurich	W. Moor AG	(01) 8406644
TAIWAN, Taipai	Promotor Co., Ltd.	(02) 536-4057
WEST GERMANY, Nettetal	Onmi-Ray GmbH	(02153) 7961
WEST GERMANY, Viersen	Mostron Halbleitervertriebs	(0216) 17024
YUGOSLAVIA, Ljubljana	Iskra Standard/Iskra IEZE	(051) 551-353



AMI
American Microsystems, Inc.
A Subsidiary of Gould Inc.

3800 Homestead Road
Santa Clara, CA 95051

Telecom Marketing and Applications
Telephone [01] (408) 554-2070