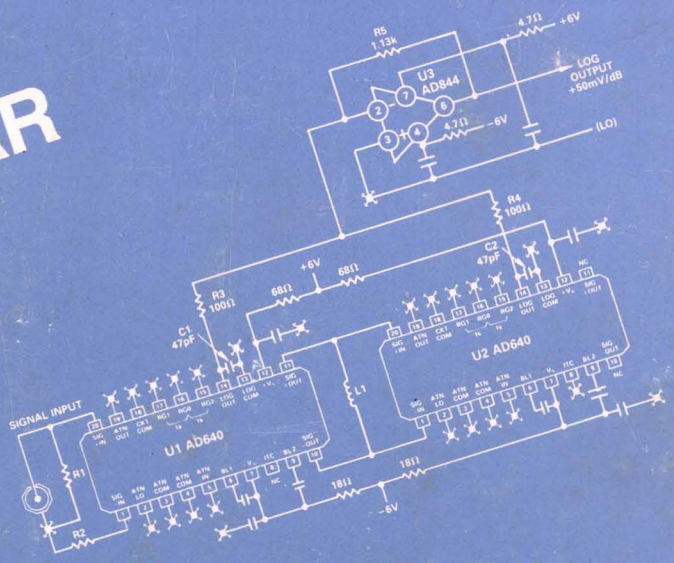
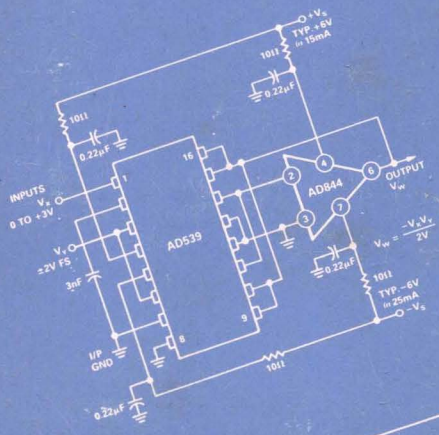
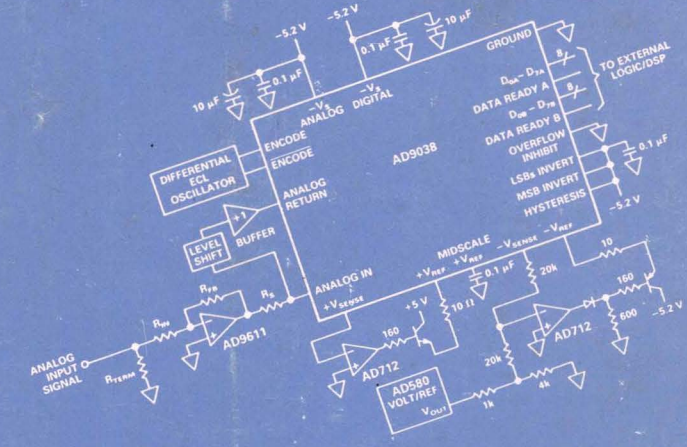
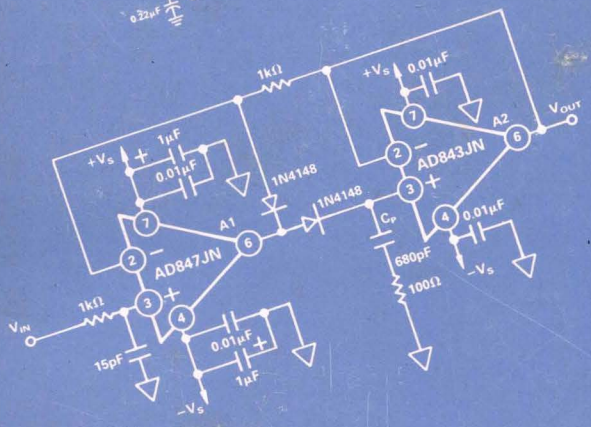
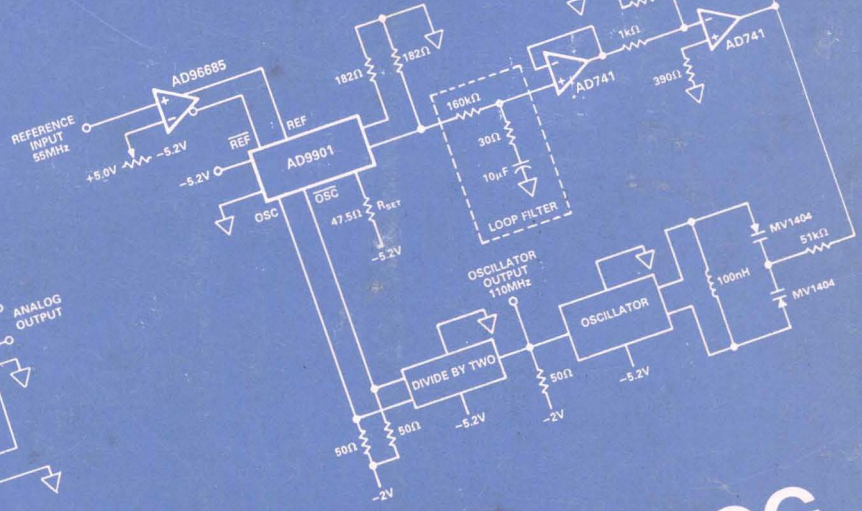
HIGH SPEED DESIGN SEMINAR

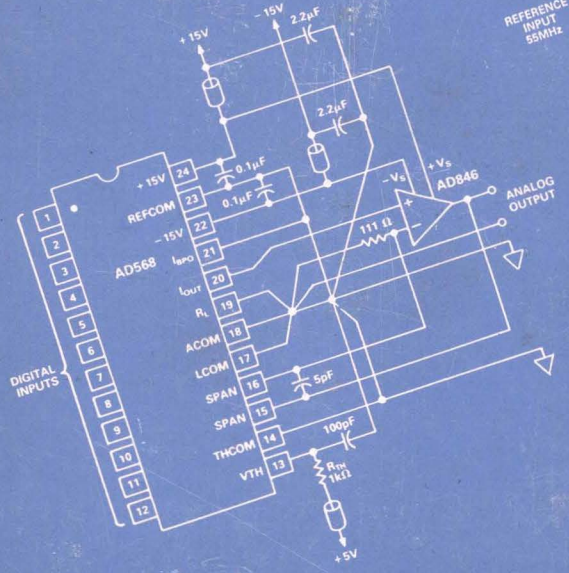












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ACKNOWLEDGEMENTS

Thanks are due to the technical staff members of Analog Devices in Engineering and Marketing who provided invaluable inputs during the preparation of this seminar. A special note of thanks goes to Linda Grimes Brandon of Brandon's WordService for layout, typesetting, and preparation of most of the illustrations.

DEDICATION

This seminar is respectfully dedicated to the memory of the late Edward L. Graves, whose long range vision and insights regarding future trends in high-speed data acquisition technology have stood the test of time.

Walt Kester
Greensboro, NC
1990

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Flash, Successive Approximation, Subranging, Digitally Corrected Subranging

A/D Converter Applications:
Undersampling (Super-Nyquist), Oversampling, Dithering, Multiplexing

A/D Converter Dynamic Specifications and Testing:
DSP Testing, Quantization Theory, DFTs and FFTs, Signal to Noise Ratio, Effective Bits, Harmonic Distortion, Two-Tone Intermodulation Distortion, Spurious Free Dynamic Range, Coherent Sampling, Non-Coherent Sampling, Windowing, Sinewave Curve Fit, Beat Frequency Tests, Histogram Tests, Noise Power Ratio, Transient Response, Overvoltage Recovery, Aperture Time, Composite Video Tests, Error Rates

References

Technical Article:
Multistage Error Correcting A/D Converters

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REFERENCES

TECHNICAL ARTICLE

Multistage Error Correcting A/D Converters

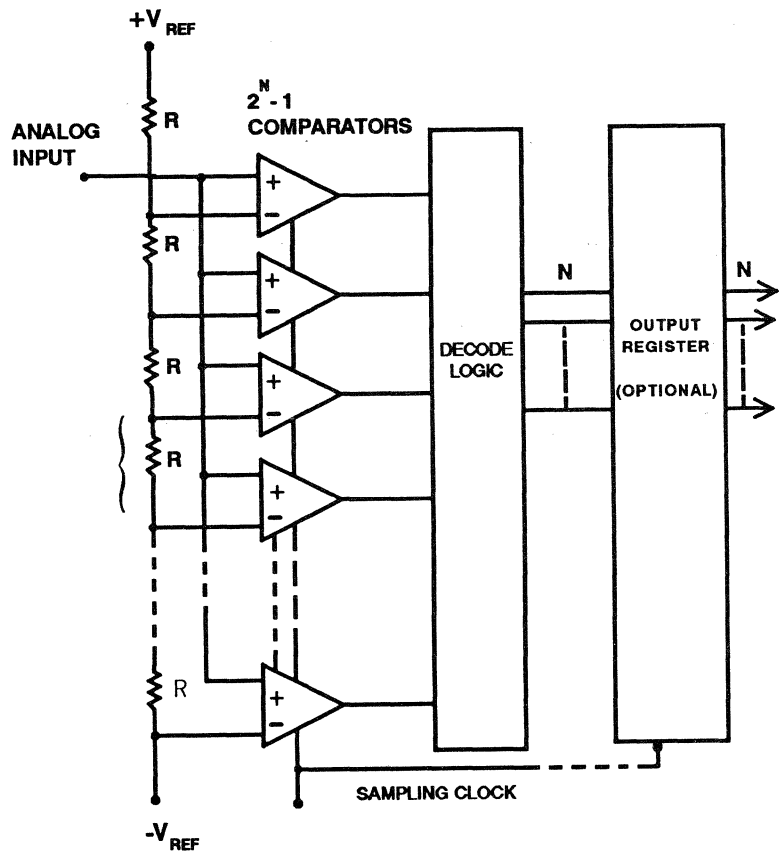
HIGH SPEED A/D CONVERTER ARCHITECTURES

- Flash
- Successive Approximation
- Subranging
- Digitally Corrected Subranging

FLASH CONVERTERS - Basic Operation

Recent advances in VLSI process technology and design techniques have made 4-10 bit flash A/D converters practical. This type of converter is characterized by high sampling rates and the ability to convert fast video input signals, usually without requiring a separate track-and-hold amplifier. The latter characteristic is limited, however, as we will discuss later.

A block diagram of a typical flash converter is shown in Figure 1.1. The analog input signal to be digitized is applied simultaneously to 2^N-1 latched comparators, where N is the number of bits. The reference voltage input for each comparator is derived from a resistive voltage divider. The reference voltage for each comparator is one least significant bit (LSB) higher than the comparator immediately below it.



N-BIT FLASH CONVERTER

Figure 1.1

When an analog signal is present at the input of the comparator bank, all comparators which have a reference voltage below the level of the input signal will assume a logic "1" output. The comparators which have their reference voltage above the input signal will assume a logic "0" output. The result is often referred to as a "thermometer code" and is applied to a stage of decoding logic (See Figure 1.2). This decoding can be accomplished in a variety of ways (such as a simple priority encoder) and ultimately results in a binary digital output. The binary output of the decoding logic often drives an on-chip output latch.

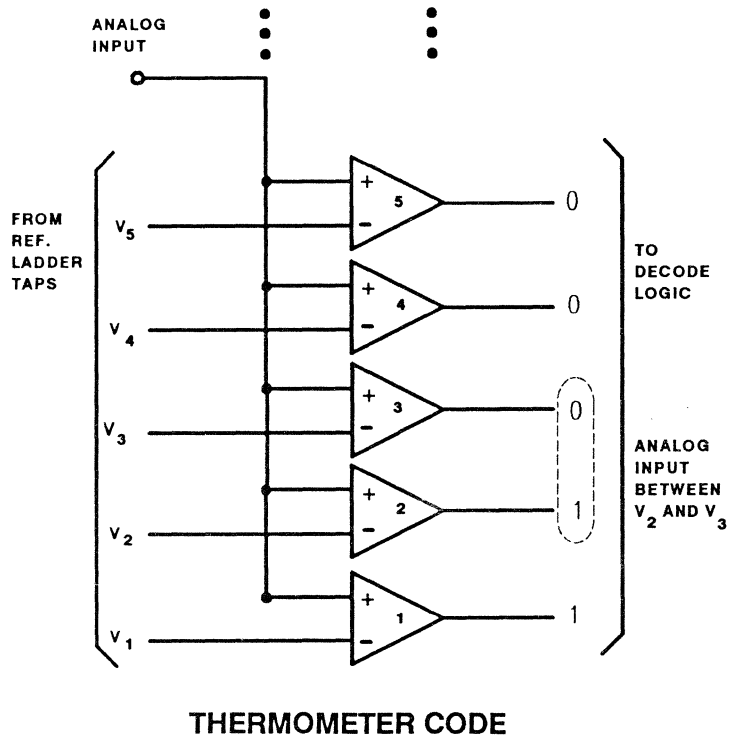
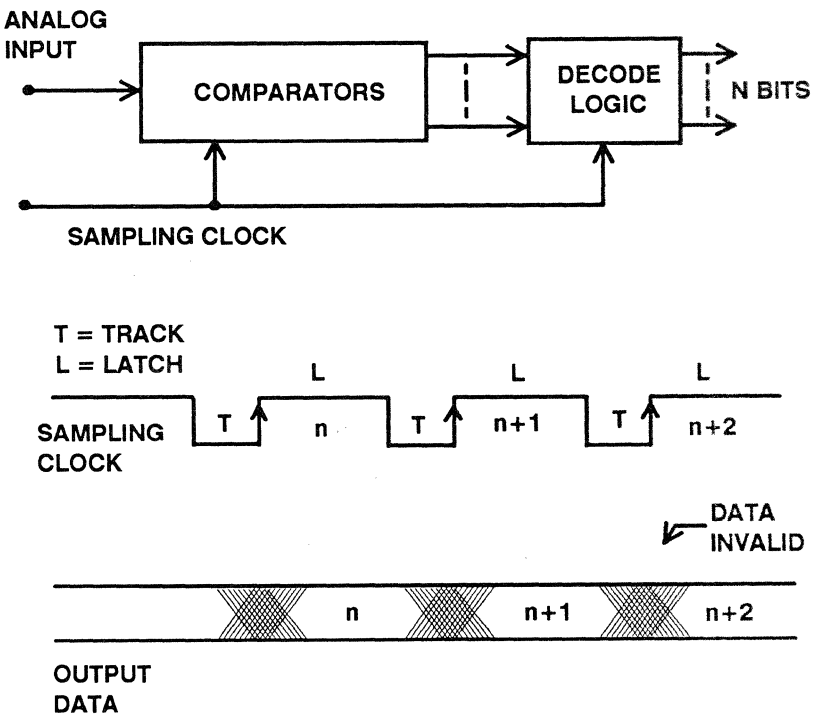


Figure 1.2

Flash Converters - Timing Considerations

The comparator bank in a flash converter has two states. In the first state (controlled by the sampling clock), the comparators essentially "track" the analog input signal. In this state, the comparator outputs are changing, and the binary decoding logic output is invalid. When the sampling clock changes to the opposite logic level, the comparators are latched or "held", much the same as in a track-and-hold amplifier.

In a flash converter which has no output data latch (such as the AD-9688 or the AD-9000), the timing of the sampling clock with respect to the output binary data is shown in Figure 1.3. Note that the output data is invalid for a period roughly equal to the sampling clock pulse width. Since this pulse width must exceed some specified minimum value for proper operation of the comparators, it follows that at high sampling rates, the time during which the output data is invalid reduces the "data valid" time, thereby making it more difficult to strobe the flash converter output into an external register. For instance, if the flash converter is operated at a 100MHz sampling rate and the sampling clock is 5ns wide (50% duty cycle), the output data will be valid for only 5ns (neglecting the rise and fall time of the output binary bits).



FLASH CONVERTER TIMING
NO PIPELINE DELAY

Figure 1.3

The addition of an internal latch after the decoding logic (such as the AD-9002, AD-9012, AD-9006, and the AD-9048) results in a timing diagram such as that shown in Figure 1.4. Note that the output data is now valid for approximately the entire clock cycle, and the flash converter can be viewed as an edge-triggered device with an inherent one-cycle "pipeline" delay. The additional pipeline delay is not usually a problem in most systems applications, and the task of clocking the output data at the proper time is simplified.

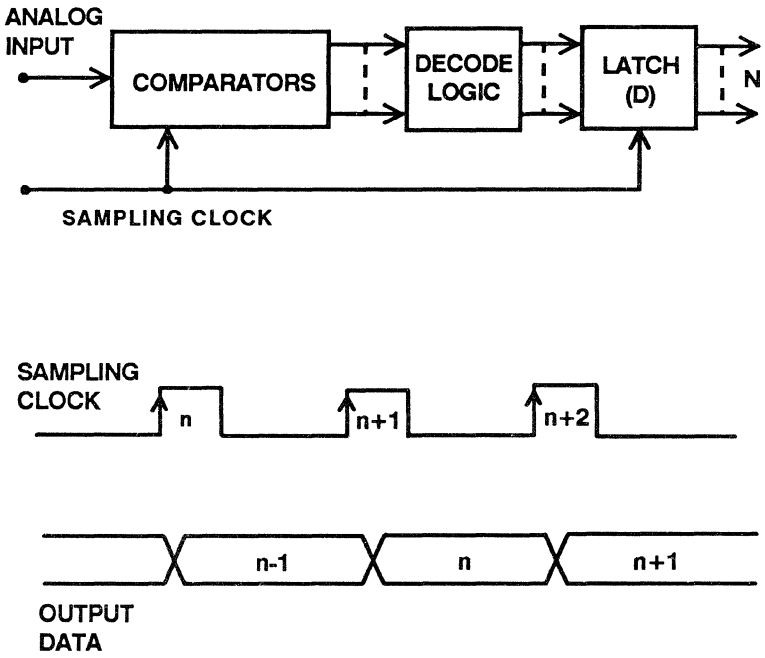


Figure 1.4

FLASH CONVERTER STATIC ERROR SOURCES

When a flash converter is digitizing a slowly changing or DC input voltage, the primary sources of integral and differential non-linearity are due to the matching of the reference ladder resistors, and the comparator input offset voltages and

currents. Although not usually specified on the data sheet, most flash converters are somewhat sensitive to the duty cycle and frequency of the encode command pulse. This problem is manifested as a shift in differential and integral non-linearity which is a function of clock duty cycle and frequency, especially when operating at or near the maximum specified sampling rate for the particular flash converter under consideration.

Another source of static flash converter errors, sometimes called "metastable state" errors, results from the finite probability that a comparator which is toggling between two logic levels (the analog input is equal to the comparator's reference voltage input) may produce an erroneous binary code at the flash converter's final output. This metastable condition can result in a fullscale error if it occurs at the flash converter's mid-scale code (i.e., bits changing from 0111...1 to 1000...0). These erroneous error codes may show up as white dots or "sparkles" when digitizing television waveforms, hence the term "sparkle codes".Proper design of the comparators and/or use of additional logic algorithms in the decoding function can minimize these errors to an acceptable level for most applications. (See section on Dynamic Testing of A/D Converters for further discussion and how to measure this error.)

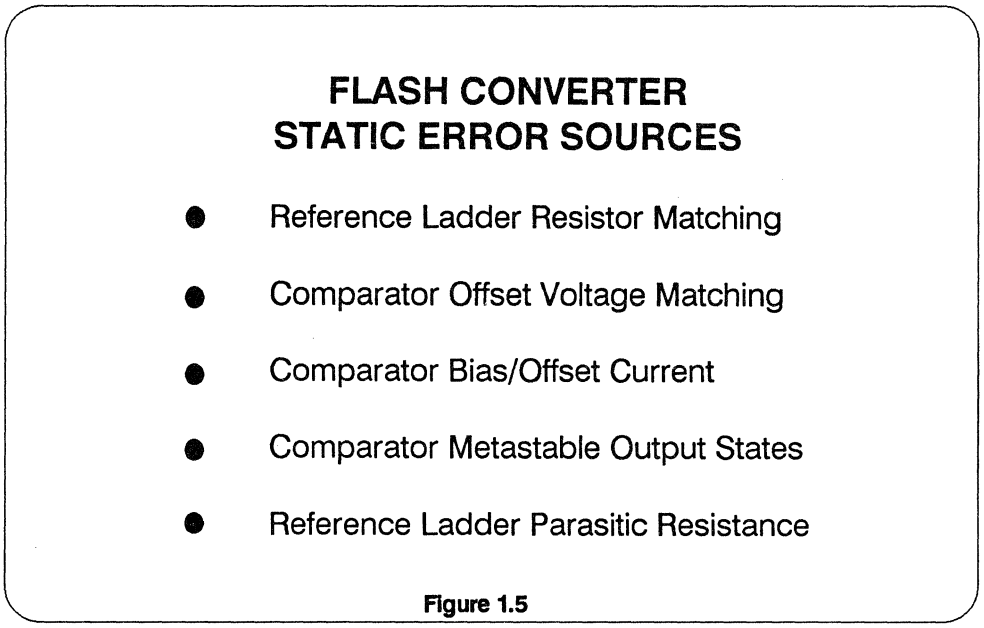


Figure 1.5

Flash Converter Dynamic Error Sources

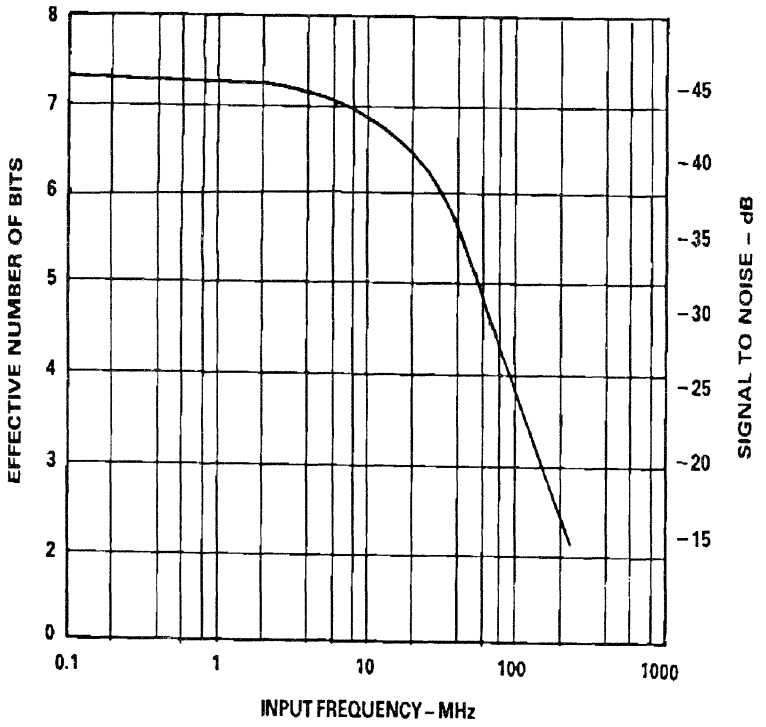
In the majority of video A/D converters (including flash converters), linearity (differential and integral) degrades as the analog input signal slew-rate increases. These errors manifest themselves as increased harmonic distortion, degrada-

tion in signal-to-noise ratio (SNR), missing codes, and spurious or "sparkle" codes. In a flash converter, these degradations occur primarily due to the relative delay mismatch between each comparator in the bank. This delay mismatch is a function of many design-related variables such as IC process variations, chip layout, comparator design, etc. A close to ideal converter would maintain its static performance specifications across the full Nyquist bandwidth (or higher for some applications).

The theoretical RMS signal-to-noise ratio for an N-bit A/D converter is given by the well-known equation

$$SNR = 6.02N + 1.76dB.$$

A typical plot of SNR versus input frequency for an 8-bit flash converter (AD-770) is shown in Figure 1.6 for a 200MHz sampling rate. The dynamic performance can also be evaluated in terms of Effective Number of Bits (ENOB) by solving the equation for N given the measured SNR. See the section on Dynamic Testing for a further discussion of this measurement.



f_S = 200 MSPS

SIGNAL TO NOISE RATIO ANDEFFECTIVE BITS FOR AD-770 8-BIT FLASH CONVERTER

Figure 1.6

Sample-to-sample variations in the effective sampling instant (aperture jitter) can also cause degradation in the overall SNR measurement for high slew-rate inputs. This jitter can be produced internally and/or externally to the flash converter. Proper grounding techniques, power supply decoupling, PC board layout, and clean sampling clock pulses (both phase and frequency stable) are the best techniques to minimize externally produced jitter components.

Glitches or "sparkle codes" due to metastable comparator states as previously discussed, can also occur for high slew-rate input signals.

In addition, high slew-rate inputs may produce what is called a "bubble" in the comparator bank thermometer code output. Ideally, the comparator bank output should be a sequence of logic "1"s followed by a sequence of logic "0"s as shown in Figure 1.2. An out-of-sequence "1" or "0" may occur for high slew-rate inputs due to comparator delay mismatches. This creates a condition which looks like a "bubble" in the normal thermometer code. Depending upon where in the sequence it occurs, the "bubble" may cause the decoding logic to produce a large error code, or "sparkle" code. The probability of getting a "bubble" due to comparator mismatch can be reduced by proper comparator design. The magnitude of the binary error (sparkle code) produced by a "bubble" can be minimized by increasing the sophistication and complexity of the decoding logic.

FLASH CONVERTER
DYNAMIC ERROR SOURCES

- Comparator Delay Mismatch
- Chip Layout Parasitics
- Thermometer Code Bubbles
- Aperture Jitter
- Sampling Clock Jitter
- Front End Bandwidth
- Non-Linear Input Impedance
- Drive Amplifier Non-Linearity
- All Static Error Sources

Figure 1.7

Flash Converter Full-Power Bandwidth

Flash converter "full power bandwidth" (FPBW) is a specification for which there is no currently accepted industry-wide definition. Users of flash converters should scrutinize the data sheet carefully and understand both the manufacturer's definition and test method.

In a traditional op-amp, FPBW typically is meant to be the maximum frequency at which the amplifier is capable of producing the maximum specified peak-to-peak output voltage at some level of distortion. Another commonly used definition is to calculate FPBW from the slew rate (SR) of the amplifier using the equation:

$$FPBW = \frac{SR}{2\pi V_o}$$

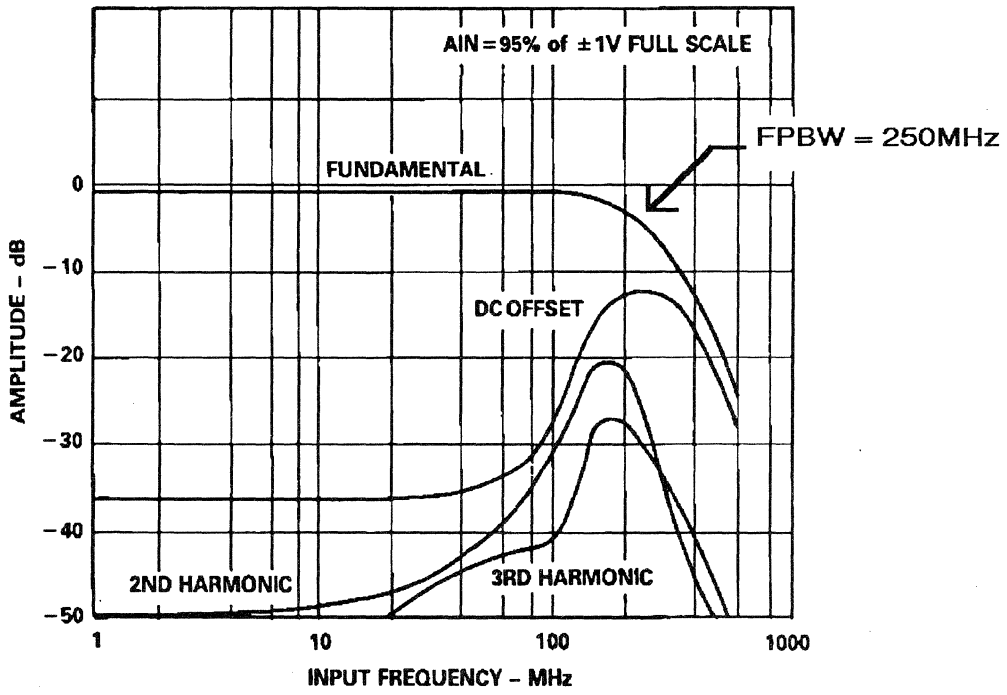
where the output voltage range of the amplifier is $\pm V_o$.

The problem in applying traditional "analog" bandwidth definitions to flash converters is that the results can be very misleading -- typically, the dynamic error sources previously discussed become dominant long before the true analog bandwidth of the comparator front end is approached.

If the FPBW is defined as the frequency at which the peak-to-peak "reconstructed" sinewave output is reduced by 3dB for a fullscale input (a common definition), then the ENOBs or SNR at this input frequency may very well render the flash converter useless in a practical application. Thus, FPBW and ENOB or SNR must be considered together when evaluating flash converter performance. It is also important that the sampling rate be specified, since dynamic degradations are also more likely to worsen as the sampling rate is increased.

Another definition sometimes encountered for FPBW is the maximum fullscale input signal that can be processed by the flash converter at a specified sampling rate without missing any codes. Using this definition will always give the most pessimistic number of any definition previously discussed and, therefore, it appears on only a few A/D data sheets.

A recently proposed definition for FPBW (courtesy Chris Manglesdorf - Senior Scientist at Analog Devices) is that frequency at which the fundamental component of the reconstructed FFT output (neglecting harmonics) of the flash converter is reduced by 3dB from fullscale. Figure 1.8 shows an FFT plot for the AD-770 where the FPBW is measured to be 250MHz using this definition.



HARMONIC DISTORTION VS. INPUT FREQUENCY AT 200 MSPS FOR AD-770

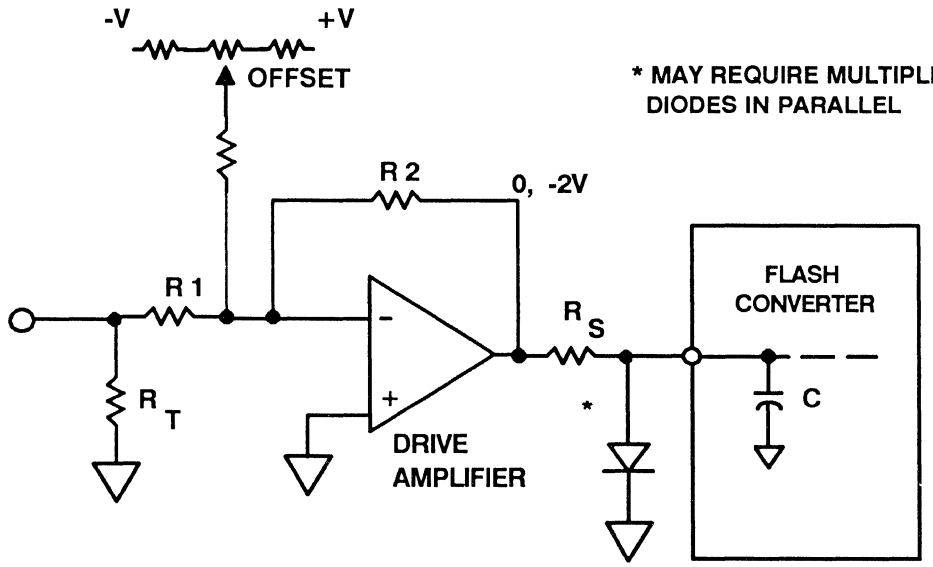
Figure 1.8

Driving Flash Converters

In a system application, the video signal to be digitized by the flash converter usually comes from a 50, 75 or 93 ohm source. This signal may be bipolar or unipolar. Obviously, if the input range of the flash converter is not compatible with the signal, a wideband amplifier will be required to produce the required gain and offset. (See Figure 1.9.)

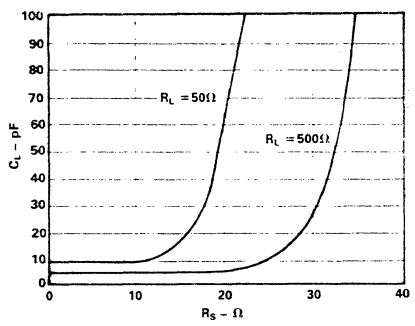
In addition, the input capacitance of some flash converters may vary as a function of the analog input signal, thereby requiring a buffer amplifier for isolation to prevent the non-linear capacitance from producing undesirable harmonics in the digitized signal.

For some flash converters, the input capacitance is so high that a buffer amplifier is required to preserve the signal bandwidth. Figure 1.10 shows the appropriate series resistor value for various load conditions when using the AD-9611 current feedback amplifier as a driver.

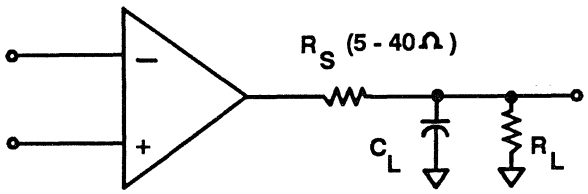


DRIVING FLASH CONVERTERS

Figure 1.9



AD-9611
AD-9615

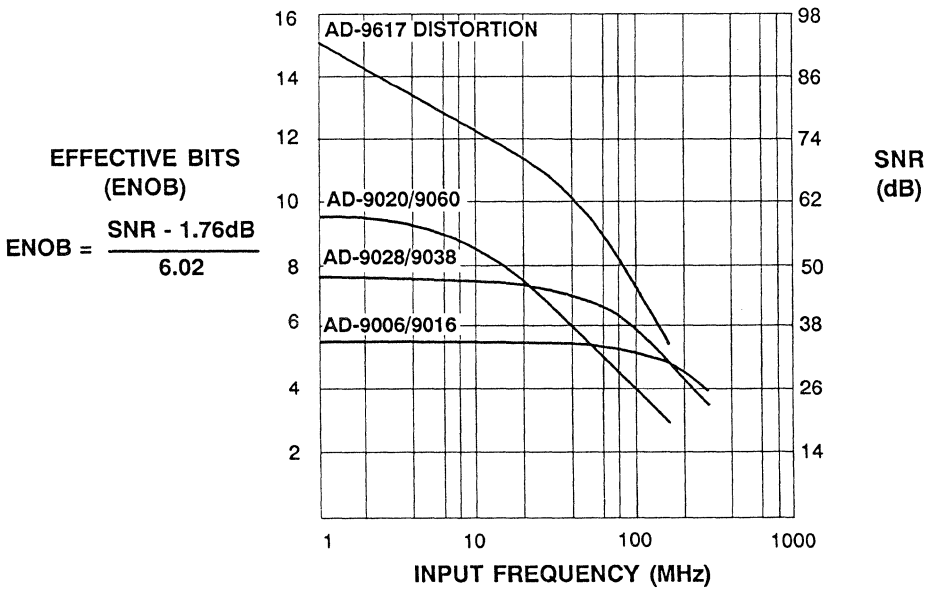


COMPENSATION WHEN DRIVING
CAPACITIVE LOADS

Figure 1.10

Since most applications do require a buffer amplifier ahead of the flash converter, the user must select it carefully. The primary consideration is to match the dynamic performance (harmonics, SNR, etc.) of the amplifier to that of the flash converter so that the inherent performance of the flash converter isn't degraded by the amplifier. Figure 1.11 shows the harmonic distortion of the AD-9617 monolithic current feedback amplifier plotted with the SNR for several flash converters. Fortunately (or unfortunately, depending on your perspective), the flash converter itself is usually the limiting factor to dynamic performance if the amplifier is properly selected. Pay particular attention to the flash converter data sheet, which should list recommended amplifiers and appropriate interface circuits.

Some flash converters have a unipolar negative input voltage range and can be damaged by positive input signals which forward bias the substrate diode. A schottkey diode offers effective protection, as shown in Figure 1.9.



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS
AD9006/9016	6 BITS	400 MSPS

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE

Figure 1.11

The value of R_s should be chosen so that the drive amplifier current is limited to an appropriate value for positive output swings. Making the value of R_s too large, however, will reduce the bandwidth because of the input capacitance of the flash converter. Figure 1.12 lists a number of flash converters along with recommended drive amplifiers.

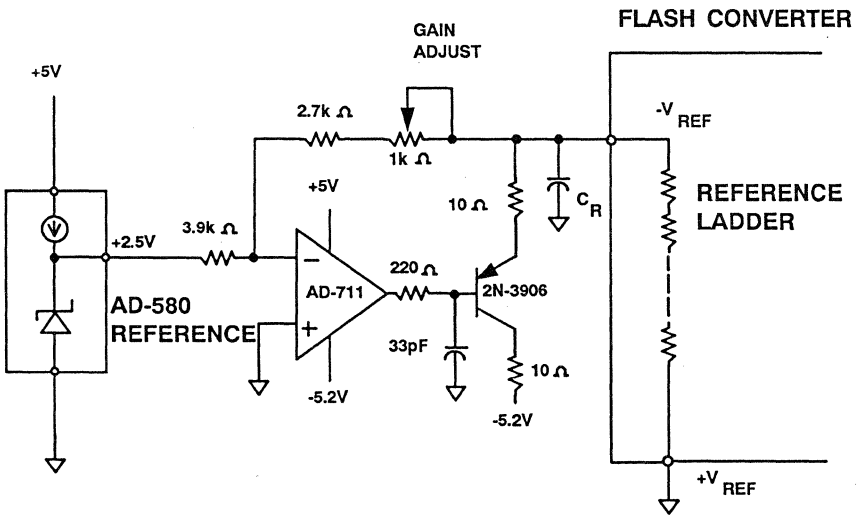
FLASH CONVERTERS AND RECOMMENDED DRIVE AMPLIFIERS

MODEL	RESOLUTION	MAX. SAMPLING RATE	INPUT C	DRIVE AMPLIFIER
AD9688	4-Bits	175 MSPS	10pF	AD5539
AD9000	6-Bits	75 MSPS	35pF	AD844
AD9006/16	6-Bits	500 MSPS	8.5pF	AD9617
AD9048	8-Bits	35 MSPS	16pF	AD847
AD9012	8-Bits	75 MSPS	16pF	AD9617
AD9002	8-Bits	125 MSPS	16pF	AD9617
AD770	8-Bits	200 MSPS	19pF	AD9617
AD9028/38	8-Bits	300 MSPS	17pF	AD9617
AD9020	10-Bits (TTL)	60 MSPS	45pF	AD9617
AD9060	10-Bits (ECL)	75 MSPS	45pF	AD9617

Figure 1.12

Flash Converter Reference Voltage Generation

Since few flash converters contain an internal voltage reference, this must be supplied by the user. A typical reference voltage circuit for a flash converter requiring a single -2V reference is shown in Figure 1.13. A buffer transistor is required since the resistance of the ladder string is usually fairly low and, therefore, fairly large drive currents are required. Also, the reference ladder resistance of a flash converter is process dependent and may vary considerably from part to part. It may also have a large temperature coefficient (see Figure 1.14).



SINGLE-ENDED REFERENCE VOLTAGE GENERATOR

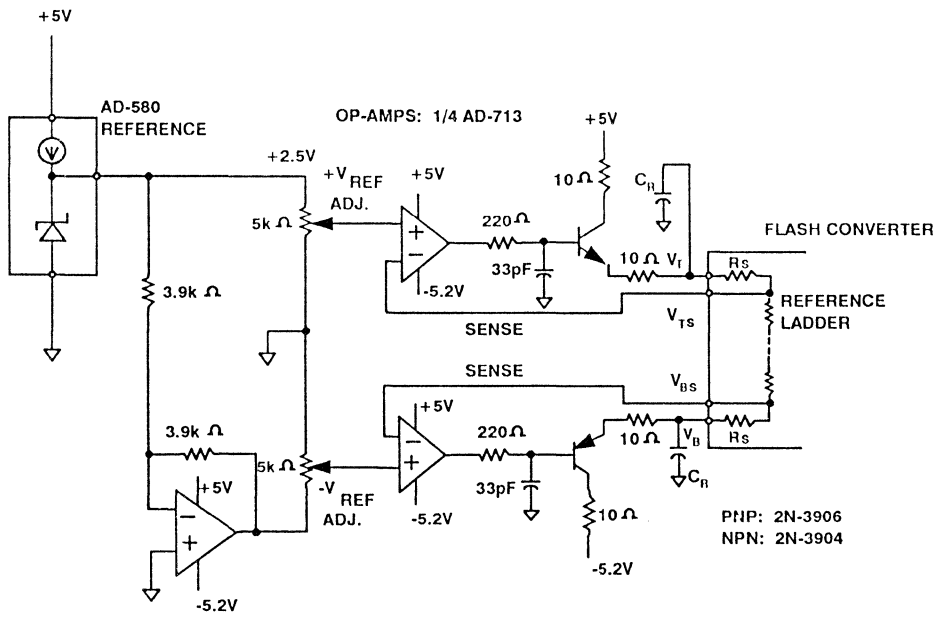
Figure 1.13

NOMINAL REFERENCE LADDER RESISTANCE AND TC

AD-9688	350 Ω, 2000 ppm/°C
AD-9000	150 Ω, 2000 ppm/°C
AD-9006/9016	80 Ω, 2750 ppm/°C
AD-9048	90 Ω, 2500 ppm/°C
AD-9012	90 Ω, 2750 ppm/°C
AD-9002	90 Ω, 2750 ppm/°C
AD-770	200 Ω, 3400 ppm/°C

Figure 1.14

If the flash converter allows bipolar operation (such as the AD-770 and the AD-9000), two reference voltages must be generated. The circuit in Figure 1.15 operates on ±5V power supplies and allows great flexibility in setting the reference voltages for a bipolar flash converter.



BIPOLAR REFERENCE VOLTAGE GENERATOR

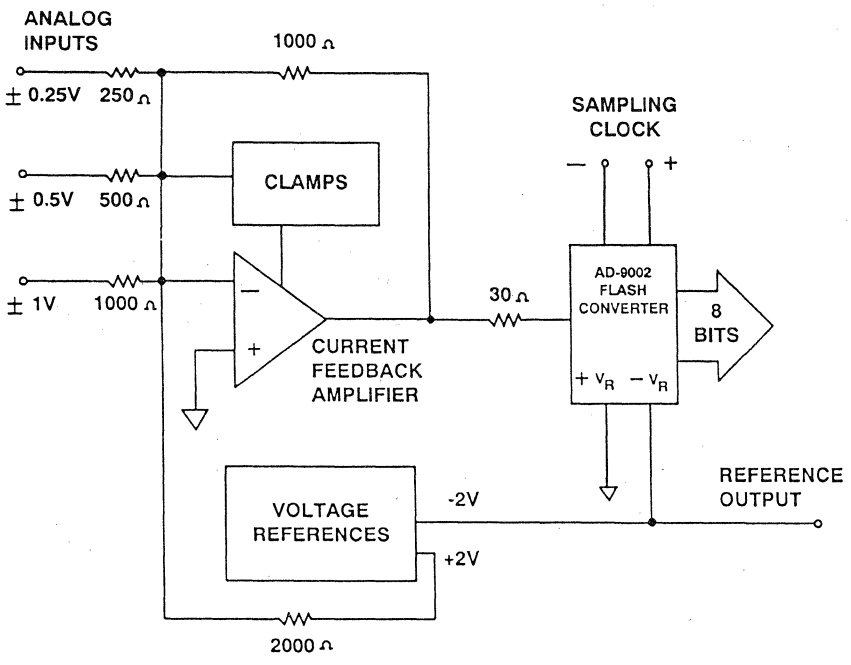
Figure 1.15

Some flash converters have a "sense" pin for the voltage reference which can be used to compensate for the voltage drop due to the package pin and bond wire resistance. This feature is utilized in the circuit shown in Figure 1.15.

Flash converters may provide access to one or more taps along the internal reference ladder resistor string. These taps can be driven from low impedance sources in order to achieve better integral linearity performance. Again, when in doubt, consult the data sheet! Bypass capacitors on the reference voltage inputs are particularly critical at sampling rates of 20MHz or greater. Ceramic chip capacitors are recommended (0.1 μF) and should be located as close to the pins as possible.

Hybrid Circuits Simplify Applications

Several hybrid circuit manufacturers have recently introduced hybrid A/D converters which contain a drive amplifier and a reference voltage as well as the flash converter itself. A block diagram of the AD-9011 8-BIT, 100MSPS hybrid A/D converter is shown in Figure 1.16.

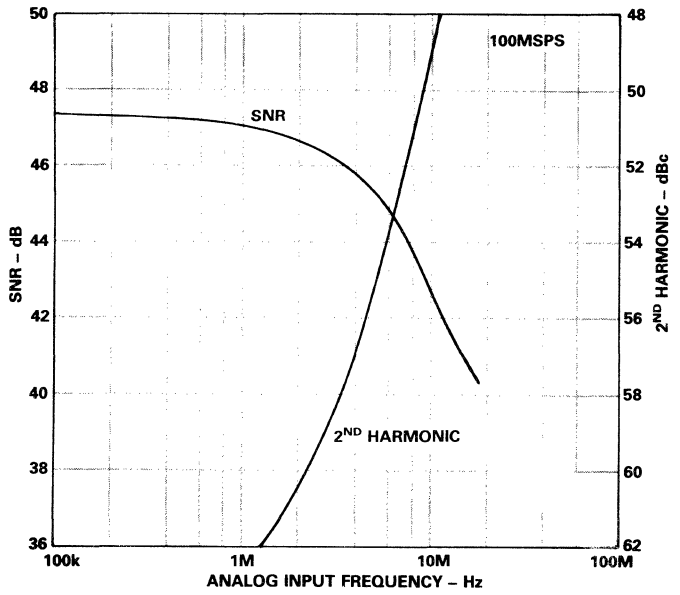


AD-9011 HYBRID: 8-BIT, 100 MSPS

Figure 1.16

The current-feedback amplifier is designed to recover from an overvoltage condition within 20ns. Clamp limits are set to protect the flash converter input. The current feedback amplifier architecture insures that the bandwidth will remain relatively constant regardless of the gain chosen.

The SNR and harmonic distortion characteristics of the AD-9011 are shown in Figure 1.17.



AD-9011 SNR AND HARMONIC PERFORMANCE, f_s = 100 MSPS

Figure 1.17

Capturing Flash Converter Output Data

At high data rates in excess of 200MHz, buffering flash converter output data can be a major challenge. It is always desirable to follow the flash converter with an appropriate buffer register located as close to the converter as possible.

If the digital outputs of a flash converter are routed directly to a backplane data bus through a card edge connector, the overall SNR and harmonic performance of the flash converter may be severely degraded by the digital output signals coupling into the analog input.

The appropriate logic family can be selected using the information in Figure 1.18.

LOGIC FAMILY MAXIMUM FLIP-FLOP TOGGLE FREQUENCY

TTL LOGIC

BIPOLAR		CMOS	
74 LS	33 MHz	74 HCT	50 MHz
74 ALS	50 MHz	74 ACT	125 MHz
74 S	95 MHz		
74 AS	125 MHz		

ECL LOGIC

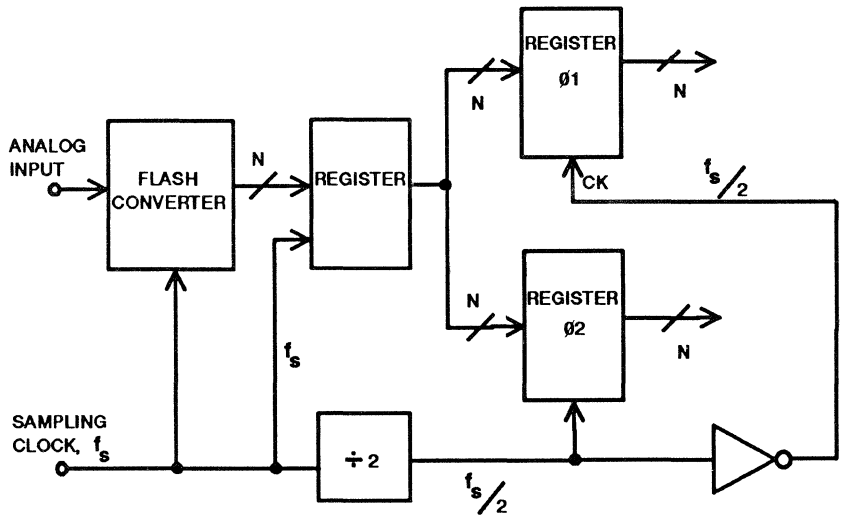
10K-100	125 MHz
10K-200	200 MHz
10KH	250 MHz
100K	375 MHz
ECLIPS	600 MHz

Figure 1.18

Proper timing of the buffer register clock with respect to the flash converter sampling clock is best accomplished by following the recommendations on the data sheet. At high data rates, the setup time and hold time specifications on the selected buffer register become particularly important in optimizing the timing for reliable operation.

In most applications, flash converter output data is stored in a buffer memory of considerable length. Schemes such as that shown in Figure 1.19 are often used to de-multiplex the high-speed data stream down to frequencies which are appropriate for low cost efficient CMOS or TTL memories.

Some of the newer flash converters which operate at sampling rates greater than 200MHz (such as the AD-9006/9016) will have de-multiplexing on-board to minimize the problems associated with high-speed data storage.



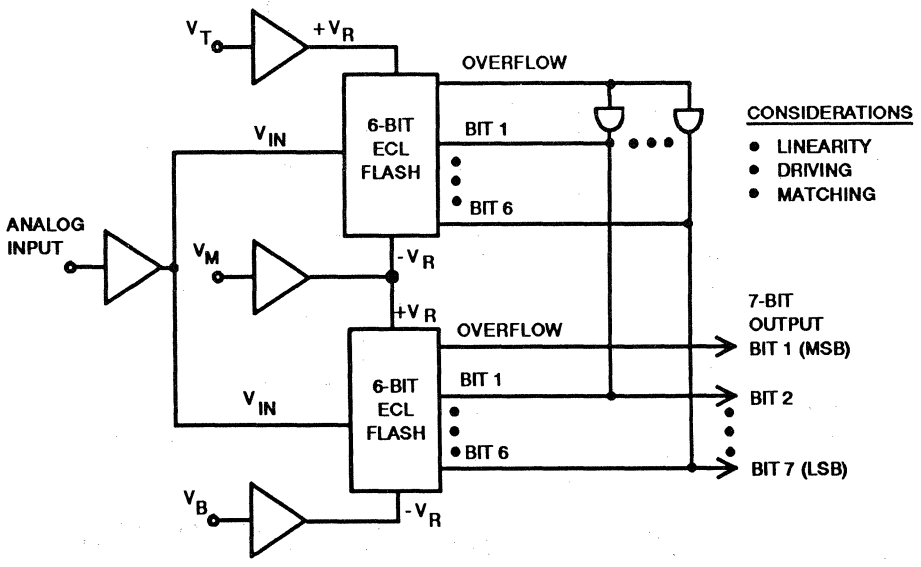
DEMULTIPLEXING FLASH CONVERTER OUTPUTS

Figure 1.19

"Stacking" Flash Converters To Achieve Higher Resolutions

The concept of "stacking" flash converters originated in the late 1970's when the only commercially available flash converters that had sampling rates in excess of 50MHz were 4-or 6-bit devices such as the AMD-6688 (4-bit) and the Seimens SDA-6020 (6-bit). The technique is much less popular today because of the availability of 8-bit 100-200MHz flash converters such as the AD-9002 and the AD-770.

Figure 1.20 shows an application where two 6-bit AD-9000 flash converters have been connected to achieve 7-bit resolution. The six LSB's are obtained by wire-oring the 6-bit ECL output of each flash converter -- the MSB is simply the "overflow" output of the bottom flash (the 64th comparator). The overflow output of the top flash converter must be used with additional logic to prevent the six LSB's from going to all zeros when the analog input signal goes out of range positive. Some flash converters have "overflow inhibit" logic which allows them to be used either stacked or unstacked without the need for additional external logic.



STACKING FLASH CONVERTERS

Figure 1.20

Several factors relating to the flash converter's performance must be considered when stacking flashes.

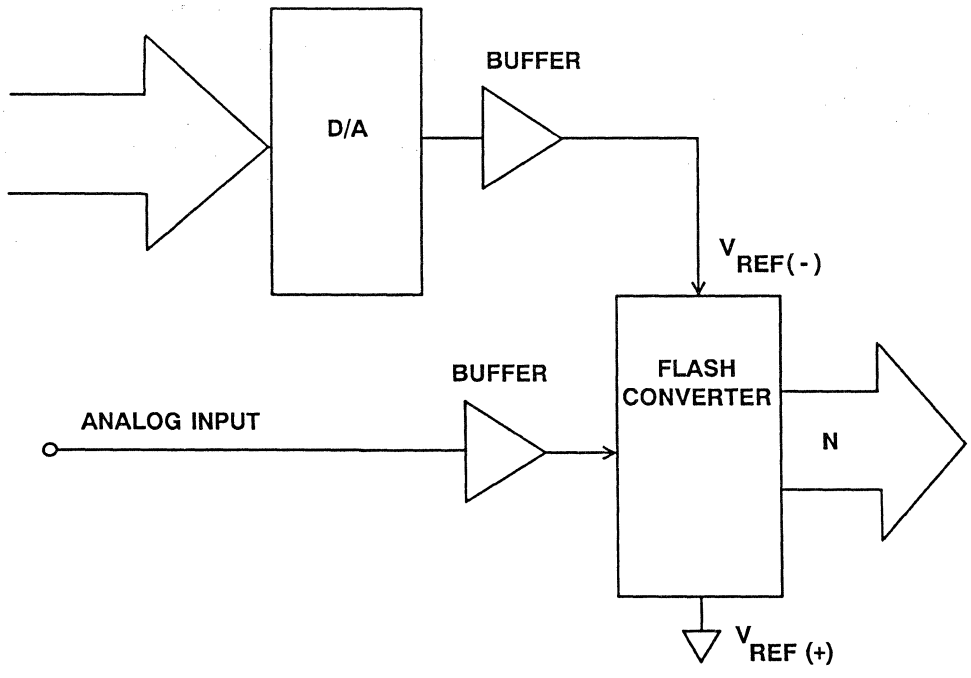
- The flash converter must have the additional "overflow" or 2^{Nth} comparator output available.
- ECL output logic levels are desirable to simplify the external logic.
- The flash converter must have the required linearity when operating at the appropriate reference voltage. For instance, if a flash converter is specified as having ±1/2 LSB linearity for a 2-volt reference, it can be assumed that operating the converter at a 1-volt reference would yield ±1 LSB linearity and produce missing codes. The linearity spec, therefore, needs to be ±1/4 LSB for a 2-volt reference in order to consider stacking two converters and still maintain the overall 2-volt reference range.
- In order to maintain dynamic performance, the two flash converters need to have well matched comparator delays. This may be difficult to insure since there is no guarantee that the two flash converters come from the same wafer or wafer lot.

In summary, stacking should be avoided except in applications where no other solution is available.

Reducing Flash Converter Reference Voltage to Achieve Greater Dynamic Range

The effective "gain" of a flash converter can be increased by lowering the reference voltage. However, the same precaution referred to in "stacking" must be observed regarding the flash linearity specification at reduced reference voltages. At least ±1/2 LSB linearity should be maintained at the lowest reference voltage. In addition, the maximum reference voltage must not exceed the data sheet spec.

Operating within these constraints, a flash converter can be configured as a Programmable Gain A/D converter if the reference voltage is derived from a D/A converter. The gain switching speed can be fairly high since the flash converter reference voltage input bandwidth specification is typically 10MHz or higher. Reference input capacitances are typically less than 50pF and are, in general, slightly higher than the analog input capacitance. A diagram of a variable-gain flash converter circuit is shown in Figure 1.21.



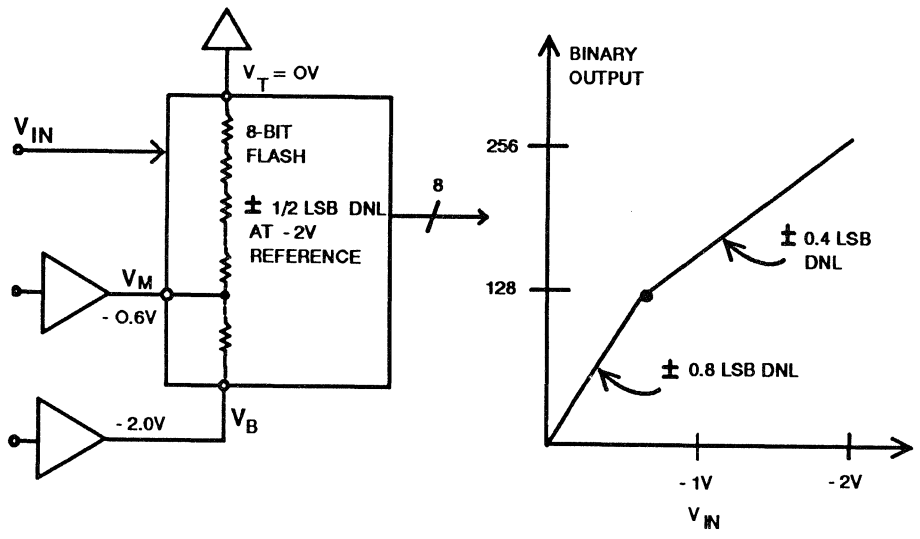
PROGRAMMABLE GAIN FLASH CONVERTER

Figure 1.21

Generation of Non-Linear Flash Converter Transfer Characteristics

If taps are available on the reference ladder string for a flash converter, a piecewise non-linear input/output transfer function can be generated. Figure 1.22 shows how the AD-9002 might be used in such an application to generate a two-piece transfer curve.

In this application, the minimum reference voltage on a portion of the resistor string is that for which the ±1/2 LSB linearity spec can still be maintained, and the maximum reference voltage for a portion of the string is governed by the data sheet spec on maximum allowable reference ladder voltage and current.



GENERATING NON-LINEAR TRANSFER FUNCTIONS

Figure 1.22

Using Two Flash Converters With Common Inputs to Double the Sampling Rate

With certain limitations, it is possible to alternate (or "ping-pong") the encode command pulse between two flash converters and effectively double the sampling rate. Figure 1.23 shows such an application. Several factors should be considered in evaluating the merits of this scheme.

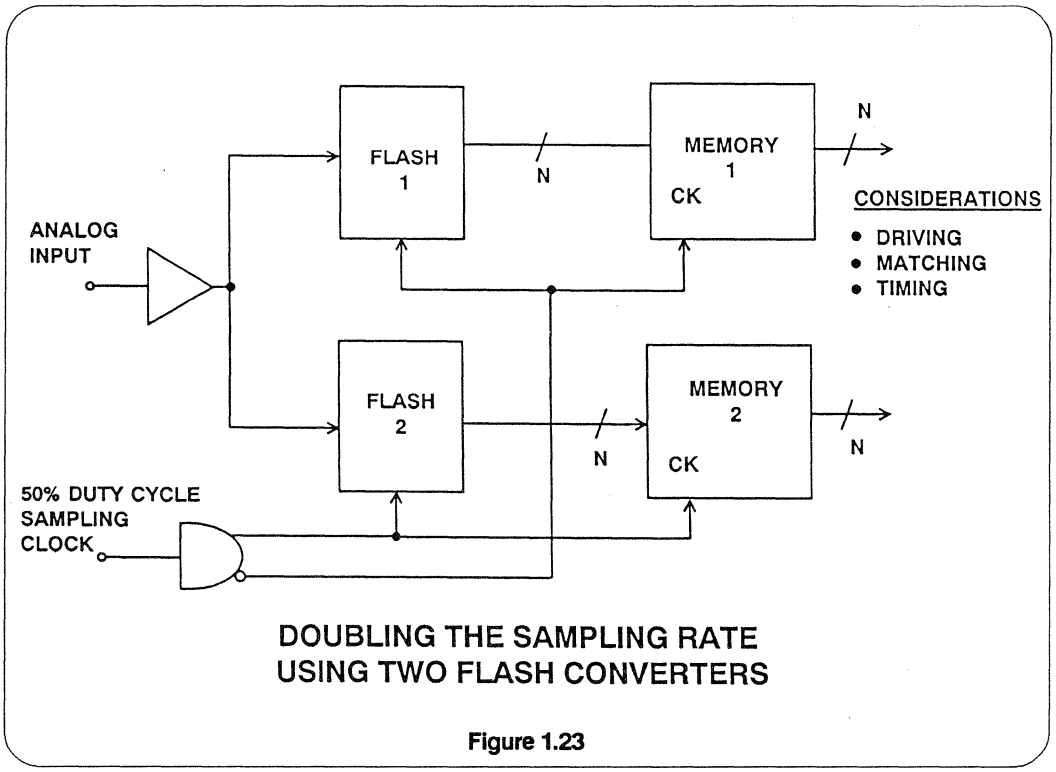


Figure 1.23

- The drive amplifier must be capable of driving the combined impedances of both flash converters to the required dynamic accuracy.

- Although the sampling rate can be doubled using this technique, the individual flash converters must maintain ENOB's, SNR, and harmonic performance at the higher analog input frequencies which will accompany the higher sampling rate. This implies that each individual flash converter be specified for analog input frequencies which are above the Nyquist rate (super-Nyquist) and which approach the maximum sampling rate.

- Delay and bandwidth mismatch between the two flash converters must not be so large as to degrade dynamic performance.

- DC differential linearity, integral linearity, gain, and offset matching between the two flash converters should be better than ±1/2 LSB.

In summary, it is difficult to use this approach and achieve anything close to Nyquist performance, but the technique may be useful for sub-Nyquist or over-sampling applications.

Use Of Track-And-Hold To Improve Flash Converter Dynamic Performance

As has been previously discussed, the effective sample time delay variations among the latched comparators in a flash converter is a primary source of dynamic errors manifested as degradation in ENOB's, SNR, and harmonic performance. Individual comparators within an array can be visualized as having variable delay lines in series with their latch strobe inputs. To understand the effect of this delay on performance, consider an 8-bit, 100MHz flash converter which is digitizing a fullscale 50MHz sinewave input (Nyquist operation). The sinewave can be expressed as:

$$v(t) = V_p \sin 2\pi f t.$$

The maximum rate-of-change of this signal occurs are the zero-crossing and is given by:

$$\left.\frac{dv}{dt}\right|_{max} = 2\pi f V_P \approx \left.\frac{\Delta v}{\Delta t}\right|_{max}$$

Solving for Δt_{max}, we obtain

$$\Delta t_{max} = \frac{\Delta v}{2\pi f V_P}$$

If the input voltage range of the flash converter is 2 volts (V_p=1V), the LSB weight is 8mV for an 8-bit flash. For the flash converter error to be less than 1 LSB (8mV), the equation can be solved for Δt_{max}, and the result is

$$\Delta t_{max} = 25ps$$

This says that the effective sample delay mismatch between comparators cannot exceed 25ps in order to ensure no missing codes when digitizing a 50MHz fullscale sinewave input.

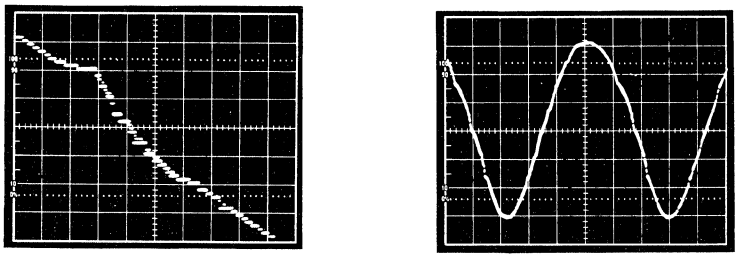
Placing an ideal track-and-hold ahead of the flash converter would theoretically eliminate this problem since the flash converter would be basically digitizing a DC input (the "held" value of the track-and-hold output). In actual practice,

track-and-holds are not ideal -- especially at high speeds. The result is that the signal actually presented to the flash converter is still changing, although at a slower rate. Even this "track-and-slow-down" approach can improve the flash converter performance at sampling rates up to about 25MHz. Above 25MHz sampling rates, the track-and-hold circuit needs to be mounted on the same substrate as the flash converter in a suitable hybrid package. Monolithic track-and-holds have been successfully used in conjunction with 8-bit flash converters in hybrid packages to achieve 7 ENOBs at Nyquist inputs sampling at a rate of 250MHz. The penalty is cost and power (7 watts). (Tektronix Model TKAD20C).

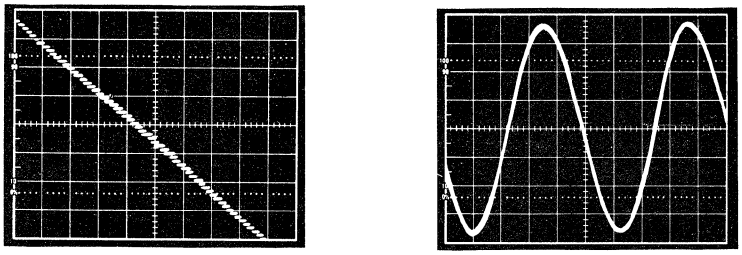
Figure 1.24 shows the improvement in dynamic linearity which can be achieved by putting a hybrid track-and-hold (HTS-0025) ahead of an older flash converter (TDC-1007).

Nevertheless, the user should strive to select a flash converter which does not need a track-and-hold in order to achieve the desired dynamic performance required for the particular application. The performance of the track-and-hold/flash converter pair is almost impossible to determine from the separate data sheet specifications alone, and considerable experimentation may be required to achieve the desired results. The optimum timing relationship between the two devices will also be difficult to determine without considerable experimentation.

In the future, lower cost monolithic track-and-holds will be packaged with the flash converters in high performance hybrids, and be fully specified for dynamic characteristics. For most applications, however, improvements in flash converter designs and IC processes will probably eliminate the need for a separate track-and-hold except for the most exacting user.



T/H INACTIVE



T/H ACTIVE

EFFECTS OF TRACK-AND-HOLD ON
FLASH A/D PERFORMANCE

f_{IN} = 19.98 MHz, f_S = 20.00 MHz

Figure 1.24

FLASH CONVERTER SELECTION GUIDE

RESOLUTION	MODEL	MAXIMUM SAMPLING RATE (MSPS)
4-Bits	AD9688	175 - ECL
6-Bits	AD9000	75 - ECL
6-Bits	AD9006/9016	500 - ECL
8-Bits	AD9048	35 - TTL
8-Bits	AD9012	75 - TTL
8-Bits	AD9002	125 - ECL
8-Bits	AD770	200 - ECL
8-Bits	AD9028/9038	300 - ECL
8-Bits	AD9011*	100 - ECL
10-Bits	AD9020	60 - TTL
10-Bits	AD9060	75 - ECL

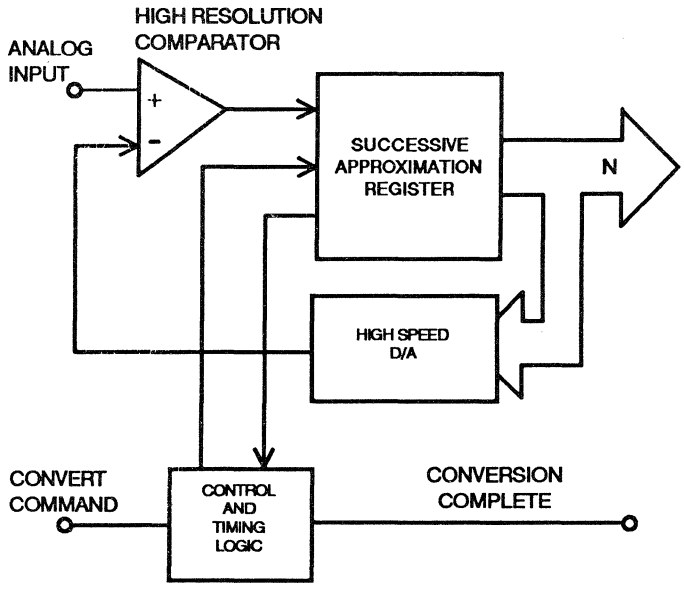
*HYBRID WITH INTERNAL AMP, REFERENCES

Figure 1.25

SUCCESSIVE APPROXIMATION A/D CONVERTERS - Basic Operation

This A/D converter architecture has been the "workhorse" in the industry primarily because it combines relatively high resolution and speed with low cost. New IC process developments in CMOS allow 12-bit, 3 μsec. converters to be achieved in monolithic form (AD-7672). In the past, this performance was only available from more expensive hybrid and modular products.

A block diagram of a successive approximation A/D converter is shown in Figure 1.26. The building blocks consist of a comparator, D/A converter, and control logic (successive approximation register, or SAR). The overall static accuracy is primarily determined by the D/A converter.



SUCCESSIVE APPROXIMATION A/D CONVERTER

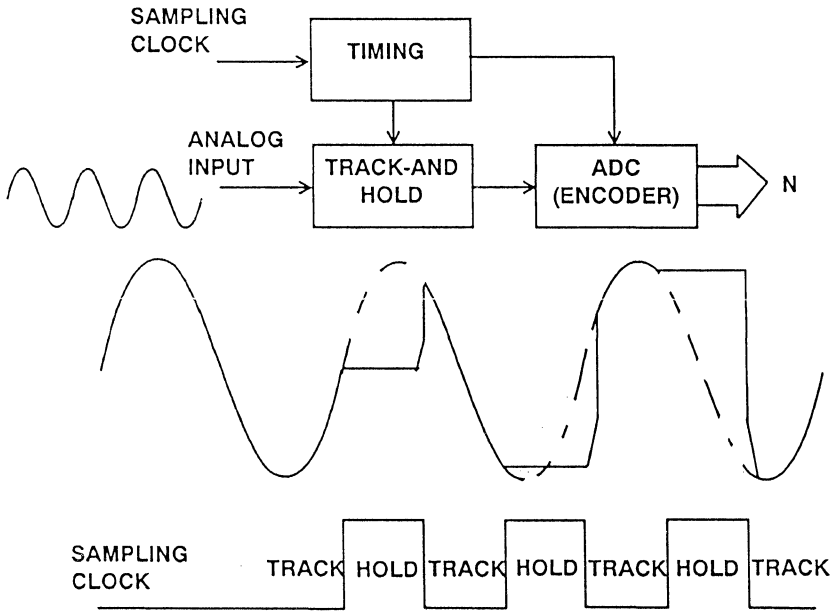
Figure 1.26

The analog input drives one input of the comparator, while the D/A converter output is connected to the other input. The conversion technique consists of comparing the unknown input against a precise voltage or current generated by a D/A converter. The input of the D/A converter is the digital number at the A/D converter's output. The conversion process is strikingly similar to a weighing process using a chemist's balance, with a set of N binary weights (e.g., 1/2 lb, 1/4 lb, 1/16 lb (=1 oz), 1/2 oz, 1/4 oz, etc., for unknowns up to 1 lb.)

After the conversion command is applied, and the converter has been cleared, the D/A converter's MSB output (1/2 full scale) is compared with the input. If the input is greater than the MSB, it remains ON (i.e., "1" in the output register), and the next bit (1/4 FS) is tried. If the input is less than the MSB, it is turned OFF (i.e., "0" in the output register), and the next bit is tried. If the second bit doesn't add enough weight to exceed the input, it is left ON ("1") and the third bit is tried. If the second bit tips the scales too far, it is turned OFF ("0") and the third bit is tried. The process continues in order of descending bit weight until the last bit has been tried. The process completed, the conversion complete line changes state to indicate that the contents of the output register now constitute a valid conversion. The contents of the output register form a binary digital code corresponding to the input signal's magnitude.

Each of the bit decisions requires a clock period. An N-bit converter will have N clock periods (plus an initialization period). Thus, the minimum conversion time of the A/D will be determined by the maximum allowable clock frequency. This frequency is limited by several factors: SAR clock-to-data-output delay, D/A settling time, comparator settling time, and SAR input data setup time. Hybrid 12-bit SAR A/D converters are available which have total conversion times approaching 1μsec.

During the conversion time, it is important that the analog input signal be held constant. This requires that a SAR A/D converter be preceded with an appropriate track-and-hold if dynamic signals are to be digitized. Figure 1.27 shows a typical configuration. As has been previously discussed, it is difficult to determine the overall dynamic performance of this system by examining the separate data sheets for the track-and-hold and the SAR A/D (sometimes called the "encoder"). A more desirable solution is to purchase a "sampling" A/D converter where the track-and-hold, encoder, and appropriate timing circuits are contained in a single package which is fully specified for dynamic performance.



ADC WITH TRACK-AND-HOLD

Figure 1.27

SUCCESSIVE APPROXIMATION A/D CONVERTER SELECTION GUIDE

ENCODERS (NO T/H)

RESOLUTION	MODEL	CONVERSION TIME	TECHNOLOGY
12-Bits	AD-7572	5 μ sec	IC-CMOS
12-Bits	AD-7672	3 μsec	IC-CMOS
12-Bits	HAS-1202-A	1.86 μ sec	Hybrid
12-Bits	AD-1377	10 μ sec	Hybrid

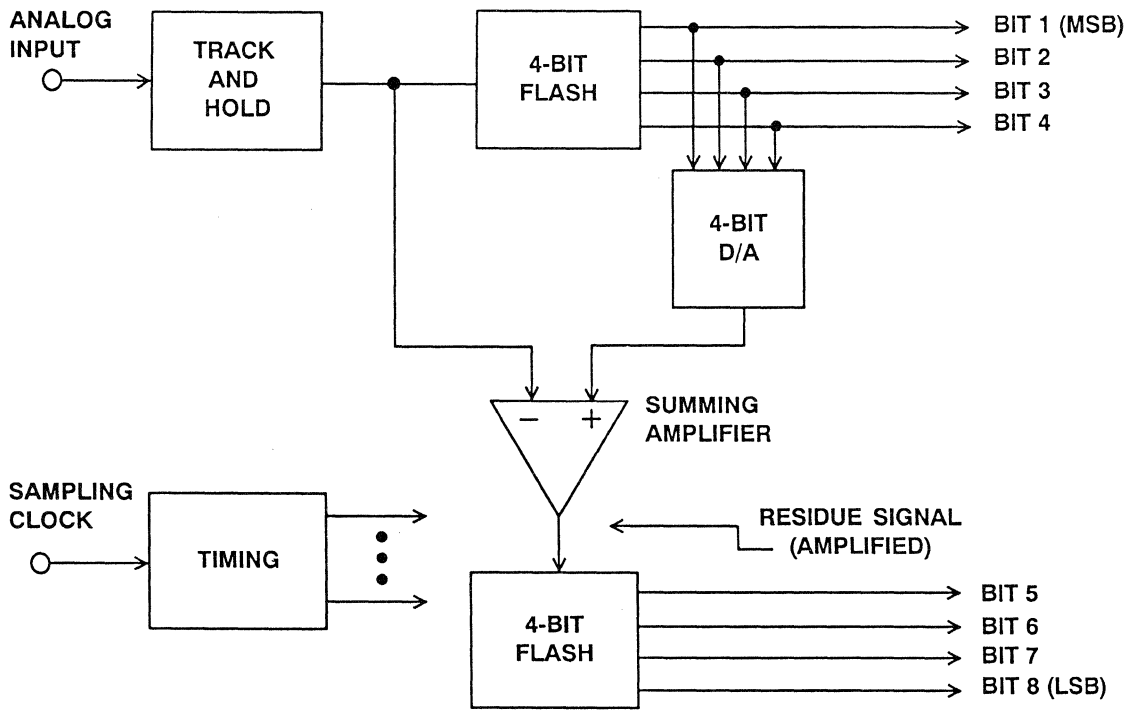
SAMPLING A/D CONVERTERS (WITH T/H)

RESOLUTION	MODEL	SAMPLING RATE	TECHNOLOGY
12-Bits	HAS-1204	500 kHz	Hybrid
12-Bits	AD-7878	100 kHz	IC-CMOS
14-Bits	AD-7871	83 kHz	IC-CMOS
16-Bits	AD-1380	50 kHz	Hybrid

Figure 1.28

SUBRANGING A/D CONVERTERS - Basic Operation

A block diagram of an 8-bit subranging A/D converter based upon two 4-bit flash converters is shown in Figure 1.29. The conversion process is done in two steps. The first four significant bits (MSBs) are digitized by the first flash (to better than 8-bits accuracy), and the 4-bit binary output is applied to a 4-bit D/A converter (better than 8-bit accurate). The D/A converter output is subtracted from the held analog input, and the resulting residue signal is amplified and applied to the second 4-bit flash converter by the summing amplifier. The outputs of the two 4-bit flash converters are then combined into a single 8-bit binary output word. If the amplified residue signal doesn't exactly fill the range of the second flash converter, non-linearities and missing codes will result.



8-BIT SUBRANGING A/D CONVERTER

Figure 1.29

Subranging A/D Converters - Error Sources

The following sources can contribute to errors in the basic subranging A/D converters:

SUBRANGING ERROR SOURCES

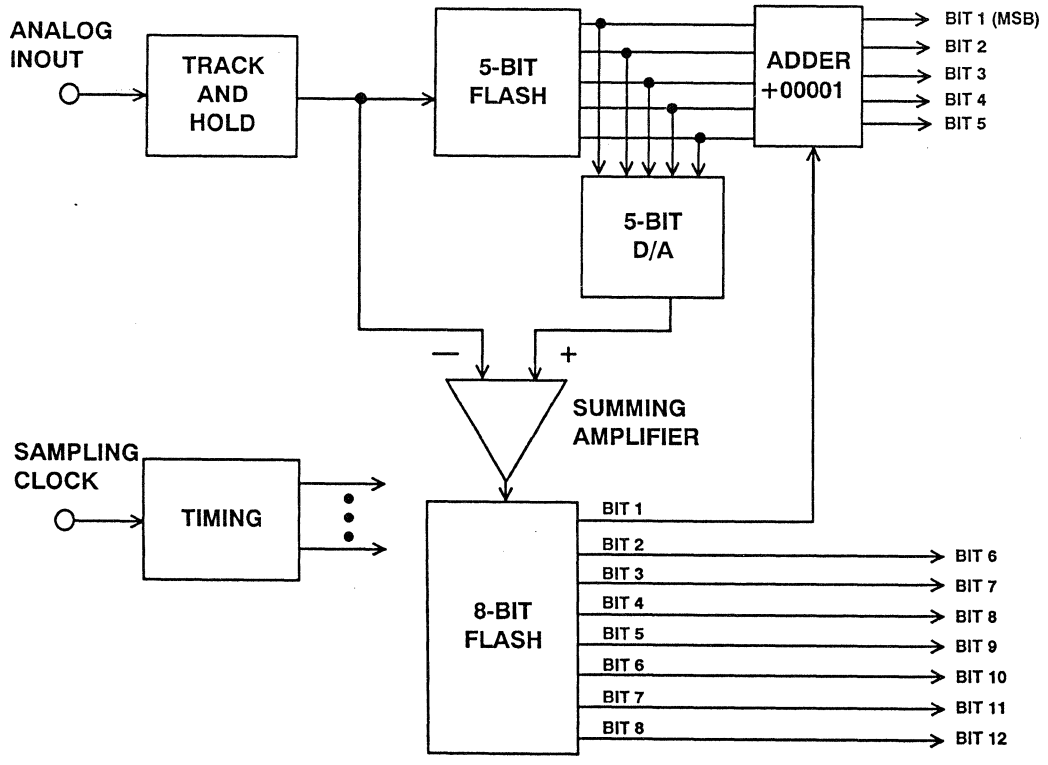
- First flash converter gain, offset, and linearity errors.
- D/A converter gain, offset, and linearity errors.
- D/A converter settling time.
- Summing amplifier gain, offset, and settling time errors.
- Second flash converter gain, offset, and linearity errors.

Figure 1.30

These errors are very troublesome at the "subranging" points and can contribute to non-linearities and missing codes in the overall A/C converter transfer function. Modern subranging A/D converters use a technique called "digital correction" to eliminate most of these problems.

DIGITALLY CORRECTED SUBRANGING (DCS) A/D CONVERTERS - Basic Operation

A block diagram of a 12-bit DCS A/D converter is shown in Figure 1.31. Note that a 5-bit and an 8-bit flash converter have been utilized to achieve a 12-bit DCS output. If there were no errors, the 5-bit "residue" signal applied to the 8-bit flash converter by the summing amplifier would never exceed one-half of the range of the 8-bit flash. The extra range in the second flash converter is used in conjunction with the error correction logic (usually just an adder) to correct the output data for most of the errors inherent in the traditional uncorrected subranging converter previously discussed. An in-depth treatment of DCS A/D converter operation and design is given in the article entitled "Multistage Error Correcting A/D Converters".



12-BIT SUBRANGING A/D CONVERTER - DCS

Figure 1.31

The following error sources can be corrected by proper use of this technique:

ERRORS CORRECTED BY DCS TECHNIQUE

- Track-and-hold droop error.
- Track-and-hold settling time error.
- First flash gain, offset, and linearity error.
- D/A converter offset error.
- Summing amplifier offset error.
- Second flash offset error.

Figure 1.32

Proper use of the DCS technique will either correct for the above errors or translate them into either a gain and/or offset error in the transfer function of the overall A/D converters.

This technique is ideally suited to high-speed cost-effective A/D converters and has been used successfully in card-level, hybrid, and monolithic A/D converters. These products have on-board track-and-hold functions and are completely specified in terms of both static and dynamic performance characteristics.

DCS A/D CONVERTER SELECTION GUIDE

SAMPLING A/Ds (WITH T/H)

RESOLUTION	MODEL	SAMPLING RATE	TECHNOLOGY
10-Bits	CAV1040	40 MHz	PC Card
12-Bits	AD1678/678	200 kHz	IC
12-Bits	AD9003	1 MHz	Hybrid
12-Bits	AD9005	10 MHz	Hybrid
12-Bits	CAV1220	20 MHz	PC Card
14-Bits	AD1679/679	100 kHz	IC
14-Bits	AD1779/779	100 kHz	IC
14-Bits	AD9014	10 MHz	PC Card

ENCODERS (NO T/H)

RESOLUTION	MODEL	CONVERSION TIME	TECHNOLOGY
12-Bits	AD671	500 ns	IC

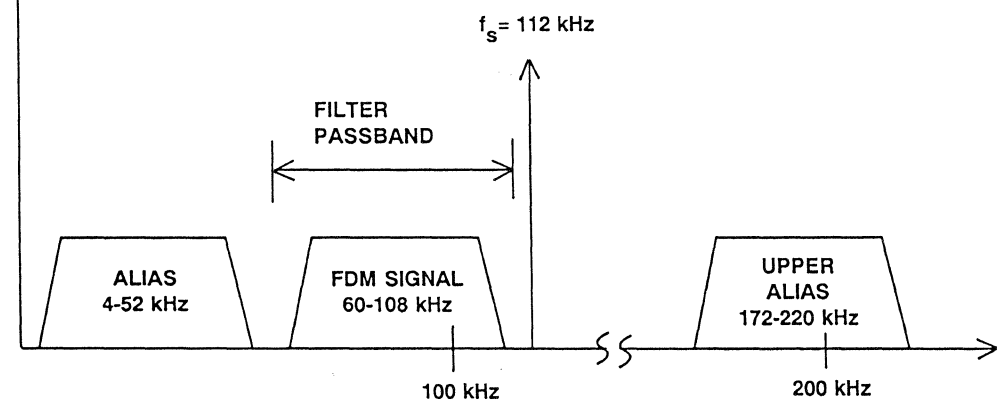
Figure 1.33

A/D CONVERTER APPLICATIONS

- Undersampling (Super-Nyquist)
- Oversampling
- Dithering
- Multiplexing

UNDERSAMPLING, SUPER-NYQUIST, AND DOWN CONVERSION APPLICATIONS

When the analog signal being digitized by an A/D converter exceeds one-half the sampling rate, the condition is often referred to as "super-Nyquist" or "undersampling". Nyquist's criterion state that the bandwidth (not the actual frequency) of the signal being digitized should not exceed one-half the sampling rate for all information to be preserved. As an example, consider a telecommunications transmultiplexer application where Frequency Division Multiplexed (FDM) data occupying the bandwidth of 60 to 108kHz is sampled at a frequency of 112kHz. Figure 1.34 shows the spectrum of the signal and the location of the "aliased" components. At the receiving end of the system, the filter which follows the reconstruction D/A converter is a bandpass rather than a lowpass and must filter out the "aliased" components falling between 4kHz and 52kHz as well as the component located at the sampling frequency of 112kHz.



SUPER-NYQUIST SAMPLING OF FDM SIGNAL

Figure 1.34

Operation of an A/D converter in super-Nyquist applications obviously requires that the dynamic performance of the converter be known for input frequencies above $f_s/2$. The SNR, ENOB, and harmonic performance of an A/D converter typically degrades as the input frequency is increased and may render the converter useless for super-Nyquist applications. For example, it may be necessary to use a track-and-hold ahead of a flash converter in order to achieve acceptable dynamic performance.

Another application for "super-Nyquist" operation is in the direct conversion of IF signals to baseband. Most traditional communication and radar receivers employing A/D converters utilize a system in which the intermediate frequency (IF) from the front end of the receiver is down-converted to a baseband signal by a mixer (see Figure 1.35). This final IF stage uses a local oscillator which is phase coherent with the signal carrier frequency. The mixer output contains a baseband signal which is proportional to the phase difference between the two inputs. Following the mixer is a lowpass filter, DC amplifier, and an A/D converter.

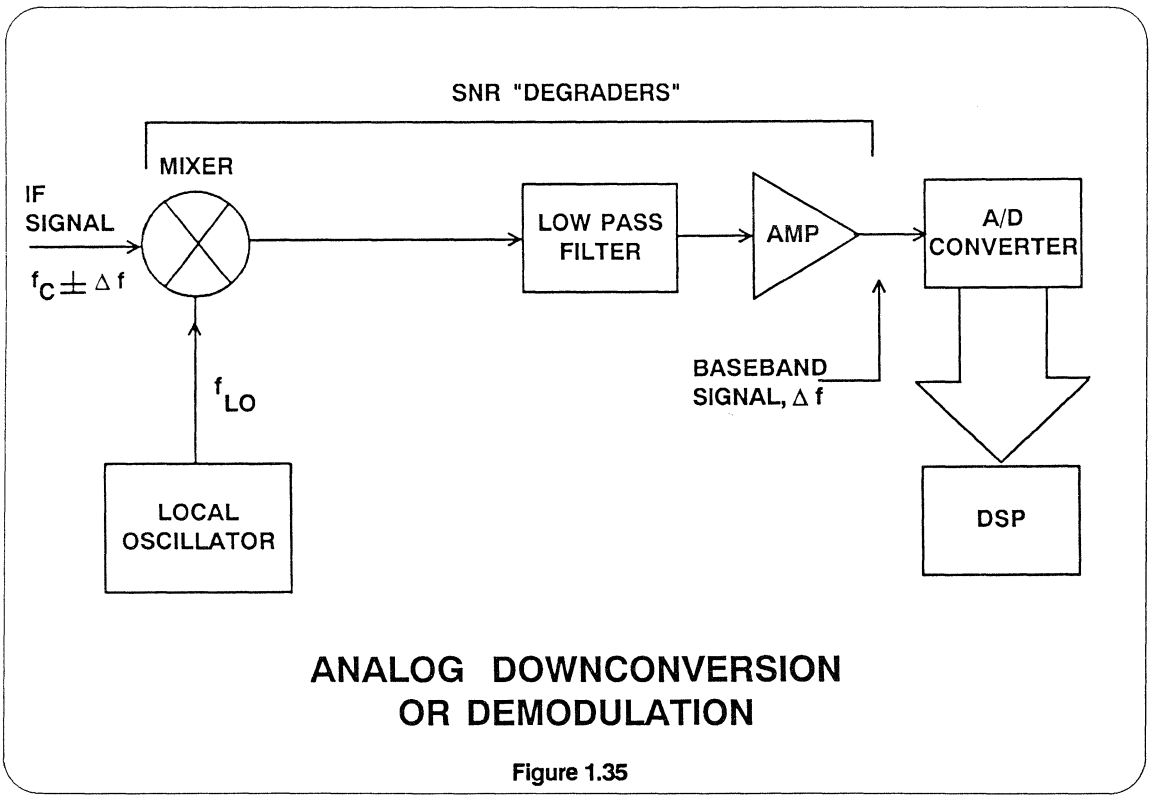
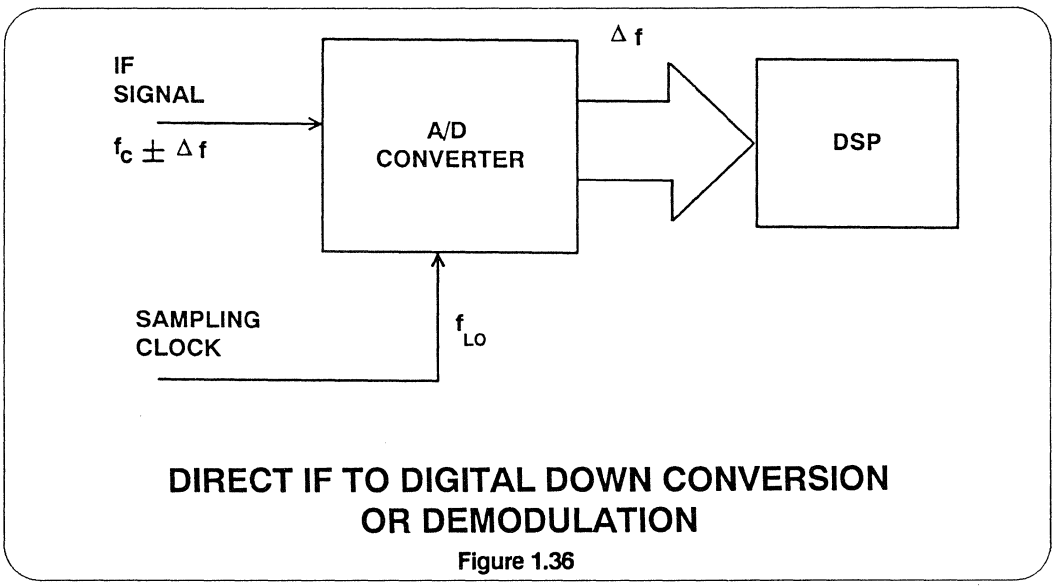


Figure 1.35

Typical mixers have a conversion loss ranging from 4 to 6dB. In cases when the signal-to-noise ratio is limited by the front end, elimination of the mixer will improve the overall noise figure of the receiver. This can be accomplished (as shown in Figure 1.36) if the IF signal is sampled at a rate which is equal to the local oscillator frequency. The A/D converter now looks like a demodulator. If the A/D converter samples an analog signal of the same frequency as the sampling frequency, the digitized output is a DC value. Any deviation in the analog signal from the sampling frequency looks like a "beat" frequency, and the demodulation process is thereby achieved.

The data from the A/D converter must be processed using an FFT which computes both the real and imaginary components of the digitized signal. This is necessary in order to preserve the phase information contained in the demodulated signal. The total bandwidth of the signal to be demodulated must be less than $f_s/2$ in order not to violate the Nyquist criterion.

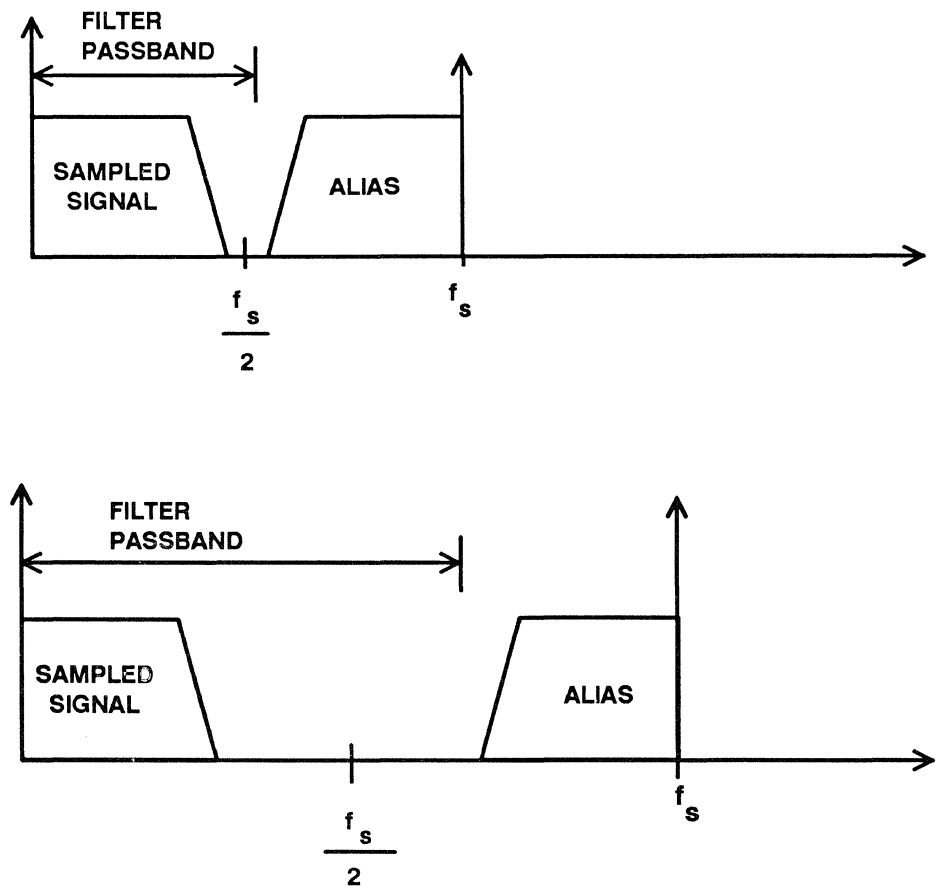


DIRECT IF TO DIGITAL DOWN CONVERSION OR DEMODULATION

Figure 1.36

OVERSAMPLING APPLICATIONS

The technique of sampling a signal at greater than twice its maximum frequency (called "oversampling") has several advantages in A/D converter applications. Increasing the sampling rate beyond the Nyquist rate $f_s/2$ makes the design of the anti-aliasing filter preceding the A/D converter much easier, as shown in Figure 1.37.



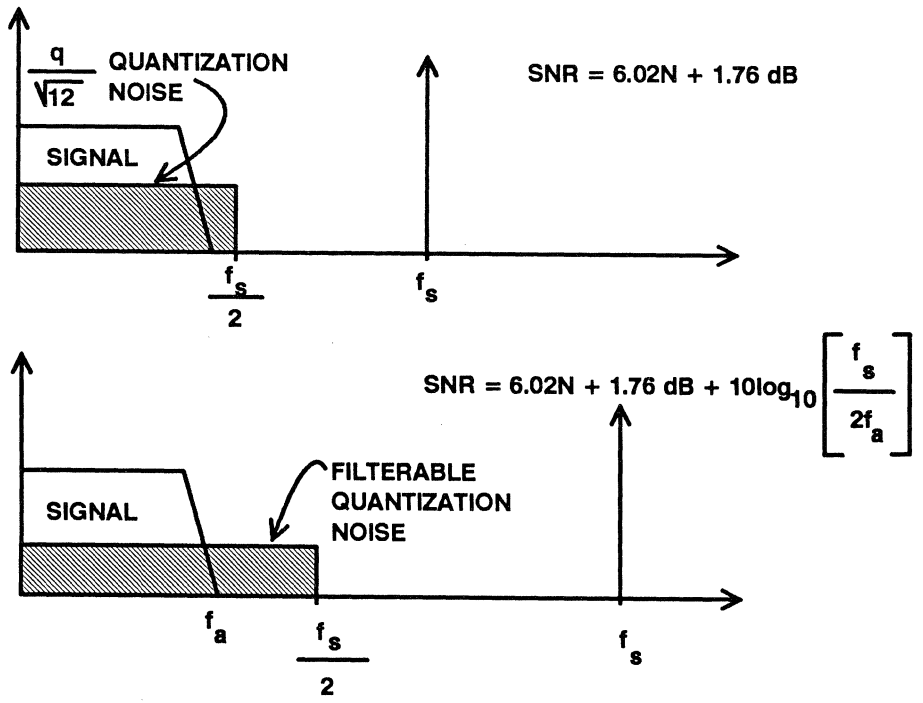
EFFECT OF OVERSAMPLING ON FILTER REQUIREMENTS

Figure 1.37

Also, the effective SNR can be improved by oversampling, as shown in Figure 1.38. For a given sampling rate f_s, the theoretical RMS quantization noise in the bandwidth $f_s/2$ is given by $q/\sqrt{12}$, where q is the weight of the least significant bit. (See derivation given in Reference 15.) From this, the theoretical formula for the SNR of an N-bit A/D converter (SNR = 6.02N + 1.76dB) can be easily derived. If the signal bandwidth f_a is held constant, and the sampling rate is increased, the effect is to "spread" the quantization noise over a wider bandwidth, thereby reducing the RMS noise in the analog bandwidth, f_a. The exact expression for the fullscale sinewave SNR under these conditions is given by

$$\mathbf{SNR = 6.02N + 1.76dB + 10log_{10}\left[\frac{f_s}{2f_a}\right]}$$

where f_s is the sampling rate and f_a is the analog bandwidth of interest. It can be seen that doubling the sampling rate for a constant analog bandwidth has the effect of increasing the SNR by 3dB or increasing the ENOBs by 1/2 bit. Digital post processing of the quantized data in conjunction with a digital lowpass filter of bandwidth f_a is usually used to obtain this improvement. The noise power in the bandwidth f_a to $f_s/2$ is removed by the digital filter. See pp. 15-22 of the February 1988 **Hewlett-Packard Journal** for further discussion of this topic.

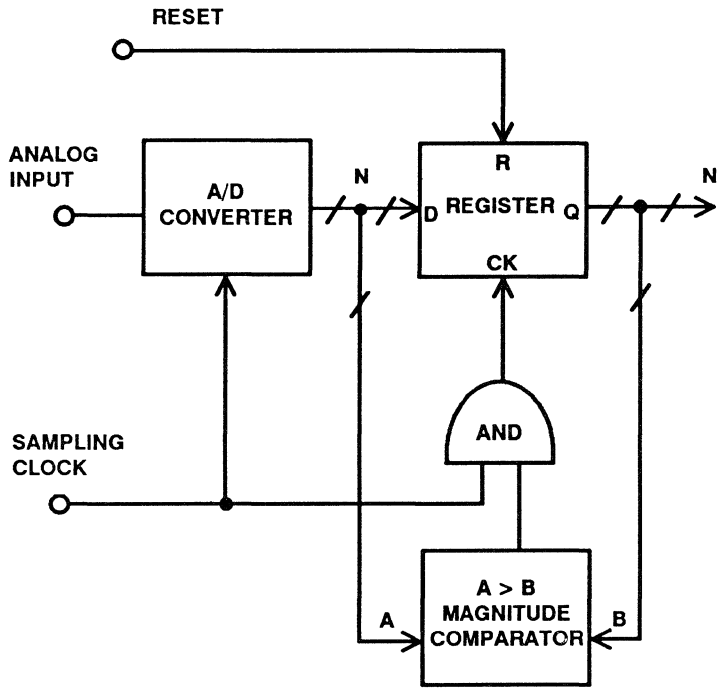


EFFECT OF OVERSAMPLING ON QUANTIZATION NOISE

Figure 1.38

Absolute Peak Detector

An absolute peak detector circuit is shown in Figure 1.39. A reset pulse is first applied to the register at the start of the time period. The A/D converter sampling clock is then initiated. The A/D converter output will only be clocked into the register if it is greater than the previous sample. In this way, the largest sample during the sampling window is always stored in the register. At the end of the period, the sampling clock is stopped, and the peak value is read. The sampling rate must be substantially higher than the analog input frequency in order to capture the peak of interest.



ABSOLUTE PEAK DETECTOR

Figure 1.39

APPLICATIONS OF DITHERING

The assumption of a random quantization error signal which is independent of input signal allows an easy derivation of the familiar expression $q/\sqrt{12}$ (q=1LSB) for the RMS quantization noise (within the Nyquist bandwidth) of an ideal A/D converter. For a sinusoidal input, however, the A/D converter output error is actually composed of a large number of harmonics of the input frequency. These harmonics (regardless of frequency) all appear within the Nyquist bandwidth (due to aliasing produced by the sampling process). If the power of all these harmonics is summed, the RMS quantization power is accurately given by $q/\sqrt{12}$.

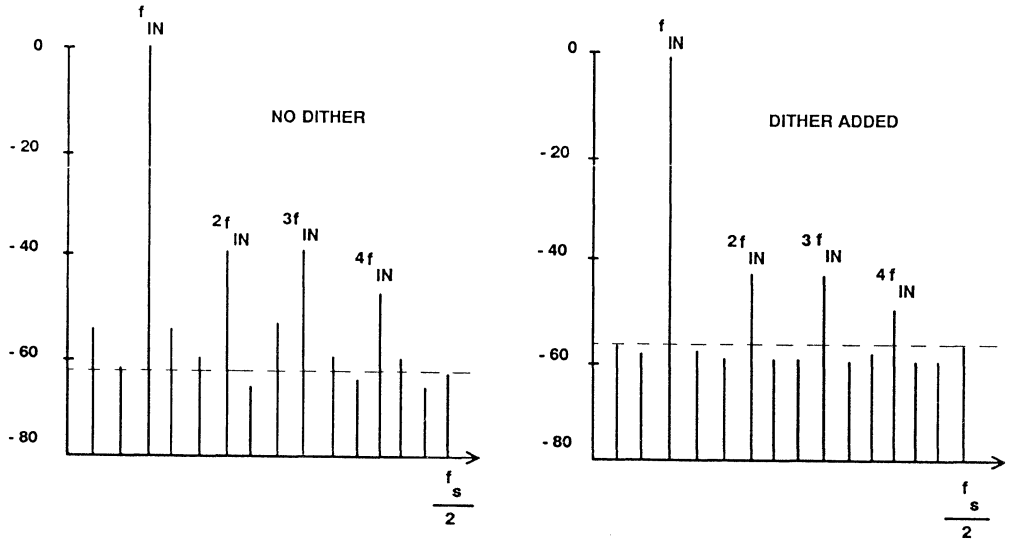
Since the error waveform produced by the quantization of a periodic waveform is itself periodic, and appears as harmonic distortion of tones present at the A/D converter input, this situation is highly undesirable in spectral analysis applications. In receiver application especially, it is more desirable to have the quantization noise power spread uniformly over the Nyquist bandwidth rather than concentrated in a discrete set of spectral lines. Also, the harmonics present in the error waveform are coherently related to the A/D input waveform. This further complicates the task of processing the signal spectrum to differentiate between signals and system-induced spurious components, especially when "searching" the spectrum for the presence of low-level signals in the presence of large signals.

If random noise which has a flat spectrum over the Nyquist bandwidth (dither) is added to the A/D input signal, the effect is to randomize the quantization noise, provided the random noise voltage is at least $q/\sqrt{12}$. Obviously, this has the effect of degrading the overall SNR by 3dB, but also has the effect of destroying any statistical correlation between sample errors. The composite noise spectrum at the A/D converter output is thus made flat over the Nyquist bandwidth. The actual noise level which provides optimum performance is very A/D and application dependent, but typically is chosen to be several dB greater than $q/\sqrt{12}$. The effects of adding noise to a digitized sinewave is shown in Figure 1.40. The process of adding random noise to the input signal is referred to as *dithering*.

In a receiver application, the front-end gain can be adjusted so that the actual receiver noise present at the A/D input is at the correct level to randomize the quantization error as shown in Figure 1.41.

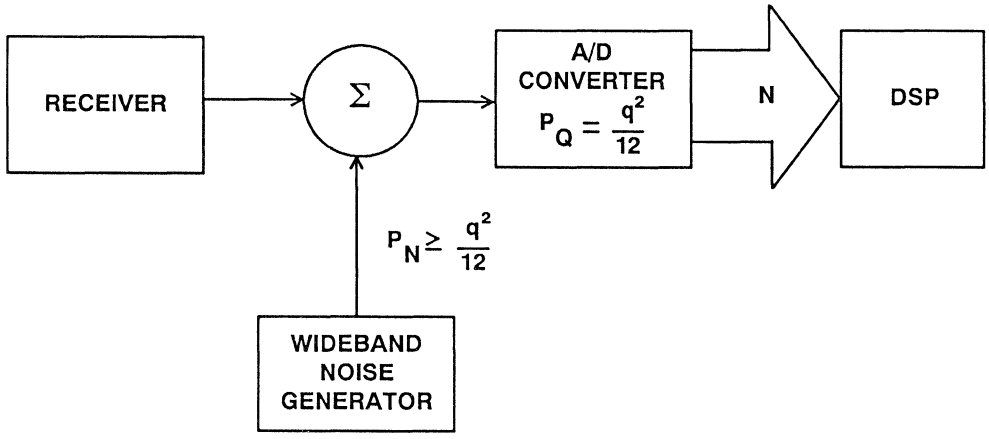
It should also be remembered that dither can be introduced into the system by phase jitter on either the sampling clock or the input sinewave. Either of these will have the effect of increasing the overall noise floor. See the section on Aperture Jitter for further discussion.

Sophisticated dithering signals (other than random noise) have been used in conjunction with digital filtering and processing to achieve improvements in A/D converter performance without degrading SNR performance. This is accomplished by adding the appropriate dither signal to the A/D input and then subtracting it from the A/D output. A detailed discussion of this technique is given on pp. 70-76 in the June 1988 **Hewlett-Packard Journal.**



EFFECTS OF DITHER ON FFT SPECTRAL RESPONSE

Figure 1.40

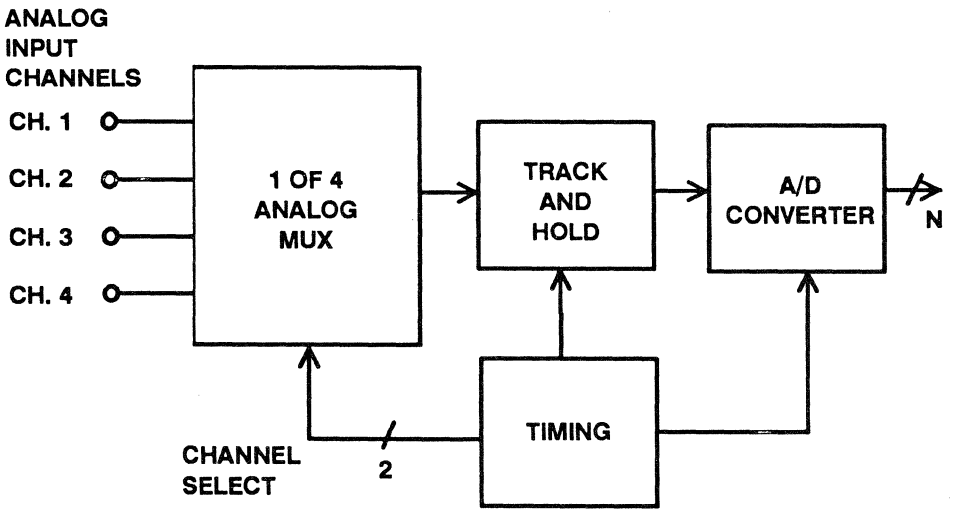


ADDING NOISE TO RECEIVER FOR INCREASED SPECTRAL RESOLUTION

Figure 1.41

MULTIPLEXING APPLICATIONS

Multiplexing many channels of analog data into a single A/D converter is quite common in low-speed data acquisition systems, and a classical block diagram is shown in Figure 1.42. A variation on this scheme, called "simultaneous sampling" is shown in Figure 1.43, where track-and-hold amplifiers are kept in the "hold" mode long enough for the multiplexer to sequence each channel into the A/D converter. These schemes have proven to offer a cost-effective solution to low speed multi-channel digitization, primarily because only one A/D converter (usually the most expensive part) is required.



TRADITIONAL DATA ACQUISITION SYSTEM USING ANALOG MULTIPLEXER

Figure 1.42

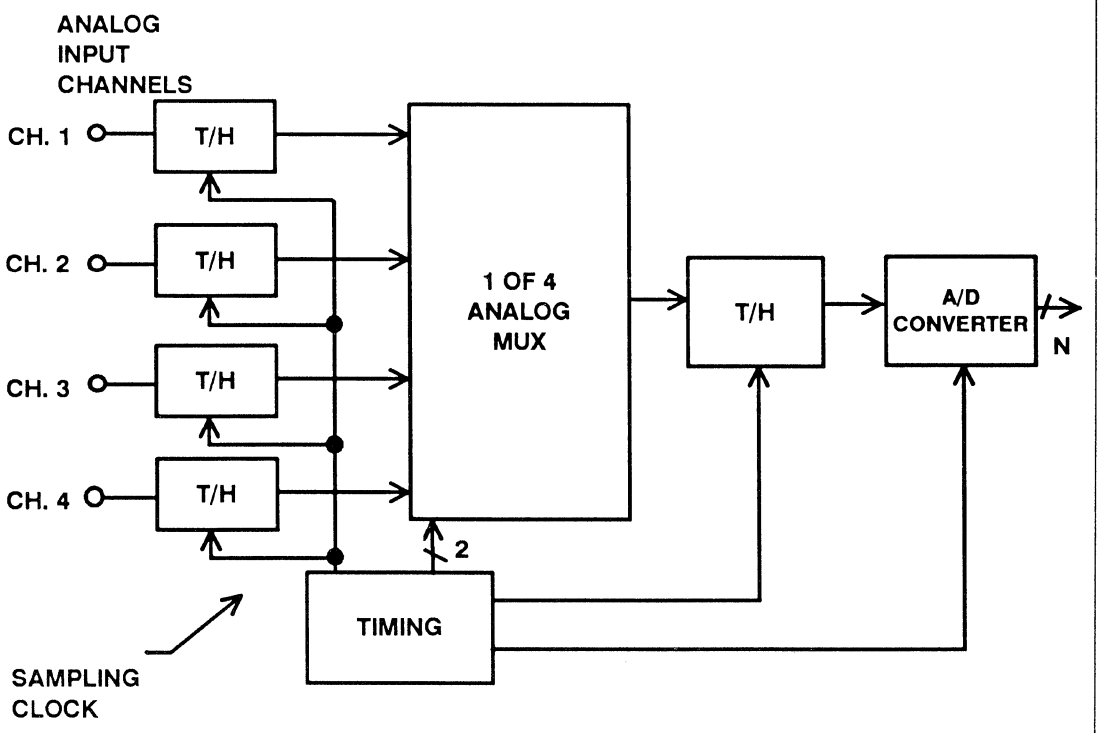


Figure 1.43

With the advent of high-speed A/D converters and faster analog multiplexer/switches, it is tempting to apply the same architecture to high-speed data acquisition systems. The user should be aware of several potential problems associated with using this approach at video speeds.

- There is no way to guarantee the per-channel dynamic performance (SNR, ENOB, etc.) based on the individual component specifications alone.
- Multiplexer settling time and A/D converter transient response become critical specifications. Remember that the multiplexer output can present a fullscale sample-to-sample change to the A/D converter analog input. If the multiplexer and A/D converters have not both settled to the required accuracy, DC channel-to-channel "crosstalk" will result.
- AC crosstalk between channels is much more of a problem when digitizing video speed signals.

In summary, the use of A/D converters on a per-channel basis is definitely the preferred solution for multichannel data acquisition systems at video speeds.

BEWARE OF ANALOG MULTIPLEXING AT VIDEO SPEEDS

- Individual Component Specs Don't Determine System Dynamic Performance
- Multiplexer Settling Time
- A/D Converter Transient Response
- DC Crosstalk Between Channels
- AC Crosstalk Between Channels

Figure 1.44

A/D CONVERTER DYNAMIC SPECIFICATIONS AND TESTING

- DSP Testing
- Quantization Theory
- DFTs and FFTs
- Signal to Noise Ratio
- Harmonic Distortion
- Two Tone Intermodulation Distortion
- Spurious Free Dynamic Range
- Coherent Sampling
- Non-Coherent Sampling
- Windowing
- Sinewave Curve Fit
- Beat Frequency Tests
- Histogram Tests
- Noise Power Ratio
- Transient Response
- Overvoltage Recovery
- Aperture Time
- Composite Video Tests
- Error Rates

DSP TESTING OF A/D CONVERTERS

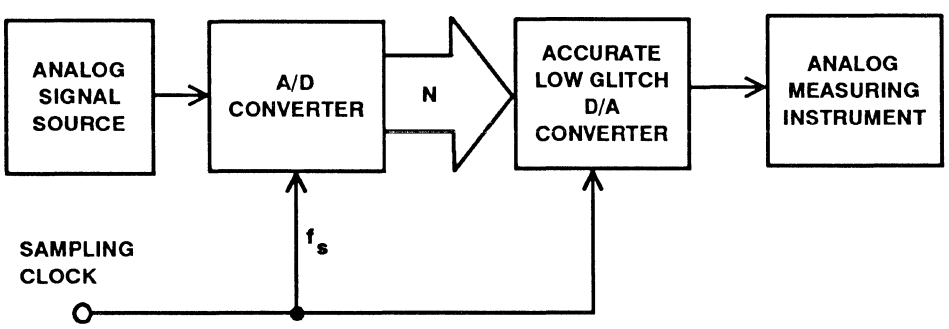
With the advent of "sampling" A/D converters, much emphasis has been placed on the dynamic performance of the converter when digitizing rapidly changing signals. The particular dynamic specifications of interest may very widely with the application as shown in Figure 1.45.

ANALOG-TO-DIGITAL DYNAMIC SPECIFICATIONS VS. APPLICATIONS

SPECIFICATION	APPLICATION
Effective number of bits (ENOB)	All
Signal-to-noise ratio (SNR)	Radar, communications, spectrum analysis
AC linearity	Radar, spectrum analysis
Noise power ratio (NPR)	Communications
Two-tone intermod distortion	Radar, spectrum analysis
Transient response	Transient analysis, radar, multiplexing
Overvoltage recovery	Radar
Aperture jitter	All
Differential gain and phase	Television
Error Rate	Radar, transient analysis, communications
Spurious free dynamic range (SFDR)	Communication receivers, spectrum analysis

Figure 1.45

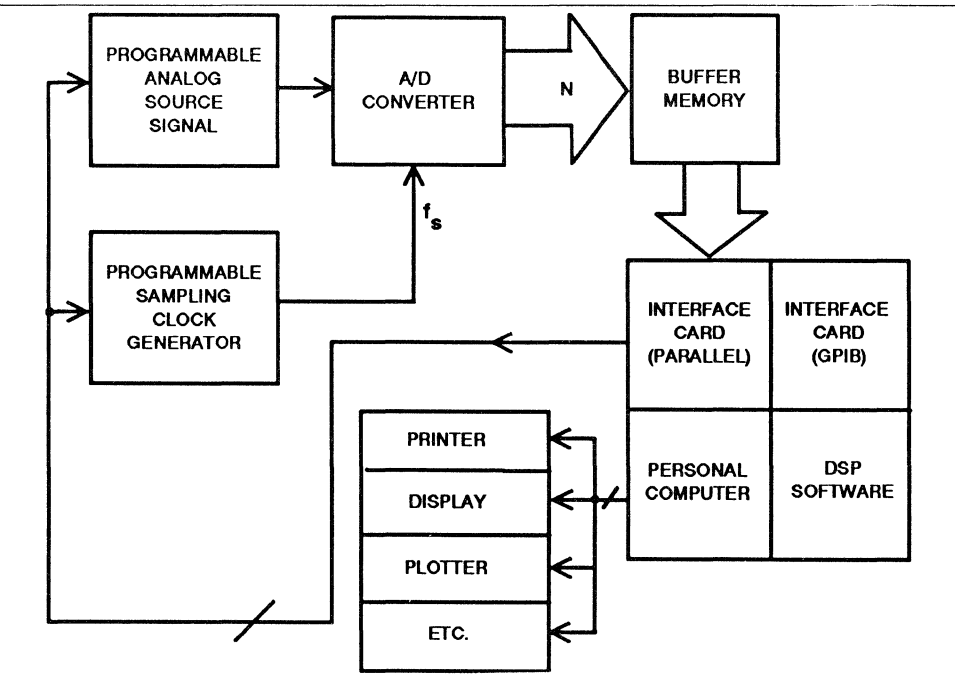
In the early days of video speed A/D converters, most dynamic testing was done in the analog realm using a high performance D/A converter to reconstruct the output of the A/D converter, as shown in Figure 1.46.



DYNAMIC A/D CONVERTER TESTING - THE OLD WAY

Figure 1.46

Today, it is possible to perform sophisticated DSP tests (such as FFTs, AC histograms, etc.), using test systems based upon user-friendly personal computers and standard software packages. The PC-based test system shown in Figure 1.47 is capable of performing a 1024-point FFT in less than one second.



A/D CONVERTER DSP TEST SYSTEM

Figure 1.47

Some key features of this system are shown in Figure 1.48. Specialized A/D converter DSP test systems are currently being offered by large ATE manufacturers such as Teradyne and LTX. These systems are well suited to large volume IC production applications, but are too costly for the end user. Other less expensive benchtop systems are now available from companies such as Tektronix and Hewlett-Packard which allow the end user to implement DSP testing of A/D converters not only at low cost but with a minimum of hardware and software development effort.

Manufacturers of video speed A/D converters such as Analog Devices are supplying product-specific evaluation boards to allow customers to easily interface the A/D converter with their DSP test system. The evaluation boards contain reference voltages, power supply decoupling, timing circuits, output registers, connectors, etc., in order to make performance evaluations as easy as possible. In addition, the evaluation boards usually have a matching D/A converter which is useful in determining the overall functionality of the A/D converter.

PC-BASED TEST SYSTEM

Personal Computer:	AT&T PC-6300
Co-Processor:	8087
Storage:	20 MByte Hard Disk Drive
Interface Card:	Metrobyte PIO-12, 24-bit Parallel
Operating Software:	Microsoft "Quickbasic"
FFT Software:	Micro Way "87 FFT"

Figure 1.48

QUANTIZATION THEORY

The RMS noise voltage measured within the Nyquist bandwidth for an ideal A/D converter is given by the familiar expression $q/\sqrt{12}$, where q is the weight of the LSB. This value is also independent of input signal frequency and amplitude.

For a fullscale sinewave input, it can be shown that the theoretical RMS signal to quantification noise ratio is given by

$$SNR = 6.02N + 1.76dB + 10\log_{10}\left[\frac{f_s}{2f_a}\right]$$

where N = number of bits, f_s = sampling rate, and f_a = analog bandwidth. The third term in the above equation represents the increase in SNR due to oversampling, as previously discussed.
The classical deviation of these expressions can be found in the following reference:

W.R. Bennett, "Spectra of Quantized Signals"
BSTJ 27, pp. 446-472, July 1948.

Practical A/D converters exhibit errors which are due to static and dynamic nonlinearities. These dynamic errors increase as input slew-rates become greater. The actual SNR measurement will, therefore, be less than theoretical, and it is useful to calculate the effective number of bits (ENOB) by solving the above equation for N:

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB - 10\log_{10}\left[\frac{f_s}{2f_a}\right]}{6.02}$$

Note that when the "noise" is calculated using DFT techniques, it includes not only quantization noise but also the harmonics of the input sinewave. Harmonics which fall outside the Nyquist bandwidth are "aliased" back into the Nyquist bandwidth because of the sampling process.

Sinewaves are the most popular signals for evaluating A/D converter dynamic performance because of their ease of generation and mathematical analysis.

QUANTIZATION THEORY BASICS

- RMS Quantization Noise In Nyquist Bandwidth, $\frac{f_s}{2}$: $\frac{q}{\sqrt{12}}$

  q = LSB

- Fullscale Sinewave RMS Signal to RMS Noise in Bandwidth f_a:

  $$SNR = 6.02N + 1.76dB + 10\log_{10}\left[\frac{f_s}{2f_a}\right]$$

- Effective Number of Bits (ENOB):

  $$ENOB = \frac{SNR_{ACTUAL} - 1.76dB - 10_{log}\left[\frac{f_s}{2f_a}\right]}{6.02}$$

Figure 1.49

DISCRETE AND FAST FOURIER TRANSFORMS

The discrete fourier transform (DFT) in the digital domain is analagous to spectrum analysis in the analog domain. The DFT is a mathematical operation which is performed on a finite record of contiguous discrete time samples to produce an equivalent number of frequency samples. Both signal level, noise levels, and harmonic content can then be calculated from the DFT output. The fast fourier transform (FFT) is simply an algorithm which is used to greatly reduce the number of mathematical calculations (and thereby the processing time) required to obtain the DFT output spectrum. An excellent in-depth treatment of DFT and FFT theory can be found in any number of references, particularly

The FFT: Fundamentals and Concepts
Robert W. Ramirez, Prentice Hall, 1985.

Calculating the DFT

To calculate the DFT, a spectrally pure sinewave is applied to A/D converter, and a number of contiguous samples are stored in a buffer memory.
Unless the record time contains an integer number of cycles of the sinewave, time-weighting of the samples is required to reduce frequency sidelobes. Without weighting, the discontinuity produced by not having an integer number of cycles will cause the main lobe energy to "leak" into many other frequency bins making accurate spectral measurements impossible. A popular weighting function is called the "Hanning" function and is given by

$$W_nD_n = D_n \left[0.5 - 0.5\cos\left(\frac{2\pi n}{M}\right)\right]$$

where W_nD_n is the nth weighted data sample, D_n is the nth input data sample, and M is the total number of samples.

By using this weighting function, the leakage energy can be compressed into a small band of frequencies centered on the fundamental sinewave frequency. This eliminates contamination of a large portion of the overall spectrum.

Next the program must find the DFT of the sequence of weighted data samples for M/2 frequencies. To do that, the program must solve the following two equations for the Kth frequency:

$$A_K = \frac{1}{M}\sum_{n=1}^{M} W_nD_n\cos\left[\frac{2\pi k(n-1)}{M}\right]$$

$$B_K = \frac{1}{M}\sum_{n=1}^{M} W_nD_n\sin\left[\frac{2\pi k(n-1)}{M}\right]$$

where A_k and B_k represent the magnitudes of the cosine and sine parts of the Kth spectral line. The total magnitude of the Kth spectral line is then expressed by the equation:

$$MAG_K = \sqrt{A_K^2 + B_K^2}\ .$$

The results yield M/2 components which are the frequency domain representation of the M time samples. The resolution or spacing between the spectral lines is given by the equation

$$\Delta f = \frac{f_s}{M}$$

where f_s is the sampling rate, and M is the total record length. The value, Δf, is often referred to as the "bin" size.

CALCULATING THE SIGNAL-TO-NOISE RATIO FROM THE FFT OUTPUT

Unless the sinewave frequency is chosen such that the record length M contains an integer number of cycles of the sinewave, the signal energy will be contained in several bins located around the fundamental. The RMS energy contained in the fundamental sinewave is computed by taking the square root of the sum of the squares of the appropriate number of samples (including the peak) located on either side of the peak. The number of samples to be included in this calculation can be determined by knowing the resolution of the A/D converter and the sidelobe roll-off characteristics of the particular weighting function being used.

The RMS energy in the remaining frequency bins represents the noise due to theoretical quantization, A/D harmonic distortion and excess noise, and FFT round-off error. This energy is calculated by taking the square root of the sum of the squares of the remaining samples (excluding the DC component).

The overall A/D converter SNR is then calculated by:

$$SNR = 20\log_{10}\left[\frac{\text{RMS SIGNAL LEVEL}}{\text{RMS NOISE LEVEL}}\right]$$

DFT FLOWCHART

- Determine Record Length, M
- Collect M Time Domain Samples at the Sampling Rate, f_S
- Multiply Each Time Sample by Appropriate Weighting or Windowing Function for Non-Coherent Sampling
- Calculate M/2 Spectral Magnitudes using DFT (FFT)
  Spacing Between Spectral Lines is $\Delta f = \frac{f_S}{M}$
- Analyze Frequency Spectrum
- Calculate RMS Signal Level
- Calculate RMS Noise Level, Neglecting DC Component
- Calculate RMS Harmonic Levels
- Calculate SNR, ENOB, Harmonic Distortion, THD, Etc.

Figure 1.50

CALCULATING HARMONIC DISTORTION FROM THE FFT OUTPUT

Harmonic distortion is calculated in a similar manner. The program "searches" the FFT frequency spectrum for the proper location of the desired harmonic (bearing in mind that harmonics above $f_s/2$ will be aliased into the baseband) and calculates the RMS energy in the harmonic. The RMS signal to RMS harmonic ratio is calculated as follows:

$$\text{HARMONIC DISTORTION} = 20\log_{10}\left[\frac{\text{RMS SIGNAL LEVEL}}{\text{RMS HARMONIC LEVEL}}\right].$$

Total harmonic distortion (THD) is often calculated by root-sum-squaring the first five harmonics of the fundamental sinewave and using the resulting number in the above formula for the RMS harmonic level.

TWO-TONE INTERMODULATION TESTS USING FFTs

It is often useful to measure the third-order intermodulation products for two sinewaves of frequency f_1 and f_2 which are applied to an A/D converter (see Figure 1.51).

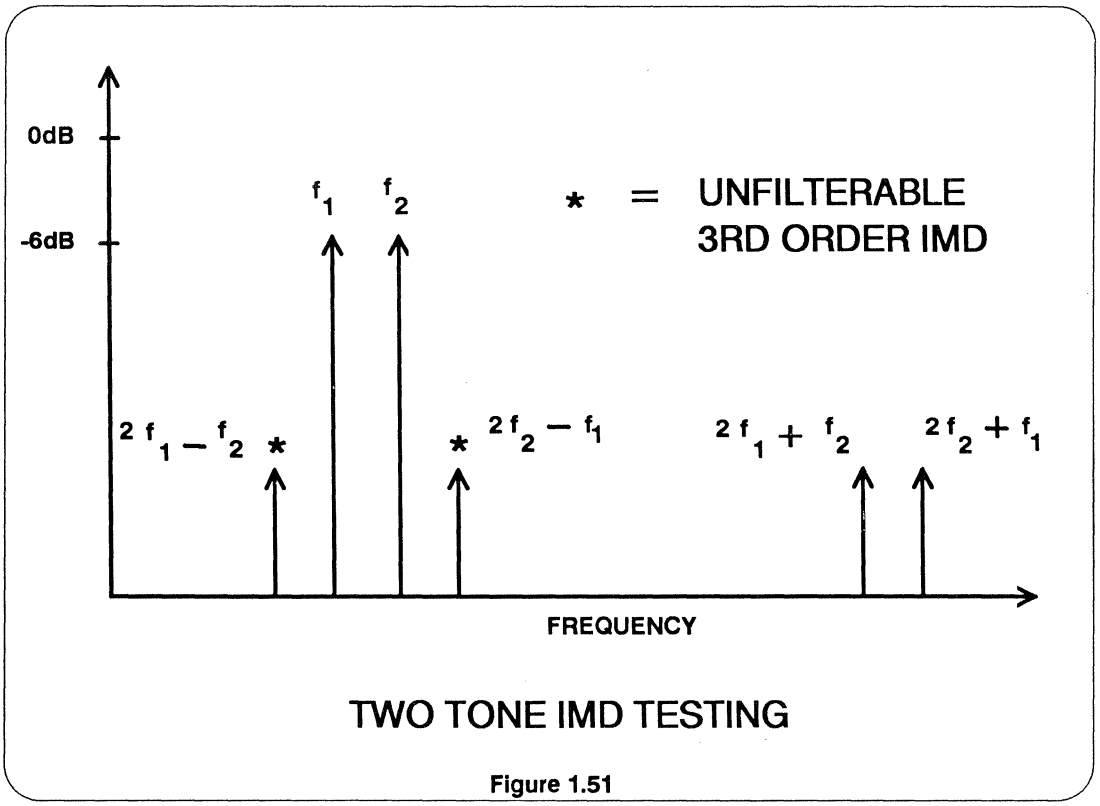


Figure 1.51

These products occur at frequencies:

$2f_1 + f_2$ $\quad$ $2f_2 + f_1$
$2f_1 - f_2$ $\quad$ $2f_2 - f_1$

Most IMD can be filtered out. However, if the two tones are of similar frequencies, the third order IMD ($2f_1$-f_2, $2f_2$-f_1) will be very close to the fundamental frequencies and cannot be easily filtered. The level of these products is of most concern in narrow bandwidth applications.

The amplitudes of the individual tones should be at least 6dB below the fullscale of the A/D converter to avoid distortion due to clipping.

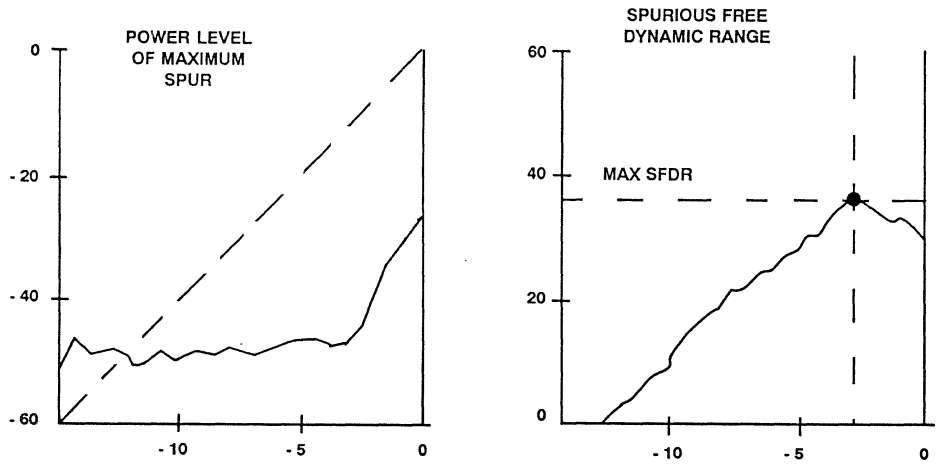
The frequency separation of the two tones should be consistent with the resolution of the FFT. As previously discussed, the spectral resolution of the FFT is a function of record length, M, coherence vs. non-coherence, and the properties of the particular windowing function chosen.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

In receiver applications, it is often desired to know the maximum ratio achievable between the amplitude of a single tone input signal and the amplitude of its maximum spur.

For an ideal A/D converter, this would occur for a fullscale input sinusoid. In a practical A/D, however, spurious content is a function of slew-rate and, therefore, the maximum spurious free dynamic range (SFDR) for a given input frequency usually occurs at a level somewhat below fullscale.

Figure 1.52 shows a typical plot of the maximum spur level vs. input power level.



SPURIOUS FREE DYNAMIC RANGE (SFDR)

Figure 1.52

This corresponding spurious free dynamic range plot is also shown in Figure 1.52. This plot shows that the maximum SFDR occurs for an input signal which is approximately 3dB below fullscale.

The SFDR is slew-rate dependent, and, therefore, a function of the input frequency as well as the amplitude.

The data needed to generate these plots is readily available from the family of FFTs calculated for the different input amplitudes.

By knowing the input signal level that gives the highest SFDR at frequencies close to Nyquist, the gain of the system can be set to take maximum advantage of the A/D converter's spectral characteristics.

Determining The Proper FFT Record Length

The first consideration in choosing the number of time-domain samples required or record length, N, is the required spectral resolution, Δf. Also, in order to perform the FFT computations, N must be equal to an integer which is a power of two. The FFT spectral resolution, Δf, is given by

$$\Delta f = f_s/M$$

where f_s is the sampling rate. This can also be expressed as

$$\Delta f = \frac{1}{M \cdot \Delta t},$$

where Δt is the sampling period, $1/f_s$.

Typically, M is selected to be between 256 and 4096 depending upon the desired resolution and the amount of buffer memory available. (See section on the selection of a windowing function for further discussion on the effects of windowing on spectral leakage).

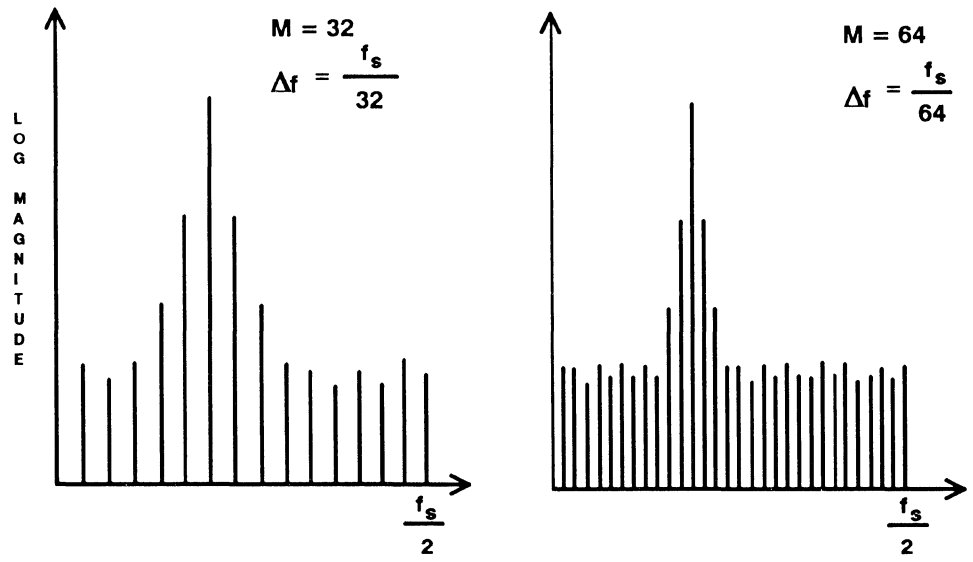
If windowing is used, the main lobe width and sidelobe rolloff (leakage) are measured in units of "bin width", f_s/M. This leakage can be "compressed" around the main lobe by using a larger record length, M, thereby leaving a larger percentage of the Nyquist spectrum uncontaminated, as shown in Figure 1.53.

For example, the Hanning weighting leakage is 10 bins around the fundamental for 68dB sidelobe suppression. If the record length is 256, then the smeared fundamental occupies 20/128, or 16% of the Nyquist bandwidth. For M = 1024, the percentage reduces to 20/512, or 4%.

Another consideration in determining the proper record length is the FFT noise floor itself. Assuming the DSP noise contribution (due to roundoff error) is negligible, the RMS signal to RMS noise level in a single frequency bin of width Δf is given by the expression

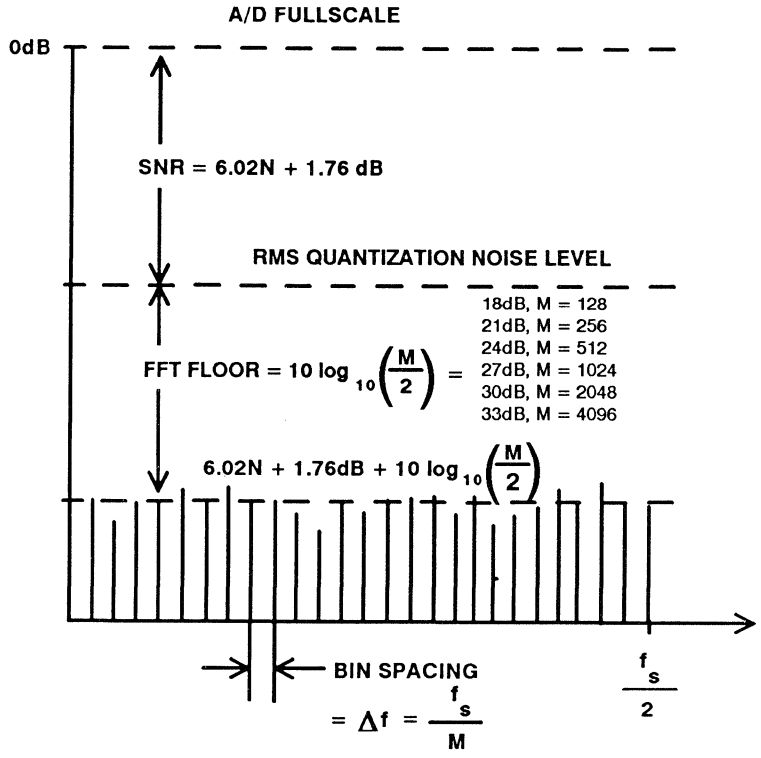
$$SNR_{FFT} = 6.02N + 1.76dB + 10\log_{10}\left(\frac{M}{2}\right)$$

This represents the FFT noise floor. The value should be chosen such that any spurious components which need to be resolved lie at least 10dB above this floor. This is illustrated in Figure 1.54.



EFFECT OF RECORD LENGTH ON LEAKAGE

Figure 1.53



FFT THEORETICAL NOISE FLOOR

Figure 1.54

DETERMINING FFT RECORD LENGTH

- Frequency Resolution

$$\Delta f = \frac{f_s}{M} = \text{"Bin Width"} = \frac{1}{M\,\Delta t}$$

- Effects of Weighting
- FFT Noise Floor

Figure 1.55

DETERMINING SINEWAVE INPUT FREQUENCY FOR COHERENT SAMPLING

As has been previously discussed, the use of coherent sampling eliminates leakage and the requirement for windowing. There are, however, some requirements placed on the choice of the sampling rate and the sinewave frequency.

First, the following ratio must be observed:

$$\frac{f_{IN}}{f_S} = \frac{M_C}{M} \quad \text{where}$$

M_C = Number of integer cycles of the sinewave during the record period.

M = Number of samples in record period.

f_{IN} = Input sinewave frequency.

f_S = Sampling rate.

For a whole number of cycles, M_C must be an integer. For non-repetitive data M_C should also be odd and prime - i.e., 1, 3, 5, 7, 11, 13, 17, etc. This insures that all samples during the record period will be unique.

When using coherent sampling, the ratio must be constant! This implies that the frequencies f_s and f_{in} be derived from sources that are locked to each other, such as two locked frequency synthesizers.

REQUIREMENTS FOR COHERENT SAMPLING

f_s = Sampling Rate

f_{IN} = Input Sinewave Frequency

M = Number of Samples in Record, Integer Power of 2

M_c = Number of Cycles of Sinewave During Record Period

$$\frac{f_{IN}}{f_s} = \frac{M_c}{M}$$

M_c:

- Integer, No Weighting Needed
- Odd
- Prime

> All Samples Unique

- 1, 3, 5, 7, 11, 13, 17, 19, 23, etc.

Figure 1.56

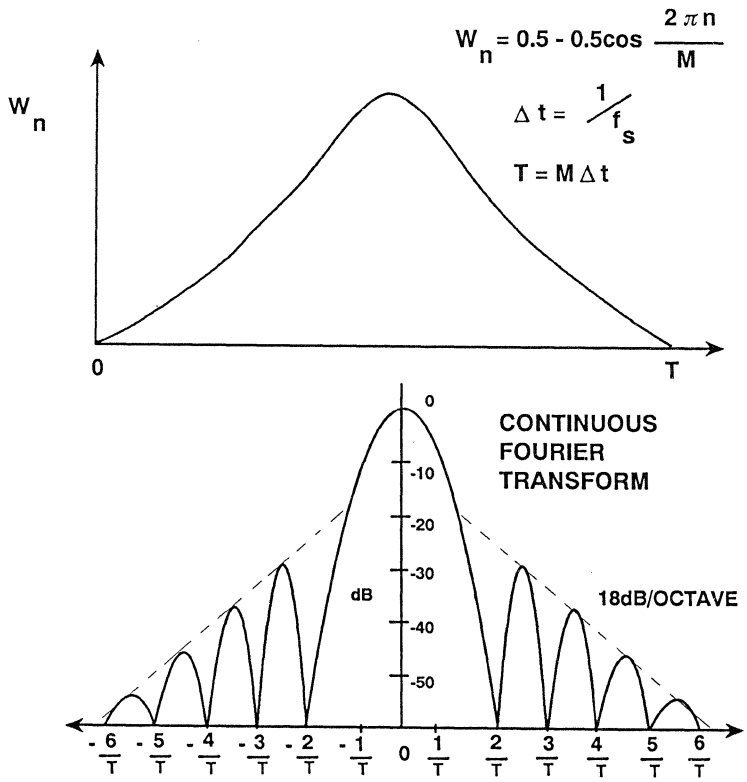
CHOOSING THE WINDOWING FUNCTION FOR NON-COHERENT SAMPLING

If non-coherent sampling is chosen, fewer restrictions apply to the selection of the input frequency. However, integer submultiples of the sampling frequency should be avoided to prevent masking out harmonics of the fundamental. It is also desirable to make the input frequency an odd multiple of the FFT frequency bin size to ensure this condition does not occur.

The selection of the weighting function is primarily a tradeoff between main-lobe spreading and sidelobe rolloff. The following reference is highly recommended for an in-depth look at windows:

> Fredric J. Harris, "On The Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," IEEE Proceedings, Vol. 66, No. 1, Jan. 1978, pp. 51-83.

The effects of "windowing" a sinewave are shown in Figure 1.57 for the popular "Hanning" window.



TIME AND FREQUENCY REPRESENTATION OF HANNING WINDOW

Figure 1.57

This window has the following characteristics:

- Highest Sidelobe Level: 32dB below fundamental
- 6dB point of main lobe: 2 bins wide
- Location of highest sidelobe: 2.5 "bins" from fundamental (recall that the width of a "bin" = f_s /M).

  Sidelobe envelope rolloff: 18dB per octave, i.e., at 5 bins from the fundamental, the sidelobe envelope will be down 32 + 18 = 50dB from the fundamental.
- The following table is useful in determining the number of samples to be included in calculating the energy in the fundamental:

BINS FROM FUNDAMENTAL	SIDELOBE ATTENUATION
2.5	32dB
5.0	50dB
10.0	68dB
20.0	86dB

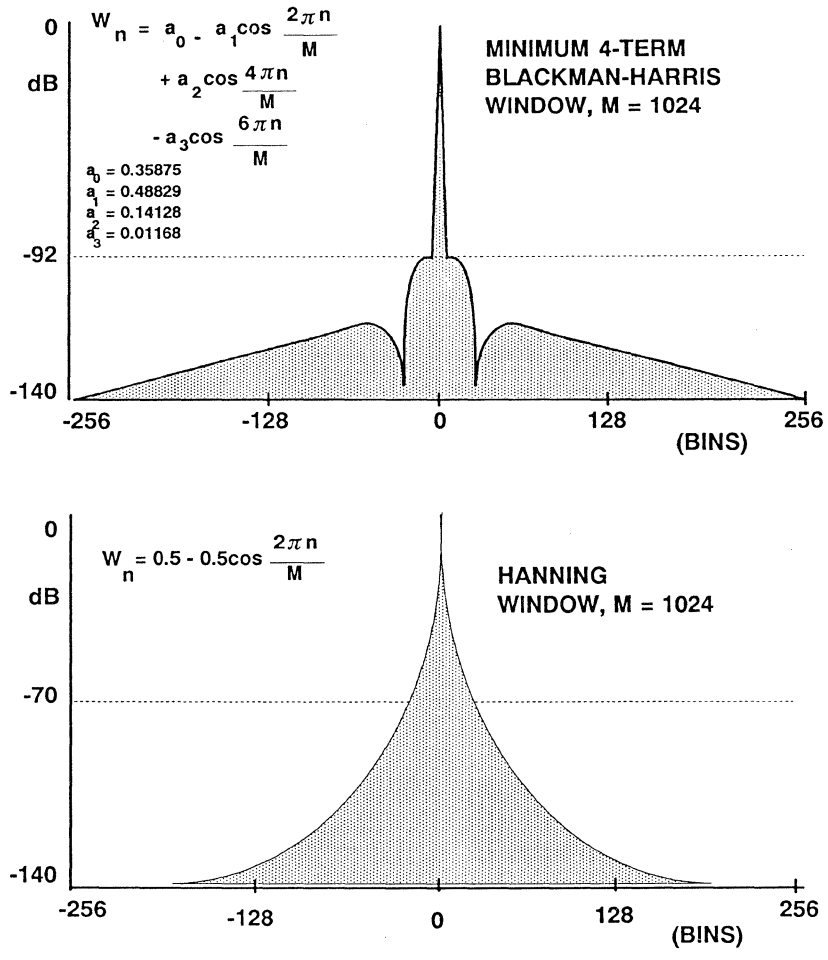
For a 12-bit A/D converter with a theoretical SNR of 74dB, it would, therefore, be appropriate to include 20 samples on either side of the fundamental in calculating the RMS signal energy (if Hanning weighting was used). It would also be appropriate to use a record length, M, of at least 1024 samples in order to achieve reasonable spectral resolution for harmonic analysis.

In order to make efficient use of the FFT processor, the weighting function coefficients should be calculated one time then stored in a lookup table. In this manner, more complex weighting functions can be used without any sacrifice in FFT processing speed.

If better spectral resolution is required, the minimum 4-term Blackman-Harris function is recommended. Figure 1.58 shows a spectral plot of this function and the Hanning function for reference (M = 1024). The equation for the minimum 4-term Blackman-Harris window is given by:

$$Wn = a_0 - a_1\cos\left(\frac{2\pi \cdot n}{M}\right) + a_2\cos\left(\frac{2\pi \cdot 2n}{M}\right) - a_3\cos\left(\frac{2\pi \cdot 3n}{M}\right)$$

where $a_0 = 0.35875$; $a_1 = 0.48829$; $a_2 = 0.14128$; $a_3 = 0.01168$



COMPARISON OF WEIGHTING FUNCTIONS

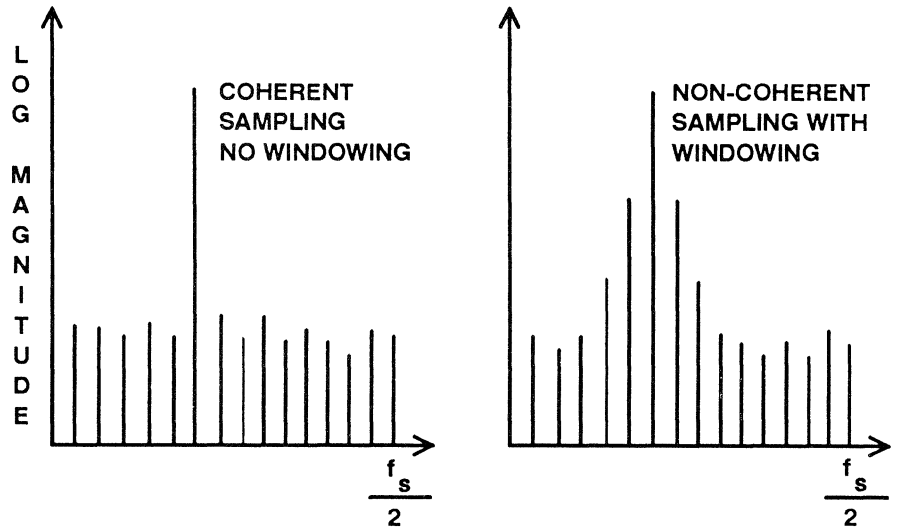
Figure 1.58

COHERENT VS. NON-COHERENT SAMPLING

The primary application of coherent sampling using FFTs is in the testing of A/D converters using sinewave inputs. If the proper ratios between f_{in} and f_s are observed, the need for windowing is eliminated, as previously discussed. This greatly increases the spectral resolution of the FFT and creates an ideal environment for critically evaluating the spectral response of the A/D converter. Great care must be taken, however, to insure the spectral purity and phase stability of f_{in} and f_s. The choice of the frequencies and their proper ratio is somewhat tedious, and high quality frequency synthesizers are needed (sometimes with additional filtering) in order to generate the phase locked signals.

In practical A/D converter applications, the precise frequency content of the signal being digitized is not usually known. If the A/D converter is being used in a spectral analysis application (as opposed to a transient recorder, for instance), a windowing function is required to process the signal, and the end user may be interested in the performance of the A/D using an identical or similar window.

In summary, both methods can be used effectively to evaluate the A/D converter performance if the proper ground rules are observed. Coherent sampling requires careful attention in the selection of the frequencies while non-coherent sampling requires careful attention and use of the windowing function. In either case, the purity of the sampling clock and the input sinewave are critical in order to achieve accurate and repeatable results. Coherent testing is more suited to a laboratory environment, while non-coherent testing is a better representation of the A/D converter performance in a "real world" application.



COHERENT VS. NON-COHERENT SPECTRUM

Figure 1.59

COHERENT SAMPLING	NON-COHERENT
• Increased Spectral Resolution, Repeatability	• Windowing Required
• Careful Selection of Frequencies, Ratio	• Real World Environment
• Phase/Frequency/Ratio Stability	
• Lab/Test Environment	

Figure 1.60

Verifying The FFT Accuracy

After selecting the record length, determining the weighting function (for non-coherent sampling), and writing the FFT program, the user should verify the overall accuracy of the program by inputting an ideal "N" bit sinewave. The SNR should be 6.02N + 1.76dB, and the spurious spectral components should be at least 10dB below those expected from the A/D converter. The ideal N-bit sinewave can be easily generated in BASIC software by using the INTEGER (INT) function to truncate the value to the proper resolution.

For instance, if the input signal whose frequency is f_{in} is given by

$$v(n) = V_O \sin\left(\frac{2\pi n f_{in}}{f_s}\right)$$

where n is the nth time sample for an ideal A/D with infinite resolution, then the corresponding quantized value can be calculated from

$$v_q(n) = \text{INT}\left[\frac{V_O \sin\left(\frac{2\pi n f_{in}}{f_s}\right)}{q}\right]$$

where $q = \frac{2V_O}{2^N}$

Substituting

$$v_q(n) = \text{INT}\left[2^{N-1} \cdot \sin\left(\frac{2\pi n f_{in}}{f_s}\right)\right]$$

The "INT" function simply truncates the fractional portion of v(n).

The overall dynamic range of the FFT can be checked by calculating the SNR for increasing values of N and observing the point at which the SNR no longer increases by 6.02dB per bit.

In the limit, the sinewave inputted to the weighting function and the FFT can be made ideal ($N \rightarrow \infty$), and the true noise floor of the FFT itself can be analyzed. This method allows the characteristics of the weighting function to also be examined in detail.

IDEAL N-BIT SINEWAVE GENERATOR

$$v(n) = V_o \sin\left(\frac{2\pi n f_{in}}{f_s}\right) \qquad \text{IDEAL}$$

$$v_q(n) = \text{INT}\left[\frac{V_o \sin\left(\frac{2\pi n f_{in}}{f_s}\right)}{q}\right] \qquad \text{IDEAL N-BITS}$$

$$q = \frac{2V_o}{2^N} = 1\text{LSB}$$

$$v_q(n) = \text{INT}\left[2^{N-1} \sin\left(\frac{2\pi n f_{in}}{f_s}\right)\right]$$

f_{in} = Input Frequency
f_s = Sampling Rate
n = nth Time Sample

Figure 1.61

SINEWAVE CURVE FITTING

This test is a global description of the dynamic performance of an A/D converter. A fullscale sinewave is digitized by the A/D converter and stored in memory (typically, 1024 samples is sufficient). The sinewave frequency is chosen to be non-subharmonically related to the sampling rate, much as in the case of non-coherent FFT testing.

The software then calculates the "best-fit" ideal N-bit sinewave to fit the data points. The sinewave amplitude, offset, frequency, and phase are chosen to minimize the RMS error between the actual sinewave and the ideal sinewave. A detailed description of the algorithms used is given in the following references:

HP Journal, November 1982, Vol 33, No. 11, pp. 24-25.

HP Journal, February 1988, Vol. 39, No. 1, p. 48.

It should be noted that the curve-fit algorithm is much simpler if the precise sinewave frequency is known. Also, the probability of the algorithm converging is much higher.

After the software computes the RMS error, Q_A, between the ideal sinewave and the actual sinewave, the ENOB can be calculated from the following equation:

$$ENOB = N - \log_2\left(\frac{Q_A}{Q_T}\right)$$

where Q_T is the theoretical RMS quantization error, $q/\sqrt{12}$.

This measurement includes errors due to differential non-linearity, integral non-linearity, missing codes, aperture jitter, noise, etc., as well as quantization noise.

The value for ENOB calculated using the sinewave curvefit method correlates well with the value obtained from the fullscale FFT SNR measurement,

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB}{6.02}$$

If the input signal is less than fullscale, a correction factor must be added to the latter equation in order to achieve correlation between the two methods:

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB + \begin{matrix}\text{LEVEL OF}\\ \text{SIGNAL}\\ \text{BELOW}\\ \text{FULLSCALE}\end{matrix}}{6.02}$$

CALCULATING ENOB USING SINEWAVE CURVE FITTING

Q_A = Actual RMS Error from Best Fit Sinewave

Q_T = Theoretical N-Bit RMS Error From Best Fit Sinewave = $q/\sqrt{12}$

$$ENOB = N - \log_2 \left(\frac{Q_A}{Q_T} \right)$$

Correlates To

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB + \text{Level of Signal Below FS}}{6.02}$$

Figure 1.62

TESTING A/D CONVERTER DYNAMIC PERFORMANCE USING THE "BEAT FREQUENCY" METHOD

A useful method for reducing the effects of the D/A converter in making gross back-to-back measurements on an A/D converter is shown in Figure 1.63. Here, the analog input sinewave is slightly lower in frequency than one-half the sampling frequency. The registers driving the D/A converter are updated at an even submultiple of the sampling rate, f_s/N, where N is a power of 2 (not the A/D resolution). The resulting signal from the D/A converter is a low frequency sinewave having a frequency equal to the difference between one-half the sampling rate and the analog input frequency.

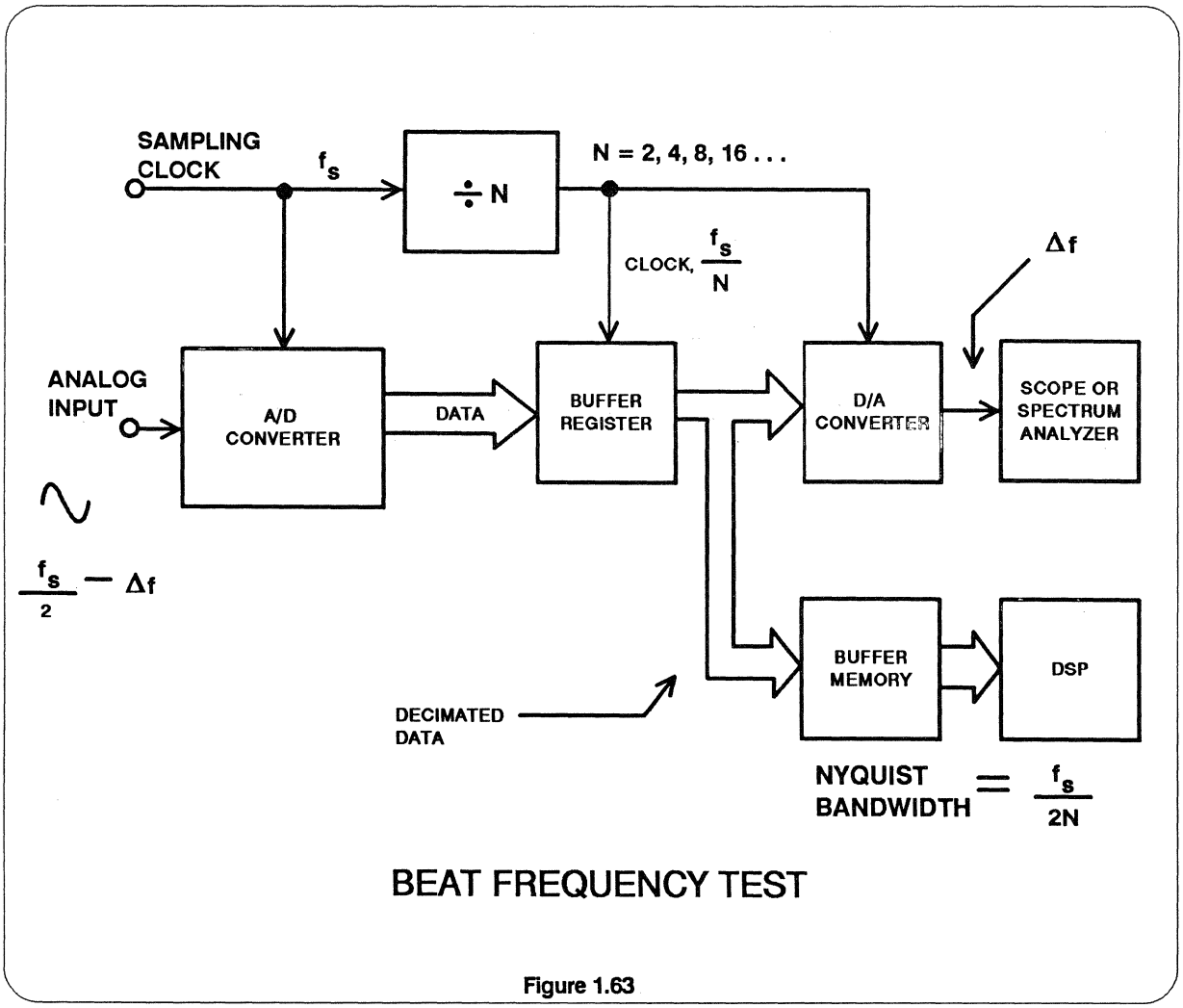


Figure 1.63

In this method, the A/D converter is being stressed with a near-Nyquist signal and is operating at its maximum sampling rate. The D/A converter is being clocked at a much lower decimated rate, f_s/N, thereby reducing the effects of glitches and other dynamic errors. Signal-to-noise measurements can be made over the Nyquist bandwidth $f_s/2N$. The low frequency "beat" can be examined easily on an oscilloscope for missing codes and other non-linearities. A standard low frequency spectrum analyzer can measure the harmonic content of the "beat" frequency.

The harmonics of the low frequency "beat" are directly related to the harmonics of the actual A/D converter analog input frequency.

In practice, a "beat" frequency of a few hundred kilohertz works well. Both the analog input sinewave and the sampling frequency should be derived from the frequency synthesizers or crystal oscillators to prevent "smearing" of the low frequency "beat" signal.

The beat frequency test is also effective in measuring the A/D converter's performance for input signals which are near the sampling frequency. The A/D performance under these conditions is of particular interest in radar I and Q systems, and in IF-to-Digital applications. In this test, the analog input frequency to the A/D is made slightly less than the sampling rate, f_s. In this case, a low frequency "beat" would be generated even if the D/A converter were updated at the sampling rate. It is still desirable, however, to update the D/A converter at f_s/N to reduce the effects of D/A dynamic errors on the measurements.

Evaluation boards which are designed to allow the user to evaluate high-speed flash converters usually have on-board D/A converters to make "coarse" performance measurements easy. The addition of output register clock frequency "decimation" circuitry on the board greatly facilitates beat frequency tests.

NON-LINEARITY TESTING USING HISTOGRAMS

In order to make a histogram analysis of an A/D converter, a known periodic input signal is digitized at a rate which is asynchronous relative to the input signal. After a statistically significant number of samples (usually at least 100,000) have been taken, the relative number of occurrences of each digital code (code density) is determined. This data is then normalized based upon the input signal, and the results are analyzed for linearity errors.

For an ideal A/D converter with a full scale triangular wave input, an equal number of codes should occur in each bin. The number of counts in the nth bin, H(n) divided by the total number of samples taken, M, is the width of the bin as a fraction of full scale. The ratio of the actual bin width to the ideal bin width P(n) is the differential linearity and should be unity. Subtracting one LSB gives the differential non-linearity in LSBs.

$$DNL(n) = \frac{H(n)}{M \cdot P(n)} - 1.$$

Integral non-linearity can be determined by compiling a cumulative histogram. The cumulative bin widths are the transition levels. The histogram approach is more often used, however, in evaluating differential non-linearity, since the cumulative effects of errors can make the integral non-linearity measurements somewhat inaccurate.

Since high speed triangles are difficult to generate to the required level of accuracy, sinewave inputs are usually selected for histogram DNL measurements. Because all codes are not equally probable with a sinewave input, the histogram data must be normalized using the probability density function for a sinewave as shown in Figure 1.65.

In order to obtain accurate results, a large number of samples must be taken. For example, to determine the DNL for an 8-bit converter to within 0.1 bit with 99 percent confidence, 268,000 samples are needed. It should be noted that these samples can be "counted" in hardware rather easily, thereby speeding up the software processing time. For high speed sampling, the output data can be decimated to rates which are compatible with slower speed memory.

An excellent treatment of this subject can be found in the following:

Joey Doernberg, Hae-Seung Lee, David A. Hodges, "Full Speed Testing of A/D Converters", **IEEE Journal of Solid State Circuits**, Vol. SC-19, No. 6, December 1984, pp. 820-827.

HP Product Note 5180A-2, pp. 3-9.

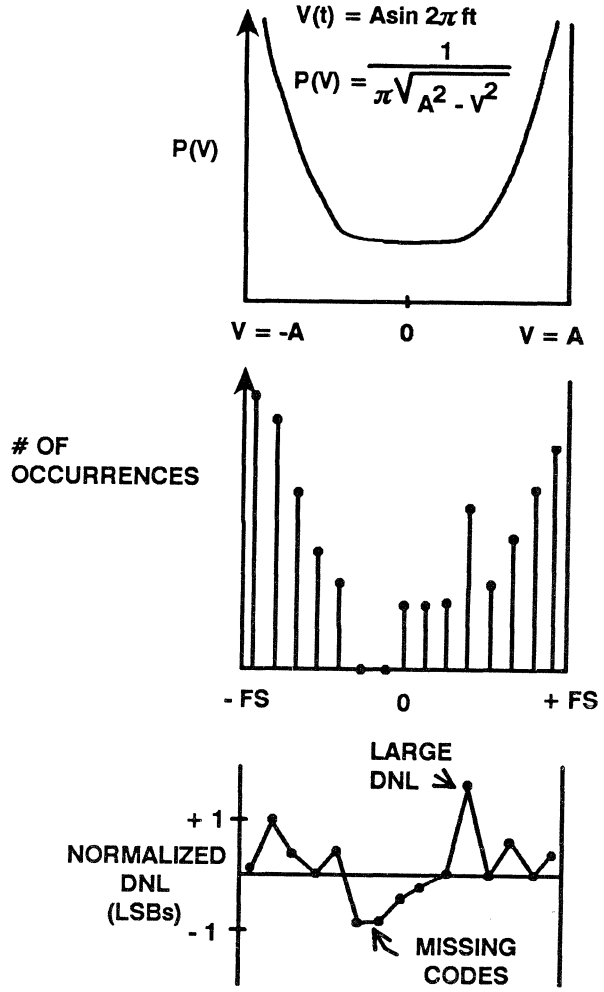
DNL HISTOGRAM USING TRIANGLE INPUT SIGNAL

$$DNL\ (Code\ n) = \frac{\#\ of\ times\ Code\ n\ Occurs}{M \cdot Probability\ of\ Code\ n} - 1$$

M = Total Number of Samples Taken.

For Triangle, Probability of Code n = $\frac{1}{2^N}$

Figure 1.64

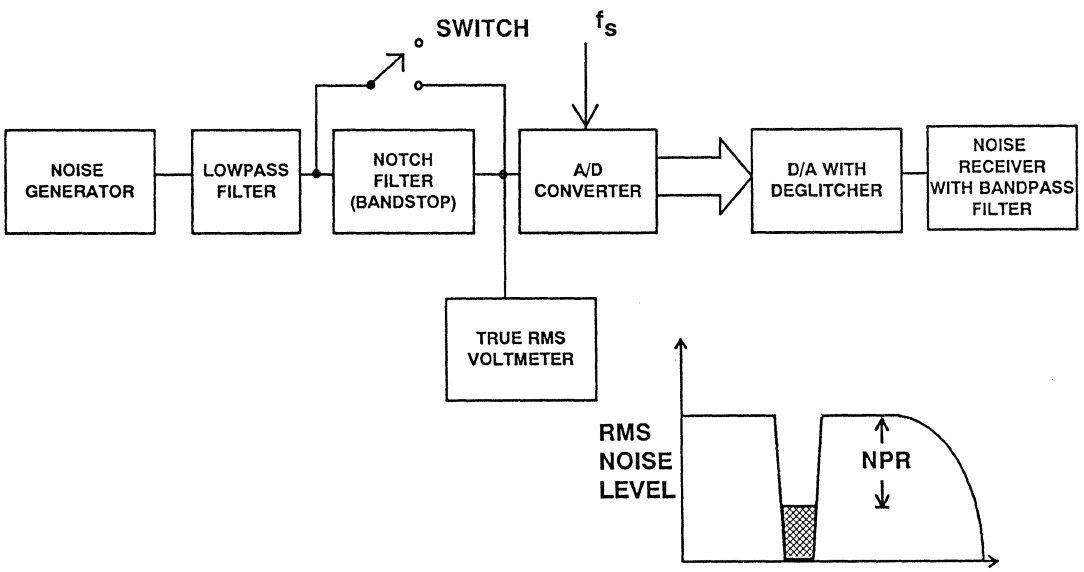


DNL HISTOGRAM USING SINEWAVE INPUT SIGNAL

Figure 1.65

NOISE POWER RATIO (NPR) TESTING

Noise power ratio testing has been used extensively to measure the transmission characteristics of Frequency Division Multiplexed (FDM) communications links. In a typical FDM system, 4kHz wide voice channels are "stacked" in frequency for transmission over coaxial, microwave, or satellite equipment. At the receiving end, the FDM data is demultiplexed and returned to 4kHz individual baseband channels. In an FDM system having more than approximately 100 channels, the FDM signal can be approximated by Gaussian noise with the appropriate bandwidth. The test setup of Figure 1.66 shows how an individual 4kHz channel can be measured for "quietness" using a narrow-band notch (bandstop) filter and a special tuned receiver which measures the noise power inside the 4kHz "notch".



NOISE POWER RATIO TEST SETUP

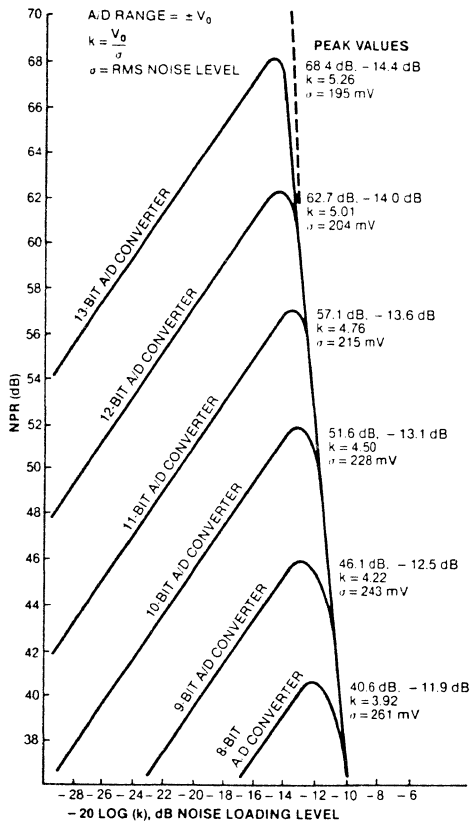
Figure 1.66

Noise Power Ratio (NPR) measurements are straightforward. With the notch filter out, the rms noise power of the signal inside the notch is measured by the receiver. The notch filter is then switched in, and the residual noise inside the slot is measured. The ratio of the two readings expressed in dB is the NPR. Several slot frequencies across the noise bandwidth (low, midband, and high) are tested to characterize the system adequately.

Noise Power Ratio is usually plotted on an NPR curve. The NPR is plotted as a function of rms noise level referred to the peak range of the system. For very low

noise loading levels, the undesired noise (in non-digital systems) is primarily thermal noise and is independent of the input noise level. Over this region of the curve, a 1dB increase in noise loading level causes a 1dB increase in NPR. As the noise loading level is increased, the amplifiers in the system begin to overload, creating intermodulation products which cause the noise floor of the system to increase. As the input noise increases further, the effects of "overload" noise predominate, and the NPR is reduced dramatically. FDM systems are usually operated at a noise loading level a few dB below the point of maximum NPR.

In a digital system containing an A/D converter, the noise within the slot is primarily quantizing noise when low values of noise input signals are applied. The NPR curve is linear in this region. As the noise input level increases, "clipping" noise caused by the hard-limiting action of the A/D converter begins to predominate. A set of theoretical NPR curves for A/D converters of various resolutions is shown in Figure 1.67.



THEORETICAL NPR CURVES FOR DIGITAL SYSTEMS

Figure 1.67

In a practical A/D converter, any dc or ac non-linearities will cause a departure from the theoretical NPR. Although the peak value of NPR occurs at a fairly low input noise level (RMS noise $\cong V_o/4$ where $\pm V_o$ is the range of the A/D converter), the broadband nature of the noise signal stresses the A/D converter, and the test provides a good indication of its dynamic performance.

Theoretically, NPR readings should not be dependent on any particular slot frequency. However, because of increased non-linearities for the higher input frequencies, NPR readings in the higher slots tend to give lower readings.

The following references are recommended for further study on NPR:

G.A. Gray and G.W. Zeoli, "Quantization and Saturation Noise Due to Analog-to-Digital Conversion," IEEE Trans. Aerospace and Electronic Systems, pp. 222-223, Jan. 1971.

M.J. Tant, "The White Noise Book", Marconi Instruments, July 1974.

NPR Testing Using DSP Techniques

Making NPR measurements on an A/D converter using FFT analysis techniques as described in the previous SNR section presents a real challenge. Consider the case where the record length is 1024 and the sampling rate is 20MHz. The FFT of 1024 contiguous time samples would place a spectral component every 19.53 kHz (20MHz/1024). Obviously, since the notch filter slot width is approximately 4kHz, the probability of a spectral component falling within the notch is very low.

To achieve reasonable data stability in the FFT NPR analysis, a number of samples must fall within the notch. If ten samples were required within the 4kHz notch, the resolution of the FFT would need to be 400Hz, necessitating a record length of 50,000 for a sampling rate of 20MHz. To avoid the need for an extremely large buffer memory (and hence more demands on the FFT processor), the notch filter can be widened to provide more samples within the notch. For 20MHz sampling and a 1024 word buffer memory, a notch filter having a width of 200kHz will provide ten frequency bins inside the notch. Even under these conditions, however, the NPR calculations for several records should be averaged to provide reasonable data stability.

DIGITAL NPR TESTING CONSIDERATIONS

- M = 1024 = Record Length
- f_s = 20.48 MHz
- $\Delta f = \frac{f_s}{M}$ = 20kHz = FFT Bin Width
- For 10 Samples in "Notch",
  Make Notch Filter Width = 200kHz
- Average Several Runs

Figure 1.68

A/D CONVERTER TRANSIENT RESPONSE TESTING

The response of an A/D converter to a transient input such as a square wave is often critical in radar applications. The major difficulty in implementing this test is obtaining a pulse which is known to be "flat" to the desired accuracy consistent with the A/D converter resolution.

A test setup for measuring the transient response of an A/D converter is shown in Figure 1.69 along with a recommended flat pulse generator. If the simple flat pulse generator is mounted as close as possible to the analog input of the A/D converter, the input applied to the A/D converter can be assumed to be flat to at least 10-bit accuracy a few nanoseconds after the schottkey diodes have been reverse biased. The programmable delay can be used to vary the phase of the sampling clock with respect to the flat pulse.

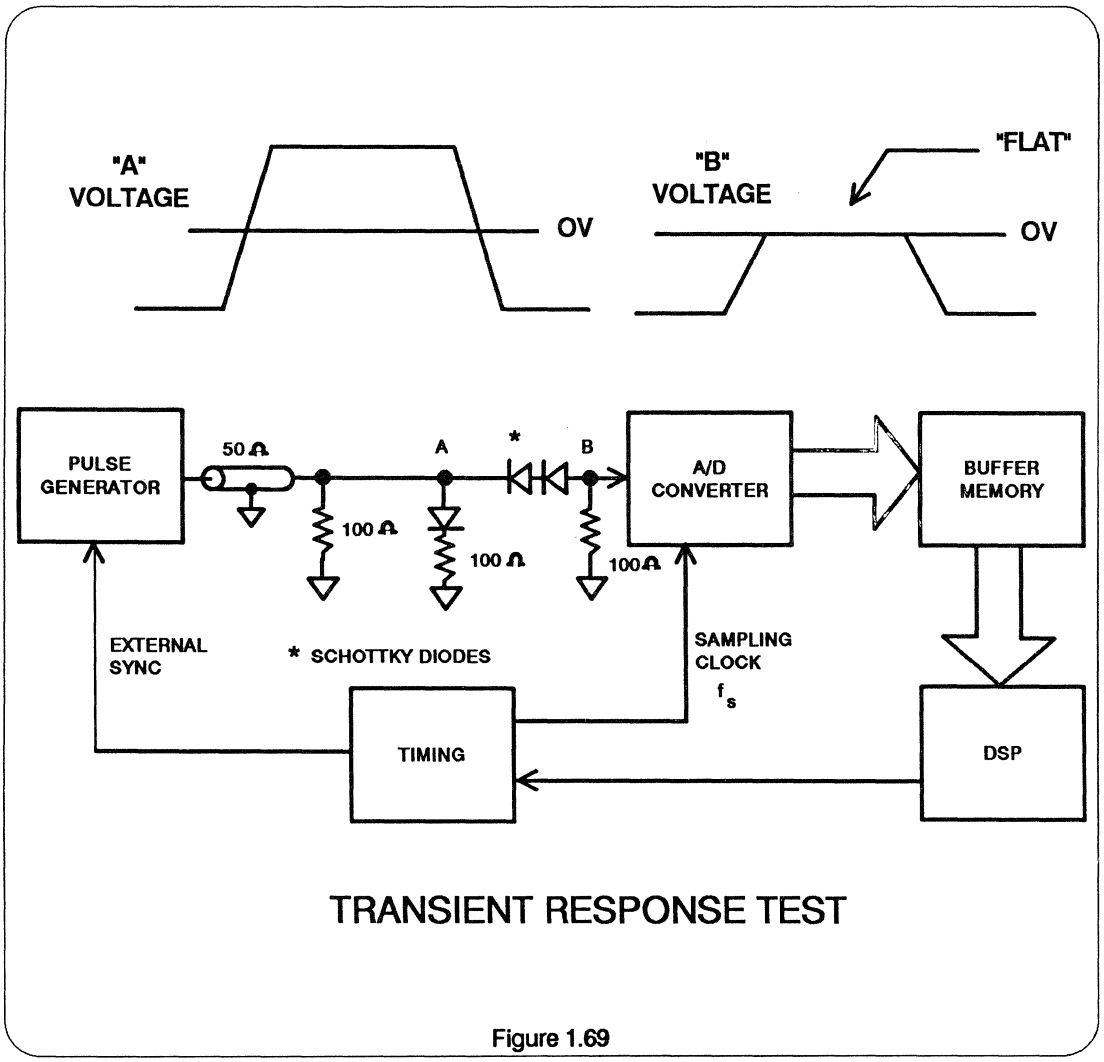


Figure 1.69

The time required for the A/D converter output to settle within 1 LSB of the final value can be measured easily using the delay generator in conjunction with the buffer memory and the computer. The effective aperture delay time must be considered when making the transient response measurement.

Further details regarding the generation of flat pulses can be found in:

"A Programmable Precision Voltage-Step Generator for Testing Waveform Recorders" IEEE Transactions on Instrumentation and Measurement, Vol. IM-33, No. 3, Sept. 1984, pp.

"Reference Waveforms Flat Pulse Generator," IEEE Transactions on Instrumentation and Measurement, Vol. IM-32, No. 1, March 1983, pp. 27-32.

A/D CONVERTER OVERVOLTAGE RECOVERY TESTING

The time required for an A/D converter to recover from a signal which falls outside the converter's range can be measured in a manner similar to the transient response measurement. Overvoltage recovery time is defined as that amount of time required for the A/D converter to achieve a specified amount of accuracy when measured from the time the overvoltage signal re-enters the converter's range, as shown in Figure 1.70. The amount of overvoltage is generally specified as a percentage of the A/D converter's range. For a converter with a 2-volt input range, 50% overvoltage would correspond to 1 volt above or below the nominal 2-volt input range.

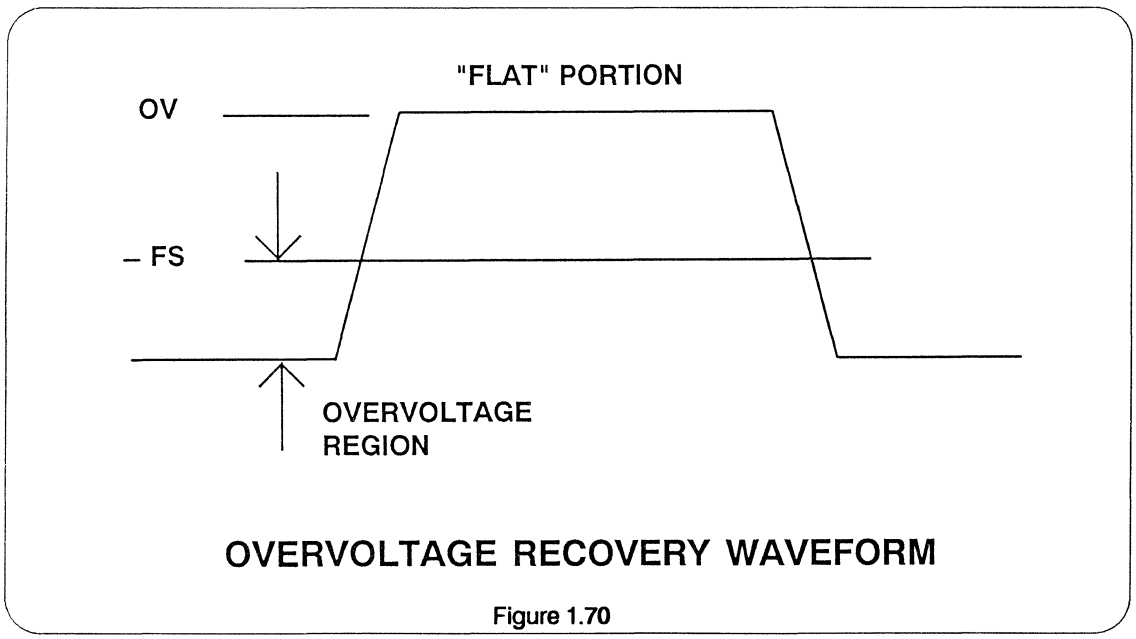
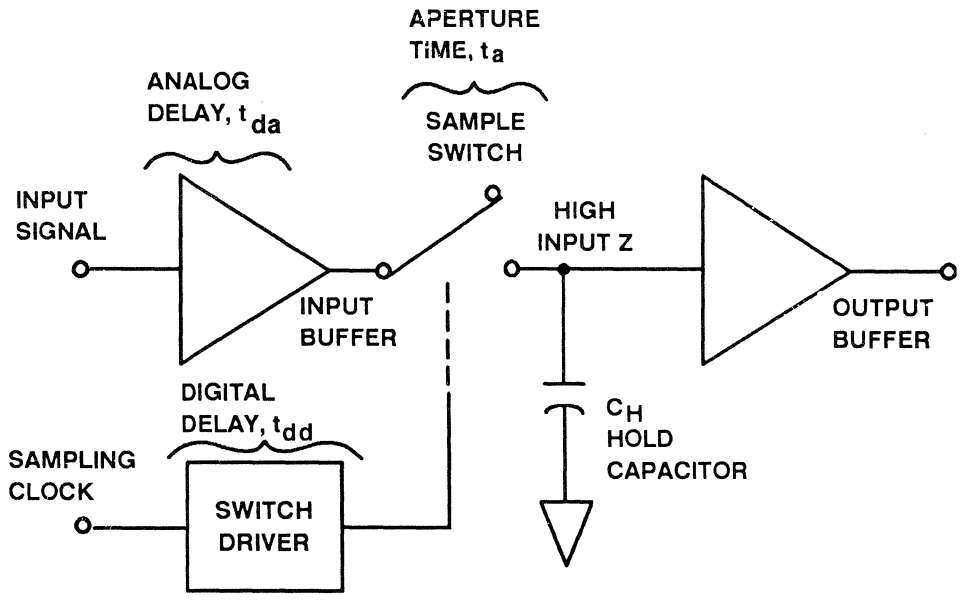


Figure 1.70

The same test setup used for measuring transient response (Figure 1.69) can be used to measure overvoltage recovery time. The "starting point" of the flat pulse is made to correspond to the desired overvoltage condition. The actual overvoltage recovery time is referenced to the time the input signal re-enters the A/D converter input range. As in the transient response test, the effective aperture delay time must be considered when making this measurement.

APERTURE TIME AND APERTURE JITTER

The aperture time and aperture jitter specifications on video A/D converters have been probably the most misunderstood and misused specifications in the entire field. The original concept of aperture time centered around the classic sample and hold circuit shown in Figure 1.71. In an ideal sample and hold, says the theory, the switch has zero resistance when closed, and opens instantly on receipt of a sampling clock. In practice, however, the sampling switch transits from a low to high resistance over some finite time interval. According to the



IDEALIZED SAMPLE-AND-HOLD CIRCUIT

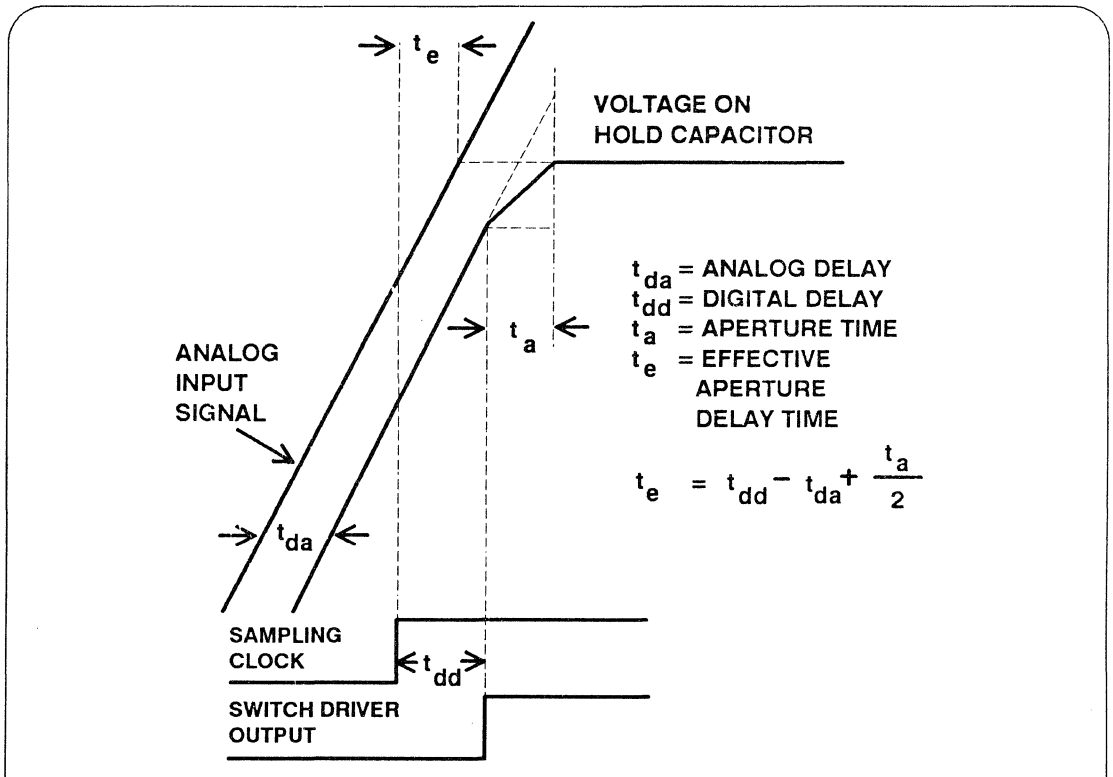
Figure 1.71

argument, an error occurs because the input signal tends to be averaged over the finite time interval required for opening the switch. The sampled voltage, therefore - the argument continues - does not exactly correspond to the voltage at the instant the switch starts to open. The time required to open the switch was referred to as aperture time. The classic formula then arose,

$$E_a = t_a \frac{dv}{dt}$$

where E_a is the aperture error, t_a is the aperture time, and dV/dt is the rate at which the input signal changes.

A simple first-order analysis which neglects non-linear effects shows that no real error exists for such a switch. As long as the switch opens in a repeatable fashion, there exists an effective sampling point in time which will cause an ideal sample and hold ($t_{dd} = t_{da} = t_a = 0$) to produce the same held voltage (see Figure 1.72). The difference between this effective sampling point and the leading



SAMPLE-AND-HOLD WAVEFORMS

Figure 1.72

edge of the actual sampling clock is a fixed delay and does not constitute an error. This delay is appropriately called effective aperture delay time, or the interval of time between the leading edge of the sampling clock and the instant when the input signal was equal to the held value. This specification is important because it helps the A/D converter user to know when to apply the sampling clock with respect to the input signal timing. The variation or tolerance placed on this value from part to part is important in simultaneous sampling applications or other applications where the A/D converters are required to track each other when processing dynamic signals. Adjustable delays in the sampling clock signals to match the effective aperture delay times of several A/D converters may be required in exacting applications such as I and Q radar receivers. Effective aperture delay time tracking over temperature may also be a consideration.

True aperture errors, however, do result from variable sample-to-sample time delays. These errors generally emanate from several sources. In a practical A/D, the sampling clock is often phase-modulated by some unwanted source; the source can be wideband random noise, power-line noise, or digital noise due to poor grounding techniques. The resulting error can be expressed in terms of an rms time jitter, and can be properly referred to as aperture jitter. The corresponding rms voltage error caused by rms aperture jitter qualifies as a valid aperture error. Phase jitter on the input sinewave can produce the same effect as jitter on the sampling clock.

The aperture jitter specification on an A/D converter is sometimes interpreted as a measure of the converter's ability to digitize rapidly changing input signals accurately. While the aperture jitter specification is important, it does not tell the entire story. An A/D converter with an impressive aperture jitter specification still may lose ENOBs when digitizing a sinewave having a maximum slew-rate calculated from the aperture formula

$$E_a = t_a dV/dt.$$

For example, assume a 20MHz, 10-bit A/D converter has a bipolar input range of $\pm V_o$ ($2V_o$ peak-to-peak) and an aperture jitter specification of 10 ps rms. To calculate the maximum aperture jitter error, the rms aperture jitter must be converted into a maximum value rather than an rms value. If one assumes that aperture jitter follows a Gaussian distribution similar to white noise, the rms aperture jitter, t_a, corresponds to the sigma (σ) of the distribution. The 2σ point on the distribution is a good place to set the maximum, and the maximum aperture jitter becomes $2t_a$.

If the corresponding maximum voltage error, Δv, at the zero crossing of a fullscale sinewave, is set to 1/2 LSB (1/2 LSB = $2V_o/2^{N+1}$, where N is the number of bits of resolution), the maximum fullscale sinewave frequency, f_{max}, which will produce the 1/2 LSB aperture error, can be calculated:

FREQUENCY REQUIRED TO PRODUCE 1/2 LSB APERTURE JITTER ERROR

$$v(t) = V_o \sin 2\pi ft$$

$$\frac{dv}{dt} = 2\pi f V_o \cos 2\pi ft$$

$$\left.\frac{dv}{dt}\right|_{MAX} = \frac{\Delta v}{2t_a} = 2\pi V_o f_{MAX}$$

$$\therefore f_{MAX} = \frac{\Delta v}{4\pi V_o t_a} = \frac{2\, V_o/2^{N+1}}{4\pi V_o t_a} = \frac{1}{2\pi t_a\, 2^{N+1}}$$

For t_a = 10psec, N=10, f_{MAX} = 7.8Mhz

Figure 1.73

For t_a = 10 ps rms, and N = 10, f_{max} is calculated to be 7.8MHz. These calculations imply the 20MHz A/D converter under consideration can accurately digitize a fullscale sinewave of 7.8MHz. In actual practice, however, the A/D converter may begin to suffer from skipped codes, decreased ENOBs and SNR, ac non-linearities, etc., at much lower frequencies. These other limitations to good high frequency performance may, in fact, be significantly greater than errors caused by the aperture jitter of the track-and-hold.

The Effects Of Aperture Jitter On A/D SNR Measurements

The effects of aperture jitter on fullscale sinewave SNR can be calculated as follows:

$$v(t) = V_0 \sin 2\pi ft$$

$$\frac{dv}{dt} = 2\pi f V_0 \cos 2\pi ft$$

$$\left.\frac{dv}{dt}\right|_{rms} = \frac{2\pi f V_0}{\sqrt{2}}$$

For an rms error voltage, Δv_{rms}, and an rms aperture jitter of t_a,

$$\frac{\Delta v_{rms}}{t_a} = \frac{2\pi f V_0}{\sqrt{2}}$$

$$\Delta v_{rms} = \frac{2\pi f V_0 t_a}{\sqrt{2}}$$

The rms signal to rms noise ratio expressed in dB becomes:

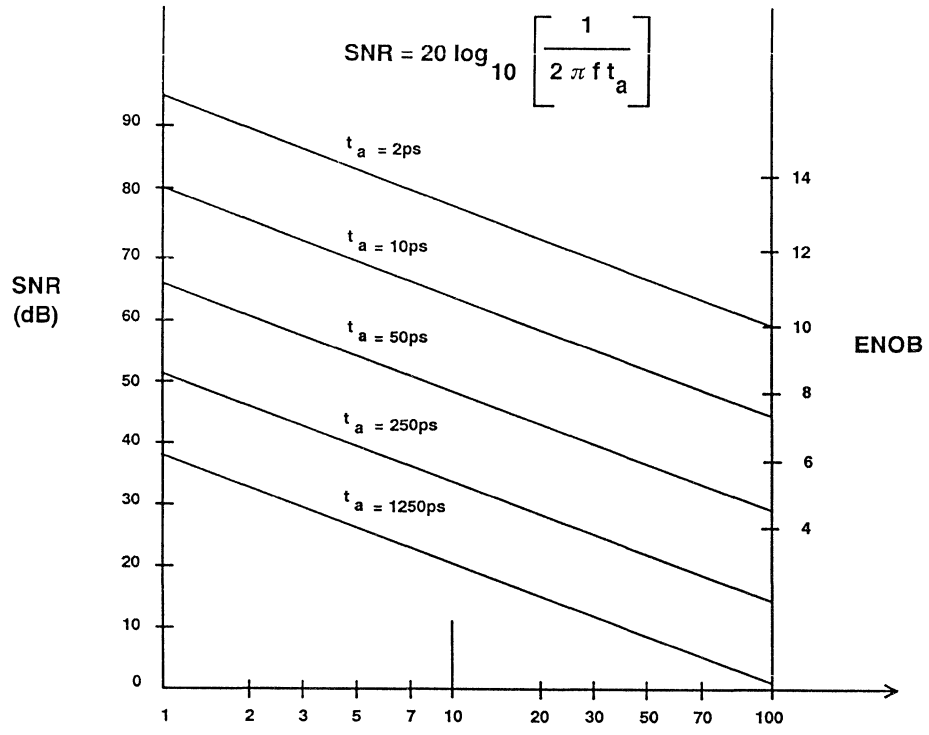
$$SNR = 20\log_{10}\left[\frac{V_0/\sqrt{2}}{\Delta v_{rms}}\right] dB$$

$$= 20\log_{10}\left[\frac{1}{2\pi f t_a}\right] dB$$

The SNR due exclusively to aperture jitter in the equation above is plotted in Figure 1.74 as a function of fullscale input sinewave frequency for various values of aperture jitter.

Consider the example above for a 10-bit, 20MHz A/D converter with an rms aperture jitter of 10 ps. For an 8-MHz fullscale input, the SNR due to only aperture jitter is 66dB as calculated from the equation. The theoretical SNR due to quantizing noise in a 10-bit A/D converter is 62dB. Combining the SNR of 66dB with the SNR of 62dB, a theoretical SNR of 60.5dB is obtained for the A/D; this encompasses both the ideal quantizing noise and the noise due to aperture jitter. A practical 10-bit A/D having an rms aperture jitter specification of 10 ps may, however, only achieve an SNR of 50dB.

From this analysis, one can conclude that the SNR, ENOB, and aperture jitter specifications must <u>all</u> be examined in order to truly evaluate the A/D converter's dynamic performance.



SIGNAL TO NOISE RATIO DUE TO APERTURE JITTER

Figure 1.74

Measurement Of Aperture Jitter Using A Locked Sinewave Histogram

The aperture jitter of an A/D converter can be measured using the test setup shown in Figure 1.75. The sampling clock and the analog input signal are derived from the same low-jitter pulse generator to minimize the phase jitter between them. The phase shifter is adjusted until the A/D converter is repetitively sampling the sinewave at its point of maximum slew-rate at midscale. A histogram is then taken on the digitized A/D converter output data.

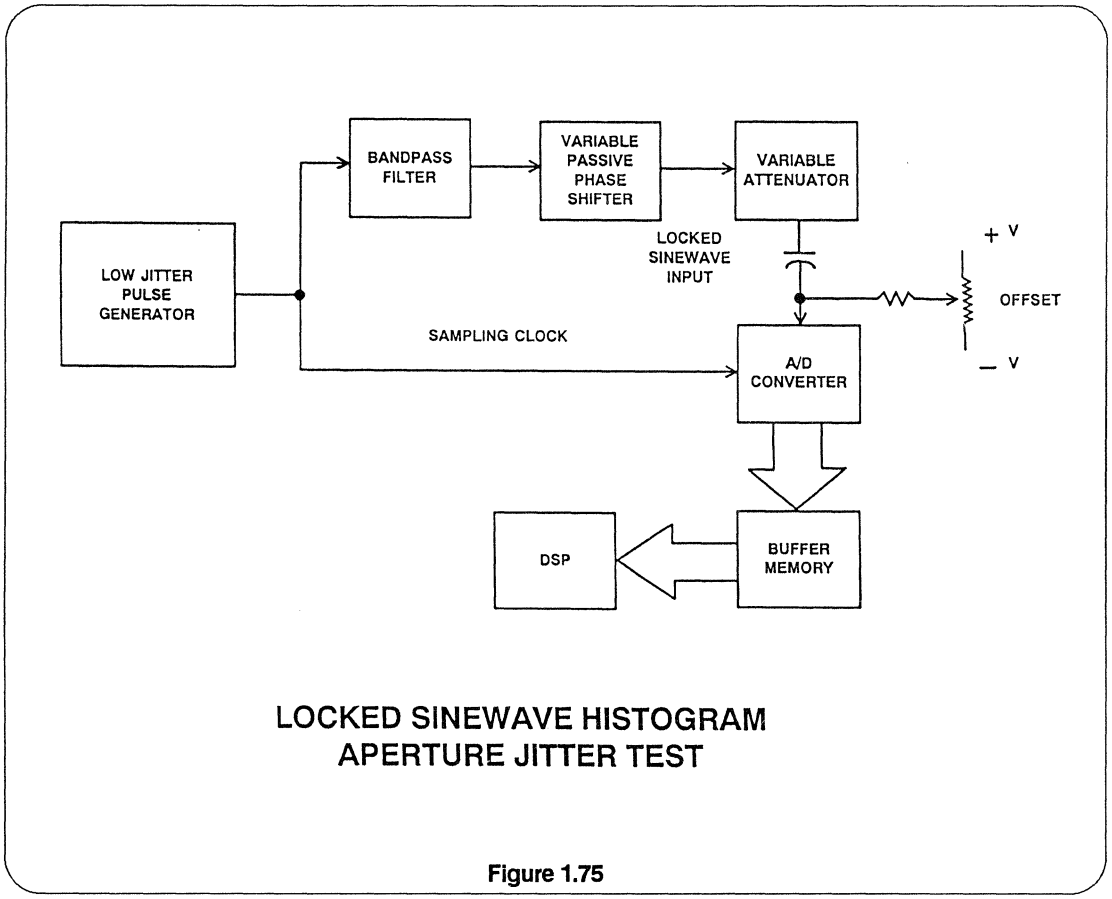
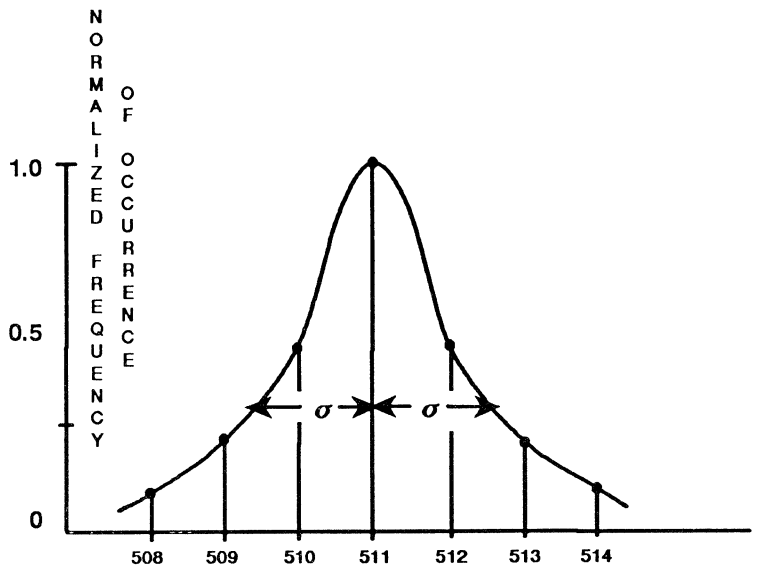


Figure 1.75

An ideal A/D converter with no aperture jitter would have only one code present on the histogram. A practical converter will give a distribution of codes as shown in Figure 1.76. The sigma (σ) of the distribution is calculated and corresponds to the rms error voltage Δv_{rms}, produced by the rms aperture jitter, t_a. The aperture jitter, t_a, can then be calculated from the formula,

$$t_a = \frac{\Delta v_{rms}}{dv/dt}$$

where dV/dt is the rate-of-change of the sinewave at zero-crossing.



APERTURE JITTER HISTOGRAM

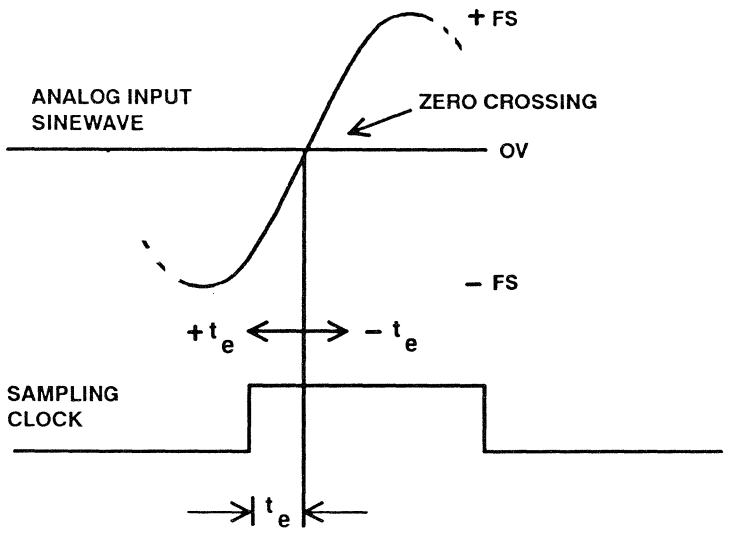
Figure 1.76

If the input sinewave is attenuated sufficiently, the width of the distribution around the nominal code is due to intrinsic A/D converter noise. As the input sinewave is increased in amplitude, the slew-rate, dV/dt, becomes proportionally greater, and the distribution begins to spread due to the aperture jitter. Caution must be exercised in interpreting the histogram for high slew-rate inputs since the ac differential linearity of the converter can also be affected by the higher slew-rate input.

The offset adjustment shown in Figure 1.75 allows the sinewave to be positioned at different points on the A/D converter range. In this way, histograms can be plotted around several nominal codes, and any variations can be attributed to range-dependent differential linearity characteristics. The A/D converter's range can be exceeded when offsetting the sinewave in this manner, so careful control of the offset is necessary.

Measurement Of Effective Aperture Delay Time

Effective aperture delay time can also be measured using the locked sinewave technique as previously shown in Figure 1.75. The phase shifter is adjusted until the A/D converter output reads midscale (i.e., the zero-crossing of the sinewave input signal). A dual trace oscilloscope is then used to measure the difference between the leading edge of the A/D converter sampling clock and the actual zero-crossing of the sinewave input (see Figure 1.77). The difference is the effective aperture delay time and can be either positive or negative depending upon the values of the internal analog and digital delays in the track-and-hold portion of the A/D converter.



MEASUREMENT OF EFFECTIVE APERTURE DELAY TIME

Figure 1.77

TESTING A/D CONVERTERS FOR COMPOSITE VIDEO APPLICATIONS

Differential gain and phase performance are of special importance when an A/D converter is to be used to digitize a composite video waveform. Differential gain is defined as the percentage difference between the output amplitudes of two stated levels of a small high frequency sinewave superimposed on a low frequency signal. Differential phase is the difference in the output phases of two stated levels of a small high frequency sinewave superimposed on a low frequency signal. Distortion free processing of a color signal requires that neither the amplitude nor the phase of the chrominance signal be altered significantly as a function of the associated luminance signal. These tests are generally performed in the analog world (A/D and D/A back-to-back) using conventional video test equipment. These and other tests relating to video applications have been described previously in the literature:

W.A. Kester, "PCM Signal Codecs for Video Applications," SMPTE Journal 88, November 1979, pp. 770-778.

DIGITAL VIDEO SPECIFICATIONS

- Differential Gain
- Differential Phase
- Bandwidth
- Linearity - Low Frequency
- "2T" Pulse Response
- "12.5T" Modulated Sin^2 Pulse Response
- Chrominance-to-Luminance Distortion
- Chrominance Phase Linearity
- Color Bar Performance

Figure 1.78

ERROR RATE AND SPARKLE CODE TESTS

At the present time, there is no industry standard for either the definition or the test for A/D converter error rates. As has been discussed in the section on flash converters, comparator metastable states can occur for low or high frequency input signals. At high frequencies, "bubbles" in the thermometer code of the comparator bank output can also produce erroneous output codes. Subranging A/D converters are subject to error codes since they use flash converters as building blocks. The measurement of error rate requires that a large number of samples be taken, since error rates less than $1x10^{-6}$ are typical for well behaved A/D converters. Great care must be taken in the error rate test set layout, grounding, shielding, and power supply decoupling so that AC 60Hz, EMI, or RFI glitches don't give false errors.

The error rate for low frequency input signals can be measured as follows. A low frequency fullscale sinewave (or triangle wave) is applied to the A/D converter and its rate of change is selected to be much less than 1 LSB per sample. This ensures that the transition zones between codes are all adequately exercised. An error amplitude of X LSBs is established as the lower limit for the definition of a "qualified" error. Usually, X is selected to be several LSBs so that random noise doesn't produce false errors. The software or hardware then examines the difference between each adjacent sample and records the number of times (NQ) this difference exceeds the error threshold X. If NQ is the number of qualified errors that occur and NT is the total number of samples taken, then the error rate, ER, is given by the equation,

$$ER = \frac{NQ}{2 \cdot NT}$$

As an example, consider an 8-bit, 100 MHz flash converter where it is desired to take at least ten samples at each code level. For one slope of the triangle wave input, this implies 10 x 256 = 2560 samples. The frequency of the triangle wave can be calculated:

$$f_T = \frac{1}{2560 \cdot 2 \cdot 10ns} = 19.5kHz$$

At a 100MHz sampling rate, the average time required to make an error for an error rate of $1x10^9$ is 10 seconds.

Dynamic errors which occur due to fast input signals can be measured in a similar manner by using the "beat frequency" approach. The low frequency beat frequency is chosen to give the proper number of samples per code level, and the decimated digital outputs are examined for adjacent sample differences which exceed the allowable error amplitude.

In summary, determining an appropriate error rate criterion for an A/D converter depends upon both the application and the characteristics of the A/D under consideration. Flash converters which use straight binary decoding are most subject to large metastable errors at midscale. For this situation, a low amplitude "dither" input signal centered on the midscale code transition might be an appropriate stimulus. In a subranging A/D converter, a fullscale signal which exercises all the "subranging" points might be desirable.

Hopefully, as this error rate phenomenon becomes more fully understood, it will be possible to establish industry standards which are meaningful to a variety of applications and A/D converters.

ERROR RATE TESTING

- Define "Error", X LSBs
- Low or High Frequency Input?
- Examine Difference Between Adjacent Codes
- Take NT Samples
- Record NQ Qualified Errors

$$\text{Error Rate} = \frac{NQ}{2\,NT}$$

- Shielding, EMI, RFI Considerations
- Industry Standards?
- A/D Converter Architecture?

Figure 1.79

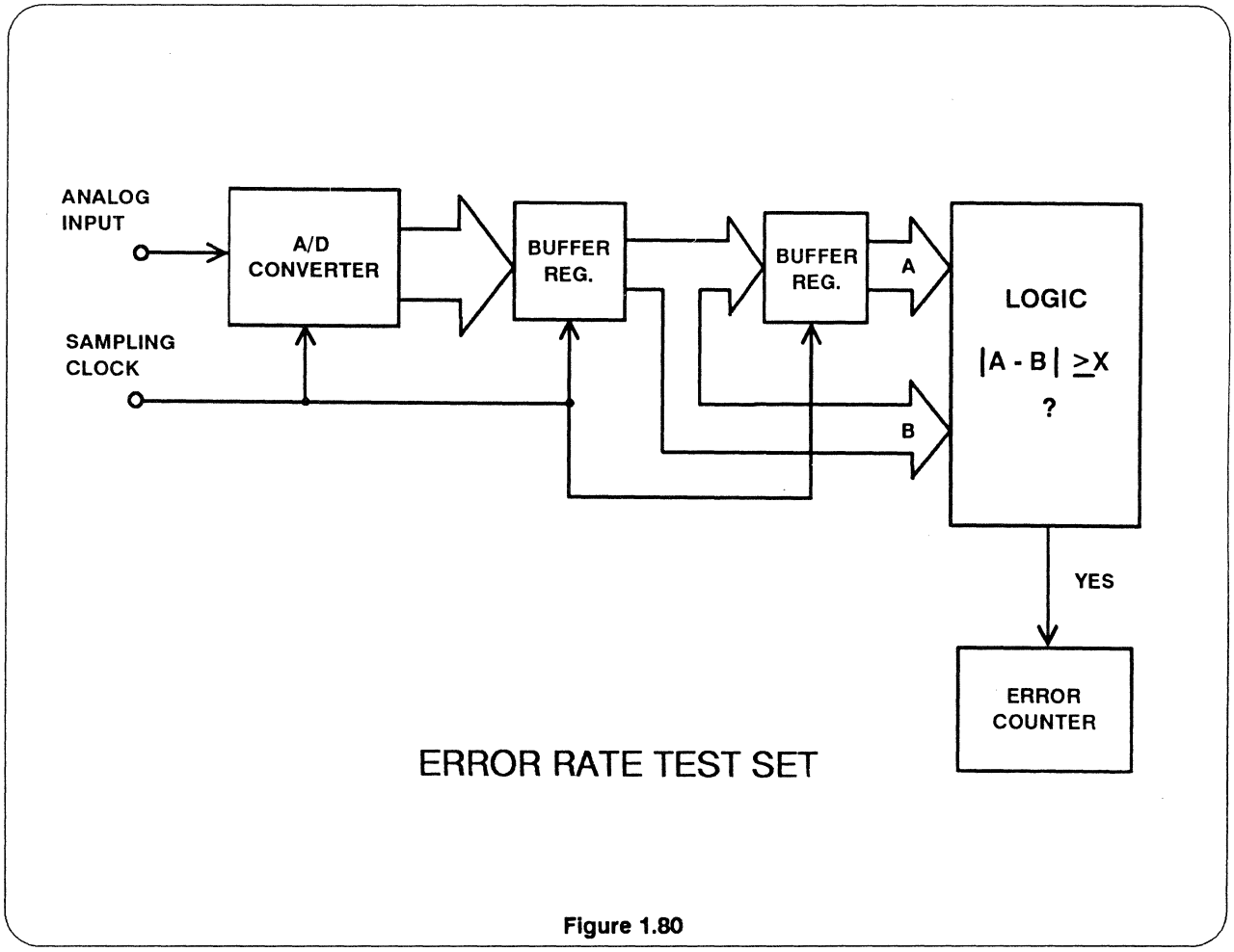

ANALOG
INPUT
A/D
CONVERTER
BUFFER
REG.
BUFFER
REG.
A
LOGIC
|A - B| ≥X
?
SAMPLING
CLOCK
B
YES
ERROR
COUNTER
ERROR RATE TEST SET

Figure 1.80

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MULTISTAGE ERROR CORRECTING A/D CONVERTERS

Analog Devices, Inc.

1

INTRODUCTION

The accelerating growth of digital signal processing has expanded the applications for high-speed data converters. High-speed (> 1 Megasample per second) analog-to-digital converters (ADC's) are required in a rapidly growing number of applications, such as video, radar, and medical instrumentation. The three primary ADC types used to meet these needs are the parallel or "flash" converter, the successive approximation converter, and the subranging converter.

This paper is intended as a tutorial on error-correcting ADC's. ADC's will be classified into two fundamental groups, and the limitations of each will be examined. The basic concepts of error correction will be developed, and a specific case will be studied in further detail. Finally, logical extensions of the basic technique will be considered.

BASIC CONVERTERS

All ADC's have three conceptual "parts" as shown in Figure 1; a reference source; a comparator; and a digital translator, which is also assumed to include control logic. The most common form of reference is the digital-to-analog converter (DAC). This is the reference element in successive approximation converters. A parallel ADC ("flash" converter) contains a multiport DAC, in the form of a resistor ladder with an output corresponding to each quantization level of the converter's transfer function. In some types of converters, the reference is not obvious. For example, the reference source of a cyclic or Grey code ADC is "hidden" in the manipulation of the input signal in each sequential stage. The actual analog-to-digital conversion element is the comparator. It can take the form of a single comparator, as in a successive approximation converter; a large bank of comparators, as in a flash; or something in between. Finally, some form of digital logic is required to convert the comparator output(s) into a digital representation of the input signal, and control the sequence. This is obviously a simplistic look at the operation of ADC's, but it is important to be able to sort out these basic functions. Sometimes a "new" technique comes along which, on a closer look, is actually one of the more familiar types.

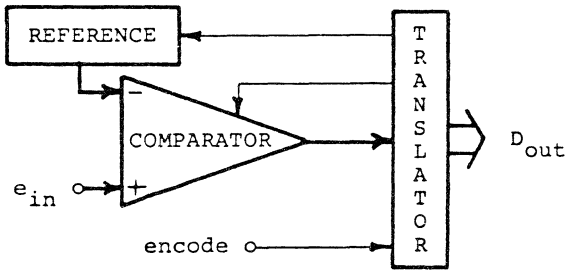


Fig. 1. Basic ADC.

Stages

The two main ADC categories germane to this session are single-stage and multistage. This categorization is somewhat misleading to anyone unfamiliar with these terms as used to describe converters. The term "single-stage" denotes any comparator which does its comparison at a single point in time. Converters in this category are full parallel or "flash" converters. All other converters are multistage. Although flash converters must perform a sequence of operations, there is only one comparison time.

"Multi-stage" ADC's can be further divided into two types. Subranging ADC's first "narrow down" the value of the analog input to a subrange of the total quantization range. This subrange is then subdivided further. A subranging ADC can have two or more stages, each of which could be further characterized as single-stage or multi-, subranging, etc. The second type of

multistage ADC's are non-subranging. This category is a catchall for such methods as integrating and tracking ADC's, whose general use is at substantially lower conversion rates. As a result, for the purposes of this paper, multi-stage and subranging can be considered the same.

Single-Stage Converters

Parallel, or "flash," converters represent a brute force approach to very high-speed conversion. The flash converter is covered in another part of this session. Because flash converters require a comparator, voltage reference, and digital translation for every quantization level, an upper limit now exists on flash resolution and linearity. This is due in part to the incredible circuit size, and also to the small differential voltage between quantization levels. If the number of converter bits increases by one, either the quantization level is reduced by one-half, or the full-scale input voltage must be doubled. The first situation puts a severe demand on comparator design, while the latter requires a higher-slew-rate, higher-power driving source. The current practical limit on this converter type (in monolithic form) is 8-9 bits. Although the theoretical resolution of a flash converter can be higher if implemented in discrete form, the cost, size, and power are generally prohibitive.

Multi-Stage Converters

Multi-stage converters provide high resolution with far fewer elements than single-stage converters. The obvious tradeoff is conversion speed. As discussed earlier, multi-stage converters common in high-speed converters are all of the subranging type. Subranging converters are used when higher resolution and/or lower power and complexity are required. A basic subranging ADC is shown in Figure 2. The first ADC is an N_1-bit encoder, usually a FLASH, which quantizes the analog input (e_{in}) into one of 2^{N_1} levels.

A DAC converts this into an equivalent voltage. This digitized, reconstructed signal is subtracted from the input e_{in} to yield the difference between the output of the first encoder and e_{in}. This, in turn, is quantized by the second encoder; and the output of N_2 LSB's and N_1 MSB's should represent the input. The primary sources of

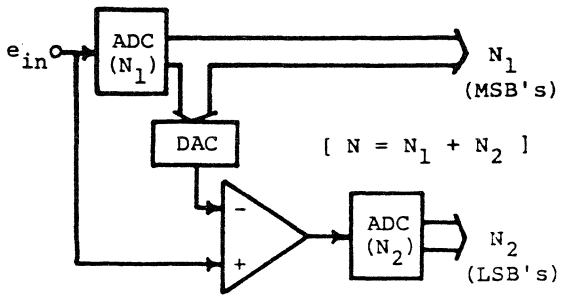


Fig. 2. N-bit Subranging ADC.

error in this type of converter are in the first conversion. Although it is only N_1 bits, it must be better than N bits accurate, and the input must settle to better than N bits accuracy before the first conversion. These requirements conflict with the need for high speed. It should be noted that this technique can be extended to any number of stages (up to N).

The successive approximation ADC is actually 12 one-bit encoders with a common DAC and comparator. This technique of using ADC stages more than once is called RECIRCULATING. The new SONY 8-bit monolithic encoder uses subranging with two 4-bit stages.[1] This is substantially less complex than an 8-bit flash, with correspondingly higher yields and lower cost.

Error Correction

The sources of error mentioned above can be overcome by use of a technique called error correction. The term error correction is a popular one and has a number of different meanings. Error correction in the context of this tutorial implies that the first stage(s) of a multi-stage ADC can make a priori unknown errors within a bounded range which are correctable via subsequent stage(s) of the converter. A more precise term is digitally corrected subranging, even though the errors to be corrected are analog in nature.

DIGITALLY CORRECTED SUBRANGING

Before developing the error correction technique, consider again the 2-stage ADC of Figure 2. The first encoder, DAC, and subtractor could also represent a circuit for testing the first encoder. The output of the subtractor vs. e_{in} should be a "sawtooth" waveform as shown in Figure 3. This will be referred to as an ERROR WAVE-

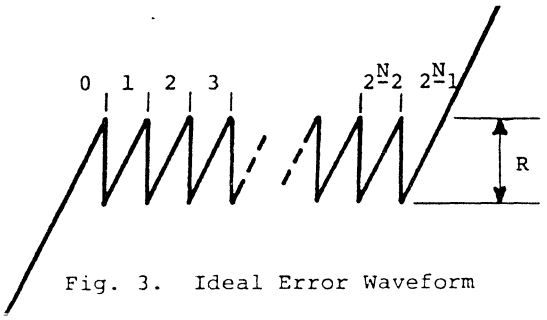


Fig. 3. Ideal Error Waveform

FORM. This waveform has 2^{N_1}-1 "teeth." Each vertical line represents the encoder changing state. Its height is the change in value of the DAC. The height of the sloped line represents the size of the corresponding quantization level of the encoder. All heights are the same because the encoder and DAC are assumed ideal. The height R represents the range of the second encoder. If each "tooth" does not exactly fill R, there will be an error in the overall converter transfer function.

For purposes of illustration, assume in Figure 2 that N_1=4(16 levels), and N_2=8(256 levels). This makes a 12-bit converter (4096 levels). Figure 4 shows the error waveform for this con-

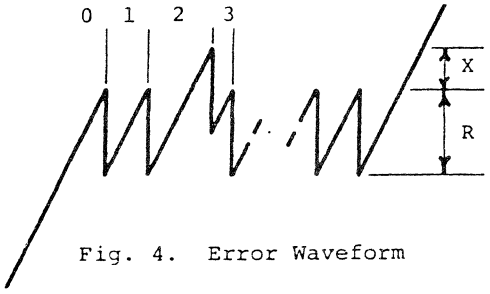


Fig. 4. Error Waveform

verter, but this time the first encoder is not perfect. Since code 2 is 1.5 times the expected quantization level and code 3 is 0.5, these codes are off by 1/2 a least significant bit (LSB) of the first encoder. This encoder, then, is 4 bits accurate. This is a perfectly respectable 4-bit ADC, but a disaster in a subranging converter. When the first "tooth" goes out of range, the code corresponding to code 2 of the first converter plus the full scale of the second converter (255) gives an output of 2 X 256 + 255 = 767. This code remains until the encoder switches to code 3. This results in an output of 3 X 256 + 128 = 896. The result is 128 missing codes! Note that this still assumed the DAC was perfect. It should be evident the missing codes can never be recovered unless the area X can be quantized with the second ADC.

What must be done to recover the "missing" codes? First, if the signal exceeds the range R, the value of the first encode must be increased by one. Then the value of the X quantization, rather than the R, is added. Therefore, the first code as the "tooth" starts to exceed R, would be (2 + 1) X 256 + 0 = 768. This would continue increasing to a peak value of (2 + 1) X 256 + 127 = 895. Thus, all the codes are found.

If the error waveform falls below the range of R, as in Figure 5, the

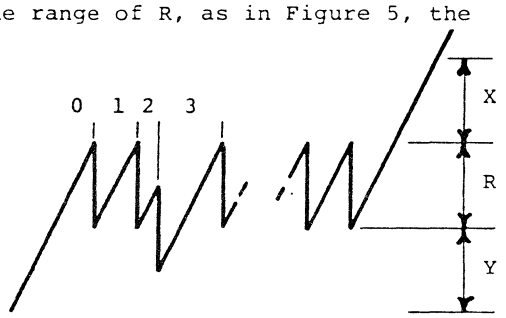


Fig. 5. Another Error Waveform.

range needs to be quantized. If the error waveform falls below the range R, the quantization of the difference between the signal and the bottom of R must be subtracted. At the top of the short "tooth," the output is 2 X 256 + 127 = 639. After switching to the next level, 3 X 256 - 128 = 640, and there are no missing codes.

The two scenarios described above could have been accomplished by adding or subtracting one count from the DAC, which would restore the error waveform to the range of the second ADC (R). This consumes significant time (DAC settling plus determining if the error waveform falls out of the range R). It is far more desirable to extend the range of the second ADC.

In the example above, to correct first stage errors of $\pm\frac{1}{2}$ LSB, the second stage would have to encode from -128 to +383 rather than from 0 to +255. The second stage could then be added directly to 256 X (first stage output). This requires a 9-bit second stage rather than an 8-bit. In effect,

this converter has one bit of correction. In general, if a stage has C bits of correction, it can correct for errors of $\pm\frac{1}{2}(2^C-1)$ LSB's. If 2 bits of correction are used in the second stage, the first stage could have errors up to $\pm 1\frac{1}{2}$ LSB's.

Returning to the example, the suggested second stage seems a bit odd, requiring a range of -128 to +383. An alternative approach is to use a "normal" 9-bit encoder (0-511); and use an offset voltage to center the error waveform in the second encoder range as shown in Figure 6. The digital output

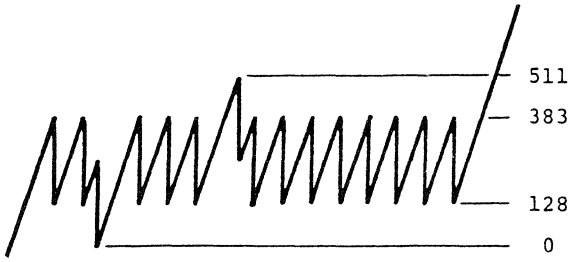


Fig. 6. Still Another Error Waveform.

will now be too high by 128 counts. This can be corrected by a digital subtractor on the output or more conveniently, by adding a voltage offset to the front end of the ADC. The converter with these modifications is shown in Figure 7.

crease, the second encoder goes to 256, which forces the adder output to all zeros! The second encoder will continue to encode until it reaches 511. Figure 8 shows the transfer function of

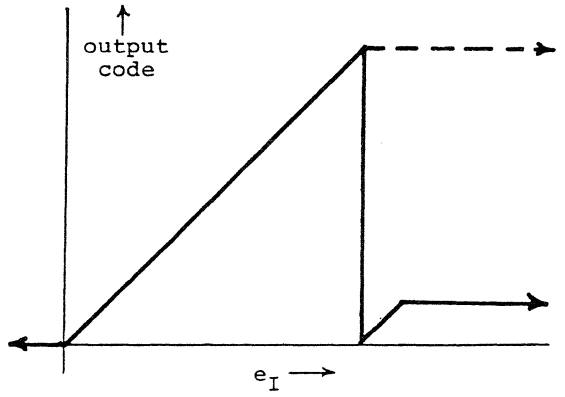


Fig. 8. Need For Overrange Correction.

this ADC, with the dotted line indicating the desired characteristic. The solution to this dilemma is to use the carry from the adder to force all output bits to a logical 1. There are several ways to implement this OVERRANGE CORRECTION, with tradeoffs available between speed and circuit complexity.

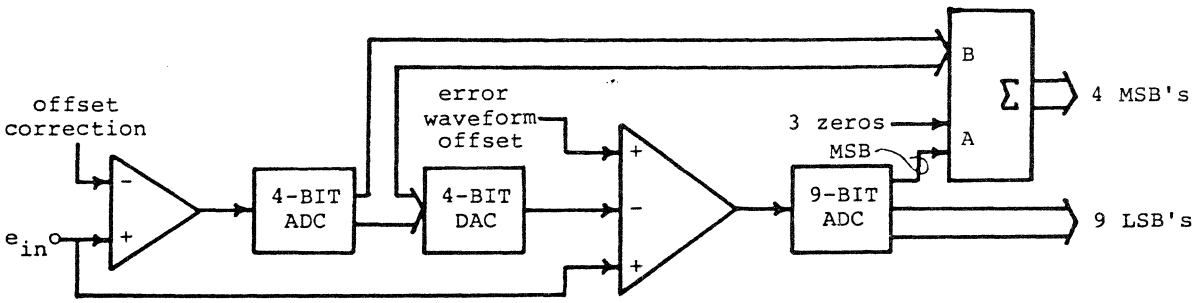


Fig. 7. Basic 12-bit Digitally Corrected Subranging ADC.

The adder would typically be implemented as a '283 for TTL or a '181 for ECL. It could also be implemented using exclusive-or gates. This circuit of Figure 7 still has a problem, although it is not at all obvious. As the waveform approaches full scale, the output will reach 2^N-1 when the second encoder is only at halfscale (255). As the input continues to in-

Implications

With a basic understanding of digital error correction, it becomes easier to take stock of its implications. Relatively simple digital logic removes the constraint of high accuracy from the first stage, allowing use of high-speed, low-accuracy monolithic "flash" converters. In fact, there are

several errors which can be virtually ignored as long as the error waveform remains in the correction range:

- o T/H droop error
- o T/H settling time error
- o 1st stage gain error
- o 1st stage offset error
- o 1st stage linearity error
- o operational amplifier offset error
- o 2nd stage offset error

Figure 9 illustrates the effect of some common errors on the error waveform. Since each waveform shown remains in the correction range, these errors have no effect on the overall converter linearity.

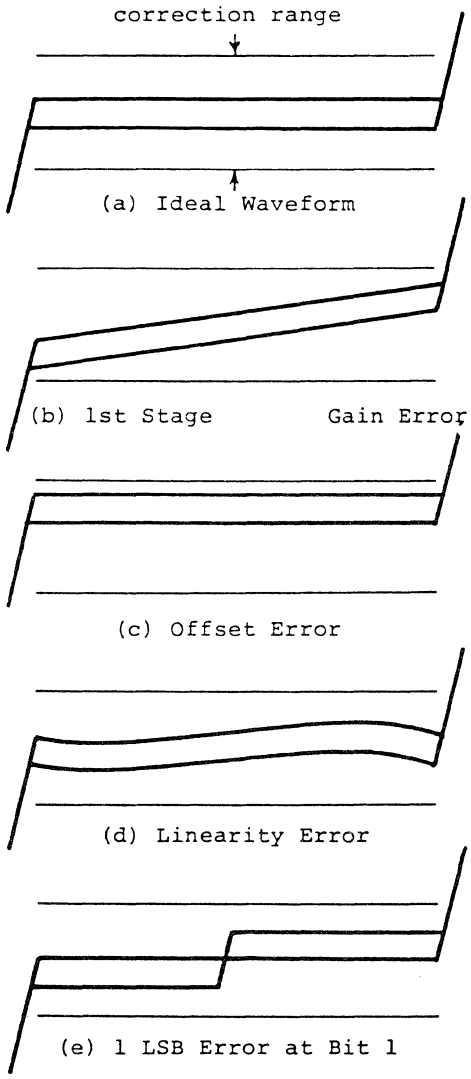


Fig. 9. Correctable Error Waveforms

The advantages of digital error correction are not without cost. Besides digital logic and the larger second encoder, each correcting stage requires three new analog adjustments. The first of these is the gain of the DAC relative to the input. This controls the "tilt" of the error waveform which, ideally, should be flat. The second is the centering of the error waveform in the range of the next stage, or error waveform "offset." The final adjustment is the gain of the error amplifier, which must make each DAC step equal to the appropriate fraction of the range of the next stage. Fortunately, consideration of each adjustment indicates its accuracy need be only somewhat better than the first stage resolution, rather than the total converter resolution.

DESIGN RULES

The first and foremost design rule is this: MAKE THE NUMBER OF BITS IN THE FIRST STAGE(s) AS SMALL AS PRACTICAL. The main reason for this is that the error waveform requires amplification to fit the range of the second encoder properly. Each additional bit in the first stage doubles the required gain; and higher gain requires longer settling time of the error amplifier. The design of this amplifier is generally the primary limitation of the overall converter speed.

A second reason is that a small number of bits in the first stage allows a larger tolerance for T/H errors and offset errors. Since it is possible, for example, to obtain 6- or 8-bit-accurate 4-bit flashes, the encoder error is a relatively small part of the correction range. This allows the majority of the range to be used to correct other errors such as temperature drift. The third reason is that fewer bits in the first stage(s) simplify the error correction circuit and reduce the size of the DAC.

The second design rule is that the overall circuit can be no better than the error DAC(s). A design goal should be that the DAC has an accuracy at least one bit better than the desired accuracy for the total converter. Cur-

rent technology can supply high-speed DAC's with 13-bit accuracy.

Figure 10 shows a general error-correcting encoder stage and the configuration of a k-stage digitally corrected subranging ADC. Of course, the DAC and subtractor for the last stage are not necessary, and an actual implementation might combine the subtraction and gain functions.

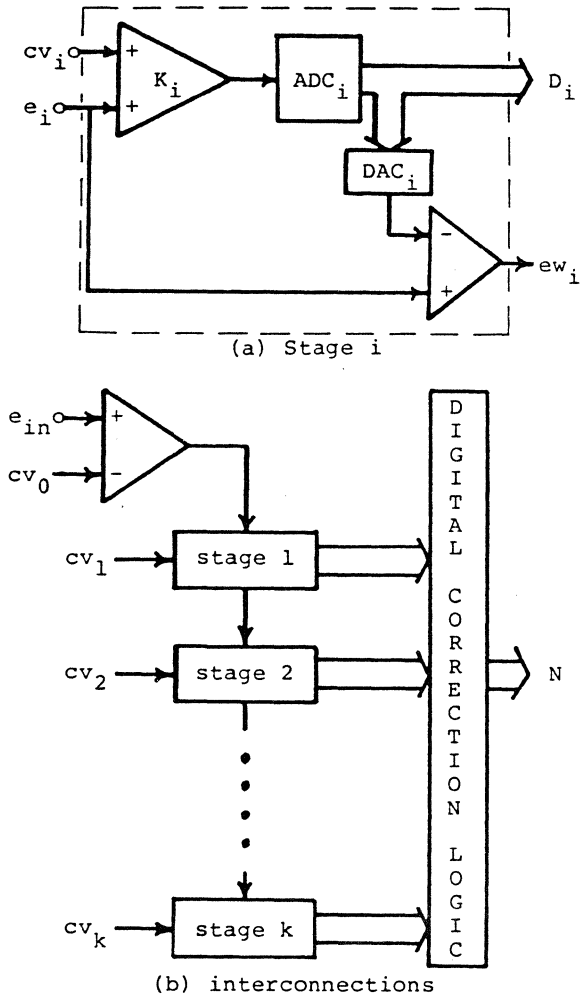


Fig. 10. Multi-stage Correcting ADC.

Table 1 provides definitions and equations for designing a k-stage correcting converter. It is assumed each DAC provides an ideal signal such that the analog output is an error waveform with "teeth" from zero volts to E_i/n_i volts. The equations neglect polarities or offsets, required by real components, which must be controlled by the circuit designer. Also, gains can be obtained in different ways. For example, rather than e_i, the output of the adder with gain K_i could be used to obtain an ew_i of higher amplitude. This would reduce the gain requirement of the next stage error amplifier. Equation 1-8 basically says that the correction bits of stage i are added to the LSB's of the previous stage; that the LSB of this sum is one bit more significant than the most significant non-correcting bit of stage i; and that the output must be limited by OVERRANGE CORRECTION.

Table 1. Digital Correction Design Calculations

k - number of stages.
N_i - number of bits of stage i encoder.
C_i - number of bits of digital correction for stage i (C_1=0).
R_i - range of encoder i in volts.
E_i - range of input voltage e_i.
EW_i - range of output voltage ew_i.
cv_i - error waveform offset voltage for stage i.
cv_0 - input offset correction for total converter.
R_0 - input voltage range for total ADC.
$D(C_i)$ - value of binary word formed by the C_i MSB's of the stage i encoder.
$D(M_i)$ - value of binary word formed by the remaining LSB's of stage i.
D(N) - value of corrected output of the complete converter.

$$n_i=2^{N_i} \quad (1\text{-}1) \qquad c_i=2^{C_i} \quad (1\text{-}2) \qquad N=\sum_{i=1}^{k} N_i-\sum_{i=1}^{k} C_i \quad (1\text{-}3)$$

$$K_i=\frac{R_i}{E_i c_i}=\frac{R_i}{R_0 c_i}\prod_{j=1}^{i-1} n_j \quad (1\text{-}4) \qquad EW_i=\frac{E_i}{n_i} \quad (1\text{-}5)$$

$$cv_i=\frac{(c_i-1)E_i}{2}=\frac{(c_i-1)}{2}\,\frac{R_0}{\prod_{j=1}^{i-1} n_j} \quad (1\text{-}6) \qquad cv_0=\sum_{i=1}^{k} cv_i \quad (1\text{-}7)$$

$$D(N)=\min\left\{2^N-1,\; D(M_k)+\sum_{i=2}^{k}[D(C_i)+D(M_{i-1})]2^{\sum_{j=i}^{k} M_j}\right\} \quad (1\text{-}8)$$

An Example

In order to get an understanding of the equations, an example will be worked. The important numbers are the gain of each input, and each of the offset voltages. These numbers are computed in Table 2.

Table 2. Sample Design Calculations

N=12	k=3	R_0=10
N_1=3	N_2=6	N_3=6
C_1=0	C_2=1	C_3=2
R_1=2	R_2=1	R_3=1

From equation 1-4:

$$K_1 = \frac{2}{10x1} \times 1 = 0.2$$

$$K_2 = \frac{2}{10x2} \times 8 = 0.8$$

$$K_3 = \frac{1}{10x4} \times 8x64 = 12.8$$

From equation 1-6:

$$cv_1 = \frac{(1-1)}{2} \times \frac{10}{1} = 0$$

$$cv_2 = \frac{(2-1)}{2} \times \frac{10}{8} = 0.625$$

$$cv_3 = \frac{(4-1)}{2} \times \frac{10}{8x64} = 0.0293$$

From equation 1-7:

$$cv_0 = 0 + .625 + .0293 = .654$$

Note that two of the computed gains are less than unity. This is due to the input voltage range being substantially greater than the input range of the first stages, and the low number of bits in the first stage. Implementation of these calculations is shown in Figures 11 and 12.

The first two adders, with gains of less than one, would simply be resistive dividers. In the last stage, the subtractor and adder with gain of 12.8 could be combined into one operational amplifier. The correcting adder in Figure 11 would normally be implemented as two 4-bit adders.

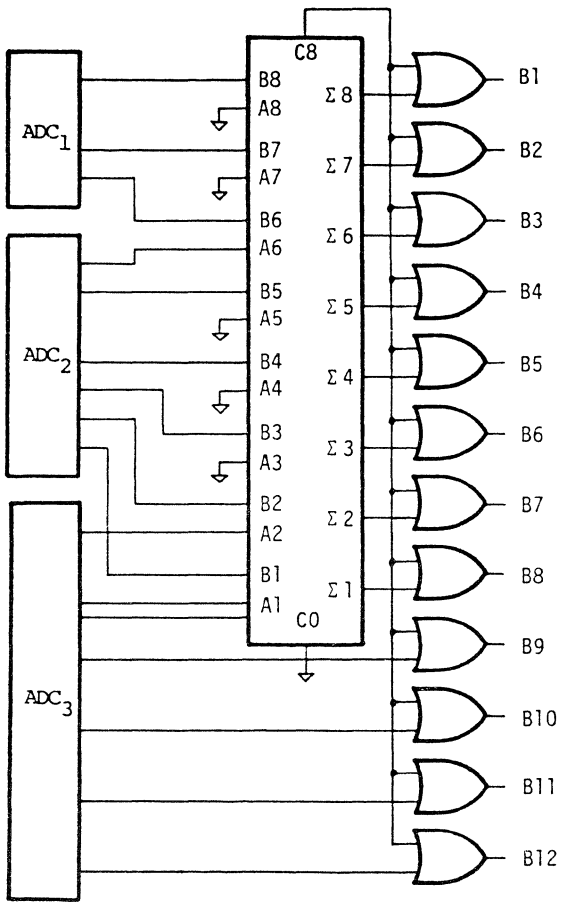


Fig. 11. Implementation of Error Correction.

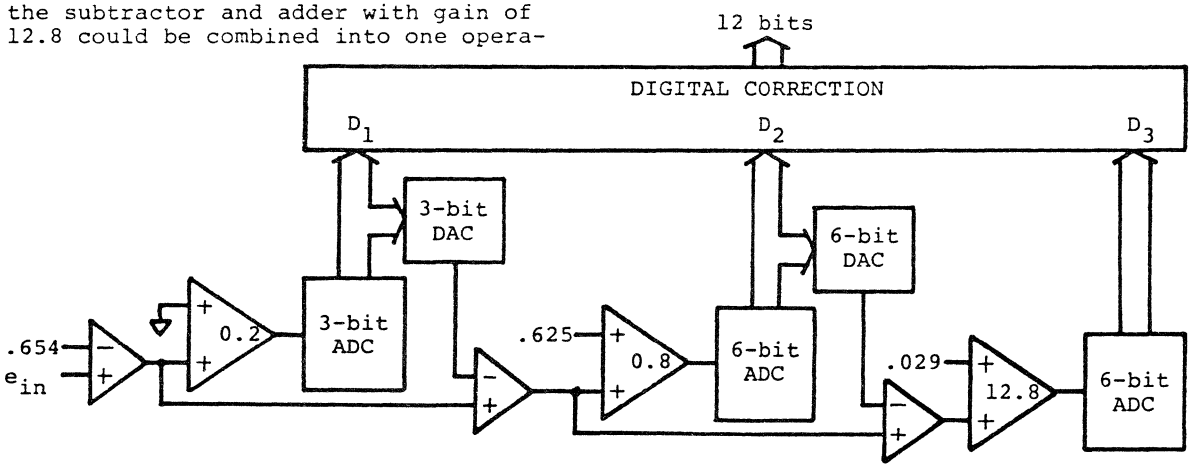


Fig. 12. 12-bit 3-stage Correcting ADC.

SECTION II

DIGITAL VIDEO APPLICATIONS

DIGITAL VIDEO APPLICATIONS

2

BROADCAST VIDEO DIGITIZATION

HIGH DEFINITION TV

MULTIPLEXING AND SWITCHING VIDEO SIGNALS

ELECTRONIC IMAGE PROCESSING

BROADCAST VIDEO DIGITIZATION

In recent years digital techniques have gained widespread popularity in professional video applications such as time base correctors, frame stores and synchronizers, standards converters, special effects generators, etc. These digital "black boxes" take advantage of developments in data conversion, data storage, and DSP to perform functions previously performed by analog technology.

The term "codec" describes the A/D and D/A portion of a typical digital device as shown in Figure 2.2. Certain standards have evolved with respect to television codecs relating to sampling rates and resolution.

In order to discuss these standards, it is first necessary to understand the basics of a color television signal.

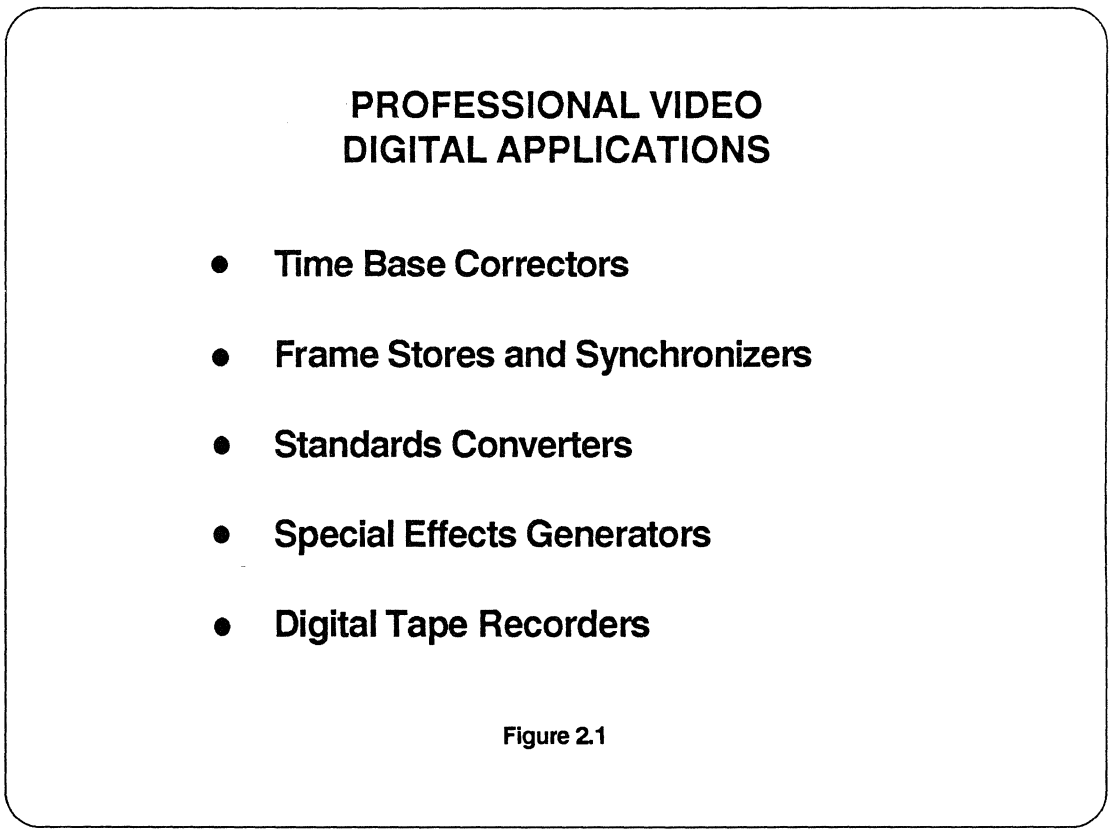
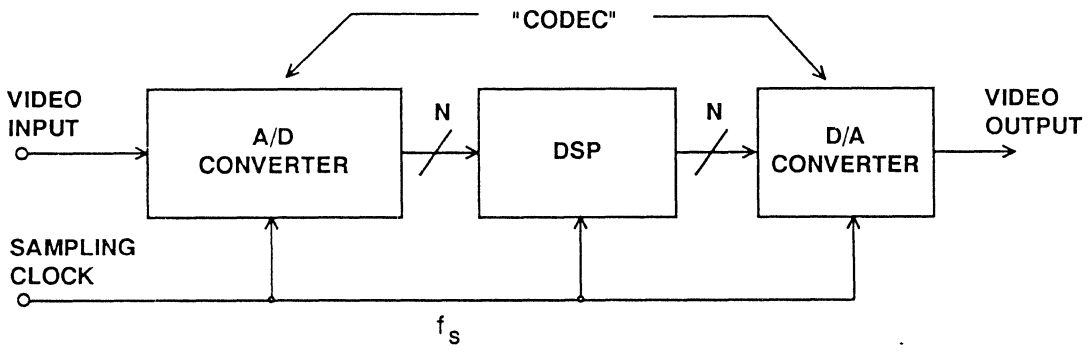


Figure 2.1



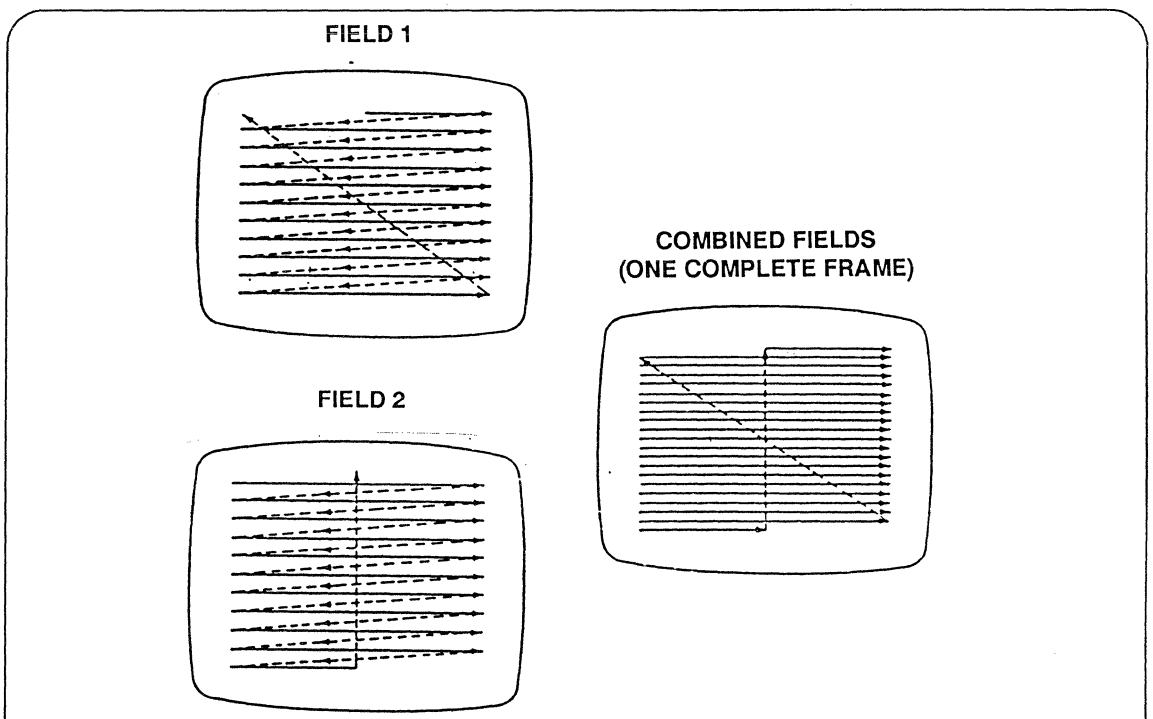
TYPICAL DIGITAL TV DEVICE

Figure 2.2

NTSC Characteristics

The *standard video format* is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera and produces a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light intensity information, synchronization pulses are added to allow the receiving device - a television monitor, for instance - to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even-numbered lines, top to bottom followed by all odd lines (see Figure 2.3). The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker.



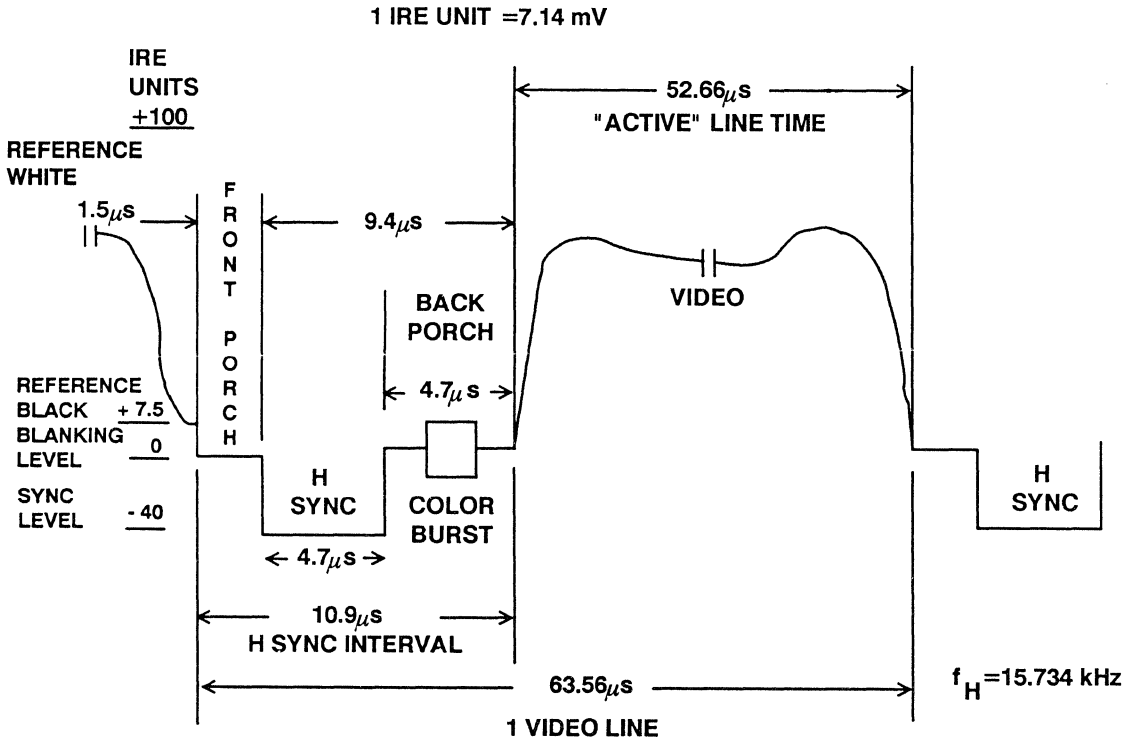
STANDARD TELEVISION INTERLACE FORMAT

Figure 2.3

The original black and white, or *monochrome*, television format specification is the EIA RS-170 specification which prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

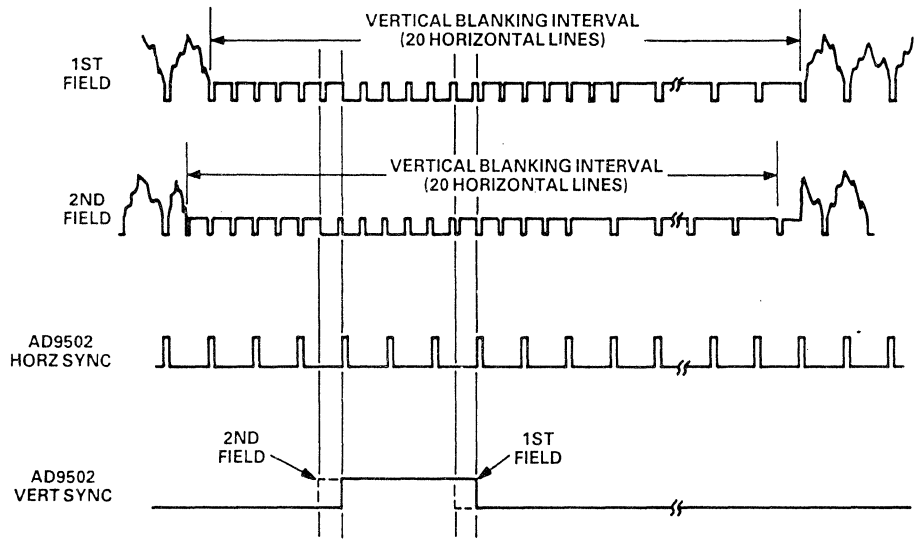
A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one. A single line for the NTSC color video signal is shown in Figure 2.4, and a field timing diagram is shown in Figure 2.5.

Figure 2.6 is a simplified block diagram of the NTSC color processing system. The three color signals (R, G, B) from the color camera are combined in a MATRIX unit to produce what is called the "luminance" signal (Y) and two color difference signals (I and Q). These "components" are further combined to produce what is called the "composite" color signal.



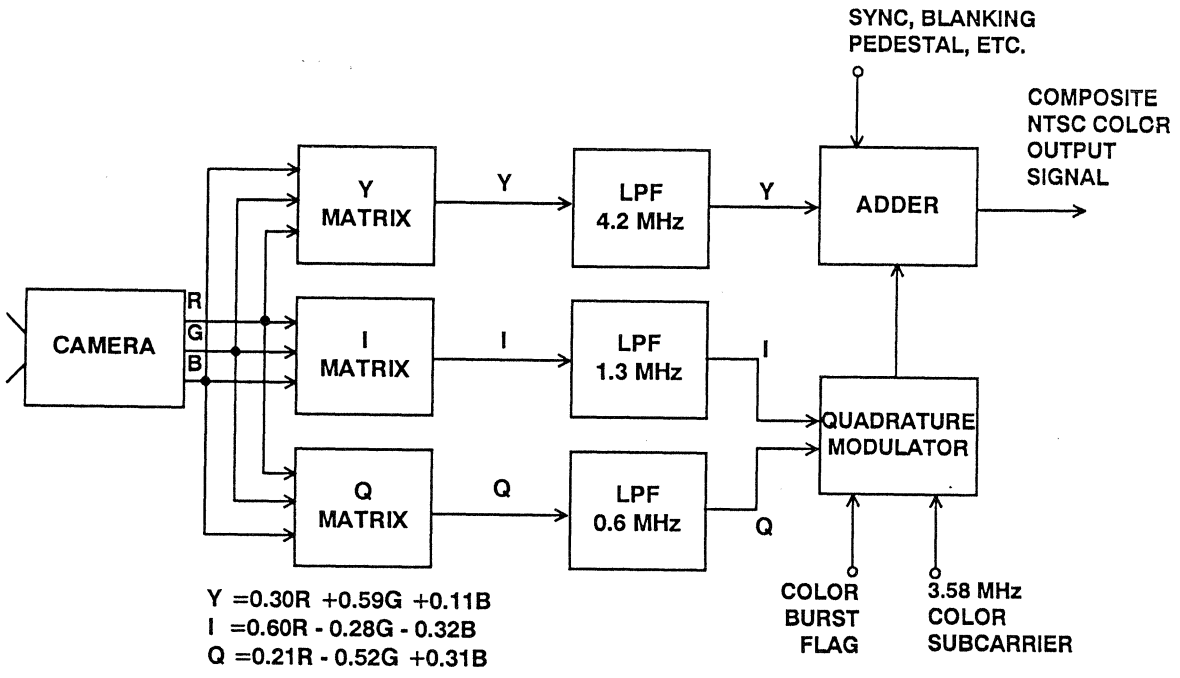
NTSC COLOR VIDEO LINE

Figure 2.4



NTSC FIELD TIMING DIAGRAM

Figure 2.5



GENERATING THE COMPOSITE NTSC COLOR SIGNAL

Figure 2.6

The A/D converter requirements in a digital application depend upon the point at which the video signal is digitized. For digital tape recorders, it is common to digitize the signal at the component level (Y, I Q) using three A/D converters. The sampling rate for the Y channel is typically twice that of the I and Q channel due to the larger bandwidth. Sampling rates of 13.5 MHz are typically used for the Y channel, and 6.75 MHz for the I and Q channel. A resolution requirement of 8 bits is quite common for component digitization. Flash converters such as the AD9048 fulfill these requirements in a cost effective manner.

In many digital television applications it is more desirable to digitize the entire composite NTSC signal. A sampling rate of 14.32 MHz (4 times the color subcarrier frequency of 3.58 MHz) is the accepted standard. The A/D converter resolution requirement is typically 8 bits, although 9 or 10 bits is more desirable if the signal must pass through multiple codecs before leaving the studio environment.

The PAL system is standard for Europe and is similar but not compatible with the NTSC system. The PAL system utilizes 625 horizontal lines (rather than 525 lines for NTSC) and a color subcarrier frequency of 4.43 MHz. The sampling rate requirement is therefore 17.73 MHz for 4x sampling of the composite signal.

Television signals are usually AC coupled, and therefore DC restoration is required ahead of the A/D converter. A track and hold can be used to sample the "back porch" portion of the video line and the DC offset reinserted using an op amp as shown in Figure 2.8. In addition to DC restoration, an anti-aliasing filter is required before applying the signal to the A/D converter input.

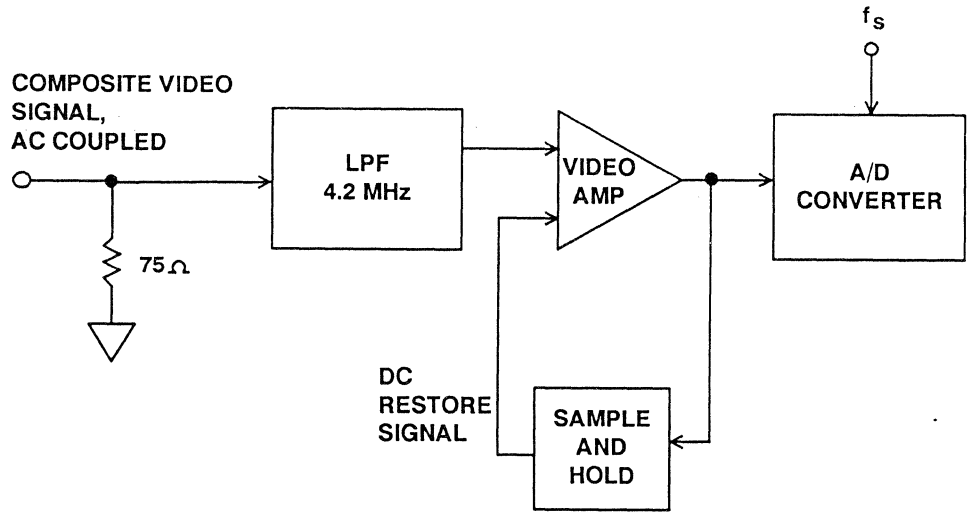
	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58 MHz	4.43 MHz
Composite Signal Sampling Rate	14.32 MHz	17.73 MHz
Frame Frequency	30 Hz	25 Hz
Field Frequency	60 Hz	50 Hz
Horizontal Sync Frequency	15.734 kHz	15.625 kHz

NTSC AND PAL CHARACTERISTICS

Figure 2. 7

Broadcast Video References

- IEEE Standard for Performance Measurements of A/D and D/A Converters for PCM Television Circuits, IEEE Standard 746-1984
- W.A. Kester, "PCM Signal Codecs for Video Applications", **SMPTE Journal**, Vol. 88, Nov. 1979, pp. 770-778.



CONDITIONING THE COMPOSITE VIDEO SIGNAL FOR DIGITIZATION

Figure 2.8

HIGH DEFINITION TV (HDTV)

Recent developments in the evolving field of High Definition TV (HDTV) require higher sampling rates and more resolution than is currently needed for NTSC, PAL, or SECAM. HDTV is touted as offering 35mm film quality video with CD quality audio. The generic requirements of HDTV that have been agreed upon internationally are the following: twice the vertical resolution of current systems, wide-screen aspect ratio, and digital audio. The similarities between systems stops there.

Different HDTV systems have been proposed in Japan, Europe, and the US. The HDTV standards in Japan and Europe are fairly well characterized, while a US standard has yet to be selected. US companies are currently participating in a series of FCC qualifications to select the US standard. It is expected that a final US standard will be established during 1991 or 1992.

Figure 2.9 shows the differences between the Japanese MUSE system (Multiple Subnyquist Sampling Encoding) and the European standard, which was developed by the Eureka-95 committee, and is known as HD-MAC (High Definition Multiplexed Analog Component). Both

MUSE and HD-MAC are designed to be delivered via DBS (Direct Broadcast Satellite) which will be received by small dishes attached to the roofs or windows of Japanese and European homes. This differs from the main means of US delivery, which are cable and terrestrial (i.e., through the air).

Because of the increased resolution of these HDTV systems (twice the vertical resolution and twice the horizontal resolution) there is four times as much data as for conventional TV systems. This increased bandwidth, even after compression, requires A/D converters with faster speeds and wider bandwidths than are needed for NTSC, PAL, or SECAM.

A major reason that HDTV is possible is the growing ability to manipulate TV images once they have been received by TV sets. IDTV (Improved Definition TV) sets are now becoming available with line and frame stores which process NTSC to improve transmission and display quality. Digital storage capability will be used not only for reception processing like ghost cancellation (the elimination of phase-shifted images received due to interference from large objects, see Figure 2.10), but also for advanced services like interactive shopping. In order to facilitate this image manipulation, the received signal must be digitized. Because of the loss of resolution due to ghost cancellation, gamma correction and a host of other

	MUSE	HD-MAC
COUNTRY/REGION	Japan	Western Europe
DELIVERY SYSTEM	DBS	DBS
VERTICAL RESOLUTION	1125 Lines	1250 Lines
FIELD RATE	60 Hz	50 Hz
INTERLACED	2:1	2:1
CHANNEL FREQUENCY	12 MHz	10.5 MHz
AUDIO	Digital	Digital
ADC CLOCK RATE	16.2 MSPS	20.25 MSPS
ADC RESOLUTION	10 Bits	10 Bits

MUSE AND HD-MAC CHARACTERISTICS

Figure 2.9

advanced image processing algorithms that may be implemented, it is generally acknowledged that more than 8-bits of resolution will be required.

NTSC, PAL, and SECAM are transmitted as composite video. Composite video modulates the image information about a number of carrier frequencies. These frequencies are typically confined to a narrow baseband frequency. A major artifact of composite video is crosstalk between the individual color and luminance information. Many HDTV systems use component video. Component video time multiplexes the image information, thereby reducing crosstalk as well as minimizing a number of other transmission related artifacts.

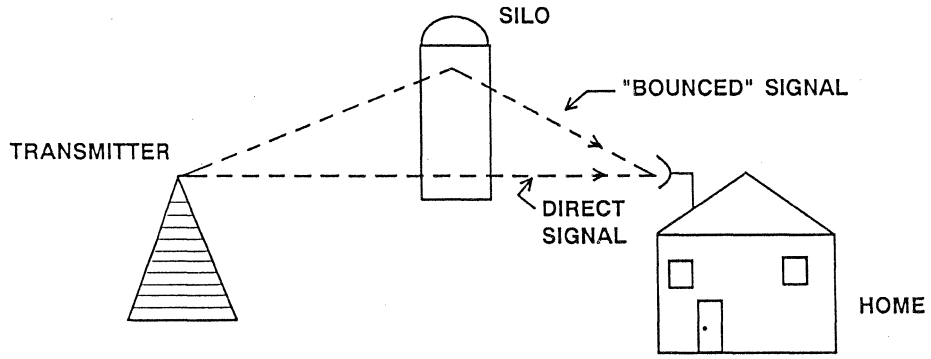
Figure 2.11 shows a block diagram of a typical HDTV system.

Analog Devices is currently working on a number of components for use in HDTV systems. The ADV7121 and ADV7122 are triple 10-bit, 80MSPS DACs which will be used to drive the CRTs of large-screen HDTV sets. Currently under development is the AD773. This 10-bit 20MSPS ADC will be suitable for use in HDTV receiver decoders for MUSE, HD-MAC, and eventually for a US standard. Also available are the AD9020 (10-BITS, 60 MSPS, TTL) and the AD9060 (10-BITS, 75 MSPS, ECL) ADCs for even higher sampling rates. The AD829 op amp is a good choice for HDTV applications due to its exellent differential gain and differential phase performance.

Further reading in HDTV:

Y. Ninomiya, et al., "NHK Proposes High-Definition TV Using MUSE Bandwidth Compression," **Journal of Electrical Engineering**, March 1985, pp. 40-44.

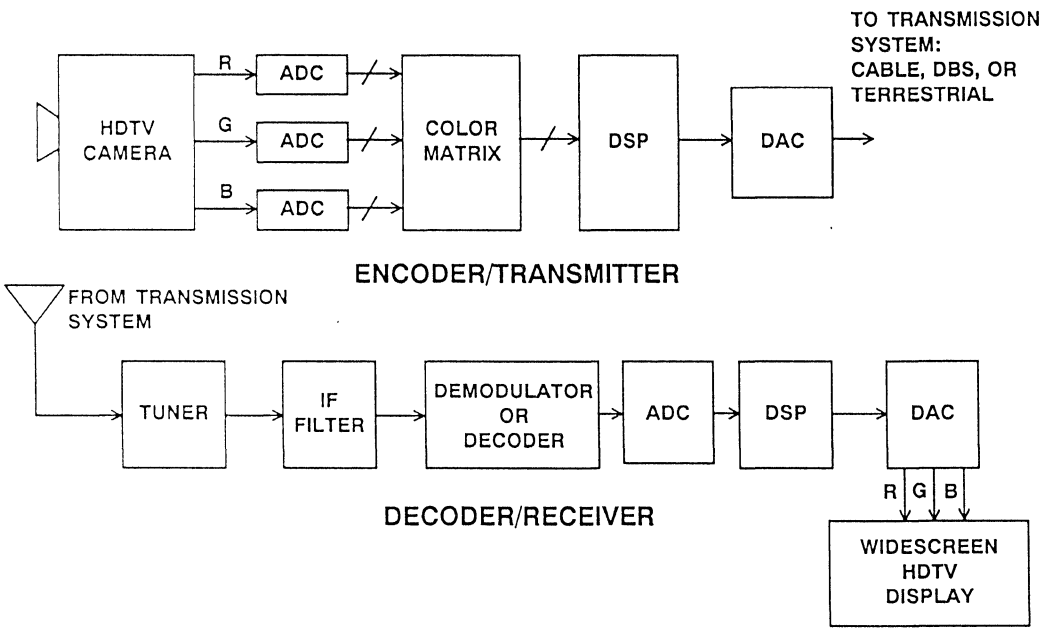
T. Ivall, "Eureka 95 - A World Standard?", **Electronics & Wireless World**, August 1988, pp. 845-850.



- SAME SIGNAL RECEIVED TWICE WITH PHASE DIFFERENCE
- RESULTS IN "GHOST" ON SCREEN
- CAN BE ELIMINATED USING DSP AND 10 BIT ADC

WHY GHOST CANCELLING IS NEEDED

Figure 2.10



TYPICAL HDTV SYSTEM

Figure 2.11

HDTV COMPONENTS

ADC: AD773 - 10 BITS, 20 MSPS
AD9020 - 10 BITS, 60 MSPS (TTL)
AD9060 - 10 BITS, 75 MSPS (ECL)

DAC: ADV7121, ADV7122 } TRIPLE 10-BIT 30, 50, 80 MSPS

AMP: AD829

Figure 2.12

MULTIPLEXING AND SWITCHING VIDEO SIGNALS

There are many applications which require multiple video signals to be routed between several points or switched at high rates into a single output line. The largest application for video multiplexers is professional video signal routing and mixing. Other applications include radar, medical imaging, ECM, instrumentation and electro optics.

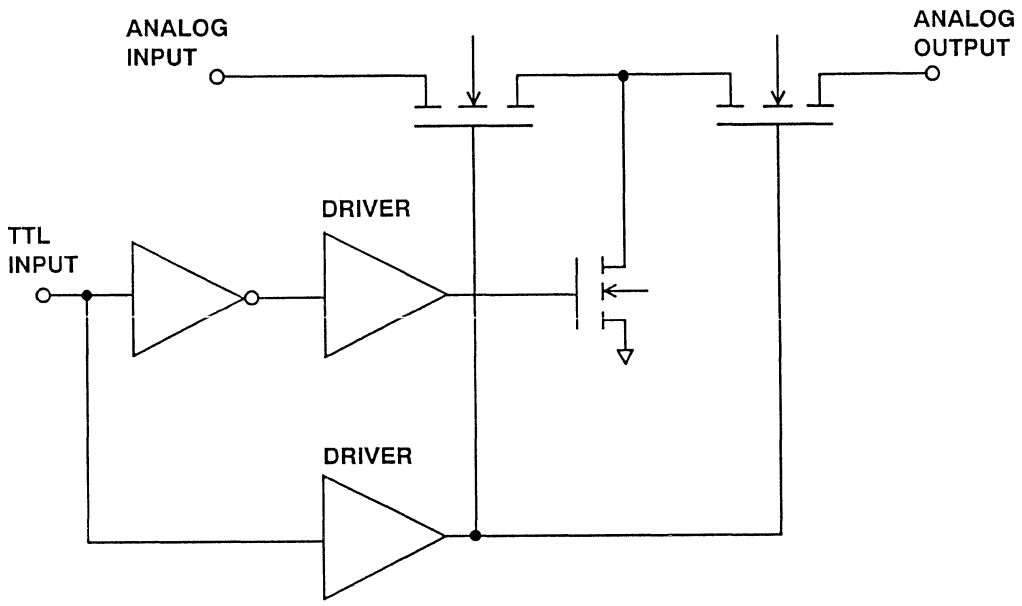
Key specifications for video multiplexers include gain tolerance, bandwidth, switching speed and settling time, channel to channel isolation, differential gain and phase and low power consumption. Individual switches are usually cascaded in a routing switch with a 64 x 16 router being a common configuration in professional video applications. The heart of a video multiplexer is the switch element. Discrete transistors and diodes are often combined in hybrid or modular packages to perform this switching function. DMOS (double diffused MOS) switches can be used in a "T" arrangement as shown in Figure 2.14 to provide the required signal isolation. Switching times of less than 100ns are achievable, but "ON" resistances are limited to about 50 ohms minimum.

The AD9300 4 x 1 wideband video multiplexer offers a totally monolithic bipolar solution with the key specifications shown in Figure 2.15.

VIDEO MULTIPLEXER KEY SPECIFICATIONS

- "On" Resistance
- Bandwidth
- Gain flatness and tolerance
- Crosstalk rejection
- Power consumption
- Cascadable
- Low input capacitance
- Low output impedance

Figure 2.13



DMOS "T" SWITCH

Figure 2.14

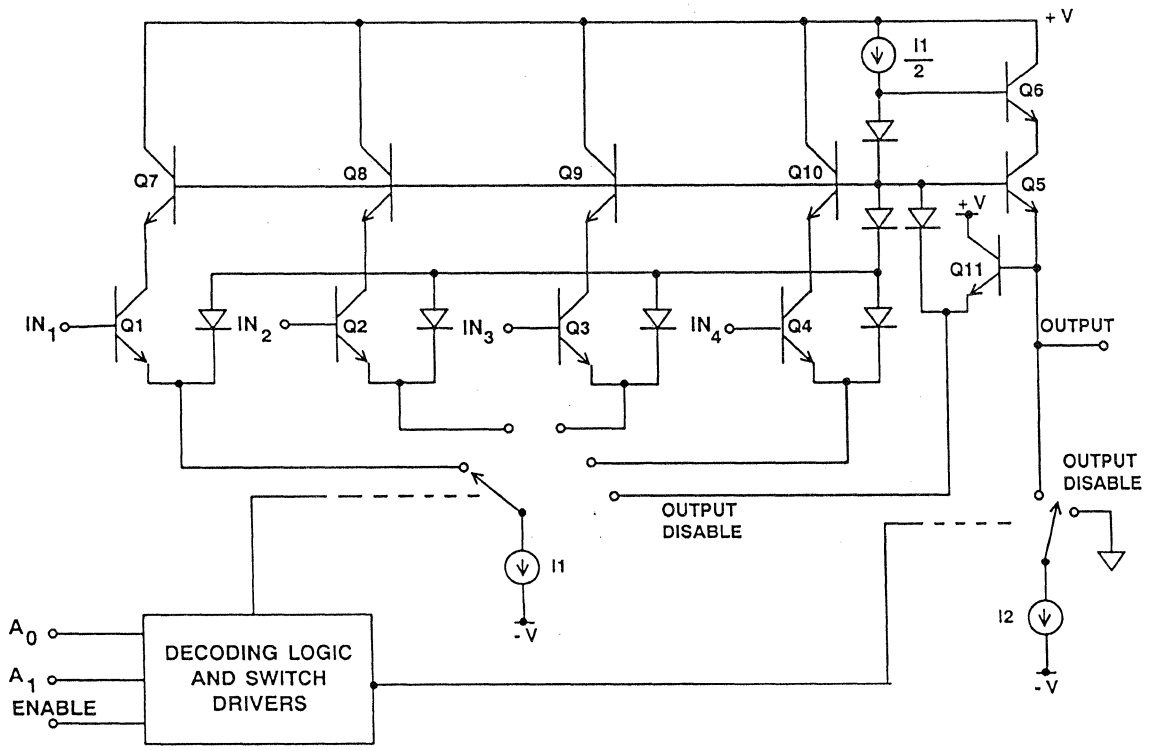
AD9300 4 x 1 Video Multiplexer Key Specifications

- 3 M Ω || 2 pF input impedance
- 34 MHz full power bandwidth, 2V p-p input
- ±0.1dB gain flatness to 8 MHz
- 75 dB crosstalk rejection at 10 MHz
- 0.05%/0.05° differential gain/phase
- 50ns switching time between channels
- 300mW power dissipation (±12V supplies)
- Outputs can be paralleled for switch matrixes
- No "On" Resistance

Figure 2.15

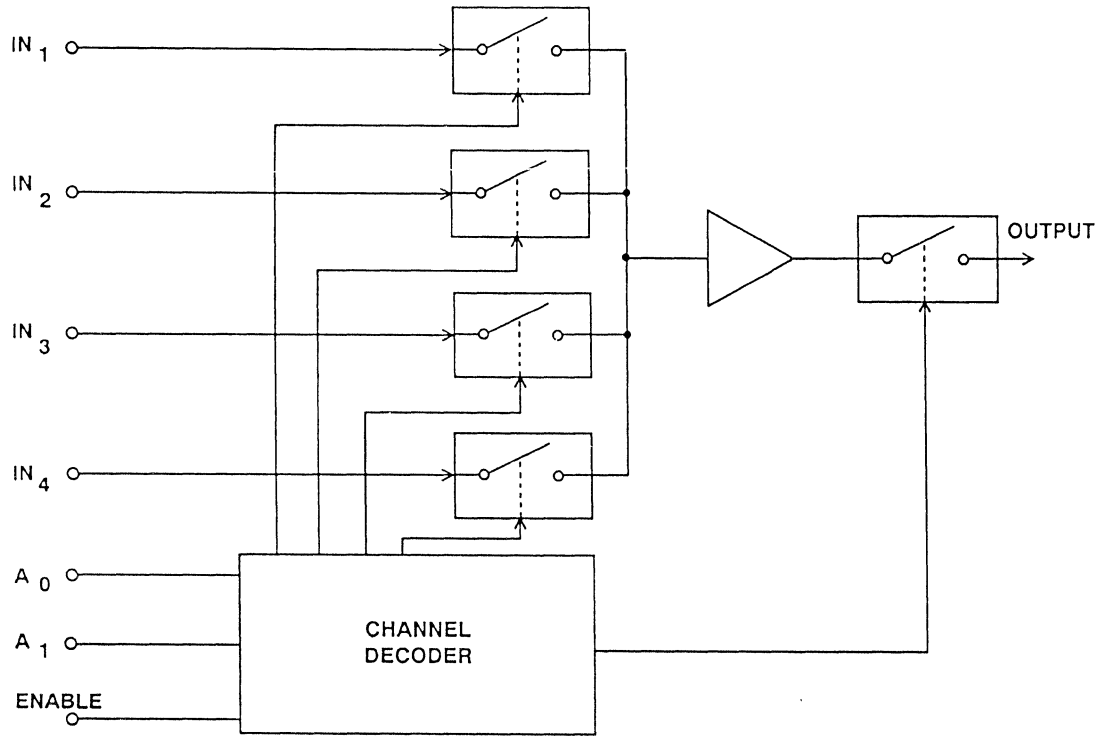
A block diagram of the AD9300 is shown in Figure 2.16. The input channel which is to be connected to the output is determined by a 2-bit TTL digital code applies to A_0 and A_1. The selected input will not appear at the output unless a digital "1" is also applied to the ENABLE input. The output is a high impedance (to allow cascading) if the ENABLE input is a logic "0".

A simplified schematic of the AD9300 is shown in Figure 2.17. Channel switching is achieved by routing the current I_1 to the appropriate cell as determined by the decoding logic. The output is disabled by turning off the current I_2 and routing the current I_1 as shown. The AD9300 achieves its high degree of linearity by utilizing bootstrapped emitter followers in the signal path which are biased at a constant V_{CB} of OV.



AD-9300 SIMPLIFIED SCHEMATIC

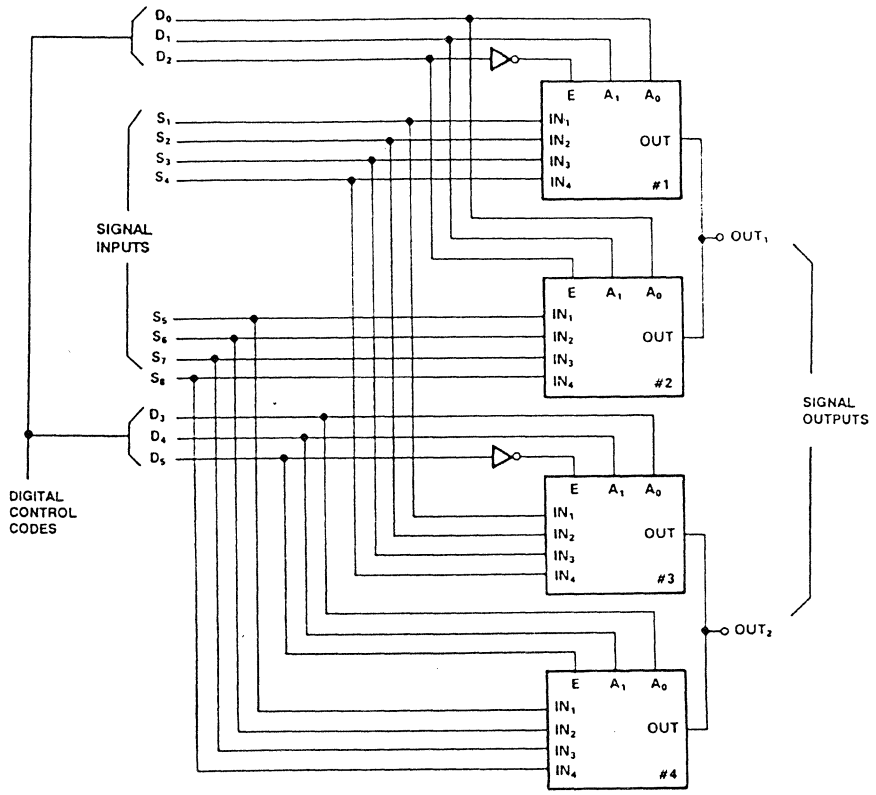
Figure 2.16



AD-9300 BLOCK DIAGRAM

Figure 2.17

Four AD9300 multiplexers can be used to implement an 8 x 2 crosspoint switch as shown in Figure 2.18. The truth table describes the relationships among the digital inputs (D_0 - D_5) and the analog input signals (S_1 - S_8); and which signal input is selected at the outputs (OUT_1 and OUT_2). The number of crosspoint modules that can be connected in parallel is limited by the drive capabilities of the input signal sources. High input impedance (3MΩ) and low input capacitance (2pF) of the AD9300 help minimize this limitation. Adding to the number of inputs applied to each crosspoint module is simply a matter of adding AD9300 multiplexers in parallel to the module. Eight devices connected in parallel result in a 32 x 1 crosspoint which can be used with input signals having 30MHz bandwidth and 1V p-p amplitude.



8 X 2 SIGNAL CROSSPOINT USING FOUR AD9300 MULTIPLEXERS

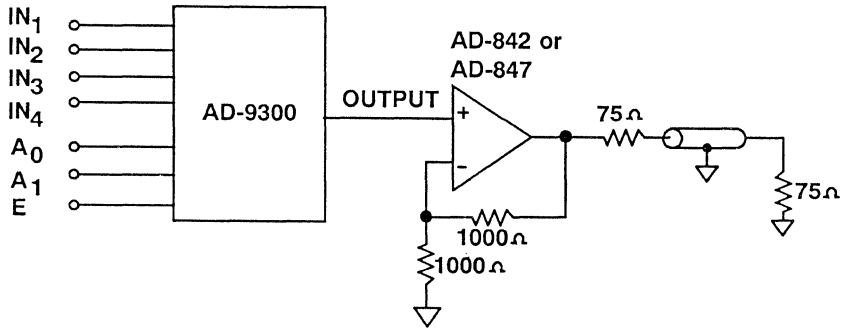
D_2 or D_5	D_1 or D_4	D_0 or D_3	OUT_1 or OUT_2
0	0	0	S_1
0	0	1	S_2
0	1	0	S_3
0	1	1	S_4
1	0	0	S_5
1	0	1	S_6
1	1	0	S_7
1	1	1	S_8

8 × 2 Crosspoint Truth Table

Figure 2.18

The output stage of the AD9300 has an impedance of approximately 10 ohms and is capable of driving a 2kΩ || 10pF load.

For applications such as cable driving, output buffers are recommended as shown in Figure 2.19.



AD-9300 MULTIPLEXER WITH BUFFERED OUTPUT DRIVING 75Ω COAXIAL CABLE

Figure 2.19

ELECTRONIC IMAGE PROCESSING SYSTEM DESCRIPTION AND APPLICATIONS

Computer processing of video images has found wide application in machine vision, pattern recognition, assembly operations, inspection, and graphic arts to name but a few. There are several important differences between an image processing system and the digital systems for broadcast television which were discussed in the previous section.

The first major difference is the lack of standardization in the image processing field. Broadcast television is regulated by the FCC, which rigidly enforces standards and performance requirements at key points in the transmission link. Since an image processing system is entirely self contained, there is no external requirement to conform to any particular standard other than the self-imposed restrictions of the camera itself. The manufacturer is thus entirely free to optimize the system design to achieve the particular performance requirements of the selected markets being addressed.

IMAGE PROCESSOR APPLICATIONS

- Machine Vision
- Pattern Recognition
- Automatic Assembly
- Inspection
- Graphic Arts

Figure 2.20

A second major difference between image processing systems and broadcast television lies in the methods used to synchronize the video signal. In broadcast applications, all cameras and other equipment inside the studio are synchronized to the studio horizontal sync, vertical sync, and color subcarrier signals. In an image processor, however, the synchronization signals are usually derived from the camera itself which serves as the master reference.

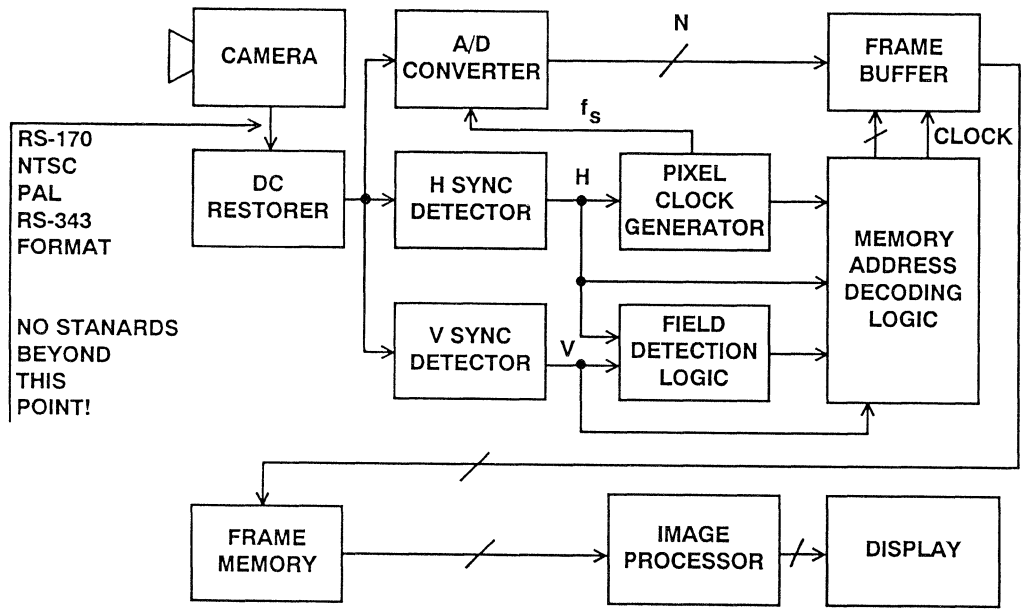
Figure 2.21 shows a block diagram of a typical image processing system. The video signal from the camera is usually AC coupled, therefore a DC restorer is required prior to further signal processing. After DC restoration, horizontal and vertical sync detectors extract the required synchronization signals from the camera video. Some high quality cameras such as CCD cameras provide the H and V sync outputs in addition to the video output. If H and V sync outputs are available from the camera, then the need for the two sync detector circuits is eliminated.

The A/D converter must then digitize the video signal for storage in the frame buffer. Typically 6- to 8-bit flash converters are used for this purpose. A number of factors enter into the process of determining the sampling rate (or pixel clock frequency) which are discussed in detail in the application note: "The AD9502 Video Signal Digitizer and Its Application". The following is a brief summary of the process.

The first step is to determine the vertical and horizontal resolution requirements. The standard RS-170 signal has an aspect ratio of 4:3, i.e., the image is wider than it is tall. The RS-170 frame consists of 525

horizontal lines of which 485 lines contain active video. The remaining 40 lines are allocated to what is called the "vertical interval" which distinguishes between the two interlaced fields of 242 1/2 active lines each.

It is important to determine what the "active" vertical and horizontal video resolution is going to be, since only the "active" video pixels need to be stored in the frame memory. Memory conservation is extremely important in image processors due to cost, power, size, and software complexity.

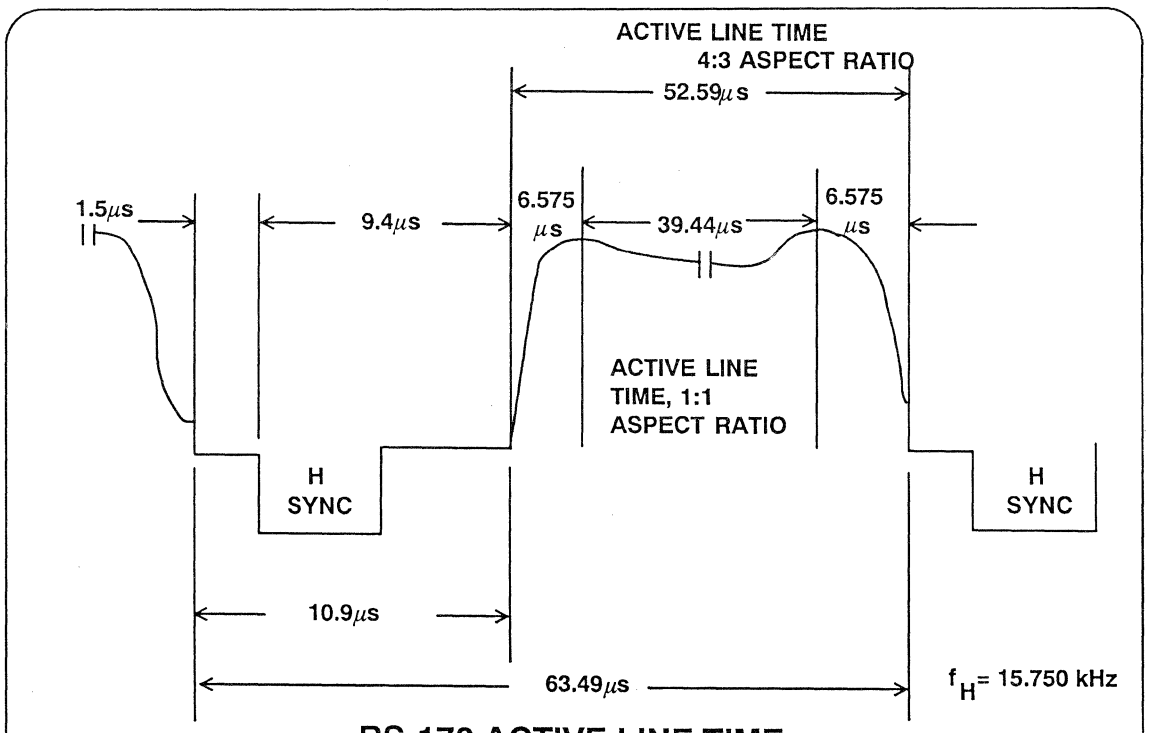


BASIC IMAGE PROCESSING SYSTEM

Figure 2.21

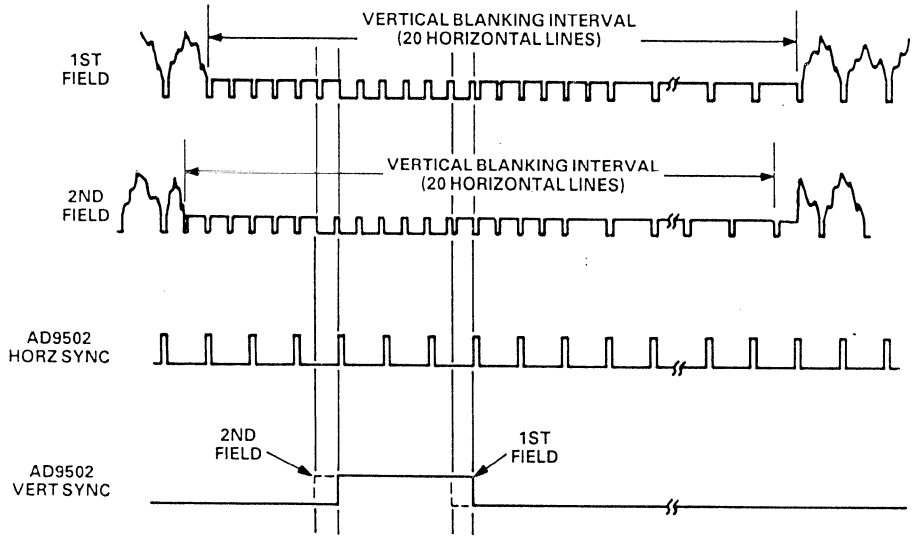
The active video portion of a horizontal line is 52.59 μs for a 4:3 aspect ratio in RS-170. (This is shown in Figure 2.22.) Many image processing algorithms are designed for a 1:1 aspect ratio, in which case the active line time is 3/4 x 52.59 μs= 39.44 μs. This new active line time of 39.44 μs is centered within the 4:3 aspect ratio line of 52.59 μs allowing an "inactive" time of 6.575 μs on either side. The ultimate image will have an aspect ratio of 1:1 appearing with black on either side to fill the entire 4:3 screen.

The active portion of the horizontal line must now be divided into a finite number of picture elements, or pixels. Each pixel on the horizontal line will represent one sample out of the A/D converter, therefore the pixel clock rate is determined by the active line time and the number of desired pixels. For instance, a resolution of 512 pixels per line is common for image processing systems. In an RS-170 system where the aspect ratio is 1:1, the active line time has been shown to be 39.44 μs. The pixel clock frequency can now be calculated by dividing the number of desired pixels (512) by the active line time (39.44 μs) resulting in a pixel clock rate of 12.98 MHz. If the pixel clock frequency is determined by a gated oscillator, the oscillator frequency is simply set to 12.98 MHz. It is often desirable, however, to have the oscillator frequency generated by a phase locked loop (PLL) which is locked to the horizontal frequency of 15.750 kHz. The nearest frequency to 12.98 MHz which is an integer multiple of 15.750 kHz is 12.978 MHz which is 824 times 15.750 kHz. The divide-by-N circuit in the PLL would therefore require N = 824.



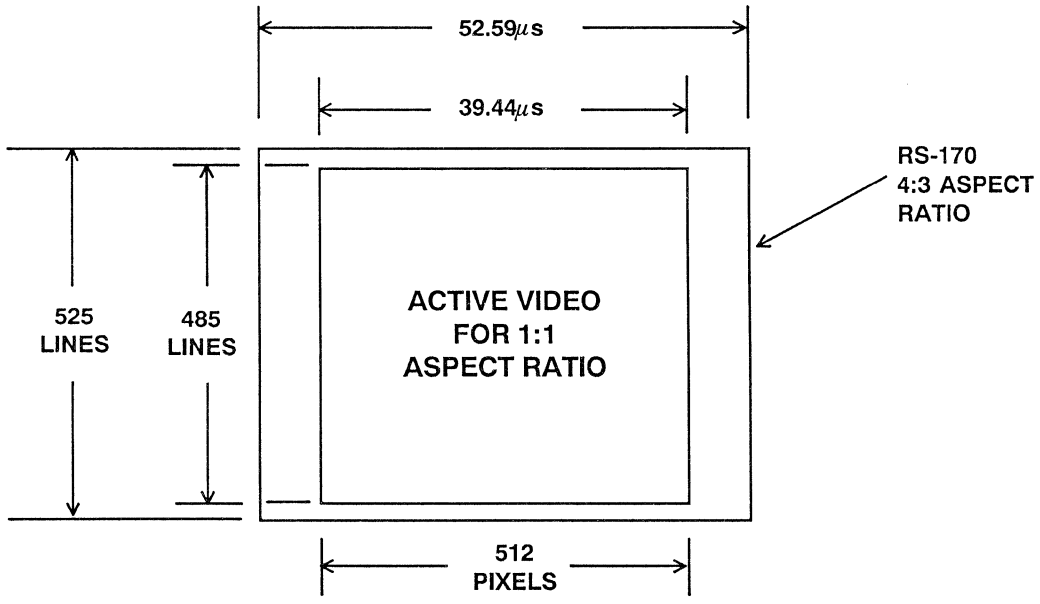
RS-170 ACTIVE LINE TIME

Figure 2.22



RS-170 FIELD TIMING

Figure 2.23



RS-170 ACTIVE VIDEO

Figure 2.24

Referring to Figure 2.21, the purpose of the memory address decoding logic is to gate the A/D converter data to the appropriate memory location in the frame buffer. The field detection logic examines the H and V sync signals and identifies which of the two fields is being processed. Pixel data from the A/D converter is only clocked into the frame buffer during the active line time of the active video lines. Field timing is shown in Figure 2.23, and the active picture area in Figure 2.24.

Image Processing Memory Management

To understand the flow of the digitization process, we start at the vertical sync time. This sync signal indicates that a field is beginning. The field detection logic determines if it is an even or odd field. Assuming it is an even field, a video line counter is set to zero. Digitization starts following the eleven blank video lines and the detection of the successive horizontal sync pulse. Horizontal sync indicates the start of a line. Once detected, the video pixel counter is set to zero and a delay timer times or counts pixels for 9.4 μs (width of remaining horizontal sync interval) plus 6.575 μs (the inactive line time for a 1:1 aspect ratio). At the end of the 15.975 μs delay interval, the sampling process begins occurring repetitively at the interval prescribed by the number of pixels in the line. Once the correct number of pixels have been sampled, sampling stops and the next horizontal sync is awaited. The arrival of the next vertical sync indicates the start of the odd field. The sampling process continues for the odd field as has been previously described for the even field.

If the pixel clock is phased locked to the H sync it will run continuously. The memory address decoding logic contains a number of counters which perform the delay function and clock the A/D converter pixel data into the appropriate address of the frame buffer at the appropriate time.

If the pixel clock is generated using a gated oscillator, the oscillator is started at the detection of the leading edge of the sync pulse. Delay counters are used in a similar manner until the last pixel of the active line time is digitized. The oscillator is then stopped until the next horizontal sync pulse is detected.

MEMORY MANAGEMENT/SYNCHRONIZATION FLOWCHART

- Detect Vertical Sync
- Detect Even or Odd Field
- Count 11 No-Video Lines
- Detect H Sync Pulse for First Active Line
- Count Out 9.4 μs to End of H Sync Interval
- Count Out Inactive Line Time 6.575 μs (For 1:1 Aspect Ratio)
- Count Out and Digitize Active Video Pixels
- Stop Pixel Counter
- Detect H Sync Pulse for Second Active Line
    -
    -
    -
- Stop Active Line Counter After Last Active Line Sync Pulse
- Detect Vertical Sync
- Detect Even or Odd Field
    -
    -
    -

Figure 2. 25

The purpose of this somewhat tedious process of memory management where only active pixels are stored in the frame buffer is illustrated in Figure 2.26. If all pixels are stored in memory and the pixel data sorted in software, a total of 432,600 pixels per frame is required. If a 1:1 aspect ratio is chosen and only the active pixels are stored, a total of only 248,320 pixels per frame are required. The 43% savings in memory is well worth the additional logic required for memory management.

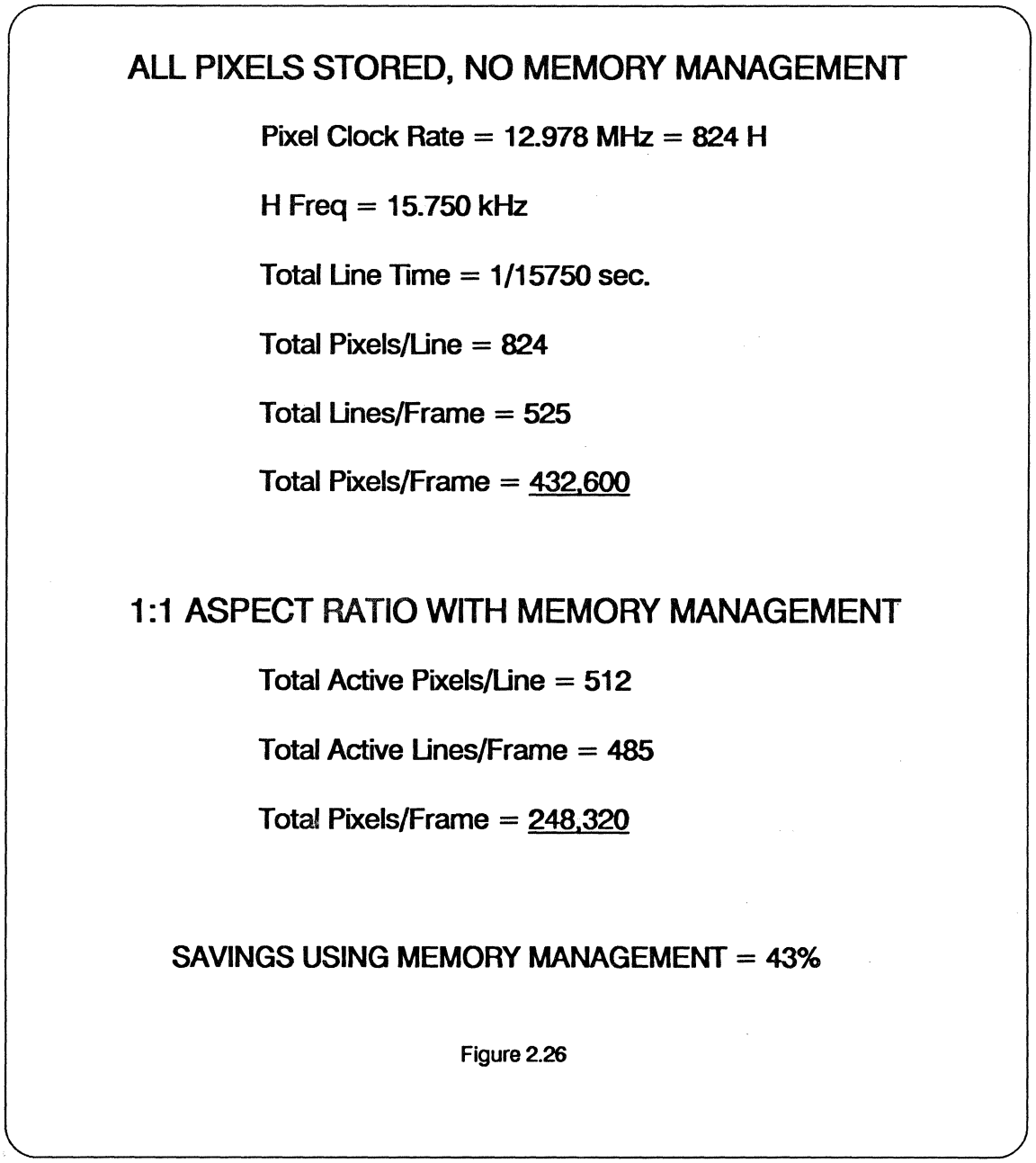


Figure 2.26

AD-9502 RS-170 DIGITIZER DESCRIPTION

The AD9502 hybrid RS-170 digitizer offers a convenient approach to signal conditioning and data acquisition for an image processor. A block diagram is shown in Figure 2.27. The AD9502 consists of four major parts: the phase locked loop (PLL), DC restoration, sync detector, timing circuits, and an 8-bit flash A/D converter.

The PLL comprises a phase detector, loop filter/amplifier, voltage controlled oscillator (VCO), and a digital divider. The frequency of the pixel clock (F_{pc}) is related to the horizontal line frequency (F_H) by the following equation:

$F_{pc} = F_H \bullet 16 \bullet N$, where $28 < N < 62$, N an Integer.

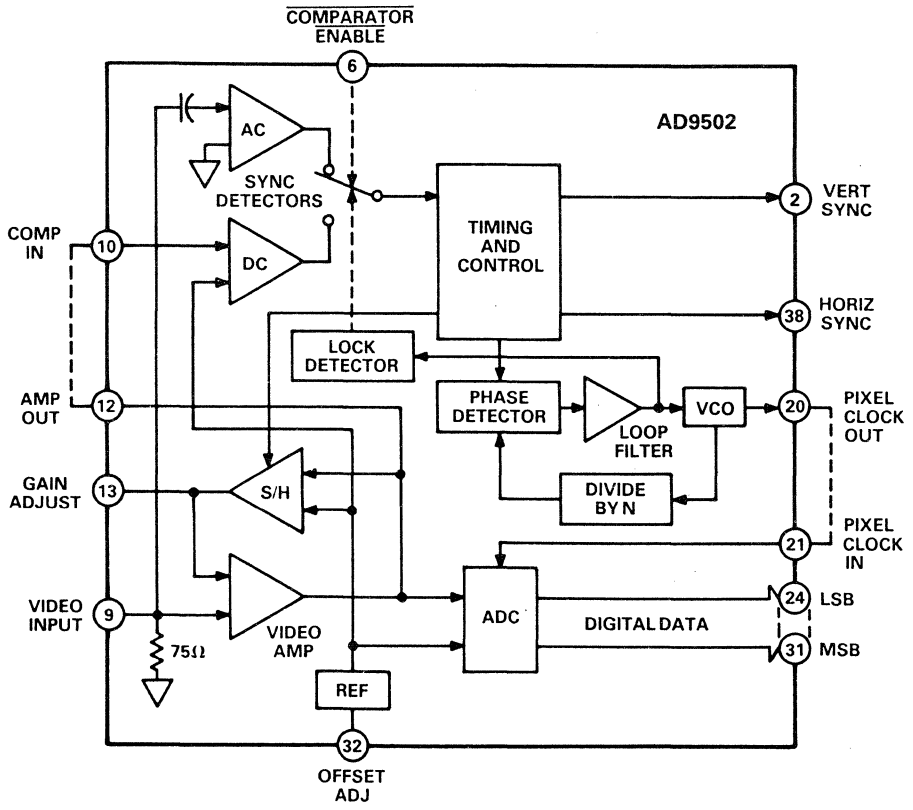
Three values of N are offered as options:

AD9502AM, N = 29, $F_{pc} = 464\ F_H$

AD9502BM, N = 39, $F_{pc} = 624\ F_H$

AD9502CM, N = 51, $F_{pc} = 816\ F_H$

For other values of N, consult the factory.



AD-9502 FUNCTIONAL BLOCK DIAGRAM

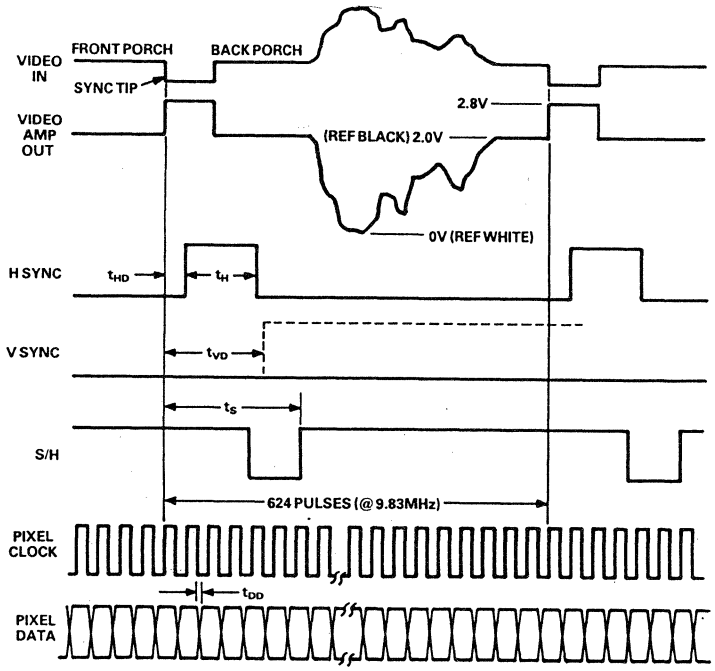
Figure 2.27

The sample and hold video amplifier establishes a feedback loop for DC restoration. Figure 2.28 depicts system timing. The sample pulse for the monolithic S/H amplifier occurs during the back porch of the video signal. When S/H is placed in the hold mode, the output of the S/H produces the proper amount of offset to DC restore the video signal into the range of the flash A/D converter.

During normal operation, sync pulses from the video amplifier drive the PLL after pulse detection and conditioning.

During power up or loss of signal the PLL will be unlocked. The comparator and all pulses are disabled during this time and the AC coupled signal path is enabled, allowing the PLL to synchronize.

The vertical sync pulse is generated whenever the duration of the incoming horizontal sync pulse is longer than 6.6 μs. This pulse is shown with a dashed line in Figure 2.28 to indicate it is present only after the correct number of horizontal lines have occurred.



		µs MIN	MAX
t_{HD}	H SYNC DELAY	−0.4	+0.7
t_H	H SYNC WIDTH	+4.5	+5.4
t_{VD}	V SYNC DELAY	+5.5	+6.7
t_S	SAMPLE DELAY	+7.9	+9.4
t_{DD}	DATA DELAY	+0.02	+0.05

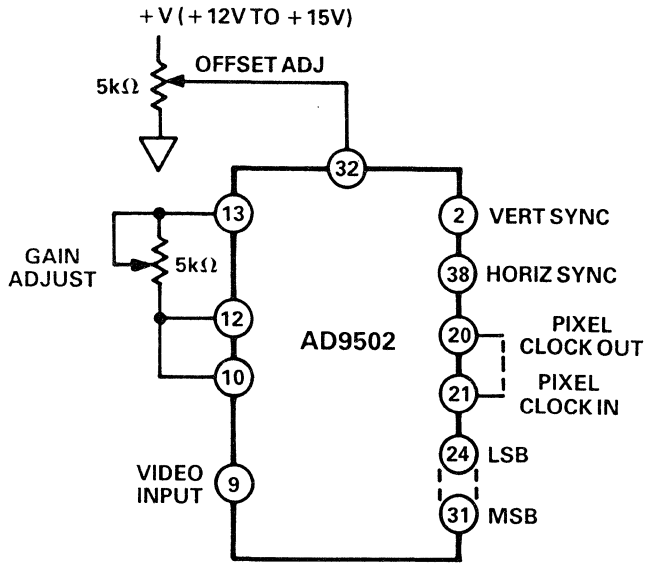
AD-9502 TIMING DIAGRAM

Figure 2.28

Since the RS-170 standard allows for differences in the amplitude and setup (difference between reference black and the blanking level) of the video signals, the AD9502 includes a capability of changing gain 3 dB and varying the offset by 200mV as shown in Figure 2.29.

The internal flash converter provides 8 bits of resolution and digitizes the range from reference white to reference black (sometimes called the "gray scale").

The application of the AD9502 to RS-170, NTSC, and PAL signals is shown in Figure 2.30.



AD-9502 GAIN AND OFFSET ADJUSTMENT

Figure 2.29

AD9502 APPLICATIONS

	RS-170		NTSC		PAL		
F_H (HORIZ. FREQ.)	15.750 kHz		15.734 kHz		15.625 kHz		
ACTIVE LINE WIDTH	52.59 μs		52.66 μs		51.95 μs		
PART NUMBER	PIXEL RATE (MHz)	PIXELS PER LINE	PIXEL RATE (MHz)	PIXELS PER LINE	PIXEL RATE (MHz)	PIXELS PER LINE	PIXEL* RATE
AD9502AM	7.308	384	7.300	384	7.250	377	464 F_H
AD9502BM	9.828	517	9.818	517	9.750	507	624 F_H
AD9502CM	12.852	676	12.839	676	12.750	663	816 F_H

*CONTACT FACTORY FOR PIXEL CLOCK FREQ = $F_H \cdot 16 \cdot N$, WHERE $28 \leq N \leq 50$.

Figure 2.30

SECTION III

SAMPLE AND HOLD AMPLIFIERS

HIGH SPEED SAMPLE AND HOLD AMPLIFIERS

SAMPLE AND HOLDS/ TRACK AND HOLDS

A sample-and-hold amplifier (SHA) is a device that has a signal input, a signal output, and a control input. As the name implies, a SHA has two steady-state operating modes. In the sample (or track) mode, the output tracks the input as faithfully as possible until the hold command is applied to the control input. In the hold mode, the output retains the last value of the input signal that it had at the instant of time the hold command was applied.

By far the largest application for SHAs is driving A/D converters. SHAs are essential for successive approximation or subranging A/D converters where the signal input to the A/D converter must remain stable within 1/2 LSB during the conversion cycle. Significant dynamic performance improvements can sometimes be realized by placing a fast SHA ahead of a flash converter. Other applications for SHAs are: D/A converter deglitchers, simultaneous sampling systems, peak detectors, pulse stretchers, delay lines, and data distribution systems.

Most track and holds and sample and holds are identical in both function and circuit implementation. The only distinction between them is how they are used in the system. A sample and hold implies that the device samples the input for a short time and stays in the hold mode for the remainder of the cycle. A track and hold, on the other hand, spends most of the time tracking the input and is switched into the hold mode for only brief intervals. In data acquisition systems operating at sampling rates greater than 1 MHz, the terms sample and hold and track and hold lose their distinction. In the following discussion the terms will therefore be used interchangeably.

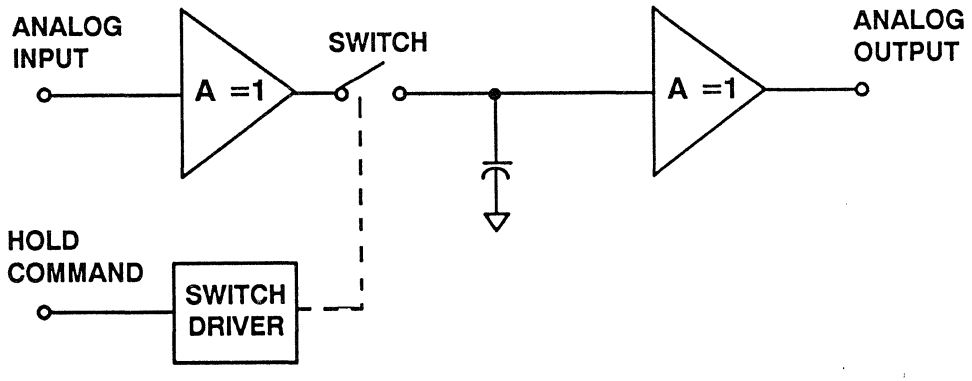
SAMPLE-AND-HOLD APPLICATIONS

- A/D Converter Drivers
- D/A Converter Deglitchers
- Data Acquisition Systems
- Data Distribution Systems
- Simultaneous Sampling
- Peak Detectors
- Analog Delay Lines

BASIC SHA OPERATION

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (hold capacitor), output buffer, and switching circuits are common to all SHAs, as shown in the typical configuration of Figure 3.1.

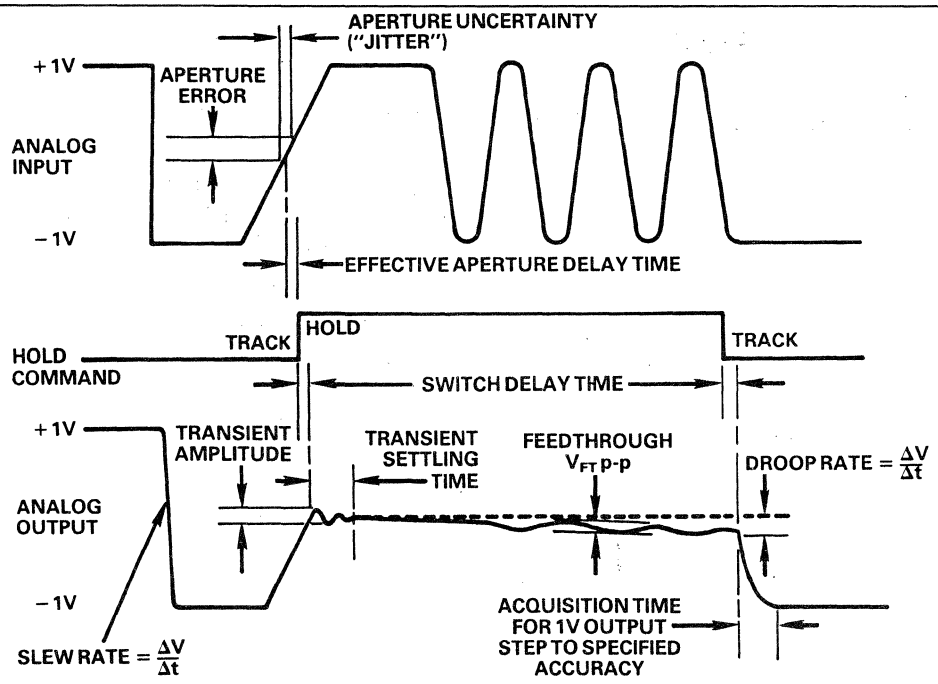
The energy-storage device, the heart of the SHA, is almost always a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to charge the hold capacitor. In the track mode, the hold capacitor usually determines the frequency response of the device; in the hold mode, the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the hold capacitor is alternately switched between track and hold.



BASIC SHA

Figure 3.1

There are four groups of specifications that properly describe SHA operation. They are the static and dynamic characteristics that describe operation in and between the track and hold modes. Unique to SHAs are the dynamic specifications that describe the transitions from track to hold, and hold to track. An understanding of the terminology used to describe these devices is of key importance to the proper selection and use of SHAs. Figure 3.2 shows errors (exaggerated) during a complete cycle from track to hold and back.



SOURCES OF ERROR (EXAGGERATED) IN A SAMPLE-HOLD

Figure 3.2

TRACK MODE SPECIFICATIONS

While in the track - or sample - mode of operation, the SHA is simply a limited-bandwidth amplifier that may or may not provide gain. Operation in this mode is described by the same specifications that are used to characterize any analog amplifier. Indeed, many SHAs are little more than an operational amplifier with a capacitor and a switch. The principal specifications used to describe sample-mode operation are:

OFFSET - That error which adds to the actual input to displace the transfer characteristics of the SHA from the ideal. It is usually measured referred to the input.

NONLINEARITY - The amount by which the plot of output vs. input deviates from a "best straight line". It is usually specified as a percentage of full scale.

GAIN - The multiplication factor describing the input to output DC transfer function.

SETTLING TIME - The time required for the output to attain its final value within a specified fraction of full scale when a full scale analog input step is applied.

BANDWIDTH - Describes the frequency response in terms of output attenuation over frequency; it is usually characterized by the -3 dB value.

SLEW(ING) RATE - The maximum rate of change of the output voltage when an analog step is applied, either as an input step or by a hold-to-sample transition.

TRACK-TO-HOLD TRANSITION SPECIFICATIONS

The specifications used to describe the transition from track to hold and from hold to track seem to be the most confusing to users of SHAs. These terms are unique to SHA devices and deserve special attention. Perhaps the most misunderstood and misused specifications are those that include the word "aperture" in their definition.

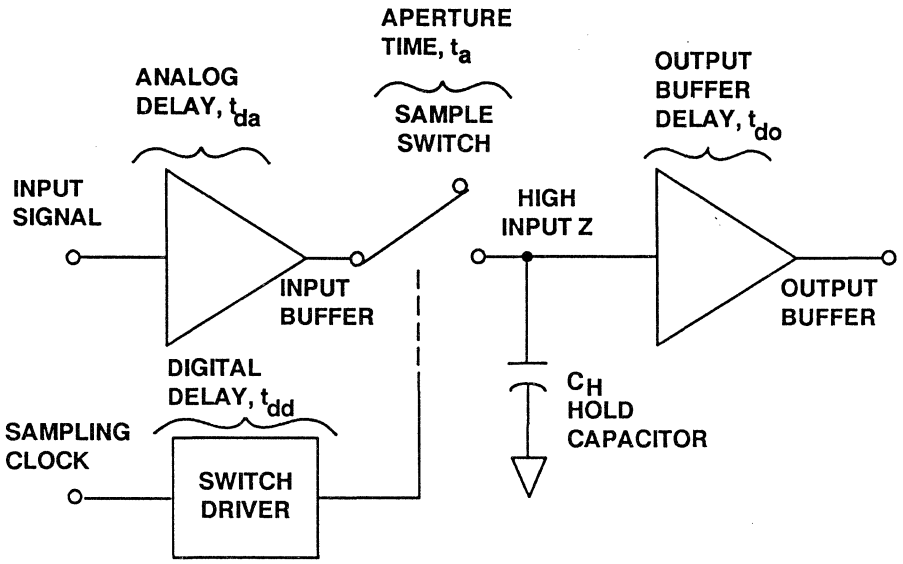
APERTURE TIME - The most essential dynamic property of a SHA is its ability to quickly disconnect the hold capacitor from the input buffer amplifier. The short (but non-zero) interval required for this action is called aperture time. The actual value of voltage that gets held at the end of this interval is a function of both the input signal and the errors introduced by the switching operation itself.

SAMPLE-TO-HOLD OFFSET OR PEDESTAL - There is a step error, which causes the held value to differ from the last value in sample; it is caused by charge dumped onto the hold capacitor via stray capacitance from the switch-control circuit. A design objective is to keep this error, resulting from a non-ideal switch, independent of the input signal level; the degree to which it in fact deviates from a constant over the input signal range can result in nonlinearities in the output with respect to the input signal. The constant offset portion of the error, called charge transfer, or offset step, can be compensated by coupling a signal of opposite phase onto the hold capacitor through an auxiliary switching circuit and compensation capacitor.

Thus, the sample-to-hold offset, or pedestal, specification depends on the actual device configuration. For SHAs having fixed internal hold capacitance, it includes the residual uncorrected step and the offset nonlinearity. For SHAs requiring external capacitors, it is the residual step error after the charge transfer is accounted for and/or cancelled. In a device for which the capacitance can be chosen by the user, these effects can be reduced by increasing the capacitance in proportion, but at the cost of increased acquisition time.

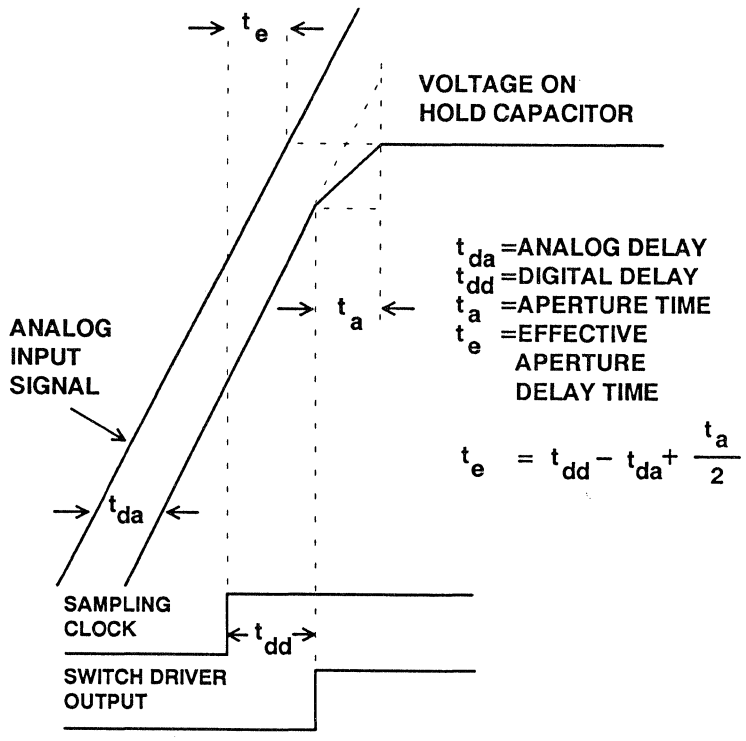
APERTURE DELAY (Or, more descriptively, *EFFECTIVE APERTURE DELAY TIME*) - This specification is important because it helps the SHA user know when to strobe the device with respect to the input signal timing. Figure 3.3 shows the sequence of what happens when the hold command is applied with an input signal of arbitrary slope (for clarity, the sample to hold offset error and switching transients are ignored). The value that finally gets held is a delayed version of the input signal, averaged over the aperture time of the switch. Effective aperture delay time is defined as the interval between the leading edge of the hold command and the instant when the input signal was equal to the held value. This is a more useful specification than aperture time alone, because it includes the effects of the analog and digital propagation delays, as well as the aperture time.

The formula in Figure 3.4 is based on the assumption that the value of voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance (aperture time).



IDEALIZED SAMPLE-AND-HOLD CIRCUIT

Figure 3.3



SAMPLE-AND-HOLD WAVEFORMS

Figure 3.4

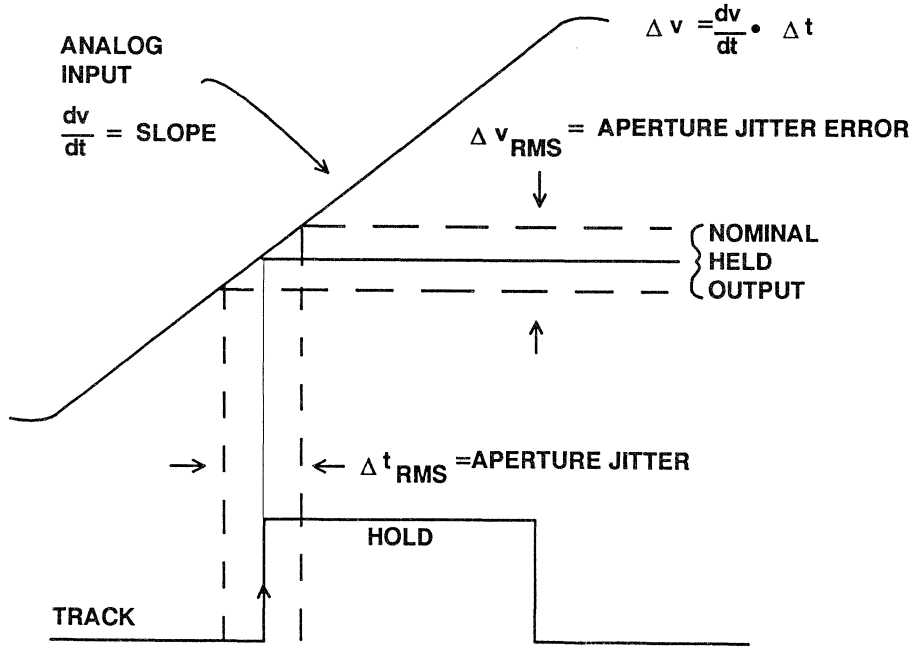
APERTURE UNCERTAINTY (JITTER) - Aperture uncertainty, or "jitter", is the result of noise which modulates the phase of the hold command. This jitter shows up as a sample to sample variation in the value of the analog signal which is being "frozen".

Aperture uncertainty manifests itself as an aperture error, as shown in Figure 3.5. The amplitude of the error is related to the rate of change of the analog input. For any given value of aperture uncertainty, aperture error will increase as the input dv/dt increases.

SWITCHING TRANSIENT - As shown in Figure 3.2, most SHA specifications include the maximum amplitude and duration of the transient that appears at the output as a result of the sample-to-hold transition. A similar transient appears during the hold-to-sample transition but is usually not noticeable because of the dominant effect of acquisition time.

SWITCH DELAY TIME - The interval between the edges of the hold command and the beginning of change of state at the analog output. This delay, as shown in Figure 3.2, occurs at both the sample-to-hold and hold-to-sample transition.

3



EFFECTS OF APERTURE JITTER ON SHA OUTPUT

Figure 3.5

HOLD MODE SPECIFICATIONS

During the hold mode there are errors due to imperfections in the switch, the output amplifier, and the hold capacitor.

DROOP - A constant drift of the output voltage due to charge leakage from the hold capacitor through the switch, output buffer, circuit board or substrate - or within the capacitor itself (dV/dt = I/C). This error can be reduced by increasing the hold capacitance (at the cost of increased acquisition time) and/or reducing leakage currents by component choice, component placement, and shielding or guarding. When droop is caused by diode leakage currents it will double with every 10°C temperature rise.

FEEDTHROUGH - The fraction of input signal that appears at the output in hold, caused primarily by capacitance across the switch. Usually measured by applying a full scale sinusoidal input at a fixed frequency (e.g., 20V peak to peak at 10 MHz) and observing the output during hold.

DIELECTRIC ABSORPTION - The tendency of charges within a capacitor to redistribute themselves over a period of time, resulting in "creep" to a new level when allowed to rest after large, fast changes. This effect, less than 0.01% for good polystyrene and teflon capacitors, can be as large as several percent for ceramic and mylar capacitors. Dielectric absorption can therefore become the dominant error in SHAs when care is not taken with the choice of the capacitor.

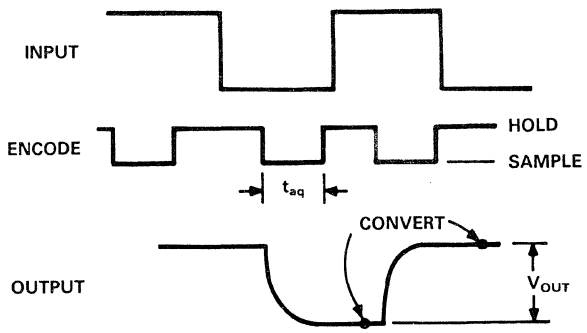
HOLD TO TRACK TRANSITION SPECIFICATIONS

ACQUISITION TIME - The length of time during which the SHA must remain in the sample mode in order for the hold capacitor to acquire a full scale step input; adequate acquisition time makes it possible for the subsequent hold mode output to be within a specified error band of the final value.

Acquisition time is a key SHA dynamic specification. The maximum sample rate of any SHA is limited by the sum of the time intervals required for the sample and the hold modes. The interval spent in the hold mode (after transients have settled) is primarily determined by the system in which the SHA is used. The minimum time spent in the sample mode, however, is established by the sample hold's acquisition time for a given degree of accuracy.

When acquisition time is measured as the interval from the hold to sample transition to the instant when the output buffer has settled, the resulting value of acquisition time is generally pessimistic. As defined, acquisition time measures the time required to acquire the signal at the hold capacitor, not necessarily at the output of the buffer (unless they are the same). For devices in which the hold capacitor is buffered by a follower, rather than used as an integrator (see the next section), a measurement at the output includes output buffer settling time as well as switch delay time. In practice, the voltage has already settled at the hold capacitor, and a hold command can be applied before the output buffer completely settles.

There is a method of determining acquisition time which is independent of output buffer effects. Figure 3.6 shows the waveforms involved. The input analog square wave is sampled and converted at twice the analog square wave frequency with relatively narrow sample pulses. The figure indicates that, on the transition to sample, the output starts to change, in order to follow the step input. Initially set wide enough for the signal to be accurately acquired, the pulsewidth, t_{aq}, is reduced until the output waveform measured directly, begins to collapse to some defined percentage of full scale. When that occurs, the width of the sample pulse is equal to the acquisition time, because the hold capacitor can no longer acquire the signal accurately with further reduction in t_{aq}. If the output is being observed with an oscilloscope, it is possible to make this measurement on high vertical sensitivity settings even if the scope is being overdriven severely.



ACQUISITION-TIME MEASUREMENT WAVEFORMS

Figure 3.6

SAMPLE AND HOLD SPECIFICATIONS

TRACK MODE

STATIC

- Offset
- Nonlinearity
- Gain

DYNAMIC

- Settling Time
- Bandwidth
- Harmonic Distortion
- Slew Rate

TRACK TO HOLD TRANSITION

STATIC

- Pedestal
- Pedestal Nonlinearity

DYNAMIC

- Switch Aperture Time
- Effective Aperture Delay Time
- Aperture Jitter
- Switch Delay Time
- Switching Transient

HOLD MODE

STATIC

- Droop
- Dielectric Absorption

DYNAMIC

- Feedthrough

HOLD TO TRACK TRANSITION

DYNAMIC

- Acquisition Time
- Switching Transient

HIGH SPEED OPEN LOOP SHAS

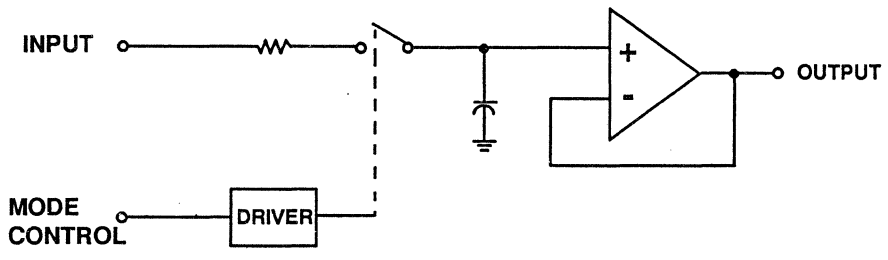
Most SHA designs fall into one of two categories: open or closed loop circuits. Closed loop SHAs exploit the accuracy, low drift, and gain flexibility available with operational amplifiers. Open loop designs take advantage of the high speed characteristics of unity gain buffer amplifiers.

Figure 3.7 shows the conceptually simplest SHA circuit. When the switch is closed, the capacitor charges exponentially to the input voltage, and the amplifier's output follows the capacitor's voltage. When the switch is opened, the charge remains on the capacitor. The capacitor's acquisition time depends on the series resistance and the current available to charge the capacitor. Once the charge is acquired to the appropriate accuracy, the switch can be opened, even though the amplifier has not yet settled, without affecting the final output value.

A disadvantage of this circuit is that the switched capacitor dynamically loads the input source, which may not have low enough output impedance and sufficient current-drive capacity. The circuit of Figure 3.8 is similar but includes an input buffer amplifier to isolate the source. The Analog Devices HTS-0025 and HTS-0010 SHAs use this scheme to achieve acquisition times as low as 10ns. These designs utilize a high speed diode switching bridge for sampling wide bandwidth signals at update rates of up to 50 MHz as shown in Figure 3.9. The high speeds are achieved by employing buffer amplifiers that do not use voltage feedback; the nonlinearities of these amplifiers limit their use to systems requiring resolutions of 12 bits or less.

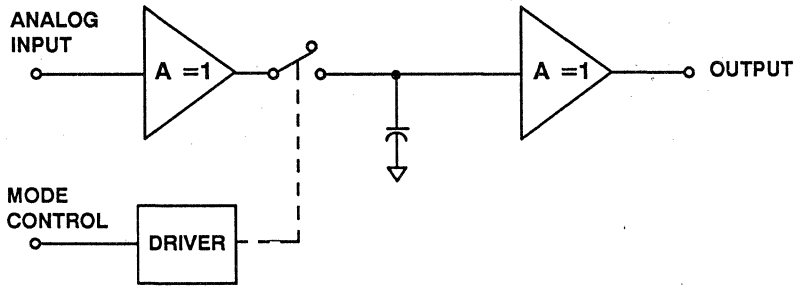
The HTS-0010 is an example of a SHA that has the hold capacitor's active terminal brought out so that additional capacitance can be employed to improve the droop rate and sample-to-hold offset (at the expense of bandwidth and acquisition time, as noted earlier).

SHA specifications and terminology are generally applicable to both open loop and closed loop SHAs. Applications requiring update rates higher than 10 MHz and acquisition times less than 100ns usually require open loop circuits. At these speeds, subtle distinctions in terminology can mislead the system designer. Before selecting a high speed SHA, the user should have a clear understanding of the intent and meaning of the manufacturer's usage of such specifications as aperture time and acquisition time.



SHA STRUCTURE - SIMPLE FOLLOWER

Figure 3.7



SHA STRUCTURE - FOLLOWER WITH INPUT BUFFER

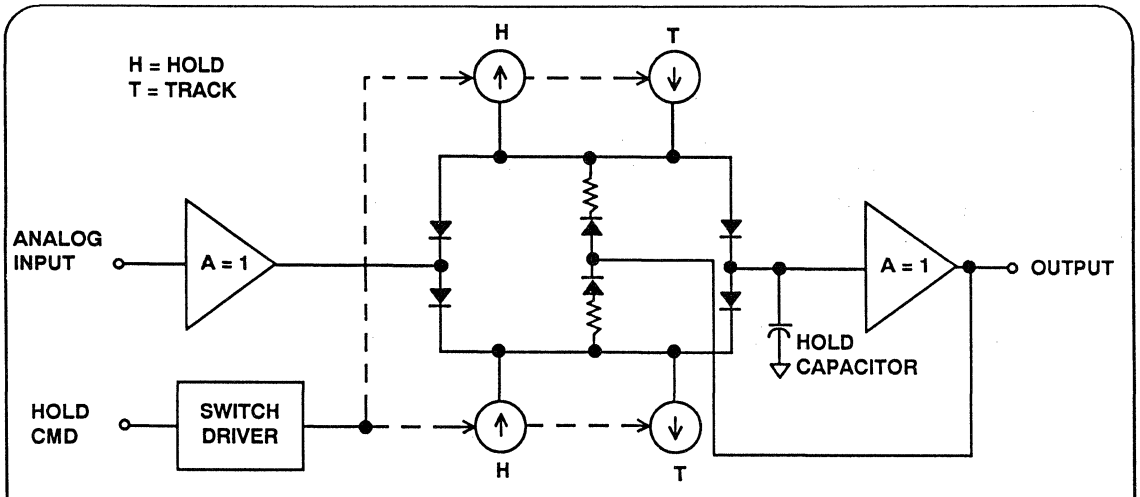
Figure 3.8

CLOSED LOOP SHAS

The circuit of Figure 3.9 has the essential advantage of potentially fast acquisition and settling time because it is an open loop device.

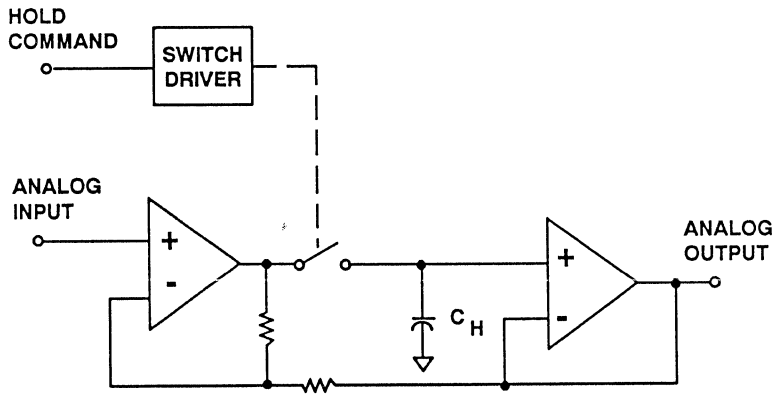
If low frequency tracking accuracy is more important than speed, this can be accomplished by closing the loop around the storage capacitor and using high loop gain to enforce tracking accuracy.

Figure 3.10 shows a configuration in which the input follower of Figure 3.9 is replaced by a high gain difference amplifier. Now, when the switch is closed, the output (which represents the charge on the capacitor) is forced to track the input, within the capability of input amplifier's gain, bandwidth, common-mode error, and current driving capabilities. SHAs using this circuit configuration to achieve



OPEN LOOP DIODE BRIDGE SHA

Figure 3.9



SHA STRUCTURE -
FEEDBACK CIRCUIT WITH OUTPUT FOLLOWER

Figure 3.10

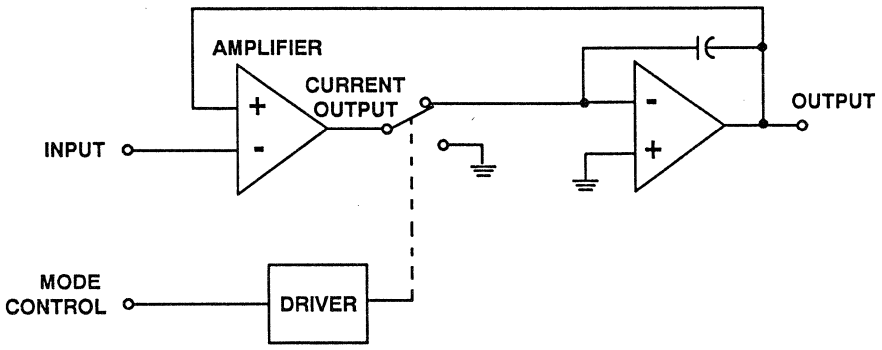
higher accuracy than that available in open loop circuits include the Analog Devices AD582, AD583 and ADSHC-85.

In Figure 3.11 (which illustrates the architecture of the closed loop AD585 and SHA1144), an integrator configuration is used to charge the capacitor, permitting the switch to operate at ground potential; this simplifies leakage problems.

Because both the output and the input affect the charge on the capacitor, the acquisition time and the settling time are identical in the circuits of both Figure 3.10 and 3.11. If the circuit of Figure 3.10 is switched into hold before the output has settled at its final value, the sample may be in error. In addition, since the loop is open during hold, the input stage must reacquire the input when the circuit is returned to sample, even if the input is unchanged. As a rule, this will result in a spike if the input amplifier has high voltage gain.

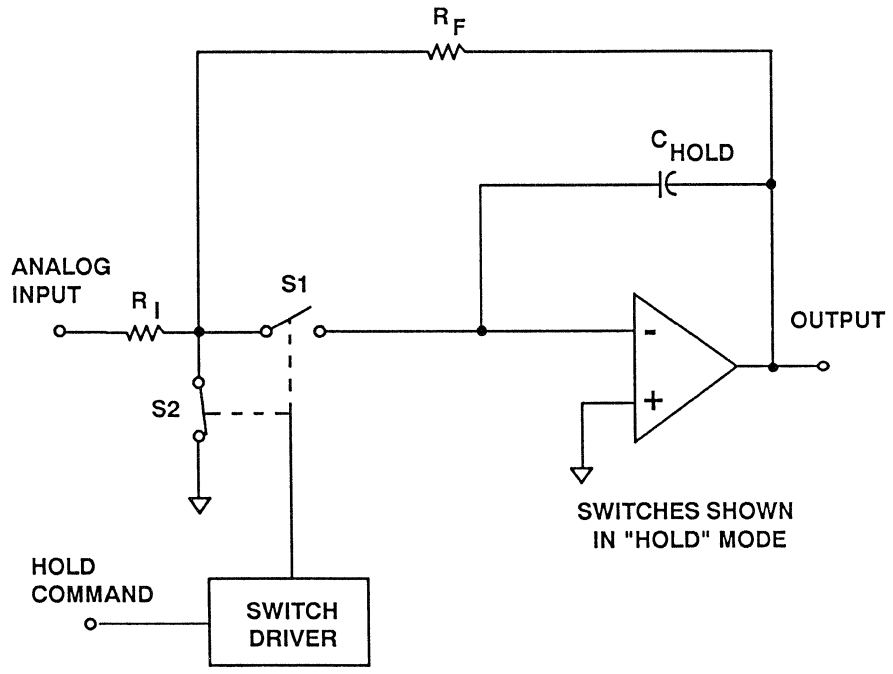
If input impedance and acquisition time are not critical, and sufficient drive current is available from the source, the circuit of Figure 3.12 may be desirable. Here, only a single operational amplifier is required; and the input impedance and gain are a function of the choice of R_I and R_F. In both sample and hold, the input impedance to ground is R_I. In the sample mode, the input circuit sees a virtual ground through R_I and the hold capacitor is charged by the amplifier. In the hold mode, the resistance mode is switched to analog ground potential to disconnect the capacitor while minimizing signal feedthrough and maintaining a constant input impedance. The Analog Devices AD346, AD389 and HTC-0300A all utilize this principle. The circuit of Figure 3.13 takes advantage of the common mode rejection of the op-amp to minimize charge injection and is implemented in the HTC-0300A design.

SHAs are most widely used in data acquisition systems, typically as shown in Figure 3.14. The SHA maintains the input to the A/D converter constant during the conversion interval; meanwhile, the multiplexer is seeking the next channel to be converted, either randomly or sequentially. As soon as conversion is completed, the SHA samples the newly established input, and the cycle is repeated.



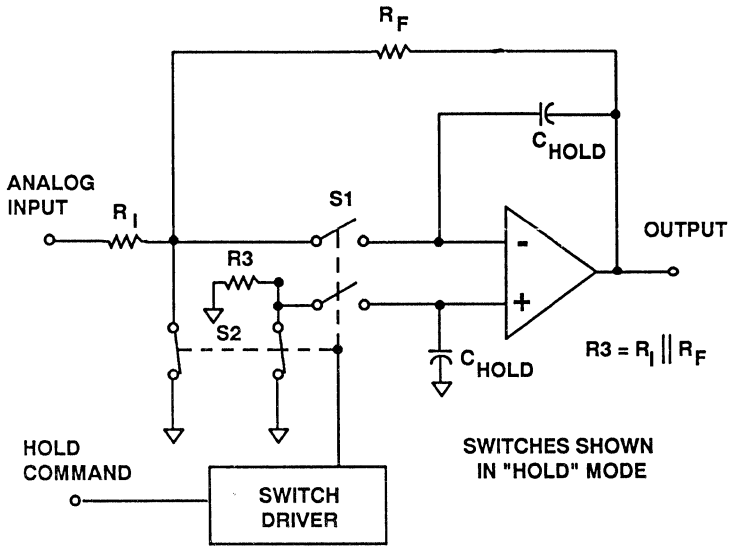
SHA STRUCTURE - FEEDBACK CIRCUIT WITH OUTPUT INTEGRATOR

Figure 3.11



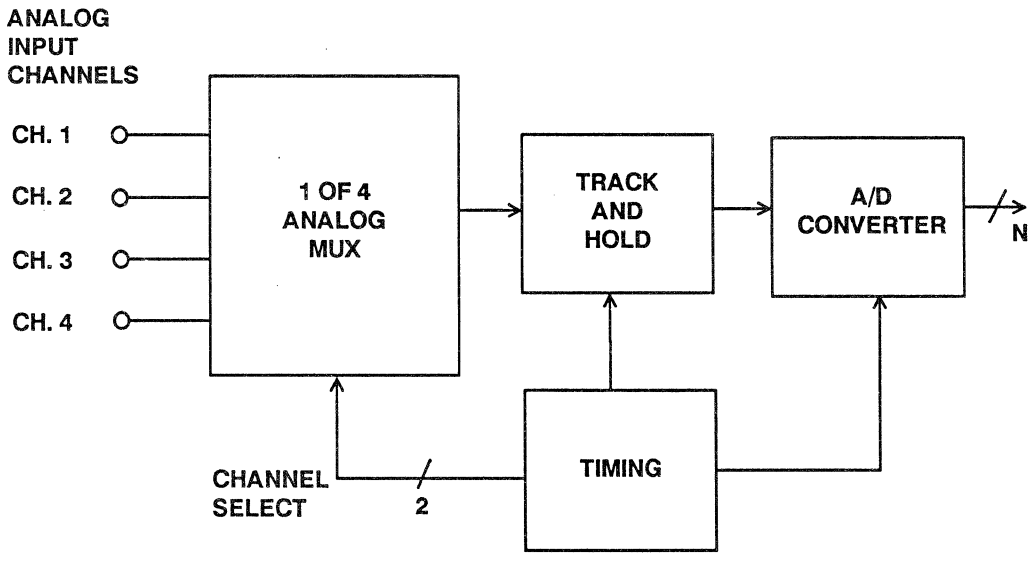
SHA STRUCTURE - INVERTING INTEGRATOR SWITCHED AT SUMMING POINT

Figure 3.12



DIFFERENTIAL SWITCHING TO REDUCE CHARGE INJECTION

Figure 3.13



TRADITIONAL DATA ACQUISITION SYSTEM USING ANALOG MULTIPLEXER

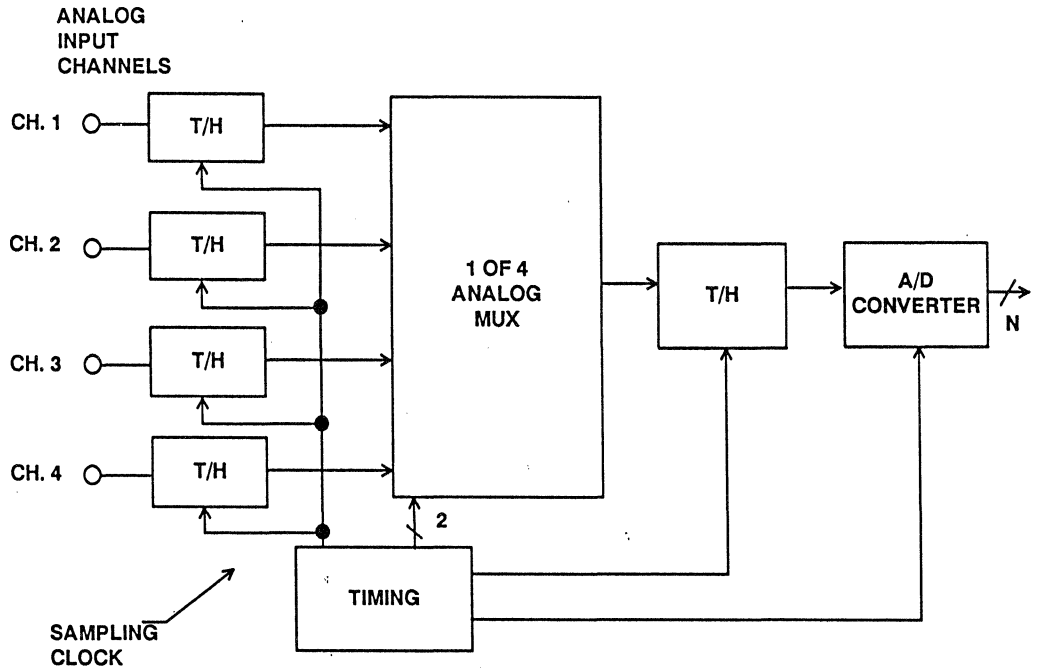
Figure 3.14

This mode of operation is known as synchronous sampling; the sample-hold operates in synchronism with the other system elements. In another mode (viz., asynchronous), a large number of SHAs may be used to acquire and store data at rates pertinent to each individual channel. They are then either interrogated by analog multiplexers as shown in Figure 3.15, or the signals are individually converted asynchronously, and then multiplexed digitally.

In data distribution, 0.01% SHAs may be less costly than large number of D/A converters having comparable accuracy. A typical data distribution system is shown in Figure 3.16. A fast, accurate D/A converter updates a number of sample-holds at speed and accuracy levels appropriate to the individual channels.

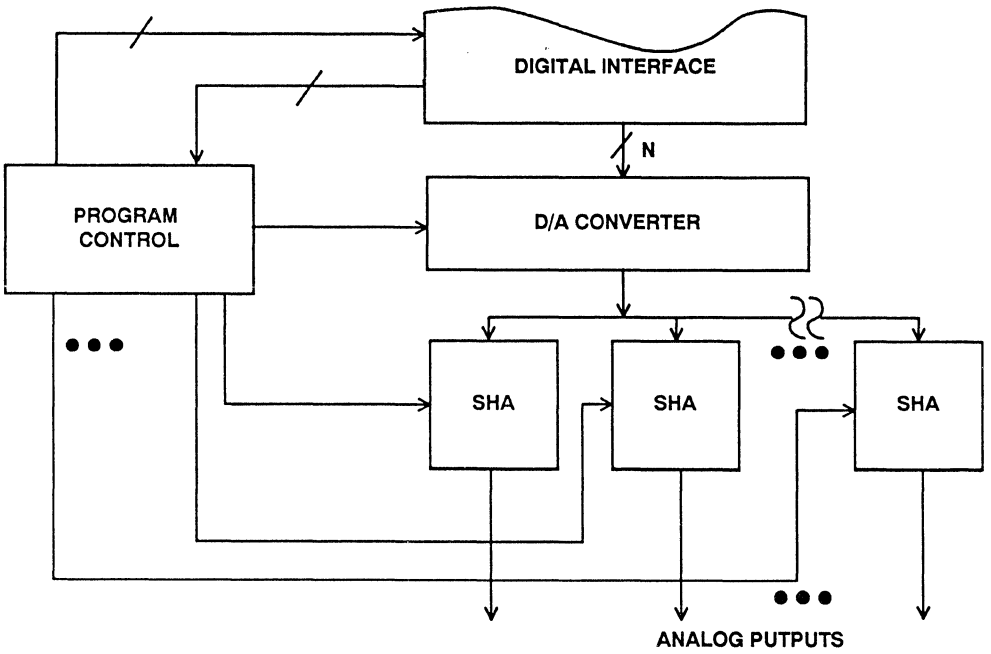
Sample-holds are also used to deglitch D/A converters in systems that are sensitive to the D/A glitches that occur at transition points. Figure 3.17 shows the timing relationship used when deglitching DACs. Just prior to latching the new data into the D/A converter, the SHA is put into the hold mode, so that D/A glitches are isolated from the output. SHAs used as deglitchers must have very small sample-to-hold and hold-to-sample transients and pedestal errors, as well as fast acquisition times.

Another application of the SHA is a peak detector. A typical example is shown in Figure 3.18. When the input is greater than the SHA output, the comparator's positive output causes the SHA to track.



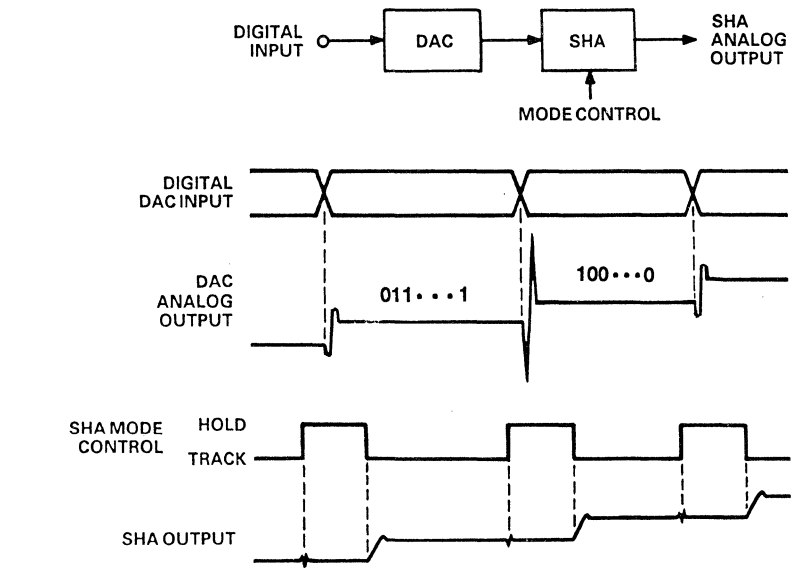
SIMULTANEOUS SAMPLING

Figure 3.15



DATA DISTRIBUTION SYSTEM USING SINGLE D/A AND MULTIPLE SHAS

Figure 3.16

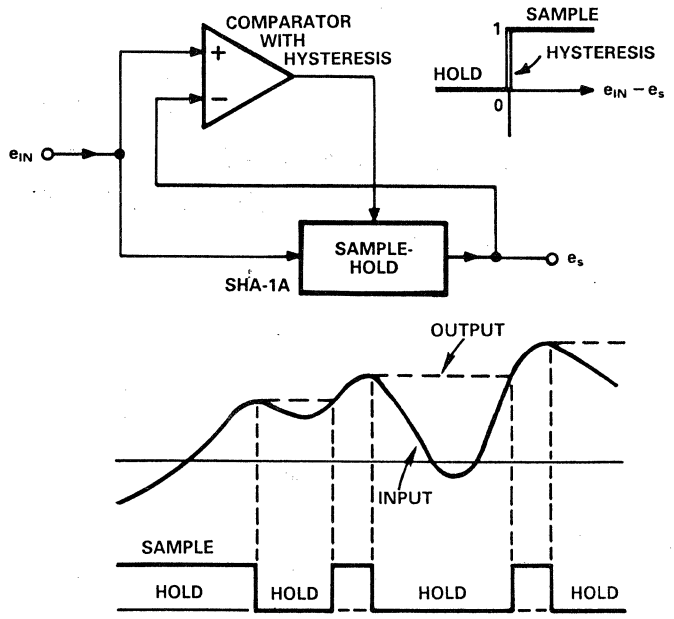


DEGLITCHING THE OUTPUT OF A D/A CONVERTER

Figure 3.17

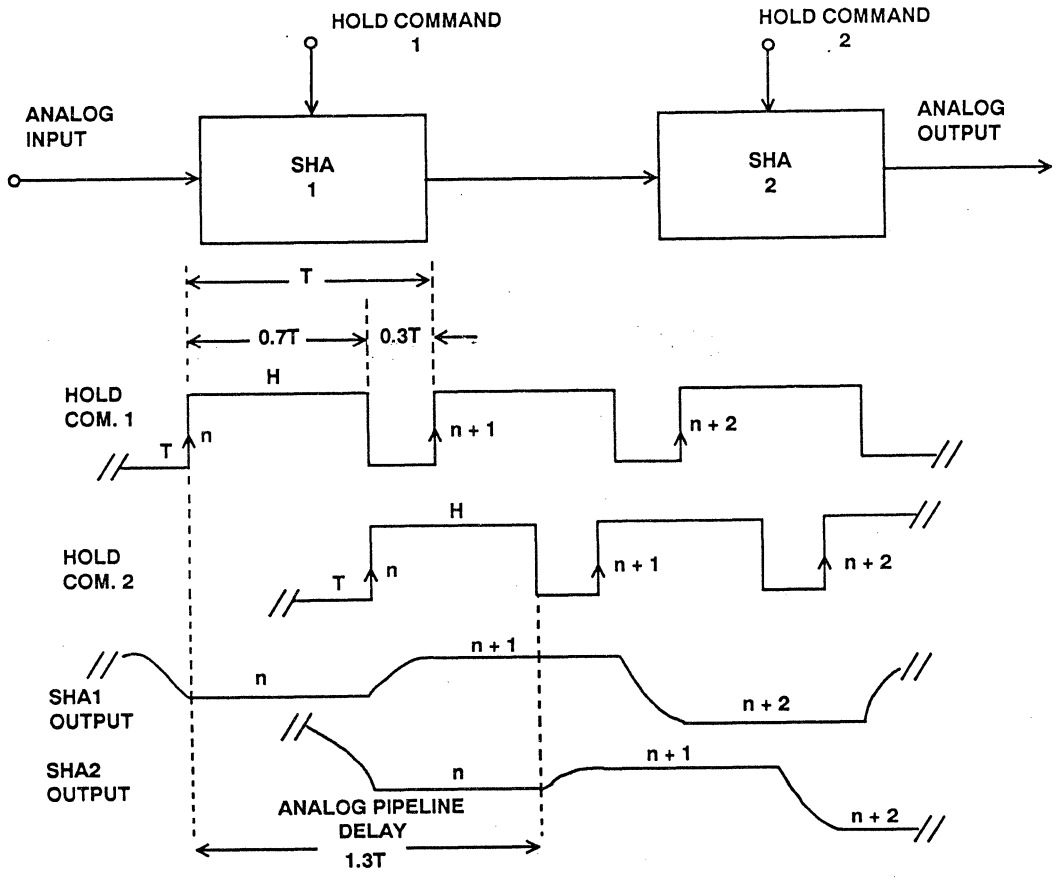
When the input decreases and becomes less than the SHA output, the comparator's 0 output causes the SHA to hold until the input again becomes greater than the output. To reset, the control input is arbitrarily switched into Sample, and the lowest expected level is applied at the input. The SHA output (or the comparator input) is biased by a few millivolts of hysteresis to avoid ambiguity during step inputs and minimize false triggering by noise.

Multiple SHAs can be used in series to generate analog delays as shown in Figure 3.19. SHA 2 is placed in hold just prior to the end of the hold interval for SHA 1. This results in a pipeline delay greater than the sampling period.



PEAK FOLLOWER, USING A SHA AND A COMPARATOR

Figure 3.18



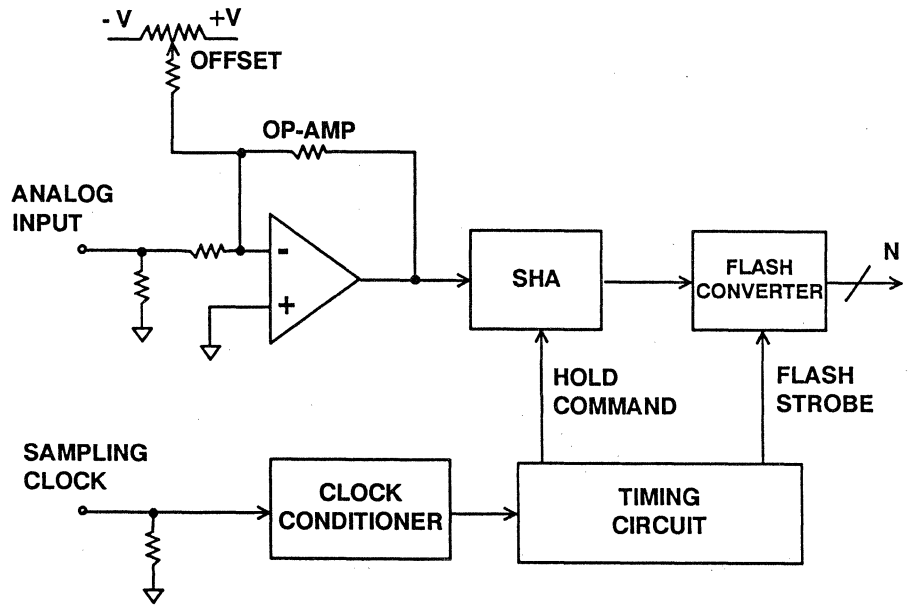
SHAS USED FOR ANALOG PIPELINE DELAY

Figure 3.19

DRIVING FLASH CONVERTERS WITH HIGH SPEED SHAS

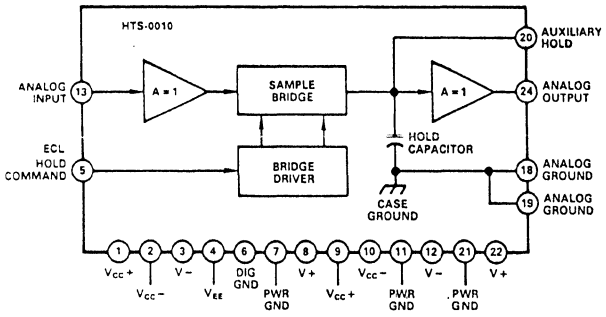
Significant improvements in the dynamic performance (ENOBs, SNR, harmonic distortion) of flash converters can sometimes be obtained by the proper use of SHAs as drivers. As has been discussed previously in the section on A/D converters, flash converter dynamic performance is often limited by the effective sampling time delay matching between the comparators in the comparator bank. By placing the appropriate SHA ahead of the flash converter as shown in Figure 3.20, the input to the flash converter can be made to appear as a DC value. The usefulness of this technique is limited to sampling rates of less than 50 MHz if discrete components must be used. Beyond 50 MHz, the SHA and the flash converter should be integrated into a carefully designed single circuit in order to avoid limitations due to parasitics associated with a package and interconnections.

The task of matching a SHA to a flash even at sampling rates of less than 50 MHz is not straightforward and will usually require some experimentation by the user in order to achieve the desired results.

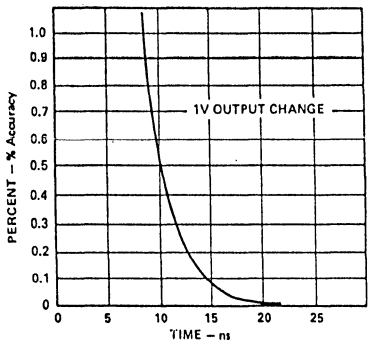


OP-AMP/SHA/FLASH CONVERTER/TIMING CIRCUITS

Figure 3.20



HTS-0010 BLOCK DIAGRAM



SETTLING ACCURACY VS. ACQUISITION TIME

- EFFECTIVE APERTURE DELAY TIME: -2ns
- APERTURE JITTER: 5ps RMS
- SLEW RATE: 300 V/μS
- INPUT RANGE: ±3V
- FPBW =50MHz, $2V_{p-p}$ INPUT
- TRACK MODE HARMONIC DISTORTION: 68dB AT 4 MHz, $2V_{p-p}$ INPUT

HTS-0010 SHA CHARACTERISTICS

Figure 3.21

The first step in the process is to determine the dynamic performance of the stand-alone flash converter itself - ENOBs, SNR, and harmonic distortion specifications should be available from the data sheet. If the data sheet performance is not being achieved, the user should make sure that dynamic performance degradation is not coming from the drive amplifier. The proper selection of the flash converter drive amplifier is discussed in detail in the flash converter section and the amplifier section of this seminar.

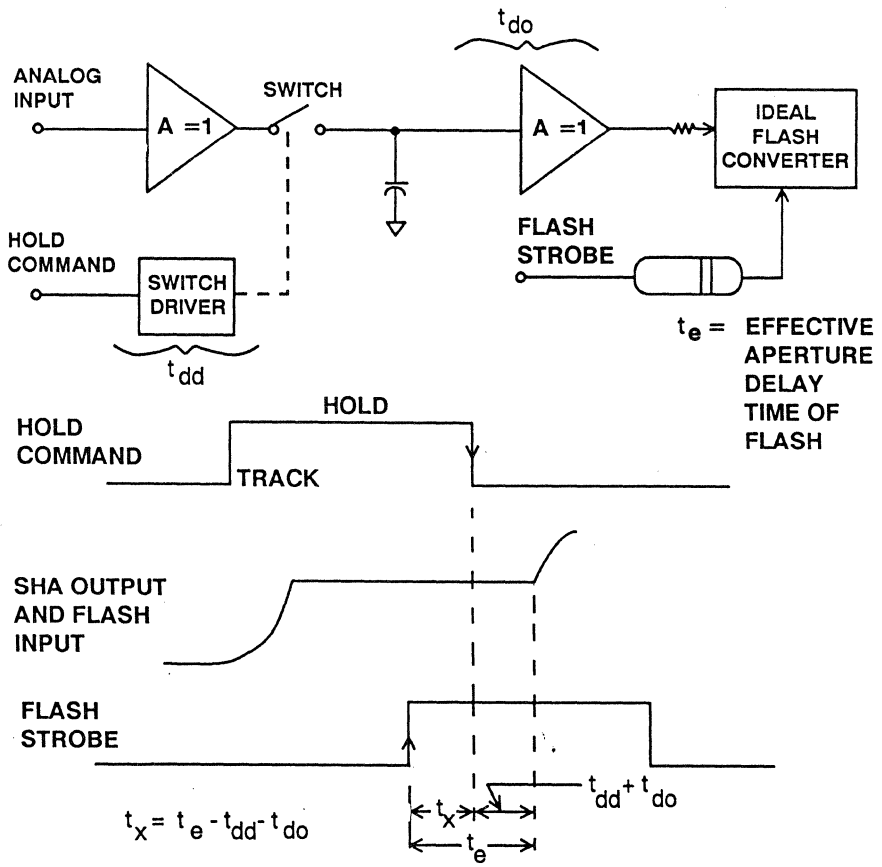
The SHA should be selected based upon acquisition time, bandwidth, aperture jitter and harmonic distortion. SHA harmonic distortion is almost always specified in the track mode and therefore may not be indicative of the performance of the SHA/flash combination. Make sure that the output voltage and drive capability of the SHA is compatible with the flash input. If level shifting is required, it should be done *ahead* of the SHA with a suitable op-amp as shown in Figure 3.20. The SHA selected will invariably have open-loop architecture such as the HTS-0010 in order to meet the acquisition time requirements. The high performance specs of the HTS-0010 hybrid SHA are given in Figure 3.21 for reference.

The most critical part of mating a SHA with a flash is the system timing. The relationship between the various pulses is

SHA/FLASH TIMING CONSIDERATIONS

- Clock Signal Conditioning If Required
- SHA Hold Command Pulse Width and Duty Cycle
- Flash Strobe Pulse Delay and Duty Cycle

Figure 3.22



SHA/FLASH TIMING RELATIONSHIIPS

Figure 3.23

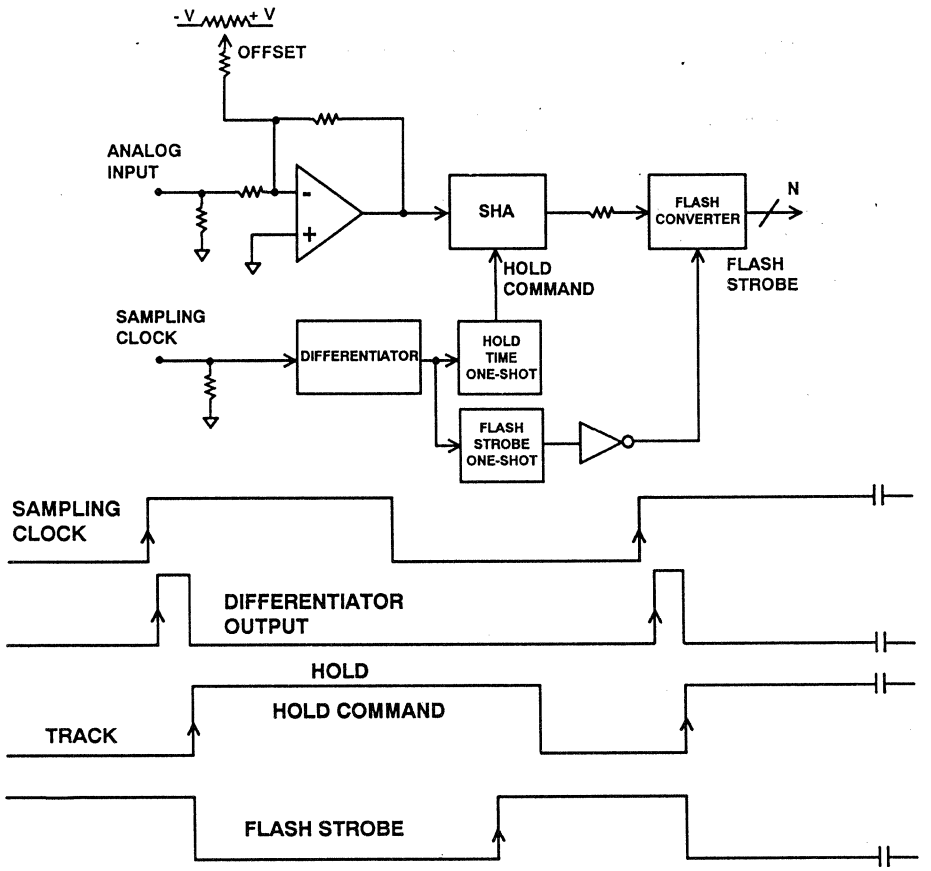
SHA/FLASH INTERFACING STEPS

- Select best flash converter
- Determine dynamic performance
- Select SHA (if required!)
- Determine approximate timing relationships between SHA and flash
- Design timing circuits for flexibility using ECL logic
- Optimize timing experimentally for best dynamic performance
- Check timing for adequate margin

Figure 3.24

shown in Figure 3.23. The basic system clock period is first determined by taking the reciprocal of the sampling rate. Next, choose the maximum SHA hold time based on the required acquisition time for the desired accuracy. For example, with the HTS-0010, an acquisition time of at least 15ns should be allowed for settling to 0.1% (roughly equivalent to 60 dB linearity). If the system sampling rate requirement is 25 MHz (T = 40ns), then a maximum hold time of 25ns is allowable (63% duty cycle). The flash strobe should be positioned as close to the end of the hold time (referenced to the SHA/flash interface) as possible. The flash effective aperture delay time (t_e), SHA switch driver delay (t_{dd}), and SHA output delay (t_{do}) can be used to determine the approximate delay time (t_x) between the trailing edge of the hold command pulse and the leading edge of the flash strobe. In practice, both t_e and $t_{dd} + t_{do}$ are typically less than 5ns.

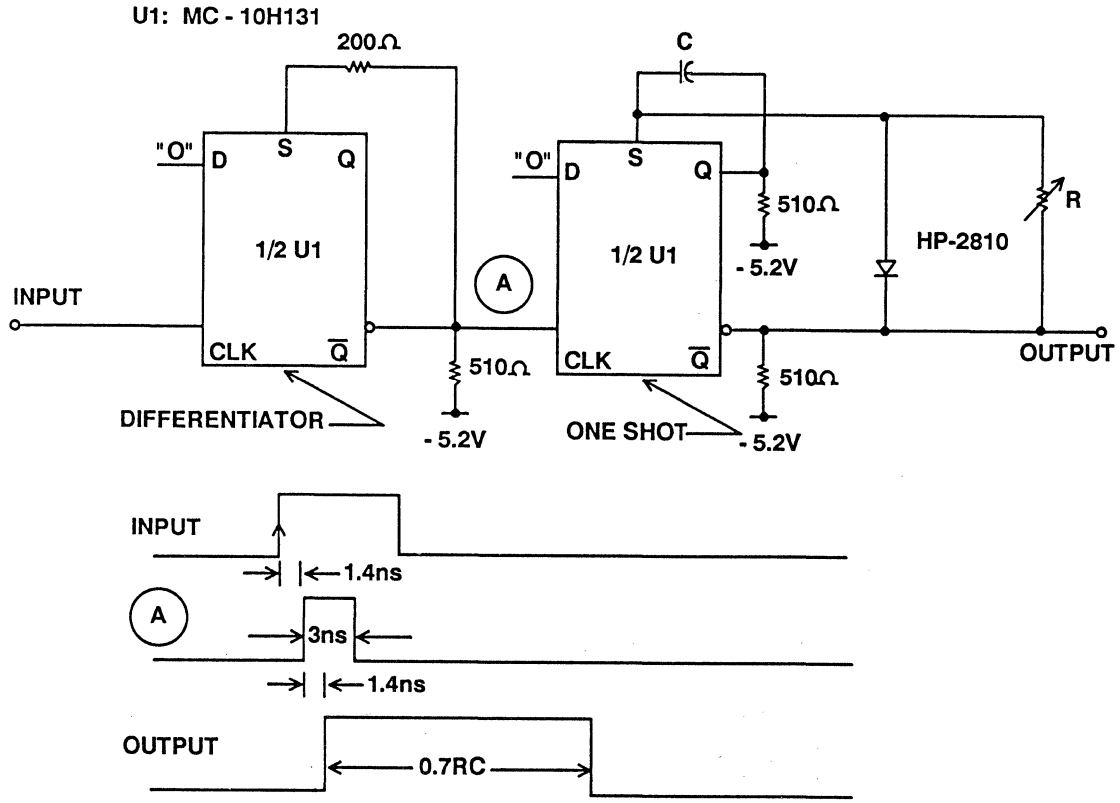
Figure 3.25 shows a complete SHA/flash system with ECL one-shot multivibrators (see Figure 3.26) used as pulse shapers and pulse delays. Potentiometers allow the timing to be optimized for best dynamic system performance. As an alternative to one-shots, ECL gates can be used with tapped lumped constant delay lines to generate controlled pulse widths and delays as shown in Figure 3.27. Since stable clocks are required for maximum phase and frequency stability, they often come from bipolar sources as sinewaves. A high-speed ECL comparator (such as the AD96685/96687) is useful for converting the stable sinewave into differential ECL levels while introducing a minimum of jitter as shown in Figure 3.27.



SHA/FLASH TIMING USING ONE-SHOTS

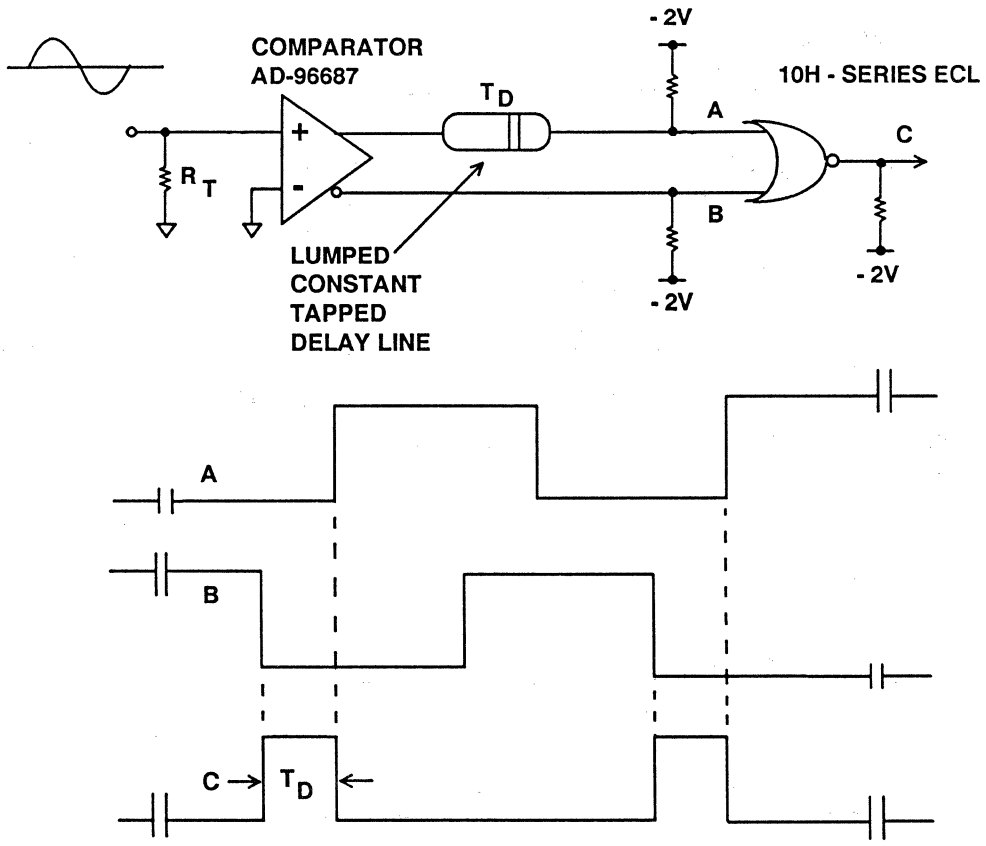
Figure 3.25

Once the optimum system timing has been determined experimentally (based on DSP analysis of the flash converter output or decimated beat frequency reconstruction), the sensitivity of the system performance to variations in the timing pulse widths and delays should be checked to insure adequate margins have been allowed.



ECL ONE-SHOT MULTIVIBRATOR

Figure 3.26



ECL PULSE CONDITIONERS

Figure 3.27

MODEL	ACQUISITION TIME	ACCURACY	APERTURE JITTER	TECHNOLOGY
HTS0010	14ns(0.1%)	0.1%	5ps	HYBRID
HTS0025	25ns(0.1%)	0.1%	20ps	HYBRID
HTC0300A	200ns(0.01%)	0.01%	50ps	HYBRID
AD346	2μs(0.01%)	0.01%	400ps	HYBRID
AD389	2.5μs(0.003%)	0.003%	400ps	HYBRID
AD386	4μs(16-BITS)	16-BITS	40ps	HYBRID
AD1154	3.5μs(16-BITS)	16-BITS	140ps	HYBRID
AD585	3μs(0.01%)	0.01%	500ps	IC
AD781	1μs(0.01%)	0.01%	50ps	IC
AD682	1μs(0.01%)	0.01%	50ps	DUAL AD781
AD684	1μs(0.01%)	0.01%	50ps	QUAD 781

SAMPLE AND HOLD SELECTION GUIDE

Figure 3.28

SECTION IV

HIGH SPEED OP AMPS

HIGH SPEED OP AMPS

HIGH SPEED OP AMP CHARACTERISTICS

Designers can choose from a variety of cost effective, high performance components. These include both voltage and current feedback (transimpedance) op amps in both hybrid and monolithic form. Depending on system requirements, the designer can also choose from bipolar or FET input op amps.

The trend in data acquisition is toward higher speed and accuracy. High performance amplifiers are required to drive cables, A/D converters, and also act as I to V converters on the outputs of fast D/A converters. Important specifications are wide bandwidth, DC accuracy, low harmonic distortion and fast settling with low overshoot.

KEY HIGH SPEED OP AMP SPECIFICATIONS

- Wide Bandwidth
- Low Harmonic Distortion
- Fast Settling Time
- Low Overshoot
- Low Noise
- High Output Current
- DC Accuracy

Figure 4.1

Each application has different requirements. For example, low bias current FET input op amps are useful in sample-and-hold (SHA) circuits and peak detectors. Current feedback op amps have low voltage noise, high bandwidths, and fast settling times while maintaining unity-gain stability. Voltage feedback op amps are cost effective, extremely versatile and are available in a wide range of bandwidths and precision.

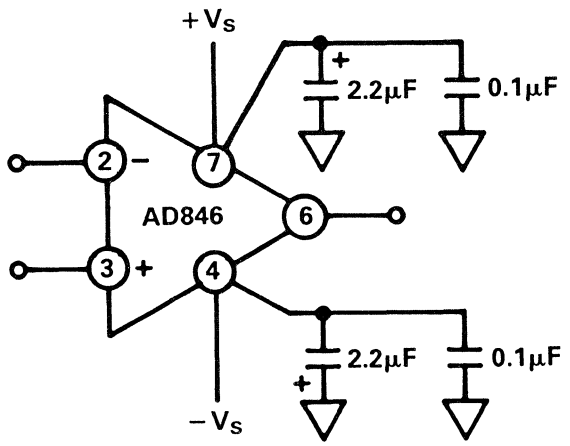
Most of the circuits in this seminar are shown in simplified form in order to convey more clearly the principles involved. These circuits can successfully be used in actual applications by following the advice on precision high speed signal handling (grounding, decoupling, isolation, etc.) given in this section and Section X. The applications section of individual device data sheets will provide additional guidance in this respect.

GROUNDING AND BYPASSING

In designing practical high speed circuits some special precautions are needed. Circuits must be wired using short interconnect leads. Ground planes should be used on the component side of the P.C. board to provide both a low resistance, low inductance circuit path and to minimize the effects of high frequency coupling. IC sockets should be avoided, since their capacitance and inductance can degrade the bandwidth of the device.

Power supply leads should be bypassed to the ground plane as close as possible to the pins of the amplifier. Again, the component leads should be kept very short. As shown in Figure 4.2, a parallel combination of a 2.2 μF tantalum and a 0.1 μF ceramic disc capacitor is recommended for amplifiers with closed-loop bandwidths less than 50MHz. If the amplifier is driving a light resistive load (>1k Ω) and only 10pF - 20pF of capacitance, then the 2.2 μF capacitor may not be needed at each amplifier, but can be shared by amplifiers within 5cm power supply run of the capacitor.

4



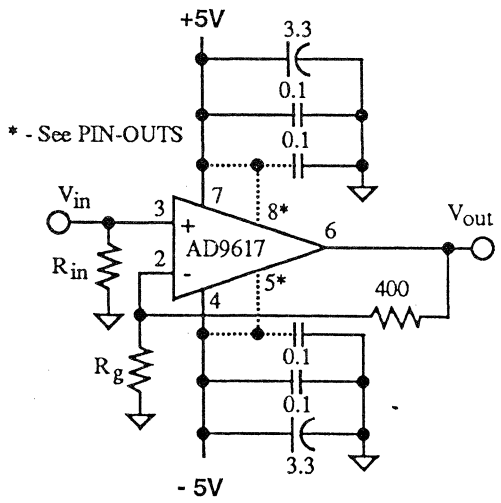
POWER SUPPLY BYPASSING FOR 50 MHz AMPLIFIERS

Figure 4.2

Amplifiers with 100MHz or higher bandwidths require additional bypassing and care in layout as illustrated in Figure 4.3. Note the use of parallel supply pins to reduce the lead inductance between the external bypass capacitors and the amplifier's internal circuitry. Using 0.1μF chip capacitors instead of 0.1μF discs further reduces lead inductance, and is highly recommended for amplifiers such as the AD9611, AD9617 and AD9618 with bandwidths of over 100MHz.

Temperature stable linear power supplies with low noise and ripple should be used for powering high speed circuits. Switching power supplies often seems to meet these criteria, including ripple specifications. However, ripple specs are generally expressed in volts rms which tends to obscure the peak amplitude of the output spikes generated by virtually all switching mode supplies. These spikes can produce virtually unfilterable noise peaks with amplitudes of several hundred millivolts.

If switching supplies are used, they should be carefully shielded, and their outputs should be well filtered right at the supply. They should also be located some distance from critical circuits to minimize electric field and magnetic field noise coupling.



POWER SUPPLY BYPASSING FOR 100+ MHz AMPLIFIERS

Figure 4.3

Special precautions should be taken in the selection of resistors, since many types of resistors have substantial parasitic capacitance. Bulk metal or carbon composition resistors have lower shunt capacitance than spirally wound types such as the RN55 series. Sockets should be avoided if possible because of their stray inductance and capacitance. If sockets are necessary, individual pin sockets (sometimes called "cage jacks") should be used. These contribute far less stray reactance than molded socket assemblies.

Evaluation boards are often available for ultra high-speed op amps. In some cases, suggested PC board layouts are shown on the individual op amp data sheets.

CLASSES OF HIGH SPEED DC COUPLED AMPLIFIERS

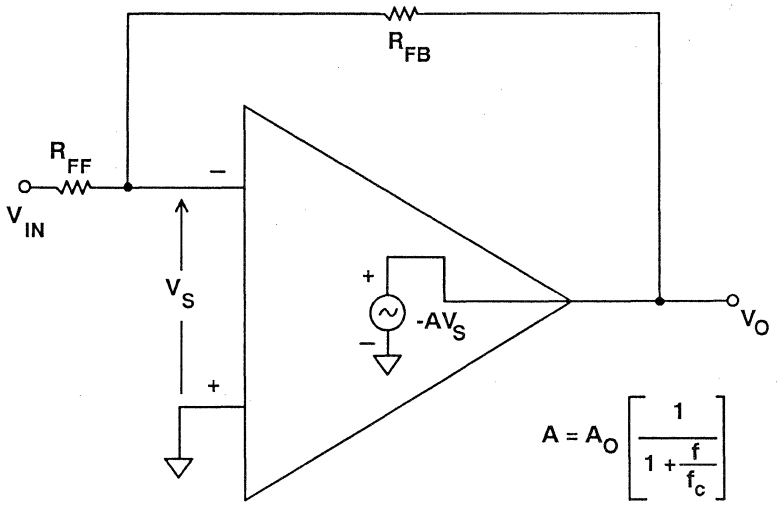
- Voltage Feedback Op-Amps
- Open-Loop Buffers
- Closed-Loop Buffers
- Current Feedback Op-Amps (Transimpedance Amplifiers)

Figure 4.4

HIGH SPEED VOLTAGE FEEDBACK OP AMPS

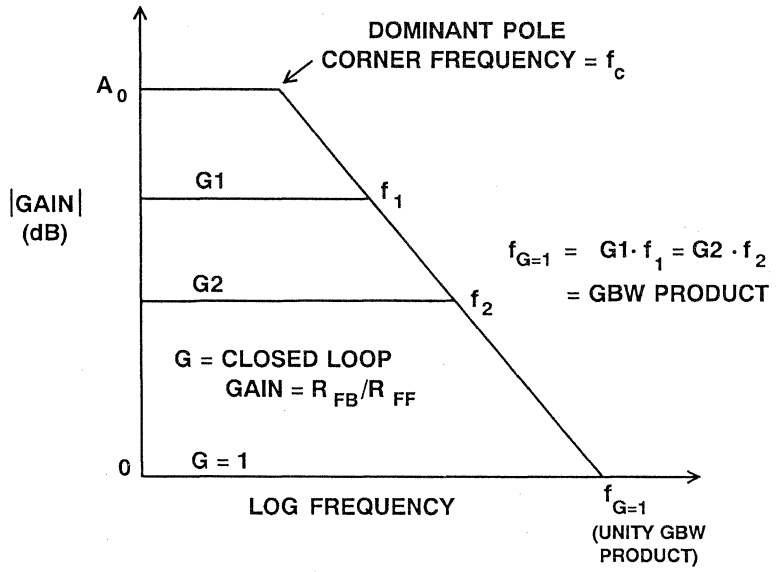
The equivalent circuit for a voltage feedback op amps is shown in Figure 4.5. Figure 4.6 shows the classic gain versus frequency response obtained with dominant pole compensation. The 6dB/octave rolloff is the optimum choice for best phase margin and fastest settling time. The product of the closed loop gain and the closed loop bandwidth (gain-bandwidth product) is constant for fixed compensation. The closed loop bandwidth therefore varies inversely with the closed loop gain.

A simplified schematic of a high speed voltage feedback is shown in Figure 4.7. For purposes of discussion the amplifier is shown in the inverting mode. The amplifier consists of a differentialinput stage (common emitter), a voltage amplification stage, and a Class AB (push-pull) output driver.



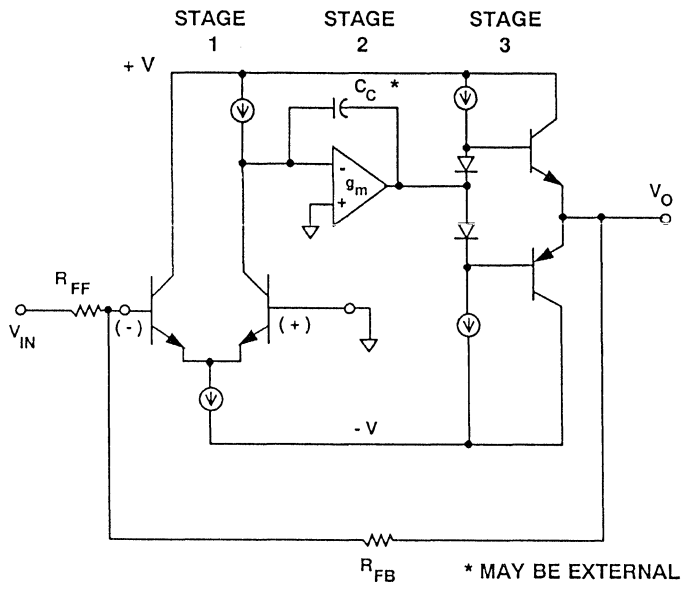
VOLTAGE FEEDBACK OP-AMP EQUIVALENT CIRCUIT

Figure 4.5



VOLTAGE FEEDBACK OP-AMP FREQUENCY RESPONSE

Figure 4.6

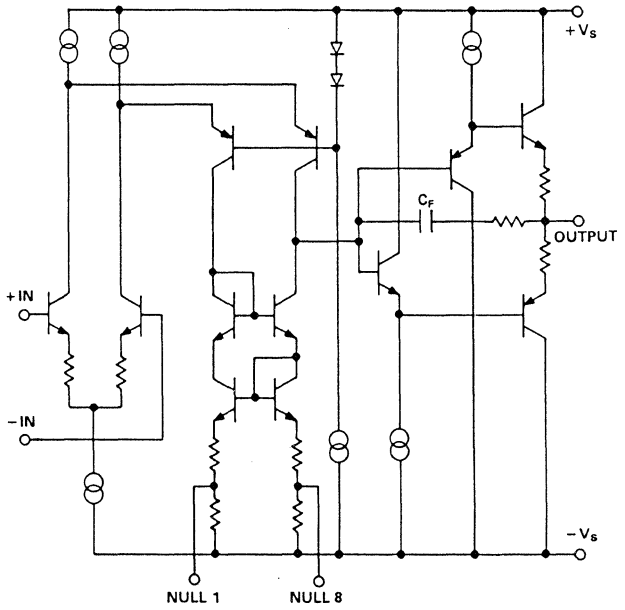


VOLTAGE FEEDBACK
OP-AMP CIRCUIT
Figure 4.7

A High Speed Voltage Feedback Op Amp: The AD847

The AD847 is fabricated on Analog Devices' proprietary complementary bipolar (CB) process which enables the construction of pnp and npn transistors with similar f_Ts in the 600MHz to 800MHz region. The AD847 circuit (Figure 4.8) includes an npn input stage followed by fast pnps in the folded cascade intermediate gain stage. The CB pnps are also used in the current amplifying output stage. The internal compensation capacitance that makes the AD847 unity gain stable is provided by the junction capacitances of transistors in the gain stage.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies and with low capacitive loads, the gain from the compensation node to the output is very close to unity. In this case C_F is bootstrapped and does not contribute to the compensation capacitance of the part. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is completely bootstrapped. Some fraction of C_F contributes to the compensation capacitance, and the unity gain bandwidth falls. As the load capacitance is increased, the bandwidth continues to fall, and the amplifier remains stable.



AD847 SIMPLIFIED SCHEMATIC
Figure 4.8

VOLTAGE FEEDBACK OP AMP DYNAMIC CHARACTERISTICS

- Constant Gain-Bandwidth Product for Fixed Compensation
- External Compensation Allows High Gain Bandwidth Products
- Closed Loop Bandwidth (CLBW) Varies Inversely with Closed Loop Gain for Fixed Compensation

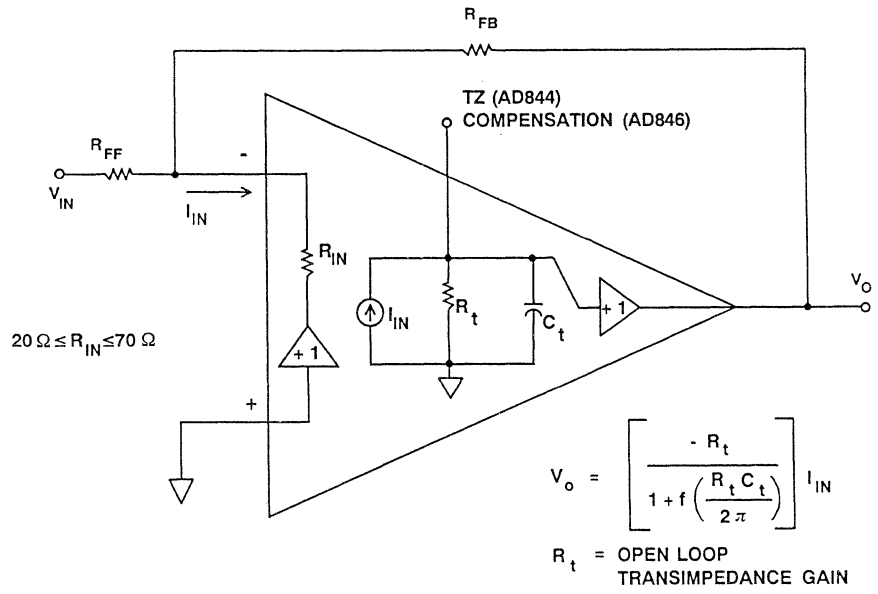
$$\frac{\text{CLBW (G = X)}}{\text{CLBW (G = 1)}} \approx \frac{1}{1 + \frac{R_{FB}}{R_{FF}}} = \frac{1}{1 - G}$$

- High Open Loop Input Impedance
- Parasitic Poles at Input Created at Summing Junction Can Compromise Bandwidth and Pulse Fidelity
- Symmetrical Inverting and Non-Inverting Inputs
- FET Input Transistors Reduce Input Bias Currents, Raise Input Impedance

Figure 4.9

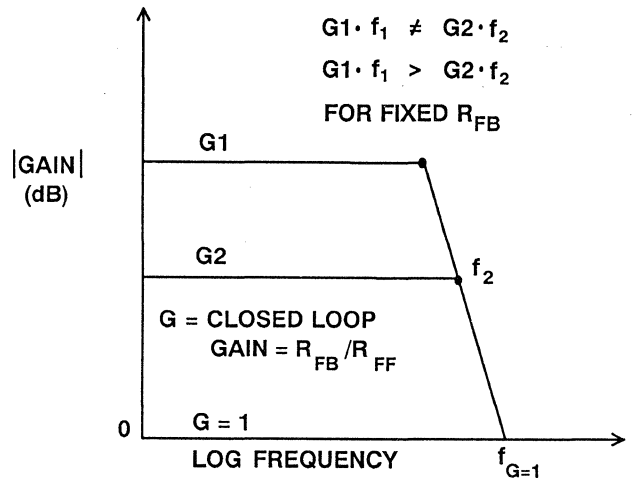
HIGH SPEED CURRENT FEEDBACK AMPLIFIERS

The equivalent circuit for a current feedback op amp is shown in Figure 4.10. An ideal current feedback amplifier has zero input impedance at its inverting input ($R_{IN} = 0$), infinite input impedance at its non-inverting input, and the voltage at the inverting input is held at that of the non-inverting by a unity gain buffer. The transfer function of this amplifier (V_O/I_{IN}) is a dimensional quantity (dimension R), not a ratio as in the case for voltage feedback op amps. Because of the very low (ideally zero) inverting input impedance, the current feedback op amp has a bandwidth which is more or less independent of closed loop gain for a fixed feedback resistor R_{FB}. This implies that the product of the closed loop gain and the closed loop bandwidth is not a constant, hence it is inappropriate to apply the term *gain bandwidth product* to current feedback amplifiers.



CURRENT FEEDBACK OP AMP EQUIVALENT CIRCUIT

Figure 4.10



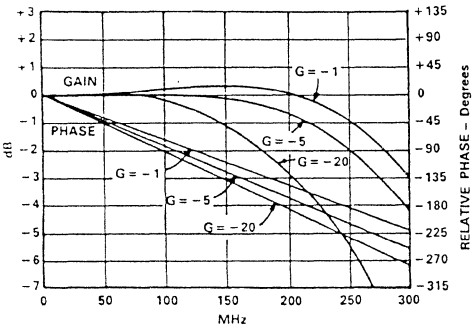
CURRENT FEEDBACK OP-AMP FREQUENCY RESPONSE

Figure 4.11

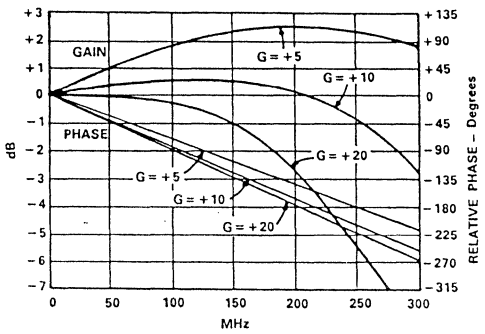
The closed loop bandwidth for the AD9611 high performance current feedback amplifier is shown in Figure 4.12. Note that the inverting 3dB bandwidth is approximately 300MHz for G = -1 and falls to only 200MHz for G = -20. A traditional voltage feedback amplifier's closed loop bandwidth would be reduced to 15MHz for G= -20 (assuming a unity gain bandwidth product of 300MHz). Note also that the phase linearity for this amplifier is excellent (typically better than 1° up to 120MHz).

The practical current feedback amplifier is based upon a common base input stage as shown in Figure 4.13. This configuration is characterized by a high impedance noninverting input which drives the inverting input via a unity gain buffer. The open loop inverting input impedance is approximately equal to any resistance in series with the emitter (R_E) plus the dynamic input impedance of the grounded base transistor (r_E). The output voltage is controlled by the input current and is related to it by the transimpedance gain expressed in ohms. Because of the low impedance inverting input common base stage, a stepped input voltage ΔV_{IN} will produce a stepped current in the emitter and collector of Q1. This will yield a slew rate of I_{IN}/C_C. Thus the rise and fall times of the output are essentially constant regardless of the output voltage swing. This attribute provides for exceptional fullpower bandwidth.

Bandwidth characteristics for several current feedback op amps are shown in Figure 4.14.



INVERTING

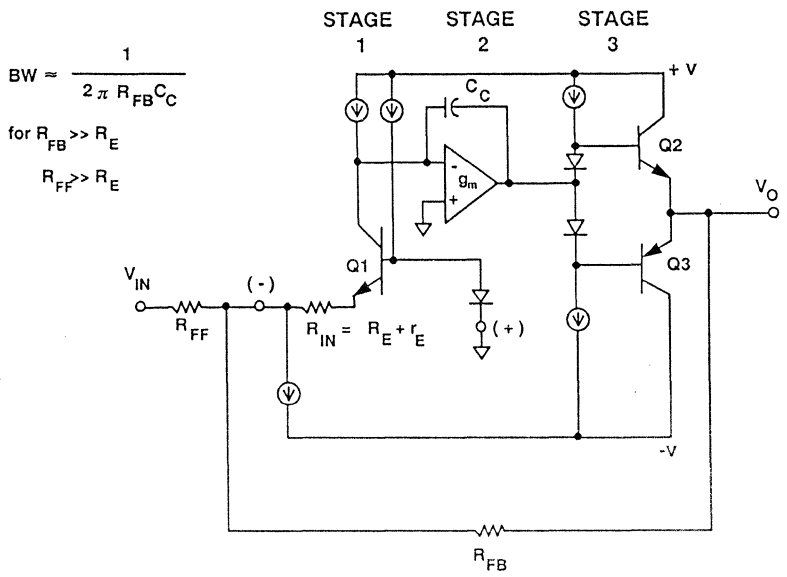


NON-INVERTING

GAIN AND PHASE VS. FREQUENCY FOR AD-9611

Figure 4.12

4



SIMPLIFIED CURRENT FEEDBACK OP-AMP CIRCUIT

Figure 4.13

CURRENT FEEDBACK OP AMP BANDWIDTH COMPARISONS

AD846:

R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
1000Ω	1000Ω	-1	46 MHz	46 MHz
1000Ω	100Ω	-10	20 MHz	200 MHz

AD844:

R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
500Ω	500Ω	-1	60 MHz	60 MHz
500Ω	50Ω	-10	33 MHz	330 MHz

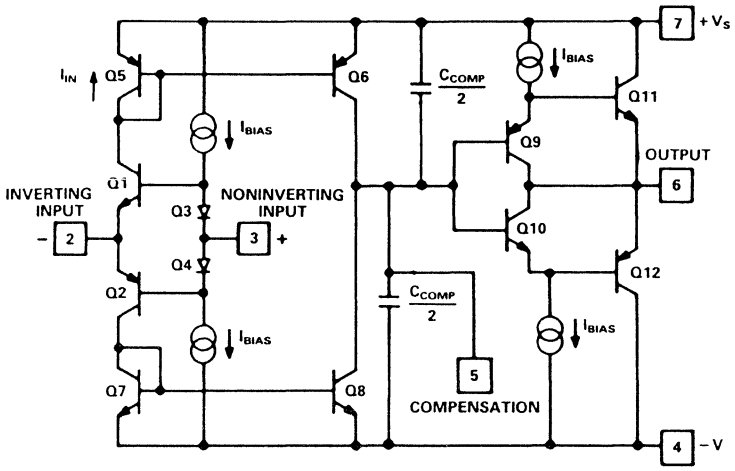
AD9617:

R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
400Ω	400Ω	±1	185 MHz	185 MHz
400Ω	27Ω	±15	105 MHz	1575 MHz

AD9611:

R_{FB}	R_{FF}	GAIN	CLBW	"GBW"
1000Ω	1000Ω	-1	300 MHz	300 MHz
1000Ω	50Ω	-20	200 MHz	4000 MHz

Figure 4.14



AD846 SIMPLIFIED SCHEMATIC

Figure 4.15

Figure 4.15 shows a simplified schematic of the AD846 current feedback amplifier which is implemented on a high speed complementary bipolar process.

Effects of Feedback Resistor on Bandwidth of Current Feedback Amplifiers

High speed current feedback amplifiers are usually optimized for a fixed value of feedback resistor. In the case of the AD9610, AD9611 and AD9615, the feedback resistor is included in the hybrid itself. One side of the resistor is connected internally to the inverting input and the other side is brought to a pin. For the AD844, AD846, AD9617 and AD9618, the feedback resistor is supplied by the user. In a current feedback amplifier, the value of the feedback resistor determines the location of the closed-loop dominant pole. As the feedback resistor is increased, the bandwidth for a given closed loop gain decreases as shown in Figure 4.16. If the feedback resistor is decreased, the bandwidth increases and phase margin decreases, possibly resulting in instability.

For high closed loop gains, it may be desirable to increase the feedback resistor so that the feed forward resistor can be made a reasonable value. If the feedback resistor is internal to the hybrid (AD9610,

EFFECT OF FEEDBACK RESISTOR VALUE ON CURRENT FEEDBACK AMPLIFIER BANDWIDTH

AD9611:

R_{FF}	R_{FB}	GAIN	CLBW
200Ω	1000Ω	- 5	280 MHz
300Ω	1500Ω	- 5	175 MHz
400Ω	2000Ω	- 5	135 MHz
500Ω	2500Ω	- 5	125 MHz

AD844:

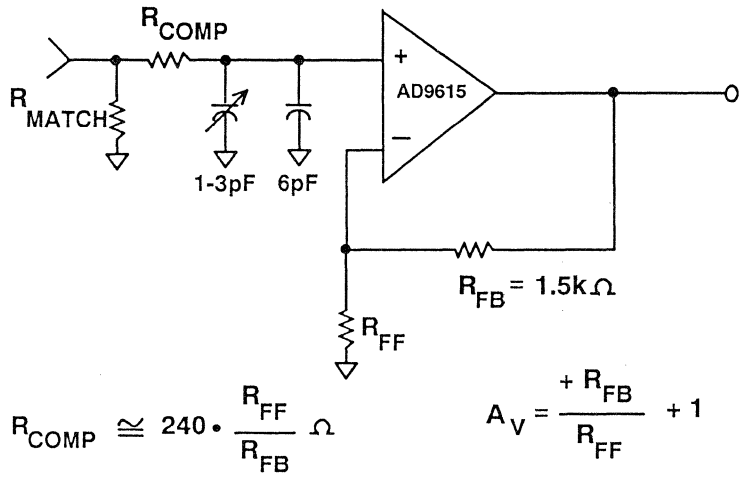
100Ω	500Ω	- 5	49 MHz
500Ω	1000Ω	- 2	30 MHz
1000Ω	2000Ω	- 2	15 MHz
1000Ω	5000Ω	- 5	5.2 MHz

Figure 4.16

AD9611, AD9615), the value of the feedback resistor should be increased by the addition of an external resistor of the appropriate value in series with the internal resistor. This will minimize the effect of the additional shunt capacitance in the feedback loop. The external resistor should be a low inductance, low capacitance type.

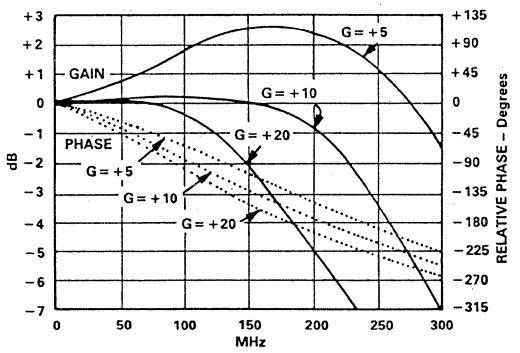
Compensating for Peaking in the Non-Inverting Mode (Current Feedback Op Amps)

Current feedback op amps which are optimized for best performance in the inverting mode may exhibit peaking for low closed loop gains when operated in the non-inverting mode. This peaking is made worse by adding additional stray capacitance to the inverting input. The peaking at low non-inverting gains can be reduced by the addition of a low-pass network to the non-inverting as shown in Figure 4.17. The results of this compensation are shown in Figure 4.18 for the AD9615 op amp.

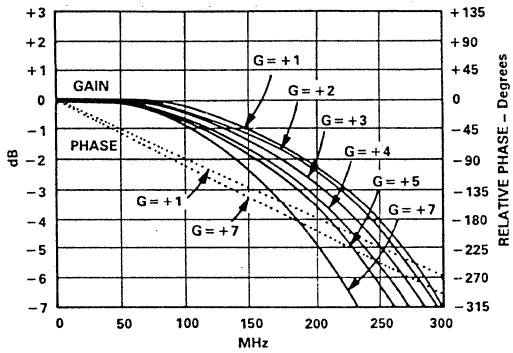


GAIN/FREQUENCY COMPENSATION FOR AD9615, NON-INVERTING MODE, LOW GAINS ($A_V \leq +8$)

Figure 4.17



NON-COMPENSATED



COMPENSATED

EFFECTS OF COMPENSATION ON GAIN/FREQUENCY PERFORMANCE OF AD9615 IN NON-INVERTING MODE

Figure 4.18

CURRENT FEEDBACK OP AMP DYNAMIC CHARACTERISTICS

- Bandwidth Less Sensitive to Closed Loop Gain Than Voltage Feedback Op Amps

$$\frac{\text{CLBW (G = X)}}{\text{CLBW (G = 1)}} \approx \frac{1}{1 + \frac{R_{IN}}{R_{FF}}} = 1,$$

For $R_{FF} >> R_{IN}$

- Wide Bandwidth
- Fast Settling
- Low Distortion (AD9617, AD9618)
- Low Inverting Input Impedance (Approx. 20Ω to 70Ω)
- Optimized and Compensated for Fixed Feedback Resistor R_{FB}

Figure 4.19

4

SETTLING TIME CHARACTERISTICS OF HIGH SPEED AMPLIFIERS

Settling time is defined as:

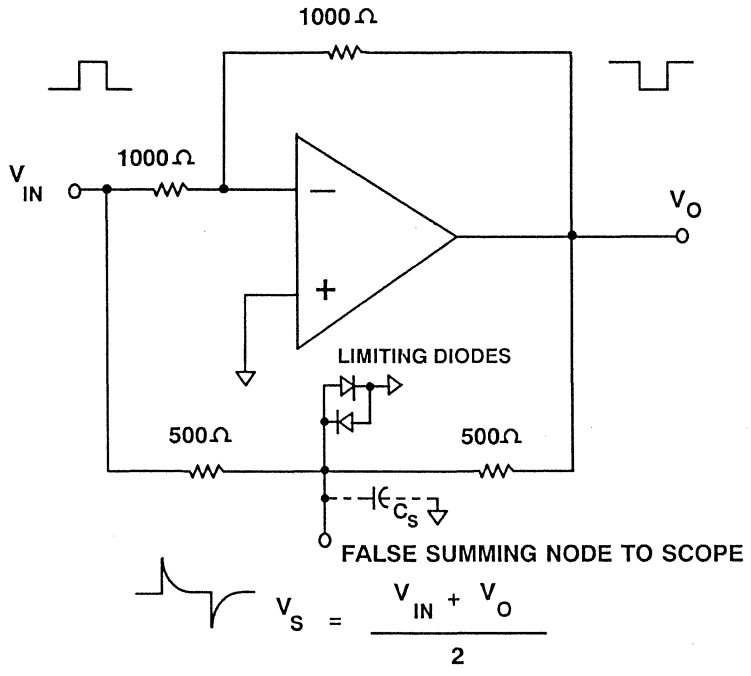
> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

This definition encompasses the major components which comprise settling time. They include (1) propagation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing and (4) linear settling to within a specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for the application.

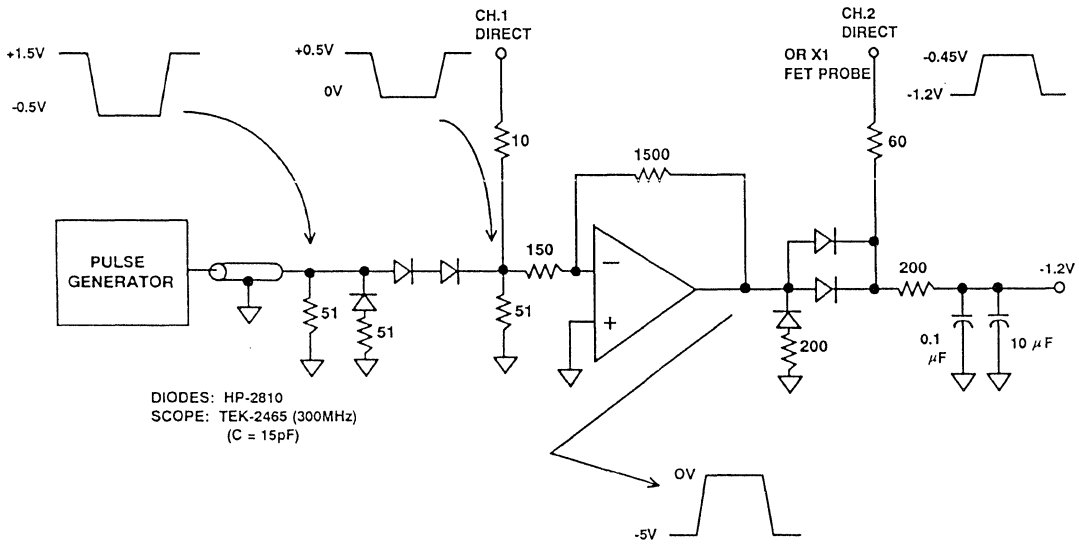
Settling times of high speed op amps are extremely fast. For example, the AD9617 op amp has a 3dB bandwidth of 180MHz and a settling time of only 14ns to 0.02%. The AD840, AD841, AD842 and AD846 all feature settling times of 100ns to 0.01%. Measuring settling times of less than 100ns in the inverting mode is usually accomplished by creating a false summing node with a resistive divider connected between the amplifier output and the input as shown in Figure 4.20. Care should be taken to insure that the time constant at the false summing junction created by the scope capacitance is less than that of the amplifier being tested. The back-to-back diodes help prevent oscilloscope overdrive. An alternative method for measuring settling time is shown in Figure 4.21. The diode network on the amplifier output limits the swing of the 5V output step to 0.75V. This step can be observed directly by the scope with approximately25mV/division vertical sensitivity without overdriving the input (see Figure 4.22). The diode network on the input of the amplifier insures that the pulse at the input of the feedforward resistor is flat.

The Data Precision 6100 Waveform Digitizer with the 640 Sampling Plug-In can be used to measure fullscale settling time directly without overdrive.



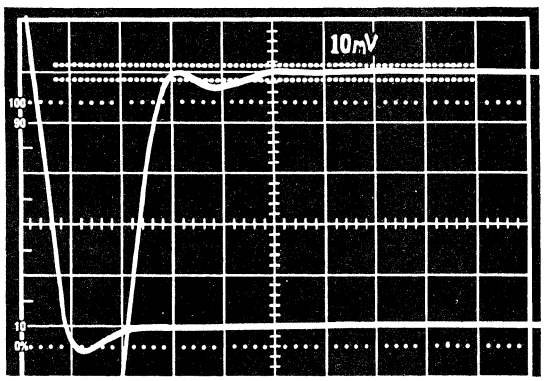
LESS THAN 100ns SETTLING TIME MEASUREMENT USING FALSE SUMMING NODE

Figure 4.20



SETTLING TIME TEST CIRCUIT

Figure 4.21



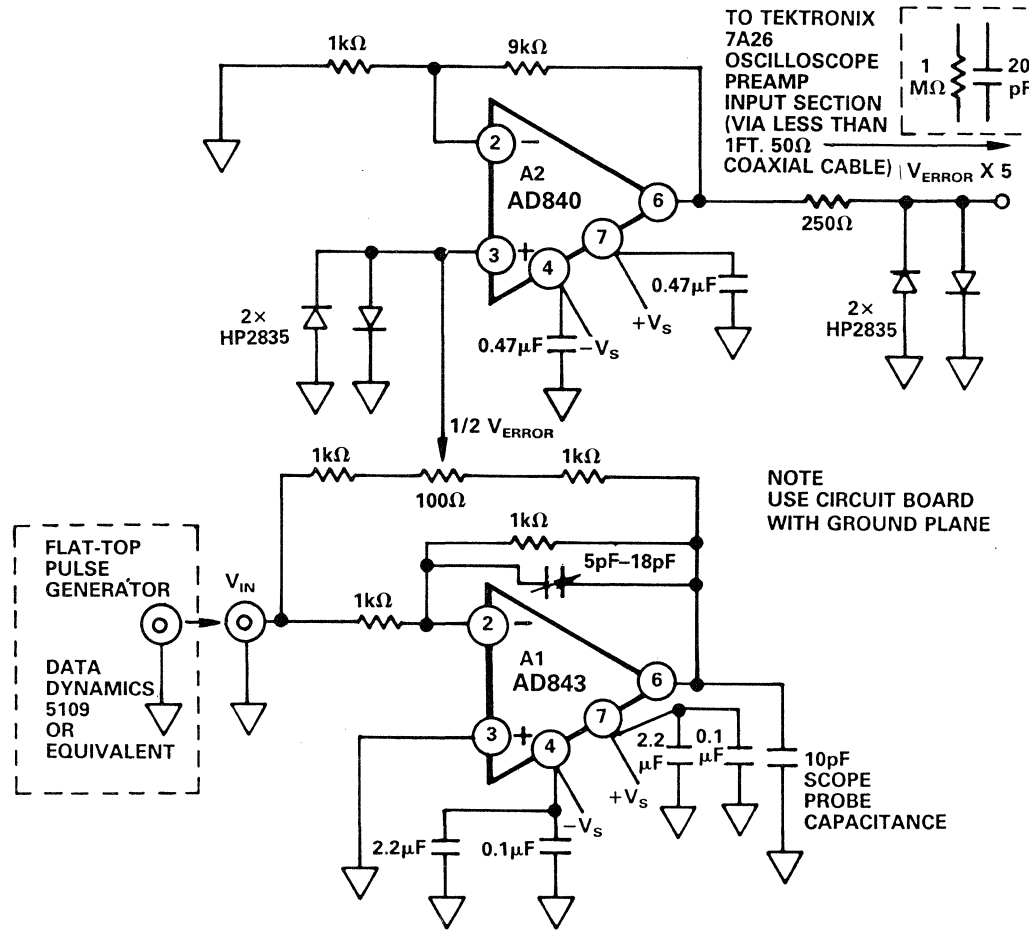
GAIN = −10; 5V OUTPUT; ERROR WINDOW (±5mV) = 0.1%; 5ns/DIV

AD9610 SETTLING TIME

Figure 4.22

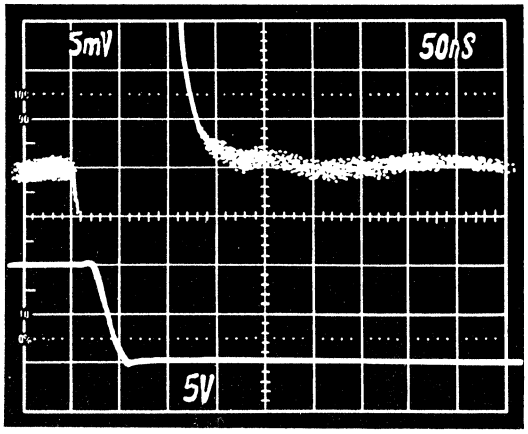
In order to duplicate results like these, excellent high speed layout techniques must be used. Attention must be given to insure a massive ground plane, compact layout, appropriate decoupling, and the use of pin sockets for the amplifier (if sockets must be used at all).

Another test configuration especially useful for measuring settling times of over 80ns to 12-bit accuracy (0.01%) is shown in Figure 4.23. This shows the test setup for the AD843 high speed FET input op amp which settles to 0.01% in less than 135ns. The actual settling time characteristics are shown in Figure 4.24.



GREATER THAN 80ns SETTLING TIME TEST CIRCUIT

Figure 4.23



UPPER TRACE: AMPLIFIED ERROR VOLTAGE (0.01%/DIV)

LOWER TRACE: OUTPUT OF AD843 (5V/DIV)

AD843 FET INPUT OP AMP SETTLING CHARACTERISTIC FOR +10V TO 0V STEP

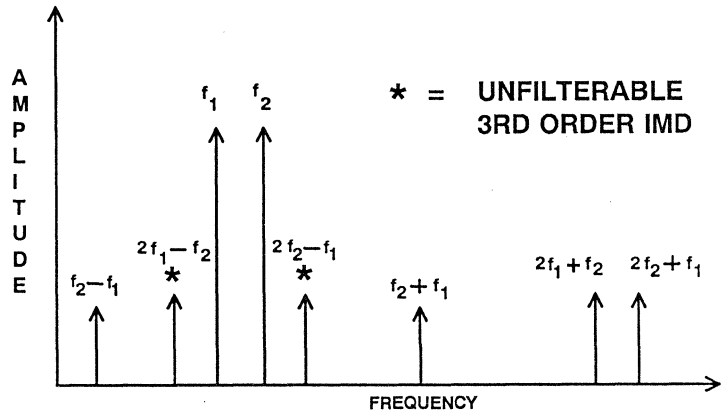
Figure 4.24

INTERMODULATION DISTORTION (IMD)

Intermodulation distortion occurs at frequencies that are the sam and/or different of integer multiples of the fundamental frequencies. Consider a non-linear amplifier with two large input signals at f_1 and f_2 (See Figure 4.25). The non-linearity gives rise to additional output components at $f_2 + f_1$ and $f_2 - f_1$: these are known as "second order intermodulation products". These second order products mix with the original signals and produce "third order intermodulation products" at frequencies of:

$2f_1 + f_2$ $\quad$ $2f_2 + f_1$
$2f_1 - f_2$ $\quad$ $2f_2 - f_1$

The third order products ($2f_1 - f_2$ and $2f_2 - f_1$) are a major nuisance in radio reception, especially in channelized systems, because they fall close to the signals causing them. Further discussion of IMD is given in the technical article at the end of this section as well as in Section V.



3RD ORDER INTERMODULATION DISTORTION

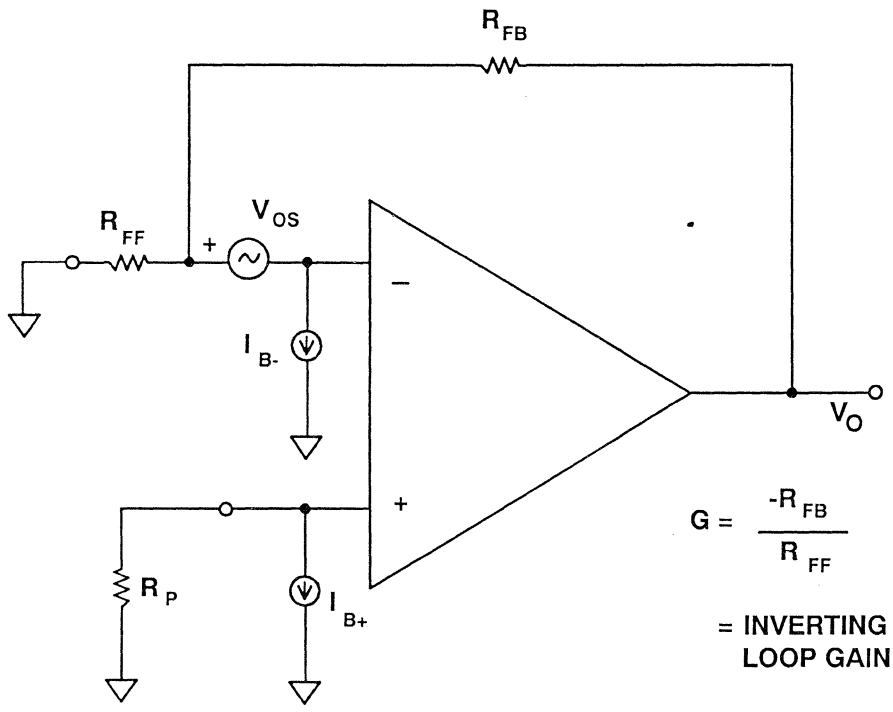
Figure 4.25

OP AMP BIAS CURRENT AND OFFSET VOLTAGE MODEL

Current feedback amplifiers must be treated somewhat differently from voltage feedback amplifiers when making output offset voltage calculations. The inverting and non-inverting inputs of standard voltage feedback op amps have similar characteristics, therefore the input bias currents are usually similar. In a current feedback amplifier, however, the inverting input is a low impedance emitter, while the non-inverting input is a high impedance. It is therefore quite likely that the respective input bias current characteristics will be different. The data sheet should always be consulted before making any assumptions.

A generalized bias current and offset voltage model for an op amp is shown in Figure 4.26. The equation for calculating the output offset voltage due to the input offset voltage and input bias currents is

easily derived by inspection. For op amps with well matched input bias currents, it is common to cancel the input bias currents by making $R_p = R_{FF} \parallel R_{FB}$. This is much less likely to be the case in current feedback op amps. Input offset voltages and bias currents are given in Figure 4.27 for several current feedback amplifiers. Due to differences in the inverting and non-inverting inputs, the input bias current temperature coefficients for current feedback amplifiers are likely to be different also. The data sheets should always be consulted.



OUTPUT OFFSET VOLTAGE =

$$V = (I_{B-})(R_{FB}) - (I_{B+})(R_P)(I - G) + V_{OS}(I - G)$$

V_{OS} = INPUT OFFSET VOLTAGE
I_{B-} = INVERTING INPUT BIAS CURRENT
I_{B+} = NONINVERTING INPUT BIAS CURRENT

OP-AMP OFFSET VOLTAGE/CURRENT MODEL

Figure 4.26

INPUT OFFSET VOLTAGE AND BIAS CURRENTS AT 25°C

	AD844	AD846	AD9610	AD9611	AD9615	AD9617/ 9618*
I_{B+}	0.15μA	0.003μA	15μA	5μA	2μA	12μA
I_{B-}	0.20μA	0.15μA	50μA	5μA	2μA	12μA
V_{os}	50μA	25μA	1mV	3mV	1mV	0.5mV

*Typical Specs

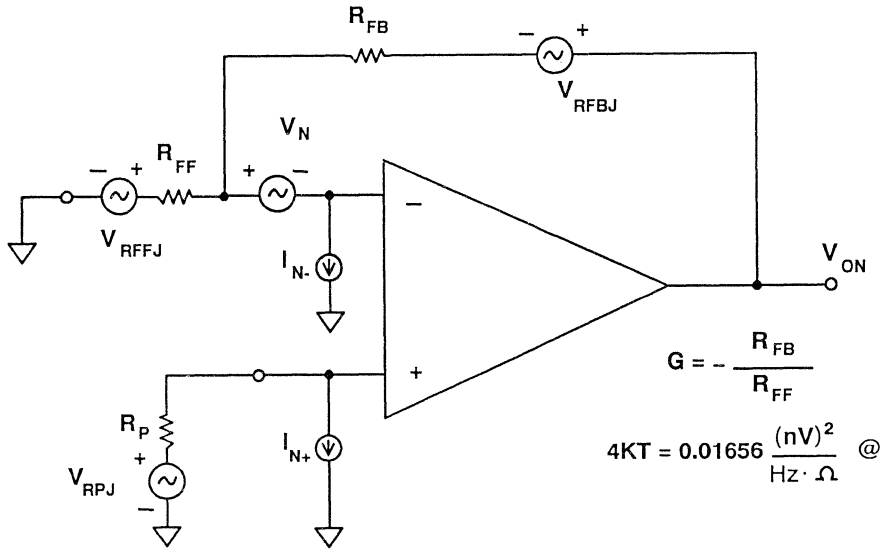
Figure 4.27

OP AMP NOISE MODEL

Current feedback amplifiers in general tend to be noisier than voltage feedback types when operating at low gains. The inverting and non-inverting input noise currents are also usually different. Figure 4.28 shows a generalized noise model which is applicable to all op amps including the current feedback variety. In addition to the input noise currents and voltages, the Johnson thermal noise voltages associated with the three resistors are also included. The equation is given for calculating the effective integrated output noise voltage in a given bandwidth. The appropriate values for I_{N-}, I_{N+}, and V_N are taken from the current and voltage noise spectral densities which are given on the data sheet. Usually the non-inverting input noise current I_{N+} is neglected because the non-inverting input is almost always grounded, bypassed, or driven from a low impedance source. In making noise performance comparisons between op amps, it is often useful to convert the output noise voltage to an effective integrated input noise voltage. This is easily accomplished by dividing the integrated output noise voltage by the noise gain, i.e., $1 + R_{FB}/R_{FF}$.

A noise current and voltage spectral density plot for the AD9611 is shown in Figure 4.29. The current noise is for the non-inverting and inverting input. Both the noise current and noise voltage are a function of frequency but flatten out above 10kHz where the 1/f current noise is no longer significant. In order to determine the effective noise over a bandwidth where the curves are not flat, the user must determine the areas under the respective curves for the bandwidth of interest.

Figure 4.30 shows a plot of the effective integrated output noise for the AD844 current feedback op amp. Note that at low closed loop gains the predominant noise source is the input current noise which flows through the feedback resistor (1000 Ω). For closed loop gains greater than 15, however, the effects of the "gained-up" input voltage noise begin to dominate the output noise.



EFFECTIVE INTEGRATED OUTPUT NOISE =

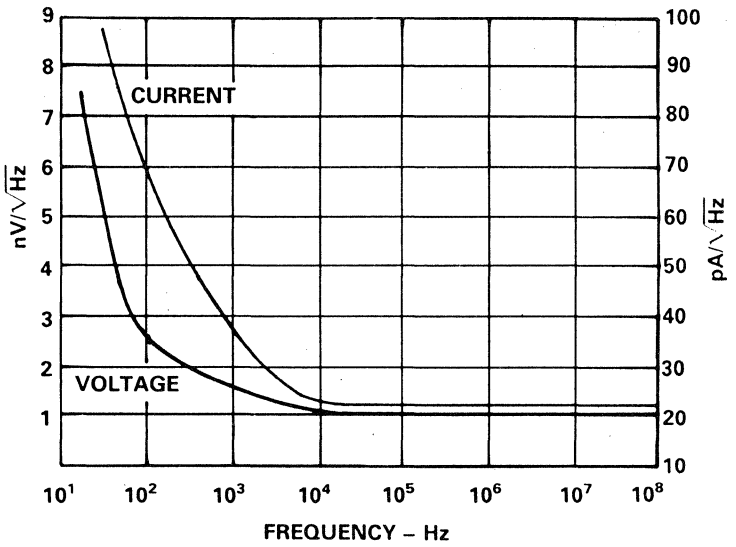
$$V_{ON} = \sqrt{BW}\left[I_{N-}^2 R_{FB}^2 + I_{N+}^2 R_P^2 (I-G)^2 + V_N^2 (I-G)^2 + 4KTR_{FB} + 4KTR_{FF} G^2 + 4KTR_P (I-G)^2\right]^{\frac{1}{2}}$$

EFFECTIVE INTEGRATED INPUT NOISE =

$$V_{IN} = \frac{V_{ON}}{I - G}$$

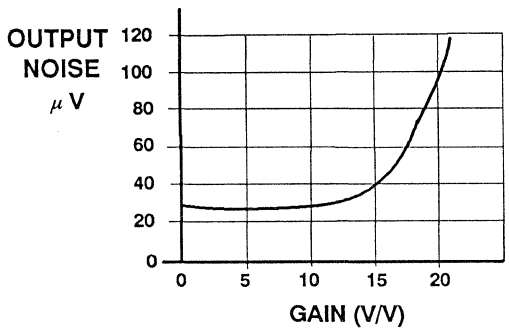
OP-AMP NOISE MODEL

Figure 4.28



INPUT NOISE VS. FREQUENCY FOR AD9611

Figure 4.29



BW = 10MHz

R_{FB} = 1000 Ω

R_P = 0

EQUIVALENT INTEGRATED OUTPUT NOISE VS. GAIN FOR AD844

Figure 4.30

HIGH SPEED OP AMP APPLICATIONS

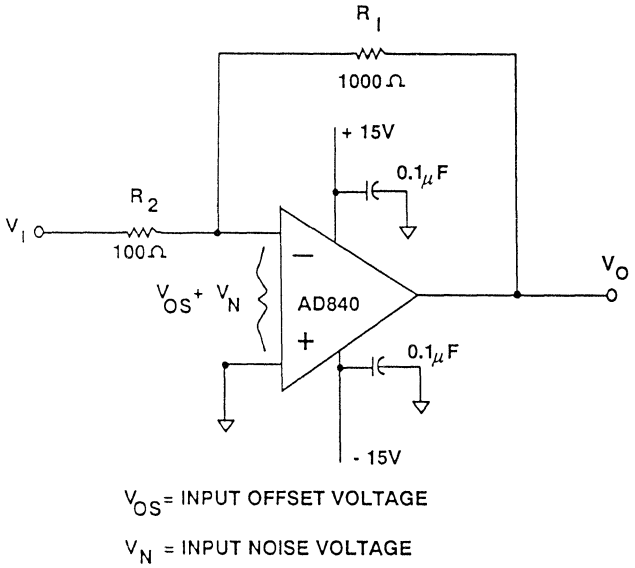
Stabilizing High Gain Op Amps at Lower Gain

In some cases, it is convenient to use an op amp that is internally compensated to be stable at a high closed loop gain at a lower gain. For example, this may minimize the number of amplifier types that are required to fill the sockets in an instrument.

The way to accomplish this is to operate the amplifier at a higher noise gain than signal gain, as illustrated in Figure 4.31 and 4.32, for a G = 10 stable amplifier in the inverting configuration. This technique can be applied to followers, but it is much trickier since the circuits' stability will depend on the input signal's source impedance.

The AD840 is stable in the inverted circuit Figure 4.31 because it is operating at a noise gain of 11 which is greater than its minimum stable noise gain of 10. In this case, the magnitude of the noise and signal gains are almost equal.

Figure 4.32 illustrates the extension of the Figure 4.31 circuit to stable operation at a gain of -1, which implies a noise gain of 2,



$$G = -\frac{R_1}{R_2} = \text{SIGNAL GAIN} = -10$$

$$1 - G = 1 + \frac{R_1}{R_2} = \text{NOISE GAIN} = 11$$

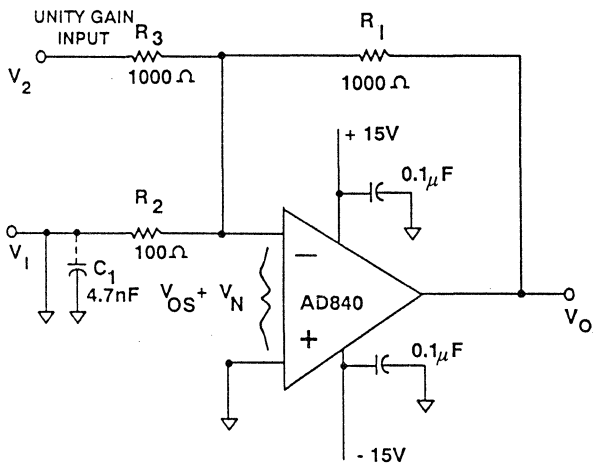
$$V_O = -\frac{R_1}{R_2} \cdot V_1 + \left(1 + \frac{R_1}{R_2}\right)\left(V_{OS} + V_N\right)$$

$$V_O = -10\,V_1 + 11\,(V_{OS} + V_N)$$

SIGNAL GAIN NOISE GAIN

NORMAL INVERTING MODE CONFIGURATION FOR MINIMUM GAIN (G = 10) OPERATION: AD840

Figure 4.31



$$V_O = -\frac{R_1}{R_2} \cdot V_1 - \frac{R_1}{R_3} \cdot V_2 + \left(1 + \frac{R_1}{R_2 \,||\, R_3}\right)\left(V_{OS} + V_N\right)$$

$$= -10V_1 - V_2 + 12\,(V_{OS} + V_N)$$

FOR $V_1 = 0$

$$V_O = -1\,V_2 + 12\,(V_{OS} + V_N)$$

SIGNAL GAIN; NOISE GAIN

FOR V_1 GROUNDED THROUGH C_1:

$$V_O = -V_2 + 2V_{OS} + 12V_N$$

LOW GAIN OPERATION FOR OP AMP WITH G_{MIN} = 10, THE AD840

Figure 4.32

far lower than the factor of 10 the AD840 requires for stability. A 1kΩ resistor is connected to the inverting terminal to provide a unity gain input for V_2. The G = -10 input, V_1, is grounded to maintain the high noise gain required for stability. Alternatively, a signal can be applied to the V_1 input from a source with an impedance much less than the 100Ω value of R_2. In this case, the output voltage will be:

$$V_0 = -10V_1 - V_2 + 12 \text{ (offset + noise)}$$

Note that the amplifiers input offset and noise "see" the noise gain of 12 so essentially this circuit trades off increased output noise and drift to achieve stability at G = -1. The output offset error can be substantially reduced by AC coupling the V_1 input (through C_1). The R_2C_1 time constant should be about 500ns (or about 100 times the circuit closed loop time constant of 5ns) to minimize distortion of the pulse response.

The small signal -3dB bandwidth will be the same for either the V_1 or V_2 inputs and in this case will be approximately 40MHz, the AD840's closed loop bandwidth at G = 10.

If the V_1 input is left open or is driven from high (>>100Ω) source impedance, the noise gain will be 2 and the circuit will oscillate. This technique can be extended to a larger number of arbitrarily weighted inputs or to other minimum stabile noise gains by insuring that this condition is met:

$$1 + \frac{R_1}{R_2 \,||\, R_3 \,||\, \cdots\, R_N} \geq G_{MIN},$$

Where G_{MIN} is the specified minimum stable (noise) gain of the amplifier.

HIGH SPEED OP AMP APPLICATIONS

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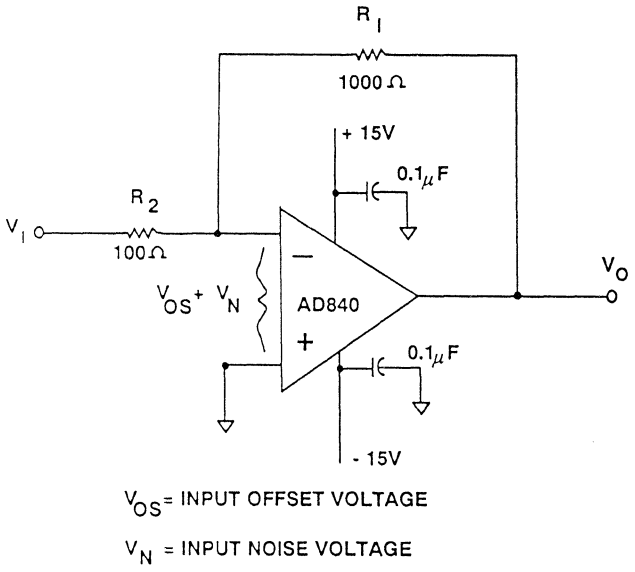

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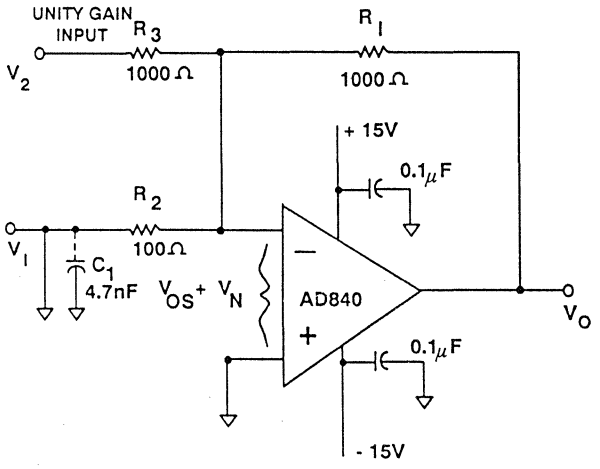
SIGNAL GAIN NOISE GAIN

NORMAL INVERTING MODE CONFIGURATION FOR MINIMUM GAIN (G = 10) OPERATION: AD840

Figure 4.31



$$V_O = -\frac{R_1}{R_2} \cdot V_1 - \frac{R_1}{R_3} \cdot V_2 + \left(1 + \frac{R_1}{R_2 \| R_3}\right)(V_{OS} + V_N)$$

$$= -10V_1 - V_2 + 12\,(V_{OS} + V_N)$$

FOR $V_1 = 0$

$$V_O = -1\,V_2 + 12\,(V_{OS} + V_N)$$

SIGNAL GAIN — NOISE GAIN

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$$1 + \frac{R_1}{R_2 \| R_3 \| \cdots R_N} \geq G_{MIN},$$

Where G_{MIN} is the specified minimum stable (noise) gain of the amplifier.

Driving Capacitive Loads with Wideband Op Amps

Most wideband amplifiers are sensitive to capacitive loading. In general, the higher the closed loop operating bandwidth, the greater the sensitivity.

A wideband amplifier will usually tolerate a small amount of capacitive loading and still maintain rated performance specifications. As the capacitive loading is increased, the performance is degraded (longer settling time, ringing and overshoot, etc.). Unless the amplifier has been designed to be unconditionally stable for all capacitive loads (AD847, AD848, AD849), as the capacitive loading is further increased, a point will be reached where the amplifier becomes unstable and oscillates. In order to prevent this instability, external compensation circuits are required which will reduce the overall closed loop bandwidth.

A list of wideband amplifiers and their relative tolerance to capacitive loads is given in Figure 4.33 and Figure 4.34.

VOLTAGE FEEDBACK OP AMP CAPACITIVE LOADING

MODEL	BW AT MIN CLOSED LOOP GAIN	C_L MAX FOR RATED PERFORMANCE	C_L MAX FOR STABILITY
AD840	40 MHz	20 pF	100 pF
AD841	40 MHz	20 pF	100 pF
AD842	40 MHz	20 pF	100 pF
AD843	35 MHz	20 pF	100 pF
AD845	16 MHz	20 pF	100 pF
AD847	50 MHz	10 pF	NO LIMIT
AD848	35 MHz	10 pF	NO LIMIT
AD849	30 MHz	10 pF	NO LIMIT

Figure 4.33

CURRENT FEEDBACK OP AMP CAPACITIVE LOADING

MODEL	BW AT MAIN CLOSED LOOP GAIN	C_L MAX FOR RATED PERFORMANCE	C_L MAX FOR STABILITY
AD844	67 MHz	10 pF	100 pF
AD846	46 MHz	20 pF	100 pF
AD9610	100 MHz	10 pF	10 pF
AD9611	300 MHz	5 pF	5 pF
AD9615	250 MHz	5 pF	5 pF
AD9617	185 MHz	10 pF	10 pF
AD9618	160 MHz	10 pF	10 pF

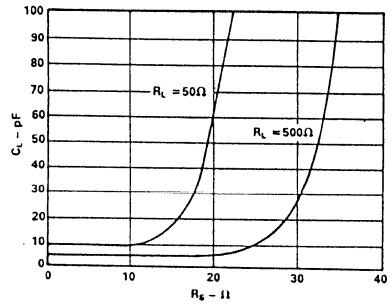
Figure 4.34

Various circuits can be used to compensate for excessive ringing, peaking and instability when driving capacitive loads. A series resistor between the op amp output and the capacitive load is often used. The graph is Figure 4.35 shows how to select the appropriate series isolation resistor R_S as a function of the capacitive and resistive load for the AD9611 and AD9615 current feedback op amps.

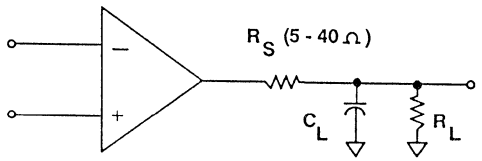
Figure 4.36 shows a typical circuit for driving a large capacitive load with the AD841 voltage feedback op amp. The 51Ω output resistor isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the summing junction via the low pass filter formed by the 51Ω resistor and the load capacitance C_L.

Figure 4.37 shows a similar circuit using the AD843 BiFET op amp to drive a 110pF load. Pulse response is shown in Figure 4.38. The AD843 is configured as a unity gain non-inverting buffer. In Figure 4.39, the AD843 is configured as a unity gain inverter, and its response is shown driving a 410pF load in Figure 4.40.

A circuit for driving a 1000pF load using the AD844 current feedback amplifier is shown in Figure 4.41. The feed forward-network is connected between the TZ pin (pin 5) and the output pin (pin 6). By using this external network capacitive drive capability can be extended to over 10,000pF, limited only by the internal power dissipation.

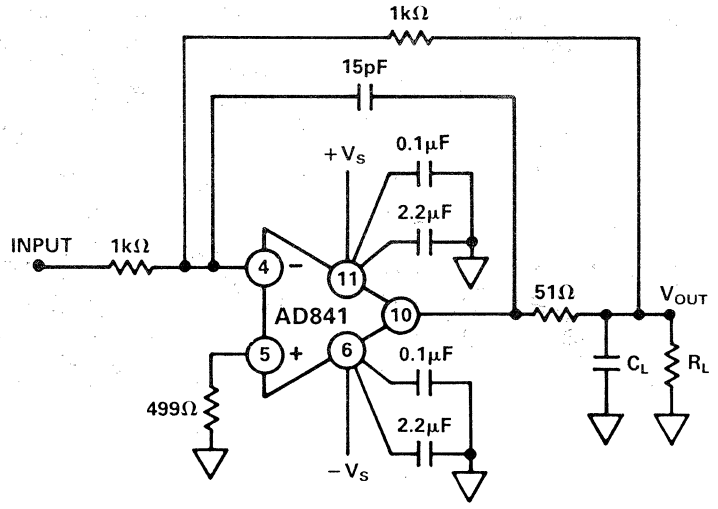


AD9611 CURRENT FEEDBACK
AD9615 OP AMPS



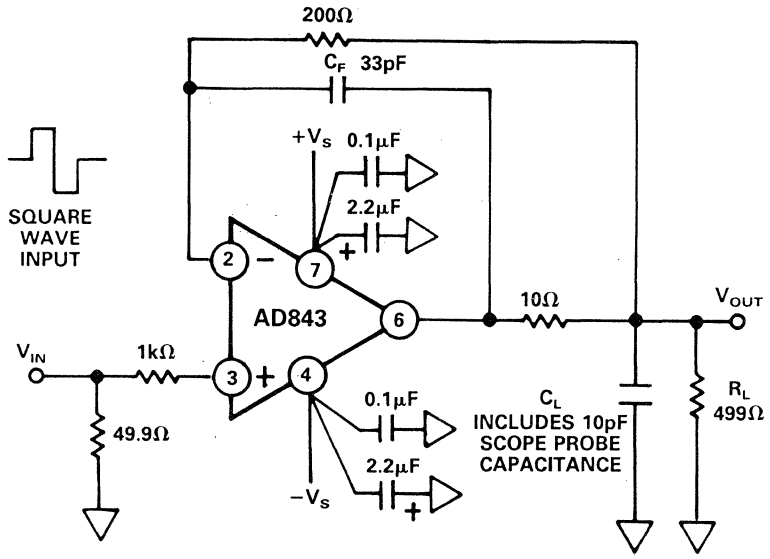
COMPENSATION WHEN DRIVING CAPACITIVE LOADS

Figure 4.35



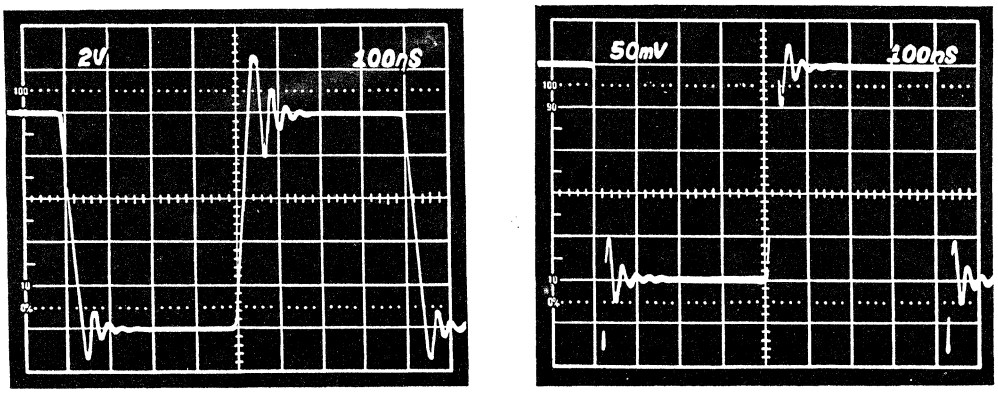
CIRCUIT FOR DRIVING A LARGE CAPACITIVE LOAD WITH THE AD841

Figure 4.36



UNITY GAIN BUFFER CIRCUIT FOR DRIVING CAPACITIVE LOADS WITH THE AD843

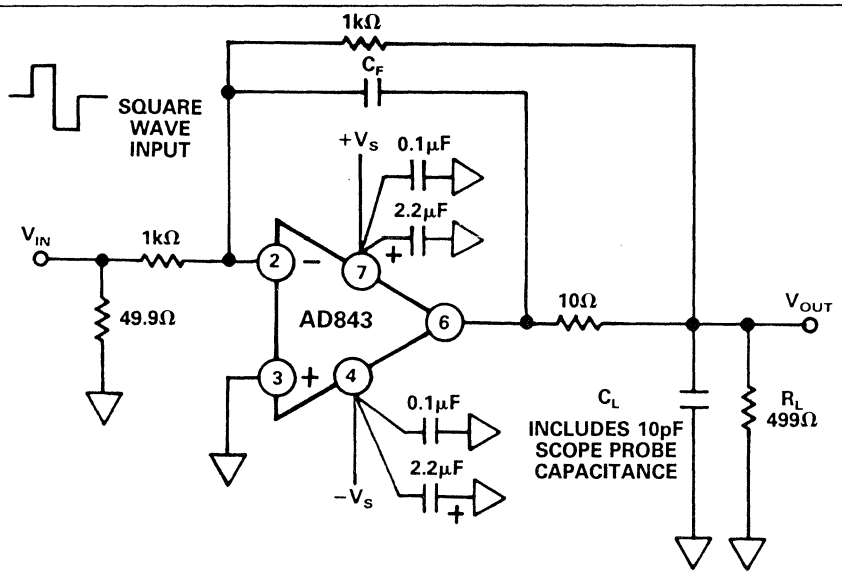
Figure 4.37



LARGE SIGNAL SMALL SIGNAL

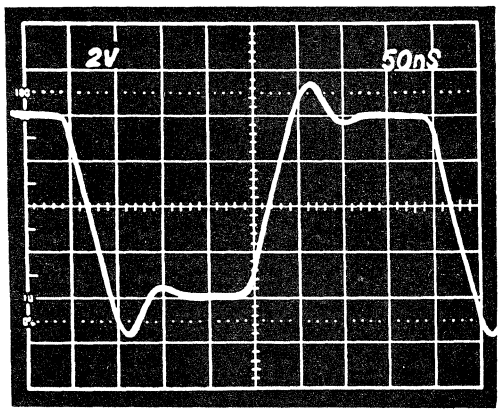
AD843 BUFFER RESPONSE, C_L = 110pF, C_F = 33pF

Figure 4.38

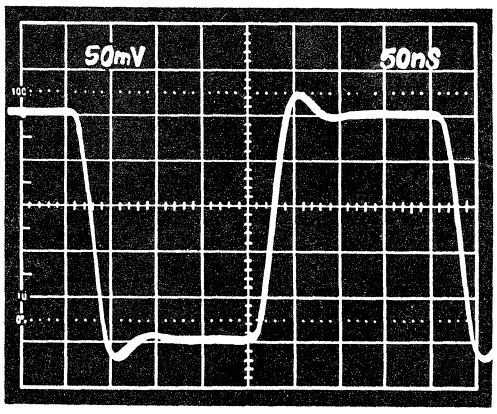


UNITY GAIN INVERTER CIRCUIT FOR DRIVING CAPACITIVE LOADS WITH AD843

Figure 4.39



LARGE SIGNAL

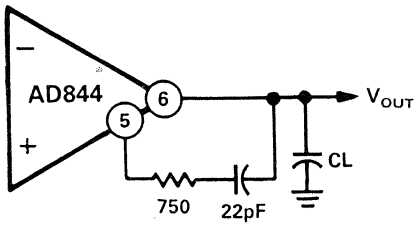


SMALL SIGNAL

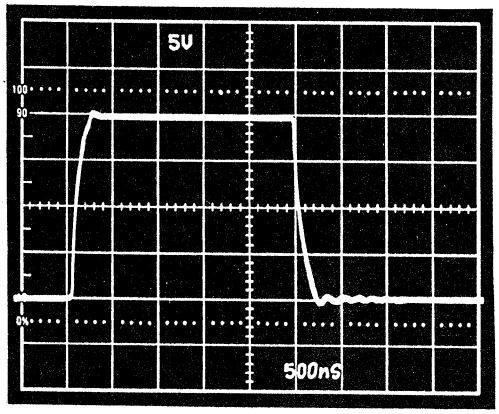
AD843 INVERTER RESPONSE, C_L = 410pF, C_F = 15pF

Figure 4.40

The AD847, AD848 and AD849 voltage feedback op amps are internally compensated to remain stable driving any value of capacitive load. The photographs in Figure 4.42 show the large signal pulse response of the AD847 driving a 100pF and a 1000pF load.



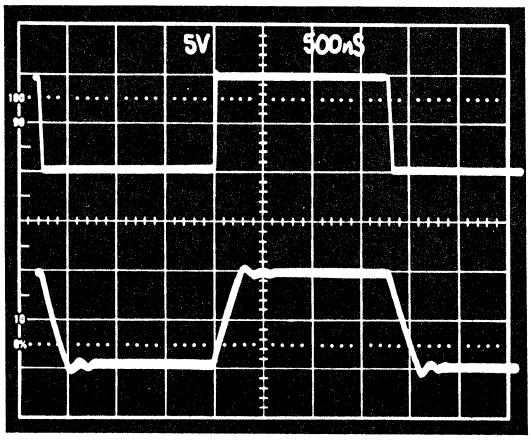
FEED FORWARD NETWORK
FOR LARGE CAPACITIVE LOADS



PULSE RESPONSE
FOR C_L = 1000pF

DRIVING LARGE CAPACITIVE LOADS WITH THE AD844

Figure 4.41

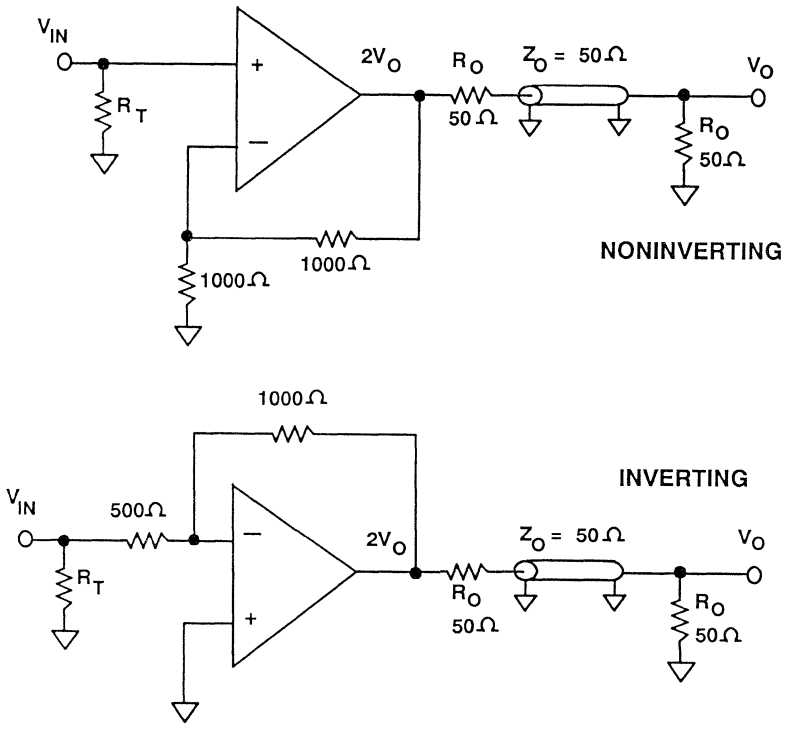


AD847 DRIVING A CAPACITIVE LOAD - NO EXTERNAL COMPENSATION

Figure 4.42

High Speed Cable Drivers and Receivers

High speed amplifiers are ideally suited for driving coaxial cables. The preferred methods are shown in Figure 4.43. Best performance is obtained by both series and load terminating the cables in order to prevent unwanted reflections. This requires that the amplifier be configured for a gain of 2 in order to maintain the original signal amplitude. If the cable is neither series or load terminated it appears as a capacitive load to the amplifier, and the suggestions in the previous section should be followed.

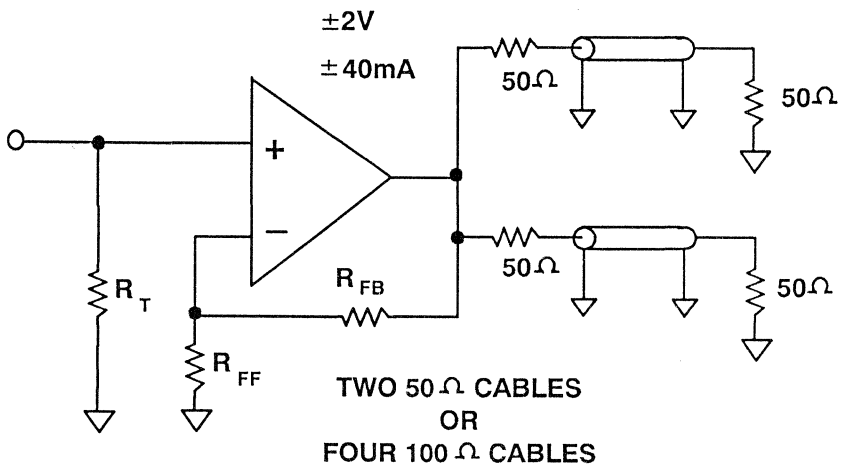


NONINVERTING AND INVERTING CABLE DRIVERS

Figure 4.43

Multiple cables can be driven by a single op amp as shown in Figure 4.44 provided the output current capability of the amplifier is not exceeded.

Appropriate values for the feedback and feedforward resistors are given in Figure 4.45 for a variety of wideband amplifiers.



DRIVING MULTIPLE CABLES

Figure 4.44

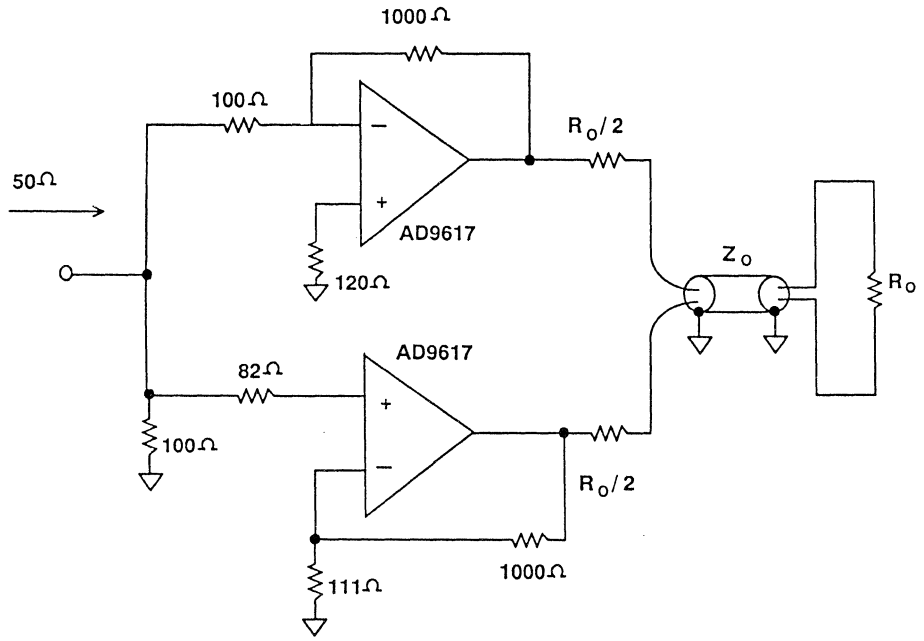
HIGH SPEED CABLE DRIVERS

MODEL	R_{FF}	R_{FB}	I_{OUT}	BW
AD841	402Ω	402Ω	50 mA	20 MHz
AD842	402Ω	402Ω	100 mA	40 MHz
AD847	402Ω	402Ω	25 mA	25 MHz
AD9610	1500Ω	1500Ω	50 mA	100 MHz
AD9611	1000Ω	1000Ω	40 mA	300 MHz
AD9615	1500Ω	1500Ω	40 mA	250 MHz
AD9617	402Ω	402Ω	50 mA	180 MHz

Figure 4.45

A circuit using two amplifiers to convert a single ended signal to a differential signal is shown in Figure 4.46. By using this circuit, a signal can be transmitted over a cable having high common mode noise.

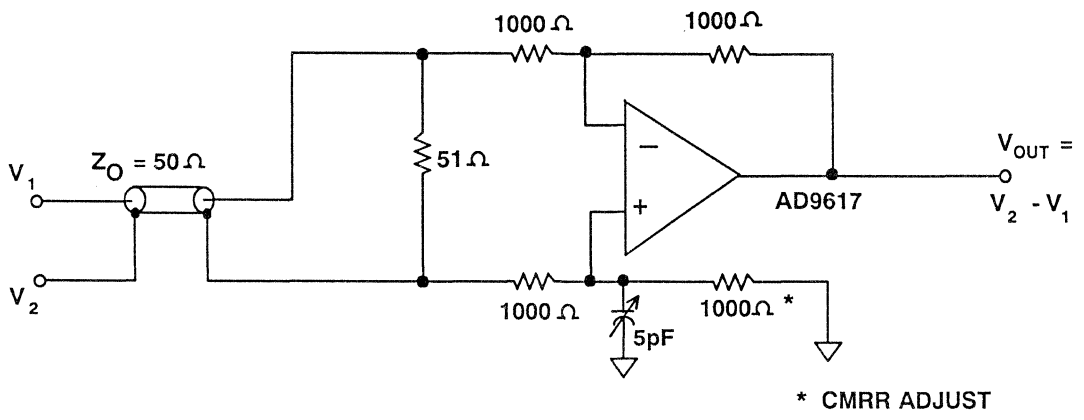
By receiving the signal with a wideband instrumentation amplifier, the common mode noise can be rejected, and the differential signal recovered at the output of the instrumentation amplifier.



SINGLE-ENDED TO DIFFERENTIAL CONVERSION

Figure 4.46

If the common mode rejection ratio at high frequencies is high enough, an op amp can effectively be used as a differential-to-single ended converter as shown in Figure 4.47. The circuit can be used to receive true differential signals or signals from coaxial cables with floating shields. Common mode noise is attenuated by the op amps CMRR.

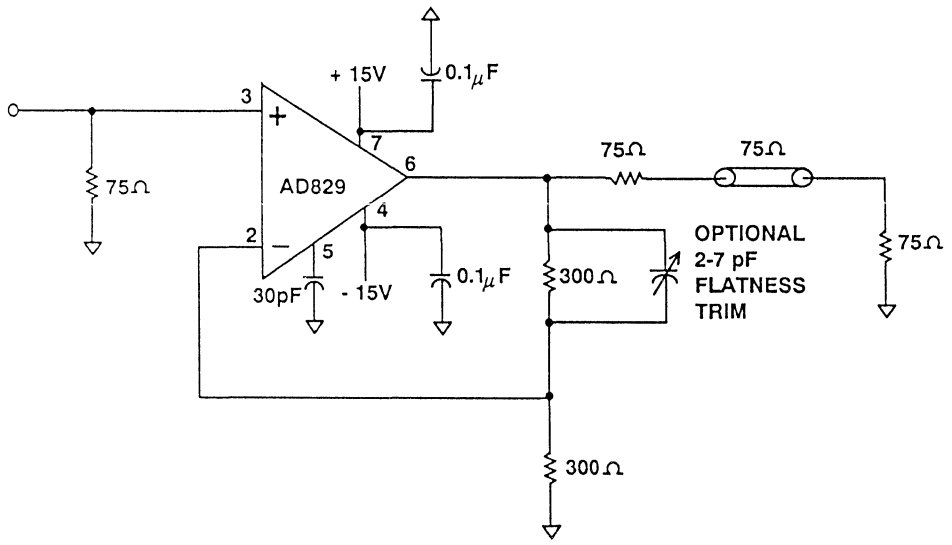


COAXIAL CABLE DIFFERENTIAL RECEIVER

Figure 4.47

Low Differential Gain and Phase Video Line Driver

The buffer circuit shown in Figure 4.48 will drive a back-terminated 75Ω video line to standard video levels (1V p-p) with 0.1 dB gain flatness to 30 MHz with only 0.02^0 and 0.02% differential phase and gain at the 4.43 MHz PAL color subcarrier frequency. This level of performance, which meets the requirements for high-definition video displays and test equipment, is achieved at just 6 mA quiescent current.



LOW DIFFERENTIAL GAIN AND PHASE VIDEO LINE DRIVER: AD829

Figure 4.48

Precision Measurement of Differential Gain and Phase

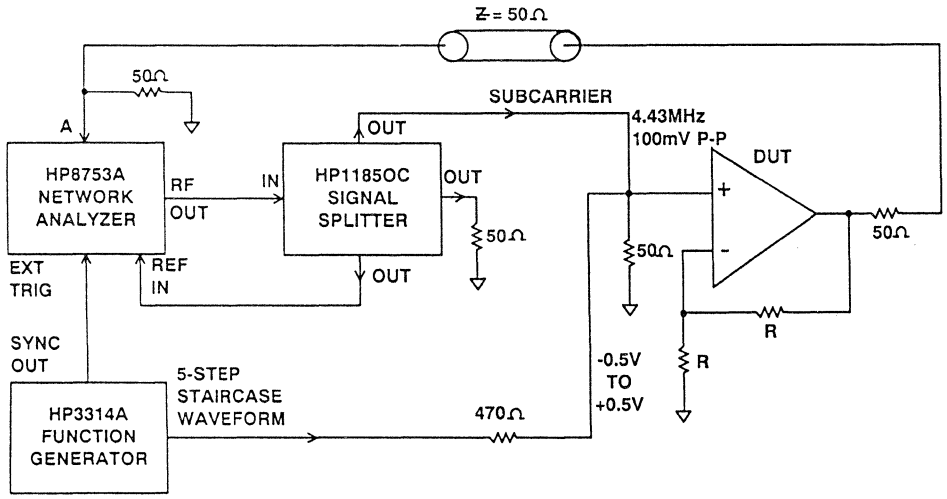
In a television transmission system, a phase- and amplitude-modulated subcarrier carries color (chrominance) information. In the National Television Standards Committed (NTSC) system used in the U.S. and Japan, the color subcarrier is at 3.58 MHz. The PAL (used in the U.K. and West Germany) and SECAM (used in France) systems use a 4.43 MHz color subcarrier. Any amplitude or phase modulation introduced on the subcarrier by the video transmission system can result in a color change for the viewer. Thus, video systems have stringent requirements for differential phase and gain, usually limiting changes to less than 0.1^0 and 0.1%.

These systems specifications mandate even more stringent standards for individual components, with the differential phase and differential gain requirements for the op amps used in video systems ideally approaching 0.01^0 and 0.01%. Measuring these levels exceeds the resolution of normal video test equipment, which is about the same as system-level specifications at 0.1^0 differential phase and 0.1% differential gain.

Figure 4.49 shows a high resolution setup that uses a HP3314A arbitrary waveform generator and a HP8753A network analyzer to measure differential phase and gain to 0.01^0 and 0.01% accuracy. The

arbitrary waveform generator generates a staircase that simulates the luminance (picture level) portion of a video waveform. The network analyzer supplies the color subcarrier waveform, in this case a 4.43 MHz color subcarrier. The network analyzer also measures the differences in the color subcarrier's phase and gain by comparing the output of the DUT and the reference signal returned by the HP11850 signal splitter.

Note that the 4.43 MHz color subcarrier and the staircase signal are summed at the input to the op amp. This summing action superimposes the color subcarrier on the staircase, thus generating the standard video test waveform. The differential phase and gain is defined as the maximum difference in the phase or gain between any of the steps in the staircase waveform. The differential phase and gain measurements are made and plotted separately. In each case, the horizontal scale shows the modulating staircase and the vertical scale shows the relative differences in phase and gain.

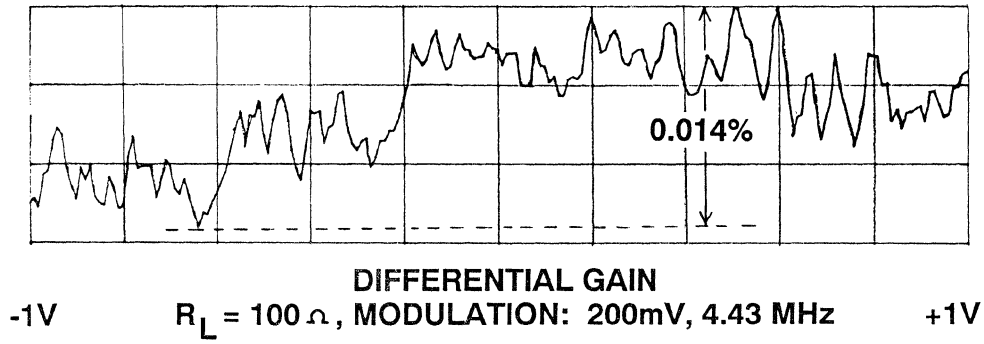


PRECISION MEASUREMENT OF DIFFERENTIAL GAIN

Figure 4.49

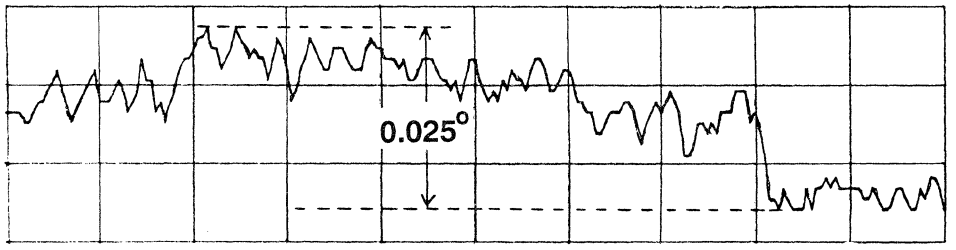
Figure 4.50 shows the differential gain of the AD829 plotted at a scale of 0.005% per vertical division for a -1V to +1V staircase. Note that the total differential gain is 2.6 divisions, or 0.013%. Figure 4.50 also shows the AD829's differential phase plotted on a vertical scale of 0.01^0 per vertical division. Note that the total differential phase is 2.7 divisions, or 0.027^0.

The circuit in Figure 4.49 also shows an op amp connected as a gain-of-2 amplifier driving a 50Ω reverse-terminated line. The 50Ω termination resistor both absorbs reflections from the line and isolates the op amp from the capacitive load presented by the line. The 50Ω termination resistor and the 50Ω load form a voltage divider, so the net gain from the input to the DUT circuit to the load is unity. It should be noted that this represents a more stringent condition than conventional video systems where 75Ω is the standard impedance level.



DIFFERENTIAL GAIN

-1V R_L = 100 Ω, MODULATION: 200mV, 4.43 MHz +1V



DIFFERENTIAL PHASE

AD829 DIFFERENTIAL GAIN AND PHASE

Figure 4.50

Driving A/D Converters

Wideband low distortion op amps are required to drive high performance A/D converters. Each A/D architecture (flash, successive approximation, and subranging) places unique requirements on the drive amplifier.

Flash ADCs require amplifiers of wide bandwidth and low distortion. Since a flash converter's input is capacitive, a small isolation resistor is often required between the op amp output and the flash converter input to maintain op amp stability. The input capacitance of the flash converter is usually signal-dependent, therefore the series resistor should be kept as small as possible to minimize non-linearities.

It is also important that the signal-to-noise ratio and harmonic distortion performance of the drive amplifier not degrade basic performance of the flash converter. Curves such as those shown in Figure 4.51 are useful in selecting the appropriate drive amplifier.

For successive approximation ADCs, the input current is modulated at the summing point of the comparator during each bit comparison. The amplifier must re-establish the proper input voltage within 1/2 LSB before the comparator output is latched, or an error will be induced. This requires that the op amp driving a successive approximation ADC must have a low output impedance at DC, at the signal frequency, and at the frequency of the conversion clock of the ADC.

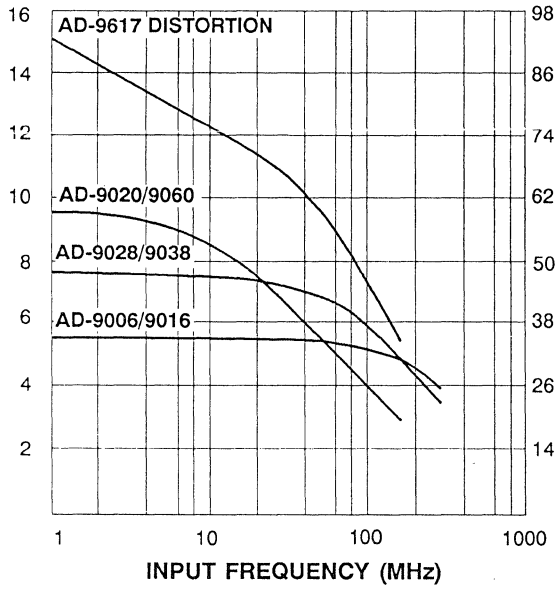
The AD846 op amp meets this requirement for most successive approximation ADCs. It is also suitable for driving subranging ADCs such as the AD671. Its output impedance at an inverting gain of 10 is 10Ω at 10 MHz. Furthermore, the AD846 is easily configured as a clamped amplifier to protect the ADC input.

If dynamic signals are to be digitized by a successive approximation ADC, a suitable SHA will be required to drive the ADC. In this case, the same requirements discussed above apply to the SHA output.

In the case of "sampling" ADCs (with internal SHAs) the drive amplifier should be selected to exceed the performance of the ADC -- especially in terms of bandwidth, distortion and noise.

EFFECTIVE BITS
(ENOB)

$$ENOB = \frac{SNR - 1.76dB}{6.02}$$



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS
AD770	8 BITS	200 MSPS
AD9002	8 BITS	125 MSPS
AD9012	8 BITS	75 MSPS
AD-9048	8 BITS	35 MSPS
AD9006/9016	6 BITS	400 MSPS

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE

Figure 4.51

A/D CONVERTERS AND RECOMMENDED DRIVE AMPLIFIERS

MODEL	RESOLUTION	MAX. SAMPLING RATE	INPUT C	DRIVE AMPLIFIER
AD9688	4-Bits	175 MSPS	10pF	AD5539
AD9000	6-Bits	75 MSPS	35pF	AD844
AD9006/16	6-Bits	500 MSPS	8.5pF	AD9617, AD9611
AD9048	8-Bits	35 MSPS	16pF	AD847, AD844
AD9012	8-Bits	75 MSPS	16pF	AD9617, AD846
AD9002	8-Bits	125 MSPS	16pF	AD9617
AD770	8-Bits	200 MSPS	19pF	AD9617
AD9028/38	8-Bits	300 MSPS	17pF	AD9617
AD9020/60	10-Bits	60 MSPS	45pF	AD9617
AD9003	12-Bits	1 MSPS	5pF	AD846
AD9005	12-Bits	10 MSPS	5pF	AD9617

Figure 4.52

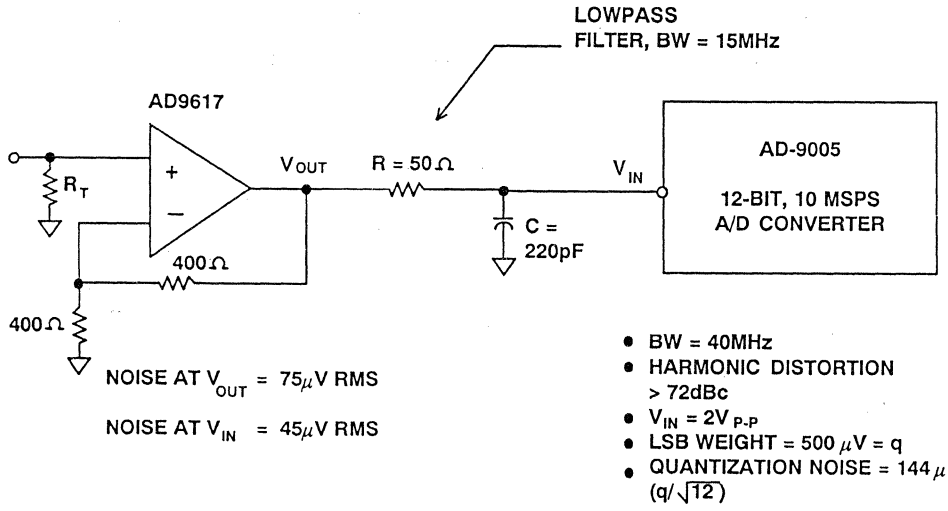
Driving High Performance 12-Bit A/D Converters

In order for the whole system to match the dynamic characteristics of the ADC itself, it is necessary to exercise great care in selecting amplifiers to drive such high speed, high performance converters as the AD9005 (a 12-bit 10MSPS ADC). For instance, the AD9005 front end bandwidth is 40MHz, and the harmonic distortion is 72dB down for a full-scale 4MHz input signal. The AD9617 current feedback amplifier harmonic distortion is approximately 80dB down under the same conditions, and will therefore not degrade the A/D converter distortion performance.

However, the effective integrated output noise voltage of the AD9617 in a 40MHz bandwidth is approximately 75 μV RMS, compared to the AD9005 LSB weight of 500 μV. A single pole lowpass filter having a 3dB bandwidth of 15MHz can be inserted between the amplifier and the A/D converter as shown in Figure 4.53.

This filter effectively reduces the RMS noise voltage to approximately 45 μV thereby improving the signal to noise ratio of the system without degrading the harmonic distortion.

The theoretical quantization noise for a 12-bit A/D converter with a 2-volt input range is $q/\sqrt{12}$, or 144 μV where q is the weight of the LSB. Combining the theoretical quantization noise of 144 μV and the integrated noise of 45 μV yields a theoretical value of 150 μV for the effective input noise to the A/D converter.



DRIVING A HIGH PERFORMANCE 12-BIT A/D CONVERTER

Figure 4.53

Use of High Speed Op Amps as D/A Converter Output Buffers

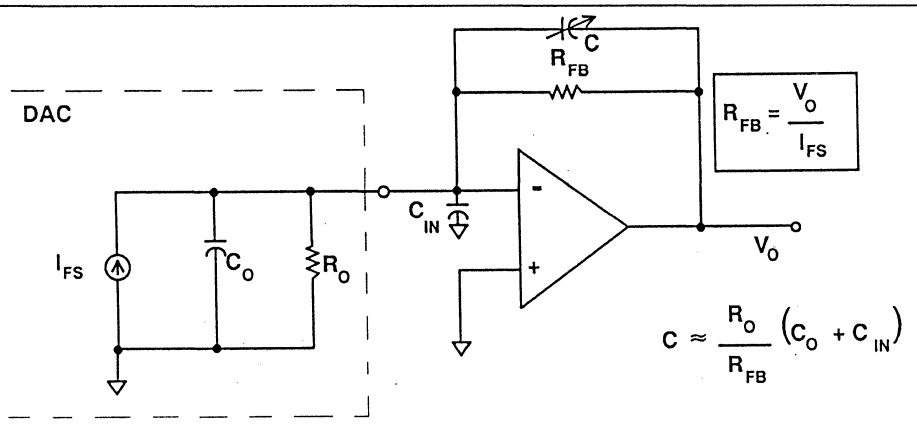
A D/A converter I to V conversion circuit using a voltage feedback op amp is shown in Figure 4.54. The value of the feedback resistor is chosen based on the fullscale D/A output current and the desired output voltage. The value of the feedback capacitor C is chosen to compensate for the pole formed by R_O, C_O, and C_{IN} in parallel with the amplifiers input resistance.

Using a current feedback amplifier with its low impedance inverting input eliminates the effects of the pole formed by R_O, C_O, and C_{IN}. It also eliminates the reduced slew rates caused by this pole. When using a current feedback amplifier with a feedback resistor value that has been optimized for best settling time and bandwidth, the D/A output current may be divided as shown in Figure 4.55 in order to provide the correct output voltage.

The series resistor R_{FF} also isolates the D/A output capacitance from the amplifier's inverting input. This capacitance could cause excessive peaking and possible instability if connected directly to the inverting input.

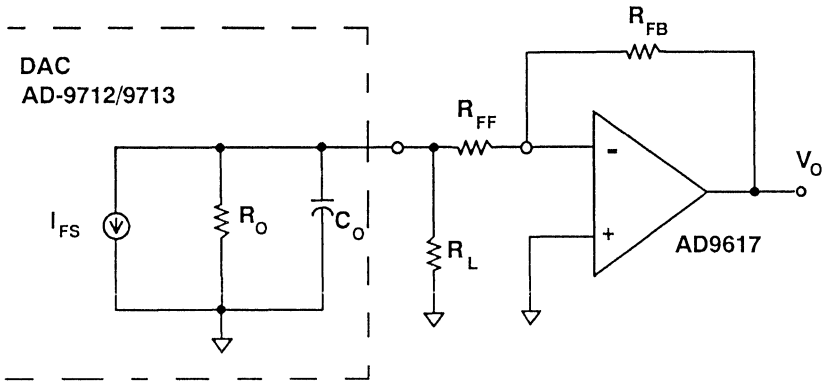
If the D/A output current matches the optimum feedback resistor and the desired output voltage, then the D/A output is connected directly to the inverting input as shown in Figure 4.56. The compensation capacitor is adjusted for optimum output pulse response and compensates for the D/A output capacitance.

Current feedback amplifiers can also be used in the non-inverting mode to buffer and amplify the D/A output. The circuit in Figure 4.57 amplifies the D/A output voltage I_{FS} R_O and provides a positive unipolar output.



D/A I TO V CONVERSION USING A VOLTAGE FEEDBACK OP AMP

Figure 4.54



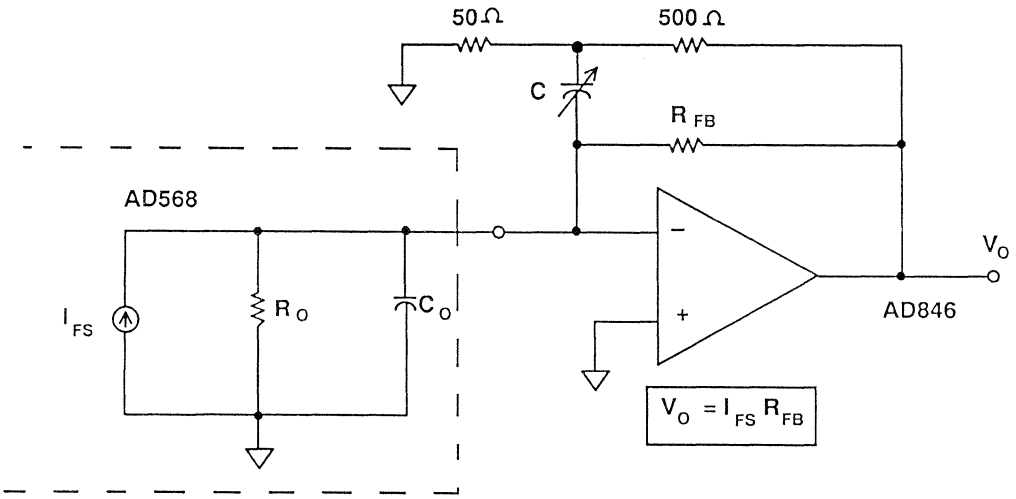
$$R_{FF} = \frac{R_O R_L}{R_O + R_L}\left[R_{FB} \cdot \frac{I_{FS}}{V_O} - 1\right]$$

I_{FS}= 20mA, R_O = 2500Ω, R_L = 50Ω, V_O = 2V

R_{FB}= 400Ω, R_{FF}= 147Ω, C_O = 30pF

I TO V CONVERSION USING CURRENT FEEDBACK AMPLIFIERS

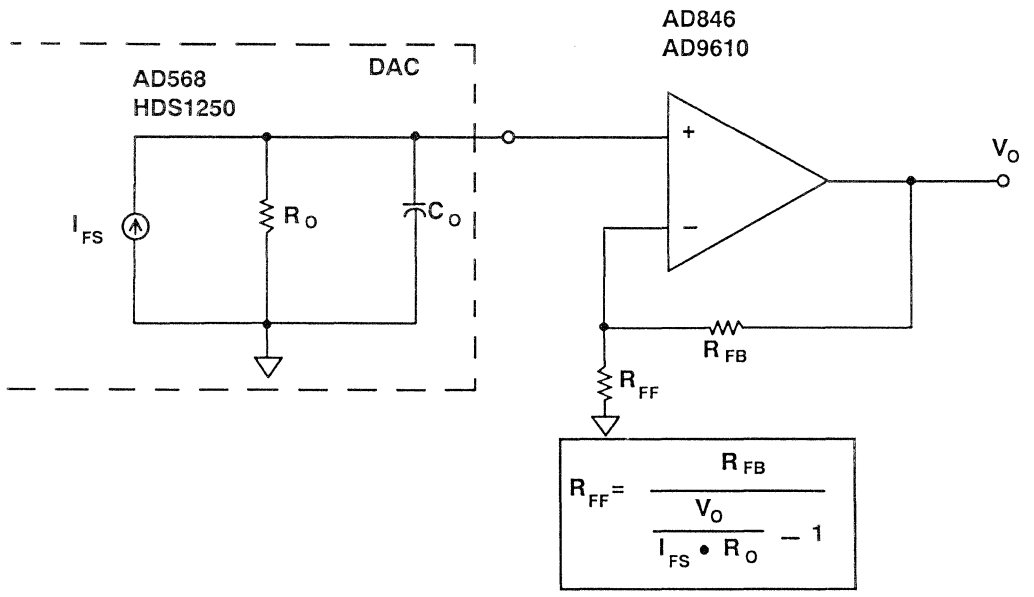
Figure 4.55



FOR D/A = AD568, OP-AMP = AD846
I_{FS} = 10mA, R_O = 100Ω, R_{FB} = 1000Ω, V_O = -10V
C_O = 15pF, C ≈ 5pF

I TO V CONVERSION USING CURRENT FEEDBACK AMPLIFIERS

Figure 4.56



FOR D/A = AD568, OP-AMP = AD846/AD9610
I_{FS} = 10mA, R_O = 100Ω , R_{FB} = 1000Ω , V_O = + 10V
R_{FF} = 111Ω

NONINVERTING D/A OUTPUT BUFFER

Figure 4.57

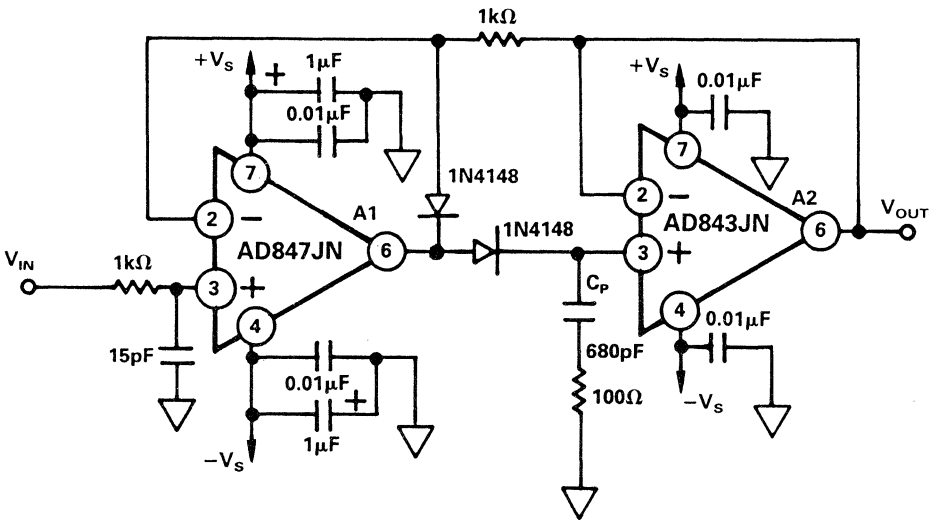
A Fast Peak Detector Circuit

The peak detector circuit of Figure 4.58 can accurately capture the amplitude of input pulses as narrow as 200 ns and can hold their value with a droop rate of less than 20 μV/μs. This circuit will capture the peak value of positive polarity waveforms; to detect negative peaks, simply reverse the polarity of the two diodes.

The high bandwidth and 200V/μ s slew rate of amplifier A2, an AD843, allows the detector's output to "keep up" with its input thus minimizing overshoot. The low (<1 nA) input current of the AD843 ensures that the droop rate is limited only by the reverse leakage of diode D2, which is typically <10 nA for the type shown.

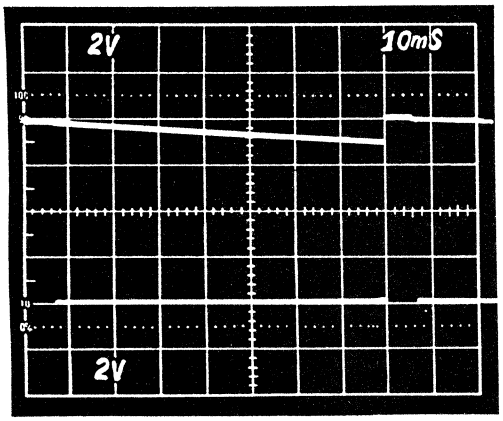
The low droop rate is apparent in Figure 4.59. The detector's output (top trace) loses slightly over a volt in the 8 volt peak input value (bottom trace) in 72 ms, or a rate of approximately 16 $\mu V/\mu s$.

Amplifier A1, an AD847, can drive 680pF hold capacitor, C_p, fast enough to "catch-up" with the next peak in 100 ns and still settle to the new value in 250 ns, as illustrated in Figure 4.59. Reducing the value of capacitor C_p to 100pF will maximize the speed of this circuit at the expense of increased overshoot and droop. Since the AD847 can drive an arbitrarily large value of capacitance, C_p can be increased to reduce droop, at the expense of response time.



A FAST PEAK DETECTOR CIRCUIT

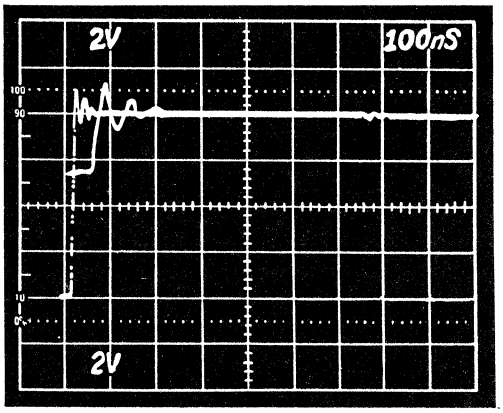
Figure 4.58



TOP TRACE: PEAK DETECTOR OUTPUT

BOTTOM TRACE: INPUT, 8V PEAK @ 125Hz

PEAK DETECTOR RESPONSE
TO 125 Hz PULSE TRAIN



TOP TRACE: PEAK DETECTOR OUTPUT, 8V

BOTTOM TRACE: INPUT VOLTAGE, 8V PEAK,
650ns PULSE WIDTH

PEAK CAPTURE TIME

PEAK DETECTOR WAVEFORMS

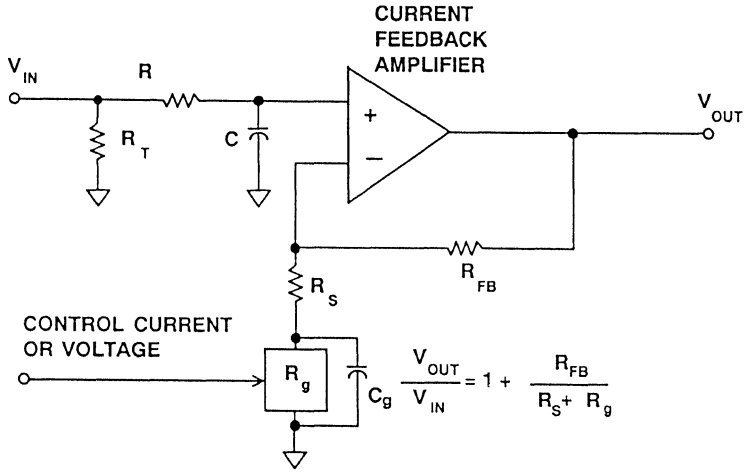
Figure 4.59

Variable Gain Current Feedback Amplifiers

Because their closed loop bandwidth is relatively independent of closed loop gain, current feedback amplifiers are excellent choices for variable gain applications. Figure 4.60 shows a simple circuit where the gain is changed by varying the control voltage or current to a variable resistance element, R_g, such as a FET or photoresistor. The series resistor R_S isolates the parasitic capacitance associated with the variable resistance and prevents peaking and instability. Peaking can also be eliminated at low gains by the addition of a simple RC network in series with the non-inverting input.

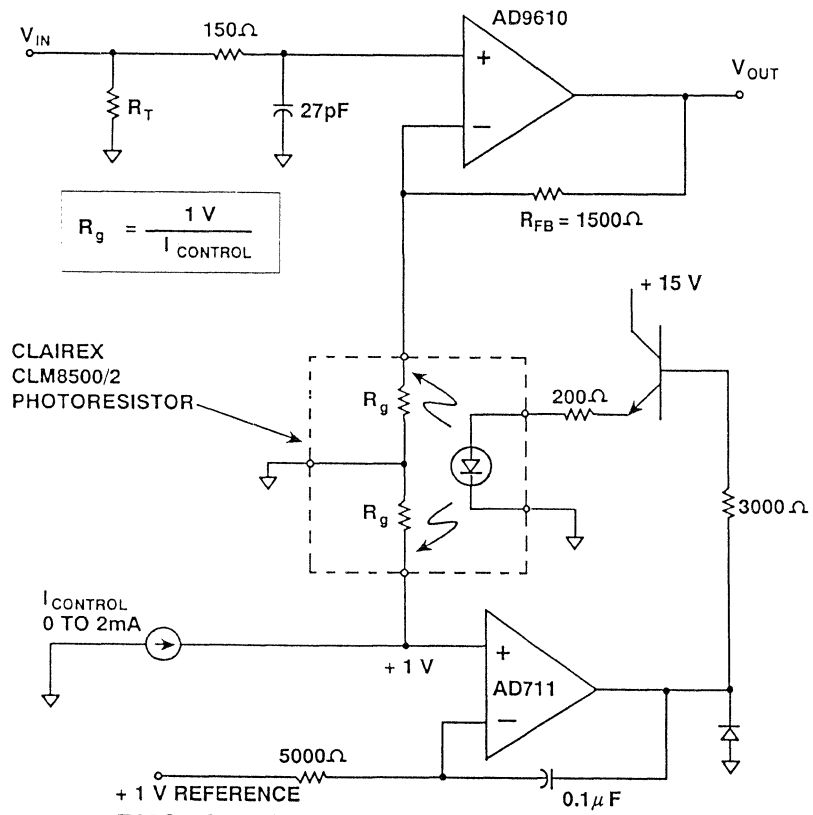
The circuit shown in Figure 4.61 used a photoresistor as the variable resistance element and provides a 12dB gain adjustment range. The gain remains flat within 1dB up to about 20MHz.

FETS can also be used as variable resistance elements, however, their on resistance varies with the drain-to-source voltage. This makes them virtually unusable if good harmonic distortion is required from the variable gain amplifier. The gain setting element resistance is signal dependent, thereby introducing undesirable non-linearities.



VARIABLE GAIN AMPLIFIER

Figure 4.60



PHOTORESISTOR VARIABLE GAIN CIRCUIT

Figure 4.61

20MHz Variable Gain Amplifier

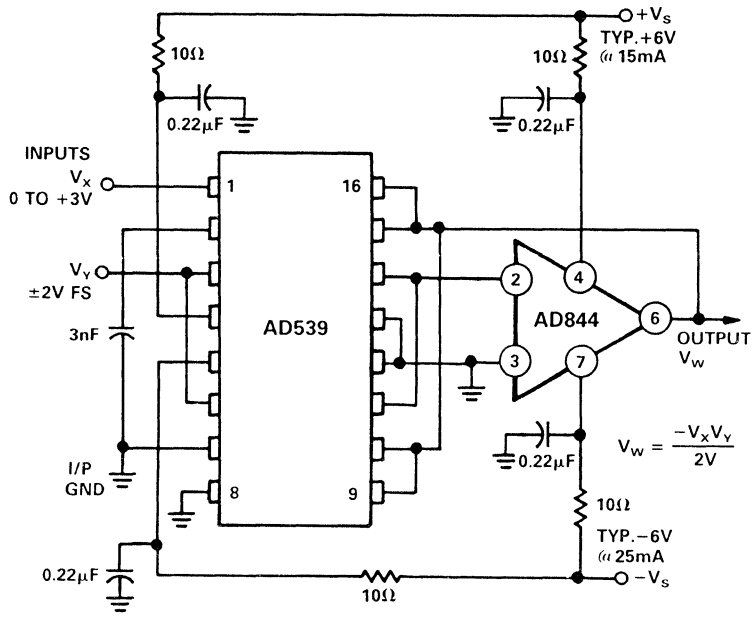
The AD844 is an excellent choice as an output amplifier for the AD539 multiplier, in all of its modes of operation. (See AD539 data sheet for full details.) Figure 4.62 shows a simple multiplier providing the output:

$$V_W = - \frac{V_X V_Y}{2V}$$

where V_X is the "gain control" input, a positive voltage of from 0 to +3.2V (max) and V_Y is the "signal voltage" nominally ±2V FS but capable of operation up to ±4.2V. The peak output in this configuration is thus ±6.7V. Using all four of the internal application resistors provided on the AD539 in parallel results in a feedback resistance of 1.5k Ω , at which value the bandwidth of the AD844 is about 22MHz, and is essentially independent of V_X. The gain at V_X = 3.16V is +4dB.

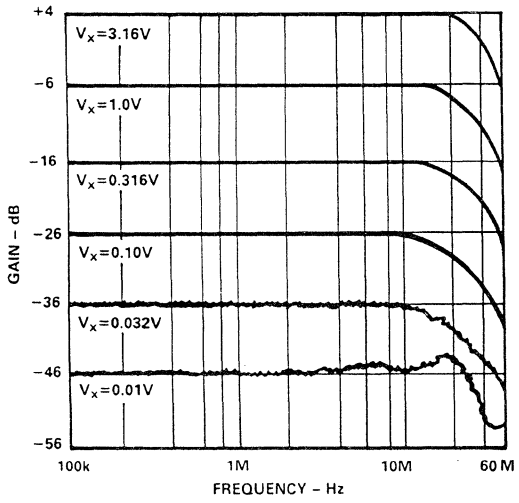
Figure 4.63 shows the small signal response for a 50dB gain control range (V_X = +10mV to +3.16V). At small values for V_X, capacitive feedthrough on the PC board becomes troublesome, and very careful layout techniques are needed to minimize this problem. A ground strip between the pins of the AD539 will be helpful in this regard. Figure 4.58 shows the response to a 2V pulse on V_Y for V_X = +1V, +2V and +3V. For these results, a load resistor of 500Ω was used and the supplies were ±9V. The multiplier will operate from supplies between ±4.5V and ±16.5V.

Disconnecting Pins 9 and 16 on the AD539 alters the denominator in the above expression to 1V, and the bandwidth will be approximately 10MHz, with a maximum gain of 10dB. Using only Pin 9 or Pin 16 results in a denominator of 0.5V, a bandwidth of 5MHz and a maximum gain of 16dB.

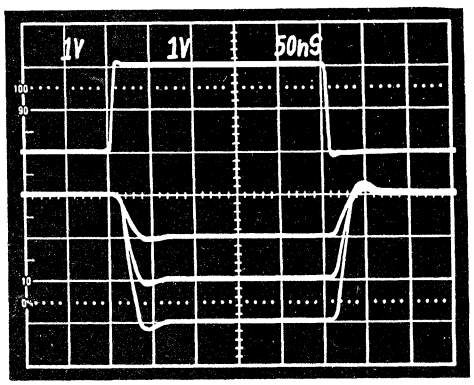


20MHz VARIABLE GAIN AMPLIFIER USING THE AD539

Figure 4.62



VGA ac Response



VGA Transient Response with V_X = 1V, 2V, and 3V

VGA AC AND TRANSIENT RESPONSE

Figure 4.63

High Speed Instrumentation Amplifier

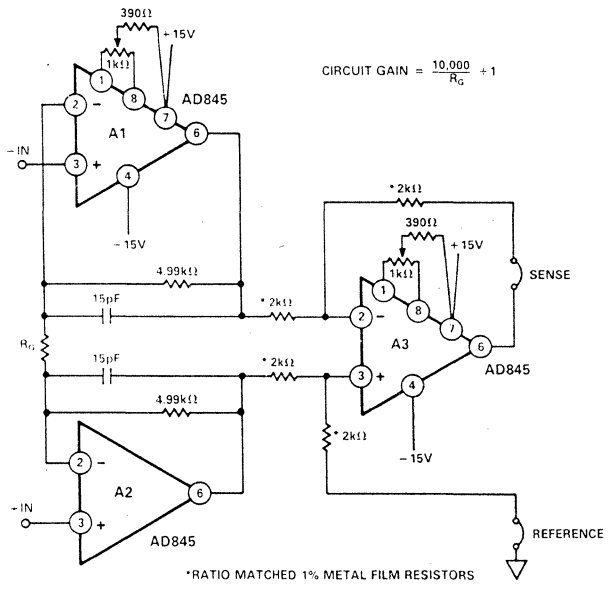
Instrumentation amplifiers are used when high input impedance balanced differential inputs are required. Instrumentation amplifiers offer performance advantages over standard op amps by offering wider common mode input ranges, high common mode rejection ratios, and stable, fixed gains.

In Figure 4.64, three AD845 FET input op amps are used to achieve these characteristics and gain ranges from unity to 1000. Low input bias currents and fast settling times are achieved with the AD845. The AD843 FET input op amp may also be used for improved performance due to its higher bandwidth, faster settling time, and higher slew rate.

Most monolithic instrumentation amplifiers do not have the high-frequency performance of the circuit in Figure 4.64. The circuit bandwidth is 4.9MHz at a gain of 1 and 1.1MHz at a gain of 10; settling time for the entire circuit is 800ns to 0.01% for a 10V step (Gain = 10).

The capacitors employed in this circuit greatly improve the amplifier's settling time and phase margin.

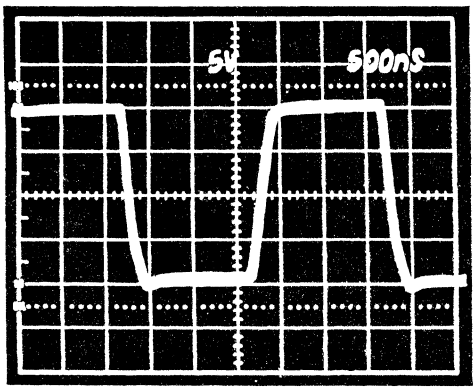
Pulse response and settling time of the three AD845 instrumentation amplifier are shown in Figure 4.65.



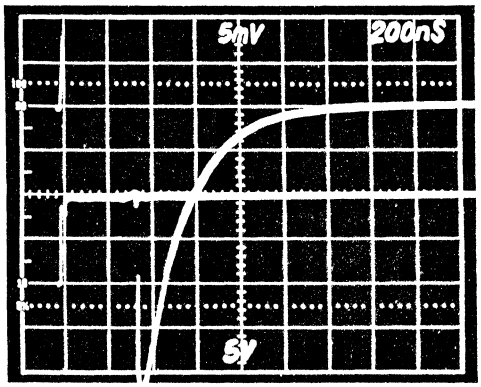
Gain	R_G	Bandwidth	Settling Time to 0.01%
1	NC	4.9MHz	700ns
2	10kΩ	4.2MHz	720ns
10	1.11kΩ	1.1MHz	800ns
100	101Ω	130kHz	3.5μs

HIGH PERFORMANCE, HIGH-SPEED INSTRUMENTATION AMPLIFIER

Figure 4.64



The Pulse Response of the Three Op Amp Instrumentation Amplifier: Gain = 1, Horizontal Scale:0.5μ s/Div, Vertical Scale: 5V/Div



Settling Time of the Three Op Amp Instrumentation Amplifier: Horizontal Scale: 200ns/Div,Vertical Scale, Pulse Input: 5V/Div; Output Settling:1mV/Div

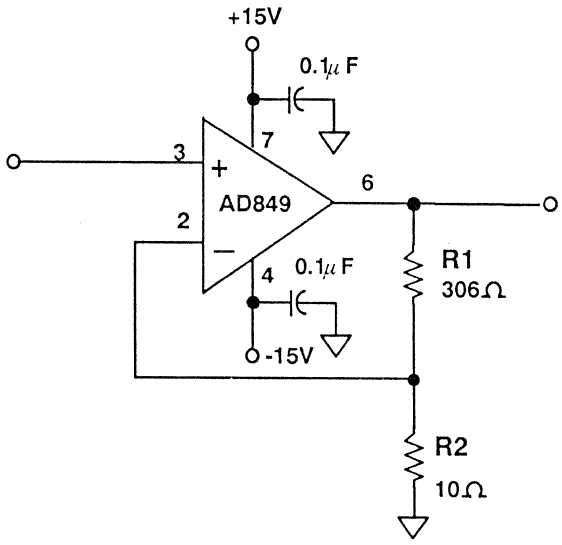
HIGH SPEED INSTRUMENTATION AMP PULSE RESPONSE AND SETTLING TIME

Figure 4.65

Low Noise Preamp Using the AD849

The circuit shown in Figure 4.66 has a gain of 30dB and uses the AD849 op amp which is stable for gains greater than 25 and has a 725MHz gain-bandwidth product. The low input noise voltage of the AD849 (3nV/$\sqrt{\text{Hz}}$ at 10kHz) and high gain bandwidth makes it well suited as a preamp in a high frequency system.

It should be noted that the current noise of the AD849 is approximately 1pA/$\sqrt{\text{Hz}}$. This implies that with source resistances of less than 550Ω , the voltage noise will dominate. For source resistances greater than 500Ω , the Johnson noise in the source resistance is dominant until 15.5kΩ source resistance, after which the current noise flowing in the source resistance wins. It is obvious, however, that with impedances as high as this, the main problem will be reduced bandwidth due to shunt capacitance.



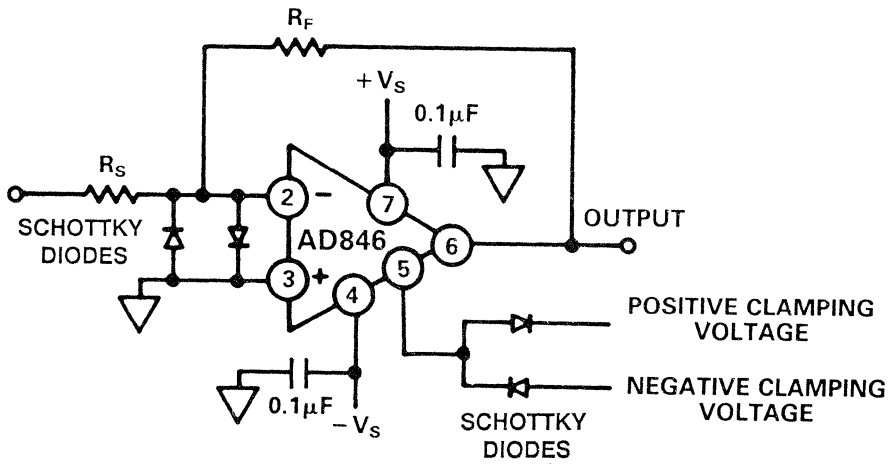
$$G_{dB} = 20\log\left[1 + \frac{R1}{R2}\right]$$

LOW NOISE PREAMP

Figure 4.66

Clamped Amplifier

The AD844 and AD846 precision current feedback op amps are well suited to act as clamped amplifiers able to protect delicate circuitry following the amplifier. Figure 4.67 shows the AD846 set up in the clamped amp configuration. By connecting schottky diodes to the compensation pin, the output is restricted to the range dictated by the diodes. The input of the amp should be clamped as well to avoid damaging the input transistors. This circuit exhibits excellent overvoltage recovery times.

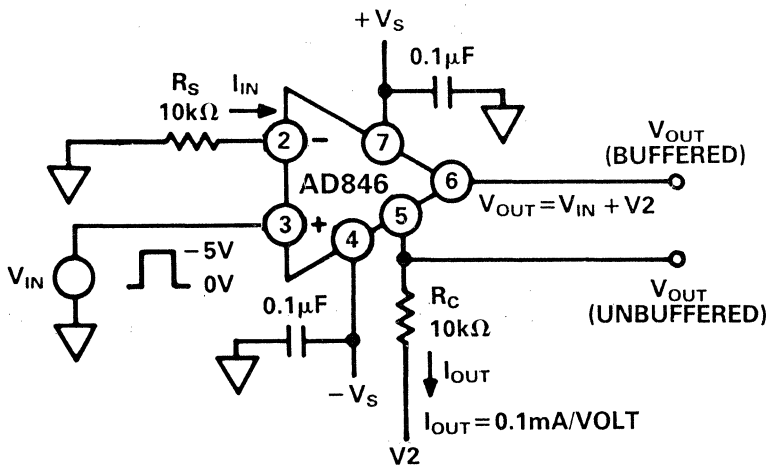


AD846 USED AS A CLAMPED AMPLIFIER

Figure 4.67

Level Shifting

Many applications require signals to be DC shifted. An extremely easy and straight forward means to accomplish this task is shown in Figure 4.68. The AD846 (or AD844) is set up with the input voltage signal connected to the non-inverting input. That voltage is mirrored to the inverting input by placing a resistor R_S in series to ground. The current developed is proportional to V_{IN}. This current flows from the compensation node (Pin 5) developing a voltage across resistor R_C (note $R_C = R_S$) which is connected to the level shifting voltage V2. The voltage developed at the compensation node is, therefore, V_{IN} + V2, and directly follows changes in V_{IN}. By scaling R_C, a level shift with voltage gain is produced. The normal output voltage developed at Pin 6 is nearly equal to the voltage seen at the compensation pin, and can provide a low output impedance, buffered, level shifted output.



AD846 CONNECTED AS A LEVEL SHIFT AMPLIFIER

Figure 4.68

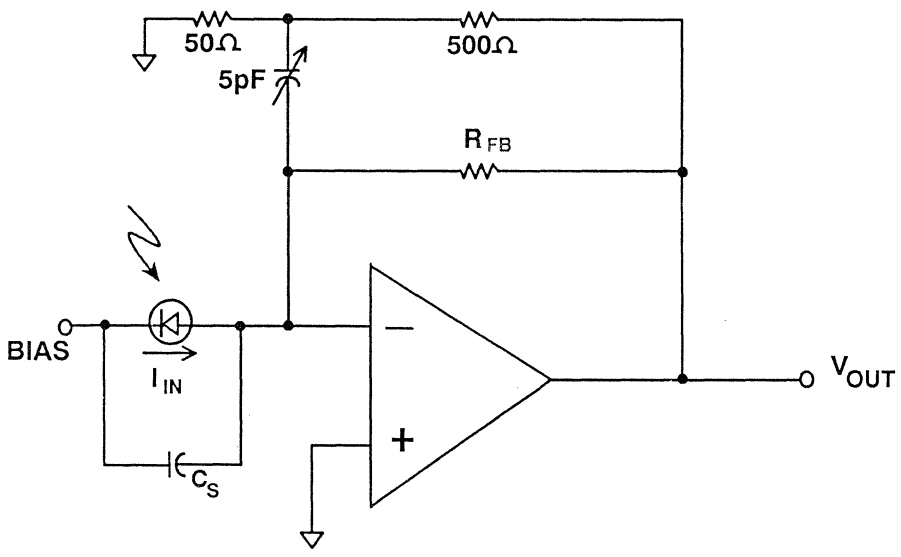
Photodiode Detectors

Current feedback amplifiers can be used to amplify the current from a wideband fiberoptic photodiode receiver as shown in Figure 4.69. The compensation circuit is required to prevent peaking and instability caused by the diode capacitance.

In photodiode applications, the effective input current noise should be calculated for the circuit conditions to verify that the diode current is not swamped out by the op amp noise.

The current noise of bipolar input voltage feedback op amps of the AD840-series (AD840, 841, 842, 847, 848, 849) is basically the schottky (shot) noise in the input junction. This is given by the formula:

$I_{IN} = 5.7 \times 10^{-10} \sqrt{BI_J}$, where
I_{IN} = rms noise current (AMPS)
I_J = junction bias current (AMPS)
B = bandwidth (Hz)



PHOTODIODE DETECTOR

Figure 4.69

Active Filters: A Wideband Sallen Key Filter

Figure 4.70 shows an AD843 FET input op amp used in a 1MHz Sallen-Key filter. This circuit also works well with the AD841, AD845 or the AD847. The circuit is designed to be a maximum-flatness Butterworth filter with a Q of 0.575, and a DC gain of 1.26. The frequency response of the filter of a 0dBm input signal is shown in Figure 4.71. (Measured with an HP8753A Network Analyzer).
In this design if R1 = R2, and C1 = C2, the circuits sensitivity to variations in component values is minimized. The cutoff frequency f_c is given by

$$f_c = \frac{1}{2\pi\sqrt{R1 \cdot R2 \cdot C1 \cdot C2}} = \frac{1}{2\pi R1 \cdot C1}$$

and the circuit Q is given by

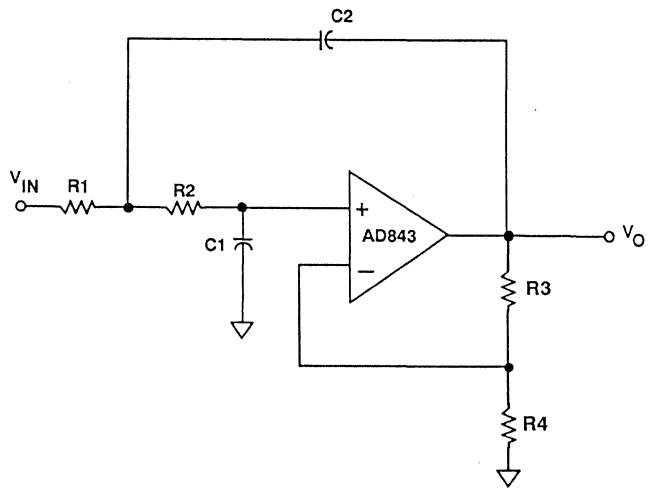
$$Q = \frac{1}{3 - K},$$

where $K = 1 + \frac{R3}{R4}$.

The complete transfer function is given by

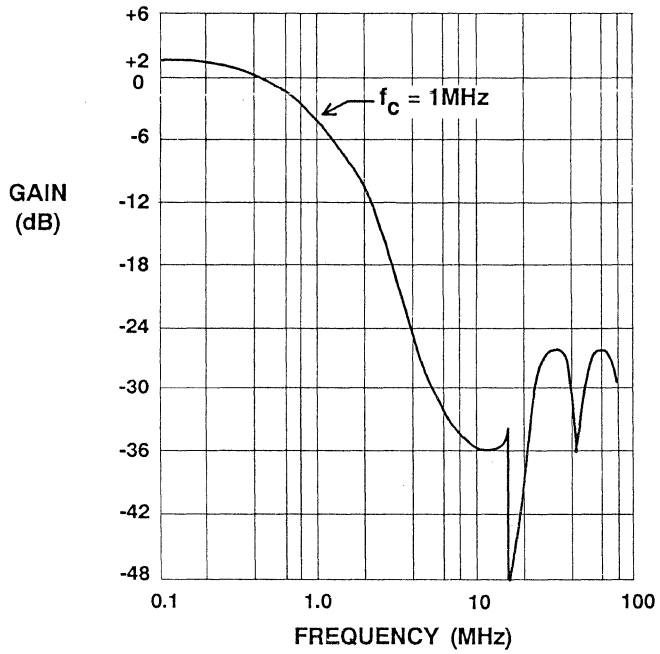
$$\frac{V_O}{V_{IN}} = \frac{K/R^2C^2}{s^2 + \left(\frac{3 - K}{RC}\right)s + \frac{1}{R^2C^2}}$$

where R = R1 = R2 and C = C1 = C2.



1 MHz SALLEN KEY FILTER

Figure 4.70



ACTIVE FILTER SMALL SIGNAL FREQUENCY RESPONSE

Figure 4.71

OP AMP SELECTION GUIDE

VOLTAGE FEEDBACK OP AMPS

MODEL	GBW (MHz)	MINIMUM STABLE GAIN	SLEW RATE (V/μs)	SETTLING TIME (ns)	POWER SUPPLY (V)	COMMENTS
AD5539	1400	+5, -4	600	12(1%)	±8	____
AD840	400	10	400	100(.01%)	±15	____
AD841	40	1	300	110(.01%)	±15	±50mA Output
AD842	80	+2, -1	375	100(.01%)	±15	±100mA Output
AD843	35	1	250	110(.01%)	±15	FET Input
AD845	16	1	100	350(.01%)	±15	FET Input
AD847	50	1	300	120(.1%)	±15, ±5	Stable With Capacitive Load
AD848	175	5	300	100(.1%)	±15, ±5	Stable With Capacitive Load
AD849	725	25	300	80(.1%)	±15, ±5	Low Noise Pre-amp
AD711	3	1	16	1000(.01%)	±15	FET Input
AD712	3	1	16	1000(.01%)	±15	Dual AD711
AD713	3	1	16	1000(.01%)	±15	Quad AD711
AD744	13	+2, -1	75	500(.01%)	±15	FET Input
AD746	13	+2, -1	75	500(.01%)	±15	Dual AD744
AD827	50	1	300	120(.1%)	±15	Dual AD847
AD829	800	1 → 25	10→300	120(.1%)	±15	Externally Compensated AD849

Figure 4.72

OP AMP SELECTION GUIDE

CURRENT FEEDBACK OP AMPS

MODEL	BW* (MHz)	MINIMUM STABLE GAIN	SLEW RATE (V/μs)	SETTLING TIME (ns)	POWER SUPPLY (V)	COMMENTS
AD844	67	1	2000	90(.1%)	±15, ±5	High Slew-Rate
AD846	46	1	450	100(.01%)	±15	Precision
** AD9610	100	1	3500	18(.1%)	±15	Large Output Swing
** AD9611	300	1	1900	13(.1%)	±5	Ultra-Fast
** AD9615	250	1	1400	13(.1%)	±5	Precision
AD9617	185	+1	1600	16(.02%)	±5	Low Distortion
AD9618	160	+5, -1	1500	16(.02%)	±5	Low Distortion

* Bandwidth stated for minimum stable gain with recommended feedback resistor

**Hybrid Op Amps

Figure 4.73

INTERMODULATION DISTORTION IN THE AD9610 and AD9611

by Tom Gratzek & Robert Kim – Analog Devices: Computer Labs Division

January 1988

Operational amplifiers and their applications have been extensively described in sources ranging from elementary textbooks to data sheets to dedicated in-depth specialty monographs (often available from established "off-the- shelf" merchant suppliers.) As vendors attempt to improve on "the state of the art", two general areas are often targeted: ac and dc performance. DC performance often includes enhancing parameters such as offset voltage, bias currents, and open loop gain. AC performance includes wider bandwidth, faster settling time, lower noise (over frequency), and less distortion (harmonic and intermodulation). The user must decide which amplifier is "best" for each application. In most cases, the "best" amplifier is the one that wins the design-in struggle.

Manufacturers have tried to improve both ac and dc specifications with novel designs and by utilizing better transistors. Another trend that has benefitted amplifier users is enhanced testing. For example, the industry-standard 741 is typically available from manufacturers with dc testing only. Parameters tested include open loop gain, output voltage swing, input offset voltage and bias current, PSRR, and supply currents.
As competition intensified and market segments increased, additional tests have been added over the years. Some of the parameters that are now tested by various manufacturers include - dc testing over temperature, rise/fall times, slew rates, -3dB bandwidth at a given gain, and harmonic distortion. Competition has moved amplifier suppliers to test their parts more thoroughly in search of an advantage in the market place.

This article centers on new ultra high-speed operational amplifiers available from Analog Devices, notably the AD9610 and AD9611. While dc specifications are important and are fully tested, the targeted market segments for these parts clearly called for superior ac performance guaranteed by the manufacturer. Enhanced testing for these parts includes detecting the -3dB bandwidth, amplitude of peaking over frequency, and distortion measurements. For the AD9610, total harmonic distortion (with a 20 MHz fundamental) is measured. The testing of the AD9611 goes even further; both second and third harmonic tones are measured separately (with a *60 MHz* fundamental).

One of the applications for which the AD9610 and AD9611 are particularly suited is driving the newest generation of flash A/D converters (such as the AD9002; 8 bits, 150MHz). Users of these premium converters are interested in obtaining the highest dynamic performance from their *Op-Amp :A/D system.* As an example, an 8-bit converter with perfect linearity will deliver a 49dB signal-to-noise ratio (SNR). This implies that distortion from the amplifier should be better than -55 dB (relative to the signal) at the required frequency to avoid affecting the system SNR.

When flash A/D users talk about distortion, they are generally concerned with the spurs introduced into the spectrum of interest. In laboratory conditions (as simulated by most production test beds), harmonic distortion is a major area of concern and is usually measured by inserting a single-tone fundamental into the device under test (DUT), then looking at the relevant frequency (2x fundamental for 2nd harmonic; and 3x fundamental for the third harmonic) to determine the magnitude of the harmonic tones.

While this testing is useful to many customers, it does not always appease everyone. Manufacturers who claim to have amplifiers with -3dB bandwidths in the tens of MHz region often test distortion with only a 10kHz input tone. The results of this testing are undoubtedly favorable (to the manufacturer) but somewhat unsatisfying to the informed customer, who usually wants to know the level of performance that can be expected at higher operational frequencies, and the magnitude of the spurs from other sources (notably intermod distortion).

After the amplifier leaves the factory and is installed in the equipment for which it was selected, there is no guarantee that it will be exposed to such a pure spectrum (implicit to harmonic distortion testing). In many cases the amplifier is asked to operate in *spectrally-rich environments* where the intermodulation distortion properties of the amplifier are of keen interest.

Examples of applications demanding good intermodulation distortion performance include: **Radar**, where interference from other radars and jammers often pollute the RF spectrum; **Satellite Communications,** where the usable bandwidth for each transponder is limited and multiple signals are frequency multiplexed onto one carrier; **Digital Radio Receivers,** where a segment of the RF spectrum is digitized and scanned by high-speed data signal processors (DSPs), often in classified national security (snooping) applications.

The **intermodulation distortion (IMD)** performance of wideband, dc-coupled amplifiers is a relatively new area for operational amplifier suppliers. Methods to measure and communicate the extent of this distortion to users have been borrowed from traditional "RF" companies which have historically supplied the radar and radio communications industries where the importance of it was first highlighted.

In the remaining sections of this article, which will be published in RF Design magazine in April, the authors describe IMD, its mathematical derivation, how to test for it, and present results for two ADI amplifiers (AD9610 and AD9611).

Mathematical Derivation of Intermodulation Distortion

Harmonic distortion is caused by nonlinearities in the amplitude transfer characteristics. The typical output contains not only the fundamental frequency, but integer multiples of it. IMD results from mixing of two or more signals of different frequencies. The spurious output occurs at the sum and/or difference of integer multiples of the input frequencies. The non-ideal characteristics of an amplifier can be described using the Power Series Expansion:

$$V_{out} = K0 + K1(Vin) + K2\,(Vin)^2 + K3(Vin)^3 + \ldots\ldots\ldots \qquad \textbf{(Eqn. 1)}$$

A one-tone input signal (V_{in} = Esinwt) produces harmonic distortion. A two-tone input signal produces harmonic distortion **and** intermodulation distortion.

$$V_{in} = E1\sin w_1 t + E2\sin w_2 t \qquad \textbf{(Eqn. 2)}$$

Combining Equations 1 and 2 results in the following identity:

$$V_{out} = K0 + K1(\,E1\sin w_1 t + E2\sin w_2 t\,) +$$

$$K2\,(\,E1\sin w_1 t + E2\sin w_2 t\,)^2 +$$

$$K3(\,E1\sin w_1 t + E2\sin w_2 t\,)^3 + \ldots\ldots \qquad \textbf{(Eqn. 3)}$$

The first term (K0) represents the dc offset of the amplifier; the second term is the fundamental signal(s). The subsequent terms represent the distortion of the amplifier. The second IMD can be found by analyzing the third term of Eqn. 3.

$$K2\,(Vin)^2 = K2\,(\,E1^2\sin^2 w_1 t + E2^2\sin^2 w_2 t + 2E1E2\sin w_1 t(\sin w_2 t))$$

(Eqn. 4)

Remembering that [$\sin^2 x = (1 - \cos 2x)/2$]

and[$\sin(x)\sin(y)=(\cos(x-y)-\cos(x+y))/2$] and substituting into Eqn 4 provides:

$$K_2 (V_{in})^2 = K_2 (E_1^2 + E_2^2)/2 - \quad (1)$$

$$(K_2/2) (E_1^2 \cos 2w_1 t + E_2^2 \cos 2w_2 t) + \quad (2)$$

$$2 K_2 E_1 E_2 (\cos(w_1 t - w_2 t) - \cos(w_1 t + w_2 t)) \quad (3)$$

(Eqn. 5)

The first and second terms in Equation 5 represent dc offset and second-order harmonics. The third term is the second-order IMD. This excercise can be repeated with the fourth term of Equation 3 to study third-order effects.

$$K_3 (V_{in})^3 = K_3(E_1^3 \sin^3 w_1 t + E_2^3 \sin^3 w_2 t + 3E_1^2 E_2 \sin^2 w_1 t (\sin w_2 t) + 3E_1 E_2^2 \sin w_1 t (\sin^2 w_2 t))$$

(Eqn. 6)

Utilizing the identities, $\sin^3 x = 1/4(3\sin x - \sin 3x)$ and
$\sin^2 x \sin y = 1/2(\sin y - 1/2(\sin(2x+y) - \sin(2x-y)))$, Equation 6 reduces to:

$$K_3 (V_{in})^3 = (3K_3/4)(E_1^3 \sin w_1 t + E_2^3 \sin w_2 t + 2E_1^2 E_2 \sin w_2 t + 2E_2^2 E_1 \sin w_1 t)$$

(1)

$$(K_3 E_2^3/4)(E_1^3 \sin 3w_1 t + E_2^3 \sin 3w_2 t) +$$

(2)

$$(3K_3 E_1^2 E_2/2)(\sin(2w_1 t - w_2 t) - 1/2\sin(2w_1 t + w_2 t)) +$$

(3)

$$(3K_3 E_2^2 E_1/2)(\sin(2w_2 t - w_1 t) - 1/2(\sin(2w_2 t + w_1 t))$$

(4)

(Eqn. 7)

Term 1 from Equation 7 represents amplitude offset at the fundamental frequencies. Term 2 signifies the third-order harmonics. Terms 3 and 4 represent third-order IMD.

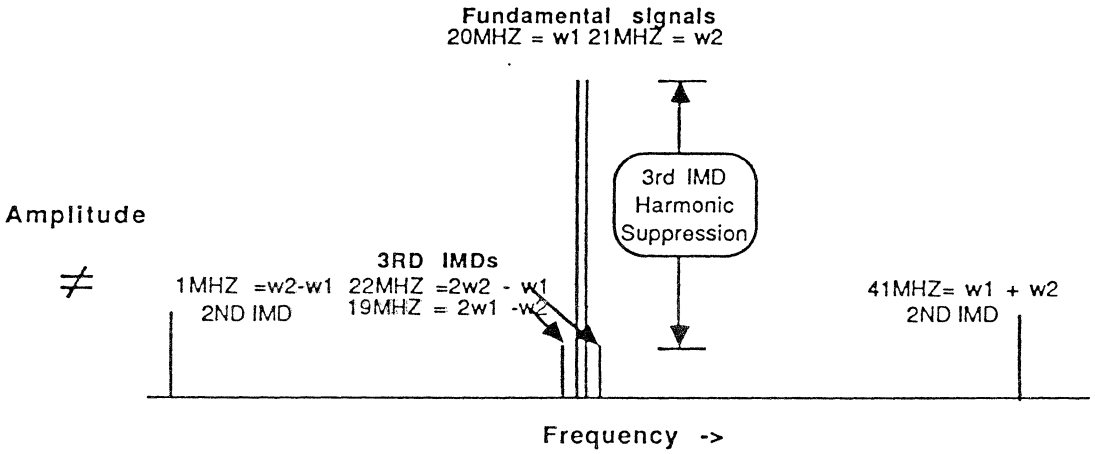
Some Simple Relationships

Intermodulation distortion occurs at frequencies that are the sum and/or difference of integer multiples of the fundamental frequencies. For example, assume a composite input signal has fundamental frequencies w1 and w2. Distortion products will occur at frequencies aw1±bw2 where a and b = 0,1,2,3... Intermodulation Distortion terms of order a+b occur when either a or b is not equal to zero. The following table illustrates this relationship.

2nd Order IMD Frequencies	3rd Order IMD Frequencies	
w1-w2	2w1+w2	2w2+w1
w1+w2	2w1-w2	2w2-w1

Most IMD can be filtered out. However, if the two input tones are of similar frequencies, the third-order IMD (2w1-w2, 2w2-w1) will be very close to the fundamental frequencies and cannot be easily filtered. Third-order IMD is of most concern in narrow bandwidth applications. Second-order IMD is of greater concern in broad bandwidth applications. Figure 1 below illustrates the 2nd and 3rd IMDs for the condition in which the fundamental tones (w1 & w2) are 20 and 21MHz sinewaves.

Figure 1: Relationship Between Fundamentals and IMDs



AMPLITUDE OF IMD vs. the FUNDAMENTAL

The location of the IMDs relative to the fundamental tones has now been defined. The relationship of the amplitudes of the IMD tones to the amplitude of the fundamental tones depends on the order of the IMD. The coefficients of the third-order IMD term in Equation 7 can be used as a starting point in the analysis.

$$\textit{Amplitude of 3rd IMD tones} = 3K3E1^2 E2/2.$$

Converting to dB provides:

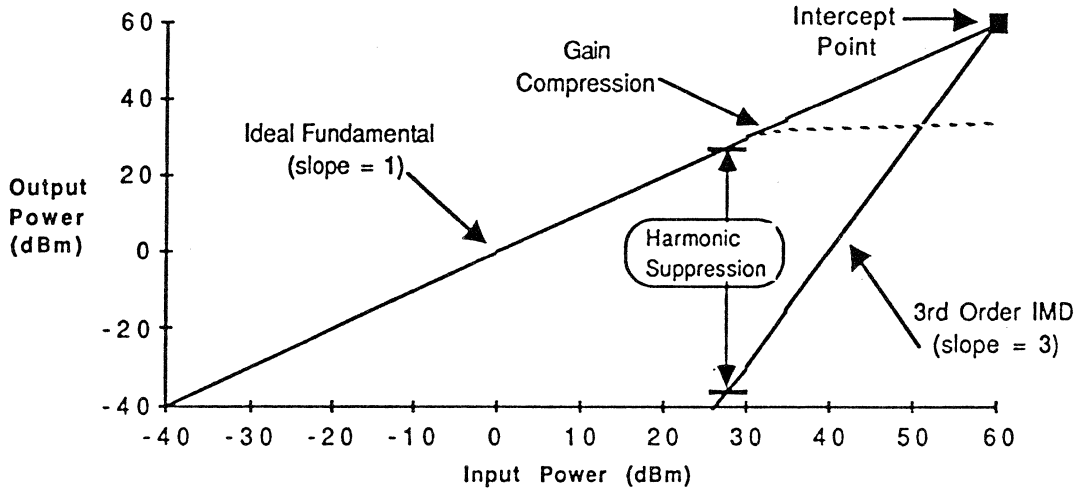
$$\textit{Amplitude of 3rd IMD tone} = 20\log(3K3/2) + 20\log(E1^{2)} + 20\log(E2).$$

$$\textit{Amplitude of 3rd IMD tone}\ (\text{dB}) = \text{Constant} + 2E1 + E2 \qquad \textbf{(Eqn. 8)}$$

where E1 & E2 are expressed in dB.

Equation 8 shows that if the two inputs are changed by 1dB, the third-order IMD amplitude will change by 3dB. The desired output of the amplifier and any IMD can be represented by two straight lines of different slopes. The desired output line has a slope of 1; any IMD has a slope of n, where n is the order of the IMD. The third-order IMD has a slope of 3. (See Figure 2.)

Figure 2: Relationship Between Fundamental and 3rd IMD



Ideally, the output of an amplifier will track the input. *Gain Compression* occurs at the point where the actual output power drops below the ideal. The *Intercept Point* is at the intersection of the ideal output signal and the extension of the IMD. The intercept point can be determined from the value of the harmonic suppression which must be determined experimentally. Equation 9 illustrates this relationship.

Intercept Point = (Harmonic Suppression)/(N-1) + (Power of One Fundamental at Output of Amplifier)

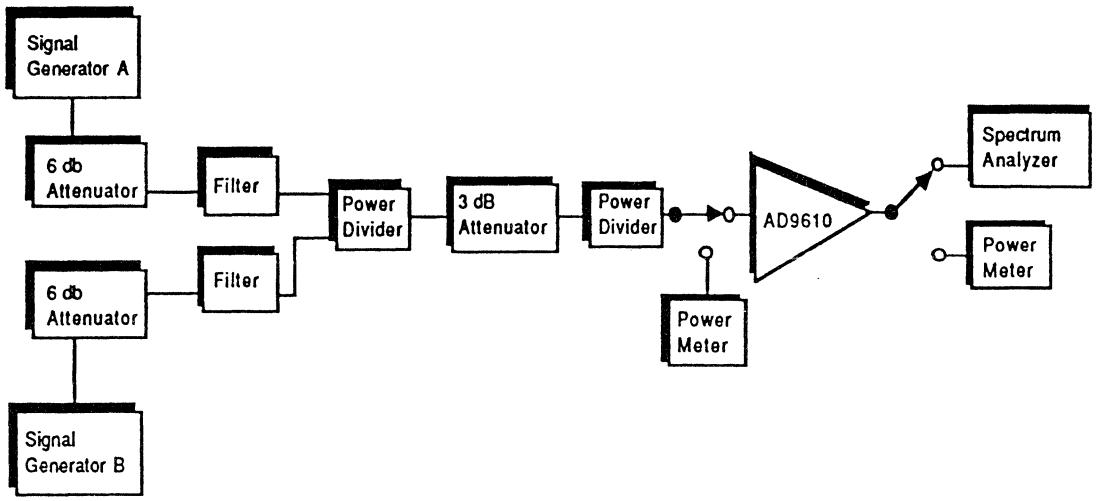
(Eqn. 9)

Harmonic suppression must be measured where the amplifier exhibits a linear output/input (i.e., below the gain compression point.) "N" is the order of the IMD of interest.

Determining Harmonic Suppression

The test system used to measure harmonic suppression for the AD9610 wide-bandwidth transimpedance amplifier is diagrammed below.

Figure 3: Test Setup to Measure Harmonic Suppression



(Attenuators are used to limit the IMD of the signal generator setup; for every 1 dB attenuation of the fundamental signals, the nth order IMD is reduced by n dB.)

4

Test Procedure to Determine Harmonic Suppression

1) Set the amplitude of the two inputs equal with the power meter.

2) Check for gain compression by reducing the signal power of both fundamentals by 1dB, then checking to make sure that the 3rd IMD tone is reduced by 3dB. If past the compression point (see Figure 2), then the amplitude of the input to the amplifier should be reduced (REPEAT STEP 1).

3) Measure the harmonic suppression of the 3rd IMD tone on the spectrum analyzer. This is the difference between the magnitude of the fundamental and the 3rd IMD. (See Figure 1.)

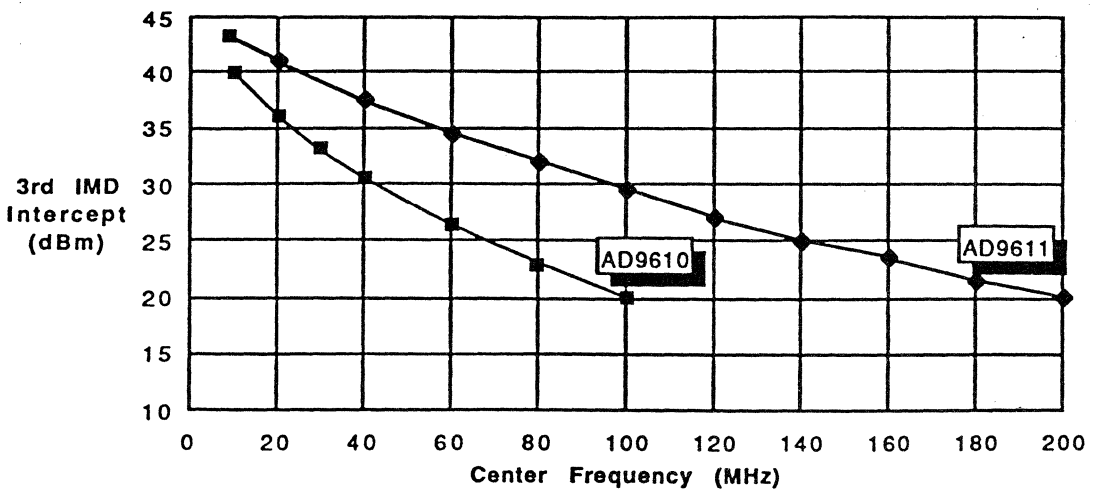
4) Measure the amplitude of a fundamental signal at the output of the AD9610 by disconnecting one of the signal generators.

5) Calculate the intercept point using Equation 9.

THIRD-ORDER IMD RESULTS FOR THE AD9610 and AD9611

The 3rd IMD intercept points were measured for the AD9610 and AD9611 using fundamental input frequencies from 2MHz to 200MHz with 500kHz separation between tones. All parts were set up in a gain of -5 and were driven into a 50Ω load.

Figure 4 is the plot of the 3rd IMD intercept points at different frequencies. The IMD Interept data are valid at different gain settings as long as the measurements are made below the gain compression point. The AD9610 is a very good performer, and becomes better than the AD9611 below 8 MHz. The AD9611 is the best dc-coupled wide band amplifier in the world in terms of IMD.



3rd Order IMD for Two ADI Amplifiers

Figure 4.

References:

Introduction to Radio Frequency Design: W. H. Hayward (Tektronix, Inc., Beaverton< Oregon 97077) 1982; Prentice-Hall, Inc.; Englewood Cliffs, NJ 07632; pp. 219 - 232.

Intercept Point and Undesired Responses; Richard C. Sagers, Motorola, Inc, 5555 North Beach Street, Fort Worth, Texas 76137. Presented before the 32nd IEEE Vehicular Technology Conference, May 23-25, 1982, pp. 1-9.

Chemical Engineers' Handbook, Fifth Edition; edited by Robert H. Perry & Cecil H. Chilton; 1973; McGraw-Hill Book Company; New York, pp. 2-20, 2-21.

SECTION V

HIGH SPEED NON-LINEAR SIGNAL PROCESSORS:

MULTIPLIERS, MODULATORS & LOG AMPS

HIGH SPEED NON-LINEAR SIGNAL PROCESSORS:

MULTIPLIERS, MODULATORS & LOG AMPS

INTRODUCTION

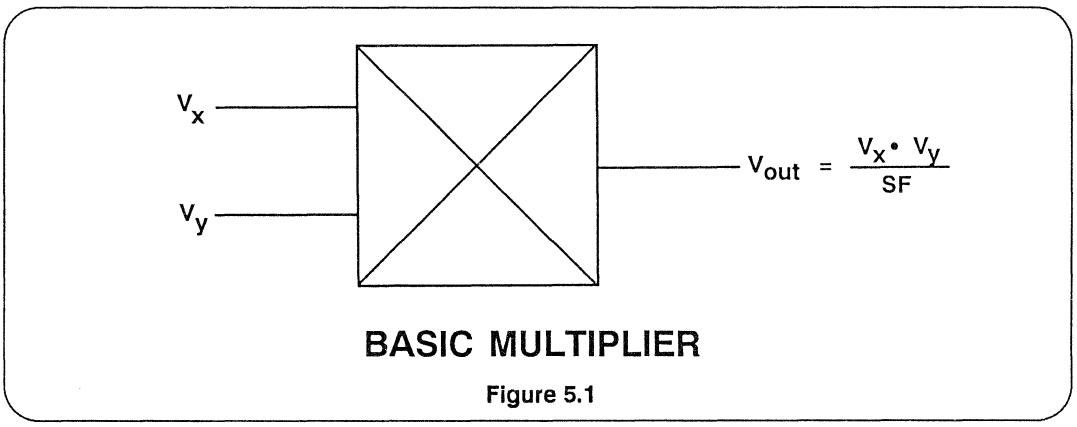
Historically analog computers have been slow devices. Although high frequency multipliers, modulators, logarithmic amplifiers and other function generators have been available for many years they have generally had relatively poor accuracy and stability and have not usually been considered as "analog computers". This section of our seminar considers a few classes of non-linear device which perform accurate analog operations of various sorts at high speeds. These devices are multipliers and modulators, and logarithmic amplifiers.

MULTIPLIERS

A multiplier is a device having two input ports and an output port. The signal at the output is the product of the two input signals. If both input and output signals are voltages, the transfer characteristic is

$$V_{out} = \frac{V_x \bullet V_y}{SF}$$, where

SF is a scaling factor and, in order that the equation be dimensionally correct, has the dimension of voltage. (See Figure 5.1)



BASIC MULTIPLIER

Figure 5.1

From a mathematical point of view multiplication is a "four quadrant" operation - that is to say that both V_x and V_y may be either positive or negative, as may be V_{out}. Some of the circuits used to produce electronic multipliers, however, are limited to signals of one polarity.

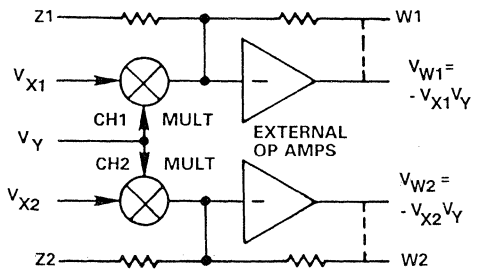
If both signals must be unipolar we have a "single quadrant" multiplier and the output will also be unipolar. If one of the signals is unipolar but the other may have either polarity, then the multiplier is a "two quadrant" multiplier and the output may have either polarity (and is "bipolar").

TYPES OF MULTIPLIERS

TYPE	V_X	V_Y	V_{OUT}
Single quadrant	Unipolar	Unipolar	Unipolar
Two quadrant	Bipolar	Unipolar	Bipolar
Four quadrant	Bipolar	Bipolar	Bipolar

Figure 5. 2

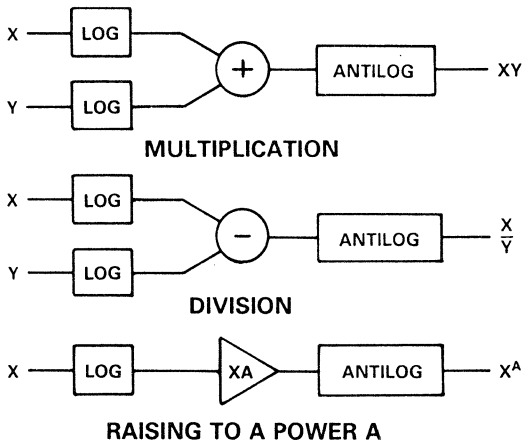
The circuitry used to produce one- and two-quadrant multipliers may be simpler than that required for four quadrant multipliers, and since there are many applications where full four quadrant multiplication is not required, it is by no means uncommon to find accurate devices which work in only one or two quadrants. An example is the AD539, which is a wideband dual two-quadrant multiplier which has a single unipolar V_y input with the relatively limited bandwidth of 5 MHz, and two bipolar V_x inputs, one per multiplier, with bandwidths of 60 MHz. A block diagram of the AD539 is shown in Figure 5.3.



AD539 FUNCTIONAL BLOCK DIAGRAM

Figure 5.3

The simplest electronic multiplier circuits use logarithmic amplifiers. The electronic principles involved will be described later, but the computation relies on the simple fact that the antilog of the sum of the logs of two numbers is the product of those numbers. (See Figure 5.4.)



COMPUTATION WITH LOG AND ANTILOG CIRCUITS

Figure 5.4

The disadvantages of this type of multiplication are a very limited bandwidth and single quadrant operation. A far better type of multiplier uses the "Gilbert Cell". This structure was invented by Barrie Gilbert in the late 1960s.[1, 2]

There is a linear relationship between the collector current of a silicon junction transistor and its transconductance (gain) which is given by

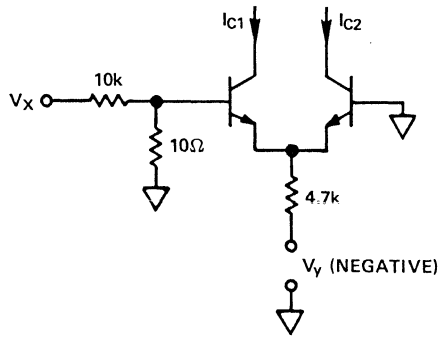
$$\frac{dI_c}{dV_{be}} = \frac{qI_c}{kT}$$

Where

I_c = the collector current
V_{be} = the base-emitter voltage
q = the electron charge (1.60219E-19)
k = Boltzmann's constant (1.38062E-23)
T = the absolute temperature

This relationship may be exploited to construct a multiplier with a long-tailed pair of silicon transistors, as shown in Figure 5.5.

This is rather a poor multiplier because (1) the Y input is offset by the V_{be} - which changes non-linearly with V_y; (2) the X input is non-linear as a result of the exponential relationship between I_c and V_{be}; and (3) the scale factor varies with temperature.



$$I_{C1} - I_{C2} = \Delta I_C = \frac{q}{kT}\left(\frac{V_Y + V_{be}}{4.7 \times 10^3}\right)\left(\frac{10}{10{,}010}\right)V_X$$

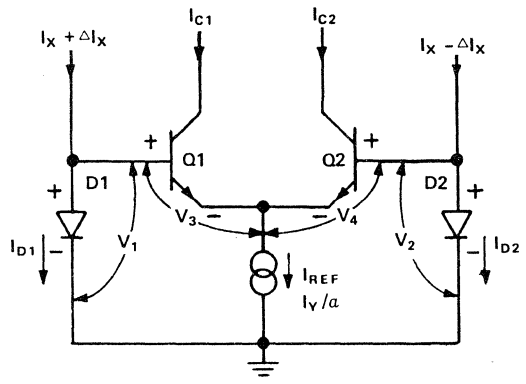
$$= 8.3 \times 10^{-6}\,(V_Y + 0.6)\,V_X \;@\; 25°C$$

BASIC TRANSCONDUCTANCE MULTIPLIER CIRCUIT

Figure 5.5

Gilbert realized that this circuit could be linearized and made temperature stable by working with currents, rather than voltages, and by exploiting the logarithmic I_C/V_{be} properties of transistors. (See Figure 5.6.)

$$\Delta I_C = I_{C1} - I_{C2}$$



$$\Delta I_C = \frac{\Delta I_X I_Y}{I_X}$$

THE GILBERT CELL - A LINEAR TWO-QUADRANT MULTIPLIER

Figure 5.6

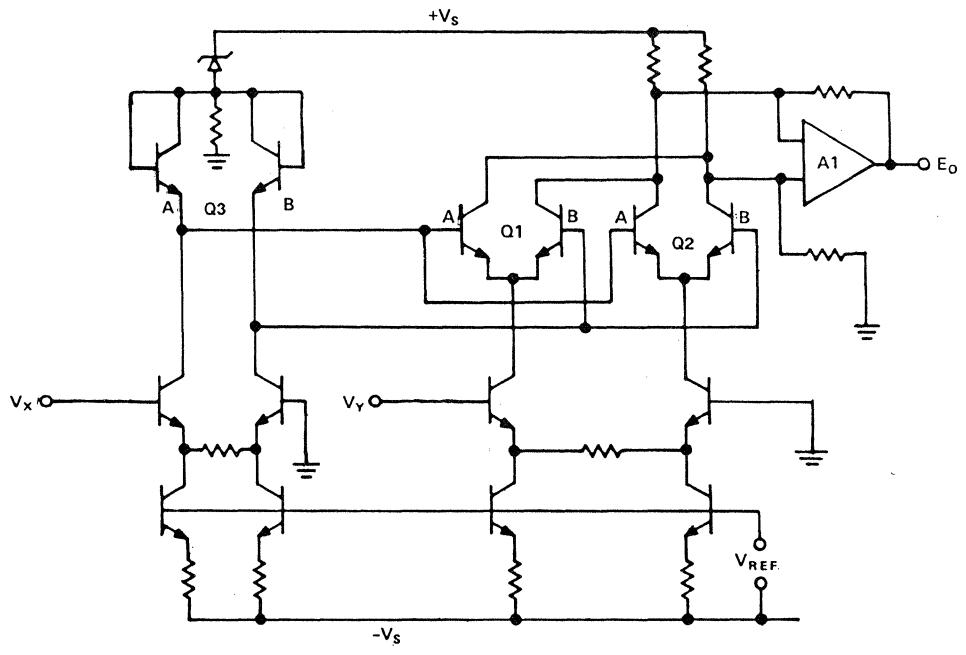
The X input to the Gilbert Cell takes the form of a differential current, and the Y input is a unipolar current. The differential X currents flow in two diode connected transistors and the logarithmic voltages compensate for the exponential V_{be}/I_c relationship. Furthermore the q/kT scale factors cancel. This gives the Gilbert Cell the linear transfer function

$$\Delta I_c = \frac{\Delta I_x \cdot I_y}{I_x}$$

As it stands the Gilbert Cell has three inconvenient features:

(1) Its X input is a differential current;
(2) Its output is a differential current; and
(3) Its Y input is a unipolar current - so the cell is only a two quadrant multiplier.

By cross-coupling two such cells and using two voltage-to-current converters (as shown in Figure 5.7) , we can convert the basic architecture to a four quadrant device with voltage inputs. At low and medium frequencies a subtractor amplifier may be used to convert the differential current at the output to a voltage - but this may not be the best way of handling signals at high frequencies.



4-QUADRANT TRANSLINEAR MULTIPLIER

Figure 5.7

In Figure 5. 7, Q1A & Q1B, and Q2A & Q2B form the two core long-tailed pairs of the two Gilbert Cells, while Q3A and Q3B are the linearizing transistors for both cells. In Figure 5.7 there is an operational amplifier acting as a differential current to single-ended voltage converter, but for higher speed applications the cross-coupled collectors of Q1 and Q2 might form a differential open collector current output.

This multiplier relies on the matching of a number of transistors and currents. This is easily accomplished on a monolithic chip but is much harder with discrete components - such multipliers are, therefore, almost invariably made as ICs. Even the best integrated circuit processes have some residual errors, however, and these show up as four DC errors in such multipliers.

TRIMMABLE ERRORS IN MULTIPLIERS

X-Input Voltage Offset:	Y Feedthrough
Y-Input Voltage Offset:	X Feedthrough
Z-Input (output amplifier) Voltage Offset:	dc output offset voltage
Resistor Mismatch:	Gain Error

Figure 5.8

In early Gilbert Cell multipliers these errors had to be trimmed by means of resistors and potentiometers external to the chip, which was somewhat inconvenient. With modern analog processes, which permit the laser trimming of SiCr thin film resistors on the chip itself, it is possible to trim these errors during manufacture so that the final device has very high accuracy. Internal trimming has the additional advantage that it does not reduce the high frequency performance, as may be the case with external trimpots.

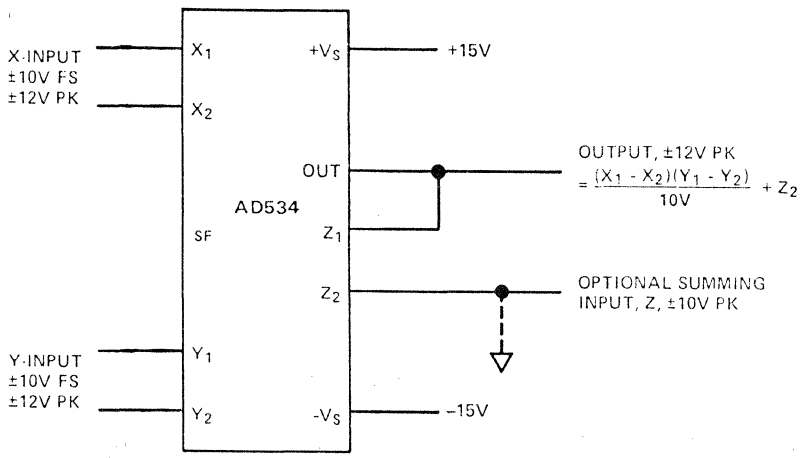
KEY FEATURES OF THE TRANSLINEAR MULTIPLIER

- High Accuracy - better than 0.1% is posssible
- Wide Bandwidth (over 60 MHz voltage output over 500 MHz current output)
- Simplicity, low cost, and ease of use

Figure 5.9

Because the internal structure of the translinear multiplier is necessarily differential, the inputs are usually differential as well (after all, if a single-ended input is required it is not hard to ground one of the inputs). This is not only convenient in allowing common-mode signals to be rejected, it also permits more complex computations to be performed.

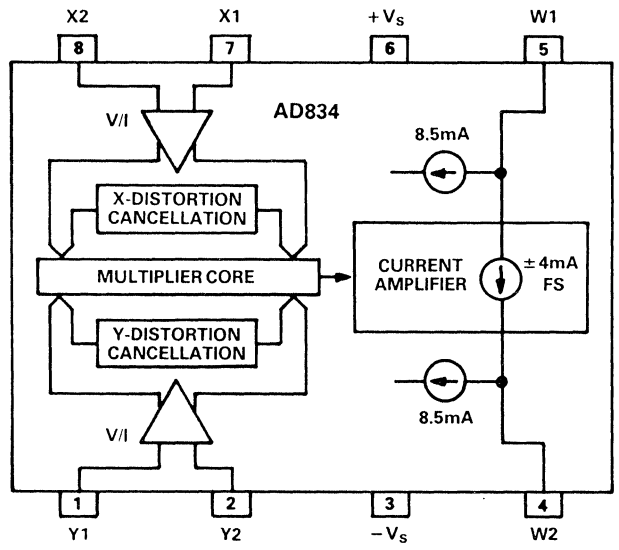
The AD534 (see Figure 5.10) is the classic example of a four-quadrant multiplier based on the Gilbert Cell. It has an accuracy of 0.1% in the multiplier mode, fully differential inputs, and a voltage output. However, as a result of its voltage output architecture, its bandwidth is only about 1MHz.



THE AD534 MULTIPLIER

Figure 5.10

For wideband applications the basic multiplier with open collector current outputs is used. The AD834 is an 8-pin device with differential X inputs, differential Y inputs, differential open collector current outputs, and a bandwidth of over 500 MHz. A block diagram is shown in Figure 5.11.



THE AD834 FUNCTIONAL BLOCK DIAGRAM

Figure 5.11

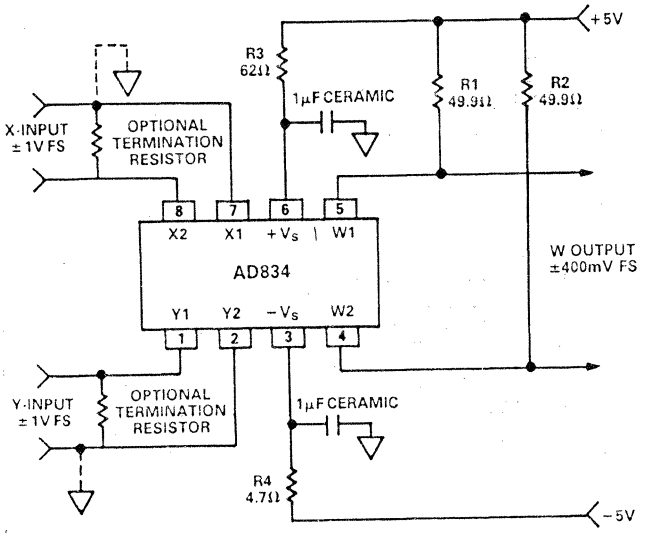
5

The AD834 is a true linear multiplier with a transfer function of

$$I_{out} = \frac{V_x \bullet V_y}{1V \bullet 250\Omega}$$

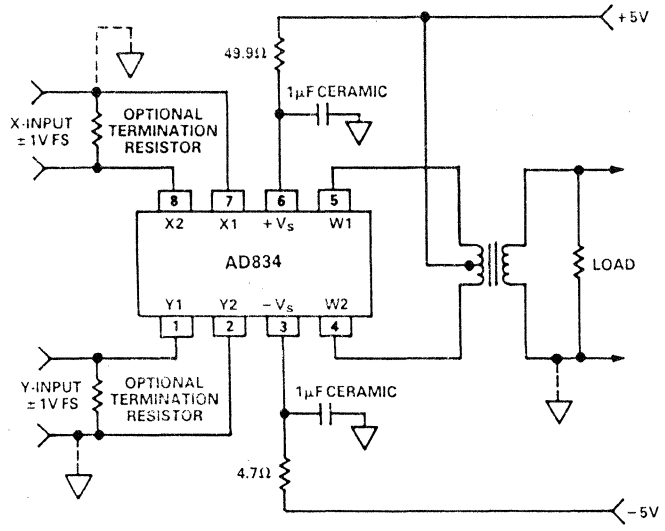
Its X and Y offsets are trimmed to 500 μV (3 mV max), and it may be used in a wide variety of applications including multipliers (broadband and narrowband), squarers, frequency doublers, and high frequency power measurement circuits. A consideration when using the AD834 is that, because of its very wide bandwidth, its input bias currents, approx 50 μA per input, must be considered in the design of input circuitry lest, flowing in source resistances, they give rise to unplanned offset voltages.

A basic wideband multiplier using the AD834 is shown in Figure 5.12. The differential current output flows in equal load resistors R1 and R2 to give a differential voltage output. This is the simplest application circuit for the device. Where only the high frequency outputs are required, transformer coupling may be used, with either simple transformers or, for better wideband performance, transmission line or "Ruthroff"[3] transformers (see Figure 5.13).



BASIC CONNECTIONS FOR WIDEBAND AD834 OPERATION

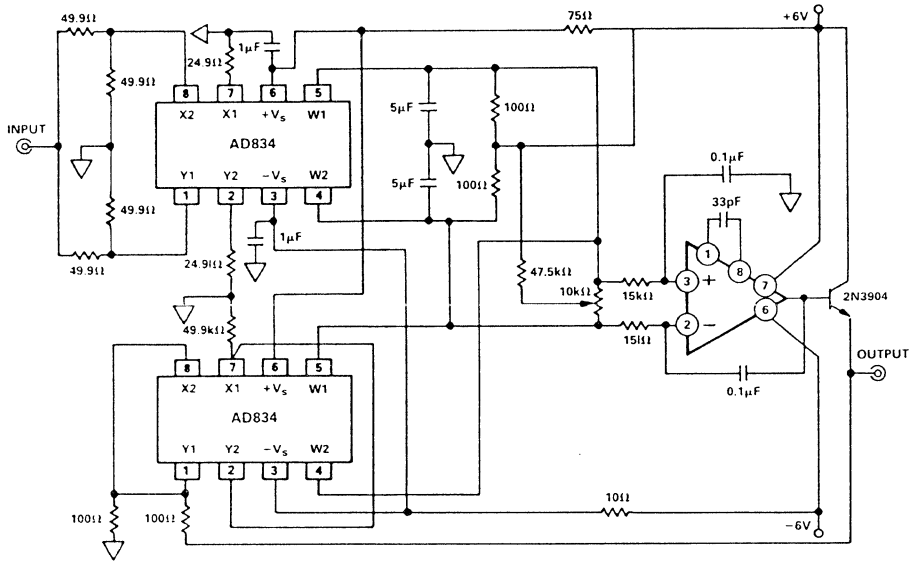
Figure 5.12



AD834 OPERATION WITH WIDEBAND TRANSFORMER COUPLED OUTPUT

Figure 5.13

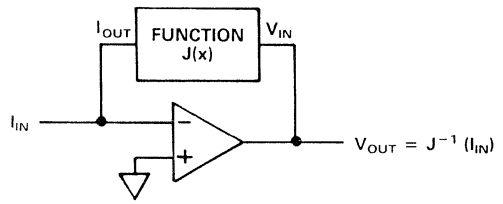
A very wideband (500 MHz) root mean square (rms) circuit is shown in Figure 5.14. This uses two AD834s, one as a wideband squarer, and one as a square rooter.



WIDEBAND R.M.S. MEASUREMENT WITH THE AD834

Figure 5.14

The operation of the circuit is described in detail in the data sheet of the AD834, but in essence the signal is applied to both inputs of the top AD834 whose output is then the square of the instantaneous value of the input. This output is averaged in the two 5 μF capacitors, and the square root of this mean square is computed by the op-amp and the second AD834, using the common principle of analog computing that a function generator in a negative feedback loop computes the inverse function (provided, of course, that the function is monotonic over the range of operation). (See Figure 5.15.)



NOTE: FUNCTION MUST BE MONOTONIC OVER THE RELEVANT RANGE

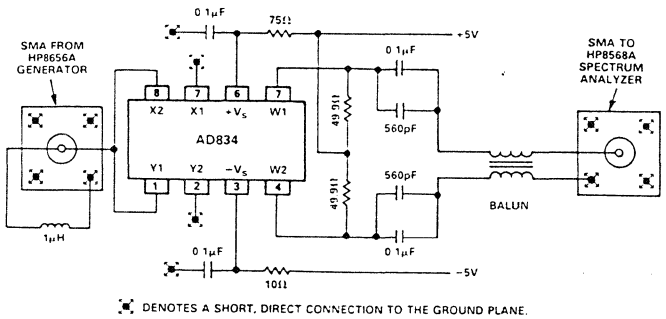
A FUNCTION GENERATOR IN A NEGATIVE-FEEDBACK LOOP GENERATES THE INVERSE FUNCTION

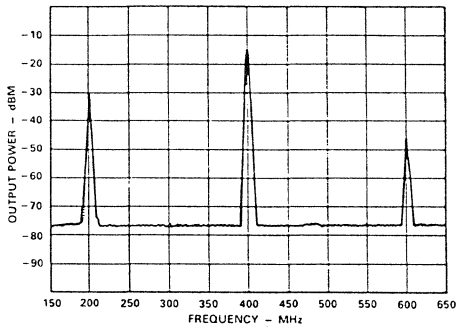
Figure 5.15

If a sinusoidal waveform is applied to a squarer, the output consists of a sinusoidal waveform at twice the frequency, plus a DC level - this necessarily follows from the well-known identity

$$\sin^2\omega t = \frac{(1 - \cos 2\omega t)}{2}$$

This relationship can be used to make a multiplier perform as a frequency doubler as shown in Figure 5.16. If a signal is applied to both ports of an AD834 and the output is AC coupled, the DC component will be lost, and only the component at twice the frequency will appear.



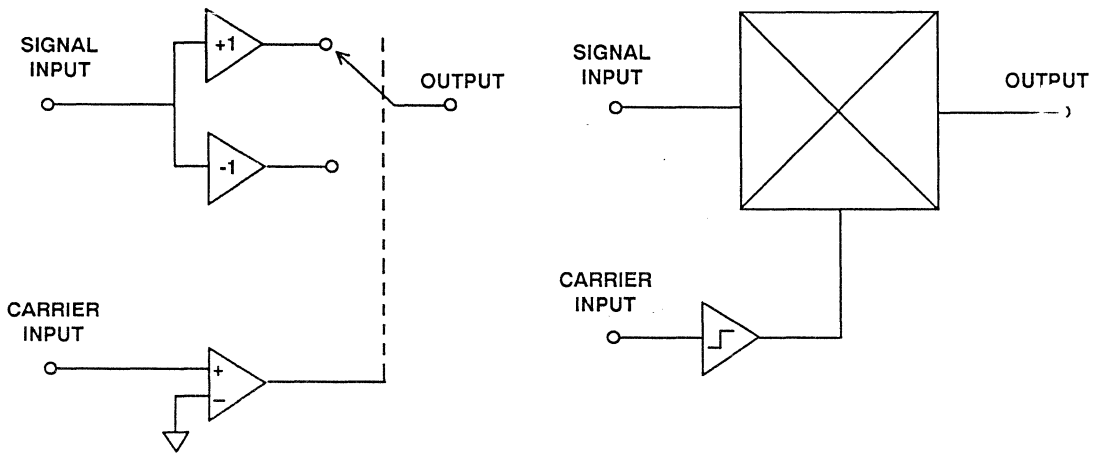


AD834 FREQUENCY DOUBLER

Figure 5.16

MODULATORS

Modulators are closely related to multipliers. The output of a multiplier is the instantaneous product of its inputs - the output of a modulator is the instantaneous product of a signal on one of its inputs (known as the signal input) and the sign of the signal on the other (known as the carrier input).



TWO MODULATOR MODELS

Figure 5.17

A modulator may be modelled as an amplifier whose gain is switched positive and negative by the output of a comparator on its carrier input - or as a multiplier with a high-gain limiting amplifier between the carrier input and one of its ports as shown in Figure 5.17. Both architectures have been used to produce modulators, but the switched amplifier version, although potentially very accurate, tends to be rather slow. Most high speed integrated circuit modulators consist of a Gilbert Cell multiplier with a limiting amplifier in the carrier path.

If two periodic waveforms $A_m \cdot \cos(\omega_m t)$ and $A_c \cdot \cos(\omega_c t)$ are applied to the inputs of a multiplier (with a scale factor of 1 V for simplicity of analysis) then the output will be

$$A_m A_c \cdot [\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t].$$

This signal contains signals at the sum and difference frequencies, but not at the original frequencies. (Note that using the cosine formulae rather than sine formulae makes the equations easier to manipulate because cos(a) = cos(-a) [which makes sign unimportant during simplification] and because cos(0) = 1, so that for DC signals [when $a\omega t = 0$], cos($a\omega t$) is equal to unity.)

When we say that the original frequencies are not present in the output of a modulator we make the assumption that the modulator is perfectly balanced - i.e. neither its signal port nor its carrier port has any offset. In practice, both ports will have some offset, and so there will be some signal and carrier leak. Trimming offset on the inputs of a modulator will reduce these leaks, but there will always be untrimmable residual leaks which are due to coupling by stray capacitance, and to nonlinearities in the core, rather than to offsets.

CAUSES OF SIGNAL & CARRIER LEAK IN MODULATORS

- OFFSET ON THE SIGNAL PORT CAUSES CARRIER LEAK
- OFFSET ON THE CARRIER PORT CAUSES SIGNAL LEAK
- EVEN WHEN ALL OFFSETS HAVE BEEN TRIMMED OUT THERE IS RESIDUAL SIGNAL AND CARRIER LEAK CAUSED BY STRAY CAPACITANCE AND CORE NONLINEARITIES

Figure 5. 18

This "sum and difference mixer" is the function which we expect of modulators. However, if we use a linear multiplier as a modulator, we find that any noise or modulation on the carrier input appears in the output signal. If we replace a simple multiplier with a modulator, any amplitude variation on the carrier input disappears.

If a signal $A_c \bullet \cos(\omega_c t)$ is clipped in a comparator or limiting amplifier the square wave output which we obtain has the form represented by the Fourier series $K[\cos(\omega_c t) - 1/3\cos(3\omega_c t) + 1/5\cos(5\omega_c t) - 1/7\cos(7\omega_c t) + ...]$.

The sum of the series 1 - 1/3 + 1/5 - 1/7..... is $\pi/4$. Therefore the value of K, such that a balanced modulator acts as a unity gain amplifier when a positive DC signal is applied to its carrier input, is $4/\pi$.

Therefore if a modulator is driven by a signal $A_m \bullet \cos(\omega_m t)$ and a carrier $\cos(\omega_c t)$ (the carrier amplitude is unimportant provided it is great enough to drive the limiting amplifier), then the output will be the product of the signal and the squared carrier above.

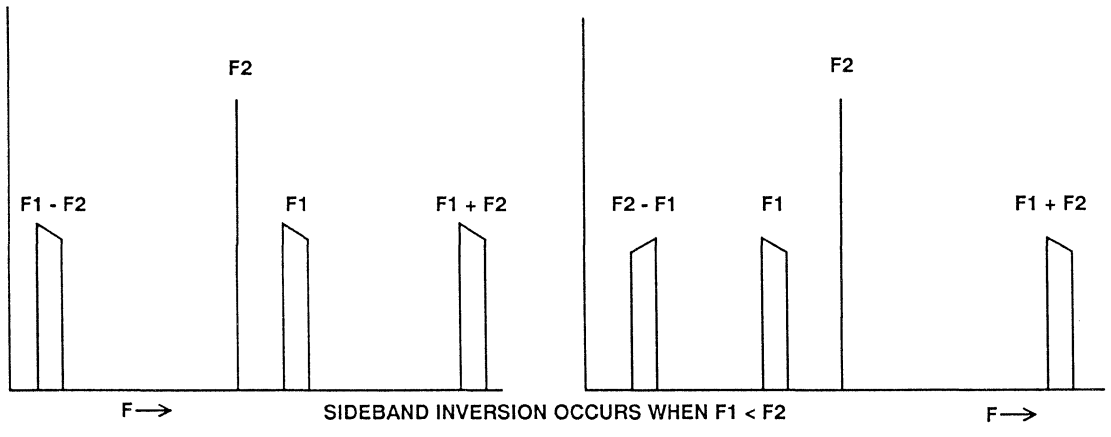
This is

$$2A_m/\pi[\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t$$
$$- 1/3\{\cos(\omega_m + 3\omega_c)t + \cos(\omega_m - 3\omega_c)t\}$$
$$+ 1/5\{\cos(\omega_m + 5\omega_c)t + \cos(\omega_m - 5\omega_c)t\}$$
$$- 1/7\{\cos(\omega_m + 7\omega_c)t + \cos(\omega_m - 7\omega_c)t\} + ...]$$

This output contains sum and difference frequencies of the signal and carrier, and of the signal and each of the odd harmonics of the carrier (in the ideal, perfectly balanced modulator, products of even harmonics are not present - in real modulators, which have residual offsets on their carrier ports, low-level even harmonic products are also present, just how low their level depends on the size of the offset). In most applications a filter is used to remove the products of the higher harmonics so that, effectively, the modulator does behave like a multiplier. (In analyzing the above expressions we must remember that $\cos(A) = \cos(-A)$, so that $\cos(\omega_m - N\omega_c)t = \cos(N\omega_c - \omega_m)t$ so we do not have to worry about "negative frequencies".)

The most obvious application of a modulator is a mixer or frequency changer. If we apply an input signal at F1 and a carrier at F2 to a modulator we find that the output contains signals at the sum and difference frequencies as shown in Figure 5.19. This applies even if the signal is a modulated signal containing a number of components.

5



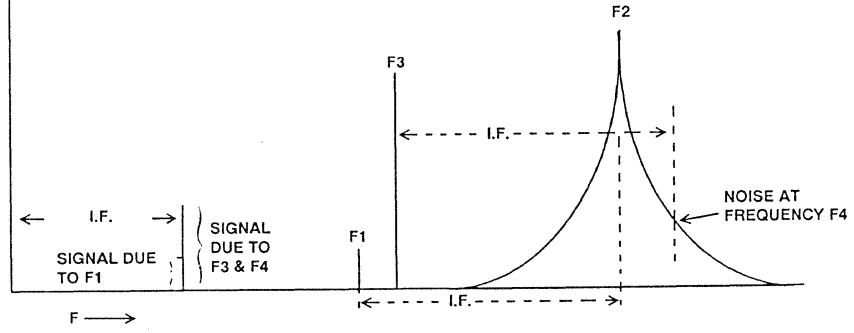
THE MODULATOR AS A MIXER

Figure 5.19

As we have mentioned above, we cannot have "negative frequencies" and so if F1-F2 is negative, what we actually see is a frequency of F2-F1. If F1 is a complex signal containing a number of components, however, we find that if the carrier frequency, F2, is less than F1 then the sidebands are uninverted in both the sum and difference products, but if F2 is greater than F1, then in the difference product, the sidebands are inverted, as shown in the diagram.

The mixer or frequency changer is a key component in most radio receivers. While it is inappropriate to go into a detailed discussion of receiver design in a seminar of this type it is perhaps useful to point out two important features of modulators for use in receivers. These are noise and strong signal performance.[4, 5]

It is self-evident that the mixer used as the front-end mixer of a radio receiver must have low noise, since the signals which it is handling may be less than a microvolt in amplitude, and any significant in-band noise would swamp them. It is less evident that noise in the carrier channel is also important.



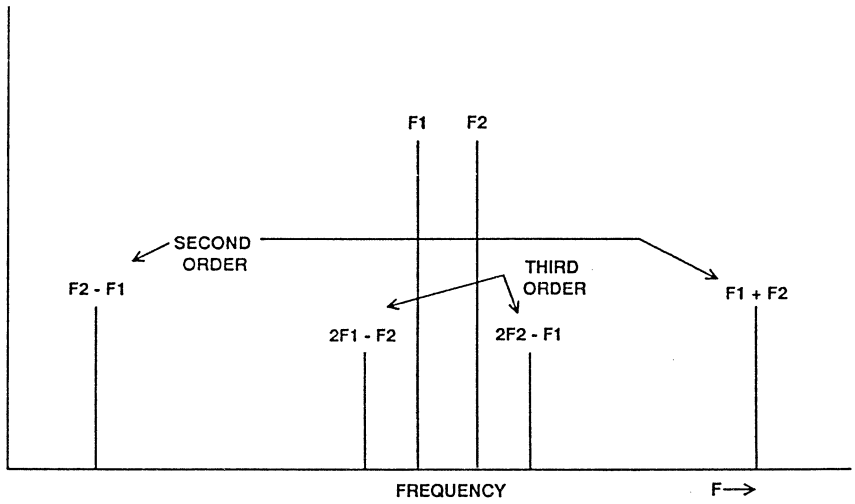
NOTE: NOISE ON THE CARRIER PORT CAUSES UNWANTED RESPONSES

RECIPROCAL MIXING

Figure 5.20

Suppose that we have a mixer with a noisy carrier channel which causes the carrier frequency, F2, to spread out on either side of its center as shown in Figure 5.20. If we are receiving a small wanted signal, F1, then we shall see a small IF output from the mixer at F2-F1. If, however, there is a strong unwanted signal at F3 then the product, F4-F3, of F3 and that part of the broadband carrier noise indicated by F4 on the diagram, will also fall at the IF and, being larger than the wanted IF component, will swamp it. This phenomenon is known as "reciprocal mixing" and can cause a severe limitation on the dynamic range of a receiver. While it is probably more commonly caused by noise or spurious synthesizer sidebands in the oscillator driving the modulator carrier port, it is by no means unknown for it to be caused by noise in the modulator itself, and it should certainly be considered when choosing a mixer for a radio receiver.[6]

In the past, the sensitivity of a radio receiver has been one of its most important features. Today, while sensitivity is still important, the behaviour of the receiver in the presence of strong signals is equally important. The characteristic chosen as a measure of a mixer's performance in this respect is its "third order intermodulation" performance. The key specification is the "Third Order Intercept Point".

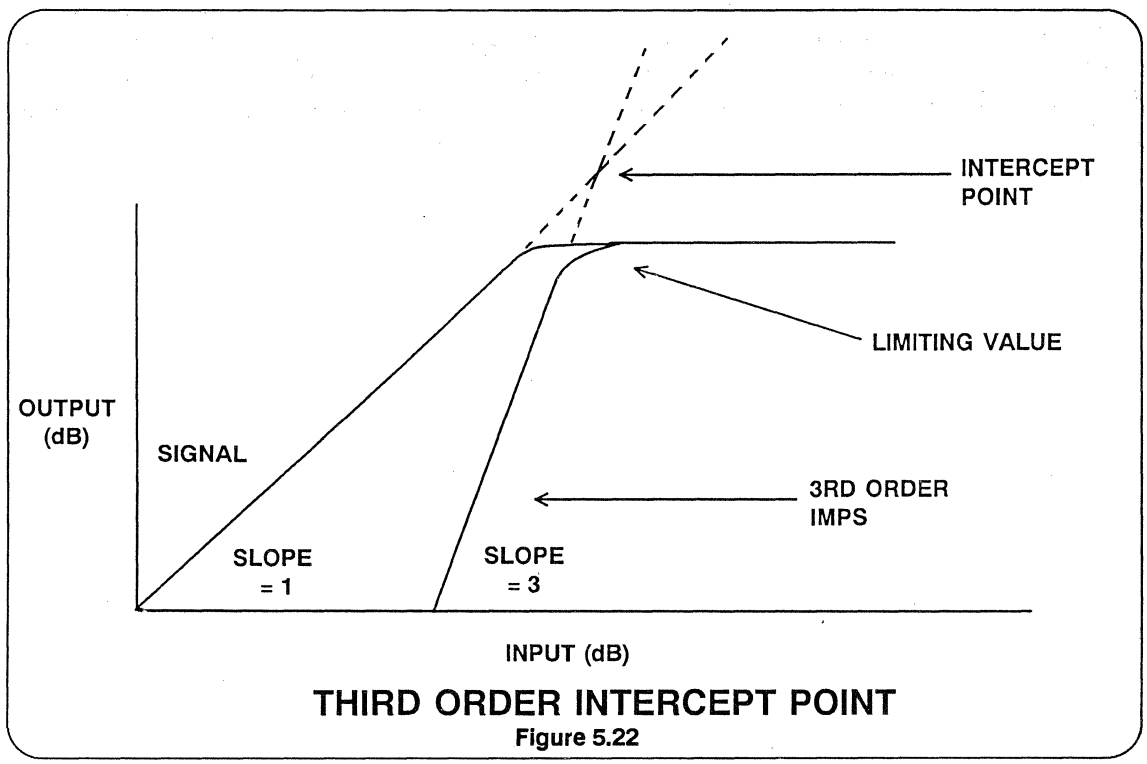


INTERMODULATION PRODUCTS
Figure 5.21

Consider a non-linear amplifier with two large input signals, at F1 and F2 as shown in Figure 5.21. The non-linearity gives rise to additional output components at F1+F2 and F1-F2: these are known as "Second Order Intermodulation Products". These second order products mix with the original signals and produce "Third Order Intermodulation Products" at frequencies of 2F1-F2 and 2F2-F1.

These third order intermodulation products are a major nuisance in radio reception, especially in channelized systems, because they fall close to the signals causing them. As an example consider a receiver monitoring a frequency of 145.500 MHz. In Europe this frequency is the calling frequency of the 2 meter Amateur Band. Working channels in this band are separated by 25 KHz. Suppose that close to the receiver monitoring 145.500 MHz are two transmitters, working at 145.400 and 145.450 MHz respectively. The third order intermodulation products of these two frequencies fall at 145.350 and 145.500 MHz. If the receiver is liable to third order intermodulation distortion (IMD) it will respond to the third order products - which it itself produces - and appear to be receiving a signal at 145.500 MHz.

It is impossible to design an amplifier or mixer which is unaffected by third order intermodulation. All that can be done is to minimize the problem. The third order intercept point mentioned above is the parameter which measures how susceptible a device is to third order intermodulation.



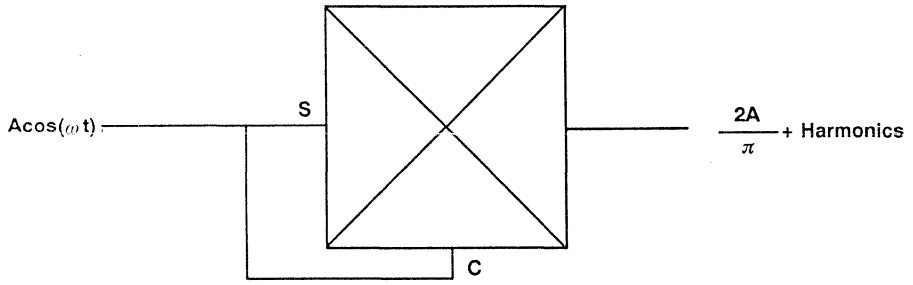
THIRD ORDER INTERCEPT POINT

Figure 5.22

If we plot the input vs the output amplitudes of an amplifier on a log/log (dB/dB) scale as shown in Figure 5.22, we obtain a straight line with a slope of unity. At a certain input level the device saturates ,and the output ceases to rise. If we plot the level of the third order intermodulation products in the output against the level of a two-tone input on the same axes, we obtain a straight line with a slope of 3. This line also ceases to rise when it reaches some limit. If, however, we extend the two straight lines past their limiting values they will eventually cross. The value of the two-tone input at this "intercept point" is the "Third Order Intercept Point" of the device or system being measured.

In mixers for receivers, values of third order intercept point can vary from -15 dBm to over +45 dBm. Any value below 0 dBm is generally considered poor, and good performance requires values of at least +15 dBm and, preferably, more. (For more detailed discussion of intermodulation distortion (IMD) see the Op-Amp section of this seminar.)

The basic mixing property of modulators is also used for many operations where dynamic range is far less important. These include frequency synthesis by mixing, frequency changing with fixed level signals, and sideband generation. Detailed discussion of these operations is beyond the scope of this seminar, but there is one more application which should be considered - precision rectifiers.

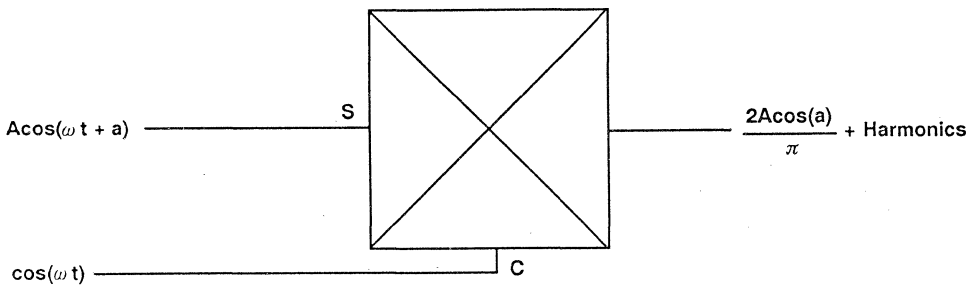


A MODULATOR AS A PRECISION RECTIFIER

Figure 5.23

If an AC signal is applied to both inputs of a modulator as shown in Figure 5.23, the instantaneous output will be equal to the input, if the input is positive, and to the inverse of the input (and therefore still positive), if the input is negative. This arrangement, therefore, behaves as a precision rectifier.

If, instead of applying a signal to both ports of a modulator, a signal is applied to the signal port and a reference signal at the same frequency (but not necessarily the same phase) to the carrier port, then the output will be proportional both to the amplitude of the signal input and the cosine of their phase difference. In this mode a modulator acts as a phase-sensitive rectifier. (See Figure 5.24).



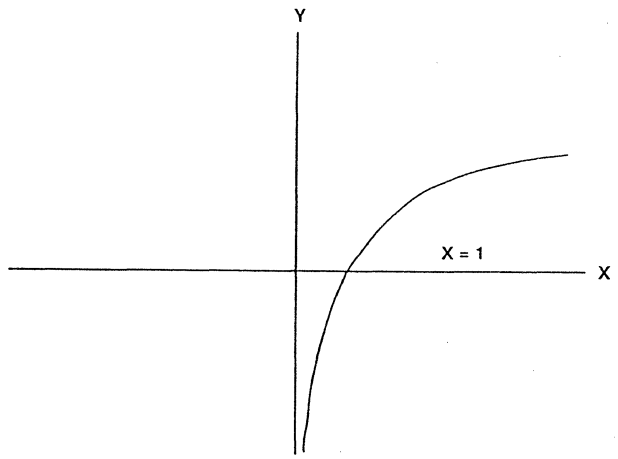
A MODULATOR AS A PHASE-SENSITIVE RECTIFIER

Figure 5.24

LOGARITHMIC AMPLIFIERS

The term "Logarithmic Amplifier" (generally abbreviated to "log amp" - which term will be used in this seminar) is something of a misnomer, and "Logarithmic Converter" would be a better description. The conversion of a signal to its equivalent logarithmic value involves a nonlinear operation, the consequences of which can be confusing if not fully understood. It is important to realize that many of the familiar concepts of linear circuits are irrelevant to log amps. For example the incremental gain of an ideal log amp approaches infinity as the input tends to zero, and a change of offset at the output of a log amp is equivalent to a change of amplitude at its input - not a change of input offset.

For the purposes of simplicity in our initial discussions we shall assume that both the input and the output of our log amp are voltages, although there is no particular reason why logarithmic current, transimpedance, or transconductance amplifiers should not also be designed.



GRAPH OF Y = LOG(X)

Figure 5.25

If we consider the equation y = log(x) we find that every time x is multiplied by a constant A, y increases by another constant A1. Thus if log(K) = K1 then log(AK) = K1+A1, log(A^2K) = K1+2A1, and log(K/A) = K1-A1, etc. This gives a graph as shown in Figure 5. 25, where y is zero when x is unity, y approaches minus infinity as x approaches zero, and which has no values of x for which y is negative.

On the whole log amps do not behave in this way. Apart from the difficulties of arranging infinite negative output voltages such a device would not, in fact, be very useful. A log amp must satisfy a transfer function of the form

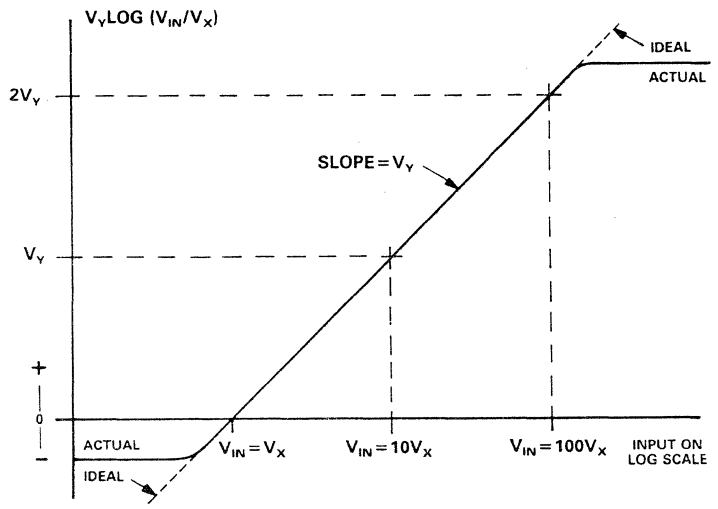
$$V_{out} = V_y \log(V_{in}/V_x)$$

over some range of input values which

may vary from 100:1 (40 dB) to over 1,000,000:1 (120 dB). This ratio is known as the dynamic range of the log amp.

With inputs very close to zero, log amps cease to behave logarithmically, and most then have a linear V_{in}/V_{out} law. This behaviour is often lost in device noise. Noise often provides the limiting factor to the dynamic range of a log amp.

The constant V_y has the dimensions of voltage because the output is a voltage. The input, V_{in}, is divided by a voltage, V_x, because the argument of a logarithm must be a simple ratio.



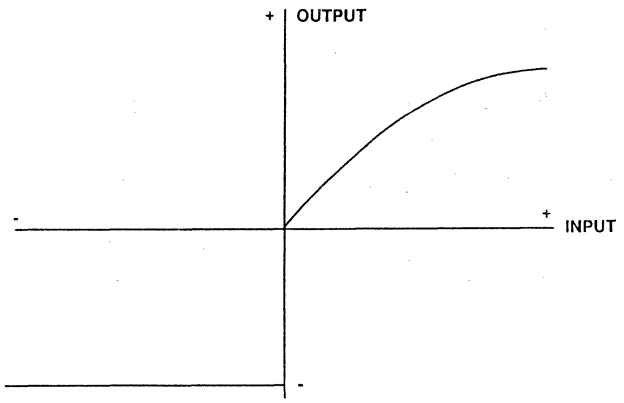
LOG AMP TRANSFER FUNCTION

Figure 5.26

A graph of the transfer characteristic of a log amp is shown in Figure 5.26. The scale of the horizontal axis (the input) is logarithmic, and the ideal transfer characteristic is a straight line. When $V_{in} = V_x$ the logarithm is zero (log1 = 0). V_x is therefore known as the "intercept voltage" of the log amp because the graph crosses the horizontal axis at this value of V_{in}.

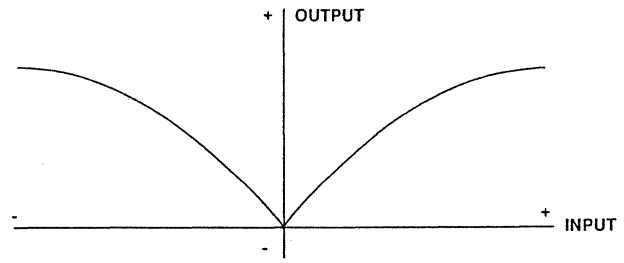
The slope of the line is proportional to V_y. When setting scales we use logarithms to the base 10 because this simplifies the relationship to decibel values: when $V_{in} = 10\,V_x$ the logarithm has the value of 1, so the output voltage is V_y. When $V_{in} = 100\,V_x$ the output is $2\,V_y$ and so forth. V_y can therefore be viewed either as the "slope voltage" or as the "volts per decade factor".

The logarithm function is indeterminate for negative values of x. Log amps can respond to negative inputs in three different ways:



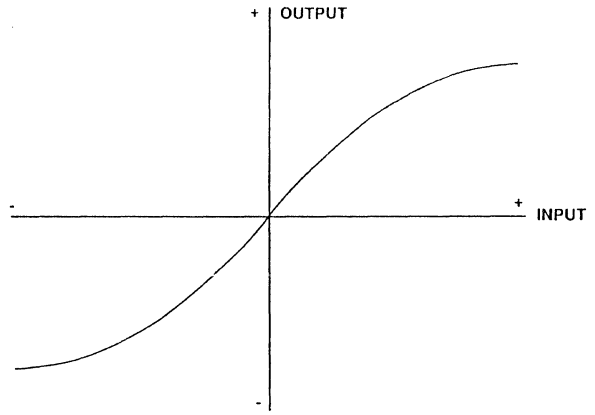
BASIC LOG AMP
(SATURATES NEGATIVE WITH NEGATIVE INPUT)
Figure 5.27

[1] They can malfunction or give a full-scale negative output as shown in Figure 5.27. This is the simplest response and the closest match to the mathematical model - but it is not necessarily the most useful. Such a log amp might be described as a basic log amp.



DETECTING LOG AMP
(OUTPUT POLARITY INDEPENDENT OF INPUT POLARITY)
Figure 5.28

[2] They can give an output which is proportional to the log of the absolute value of the input and disregards its sign as shown in Figure 5.28. This type of log amp can be considered to be a full-wave detector with a logarithmic characteristic, and is often referred to as a detecting log amp.

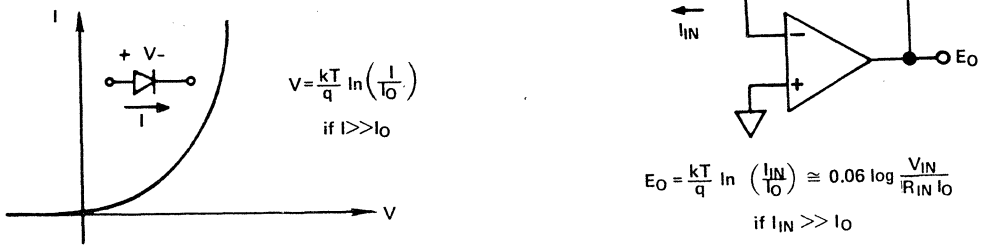


LOG VIDEO AMP OR "TRUE LOG AMP"
(SYMMETRICAL RESPONSE TO POSITIVE OR NEGATIVE SIGNALS)
Figure 5.29

[3] They can give an output which is proportional to the log of the absolute value of the input and has the same sign as the input as shown in Figure 5.29. This type of log amp can be considered to be a video amp with a logarithmic characteristic, and may be known as a logarithmic video amplifier or, sometimes, a "true log amp".

There are three basic architectures which may be used to produce log amps: the basic diode log amp, the successive detection log amp, and the "true log amp" which is based on cascaded semi-limiting amplifiers.

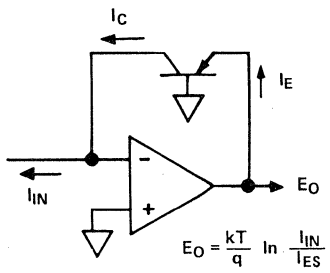
5



THE DIODE/OP-AMP LOG AMP

Figure 5.30

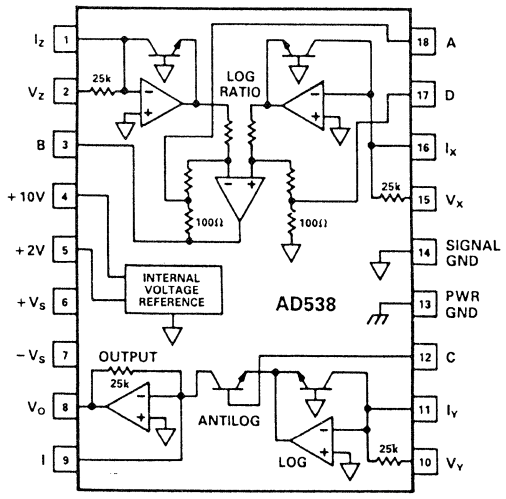
The voltage across a silicon diode is proportional to the logarithm of the current through it. If a diode is placed in the feedback path of an inverting op-amp, the output voltage will be proportional to the log of the input current. (See Figure 5.30)



TRANSISTOR LOG AMP

Figure 5.31

In practice, a combination of bulk resistivity (at high currents) and surface leakage (at low currents) limits the dynamic range of a diode log amp of this type to 40-60 dB. Fortunately, replacing the diode with a diode-connected transistor can easily increase the dynamic range to 120 dB or more. (See Figure 5.31.)

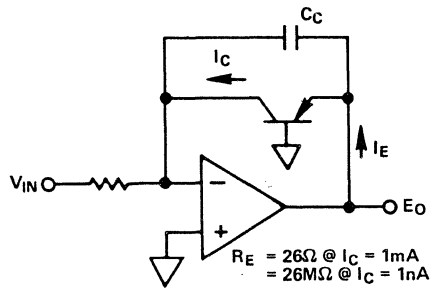


$$V_{out} = V_y\left(\frac{V_z}{V_x}\right)^m$$

THE AD538

Figure 5.32

This type of log amp has three disadvantages: (1) both the slope and intercept are temperature dependent; (2) it will only handle unipolar signals; and (3) its bandwidth is both limited and dependent on signal amplitude. Where several such log amps are used on a single chip to produce an analog computer which performs both log and antilog operations, the temperature variation in the log operations is unimportant, since it is compensated by similar variation in the antilogging. This makes possible the AD538, a monolithic analog computer which can multiply, divide and raise to powers (see Figure 32). Where actual logging is required, however, the AD538 and similar circuits require temperature compensation.[7]



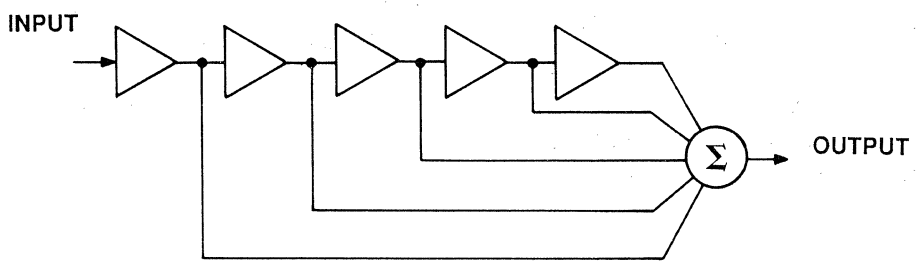
Time Constant $C_C \cdot R_E$ Varies by 1,000,000:1 as I_E goes from 1 mA to 1 nA

LOG AMP BANDWIDTH IS AMPLITUDE DEPENDENT

Figure 5.33

The major disadvantage of this type of log amp for high frequency applications, though, is its limited frequency response - which cannot be overcome. However carefully the amplifier is designed, there will always be a residual feedback capacitance, C_c (often known as "Miller" capacitance[8]), from output to input, which limits the high frequency response. (See Figure 5.33.)

What makes this Miller capacitance particularly troublesome is that the impedance of the transistor emitter-base junction is inversely proportional to the current flowing in it - so that if the log amp has a dynamic range of 1,000,000:1, then its bandwidth will also vary by 1,000,000:1. In practice, the variation is less because other considerations limit the large signal bandwidth, but it is very difficult to make a log amp of this type with a bandwidth, at small signals, greater than a few hundred KHz.



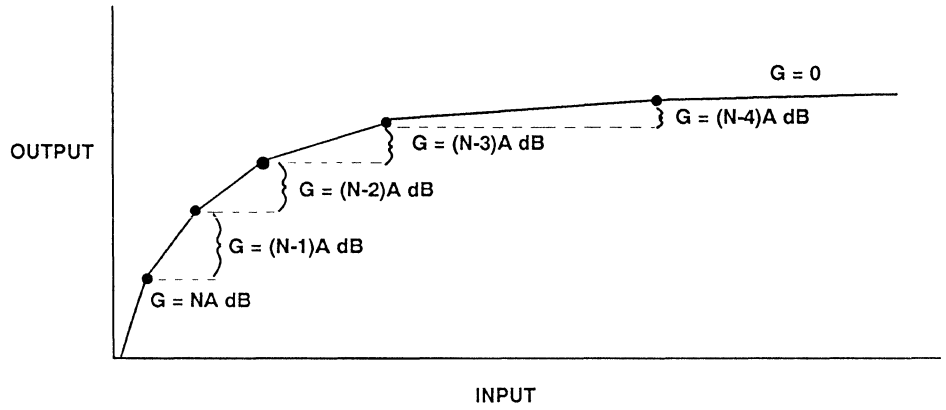
BASIC MULTI-STAGE LOG AMP ARCHITECTURE

Figure 5.34

For high frequency applications, therefore, detecting and "true log" architectures are used. Although these differ in detail, the general principle behind their design is common to both: instead of one amplifier having a logarithmic characteristic, these designs use a number of similar cascaded linear stages having well-defined large signal behaviour.

Consider N cascaded limiting amplifiers, the output of each driving a summing circuit as well as the next stage as shown in Figure 5.34. If each amplifier has a gain of A dB the small signal gain of the strip is NA db. If the input signal is small enough for the last stage not to limit the output of the summing amplifier will be dominated by the output of the last stage.

As the input signal increases the last stage will limit. It will now make a fixed contribution to the output of the summing amplifier, but the incremental gain to the summing amplifier will drop to (N-1)A db. As the input continues to increase, this stage in turn will limit and make a fixed contribution to the output, and the incremental gain will drop to (N-2)A db, and so forth - until the first stage limits, and the output ceases to change with increasing signal input.



BASIC MULTI-STAGE LOG AMP RESPONSE (UNIPOLAR CASE)

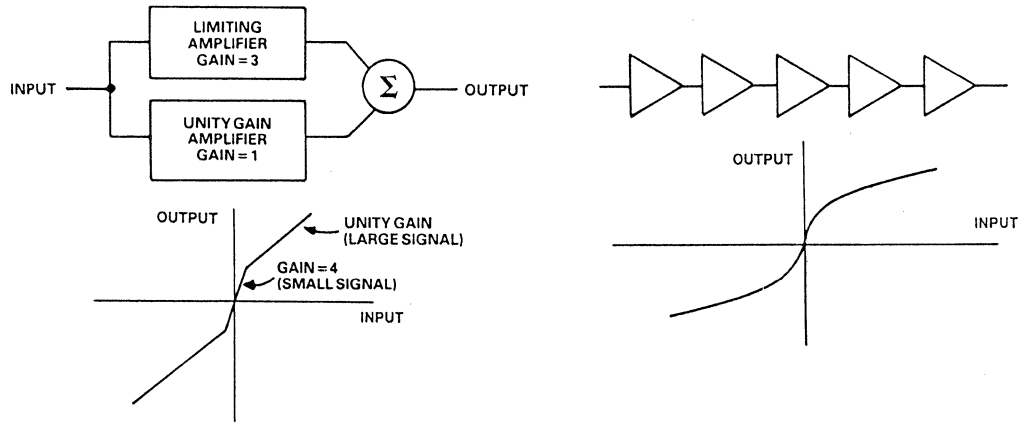
Figure 5.35

The response "curve" is thus a set of straight lines as shown in Figure 5.35. The total of these lines, though, is a very good approximation to a logarithmic curve, and in practical cases is an even better one because few limiting amplifiers, especially high frequency ones, limit quite as abruptly as this model assumes.

The choice of gain, A, will also affect the log linearity. If the gain is too high the log approximation will be poor, if it is too low too many stages will be required. Generally gains of 10-12 dB (3x to 4x) are chosen.

This is, of course, an ideal and very general model - it demonstrates the principle but its practical implementation at very high frequencies is difficult. Assume that there is a delay in each limiting amplifier of t ns (this delay may also change when the amplifier limits but let's consider first order effects!). The signal which passes through all N stages will undergo delay of Nt ns, while the signal which only passes one stage will be delayed only t ns. This means that a small signal is delayed by Nt ns while a large one is "smeared", and arrives spread over Nt ns. A nanosecond equals a foot at the speed of light, so such an effect represents a spread in position of Nt feet in the resolution of a radar system - which may be unacceptable in some systems (for most log amp applications this is not a problem).

A solution is to insert delays in the signal paths to the summing amplifier, but this can become complex. Another solution is to alter the architecture slightly so that instead of limiting gain stages we have stages with small signal gain of A and large signal (incremental) gain of unity (0 dB). We can model such stages as two parallel amplifiers, a limiting one with gain, and a unity gain buffer, which together feed a summing amplifier.

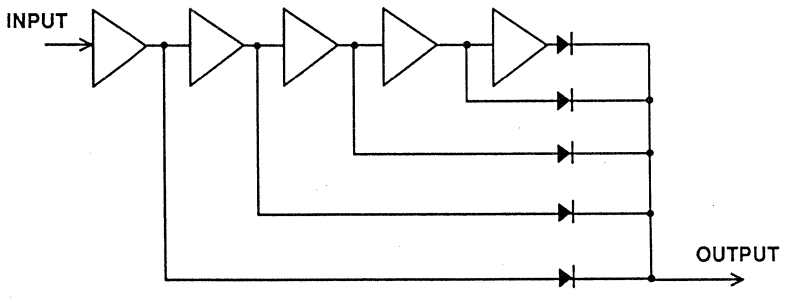


STRUCTURE AND PERFORMANCE OF TRUE LOG AMPLIFIER ELEMENT AND OF A LOG AMP FORMED BY CASCADING SEVERAL SUCH ELEMENTS

Figure 5.36

Figure 5.36 shows that such stages, cascaded, form a log amp without the necessity of summing from individual stages.

Both the multi-stage architectures described above are video log amplifiers or "true log amplifiers", but the commonest type of high frequency log amplifier is the successive detection log amp as shown in Figure 5.37.



Detectors may be full- or half-wave but should be current output devices (not simple diodes) so that the detector outputs may be summed without additional summing components being necessary.

SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER

Figure 5.37

The successive detection log amp consists of cascaded limiting stages, as in the first example, but instead of summing their outputs directly, these outputs are applied to detectors, and the detector outputs are summed. If the detectors have current outputs, the summing process may involve no more than connecting all the detector outputs together.

Log amps using this architecture have two outputs: the log output and a limiting output. In many applications the limiting output is not used, but in some (FM receivers with "S"- meters, for example), both are necessary.

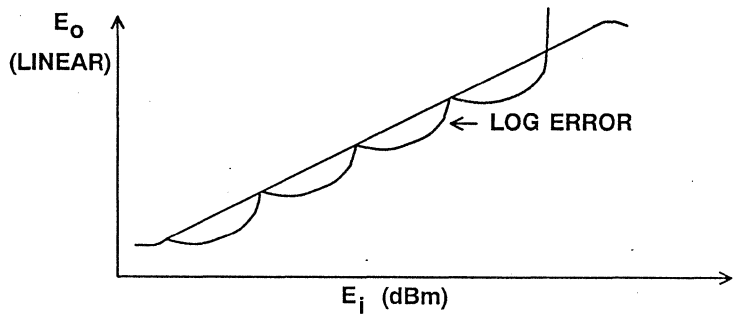
The log output of a successive detection log amplifier generally contains amplitude information, and the phase and frequency information is lost. This is not necessarily the case, however, if a half-wave detector is used, and attention is paid to equalizing the delays from successive detectors - but the design of such log amps is demanding.

The specifications of log amps will, of course, include noise, dynamic range, frequency response (some of the amplifiers used as successive detection log amp stages have low frequency as well as high frequency cutoff), the slope of the transfer characteristic (which is expressed as V/dB or mA/dB depending on whether we are considering a voltage- or current-output device), the intercept point (the input level at which the output voltage or current is zero), and the log linearity. (See Figures 5.38 and 5.39.)

KEY PARAMETERS OF LOG AMPS

- **NOISE** The noise referred to the input (RTI) of the log amp - it may be expressed as a noise figure or as a noise spectral density (voltage, current or both) or as a noise voltage, a noise current, or both
- **DYNAMIC RANGE** Range of signal over which the amplifier behaves in a logarithmic manner (expressed in dB)
- **FREQUENCY RESPONSE** Range of frequencies over which the log amp functions correctly
- **SLOPE** Gradient of transfer characteristic in V/dB or mA/dB
- **INTERCEPT POINT** Value of input signal at which output is zero
- **LOG LINEARITY** Deviation of transfer characteristic (plotted on log/lin axes) from a straight line (expressed in dB)

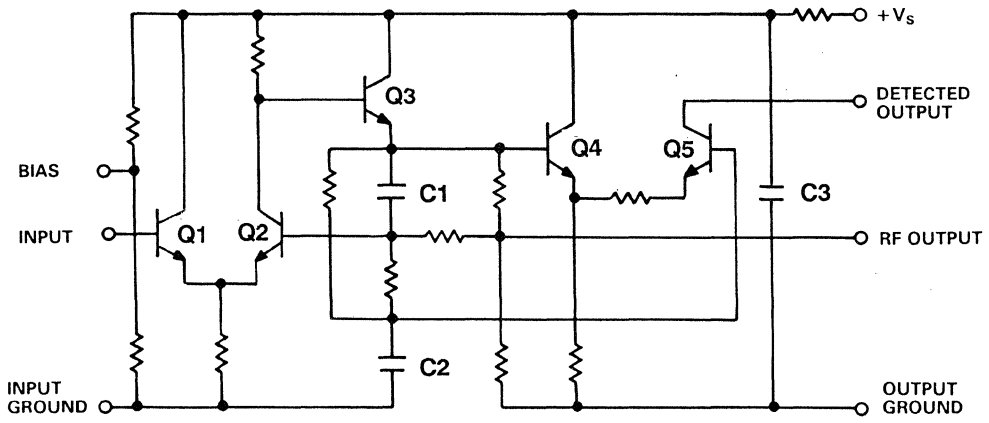
Figure 5. 38



LOG LINEARITY

Figure 5.39

The AD9521 (see Figure 5.40)is a typical high performance successive detection log amplifier component (note that such components are not, themselves, log amplifiers but are components from which log amplifiers may be made). It contains a limiting amplifier which drives both the output and an internal half-wave detector.



AD9521 SIMPLIFIED SCHEMATIC

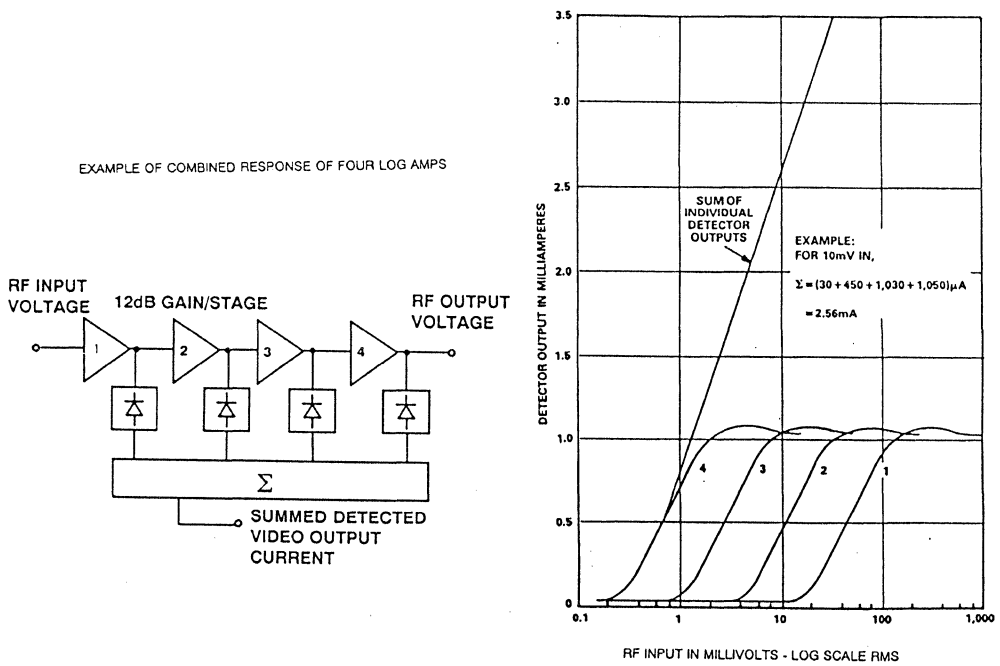
Figure 5.40

AD9521 PERFORMANCE CHARACTERISTICS

- Bandwidth: 7 MHz TO 245 MHz
- Voltage Gain: 12dB
- Maximum Detected Output Current: 0.9 TO 1.1mA at 60 MHz, RF INPUT = 0.5V rms
- Maximum RF Output Voltage: 1.6V P-P
- Maximum Input Before Overload: 1.9V rms
- Power Dissipation: 84mW

Figure 5.41

Figure 5.42 shows the overall transfer function of a log amp made with four cascaded AD9521 devices. The detected current outputs of each stage are plotted against input, as is the sum of all the outputs. It is clear that the sum of these currents approximates to a straight line for inputs between 300 μV and 100 mV - about 48 db.



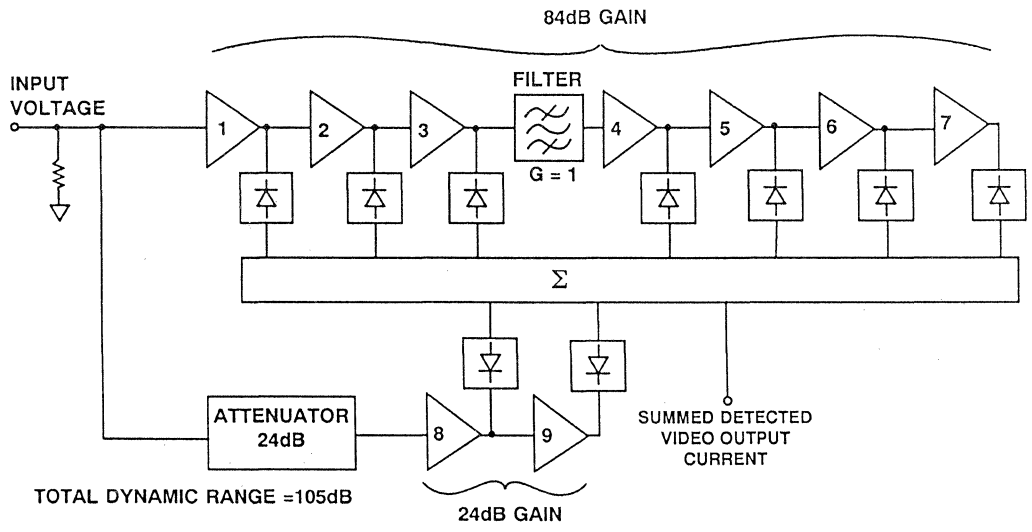
4-STAGE SUCCESSIVE DETECTION LOG STRIP

Figure 5.42

If we add stages, the dynamic range increases by 12 dB with each stage until the strip limits on the noise of its own input stage. This occurs with six stages if they are simply connected together broadband. If NF = 5 dB at 450 Ohms, this gives 70 μV broadband noise [assuming 220 MHz bandwidth] Since an AD9521 limits with 100 mV drive, there must be a gain of less than 1428 (63 dB) to the input of the last stage. At 12 dB/stage this requires five stages so, with the output stage, we cannot have more than six stages without limiting on noise. This gives a dynamic range of less than 70 dB.

We can increase the dynamic range by placing an interstage filter between the third and fourth stages of the strip to limit the bandwidth. If we reduce the bandwidth to 10 MHz, the noise is reduced by the square root of 22 (13.5 dB), so we are still limited to seven stages. The interstage filter used does not affect the accuracy of the log response PROVIDED that it has a voltage gain which is accurately unity throughout its passband.

If we allow for the effects of noise, seven stages will only give us some 80 dB dynamic range. If further dynamic range is required we must use an auxiliary strip. This makes use of the fact that although the output of an AD9521 saturates with 100 mV input, the device operates without problems with inputs of up to 1.9 V.



105 dB LOG AMP USING AN AUXILIARY STRIP

Figure 5.43

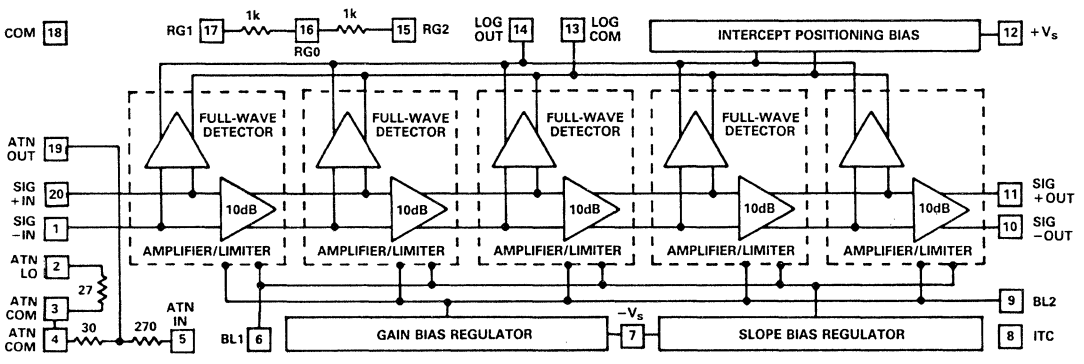
If, therefore, we add another two stage strip of AD9521s, with a 24 dB attenuator at its input, in parallel with the existing strip, and summing its outputs to those of the existing strip, we can add another 24 dB of detector range before the input to the main, seven-stage, strip is overloaded. This gives us nine stages for a theoretical dynamic range of 108 dB - in practice it is possible to achieve about 103-105 dB. This log strip configuration is shown in Figure 5.43.

When using AD9521s in long strips there are various considerations of coupling, decoupling, filter design and feedback via the detector pins which must be addressed in any successful design. These are considered in detail in the AD9521 Application Note which is to be published in late 1989.

The AD9521 contains a single stage limiting amplifier/detector. Moreover, it has a low frequency cutoff of about 10 MHz which makes it impossible to use in many lower frequency applications. The AD640 contains five such stages in a single package and its logarithmic performance extends from DC to 145 MHz. Furthermore its amplifier and detector stages are all balanced so that, with reasonably well-considered layout, instability from feedback via supply rails is unlikely. A block diagram of the AD640 is shown in Figure 5.44.

Unlike all previous integrated circuit log amps, the AD640 is laser trimmed to high absolute accuracy of both slope and intercept, and is fully temperature compensated.

5



BLOCK DIAGRAM OF THE AD640

Figure 5.44

AD640 FEATURES

- 45 dB Dynamic Range - Two AD640s cascadable to 95 dB
- Bandwidth DC to 145 MHz - 120 MHz when cascaded
- Laser-trimmed slope of 1 mA/decade - temperature stable
- Laser-trimmed intercept of 1 mV - temperature stable
- Less than 1 dB log non-linearity
- Balanced circuitry for stability
- Minimal external component requirement

Figure 5.45

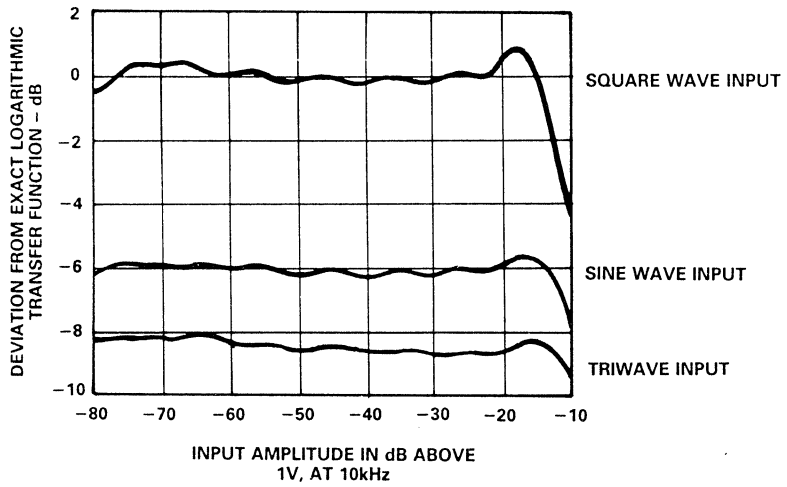
Because of this high accuracy the actual waveform driving the AD640 must be considered when calculating responses. When a waveform passes through a log function generator, the mean value of the resultant waveform changes. This does not affect the slope of the response, but the apparent intercept is modified according to the table. (See Figure 5.46.)

THE EFFECT OF WAVEFORM ON LOG INTERCEPT

Input Waveform	Peak or rms	Intercept Factor	Error (Relative to a dc Input)
Square Wave	Either	1	0.00dB
Sine Wave	Peak	2	-6.02dB
Sine Wave	rms	1.414 ($\sqrt{2}$)	-3.01dB
Triwave	Peak	2.718 (e)	-8.68dB
Triwave	rms	1.569 (e/$\sqrt{3}$)	-3.91dB
Gaussian Noise	rms	1.887	-5.52dB

Figure 5.46

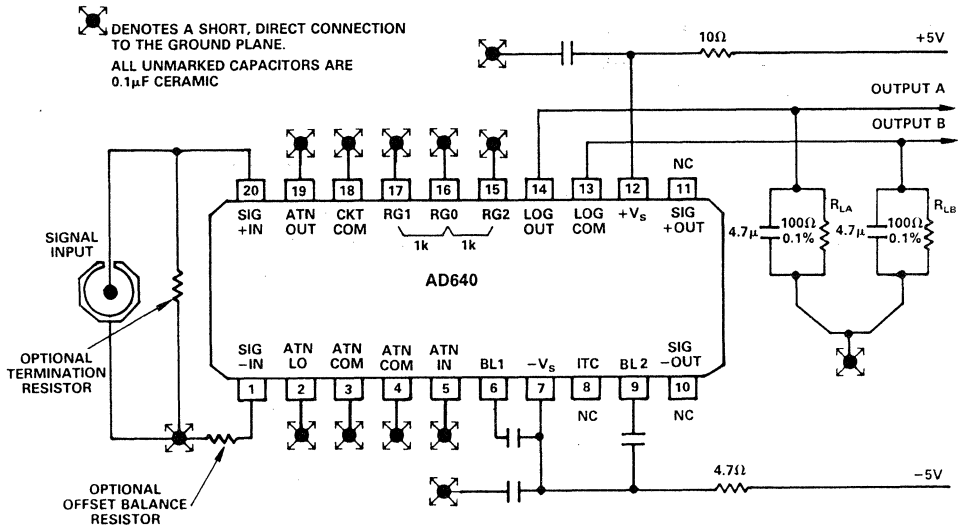
The AD640 is calibrated and laser trimmed to give its defined response to a DC level or a symmetrical 2 KHz square wave, it is also specified to have an intercept of 2 mV for a sine wave input (that is to say a 2 KHz sine wave of amplitude 2 mV pk [NOT pk-pk] gives the same mean output signal as a DC or square wave signal of 1 mV).



THE EFFECT OF WAVEFORM ON LOG LINEARITY AND INTERCEPT

Figure 5.47

The waveform also affects the ripple or non-linearity of the log response. This ripple is greatest for DC or square wave inputs because every value of the input voltage maps to a single location on the transfer function, and thus traces out the full nonlinearities of the log response. By contrast, a general time varying signal has a continuum of values within each cycle of its waveform. The averaged output is thereby "smoothed" because the periodic deviations away from the ideal response, as the waveform "sweeps over" the transfer function, tend to cancel. As is clear in Figure 5.47, this smoothing effect is greatest for a triwave.

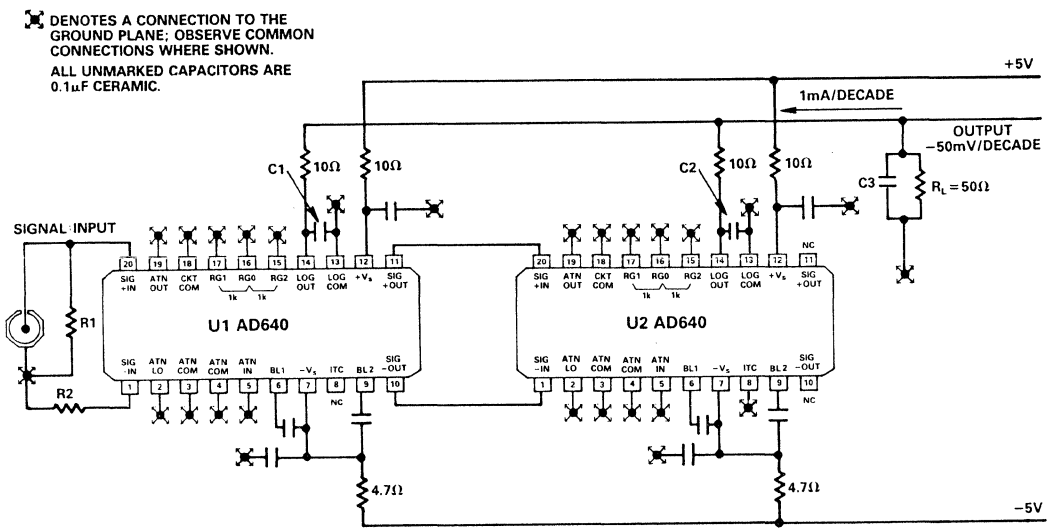


BASIC SINGLE-STAGE AD640 APPLICATION

Figure 5.48

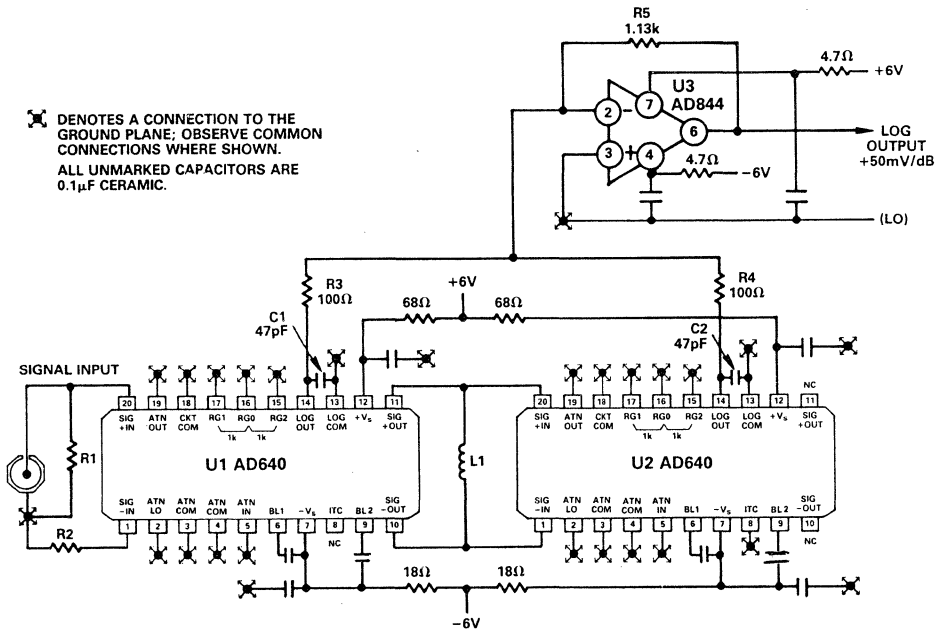
In principle the AD640 is very easy to use (see Figure 5.48) but with such a high wideband gain great care must be taken to keep ground connections short, low inductance and low resistance, to exclude unwanted external signals, and to prevent outputs feeding back to inputs. Detailed applications information is available on the AD640 data sheet.

When two AD640s are cascaded as shown in Figure 5.49, the second will be delivering an output from the noise of the first. If the full potential dynamic range is to be realized the bandwidth must be limited. This may be done with high-pass, low-pass or band-pass filters, depending on the required response, but, as with the AD9521, the voltage gain of these filters in their passband must be unity or there will be a kink in the log response. Figure 5.50 shows a 70 dB log amp for broadband operation from 50 to 150 MHz. The 100 MHz passband limits the possible dynamic range, but the performance is still exceptional. Figure 5.51 shows a 95dB 10Hz to 100KHz log amp using two cascaded AD640s.



BASIC CASCADED AD640 APPLICATION

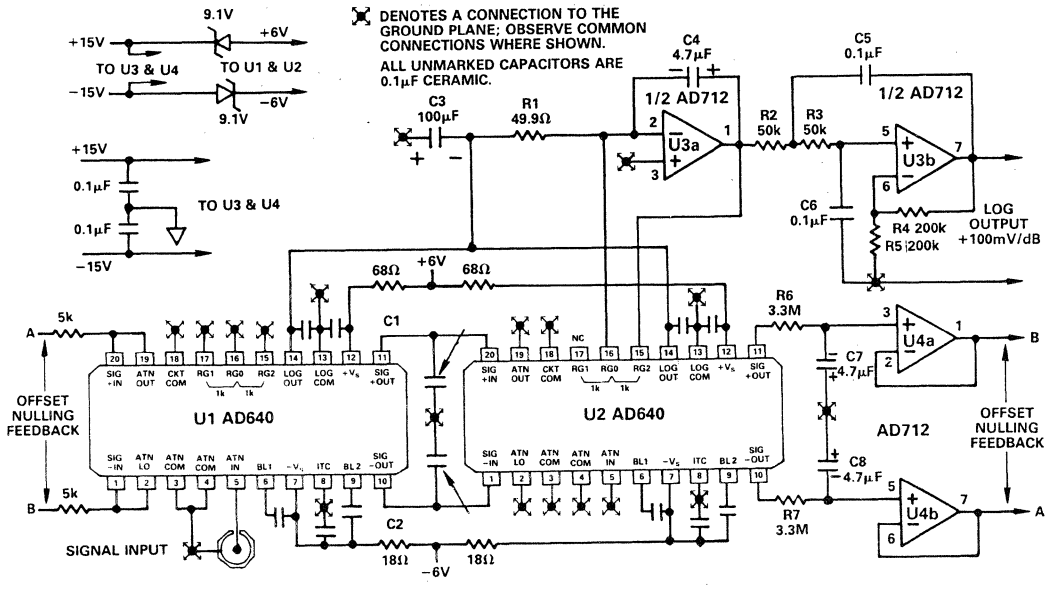
Figure 5.49



70 dB LOG AMP FOR 50-150 MHz USING TWO AD640

Figure 5.50

5



95 dB L.F. LOG AMP (10Hz-100kHZ) USING TWO AD640

Figure 5.51

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SECTION VI

TIME DOMAIN FUNCTIONS: COMPARATORS AND PIN ELECTRONICS

TIME DOMAIN FUNCTIONS: COMPARATORS AND PIN ELECTRONICS

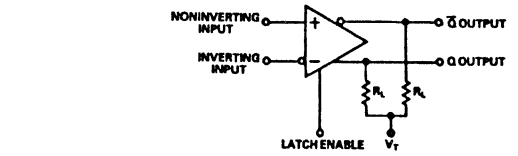
COMPARATOR OPERATION

High speed comparators have widespread applications in automatic test equipment, instrumentation, electronic warfare, radar, and telecommunications. In the field of data acquisition, high speed comparators form the basic building block for flash converters and successive approximation A/D converters.

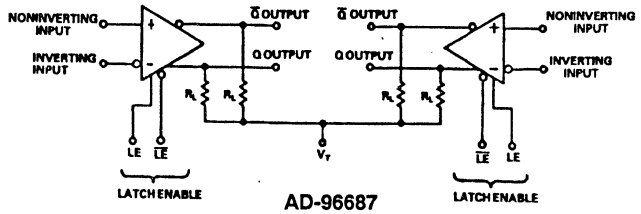
A block diagram, timing, and characteristic data for the AD96685 (single) and AD96687 (dual) ECL comparators is shown in Figure 6.1. In addition to performing the basic compare function, this comparator contains an integral latch. The AD96687 comparator "tracks" the input signal when the LE line is high and the LE line is low. The comparator data is latched when the LE line goes low and the LE line goes high. Differential inputs on the latch enable lines on the AD96687 insure a minimum amount of clock feedthrough which could alter the comparator's input threshold. If the latch function is not going to be used, the LE line should be grounded, and the LE left floating or tied to -2V, thereby disabling the latching function. Occasionally, one of the two comparator stages in the AD96687 will not be used. The inputs of the unused comparator should not be allowed to "float". The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by insuring that the two inputs are at least one diode drop apart, while also grounding the LE input.

Best performance of high speed ECL comparators will be achieved with the proper use of ECL terminations. The open-emitter outputs of the AD96685/AD96687 are designed to be terminated in 50 ohms to -2V. If a -2V supply is not available, an 82 ohm resistor to ground and a 180 ohm resistor to -5.2V provides a suitable equivalent. If high speed ECL signals must be routed more than a few centimeters, microstrip techniques should be used to prevent ringing and possible oscillation or false triggering. The use of a low impedance ground plane and power supply decoupling (with 0.1μF ceramic capacitors) at the power pins is also essential. Sockets should be avoided due to stray capacitance and inductance. If proper high speed techniques are used, the AD96685/96687 should be free from oscillation when the comparator input signal passes through the switching threshold, and resolution approaching 1mV should be achievable.

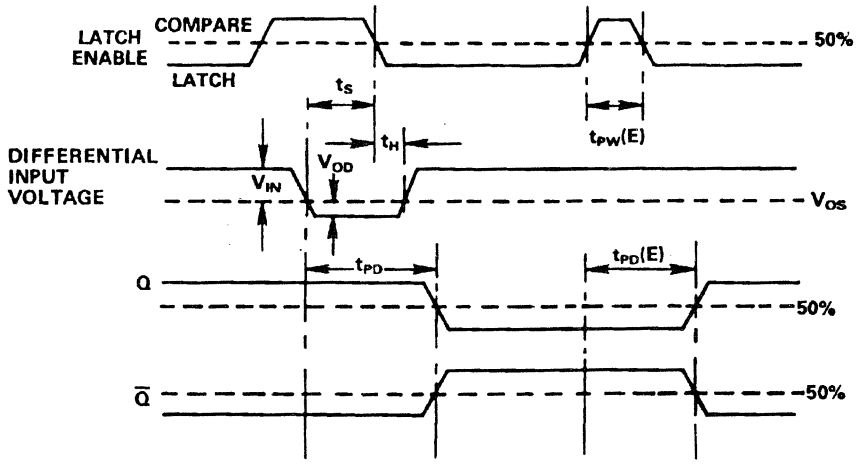
Another technique for reducing the possibility of oscillation when the input signal is near the switching threshold is the use of a narrow latch enable strobe. If the latch enable pulse width is made equal to or slightly less than the comparator propagation delay, the effects of positive feedback from the output to the input are greatly reduced. For the AD96685/96687, the minimum latch enable pulse width is 2ns compared to the propagation delay of 2.5ns. In this mode, the comparator is allowed to compare or "track" for only 2ns. The remainder of the time is spent in the "latch" mode until the next comparison is made.



AD-96685



AD-96687



t_S = 0.5ns - Minimum Setup Time
t_H = 0.5ns - Minimum Hold Time
t_{PD} = 2.5ns - Input to Output Delay
t_{PD} (E) = 2.5ns - LATCH ENABLE to Output Delay
t_{PW}(E) = 2.0ns - Minimum LATCH ENABLE Pulse Width
V_{OS} = 10mV - Input Offset Voltage
V_{OD} = 10mV - Overdrive Voltage

- DISPERSION: 50ps
- COMMON MODE REJECTION RATIO: 90dB
- ECL COMPATIBLE
- INPUT IMPEDANCE: 200k Ω||2pF
- INPUT VOLTAGE RANGE: -2.5V, +5V
- POWER DISSIPATION: AD-96685 (SINGLE) - 120mW
  AD-96687 (DUAL) - 240mW
- POWER SUPPLY REJECTION RATIO: 70dB

AD-96685/AD-96687 COMPARATOR SPECIFICATIONS

Figure 6.1

REDUCING COMPARATOR OSCILLATION

- **Layout - Microstrip Techniques**
- **Ground Plane**
- **No Sockets**
- **Power Supply Decoupling at Pins Using Chip Capacitors**
- **Narrow Latch Strobe**
- **Hysteresis**

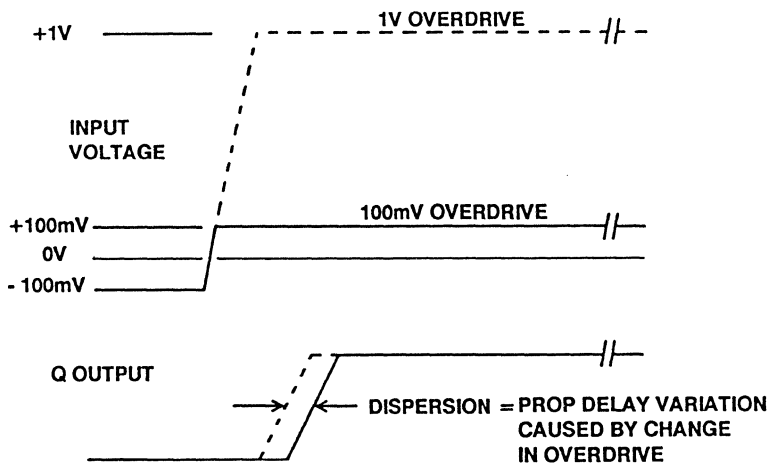
Figure 6.2

COMPARATOR PROPAGATION DELAY DISPERSION

Dispersion is a specification which is important in critical timing applications such as ATE, bench instruments, and nuclear instrumentation. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed. For the AD96685/96687 comparators, dispersion is typically 50ps as the overdrive is changed from 100mV to 1V (see Figure 6.3). This specification applies for both positive and negative overdrives since the AD96685/96687 has equal delays for positive and negative going inputs.

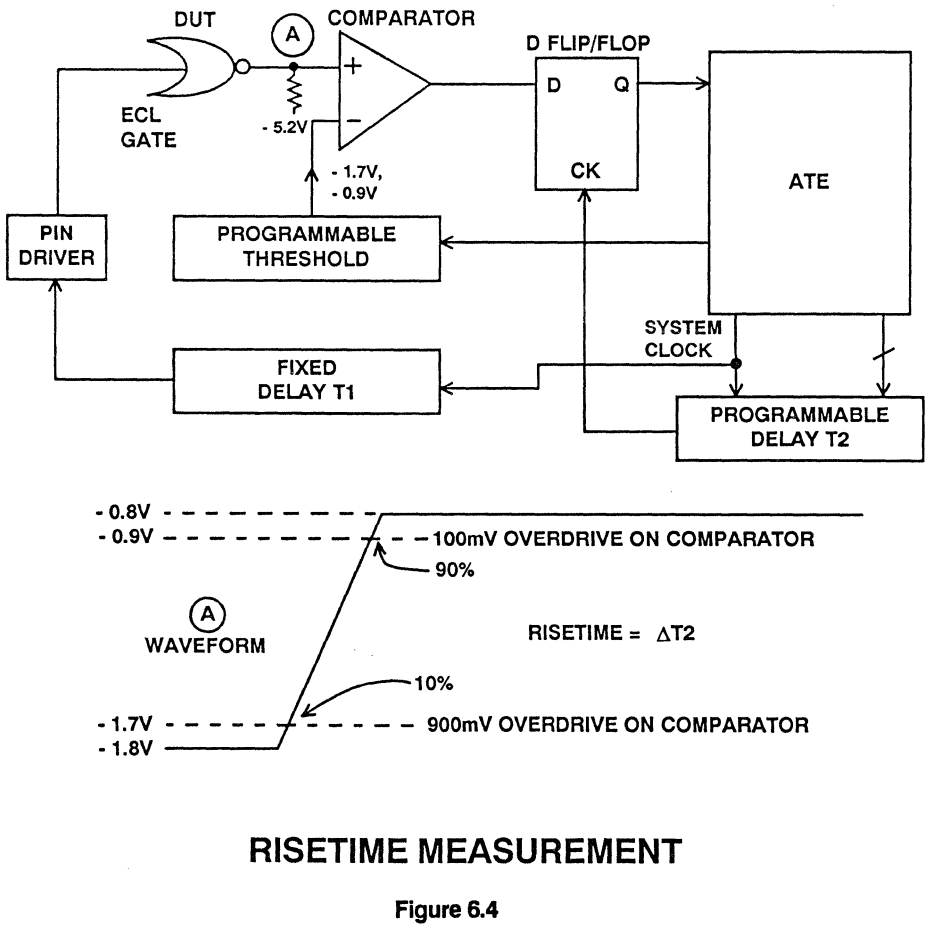
The 50ps propagation delay dispersion of the AD96685/96687 offers considerable improvement over the 200-300ps dispersion of the older 685/687 series comparators.

The effects of dispersion are illustrated in the ATE application shown in Figure 6.4, where the device under test (DUT) is being tested for output logic risetime. The comparator threshold is first set to -1.7V (10% point). The programmable delay T2 is set until the output of the D flip-flop is toggling equally between the 1 and 0 state. The comparator threshold is then set to -0.9V (90% point) and the programmable delay is changed until the D flip-flop is again toggling equally between the 1 and 0 state. The change in T2 between the two measurements corresponds to the DUT output logic risetime. Any propagation delay dispersion in the comparator will cause a corresponding risetime measurement error due to the two different overdrive conditions required to perform the 10% and 90% measurement.



COMPARATOR DISPERSION

Figure 6.3



RISETIME MEASUREMENT

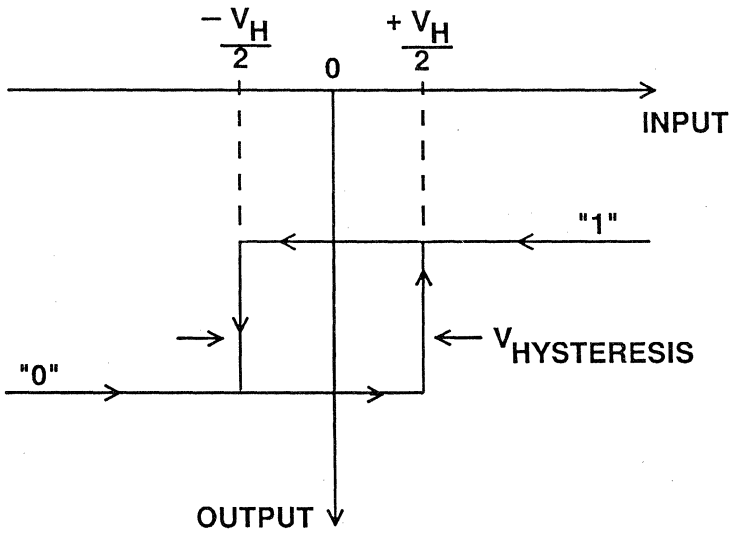
Figure 6.4

COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often useful in a noisy environment or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 6.5. If the input voltage approaches the threshold from the negative direction, the comparator will switch from a "0" to a "1" when the input crosses $+V_H/2$. The "new" switching threshold now becomes $-V_H/2$. The comparator will remain in a "1" state until the threshold $-V_H/2$ is crossed coming from the positive direction. In this manner, noise centered around OV input will not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

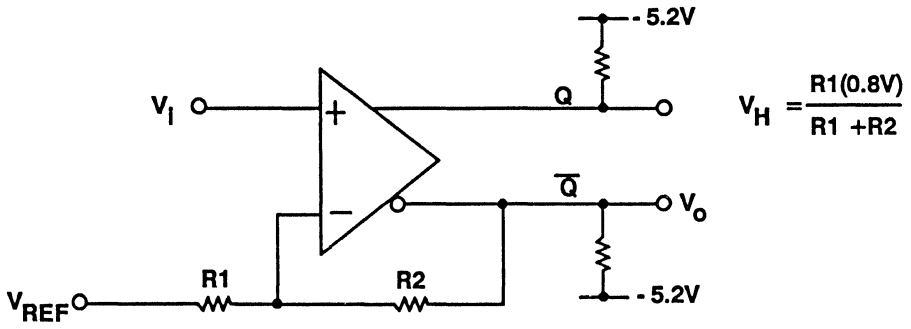
Positive feedback from the output to the input is often used to produce hysteresis in a comparator (see Figure 6.6).

The AD96685/96687 series comparators are designed so that the latch enable function can be used to produce hysteresis as shown in Figure 6.7.



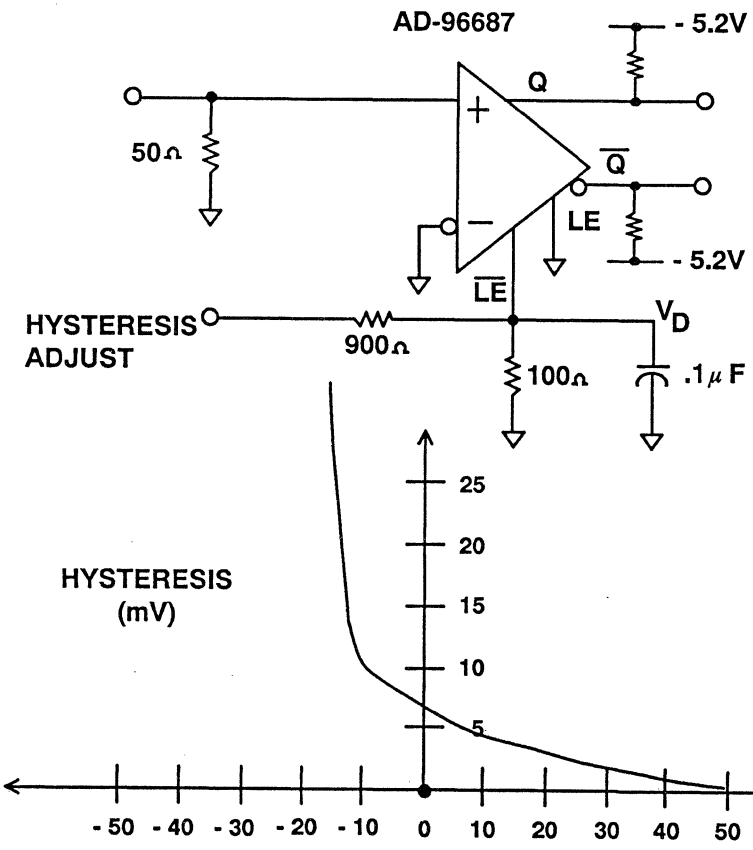
COMPARATOR HYSTERESIS

Figure 6.5



HYSTERESIS USING POSITIVE FEEDBACK

Figure 6.6

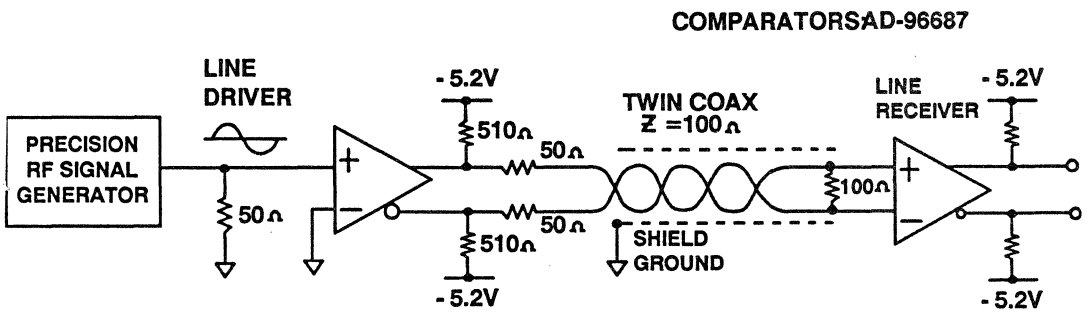


HYSTERESIS USING LATCH ENABLE

Figure 6.7

COMPARATOR LINE DRIVER AND RECEIVER

Figure 6.8 shows how high speed comparators can be used to transmit and receive high speed clock and logic signals across noisy interfaces with minimal degradation. The line driving comparator converts the sinewave output of the RF signal generator into balanced differential ECL logic signals. The driver is source terminated and the signal transmitted over shielded 100 ohm twin-conductor coaxial cable. The line receiving comparator input is terminated in 100 ohms line-to-line. This arrangement makes the output of the line receiver virtually immune to jitter caused by common mode noise on the twin conductors.

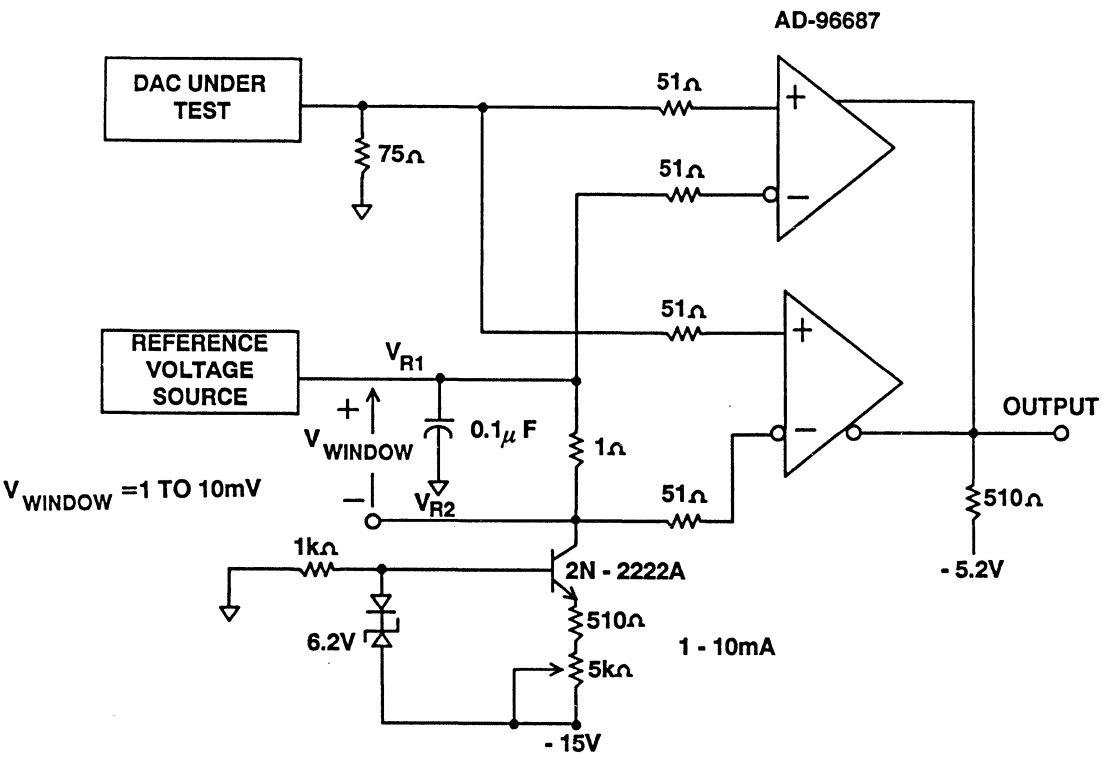


PRECISION CLOCK DISTRIBUTION: COMPARATOR LINE DRIVER AND RECEIVER

Figure 6.8

HIGH SPEED WINDOW COMPARATOR CIRCUIT FOR SETTLING TIME MEASUREMENTS

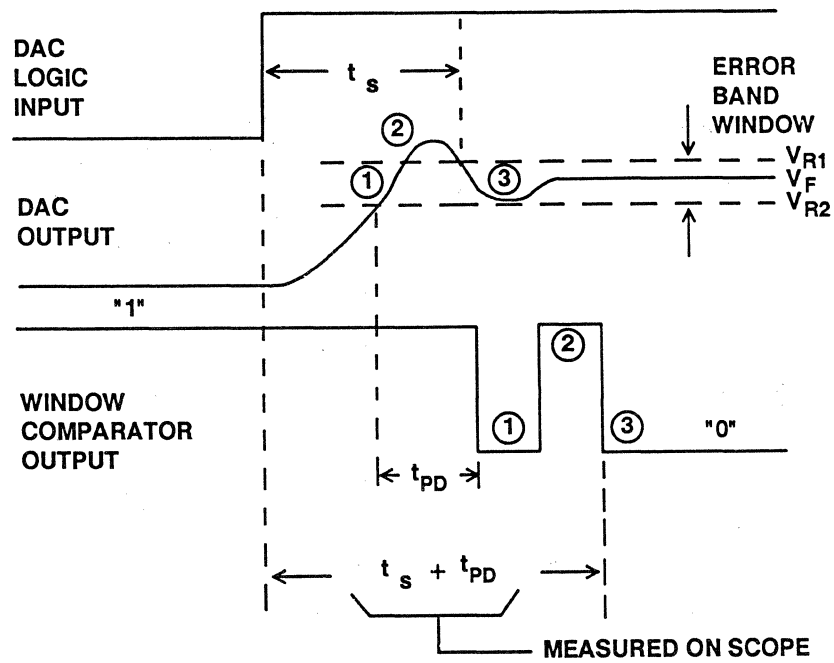
A dual AD96687 comparator can be used to make settling time measurements as shown in Figure 6.9. The wire-or feature of ECL logic is used so that the output of the window comparator circuit is a logic 0 whenever the common input signal lies between the window voltage set by V_{R1} and V_{R2}. The error band window is set by adjusting the current source which develops the window voltage across the 1 ohm resistor. The upper reference voltage V_{R1} is set by the reference voltage generator.



WINDOW COMPARATOR FOR MEASURING D/A CONVERTER SETTLING TIME

Figure 6.9

Figure 6.10 shows the resulting waveforms after proper setting of the reference voltages. The upper reference voltage V_{R1} is set to the final value of the DAC output (measured with a DVM) plus 1/2 the error band window. The current source is set so that V_{R2} is 1/2 the error band below the final value. The DAC is then switched from all zeros to all ones, and the settling time is measured as shown. The propagation delay of the comparator (t_{PD} = 2.5ns) must be subtracted in order to obtain the correct settling time measurement.



WINDOW COMPARATOR SETTLING TIME WAVEFORMS

Figure 6.10

HIGH SPEED COMPARATOR SELECTION GUIDE

PART #	TYPE	TTL/ECL	PROP. DELAY	POWER DISSIPATION
[1] AD-96685	Single	ECL	3.5 ns MAX	135 mW MAX
[1] AD-96687	Dual	ECL	3.5 ns MAX	270 mW MAX
AD-9686	Single	TTL	7 ns MAX	306 mW MAX
[2] AD-9696	Single	TTL	6 ns MAX	351 mW MAX
[2] AD-9698	Dual	TTL	6 nx MAX	176 mW MAX
[3] AD-790	Single	TTL	40 ns MAX	60-240 mW

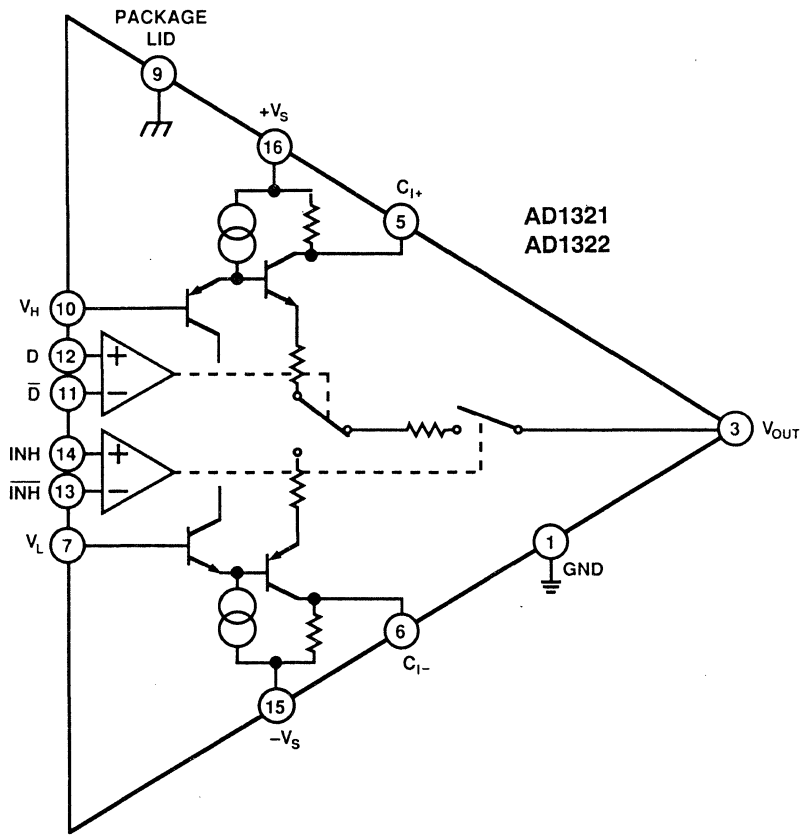
[1] DISPERSION = 50 ps TYP
[2] DISPERSION = 100 ps TYP
[3] WIDE COMMON MODE INPUT RANGE
SINGLE + 5 V OR ±15V SUPPLY OPERATION

Figure 6.11

PIN ELECTRONICS FOR ATE

AD1321 and AD1322 High Speed Pin Drivers

The AD1321 and AD1322 pin drivers are designed to be used in general purpose instrumentation and digital functional test equipment. The main difference between the AD1321 and AD1322 is rise and fall times. The AD1321 is best suited for operation at or below 100MHz, where the AD1322 is capable of greater than 200MHz operation. A block diagram of the AD1321 and AD1322 is shown in Figure 6.12. The purpose of the pin driver is to accept digital, analog and timing information from a system source known as the Formatter and combine these to drive the device under test. Simply stated, a pin driver performs the function of a precise, high speed level translator. Key features of the AD1321 and AD1322 are summarized in Figure 6.13.



HIGH SPEED PIN DRIVER BLOCK DIAGRAM

Figure 6.12

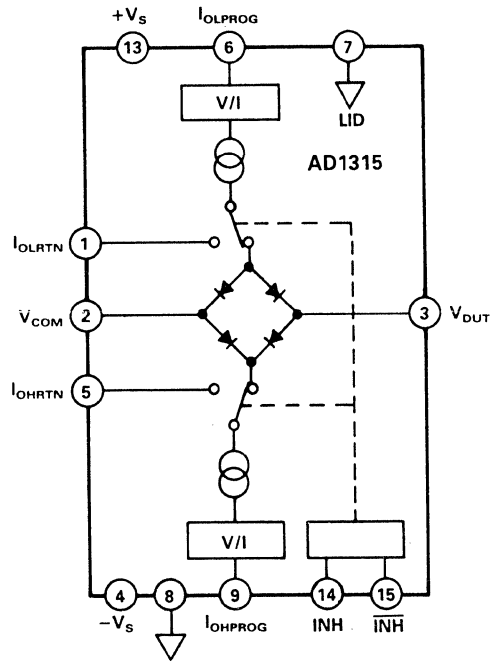
KEY FEATURES: AD1321/AD1322 PIN DRIVERS

- Driver Operation: 100MHz (AD1321), 200MHz (AD1322)
- Slew Rate: 1V/ns (AD1321), 2V/ns (AD1322)
- Edge Matching: 250 ps (AD1321), 200ps (AD1322)
- Variable Output Voltages for ECL, TTL, CMOS
- 50Ω Output Impedance
- Driver Inhibit Function
- High Speed Differential Inputs for Maximum Flexibility
- Hermetically Sealed Small Gull Wing Package

Figure 6.13

AD1315 High Speed Active Load

The AD1315 high speed active load is also used in the same tester application. The function of the active load is to provide independently variable source and sink currents for the device under test. The AD1315 block diagram is shown in Figure 6.14. An active load performs the function of loading the output of the device under test with a programmed I_{OH} and I_{OL}. These currents are independently programmed. V_{COM} is the commutation voltage point at which the load switches from a source to sink mode. The active load may also be inhibited, steering current to the IOLRTN and IOHRTN pins, effectively disconnecting it from the test pin. Key features of the AD1315 are summarized in Figure 6.15.



ACTIVE LOAD BLOCK DIAGRAM

Figure 6.14

6

KEY FEATURES: AD1315 ACTIVE LOAD

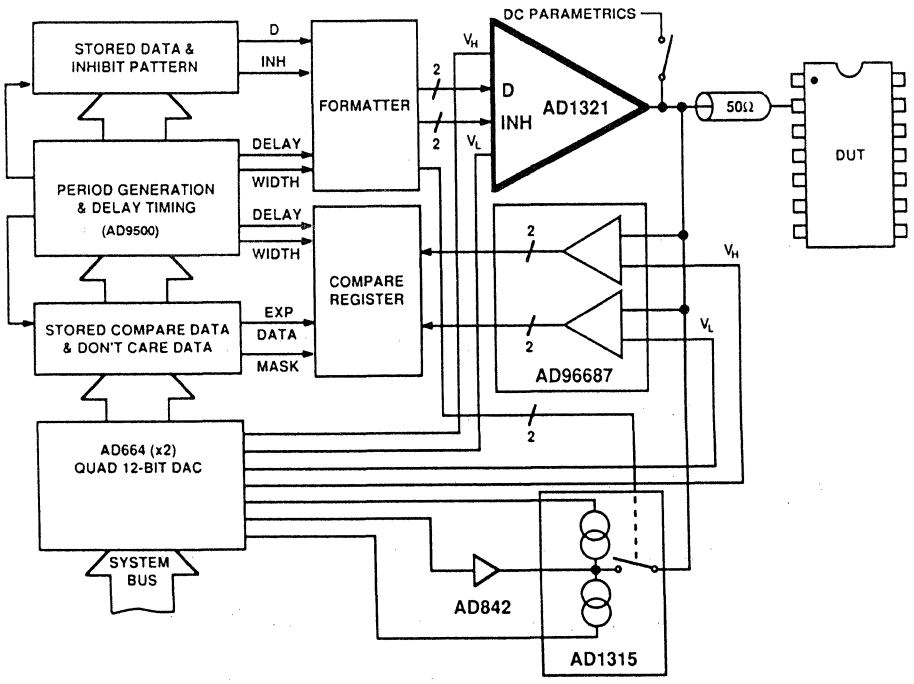
- ±50mA Voltage Programmable Current Range
- 1.5ns Propagation Delay
- Inhibit Mode Function
- High Speed Differential Inputs for Maximum Flexibility
- Hermetically Sealed Small Gull Wing Package
- Compatible with AD1321, AD1322 Pin Drivers

Figure 6.15

Tester Application

Figure 6.16 shows a block diagram illustrating the electronics behind a single pin of a high speed digital functional test system with the ability to test I/O pins on logic devices. As shown, the AD9500 programmable delay generator is used to define the shape, in time, of the digital waveform being constructed in the Formatter. It can also be used to correct each channel for timing deskews which may originate "downstream" from the Formatter (refer to Section VII). The Formatter waveforms, or vectors as they are called, are sent to the driver and active load.

The driver converts the ECL logic "1" to the programmed logic high level, V_H, and the ECL logic "0" to the programmed logic low level, V_L. Since these vectors have all been deskewed, any variation in propagation delay through the driver due to temperature and duty cycle will result in testing errors. The driver is required to swing the full TTL levels of +7V and down to the minimum ECL levels of -1.8V.



HIGH-SPEED DIGITAL TEST SYSTEM BLOCK DIAGRAM

Figure 6.16

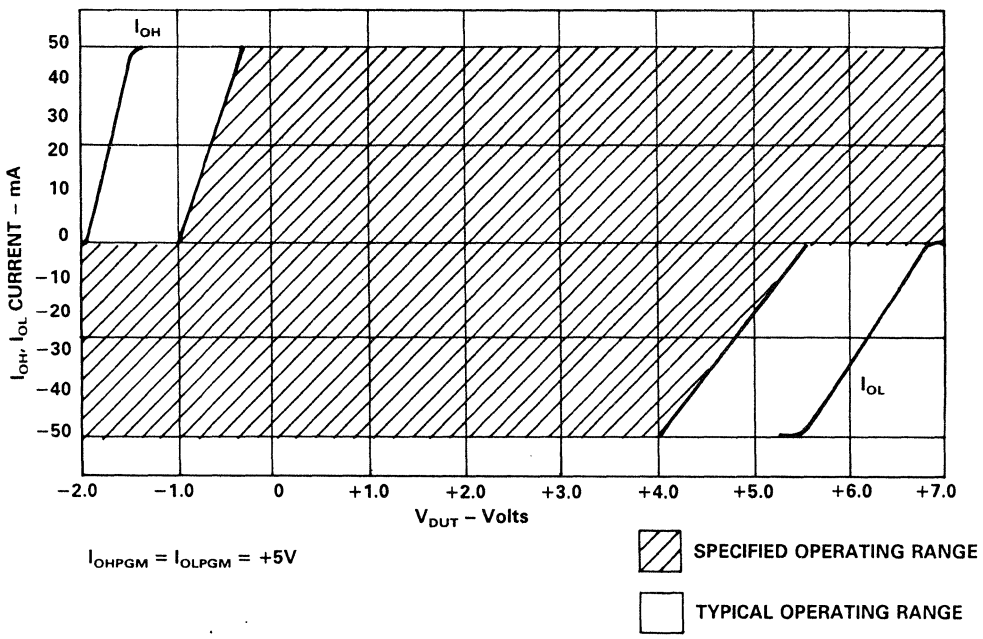
When the driver is stimulating the input of a device under test the output is normally being monitored to ensure that the output meets the data sheet logic "1" and "0" minimum and maximum logic voltage and current levels. As an example, for standard TTL logic, the driver will force a logic "1" of 2.4V at the output by driving the input to a logic low, or 0.8V. The output of the DUT must sustain a 2.4V level under a current load of -400μA. When the driver delivers a logic "1" to the DUT's input its output must sustain a 0.4V level while under a current load of 16mA. With a transfer function of 1V/10mA, the AD1315's logic high and low current program voltages are set at 1.6V and 0.4V, respectively (removing any gain and offset errors). The point at which the DUT changes from sink to source mode occurs when the DUT's output voltage passes through the programmed active load's commutation voltage, in this case 1.6V.

Similar to the driver, propagation changes through the active load due to variation in temperature and duty cycle will directly influence the overall accuracy of the tester. Recent advances in design and process technology allow the driver and active load functions to be developed in a single monolithic IC which greatly reduces these errors.

AD1315 V_{DUT} Voltage Range

In Figure 6.17, V_{DUT} range, I_{OH} and I_{OL} typical current maximums are plotted versus DUT voltage. In the I_{OH} mode (V_{DUT} higher than V_{COM}), the load will sink 50 mA, until its output starts to saturate at approximately -1.5V. In the I_{OL} mode (V_{DUT} lower than V_{COM}), the load will source 50 mA until its output starts to saturate at approximately +5.5V. At +7V, the source current will be close to zero.

Ideally, the commutation point set at V_{COM} would provide instantaneous current sink/source switching. Because of I/V characteristics of the internal bridge diodes, this is not the case. To guarantee full current switching at the DUT, at least a 1 volt difference between V_{COM} and V_{DUT} must be maintained in steady state conditions. Because of the relatively fast edge rates exhibited by typical logic device outputs, this should not be a problem in normal ATE applications.

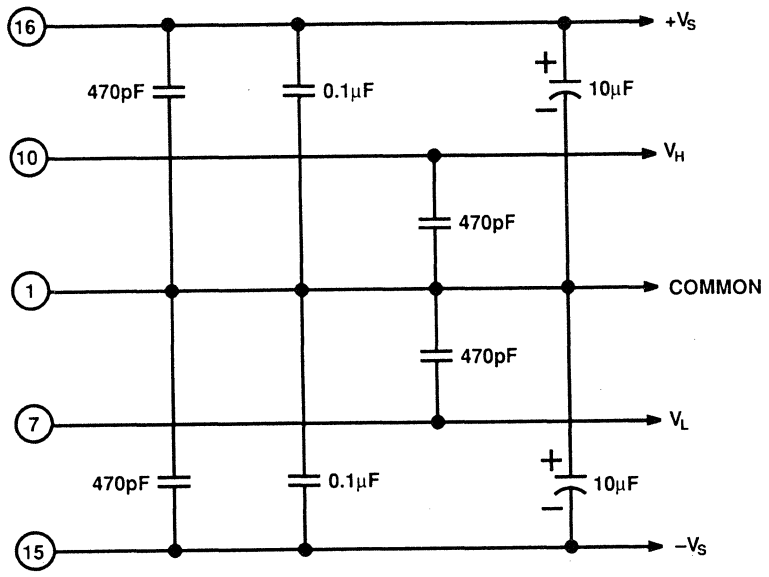


ALLOWABLE CURRENT RANGE FOR I_{OH}, I_{OL} vs. V_{DUT} FOR AD1315

Figure 6.17

Layout Considerations for AD1321/AD1322 Pin Drivers

Good engineering practice to capacitively decouple the power supplies is essential with high speed drivers where dynamic power supply current changes from -100mA to +100mA is required in only a few nanoseconds. A 470pF high frequency decoupling capacitor must be located within 0.25 inches of the +Vs and -Vs terminals to a low impedance ground. A 0.1μF capacitor in parallel with a 10μF tantalum capacitor should also be situated between the power supplies and ground; however, proximity to the device is less critical. Circuit performance will be similarly enhanced and noise minimized by locating a 470pF capacitor as close to V_H and V_L and connected to ground. Bypass considerations have been summarized in Figure 6.18.



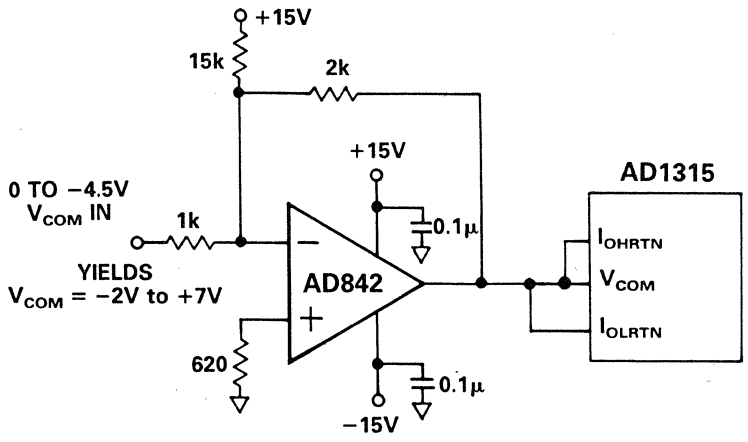
DECOUPLING CIRCUIT FOR AD1321/AD1322

Figure 6.18

Layout Considerations for AD1315 Active Load

I_{OHRTN} and I_{OLRTN} may be connected to any potential between -2V and +7V. These return points must be able to source or sink 50 mA, since the I_{OH} and I_{OL} programmed currents are diverted here in the inhibit mode. The RTNs may be connected to a suitable GND. However, to keep transient ground currents to a minimum, they are typically tied to the V_{COM} programming voltage point.

The V_{COM} input sets the commutation voltage of the active load. With DUT output voltage above V_{COM}, the load will sink current (I_{OH}). With DUT output voltage below V_{COM}, the load will source current (I_{OL}). Like the I_{OH} and I_{OL} return lines, the V_{COM} must be able to sink or source 50 mA; therefore a standard op amp will not suffice. An op amp with an external complementary output stage or a high power op amp such as the AD842 will work well here. A typical application is shown in Figure 6.19.



SUGGESTED I_{OHRTN}, I_{OLRTN}, V_{COM} HOOKUP

Figure 6.19

SECTION VII

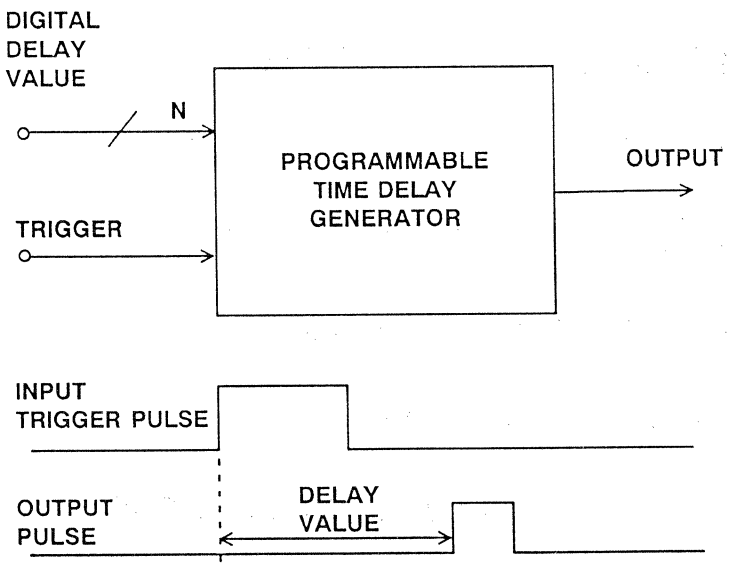
TIME DOMAIN FUNCTIONS: TIME DELAY GENERATORS

TIME DOMAIN FUNCTIONS: TIME DELAY GENERATORS

PROGRAMMABLE TIME DELAY GENERATION TECHNIQUES

There are numerous applications where it is desired to generate precise time delays under computer control as shown in Figure 7.1. A primary example is multiple channel deskewing in ATE systems. High pin count logic testers may have over one-hundred line drivers whose outputs must be routed to a remote testhead. Subnanosecond delay matching at the testhead is required for accurate delay measurements to be made on high speed ECL logic. Other applications for programmable delay generators are in pulse generators, timing circuits, multiple phase clock generators and arbitrary waveform generators.

High speed counters are often used to generate controlled delays but are not practical where subnanosecond resolution is required. Passive tapped delay lines offer precision but have limited resolution and delays can only be changed by switching taps. Hybrid delay lines (see Figure 7.3) which are a combination of passive and active elements offer digitally controlled step sizes of 100ps and fullscale delays of up to 20ns but are expensive and typically have high power dissipation (1 watt) thereby making them unsuitable for large volume high density applications.



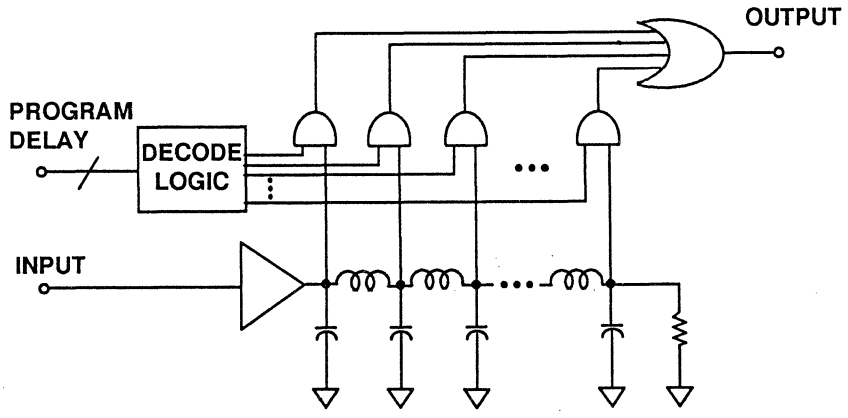
PROGRAMMABLE TIME DELAY GENERATOR

Figure 7.1

PROGRAMMABLE DELAY GENERATION

- High Speed Counters
  - 100ps Resolution Required 10 GHz Flip-Flop
- Passive Tapped Delay Lines
  - 100ps Resolution
  - Awkward to Switch Delay
- Hybrid Delay Lines
  - On Board Decoding Logic
  - 100ps Resolution
  - High Power
- Ramp/Comparator/DAC
  - 10ps Resolution, 8 BITS
  - Variable Full Scale Delays
  - Low Power, Low Cost IC

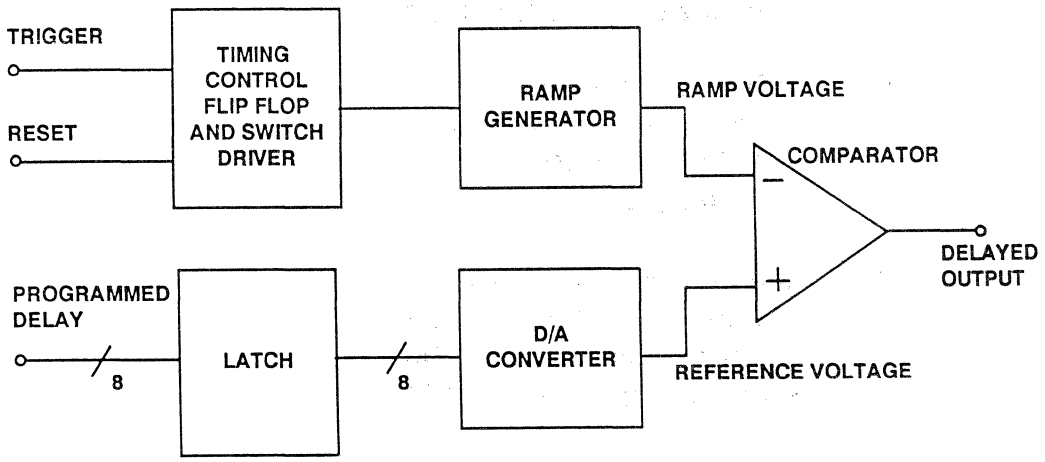
Figure 7.2



PROGRAMMABLE PASSIVE/ACTIVE HYBRID DELAY LINE

Figure 7.3

By far the most flexible approach to generating programmable delays is the ramp/comparator/DAC method shown in Figure 7.4. Upon the receipt of a trigger pulse, the ramp voltage generator is started. When the ramp voltage crosses the comparator threshold set by the DAC, the comparator output goes high, thereby generating a pulse edge which is delayed from the trigger pulse edge by an amount of time proportional to the DAC binary input. This approach to digital-to-time conversion (DTC) is not new, but recent advances in design and process techniques allow this function to be implemented in a single monolithic IC which offers not only precision but low power and cost.

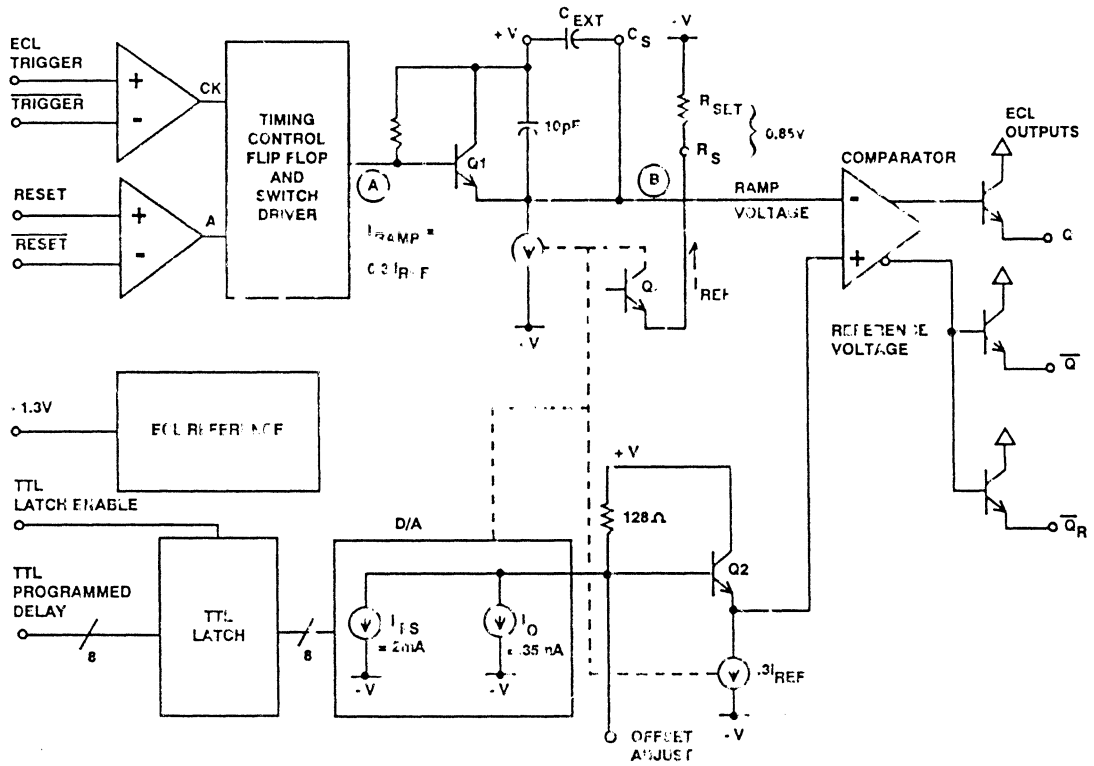


RAMP/COMPARATOR/DAC DELAY GENERATOR

Figure 7.4

AD9500 PROGRAMMABLE DELAY GENERATOR

A block diagram of the AD9500 DTC is shown in Figure 7.5. A positive going differential ECL pulse edge between the TRIGGER and the $\overline{\text{TRIGGER}}$ input causes the timing control flip flop and switch driver to force the base of Q1 negative, thereby causing the precision current source ($0.3I_{REF}$) to charge the capacitance ($10pF||C_{EXT}$) and creating a linear negative-going ramp voltage at Point B (the negative input of the comparator). The positive input reference voltage to the comparator is set by the 8-bit D/A converter after buffering by emitter follower Q2. When the ramp voltage crosses the programmed threshold, the Q output goes high while the $\overline{Q}$ and $\overline{Q}_R$ outputs go low. A differential RESET signal resets the timing control flip flop which returns Point A to +V and discharges the capacitance $10pF||C_{EXT}$ through the emitter of Q1. The RESET input is *level sensitive*



AD-9500 BLOCK DIAGRAM

Figure 7.5

and overrides the *edge sensitive* TRIGGER input (exactly like the reset input in a D flip flop). The reference current through Q3 is set by the external R_{SET} resistor with a minimum value of 250 ohms corresponding to I_{REF} = 3.4mA. I_{REF} is scaled to 0.3 I_{REF} which becomes the ramp current as well as the emitter current for Q2. Since Q1 and Q2 operate at the same current, their V_{BE} drops act as a common mode signal to the comparator inputs. The ramp charging current is given by:

$$I_{RAMP} = 0.3\, I_{REF} = 0.3\left(\frac{0.85V}{R_{SET}}\right) = \frac{0.255V}{R_{SET}}.$$

The slope of the ramp voltage becomes:

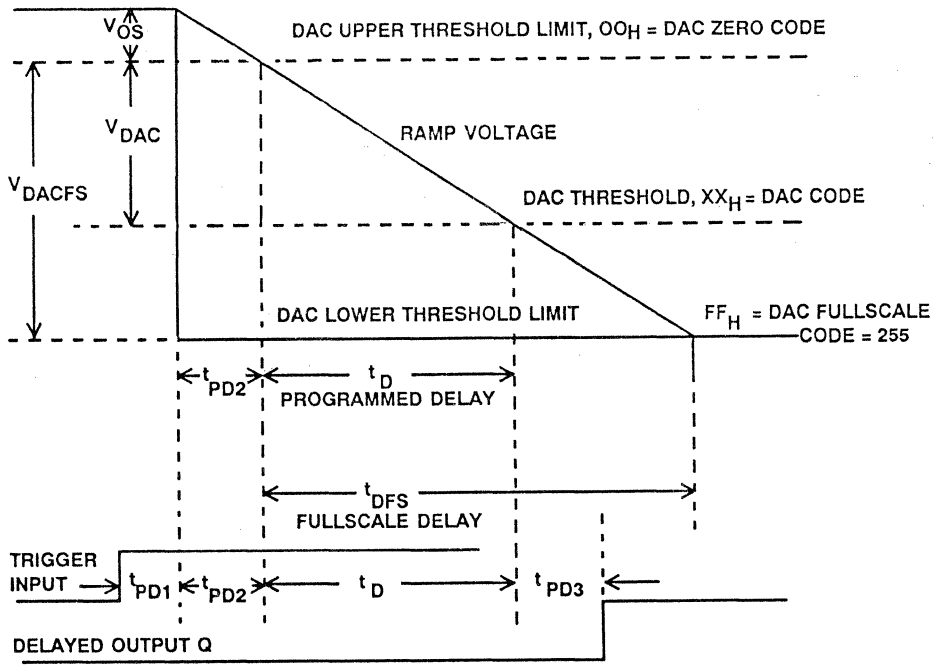
$$\frac{dV}{dt} = \frac{I_{RAMP}}{C_{EXT} + 10pF} = \frac{0.255V}{R_{SET}(C_{EXT} + 10pF)} \simeq \frac{\Delta v}{\Delta t}$$

The details of the ramp voltage and the various timing relationships are shown in Figure 7.6. Note that there is an initial

offset voltage of approximately 45mV across the 128 Ω resistor. This insures that the comparator is always off (Q output 0) at the start of the ramp. The offset also prevents the comparator from false triggering because of the small amount of ringing which occurs on the ramp voltage when it is reset.

The fullscale DAC current is set for 2mA corresponding to a fullscale DAC lower threshold limit (FF_H) of 256mV below the DAC upper threshold limit (OO_H). The DAC current is slaved to the reference current through Q3 to minimize the effects of temperature and device mismatch on the programmed delay t_D.

The programmed delay t_D is the time required for the ramp voltage to pass from the upper threshold limit OO_H to the DAC threshold voltage XX_H. The difference between these two levels is V_{DAC}.



t_{PD1} = INPUT DELAY (CONSTANT)

t_{PD2} = OFFSET DELAY (VARIABLE WITH t_{DFS})

t_{PD3} = OUTPUT DELAY (CONSTANT)

$t_{PD} = t_{PD1} + t_{PD2} + t_{PD3}$ = MINIMUM PROP. DELAY

TOTAL DELAY = $t_{PD} + t_D$

RAMP/TIMING RELATIONSHIPS

Figure 7.6

The previous equation can be rewritten:

$$\Delta v = \frac{0.255V \bullet R_{SET}\,(C_{EXT} + 10pF)}{\Delta v}.$$

The fullscale programmed delay t_{DFS} occurs when

$\Delta v = 256mV,$

$t_{DFS} = R_{SET}\,(C_{EXT} + 10pF).$

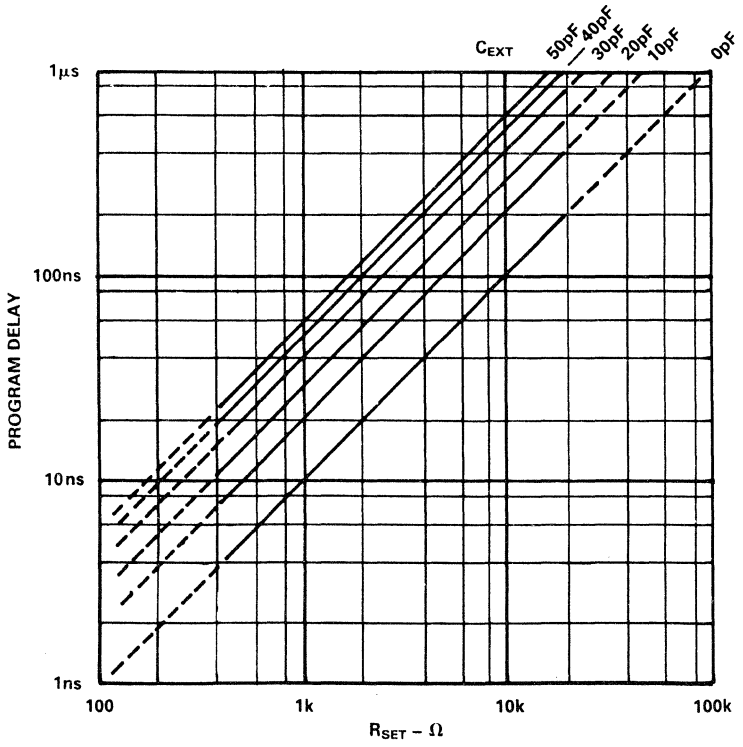
The graph of this function is shown in Figure 7.7. The program delay t_D can be written as

$$t_D = \frac{V_{DAC}}{V_{DACFS}} \bullet t_{DFS} = \frac{XX_H}{FF_H} \bullet R_{SET}\,(C_{EXT} + 10pF).$$

The total delay through the AD9500 is the sum of the minimum propagation delay t_{PD} and the programmed delay t_D. The minimum propagation delay t_{PD} is made up of the fixed input delay t_{PD1}, the offset delay t_{PD2}, and the fixed output delay t_{PD3}. Note that the offset delay t_{PD2} is a function of the fullscale delay and is given by:

$$t_{PD2} = t_{DFS} \bullet \frac{V_{OS}}{V_{DACFS}} =$$

$$\frac{V_{OS}}{V_{DACFS}} \bullet R_{SET}\,(C_{EXT} + 10pF)$$



TYPICAL PROGRAMMED DELAY RANGES

Figure 7.7

The minimum propagation delay t_{PD} becomes:

$$t_{PD} = t_{PD1} + t_{PD3} + t_{PD2}$$

$$t_{PD} = t_{PD1} + t_{PD3} + \frac{V_{OS}}{V_{DACFS}} \cdot R_{SET}\,(C_{EXT}+10pF)$$

The total delay then becomes:

$$\text{TOTAL DELAY} = t_{PD} + t_D$$

$$= t_{PD1} + t_{PD3} + \frac{V_{OS}}{V_{DACFS}} \cdot R_{SET}\,(C_{EXT}+10pF) + \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT}+10pF).$$

In the AD9500, $t_{PD1} + t_{PD3} = 4ns$,
$V_{OS} = 45mV$
$V_{DACFS} = 256mV$.

$$\text{TOTAL DELAY} = t_{PD} + t_D$$

$$= 4ns + \frac{45}{256} \cdot R_{SET}\,(C_{EXT} + 10pF) + \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT} + 10pF)$$

$$= 4ns + 0.18\,R_{SET}\,(C_{EXT} + 10pF) + \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT} + 10pF).$$

MINIMUM PROP. DELAY = t_{PD}

$$t_{PD} = 4ns + 0.18\,R_{SET}\,(C_{EXT} + 10pF)$$

PROGRAMMED DELAY = t_D

$$t_D = \frac{XX_H}{FF_H} \cdot R_{SET}\,(C_{EXT}+10pF).$$

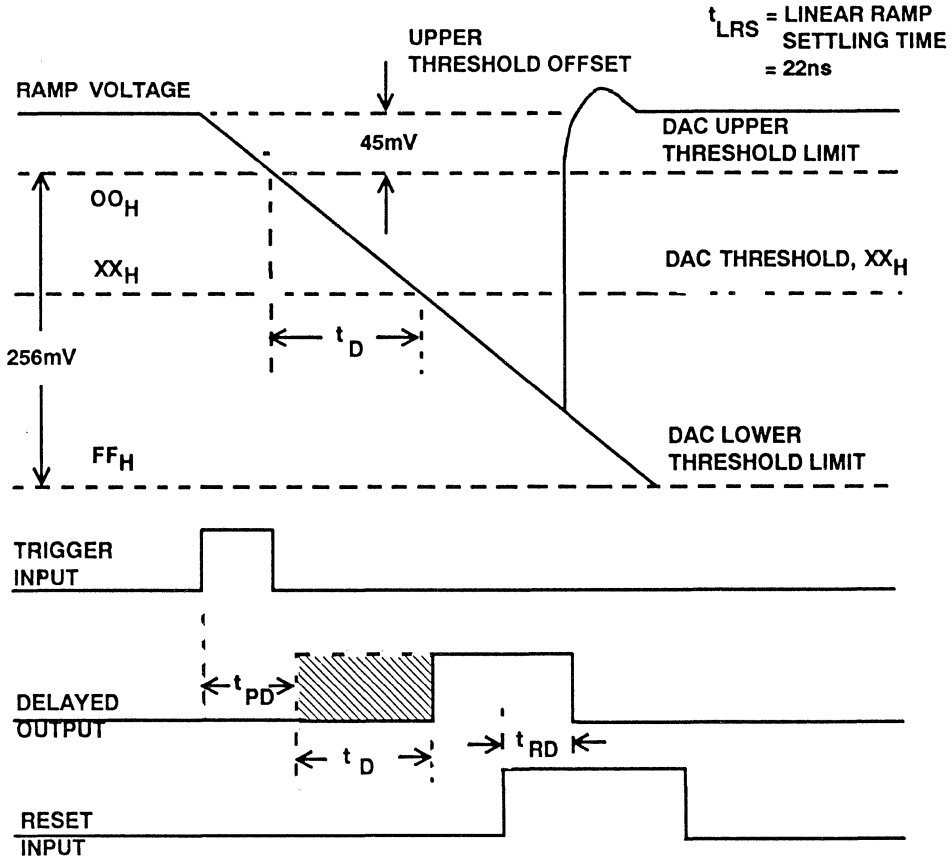
Another important AD9500 specification is the reset propagation delay t_{RD} which is the time from the leading edge of the RESET pulse input until the delayed output Q returns to a logic "0". This requires that the ramp voltage cross the upper threshold limit and thereby return the comparator to its initial state. The timing relationships are shown in Figure 7.8. Note that the time required for the linear ramp voltage to settle after reset t_{LRS} is typically 22ns.

The input latch is designed to accept an 8-bit TTL program delay input and has a TTL latch enable function. When the LATCH ENABLE is a logic "0" the input data is passed to the DAC. A logic "1" freezes the data in the latch.

Key specifications for the AD9500 are summarized in Figure 7.9 along with a simplified functional block diagram.

Further details of the operation of the circuits within the AD9500 can be found in the following United States Patent:

Patent #4742331
Date of patent: May 3, 1988
Inventors: Jeffrey G. Barrow
Adrian P. Brokaw
Assignee: Analog Devices, Inc.
Norwood, MA



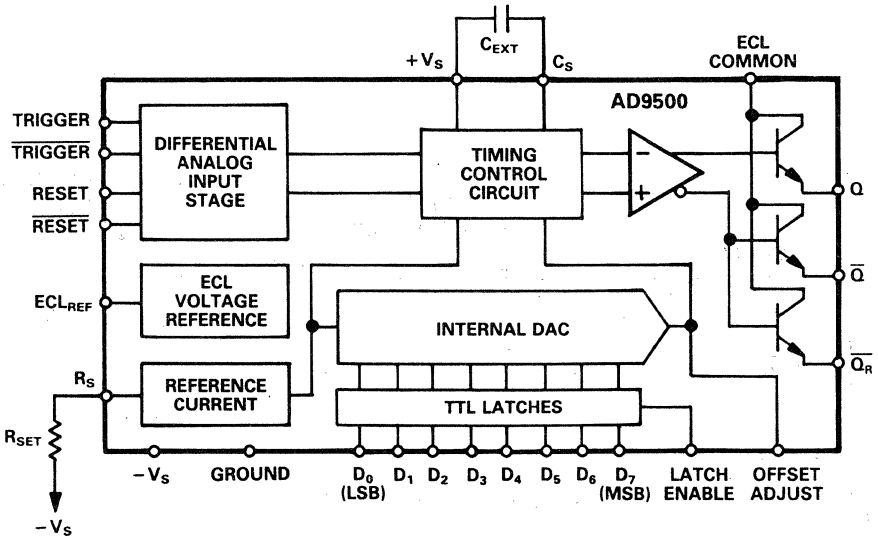
t_{PD} = MINIMUM PROPAGATION DELAY

t_D = PROGRAMMED DELAY

t_{RD} = RESET PROPAGATION DELAY

AD-9500 TIMING RELATIONSHIPS

Figure 7.8



- 2.5ns TO 100 μs+FULLSCALE RANGE
- 10ps DELAY RESOLUTION
- 8-BIT TTL INTERNAL LATCH AND DAC
- LOW POWER DISSIPATION - 310mW

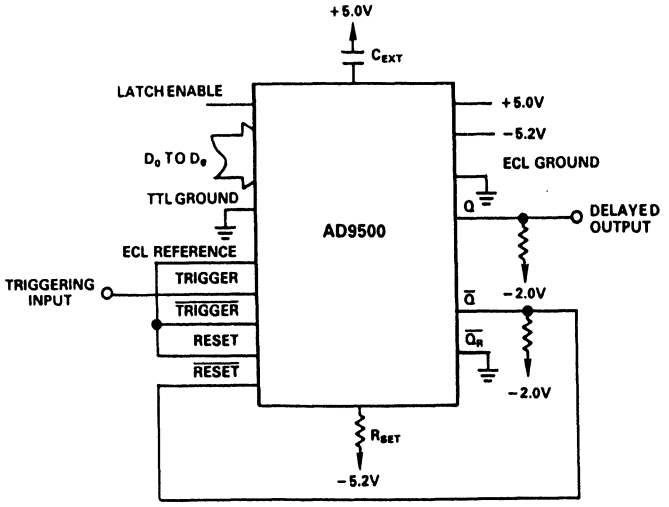
AD-9500 KEY SPECIFICATIONS

Figure 7.9

AD9500 MINIMUM OUTPUT PULSE WIDTH CONFIGURATION

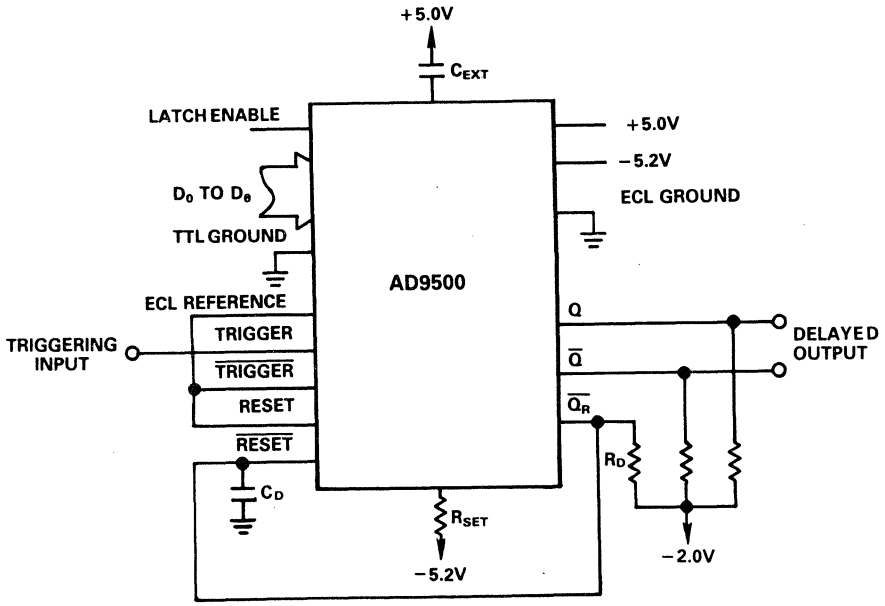
Figure 7.10 shows the AD9500 configured for minimum output pulse width. Only one of the TRIGGER inputs is used. The other is connected to the ECL reference midpoint, ECL_{REF}. This allows the AD9500 to be triggered with standard 10K or 10KH single-ended ECL signals. Improved noise margin, temperature tracking, and common mode noise rejection are obtained, however, if the TRIGGER and $\overline{\text{TRIGGER}}$ inputs are driven differentially.

Once the triggering event occurs, the Q output will go to a logic 1 state after the total delay interval has passed. The $\overline{Q}$ output is then used to drive the RESET input, causing the AD9500 to reset itself. The result is a delayed output pulse which is only as wide as the reset propagation delay ($t_{RD} \simeq 5$ns).



AD-9500 MINIMUM OUTPUT PULSE WIDTH CONFIGURATION

Figure 7.10



RESET TIME = t_{RD} + 0.54R_DC_D

$R_D \geq 300\Omega$

NOTE: IF R_D RETURNED TO -5.2V,

RESET TIME = t_{RD} + 0.12R_DC_D,

$R_D \geq 1000\Omega$

AD-9500 EXTENDED OUTPUT PULSE WIDTH CONFIGURATION

Figure 7.11

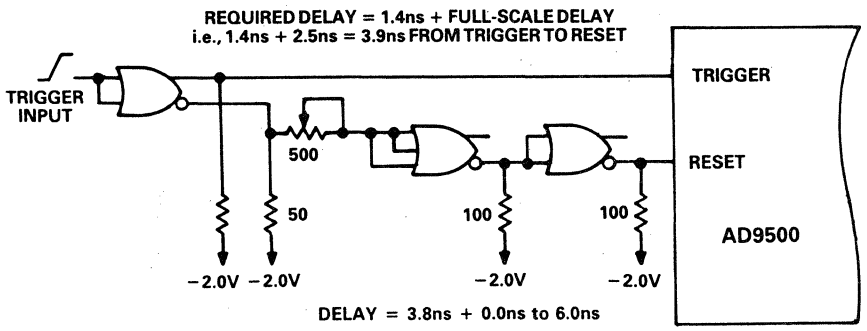
7

AD9500 CONFIGURED FOR EXTENDED OUTPUT PULSE WIDTHS

The extended output pulse configuration shown in Figure 7.11 is similar to the minimum configuration except that the output pulse width is extended. The $\overline{Q_R}$ output is used to drive the RESET input through a resistor/capacitor charging network. The charging network causes the signal at the RESET input to fall more slowly thereby extending the output pulse width. The appropriate values for R_D and C_D are determined using the equations in Figure 7.11.

AD9500 CONFIGURED FOR HIGH SPEED TRIGGERING

The AD9500 can be triggered at rates above 100 MHz. This is accomplished by resetting the AD9500 shortly after it is triggered, which also tends to generate an extremely narrow output pulse. The delay circuit shown in Figure 7.12 between the TRIGGER input and the RESET input provides the variable delay required for various configurations from 2.5ns fullscale to over 10ns fullscale (greater than 10ns total delay precludes 100 MHz triggering).



AD-9500 CONFIGURED FOR HIGH SPEED TRIGGERING

Figure 7.12

MULTIPLE PATH DESKEWING

High speed electronic systems with parallel signal paths require that close delay matching be maintained. If delay mismatch (or skew) occurs, errors can be made in transfer of data. Therefore, delays are matched, usually by carefully matching lead lengths.

High-speed, high-pin-count testers must maintain close matching under different circuit conditions to test different device types. In these cases, matching of lead length is not sufficient to maintain matching to the required subnanosecond tolerance. A calibration cycle is typically included in the changeover from one device to another. During the calibration cycle, a single stimulus pulse is applied to each input of the circuit shown in Figure 7.13.

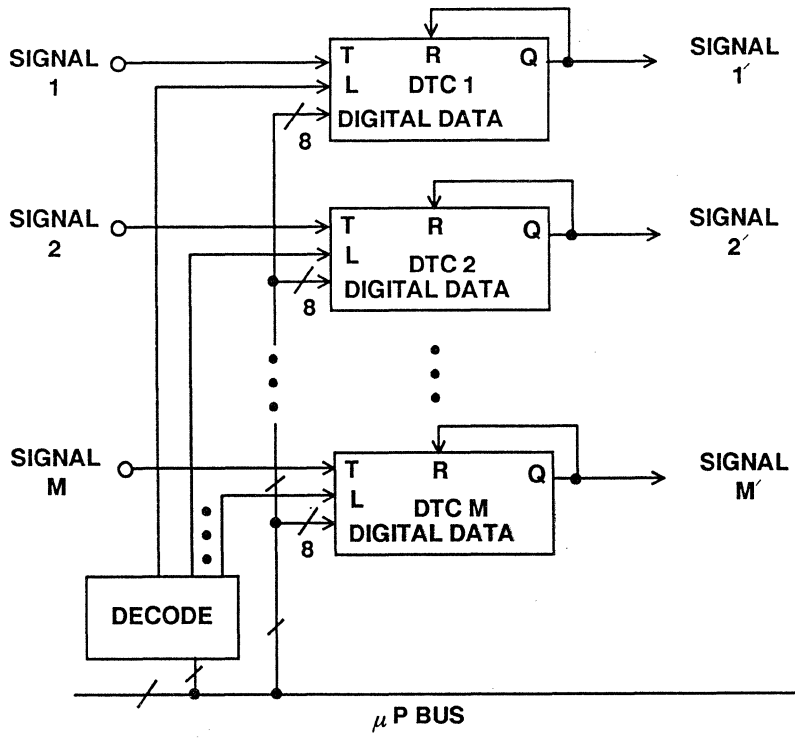
The delay of each signal path is then measured by the tester delay measurement circuitry. Using a closed-loop technique, each delay is equalized by changing the digital value held in the register of the DTC. Once the delays are matched to the desired tolerance, the calibration loop is opened, and the tester is ready to test.

Delay for each DTC can be calculated with the equations:

$$T_{DTC} = t_{DTC} + t_{pd}$$

when:

$$t_{DTC} = (XX_H/FF_H) * RC$$



MULTIPLE PATH DESKEWING

Figure 7.13

where:

T_{DTC} is total delay through the DTC.
t_{DTC} is the programmed delay.
t_{pd} is the prop delay with zero programmed delay.
XX_H is the 8-bit digital input.
FF_H is full-scale digital input.
R is in ohms.
C is in farads.

PROGRAMMABLE PULSE GENERATOR

In this application, (see Figure 7.14), two DTCs are triggered from a common clock signal. Their outputs go to the inputs of an RS flip-flop. A digital delay value is latched into each DTC with DTC #2 typically having a greater value than DTC #1.

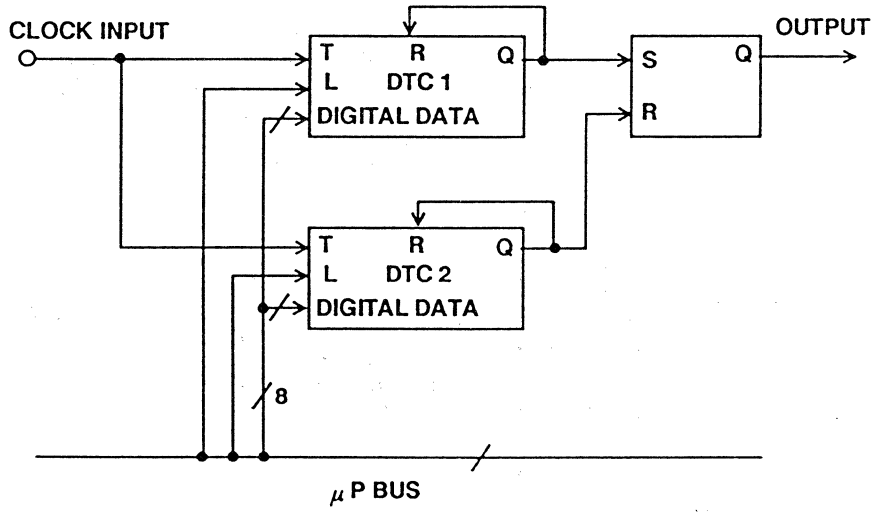
Changing the delay value from one clock cycle to the next generates a pseudo-random pulse whose leading and trailing edge delays are controlled relative to Clock In.

The frequency and pulse width of the pulse generator can be determined as follows:

$$f = f_{CLOCK\ IN}$$

and:

$$t_{pw} = t_{DTC2} - t_{DTC1}$$



PROGRAMMABLE PULSE GENERATOR

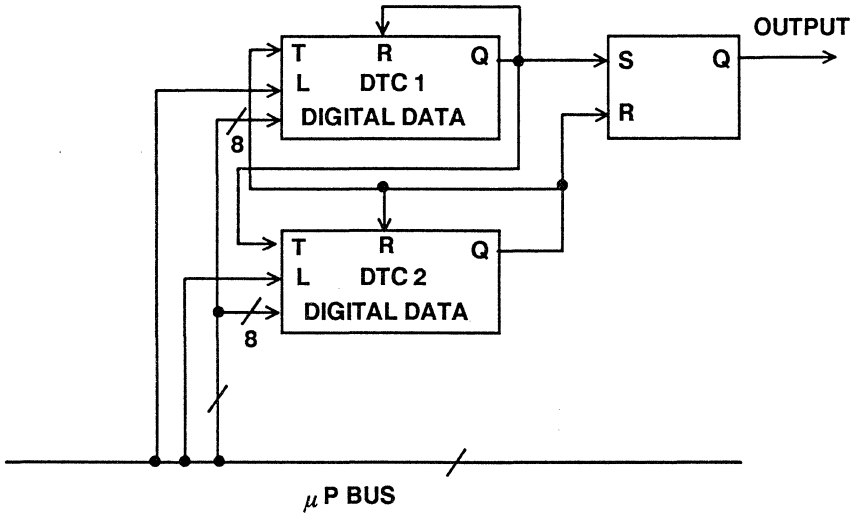
Figure 7.14

PROGRAMMABLE OSCILLATOR

Two DTCs are configured as an astable oscillator as shown in Figure 7.15. Delay through each side of the oscillator is determined by the value held in the DTCs register, plus the fixed propagation delay of each DTC. Increasing the digital value decreases frequency, just as increasing RC decreases frequency in a traditional oscillator. Frequency and duty cycle are both controllable.

Frequency can be found by the equation:

$$f = 1/(2t_{pd} + t_{DTC1} + t_{DTC2}).$$



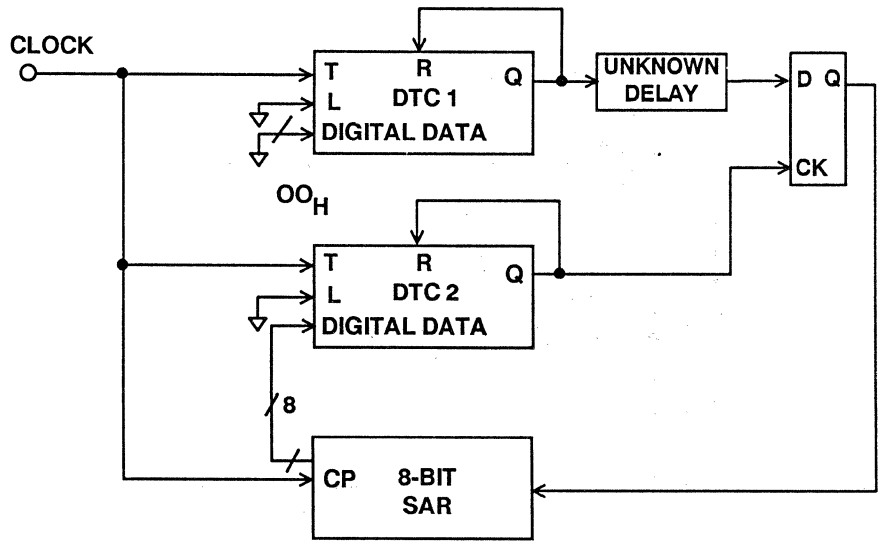
PROGRAMMABLE OSCILLATOR

Figure 7.15

DIGITAL DELAY DETECTOR

An unknown digital delay can be measured by applying a repetitive clock to the circuit shown in Figure 7.16. DTC #1 is set to zero delay. Like a successive approximation ADC, this delay detector requires 8 cycles of the clock to determine the value of the unknown delay.

Since, in reality, there are non-ideal characteristics in the circuits which are shown, the value of DTC #1 should be adjusted with zero delay substituted for the unknown delay; this will compensate for set-up time of the flip-flop, stray delays, etc.



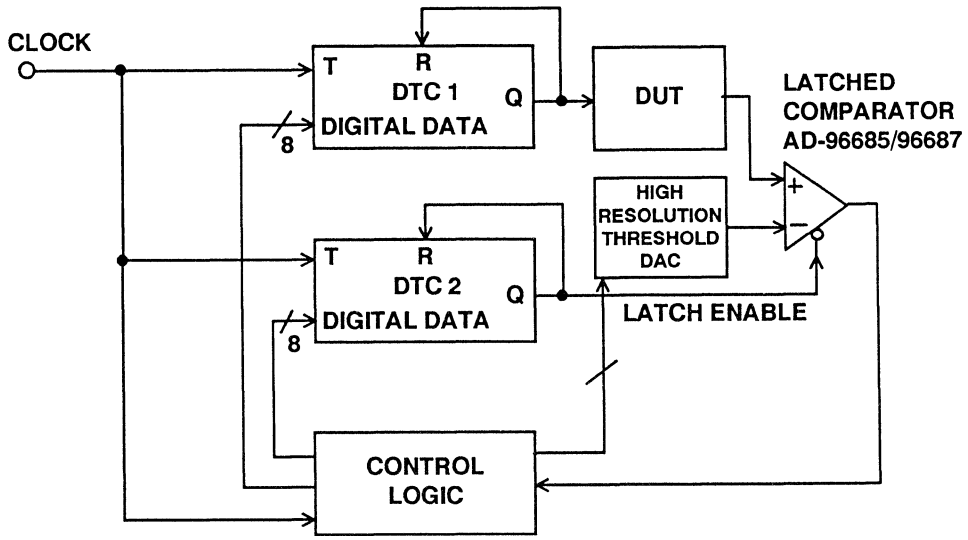
MEASURING UNKNOWN DELAYS

Figure 7.16

DIGITIZING AC WAVEFORMS

The circuit shown in Figure 7.17 can be used to measure the time profile of high-speed waveforms. The DAC sets a threshold level which drives one of the differential comparator inputs. The other comparator input is driven by the device under test (DUT). The output of the first AD9500 causes the DUT to produce an output. The second AD9500, which is also triggered along with the first AD9500, strobes the comparator latch enable.

If the DUT output is greater than the DAC threshold when the comparator is latched, the comparator output will be a logic 1. If the output is below the DAC threshold, the comparator will be a logic 0. The programmed delay setting of the second AD9500 is adjusted to the point where the DUT output equals the DAC threshold. By varying the DAC threshold level and adjusting the second AD9500 programmed delay, a point by point reconstruction of the AC waveform can be created.



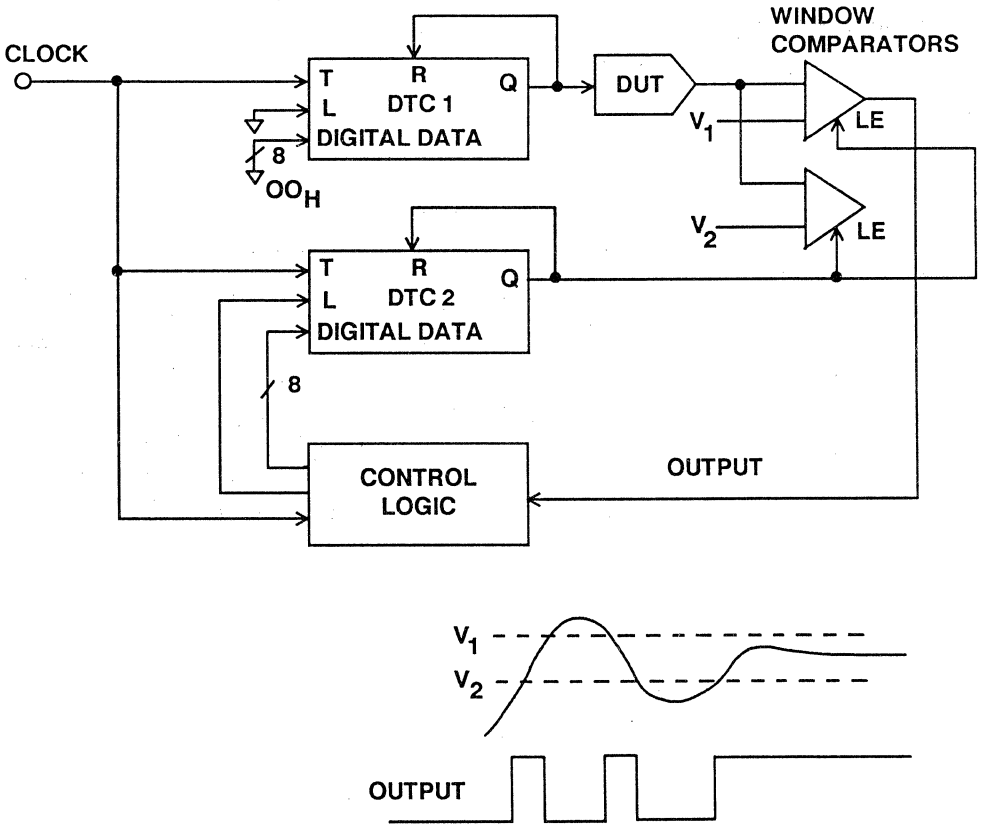
MEASURING AC WAVEFORMS

Figure 7.17

MEASURING ANALOG SETTLING TIME

This circuit as shown in Figure 7.18 functions in a manner similar to the digital delay detector circuit of Figure 7.16. The clock must be repetitive; and DTC #1 is used to cancel prop delay of DTC #2, set-up time of the comparators, stray delays, etc. The difference is in the detection method. The register is replaced by a window comparator.

Timing for this circuit operates by starting at fullscale (after the DUT has settled) and decrementing the latch strobe delay. The output of the detector will be high as long as the signal is within the limits set by V_1 and V_2.



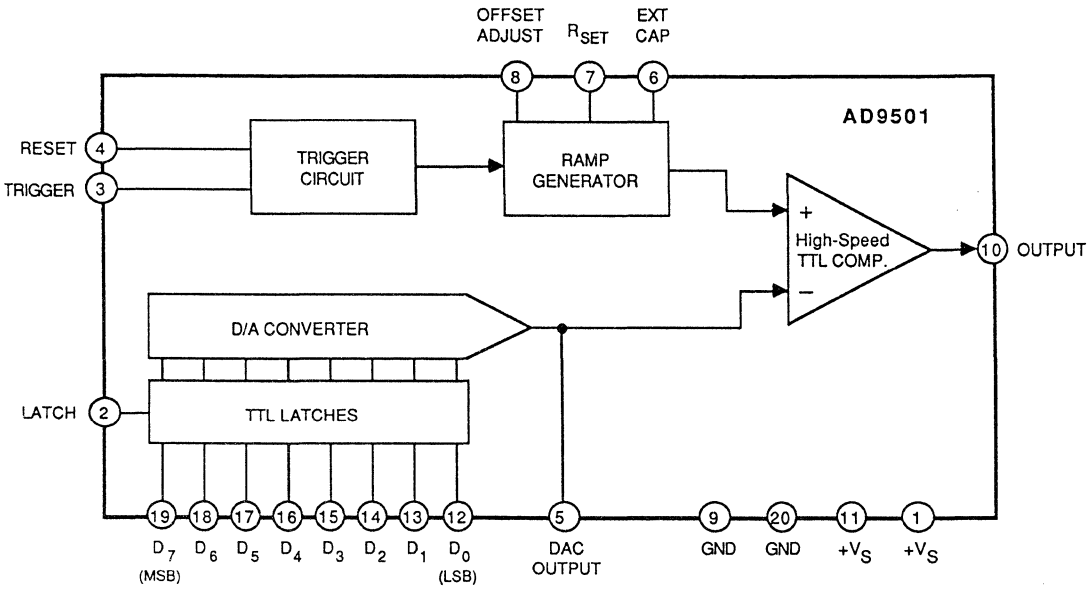
ANALOG SETTLING TIME MEASUREMENT

Figure 7.18

AD-9501: TTL COMPATIBLE PROGRAMMABLE DELAY GENERATOR

The AD-9501 is a fully TTL compatible version of the AD-9500, operating off a single +5V power supply. The principles of operation are similar to the AD-9500.

A block diagram along with key specifications for the AD-9501 are shown in Figure 7.19



AD9501 Functional Block Diagram

- 2.5 ns TO 10μs FULLSCALE RANGE
- 10 ps DELAY RESOLUTION
- TTL AND CMOS COMPATIBLE
- SINGLE +5V SUPPLY
- LOW POWER DISTRIBUTION: 415 mW

AD-9501 KEY SPECIFICATIONS

Figure 7.19

SECTION VIII

FREQUENCY DOMAIN FUNCTIONS: PHASE LOCKED LOOPS

FREQUENCY DOMAIN FUNCTIONS: PHASE LOCKED LOOPS

BASIC PHASE LOCKED LOOP

PHASE DETECTORS:
Double Balanced Mixer, Digital Phase/Frequency Detector

PHASE DETECTION USING THE AD9901 PHASE/FREQUENCY DISCRIMINATOR

PLL MATHEMATICS AND DESIGN BASICS

USING THE AD9901 IN A PLL

USE OF DUAL MODULUS PRESCALERS

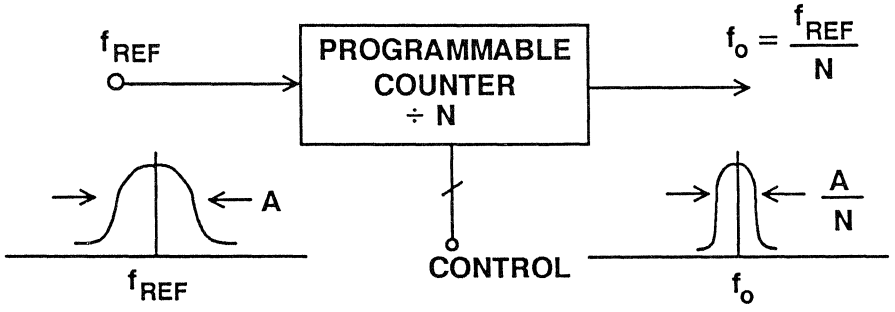
BASIC PHASE-LOCKED LOOP

High purity reference frequencies are key elements in communications equipment, radar systems, and instrumentation. Crystal oscillators followed by suitable filtering provide signals which have excellent stability and purity coupled with very low phase noise. Unfortunately, this requires one crystal oscillator per frequency, and hence this approach soon becomes expensive and bulky.

Frequency division is one technique commonly used to generate frequencies which are less than or equal to a single reference frequency. Prescalers, counters, and dual modulus type digital circuits are all in common use and available in silicon ICs. Galium arsenide digital circuits operate at frequencies up to about 2 GHz. High speed prescalers can be used ahead of conventional silicon circuits to provide cost effective solutions to high speed frequency division.

Digital frequency dividers are often treated as "noise-less" devices since the phase noise in the reference source is almost always greater than that of the divider itself.

Frequency dividers reduce the reference frequency in proportional steps, 1/2, 1/3, 1/4, 1/N. They also tend to proportionally compress the phase spectra as shown in Figure 8.1.

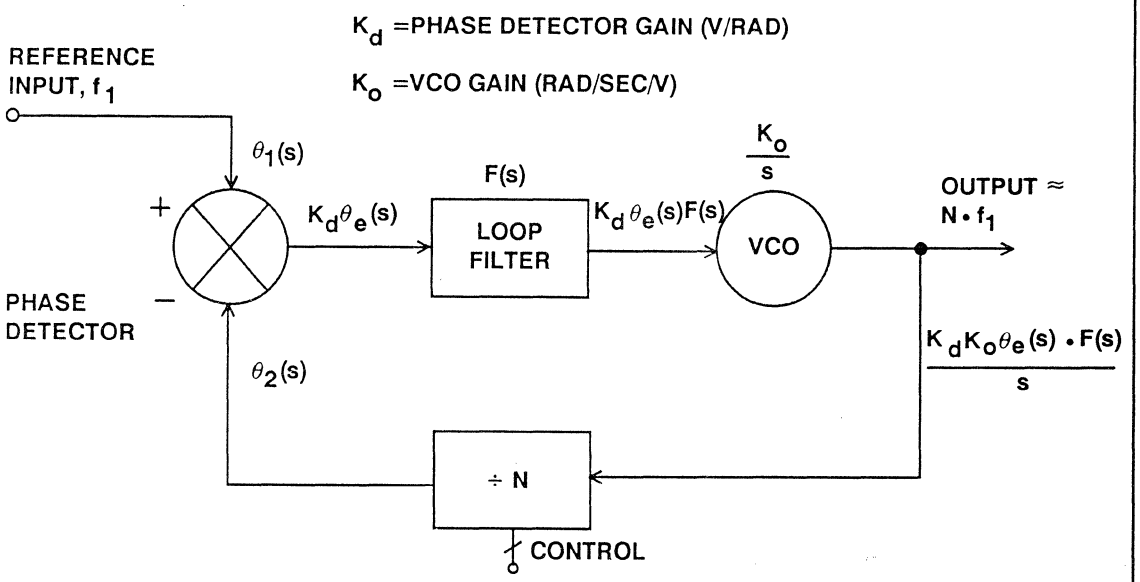


PROGRAMMABLE FREQUENCY DIVISION

Figure 8.1

The phase locked loop (PLL) as shown in Figure 8.2 makes use of a programmable frequency divider in the feedback loop to produce an output frequency which is a multiple of the input frequency. The basic elements of a PLL are the reference input source, loop filter, voltage controlled oscillator (VCO), digital divider, and the phase detector. Each element has a transfer function which can be expressed using Laplace transforms. The basic PLL is analyzed using standard feedback control theory as will be discussed later in this section.

In the most basic PLL, the divided VCO signal is compared to a reference frequency in the phase detector to generate an error signal which will retune the VCO so as to track the reference signal. Since the phase detector is really a multiplier, it produces a sum frequency component as well as a difference component. The loop filter eliminates the sum component as well as any out of band interfering signals present at the input. The proper loop filter design for a given PLL application involves a fairly complex series of tradeoffs and is the subject of much of the material contained in the recommended references at the end of this section. An elementary treatment of loop filter design is contained in this section.



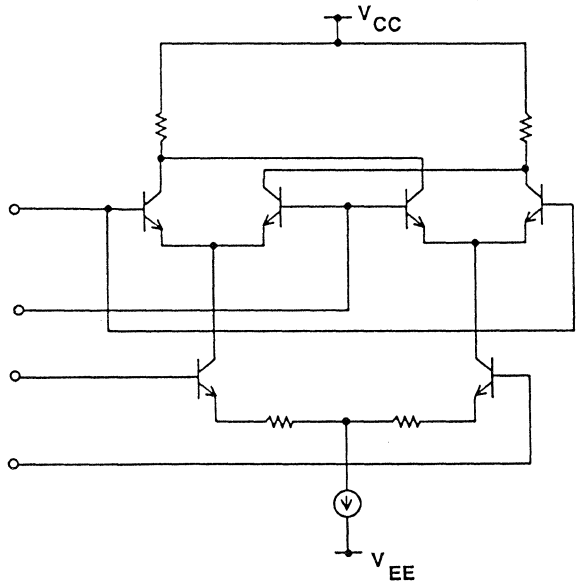
BASIC PHASE LOCKED LOOP

Figure 8.2

PHASE DETECTORS

The purpose of the phase detector is to generate an error signal which is used to retune the oscillator should its output deviate from the reference input signal. The two most common phase detector implementations are the analog mixer and a family of sequential logic circuits known as digital phase detectors.

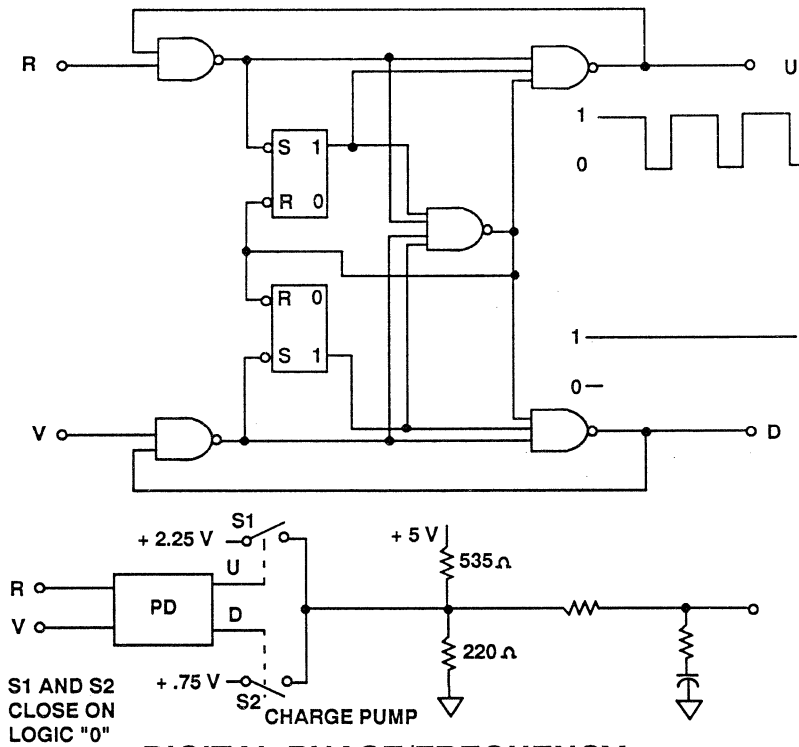
The phase detector is basically a double balanced analog mixer which has good noise rejection and phase response. A typical circuit implementation is shown in Figure 8.3. The phase detector has several important limitations when used in PLL applications. First, large steps in the loop frequency may cause the PLL to unlock and not regain lock. Second, the PLL may never achieve lock upon power up if the VCOs free running frequency is far enough away from PLLs operating frequency. Third, the PLL may lock on a harmonic of the VCO frequency.



DOUBLE BALANCED MIXER/PHASE DETECTOR
Figure 8.3

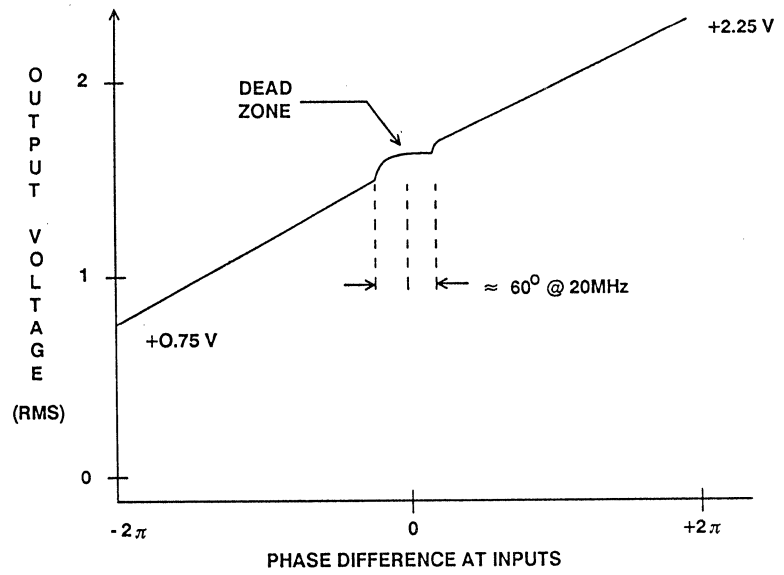
The digital phase/frequency detector circuit shown in Figure 8.4 solves many of the problems associated with the analog phase detector. The digital phase/frequency detector first pulls the VCO frequency close to the reference frequency. At this point, phase acquisition takes over and phase lock is achieved. This type of phase/frequency detector circuit has been implemented in IC form, such as the Motorola MC-4044, but also suffers from several limitations. Loop lockup occurs when all the negative transitions on R (the reference input) and V (the feedback input) coincide. Under these conditions both outputs U and D remain high. Unfortunately, this results in a so-called "dead zone" at phase lock which results in an increase in phase noise. When the input phases are differ-

ent, one output pulses, while the other output is locked low. The average value of the pulsating output waveform is proportional to the phase difference between the two inputs. This implies that the phase detector outputs must either drive a charge pump as shown in Figure 8.4 or a differential filter. This is required to convert the noncomplementary differential output to a single ended output suitable for driving the VCO. Figure 8.5 shows a typical phase gain plot for the Motorola MC-4044 when driving its internal charge pump. Although the dead zone at 0° phase difference may be avoided by offsetting the VCO input voltage by an appropriate amount, this results in a decrease in the linear phase detection operating range.



DIGITAL PHASE/FREQUENCY DETECTOR AND CHARGE PUMP

Figure 8.4



PHASE GAIN PLOT FOR DIGITAL PHASE/FREQUENCY DETECTOR AT 20MHz

Figure 8.5

PHASE DETECTION USING THE AD9901 PHASE/ FREQUENCY DISCRIMINATOR

The AD9901 is a digital phase detector. Figure 8.6 shows the straightforward sequential logic design of the AD9901. The main components include four "D" flip-flops, an exclusive-OR gate (XOR), and some combinational output logic. The circuit operates in two distinct modes; as a linear phase detector, and as a frequency discriminator. When the reference and oscillator are very close in frequency, only the phase detection circuit is active. If the two inputs are substantially different in frequency, the frequency discrimination circuit overrides the phase detector portion to drive the oscillator frequency toward the reference frequency.

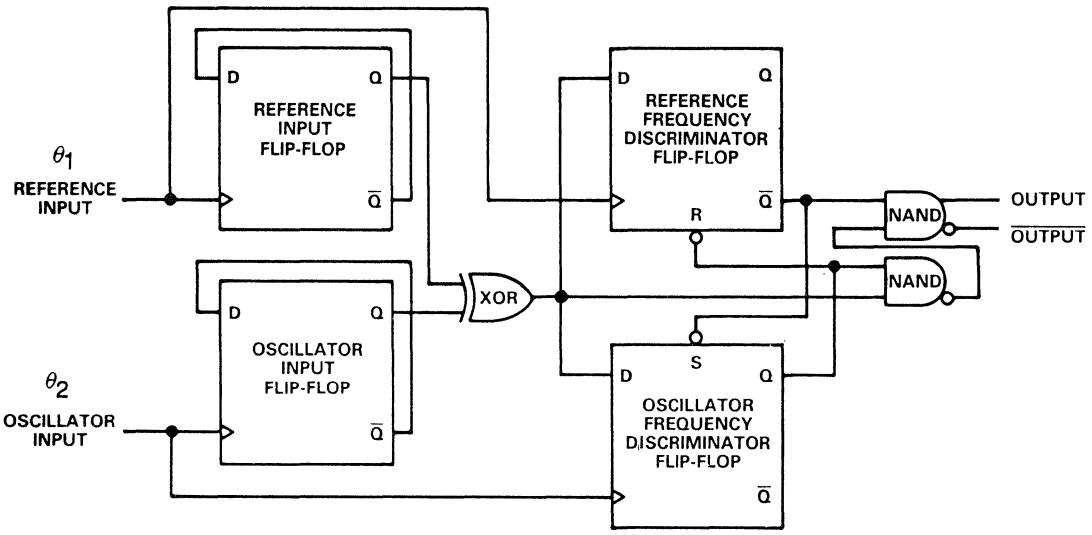
Its input signals are pulse trains, and its output duty cycle is proportional to the phase difference of the oscillator and reference inputs. Figures 8.7, 8.8 and 8.9 illustrate the input-output relationships at lock, with oscillator leading, and oscillator lagging respectively. This output pulse train is low-pass filtered to extract the mean value $K_d(\theta_1 - \theta_2)$, where K_d is a proportionality constant (phase gain).

At or near lock (Figures 8.7, 8.8 and 8.9) only the two input flip-flops and the exclusive-OR gate are active. The input flip-flops divide both reference and oscillator inputs by two. This insures that the inputs to the exclusive-OR are square waves, no matter what the input duty cycles might be. When the two square-waves are combined by the XOR, an output with 50% duty cycle results when the reference and the oscillator inputs are 180° out of phase. Any shift in the phase relationship of the input signals results in

a change in the output duty cycle. Near lock, the frequency discriminator flip-flops provide constant HIGH levels to gate the XOR output to the final output.

Near lock, the duty cycle of the AD9901 is a direct measure of the phase difference between the two input signals. The transfer function can be stated as $[K_d(\theta_1 - \theta_2)]$(V/rad), where K_d is the output voltage range of the AD9901 divided by 2π • (1.8V/2π = .285V/rad). Figure 8.10 shows the relationship of the mean value of the AD9901 output as a function of the phase difference of the two inputs. It is important to note that the slope of the transfer function is constant near its midpoint and does not exhibit the "dead zone" characteristic of other digital phase detectors (see Figure 8.5). The AD9901 avoids this "dead zone" by shifting it off to the endpoints of its transfer curve as indicated in Figure 8.10. The increasing gain at either end increases the effective error signal to pull the oscillator back into the linear region. This does not affect phase noise which is far more dependent upon lock region characteristics. It should be noted, however, that as frequency increases, the linear range is decreased. This effect is caused by the fixed propagation delay through the phase detector. This fixed delay is nominally 3.6 nsec. Therefore, the typical detection range can be found using the following equation:

$$\text{Detection Range} = F \bullet 360^\circ \left[\frac{1}{F} - 3.6\text{ns}\right].$$



AD-9901 PHASE/FREQUENCY DISCRIMINATOR BLOCK DIAGRAM

Figure 8.6

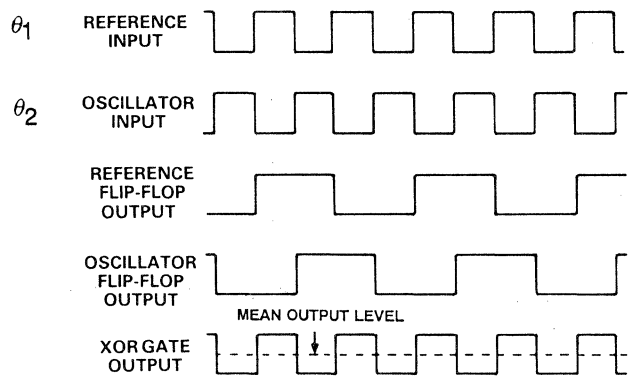
As an example, this yields 100° linear phase detection range for F = 200 MHz.

Away from lock, the AD9901 becomes a frequency discriminator. If the reference frequency and the oscillator frequency are significantly different, the appropriate Discriminator Flip-Flop Output Frequency will be clocked to logic LOW. This overrides the XOR output and holds the output at the appropriate level to pull the oscillator toward the reference frequency. Once the frequencies are within the linear range, the phase detector circuit takes over again. Because the AD9901 combines a frequency discriminator with the phase detector, the possibility of locking to a harmonic of the reference is eliminated.

The AD9901 can operate with ECL inputs when using a single -5.2V supply or TTL/CMOS when using a single +5V supply. A current setting resistor controls the current in the open collector differential pair output stage. The open collector outputs allow flexibility in varying the output voltage swing to match the amplifier and loop filter requirements. A functional circuit diagram of the AD9901 configured for TTL and ECL mode operation is shown in Figure 8.11. In the TTL mode, the output voltage swing is nominally +3.4V to +5V. In the ECL mode, the output voltage swing is nominally -1.8V to 0V. The output stage current is controlled by an external R_{SET} resistor, where $I_{LOAD} = 0.47V/R_{SET}$. Nominally $R_{SET} = 47.5$ ohms and $R_{LOAD} = 182$ ohms will yield an output voltage swing of 1.8Vp-p.

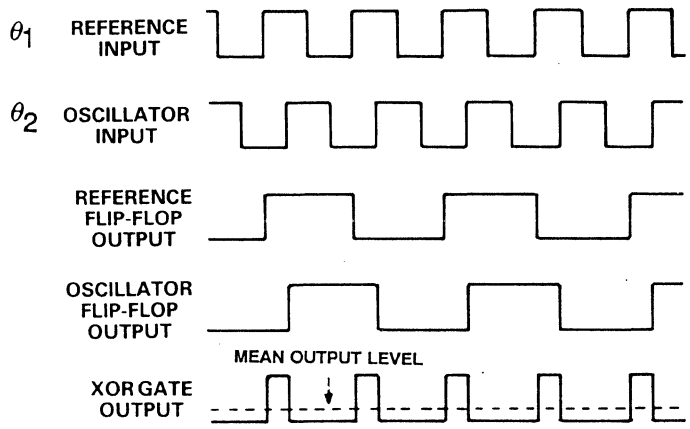
Since the AD9901 has complementary differential outputs, it can be used either single-ended or differentially. The output can be filtered with a passive filter thereby eliminating the need for a high frequency op amp, or the AD9901s output can be used in a fully differential mode.

Another shortcoming of previous phase detectors was the output stability over temperature. This has been eliminated in the AD9901 as has been previously described by the use of an internal bandgap reference in conjunction with external R_{SET} and R_{LOAD} resistors to control the output voltage swing. This gives a stable output voltage swing over temperature thus making a single ended output an alternative to a differential output.



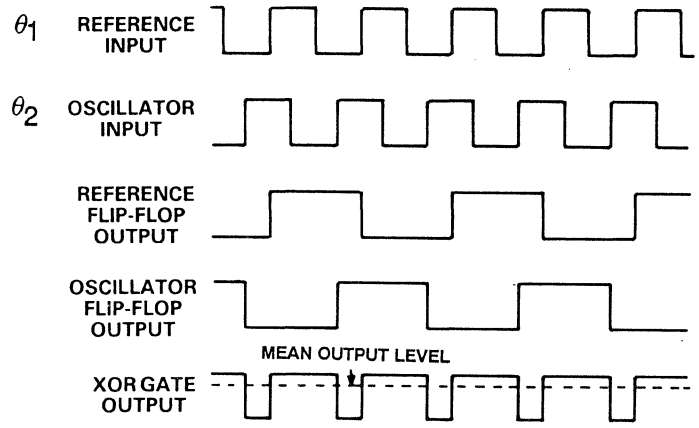
AD-9901 TIMING WAVEFORMS AT "LOCK"

Figure 8.7



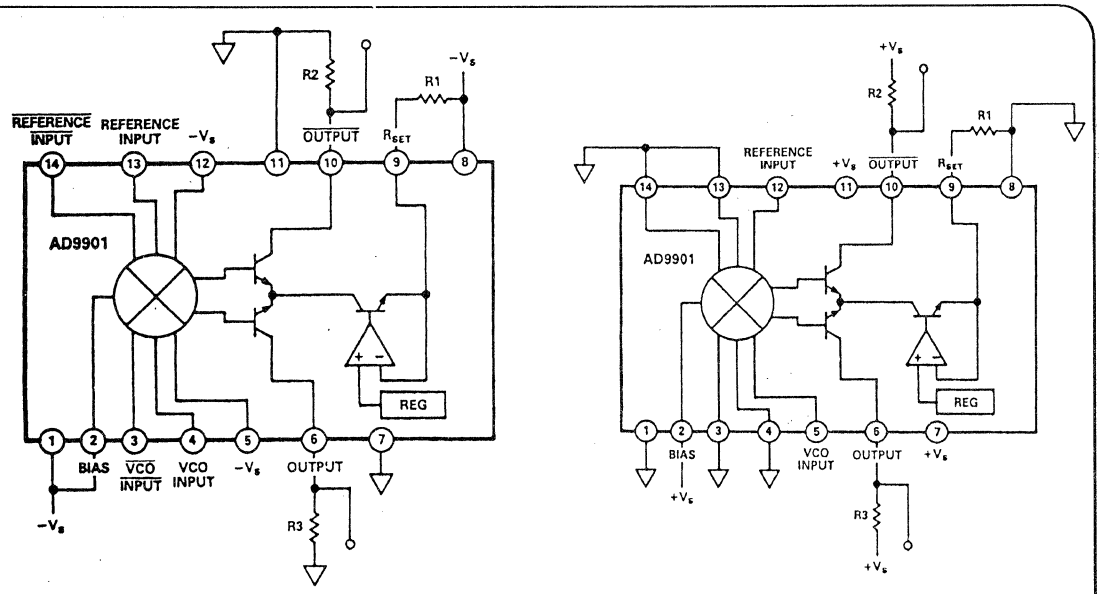
AD-9901 TIMING WAVEFORMS θ_1 LEADS θ_2

Figure 8.8



AD-9901 TIMING WAVEFORMS, θ_1 LAGS θ_2

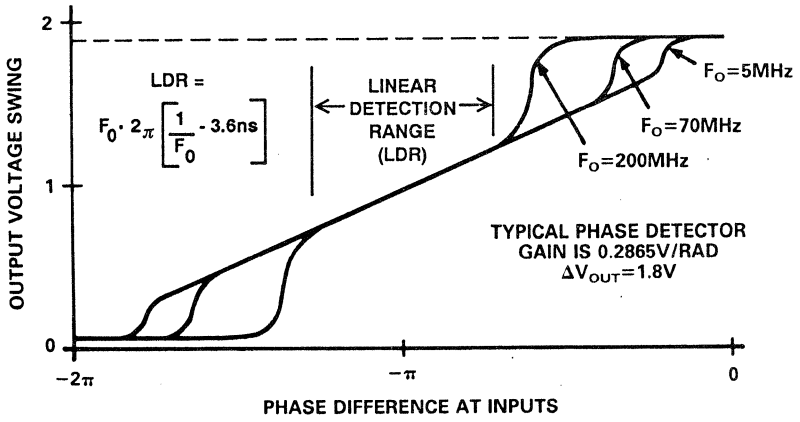
Figure 8.9



ECL MODE TTL MODE

ECL/TTL CONFIGURATIONS FOR AD-9901

Figure 8.10



PHASE GAIN PLOT FOR AD-9901

Figure 8.11

PLL MATHEMATICS AND DESIGN BASICS

PLLs are analyzed using feedback control theory with Laplace transforms used to represent transfer functions of the various elements in the loop. Refer to Figure 8.12 and obtain:

Phase error, $\theta_e(s)$:

$$\theta_e(s) = \theta_1(s) - \theta_2(s) \qquad (1)$$

$$\theta_2(s) = \frac{K_d K_o \cdot \theta_e(s) \cdot F(s)}{Ns} \qquad (2)$$

Combine (1) and (2) and solve for the phase error transfer function, $\frac{\theta_e(s)}{\theta_1(s)}$:

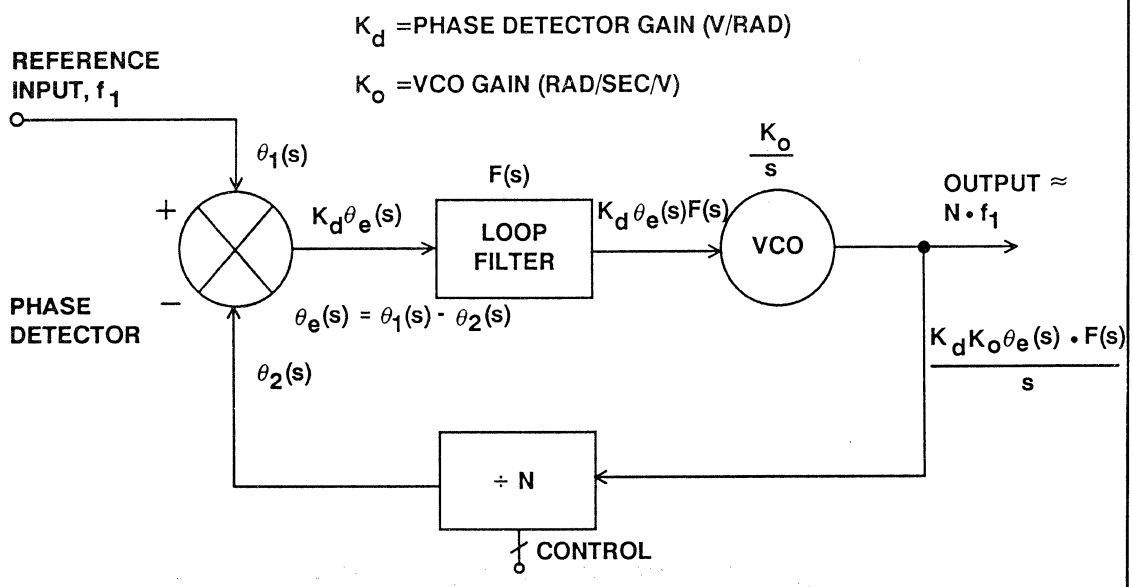
$$H_e(s) = \frac{\theta_e(s)}{\theta_1(s)} = \frac{Ns}{Ns + K_d K_o \cdot F(s)} \qquad (3).$$

Combine (2) and (3) and solve for the phase transfer function, $\frac{\theta_2(s)}{\theta_1(s)}$:

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{K_d K_o F(s)}{Ns + K_d K_o F(s)} \quad , \quad (4)$$

where

K_d = Phase Detector Gain (V/rad)
K_o = VCO Gain (rad/sec/V)
F(s) = Loop Filter Transfer Function
N = Integer Divisor



BASIC PHASE LOCKED LOOP

Figure 8.12

8

From the phase transfer function H(s), it is obvious that the basic loop without a filter is a first order (one pole) system. Let F(s) = 1 (i.e., an all pass filter), and

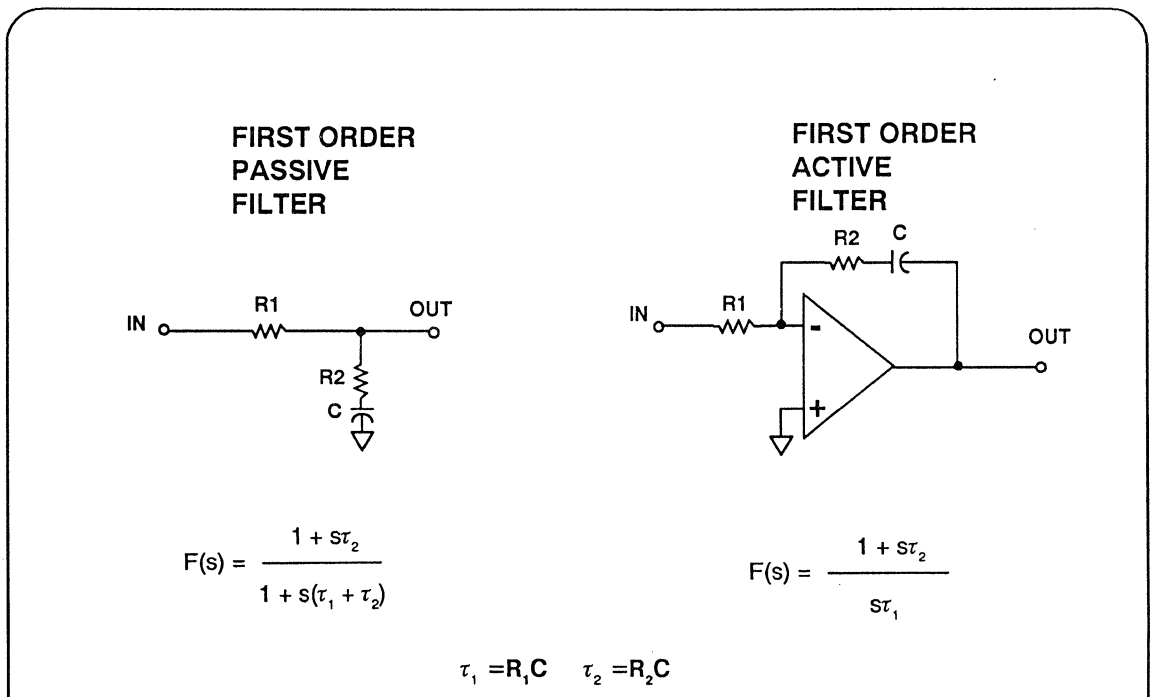
$$H(s) = \frac{K_d K_o}{Ns + K_d K_o}$$

Therefore, if we introduce a one pole loop filter, it is obvious that the PLL system becomes a second order system.

The most popular loop configuration is the second order loop, which is technically stable under all conditions. The second order loop gets one pole from the VCO and one pole from the loop filter. With the second order loop, the phase detector output is filtered before being used to control the VCO, thereby greatly reducing reference frequency sidebands in the VCO output.

Higher order loops should be used with caution since they become very difficult to stabilize. In fact, a second order loop can become unstable due to high frequency parasitics which may increase the loop order unintentionally.

The transfer functions F(s) are given in Figure 8.13 for the most popular passive and active first order loop filters, each having one pole and one zero. Recall that a first order loop filter will produce a second order unconditionally stable PLL.



FIRST ORDER PASSIVE AND ACTIVE LOOP FILTERS USED IN SECOND ORDER PLLs

Figure 8.13

The basic analysis and design of a PLL now centers around the optimization of the loop filter transfer function F(s) for the desired PLL characteristics. If the values of F(s) for the passive and active case from Figure 8.13 are substituted in the equation for H(s), we obtain the following results:

PASSIVE LOOP:

$$H_p(s) = \frac{N_p(s)}{s^2 + 2\delta\omega_n s + \omega_n^2}, \text{ where}$$

$$\omega_n = \left[\frac{K_o K_d}{N(\tau_1 + \tau_2)}\right]^{\frac{1}{2}} =$$

natural frequency

$$\delta = \frac{1}{2}\left[\frac{K_o K_d}{N(\tau_1 + \tau_2)}\right]^{\frac{1}{2}}\left(\tau_2 + \frac{N}{K_o K_d}\right) =$$

damping factor

$N_p(s)$ = Numerator Function of s

ACTIVE LOOP:

$$H_A(s) = \frac{N_A(s)}{s^2 + 2\delta\omega_n s + \omega_n 2}, \text{ where}$$

$$\omega_n = \left(\frac{K_o K_d}{N\tau_1}\right)^{\frac{1}{2}} =$$

natural frequency

$$\delta = \frac{\tau_2}{2}\left(\frac{K_o K_d}{N\tau_1}\right)^{\frac{1}{2}} =$$

damping factor

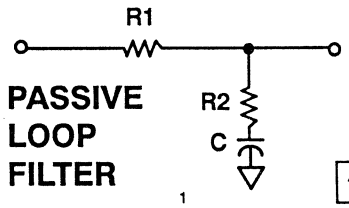
$N_A(s)$ = Numerator Function of S

The above equations were obtained by writing the transfer functions in normalized form as is often done in filter design. The natural frequency of the PLL (ω_n) is the frequency of a damped oscillation caused by a transient input. The damping factor of the PLL (δ) in conjunction with the natural frequency (ω_n) are the traditional servo loop parameters which dominate the PLL control voltage response characteristics. If $\delta = 1$, the system is critically damped. If $\delta < 1$, the system becomes oscillatory and tends to overshoot. In most practical systems, an optimally flat frequency-transfer characteristic is the goal. This implies $\delta = 1/\sqrt{2} \approx 0.7$. If $\delta >> 1$, the transfer function flattens out, and the dynamic response becomes sluggish. The second order PLL is actually a low pass filter for input signals whose frequency spectrum is between zero and approximately the natural frequency ω_n. This means that a second order PLL is able to track for phase and frequency modulations of the reference signal as long as the modulation frequencies remain within an angular frequency band roughly between zero and ω_n. Damping curves which show the relationship between ω_n, phase error and δ are given in Reference 2, p. 49 (Gardner). It should be noted, however, that these curves assume that $K_o K_d >> \omega_n$, the criterion for a high gain loop.

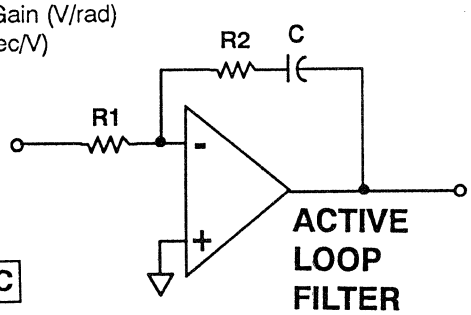
SECOND ORDER PLL DESIGN EQUATIONS

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \text{PHASE TRANSFER FUNCTION} = \frac{\text{NUMERATOR (s)}}{s^2 + 2\delta\omega_n s + \omega_n^2}$$

ω_n = Natural Frequency
δ = Damping Factor
K_d = Phase Detector Gain (V/rad)
K_o = VCO Gain (rad/sec/V)
N = Integer Divisor



PASSIVE LOOP FILTER



ACTIVE LOOP FILTER

$\tau_1 = R_1C \quad \tau_2 = R_2C$

$$\omega_n = \left[\frac{K_oK_d}{N(\tau_1 + \tau_2)}\right]^{\frac{1}{2}}$$

$$\delta = \frac{\omega_n}{2}\left[\tau_2 + \frac{N}{K_oK_d}\right]$$

If $K_oK_d >> \omega_n$
$K_oK_d\tau_2 >> N$
$\tau_1 >> \tau_2$

$$\omega_n \simeq \left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}}$$

$$\delta \simeq \frac{\omega_n\tau_2}{2}$$

$$\omega_n = \left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}}$$

$$\delta = \frac{\omega_n\tau_2}{2}$$

Figure 8.14

If $K_oK_d >> \omega_n$, and $K_oK_d\tau_2 >> 1$ (the criteria for a high gain passive loop), then the equations for ω_n and δ reduce to those of the active loop:

Active/Passive Loop, $K_oK_d >> \omega_n$
$K_oK_d\tau_2 >> N$
$\tau_1 >> \tau_2$

$$\omega_n \simeq \left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}}$$

$$\delta \simeq \frac{\tau_2}{2}\left(\frac{K_oK_d}{N\tau_1}\right)^{\frac{1}{2}} = \frac{\tau_2\omega_n}{2}$$

If the PLL is used for frequency synthesis, the damping factor δ is a function of the divider ratio N. If the divider ratio is variable in the range $N_{MIN} \le N \le N_{MAX}$,

$$\frac{\delta_{MAX}}{\delta_{MIN}} = \sqrt{\frac{N_{MAX}}{N_{MIN}}}$$

If N is changed by a factor of 100, δ varies by a factor of 10, which would be intolerable. The PLL would be underdamped or overdamped at the limits of its frequency range. In such applications, the loop filter time constants have to be switched in accordance with the instantaneous value of N in order to achieve a damping factor in the approximate range between 0.5 and 1.

USING THE AD9901 IN A PLL

A PLL which multiplies a 56 MHz reference frequency input to 112 MHz is shown in Figure 8.15. A FET Colpitts oscillator was chosen along with two MV1404 varactor diodes and a 100nH coil in the circuit shown. For this circuit, the output frequency versus varactor diode reverse bias voltage is plotted in Figure 8.16 (data obtained experimentally). Note that an operating point of 5.5V is optimum for an output frequency of about 110 MHz. The VCO gain can be calculated from Figure 8.16.

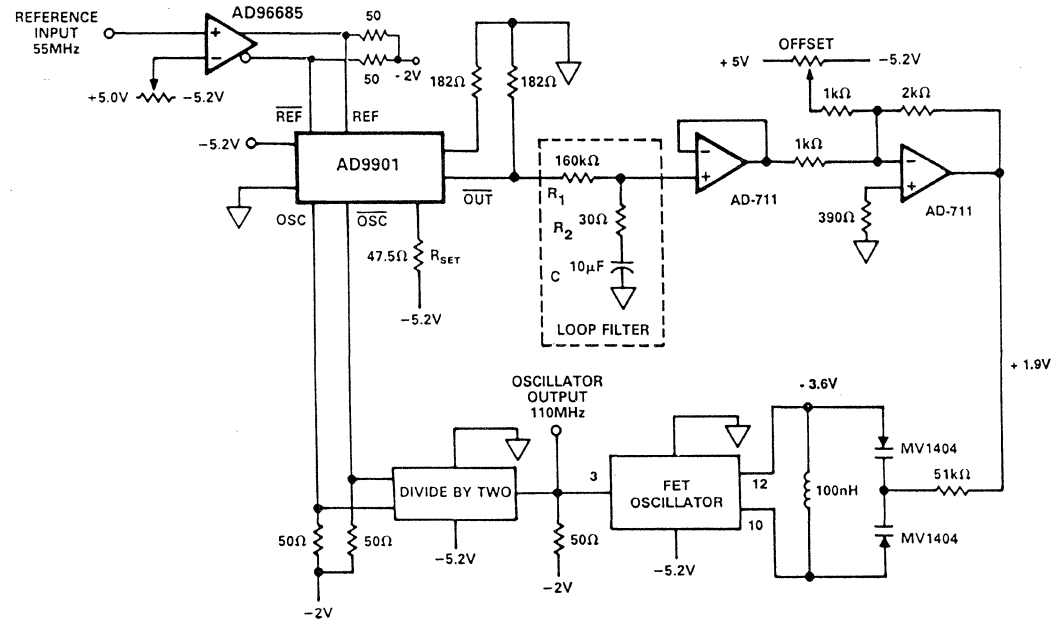
$$K_o = 115 \times 10^6 \text{ rad/sec/V.}$$

An output swing of 1.8V is chosen for the AD9901 operating in the ECL mode. R_{SET} is chosen to be 47.5Ω such that the output current is 9.9mA. With a 182Ω output resistor, the output swing is 1.8V. This low value for R_{LOAD} assures that the parasitic pole associated with the output capacitance of the AD9901 is minimized. The phase detector gain is next calculated:

$$K_d = \frac{1.7\text{V}}{2\pi \text{ rad}} = 0.286\text{V/rad}$$

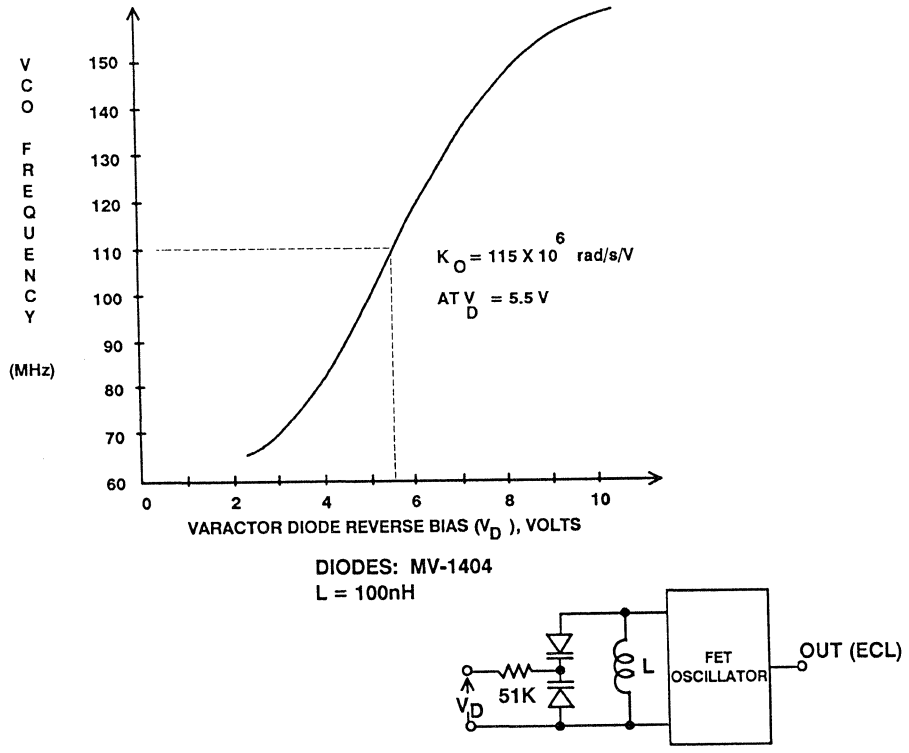
Because the phase detector is used in ECL mode, its output swing is -1.8V to 0V. At phase lock, the nomimal mean output is therefore -0.9V. This must be matched to the VCO input range.

The optimum varactor diode reverse bias voltage was determined to be +5.5V for an output frequency of 110 MHz. The nominal input voltage for the FET oscillator is -3.6V. The input voltage to the 51kΩ resistor required to maintain the 5.5V varactor diode reverse bias is +5.5 - 3.6 = +1.9V.



PLL USING AD-9901 PHASE/FREQUENCY DISCRIMINATOR

Figure 8.15



VCO CHARACTERISTICS

Figure 8.16

Since the mean value of the AD9901 at lock is -0.9V, an inverting gain stage of -2 is used after the unity gain follower stage. An offset adjustment is provided to allow the user to vary the phase of the output signal versus the input signal. This is an easy way for the user to check the output linearity of the phase detector.

Another advantage of the complementary differential outputs of the AD9901 is the designer can choose which output (either increasing or decreasing) is correct for the application. Since an inverting gain stage was used, the inverting AD9901 output was chosen. This inverts the signal before the gain stage corrects the signal polarity.

A passive loop filter having a single pole is used to produce a second order PLL. The output of the loop filter is buffered by a unity gain follower before going to the inverting gain stage.

The final stage of the design is to calculate the natural frequency ω_n and the damping factor δ. From the damping curves, a damping factor of 0.7 allows the loop to settle to within 5% of its final value within one millisecond with less than 25% overshoot.

From the set of damping curves, p. 49, Ref. 2

$$\omega_n t = 4.5$$

For t = 1ms

$$\omega_n = 4.5 \text{ KHz}$$

The gain of the inverting stage is then lumped into the phase detector gain to give

$K_d = 0.286\text{V/rad} \times 2 = 0.572\text{V/rad}.$

With $K_o = 115 \times 10^6$ rad/sec/V, the equations

$$\omega_n \approx \left(\frac{k_o k_d}{N\tau_1}\right)^{\frac{1}{2}} \quad \text{and}$$

$$\delta \approx \frac{\tau_2 \omega_n}{2} \quad \text{with N = 2,}$$

are solved for τ_1 and τ_2 yielding:

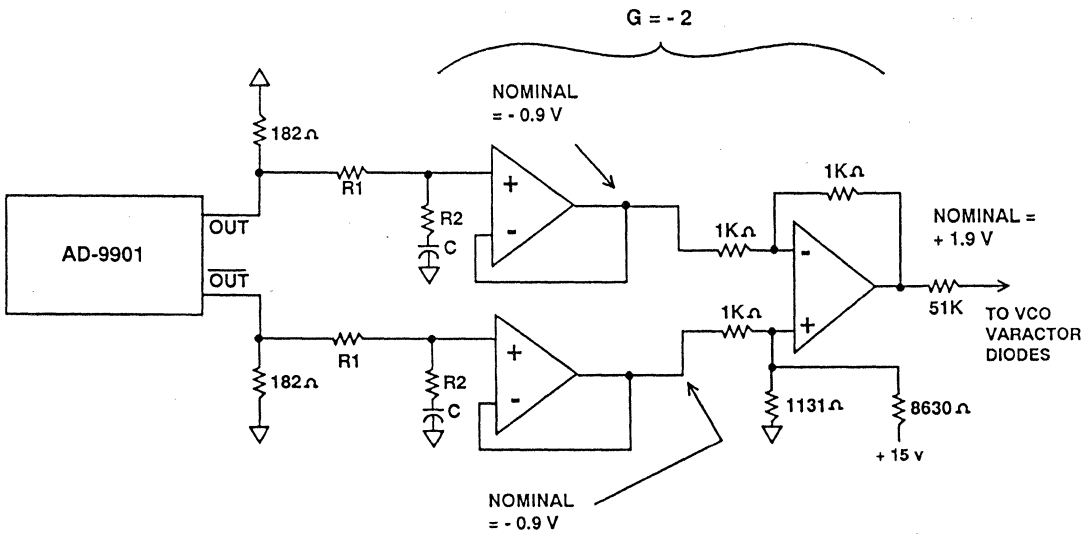
$\tau_1 = 1.624$ sec = R1•C
$\tau_2 = 311 \times 10^{-6}$ sec. = R2•C

The following values are chosen for R1, R2 and C:

C = 10μF
R1 = 160kΩ
R2 = 30Ω

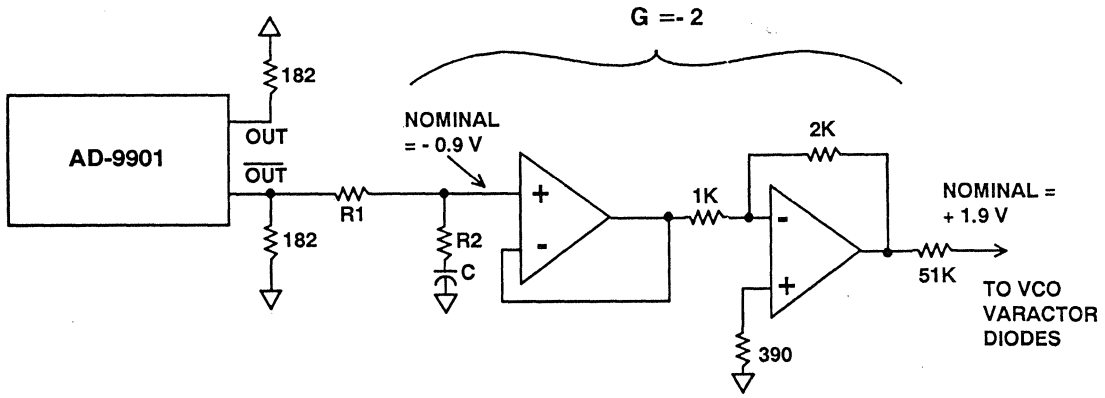
The design is now complete.

The outputs of the AD9901 can be used in the single ended or differential mode. Figure 8.17 shows the single ended configuration while Figure 8.18 shows the differential connection.



AD-9901 USED IN DIFFERENTIAL OUTPUT MODE

Figure 8.17



AD-9901 USED IN SINGLE-ENDED OUTPUT MODE

Figure 8.18

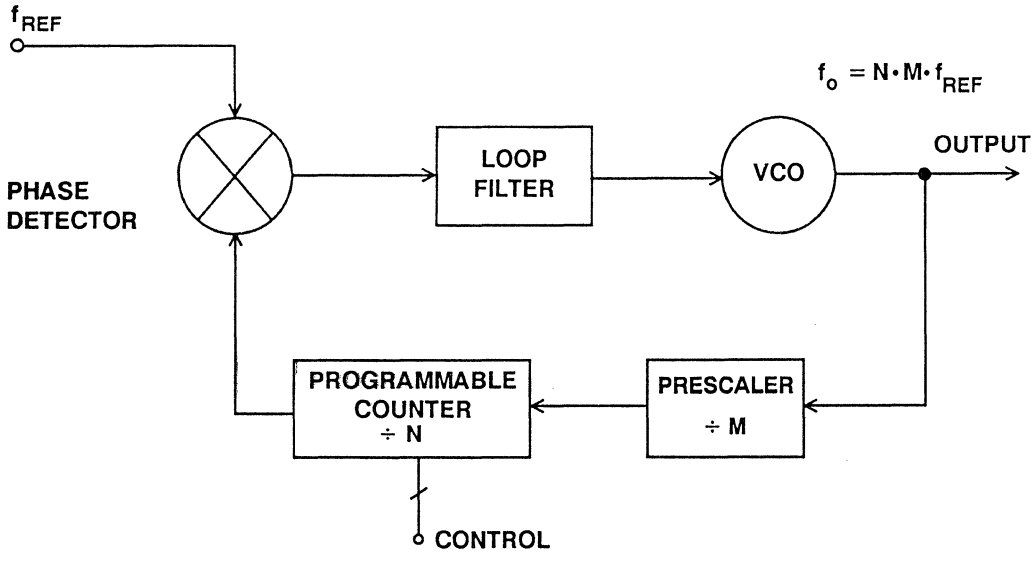
USE OF DUAL MODULUS PRESCALERS

In a PLL which does not use fractional division techniques (such as pulse swallowers), the output frequency is limited to integer multiples of the reference frequency, i.e., $f_o = N \cdot f_{REF}$. Flexible programmable counters can perform this function but often must be preceded by higher speed dividers called prescalers which bring the VCO frequency into the range of the programmable counter as shown in Figure 8.19. The use of a prescaler which divides the VCO output frequency by M limits the frequency resolution of the PLL to multiples of $M \cdot f_{REF}$ rather than f_{REF}.

High speed dual modulus prescalers as shown in Figure 8.20 solve this problem as follows. The modulus of the prescaler is controlled by a third counter causing it to alternate between M and M + 1. Assume all three counters have been set for the beginning of a cycle: the prescaler for division by M + 1, the modulus control counter for division by N_{MC}, and the programmable counter for division by N_{PC}. The prescaler will divide by M + 1 until the modulus control counter has counted down to zero. At this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle. The output frequency is given by:

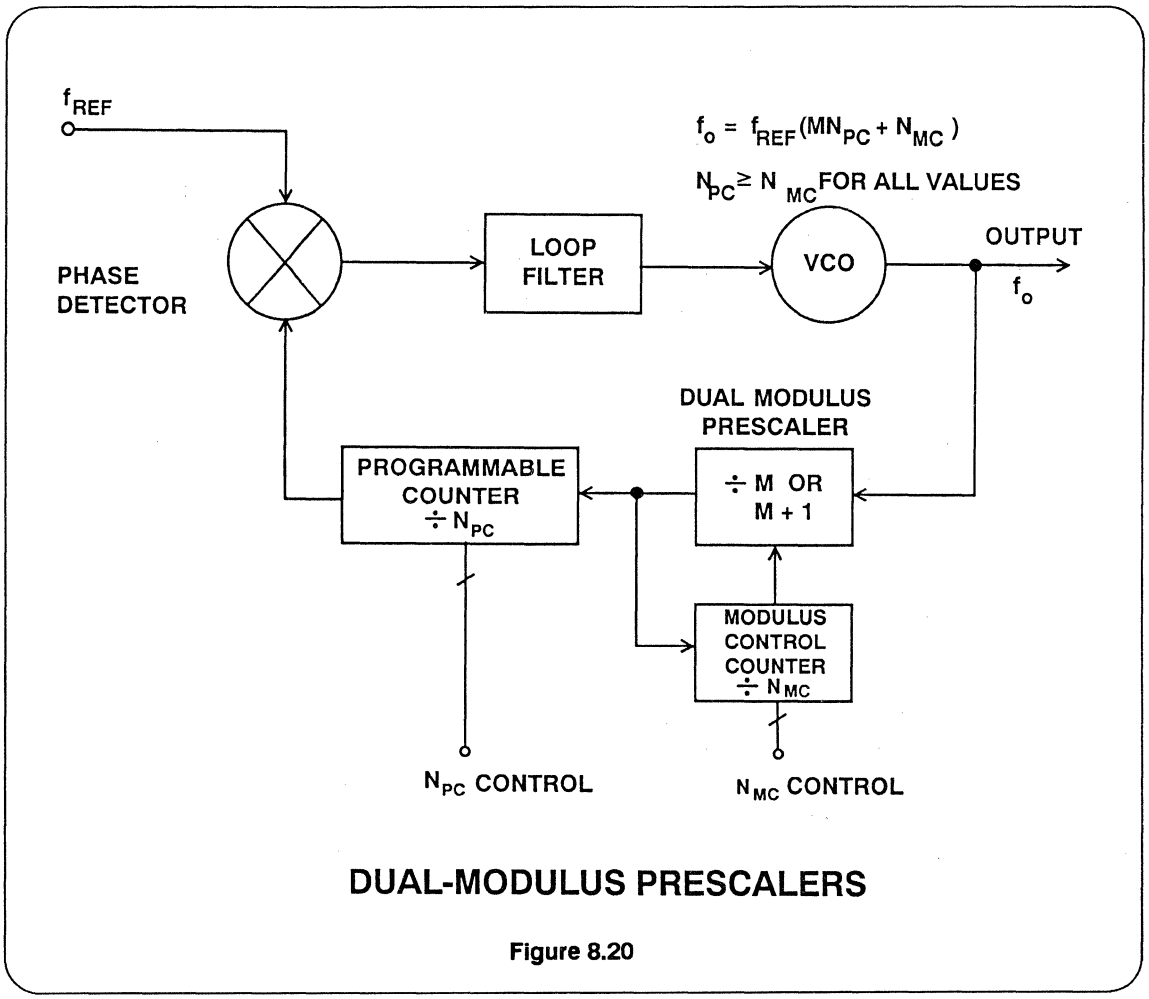
$$f_o = (MN_{PC} + N_{MC}) \cdot f_{REF}$$

Note that channels can be selected every f_{REF} by letting N_{PC} and N_{MC} take on suitable integer values, including zero, provided $N_{PC} \geq N_{MC}$ for all values.



HIGH-SPEED PRESCALER

Figure 8.19



DUAL-MODULUS PRESCALERS

Figure 8.20

PLL REFERENCES

1. R.E. Best, **Phase-Locked Loops**, McGraw-Hill, New York, 1984.

2. F.M. Gardner, **Phaselock Techniques**, 2nd ed., John Wiley and Sons, New York, 1979.

3. Applications Note AN-535, Phase-locked Loop Design Fundamentals, Motorola, Inc.

4. Corinn Fahrenkrug, CAE Basics for Phase-locked Loops, **RF Design**, May 1988.

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6. Richard Goodall, Signal Source Specs Hold Key to Receiver Tests, **Microwaves and RF**, November 1986.

7. Bill Travis, Phase-locked Loops and Frequency Dividers Handler Higher Speed Circuit Functions, **EDN**, August 21, 1986.

8. William Rischpater, Predict PLL Phase Noise from Oscillator Data, **Microwaves and RF**, April 1987, pp. 117-120.

9. Understanding and Measuring Phase Noise in the Frequency Domain, HP Application Note AN-207, October 1976.

SECTION IX

FREQUENCY DOMAIN FUNCTIONS:

D/A CONVERSION AND DIRECT DIGITAL SYNTHESIS

FREQUENCY DOMAIN FUNCTIONS: D/A CONVERSION AND DIRECT DIGITAL SYNTHESIS

APPLICATIONS FOR HIGH SPEED DACs

DYNAMIC PERFORMANCE CONSIDERATIONS AND SPECIFICATIONS FOR DACs
- Settling Time, Update Rate, Glitch Impulse, Harmonic Distortion, Phase Noise

SIN X/X ROLLOFF EFFECT

HIGH SPEED DAC IMPLEMENTATIONS

DESIGNING FOR MINIMUM GLITCH IMPULSE

GLITCH REDUCTION USING SEGMENTATION

DEGLITCHING USING SHAs

DIRECT DIGITAL SYNTHESIS TECHNIQUES

FREQUENCY SYNTHESIS FIGURES OF MERIT

DIRECT DIGITAL SYNTHESIS APPLICATIONS

9

APPLICATIONS FOR DACS

High-speed D/A converters (DACs) have wide applications in instrumentation, waveform reconstruction and generation, and direct digital synthesis (DDS). A new class of function generators called Arbitrary Waveform Generators allow a wide variety of complex waveforms to be programmed into a memory and then read out through a DAC.

Graphics display systems also utilize high-speed DACs to direct and/or modulate the scanning electron beam across the CRT screen. Vector scan display systems and raster scan display systems are the two most popular video displays in use today. A special type of high-speed DAC, sometimes referred to as a "VIDEODAC", contains functions which allow ease of use in raster scan display systems. Some newer videodacs contain color palette memories and are often referred to as "RAMDACs".

High-speed DACs are essential building blocks for successive approximation and digitally corrected subranging A/D converters. This application has been discussed previously in the section on A/D Conversion.

DYNAMIC PERFORMANCE CONSIDERATIONS AND SPECIFICATIONS FOR DACS

Settling time of a DAC is traditionally defined as the time from the digital input transition (usually measured from the 50% point) until the DAC output settles to within a certain error band (usually 1/2 LSB) which is centered around the final value. As shown in Figure 9.2, a portion of the settling time may be due to a fixed propagation delay through the switches. If the DAC has a set of input latches or registers, the settling time is measured from the 50% point of the latch strobe or register clock. Fullscale DAC settling time is measured for a digital input transition from 000...0 to 111...1. Midscale settling time is measured for a digital transition from 011...1 to 100...0 or 100.0 to 011...1.

DAC *update rate* must be considered in conjunction with settling time and propagation delay in order to be a meaningful spec. Typically, the maximum update rate is the reciprocal of the difference between the settling time and the propagation delay. Updating the DAC faster will cause errors since the output is not given enough time to settle to within $\pm 1/2$ LSB. This situation may be acceptable in some applications - especially where the maximum digital input change between updates is limited to a few LSBs.

HIGH SPEED DAC APPLICATIONS

- Instrumentation
  - Waveform Reconstruction
  - Arbitrary Waveform Generators
- Direct Digital Synthesis (DDS)
- Graphics Display Systems
  - Vector Scan
  - Raster Scan - Videodacs, Ramdacs
- A/D Converters
  - Successive Approximation
  - Digitally Corrected Subranging (DCS)

Figure 9.1

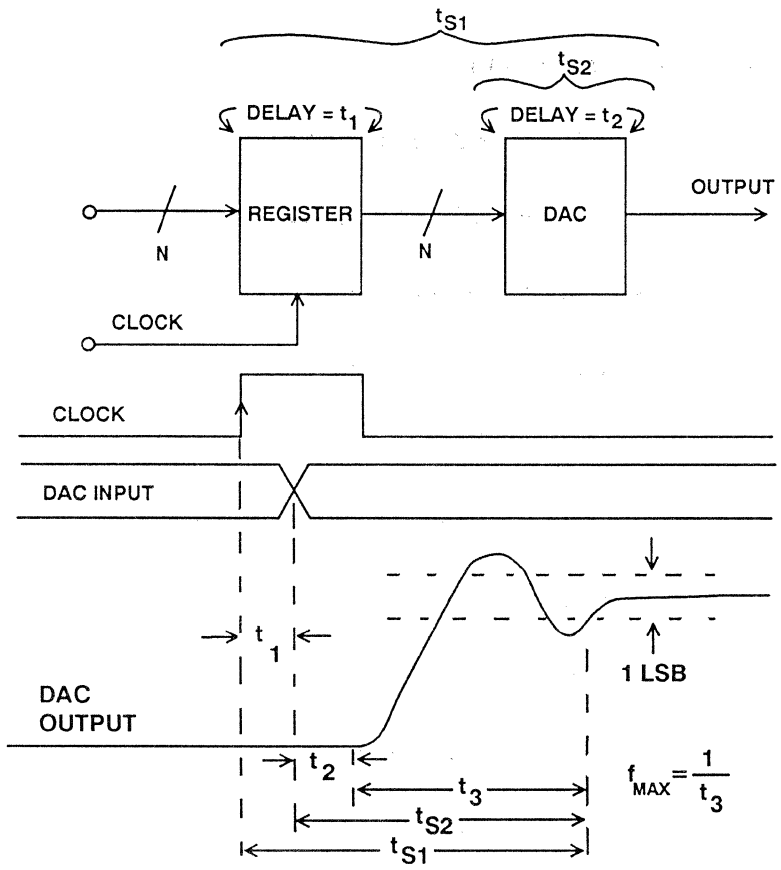
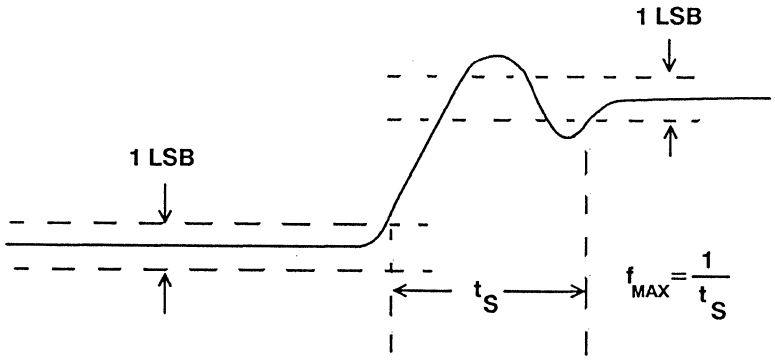


Figure 9.2

It is entirely correct to define DAC settling time with respect to the output alone as shown in Figure 9.3. Settling time is measured from the time the output leaves a ±1/2 LSB error band centered around the initial value until the time the output remains within a ±1/2 LSB error band centered around the final value. The maximum DAC update rate allowable for ±1/2 LSB settling time then becomes:

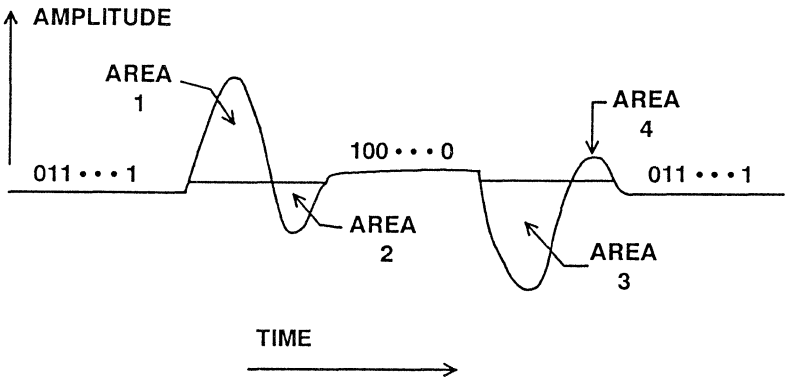
$$f_{MAX} = \frac{1}{t_S}$$

This technique effectively removes the propagation delay due to the input registers and the DAC switches from the measurement. Window comparators are useful in performing this measurement.



SETTLING TIME REFINED WITH RESPECT TO DAC OUTPUT

Figure 9.3



GLITCH IMPULSE AREAS: AREA 1
AREA 2
AREA 3
AREA 4

NET GLITCH IMPULSE AREAS: | AREA 1 - AREA 2 |

| AREA 3 - AREA 4 |

GLITCH IMPULSE WAVEFORMS

Figure 9.4

Glitch impulse area is best understood by examining the waveform shown in Figure 9.4. DAC glitches occur because of digital input logic skew and unequal propagation delays through the DAC switches. The glitches are usually the largest at the midscale transition because all bits in the DAC are changing at this point. The glitch produced by the 011...1 to 100...0 transition is usually different from that produced by the 100...0 to 011...1 transition, so each must be analyzed. *Glitch impulse area* is simply the area of a particular glitch and is usually measured in the units of pV-sec, therefore the fullscale output voltage of the DAC must be known in order to make meaningful comparisons between DACs. The term "glitch energy" is incorrect since the unit pV-sec is *not* a measure of energy.

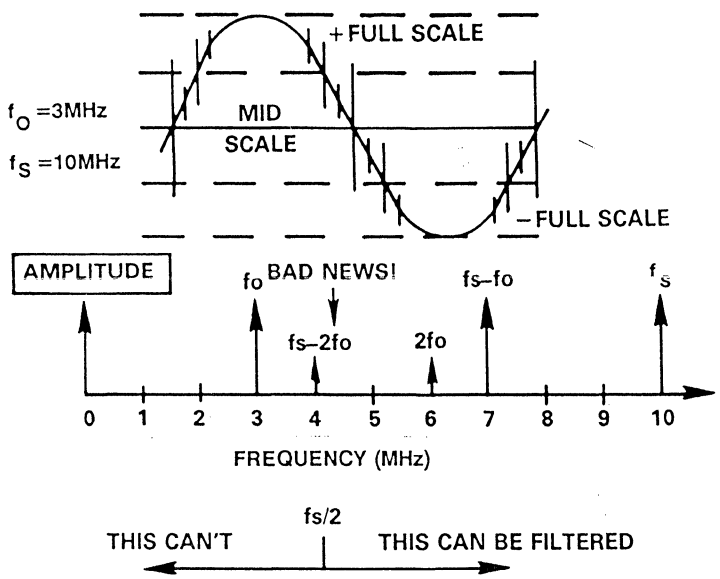
Glitches may also be caused by charge coupling by stray capacitance between the digital and analog regions of the DAC. These glitches are unaffected by reference amplitude so may be measured, independent of skew-related glitches, by measurements made in the absence of a reference voltage.

From Figure 9.4 it is clear that there are six possible glitch impulse areas to deal with. There are two glitch impulses associated with each transition. Their respective areas are designed 1, 2, 3 and 4. In addition, it is also useful to consider the *net glitch impulse* area associated with each of the two transitions. There are, respectively, AREA 1 - AREA 2 , and AREA 3 - AREA 4 . When examining the glitch impulse area specification on a DAC data sheet, it is therefore clear that there is much room for confusion unless a considerable amount of clarification is provided by the manufacturer.

Glitch impulse area remains constant regardless of filtering. Fast settling time specifications do not always imply low glitch impulse areas. The desirable situation is for the DAC to have a net glitch impulse area of zero for each of the two transitions, i.e., AREA 1 - AREA 2 = AREA 3 - AREA 4 = 0. In the ideal case, of course, AREA 1 = AREA 2 = AREA 3 = AREA 4 = 0.

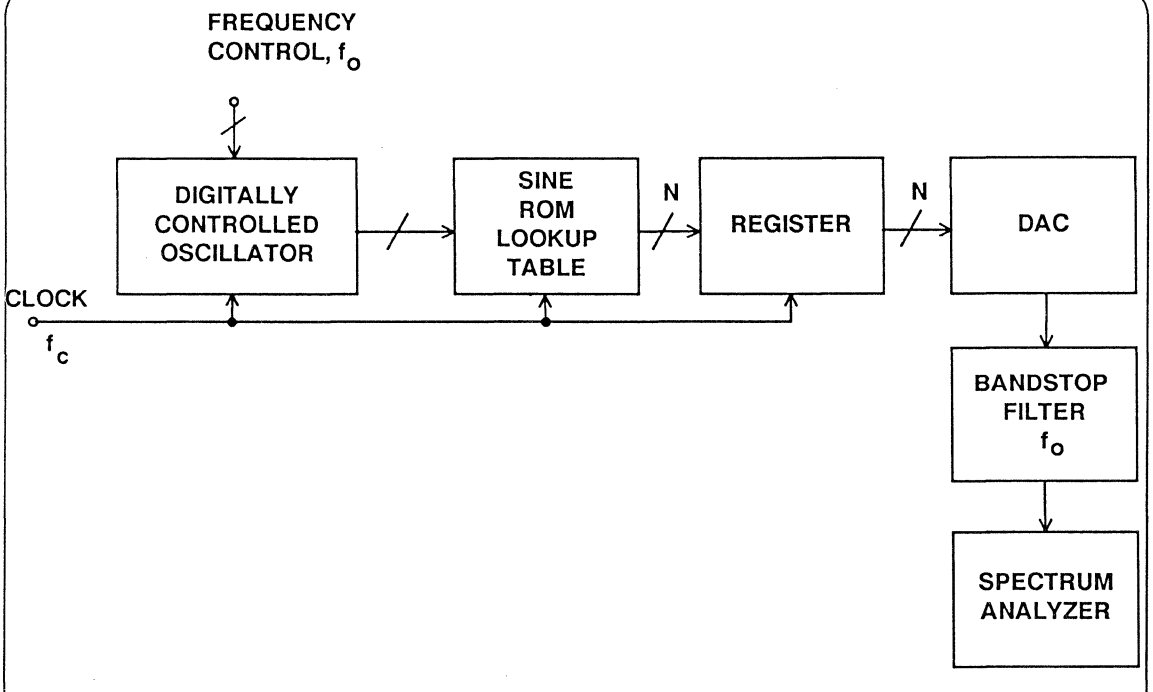
Because the net glitch impulse area is code dependent, it will produce harmonics when the DAC is reconstructing a sinewave. A net midscale glitch occurs twice during a single cycle of the reconstructed sinewave (at each zero crossing) and, therefore, will produce a second harmonic of the sinewave as shown in Figure 9.5. As shown in Figure 9.5, higher order harmonics of the fundamental sinewave which alias back into the Nyquist bandwidth are not filterable. It is difficult to predict the harmonic distortion caused by a specified net glitch impulse area, therefore, both specifications are required to adequately evaluate the dynamic performance of a high-speed DAC.

Distortion present at the output of a DAC reconstructing a sinewave from a ROM can be measured directly using an analog spectrum analyzer as shown in Figure 9.6. It is often useful to insert a bandstop filter between the DAC and the analyzer input in order to prevent erroneous readings due to overdriving the analyzer's front end amplifier. As with A/D converters, the harmonic distortion levels in a DAC are not necessarily related to the DAC resolution. It is entirely possible for a low-glitch 8-bit ECL DAC such as the AD9768 to have lower harmonic distortion levels than a 12-bit TTL DAC such as the AD-568.



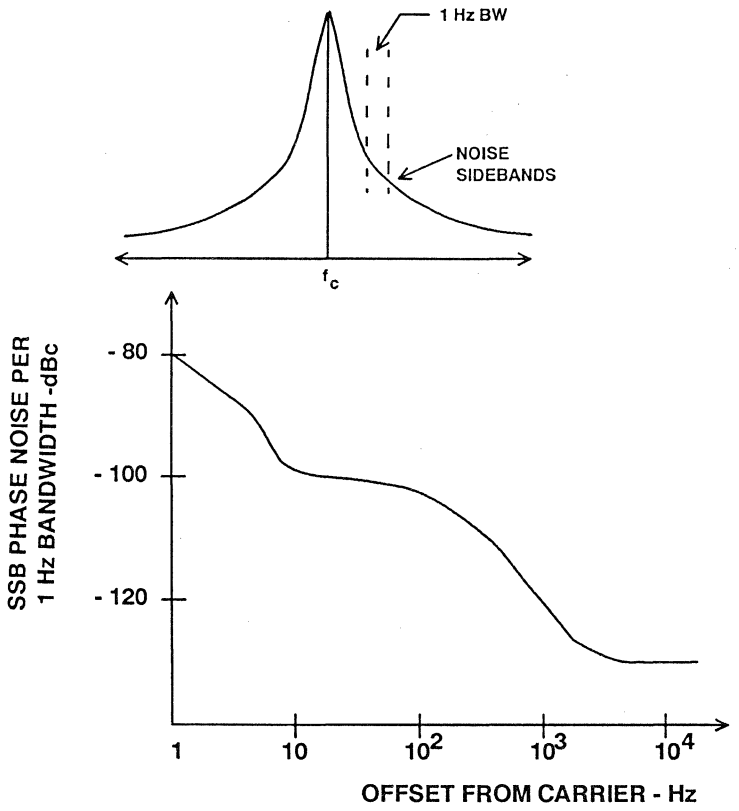
EFFECTS OF DAC GLITCHES

Figure 9.5



MEASURING DAC HARMONIC DISTORTION

Figure 9.6



SINGLE-SIDED PHASE NOISE SPECTRAL DENSITY

Figure 9.7

Various techniques for reducing the glitch impulse area of a DAC (and thereby reducing harmonic distortion) will be discussed later in this section.

Phase noise of a reconstruction DAC is measured and specified in a manner similar to that of a high quality frequency synthesizer. The noise specification that is most widely used in the signal generator industry is the single-sided phase noise spectral density as shown in Figure 9.7. The spectral density is a plot of the noise power per Hertz bandwidth as a function of frequency offset from the carrier frequency.

Direct measurement of this spectral density function with a spectrum analyzer may not be possible, and the signal may have to be demodulated to baseband in order to obtain the measurement with low-frequency instruments.

As high-speed, high-resolution reconstruction DACs begin to proliferate in the field of arbitrary waveform generation and direct digital synthesis, dynamic performance specifications such as harmonic distortion and phase noise will begin to become commonplace on DAC data sheets.

SINX/X FREQUENCY ROLLOFF EFFECT

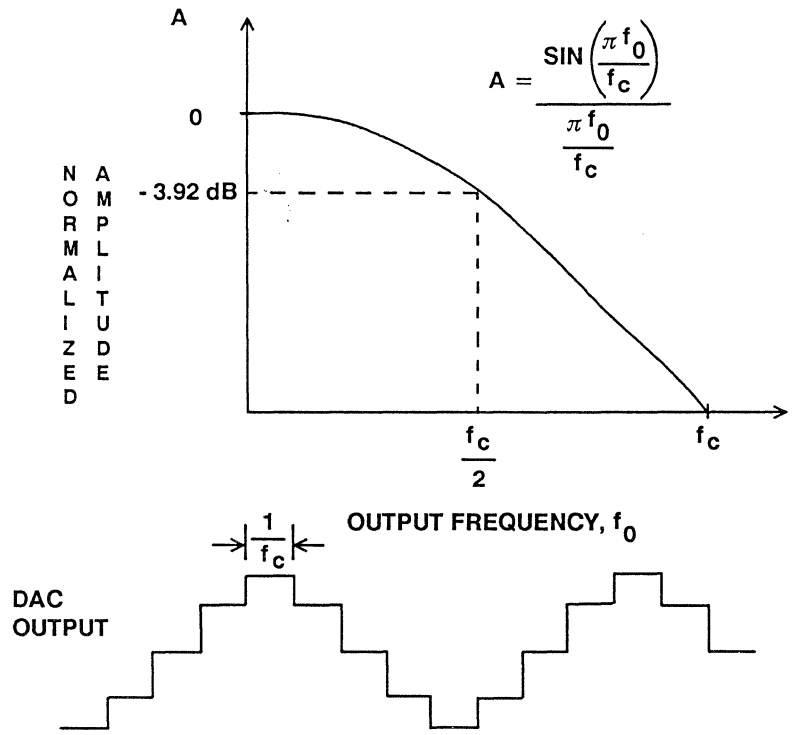
The output of a reconstruction DAC can be visualized as a series of rectangular pulses whose width is equal to the reciprocal of the update rate (see Figure 9.8). The frequency response is given by the equation:

$$A = \frac{\sin\left(\frac{\pi f_o}{f_c}\right)}{\frac{\pi f_o}{f_c}}$$

where

A = normalized output amplitude
f_c = DAC update frequency
f_o = reconstructed output frequency

Note that the reconstructed signal is down 3.92dB at the Nyquist limit with respect to the low frequency value. An "inverse" SINX/X filter is sometimes placed after the DAC to correct for this effect.



SIN X/X ROLLOFF

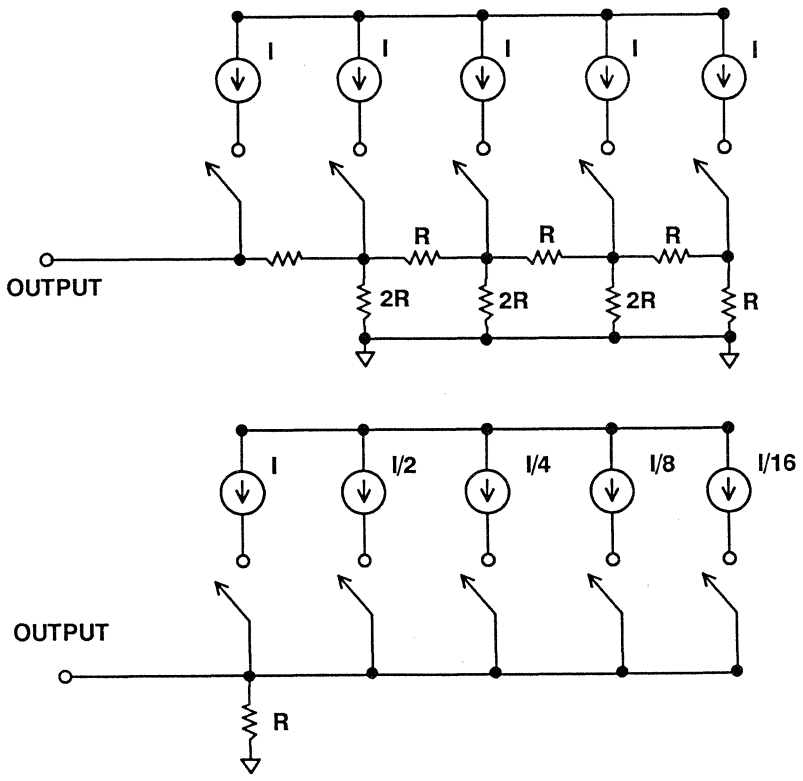
Figure 9.8

HIGH SPEED DAC IMPLEMENTATIONS

Most DACs consist of two basic elements: a set of current switches and a method for binary current division. Figure 9.9 shows two methods for constructing a DAC. In the first method, the current switches carry equal currents and the binary scaling is done with a R-2R resistor network. The second method utilizes binarily weighted current sources whose switched outputs are summed together.

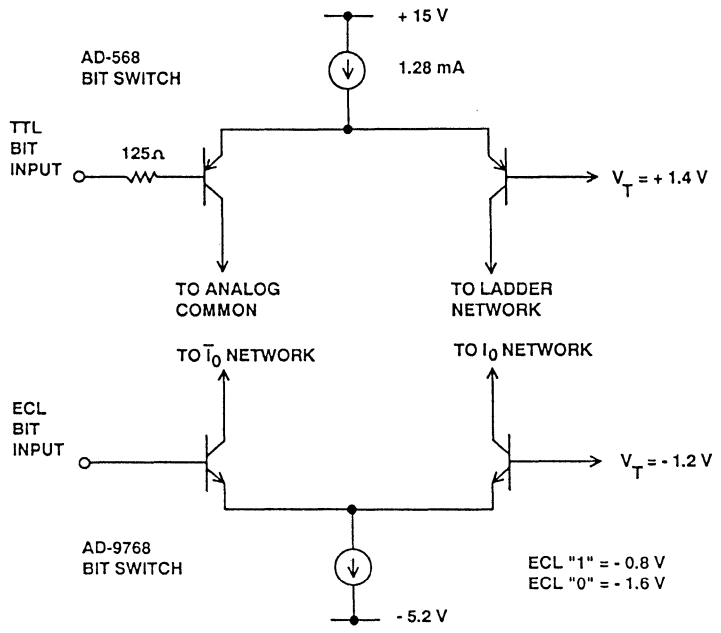
Some high-speed DACs use a combination of the two methods: binarily weighted current switches for the MSBs followed by R-2R current division for the LSBs.

Differential pairs are often utilized for the actual current switches. Figure 9.10 shows a typical PNP current switch for a TTL DAC (AD-568) and an NPN switch for an ECL DAC (AD9768).



DAC ARCHITECTURES

Figure 9.9



TTL AND ECL BIT SWITCHES

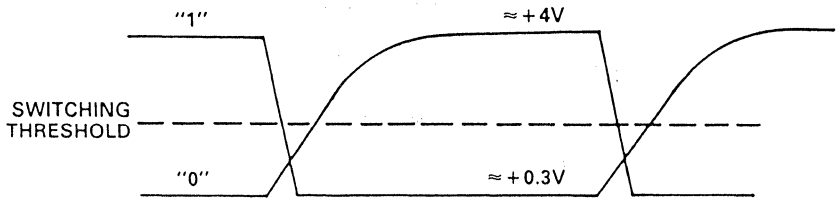
Figure 9.10

DESIGNING FOR MINIMUM GLITCH IMPULSE

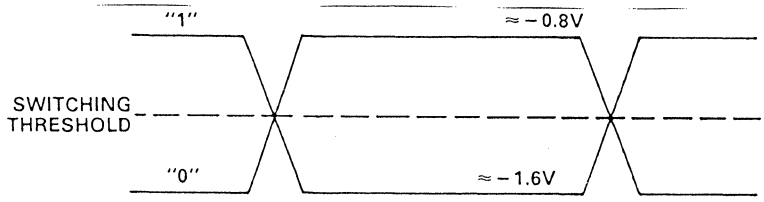
Most low glitch high-speed DACs are designed around differential NPN switches which are driven by ECL logic levels. ECL logic swings are symmetrical and have an amplitude which is more than sufficient to switch a differential pair. TTL logic swings on the other hand are not symmetrical and have propagation delays which depend upon the direction of the logic transition as shown in Figure 9.11. HCMOS and fast logic swings are more symmetrical than standard bipolar TTL and provide a better choice for driving high-speed TTL DACs such as the AD-568. The effect of drive logic on the dynamic performance of the 12-bit AD-568 DAC is shown in Figure 9.12.

Deskewing is a technique which is often used to reduce the glitch impulse. This amounts to equalizing the delay of the first two or three most significant bits by the use of an external RC network as shown in Figure 9.13. The resistors and capacitors are adjusted until both the 011...1 to 100...0 and the 100...0 to 011...1 glitch have been minimized. Some high-speed DACs such as the AD-568 have the capability of externally "tweaking" the switching logic voltage threshold and thereby reducing the data skew further. The effects of this threshold adjustment for the AD-568 are shown in Figure 9.14.

ECL DACS such as the 8-bit AD9768 can be effectively deskewed using capacitors as shown in Figure 9.15. Using this technique, it is possible to reduce the glitch impulse to less than 100pV-sec.



TTL LOGIC SWITCHING



ECL LOGIC SWITCHING

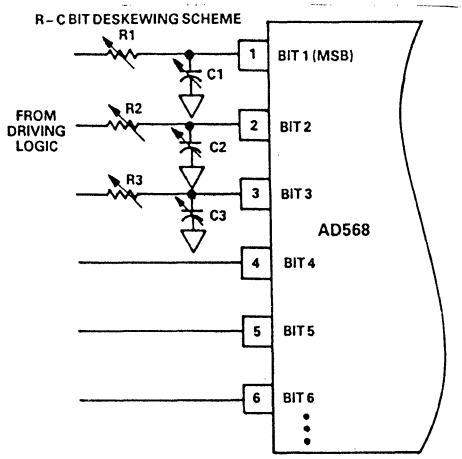
TTL AND ECL LOGIC TRANSITIONS

Figure 9.11

AD-568
DAC PERFORMANCE VS. DRIVE LOGIC

Logic Family	10-90% DAC Rise Time	DAC Settling Time 1%	0.1%	0.025%	Glitch Impulse	Maximum Glitch Excursion
TTL	11ns	18ns	34ns	50ns	2.5nV-s	240mV
LSTTL	11ns	28ns	46ns	80ns	950pV-s	160mV
STTL	9.5ns	16ns	33ns	50ns	850pV-s	150mV
HCMOS	11ns	24ns	38ns	50ns	350pV-s	115mV
FAST*	12ns	16ns	36ns	42ns	1.0nV-s	250mV

Figure 9.12

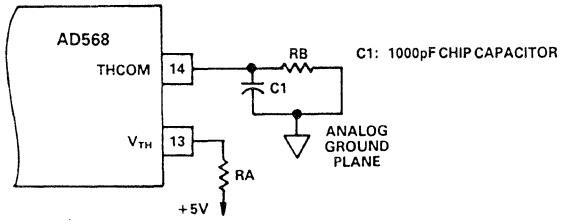


Logic Family	Gate	Uncompensated Glitch	Compensation Used	Compensated Glitch
HCMOS	74157	350pV-s	C2 = 5pF	250pV-s
STTL	74158	850pV-s	R1 = 50Ω, C1 = 7pF	600pV-s

R and C Values = 0 Unless Otherwise Noted

EFFECTS OF DESKEWING ON AD-568 GLITCH
Figure 9.13

SELECTING RA AND RB:
RA + RB = 5V/3.6mA
THRESHOLD VOLTAGE = V_{TH} = 1.4V + (3.6mA × R_B)



POSITIVE THRESHOLD VOLTAGE SHIFT

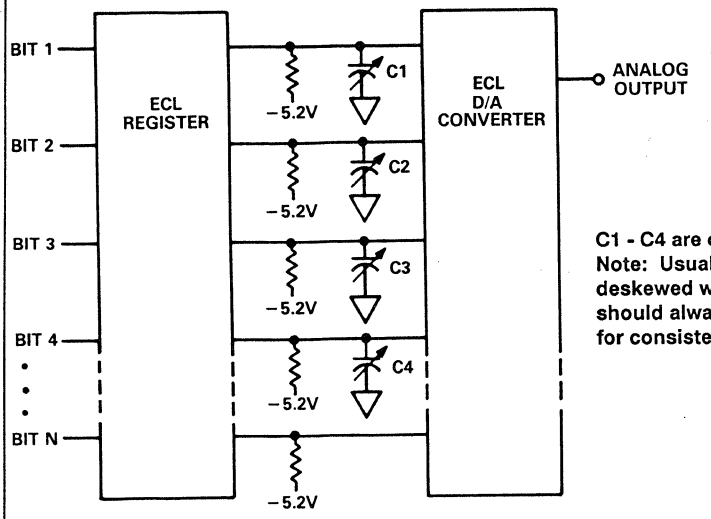
THRESHOLD SHIFT FOR GLITCH IMPROVEMENT[1]

Logic Family	Gate	Uncompensated Glitch	Modified Threshold[2]	Resulting Glitch
HCMOS	74HC158	350pV-s	1.7V	150pV-s
STTL	74S158	850pV-s	1.0V	200pV-s
FAST	74F158	1000pV-s	1.3V	480pV-s

NOTES:
[1] Measurements made on a modified version of the circuit shown in Figure 13, with a 1V full scale.
[2] Use care in any scheme that lowers the threshold voltage since the output voltage compliance of the DAC is sensitive to this voltage. If the DAC is to be operated in the voltage output mode, it is strongly suggested that the threshold voltage be set at least 200mV above the output voltage full scale.
For threshold voltage less than + 1.4V, drive pin 3 directly with a voltage source and tie pin 14 to ground.

EFFECTS OF THRESHOLD VOLTAGE ON AD-568 GLITCH

Figure 9.14



C1 - C4 are optimized for minimum glitch on D/A output. Note: Usually, only the first 3 or 4 bits need to be deskewed with capacitors. The most significant bits should always be routed through one 10131 or 10176 for consistency in timing and reduced data skew.

DESKEWING ECL DACs

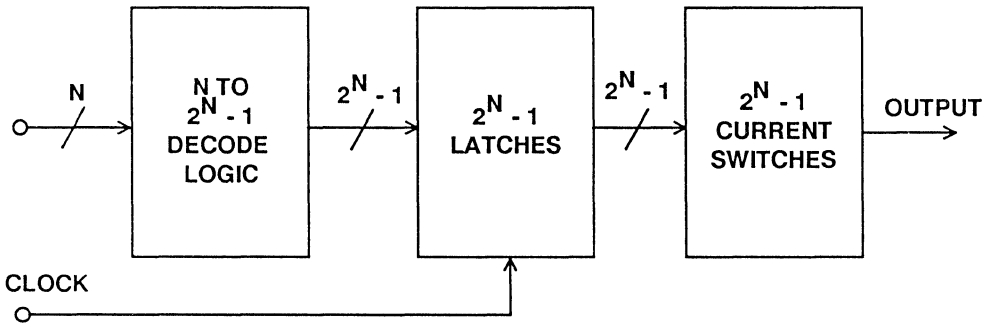
Figure 9.15

GLITCH REDUCTION USING SEGMENTATION

If real estate, cost, power and capacitance were of no consideration, the ideal "glitchless" DAC would consist of 2^N-1 equally weighted current switches preceded by decoding logic as shown in Figure 9.16. The glitch produced by switching between levels is code-independent and, therefore, does not generate harmonics of the sinewave being reconstructed. A set of latches is required after the binary decoding logic in order to equalize the delays to the actual switches themselves.

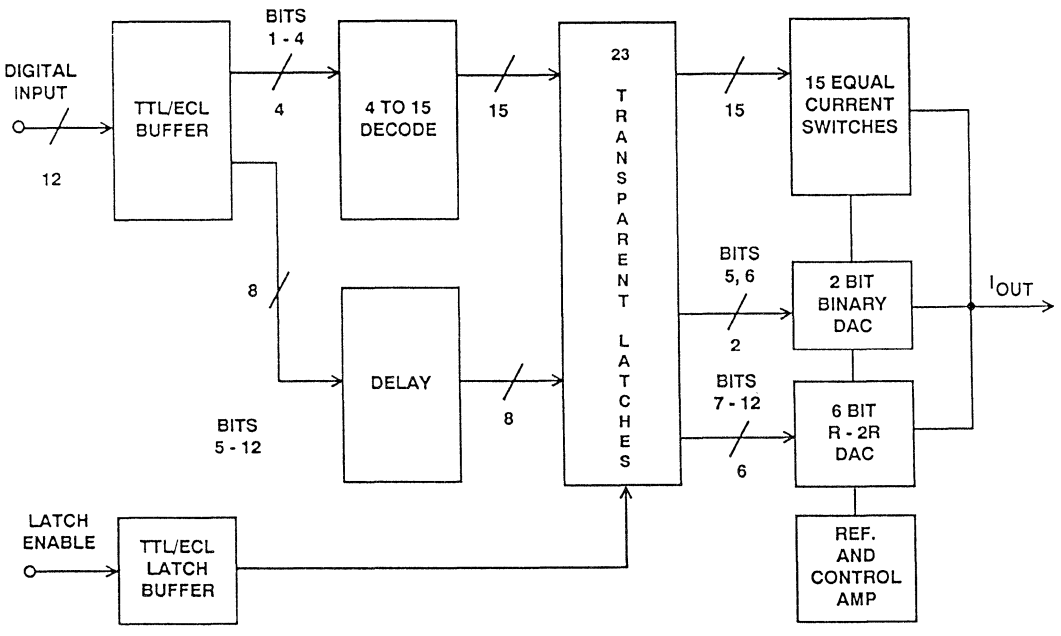
The scheme shown in Figure 9.16 is not practical for high resolution 12-bit reconstruction DACs, but a significant amount of glitch impulse reduction can be achieved by applying the concept to the first few MSBs. A block diagram of the AD9712/13 12-bit reconstruction DAC is shown in Figure 9.17 to illustrate the segmented architecture. The four MSBs are decoded into a "thermometer" code which drives 15 equally weighted current switches after latching. The remaining bits are obtained using binary current weighting (bits 5 and 6) and R-2R current division (bits 7-12). Segmentation of the four MSBs reduces the effects of the midscale glitch impulse by a factor of 16 compared to the glitch which would result if straight binary decoding were employed. This technique used in the AD9712 should result in a midscale glitch impulse area of less than 50pV-sec.

Typical harmonic distortion performance at various update rates for the AD-9712 is given in Figure 9.18.



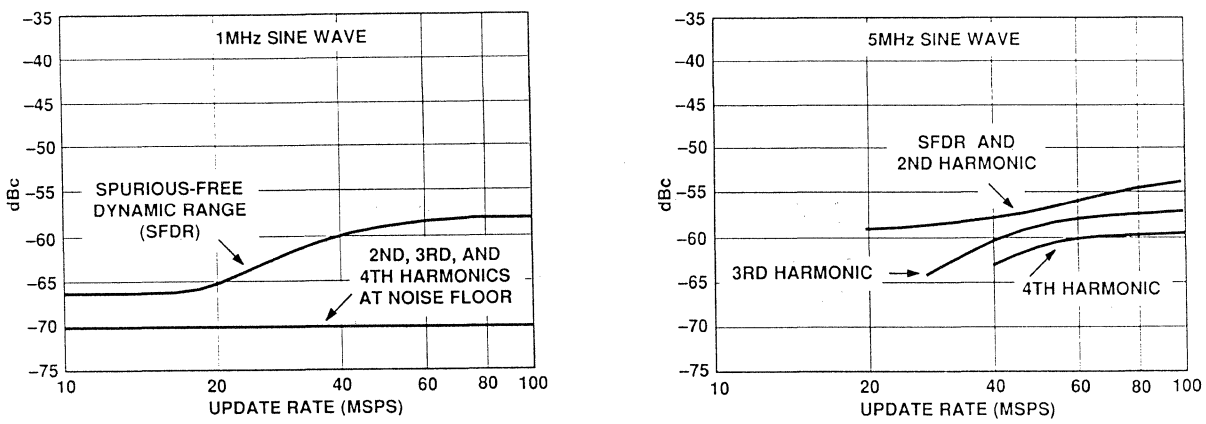
IDEAL DAC FOR MINIMUM GLITCH

Figure 9.16



AD-9712/9713 BLOCK DIAGRAM

Figure 9.17

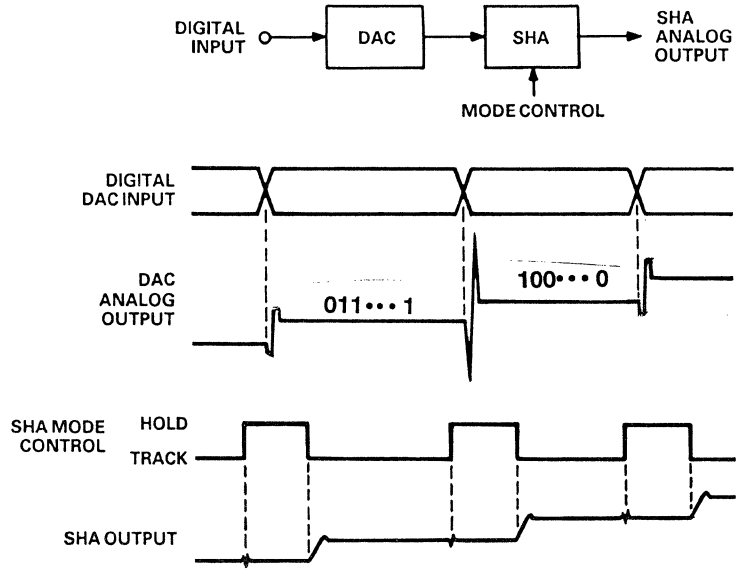


AD9712 HARMONIC DISTORTION

Figure 9.18

DEGLITCHING USING SHAS

SHAs can be used to deglitch DACs as shown in Figure 9.19. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are code-independent and occur at the update frequency, hence, they are easily filterable.

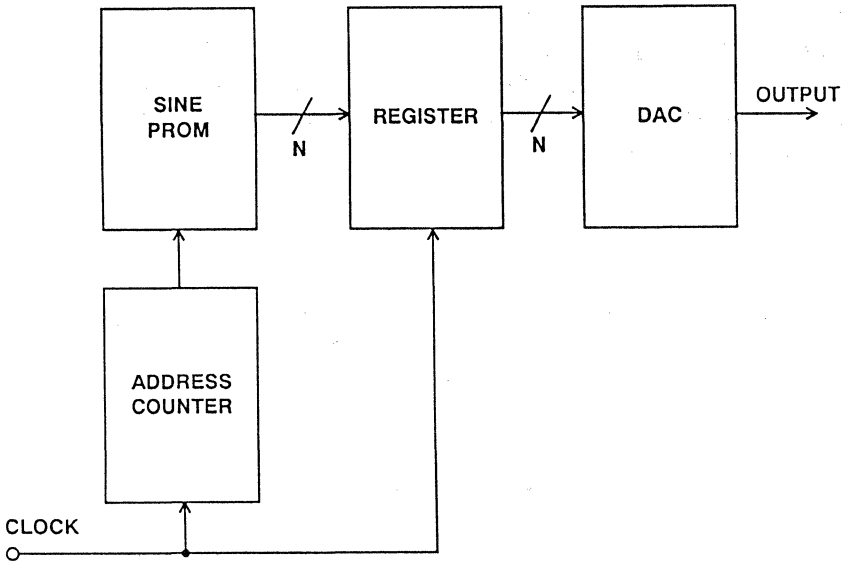


SHA DEGLITCHING

Figure 9.19

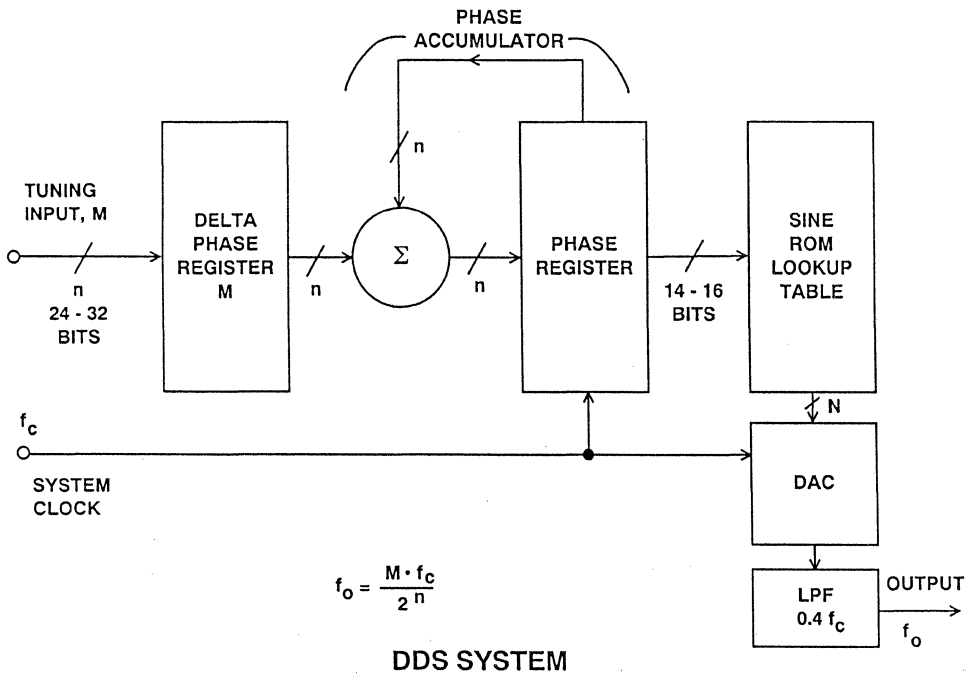
DIRECT DIGITAL SYNTHESIS TECHNIQUES

A simple circuit for generating a sinewave using a PROM and a DAC is shown in Figure 9.20. Each location in the PROM corresponds to a discrete sample of the sinewave. Note that the PROM must contain an integer number of cycles in order to prevent a discontinuity from occurring when the PROM "rolls over". In addition, the PROM should contain a prime integer number of cycles of the sinewave so that the quantization noise is not concentrated in the harmonics of the fundamental. This process is analogous to selecting the proper input sinewave frequency when performing coherent DSP testing on an A/D converter. The simple approach described above is severely limited because the sinewave frequency can only be changed by varying the clock rate or by reprogramming the PROM.



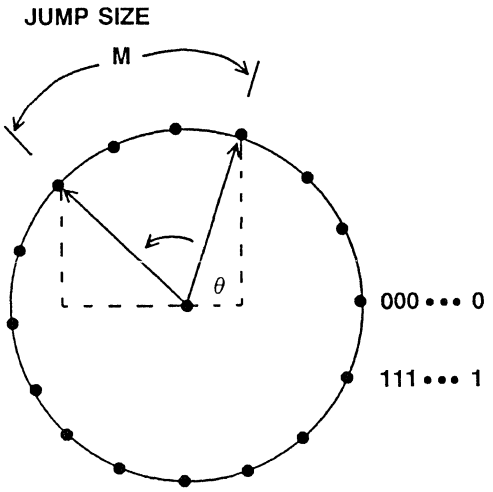
SIMPLE DDS SYSTEM

Figure 9.20



DDS SYSTEM

Figure 9.21



n	NUMBER OF POINTS
8	256
12	4096
16	65536
20	1048576
24	16777216
28	268435456
32	4294967296

DIGITAL PHASE CIRCLE

$$f_o = \frac{M \cdot f_C}{2^n}$$

PHASE ACCUMULATOR OSCILLATOR

Figure 9.22

A much more flexible scheme is shown in Figure 9.21 and is the basis of modern DDS techniques. In order to understand how it works, first consider a sinewave oscillation as a vector rotating around a phase circle as shown in Figure 9.22. Each point on the phase circle corresponds to a particular point on the output waveform. As the vector travels around the phase circle, the corresponding output waveform is generated. One revolution on the phase circle corresponds to one complete cycle of the sinewave. A phase accumulator is used to perform the linear motion around the phase circle. The number of discrete points on the phase circle is determined by the resolution of the phase accumulator. For an n-bit accumulator, there are 2^n number of points on the phase circle. The digital word in the delta phase register (M) represents the "jump size" between updates. It commands the phase accumulator to jump by M number of points on the phase circle each time the system is clocked. If M is the number stored in the delta phase register, f_C is the clock frequency, and n is the phase accumulator resolution, then the frequency of rotation around the phase circle (the output frequency) is given by

$$f_O = \frac{M \cdot f_C}{2^n}$$

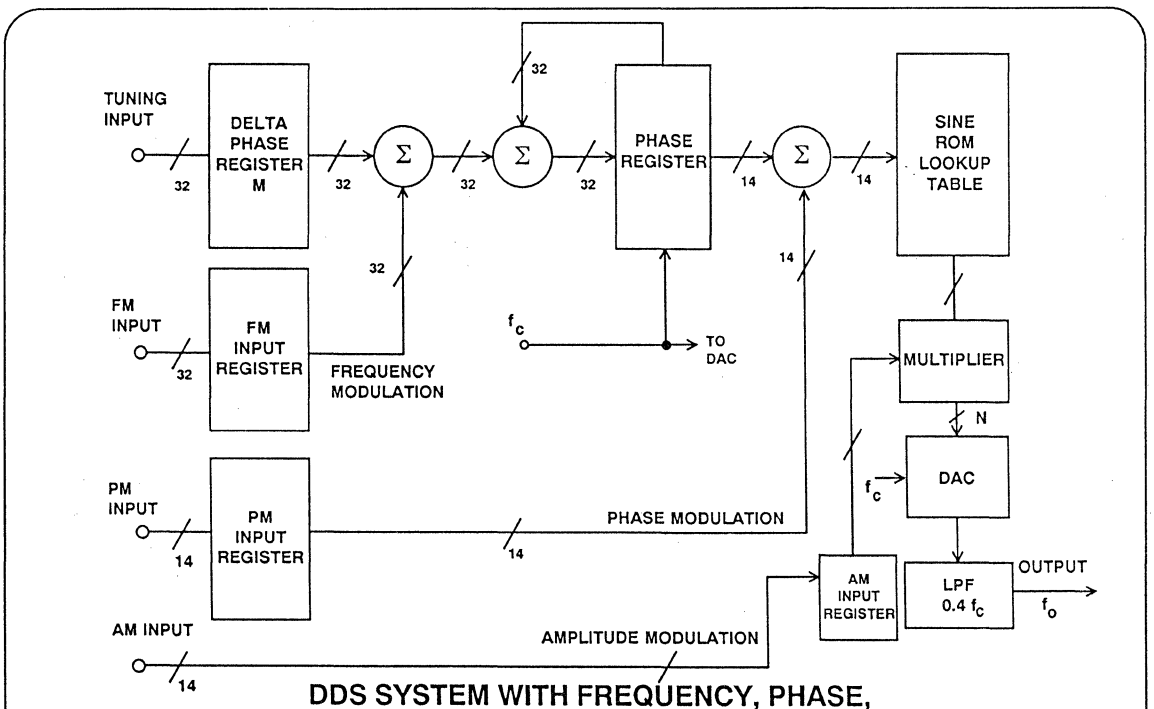
which is known as the DDS "tuning equation".

Phase Truncation

Note that the frequency resolution of the system is $f_C/2^n$ which represents the smallest incremental frequency capable of being produced. The delta-phase register and the accumulator are typically 24 to 32 bits wide.

The output of the phase accumulator drives the address input of a sinewave ROM lookup table in which is stored amplitude information for exactly one cycle of a sinewave. The ROM thus acts as a phase-to-sine amplitude converter. The output of the ROM drives a DAC which then reconstructs the analog sinewave. Ideally, there is a specific value in the ROM lookup table for each possible phase angle in the accumulator. This can easily result in the need for extremely large ROMS. In practice, the phase data is usually truncated to reduce the ROM size. The amount of phase resolution directly affects the spectral purity of the output sinewave. If the phase information is truncated to 16-bits, the largest phase spur is about 96dB below the fundamental reconstructed sinewave frequency.

In practice, the phase information is typically truncated to 14-16 bits. A DDS system having 32-bits in the delta-phase register and the accumulator and 16-bits of phase information driving the sine ROM is capable of taxing the state of the art in 12-bit DACs at system clock rates of 30 MHz. Using a low glitch 12-bit DAC such as the AD9712/13 will allow the spurs due to phase truncation and glitch impulse to be kept below -70dBc at a system clock rate up to 30 MHz.



DDS SYSTEM WITH FREQUENCY, PHASE, AND AMPLITUDE MODULATION

Figure 9.23

A DDS system is capable of generating frequencies ranging from $f_C/2^n$ to $f_C/2$. However, the steepness of the rolloff of the lowpass filter determines the practical upper limit of the output frequency to about 40% of the system clock rate.

If the output frequency is not relatively prime to the system clock frequency, spurious quantization noise will be concentrated in the harmonics of the output frequency. The use of a prime number in the delta-phase register will avoid this effect.

Figure 9.23 shows a DDS system which is capable of frequency, phase, and amplitude modulation. Frequency modulation is achieved by inserting an adder between the delta phase register and the phase accumulator. The frequency modulator has the same resolution as the phase accumulator thereby enabling frequency modulation over the entire tuning bandwidth. Phase modulation is achieved by inserting an adder after the phase accumulator. Amplitude modulation is achieved by inserting a digital multiplier after the sine ROM lookup table.

A summary of frequency synthesis figures of merit is given in Figure 9.24 and applications for DDS systems are given in Figure 9.25.

A block diagram of a new 300 MHz DDS chip, the AD9950, is shown in Figure 9.26.

FREQUENCY SYNTHESIS FIGURES OF MERIT

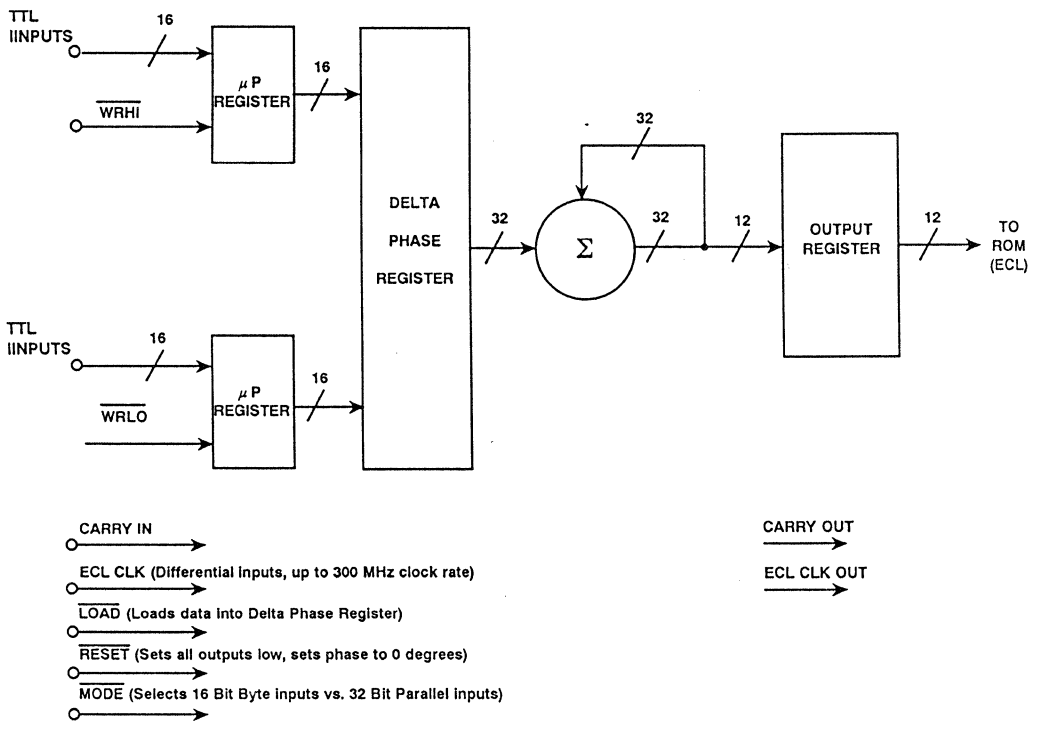
- Tuning Speed
- Resolution (Frequency Step Size)
- Tuning Bandwidth
- Spurious Signal Suppression
- Harmonic Suppression
- Phase Noise

Figure 9.24

DDS APPLICATIONS

- Radio Receiver Local Oscillators
- Signal Generators, Instrumentation
- Frequency Hopping Radios
- Communication Systems
- QAM Systems
- Radar Systems

Figure 9.25



AD9950 BLOCK DIAGRAM

Figure 9.26

HIGH SPEED RECONSTRUCTION DAC SELECTION GUIDE

MODEL	RESOLUTION	SETTLING TIME	COMMENTS
AD9768	8 BITS	5ns	ECL, 20mA Output Current, Int. Ref.
AD565A	12 BITS	250ns	TTL, 5mA Output Current, Int. Ref.
AD568	12 BITS	35ns	TTL, 10mA Output Current, Int. Ref..
AD9712/9713	12 BITS	30ns	ECL/TTL Low Glitch Reconstruction DAC - 100MHz Input Latch

Figure 9.27

SECTION X

COMPUTER GRAPHICS AND RAM-DACs

COMPUTER GRAPHICS AND RAM-DACS

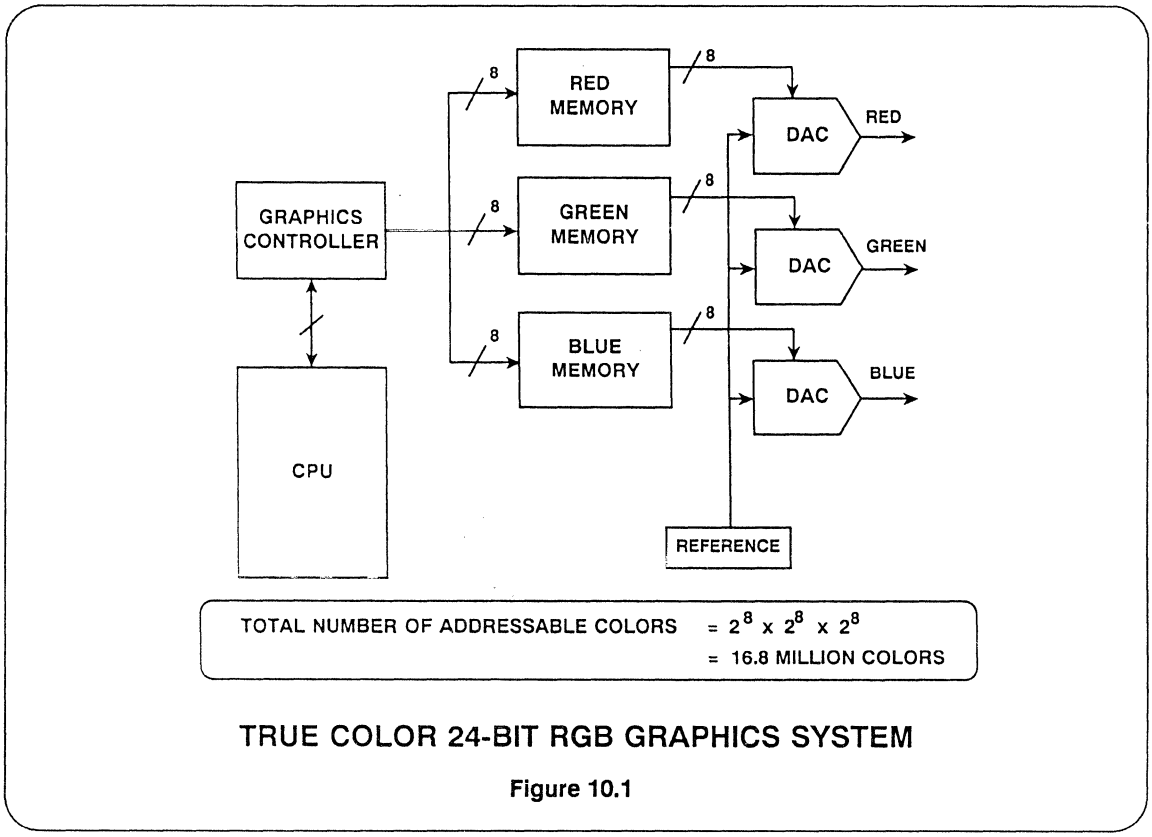
INTRODUCTION

Just as advances in microprocessor technology have been able to bring the processing power of a mainframe to desktop and laptop computers, the advances made in digital-to-analog converters have increased the performance and integration to a point where photorealistic rendering is now becoming commonplace on PCs. The drive towards larger displays, windows based graphics systems, higher resolution, and lower cost is expanding the options available to designers. This section deals with Video DACs and RAM-DACS and methods to enhance computer graphics systems.

COMPUTER COLOR GRAPHICS SYSTEMS

There are several system architectures which may be used to build a graphics system. The most general approach is illustrated in Figure 10.1. It consists of the host microprocessor, a graphics controller, three color memory banks or frame buffer, one for each of the primary colors red, green and blue (only one for monochrome systems), three high speed video DACs (only one for monochrome), and a voltage reference. The microprocessor provides the image information to the graphics controller. This information typically includes position and color information. The graphics controller is responsible for interpreting this information and adding the required output signals such as sync, blank, and memory management tasks. The memory holds the intensity information for each pixel on the screen. The DACs use the words in the memory and information from the memory controller to write the pixel information to the monitor. The reference provides a stable voltage to the DACs.

This system, when used with 8 bits for each DAC, is known as a 24 bit true color system. A total of 16.8 million addressable colors can be displayed simultaneously. The system is straightforward, but is very memory and bus intensive since each DAC must have a frame buffer associated with it. The memory requirements are based on the CRT resolution and is equal to the number of horizontal pixels times the number of vertical pixels. For an 800 x 600 Enhanced VGA display, this requires 480,000 bytes per DAC. The price of photorealistic rendering is even higher at over 4MB per DAC.



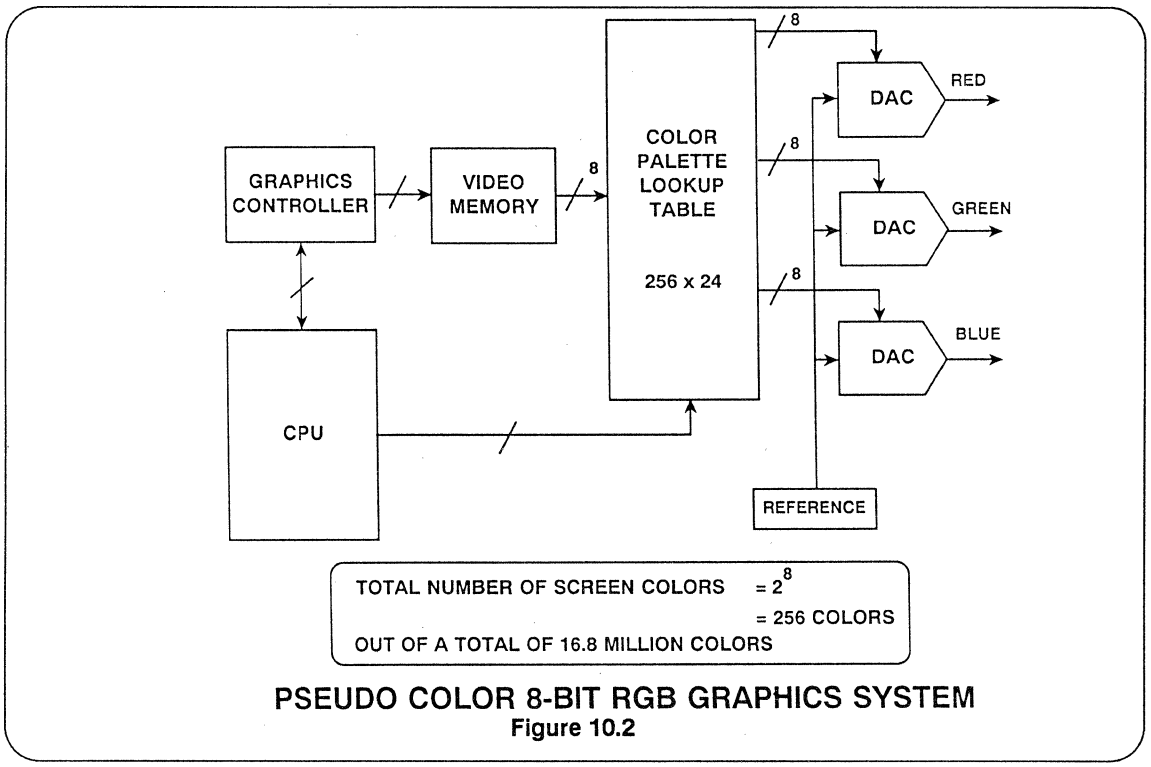
TRUE COLOR 24-BIT RGB GRAPHICS SYSTEM

Figure 10.1

COLOR LOOK-UP TABLES

In an effort to reduce system costs while maintaining a high degree of flexibility, an alternative configuration was developed. Known as a pseudo-color system, the architecture shown in Figure 10.2 reduces memory requirements to 1/3 of the true color system.

The color look-up table (CLUT) allows a total of 2^N simultaneously displayed colors to be used out of a total of $2^{M \bullet 3}$ available colors, where N is the number of address bits of the CLUT and M is the number of bits of each DAC. For an 8 bit VGA pseudo-color system, 256 colors may be displayed on the screen at once selected from a palette of 16.8 million colors. For the majority of business and home applications, this is sufficient.



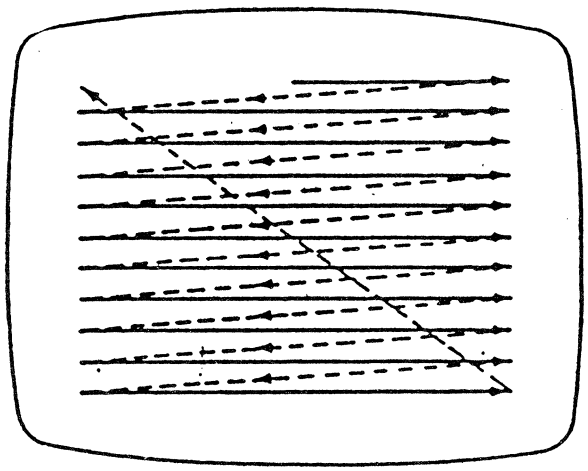
PSEUDO COLOR 8-BIT RGB GRAPHICS SYSTEM
Figure 10.2

VIDEO FORMATS

Standard computer graphics monitors, like television monitors, use a display technique known as raster scan. This technique writes information to the screen line by line, left to right, top to bottom as shown in Figure 10.3. The monitor must receive a great deal of information to display a complete picture. Not only must the intensive information for each pixel be present in the signal, but information must be provided to determine when a new line needs to start (HSYNC) and when a new picture frame should start (VSYNC). The computer industry has generally standardized around EIA standard RS-343A.

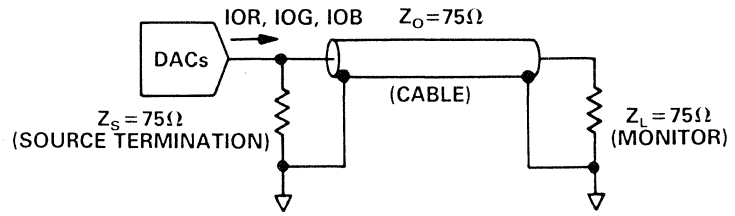
Figure 10.4 shows the RS-343A voltage standard. There are three regions within the signal, Sync, Setup and Intensity. Three signals are required by a color monitor to drive the Red, Blue and Green guns. However most monitors only require that the sync signal be present on the Green signal. Peak to peak signal levels on the green signal are 140 IRE units within the region between the blank and the reference white levels of the signal. The red and blue peak signals have 100 IRE units or 0.714 Volts, lower than green because there is no sync info.

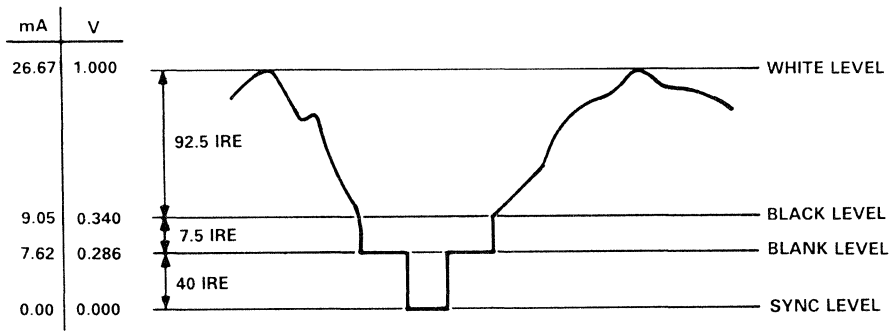
The sync region is defined as having 0.286V ± 0.05V or 40 IRE units. This portion of the signal tells the monitor when to retrace horizontally and vertically. The setup region is between the blank and black levels and has 0.054V ± 0.018V or 7.5 ± 2.5 IRE units. This portion turns off the intensity to the guns during retrace. Blank level is below reference black to insure no writing to the screen even when the screen intensity is turned up. Finally, the intensity information consisting of 0.660V ± 0.018V or 92.5 ± 2.5 IRE units, lies between reference black and reference white levels. It is this portion of the signal which is controlled by the DAC. Thus, the maximum number of colors available is determined by the resolution of the DAC, as is illustrated by Figure 10.5.



RASTER SCAN DISPLAY

Figure 10.3





RS-343A VIDEO OUTPUT

Figure 10.4

MAXIMUM NUMBER OF AVAILABLE COLOR PALETTES

DAC BITS N	DAC OUTPUT LEVELS 2^N	AVAILABLE COLOR PALETTES 2^{3N}
1	2	8
2	4	16
3	8	512
4	16	4,096
5	32	32,768
6	64	262,144
7	128	2,097,152
8	256	16,777,216

Figure 10.5

SPECIFICATIONS

It is important to be aware of the effect of a DAC specification on display performance. Important specifications include number of bits and differential non-linearity (DNL), update rise, rise and fall times, settling time, glitch impulse energy, feedthrough rejection and drive capability.

As was shown in the previous section, the number of bits a DAC has determines the number of potentially available colors that can be displayed. This assumes that the DAC has a DNL of ±1 LSB or better. The lower the DNL, the higher the accuracy for controlling color and intensity.

The update rate is typically the gateing specification used in determining if a DAC is fast enough to be used to drive a monitor of a given resolution. Figure 10.6 shows the equation for calculating the required video DAC update rate for a non-interlaced screen. The retrace factor accounts for the fact that the display is blanked for the horizontal and vertical retrace which typically account for about 25% to 30% of a given frame time. Figure 10.7 shows the DAC update rate required for various monitor resolutions.

VIDEO DAC UPDATE RATE

DAC update rate (Hz) = (Pixels/Line) • (Lines/Frame) • (60) • 1.30

- **Pixels/Line = Horizontal Resolution**
- **Lines/Frame = Vertical Resolution**
- **1.30 = Retrace Factor**
- **60 Hz = Refresh Rate**

Figure 10.6

GRAPHICS RESOLUTIONS

RESOLUTION	UPDATE	APPLICATION
500 X 250	10 MHz	LOW-END PC (HOME COMPUTERS)
640 X 480	25 MHz	PC
800 X 600	38 MHz	PC
768 X 576	35 MHz	PC
1024 X 768	65 MHz	PC AND LOW-END WORKSTATIONS
1024 X 1024	85 MHz	LOW-END WORKSTATIONS
1280 X 1024	105 MHz	CAD/CAE AND WORKSTATIONS
1500 X 1024	125 MHz	3D IMAGING AND HIGH-END WORKSTATIONS
1500 X 1500	180 MHz	3D IMAGING
2048 X 2048	330 MHz	PHOTO-QUALITY

60 Hz NON-INTERLACE REFRESH RATE

Figure 10.7

The time it takes for the output of a DAC to transition from 10% to 90% of the full scale range is known as rise time (fall time is from 90% to 10%). Rise and fall times must be small for high update rate DACs. Settling time is the time it takes the output to transition from one band and settle within another band. Settling time affects the performance of a color graphics system only if it is longer than the pixel interval, in which case, depending on phosphor characteristics, colors may not be accurately rendered. Additionally, the settling time will be smaller for higher speed DACs.

Glitch impulse area was covered extensively in Section IX of this seminar. Glitching can cause the signals transmitted to the monitor to have an erroneous value, thereby causing changes in color or intensity and can even create ghosts. When trying to minimize glitching, first pick a DAC with low glitch impulse area. Second, choosing the correct logic family to control the DAC is essential. Lastly, deskewing the digital inputs and controls may be of help as was pointed out in Section IX.

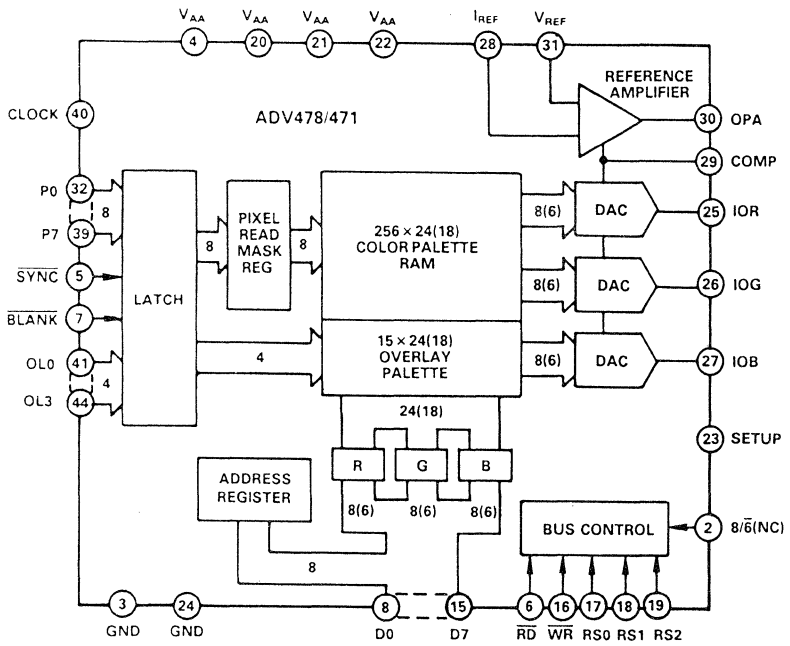
Feedthrough of either the clock or the digital data can result in noise at the output of the DAC. Feedthrough rejection tends to decrease as frequencies go higher, and therefore at high edge rates. To minimize feedthrough, use of slower speed logic can help reduce feedthrough noise, but may result in higher glitch impulse in video DACs.

In order to minimize the ghosting and distortion caused by impedance mismatch at the output, the DAC should be capable of driving a doubly terminated 75 ohm loads to RS-343A levels as shown in Figure 10.4.

RAM-DACs

The development of advanced CMOS processes has allowed the integration of the DACs, CLUT RAM, reference and logic on a single chip. Figure 10.8 shows a block diagram of the ADV478/471, pseudo-color, VGA compatible Video RAM-DACs. integrated into these devices are three DACs, color look-up table comprised of the pixel palette RAM and the overlay palette RAM, various latches, registers, control logic and a reference.

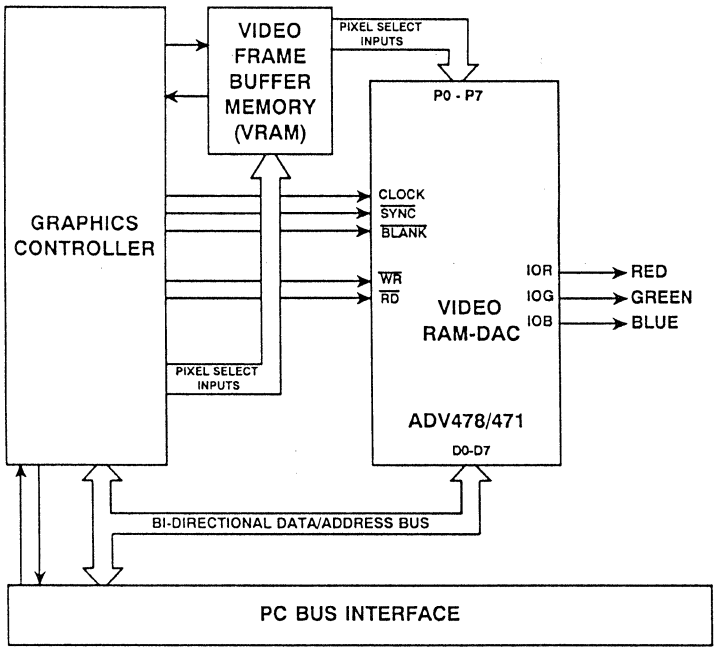
The colors associated with a particular image are loaded into the color palette RAMS through the microprocessor bus. VRAMs feed the image data into the pixel port at video rates. The pixel read mask register can be loaded through the pixel ports as well. Its function is to speed up simple animated renderings, as explained in the application note which appears at the end of this chapter. Figure 10.9 shows the architecture for the IBM PS/2 and PC VGA color graphics card. Note the component count reduction that is afforded by using RAM-DAC technology over discrete implementations shown earlier.



NOTES
1. NUMBERS IN PARENTHESIS INDICATE PIN NAMES FOR THE ADV471.
2. NC = NO CONNECT

VIDEO RAM-DAC

Figure 10.8



PS/2 & PC VGA GRAPHICS SYSTEM ARCHITECTURE

Figure 10.9

USING OVERLAY PALETTES

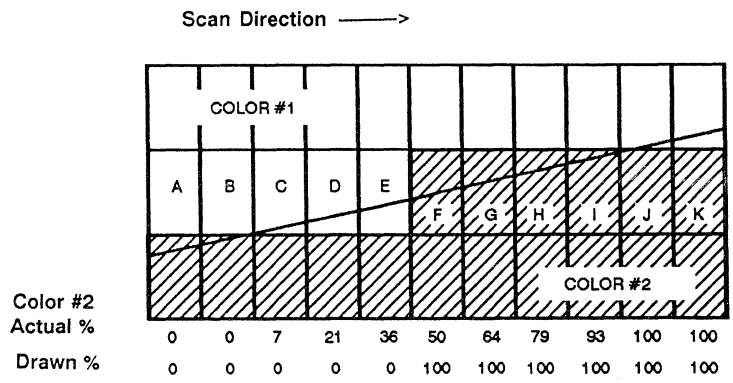
Overlay palettes are provided on RAM-DACs to reduce both hardware and software overhead when producing system level graphics shown as pull-down menus, cursors, grids, pointers, etc. The palette selection inputs control whether the pixel data will use color information from the color palette RAM or one of the overlay palettes. When at least one of the overlay bits is set high, the "Priority" overlay color addressed will be displayed instead of the color from the CLUT palettes.

By providing limited depth overlay palettes, the system software, which is generally responsible for cursor and pointer control, menus, etc., can efficiently control these graphics without altering the main graphic image which is controlled by the application software. This provides for an improvement in graphic performance, and can minimize software overhead.

By allowing independent access to the overlay palette, an EGA window may be generated over the main VGA screen image through the use of 4 bits of overlay.

CONTINUOUS EDGE GRAPHICS DIGITAL SIGNAL PROCESSOR

Graphic images of circles, lines and other objects are rendered on the monitor in a best fit method to accommodate the finite size of a pixel. A pixel is on when an object occupies 50% or more of the pixel. The pixel is off if the object crosses over less than 50% of the pixel. This graphic fact of life produces images which have jagged edges. This effect is referred to as Aliasing, and Figure 10.10 illustrates the problem. Even with a very high resolution display, the eye can quickly perceive the rough edge.

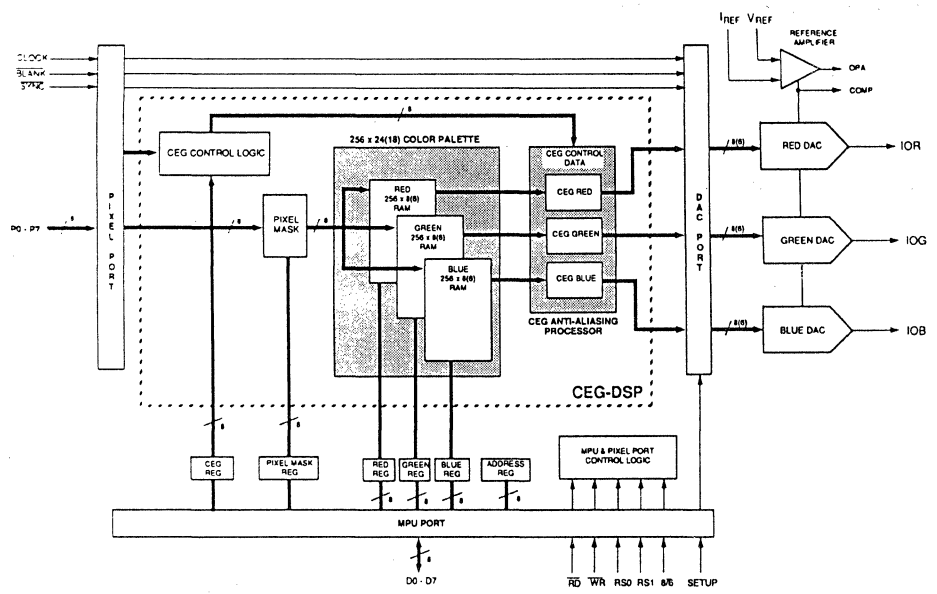


CONVENTIONAL PIXEL COVERAGE WITH ALIASING

Figure 10.10

A new device from ANALOG DEVICES dramatically improves the image quality of standard analog color systems by performing anti-aliasing and by effectively providing an extended color palette. The Continuous Edge Graphics - Digital Signal Processors (CEG-DSP) combine three matched DACs, a Color Look-up Table (CLUT), Pixel mask and a reference as shown in Figure 10.11. For designs which do not use the overlay palette, the ADV7148/ADV7141 are pin and functionally compatible with the ADV476/ADV471 and the ADV7146 is pin and functionally compatible with the ADV476 and the INMOS171/176.

The CEG achieves anti-aliasing by being able to display pixels as the linear mix of two colors from the color look-up table



CONTINUOUS EDGE GRAPHICS
DIGITAL SIGNAL PROCESSOR
Figure 10.11

(CLUT). The natural color integration of the human eye gives the display the smoothing effect as shown in Figure 10.12. When the CEG powers up, it is in a non-CEG mode, i.e., it is in a VGA compatible RAM-DAC mode. By writing a particular code sequence into the device via the MPU port, the CEG mode may be activated. In the CEG mode, the device computes the real-time weighted average on each of the primary colors which are read out of the CLUT. This computation takes the form

$$P_{MC} = [MIX \bullet P_{N-1}] + [(1\text{-}MIX) \bullet P_N],$$

where P_{MC} = Mixed Color

P_N = New Pixel Color

P_{N-1} = Previous Pixel Color

MIX = Ratio of Previous Color to New Color

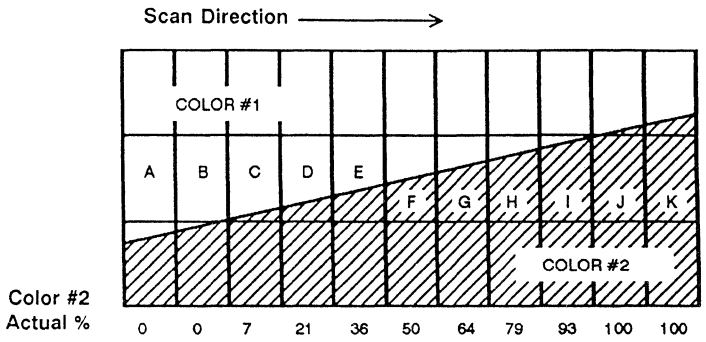
or alternatively,

Mixed color = (Ratio of the Previous Color • Previous Color) + (Ratio of the New Color • New Color).

These mixed colors, one per DAC (Red, Green, Blue), are then input into a gamma correction circuit. The outputs then drive the three DACs.

In addition to the anti-aliasing effect the CEG provides, the linear mixing of colors effectively extends the number of simultaneously available colors. This is of particular importance to applications involving photoquality rendering and solids modeling. The blending of colors allows

for the perception of much greater depth. Mixed colors, one per DAC (Red, Green, Blue), are then input into a gamma correction circuit. The outputs then drive the three DACs.



USING CEG DSP TO ELIMINATE ALIASING

Figure 10.12

VIDEO DAC SELECTION GUIDE

MODEL	RESOLUTION	UPDATE RATE	COMMENTS
AD9702	4 BITS	125 MHz	RGB Output, TTL or ECL
AD9700	8 BITS	100 MHz	ECL, Single -5.2V Supply
AD9701	8 BITS	225 MHz	ECL, Single -5.2V Supply
AD9703	8 BITS	300 MHz	ECL, Single -5.2V Supply
ADV7120	8 BITS	30, 50, 80 MHz	CMOS Triple DAC
ADV7121	10 BITS	30, 50, 80 MHz	CMOS Triple HDTV DAC, 40 Pin DIP
ADV7122	10 BITS	30, 50, 80 MHz	CMOS Triple HDTV DAC, Sync and Blanking, 44 Pin PLCC

Figure 10.13

RAM-DAC SELECTION GUIDE

MODEL	RESOLUTION	UPDATE RATE	COMMENTS
ADV471	6 BITS	35, 50, 80 MHz	CMOS Triple Color Palette RAM-DAC
ADV478	8 BITS	35, 50, 80 MHz	CMOS Triple Color Palette RAM-DAC
ADV453	8 BITS	40, 60 MHz	CMOS Triple Color Palette RAM-DAC
ADV476	6 BITS	35, 50, 66 MHz	CMOS Triple Color Palette RAM-DAC. Plug-in Replacement for INMOS 171/176
ADV7150	10 BITS	85, 110, 135, 170 MHz	CMOS 24 Bit True Color Triple Palette RAM-DAC
ADV7151	10 BITS	85, 110, 135, 170 MHz	CMOS Pseudo Color Triple Palette RAM-DAC
ADV7148	8 BITS	35, 50, 66 MHz	CMOS CEG DSP Triple Palette RAM-DAC
ADV7141	8 BITS	35, 50, 66 MHz	CMOS CEG DSP Triple Palette RAM-DAC
ADV7146	6 BITS	35, 50, 66 MHz	CMOS CEG DSP Triple Palette RAM-DAC. Plug-in Replacement for INMOS 171/176

Figure 10.14

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2. W. A. Kester, "Test Setups Judge Speed of Ultrafast 8-Bit DACs", **Electronic Design**, May 14, 1981.

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4. Tom Tice, "8-Bit, 300 MHz Monolithic D/A Converter for Displays", **Analog Dialogue**, 21-1, 1987.

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6. Bill Slattery and John Wynne, "Design and Layout of a Video Graphics System for Reduced EMI", Analog Devices, E1309-15-10/89, Included in this Section.

7. Bill Slattery and Eamonn Gormley, "Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs", Analog Devices, E1316-15-10/89, Included in this Section.

ANALOG DEVICES

APPLICATION NOTE

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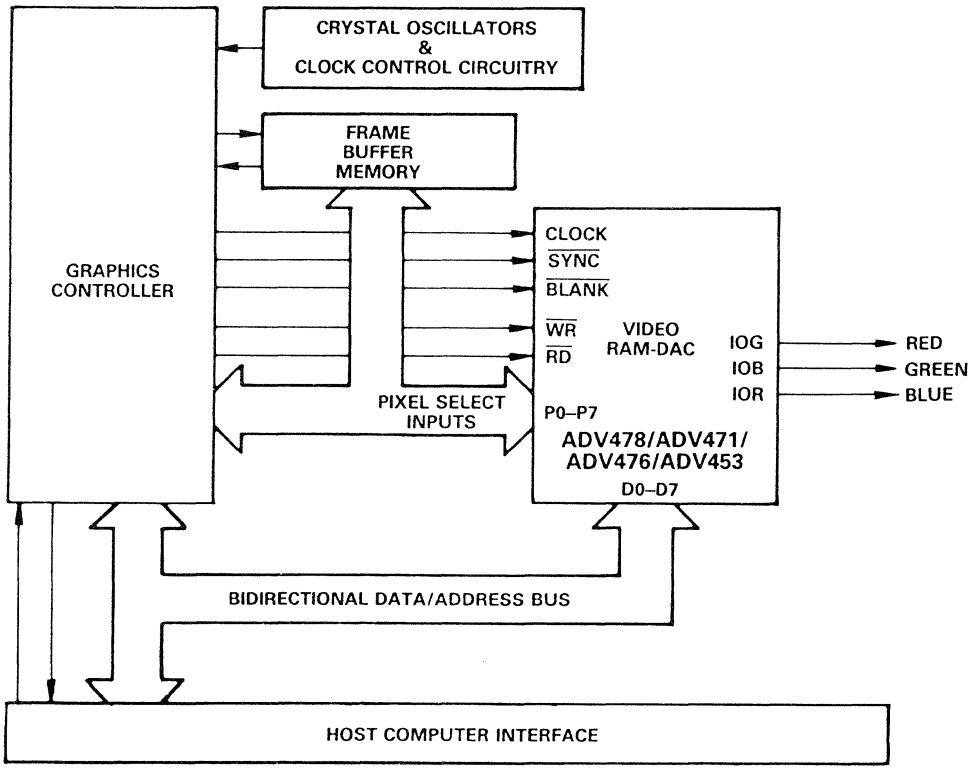
Design and Layout of a Video Graphics System for Reduced EMI

by Bill Slattery & John Wynne

The availability of low cost, high performance video RAM-DACs is a key element in the spread of personal computers into application areas previously considered the preserve of expensive, high-end computer systems. Applications such as Computer Aided Engineering (CAE), Computer Aided Design (CAD), Solids Modelling, Desktop Publishing, etc., are becoming more widespread as the cost of the necessary hardware drops. Successfully incorporating a video RAM-DAC into a personal computer or onto a video graphics plug-in board is not difficult once some basic concepts are grasped and some simple guidelines followed.

This application note is intended as a guide to the design of a video graphics system in terms of Electromagnetic Compatibility (EMC). EMC design will be considered as the technique of reducing radiated emissions and Electromagnetic Interference (EMI) from a high speed video graphics system. EMC implies that the system should not electrically or magnetically interfere with its surroundings, and conversely, the surroundings should not interfere with the operation of the system. In order to provide control of EMI in the radio spectrum, government agencies and other international organizations have established limits relating to EMI, most notably, the U.S. government's FCC Part 15.



Simplified Block Diagram of a Typical Graphics System Using a Video RAM-DAC

OVERVIEW

This application note is divided into a number of sections as outlined below:

1. International EMI Regulatory Bodies – guidelines, testing and radiation limits.
2. System Noise Identification – identifying various sources of noise in a system.
3. PCB Layout & Design – component placement, multilayer boards, grounding, shielding and filtering components
4. Practical example of a VGA board design and associated FCC Testing.

REGULATIONS CONTROLLING EMI

The ultimate goal which must be achieved if EMC design is to be considered successful is the attainment of "Agency Certification." A number of international government agencies impose strict criteria on the allowable electromagnetic interference that electronic apparatus can emit. Electronic apparatus is required by law to conform to these agency limits, or else face severe government penalties.

In the United States, the Federal Communications Commission (FCC) is the national regulatory body which sets down strict controls on interference from computing devices. The FCC has divided computer interference into two principal types. The first type, and by far the most demanding of the two, deals with radiated emissions over the frequency range of 30 MHz to 1 GHz. Radiated emissions from personal computers, in a commercial environment, must conform to the limits set out for a Class B computing device pursuant to Subpart J of Part 15 of the FCC Rules. Table I lists the maximum permissible radiation from such devices, measured in terms of Electric Field Strength.

Frequency MHz	Distance Meters	Field Strength* μV/Meter
30–88	3	100
88–216	3	150
216–1000	3	200

Table I. Radiation Limits for Class B Computing Devices According to FCC Rules

The second type of emission deals with interference fed back onto the power lines. The FCC conduction limit on this interference is 250 μV* maximum over the frequency range 450 kHz to 30 MHz. This type of interference is heavily influenced by the design of the switched-mode power supply within the computer cabinet.

FCC Certification is awarded on the submission to the FCC of a complete report which consists of acceptable test results as well as a detailed description of the test and measurement procedure. Testing has to be carried out by an FCC-accredited test laboratory.

Class C Certification, which has less stringent limits, is allowable in certain commercial and industrial applications.

A list of the various international agencies is given in the Reference section. All agencies have very similar requirements to those of the FCC.

NOISE SOURCES

Identification of noise sources or potential noise sources in a system is the first and probably the most valuable step that has to be taken for successful EMI design.

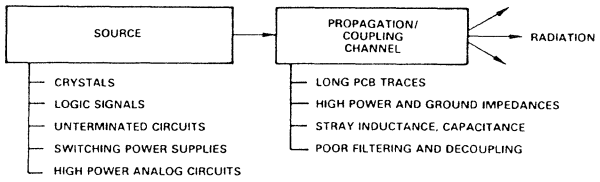


Figure 1. Noise Model of a Video Graphics System

It may even be possible to eliminate a particular noisy circuit completely from the design thus avoiding the later need for filtering. Unfortunately, many possible sources of noise cannot be eliminated from the design, but by being aware of their existence, their effects can be minimized at the source and in the coupling channel by optimum filtering and decoupling. Some of the inherent sources of noise in a video graphics system include:

1. Crystal oscillator and clock frequency division circuits.
2. Circuits with fast transition times (rise/fall times), e.g., logic families that are unnecessarily fast.
3. Unterminated circuits.
4. Stray inductances/capacitances.
5. Switching power supplies.
6. High power analog circuits such as video RAM-DACs.

Crystal Oscillators & Associated Circuitry

A video system usually contains a number of crystal oscillators and associated clock and pixel data circuits, which are required to achieve various on-screen pixel resolutions. In a VGA system, for example, there could be as many as five crystal oscillators varying in frequency from 25 MHz to 65 MHz, and maybe up to 80 MHz. These crystal oscillators and their associated circuitry tend to be rich in unwanted noise and harmonic components. They can be a prime source in the generation of EMI if some basic guidelines are not followed.

***Measured pursuant to §15.840 of the FCC Rules.**

Some of the important actions are:

1. Place crystal oscillator circuits as far as possible from analog circuitry and video output connectors.
2. Isolate power supply to crystals through the use of ferrite beads.
3. Avoid the mixing of clock buffers and other logic in the same IC package.
4. Use several low power data drivers or buffers for clock and pixel data lines distributed throughout the board, in preference to using a single high power driver.

With regard to the crystal oscillators themselves, the critical aspects which must be considered include the wave shape and the transition time (rise/fall time). Figure 2 is a plot of the output frequency spectrum of a typical 28.5 MHz crystal oscillator. It shows the amplitude of the harmonic components relative to the fundamental. It can be clearly seen that although the crystal's fundamental frequency lies outside the FCC's lower limit of 30 MHz, for radiated EMI, higher-order harmonic components exist throughout the FCC-controlled band. The frequency of the crystal oscillators should be kept to the required minimum, and transition times should be kept as slow as possible. This reduces the amplitude of unwanted harmonics, while still satisfying system functional performance needs.

The clock circuitry, which includes crystal oscillators and pixel data lines, is the primary source of most of a system's noise. Keeping this circuitry as far and as isolated as possible from other circuitry, especially analog circuitry, is all-important. On the other hand, it could be argued that by running long pixel data and clock lines from such circuitry to the Video RAM-DAC in itself is not desirable. Long lines increase noise coupling to other parts of the system. A tradeoff between length of pixel lines and the placement of high speed clock circuitry must be considered. The designer must attempt to optimize these two competing goals. As was mentioned earlier, the use of multiple low power buffers will help to ease such a conflict. A distance of less that three inches between buffers would be desirable in such circumstances.

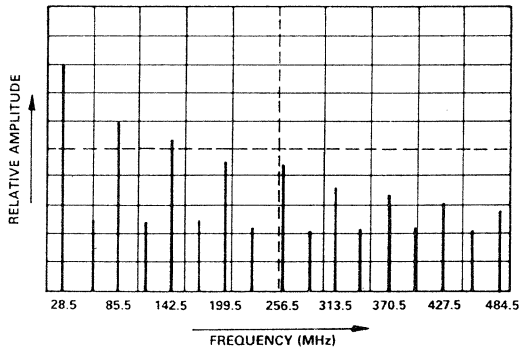


Figure 2. Magnitude of Harmonic Components Relative to the Fundamental for a 28.5 MHz Crystal Oscillator

Other Noise Sources

A number of other noise generators can be easily identified. Circuits with fast transition times including memory chips, logic circuitry and the graphics controller all contribute to the overall noise of the system. The faster the signal transition time, the greater will be the amplitude of the resulting harmonics, as was seen in the previous section relating to crystal oscillator circuits.

As a general rule, devices with the slowest possible rise/fall times that will achieve the system's tasks should be used. Table II lists some typical rise/fall times for various logic families.

Technology	IC Family	Transition Time
TTL	74	10 ns
	74LS	12 ns
	74ALS	3→20 ns
	74S	6 ns
	74AS	2→9 ns
	74F	1.2→8 ns
CMOS	74HC	20→150 ns

Table II. Comparison of Transition Times for IC Logic Families

Stray inductances and capacitances can cause signals to ring, to overshoot or undershoot the steady state voltage levels. This ringing is a source of EMI which can be minimized by keeping wires or traces short and adding series, damping resistances at the source or termination of long signal paths.

Unterminated circuits with floating signal lines should be avoided. Unwanted oscillations can result.

Power to all devices of a system is usually derived from switch-mode power supplies. While the design of the power supply is critical to the reduction of conducted noise in the FCC's band of 450 kHz up to 30 MHz, harmonics generated by the switching power supplies can extend well into the radiation frequency band and thus add to EMI.

Modern high resolution color graphics monitors are driven by analog signal levels direct from the DACs. The relatively high power, analog output levels from the Red, Green and Blue current sources of the video DAC require careful attention. As will be discussed in the PCB layout section, the power to the Video RAM-DAC should be isolated from the remainder of the PCB power plane. If noise on the high speed pixel and clock input section to the Video RAM-DAC has not been minimized, noise will be coupled through to the analog output section and onto the connecting cable to the monitor, causing this cable to act as an antenna. Filtering at the source termination of each of the three DAC outputs can be used if required to minimize the noise further. (See Appendix 1, *Three-Terminal Capacitor.*)

PRINTED CIRCUIT BOARD DESIGN

The extent of radiated emissions from a printed circuit board (PCB), will be determined by the effectiveness of the PCB to act as a propagation channel for unavoidable noise sources, its ability to couple this noise onto other circuitry, and the radiation into free space of this undesired noise. Apart altogether from a PCB's ability to radiate EMI, noise coupled from digital circuits on the board to the video RAM-DAC can adversely affect the system's functional performance.

Causes of EMI

The main sources which conduct or radiate EMI from a printed circuit board are as follows:

1. Common impedance coupling via power and ground traces.
2. Antenna loops formed by ICs and their bypass capacitors. Note that these loops also include the power and ground lead frame members within the IC packages.
3. Printed circuit board traces carrying signal currents. Note again that signal lead frame members within the IC packages are also included.
4. Crosstalk between adjoining signal traces.

Common Impedance Coupling

An example of common impedance coupling via power and ground traces is shown in Figure 3a where a number of logic gates are supplied with power over common printed circuit board traces. A typical V_{IN} input signal to one of these gates is shown in Figure 3b with the resulting transient and signal currents due to the gate switching also shown.

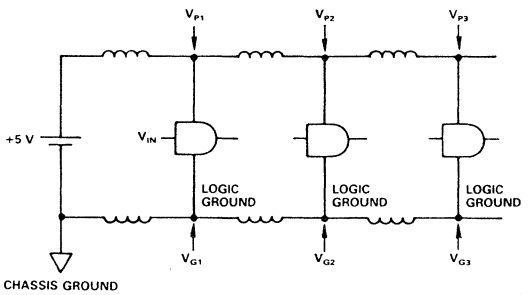


Figure 3a. Common Impedance Coupling via Power and Ground Traces

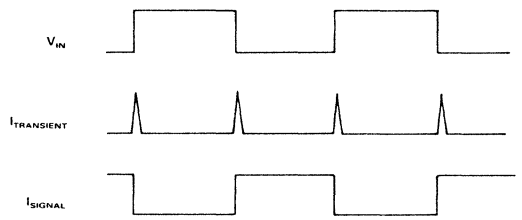


Figure 3b. Signal and Transient Currents Due to Gate Switching

The distributed trace inductances act as impedances to these switching currents spreading the resulting high frequency noise to all nodes common to the culprit. To get an idea of the magnitude of the generated high frequency noise, let's take a look at the effect of a single gate, as shown in Figure 4a. The associated worst signal current for a standard TTL gate is shown in Figure 4b.

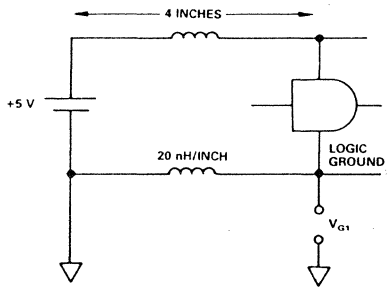


Figure 4a. Common Impedance Coupling Due to One Gate

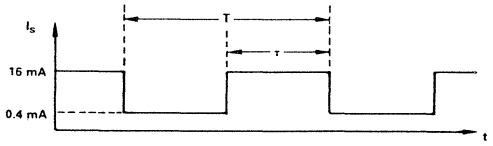


Figure 4b. Signal Current Due to TTL Gate Switching

Consider the harmonic components present in the switching signal current of Figure 4b. This assumes the gate is driving 10 standard TTL loads with a maximum sink current of 16 mA and a maximum source current of 0.4 mA.

With a mark/space ratio of τ/T and using a Fourier Series expansion, the formula for the amplitude of the nth harmonic is given by

$$I_n = \frac{2A\tau}{T}\left[\frac{Sin\left(\frac{n\pi\tau}{T}\right)}{\frac{n\pi\tau}{T}}\right]$$

where n = 1, 2, 3 . . . .

For a square wave $\tau/T = 0.5$, the amplitude of the third harmonic (n=3) is

$$I_3 = 3.4 \text{ mA, zero to peak.}$$

At 28.5 MHz, a standard VGA pixel clock frequency, the magnitude of the impedance of the ground trace in Figure 4a is given by

$$Z = [2\pi fL]$$

where f = 28.5 MHz
L = 20 nH/inch (typically)

hence Z = 3.58 Ω/inch.

At 85.5 MHz (3×28.5 MHz) the impedance is 10.74 Ω/inch. Thus the high frequency voltage at the logic

ground node of the switching gate due to the third harmonic alone is equal to

$$V_{G1} = (3.4 \times 10^{-3})(4)(10.74)\ V$$

$$= 146\ mV\ peak\ at\ 85.5\ MHz.$$

This high frequency component and other similar components will be circulated around the printed circuit board via the common ground traces. It will also appear on any cable shielding attached to this common ground trace and, depending on how efficient the cable shield is as an antenna, will be radiated into free space.

Antenna Loops

One of the most important principles of PCB layout and design for noise reduction can be described by the phrase:

"Minimize Signal Loop Areas."

In most circuit designs, we tend to think of the currents we're interested in as flowing "out" of one place, "through" some other place and "to" the target point. Unfortunately however, this often leads us to neglect to consider how these currents will eventually find their way back to their source. Ground and supply voltage points are considered "equivalent," and the fact that they are parts of a network of conductors through which currents flow and develop finite voltages is often not appreciated. These voltages can radiate to cause EMI, see Figure 5.

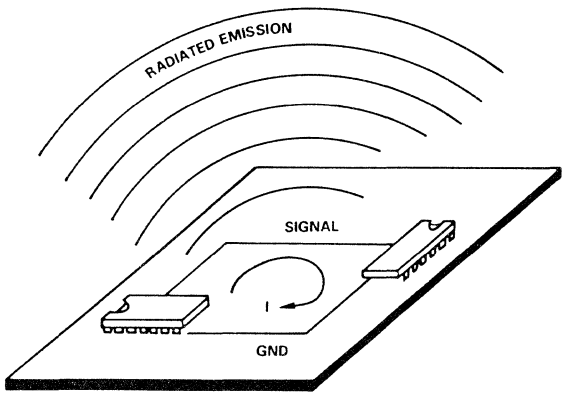


Figure 5. Currents Flowing in Large Loops Add to EMI

Voltages are generated because wires and traces do not have zero impedance due mainly to inherent inductances.

Many of the problems associated with power and ground loops can be avoided through the deployment of effective bypassing techniques.

The aim of effective bypassing is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. Figure 6a shows a poor bypass arrangement and the associated inductances due to the large loop area are illustrated in Figure 6b.

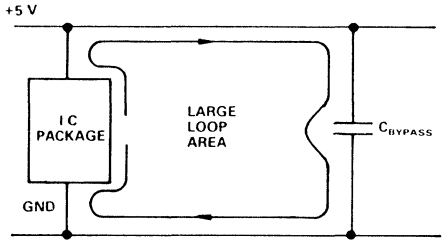


Figure 6a. Large Loop Associated with Poorly Placed Bypass Capacitor

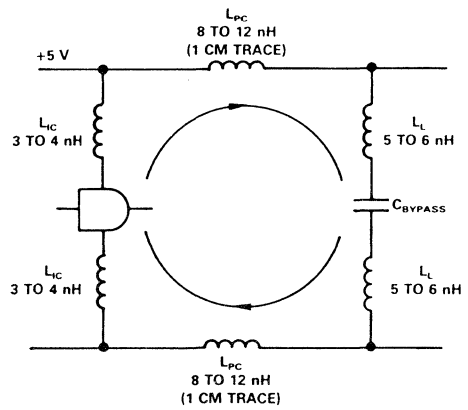


Figure 6b. Equivalent Circuit of Bypass Loop of Figure 6a

where L_L = inductance of the lead from the capacitor body to the PC board

L_{PC} = inductance of the trace between the lead arrival on the PC board and the IC pin

L_{IC} = inductance of the lead frame member carrying power within the IC package.

As well as loop inductances due to the above, the series inductance of the bypass capacitor itself must also be considered. It is well known that there is more inside a capacitor's body than a pure capacitance.

The simplified equivalent circuit of a 0.1 μF capacitor in Figure 7 shows an effective series resistance (ESR) and effective series inductance (ESL) in series with the ideal 0.1 μF capacitance.

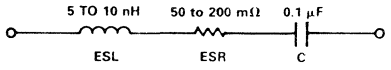


Figure 7. Equivalent Series Representation of a Bypass Capacitor

Figure 8 shows the complete inductive loop associated with the bypass circuit.

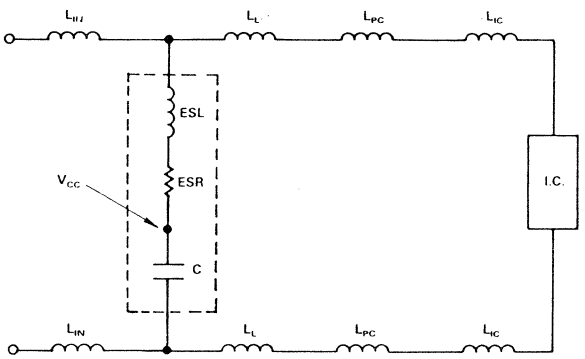


Figure 8. Inductive Loop of a Bypass Circuit

These inductances increase the total series inductance of the bypass loop and hence lower the series resonant frequency as determined by the equation:

$$f_O = \frac{1}{2\pi\sqrt{LC.}}$$

Above the series resonant frequency the impedance becomes more inductive, increasing linearly with increasing frequency. For instance, a 0.1 μF ceramic radial lead capacitor with 1/4 inch leads generally resonates around 10 MHz.

The minimum value of bypass capacitor required is determined by the maximum amount of voltage drop allowable across the capacitor as a result of the transient current. An approximate value for a bypass capacitor is given as

$$C = \frac{I.\Delta t}{\Delta V} \; Farads$$

where I = Maximum Transient Current
Δt = Transient Duration
ΔV = Allowable Voltage Drop.

For example, a typical 74 HC I_{CC} transient is 20 mA high lasting 20 ns. If the voltage drop is to be kept below 100 mV, then the required bypass capacitor is

(20 mA) (20 ns) / (100 mV)

or 4 nF per output.

However, any series inductance in the bypass loop will cause additional voltage spiking. For any given magnitude of noise spike, an approximate expression for the maximum amount of series inductance is given by

$$L = \frac{V.\Delta t}{\Delta I} \; Henrys$$

where V = Maximum Noise Spike
Δt = Transient Duration
ΔI = Transient Current.

The typical 74 HC I_{CC} transient of 20 mA has a rise/fall time of 4 ns. If we wish to restrict the inductive noise spike to, say, 100 mV peak, the maximum amount of series inductance is

(100 mV) (4 ns) / (20 mA)

or 20 nH.

Referring back to Figure 8, this means that the combined total of ESL, L_L, L_{PC} and L_{IC} must be kept below 20 nH. To a greater or lesser extent the first three terms are within the PC board designer's influence; the fourth term, the inductance of the IC lead frame member or L_{IC}, is invariable, being determined by the IC package. The use of PLCC packaged parts, such as the ADV478/ADV471, inherently reduces L_{IC} to 2–3 nH as against 10–12 nH for the more traditional DIP parts (see section on "Surface Mount Technology").

Appendix 1 examines in greater detail the characteristics and filtering capabilities of various bypass elements including two and three terminal capacitors.

Multilayer PC Boards

In the design of a high performance, high speed graphics system, it is recommended that a four-layer printed circuit board be used.

Figure 9 shows a cross-sectional view of a four-layer printed circuit board, with power and ground planes separating the signal-carrying traces of the component and solder sides of the PCB. As well as using multilayer boards, consideration should be given to the relevant placement of components. Figure 10 shows a suggested component placement scheme.

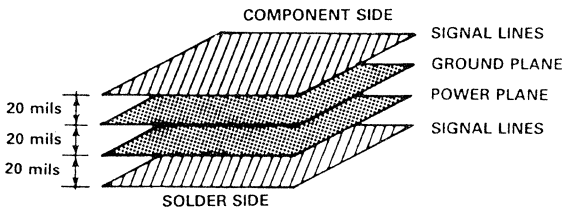


Figure 9. Four-Layer Printed Circuit Board Construction

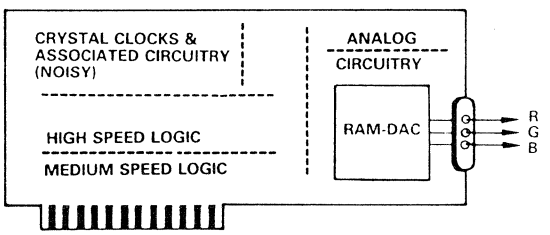


Figure 10. Printed Circuit Board Component Placement

Power and Ground Planes

Power supply decoupling attempts to contain the transient currents within the bypass loop. However it cannot be 100% successful, and some high frequency components will escape onto the power and ground traces. High frequency signal currents will also be flowing in the power and ground traces. In order to avoid common-impedance noise coupling due to these currents, it is necessary to reduce the impedance of the power and ground traces to an absolute minimum. The only satisfactory way to achieve this is not to use traces at all but to use power and ground planes. On a PC-card-sized, two-layer board with one side devoted to a ground plane, the impedance of the plane is in the tens of milliohms range.

A four-layer board allows another plane to be used as a power plane. Low impedance power and ground contacts are thus available over the full area of the board. Additionally, in a four-layer board with power and ground planes inside the board and signal traces on the top and bottom of the "sandwich," overlapping power and ground planes act as an inherent distributed capacitor, as shown in Figure 9. This provides some measure of high frequency decoupling. From the signal interconnect point of view, the major advantage of using a ground plane is the very substantial reduction in signal loop area it provides. In a typical PCB layout, signal current flows out through one trace and back through a ground trace. Such a path can include a large loop area; a large loop area, as has already been discussed, implies high inductance for the traces with follow-on consequences of signal ringing, EMI radiation and crosstalk. To reduce the inductance it is necessary to reduce the loop area through which the signal current flows. The use of power and ground planes minimizes loop areas, thereby reducing inductances and resulting EMI.

The electromagnetic fields associated with an idealized case of two parallel wires carrying equal and opposite currents are shown in Figure 11.

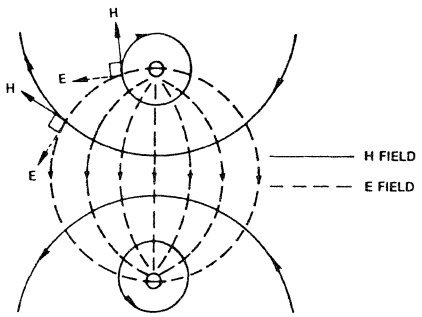


Figure 11. Electromagnetic Field about Two Parallel Conductors Carrying Equal and Opposite Currents

The two fields (electric, E, and magnetic, H) tend to be confined between or near the conductors. The electric field is strongest in the plane of the conductors. The magnetic field is nonzero at points close to the conductors, but farther away (relative to the wire spacing) the fields from both conductors tend to cancel out. Keeping the conductors together promotes field cancellation which can be viewed either as minimizing the loop area or minimizing the inductance; the results are the same.

Introducing a ground plane (sheet of copper) halfway between the wires, as shown in Figure 12, does not disturb the field pattern even when the lower wire is removed.

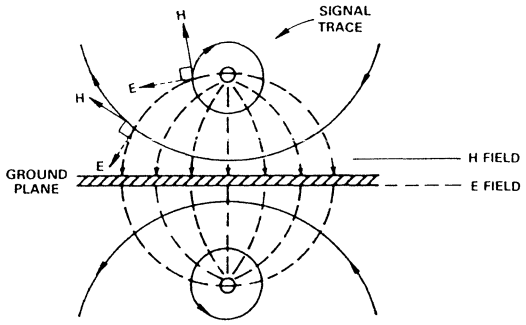


Figure 12. Electromagnetic Field about Two Parallel Conductors Separated by a Ground (Copper) Plane

A virtual image of the lower wire has been produced in the copper plane maintaining the original field configuration. This is the basis of microstrip. With a properly designed ground plane system, the return current will always flow under the signal trace, the path of lowest impedance.

Digital Signal Interconnections

The use of a ground plane allows the signal interconnects to be viewed as microstrip transmission lines whose characteristic impedances, propagation delays, etc., can be readily calculated. Microstrip is the name given to a transmission line which consists of a signal trace separated from a ground plane by a dielectric. Figure 13 shows the cross section of such a line.

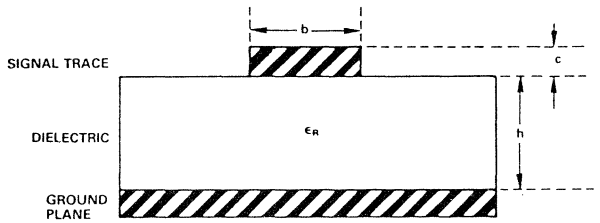


Figure 13. Cross Section of Microstrip Transmission Line

The characteristic impedance, Z_0, of this line is

$$Z_O = \frac{87}{\sqrt{\epsilon_R + 1.41}} Ln \left\{ \frac{5.98\ h}{0.89\ b + c} \right\} \Omega$$

where ϵ_R = Relative Dielectric Constant of Board

typically ϵ_R = 5 for glass/epoxy boards.

b, c, h = dimensions indicated in Figure 13

The propagation delay, t_{PD}, of a microstrip line is given by

$$t_{PD} = 1.017 \sqrt{0.475 \epsilon_R + 0.67}\ ns/ft.$$

Note that this propagation delay is dependent only on the dielectric constant and not on the line geometry.

The graph below shows impedance values for various configurations of microstrip line.

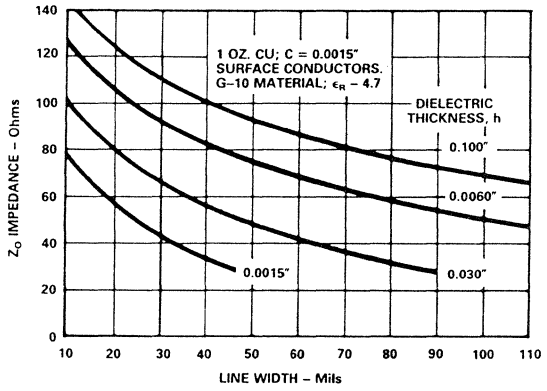


Figure 14. Impedance Versus Line Width & Dielectric Thickness for Microstrip Lines

Gross impedance mismatches between the transmission line's characteristic impedance and the source (driver output) or load (receiver input) impedances connected to the line reflect the signal back and forth on the line. These reflections will cause overshoot, EMI radiation and crosstalk. By properly terminating the line with either source or load impedances which match that of the transmission line, reflections can be eliminated or substantially reduced. However, not every signal interconnect demands line termination; the need is determined by the relationship between the rise (or fall) time of the signal and the time required for the signal to travel the length of the interconnect. As a general guideline for digital signals, line termination is needed if the one way propagation delay, t_P, over the length of the interconnect is greater than one eighth of the signal rise time, t_R, i.e., line termination is needed if

$$t_P \geq (1/8) \bullet t_R\ secs.$$

A number of dc and ac termination techniques exist which trade increased power dissipation against component count. The simplest termination technique which dissipates no extra power is a series termination one where a resistor is placed in series with the signal interconnect at the source end of the line, see Figure 15. The resistor should have a value equal to the characteristic impedance of the line minus the output impedance of the driver and should be of metal-film construction or some other low-inductance material. The load impedance is considered an open circuit. Series termination is most suitable for systems where only one receiver (e.g., ADV478/ADV471) is connected to the line. Note that if pull-up resistors are required on digital or clock signals, they should be connected to the PCB Power Plane (V_{CC}).

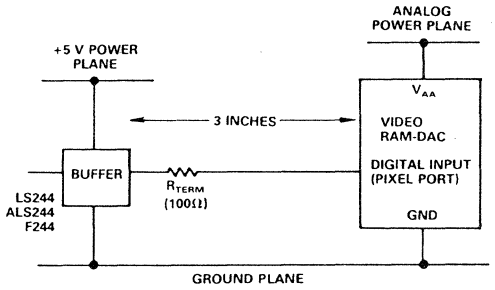


Figure 15. Series Termination of Signal Lines

Crosstalk

Crosstalk is any unwanted signal coupling between parallel PC-board traces due to mutual inductance (L_M) and capacitance (C_M), as illustrated in Figure 16.

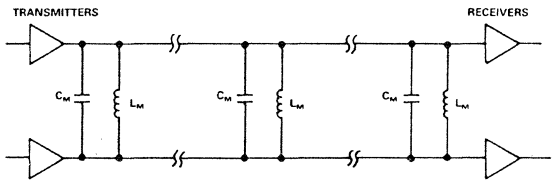


Figure 16. Capacitive and Inductive Coupling between Signal Traces

In general, crosstalk is directly proportional to line impedances, frequency and line lengths and inversely proportional to line spacing. Much of the induced crosstalk in a signal line is from immediately adjacent transmission lines which suggests that wider spacing between lines will reduce the problem. This may not always be possible in closely spaced circuits, so an alternative approach is to shield the signal lines by inserting narrow grounded traces between each signal line on the same wiring plane, as shown in Figure 17.

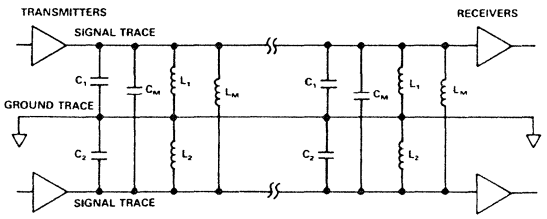


Figure 17. Ground Trace between Signal Lines Reduces Crosstalk

At high frequencies capacitive coupling dominates. The addition of a shield (or ground trace) between the signal lines changes the equivalent circuit. Crosstalk is now reduced since the inductance L_M is now much larger than either L_1 or L_2 and capacitance C_M is much smaller than either C_1 or C_2.

Separate Power Plane for Video RAM-DAC

To further isolate the Video RAM-DAC from the PCB's power supply, V_{CC}, it is recommended that a separate power plane, V_{AA}, be used for the video RAM-DAC and its associated circuitry. This analog power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a suitable filtering device such as a ferrite bead (see Appendix 1 – *Ferrite Bead Inductor*). This ferrite bead should be located no more than three inches away from the Video RAM-DAC. In the case of Analog Devices' ADV478 and ADV471, which have multiple power (V_{AA}) pins, it is important to connect all these V_{AA} pins to the analog power plane. This eliminates any possibility of latchup in the device.

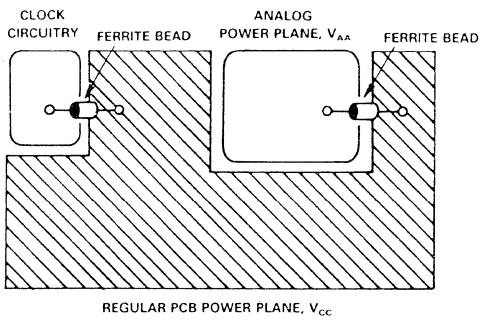


Figure 18. Power Plane Decoupling Using Ferrite Beads

Common Ground Plane

Due to the presence of RAM on board the ADV478/ADV471 and ADV476, it is not recommended to isolate the device's ground circuitry from the main PCB ground. Corruption of data could occur. These Video RAM-DACs should have all GND pins connected to the PCB's regular ground plane.

Analog Outputs

The analog outputs of Analog Devices' video RAM-DACs are driven by switched current sources. These parts are designed to drive either a singly or doubly terminated 75 Ω load. The doubly terminated configuration shown in Figure 19 is the preferred choice.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the Video RAM-DAC be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches). The 75 Ω termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane.

As well as minimizing reflections, short analog output traces will reduce noise pick up due to neighboring digital circuitry.

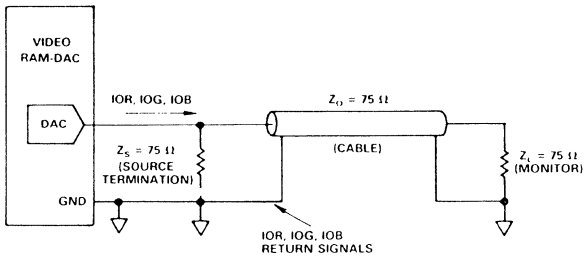


Figure 19. Recommended Analog Output Termination for Video RAM-DACs

Surface Mount Technology (SMT)

Surface mount technology (SMT) offers many EMI advantages over traditional through-hole designs. Because SMT allows the designer to place components on both sides of the printed circuit board as well as featuring smaller component sizes, it provides superior PCB integration. This means that loop lengths can be reduced and noisy signal traces can be shortened, all having a positive effect on EMI. The shorter lead lengths of SMT packages decrease inductance, thereby providing better high frequency performance.

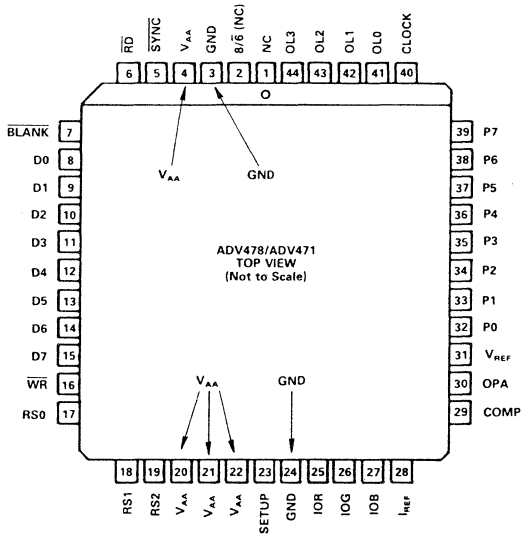
Many, if not all components required for a video graphics system are available as surface mount devices. Memories, controller chips and logic are all available in small SMT packages. Resistors and capacitors can also be purchased in a small "chip" format.

As well as producing Video RAM-DACs in a dual-in-line package (DIP), e.g., the ADV476 (28-pin DIP), Analog Devices packages its ADV478/ADV471 in 44-pin plastic leaded chip carriers (PLCC). This package has substantial advantages over DIP packages in that the lead-frame inductance is small (2-3 nH) and constant for any pin around the package. A DIP package usually has power and ground on diagonally opposing corner pins which presents a much larger lead-frame inductance (10–12 nH). Additionally lead-frame inductance varies with pin position.

In addition to the PLCC package the ADV478/ADV471 video DACs have a number of design features intended to minimize EMI problems.

The pinout of the ADV478/ADV471 in Figure 20 shows four power pins and two ground pins. In operation, the four V_{AA} pins are tied together at the package and supplied with a single +5 V supply. Similarly the two ground pins are tied together at the package and connected to the PCB ground. Internally, however, power rail routing has been separated according to functionality. The various V_{AA} pins are used to drive different internal sections of the ADV478/ADV471. One V_{AA} pin provides a common power rail for "digital" logic;

another provides an "analog" power rail for the DAC and reference circuitry; while yet another provides power to the n-substrate of the device. Since all p-channel transistors have as their back-gate the n-substrate, a separate substrate supply acts to isolate the DAC power rail from noise transients injected into the substrate by switching transistors. The use of multiple power and ground pins results in reduced voltage spiking and improved power supply rejection at the DAC outputs.

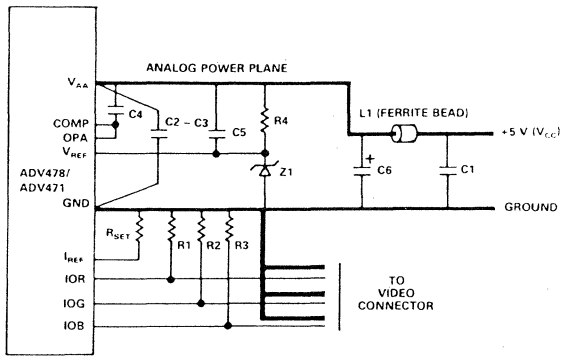


1. PIN NAMES FOR THE ADV471 INDICATED IN PARENTHESES
2. NC = NO CONNECT

Figure 20. ADV478/ADV471 PLCC Pin Assignment Showing Multiple Power and Ground Connection Points

CIRCUIT LAYOUT FOR THE ADV478/ADV471

A recommended layout and component listing for the ADV478/ADV471 is shown in Figure 21. More details regarding the characteristics of various decoupling and filtering components can be found in Appendix 1 of this application note.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1 μF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10 μF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75 Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R4	1 kΩ 5% RESISTOR	
R_{SET}	1% METAL FILM RESISTOR	
Z1	1.235 V VOLTAGE REFERENCE	ANALOG DEVICES AD589KH

Figure 21. Connection Diagram and Component Listing for the ADV478/ADV471

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The final chapter in EMI design is the actual test. With good design practice and even a partial adherence to some of the issues raised in this application note, no difficulty should be encountered in achieving certification. The testing itself however must be carried out with great care in order to do justice to your design. It should be remembered that in the case of a peripheral device such as a VGA board, FCC testing is applied to a complete operating computer system. This complete system must pass with the VGA board present before the VGA board itself is considered to have passed.

A complete operating computer system is configured using the following:

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It is paramount that only the best equipment is used. If for example a noisy monitor is used, the test results might not pass the agency limits, not because your board is at fault, but perhaps because of a poor quality, noisy monitor used in the test. An excellent choice of monitor is IBM's 851X series. Another principal culprit, causing EMI in such a system, is the parallel printer cable. A good quality, shielded cable must be used.

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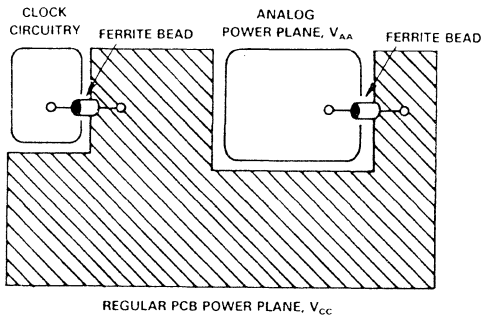

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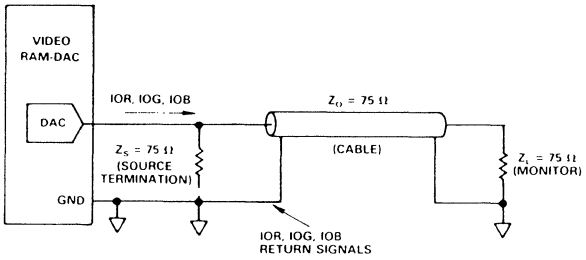

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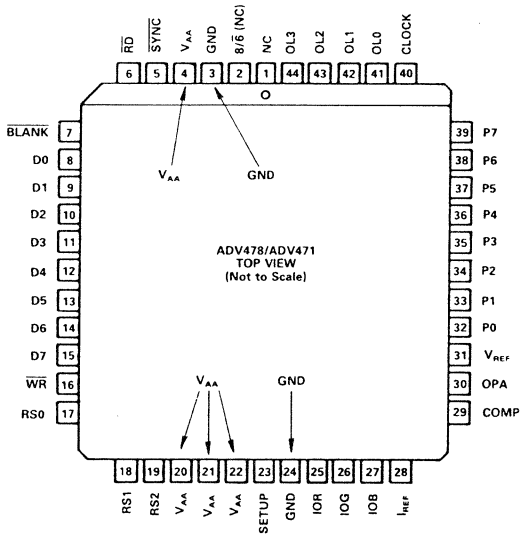

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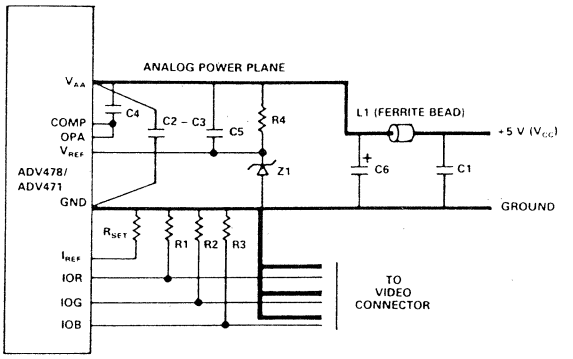

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R4	1 kΩ 5% RESISTOR	
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If you are using an outside test house, it is advisable to be present during testing, or at least have a representative from your company who understands the operation of the system and its various components.

AD/VGA

Analog Devices has designed its own high performance graphics board, AD/VGA for evaluation purposes. The board design is based on the ET3000AX* Video Graphics Controller from Tseng Labs and the high performance ADV478/ADV471 Color Palette RAM-DAC from Analog Devices. The board is fully compatible with all IBM PC† video standards as well as IBM PS/2† Video Graphics Array (VGA). It has additional modes including 800 × 600 resolution with 256 colors as well as 1024 × 768 in 16 colors. These modes require pixel data rates of up to 45 MHz or 66 MHz. The silkscreen showing component placement and type for the AD/VGA board is shown in the appendix.

The board has been certified to comply with the limits for a Class B computing device pursuant to Subpart J of Part 15 of FCC Rules.

FCC ID: HRF55L8826VGA

One actual set of measurements for radiated emissions from the AD/VGA board is shown in Appendix 2. Results can be compared to the FCC limits as listed in Table I.

The AD/VGA board was installed in a DELL SYS 200‡ computer using an IBM 8514 monitor. A modem, printer and mouse were attached. These measurements were made in 132 × 44 text mode.

A complete set of test results is available for inspection.

REFERENCES

1. International EMI Emission Regulations

USA:	FCC–15 Part J
West Germany:	VDE 0871/VDE 0875
Canada:	CSA C108.8–M1983
Japan:	CISPR(VCCI)/PUB 22

2. EMI Countermeasures – Application Guidance – Murata Mfg. Co. Ltd.
3. Henry. W. Ott, "Noise Reduction Techniques in Electronic Systems." John Wiley, N.Y., 1986.
4. Paul A. Brokaw, "An I.C. Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right for a Change." Analog Devices Data-Acquisition Databook 1984, Volume 1, Pages 20–13 to 20–20.
5. Motorola Inc., "MECL Design Handbook" 2nd Edition, 1972.

†IBM PC, IBM PS/2, IBM8514/A and VGA are trademarks of International Business Machines Corp.
‡DELL SYS 200 is a trademark of Dell Computer Corporation.
*ET3000AX is a trademark of Tseng Laboratories, Inc.

APPENDIX 1

EMI FILTERING COMPONENTS

No matter how well a PCB is laid out, there will always be a need for some kind of filtering. This section of the application note examines, in some detail, a number of filtering devices which are suitable for a high speed graphics system. The frequency characteristics of such devices as well as their inherent limitations will be discussed.

The effect of an EMI filter is generally expressed in terms of insertion loss. Noise suppression is described as a logarithm of the ratio of the output voltage without a filter to that with a filter in the circuit and is normally expressed in units of dBs. The simplest example is a first order device, a parallel capacitor or series inductor. A first order filter has an insertion loss slope of 20 dB per decade.

Table 1-1 shows a list of suitable filtering devices and their useful frequency bandwidth.

Filtering Device	Effective Bandwidth
Two-Terminal Capacitor	100 kHz–50 MHz
Ferrite-Bead Inductor	10 MHz–500 MHz
Three-Terminal Capacitor	1 MHz–800 MHz
Four-Terminal LC Filter	100 kHz–1 GHz

Table 1-1. Effective Bandwidth of Various Filtering Devices

The favorite and most widely used filtering device in electronic apparatus today is undoubtedly the "Bypass-Capacitor." It is simple to use, very effective and cheap. Unfortunately though, its effect in a high frequency graphics systems is sometimes the opposite to what is desired. A little thought regarding choice of capacitor, in terms of construction and value can lead to a dramatic improvement in noise performance.

Two-Terminal Capacitor

Let us first take a more detailed look at the structure of a real capacitor.

The impedance of an ideal capacitor connected between line (V_{CC}) and ground is given by

$$Z_C = \frac{1}{2\pi f C.}$$

From Figure 1-1, we can see that the insertion loss of an ideal capacitor increases with frequency at a rate equal to 20 dB/decade. In other words, the capacitor's filtering effect is greatest for higher value frequency components. Increasing the value of capacitance has the effect of filtering out lower frequency components. In the real world, however, a two-terminal capacitor has inductance in series with the capacitance, due to the inherent inductance of the lead wires as shown in Figure 1-2. The reactance characteristic of such a capacitor is shown in Figure 1-3 with the composite insertion loss characteristic shown in Figure 1-4. Clearly, the inductance, ESL, limits the insertion loss. The residual inductance of a capacitor is a function of both the electrode construction as well as lead length. This inductance can vary between 5 nH and 150 nH.

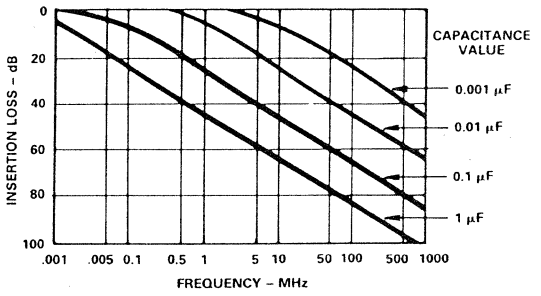


Figure 1-1. Insertion Loss Versus Frequency for Ideal Capacitors

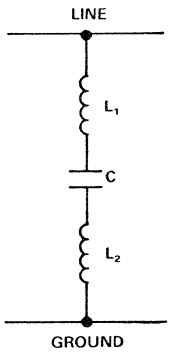


Figure 1-2. Real Capacitor Showing ESL Due to L_1 and L_2

Table 1-2 shows typical values of series inductance for various capacitor types.

Capacitor Type	Capacitance μF	Equivalent Series Inductance (ESL) nH
Lead Type		
Monolithic Ceramic	0.01	5
	0.1	5
	1.0	6
Disc/Lead Type Ceramic	0.0002	4.5
PolyethyleneTelephthalate	0.03	9
Mica	0.01	52
Polystyrene Film	0.001	12
	0.1	100
Tantalum Electrolytic (with Solid Electrolyte)	16	5
Aluminum Electrolytic		
RF Specific	470	13
Standard	470	130

Table 1-2. ESL for Various Capacitor Constructions and Values

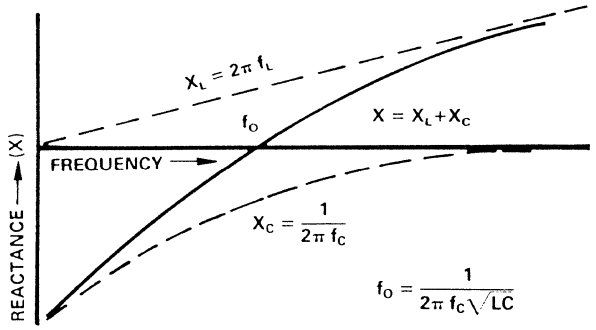


Figure 1-3. Reactance Characteristic of a Capacitor with Finite ESL

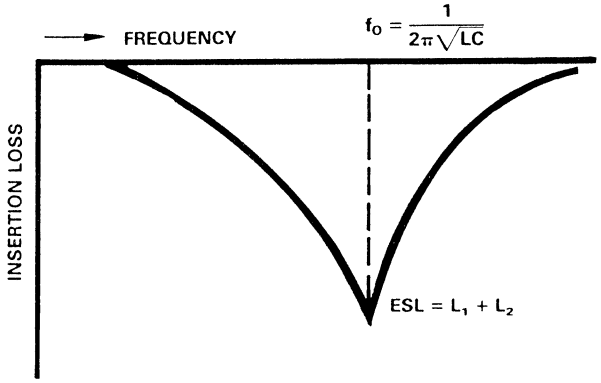


Figure 1-4. Insertion Loss of a Capacitor is Limited by f_O

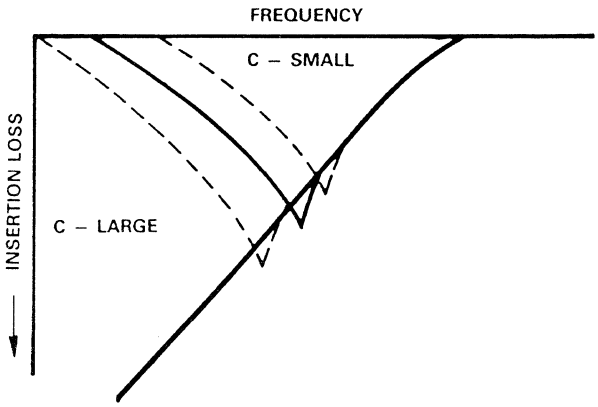


Figure 1-5. A Large Value Capacitor Has a Decreased f_O

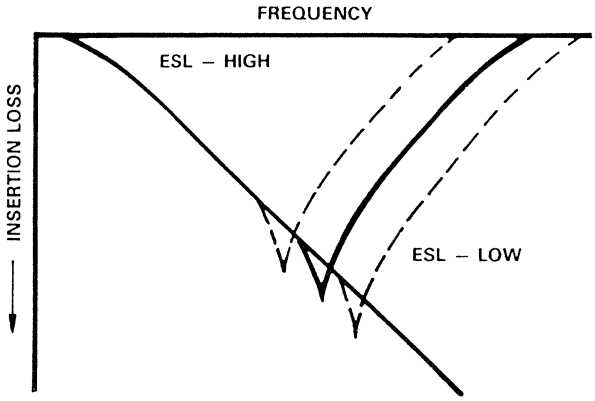


Figure 1-6. A Capacitor with Low ESL Has an Increased f_O

The resulting effect of this equivalent series inductance (ESL) is a reduction in the effectiveness of the capacitor at filtering frequency components beyond a certain point, known as the resonant frequency, f_O. It can be seen from Figures 1-4 to 1-6 that increasing the capacitance value can have the effect of reducing the resonant frequency thereby reducing the ability of this device to filter out higher frequency components. It is therefore imperative that a capacitor with low residual inductance be used. A good choice of high frequency decoupling capacitor would be a 0.1 μF lead type monolithic ceramic capacitor (MCC). This has a series inductance of approximately 5 nH. The resonant frequency, f_O, is thus kept high thereby maximizing high frequency rejection.

As well as series inductance, a capacitor will also contain resistance, referred to as equivalent series resistance (ESR). See Figure 1-7.

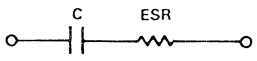


Figure 1-7. Real Capacitor showing ESR

This resistance imposes a finite limit on the ability of a capacitor to bypass high frequencies to ground. Total impedance of the device can never be lower than that imposed by the equivalent series resistance. A capacitor having a high ESR will exhibit a flattened insertion loss curve, compared with the sharp resonant point typically observed in capacitors with lower ESR values.

The overall equivalent circuit of a two-terminal capacitor with ESL and ESR is shown in Figure 1-8.

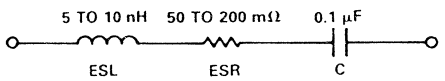


Figure 1-8. Equivalent Circuit of a Real Capacitor

Maximum noise reduction will be achieved through the selection of capacitors with lowest ESL and ESR values.

At least one decoupling capacitor should be used for each IC in the system. In the case of the Video RAM-DAC, it is recommended that for high frequency suppression, a 0.1 μF ceramic capacitor be used to decouple

each group of V_{AA} pins to ground. Low frequency components can be decoupled through the use of a 10 μF tantalum capacitor. Figure 21 shows the recommended decoupling scheme for the ADV478/ADV471. Capacitors with minimal lead length, should be placed as close as is physically possible to the device.

Three-Terminal Capacitor

Three-terminal capacitors have filtering characteristics extending to several hundred MHz. Two leads at the line side of the capacitor provide line input and output respectively, see Figure 1-9. This reduces effective series inductance.

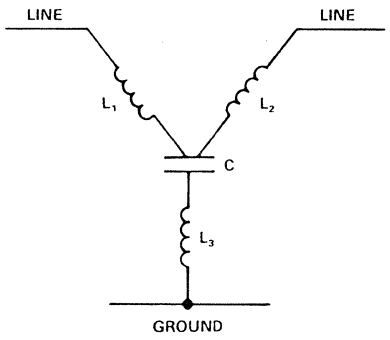


Figure 1-9. Equivalent Circuit of a Three-Terminal Capacitor

One particular example of the use of such a three-terminal device would be at the analog outputs of the Video RAM-DAC. The NFV510 series of three-terminal capacitors from Murata have a sharp insertion loss characteristic. This means that high frequency signals can be filtered without affecting the integrity of the signal itself. The NFV510 series has an excellent shape factor, due to an inherent roll-off of 100 dB/decade, see Figure 1-10. It therefore suppresses noise without reducing resolution. In the case of a graphics system with video output rates of 80 MHz, the NFV510-655 T2A 107 could be employed at the outputs of each of the red, green and blue DACs.

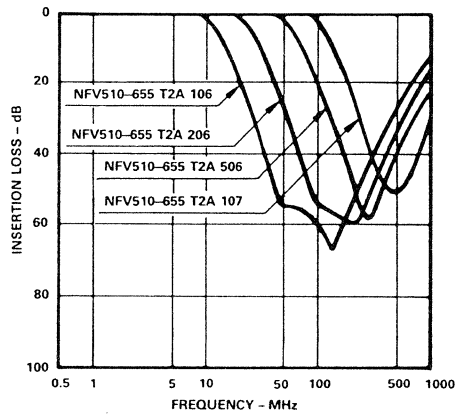


Figure 1-10. Frequency Response of the NVF510 Series of Three-Terminal Capacitors

Ferrite Bead Inductor

A ferrite is another very useful component in the effective suppression of EMI. One can consider a ferrite bead as a high frequency resistor with no resistance at dc. Ferrites have filtering characteristics which extend well into the megahertz range. They can be used to provide isolated power planes, e.g., a PCB's power plane may be subdivided into an analog power plane (V_{AA}) and clock circuitry power plane, see Figure 18. Ferrite beads work both ways; one prevents noise components on the PCB power plane from being coupled onto the analog power plane, while the other filters out noise components from the clock circuitry. The analog power plane provides power to the Video RAM-DAC and all its associated analog circuit, while the clock circuitry power plane provides power to the crystal oscillators and clock divide circuitry.

It is not, however, recommended to use a ferrite bead in separating ground planes; a separate analog ground plane to the Video RAM-DAC may have disastrous effects on the contents of the on-board color look-up table. One common ground plane should encompass the entire PCB.

The system's shield ground or earth may be connected through a ferrite bead to the regular PCB ground.

Ferrite is the generic term given to a class of non-conductive ceramics. They are constructed using combinations including oxides of iron, cobalt, nickel, zinc, magnesium and some rare earth materials. It is important to be careful in choosing ferrite beads. Ferrite composition and therefore filtering characteristics can vary quite significantly from manufacturer to manufacturer. Analog Devices recommends the use of the BL01/02/03 series of ferrite bead inductors from Murata as well as the Fair-Rite 2743001111. The frequency characteristic of a radial single bead ferrite bead is shown in Figure 1-11.

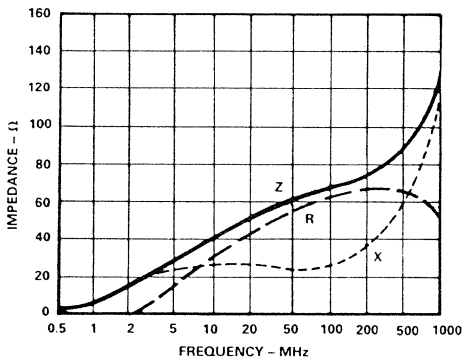


Figure 1-11. Frequency Characteristic of the BL01RN Ferrite Bead Inductor

DC Power Filter

In some cases it might be necessary to filter the power source's high frequency components. This is often the case when switched mode power supplies are used. If it is found that the system's power supply is excessively noisy, one could consider the use of a dc power filter

such as a BNX002-01 from Murata or equivalent. This filter which consists of a large value monolithic 4-terminal capacitor, a feed-through capacitor and beads, as shown in Figure 1-12, produces an effective filtering effect, 40 dB min over the frequency range 1 MHz to 1 GHz. Figure 1-13 shows the filtering characteristic of the BNX series of power filters from Murata.

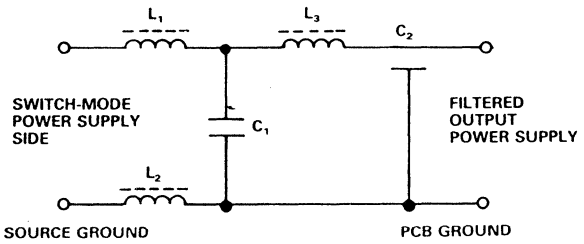


Figure 1-12. Equivalent Circuit of a dc Power Filter

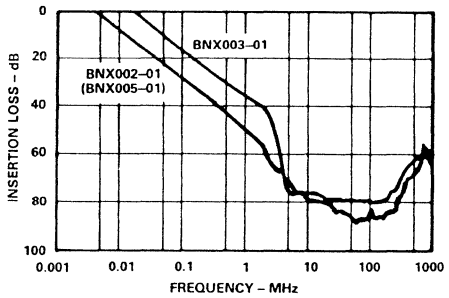


Figure 1-13. Frequency Response of the BNX Series of dc Power Filters

APPENDIX 2

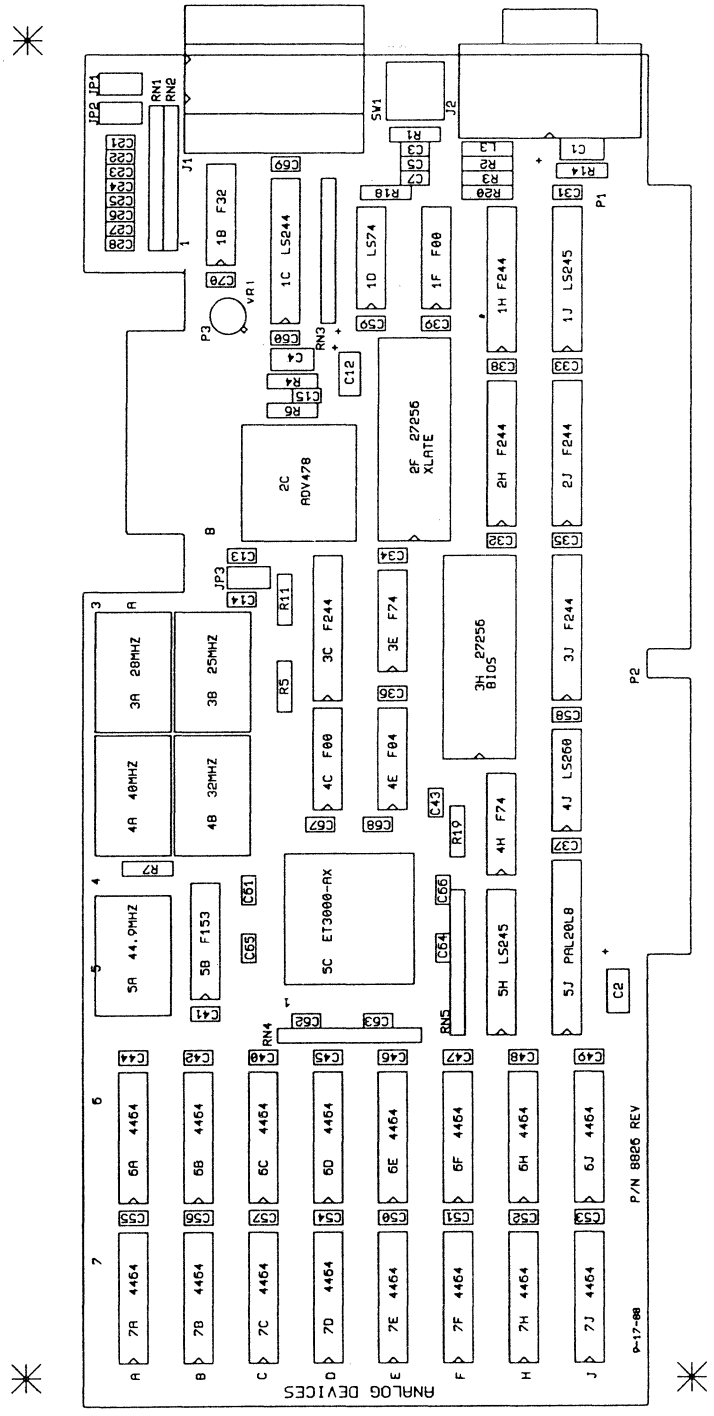
FCC TEST RESULTS OF AD/VGA

Frequency	EUT Orientation	Ambient Radiation	Antenna		EUT Radiation			Field Strength
			Polarization	Height	Factor	Maximum	Corrected	
MHz	Degrees	dB μV	H/V	Meters	dB/M	dB μV	dB μV/M	μV/m
37.2	60	6.7	V	1	12.9	18.8	31.7	38.5
48.1	20	3.6	V	1	12.9	19.0	31.9	39.5
60.6	90	7.8	V	1	11.4	20.3	31.7	38.5
62.8	90	9.8	V	1	10.6	17.3	27.9	24.8
69.5	50	8.6	V	1	8.9	19.9	28.8	27.5
70.9	30	10.8	V	1.5	8.9	24.0	32.9	44.2
72.7	90	10.9	V	1	8.6	20.1	28.7	27.2
75.8	30	14.2	V	1	8.4	22.4	30.8	34.7
78.9	30	13.1	V	1	8.4	24.5	32.9	44.2
80.7	0	10.9	V	1	8.5	19.1	27.6	24.0
88.0	0	12.0	V	1.5	10.0	22.1	32.1	40.3
119.7	330	4.4	H	1.5	15.8	16.9	32.7	43.2

Sample of FCC Test Results for AD/VGA Board

APPENDIX 3

AD/VGA COMPONENT PLACEMENT (SILKSCREEN)



ANALOG DEVICES

APPLICATION NOTE

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Animation Using the Pixel Read Mask Register of the ADV47X Series of Video RAM-DACs

by Bill Slattery & Eamonn Gormley

INTRODUCTION

The Pixel Read Mask Register, which is an integral part of IBM's VGA* graphics system, can be used as a hardware-level Pixel Processing Unit. This allows real time motion or animation to be implemented with minimal software overhead. This application note examines the operation and structure of such a pixel processing unit with the pixel read mask register as the central controller. A practical application which uses the pixel read mask register to animate a picture scene is described. A complete listing of the Turbo-C source code is given in the appendix.

No additional hardware is required for existing VGA graphics systems to implement this application.

VIDEO RAM-DAC

Analog Devices produces a range of video RAM-DACs, which are specifically designed for IBM's Personal System/2* VGA. The range includes the ADV478, ADV471 and ADV476, all of which are monolithic +5 V CMOS video RAM-DACs. These parts are specified over a number of speed grades; 35 MHz, 50 MHz, 66 MHz and 80 MHz. The RAM-DACs are packaged as 44-pin PLCC and 28-pin plastic DIP devices.

The ADV471 and ADV476 each contain a triple 6-bit digital-to-analog converter and a 256 location by 18 bits deep color look-up table. The devices also include an asynchronous pixel input port and bidirectional microprocessor (MPU) port. These devices and the associated control circuitry allow for flexible interface to many graphics systems configurations. The ADV478 differs from the ADV471 only in terms of its color resolution. The ADV478 has a triple 6-bit/8-bit D/A converter with a 256 × 24/18 color look-up table. The color resolution of the ADV478 is user selectable between 6 bits and 8 bits. The higher 8-bit performance can be used with IBM's 8514/A* graphics standard (upgrade on standard VGA). More detailed information on these and other video RAM-DACs can be obtained in the relevant product data sheets.

Built into all three devices is an 8-bit register known as the Pixel Read Mask Register. Figures 1 and 2 are block diagrams of the ADV478/ADV471 and ADV476 which show the Pixel Read Mask Register.

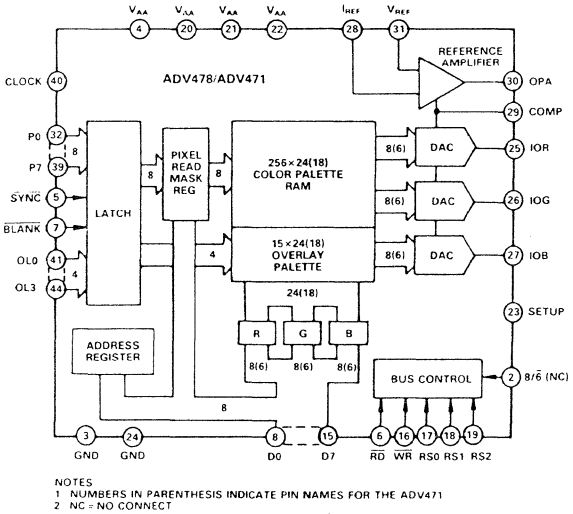


Figure 1. ADV478/ADV471 Functional Block Diagram

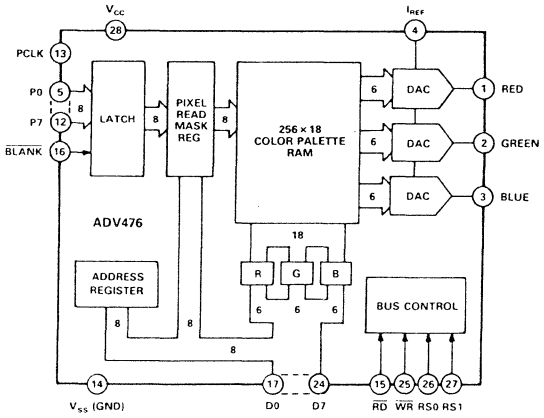


Figure 2. ADV476 Functional Block Diagram

*IBM, VGA, Personal System/2 and 8514/A are trademarks of International Business Machines Corp.

Some of the uses to which the Pixel Read Mask Register can be put include on-screen special effects such as real time animation, flashing objects and overlays.

PIXEL READ MASK REGISTER

The Pixel Read Mask Register is placed in the path of the pixel input stream of data as shown in Figure 3.

The input pixel data stream (P0–P7) is gated with the contents of the Pixel Read Mask Register. The operation is a bitwise logical ANDing of the pixel data. The contents of the Pixel Read Mask Register can be accessed and altered at any time by the MPU (D0–D7). Table I shows the relevant control signals. Under normal operating conditions, this register is loaded with all 1s, i.e., transparent mode.

In a VGA graphics system, the Pixel Read Mask Register is memory mapped and is accessible (read/write) by addressing memory location 36CH.

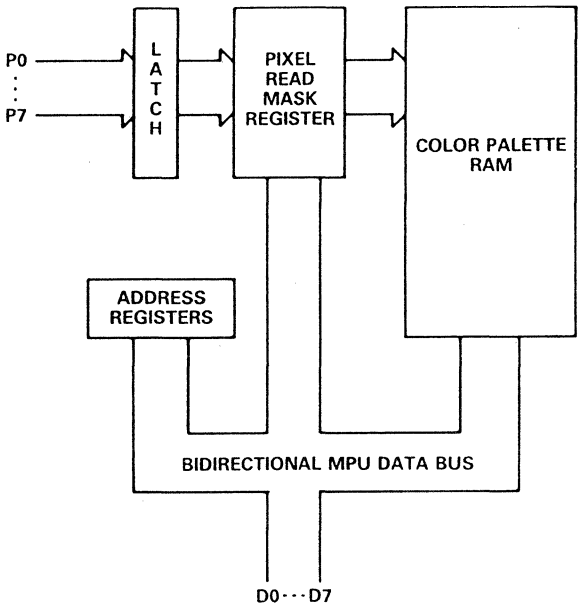


Figure 3. Video RAM-DAC Pixel & Data Ports Showing the Pixel Read Mask Register

RS2*	RS1	RS0	Addressed by MPU
0	0	0	Address Register (RAM Write Mode)
0	1	1	Address Register (RAM Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register

*RS2 is only present on ADV478/ADV471

Table I. Control Input Truth Table for Video RAM-DAC

Figure 4 shows the internal architecture of the pixel input port. The input word Pi, which corresponds to an on-screen pixel location, is ANDed with the contents of the Pixel Read Mask Register, Pm.

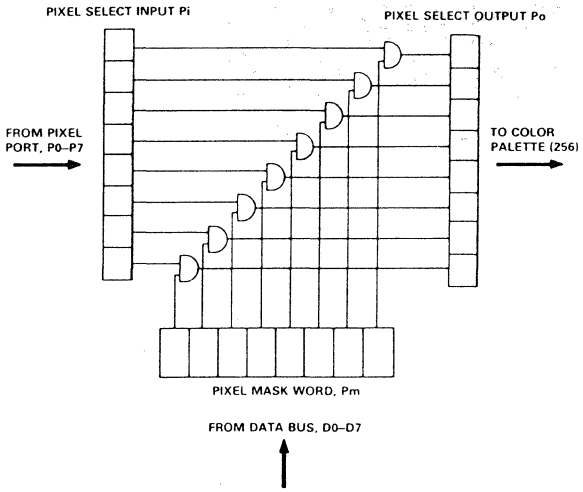


Figure 4. Internal Architecture of Pixel Input Port

The resulting output word, Po, determines which location in the color palette will be assigned to a particular on-screen pixel. Figure 5 shows the logical diagram for this masking operation.

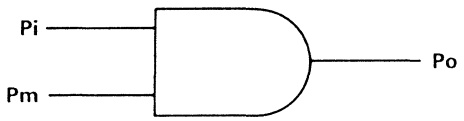


Figure 5. Equivalent Logical Representation of Masking Operation

$$Po = Pi \cdot Pm \quad (1)$$

If Pm = 1, transparent mode, then

$$Po = Pi \quad (2)$$

The pixel stream of data, Po, which arrives at the color palette is a function of both the pixel input stream, Pi, from the Frame Buffer and the contents of the Pixel Read Mask Register, Pm. In the case of an animation application, which will be discussed later in this application note, the rate at which the pixel mask word is changed will determine the motion speed of the scene.

This pixel masking operation can be used to alter the displayed colors without changing the contents of either the video Frame Buffer or the Color Palette RAM. One interpretation of this operation is to consider the pixel input structure of the video RAM-DAC as an on board Pixel Processing Unit.

PIXEL PROCESSING UNIT

The Pixel Input Port (Pi), Pixel Read Mask Register (Pm) and Data Input Port (MPU) within the video RAM-DAC, are the hardware components of this Pixel Processing Unit (PPU). An associated software routine to control the operation is the final element in the complete PPU system. This interpretation enables the color palette to be configured as a multidimensional, paged memory address space, see Figure 6.

In the case of the ADV471 and ADV476 the color palette can be perceived as being broken into an even number of 18-bit color planes instead of just one 18-bit deep color plane. (In the case of the ADV478, each plane is 24 bits deep.)

The palette can therefore be partitioned to produce up to a total of 256 discrete contiguous color memory planes, some of which are shown in Figure 6. A tradeoff, however, must be considered when dividing the color palette into multiple color planes. The number of simultaneously displayable screen colors is inversely proportional to the number of color planes within the color palette. Table II illustrates this relationship. This contiguous configuration is not, however, the sole way of segmenting the memory within the palette. Other non-contiguous configurations including interleaving can be implemented. The choice of memory configuration will be determined by the particular application so as to make most efficient use of the available video memory (Image Frame Buffer and Color Palette RAM).

Number of Color Planes	Number of Simultaneously Displayable Colors
1	256
2	128
4	64
.	.
.	.
256	1

Table II. Simultaneously Displayable Screen Colors versus Number of Color Planes

To operate the PPU, two principal steps must be taken:

1. Load the image data in the correct paged configuration to both the frame buffer and color look-up table, e.g., four frame composite images to the frame buffer corresponding to four discrete planes of color to the palette RAM.
2. Generate the corresponding pixel mask words. These words are individually written to the Pixel Read Mask Register, Pm (at VGA memory location 36CH) and select which of the color planes is to be assigned to the incoming pixel data stream. In the case where four planes are implemented (see Figure 6), four pixel mask words are required.

The overall VGA System Block Diagram showing the PPU and an associated 8-page memory configuration of the color palette is shown in Figure 7.

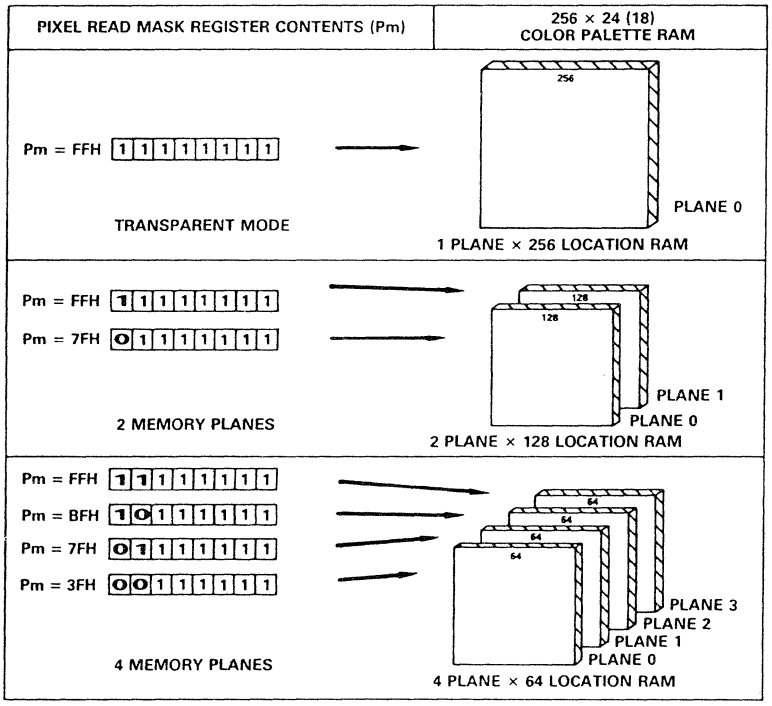


Figure 6. Some Color Palette RAM Configurations Showing Paged Memory Planes and Associated Pixel Read Mask Word (Pm)

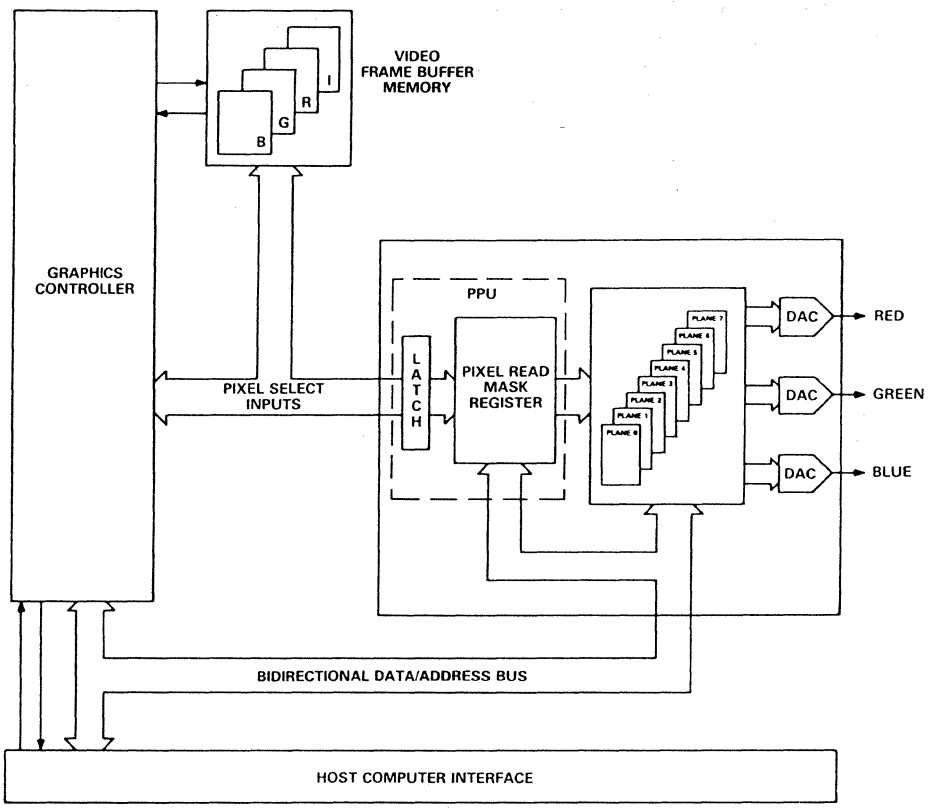
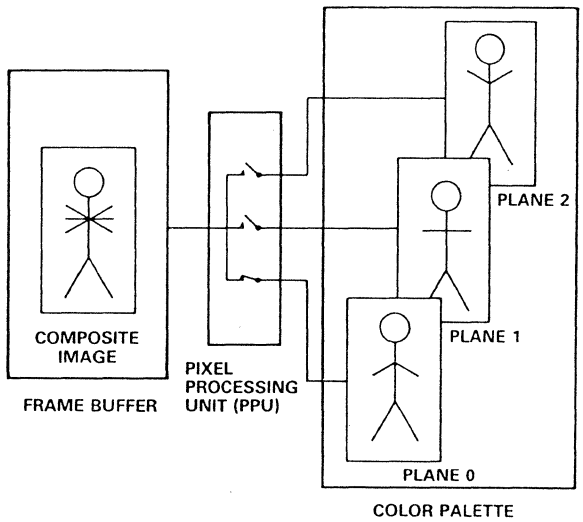


Figure 7. VGA System Block Diagram Showing Color Palette Broken into a Number of Color Planes

ANIMATION

Real time animation using the Pixel Processing Unit is based on the principle that rapidly changing the colors of a stationary object gives the illusion of motion. In other words, a number of similar images or frames, differing only by the relative position of the various colors, displayed in quick succession, can result in motion.

A simple example to explain the idea of animation is illustrated opposite. The animated image consists of three frames; each of the three frames is initially drawn as one composite picture (Frame Buffer image). The color palette contains three discrete, memory blocks or planes of color information, corresponding to three stages of animation. The animation effect in this example is "arm waving" of the cartoon character. By assigning the color planes one by one to the image in the Frame Buffer, the effect of animation can be perceived on the screen. The color plane assigned to the composite image is determined by the PPU which is controlled by the word in the Pixel Read Mask Register. Frame 1 is assigned Color Plane 0, this colors the down arm position in black, while the up and horizontal arm positions take on the background color. Frame number 2 is assigned Color Plane 1, this colors the horizontal arm position in black while the other two arm positions are assigned the back ground color.



Finally, Frame 3 takes on Color Plane 2. This process is then repeated giving the illusion of motion. The rate at which each frame is selected determines the rapidity of the arm waving.

ANIMATION USING THE PPU

This section describes a particular animation example. The scene used in this example consists of traveling space ships and rotating planets. The program which draws the scene and implements the animation is described in the flow diagram of Figure 8. The associated source code, written in Borland's Turbo-C, is given in the Appendix. This application implements 8-stage animation.

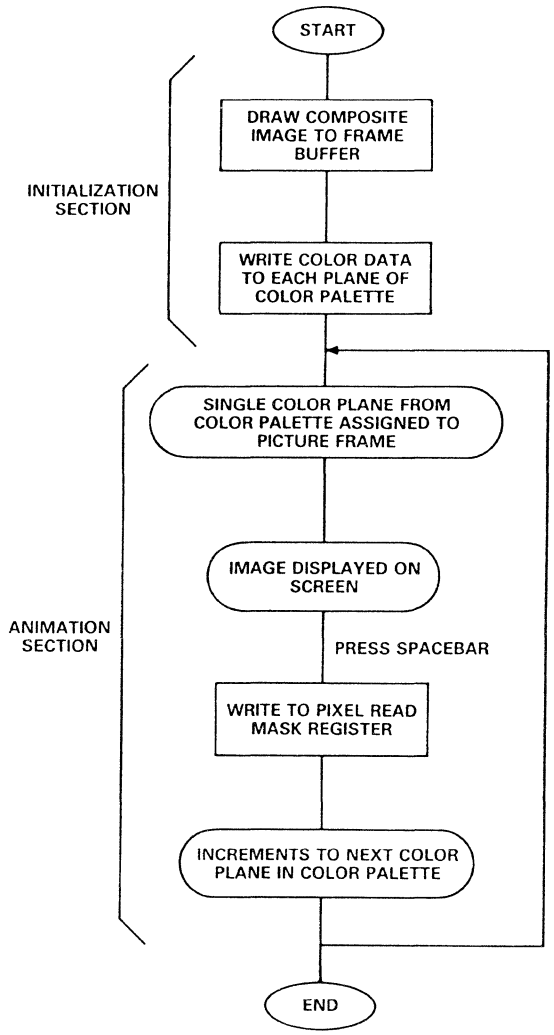


Figure 8. Flow Diagram Representation of Animation Using the PPU

The complete image is drawn to the Frame Buffer. This composite picture contains eight frames of information. The corresponding color planes for each of the eight frames in this composite image, are drawn to the color palette. The color information is arranged in a paged memory format corresponding to that shown in Figure 7. Each of these eight color planes has similar color data; they differ from each other only in terms of the relevant position of the particular colors. For example, Plane 0 could have blue in its first location and color yellow in its second location, while Plane 1 could have the opposite, yellow in Location 1 and blue in Location 2. During the display period, the color palette will only allocate colors to one of the eight frames (i.e., one color plane) at a particular instant. Each plane of color information is mapped to a particular frame within the Frame Buffer. The user-defined value of the Pixel Read Mask Register determines which of the color planes within the palette will be chosen for display at any particular instant. The hex codes, written to the Pixel Read Mask Register Pm, which correspond to each of the color planes (Plane 0 to Plane 7) are listed in Table III.

3C6F	: Address of Pixel Read Mask Register (Pm)	
8FH → Pm	: Plane 0 Selected	Pm = 1000 1111
9FH → Pm	: Plane 1 Selected	Pm = 1001 1111
AFH → Pm	: Plane 2 Selected	Pm = 1010 1111
BFH → Pm	: Plane 3 Selected	Pm = 1011 1111
CFH → Pm	: Plane 4 Selected	Pm = 1100 1111
DFH → Pm	: Plane 5 Selected	Pm = 1101 1111
EFH → Pm	: Plane 6 Selected	Pm = 1110 1111
FFH → Pm	: Plane 7 Selected	Pm = 1111 1111

Table III. Value Written to Pixel Read Mask Register and Associated Color Plane

Pressing the "Spacebar" increments the pixel read mask register corresponding to a jump of 16 locations in the color palette. As there are 16 colors in each color plane, a jump of 16 locations will select the corresponding color in the next highest plane. Continuously pressing the "Spacebar" cycles the incoming pixel stream of data through each of the eight color planes within the palette. This results in the apparent motion or animation of the image.

APPENDIX

C Program for ANIMATION EXAMPLE

Pixel Processing Using Video RAM-DACs
"Rotating Planets & Spaceships"

```
#include <stdlib.h>  /* Turbo C include files */
#include <math.h>    /* these are available under most versions */
#include <dos.h>     /* of C for the IBM & compatibles */
#include <graphics.h>
void palette(int col,int red,int green,int blue);
void plot13(int x,int y,int col);                    /* function definitions */
void model3();
void circle13(int x,int y,int r,double tilt);
void planets();
void stars();
void line13(int x1,int y1,int x2,int y2,int col);
void triangle();

main()
{
 int gd=0,gm=0,opt;
 union REGS reg;
 detectgraph(&gd,&gm);                  /* check for a VGA card */
 if (gd != 9){
  printf("This program cannot find a VGA card installed in this computer.\n");
  printf("A VGA card is necessary to run the tests.");
  exit(1); }

 planets();                             /* do demo */
 reg.h.ah = 0x00;
 reg.h.al = 0x03;
 int86(0x10,&reg,&reg);                 /* return to text mode when finished */
}

void mode13()                           /* set up mode hex 13 = decimal 19 */
{                                       /* this is a 256 color mode with */
 union REGS reg;                        /* 320 x 200 pixel resolution */
 reg.x.ax = 0x0013;
 int86(0x10,&reg,&reg);                 /* set mode 0x13 */
}

void palette(int col,int red,int green,int blue)
             /* assigns a physical color to a logical color */
{
  union REGS reg;
     reg.x.ax = 0x1010;
     reg.x.bx = col;
     reg.h.dh = red;
     reg.h.ch = green;
     reg.h.cl = blue;
     int86(0x10,&reg,&reg);         /* call bios routine to change palette */
}

void plot13(int x,int y,int col)    /* special plot routine for mode 0x13 */
{
     union REGS reg;
     if(x>=0 && y>=0 && x <320 && y<200){
        reg.x.dx = y;               /* set up registers */
        reg.x.cx = x;
        reg.h.ah = 0x0c;
        reg.h.al = col;
        int86(0x10,&reg,&reg);      /* call bios plot routine */
     }}

void circle13(int x,int y,int r,double tilt)
{                                    /* routine draws a single planet */
```

```
int la,yy;
double ang,oldx,oldy,newx,newy,sintl,costl,rcos,rsin;
for(la = -r; la < r; la++)
{                                       /* routine uses a fairly simple */
 yy = sqrt(r*r - la*la) + 1;            /* algorithm to draw a solid circle */
 line13(la+x,y-yy,la+x,y+yy,14); }

costl = cos(tilt);                      /* set up some variables */
sintl = sin(tilt);
yy = 240;                               /* To draw lines of longitude: */
for(la = r; la >= -r; la-=r/15)         /* draw portions of ellipses */
  {                                     /* and rotate them by tilt radians */
   oldx = x-r*sintl;
   oldy = y+r*costl;
   for(ang = -1.57;ang <1.57;ang+=.195) {
    newx = x+la*cos(ang)*costl+r*sin(ang)*sintl;
    newy = y-r*sin(ang)*costl+la*cos(ang)*sintl;
    line13(newx,newy,oldx,oldy,yy); /* line segment of ellipse */
    oldx = newx;                        /* store endpoints */
    oldy = newy;  }
   yy = (yy==247) ? 240 : ++yy;         /* incrememt color used */
  }
for(ang=-1.57;ang<1.57;ang+=.39)        /* draw lines of latitude */
   {                                    /* ie sloped lines */
    rcos = r*cos(ang);
    rsin = r*sin(ang);
    line13(x+rcos*costl-rsin*sintl,y+rsin*costl+rcos*sintl
          ,x-rcos*costl-rsin*sintl,y+rsin*costl-rcos*sintl,15);
   }}

void planets()              /* routine to draw and animate the planets */
{
 int la,lb;

 model3();
 palette(7,255,255,255);
 printf("       Pixel Read Mask Demo\n");
 printf("     ========================\n");
 printf("  This program contains an animated     picture scene which ");
 printf("is initially drawn  on the screen and then ANIMATED ");
 printf("using   the Pixel Read Mask Register.\n");
 printf("\n  Press the spacebar to draw scene and  hold it down ");
 printf("when scene is ready for    animation. When finished, ");
 printf("press any     other key.....");
 while(getch() != ' ');                 /* wait for keypress */

 model3();
 for (la=8;la<16;la++)                  /* set up the palette for animation */
   {
    for (lb=0;lb<8;lb++)
    palette(la*16+lb,0,10,63);          /* set planet lines to blue */
    for (lb=8;lb<16;lb++)
    palette(la*16+lb,0,0,0);            /* stars are initially black */
   }
 for (la=128;la<256;la+=17)
    palette(la,63,63,63),               /* define one line on planet to white */
    palette(la+8,63,63,0);              /* and one star to yellow, per frame */

 palette(15,255,255,255);               /* set color 15 to pure white */
 palette(7,20,255,0);                   /* color 7 to green */
 palette(14,0,10,63);                   /* color 14 used for planet background */

 stars();                               /* draw stars in background */
 circle13(30,30,30,0.9);                /* draw the actual planets */
 circle13(280,35,35,4.0);
 circle13(130,100,70,-0.8);
```

```
  circle13(40,240,125,0.5);
  triangle();                          /* draw the spaceship thingy */
  gotoxy(30,21);printf("Space to");
  gotoxy(30,22);printf("animate.");    /* on screen instructions */
  gotoxy(30,24);printf("Other key");
  gotoxy(30,25);printf("to stop.");
   la=143;                             /* 143 = %10001111 */
   do
    outportb(0x3c6,la),                /* this part does the actual animation */
    la = (la<255) ? la+16 : 143;       /* loop through the palette */
   while((lb = getch()) == ' ');       /* while the spacebar is being pressed */
}

void stars()                           /* routine to plot in the stars */
{
 int la,lb,lc,ld,le,col = 248;
 long q;
 srand(time(&q) % 37);                 /* set up random background */
 for (la=0;la<200;la+=5)  {
    lc = (rand()&0x7)-0x4;
    ld = la;
    le = (rand()&7)+3;
    for (lb=1;lb<320;lb+=le,ld=la+lc*lb/64)
       plot13(lb,ld,col),     /* plot the star */
       col = (col == 255) ? 248 : ++col;
  }}

void line13(int x1,int y1,int x2,int y2,int col)
{                                      /* this routine draws a line in */
 int la,lb,lc;                         /* graphics mode 13H */
 if (abs(x1-x2) > abs(y1-y2))  {       /* line longer in x or y direction ? */
   lc = (x2-x1);lb = (x2 - x1 >=0) ? 1 : -1;
   for (la=x1;la!=x2;la+=lb)           /* loop works out the points on */
   plot13(la,y1+(la-x1)*(y2-y1)/lc,col);   /* the line and plots them */
  }
  else  {
   lc = (y2-y1);lb = (y2 - y1 >=0) ? 1 : -1;
   for (la=y1;la!=y2;la+=lb)
   plot13(x1+(la-y1)*(x2-x1)/lc,la,col);
  }}

void triangle()          /* This routine draws a simple spacecraft-type */
{                        /* object for animation. */
 int la,lb=19,col=248;   /* starting size = 19, color = 248 */
 double tilt=0.5236;     /* starting tilt */

 for (la=200;lb>0;la-=lb,lb--,tilt += .3)
 {                       /* loop to draw 19 objects */
  line13(200+la/2+lb*cos(tilt),la+lb*sin(tilt),
         200+la/2+lb*cos(tilt+2.0944),la+lb*sin(tilt+2.0944),col);
  line13(200+la/2+lb*cos(tilt+2.0944),la+lb*sin(tilt+2.0944),
         200+la/2+lb*cos(tilt+4.1888),la+lb*sin(tilt+4.1888),col);
  line13(200+la/2+lb*cos(tilt+4.1888),la+lb*sin(tilt+4.1888),200+la/2,la,col);
  line13(200+la/2,la,200+la/2+lb*cos(tilt),la+lb*sin(tilt),col);
  col = (col==255) ? 248 : ++col;     /* col = col + 1 until col = 255, when */
 }}                                   /* col returns to zero */
```

SECTION XI

HIGH SPEED TECHNIQUES

HIGH SPEED TECHNIQUES

INTRODUCTION

IMPEDANCE
- Resistance, Inductance, Capacitance

GROUNDS AND GROUNDING
- Kirchoff's Law, Ground Systems

NOISE
- Conducted, Capacitive Coupling, Inductive Coupling, Electromagnetic Coupling, Overall Layout, Multiple Card Systems, Logic Types

CONSTRUCTION
- IC Sockets

PROTOTYPING HIGH SPEED CIRCUITS

HIGH SPEED PROBING TECHNIQUES

INTRODUCTION

Low speed digital circuits can be fabricated using the "node" approach. That is to say, the components are wired together according to the circuit diagram, and any two points in the circuit which are connected by conductors, either wire or PC track, are assumed to be at the same potential. This approach does not work with high speed or high precision circuits and most especially does not work with high speed high precision circuits. This is because the conductors making connections between the components are not pure short circuits, as the "node" approach assumes, but have resistance, inductance and capacitance and therefore modify the original circuit.

One of the most important mistakes arising from the "node" approach is the assumption that all points in a circuit which are connected to "ground" on the circuit diagram will be at the same potential. As we shall see, this is a major source of errors.

Low speed digital circuits are also highly resistant to noise problems - whether from internally or externally generated noise. High speed and high precision analog circuits are not resistant to noise, and again we must consider all possible noise effects when designing the physical layout of such systems.

It is quite difficult to formulate rules for the efficient layout of high speed and high precision circuits, which is why effective CAD software for such a task is largely unavailable. This section of our seminar is devoted to discussion of the problems involved in such layouts. While it contains considerable detail of potential problems, it contains few specific rules for precision high speed layout, since almost all such "rules" tend to be more misleading than useful.

The rules that it does offer, as absolutes, are some Laws of Physics: Ohm's Law, Kirchoff's Law, Faraday's Laws and Lenz's Law, together with a basic law of life: Murphy's Law (sometimes known as Klipstein's Law in German-speaking countries) - this states that if anything can go wrong, it will!

BASIC LAWS INVOLVED IN PCB LAYOUT.

(MURPHY'S LAW IS THE MOST IMPORTANT.)

- OHM'S LAW
- KIRCHOFF'S LAW
- FARADAY'S LAWS
- LENZ'S LAW
- MURPHY'S LAW

Figure 11.1

Consideration of these laws reminds us that, since room temperature superconductors are not yet available (at the time of writing this section of the seminar, at any rate), any conductor, whether wire or PC track, will have resistance. It will also have self-inductance, and self-capacitance, and mutual inductance and capacitance to any adjacent conductors. All these properties will affect circuit performance and must be considered when designing the physical layout of high-performance analog systems. Murphy's law tells us that when designing such systems it is extremely ill-advised to disregard any physical effect known to be present without doing a calculation (or an experiment) to prove that such neglect is justified.[1]

IMPEDANCE - Resistance

At 25°C the resistivity of pure copper is 1.724E-6 ohm cm. The thickness of standard weight (1 ounce) PCB foil is 0.038 mm (0.0015"). The sheet resistance of standard PCB copper is therefore 0.45 milliohms/square, which implies a resistance for the 0.25 mm track frequently used in computer designed digital circuitry of 18 milliohms/cm, which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4% /degree C around room temperature, which can be a further inconvenience.

As an illustration of the effect of PCB track resistance, consider a 16-bit ADC with a 5K input resistance which has 5 cm of 0.25 mm PCB track between it and its signal source. This track has a resistance of approximately 0.09 ohms and introduces a gain error of well over 1 LSB into the ADC.

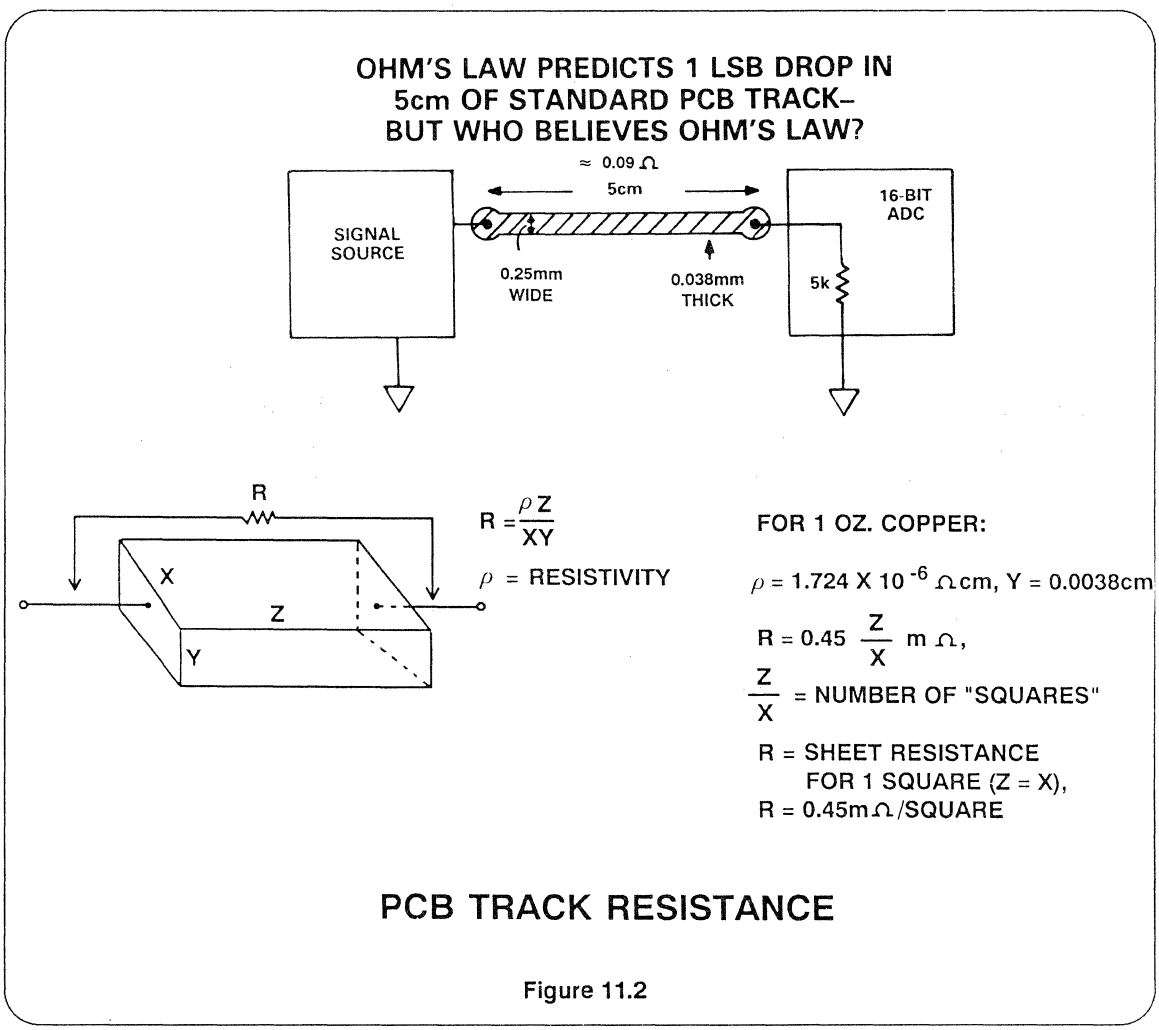


Figure 11.2

This, of course, is a DC effect. At high frequencies we must also consider the "skin effect" where inductive effects cause currents to flow only in the surface of conductors. This has the effect of increasing the resistance of a conductor at high frequencies (note that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased - that will be dealt with later). Skin effect is quite a complex phenomenon and detailed calculations are beyond the scope of this seminar. However a good approximation for copper is that the skin depth is

$6.61/\sqrt{f}$ cm, where f is the frequency in Hz.

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the PC foil this tells us that for normal 0.038 mm PC foil we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important, the resistance in ohms per square for the surface area of copper is

$2.6 \times 10^{-7} \sqrt{f}$ ohms per square.

When calculating skin effects in PCBs it is important to remember that current flows in both sides of the PC foil (this is not necessarily the case in microstrip lines), so the resistance per square of PC foil is half the above value.

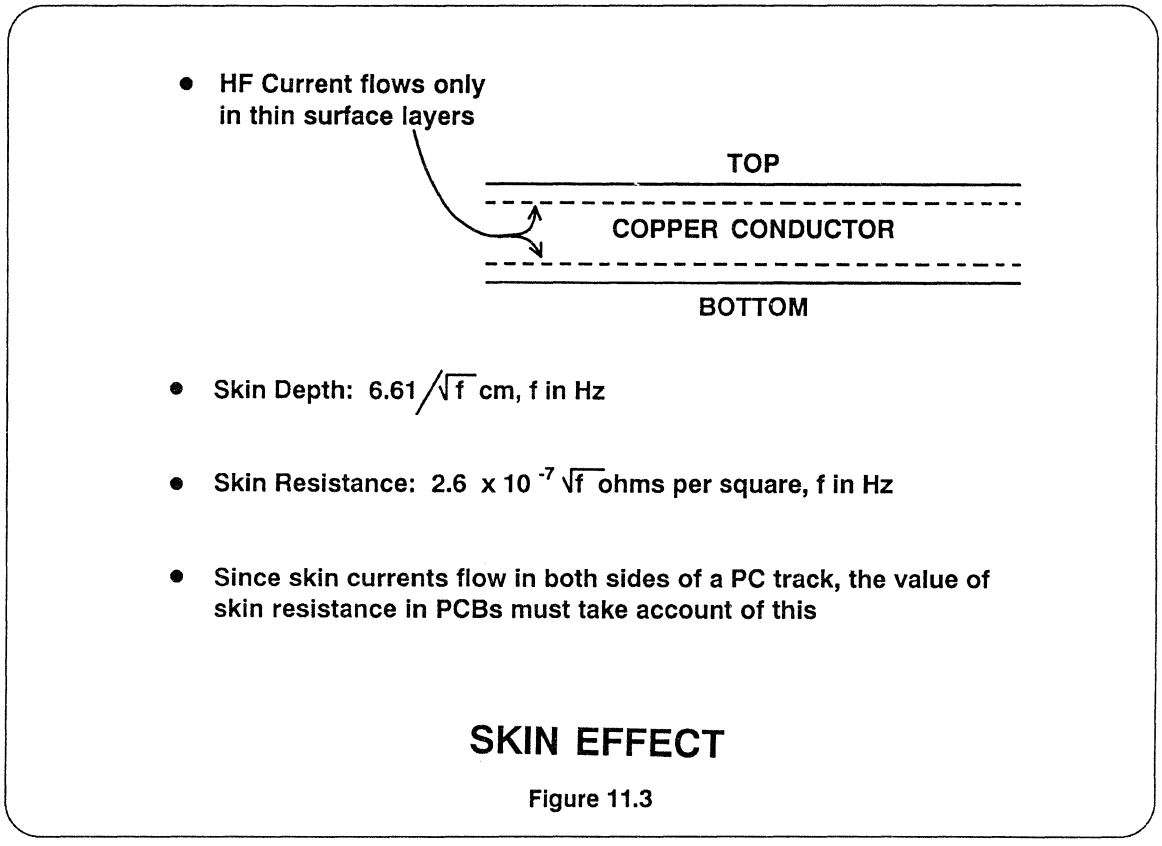


Figure 11.3

IMPEDANCE - Inductance

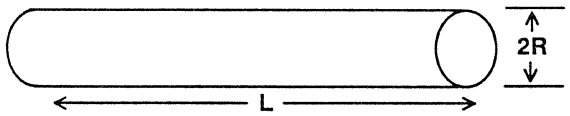
The inductance of conductors is also important. The inductance of a wire of length L mm and circular cross-section with radius R mm in free space is

$$0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\mu H.$$

The inductance of a strip conductor (an approximation to a PC track) of width W mm and thickness H mm in free space is

$$0.0002L\left[\ln\left(\frac{2\text{-}L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\ \mu H\ .$$

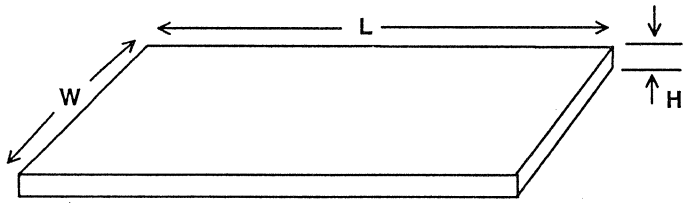
In real systems these formulae both turn out to be very approximate but they do give some idea of the order of magnitude of inductance involved. They tell us that 1 cm of 0.5 mm outside diameter wire has an inductance of 7.26 nH and 1 cm of 0.25 mm PC track has an inductance of 9.59 nH - these figures are reasonably close to measured results.



L, R in mm

WIRE INDUCTANCE = $0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right]\mu H$

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH
(2R = 0.5mm, L = 1cm)



STRIP INDUCTANCE = $0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right]\mu H$

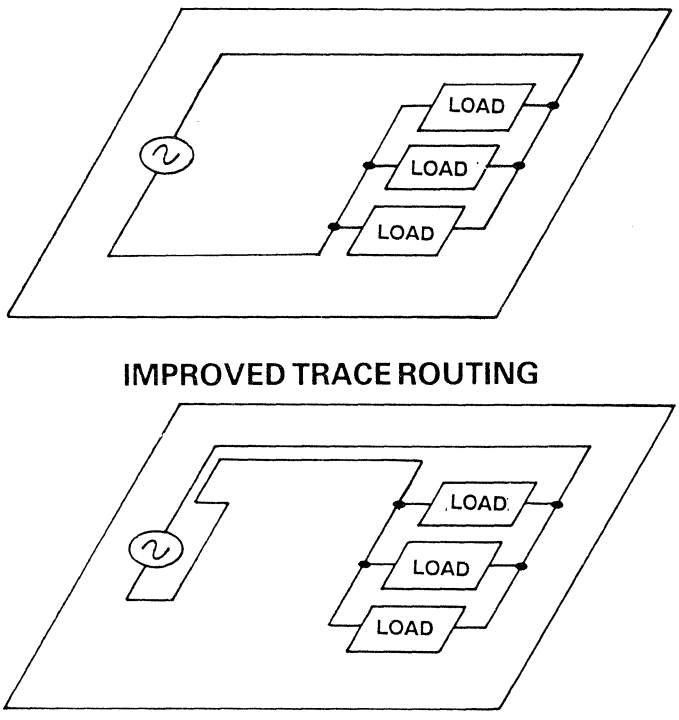
EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH
(H = 0.038mm, W = 0.25mm, L = 1cm)

INDUCTANCE

Figure 11.4

Another consideration with respect to inductance is the separation of outward and return currents. As we shall discuss in more detail later, Kirchoff's Law tells us that current flows in circles - there is always an outward and return path. The whole path forms a single-turn inductor.

If the area enclosed by the turn is large, the inductance, and hence the AC impedance, will also be large, whereas if the outward and return paths are close together the inductance will be much smaller. The principle is illustrated in Figure 11.5.



NONIDEAL AND IMPROVED SIGNAL ROUTING

Figure 11.5

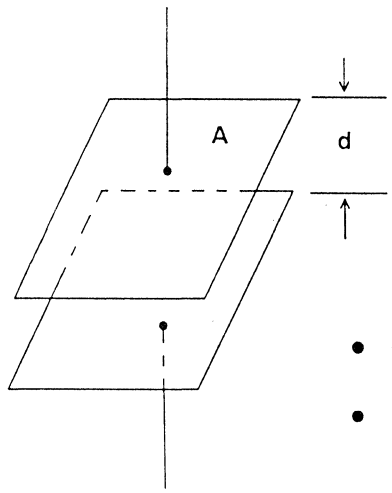
The nonideal routing in Figure 11.5 has another drawback - the large area enclosed by the conductor produces extensive external magnetic fields, which may interact with other circuits and cause unwanted coupling. Similarly the large area is more vulnerable to interaction with external magnetic fields, which can induce unwanted signals in the loop. The small area routing is far less liable to these mutual inductance effects.

IMPEDANCE - Capacitance

Like inductance calculations, capacitance calculations on PCBs are somewhat approximate, being affected by edge effects. The commonest calculation, that of a PC track above a ground plane, uses the simple parallel plate capacitor formula

$$C = 0.00885\ E_r\ A/d\ pF$$

where A is the area of plates in square mm, d is their separation (the board thickness) in mm, and E_r is the dielectric constant (relative to air). Given that one of the commonest types of PCB uses glass-fibre/epoxy material with E_r of approximately 4.7 and that the most often used thickness is 1.5 mm (approximately equal to 1/16 inch), the capacity of PC track over a ground plane may be roughly estimated at 0.28 pF/sq.cm. Such capacitors do not have particularly good Q (unless expensive low-loss board materials such as teflon are used) and so are not generally used in place of discrete capacitors in critical applications. However, their effect on circuit performance must always be considered.



$$C = \frac{0.00885\ E_r\ A}{d}\ pF$$

A = plate area in mm

d = plate separation in mm^2

E_r = dielectric constant relative to air

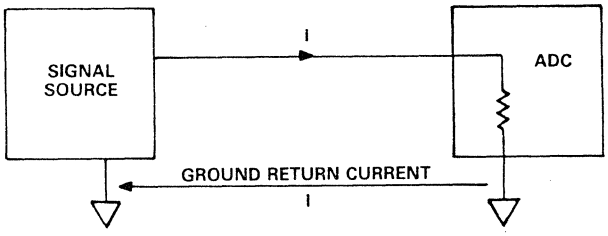
- Commonest type of PCB uses 1.5mm glass-fiber epoxy material with $E_r = 4.7$
- Capacity of PC track over ground plane is roughly $0.28pF/cm^2$

CAPACITANCE

Figure 11.6

GROUNDS & GROUNDING - Kirchoff's Law

Kirchoff's Law tells us that at any point in a circuit, the algebraic sum of the currents is zero. This means that all currents flow in circles and, particularly, the return current must always be considered when analyzing a high-speed or high precision circuit.[2]

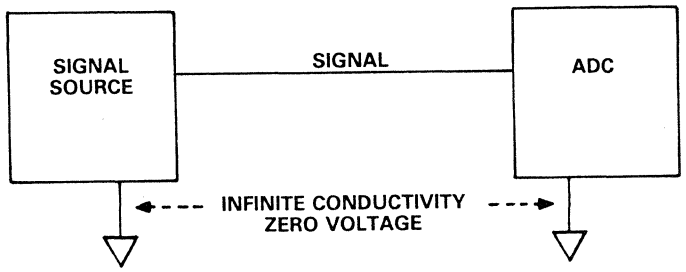


AT ANY POINT IN A CIRCUIT
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO
OR
WHAT GOES OUT MUST COME BACK
WHICH LEADS TO THE CONCLUSION THAT
ALL VOLTAGES ARE DIFFERENTIAL
(EVEN IF THEY'RE GROUNDED)

KIRCHOFF'S LAW

Figure 11.7

Most people consider the return current when considering a fully differential circuit, but when considering the more usual circuit where a signal is referred to "ground" it is far too common for engineers to assume that all the points on the circuit diagram where the ground symbol is to be found are at the same potential.

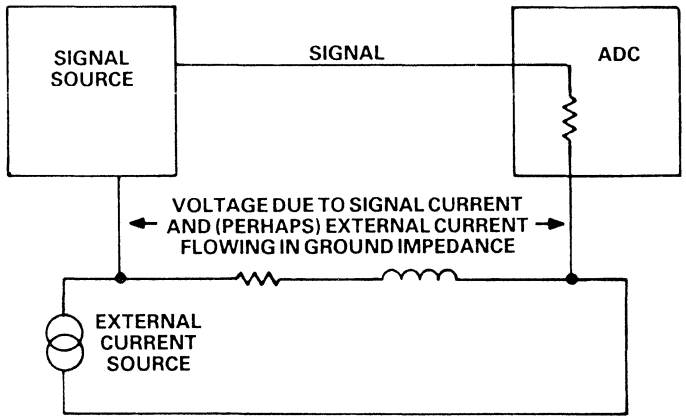


THE IDEAL GROUND

Figure 11.8

A more realistic model of ground is shown in Figure 11.9. Not only does the return current flow in the complex impedance which exists between the two "ground" points shown in Figure 11.8, giving rise to a voltage drop in the total signal path, but also external currents may flow in the same path, generating uncorrelated noise voltages which are seen by the ADC.

Once we have defined the problem, the nature of the solution becomes obvious: minimize ground impedances so that the ground of a system really is unipotential and also attempt to minimize externally-generated noise currents in sensitive ground impedances. Unfortunately, this is more easily said than done, and many diferent ground arrangements have been adopted at various times to try to solve the basic problem.



A MORE REALISTIC GROUND

Figure 11.9

GROUNDS & GROUNDING - Ground Systems

The most common techniques are the star ground, separate analog and digital grounds, the ground plane, and the elimination of the need for an accurate ground by the use of differential signal transmission. All have their advantages and disadvantages but, as it is rare for one approach to solve all problems, hybrid solutions are frequently chosen.

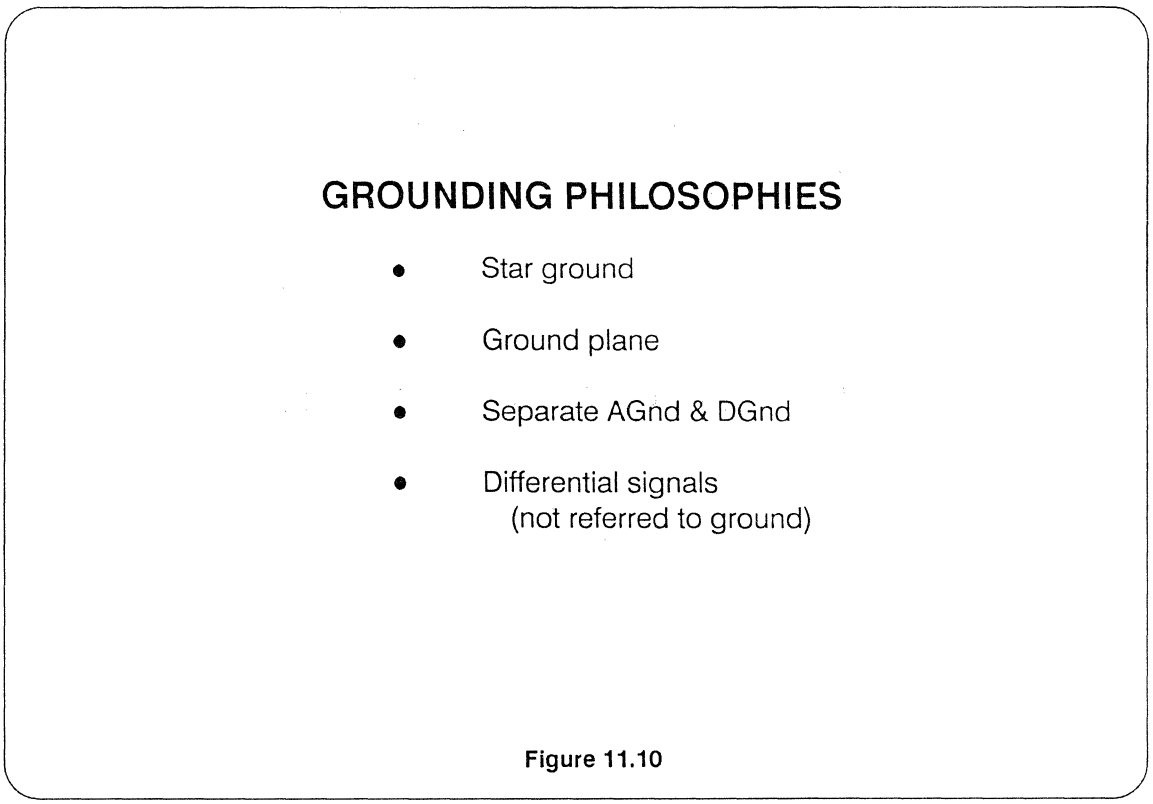


Figure 11.10

The "star" or "Mecca" ground philosophy is based on the theory that there is a single point in a circuit to which all voltages are referred. This is known as the "star" or "Mecca" point.

This philosophy is reasonable but encounters practical difficulties. For example, if we design a system with a star ground, we first draw all the signal paths to minimize signal interaction and the effects of high impedance signal or ground paths. We frequently find, however, when the power supplies are added to the circuit diagram, that the power supplies either add unwanted ground paths, or that supply currents, flowing in existing ground paths, are sufficiently large, or noisy, or both, as to corrupt the signal transmission. This problem is often avoided by having separate analog and digital power supplies and separate

analog and digital grounds, joined at the star point.

There is often a practical problem with analog-digital converters (ADCs). For reasons concerned with practical interfacing techniques and available integrated circuit architectures, it is common for monolithic and hybrid ADCs to have separate analog ground (AGnd) and digital ground (DGnd) pins. Nevertheless, they must not see a potential difference of more than a few mV, and must therefore be connected close to the ADC package. How do we accomplish this? We can, of course, make this point the star point of the whole system but it is rarely convenient to do so - and impossible if there are several such ADCs in a system.

ANALOG GROUND & DIGITAL GROUND

- Monolithic & hybrid ADCs frequently have separate AGnd & DGnd pins which must be joined together at the device.
- This is not done from a desire to be difficult, but because the voltage drop in the bondwires is too large to allow the connection to be made internally.
- The best solution to the grounding problem arising from this requirement is to connect both pins to system "analog ground".
- It is likely that neither the digital noise so introduced in the system AGnd, nor the loss of digital noise immunity, will seriously affect the system performance.

Figure 11.11

In most cases the correct way to connect such an ADC is to join AGnd and DGnd at the device as instructed, and then join the node to the system AGnd. If the system AGnd has suitably low impedance, the digital currents flowing in it should not seriously affect the ground noise. The degradation of digital noise immunity caused by noise voltages between system AGnd and DGnd is most unlikely to have any effect at all (most logic families have at least hundreds of millivolts of noise immunity - a few have volts).

Related to the star ground system is the use of a ground plane. One side of a double-sided PCB, or one layer of a multi-layer board, is made of continuous metal, which is used as ground. The theory behind this is that the large amount of metal will have low resistance and as low inductance as is possible.

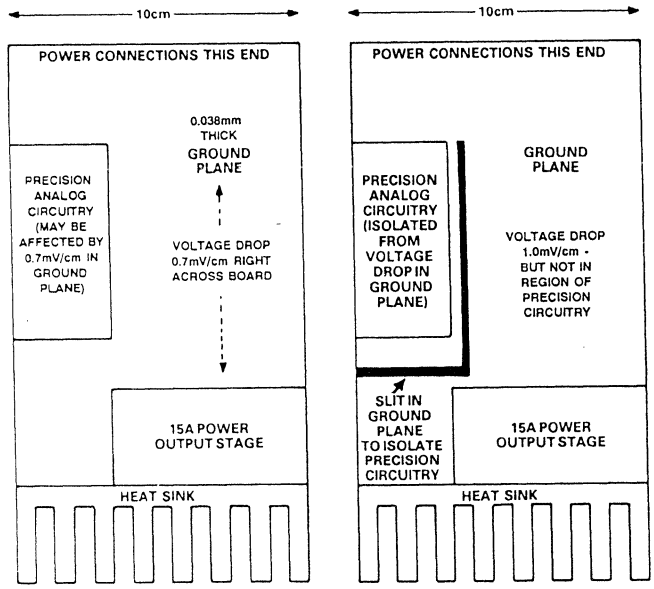
GROUND PLANES

- One entire side or layer of a PCB is continuous grounded conductor.
- This gives minimum ground resistance and inductance but is not always sufficient to solve all grounding problems.
- Breaks in ground planes can improve or degrade circuit performance - there is no general rule.
- Twenty years ago ground planes were difficult to fabricate. Today they are not.
- If your PCB facility objects to fabricating ground planes - GET A NEW PCB FACILITY!

Figure 11.12

It is sometimes argued that ground planes should not be used because they are liable to introduce problems in manufacture and assembly. Such an argument may have had limited validity twenty years ago when PCB physics were less understood, wave-soldering less reliable, and solder resist techniques less well understood, but today it should not be tolerated.

Ground planes solve many ground impedance problems, but not all. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances they can be enough to prevent proper circuit function. Figure 11.13 shows such a problem - and a possible solution.



A SLIT IN A GROUND PLANE CAN
RECONFIGURE CURRENT FLOW FOR BETTER ACCURACY

Figure 11.13

Consider a ground-plane PCB 100 mm wide with a ground connection at one end and a power amplifier at the other drawing 15A. If the ground plane is 0.038 mm thick and 15A flows in it, there will be a voltage drop of 68 μV/mm. This voltage drop would cause quite serious problems to any ground-referenced precision circuitry sharing the PCB. However, if we slit the ground plane so that high current does not flow in the region of the precision circuitry, we can probably solve the problem - even though the voltage gradient will increase in those parts of the ground plane where the current does flow.

A break in a ground plane is not always a good thing. We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. When an HF signal flows in a PC track running over a ground plane, the arrangement functions as a microstrip transmission line, and the majority of the return current flows in the ground plane underneath the line. Suppose that there is a break in the ground plane (in Figure 11.14 the break is to allow another conductor to cross the first): the return current must flow around the break and both the inductance, and the vulnerability of the circuit to external fields are increased.

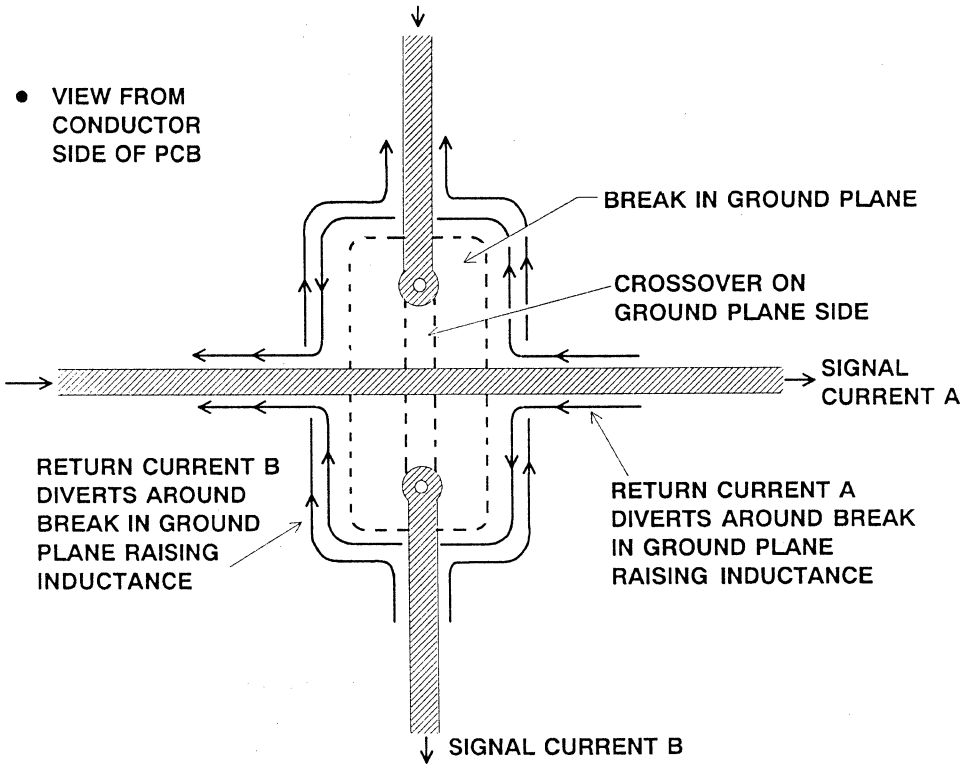

• VIEW FROM CONDUCTOR SIDE OF PCB
BREAK IN GROUND PLANE
CROSSOVER ON GROUND PLANE SIDE
SIGNAL CURRENT A
RETURN CURRENT B DIVERTS AROUND BREAK IN GROUND PLANE RAISING INDUCTANCE
RETURN CURRENT A DIVERTS AROUND BREAK IN GROUND PLANE RAISING INDUCTANCE
SIGNAL CURRENT B
• RETURN CURRENTS A AND B MAY INTERACT
BREAKS IN GROUND PLANE RAISE INDUCTANCE

Figure 11.14

It would be far better if the second signal were carried across both the first signal and the ground plane by means of a piece of wire. The ground plane then acts as a Faraday shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multilayer board both the cross-over and the continuous ground plane can be accomodated without the need for a wire link. Multilayer PCBs are expensive and harder to troubleshoot than simple double-sided boards but do offer even better shielding and signal routing. The principles involved remain unchanged, but the range of layout options is increased.

Use of double-sided or multilayer board with at least one continuous ground plane is undoubtedly one of the most successful approaches to the design of high performance, high frequency analog and converter PC cards.

NOISE

We have discussed elsewhere the problems of noise intrinsic to electronic circuitry: Johnson noise, Schottky noise, 1/f noise, etc. In this section we shall consider noise which is the result of external signals finding their way into a system and degrading its performance.

NOISE SOURCES

- Conducted noise
- Capacitively coupled noise
- Inductively coupled noise
- Electromagnetically coupled noise

Figure 11.15

NOISE - Conducted

Rather obviously, conducted noise is noise which enters the circuit on conductors. We have already seen how currents flowing in a ground impedance produce voltages which may corrupt circuit performance. The other common source of conducted noise is power supplies.

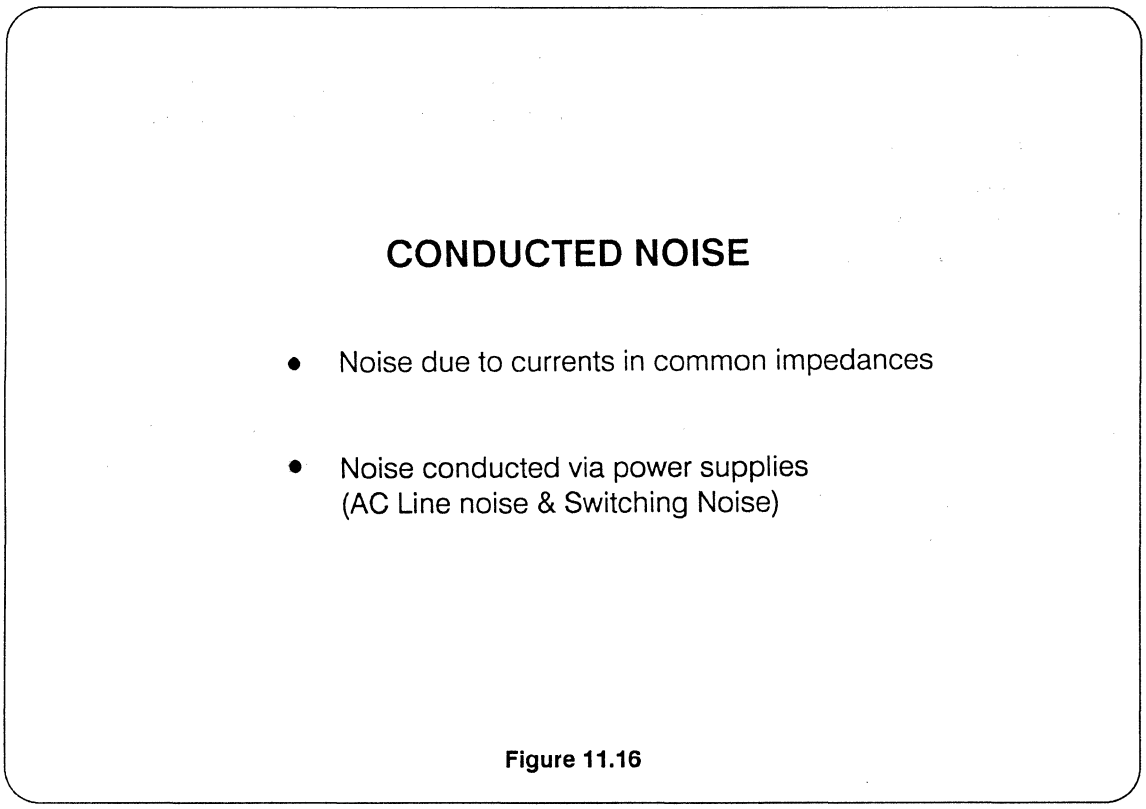


Figure 11.16

When we design an electronic circuit we generally assume that our power supplies are noise-free voltages, of exactly the nominal voltage, with zero source impedance at all frequencies. This is not the case.

We also assume that the published power supply rejection figures (PSRR) for the devices which we use are valid at all frequencies from DC to light. This is not the case either.

POWER SUPPLY NOISE

- Long-term voltage variation
  (Long-term variations in voltage or AC line voltage)
- AC Line noise
  (Both 100/120 Hz ripple on rectifier output and transient noise on the AC line which passes to the DC output)
- Switching noise
  (Digital noise from switching- mode power supplies)
- Power line noise transfer
  (Unwanted signals which pass from one part of a circuit to another via the common power supply)

Figure 11.17

All power supplies have noisy outputs. This noise may consist of long-term voltage drift, line ripple at 100 or 120 Hz, or high frequency spikes from switching regulators. All power supplies also have finite output impedance, so that if a circuit draws a varying current, the supply voltage will vary with the current. If two circuits are supplied from a common supply, this provides a mechanism whereby one circuit may affect the other. Once we appreciate all these effects, we can attempt to quantify them, and take steps to minimize their adverse effects on our systems.

Long-term supply voltage changes, whether due to battery voltage drop during life, or line voltage variations, are rarely a problem. Where such variations might cause difficulties, the system will incorporate a supply voltage regulator to keep variations within acceptable limits. Similarly, ripple at twice the AC line frequency, and any spikes or HF noise which may enter the system via the AC supply, should not cause degradation of performance in a well-designed system. If the decoupling capacitors in the rectifier do not adequately minimize the effect, the series regulator almost certainly will. It is, however, always worthwhile to have a surge eliminator on the AC line input to any system. While such a circuit is unlikely to be needed in preventing normal line noise from currupting system performance, it is essential to prevent occasional large surges (from lightning or

similar causes) from causing actual damage to the power supply or the system that it is powering.

The commonest type of power supply noise is switching noise. Switching power supplies are small, cheap, efficient and, in too many cases, extremely noisy! Not only do they generate conducted noise, they are also efficient producers of capacitively coupled noise, magnetically coupled noise, and electromagnetically coupled noise. The *best* possible advice is to not use them.

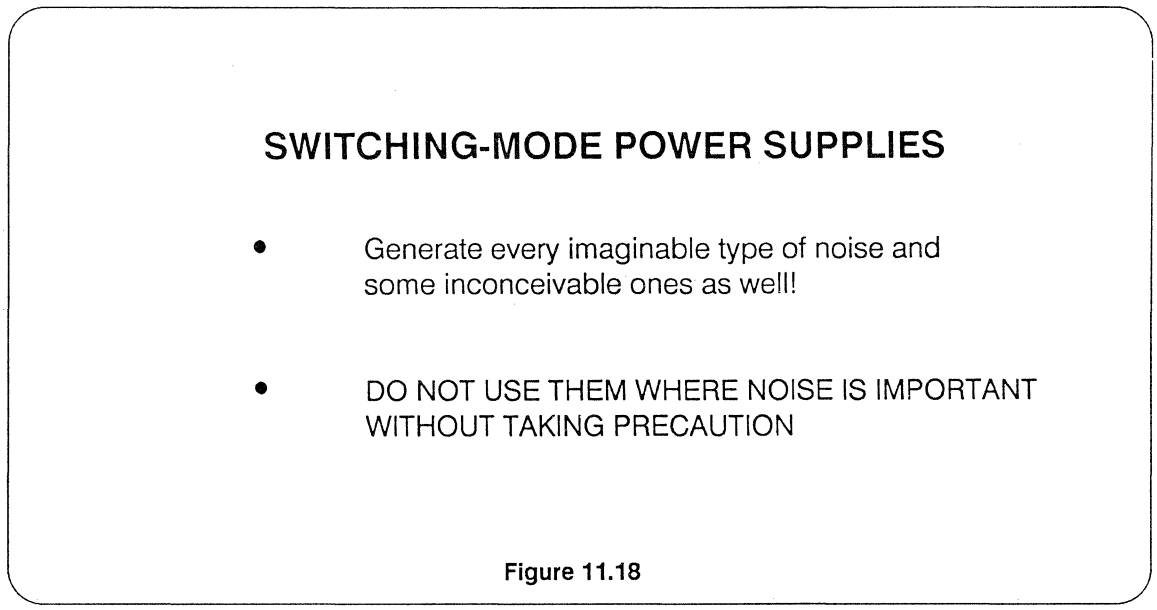


Figure 11.18

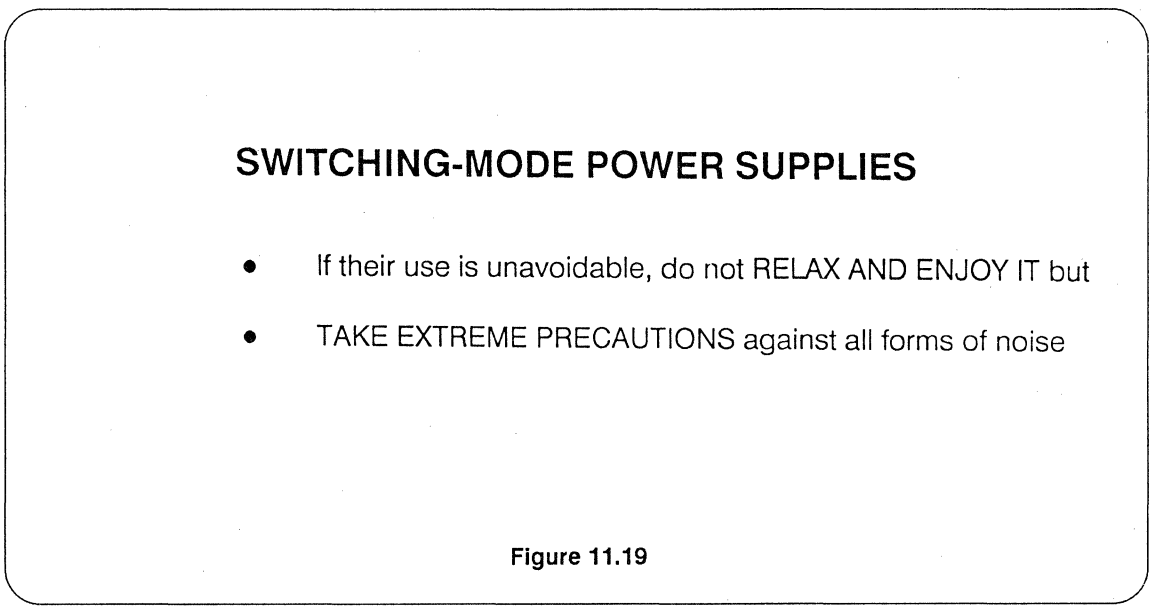
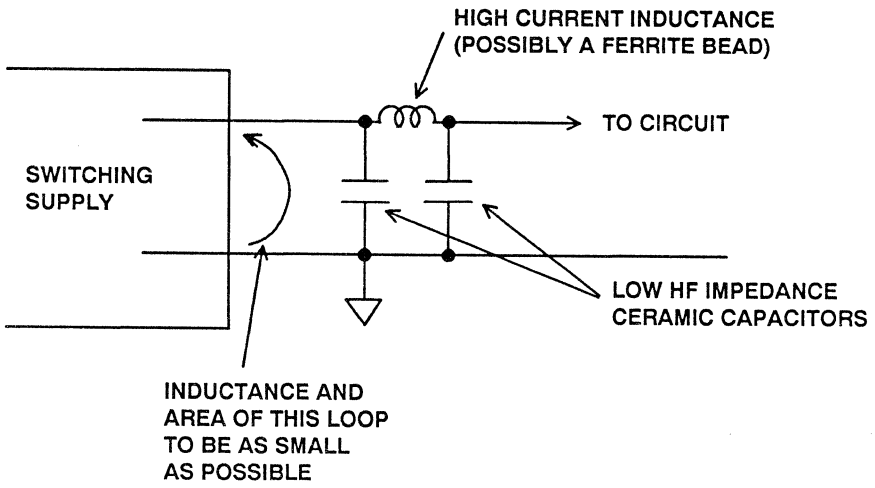


Figure 11.19

It is, unfortunately, not always possible to avoid the use of switching power supplies. Where they must be used, they must be treated with the gravest suspicion, and all possible precautions should be taken to prevent their noise from corrupting the analog circuits that they power. Their input and output lines should be decoupled at all frequencies, they should be shielded to prevent external electric and magnetic fields from causing interference, and they should be sited as far as possible from sensitive circuits so that residual electric and magnetic fields are prevented by distance from causing serious damage.

Where switching supplies are used, it is always worthwhile to remove them temporarily and supply the system with batteries or a low noise bench supply in order to determine if the system performance is being compromised by the switching supply. It often is.

The noise transients on the output lines of switching supplies consist of voltage spikes of very short duration. Large capacitors, such as electrolytic or plastic film types, have considerable inductance and too high an impedance at HF to decouple such spikes satisfactorily. The best output filter for a switching supply will have high value capacitors to remove the low frequency noise which will also be present. In addition, a pi filter using ceramic capacitors, with short leads, having low impedance at HF plus a series inductor (which may be a ferrite bead on the output line) can provide inductive blocking of the spikes. It is possible to buy such a pi filter as a single bulkhead mounted feedthrough component.

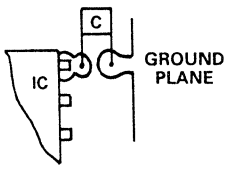


PI - FILTER ON SWITCHING SUPPLY OUTPUT
(SOMETIMES AVAILABLE AS A SINGLE CERAMIC COMPONENT)

Figure 11.20

Power lines in electronic circuitry have decoupling capacitors for two reasons: to remove ripple and noise originating in the power supply, and to remove ripple and noise resulting from modulation of the supply current by the circuitry it feeds. We have discussed the former, but the latter needs more consideration.

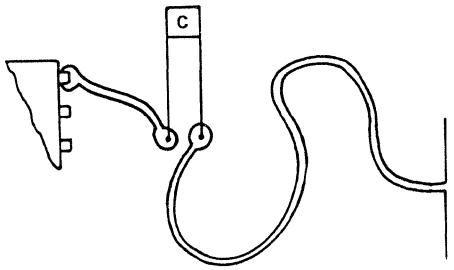
Even low frequency integrated circuits contain transistors having f_t of hundreds of MHz. If the power supply to a circuit behaves as a resonant circuit at a few hundred MHz, it may be possible for the circuit to oscillate. Such oscillation will seriously degrade the performance of the circuit and yet will be too high in frequency to be detected by a standard oscilloscope (indeed, the capacity of the oscilloscope probe may be enough to stop the oscillation). To prevent such parasitic oscillation, and also to restrict high frequency supply currents to the region of the device, all integrated circuit supply pins should be decoupled with a capacitor having low HF reactance and short leads, placed very close to the device (if there are two pins for one supply, both should be decoupled). Ideally, surface-mount capacitors should be used for this purpose, because of their very low inductance, but in most cases monolithic ceramic capacitors with lead lengths of under 2 mm will be satisfactory. Where very low impedance decoupling may be needed, two or more capacitors in parallel should be used.



IDEAL HF DECOUPLING HAS

1. LOW INDUCTANCE CAPACITOR (MONOLITHIC CERAMIC)
2. MOUNTED VERY CLOSE TO THE IC
3. WITH SHORT LEADS
4. AND SHORT, WIDE PC TRACKS

IT MAY BE SHUNTED WITH A TANTALUM BEAD ELECTROLYTIC TO PROVIDE GOOD LF DECOUPLING AS WELL.

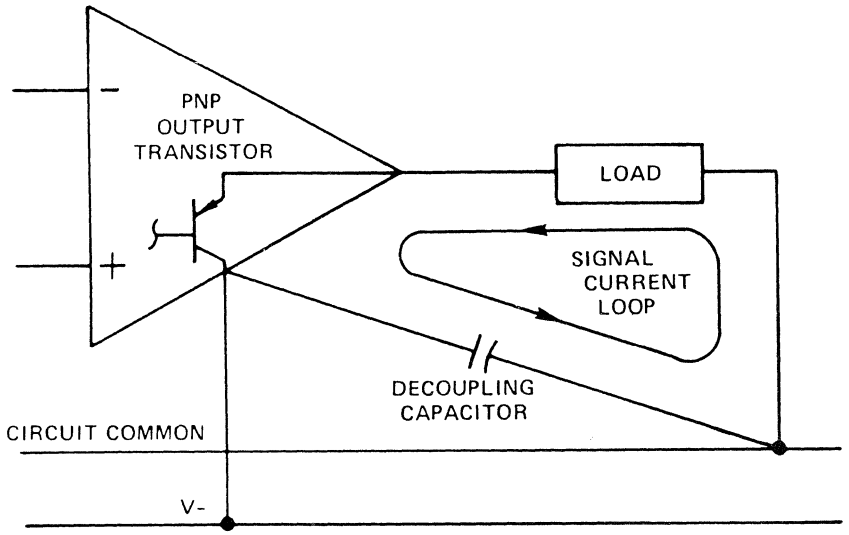


THIS SORT OF THING IS USELESS!

HIGH FREQUENCY DECOUPING
(REQUIRED EVEN BY LF ANALOG CIRCUITS)

Figure 11.21

If the integrated circuit so decoupled is driving a load at HF, Kirchoff's Law tells us that there should be a low impedance between the ground connection to the load and the ground connection of the decoupling capacitor. This topic is more fully covered in an Application Note.[3]

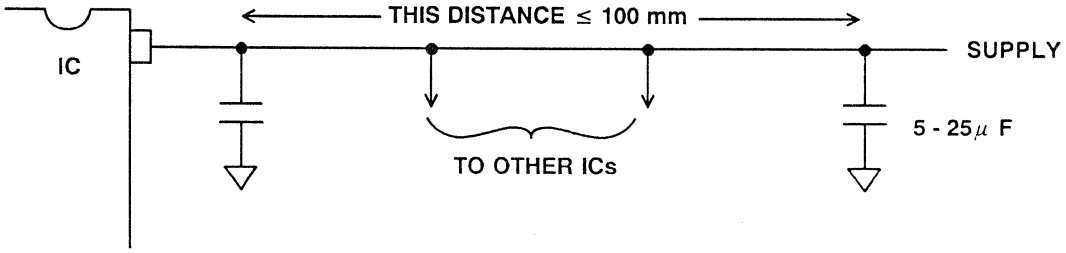


DECOUPLING OF NEGATIVE SUPPLY FOR A GROUNDED LOAD

Figure 11.22

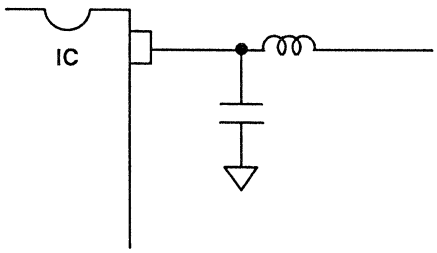
In addition to HF decoupling at every device, it is good practice in high precision circuits to have LF decoupling capacitors of 5-25 μF on all supplies where LF noise could be a problem (in effect this generally means analog circuit supplies, but not necessarily logic supplies). A good rule of thumb is that no IC should be more than 100 mm of circuit track away from such a capacitor, but circumstances will change this. Power supply tracks should be as wide as possible, not just to prevent them from melting from the currents that they carry but to minimize their impedance.

Sometimes low impedance supply lines can be a disadvantage. We have pointed out that any conductor has inductance. The inductance of a power line, combined with a decoupling capacitor, can form an LC resonant circuit which may ring at its resonant frequency when excited by transient currents. In some cases a small series resistance in the power line can be useful in lowering the Q of such a resonant circuit and preventing such effects.



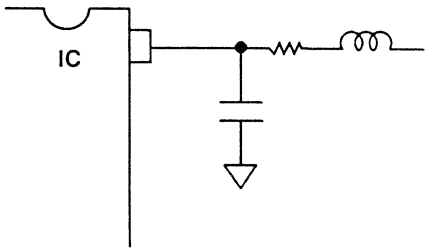
ON-BOARD LF DECOUPLING

Figure 11.23



EQUIVALENT CIRCUIT
OF DECOUPLED POWER
LINE - RESONANT AT

$$f = \frac{1}{2\pi\sqrt{LC}}$$



SMALL SERIES RESISTANCE
CLOSE TO THE IC REDUCES THE Q

RESONANT CIRCUITS FORMED BY DECOUPLED POWER LINES

Figure 11.24

Even with ample decoupling, noise from one part of a circuit can sometimes interfere with another part by coupling through the power supplies. Where such a problem occurs, it is often best to have separate power supplies. In many cases a separate series regulator will be an effective solution, but sometimes a separate transformer winding and rectifier is necessary. The latter expedient offers the further advantage that it may often be connected so as to remove common ground coupling problems as well.

SEPARATE POWER SUPPLIES

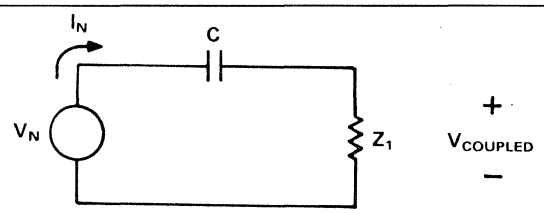
- Separate power supplies help minimize coupling of signals from one part of a system to another.
- Often separate series regulators will provide adequate isolation at low cost.
- In extreme cases completely separate transformer windings, rectifiers and regulators may be necessary to isolate both "supply" and "ground" lines.
- Where supply coupling of noise is suspected replace the supply to one part of the circuit with a battery - and see if the problem is resolved.

Figure 11.25

NOISE - Capacitive coupling

There is a capacitance between any two conductors separated by a dielectric (air or vacuum is a dielectric). If there is a change of voltage on one there will be a movement of charge on the other. The basic model is shown in Figure 11.26.

It is evident that the voltage coupled into Z1 may be reduced by reducing V_n, the frequency involved, the capacitance, or Z1, but frequently none of these can be changed. The best solution is to insert a grounded conductor (known as a Faraday shield) between the noise source and the circuit which it affects.



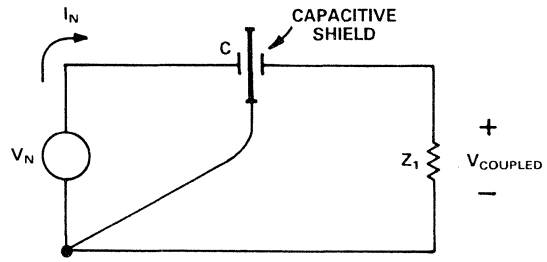
Z_1 = CIRCUIT IMPEDANCE
$Z_2 = 1/j\omega C$

$$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$$

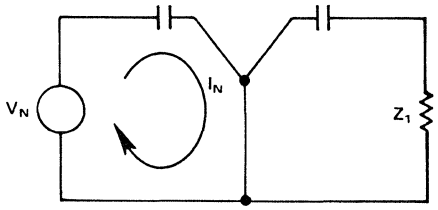
CAPACITIVE COUPLING EQUIVALENT CIRCUIT

Figure 11.26

CAPACITIVE SHIELD INTERRUPTS THE COUPLING ELECTRIC FIELD



EQUIVALENT CIRCUIT ILLUSTRATES HOW A CAPACITIVE SHIELD CAUSES THE NOISE CURRENTS TO RETURN TO THEIR SOURCE WITHOUT FLOWING THROUGH Z_1

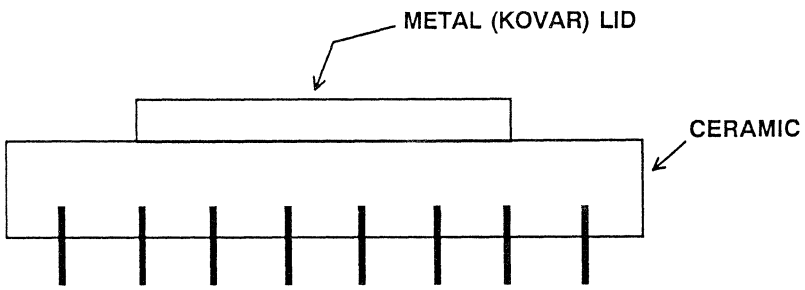


CAPACITIVE SHIELDING

Figure 11.27

The Faraday shield is easily implemented and almost invariably successful. For this reason, capacitively coupled noise is rarely an intractable problem. However, to be effective, the shield must completely block the electric field between the noise source and the shielded circuit and must be connected so that the noise current returns to its source without flowing in any part of the circuit where it might introduce conducted noise. A Faraday shield must never be left unconnected, as this almost always makes capacitively coupled noise worse.

An example of this problem is seen in sidebrazed ceramic IC packages. These D.I.L. packages have a small square conducting kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package or it may be left unconnected. Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Many analog circuits do not have a ground pin at a package corner and the lid is left floating. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic D.I.L. package where the chip is completely unshielded.



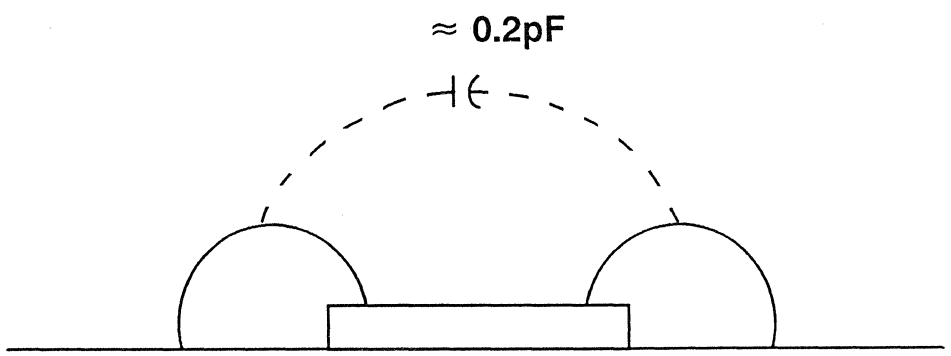
- SIDEBRAZE CERAMIC D.I.L. PACKAGES SOMETIMES HAVE ISOLATED METAL LIDS
- THESE ARE VULNERABLE TO CAPACITIVE INTERFERENCE AND SHOULD BE GROUNDED (IF POSSIBLE)

CAPACITIVE EFFECTS DUE TO METAL LIDS

Figure 11.28

In fact, it is good practice for the user to ground the lid of any sidebrazed ceramic IC where the lid is not grounded by the manufacturer. This can be done with conductive paint from the lid to the ground pin, with a wire soldered to the lid (this will not damage the device if the joint is made reasonably quickly with standard 60:40 solder), or with a phosphor-bronze clip with a tag which is soldered to ground. Never attempt to ground such a lid without verifying that it is, in fact, unconnected, as occasionally device types will be found with the lid connected to a power supply rather than to ground!

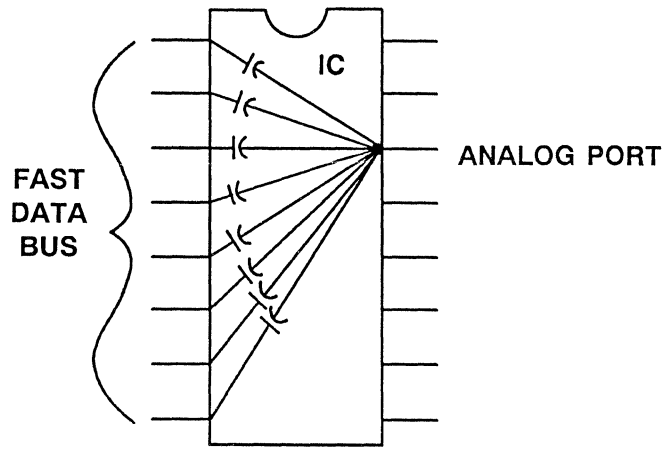
One case where a Faraday shield is impracticable is between the bondwires of an integrated circuit chip. This has important consequences.



STRAY CAPACITY BETWEEN CHIP BONDWIRES

Figure 11.29

The stray capacitance between two chip bondwires is of the order of 0.2 pF. If we have a high resolution converter (ADC or DAC) which is connected to a high speed data bus, then each line of the data bus, which will be carrying noise with 2-5 V/ns dV/dt, is connected to the converter analog port by 0.2 pF. Whenever the bus is active, this will couple intolerable amounts of noise to the analog port and will seriously degrade the performance of the converter.

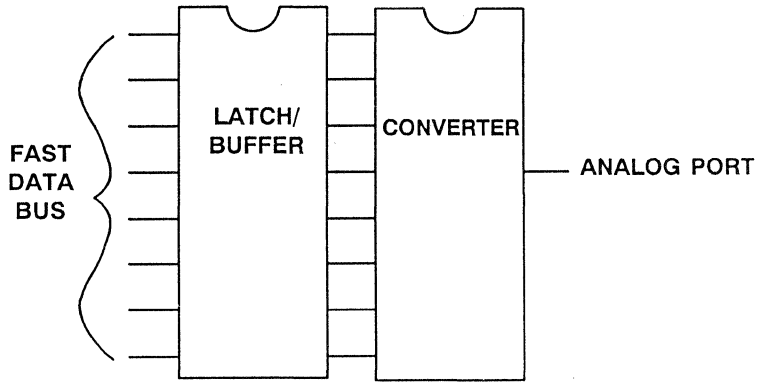


WITH A HIGH PERFORMANCE CONVERTER ON A HIGH SPEED DATA BUS, IT IS NOT POSSIBLE TO SHIELD THE ANALOG PORT FROM THE DIGITAL NOISE

Figure 11.30

Present technology offers no cure for this problem, which also sets serious limits on the performance possible from "mixed signal" ICs having analog and digital circuitry on a single chip. However, it may avoided quite simply by not connecting the databus directly to the converter, but by using a latched buffer as an interface.

This solution costs money, occupies board area, reduces reliability (very slightly), consumes power and complicates design - but it does improve the signal-to-noise ratio of the converter. The designer must decide whether it is worthwhile in individual cases.



- A BUFFER/LATCH CAN ACT AS A FARADAY SHIELD BETWEEN A FAST DATA BUS AND A HIGH PERFORMANCE CONVERTER
- IT ADDS COST, BOARD AREA, POWER CONSUMPTION, RELIABILITY REDUCTION, DESIGN COMPLEXITY AND IMPROVED PERFORMANCE

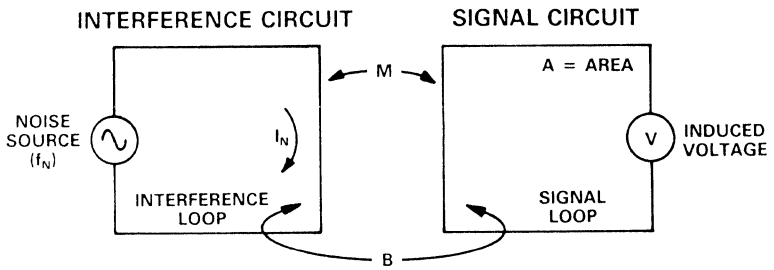
BUFFER LATCH USED AS FARADAY SHIELD

Figure 11.31

NOISE - Inductive Coupling

The mutual inductance of two conductors couples AC signals between them. The basic principle is illustrated in Figure 11.32 and is a common mechanism for the transfer of unwanted signals (noise) between circuits.

As with all other sources of noise, as soon as we define the principle at work, we can see ways of reducing the effect. In this case, reducing any or all of the terms in the equations in Figure 11.32 will reduce the coupling. Reducing the frequency or amplitude of the current causing the interference may be impracticable, but it is frequently possible to reduce the mutual inductance between the interfering and interfered with circuits by reducing loop areas on both sides and, possibly, increasing the distance between them.

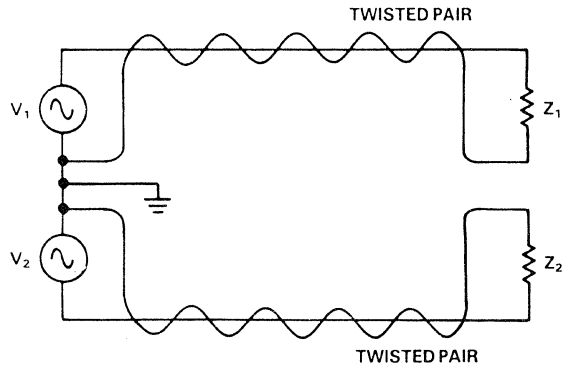


M = MUTUAL INDUCTANCE
B = MAGNETIC FLUX DENSITY
A = AREA OF SIGNAL LOOP
$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE

V = INDUCED VOLTAGE = $\omega_N M I_N = \omega AB$

BASIC PRINCIPLES OF INDUCTIVE COUPLING

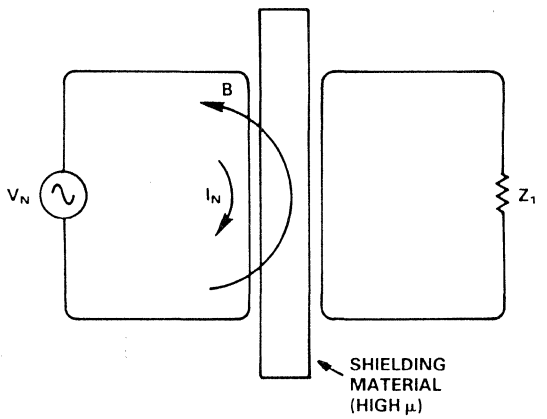
Figure 11.32



PROPER SIGNAL ROUTING REDUCES LOOP AREA

Figure 11.33

Shielding magnetic fields to reduce mutual inductance is sometimes possible ,but is by no means as easy as shielding electric fields with a Faraday shield. HF magnetic fields are blocked by conductive material, while LF and DC fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permiability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.



- Magnetic shielding is not as easily accomplished as electrostatic shielding, but may be done at HF with a simple conducting screen, and at LF and DC with a screen of high permeability material such as Mu-metal.

MAGNETIC SHIELDING

Figure 11.34

NOISE - Electromagnetic Coupling

Noise can enter a circuit as electromagnetic radiation. Circuits can also generate electromagnetic radiation which can interfere with electronic devices at quite considerable distances away. Recent legisation in both the United States and the European Community sets limits on the amount of interference generated and the vulnerability of circuits to such interference.[4] This legislation, and the techniques needed to comply with it, are the subjects of many seminars and training courses, and an Analog Devices Application Note. It is not proposed to cover the topics in detail in this seminar.[5]

ELECTROMAGNETIC NOISE GENERATION

- Circuits must be designed so that external E/M fields are minimized.
- This is done by shielding, decoupling, minimising the area of HF current loops and designing circuits which generate as little EMI as possible.
- IT'S NOT JUST A GOOD IDEA
- IT'S THE LAW!

Figure 11.35

However, the principles of minimizing external radiation are closely related to the principles of low noise design which we have already discussed: high frequency and high dV/dt signals should be screened with Faraday shields, the area of current loops should be minimized, conductors should be decoupled at HF wherever unnecesary HF signals might otherwise occur, and external wires should be isolated with inductors or ferrite beads.

It is still too common at seminars like this to encounter skepticism about the need to protect circuitry from external electromagnetic fields. Even twenty years ago such skepticism was unjustified but today, when transmitters are ubiquitous, it is folly. Besides the more obvious broadcast, emergency and mobile radio services there are cellular and cordless telephones, radar, garage door openers and other remote controls, telemetry, and amateur and CB radio. For any designer to imagine that his circuit will never encounter a radio transmitter during its lifetime is folly on a grand scale.

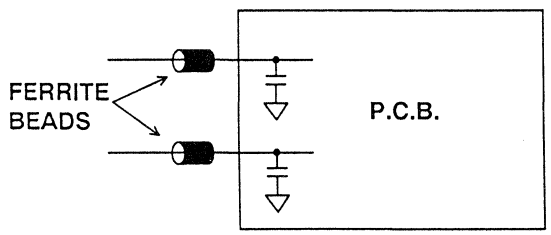
This is particularly so because the design of circuits which are immune to electromagnetic radiation of reasonable levels is not particularly difficult. If every conductor which leaves a PCB is decoupled with a ceramic capacitor and a ferrite bead, it is probable that no further precaution is necessary.

ELECTROMAGNETIC NOISE INTERFERENCE

- The World is full of radio transmitters.
- Police, taxis, broadcast, amateur, CB, cellular and cordless telephones, telemetry and garage door openers.
- Do not imagine that your circuit will never encounter one.

Figure 11.36

A few ports may be more vulnerable and require a pi filter rather than an L filter, and, of course, ports where an HF signal must actually enter or leave the board must be filtered to suppress other EMI but allow the signal to pass unaffected.



IN MANY CASES, ALL THAT IS REQUIRED
IS AN L FILTER, CONSISTING OF A FERRITE BEAD
AND A CAPACITOR, ON EACH EXTERNAL
CONNECTION TO THE BOARD

EMI PREVENTION

Figure 11.37

NOISE - Overall Layout

We have considered sources of noise in circuit design. Having assessed some of the causes of noise and how to minimize them individually, it is worthwhile to consider noise reduction on a complete PCB.

It is evident that we can minimize noise by paying attention to the layout of the whole board and preventing diferent signals from interfering with each other.

High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems, the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

HIGH SPEED PC BOARD SIGNAL ROUTING

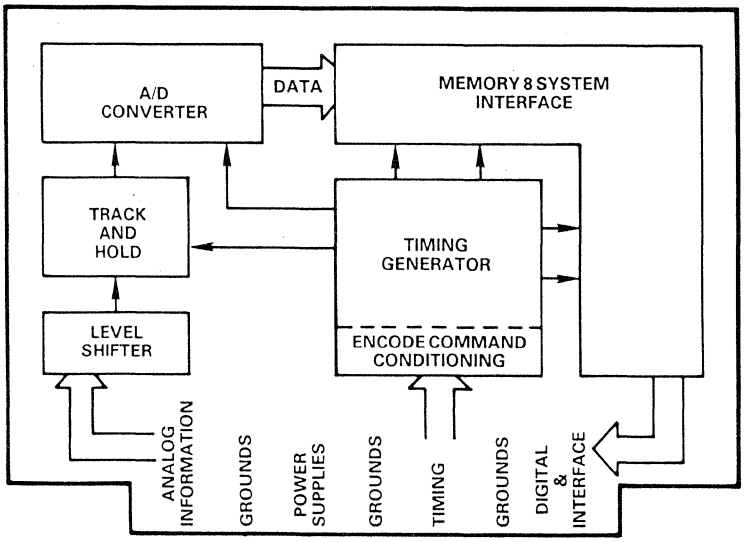
- Physically Separate Analog and Digital Signals
- Avoid Crossovers Between Analog and Digital Signals
- Be Careful with Sampling Clock and A/D Converter Analog Input Runs
- Be Careful with High Impedance Points
- Use Lots of Ground Plane
- Use Microstrip Techniques for Controlled Impedances

Figure 11.38

If a ground plane is used (and it should be in almost all cases) it can be used as a shield where sensitive signals cross. Figure 11.39 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other, and signal paths are kept as short as possible. While real life is frequently not as tidy as this, the principle still applies.

There are several important considerations to the connectors at the edge of the board. First of all, this is the one place in the system where all signal conductors run parallel. It is therefore a good idea to separate them with ground pins to reduce coupling.

Multiple ground pins are important for another reason: to keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10



PCB "FLOW CHART" LAYOUT

Figure 11.39

EDGE CONNECTIONS

- Separate sensitive signals by ground pins
- Keep down ground impedance with multiple (20-30% of total) ground pins
- Have several pins for each power line
- Critical signals may require a separate connector (possibly co-ax)

Figure 11.40

mOhms) when the board is new. As the board gets older, the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 20-30% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

NOISE - Multiple Card Systems

In systems where there are several PCBs, noise may be more of a problem. At first sight it would appear that the problem is similar to that of a single PCB where particular subsystems must be positioned so that harmful interactions are minimized. In a multicard system individual PCBs must be interconnected so that harmful interactions are minimized. There are three problems with this. First of all, there is far less opportunity for rearranging the physical layout of a system consisting of a few cards connected to a common backplane. Secondly, many multicard systems are designed to be reconfigured in a "mix 'n' match" arrangement to allow large numbers of system options. It can be impossible to predict what systems are going to be required and to ensure that all of them are noise free. Finally, multicard systems are likely to have higher ground currents than those occuring on single, relatively simple, PCBs. These currents must flow in the higher impedances which are associated with the intercard connectors, even when multiple ground pins are used.

The basic principles still apply: ground impedance must be as low as possible, high level and low level signals must be separated so that they do not interfere with each other, and capacitance and mutual inductance coupling must be avoided. Nevertheless, it must be accepted that situations can arise where it is not possible to transfer a high speed, high accuracy signal from one PCB to another without unacceptable signal degradation.

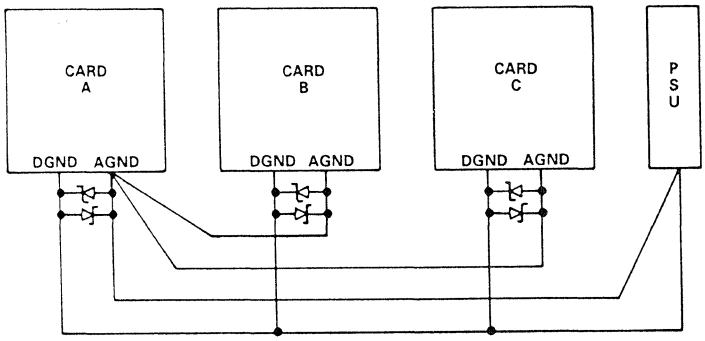
MULTIPLE CARD SYSTEMS

- Multiple card systems are likely to have higher ground currents and higher ground impedances than are found on a single PCB.
- It is therefore more difficult to transfer ground-referenced signals accurately between cards than across a PCB.
- In some cases it will be IMPOSSIBLE to transfer ground-referenced signals between PCBs without unacceptable loss of quality.

Figure 11.41

The best way of minimizing ground impedance in a multicard system is to use another PCB as a backplane and have a ground plane (or even two - one analog, one digital) on that mother card. If the earlier advice about multiple ground pins has been observed, this arangement is capable of excellent performance. Where there are several card cages (racks for PCBs) the ground planes of the several mother boards must be tied together and, probably, to the metal chassis holding the card cages. The exact layout of the inter-connections will depend on the overall system architecture.

If a mother board with a ground plane is not possible, then the ground pins of the PCB sockets must be wired together, with due attention to probable current flows and common ground impedances, with heavy, multi-strand wire, having as low resistance as possible. In many cases the resulting ground screen will be tied to chassis ground at a number of points, but it will sometimes be better to join them at a single star point.

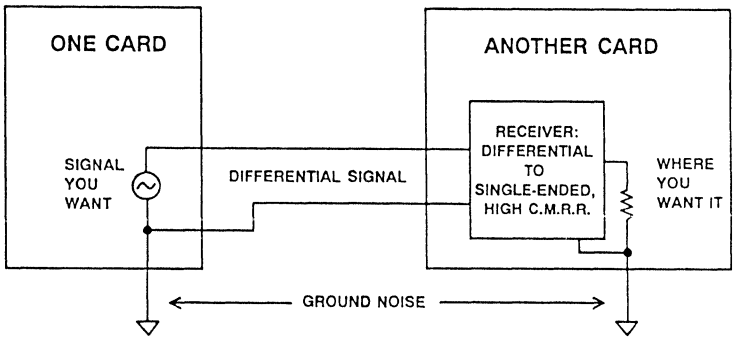


- Schottky diodes protect cards in the event of loss of analog ground
- This grounding system may be inadequate at high resolution or where large ground currents flow
- This MAY permit accurate intercard transmission of ground referenced signals

STAR ANALOG GROUND IN A MULTICARD SYSTEM

Figure 11.42

Modern high performance analog systems handle signals with resolutions of 8 bits at sampling rates of over 500 MHz and resolutions of 14 bits sampled at more than 10 MHz. Preserving signal integrity between cards is extremely difficult and may be impossible.



- At DC and LF the receiver will be an instrumentation amplifier
- At HF the receiver will be a transformer
- There is no ideal receiver for video signals which have components from DC to HF

DIFFERENTIAL TRANSMISSION MINIMIZES GROUND ERRORS

Figure 11.43

The use of balanced transmission lines can help, but if the signal bandwidth extends to DC, there will be a need for a very high performance instrumentation amplifier at the receiving end to restore a ground referenced signal.

The best solution to problems of this sort, and in many cases the only solution, is to partition the system so that the highest quality signals are not required to be transferred to another board.

VIDEO SIGNAL TRANSMISSION

- It is often IMPOSSIBLE to transmit very broadband high accuracy signals between the PCBs of a multicard system without unacceptable loss of quality.
- In such cases the system must be reconfigured to allow all the analog processing to take place on a single PCB.
- It may be inconvenient, but it's the only way you'll get it to work!

Figure 11.44

NOISE - Logic Types

It is well-known that TTL is noisy. This is partly because the "totem pole" output stage structure acts as a short-circuit on the supply for a nanosecond or so during switching. This gives rise to a large current spike, partly because the current flowing in the input changes, and changes quickly, between logic 0 and logic 1, and partly because the output swing, which takes place in a few nanoseconds, is several volts.

High speed CMOS does not have the change in input current (although there is a capacitance charging current pulse during switching, this is smaller) but may draw a supply current pulse during switching, and certainly has a large output swing with a large dV/dt.

ECL, on the other hand, draws almost constant current during switching (unless it is driving asymmetrical loads) and has much smaller output voltage swings. Thus, although ECL is faster than TTL and CMOS, it tends to generate less noise.[6]

In high speed systems where noise is important, therefore, ECL should be used rather than TTL or CMOS where this is possible.

LOGIC NOISE

- TTL & CMOS have large voltage swings, large, fast current pulses and asymmetrical circuitry.
- ECL has smaller voltage swings and smaller current surges, even though it is faster. It is also fully differential.
- ECL is therefore less likely than TTL or CMOS to cause noise in adjacent high speed high precision analog circuits.

Figure 11.45

CONSTRUCTION - IC Sockets

It is tempting to mount expensive high speed components in sockets rather than soldering them in circuit - especially during circuit development.

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon not to degrade the performance of high speed devices (and as the socket ages, and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise).

With skillful use of a "solder sucker" or solder absorbtion wick, it is generally possible to remove and replace a D.I.L. package on a board several times without damage to the device and only minimal damage to the board (it is helpful to use copper loaded "Savebit" solder to do this to prevent the copper PC pads from being dissolved by the repeated soldering operations). If this is completely unacceptable, then individual pin sockets (sometimes called "cage jacks") may be used to make up a multi-pin socket in the PCB itself.

This approach still adds some resistance, inductance and capacitance to the circuit - but less than would be added by any multi-pin socket. Once the circuit is working, and it is obvious that the IC will not need to be removed, it may be soldered into the pin sockets to reduce resistance and the risk of increased resistance with age.

USE OF IC SOCKETS

- Don't!
- Use Individual "Pin Sockets" or "Cage Jacks" for Each Component Pin Such as AMP Part No. 5-330808-3 (Capped) and 5-330808-6 (Uncapped)

Figure 11.46

PROTOTYPING HIGH SPEED CIRCUITS

As we have seen, the circuit board layout is part of the circuit design of all high speed and high precision analog circuits. The primitive prototyping techniques derived from the "node" theory are quite unsuitable for circuits of this type: vector board and wire wrap prototyping will tell the engineer nothing about the behavior of a properly laid out version of the circuit.

The best technique for prototyping is to use a prototype of the final PCB. Certainly no design is complete until the final PCB layout has been proved to give the required performance. Nevertheless this approach may be a little limiting where a number of different possibilities are to be evaluated.

HIGH-SPEED PROTOTYPING

- Do not use vector board or wire-wrap.
- Do not use IC sockets (use pin sockets if you must).
- Use a prototype of your final PCB if you can. (Go to CAD layout as early as possible.)
- Use manufacturers' evaluation boards if possible.
- Pay as much attention to signal routing, component placing and supply decoupling on the prototype as on the final board.
- For "freehand" prototyping use a double-sided copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mount adhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 11.47

In this case, components should be mounted on a board having double-sided continuous copper ground plane, with ground connections made to the plane and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout. In fact, it is a good idea to wire point-to-point in a manner similar to how the traces on the PC board will ultimately be arranged (e.g., no more crossovers than allowed by the number of layers). That is, treat the prototyping phase almost as a PC layout phase.

As we have already indicated, IC sockets can destroy the performance of analog ICs, even in prototype equipments. Again, directly soldered components are best,

pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board). Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributer's addresses are given in the references at the end of this section.[7]

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. In fact, PCB layouts of many high speed evaluation boards are available from Analog Devices in the form of artwork which the users may incorporate into their own PCBs.

When the prototype layout is transferred to a CAD system for PCB layout, it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

HIGH SPEED PROBING TECHNIQUES

A problem often encountered in dealing with high speed circuits is the proper selection and use of high speed oscilloscopes and especially of their associated probes.[8]

In microwave systems, most impedance levels are 50 ohms and signals are transmitted over high quality transmission lines (stripline or co-ax) directly to the 50 ohm input of the oscilloscope. No probes are necessary, and the oscilloscope bandwidth is chosen to be two or three times greater than the maximum signal of interest. Bandwidth (BW) can be calculated from rise time using the approximations:

$$BW = \frac{0.35}{t_R}$$

$t_R = 2.2\ \tau$ where
t_R = Rise time (10% to 90%)
τ = Time constant
(= RC for a single-pole network)

In high speed analog circuits, however, not all high speed signals are necessarily

at 50 ohm levels, and it is often desirable to use a probe with higher impedance to minimize loading effects. If the probe bandwidth is BW_p and the oscilloscope bandwidth is BW_s, then then the approximate overall bandwidth of the measuring system is given by

$$BW_M = \left[\frac{1}{\left(\frac{1}{BW_P}\right)^2 + \left(\frac{1}{BW_S}\right)^2}\right]^{\frac{1}{2}}.$$

For instance, a 400 MHz oscilloscope (Tektronix 2465B) combined with a 400 MHz probe (Tektronix P6137) will yield an overall measurement bandwidth of approximately 280 MHz. The corresponding measurement rise time is 1.2 ns.

In addition to bandwidth, the probe input impedance (both real and imaginary parts) must be considered. There are four basic types of probes: low impedance passive probes, high impedance passive probes, active FET probes and sampling probes.

HIGH SPEED PROBE CONSIDERATIONS

- Grounding - Probe Tip Shield to PC Board Connection < 1 Inch!
- Bandwidth of Measuring System, BW_M:

$$BW_M = \left[\frac{1}{\left(\frac{1}{BW_p}\right)^2 + \left(\frac{1}{BW_s}\right)^2}\right]^{\frac{1}{2}}.$$

  BW_p = Probe Bandwidth
  BW_s = Scope Bandwidth
- BW = $0.35/t_R$, t_R = Rise Time (10% to 90%)
  $t_R = 2.2\,\tau$, τ = Time Constant (RC)
- Capacitance (Loading Effects)
- Resistance (Loading Effects)
- Attentuation
- Overdrive Characteristics

Figure 11.48

A low impedance passive probe and its typical characteristics are shown in Figure 11.49. Successful use of such a probe requires that the ground inductance be kept extremely low. This implies that the ground connection to the PCB ground plane be extremely short. This may be accomplished by using a "bayonet" ground probe sleeve equipped with a short sharpened "pogo pin" ground which connects directly to the probe tip shield ground. These fittings may or may not be part of the standard fittings supplied with the probe - if they are not they will generally be available from the probe manufacturer, whose catalogue should be consulted. In many cases special PCB mounted test jacks are available to provide suitable low impedance plug-in connection of the probe to a PCB.

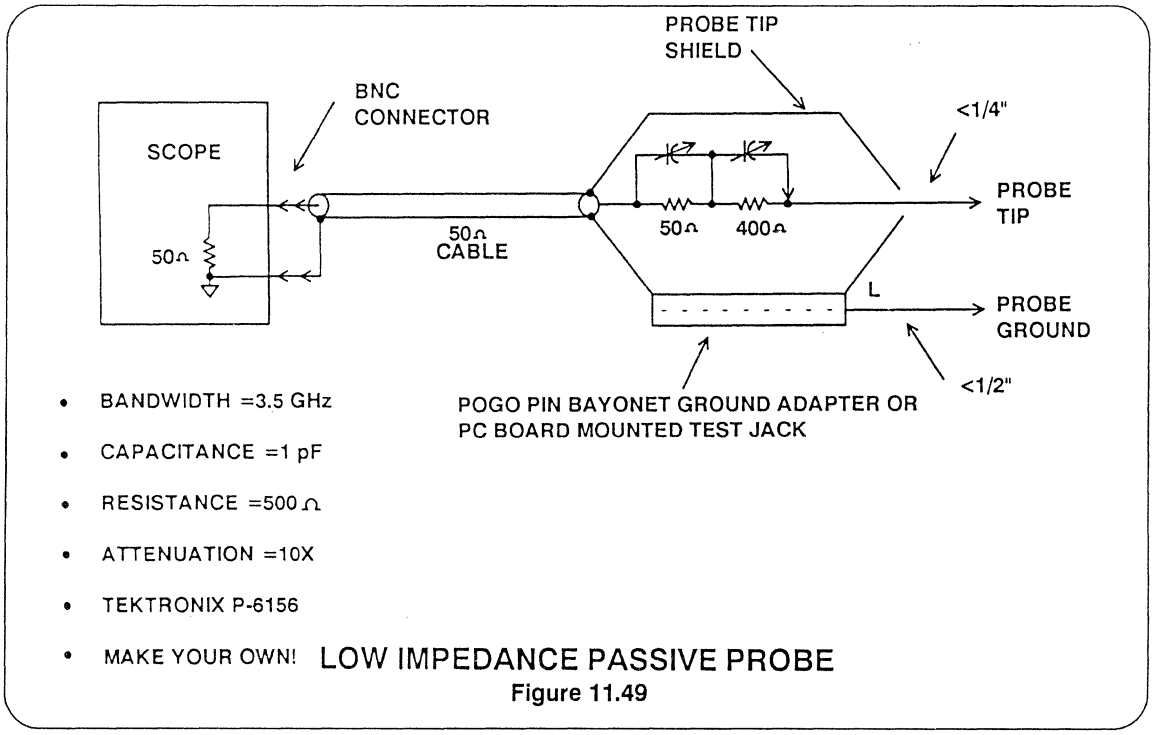


Figure 11.49

The use of long "alligator clip" probe ground leads is pointless at high frequencies, as they hopelessly corrupt the probe performance. To minimize ringing and other perturbations associated with probe ground inductance, the probe tip shield to system ground length should be kept to about 12 mm or less.

It is possible to construct a 500 ohm passive probe. Mount a PCB mounted oscilloscope probe test jack as close as possible to the point in the circuit to be monitored - the shield of the jack being soldered directly to the PCB ground plane. Connect the point in the circuit to be measured to the center conductor of the test jack with a 450 ohm high quality metal film resistor (ideally the jack should be placed so that the resistor leads are just long enough to solder to and not one tenth of a mm longer). The test jack is

connected to the oscilloscope with 50 ohm coaxial cable.

When using this, or any, low impedance probe it is important to consider the effect of the 500 ohm resistive loading on the circuit being measured.

The characteristics of a typical high impedance passive probe are listed in Figure 11.50. This type of probe is standard equipment with wideband analog oscilloscopes. Despite the higher resistance the 10.8 pF capacitance means that the impedance at HF is still quite low (approximately 40 ohms at 400 MHz), and the same precautions must be taken about probe tip shield grounding.

HIGH IMPEDANCE PASSIVE PROBE CHARACTERISTICS

Bandwidth: 400 MHz

Capacitance: 10.8pF

Resistance: 10MΩ

Attentuation: 10X

Example: Tektronix P6137 (Standard with 2465B Portable Scope)

Figure 11.50

HIGH IMPEDANCE ACTIVE FET PROBE CHARACTERISTICS

Bandwidth: 1 GHz

Capacitance: 3pF

Resistance: 100kΩ

Attenuation: 1X

Example: Tektronix P6201

Limited Dynamic Range (±0.6V)

Figure 11.51

The active FET probe, whose characteristics are shown in Figure 11.51, uses an FET amplifier in the probe itself to improve bandwidth and input impedance.

Although active FET probes have high sensitivity and wide bandwidth, their dynamic range is usually limited, and their overdrive recovery may be very slow. If they are overdriven very much, they may never recover at all - a painful and expensive experience. Because of these difficulties, measurements made with FET probes should be viewed with some suspicion - particularly intermodulation measurements.

Figure 11.52 shows the characteristics of two sampling probes, designed to be used with sampling oscilloscopes. They both allow very accurate measurements to be made of repetitive waveforms (sampling oscilloscopes take time-varying samples of successive cycles of a repetitive waveform to build up a picture of the complete wave shape - they cannot be used with single events).

The Data Precision probe is used with the Data Precision 640 digitizing plug-in, and the comparator of the digitizing ADC is located in the probe tip. This allows a vertical resolution of approximately 1 mV/division to be achieved while observing a 5 V step function - with practically no overshoot. Systems of this type are ideal for measuring the settling time, after large steps, of high accuracy, high speed op-amps and DACs.

HIGH SPEED SAMPLING PROBE CHARACTERISTICS

EXAMPLE 1: TEKTRONIX S3A

- Bandwidth: 1 GHz
- Capacitance: 2pF
- Resistance: 100k Ω
- Sensitivity: 2mV/division

EXAMPLE 2: DATA PRECISION 640

- Bandwidth: 1 GHz
- Capacitance: 4pF
- Resistance: 50k Ω
- Sensitivity: < 1mV/division to 5V Step Input
- Settling Time: < 10ns to 0.01% for 5V Step Input

Figure 11.52

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