CROSSPOINT

1992 *Data Book*

CP20K

Field Programmable Gate Arrays

Density.
Speed.
Gate utilization.
Design methodology.

It looks and acts like a gate array. It is one.

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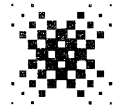


Crosspoint Solutions, Inc.

Crosspoint has built the first field-programmable replacement for standard mask-programmable gate arrays, the true *Field Programmable Gate Array* (FPGA). System designers now have the flexibility and freedom to:

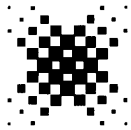
- Experiment with design ideas quickly and inexpensively without having to commit to customized gate arrays
- Move finished designs into production with little delay
- Migrate easily to mask-programmable gate arrays when it is necessary.

The result is a dramatic improvement in productivity, time-to-market, and cost.

Crosspoint's chip architecture and EDA tools are compatible with established gate array architecture and design methodologies. This enables design engineers to use *familiar* gate array tools for schematic entry, synthesis, simulation, timing analysis, Automatic Test Pattern Generation (ATPG), etc.

In addition to delivering superior technical solutions to its customers, Crosspoint is committed to creating the highest *quality* semiconductor, software and hardware products available in the industry. This intent is clearly delineated in Crosspoint's Quality Policy statement:

"Satisfy our customers by consistently exceeding their expectations."



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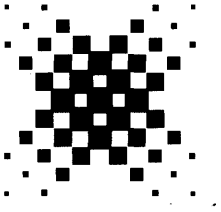
Chapter 1

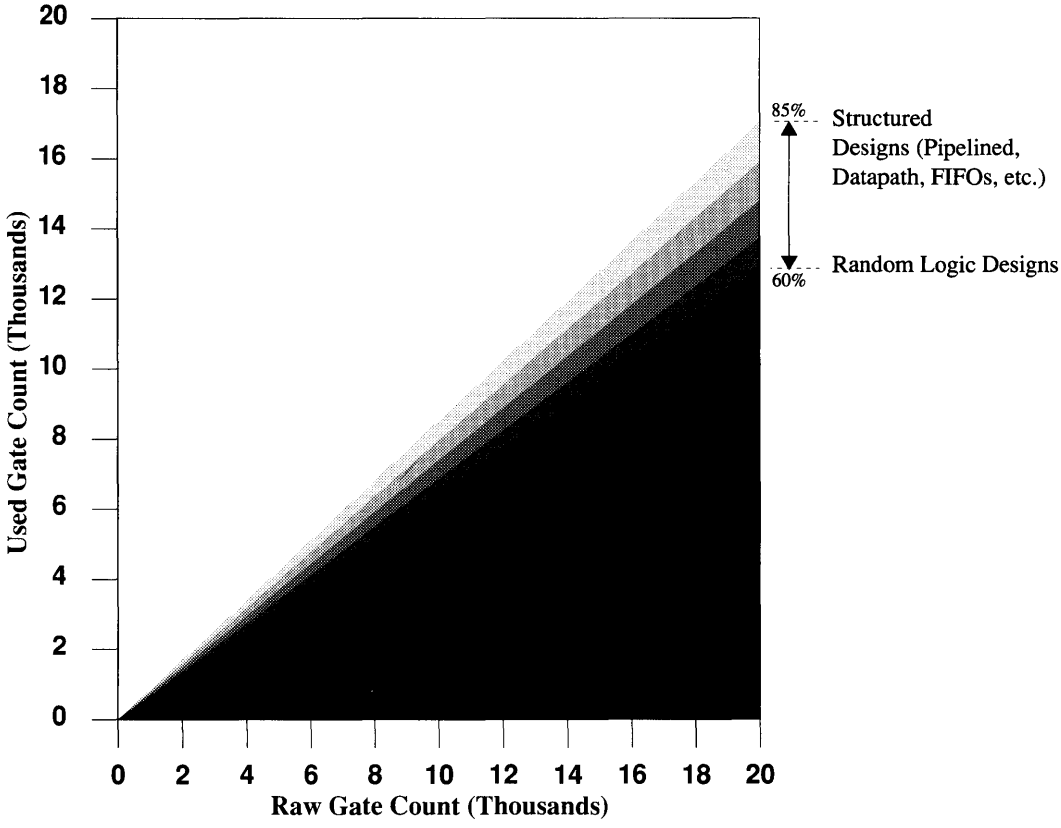
CP20K Series Field-Programmable Gate Arrays



Key Features

- True gate array architecture
  - Transistor-level interconnect programmability
  - Gate array macro library
  - Gate array design methodology
- 50% - 100% faster than other *programmable logic devices* (PLDs)/FPGAs
- Field programmability based on a unique and proprietary low-impedance antifuse technology
- Six density options: 2.2K to 20K available gates
- Four independent clock grids to minimize internal clock skew to less than 1.0 ns
- Flexible I/O configuration
  - Input: CMOS or TTL thresholds with or without pull-up; 7 pins also feature Schmitt thresholds
  - Output: 4mA, 8mA or 12mA drive; three-state; programmable slew rate; open-drain and open-source options
  - Bidirectional: Any combination of the above input and output configurations
- High I/O count
- Flexible memory block implementation
- Built-in IEEE 1149.1 (JTAG) interface
- Design entry, simulation, timing analysis, fault simulation, and test pattern generation done with familiar industry-standard EDA tools
- Gate-level-granularity architecture takes maximum advantage of HDL/Synthesis top-down design methodology
- Automatic and interactive place and route capability for maximum flexibility to fine-tune performance and increase gate utilization.

Figure 1-2
CP20K usable gate capacity



The CP20K Series is manufactured using a high-performance, high-density 0.8 µm CMOS process with two-layer metallization. This process, coupled with Crosspoint's gate array architecture and interconnect scheme, yields performance and design flexibility far superior to other programmable logic alternatives.

Central to Crosspoint's process architecture is a proprietary antifuse technology. An antifuse is a programmable element that has a very high impedance (>100MΩ) initially, but exhibits a low resistance (<100Ω) after programming. Crosspoint's unique antifuse fabrication technique provides antifuse elements with very low capacitance when unprogrammed and very low resistance when programmed. This translates

directly to higher speed, since interconnect RC delays are reduced. The programming is permanent (that is, non-volatile) resulting in a one-time programmable (OTP) device.

Developing FPGAs with gate densities in the 20,000 gate range and system speeds of 40-50 MHz and higher requires an advanced development environment. Crosspoint addresses this need by allowing designers to use the familiar EDA tools for ASIC design and coupling them tightly to the CP20K specific tools for placement and routing.

Designers use existing third-party EDA tools for schematic entry, synthesis, simulation, timing analysis, fault analysis, and test vector generation. The Crosspoint Design System (CDS) is then used to place and route the designs. A choice of automatic or interactive place and route features give the designer maximum flexibility to fine-tune performance. Post-layout simulation uses RC-tree back annotation and provides for certified accuracy on third party tools.

When the design is complete, an antifuse map is generated and downloaded to a Crosspoint FPGA Programmer. The Programmer is connected directly to the user's workstation through a SCSI interface. The Programmer programs the FPGA, and also may perform functional testing if desired. Numerous densities and package options are supported via individual socket adapters.

The JTAG boundary scan is a built-in feature of all CP20K parts. This feature is also used by Crosspoint for the programming and functional testing of each FPGA. The JTAG boundary scan implementation is fully IEEE 1149 compliant and enables board level testing.

Crosspoint Design Environment

Crosspoint's suite of development tools tie into many established Electronic Design Automation (EDA) tool environments for schematic entry, logic synthesis, simulation, timing analysis, fault analysis, test pattern generation, etc. (including those from Cadence, Mentor, Synopsys, Viewlogic and others). This allows users to preserve their investment in EDA tools and training.

Included in the Crosspoint suite of tools are:

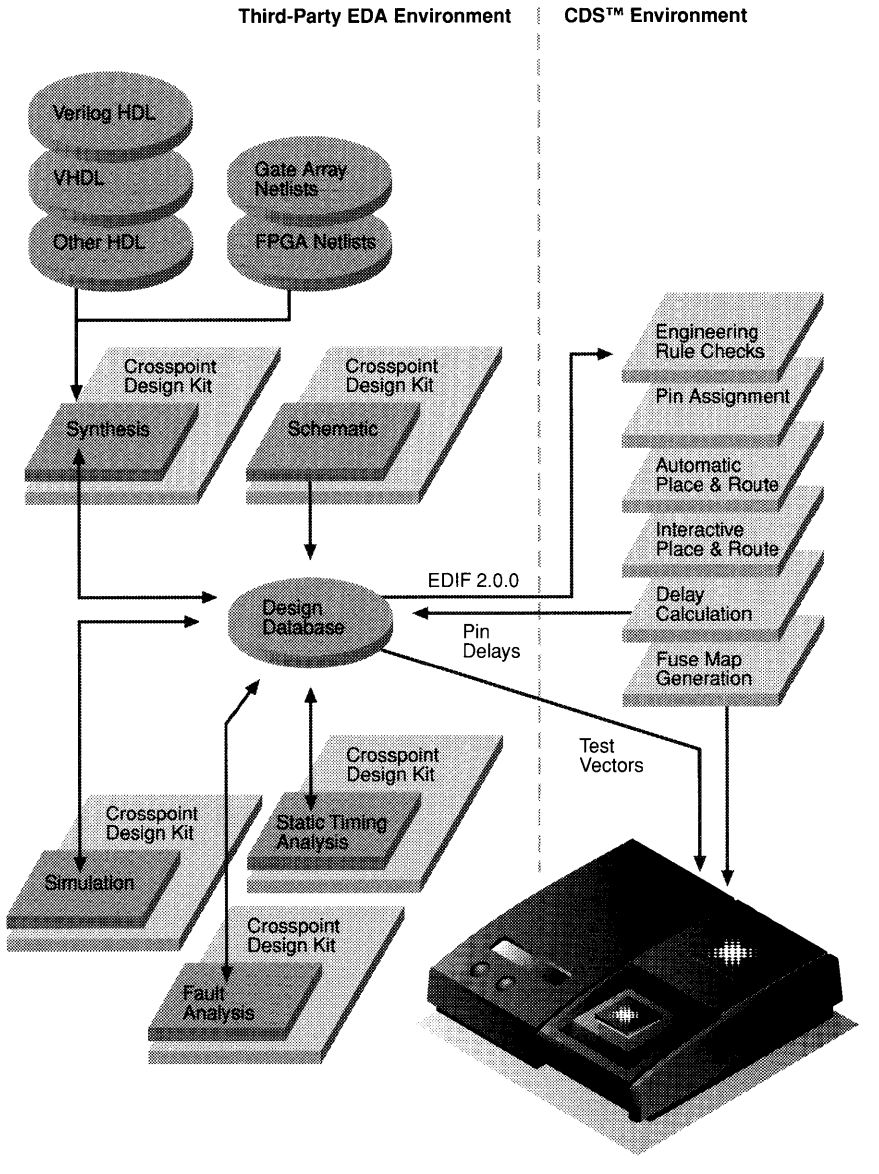
1. A design kit for each third-party EDA environment which allows users to enter and analyze designs using Crosspoint's extensive library of macrocells.

2. The Crosspoint Design System (CDS) for the Crosspoint-specific portions of the design process:

   - Mapping a logic design from an EDA tool into a CP20K FPGA layout
   - Package selection and pin assignment
   - Generating delay for back annotation to an EDA simulator
   - Generating antifuse maps
   - Translating test vectors for the Programmer
   - Communicating with the Programmer during programming and testing of the chips.

The interchange of information between the EDA vendor-specific tools and CDS consists of EDIF netlists, pin delays, and test vectors, as illustrated in Figure 1-3.

Figure 1-3
Third-party EDA tool and Crosspoint Design System Interface



Design Kits

Crosspoint offers Design Kits for the EDA tools listed in Table 1-2.

Table 1-2 Design Kits

Vendor EDA	Synthesis	Schematic	Simulation	Timing Analysis	Fault Analysis
Mentor Graphics 8.X	✔ Autologic 8.X	✔ Design Architect	✔ Quicksim II	✔ Quickpath	* Quickfault/ Quickgrade
Viewlogic	* VHDL Designer II Retargeter II	✔ Viewdraw	✔ Viewsim/SD		
Synopsys	✔ Design Compiler		* VHDL System Simulator	✔	
Cadence			✔ Verilog-XL	* Veritime	* Verifault
Dazix	*†	*†	*†	*†	
Exemplar Logic	*†				

* Future introductions planned.
† To be supported by EDA vendor.

Design Kits include the following modules depending on the EDA tool:

- **Synthesis Models:** Synthesis tools require libraries containing information on the functionality, size, and timing of library macrocells. With these models, a synthesis tool allows the user to optimize design trade-offs such as performance vs. size of the circuit.
- **Schematic Symbols:** Schematic symbols are the graphical representation created for each macrocell.
- **Simulation Models:** Simulation models describe the logical and timing functions of macrocells. These are unique to each supported simulator.

- **Test Vector Translator:** Test vector translators are supplied for all Crosspoint supported simulators. This capability allows the user to convert the stimulus and response vectors from the simulator directly into a form that can be downloaded into the Crosspoint FPGA Programmer. The Programmer then tests the programmed FPGA for proper functionality.

- **Delay Back Annotation:** Each supported simulator can include layout effects in the simulation. Crosspoint supplies simulator-specific tools for back-annotating delay into the design database. Since delays are calculated within ***cptools*** prior to back annotation, each simulator produces identical post-layout timing when using Crosspoint's simulation models with back annotation. Crosspoint Solutions guarantees the simulation timing on any platform using the Crosspoint provided CP20K Design Kit.

Crosspoint Design System (CDS)

When design entry through the third-party tools is completed, the designs are transferred to CDS for placement and routing. Crosspoint offers an integrated suite of automatic and interactive layout tools for this purpose.

A single user interface controls all functions of the tools through pulldown menus, dialog boxes, and keyboard accelerators.

The Crosspoint *place and route* environment provides the following capabilities:

- **EDIF Reader:** This module converts a standard EDIF 2 0 0 netlist into a Crosspoint place and route database.

- **Automatic Placement:** The automatic placement tool is invoked either at the very beginning of the layout phase or after the user is done with hand-placement. The tool optimizes all cell placements that have not been previously placed and frozen.

- **Automatic Routing:** When placement is complete, the automatic routing tool routes all nets in the design that are not frozen.

- **Interactive Placement:** Interactive placement may be used in the layout process for pre-placement of the critical portions of the circuitry. It can also be used after the entire circuit has been placed automatically to rework critical portions of the circuit, to improve gate utilization or timing.

- **Interactive Routing:** Interactive routing gives the user the ability to directly control the routing of individual nets. This is advantageous for pre-routing critical nets, and for fine-tuning a design after the automatic place and route. This function may be performed as a detailed segment-by-segment manual operation, or as a net-by-net automatic route.

- **Delay Calculation:** Net delays are extracted after placement and routing of a design is complete. An accurate RC extraction and delay analysis is performed on each net.

CDS supports some of the most widely used committee and de facto standards that have evolved for EDA tools:

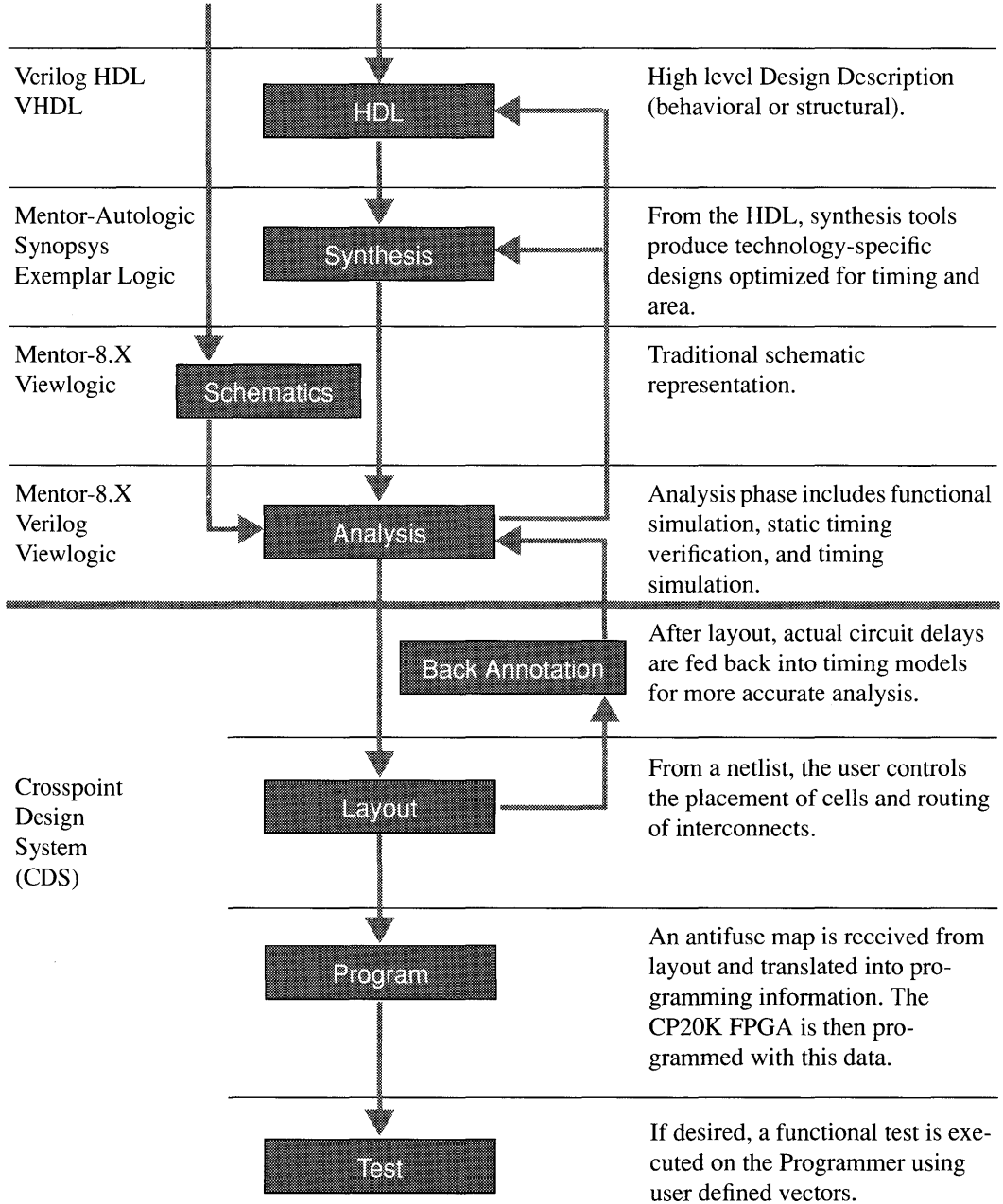
- **X-Windows (X11-R4):** The CDS interface uses X11-R4, the standard X-Windows protocol from MIT. X-Windows is currently supported on virtually all hardware platforms (DEC, DOS/PCs, HP/Apollo, IBM/PC, IBM/RS, Macintosh, Silicon Graphics, SUN, etc.). This windowing technique allows the user to run Crosspoint software in a client/server mode where the X-client can be a SUN or HP/Apollo system, and the X-graphics server is any platform that runs X-11 in server mode.

- **OSF/Motif:** A common *look and feel* across tools relieves the user from having to relearn the user interface for a new tool. The most widely accepted look and feel has been OSF/Motif. This standard defines the look of the screen, buttons, menu structure, coloring, etc. OSF/Motif is currently supported by Cadence, Mentor Graphics, Synopsys, Viewlogic, and other EDA vendors.

- **EDIF 2 0 0:** Crosspoint supports EDIF 2 0 0 as the netlist interface for translating circuits into CDS. EDIF 2 0 0 is supported as a netlist format by Cadence, Mentor Graphics, Synopsys, Viewlogic, and other EDA companies.

- **Hardware Platforms:** CDS resides on commonly available UNIX workstations, such as HP/Apollo and SUN. The software was written in C++ with UNIX platform portability in mind. Additional workstation platforms are planned.

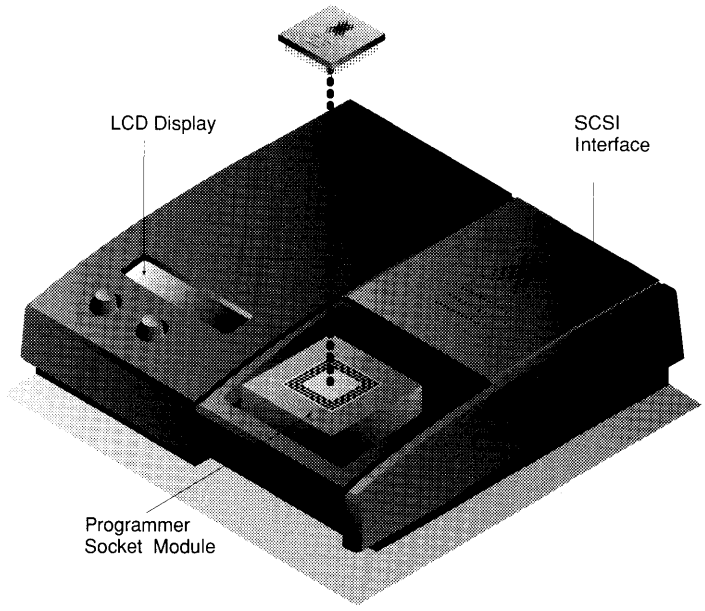
Figure 1-4
Sample customer design process



Programming and Test

The Crosspoint FPGA Programmer/Tester (see Figure 1-5) is used to convert the antifuse map from a completed place and route into a JTAG bitstream, clock the data into a CP20K packaged part and program each required antifuse map. At the end of programming, users can functionally verify the part by applying test vectors.

Figure 1-5
Programmer/Tester



Programmer/Tester Features

- Workstation communication via SCSI interface
- IEEE 1149.1 interface to the device to be programmed
- 2-line by 20-character LCD for soft setup and local status during programming and testing
- Pre-program testing
- Post-program synchronous functional testing
- Socket modules to accommodate all package types.

Workstation User Interface

The interface between the Programmer and the Crosspoint Design System is seamless and intuitive. All operating and data files for the Programmer are stored on the workstation. When a project is selected, all appropriate files are automatically downloaded to the Programmer. Some of the functions performed with this interface are:

- Selection of an active project
- Setup for customer identification register programming
- Translation of simulation vectors for post-program testing
- Post-program testing
- Display results of current action (usually a pass/fail for programming or test).

Pre-Program Testing

Crosspoint implements pre-program testing, consisting of a *fuses open* test and an I/O functionality test. This ensures that:

- The part has not been previously programmed
- The part has not been damaged from improper handling including ESD
- All connections required for programming are present.

Post-Program Testing

Crosspoint's FPGA Programmer also supports post-program testing for synchronous designs. This is a slow-speed synchronous test that checks functionality of the device only, not speed or timing parameters.The test is done through the IEEE 1149.1 interface using the INTEST mode.

Electrical Specifications

Absolute Maximum Ratings*

DC Supply Voltage, V_{CC} ..... -0.5V to +7.0V

DC Programming Voltages, V_{PP}, V_{PB} ..... -0.5 to +10.5V

DC Input Voltage, V_I ..... -0.5V to Vcc +0.5V

DC Input Clamp Current, I_{IK} (V_I<0 or V_I>V_{DD}) ..... ± 20mA

DC Output Current Per Pin (V_O = 0 to V_{CC}) ..... ± 25mA

Storage Temperature, T_{STG}

Ceramic Packages ..... -65°C to +150°C

Plastic Packages ..... -40°C to +125°C

* Stresses beyond these ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* section of this specification is not implied. Exposure to conditions exceeding the absolute maximum ratings for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Commercial Industrial & Military	4.75 4.5	5.25 5.5	V
V_I	Input Voltage		0	V_{CC}	V
V_O	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature	Commercial Industrial Military	0 -40 -55	+70 +85 +125	°C
$t_{R,F}$	Input Rise & Fall Times	Normal Inputs Clock Inputs		250 100	ns

DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-Level Input Voltage TTL Compatible Inputs - Commercial - Industrial & Military CMOS Compatible Inputs		 2.0 2.25 $0.7V_{CC}$	 V_{CC} V_{CC} V_{CC}	V
V_{IL}	Low-Level Input Voltage TTL Compatible Inputs CMOS Compatible Inputs		 0 0	 0.8 $0.3V_{CC}$	V
V_{T+}	Positive-Going Threshold Voltage for Schmitt Trigger Inputs	TTL CMOS*	1.4 2.3	2.4 3.7	V
V_{T-}	Negative-Going Threshold Voltage for Schmitt Trigger Inputs	TTL CMOS*	0.8 1.2	1.8 2.5	V
V_{HYS}	Hysteresis for Schmitt Trigger Inputs	TTL CMOS	0.4 0.5	1.2 1.6	V
I_I	Input Current Inputs with No Pull-up Resistors Inputs with Pull-up Resistors	 $V_I = V_{CC}$ or GND V_I = GND	 -10 -250	 10 -250	µA
V_{OH}	High-Level Output Voltage TTL Levels 4mA Type 8mA Type 12mA Type	 I_{OH} = -4mA I_{OH} = -8mA I_{OH} = -12mA	 3.0		V
	CMOS Levels 2mA Type 4mA Type 8mA Type	I_{OH} = -2mA I_{OH} = -4mA I_{OH} = -8mA	3.7		
V_{OL}	Low-Level Output Voltage 4mA Type 8mA Type 12mA Type	 I_{OL} = 4mA I_{OL} = 8mA I_{OL} = 12mA		0.4	V
I_{OZ}	Three-State Output Leakage Current	$V_O = V_{CC}$ or GND	-10	10	µA
I_{CC}	Quiescent Supply Current	All V_I at V_{CC} or GND Outputs Floating			mA

* Only three JTAG pins and the four clock inputs feature Schmitt trigger as an input option. Other I/O's feature only TTL and CMOS input threshold options.

Timing

Propagation delays in the CP20K FPGAs depend upon the physical implementation of the circuit. After a design has gone through the layout process, the Crosspoint Design System uses layout and cell library data to model circuit timing and provide information necessary to accurately model both propagation delay and timing constraint parameters.

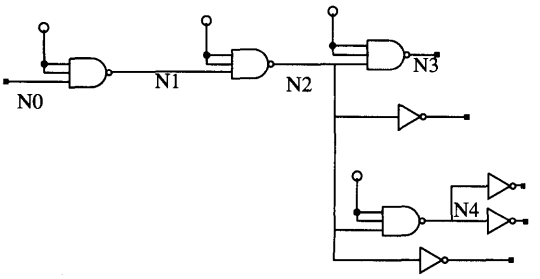
Prior to layout, data provided in this manual can be used to estimate what these timing parameters will be in the completed circuit. This section provides the information needed to correctly interpret timing data and to apply it to the estimation and analysis of circuit timing performance.

Timing Behavior of FPGA Circuits

In order to properly analyze the timing behavior of a circuit implemented in a CP20K array it is necessary to account for the effects of routing interconnect load capacitance and resistance and the intrinsic delay of signals through library components in the design.

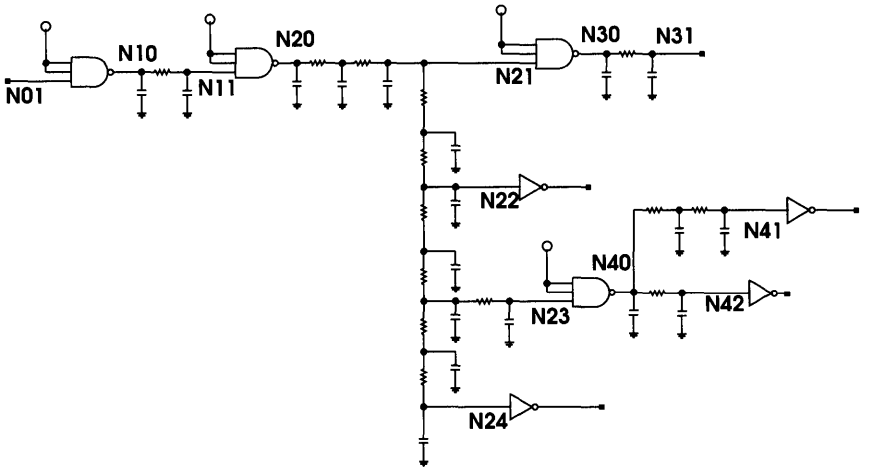
To understand the effect of resistance on a digital circuit, consider the circuit shown in Figure 1-20.

Figure 1-20
Logical schematic



The effect of resistance in the interconnect is to split a single logical net in the digital design into a number of sub-nets, as illustrated in Figure 1-21.

Figure 1-21
Splitting logical nets into physical nets

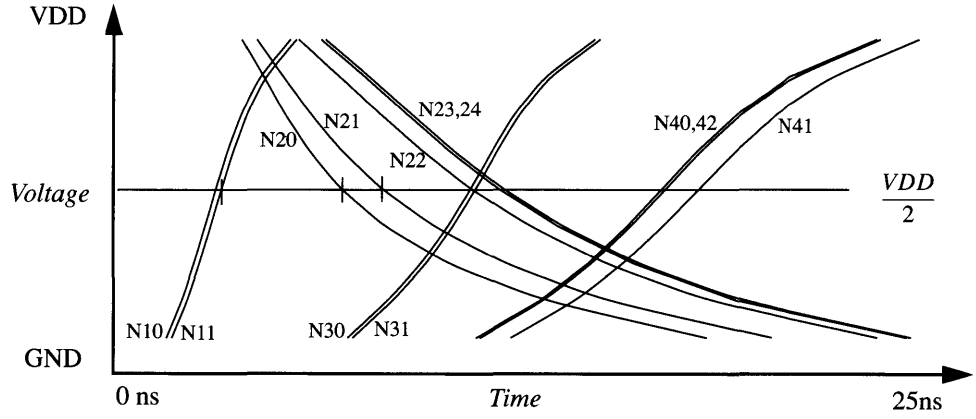


In Figure 1-20, net `N10` and `N11` are subnets formed from a single net (corresponding to the logical net `N1`) by the introduction of a resistor. Similarly, logical nets `N2`, `N3` and `N4` are split into the subnets indicated in Figure 1-21 by the introduction of resistors.

In a CP20K circuit, the principal cause of resistance in interconnect is the presence of antifuses. Except for very long routing segments, wire resistance may be ignored in the interconnect model. Thus, most nets split into interconnect networks with resistors representing antifuses and capacitors representing wire segments.

A SPICE simulation of the above circuit reveals that there is a delay between the signals arriving at each point on an interconnect network. The signal waveforms are plotted (between 10% and 90% of V_{DD}) for each node labeled in Figure 1-22.

Figure 1-22
Actual signal waveforms



Delays are measured by taking the difference between the times when the waveforms of interest cross the voltage $V_{DD}/2$. The delay of the 3-input **NAND** gate between the gate input at node `N11` and the gate output at node `N20` as well as the net delay between nodes `N20` and `N21` illustrate this point.

In summary, the delay through a stage of logic essentially consists of four components:

- The *intrinsic delay* from the cell input pin to the cell output pin that would be observed if the loading or capacitance on both input and output pins were zero.
- The *output transition time* or additional delay through the cell (from input pin to output pin) which is due to the effects of loading on the output pin. This is modeled as the product of an output drive resistance and the output net capacitance.
- The *input slew time* or change in delay through the cell which is due to the effects of loading on the input pin. Essentially, this is the difference between the time at which the signal on the input pin crosses 50% of V_{DD} (the reference point for delay measurement) and the time at which the signal reaches the voltage which physically initiates a transition of the gate (logic threshold voltage). The slew time can be either positive or negative. This is modeled as the product of a slew-rate

factor and a time-constant which is characteristic of the signal on the input pin. The time-constant is approximately the sum of the transition time of the previous stage and the net delay associated with the input net.

- The *net delay* is the time it takes a signal to propagate from a cell output pin, through interconnect wiring, to the next stage input pin. This is modeled by analyzing the RC network representing the interconnect associated with each logical net as described below.

Estimating Delay Prior to Layout

While timing is not determined until after layout, reasonable estimates can be made prior to layout using the *macrocell datasheets*. A much simplified model is used based upon some carefully chosen assumptions and statistical analysis of post-layout timing obtained from several completed FPGA designs.

The key features of the pre-layout timing estimation model are:

- Propagation delay is modeled as the sum of an intrinsic component and a load dependent component. Datasheets list values for intrinsic delay and for the drive factor for each macrocell timing arc (see Equation 1-1).

$$Delay = Intrinsic + (Drive \cdot Load) \qquad \text{(EQ1- 1)}$$

- Capacitance is given in units of standard loads. Each datasheet lists the load for each pin. (A standard load is approximately that of a unit strength inverter.)
- A *wire load* model which lists expected interconnect capacitance, in units of standard load, as a function of net fanout is given in Table 1-7. Add the wire load to that of each pin on the cell's fan-out to obtain the total load for Equation 1-1.
- Net delays, time constants and slew rate effects are accounted for, on a statistical basis only, by modification of cell intrinsic and drive factors and of wire load values. Since these modifications have already been applied to the appropriate tables, they are transparent to the user.
- Derating factors are applied after delays are computed at nominal conditions. Derating factors are either the same for all cells or are given different values for I/O buffers than for internal cells.

Interconnect Wire Load

Table 1-7 tabulates estimated wire capacitance as a function of fanout in standard load units (1 standard load = 0.488 pF) for place and route of typical designs and for optimized layout of critical portions of a design.

Table 1-7 Wire Load per Fanout*

Fanout	Optimized Layout (std load units)	Typical (std load units)
1	2.5	3.6
2	3.5	5.9
3	4.6	8.2
4	5.8	10.5
5	7.2	12.8
6	8.8	15.1
7	10.6	17.4
8	13	19.7
9	16	22.0
10	20	24.2
11	-	26.5
12	-	28.8
13	-	31.1
14	-	33.4
15	-	35.7
16	-	38.0
17	-	40.3
18	-	42.6
19	-	44.9
20	-	47.2
21	-	49.5
22	-	51.8
23	-	54.1
24	-	56.4
25	-	58.7

* Use zero wireload for clock buffers.

It is statistically derived from the analysis of a variety of circuits. Actual wire load may vary significantly from that listed.

Loading for clock distribution networks is included in clock buffer intrinsic timing. For clock buffers, zero wire-load must be used regardless of fanout.

Derating Timing for Best Case/Worst Case Analysis

The timing data in the macrocell datasheets in this manual is for *nominal* conditions. Nominal is defined as worst-case process conditions for -1 speed grade parts (see the following section for a description of speed bins), nominal power supply voltage (5.0 V) and junction temperature of 25 °C. This section describes how to modify estimated delay for other than *nominal* conditions.

Derating timing after it is determined at nominal conditions by using Equation 1-2.

$$delay = (f_{temp} \cdot f_{process} \cdot f_{voltage}) \cdot (delay)_{nominal} \quad \text{(EQ1- 2)}$$

Temperature Derating

The junction temperature will typically be 10 to 40 °C above ambient temperature, depending upon package properties and chip power dissipation. Table 1-8 may be used in most cases as a reasonable guide to the highest and lowest junction temperatures that should be expected when designing to commercial and military specifications:

Table 1-8 Junction Temperatures Ranges for Commercial and Military Specifications

Specification Type	Junction Temperature
Commercial	0° C to 115 °C
Industrial	-40° C to 125 °C
Military	-55° C to 150 °C

The derating factor is determined using Equation 1-3.

$$f_{temp} = 1 + k_T (T_J - 25°C) \quad \text{(EQ1- 3)}$$

where:

Table 1-9 Temperature K-Factors *(Preliminary)*

Cell Type	k_T
Internal Cells	0.0022 per °C
Pad Buffers	0.0022 per °C

Supply Voltage Derating

The voltage derating factors depend upon cell type and, for pad buffers, the transition type. They are listed in Table 1-10 for nominal (5.0V), commercial (4.75 to 5.25) and military (4.5 to 5.5) voltages.

Table 1-10 Voltage Derating Factors *(Preliminary)*

Cell Type	4.5 V_{CC}	4.75 V_{CC}	5.0 V_{CC}	5.25 V_{CC}	5.5 V_{CC}
Internal Cell	1.03	1.02	1.0	0.97	0.97
Output Buffer	1.08	1.04	1.0	0.96	0.93
Input Buffer, Falling Transition	1.05	1.02	1.0	0.98	0.95
Input Buffer, Rising Transition	1.02	1.01	1.0	0.99	0.98
Clock Buffer	1.04	1.02	1.0	0.98	0.96

Process Derating—Speed Bins and Worst/Best Case

Delay depends upon several process factors including transistor drive strength, capacitance and antifuse on-resistance which are fixed when a part is manufactured or, in the case of antifuse resistance, when the part is programmed. A Crosspoint customer may purchase parts which have been tested and qualified according to defined *speed-bins*. For each speed-bin, the FPGA designer may analyze timing under either *worst-case* or *best-case* process conditions.

The derating factors for best and worst case process conditions for each bin are listed in Table 1-11.

Table 1-11 Process Derating Factors *(Preliminary)*

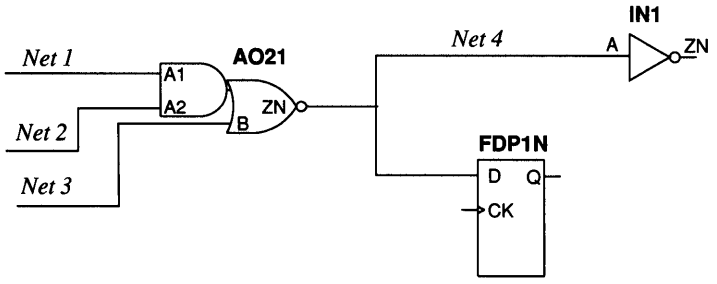
Speed Grade	Worst Case	Best Case
-0	1.4	0.9
-1	1.0	0.7

Estimating Delay Using the Macrocell Datasheets—An Example

The procedure to estimate delay is illustrated using the example in Figure 1-23. Estimation is made for the following conditions:

- 0 degrees C junction temperature
- 5.5 V supply voltage
- -0 speed grade, best case process.

Figure 1-23
Delay calculation example



Use the following steps to find delay:

1. Select a path in the design for analysis, noting all the *hard* macrocells and the fanout of each net in the path. (Soft macros must be decomposed into their hard-macro components.) The example requires the delay between *Net 1* and *Net 4* for the transition *Net 1* rising and *Net 4* falling.

2. Use Table 1-7 to determine the wire load for each net in the path. For clock nets use zero wire load. For output buffers the expected load capacitance should be known and there is no wire load. In this case the fan-out on *Net 4* is 2 and Table 1-7 gives a wire load of 5.9.

3. Use the *macrocell datasheets* to determine the pin loads for each input pin and add to the wire load to arrive at a total load for each net in the path. The example has a load of 1.0 for the IN1 and a load of 0.5 for pin D of FDP1N. Total load on *Net 4* is $5.9 + 1.0 + 0.5 = 7.4$ standard loads.

4. Use the *macrocell datasheets* to determine the delay for each macrocell in the path, given the net loads. For example, refer to the *macrocell datasheet for AO21* and find the entries in the Timing Parameter Table for the transition "A1(↑) to ZN(↓)". The delay may be determined in one of two ways:

   - Use the appropriate value found under the table heading *Delay Given Standard Load*. Either round-off the calculated load (7.4) to the nearest table entry (8.0) or interpolate. The example has a delay of 2.7 ns for a load of 8.
   - Calculate the delay using the intrinsic and drive values given in the table using Equation 1-1. In this case, the delay is $1.42 + 0.165 \times 7.4 = 2.64$ nano-seconds.

   Repeat this procedure for each macrocell in the path of interest and sum the delays. In this example, only a single-stage path is illustrated; the total path delay is 2.6 ns (0.1 ns precision is sufficient).

5. Use Equation 1-3 and Table 1-9 to find the temperature derating factor. Note that the same derating factor is applied to all timing values for a given temperature. The example shows $f_T = 1 + 0.0022 \times (0 - 25) = 0.945$.

6. Use Table 1-10 to find the supply voltage derating. In this case $VCC = 5.5$, the example shows $f_V = 0.97$.

7. Use Table 1-11 to find the process derating. In the case of speed grade -0, best case is $f_P = 0.9$.

8. Multiply the timing values found in step 4 by the derating factors to find the final values. In this case, $2.64 \times 0.945 \times 0.97 \times 0.9 = 2.2$ nano-seconds.

The estimated delay sums the propagation times from cell input-pin to cell input-pin.

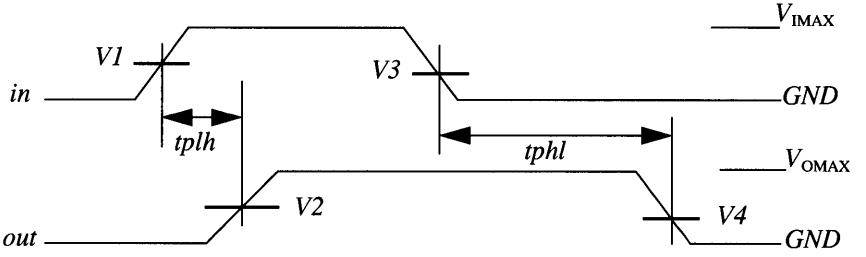
NOTE: In comparing estimated timing to post-layout delay calculator timing the delay calculator sums delays from output-pin to output-pin.

Pad Buffer Delay Measurement Conditions

Delay to and from internal pins of macrocells is measured at 50% of the internal supply voltage. Delay to and from the PAD pin of Pad Buffers and External Clock Buffers is measured as described in this section.

Figure 1-24 shows the propagation of a signal through a buffer from a buffer input to buffer output. The voltage levels *V1*, *V2*, *V3* and *V4* are reference points for timing measurement and the levels V_{IMAX} and V_{OMAX} represent the maximum high voltage level in the logic one state.

Figure 1-24
Signal propagation through a buffer from a buffer input to buffer output



The reference voltage levels for each buffer type are tabulated in Table 1-12 below.

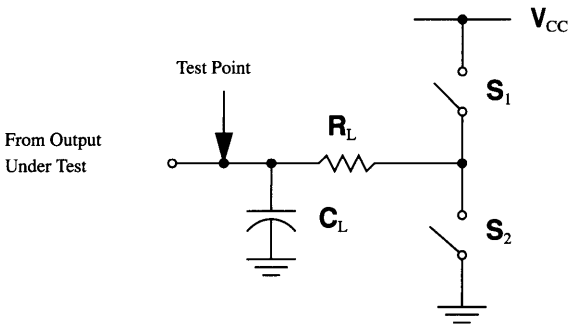
Table 1-12 Buffer Reference Voltages for Delay Measurement*

Buffer Type	V1	V2	V3	V4	VIH	VOH
CMOS Input	50% V_{CC}	50% V_{CCD}	50% V_{CC}	50% V_{CCD}	V_{CC}	V_{CCD}
TTL Input	1.5V	50% V_{CCD}	1.5V	50% V_{CCD}	3.0 V	V_{CCD}
Clock Buffers	50% V_{CC}	50% V_{CCD}	50% V_{CC}	50% V_{CCD}	V_{CC}	V_{CCD}
Driven Output	50% V_{CCD}	1.5 V	50% V_{CCD}	1.5 V	V_{CCD}	V_{CC}
Three-State Output	50% V_{CCD}	10% V_{CC}	50% V_{CCD}	90% V_{CC}	V_{CCD}	V_{CC}

* V_{CCD} is the regulated internal supply voltage.

In the case of buffers with non-driving states, which include three-state, open drain and bidirectional buffers, the load circuit shown in Figure 1-25 is added to the PAD output pin for a timing measurement in which the PAD makes a transition either to or from the undriven "Z" state:

Figure 1-25
Buffers with non-driving states



C_L is the (variable) load capacitance and R_L is fixed at 1 kΩ. The switches are set as illustrated in Table 1-13.

Table 1-13 Switch Setting

Parameter	S1	S2
t_{PZH}	open	closed
t_{PZL}	closed	open
t_{PHZ}	open	closed
t_{PLZ}	closed	open
t_{PLH}	open	open
t_{PHL}	open	open

NOTE: For open drain buffers, S_1 is always closed and S_2 is always open.

Reading the Macrocell Datasheets

This section provides the information necessary to correctly read and interpret the macrocell datasheets. Each individual macrocell datasheet contains the following information:

- Cell Name
- Description of the Cell
- Cell Type
- Resource Utilization
- Function Table
- Symbol
- Schematic
- Timing Parameter Table

Hard and Soft Macros

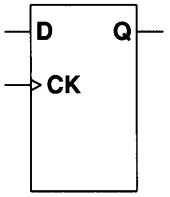
Macrocells and macrofunctions in the Crosspoint library are organized into two categories: *hard macros* and *soft macros*. A soft macro is simply a library component that is designed using other CP20K library macrocells. When expanding an EDIF netlist for placement and routing in ***cptools***, all references to soft macros are replaced with a netlist of hard macros. Only hard macros are placable using ***cptools***. They correspond to predetermined configurations of CP20K resources and are modeled within ***cptools*** for back annotation of timing. Most macrocells are hard macros. Most macro-functions (more complex functions) are soft macros.

• Positive edge triggered D Flip-Flop with single clock input. (1)

(2) • Hard Macrocell
(3) • 6 Gate Equivalents
(4) • 3 TPTs
(5) • 2 RLTs

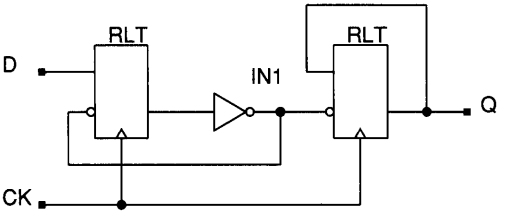
Symbol

(6)



Schematic

(7)



(8)

Function Table

Inputs		Output
CK	D	Q
↑	?	D
1	?	Q
↓	?	Q
0	?	Q

(9)

Pin Load

Pin	Std Load
CK	1.1
D	0.5

(12)

Timing Parameters*

(10) (11) (13)

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)†				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓) with D(0)	2.84	0.113	3.3	3.7	4.2	4.6	5.1
t_{PD}	CK(↑) to Q(↑) with D(1)	2.3	0.179	3.0	3.7	4.4	5.2	5.9
t_S	D(0) setup CK(↑)	3.24	0.000	3.2	3.2	3.2	3.2	3.2
t_S	D(1) setup CK(↑)	3.15	0.000	3.1	3.1	3.1	3.1	3.1
t_H	D(0) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width CK(1) [use load on Q]	2.84	0.179	3.6	4.3	5.0	5.7	6.4
t_W	pulse width CK(0)	3.24	0.000	3.2	3.2	3.2	3.2	3.2

* Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, -1 speed grade parts.
† Sum pin load and wire load to get total load.

Datasheet Definitions

The following list describes the corresponding items in the ***FDP1N*** sample datasheet.

(1) A description of macrocell functionality and notes on usage.

(2) The type of the macrocell indicates how it is placed in ***cptools***. The following types are defined in Table 1-14:

Table 1-14 Macrocell Types

Type	Description
Hard Macrocell	Placed on a TPT or RLT site in a single row.
Soft Macrocell	Expanded into Hard Macrocells prior to placement.
External Buffer	Placed on an I/O buffer site.
Clock Buffer	Placed on a specialized clock buffer site.

(3) The number of equivalent gates is defined as the number of 2-input *NAND* gate equivalents that would be required to implement the same function in a Masked-Programmed Gate Array architecture such as the LSI Logic LCA10K Series.

(4) The number of Transistor-Pair Tile sites used in the macrocell, including that required for gate isolation.

(5) The number of RAM-Logic Tiles used in the macrocell.

(6) The macrocell symbol as it would appear in a schematic.

(7) The macrocell schematic indicates macrocell structure. Refer to hard macrocell datasheets to see composition in transistors and RLTs.

(8) The function table describes logic operation for both combinational and sequential macrocells. A column is listed for each pin and, if needed to define sequential operation, a column for internal state variables. The table may list '0' or '1' to indicated a stable logic value or '?' to indicate either. A row with a '↑' or '↓' on an input pin (usually a clock) indicates the logic function when there is a rising or falling transition (respectively) on that pin. A 'Z' value in an output pin column

indicates an undriven state (three-state). Sometimes an output or state value is indicated by referencing an input value or its negation. For example, an inverter function is specified with a single row, as shown in Table 1-15:

Table 1-15 Function Table for an Inverter

Input	Output
A	ZN
?	$\overline{A}$

⑨ The pin load table indicates pin capacitance in standard load units. A standard load unit is equal to the input capacitance of an inverter (*IN1* macrocell). Loading is listed only for pins that would occur on the fan-out of an internal.

⑩ The timing parameter table lists values for each *timing arc* specified for the macrocell. A timing arc may be either a propagation delay or a timing constraint. The type of timing arc is indicated by the symbol, as shown in Table 1-16.

Table 1-16 Timing Arc Types

Symbol	Description
t_{PD}	Propagation delay
t_S	Minimum set-up or recovery time
t_H	Minimum hold time
t_W	Minimum pulse width
t_{SKEW}	Maximum clock skew (applies to dual phase clock macros only.)

⑪ A statement describing each timing arc is given. Either rising (↑), falling (↓) or static levels (0, 1 or Z) are specified for each pin involved in the transition.

A timing arc is either a path from input to output pin or a timing constraint between two edges on one or two input pins. In most cases the timing arc is identified uniquely in a statement which specifies only the beginning and ending point of the timing arc. For example, A(↑) to ZN(↓) or D(0) setup CK(↑). Occasionally, multiple paths exist for a propagation delay from an input pin to an output pin or a timing constraint may only be specified when the macrocell is in certain states. In these cases it is necessary to specify the values on additional input pins in order to uniquely identify the timing arc. These input pin values are specified using the syntax: *timing_arc* with *input_pin_value_list.*

A statement like *[use load on Q]* is given for timing constraints which depend on an the loading of an output pin.

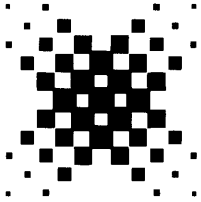
⑫ The Intrinsic and Drive columns may be used to determine the delay or time constraint using Equation 1-4. *Estimating Delay Using the Macrocell Datasheets—An Example* on page 1-46 to see how to determine output pin load.

$$Delay = Intrinsic + (Drive \cdot Load) \qquad \text{(EQ 1-4)}$$

⑬ For convenience, precomputed delays are listed in the table for common values of output loading.

Chapter 2

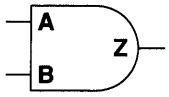
CP20K Macrocell Library



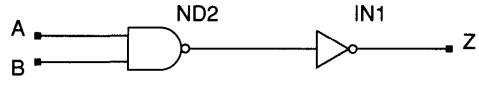
- 2-Input AND

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	Z
0	?	0
?	0	0
1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0

Timing Parameters[1]

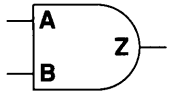
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.46	0.198	2.3	3.0	3.8	4.6	5.4
t_{PD}	A(↓) to Z(↓)	1.57	0.183	2.3	3.0	3.8	4.5	5.2
t_{PD}	B(↑) to Z(↑)	1.53	0.198	2.3	3.1	3.9	4.7	5.5
t_{PD}	B(↓) to Z(↓)	1.62	0.183	2.4	3.1	3.8	4.5	5.3

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

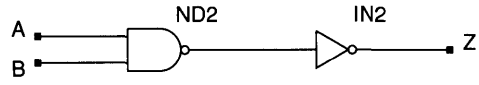
- High drive 2-Input AND

- Hard Macrocell
- 2 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	Z
0	?	0
?	0	0
1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0

Timing Parameters[1]

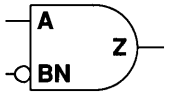
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.71	0.131	2.2	2.8	3.3	3.8	4.3
t_{PD}	A(↓) to Z(↓)	1.71	0.13	2.2	2.8	3.3	3.8	4.3
t_{PD}	B(↑) to Z(↑)	1.77	0.131	2.3	2.8	3.3	3.9	4.4
t_{PD}	B(↓) to Z(↓)	1.73	0.132	2.3	2.8	3.3	3.8	4.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

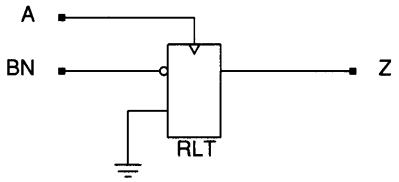
- 2-Input AND with one inverted input.

- Hard Macrocell
- 2 Gate Equivalents
- 0 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	BN	Z
0	?	0
?	1	0
1	0	1

Pin Load

Pin	Std Load
A	0.6
BN	0.4

Timing Parameters[1]

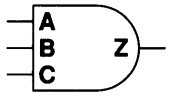
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	A(↓) to Z(↓)	2.28	0.147	2.9	3.5	4.0	4.6	5.2
t_{PD}	BN(↑) to Z(↓)	2.83	0.113	3.3	3.7	4.2	4.6	5.1
t_{PD}	BN(↓) to Z(↑)	2.3	0.25	3.3	4.3	5.3	6.3	7.3

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

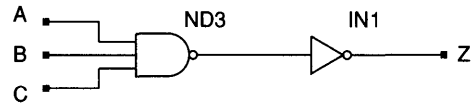
- 3-Input AND

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	Z
0	?	?	0
?	0	?	0
?	?	0	0
1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0

Timing Parameters[1]

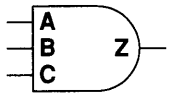
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.74	0.198	2.5	3.3	4.1	4.9	5.7
t_{PD}	A(↓) to Z(↓)	1.74	0.183	2.5	3.2	3.9	4.7	5.4
t_{PD}	B(↑) to Z(↑)	1.83	0.197	2.6	3.4	4.2	5.0	5.8
t_{PD}	B(↓) to Z(↓)	1.89	0.185	2.6	3.4	4.1	4.8	5.6
t_{PD}	C(↑) to Z(↑)	1.87	0.197	2.7	3.4	4.2	5.0	5.8
t_{PD}	C(↓) to Z(↓)	1.88	0.186	2.6	3.4	4.1	4.9	5.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

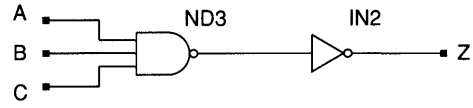
- High drive 3-Input AND

- Hard Macrocell
- 3 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	Z
0	?	?	0
?	0	?	0
?	?	0	0
1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0

Timing Parameters[1]

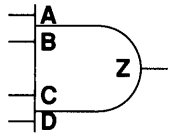
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.99	0.132	2.5	3.0	3.6	4.1	4.6
t_{PD}	A(↓) to Z(↓)	1.85	0.132	2.4	2.9	3.4	4.0	4.5
t_{PD}	B(↑) to Z(↑)	2.06	0.132	2.6	3.1	3.6	4.2	4.7
t_{PD}	B(↓) to Z(↓)	1.97	0.133	2.5	3.0	3.6	4.1	4.6
t_{PD}	C(↑) to Z(↑)	2.1	0.131	2.6	3.2	3.7	4.2	4.7
t_{PD}	C(↓) to Z(↓)	1.96	0.134	2.5	3.0	3.6	4.1	4.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

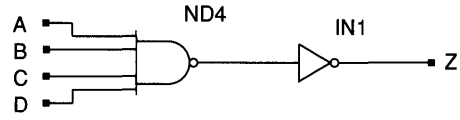
- 4-Input AND

- Hard Macrocell
- 3 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A	B	C	D	Z
0	?	?	?	0
?	0	?	?	0
?	?	0	?	0
?	?	?	0	0
1	1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

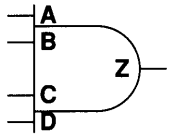
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.9	0.199	2.7	3.5	4.3	5.1	5.9
t_{PD}	A(↓) to Z(↓)	1.8	0.183	2.5	3.3	4.0	4.7	5.5
t_{PD}	B(↑) to Z(↑)	2.03	0.198	2.8	3.6	4.4	5.2	6.0
t_{PD}	B(↓) to Z(↓)	1.96	0.185	2.7	3.4	4.2	4.9	5.7
t_{PD}	C(↑) to Z(↑)	2.1	0.197	2.9	3.7	4.5	5.2	6.0
t_{PD}	C(↓) to Z(↓)	2.09	0.187	2.8	3.6	4.3	5.1	5.8
t_{PD}	D(↑) to Z(↑)	2.13	0.196	2.9	3.7	4.5	5.3	6.1
t_{PD}	D(↓) to Z(↓)	2.03	0.189	2.8	3.5	4.3	5.1	5.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

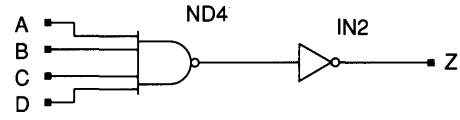
- High drive 4-input AND

- Hard Macrocell
- 3 Gate Equivalents
- 8 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A	B	C	D	Z
0	?	?	?	0
?	0	?	?	0
?	?	0	?	0
?	?	?	0	0
1	1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

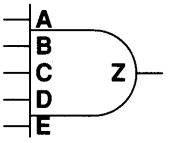
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.16	0.133	2.7	3.2	3.8	4.3	4.8
t_{PD}	A(↓) to Z(↓)	1.92	0.132	2.4	3.0	3.5	4.0	4.6
t_{PD}	B(↑) to Z(↑)	2.27	0.133	2.8	3.3	3.9	4.4	4.9
t_{PD}	B(↓) to Z(↓)	2.04	0.133	2.6	3.1	3.6	4.2	4.7
t_{PD}	C(↑) to Z(↑)	2.33	0.132	2.9	3.4	3.9	4.4	5.0
t_{PD}	C(↓) to Z(↓)	2.14	0.135	2.7	3.2	3.8	4.3	4.8
t_{PD}	D(↑) to Z(↑)	2.37	0.132	2.9	3.4	4.0	4.5	5.0
t_{PD}	D(↓) to Z(↓)	2.09	0.136	2.6	3.2	3.7	4.3	4.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

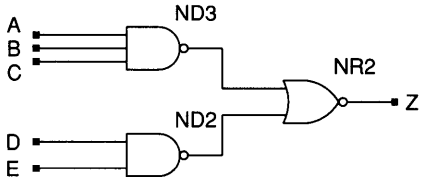
- 5-Input AND

- Hard Macrocell
- 4 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A	B	C	D	E	Z
0	?	?	?	?	0
?	0	?	?	?	0
?	?	0	?	?	0
?	?	?	0	?	0
?	?	?	?	0	0
1	1	1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Timing Parameters[1]

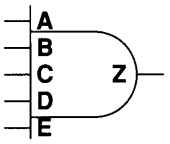
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.07	0.299	3.3	4.5	5.7	6.8	8.0
t_{PD}	A(↓) to Z(↓)	1.78	0.182	2.5	3.2	4.0	4.7	5.4
t_{PD}	B(↑) to Z(↑)	2.2	0.299	3.4	4.6	5.8	7.0	8.2
t_{PD}	B(↓) to Z(↓)	1.93	0.183	2.7	3.4	4.1	4.9	5.6
t_{PD}	C(↑) to Z(↑)	2.27	0.298	3.5	4.7	5.8	7.0	8.2
t_{PD}	C(↓) to Z(↓)	2.04	0.185	2.8	3.5	4.3	5.0	5.7
t_{PD}	D(↑) to Z(↑)	1.9	0.301	3.1	4.3	5.5	6.7	7.9
t_{PD}	D(↓) to Z(↓)	1.67	0.181	2.4	3.1	3.8	4.6	5.3
t_{PD}	E(↑) to Z(↑)	2	0.301	3.2	4.4	5.6	6.8	8.0
t_{PD}	E(↓) to Z(↓)	1.82	0.182	2.5	3.3	4.0	4.7	5.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

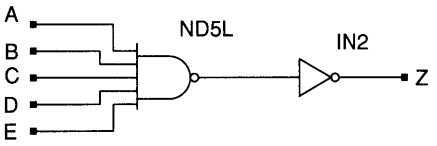
- High drive 5-input AND

- Hard Macrocell
- 4 Gate Equivalents
- 8 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A	B	C	D	E	Z
0	?	?	?	?	0
?	0	?	?	?	0
?	?	0	?	?	0
?	?	?	0	?	0
?	?	?	?	0	0
1	1	1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Timing Parameters[1]

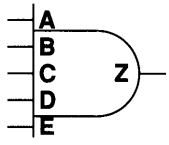
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.44	0.134	3.0	3.5	4.1	4.6	5.1
t_{PD}	A(↓) to Z(↓)	2.07	0.133	2.6	3.1	3.7	4.2	4.7
t_{PD}	B(↑) to Z(↑)	2.57	0.134	3.1	3.6	4.2	4.7	5.2
t_{PD}	B(↓) to Z(↓)	2.19	0.134	2.7	3.3	3.8	4.3	4.9
t_{PD}	C(↑) to Z(↑)	2.67	0.133	3.2	3.7	4.3	4.8	5.3
t_{PD}	C(↓) to Z(↓)	2.29	0.136	2.8	3.4	3.9	4.5	5.0
t_{PD}	D(↑) to Z(↑)	2.72	0.133	3.3	3.8	4.3	4.9	5.4
t_{PD}	D(↓) to Z(↓)	2.38	0.138	2.9	3.5	4.0	4.6	5.1
t_{PD}	E(↑) to Z(↑)	2.75	0.133	3.3	3.8	4.3	4.9	5.4
t_{PD}	E(↓) to Z(↓)	2.3	0.139	2.9	3.4	4.0	4.5	5.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

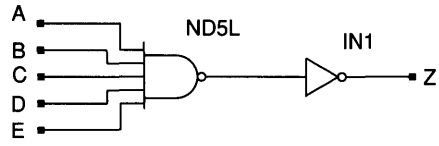
- Low drive, minimum area 5-input AND

- Hard Macrocell
- 3 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A	B	C	D	E	Z
0	?	?	?	?	0
?	0	?	?	?	0
?	?	0	?	?	0
?	?	?	0	?	0
?	?	?	?	0	0
1	1	1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Timing Parameters[1]

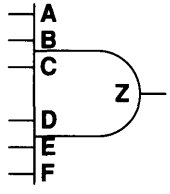
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.18	0.2	3.0	3.8	4.6	5.4	6.2
t_{PD}	A(↓) to Z(↓)	1.96	0.184	2.7	3.4	4.2	4.9	5.6
t_{PD}	B(↑) to Z(↑)	2.33	0.199	3.1	3.9	4.7	5.5	6.3
t_{PD}	B(↓) to Z(↓)	2.12	0.186	2.9	3.6	4.4	5.1	5.8
t_{PD}	C(↑) to Z(↑)	2.43	0.198	3.2	4.0	4.8	5.6	6.4
t_{PD}	C(↓) to Z(↓)	2.25	0.188	3.0	3.8	4.5	5.3	6.0
t_{PD}	D(↑) to Z(↑)	2.49	0.197	3.3	4.1	4.8	5.6	6.4
t_{PD}	D(↓) to Z(↓)	2.36	0.191	3.1	3.9	4.6	5.4	6.2
t_{PD}	E(↑) to Z(↑)	2.51	0.197	3.3	4.1	4.9	5.7	6.4
t_{PD}	E(↓) to Z(↓)	2.25	0.192	3.0	3.8	4.6	5.3	6.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

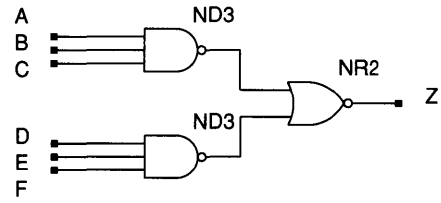
- 6-Input AND

- Hard Macrocell
- 5 Gate Equivalents
- 10 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A	B	C	D	E	F	Z
0	?	?	?	?	?	0
?	0	?	?	?	?	0
?	?	0	?	?	?	0
?	?	?	0	?	?	0
?	?	?	?	0	?	0
?	?	?	?	?	0	0
1	1	1	1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Timing Parameters[1]

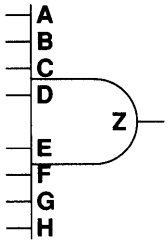
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.06	0.299	3.3	4.4	5.6	6.8	8.0
t_{PD}	A(↓) to Z(↓)	1.78	0.182	2.5	3.2	4.0	4.7	5.4
t_{PD}	B(↑) to Z(↑)	2.18	0.299	3.4	4.6	5.8	7.0	8.2
t_{PD}	B(↓) to Z(↓)	1.92	0.183	2.7	3.4	4.1	4.9	5.6
t_{PD}	C(↑) to Z(↑)	2.24	0.299	3.4	4.6	5.8	7.0	8.2
t_{PD}	C(↓) to Z(↓)	1.97	0.185	2.7	3.5	4.2	4.9	5.7
t_{PD}	D(↑) to Z(↑)	2.1	0.301	3.3	4.5	5.7	6.9	8.1
t_{PD}	D(↓) to Z(↓)	1.82	0.182	2.5	3.3	4.0	4.7	5.5
t_{PD}	E(↑) to Z(↑)	2.23	0.301	3.4	4.6	5.8	7.0	8.2
t_{PD}	E(↓) to Z(↓)	1.97	0.183	2.7	3.4	4.2	4.9	5.6
t_{PD}	F(↑) to Z(↑)	2.3	0.3	3.5	4.7	5.9	7.1	8.3
t_{PD}	F(↓) to Z(↓)	2.08	0.185	2.8	3.6	4.3	5.0	5.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

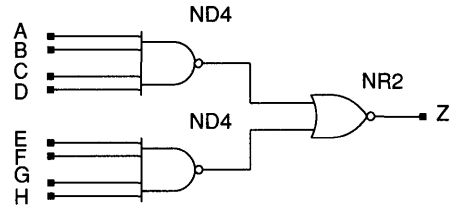
- 8-Input AND

- Soft Macrocell
- 5 Gate Equivalents
- 13 TPTs
- 0 RLTs

Symbol



Schematic



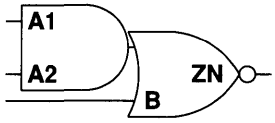
Function Table

Inputs								Output
A	B	C	D	E	F	G	H	Z
0	?	?	?	?	?	?	?	0
?	0	?	?	?	?	?	?	0
?	?	0	?	?	?	?	?	0
?	?	?	0	?	?	?	?	0
?	?	?	?	0	?	?	?	0
?	?	?	?	?	0	?	?	0
?	?	?	?	?	?	0	?	0
?	?	?	?	?	?	?	0	0
1	1	1	1	1	1	1	1	1

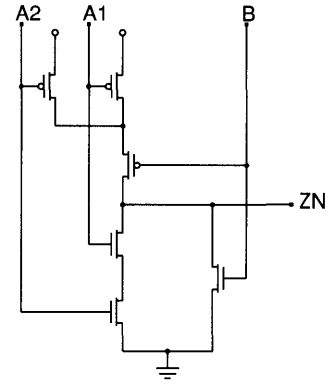
- 2-AND into 2-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A1	A2	B	ZN
1	1	?	0
?	?	1	0
?	0	0	1
0	?	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B	1.0

Timing Parameters[1]

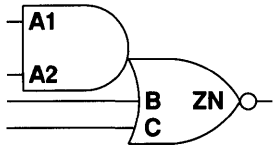
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.42	0.165	2.1	2.7	3.4	4.1	4.7
t_{PD}	A1(↓) to ZN(↑)	0.955	0.435	2.7	4.4	6.2	7.9	9.7
t_{PD}	A2(↑) to ZN(↓)	1.5	0.154	2.1	2.7	3.3	4.0	4.6
t_{PD}	A2(↓) to ZN(↑)	1.04	0.527	3.1	5.3	7.4	9.5	11.6
t_{PD}	B(↑) to ZN(↓)	1.42	0.144	2.0	2.6	3.2	3.7	4.3
t_{PD}	B(↓) to ZN(↑)	0.997	0.527	3.1	5.2	7.3	9.4	11.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

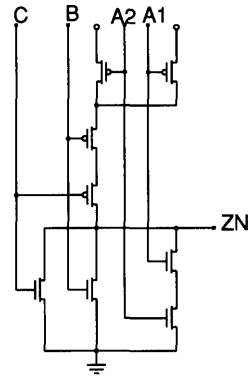
- 2-AND into 3-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A1	A2	B	C	ZN
1	1	?	?	0
?	?	1	?	0
?	?	?	1	0
?	0	0	0	1
0	?	0	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B	1.0
C	1.0

Timing Parameters[1]

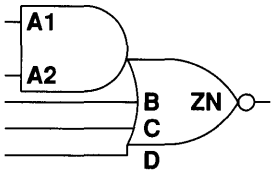
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.65	0.181	2.4	3.1	3.8	4.5	5.3
t_{PD}	A1(↓) to ZN(↑)	1.34	0.595	3.7	6.1	8.5	10.9	13.2
t_{PD}	A2(↑) to ZN(↓)	1.71	0.172	2.4	3.1	3.8	4.5	5.1
t_{PD}	A2(↓) to ZN(↑)	1.6	0.703	4.4	7.2	10.0	12.8	15.7
t_{PD}	B(↑) to ZN(↓)	1.62	0.159	2.3	2.9	3.5	4.2	4.8
t_{PD}	B(↓) to ZN(↑)	1.37	0.698	4.2	7.0	9.7	12.5	15.3
t_{PD}	C(↑) to ZN(↓)	1.56	0.147	2.1	2.7	3.3	3.9	4.5
t_{PD}	C(↓) to ZN(↑)	1.39	0.693	4.2	6.9	9.7	12.5	15.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

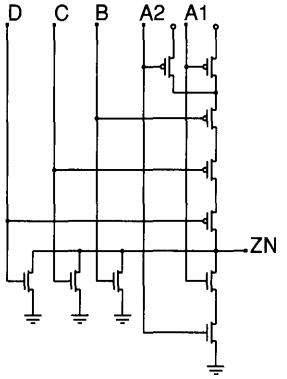
- 2-AND into 4-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A1	A2	B	C	D	ZN
1	1	?	?	?	0
?	?	1	?	?	0
?	?	?	1	?	0
?	?	?	?	1	0
?	0	0	0	0	1
0	?	0	0	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

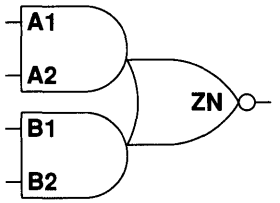
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.78	0.17	2.5	3.1	3.8	4.5	5.2
t_{PD}	A1(↓) to ZN(↑)	1.69	0.761	4.7	7.8	10.8	13.9	16.9
t_{PD}	A2(↑) to ZN(↓)	1.78	0.161	2.4	3.1	3.7	4.3	5.0
t_{PD}	A2(↓) to ZN(↑)	2.17	0.878	5.7	9.2	12.7	16.2	19.7
t_{PD}	B(↑) to ZN(↓)	1.76	0.147	2.3	2.9	3.5	4.1	4.7
t_{PD}	B(↓) to ZN(↑)	1.87	0.869	5.3	8.8	12.3	15.8	19.2
t_{PD}	C(↑) to ZN(↓)	1.66	0.158	2.3	2.9	3.6	4.2	4.8
t_{PD}	C(↓) to ZN(↑)	1.77	0.869	5.2	8.7	12.2	15.7	19.1
t_{PD}	D(↑) to ZN(↓)	1.58	0.159	2.2	2.8	3.5	4.1	4.8
t_{PD}	D(↓) to ZN(↑)	1.66	0.864	5.1	8.6	12.0	15.5	18.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

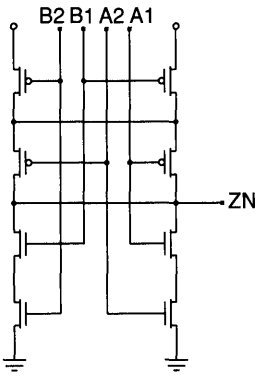
- Two 2-ANDs into 2-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A1	A2	B1	B2	ZN
1	1	?	?	0
?	?	1	1	0
?	0	?	0	1
0	?	?	0	1
?	0	0	?	1
0	?	0	?	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B1	1.0
B2	1.0

Timing Parameters[1]

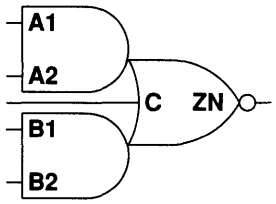
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.49	0.165	2.1	2.8	3.5	4.1	4.8
t_{PD}	A1(↓) to ZN(↑)	1.04	0.527	3.1	5.3	7.4	9.5	11.6
t_{PD}	A2(↑) to ZN(↓)	1.51	0.154	2.1	2.7	3.4	4.0	4.6
t_{PD}	A2(↓) to ZN(↑)	1.25	0.527	3.4	5.5	7.6	9.7	11.8
t_{PD}	B1(↑) to ZN(↓)	1.66	0.165	2.3	3.0	3.6	4.3	5.0
t_{PD}	B1(↓) to ZN(↑)	1.27	0.527	3.4	5.5	7.6	9.7	11.8
t_{PD}	B2(↑) to ZN(↓)	1.66	0.155	2.3	2.9	3.5	4.1	4.8
t_{PD}	B2(↓) to ZN(↑)	1.44	0.527	3.5	5.7	7.8	9.9	12.0

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

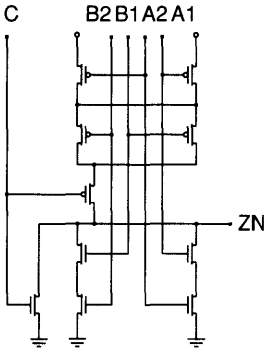
- Two 2-ANDs into 3-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 8 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A1	A2	B1	B2	C	ZN
1	1	?	?	?	0
?	?	1	1	?	0
?	?	?	?	1	0
?	0	?	0	0	1
0	?	?	0	0	1
?	0	0	?	0	1
0	?	0	?	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B1	1.0
B2	1.0
C	1.0

Timing Parameters[1]

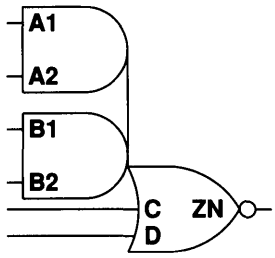
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.93	0.17	2.6	3.3	4.0	4.6	5.3
t_{PD}	A1(↓) to ZN(↑)	2.2	0.8	5.4	8.6	11.8	15.0	18.2
t_{PD}	A2(↑) to ZN(↓)	1.88	0.161	2.5	3.2	3.8	4.4	5.1
t_{PD}	A2(↓) to ZN(↑)	2.57	0.8	5.8	9.0	12.2	15.4	18.6
t_{PD}	B1(↑) to ZN(↓)	1.84	0.178	2.6	3.3	4.0	4.7	5.4
t_{PD}	B1(↓) to ZN(↑)	1.81	0.712	4.7	7.5	10.4	13.2	16.1
t_{PD}	B2(↑) to ZN(↓)	1.83	0.17	2.5	3.2	3.9	4.6	5.2
t_{PD}	B2(↓) to ZN(↑)	2.27	0.795	5.5	8.6	11.8	15.0	18.2
t_{PD}	C(↑) to ZN(↓)	1.69	0.158	2.3	3.0	3.6	4.2	4.9
t_{PD}	C(↓) to ZN(↑)	1.9	0.786	5.0	8.2	11.3	14.5	17.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

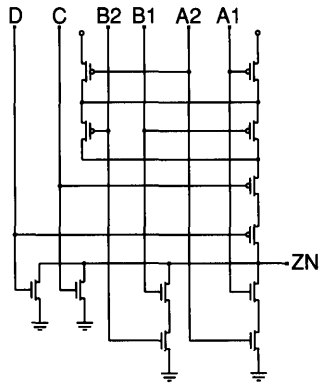
- Two 2-ANDs into 4-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A1	A2	B1	B2	C	D	ZN
1	1	?	?	?	?	0
?	?	1	1	?	?	0
?	?	?	?	1	?	0
?	?	?	?	?	1	0
?	0	?	0	0	0	1
0	?	?	0	0	0	1
?	0	0	?	0	0	1
0	?	0	?	0	0	1

Pin Load

Pin	Std Load
A1	1.7
A2	1.0
B1	1.0
B2	1.0
C	1.0
D	1.0

Timing Parameters[1]

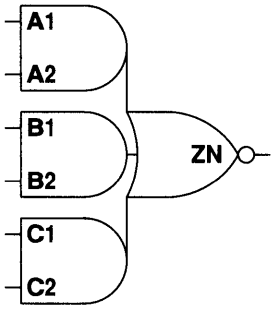
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	2.07	0.181	2.8	3.5	4.2	5.0	5.7
t_{PD}	A1(↓) to ZN(↑)	2.97	0.976	6.9	10.8	14.7	18.6	22.5
t_{PD}	A2(↑) to ZN(↓)	1.97	0.173	2.7	3.4	4.0	4.7	5.4
t_{PD}	A2(↓) to ZN(↑)	3.46	0.976	7.4	11.3	15.2	19.1	23.0
t_{PD}	B1(↑) to ZN(↓)	1.96	0.179	2.7	3.4	4.1	4.8	5.5
t_{PD}	B1(↓) to ZN(↑)	2.41	0.878	5.9	9.4	13.0	16.5	20.0
t_{PD}	B2(↑) to ZN(↓)	1.93	0.171	2.6	3.3	4.0	4.7	5.3
t_{PD}	B2(↓) to ZN(↑)	3.05	0.971	6.9	10.8	14.7	18.6	22.5
t_{PD}	C(↑) to ZN(↓)	1.83	0.157	2.5	3.1	3.7	4.3	5.0
t_{PD}	C(↓) to ZN(↑)	2.41	0.961	6.3	10.1	13.9	17.8	21.6
t_{PD}	D(↑) to ZN(↓)	1.76	0.157	2.4	3.0	3.6	4.3	4.9
t_{PD}	D(↓) to ZN(↑)	2.28	0.956	6.1	9.9	13.8	17.6	21.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

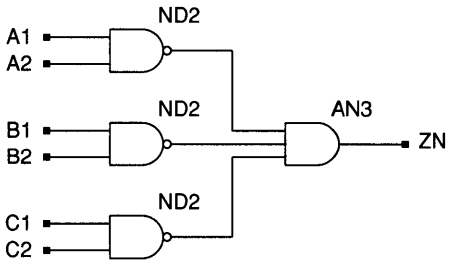
- Three 2-ANDs into 3-NOR

- Soft Macrocell
- 5 Gate Equivalents
- 14 TPTs
- 0 RLTs

Symbol



Schematic



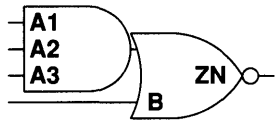
Function Table

Inputs						Output
A1	A2	B1	B2	C1	C2	ZN
1	1	?	?	?	?	0
?	?	1	1	?	?	0
?	?	?	?	1	1	0
?	0	?	0	0	?	1
0	?	?	0	0	?	1
?	0	0	?	0	?	1
0	?	0	?	0	?	1
?	0	?	0	?	0	1
0	?	?	0	?	0	1
?	0	0	?	?	0	1
0	?	0	?	?	0	1

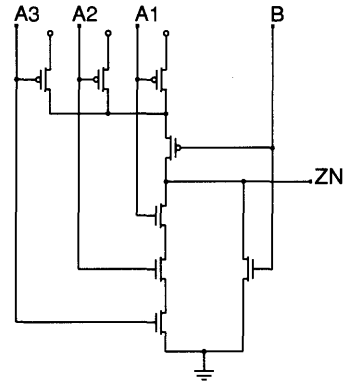
- 3-AND into 2-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A1	A2	A3	B	ZN
1	1	1	?	0
?	?	?	1	0
?	?	0	0	1
?	0	?	0	1
0	?	?	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
B	1.0

Timing Parameters[1]

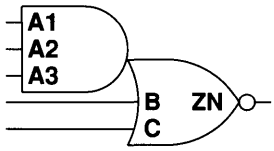
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.45	0.184	2.2	2.9	3.7	4.4	5.1
t_{PD}	A1(↓) to ZN(↑)	1.05	0.435	2.8	4.5	6.3	8.0	9.8
t_{PD}	A2(↑) to ZN(↓)	1.58	0.174	2.3	3.0	3.7	4.4	5.1
t_{PD}	A2(↓) to ZN(↑)	1.16	0.527	3.3	5.4	7.5	9.6	11.7
t_{PD}	A3(↑) to ZN(↓)	1.59	0.167	2.3	2.9	3.6	4.3	4.9
t_{PD}	A3(↓) to ZN(↑)	1.33	0.527	3.4	5.5	7.7	9.8	11.9
t_{PD}	B(↑) to ZN(↓)	1.53	0.144	2.1	2.7	3.3	3.8	4.4
t_{PD}	B(↓) to ZN(↑)	1.27	0.527	3.4	5.5	7.6	9.7	11.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

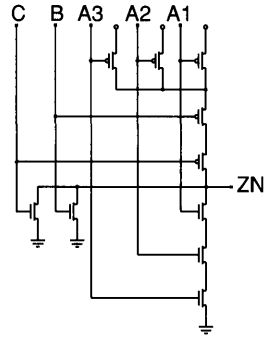
- 3-AND into 3-NOR

- Hard Macrocell
- 2 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A1	A2	A3	B	C	ZN
1	1	1	?	?	0
?	?	?	1	?	0
?	?	?	?	1	0
?	?	0	0	0	1
?	0	?	0	0	1
0	?	?	0	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
B	1.0
C	1.0

Timing Parameters[1]

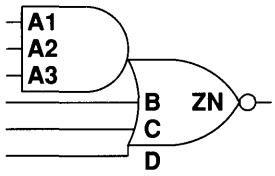
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.74	0.206	2.6	3.4	4.2	5.0	5.9
t_{PD}	A1(↓) to ZN(↑)	1.53	0.595	3.9	6.3	8.7	11.1	13.4
t_{PD}	A2(↑) to ZN(↓)	1.86	0.199	2.7	3.5	4.2	5.0	5.8
t_{PD}	A2(↓) to ZN(↑)	1.82	0.708	4.7	7.5	10.3	13.1	16.0
t_{PD}	A3(↑) to ZN(↓)	1.87	0.194	2.6	3.4	4.2	5.0	5.8
t_{PD}	A3(↓) to ZN(↑)	2.08	0.708	4.9	7.7	10.6	13.4	16.2
t_{PD}	B(↑) to ZN(↓)	1.75	0.165	2.4	3.1	3.7	4.4	5.1
t_{PD}	B(↓) to ZN(↑)	1.8	0.703	4.6	7.4	10.2	13.0	15.9
t_{PD}	C(↑) to ZN(↓)	1.67	0.149	2.3	2.9	3.5	4.1	4.6
t_{PD}	C(↓) to ZN(↑)	1.84	0.698	4.6	7.4	10.2	13.0	15.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

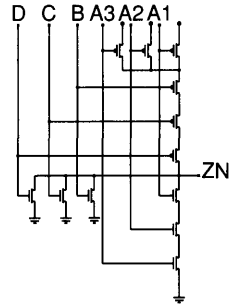
- 3-input AND into a 4-input NOR

- Hard Macrocell
- 3 Gate Equivalents
- 8 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A1	A2	A3	B	C	D	ZN
1	1	1	?	?	?	0
?	?	?	1	?	?	0
?	?	?	?	1	?	0
?	?	?	?	?	1	0
?	?	0	0	0	0	1
?	0	?	0	0	0	1
0	?	?	0	0	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

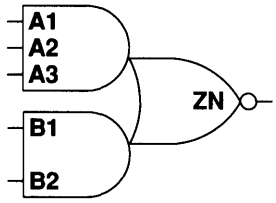
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.98	0.198	2.8	3.6	4.4	5.2	5.9
t_{PD}	A1(↓) to ZN(↑)	2.22	0.791	5.4	8.5	11.7	14.9	18.0
t_{PD}	A2(↑) to ZN(↓)	2.03	0.19	2.8	3.6	4.3	5.1	5.8
t_{PD}	A2(↓) to ZN(↑)	2.79	0.908	6.4	10.1	13.7	17.3	20.9
t_{PD}	A3(↑) to ZN(↓)	1.96	0.185	2.7	3.4	4.2	4.9	5.7
t_{PD}	A3(↓) to ZN(↑)	3.22	0.908	6.9	10.5	14.1	17.7	21.4
t_{PD}	B(↑) to ZN(↓)	1.97	0.155	2.6	3.2	3.8	4.4	5.1
t_{PD}	B(↓) to ZN(↑)	2.89	0.903	6.5	10.1	13.7	17.3	20.9
t_{PD}	C(↑) to ZN(↓)	1.83	0.188	2.6	3.3	4.1	4.8	5.6
t_{PD}	C(↓) to ZN(↑)	2.8	0.903	6.4	10.0	13.6	17.2	20.9
t_{PD}	D(↑) to ZN(↓)	1.74	0.188	2.5	3.2	4.0	4.8	5.5
t_{PD}	D(↓) to ZN(↑)	2.67	0.898	6.3	9.9	13.4	17.0	20.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.. Sum wire and input pin load to get total load.

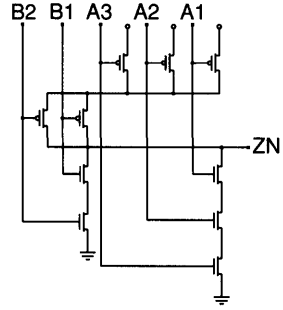
- 3-AND, 2-AND into 2-NOR

- Hard Macrocell
- 5 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A1	A2	A3	B1	B2	ZN
1	1	1	?	?	0
?	?	?	1	1	0
?	?	0	?	0	1
?	0	?	?	0	1
0	?	?	?	0	1
?	?	0	0	?	1
?	0	?	0	?	1
0	?	?	0	?	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
B1	1.0
B2	1.0

Timing Parameters[1]

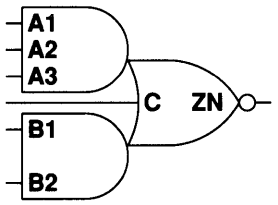
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.72	0.184	2.5	3.2	3.9	4.7	5.4
t_{PD}	A1(↓) to ZN(↑)	1.38	0.527	3.5	5.6	7.7	9.8	11.9
t_{PD}	A2(↑) to ZN(↓)	1.77	0.175	2.5	3.2	3.9	4.6	5.3
t_{PD}	A2(↓) to ZN(↑)	1.57	0.527	3.7	5.8	7.9	10.0	12.1
t_{PD}	A3(↑) to ZN(↓)	1.76	0.168	2.4	3.1	3.8	4.4	5.1
t_{PD}	A3(↓) to ZN(↑)	1.74	0.532	3.9	6.0	8.1	10.3	12.4
t_{PD}	B1(↑) to ZN(↓)	1.62	0.164	2.3	2.9	3.6	4.2	4.9
t_{PD}	B1(↓) to ZN(↑)	1.31	0.527	3.4	5.5	7.6	9.7	11.9
t_{PD}	B2(↑) to ZN(↓)	1.62	0.154	2.2	2.8	3.5	4.1	4.7
t_{PD}	B2(↓) to ZN(↑)	1.53	0.527	3.6	5.7	7.9	10.0	12.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

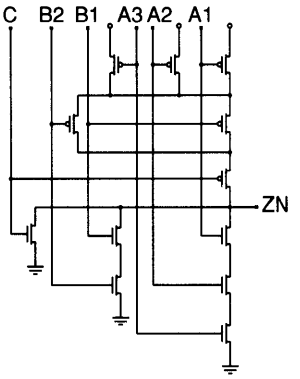
- 3-AND, 2-AND into 3-NOR

- Hard Macrocell
- 5 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A1	A2	A3	B1	B2	C	ZN
1	1	1	?	?	?	0
?	?	?	1	1	?	0
?	?	?	?	?	1	0
?	?	0	?	0	0	1
?	0	?	?	0	0	1
0	?	?	?	0	0	1
?	?	0	0	?	0	1
?	0	?	0	?	0	1
0	?	?	0	?	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
B1	1.0
B2	1.0
C	1.0

Timing Parameters[1]

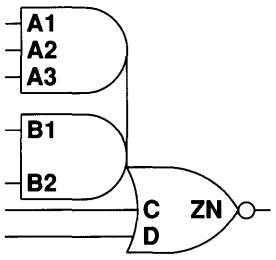
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	2.09	0.2	2.9	3.7	4.5	5.3	6.1
t_{PD}	A1(↓) to ZN(↑)	2.58	0.805	5.8	9.0	12.2	15.5	18.7
t_{PD}	A2(↑) to ZN(↓)	2.1	0.192	2.9	3.6	4.4	5.2	5.9
t_{PD}	A2(↓) to ZN(↑)	2.95	0.81	6.2	9.4	12.7	15.9	19.2
t_{PD}	A3(↑) to ZN(↓)	2.05	0.187	2.8	3.5	4.3	5.0	5.8
t_{PD}	A3(↓) to ZN(↑)	3.3	0.81	6.5	9.8	13.0	16.3	19.5
t_{PD}	B1(↑) to ZN(↓)	1.98	0.178	2.7	3.4	4.1	4.8	5.5
t_{PD}	B1(↓) to ZN(↑)	2.29	0.722	5.2	8.1	11.0	13.8	16.7
t_{PD}	B2(↑) to ZN(↓)	1.95	0.17	2.6	3.3	4.0	4.7	5.3
t_{PD}	B2(↓) to ZN(↑)	2.82	0.805	6.0	9.3	12.5	15.7	18.9
t_{PD}	C(↑) to ZN(↓)	1.81	0.157	2.4	3.1	3.7	4.3	5.0
t_{PD}	C(↓) to ZN(↑)	2.44	0.795	5.6	8.8	12.0	15.2	18.3

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

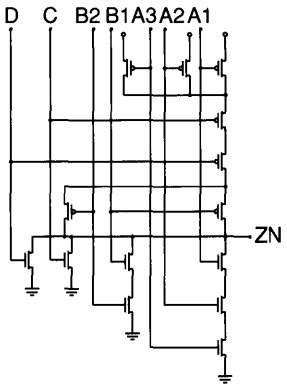
- 3-input AND and 2-input AND into a 4-input NOR

- Hard Macrocell
- 5 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs							Output
A1	A2	A3	B1	B2	C	D	ZN
1	1	1	?	?	?	?	0
?	?	?	1	1	?	?	0
?	?	?	?	?	1	?	0
?	?	?	?	?	?	1	0
?	?	0	?	0	0	0	1
?	0	?	?	0	0	0	1
0	?	?	?	0	0	0	1
?	?	0	0	?	0	0	1
?	0	?	0	?	0	0	1
0	?	?	0	?	0	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
B1	1.0
B2	1.0
C	1.0
D	1.0

Timing Parameters[1]

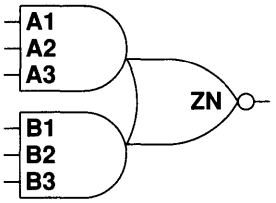
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	2.21	0.2	3.0	3.8	4.6	5.4	6.2
t_{PD}	A1(↓) to ZN(↑)	3.27	0.874	6.8	10.3	13.8	17.2	20.7
t_{PD}	A2(↑) to ZN(↓)	2.21	0.193	3.0	3.8	4.5	5.3	6.1
t_{PD}	A2(↓) to ZN(↑)	4.05	0.986	8.0	11.9	15.9	19.8	23.8
t_{PD}	A3(↑) to ZN(↓)	2.12	0.188	2.9	3.6	4.4	5.1	5.9
t_{PD}	A3(↓) to ZN(↑)	4.52	0.986	8.5	12.4	16.3	20.3	24.2
t_{PD}	B1(↑) to ZN(↓)	1.9	0.206	2.7	3.6	4.4	5.2	6.0
t_{PD}	B1(↓) to ZN(↑)	2.45	0.903	6.1	9.7	13.3	16.9	20.5
t_{PD}	B2(↑) to ZN(↓)	1.88	0.203	2.7	3.5	4.3	5.1	5.9
t_{PD}	B2(↓) to ZN(↑)	3.26	0.976	7.2	11.1	15.0	18.9	22.8
t_{PD}	C(↑) to ZN(↓)	2.14	0.156	2.8	3.4	4.0	4.6	5.3
t_{PD}	C(↓) to ZN(↑)	4.12	0.981	8.0	12.0	15.9	19.8	23.7
t_{PD}	D(↑) to ZN(↓)	2.13	0.188	2.9	3.6	4.4	5.1	5.9
t_{PD}	D(↓) to ZN(↑)	3.97	0.981	7.9	11.8	15.7	19.7	23.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

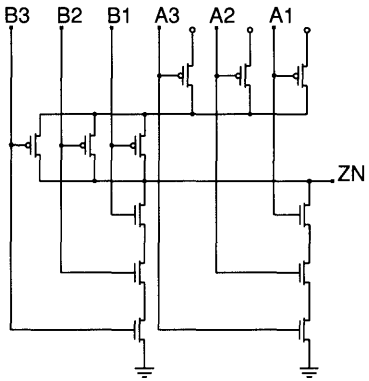
- Two 3-ANDs into 2-NOR

- Hard Macrocell
- 5 Gate Equivalents
- 8 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A1	A2	A3	B1	B2	B3	ZN
1	1	1	?	?	?	0
?	?	?	1	1	1	0
?	?	0	?	?	0	1
?	0	?	?	?	0	1
0	?	?	?	?	0	1
?	?	0	?	0	?	1
?	0	?	?	0	?	1
0	?	?	?	0	?	1
?	?	0	0	?	?	1
?	0	?	0	?	?	1
0	?	?	0	?	?	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
B1	1.0
B2	1.0
B3	1.0

Timing Parameters[1]

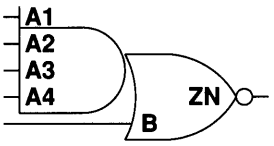
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.97	0.183	2.7	3.4	4.2	4.9	5.6
t_{PD}	A1(↓) to ZN(↑)	1.84	0.527	3.9	6.1	8.2	10.3	12.4
t_{PD}	A2(↑) to ZN(↓)	1.99	0.174	2.7	3.4	4.1	4.8	5.5
t_{PD}	A2(↓) to ZN(↑)	2.03	0.532	4.2	6.3	8.4	10.5	12.7
t_{PD}	A3(↑) to ZN(↓)	1.96	0.167	2.6	3.3	4.0	4.6	5.3
t_{PD}	A3(↓) to ZN(↑)	2.2	0.532	4.3	6.5	8.6	10.7	12.8
t_{PD}	B1(↑) to ZN(↓)	1.74	0.183	2.5	3.2	3.9	4.7	5.4
t_{PD}	B1(↓) to ZN(↑)	1.52	0.527	3.6	5.7	7.8	10.0	12.1
t_{PD}	B2(↑) to ZN(↓)	1.78	0.173	2.5	3.2	3.9	4.6	5.2
t_{PD}	B2(↓) to ZN(↑)	1.74	0.527	3.8	6.0	8.1	10.2	12.3
t_{PD}	B3(↑) to ZN(↓)	1.76	0.166	2.4	3.1	3.8	4.4	5.1
t_{PD}	B3(↓) to ZN(↑)	1.94	0.527	4.0	6.2	8.3	10.4	12.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

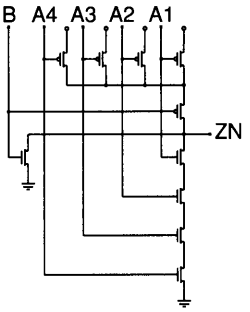
- 4-AND into 2-NOR

- Hard Macrocell
- 4 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A1	A2	A3	A4	B	ZN
1	1	1	1	?	0
?	?	?	?	1	0
?	?	?	0	0	1
?	?	0	?	0	1
?	0	?	?	0	1
0	?	?	?	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
A4	1.0
B	1.0

Timing Parameters[1]

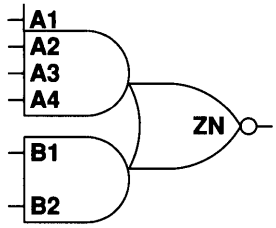
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.51	0.203	2.3	3.1	4.0	4.8	5.6
t_{PD}	A1(↓) to ZN(↑)	1.21	0.435	3.0	4.7	6.4	8.2	9.9
t_{PD}	A2(↑) to ZN(↓)	1.67	0.193	2.4	3.2	4.0	4.8	5.5
t_{PD}	A2(↓) to ZN(↑)	1.35	0.527	3.5	5.6	7.7	9.8	11.9
t_{PD}	A3(↑) to ZN(↓)	1.73	0.186	2.5	3.2	4.0	4.7	5.4
t_{PD}	A3(↓) to ZN(↑)	1.54	0.532	3.7	5.8	7.9	10.1	12.2
t_{PD}	A4(↑) to ZN(↓)	1.73	0.182	2.5	3.2	3.9	4.6	5.4
t_{PD}	A4(↓) to ZN(↑)	1.7	0.532	3.8	6.0	8.1	10.2	12.3
t_{PD}	B(↑) to ZN(↓)	1.63	0.143	2.2	2.8	3.3	3.9	4.5
t_{PD}	B(↓) to ZN(↑)	1.52	0.527	3.6	5.7	7.8	10.0	12.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

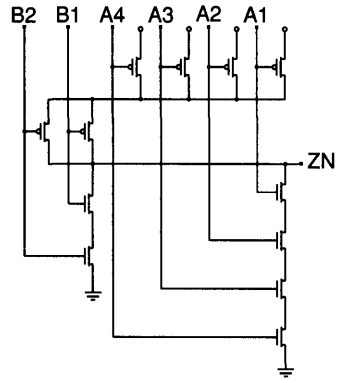
- 4-AND, 2-AND into 2-NOR

- Hard Macrocell
- 6 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A1	A2	A3	A4	B1	B2	ZN
1	1	1	1	?	?	0
?	?	?	?	1	1	0
?	?	?	0	?	0	1
?	?	0	?	?	0	1
?	0	?	?	?	0	1
0	?	?	?	?	0	1
?	?	?	0	0	?	1
?	?	0	?	0	?	1
?	0	?	?	0	?	1
0	?	?	?	0	?	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
A3	1.0
A4	1.0
B1	1.3
B2	1.3

Timing Parameters[1]

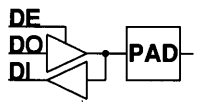
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.84	0.203	2.7	3.5	4.3	5.1	5.9
t_{PD}	A1(↓) to ZN(↑)	1.62	0.527	3.7	5.8	7.9	10.1	12.2
t_{PD}	A2(↑) to ZN(↓)	1.93	0.194	2.7	3.5	4.3	5.0	5.8
t_{PD}	A2(↓) to ZN(↑)	1.82	0.532	3.9	6.1	8.2	10.3	12.5
t_{PD}	A3(↑) to ZN(↓)	1.96	0.187	2.7	3.5	4.2	5.0	5.7
t_{PD}	A3(↓) to ZN(↑)	2.01	0.532	4.1	6.3	8.4	10.5	12.6
t_{PD}	A4(↑) to ZN(↓)	1.95	0.183	2.7	3.4	4.1	4.9	5.6
t_{PD}	A4(↓) to ZN(↑)	2.18	0.532	4.3	6.4	8.6	10.7	12.8
t_{PD}	B1(↑) to ZN(↓)	1.81	0.163	2.5	3.1	3.8	4.4	5.1
t_{PD}	B1(↓) to ZN(↑)	1.73	0.527	3.8	5.9	8.1	10.2	12.3
t_{PD}	B2(↑) to ZN(↓)	1.79	0.153	2.4	3.0	3.6	4.2	4.9
t_{PD}	B2(↓) to ZN(↑)	1.96	0.527	4.1	6.2	8.3	10.4	12.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

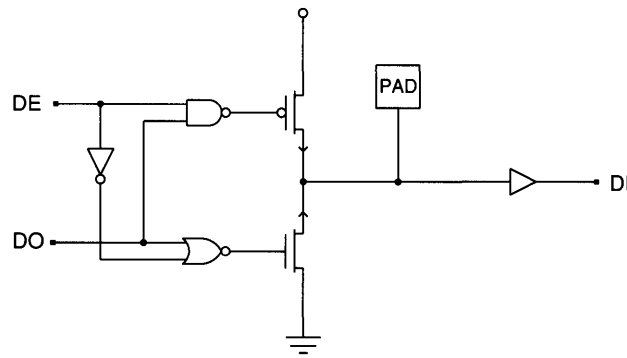
- Bidirectional pad buffer series. Buffers are available with 4, 8 or 12 ma DC current, with CMOS or TTL input levels and with optional output slew rate control for low-noise operation.
- External Buffer
- 0 TPTs
- 0 RLTs

Macro Name	Current	CMOS	TTL	Slew Control
BFB4C	*4ma*	*X*		
BFB4CR	*4ma*	*X*		*X*
BFB4T	*4ma*		*X*	
BFB4TR	*4ma*		*X*	*X*
BFB8C	*8ma*	*X*		
BFB8CR	*8ma*	*X*		*X*
BFB8T	*8ma*		*X*	
BFB8TR	*8ma*		*X*	*X*
BFB12C	*12ma*	*X*		
BFB12CR	*12ma*	*X*		*X*
BFB12T	*12ma*		*X*	
BFB12TR	*12ma*		*X*	*X*

Symbol



Schematic



Function Table

Inputs			Outputs	
DE	DO	PAD	PAD	DI
0	?	?	*Z*	PAD
1	?	?	DO	PAD

Pin Load

Pin	Std Load
DO	1.3
DE	1.6

BFB4C Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.72	0.0414	4.5	5.4	6.2	7.0	7.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.95	0.0764	3.5	5.0	6.5	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	1.71	0.0173	2.1	2.4	2.7	3.1	3.4
t_{PD}	DO(↑) to PAD(↑)	4.23	0.0728	5.7	7.1	8.6	10.1	11.5
t_{PD}	DO(↓) to PAD(↓)	4.16	0.0861	5.9	7.6	9.3	11.0	12.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.68	0.123	2.2	2.7	3.2	3.7	4.1

BFB8C Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.35	0.0247	3.8	4.3	4.8	5.3	5.8
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0387	4.7	5.4	6.2	7.0	7.8
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.06	0.0612	3.3	4.5	5.7	7.0	8.2
t_{PD}	DO(↑) to PAD(↑)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↓) to PAD(↓)	3.56	0.0484	4.5	5.5	6.5	7.4	8.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.68	0.123	2.2	2.7	3.2	3.7	4.1

BFB12C Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.18	0.0188	3.6	3.9	4.3	4.7	5.1
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0957	4.2	6.1	8.0	9.9	11.8
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0278	4.3	4.8	5.4	5.9	6.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.25	0.0758	3.8	5.3	6.8	8.3	9.8
t_{PD}	DO(↑) to PAD(↑)	3.71	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	3.27	0.0358	4.0	4.7	5.4	6.1	6.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.68	0.123	2.2	2.7	3.2	3.7	4.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

BFB4CR Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	4.23	0.0469	5.2	6.1	7.0	8.0	8.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.96	0.0766	3.5	5.0	6.6	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.21	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	1.71	0.0173	2.1	2.4	2.7	3.1	3.4
t_{PD}	DO(↑) to PAD(↑)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↓) to PAD(↓)	5.59	0.123	8.1	10.5	13.0	15.4	17.9
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.68	0.123	2.2	2.7	3.2	3.7	4.1

BFB8CR Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.71	0.0292	4.3	4.9	5.5	6.0	6.6
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.06	0.0612	3.3	4.5	5.7	7.0	8.2
t_{PD}	DO(↑) to PAD(↑)	3.88	0.0386	4.7	5.4	6.2	7.0	7.7
t_{PD}	DO(↓) to PAD(↓)	4.53	0.0722	6.0	7.4	8.9	10.3	11.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.68	0.123	2.2	2.7	3.2	3.7	4.1

BFB12CR Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.48	0.0226	3.9	4.4	4.8	5.3	5.7
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0958	4.2	6.1	8.0	9.9	11.9
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.25	0.0758	3.8	5.3	6.8	8.3	9.8
t_{PD}	DO(↑) to PAD(↑)	3.7	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	4.06	0.0538	5.1	6.2	7.3	8.4	9.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.68	0.123	2.2	2.7	3.2	3.7	4.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

BFB4T Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.72	0.0414	4.5	5.4	6.2	7.0	7.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.95	0.0764	3.5	5.0	6.5	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	1.71	0.0173	2.1	2.4	2.7	3.1	3.4
t_{PD}	DO(↑) to PAD(↑)	4.23	0.0728	5.7	7.1	8.6	10.1	11.5
t_{PD}	DO(↓) to PAD(↓)	4.16	0.0861	5.9	7.6	9.3	11.0	12.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.64	0.101	2.0	2.4	2.8	3.2	3.7
t_{PD}	PAD(↓) to DI(↓)	2.02	0.122	2.5	3.0	3.5	4.0	4.5

BFB8T Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.35	0.0247	3.8	4.3	4.8	5.3	5.8
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0387	4.7	5.4	6.2	7.0	7.8
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.06	0.0612	3.3	4.5	5.7	7.0	8.2
t_{PD}	DO(↑) to PAD(↑)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↓) to PAD(↓)	3.56	0.0484	4.5	5.5	6.5	7.4	8.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.64	0.101	2.0	2.4	2.8	3.2	3.7
t_{PD}	PAD(↓) to DI(↓)	2.02	0.122	2.5	3.0	3.5	4.0	4.5

BFB12T Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.18	0.0188	3.6	3.9	4.3	4.7	5.1
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0957	4.2	6.1	8.0	9.9	11.8
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0278	4.3	4.8	5.4	5.9	6.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.25	0.0758	3.8	5.3	6.8	8.3	9.8
t_{PD}	DO(↑) to PAD(↑)	3.71	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	3.27	0.0358	4.0	4.7	5.4	6.1	6.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.64	0.101	2.0	2.4	2.8	3.2	3.7
t_{PD}	PAD(↓) to DI(↓)	2.02	0.122	2.5	3.0	3.5	4.0	4.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

BFB4TR Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	4.23	0.0469	5.2	6.1	7.0	8.0	8.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.96	0.0766	3.5	5.0	6.6	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.21	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	1.71	0.0173	2.1	2.4	2.7	3.1	3.4
t_{PD}	DO(↑) to PAD(↑)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↓) to PAD(↓)	5.59	0.123	8.1	10.5	13.0	15.4	17.9
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.64	0.101	2.0	2.4	2.8	3.2	3.7
t_{PD}	PAD(↓) to DI(↓)	2.02	0.122	2.5	3.0	3.5	4.0	4.5

BFB8TR Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.71	0.0292	4.3	4.9	5.5	6.0	6.6
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.06	0.0612	3.3	4.5	5.7	7.0	8.2
t_{PD}	DO(↑) to PAD(↑)	3.88	0.0386	4.7	5.4	6.2	7.0	7.7
t_{PD}	DO(↓) to PAD(↓)	4.53	0.0722	6.0	7.4	8.9	10.3	11.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.64	0.101	2.0	2.4	2.8	3.2	3.7
t_{PD}	PAD(↓) to DI(↓)	2.02	0.122	2.5	3.0	3.5	4.0	4.5

BFB12TR Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.48	0.0226	3.9	4.4	4.8	5.3	5.7
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0958	4.2	6.1	8.0	9.9	11.9
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.25	0.0758	3.8	5.3	6.8	8.3	9.8
t_{PD}	DO(↑) to PAD(↑)	3.7	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	4.06	0.0538	5.1	6.2	7.3	8.4	9.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.64	0.101	2.0	2.4	2.8	3.2	3.7
t_{PD}	PAD(↓) to DI(↓)	2.02	0.122	2.5	3.0	3.5	4.0	4.5

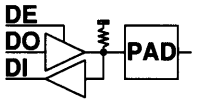
1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

- Bidirectional pad buffer series with weak pull-up. Buffers are available with 4, 8 or 12 ma DC current, with CMOS or TTL input levels and with optional output slew rate control for low-noise operation. The passive pull-up ensures that the pin is high when it is not driven.

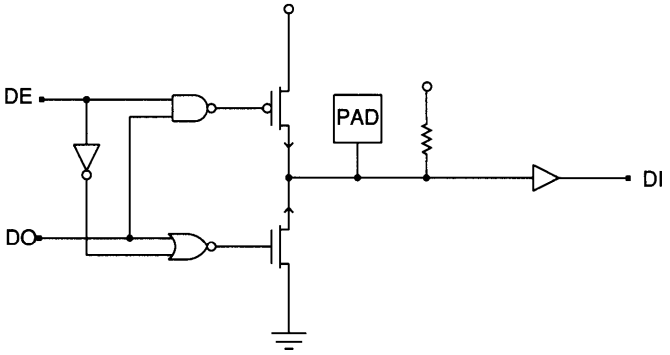
- External Buffer
- 0 TPTs
- 0 RLTs

Macro Name	Current	CMOS	TTL	Slew Control
BFB4CU	*4ma*	*X*		
BFB4CRU	*4ma*	*X*		*X*
BFB4TU	*4ma*		*X*	
BFB4TRU	*4ma*		*X*	*X*
BFB8CU	*8ma*	*X*		
BFB8CRU	*8ma*	*X*		*X*
BFB8TU	*8ma*		*X*	
BFB8TRU	*8ma*		*X*	*X*
BFB12CU	*12ma*	*X*		
BFB12CRU	*12ma*	*X*		*X*
BFB12TU	*12ma*		*X*	
BFB12TRU	*12ma*		*X*	*X*

Symbol



Schematic



Function Table

Inputs			Outputs	
DE	DO	PAD	PAD	DI
0	?	?	1r	PAD
1	?	?	DO	PAD

Pin Load

Pin	Std Load
DO	1.3
DE	1.6

BFB4CU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.72	0.0414	4.5	5.4	6.2	7.0	7.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.95	0.0764	3.5	5.0	6.5	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↑) to PAD(↑)	4.23	0.0728	5.7	7.1	8.6	10.1	11.5
t_{PD}	DO(↓) to PAD(↓)	4.16	0.0861	5.9	7.6	9.3	11.0	12.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.7	0.123	2.2	2.7	3.2	3.7	4.2

BFB8CU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.35	0.0247	3.8	4.3	4.8	5.3	5.8
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0387	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↑) to PAD(↑)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↓) to PAD(↓)	3.56	0.0484	4.5	5.5	6.5	7.4	8.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.7	0.123	2.2	2.7	3.2	3.7	4.2

BFB12CU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.18	0.0188	3.6	3.9	4.3	4.7	5.1
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0957	4.2	6.1	8.0	9.9	11.8
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0278	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↑) to PAD(↑)	3.71	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	3.27	0.0358	4.0	4.7	5.4	6.1	6.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.7	0.123	2.2	2.7	3.2	3.7	4.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

BFB4CRU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	4.23	0.0469	5.2	6.1	7.0	8.0	8.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.96	0.0766	3.5	5.0	6.6	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.21	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↑) to PAD(↑)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↓) to PAD(↓)	5.59	0.123	8.1	10.5	13.0	15.4	17.9
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.7	0.123	2.2	2.7	3.2	3.7	4.2

BFB8CRU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.71	0.0292	4.3	4.9	5.5	6.0	6.6
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↑) to PAD(↑)	3.88	0.0386	4.7	5.4	6.2	7.0	7.7
t_{PD}	DO(↓) to PAD(↓)	4.53	0.0722	6.0	7.4	8.9	10.3	11.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.7	0.123	2.2	2.7	3.2	3.7	4.2

BFB12CRU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.48	0.0226	3.9	4.4	4.8	5.3	5.7
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0958	4.2	6.1	8.0	9.9	11.9
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↑) to PAD(↑)	3.7	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	4.06	0.0538	5.1	6.2	7.3	8.4	9.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.7	0.123	2.2	2.7	3.2	3.7	4.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

BFB4TU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.72	0.0414	4.5	5.4	6.2	7.0	7.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.95	0.0764	3.5	5.0	6.5	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↑) to PAD(↑)	4.23	0.0728	5.7	7.1	8.6	10.1	11.5
t_{PD}	DO(↓) to PAD(↓)	4.16	0.0861	5.9	7.6	9.3	11.0	12.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.62	0.101	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	2.06	0.122	2.5	3.0	3.5	4.0	4.5

BFB8TU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.35	0.0247	3.8	4.3	4.8	5.3	5.8
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0387	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↑) to PAD(↑)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↓) to PAD(↓)	3.56	0.0484	4.5	5.5	6.5	7.4	8.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.62	0.101	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	2.06	0.122	2.5	3.0	3.5	4.0	4.5

BFB12TU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.18	0.0188	3.6	3.9	4.3	4.7	5.1
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0957	4.2	6.1	8.0	9.9	11.8
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0278	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↑) to PAD(↑)	3.71	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	3.27	0.0358	4.0	4.7	5.4	6.1	6.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.62	0.101	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	2.06	0.122	2.5	3.0	3.5	4.0	4.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

BFB4TRU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	4.23	0.0469	5.2	6.1	7.0	8.0	8.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.96	0.0766	3.5	5.0	6.6	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.21	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↑) to PAD(↑)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↓) to PAD(↓)	5.59	0.123	8.1	10.5	13.0	15.4	17.9
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.62	0.101	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	2.06	0.122	2.5	3.0	3.5	4.0	4.5

BFB8TRU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.71	0.0292	4.3	4.9	5.5	6.0	6.6
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↑) to PAD(↑)	3.88	0.0386	4.7	5.4	6.2	7.0	7.7
t_{PD}	DO(↓) to PAD(↓)	4.53	0.0722	6.0	7.4	8.9	10.3	11.8
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.62	0.101	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	2.06	0.122	2.5	3.0	3.5	4.0	4.5

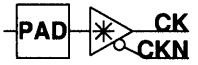
BFB12TRU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.48	0.0226	3.9	4.4	4.8	5.3	5.7
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0958	4.2	6.1	8.0	9.9	11.9
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↑) to PAD(↑)	3.7	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	4.06	0.0538	5.1	6.2	7.3	8.4	9.4
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.62	0.101	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	2.06	0.122	2.5	3.0	3.5	4.0	4.5

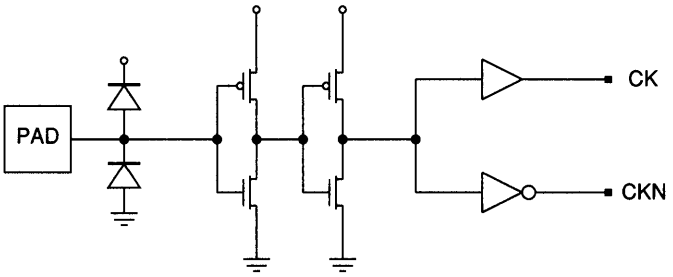
1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

- Clock grid driver with PAD input and inverting and non-inverting outputs. There may be up to 4 clock grid drivers (BFCKGx series and CKGx series) in a design. Placement is restricted to an external clock buffer site—CLKA, CLKB, CLKC or CLKD.
- External Clock Buffer
- 0 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Outputs	
PAD	CK	CKN
?	PAD	$\overline{PAD}$

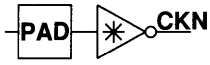
Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				50	100	150	200	250
t_{PD}	PAD(↑) to CK(↑)	6.69	0.0016	6.8	6.9	6.9	7.0	7.1
t_{PD}	PAD(↓) to CK(↓)	5.72	0.00155	5.8	5.9	6.0	6.0	6.1
t_{PD}	PAD(↑) to CKN(↓)	5.7	0.00155	5.8	5.9	5.9	6.0	6.1
t_{PD}	PAD(↓) to CKN(↑)	6.66	0.0016	6.7	6.8	6.9	7.0	7.1

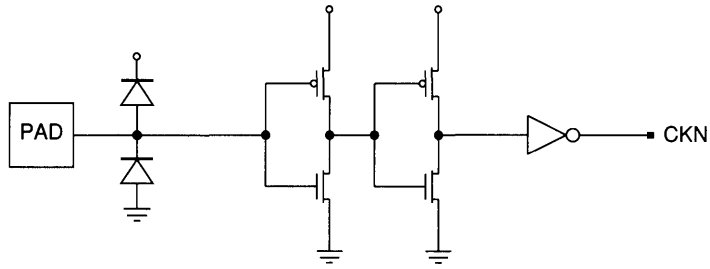
1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin loads only to get total load. Wire load is zero.

- Clock grid driver with PAD input and inverting output. There may be up to 4 clock grid drivers (BFCKGx series and CKGx series) in a design. Placement is restricted to an external clock buffer site—CLKA, CLKB, CLKC or CLKD.
- External Clock Buffer
- 0 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
PAD	CKN
?	$\overline{\text{PAD}}$

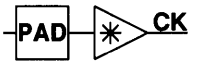
Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				50	100	150	200	250
t_{PD}	PAD(↑) to CKN(↓)	5.7	0.00155	5.8	5.9	5.9	6.0	6.1
t_{PD}	PAD(↓) to CKN(↑)	6.66	0.0016	6.7	6.8	6.9	7.0	7.1

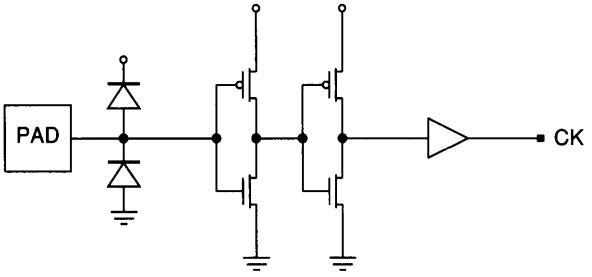
1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin loads only to get total load. Wire load is zero.

- Clock grid driver with PAD input and non-inverting output. There may be up to 4 clock grid drivers (BFCKGx series and CKGx series) in a design. Placement is restricted to an external clock buffer site—CLKA, CLKB, CLKC or CLKD.
- External Clock Buffer
- 0 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
PAD	CK
?	PAD

Timing Parameters[1]

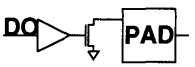
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				50	100	150	200	250
t_{PD}	PAD(↑) to CK(↑)	6.69	0.0016	6.8	6.9	6.9	7.0	7.1
t_{PD}	PAD(↓) to CK(↓)	5.72	0.00155	5.8	5.9	6.0	6.0	6.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin loads only to get total load. Wire load is zero.

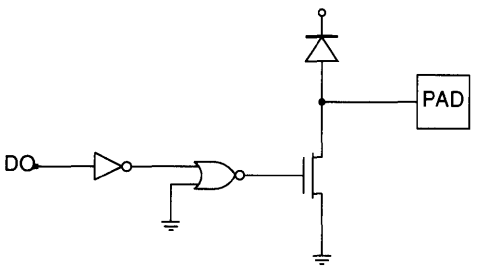
- Open-drain pad output series. Buffers are available with 4, 8 or 12 ma DC sink current and with optional output slew rate control for low noise operation. Buffer is inverting.
- External Buffer
- 0 TPTs
- 0 RLTs

Macro Name	Current	Slew Control
BFD4	*4ma*	
BFD4R	*4ma*	*X*
BFD8	*8ma*	
BFD8R	*8ma*	*X*
BFD12	*12ma*	
BFD12R	*12ma*	*X*

Symbol



Schematic



Function Table

Input	Output
DO	PAD
1	0
0	*Z*

Pin Load

Pin	Std Load
DO	1.6

BFD4 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↓)	3.72	0.0414	4.5	5.4	6.2	7.0	7.9
t_{PD}	DO(↓) to PAD(Z)	1.95	0.0764	3.5	5.0	6.5	8.1	9.6

BFD4R Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↓)	4.23	0.0469	5.2	6.1	7.0	8.0	8.9
t_{PD}	DO(↓) to PAD(Z)	1.96	0.0766	3.5	5.0	6.6	8.1	9.6

BFD8 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↓)	3.35	0.0247	3.8	4.3	4.8	5.3	5.8
t_{PD}	DO(↓) to PAD(Z)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2

BFD8R Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↓)	3.71	0.0292	4.3	4.9	5.5	6.0	6.6
t_{PD}	DO(↓) to PAD(Z)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2

BFD12 Timing Parameter[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↓)	3.18	0.0188	3.6	3.9	4.3	4.7	5.1
t_{PD}	DO(↓) to PAD(Z)	2.28	0.0957	4.2	6.1	8.0	9.9	11.8

BFD12R Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↓)	3.48	0.0226	3.9	4.4	4.8	5.3	5.7
t_{PD}	DO(↓) to PAD(Z)	2.28	0.0958	4.2	6.1	8.0	9.9	11.9

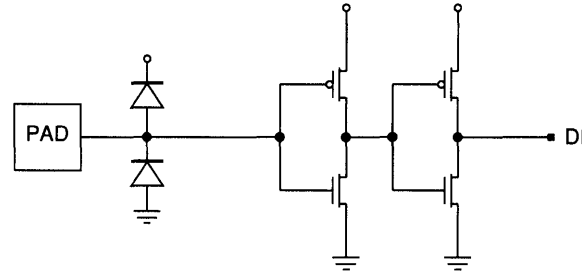
1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.

- Pad input buffer series. Buffers are available with TTL or CMOS input levels.
- External Buffer
- 0 TPTs
- 0 RLTs

Macro Name	CMOS	TTL
BFIC	*X*	
BFIT		*X*

Symbol

Schematic



Function Table

Input	Output
PAD	DI
?	PAD

BFIC Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.68	0.123	2.2	2.7	3.2	3.7	4.1

BFIT Timing Parameters[1]

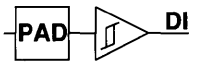
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.64	0.101	2.0	2.4	2.8	3.2	3.7
t_{PD}	PAD(↓) to DI(↓)	2.02	0.122	2.5	3.0	3.5	4.0	4.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

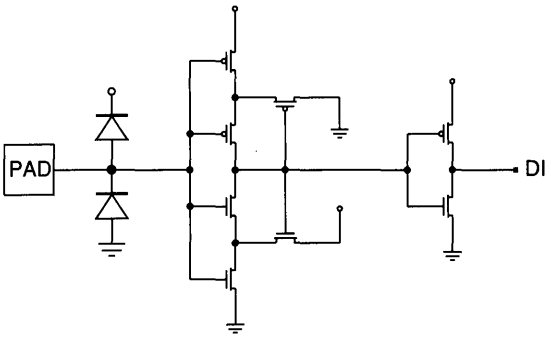
- Schmitt trigger input buffer series. Buffer is available with either CMOS or TTL input levels. There may be up to 7 Schmitt Trigger Input Buffers in a design. Placement is restricted to a clock buffer site, CLKA, CLKB, CLKC, CLKD, or a JTAG TAP input buffer site, TCK, TDI or TMS.
- External Buffer
- 1 Gate Equivalents
- 0 TPTs
- 0 RLTs

Macro Name	CMOS	TTL
BFICS	*X*	
BFITS		*X*

Symbol



Schematic



Function Table

Input	Output
PAD	DI
?	PAD

BFICS Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	3.24	0.1	3.6	4.0	4.4	4.8	5.2
t_{PD}	PAD(↓) to DI(↓)	3.1	0.127	3.6	4.1	4.6	5.1	5.6

BFITS Timing Parameters[1]

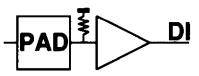
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	2.95	0.0996	3.3	3.7	4.1	4.5	4.9
t_{PD}	PAD(↓) to DI(↓)	3.36	0.13	3.9	4.4	4.9	5.4	6.0

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

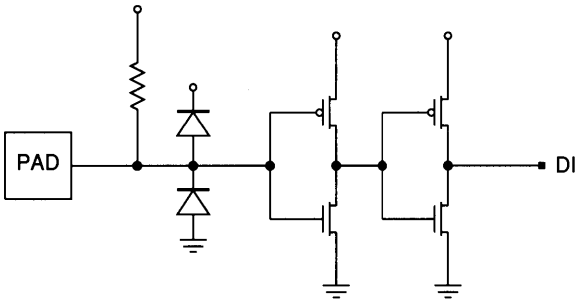
- Pad input buffers with weak pull-up. Buffer is available with either CMOS or TTL input levels. Pull-up ensures that PAD is high when it is not driven.
- External Buffer
- 0 TPTs
- 0 RLTs

Macro Name	CMOS	TTL
BFICU	*X*	
BFITU		*X*

Symbol



Schematic



Function Table

Input	Output
PAD	DI
?	PAD

BFICU Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.65	0.0991	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	1.7	0.123	2.2	2.7	3.2	3.7	4.2

BFITU Timing Parameters[1]

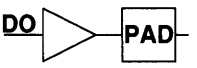
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	PAD(↑) to DI(↑)	1.62	0.101	2.0	2.4	2.8	3.2	3.6
t_{PD}	PAD(↓) to DI(↓)	2.06	0.122	2.5	3.0	3.5	4.0	4.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

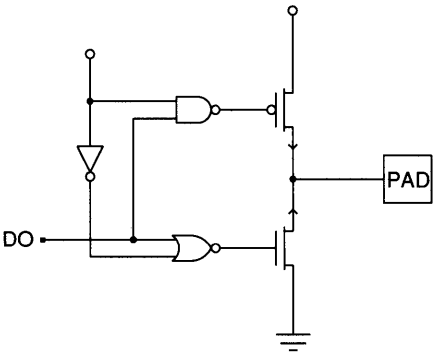
- Pad output buffer series. Buffers are available with 4, 8 or 12 ma DC current and with optional output slew rate control for low-noise operation.
- External Buffer
- 0 TPTs
- 0 RLTs

Macro Name	Current	Slew Control
BFO4	*4ma*	
BFO4R	*4ma*	*X*
BFO8	*8ma*	
BFO8R	*8ma*	*X*
BFO12	*12ma*	
BFO12R	*12ma*	*X*

Symbol



Schematic



Function Table

Input	Output
DO	PAD
?	DO

Pin Load

Pin	Std Load
DO	1.3

BFO4 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↑)	4.23	0.0728	5.7	7.1	8.6	10.1	11.5
t_{PD}	DO(↓) to PAD(↓)	4.16	0.0861	5.9	7.6	9.3	11.0	12.8

BFO4R Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↑)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↓) to PAD(↓)	5.59	0.123	8.1	10.5	13.0	15.4	17.9

BFO8 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↑)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↓) to PAD(↓)	3.56	0.0484	4.5	5.5	6.5	7.4	8.4

BFO8R Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↑)	3.88	0.0386	4.7	5.4	6.2	7.0	7.7
t_{PD}	DO(↓) to PAD(↓)	4.53	0.0722	6.0	7.4	8.9	10.3	11.8

BFO12 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↑)	3.71	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	3.27	0.0358	4.0	4.7	5.4	6.1	6.8

BFO12R Timing Parameters[1]

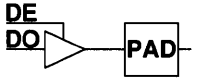
Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DO(↑) to PAD(↑)	3.7	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	4.06	0.0538	5.1	6.2	7.3	8.4	9.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.

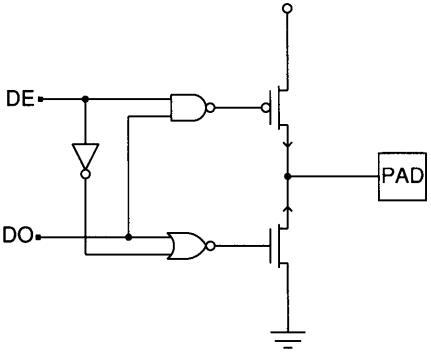
- Three-state pad output buffer series. Buffers are available with 4, 8 or 12 ma DC sink current and with optional output slew rate control for low noise operation.
- External Buffer
- 0 TPTs
- 0 RLTs

Macro Name	Current	Slew Control
BFT4	*4ma*	
BFT4R	*4ma*	*X*
BFT8	*8ma*	
BFT8R	*8ma*	*X*
BFT12	*12ma*	
BFT12R	*12ma*	*X*

Symbol



Schematic



Function Table

Inputs		Output
DE	DO	PAD
0	?	*Z*
1	?	DO

Pin Load

Pin	Std Load
DO	1.3
DE	1.6

BFT4 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.72	0.0414	4.5	5.4	6.2	7.0	7.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.95	0.0764	3.5	5.0	6.5	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	1.71	0.0173	2.1	2.4	2.7	3.1	3.4
t_{PD}	DO(↑) to PAD(↑)	4.23	0.0728	5.7	7.1	8.6	10.1	11.5
t_{PD}	DO(↓) to PAD(↓)	4.16	0.0861	5.9	7.6	9.3	11.0	12.8

BFT8 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.35	0.0247	3.8	4.3	4.8	5.3	5.8
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0387	4.7	5.4	6.2	7.0	7.8
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.06	0.0612	3.3	4.5	5.7	7.0	8.2
t_{PD}	DO(↑) to PAD(↑)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DO(↓) to PAD(↓)	3.56	0.0484	4.5	5.5	6.5	7.4	8.4

BFT12 Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.18	0.0188	3.6	3.9	4.3	4.7	5.1
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0957	4.2	6.1	8.0	9.9	11.8
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0278	4.3	4.8	5.4	5.9	6.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.25	0.0758	3.8	5.3	6.8	8.3	9.8
t_{PD}	DO(↑) to PAD(↑)	3.71	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	3.27	0.0358	4.0	4.7	5.4	6.1	6.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.

BFT4R Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	4.23	0.0469	5.2	6.1	7.0	8.0	8.9
t_{PD}	DE(↓) to PAD(Z) with DO(0)	1.96	0.0766	3.5	5.0	6.6	8.1	9.6
t_{PD}	DE(↑) to PAD(↑) with DO(1)	4.21	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	1.71	0.0173	2.1	2.4	2.7	3.1	3.4
t_{PD}	DO(↑) to PAD(↑)	4.22	0.0728	5.7	7.1	8.6	10.0	11.5
t_{PD}	DO(↓) to PAD(↓)	5.59	0.123	8.1	10.5	13.0	15.4	17.9

BFT8R Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.71	0.0292	4.3	4.9	5.5	6.0	6.6
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.15	0.0908	4.0	5.8	7.6	9.4	11.2
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.89	0.0386	4.7	5.4	6.2	7.0	7.8
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.06	0.0612	3.3	4.5	5.7	7.0	8.2
t_{PD}	DO(↑) to PAD(↑)	3.88	0.0386	4.7	5.4	6.2	7.0	7.7
t_{PD}	DO(↓) to PAD(↓)	4.53	0.0722	6.0	7.4	8.9	10.3	11.8

BFT12R Timing Parameters[1]

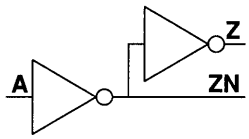
Type	Description	Intrinsic (ns)	Drive (ns/pF)	20 pF	40 pF	60 pF	80 pF	100 pF
t_{PD}	DE(↑) to PAD(↓) with DO(0)	3.48	0.0226	3.9	4.4	4.8	5.3	5.7
t_{PD}	DE(↓) to PAD(Z) with DO(0)	2.28	0.0958	4.2	6.1	8.0	9.9	11.9
t_{PD}	DE(↑) to PAD(↑) with DO(1)	3.72	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DE(↓) to PAD(Z) with DO(1)	2.25	0.0758	3.8	5.3	6.8	8.3	9.8
t_{PD}	DO(↑) to PAD(↑)	3.7	0.0277	4.3	4.8	5.4	5.9	6.5
t_{PD}	DO(↓) to PAD(↓)	4.06	0.0538	5.1	6.2	7.3	8.4	9.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.

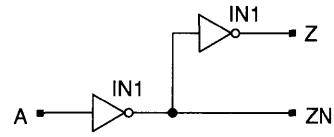
- Buffer, Inverting and Non-inverting Outputs

- Hard Macrocell
- 1 Gate Equivalents
- 3 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Outputs	
A	Z	ZN
?	A	$\overline{A}$

Pin Load

Pin	Std Load
A	1.0

Timing Parameters[1]

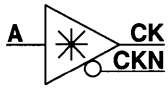
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.22	0.146	1.8	2.4	3.0	3.6	4.1
t_{PD}	ZN(↓) to Z(↑)	0.508	0.283	1.6	2.8	3.9	5.0	6.2
t_{PD}	A(↓) to ZN(↑)	1.06	0.297	2.2	3.4	4.6	5.8	7.0
t_{PD}	ZN(↑) to Z(↓)	1.04	0.146	1.6	2.2	2.8	3.4	4.0
t_{PD}	A(↓) to ZN(↑)	1.06	0.297	2.2	3.4	4.6	5.8	7.0
t_{PD}	A(↑) to ZN(↓)	1.22	0.146	1.8	2.4	3.0	3.6	4.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

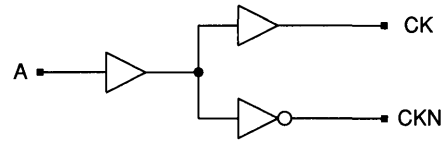
- Clock grid driver with internal input and inverting and non-inverting outputs. There may be up to 4 clock grid drivers (BFCKGx series and CKGx series) in a design. Placement is restricted to an internal clock buffer site—CLKT1, CLKT2, CLKT3 or CLKT4.

- Internal Clock Driver
- 2 Gate Equivalents
- 0 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Outputs	
A	CK	CKN
?	A	$\overline{A}$

Pin Load

Pin	Std Load
A	1.0

Timing Parameters[1]

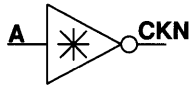
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				50	100	150	200	250
t_{PD}	A(↑) to CK(↑)	7.16	0.0016	7.2	7.3	7.4	7.5	7.6
t_{PD}	A(↓) to CK(↓)	6.51	0.00155	6.6	6.7	6.7	6.8	6.9
t_{PD}	A(↑) to CKN(↓)	6.63	0.00154	6.7	6.8	6.9	6.9	7.0
t_{PD}	A(↓) to CKN(↑)	7.54	0.0016	7.6	7.7	7.8	7.9	7.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin loads only to get total load. Wire load is zero.

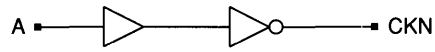
- Clock grid driver with internal input and inverting output. There may be up to 4 clock grid drivers (BFCKGx series and CKGx series) in a design. Placement is restricted to an internal clock buffer site—CLKT1, CLKT2, CLKT3 or CLKT4.

- Internal Clock Driver
- 2 Gate Equivalents
- 0 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	CKN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	1.0

Timing Parameters[1]

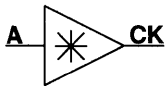
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				50	100	150	200	250
t_{PD}	A(↑) to CKN(↓)	6.63	0.00154	6.7	6.8	6.9	6.9	7.0
t_{PD}	A(↓) to CKN(↑)	7.54	0.0016	7.6	7.7	7.8	7.9	7.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin loads only to get total load. Wire load is zero.

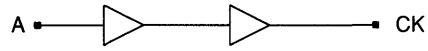
- Clock grid driver with internal input and non-inverting output. There may be up to 4 clock grid drivers (BFCKGx series and CKGx series) in a design. Placement is restricted to an internal clock buffer site—CLKT1, CLKT2, CLKT3 or CLKT4.

- Internal Clock Driver
- 2 Gate Equivalents
- 0 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	CK
?	A

Pin Load

Pin	Std Load
A	1.0

Timing Parameters[1]

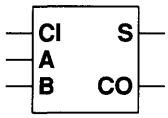
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				50	100	150	200	250
t_{PD}	A(↑) to CK(↑)	7.16	0.0016	7.2	7.3	7.4	7.5	7.6
t_{PD}	A(↓) to CK(↓)	6.51	0.00155	6.6	6.7	6.7	6.8	6.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin loads only to get total load. Wire load is zero.

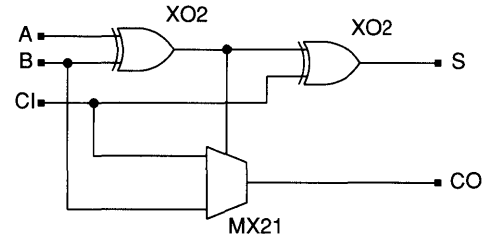
- 1-Bit Full Adder

- Soft Macrocell
- 10 Gate Equivalents
- 2 TPTs
- 3 RLTs

Symbol



Schematic



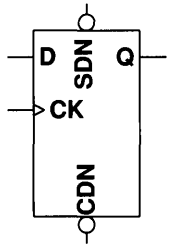
Function Table

Inputs			Outputs	
A	B	CI	S	CO
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

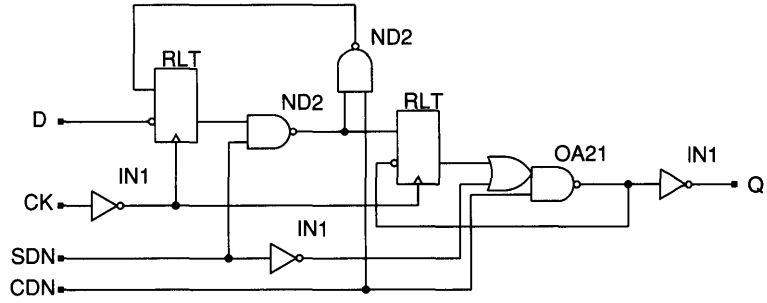
- Positive edge triggered D Flip-Flop with pre-set, clear and single clock input.

- Hard Macrocell
- 7 Gate Equivalents
- 15 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs				Output
CDN	SDN	CK	D	Q
0	?	?	?	0
1	0	?	?	1
1	1	↑	?	D
1	1	1	?	Q
1	1	↓	?	Q
1	1	0	?	Q

Pin Load

Pin	Std Load
CK	1.0
D	0.4
CDN	2.0
SDN	2.0

Timing Parameters[1]

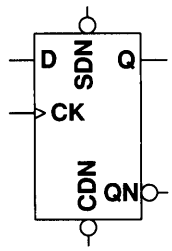
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓) with D(0)	5.67	0.148	6.3	6.9	7.5	8.0	8.6
t_{PD}	CK(↑) to Q(↑) with D(1)	5.09	0.2	5.9	6.7	7.5	8.3	9.1
t_{PD}	CDN(↓) to Q(↓)	1.82	0.191	2.6	3.3	4.1	4.9	5.6
t_{PD}	CDN(↑) to Q(↑)	2.55	0.206	3.4	4.2	5.0	5.9	6.7
t_{PD}	SDN(↓) to Q(↑)	3.31	0.295	4.5	5.7	6.8	8.0	9.2
t_S	CDN(1) recovery CK(↑)	0.12	0.000	0.1	0.1	0.1	0.1	0.1
t_H	CDN(0) hold CK(↑)	4.04	0.000	4.0	4.0	4.0	4.0	4.0
t_W	pulse width CDN(0)	3.71	0.000	3.7	3.7	3.7	3.7	3.7
t_S	SDN(1) recovery CK(↑)	0.958	0.000	1.0	1.0	1.0	1.0	1.0
t_H	SDN(0) hold CK(↑)	3.07	0.000	3.1	3.1	3.1	3.1	3.1
t_W	pulse width SDN(0)	3.8	0.000	3.8	3.8	3.8	3.8	3.8
t_S	D(0) setup CK(↑)	2.93	0.000	2.9	2.9	2.9	2.9	2.9
t_S	D(1) setup CK(↑)	3.41	0.000	3.4	3.4	3.4	3.4	3.4
t_H	D(0) hold CK(↑)	0.965	0.000	1.0	1.0	1.0	1.0	1.0
t_H	D(1) hold CK(↑)	0.889	0.000	0.9	0.9	0.9	0.9	0.9
t_W	pulse width CK(1)	5	0.000	5.0	5.0	5.0	5.0	5.0
t_W	pulse width CK(0)	4.8	0.000	4.8	4.8	4.8	4.8	4.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

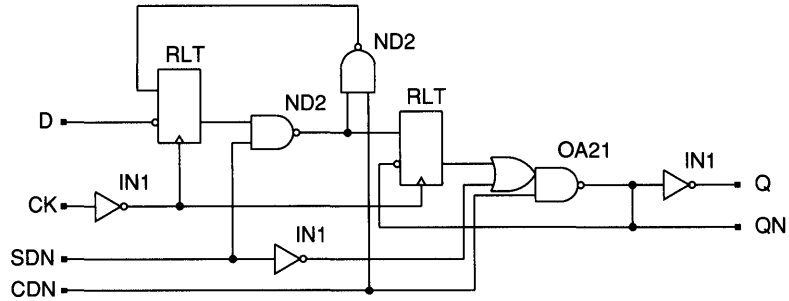
- Positive edge triggered D Flip-Flop with pre-set, clear and single clock input. Output QN is the complement of Q.

- Hard Macrocell
- 9 Gate Equivalents
- 15 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs				Outputs	
CDN	SDN	CK	D	Q	QN
0	?	?	?	0	$\overline{Q}$
1	0	?	?	1	$\overline{Q}$
1	1	↑	?	D	$\overline{Q}$
1	1	1	?	Q	$\overline{Q}$
1	1	↓	?	Q	$\overline{Q}$
1	1	0	?	Q	$\overline{Q}$

Pin Load

Pin	Std Load
CK	1.0
D	0.4
CDN	2.0
SDN	2.0

Timing Parameters[1]

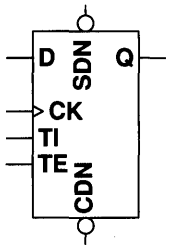
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to QN(↑) with D(0)	4.88	0.307	6.1	7.3	8.6	9.8	11.0
t_{PD}	CK(↑) to QN(↓) with D(1)	4.35	0.154	5.0	5.6	6.2	6.8	7.4
t_{PD}	CK(↑) to QN(↑) with D(0)	4.88	0.307	6.1	7.3	8.6	9.8	11.0
t_{PD}	QN(↑) to Q(↓) with D(0)	1.42	0.16	2.1	2.7	3.3	4.0	4.6
t_{PD}	CK(↑) to QN(↓) with D(1)	4.35	0.154	5.0	5.6	6.2	6.8	7.4
t_{PD}	QN(↓) to Q(↑) with D(1)	0.855	0.293	2.0	3.2	4.4	5.5	6.7
t_{PD}	CDN(↓) to QN(↑)	1.31	0.296	2.5	3.7	4.9	6.0	7.2
t_{PD}	CDN(↑) to QN(↓)	1.7	0.225	2.6	3.5	4.4	5.3	6.2
t_{PD}	SDN(↓) to QN(↓)	2.24	0.276	3.3	4.4	5.5	6.7	7.8
t_{PD}	CDN(↓) to QN(↑)	1.31	0.296	2.5	3.7	4.9	6.0	7.2
t_{PD}	QN(↑) to Q(↓) with D(0)	1.42	0.16	2.1	2.7	3.3	4.0	4.6
t_{PD}	CDN(↑) to QN(↓)	1.7	0.225	2.6	3.5	4.4	5.3	6.2
t_{PD}	QN(↓) to Q(↑) with D(1)	0.855	0.293	2.0	3.2	4.4	5.5	6.7
t_{PD}	SDN(↓) to QN(↓)	2.24	0.276	3.3	4.4	5.5	6.7	7.8
t_{PD}	QN(↓) to Q(↑) with D(1)	0.855	0.293	2.0	3.2	4.4	5.5	6.7
t_S	CDN(1) recovery CK(↑)	0.0588	0.000	0.1	0.1	0.1	0.1	0.1
t_H	CDN(0) hold CK(↑)	4.03	0.000	4.0	4.0	4.0	4.0	4.0
t_W	pulse width CDN(0) [use load on QN]	5.61	0.209	6.4	7.3	8.1	9.0	9.8
t_S	SDN(1) recovery CK(↑)	0.961	0.000	1.0	1.0	1.0	1.0	1.0
t_H	SDN(0) hold CK(↑)	3.07	0.000	3.1	3.1	3.1	3.1	3.1
t_W	pulse width SDN(0) [use load on QN]	5.14	0.276	6.2	7.3	8.4	9.6	10.7
t_S	D(0) setup CK(↑)	2.93	0.000	2.9	2.9	2.9	2.9	2.9
t_S	D(1) setup CK(↑)	3.35	0.000	3.4	3.4	3.4	3.4	3.4
t_H	D(0) hold CK(↑)	0.963	0.000	1.0	1.0	1.0	1.0	1.0
t_H	D(1) hold CK(↑)	0.95	0.000	0.9	0.9	0.9	0.9	0.9
t_W	pulse width CK(1) [use load on QN]	4.88	0.307	6.1	7.3	8.6	9.8	11.0
t_W	pulse width CK(0)	4.8	0.000	4.8	4.8	4.8	4.8	4.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

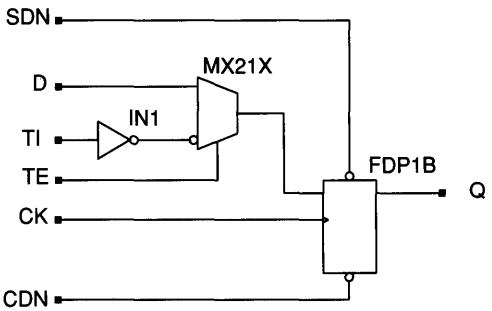
- Positive edge triggered D Flip-Flop with pre-set, clear and single clock input. Multiplexer on data input allows selection of D for normal operation or TI for scan testing.

- Soft Macrocell
- 12 Gate Equivalents
- 17 TPTs
- 3 RLTs

Symbol



Schematic



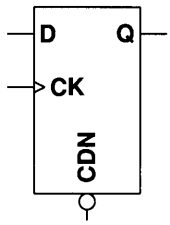
Function Table

Inputs						Output
CDN	SDN	CK	TE	TI	D	Q
0	?	?	?	?	?	0
1	0	?	?	?	?	1
1	1	↑	0	?	?	D
1	1	↑	1	?	?	TI
1	1	1	?	?	?	Q
1	1	↓	?	?	?	Q
1	1	0	?	?	?	Q

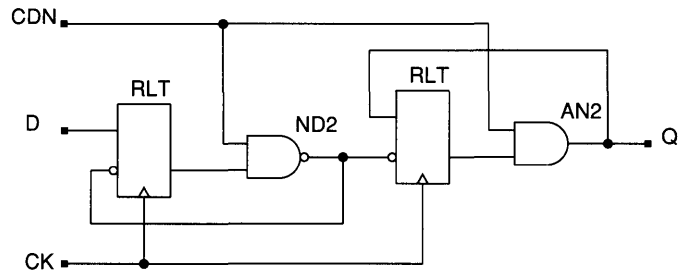
- Positive edge triggered D Flip-Flop with clear and single clock input.

- Hard Macrocell
- 9 Gate Equivalents
- 7 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs			Output
CDN	CK	D	Q
0	?	?	0
1	↑	?	D
1	1	?	Q
1	↓	?	Q
1	0	?	Q

Pin Load

Pin	Std Load
CK	1.1
D	0.5
CDN	2.0

Timing Parameters[1]

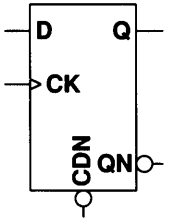
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓) with D(0)	4.13	0.14	4.7	5.3	5.8	6.4	6.9
t_{PD}	CK(↑) to Q(↑) with D(1)	3.57	0.206	4.4	5.2	6.0	6.9	7.7
t_{PD}	CDN(↓) to Q(↓)	1.76	0.189	2.5	3.3	4.0	4.8	5.5
t_S	CDN(1) recovery CK(↑)	1.2	0.000	1.2	1.2	1.2	1.2	1.2
t_H	CDN(0) hold CK(↑)	2.72	0.000	2.7	2.7	2.7	2.7	2.7
t_W	pulse width CDN(0) [use load on Q]	4.94	0.189	5.7	6.5	7.2	8.0	8.7
t_S	D(0) setup CK(↑)	3.17	0.000	3.2	3.2	3.2	3.2	3.2
t_S	D(1) setup CK(↑)	3.16	0.000	3.2	3.2	3.2	3.2	3.2
t_H	D(0) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width CK(1) [use load on Q]	4.13	0.206	5.0	5.8	6.6	7.4	8.2
t_W	pulse width CK(0)	3.24	0.000	3.2	3.2	3.2	3.2	3.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

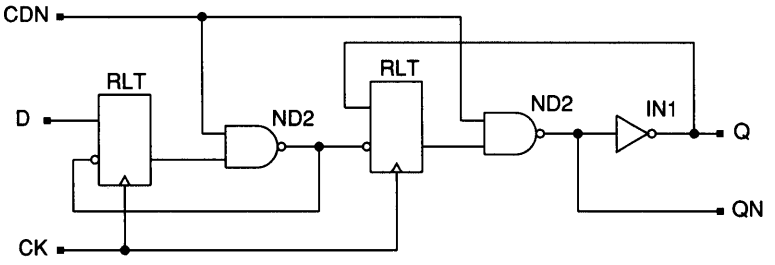
- Positive edge triggered D Flip-Flop with clear and single clock input. Output QN is the complement of Q.

- Hard Macrocell
- 6 Gate Equivalents
- 8 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs			Outputs	
CDN	CK	D	Q	QN
0	?	?	0	$\overline{Q}$
1	↑	?	D	$\overline{Q}$
1	1	?	Q	$\overline{Q}$
1	↓	?	Q	$\overline{Q}$
1	0	?	Q	$\overline{Q}$

Pin Load

Pin	Std Load
CK	1.1
D	0.5
CDN	2.0

Timing Parameters[1]

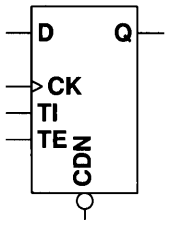
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to QN(↑) with D(0)	3.49	0.208	4.3	5.2	6.0	6.8	7.6
t_{PD}	CK(↑) to QN(↓) with D(1)	3.02	0.162	3.7	4.3	5.0	5.6	6.3
t_{PD}	CK(↑) to QN(↑) with D(0)	3.49	0.208	4.3	5.2	6.0	6.8	7.6
t_{PD}	QN(↑) to Q(↓) with D(0)	1.21	0.193	2.0	2.8	3.5	4.3	5.1
t_{PD}	CK(↑) to QN(↓) with D(1)	3.02	0.162	3.7	4.3	5.0	5.6	6.3
t_{PD}	QN(↓) to Q(↑) with D(1)	1.15	0.317	2.4	3.7	5.0	6.2	7.5
t_{PD}	CDN(↓) to QN(↑)	1.52	0.295	2.7	3.9	5.1	6.2	7.4
t_{PD}	CDN(↓) to QN(↑)	1.52	0.295	2.7	3.9	5.1	6.2	7.4
t_{PD}	QN(↑) to Q(↓) with D(0)	1.21	0.193	2.0	2.8	3.5	4.3	5.1
t_S	CDN(1) recovery CK(↑)	1.09	0.000	1.1	1.1	1.1	1.1	1.1
t_H	CDN(0) hold CK(↑)	2.75	0.000	2.8	2.8	2.8	2.8	2.8
t_W	pulse width CDN(0) [use load on Q]	7.28	0.271	8.4	9.5	10.5	11.6	12.7
t_S	D(0) setup CK(↑)	3.15	0.000	3.1	3.1	3.1	3.1	3.1
t_S	D(1) setup CK(↑)	3.14	0.000	3.1	3.1	3.1	3.1	3.1
t_H	D(0) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width CK(1) [use load on Q]	6.1	0.271	7.2	8.3	9.4	10.4	11.5
t_W	pulse width CK(0)	3.23	0.000	3.2	3.2	3.2	3.2	3.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

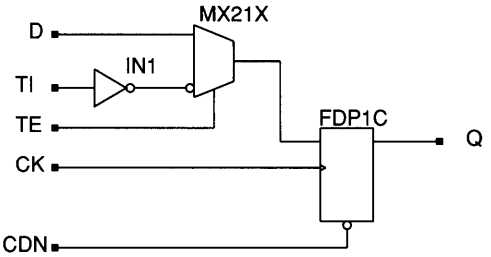
- Positive edge triggered D Flip-Flop with clear and single clock input. Multiplexer on data input allows selection of D for normal operation or TI for scan testing.

- Soft Macrocell
- 14 Gate Equivalents
- 9 TPTs
- 3 RLTs

Symbol



Schematic



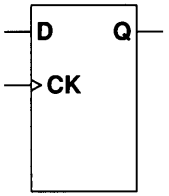
Function Table

Inputs					Output
CDN	CK	TE	TI	D	Q
0	?	?	?	?	0
1	↑	0	?	?	D
1	↑	1	?	?	TI
1	1	?	?	?	Q
1	↓	?	?	?	Q
1	0	?	?	?	Q

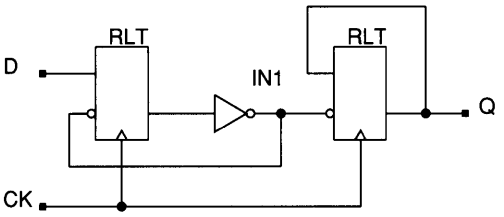
- Positive edge triggered D Flip-Flop with single clock input.

- Hard Macrocell
- 6 Gate Equivalents
- 3 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs		Output
CK	D	Q
↑	?	D
1	?	Q
↓	?	Q
0	?	Q

Pin Load

Pin	Std Load
CK	1.1
D	0.5

Timing Parameters[1]

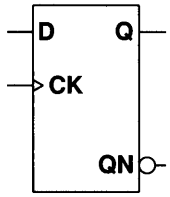
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓) with D(0)	2.84	0.113	3.3	3.7	4.2	4.6	5.1
t_{PD}	CK(↑) to Q(↑) with D(1)	2.3	0.179	3.0	3.7	4.4	5.2	5.9
t_S	D(0) setup CK(↑)	3.24	0.000	3.2	3.2	3.2	3.2	3.2
t_S	D(1) setup CK(↑)	3.15	0.000	3.1	3.1	3.1	3.1	3.1
t_H	D(0) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width CK(1) [use load on Q]	2.84	0.179	3.6	4.3	5.0	5.7	6.4
t_W	pulse width CK(0)	3.24	0.000	3.2	3.2	3.2	3.2	3.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

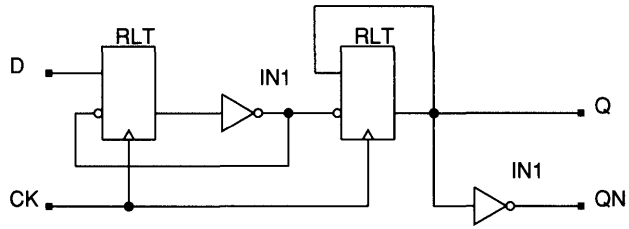
- Positive edge triggered D Flip-Flop with single clock input. The output QN is the complement of Q.

- Hard Macrocell
- 7 Gate Equivalents
- 3 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs		Outputs	
CK	D	Q	QN
↑	?	D	$\overline{Q}$
1	?	Q	$\overline{Q}$
↓	?	Q	$\overline{Q}$
0	?	Q	$\overline{Q}$

Pin Load

Pin	Std Load
CK	1.1
D	0.5

Timing Parameters[1]

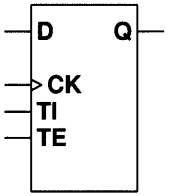
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓) with D(0)	2.93	0.113	3.4	3.8	4.3	4.7	5.2
t_{PD}	CK(↑) to Q(↑) with D(1)	2.48	0.18	3.2	3.9	4.6	5.4	6.1
t_{PD}	CK(↑) to Q(↓) with D(0)	2.93	0.113	3.4	3.8	4.3	4.7	5.2
t_{PD}	Q(↓) to QN(↑) with D(0)	0.607	0.296	1.8	3.0	4.2	5.3	6.5
t_{PD}	CK(↑) to Q(↑) with D(1)	2.48	0.18	3.2	3.9	4.6	5.4	6.1
t_{PD}	Q(↑) to QN(↓) with D(1)	1.01	0.148	1.6	2.2	2.8	3.4	4.0
t_S	D(0) setup CK(↑)	3.13	0.000	3.1	3.1	3.1	3.1	3.1
t_S	D(1) setup CK(↑)	3.05	0.000	3.0	3.0	3.0	3.0	3.0
t_H	D(0) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width CK(1) [use load on Q]	2.93	0.180	3.6	4.4	5.1	5.8	6.5
t_W	pulse width CK(0)	3.14	0.000	3.1	3.1	3.1	3.1	3.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

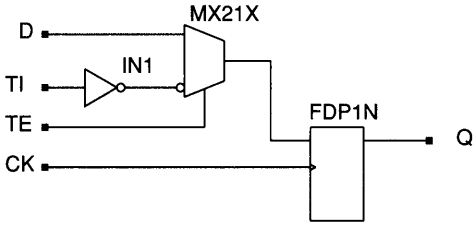
- Positive edge triggered D Flip-Flop with single clock input. Multiplexer on data input allows selection of D for normal operation or TI for scan testing.

- Soft Macrocell
- 11 Gate Equivalents
- 5 TPTs
- 3 RLTs

Symbol



Schematic



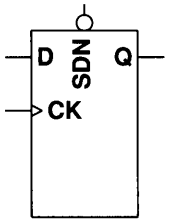
Function Table

Inputs				Output
CK	TE	TI	D	Q
↑	0	?	?	D
↑	1	?	?	TI
1	?	?	?	Q
↓	?	?	?	Q
0	?	?	?	Q

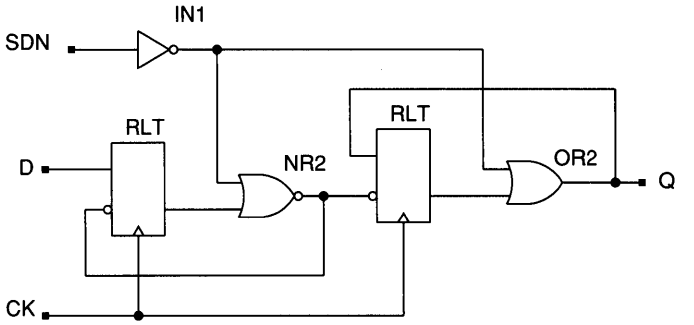
- Positive edge triggered D Flip-Flop with pre-set and single clock input.

- Hard Macrocell
- 8 Gate Equivalents
- 10 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs			Output
SDN	CK	D	Q
0	?	?	1
1	↑	?	D
1	1	?	Q
1	↓	?	Q
1	0	?	Q

Pin Load

Pin	Std Load
CK	1.1
D	0.5
SDN	1.0

Timing Parameters[1]

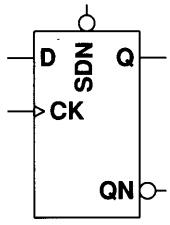
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓) with D(0)	4.55	0.143	5.1	5.7	6.3	6.8	7.4
t_{PD}	CK(↑) to Q(↑) with D(1)	3.64	0.207	4.5	5.3	6.1	7.0	7.8
t_{PD}	SDN(↓) to Q(↑)	2.96	0.294	4.1	5.3	6.5	7.7	8.8
t_S	SDN(1) recovery CK(↑)	2.48	0.000	2.5	2.5	2.5	2.5	2.5
t_H	SDN(0) hold CK(↑)	1.26	0.000	1.3	1.3	1.3	1.3	1.3
t_W	pulse width SDN(0) [use load on Q]	4.9	0.207	5.7	6.6	7.4	8.2	9.0
t_S	D(0) setup CK(↑)	3.45	0.000	3.5	3.5	3.5	3.5	3.5
t_S	D(1) setup CK(↑)	3.08	0.000	3.1	3.1	3.1	3.1	3.1
t_H	D(0) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width CK(1) [use load on Q]	4.55	0.207	5.4	6.2	7.0	7.9	8.7
t_W	pulse width CK(0)	3.38	0.000	3.4	3.4	3.4	3.4	3.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

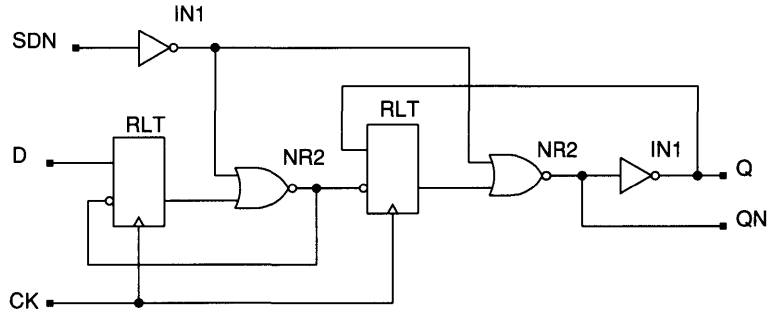
- Positive edge triggered D Flip-Flop with pre-set and single clock input. The output QN is the complement of Q.

- Hard Macrocell
- 8 Gate Equivalents
- 9 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs			Outputs	
SDN	CK	D	Q	QN
0	?	?	1	$\overline{Q}$
1	↑	?	D	$\overline{Q}$
1	1	?	Q	$\overline{Q}$
1	↓	?	Q	$\overline{Q}$
1	0	?	Q	$\overline{Q}$

Pin Load

Pin	Std Load
CK	1.1
D	0.5
SDN	1.0

Timing Parameters[1]

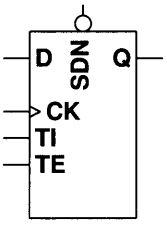
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to QN(↑) with D(0)	3.84	0.307	5.1	6.3	7.5	8.8	10.0
t_{PD}	CK(↑) to QN(↓) with D(1)	3.05	0.14	3.6	4.2	4.7	5.3	5.8
t_{PD}	CK(↑) to QN(↑) with D(0)	3.84	0.307	5.1	6.3	7.5	8.8	10.0
t_{PD}	QN(↑) to Q(↓) with D(0)	1.57	0.195	2.4	3.1	3.9	4.7	5.5
t_{PD}	CK(↑) to QN(↓) with D(1)	3.05	0.14	3.6	4.2	4.7	5.3	5.8
t_{PD}	QN(↓) to Q(↑) with D(1)	1.07	0.315	2.3	3.6	4.9	6.1	7.4
t_{PD}	SDN(↓) to QN(↓)	2.12	0.19	2.9	3.6	4.4	5.2	5.9
t_{PD}	SDN(↓) to QN(↓)	2.12	0.19	2.9	3.6	4.4	5.2	5.9
t_{PD}	QN(↓) to Q(↑) with D(1)	1.07	0.315	2.3	3.6	4.9	6.1	7.4
t_S	SDN(1) recovery CK(↑)	2.19	0.000	2.2	2.2	2.2	2.2	2.2
t_H	SDN(0) hold CK(↑)	1.25	0.000	1.2	1.2	1.2	1.2	1.2
t_W	pulse width SDN(0) [use load on Q]	5.89	0.222	6.8	7.7	8.5	9.4	10.3
t_S	D(0) setup CK(↑)	3.42	0.000	3.4	3.4	3.4	3.4	3.4
t_S	D(1) setup CK(↑)	3.03	0.000	3.0	3.0	3.0	3.0	3.0
t_H	D(0) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold CK(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width CK(1) [use load on Q]	7.73	0.275	8.8	9.9	11.0	12.1	13.2
t_W	pulse width CK(0)	3.34	0.000	3.3	3.3	3.3	3.3	3.3

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

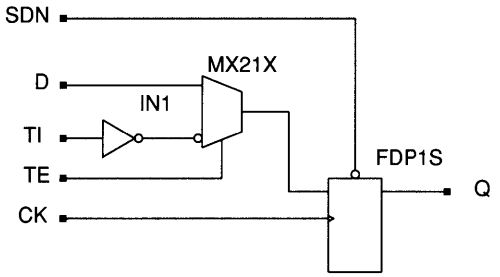
- Positive edge triggered D Flip-Flop with pre-set and single clock input. Multiplexer on data input allows selection of D for normal operation or TI for scan testing.

- Soft Macrocell
- 13 Gate Equivalents
- 12 TPTs
- 3 RLTs

Symbol



Schematic



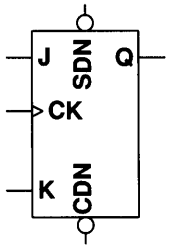
Function Table

Inputs					Output
SDN	CK	TE	TI	D	Q
0	?	?	?	?	1
1	↑	0	?	?	D
1	↑	1	?	?	TI
1	1	?	?	?	Q
1	↓	?	?	?	Q
1	0	?	?	?	Q

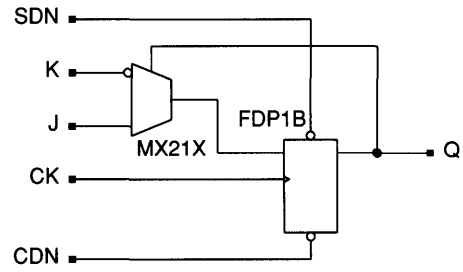
- Positive edge triggered JK Flip-Flop with pre-set, clear and single clock input.

- Soft Macrocell
- 11 Gate Equivalents
- 15 TPTs
- 3 RLTs

Symbol



Schematic



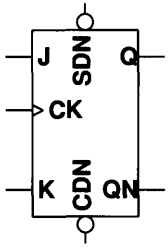
Function Table

Inputs					Output
CDN	SDN	CK	J	K	Q
0	?	?	?	?	0
1	0	?	?	?	1
1	1	↑	1	1	$\overline{Q}$
1	1	↑	0	1	0
1	1	↑	1	0	1
1	1	↑	0	0	Q
1	1	↓	?	?	Q
1	1	0	?	?	Q
1	1	1	?	?	Q

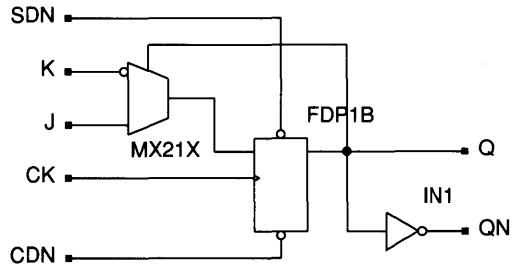
- Positive edge triggered JK Flip-Flop with pre-set, clear and single clock input. Output QN is the complement of Q.

- Soft Macrocell
- 12 Gate Equivalents
- 17 TPTs
- 3 RLTs

Symbol



Schematic



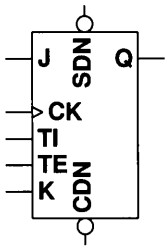
Function Table

Inputs					Outputs	
CDN	SDN	CK	J	K	Q	QN
0	?	?	?	?	0	$\overline{Q}$
1	0	?	?	?	1	$\overline{Q}$
1	1	↑	1	1	$\overline{Q}$	$\overline{Q}$
1	1	↑	0	1	0	$\overline{Q}$
1	1	↑	1	0	1	$\overline{Q}$
1	1	↑	0	0	Q	$\overline{Q}$
1	1	↓	?	?	Q	$\overline{Q}$
1	1	0	?	?	Q	$\overline{Q}$
1	1	1	?	?	Q	$\overline{Q}$

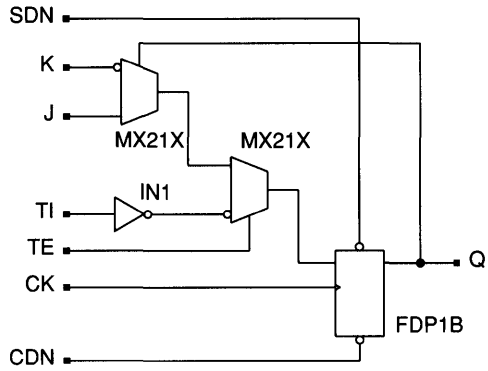
- Positive edge triggered JK Flip-Flop with pre-set, clear and single clock input. Multiplexer on data input allows selection of normal operation or scan testing.

- Soft Macrocell
- 16 Gate Equivalents
- 17 TPTs
- 4 RLTs

Symbol



Schematic



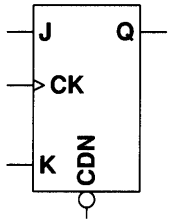
Function Table

Inputs							Output
CDN	SDN	CK	TE	TI	J	K	Q
0	?	?	?	?	?	?	0
1	0	?	?	?	?	?	1
1	1	↑	1	?	?	?	TI
1	1	↑	0	?	1	1	$\overline{Q}$
1	1	↑	0	?	0	1	0
1	1	↑	0	?	1	0	1
1	1	↑	0	?	0	0	Q
1	1	↓	?	?	?	?	Q
1	1	0	?	?	?	?	Q
1	1	1	?	?	?	?	Q

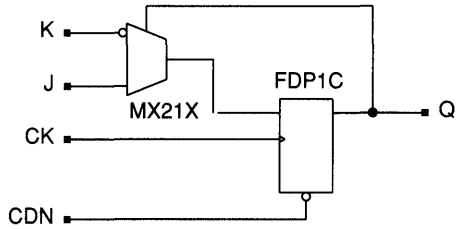
- Positive edge triggered JK Flip-Flop with clear and single clock input.

- Soft Macrocell
- 13 Gate Equivalents
- 7 TPTs
- 3 RLTs

Symbol



Schematic



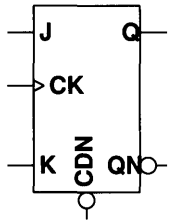
Function Table

Inputs				Output
CDN	CK	J	K	Q
0	?	?	?	0
1	↑	1	1	$\overline{Q}$
1	↑	0	1	0
1	↑	1	0	1
1	↑	0	0	Q
1	↓	?	?	Q
1	0	?	?	Q
1	1	?	?	Q

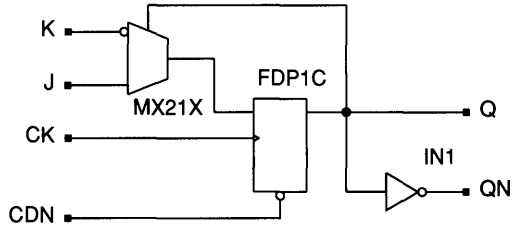
- Positive edge triggered JK Flip-Flop with clear and single clock input. Output QN is the complement of Q.

- Soft Macrocell
- 14 Gate Equivalents
- 9 TPTs
- 3 RLTs

Symbol



Schematic



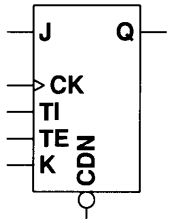
Function Table

Inputs				Outputs	
CDN	CK	J	K	Q	QN
0	?	?	?	0	$\overline{Q}$
1	↑	1	1	$\overline{Q}$	$\overline{Q}$
1	↑	0	1	0	$\overline{Q}$
1	↑	1	0	1	$\overline{Q}$
1	↑	0	0	Q	$\overline{Q}$
1	↓	?	?	Q	$\overline{Q}$
1	0	?	?	Q	$\overline{Q}$
1	1	?	?	Q	$\overline{Q}$

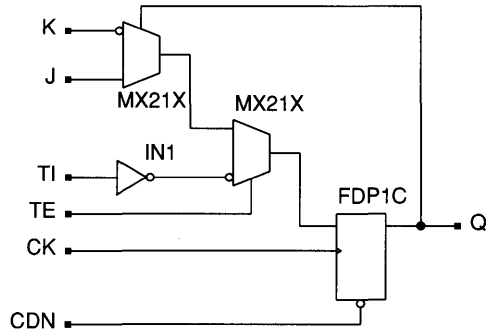
- Positive edge triggered JK Flip-Flop with clear and single clock input. Multiplexer on data input allows selection of normal operation or scan testing.

- Soft Macrocell
- 18 Gate Equivalents
- 9 TPTs
- 4 RLTs

Symbol



Schematic



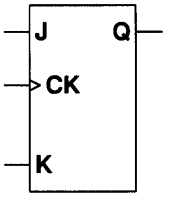
Function Table

Inputs						Output
CDN	CK	TE	TI	J	K	Q
0	?	?	?	?	?	0
1	↑	1	?	?	?	TI
1	↑	0	?	1	1	$\overline{Q}$
1	↑	0	?	0	1	0
1	↑	0	?	1	0	1
1	↑	0	?	0	0	Q
1	↓	?	?	?	?	Q
1	0	?	?	?	?	Q
1	1	?	?	?	?	Q

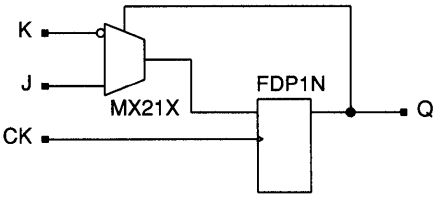
- Positive edge triggered JK Flip-Flop with single clock input.

- Soft Macrocell
- 10 Gate Equivalents
- 3 TPTs
- 3 RLTs

Symbol



Schematic



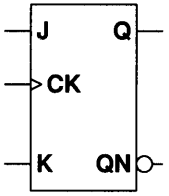
Function Table

Inputs			Output
CK	J	K	Q
↑	1	1	$\overline{Q}$
↑	0	1	0
↑	1	0	1
↑	0	0	Q
↓	?	?	Q
0	?	?	Q
1	?	?	Q

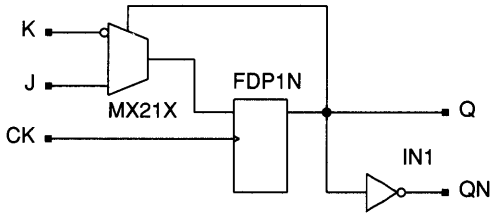
- Positive edge triggered JK Flip-Flop with single clock input. The output QN is the complement of Q.

- Soft Macrocell
- 11 Gate Equivalents
- 5 TPTs
- 3 RLTs

Symbol



Schematic



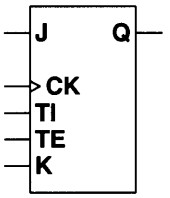
Function Table

Inputs			Outputs	
CK	J	K	Q	QN
↑	1	1	$\overline{Q}$	$\overline{Q}$
↑	0	1	0	$\overline{Q}$
↑	1	0	1	$\overline{Q}$
↑	0	0	Q	$\overline{Q}$
↓	?	?	Q	$\overline{Q}$
0	?	?	Q	$\overline{Q}$
1	?	?	Q	$\overline{Q}$

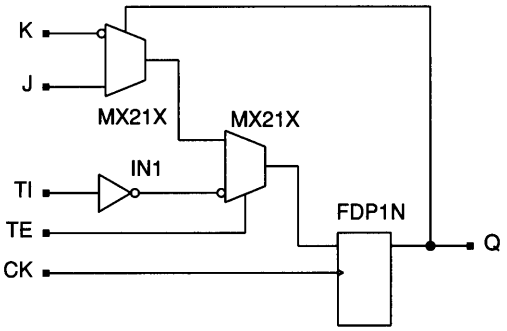
- Positive edge triggered JK Flip-Flop with single clock input. Multiplexer on data input allows selection of normal operation or scan testing.

- Soft Macrocell
- 15 Gate Equivalents
- 5 TPTs
- 4 RLTs

Symbol



Schematic



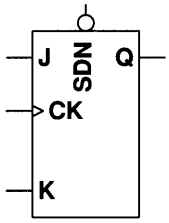
Function Table

Inputs					Output
CK	TE	TI	J	K	Q
↑	1	?	?	?	TI
↑	0	?	1	1	$\overline{Q}$
↑	0	?	0	1	0
↑	0	?	1	0	1
↑	0	?	0	0	Q
↓	?	?	?	?	Q
0	?	?	?	?	Q
1	?	?	?	?	Q

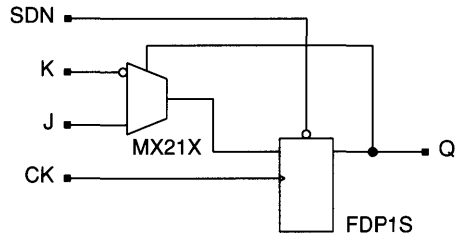
- Positive edge triggered JK Flip-Flop with pre-set and single clock input.

- Soft Macrocell
- 12 Gate Equivalents
- 10 TPTs
- 3 RLTs

Symbol



Schematic



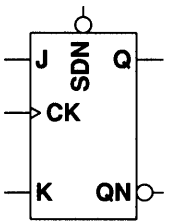
Function Table

Inputs				Output
SDN	CK	J	K	Q
0	?	?	?	1
1	↑	1	1	$\overline{Q}$
1	↑	0	1	0
1	↑	1	0	1
1	↑	0	0	Q
1	↓	?	?	Q
1	0	?	?	Q
1	1	?	?	Q

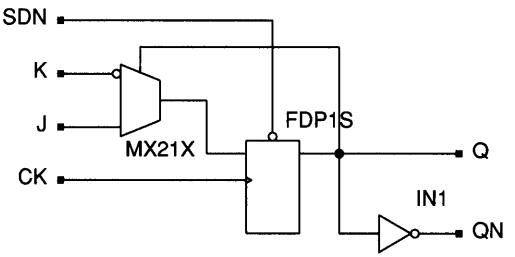
- Positive edge triggered JK Flip-Flop with pre-set and single clock input. The output QN is the complement of Q.

- Soft Macrocell
- 13 Gate Equivalents
- 12 TPTs
- 3 RLTs

Symbol



Schematic



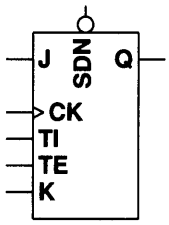
Function Table

Inputs				Outputs	
SDN	CK	J	K	Q	QN
0	?	?	?	1	$\overline{Q}$
1	↑	1	1	$\overline{Q}$	$\overline{Q}$
1	↑	0	1	0	$\overline{Q}$
1	↑	1	0	1	$\overline{Q}$
1	↑	0	0	Q	$\overline{Q}$
1	↓	?	?	Q	$\overline{Q}$
1	0	?	?	Q	$\overline{Q}$
1	1	?	?	Q	$\overline{Q}$

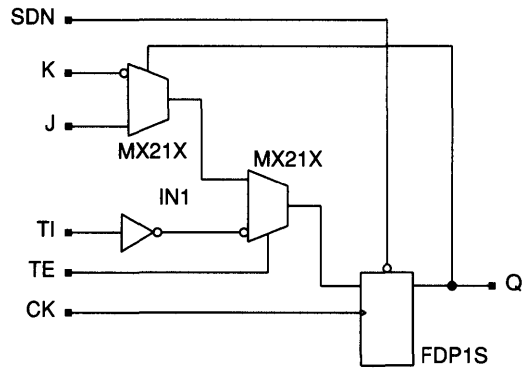
- Positive edge triggered JK Flip-Flop with pre-set and single clock input. Multiplexer on data input allows selection of normal operation or scan testing.

- Soft Macrocell
- 17 Gate Equivalents
- 12 TPTs
- 4 RLTs

Symbol



Schematic



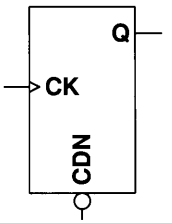
Function Table

Inputs						Output
SDN	CK	TE	TI	J	K	Q
0	?	?	?	?	?	1
1	↑	1	?	?	?	TI
1	↑	0	?	1	1	$\overline{Q}$
1	↑	0	?	0	1	0
1	↑	0	?	1	0	1
1	↑	0	?	0	0	Q
1	↓	?	?	?	?	Q
1	0	?	?	?	?	Q
1	1	?	?	?	?	Q

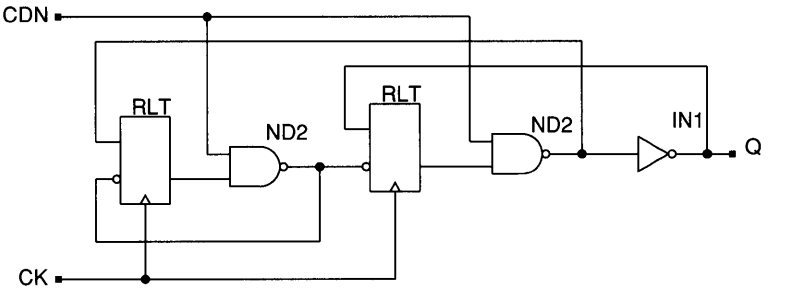
- Positive edge-triggered toggle flip-flop with clear.

- Hard Macrocell
- 8 Gate Equivalents
- 8 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs		Output
CDN	CK	Q
0	?	0
1	↑	$\overline{Q}$
1	1	Q
1	↓	Q
1	0	Q

Pin Load

Pin	Std Load
CK	1.1
CDN	2.0

Timing Parameters[1]

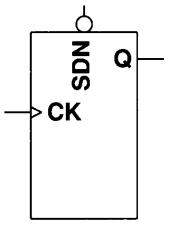
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓)	4.4	0.193	5.2	5.9	6.7	7.5	8.3
t_{PD}	CK(↑) to Q(↑)	4.17	0.22	5.0	5.9	6.8	7.7	8.6
t_{PD}	CDN(↓) to Q(↓)	2.08	0.272	3.2	4.3	5.3	6.4	7.5
t_S	CDN(1) recovery CK(↑)	1.12	0.000	1.1	1.1	1.1	1.1	1.1
t_H	CDN(0) hold CK(↑)	2.72	0.000	2.7	2.7	2.7	2.7	2.7
t_W	pulse width CDN(0) [use load on Q]	5.11	0.272	6.2	7.3	8.4	9.5	10.5
t_W	pulse width CK(1) [use load on Q]	4.4	0.272	5.5	6.6	7.7	8.7	9.8
t_W	pulse width CK(0)	3.18	0.000	3.2	3.2	3.2	3.2	3.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

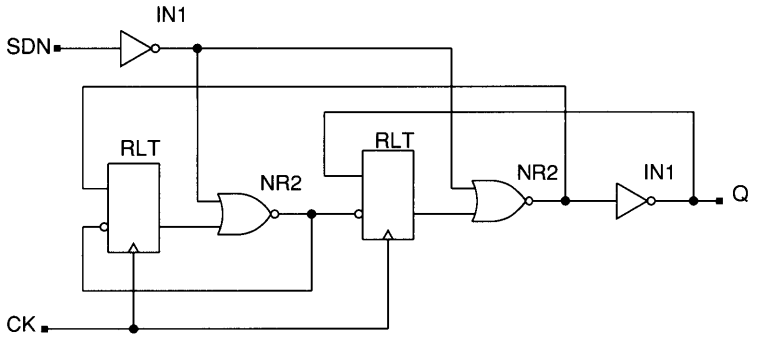
- Positive edge-triggered toggle flip-flop with set.

- Hard Macrocell
- 8 Gate Equivalents
- 9 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs		Output
SDN	CK	Q
0	?	1
1	↑	$\overline{Q}$
1	1	Q
1	↓	Q
1	0	Q

Pin Load

Pin	Std Load
CK	1.1
SDN	1.0

Timing Parameters[1]

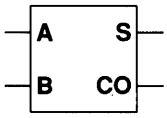
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	CK(↑) to Q(↓)	4.97	0.195	5.7	6.5	7.3	8.1	8.9
t_{PD}	CK(↑) to Q(↑)	4.04	0.219	4.9	5.8	6.7	7.5	8.4
t_{PD}	SDN(↓) to Q(↑)	3.08	0.312	4.3	5.6	6.8	8.1	9.3
t_S	SDN(1) recovery CK(↑)	2.2	0.000	2.2	2.2	2.2	2.2	2.2
t_H	SDN(0) hold CK(↑)	1.29	0.000	1.3	1.3	1.3	1.3	1.3
t_W	pulse width SDN(0) [use load on Q]	5.14	0.219	6.0	6.9	7.8	8.6	9.5
t_W	pulse width CK(1) [use load on Q]	4.97	0.274	6.1	7.2	8.3	9.4	10.5
t_W	pulse width CK(0)	3.39	0.000	3.4	3.4	3.4	3.4	3.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

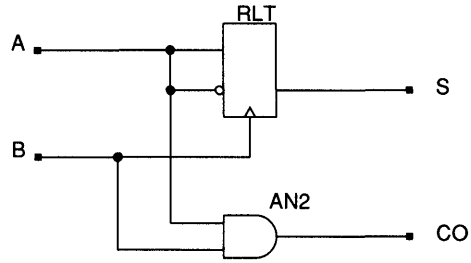
- 1-Bit Half Adder

- Hard Macrocell
- 5 Gate Equivalents
- 5 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs		Outputs	
A	B	S	CO
0	0	0	0
1	0	1	0
0	1	1	0
1	1	0	1

Pin Load

Pin	Std Load
A	1.8
B	1.6

Timing Parameters[1]

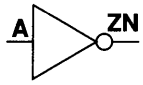
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to S(↑) with B(0)	2.35	0.179	3.1	3.8	4.5	5.2	5.9
t_{PD}	A(↓) to S(↓) with B(0)	2.39	0.147	3.0	3.6	4.2	4.7	5.3
t_{PD}	A(↑) to S(↓) with B(1)	2.87	0.113	3.3	3.8	4.2	4.7	5.1
t_{PD}	A(↓) to S(↑) with B(1)	2.34	0.25	3.3	4.3	5.3	6.3	7.3
t_{PD}	B(↑) to S(↑) with A(0)	2.22	0.179	2.9	3.7	4.4	5.1	5.8
t_{PD}	B(↓) to S(↓) with A(0)	2.31	0.147	2.9	3.5	4.1	4.7	5.3
t_{PD}	B(↑) to S(↓) with A(1)	2.79	0.113	3.2	3.7	4.1	4.6	5.1
t_{PD}	B(↓) to S(↑) with A(1)	2.42	0.25	3.4	4.4	5.4	6.4	7.4
t_{PD}	A(↑) to CO(↑)	1.54	0.203	2.4	3.2	4.0	4.8	5.6
t_{PD}	A(↓) to CO(↓)	1.68	0.19	2.4	3.2	4.0	4.7	5.5
t_{PD}	B(↑) to CO(↑)	1.6	0.202	2.4	3.2	4.0	4.8	5.6
t_{PD}	B(↓) to CO(↓)	1.7	0.191	2.5	3.2	4.0	4.8	5.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

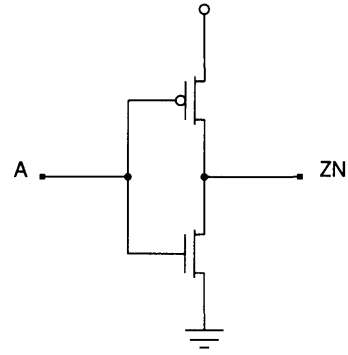
- Inverter, 1X Drive

- Hard Macrocell
- 1 Gate Equivalents
- 2 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	1.0

Timing Parameters[1]

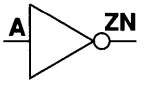
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.08	0.145	1.7	2.2	2.8	3.4	4.0
t_{PD}	A(↓) to ZN(↑)	0.66	0.289	1.8	3.0	4.1	5.3	6.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

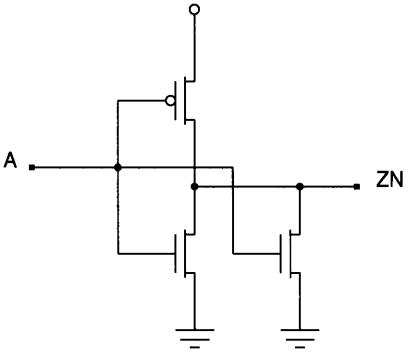
- Inverter, 1X Pull-up, 2X Pull-down

- Hard Macrocell
- 1 Gate Equivalents
- 4 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	1.4

Timing Parameters[1]

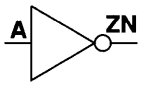
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	0.957	0.111	1.4	1.8	2.3	2.7	3.2
t_{PD}	A(↓) to ZN(↑)	0.668	0.286	1.8	3.0	4.1	5.2	6.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

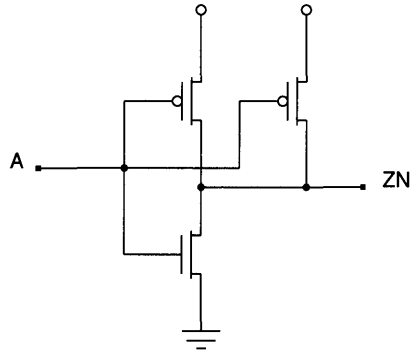
- Inverter, 1X Pull-down, 2X Pull-up

- Hard Macrocell
- 1 Gate Equivalents
- 4 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	1.6

Timing Parameters[1]

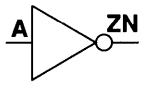
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	0.945	0.144	1.5	2.1	2.7	3.2	3.8
t_{PD}	A(↓) to ZN(↑)	0.846	0.188	1.6	2.4	3.1	3.9	4.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

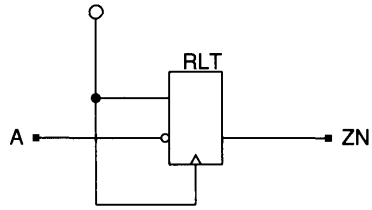
- Inverter using an RLT

- Hard Macrocell
- 1 Gate Equivalents
- 0 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	0.4

Timing Parameters[1]

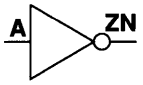
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	2.79	0.113	3.2	3.7	4.1	4.6	5.1
t_{PD}	A(↓) to ZN(↑)	2.08	0.25	3.1	4.1	5.1	6.1	7.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

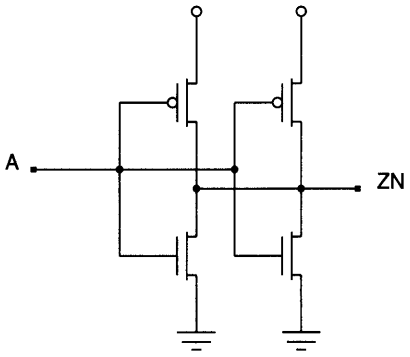
- Inverter, 2X Drive

- Hard Macrocell
- 1 Gate Equivalents
- 4 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	2.0

Timing Parameters[1]

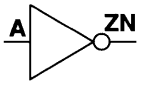
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	0.843	0.111	1.3	1.7	2.2	2.6	3.1
t_{PD}	A(↓) to ZN(↑)	0.694	0.183	1.4	2.2	2.9	3.6	4.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

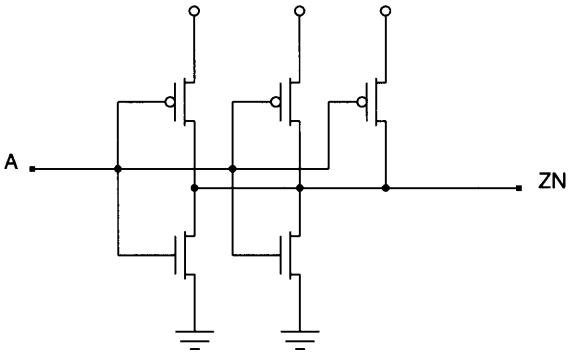
- Inverter, 2X Pull-down, 3X Pull-up drive.

- Hard Macrocell
- 2 Gate Equivalents
- 4 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	2.6

Timing Parameters[1]

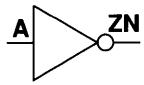
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	0.866	0.137	1.4	2.0	2.5	3.1	3.6
t_{PD}	A(↓) to ZN(↑)	0.797	0.182	1.5	2.2	3.0	3.7	4.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

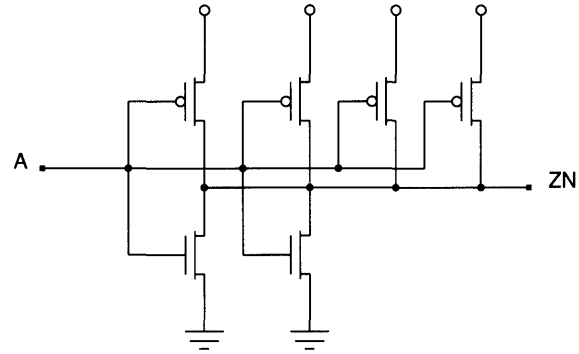
- Inverter, 2X Pull-down, 4X Pull-up drive.

- Hard Macrocell
- 2 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	3.2

Timing Parameters[1]

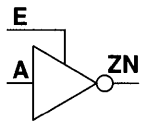
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	0.776	0.109	1.2	1.6	2.1	2.5	3.0
t_{PD}	A(↓) to ZN(↑)	0.697	0.134	1.2	1.8	2.3	2.8	3.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

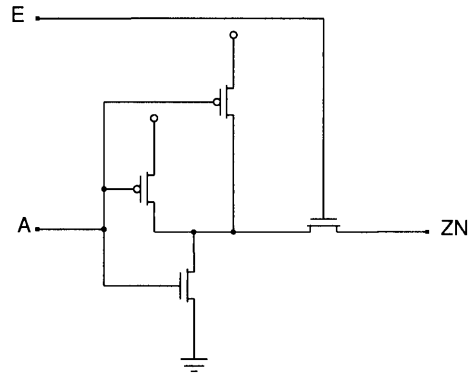
- Inverting three-state buffer, 1X drive. Macrocell must be used in conjunction with a three-state bus receiver (see IZ1 and NZ1).

- Hard Macrocell
- 1 Gate Equivalents
- 3 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	E	ZN
?	0	*Z*
?	1	$\overline{A}$

Pin Load

Pin	Std Load
A	1.0
E	0.5

Timing Parameters[1]

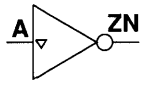
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)							
t_{PD}	A(↓) to ZN(↑)							

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

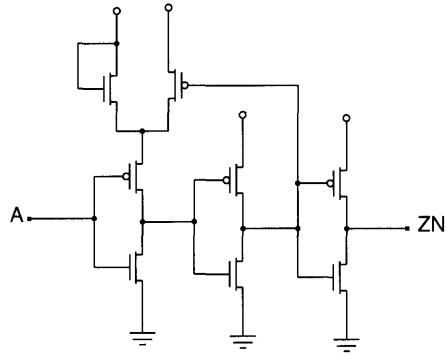
- Inverting three-state bus receiver. Note: A bus receiver cell must be used in conjunction with three-state bus drivers.

- Hard Macrocell
- 2 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	ZN
?	$\overline{A}$

Pin Load

Pin	Std Load
A	1.0

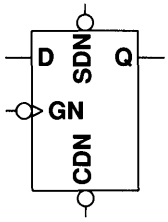
Timing Parameters

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)							
t_{PD}	A(↓) to ZN(↑)							

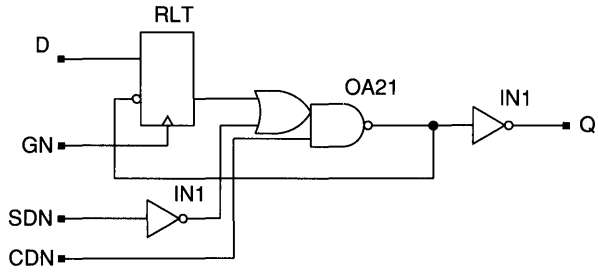
- D-Latch with clear and set. Latch is transparent when GN is asserted low and is latched when GN is high.

- Hard Macrocell
- 5 Gate Equivalents
- 9 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs				Output
CDN	SDN	GN	D	Q
0	?	?	?	0
1	0	?	?	1
1	1	0	?	D
1	1	1	?	Q

Pin Load

Pin	Std Load
GN	0.5
D	0.5
CDN	1.0
SDN	1.0

Timing Parameters[1]

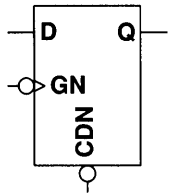
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	GN(↓) to Q(↓) with D(0)	4.77	0.203	5.6	6.4	7.2	8.0	8.8
t_{PD}	GN(↓) to Q(↑) with D(1)	4.28	0.294	5.5	6.6	7.8	9.0	10.2
t_{PD}	D(↑) to Q(↑)	4.2	0.207	5.0	5.9	6.7	7.5	8.3
t_{PD}	D(↓) to Q(↓)	4.86	0.203	5.7	6.5	7.3	8.1	8.9
t_{PD}	CDN(↓) to Q(↓)	1.75	0.191	2.5	3.3	4.0	4.8	5.6
t_{PD}	CDN(↑) to Q(↑)	1.89	0.205	2.7	3.5	4.4	5.2	6.0
t_{PD}	SDN(↓) to Q(↑)	3.26	0.295	4.4	5.6	6.8	8.0	9.2
t_{PD}	SDN(↑) to Q(↓)	3.64	0.149	4.2	4.8	5.4	6.0	6.6
t_S	D(0) setup GN(↑)	4.16	0.000	4.2	4.2	4.2	4.2	4.2
t_S	D(1) setup GN(↑)	3.42	0.000	3.4	3.4	3.4	3.4	3.4
t_W	pulse width GN(0)	4.07	0.000	4.1	4.1	4.1	4.1	4.1
t_S	CDN(1) recovery GN(↑)	1.11	0.000	1.1	1.1	1.1	1.1	1.1
t_H	CDN(0) hold GN(↑)	2.72	0.000	2.7	2.7	2.7	2.7	2.7
t_W	pulse width CDN(0)	3.56	0.000	3.6	3.6	3.6	3.6	3.6
t_S	SDN(1) recovery GN(↑)	2.94	0.000	2.9	2.9	2.9	2.9	2.9
t_H	SDN(0) hold GN(↑)	1.41	0.000	1.4	1.4	1.4	1.4	1.4
t_W	pulse width SDN(0)	4.68	0.000	4.7	4.7	4.7	4.7	4.7

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

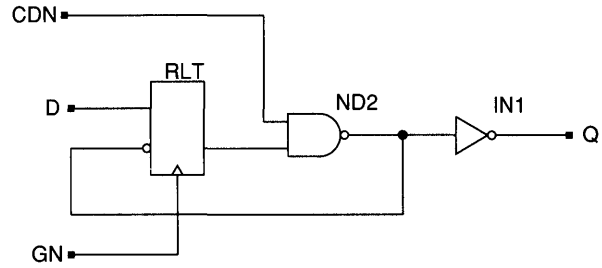
- D-Latch with clear. Latch is transparent when GN is asserted low and is latched when GN is high.

- Hard Macrocell
- 4 Gate Equivalents
- 5 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs			Output
CDN	GN	D	Q
0	?	?	0
1	0	?	D
1	1	?	Q

Pin Load

Pin	Std Load
GN	0.5
D	0.5
CDN	1.0

Timing Parameters[1]

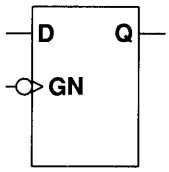
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	GN(↓) to Q(↓) with D(0)	3.7	0.19	4.5	5.2	6.0	6.7	7.5
t_{PD}	GN(↓) to Q(↑) with D(1)	3.81	0.291	5.0	6.1	7.3	8.5	9.6
t_{PD}	D(↑) to Q(↑)	3.73	0.205	4.6	5.4	6.2	7.0	7.8
t_{PD}	D(↓) to Q(↓)	3.79	0.19	4.6	5.3	6.1	6.8	7.6
t_{PD}	CDN(↓) to Q(↓)	1.75	0.191	2.5	3.3	4.0	4.8	5.6
t_{PD}	CDN(↑) to Q(↑)	1.63	0.202	2.4	3.2	4.1	4.9	5.7
t_S	D(0) setup GN(↑)	3.25	0.000	3.2	3.2	3.2	3.2	3.2
t_S	D(1) setup GN(↑)	3.2	0.000	3.2	3.2	3.2	3.2	3.2
t_H	D(0) hold GN(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold GN(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width GN(0)	3.28	0.000	3.3	3.3	3.3	3.3	3.3
t_S	CDN(1) recovery GN(↑)	1.14	0.000	1.1	1.1	1.1	1.1	1.1
t_H	CDN(0) hold GN(↑)	2.74	0.000	2.7	2.7	2.7	2.7	2.7
t_W	pulse width CDN(0)	3.71	0.000	3.7	3.7	3.7	3.7	3.7

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

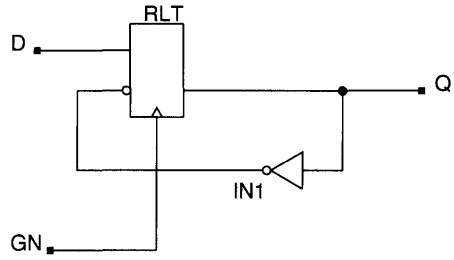
- D-Latch. Latch is transparent when GN is asserted low and is latched when GN is high.

- Hard Macrocell
- 3 Gate Equivalents
- 2 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs		Output
GN	D	Q
0	?	D
1	?	Q

Pin Load

Pin	Std Load
GN	0.5
D	0.5

Timing Parameters[1]

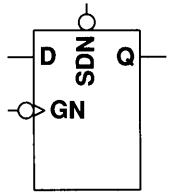
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	GN(↓) to Q(↓) with D(0)	2.37	0.147	3.0	3.5	4.1	4.7	5.3
t_{PD}	GN(↓) to Q(↑) with D(1)	2.58	0.25	3.6	4.6	5.6	6.6	7.6
t_{PD}	D(↑) to Q(↑)	2.5	0.18	3.2	3.9	4.7	5.4	6.1
t_{PD}	D(↓) to Q(↓)	2.46	0.147	3.0	3.6	4.2	4.8	5.4
t_S	D(0) setup GN(↑) [use load Q]	2.46	0.147	3.0	3.6	4.2	4.8	5.4
t_S	D(1) setup GN(↑) [use load Q]	2.5	0.180	3.2	3.9	4.7	5.4	6.1
t_H	D(0) hold GN(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold GN(↑)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width GN(0) [use load on Q]	2.58	0.180	3.3	4.0	4.7	5.5	6.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

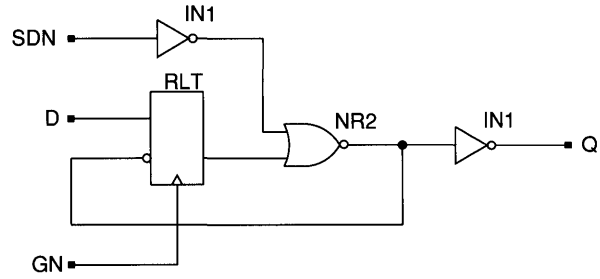
- D-Latch with set. Latch is transparent when GN is asserted low and is latched when GN is high.

- Hard Macrocell
- 4 Gate Equivalents
- 6 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs			Output
SDN	GN	D	Q
0	?	?	1
1	0	?	D
1	1	?	Q

Pin Load

Pin	Std Load
GN	0.5
D	0.5
SDN	1.0

Timing Parameters[1]

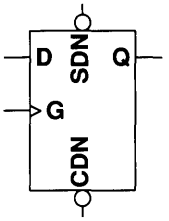
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	GN(↓) to Q(↓) with D(0)	4.15	0.195	4.9	5.7	6.5	7.3	8.1
t_{PD}	GN(↓) to Q(↑) with D(1)	3.83	0.294	5.0	6.2	7.4	8.5	9.7
t_{PD}	D(↑) to Q(↑)	3.74	0.207	4.6	5.4	6.2	7.1	7.9
t_{PD}	D(↓) to Q(↓)	4.24	0.195	5.0	5.8	6.6	7.4	8.1
t_{PD}	SDN(↓) to Q(↑)	2.33	0.293	3.5	4.7	5.8	7.0	8.2
t_{PD}	SDN(↑) to Q(↓)	2.79	0.144	3.4	3.9	4.5	5.1	5.7
t_S	D(0) setup GN(↑) with SDN(1)	3.59	0.000	3.6	3.6	3.6	3.6	3.6
t_S	D(1) setup GN(↑) with SDN(1)	3.1	0.000	3.1	3.1	3.1	3.1	3.1
t_W	pulse width GN(0) with SDN(1)	3.5	0.000	3.5	3.5	3.5	3.5	3.5
t_S	SDN(1) recovery GN(↑)	2.15	0.000	2.1	2.1	2.1	2.1	2.1
t_H	SDN(0) hold GN(↑)	1.45	0.000	1.4	1.4	1.4	1.4	1.4
t_W	pulse width SDN(0)	3.83	0.000	3.8	3.8	3.8	3.8	3.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

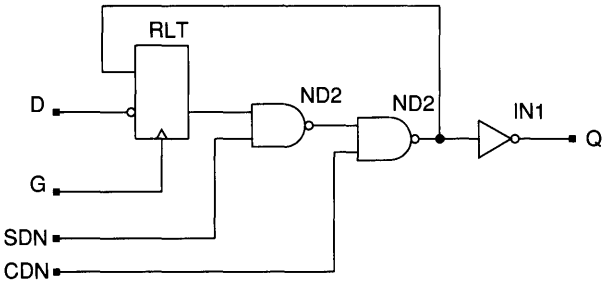
- D-Latch with clear and set. Latch is transparent when G is asserted high and is latched when G is low.

- Hard Macrocell
- 5 Gate Equivalents
- 7 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs				Output
CDN	SDN	G	D	Q
0	?	?	?	0
1	0	?	?	1
1	1	1	?	D
1	1	0	?	Q

Pin Load

Pin	Std Load
G	0.6
D	0.4
CDN	1.0
SDN	1.0

Timing Parameters[1]

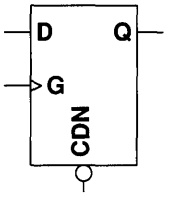
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	G(↑) to Q(↓) with D(0)	4.69	0.141	5.3	5.8	6.4	6.9	7.5
t_{PD}	G(↑) to Q(↑) with D(1)	4.84	0.205	5.7	6.5	7.3	8.1	8.9
t_{PD}	D(↑) to Q(↑)	4.91	0.205	5.7	6.5	7.4	8.2	9.0
t_{PD}	D(↓) to Q(↓)	4.79	0.191	5.6	6.3	7.1	7.8	8.6
t_{PD}	CDN(↓) to Q(↓)	1.76	0.191	2.5	3.3	4.0	4.8	5.6
t_{PD}	CDN(↑) to Q(↑)	1.65	0.202	2.5	3.3	4.1	4.9	5.7
t_{PD}	SDN(↓) to Q(↑)	2.54	0.289	3.7	4.9	6.0	7.2	8.3
t_{PD}	SDN(↑) to Q(↓)	2.82	0.141	3.4	3.9	4.5	5.1	5.6
t_S	D(0) setup G(↓)	4.25	0.000	4.2	4.2	4.2	4.2	4.2
t_S	D(1) setup G(↓)	4.37	0.000	4.4	4.4	4.4	4.4	4.4
t_W	pulse width G(1)	4.3	0.000	4.3	4.3	4.3	4.3	4.3
t_S	CDN(1) recovery G(↑)	1.1	0.000	1.1	1.1	1.1	1.1	1.1
t_H	CDN(0) hold G(↑)	3.25	0.000	3.2	3.2	3.2	3.2	3.2
t_W	pulse width CDN(0)	3.42	0.000	3.4	3.4	3.4	3.4	3.4
t_S	SDN(1) recovery G(↓)	2.28	0.000	2.3	2.3	2.3	2.3	2.3
t_H	SDN(0) hold G(↓)	2.19	0.000	2.2	2.2	2.2	2.2	2.2
t_W	pulse width SDN(0)	4.27	0.000	4.3	4.3	4.3	4.3	4.3

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

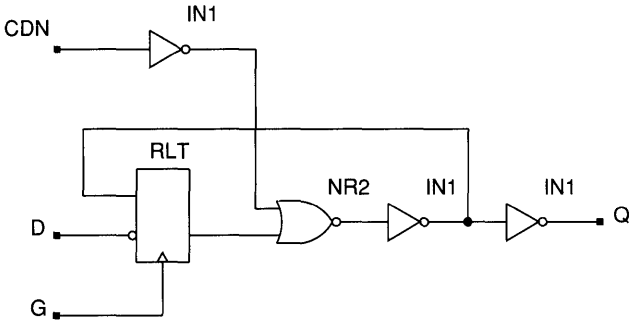
- D-Latch with clear. Latch is transparent when G is asserted high and is latched when G is low.

- Hard Macrocell
- 4 Gate Equivalents
- 7 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs			Output
CDN	G	D	Q
0	?	?	0
1	1	?	D
1	0	?	Q

Pin Load

Pin	Std Load
G	0.6
D	0.4
CDN	1.0

Timing Parameters[1]

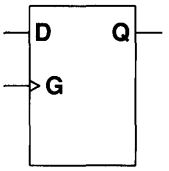
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	G(↑) to Q(↓) with D(0)	4.39	0.141	5.0	5.5	6.1	6.6	7.2
t_{PD}	G(↑) to Q(↑) with D(1)	5.05	0.205	5.9	6.7	7.5	8.3	9.1
t_{PD}	D(↑) to Q(↑)	5.13	0.205	5.9	6.8	7.6	8.4	9.2
t_{PD}	D(↓) to Q(↓)	4.5	0.19	5.3	6.0	6.8	7.5	8.3
t_{PD}	CDN(↓) to Q(↓)	2.9	0.19	3.7	4.4	5.2	5.9	6.7
t_{PD}	CDN(↑) to Q(↑)	3.27	0.205	4.1	4.9	5.7	6.5	7.4
t_S	D(0) setup G(↓)	4.05	0.000	4.0	4.0	4.0	4.0	4.0
t_S	D(1) setup G(↓)	4.66	0.000	4.7	4.7	4.7	4.7	4.7
t_H	D(0) hold G(↓)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold G(↓)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width G(1)	4.59	0.000	4.6	4.6	4.6	4.6	4.6
t_S	CDN(1) recovery G(↑)	2.86	0.000	2.9	2.9	2.9	2.9	2.9
t_H	CDN(0) hold G(↑)	1.63	0.000	1.6	1.6	1.6	1.6	1.6
t_W	pulse width CDN(0)	3.64	0.000	3.6	3.6	3.6	3.6	3.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

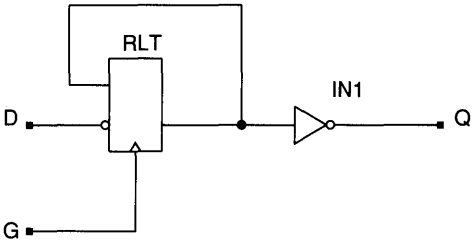
- D-Latch. Latch is transparent when G is asserted high and is latched when G is low.

- Hard Macrocell
- 3 Gate Equivalents
- 2 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs		Output
G	D	Q
1	?	D
0	?	Q

Pin Load

Pin	Std Load
G	0.6
D	0.4

Timing Parameters[1]

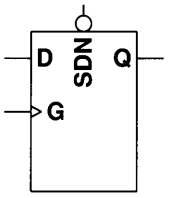
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	G(↑) to Q(↓) with D(0)	2.96	0.141	3.5	4.1	4.6	5.2	5.8
t_{PD}	G(↑) to Q(↑) with D(1)	3.29	0.207	4.1	4.9	5.8	6.6	7.4
t_{PD}	D(↑) to Q(↑)	3.36	0.207	4.2	5.0	5.8	6.7	7.5
t_{PD}	D(↓) to Q(↓)	3.07	0.19	3.8	4.6	5.3	6.1	6.9
t_S	D(0) setup G(↓)	2.54	0.000	2.5	2.5	2.5	2.5	2.5
t_S	D(1) setup G(↓)	2.82	0.000	2.8	2.8	2.8	2.8	2.8
t_H	D(0) hold G(↓)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_H	D(1) hold G(↓)	0	0.000	0.0	0.0	0.0	0.0	0.0
t_W	pulse width G(1)	2.74	0.000	2.7	2.7	2.7	2.7	2.7

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

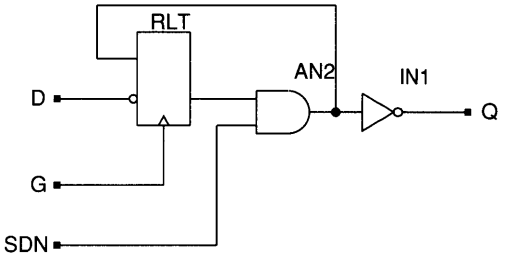
- D-Latch with set. Latch is transparent when G is asserted high and is latched when G is low.

- Hard Macrocell
- 4 Gate Equivalents
- 6 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs			Output
SDN	G	D	Q
0	?	?	1
1	1	?	D
1	0	?	Q

Pin Load

Pin	Std Load
G	0.6
D	0.4
SDN	1.0

Timing Parameters[1]

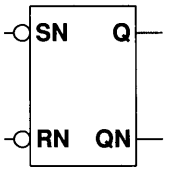
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	G(↑) to Q(↓) with D(0)	4.52	0.14	5.1	5.6	6.2	6.8	7.3
t_{PD}	G(↑) to Q(↑) with D(1)	4.61	0.205	5.4	6.3	7.1	7.9	8.7
t_{PD}	D(↑) to Q(↑)	4.67	0.205	5.5	6.3	7.1	8.0	8.8
t_{PD}	D(↓) to Q(↓)	4.63	0.19	5.4	6.1	6.9	7.7	8.4
t_{PD}	SDN(↓) to Q(↑)	2.31	0.29	3.5	4.6	5.8	6.9	8.1
t_{PD}	SDN(↑) to Q(↓)	2.66	0.14	3.2	3.8	4.3	4.9	5.5
t_S	D(0) setup G(↓) with SDN(1)	4.2	0.000	4.2	4.2	4.2	4.2	4.2
t_S	D(1) setup G(↓) with SDN(1)	4.25	0.000	4.2	4.2	4.2	4.2	4.2
t_W	pulse width G(1) with SDN(1)	4.18	0.000	4.2	4.2	4.2	4.2	4.2
t_S	SDN(1) recovery G(↓)	2.23	0.000	2.2	2.2	2.2	2.2	2.2
t_H	SDN(0) hold G(↓)	2.19	0.000	2.2	2.2	2.2	2.2	2.2
t_W	pulse width SDN(0)	4.12	0.000	4.1	4.1	4.1	4.1	4.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

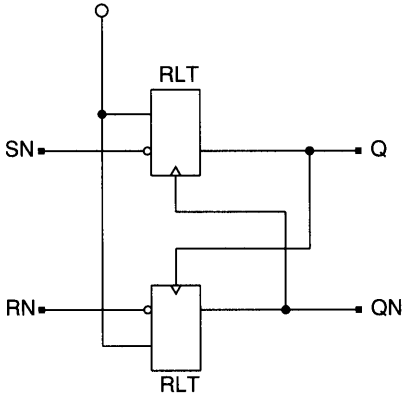
- SR Latch (cross-coupled NAND gates). Set (SN) and re-set (RN) are asserted low. Both Q and QN are high when both set and re-set are asserted. Note: If SN and RN are released at the same time the final state of the latch is not predictable.

- Hard Macrocell
- 4 Gate Equivalents
- 0 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs		Outputs	
SN	RN	Q	QN
0	?	1	$\overline{RN}$
?	0	$\overline{SN}$	1
1	1	Q	QN

Pin Load

Pin	Std Load
SN	0.4
RN	0.4

Timing Parameters[1]

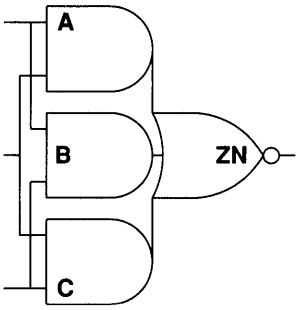
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	SN(↑) to Q(↓)	2.91	0.113	3.4	3.8	4.3	4.7	5.2
t_{PD}	RN(↑) to QN(↓)	2.91	0.113	3.4	3.8	4.3	4.7	5.2
t_{PD}	SN(↓) to Q(↑)	2.41	0.25	3.4	4.4	5.4	6.4	7.4
t_{PD}	RN(↓) to QN(↑)	2.41	0.25	3.4	4.4	5.4	6.4	7.4
t_{PD}	SN(↓) to Q(↑)	2.41	0.25	3.4	4.4	5.4	6.4	7.4
t_{PD}	Q(↑) to QN(↓) with RN(1)	2.73	0.113	3.2	3.6	4.1	4.5	5.0
t_{PD}	RN(↓) to QN(↑)	2.41	0.25	3.4	4.4	5.4	6.4	7.4
t_{PD}	QN(↑) to Q(↓) with SN(1)	2.73	0.113	3.2	3.6	4.1	4.5	5.0
t_W	pulse width SN(0) [use load on QN]	6.27	0.147	6.9	7.4	8.0	8.6	9.2
t_W	pulse width RN(0) [use load on Q]	6.27	0.147	6.9	7.4	8.0	8.6	9.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

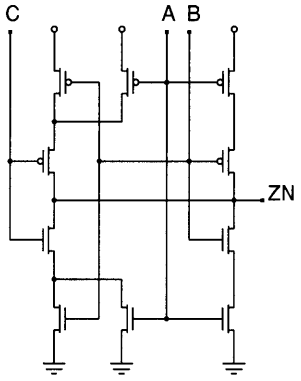
- Majority 2-of-3 "Voter", Inverting

- Hard Macrocell
- 3 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	ZN
0	0	?	1
0	?	0	1
?	0	0	1
1	1	?	0
1	?	1	0
?	1	1	0

Pin Load

Pin	Std Load
A	2.0
B	1.9
C	1.0

Timing Parameters[1]

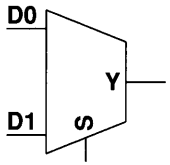
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓) with B(0) C(1)	1.64	0.154	2.3	2.9	3.5	4.1	4.7
t_{PD}	A(↓) to ZN(↑) with B(0) C(1)	1.3	0.434	3.0	4.8	6.5	8.2	10.0
t_{PD}	B(↑) to ZN(↓) with A(0) C(1)	1.37	0.209	2.2	3.0	3.9	4.7	5.5
t_{PD}	B(↓) to ZN(↑) with A(0) C(1)	1.44	0.439	3.2	4.9	6.7	8.5	10.2
t_{PD}	C(↑) to ZN(↓) with A(0) B(1)	1.47	0.217	2.3	3.2	4.1	4.9	5.8
t_{PD}	C(↓) to ZN(↑) with A(0) B(1)	1.16	0.436	2.9	4.7	6.4	8.1	9.9
t_{PD}	A(↑) to ZN(↓) with B(1) C(0)	1.55	0.156	2.2	2.8	3.4	4.0	4.7
t_{PD}	A(↓) to ZN(↑) with B(1) C(0)	1.18	0.435	2.9	4.7	6.4	8.1	9.9
t_{PD}	B(↑) to ZN(↓) with A(1) C(0)	1.64	0.165	2.3	3.0	3.6	4.3	4.9
t_{PD}	B(↓) to ZN(↑) with A(1) C(0)	0.88	0.527	3.0	5.1	7.2	9.3	11.4
t_{PD}	C(↑) to ZN(↓) with A(1) B(0)	1.44	0.165	2.1	2.8	3.4	4.1	4.7
t_{PD}	C(↓) to ZN(↑) with A(1) B(0)	0.913	0.527	3.0	5.1	7.2	9.3	11.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

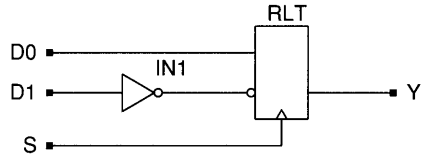
- 2 to 1 Mux, Non-inverting

- Hard Macrocell
- 4 Gate Equivalents
- 2 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs			Output
D1	D0	S	Y
?	?	0	D0
?	?	1	D1

Pin Load

Pin	Std Load
D0	0.5
D1	1.0
S	0.6

Timing Parameters[1]

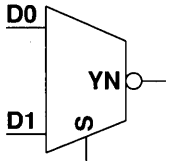
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	D0(↑) to Y(↑)	2.33	0.179	3.0	3.8	4.5	5.2	5.9
t_{PD}	D0(↓) to Y(↓)	2.37	0.147	3.0	3.5	4.1	4.7	5.3
t_{PD}	D1(↑) to Y(↑)	2.78	0.179	3.5	4.2	4.9	5.6	6.4
t_{PD}	D1(↓) to Y(↓)	3.24	0.147	3.8	4.4	5.0	5.6	6.2
t_{PD}	S(↑) to Y(↓) with D0(1) D1(0)	2.79	0.113	3.2	3.7	4.1	4.6	5.1
t_{PD}	S(↓) to Y(↑) with D0(1) D1(0)	2.4	0.25	3.4	4.4	5.4	6.4	7.4
t_{PD}	S(↑) to Y(↑) with D0(0) D1(1)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	S(↓) to Y(↓) with D0(0) D1(1)	2.28	0.147	2.9	3.5	4.0	4.6	5.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

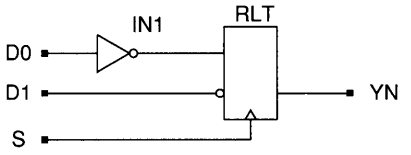
- 2 to 1 Mux, Inverting

- Hard Macrocell
- 3 Gate Equivalents
- 2 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs			Output
D1	D0	S	YN
?	?	0	$\overline{D0}$
?	?	1	$\overline{D1}$

Pin Load

Pin	Std Load
D0	1.0
D1	0.4
S	0.6

Timing Parameters[1]

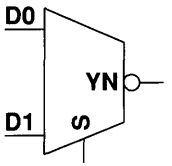
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	D0(↑) to YN(↓)	3.07	0.113	3.5	4.0	4.4	4.9	5.3
t_{PD}	D0(↓) to YN(↑)	2.82	0.25	3.8	4.8	5.8	6.8	7.8
t_{PD}	D1(↑) to YN(↓)	2.83	0.113	3.3	3.7	4.2	4.6	5.1
t_{PD}	D1(↓) to YN(↑)	2.3	0.25	3.3	4.3	5.3	6.3	7.3
t_{PD}	S(↑) to YN(↑) with D0(1) D1(0)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	S(↓) to YN(↓) with D0(1) D1(0)	2.28	0.147	2.9	3.5	4.0	4.6	5.2
t_{PD}	S(↑) to YN(↓) with D0(0) D1(1)	2.76	0.113	3.2	3.7	4.1	4.6	5.0
t_{PD}	S(↓) to YN(↑) with D0(0) D1(1)	2.41	0.25	3.4	4.4	5.4	6.4	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

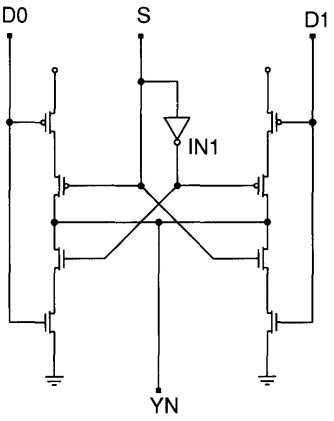
- 2 to 1 Mux, Inverting. Uses TPTs rather than RLTs.

- Hard Macrocell
- 3 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
D1	D0	S	YN
?	?	0	$\overline{D0}$
?	?	1	$\overline{D1}$

Pin Load

Pin	Std Load
D0	1.0
D1	1.0
S	1.8

Timing Parameters[1]

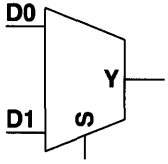
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	D0(↑) to YN(↓)	1.27	0.166	1.9	2.6	3.3	3.9	4.6
t_{PD}	D0(↓) to YN(↑)	0.912	0.433	2.6	4.4	6.1	7.8	9.6
t_{PD}	D1(↑) to YN(↓)	1.35	0.155	2.0	2.6	3.2	3.8	4.4
t_{PD}	D1(↓) to YN(↑)	0.944	0.433	2.7	4.4	6.1	7.9	9.6
t_{PD}	S(↑) to YN(↑) with D0(1) D1(0)	1.6	0.296	2.8	4.0	5.1	6.3	7.5
t_{PD}	S(↓) to YN(↓) with D0(1) D1(0)	1.73	0.218	2.6	3.5	4.3	5.2	6.1
t_{PD}	S(↑) to YN(↓) with D0(0) D1(1)	1.47	0.166	2.1	2.8	3.5	4.1	4.8
t_{PD}	S(↓) to YN(↑) with D0(0) D1(1)	1.18	0.436	2.9	4.7	6.4	8.2	9.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

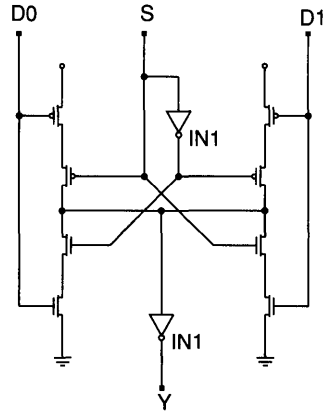
• 2 to 1 Mux, Non-inverting. Uses TPTs rather than RLTs.

- Hard Macrocell
- 4 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
D1	D0	S	Y
?	?	0	D0
?	?	1	D1

Pin Load

Pin	Std Load
D0	1.0
D1	1.0
S	2.0

Timing Parameters[1]

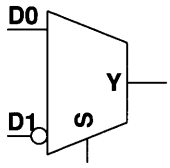
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	D0(↑) to Y(↑)	1.98	0.201	2.8	3.6	4.4	5.2	6.0
t_{PD}	D0(↓) to Y(↓)	2.16	0.185	2.9	3.6	4.4	5.1	5.9
t_{PD}	D1(↑) to Y(↑)	1.72	0.198	2.5	3.3	4.1	4.9	5.7
t_{PD}	D1(↓) to Y(↓)	2.06	0.189	2.8	3.6	4.3	5.1	5.8
t_{PD}	S(↑) to Y(↓) with D0(1) D1(0)	2.68	0.138	3.2	3.8	4.3	4.9	5.4
t_{PD}	S(↓) to Y(↑) with D0(1) D1(0)	2.52	0.286	3.7	4.8	6.0	7.1	8.2
t_{PD}	S(↑) to Y(↑) with D0(0) D1(1)	1.8	0.199	2.6	3.4	4.2	5.0	5.8
t_{PD}	S(↓) to Y(↓) with D0(0) D1(1)	2.35	0.188	3.1	3.9	4.6	5.4	6.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

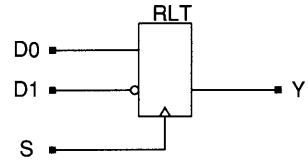
- 2 to 1 Mux, Inverting Input D1

- Hard Macrocell
- 4 Gate Equivalents
- 0 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs			Output
D1	D0	S	Y
?	?	0	D0
?	?	1	$\overline{D1}$

Pin Load

Pin	Std Load
D0	0.5
D1	0.4
S	0.6

Timing Parameters[1]

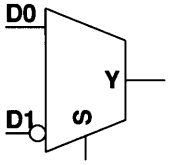
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	D1(↑) to Y(↓)	2.83	0.113	3.3	3.7	4.2	4.6	5.1
t_{PD}	D1(↓) to Y(↑)	2.3	0.25	3.3	4.3	5.3	6.3	7.3
t_{PD}	D0(↑) to Y(↑)	2.32	0.179	3.0	3.8	4.5	5.2	5.9
t_{PD}	D0(↓) to Y(↓)	2.37	0.147	3.0	3.5	4.1	4.7	5.3
t_{PD}	S(↑) to Y(↑) with D0(0) D1(0)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	S(↓) to Y(↓) with D0(0) D1(0)	2.28	0.147	2.9	3.5	4.0	4.6	5.2
t_{PD}	S(↑) to Y(↓) with D0(1) D1(1)	2.76	0.113	3.2	3.7	4.1	4.6	5.0
t_{PD}	S(↓) to Y(↑) with D0(1) D1(1)	2.41	0.25	3.4	4.4	5.4	6.4	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

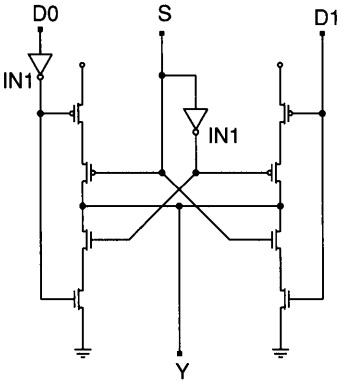
• 2 to 1 Mux, Inverting Input D1. Uses TPTs rather than RLTs.

- Hard Macrocell
- 4 Gate Equivalents
- 8 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
D1	D0	S	Y
?	?	0	D0
?	?	1	$\overline{D1}$

Pin Load

Pin	Std Load
D0	1.0
D1	1.0
S	1.9

Timing Parameters[1]

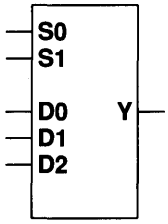
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	D1(↑) to Y(↓)	1.35	0.155	2.0	2.6	3.2	3.8	4.4
t_{PD}	D1(↓) to Y(↑)	0.929	0.433	2.7	4.4	6.1	7.9	9.6
t_{PD}	D0(↑) to Y(↑)	1.95	0.301	3.2	4.4	5.6	6.8	8.0
t_{PD}	D0(↓) to Y(↓)	1.66	0.229	2.6	3.5	4.4	5.3	6.2
t_{PD}	S(↑) to Y(↑) with D0(0) D1(0)	1.92	0.299	3.1	4.3	5.5	6.7	7.9
t_{PD}	S(↓) to Y(↓) with D0(0) D1(0)	1.75	0.227	2.7	3.6	4.5	5.4	6.3
t_{PD}	S(↑) to Y(↓) with D0(1) D1(1)	1.43	0.166	2.1	2.8	3.4	4.1	4.8
t_{PD}	S(↓) to Y(↑) with D0(1) D1(1)	1.01	0.436	2.8	4.5	6.2	8.0	9.7

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

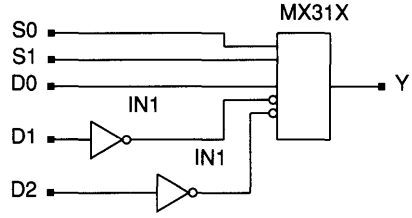
- 3 to 1 Mux, Non-inverting

- Soft Macrocell
- 8 Gate Equivalents
- 4 TPTs
- 2 RLTs

Symbol



Schematic



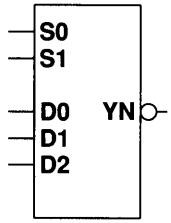
Function Table

Inputs					Output
D2	D1	D0	S1	S0	Y
?	?	?	0	0	D0
?	?	?	0	1	D1
?	?	?	1	?	D2

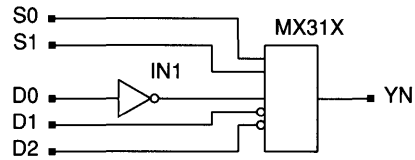
- 3 to 1 Mux, Inverting

- Soft Macrocell
- 7 Gate Equivalents
- 2 TPTs
- 2 RLTs

Symbol



Schematic



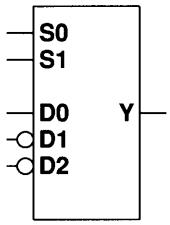
Function Table

Inputs					Output
D2	D1	D0	S1	S0	YN
?	?	?	0	0	$\overline{D0}$
?	?	?	0	1	$\overline{D1}$
?	?	?	1	?	$\overline{D2}$

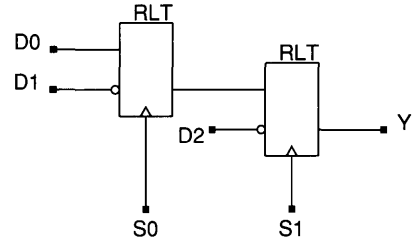
- 3 to 1 Mux, Inverting D1, D2 Inputs

- Hard Macrocell
- 6 Gate Equivalents
- 0 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs					Output
D2	D1	D0	S1	S0	Y
?	?	?	0	0	D0
?	?	?	0	1	$\overline{D1}$
?	?	?	1	?	$\overline{D2}$

Pin Load

Pin	Std Load
D0	0.5
D1	0.4
D2	0.4
S0	0.6
S1	0.6

Timing Parameters[1]

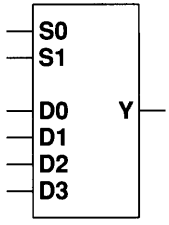
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	D0(↑) to Y(↑)	4.28	0.179	5.0	5.7	6.4	7.1	7.9
t_{PD}	D0(↓) to Y(↓)	4.51	0.147	5.1	5.7	6.3	6.9	7.5
t_{PD}	D1(↑) to Y(↓)	4.97	0.113	5.4	5.9	6.3	6.8	7.2
t_{PD}	D1(↓) to Y(↑)	4.26	0.25	5.3	6.3	7.3	8.3	9.3
t_{PD}	D2(↑) to Y(↓)	2.83	0.113	3.3	3.7	4.2	4.6	5.1
t_{PD}	D2(↓) to Y(↑)	2.3	0.25	3.3	4.3	5.3	6.3	7.3
t_{PD}	S0(↑) to Y(↑) with D0(0) D1(0)	4.17	0.179	4.9	5.6	6.3	7.0	7.8
t_{PD}	S0(↓) to Y(↓) with D0(0) D1(0)	4.42	0.147	5.0	5.6	6.2	6.8	7.4
t_{PD}	S0(↑) to Y(↓) with D0(1) D1(1)	4.9	0.113	5.4	5.8	6.3	6.7	7.2
t_{PD}	S0(↓) to Y(↑) with D0(1) D1(1)	4.38	0.25	5.4	6.4	7.4	8.4	9.4
t_{PD}	S1(↑) to Y(↑) with D0(0) D1(0) D2(0) S0(0)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	S1(↓) to Y(↓) with D0(0) D1(0) D2(0) S0(0)	2.28	0.147	2.9	3.5	4.0	4.6	5.2
t_{PD}	S1(↑) to Y(↓) with D0(1) D1(0) D2(1) S0(0)	2.76	0.113	3.2	3.7	4.1	4.6	5.0
t_{PD}	S1(↓) to Y(↑) with D0(1) D1(0) D2(1) S0(0)	2.41	0.25	3.4	4.4	5.4	6.4	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

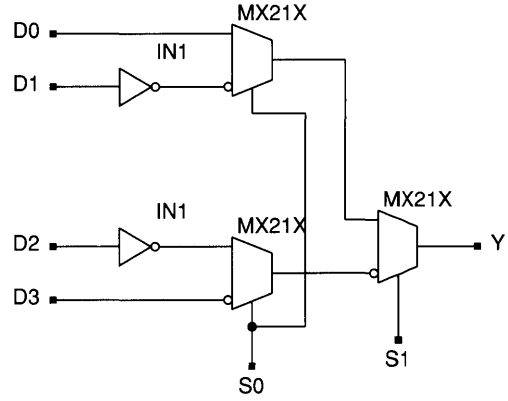
- 4 to 1 Mux, Non-inverting

- Soft Macrocell
- 14 Gate Equivalents
- 4 TPTs
- 3 RLTs

Symbol



Schematic



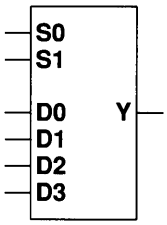
Function Table

Inputs						Output
D3	D2	D1	D0	S1	S0	Y
?	?	?	?	0	0	D0
?	?	?	?	0	1	D1
?	?	?	?	1	0	D2
?	?	?	?	1	1	D3

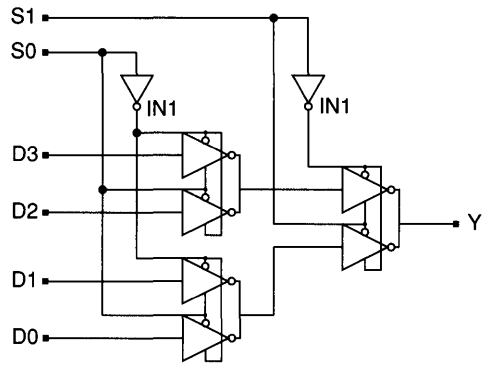
- Non-inverting 4 to 1 Multiplexer, TPT Implementation

- Hard Macrocell
- 6 Gate Equivalents
- 16 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
D3	D2	D1	D0	S1	S0	Y
?	?	?	?	0	0	D0
?	?	?	?	0	1	D1
?	?	?	?	1	0	D2
?	?	?	?	1	1	D3

Pin Load

Pin	Std Load
D0	1.0
D1	1.0
D2	1.0
D3	1.0
S1	1.9
S0	2.9

Timing Parameters[1]

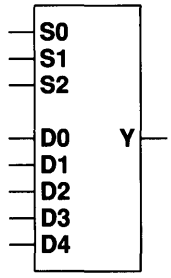
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_P	D0(↑) to Y(↑)	2.35	0.301	3.6	4.8	6.0	7.2	8.4
t_P	D0(↓) to Y(↓)	2.26	0.229	3.2	4.1	5.0	5.9	6.8
t_P	D1(↑) to Y(↑)	2.38	0.301	3.6	4.8	6.0	7.2	8.4
t_P	D1(↓) to Y(↓)	2.27	0.23	3.2	4.1	5.0	6.0	6.9
t_P	D2(↑) to Y(↑)	2.97	0.302	4.2	5.4	6.6	7.8	9.0
t_P	D2(↓) to Y(↓)	2.31	0.207	3.1	4.0	4.8	5.6	6.5
t_P	D3(↑) to Y(↑)	2.35	0.301	3.6	4.8	6.0	7.2	8.4
t_P	D3(↓) to Y(↓)	2.32	0.209	3.2	4.0	4.8	5.7	6.5
t_P	S0(↑) to Y(↓) with S1(0)	3.39	0.167	4.1	4.7	5.4	6.1	6.7
t_P	S0(↓) to Y(↑) with S1(0)	3.21	0.44	5.0	6.7	8.5	10.3	12.0
t_P	S0(↑) to Y(↑) with S1(0)	2.39	0.301	3.6	4.8	6.0	7.2	8.4
t_P	S0(↓) to Y(↓) with S1(0)	2.28	0.23	3.2	4.1	5.0	6.0	6.9
t_P	S0(↑) to Y(↓) with S1(1)	3.47	0.152	4.1	4.7	5.3	5.9	6.5
t_P	S0(↓) to Y(↑) with S1(1)	3.11	0.44	4.9	6.6	8.4	10.2	11.9
t_P	S0(↑) to Y(↑) with S1(1)	2.57	0.301	3.8	5.0	6.2	7.4	8.6
t_P	S0(↓) to Y(↓) with S1(1)	2.39	0.208	3.2	4.1	4.9	5.7	6.5
t_P	S1(↑) to Y(↓)	1.53	0.171	2.2	2.9	3.6	4.3	4.9
t_P	S1(↓) to Y(↑)	1.09	0.434	2.8	4.6	6.3	8.0	9.8
t_P	S1(↑) to Y(↑)	1.91	0.299	3.1	4.3	5.5	6.7	7.9
t_P	S1(↓) to Y(↓)	1.64	0.226	2.5	3.5	4.4	5.3	6.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, "bin-1" parts.
2 Sum pin load and wire load to get total load.

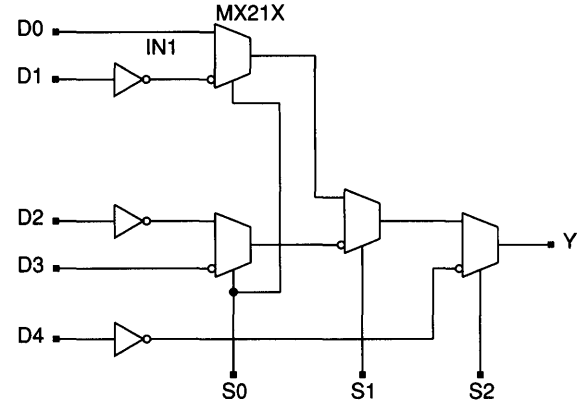
- 5 to 1 Mux, Non-inverting

- Soft Macrocell
- 19 Gate Equivalents
- 6 TPTs
- 4 RLTs

Symbol



Schematic



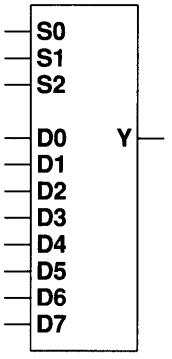
Function Table

Inputs								Output
D4	D3	D2	D1	D0	S2	S1	S0	Y
?	?	?	?	?	0	0	0	D0
?	?	?	?	?	0	0	1	D1
?	?	?	?	?	0	1	0	D2
?	?	?	?	?	0	1	1	D3
?	?	?	?	?	1	?	?	D4

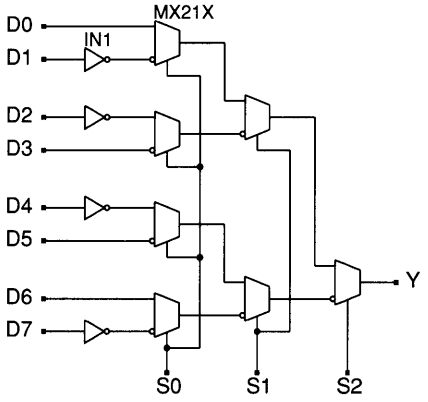
- 8 to 1 Mux, Non-inverting

- Soft Macrocell
- 32 Gate Equivalents
- 8 TPTs
- 7 RLTs

Symbol



Schematic



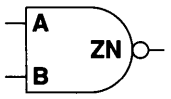
Function Table

Inputs											Output
D7	D6	D5	D4	D3	D2	D1	D0	S2	S1	S0	Y
?	?	?	?	?	?	?	?	0	0	0	D0
?	?	?	?	?	?	?	?	0	0	1	D1
?	?	?	?	?	?	?	?	0	1	0	D2
?	?	?	?	?	?	?	?	0	1	1	D3
?	?	?	?	?	?	?	?	1	0	0	D4
?	?	?	?	?	?	?	?	1	0	1	D5
?	?	?	?	?	?	?	?	1	1	0	D6
?	?	?	?	?	?	?	?	1	1	1	D7

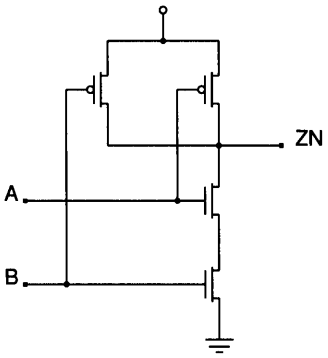
- 2-Input NAND

- Hard Macrocell
- 1 Gate Equivalents
- 3 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	ZN
0	?	1
?	0	1
1	1	0

Pin Load

Pin	Std Load
A	1.0
B	1.0

Timing Parameters[1]

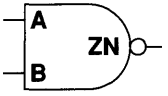
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.18	0.166	1.8	2.5	3.2	3.8	4.5
t_{PD}	A(↓) to ZN(↑)	0.968	0.29	2.1	3.3	4.4	5.6	6.8
t_{PD}	B(↑) to ZN(↓)	1.22	0.155	1.8	2.5	3.1	3.7	4.3
t_{PD}	B(↓) to ZN(↑)	1.04	0.289	2.2	3.4	4.5	5.7	6.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

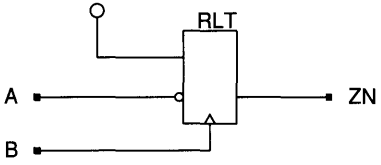
- 2-Input NAND using an RLT

- Hard Macrocell
- 1 Gate Equivalents
- 0 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	ZN
0	?	1
?	0	1
1	1	0

Pin Load

Pin	Std Load
A	0.4
B	0.5

Timing Parameters[1]

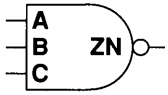
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	2.83	0.113	3.3	3.7	4.2	4.6	5.1
t_{PD}	A(↓) to ZN(↑)	2.3	0.25	3.3	4.3	5.3	6.3	7.3
t_{PD}	B(↑) to ZN(↓)	2.76	0.113	3.2	3.7	4.1	4.6	5.0
t_{PD}	B(↓) to ZN(↑)	2.41	0.25	3.4	4.4	5.4	6.4	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

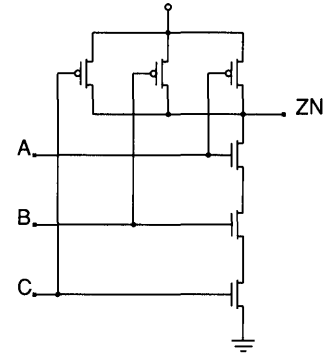
- 3-Input NAND

- Hard Macrocell
- 2 Gate Equivalents
- 4 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	ZN
0	?	?	1
?	0	?	1
?	?	0	1
1	1	1	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0

Timing Parameters[1]

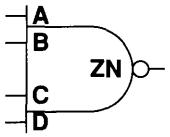
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.19	0.185	1.9	2.7	3.4	4.1	4.9
t_{PD}	A(↓) to ZN(↑)	1.05	0.29	2.2	3.4	4.5	5.7	6.8
t_{PD}	B(↑) to ZN(↓)	1.28	0.175	2.0	2.7	3.4	4.1	4.8
t_{PD}	B(↓) to ZN(↑)	1.13	0.29	2.3	3.4	4.6	5.8	6.9
t_{PD}	C(↑) to ZN(↓)	1.3	0.167	2.0	2.6	3.3	4.0	4.6
t_{PD}	C(↓) to ZN(↑)	1.2	0.29	2.4	3.5	4.7	5.8	7.0

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

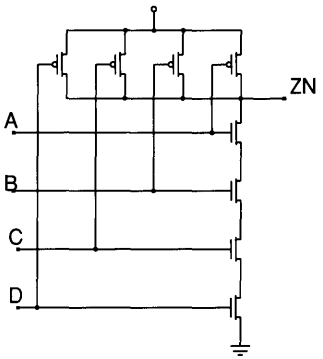
- 4-Input NAND

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A	B	C	D	ZN
0	?	?	?	1
?	0	?	?	1
?	?	0	?	1
?	?	?	0	1
1	1	1	1	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

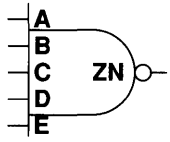
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.27	0.202	2.1	2.9	3.7	4.5	5.3
t_{PD}	A(↓) to ZN(↑)	1.19	0.29	2.3	3.5	4.7	5.8	7.0
t_{PD}	B(↑) to ZN(↓)	1.38	0.192	2.1	2.9	3.7	4.5	5.2
t_{PD}	B(↓) to ZN(↑)	1.29	0.289	2.4	3.6	4.8	5.9	7.1
t_{PD}	C(↑) to ZN(↓)	1.45	0.185	2.2	2.9	3.7	4.4	5.1
t_{PD}	C(↓) to ZN(↑)	1.37	0.289	2.5	3.7	4.8	6.0	7.2
t_{PD}	D(↑) to ZN(↓)	1.46	0.18	2.2	2.9	3.6	4.3	5.1
t_{PD}	D(↓) to ZN(↑)	1.42	0.29	2.6	3.7	4.9	6.1	7.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

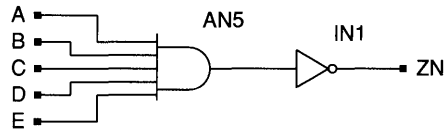
- 5-Input NAND

- Hard Macrocell
- 4 Gate Equivalents
- 10 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A	B	C	D	E	ZN
0	?	?	?	?	1
?	0	?	?	?	1
?	?	0	?	?	1
?	?	?	0	?	1
?	?	?	?	0	1
1	1	1	1	1	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Timing Parameters[1]

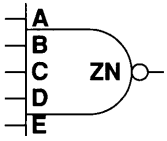
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	3.07	0.138	3.6	4.2	4.7	5.3	5.8
t_{PD}	A(↓) to ZN(↑)	2.36	0.286	3.5	4.7	5.8	6.9	8.1
t_{PD}	B(↑) to ZN(↓)	3.19	0.138	3.7	4.3	4.8	5.4	5.9
t_{PD}	B(↓) to ZN(↑)	2.49	0.286	3.6	4.8	5.9	7.1	8.2
t_{PD}	C(↑) to ZN(↓)	3.26	0.138	3.8	4.4	4.9	5.5	6.0
t_{PD}	C(↓) to ZN(↑)	2.58	0.286	3.7	4.9	6.0	7.2	8.3
t_{PD}	D(↑) to ZN(↓)	2.87	0.138	3.4	4.0	4.5	5.1	5.6
t_{PD}	D(↓) to ZN(↑)	2.09	0.283	3.2	4.4	5.5	6.6	7.8
t_{PD}	E(↑) to ZN(↓)	2.97	0.138	3.5	4.1	4.6	5.2	5.7
t_{PD}	E(↓) to ZN(↑)	2.22	0.283	3.4	4.5	5.6	6.7	7.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

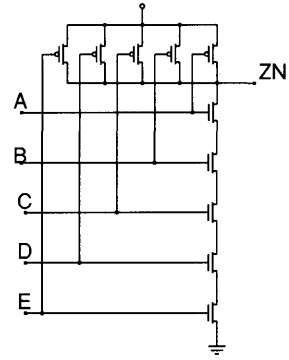
- Low drive, minimum area 5-input NAND

- Hard Macrocell
- 3 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A	B	C	D	E	ZN
0	?	?	?	?	1
?	0	?	?	?	1
?	?	0	?	?	1
?	?	?	0	?	1
?	?	?	?	0	1
1	1	1	1	1	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Timing Parameters[1]

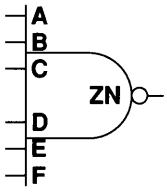
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.26	0.221	2.1	3.0	3.9	4.8	5.7
t_{PD}	A(↓) to ZN(↑)	1.26	0.29	2.4	3.6	4.7	5.9	7.1
t_{PD}	B(↑) to ZN(↓)	1.41	0.211	2.3	3.1	3.9	4.8	5.6
t_{PD}	B(↓) to ZN(↑)	1.36	0.289	2.5	3.7	4.8	6.0	7.1
t_{PD}	C(↑) to ZN(↓)	1.5	0.204	2.3	3.1	3.9	4.8	5.6
t_{PD}	C(↓) to ZN(↑)	1.45	0.289	2.6	3.8	4.9	6.1	7.2
t_{PD}	D(↑) to ZN(↓)	1.56	0.199	2.4	3.2	3.9	4.7	5.5
t_{PD}	D(↓) to ZN(↑)	1.52	0.289	2.7	3.8	5.0	6.2	7.3
t_{PD}	E(↑) to ZN(↓)	1.58	0.196	2.4	3.1	3.9	4.7	5.5
t_{PD}	E(↓) to ZN(↑)	1.57	0.29	2.7	3.9	5.1	6.2	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

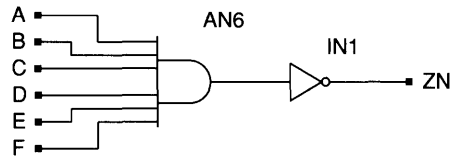
- 6-Input NAND

- Hard Macrocell
- 5 Gate Equivalents
- 11 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A	B	C	D	E	F	ZN
0	?	?	?	?	?	1
?	0	?	?	?	?	1
?	?	0	?	?	?	1
?	?	?	0	?	?	1
?	?	?	?	0	?	1
?	?	?	?	?	0	1
1	1	1	1	1	1	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Timing Parameters[1]

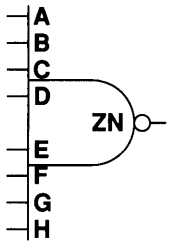
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	3.06	0.138	3.6	4.2	4.7	5.3	5.8
t_{PD}	A(↓) to ZN(↑)	2.36	0.286	3.5	4.7	5.8	6.9	8.1
t_{PD}	B(↑) to ZN(↓)	3.19	0.138	3.7	4.3	4.8	5.4	5.9
t_{PD}	B(↓) to ZN(↑)	2.49	0.286	3.6	4.8	5.9	7.1	8.2
t_{PD}	C(↑) to ZN(↓)	3.25	0.138	3.8	4.4	4.9	5.5	6.0
t_{PD}	C(↓) to ZN(↑)	2.58	0.286	3.7	4.9	6.0	7.2	8.3
t_{PD}	D(↑) to ZN(↓)	3.11	0.138	3.7	4.2	4.8	5.3	5.9
t_{PD}	D(↓) to ZN(↑)	2.24	0.283	3.4	4.5	5.6	6.8	7.9
t_{PD}	E(↑) to ZN(↓)	3.23	0.138	3.8	4.3	4.9	5.4	6.0
t_{PD}	E(↓) to ZN(↑)	2.38	0.283	3.5	4.6	5.8	6.9	8.0
t_{PD}	F(↑) to ZN(↓)	3.3	0.138	3.9	4.4	5.0	5.5	6.1
t_{PD}	F(↓) to ZN(↑)	2.48	0.282	3.6	4.7	5.9	7.0	8.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

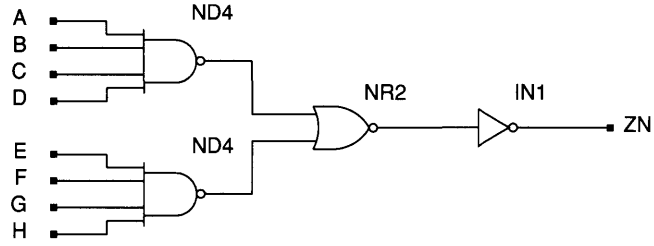
- 8-Input NAND

- Soft Macrocell
- 6 Gate Equivalents
- 15 TPTs
- 0 RLTs

Symbol



Schematic



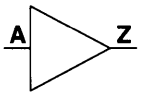
Function Table

Inputs								Output
A	B	C	D	E	F	G	H	ZN
0	?	?	?	?	?	?	?	1
?	0	?	?	?	?	?	?	1
?	?	0	?	?	?	?	?	1
?	?	?	0	?	?	?	?	1
?	?	?	?	0	?	?	?	1
?	?	?	?	?	0	?	?	1
?	?	?	?	?	?	0	?	1
?	?	?	?	?	?	?	0	1
1	1	1	1	1	1	1	1	0

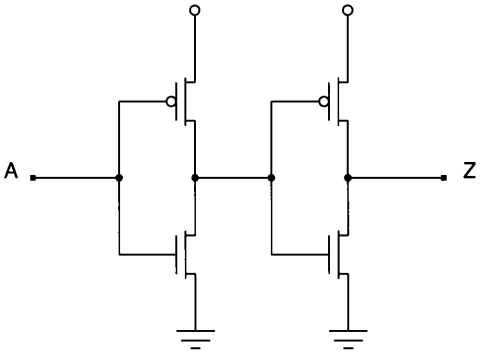
- Non-inverting buffer, 1X Drive

- Hard Macrocell
- 1 Gate Equivalents
- 3 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	Z
?	A

Pin Load

Pin	Std Load
A	1.0

Timing Parameters[1]

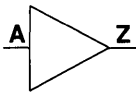
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.29	0.198	2.1	2.9	3.7	4.5	5.3
t_{PD}	A(↓) to Z(↓)	1.4	0.181	2.1	2.8	3.6	4.3	5.0

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

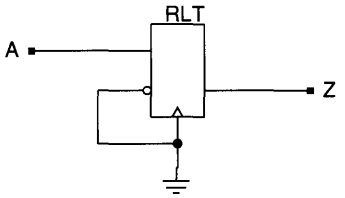
- Non-inverting buffer using an RLT

- Hard Macrocell
- 1 Gate Equivalents
- 0 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Input	Output
A	Z
?	A

Pin Load

Pin	Std Load
A	0.5

Timing Parameters[1]

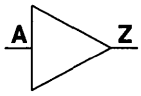
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.28	0.179	3.0	3.7	4.4	5.1	5.9
t_{PD}	A(↓) to Z(↓)	2.26	0.147	2.8	3.4	4.0	4.6	5.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

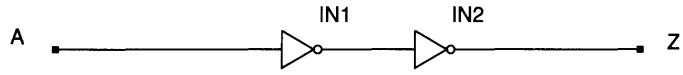
- Non-inverting buffer, 2X Drive

- Hard Macrocell
- 1 Gate Equivalents
- 4 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	Z
?	A

Pin Load

Pin	Std Load
A	1.0

Timing Parameters[1]

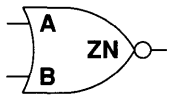
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.54	0.131	2.1	2.6	3.1	3.6	4.2
t_{PD}	A(↓) to Z(↓)	1.55	0.13	2.1	2.6	3.1	3.6	4.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

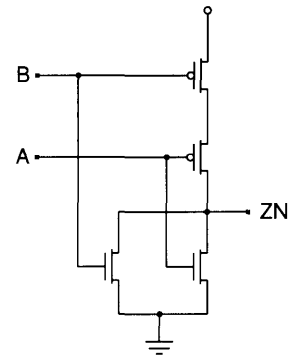
- 2-Input NOR

- Hard Macrocell
- 1 Gate Equivalents
- 3 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	ZN
1	?	0
?	1	0
0	0	1

Pin Load

Pin	Std Load
A	1.0
B	1.0

Timing Parameters[1]

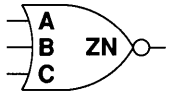
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.34	0.15	1.9	2.5	3.1	3.7	4.3
t_{PD}	A(↓) to ZN(↑)	0.985	0.444	2.8	4.5	6.3	8.1	9.9
t_{PD}	B(↑) to ZN(↓)	1.35	0.158	2.0	2.6	3.2	3.9	4.5
t_{PD}	B(↓) to ZN(↑)	0.921	0.442	2.7	4.5	6.2	8.0	9.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

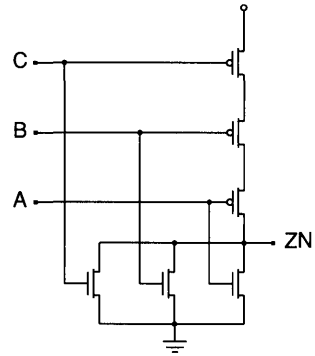
- 3-Input NOR

- Hard Macrocell
- 2 Gate Equivalents
- 4 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	ZN
1	?	?	0
?	1	?	0
?	?	1	0
0	0	0	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0

Timing Parameters[1]

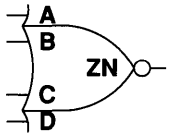
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.44	0.15	2.0	2.6	3.2	3.8	4.4
t_{PD}	A(↓) to ZN(↑)	1.04	0.595	3.4	5.8	8.2	10.6	12.9
t_{PD}	B(↑) to ZN(↓)	1.45	0.166	2.1	2.8	3.4	4.1	4.8
t_{PD}	B(↓) to ZN(↑)	1	0.595	3.4	5.8	8.1	10.5	12.9
t_{PD}	C(↑) to ZN(↓)	1.5	0.166	2.2	2.8	3.5	4.2	4.8
t_{PD}	C(↓) to ZN(↑)	1.03	0.595	3.4	5.8	8.2	10.6	12.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

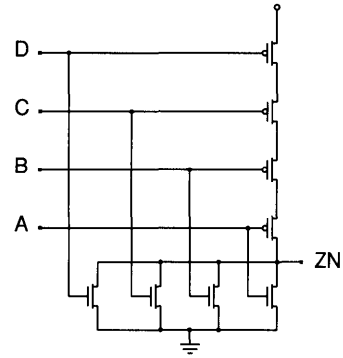
- 4-Input NOR

- Hard Macrocell
- 2 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A	B	C	D	ZN
1	?	?	?	0
?	1	?	?	0
?	?	1	?	0
?	?	?	1	0
0	0	0	0	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

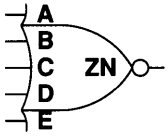
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	1.45	0.166	2.1	2.8	3.4	4.1	4.8
t_{PD}	A(↓) to ZN(↑)	1.24	0.761	4.3	7.3	10.4	13.4	16.5
t_{PD}	B(↑) to ZN(↓)	1.54	0.166	2.2	2.9	3.5	4.2	4.9
t_{PD}	B(↓) to ZN(↑)	1.29	0.761	4.3	7.4	10.4	13.5	16.5
t_{PD}	C(↑) to ZN(↓)	1.63	0.15	2.2	2.8	3.4	4.0	4.6
t_{PD}	C(↓) to ZN(↑)	1.34	0.766	4.4	7.5	10.5	13.6	16.7
t_{PD}	D(↑) to ZN(↓)	1.66	0.15	2.3	2.9	3.5	4.1	4.7
t_{PD}	D(↓) to ZN(↑)	1.37	0.766	4.4	7.5	10.6	13.6	16.7

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

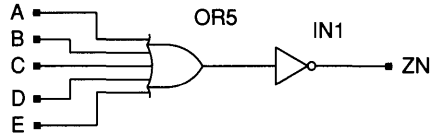
- 5-Input NOR

- Hard Macrocell
- 4 Gate Equivalents
- 10 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A	B	C	D	E	ZN
1	?	?	?	?	0
?	1	?	?	?	0
?	?	1	?	?	0
?	?	?	1	?	0
?	?	?	?	1	0
0	0	0	0	0	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Timing Parameters[1]

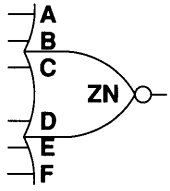
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	2.63	0.135	3.2	3.7	4.3	4.8	5.3
t_{PD}	A(↓) to ZN(↑)	2.97	0.282	4.1	5.2	6.4	7.5	8.6
t_{PD}	B(↑) to ZN(↓)	2.71	0.135	3.3	3.8	4.3	4.9	5.4
t_{PD}	B(↓) to ZN(↑)	3.03	0.282	4.2	5.3	6.4	7.5	8.7
t_{PD}	C(↑) to ZN(↓)	2.75	0.135	3.3	3.8	4.4	4.9	5.5
t_{PD}	C(↓) to ZN(↑)	3.07	0.282	4.2	5.3	6.5	7.6	8.7
t_{PD}	D(↑) to ZN(↓)	2.51	0.135	3.1	3.6	4.1	4.7	5.2
t_{PD}	D(↓) to ZN(↑)	2.45	0.283	3.6	4.7	5.8	7.0	8.1
t_{PD}	E(↑) to ZN(↓)	2.57	0.135	3.1	3.7	4.2	4.7	5.3
t_{PD}	E(↓) to ZN(↑)	2.47	0.283	3.6	4.7	5.9	7.0	8.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

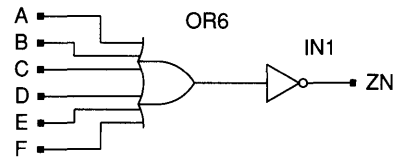
- 6-Input NOR

- Hard Macrocell
- 5 Gate Equivalents
- 11 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A	B	C	D	E	F	ZN
1	?	?	?	?	?	0
?	1	?	?	?	?	0
?	?	1	?	?	?	0
?	?	?	1	?	?	0
?	?	?	?	1	?	0
?	?	?	?	?	1	0
0	0	0	0	0	0	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Timing Parameters[1]

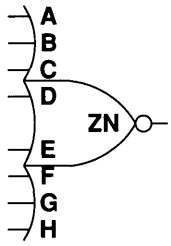
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓)	2.63	0.135	3.2	3.7	4.3	4.8	5.3
t_{PD}	A(↓) to ZN(↑)	2.96	0.282	4.1	5.2	6.3	7.5	8.6
t_{PD}	B(↑) to ZN(↓)	2.71	0.135	3.3	3.8	4.3	4.9	5.4
t_{PD}	B(↓) to ZN(↑)	3.03	0.282	4.2	5.3	6.4	7.5	8.7
t_{PD}	C(↑) to ZN(↓)	2.75	0.135	3.3	3.8	4.4	4.9	5.5
t_{PD}	C(↓) to ZN(↑)	3.07	0.282	4.2	5.3	6.5	7.6	8.7
t_{PD}	D(↑) to ZN(↓)	2.7	0.135	3.2	3.8	4.3	4.9	5.4
t_{PD}	D(↓) to ZN(↑)	2.9	0.282	4.0	5.2	6.3	7.4	8.5
t_{PD}	E(↑) to ZN(↓)	2.79	0.135	3.3	3.9	4.4	5.0	5.5
t_{PD}	E(↓) to ZN(↑)	2.97	0.282	4.1	5.2	6.3	7.5	8.6
t_{PD}	F(↑) to ZN(↓)	2.83	0.135	3.4	3.9	4.5	5.0	5.5
t_{PD}	F(↓) to ZN(↑)	3.01	0.282	4.1	5.3	6.4	7.5	8.6

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

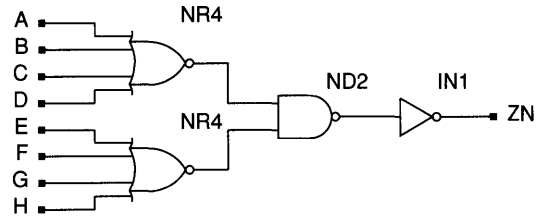
- 8-Input NOR

- Soft Macrocell
- 6 Gate Equivalents
- 17 TPTs
- 0 RLTs

Symbol



Schematic



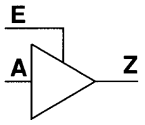
Function Table

Inputs								Output
A	B	C	D	E	F	G	H	ZN
1	?	?	?	?	?	?	?	0
?	1	?	?	?	?	?	?	0
?	?	1	?	?	?	?	?	0
?	?	?	1	?	?	?	?	0
?	?	?	?	1	?	?	?	0
?	?	?	?	?	1	?	?	0
?	?	?	?	?	?	1	?	0
?	?	?	?	?	?	?	1	0
0	0	0	0	0	0	0	0	1

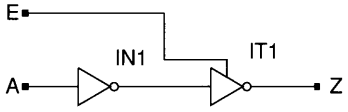
- Non-inverting three-state buffer, 1X drive. Enable is active high. Macro must be used in conjunction with a three-state bus receiver macro (see NZ1.)

- Hard Macrocell
- 1 Gate Equivalents
- 3 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	E	Z
?	0	*Z*
?	1	A

Pin Load

Pin	Std Load
A	1.0
E	0.5

Timing Parameters[1]

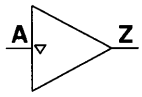
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)							
t_{PD}	A(↓) to Z(↓)							

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

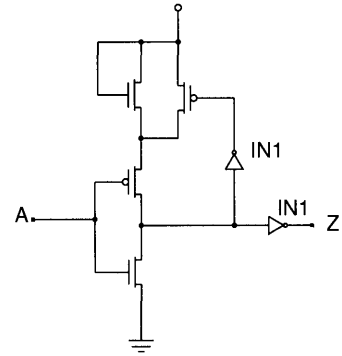
- Non-inverting three-state bus receiver. Note: A bus receiver cell must be used in conjunction with a three-state bus driver.

- Hard Macrocell
- 1 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Input	Output
A	Z
?	A

Pin Load

Pin	Std Load
A	1.0

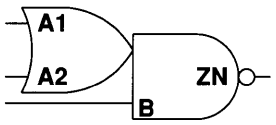
Timing Parameters

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)							
t_{PD}	A(↓) to Z(↓)							

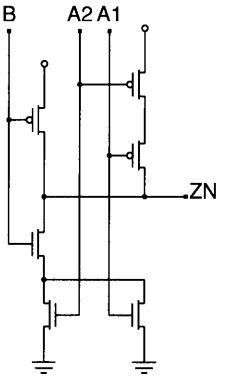
- 2-OR into 2-NAND

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A1	A2	B	ZN
1	?	1	0
?	1	1	0
0	0	?	1
?	?	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B	1.0

Timing Parameters[1]

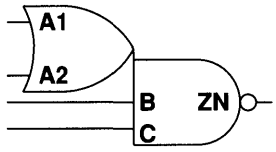
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.51	0.153	2.1	2.7	3.3	4.0	4.6
t_{PD}	A1(↓) to ZN(↑)	1.28	0.436	3.0	4.8	6.5	8.3	10.0
t_{PD}	A2(↑) to ZN(↓)	1.42	0.189	2.2	2.9	3.7	4.4	5.2
t_{PD}	A2(↓) to ZN(↑)	1.21	0.436	3.0	4.7	6.4	8.2	9.9
t_{PD}	B(↑) to ZN(↓) with A1(0) A2(1)	1.25	0.218	2.1	3.0	3.9	4.7	5.6
t_{PD}	B(↓) to ZN(↑) with A1(0) A2(1)	1.13	0.291	2.3	3.5	4.6	5.8	6.9

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

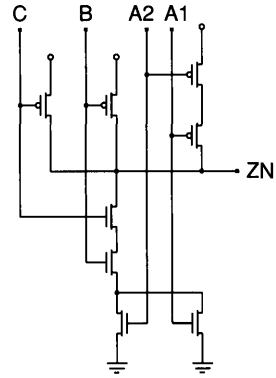
- 2-OR into 3-NAND

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A1	A2	B	C	ZN
1	?	1	1	0
?	1	1	1	0
0	0	?	?	1
?	?	0	?	1
?	?	?	0	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B	1.0
C	1.0

Timing Parameters[1]

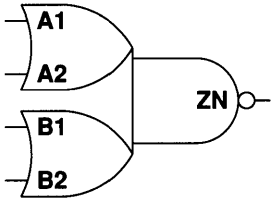
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓)	1.66	0.165	2.3	3.0	3.6	4.3	5.0
t_{PD}	A1(↓) to ZN(↑)	1.61	0.438	3.4	5.1	6.9	8.6	10.4
t_{PD}	A2(↑) to ZN(↓)	1.62	0.206	2.4	3.3	4.1	4.9	5.7
t_{PD}	A2(↓) to ZN(↑)	1.56	0.437	3.3	5.1	6.8	8.6	10.3
t_{PD}	B(↑) to ZN(↓) with A1(0) A2(1)	1.48	0.226	2.4	3.3	4.2	5.1	6.0
t_{PD}	B(↓) to ZN(↑) with A1(0) A2(1)	1.38	0.29	2.5	3.7	4.9	6.0	7.2
t_{PD}	C(↑) to ZN(↓) with A1(0) A2(1)	1.31	0.237	2.3	3.2	4.2	5.1	6.0
t_{PD}	C(↓) to ZN(↑) with A1(0) A2(1)	1.24	0.291	2.4	3.6	4.7	5.9	7.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

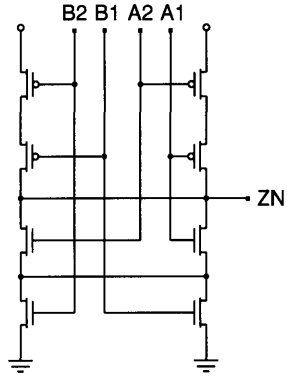
- Two 2-ORs into 2-NAND

- Hard Macrocell
- 2 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A1	A2	B1	B2	ZN
1	?	1	?	0
?	1	1	?	0
1	?	?	1	0
?	1	?	1	0
?	?	0	0	1
0	0	?	?	1

Pin Load

Pin	Std Load
A1	1.0
A2	1.0
B1	1.0
B2	1.7

Timing Parameters[1]

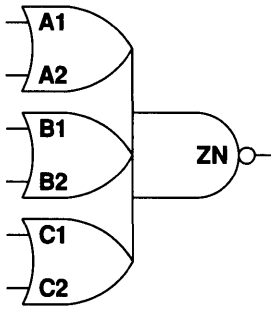
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A1(↑) to ZN(↓) with B1(0) B2(1)	1.45	0.217	2.3	3.2	4.1	4.9	5.8
t_{PD}	A1(↓) to ZN(↑) with B1(0) B2(1)	1.1	0.437	2.8	4.6	6.3	8.1	9.8
t_{PD}	A2(↑) to ZN(↓) with B1(0) B2(1)	1.39	0.165	2.0	2.7	3.4	4.0	4.7
t_{PD}	A2(↓) to ZN(↑) with B1(0) B2(1)	0.888	0.433	2.6	4.4	6.1	7.8	9.6
t_{PD}	B1(↑) to ZN(↓) with A1(0) A2(1)	1.53	0.19	2.3	3.0	3.8	4.6	5.3
t_{PD}	B1(↓) to ZN(↑) with A1(0) A2(1)	1.43	0.439	3.2	4.9	6.7	8.4	10.2
t_{PD}	B2(↑) to ZN(↓) with A1(0) A2(1)	1.7	0.154	2.3	2.9	3.5	4.2	4.8
t_{PD}	B2(↓) to ZN(↑) with A1(0) A2(1)	1.4	0.435	3.1	4.9	6.6	8.4	10.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

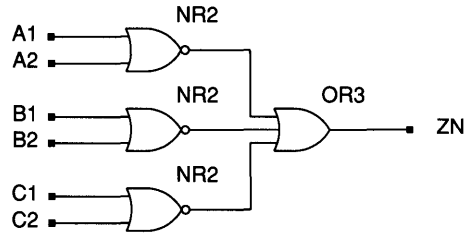
- Three 2-ORs into 3-NAND

- Soft Macrocell
- 5 Gate Equivalents
- 14 TPTs
- 0 RLTs

Symbol



Schematic



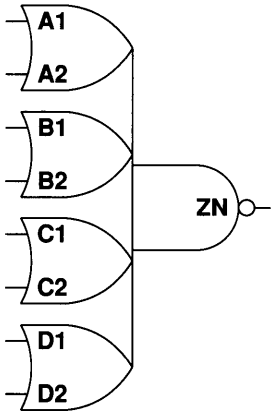
Function Table

Inputs						Output
A1	A2	B1	B2	C1	C2	ZN
1	?	1	?	1	?	0
?	1	1	?	1	?	0
1	?	?	1	1	?	0
?	1	?	1	1	?	0
1	?	1	?	?	1	0
?	1	1	?	?	1	0
1	?	?	1	?	1	0
?	1	?	1	?	1	0
0	0	?	?	?	?	1
?	?	0	0	?	?	1
?	?	?	?	0	0	1

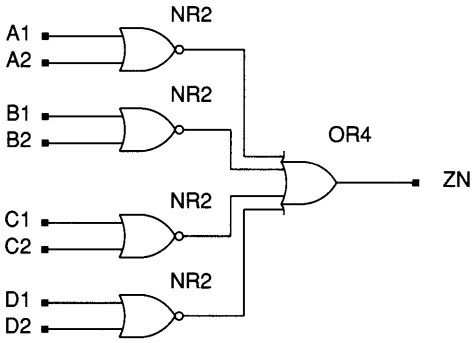
- Four 2-ORs into 4-NAND

- Soft Macrocell
- 7 Gate Equivalents
- 20 TPTs
- 0 RLTs

Symbol



Schematic



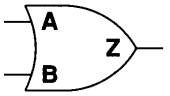
Function Table

Inputs								Output
A1	A2	B1	B2	C1	C2	D1	D2	ZN
1	?	1	?	1	?	1	?	0
?	1	1	?	1	?	1	?	0
1	?	?	1	1	?	1	?	0
?	1	?	1	1	?	1	?	0
1	?	1	?	?	1	1	?	0
?	1	1	?	?	1	1	?	0
1	?	?	1	?	1	1	?	0
?	1	?	1	?	1	1	?	0
1	?	1	?	1	?	?	1	0
?	1	1	?	1	?	?	1	0
1	?	?	1	1	?	?	1	0
?	1	?	1	1	?	?	1	0
1	?	1	?	?	1	?	1	0
?	1	1	?	?	1	?	1	0
1	?	?	1	?	1	?	1	0
?	1	?	1	?	1	?	1	0
0	0	?	?	?	?	?	?	1
?	?	0	0	?	?	?	?	1
?	?	?	?	0	0	?	?	1
?	?	?	?	?	?	0	0	1

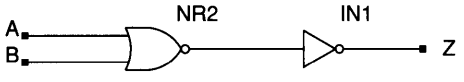
- 2-Input OR

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	Z
1	?	1
?	1	1
0	0	0

Pin Load

Pin	Std Load
A	1.0
B	1.0

Timing Parameters[1]

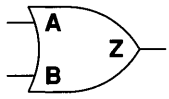
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.66	0.202	2.5	3.3	4.1	4.9	5.7
t_{PD}	A(↓) to Z(↓)	1.77	0.183	2.5	3.2	4.0	4.7	5.4
t_{PD}	B(↑) to Z(↑)	1.46	0.198	2.3	3.0	3.8	4.6	5.4
t_{PD}	B(↓) to Z(↓)	1.79	0.185	2.5	3.3	4.0	4.8	5.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

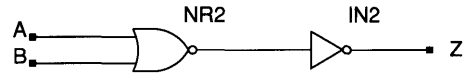
- High drive 2-Input OR

- Hard Macrocell
- 2 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	Z
1	?	1
?	1	1
0	0	0

Pin Load

Pin	Std Load
A	1.0
B	1.0

Timing Parameters[1]

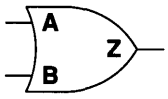
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.85	0.132	2.4	2.9	3.4	4.0	4.5
t_{PD}	A(↓) to Z(↓)	1.95	0.134	2.5	3.0	3.6	4.1	4.6
t_{PD}	B(↑) to Z(↑)	1.71	0.131	2.2	2.8	3.3	3.8	4.3
t_{PD}	B(↓) to Z(↓)	1.96	0.135	2.5	3.0	3.6	4.1	4.7

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

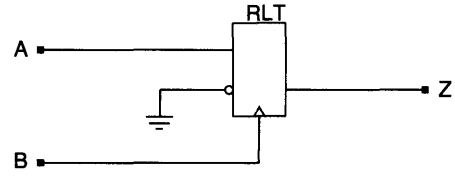
- 2-Input OR using an RLT

- Hard Macrocell
- 2 Gate Equivalents
- 0 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	Z
1	?	1
?	1	1
0	0	0

Pin Load

Pin	Std Load
A	0.5
B	0.6

Timing Parameters[1]

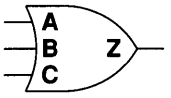
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.32	0.179	3.0	3.8	4.5	5.2	5.9
t_{PD}	A(↓) to Z(↓)	2.37	0.147	3.0	3.5	4.1	4.7	5.3
t_{PD}	B(↑) to Z(↑)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	B(↓) to Z(↓)	2.28	0.147	2.9	3.5	4.0	4.6	5.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

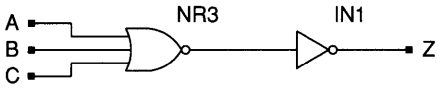
- 3-Input OR

- Hard Macrocell
- 2 Gate Equivalents
- 5 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	Z
1	?	?	1
?	1	?	1
?	?	1	1
0	0	0	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0

Timing Parameters[1]

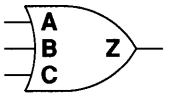
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.86	0.202	2.7	3.5	4.3	5.1	5.9
t_{PD}	A(↓) to Z(↓)	2.25	0.192	3.0	3.8	4.6	5.3	6.1
t_{PD}	B(↑) to Z(↑)	1.95	0.202	2.8	3.6	4.4	5.2	6.0
t_{PD}	B(↓) to Z(↓)	2.31	0.191	3.1	3.8	4.6	5.4	6.1
t_{PD}	C(↑) to Z(↑)	1.71	0.198	2.5	3.3	4.1	4.9	5.7
t_{PD}	C(↓) to Z(↓)	2.39	0.193	3.2	3.9	4.7	5.5	6.3

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

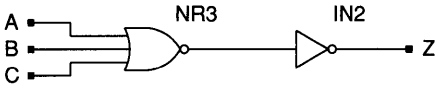
- High drive 3-Input OR

- Hard Macrocell
- 3 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	Z
1	?	?	1
?	1	?	1
?	?	1	1
0	0	0	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0

Timing Parameters[1]

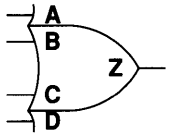
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	2.03	0.132	2.6	3.1	3.6	4.1	4.7
t_{PD}	A(↓) to Z(↓)	2.46	0.141	3.0	3.6	4.2	4.7	5.3
t_{PD}	B(↑) to Z(↑)	2.12	0.132	2.6	3.2	3.7	4.2	4.8
t_{PD}	B(↓) to Z(↓)	2.5	0.141	3.1	3.6	4.2	4.8	5.3
t_{PD}	C(↑) to Z(↑)	1.93	0.131	2.5	3.0	3.5	4.0	4.6
t_{PD}	C(↓) to Z(↓)	2.59	0.142	3.2	3.7	4.3	4.9	5.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

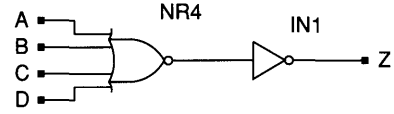
- 3-Input OR

- Hard Macrocell
- 3 Gate Equivalents
- 8 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A	B	C	D	Z
1	?	?	?	1
?	1	?	?	1
?	?	1	?	1
?	?	?	1	1
0	0	0	0	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

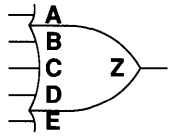
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.68	0.199	2.5	3.3	4.1	4.9	5.7
t_{PD}	A(↓) to Z(↓)	2.76	0.202	3.6	4.4	5.2	6.0	6.8
t_{PD}	B(↑) to Z(↑)	2.04	0.202	2.8	3.7	4.5	5.3	6.1
t_{PD}	B(↓) to Z(↓)	2.8	0.201	3.6	4.4	5.2	6.0	6.8
t_{PD}	C(↑) to Z(↑)	2.11	0.202	2.9	3.7	4.5	5.3	6.2
t_{PD}	C(↓) to Z(↓)	4.92	0.2	5.7	6.5	7.3	8.1	8.9
t_{PD}	D(↑) to Z(↑)	2.16	0.203	3.0	3.8	4.6	5.4	6.2
t_{PD}	D(↓) to Z(↓)	2.96	0.2	3.8	4.6	5.4	6.2	7.0

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

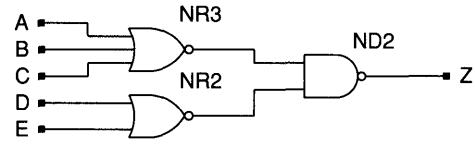
- 5-Input OR

- Hard Macrocell
- 5 Gate Equivalents
- 9 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs					Output
A	B	C	D	E	Z
1	?	?	?	?	1
?	1	?	?	?	1
?	?	1	?	?	1
?	?	?	1	?	1
?	?	?	?	1	1
0	0	0	0	0	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0

Timing Parameters[1]

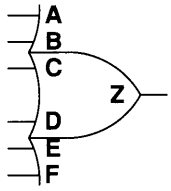
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.88	0.202	2.7	3.5	4.3	5.1	5.9
t_{PD}	A(↓) to Z(↓)	2.42	0.238	3.4	4.3	5.3	6.2	7.2
t_{PD}	B(↑) to Z(↑)	1.97	0.202	2.8	3.6	4.4	5.2	6.0
t_{PD}	B(↓) to Z(↓)	2.49	0.237	3.4	4.4	5.3	6.3	7.2
t_{PD}	C(↑) to Z(↑)	2.02	0.202	2.8	3.6	4.4	5.3	6.1
t_{PD}	C(↓) to Z(↓)	2.54	0.236	3.5	4.4	5.4	6.3	7.3
t_{PD}	D(↑) to Z(↑)	1.82	0.202	2.6	3.4	4.2	5.0	5.9
t_{PD}	D(↓) to Z(↓)	1.86	0.232	2.8	3.7	4.6	5.6	6.5
t_{PD}	E(↑) to Z(↑)	1.87	0.202	2.7	3.5	4.3	5.1	5.9
t_{PD}	E(↓) to Z(↓)	1.89	0.232	2.8	3.7	4.7	5.6	6.5

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

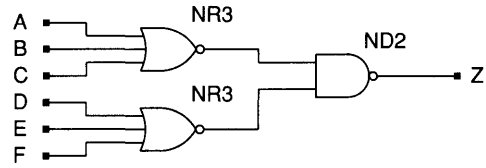
- 6-Input OR

- Hard Macrocell
- 6 Gate Equivalents
- 10 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs						Output
A	B	C	D	E	F	Z
1	?	?	?	?	?	1
?	1	?	?	?	?	1
?	?	1	?	?	?	1
?	?	?	1	?	?	1
?	?	?	?	1	?	1
?	?	?	?	?	1	1
0	0	0	0	0	0	0

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0
E	1.0
F	1.0

Timing Parameters[1]

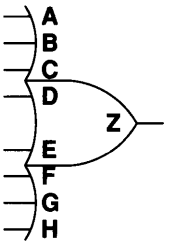
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑)	1.88	0.202	2.7	3.5	4.3	5.1	5.9
t_{PD}	A(↓) to Z(↓)	2.42	0.238	3.4	4.3	5.3	6.2	7.2
t_{PD}	B(↑) to Z(↑)	1.97	0.202	2.8	3.6	4.4	5.2	6.0
t_{PD}	B(↓) to Z(↓)	2.48	0.237	3.4	4.4	5.3	6.3	7.2
t_{PD}	C(↑) to Z(↑)	2.02	0.202	2.8	3.6	4.4	5.3	6.1
t_{PD}	C(↓) to Z(↓)	2.53	0.237	3.5	4.4	5.4	6.3	7.3
t_{PD}	D(↑) to Z(↑)	2.02	0.202	2.8	3.6	4.4	5.3	6.1
t_{PD}	D(↓) to Z(↓)	2.34	0.235	3.3	4.2	5.2	6.1	7.0
t_{PD}	E(↑) to Z(↑)	2.1	0.202	2.9	3.7	4.5	5.3	6.1
t_{PD}	E(↓) to Z(↓)	2.41	0.235	3.3	4.3	5.2	6.2	7.1
t_{PD}	F(↑) to Z(↑)	2.15	0.202	3.0	3.8	4.6	5.4	6.2
t_{PD}	F(↓) to Z(↓)	2.46	0.235	3.4	4.3	5.3	6.2	7.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

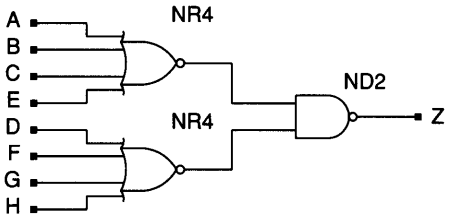
- 8-Input OR

- Soft Macrocell
- 5 Gate Equivalents
- 15 TPTs
- 0 RLTs

Symbol



Schematic



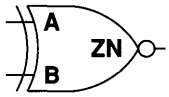
Function Table

Inputs								Output
A	B	C	D	E	F	G	H	Z
1	?	?	?	?	?	?	?	1
?	1	?	?	?	?	?	?	1
?	?	1	?	?	?	?	?	1
?	?	?	1	?	?	?	?	1
?	?	?	?	1	?	?	?	1
?	?	?	?	?	1	?	?	1
?	?	?	?	?	?	1	?	1
?	?	?	?	?	?	?	1	1
0	0	0	0	0	0	0	0	0

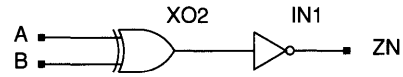
- 2-Input Exclusive NOR

- Soft Macrocell
- 4 Gate Equivalents
- 2 TPTs
- 1 RLTs

Symbol



Schematic



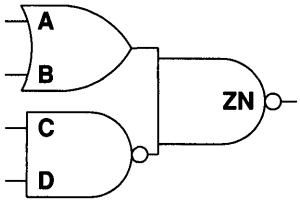
Function Table

Inputs		Output
A	B	ZN
0	0	1
1	0	0
0	1	0
1	1	1

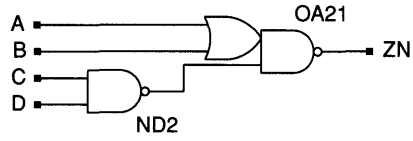
- 2-OR, 2-NAND into 2-NAND

- Hard Macrocell
- 3 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A	B	C	D	ZN
1	?	0	?	0
?	1	0	?	0
1	?	?	0	0
?	1	?	0	0
0	0	?	?	1
?	?	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

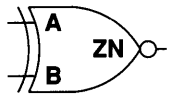
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓) with C(1) D(0)	1.36	0.165	2.0	2.7	3.3	4.0	4.7
t_{PD}	A(↓) to ZN(↑) with C(1) D(0)	1.27	0.437	3.0	4.8	6.5	8.3	10.0
t_{PD}	B(↑) to ZN(↓) with C(1) D(0)	1.25	0.213	2.1	3.0	3.8	4.7	5.5
t_{PD}	B(↓) to ZN(↑) with C(1) D(0)	1.21	0.436	3.0	4.7	6.4	8.2	9.9
t_{PD}	C(↑) to ZN(↑) with A(0) B(1)	1.9	0.202	2.7	3.5	4.3	5.1	5.9
t_{PD}	C(↓) to ZN(↓) with A(0) B(1)	1.91	0.301	3.1	4.3	5.5	6.7	7.9
t_{PD}	D(↑) to ZN(↑) with A(0) B(1)	2	0.201	2.8	3.6	4.4	5.2	6.0
t_{PD}	D(↓) to ZN(↓) with A(0) B(1)	2.06	0.301	3.3	4.5	5.7	6.9	8.1

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

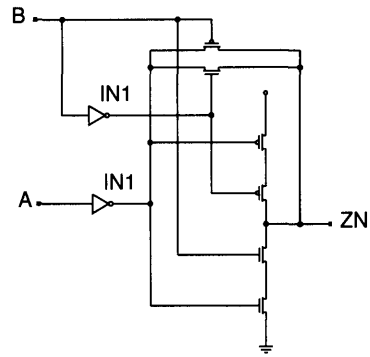
- 2-Input Exclusive NOR using TPTs.

- Hard Macrocell
- 3 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	ZN
0	0	1
1	0	0
0	1	0
1	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.8

Timing Parameters[1]

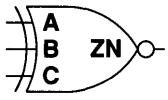
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to ZN(↓) with B(0)	1.65	0.156	2.3	2.9	3.5	4.1	4.8
t_{PD}	A(↓) to ZN(↑) with B(0)	1.57	0.331	2.9	4.2	5.5	6.9	8.2
t_{PD}	A(↑) to ZN(↑) with B(1)	2.07	0.301	3.3	4.5	5.7	6.9	8.1
t_{PD}	A(↓) to ZN(↓) with B(1)	1.74	0.205	2.6	3.4	4.2	5.0	5.8
t_{PD}	B(↑) to ZN(↓) with A(0)	1.48	0.172	2.2	2.9	3.5	4.2	4.9
t_{PD}	B(↓) to ZN(↑) with A(0)	0.996	0.316	2.3	3.5	4.8	6.1	7.3
t_{PD}	B(↑) to ZN(↑) with A(1)	1.65	0.296	2.8	4.0	5.2	6.4	7.6
t_{PD}	B(↓) to ZN(↓) with A(1)	1.31	0.195	2.1	2.9	3.7	4.4	5.2

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

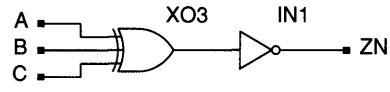
- 3-Input Exclusive NOR

- Soft Macrocell
- 7 Gate Equivalents
- 2 TPTs
- 2 RLTs

Symbol



Schematic



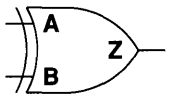
Function Table

Inputs			Output
A	B	C	ZN
0	0	0	1
1	0	1	1
1	1	0	1
0	1	1	1
1	0	0	0
0	1	0	0
0	0	1	0
1	1	1	0

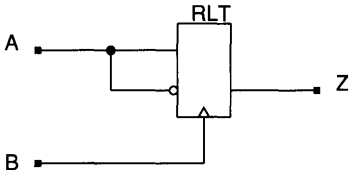
- 2-Input Exclusive OR

- Hard Macrocell
- 3 Gate Equivalents
- 0 TPTs
- 1 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0

Pin Load

Pin	Std Load
A	0.9
B	0.6

Timing Parameters[1]

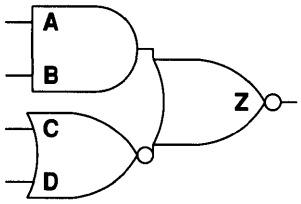
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑) with B(0)	2.33	0.179	3.0	3.8	4.5	5.2	5.9
t_{PD}	A(↓) to Z(↓) with B(0)	2.38	0.147	3.0	3.6	4.1	4.7	5.3
t_{PD}	A(↑) to Z(↓) with B(1)	2.84	0.113	3.3	3.7	4.2	4.7	5.1
t_{PD}	A(↓) to Z(↑) with B(1)	2.32	0.25	3.3	4.3	5.3	6.3	7.3
t_{PD}	B(↑) to Z(↑) with A(0)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	B(↓) to Z(↓) with A(0)	2.28	0.147	2.9	3.5	4.0	4.6	5.2
t_{PD}	B(↑) to Z(↓) with A(1)	2.76	0.113	3.2	3.7	4.1	4.6	5.0
t_{PD}	B(↓) to Z(↑) with A(1)	2.41	0.25	3.4	4.4	5.4	6.4	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

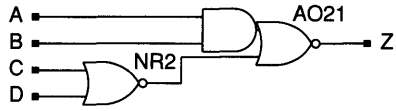
- 2-AND, 2-NOR into 2-NOR

- Hard Macrocell
- 3 Gate Equivalents
- 7 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs				Output
A	B	C	D	Z
1	1	?	?	0
?	?	0	0	0
0	?	1	?	1
?	0	1	?	1
0	?	?	1	1
?	0	?	1	1

Pin Load

Pin	Std Load
A	1.0
B	1.0
C	1.0
D	1.0

Timing Parameters[1]

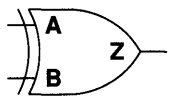
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↓) with C(0) D(1)	1.42	0.165	2.1	2.7	3.4	4.1	4.7
t_{PD}	A(↓) to Z(↑) with C(0) D(1)	0.96	0.435	2.7	4.4	6.2	7.9	9.7
t_{PD}	B(↑) to Z(↓) with C(0) D(1)	1.5	0.154	2.1	2.7	3.3	4.0	4.6
t_{PD}	B(↓) to Z(↑) with C(0) D(1)	1.05	0.527	3.2	5.3	7.4	9.5	11.6
t_{PD}	C(↑) to Z(↑) with A(1) B(0)	2.16	0.36	3.6	5.0	6.5	7.9	9.4
t_{PD}	C(↓) to Z(↓) with A(1) B(0)	2.12	0.185	2.9	3.6	4.3	5.1	5.8
t_{PD}	D(↑) to Z(↑) with A(1) B(0)	2.21	0.359	3.6	5.1	6.5	8.0	9.4
t_{PD}	D(↓) to Z(↓) with A(1) B(0)	2.15	0.185	2.9	3.6	4.4	5.1	5.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

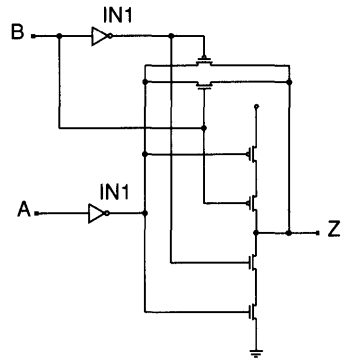
- 2-Input Exclusive OR using TPTs

- Hard Macrocell
- 3 Gate Equivalents
- 6 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs		Output
A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0

Pin Load

Pin	Std Load
A	1.0
B	1.9

Timing Parameters[1]

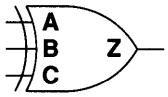
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑) with B(0)	2	0.301	3.2	4.4	5.6	6.8	8.0
t_{PD}	A(↓) to Z(↓) with B(0)	1.72	0.229	2.6	3.6	4.5	5.4	6.3
t_{PD}	A(↑) to Z(↓) with B(1)	1.62	0.151	2.2	2.8	3.4	4.0	4.6
t_{PD}	A(↓) to Z(↑) with B(1)	1.57	0.322	2.9	4.1	5.4	6.7	8.0
t_{PD}	B(↑) to Z(↑) with A(0)	1.64	0.21	2.5	3.3	4.2	5.0	5.8
t_{PD}	B(↓) to Z(↓) with A(0)	1.35	0.221	2.2	3.1	4.0	4.9	5.8
t_{PD}	B(↑) to Z(↓) with A(1)	1.4	0.152	2.0	2.6	3.2	3.8	4.4
t_{PD}	B(↓) to Z(↑) with A(1)	1.1	0.434	2.8	4.6	6.3	8.0	9.8

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

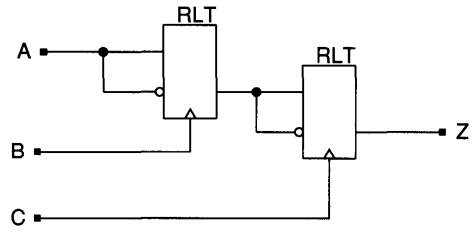
- 3-Input Exclusive OR

- Hard Macrocell
- 6 Gate Equivalents
- 0 TPTs
- 2 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	Z
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	0
1	0	0	1
0	1	0	1
0	0	1	1
1	1	1	1

Pin Load

Pin	Std Load
A	0.9
B	0.6
C	0.6

Timing Parameters[1]

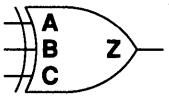
Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑) with B(0) C(0)	4.41	0.179	5.1	5.8	6.6	7.3	8.0
t_{PD}	A(↓) to Z(↓) with B(0) C(0)	4.59	0.147	5.2	5.8	6.4	6.9	7.5
t_{PD}	A(↑) to Z(↓) with B(0) C(1)	4.85	0.113	5.3	5.8	6.2	6.7	7.1
t_{PD}	A(↓) to Z(↑) with B(0) C(1)	4.21	0.25	5.2	6.2	7.2	8.2	9.2
t_{PD}	A(↑) to Z(↓) with B(1) C(0)	5.05	0.113	5.5	6.0	6.4	6.9	7.3
t_{PD}	A(↓) to Z(↑) with B(1) C(0)	4.39	0.25	5.4	6.4	7.4	8.4	9.4
t_{PD}	A(↑) to Z(↑) with B(1) C(1)	4.68	0.179	5.4	6.1	6.8	7.5	8.3
t_{PD}	A(↓) to Z(↓) with B(1) C(1)	4.84	0.147	5.4	6.0	6.6	7.2	7.8
t_{PD}	B(↑) to Z(↑) with A(0) C(0)	4.27	0.179	5.0	5.7	6.4	7.1	7.9
t_{PD}	B(↓) to Z(↓) with A(0) C(0)	4.49	0.147	5.1	5.7	6.3	6.8	7.4
t_{PD}	B(↑) to Z(↓) with A(0) C(1)	4.72	0.113	5.2	5.6	6.1	6.5	7.0
t_{PD}	B(↓) to Z(↑) with A(0) C(1)	4.11	0.25	5.1	6.1	7.1	8.1	9.1
t_{PD}	B(↑) to Z(↓) with A(1) C(0)	4.97	0.113	5.4	5.9	6.3	6.8	7.2
t_{PD}	B(↓) to Z(↑) with A(1) C(0)	4.48	0.25	5.5	6.5	7.5	8.5	9.5
t_{PD}	B(↑) to Z(↑) with A(1) C(1)	4.59	0.179	5.3	6.0	6.7	7.5	8.2
t_{PD}	B(↓) to Z(↓) with A(1) C(1)	4.93	0.147	5.5	6.1	6.7	7.3	7.9
t_{PD}	C(↑) to Z(↑) with A(0) B(0)	2.21	0.179	2.9	3.6	4.4	5.1	5.8
t_{PD}	C(↓) to Z(↓) with A(0) B(0)	2.28	0.147	2.9	3.5	4.0	4.6	5.2
t_{PD}	C(↑) to Z(↓) with A(0) B(1)	2.79	0.113	3.2	3.7	4.1	4.6	5.1
t_{PD}	C(↓) to Z(↑) with A(0) B(1)	2.4	0.25	3.4	4.4	5.4	6.4	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

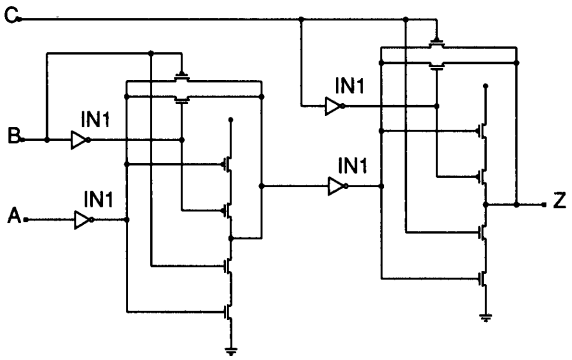
• 3-Input Exclusive OR using TPTs

- Hard Macrocell
- 6 Gate Equivalents
- 12 TPTs
- 0 RLTs

Symbol



Schematic



Function Table

Inputs			Output
A	B	C	Z
0	0	0	0
1	0	1	0
1	1	0	0
0	1	1	0
1	0	0	1
0	1	0	1
0	0	1	1
1	1	1	1

Pin Load

Pin	Std Load
A	1.0
B	2.0
C	1.8

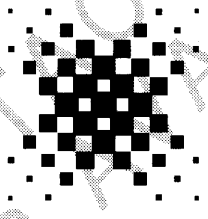
Timing Parameters[1]

Type	Description	Intrinsic (ns)	Drive (ns/ld)	Delay Given Standard Load (ns)[2]				
				4	8	12	16	20
t_{PD}	A(↑) to Z(↑) with B(0) C(0)	3.19	0.23	4.1	5.0	5.9	6.9	7.8
t_{PD}	A(↓) to Z(↓) with B(0) C(0)	3.04	0.213	3.9	4.7	5.6	6.4	7.3
t_{PD}	A(↑) to Z(↓) with B(0) C(1)	3.37	0.151	4.0	4.6	5.2	5.8	6.4
t_{PD}	A(↓) to Z(↑) with B(0) C(1)	3.62	0.441	5.4	7.1	8.9	10.7	12.4
t_{PD}	A(↑) to Z(↓) with B(1) C(0)	3.71	0.155	4.3	5.0	5.6	6.2	6.8
t_{PD}	A(↓) to Z(↑) with B(1) C(0)	3.33	0.329	4.6	6.0	7.3	8.6	9.9
t_{PD}	A(↑) to Z(↑) with B(1) C(1)	4.31	0.302	5.5	6.7	7.9	9.1	10.4
t_{PD}	A(↓) to Z(↓) with B(1) C(1)	3.54	0.206	4.4	5.2	6.0	6.8	7.7
t_{PD}	B(↑) to Z(↑) with A(0) C(0)	2.88	0.229	3.8	4.7	5.6	6.5	7.5
t_{PD}	B(↓) to Z(↓) with A(0) C(0)	2.59	0.211	3.4	4.3	5.1	6.0	6.8
t_{PD}	B(↑) to Z(↓) with A(0) C(1)	3.08	0.151	3.7	4.3	4.9	5.5	6.1
t_{PD}	B(↓) to Z(↑) with A(0) C(1)	3.23	0.441	5.0	6.8	8.5	10.3	12.0
t_{PD}	B(↑) to Z(↓) with A(1) C(0)	3.31	0.154	3.9	4.5	5.2	5.8	6.4
t_{PD}	B(↓) to Z(↑) with A(1) C(0)	2.93	0.329	4.2	5.6	6.9	8.2	9.5
t_{PD}	B(↑) to Z(↑) with A(1) C(1)	3.94	0.302	5.1	6.4	7.6	8.8	10.0
t_{PD}	B(↓) to Z(↓) with A(1) C(1)	3.14	0.206	4.0	4.8	5.6	6.4	7.3
t_{PD}	C(↑) to Z(↑) with A(0) B(0)	1.66	0.296	2.8	4.0	5.2	6.4	7.6
t_{PD}	C(↓) to Z(↓) with A(0) B(0)	1.29	0.206	2.1	2.9	3.8	4.6	5.4
t_{PD}	C(↑) to Z(↓) with A(0) B(1)	1.48	0.172	2.2	2.9	3.5	4.2	4.9
t_{PD}	C(↓) to Z(↑) with A(0) B(1)	1.01	0.317	2.3	3.5	4.8	6.1	7.4

1 Data for VCC = 5 V, $T_J = 25^0$ C, worst-case process, bin-1 parts.
2 Sum pin load and wire load to get total load.

Chapter 3

Fixed-Place Macrofunctions



Fixed-Place Macrofunctions

A number of *fixed-place* macrofunctions are provided as part of the CP20K cell library. These include RAM (Random Access Memory) modules (see Table 3-1) for general-purpose RAM applications and multiplexer bus modules (see Table 3-3) for high-speed on chip bus applications. The latter are of the form *MXmxn*, and provide data transmission over a *n*-bit wide bus from one of *m* n-bit wide sources.

The *fixed-place* in these modules refers to the requirement that the modules be manually placed in pre-defined locations before manual or automatic placement of the other cells in the design.

Each RAM module is implemented as a hard cell and several soft cells. The hard cell consists of a matrix of RLTs configured as storage cells and a row of RLTs configured as sense amplifiers. The soft cells provide the address decoding and output multiplexing required to realize a given RAM module.

Each multiplexer bus module is implemented as a hard cell and two soft cells. The hard cell consists of a matrix of RLTs and TPTs configured as 2-input multiplexers and a row of RLTs configured as bus receivers. The soft cells provides the address decoding required to select one set of multiplexer inputs in a row.

User interface to the RAM modules and multiplexer bus modules is via the pins in Table 3-3 and Table 3-4, respectively.

Table 3-1 RAM Module Sizes and Gate Count

RAM Module	Description	Total Gate Count	RLT Count	TPT Count
RAM8x4	8 words by 4 bits	186	36	100
RAM16x4	16 words by 4 bits	332	72	110
RAM32x4	32 words by 4 bits	631	144	130
RAM64x4	64 words by 4 bits	1232	288	204
RAM8x8	8 words by 8 bits	334	72	108
RAM16x8	16 words by 8 bits	624	144	122
RAM32x8	32 words by 8 bits	1215	288	150
RAM64x8	64 words by 8 bits	2408	576	264
RAM8x9	8 words by 9 bits	371	81	110
RAM16x9	16 words by 9 bits	697	162	125
RAM32x9	32 words by 9 bits	1361	324	155

Table 3-1 RAM Module Sizes and Gate Count

RAM Module	Description	Total Gate Count	RLT Count	TPT Count
RAM8x16	8 words by 16 bits	630	144	124
RAM16x16	16 words by 16 bits	1208	288	146
RAM32x16	32 words by 16 bits	2383	576	190
RAM8x32	8 words by 32 bits	1222	288	156
RAM16x32	16 words by 32 bits	2376	576	194

Table 3-2 Multiplexer Bus Module Pins

Pin	Function
A[p-1]	Row Address Input
EN	Receive Data Enable (Active Low)
DI[m-1][n-1]	Data Inputs
DO[n-1]	Data Outputs

Table 3-3 RAM Module Pins

Pin	Function
A[m-1]	Row and Column Address Inputs
EN	RAM Enable Input (Active Low)
R	Read Input (Active High)
W	Write Input (Active High)
DI[n-1]	Data Inputs
DO[n-1]	Data Outputs

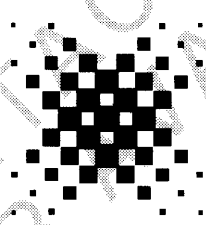
Table 3-4 Multiplexer Bus Module Sizes and Gate Count

Multiplexer Bus Module	Description	Total Gate Count	RLT Count	TPT Count
MX8x9	1 of 8 — 9 bit wide multiplexer bus	224	45	92
MX8x18	1 of 8 — 18 bit wide multiplexer bus	440	90	160
MX16x9	1 of 16 — 9 bit wide multiplexer bus	417	81	192
MX16x18	1 of 16 — 18 bit wide multiplexer bus	773	152	326

Chapter 4

Macrofunction Library Summary

This is a preliminary listing of macrofunctions and is subject to change without notice. Contact Crosspoint for availability.



Macrofunction Library Summary

The CP20K library is comparable to gate array libraries in terms of the variety and the number of elements. The CP20K library also supports the majority of generic gate array macrofunctions. These elements are listed in the following tables. A macrofunction is routed when the overall design containing it is routed. In order to make comparisons straightforward, the gate counts shown approximate to standard mask-programmable gate array gate counts.

NOTE: All macrofunctions with a CLS prefix are compatible with TTL74 series functions.

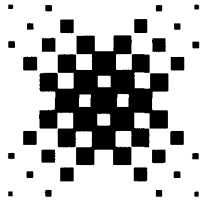
Macro-function Name	Description	Gate Count
	Adders	
CLS82	2 Bit Full Adder	14
CLS181	Arithmetic Logic Unit / Function Generator	94
CLS182	Look-Ahead Carry Generator	29
CLS183	Dual Carry Save Full Adders	26
CLS283	4-Bit Binary Full Adder, with Fast Carry	62
	Parity Checkers	
CLS180	8-Bit Odd/Even Parity Generator/Checker	26
CLS280	9-Bit Odd/Even Parity Generator/Checker	37
	Comparators	
CMP4	4-Bit Equality Comparator	12
CLS85	4-Bit Magnitude Comparator	70
	Decoders	
DE12	1 to 2 Decoder	4
DE24	2 Bit Decoder	8
DE24G	2 Bit Decoder, with Enable	11
DE38G	3 Bit Decoder, with Enable	18
CLS137	3-to-8 Decoder/Demultiplexer with Address Latches	36
CLS138	3-to-8 Decoder/Demultiplexer	22
CLS139	Dual 2-to-4 Decoders/ Demultiplexers	22
CLS154	4-to-6 Decoder/Demultiplexer	87
CLS155	Dual 2-to-4 Decoders/ Demultiplexers	21
	Encoders	
CLS148	8-to-3 Priority Encoder	44
CLS147	10-to-4 Priority Encoder	41

Macro-function Name	Description	Gate Count
	Latches	
LDP4	4-Bit D Latch	20
LDPC4	4-Bit D Latch, with CLR	26
CLS259	8-Bit Addressable Latch	87
	Flip-Flops	
FDP4	4-Bit D Flip-Flop	28
FDPC4	4-Bit D Flip-Flop, with CLR	33
	Linear Feedback Shift Registers	
LFR2	2-Bit Shift Register	10
LFRC2	2-Bit Shift Register, with CLR	12
LFRB2	2-Bit Shift Register, with CLR/SET	14
LFRC4	4-Bit Shift Register, with CLR	23
CLS91	8-Bit Shift Register	41
CLS94	4-BIt Shift Register	49
CLS95	4-BIt Shift Register	35
CLS96	5-Bit Shift Register (Dual Parallel-In, Parallel-Out)	53
CLS164	8-Bit Parallel-Out Shift Register	53
CLS165	Parallel-Load 8-Bit Shift Register	84
CLS166	Parallel-Load 8-Bit Shift Register	76
CLS194	4-Bit Bidirectional Universal Shift Register	63
CLS195	4-Bit Parallel Access Shift Register	41
CLS198	8-BIt Parallel-in, Parallel-Out Bidirectional Shift Register	95
CLS199	8-Bit Parallel-in, Parallel-Out Shift Register, J-K Input First Stage	79

Macro-function Name	Description	Gate Count
	Counters	
CLS90	Decade Counter	39
CLS92	Divide-by-Twelve Counter	32
CLS93	4-Bit Binary Counter	32
CLS98	4-Bit Data Selector/ Storage Register	34
CLS99	4-Bit Right-Shift Left-Shift Register	42
CLS160	Synchronous Decade Counter	75
CLS161	Synchronous 4-Bit Binary Counter	76
CLS162	Fully Synchronous Decode Counter	72
CLS163	Fully Synchronous 4-Bit Binary Counter	74
CLS168	Synchronous Decade Up/Down Counter	87
CLS169	Synchronous Binary Up/Down Counter	77
CLS176	Presettable Decade Counter	65
CLS177	Presettable 4-Bit Binary Counter	57
CLS190	Synchronous Up/Down Decade Counter, Single Clock	92
CLS191	Synchronous Up/Down 4-Bit Counter, Single Clock	87
CLS192	Synchronous Up/Down Decade Counter, Dual Clock	82
CLS193	Synchronous Up/Down 4-Bit Counter, Dual Clock	78
CLS290	Decade Counter	40
CLS293	4-Bit Binary Counter	32
CLS390	Dual Decade Counters	66
CLS393	Dual 4-Bit Binary Counters	58
CLS490	Dual 4-Bit Decade Counters	76
CLS668	Synchronous Decade Up/Down Counter	89
CLS669	Synchronous 4-Bit Binary Up/Down Counter	78
	Multiplexers/Demultiplexers	
CLS97	Synchronous 6-Bit Binary Rate Multiplexer	136
CLS150	16 Bit Data Selector/Multiplexer	98
CLS151	1-of-8 Data Selector/ Multiplexer, with Strobe	51
CLS152	1-of-8 Data Selector/Multiplexer	24
CLS157	Quadruple 2-of-1 Data Selectors/Multiplexers, with Non-inverted Data Outputs	15
CLS158	Quadruple 2-of-1 Data Selectors/Multiplexers, with Inverted Data Outputs	11
CLS298	Quadruple 2-Input Multiplexers, with Storage	34

Chapter 5

Package Options



Packaging Specifications and Pinout

A high-performance FPGA solution demands a high-performance packaging solution. Crosspoint uses the latest packaging technology to fulfill the unique requirements of high-performance FPGA design.

Crosspoint's package offerings include: Ceramic Pin Grid Arrays (CPGA), Ceramic Quad Flat Packs (CQFP), and Plastic Quad Flat Packs (PQFP). Key features of these packages are:

- Cavity-down orientation for improved thermal dissipation
- Five power and ground planes
- Low inductance power and ground traces
- I/O power planes which are isolated from the array power planes
- Four decoupling chip capacitors, two for the I/O power planes and two for the array power planes.

Low-cost Plastic Leadless Chip Carriers (PLCC) are also planned.

Ceramic Pin Grid Array (CPGA)

Crosspoint's CPGA family consists of 155, 223, 299 and 383 pin options. The CPGA family follows an established format for footprint and power/ground locations as used by the major mask-programmable gate array (MPGA) suppliers.

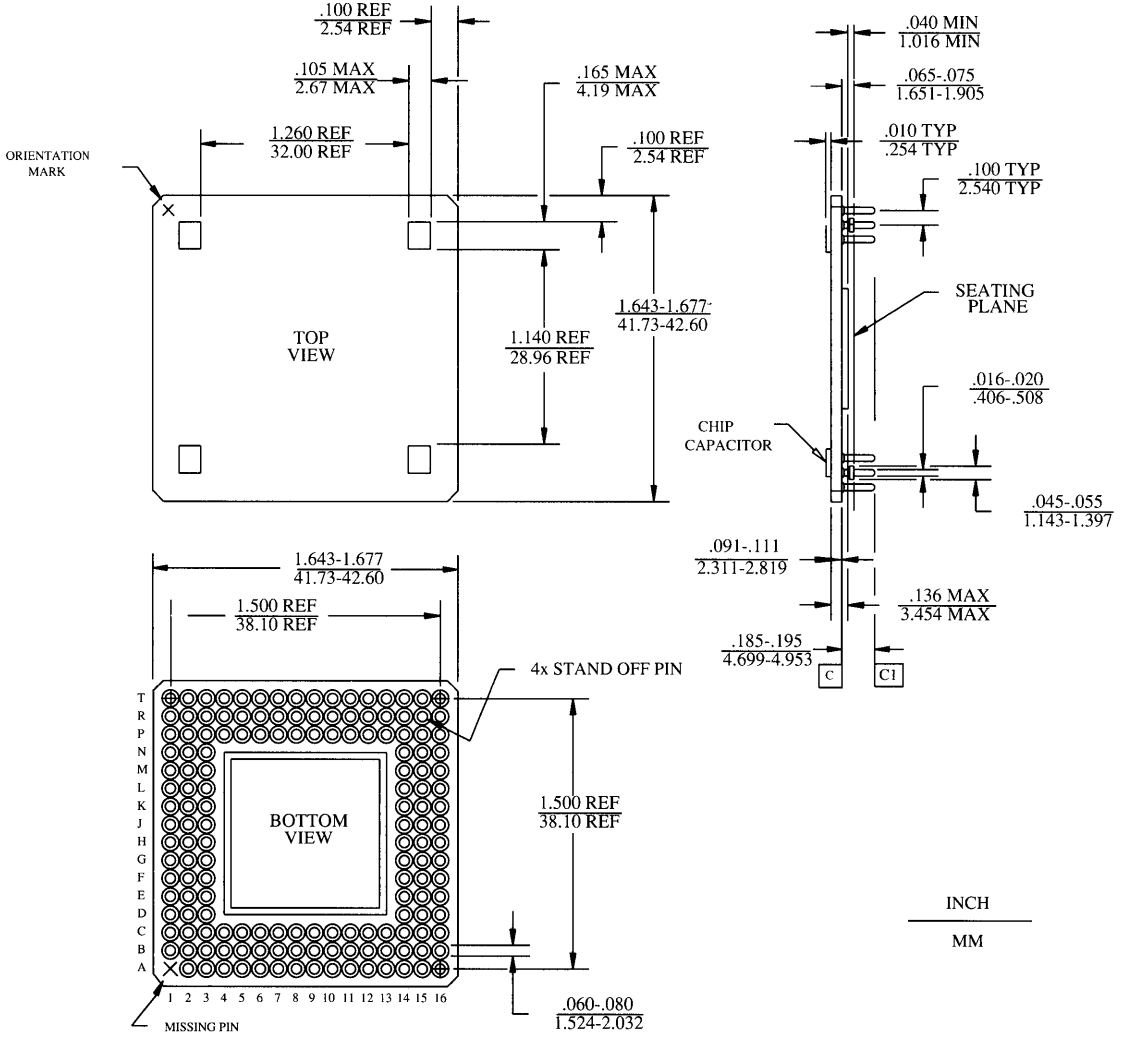
Ceramic Quad Flat Pack (CQFP)

Crosspoint's Ceramic Quad Flat Pack family includes 160 and 208 lead counts. The footprints for this family follow the industry standard for metric flat packs, which make them compatible with most MPGA packages. QFP packages are shipped in a special carrier which enables programming without compromising lead coplanarity.

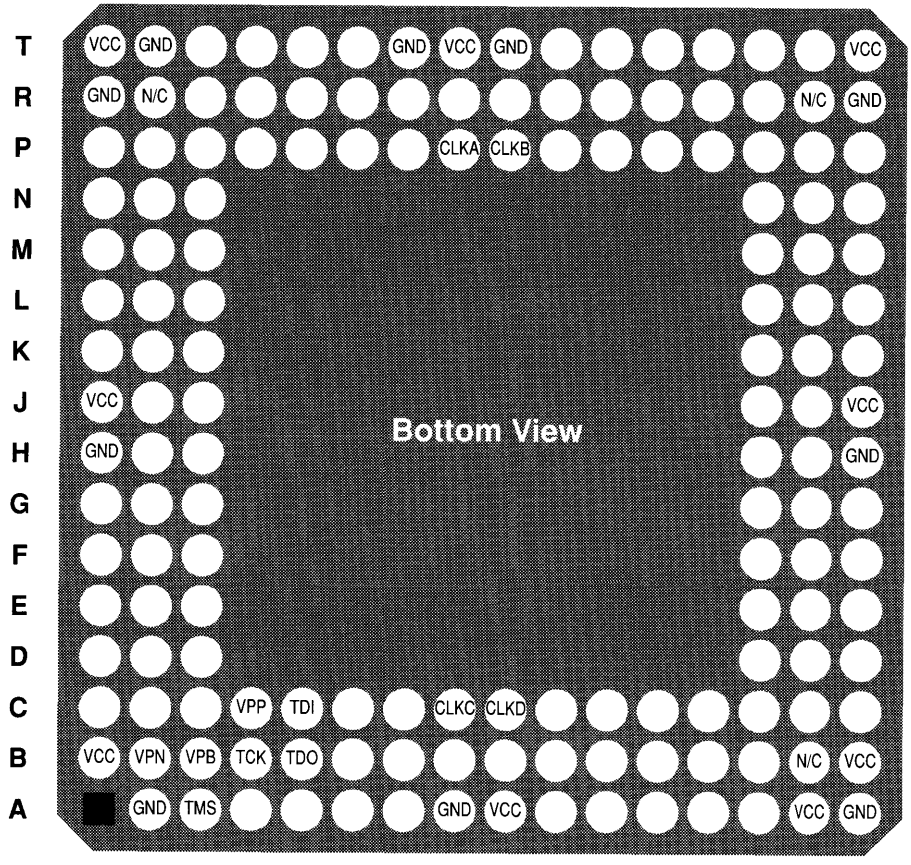
Plastic Quad Flat Pack (PQFP)

These are the equivalent plastic versions of the CQFP packages as described above. A 240 pin PQFP package is also offered for higher I/O.

155 CPGA Package Dimensions



CP20420 Pinout in 155 CPGA

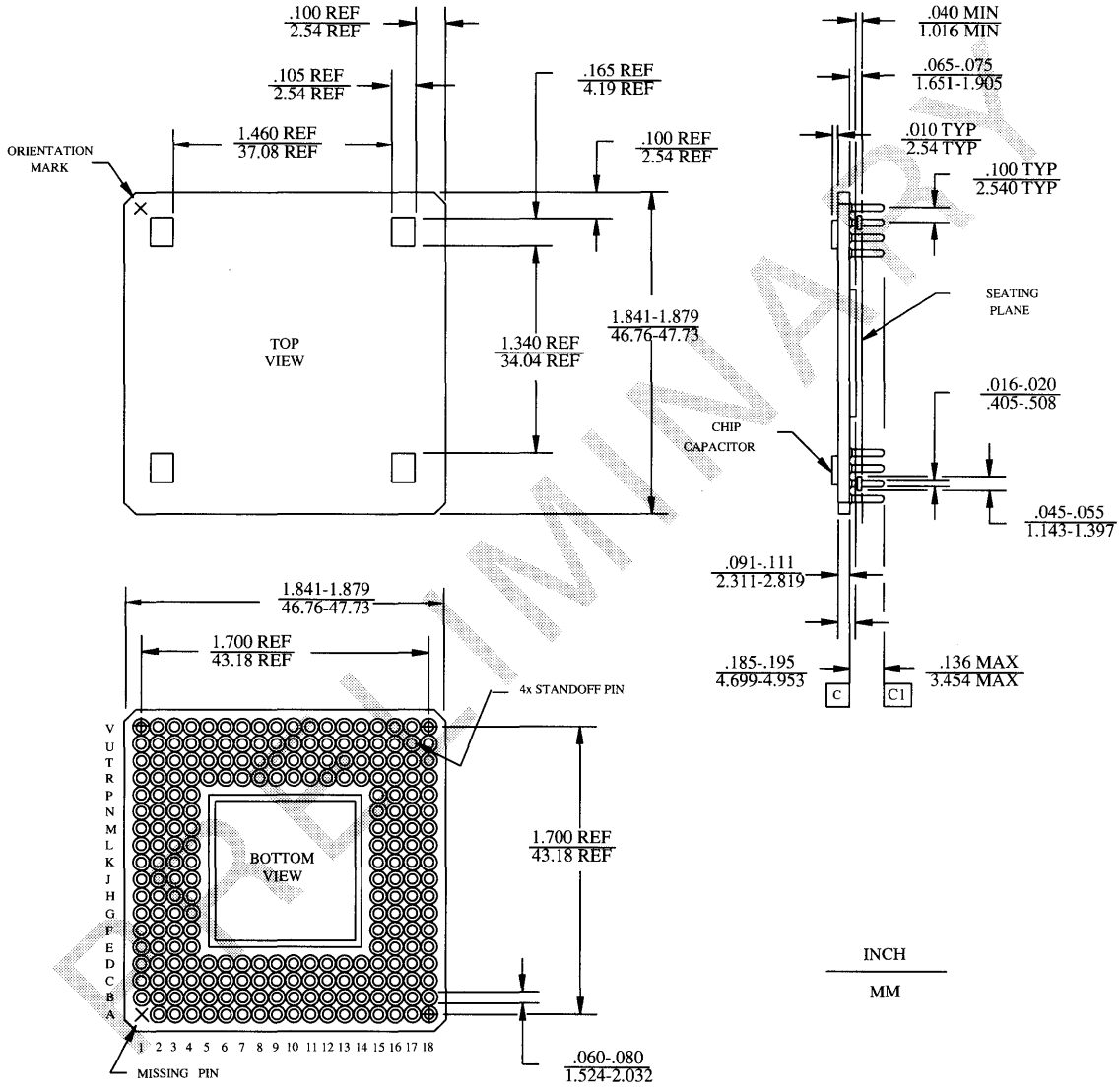


VCC	Power	N/C	No Connect	TDI	JTAG in
GND	Ground	VPP	Program[1]	TDO	TDO JTAG Out
CLK	Clock	VPB	JTAG Select[2]	TCK	JTAG Clock
		VPN	Ground[3]	TMS	JTAG Mode Select

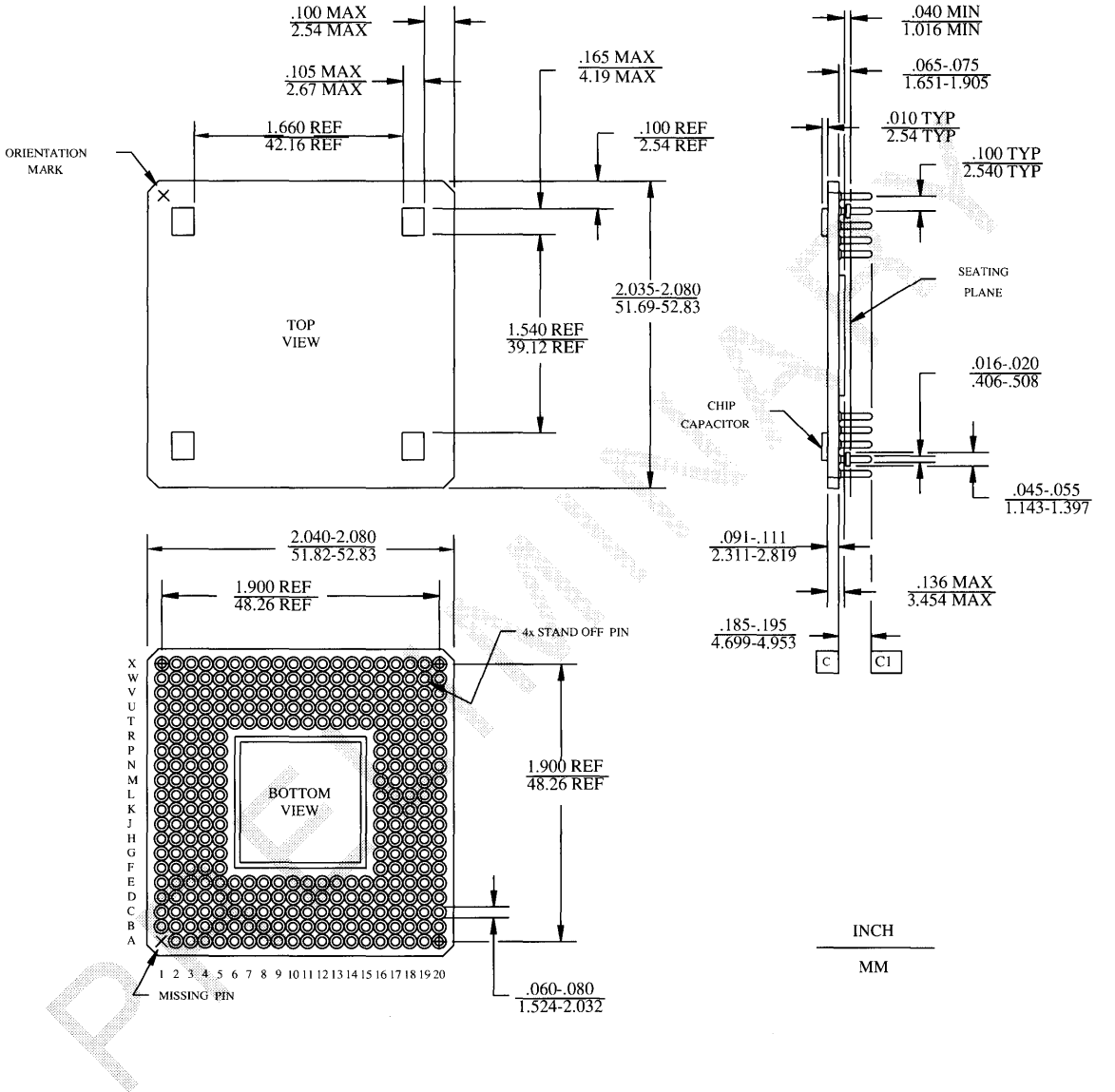
All unmarked pins are for general I/O

1. Connect to Vcc
2. Connect to GND if not using JTAG Reset
3. Connect to GND

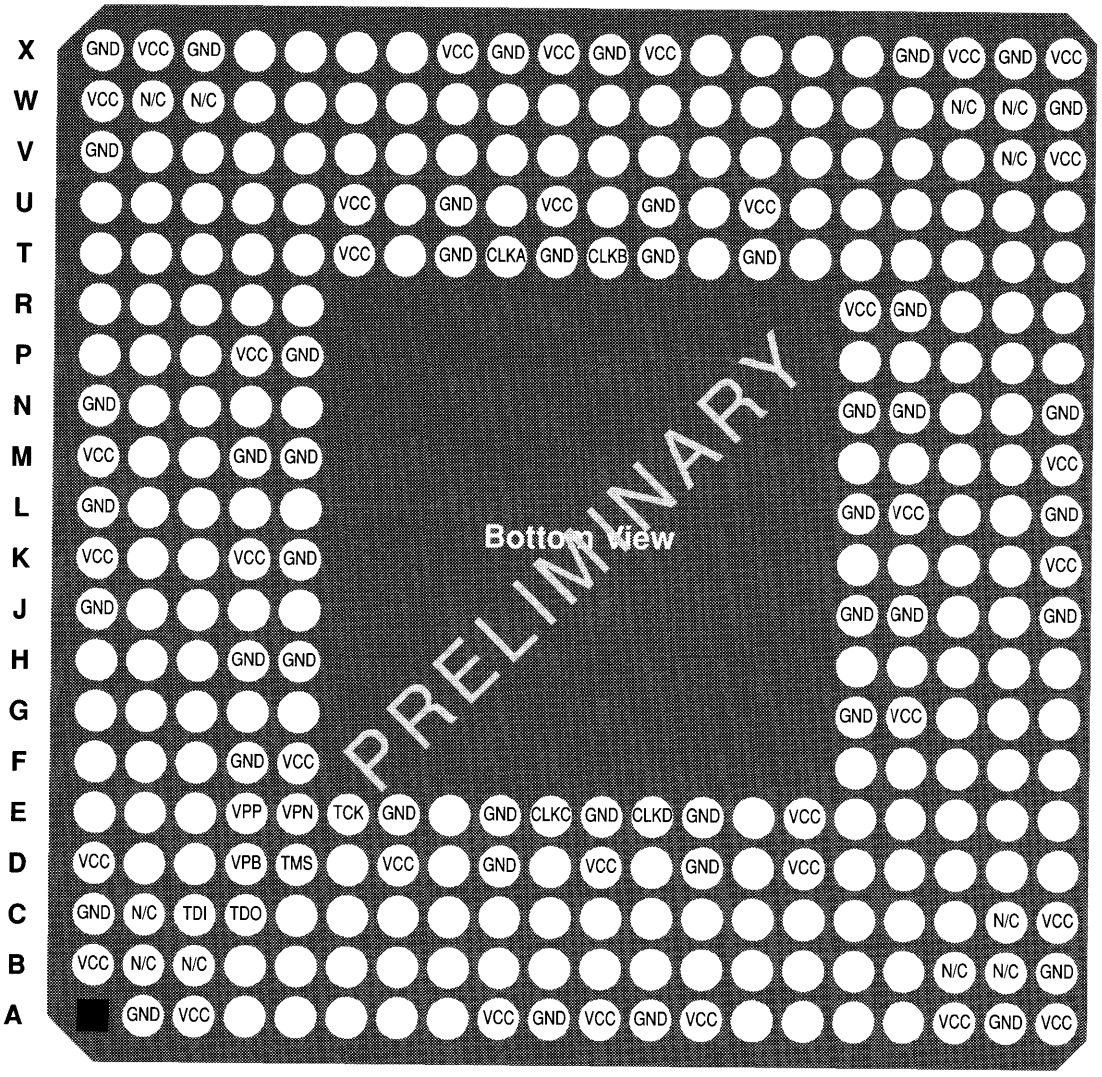
223 CPGA Package Dimensions



299 CPGA Package Dimensions



CP21200 Pinout in 299 CPGA



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
X	GND	VCC	GND					VCC	GND	VCC	GND	VCC					GND	VCC	GND	VCC
W	VCC	N/C	N/C														N/C	N/C	GND	
V	GND																	N/C	VCC	
U					VCC		GND		VCC		GND		VCC							
T					VCC		GND	CLKA	GND	CLKB	GND		GND							
R																VCC	GND			
P				VCC	GND															
N	GND															GND	GND		GND	
M	VCC			GND	GND														VCC	
L	GND															GND	VCC		GND	
K	VCC			VCC	GND														VCC	
J	GND															GND	GND		GND	
H				GND	GND															
G																GND	VCC			
F				GND	VCC															
E				VPP	VPN	TCK	GND		GND	CLKC	GND	CLKD	GND		VCC					
D	VCC			VPB	TMS		VCC		GND		VCC		GND		VCC					
C	GND	N/C	TDI	TDO														N/C	VCC	
B	VCC	N/C	N/C															N/C	N/C	GND
A	■	GND	VCC						VCC	GND	VCC	GND	VCC					VCC	GND	VCC

VCC	Power	N/C	No Connect	TDI	JTAG in
GND	Ground	VPP	Program[1]	TDO	JTAG Out
CLK	Clock	VPB	JTAG Select[2]	TCK	JTAG Clock
		VPN	Ground[3]	TMS	JTAG Mode Select

All unmarked pins are for general I/O

1. Connect to Vcc
2. Connect to GND if not using JTAG Reset
3. Connect to GND

CP20420 Pinout in 160 CQFP

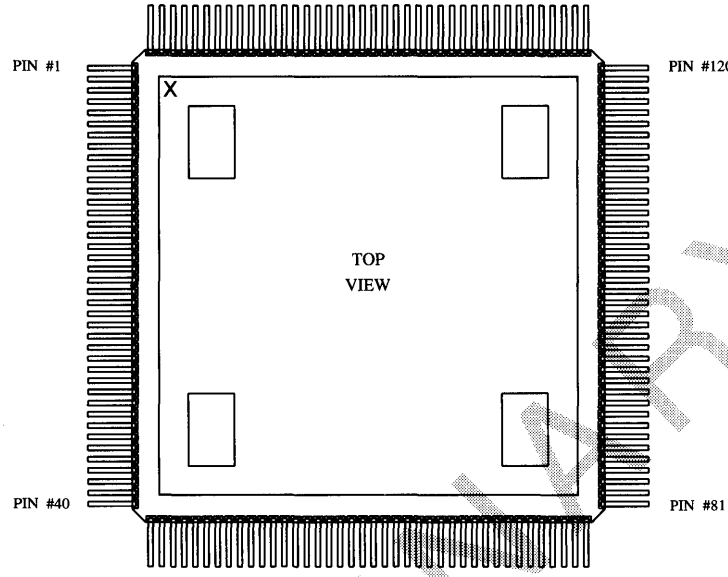


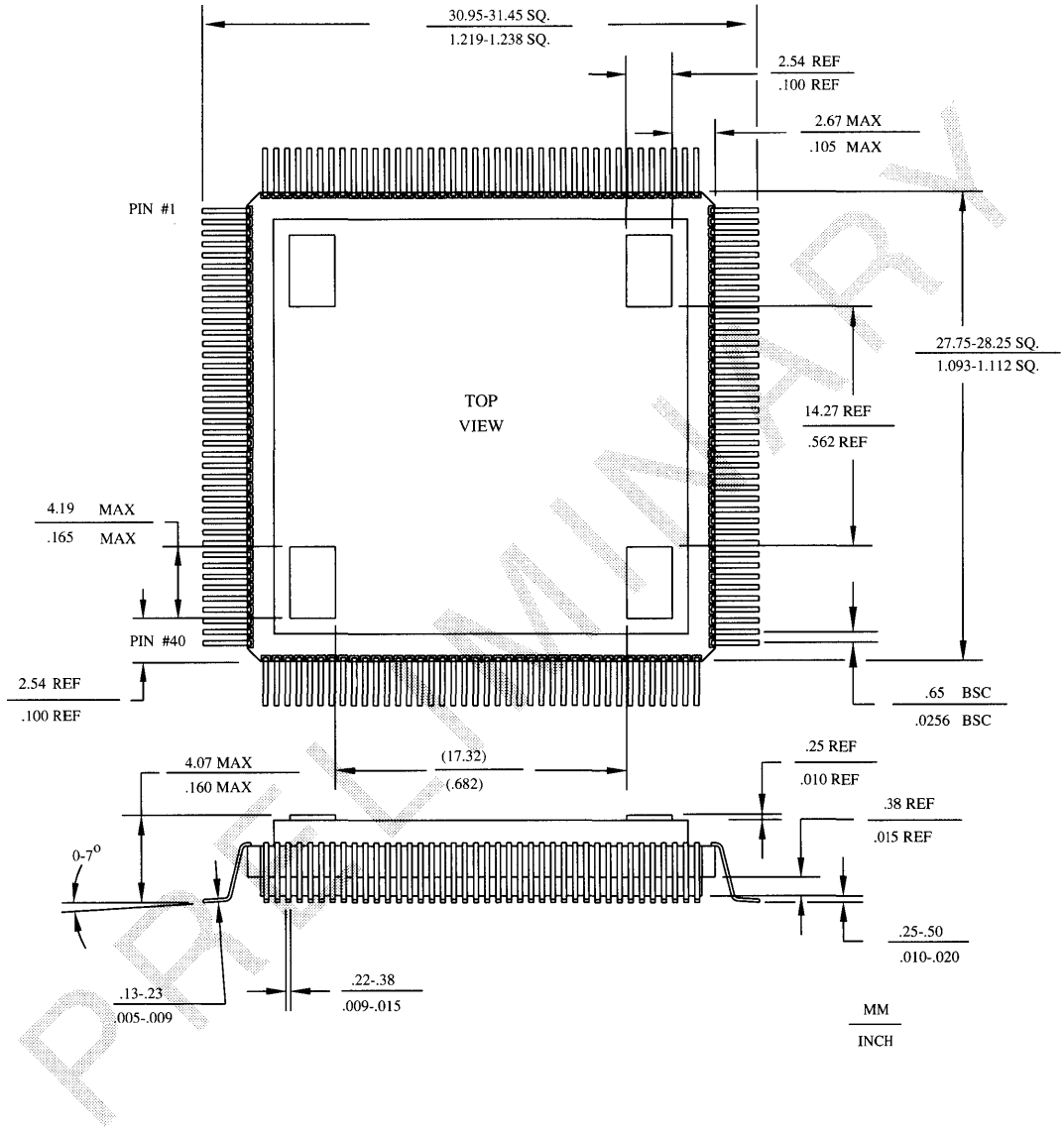
Table 1-1 CP20420 Pinout in 160 CQFP

Left		Bottom		Right		Top	
Lead No.	Function	Lead No.	Function	Lead No.	Function	Lead No.	Function
1	GND	41	GND	81	GND	121	GND
10	GND	42	N/C*	90	GND	122	N/C
20	VCC	50	GND	100	VCC	130	GND
30	GND	58	CLKD	110	GND	131	N/C
40	VCC	59	GND	120	VCC	137	N/C
		60	VCC			138	CLKA
		61	CLKC			139	GND
		70	GND			140	VCC
		73	TDO			141	CLKB
		74	TMS			150	GND
		75	TCK			159	N/C
		76	TDI			160	VCC
		77	VPB†				
		78	VPN‡				
		79	VPP**				
		80	VCC				

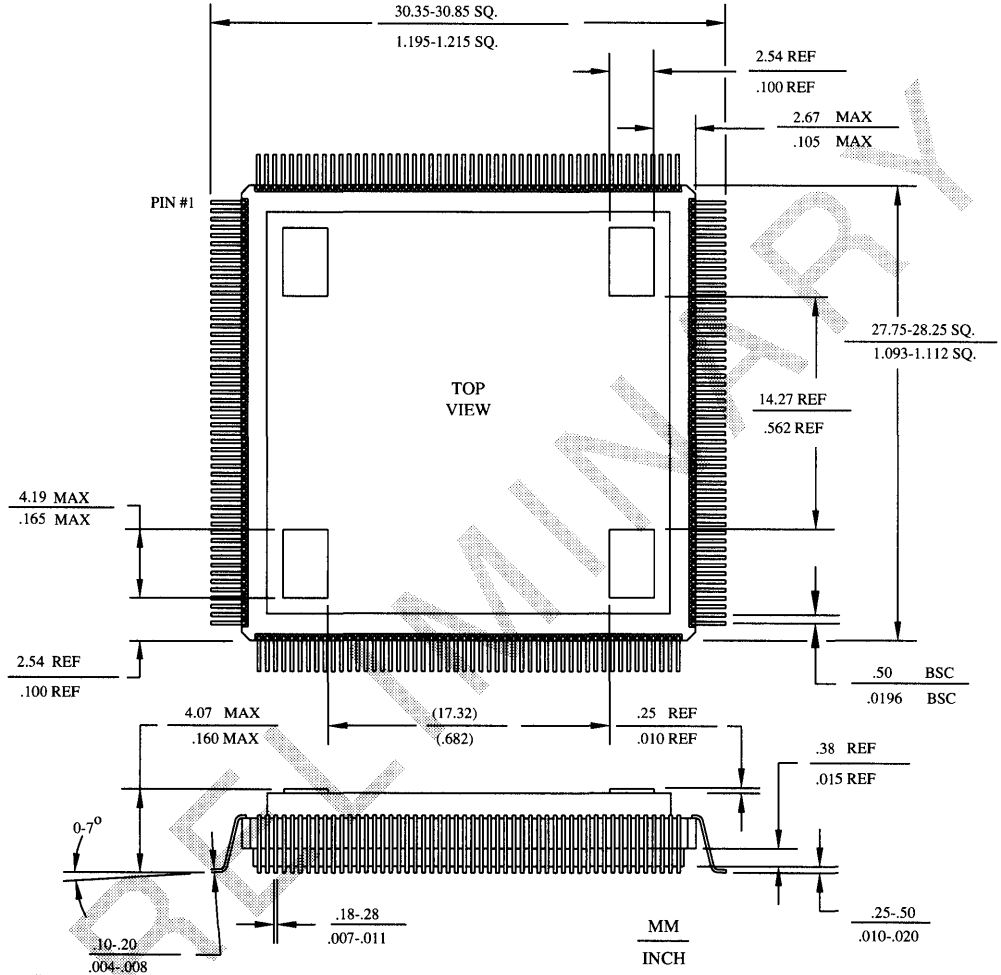
All unlisted pins are for general I/O

* No Connect
† Connect to GND if not using JTAG Reset
‡ Connect to GND
** Connect to Vcc

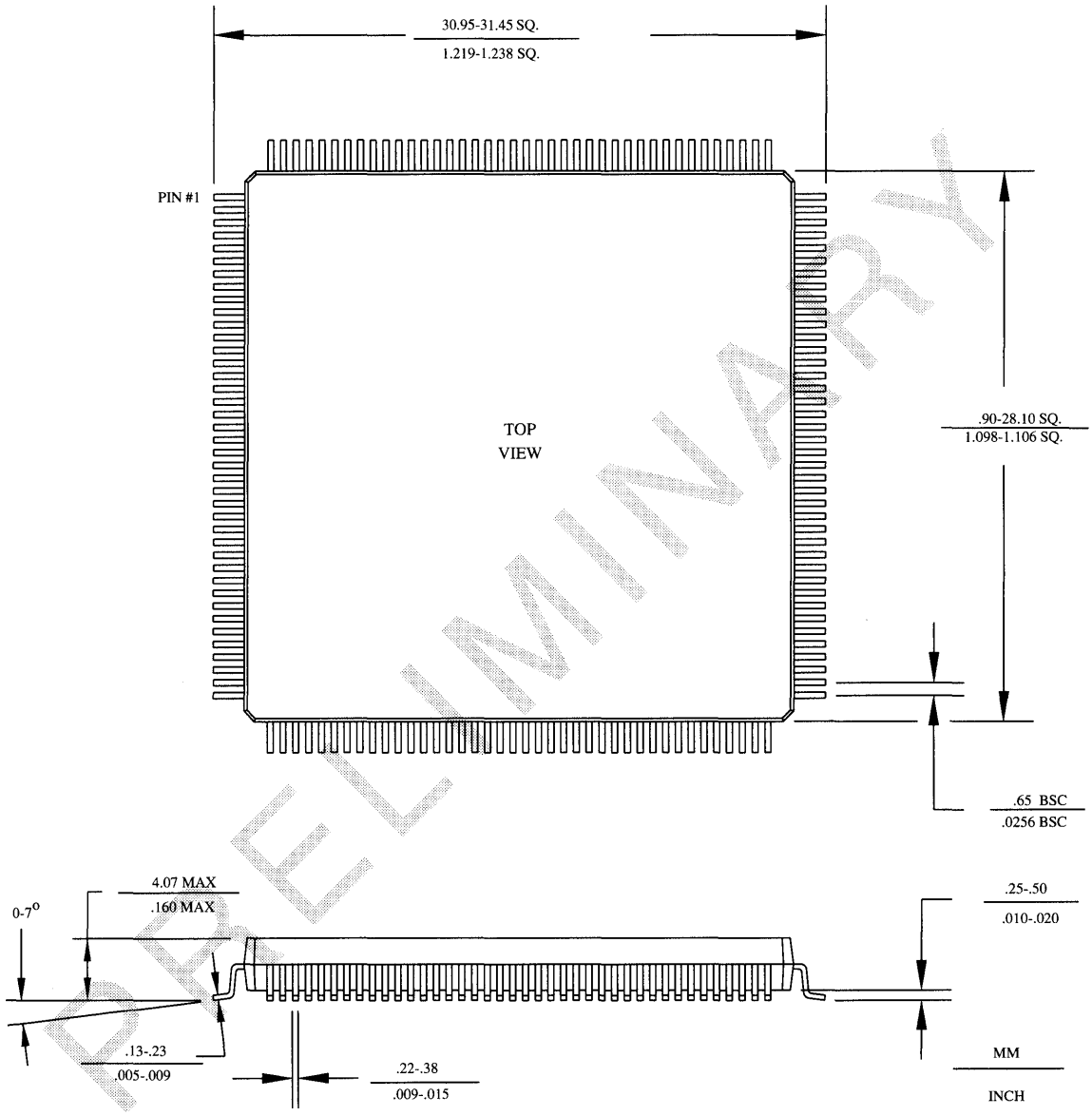
160 CQFP Package Dimensions



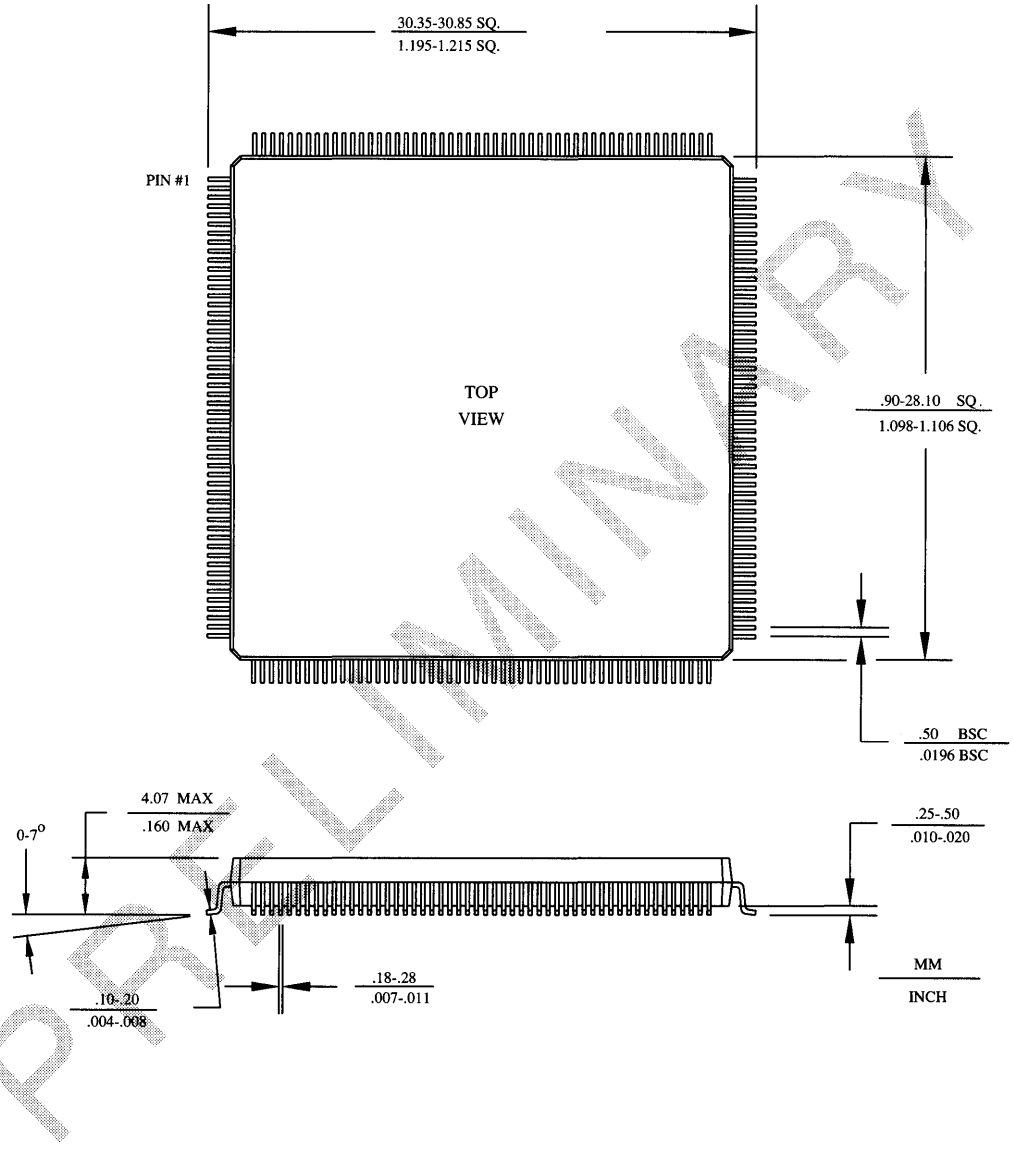
208 CQFP Package Dimensions



160 PQFP Package Dimensions

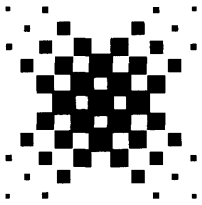


208 PQFP Package Dimensions



Chapter 6

Product Ordering Guidelines



Part Numbering Scheme

CP 20420 CPGA 155 A - 1 C

Part Number Prefix: CP

Part Number:

2.2K Gates -	20220
4.2K Gates -	20420
8.4K Gates -	20840
12K Gates -	21200
16K Gates -	21600
20K Gates -	22000

Package Type:

CLCC -	Ceramic Leaded Chip Carriers
CPGA -	Ceramic Pin Grid Array
CQFP -	Ceramic Quad Flat Pack
PQFP -	Plastic Quad Flat Pack
PLCC -	Plastic Leadless Chip Carrier

Pin Count:

Die Revision:

A
B

Speed Selection:

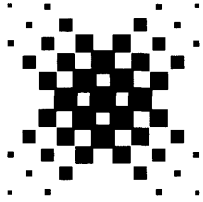
1 -	High Speed
0 -	Normal

Operating Temperature Range:

C -	Commercial (0^{o} to 70^{o} C)
I -	Industrial (-40^{o} to 85^{o} C)
M -	Military (-55^{o} to 125^{o} C)

Chapter 7

Sales Offices, Representatives & Distributors



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Fax: (714) 258-1804

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S. Dakota

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