DATA BOOK

VOL 1

CRYSTAL

Analog/Digital Conversion IC's

1990

CRYSTAL
Semiconductor Corporation

DATA BOOK VOL 1
ANALOG/DIGITAL CONVERSION IC's

MODEL INDEX

Crystal Semiconductor brings the benefits of leadership, high quality, analog VLSI solutions to our customers.

Crystal Semiconductor Corporation

Data Acquisition Data Book

LIFE SUPPORT AND NUCLEAR POLICY

CRYSTAL SEMICONDUCTOR PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF CRYSTAL SEMICONDUCTOR.

Life Support Systems are equipment intended to support or sustain life and whose failure to perform when properly used in accordance with instructions provide can be reasonably expected to result in personal injury or death. Users contemplating applications of Crystal Semiconductor products in Life Support Systems are requested to contact Crystal Semiconductor factory headquarters to establish suitable terms and conditions for these applications. Crystal Semiconductor's warranty is limited to replacement of defective components and does not cover injury to persons or property or other consequiential damages.

Examples of devices considered to be life support devices are neonatal oxygen analyzers, nerve stimulators (whether used for anasthesia, pain relief, or other purposes), autotransfusion devices, blood pumps, defibrillators, arrhythmia detectors and alarms, pacemakers, hemodialysis systems, pertoneal dialysis systems, neonatal ventilator incubators, ventilators for both adults and infants, aneshesia ventilators, and infusion pumps, as well as other devices designated as "critical" by the FDA. The above are examples only and are not intended to be conclusive or exclusive of any other life support device.

Examples of nuclear facility applications are applications in (a) a nuclear reactor, or (b) any device designed or used in connection with the handling, processing, packaging, preparation, utilization, fabricating, alloying, storing, or disposal of fissionable material or waste products thereof.

CONTENTS

COMPANY INFORMATION

Crystal's proprietary SMART Analog™ design technique, incorporating analog and digital circuitry in monolithic CMOS devices, represents a powerful new technology in the semiconductor industry. This innovative approach to design eliminates many of the sources of inconsistent performance in traditional analog circuitry.

Maximum system performance is built-in from initial research on end-user requirements through product definition. Product quality and reliability is designed into the device architecture and is further assured through rigorous standards for fabrication, assembly and testing. Crystal's part numbering scheme is as follows:

CSLXXXX - TPNNH/R

DEVICE REVISION: DOES NOT APPEAR HERE ON PACKAGE MARK.
REVISION IS COVERED IN DATE CODE STAMP.
USED ONLY FOR ORDERING/TRACKING.

SPECIAL HANDLING ,ALPHA ONLY A-COMMERCIAL HIGH-REL
B-MILITARY 883B REV. C PROCESSING

ELECTRICAL OR SPEED SPECIFICATION. (OPTIONAL) UP TO 2
NUMERIC DIGITS. NO ALPHA CHARACTERS. SEE DATA SHEET

PACKAGE CODE -REQUIRED ,ALPHA CHARACTER ONLY,NO NUMERICS

P = PLASTIC DIP	S = 0.3" SOIC
C = CERAMIC SIDEBRAZE	E= CERAMIC LCC
D = CERDIP	J= J-LEAD CERAMIC CHIP CARRIER
L = PLASTIC LEADED CHIP CARRIER,J LEAD	G= GULLWING CERAMIC CHIP CARRIER
U= UNPACKAGED DIE	

TEMPERATURE SPECIFICATION - REQUIRED,ALPHA CHARACTER ONLY
SIGNAL CONDITIONING/COMMUNICATION:
BLANK = 0 °C to 70 °C
I = -40 °C to 85 °C
M = -55 °C to 125 °C

TEMPERATURE/ACCURACY - REQUIRED,ALPHA CHARACTER ONLY
DATA ACQUISITION:

TEMPERATURE	ACCURACY		
	GOOD	BETTER	BEST
0 °C to 70 °C	J	K	L
-40 °C to 85 °C	A	B	C
-55 °C to 125 °C	S	T	U

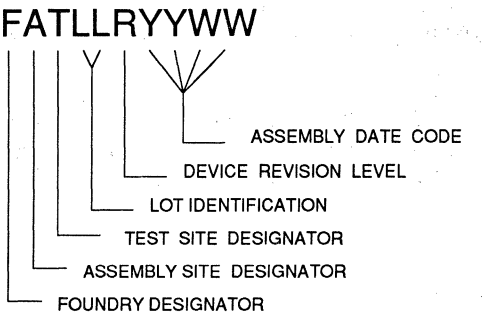
UP TO FOUR ALPHANUMERIC DIGITS COMPRISE REMAINDER OF BASIC PART NUMBER

CRYSTAL PRODUCT LINE (PROPRIETARY PARTS; SECOND-SOURCE PARTS HAVE EXCEPTIONS):
3 = DATA ACQ. SUPPORT CIRCUITS
4 = D/A CONVERTERS
5 = A/D CONVERTERS
6 = TELECOMMUNICATIONS
7 = SIGNAL CONDITIONING
8 = DATACOMMUNICATIONS

CRYSTAL SEMICONDUCTOR
"CS" = ALL CRYSTAL PRODUCTS;EXCEPT FOR
"CXT" = QUARTZ CRYSTALS
"CDB" = EVALUATION BOARD
"CX" = CUSTOM PRODUCTS

REV3

In addition to the part number, all Crystal parts have a second line of marking, which can be decoded as follows:



LOT CODE IDENTIFIER - TWO DIGIT ALPHA CHARACTER. IDENTIFIER SEQUENCE WILL BEGIN WITH AA,AB,AC, ETC. EACH LOT WILL RECEIVE A UNIQUE IDENTIFIER REGARDLESS OF DEVICE OR START DATE. SEQUENCE BEGINS AGAIN WITH AA WHEN ZZ HAS BEEN UTILIZED.

COMPANY BACKGROUND

Crystal Semiconductor Corporation was founded in 1984 with the goal of supplying the industry with high-performance, mixed analog/digital CMOS circuits.

To meet its objectives, Crystal recruited a staff of renowned CMOS analog design engineers, a scarce resource in the industry, and teamed them with designers trained in system architecture development.

By coupling this design staff with highly qualified application and test engineers and seasoned management, Crystal has achieved several industry firsts. Systems designers now benefit from the performance and cost savings of Crystal breakthroughs such as self-calibrating ADCs, a universal filter, monolithic T1 interfaces and the industry's first implementations of "delta sigma" oversampling A-to-D converters.

Headquartered in Austin, Texas, Crystal sells its products worldwide through a network of manufacturer's representatives. Crystal's entire marketing and sales organization is committed to providing quality products and reliable, rapid service.

QUALITY AND RELIABILITY INFORMATION

Crystal Semiconductor is committed at every level of the company to the highest possible standards of quality and reliability in its products. This committment is evident in all phases of operations: initial product definition, design, fabrication, assembly, test, qualification and customer service. Product quality and reliability is an active concern of each Crystal employee.

In Product Definition

To ensure maximum system performance, Crystal works with users to identify and quantify the parameters, including quality and reliability issues, that best serve customer needs. Quality and reliability become part of the design goals, along with electrical performance and cost.

In Design

Conservative 3-micron CMOS design rules are the basis for all current Crystal products. In addition, extensive use is made of proven standard cells to drastically reduce the possibility of design errors.

Each pin in every SMART Analog product is designed to meet ESD levels of at least 2500V when tested per MIL STD 883C, Method 3015. Each pin is also designed to withstand more than 200mA of DC latch current.

Crystal SMART Analog design architectures provide quality and reliability comparable to leading digital devices and memories. This is far superior to traditional analog ICs and hybrids. On-chip digital error correction provides stable performance over time and temperature by taking advantage of digital controls that are insensitive to parametric analog problems such as leakages and shifts in threshold voltage. Using Crystal devices, designers have fewer error sources to consider. The result is a less complicated, more reliable system.

In Fabrication and Assembly

Crystal ensures reliable delivery of quality parts by accessing established foundries in multiple locations (Japan and California today). Each fabrication facility is qualified by Crystal. Assembly is performed both domestically and offshore under carefully documented and well-controlled conditions.

Wafer fabrication and assembly processes undergo in-line quality inspections. Wafers are inspected optically to guidelines based on MIL STD 883C, Method 2010. Each die is electrically tested using proprietary test circuits that verify key parameters. Following assembly, packages are subjected to a variety of mechanical inspections to verify integrity and insure high quality. (For example, x-ray inspection to 3.0 percent LTPD is one of the standard production tests.)

In Test

In a break from traditional analog components, Crystal's SMART Analog products include basic test capabilities designed into each chip. Crystal's in-process quality assurance program uses this designed-in testability to monitor and track the performance and quality of these complex circuits. Finished packaged components are tested 100 percent electrically, over temperature where critical parameters are involved. With these extensive quality programs, Crystal guarantees outgoing electrical quality levels on all data sheet specifications to a 0.065 percent AQL level over the full specified temperature range.

Throughout the assembly and test phases, traceability to the original wafer lot is carefully maintained.

In Product Qualification

Before any Crystal product is released to production and shipped in volume, it must undergo a thorough qualification program. Crystal has separate qualification criteria to address both long-term reliability and infant mortality so that the sources of failure are identified and eliminated. Crystal uses military specifications as the guidelines for reliability tests, methods and procedures. (See Table 1.)

To ensure reliability of the design and processes, full qualification requires that three non-consecutive lots are used during the qualification program. Fabrication and assembly facilities are audited every six months and periodically monitored. Any major design or process changes restart the qualification procedure.

These steps guarantee that Crystal products maintain the high standards of reliability designed-in from the start.

TABLE 1 - QUALIFICATION TESTS

TEST	MIL STD 883C METHOD	CONDITION	INFANT MORTALITY TESTS		LONG-TERM RELIABILITY TESTS		
			DURATION	PASS/FAIL CRITERION	DURATION	PASS/FAIL CRITERION	CRYSTAL GOAL
OPERATING LIFE	1015 COND D	+125°C, Dynamic Bias +/-5.5V Supplies	168 hrs	0.25%	1000 HRS	75 FITS†† (25°C/60%UCL 1.0 eV Act. Energy)	10 FITS† (25° C/ 60% UCL)
TEMPERATURE HUMIDITY STRESS (Plastic Parts)		+85°C/85% RH Static Bias	168 hrs	1.0 LTPD	1000 HRS	3.0 LTPD	1.0 LTPD
TEMPERATURE CYCLING Hermetic Packages	1010.5 COND C	-65°C to + 150°C Then Gross Leak Test	100 CYCLES	1.0 LTPD	1000 CYCLES	3.0 LTPD	1.0 LTPD
TEMPERATURE CYCLING Molded Packages	1010.5 COND B or *	-55°C to + 125°C or -40°C to + 125°C	100 CYCLES	1.0 LTPD	500 CYCLES	3.0 LTPD	1.0 LTPD
THERMAL SHOCK	1011.4 COND B or **	-55°C to + 125°C or -40°C to + 125°C *** Then Gross Leak Test	100 CYCLES	1.0 LTPD	500 CYCLES	3.0 LTPD	1.0 LTPD
AUTOCLAVE (Plastic Parts)		+121°C/100% RH 2 Atmosphere, No Bias	48 HRS	1.0 LTPD	144 HRS	3.0 LTPD	1.0 LTPD
CENTRIFUGE	2001	30 Kg/Y1 Axis				5.0 LTPD	1.0 LTPD
ELECTROSTATIC DISCHARGE	3015			1500V-0 Fail	5 UNITS, ALL PINS	1500V-0 FAIL	4000V
LATCH UP		dc Current		100 mA-0Fail	5 UNITS, ALL PINS	100mA-0 FAIL	200mA

* JEDEC STD 22-B, A104 COND B
** JEDEC STD 22-B, A106 COND C
*** For hermetic Packages Only
† Equivalent to 50 FITS, 70°C/60% UCL, 0.7 eV
†† Equivalent to 300 FITS, 70°C/60% UCL, 0.7 eV

In Customer Service

Compliance with purchasing requirements is ensured through the use of Crystal's computerized system "Compass"(Crystal On-line Marketing Production and Sales System). This processing system ensures that all orders are entered correctly, scheduled properly, produced according to schedule, and shipped with zero discrepancies.

All systems and procedures at Crystal Semiconductor are aimed at continously improving the quality and reliability of our products and services to meet the needs of our customers.

Crystal's philosophy on quality is to anticipate problems and develop systems and controls to alleviate possible problems. It is a well stated fact by Juran and Deming, two of the nation's foremost experts on quality, that 85% of all quality problems are system related and 15% are worker related. Therefore, Crystal devotes its major quality efforts toward preventing system related quality problems.

Crystal has a very aggressive audit program in place. Monthly internal audits are performed to insure compliance to the extensive documentation of instructions and criteria for testing and inspection. Semiannual vendor audits are performed on the assembly and fabrication foundries. Vendor audits insure the adequacy and compliance of specifications, product flow, training, process controls and cleanliness. All internal and external audits have provisions for ratings and a system for corrective action requirements. These frequent audits by assembly, fabrication and quality engineers maximize system quality compliance.

As an added measure of continued high quality from assembly and fabrication foundries, thorough incoming inspections are performed. Wafer level optical inspection is based upon guidelines of MIL STD 883C, METHOD 2010. Test die are electrically tested to verify compliance to key process parameters based upon design rules specifications. These electrical parameters include threshold voltages, breakdown voltages, material resistance, and contact resistance. Assembly packaging inspection includes external visual, marking permanency, solderability, x-ray, hermeticity, die shear, wirepull and internal visual.

Preventive measures are very much in force in the final test area. Equipment calibration and preventive maintenance procedures are strictly adhered to. Handling procedures for Electrostatic Discharge are in place throughout the test areas. Non-conforming material is segregated until corrective action is agreed upon. There are controlled procedures for releasing new test programs and new test equipment to the production environment. In summary, Crystal Semiconductor is committed to meet the quality requirements of its customers.

• Notes •

T1, PCM-30 and ISDN Primary Rate Line Interface Circuits

Crystal Semiconductor offers a broad family of CMOS PCM line interface circuits, with each device optimized for a unique system application. The CS6152, CS6159, CS61535 and CS61574 are recommended for use in new designs.

Since introducing the industry's first T1 and PCM-30 line interface circuits (the CS61534 and CS61544), we have shipped more CMOS PCM line interface ICs than any other vendor worldwide. Crystal Semiconductor's leadership continues with the best in pulse shapes, jitter attenuation, jitter tolerance and low power dissipation.

Product	CS6152	CS6159	CS61535	CS61574
Application	T1	T1 & PCM-30	T1 & PCM-30	T1 & PCM-30
Receiver Functions	Data Slicer	Clock & Data Recovery	Clock & Data Recovery	Clock & Data Recovery & Jitter Attn
Transmitter functions	Low Power Driver	Low Power Driver	Jitter Atten. & Driver	Driver
Serial Control Port	-	-	yes	yes
DIP Package	24-pin, 300 mil	24-pin, 300 mil	28-pin, 600 mil	28-pin, 600 mil

No one has a wider family of line interface IC's.

CS6152: Basic DSX-1 driver and receive buffer. For low power cards using digital-ASIC clock recovery. Ideal for trunk card bays where T1 density is limited by heat dissipation.

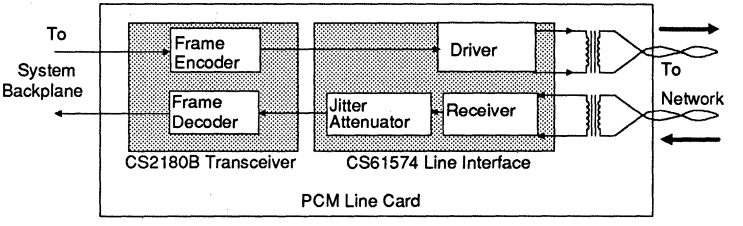
CS6159: Ideal for large synchronous systems such as central offices and DCS 0/1, which need the lowest cost per line, small package and low power dissipation.

CS61535: Enhanced transmit-side jitter attenuator supports SONET VT1.5 and VT2, and other high speed transmission systems such as digital microwave radio.

CS61574: Receive-side jitter attenuation supports loop-timing in customer-premises equipment (which needs to meet AT&T 62411) and in channel banks.

T1 Transceiver

Crystal Semiconductor's CS2180B T1 Transceiver is a perfect companion to our T1 line interface ICs. This device handles encoding and decoding of all T1 frame formats (D4, SLC-96 and T1DM and ESF). Serial interface and control registers make it simple to configure from a microprocessor, including per-channel control options. Packages available include 40-pin DIP or 44-lead PLCC.



The CS2180A is ideal for use with Crystal's family of line interface IC's

Jitter Attenuation Circuits

Crystal Semiconductor's jitter attenuation technology is available stand alone for a wide variety of applications. The CS61600 is ideal for T1 and PCM-30 applications while the CS80600 attenuates jitter in T2, 2nd-level CEPT lines and Token Ring LANs.

Quartz Crystals

To compliment our family of T1 line interface circuits, Crystal Semiconductor now supplies pullable quartz crystals. The CXT6176 and CXT8192, are designed for 100% compatibility with our PCM line interface and jitter attenuator circuits.

Optical Data Links

Crystal Semiconductor has smashed through cost barriers for fiber optic links with new low-cost bi-directional OPTIMODEMS™. The CS8123 and CS8124 support full-duplex voice and data communications at speeds to 256 kbps, while using just one optical component at each end of the link. The CS8125 and CS8126 transmitter replace expensive hybrids with CMOS ICs to provide T1 links over a fiber pair. The CS8127 is a unique light Emitting and Detecting diode for use with OPTIMODEMS™.

Applications for the family of optical data links include: secure (TEMPEST) communication of voice and data at ISDN data rates, communication in electrically - noisy environments such as a factory floor, links where the physical size and weight of cables and connectors are a concern, and inter-building connections which require lightning immunity.

Ethernet

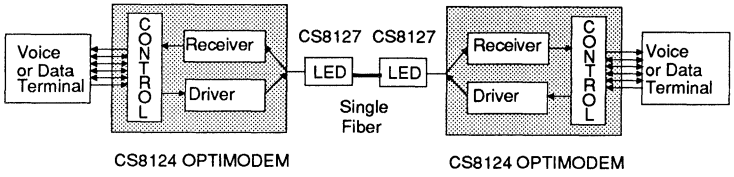
Crystal Semiconductor will be introducing a complete family of circuits for Ethernet applications. Included in the family is the CS83C92A, the industry's first low-power CMOS transceiver, the CS8023 Serial Interface Adaptor, and the CS8005 CSMA/CD controller, which supports 10 Mbps throughput and 64 kbytes of local packet buffers.

AES/EBU Transmitters and Receivers

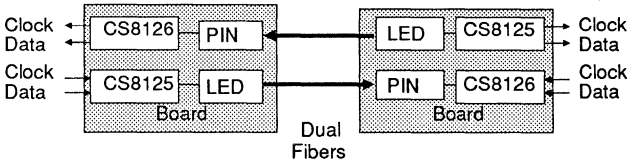
The CS8401/2 AES/EBU transmitters, along with the CS8411/2 AES/EBU receivers, allow digital communication between audio equipment. Requiring minimum external circuitry, these IC's support both professional and consumer formats.

DTMF Receivers

Crystal Semiconductor has improved on industry standard DTMF receiver ICs while maintaining 100% pin compatibility. Our device features on-chip filters which offer the best possible signal-to-noise ratio allowing highly accurate decoding of telephone tones.



The OPTIMODEM™ is a powerful optical data link for a variety of applications.



T1 Rate (1.544 MBit/s) Bi-Directional Link

CONTENTS

See the Crystal Telecommunications Data Book for the complete data sheets on the above products

Semiconductor Corporation

CS202/3

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Detects 12 or 16 DTMF Tone Pairs
- Uses Inexpensive 3.579 MHz Colorburst Crystal
- Hex or Binary 2-of-8 Output
- Synchronous or Handshake Controlled Output
- Built-in Filter for Dial Tone Rejection
- 18 Pin Package
- Single 5 Volt ±10% Power Supply
- Early Detect Output
- Pin Compatible with SSI 202/SSI 203

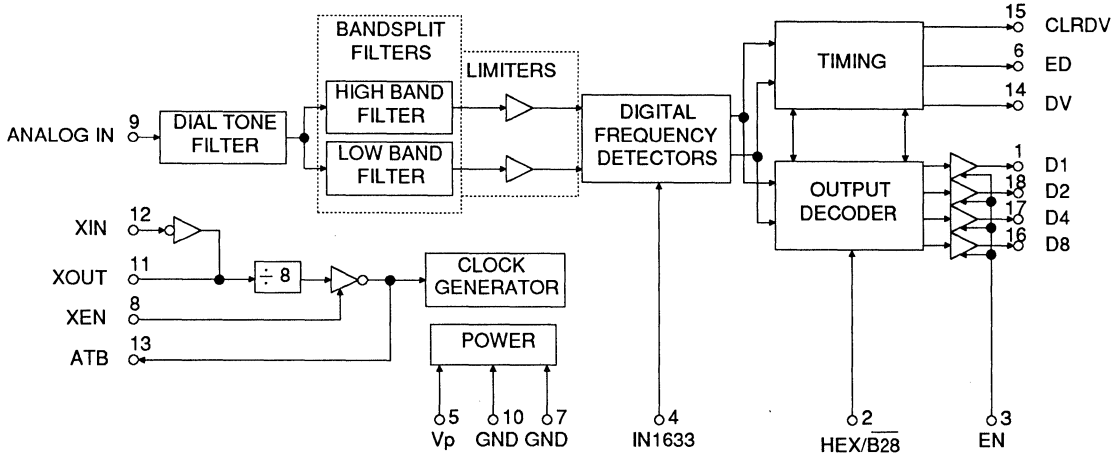
General Description

The CS202 and CS203 are fully integrated DTMF (Dual Tone Multifrequency) receivers that decode the tone pairs used in standard dialing schemes. All of the functions needed for decoding the tone pairs are implemented using Crystal's double-poly CMOS process for low power and high performance.

ORDERING INFORMATION

CS202-P - 18 Pin Plastic DIP
CS203-P - 18 Pin Plastic DIP
All standard 300 mil DIPs

Block Diagram



CRYSTAL
Semiconductor Corporation

CS2180B
CS2180A

T1 Transceivers

Features

- Monolithic T1 Framing Device
- Both Transceivers support D4 and ESF framing formats
- CS2180B also supports SLC-96 and T1DM framing formats
- CS2180B has updated AIS and Carrier Loss detection criteria
- CS2180B is Plug Compatible with CS2180A, DS2180A and DS2180

General Description

The CS2180A and CS2180B are monolithic CMOS devices which encode and decode T1 framing formats. The devices support bit-seven and B8ZS zero suppression, and bit-robbed signaling. Clear channel mode can be selected on a per channel basis.

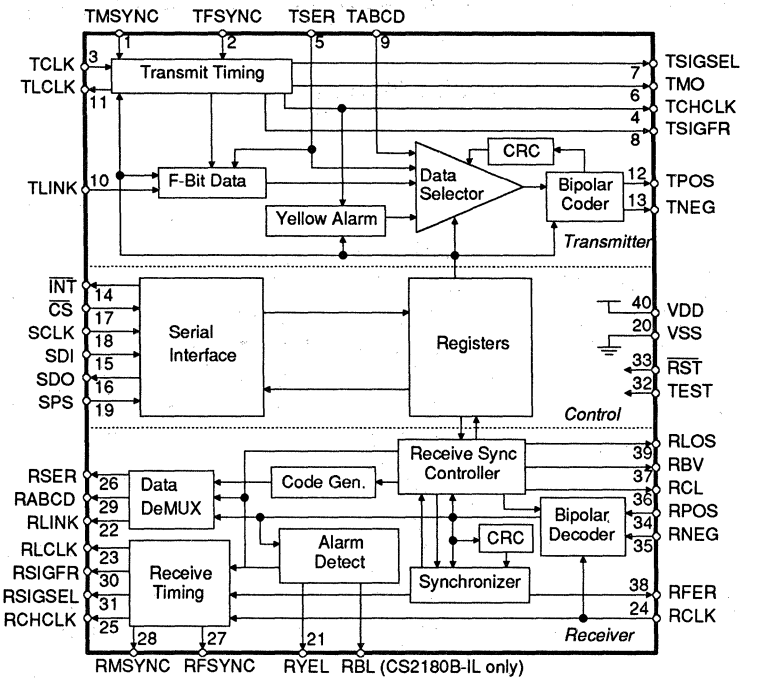
The serial interface has been enhanced to allow the CS2180A and CS2180B to share a chip select signal and register address space with the CS61534/35/74 PCM Line Interface device.

Applications

- T1 Line Cards
- ISDN Primary Rate Line Cards

Ordering Information:

CS2180B-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180B-IL	44 Pin PLCC	-40 to 85 °C
CS2180A-IP	40 Pin Plastic DIP	-40 to 85 °C
CS2180A-IL	44 Pin PLCC	-40 to 85 °C



Semiconductor Corporation

CS6152

Low Power PCM Analog Interface

Features

- Provides Analog T1 Line Interface
- Low Power Consumption (normally 180 mW)
- EXPERT *Pulse* ™ Programmable Pulse-Shaping Line Driver
- Provides Receiver AMI-to-TTL Buffer Which Compliments Digital Gate Array Clock-Recovery Circuits
- Driver Performance Monitor
- Minimal External Components
- Upwards Compatible From CS61534

General Description

The CS6152 combines the analog transmit and receive line interface functions for T1 system interface in one device. The T1 analog interface operates from a 5 Volt supply, and is transparent to the T1 framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape at the DSX-1 cross-connect for line lengths ranging from 0 to 655 feet. The device provides the ideal front-end to digital gate array based clock recovery circuits.

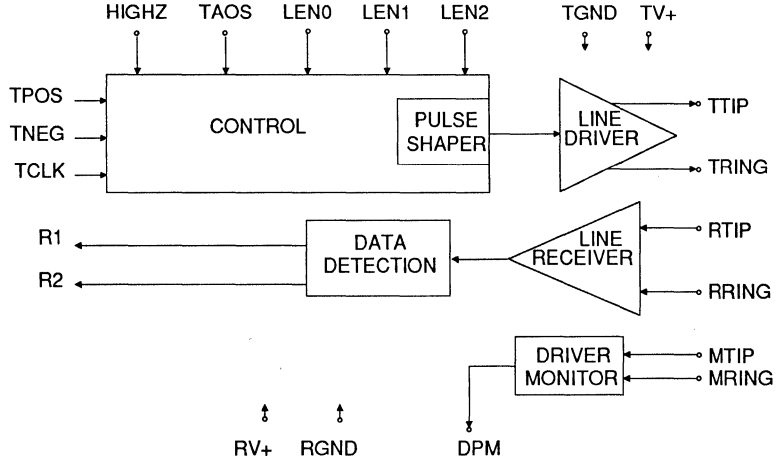
Applications

- Interfacing Network Equipment such as Multiplexors, Channel Banks and Switching Systems to a DSX-1 Cross Connect.
- Interfacing Customer Premises Equipment such as PABX's, T1 Multiplexors, Data PBX's and LAN Gateways to a Channel Service Unit or T1 modem.

ORDERING INFORMATION

CS6152-IP	-	28 Pin Plastic, 600 mil DIP
CS6152A-IP	-	24 Pin Plastic, 300 mil DIP
CS6152-IL	-	28 Pin J-lead PLCC

Block Diagram



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS6159

Low Power PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Internal generation of transmitted T1 pulse width and pulse shape. Pulses meet template requirements over full power supply and temperature range.
- Fully Monolithic Clock Recovery
- Minimum External Components

General Description

The CS6159 combines the analog transmit and receive line interface functions for a T1 or PCM-30 interface in a 24-pin skinny-DIP or SOIC device. The line interface operates from a single 5 volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for line lengths ranging from 0 to 655 feet from a DSX-1 cross connect.

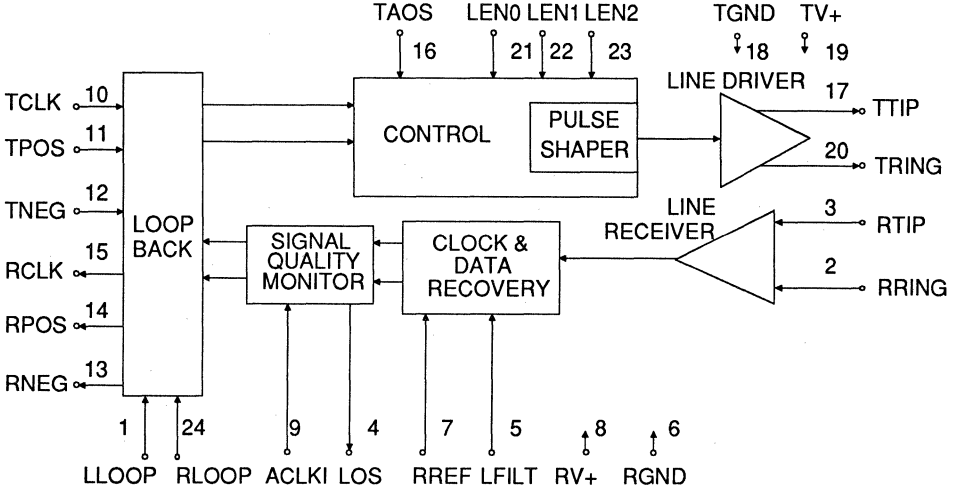
Applications

- Central Office Exchanges
- Digital Access and Cross Connect Systems
- Customer Premises Equipment
- PABX's

Ordering Information

CS6159-IP1 24 Pin Plastic DIP (300 mils) T1 & PCM-3(
CS6159-IS1 24 Pin SOIC (300 mils) T1 & PCM-3(

Block Diagram



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Semiconductor Corporation

CS61535

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and PCM-30 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- Jitter Tolerance of Receiver: 0.4 UI's to 100 kHz
- Microprocessor Controllable
- Compatible with SONET, CCITT G.742, and Other Async. Muxes
- CS61534 Compatibility

General Description

The CS61535 combines the analog transmit and receive line interface functions for a T1/PCM-30 interface in a single 28 pin device. The line interface operates from a single 5 volt supply and is transparent to the framing format. Crystal's EXPERT *Pulse*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CCITT G.703, or for connecting to DSX-1 cross connects for line lengths ranging from 0 to 655 feet. The transmitter uses a 32-bit elastic store to remove jitter from the transmit data.

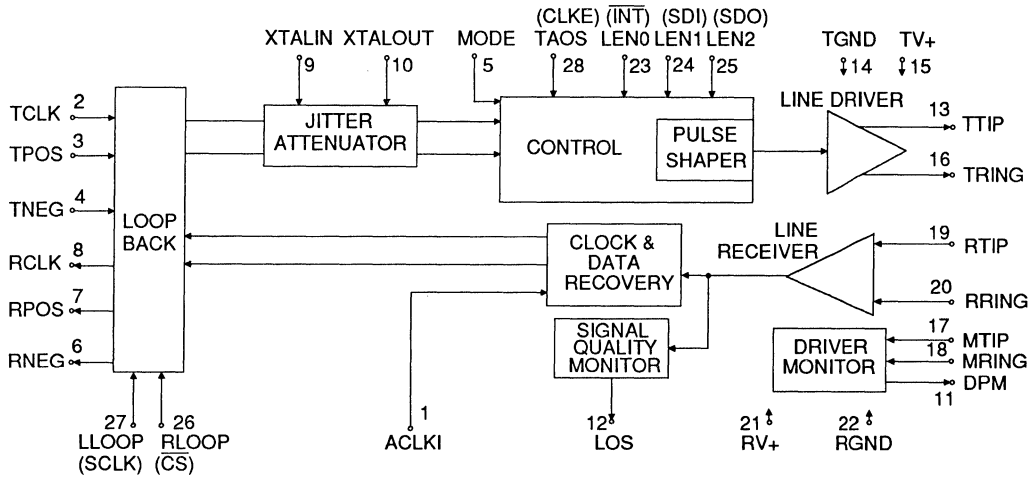
Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.
- Interfacing to PCM-30 links.

Ordering Information

CS61535-IP	28 Pin Plastic DIP T1 only
CS61535-IP1	28 Pin Plastic DIP T1 & PCM-30
CS61535-IL	28 Pin PLCC (j-leads) T1 only
CS61535-IL1	28 Pin PLCC (j-leads) T1 & PCM-30

Block Diagram



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Semiconductor Corporation

CS61574

PCM Line Interface

Features

- Provides Analog PCM Line Interface for T1 and 2.048 MHz Applications
- Provides Line Driver and Data Clock Recovery Functions
- Jitter Attenuation Starting at 6 Hz with >300 UIs of Tolerance in Attenuator
- Jitter Tolerance of Receiver: 0.4 UIs to 100 kHz
- Microprocessor Controllable
- Compatible with CSUs and DACSs
- CS61534 Compatibility Mode
- Diagnostic Features

General Description

The CS61574 combines the analog transmit and receive line interface functions for a T1/CEPT interface in a 28 pin device. The line interface operates from a single 5V supply and is transparent to the framing format.

Crystal's SMART *Analog*™ circuitry shapes the transmit pulse internally, providing the appropriate pulse shape for CSUs or for connecting to PCM cross-connects for line lengths ranging from 0 to 655 feet. Maximum range is greater than 1500 feet. The receiver uses an elastic store to remove jitter from the incoming data.

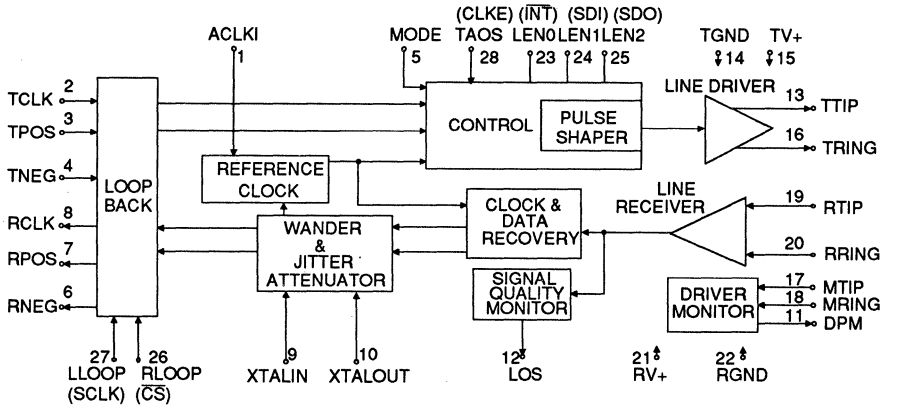
Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

ORDERING INFORMATION

CS61574-IP	-	28 Pin Plastic DIP; T1 only
CS61574-IP1	-	28 Pin Plastic DIP; T1 and CEPT
CS61574-IL	-	28 Pin PLCC (j-leads); T1 only
CS61574-IL1	-	28 Pin PLCC (j-leads); T1 and CEPT

Block Diagram



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Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 TWX: 910-874-1352

Semiconductor Corporation

CS61600

PCM Jitter Attenuator

Features

- Unique Clock-Tracking Circuitry Filters 50 Hz or Higher Frequency Jitter for T1 and PCM-30 Applications
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS61600 from Crystal Semiconductor accepts T1 (1.544 Mb/s) or CCITT standard (2.048 Mb/s) data and clock inputs, and tolerates at least 7 (and up to 14) unit intervals, peak-to-peak, of jitter. Before outputting data and clock, jitter is attenuated using an internal clock-tracking variable oscillator and a 16 bit FIFO elastic store.

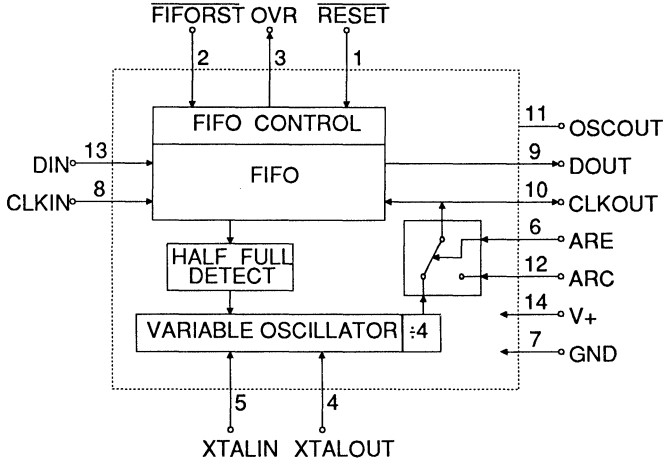
The jitter attenuation function can be determined by appropriate specification of the external crystal.

The CS61600 is transparent to data format, and is intended for application in carrier systems, switching systems, Local Area Network gateways and multiplexers.

ORDERING INFORMATION

CS61600-IP - 14 Pin Plastic DIP; T1 only
CS61600-IP1 - 14 Pin Plastic DIP; T1 and CCITT

Block Diagram



Semiconductor Corporation

CXT6176
CXT8192

Pullable Quartz Crystals

Features

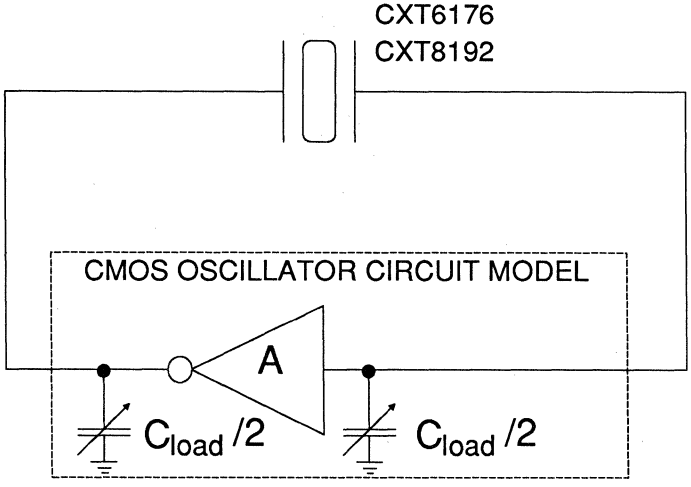
- Complements CS615x4 PCM Line Interface integrated circuits and CS61600 PCM Jitter Attenuator.
- Crystal's operating frequency is a function of variable load capacitance provided by CS615x4 Line Interface or CS61600 Jitter Attenuator.

Description

Crystal Semiconductor's line interface and jitter attenuator IC's require unique performance specifications for the crystals. The CXT6176 and CXT8192 are built to meet Crystal's specifications for T1 and PCM-30 applications respectively.

Ordering Information

CXT6176	Crystal for T1 Applications
CXT8192	Crystal for PCM-30 Applications



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS8005

CSMA/CD Ethernet Data Link Controller

Features

- High Throughput
  - Supports full 10M BPS data rate
  - Back-to-Back Packets
- 64 K-Byte Local Packet Buffer
  - Provides refresh for DRAMs
  - Off-loads host bus
- Conforms to ISO/ISEE 802.3 Standard
- Flexible Bus Interface
  - Intel and Motorola bus modes
  - I/O, string move, DMA access
  - Memory or I/O mapped
  - 8 or 16 bit bus width
- Recognizes One to Six Receive Addresses, Specific, Multicast or Broadcast
- Advanced Error Correction and Handling
  - Automatic re-transmit after a collision
  - Automatically discards bad packets

General Description

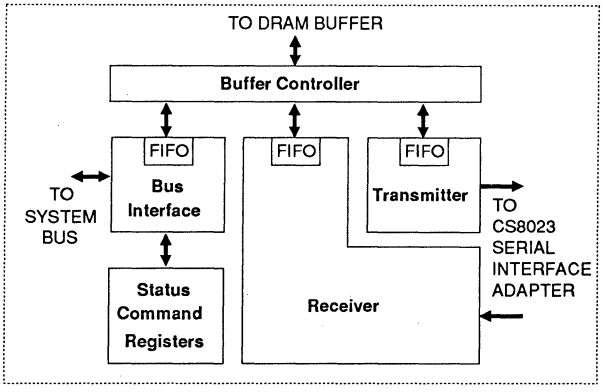
The CS8005 has five major blocks: the Transmitter, Receiver, Buffer Controller, Bus Interface and Status and Command Register.

The CS8005 supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, CRC generation/stripping, transmission deferral, collision handling and address recognition of up to 6 station addresses including multicast/broadcast addresses.

The Buffer Controller manages a 64K byte local packet buffer. This block provides arbitration and control for four memory ports: the transmitter, the receiver, the bus interface and an internal DRAM refresh generator. Received packets are temporarily stored until the system either reads or disposes of them, and packets placed there by the system are held for transmission over the link.

The Bus Interface interfaces to the system bus and provides access to internal configuration and status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of Packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called DMA FIFO. This permits high speed data transfers to occur even when the Buffer Controller is busy servicing the Transmitter or Receiver or refreshing the DRAM.

ORDERING INFORMATION:
Contact Crystal Semiconductor



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 455 7581

Semiconductor Corporation

CS8023A

Serial Interface Adapter

Features

- Compliant with IEEE 802.3 and Ethernet Rev. 1
- Works with the CS8005 and Intel 82586 LAN Controllers.
- Manchester Data Encoding/Decoding and Receiver Clock Recovery
- Loopback Capability for Diagnostics and Isolation
- Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission.
- Transceiver Interface High Voltage (16V) Short Circuit Protection
- Low Power CMOS Technology with Single 5V Supply.

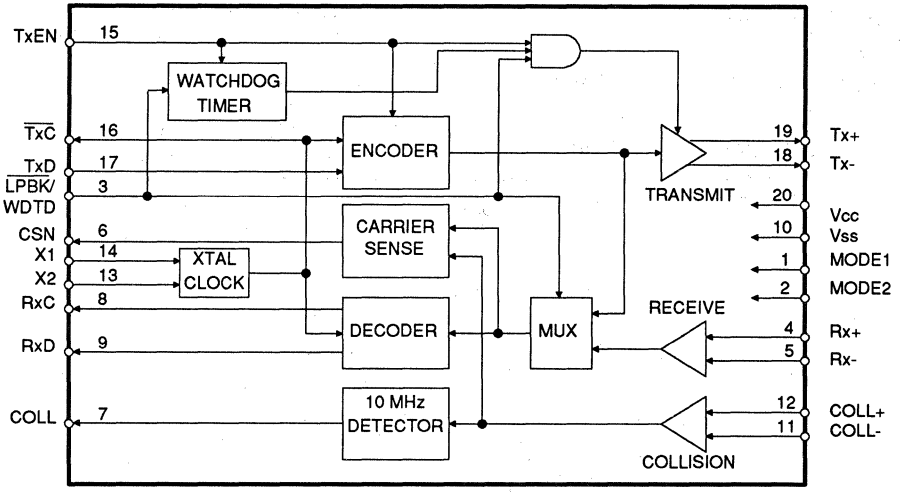
General Description

The CS8023A Serial Interface Adapter provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the CS8005 CSMA/CD Data Link Controller or to the Intel 82586 LAN Controller and any standard Ethernet transceiver as defined by IEEE 802.3 and Ethernet Revision 1.

The CS8023A is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the CS8023A includes a 25 millisecond watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

Together with the CS8005 and CS83C92, the CS8023A Serial Interface Adaptor provides a high performance minimum cost interface for any system to Ethernet.

ORDERING INFORMATION:
Contact Crystal Semiconductor



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS80600

High Speed Jitter Attenuator

Features

- Accepts Input Clock with Frequency of 4.5 MHz to 8.5 MHz
- Unique Clock-Tracking Circuitry
- Tolerates and Attenuates At Least 3 Unit Intervals of Jitter
- Minimal External Components Required
- 14 Pin DIP
- Single 5 Volt Supply
- 3 Micron CMOS for High Reliability and Low Power Dissipation: 50 mW Typical at 25 °C

General Description

The CS80600 from Crystal Semiconductor accepts 4.5 to 8.5 MHz clock and data inputs and removes up to ±3 data bits of jitter before outputting the data and clock. Jitter is removed using an internal clock tracking circuit and an 8-bit FIFO elastic store.

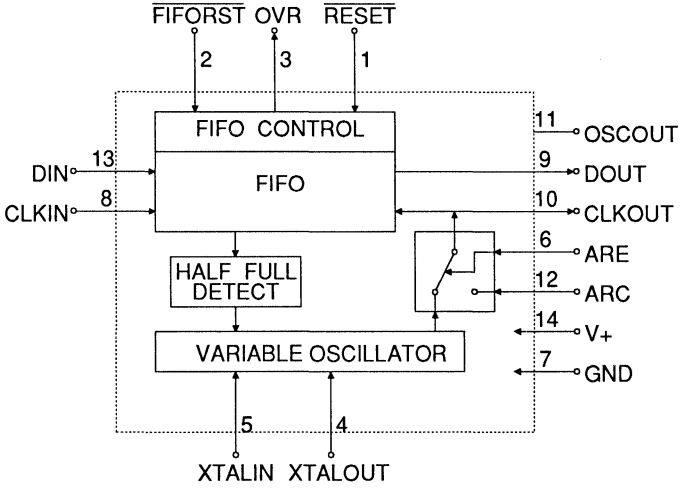
Applications

- **Token Ring:** The CS80600 can be used to eliminate the accumulation of data-pattern dependent jitter which is the primary factor limiting the size of token rings. The CS80600 is intended for application in station adaptor cards, in active wiring concentrators, and in repeators.
- **PCM:** TIC, T2, and CEPT2 and second order multiplexors.

ORDERING INFORMATION

CS80600-P - 14 Pin Plastic DIP

Block Diagram



Semiconductor Corporation

CS8123/4

OPTIMODEM™

Features

- Time Compression Multiplexing for full-duplex communication over a single optical fiber
- Synchronous operation from 2.4 kbps to 256 kbps
- Asynchronous operation from dc to 38.4 kbps
- 10^{-9} BER up to 1.3 km
- System diagnostic capabilities
- Four optional secondary control channels provide independent end-to-end transmission links
- Independent transmit and receive clocks

General Description

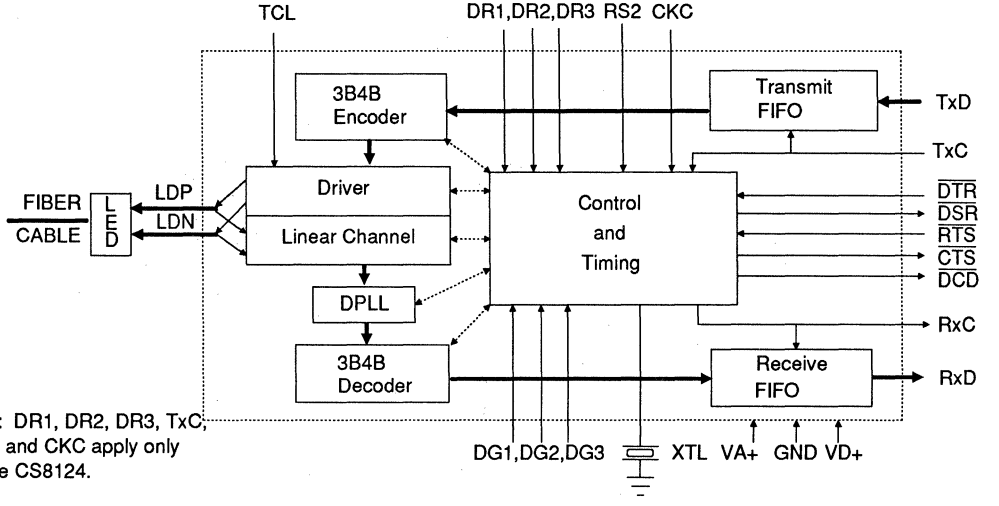
The CS8123 and CS8124 from Crystal Semiconductor Corporation are SMART *Analog*™ full-duplex modem devices that receive and transmit serial binary data over a single fiber-optic cable. Both devices provide the filtering, encoding, decoding, and data buffering to implement a "ping-pong" communication channel

The CS8123 device supports asynchronous communication. The CS8124 device supports asynchronous and synchronous communicatons. The RTS, CTS, DTR, and DSR control lines can be used for RS232C compatible modem control, or end-to-end transmission channels.

SMART *Analog* and OPTIMODEM are trademarks of Crystal Semiconductor Corporation.

Ordering Information

CS8123-IP	24 Pin 0.6" DIP*	* The 24-pin 0.6" package will be discontinued and replaced by the 24-pin 0.3" package. Lay out your PCB for both.
CS8123-IL	28 Pin PLCC	
CS8123A-IP	24 Pin 0.3" DIP	
CS8124-IP	24 Pin 0.6" DIP*	
CS8124-IL	28 Pin PLCC	
CS8124A-IP	24 Pin 0.3" DIP	



Note: DR1, DR2, DR3, TxC, RxC, and CKC apply only to the CS8124.

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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS8125/6

T1 Optical Line Interface

Features

- Supports Links at 1.544 MHz up to 5 km
- Supports both single-mode and multi-mode cable
- Receiver Sensitivity : 30 nA to 30 uA, -42 dBm (assuming R=0.5 nA/nW)
- Selectable Transmit Power Level, 10 mA to 100 mA
- Optical Dynamic Range of 30 dB
- Monolithic Clock Recovery
- 3B4B Line Encoding/Decoding

General Description

The CS8125 and CS8126 from Crystal Semiconductor Corporation are SMART Analog™ interface devices that receive and transmit serial binary data at T1 rates over two fiber-optic cables. Combined with an external LED and PIN diode, the CS8125/6 provide a low-cost, easy-to-design optical link. Functions included are 3B4B encoding/decoding, clock recovery, PIN diode amplification, and control of transmitter power.

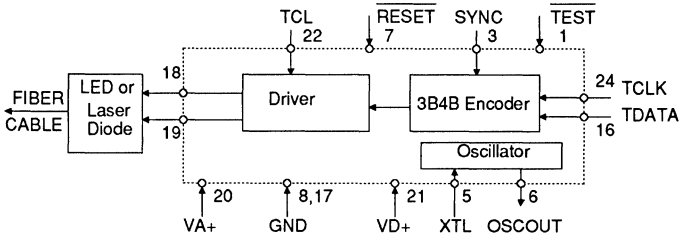
Applications

- Campus T1 Networks
- Secure T1 links
- T1 links in electrically noisy environment

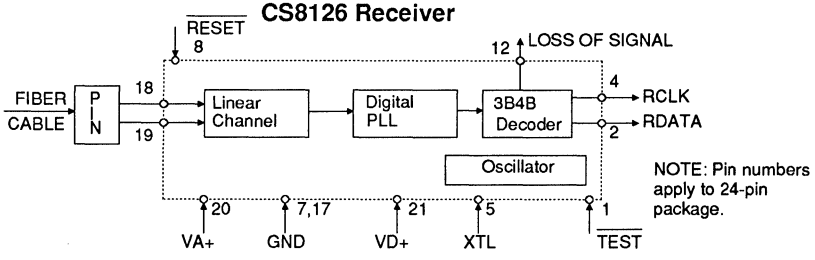
ORDERING INFORMATION

CS8125-IP	24 Pin 0.6" DIP*	*The 24-pin 0.6" package will be discontinued and replaced by the 24-pin 0.3" package. Lay out your PCB for both.
CS8125-IL	28 Pin PLCC	
CS8125A-IP	24 Pin 0.3" DIP	
CS8126-IP	24 Pin 0.6" DIP*	
CS8126-IL	28 Pin PLCC	
CS8126A-IP	24 Pin 0.3" DIP	

CS8125 Transmitter



CS8126 Receiver



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Crystal Semiconductor Corporation
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(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS8127

Light Emitting Diode

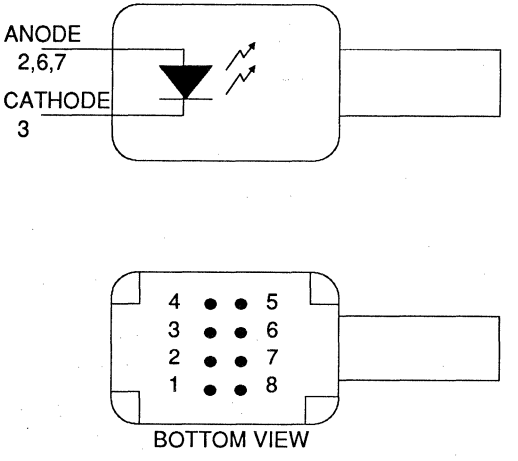
Features

- Supports bi-direction communication when used with the CS8123 and CS8124 OPTIMODEMs™
- Compatible with the CS8125 T1 Optical Driver
- Couples efficiently into 62.5/125 µm, 100/140 µm, 50/125 µm and 200 µm PCS cables
- Responsivity as receiver ≥ 0.025 A/W
- Dark Current ≥ 1.0 µA @ -1.2V
- ST-Connector

General Description

The CS8127 fiber optic transceiver is designed to support bi-directional, ping-pong communication over a singe optical cable. In bi-directional applications, the CS8127 acts alternately as a transmitter and as a receiver. Receiver responsivity is guaranteed to be at least 0.025A/W.

ORDERING INFORMATION: CS8127



1, NC
2, ANODE
3, CATHODE
4, NC
5, NC
6, ANODE
7, ANODE
8, NC

Product Preview

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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS83C92

Coaxial Tranceiver Interface

Features

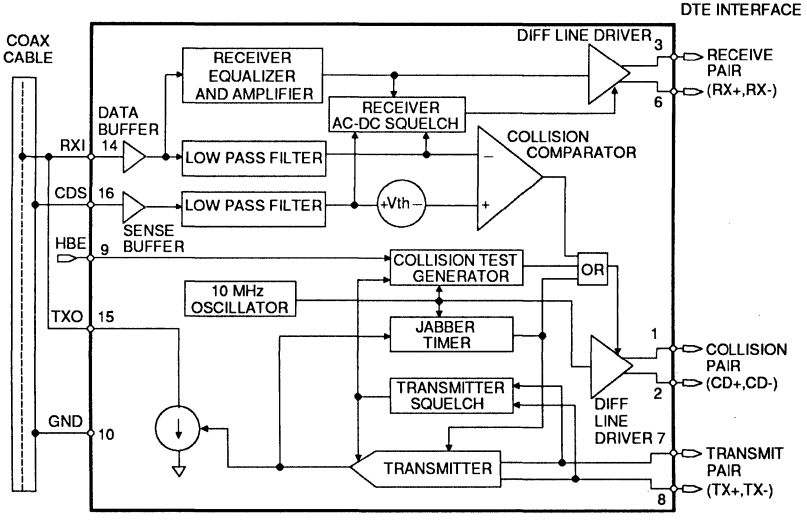
- Implemented in High Voltage CMOS
- Compatible with IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet)
- All Tranceiver Functions Integrated Except Signal and Power Isolation
- Squelch Circuitry Rejects Noise
- CD Heartbeat Externally Selectable Allowing Operation with IEEE 802.3 Compatible Repeaters
- Receive Mode Collision Detection
- Fully Compatible with National DP8392A
- Standard 16-pin DIP Package

General Description

The CS83C92 Ethernet Transceiver interfaces an Ethernet or Cheapernet Local Area Network (LAN) to a LAN Adapter board, and may be located up to 50 meters from the station equipment. The Transceiver operates with the Crystal LAN components CS8005 CSMA/CD Data Link Controller and the CS8023A Serial Interface Adapter.

For an Ethernet network, the CS83C92 Tranceiver is mounted on the RG8 COAX cable, and connects to the station equipment through a transceiver drop cable. In a Cheapernet network, the CS83C92 Transceiver is usually mounted on the LAN adapter in the station equipment, where it connects to the RG58 COAX through a BNC connector.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



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Semiconductor Corporation

CS8401 CS8402

AES/ EBU Interface Line Driver

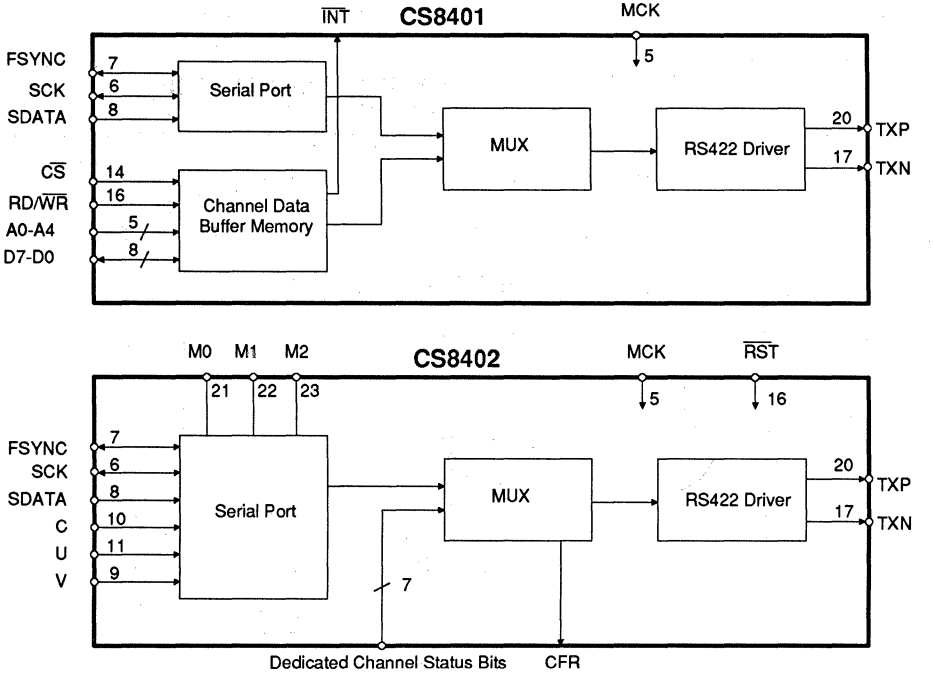
Features

- Monolithic AES/EBU Interface Transmitter
- Supports S/PDIF and EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver

General Description

The CS8401/2 is a monolithic CMOS device which encodes and transmits audio data according to the AES/EBU interface standards. The CS8401/2 accept audio and digital data, which is then multiplexed, encoded and driven directly, or through a transformer, onto a cable. The CS8401 has an internal buffer memory for 1 block of channel data, which is loaded via an 8-bit parallel interface. The CS8402 multiplexes in the channel data directly from external input pins.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

AES/ EBU Interface Line Receiver

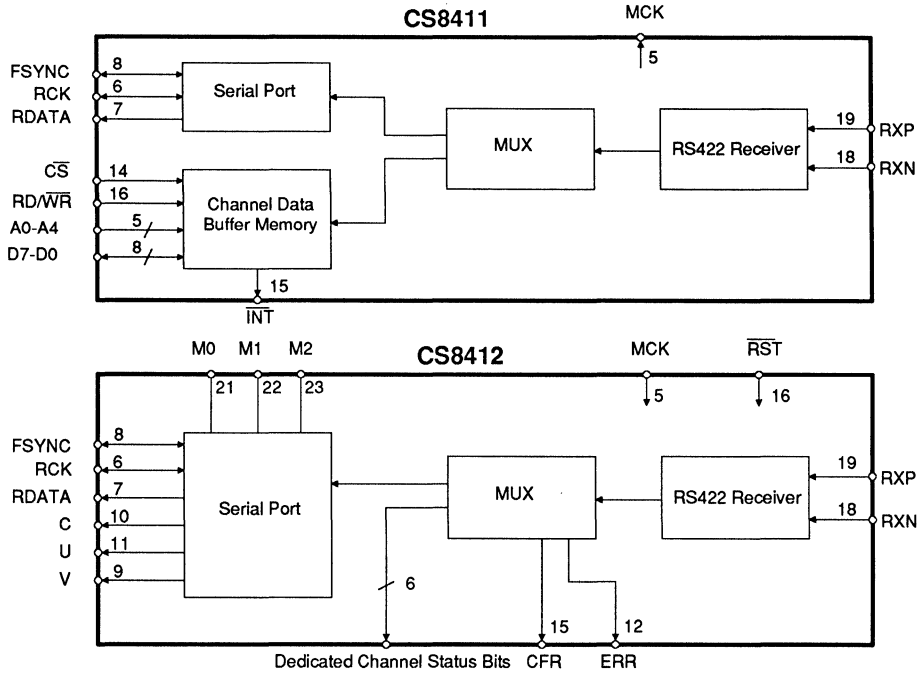
Features

- Monolithic AES/EBU Interface Receiver
- Supports S/PDIF and EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Checks CRC Codes and Parity Bits
- On-Chip RS422 Line Receiver
- Low Jitter Clock Recovery

General Description

The CS8411/12 is a monolithic CMOS device which receives and decodes audio data encoded according to the AES/EBU interface standard. The CS8411/12 receives data from the transmission line, recovers the clock and synchronization signals, and de-multiplexes the audio and digital data. Differential or single ended inputs can be decoded to the professional and consumer interface standards. The CS8411 has an internal buffer memory for 1 block of channel data, which is read via an 8-bit parallel interface. The CS8412 de-multiplexes channel data directly to external pins.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Semiconductor Corporation

CS8870

DTMF Receiver

Features

- Full Receiver Implementation
- Central Office Quality
- Adjustable Receive Sensitvity
- Adjustable Detection and Release Time
- Single Supply Operation
- Low Power Consumption
- 18 Pin Package
- Pin Compatible with MT8870

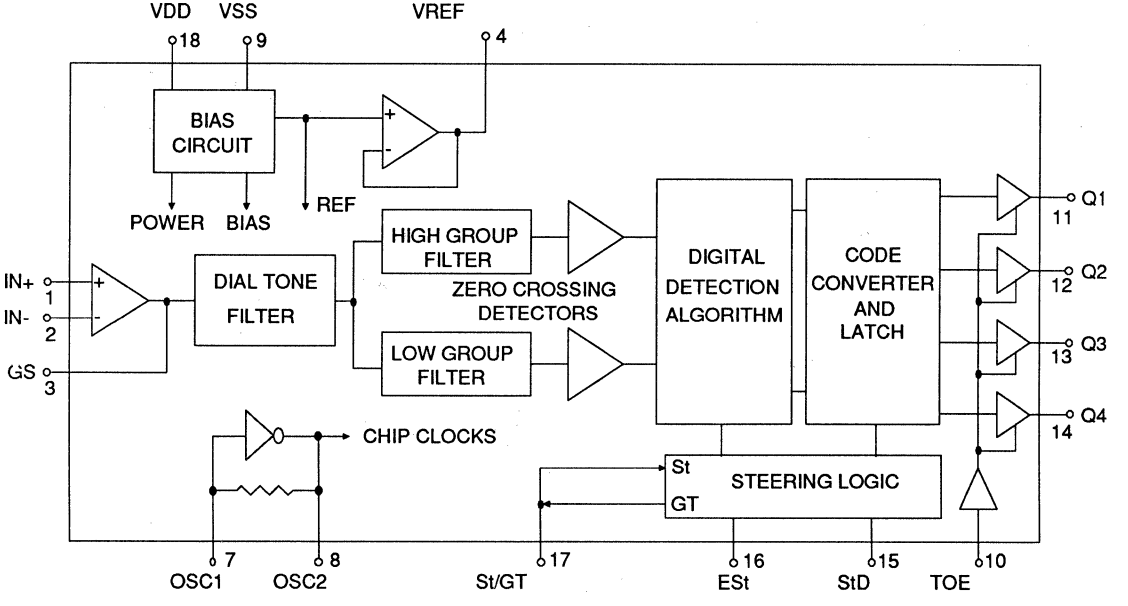
General Description

The CS8870 is a fully integrated DTMF (Dual Tone Multifrequency) receiver for decoding tone pairs generated by a tone dialing telephone. The decoded signal is output as a four bit binary code. All of the functions needed to decode the 16 DTMF tone pairs are integrated in the CS8870 using Crystal's CMOS double-poly process, taking advantage of the low power and high performance offered by this technology.

ORDERING INFORMATION

CS8870-IP - 18 Pin Plastic DIP

Block Diagram



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

INTRODUCTION

Using SMART *Analog* technology, Crystal Semiconductor has created a family of A/D Converters which feature patented on-chip self-calibrating architectures to maintain accuracy and linearity over their full temperature range and device lifetime. Each of our A/D Converters feature an on-chip sample and hold, and are manufactured in low-power CMOS. Some devices include a power-down sleep mode. All feature outstanding specifications ideally suited to their intended applications.

CS5012A, CS5014, CS5016 SAR Family

The CS5012A, CS5014 and CS5016 converters have 12, 14 & 16 bits of resolution, with conversion times of 7 µs to 16 µs. The converters are tested both for static and dynamic performance, at full rated conversion speed. On-chip self-calibration ensures that linearity, offset and full-scale errors remain within spec., with no missing codes.

CS5101 16-bit 100 kHz ADC

Derived from the CS5016, the CS5101 is a 16-bit ADC capable of converting in 8 µs, yielding sample rates of 100 kHz. A 2-channel analog input mux. is included. Output data is available serially, with 4 interface modes. An on-chip crystal oscillator is provided, along with a power-down control.

CS5102 16-bit, 20 kHz Low Power ADC

The CS5102 is a low power version of the CS5101. Requiring only 44 mW from ±5V supplies, along with a 1 mW power down mode, the CS5102 is ideal for battery powered applications. The part also features the same high speed serial interface as the CS5101.

CS5412 12-bit, 1 MHz ADC

Using a 2-step flash approach, the CS5412 achieves 12-bit performance at 1MHz sample rate. Self calibration insures accuracy over time and the military temperature range. Available in both DIP and J-lead LCC packages, with on-chip S/H, the IC offers a very compact ADC solution.

CS5317 16-bit Voice Band ADC

The CS5317 is well suited for a wide range of voiceband applications, from speech recognition to passive sonar. An on-chip PLL/Clock generator makes the part perfect for high-performance modems. The device features a 20 kHz word rate, a 10 kHz bandwidth, 84 dB dynamic range and 80 dB THD. CMOS design keeps power consumption to 280 mW.

CS5126 Audio A/D Converter

The CS5126 2-channel ADC is ideal for digital audio applications. An on-chip sample and hold is included, and sampling rates can be up to 100 kHz for 2X oversampling, yielding a dynamic range of 95 dB. Signal to noise plus distortion is 92 dB and self-calibration insures excellent low-level distortion characteristics.

CS5326,7,8,9 and CS5336,7,8,9 Delta Sigma Audio A/D Converters

This new class of device features 64X oversampling using a delta sigma architecture, with resolutions of 16 or 18-bits. Output word rates can be from 1kHz to 50kHz. These stereo parts have 2 sample and holds, dual delta sigma modulators, two anti-aliasing and decimation filters, and a voltage reference, all in a 28-pin package. Performance measures include 95 dB dynamic range in stereo mode, up to 100 dB in mono mode, along with 0.0015% THD.

CS5501/3 16/20-bit DC Measurement ADC

The CS5501/3 feature an on-chip 6-pole low pass filter with adjustable corner frequencies from 0.1 Hz to 10 Hz. The parts achieve linearity errors of 0.0007%, with no missing codes. A highly flexible serial interface, along with 25 mW power consumption, all in a 20 pin package, make the parts ideal for weigh scale and process control applications. The CS5503 is the 20-bit version of the CS5501, offering increased dynamic range, often removing the need for external gain scaling.

CS5505 4-Channel, 16-bit, DC Measurement ADC

Very low power consumption of 2 mW, along with the 4 channel input mux, make this part ideal for process control applications.

CS5322, CS5323, CS5324 24-bit Variable Bandwidth ADC

The CS5323 modulator, combined with the CS5322 digital filter, offers >120 dB dynamic range in the DC to 500 Hz frequency band. Eight different filter corner frequencies and output update rates are offered, allowing the ADC to be optimized for different types of seismic measurements. The CS5324 includes a modulator and the first stage of digital filtering, allowing the user to implement their own final filter stage.

CS7820 8-bit 1.4 µs ADC

The CS7820 8-bit sampling A/D has an inherent track-and-hold input, along with a 1.4 µs conversion time and easy interfacing to microprocessors.

3

Specifications	CS5012A/14/16	CS5101/2	CS5126	CS5317	CS5322/3 CS5324	CS5326/7 CS5328/9 CS5336/7 CS5338/9	CS5412	CS5501/3	CS5505	CS7820
Application	GP	GP	Audio	Modem	Seismic	Audio	GP Fast	DC Measurement		GP
Resolution (bits)	12/14/16	16	16	16	24	16/18	12	16/20	16	8
Conversion Time (us)	7/14/16	8/40	8	-	-	-	1.25	-	-	1.4
Throughput (kHz)	100/56/50	100/20	100	20	-	50	1 MHz	4	20Hz	-
Number of Inputs	1	2	2	1	1	2	1	1	4	1
Input Bandwidth	-	-	24 kHz	10 kHz	500 Hz	22/20 kHz	4 MHz	10Hz	10 Hz	-
Integral Non-Linearity	.006/.002/.001 %	.0015%	-	-	-	-	.01 %	.0007/.003 %	.001 %	.2%
Differential (± LSB) Non-Linearity	0.25/0.25/NMC	NMC	NMC	NMC	NMC	NMC	0.9	0.125/NMC	0.125	NMC
No Missing Codes	12/14/16	16	16	16	20	16/18	12	16/20	16	8
Total Harmonic Distortion (%)	.008/.003/.001	.001	.001	.007	.0003	.0015	.02	-	-	-
Signal-to-Noise plus Distortion (dB)	73/83/92	92	92	80	-	92	70	-	-	-
Dynamic Range (dB)	73/83/92	92	92	84	120	95/100*	70	-	-	-
Power Needed (mW)	120	280/44	280	220	150	450/400	750	25	2	40
Conversion Method	Succ. Approx.	Succ. Approx.	Succ. Approx.	Delta Sigma	Delta Sigma	Delta Sigma	2-Step Flash	Delta Sigma	Delta Sigma	2-Step Flash
Power Down Mode		√	√		√	√		√	√	
On-Chip Sample and Hold	√	√	√	√	√	√	√	√	√	√
On-Chip V. Ref				√		√			√	
On-Chip Filtering				√	√	√		√	√	
Statically Tested	√	√					√	√	√	√
Dynamically Tested	√	√	√	√	√	√	√			
Temperature Range	Com Ind Mil	Com Ind Mil	Com	Com Ind Mil	Com Ind	Com	Com Ind Mil	Com Ind Mil	Com Ind	Com Ind Mil
Number of Pins (DIP)	40	28	28	18	28	28	40	20	20	20
Packages	DIP PLCC LCC	DIP PLCC LCC	DIP PLCC	DIP SOIC	DIP PLCC	DIP SOIC	DIP CLCC	DIP SOIC	DIP SOIC	DIP

NMC=No Missing Codes * CS5328 In Mono Mode GP=General Purpose

CONTENTS

Semiconductor Corporation

CS5012A

12-Bit, 7 us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 12-Bit Precision
  - Linearity Error: ±1/4 LSB
  - Total Unadjusted Error: ±1/4 LSB
  - DNL: ±1/16 LSB
- Low Distortion
  - Total Harmonic Distortion: 0.008%
  - Peak Harmonic or Noise: -92 dB
- 7.2 Microsecond Conversion Time
  - Throughout Rates up to 100 kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 150 mW
- Pin Compatible with CS5014/CS5016

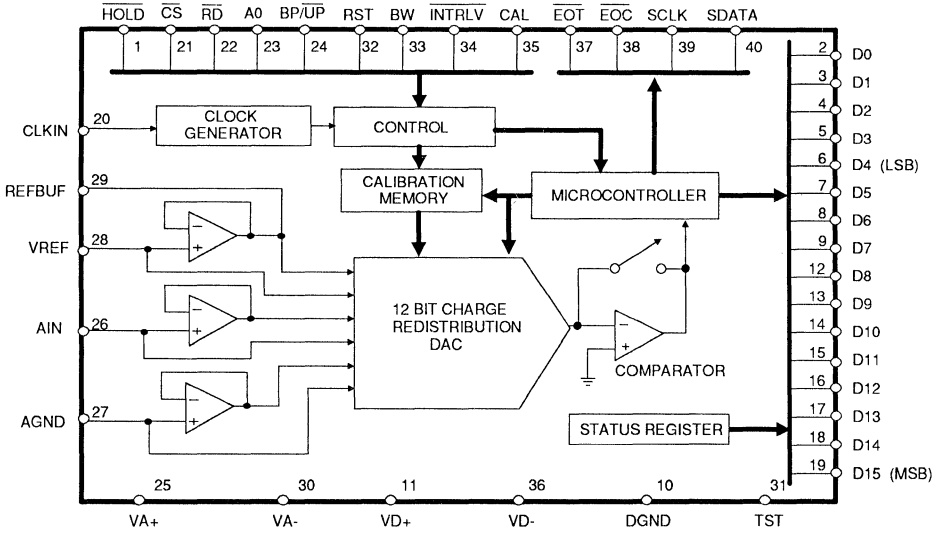
General Description

The CS5012A is a 12-bit monolithic analog to digital converter with a conversion time as fast as 7.2 µs. Unique self-calibration circuitry insures maximum nonlinearity of 1/2 LSB and no missing codes. Offset and full scale errors are kept within 1/2 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5012A consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 2.8 µs to 0.01%, allowing throughput rates up to 100 kHz.

An evaluation board (CDB5012) is available for the CS5012A which can be easily configured to simulate any combination of operating conditions to greatly simplify system design and testing. The CS5012A is pin compatible with the CS5014 and CS5016 A/D converters allowing system upgrading and downgrading without hardware alterations.

ORDERING INFORMATION: Page 3-33



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 455 7581

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V to 4.5V; f_{clk} = 6.4 MHz for –7, 4 MHz for –12, 2 MHz for –24; Analog Source Impedance = 200 Ω)

Parameter *	CS5012-K,L CS5012A-K min	typ	max	CS5012-B CS5012A-B min	typ	max	CS5012-T CS5012A-T min	typ	max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Accuracy										
Linearity Error (Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Drift (Note 2)		±1/8			±1/8			±1/8		ΔLSB
Differential Linearity -K,B,T (Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
-L (Note 1)		±1/16	±1/8							LSB
Drift (Note 2)		±1/32			±1/32			±1/32		ΔLSB
Full Scale Error (Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Drift (Note 2)		±1/16			±1/16			±1/8		ΔLSB
Unipolar Offset (Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Drift (Note 2)		±1/16			±1/16			±1/16		ΔLSB
Bipolar Offset (Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Drift (Note 2)		±1/16			±1/16			±1/16		ΔLSB
Bipolar Negative Full-Scale Error (Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB
Drift (Note 2)		±1/16			±1/16			±1/16		ΔLSB
Total Unadjusted Error (Note 1)		±1/4			±1/4			±1/4		LSB
Drift (Note 2)		±1/4			±1/4			±1/4		ΔLSB
Dynamic Performance (Bipolar Mode)										
Peak Harmonic or Spurious Noise (Note 1)										
Full-Scale, 1 kHz Input	84	92		84	92		84	92		dB
Full-Scale, 12 kHz Input	84	88		84	88		84	88		dB
Total Harmonic Distortion		0.008			0.008			0.008		%
Signal-to-Noise Ratio (Note 1)										
1 kHz, 0 dB Input	72	73		72	73		72	73		dB
1 kHz, -60 dB Input		13			13			13		dB
Noise Unipolar Mode (Note 3)		45			45			45		uV_{rms}
Bipolar Mode		90			90			90		uV_{rms}

Notes: 1. Applies after calibration at any temperature within the specified temperature range.
2. Total drift over specified temperature range since calibration at power-up at 25 °C.
3. Wideband noise aliased into the baseband. Referred to the input.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

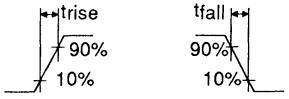
Parameter *		CS5012-K,L CS5012A-K min	typ	max	CS5012-B CS5012A-B min	typ	max	CS5012-T CS5012A-T min	typ	max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125		°C
Analog Input											
Aperture Time			25			25			25		ns
Aperture Jitter			100			100			100		ps
Aperture Time Matching	(Note 4)		TBD			TBD			TBD		ns
Input Capacitance	(Note 5)										
Unipolar Mode	CS5012		275	375		275	375		275	375	pF
	CS5012A		103	137		103	137		103	137	pF
Bipolar Mode	CS5012		165	220		165	220		165	220	pF
	CS5012A		72	96		72	96		72	96	pF
Conversion & Throughput											
Conversion Time	-7			7.2			7.2			7.2	us
(Notes 6, 7)	-12			12.25			12.25			12.25	us
	-24			24.5			24.5			24.5	us
Acquisition Time	-7		2.5	2.8		2.5	2.8		2.5	2.8	us
(Note 7)	-12		3.0	3.75		3.0	3.75		3.0	3.75	us
	-24		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput	-7	100			100			100			kHz
(Note 7)	-12	62.5			62.5			62.5			kHz
	-24	33.6			33.6			33.6			kHz
Power Supplies											
DC Power Supply Currents	(Note 8)										
I_{A+}			12	19		12	19		12	19	mA
I_{A-}			–12	–19		–12	–19		–12	–19	mA
I_{D+}			3	6		3	6		3	6	mA
I_{D-}			–3	–6		–3	–6		–3	–6	mA
Power Dissipation	(Note 8)		150	250		150	250		150	250	mW
Power Supply Rejection	(Note 9)										
Positive Supplies			84			84			84		dB
Negative Supplies			84			84			84		dB

Notes:
4. Part to part.
5. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
6. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
7. Conversion, acquisition, and throughput times depend on CLKIN, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5012A's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. Refer to the section *Conversion Time/Throughput* for a detailed discussion of conversion timing.
8. All outputs unloaded. All inputs CMOS levels.
9. With 300 mV p-p, 1 kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 18 shows a plot of typical power supply rejection versus frequency.

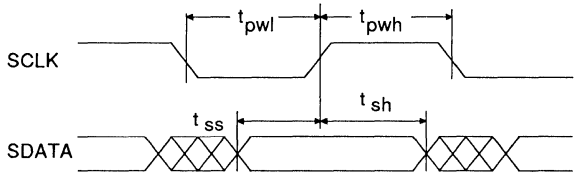
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V±10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF, BW = VD+)

Parameter	Symbol	Min	Typ	Max	Units
CLKIN Frequency:					
Internally Generated: K,B, - 7,- 12	f_{CLK}	2	-	-	MHz
T, - 7,- 12		1.75	-	-	
- 24		1	-	-	
Externally Supplied: - 7		100 kHz	-	6.4	
- 12		100 kHz	-	4.0	
CLKIN Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK}$+ 50	-	t_c	ns
Conversion Time	t_c	$49/f_{CLK}$ + 50	-	$53/f_{CLK}$+ 235	ns
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 10)	t_{epw}	$4/f_{CLK}$ - 20	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-K, B	t_{ca}	-	90	120	ns
-T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-K, B	t_{ra}	-	90	120	ns
-T		-	115	150	
Output Float Delay: -K, B	t_{fd}	-	90	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -T			90	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK}$ - 50	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK}$ - 100	$2/f_{CLK}$	-	ns

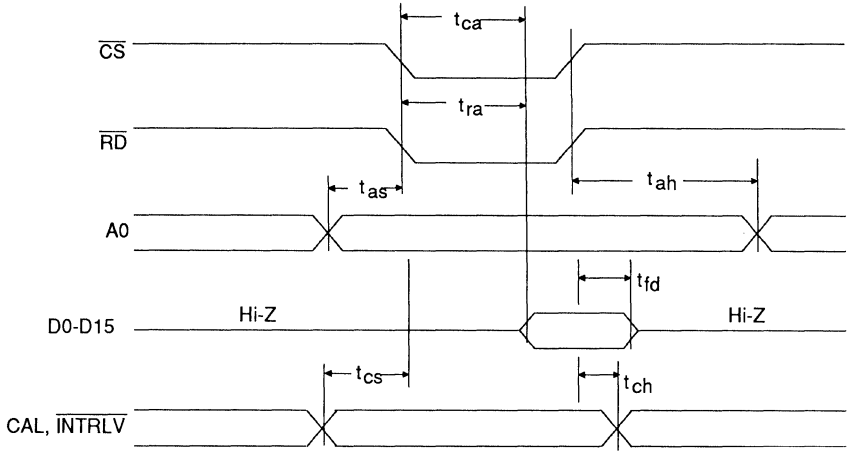
Note: 10. $\overline{EOC}$ remains low 4 CLKIN cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 CLKIN cycles from the start of a data read operation or a conversion cycle.



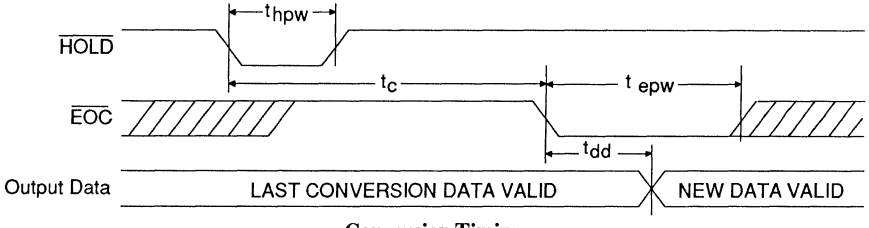
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	0.8	V
High-Level Output Voltage (Note 11)	V_{OH}	(VD+) - 1.0V	–	–	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	–	–	0.4	V
Input Leakage Current	I_{in}	–	–	10	uA
3-State Leakage Current	I_{OZ}	–	–	±10	uA
Digital Output Pin Capacitance	C_{out}	–	9	–	pF

Note: 11. I_{out} = -100 µA. This specification guarantees TTL compatability (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 12.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	2.5	(VA+) - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	–	VREF	V
(Note 13)	Bipolar	V_{AIN}	-VREF	–	VREF	V

Notes: 12. All voltages with respect to ground.

13. The CS5012A can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 14)		I_{in}	–	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VA+) + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 14. Transient currents of up to 100 mA will not cause SCR latch-up.

THEORY OF OPERATION

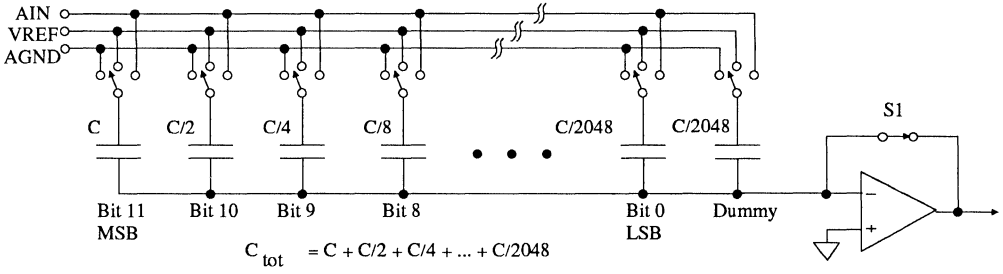


Figure 1. Charge Redistribution DAC

The CS5012A/CS5012 family utilizes a successive approximation conversion technique. The analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

A unique charge redistribution architecture is used to implement the successive approximation algorithm. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory

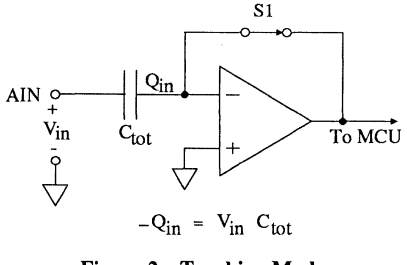


Figure 2a. Tracking Mode

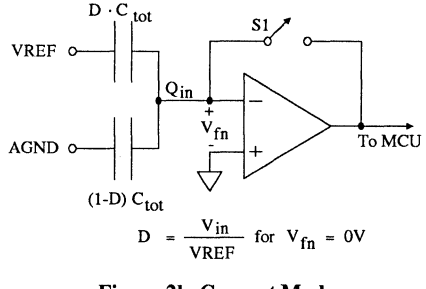


Figure 2b. Convert Mode

during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

This charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5012A to convert accurately to 12-bits clearly depends on the accuracy of its comparator and DAC. The CS5012A utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 12-bit accuracy from the DAC, the CS5012A uses a novel self-calibration scheme. Each bit capacitor, shown in Figure 1, actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

DIGITAL CIRCUIT CONNECTIONS

The CS5012A can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CS5012A operates from a master clock (CLKIN) which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5012A can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

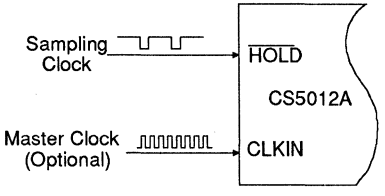


Figure 3a. Asynchronous Sampling

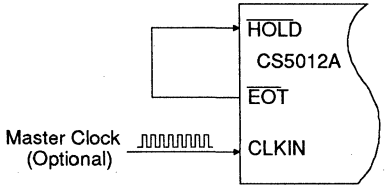


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to CLKIN frequency. Thus, throughput can be precisely controlled and/or maximized using an external CLKIN signal. In contrast, the CS5012A's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -7 version of the CS5012A is specified for accurate operation with an external clock up to 6.4 MHz; its internal clock frequency is specified at a minimum of 2 MHz. The -12 version of the CS5012A is specified for accurate operation with an external clock up to 4 MHz; its internal clock frequency is specified at a minimum of 2 MHz. Both versions can typically convert with clocks as low as 10 kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. Upon completion of the conversion cycle, the CS5012A automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one CLKIN cycle plus 50 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the device's decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5012A's base address will initiate a conversion. However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset* below).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are inputs to a set of transparent latches. These signals are internally latched by $\overline{\text{CS}}$ returning high. They must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5012A's base address will initiate or terminate calibration. Alternatively, A0, $\overline{\text{INTRLV}}$, and CAL may be connected to the microprocessor data bus.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5012A requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six CLKIN cycles plus 2.25 µs (1.32 µs for the -7 version only). This adds to the conversion time to define the converter's maxi-

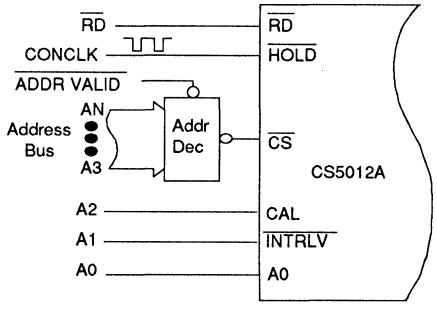


Figure 4a. Conversions Asynchronous to CLKIN

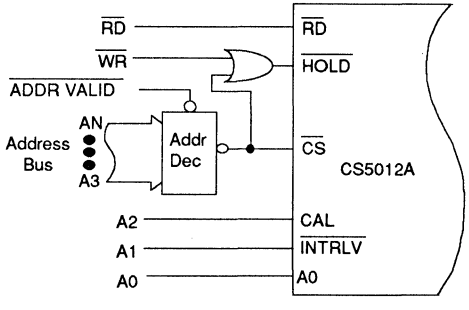


Figure 4b. Conversions under Microprocessor Control

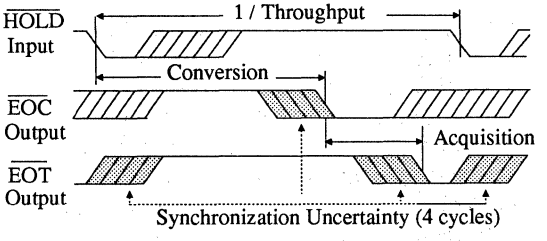


Figure 5a. Asynchronous Sampling (External Clock)

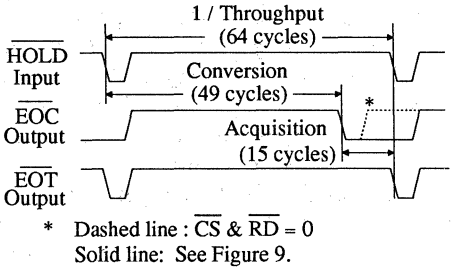


Figure 5b. Synchronous (Loopback) Mode

mum throughput. The conversion time of the CS5012A, in turn, depends on the sampling, calibration, and CLKIN conditions.

Asynchronous Sampling

The CS5012A internally operates from a clock which is delayed and divided down from CLKIN ($f_{CLKIN}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after HOLD goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 49 clock cycles to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track (EOT) output to HOLD (Figure 3b). The EOT output falls 15 CLKIN cycles after EOC indicating the analog input has been acquired to the CS5012A's specified accuracy. The EOT output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/64th of the CLKIN frequency (see Figure 5b and Table 1).

Also, the CS5012A's internal RC oscillator exhibits jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CS5012A is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity. The user can obtain best sampling purity while synchronously sampling by using an external crystal-based clock.

Reset

Upon power up, the CS5012A must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5012A's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized

Sampling Mode		Conversion Time Min	Conversion Time Max	Throughput Time Min	Throughput Time Max
Synchronous (Loopback)		49 t_{clk}	49 t_{clk}	64 t_{clk}	64 t_{clk}
Asynchronous	-7	49 t_{clk}	53 t_{clk}+ 235 ns	N/A	59 t_{clk}+ 1.32 us
	-12,-24	49 t_{clk}	53 t_{clk}+ 235 ns	N/A	59 t_{clk}+ 2.25 us

Table 1. Conversion and Throughput Times (t_{clk} = Master Clock Period)

to within 5% of its final value before RST falls to guarantee an accurate calibration. Later, the CS5012A may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5012A will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

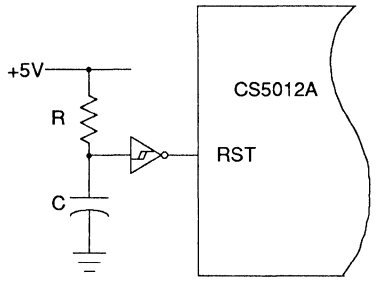


Figure 6. Power-On Reset Circuit

Resets can be initiated in hardware or software. The simplest method of resetting the CS5012A involves strobing the RST pin high for at least 100 ns. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 58,280 CLKIN cycles (approximately 9.1 ms with a 6.4 MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmitt-trigger inverter to prevent oscillation (see Figure 6). The CS5012A can also be reset in software when under microprocessor control. The CS5012A will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section (below) to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5012A is ready for operation. While calibrating, the $\overline{HOLD}$ input is ignored until $\overline{EOC}$ falls. After $\overline{EOC}$ falls, six CLKIN cycles plus 2.25 µs (1.32 µs for the -7 version only) must be allowed for signal acquisition before $\overline{HOLD}$ is activated.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5012A's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is normally only required once, after power-up.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 CLKIN cycles plus 2.25 µs (1.32 µs for the -7 version only) must be allowed before a conversion is initiated to ensure the CS5012A has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment.

The CS5012A features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5012A gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 2,014 conversions). Initiated by bringing both the $\overline{INTRLV}$ input and $\overline{CS}$ low (or hard-wiring $\overline{INTRLV}$ low), interleave extends the CS5012A's effective

conversion time by 20 CLKIN cycles. Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CS5012A sees free time. Interleave is subordinate to burst calibrations, so $\overline{\text{INTRLV}}$ could still be externally tied low. If used, interleave should be left active continuously.

The fact that the CS5012A offers several calibration modes is not to imply that the device needs to be recalibrated often. The device is very stable in the presence of large temperature changes. Tests have indicated that after using a single reset calibration at 25 °C most devices exhibit very little change in offset or gain when exposed to temperatures from -55 to +125 °C. The data indicated 30 ppm as the typical worst case total change in offset or gain over this temperature range. Differential linearity remained virtually unchanged. System error sources outside of the A/D converter, whether due to changes in temperature or to long-term aging, will generally dominate total system error.

Microprocessor Interface

The CS5012A features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low enables the CS5012A's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{\text{HOLD}}$ is low, or a software reset will result* (see *Reset* above).

Alternatively, the End-of-Convert ($\overline{\text{EOC}}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{\text{EOC}}$ pin falls

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{\text{END OF CONVERSION}}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{\text{HIGH BYTE}}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{\text{END OF TRACK}}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the intput.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Pin Definitions

as each conversion cycle is completed and data is valid at the output. It returns high within four CLKIN cycles of the first subsequent data read operation or after the start of a new conversion cycle.

To interface with a 16-bit data bus, the BW input to the CS5012A should be held high and all 12 data bits read in parallel on pins D4-D15. With an 8-bit bus, the converter's 12-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 4 LSB's with 4 trailing zeros. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5012A internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5012A is converting will not introduce conversion errors. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

Microprocessor Independent Operation

The CS5012A can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low. This permanently enables the 3-state output buffers and allows transparent latch inputs (CAL and $\overline{INTRLV}$) to be active. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The CS5012A's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four CLKIN cycles after each conversion. Data will be unstable up to 100 ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with

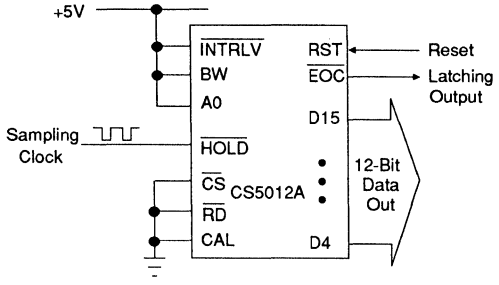


Figure 8. Microprocessor-Independent Connections

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Status (A0=0)	X	X	X	X	X	X	X	X	S7	S6	S5	S4	S3	S2	S1	S0	8- or 16-Bit Data Bus
Data (A0=1)	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	0	0	16-Bit Bus (BW=1)
	X	X	X	X	X	X	X	X	B11	B10	B9	B8	B7	B6	B5	B4	8-Bit Bus (BW=0)
									B3	B2	B1	B0	0	0	0	0	

"X" Denotes High Impedance Output

Figure 7. Data Format

the MSB. The CS5012A presents each bit to the SDATA pin four CLKIN cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5012A (See Figure 9).

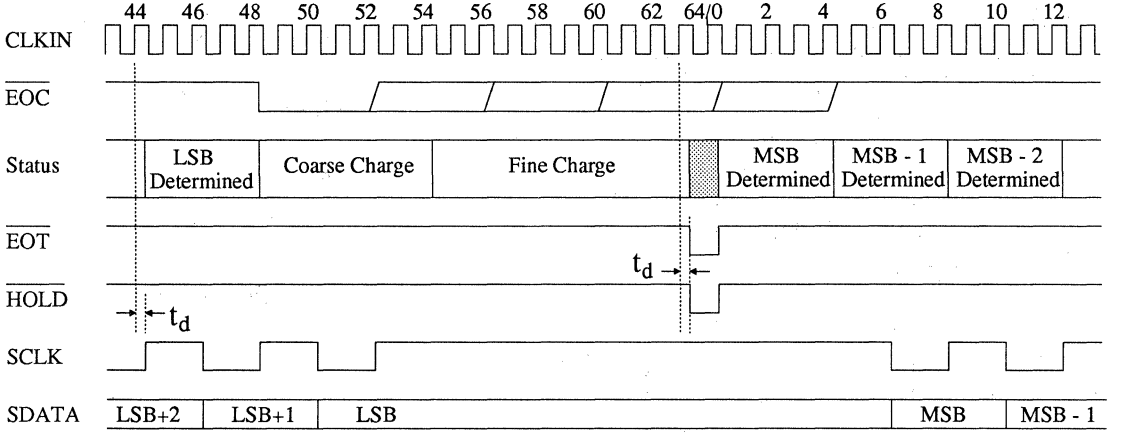
ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5012A internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X Series of A/D Converters*" is available for the CS5012A. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5012A includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby



Notes: 1. Synchronous (loopback) mode is illustrated. After $\overline{EOC}$ falls the converter goes into coarse charge mode for 6 CLKIN cycles, then to fine charge mode for 9 cycles, then $\overline{EOT}$ falls. In loopback mode, $\overline{EOT}$ trips $\overline{HOLD}$ which captures the analog sample. Conversion begins on the next rising edge of CLKIN. If operated asynchronously, $\overline{EOT}$ will remain low until after $\overline{HOLD}$ is taken low. When $\overline{HOLD}$ occurs the analog sample is captured immediately, but conversion may not begin until four CLKIN cycles later. $\overline{EOT}$ will return high when conversion begins.

2. Timing delay t_d (relative to CLKIN) can vary between 135 ns to 235 ns over the military temperature range and over ± 10% supply variation

3. $\overline{EOC}$ returns high in 4 CLKIN cycles if A0 = 1 and $\overline{CS}$ = $\overline{RD}$ = 0 (Microprocessor Independent Mode); within 4 CLKIN cycles after a data read (Microprocessor Mode); or 4 CLKIN cycles after $\overline{HOLD}$ = 0 is recognized on a rising edge of CLKIN/4.

Figure 9. Serial Output Timing

providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5012A sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc.

The magnitude of the current load on the external reference circuitry will scale to the CLKIN frequency. At full speed, the reference must supply a maximum load current of 10 µA peak-to-peak (1 µA typical). An output impedance of 15 Ω will therefore yield a maximum error of 150 µV. With a 2.5V reference and LSB size of 600 µV, this would insure better than 1/4 LSB accuracy. A 1 µF capacitor exhibits an impedance of less than 15 Ω at frequencies greater than 10 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5012A can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference

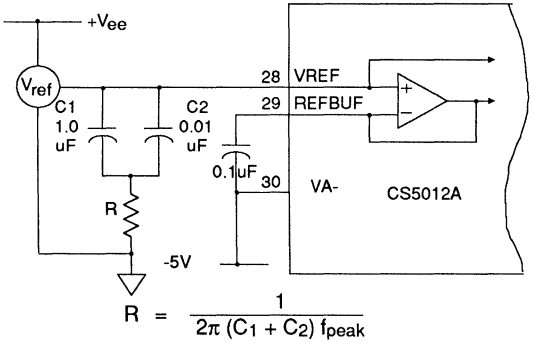


Figure 10. Reference Connections

voltage is between 2.5 and 4.5 volts. The CS5012A can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult the application note: *Voltage References for the CS501X Series of A/D Converters.* For an example of using the CS5012A with a 5 volt reference, see the application note: *A Collection of Application Hints for the CS501X Series of A/D Converters.*

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six CLKIN cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 illustrates this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

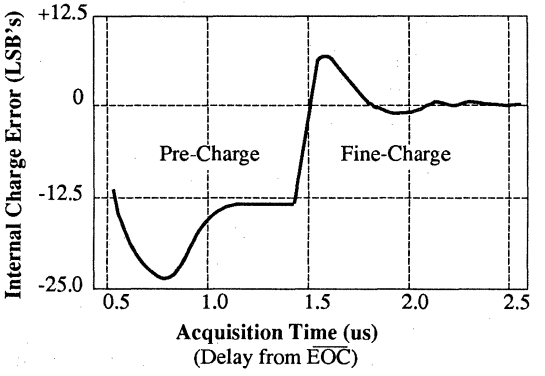


Figure 11. Internal Acquisition Time

The acquisition time of the CS5012A depends on the CLKIN frequency. This is due to a fixed pre-charge period. For instance, operating the -12 version with an external 4 MHz CLKIN results in a 3.75 µs acquisition time: 1.5 µs for pre-charging (6 clock cycles) and 2.25 µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25 µs for an analog source impedance of less than 200 Ω. (For the -7 version it is specified as 1.32 µs.) In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input applications, consult the application note: *Input Buffer Amplifiers for the CS501X Family of A/D Converters.*

During the first six clock cycles following a conversion (pre-charge), the CS5012A is capable of slewing at 20V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5012A can slew at 40V/µs. After the first six CLKIN cycles, it will slew at 1.25V/µs in the unipolar mode and 3.0V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5012A is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CS5012A can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 111111111111, and negative full scale gives a digital output of 000000000000.

The BP/$\overline{UP}$ mode pin may be switched after calibration without having to recalibrate the converter. However, the BP/$\overline{UP}$ mode should be changed during the previous conversion cycle, that is, between $\overline{HOLD}$ falling and $\overline{EOC}$ falling.

If BP/$\overline{UP}$ is changed at any other time, one dummy conversion cycle must be allowed for proper acquisition of the input.

Grounding and Power Supply Decoupling

The CS5012A uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference point.

The digital and analog supplies to the CS5012A are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5012A must never exceed the positive analog supply by more than a diode drop or the CS5012A could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram in Figure 20 shows a decoupling scheme which allows the CS5012A to be powered from a single set of ± 5V rails.

As with any high-precision A/D converter, the CS5012A requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5012A. The CDB5012 evaluation board is available for the CS5012A, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5012A, and can be quickly reconfigured to simulate any combination of sampling, calibration, CLKIN, and analog input range conditions.

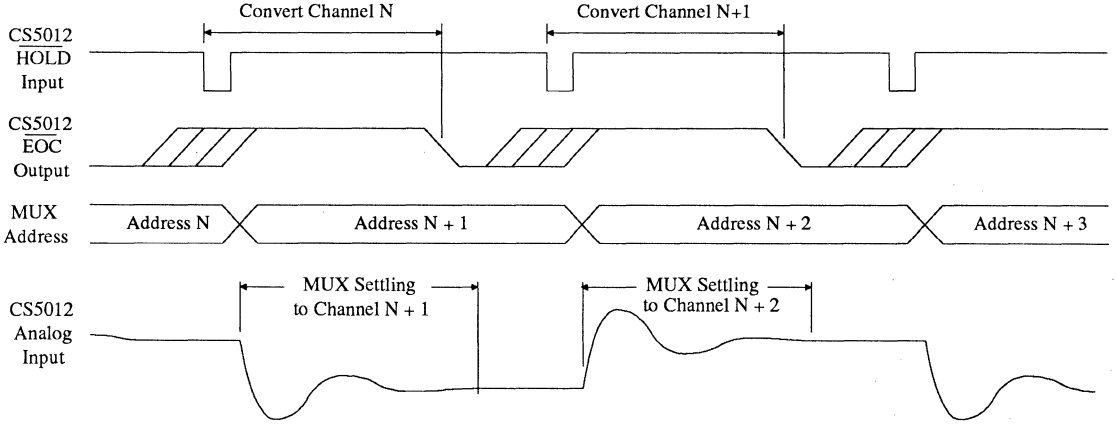


Figure 12. Pipelined MUX Input Channels

Power Supply Rejection

The CS5012A's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5012A's accuracy. This is because the CS5012A adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 13 shows power supply rejection of the CS5012A in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

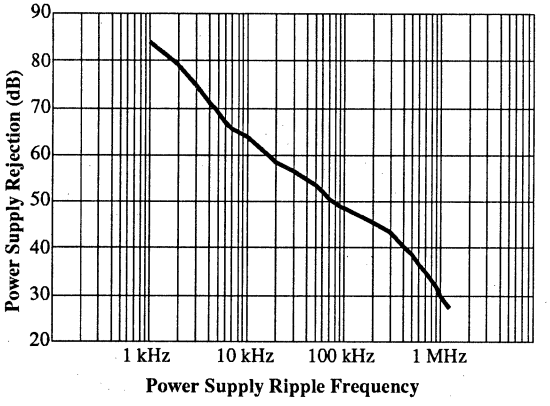


Figure 13. Power Supply Rejection

CS5012A PERFORMANCE

Differential Nonlinearity

One source of nonlinearity in A/D converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5012A calibrates all bits in the capacitor array to a small fraction of an LSB resulting in nearly ideal DNL. A histogram plot of typical DNL of the CS5012A can be seen in Figure 14. Figure 15 illustrates the DNL plot of the CS5012 for comparison.

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows in the transfer curve generate harmonic distortion. The worst-case condition of bit-weight errors (DNL) has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in

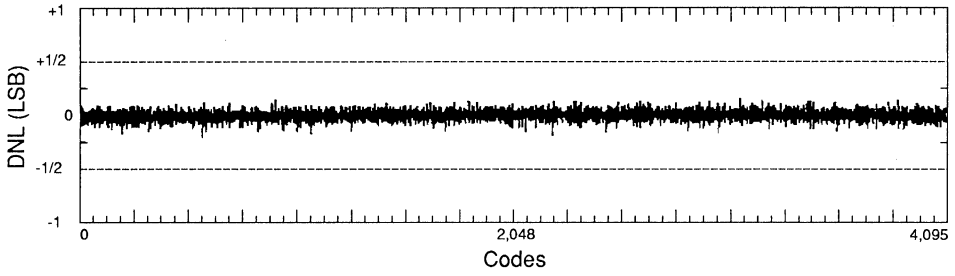


Figure 14. CS5012A Differential Nonlinearity Plot

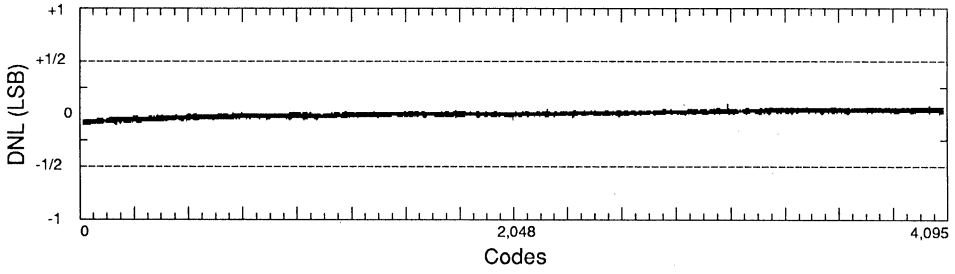


Figure 15. CS5012 Differential Nonlinearity Plot

and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CS5012A achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CS5012A calibrates its bit weight errors to a small fraction of an LSB at 12-bits yielding peak distortion below the noise floor (see Figure 17). Unlike traditional ADC's, the linearity of the CS5012A is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

FFT Tests and Windowing

In the factory, the CS5012A is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5012A, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5012A.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large

discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

Figure 16 shows an FFT computed from an ideal 12-bit sinewave. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten 1024 point time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics which exist above the noise floor are therefore more clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

Figures 17 and 18 show the performance of the CS5012A with 1kHz and 12kHz full scale inputs. Notice that the performance closely approaches that of an ideal 12-bit ADC.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ± 1/2 LSB, but any value within this range has equal probability of occurence. Such a probability

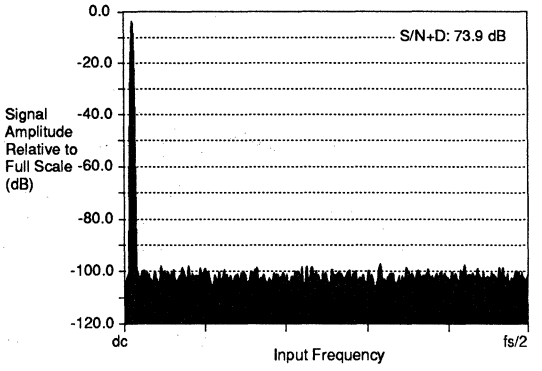


Figure 16. FFT Plot of Ideal 12-bit ADC

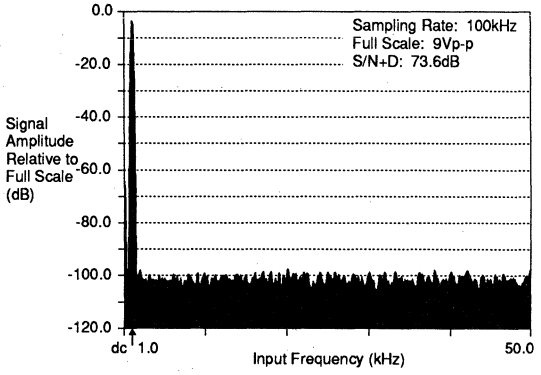


Figure 17. FFT Plot of CS5012A with 1 kHz Full-Scale Input

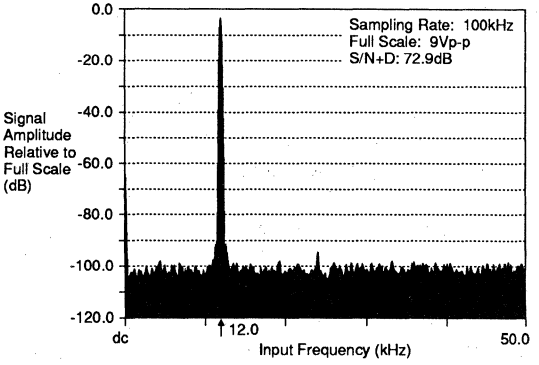


Figure 18. FFT Plot of CS5012A with 12 kHz Full-Scale Input

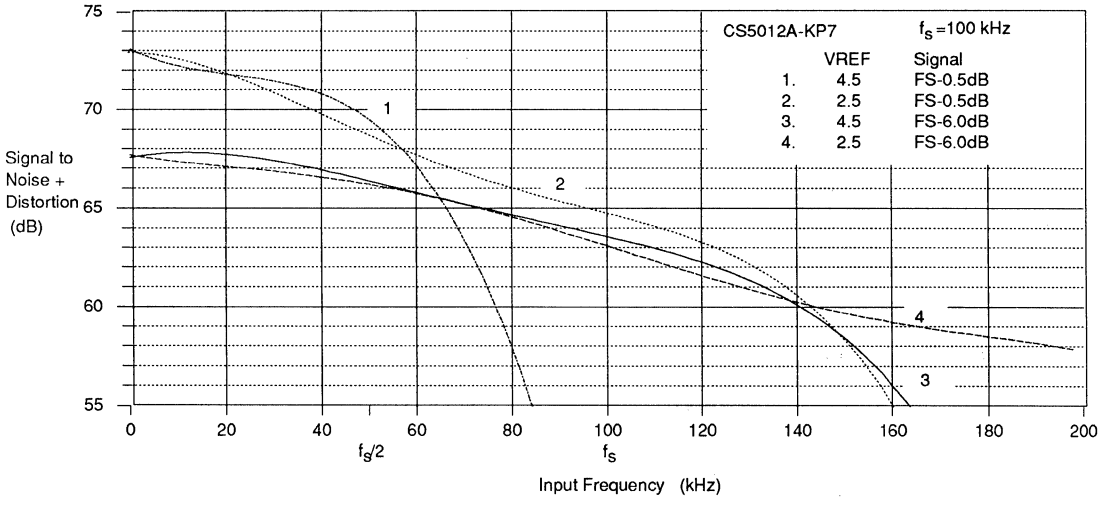


Figure 19. CS5012A High Frequency Input Performance

distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 12-bit signal-to-noise ratio of 74 dB.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

The CS5012A performs very well over a wide range of input frequencies as shown in Figure 19. The figure depicts the CS5012A-KP7 tested under four different conditions. The conditions include tests with the voltage reference set at 4.5 and at 2.5 volts with input signals at 0.5 dB down from full scale and 6.0 dB down from full scale. The sample rate is at 100kHz for all cases. The plots indicate that the part performs very well even with input frequencies above the Nyquist rate. Best performance at the higher frequencies is achieved with a 2.5 volt reference.

Differences between the CS5012A and the CS5012

The differences between the CS5012A and the CS5012 are tabulated in Table 3. The CS5012 is a short-cycled version of the CS5016 A/D converter and includes the same 18-bit calibration circuitry. This calibration circuitry sets the calibration resolution of the CS5012 at 1/64th of an LSB and achieves the near perfect differential linearity performance illustrated by the CS5012 DNL plot in Figure 14. The CS5012A calibration circuitry was modified to provide calibration to 15-bit resolution therefore achieving calibration to 1/8 of an LSB. This reduction in calibration resolution for the CS5012A reduces the time required to calibrate the device (see Table 3) and reduces the size of the total array capacitance. The reduced array capacitance improves the high

	CS5012A	CS5012
Calibration resolution	15 bits. Results in DNL calibration to 1/8 LSB at 12 bits.	18 bits. Results in DNL calibration to 1/64 LSB at 12 bits.
Calibration time reset: interleave: burst:	 58,280 CLKIN cycles 2,014 conversions fully functional	 1,441,020 CLKIN cycles 72,051 conversions not functional
End of calibration indicator	$\overline{EOC}$ falls in either microprocessor or microprocessor-independent mode at the completion of a RESET calibration cycle.	$\overline{EOC}$ falls at the completion of a RESET calibration cycle in microprocessor mode only. In microprocessor-independent mode $\overline{EOT}$ must be used. $\overline{EOT}$ falls 15 CLKIN cycles after completion of a RESET calibration.
Throughput rate in loopback mode	The device acquires and converts a sample in 64 CLKIN cycles for all CLKIN frequencies when in loopback.	The device acquires and converts in 64 CLKIN cycles for CLKIN=4MHz, but will require 68 CLKIN cycles at 100kHz throughput. This is due to excess delay on $\overline{EOT}$.
Input capacitance in fine-charge mode	103pF typical, unipolar mode 72pF typical, bipolar mode	275pF typical, unipolar mode 165pF typical, bipolar mode
Slew Rate Unipolar Coarse charge Fine charge Bipolar Coarse charge Fine charge	 20V/us 1.5V/us 40V/us 3.0V/us	 5V/us 0.25V/us 10V/us 0.5V/us

Table 3. Differences between CS5012A and CS5012

frequency performance by allowing higher slew rate in the input circuitry.

Table 3 documents some other improvements included in the CS5012A. The burst mode calibration, while not generally needed, was made functional. The device was also modified so the $\overline{EOC}$ signal goes low at the end of a reset calibration in either microprocessor or microprocessor-independent mode. The CS5012A was modified to maintain a throughput rate of 64 CLKIN cycles in loopback mode for all frequencies of CLKIN.

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

Table 4. CS5012A Truth Table

3

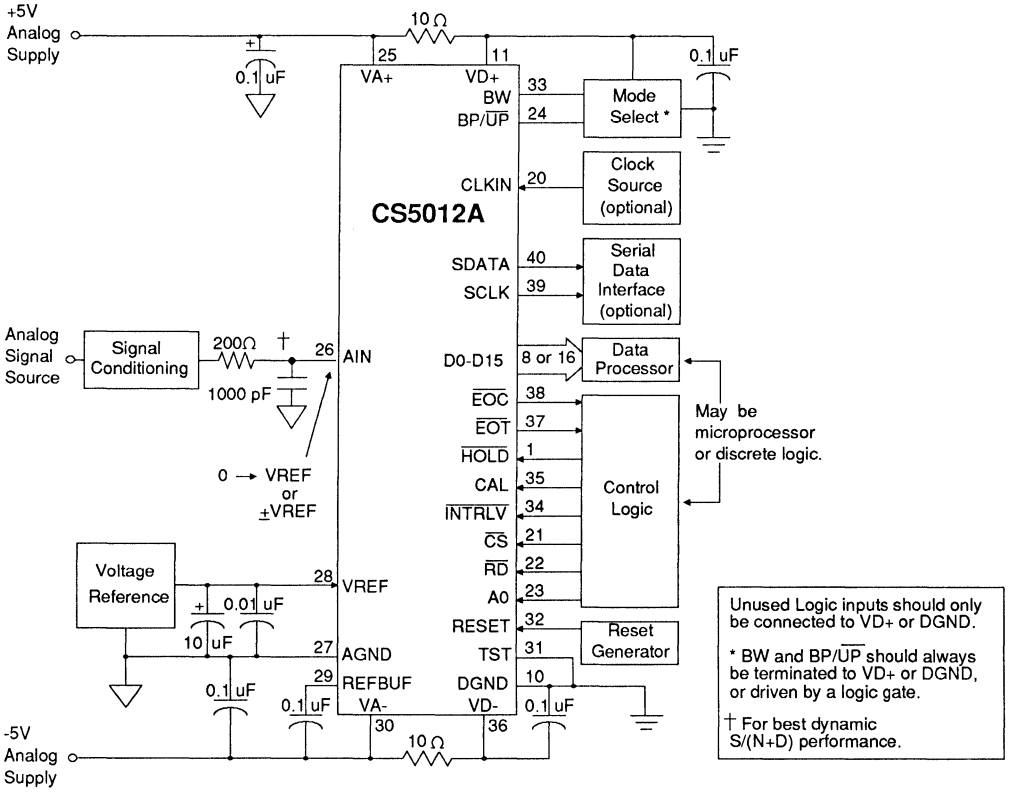
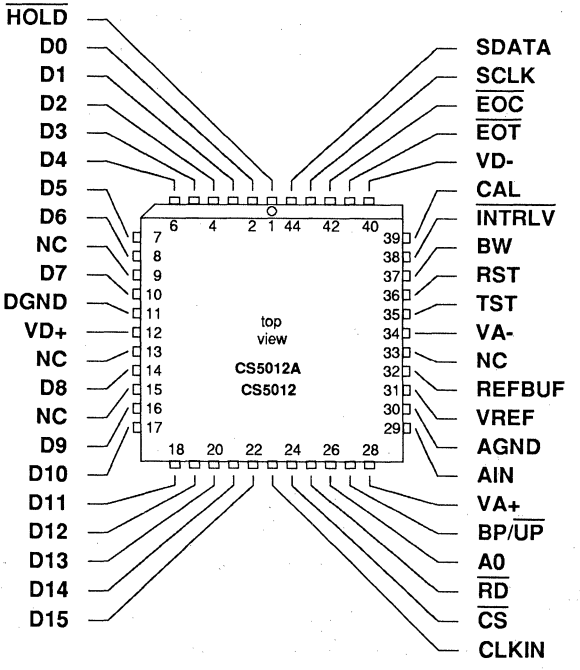


Figure 20. CS5012A System Connection Diagram

HOLD	$\overline{\text{HOLD}}$	1	40	SDATA	SERIAL OUTPUT
DATA BUS BIT 0	D0	2	39	SCLK	SERIAL CLOCK
DATA BUS BIT 1	D1	3	38	$\overline{\text{EOC}}$	END OF CONVERSION
DATA BUS BIT 2	D2	4	37	$\overline{\text{EOT}}$	END OF TRACK
DATA BUS BIT 3	D3	5	36	VD-	NEGATIVE DIGITAL POWER
(LSB) DATA BUS BIT 4	D4	6	35	$\overline{\text{CAL}}$	CALIBRATE
DATA BUS BIT 5	D5	7	34	$\overline{\text{INTRLV}}$	INTERLEAVE
DATA BUS BIT 6	D6	8	33	BW	BUS WIDTH SELECT
DATA BUS BIT 7	D7	9	32	RST	RESET
DIGITAL GROUND	DGND	10	31	TST	TEST
POSITIVE DIGITAL POWER	VD+	11	30	VA-	NEGATIVE ANALOG POWER
DATA BUS BIT 8	D8	12	29	REFBUF	REFERENCE BUFFER OUTPUT
DATA BUS BIT 9	D9	13	28	VREF	VOLTAGE REFERENCE
DATA BUS BIT 10	D10	14	27	AGND	ANALOG GROUND
DATA BUS BIT 11	D11	15	26	AIN	ANALOG INPUT
DATA BUS BIT 12	D12	16	25	VA+	POSITIVE ANALOG POWER
DATA BUS BIT 13	D13	17	24	BP/$\overline{\text{UP}}$	BIPOLAR/UNIPOLAR SELECT
DATA BUS BIT 14	D14	18	23	A0	READ ADDRESS
(MSB) DATA BUS BIT 15	D15	19	22	$\overline{\text{RD}}$	READ
CLOCK INPUT	CLKIN	20	21	$\overline{\text{CS}}$	CHIP SELECT

CS5012A
CS5012



NOTE: All pin references in this data sheet refer to the 40-pin DIP package numbering. Use this figure to determine pin numbers for 44-pin package.

PIN DESCRIPTIONS

Power Supply Connections

VD+ – Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- – Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND – Digital Ground, PIN 10.
Digital ground.

VA+ – Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- – Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND – Analog Ground, PIN 27.
Analog ground.

Oscillator

CLKIN – Clock Input, PIN 20.
All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ – Hold, PIN 1.
A falling transition on this pin sets the CS5012A to the hold state and initiates a conversion. This input must remain low at least one CLKIN cycle plus 50 ns.

$\overline{\text{CS}}$ – Chip Select, PIN 21.
When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ – Read, PIN 22.
When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 – Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{UP}$ – Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format. Once calibration has been performed, either bipolar or unipolar mode may be selected without the need to recalibrate.

RST – Reset, PIN 32.

When taken high for at least 100 ns, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW – Bus Width Select, PIN 33.

When hard-wired high, all 12 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D0-D7. A second read cycle places the four LSB's with four trailing zeros on D0-D7. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D0-D7.

$\overline{INTRLV}$ – Interleave, PIN 34.

When latched low using $\overline{CS}$, the device goes into interleave calibration mode. A full calibration will complete every 2,014 conversions. The effective conversion time extends by 20 clock cycles.

CAL – Calibrate, PIN 35. (See Addendum appending this data sheet))

When latched high using $\overline{CS}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 58,280 CLKIN cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN – Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200 Ω.

VREF – Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 – Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{CS}$ and $\overline{RD}$, they offer the converter's 12-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register data.

$\overline{EOT}$ – End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal.

$\overline{EOC}$ – End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

3

SDATA – Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK – Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5012A. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF – Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST – Test, PIN 31.

Allows access to the CS5012A's test functions which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Throughput	Conversion Time	Maximum DNL	Temp. Range	Package
CS5012A-KP12	63 kHz	12.25 µs	±1/2 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5012A-KP7	100 kHz	7.20µs	±1/2 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5012A-KL12	63 kHz	12.25 µs	±1/2 LSB	0 to 70 °C	44-Pin PLCC
CS5012A-KL7	100 kHz	7.20 µs	±1/2 LSB	0 to 70 °C	44-Pin PLCC
CS5012A-BD12	63 kHz	12.25 µs	±1/2 LSB	-40 to +85 °C	40-Pin CerDIP
CS5012A-BD7	100 kHz	7.20 µs	±1/2 LSB	-40 to +85 °C	40-Pin CerDIP
CS5012A-BL12	63 kHz	12.25 µs	±1/2 LSB	-40 to +85 °C	44-Pin PLCC
CS5012A-BL7	100 kHz	7.20 µs	±1/2 LSB	-40 to +85 °C	44-Pin PLCC
CS5012A-TD12	63 kHz	12.25 µs	±1/2 LSB	-55 to +125 °C	40-Pin CerDIP
CS5012A-TD7	100 kHz	7.20 µs	±1/2 LSB	-55 to +125 °C	40-Pin CerDIP
CS5012A-TE12	63 kHz	12.25 µs	±1/2 LSB	-55 to +125 °C	44-Pin Ceramic LCC
CS5012A-TE7	100 kHz	7.20 µs	±1/2 LSB	-55 to +125 °C	44-Pin Ceramic LCC
CS5012-KP24	34 kHz	24.50 µs	±1/2 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5012-KP12	63 kHz	12.25 µs	±1/2 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5012-LP12	63 kHz	12.25 µs	±1/8 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5012-KL24	34 kHz	24.50 µs	±1/2 LSB	0 to 70 °C	44-Pin PLCC
CS5012-KL12	63 kHz	12.25 µs	±1/2 LSB	0 to 70 °C	44-Pin PLCC
CS5012-LL12	63 kHz	12.25 µs	±1/8 LSB	0 to 70 °C	44-Pin PLCC
CS5012-BD24	34 kHz	24.50 µs	±1/2 LSB	-40 to +85 °C	40-Pin CerDIP
CS5012-BD12	63 kHz	12.25 µs	±1/2 LSB	-40 to +85 °C	40-Pin CerDIP
CS5012-BL24	34 kHz	24.50 µs	±1/2 LSB	-40 to +85 °C	44-Pin PLCC
CS5012-BL12	63 kHz	12.25 µs	±1/2 LSB	-40 to +85 °C	44-Pin PLCC
CS5012-TD24	34 kHz	24.50 µs	±1/2 LSB	-55 to +125 °C	40-Pin CerDIP
CS5012-TD12	63 kHz	12.25 µs	±1/2 LSB	-55 to +125 °C	40-Pin CerDIP
CS5012-TE24	34 kHz	24.50 µs	±1/2 LSB	-55 to +125 °C	44-Pin Ceramic LCC
CS5012-TE12	63 kHz	12.25 µs	±1/2 LSB	-55 to +125 °C	44-Pin Ceramic LCC

3

The CS5012A is recommended for new designs. The following table shows the upgrade parts.

Old Part Number	New Design Recommended Device.
CS5012-KP24	CS5012A-KP12
CS5012-KP12	CS5012A-KP12
CS5012-KP7	CS5012A-KP7
CS5012-KL24	CS5012A-KL12
CS5012-KL12	CS5012A-KL12
CS5012-KL7	CS5012A-KL7
CS5012-BD24	CS5012A-BD12
CS5012-BD12	CS5012A-BD12
CS5012-BD7	CS5012A-BD7
CS5012-BL24	CS5012A-BL12
CS5012-BL12	CS5012A-BL12
CS5012-BL7	CS5012A-BL7
CS5012-TD24	CS5012A-TD12
CS5012-TD12	CS5012A-TD12
CS5012-TE24	CS5012A-TE12
CS5012-TE12	CS5012A-TE12

ADDENDUM

Burst Calibration in CS5012

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used in the CS5012. The silicon for the CS5012A has been revised to prevent this effect.

Interleave calibration works perfectly, provided it is not used intermittently in the CS5012.

The reset calibration always works perfectly, and typically should be used instead of burst mode. The CS5012's and CS5012A's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

Semiconductor Corporation

CS5014

14-Bit, 14 us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 14-Bit Precision
  - Linearity Error: ±1/4 LSB
  - Total Adjusted Error: ±1 LSB
  - No Missing Codes
- Low Distortion
  - Total Harmonic Distortion: 0.003%
  - Peak Harmonic or Noise: -98 dB
- 14.25 Microsecond Conversion Time
  - Throughout Rates up to 56 kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120 mW
- Pin Compatible with CS5012/CS5016

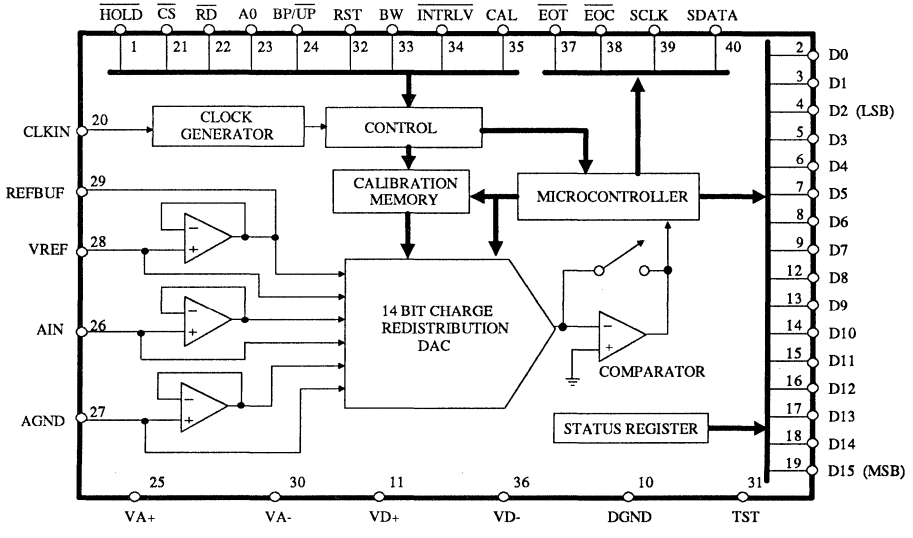
General Description

The CS5014 is a 14-bit monolithic analog to digital converter with a 14.25 µs conversion time. Unique self-calibration circuitry, which can be under intelligent control, insures maximum nonlinearity of 1/2 LSB and no missing codes. Offset and full scale errors are kept within 1/2 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5014 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75 µs to 0.003%, allowing throughput rates up to 56 kHz.

An evaluation board (CDB5014) is available for the CS5014 which can be easily configured to simulate any combination of operating conditions to greatly simplify system design and testing. The CS5014 is pin compatible with the CS5012 and CS5016 A/D converters allowing system upgrading and downgrading without hardware alterations

ORDERING INFORMATION: Page 3-63



ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; f_{clk} = 4 MHz for –14, 2 MHz for –28; Analog Source Impedance = 200 Ω)

Parameter *			CS5014-K min	CS5014-K typ	CS5014-K max	CS5014-B min	CS5014-B typ	CS5014-B max	CS5014-S,T min	CS5014-S,T typ	CS5014-S,T max	Units
Specified Temperature Range				0 to +70			-40 to +85			-55 to +125		°C
Accuracy												
Linearity Error	(Note 1)	K,B,T		± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
		S								± 1/2	± 1.5	LSB
Drift	(Note 2)			± 1/8			± 1/8			± 1/8		ΔLSB
Differential Linearity	(Note 1)			± 1/4	± 1/2		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Drift	(Note 2)			± 1/32			± 1/32			± 1/32		ΔLSB
Full Scale Error	(Note 1)			± 1/2	± 1		± 1/2	± 1		± 1/2	± 1	LSB
Drift	(Note 2)			± 1/4			± 1/4			± 1/2		ΔLSB
Unipolar Offset	(Note 1)	K,B,T		± 1/4	± 3/4		± 1/4	± 3/4		± 1/4	± 3/4	LSB
		S									± 1	LSB
Drift	(Note 2)			± 1/4			± 1/4			± 1/2		ΔLSB
Bipolar Offset	(Note 1)	K,B,T		± 1/4	± 3/4		± 1/4	± 3/4		± 1/4	± 3/4	LSB
		S									± 1	LSB
Drift	(Note 2)			± 1/4			± 1/2			± 1/2		ΔLSB
Bipolar Negative Full-Scale Error	(Note 1)											
		K,B,T		± 1/2	± 1		± 1/2	± 1		± 1/2	± 1	LSB
		S									± 1.5	LSB
Drift	(Note 2)			± 1/4			± 1/4			± 1/2		ΔLSB
Total Unadjusted Error	(Note 1)			± 1			± 1			± 1		LSB
Drift	(Note 2)			± 1/2			± 1			± 1		ΔLSB
Dynamic Performance	(Bipolar Mode)											
Peak Harmonic or Spurious Noise	(Note 1)											
Full-Scale, 1 kHz Input		K,B,T	94	98		94	98		94	98		dB
		S								85		dB
Full-Scale, 12 kHz Input		K,B,T	84	87		84	87		84	87		dB
		S								80		dB
Total Harmonic Distortion				0.003			0.003			0.003		%
Signal-to-Noise Ratio	(Note 1, 3)											
1 kHz, 0 dB Input		K,B,T	82	84		82	84		82	84		dB
		S								80		dB
1 kHz, -60 dB Input				23			23			23		dB
Noise	Unipolar Mode	(Note 4)		45			45			45		uV_{rms}
	Bipolar Mode			90			90			90		uV_{rms}

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Total drift over specified temperature range since calibration at power-up at 25 °C.
3. A detailed plot of S/(N+D) vs. input amplitude appears in Figure 16.
4. Wideband noise aliased into the baseband. Referred to the input.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter *	CS5014-K min	CS5014-K typ	CS5014-K max	CS5014-B min	CS5014-B typ	CS5014-B max	CS5014-S,T min	CS5014-S,T typ	CS5014-S,T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Aperture Time Matching (Note 5)		TBD			TBD			TBD		ns
Input Capacitance (Note 6)										
Unipolar Mode		275	375		275	375		275	375	pF
Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput										
Conversion Time −14			14.25			14.25			14.25	us
−28 (Notes 7, 8)			28.5			28.5			28.5	us
Acquisition Time −14		3.0	3.75		3.0	3.75		3.0	3.75	us
−28 (Note 8)		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput −14		55.6			55.6			55.6		kHz
−28 (Note 8)		27.7			27.7			27.7		kHz
Power Supplies										
DC Power Supply Currents (Note 9)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		−9	−19		−9	−19		−9	−19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		−3	−6		−3	−6		−3	−6	mA
Power Dissipation (Note 9)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 10)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

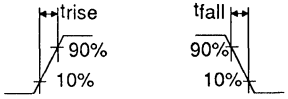
Notes:
5. Part to part.
6. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
7. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
8. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5014's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. Refer to the section *Conversion Time/Throughput* for a detailed discussion of conversion timing.
9. All outputs unloaded. All inputs CMOS levels.
10. With 300 mV p-p, 1 kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 21 shows a plot of typical power supply rejection versus frequency.

3

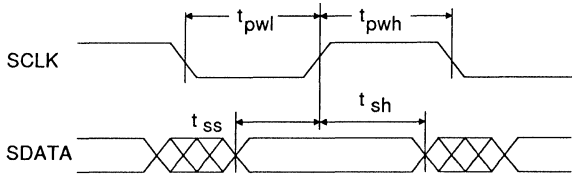
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF; BW = VD+)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: K,B,-14	f_{CLK}	2	-	-	MHz
S,T,-14		1.75			
-28		1	-	-	
Externally Supplied: -14		100 kHz	-	4	
-28		100 kHz	-	2	
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK}$ + 50	-	t_c	ns
Conversion Time	t_c	$57/f_{CLK}$	-	$61/f_{CLK}$+235	ns
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 11)	t_{epw}	$4/f_{CLK}$ - 20	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-K, B	t_{ca}	-	90	120	ns
-S, T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-K, B	t_{ra}	-	90	120	ns
-S, T		-	115	150	
Output Float Delay: -K, B	t_{fd}	-	90	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -S, T			90	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK}$ - 50	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK}$ - 100	$2/f_{CLK}$	-	ns

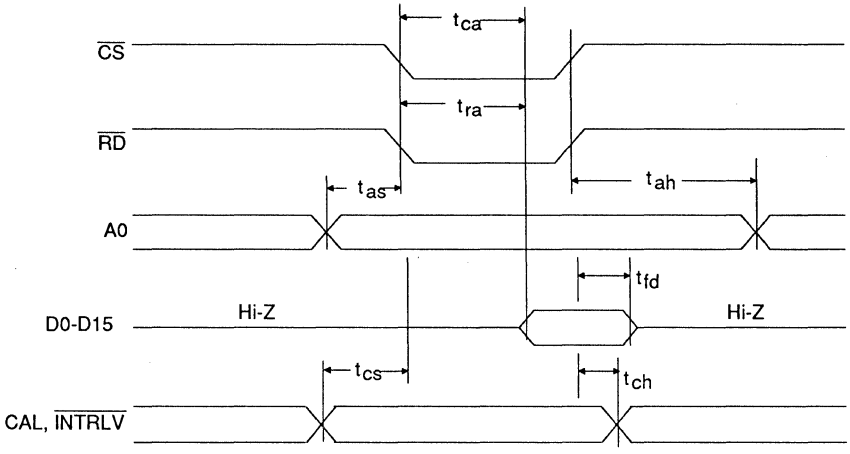
Note: 11. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 master clock cycles from the start of a data read operation or a conversion cycle.



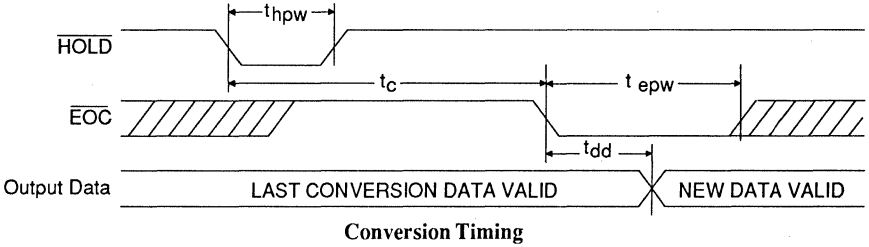
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	0.8	V
High-Level Output Voltage (Note 12)	V_{OH}	(VD+) - 1.0V	–	–	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	–	–	0.4	V
Input Leakage Current	I_{in}	–	–	10	uA
3-State Leakage Current	I_{OZ}	–	–	±10	uA
Digital Output Pin Capacitance	C_{out}	–	9	–	pF

Note: 12. I_{out} = -100 µA. This specification guarantees TTL compatability (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 13.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage: (Note 14)	Unipolar	V_{AIN}	AGND	–	VREF	V
	Bipolar	V_{AIN}	-VREF	–	VREF	V

Notes: 13. All voltages with respect to ground.

14. The CS5014 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 15)		I_{in}	–	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VA+) + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 15. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

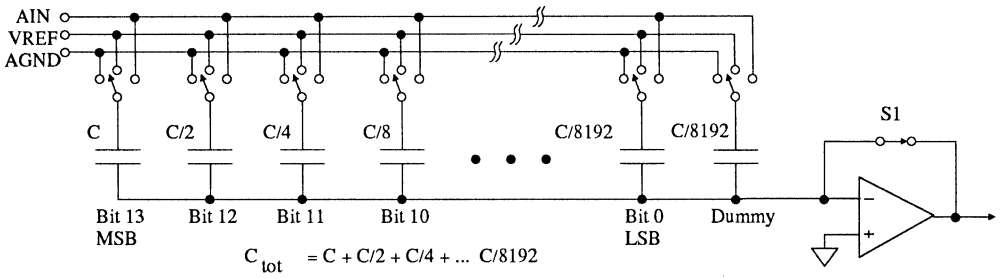


Figure 1. Charge Redistribution DAC

The CS5014 utilizes a successive approximation conversion technique. The analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

The CS5014 implements the successive-approximation algorithm using a unique charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

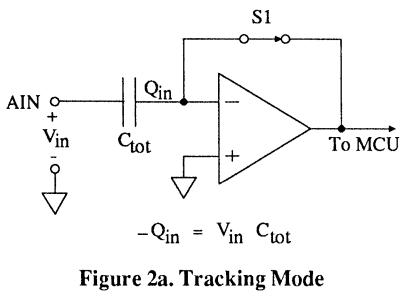


Figure 2a. Tracking Mode

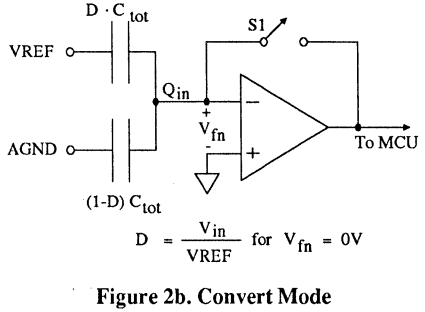


Figure 2b. Convert Mode

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

The CS5014's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5014 to convert accurately to 14-bits clearly depends on the accuracy of its comparator and DAC. The CS5014 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 14-bit accuracy from the DAC, the CS5014 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

DIGITAL CIRCUIT CONNECTIONS

The CS5014 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CS5014 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5014 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

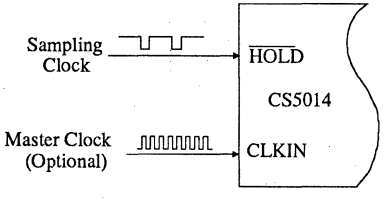


Figure 3a. Asynchronous Sampling

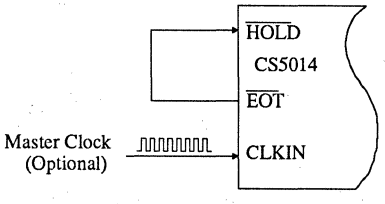


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CS5014's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -14 version of the CS5014 is specified for accurate operation with an external clock up to 4 MHz; its internal clock frequency is specified at a minimum of 2 MHz. The -28 version can handle external clocks up to 2 MHz; its internal clock can range as low as 1 MHz (see the table, *Switching Characteristics*, at the front of this data sheet). Both versions can typically convert with clocks as low as 10 kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. Upon completion of the conversion cycle, the CS5014 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the device's decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5014's base address will initiate a conversion. However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset* below).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are also internally latched by $\overline{\text{CS}}$, so they must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5014's base address will initiate or terminate calibration. Alternatively, A0, $\overline{\text{INTRLV}}$, and CAL may be connected to the microprocessor data bus.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5014 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25 µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5014, in turn, depends on the

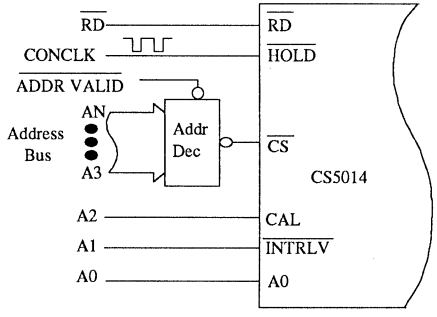


Figure 4a. Conversions Asynchronous to Master Clock

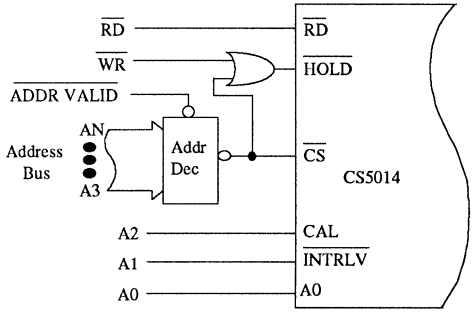


Figure 4b. Conversions under Microprocessor Control

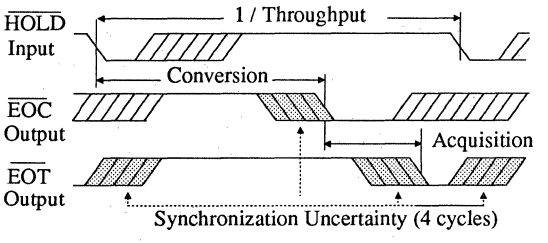


Figure 5a. Asynchronous Sampling (External Clock)

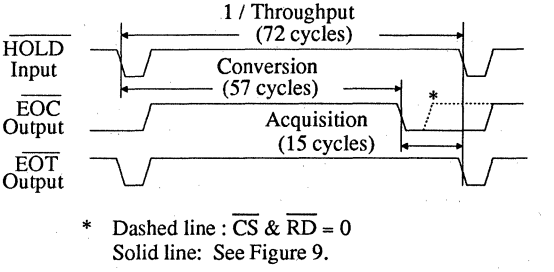


Figure 5b. Synchronous (Loopback) Mode

sampling, calibration, and master clock conditions.

Asynchronous Sampling

The CS5014 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 57 clock cycles to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CS5014's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/72th of the master clock frequency (see Figure 5b and Table 1).

Also, the CS5014's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CS5014 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

Reset

Upon power up, the CS5014 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5014's low power dissipation and low temperature drift, no warm-up time is required before reset to ac-

Sampling Mode	Conversion Time Min	Conversion Time Max	Throughput Time Min	Throughput Time Max
Synchronous (Loopback)	$57\,t_{clk}$	$57\,t_{clk}$	$72\,t_{clk}$	$72\,t_{clk}$
Asynchronous	$57\,t_{clk}$	$61\,t_{clk}$ + 235 ns	N/A	$67\,t_{clk}$ + 2.25 us

Table 1. Conversion and Throughput Times (t_{clk} = Master Clock Period)

commodate any self-heating effects. However, the voltage reference input should have stabilized to within 1% of its final value before RST falls to guarantee an accurate calibration. Later, the CS5014 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5014 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

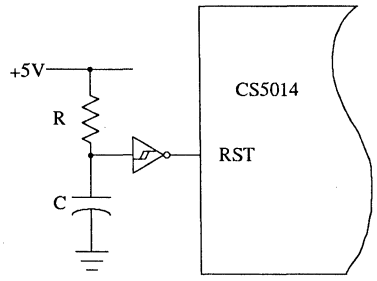


Figure 6. Power-On Reset Circuit

Resets can be initiated in hardware or software. The simplest method of resetting the CS5014 involves strobing the RST pin high for at least 100 ns. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,441,020 master clock cycles (approximately 360 ms with a 4 MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmitt-trigger inverter to prevent oscillation (see Figure 6). The CS5014 can also be reset in software when under microprocessor control. The CS5014 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section (below) to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5014 is ready for operation. Six master clock cycles plus 2.25 µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5014's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is normally only required once, after power-up.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25 µs (8.75 µs @ 4 MHz clock) must be allowed before a conversion is initiated to ensure the CS5014 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See the *Addendum* which appends this data sheet.)

The CS5014 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5014 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,051

conversions). Initiated by bringing both the $\overline{\text{INTRLV}}$ input and $\overline{\text{CS}}$ low (or hard-wiring $\overline{\text{INTRLV}}$ low), interleave extends the CS5014's effective conversion time by 20 master clock cycles (5 µs @ 4 MHz). Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CS5014 sees free time. Interleave is subordinate to burst calibrations, so $\overline{\text{INTRLV}}$ could still be externally tied low. If used, interleave should be left active continuously.

The fact that the CS5014 offers several calibration modes is not to imply that the device needs to be recalibrated often. The device is very stable in the presence of large temperature changes. Tests have indicated that after using a single reset calibration at 25 °C most devices exhibit very little change in offset or gain when exposed to temperatures from -55 to +125 °C. The data indicated 30 ppm as the typical worst case total change in offset or gain over this temperature range. Differential linearity remained virtually unchanged. System error sources outside of the A/D converter, whether due to changes in temperature or to long-term aging, will generally dominate total system error.

Microprocessor Interface

The CS5014 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low enables the CS5014's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{\text{HOLD}}$ is low, or a software reset will result* (see *Reset* above).

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{\text{END OF CONVERSION}}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{\text{HIGH BYTE}}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{\text{END OF TRACK}}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the input.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Pin Definitions

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle.

To interface with a 16-bit data bus, the BW input to the CS5014 should be held high and all 14 data bits read in parallel on pins D2-D15. With an 8-bit bus, the converter's 14-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 6 LSB's with 2 trailing zeros. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5014 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5014 is converting will not introduce conversion errors. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

Microprocessor Independent Operation

The CS5014 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low. This permanently enables the 3-state output buffers and allows transparent latch inputs (CAL and $\overline{INTRLV}$) to be active. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The CS5014's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100 ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

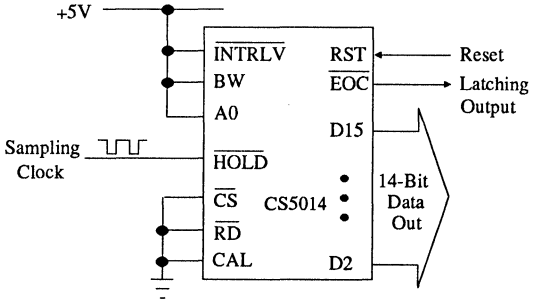


Figure 8. Microprocessor-Independent Connections

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
Status (A0=0)	X	X	X	X	X	X	X	X	S7	S6	S5	S4	S3	S2	S1	S0	8- or 16-Bit Data Bus
Data (A0=1)	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	0	0	16-Bit Bus (BW=1)
	X	X	X	X	X	X	X	X	B13	B12	B11	B10	B9	B8	B7	B6	8-Bit Bus (BW=0)
									B5	B4	B3	B2	B1	B0	0	0	

"X" Denotes High Impedance Output

Figure 7. Data Format

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5014 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5014 (See Figure 9).

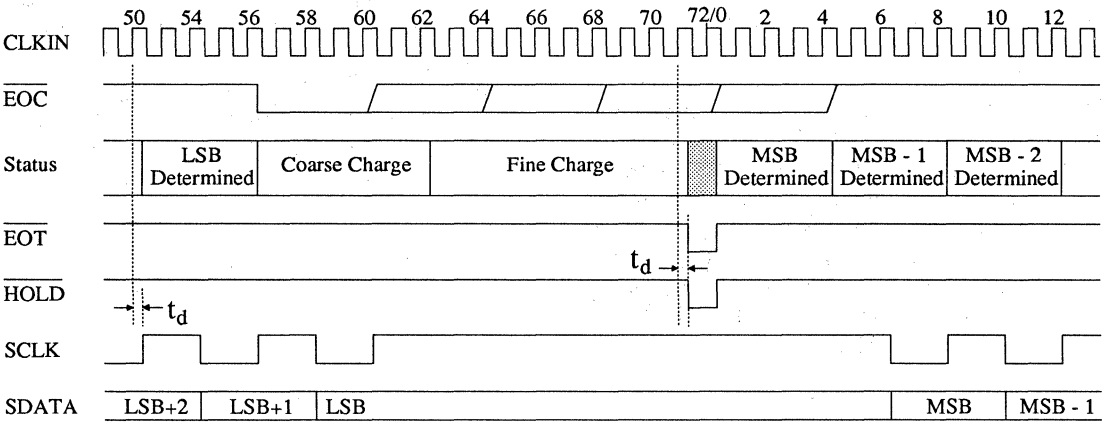
ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5014 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X/CSZ511X Series of A/D Converters*" is available for the CS5014. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5014 in-



Notes: 1. Synchronous (loopback) mode is illustrated. After $\overline{EOC}$ falls the converter goes into coarse charge mode for 6 CLKIN cycles, then to fine charge mode for 9 cycles, then $\overline{EOT}$ falls. In loopback mode, $\overline{EOT}$ trips $\overline{HOLD}$ which captures the analog sample. Conversion begins on the next rising edge of CLKIN. If operated asynchronously, $\overline{EOT}$ will remain low until after $\overline{HOLD}$ is taken low. When $\overline{HOLD}$ occurs the analog sample is captured immediately, but conversion may not begin until four CLKIN cycles later.

2. Timing delay td (relative to CLKIN) can vary between 135 ns to 235 ns over the military temperature range and over ± 10% supply variation
3. $\overline{EOC}$ returns high in 4 CLKIN cycles if A0 = 1 and $\overline{CS}$ = $\overline{RD}$ = 0 (Microprocessor Independent Mode); within 4 CLKIN cycles after a data read (Microprocessor Mode); or 4 CLKIN cycles after $\overline{HOLD}$ = 0 is recognized on a rising edge of CLKIN/4.

Figure 9. Serial Output Timing

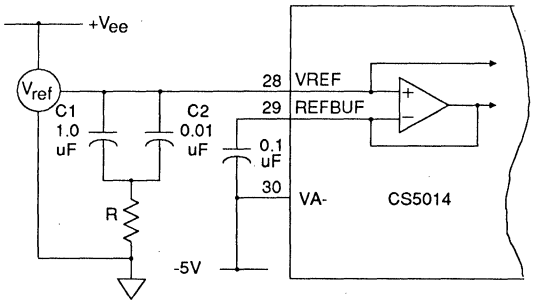
cludes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5014 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4 MHz clock), the reference must supply a maximum load current of 10 µA peak-to-peak (1 µA typical). An output impedance of 4 Ω will therefore yield a maximum error of 40 µV. With a 4.5V reference and LSB size of 275 µV, this would insure better than 1/4 LSB accuracy. A 2.2 µF capacitor exhibits an impedance of less than 4 Ω at frequencies greater than 5 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.



$$R = \frac{1}{2\pi (C_1 + C_2) f_{peak}}$$

Figure 10. Reference Connections

The CS5014 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5014 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X/CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

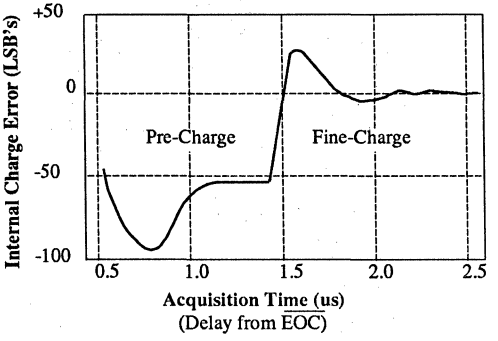


Figure 11. Internal Acquisition Time

The acquisition time of the CS5014 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -14 version with an external 4 MHz master clock results in a 3.75 µs acquisition time: 1.5 µs for pre-charging (6 clock cycles) and 2.25 µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25 µs for an analog source impedance of less than 200 Ω. In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input applications, consult the application note: *Input Buffer Amplifiers for the CS501X Family of A/D Converters.*

During the first six clock cycles following a conversion (pre-charge), the CS5014 is capable of slewing at 5 V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5014 can slew at 10 V/µs. After the first six master clock cycles, it will slew at 0.25 V/µs in the unipolar mode and 0.5 V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5014 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CS5014 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111, and negative full scale gives a digital output of 0000000000000.

The BP/$\overline{UP}$ mode pin may be switched after calibration without having to recalibrate the converter. However, the BP/$\overline{UP}$ mode should be changed during the previous conversion cycle, that is, between $\overline{HOLD}$ falling and $\overline{EOC}$ falling.

If BP/$\overline{UP}$ is changed at any other time, one dummy conversion cycle must be allowed for proper acquisition of the input.

Grounding and Power Supply Decoupling

The CS5014 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference point.

The digital and analog supplies are isolated within the CS5014 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5014 must never exceed the positive analog supply by more than a diode drop or the CS5014 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram in Figure 22 shows a decoupling scheme which allows the CS5014 to be powered from a single set of ± 5V rails.

As with any high-precision A/D converter, the CS5014 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5014. The CDB5014 evaluation board is available for the CS5014, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5014, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

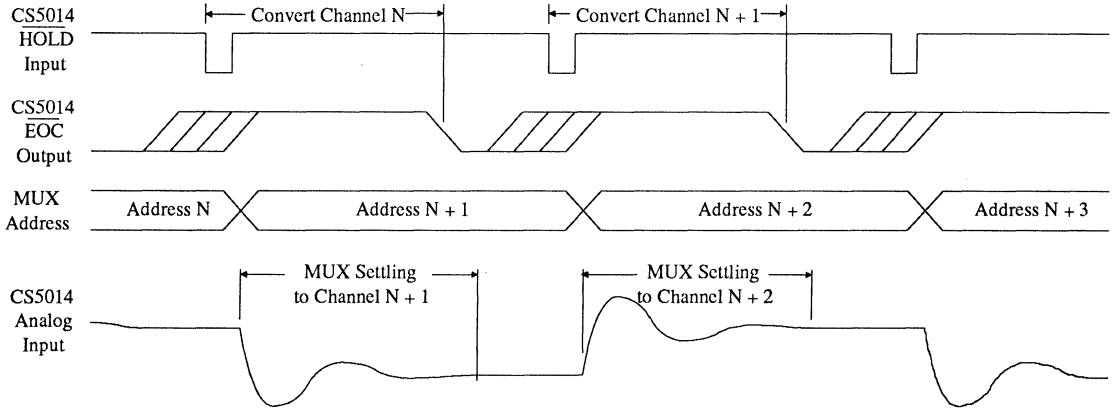


Figure 12. Pipelined MUX Input Channels

CS5014 PERFORMANCE

Differential Nonlinearity

One source of nonlinearity in A/D converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5014 calibrates all bits in the capacitor array to a small fraction of an LSB resulting in nearly ideal DNL. A histogram plot of typical DNL can be seen in Figure 13.

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows in the transfer curve generate harmonic distortion. The worst-case condition of bit-weight errors (DNL) has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CS5014 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CS5014 calibrates its bit weights to within ± 1/16 LSB at 14-bits (± 0.0004% FS) yielding peak distortion as low as -100 dB (see Figure 14). Unlike traditional ADC's, the linearity of the CS5014 is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

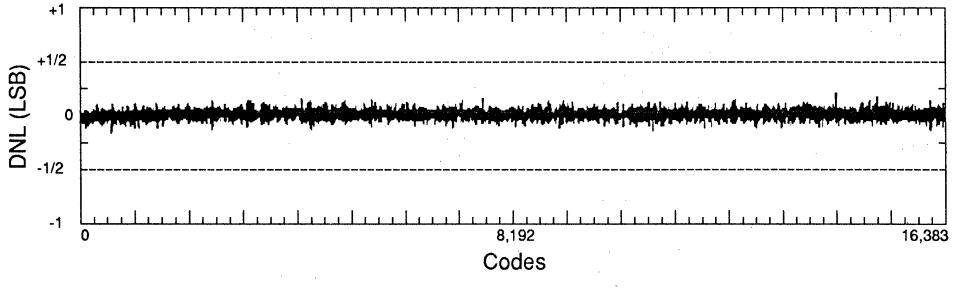


Figure 13. CS5014 Differential Nonlinearity Plot

FFT Tests and Windowing

In the factory, the CS5014 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5014, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5014.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CS5014 has a maximum side-lobe level of -92 dB. Figure 14 shows an FFT computed from an ideal 14-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is

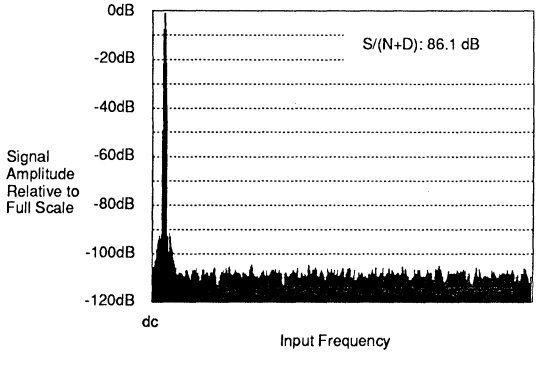


Figure 14. FFT Plot of Ideal 14-bit Signal

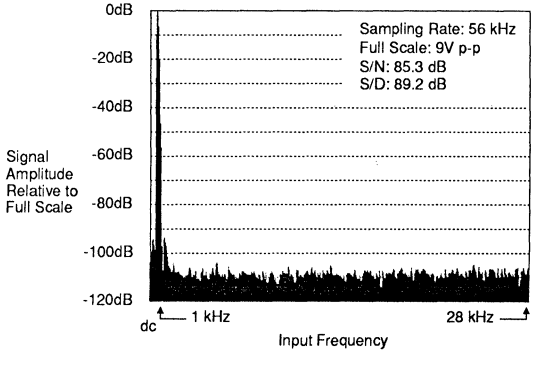


Figure 15. FFT Plot with 1 kHz Full-Scale Input

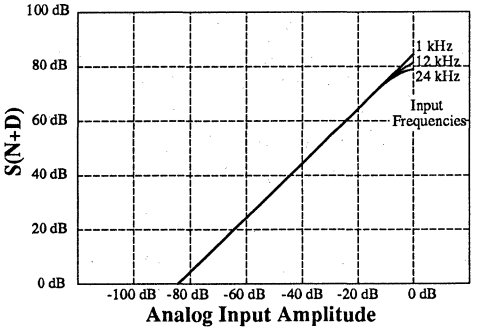


Figure 16. S/(N+D) vs. Input Amplitude (9V p-p Full-Scale Input)

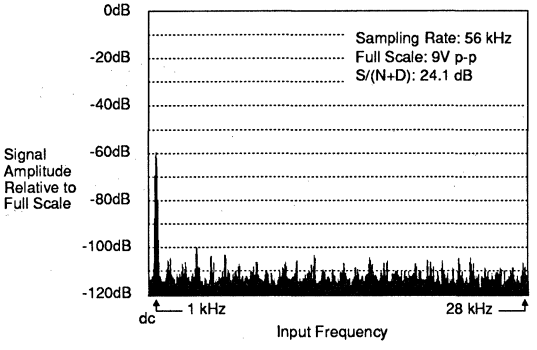


Figure 17. FFT Plot with 1 kHz -60 dB Input

± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ± 1/2 LSB, but any value within this range has equal probability of occurance. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 14-bit signal-to-noise ratio of 86 dB.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

As illustrated in Figures 16 and 17, the CS5014's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals.

Sampling Distortion

The ultimate limitation on the CS5014's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 15).

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figure 16 since the magnitude of the steady state current increases. First noticeable at 1 kHz, this distortion assumes a linear relationship with input frequency. With signals 20 dB or more below full-scale, it no

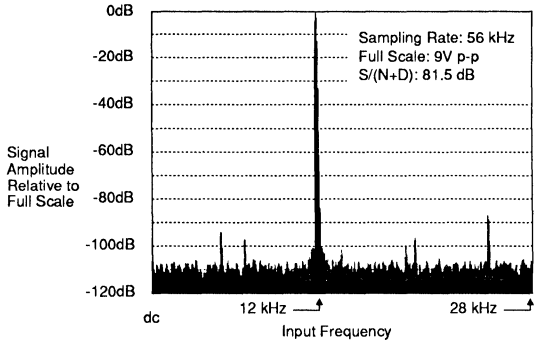


Figure 18. FFT Plot with 12 kHz Full-Scale Input

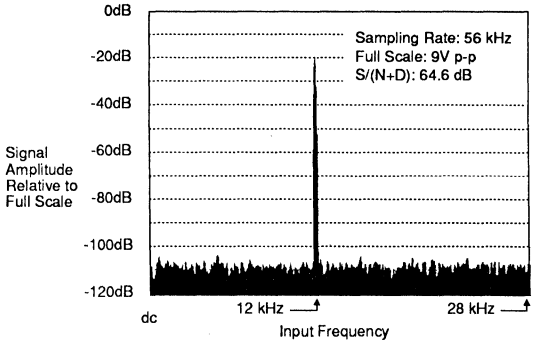


Figure 19. FFT Plot with 12 kHz -20 dB Input

longer dominates the converter's overall S/(N+D) performance (Figures 18 and 19).

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5014 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5014 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5014's analog input and master clock.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200 Ω	80uV	325uV

Figure 20. Examples of Measured Clock Feedthrough

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5014's output. The offset could theoretically reach the peak coupling magnitude (Figure 20), but the probability of this occurring is small since the peaks are spikes of short duration.

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CS5014's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (N f_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CS5014's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 20, a typi-

cal CS5014 operating with its internal oscillator at 2 MHz and 50 Ω of analog input source impedance will exhibit only 15 µV rms of clock feedthrough. However, if a 2 MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25 µV rms. Feedthrough also increases with clock frequency; a 4 MHz clock yields 40 µV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 20, reducing source impedance from 50 Ω to 25 Ω yields a 15 µV rms reduction in feedthrough. Therefore, when operating the CS5014 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5014's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5014 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Power Supply Rejection

The CS5014's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5014's accuracy. This, of course, is because the CS5014 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 21 shows power supply rejection of the CS5014 in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

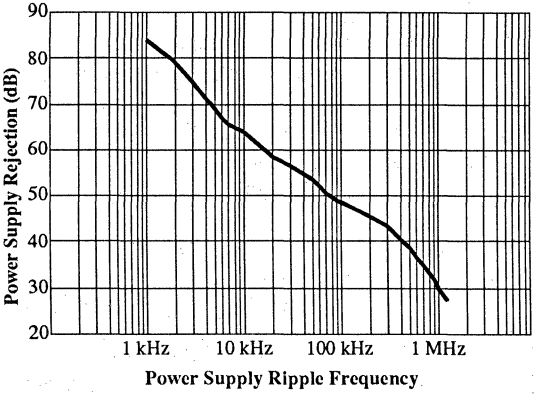


Figure 21. Power Supply Rejection

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

Table 3. CS5014 Truth Table

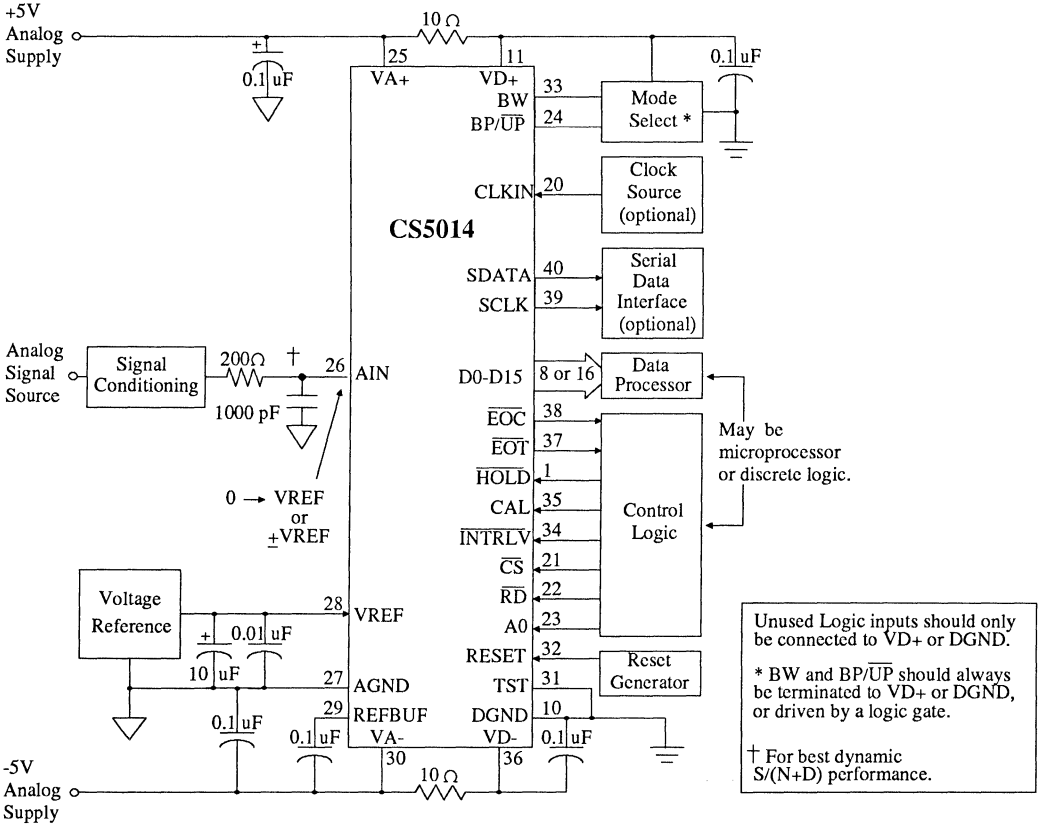
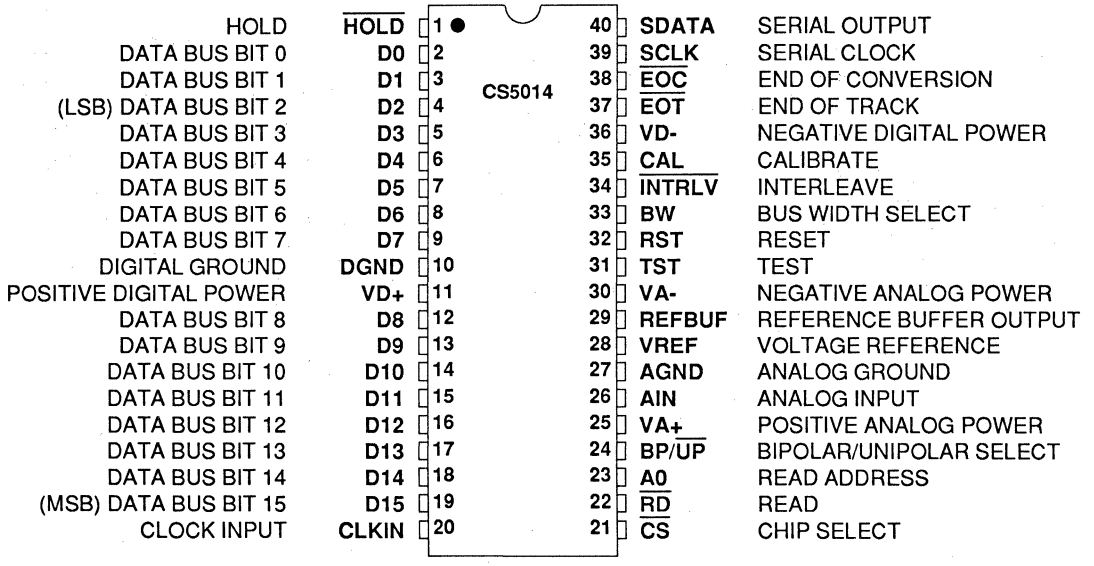
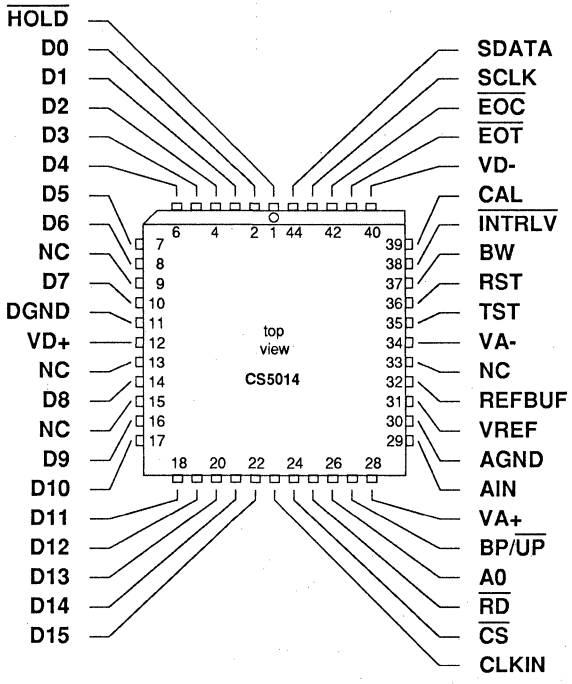


Figure 22. CS5014 System Connection Diagram





NOTE: All pin references in this data sheet refer to the 40-pin DIP package numbering. Use this figure to determine pin numbers for 44-pin package.

PIN DESCRIPTIONS

Power Supply Connections

VD+ – Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- – Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND – Digital Ground, PIN 10.
Digital ground.

VA+ – Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- – Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND – Analog Ground, PIN 27.
Analog ground.

Oscillator

CLKIN – Clock Input, PIN 20.
All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ – Hold, PIN 1.
A falling transition on this pin sets the CS5014 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50 ns.

$\overline{\text{CS}}$ – Chip Select, PIN 21.
When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ – Read, PIN 22.
When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 – Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{UP}$ – Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format. Once calibration has been performed, either bipolar or unipolar may be selected without the need to recalibrate.

RST – Reset, PIN 32.

When taken high for at least 100 ns, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW – Bus Width Select, PIN 33.

When hard-wired high, all 14 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D0-D7. A second read cycle places the six LSB's with two trailing zeros on D0-D7. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D0-D7.

$\overline{INTRLV}$ – Interleave, PIN 34.

When latched low using $\overline{CS}$, the device goes into interleave calibration mode. A full calibration will complete every 72,051 conversions. The effective conversion time extends by 20 clock cycles.

CAL – Calibrate, PIN 35. (See Addendum appending this data sheet))

When latched high using $\overline{CS}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,441,020 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN – Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200 Ω.

VREF – Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 – Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{CS}$ and $\overline{RD}$, they offer the converter's 14-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register.

$\overline{EOT}$ – End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75 µs for 4 MHz external clock).

$\overline{EOC}$ – End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

3

SDATA – Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK – Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5014. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF – Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST – Test, PIN 31.

Allows access to the CS5014's test functions which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Throughput	Conversion Time	Linearity	Temp. Range	Package
CS5014-KP28	28 kHz	28.50 µs	±0.5 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5014-KP14	56 kHz	14.25 µs	±0.5 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5014-KL28	28 kHz	28.50 µs	±0.5 LSB	0 to 70 °C	44-Pin PLCC
CS5014-KL14	56 kHz	14.25 µs	±0.5 LSB	0 to 70 °C	44-Pin PLCC
CS5014-BD28	28 kHz	28.50 µs	±0.5 LSB	-40 to +85 °C	40-Pin CerDIP
CS5014-BD14	56 kHz	14.25 µs	±0.5 LSB	-40 to +85 °C	40-Pin CerDIP
CS5014-BL28	28 kHz	28.50 µs	±0.5 LSB	-40 to +85 °C	44-Pin PLCC
CS5014-BL14	56 kHz	14.25 µs	±0.5 LSB	-40 to +85 °C	44-Pin PLCC
CS5014-SD14	56 kHz	14.25 µs	±1.5 LSB	-55 to +125 °C	40-Pin CerDIP
CS5014-TD14	56 kHz	14.25 µs	±0.5 LSB	-55 to +125 °C	40-Pin CerDIP
CS5014-SE14	56 kHz	14.25 µs	±1.5 LSB	-55 to +125 °C	44-Pin Ceramic LCC
CS5014-TE14	56 kHz	14.25 µs	±0.5 LSB	-55 to +125 °C	44-Pin Ceramic LCC

3

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

Interleave calibration works perfectly, provided it is not used intermittently.

The reset calibration always works perfectly, and typically should be used instead of burst mode. The CS5014's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

• Notes •

Semiconductor Corporation

CS5016

16-Bit, 16 us Self-Calibrating A/D Converter

Features

- Monolithic CMOS A/D converter
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 16-Bit Precision
  - Linearity Error: 0.001% FS
  - No Missing Codes
- Ultra-Low Distortion
  - Total Harmonic Distortion: 0.001%
  - Peak Harmonic or Noise: -104 dB
- 16.25 µs Conversion Time
  - Sample Rates up to 50 kHz
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 120 mW
- Pin Compatible with CS5012/CS5014

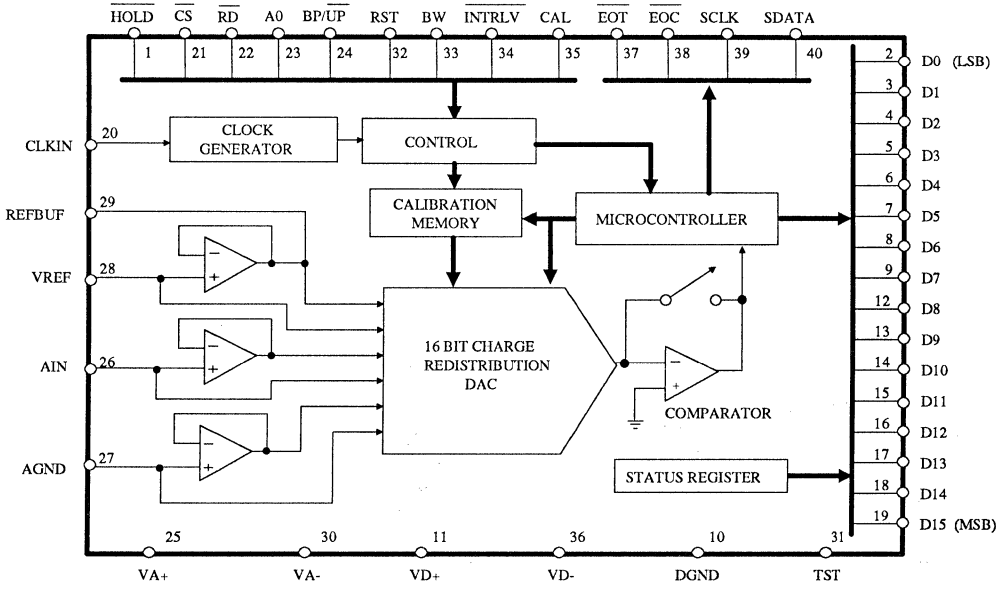
General Description

The CS5016 is a 16-bit monolithic analog to digital converter with a 16.25 µs conversion time. Unique self-calibration circuitry insures maximum nonlinearity of 0.001% FS and no missing codes. This insures low distortion and maintains good signal to noise performance with low-level signals. Offset and full scale errors are kept within 1 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5016 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75 µs to 0.01%, allowing throughput rates up to 50 kHz.

An evaluation board (CDB5016) is available for the CS5016 which can be easily configured to simulate any combination of operating conditions to greatly simplify system design and testing.

ORDERING INFORMATION: Page 8-94



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; f_{clk} = 4 MHz for -16, 2 MHz for -32; Analog Source Impedance = 200 Ω; Synchronous Sampling.)

Parameter *			CS5016 -J,K min	CS5016 -J,K typ	CS5016 -J,K max	CS5016 -A,B min	CS5016 -A,B typ	CS5016 -A,B max	CS5016 -S,T min	CS5016 -S,T typ	CS5016 -S,T max	Units
Specified Temperature Range				0 to +70			-40 to +85			-55 to +125		°C
Accuracy												
Linearity Error	(Note 1)	-J,A,S		0.002	0.003		0.002	0.003		0.002	0.0076	% FS
		-K,B,T		0.001	0.0015		0.001	0.0015		0.001	0.0015	% FS
	(Note 3)	Drift		± 1/4			± 1/4			± 1/4		Δ LSB
Differential Linearity		(Note 2)	16			16			16			Bits
Full Scale Error	(Note 1)	-J,A,S		± 2	± 3		± 2	± 3		± 2	± 4	LSB
		-K,B,T		± 2	± 3		± 2	± 3		± 2	± 3	LSB
	(Note 3)	Drift		± 1			± 1			± 2		Δ LSB
Unipolar Offset	(Note 1)	-J,A,S		± 1	± 2		± 1	± 3		± 1	± 4	LSB
		-K,B,T		± 1	± 3/2		± 1	± 3		± 1	± 3	LSB
	(Note 3)	Drift		± 1			± 1			± 2		Δ LSB
Bipolar Offset	(Note 1)	-J,A,S		± 1	± 2		± 1	± 2		± 1	± 4	LSB
		-K,B,T		± 1	± 3/2		± 1	± 2		± 1	± 2	LSB
	(Note 3)	Drift		± 1			± 2			± 2		Δ LSB
Bipolar Negative Full-Scale Error	(Note 1)	-J,A,S		± 2	± 3		± 2	± 3		± 2	± 5	LSB
		-K,B,T		± 2	± 3		± 2	± 3		± 2	± 3	LSB
	(Note 3)	Drift		± 1			± 2			± 2		Δ LSB
Dynamic Performance		(Bipolar Mode)										
Peak Harmonic or Spurious Noise												
Full-Scale, 1kHz Input	(Note 1)	-J,A,S	96	100		96	100		92	100		dB
		-K,B,T	100	104		100	104		100	104		dB
Full-Scale, 12kHz Input		-J,A,S	85	88		85	88		82	88		dB
		-K,B,T	85	91		85	91		85	91		dB
Total Harmonic Distortion												
Full-Scale, 1kHz Input		-J,A,S		0.002			0.002			0.002		%
		-K,B,T		0.001			0.001			0.001		%
Signal-to-Noise Ratio												
1kHz, 0dB Input		-J,A,S	87	90		87	90		84	90		dB
	(Note 1, 4)	-K,B,T	90	92		90	92		90	92		dB
1kHz, -60dB Input		-J,A,S		30			30			30		dB
		-K,B,T		32			32			32		dB
Noise		Unipolar Mode		35			35			35		uV_{rms}
(Note 5)		Bipolar Mode		70			70			70		uV_{rms}

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Minimum resolution for which no missing codes is guaranteed.
3. Total drift over specified temperature range since calibration at power-up at 25 °C.
4. Refer to Figure 16 for a detailed plot of S/(N+D) vs. Input Amplitude.
5. Wideband noise aliased into the baseband. Referred to the input.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

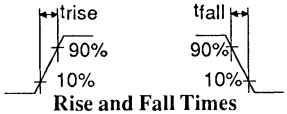
Parameter *	CS5016 -J,K min	typ	max	CS5016 -A,B min	typ	max	CS5016 -S,T min	typ	max	Units
Specified Temperature Range	0 to +70			-40 to +85			-55 to +125			°C
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Aperture Time Matching (Note 6)		TBD			TBD			TBD		ns
Input Capacitance (Note 7)										
Unipolar Mode		275	375		275	375		275	375	pF
Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput										
Conversion Time −16			16.25			16.25			16.25	us
(Notes 8, 9) −32			32.5			32.5			32.5	us
Acquisition Time −16		3.0	3.75		3.0	3.75		3.0	3.75	us
(Note 9) −32		4.5	5.25		4.5	5.25		4.5	5.25	us
Throughput −16	50			50			50			kHz
(Note 9) −32	26.5			26.5			26.5			kHz
Power Supplies										
Power Supply Currents (Note 10)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		−9	−19		−9	−19		−9	−19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		−3	−6		−3	−6		−3	−6	mA
Power Dissipation (Note 10)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 11)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

Notes:
6. Part to part.
7. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
8. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
9. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5016's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. Refer to the section *Conversion Time/Throughput* for a detailed discussion of conversion timing.
10. All outputs unloaded. All inputs CMOS levels.
11. With 300 mV p-p, 1 kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 22 shows a plot of typical power supply rejection versus frequency.

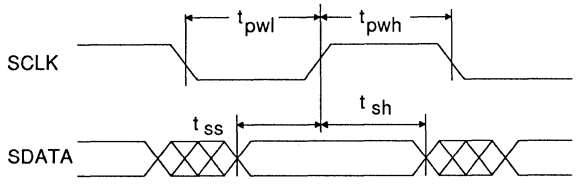
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF; BW = VD+)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: J,K,A,B, -16	f_{CLK}	2	-	-	MHz
S,T, -16		1.75	-	-	
-32		1	-	-	
Externally Supplied: -16		100 kHz	-	4	
-32		100 kHz	-	2	
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	$65/f_{CLK}$	-	$69/f_{CLK} + 235$	ns
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 12)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-J,K,A,B	t_{ca}	-	90	120	ns
-S,T		-	115	150	
$\overline{RD}$ Low to Data Valid					
-J,K,A,B	t_{ra}	-	90	120	ns
-S,T		-	115	150	
Output Float Delay: -J,K,A,B	t_{fd}	-	90	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -S,T			90	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 50$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

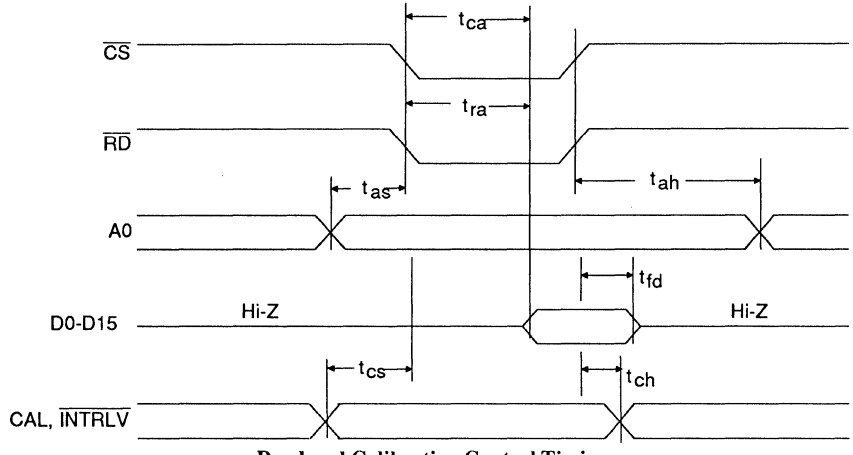
Note: 12. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 master clock cycles from the start of a data read operation or a conversion cycle.



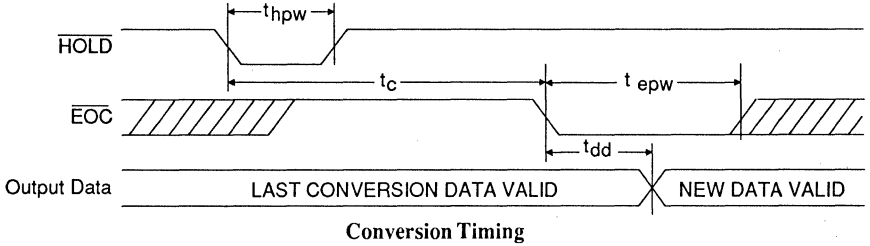
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	–	–	V
Low-Level Input Voltage	V_{IL}	–	–	0.8	V
High-Level Output Voltage (Note 13)	V_{OH}	(VD+) - 1.0V	–	–	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	–	–	0.4	V
Input Leakage Current	I_{in}	–	–	10	uA
3-State Leakage Current	I_{OZ}	–	–	±10	uA
Digital Output Pin Capacitance	C_{out}	–	9	–	pF

Note: 13. I_{out} = -100 µA. This specification guarantees TTL compatability (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 14.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	–	VREF	V
(Note 15)	Bipolar	V_{AIN}	-VREF	–	VREF	V

Notes: 14. All voltages with respect to ground.

15. The CS5016 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 16)		I_{in}	–	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VA+) + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 16. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

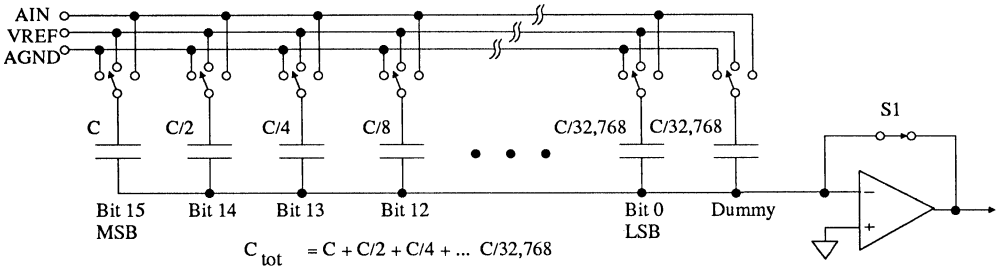


Figure 1. Charge Redistribution DAC

The CS5016 utilizes a successive approximation conversion technique. The analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

The CS5016 implements the successive-approximation algorithm using a unique charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

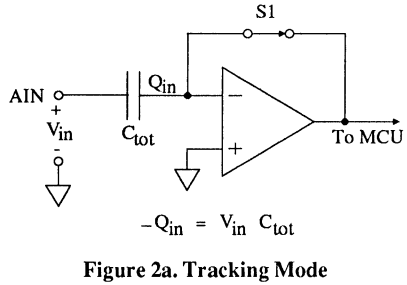


Figure 2a. Tracking Mode

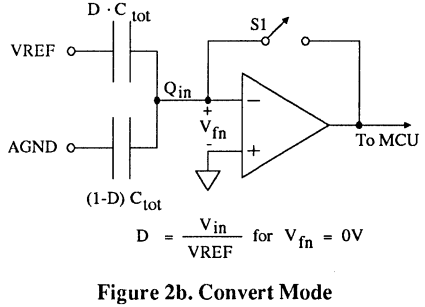


Figure 2b. Convert Mode

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

The CS5016's charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5016 to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. The CS5016 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CS5016 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). During calibration, the CS5016 implements statistical noise reduction to calibrate accurately to ± 1/4 LSB. It performs multiple experiments per calibration decision to reduce the effective noise bandwidth and the probability of making an incorrect decision.

DIGITAL CIRCUIT CONNECTIONS

The CS5016 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the device's conversion time and throughput. The device also features on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CS5016 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5016 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

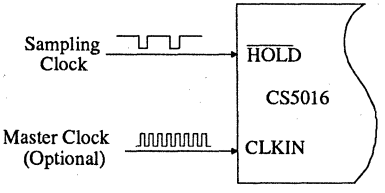


Figure 3a. Asynchronous Sampling

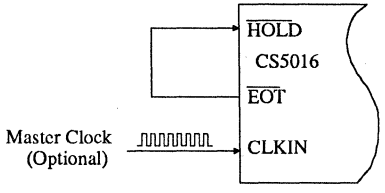


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the CS5016's internal oscillator will vary from unit-to-unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The -16 version of the CS5016 is specified for accurate operation with an external clock up to 4 MHz; its internal clock frequency is specified at a minimum of 2 MHz. The -32 version can handle external clocks up to 2 MHz; its internal clock can range as low as 1 MHz (see the table, *Switching Characteristics*, at the front of this data sheet). Both versions can typically convert with clocks as low as 10 kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. Upon completion of the conversion cycle, the CS5016 automatically returns to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one master clock cycle plus 50 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the device's decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5016's base address will initiate a conversion. However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset* below).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are also internally latched by $\overline{\text{CS}}$, so they must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5016's base address will initiate or terminate calibration. Alternatively, A0, $\overline{\text{INTRLV}}$, and CAL may be connected to the microprocessor data bus.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5016 requires time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six master clock cycles plus 2.25 µs. This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5016, in turn, depends

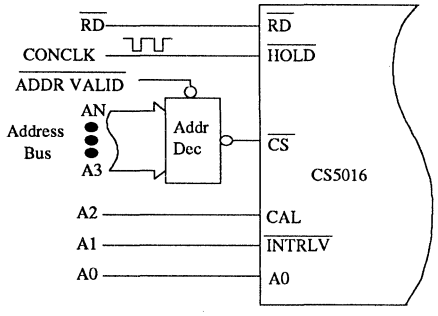


Figure 4a. Conversions Asynchronous to Master Clock

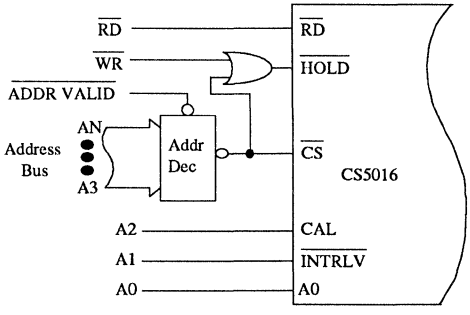


Figure 4b. Conversions under Microprocessor Control

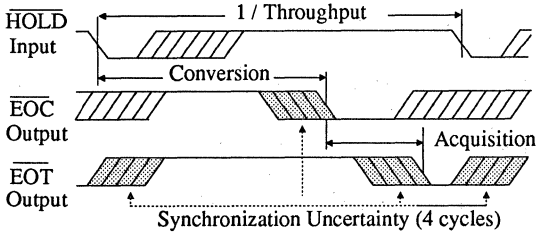


Figure 5a. Asynchronous Sampling (External Clock)

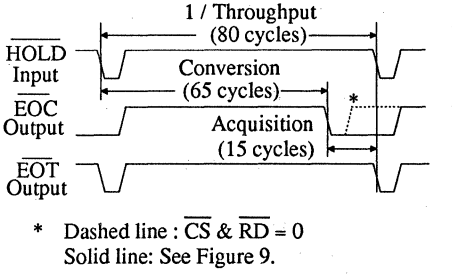


Figure 5b. Synchronous (Loopback) Mode

on the sampling, calibration, and master clock conditions.

Asynchronous Sampling

The CS5016 internally operates from a clock which is delayed and divided down from the master clock ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 65 clock cycles to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 master clock cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CS5016's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at 1/80th of the master clock frequency (see Figure 5b and Table 1).

Also, the CS5016's internal RC oscillator exhibits significant jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CS5016 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity.

Reset

Upon power up, the CS5016 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5016's low power dissipation and low temperature drift, no warm-up time is required before reset to ac-

Sampling Mode	Conversion Time Min	Conversion Time Max	Throughput Time Min	Throughput Time Max
Synchronous (Loopback)	$65\,t_{clk}$	$65\,t_{clk}$	$80\,t_{clk}$	$80\,t_{clk}$
Asynchronous	$65\,t_{clk}$	$69\,t_{clk}$ + 235 ns	N/A	$75\,t_{clk}$ + 2.25 us

Table 1. Conversion and Throughput Times (t_{clk} = Master Clock Period)

commodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before RST falls to guarantee an accurate calibration. Later, the CS5016 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5016 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

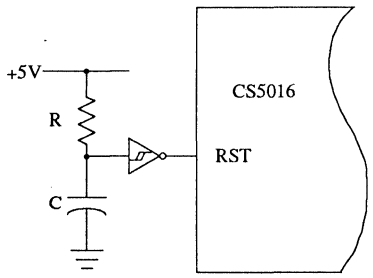


Figure 6. Power-On Reset Circuit

Resets can be initiated in hardware or software. The simplest method of resetting the CS5016 involves strobing the RST pin high for at least 100 ns. When RST is brought high all internal logic clears. When it returns low a full calibration begins which takes 1,441,020 master clock cycles (approximately 360 ms with a 4 MHz clock) to complete. A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmitt-trigger inverter to prevent oscillation (see Figure 6). The CS5016 can also be reset in software when under microprocessor control. The CS5016 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section (below) to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5016 is ready for operation. Six master clock cycles plus 2.25 µs must be allowed after $\overline{EOC}$ falls to allow for acquisition. Under microprocessor-independent operation with 3-states permanently enabled ($\overline{CS}$, $\overline{RD}$ low; A0 high) the $\overline{EOC}$ output will not fall at the completion of the reset operation.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5016's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is normally only required once, after power-up.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, "burst" cal, is useful when the ADC sees some downtime but not enough to perform a full reset calibration. Burst cal can be terminated mid-calibration; it picks up where it left off previously, so calibrations can be done in piecemeal fashion. Burst cal is initiated by bringing the CAL input high with $\overline{CS}$ low. The CAL input is level-triggered and latches on the rising edge of $\overline{CS}$, so a write cycle can be used to control calibration in software. Burst cal will continue to loop through calibration cycles until terminated. Once CAL returns low, at least 26 master clock cycles plus 2.25 µs (8.75 µs @ 4 MHz clock) must be allowed before a conversion is initiated to ensure the CS5016 has completed its calibration experiment and has acquired the analog input. The $\overline{EOC}$ output indicates the completion of the final calibration experiment. (See the *Addendum* which appends this data sheet.)

The CS5016 features a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5016 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 72,051

conversions). Initiated by bringing both the $\overline{\text{INTRLV}}$ input and $\overline{\text{CS}}$ low (or hard-wiring $\overline{\text{INTRLV}}$ low), interleave extends the CS5016's effective conversion time by 20 master clock cycles (5 µs @ 4 MHz). Other than reduced throughput, interleave is totally transparent to the user.

Burst calibrations initiated at CAL pick up where interleave left off, so calibration cycles can be hastened by "bursting" a number of experiments whenever the CS5016 sees free time. Interleave is subordinate to burst calibrations, so $\overline{\text{INTRLV}}$ could still be externally tied low. If used, interleave should be left active continuously.

The fact that the CS5016 offers several calibration modes is not to imply that the device needs to be recalibrated often. The device is very stable in the presence of large temperature changes. Tests have indicated that after using a single reset calibration at 25 °C most devices exhibit very little change in offset or gain when exposed to temperatures from -55 to +125 °C. The data indicated 30 ppm as the typical worst case total change in offset or gain over this temperature range. Differential linearity remained virtually unchanged. System error sources outside of the A/D converter, whether due to changes in temperature or to long-term aging, will generally dominate total system error.

Microprocessor Interface

The CS5016 features an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low enables the CS5016's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{\text{HOLD}}$ is low, or a software reset will result* (see *Reset* above).

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	$\overline{\text{END OF CONVERSION}}$	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/$\overline{\text{HIGH BYTE}}$	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	$\overline{\text{END OF TRACK}}$	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the input.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Pin Definitions

Alternatively, the End-of-Convert ($\overline{EOC}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{EOC}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four master clock cycles of the first subsequent data read operation or after the start of a new conversion cycle.

To interface with a 16-bit data bus, the BW input to the CS5016 should be held high and all 16 data bits read in parallel on pins D0-D15. With an 8-bit bus, the converter's 16-bit result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the 8 LSB's. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5016 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5016 is converting will not introduce conversion errors. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

Microprocessor Independent Operation

The CS5016 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low. This permanently enables the 3-state output buffers and allows transparent latch inputs (CAL and $\overline{INTRLV}$) to be active. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The CS5016's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four master clock cycles after each conversion. Data will be unstable up to 100 ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

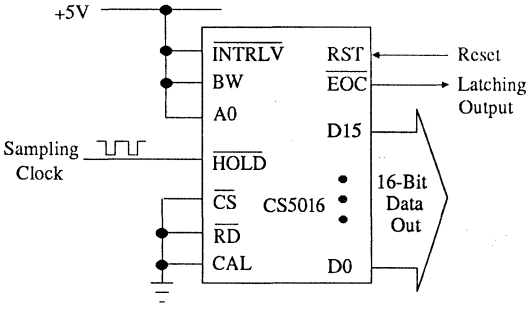


Figure 8. Microprocessor-Independent Connections

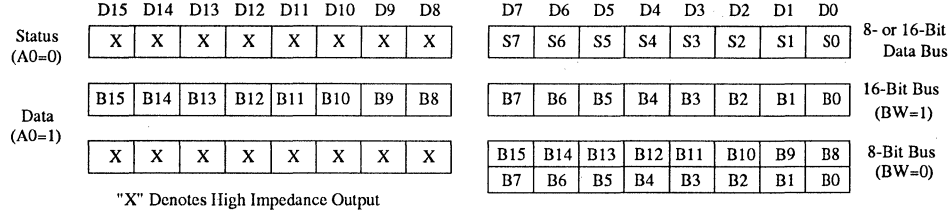


Figure 7. Data Format

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5016 presents each bit to the SDATA pin four master clock cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5016 (See Figure 9).

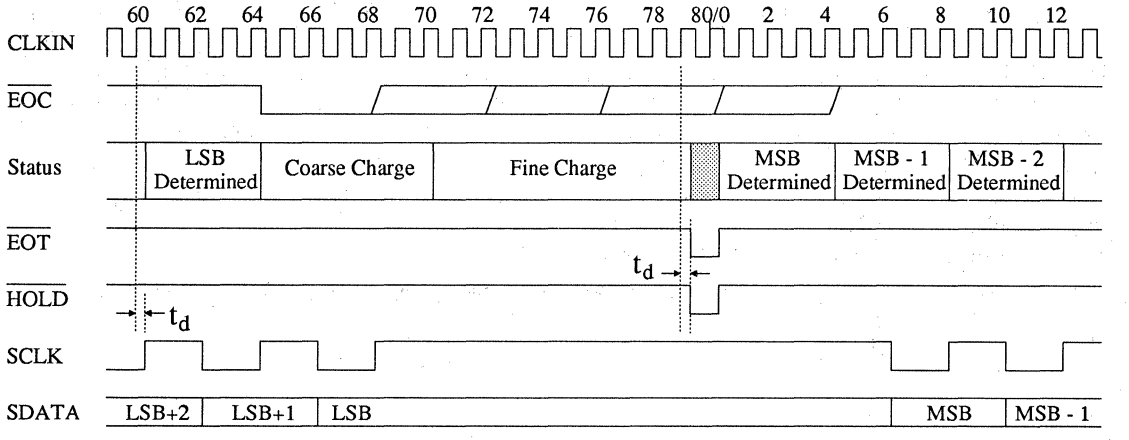
ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5016 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X/CSZ511X Series of A/D Converters*" is available for the CS5016. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5016 in-



Notes: 1. Synchronous (loopback) mode is illustrated. After $\overline{EOC}$ falls the converter goes into coarse charge mode for 6 CLKIN cycles, then to fine charge mode for 9 cycles, then $\overline{EOT}$ falls. In loopback mode, $\overline{EOT}$ trips $\overline{HOLD}$ which captures the analog sample. Conversion begins on the next rising edge of CLKIN. If operated asynchronously, $\overline{EOT}$ will remain low until after $\overline{HOLD}$ is taken low. When $\overline{HOLD}$ occurs the analog sample is captured immediately, but conversion may not begin until four CLKIN cycles later.

2. Timing delay td (relative to CLKIN) can vary between 135 ns to 235 ns over the military temperature range and over ± 10% supply variation

3. $\overline{EOC}$ returns high in 4 CLKIN cycles if A0 = 1 and $\overline{CS}$ = $\overline{RD}$ = 0 (Microprocessor Independent Mode); within 4 CLKIN cycles after a data read (Microprocessor Mode); or 4 CLKIN cycles after $\overline{HOLD}$ = 0 is recognized on a rising edge of CLKIN/4.

Figure 9. Serial Output Timing

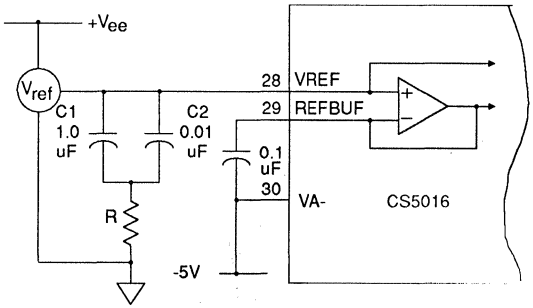
cludes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5016 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At full speed (4 MHz clock), the reference must supply a maximum load current of 10 µA peak-to-peak (1 µA typical). An output impedance of 2 Ω will therefore yield a maximum error of 20 µV. With a 4.5V reference and LSB size of 69 µV, this would insure approximately 1/4 LSB accuracy. A 10 µF capacitor exhibits an impedance of less than 2 Ω at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.



$$R = \frac{1}{2\pi (C_1 + C_2) f_{peak}}$$

Figure 10. Reference Connections

The CS5016 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5016 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X/CSZ511X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

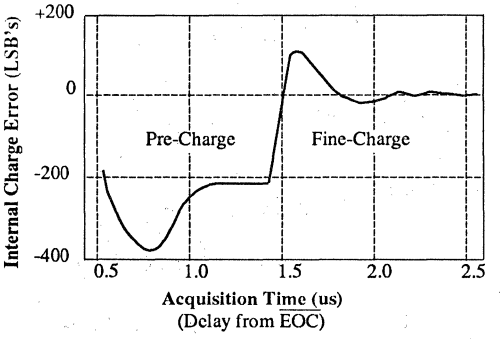


Figure 11. Internal Acquisition Time

The acquisition time of the CS5016 depends on the master clock frequency. This is due to a fixed pre-charge period. For instance, operating the -16 version with an external 4 MHz master clock results in a 3.75 µs acquisition time: 1.5 µs for pre-charging (6 clock cycles) and 2.25 µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25 µs for an analog source impedance of less than 200 Ω. In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input applications, consult the application note: *Input Buffer Amplifiers for the CS501X Family of A/D Converters.*

During the first six clock cycles following a conversion (pre-charge), the CS5016 is capable of slewing at 5 V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5016 can slew at 10 V/µs. After the first six master clock cycles, it will slew at 0.25 V/µs in the unipolar mode and 0.5 V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5016 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CS5016 can convert at full speed.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of 1111111111111111, and negative full scale gives a digital output of 0000000000000000.

The BP/$\overline{UP}$ mode pin may be switched after calibration without having to recalibrate the converter. However, the BP/$\overline{UP}$ mode should be changed during the previous conversion cycle, that is, between $\overline{HOLD}$ falling and $\overline{EOC}$ falling.

If BP/$\overline{UP}$ is changed at any other time, one dummy conversion cycle must be allowed for proper acquisition of the input.

Grounding and Power Supply Decoupling

The CS5016 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference point.

The digital and analog supplies are isolated within the CS5016 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5016 must never exceed the positive analog supply by more than a diode drop or the CS5016 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram in Figure 23 shows a decoupling scheme which allows the CS5016 to be powered from a single set of ± 5V rails.

As with any high-precision A/D converter, the CS5016 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5016. The CDB5016 evaluation board is available for the CS5016, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5016, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

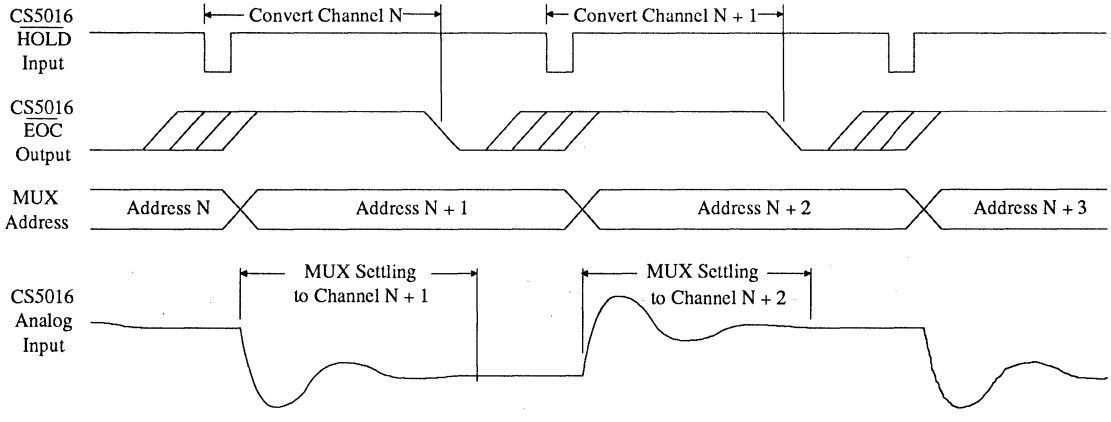


Figure 12. Pipelined MUX Input Channels

CS5016 PERFORMANCE

Differential Nonlinearity

One source of nonlinearity in A/D converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5016 calibrates all bits in the capacitor array to within ± 1/4 LSB resulting in nearly ideal DNL. A histogram plot of typical DNL can be seen in Figure 13.

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows in the transfer curve generate harmonic distortion. The worst-case condition of bit-weight errors (DNL) has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CS5016 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CS5016 calibrates its bit weights to within ± 1/4 LSB at 16-bits (± 0.0004% FS) yielding peak distortion as low as -105 dB (see Figure 14). Unlike traditional ADC's, the linearity of the CS5016 is not limited by bit-weight errors; its performance is therefore extremely repeatable and independent of input signal conditions.

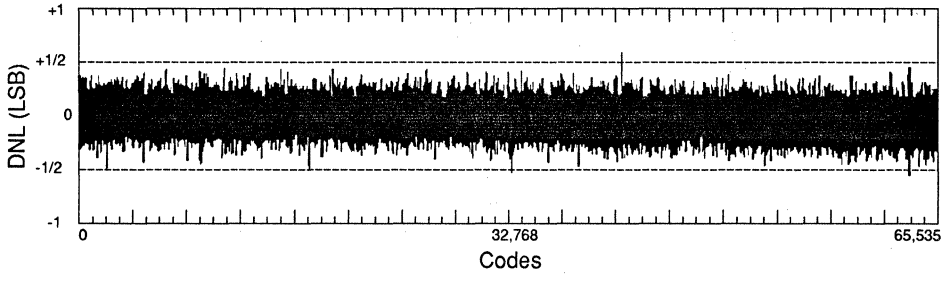


Figure 13. CS5016 Differential Nonlinearity Plot

FFT Tests and Windowing

In the factory, the CS5016 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5016, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5016.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CS5016 has a maximum side-lobe level of -92 dB. Figure 14 shows an FFT computed from an ideal 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is

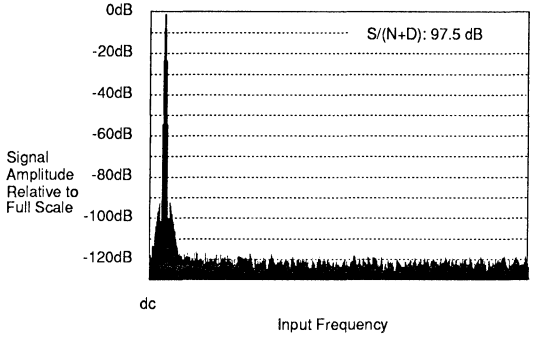


Figure 14. FFT Plot of Ideal 16-bit Signal

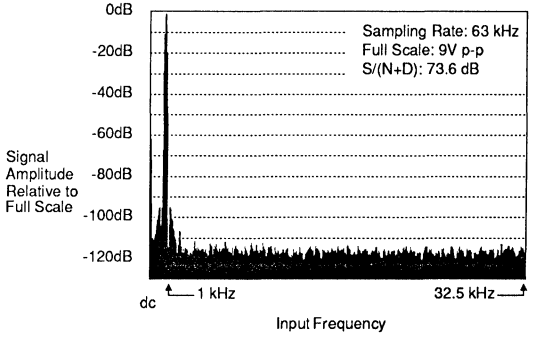


Figure 15. FFT Plot with 1 kHz Full-Scale Input

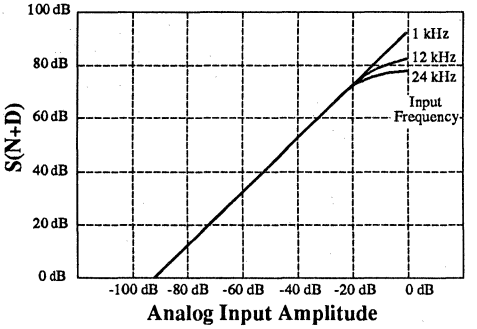


Figure 16. S/(N+D) vs. Input Amplitude (9V p-p Full-Scale Input)

± 1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ± 1/2 LSB, but any value within this range has equal probability of occurance. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to an ideal 16-bit signal-to-noise ratio of 97.7 dB.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

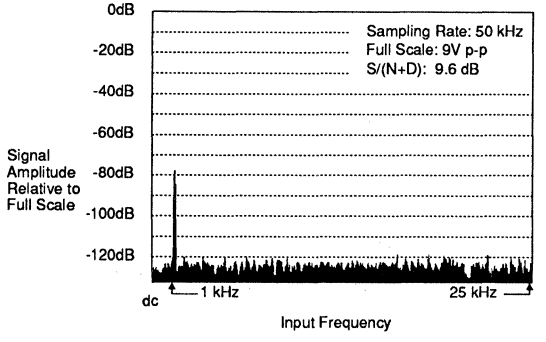


Figure 17. FFT Plot with 1 kHz -80 dB Input

As illustrated in Figures 16 and 17, the CS5016's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals. In fact, quantization noise remains below the noise floor in the CS5016 which dictates the converter's signal-to-noise performance.

Noise

All analog circuitry in the CS5016 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5016 integrates to 35 µV rms in unipolar mode (70 µV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 18 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a CS5016 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the CS5016 has a "bell" shape with all codes other than 80CD due to internal noise.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5016 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 µV rms in unipolar mode.

Noise can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the

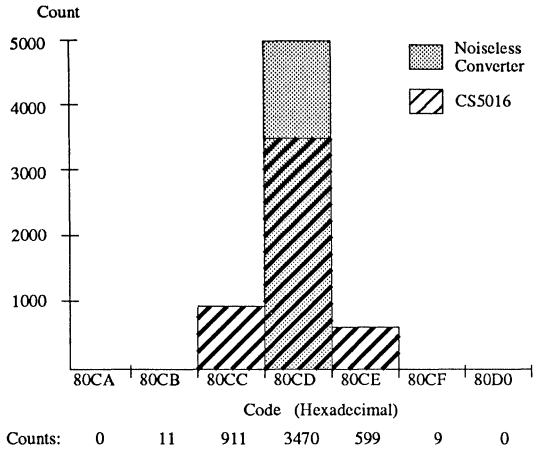


Figure 18. Histogram Plot of 5000 Conversion Inputs

CS5016's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the CS5016's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50 kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

Sampling Distortion

The ultimate limitation on the CS5016's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the HOLD command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 15).

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figure 16 since the magnitude of the steady state current increases.

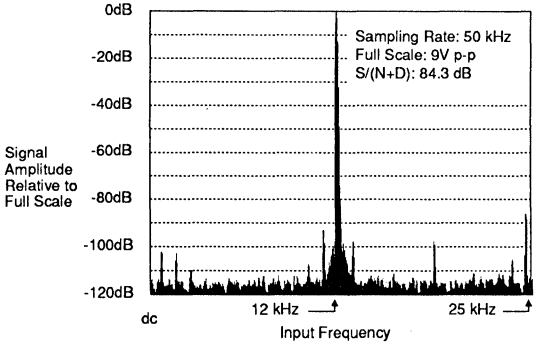


Figure 19. FFT Plot with 12 kHz Full-Scale Input

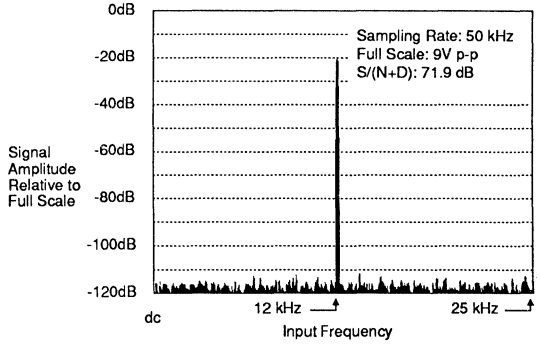


Figure 20. FFT Plot with 12 kHz -20 dB Input

First noticeable at 1 kHz, this distortion assumes a linear relationship with input frequency. With signals 20 dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figures 19 and 20).

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5016 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

Clock Feedthrough

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5016 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5016's analog input and master clock.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200 Ω	80uV	325uV

Figure 21. Examples of Measured Clock Feedthrough

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5016's output. The offset could theoretically reach the peak coupling magnitude (Figure 21), but the probability of this occurring is small since the peaks are spikes of short duration.

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CS5016's output. With a fixed sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (N f_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CS5016's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 21, a typical CS5016 operating with its internal oscillator at 2 MHz and 50 Ω of analog input source impedance will exhibit only 15 µV rms of clock feedthrough. However, if a 2 MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25 µV rms. Feedthrough also increases with clock frequency; a 4 MHz clock yields 40 µV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 21, reducing source impedance from 50 Ω to 25 Ω yields a 15 µV rms reduction in feedthrough. Therefore, when operating the CS5016 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5016's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5016 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Power Supply Rejection

The CS5016's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5016's accuracy. This, of course, is because the CS5016 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 22 shows power supply rejection of the CS5016 in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

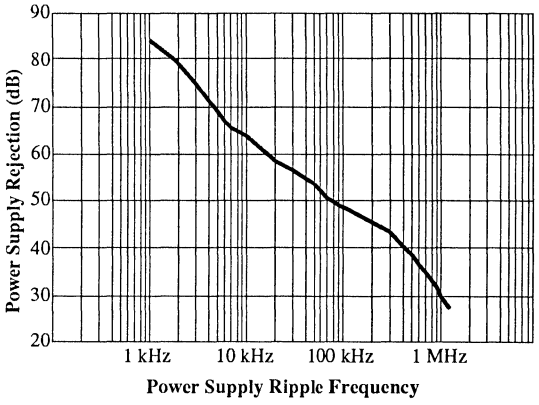


Figure 22. Power Supply Rejection

3

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

Table 3. CS5016 Truth Table

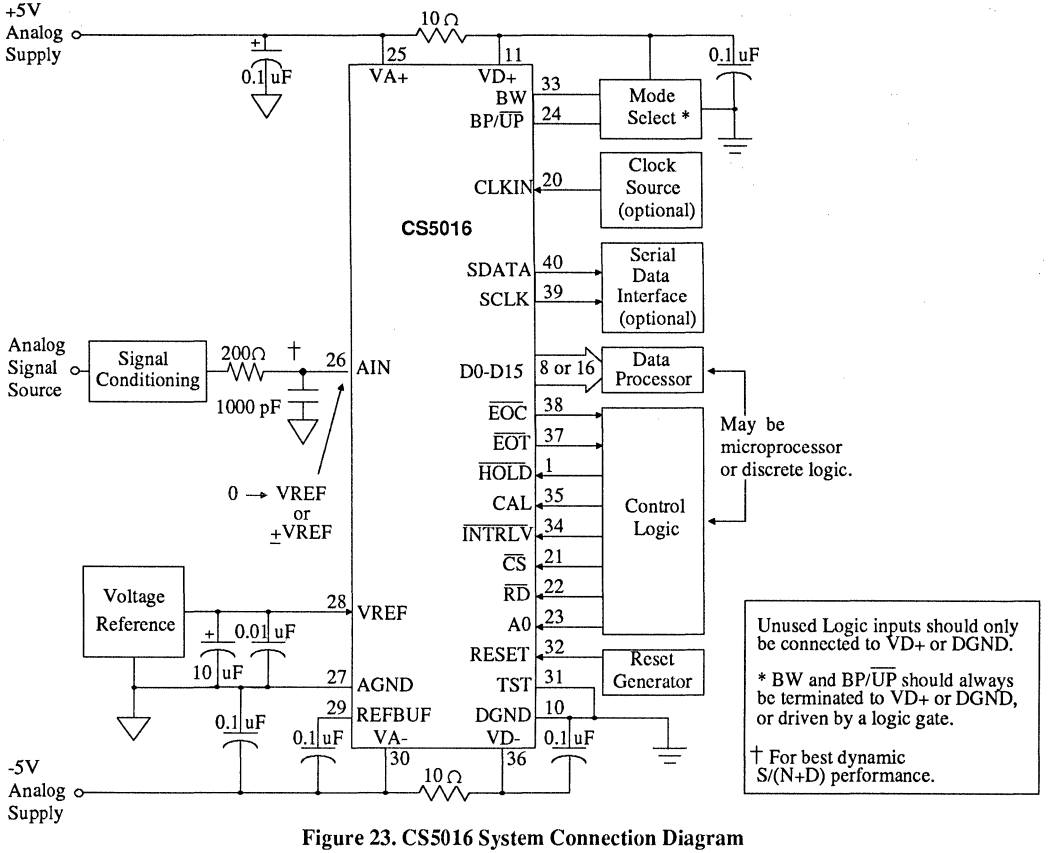
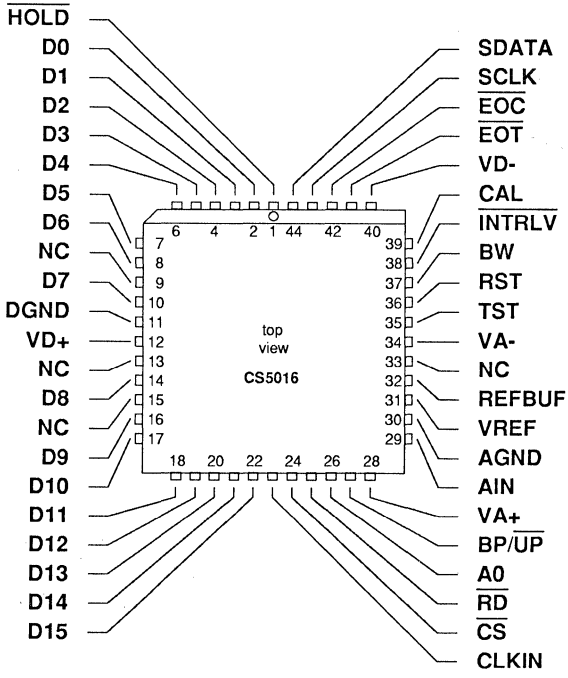


Figure 23. CS5016 System Connection Diagram

HOLD	HOLD	1	40	SDATA	SERIAL OUTPUT
(LSB) DATA BUS BIT 0	D0	2	39	SCLK	SERIAL CLOCK
DATA BUS BIT 1	D1	3	38	EOC	END OF CONVERSION
DATA BUS BIT 2	D2	4	37	EOT	END OF TRACK
DATA BUS BIT 3	D3	5	36	VD-	NEGATIVE DIGITAL POWER
DATA BUS BIT 4	D4	6	35	CAL	CALIBRATE
DATA BUS BIT 5	D5	7	34	INTRLV	INTERLEAVE
DATA BUS BIT 6	D6	8	33	BW	BUS WIDTH SELECT
DATA BUS BIT 7	D7	9	32	RST	RESET
DIGITAL GROUND	DGND	10	31	TST	TEST
POSITIVE DIGITAL POWER	VD+	11	30	VA-	NEGATIVE ANALOG POWER
DATA BUS BIT 8	D8	12	29	REFBUF	REFERENCE BUFFER OUTPUT
DATA BUS BIT 9	D9	13	28	VREF	VOLTAGE REFERENCE
DATA BUS BIT 10	D10	14	27	AGND	ANALOG GROUND
DATA BUS BIT 11	D11	15	26	AIN	ANALOG INPUT
DATA BUS BIT 12	D12	16	25	VA+	POSITIVE ANALOG POWER
DATA BUS BIT 13	D13	17	24	BP/UP	BIPOLAR/UNIPOLAR SELECT
DATA BUS BIT 14	D14	18	23	A0	READ ADDRESS
(MSB) DATA BUS BIT 15	D15	19	22	RD	READ
CLOCK INPUT	CLKIN	20	21	CS	CHIP SELECT

CS5016



NOTE: All pin references in this data sheet refer to the 40-pin DIP package numbering. Use this figure to determine pin numbers for 44-pin package.

PIN DESCRIPTIONS

Power Supply Connections

VD+ – Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- – Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND – Digital Ground, PIN 10.
Digital ground.

VA+ – Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- – Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND – Analog Ground, PIN 27.
Analog ground.

Oscillator

CLKIN – Clock Input, PIN 20.
All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ – Hold, PIN 1.
A falling transition on this pin sets the CS5016 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50 ns.

$\overline{\text{CS}}$ – Chip Select, PIN 21.
When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ – Read, PIN 22.
When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 – Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{UP}$ – Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format. Once calibration has been performed, either bipolar or unipolar may be selected without the need to recalibrate.

RST – Reset, PIN 32.

When taken high for at least 100 ns, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

3

BW – Bus Width Select, PIN 33.

When hard-wired high, all 16 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D0-D7. A second read cycle places the eight LSB's on D0-D7. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D0-D7.

$\overline{INTRLV}$ – Interleave, PIN 34.

When latched low using $\overline{CS}$, the device goes into interleave calibration mode. A full calibration will complete every 72,051 conversions. The effective conversion time extends by 20 clock cycles.

CAL – Calibrate, PIN 35. (See Addendum appending this data sheet))

When latched high using $\overline{CS}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 1,441,020 master clock cycles. If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN – Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200 Ω.

VREF – Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 – Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{CS}$ and $\overline{RD}$, they offer the converter's 16-bit output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register.

$\overline{EOT}$ – End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal (3.75 µs for 4 MHz external clock).

$\overline{EOC}$ – End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA – Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK – Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5016. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF – Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST – Test, PIN 31.

Allows access to the CS5016's test functions which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Ordering Guide

Model	Linearity	Signal to Noise Ratio	Conversion Time	Temp. Range	Package
CS5016-JP32	.0030%	87 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-JP16	.0030%	87 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-KP32	.0015%	90 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-KP16	.0015%	90 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-JL32	.0030%	87 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
CS5016-JL16	.0030%	87 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
CS5016-KL32	.0015%	90 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
CS5016-KL16	.0015%	90 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
CS5016-AD32	.0030%	87 dB	32.50 µs	-40 to +85 °C	40-Pin CerDIP
CS5016-AD16	.0030%	87 dB	16.25 µs	-40 to +85 °C	40-Pin CerDIP
CS5016-BD32	.0015%	90 dB	32.50 µs	-40 to +85 °C	40-Pin CerDIP
CS5016-BD16	.0015%	90 dB	16.25 µs	-40 to +85 °C	40-Pin CerDIP
CS5016-AL32	.0030%	87 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
CS5016-AL16	.0030%	87 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
CS5016-BL32	.0015%	90 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
CS5016-BL16	.0015%	90 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
CS5016-SD16	.0076%	87 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
CS5016-TD16	.0015%	90 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
CS5016-SE16	.0076%	87 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
CS5016-TE16	.0015%	90 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC

ADDENDUM

Burst Calibration

Burst calibration mode allows control of partial calibration cycles. Due to an unforeseen condition inside the part, asynchronous termination of calibration (CAL brought low) may result in a sub-optimal calibration result. It is recommended that burst calibration is not used, until the silicon is revised to prevent this effect.

Interleave calibration works perfectly, provided it is not used intermittently.

The reset calibration always works perfectly, and typically should be used instead of burst mode. The CS5016's very low drift over temperature means that, under most circumstances, calibration need only be performed at power-up, using reset.

If you wish to use burst calibration, then please contact the factory for advice and new part availability information.

Semiconductor Corporation

CS5101

16-Bit, 100 kHz Serial-Output A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 92 dB; THD: 0.001%
- Linearity Error: ± 0.001% FS
- 8.1 µs Conversion Time with Guaranteed 16-bit No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption: 320 mW
  - Power-down Mode: 1 mW
- Evaluation Board Available

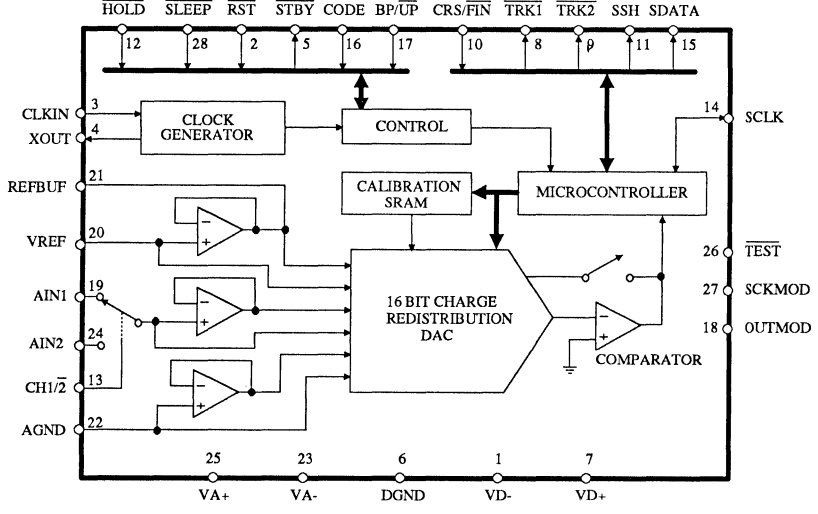
General Description

The CS5101 is a 16-bit monolithic CMOS analog-to-digital converter capable of 100 kHz throughput. On-chip self-calibration circuitry achieves nonlinearity of ±0.001% of FS and guarantees 16-bit no missing codes. Superior linearity also leads to 92 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are similarly kept within 2 LSB, eliminating the need for manual calibration of any kind.

The CS5101 consists of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, crystal oscillator, comparator, and serial communications port. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input after each conversion within 1.9 µs, allowing throughput rates up to 100 kHz.

The converter's 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION: Page 3-120



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; Full-Scale Input Sinewave, 1 kHz; f_{clk} = 4 MHz for –16, 8 MHz for –8; f_s = 50 kHz for –16, 100 kHz for –8; Bipolar Mode; SSC Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 200 Ω unless otherwise specified)

Parameter *			CS5101 -J,K min	CS5101 -J,K typ	CS5101 -J,K max	CS5101 -A,B min	CS5101 -A,B typ	CS5101 -A,B max	CS5101 -S,T min	CS5101 -S,T typ	CS5101 -S,T max	Units
Specified Temperature Range				0 to +70			-40 to +85			-55 to +125		°C
Accuracy												
Linearity Error	(Note 1)	-J,A,S		0.002	0.003		0.002	0.003		0.002	0.004	% FS
		-K,B,T		0.001	0.002		0.001	0.002		0.001	0.003	% FS
	(Note 3)	Drift		± 1/4			±1/4			± 1/2		ΔLSB
Differential Linearity	(Note 2, 12)		16			16			16			Bits
Full Scale Error	(Note 1)	-J,A,S		± 2	± 4		± 2	± 4		± 2	± 5	LSB
		-K,B,T		± 2	± 4		± 2	± 4		± 2	± 4	LSB
	(Note 3)	Drift		± 1			± 1			± 2		ΔLSB
Unipolar Offset	(Note 1)	-J,A,S		± 1	± 4		± 1	± 4		± 1	± 5	LSB
		-K,B,T		± 1	± 3		± 1	± 3		± 1	± 4	LSB
	(Note 3)	Drift		± 1			± 1			± 2		ΔLSB
Bipolar Offset	(Note 1)	-J,A,S		± 1	± 4		± 1	± 4		± 1	± 5	LSB
		-K,B,T		± 1	± 3		± 1	± 3		± 1	± 3	LSB
	(Note 3)	Drift		± 1			± 2			± 2		ΔLSB
Bipolar Negative Full-Scale Error	(Note 1)	-J,A,S		± 2	± 4		± 2	± 4		± 2	± 5	LSB
		-K,B,T		± 2	± 3		± 2	± 3		± 2	± 4	LSB
	(Note 3)	Drift		± 1			± 2			± 2		ΔLSB
Dynamic Performance			(Bipolar Mode)									
Peak Harmonic or Spurious Noise												
1kHz Input	(Note 1)	-J,A,S	96	100		96	100		94	100		dB
		-K,B,T	98	102		98	102		98	102		dB
12kHz Input		-J,A,S	85	88		85	88		83	88		dB
		-K,B,T	85	91		85	91		85	91		dB
Total Harmonic Distortion												
		-J,A,S		0.002			0.002			0.002		%
		-K,B,T		0.001			0.001			0.001		%
Signal-to-Noise Ratio												
0dB Input	(Note 1)	-J,A,S	87	90		87	90		87	90		dB
		-K,B,T	90	92		90	92		90	92		dB
-60dB Input		-J,A,S		30			30			30		dB
		-K,B,T		32			32			32		dB
Noise (Note 4)	Unipolar Mode			35			35			35		uV_{rms}
	Bipolar Mode			70			70			70		uV_{rms}

Notes: 1. Applies after calibration at any temperature within the specified temperature range.
2. Minimum resolution for which no missing codes is guaranteed over the specified temperature range.
3. Total drift over specified temperature range after calibration at power-up at 25 °C.
4. Wideband noise aliased into the baseband. Referred to the input.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

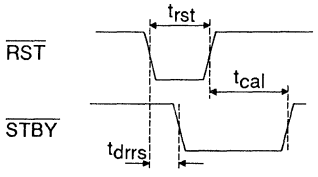
Parameter *	Symbol	CS5101 -J,K min	typ	max	CS5101 -A,B min	typ	max	CS5101 -S,T min	typ	max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125			°C
Analog Input											
Aperture Time	-		25			25			25		ns
Aperture Jitter	-		100			100			100		ps
Input Capacitance (Note 5) Unipolar Mode	-		320	425		320	425		320	425	pF
Bipolar Mode	-		200	265		200	265		200	265	pF
Conversion & Throughput											
Conversion Time −8	t_c			8.12			8.12			8.12	us
(Notes 6) −16	t_c			16.25			16.25			16.25	us
Acquisition Time −8	t_a		–	1.88		–	1.88		–	1.88	us
(Note 7) −16	t_a		2.6	3.75		2.6	3.75		2.6	3.75	us
Throughput −8	f_{tp}	100			100			100			kHz
(Note 8) −16	f_{tp}	50			50			50			kHz
Power Supplies											
Power Supply Current Positive Analog	I_{A+}		21	25		21	25		21	25	mA
$\overline{\text{SLEEP}}$ High) Negative Analog	I_{A-}		−21	−25		−21	−25		−21	−25	mA
(Note 9) Positive Digital	I_{D+}		11	15		11	15		11	15	mA
Negative Digital	I_{D-}		−11	−15		−11	−15		−11	−15	mA
Power Dissipation ($\overline{\text{SLEEP}}$ High)	P_{do}		320	400		320	400		320	400	mW
(Notes 9, 10) ($\overline{\text{SLEEP}}$ Low)	P_{ds}		1			1			1		mW
Power Supply Rejection (Note 11) Positive Supplies	PSR		84			84			84		dB
Negative Supplies	PSR		84			84			84		dB

Notes:
5. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
6. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of $\overline{\text{HOLD}}$ and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.
7. The CS5101 requires 6 clock cycles of coarse charge, followed by a minimum of 1.125 µs of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 1.125 µs with an 8 MHz clock, however; in PDT, RBT, or SSC modes, at clock frequencies less than 8 MHz, fine charge may be less than 9 clock cycles. This reflects the typ. specification (6 clock cycles + 1.125 µs).
8. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described above.
9. All outputs unloaded. All inputs CMOS levels.
10. Power dissipation in the sleep mode applies with no master clock applied (CLKIN held high or low).
11. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 17 shows a plot of typical power supply rejection versus frequency.

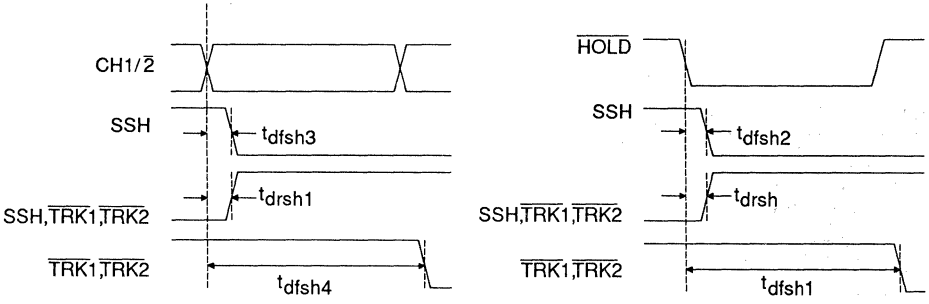
SWITCHING CHARACTERISTICS (T_A=T_{MIN} to T_{MAX}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter			Symbol	Min	Typ	Max	Units
CLKIN Period	(Note 12)	-8 -16	t_{clk}	125 250	–	10,000 10,000	ns ns
CLKIN Low time			t_{clkl}	37.5	–	–	ns
CLKIN High time			t_{clkh}	37.5	–	–	ns
Crystal Frequency	(Note 13)	-8 -16	f_{xtal}	2.0 2.0	– –	8.0 4.0	MHz MHz
$\overline{SLEEP}$ Rising to Oscillator Stable		(Note 14)	–	–	2	–	ms
$\overline{RST}$ Pulse Width			t_{rst}	150	–	–	ns
$\overline{RST}$ to $\overline{STBY}$ Falling			t_{drrs}	–	100	–	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising			t_{cal}	–	11,528,160	–	t_{clk}
CH1/$\overline{2}$ edge to SSH falling		(Note 15)	t_{dfsh3}	–	40	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ rising		(Note 15)	t_{drsh1}	–	80	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ falling		(Note 15)	t_{dfsh4}	–	–	66 t_{clk} + 260	ns
$\overline{HOLD}$ to SSH Falling		(Note 16)	t_{dfsh2}	–	60	–	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, Falling		(Note 16)	t_{dfsh1}	66t_{clk}	–	68t_{clk} + 260	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, SSH Rising		(Note 16)	t_{drsh}	–	120	–	ns
$\overline{HOLD}$ Pulse Width			t_{hold}	130	–	64t_{clk}	ns
$\overline{HOLD}$ to CH1/$\overline{2}$ Edge		(Note 16)	t_{dhlri}	-30	–	64t_{clk}	ns
CLKIN Falling to $\overline{HOLD}$ Falling		(Note 17)	t_{cfh}	–	–	-10	ns
$\overline{HOLD}$ FALLING to CLKIN Falling		(Note 17)	t_{hcf}	55	–	–	ns

Note:
12. Clock speeds of less than 1.0 MHz, at temperatures > 100°C, will degrade DNL performance.
13. External loading capacitors are required to allow the crystal to oscillate.
14. With 8MHz crystal, two 10 pF loading capacitors and a 10 MΩ parallel resistor (see Figure 8).
15. These times are for FRN mode.
16. SSH only works correctly if $\overline{HOLD}$ falling edge is within ±30ns of CH1/$\overline{2}$ edge or if CH1/$\overline{2}$ edge occurs between 30ns before $\overline{HOLD}$ rises to 64 t_{clk} after $\overline{HOLD}$ has fallen. These times are for SSC, PDT and RBT modes.
17. When $\overline{HOLD}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{HOLD}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{HOLD}$ is latched.



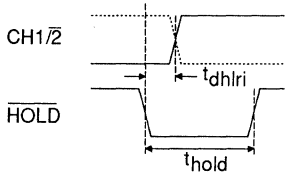
Reset and Calibration Timing



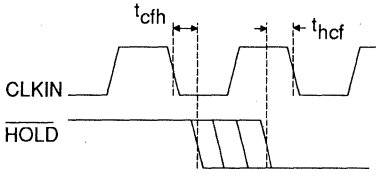
a. FRN mode

b. SSC, PDT, RBT modes

Control Output Timing



Channel Selection Timing



Start Conversion Timing

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Input Pulse Period	t_{sclk}	200	–	–	ns
SCLK Input Pulse Width Low	t_{sclkl}	50	–	–	ns
SCLK Input Pulse Width High	t_{sclkh}	50	–	–	ns
SCLK Input Falling to SDATA Valid	t_{dss}	–	100	150	ns
SCLK Output Pulse Width Low	t_{slkl}	–	$2t_{clk}$	–	t_{clk}
SCLK Output Pulse Width High	t_{slkh}	–	$2t_{clk}$	–	t_{clk}
SDATA valid before rising SCLK	t_{ss}	$2t_{clk}$ - 100	–	–	ns
SDATA valid after rising SCLK	t_{sh}	$2t_{clk}$ - 100	–	–	ns
$\overline{HOLD}$ falling to 1st falling SCLK	t_{hfs}	$6t_{clk}$	–	$8t_{clk}$ + 165	ns
CH1/$\overline{2}$ edge to 1st falling SCLK	t_{chfs}	–	$7t_{clk}$	–	t_{clk}
$\overline{HOLD}$ falling to SDATA Valid PDT mode	t_{dhs}	–	140	230	ns
$\overline{TRK1}$, $\overline{TRK2}$ Falling to SDATA Valid (Note 18)	t_{dts}	–	65	125	ns

Note: 18. Only valid for $\overline{TRK1}$, $\overline{TRK2}$ falling when SCLK is low. If SCLK is high when $\overline{TRK1}$, $\overline{TRK2}$ falls, then SDATA is valid t_{dss} time after the next falling SCLK.

DIGITAL CHARACTERISTICS (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention (Note 19) Power Supply Voltage VA+ and VD+	V_{MR}	2.0	-	-	V
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 20)	V_{OH}	(VD+) - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 21)	I_{in}	-	-	60	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 19. VA- and VD- can be any value from zero to -5V for memory retention. Neither VA- or VD- should be allowed to go positive. AIN1, AIN2 or VREF must not be greater than VA+ or VD+. This parameter is guaranteed by characterization.

20. I_{OUT} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ Iout = -40 µA).

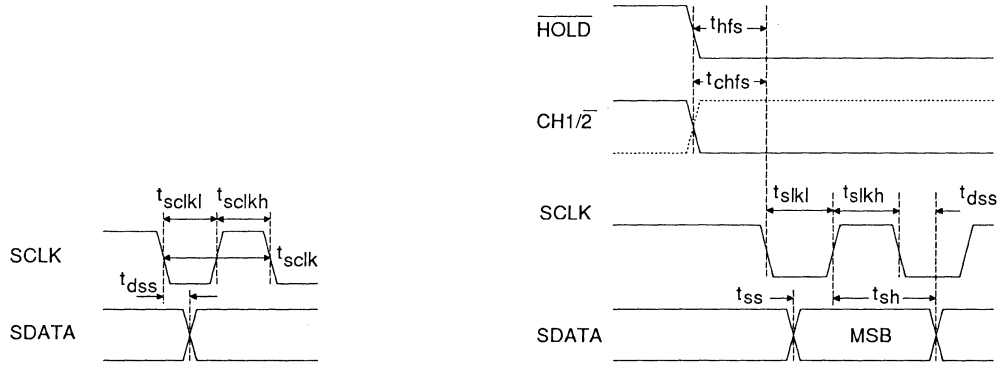
21. All digital inputs except CLKIN and SCLK have internal pull-up devices, nominally 200 kΩ.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 22.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage: (Note 23)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 22. All voltages with respect to ground.

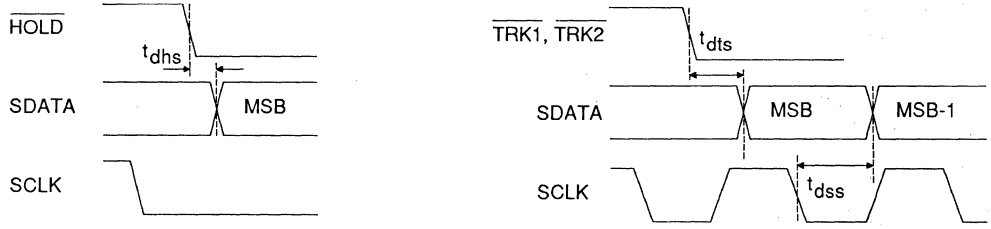
23. The CS5101 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.



a. SCLK input (RBT and PDT mode)

b. SCLK output (SSC and FRN modes)

Serial Data Timing



a. Pipelined Data Transmission (PDT) Mode

b. Register Burst Transmission (RBT) Mode

Data Transmission Timing

ABSOLUTE MAXIMUM RATINGS* (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 24)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	−0.3	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	−55	125	°C
Storage Temperature		T_{stg}	−65	150	°C

Note: 24. Transient currents of up to 100 mA will not cause SCR latch-up.

*WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5101 is a 2-channel, 100 kHz, 16-bit A/D converter. The device includes an inherent sample/hold and an on-chip analog switch for 2-channel operation. Both channels can thus be sampled and converted at rates up to 50 kHz each. Alternatively, the CS5101 can be operated as a single channel, 100 kHz ADC.

The CS5101 can be configured to accept either unipolar or bipolar input ranges, and data is output serially in either binary or 2's complement coding. The device can be configured in 3 different output modes, as well as internal, synchronous loopback for maximum throughput.

The CS5101 provides coarse charge/fine charge control, to allow accurate tracking of high-slew signals. A control output is also supplied for use with an external sample/hold amplifier to implement simultaneous sampling.

THEORY OF OPERATION

The CS5101 implements the successive-approximation algorithm using a charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. As shown in Figure 1, their other terminals are capable of being connected to AGND, VREF, or AIN (1 or 2). When the device is not calibrating or converting, all capacitors are tied to AIN. Switch S1 is closed and the charge on the array, tracks the input signal.

When the conversion command is issued, switch S1 opens. This traps the charge on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, which when connected to the reference will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.

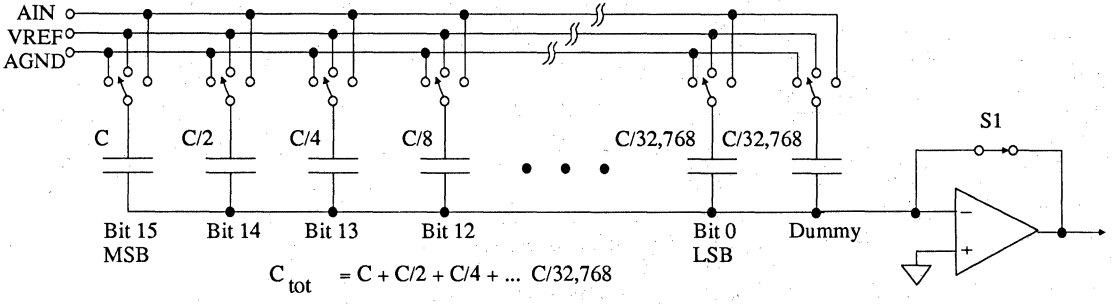


Figure 1. Charge Redistribution DAC

Calibration

The ability of the CS5101 to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. The CS5101 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CS5101 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller precisely adjusts the sub-arrays to yield an effective resolution of 18 bits.

The CS5101 should be reset upon power-up, thus initiating a calibration cycle. The CS5101 then stores its calibration coefficients in on-chip SRAM. When the CS5101 is in power-down mode ($\overline{SLEEP}$ low), it retains the calibration coefficients in memory, and need not be recalibrated when normal operation is resumed.

OPERATION OVERVIEW

The CS5101's monolithic design and inherent sampling architecture make it extremely easy to use.

Initiating Conversions

A falling transition on the $\overline{HOLD}$ pin places the input in the hold mode and initiates a conversion cycle. The charge is trapped on the capacitor array the instant $\overline{HOLD}$ goes low. The CS5101 will complete conversion of the sample within 66 master clock cycles. Upon completion of the conversion cycle, the CS5101 automatically returns to the track mode. After allowing a short time for acquisition (15 clock cycles @ 8 MHz), the CS5101 will be ready for another conversion.

In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{HOLD}$ input. The duty cycle of this clock is not critical. The $\overline{HOLD}$ input is latched internally by the master clock, so it need only remain low for 150 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

As with any high-resolution A-to-D system, it is recommended that sampling is synchronized to the master system clock in order to minimize the effects of clock feedthrough. However, the CS5101 may be operated entirely asynchronous to the master clock if necessary.

Tracking the Input

Upon completing a conversion cycle the CS5101 immediately returns to the track mode. The $CH1/\overline{2}$ pin directly controls the input switch, and therefore directly determines which channel will be tracked. Ideally, the $CH1/\overline{2}$ pin should be switched during the conversion cycle, thereby nullifying the 100 ns switching time, and guaranteeing a stable input at the start of acquisition. If, however, the $CH1/\overline{2}$ control is changed during the acquisition phase, adequate coarse charge and fine charge time must be allowed before initiating conversion.

When the CS5101 enters tracking mode, it uses an input buffer amplifier to provide the bulk of the charge on the capacitor array (coarse-charge), thereby reducing the current load on the external analog circuitry. Coarse-charge is internally initiated for 6 clock cycles at the end of every conversion. The buffer amplifier is then bypassed, and the capacitor array is directly connected to the input. This is referred to as fine-charge, during which the charge on the array

is allowed to accurately settle to the input voltage (see Figure 11).

During coarse-charge, the CS5101 is capable of slewing at 13 V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5101 can slew at 26 V/µs. In fine-charge, it will slew at 1.3 V/µs in the unipolar mode and 2.6 V/µs in bipolar mode. Acquisition of fast slewing signals can be hastened if the voltage change occurs during or immediately following the conversion cycle. For instance, in multiple channel applications (using either the CS5101's internal channel selector or an external MUX), channel selection should occur while the CS5101 is converting. Multiplexor switching and settling time is thereby removed from the overall throughput equation.

If the input signal changes drastically during the acquisition period (such as changing the signal source), the device should be in coarse-charge for an adequate period following the change. The CS5101 can be forced into coarse-charge by bringing CRS/$\overline{\text{FIN}}$ high. The buffer amplifier is engaged when CRS/$\overline{\text{FIN}}$ is high, and may be switched in any number of times during tracking. If CRS/$\overline{\text{FIN}}$ is held low, the CS5101 will only coarse-charge for the first 6 clock cycles following a conversion, and will stay in fine-charge until $\overline{\text{HOLD}}$ goes low. To get an accurate sample, at least 750 ns of coarse-charge, followed by 1.125 µs of fine-charge is required before initiating a conversion (see Figure 2). If course charge is not invoked, then up to 20 µs should be allowed after a step change input for proper acquisition.

Master Clock

The CS5101 can operate either from an externally-supplied master clock, or from it's own crystal oscillator (with a crystal). To enable the CS5101's internal crystal oscillator, simply tie a crystal across the XOUT and CLKIN pins, as shown on the system connection diagram in Figure 8.

Calibration and conversion times directly scale to the master clock frequency. The CS5101-8 can operate with clock or crystal frequencies up to 8 MHz. This allows maximum throughput of up to 50 kHz per channel in dual-channel operation, or 100 kHz in a single channel configuration. The –16 can accept a maximum clock speed of 4 MHz, with corresponding throughput of 50 kHz.

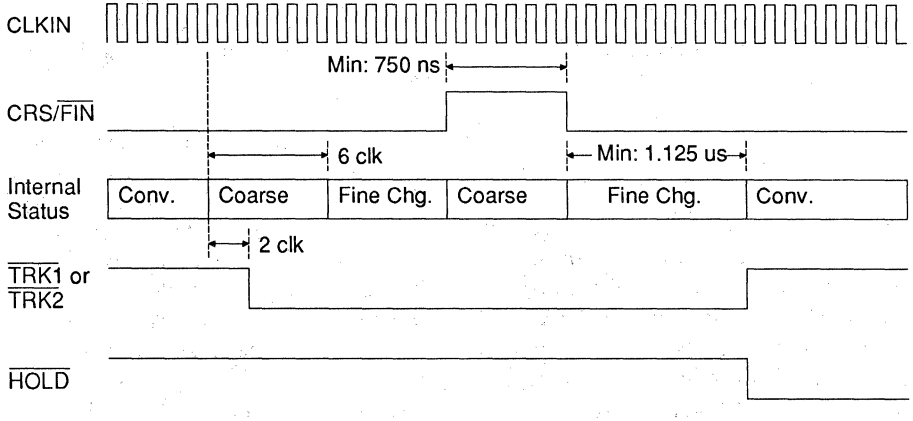


Figure 2. Coarse-Charge/Fine-Charge Control

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF.

The CS5101 can output data in either 2's complement, or binary format. If the CODE pin is high, the output is in 2's complement format with a range of -32,768 to +32,767. If the CODE pin is low, the output is in binary format with a range of 0 to +65,535.

Output Mode Control

The CS5101 can be configured in three different output modes, as well as an internal, synchronous loop-back mode. This allows great flexibility for design into a wide variety of systems. The operating mode is selected by setting the states of the SCKMOD and OUTMOD pins. In all modes, data is output on SDATA, starting with the MSB, and is updated on the falling edge of SCLK.

When SCKMOD is high, SCLK is an input, allowing the data to be clocked out with an external serial clock at rates up to 5 MHz. Tying SCKMOD low reconfigures SCLK as an output, and the CS5101 clocks out each bit as it's determined during the conversion process, at a rate of 1/4 the master clock speed. Table 1 shows an overview of the different states of SCKMOD and OUTMOD, and the corresponding output modes.

Pipelined Data Transmission (PDT)

PDT mode is selected by tying both SCKMOD and OUTMOD high. In PDT mode, the SCLK pin is an input. Data is registered during conversion, and output during the following conversion cycle. $\overline{HOLD}$ must be brought low, initiating another conversion, before data from the previous conversion is available on SDATA. If all the data has not been clocked out before the next falling edge of $\overline{HOLD}$, the old data will be lost.

Registered Burst Transmission (RBT)

RBT mode is selected by tying SCKMOD high, and OUTMOD low. As in PDT mode, SCLK is an input, however data is available immediately following conversion, and may be clocked out the moment $\overline{TRK1}$ or $\overline{TRK2}$ falls. *The falling edge of $\overline{HOLD}$ clears the output buffer*, so any unread data will be lost, although a new conversion may be initiated before all the data has been clocked out (Figure 4).

Synchronous Self-Clocking (SSC)

SSC mode is selected by tying SCKMOD low, and OUTMOD high. In SSC mode, SCLK is an output, and will clock out each bit of the data as it's being converted. SCLK will remain high between conversions, and run at a rate of 1/4 the master clock speed for 16 low pulses during conversion (Figure 5).

MODE	SCKMOD	OUTMOD	SCLK	CH1/$\overline{2}$	$\overline{HOLD}$
PDT	1	1	Input	Input	Input
RBT	1	0	Input	Input	Input
SSC	0	1	Output	Input	Input
FRN	0	0	Output	Output	X

Table 1. Serial Output Modes

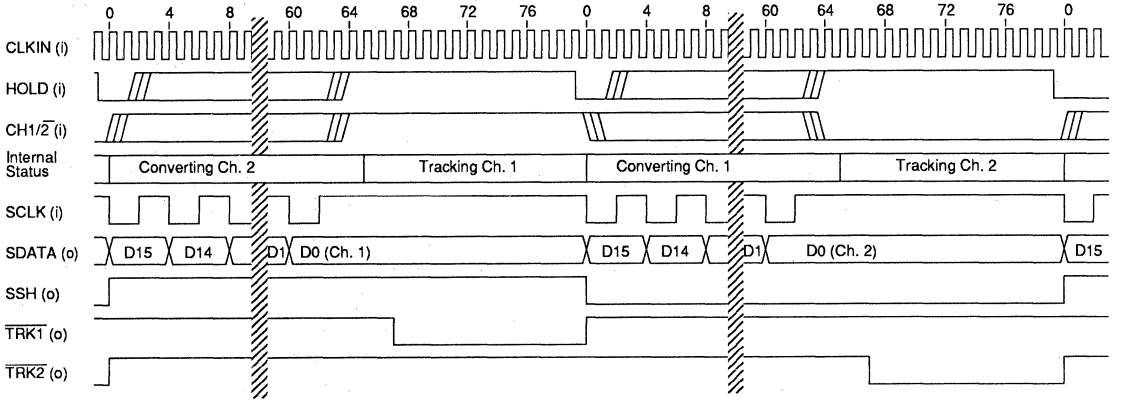


Figure 3. Pipelined Data Transmission Mode (PDT)

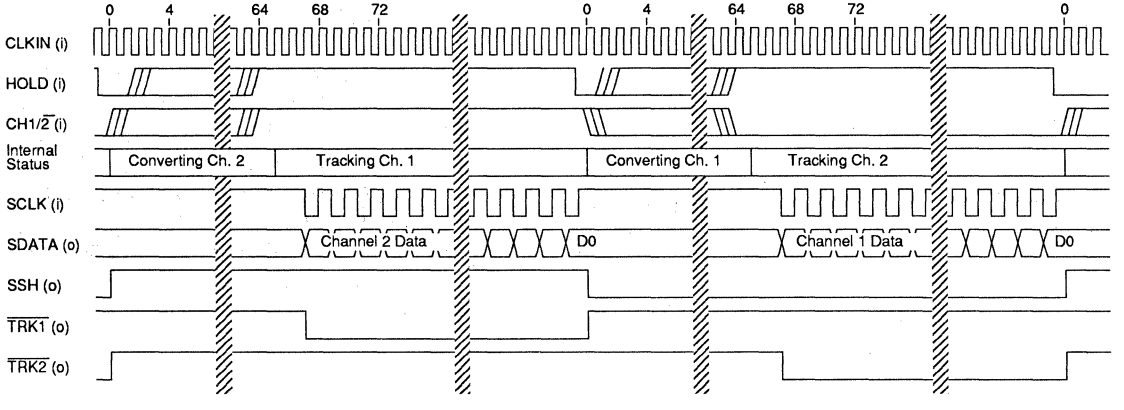


Figure 4. Registered Burst Transmission Mode (RBT)

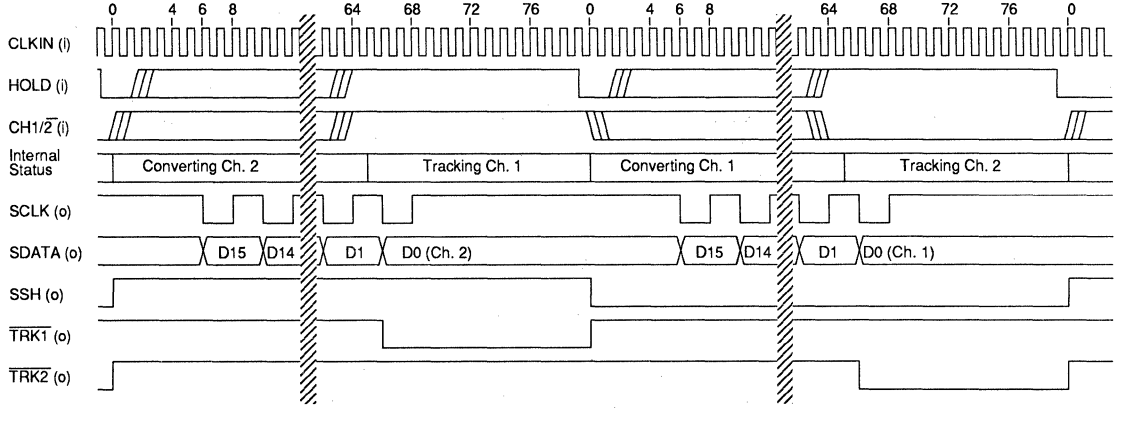


Figure 5. Synchronous Self-Clocking Mode (SSC)

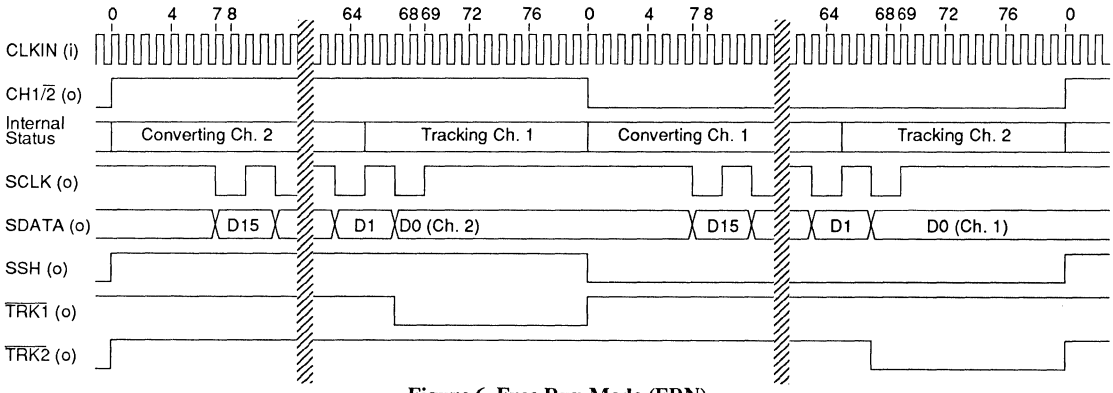


Figure 6. Free Run Mode (FRN)

Free Run (FRN)

Free Run is the internal, synchronous loopback mode. FRN mode is selected by tying SCKMOD and OUTMOD low. SCLK is an output, and operates exactly the same as SSC. In Free Run mode, the CS5101 initiates a new conversion every 80 master clock cycles, and alternates between channel 1 and channel 2. $\overline{HOLD}$ is disabled, and should be tied to either VD+ or DGND. CH1/$\overline{2}$ is an output, and will change at the start of each new conversion cycle, indicating which channel will be tracked after the current conversion is finished (Figure 6).

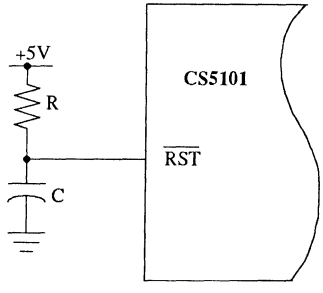


Figure 7. Power-up Reset Circuit

SYSTEM DESIGN WITH THE CS5101

Figure 8 shows a general system connection diagram for the CS5101.

Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

System Initialization

Upon power up, the CS5101 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5101's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before $\overline{RST}$ rises to guarantee an accurate calibration. Later, the CS5101 may be reset at any time to initiate a single full calibration.

When $\overline{RST}$ is brought low all internal logic clears. When it returns high a calibration cycle begins which takes 11,528,160 master clock cycles to complete (approximately 1.4 seconds with an 8 MHz master clock). The CS5101's $\overline{STBY}$ output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation. While calibrating, the CS5101 will ignore changes on the $\overline{HOLD}$ input. The CRS/$\overline{FIN}$ pin must remain low for the entire calibration cycle.

To perform the reset function, a simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 7. The RC time constant must be long enough to guarantee the rest of the system is fully powered up and stable by the end of reset. The resistor should be less than or equal to 10 kΩ.

Simultaneous Sampling

The CS5101 offers three digital output signals, SSH, $\overline{TRK1}$, and $\overline{TRK2}$ which can be used to

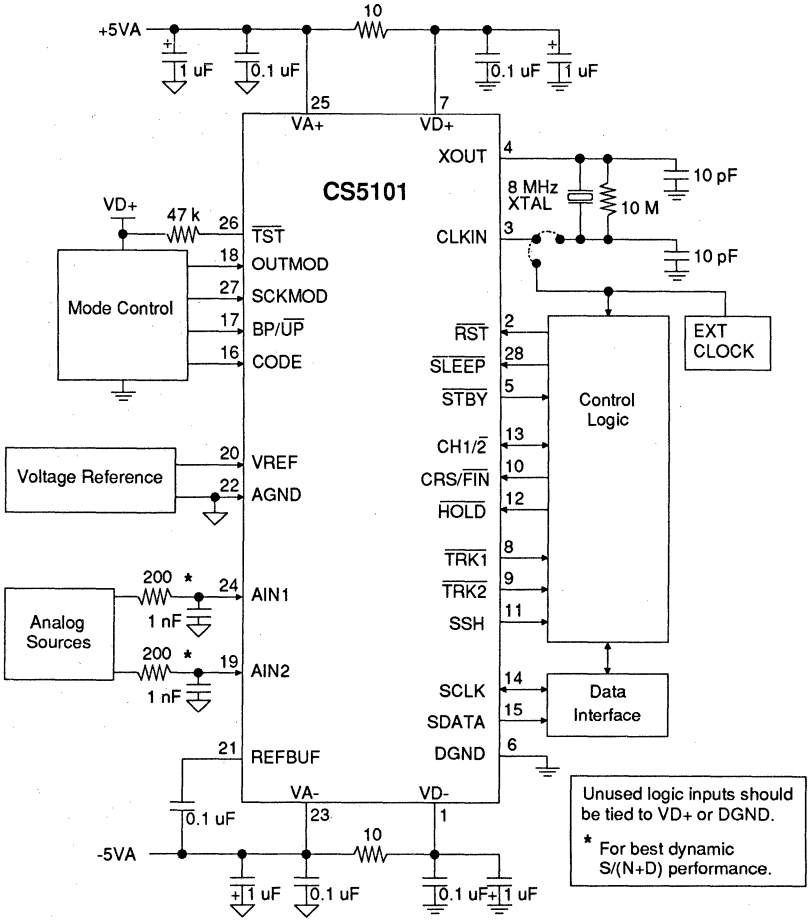


Figure 8. CS5101 System Connection Diagram

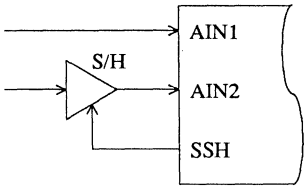


Figure 9. Simultaneous Sampling

control an external sample/hold amplifier to achieve simultaneous sampling of both channels.

Figures 3-6 show the timing relationships for SSH, $\overline{TRK1}$, and $\overline{TRK2}$. In the standard two-channel configuration, such as free run, the CS5101 samples the left and right channels 180° out of phase. Simultaneous sampling between channels 1 and 2 can be achieved as shown in Figure 9 using the CS5101's SSH output. The external sample/hold will freeze the analog signal on channel 2 as the CS5101 freezes the channel 1 input at AIN1. The external sample/hold will hold that signal valid at AIN2 until the CS5101 begins conversion of channel 2. Once that conversion begins, the sample/hold returns to the sample mode. The external sample/hold will have from the $\overline{HOLD}$ on channel 2 until the $\overline{HOLD}$ on channel 1 (80 clock cycles) to acquire the signal. This allows at least 10 µs for acquisition, followed by the same period to hold the signal.

Single-Channel Operation

The CS5101 can alternatively be used to sample one channel by tying the CH1/$\overline{2}$ input high or low. The unused AIN pin should be tied to the analog input signal or to AGND. (If operating in free run mode, AIN1 and AIN2 must be tied to the same source, as CH1/$\overline{2}$ is reconfigured as an output.)

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5101 internally buffers all analog inputs (AIN1, AIN2, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X Series of A/D Converters*" is available for the CS5101. In addition to working through a reference circuit design example, it offers seven built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5101 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to coarse-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after coarse-charging from the buffer. This creates an ac current load as the CS5101 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output im-

pedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 8 MHz clock the reference must supply a maximum load current of 20 µA peak-to-peak (2 µA typical). An output impedance of 2 Ω will therefore yield a maximum error of 40 µV. With a 4.5 V reference and LSB size of 138 µV this would insure approximately 1/4 LSB accuracy. A 10 µF capacitor exhibits an impedance of less than 2 Ω at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

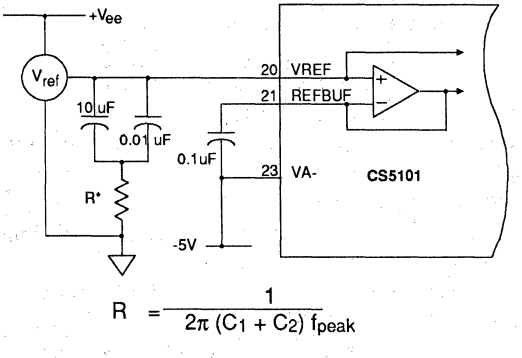


Figure 10. Reference Connections

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors. The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5101 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5101 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for coarse-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During coarse-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage may be offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

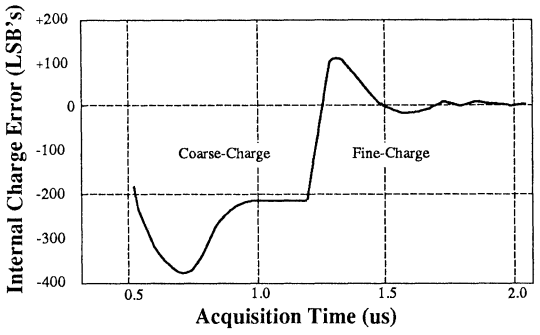


Figure 11. Charge Settling Time (8 MHz Clock)

Fine-charge settling is specified as a maximum of 1.25 µs for an analog source impedance of less than 200 Ω. In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input amplifiers, consult the application note: *Buffer Amplifiers for the CS501X Series of A/D Converters.*

$\overline{\text{SLEEP}}$ Mode Operation

The CS5101 includes a $\overline{\text{SLEEP}}$ pin. When $\overline{\text{SLEEP}}$ is active (low) the CS5101 will dissipate very low power to retain its calibration memory when the device is not sampling. It does not require calibration after $\overline{\text{SLEEP}}$ is made inactive (high). When coming out of $\overline{\text{SLEEP}}$, sampling can begin as soon as the oscillator starts (time will depend on the particular oscillator components) and the REFBUF capacitor is charged (which takes about 3 ms). To achieve minimum start-up time, use an external clock and leave the voltage reference powered-up. Connect a resistor (2 kΩ) between pins 20 and 21 to keep the REFBUF capacitor charged. Conversion can then begin as soon as the A/D has completed a coarse/fine sample period.

To retain calibration memory while $\overline{\text{SLEEP}}$ is active (low) VA+ and VD+ must be maintained at greater than 2.0V. VA- and VD- can be allowed to go to 0 volts. The voltages into VA- and VD- cannot just be "shut-off" as these pins cannot be allowed to float to potentials greater than AGND/DGND. If the supply voltages to VA- and VD- are removed, use a transistor switch to short these to the power supply ground while in $\overline{\text{SLEEP}}$ mode.

Grounding and Power Supply Decoupling

The CS5101 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference.

The digital and analog supplies are isolated within the CS5101 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5101 must never exceed the positive analog supply by more than a diode drop or the CS5101 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram (Figure 8) shows a decoupling scheme which allows the CS5101 to be powered from a single set

of ± 5V rails. The positive digital supply is derived from the analog supply through a 10 Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10 Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5101 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5101. The CDB5101 evaluation board is available for the CS5101, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5101, and can be quickly reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CS5101 PERFORMANCE

Differential Nonlinearity

The self-calibration scheme utilized in the CS5101 features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of ±1/4 LSB, with code widths ranging from 3/4 to 5/4 LSB's.

Traditional laser trimmed ADC's have significant differential nonlinearities. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer function to be missing. Although their affect is minor on S/(N+D) with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80 dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional ADC capable of only 14-bit DNL.

The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is driven too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algorithm. The worst-case codes for dynamic errors

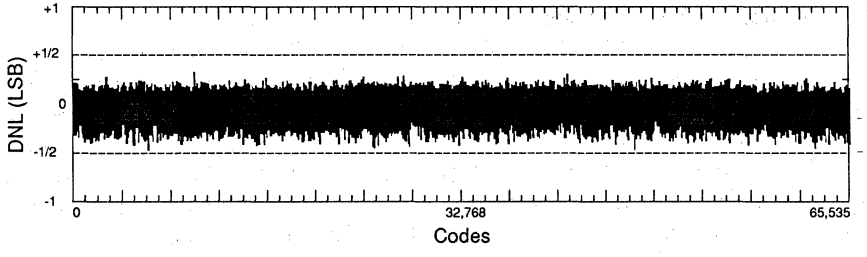


Figure 12. CS5101 DNL Plot

are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with low-level signals, the codes around mid-scale (1/2 FS) are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5101 maintains accurate bit weights. DNL errors are dominated by residual calibration errors of ±1/4 LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on S/(N+D) are buried by white broadband noise. (See Figure 14)

A histogram plot of typical DNL of the CS5101 can be seen in Figure 12. A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

FFT Tests and Windowing

In the factory, the CS5101 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5101, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5101.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

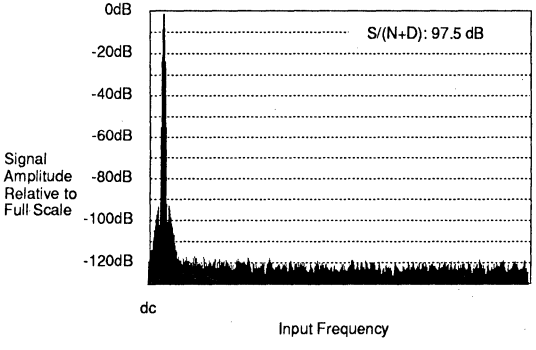


Figure 13. FFT Plot of Ideal 16-bit A/D Converter

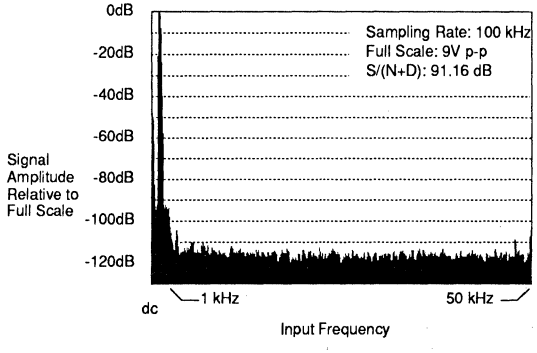


Figure 14. CS5101 FFT (FRN Mode, 1-Channel)

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CS5101 has a maximum side-lobe level of -92 dB. Figure 13 shows an FFT computed from an ideal 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. Averaging the FFT results from ten time records filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semicondutctor.

As illustrated in Figure 14, the CS5101 typically provides 92 dB S/(N+D) and 0.001% THD. Unlike conventional successive-approximation ADC's, the CS5101's signal-to-noise and dynamic range are not limited by differential non-linearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the baseband. This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

Sampling Distortion

Like most discrete sample/hold amplifier designs, the CS5101's inherent sample/hold exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

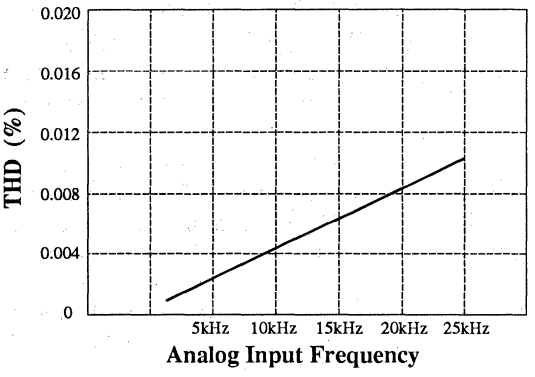


Figure 15. THD vs. Input Frequency with Full Scale Input (±4.5V)

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 14).

The ideal relationship between the charge on the array and the input voltage can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate as shown in Figure 15 since the magnitude of the steady state current increases. First noticeable at 1 kHz, this distortion assumes a linear relationship with input frequency. This distortion is negligible at signal levels below -20 dB of full-scale.

Noise

An A/D converter's noise can be described like that of any other analog component. However, the converter's output is in digital form so any filtering of its noise must be performed in the digital domain. Digitized samples of analog inputs are often considered individual, static snap-shots in time with no uncertainty or noise. In reality, the result of each conversion depends on the analog input level and the instantaneous value of noise sources in the ADC. If sequential samples from the ADC are treated as a "waveform", simple filtering can be implemented in software to improve noise performance with minimal processing overhead.

All analog circuitry in the CS5101 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5101 integrates to 35 µV rms in unipolar mode (70 µV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 16 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a CS5101 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the CS5101 has a "bell" shape with all codes other than 80CD due to internal noise.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5101 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 µV rms in unipolar mode.

Noise in the digital domain can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the CS5101's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the CS5101's noise performance can be

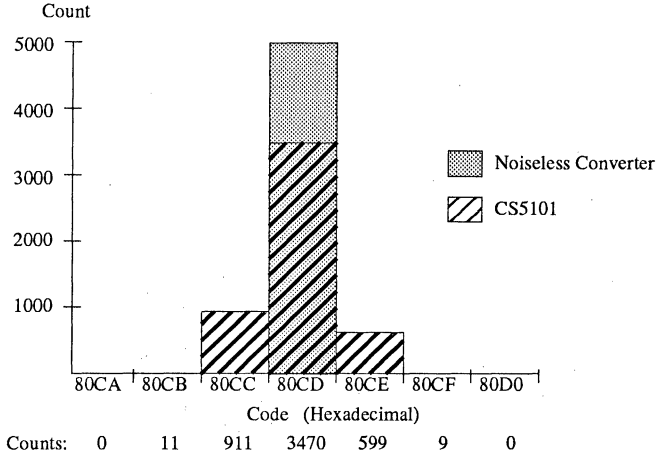


Figure 16. Histogram Plot of 5000 Conversion Inputs

maximized in any application by always sampling at the maximum specified rate of 100 kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependency causes distortion at high frequencies. The CS5101's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter, due to component noise, assumes a random nature. With only 100 ps peak-to-peak aperture jitter, the CS5101 can process full-scale signals up to 1/2 the throughput frequency without significant errors due to aperture jitter.

Power Supply Rejection

The CS5101's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5101's accuracy. This is because the CS5101 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 17 shows power supply rejection of the CS5101 in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

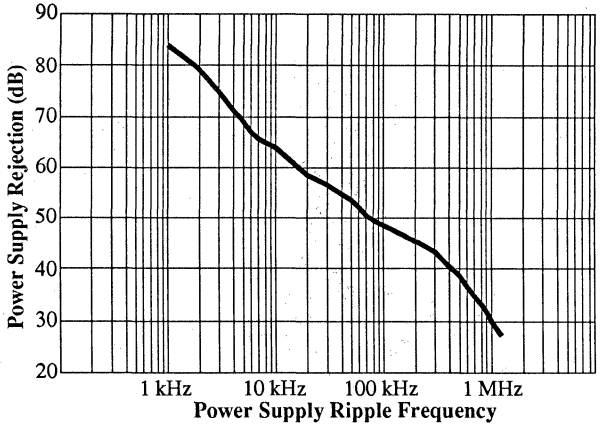
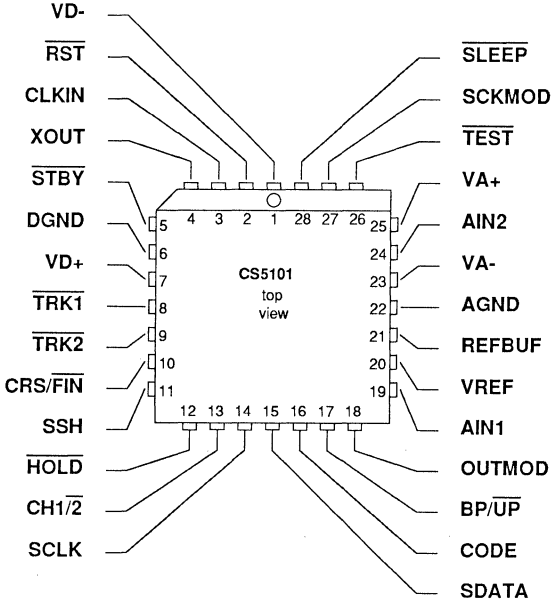


Figure 17. Power Supply Rejection

PIN DESCRIPTIONS

NEGATIVE DIGITAL POWER	VD-	1	28	$\overline{\text{SLEEP}}$	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	$\overline{\text{RST}}$	2	27	SCKMOD	SERIAL CLOCK MODE SELECT
MASTER CLOCK INPUT	CLKIN	3	26	$\overline{\text{TEST}}$	TEST
CRYSTAL OUTPUT	XOUT	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	$\overline{\text{STBY}}$	5	24	AIN2	CHANNEL 2 ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING CHANNEL 1	$\overline{\text{TRK1}}$	8	21	REFBUF	REFERENCE BUFFER
TRACKING CHANNEL 2	$\overline{\text{TRK2}}$	9	20	VREF	VOLTAGE REFERENCE
COARSE/FINE CHARGE CONTROL	CRS/$\overline{\text{FIN}}$	10	19	AIN1	CHANNEL 1 ANALOG INPUT
SIMULTANEOUS SAMPLE/HOLD	SSH	11	18	OUTMOD	OUTPUT MODE SELECT
HOLD & CONVERT	$\overline{\text{HOLD}}$	12	17	BP/$\overline{\text{UP}}$	BIPOLAR/UNIPOLAR SELECT
INPUT CHANNEL SELECT	CH1/$\overline{2}$	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT

CS5101



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 1.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 6.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 23.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 22.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 3.
All conversions and calibrations are timed from a master clock which can be externally supplied by driving CLKIN with a CMOS-compatible clock.

XOUT - Crystal Output, PIN 4.
The master clock can be generated by tying a crystal across the CLKIN and XOUT pins. If an external clock is used, XOUT must be left floating.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 12.
A falling transition on this pin sets the CS5101 to the hold state and initiates a conversion. This input must remain low at least 150 ns. When operating in Free Run Mode, $\overline{\text{HOLD}}$ is disabled, and should be tied to DGND or VD+.

CRS/$\overline{\text{FIN}}$ - Coarse Charge/Fine Charge Control, PIN 10.
When brought high during acquisition time, CRS/$\overline{\text{FIN}}$ forces the CS5101 into coarse charge state. This engages the internal buffer amplifier to track the analog input and charges the capacitor array much faster, thereby allowing the CS5101 to track high slewing signals. In order to get an accurate sample, the last coarse charge period before initiating a conversion (bringing $\overline{\text{HOLD}}$ low) must be longer than 0.75 µs. Similarly, the fine charge period immediately prior to conversion must be at least 1.125 µs. The CRS/$\overline{\text{FIN}}$ pin must be low during conversion time and during calibration time. For normal operation, CRS/$\overline{\text{FIN}}$ should be tied low, in which case the CS5101 will automatically enter coarse charge for 6 clock cycles immediately after the end of conversion.

CH1/$\overline{2}$ - Left/Right Input Channel Select, PIN 13.

Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle. When in Free Run Mode, CH1/2 is an output, and will indicate which channel is being sampled during the current acquisition phase.

$\overline{\text{SLEEP}}$ - Sleep, PIN 28.

When brought low causes the CS5101 to enter a power-down state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode. If using the internal crystal oscillator, 2 ms must be allowed after $\overline{\text{SLEEP}}$ returns high for the crystal oscillator to stabilize. $\overline{\text{SLEEP}}$ should be tied high for normal operation.

CODE - 2's Complement/Binary Coding Select, PIN 16.

Determines whether output data appears in 2's complement or binary format. If high, 2's complement; if low, binary.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Range Select, PIN 17.

When low, the CS5101 accepts a unipolar input range from AGND to VREF. When high, the CS5101 accepts bipolar inputs from -VREF to +VREF.

3

SCKMOD - Serial Clock Mode Select, PIN 27.

When high, the SCLK pin is an input; when low, it is an output. Used in conjunction with OUTMOD to select one of 4 output modes described in Table 1.

OUTMOD - Output Mode Select, PIN 18.

The status of SCKMOD and OUTMOD determine which of four output modes is utilized. The four modes are described in Table 1.

SCLK - Serial Clock, PIN 14.

Serial data changes status on a falling edge of this input, and is valid on a rising edge. When SCKMOD is high SCLK acts as an input. When SCKMOD is low the CS5101 generates its own serial clock at one-fourth the master clock frequency and SCLK is an output.

$\overline{\text{RST}}$ - Reset, PIN 2.

When taken low, all internal digital logic is reset. Upon returning high, a full calibration sequence is initiated which takes 11,528,160 CLKIN cycles to complete. During calibration, the $\overline{\text{HOLD}}$ input will be ignored. The CRS/FIN pin must be low when $\overline{\text{RST}}$ rises and remain low during the calibration time. The CS5101 must be reset at power-up for calibration, however; calibration is maintained during $\overline{\text{SLEEP}}$ mode, and need not be repeated when resuming normal operation.

Analog Inputs

AIN1, AIN2 - Channel 1 and 2 Analog Inputs, PINS 19 and 24.

Analog input connections for the left and right input channels.

VREF - Voltage Reference, PIN 20.

The analog reference voltage which sets the analog input range. In unipolar mode VREF sets full-scale; in bipolar mode its magnitude sets both positive and negative full-scale.

Digital Outputs

$\overline{\text{STBY}}$ - Standby (Calibrating), PIN 5.

Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

SDATA - Serial Output, PIN 15.

Presents each output data bit on a falling edge of SCLK. Data is valid to be latched on the rising edge of SCLK.

SSH - Simultaneous Sample/Hold, PIN 11.

Used to control an external sample/hold amplifier to achieve simultaneous sampling between channels.

$\overline{\text{TRK1}}$, $\overline{\text{TRK2}}$ - Tracking Channel 1, Tracking Channel 2, PINS 8 and 9.

Falls low at the end of a conversion cycle, indicating the acquisition phase for the corresponding channel. The $\overline{\text{TRK1}}$ or $\overline{\text{TRK2}}$ pin will return high at the beginning of conversion for that channel.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 21.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

$\overline{\text{TEST}}$ - Test, PIN 26.

Allows access to the CS5101's test functions which are reserved for factory use. Must be tied to VD+.

Ordering Guide

Model	Conversion Time	Throughput	Linearity	Temperature	Package
CS5101-JP8	8.13 µs	100 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5101-KP8	8.13 µs	100 kHz	0.002%	0 to 70 °C	28-Pin Plastic DIP
CS5101-JP16	16.25 µs	50 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5101-KP16	16.25 µs	50 kHz	0.002%	0 to 70 °C	28-Pin Plastic DIP
CS5101-JL8	8.13 µs	100 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5101-KL8	8.13 µs	100 kHz	0.002%	0 to 70 °C	28-Pin PLCC
CS5101-JL16	16.25 µs	50 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5101-KL16	16.25 µs	50 kHz	0.002%	0 to 70 °C	28-Pin PLCC
CS5101-AD8	8.13 µs	100 kHz	0.003%	-40 to 85 °C	28-Pin CerDIP
CS5101-BD8	8.13 µs	100 kHz	0.002%	-40 to 85 °C	28-Pin CerDIP
CS5101-AD16	16.25 µs	50 kHz	0.003%	-40 to 85 °C	28-Pin CerDIP
CS5101-BD16	16.25 µs	50 kHz	0.002%	-40 to 85 °C	28-Pin CerDIP
CS5101-AL8	8.13 µs	100 kHz	0.003%	-40 to 85 °C	28-Pin PLCC
CS5101-BL8	8.13 µs	100 kHz	0.002%	-40 to 85 °C	28-Pin PLCC
CS5101-AL16	16.25 µs	50 kHz	0.003%	-40 to 85 °C	28-Pin PLCC
CS5101-BL16	16.25 µs	50 kHz	0.002%	-40 to 85 °C	28-Pin PLCC
CS5101-SD8	8.13 µs	100 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
CS5101-TD8	8.13 µs	100 kHz	0.003%	-55 to 125 °C	28-Pin CerDIP
CS5101-SD16	16.25 µs	50 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
CS5101-TD16	16.25 µs	50 kHz	0.003%	-55 to 125 °C	28-Pin CerDIP

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Signal to Peak Harmonic or Noise

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-(Noise + Distortion)

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

•Notes•

Semiconductor Corporation

CS5102

16-Bit, 20 kHz Serial-Output A/D Converter

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 91 dB; THD: 0.001%
- 40 µs Conversion Time
  - Linearity Error: ± 0.001% FS
  - Guaranteed No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption: 44 mW
  - Power-down Mode: 1 mW
- Evaluation Board Available
- Pin compatible with CS5101, 100 kHz 16-bit ADC

General Description

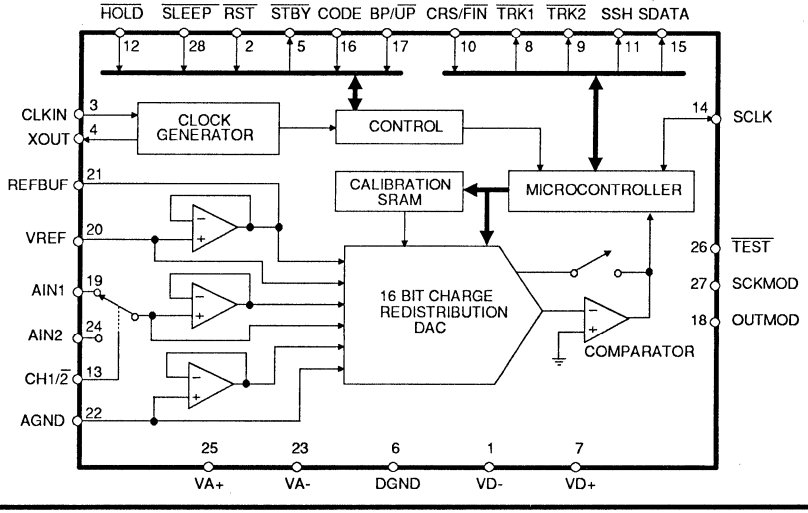
The CS5102 is a 16-bit monolithic CMOS analog-to-digital converter capable of 20 kHz throughput. The CS5102's low power consumption of 44 mW, coupled with a power down mode, makes it particularly suitable for battery powered operation.

On-chip self-calibration circuitry achieves nonlinearity of ±0.0015% of FS and guarantees 16-bit no missing codes up to 20 kHz throughput. Superior linearity also leads to 91 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are similarly kept within 2 LSB, eliminating the need for manual calibration of any kind.

The CS5102 consists of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input after each conversion, allowing throughput rates up to 20 kHz.

The converter's 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION: Page 3-148



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445-7222 Fax: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; Full-Scale Input Sinewave, 200 Hz; CLKIN = 1.6 MHz; f_s = 20 kHz; Bipolar Mode; SSC Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 200 Ω with 1000pF to AGND unless otherwise specified)

Parameter *			CS5102 -J,K min	CS5102 -J,K typ	CS5102 -J,K max	CS5102 -A,B min	CS5102 -A,B typ	CS5102 -A,B max	CS5102 -S,T min	CS5102 -S,T typ	CS5102 -S,T max	Units
Specified Temperature Range				0 to +70			-40 to +85			-55 to +125		°C
Accuracy												
Linearity Error	(Note 1)	-J,A,S		0.002	0.003		0.002	0.003		0.002	0.004	% FS
		-K,B,T		0.001	0.002		0.001	0.002		0.001	0.003	% FS
	(Note 3)	Drift		± 1/4			± 1/4			± 1/2		ΔLSB
Differential Linearity		-J,A,S	16	16		16	16		15	16		Bits
	(Note 2, 12)	-K,B,T	16			16			16			
Full Scale Error	(Note 1)	-J,A,S		± 2	± 4		± 2	± 4		± 2	± 5	LSB
		-K,B,T		± 2	± 4		± 2	± 4		± 2	± 4	LSB
	(Note 3)	Drift		± 1			± 1			± 2		ΔLSB
Unipolar Offset	(Note 1)	-J,A,S		± 1	± 4		± 1	± 4		± 1	± 5	LSB
		-K,B,T		± 1	± 3		± 1	± 3		± 1	± 4	LSB
	(Note 3)	Drift		± 1			± 1			± 2		ΔLSB
Bipolar Offset	(Note 1)	-J,A,S		± 1	± 4		± 1	± 4		± 1	± 5	LSB
		-K,B,T		± 1	± 3		± 1	± 3		± 1	± 3	LSB
	(Note 3)	Drift		± 1			± 2			± 2		ΔLSB
Bipolar Negative Full-Scale Error	(Note 1)	-J,A,S		± 2	± 4		± 2	± 4		± 2	± 5	LSB
		-K,B,T		± 2	± 3		± 2	± 3		± 2	± 4	LSB
	(Note 3)	Drift		± 1			± 2			± 2		ΔLSB
Dynamic Performance		(Bipolar Mode)										
Peak Harmonic or Spurious Noise	(Note 1)	-J,A,S	96	100		96	100		94	100		dB
		-K,B,T	98	102		98	102		98	102		dB
Total Harmonic Distortion		-J,A,S		0.002			0.002			0.002		%
		-K,B,T		0.001			0.001			0.001		%
Signal-to-Noise Ratio												
0dB Input	(Note 1)	-J,A,S	87	90		87	90		87	90		dB
		-K,B,T	90	92		90	92		90	92		dB
-60dB Input		-J,A,S		30			30			30		dB
		-K,B,T		32			32			32		dB
Noise		Unipolar Mode		35			35			35		uV_{rms}
(Note 4)		Bipolar Mode		70			70			70		uV_{rms}

Notes: 1. Applies after calibration at any temperature within the specified temperature range.
2. Minimum resolution for which no missing codes is guaranteed over the specified temperature range.
3. Total drift over specified temperature range after calibration at power-up at 25 °C.
4. Wideband noise aliased into the baseband. Referred to the input.

*Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter *	Symbol	CS5102 -J,K min typ max	CS5102 -A,B min typ max	CS5102 -S,T min typ max	Units
Specified Temperature Range		0 to +70	-40 to +85	-55 to +125	°C
Analog Input					
Aperture Time	-	30	30	30	ns
Aperture Jitter	-	100	100	100	ps
Input Capacitance (Note 5) Unipolar Mode	-	320 425	320 425	320 425	pF
Bipolar Mode	-	200 265	200 265	200 265	pF
Conversion & Throughput					
Conversion Time (Note 6)	t_c	40.625	40.625	40.625	us
Acquisition Time (Note 7)	t_a	9.375	9.375	9.375	us
Throughput (Note 8)	f_{tp}	20	20	20	kHz
Power Supplies					
Power Supply Current Positive Analog	I_{A+}	2.4 3.5	2.4 3.5	2.4 3.5	mA
Negative Analog	I_{A-}	- 2.4 - 3.5	- 2.4 - 3.5	- 2.4 - 3.5	mA
($\overline{SLEEP}$ High) Positive Digital	I_{D+}	2.5 3.5	2.5 3.5	2.5 3.5	mA
(Note 9) Negative Digital	I_{D-}	- 1.5 - 2.5	- 1.5 - 2.5	- 1.5 - 2.5	mA
Power Dissipation ($\overline{SLEEP}$ High)	P_{do}	44 65	44 65	44 65	mW
(Notes 9, 10) ($\overline{SLEEP}$ Low)	P_{ds}	1	1	1	mW
Power Supply Rejection (Note 11) Positive Supplies	PSR	84	84	84	dB
Negative Supplies		84	84	84	dB

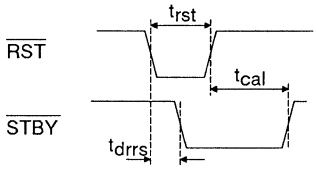
Notes:
5. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
6. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of $\overline{HOLD}$ and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.
7. The CS5102 requires 6 clock cycles of coarse charge, followed by a minimum of 5.625 µs of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 5.625 µs with an 1.6 MHz clock, however; in PDT, RBT, or SSC modes, at clock frequencies less than 1.6 MHz, fine charge may be less than 9 clock cycles.
8. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described in Note 6 and Note 7.
9. All outputs unloaded. All inputs CMOS levels. See table below for power dissipation vs. clock frequency.
10. Power dissipation in the sleep mode applies with no master clock applied (CLKIN held high or low).
11. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 17 shows a plot of typical power supply rejection versus frequency.

Typ. Power (mW)	CLKIN (MHz)
34	0.8
37	1.0
39	1.2
41	1.4
44	1.6

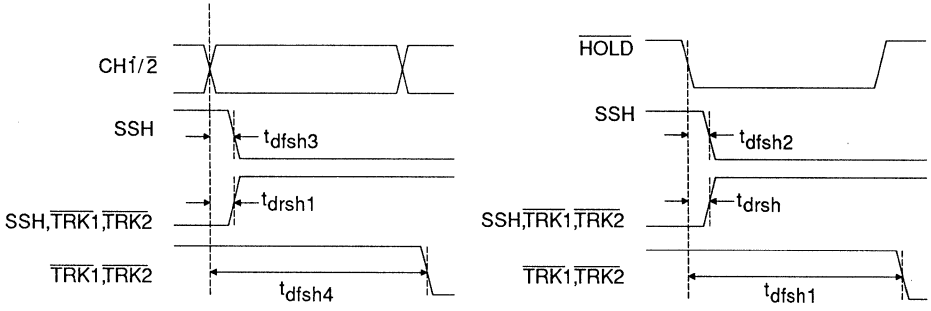
SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Period	(Note 12)	t_{clk}	0.625	–	10	us
CLKIN Low time		t_{clkl}	375	–	–	ns
CLKIN High time		t_{clkh}	375	–	–	ns
Crystal Frequency	(Note 13)	f_{xtal}	TBD	–	1.6	MHz
$\overline{SLEEP}$ Rising to Oscillator Stable	(Note 14)	–	–	20	–	ms
$\overline{RST}$ Pulse Width		t_{rst}	240	–	–	ns
$\overline{RST}$ to $\overline{STBY}$ Falling		t_{drrs}	–	100	–	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising		t_{cal}	–	2,882,040	–	t_{clk}
CH1/$\overline{2}$ edge to SSH falling	(Note 15)	t_{dfsh3}	–	40	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ rising	(Note 15)	t_{drsh1}	–	80	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ falling	(Note 15)	t_{dfsh4}	–	–	$66\,t_{clk}$ + 260	ns
$\overline{HOLD}$ to SSH Falling	(Note 16)	t_{dfsh2}	–	60	–	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, Falling	(Note 16)	t_{dfsh1}	$66t_{clk}$	–	$68t_{clk}$ + 260	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, SSH Rising	(Note 16)	t_{drsh}	–	120	–	ns
$\overline{HOLD}$ Pulse Width		t_{hold}	130	–	$64t_{clk}$	ns
$\overline{HOLD}$ to CH1/$\overline{2}$ Edge	(Note 16)	t_{dhlri}	-30	–	$64t_{clk}$	ns
CLKIN Falling to $\overline{HOLD}$ Falling	(Note 17)	t_{cfh}	–	–	-10	ns
$\overline{HOLD}$ FALLING to CLKIN Falling	(Note 17)	t_{hcf}	55	–	–	ns

Note:
12. Clock speeds of less than 1.6 MHz, at temperatures >100°C, will degrade DNL performance.
13. External loading capacitors are required to allow the crystal to oscillate.
14. With a 1.6 MHz crystal, two 47 pF loading capacitors and a 10 MΩ parallel resistor (see Figure 8).
15. These times are for FRN mode.
16. SSH only works correctly if $\overline{HOLD}$ falling edge is within ±30ns of CH1/$\overline{2}$ edge or if CH1/$\overline{2}$ edge occurs between 30ns before $\overline{HOLD}$ rises to 64 t_{clk} after $\overline{HOLD}$ has fallen. These times are for SSC, PDT and RBT modes.
17. When $\overline{HOLD}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{HOLD}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{HOLD}$ is latched.



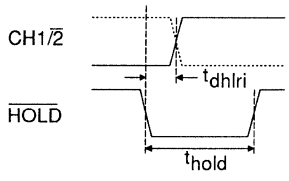
Reset and Calibration Timing



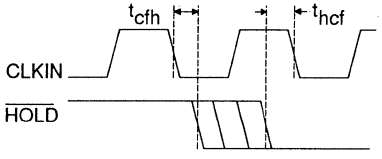
a. FRN Mode

b. SSC, PDT, RBT Mode

Control Output Timing



Channel Selection Timing



Start Conversion Timing

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Input Pulse Period	t_{sclk}	200	–	–	ns
SCLK Input Pulse Width Low	t_{sclkl}	50	–	–	ns
SCLK Input Pulse Width High	t_{sclkh}	50	–	–	ns
SCLK Input Falling to SDATA Valid	t_{dss}	–	100	150	ns
SCLK Output Pulse Width Low	t_{slkl}	–	$2t_{clk}$	–	t_{clk}
SCLK Output Pulse Width High	t_{slkh}	–	$2t_{clk}$	–	t_{clk}
SDATA valid before rising SCLK	t_{ss}	$2t_{clk}$ - 100	–	–	ns
SDATA valid after rising SCLK	t_{sh}	$2t_{clk}$ - 100	–	–	ns
$\overline{HOLD}$ falling to 1st falling SCLK	t_{hfs}	$6t_{clk}$	–	$8t_{clk}$ + 165	ns
CH1/$\overline{2}$ edge to 1st falling SCLK	t_{chfs}	–	$7t_{clk}$	–	t_{clk}
$\overline{HOLD}$ falling to SDATA Valid PDT mode	t_{dhs}	–	140	230	ns
$\overline{TRK1}$, $\overline{TRK2}$ Falling to SDATA Valid (Note 18)	t_{dts}	–	65	125	ns

Note: 18. Only valid for $\overline{TRK1}$, $\overline{TRK2}$ falling when SCLK is low. If SCLK is high when $\overline{TRK1}$, $\overline{TRK2}$ falls, then SDATA is valid t_{dss} time after the next falling SCLK.

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

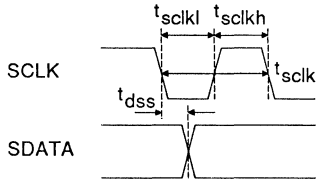
Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention (Note 19) Power Supply Voltage VA+ and VD+	V_{MR}	2.0	-	-	V
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 20)	V_{OH}	(VD+) - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 21)	I_{in}	-	-	60	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 19. VA- and VD- can be any value from zero to -5V for memory retention. Neither VA- or VD- should be allowed to go positive. AIN1, AIN2 or VREF must not be greater than VA+ or VD+. This parameter is guaranteed by characterization.
20. I_{OUT} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ Iout = -40 µA).
21. All digital inputs except CLKIN and SCLK have internal pull-up devices, nominally 200 kΩ.

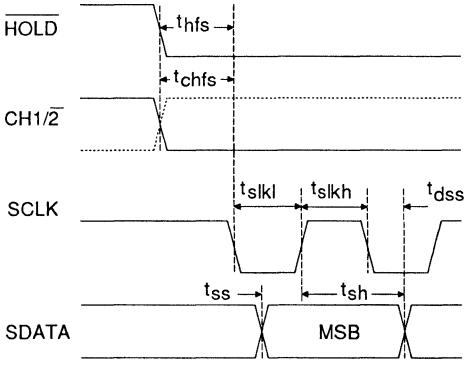
RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 22.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage: (Note 23)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 22. All voltages with respect to ground.
23. The CS5102 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode, with binary coding (CODE = low).

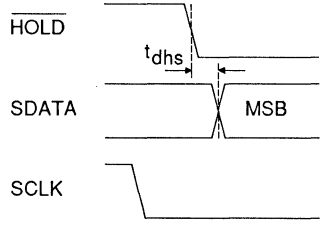


a. SCLK input (RBT and PDT mode)

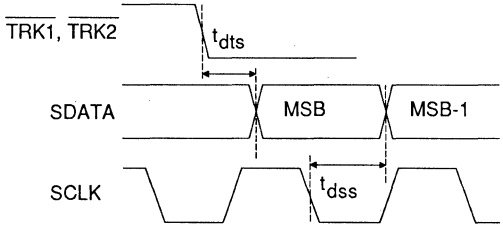


b. SCLK output (SSC and FRN modes)

Serial Data Timing



a. Pipelined Data Transmission (PDT)



b. Register Burst Transmission (RBT) Mode

Data Transmission Timing

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 24)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	−0.3	(VA+) + 0.3	V
Ambient Operating Temperature		T_A	−55	125	°C
Storage Temperature		T_{stg}	−65	150	°C

Note: 24. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5102 is a 2-channel, 20 kHz, 16-bit A/D converter. The device includes an inherent sample/hold and an on-chip analog switch for 2-channel operation. Both channels can thus be sampled and converted at rates up to 10 kHz each. Alternatively, the CS5102 can be operated as a single channel, 20 kHz ADC.

The CS5102 can be configured to accept either unipolar or bipolar input ranges, and data is output serially in either binary or 2's complement coding. The device can be configured in 3 different output modes, as well as internal, synchronous loopback for maximum throughput.

The CS5102 provides coarse charge/fine charge control, to allow accurate tracking of high-slew signals. A control output is also supplied for use with an external sample/hold amplifier to implement simultaneous sampling.

THEORY OF OPERATION

The CS5102 implements the successive-approximation algorithm using a charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. As shown in Figure 1, their other terminals are capable of being connected to AGND, VREF, or AIN (1 or 2). When the device is not calibrating or converting, all capacitors are tied to AIN. Switch S1 is closed and the charge on the array, tracks the input signal.

When the conversion command is issued, switch S1 opens. This traps the charge on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, which when connected to the reference will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.

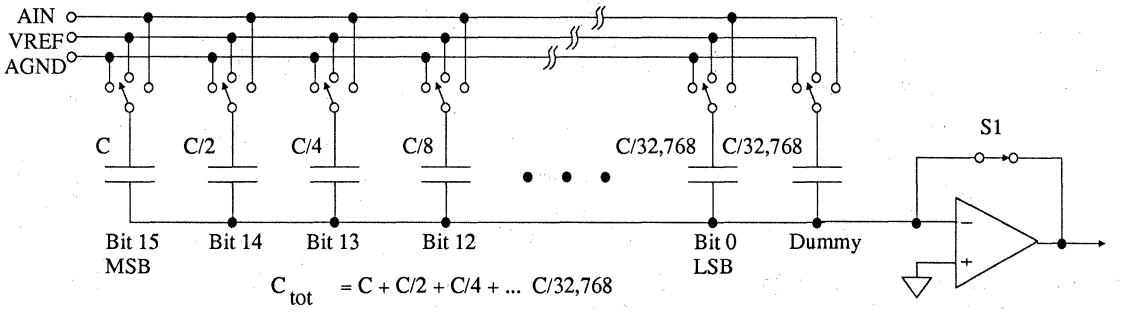


Figure 1. Charge Redistribution DAC

Calibration

The ability of the CS5102 to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. The CS5102 utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CS5102 uses a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller precisely adjusts the sub-arrays to yield an effective resolution of 18 bits.

The CS5102 should be reset upon power-up, thus initiating a calibration cycle. The CS5102 then stores its calibration coefficients in on-chip SRAM. When the CS5102 is in power-down mode ($\overline{SLEEP}$ low), it retains the calibration coefficients in memory, and need not be recalibrated when normal operation is resumed.

OPERATION OVERVIEW

The CS5102's monolithic design and inherent sampling architecture make it extremely easy to use.

Initiating Conversions

A falling transition on the $\overline{HOLD}$ pin places the input in the hold mode and initiates a conversion cycle. The charge is trapped on the capacitor array the instant $\overline{HOLD}$ goes low. The CS5102 will complete conversion of the sample within 65 master clock cycles. Upon completion of the conversion cycle, the CS5102 automatically returns to the track mode. After allowing a short time for acquisition (15 clock cycles @ 1.6MHz), the CS5102 will be ready for another conversion.

In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{HOLD}$ input. The duty cycle of this clock is not critical. The $\overline{HOLD}$ input is latched internally by the master clock, so it need only remain low for 130 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

As with any high-resolution A-to-D system, it is recommended that sampling is synchronized to the master system clock in order to minimize the effects of clock feedthrough. However, the CS5102 may be operated entirely asynchronous to the master clock if necessary.

Tracking the Input

Upon completing a conversion cycle the CS5102 immediately returns to the track mode. The CH1/$\overline{2}$ pin directly controls the input switch, and therefore directly determines which channel will be tracked. Ideally, the CH1/$\overline{2}$ pin should be switched during the conversion cycle, thereby nullifying the input mux switching time, and guaranteeing a stable input at the start of acquisition. If, however, the CH1/$\overline{2}$ control is changed during the acquisition phase, adequate coarse charge and fine charge time must be allowed before initiating conversion.

When the CS5102 enters tracking mode, it uses an input buffer amplifier to provide the bulk of the charge on the capacitor array (coarse-charge), thereby reducing the current load on the external analog circuitry. Coarse-charge is internally initiated for 6 clock cycles at the end of every conversion. The buffer amplifier is then bypassed, and the capacitor array is directly connected to the input. This is referred to as fine-charge, during which the charge on the array

is allowed to accurately settle to the input voltage (see Figure 11).

During coarse-charge, the CS5102 is capable of slewing at 1.5 V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5102 can slew at 3.0 V/µs. In fine-charge, it will slew at 0.1 V/µs in the unipolar mode and 0.2 V/µs in bipolar mode. Acquisition of fast slewing signals can be hastened if the voltage change occurs during or immediately following the conversion cycle. For instance, in multiple channel applications (using either the CS5102's internal channel selector or an external MUX), channel selection should occur while the CS5102 is converting. Multiplexor switching and settling time is thereby removed from the overall throughput equation.

If the input signal changes drastically during the acquisition period (such as changing the signal source), the device should be in coarse-charge for an adequate period following the change. The CS5102 can be forced into coarse-charge by bringing CRS/$\overline{\text{FIN}}$ high. The buffer amplifier is engaged when CRS/$\overline{\text{FIN}}$ is high, and may be switched in any number of times during tracking. If CRS/$\overline{\text{FIN}}$ is held low, the CS5102 will only coarse-charge for the first 6 clock cycles following a conversion, and will stay in fine-charge until $\overline{\text{HOLD}}$ goes low. To get an accurate sample, at least 3.75 µs of coarse-charge, followed by 5.625 µs of fine-charge is required before initiating a conversion (see Figure 2). If coarse charge is not invoked, then up to 200 µs should be allowed after a step change input for proper acquisition. The CRS/$\overline{\text{FIN}}$ pin must be low prior to $\overline{\text{HOLD}}$ becoming active and during conversion.

Master Clock

The CS5102 can operate either from an externally-supplied master clock, or from it's own crystal oscillator (with a crystal). To enable the CS5102's internal crystal oscillator, simply tie a crystal across the XOUT and CLKIN pins and add 2 capacitors and a resistor, as shown on the system connection diagram in Figure 8.

Calibration and conversion times directly scale to the master clock frequency. The CS5102 can operate with clock or crystal frequencies up to 1.6 MHz. This allows maximum throughput of up to 10 kHz per channel in dual-channel operation, or 20 kHz in a single channel configuration.

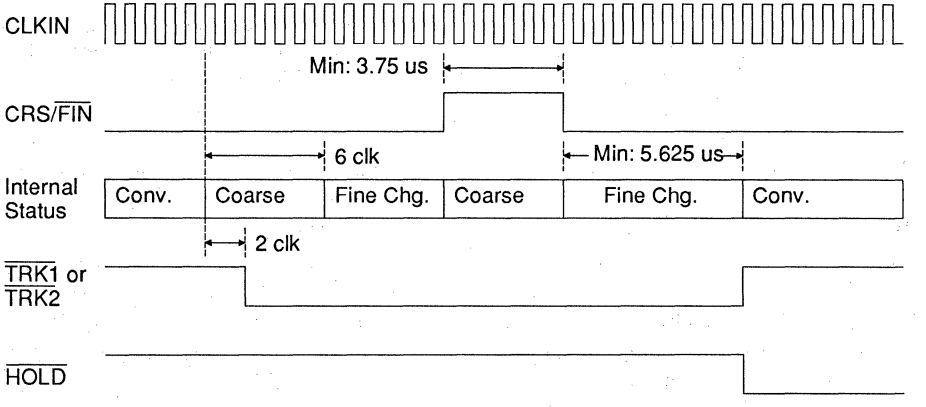


Figure 2. Coarse-Charge/Fine-Charge Control

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF.

The CS5102 can output data in either 2's complement, or binary format. If the CODE pin is high, the output is in 2's complement format with a range of -32,768 to +32,767. If the CODE pin is low, the output is in binary format with a range of 0 to +65,535.

Output Mode Control

The CS5102 can be configured in three different output modes, as well as an internal, synchronous loop-back mode. This allows great flexibility for design into a wide variety of systems. The operating mode is selected by setting the states of the SCKMOD and OUTMOD pins. In all modes, data is output on SDATA, starting with the MSB, and is updated on the falling edge of SCLK.

When SCKMOD is high, SCLK is an input, allowing the data to be clocked out with an external serial clock at rates up to 5 MHz. Additional clock edges after #16 will clock out logic '1's on SDATA. Tying SCKMOD low reconfigures SCLK as an output, and the CS5102 clocks out each bit as it's determined during the conversion process, at a rate of 1/4 the master clock speed.

Table 1 shows an overview of the different states of SCKMOD and OUTMOD, and the corresponding output modes.

Pipelined Data Transmission (PDT)

PDT mode is selected by tying both SCKMOD and OUTMOD high. In PDT mode, the SCLK pin is an input. Data is registered during conversion, and output during the following conversion cycle. $\overline{HOLD}$ must be brought low, initiating another conversion, before data from the previous conversion is available on SDATA. If all the data has not been clocked out before the next falling edge of $\overline{HOLD}$, the old data will be lost.

Registered Burst Transmission (RBT)

RBT mode is selected by tying SCKMOD high, and OUTMOD low. As in PDT mode, SCLK is an input, however data is available immediately following conversion, and may be clocked out the moment $\overline{TRK1}$ or $\overline{TRK2}$ falls. *The falling edge of $\overline{HOLD}$ clears the output buffer*, so any unread data will be lost. A new conversion may be initiated before all the data has been clocked out if the unread data bits are not important (Figure 4).

Synchronous Self-Clocking (SSC)

SSC mode is selected by tying SCKMOD low, and OUTMOD high. In SSC mode, SCLK is an output, and will clock out each bit of the data as it's being converted. SCLK will remain high between conversions, and run at a rate of 1/4 the master clock speed for 16 low pulses during conversion (Figure 5).

MODE	SCKMOD	OUTMOD	SCLK	CH1/$\overline{2}$	$\overline{HOLD}$
PDT	1	1	Input	Input	Input
RBT	1	0	Input	Input	Input
SSC	0	1	Output	Input	Input
FRN	0	0	Output	Output	X

Table 1. Serial Output Modes

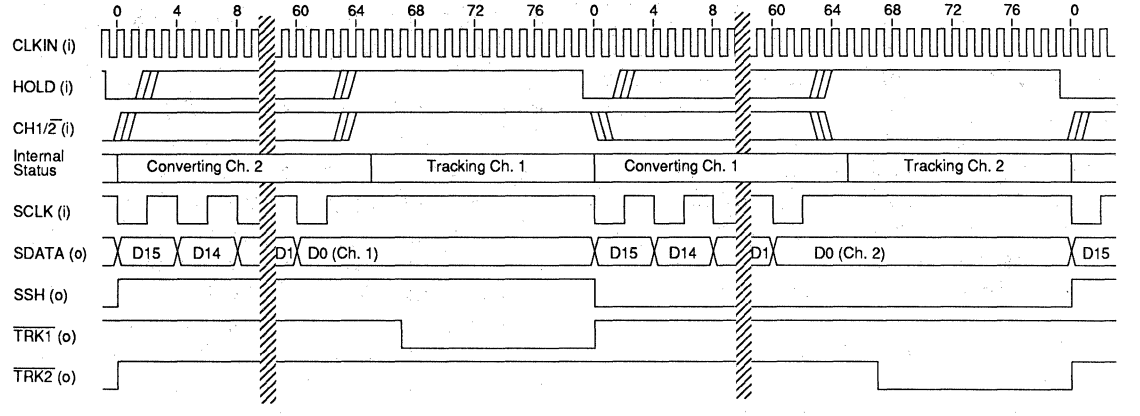


Figure 3. Pipelined Data Transmission Mode (PDT)

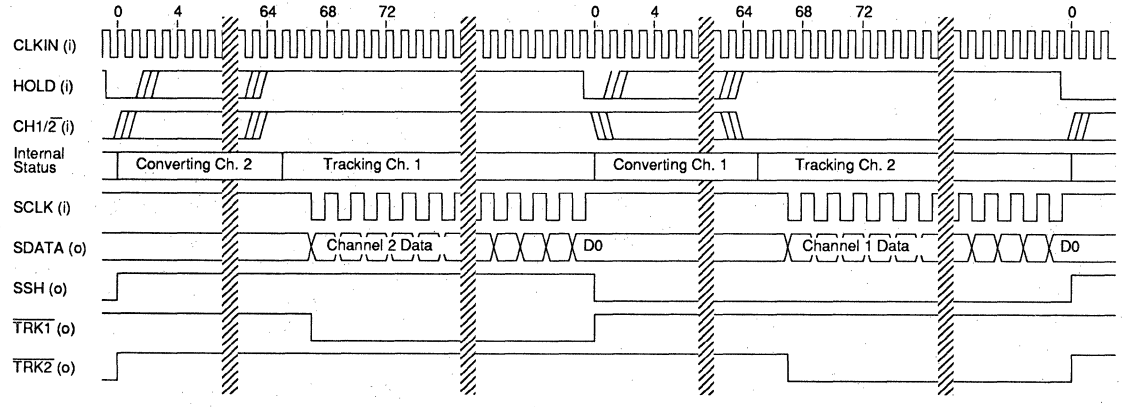


Figure 4. Registered Burst Transmission Mode (RBT)

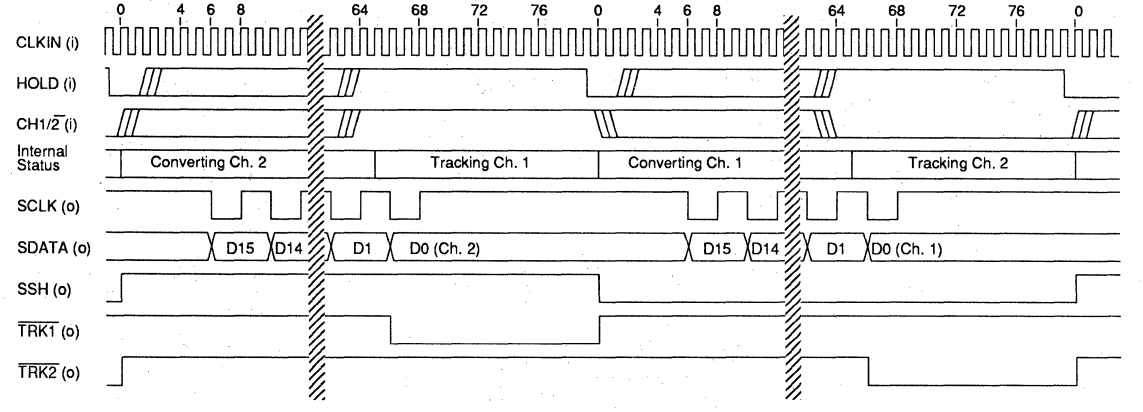


Figure 5. Synchronous Self-Clocking Mode (SSC)

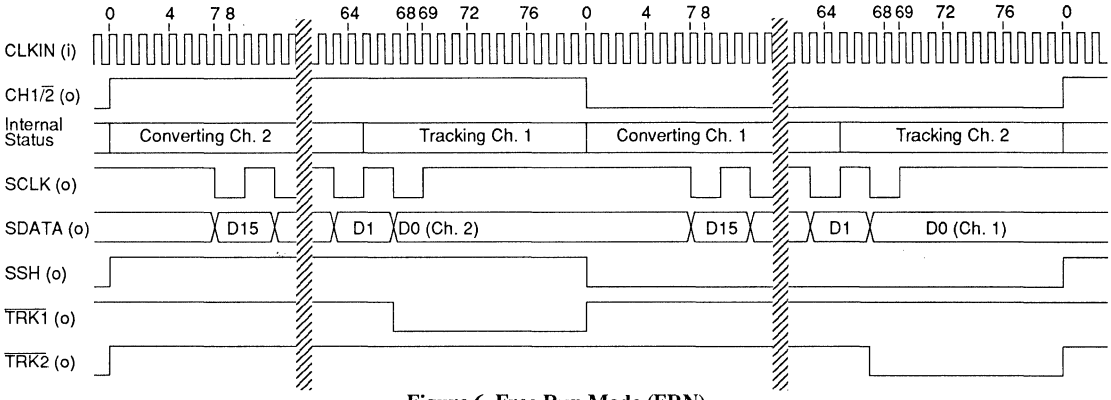


Figure 6. Free Run Mode (FRN)

Free Run (FRN)

Free Run is the internal, synchronous loopback mode. FRN mode is selected by tying SCKMOD and OUTMOD low. SCLK is an output, and operates exactly the same as SSC. In Free Run mode, the CS5102 initiates a new conversion every 80 master clock cycles, and alternates between channel 1 and channel 2. $\overline{HOLD}$ is disabled, and should be tied to either VD+ or DGND. CH1/$\overline{2}$ is an output, and will change at the start of each new conversion cycle, indicating which channel will be tracked after the current conversion is finished (Figure 6).

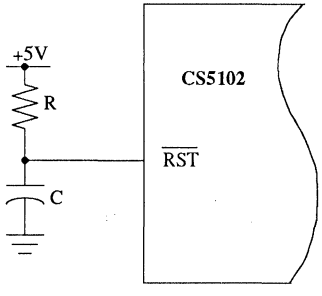


Figure 7. Power-up Reset Circuit

SYSTEM DESIGN WITH THE CS5102

Figure 8 shows a general system connection diagram for the CS5102.

Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

System Initialization

Upon power up, the CS5102 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5102's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before $\overline{RST}$ rises to guarantee an accurate calibration. Later, the CS5102 may be reset at any time to initiate a single full calibration.

When $\overline{RST}$ is brought low all internal logic clears. When it returns high a calibration cycle begins which takes 2,882,040 master clock cycles to complete (approximately 1.8 seconds with a 1.6 MHz master clock). The CS5102's $\overline{STBY}$ output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation. While calibrating, the CS5102 will ignore changes on the $\overline{HOLD}$ input. The CRS/$\overline{FIN}$ pin must remain low for the entire calibration cycle.

To perform the reset function, a simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 7. The RC time constant must be long enough to guarantee the rest of the system is fully powered up and stable by the end of reset. The resistor should be less than or equal to 10 kΩ.

Simultaneous Sampling

The CS5102 offers three digital output signals, SSH, $\overline{TRK1}$, and $\overline{TRK2}$ which can be used to

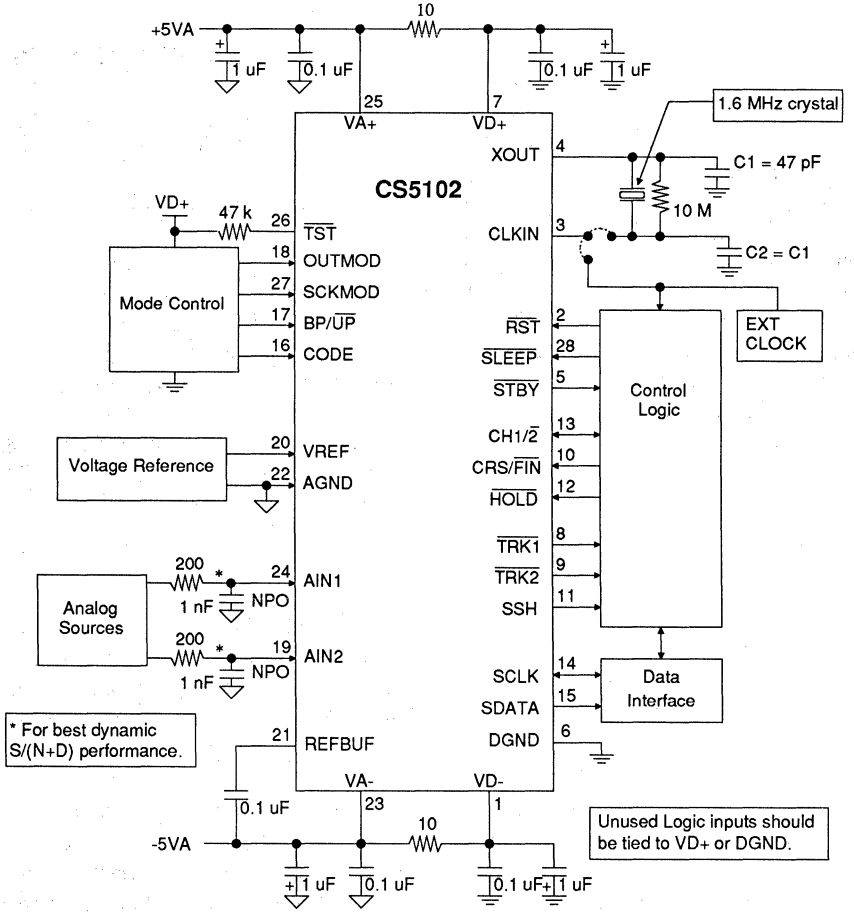


Figure 8. CS5102 System Connection Diagram

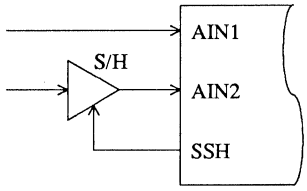


Figure 9. Simultaneous Sampling

control an external sample/hold amplifier to achieve simultaneous sampling of both channels.

Figures 3-6 show the timing relationships for SSH, $\overline{TRK1}$, and $\overline{TRK2}$. In the standard two-channel configuration, such as free run, the CS5102 samples the left and right channels 180° out of phase. Simultaneous sampling between channels 1 and 2 can be achieved as shown in Figure 9 using the CS5102's SSH output. The external sample/hold will freeze the analog signal on channel 2 as the CS5102 freezes the channel 1 input at AIN1. The external sample/hold will hold that signal valid at AIN2 until the CS5102 begins conversion of channel 2. Once that conversion begins, the sample/hold returns to the sample mode. The external sample/hold will have from the $\overline{HOLD}$ on channel 2 until the $\overline{HOLD}$ on channel 1 (80 clock cycles) to acquire the signal.

Single-Channel Operation

The CS5102 can alternatively be used to sample one channel by tying the CH1/$\overline{2}$ input high or low. The unused AIN pin should be tied to the analog input signal or to AGND. (If operating in free run mode, AIN1 and AIN2 must be tied to the same source, as CH1/$\overline{2}$ is reconfigured as an output.)

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5102 internally buffers all analog inputs (AIN1, AIN2, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X Series of A/D Converters*" is available for the CS5102. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5102 includes an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to coarse-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after coarse-charging from the buffer. This creates an ac current load as the CS5102 sequences through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 1.6 MHz clock the reference must supply a maximum load current of 4 µA peak-to-peak (0.4 µA typical). An output impedance of 2 Ω will therefore yield a maximum error of 8.0 µV. With a 4.5 V reference and LSB size of 138 µV this would insure approximately 1/20 LSB accuracy. A 10 µF capacitor exhibits an impedance of less than 2 Ω at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors. The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

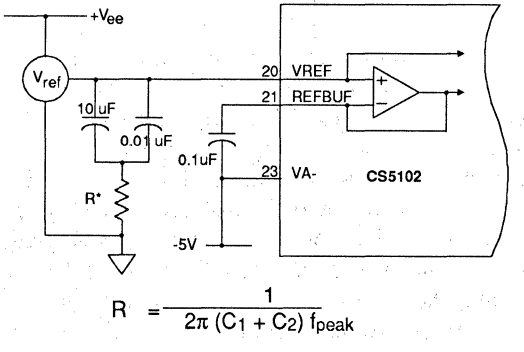


Figure 10. Reference Connections

The CS5102 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5102 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for coarse-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 11 exemplifies this operation. During coarse-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage may be offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

Fine-charge settling is specified as a maximum of 5.625 µs for an analog source impedance of less than 200 Ω. In addition, the comparator requires a

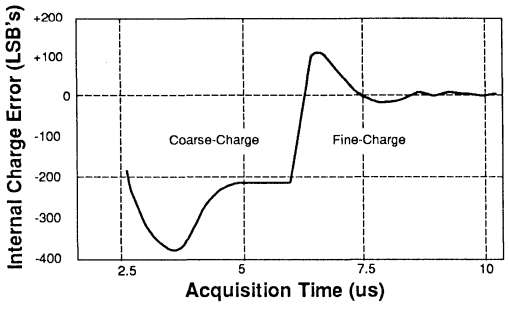


Figure 11. Charge Settling Time (1.6 MHz Clock)

source impedance of less than 400 Ω around 2 MHz for stability. The source impedance can be effectively reduced at high frequencies by adding capacitance from AIN to ground (typically 200 pF). However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input amplifiers, consult the application note: *Buffer Amplifiers for the CS501X Series of A/D Converters.*

$\overline{\text{SLEEP}}$ Mode Operation

The CS5102 includes a $\overline{\text{SLEEP}}$ pin. When $\overline{\text{SLEEP}}$ is active (low) the CS5102 will dissipate very low power to retain its calibration memory when the device is not sampling. It does not require calibration after $\overline{\text{SLEEP}}$ is made inactive (high). When coming out of $\overline{\text{SLEEP}}$, sampling can begin as soon as the oscillator starts (time will depend on the particular oscillator components) and the REFBUF capacitor is charged (which takes about 3 ms). To achieve minimum start-up time, use an external clock and leave the voltage reference powered-up. Connect a resistor (2 kΩ) between pins 20 and 21 to keep the REFBUF capacitor charged. Conversion can then begin as soon as the A/D has completed a coarse/fine sample period.

To retain calibration memory while $\overline{\text{SLEEP}}$ is active (low) VA+ and VD+ must be maintained at greater than 2.0V. VA- and VD- can be allowed to go to 0 volts. The voltages into VA- and VD- cannot just be "shut-off" as these pins cannot be allowed to float to potentials greater than AGND/DGND. If the supply voltages to VA- and VD- are removed, use a transistor switch to short these to the power supply ground while in $\overline{\text{SLEEP}}$ mode.

Grounding and Power Supply Decoupling

The CS5102 uses the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference.

The digital and analog supplies are isolated within the CS5102 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5102 must never exceed the positive analog supply by more than a diode drop or the CS5102 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram (Figure 8) shows a decoupling scheme which allows the CS5102 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10 Ω resistor to avoid the analog supply dropping

below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10 Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5102 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5102. The CDB5102 evaluation board is available for the CS5102, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5102, and can be reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CS5102 PERFORMANCE

Differential Nonlinearity

The self-calibration scheme utilized in the CS5102 features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of ±1/4 LSB, with code widths ranging from 3/4 to 5/4 LSB's.

Traditional laser trimmed ADC's have significant differential nonlinearities. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer function to be missing. Although their affect is minor on S/(N+D) with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80 dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional 16-bit ADC which achieves only 14-bit DNL.

The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algorithm. The worst-case codes for dynamic errors are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with

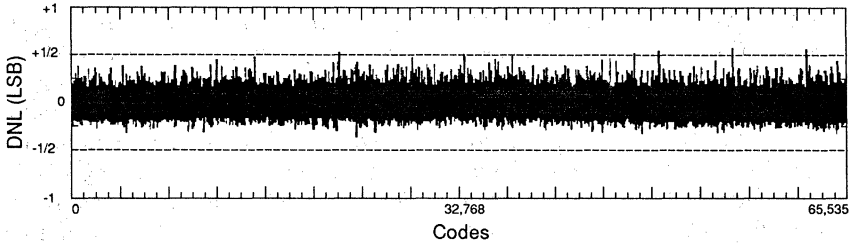


Figure 12. CS5102 DNL Plot

low-level signals, the codes around mid-scale (1/2 FS) are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5102 maintains accurate bit weights. DNL errors are dominated by residual calibration errors of ±1/4 LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on S/(N+D) are buried by white broadband noise. (See Figure 14)

A histogram plot of typical DNL of the CS5102 can be seen in Figure 12. A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

FFT Tests and Windowing

In the factory, the CS5102 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5102, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5102.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

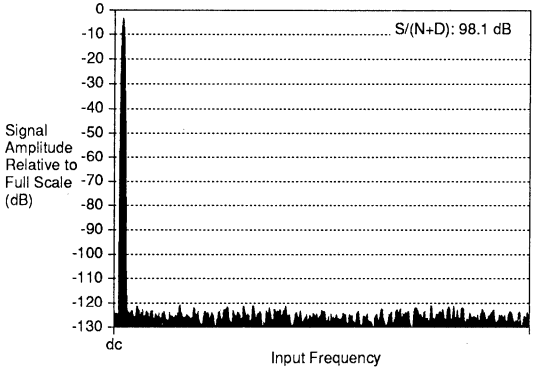


Figure 13. FFT Plot of Ideal 16-bit A/D Converter

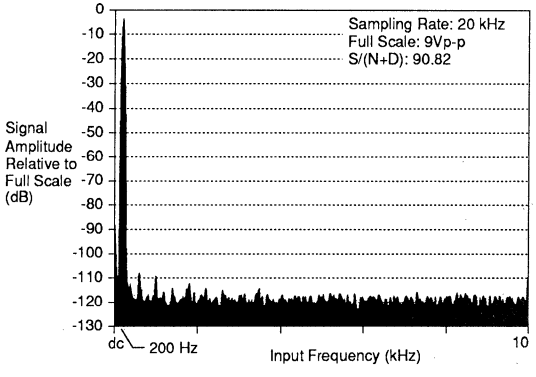


Figure 14. CS5102 FFT (FRN Mode, 1-Channel)

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CS5102 has a maximum side-lobe level of -92 dB. Figure 13 shows an FFT computed from an ideal 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. Averaging the FFT results from ten time records filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

As illustrated in Figure 14, the CS5102 typically yeilds >90 dB S/(N+D) and 0.001% THD. Unlike conventional successive-approximation ADC's, the CS5102's signal-to-noise and dynamic range are not limited by differential nonlinearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the baseband. This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

Sampling Distortion

Like most discrete sample/hold amplifier designs, the CS5102's inherent sample/hold exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is

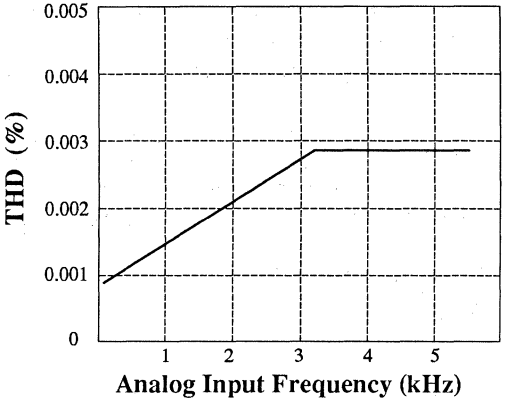


Figure 15. THD vs. Input Frequency with Full Scale Input (±4.5V)

given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 14).

The ideal relationship between the charge on the array and the input voltage can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate as shown in Figure 15. This distortion is negligible at signal levels below -10 dB of full-scale.

Noise

An A/D converter's noise can be described like that of any other analog component. However, the converter's output is in digital form so any filtering of its noise must be performed in the digital domain. Digitized samples of analog inputs are often considered individual, static snap-shots in time with no uncertainty or noise. In reality, the result of each conversion depends on the analog input level and the instantaneous value of noise sources in the ADC. If sequential samples from the ADC are treated as a "waveform", simple filtering can be implemented in software to improve noise performance with minimal processing overhead.

All analog circuitry in the CS5102 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5102 integrates to 35 µV rms in unipolar mode (70 µV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 16 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a CS5102 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the CS5102 has a "bell" shape with all codes other than 80CD due to internal noise.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5102 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 µV rms in unipolar mode.

Noise in the digital domain can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the CS5102's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the CS5102's noise performance can be

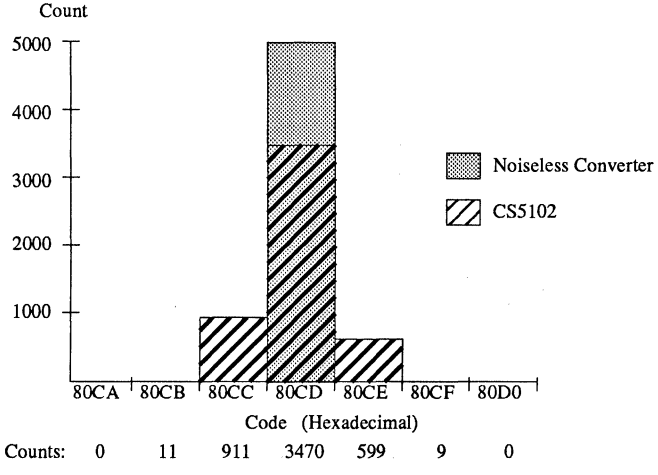


Figure 16. Histogram Plot of 5000 Conversion Inputs

maximized in any application by always sampling at the maximum specified rate of 20 kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependency causes distortion at high frequencies. The CS5102's proprietary architecture avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter, due to component noise, assumes a random nature. With only 100 ps peak-to-peak aperture jitter, the CS5102 can process full-scale signals up to 1/2 the throughput frequency without significant errors due to aperture jitter.

Power Supply Rejection

The CS5102's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5102's accuracy. This is because the CS5102 adjusts its offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 17 shows power supply rejection of the CS5102 in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

Notches of increased rejection arise from the auto-zeroing at the conversion rate. The frequencies at which these notches occur also depend on the value of the captured analog input. The line shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

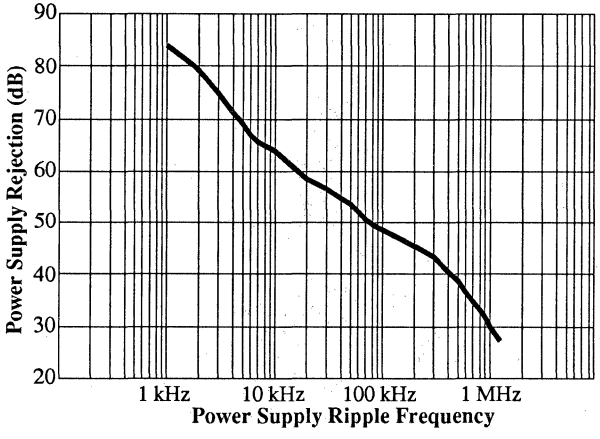
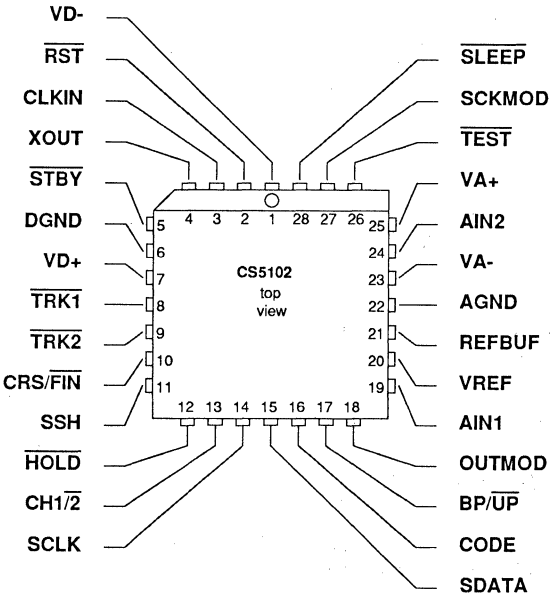


Figure 17. Power Supply Rejection

PIN DESCRIPTIONS

NEGATIVE DIGITAL POWER	VD-	1	28	SLEEP	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	RST	2	27	SCKMOD	SERIAL CLOCK MODE SELECT
MASTER CLOCK INPUT	CLKIN	3	26	TEST	TEST
CRYSTAL OUTPUT	XOUT	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	STBY	5	24	AIN2	CHANNEL 2 ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING CHANNEL 1	TRK1	8	21	REFBUF	REFERENCE BUFFER
TRACKING CHANNEL 2	TRK2	9	20	VREF	VOLTAGE REFERENCE
COARSE/FINE CHARGE CONTROL	CRS/FIN	10	19	AIN1	CHANNEL 1 ANALOG INPUT
SIMULTANEOUS SAMPLE/HOLD	SSH	11	18	OUTMOD	OUTPUT MODE SELECT
HOLD & CONVERT	HOLD	12	17	BP/UP	BIPOLAR/UNIPOLAR SELECT
INPUT CHANNEL SELECT	CH1/2	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT

CS5102



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 1.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 6.
Digital ground.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 23.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 22.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 3.
All conversions and calibrations are timed from a master clock which can be externally supplied by driving CLKIN.

XOUT - Crystal Output, PIN 4.
The master clock can be generated by tying a crystal across the CLKIN and XOUT pins. If an external clock is used, XOUT must be left floating.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 12.
A falling transition on this pin sets the CS5102 to the hold state and initiates a conversion. This input must remain low for at least 130 ns. When operating in Free Run Mode, $\overline{\text{HOLD}}$ is disabled, and should be tied to DGND or VD+.

CRS/$\overline{\text{FIN}}$ - Coarse Charge/Fine Charge Control, PIN 10.
When brought high during acquisition time, CRS/$\overline{\text{FIN}}$ forces the CS5102 into coarse charge state. This engages the internal buffer amplifier to track the analog input and charges the capacitor array much faster, thereby allowing the CS5102 to track high slewing signals. In order to get an accurate sample, the last coarse charge period before initiating a conversion (bringing $\overline{\text{HOLD}}$ low) must be longer than 3.75 µs. Similarly, the fine charge period immediately prior to conversion must be at least 5.625 µs. The CRS/$\overline{\text{FIN}}$ pin must be low during conversion time and during calibration time. For normal operation, CRS/$\overline{\text{FIN}}$ should be tied low, in which case the CS5102 will automatically enter coarse charge for 6 clock cycles immediately after the end of conversion.

CH1/$\overline{2}$ - Left/Right Input Channel Select, PIN 13.

Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle. When in Free Run Mode, CH1/$\overline{2}$ is an output, and will indicate which channel is being sampled during the current acquisition phase.

$\overline{\text{SLEEP}}$ - Sleep, PIN 28.

When brought low causes the CS5102 to enter a power-down state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode. If using the internal crystal oscillator, time must be allowed after $\overline{\text{SLEEP}}$ returns high for the crystal oscillator to stabilize. $\overline{\text{SLEEP}}$ should be tied high for normal operation.

CODE - 2's Complement/Binary Coding Select, PIN 16.

Determines whether output data appears in 2's complement or binary format. If high, 2's complement; if low, binary.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Range Select, PIN 17.

When low, the CS5102 accepts a unipolar input range from AGND to VREF. When high, the CS5102 accepts bipolar inputs from -VREF to +VREF.

SCKMOD - Serial Clock Mode Select, PIN 27.

When high, the SCLK pin is an input; when low, it is an output. Used in conjunction with OUTMOD to select one of 4 output modes described in Table 1.

OUTMOD - Output Mode Select, PIN 18.

The status of SCKMOD and OUTMOD determine which of four output modes is utilized. The four modes are described in Table 1.

SCLK - Serial Clock, PIN 14.

Serial data changes status on a falling edge of this input, and is valid on a rising edge. When SCKMOD is high SCLK acts as an input. When SCKMOD is low the CS5102 generates its own serial clock at one-fourth the master clock frequency and SCLK is an output.

$\overline{\text{RST}}$ - Reset, PIN 2.

When taken low, all internal digital logic is reset. Upon returning high, a full calibration sequence is initiated which takes 2,882,040 CLKIN cycles to complete. During calibration, the $\overline{\text{HOLD}}$ input will be ignored. The CRS/$\overline{\text{FIN}}$ pin must be low when $\overline{\text{RST}}$ rises and remain low during the calibration time. The CS5102 must be reset at power-up for calibration, however; calibration is maintained during $\overline{\text{SLEEP}}$ mode, and need not be repeated when resuming normal operation.

Analog Inputs

AIN1, AIN2 - Channel 1 and 2 Analog Inputs, PINS 19 and 24.

Analog input connections for the left and right input channels.

VREF - Voltage Reference, PIN 20.

The analog reference voltage which sets the analog input range. In unipolar mode VREF sets full-scale; in bipolar mode its magnitude sets both positive and negative full-scale.

Digital Outputs

$\overline{\text{STBY}}$ - Standby (Calibrating), PIN 5.

Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

SDATA - Serial Output, PIN 15.

Presents each output data bit on a falling edge of SCLK. Data is valid to be latched on the rising edge of SCLK.

SSH - Simultaneous Sample/Hold, PIN 11.

Used to control an external sample/hold amplifier to achieve simultaneous sampling between channels.

$\overline{\text{TRK1}}$, $\overline{\text{TRK2}}$ - Tracking Channel 1, Tracking Channel 2, PINS 8 and 9.

Falls low at the end of a conversion cycle, indicating the acquisition phase for the corresponding channel. The $\overline{\text{TRK1}}$ or $\overline{\text{TRK2}}$ pin will return high at the beginning of conversion for that channel.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 21.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

$\overline{\text{TEST}}$ - Test, PIN 26.

Allows access to the CS5102's test functions which are reserved for factory use. Must be tied to VD+.

Ordering Guide

Model	Conversion Time	Throughput	Linearity	Temperature	Package
CS5102-JP	40 µs	20 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5102-KP	40 µs	20 kHz	0.002%	0 to 70 °C	28-Pin Plastic DIP
CS5102-JL	40 µs	20 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5102-KL	40 µs	20 kHz	0.002%	0 to 70 °C	28-Pin PLCC
CS5102-AD	40 µs	20 kHz	0.003%	-40 to 85 °C	28-Pin CerDIP
CS5102-BD	40 µs	20 kHz	0.002%	-40 to 85 °C	28-Pin CerDIP
CS5102-AL	40 µs	20 kHz	0.003%	-40 to 85 °C	28-Pin PLCC
CS5102-BL	40 µs	20 kHz	0.002%	-40 to 85 °C	28-Pin PLCC
CS5102-SD	40 µs	20 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
CS5102-TD	40 µs	20 kHz	0.003%	-55 to 125 °C	28-Pin CerDIP

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Signal to Peak Harmonic or Noise

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-(Noise + Distortion)

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

• Notes •

Semiconductor Corporation

CS5126

16-Bit, Stereo A/D Converter for Digital Audio

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Stereo or Monaural Capability
  - Serial Output
- Monaural Sampling Rates up to 100 kHz
  - 50 kHz/Channel Stereo Sampling
- Signal-to-(Noise+Distortion): 92 dB
- Dynamic Range: 92 dB
  - 95dB in 2X Oversampling Schemes
- Interchannel Isolation: 90 dB
- 2's Complement or Binary Coding
- Low Power Dissipation: 260 mW
  - Power Down Mode for Portable Applications
- Evaluation Board Available

General Description

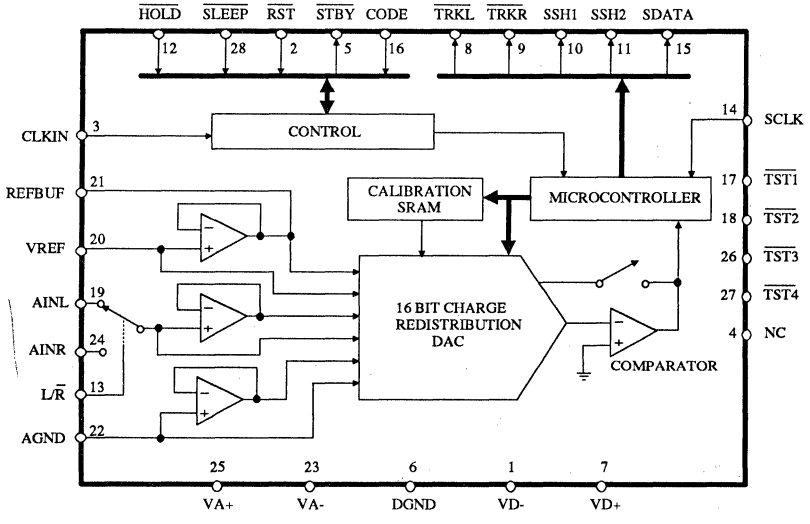
The CS5126 CMOS analog-to-digital converter is an ideal front-end for stereo or monaural digital audio systems. The CS5126 can be configured to handle two channels at up to 50kHz sampling per channel, or it can be configured to sample one channel at rates up to 100kHz.

The CS5126 executes a successive approximation algorithm using a charge redistribution architecture. On-chip self-calibration circuitry has 18-bit resolution thus avoiding any degradation in performance with low-level signals. The charge redistribution technique also provides an inherent sampling function which avoids the need for external sample/hold amplifiers.

Signal-to-(noise+distortion) in stereo operation is 92dB, and is dominated by internal broadband noise (1/2 LSB rms). When the CS5126 is configured for 2X oversampling, digital post-filtering bandlimits this white noise to 20kHz, increasing dynamic range to 95dB.

ORDERING INFORMATION: (was CSZ5126-KP)

CS5126-KP	0 °C to 70 °C	28-Pin Plastic DIP
CS5126-KL	0 °C to 70 °C	28-Pin PLCC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 TWX: 910-874-1352

ANALOG CHARACTERISTICS (T_A = 25°C;
VA+, VD+ = 5V; VA-, VD- = -5V; Full-Scale Input Sinewave, 1kHz; f_{clk} = 24.578MHz; VREF = 4.5V;
Analog Source Impedance = 200Ω; Stereo operation, L/$\overline{R}$ toggling at 48 kHz unless otherwise specified.)

Parameter*	Symbol	CS5126-KP min	typ	max	Units
Resolution				16	Bits
Dynamic Performance					
Signal-to-(Noise plus Distortion) V IN = ±FS (10Hz to 20kHz) V IN = -20dB (f = 20kHz)	S/(N+D)	 90 70	 92 72		 dB dB
Total Harmonic Distortion	THD		0.001		%
Dynamic Range Stereo Mode Monaural (20kHz BW)	DR	90	92 95		dB dB
Idle Channel Noise	$V_{n(ic)}$		1/2		LSB rms
Interchannel Isolation (Note 1)	I_{ic}		90		dB
Interchannel Mismatch	M_{ic}		0.01		dB
dc Accuracy					
Full-Scale Error	FSE		± 4		LSB
Bipolar Offset Error	BPO		± 4		LSB
Analog Input					
Aperture Time	t_{apt}		30		ns
Aperture Jitter	t_{ajt}		100		ps
Input Capacitance (Note 2)	C_{in}		200		pF
Power Supplies					
Power Supply Current Positive Analog ($\overline{SLEEP}$ High) Negative Analog Positive Digital (Note 3) Negative Digital	I_{A+} I_{A-} I_{D+} I_{D-}		18 −18 8 −8	23 −23 12 −12	mA mA mA mA
Power Dissipation ($\overline{SLEEP}$ High) (Notes 3,4) ($\overline{SLEEP}$ Low)	P_{do} P_{ds}		260 1	350	mW mW
Power Supply Rejection (Note 5) Positive Supplies Negative Supplies	PSR		 84 84		 dB dB

Notes:
1. dc to 20kHz
2. Applies only in the track mode. When converting or calibrating, input capacitance will typically be 10 pF.
3. All outputs unloaded. All inputs CMOS levels.
4. Power dissipation in sleep mode applies with no master clock applied (CLKIN high or low).
5. With 300mV p-p, 1kHz ripple applied to each supply separately. A plot of typical power supply rejection appears in the *Analog Circuit Connections* section.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 6)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current - CLKIN pin	I_{in}	-	-	10	uA
Input Leakage Current - Except CLKIN pin	I_{in}	-	-	60	uA

Note: 6. I_{OUT} = -100 µA. This specification guarantees that each digital output will drive one TTL load (V_{OH} = 2.4V @ I_{OUT} = -40 µA).

3

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 7.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage: (Note 8)		V_{AIN}	−VREF	-	VREF	V

Notes: 7. All voltages with respect to ground.
8. The CS5126 can accept input voltages up to the analog supplies (VA+, VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below -VREF.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 9)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	−0.3	VD+ + 0.3	V
Ambient Temperature (power applied)		T_A	−55	125	°C
Storage Temperature		T_{stg}	−65	150	°C

Notes: 9. Transient currents of up to 100 mA will not cause SCR latch-up.

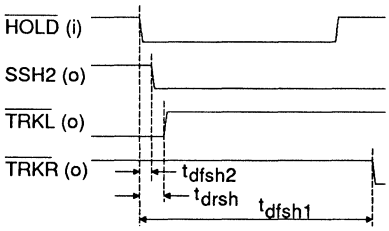
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

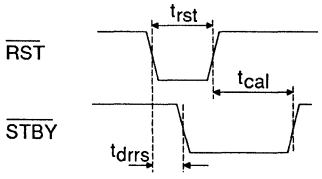
(T_A = 25 °C; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Period	t_{clk}	40	-	-	ns
$\overline{HOLD}$ to SSH2 Falling (Note 10)	t_{dfsh2}	-	80	-	ns
$\overline{HOLD}$ to $\overline{TRKL}$, $\overline{TRKR}$ SSH1 Falling	t_{dfsh1}	198 t_{clk}	-	214 t_{clk} + 50	ns
$\overline{HOLD}$ to $\overline{TRKL}$, $\overline{TRKR}$ SSH1, SSH2 Rising	t_{drsh}		80		ns
$\overline{RST}$ Pulse Width	t_{rst}	150	-	-	ns
$\overline{RST}$ to $\overline{STBY}$ Falling	t_{drrs}	-	100	-	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising	t_{cal}	-	34,584,480	-	t_{clk}
$\overline{HOLD}$ Pulse Width	t_{hold}	2 t_{clk} + 50	-	192 t_{clk}	ns
$\overline{HOLD}$ to L/$\overline{R}$ Edge (Note 10)	t_{dhlri}	- 30	-	192 t_{clk}	ns
SCLK period	t_{sclk}	200	-	-	ns
SCLK Pulse Width Low	t_{sclkl}	50	-	-	ns
SCLK Pulse Width High	t_{sclkh}	50	-	-	ns
SCLK Falling to SDATA Valid	t_{dss}	-	100	140	ns
$\overline{HOLD}$ Falling to SDATA Valid	t_{dhs}	-	140	200	ns

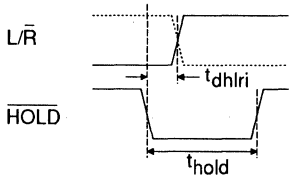
Note: 10. SSH2 only works correctly if $\overline{HOLD}$ falling edge is within ±30ns of L/$\overline{R}$ edge OR if $\overline{HOLD}$ falling edge occurs between 30ns before $\overline{HOLD}$ rises to 192 t_{clk} after $\overline{HOLD}$ falls.



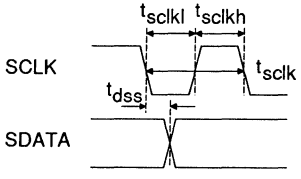
Control Output Timing



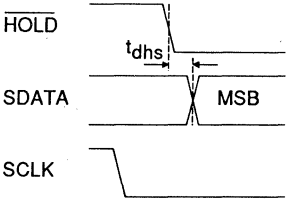
Reset and Calibration Timing



Channel Selection Timing



Serial Data Timing



Data Transmit Start Timing

GENERAL DESCRIPTION

The CS5126 is a 2-channel, 100kHz A/D converter designed specifically for stereo digital audio. The device includes an inherent sample/hold and an on-chip analog switch for stereo operation. Both left and right channels can thus be sampled and converted at rates up to 50kHz per channel. Alternatively, the CS5126 can be implemented in 2X oversampling schemes for improved dynamic range and distortion.

Output data is available in serial form with either binary or 2's complement coding. Control outputs are also supplied for use with an external sample/hold amplifier to implement simultaneous sampling.

THEORY OF OPERATION

The CS5126 implements a standard successive-approximation algorithm using a charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. When not converting, the CS5126 tracks the analog input signal. The input voltage is applied across each leg of the DAC capacitor array, thus performing a voltage-to-charge conversion.

When the conversion command is issued, the charge is trapped on the capacitor array and the analog input is thereafter ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the binary-weighted legs of the capacitor array to the voltage reference and analog ground. All legs share one common node at the input to the converter's comparator. This forms a binary-weighted capacitive divider. Since the charge at the comparator's input remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance which will drive the voltage to the comparator's trip point. That binary fraction of capacitance represents the converter's digital output.

Calibration

The ability of the CS5126 to convert accurately clearly depends on the accuracy of its DAC. The CS5126 uses an on-chip self-calibration scheme to insure low distortion and excellent dynamic range *independent of input signal conditions.*

Each binary-weighted bit capacitor actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). The result is typical differential nonlinearity of ±1/4 LSB. That is, codes typically range from 3/4 to 5/4 LSB's wide.

The CS5126 should be reset upon power-up, thus initiating a calibration cycle which takes 1.4 seconds to complete. The CS5126 then stores its calibration coefficients in on-chip SRAM, and can be recalibrated at any later time.

SYSTEM DESIGN WITH THE CS5126

All timing and control inputs to the CS5126 can be easily generated from a master system clock. The CS5126 outputs serial data and a variety of digital outputs which can be used to control an external sample/hold amplifier for simultaneous sampling. The actual circuit connections depend on the system architecture (stereo or monaural 2X oversampling), and on the sampling characteristics (simultaneous or sequential sampling between channels).

System Initialization

Upon power up, the CS5126 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5126's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before $\overline{RST}$ rises to guarantee an accurate calibration. Later, the CS5126 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5126 will clear and initiate a new calibration cycle mid-conversion or midcalibration.

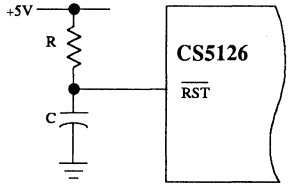


Figure 1. Power-On Reset Circuit

When $\overline{RST}$ is brought low all internal logic clears. When it returns high a calibration cycle begins which takes 34,584,480 master clock cycles to complete (approximately 1.4 seconds with a standard 24MHz master clock). The CS5126's $\overline{STBY}$ output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation.

A simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 1. The RC time constant must be long enough to guarantee the rest of the system is fully powered up and stable by the end of reset.

Master Clock

The CS5126 operates from an externally-supplied master clock. In stereo operation, the master clock frequency is set at 512 times the per-channel sampling rate (256 in 2X oversampling schemes). The CS5126 can accept master clocks up to 24.576 MHz for 48kHz stereo sampling or 96kHz monaural oversampling.

All timing and control inputs for channel selection, sampling, and serial data transmission may be divided down from the master clock. This yields a completely synchronous system, avoiding sampling and conversion errors due to asynchronous digital noise.

3

CIRCUIT CONNECTIONS

Stereo Operation

Figure 2 shows the standard circuit connections for operating the CS5126 in its stereo mode. The $\overline{HOLD}$, L/$\overline{R}$, and SCLK inputs are derived from the master clock using a binary divider string. A 24.576 MHz master clock is required for a sampling rate of 48kHz per channel.

For 48kHz stereo sampling, the CS5126 must sample and convert at a 96kHz rate to handle both channels. The master clock is divided by 256 and applied to the $\overline{HOLD}$ input. A falling transition on the $\overline{HOLD}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{HOLD}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns.

In stereo operation the CS5126 alternately samples and converts the left and right input channels. This alternating channel selection is achieved by dividing the $\overline{HOLD}$ input by two (that is, dividing the master clock by 512) and applying it to the L/$\overline{R}$ input. Upon completion of each conversion cycle, the CS5126 automatically returns to the track mode. The status of L/$\overline{R}$ as

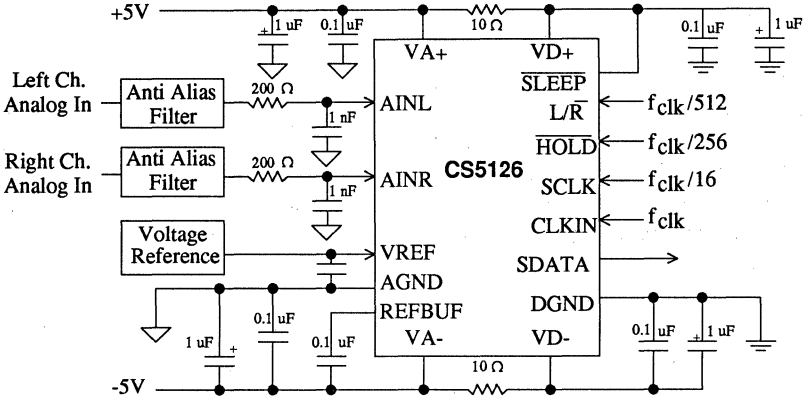


Figure 2. Stereo Mode Connection Diagram

each conversion finishes determines which channel is acquired and tracked. The L/$\overline{R}$ input must remain valid at least until 30ns before the next falling transition on $\overline{HOLD}$.

As shown in the timing diagram in Figure 3, the CS5126 uses pipelined data transmission. That is, data from a particular conversion transmits during the *next* conversion cycle. The serial clock input, SCLK, is derived by dividing the master clock by 16. The MSB (most-significant- bit) will be stable on the first rising edge of SCLK after a falling transition on HOLD. With a serial clock of $f_{clk}/16$, transmission of all 16 output bits will span an entire conversion and acquisition cycle.

STEREO MODE PERFORMANCE

As illustrated in Figure 4, the CS5126 typically provides 92dB S/(N+D) and 0.001% THD. Unlike conventional successive-approximation ADC's, the CS5126's signal-to-noise and dynamic range are not limited by differential nonlinearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the baseband.

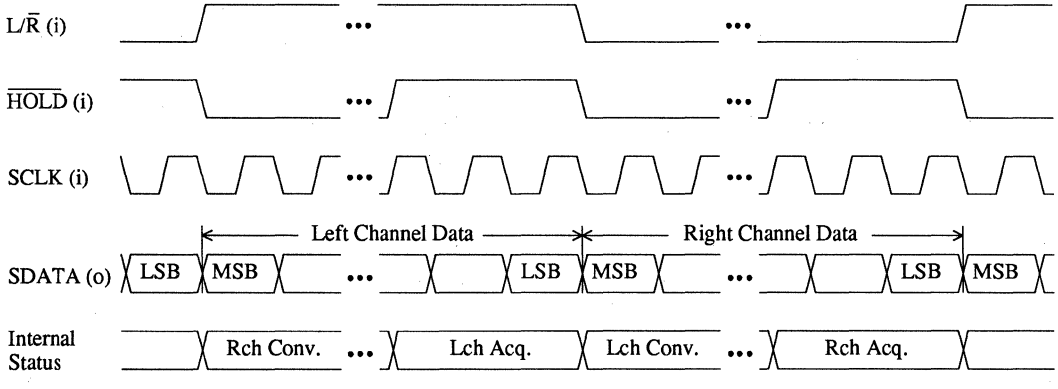


Figure 3. Stereo Mode Timing

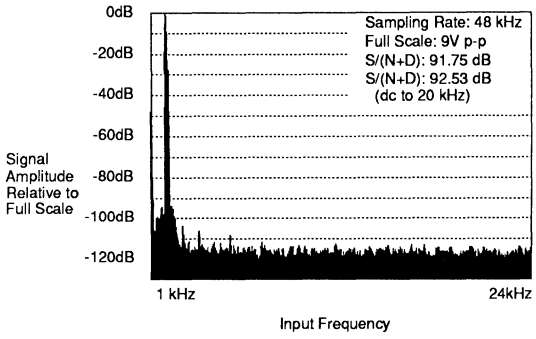


Figure 4. FFT Plot of CS5126 in Stereo Mode (Left Channel with 1 kHz, Full-Scale Input)

This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

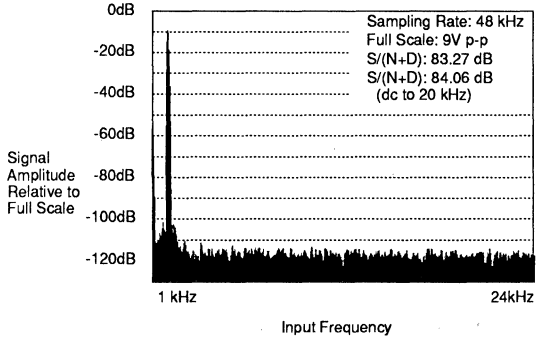
Differential Nonlinearity

The self-calibration scheme utilized in the CS5126 features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of ±1/4 LSB, with code widths ranging from 3/4 to 5/4 LSB's. This insures consistent sound quality independent of signal level.

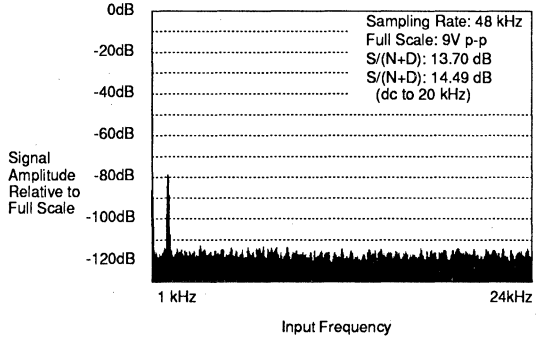
Traditional laser trimmed ADC's have significant differential nonlinearities which are disastrous to sound quality with low-level signals. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer function to be missing. Although their affect is minor on S/(N+D) with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional hybrid ADC capable of only 14-bit DNL.

The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is



a. Left Channel with 1 kHz, -10 dB Input



b. Left Channel with 1 kHz, -80 dB Input

Figure 5. FFT Plots of CS5126 in Stereo Mode

driven too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algorithm. The worst-case codes for dynamic errors are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with low-level signals, the codes around in mid-scale, (that is, 1/2 FS), are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5126 maintains accurate bit weights. DNL errors are dominated by residual calibration errors of ±1/4 LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on S/(N+D) are buried by white broadband noise. This yields excellent sound quality *independent of signal level.*
(See Figure 5)

Sampling Distortion

Like most discrete sample/hold amplifier designs, the CS5126's inherent sample/hold exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 4).

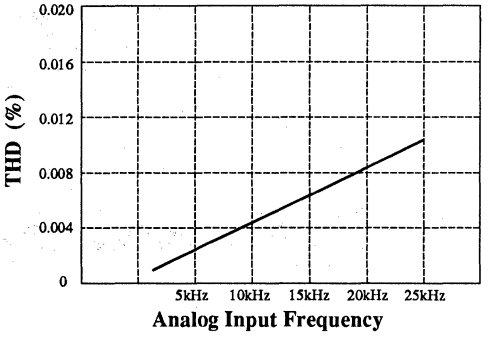


Figure 6. THD vs Input Frequency (9V p-p Full-Scale Input)

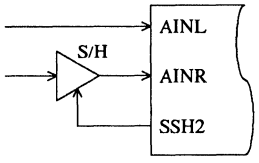
The ideal relationship between the charge on the array and the input voltage can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate as shown in Figure 6 since the magnitude of the steady state current increases. First noticeable at 1kHz, this distortion assumes a linear relationship with input frequency. *With signals 20dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance.*

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5126 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

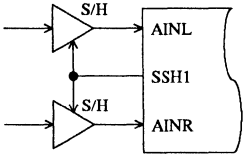
Simultaneous Sampling

The CS5126 offers four digital output signals, SSH1, SSH2, $\overline{TRKL}$, and $\overline{TRKR}$ which can be used to control external sample/hold amplifiers to achieve simultaneous sampling and/or reduce sampling distortion.

Figure 7 shows the timing relationships for SSH1, SSH2, $\overline{TRKL}$, and $\overline{TRKR}$. In the stereo configuration shown in Figure 1 the CS5126 samples the left and right channels 180° out of phase. Simultaneous sampling between the left and right channels can be achieved as shown in Figure 8a using the CS5126's SSH2 output. The external sample/hold will freeze the right channel analog signal as the CS5126 freezes the left channel input at AINL. It will hold that signal valid at AINR until the CS5126 begins a right channel conversion. Once that conversion begins, the sample/hold returns to the sample mode. The acquisition time for the external sample/hold amplifier must not exceed the CS5126's minimum conversion time of 192 master clock cycles (7.8µs for 48kHz stereo sampling).



a. Standard Connections



b. High-Slew Conditions

Figure 8. Simultaneous Sampling Connections

The CS5126's sampling distortion with high-frequency, high-amplitude input signals may be improved if a low distortion sample/hold amplifier is used as shown in Figure 8a. The right channel input at AINR will appear as dc to the CS5126 resulting in *no ac current* flowing through the internal MOS switches. Sampling distortion can

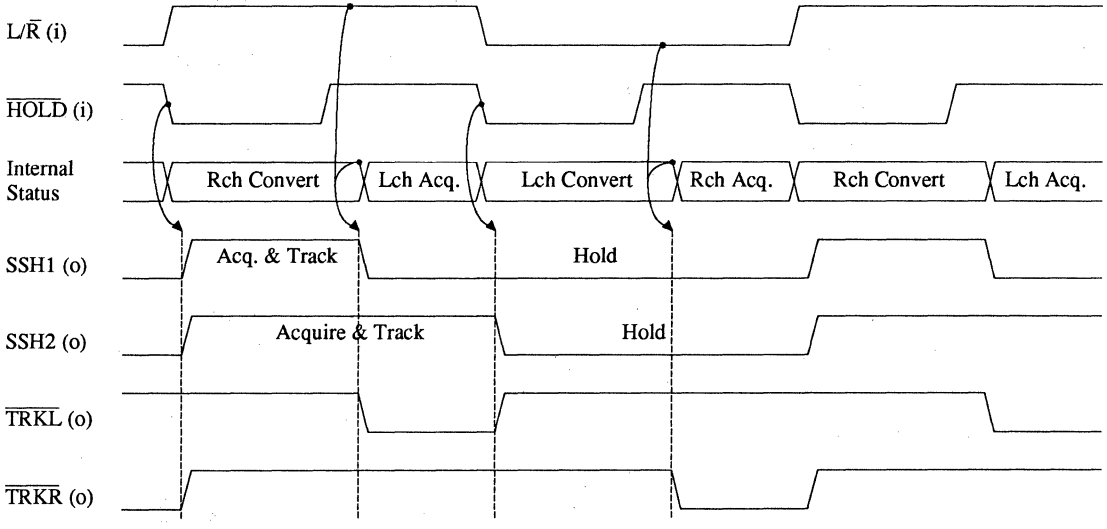
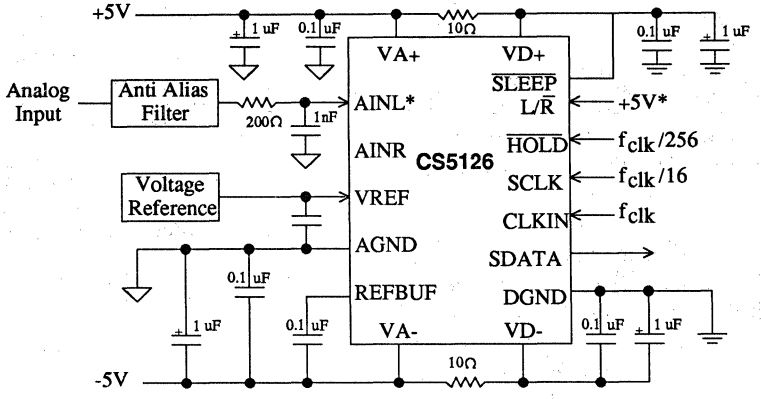


Figure 7. External Sampling Control Output Timing



* AINR can alternatively be used with L/$\overline{R}$ grounded

Figure 9. Monaural 2X Oversampling Connections

likewise be improved for *both channels* using the SSH1 output as shown in Figure 8b. Similarly, the acquisition time for the external sample/hold amplifiers must not exceed the minimum conversion time of 192 master clock cycles (7.8µs for 48kHz stereo sampling).

Oversampling

The CS5126 can alternatively be used to oversample *one channel* (monaural) by 2X simply by tying the L/$\overline{R}$ input high or low. This moves much of the anti-alias burden from analog filters to digital post-filtering. The analog filters' corner can be pushed out in frequency with lower roll-off, allowing lower passband ripple and more linear phase in the audioband. Digital FIR filtering, meanwhile, can be used to implement high roll-off filters with ultra-low passband ripple and perfectly linear phase.

Oversampling not only improves system-level filtering performance, but it also enhances the ADC's dynamic range and distortion characteristics. All noise energy in a sampled, digital signal aliases into the baseband between dc and one-half the sampling rate. For an *ideal* successive-approximation ADC the noise spectral content is

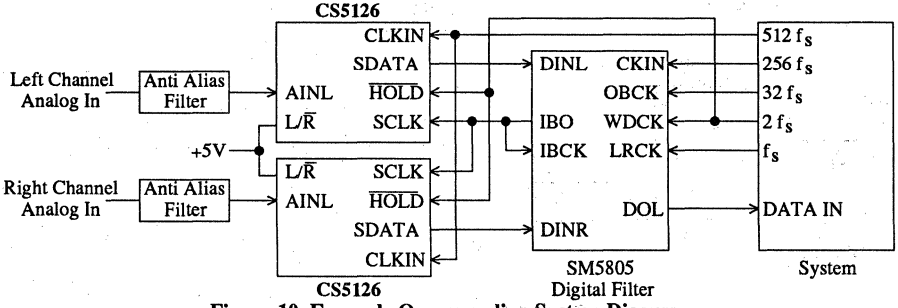


Figure 10. Example Oversampling System Diagram

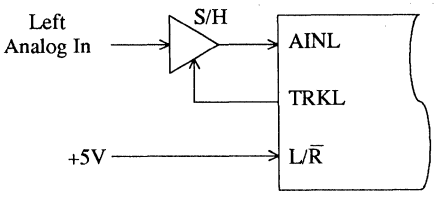


Figure 11. High-Slew Monaural Connections

white. Therefore, in a 2X oversampling scheme such as 96kHz sampling the ADC's noise will be be spread *uniformly* from dc to 48kHz. Digital post-filtering then rejects noise outside of the 20kHz or 22kHz bandwidth, resulting in improved signal-to-noise and dynamic range. For a white noise spectrum, a 2X reduction in bandwidth yields a 3dB improvement in dynamic range.

Due to its on-chip self-calibration scheme, the CS5126's dynamic range is limited only by *white* broadband noise rather than signal-dependent DNL errors. Therefore, the CS5126 picks up a full 3dB improvement in dynamic range to 95dB when implemented in 2X oversampling schemes.

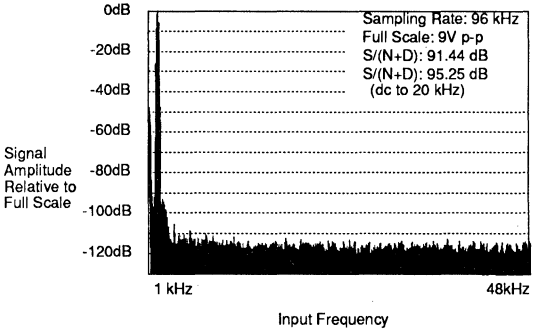


Figure 12. FFT Plot of CS5126 in Monaural 2X Oversampling Mode

Oversampling and digital filtering also enhance the ADC's distortion performance. Consider for example a full-scale 15kHz input signal to the CS5126 sampling at 96kHz. Sampling distortion produces THD of approximately 0.005% (86dB) at the converter's output. Most of the distortion energy resides in the second and third harmonics at 30kHz and 45kHz. Meanwhile, digital filters such as the SM5805 shown in Figure 10 will roll-off rapidly from 22kHz to 28kHz and reject distortion energy in the second, third, and fourth harmonics. Clearly, oversampling results in superior system-level distortion.

Still, if the CS5126's distortion performance with high-frequency, high-amplitude signals must be enhanced in 2X oversampling schemes, the $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ outputs can be used. Either $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ will fall at the end of each conversion cycle depending on which channel is being acquired. The AINL and $\overline{\text{TRKL}}$ connections (or AINR and $\overline{\text{TRKR}}$) can be used as shown in Figure 11 to control an external low-distortion sample/hold to create an effective dc input for the CS5126 and remove sampling distortion.

Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The CS5126 has a power down mode, initiated by bringing $\overline{\text{SLEEP}}$ low. During power down, the A/D Converter's calibration information is retained. The CS5126 may be used for conversion immediately after $\overline{\text{SLEEP}}$ is brought high.

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5126 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

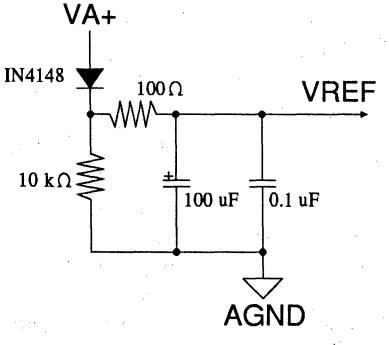
Reference Considerations

An application note titled "*Voltage references for the CS501X/CSZ511X Series of A/D Converters*" is available which describes the dynamic load conditions presented by the VREF input on Crystal's self-calibrating SAR A/D converters (including the CS5126). As the CS5126 sequences through bit decisions it switches portions of the capacitor array to the VREF pin in accordance with the successive-approximation algorithm. For proper operation, the source impedance at the VREF pin must remain low at frequencies up to 1MHz.

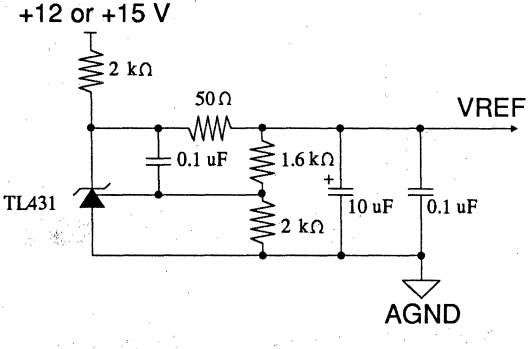
A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the frequencies of interest, so the reference voltage can simply be derived as shown in Figure 13a. Although very low cost, this reference has almost no power supply rejection from the VA+ line.

Alternatively, a more stable and precise reference can be generated using a TL431 shunt reference from T.I. or Motorola, as shown in Figure 13b.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 24 MHz clock the reference must supply a maximum load current of 20µA peak-to-peak (2µA typical). An output impedance of 2Ω will therefore yield a maximum error of 40µV. With a 4.5V reference and LSB size of 138µV this would insure approximately 1/4 LSB accuracy. A 10µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.



a. Simple Reference



b. Low-cost Shunt Reference

Figure 13. Suggested Voltage Reference Circuits

The CS5126 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5126 can actually accept reference voltages up to the positive analog supply. However, as the reference voltage approaches VA+ the external drive requirements may increase at VREF.

An internal reference buffer is used to protect the external reference from current transients during conversion. This internal buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-.

Analog Input Connection

Each time the CS5126 finishes a conversion cycle it switches the internal capacitor array to the appropriate analog input pin, AINL or AINR. This creates a minor dynamic load at the sampling frequency. All throughput specifications apply for maximum analog source impedances of 200Ω at AINL and AINR. In addition, the comparator requires source impedances of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. For more information, see our Application Note: "*Input Buffers for the CS501X/CSZ511X Series of A/D Converters*"

Analog Input Range/Coding Format

The CS5126 features a bipolar input range with the reference voltage applied to VREF defining both positive and negative full-scale. The coding format is set by the state of the CODE input. If high, coding is 2's complement; if low, the CS5126's output is in offset-binary format.

Grounding and Power Supply Decoupling

The CS5126 uses the analog ground connection, AGND, only as a reference voltage. *No dc power or signal currents flow through the AGND connection,* thus minimizing the potential for interchannel crosstalk. Also, AGND is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both analog inputs and the reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground. The digital and analog supplies are isolated within the CS5126 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5126 must never exceed the positive analog supply by more than a diode drop or the CS5126 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagrams in Figures 2 and 9 show a decoupling scheme which allows the CS5126 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10 Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5126 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5126. The CDB5126 evaluation board is available for the CS5126, which avoids the need to design, build, and debug a high-precision PC

board to initially characterize the part. The board comes with a socketed CS5126, and can be quickly reconfigured to simulate any combination of sampling and master clock conditions.

Power Supply Rejection

The CS5126 features a fully differential comparator design, resulting in superior power supply rejection. Rejection is further enhanced by the on-chip self-calibration and "auto-zero" process. Figure 14 shows worst-case rejection for all combinations of conversion rates and input conditions.

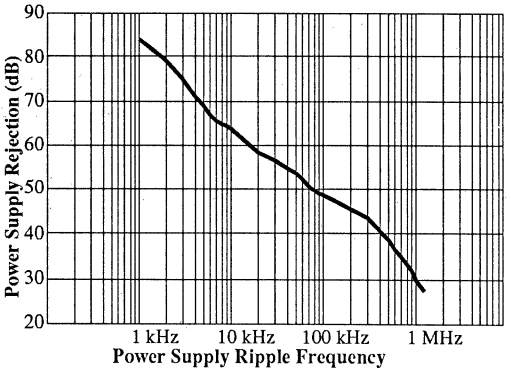
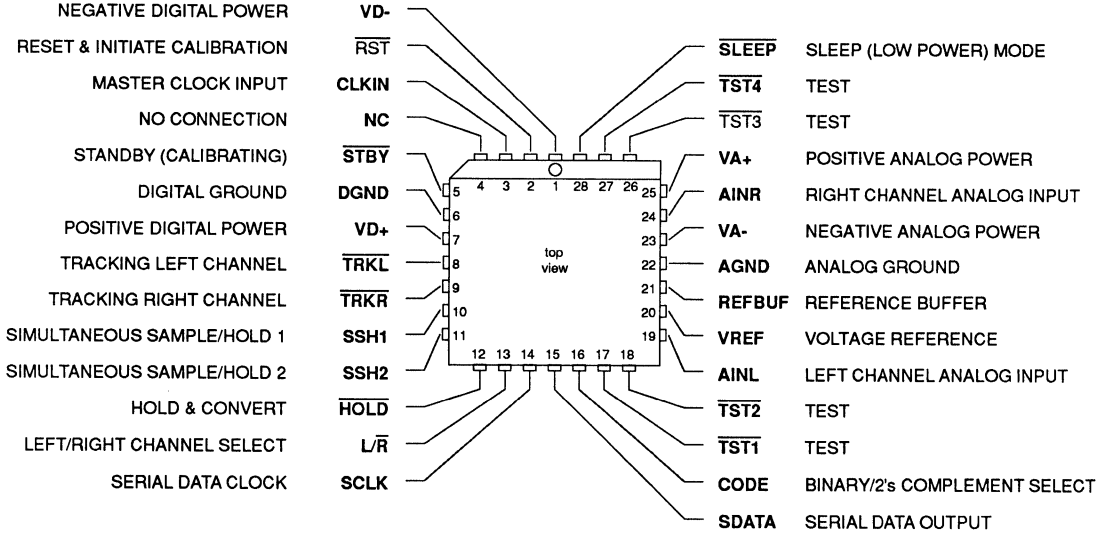


Figure 14. Power Supply Rejection

PIN DESCRIPTIONS

NEGATIVE DIGITAL POWER	VD-	1	28	$\overline{\text{SLEEP}}$	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	$\overline{\text{RST}}$	2	27	$\overline{\text{TST4}}$	TEST
MASTER CLOCK INPUT	CLKIN	3	26	$\overline{\text{TST3}}$	TEST
NO CONNECTION	NC	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	$\overline{\text{STBY}}$	5	24	AINR	RIGHT CHANNEL ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING LEFT CHANNEL	$\overline{\text{TRKL}}$	8	21	REFBUF	REFERENCE BUFFER
TRACKING RIGHT CHANNEL	$\overline{\text{TRKR}}$	9	20	VREF	VOLTAGE REFERENCE
SIMULTANEOUS SAMPLE/HOLD 1	SSH1	10	19	AINL	LEFT CHANNEL ANALOG INPUT
SIMULTANEOUS SAMPLE/HOLD 2	SSH2	11	18	$\overline{\text{TST2}}$	TEST
HOLD & CONVERT	$\overline{\text{HOLD}}$	12	17	$\overline{\text{TST1}}$	TEST
LEFT/RIGHT CHANNEL SELECT	L/$\overline{\text{R}}$	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 1.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 6.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 23.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 22.
Analog ground reference.

Digital Inputs

CLKIN - Clock Input, PIN 3.
All conversions and calibrations are timed from a master clock which must be externally supplied.

$\overline{\text{HOLD}}$ - Hold, PIN 12.
A falling transition on this pin sets the CS5126 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

L/$\overline{\text{R}}$ - Left/Right Input Channel Select, PIN 13.
Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle.

$\overline{\text{SLEEP}}$ - Sleep, PIN 28.
When brought low causes the CS5126 to enter a low-power quiescent state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode.

CODE - 2's Complement/Binary Coding Select, PIN 16.
Determines whether data appears in 2's complement or offset-binary format. If high, 2's complement; if low, offset-binary.

SCLK - Serial Clock, PIN 14.
Serial data changes status on a falling edge of this input, and is valid on a rising edge.

$\overline{\text{RST}}$ - Reset, PIN 32.

When taken low, all internal digital logic is reset. Upon returing high, a full calibration sequence is initiated which takes 34,584,480 master clock cycles to complete.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 19 and 24.

Analog input connections for the left and right input channels.

VREF - Voltage Reference, PIN 20.

The analog reference voltage which sets the analog input range. Its magnitude sets both positive and negative full-scale.

Digital Outputs

$\overline{\text{STBY}}$ - Standby (Calibrating), PIN 5.

Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

SDATA - Serial Output, PIN 15.

Presents each output data bit on a falling edge of the SCLK input. Data is valid to be latched on the rising edge of SCLK.

SSH1, SSH2 - Simultaneous Sample/Hold 1 and 2, PINS 10 and 11.

Used to control external sample/hold amplifier(s) to achieve simultaneous stereo sampling.

$\overline{\text{TRKL}}$, $\overline{\text{TRKR}}$ - Tracking Left, Tracking Right, PINS 8 and 9.

Indicate the end of a conversion cycle. Either $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ falls at the end of a conversion cycle depending on the status of L/$\overline{\text{R}}$ and which channel is to be tracked.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 21.

Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

NC - No Connection, PIN 4.

Must be left floating for proper operation.

$\overline{\text{TST1}}$, $\overline{\text{TST2}}$, $\overline{\text{TST3}}$, $\overline{\text{TST4}}$ - Test, PINS 17, 18, 26, 27.

Allow access to the CS5126's test functions which are reserved for factory use. Must be tied to VD+.

PARAMETER DEFINITIONS

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Dynamic Range - Full-scale Signal-to-Noise plus Distortion with the input signal 60dB below full-scale. Units in decibels.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's) after all offsets have been externally compensated. Units in decibels relative to full scale.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND). Units in microvolts.

Interchannel Mismatch - The difference in output codes between the left and right channels with the same analog input applied. Units expressed in decibels relative to full scale. Tested at full scale input.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

CRYSTAL
Semiconductor Corporation

CS5317

16-Bit, 20 kHz Oversampling A/D Converter

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track & Hold Amplifier
  - On-Chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

General Description

The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

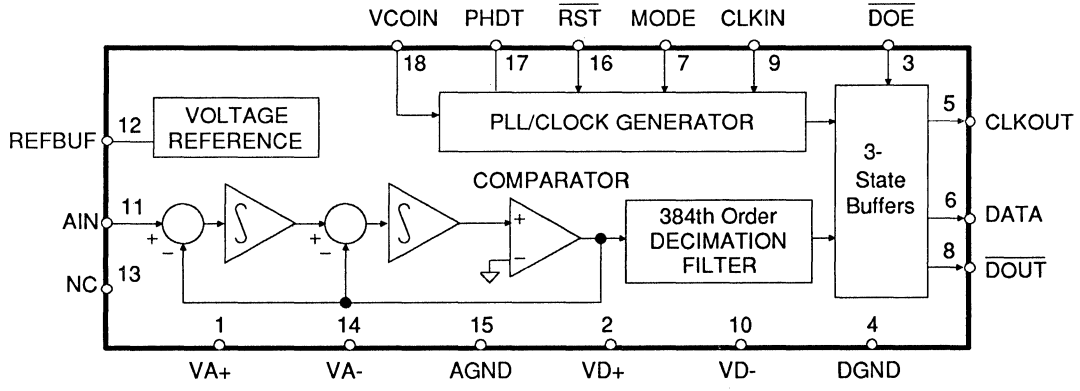
The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION: See page 3-190

3

Block Diagram



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS ($T_A = T_{MIN} - T_{MAX}$; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%; CLKIN = 4.9152 MHz in CLKOR mode; 1kHz Input Sinewave; with 1.2 kΩ, .01 µF antialiasing filter.)

Parameter*		CS5317-K min	CS5317-K typ	CS5317-K max	CS5317-B min	CS5317-B typ	CS5317-B max	CS5317-T min	CS5317-T typ	CS5317-T max	Units
Specified Temperature Range			0 to 70			-40 to +85			-55 to +125		°C
Resolution			16			16			16		Bits
Dynamic Performance											
Dynamic Range	(Note 1)		78	84		78	84		78	84	dB
Total Harmonic Distortion			72	80		72	80		72	80	dB
Signal to Intermodulation Distortion				84			84			84	dB
dc Accuracy											
Differential Nonlinearity	(Note 2)		±0.4			±0.4			±0.4		LSB
Positive Full-Scale Error			±150			±150			±150		mV
Positive Full-Scale Drift			±500			±500			±500		uV/°C
Bipolar Offset Error			±10			±10			±10		mV
Bipolar Offset Drift			±50			±50			±50		uV/°C
Filter Characteristics											
Absolute Group Delay	(Note 3)		78.125			78.125			78.125		us
Passband Frequency	(Note 4)		5			5			5		kHz
Input Characteristics											
AC Input Impedance (1kHz)			80			80			80		kohms
Analog Input Full Scale Signal Level			±2.75			±2.75			±2.75		V
Power Supplies											
Power Dissipation	(Note 5)		220	300		220	300		220	300	mW
Power Supply Rejection VA+	(Note 6)		60			60			60		dB
VA-			45			45			45		dB
VD+			60			60			60		dB
VD-			55			55			55		dB

Notes:
1. Measured over the full 0 to 9.6kHz band with a -20dB input and extrapolated to full-scale. Since this includes energy in the stopband above 5kHz, additional post-filtering at the CS5317's output can typically achieve 88dB dynamic range by improving rejection above 5kHz. This can be increased to 90dB by bandlimiting the output to 2.5kHz.
2. No missing codes is guaranteed by design.
3. Group delay is constant with respect to input analog frequency; that is, the digital FIR filter has linear phase. Group delay is determined by the formula D_{grp} = 384/CLKIN in CLKOR mode, or 192/CLKOUT in any mode.
4. The digital filter's frequency response scales with the master clock. Its -3dB point is determined by f_{-3dB} = CLKIN/977.3 in CLKOR mode, or CLKOUT/488.65 in any mode.
5. All outputs unloaded. All inputs CMOS levels.
6. With 300mV p-p, 1kHz ripple applied to each supply separately.

* Refer to the *Parameter Definitions* section after the Pin Description section.

ANALOG CHARACTERISTICS (Continued)

Parameter	CS5317-K min	CS5317-K typ	CS5317-K max	CS5317-B min	CS5317-B typ	CS5317-B max	CS5317-T min	CS5317-T typ	CS5317-T max	Units
Specified Temperature Range		0 to 70			-40 to +85			-55 to +125		°C
Phase-Lock Loop Characteristics					-4V < PHDT = VCOIN < 3V					
VCO Gain Constant, Ko (Note 7)	-4	-10	-30	-4	-10	-30	-4	-10	-30	M rad/Vs
VCO operating frequency	1.28		5.12	1.28		5.12	1.28		5.12	MHz
Phase Detector Gain Control, Kd	-5	-8	-12	-5	-8	-12	-5	-8	-12	ua/rad
Phase Detector Prop. Delay (Note 8)		50	100		50	100		50	100	ns

Notes: 7. Over 1.28 MHz to 5.12 MHz VCO output range, where VCO frequency = 2 * CLKOUT.
8. Delay from an input edge to the phase detector to a response at the PHDT output pin.

3

DIGITAL CHARACTERISTICS ($T_A = T_{MIN} - T_{MAX}$; VA+ , VD+ = 5V ±10%; VA-, VD- = -5V ±10%)

All measurements performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 9)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 9. I_{out}=-100µA. This specification guarantees the ability to drive one TTL load (V_{OH}=2.4V @ I_{out}=-40µA.).

RECOMMENDED OPERATING CONDITIONS (DGND, AGND = 0 V, see Note 10.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	5.5	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Master Clock Frequency		f_{clk}	0.01	-	5.12	MHz

Note: 10. All voltages with respect to ground.

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A=T_{MIN}-T_{MAX};C_L= 50 pF; VD+ = 5V ±10%;VD- = -5V ±10%)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency: CLKIN						
	CLKG1 Mode	f_{clkg1}	-	-	20	kHz
	CLKG2 Mode	f_{clkg2}	-	-	10	kHz
	CLKOR Mode	f_{clkor}	-	-	5.12	MHz
Output Word Rate: $\overline{DOUT}$		f_{dout}	-	-	20	kHz
Rise Times:	Any Digital Input	t_{risein}	-	20	1000	ns
	Any Digital Output	$t_{riseout}$	-	15	20	ns
Fall Times:	Any Digital Input	t_{fallin}	-	20	1000	ns
	Any Digital Output	$t_{fallout}$	-	15	20	ns
CLKIN Duty Cycle						
CLKG1 and CLKG2 Modes	Pulse Width Low	t_{pwl1}	200	-	-	ns
	Pulse Width High	t_{pwh1}	200	-	-	ns
CLKOR Mode	Pulse Width Low	t_{pwl1}	45	-	-	ns
	Pulse Width High	t_{pwh1}	45	-	-	ns
$\overline{RST}$ Pulse Width Low		t_{pwr}	400	-	-	ns
Set Up Times:						
	$\overline{RST}$ High to CLKIN High	t_{su1}	40	-	-	ns
	CLKIN High to $\overline{RST}$ High	t_{su2}	40	-	-	ns
Propagation Delays:						
$\overline{DOE}$ Falling to Data Valid		t_{phl1}	-	-	150	ns
CLKIN Rising to $\overline{DOUT}$ Falling	(Note 11)	t_{phl2}	-	1	-	CLKOUT cycles
$\overline{DOE}$ Rising to Hi-Z Output		t_{plh1}	-	-	80	ns
CLKOUT Rising to $\overline{DOUT}$ Falling		t_{plh2}	-	-	60	ns
CLKOUT Rising to $\overline{DOUT}$ Rising		t_{plh3}	-	-	60	ns
CLKOUT Rising to Data Valid		t_{plh4}	-	-	100	ns
CLKIN Rising to CLKOUT Falling	(Note 12)	t_{plh5}	-	-	200	ns
CLKIN Rising to CLKOUT Rising	(Note 12)	t_{plh6}	-	-	200	ns

Notes: 11. CLKIN only pertains to CLKG1 and CLKG2 modes.
12. Only valid in CLKOR mode.

ABSOLUTE MAXIMUM RATINGS (DGND, AGND = 0 V, all voltages with respect to ground.)

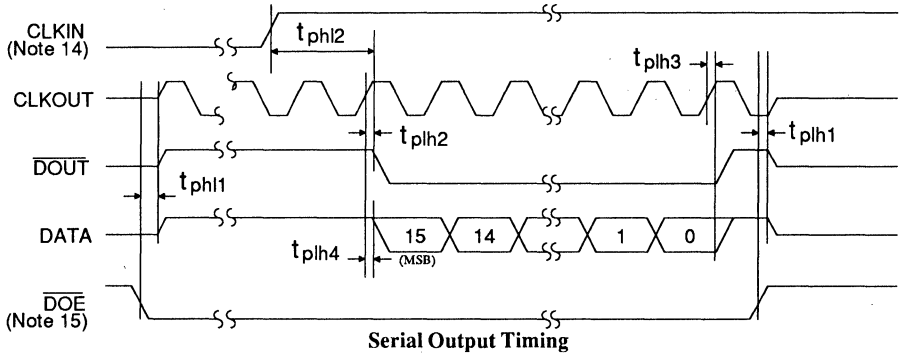
Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies	(Note 13)	I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VD+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 13. Transient currents up to 100mA will not cause SCR latch-up.

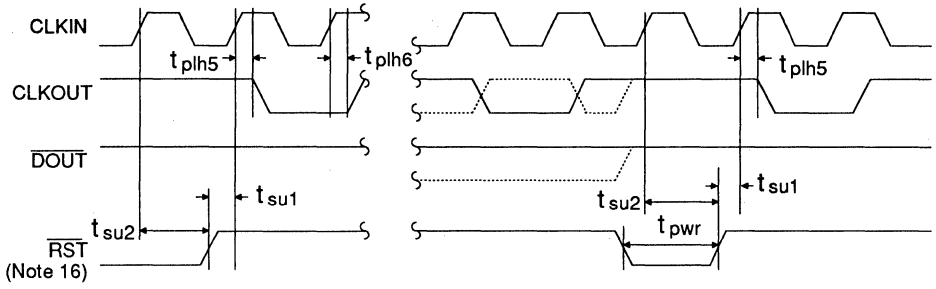
WARNING: Operating this device at or beyond these extremes may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

Rise and Fall Times

CLKIN Timing



Serial Output Timing



Reset Timing

Notes: 14. CLKIN only pertains to CLKG1 and CLKG2 modes.
15. If $\overline{DOE}$ is brought high during serial data transfer, CLKOUT, $\overline{DOUT}$, and DATA will immediately 3-state and the rest of the serial data is lost.
16. $\overline{RST}$ must be held high except in the clock override (CLKOR) mode where it can be used to align the phases of all internal clocks.

GENERAL DESCRIPTION

The CS5317 functions as a complete data conversion subsystem for voiceband signal processing. The A/D converter, sample/hold, voltage reference, and much of the antialiasing filtering are performed on-chip. The CS5317's serial interface offers its 16-bit, 2's complement output in a format which easily interfaces with industry-standard micro's and DSP's.

The CS5317 also includes a phase-locked loop that simplifies the converter's application in systems which require sampling to be locked to an external signal source. The CS5317 continuously samples its analog input at a rate set by an external clock source. On-chip digital filtering, an integral part of the delta-sigma ADC, processes the data and updates the 16-bit output register at up to 20 kHz. The CS5317 can be read at any rate up to 20 kHz.

The CS5317 is a CSZ5316 with an on-chip sampling clock generator. As such, it replaces the CSZ5316 and should be considered for all new designs. In addition, a CSZ5316 look-alike mode is included, allowing a CS5317 to be dropped into a CSZ5316 socket.

THEORY OF OPERATION

The CS5317 utilizes the delta-sigma technique of executing low-cost, high-resolution A/D conversions. A delta-sigma A/D converter consists of two basic blocks: an analog modulator and a digital filter.

Conversion

The analog modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog negative feedback loop with high open-loop gain. The modulator samples and converts the analog input at a rate well above the bandwidth of interest (2.5 MHz for the CS5317). The modulator's 1-bit output conveys information in the form of duty cycle. The digital filter then processes the 1-bit signal and extracts a high resolution output at a much lower rate (that is, 16-bits at a 20 kHz word rate with a 5 kHz input bandwidth).

An elementary example of a delta-sigma A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty-cycle), which is then filtered (averaged) by the counter for higher resolution. In comparison, the CS5317 uses a more sophisticated multi-order modulator and more powerful FIR filtering to extract higher word rates, much lower noise, and more useful system-level filtering.

Filtering

At the system level, the CS5317's digital filter can be modeled exactly like an analog filter with a few minor differences. First, digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially saturate the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5317's analog modulator and digital filter reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

An Application Note called "Delta Sigma Overview" contains more details on delta-sigma conversion and digital filtering.

SYSTEM DESIGN WITH THE CS5317

Like a tracking ADC, the CS5317 continuously samples and converts, always tracking the analog input signal and updating its output register at a 20 kHz rate. The device can be read at any rate to create any system-level sampling rate desired up to 20kHz.

Clocking

Oversampling is a critical function in delta-sigma A/D conversion. Although system-level *output* sample rates typically remain between 7kHz and 20kHz in voiceband applications, the CS5317 actually samples and converts the analog input at rates up to 2.56 MHz. This *internal* sampling rate is typically set by a master clock which is on the order of several megahertz. See Table1 for a complete description of the clock relationships in the various CS5317 operating modes.

Some systems such as echo-cancelling modems, though, require the *output* sampling rate to be locked to a sampling signal which is 20 kHz or below. For this reason the CS5317 includes an on-chip phase-lock loop (PLL) which can generate its requisite 5.12 MHz master clock from a 20 kHz sampling signal.

The CS5317 features two modes of operation which utilize the internal PLL. The first, termed *Clock Generation 1* (CLKG1), accepts a sampling clock up to 20 kHz at the CLKIN pin and internally generates the requisite 5.12 MHz clock. The CS5317 then processes samples updating its output register at the rate defined at CLKIN, typically 20 kHz. For a 20 kHz clock input the digital filter's 3 dB corner is set at 5.239 kHz, so *CLKG1 provides a factor of 2X oversampling at the system level* (20 kHz is twice the minimum possible sampling frequency needed to reconstruct a 5 kHz input). The CLKG1 mode is initiated by tying the MODE input to +5V.

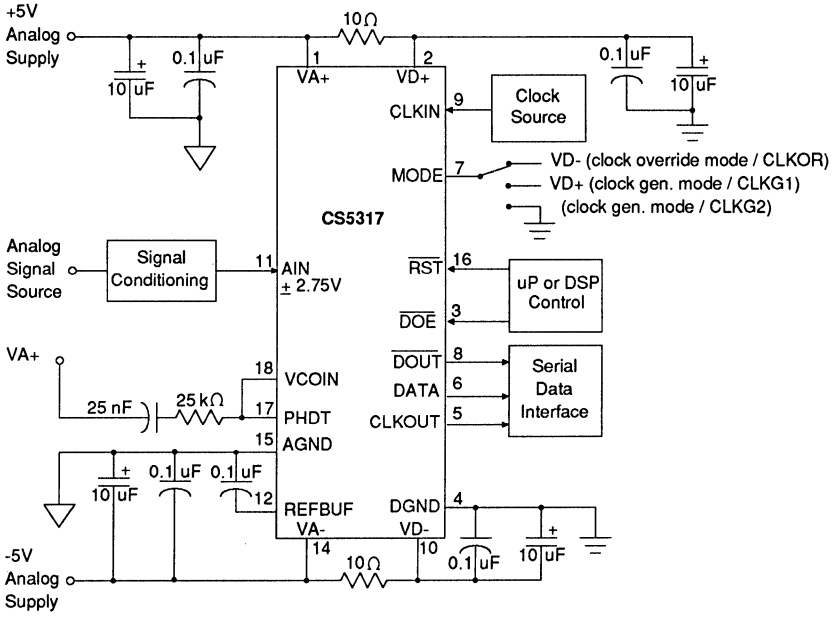


Figure 1. System Connection Diagram with Example PLL Components

Mode	Symbol	Mode Pin	RESET	Output Word Rate Provides System-level 2X Oversampling?	CLKIN (kHz)	CLKOUT f_{sin} (MHz)	$\overline{DOUT}$ f_{sout} (kHz)	F (kHz)	t_{dcD}* (ns)
Clock Gen. 2	CLKG2 CLKG2 CLKG2	0 V	HIGH	NO	7.2 9.6 10.0 (max)	1.8432 2.4576 2.56	7.2 9.6 10.0	14.4 19.2 20.0	542.5 406.9 390.6
Clock Gen. 1	CLKG1 CLKG1 CLKG1	+5 V	HIGH	YES	14.4 19.2 20.0 (max)	1.8432 2.4576 2.56	14.4 19.2 20.0	14.4 19.2 20.0	542.5 406.9 390.6
Clock Override	CLKOR CLKOR CLKOR	-5 V	SYNC	YES	3686.4 4915.2 5120.0 (max)	1.8432 2.4576 2.56	14.4 19.2 20.0	14.4 19.2 20.0	N/A N/A N/A
CSZ5316	CSZ5316	FSYNC	LOW	YES	5120.0 (max)	2.56	20.0	20.0	N/A

* t_{dcD} - Delay from CLKIN rising to $\overline{DOUT}$ falling = 1 CLKOUT cycle

Table 1. Mode Comparisons

The second PLL mode is termed *Clock Generation 2* (CLKG2) which generates its 5.12 MHz clock from a *10 kHz* external sampling signal. Again, output samples are available at the system sampling rate set by CLKIN, typically 10 kHz. For the full-rated 10 kHz clock CLKG2 still sets the filter's 3 dB point at 5 kHz. Therefore, *CLKG2 provides no oversampling* beyond the Nyquist requirement at the system level (10 kHz : 5 kHz) and its internal digital filter provides little anti-aliasing value. The CLKG2 mode is initiated by grounding the MODE pin.

The CS5317 features a third operating mode called *Clock Override* (CLKOR). Initiated by tying the MODE pin to -5V, CLKOR allows the 5.12 MHz master clock to be driven directly into the CLKIN pin. The CS5317 then processes samples updating its output register at $f_{clkin}/256$. Since all clocking is generated internally, the CLKOR mode includes a *Reset* capability which allows the output samples of multiple CS5317's to be synchronized.

The CS5317 also has a CSZ5316 compatible mode, selected by tying $\overline{RST}$ low, and using MODE (pin 7) as the FSYNC pin. See the CSZ5316 data sheet for detailed timing information.

Analog Design Considerations

DC Characteristics

The CS5317 was designed for signal processing. Its analog modulator uses CMOS amplifiers resulting in offset and gain errors which drift over temperature. If the CS5317 is being considered for low-frequency (< 10 Hz) measurement applications, Crystal Semiconductor recommends the CS5501, a low-cost, d.c. accurate, delta-sigma ADC featuring excellent 60 Hz rejection and a system-level calibration capability.

The Analog Input Range and Coding Format

The input range of the CS5317 is nominally ± 3V, with ± 250 mV possible gain error. Because of this gain error, analog input levels should be kept below ± 2.75V. The converter's serial output appears MSB-first in 2's complement format.

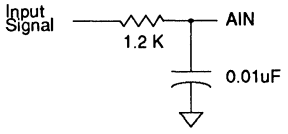
Antialiasing Considerations

In applying the CS5317, aliasing occurs during both the initial sampling of the analog input at $f_{s_{in}}$ (~2.5 MHz) and during the digital decimation process to the 16-bit output sample rate, $f_{s_{out}}$.

Initial Sampling

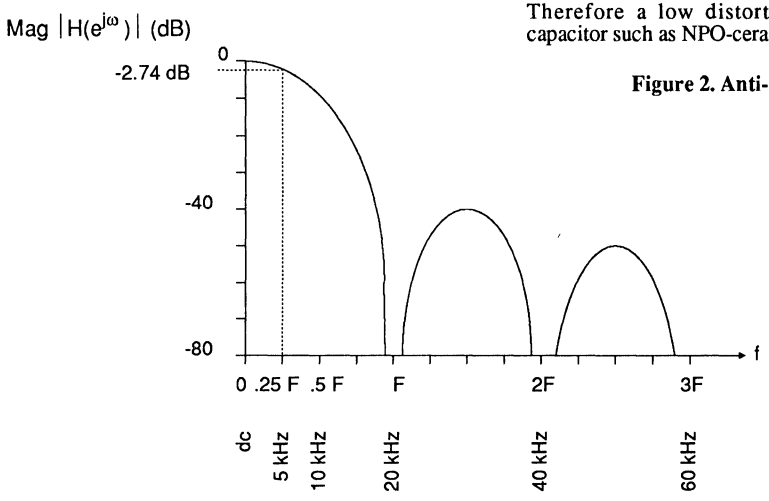
The CS5317 samples the analog input, AIN, at one-half the master clock frequency (~2.5 MHz max). The input sampling frequency, $f_{S_{in}}$, appears at CLKOUT regardless of whether the master clock is generated on-chip (CLKG1 and CLKG2 modes) or driven directly into the CS5317 (CLKOR mode). The digital filter then processes the input signal at the input sample rate.

Like any sampled-data filter, though, the digital filter's passband spectrum repeats around integer multiples of the sample rate, $f_{S_{in}}$. That is, when the CS5317 is operating at its full-rated speed any noise within ± 5 kHz bands around 2.5 MHz, 5 MHz, 7.5 MHz, etc. will pass unfiltered and alias into the baseband. Such noise can only be filtered by analog filtering *before the signal is sampled.* Since the signal is heavily oversampled (2.5 MHz : 5 kHz, or 500 : 1), a single-pole passive RC filter can be used as shown in Figure 2.



Note: Any nonlinearities contributed by this filter will be encoded as distortion by the CS5317. Therefore a low distortion, high frequency capacitor such as NPO-ceramic is recommended.

Figure 2. Anti-alias Filter



$\left| \left(\frac{\sin(128\pi fT)}{128\sin(\pi fT)} \right)^3 \right|$ = Magnitude where: T = $1/f_{sin}$

f_{sin} = input sampling frequency = CLKOUT frequency for all modes
= CLKIN/2 in CLKOR mode
= CLKIN*128 in CLKG1 mode
= CLKIN*256 in CLKG2 mode

F = $f_{sin}/128$ for all modes

f = input frequency

f_{sout} = $f_{sin}/128$ = output data rate for CLKOR & CLKG1 = F

f_{sout} = $f_{sin}/256$ = output data rate for CLKG2 = F/2

Examples:
For f_{sin} = 2.56 MHz at f = 5 kHz: Magnitude is -2.74 dB
For f_{sin} = 2.56 MHz at f = 10 kHz: Magnitude is -11.8 dB

Figure 3. CS5317 Low-Pass Filter Response

Decimation

Aliasing effects due to decimation are identical in the CLKOR and CLKG1 modes. Aliasing is different in the CLKG2 mode due to the difference in output sample rates (10 kHz vs. 20 kHz) and thus will be discussed separately.

Aliasing in the CLKOR and CLKG1 Modes

The delta-sigma modulator output is fed into the digital low-pass filter at the input sampling rate, fs_{in}. The filter's frequency response is shown in Figure 3. In the process of filtering the digitized signal the filter *decimates* the sampling rate by 128 (that is, $fs_{out} = fs_{in}/128$). In its most elementary form, decimation simply involves ignoring - or selectively reading - a fraction of the available samples.

In the process of decimation the output of the digital filter is effectively *resampled* at fs_{out}, the output word rate, *which has aliasing implications.* Residual signals *after filtering* at multiples of fs_{out} will alias into the baseband. For example, an input tone at 28 kHz will be attenuated by 39.9 dB. If fs_{out} = 20 kHz, the residual tone will alias into the baseband and appear at 8 kHz in the output spectrum.

If the input signal contains a large amount of out-of-band energy, additional analog and/or digital antialias filtering may be required. If digital post-filtering is used to augment the CS5317's rejection above $fs_{out}/4$ (that is, above 5 kHz), the filtering will also reject residual quantization noise from the modulator (see Appendix A). This will typically increase the converter's dynamic range to 88 dB. Further bandlimiting the digital output to $fs_{out}/8$ (2.5 kHz at full speed) will typically increase dynamic range to 90 dB.

Aliasing in the CLKG2 Mode

Aliasing effects in the CLKG2 mode can be modeled exactly as those in the CLKG1 mode with the output decimated by two (from 20 kHz to 10 kHz). This is most easily achieved by ignoring every other sample. In the CLKG2 mode the ratio of the output sampling rate to the filter's -3 dB point is two, with no oversampling beyond the demands of the Nyquist criterion. Without the ability to roll-off substantially before $fs_{out}/2$, the on-chip digital filter's antialiasing value is diminished.

The CLKG2 mode should therefore be used only when the output data rate must be minimized due to communication and/or storage reasons. In addition, adequate analog filtering must be provided prior to the A/D converter.

Digital Design Considerations

The CS5317 presents its 16-bit serial output MSB-first in 2's complement format. The converter's serial interface was designed to easily interface to a wide variety of micro's and DSP's. Appendix A offers several hardware interfaces to industry-standard processors.

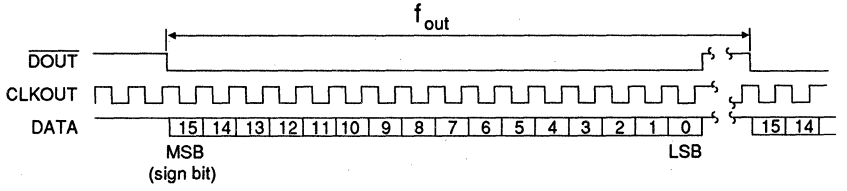


Figure 4. Data Output

Data Output Characteristics & Coding Format

As shown in Figure 4, the CS5317 outputs its 16-bit data word in a serial burst. The data appears at the DATA pin on the rising edge of the same CLKOUT cycle in which $\overline{DOUT}$ falls. Data changes on the rising edge of CLKOUT, and can be latched on the falling edge. The CLKOUT rate is set by the CLKIN input ($f_{clkin}/2$ in the CLKOR mode; $f_{clkin}*128$ in the CLKG1 mode; and $f_{clkin}*256$ in the CLKG2 mode). $\overline{DOUT}$ returns high after the last bit is transmitted. After transmitting the sixteen data bits, DATA will remain high until $\overline{DOUT}$ falls again, initiating the next data output cycle.

A 3-state capability is available for bus-oriented applications. The 3-state control input is termed Data Output Enable, $\overline{DOE}$, and is asynchronous with respect to the rest of the CS5317. If $\overline{DOE}$ is taken high at any time, even during a data burst, the DATA, $\overline{DOUT}$ and CLKOUT pins go to a high impedance state. Any data which would be output while $\overline{DOE}$ is high is lost.

Power Supplies

Since the A/D converter's output is digitally filtered in the CS5317, the device is more forgiving and requires less attention than conventional 16-bit A/D converters to grounding and layout arrangements. Still, care must be taken at the design and layout stages to apply the device properly. The CS5317 provides separate analog and digital power supply connections to isolate digital noise from its analog circuitry. Each supply pin should be decoupled to its respective ground, AGND or DGND. Decoupling should be accomplished with 0.1 µF ceramic capacitors. If significant low frequency noise is present in the supplies, 10 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5317 must never exceed the positive analog supply by more than a diode drop or the chip could be permanently damaged. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. Figure 1 shows a decoupling scheme which allows the CS5317 to be powered from a single set of ±5V rails. The digital supplies are derived from the analog supplies through 10 Ω resistors to prevent the analog supply from dropping below the digital supply.

PLL Characteristics

A phase-locked loop is included on the CS5317 and is used to generate the requisite high frequency A/D sampling clock. A functional diagram of the PLL is shown in Figure 5. The PLL consists of a phase detector, a filter, a VCO (voltage-controlled oscillator), and a counter/divider. The phase detector inputs are CLKIN (θ_1) and a sub-multiple of the VCO output signal (θ_2). The inputs to the phase detector are positive-edge triggered and therefore the duty cycle of the CLKIN signal is not significant. With this type of phase detector, the lock range of the PLL is equal to the capture range and is independent of the low pass filter. The output of the phase detector is input to an external low pass filter. The filter characteristics are used to determine the transient response of the loop. The output voltage from the filter functions as the input control voltage to the VCO. The output of the VCO is then divided in frequency to provide an input to the phase detector. The clock divider ratio is a function of the PLL mode which has been selected.

Phase Detector Gain (Kd)

A properly designed and operating phase-locked loop can be described using steady state linear analysis. Once in frequency lock, any phase difference between the two inputs to the phase detector cause a current output from the detector during the phase error. While either the +50 µA or the -50 µA current source may be turned on, the average current flow is:

$$i_{out\ avg} = Kd\ (\theta_1-\theta_2) \approx (-50\mu A/2\pi)\ (\theta_1-\theta_2)$$

where θ_1 is the phase of IN1, θ_2 is the phase of IN2 and Kd is the phase detector gain. The factor 2π comes from averaging the current over a full CLKIN cycle. Kd is in units of micro-amperes/radian.

VCO Gain (Ko)

The output frequency from the VCO ranges from 1.28 MHz to 5.12 MHz. The frequency is a function of the control voltage input to the VCO. The VCO has a negative gain factor, meaning that as the control voltage increases more positively the output frequency decreases. The gain factor units are Megaradians per Volt per Second. This is equivalent to 2π Megahertz per volt. Changes in output frequency are given by:

$$\Delta\omega_{VCO} = Ko\ \Delta VCO_{in} \quad [Ko \text{ is typ. } -10Mrad/Vs.]$$

Counter/Divider Ratio

The CS5317 PLL multiplies the CLKIN rate by an integer value. To set the multiplication rate, a counter/divider chain is used to divide the VCO output frequency to develop a clock whose frequency is compared to the CLKIN frequency in the phase detector. The binary counter/divider ratio sets the ratio of the VCO frequency to the CLKIN frequency. As illustrated in Figure 5, the VCO output is always divided by two to yield the CLKOUT signal which is identical in frequency to the delta-sigma modulator sampling clock. The CLKOUT signal is then further divided by either 128 in the CLKG1 mode or by 256 in the CLKG2 mode. When the divide by two stage is included, the divider ratio (N) for the PLL in the CLKG1 mode is effectively 256. In the CLKG2 mode the divider ratio (N) is 512.

Loop Transfer Function

As the phase-locked loop is a closed loop system, an equation can be determined which describes its closed loop response. Using the gain factors for the phase detector and the VCO, the filter arrangement and the counter/divider constant N, analysis will yield the following equation which describes the transfer function of the PLL:

$$\frac{\theta_2}{\theta_1} = \frac{\frac{Ko\ Kd\ R}{N}s + \frac{Ko\ Kd}{NC}}{s^2 + \frac{Ko\ KdR}{N}s + \frac{Ko\ Kd}{NC}}$$

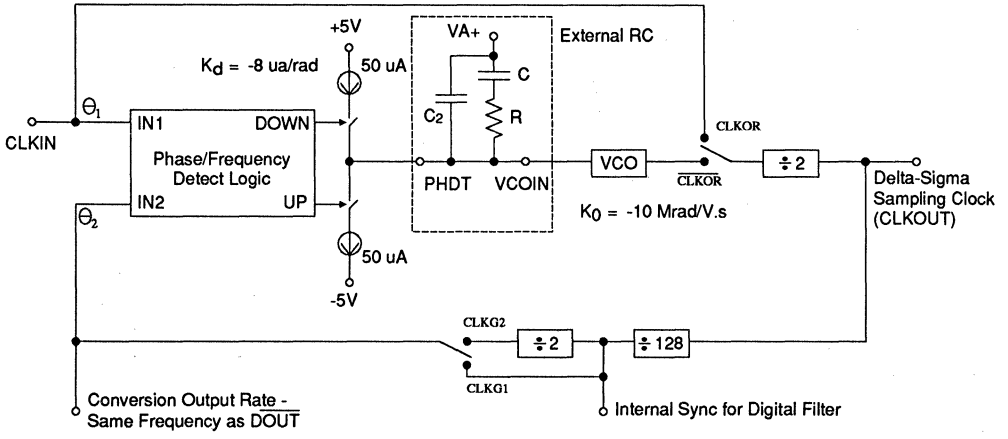


Figure 5. PLL Functional Diagram

This equation may be rewritten such that its elements correspond with the following characteristic form in which the damping factor, ζ, and the natural frequency, ω_n , are evident:

$$\frac{\theta_2}{\theta_1} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Both the natural frequency and the damping factor are particularly important in determining the transient response of the phase- locked loop when subjected to a step input of phase or frequency. A family of curves are illustrated in Figure 6 that indicate the overshoot and stability of the loop as a function of the damping factor. Each response is plotted as a function of the normalized time, $\omega_n t$. For a given ζ and lock time, t, the ω_n required can be determined. Alternatively, phase lock control loop bandwidth may be a specified parameter. In some systems it may be desireable to reduce the -3dB bandwidth of the PLL control loop to reduce the effects of jitter in the phase of the input clock. The 3 dB bandwidth of the PLL control loop is defined by the following equation:

$$\omega_{3dB} = \omega_n\sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

The equations used to describe the PLL and the 3 dB bandwidth are valid only if the frequency of CLKIN is approximately 20 times greater than the 3 dB corner frequency of the control loop.

Filter Components

Using the equations which describe the transfer function of the PLL system, the following external filter component equations can be determined:

$$C = \frac{KoKd}{N\omega_n^2}$$

$$R = 2\zeta\omega_n \frac{N}{KoKd}$$

The gain factors (Ko, Kd) are specified in the Analog Characteristics table. In the event the system calls for very low bandwidth, hence a corresponding reduction in loop gain, the phase detector gain factor Kd can be reduced. A large series resistor (R1) can be inserted between the output of the detector and the filter. Then the 50 µA current sources will saturate to the supplies and yield the following gain factor:

$$Kd \approx \frac{-5V}{2\pi R_1}$$

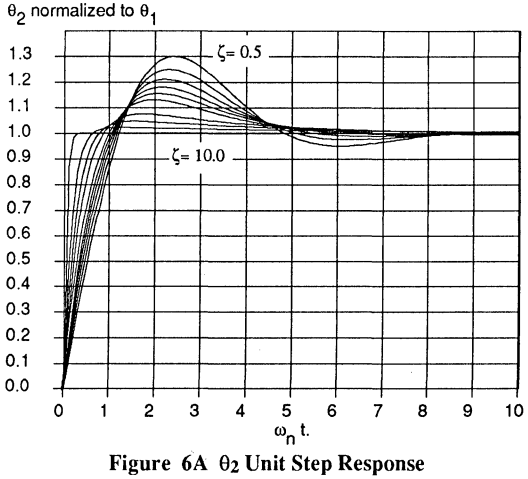


Figure 6A θ_2 Unit Step Response

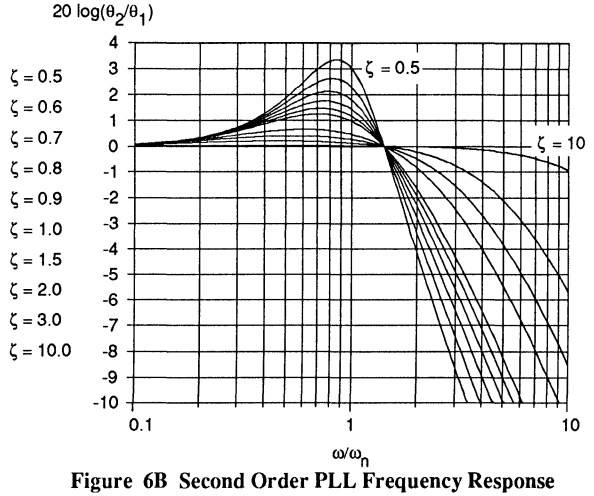


Figure 6B Second Order PLL Frequency Response

In some applications additional filtering may be useful to eliminate any jitter associated with the discrete current pulses from the phase detector. In this case a capacitor whose value is no more than 0.1 C can be placed across the RC filter network (C_2 in Figure 5).

Filter Design Example

The following is a step by step example of how to derive the loop filter components. The CS5317 A/D sampling clock is to be derived from a 9600 Hz clock source. The application requires the signal passband of the CS5317 to be 4 kHz. The on-chip digital filter of the CS5317 has a 3 dB passband of CLKOUT/488.65 (see Note 4 in the data sheet specifications tables). The 4 kHz passband requirement dictates that the sample clock (CLKOUT) of the CS5317 be a minimum of 4000 X 488.65 = 1.954 MHz. This requires the VCO to run at 3.908 MHz. The 3.908 MHz rate is 407 times greater than the 9600 Hz PLL input clock. Therefore the CS5317 must be set up in mode CLKG2 with N = 512. If the CLKG1 mode were used (N = 256), too narrow of a signal bandwidth through the A/D would result.

Once the operating mode has been determined from the system requirements, a value for the damping factor must be chosen. Figure 6 illustrates the dynamic aspects of the system with a given damping factor. Damping factor is generally chosen to be between 0.5 and 2.0. The choice of 0.5 will result in an overshoot of 30 % to a step response whereas the choice of 2.0 will result in an overshoot of less than 5 %. For example purposes, let us use a damping factor of 1.0.

So, let us begin with the following variables :

Ko = - 10 Mradians/volt.sec
Kd = - 8 μA/radian
N = 512
$\zeta = 1.0$

To calculate values for the resistor R and capacitor C of the filter, we must first derive a value for ω_n. Using the general rule that the sample clock should be at least 20 times higher frequency than the 3dB bandwidth of the PLL control loop:

$CLKIN \geq 20\ \omega_{3dB}$

where CLKIN = 9600 Hz $= 2\pi$ 9600 radians/sec.

So: $\omega_{3dB} = 2\pi\ 9600/20 = 3016$ radians/sec.

Knowing ω_{3dB} and the damping factor of 1.0, we can calculate the natural frequency, ω_n , of the control loop:

$$\omega_n = \omega_{3dB}/\sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

$$\omega_n = 3016/\sqrt{2(1)^2 + 1 + \sqrt{(2(1)^2 + 1)^2 + 1}}$$

$\omega_n = 1215$ 1/sec

Once the natural frequency, ω_n , is determined, values for R and C for the loop filter can be calculated:

$R = 2\zeta\omega_n N/KoKd$

R = 2(1) (1215 1/s) 512/(-10Mrad/v.s.)(-8 uA/rad)

R = 15552 v/A = 15.55 kΩ. Use R = 15 kΩ.

$C = KoKd/N\omega_n^2$

$C = (-10\ Mrad/v.s)(-\ 8\ \mu A/rad)/512\ (1215\ 1/s)^2$

$C = 105.8 \times 10^{-9}$ A.s/v = 105 nF. Use 0.1 uF.

The above example assumed typical values for Ko and Kd. Your application may require a worst case analysis which includes the minimum or maximum values. Table 2 shows some other example situations and R and C values.

CLKIN (Hz)	Mode	N	CLKOUT (MHz)	ζ	ω_{3dB}	ω_n	R * (kΩ)	C * (nF)
7200	CLKG2	512	1.8432	1.0	2262	911	11.6	187
9600	CLKG2	512	2.4576	1.0	3016	1215	15.5	106
14400	CLKG1	256	1.8432	1.0	4524	1822	11.6	94
19200	CLKG1	256	2.4576	1.0	6032	2430	15.5	52

* The values for R and C are as calculated using the described method. Component tolerances have not been allowed for. Notice that Ko and Kd can vary over a wide range, so using tight tolerances for R and C is not justified. Use the nearest conveniently available value.

Table 2 Example PLL Loop Filter R and C values

CS5317 PERFORMANCE

The CS5317 features 100% tested dynamic performance. The following section is included to illustrate the test method used for the CS5317.

FFT Tests and Windowing

The CS5317 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sine wave is applied to the CS5317 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins". Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5317.

If sampling is not synchronized to the input sinewave it is highly unlikely that the time record will contain an exact integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, removing the discontinuities. The effect of the "window" in the frequency domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used to test the CS5317 has a maximum side-lobe level of -92 dB.

Figure 7 shows an FFT plot of a typical CS5317 with a 1 kHz sinewave input generated by an "ultra-pure" sine wave generator and the output multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the

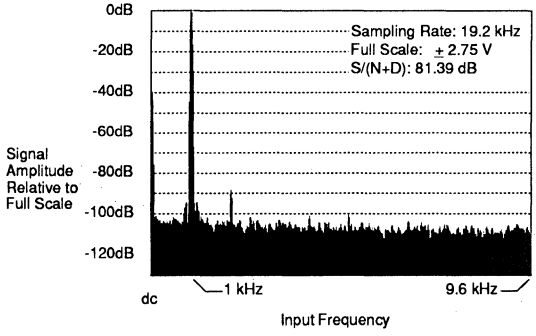


Figure 7. CS5317 Dynamic Performance

spectral variability that can arise from capturing finite time records, without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots.

Full-scale signal-to-noise-plus-distortion [S/(N+D)] is calculated as the ratio of the RMS power of the fundamental to the sum of the RMS power of the FFT's other frequency bins, which include both noise and distortion. For the CS5317, signal-to-noise-plus-distortion is shown to be better than 81 dB for an input frequency range of 0 to 9.6 kHz (fs/2).

Harmonic distortion characteristics of the CS5317 are excellent at 80 dB full scale signal to THD (typical), as are intermodulation distortion characteristics, shown in Figure 8. Intermodulation distortion results from the modulation distortion of two or more input frequencies by a non-linear transfer function.

DNL Test

Figure 9 shows a plot of the typical differential non-linearity (DNL) of the CS5317. This test is done by taking a large number of conversion results, and counting the occurrences of each code. A perfect A/D converter would have all codes of equal size and therefore equal numbers

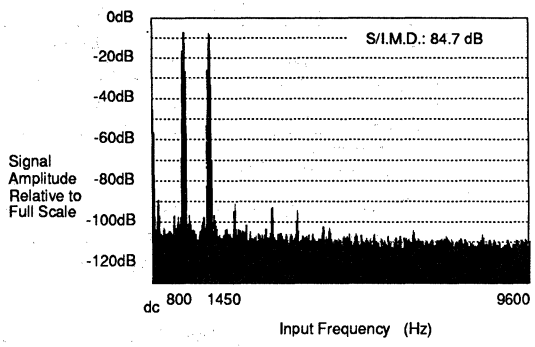


Figure 8. CS5317 Intermodulation Distortion

of occurrences. In the DNL test, a code with the average number of occurences is considered ideal and plotted as DNL = 0 LSB. A code with more or less occurrences than average will appear as a DNL of greater than or less than zero. A missing code has zero occurences, and will appear as a DNL of -1 LSB.

The plot below illustrates the typical DNL performance of the CS5317, and clearly shows the part easily achieves no missing codes.

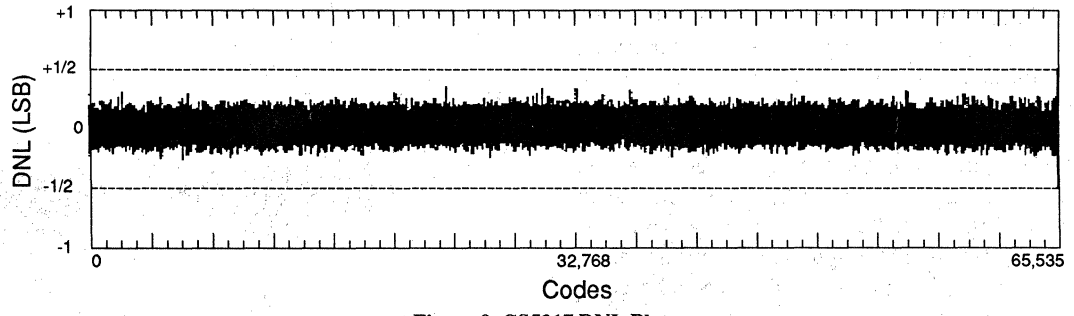
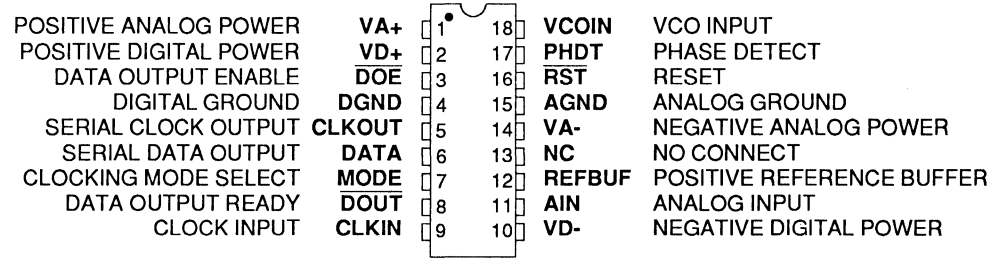


Figure 9. CS5317 DNL Plot

18 pin DIP Pinout



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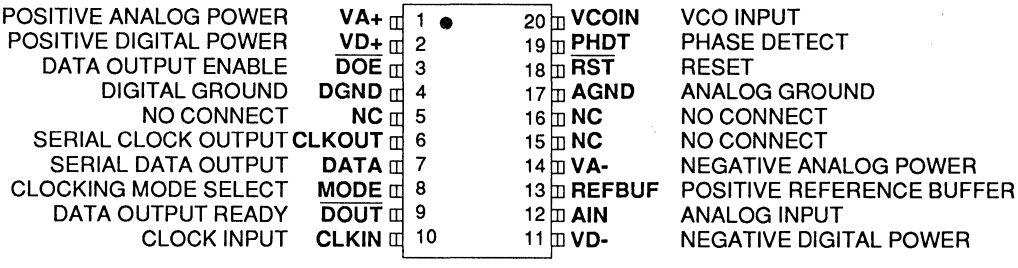
20 pin SOIC pinout



PIN DESCRIPTIONS (Pin numbers refer to the 18-pin DIP package)

Power Supplies

VD+ - Positive Digital Power, PIN 2.
Positive digital supply voltage. Nominally 5 volts.

VD- - Negative Digital Power, PIN 10.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 4.
Digital ground reference.

VA+ - Positive Analog Power, PIN 1.
Positive analog supply voltage. Nominally 5 volts.

VA- - Negative Analog Power, PIN 14.
Negative analog supply voltage. Nominally -5 volts.

AGND - Analog Ground, PIN 15.
Analog ground reference.

PLL/Clock Generator

CLKIN - Clock Input, PIN 9.
Clock input for both clock generation modes and the clock override mode (see MODE).

MODE - Mode Set, PIN 7.
Determines the internal clocking mode utilized by the CS5317. Connect to +5V to select CLKG1 mode. Connect to DGND to select CLKG2 mode. Connect to -5V to select CLKOR mode. This pin becomes equivalent to FSYNC in the CSZ5316 compatible mode.

VCOIN - VCO Input, PIN 18.
This pin is typically connected to PHDT. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

PHDT - Phase Detect, PIN 17.
This pin is typically connected to VCOIN. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

Inputs

AIN - Analog Input, PIN 11.

$\overline{\text{DOE}}$ - Data Output Enable, PIN 3.
Three-state control for serial output interface. When low, DATA, $\overline{\text{DOUT}}$, and CLKOUT are active. When high, they are in a high impedance state.

$\overline{\text{RST}}$ - Sample Clock Reset, PIN 16.
Sets phase of CLKOUT. Functions only in the clock override mode, CLKOR. Used to synchronize the output samples of multiple CS5317's. Must be kept high in CLKG1 or CLKG2 modes. Also, tying this pin low, with MODE not tied to - 5V, will place the CS5317 into CSZ5316 compatible mode.

Outputs

$\overline{\text{DOUT}}$ - Data Output Flag, PIN 8.
The falling edge indicates the start of serial data output on the DATA pin. The rising edge indicates the end of serial data output.

DATA - Data Output, PIN 6.
Serial data output pin. Converted data is clocked out on this pin by the rising edge of CLKOUT. Data is sent MSB first in two's complement format.

CLKOUT - Data Output Clock, PIN 5.
Serial data output clock. Data is clocked out on the rising edge of this pin. The falling edge should be used to latch data. Since CLKOUT is a free running clock, $\overline{\text{DOUT}}$ can be used to indicate valid data.

REFBUF - Positive Voltage Reference Noise Buffer, PIN 12.
Used to attenuate noise on the internal positive voltage reference. Must be connected to the analog ground through a 0.1µF ceramic capacitor.

3

PARAMETER DEFINITIONS

Resolution - The number of different output codes possible. Expressed as N, where 2^N is the number of available output codes.

Dynamic Range - The ratio of the largest allowable input signal to the noise floor.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics to the rms value of the largest allowable input signal. Units in dB's.

Signal to Intermodulation Distortion - The ratio of the rms sum of two input signals to the rms sum of all discernible intermodulation and harmonic distortion products.

Linearity Error - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in %FS.

Differential Nonlinearity - The deviation of a code's width from the ideal width. Units in LSB's.

Positive Full Scale Error - The deviation of the last code transition from the ideal, (VREF - 3/2 LSB). Units in mV.

Positive Full Scale Drift - The drift in effective, positive, full-scale input voltage with temperature.

Negative Full Scale Error - The deviation of the first code transition from the ideal, (-VREF + 1/2 LSB). Units in mV.

Negative Full Scale Drift - The drift in effective, negative, full-scale input voltage with temperature.

Bipolar Offset - The deviation of the mid-scale transition from the ideal. The ideal is defined as the middle transition lying on a straight line between actual positive full-scale and actual negative full-scale.

Bipolar Offset Drift - The drift in the bipolar offset error with temperature.

Absolute Group Delay - The delay through the filter section of the part.

Passband Frequency - The upper -3 dB frequency of the CS5317.

ORDERING GUIDE

Model Number	Temperature Range	Package
CS5317-KP	0 to 70°C	18 Pin Plastic DIP
CS5317-KS	0 to 70°C	20 Pin Plastic SOIC
CS5317-BD	-40 to +85°C	18 Pin Cer DIP
CS5317-TD	-55 to +125°C	18 Pin Cer DIP

APPENDIX A

APPLICATIONS

Figure A1 shows one method of converting the serial output of the CS5317 into 16-bit, parallel words. The associated timing is also shown.

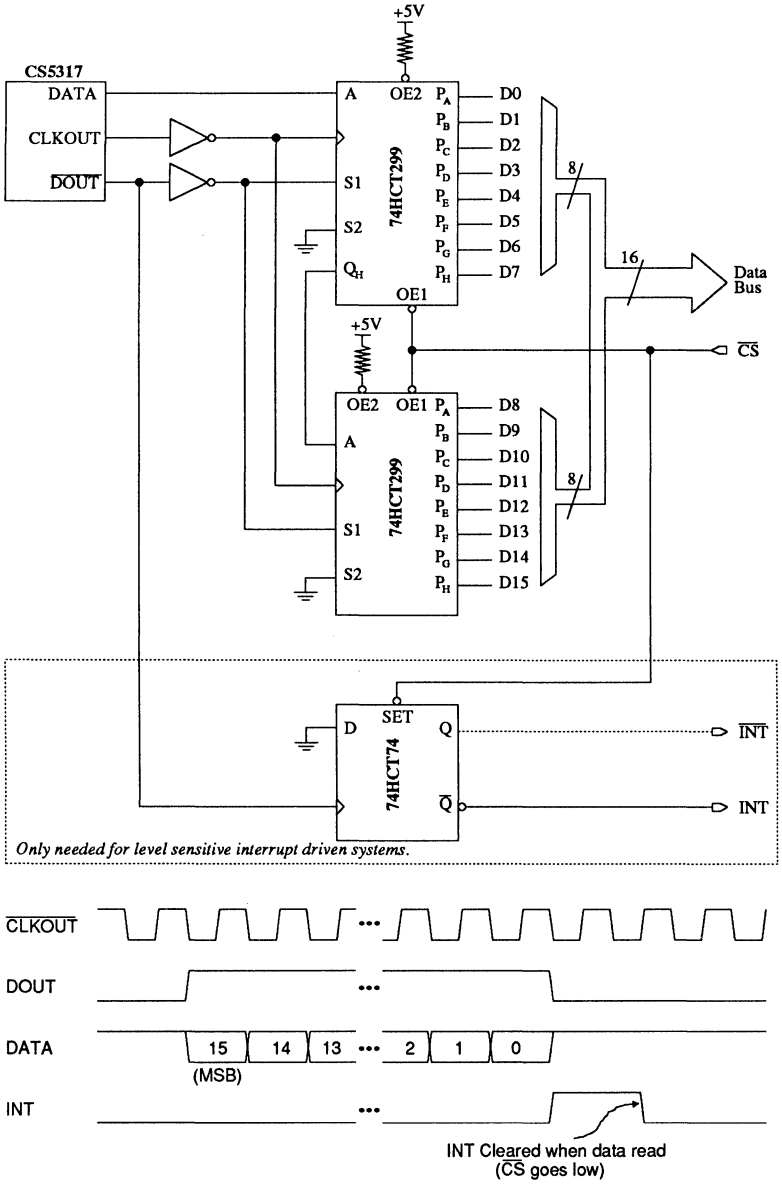


Figure A1. CS5317-to-Parallel Data Bus Interface

Figure A2 shows the interconnection and timing details for connecting a CS5317 to a NEC μPD7730 DSP chip.

Figure A3 shows the interconnection and timing details for connecting a CS5317 to a Motorola DSP 56000.

Status Register (SR)

Bit	Mnemonic	Setting	Meaning
9	SCI	0	External Clock
7, 6	SDLI	1, 0	16 bit data
3	SIF	0	MSB First

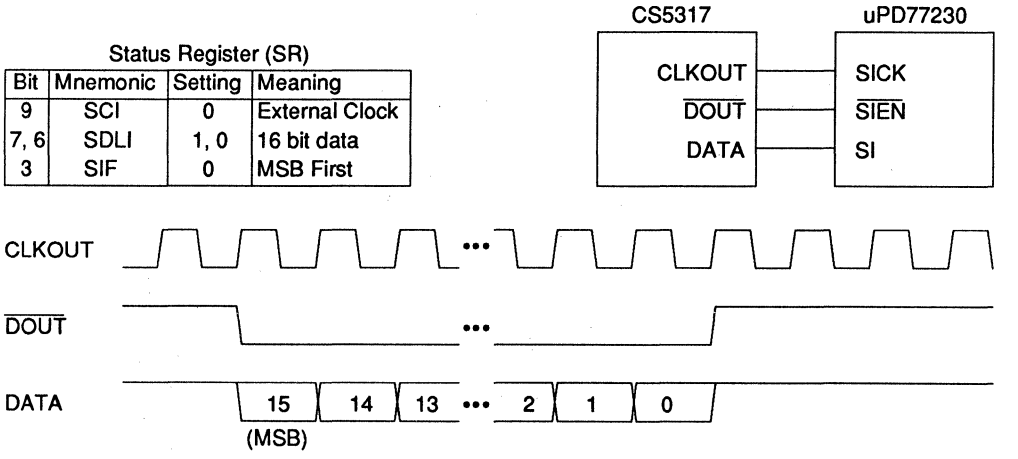


Figure A2. CS5317-to-NEC μPD77230 Serial Interface

SSI Control Reg. A CRA (X:FFEC)	
WL1 = 1, WL0 = 0	16 bits

	PINS	SYNC: CLKOUT / DOUT	SYNC: SCK / SC2	ASYNC: SC0 / SC1
SSI Control Reg. B CRB (X:FFED)	GCK		0	0
	SYN		1	0
	FSL		0	0
	SCKD		0	-
	SCD2		0	-
	SCD1		-	0
	SCD0		-	0

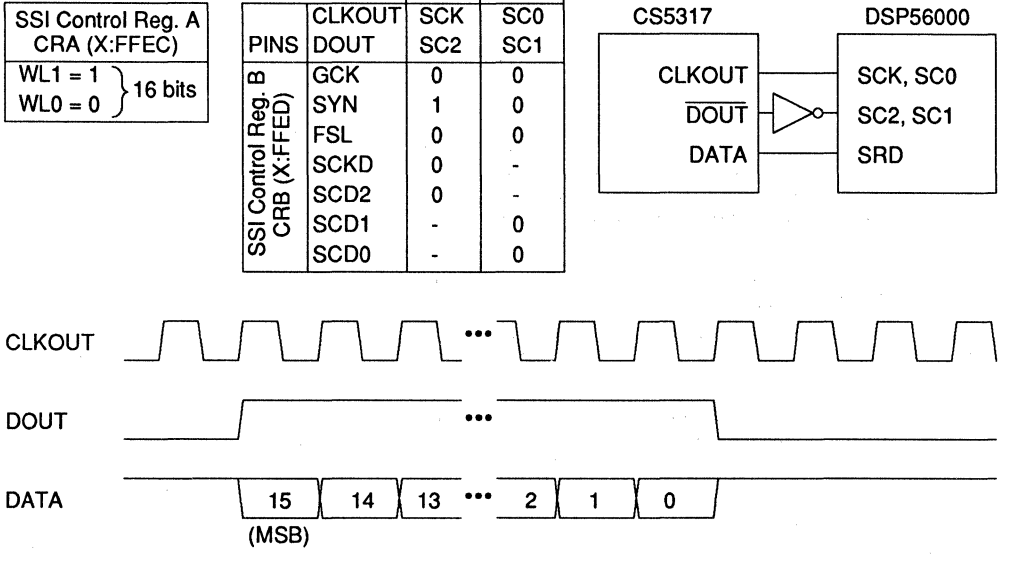


Figure A3. CS5317-to-Motorola DSP56000 Serial Interface

Figure A4 shows the interconnection and timing details for connecting a CS5317 to a WE DSP16 DSP chip.

Figure A5 shows the interconnection and timing details for connecting a CS5317 with TMS32020 and TMS320C25 DSP chips.

Serial I/O Control Register (SIOC)

Field	Value	Meaning
MSB	1	MSB input first
ILD	0	ILD is an input
ICK	0	ICK is an input
ILEN	0	16 bit input data

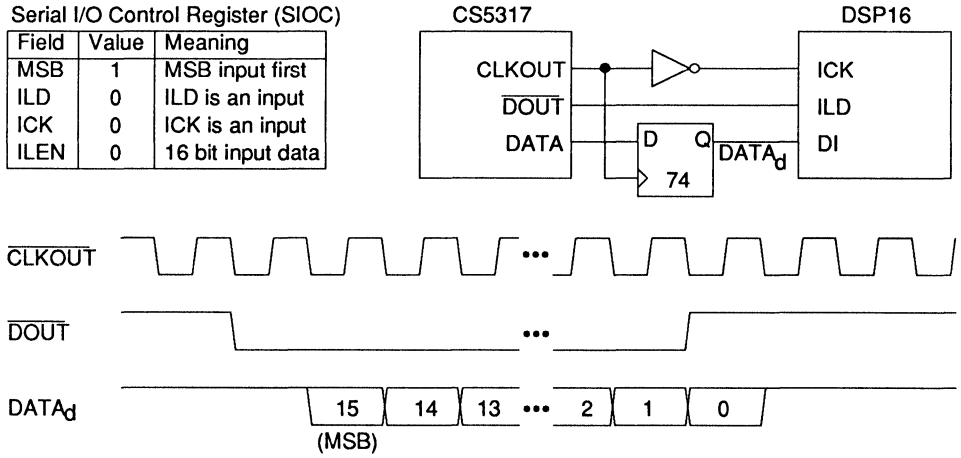


Figure A4. CS5317-to-WE DSP16 Serial Interface

TMS32020 Status Register (ST1):
F0 = 0 (16 bit data)
TMS320C25 Status Register (ST1):
F0 = 0 (16 bit data)
FSM = 1 (Frame Sync used)

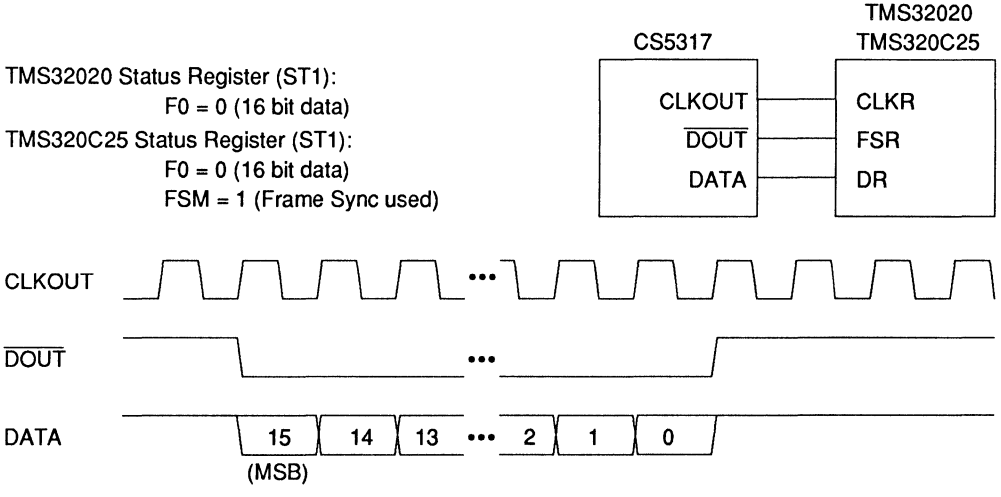


Figure A5. CS5317-to-TMS32020/TMS320C25 Serial Interface

•Notes•

Semiconductor Corporation

CS5322/CS5323

24-Bit Variable Bandwidth A/D Converter

Features

- Monolithic CMOS A/D Converter
- 100 dB Harmonic Distortion
- Delta-Sigma Architecture
  -Variable Oversampling: X32 to X4096
  -Internal Track-and-Hold Amplifier
- Flexible Filter Chip
  -Hardware or Software Selectable Options
  -Eight Selectable Filter Corner Frequencies: 23, 47, 94, 187, 375, 750, 1500 and 3000 Hz
- Low Power Dissipation

General Description

The CS5323 analog modulator and the CS5322 digital filter function together as a unique high resolution A/D converter intended for geophysical and other applications which require high dynamic range. The CS5323/CS5322 combination performs sampling, A/D conversion, and anti-alias filtering.

The pair use Delta-Sigma modulation to produce highly accurate conversions. The CS5323 oversamples, virtually eliminating the need for external anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of eight selectable update periods: 16, 8, 4, 2, 1, 0.5, 0.25 and 0.125 milliseconds. Data is output from the digital filter in a 24-bit serial format.

The CMOS design of the CS5322/CS5323 achieves high reliability while minimizing power dissipation. Power dissipation for the pair is less than 250 mW.

ORDERING INFORMATION

CS5322-BL -40 to +85 °C 28-pin PLCC
CS5323-BL -40 to +85 °C 28-pin PLCC

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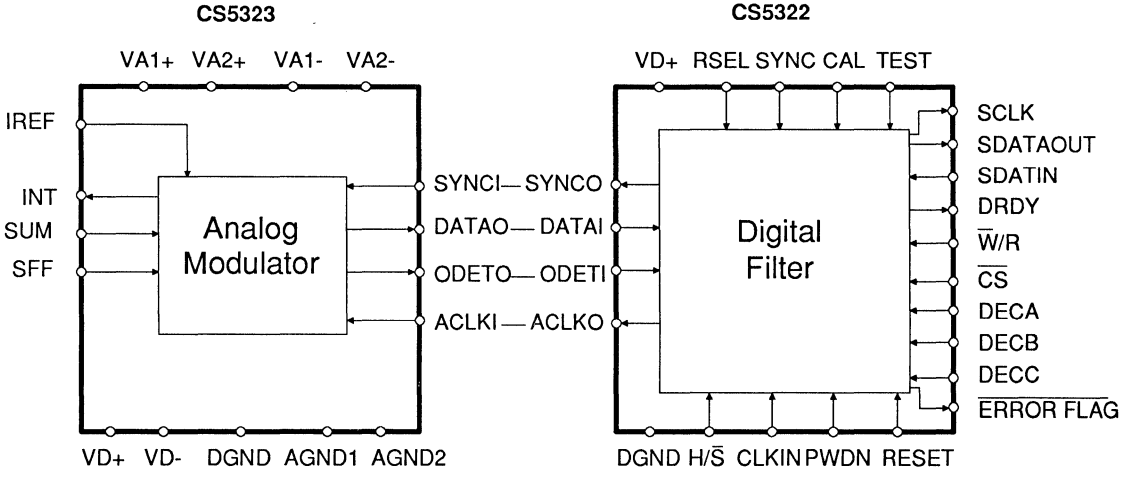

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

•Notes•

Semiconductor Corporation

CS5324

120 dB, 500 Hz Oversampling A/D Converter

Features

- Monolithic CMOS A/D converter
- 120dB Dynamic Range
- dc-500 Hz Bandwidth
- 110 dB Total Harmonic Distortion
- Internal Track-and-Hold Amplifier
- Delta-Sigma Architecture
  - —256X Oversampling
  - —Linear Phase Digital Filter
  - —Output Word Rate 32 kHz
- Low Power Dissipation: 180 mW max.
- Evaluation Board Available

General Description

The CS5324 analog to digital converter is a unique, very high resolution A/D converter intended for geophysical and sonar applications. It is a complete analog front end to a Digital Signal Processor and provides the DSP with a low distortion digital input suitable for precision signal analysis. The CS5324 performs sampling, A/D conversion, and anti-alias filtering.

The CS5324 uses delta-sigma modulation to produce highly accurate conversions. The device oversamples at 256X, virtually eliminating the need for external anti-aliasing filters. An on-chip linear-phase FIR digital filter decimates the output to a 32 kHz output word rate. Data is transmitted to the DSP as two, 8-bit bytes. An additional FIR filter in the DSP further decimates the signal to achieve 120 dB dynamic range over 500 Hz bandwidth with signal-to-distortion of 110 dB.

The CMOS design of the CS5324 ensures high reliability and power dissipation of less than 180 mW.

ORDERING GUIDE:

CS5324-KL	0° to 70°C	28-pin PLCC
CS5324-BL	-40° to +85°C	28-pin PLCC
CDB5324	Evaluation Board	

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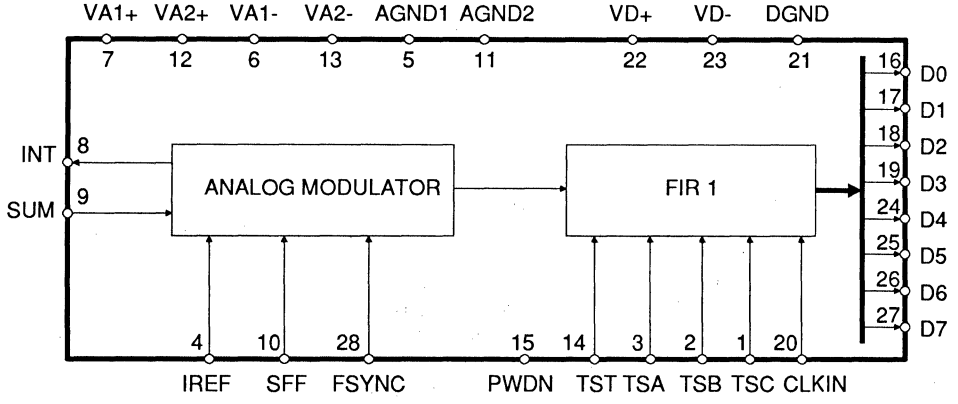
Block Diagram



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

ANALOG CHARACTERISTICS (T_A= 25°c ; VA-=-5V; VA+= 5V; AGND=0V;

CLKIN=1.024 MHz Device is connected as shown in Figure 9, the System Connection Diagram. Output data is further processed using off-chip filtering described in Appendix 1.)

Parameter*		Symbol	CS5324-K min	typ	max	CS5324-B min	typ	max	CS5324-T min	typ	max	Units
Specified Temperature Range			0	-	+70	-40	-	+85	-55	-	+125	°C
Dynamic Performance												
Dynamic Range		DR	-	120	-	-	120	-	-	TBD	-	dB
Signal-to-Distortion	(Note 1)	SDR	100	110	-	100	110	-	TBD	TBD	-	dB
Intermodulation Distortion	(Note 2)		-	110	-	-	110	-	-	TBD	-	dB
dc Accuracy												
Full Scale Error	(Note 3)		-	-	2	-	-	2	-	-	TBD	%
Full Scale Drift	(Note 3, 4)		-	0.003	0.006	-	0.003	0.006	-	0.003	TBD	%/ °C
Offset	(Note 3)		-	-	250	-	-	250	-	-	TBD	mV
Offset Drift	(Note 3, 4)		-	500	750	-	500	750	-	500	TBD	uV/ °C
Input Characteristics												
Input Signal Frequencies	(Note 5)	BW	dc	-	500	dc	-	500	dc	-	500	Hz
Input Voltage Range	(Note 6)	V_{IN}	-10.0	-	+10.0	-10.0	-	+10.0	-10.0	-	+10.0	V
Power Supplies												
DC Power Supply Currents												
IA+	(Note 7)		-	12.5	TBD	-	12.5	TBD	-	12.5	TBD	mA
IA-			-	14.5	TBD	-	14.5	TBD	-	14.5	TBD	mA
ID+			-	1.0	TBD	-	1.0	TBD	-	1.0	TBD	mA
ID-			-	0.6	TBD	-	0.6	TBD	-	0.6	TBD	mA
Power Dissipation												
PWDN Low	(Note 7)		-	150	180	-	150	180	-	150	180	mW
PWDN High			-	5	10	-	5	10	-	5	10	mW
Power Supply Rejection												
(dc to 500 Hz)	(Note 8)											
VA+			-	55	-	-	55	-	-	55	-	dB
VA-			-	45	-	-	45	-	-	45	-	dB
VD+			-	48	-	-	48	-	-	48	-	dB
VD-			-	38	-	-	38	-	-	38	-	dB
(500 Hz to 128 kHz)	(Note 9)											
VA+			-	60	-	-	60	-	-	60	-	dB
VA-			-	60	-	-	60	-	-	60	-	dB
VD+			-	50	-	-	50	-	-	50	-	dB
VD-			-	55	-	-	55	-	-	55	-	dB

Notes:
1. Tested with full scale input signal of 100 Hz.
2. Tested with input signals of 100 Hz and 140 Hz, each 6 dB down from full scale.
3. Specification is for the parameter over the specified temperature range and is for the CS5324 device only. It does not include the effects of external components.
4. Drift specifications are guaranteed by design and characterization.
5. The upper bandwidth limit is determined by the off-chip digital filter.
6. This input voltage range is for the configuration depicted in Figure 9, the System Connection Diagram.
7. All outputs unloaded. All logic inputs CMOS levels.
8. Tested with a 100 mVp-p 120 Hz sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).
9. Tested with a 100 mVp-p 120 kHz sine wave applied separately to each supply (VA1 and VA2 ard considered as one input for this test).

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA+,VD+=5V±5%; VA-, VD- =-5V±5%; Inputs: Logic 0 = 0V Logic 1 = VD+; C_L=50pF.)

Parameter			Symbol	Min	Typ	Max	Units
CLKIN Frequency		(Note 10)	f_c	0.9	1.024	1.1	MHz
CLKIN Duty Cycle				40	-	60	%
CLKIN Jitter				-	-	5	ps
Rise Times:	Any Digital Input Any Digital Output	(Note 11)	t_{rise}	- -	- 50	1.0 200	us ns
Fall Times:	Any Digital Input Any Digital Output	(Note 11)	t_{fall}	- -	- 50	1.0 200	us ns
CLKIN Rising edge to FSYNC Rising		(Note 12)	t_{cf}	70	-	-	ns
FSYNC Rising to CLKIN Falling Edge			t_{fc}	150	-	-	ns
Output Data Delay: CLKIN Rising to Valid Data			t_{dd}	-	200	TBD	ns
Output Float Delay: CLKIN Rising to Hi-Z			t_{fd}	-	150	TBD	ns

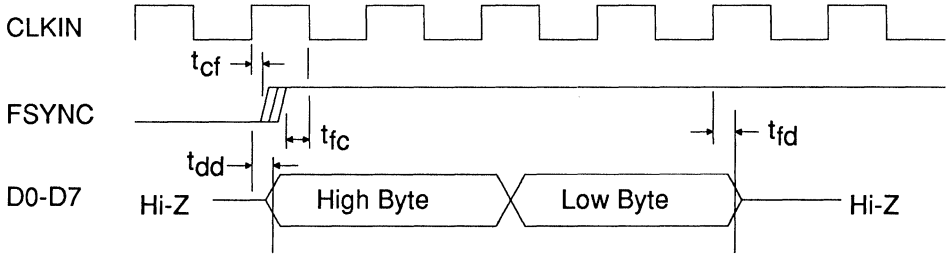
Notes: 10. If CLKIN is removed the device will enter the power down mode.
11. Excludes CLKIN input. CLKIN should be driven with a signal having rise and fall times of 25ns or faster.
12. Only the rising edge of FSYNC relative to CLKIN is used to sychronize the device. FSYNC can return low at any time as long as it remains high for at least one CLKIN cycle.

DIGITAL CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA+,VD+ = 5V±5%; VA-,VD- = -5V±5%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	(VD+) - 1.0V	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	1.0	V
High-Level Output Voltage I_{OUT} = -600 uA (Note 13)	V_{OH}	(VD+) - 0.4V	-	-	V
Low-Level Output Voltage I_{OUT} = 800 uA (Note 13)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{LKG}	-	-	10	uA
Tri-State Leakage Current	I_{OZ}	-	-	10	uA
Digital Output Pin Capacitance	C_{OUT}	-	9	-	pF

Notes: 13. The device is designed for low current output drive to minimize induced noise. CMOS interfacing is highly recommended.



Digital Timing Relationships

RECOMMENDED OPERATING CONDITIONS (DGND=0V; AGND=0V. All voltages measured with respect to ground.)

Parameter	Symbol	Min	Typ	Max	Units
DC Supply					
Positive Analog	VA+	4.75	5.0	5.25	V
Negative Analog	VA-	- 4.75	- 5.0	- 5.25	V
Positive Digital	VD+	4.75	5.0	5.25	V
Negative Digital	VD-	- 4.75	- 5.0	- 5.25	V

ABSOLUTE MAXIMUM RATINGS (DGND=0V; AGND=OV. All voltages measured with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	- 0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	- 6.0	V
	Positive Analog	VA+	- 0.3	6.0	V
	Negative Analog	VA-	0.3	- 6.0	V
Input Current, Any Pin Except Supplies (Note 14)		I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	- 0.3	(VA+) + 0.3	V
Ambient Operating Temperature		T_A	- 55	125	°C
Storage Temperature		T_{stg}	- 65	150	°C

Note: 14. Transient currents up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

General Description

The CS5324 is a monolithic CMOS A/D converter designed specifically for very high resolution measurement of signals between dc and 500 Hz. The device consists of a fourth-order delta-sigma modulator followed by an on-chip digital decimation filter.

The modulator of the CS5324 samples the analog input signal at a 256X oversampling rate. This high oversampling rate, along with subsequent digital filtering, enables the CS5324 to achieve a dynamic range which exceeds 120 dB. To achieve optimum performance, the CS5324 uses off-chip circuitry to develop the reference and operating currents necessary to set the gain and offset of the modulator portion of the A/D converter. Discrete components are also used for the first stage integrator input resistor and integration capacitor.

The CS5324 performs conversions continuously and outputs twelve data bits for further data decimation by an off-chip digital filter. A separate DSP chip can be utilized to perform the off-chip filtering. A single DSP chip can perform the filter function for several CS5324 devices. For this reason, the CS5324 was designed to output its data in a simple time-division multiplexing (TDM) format. This TDM architecture allows up to eight CS5324 devices to share the same data bus.

Theory of Operation

The CS5324 utilizes a fourth order oversampling delta-sigma architecture to achieve high-resolution A/D conversion. The converter consists of an analog modulator, along with an on-chip digital decimation filter. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The first stage of the fourth order modulator uses discrete components external to the chip to maximize signal performance relative to noise.

The modulator samples at 256 kHz (CLKIN = 1.024 MHz) which is 256X oversampling above two times the maximum signal frequency of 500 Hz. The modulator output is followed by a decimate by 8, fourth-order (sinx)/x filter. The result from this filter is a 12-bit word which is output from the chip at a 32 kHz rate. The 12-bit data is then further filtered by means of an off-chip digital filter. The off-chip filter can be implemented by either a DSP chip or an ASIC designed for this purpose. The exact characteristics of the on-chip filter and some recommended off-chip digital filters are discussed under the Filter Characteristics section of the data sheet. Upon reduction with the off-chip filtering, the data results in resolution which exceeds 20-bits. The final result yields a dynamic range exceeding 120 dB.

The architecture of the CS5324 was chosen to maximize performance. The input integrator uses off-chip discrete components. The chip is designed to use a current-source type reference, rather than a voltage source to minimize noise. In addition, the amount of on-chip digital filtering is minimized to reduce the possibility of the digital noise of the filter coupling into the analog sections of the chip. Configuring the chip to use additional off-chip digital filtering also allows the user maximum flexibility in implementing a filter appropriate to his system requirements.

Signal Input and Current Reference

The CS5324 uses a number of external discrete components to achieve maximum performance. Figure 1 illustrates the recommended circuit configuration for the current reference components and for the signal input components.

The CS5324 is designed to use a current reference of 2 mA into the IREF pin. A current reference rather than a voltage reference was chosen to achieve better noise performance. For optimum performance the dc source impedance at the IREF pin should be approximately 5 kΩ. This

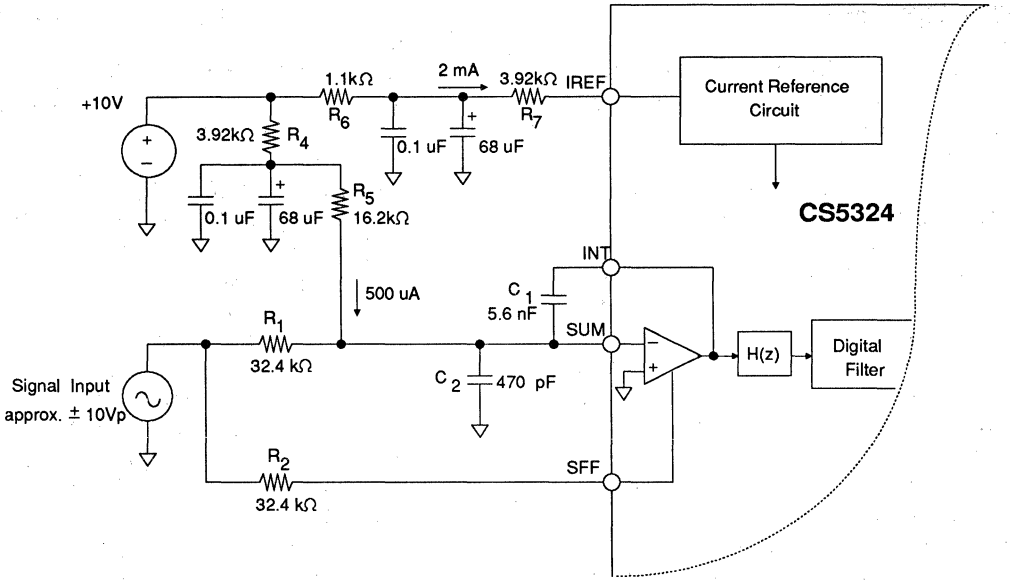


Figure 1. Signal Input and Current Reference Circuitry

calls for a 10 volt source driving the 5 kΩ (R_6+R_7) resistor to achieve the desired 2 mA current source. The IREF input sets the full scale gain of the A/D converter.

To properly bias the input integrator to a midrange operating point, a current source 1/4 the size of the IREF input current must be sourced into the integrator summing junction at the SUM pin. This requires a 20 kΩ resistance (R4+R5) be placed from the 10 V reference to the SUM pin.

Both the 2 mA IREF current and the 500 µA sources have capacitive filtering to aid in reducing the broadband current noise from the voltage reference. These capacitors should be of quality construction. Particular attention should be paid to leakage current variation over the desired operating temperature, as this leakage will affect the system gain.

The signal input pin (SUM) of the CS5324 is the summing junction of the input integrator stage. This integrator is designed to use an external input resistor (R_1) and integrating capacitor (C_1). In addition, a capacitor (C_2) is required at this node for proper phase compensation. The size of the input resistor (R_1) is determined by the magnitude of the signal current. With a maximum input voltage into the resistor, the integrator input current must be set equal to approximately 0.15 the current value injected into the IREF pin. With a 2 mA IREF current, the full scale signal current should be about 300 µA. Additionally, to minimize current noise into the summing junction, the value of the effective input resistance should be above 8 kΩ. Using a 32.4 kΩ resistor for R_1 sets the full scale input voltage into the integrating resistor to a value near 10 volts. The input signal then spans 20 V_{p-p}.

Once the integrator input resistor is chosen, the integrator capacitor can be determined. The resistor and capacitor combination should yield a frequency ($f = 1/(2 \pi R_1 C_1)$) between 800 and 900 Hz to achieve maximum performance. This yields a capacitor value near 5.6 nF. The capacitor should be chosen for minimum leakage, mini-

	D7	D6	D5	D4	D3	D2	D1	D0
Hi Byte	B11	B10	B9	B8	B7	B6	B5	B4
Lo Byte	B3	B2	B1	B0	0	OF	UF	ORST

Data is 2's complement with B11 as sign bit

Figure 2. Output Data Format

mum dielectric absorbtion, and minimum voltage coefficient of capacitance. While a teflon foilwrap capacitor is preferred, high quality film capacitors may be acceptable in many applications.

The CS5324 has a second signal input pin called the Signal Feedforward (SFF) pin. The signal into this pin bypasses the input stage of the input integrator, improving signal performance in the passband. The resistor (R_2) used at this input should be identical in value and performance characteristics to the input resistor (R_1).

Digital Output and Data Format

For proper operation the CS5324 must be provided with a CMOS-compatible clock into the CLKIN pin. The normal operating frequency is 1.024 MHz. This clock determines the input sample rate and the output word rate of the converter. The sample rate is CLKIN/4 while the output word rate is at CLKIN/32.

The CS5324 will compute a 12-bit output word at a 32 kHz rate (CLKIN = 1.024 MHz). The data is output from Data Output pins D7-D0 in the form of two eight bit bytes. The first byte is the high order byte with the MSB in the D7 position. The second 8-bit byte is the low order byte, and includes three status bits and an unused bit. The data is in two's complement format. Figure 2 illustrates the format of the output data.

Input Signal	Output Code
approx. +16 V	0111 1111 1111
+F.S. - 1.5 LSB (approx.+10 V)	0101 0000 0000
0V	0000 0000 0000
-F.S. + 0.5 LSB (approx. -10 V)	1011 0000 0000
approx. -16 V	1000 0000 0000

Notes: 1. Output codes from the on-chip digital filter will typically exhibit ±50 LSB's of noise (p-p).
2. Table depicts output codes for circuit configuration of Figure 9.

Table 1. Output Coding

For 12-bit two's complement data the codes range from -2048 to +2047. The output codes from the CS5324 will range from approximately -1280 to +1280 for a full scale sine wave input into the converter as shown in Table 1. There may be typically ±50 codes of noise (p-p) on the data in the 12-bit data output. Off-chip digital filtering is required to achieve the full dynamic range capability of the CS5324.

Status Bits

Three status bits are output from the CS5324. The three status bits are overflow, underflow, and oscillation reset. The overflow and underflow status bits indicate whenever the digital filter accumulator results in an overflow or underflow condition. With the present on-chip digital filter, the underflow condition will never occur. The overflow bit will go high indicating an accumulator overflow only if the input signal to the converter exceeds positive full scale by approximately 1.6X. Upon overflow, the accumulator will contain the value +2047 (or 2048 after underflow). The oscillation reset status bit indicates that output data may be in error. An oscillation detection circuit monitors the modulator loop to see if it is operating within its stable operating range. If the modulator is operat-

ing outside its normal operating range the output data may be corrupted. The ORST status bit may go high as a result of power-up, or, if the input signal exceeds the specified full scale input value. If ORST does occur, it will remain high for a total of four update cycles (of 32 kHz) to the output port, while the modulator and the digital filter are reset. Once ORST goes back low, output data will not be valid until the modulator and the digital filter(s) settle.

Initialization and Output Data Sequencing

The CS5324 updates its output register at a 32 kHz rate (CLKIN = 1.024 MHz). Between updates 32 CLKIN cycles occur. The CS5324 is designed such that eight data output time slots occur during these 32 CLKIN cycles. Each time slot lasts for 4 CLKIN cycles. The CS5324 is designed to allow eight devices to share the same 8-bit data bus when each device is set-up to output its data in an individual time slot. The exact time the CS5324 will output data is determined by the TSA, TSB, TSC, and FSYNC inputs. After power is applied to the devices, the FSYNC input must be brought high. When FSYNC is brought high (within the required timing specifications), each chip will be assigned to a data output time slot according to the logic levels of its TSA, TSB, and TSC inputs. Table 2 tabulates the decoding of these inputs.

TSA	TSB	TSC	Time Slot
0	0	0	TS0
0	0	1	TS1
0	1	0	TS2
0	1	1	TS3
1	0	0	TS4
1	0	1	TS5
1	1	0	TS6
1	1	1	TS7

Table 2. Time - Slot Decoding

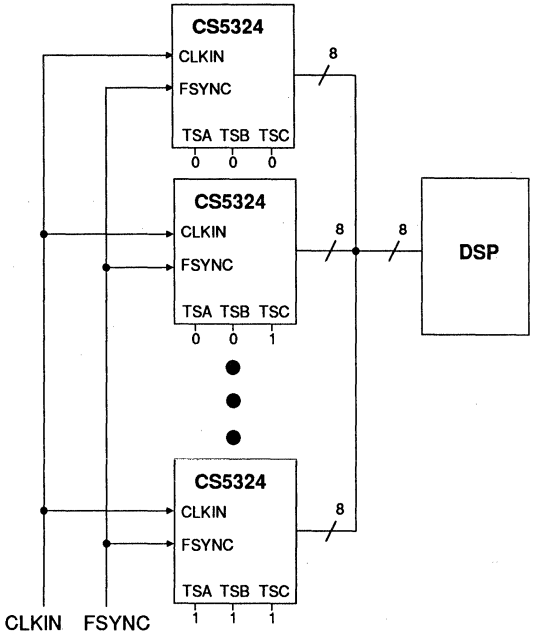
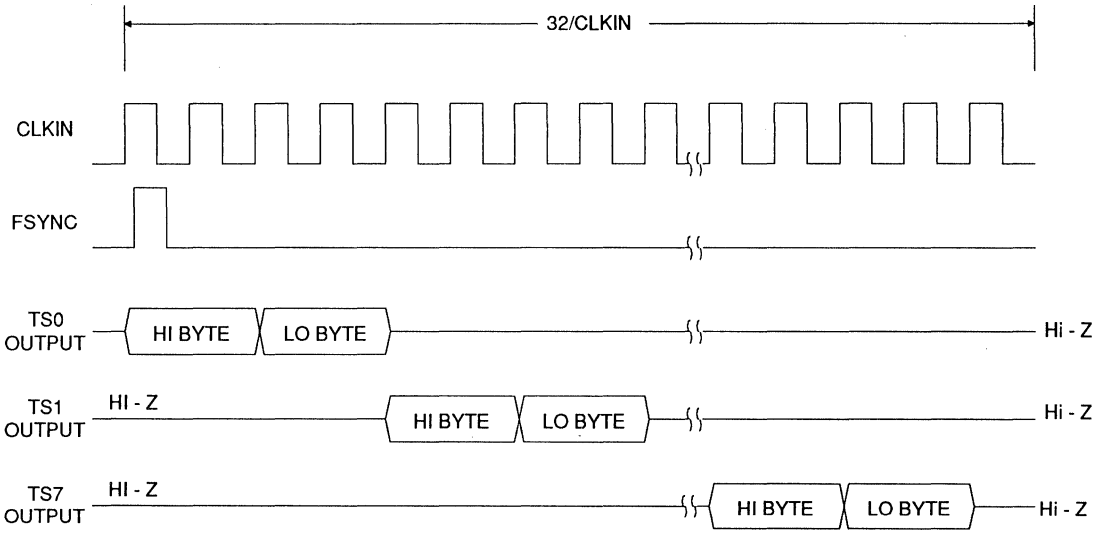


Figure 3. Multiple CS5324 to DSP Interface.

If all the CS5324s in the system are initialized with the same FSYNC signal, they will all compute filter results in phase with each other and update their output registers at the same time. Only the time slot in which the data is output from the devices is different.

The FSYNC signal used to intialize the CS5324 need only be activated once after power up. In some systems, it may be preferable to have this signal occur every 32 CLKIN cycles. Only the occurance of the rising edge of FSYNC is significant in determining the system intialization. Figure 3 illustrates a system configuration using multiple CS5324s interfaced to the same DSP chip.

Four cycles of CLKIN occur during each time slot. During the time slot designated for a CS5324 to output its data, the high-order byte



Note: UP to eight A/D converters can share the same digital output bus as long as each converter is assigned to put out its data in a different time slot with respect to all other converters on the bus.

Figure 4. Data Output Sequence for Multiple CS5324s.

will be output for the first two CLKIN cycles of the time slot. The second byte will be output during the last two CLKIN cycles of the period.

If four or less CS5324's share the same data bus, it is preferable to use alternate time slots (i.e. TS0, TS2, TS4, TS6) to minimize the possibility of bus contention problems. Slight timing differences between chips may result in timing overlap if adjacent time slots are used.

Filter Characteristics

The CS5324 utilizes a fourth-order delta-sigma modulator which has superb linearity. The full capability of the A/D conversion block can be obtained with an appropriate digital filter. Many applications, (seismic applications in particular) require the A/D conversion function to accurately reproduce the pulse shape of the input signal waveform, not just the spectral content. To accurately digitize the shape of the input signal requires a linear phase response in the signal processing system. Any non-linearities in the phase response of the signal processing system will corrupt the true waveshape information. For this reason, the design of the digital filtering to be used with the CS5324 should include particular attention to the phase characteristics of the filter function.

While the on-chip filter is fixed in its characteristics, the off-chip filter will be defined by the system requirements of the particular application. A low pass filter specification to be used with the CS5324 will include the following parameters: Passband ripple (or flatness); group delay or phase characteristics; transition band rolloff; stop band rejection; and filter complexity. All of these parameters are interrelated in any given filter design. There is no one particular solution to be used with the CS5324.

The CS5324 samples the input signal at 256 kHz (CLKIN = 1.024 MHz). With a signal bandwidth

$$X(z) = \sum_{n=0}^{28} h(n+1)\, z^{-n}$$

Coefficient			Value
h(1)	=	h(29)	1.00
h(2)	=	h(28)	4.00
h(3)	=	h(27)	10.00
h(4)	=	h(26)	20.00
h(5)	=	h(25)	35.00
h(6)	=	h(24)	56.00
h(7)	=	h(23)	84.00
h(8)	=	h(22)	120.00
h(9)	=	h(21)	161.00
h(10)	=	h(20)	204.00
h(11)	=	h(19)	246.00
h(12)	=	h(18)	284.00
h(13)	=	h(17)	315.00
h(14)	=	h(16)	336.00
h(15)			344.00

Table 3. On-chip Filter Coefficients

of 500 Hz, the output data rate from the A/D system (including the off-chip digital filtering) need only be 1 kHz to adequately represent the input signal. For this reason, it is desirable to decimate the 256 kHz sample rate to 1 kHz. To accomplish this while also providing the necessary low-pass filtering, three stages of filtering are utilized. The first of these is the on-chip filter. This filter is a decimate-by-8 function, and reduces the output word rate from the CS5324 chip to 32 kHz. Two additional filtering stages are to be implemented off-chip with either a DSP, a dedicated ASIC, or another computing device. The first off-chip stage is a decimate-by-8 function, which reduces the output word rate to 4 kHz. The last stage will be a decimate-by-4 function, which will reduce the word rate to 1 kHz. The filter stages are designed so that the first filter has zeroes in its transfer function, such that it rejects the aliased components, due to the first decimate-by-8. The second stage has zeroes such that it rejects the aliased components due to the second decimate-by-8. Neither the on-chip filter, nor the first off-chip stage really affect the passband, but instead, these two stages reduce the output data rate, while at the same time providing anti-alias filtering. The third stage provides the low-pass filtering function.

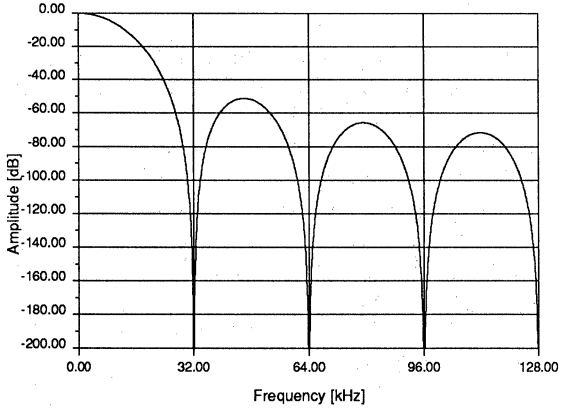


Figure 5. On-chip Filter Response

The CS5324 includes an on-chip 29th-order linear phase FIR (finite-impulse-response) filter and decimator. The response of this filter is illustrated in Figure 5. The filter coefficients are listed in Table 3. The filter performs a fourth-order sinc function, and has a monotonic rolloff in the passband. Attenuation at 500 Hz is 0.0137 dB. The minimum attenuation in the (n x 32 kHz) +/-500 Hz bands is 147 dB. The data output from the on-chip filter has been described in the Data Output and Data Format section above. Data is output at a 32 kHz rate.

The two proposed off-chip filter stages are as follows: The first off-chip stage is a 43rd-order modified sinc FIR filter. Its coefficients are listed in Appendix 1, along with a plot of its transfer function. Attenuation at 500 Hz (CLKIN = 1.024 MHz) is 1.47 dB. The minimum attenuation in the (n x 4 kHz) +/- 500 Hz bands is 132 dB.

The second off-chip filter stage is a 301st-order FIR filter that performs the necessary low-pass function, with less than 0.00016 dB ripple in the dc-400 Hz band. Attenuation in the region from 500 Hz to 2 kHz is typically greater than 130 dB. The coefficients for the second off-chip filter

stage are listed in Appendix 1, along with a plot of its transfer function. An alternate final stage filter is also listed in Appendix 1. It is a 201st-order FIR filter and allows more passband ripple (0.07 dB).

If more ripple or less stop band rejection is acceptable, the off-chip filter complexity can be reduced. The filter examples given have been illustrated only as possible filters which can be utilized with the CS5324 to achieve quality performance from the A/D.

CS5324 Performance

The CS5324 A/D converter is intended for use in seismic and passive sonar applications. These applications require particularly high dynamic range capability. The CS5324 offers high dynamic range without compromising spectral purity. The CS5324 typically achieves 120 dB of dynamic range, while maintaining signal/distortion at 110 dB.

An A/D converter system using the CS5324 A/D converter as its core was tested using Fast Fourier Transform techniques. The CS5324 was connected using the components as shown in the system connection diagram, Figure 9. Data was collected from the CS5324 with the use of a parallel I/O card in a PC-compatible computer. Software was used to implement the two stage digital filtering function. The output from the digital filtering software was submitted to a windowing algorithm and then to the FFT algorithm. Figure 6 illustrates the performance of the CS5324 when tested with a full scale 113 Hz signal. The CS5324 exhibits some second harmonic but no third harmonic. The test frequency of 113 Hz was selected, as this was the center frequency of a bandpass filter, constructed to reject harmonics and line frequencies present at the output of the signal generator. Note that the performance of the CS5324 will generally exceed the capability of most available sine wave test generators for frequencies between 2-500 Hz, as is the case in Figure 6. The excess noise, in this case, is due to the signal source. Figure 7 illustrates the performance of the CS5324 with a -60 dB 100 Hz input signal. The CS5324 is capable of converting with minimal intermodulation distortion as depicted in Figure 8.

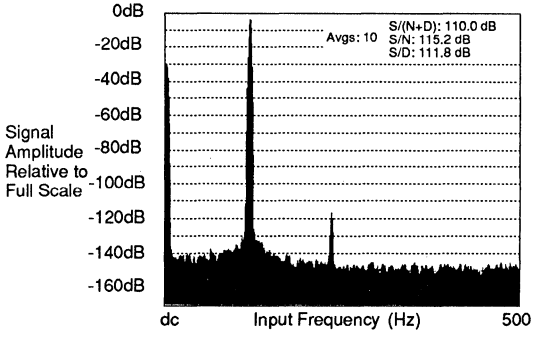


Figure 6. 1024 Point FFT Plot with Full Scale Input, 113 Hz.

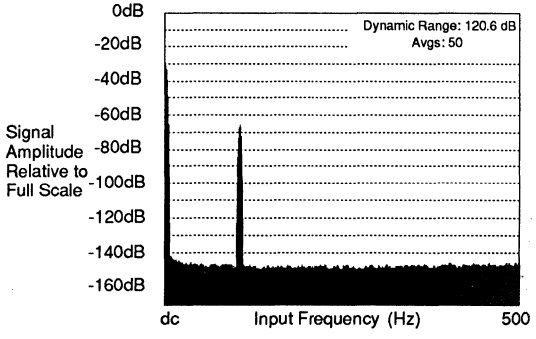
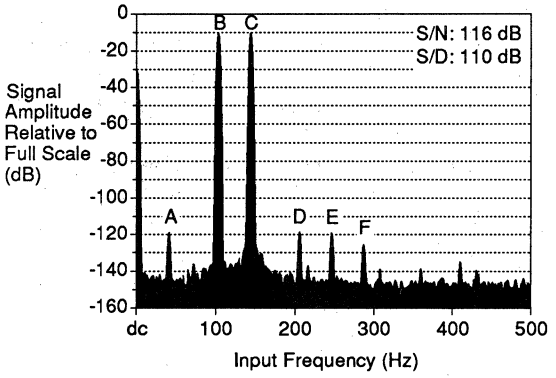


Figure 7. 1024 Point FFT Plot with -60 dB Input, 100 Hz.



A – 40 Hz Intermodulation Distortion Term
B – 100 Hz Fundamental at 6 dB down
C – 140 Hz Fundamental at 6 dB down
D – 200 Hz Second Order Distortion Term
E – 240 Hz Intermodulation Distortion Term
F – 280 Hz Second Order Distortion Term

Note: S/N noise degradation is due to input signal source.

Figure 8. 1024 Point FFT Plot of Intermodulation Products.

Clock Source Considerations

To obtain maximum performance from the CS5324 requires a CLKIN signal which has a low level of clock jitter, i.e., less than 5 picoseconds of jitter. A well-designed crystal-based clock is preferred. The clock oscillator should have a well-regulated supply, with local bypass capacitors at the oscillator. The output from the oscillator should pass through as few logic gates or counter-divider stages as possible, as these can add jitter. Excess clock jitter will reduce the signal/noise performance of the A/D converter.

Power Supply Rejection Ratio

The power supply noise rejection of the CS5324 is frequency dependent. The rejection for frequencies between dc and 500 Hz (CLKIN=1.024 MHz) is nearly constant. Above 500 Hz, the off-chip digital filter will aid in rejecting interference until the frequency of the interference approaches frequencies near CLKIN/21.3 (above 48 kHz for CLKIN=1.024 MHz). Power supply interference above this frequency may cause noise to be modulated into the passband (dc to 500 Hz), degrading the performance of the A/D.

Power Supply Considerations

The system connection diagram, Figure 9, illustrates the recommended power supply arrangements. The CS5324 has two positive analog supply pins and two negative analog supply pins. Multiple pins are used to minimize the possibility of noise coupling on the chip. All six power supply pins should be decoupled to their respective grounds, with a 0.1 uF capacitor located near the device. The digital supplies are decoupled from the analog supplies with 10 ohm resistors to minimize the effects of digital noise in the converter.

The positive digital power supply of the CS5324 must never exceed either positive analog supply by more than a diode drop, or the CS5324 could experience permanent damage. If separate supplies are used for the analog and digital sections of the chip, care must be taken that the analog supply comes up first at power-up. Additionally, the power supplies to the CS5324 should be active before the reference current generator supplies the IREF input current. For proper start-up, the CLKIN signal should be active before IREF is applied. The recommended filter capacitors, which filter the reference currents, will aid in accomplishing these requirements. Use of good ground plane layout is recommended to achieve maximum performance.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filtering in the A/D converter. To achieve maximum benefit of the digital filter in the A/D, the dc-dc operating frequency should be located below 48 kHz (see Power Supply Rejection). A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5324, will minimize the potential for "beat frequencies" appearing in the dc to 500 Hz passband.

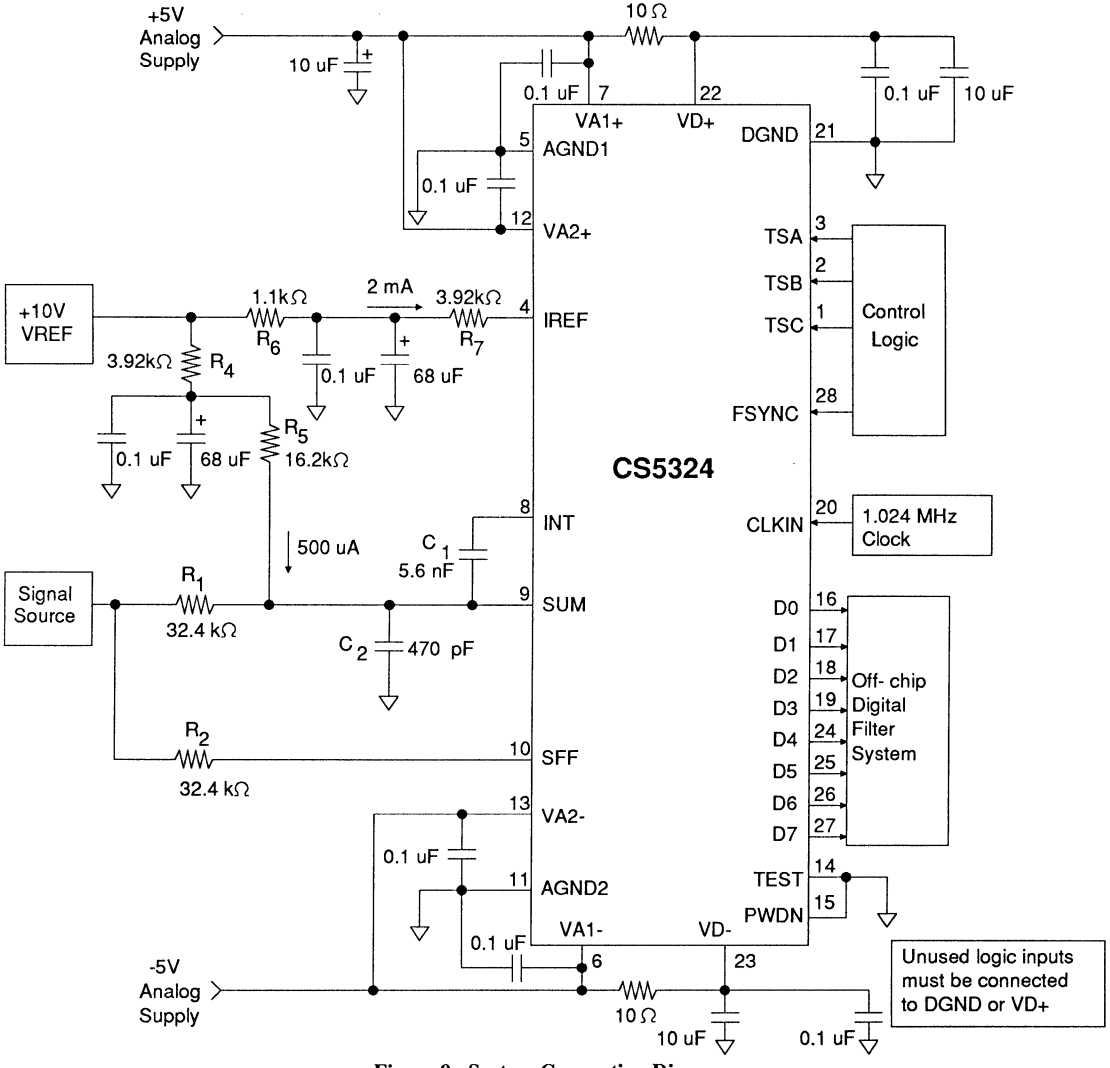
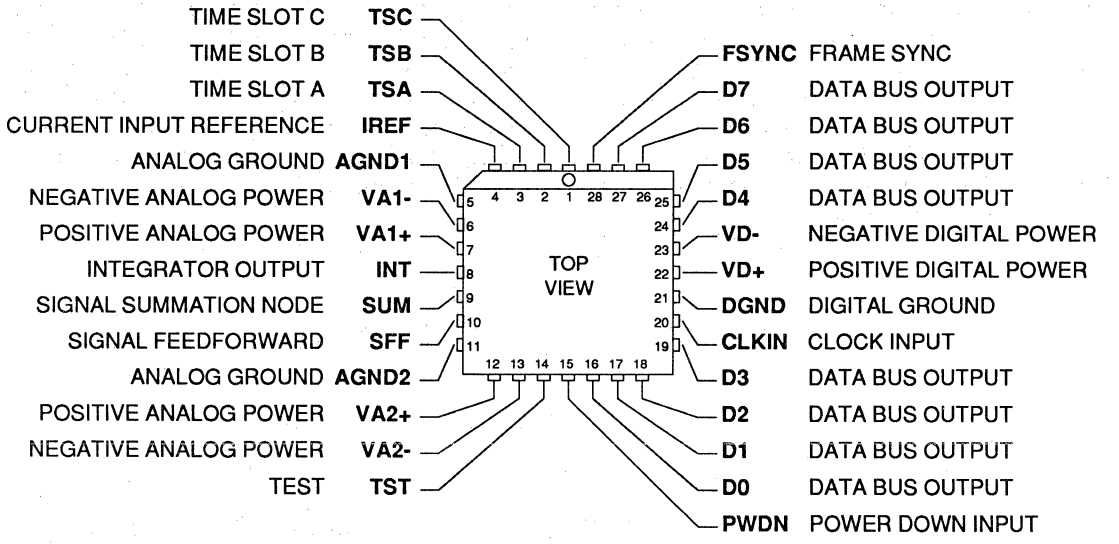


Figure 9. System Connection Diagram



PIN DESCRIPTIONS

Power Supplies

VA1+, VA2+ – Positive Analog Power, PINS 7, 12
Positive analog supply voltage. Nominally +5 volts.

VA1-, VA2- – Negative Analog Power, PINS 6, 13
Negative analog supply voltage. Nominally -5 volts.

AGND1, AGND2 – Analog Ground, PINS 5, 11
Analog ground reference.

VD+ – Positive Digital Power, PIN 22
Positive digital supply voltage. Nominally +5 volts.

VD- – Negative Digital Power, PIN 23
Negative digital supply voltage. Nominally -5 volts.

DGND – Digital Ground, PIN 21
Digital ground reference.

Analog Inputs

IREF – Current Input Reference Node, PIN 4

This node accepts a 2 mA reference current to set the signal gain of the A/D converter.

SFF – Signal Feedforward, PIN 10

The input signal is fed forward around the integrator input stage by means of this input pin. This maximizes signal performance.

SUM – Signal Summation node, PIN 9

This is the input integrator virtual ground summing junction. The external integrator input resistor and integrating capacitor are connected to this node, along with a 500 uA bias current network.

INT – Integrator Output, PIN 8

Output pin of the input integrator stage. The external integrating capacitor is connected to this pin for proper operation.

Digital Inputs

CLKIN – Clock Input, PIN 20

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

PWDN – Power Down Input, PIN 15

When connected to +5 V (VD+) the CS5324 will enter a low-power state. For normal operation this pin should be tied to DGND.

TSA – Time Slot A, PIN 3

See TSC below.

TSB – Time Slot B, PIN 2

See TSC below.

TSC – Time Slot C, PIN1

The TSC input along with TSA and TSB select one of eight possible time periods in which data is output from the CS5324 in a time-multiplexed architecture. Table 2 indicates the decoding of the TSA, TSB, and TSC inputs.

FSYNC – Frame Sync, PIN 28

A transition from a low to high level on this input will re-initialize the CS5324. The digital filter will be initialized and the time-slot counter will be set to zero.

D0 through D7 – Data Bus Outputs, PINS 16-19, 24-27

3-state output pins. Data will be presented out of these pins in the form of two eight-bit bytes during a time slot selected by the TSA, TSB and TSC inputs. The high-order byte with eight data bits will be presented first followed by a second eight-bit byte, which consists of the four low-order data bits, three status bits, and one unused bit.

Miscellaneous

TST – Test, PIN 14

Reserved for production test facility. Should be tied to DGND for normal operation.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale (rms) signal to the broadband noise signal. Broadband noise is measured with the input grounded within the bandwidth of dc to 500 Hz. Units in dB.

Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to 500 Hz. Units in dB.

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (100 and 140 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the the bandwidth of dc to 500 Hz. Units in dB.

Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted to yield a code value of 1280 out of the CS5324. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

Full Scale Drift

The change in the Full Scale value with temperature. Units in %/°C.

Offset

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5324 of 00(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

Offset Drift

The change in the Offset value with temperature. Units in µV/°C.

Appendix 1.

Off-chip Filter Stages

Two stages of off-chip filtering are recommended for use with the CS5324. The first stage is a decimate-by-8 modified-sinc filter with 43 coefficients. Its magnitude response is illustrated in Figure A1.1. Table A1.1 lists its coefficients.

The second filter stage is a 301st-order low-pass filter. Its magnitude plot is illustrated in Figure A1.2 with an expanded view of the passband ripple illustrated in Figure A1.3. Table A1.2 lists the coefficients for this filter.

An alternative second stage filter is also included. It has fewer coefficients, and therefore, is less complex than the previous second stage filter. The magnitude plot of the alternative filter is illustrated in Figure A1.4 with an expanded view of the passband ripple in Figure A1.5. Note that this low-pass function has slightly less out-of-band rejection and somewhat higher passband ripple. The filter coefficients for the alternative final stage are listed in Table A1.3.

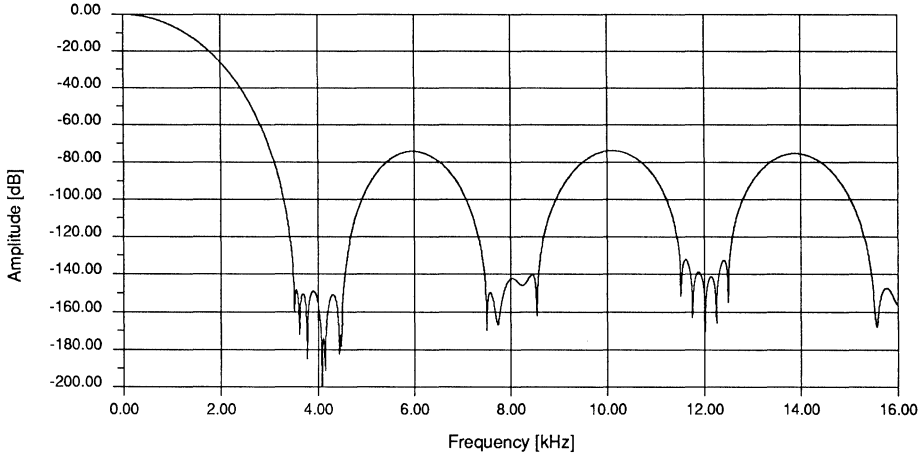


Figure A1.1. First Stage Off-chip Filter – Magnitude Plot

h(1)	= h(43) =	1623	h(12)	= h(32) =	1143595
h(2)	= h(42) =	5137	h(13)	= h(31) =	1494661
h(3)	= h(41) =	12950	h(14)	= h(30) =	1889251
h(4)	= h(40) =	28499	h(15)	= h(29) =	2315005
h(5)	= h(39) =	55210	h(16)	= h(28) =	2752059
h(6)	= h(38) =	99783	h(17)	= h(27) =	3185947
h(7)	= h(37) =	169332	h(18)	= h(26) =	3584677
h(8)	= h(36) =	272838	h(19)	= h(25) =	3926472
h(9)	= h(35) =	414146	h(20)	= h(24) =	4191616
h(10)	= h(34) =	604491	h(21)	= h(23) =	4354400
h(11)	= h(33) =	847470	h(22)	=	4410541

Table A1.1. First Stage Off-chip Filter – 43 Coefficients

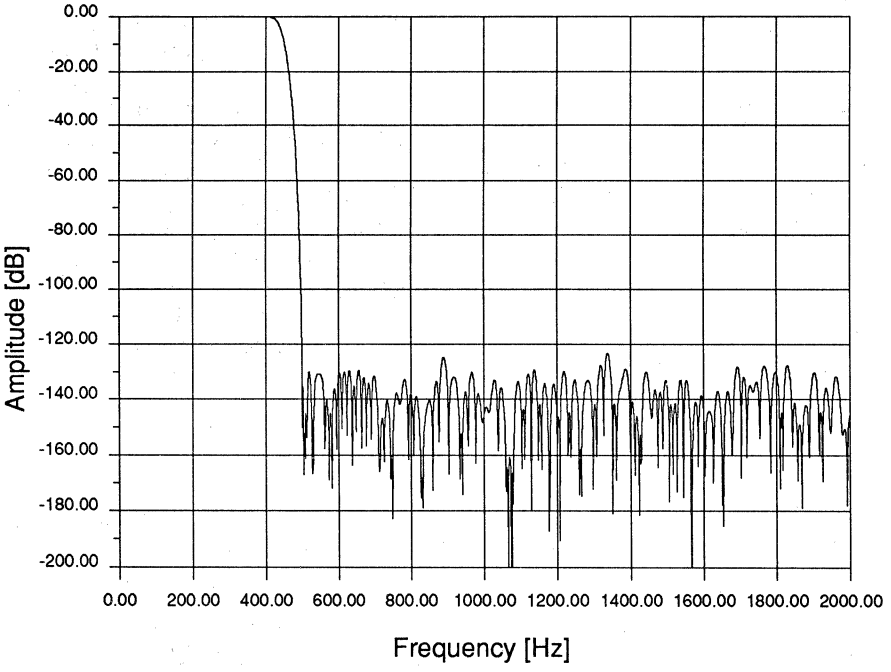


Figure A1.2. Second Stage Off-chip Filter – Magnitude Plot

Table A1.2. Second Stage Off-chip Filter – 301 Coefficients

h(1) = h(301) = 4	h(22) = h(280) = 565	h(43) = h(259) = -1168
h(2) = h(300) = 6	h(23) = h(279) = 467	h(44) = h(258) = -3814
h(3) = h(299) = 4	h(24) = h(278) = 106	h(45) = h(257) = -5004
h(4) = h(298) = -6	h(25) = h(277) = -399	h(46) = h(256) = -3886
h(5) = h(297) = -28	h(26) = h(276) = -826	h(47) = h(255) = -631
h(6) = h(296) = -58	h(27) = h(275) = -935	h(48) = h(254) = 3478
h(7) = h(295) = -85	h(28) = h(274) = -594	h(49) = h(253) = 6517
h(8) = h(294) = -93	h(29) = h(273) = 127	h(50) = h(252) = 6784
h(9) = h(293) = -68	h(30) = h(272) = 947	h(51) = h(251) = 3702
h(10) = h(292) = -7	h(31) = h(271) = 1468	h(52) = h(250) = -1711
h(11) = h(291) = 75	h(32) = h(270) = 1359	h(53) = h(249) = -7104
h(12) = h(290) = 146	h(33) = h(269) = 538	h(54) = h(248) = -9771
h(13) = h(289) = 166	h(34) = h(268) = -725	h(55) = h(247) = -7963
h(14) = h(288) = 108	h(35) = h(267) = -1882	h(56) = h(246) = -1918
h(15) = h(287) = -23	h(36) = h(266) = -2320	h(57) = h(245) = 5964
h(16) = h(286) = -185	h(37) = h(265) = -1673	h(58) = h(244) = 12013
h(17) = h(285) = -302	h(38) = h(264) = -56	h(59) = h(243) = 12943
h(18) = h(284) = -300	h(39) = h(263) = 1898	h(60) = h(242) = 7567
h(19) = h(283) = -144	h(40) = h(262) = 3264	h(61) = h(241) = -2315
h(20) = h(282) = 130	h(41) = h(261) = 3239	h(62) = h(240) = -12399
h(21) = h(281) = 414	h(42) = h(260) = 1580	h(63) = h(239) = -17689

h(64) = h(238) = -14905
h(65) = h(237) = -4360
h(66) = h(236) = 9720
h(67) = h(235) = 20798
h(68) = h(234) = 22983
h(69) = h(233) = 14065
h(70) = h(232) = -2922
h(71) = h(231) = -20553
h(72) = h(230) = -30166
h(73) = h(229) = -26027
h(74) = h(228) = -8537
h(75) = h(227) = 15226
h(76) = h(226) = 34244
h(77) = h(225) = 38558
h(78) = h(224) = 24349
h(79) = h(223) = -3468
h(80) = h(222) = -32689
h(81) = h(221) = -49042
h(82) = h(220) = -43038
h(83) = h(219) = -15194
h(84) = h(218) = 23126
h(85) = h(217) = 54160
h(86) = h(216) = 61841
h(87) = h(215) = 39925
h(88) = h(214) = -3894
h(89) = h(213) = -50321
h(90) = h(212) = -76781
h(91) = h(211) = -68222
h(92) = h(210) = -25304
h(93) = h(209) = 34332
h(94) = h(208) = 83049
h(95) = h(207) = 95832
h(96) = h(206) = 62860
h(97) = h(205) = -4158
h(98) = h(204) = -75642
h(99) = h(203) = -116939
h(100) = h(202) = -104877
h(101) = h(201) = -40254
h(102) = h(200) = 50253
h(103) = h(199) = 124723
h(104) = h(198) = 145121
h(105) = h(197) = 96333
h(106) = h(196) = -4251
h(107) = h(195) = -112209
h(108) = h(194) = -175323
h(109) = h(193) = -158449
h(110) = h(192) = -62339
h(111) = h(191) = 73359
h(112) = h(190) = 185878
h(113) = h(189) = 217891
h(114) = h(188) = 146090
h(115) = h(187) = -4196
h(116) = h(186) = -166796
h(117) = h(185) = -263179
h(118) = h(184) = -239689
h(119) = h(183) = -96169
h(120) = h(182) = 108776
h(121) = h(181) = 280687
h(122) = h(180) = 331861
h(123) = h(179) = 224879
h(124) = h(178) = -4045
h(125) = h(177) = -255205
h(126) = h(176) = -407467
h(127) = h(175) = -375114
h(128) = h(174) = -153475
h(129) = h(173) = 169870
h(130) = h(172) = 447384
h(131) = h(171) = 536503
h(132) = h(170) = 369619
h(133) = h(169) = -3865
h(134) = h(168) = -426733
h(135) = h(167) = -696076
h(136) = h(166) = -655325
h(137) = h(165) = -276498
h(138) = h(164) = 307141
h(139) = h(163) = 839720
h(140) = h(162) = 1044525
h(141) = h(161) = 751372
h(142) = h(160) = -3724
h(143) = h(159) = -953887
h(144) = h(158) = -1671933
h(145) = h(157) = -1718209
h(146) = h(156) = -813868
h(147) = h(155) = 1027355
h(148) = h(154) = 3464481
h(149) = h(153) = 5912858
h(150) = h(152) = 7722306
h(151) = h(151) = 8388608

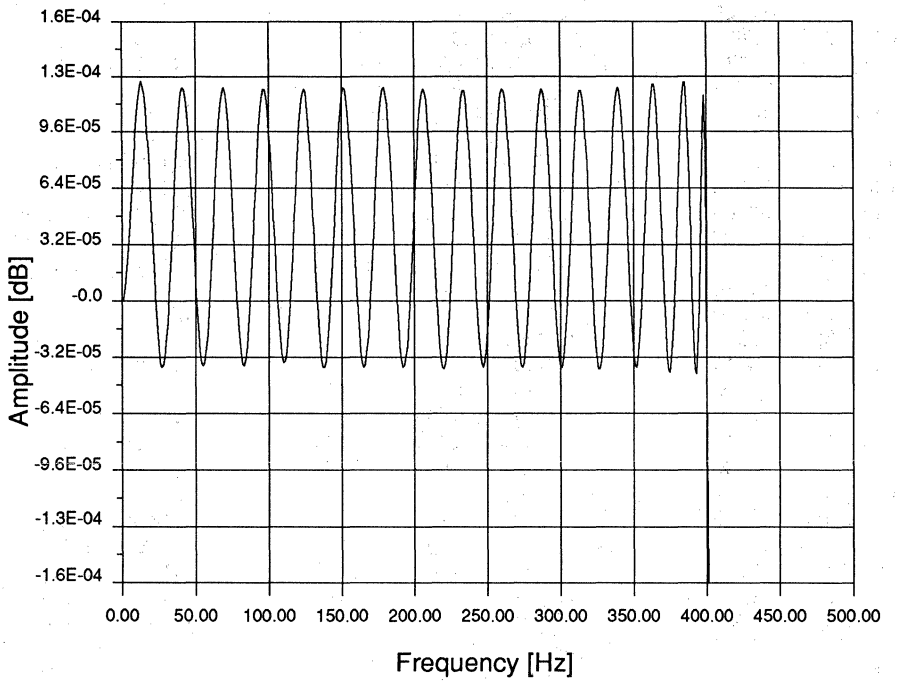


Figure A 1.3. Second Stage Off-chip Filter – Passband Ripple Plot

Table A 1.3. Alternate Second Stage Off-chip Filter – 201 Coefficients

h(1) = h(201) = -68	h(21) = h(181) = -5542	h(41) = h(161) = 13122
h(2) = h(200) = -266	h(22) = h(180) = 4957	h(42) = h(160) = 49003
h(3) = h(199) = -681	h(23) = h(179) = 15066	h(43) = h(159) = 66874
h(4) = h(198) = -1350	h(24) = h(178) = 20225	h(44) = h(158) = 56133
h(5) = h(197) = -2192	h(25) = h(177) = 17383	h(45) = h(157) = 18103
h(6) = h(196) = -2938	h(26) = h(176) = 6584	h(46) = h(156) = -33025
h(7) = h(195) = -3124	h(27) = h(175) = -8560	h(47) = h(155) = -75161
h(8) = h(194) = -2181	h(28) = h(174) = -21921	h(48) = h(154) = -87623
h(9) = h(193) = 366	h(29) = h(173) = -27236	h(49) = h(153) = -60982
h(10) = h(192) = 4634	h(30) = h(172) = -20930	h(50) = h(152) = -2877
h(11) = h(191) = 10142	h(31) = h(171) = -4177	h(51) = h(151) = 63451
h(12) = h(190) = 15743	h(32) = h(170) = 16903	h(52) = h(150) = 108121
h(13) = h(189) = 19809	h(33) = h(169) = 33304	h(53) = h(149) = 107776
h(14) = h(188) = 20712	h(34) = h(168) = 36843	h(54) = h(148) = 57300
h(15) = h(187) = 17462	h(35) = h(167) = 24059	h(55) = h(147) = -25620
h(16) = h(186) = 10292	h(36) = h(166) = -1482	h(56) = h(146) = -106083
h(17) = h(185) = 889	h(37) = h(165) = -29822	h(57) = h(145) = -146288
h(18) = h(184) = -7915	h(38) = h(164) = -48300	h(58) = h(144) = -122895
h(19) = h(183) = -13029	h(39) = h(163) = -47054	h(59) = h(143) = -39611
h(20) = h(182) = -12292	h(40) = h(162) = -24000	h(60) = h(142) = 71441

h(61) = h(141) = 161525	h(75) = h(127) = -349221	h(89) = h(113) = 932553
h(62) = h(140) = 186220	h(76) = h(126) = -386474	h(90) = h(112) = 1005109
h(63) = h(139) = 126698	h(77) = h(125) = -245727	h(91) = h(111) = 595458
h(64) = h(138) = 1412	h(78) = h(124) = 28395	h(92) = h(110) = -209660
h(65) = h(137) = -138356	h(79) = h(123) = 323264	h(93) = h(109) = -1121850
h(66) = h(136) = -228840	h(80) = h(122) = 502448	h(94) = h(108) = -1730461
h(67) = h(135) = -222225	h(81) = h(121) = 466350	h(95) = h(107) = -1642084
h(68) = h(134) = -110815	h(82) = h(120) = 203318	h(96) = h(106) = -632318
h(69) = h(133) = 64893	h(83) = h(119) = -193406	h(97) = h(105) = 1247052
h(70) = h(132) = 229769	h(84) = h(118) = -554902	h(98) = h(104) = 3649798
h(71) = h(131) = 305309	h(85) = h(117) = -704448	h(99) = h(103) = 6019586
h(72) = h(130) = 245984	h(86) = h(116) = -538246	h(100) = h(102) = 7753188
h(73) = h(129) = 64260	h(87) = h(115) = -84243	h(101) = h(101) = 8388608
h(74) = h(128) = -168625	h(88) = h(114) = 490248	

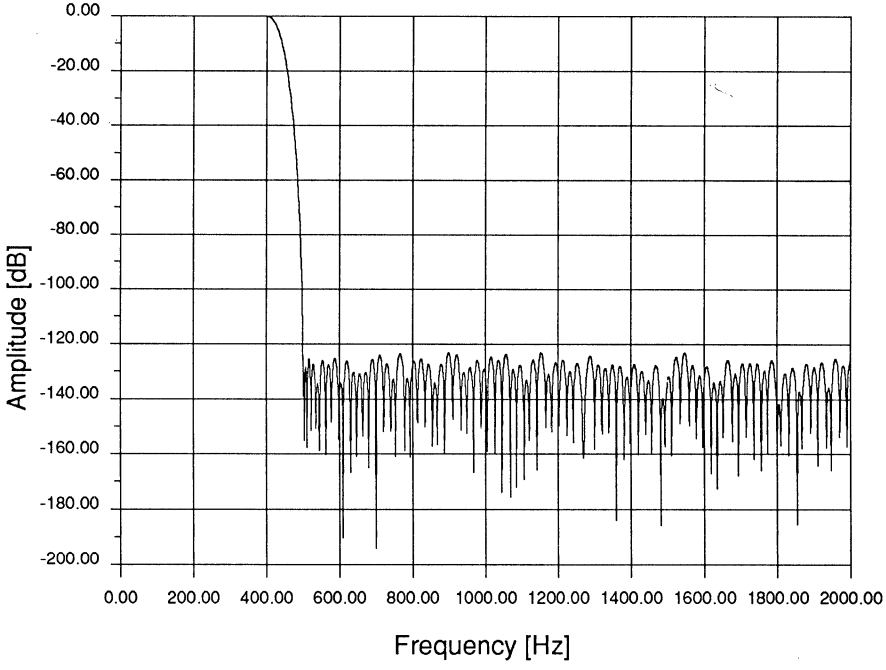


Figure A 1.4 Alternate Second Stage Off-chip Filter – Magnitude Plot

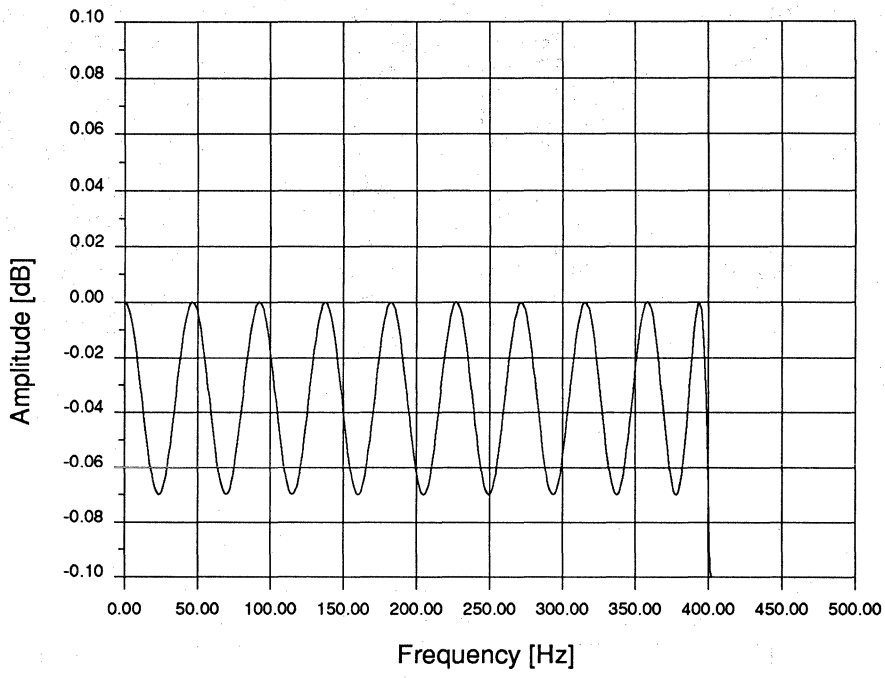


Figure A1.5 Alternate Second Stage Off-chip Filter – Passband Ripple Plot

Semiconductor Corporation

CS5326 CS5327
CS5328 CS5329

16 & 18-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates
  - 30 kHz to 50 kHz
- Low Noise and Distortion
  - 95 dB dynamic range, 16-Bit
  - 97 dB dynamic range, 18-Bit
  - 100 dB dynamic range, 19-Bit Mono
  - 0.0015% THD
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.001dB Passband Ripple
  - 86dB Stopband Rejection
- Low Power Dissipation: 450 mW
  - Power-Down Mode for Portable Applications

General Description

The CS5326, CS5327, CS5328 & CS5329 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16 or 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

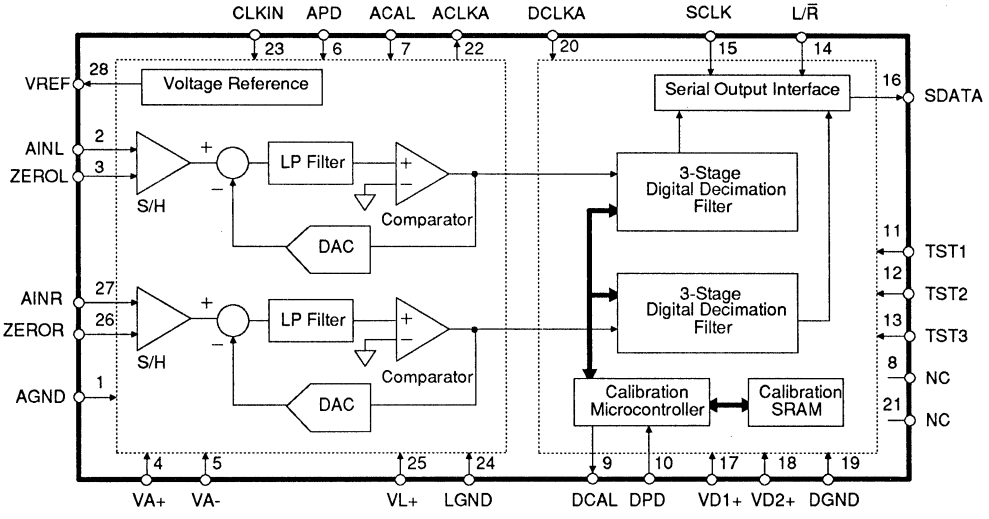
The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5326 & CS5327 are 16-bit ADCs, achieving 95 dB dynamic range. The CS5328 & CS5329 are 18-bit ADCs with 97 dB dynamic range in stereo mode and 100 dB dynamic range in mono mode.

The CS5326 & CS5328 have digital filters which are compatible with CD requirements. The CS5327 & CS5329 have filters which guarantee no aliasing. The filters have linear phase, 0.001 dB passband ripple, and >86 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP.

ORDERING INFORMATION: See Page 3-237



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VL+,VD1+,VD2+ = 5V; VA- = -5V; Full-Scale Input Sinewave, 4kHz; CLKIN = 6.144MHz; SCLK = 3.072 MHz; Source Impedance = 50Ω with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter*			Symbol	Specification min	typ	max	Units
Resolution		CS5326, CS5327		16			Bits
		CS5328, CS5329		18			Bits
Dynamic Performance							
Dynamic Range		CS5326, CS5327		92.7	95.7		dB
		CS5328, CS5329		94.7	97.1		dB
(Note 1)	Mono	CS5328, CS5329			100.1		dB
Signal-to-		CS5326, CS5327		90.7	92.7		dB
(Noise + Distortion)		CS5328, CS5329	S/(N+D)	92.5	94.5		dB
(Note 1)	Mono	CS5328, CS5329			97		dB
Total Harmonic Distortion							
Vin = ± FS			THD	0.003	0.0015		%
Vin = -20 dB					0.001		%
Interchannel Phase Deviation					0.0001		Degrees
Interchannel Isolation (dc to 20 kHz)				100	106		dB
dc Accuracy							
Interchannel Gain Mismatch					0.01	0.05	dB
Gain Error					± 1	± 5	%
Gain Drift					50		ppm/ °C
Bipolar Offset Error		CS5326, CS5327			± 5	± 15	LSB (16-bit)
(After Calibration)		CS5328, CS5329			± 20	± 60	LSB (18-bit)
Analog Input							
Input Voltage Range	(± Full Scale)		VIN	± 3.50	± 3.68		Volts
Input Impedance			ZIN		65		kΩ
Power Supplies							
Power Supply Current	(VA+) + (VL+)		IA+		25	TBD	mA
with APD,DPD low	VA-		IA-		25	TBD	mA
(Normal Operation)	(VD1+) + (VD2+)		ID+		40	TBD	mA
Power Supply Current	(VA+) + (VL+)		IA+		10		uA
with APD,DPD high	VA-		IA-		10		uA
(Power-Down Mode)	(VD1+) + (VD2+)		ID+		4	TBD	mA
Power Dissipation	(APD, DPD Low)		PDN		450	TBD	mW
	(APD, DPD High)		PDS		20	TBD	mW
Power Supply Rejection Ratio (dc to 26 kHz)			PSRR		54		dB
(26 kHz to 3.046 MHz)					100		dB

Notes: 1. Mono means connecting AINL & AINR together and adding together the output words from each channel.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD1+,VD2+= 5V ± 5%; VA- = -5V ± 5%; CLKIN = 6.144MHz)

Parameter			Symbol	Min	Typ	Max	Units
Passband	(-3 dB)	CS5326, CS5328		0		23.5	kHz
	(-3 dB)	CS5327, CS5329		0		21.6	kHz
	(-0.001 dB)	CS5326, CS5328		0		21.8	kHz
	(-0.001 dB)	CS5327, CS5329		0		20.0	kHz
Passband Ripple						0.001	dB
Stopband		CS5326, CS5328		26		3046	kHz
		CS5327, CS5329		24		3052	kHz
Stopband Attenuation		(Note 2)		86			dB
Group Delay			t_{gd}		4274/CLKIN		s
Group Delay Variation vs. Frequency			$\triangle t_{gd}$			0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for a CLKIN of 6.144MHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±21.8kHz for the CS5326 & CS5328, or n x 3.072MHz ±20.0kHz for the CS5327 & CS5329 , where n = 0,1,2,3...).

3

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD1+,VD2+= 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (CLKIN)	V_{IH}	(VD+) - 1.0	-	-	V
Low-Level Input Voltage (CLKIN)	V_{IL}	-	-	1.0	V
High-Level Input Voltage (except CLKIN)	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage (except CLKIN)	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD1+,VD2+	4.75	5.0	5.25	V
	Positive Logic	VL+	4.75	5.0	VA+	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	−4.75	−5.0	−5.25	V
Analog Input Voltage	(Note 3)	V_{AIN}	−3.68	-	3.68	V
CLKIN Frequency		f_{CLK}	3.84	-	6.4	MHz
SCLK Frequency		f_{SCLK}	f_{CLK} /2	-	f_{CLK}	Hz
L/$\overline{R}$ Frequency		$f_{L/\overline{R}}$	f_{CLK} /128	-	f_{CLK} /128	Hz

Notes: 3. The ADCs accept input voltages up to the analog supplies (VA+, VA-). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification.

SWITCHING CHARACTERISTICS

(T_A = 25 °C; VA+, VL+, VD1+ , VD2+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

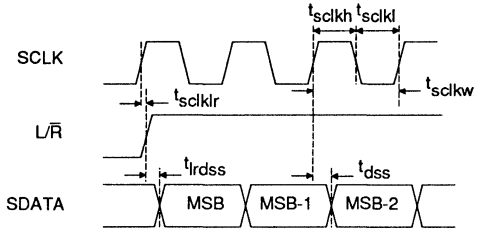
Parameter	Symbol	Min	Typ	Max	Units
CLKIN Period	t_{clkw}	155	-	260	ns
CLKIN Low	t_{clkl}	50	-	-	ns
CLKIN High	t_{clkh}	50	-	-	ns
CLKIN Rising to ACLKA edge (Note 4)	t_{clka}	40	-	100	ns
ACLKA Falling to L/$\overline{R}$ Edge (Note 4)	t_{aclr}	-140	-	140	ns
CLKIN Rising to L/$\overline{R}$ Edge (Note 4) ACLKA to CLKIN phase correct ACLKA to CLKIN phase unknown	t_{clr}	 -10 -10	 - -	 170 30	ns
SCLK Pulse Width Low	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High	t_{sclkh}	60	-	-	ns
SCLK Period	t_{sclkw}	155	-	-	ns
SCLK Rising to SDATA Valid	t_{dss}	-	-	45	ns
L/$\overline{R}$ edge to MSB Valid	t_{lrdss}	-	-	50	ns
SCLK Rising to L/$\overline{R}$ edge	t_{sclklr}	-40	-	40	ns
DPD, APD pulse width	t_{pd}	150	-	-	ns
CLKIN Falling to APD Falling	t_{apdclk}	-30	-	30	ns

Notes: 4. It is recommended that L/$\overline{R}$ be generated by dividing ACLKA by 64. If CLKIN is used to generate L/$\overline{R}$, a longer CLKIN to L/$\overline{R}$ delay may be tolerated if the phase of ACLKA is determined through the use of the APD pin. When high, the APD pin resets the divide-by-two circuit that generates ACLKA from CLKIN (that is, ACLKA is reset to "0"). APD should be brought low on a falling edge of CLKIN. This falling edge should be chosen such that L/$\overline{R}$ edges nominally occur at ACLKA falling edges.

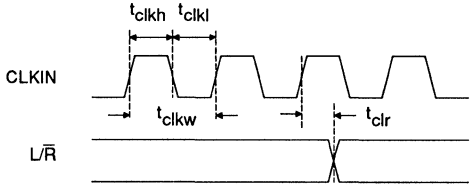
ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	+6.0	V
	Negative Analog	VA-	+0.3	-6.0	V
	Positive Logic	VL+	-0.3	(VA+) + 0.3	V
	Positive Digital	VD1+,VD2+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	± 10	mA
Analog Input Voltage (AIN and ZERO pins)		V_{INA}	(VA-)- 0.3	(VA+)+ 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Temperature (power applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

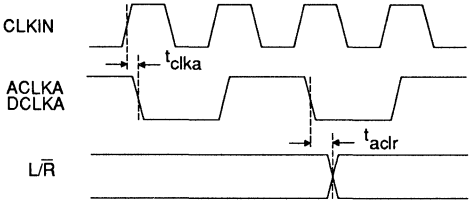
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.



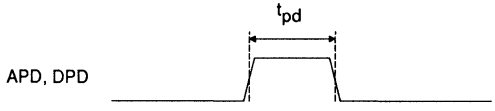
Serial Data Timing



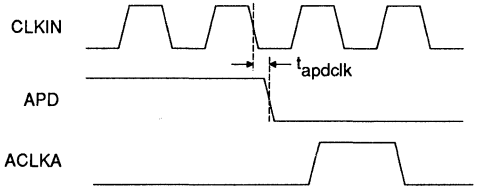
Channel Selection Timing Using L/R Derived From CLKIN/128



Channel Selection Timing Using L/R Derived from ACLKA/64



Power Down Timing



ACLKA Phase Determination using APD

GENERAL DESCRIPTION

The CS5326, CS5327, CS5328 and CS5329 are 16 & 18-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64× sampling rate. A three-stage digital filter then constructs pairs of 16-bit or 18-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of ± 3.68 volts. Any zero offset can be internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16 or 18-bit numbers. Typical power consumption of only 450 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these ADCs, see the references at the end of this data sheet.

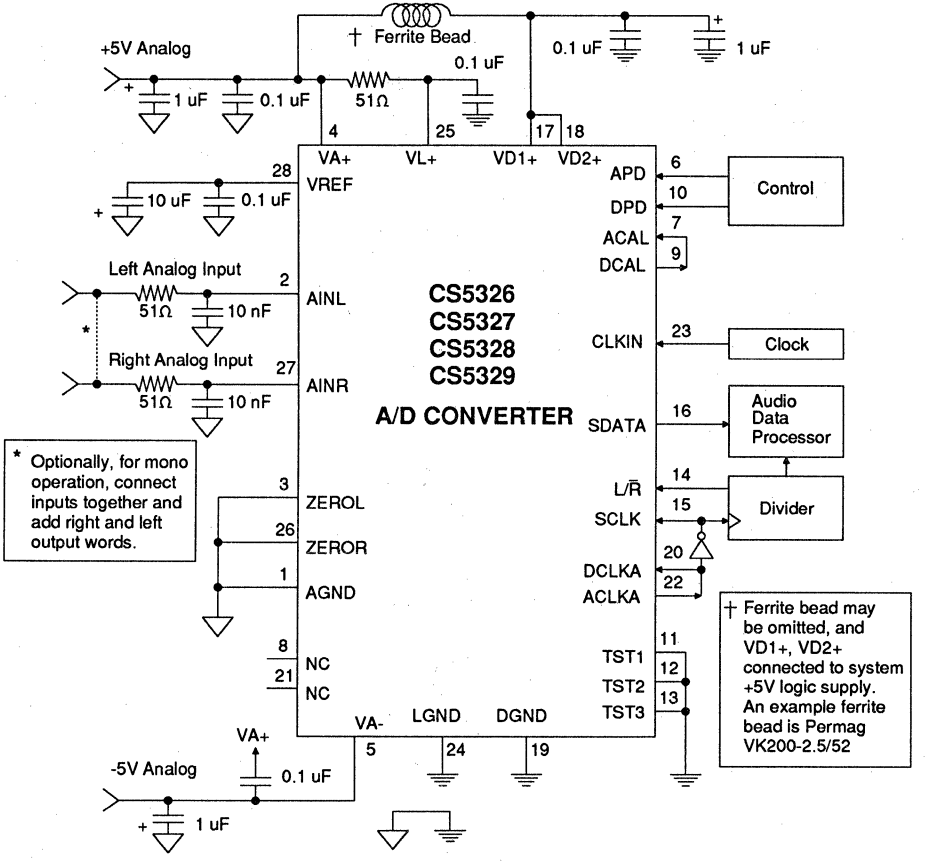


Figure 1. Typical Connection Diagram

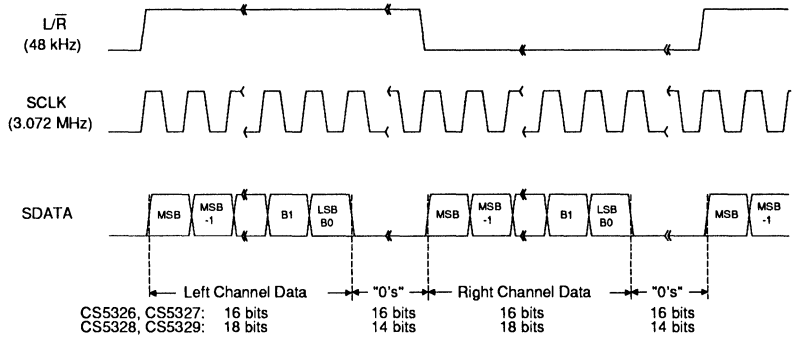


Figure 2. Data Output Timing

SYSTEM DESIGN WITH THE CS5326/7/8/9

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required.

Clocks and Data Output Format

All timing and control inputs to the ADC can be easily generated from a master system clock. This clock, connected to the CLKIN pin on the device, must be exactly equal to 128 times the desired output word rate. Standard digital audio rates are 32 kHz, 44.1 kHz and 48 kHz, requiring master clock rates of 4.096 MHz, 5.6448 MHz and 6.144 MHz, respectively.

The CLKIN signal should be greater than 4 volts for a logic one and less than 1 volt for a logic zero. This is to minimize any clock related jitter in the sampling process, which can smear high frequency signals. Indeed, a low jitter (such as a crystal-based) clock is recommended.

Data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The rising edge of SCLK causes the part to output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. Even so, a rising SCLK edge must occur coincident (within the timing tolerance) with the L/$\overline{R}$ edge for internal housekeeping purposes.

It is recommended to connect SCLK to ACLKA, as shown in Figure 1. Fourteen or sixteen trailing zero's will be clocked out on SDATA as part of each data word, as shown in Figure 2. ACLKA's frequency is the analog modulator sampling rate, and if a lower frequency is used for SCLK, slight degradation of the ADC dynamic range can occur due to interference effects.

Selection of left channel or right channel data is accomplished using the L/$\overline{R}$ input pin. The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled inputs.

Rising edges of L/$\overline{R}$ are used to synchronize the digital filter; therefore L/$\overline{R}$'s frequency must be CLKIN/128. It is preferable to generate L/$\overline{R}$ by dividing ACLKA by 64. If CLKIN is used to generate L/$\overline{R}$, it is best to determine the phase of ACLKA through the use of the APD pin. (When high, the APD pin resets the internal divide-by-two circuit that generates ACLKA. See Figure 4 for an example circuit.) If ACLKA phase is left indeterminate, then the CLKIN to L/$\overline{R}$ delay must be shorter than the smaller delay shown in the Switching Characteristics table (see Note 4.).

Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically ± 3.68 volts.

The ADC samples the analog inputs at 3.072 MHz for a 6.144 MHz CLKIN. For the CS5326 & CS5328 the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5327 & CS5329 the digital filter rejects all noise between 24 kHz and (3.072 MHz-24 kHz). However, the filter will not reject frequencies right around 3.072 MHz. Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 51 Ω resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins.

The on-chip voltage reference output is brought out to the VREF pin. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 20 mW. In addition, exiting the power-down state initiates the offset calibration procedure. This can be important for digital audio applications since any initial offset manifests itself as an audible power-on click.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle, whereas APD going low sets the phase of the ACLKA signal. If not using the power down feature and if not using APD to set the phase of ACLKA, APD should be tied to ground. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10 µF, as stated in the "Power-Up Considerations" section.

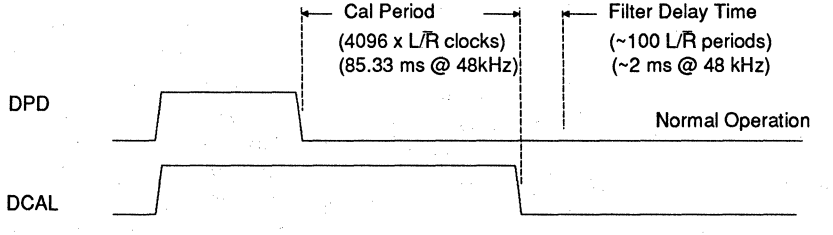


Figure 3. Initial Calibration Cycle Timing

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 3, the DCAL output is high during calibration, which takes 4096 L/$\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to ground the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present on the front end.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 100 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals. The transition is simply the natural filter response and is, of course, graceful.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference, however, can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

3

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows powering the part from single ±5 volt supplies. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground planes, with the ADC straddling the boundary. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

Multiple ADC's

In systems where multiple ADC's are used, care must be taken to ensure that the ACLKA phases

are synchronized if simultaneous sampling is desired. In the absence of this synchronization, the sampling difference could be one CLKIN cycle (typically 162 ns). If this difference is unacceptable, the parts may be synchronized to within several nanoseconds by using the circuit shown in Figure 4. This circuit ensures that when the ADC's come out of power-down mode, ACLKA will have the same phase between all ADC's. The APD signal is used to reset the internal divide-by-two flip-flop which generates ACLKA. The circuit also ensures that L/$\overline{R}$ and SCLK occur at the correct time.

PERFORMANCE

FFT Tests

For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 5 shows the spectral purity of the CS5326 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 94.63 dB.

Figure 6 shows the CS5326 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at -112 dB.

Figure 7 shows the low-level performance of the CS5326. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 8 shows the same very low input amplitude performance, but at 9kHz input frequency.

Figure 9 shows the CS5327 FFT plot with an input signal of 1 kHz at -10 dB. This is very similar to the CS5326 plot, but notice the reduction in the noise floor between 22 kHz and

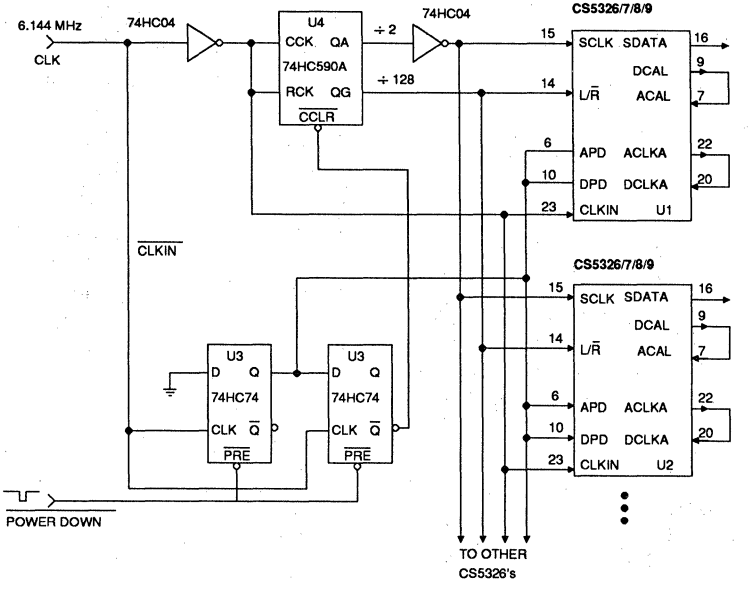


Figure 4. Connections for Synchronization of Multiple CS5326/7/8/9 ADC's.

24 kHz. This is caused by the digital filter attenuating the noise in its transition band.

Figure 10 shows a plot of Signal to (Noise + Distortion) versus input amplitude relative to full scale. For an ideal ADC, this plot would be a straight line at 45° for all input frequencies between dc and half the output word rate. The

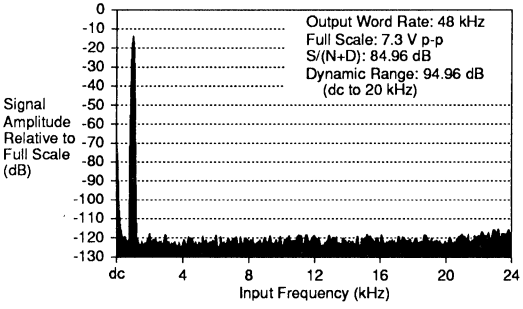


Figure 5. CS5326 FFT Plot with -10 dB, 1 kHz Input

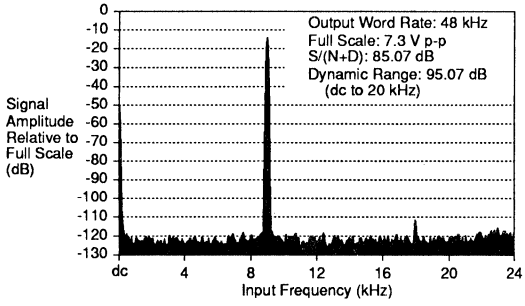


Figure 6. CS5326 FFT Plot with -10 dB, 9 kHz Input

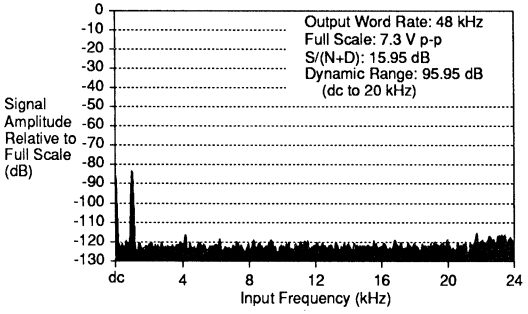


Figure 7. CS5326 FFT Plot with -80 dB, 1 kHz Input

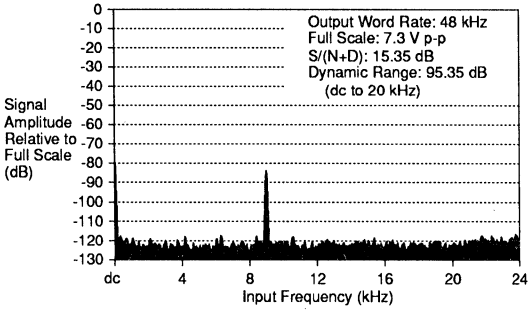


Figure 8. CS5326 FFT Plot with -80 dB, 9 kHz Input

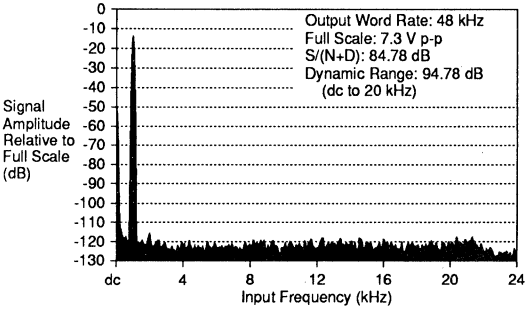


Figure 9. CS5327 FFT Plot with -10 dB, 1 kHz Input

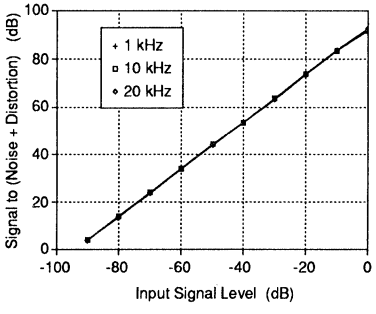


Figure 10. CS5326, CS5327 Signal to Noise+Distortion Ratio vs. Input Level

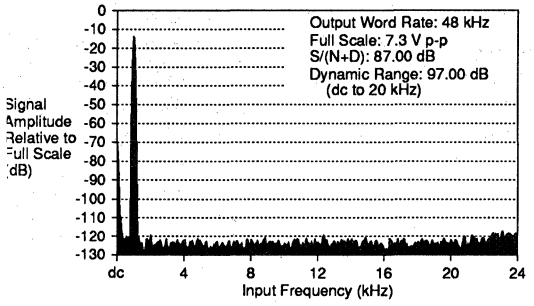


Figure 11. CS5328 FFT Plot with -10 dB, 1 kHz Input

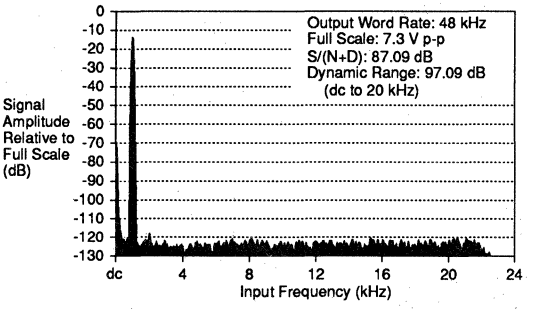


Figure 12. CS5329 FFT Plot with -10 dB, 1 kHz Input

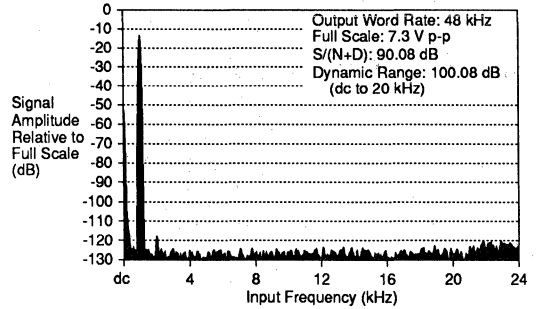


Figure 13. CS5328 in Mono Mode FFT Plot with -10 dB, 1 kHz Input

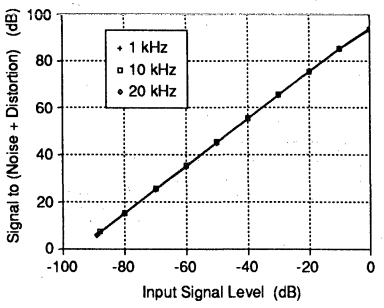


Figure 14. CS5328 Signal to Noise+Distortion Ratio vs. Input Level

measured data from a CS5326 shows both the excellent high frequency performance as well as the maintenance of good performance with low input levels.

Figure 11 shows the18-bit CS5328 FFT plot. Notice the 2 dB improvement in dynamic range over the CS5326.

Figure 12 shows the18-bit CS5329 FFT plot. Notice the filter cut-off at 22 kHz, and the 2 dB improvement in dynamic range over the CS5327.

Figure 13 shows the CS5328 operated in 19-bit mono mode, with the two inputs joined together, and the output words added. Notice the 3 dB improvement over Figure 11.

Figure 14 shows a plot of Signal to Noise + Distortion versus Input Level for the 18-bit CS5328. Notice the improvement in values over Figure 10.

DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the codewidths. Figure 15 shows the excellent Differential Non-Linearity of the CS5326. This plot displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within ± 0.2 LSB's of

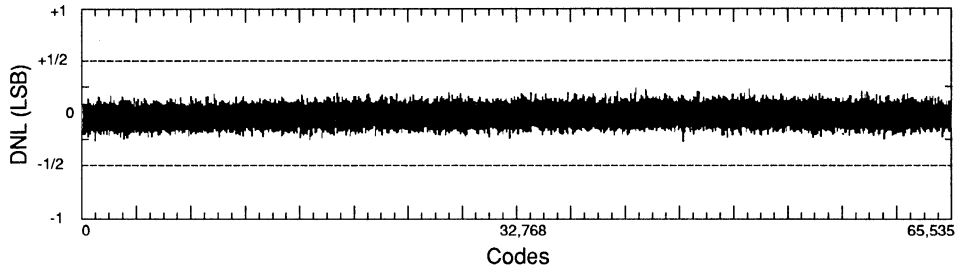


Figure 15. CS5326 Differential Non-Linearity Plot

ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 10 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.

Digital Filter

Figures 16 through 21 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz, with a CLKIN frequency of 6.144 MHz. The filter frequency response will scale precisely with changes in CLKIN frequency. The passband ripple is flat to ± 0.001 dB maximum. Stopband rejection is greater than 86 dB.

Figures 16,18 &20 show the CS5326 and CS5328 filter characteristics. Figure 20 is an expanded view of the transition band.

Figures 17,19 & 21 show the CS5327 and CS5329 filter characteristics. Figure 21 is an expanded view of the transition band. Notice how the filter enters the stopband at exactly 24 kHz, which is half the output word rate, thereby guaranteeing no aliasing.

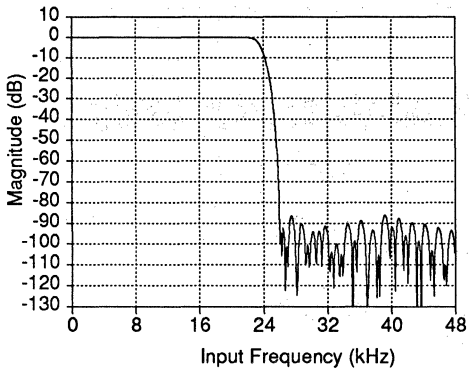


Figure 16. CS5326 /8 Digital Filter Stopband Rejection

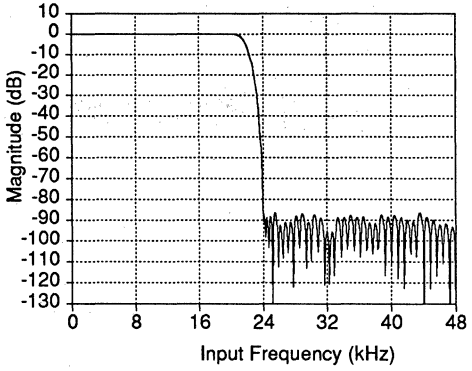


Figure 17. CS5327/9 Digital Filter Stopband Rejection

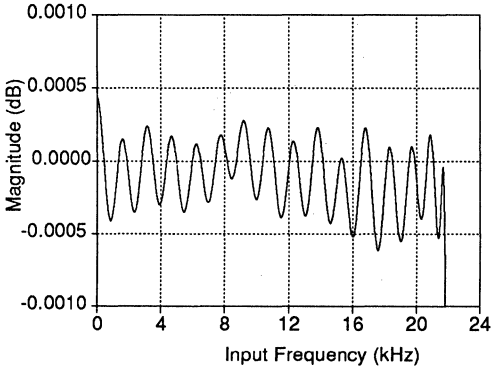


Figure 18. CS5326/8 Digital Filter Passband Ripple

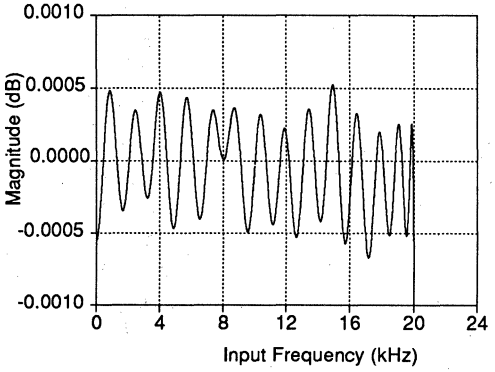


Figure 19. CS5327/9 Digital Filter Passband Ripple

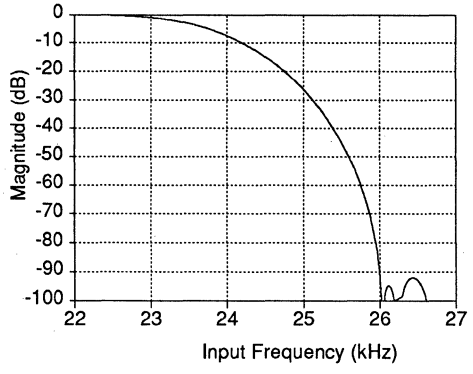


Figure 20. CS5326/8 Digital Filter Transition Band

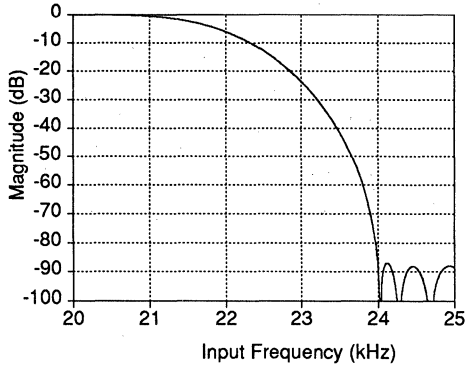
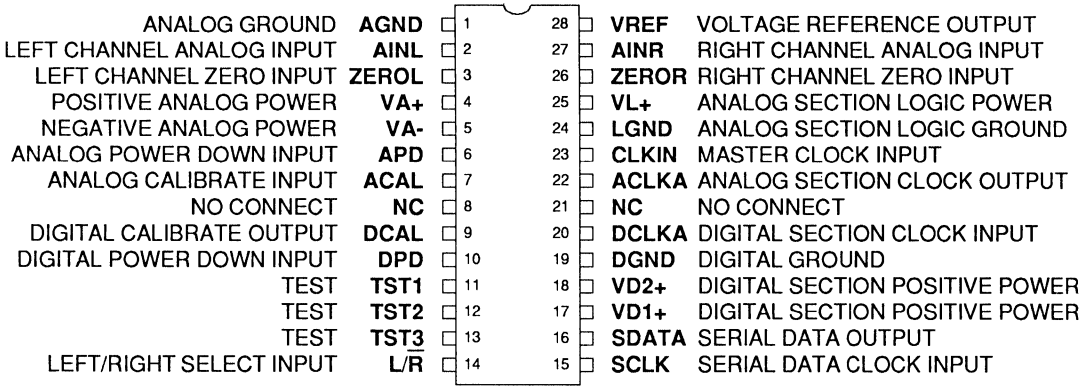


Figure 21. CS5327/9 Digital Filter Transition Band

PIN DESCRIPTIONS



3

Power Supply Connections

VA+ - Positive Analog Power, PIN 4.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 25.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 24
Ground for the logic portions of the analog section.

VD1+, VD2+ - Positive Digital Power, PINS 17, 18.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.
Digital ground for the digital section.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27
Analog input connections for the left and right input channels. Nominally ±3.68 volts full scale.

ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks..

Analog Outputs

VREF - Voltage Reference Output, PIN 28.

Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

Digital Inputs

CLKIN - Master Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators sample rate. Sampling rates, output rates, and digital filter characteristics scale to CLKIN frequency. CLKIN frequency of 6.144 MHz corresponds to an output word rate of 48 kHz per channel.

DCLKA - Digital Section Input Clock, PIN 20.

This clock is used to clock the modulator output data into the digital section. Must be connected to ACLKA.

SCLK - Serial Output Data Clock, PIN 15.

Data bits are output on the rising edge of SCLK.

L/$\overline{R}$ - Left/Right Select, PIN 14.

Select the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. Thereafter, CLKIN, SCLK and L/$\overline{R}$ should run synchronously. L/$\overline{R}$ must be equal to CLKIN/128. Although the outputs of each channel are transmitted at different times, the two words in a L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high the analog circuitry is in power-down mode. It also causes the analog section to reset the clock output (ACLKA). APD is normally connected to DPD when using the power down feature.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 L/$\overline{R}$ periods (85.33 ms with a 6.144 MHz clock). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.

Digital Outputs

ACLKA - Analog Section Output Clock, PIN 22.

This clock is CLKIN/2. It is used by the digital section to clock in the modulator output data. ACLKA must be connected to DCLKA. The phase of ACLKA may be reset by using APD.

SDATA - Serial Data Output, PIN 16.

Data bits are presented MSB first, in 2's complement format.

DCAL - Digital Calibrate Output, PIN 9.

This pin rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 $L/\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 6.144 MHz CLKIN). May be connected to ACAL. (See Figure 3)

Miscellaneous

NC - No Connection, PINS 8,21.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST1, TST2, TST3 -Test Inputs, PINS 11, 12, 13.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error -The deviation of the gain value from the typical number given in the analog specifications table.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

Differential Non-Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

REFERENCES

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Ordering Guide

Model	Resolution	Filter Enters Stopband	Temperature	Package
CS5326-KP	16-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5327-KP	16-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5328-KP	18-bits	26 kHz	0°C to 70 °C	28-pin Plastic DIP
CS5329-KP	18-bits	24 kHz	0°C to 70 °C	28-pin Plastic DIP

CDB5326	CS5326 Evaluation Board
CDB5327	CS5327 Evaluation Board
CDB5328	CS5328 Evaluation Board
CDB5329	CS5329 Evaluation Board

•Notes•

Semiconductor Corporation

CS5336 CS5337
CS5338 CS5339

16-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Low Noise and Distortion >90 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 400 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

The CS5336, CS5337, CS5338 & CS5339 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

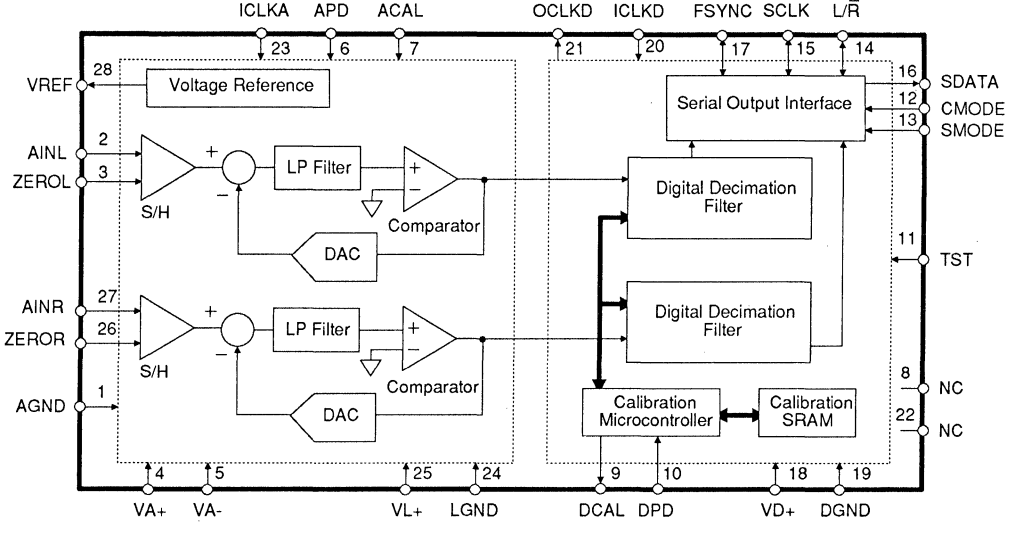
The ADCs use delta-sigma modulation with 64X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5336 & CS5338 have an SCLK which clocks out data on rising edges. The CS5337 & CS5339 have an SCLK which clocks out data on falling edges.

The CS5336 & CS5337 have a filter passband of dc to 22kHz. The CS5338 & CS5339 have a filter passband of dc to 24 kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package.

ORDERING INFORMATION: See Page 3-258



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VL+,VD+ = 5V; VA- = -5V; Full-Scale Input Sinewave, 1kHz; Output word rate = 48 kHz; SCLK = 3.072 MHz; Source Impedance = 50Ω with 10 nF to AGND; Measurement Bandwidth is 10 Hz to 20 kHz; unless otherwise specified.)

Parameter*	Symbol	Specification min	typ	max	Units
Resolution		16			Bits
Dynamic Performance					
Dynamic Range		92.7	95.7		dB
Signal-to-(Noise + Distortion); THD+N	S/(N+D)	90.7	92.7		dB
Total Harmonic Distortion Vin = -10 dB	THD		0.001		%
Interchannel Phase Deviation			0.0001		Degrees
Interchannel Isolation (dc to 20 kHz)		100	106		dB
dc Accuracy					
Interchannel Gain Mismatch			0.01	0.05	dB
Gain Error			± 1	± 5	%
Gain Drift (Note 1)			50	150	ppm/ ^{o} C
Bipolar Offset Error (After Calibration)			± 5	± 10	LSB
Analog Input					
Input Voltage Range (± Full Scale)	VIN	± 3.50	± 3.68		Volts
Input Impedance	ZIN		65		kΩ
Power Supplies					
Power Supply Current (VA+) + (VL+)	IA+		25	TBD	mA
with APD,DPD low VA-	IA-		25	TBD	mA
(Normal Operation) VD+	ID+		30	TBD	mA
Power Supply Current (VA+) + (VL+)	IA+		10		uA
with APD,DPD high VA-	IA-		10		uA
(Power-Down Mode) VD+	ID+		10		uA
Power Dissipation (APD, DPD Low)	PDN		400	TBD	mW
(APD, DPD High)	PDS		150		uW
Power Supply Rejection Ratio (dc to 26 kHz)	PSRR		54		dB
(26 kHz to 3.046 MHz)			100		dB

Notes: 1. This parameter is guaranteed by design and/or characterization

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

(T_A = 25 ° C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%; Output word rate of 48 kHz)

Parameter			Symbol	Min	Typ	Max	Units
Passband	(-3 dB)	CS5336, CS5337		0	to	22	kHz
	(-3 dB)	CS5338, CS5339		0	to	24	kHz
	(-0.01 dB)	CS5336, CS5337		0	to	20	kHz
	(-0.01 dB)	CS5338, CS5339		0	to	22	kHz
Passband Ripple				-	-	± 0.01	dB
Stopband		CS5336, CS5337		26	to	3046	kHz
		CS5338, CS5339		28	to	3044	kHz
Stopband Attenuation		(Note 2)		80	-	-	dB
Group Delay (OWR = Output Word Rate)			t_{gd}	-	18/OWR	-	s
Group Delay Variation vs. Frequency			$\triangle t_{gd}$	-	-	0.0	us

Notes: 2. The analog modulator samples the input at 3.072MHz for an output word rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (that is: there is no rejection for n x 3.072MHz ±22kHz for the CS5338 & CS5339, or n x 3.072MHz ±20.0kHz for the CS5336 & CS5337 , where n = 0,1,2,3...).

3

DIGITAL CHARACTERISTICS

(T_A = 25 °C; VA+, VL+ ,VD+ = 5V ± 5%; VA- = -5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%VD+	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	30% VD+	V
High-Level Output Voltage at Io = -20uA	V_{OH}	4.4	-	-	V
Low-Level Output Voltage at Io = 20uA	V_{OL}	-	-	0.1	V
Input Leakage Current	Iin	-	1.0	-	uA

ABSOLUTE MAXIMUM RATINGS (AGND, LGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Analog	VA+	-0.3	+6.0	V
	Negative Analog	VA-	+0.3	-6.0	V
	Positive Logic	VL+	-0.3	(VA+) + 0.3	V
	Positive Digital	VD+	-0.3	+6.0	V
Input Current, Any Pin Except Supplies		I_{in}	-	± 10	mA
Analog Input Voltage (AIN and ZERO pins)		V_{INA}	(VA-)- 0.3	(VA+)+ 0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Temperature (power applied)		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

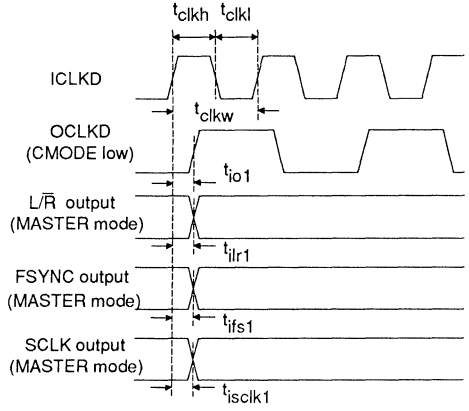
WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

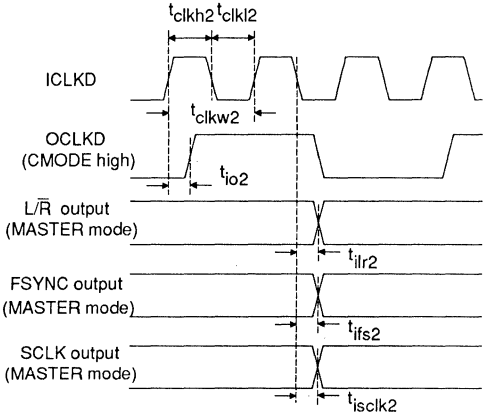
(T_A = 25 °C; VA+, VL+, VD+ = 5V ± 5%; VA- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
ICLKD Period (CMODE low)	t_{clkw1}	78	-	3906	ns
ICLKD Low (CMODE low)	t_{clkl1}	31	-	-	ns
ICLKD High (CMODE low)	t_{clkh1}	31	-	-	ns
ICLKD rising to OCLKD rising (CMODE low)	t_{io1}	5	-	40	ns
ICLKD Period (CMODE high)	t_{clkw2}	52	-	2604	ns
ICLKD Low (CMODE high)	t_{clkl2}	20	-	-	ns
ICLKD High (CMODE high)	t_{clkh2}	20	-	-	ns
ICLKD rising or falling to OCLKD rising (CMODE high, Note 3)	t_{io2}	5	-	45	ns
ICLKD rising to L/$\overline{R}$ edge (CMODE low, MASTER mode)	t_{ilr1}	5	-	50	ns
ICLKD rising to FSYNC edge (CMODE low, MASTER mode)	t_{ifs1}	5	-	50	ns
ICLKD rising to SCLK edge (CMODE low, MASTER mode)	t_{isclk1}	5	-	50	ns
ICLKD falling to L/$\overline{R}$ edge (CMODE high, MASTER mode)	t_{ilr2}	5	-	50	ns
ICLKD falling to FSYNC edge (CMODE high, MASTER mode)	t_{ifs2}	5	-	50	ns
ICLKD falling to SCLK edge (CMODE high, MASTER mode)	t_{isclk2}	5	-	50	ns
SCLK rising to SDATA valid (MASTER mode, Note 4)	t_{sdo}	0	-	50	ns
SCLK duty cycle (MASTER mode)		40	50	60	%
SCLK rising to L/$\overline{R}$ (MASTER mode, Note 4)	t_{mslr}	-20	-	20	ns
SCLK rising to FSYNC (MASTER mode, Note 4)	t_{msfs}	-20	-	20	ns
SCLK Period (SLAVE mode)	t_{sclkw}	155	-	-	ns
SCLK Pulse Width Low (SLAVE mode)	t_{sclkl}	60	-	-	ns
SCLK Pulse Width High (SLAVE mode)	t_{sclkh}	60	-	-	ns
SCLK rising to SDATA valid (SLAVE mode, Note 4)	t_{dss}	-	-	50	ns
L/$\overline{R}$ edge to MSB valid (SLAVE mode)	t_{lrdss}	-	-	50	ns
Falling SCLK to L/$\overline{R}$ edge delay (SLAVE mode, Note 4)	t_{slr1}	30	-	-	ns
L/$\overline{R}$ edge to falling SCLK setup time (SLAVE mode, Note 4)	t_{slr2}	30	-	-	ns
Falling SCLK to rising FSYNC delay (SLAVE mode, Note 4)	t_{sfs1}	30	-	-	ns
Rising FSYNC to falling SCLK setup time (SLAVE mode, Note 4)	t_{sfs2}	30	-	-	ns
DPD pulse width	t_{pdw}	150	-	-	ns
DPD rising to DCAL rising	t_{pcr}	-	-	50	ns
DPD falling to DCAL falling (OWR = Output Word Rate)	t_{pcf}		4096		1/OWR

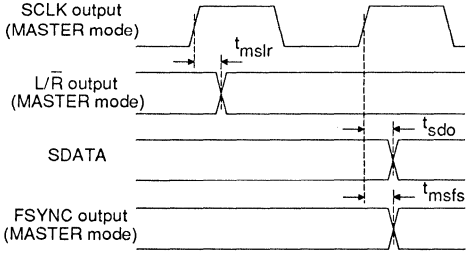
Notes: 3. ICLKD rising or falling depends on DPD to L/$\overline{R}$ timing (see Figure 2).
4. SCLK is shown for CS5336, CS5338. SCLK is inverted for CS5337, CS5339.



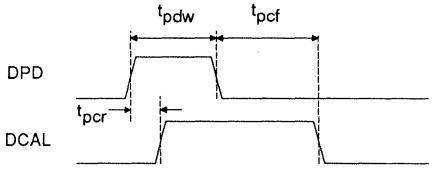
ICLKD to Outputs Propagation Delays (CMODE low)



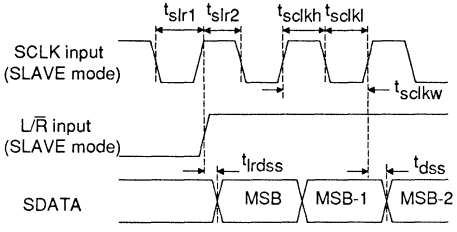
ICLKD to Outputs Propagation Delays (CMODE high)



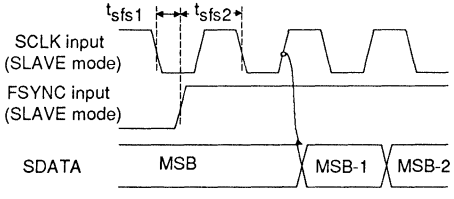
SCLK to SDATA, L/R & FSYNC - MASTER Mode



Power Down & Calibration Timing



SCLK to L/R & SDATA - SLAVE mode, FSYNC high



FSYNC to SCLK - SLAVE Mode, FSYNC Controlled.

RECOMMENDED OPERATING CONDITIONS

(AGND, LGND, DGND = 0V; all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	VA+	V
	Positive Logic	VL+	4.75	5.0	VA+	V
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	−4.75	−5.0	−5.25	V
Analog Input Voltage	(Note 5)	V_{AIN}	−3.68	-	3.68	V

Notes: 5. The ADCs accept input voltages up to the analog supplies (VA+, VA-). They will produce a positive full-scale output for inputs above 3.68 V and negative full-scale output for inputs below -3.68 V. These values are subject to the gain error tolerance specification. Additional tag bits are output to indicate the amount of overdrive.

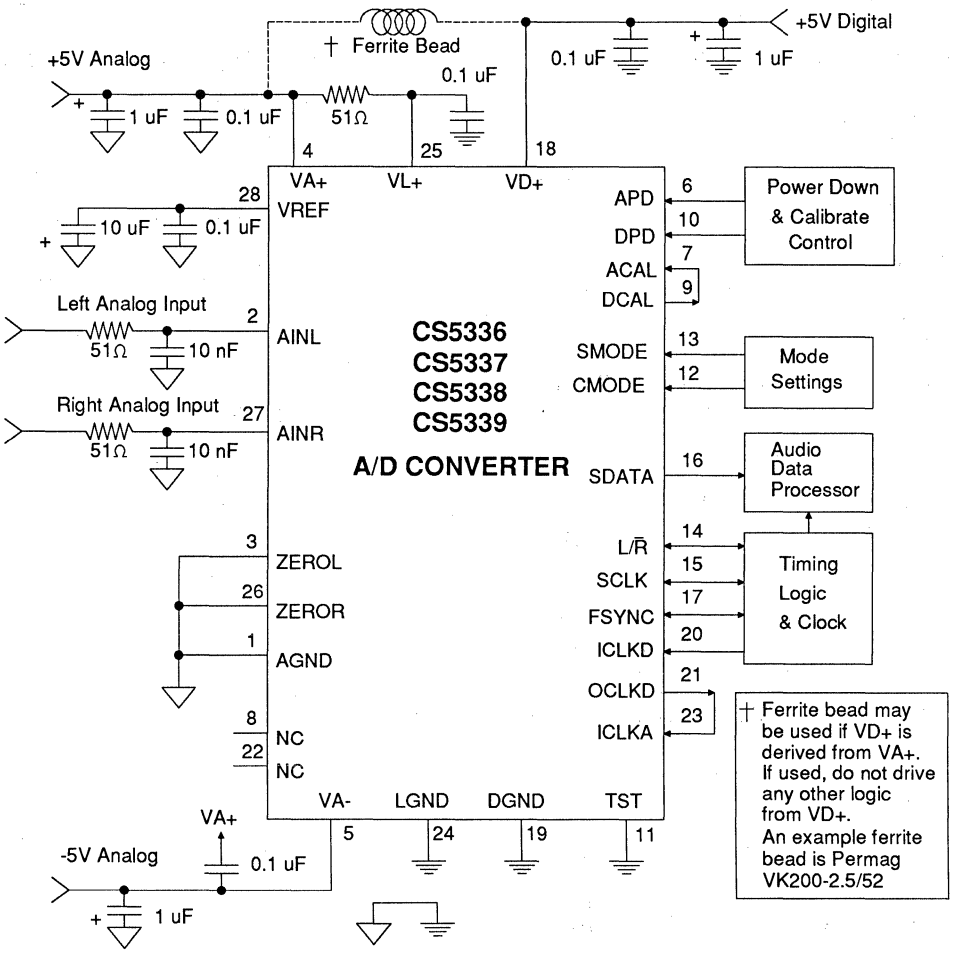


Figure 1. Typical Connection Diagram

GENERAL DESCRIPTION

The CS5336, CS5337, CS5338 and CS5339 are 16-bit, 2-channel A/D converters designed specifically for stereo digital audio applications. The devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at a 64 X sampling rate. The resulting serial bit streams are digitally filtered, yielding pairs of 16-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converters do not require difficult-to-design or expensive anti-alias filters, and do not require external sample-and-hold amplifiers or a voltage reference.

An on-chip voltage reference provides for an input signal range of ± 3.68 volts. Any zero offset is internally calibrated out during a power-up self-calibration cycle. Output data is available in serial form, coded as 2's complement 16-bit numbers. Typical power consumption of only 400 mW can be further reduced by use of the power-down mode.

For more information on delta-sigma modulation and the particular implementation inside these ADCs, see the references at the end of this data sheet.

L/$\overline{R}$ (kHz)	CMODE	ICLKD (MHz)	OCLKD/ ICLKA (MHz)	SCLK (MHz)
32	low	8.192	4.096	2.048
32	high	12.288	4.096	2.048
44.1	low	11.2896	5.6448	2.8224
44.1	high	16.9344	5.6448	2.8224
48	low	12.288	6.144	3.072
48	high	18.432	6.144	3.072

Table 1. Common Clock Frequencies

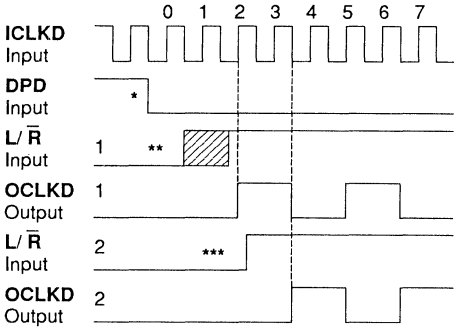
SYSTEM DESIGN

Very few external components are required to support the ADC. Normal power supply decoupling components, voltage reference bypass capacitors and a single resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

Master Clock Input

The master input clock (ICLKD) into the ADC runs the digital filter, and is used to generate the modulator sampling clock. ICLKD frequency is determined by the desired Output Word Rate (OWR) and the setting of the CMODE pin. CMODE high will set the required ICLKD frequency to 384 X OWR, while CMODE low will set the required ICLKD frequency to 256 X OWR. Table 1 shows some common clock frequencies. The digital output clock (OCLKD) is always equal to 128 X OWR, which is always 2 X the input sample rate. OCLKD should be connected to ICLKA, which controls the input sample rate.

The phase alignment betwen ICLKD and OCLKD is determined as follows: when CMODE



* DPD low is recognized on the next ICLKD rising edge (#0)
** L/$\overline{R}$ rising before ICLKD rising #2 causes OCLKD -1
*** L/$\overline{R}$ rising after ICLKD rising #2 causes OCLKD - 2

Figure 2. ICLKD to OCLKD Timing with CMODE high (384 X OWR)

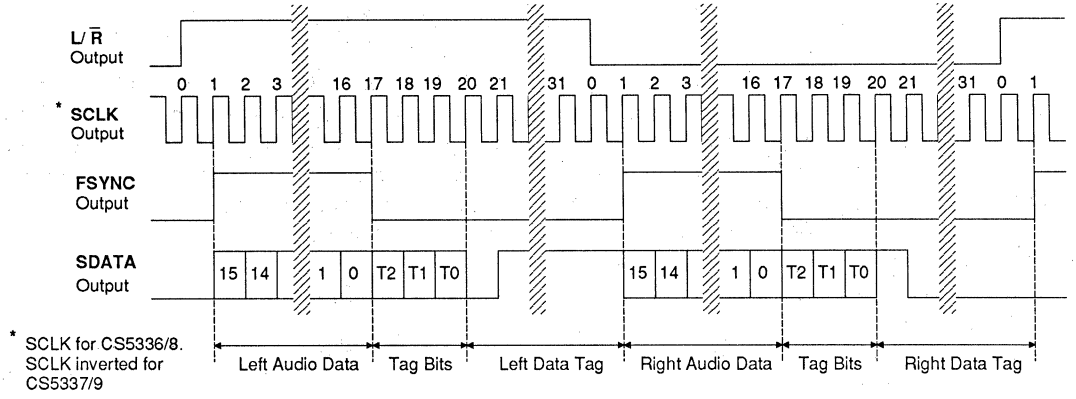


Figure 3. Data Output Timing - MASTER mode

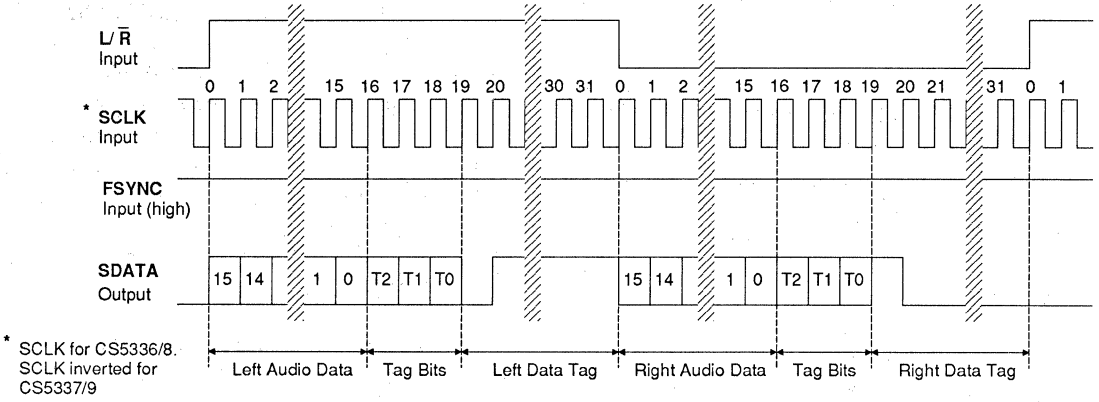


Figure 4. Data Output Timing - SLAVE Mode, FSYNC high

is low, ICLKD is divided by 2 to generate OCLKD. The phase relationship between ICLKD and OCLKD is always the same, and is shown in the Switching Characteristics Timing Diagrams. When CMODE is high, OCLKD is ICLKD divided by 3. There are two possible phase relationships between ICLKD and OCLKD, which depend on the start-up timing between DPD and L/$\overline{R}$, shown in Figure 2.

Serial Data Interface

The serial data output interface has 3 possible modes of operation: MASTER mode, SLAVE mode with FSYNC high, and SLAVE mode with FSYNC controlled. In MASTER mode, the A/D converter is driven from a master clock (ICLKD) and outputs all other clocks, derived from ICLKD (see Figure 3). Notice the one SCLK cycle delay between L/$\overline{R}$ edges and FSYNC rising edges. FSYNC brackets the 16 data bits for each channel.

In SLAVE mode, L/$\overline{R}$ and SCLK are inputs. L/$\overline{R}$ must be externally derived from ICLKD, and should be equal to the Output Word Rate. SCLK should be equal to the input sample rate, which is equal to OCLKD/2. Other SCLK frequencies are possible, but may degrade dynamic range because of interference effects. Data bits are clocked out via the SDATA pin using the SCLK and L/$\overline{R}$ inputs. The rising edge of SCLK causes the ADC to

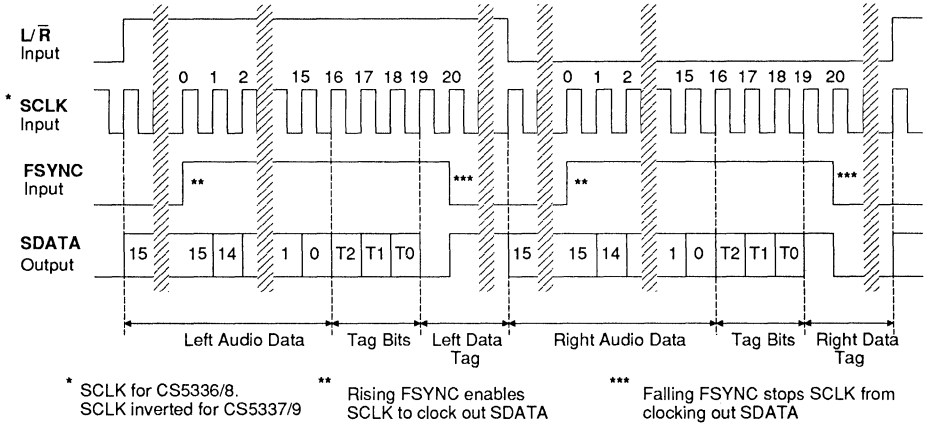


Figure 5. Data Output Timing - SLAVE Mode, FSYNC controlled

3

output each bit, except the MSB, which is clocked out by the L/$\overline{R}$ edge. As shown in Figure 4, when FSYNC is high, serial data bits are clocked immediately following the L/$\overline{R}$ edge.

In SLAVE mode with FSYNC controlled, as shown in Figure 5, when FSYNC is low, only the MSB is clocked out after the L/$\overline{R}$ edge. With FSYNC low, SCLK is ignored. When it is desired to start clocking out data, bring FSYNC high which enables SCLK to start clocking out data. Bringing FSYNC low will stop the data being clocked out. This feature is particularly useful to position in time the data bits onto a common serial bus.

The serial nature of the output data results in the left and right data words being read at different times. However, the words within an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

In all modes, additional bits are output after the data bits: 3 tag bits and a left/right indicator. The tag bits indicate a near-to-clipping input condition for the data word to which the tag bits are attached. Table 2 shows the relationship between input level and the tag bit values. The serial bit immediately following the tag bits is 0 for the left channel, and 1 for the right channel. The remaining bits before the next L/$\overline{R}$ edge will be 1's for the left channel and 0's for the right channel. Normally, the tag bits are separated from the audio data by the digital signal processor. However, if the tag bits are interpreted as audio data, their position below the LSB would result as a very small dc offset.

In all modes, SCLK is shown for the CS5336 and CS5338, where data bits are clocked out on rising edges. SCLK is inverted for the CS5337 and the CS5339.

Input Level	T2	T1	T0
1.375 x FS	1	1	1
1.250 x FS to 1.375 x FS	1	1	0
1.125 x FS to 1.250 x FS	1	0	1
1.000 x FS to 1.125 x FS	1	0	0
-1.006dB to 0.000dB	0	1	1
-3.060dB to -1.006dB	0	1	0
-6.000dB to -3.060dB	0	0	1
< -6.000dB	0	0	0

FS = Full Scale (0dB) Input

Table 2. Tag Bit Definition

Certain serial modes align well with various interface requirements. A CS5337 in MASTER mode, with an inverted L/$\overline{R}$ signal, generates I^2S (Philips) compatible timing. A CS5336 in MASTER mode, using FSYNC, interfaces well with a Motorola DSP56000. A CS5336 in SLAVE mode emulates a CS5326 style interface, and also links up to a DSP56000 in network mode.

Analog Connections

The analog inputs are presented to the modulators via the AINR and AINL pins. The analog input signal range is determined by the internal voltage reference value, which is typically -3.68 volts. The input signal range therefore is typically ± 3.68 volts.

The ADC samples the analog inputs at 3.072 MHz for a 12.288 MHz ICLKD (CMODE low). For the CS5336 & CS5337, the digital filter rejects all noise between 26 kHz and (3.072 MHz-26 kHz). For the CS5338 & CS5339, the digital filter rejects all noise between 28 kHz and (3.072 MHz-28 kHz). However, the filter will not reject frequencies right around 3.072 MHz (and multiples of 3.072 MHz). Most audio signals do not have significant energy at 3.072 MHz. Nevertheless, a 51 Ω resistor in series with the analog input, and a 10 nF NPO or COG capacitor to ground will attenuate any noise energy at 3.072 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient (such as general purpose ceramics) should be avoided since these can degrade signal linearity. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with output word rate.

The on-chip voltage reference output is brought out to the VREF pin. A 10 µF electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor attached to this pin eliminates the effects of high frequency noise. Note the negative value of VREF when using polarized capacitors. No load current may be taken from the VREF output pin.

The analog input level used as zero during the offset calibration period (described later) is input on the ZEROL and ZEROR pins. Typically, these pins are directly attached to AGND. For the ultimate in offset nulling, networks can be attached to ZEROR and ZEROL whose impedances match the impedances present on AINL and AINR.

Power-Down and Offset Calibration

The ADC has a power-down mode wherein typical consumption drops to 150 µW. In addition, exiting the power-down state initiates an offset calibration procedure.

APD and DPD are the analog and digital power-down pins. When high, they place the analog and digital sections in the power-down mode. Bringing these pins low takes the part out of power-down mode. DPD going low initiates a calibration cycle. If not using the power down

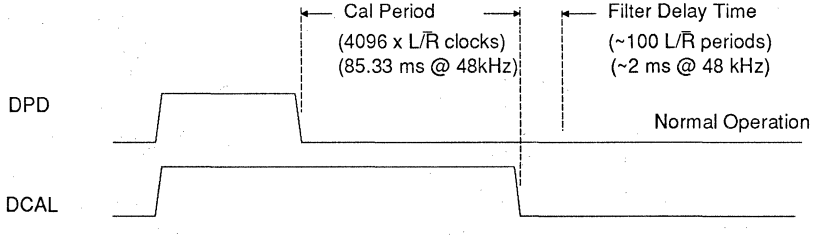


Figure 6. Initial Calibration Cycle Timing

feature, APD should be tied to AGND. When using the power down feature, DPD and APD may be tied together if the capacitor on VREF is not greater than 10 µF, as stated in the "Power-Up Considerations" section.

During the offset calibration cycle, the digital section of the part measures and stores the value of the calibration input of each channel in registers. The calibration input value is subtracted from all future outputs. The calibration input may be obtained from either the analog input pins (AINL and AINR) or the zero pins (ZEROL and ZEROR) depending on the state of the ACAL pin. With ACAL low, the analog input pin voltages are measured, and with ACAL high, the zero pin voltages are measured.

As shown in Figure 6, the DCAL output is high during calibration, which takes 4096 L/$\overline{R}$ clock cycles. If DCAL is connected to the ACAL input, the calibration routine will measure the voltage on ZEROR and ZEROL. These should be connected directly to ground or through a network matched to that present on the analog input pins. Internal offsets of each channel will thus be measured and subsequently subtracted.

Alternatively, ACAL may be permanently connected low and DCAL utilized to control a multplexer which grounds the user's front end. In this case, the calibration routine will measure and store not only the internal offsets but also any offsets present in the front end input circuitry.

During calibration, the digital output of both channels is forced to a 2's complement zero. Subtraction of the calibration input from conversions after calibration substantially reduces any power-on click that might otherwise be experienced. A short delay of approximately 100 output words will occur following calibration for the digital filter to begin accurately tracking audio band signals.

Power-up Considerations

Upon initial application of power to the supply pins, the data in the calibration registers will be indeterminate. A calibration cycle should always be initiated after application of power to replace potentially large values of data in these registers with the correct values.

The modulators settle very quickly (a matter of microseconds) after the analog section is powered on, either through the application of power, or by exiting the power-down mode. The voltage reference can take a much longer time to reach a final value due to the presence of large external capacitance on the VREF pin; allow approximately 5 ms/µF. The calibration period is long enough to allow the reference to settle for capacitor values of up to 10 µF. If a larger capacitor is used, additional time between APD going low and DPD going low should be allowed for VREF settling before a calibration cycle is initiated.

Grounding and Power Supply Decoupling

As with any high resolution converter, the ADC requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA+, VA- and VL+ connected to a clean ±5 V supply. VD+, which powers the digital filter, may be run from the system +5V logic supply, provided that it is not excessively noisy (< ± 50 mV pk-to-pk). Alternatively, VD+ may be powered from VA+ via a ferrite bead. In this case, no additional devices should be powered from VD+. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the ADC as possible, with the low value ceramic capacitor being the nearest.

The printed circuit board layout should have separate analog and digital regions and ground

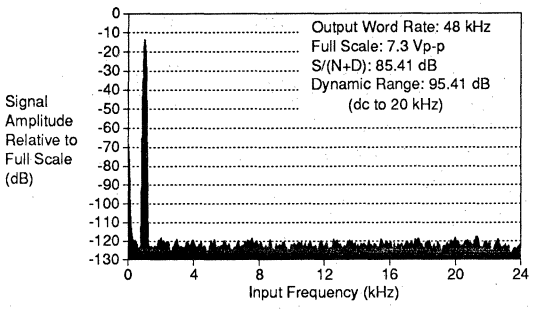


Figure 7. CS5336 FFT Plot with -10 dB, 1 kHz Input

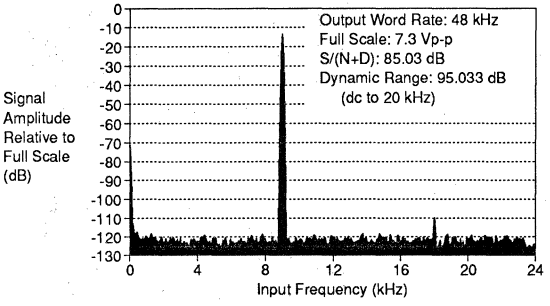


Figure 8. CS5336 FFT Plot with -10 dB, 9 kHz Input

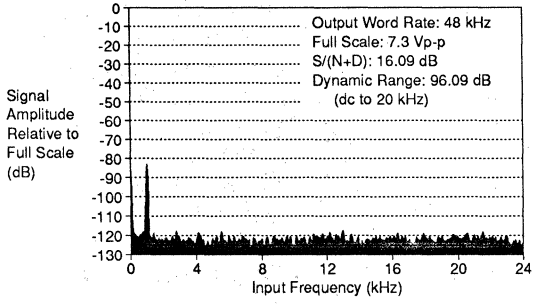


Figure 9. CS5336 FFT Plot with -80 dB, 1 kHz Input

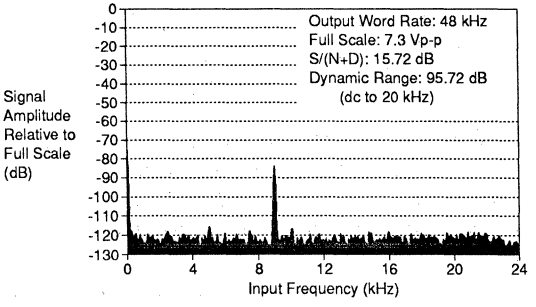


Figure 10. CS5336 FFT Plot with -80 dB, 9 kHz Input

planes, with the ADC straddling the boundary. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the modulators. An evaluation board is available which demonstrates the optimum layout and power supply arrangements, as well as allowing fast evaluation of the ADC.

To minimize digital noise, connect the ADC digital outputs only to CMOS inputs.

PERFORMANCE

FFT Tests

For FFT based tests, a very pure sine wave is presented to the ADC, and an FFT analysis is performed on the output data. The resulting spectrum is a measure of the performance of the ADC.

Figure 7 shows the spectral purity of the CS5336 with a 1 kHz, -10 dB input. Notice the low noise floor, the absence of any harmonic distortion, and the Dynamic Range value of 95.41 dB.

Figure 8 shows the CS5336 high frequency performance. The input signal is a -10 dB, 9 kHz sine wave. Notice the small 2nd harmonic at 110 dB down.

Figure 9 shows the low-level performance of the CS5336. Notice the lack of any distortion components. Traditional R-2R ladder based ADC's can have problems with this test, since differential non-linearities around the zero point become very significant. Figure 10 shows the same very

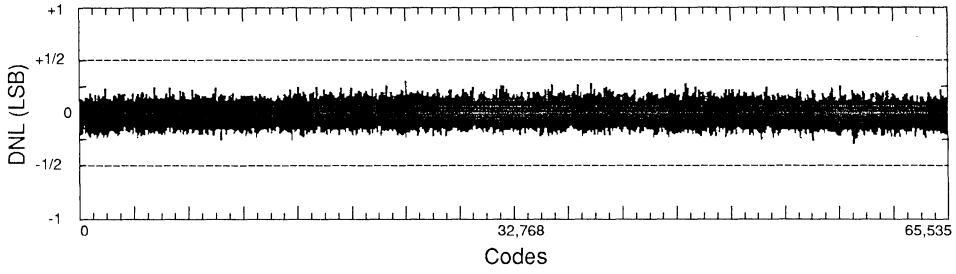


Figure 11. CS5336 Differential Non-Linearity Plot

low input amplitude performance, but at 9kHz input frequency.

DNL Tests

A Differential Non-Linearity test is also shown. Here, the converter is presented with a linear ramp signal. The resulting output codes are counted to yield a number which is proportional to the codewidth. A plot of codewidth versus code graphically illustrates the uniformity of the codewidths. Figure 11 shows the excellent Differential Non-Linearity of the CS5336. This plot displays the worst case positive and negative errors in each of 512 groups of 128 codes. Codewidths typically are within ± 0.2 LSB's of ideal. A delta-sigma modulator based ADC has no inherent mechanism for generating DNL errors. The residual small deviations shown in Figure 11 are a result of noise. Nevertheless, the performance shown is extremely good, and is superior to typical R-2R ladder based designs.

Digital Filter

Figures 12 through 17 show the performance of the digital filter included in the ADC. All the plots assume an output word rate of 48 kHz. The filter frequency response will scale precisely with changes in output word rate. The passband ripple is flat to ± 0.01 dB maximum. Stopband rejection is greater than 80 dB.

Figures 12,14 &16 show the CS5338 and CS5339 filter characteristics. Figure 16 is an expanded view of the transition band.

Figures 13,15 & 17 show the CS5336 and CS5337 filter characteristics. Figure 17 is an expanded view of the transition band.

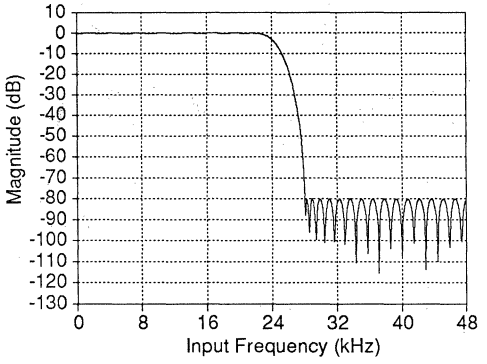


Figure 12. CS5338/9 Digital Filter Stopband Rejection

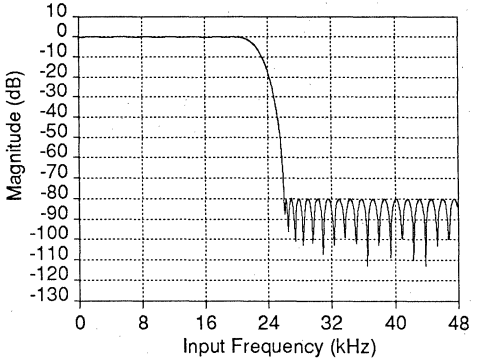


Figure 13. CS5336/7 Digital Filter Stopband Rejection

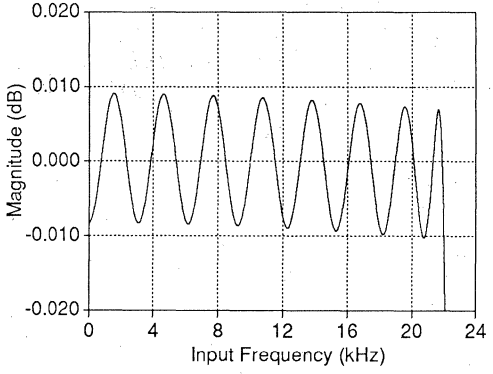


Figure 14. CS5338/9 Digital Filter Passband Ripple

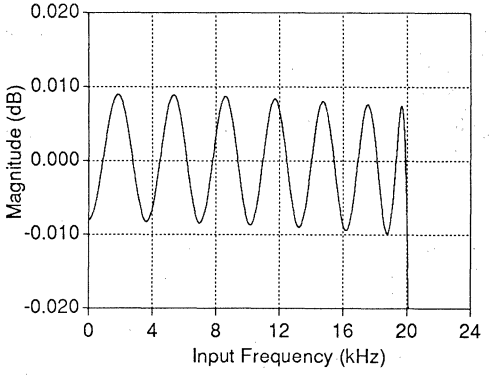


Figure 15. CS5336/7 Digital Filter Passband Ripple

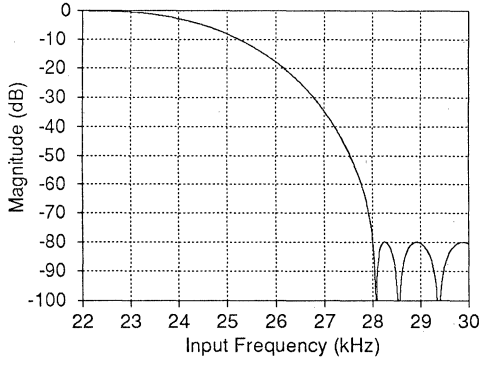


Figure 16. CS5338/9 Digital Filter Transition Band

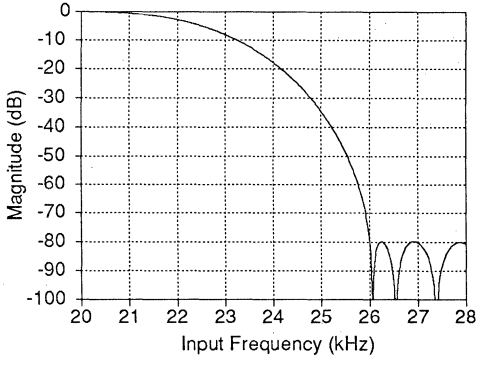
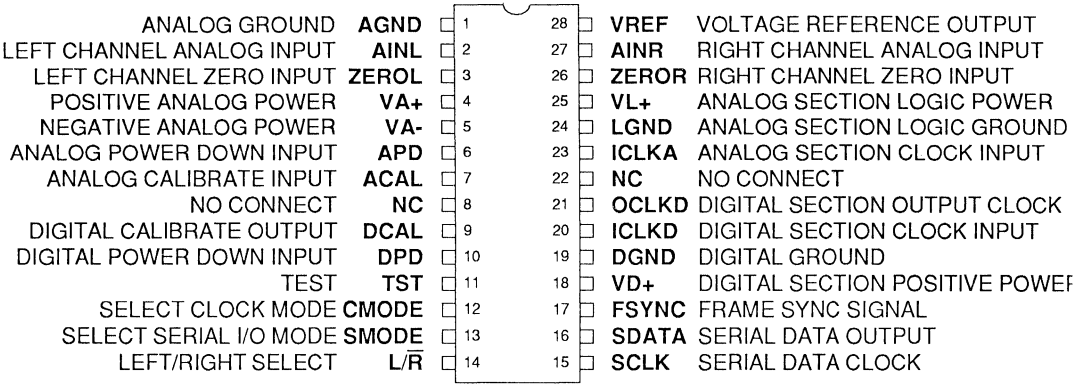


Figure 17. CS5336/7 Digital Filter Transition Band

PIN DESCRIPTIONS



3

Power Supply Connections

VA+ - Positive Analog Power, PIN 4.
Positive analog supply. Nominally +5 volts.

VL+ - Positive Logic Power, PIN 25.
Positive logic supply for the analog section. Nominally +5 volts.

VA- - Negative Analog Power, PIN 5.
Negative analog supply. Nominally -5 volts.

AGND - Analog Ground, PIN 1.
Analog ground reference.

LGND - Logic Ground, PIN 24
Ground for the logic portions of the analog section.

VD+ - Positive Digital Power, PIN 18.
Positive supply for the digital section. Nominally +5 volts.

DGND - Digital Ground, PIN 19.
Digital ground for the digital section.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 2, 27
Analog input connections for the left and right input channels. Nominally ±3.68 volts full scale.

ZEROL, ZEROR - Zero Level Inputs for Left and Right Channels, PINS 3, 26.

Analog zero level inputs for the left and right channels. The levels present on these pins can be used as zero during the offset calibration cycle. Normally connected to AGND, optionally through networks matched to the analog input networks.

Analog Outputs

VREF - Voltage Reference Output, PIN 28.

Nominally -3.68 volts. Normally connected to a 0.1µF ceramic capacitor in parallel with a 10µF or larger electrolytic capacitor. Note the negative output polarity.

Digital Inputs

ICLKA - Analog Section Input Clock, PIN 23.

This clock is internally divided by 2 to set the modulators' sample rate. Sampling rates, output rates, and digital filter characteristics scale to ICLKA frequency. ICLKA frequency is 128 X the output word rate. For example, 6.144 MHz ICLKA corresponds to an output word rate of 48 kHz per channel. Normally connected to OCLKD.

ICLKD - Digital Section Input Clock, PIN 20.

This is the clock which runs the digital filter. ICLKD frequency is determined by the required output word rate and by the CMODE pin. If CMODE is low, ICLKD frequency should be 256 X the desired output word rate. If CMODE is high, ICLKD should be 384 X the desired output word rate. For example, with CMODE low, ICLKD should be 12.288 MHz for an output word rate of 48 kHz. This clock also generates OCLKD, which is always 128 X the output word rate.

APD - Analog Power Down, PIN 6.

Analog section power-down command. When high, the analog circuitry is in power-down mode. APD is normally connected to DPD when using the power down feature. If power down is not used, then connect APD to AGND.

DPD - Digital Power Down, PIN 10

Digital section power-down command. Bringing DPD high puts the digital section into power-down mode. Upon returning low, the ADC starts an offset calibration cycle. This takes 4096 $L/\overline{R}$ periods (85.33 ms with a 12.288 MHz ICLKD). DCAL is high during the calibrate cycle and goes low upon completion. DPD is normally connected to APD when using the power down feature. A calibration cycle should always be initiated after applying power to the supply pins.

ACAL - Analog Calibrate, PIN 7.

Analog section calibration command. When high, causes the left and right channel modulator inputs to be internally connected to ZEROL and ZEROR inputs respectively. May be connected to DCAL.

CMODE - Clock Mode Select, PIN 12.

CMODE should be tied low to select an ICLKD frequency of 256 X the output word rate. CMODE should be tied high to select an ICLKD frequency of 384 X the output word rate.

SMODE - Serial Interface Mode Select, PIN 13.

SMODE should be tied high to select serial interface master mode, where SCLK, FSYNC and L/$\overline{R}$ are all outputs, generated by internal dividers operating from ICLKD. SMODE should be tied low to select serial interface slave mode, where SCLK, FSYNC and L/$\overline{R}$ are all inputs. In slave mode, L/$\overline{R}$, FSYNC and SCLK need to be derived from ICLKD using external dividers.

Digital Outputs

SDATA - Serial Data Output, PIN 16.

Audio data bits are presented MSB first, in 2's complement format. Additional tag bits, which indicate input overload and left/right channel data, are output immediately following each audio data word.

DCAL - Digital Calibrate Output, PIN 9.

DCAL rises immediately upon entering the power-down state (DPD brought high). It returns low 4096 L/$\overline{R}$ periods after leaving the power down state (DPD brought low), indicating the end of the offset calibration cycle (which = 85.33 ms with a 12.288 MHz ICLKD). May be connected to ACAL.

OCLKD - Digital Section Output Clock, PIN 21.

OCLKD is always 128 X the output word rate. Normally connected to ICLKA.

Digital Inputs or Outputs

SCLK - Serial Data Clock, PIN 15.

Data is clocked out on the rising edge of SCLK for the CS5336 and CS5338. Data is clocked out on the falling edge of SCLK for the CS5337 and CS5339.

In master mode (SMODE high), SCLK is a continuous output clock at 64 X the output word rate.

In slave mode (SMODE low), SCLK is an input, which requires a continuously supplied clock at any frequency from 32 X to 128 X the output word rate (64 X is preferred). When FSYNC is high, SCLK clocks out serial data, except for the MSB which appears on SDATA when L/$\overline{R}$ changes.

L/$\overline{R}$ - Left/Right Select, PIN 14.

In master mode (SMODE high), L/$\overline{R}$ is an output whose frequency is at the output word rate. L/$\overline{R}$ edges occur 1 SCLK cycle before FSYNC rises. When L/$\overline{R}$ is high, left channel data is on SDATA, except for the first SCLK cycle. When L/$\overline{R}$ is low, right channel data is on SDATA, except for the first SCLK cycle. The MSB data bit appears on SDATA one SCLK cycle after L/$\overline{R}$ changes.

In slave mode (SMODE low), L/$\overline{R}$ is an input which selects the left or right channel for output on SDATA. The rising edge of L/$\overline{R}$ starts the MSB of the left channel data. L/$\overline{R}$ frequency must be equal to the output word rate.

Although the outputs of each channel are transmitted at different times, the two words in an L/$\overline{R}$ cycle represent simultaneously sampled analog inputs.

FSYNC - Frame Synchronization Signal, PIN 17.

In master mode (SMODE high), FSYNC is an output which goes high coincident with the start of the first SDATA bit (MSB) and falls low immediately after the last SDATA audio data bit (LSB).

In slave mode (SMODE low), FSYNC is an input which controls the clocking out of the data bits on SDATA. FSYNC is normally tied high, which causes the data bits to be clocked out immediately following L/$\overline{R}$ transitions. If it is desired to delay the data bits from the L/$\overline{R}$ edge, then FSYNC must be low during the delay period. Bringing FSYNC high will then enable the clocking out of the SDATA bits. Note that the MSB will be clocked out based on the L/$\overline{R}$ edge, independent of the state of FSYNC.

Miscellaneous

NC - No Connection, PINS 8, 22.

These two pins are bonded out to test outputs. They must not be connected to any external component or any length of PC trace.

TST -Test Input, PIN 11.

Allows access to the ADC test modes, which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Resolution - The total number of possible output codes is equal to 2^N, where N = the number of bits in the output word for each channel.

Dynamic Range - Full scale (RMS) signal to broadband noise ratio. The broadband noise is measured over the specified bandwidth, and with an input signal 60dB below full-scale. Units in decibels.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Interchannel Phase Deviation - The difference between the left and right channel sampling times.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation of the gain value from the typical number given in the analog specifications table.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

Bipolar Offset Error - The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSBs.

REFERENCES

1) "A Stereo 16-bit Delta-Sigma A/D Converter for Digital Audio" by D.R. Welland, B.P. Del Signore, E.J. Swanson, T. Tanaka, K. Hamashita, S. Hara, K. Takasuka. Paper presented at the 85th Convention of the Audio Engineering Society, November 1988.

2) " The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's" by Steven Harris. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

3) " An 18-Bit Dual-Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example" by Clif Sanchez. Paper presented at the 87th Convention of the Audio Engineering Society, October 1989.

Ordering Guide

Model	Resolution	Passband	SCLK	Temperature	Package
CS5336-KP	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5337-KP	16-bits	22 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5338-KP	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin Plastic DIP
CS5339-KP	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin Plastic DIP
CS5336-KS	16-bits	22 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5337-KS	16-bits	22 kHz	↓ active	0°C to 70 °C	28-pin SOIC
CS5338-KS	16-bits	24 kHz	↑ active	0°C to 70 °C	28-pin SOIC
CS5339-KS	16-bits	24 kHz	↓ active	0°C to 70 °C	28-pin SOIC

CDB5336	CS5336 Evaluation Board
CDB5337	CS5337 Evaluation Board
CDB5338	CS5338 Evaluation Board
CDB5339	CS5339 Evaluation Board

Semiconductor Corporation

CS5412

12-Bit, 1MHz Self-Calibrating A/D Converter

Features

- Monolithic CMOS Sampling ADC
  On-Chip Track and Hold Amplifier
  Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  Typical Nonlinearity: 3/4 LSB
  No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 750mW

General Description

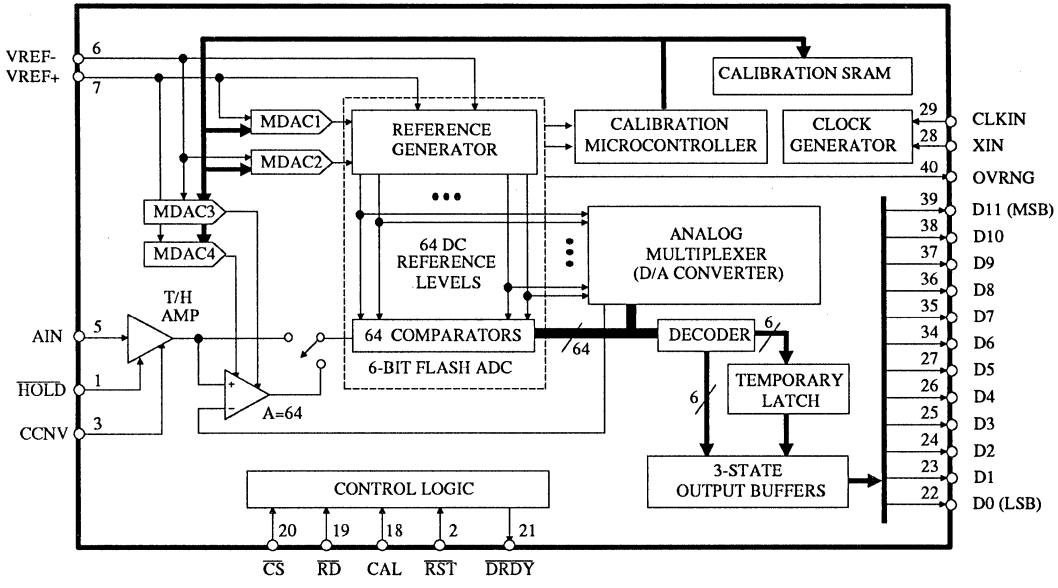
The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acqusition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

ORDERING INFORMATION: Page 3-277



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = 25°C (Note 1); All VA+ pins, VD+ = 5V; All VA- pins, VD- = -5V; VREF+ = +1.5V; VREF- = -1.5V; f_{CLK} = 8MHz for -1; 100 kHz Full Scale Input Sinewave; Continuous Convert Mode unless otherwise specified).

Parameter*	CS5412-J,K min	CS5412-J,K typ	CS5412-J,K max	CS5412-A,B min	CS5412-A,B typ	CS5412-A,B max	CS5412-S,T min	CS5412-S,T typ	CS5412-S,T max	Units
Resolution T_{min} to T_{max}	12			12			12			Bits
Specified Temperature Range		0 to 70			-40 to +85			-55 to +125		°C
Dynamic Performance										
Peak Harmonic or Spurious Noise (Note 1) T_{min} to T_{max} 100kHz Input	75	82		75	82		75	82		dB
490kHz Input		70			70			70		
Total Harmonic Distortion		0.0125			0.0125			0.0125		%
Signal-to-(Noise plus Distortion)(Note 1) 0dB Input (Full Scale) T_{min} to T_{max} -J,A,S	65	71		65	71		65	71		dB
-K,B,T	68	71		68	71		68	71		
-40dB Input		32			32			32		
dc Accuracy										
Linearity Error (Note 1) T_{min} to T_{max} -J,A,S		±3/4	±2.0		±3/4	±2.0		±1	±3.0	LSB
T_{min} to T_{max} -K,B,T		±3/4	±1.0		±3/4	±1.0		±3/4	±2.0	
Differential Linearity (Note 1) T_{min} to T_{max} -J,A,S		±1/2	NMC		±1/2	NMC		±1/2	NMC	LSB
T_{min} to T_{max} -K,B,T		±1/2	±0.9		±1/2	±0.9		±1/2	-0.9/+1.25	
Full Scale Error (Note 1) T_{min} to T_{max}		±2	±8		±2	±8		±3	±10	LSB
Offset Error (Note 1) T_{min} to T_{max}		±1.5	±3		±1.5	±3		±1.5	±4	LSB

NMC = No Missing Codes

Notes: 1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest. Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

* Refer to *Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter	CS5412-J,K min	typ	max	CS5412-A,B min	typ	max	CS5412-S,T min	typ	max	Units
Analog Input										
Aperture Time		35			35			35		ns
Aperture Jitter		50			50			50		ps, rms
Input Bandwidth										
Small Signal, -3dB (Note 2)		4			4			4		MHz
Full Power, -3dB		3.5			3.5			3.5		MHz
Analog Input Impedance at dc		10			10			10		Mohms
Input Capacitance VREF- pin		50			50			50		pF
AIN, VREF+ pins		10			10			10		pF
Conversion & Throughput										
Conversion Time (Notes 3, 4)	1.25		1.375	1.25		1.375	1.25		1.375	us
Throughput Rate	1			1			1			MHz
Acquisition Time (Note 5)		400			400			400		ns
Power Supplies										
Power Supply Current (Note 6)										
I_{A+}		70	90		70	90		70	90	mA
I_{A-}		-70	-90		-70	-90		-70	-90	mA
I_{D+}		5	10		5	10		5	10	mA
I_{D-}		-5	-10		-5	-10		-5	-10	mA
Power Dissipation (Note 6)		750	1000		750	1000		750	1000	mW
Power Supply Rejection at dc										
Positive Supplies		50			50			50		dB
Negative Supplies		50			50			50		dB

Notes:
2. Input 40 dB below full scale.
3. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{DRDY}$.
4. Applies to conversions triggered externally. In Continuous Convert mode throughput proceeds at one-eighth the master clock frequency with a fixed 10 clock cycle conversion time.
5. The internal track-and-hold returns to the track mode on the fourth master clock cycle after the start of a conversion cycle. It is guaranteed to acquire a full-scale step to 12-bit accuracy while operating at full throughput.
6. All outputs unloaded. All inputs CMOS levels.

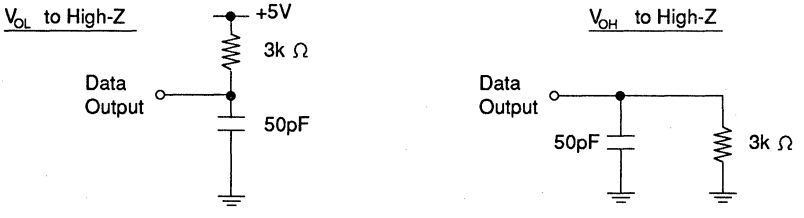
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF).

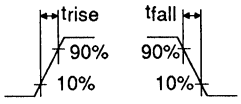
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:	f_{CLK}	3	-	8	MHz
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input (Note 7) Any Digital Output	t_{rise}	- -	- 20	1.0 -	us ns
Fall Times: Any Digital Input (Note 7) Any Digital Output	t_{fall}	- -	- 20	1.0 -	us ns
$\overline{HOLD}$/CLKIN Phase Relationship State 7 to $\overline{HOLD}$ Low $\overline{HOLD}$ Low to State 0 State 0 to $\overline{HOLD}$ High $\overline{HOLD}$ High to State 7	 t_{ha} t_{hb} t_{hc} t_{hd}	 62.5 0 75 30	 - - - -	 - - - -	 ns ns ns ns
Conversion Time (Note 8)	t_c	10	-	11	MCC*
$\overline{DRDY}$ Pulse Width	t_{dpw}	-	3	-	MCC*
Data Delay Time	t_{dd}	-	20	50	ns
Access Times: $\overline{CS}$ Low to Data Valid (Note 9) $\overline{RD}$ Low to Data Valid	t_{csa} t_{rda}	- -	55 55	110 110	ns ns
Output Float Delay: $\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	t_{fd}	-	40	110	ns
Cal Pulse Width: (Note 10) CAL high and $\overline{CS}$ Low	t_{csh}	2	-	-	MCC*
$\overline{RST}$ Pulse Width	t_{rpw}	2	-	-	MCC*

Notes: 7. $\overline{HOLD}$ and CLKIN should be driven with signals which have rise and fall times of 25 ns or faster.
8. Conversion time in the Continuous Convert mode is a fixed 10 clock cycles.
9. Data goes valid when both $\overline{CS}$ and $\overline{RD}$ are low simultaneously. Each access time assumes the other control input is already low or falls concurrently.
10. If CAL is brought low while $\overline{CS}$ is low, a calibration cycle will be initiated.

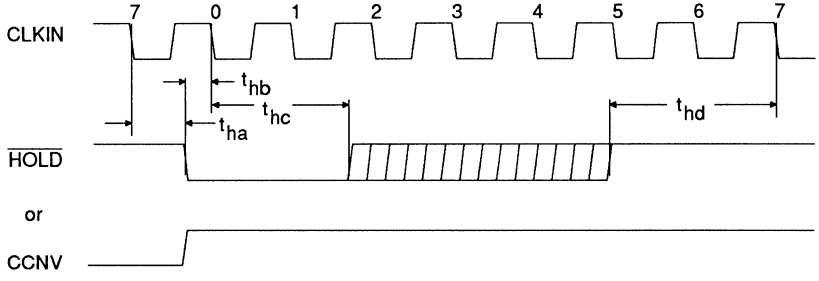
* MCC = Master Clock Cycles; 1 MCC = $1/f_{CLK}$

Float Delay Test Circuits

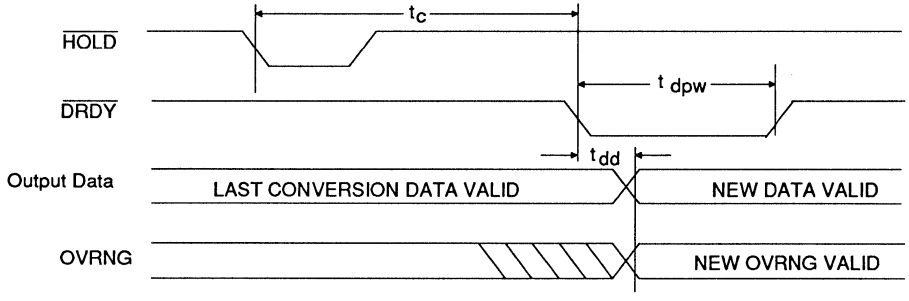




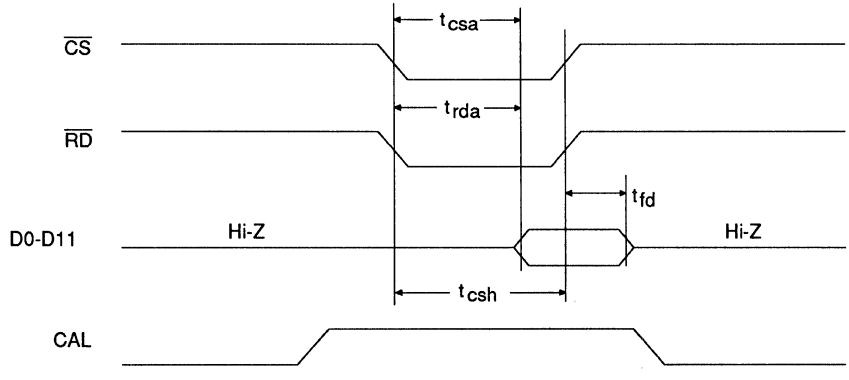
Rise and Fall Times



Hold/Master Clock Phase Relationship



Conversion Timing



Read and Calibration Control Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%) All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 11)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 11)	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 12)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-10	-	+10	uA
3-State Leakage Current	I_{OZ}	-10	-	+10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 11. All pins except HOLD and CLKIN which require inputs of V_{IL} = 0.5V and V_{IH} = VD+ - 0.5V.
12. I_{out} = -100µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 13).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.75	5.0	VA2+, VA5+	V
Negative Digital	VD-	−4.75	−5.0	−5.25	V
Positive Analog	VA1+ - VA5+	4.75	5.0	5.25	V
Negative Analog	VA1- - VA3-	−4.75	−5.0	−5.25	V
Analog Input Voltage	V_{AIN}	VREF-	-	VREF+	V
Analog Reference Voltages					
Unipolar Input Range	VREF+	2.0	-	3.0	V
	VREF-	-	AGND	-	V
Bipolar Input Range	VREF+	1.0	-	1.5	V
	VREF-	−1.0	-	−1.5	V

Notes: 13. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	VD+	−0.3	VA2+,VA5+ + 0.3	V
Negative Digital	VD-	0.3	−6.0	V
Positive Analog (Note 14)	VA1+ - VA5+	−0.3	6.0	V
Negative Analog	VA1- - VA3-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 15)	I_{in}	-	+10	mA
Analog Input Voltage (AIN and VREF pins)	V_{INA}	VA1- - VA3- - 0.3	VA2+,VA5+ + 0.3	V
Digital Input Voltage	V_{IND}	−0.3	VA2+,VA5+ + 0.3	V
Ambient Operating Temperature	T_A	−55	125	°C
Storage Temperature	T_{stg}	−65	150	°C
Junction Temperature	T_J	-	160	°C
Junction to Ambient Tempco for CLCC Package	Θ_{JA}	-	60	°C/W

Notes: 14. VA1+, VA3+, VA4+ must never exceed VA2+ and VA5+ by more than 0.3V.
15. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

To achieve high speed and high accuracy, the CS5412 implements a standard 2-step flash A/D conversion using a self-calibrating architecture. Throughput is further maximized using pipelined acquisition and settling times as well as overlapped conversion cycles.

2-Step Flash A/D Conversion

The fastest method of performing A/D conversion is the brute-force single-step flash approach, for which an N-bit conversion involves comparing the analog input to 2^N-1 graduated voltage levels. The outputs from the 2^N-1 comparators are then processed and encoded into the proper binary format. The major limitation to this technique is that the number (and accuracy requirements) of comparators doubles with each additional bit of resolution. Thus, single-step flash converters are impractical today at greater than 8 or 10 bits of resolution.

The 2-step technique that the CS5412 uses employs slightly more complex sub-circuit blocks to achieve high resolution and results in negligible speed degradation. As shown in Figure 1, the CS5412 consists of a track-and-hold amplifier (T/H_1), a 6-bit flash ADC, a 6-bit DAC, and a differential amplifier. When the convert command is issued, T/H_1 holds the analog input signal and the flash ADC converts the six MSB's (most-significant-bits) of the output word. The MSB's, once decoded, are latched. The flash converter's output is also loaded into the DAC. The DAC's output therefore represents the analog input less the quantization error of the first 6-bit flash conversion. This signal is then subtracted from the original analog input to yield the quantization error, which is then multiplied by 64 (2^6) and again applied to the flash ADC to yield the six LSB's (least-significant-bits). In effect, the first 6-bit flash forms the transfer function into 64 segments which are then filled in with 64 codes each by the second 6-bit flash. This yields a total of 4096 codes (64x64) for 12-bit resolution.

Calibration

The CS5412 uses several calibration techniques to insure 12-bit accuracy over time and temperature. A unique reference generating circuit provides the 64 graduated reference levels for the flash ADC and DAC. Critical to the CS5412's overall linearity, these references are continually adjusted to 12-bit accuracy during device operation. This background adjustment process is completely transparent to the user and results in less than ±1/2 LSB nonlinearity. Also, all comparators in the flash ADC are auto-zeroed to avoid differential linearity errors at the 64 segment boundaries due to noise and/or offsets in the comparators.

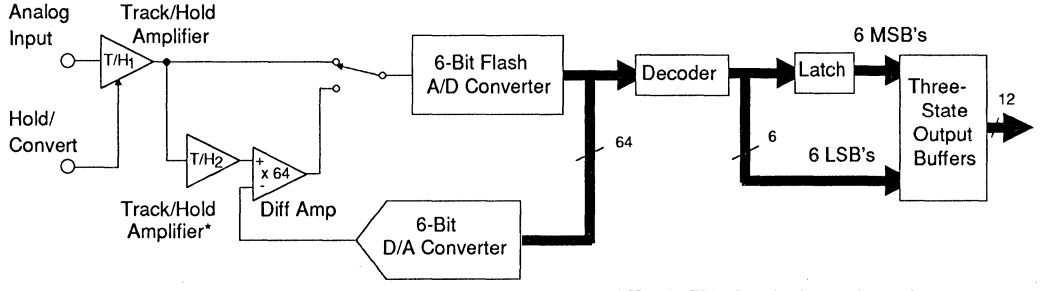


Figure 1. Block Diagram of 2-Step Flash A/D Converter

The CS5412 also uses digital correction schemes. An on-chip microcontroller manipulates dedicated MDAC's to set the gain and offset of the 6-bit flash ADC; this insures less than ±1/2 LSB overall full-scale and offset errors in the CS5412. Gain and offset are similarly calibrated in the differential amplifier to avoid linearity errors at the 64 segment boundaries.

Upon power-up, the CS5412 is reset in hardware or software to initially calibrate the device. Calibration can be similarly initiated at any later time throughout operating life to insure 12-bit accuracy independent of environmental conditions.

Pipelined Timing

To achieve throughput rates up to 1MHz, the CS5412 pipelines settling times in both the sampling and conversion processes. The CS5412 can actually begin a conversion cycle while still operating on the previous sample. As shown in Figure 2, the *Hold and Convert* command for Sample N+1 can be issued before data from Sample N is valid at the output. By definition, the throughput time of the CS5412 is shorter than the conversion time due to the overlapped conversion cycles. Compared to a non-pipelined 1MHz ADC, the CS5412 provides the same 1MHz throughput, only the output data is delayed slightly in time (1.25µs delay through the ADC rather than 1µs).

The CS5412 also uses a second track-and-hold amplifier (termed T/H_2 in Figure 3) to pipeline the converter's acquisition time. As shown in Figure 3, T/H_2 holds the output from T/H_1 valid for the second flash conversion, *Flash 2*. This allows T/H_1 to release and acquire the analog input signal during the second flash conversion, allowing another *Hold & Convert* command to be issued even before the completion of *Flash 2*.

DIGITAL CIRCUIT CONNECTIONS

In addition to master clock and sampling connections which set the converter's timing, the CS5412 offers an *Overrange* output, 3-state output buffers, and flexible control interface. The CS5412 can therefore connect directly to a microprocessor's data and control busses or can be operated in a stand-alone mode.

Master Clock

The CS5412 operates from a master clock reference which must be supplied in the form of either a crystal or external clock. A crystal can be tied across the CLKIN and XIN pins, or alternatively, the CS5412 can be synchronized to the external system by driving CLKIN with a CMOS-compatible clock (XIN left floating). If the master clock is shut off while the CS5412 is powered up, an internal oscillator will start-up to keep all in-

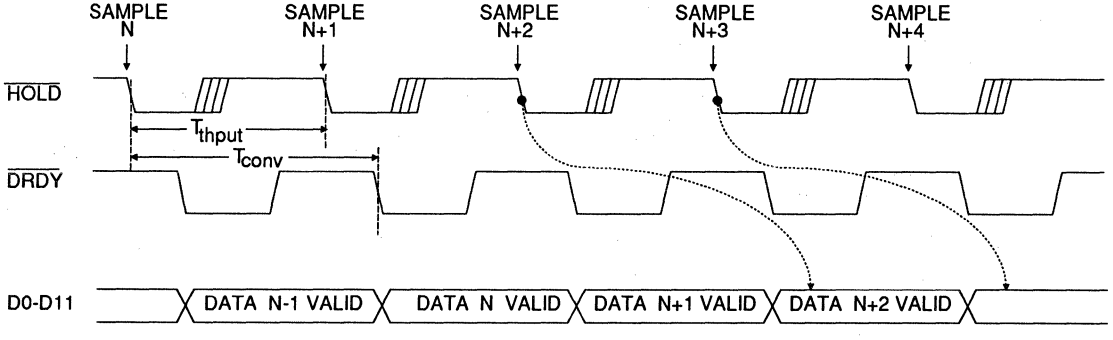


Figure 2. Pipelined Conversion Cycles

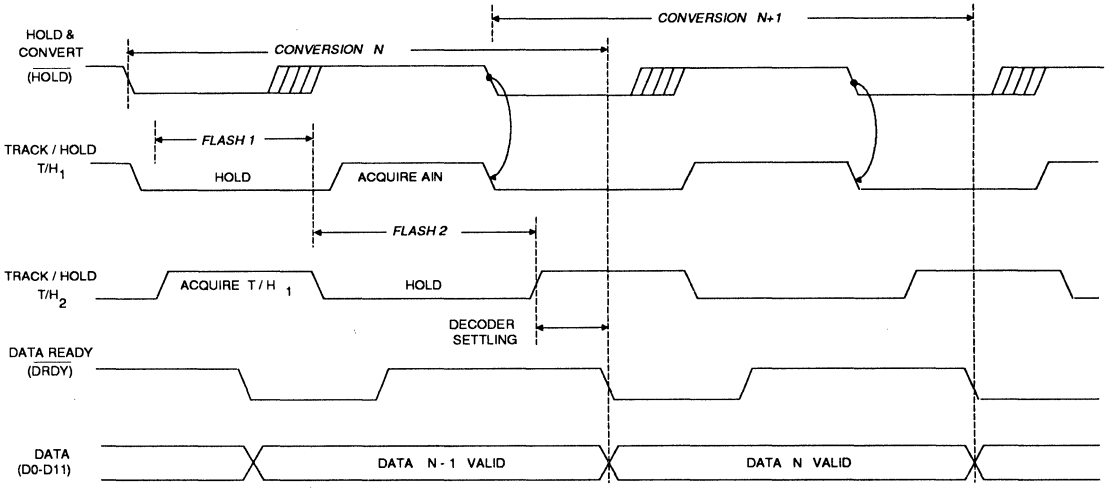


Figure 3. Pipelined Acquisition and Settling Times.

ternal dynamic logic refreshed. This internal oscillator should not be used for conversions. Clock cycles can be selectively skipped at any time, but the clock's average frequency should never drop below the device's minimum specification (see Switching Characteristics).

Sampling/Initiating Conversions

There are two methods of controlling the CS5412's sampling/conversion timing. First, the CS5412 has a $\overline{\text{HOLD}}$ input which, on a falling edge, places the input track-and-hold amplifier in the hold state and initiates a conversion cycle. The CS5412 also features a *Continuous Convert* mode (CCNV and $\overline{\text{HOLD}}$ high) in which hold commands are internally generated every eight master clock cycles. The sampling/throughput rate is therefore controlled by adjusting the master clock frequency and there is no need to generate a sampling clock.

When CCNV is brought high with the proper relationship to CLKIN (shown in the timing diagrams), the next falling clock edge defines state 0.

Lower sampling rates can be created in the *Continuous Convert* mode by running the CS5412 at full throughput and decimating the output, selectively reading only a fraction of the available samples. Variable sampling rates can be implemented in this manner using a programmable divider on the $\overline{\text{DRDY}}$ output. When operating in the *Continuous Convert* mode, attention should be paid to jitter on the master clock, since jitter will directly affect sampling purity.

If the phase of sampling must be precisely controlled, the $\overline{\text{HOLD}}$ input must be used since the hold signal is internally-generated in the *Continuous Convert* mode. A falling edge on $\overline{\text{HOLD}}$ places the internal track-and-hold amplifier in the hold state and signals a conversion cycle to begin on the next falling edge of the master clock. The $\overline{\text{HOLD}}$ input was designed for minimum aperture jitter and therefore requires CMOS-compatible logic levels (not TTL-compatible).

Due to the CS5412's refreshing the 64 reference levels in the background, $\overline{\text{HOLD}}$ commands must be synchronized to the master clock and can only occur at intervals of 8 master clock cycles. The first $\overline{\text{HOLD}}$ command after the start of a reset or

calibration cycle defines state 0 in the CS5412's timing circuitry (see Figure 4). The sampling signal applied to $\overline{HOLD}$ must adhere to frequencies of $f_{clk}/8N$ such that subsequent $\overline{HOLD}$ commands will always fall between state 7 and state 0. If the sampling clock changes phase and a $\overline{HOLD}$ command occurs before state 7 or after state 0 the CS5412 may be thrown out of calibration, and 4288 clock cycles must be allowed for the converter to complete two full background refresh cycles. Likewise, conversion data should be considered invalid for 4288 clock cycles following the first $\overline{HOLD}$ command after the end of calibration to insure specified accuracy. If a normal, periodic, $\overline{HOLD}$ signal is applied during the entire calibration period, the data will be valid immediately after calibration, i.e. when OVRNG goes low.

Most often the sampling signal applied to $\overline{HOLD}$ can be derived from the master clock. In these cases, the master clock is divided by 8, 16, 24, 32, etc. If sampling must be locked to some external clock source, a phase-locked loop can be used to generate a master clock signal for CLKIN from the sampling signal. In this instance jitter on the $\overline{HOLD}$ input will directly affect sampling purity; however, the CS5412 will tolerate significant jitter on the master clock without loss of accuracy (assuming the $\overline{HOLD}$/CLKIN phase specifications are met).

Conversion Time/Throughput

In the *Continuous Convert* mode, throughput will proceed at one-eighth the master clock frequency and the delay through the CS5412 will be ten master clock cycles. When hold commands are generated externally at the $\overline{HOLD}$ pin, the analog input is held immediately as the $\overline{HOLD}$ input falls and the conversion cycle begins on the next falling edge of the master clock. The CS5412's conversion time will range from 10 to 11 clock cycles depending on the phase relationship of the $\overline{HOLD}$ signal to the master clock (see Figure 4). Throughput can still proceed at $f_{clk}/8$ independent of the conversion time. The pipelined overlap between conversion cycles will range from to 2 to 3 clock cycles.

Reset

Upon power-up, the CS5412 must be reset to guarantee a consistent starting condition and initially calibrate the device. A falling edge on the $\overline{RST}$ pin clears internal logic and a rising edge initiates a calibration cycle which takes 6,052,445 master clock cycles to complete. The $\overline{RST}$ input must remain low for at least 2 master clock cycles to be considered valid. A simple power-up reset circuit can be constructed by tying a capacitor from $\overline{RST}$ to DGND and a resistor from $\overline{RST}$ to VD+.

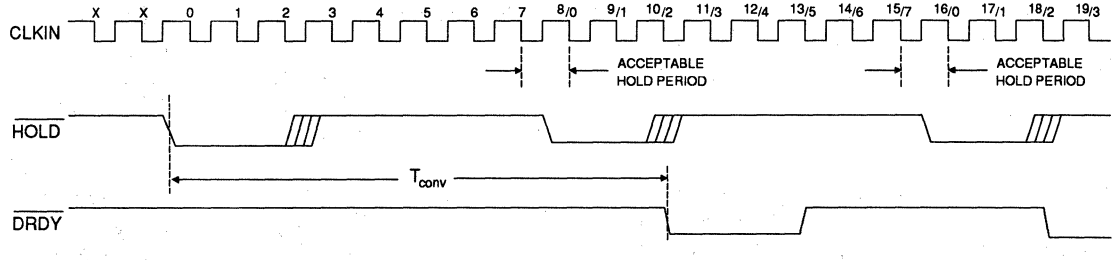


Figure 4. Hold / Conversion Timing.

Due to the CS5412's modest power dissipation and low temperature drift, no warm-up time is needed before reset to accommodate any self-heating effects. However, the voltage references (VREF+ and VREF-) should have stabilized to within their specified accuracies. The CS5412 can be reset later at any time during operation to initiate calibration. Reset overrides all other functions. If reset, the CS5412 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Overrange

The CS5412 will flag an overrange input at the OVRNG pin whenever *the sampled analog input* exceeds either the positive or negative reference voltage. If the sampled input exceeds VREF+, OVRNG will go high as DRDY falls, and all ones will be loaded into the output buffers. Similarly, if the analog input is below VREF-, OVRNG will go high as all zeroes are loaded into the output buffers. OVRNG should be latched on the rising edge of $\overline{DRDY}$. The internal reference voltages are not affected by excursions of AIN outside the external reference voltages up to the supply voltages.

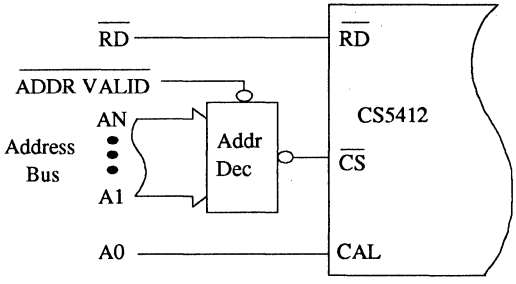


Figure 5. Microprocessor Controlled Operation.

Thirteen clock cycles after $\overline{RST}$ or CAL transitions, OVRNG goes high. The OVRNG output remains high throughout a reset/calibration sequence and will return low after its completion. It can therefore be used to generate an interrupt indicating the CS5412 has completed calibration and is ready for operation.

Microprocessor Controlled Operation

The CS5412 features 3-state output buffers and a control interface which allow the device to connect directly to a microprocessor's data and control busses. Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CS5412's 3-state output buffers with the converter's 12-bit output word. As shown in Figure 5, a decoded address is normally applied

$\overline{CS}$	$\overline{RD}$	CCNV	$\overline{HOLD}$	CAL	$\overline{RST}$	Function
0	0	X	X	0	1	Read Output Data
*	1	X	X	*	1	High Impedance Data Bus
1	X	X	X	X	1	High Impedance Data Bus
*	X	1	X	*	1	Continuous Convert Mode
*	X	0	↓	*	1	Hold and Start Convert
X	X	X	X	X	↓	Start Reset
0	X	X	X	↓	X	Start Reset

*** Not critical to the operation specified. However, $\overline{CS}$ should not be low with CAL transitioning low or a software reset will result.**

Table 1. CS5412 Truth Table.

to $\overline{CS}$, and the $\overline{RD}$ input is derived from read and strobe signals from the microprocessor's control bus. The Data Ready ($\overline{DRDY}$) output can be used to generate an interrupt or drive a DMA controller to dump the CS5412's output directly into memory after each conversion. The $\overline{DRDY}$ output falls as new data is being loaded into the output buffers. Data should be latched on the rising edge of $\overline{DRDY}$ which occurs three master clock cycles after it falls.

The CS5412 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. The CS5412 should be synchronized to the digital system via CLKIN to avoid potential errors due to enabling the 3-state output buffers while the part is converting. Using TTL loads also increases the potential for crosstalk between the digital and analog portions of the system. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the CS5412's digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

Initiating Calibration

In addition to the hardware reset, the CS5412 features a software calibration capability. Whenever CAL transitions low with $\overline{CS}$ low, or $\overline{CS}$ transitions high with CAL high, a calibration cycle will be initiated which is equivalent to the reset function. As shown in Figure 5, line A0 from the address bus can be connected to the CAL input when operating under microprocessor control. A read cycle from the CS5412's base address with A0 low will therefore retrieve output data while a read or write cycle with A0 high will initiate calibration. The CAL input is level sensitive, and like $\overline{RST}$, CAL overrides all other functions. Software-initiated calibrations can thus be used in lieu of a hardware reset at power-up.

Stand-Alone Operation

The CS5412 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low, permanently enabling the 3-state output buffers. A free-running condition is established when CAL is tied low, and $\overline{HOLD}$ is continually strobed low or CCNV is held high. The CS5412's $\overline{DRDY}$ output can be used to externally latch the output data if desired. The $\overline{DRDY}$ output will strobe low for three master clock cycles after each conversion. Data will typically be unstable for 40ns after $\overline{DRDY}$ falls, so it should be latched on the rising edge of $\overline{DRDY}$. This results in a total delay of 13 master clock cycles through the CS5412.

ANALOG CIRCUIT CONNECTIONS

Like most 2-step flash A/D converters with internal track-and-hold amplifiers, the CS5412 offers a trivial load at its analog input compared to successive-approximation and single-step flash A/D converters. The reference connections similarly present high impedance loads. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Analog Input and Reference Connections

The CS5412's analog input range is defined by the voltages applied to the VREF- and VREF+ pins. The analog input (AIN) is referenced only to these reference voltages and is completely independent of the analog ground pins. The first code transition ideally occurs 1 LSB above VREF- and the last transition occurs 1 LSB below VREF+. The CS5412 can operate with a full-scale reference as low as 2.0V p-p, but signal-to-noise performance is maximized by using the full specified range of 3V p-p. Unipolar input ranges are achieved by tying VREF- to the system's analog ground and applying the reference voltage to VREF+. Bipolar input ranges are achieved by

applying positive and negative voltages of equal magnitude to VREF+ and VREF- respectively. In this configuration, coding is in offset-binary format.

The CS5412's analog input (AIN) pin looks directly into the noninverting terminal of the track-and-hold amplifier resulting in over 10MΩ input impedance and less than 10pF input capacitance.

The reference voltages at the +VREF and -VREF inputs are dynamically sampled. This pulsed charge load requires each of the reference inputs to be decoupled with a 0.1µF ceramic capacitor in parallel with a 3.3µF tantalum capacitor. The tantalum capacitors should be chosen to maintain 3.3µF minimum capacitance over the operating temperature range. To maintain DC accuracy the reference(s) should have an output impedance of less than 5Ω at DC.

The CS3901 voltage reference provides +3V or ±1.5V for the CS5412 (see CS3901 data sheet).

Grounding and Power Supply Decoupling

The CS5412 uses the analog ground connections, AGND1 and AGND2, only as stable, low impedance sources. No dc power currents flow through these connections, and they are completely independent of AIN and DGND. Still, AGND1 and AGND2 should be tied to the system's analog ground. The CS5412's analog input is referenced only to VREF+ and VREF-. Therefore, the analog input and reference voltages should be referred to the same ground potential (not necessarily AGND) which should be used as the entire system's analog ground. The optimal grounding configuration for the CS5412 utilizes one ground plane under the CS5412. Peripheral analog and digital circuitry should be partitioned on the circuit board and separate ground planes may or may not be used.

The digital and analog supplies are isolated within the CS5412 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. The analog supplies also have multiple connections which minimize lead inductances and power separate portions of the converter's analog circuitry. The decoupling scheme shown in the *System Connection Diagram* in Figure 9 provides optimal decoupling between the CS5412's digital circuitry and the various analog sections of the chip. Ceramic capacitors are acceptable for all decoupling, and they should be placed as close to the supply pins as possible. If significant low-frequency noise is present on the supplies, 10µF tantalum capacitors are recommended in parallel with 0.1µF ceramic capacitors on the ±5V rails.

The positive digital power supply (VD+) should never exceed the positive analog supplies (VA2+ or VA5+) or the CS5412 could experience permanent damage. If the two supplies are derived from separate sources, care should be taken that the analog supply comes up first at power-up. The *System Connection Diagram* in Figure 8 shows a decoupling scheme which allows the CS5412 to be powered from a single set of ±5V rails. The positive digital supply is derived from the analog supplies though a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is used, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of the digital supplies to drop below their minimum specification of 4.75V.

As with any high-speed, high-precision A/D converter, the CS5412 requires careful attention to grounding and layout arrangements. The CDB5412 evaluation board is available for the CS5412, which eliminates the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5412 and can be quickly reconfigured to simulate any combination of sampling, calibration, and master clock conditions.

Performance

Two types of performance test results are presented here. With FFT based tests, a pure sine wave is input to the CS5412, and an FFT analysis is performed on the output data. Figure 6 shows the resulting plot with a 100 kHz input sine. Notice the absence of any harmonic distortion and the overall Signal to (Noise + Distortion) value of 70.3 dB.

Figure 7 shows the FFT plot when two sine waves are simultaneously applied to the input. Notice the lack of sum and difference products, indicating very good linearity.

A second test looks for variation in the codewidth of the CS5412, as the input moves from -Full Scale to +Full Scale. This is called the Differential Non Linearity (DNL) and is expressed as a deviation from the ideal (in LSB), with 0 being perfect. Figure 8 shows the CS5412's excellent DNL performance with most codes being within ± 0.1 LSB of perfect.

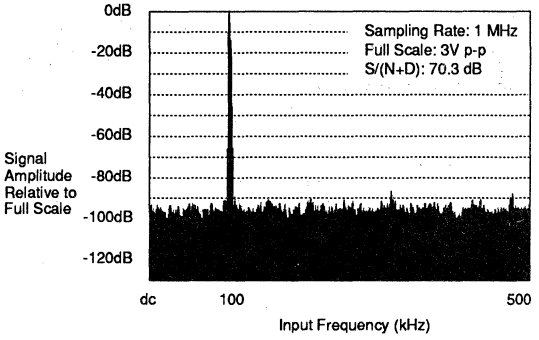


Figure 6. Typical CS5412 FFT Performance

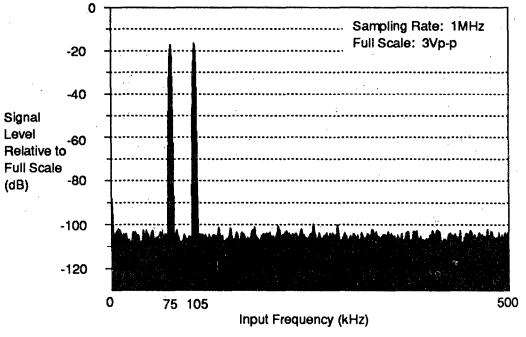


Figure 7. Intermodulation Distortion Performance

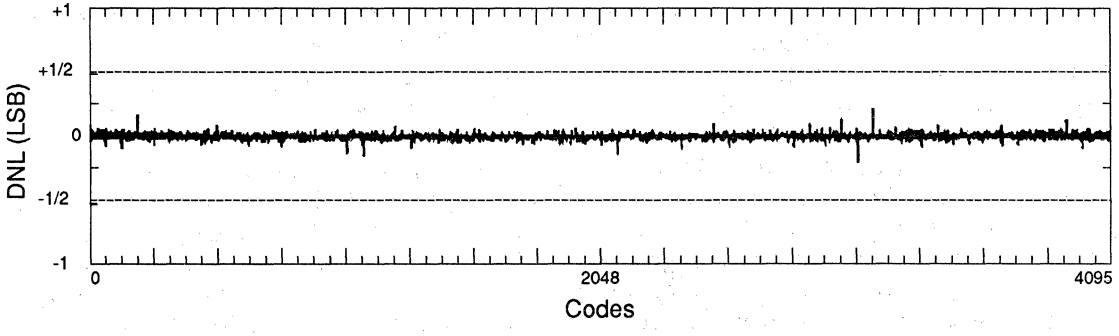
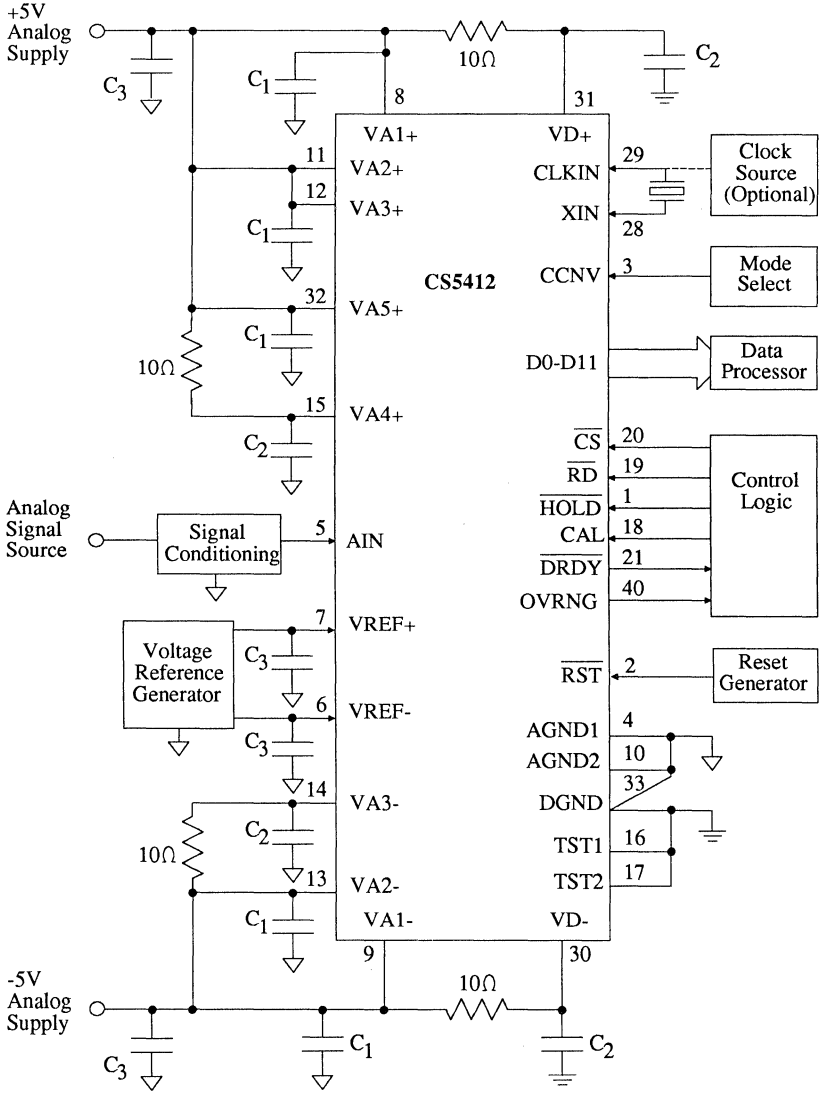


Figure 8. Typical CS5412 Differential Non-Linearity Plot

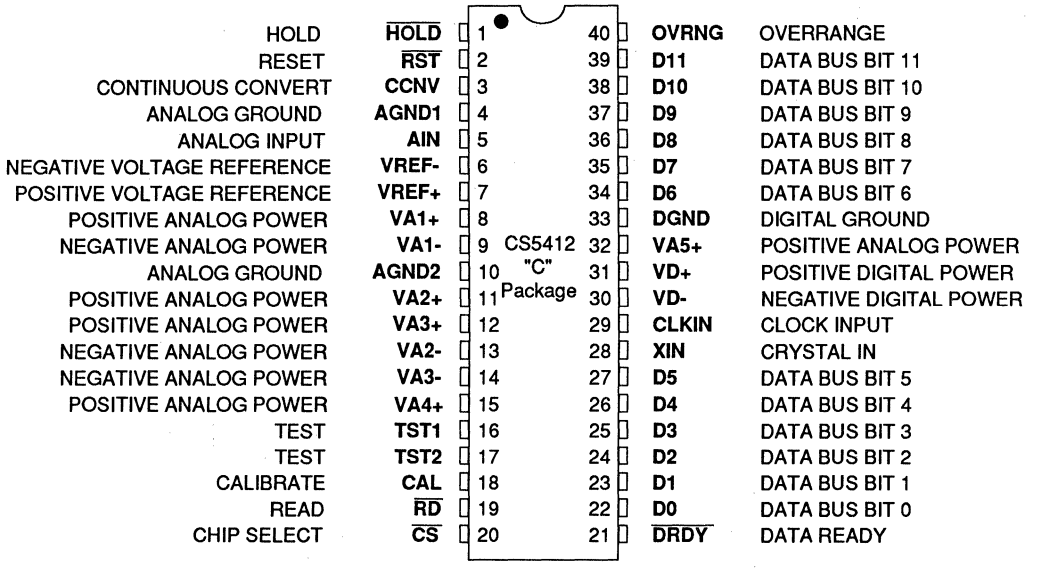


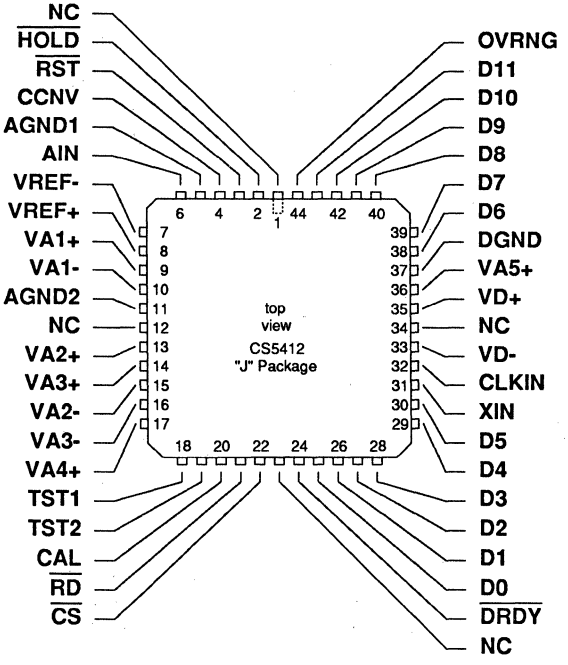
*VA2+ and VA5+ must be externally connected.

C1 - 0.01µF ceramic
C2 - 0.01µF in parallel with 0.1µF ceramic
C3 - 0.1µF ceramic in parallel with 3.3 µF tantalum

Figure 9. System Connection Diagram.

PIN DESCRIPTIONS





Power Supply Connections

VD+ - Positive Digital Power, PIN 31.
Positive digital supply voltage. Nominally +5 volts.

VD- - Negative Digital Power, PIN 30.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 33.
Digital ground reference.

VA+ - Positive Analog Power, PINS 8, 11, 12, 15, 32.
Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, PINS 9, 13, 14.
Negative analog supply voltage. Nominally -5 volts.

AGND - Analog Ground, PIN 4, 10.
Analog ground reference.

Oscillator

CLKIN; XIN - Clock In, PIN 29; Crystal In, PIN 28.
Used to generate the internal master clock. A crystal can be tied across the two pins or an external CMOS-compatible clock can be driven into CLKIN if XIN is left floating.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold Input, PIN 1.
A negative transition on $\overline{\text{HOLD}}$ puts the track-and-hold amplifier into the hold state and initiates the conversion sequence. Conversions must be synchronized with the master clock at $f_{CLK}/8N$ where N = 1,2,3. The $\overline{\text{HOLD}}$ input is CMOS-compatible.

CCNV - Continuous Convert, PIN 3.
When held high throughput will proceed at $1/8^{th}$ the master clock frequency. The $\overline{\text{HOLD}}$ pin can be high or low but must not transition.

$\overline{\text{CS}}$ - Chip Select, PIN 20.
Activates the $\overline{\text{RD}}$ and CAL inputs. When $\overline{\text{CS}}$ is high, these inputs have no effect and the data bus (D0 through D11) is held in a high impedance state.

$\overline{\text{RD}}$ - Read, PIN 19.
When held low with $\overline{\text{CS}}$ also low, enables D0-D11.

Note: Pin numbers are for the DIP package.

$\overline{\text{RST}}$ - Reset, PIN 2.

When $\overline{\text{RST}}$ transitions from low to high a full calibration is started 13 master clock cycles later indicated by OVRNG going high. OVRNG will return low when calibration is finished. Calibration takes 6,052,445 master clock cycles.

CAL - Calibrate, PIN 18.

Same as $\overline{\text{RST}}$ except it it logically inverted and enabled by $\overline{\text{CS}}$ going low .

Analog Inputs

VREF+ - Positive Voltage Reference, PIN 7.

Represents positive full scale voltage. Typically +1.5V with respect to AGND (bipolar system) or +3V with respect to AGND and VREF- (unipolar system).

VREF- - Negative Voltage Reference, PIN 6.

Represents negative full scale voltage. Typically -1.5V with respect to AGND (bipolar system) or tied to AGND (unipolar system).

AIN - Analog Input, PIN 5.

Analog input to the track-and-hold amplifier.

Digital Outputs

OVRNG - Overrange, PIN 40.

Goes high if the sampled analog input voltage exceeds VREF+ or VREF-. OVRNG also goes high during calibration cycles and can therefore be used to indicate end of calibration.

$\overline{\text{DRDY}}$ - Data Ready, PIN 21.

Falls when new data is becoming available at the outputs. Returns high three master clock cycles later. Data should be retrieved on the rising edge of $\overline{\text{DRDY}}$.

Digital Input/Outputs

D0 through D11 - Data Bus, PINS 22 thru 27, 34 thru 39.

Three-state data bus where D11 is the MSB and D0 is the LSB. The output coding is binary for unipolar and offset binary for bipolar.

Miscellaneous Pins

TST1 - Test, PIN 16.

Reserved for factory use. Must be tied to DGND for proper device operation.

TST2 - Test, PIN 17.

Reserved for factory use. Must be tied to DGND for proper device operation.

Note: Pin numbers are for the DIP package.

Ordering Guide

Model	Throughput	Signal to (Noise plus Distortion)	Linearity Error	Temp Range	Package
CS5412-JC1	1MHz	65 dB	±2.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-JJ1	1MHz	65 dB	±2.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-KC1	1MHz	68 dB	±1.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-KJ1	1MHz	68 dB	±1.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-AC1	1MHz	65 dB	±2.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-BC1	1MHz	68 dB	±1.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-SC1	1MHz	65 dB	±3.0 LSB	-55 to +125°C	40-Pin Ceramic SB DIP
CS5412-TC1	1MHz	68 dB	±2.0 LSB	-55 to +125°C	40-Pin Ceramic SB DIP
CS5412-SJ1	1MHz	65 dB	±3.0 LSB	-55 to +125°C	44-Pin J Lead CLCC
CS5412-TJ1	1MHz	68 dB	±2.0 LSB	-55 to +125°C	44-Pin J Lead CLCC

3

DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - Ratio of the rms sum of all harmonics to the rms value of of the signal. Units in percent.

Signal-to-(Noise plus Distortion) - Ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc). Expressed in decibels.

Linearity Error - The deviation of the worst code width center, out of all 4096 codes, from a straight line. The straight line is determined by using a least squares fit algorithm from the measured points. Units in LSB's.

Differential Nonlinearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full Scale Error - The deviation of the last code transition from the ideal (VREF+ - 1 LSB). Units in LSB's.

Offset Error - The deviation of the first code transition from the ideal (VREF- + 1 LSB). Units in LSB's.

Aperture Time - The time required after the hold command is issued for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuracy. Units in picoseconds.

Semiconductor Corporation

CS5501

Low-Cost, 16-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering
  6-Pole, Low-Pass Gaussian Filter
  Corner Frequencies from 0.1 to 10Hz
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  Linearity Error: ±0.0015% FS Max
  Offset and Full-Scale Errors: ±1/2 LSB
  16-Bit No Missing Codes (DNL ±1/8 LSB)
- System Calibration Capability
- Flexible Serial Communications Port
  UART- and µC-Compatible Formats
  3-State Data and Clock Outputs
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  10µW Sleep Mode for Portable Applications
- Evaluation Board Available

General Description

The CS5501 is a low-cost CMOS A/D converter which is ideal for measuring low-frequency signals representing physical, chemical, and biological processes. The CS5501 utilizes charge-balance techniques to achieve true 16-bit accuracy with up to 4kHz word rates at very low cost.

The CS5501 continuously samples at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The filter has a low-pass, 6-pole Gaussian response with no overshoot in response to step functions. Corner frequencies can be set from 0.1Hz to 10Hz, thus rejecting 50Hz and 60Hz line frequencies and any noise at spurious frequencies.

The CS5501 includes on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB. The device can also be applied in system calibration schemes to null offset and gain errors in the input channel.

The CS5501's serial port offers three modes of operation. In addition to a UART-compatible mode of asynchronous communication, there are two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

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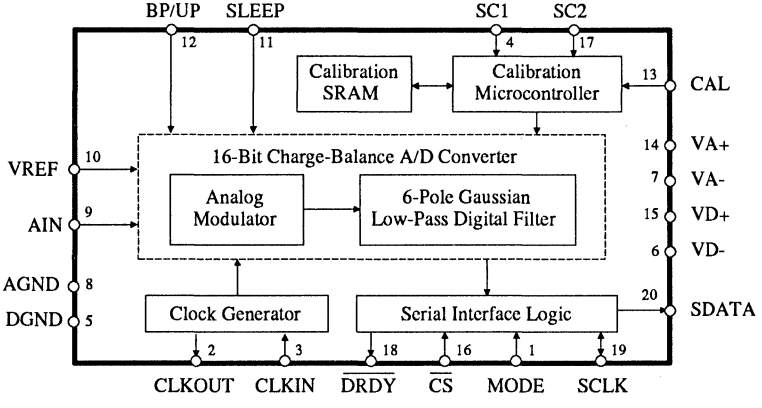

Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
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(512) 445-7222 FAX: 512 445-7581

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V; f_{CLK} = 4.096MHz; Bipolar Mode; MODE = +5V; R_{source} = 750Ω with a 1nF to AGND at AIN (see Note 1): unless otherwise specified.)

Parameter *		CS5501-J,K min	CS5501-J,K typ	CS5501-J,K max	CS5501-A,B min	CS5501-A,B typ	CS5501-A,B max	CS5501-S,T min	CS5501-S,T typ	CS5501-S,T max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125		°C
Accuracy											
Linearity Error	-J,A,S		-	0.003		-	0.003		-	0.003	±% FS
T_{min} to T_{max}	-K,B,T		0.0007	0.0015		0.0007	0.0015		0.0007	TBD	
Differential Nonlinearity T_{min} to T_{max}			± 1/8	± 1/2		± 1/8	± 1/2		± 1/8	± 1/2	LSB
Full Scale Error	(Note 2)		± 0.13	± 0.5		± 0.13	± 0.5		± 0.13	± 0.5	LSB
Full Scale Drift	(Note 3)		± 1.2	TBD		± 1.2	TBD		± 2.3	TBD	LSB
Unipolar Offset	(Note 2)		± 0.25	± 1		± 0.25	± 1		± 0.25	± 1	LSB
Unipolar Offset Drift	(Note 3)		± 1.6	TBD		± 4.2	TBD		+3.0 -25.0	TBD	LSB
Bipolar Offset	(Note 2)		± 0.25	± 1		± 0.25	± 1		± 0.25	± 1	LSB
Bipolar Offset Drift	(Note 3)		± 0.8	TBD		± 2.1	TBD		+1.5 -12.5	TBD	LSB
Bipolar Negative Full Scale Error	(Note 2)		± 0.5	± 2		± 0.5	± 2		± 0.5	± 2	LSB
Bipolar Negative Full Scale Drift	(Note 3)		± 0.6	TBD		± 0.6	TBD		± 1.2	TBD	LSB
Noise (Referred to Output)			1/10			1/10			1/10		LSB rms
Power Supplies											
DC Power Supply Currents											
I_{A+}			2	3.2		2	3.2		2	3.2	mA
I_{A-}			2	3.2		2	3.2		2	3.2	mA
I_{D+}			1	1.5		1	1.5		1	1.5	mA
I_{D-}	(Note 4)		0.03	0.1		0.03	0.1		0.03	0.1	mA
Power Dissipation											
$\overline{SLEEP}$ High			25	40		25	40		25	40	mW
$\overline{SLEEP}$ Low	(Note 4)		10	20		10	20		10	40	uW
Power Supply Rejection											
Positive Supplies			70			70			70		dB
Negative Supplies	(Note 5)		75			75			75		dB
Analog Input											
Analog Input Range											
Unipolar			0 to +2.5			0 to +2.5			0 to +2.5		V
Bipolar			± 2.5			± 2.5			± 2.5		V
Input Capacitance			20			20			20		pF
DC Bias Current	(Note 1)		1			1			1		nA

* Refer to the Specification Definitions immediately following the Pin Description Section.

ANALOG CHARACTERISTICS (Continued)

CS5501-J,K,A,B,S,T								
System Calibration Specifications		Unipolar Mode min	typ	max	Bipolar Mode min	typ	max	Units
Positive Full Scale Calibration Range		-	-	VREF+0.1	-	-	VREF+0.1	V
Positive Full Scale Input Overrange		-	-	VREF+0.1	-	-	VREF+0.1	V
Negative Full Scale Input Overrange		-	-	-(VREF+0.1)	-	-	-(VREF+0.1)	V
Maximum Offset Calibration Range	(Note 6) (Note 7)	-	-	-(VREF+0.1)	-	-	-40% VREF to +40%VREF	V
Input Span	(Note 8)	80% VREF		200%VREF + 0.2	80% VREF		200%VREF + 0.2	V

Notes:
1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5501's source impedance requirements. For more information refer the text section *Analog Input Impedance Considerations*.
2. Applies after calibration at the temperature of interest.
3. Total drift over the specified temperature range since calibration at power-up at 25°C (see Figure 11). This is guaranteed by design and /or characterization. Recalibration at any temperature will remove these errors.
4. All outputs unloaded. All inputs CMOS levels.
5. 0.1Hz to 10Hz. PSRR at 60 Hz will exceed 120 dB due to the benefit of the digital filter.
6. In unipolar mode the offset can have a negative value (-VREF) such that the unipolar mode can mimic bipolar mode operation.
7. The specifications for Input Overrange and for Input Span apply additional constraints on the offset calibration range.
8. For Unipolar mode, Input Span is the difference between full scale and zero scale. For Bipolar mode, Input Span is the difference between positive and negative full scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of ±(VREF + 0.1).

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Specifications are subject to change without notice.

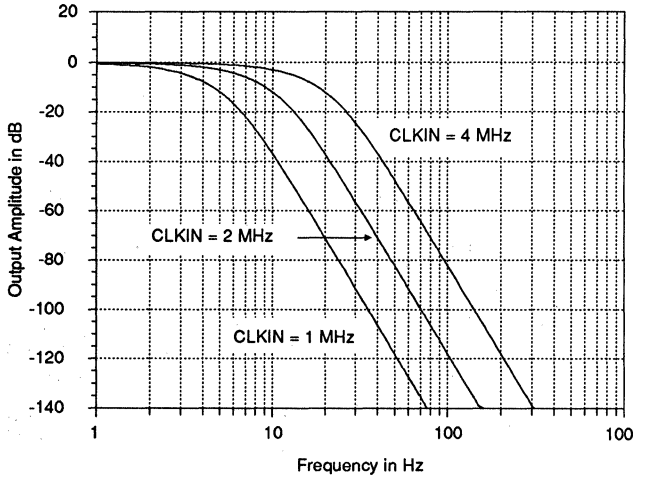
	Unipolar Mode			Bipolar Mode		
uV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

VREF=2.5V

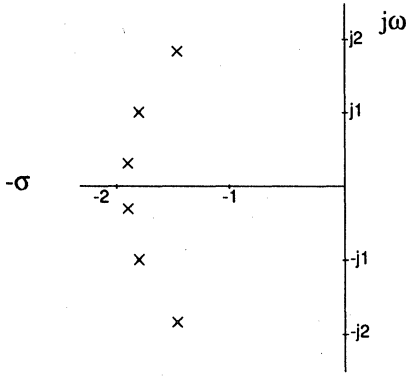
Unit Conversion Factors

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Sampling Frequency	f_s	f_{clk} / 256	Hz
Output Update Rate	f_{out}	f_{clk} /1024	Hz
Filter Corner Frequency	f_{-3dB}	f_{clk} /409,600	Hz
Settling Time to ±0.0007% FS (FS Step)	t_s	506,880/ f_{clk}	s



Frequency Response



$S_{1,2} = -1.4667 \pm j1.8199$

$S_{3,4} = -1.7559 \pm j1.0008$

$S_{5,6} = -1.8746 \pm j0.32276$

S-Domain Pole/Zero Plot (Continuous-Time Representation)

$$H(x) = [1 + 0.694x^2 + 0.241x^4 + 0.0557x^6 + 0.009664x^8 + 0.00134x^{10} + 0.000155x^{12}]^{-1/2}$$

where $x = f/f_{-3dB}$, $f_{-3dB} = f_{clk}/409{,}600$, and f is the frequency of interest.

Continuous-Time Representation of 6-Pole Gaussian Filter

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage (VD+ and VA+)	V_{MR}	2.0	-	-	V
High-Level Input Voltage All Except CLKIN	V_{IH}	2.0	-	-	V
High-Level Input Voltage CLKIN	V_{IH}	3.5	-	-	V
Low-Level Input Voltage All Except CLKIN	V_{IL}	-	-	0.8	V
Low-Level Input Voltage CLKIN	V_{IL}	-	-	1.5	V
High-Level Output Voltage (Note 9)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

3

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 10.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	1.0	2.5	3.0	V
Analog Input Voltage: (Note 11)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 10. All voltages with respect to ground.

11. The CS5501 can accept input voltages up to the analog supplies (VA+ and VA-). It will accurately convert and filter signals with noise excursions up to 100mV beyond |VREF|. After filtering, the CS5501 will output all 1's for any input above VREF and all 0's for any input below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Notes 12,13)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 12. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.

13. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency: (Note 14) Internal gate oscillator (See Table 1)	f_{clk}	200	4096	4200	kHz
Externally Supplied: Maximum -J,K		-	-	4200	
-A,B		-	-	4200	
-S,T		-	-	4200	
Minimum (Note 15) -J,K		200	40	-	
-A,B		200	40	-	
-S,T		200	40	-	
Master Clock Duty Cycle	-	20	-	80	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output (Note 16)		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output (Note 16)		-	20	-	ns
Set Up Times: $\overline{SC1}$, $\overline{SC2}$ to CAL High	t_{scs}	0	-	-	ns
$\overline{SLEEP}$ High to CLKIN High (Note 17)	t_{sls}	1	-	-	us
SSC Mode (Mode = VD+)					
Access Time: $\overline{CS}$ Low to SDATA Out	t_{csd1}	$3/f_{clk}$	-	-	ns
SDATA Delay Time SCLK Falling to New SDATA bit	t_{dd1}	-	25	100	ns
SCLK Delay Time (at 4.096 MHz) SDATA MSB bit to SCLK Rising	t_{cd1}	250	380	-	ns
Serial Clock (Out) Pulse Width High (at 4.096 MHz)	t_{ph1}	-	240	300	ns
Pulse Width Low	t_{pl1}	-	730	790	ns
Output Float Delay: SCLK Rising to Hi-Z	t_{fd2}	-	$1/f_{clk}$ +100	$1/f_{clk}$ + 200	ns
Output Float Delay: (Note 18) $\overline{CS}$ High to Output Hi-Z	t_{fd1}	-	-	$4/f_{clk}$ + 200	ns

Notes:
14. A master clock must be supplied whenever the CS5501 is not in $\overline{SLEEP}$ mode. If no clock is present when not in $\overline{SLEEP}$ mode, the CS5501 can draw higher current than specified and possibly become uncalibrated.
15. The CS5501 is designed to operate at 40kHz, but is not production tested at this frequency. Instead, the part is tested at 200kHz to reduce production test time.
16. Specified using 10% and 90% points on waveform of interest.
17. In order to synchronize several CS5501's together using the $\overline{SLEEP}$ pin, this specification must be met.
18. If $\overline{CS}$ is returned high before all 16 data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

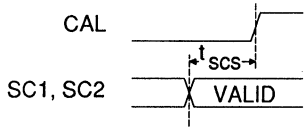
SWITCHING CHARACTERISTICS (continued) (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
SEC Mode (Mode = DGND)					
Serial Clock (In)	f_{sclk}	0		4.2	MHz
Serial Clock (In) Pulse Width High	t_{ph2}	50	-	-	ns
Pulse Width Low	t_{pl2}	180	-	-	ns
Access Time: $\overline{CS}$ Low to Data Valid (Note 19)	t_{csd2}	-	80	160	ns
Maximum Data Delay Time (Note 20) SCLK Falling to New SDATA bit	tdd2	-	75	150	ns
Output Float Delay $\overline{CS}$ High to Output Hi-Z	t_{fd3}	-	-	250	ns
Output Float Delay SCLK Falling to Output Hi-Z	t_{fd4}	-	100	200	ns
AC Mode (Mode = VD-)					
Serial Clock (In)	f_{sclk}	0	-	4.2	MHz
Serial Clock (In) Pulse Width High	t_{ph3}	50	-	-	ns
Pulse Width Low	t_{pl3}	180	-	-	ns
Set-up Time $\overline{CS}$ Low to SCLK Falling	t_{css}	-	20	40	ns
Maximum Data Delay Time SCLK Falling to New Output Bit	t_{dd3}	-	90	180	ns
Output Float Delay (Note 21) SCLK Falling to Output Hi-Z	t_{fd5}	-	100	200	ns

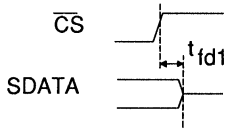
Notes: 19. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 4 clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asychronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 4 CLKIN cycles plus 160ns after $\overline{CS}$ goes low.

20. SDATA transitions on the falling edge of SCLK(i).

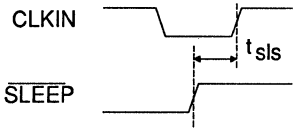
21. If $\overline{CS}$ is returned high after an 11-bit data packet is started, the SDATA output will continue to output data until the end of the second stop bit. At that time the SDATA output will go to high impedance.



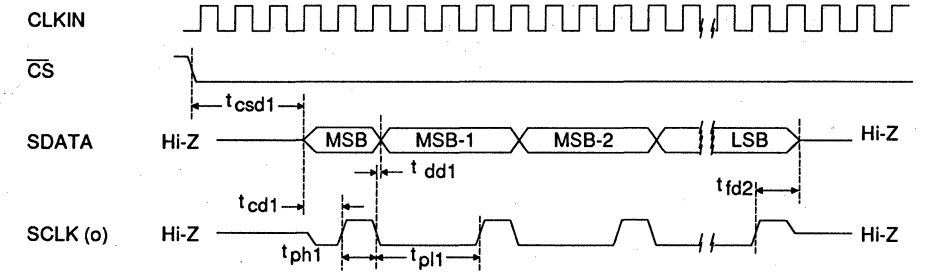
Calibration Control Timing



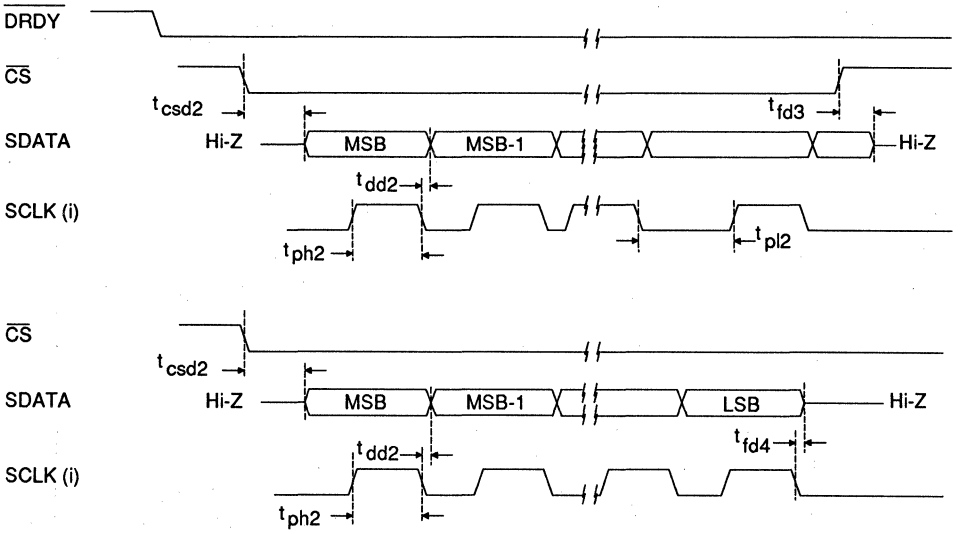
Output Data Access Timing SSC Mode (Note 18)



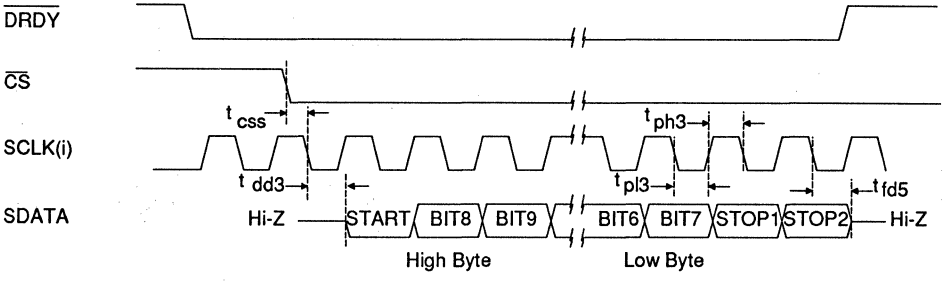
Sleep Mode Timing for Synchronization



SSC MODE Timing Relationships



SEC MODE Timing Relationships



AC MODE Timing Relationships

GENERAL DESCRIPTION

The CS5501 is a monolithic CMOS A/D converter designed specifically for high resolution measurement of low-frequency signals. The device consists of a 16-bit charge-balance converter, calibration microcontroller with on-chip SRAM, and serial communications port.

The CS5501 A/D converter performs conversions continuously and updates its output port after each conversion (unless the serial port is active). Conversions are performed and the serial port is updated independent of external control. The CS5501 is capable of measuring either unipolar or bipolar input signals. The device is also capable of calibrating itself at any time to ensure measurement accuracy.

The CS5501 performs conversions at a rate determined by the master clock signal. The master clock can be set by an external clock or with a crystal connected to the pins of the on-chip gate oscillator. The master clock frequency determines firstly, the rate at which the analog front end samples the analog input signal, secondly, the filter corner frequency of the on-chip digital filter, and thirdly, the output update rate of the serial output port.

The CS5501 design includes several self-calibration modes and several serial port interface modes to offer users maximum system design flexiblity.

The Delta-Sigma Conversion Method

The CS5501 A/D converter uses charge-balance techniques to achieve low cost, high resolution measurements. A charge-balance A/D converter consists of two basic blocks: an analog modulator and a digital filter. An elementary example of a charge-balance A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty cycle),

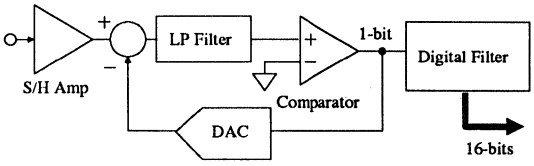
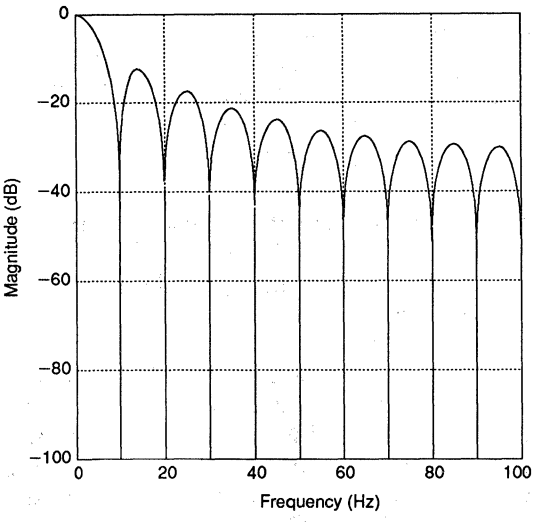


Figure 1. Charge Balance (Delta-Sigma) A/D Converter

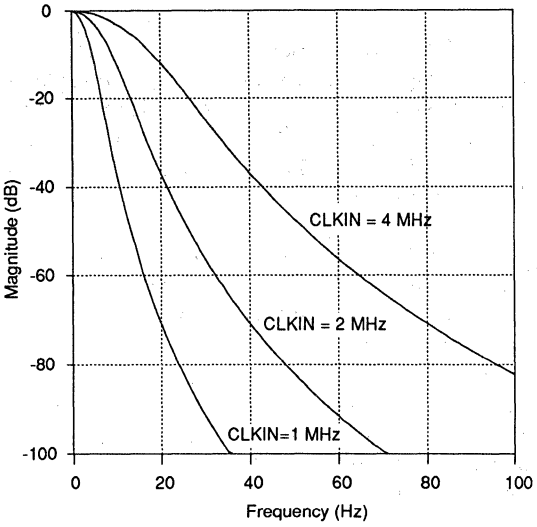
which is then filtered (averaged) by the counter for higher resolution.

The analog modulator of the CS5501 A/D converter is a multi-order delta-sigma modulator. The modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog feedback loop with high open loop gain (see Figure 1). The modulator samples and converts the input at a rate well above the bandwidth of interest. The 1-bit output of the comparator is sampled at intervals based on the clock rate of the part and this information (either a 1 or 0) is conveyed to the digital filter. The digital filter of the CS5501 is much more sophisticated than a simple counter. The filter on the chip has a 6-pole low pass Gaussian response which rolls off at 120 dB/decade (36 dB/octave). The corner frequency of the digital filter scales with the master clock frequency. In comparison, VFC's and dual slope converters offer (sin x)/x filtering for high frequency rejection (see Figure 2 for a comparison of the characteristics of these two filter types). When operating from a 1 MHz master clock the digital filter in the CS5501 offers better than 120 dB rejection of 50 and 60 Hz line frequencies and does not require any type of line synchronization to achieve this rejection. It should be noted that the CS5501 will update its output port almost a 1000 times per second when operating from the 1 MHz clock. This is a much higher update rate (typically by a factor of at least 50 times) than either VFCs or dual-slope converters can offer.

For a more detailed discussion on the delta-sigma modulator see the Application note "Delta-Sigma



a. Averaging (Integrating) Filter Response (t_{avg} = 100ms)



b. 6-Pole Gaussian Filter Response (CS5501)

Figure 2. Filter Responses

A/D Conversion Technique Overview" in the application note section of the data book. The application note discusses the delta-sigma modulator and some aspects of digital filtering.

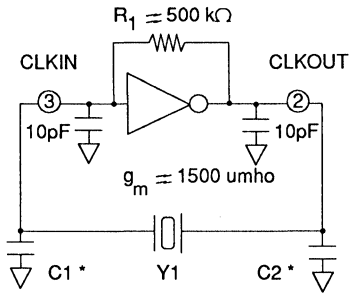
OVERVIEW OF THE CS5501

As shown in the block diagram on the front page of the data sheet, the CS5501 can be segmented into five circuit functions. The heart of the chip is the 16-bit charge balance A/D converter. The converter and all of the other circuit functions on the chip must be driven by a clock signal from the clock generator. The serial interface logic outputs the converted data. The calibration microcontroller along with the calibration SRAM (static RAM), supervises the calibration of the CS5501. Each of the segments of the CS5501 has control lines associated with it. The function of each of the pins is described in the pin description section of the data sheet.

Clock Generator

The CS5501 includes a gate which can be connected as a crystal oscillator to provide the master clock signal for the chip. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. Figure 3 illustrates a simple model of the on-chip gate oscillator. The gate has a typical transconductance of 1500 µmho. The gate model includes 10 pf capacitors at the input and output pins. These capacitances include the typical stray capacitance of the pins of the device. The on-chip gate oscillator of the CS5501 is designed to properly operate without additional loading capacitors when using a 4.096 MHz crystal. If other crystal frequencies or if ceramic resonators are used, loading capacitors may be necessary for reliable operation of the oscillator. Table 1 illustrates some typical capacitor values to be used with selected resonating elements.

CLKOUT (pin 2) can be used to drive one external CMOS gate for system clock requirements. Be sure to include the gate's input capacitance



* See Table 1

Figure 3. On-chip Gate Oscillator Model

Resonators	C1	C2
Ceramic		
200 kHz	330pF	470pF
455 kHz	100pF	100pF
1.0 MHz	50pF	50pF
2.0 MHz	20pF	20pF
Crystals		
2.000 MHz	30pF	30pF
3.579 MHz	20pF	20pF
4.096 MHz	None	None

Table 1. Resonator Loading Capacitors

and stray capacitance as part of the loading capacitance for the resonating element.

Caution: A clock signal should always be present whenever the device is not in $\overline{\text{SLEEP}}$ mode. If no clock is provided to the part when not in $\overline{\text{SLEEP}}$, the part may draw excess current and possibly even lose its calibration data. This is because the device utilizes dynamic refreshed logic internally.

Serial Interface Logic

The CS5501 serial data output can operate in any one of three different serial interface modes depending upon the MODE pin selection.

The following serial output modes are available:
SSC (Synchronous Self-Clocking) mode;
MODE pin tied to VD+ (+5V).

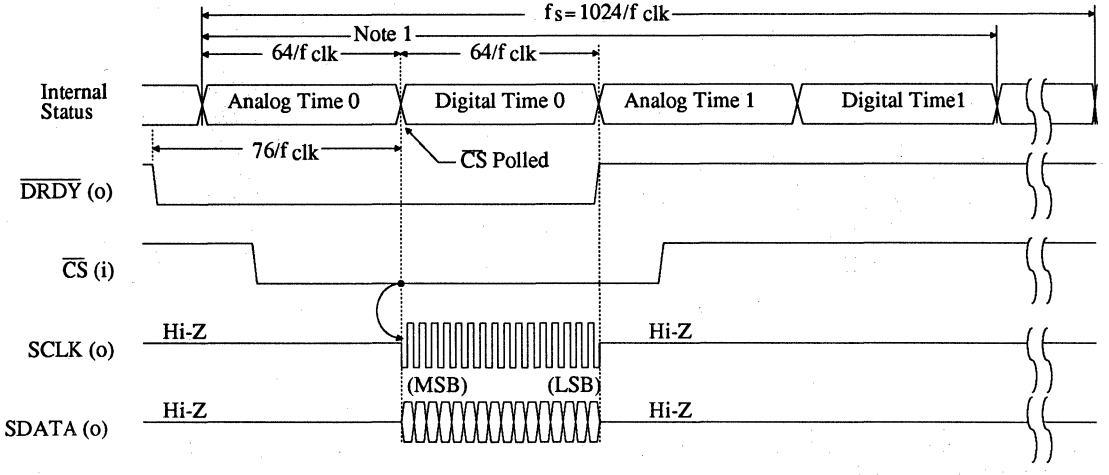
SEC (Synchronous External Clocking) mode;
MODE pin tied to DGND.

and AC (Asynchronous Communication) mode;
MODE pin tied to VD- (-5V).

The digital filter completes a filter cycle every 1024 cycles of the CLKIN frequency. At the end of each filter cycle the filter will attempt to update the output register with a new 16-bit word. If the port is empty (the last word has been output) or the $\overline{\text{CS}}$ line is inactive (high) the new 16-bit word will be loaded into the output register. When this occurs the $\overline{\text{DRDY}}$ line will go low. $\overline{\text{DRDY}}$ will return high after all data is removed from the port or after 1020 CLKIN cycles, whichever occurs first. In each of the interface modes the converter will update the output register at a rate determined by the master clock frequency (CLKIN/1024). In the event the $\overline{\text{CS}}$ line is active the port will not be updated until the $\overline{\text{CS}}$ becomes inactive or all the data bits have been serially output from the port.

Synchronous Self-Clocking Mode

When operated in the SSC mode (MODE pin tied to VD+), the CS5501 furnishes both serial output data (SDATA) and an internally-generated serial clock (SCLK). The timing for this mode is illustrated in Figures 4 and 5. In the CS5501, a filter cycle occurs every 1024 cycles of CLKIN. During each filter cycle the status of the $\overline{\text{CS}}$ is polled at eight specific times during the cycle. If $\overline{\text{CS}}$ is low when it is polled, the CS5501 begins clocking the data bits out, MSB first, at a SCLK output rate of CLKIN/4. Once transmission is complete, $\overline{\text{DRDY}}$ rises and both SDATA and SCLK outputs go into a high impedance state. A filter cycle begins each time $\overline{\text{DRDY}}$ falls. If the $\overline{\text{CS}}$ line is not active, $\overline{\text{DRDY}}$ will return high 1020 clock cycles after it falls. Four clock cycles later $\overline{\text{DRDY}}$ will fall to signal that the serial port



Note 1: There are 16 analog and digital settling periods per filter cycle (4 are shown). Data can be output in the SSC mode in only 1 of the 8 digital time periods in each filter cycle.

Figure 4. Internal Timing

has been updated with new data and that a new filter cycle has begun. The first $\overline{CS}$ polling during a filter cycle occurs 76 clock cycles after $\overline{DRDY}$ falls (the rising edge of CLKIN on which $\overline{DRDY}$ falls is considered clock cycle number one). Subsequent pollings of $\overline{CS}$ occur at intervals of 128 clock cycles thereafter (76, 204, 332, etc.). The $\overline{CS}$ signal is polled at the beginning of each of eight data output windows which occur in a filter cycle. To transmit data during any one of the eight output windows, $\overline{CS}$ must be low at least three CLKIN cycles before it is polled. If $\overline{CS}$ does not meet this set-up time, data will not be transmitted during the window time. Furthermore, $\overline{CS}$ is not latched internally and therefore must be held low during the entire data transmission to obtain all 16 bits of data.

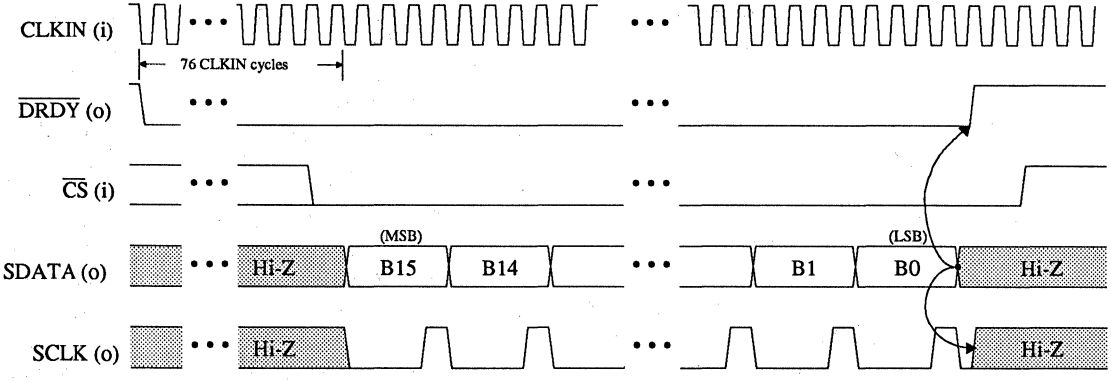


Figure 5. Synchronous Self-Clocking (SSC) Mode Timing

The eighth output window time overlaps the time in which the serial output port is to be updated. If the $\overline{CS}$ is recognized as being low when it is polled for the eighth window time, data will be output as normal, but the serial port will not be updated with new data until the next serial port update time. Under these conditions, the serial port will experience an update rate of only 2 kHz (CLKIN = 4.096 MHz) instead of the regular 4 kHz serial port update rate.

Upon completion of transmission of all 16 data bits the SCLK and SDATA outputs will go to a high impedance state even with $\overline{CS}$ held low. In the event that $\overline{CS}$ is taken high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit output and go to a high impedance state when SCLK goes low.

Synchronous External Clocking Mode

When operated in the SEC mode (MODE pin tied to DGND), the CS5501 outputs the data in its serial port at a rate determined by an external clock which is input into the SCLK pin. In this mode the output port will be updated every 1024 CLKIN cycles. $\overline{DRDY}$ will go low when new data is loaded into the output port. If $\overline{CS}$ is not active, $\overline{DRDY}$ will return positive 1020 CLKIN cycles later and remain so for four CLKIN cycles. If $\overline{CS}$ is taken low it will be recognized immediately unless it occurs while $\overline{DRDY}$ is high for the four clock cycles. As soon as $\overline{CS}$ is recognized, the SDATA output will come out of its high-impedance state and present the MSB data bit. The MSB data bit will remain present until a falling edge of SCLK occurs to advance the output to the MSB-1 bit. If the $\overline{CS}$ and external SCLK are operated asynchronously to CLKIN, errors can result in the output data unless certain precautions are taken. If $\overline{CS}$ is activated asynchronously, it may occur during the four clock cycles when $\overline{DRDY}$ is high and therefore not be recognized immediately. To be certain that data misread errors will not result if $\overline{CS}$ occurs at this time, the SCLK input should not transition high to latch the MSB until four CLKIN cycles plus 160 ns after $\overline{CS}$ is taken low. This assures that $\overline{CS}$ will be recognized and the MSB bit will become stable before the SCLK transitions positive to latch the MSB data bit.

When SCLK returns low the serial port will present the MSB-1 data bit on its output. Subsequent cycles of SCLK will advance the data output. When all data bits are clocked out, $\overline{DRDY}$ will then go high and the SDATA output will go into a high impedance state. If the $\overline{CS}$ input goes low and all of the data bits are not clocked out of the port, filter cycles will continue to occur but the output serial port will not be updated with new data. If $\overline{CS}$ is taken high at any time, the

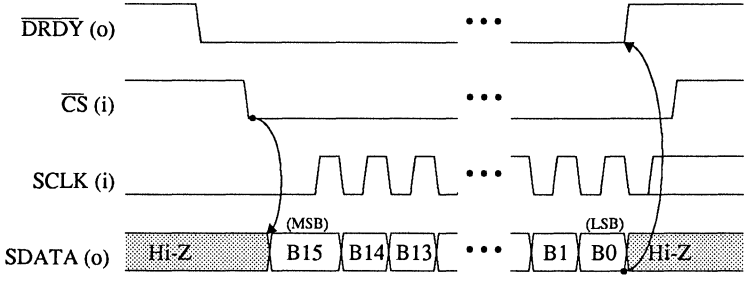


Figure 6. Synchronous External-Clocking (SEC) Mode Timing

SDATA output pin will go to a high impedance state. If any of the 16 bits in the serial port have not been clocked out, they will remain available until $\overline{DRDY}$ returns high for four clock cycles. After this $\overline{DRDY}$ will fall and the port will be updated with a new 16 bit word. Figure 6 illustrates the serial port timing in the SEC mode.

Asynchronous Communication Mode

The AC mode is activated when the MODE pin is tied to VD- (-5 V). When operating in the AC mode the CS5501 is designed to provide data output in UART compatible format. The baud rate of the SDATA output will be determined by the rate of the SCLK input. The data which is output of the SDATA pin will be formated such that it will contain two 11 bit data packets. Each packet includes one start bit, eight data bits, and two stop bits. The packet which carries the most-significant-byte data will be output first, with its lsb being the first data bit output after the start bit.

In this mode, $\overline{DRDY}$ will occur every 1024 clock cycles. If the serial port is not outputting a data byte, $\overline{DRDY}$ will return high after 1020 clock cycles and remain high for 4 clock cycles. $\overline{DRDY}$ will then go low to indicate that an update to the serial output port with a new 16 bit word has occured. To initiate a transmission from the port the $\overline{CS}$ line must be taken low. Then SCLK, which is an input in this mode, must transition from a high to a low to latch the state of $\overline{CS}$ internal to the CS5501. Once $\overline{CS}$ is recognized and latched as a low, the port will begin to output data. Figure 7 details the timing for this output. $\overline{CS}$ can be returned high before the end of the 11-bit transmission and the transmission will continue until the second stop bit of the first 11-bit packet is output. The SDATA output will go into a high impedance state after the second stop bit is output. To obtain the second 11-bit packet $\overline{CS}$ must again be brought low before $\overline{DRDY}$ goes high or the second 11-bit data packet will be overwritten with a serial port update. For the second 11-bit packet, $\overline{CS}$ need only to go low for 50 ns; it need not be latched by a falling edge of SCLK. Alternately, the $\overline{CS}$ line can be taken low and held low until both 11-bit data packets are output. This is the preferred method of control as it will prevent losing the second 11-bit data packet if the port is updated. Some serial data rates can be quite slow compared to the rate at which the CS5501 can update its output port. A slow data rate will leave only a short period of time to start the second 11-bit packet if $\overline{CS}$ is returned high momentarily. If $\overline{CS}$ is held low continuously ($\overline{CS}$ hard-wired to DGND), the serial port will be updated only after all 22 bits have been clocked out of the port.

Upon the completion of a transmission of the two 11-bit data packets the SDATA output will go into

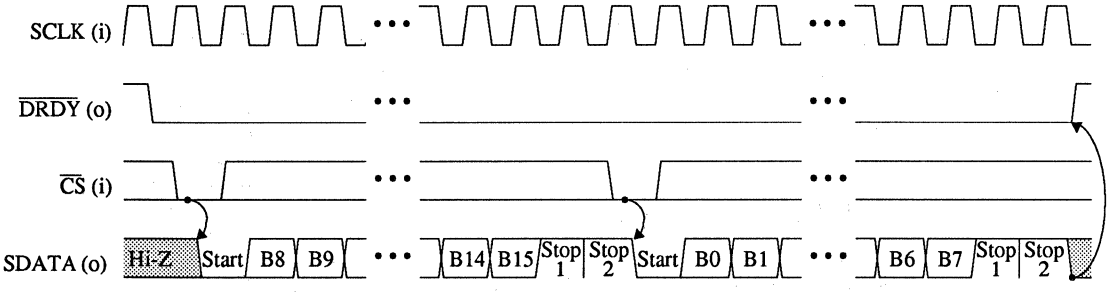


Figure 7 Asynchronous (UART) Mode Timing

a high impedance state. If at any time during transmission the $\overline{CS}$ is taken back high, the current 11-bit data packet will continue to be output. At the end of the second stop bit of the data packet, the SDATA output will go into a high impedance state.

Linearity Performance

The CS5501 delta-sigma converter is like conventional charge-balance converters in that it has no source of nonmonotonicity. The CS5501 therefore has no missing codes in its transfer function. See Figure 8 for a plot of the excellent differential linearity achieved by the CS5501. The CS5501 also has excellent integral linearity. The excellent integral linearity in the CS5501 is accomplished with a well-designed charge-balance architecture. The device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To assure that the CS5501 achieves excellent performance over time and temperature, it uses digital calibration techniques to minimize offset and gain errors to typically within ± 1/2 LSB at 16 bits.

Understanding Converter Calibration

The CS5501 offers two different digital calibration modes: self-cal; and system cal. Executing a self-calibration cycle causes the CS5501 to calibrate only itself to insure the accuracy of its own offset and gain scale factors. If system calibration is used the CS5501 calibrates taking into consideration the offset of the signal conditioning circuitry and the gain scale factor of the signal conditioning circuitry. The detailed calibration function which is executed internally by the CS5501 will depend upon the calibration mode which is selected via the SC1 and SC2 pins and upon the state of the BP/$\overline{UP}$ pin of the device. Note that any time the BP/$\overline{UP}$ pin is changed, the device needs to be recalibrated to properly function for the new measurement range.

To understand how calibration is accomplished a general explanation follows. As mentioned previously in this data sheet, the converter consists of two sections. First is the analog modulator which is a delta-sigma type charge-balance converter. This is followed by a digital filter. The filter circuitry is actually an arithematic logic unit (ALU) whose architecture and instructions execute the filter function. The modulator (the application note "Delta-Sigma Conversion Technique Overview" explains the modulator in more detail) is a charge-balance converter which uses the VREF voltage connected on pin 10 to determine the magnitude of the voltages used in its feedback DAC. The modulator accepts an analog voltage at its input and produces a data stream of 1's and 0's as its output. This data stream value can change (from 1 to 0 or vice versa) every 256 CLKIN cycles. As the input

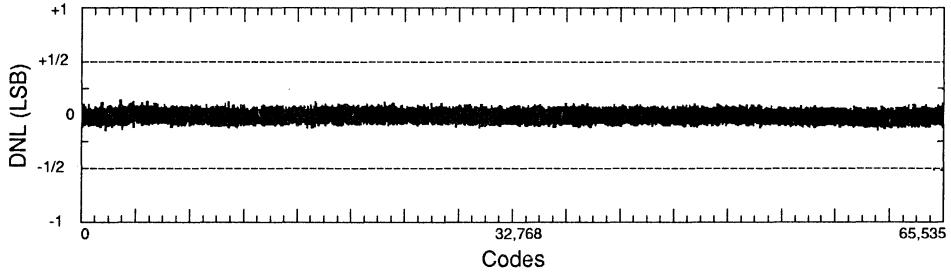


Figure 8. CS5501 Differential Nonlinearity Plot

voltage increases the ratio of the number of 1's to the number of 0's out of the modulator increases proportionally. The 1's density of the data stream out of the modulator therefore provides a digital representation of the analog input signal where the 1's density is defined as the ratio of the number of 1's to the number of 0's out of the modulator for a given period of time. The 1's density output of the modulator is also a function of the voltage on the VREF pin. If the voltage on the VREF pin increases in value (say, due to temperature drift), and the analog input voltage into the modulator remains constant, the 1's density output of the modulator will decrease (less 1's will occur). The analog input signal into the modulator which is necessary to produce a given binary output code from the converter is ratiometric to the voltage on the VREF pin. This means that if VREF increases by one per cent, the analog signal on AIN must also increase by one per cent to maintain the same binary output code from the converter.

During calibration, the calibration microcontroller examines the data stream output from the modulator. The microcontroller measures the 1's density output from the modulator of the CS5501 to establish reference points for zero scale and for full scale. The term "zero scale" will refer to the analog input value which causes the CS5501 to output 0000 (H) in unipolar mode or 8000 (H) in bipolar mode. The term "full scale" will refer to the analog input value which causes the CS5501 to output FFFF (H) in either unipolar or bipolar mode. In self-cal mode the CS5501 connects the input of the modulator to AGND, and uses this 1's density number as the zero scale point. It then measures the 1's density output of the modulator with the input of the modulator connected to the voltage on VREF. It uses this number along with the zero point to calculate a slope factor (LSB/μV) representing a gain slope for the input to output transfer function of the converter. In unipolar mode the slope factor is determined by dividing the span between the zero point and the full scale point into 65,536 segments. In bipolar mode the span between these two points is divided into 32,768 segments. The microcontroller then extends the measurement range 32,768 segments below the zero scale point to achieve bipolar measurement capability. The slope factor (LSB/μV) which has been calculated is saved and later used to calculate the binary output codes representative of the modulator 1's density during measurement conversions.

In system cal mode the microcontroller firstly measures the 1's density output of the modulator with the input signal on the AIN pin connected to system zero. It then remembers this 1's density number as the system zero scale point. A second measurement of the modulator output is taken with the input of the modulator connected to the system input voltage representative of full-scale. The microcontroller then calculates the necessary slope factor (LSB/μV) to yield 65,536 segments between the system zero scale point and the system full scale point when in unipolar mode. In bipolar mode the slope factor is determined which yields 32,768 segments between the system zero scale and full scale points. The microcontroller then extends the measurement range 32,768 segments below the system zero scale point to achieve bipolar measurement capability. The slope factor which has been calculated is saved and later used to calculate the binary codes representative of the modulator 1's density during measurement conversions.

Several Tables are listed which aid in understanding the converter calibration and output coding. Table 2 indicates the various modes in which the CS5501 can be calibrated. Figure 9 illustrates the calibration equations for unipolar and bipolar calibration. Table 3 illustrates the size of the resulting code width in each calibration mode while Table 4 illustrates the output coding for various levels of input signals.

Note that for the microcontroller to properly calculate the correct span or the slope in LSB/μV,

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence	Calibration Time
↴	0	0	Self-Cal	AGND	VREF	One Step	3,145,655/fclk
↴	1	1	System Offset & System Gain	AIN	-	1st Step	1,052,599/fclk
↴	0	1		-	AIN	2nd Step	1,068,813/fclk
↴	1	0	System Offset	AIN	VREF	One Step	2,117,389/fclk

* $\overline{\text{DRDY}}$ remains high throughout the calibration sequence. In Self-Cal mode (SC1 and SC2 low) $\overline{\text{DRDY}}$ falls once the CS5501 has settled to the analog input. In all other modes $\overline{\text{DRDY}}$ falls immediately after the calibration term has been determined.

Table 2. CS5501 Calibration Control

the microcontroller must measure a zero scale point first and then a full scale point. In the system calibration mode, there are limitations on the value that the zero scale point can differ from AGND. Restrictions also apply to the range for the input span when using system calibration. See the Analog Characteristics table for specifications.

The CS5501 has 16 bits of resolution (unipolar) or 15 bits of resolution (bipolar) between the zero and full scale points. Bipolar mode will have 16 bits resolution between positive and negative full scale points. In conclusion, during self-cal the CS5501 uses the modulator outputs for AGND and VREF and determines the offset and gain slope accordingly. In system cal mode the CS5501 microcontroller reads the modulator outputs for the system zero signal and the modulator output for the system full scale signal and determines the offset and gain slope accordingly. The microcontroller then uses the calibration offset and gain slope characteristics for subsequent measurements. The modulator output still remains ratiometric to the voltage on VREF and achieves its actual linearity over the measurement range within the modulator itself.

Initiating Calibration

A calibration cycle can be initiated by bringing the CAL pin (13) high for at least four CLKIN cycles to reset the part and then taking CAL low. The type of calibration will be determined by the state of SC1 (pin 4) and SC2 (pin 17), and the BP/$\overline{\text{UP}}$ pin. The SC1 and SC2 inputs will be latched inside the CS5501 when CAL goes high. The state of the BP/$\overline{\text{UP}}$ pin is not latched but should be fixed prior to CAL going high. The state of the BP/$\overline{\text{UP}}$ pin must be held at a steady state all during calibration. Any time the state of BP/$\overline{\text{UP}}$ is changed a new calibration must be performed to enable the CS5501 to properly function in the new mode. The time necessary to perform a calibration cycle is listed in Table 2. Whenever a calibration is initiated the $\overline{\text{DRDY}}$ line will go high and then return low when the calibration step is complete. Once a calibration cycle is initiated the cycle must finish before a new calibration cycle can be executed. In the self-cal

$$D_{OUT} = \text{Slope}\,(A_{IN} - \text{Unipolar Offset}) + 0.5\ \text{LSB}$$

a. Unipolar Calibration

$$D_{OUT} = \text{Slope}\,(A_{IN} - \text{Bipolar Offset}) + 2^{15} + 0.5\ \text{LSB}$$

b. Bipolar Calibration

Figure 9. CS5501 Calibration Equations

Cal Mode	Zero Scale	Gain Factor	1LSB	
			Unipolar	Bipolar
Self-Cal	AGND	VREF	$\frac{VREF}{65,536}$	$\frac{2VREF}{65,536}$
System Cal	SOFF	SGAIN	$\frac{SGAIN - SOFF}{65,536}$	$\frac{2(SGAIN - SOFF)}{65,536}$

Table 3. Output Code Size After Calibration

modes a calibrated output word representing the digitized analog input will be loaded into the output serial port when $\overline{DRDY}$ falls at the completion of a calibration. In the system cal modes $\overline{DRDY}$ will go high when each step of the calibration is initiated and fall when the step is complete. In the system cal modes the word loaded into the output port when $\overline{DRDY}$ falls will be representative of the last calibration point measured. For a full scale calibration point the port will be loaded with all 1's. After the final system calibration step is complete, the filter will require the necessary settling time to present an output code representative of the analog input signal to the CS5501.

Some Additional Points On Using The System Calibration Modes

Two system calibration modes are available. The first of these allows the CS5501 to calibrate out system offset errors only. In this mode the CS5501 uses the voltage on the VREF pin as the gain slope calibration point for full scale. The calibration is initiated when CAL is activated with SC1 high, SC2 low, and the BP/$\overline{UP}$ pin

Input Voltage, Unipolar Mode			Input Voltage, Bipolar Mode	
System-Cal	Self-Cal	Output Codes	Self-Cal	System-Cal
>(SGAIN - 1.5 LSB)	>(VREF - 1.5 LSB)	FFFF	>(VREF - 1.5 LSB)	>(SGAIN - 1.5 LSB)
SGAIN-1.5 LSB	VREF - 1.5 LSB	$\frac{FFFF}{FFFE}$	VREF - 1.5 LSB	SGAIN-1.5 LSB
(SGAIN-SOFF)/2 - 0.5 LSB	VREF/2 - 0.5 LSB	$\frac{8000}{7FFF}$	AGND - 0.5 LSB	SOFF - 0.5 LSB
SOFF + 0.5 LSB	AGND + 0.5 LSB	$\frac{0001}{0000}$	-VREF + 0.5 LSB	-SGAIN + 2 SOFF + 0.5 LSB
<(SOFF + 0.5 LSB)	<(AGND + 0.5 LSB)	0000	<(-VREF + 0.5 LSB)	<(-SGAIN + 2 SOFF + 0.5 LSB)

Table 4. Output Coding

either low (unipolar) or high (bipolar). In this mode the CS5501 will first measure the modulator output while the modulator is converting on the signal present on the AIN pin. The input signal must remain constant throughout the calibration step. The CS5501 will then tie the input of the modulator to the voltage on VREF pin and measure the modulator output. A gain slope calculation is then performed using these two measurement points to yield 65,536 segments (unipolar) or 32,768 segments (bipolar) between these two points.

A second system calibration mode is available which requires a two step calibration sequence. The first step is used to calibrate the system zero point. Prior to initiating this calibration step the input signal which represents the system zero value must be input into the AIN pin of the CS5501. This voltage must remain stable throughout the calibration step. To initiate calibration in this mode the SC1 and SC2 pins must be high, and the BP/$\overline{UP}$ pin either high or low. The CAL pin must then be taken high for at least four CLKIN cycles and the calibration step will begin when CAL falls. The calibration microcontroller will record the 1's density out of the modulator due to the system input voltage and use this 1's density as the zero scale point. The CS5501 will indicate that the first calibration step is complete with $\overline{DRDY}$ going low. To perform the second step of the calibration, the system input voltage which represents the full scale point is input to the AIN pin. This voltage must remain stable throughout the second step calibration time. To initiate the second step of the calibration cycle the SC1 pin must be changed from a high state to a low state and the CAL pin taken high and then low. During the second step, the microcontroller will measure the 1's density out of the modulator and use this as the full scale point. Then a slope factor will be calculated and saved for calculating output codes during subsequent measurements. Limits apply to the amount of offset and to the amount of span range which can be accommodated.

The offset voltage which can be input can extend from +20 % of the voltage on VREF to -100 % of the voltage on VREF for unipolar or from +40% of the voltage on VREF to -40% of the voltage on VREF in bipolar mode. In the unipolar mode this means that the CS5501 can be calibrated to handle negative input signals and actually mimic the bipolar mode. Caution is advised that when using offset calibration for negative input voltages for the zero reference point, that the maximum negative overrange capability of the CS5501 is not exceeded in bipolar mode. See Table 4 for the converter output codes in the system offset calibration mode. Note that the minimum allowable input span (+F.S. to -F.S.) is 80% of VREF. For a VREF voltage equal to 2.5 V, the minimum span is 2V. This 2V span can fall anywhere in the range of +VREF to -VREF. The amount of offset which can be calibrated in system cal is a function of the input span. For example, in bipolar mode with +F.S. = 2.5V = VREF, the most negative bipolar offset that can be calibrated without exceeding the negative full scale input overrange limit would be -2% of VREF.

The two step system calibration mode offers another calibration feature. After a two step calibration sequence has been properly performed, any time later additional offset calibrations can be performed by themselves to reposition the gain slope (the slope scale factor is not changed) in offset to adjust its zero reference point to the new system zero reference value.

Underrange And Overrange Considerations

The input signal range of the CS5501 will be determined by the mode in which the part is calibrated. Table 4 indicates the input signal range in the various modes of operation. If the input signal exceeds the full scale point the converter will output all ones. If the signal is less than the zero scale point (in unipolar) or more negative in magnitude than minus the full scale point (in bipolar) it will output all zeroes.

Note that the modulator-filter combination in the CS5501 is designed to accurately convert and filter input signals with noise excursions which extend up to 100 mV below the analog value which produces all zeros out or above the analog value which produces all ones out. Overrange noise excursions greater than 100 mV may increase output noise.

All pins of the CS5501 include diodes which clamp the input signals to the positive and negative supplies. If a signal on any pin (including AIN) exceeds the supply voltage (either + or -) a clamp diode will be forward-biased. Under these fault conditions the CS5501 might be damaged. Three failure modes are possible. First, excess current into the pin might short the clamp diode. Second, if the clamp diode does not fail, the bond wire from the package to the chip might fuse open. (Note that it is particularly important that input signals not be supplied into pins of the part when power is not applied). Under normal operating conditions (with the power supplies established), the device will survive transient currents through the clamp diodes up to 100 mA and continuous currents up to 10 mA. But even if the current is limited to these values, a third potential failure mode is possible. The CS5501 typically uses 3 mA of supply current. If an input signal exceeds the supply voltage of the CS5501, and can source current greater than that consumed by the circuitry connected to the 5 volt supply line, the voltage on the supply might increase in value and cause an over-voltage condition to occur. The potential for this to occur is greater if higher supply voltages exist (for example ± 15 volts) in the analog conditioning circuitry. Note that most power supply regulators are designed to source current (positive regulators) or to sink current (negative regulators) but are generally not capable of both sourcing and sinking and therefore may not be able to maintain a regulated output voltage under this type of fault condition. Therefore, the drive current into the AIN pin should be limited to a safe value if an overvoltage condition is likely to occur.

System Synchronization

If more than one CS5501 is included in a system which is operating from a common clock, all of the CS5501s can be synchronized to sample and output at exactly the same time. This can be accomplished in either of two ways. First, a single CAL signal can be issued to all the CS5501s in the system. To insure synchronization on the same clock signal the CAL signal should go low on the falling edge of CLKIN. Or second, a common $\overline{\text{SLEEP}}$ control signal can be issued. If the $\overline{\text{SLEEP}}$ signal goes positive with the appropriate set up time to CLKIN, all parts will be synchronized on the same clock cycle.

Analog Input Impedance Considerations

The analog input of the CS5501 can be modeled as illustrated in Figure 10. A 20 pF capacitor is used to dynamically sample the input signal. Every 64 CLKIN cycles the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) will be required from the input source to settle the voltage on the sample capacitor to its final value. The voltage at the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows 64 cycles of master clock (CLKIN) for the voltage on the sample capacitor to settle to its final value. The equation which defines settling time is:

$$Vo = Vin\ [1 - e^{-t/RC}]$$

Where Vo is the final settled value, Vin is the value of the input signal, R is the value of the input source resistance, C is the 20 pF sample capacitor plus the value of any stray or additional

capacitance at the input pin. The value of t is equal to 64/fclk.

From this basic equation the following equation can be developed:

$$R_{Smax} = \frac{64}{f_{clk}\,(20pF + C_{str})\;\ln(100mV/V_e)}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of V_e is the maximum error voltage which is acceptable.

For a maximum offset voltage of 10 µV (1/4LSB at 16-bits), the above equation indicates that when operating from a 4.096 MHz CLKIN, source resistances up to 75 kΩ are acceptable in the absence of stray capacitance (Cstr = 0). If higher input source resistances are desired the master clock rate can be reduced to yield a longer settling time for the 64 cycle period.

Analog Input Drift Considerations

The CS5501 analog input uses chopper-stabilization techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 11 indicates the typical offset drift due to temperature changes experienced after calibration at 25 °C. Drift is relatively flat up to about 75 °C. Above 75 °C leakage current becomes the dominant source of offset drift. Leakage currents approximately double with each 10 °C of temperature increase. Therefore the offset drift due to leakage current increases as the temperature increases. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples. In conclusion, the offset drift increases with temperature and is inversely proportional to the master clock rate. To minimize offset drift with increased temperature, higher master clock rates are desireable. At temperatures above 100 °C, a master clock rate above 1 MHz is

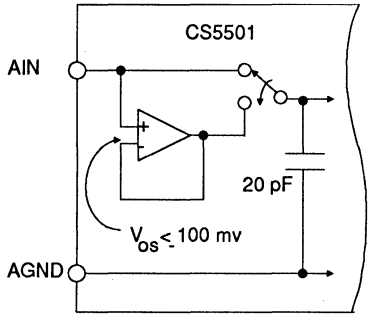


Figure 10. Analog Input Model

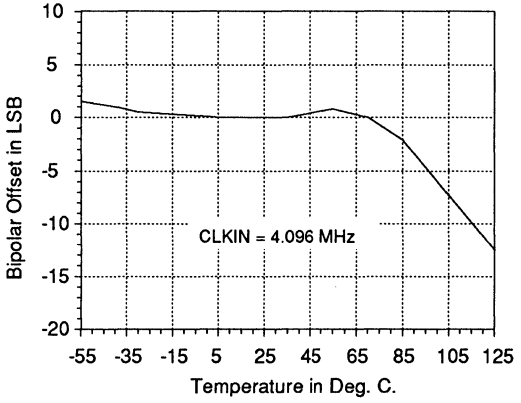


Figure 11. Typical Self-Cal Bipolar Offset vs. Temperature After Calibration at 25° C

recommended. The effects of offset drift due to temperature changes can be eliminated by recalibrating the CS5501 whenever the temperature has changed.

Gain drift within the converter depends predominately upon the temperature tracking of internal capacitors. Gain drift is not affected by leakage currents, therefore gain drift is significantly less than comparable offset errors due to temperature increases. The typical gain drift of the CS5501 is less than 2.5 LSB's over the specified temperature range.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. The CS5501 can be recalibrated at any temperature to remove the effects of these errors.

Linearity and differential non linearity are not significantly affected by temperature changes.

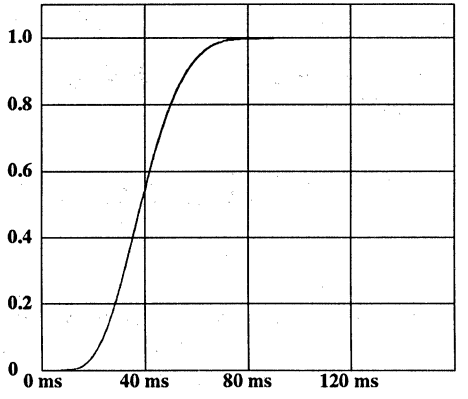


Figure 12. Output Settling (f_{clk} = 4MHz)

Filtering

At the system level, the CS5501's digital filter can be modeled exactly like an analog filter with a few minor differences. Digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially over-range the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5501's analog modulator and digital filter reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

The digital filter's corner frequency occurs at $f_{clk}/409{,}600$, where f_{clk} is the master clock frequency. With a 4.096MHz clock, the filter corner is at 10Hz and the output register is updated at a 4kHz rate. The master clock frequency can be reduced with a proportional reduction in the filter corner frequency and in the update rate to the output register. A plot of the filter response is shown in the specification tables section of this data sheet.

The CS5501's internal digital filtering creates a 6-pole Gaussian relationship. With its corner frequency set at 10Hz for minimized settling time, the CS5501 offers approximately 55dB rejection at 60Hz to signals coming into either the AIN or VREF pins. With a 5Hz cut-off, 60Hz rejection increases to more than 90dB.

Bits of Output Accuracy	Filter Cycles	CLKIN Cycles
9	340	348,160
10	356	364,544
11	389	398,336
12	435	445,440
13	459	470,016
14	475	486,400
15	486	497,664
16	495	506,880
17	500	512,000
18	504	516,096
19	506	518,144
20	507	519,168

Table 5. Settling Time Of The 6 Pole Low Pass Filter In The CS5501 To 1/2 LSB Accuracy With A Full Scale Step Input

The digital filter (rather than the analog modulator) dominates the converter's settling for step-function inputs. As shown in Figure 12, its Gaussian response demonstrates no overshoot and rapid settling. Settling time for a given level of accuracy is documented in Table 5.

Anti-Alias Considerations

The digital filter in the CS5501 does not provide rejection around integer multiples of the oversampling rate [(N*CLKIN)/256, where N = 1,2,3,...]. That is, with a 4.096 MHz master clock the noise on the analog input signal within the narrow ± 10 Hz bands around the 16 kHz, 32 kHz, 48 kHz, etc., passes unfiltered to the digital output. Most broadband noise will be very well filtered because the CS5501 uses a very high oversampling ratio of 800 (16 kHz: 2x10 Hz). Broadband noise is reduced by:

$$e_{out} = e_{in} \sqrt{2f_{-3dB}/ f_s}$$

$$e_{out} = 0.035\ e_{in}$$

where e_{in} and e_{out} are rms noise terms referred to the input. Since f_{-3dB} equals $f_{clk}/409{,}600$ and f_s equals $f_{clk}/256$, the digital filter reduces white, broadband noise by 96.5% independent of the master clock frequency. For example, the CS5501 would reduce a typical operational amplifier's 50µV rms noise to 1.75µV rms, or 0.035 LSB's rms at the 16-bit level.

Simple high frequency analog filtering in the signal conditioning circuitry can aid in removing energy at multiples of the sampling rate.

Voltage Reference Connection

The voltage reference applied to the VREF input pin defines the analog input range of the CS5501. The suggested reference is 2.5V, but the device can typically accept references from 1V to 3V with minimal performance degradation.

The circuitry inside the VREF pin is identical to that as seen at the AIN pin. The sample capacitor (see Figure 10) requires packets of charge from the external reference just as the AIN pin does. Therefore the same settling time requirements apply. Most reference IC's can handle this dynamic load requirement without inducing errors. They exhibit sufficiently low output impedance and wide enough bandwidth to settle to within 10 µV in the requisite 64 CLKIN cycles.

Noise from the reference is filtered by the digital filter in the CS5501, but the reference should be chosen to minimize noise below 10 Hz. The CS5501 typically exhibits 1/10 LSB rms noise in its measurements. This specification assumes a clean reference voltage. To insure no degradation in performance due to reference noise, the reference source should have 0.1 Hz to 10 Hz noise equivalent to 1/10 LSB rms or less. Many monolithic "band-gap" references are available which can supply 2.5 V for use with the CS5501. Many of these devices are not specified for noise, especially in the 0.1 to 10 Hz bandwidth. Some

of these devices may exhibit noise characteristics which degrade the performance of the CS5501. Figure 13 illustrates the voltage reference connections to the CS5501.

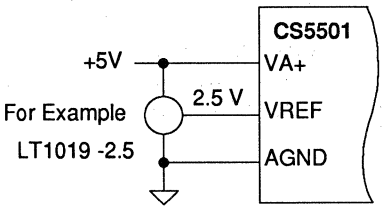


Figure 13. Voltage Reference Connections

Power Supplies And Grounding

The CS5501 uses the analog ground connection, AGND, as a measurement reference node. It carries no power supply current. The AGND pin is to be used as the reference node for both the analog input signal and for the reference voltage which is input into the VREF pin.

The analog and digital supply pins to the CS5501 chip are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF capacitors if maximum performance from the CS5501 is expected. The System Connection Diagram for the CS5501 is illustrated at the end of this section of the data sheet (See Figure 16).

As a CMOS device, the CS5501 requires that the positive analog supply voltage always be greater than or equal to the positive digital supply voltage. If the voltage on the positive digital supply should ever become greater than the voltage on the positive analog supply, diode junctions in the CMOS structure which are normally reverse-biased will become forward-biased. This may cause the part to draw high currents and experience permanent damage. The connections shown in Figure 16 eliminate this possibility.

To insure reliable operation of the CS5501, be certain that power is applied to the part before signals at AIN, VREF, or the logic input pins are present. If current is supplied into any pin before the chip is powered-up, latch-up may result. As a system, it is desirable to power the CS5501, the voltage reference, and the analog signal conditioning circuitry from the same primary source. If separate supplies are used, it is recommended that the CS5501 is powered up first. If a common power source is used for the analog signal conditioning circuitry as well as the A/D converter, this power source should be applied before application of power to the digital logic supply.

The CS5501 exhibits good power supply rejection for frequencies within the passband (dc to 10 Hz). Any small offset or gain error caused by long term drift of the power supplies can be removed by recalibration. Above 10 Hz the digital filter will provide additional rejection. When the benefits of the digital filter are added to the regular power supply rejection the effects of line frequency variations (60 Hz) on the power supplies will be reduced greater than 120 dB. If the supply voltages for the CS5501 are generated with a dc-dc converter the operating frequency of the dc-dc converter should not operate at the sampling frequency of the CS5501 or at integer multiples thereof. At these frequencies the digital filter will not aid in power supply rejection. See Anti-Alias Considerations section of this data sheet.

The recommended system connection diagram for the CS5501 is illustrated in Figure 16. Note that any digital logic inputs which are to be unused should be tied to either DGND or the VD+ as appropriate. They should not be left floating; nor should they be tied to some other logic supply voltage in the system.

Power-Up and Initialization

Upon power-up, a calibration cycle must be initiated at the CAL pin to insure a consistent starting condition and to initially calibrate the device. The CAL pin must be strobed high for a minimum of 4 clock cycles. The falling edge will initiate a calibration cycle. A simple power-on reset circuit can be built using a resistor and capacitor (see Figure 14). The resistor and capacitor values should allow for clock or oscillator startup time.

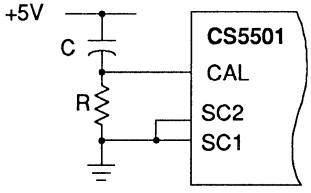


Figure 14. Power-On Reset Circuitry (Self-Calibration Only)

Due to the CS5501's low power dissipation and low temperature drift, no warm-up time is required to accommodate any self-heating effects. However, the voltage reference should have stabilized before calibration is initiated.

Sleep Mode

The CS5501 includes a sleep mode ($\overline{\text{SLEEP}}$ low) which shuts down the internal analog and digital circuitry reducing power consumption to less than 10 µW. All calibration coefficients are retained in memory such that no time is required after "awakening" for recalibration. Still, the CS5501 will require time for the digital filter to settle before an accurate reading will occur after a rising edge on $\overline{\text{SLEEP}}$ occurs.

Battery Backed-Up Calibrations

The CS5501 uses SRAM to store calibration information. The contents of the SRAM will be lost whenever power is removed from the CS5501. Figure 15 shows a battery back-up scheme that can be used to retain the calibration memory during system down time and/or protect it against intermittent power loss. Note that upon loss of power, the CS5501's $\overline{\text{SLEEP}}$ input goes low, reducing power consumption to just 10 µW. Lithium cells of 3.6 V are available which average 1750 mA-hours before they drop below the typical 2 V memory-retention spec of the CS5501. Calibration memory could therefore be maintained for approximately 20 years down time, allowing one-time factory calibrations of the transducer and all electronics.

During $\overline{\text{SLEEP}}$ both VD+ and VA+ must remain powered to no less than 2 V to retain calibration memory. The VD- and VA- voltages can be reduced to 0 V but must not be allowed to go above ground potential. Care should be taken to insure that logic inputs are maintained at either VD+ ar DGND potential during $\overline{\text{SLEEP}}$.

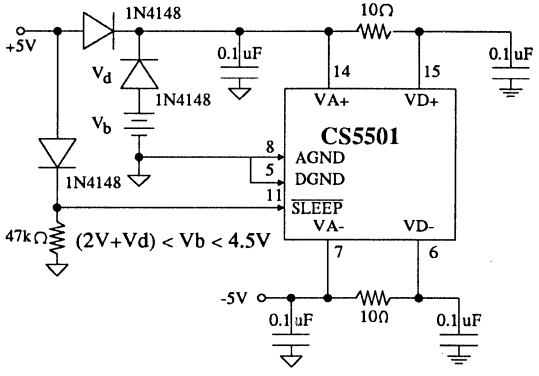


Figure 15. Example Calibration Memory Battery Back-up Circuit

Note that battery life could be shortened if the +5 V supply drops slowly during power-down. As the supply drops below the battery voltage but not yet below the logic threshold of the $\overline{\text{SLEEP}}$ pin, the battery will be supplying the CS5501 at full power (typically 3 mA). Faster transi-

tions at $\overline{\text{SLEEP}}$ can be triggered using a resistive divider or a simple resistor network to generate the $\overline{\text{SLEEP}}$ input from the +5 V supply.

Output Loading Considerations

To maximize performance of the CS5501, the output drive currents from the digital output lines should be minimized. It is recommended that CMOS logic gates (4000B, 74HC, etc.) be used to provide minimum loading. If it is necessary to drive an optoisolator the outputs of the CS5501 should be buffered. An easy means of driving the LED of an optoisolator is to use a 2N7000 or 2N7002 low cost FET.

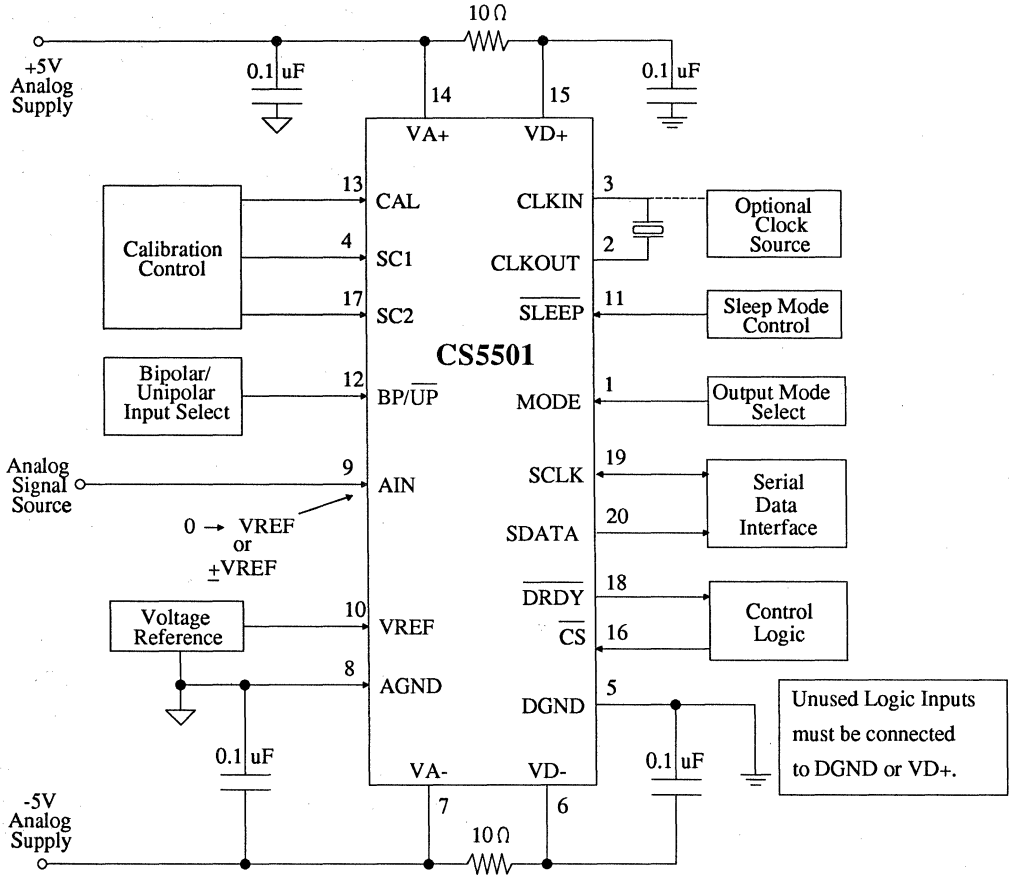


Figure 16. System Connection Diagram

PIN DESCRIPTIONS

SERIAL INTERFACE MODE SELECT	MODE	1	20	SDATA	SERIAL DATA OUTPUT
CLOCK OUT	CLKOUT	2	19	SCLK	SERIAL CLOCK INPUT/OUTPUT
CLOCK IN	CLKIN	3	18	$\overline{\text{DRDY}}$	DATA READY
SYSTEM CALIBRATION 1	SC1	4	17	SC2	SYSTEM CALIBRATION 2
DIGITAL GROUND	DGND	5	16	$\overline{\text{CS}}$	CHIP SELECT
NEGATIVE DIGITAL POWER	VD-	6	15	VD+	POSITIVE DIGITAL POWER
NEGATIVE ANALOG POWER	VA-	7	14	VA+	POSITIVE ANALOG POWER
ANALOG GROUND	AGND	8	13	CAL	CALIBRATE
ANALOG IN	AIN	9	12	$\overline{\text{BP/UP}}$	BIPOLAR/UNIPOLAR SELECT
VOLTAGE REFERENCE	VREF	10	11	$\overline{\text{SLEEP}}$	SLEEP

* Pinout applies to both DIP and SOIC packages

3

Clock Generator

CLKIN; CLKOUT -Clock In; Clock Out, Pins 3 and 2.

A gate inside the CS5501 is connected to these pins and can be used with a crystal or ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. When not in SLEEP mode, a master clock (f_{CLK}) should be present at all times.

Serial Output I/O

MODE -Serial Interface Mode Select, Pin 1.

Selects the operating mode of the serial port. If tied to VD- (-5V), the CS5501 will operate in the UART-compatible AC mode for Asynchronous Communication. The SCLK pin will operate as an *input* to set the data rate, and data will transmit *formatted* with one start and two stop bits. If MODE is tied to DGND, the CS5501 will operate in the SEC (Synchronous External-Clocking) mode, with the SCLK pin operating as an *input* and the output appearing MSB-first. If MODE is tied to VD+ (+5V), the CS5501 will operate in its SSC (Synchronous Self-Clocking) mode, with SCLK providing a serial clock *output* of $f_{clk}/4$ (25% duty-cycle).

$\overline{\text{DRDY}}$ -Data Ready, Pin 18.

$\overline{\text{DRDY}}$ goes low every 1024 cycles of CLKIN to indicate that new data has been placed in the output port. $\overline{\text{DRDY}}$ goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when $\overline{\text{SLEEP}}$ is low.

$\overline{\text{CS}}$ -Chip Select, Pin 16.

An input which can be enabled by an external device to gain control over the serial port of the CS5501.

SDATA -Serial Data Output, Pin 20.

Data from the serial port will be output from this pin at a rate determined by SCLK and in a format determined by the MODE pin. It furnishes a high impedance output state when not transmitting data.

SCLK -Serial Clock Input/Output, Pin 19.

A clock signal at this pin determines the output rate of the data from the SDATA pin. The MODE pin determines whether the SCLK signal is an input or output. SCLK may provide a high impedance output when data is not being output from the SDATA pin.

Calibration Control Inputs

SC1; SC2 -System Calibration 1 and 2, Pins 4 and 17.

Control inputs to the CS5501's calibration microcontroller for calibration. The state of SC1 and SC2 determine which of the calibration modes is selected for operation (see Table 2).

BP/$\overline{UP}$ -Bipolar/Unipolar Select, Pin 12.

Determines whether the CS5501 will be calibrated to measure bipolar (BP/$\overline{UP}$ = VD+) or unipolar (BP/$\overline{UP}$ = DGND) input signals. Recalibration is necessary whenever the state of BP/$\overline{UP}$ is changed.

CAL -Calibrate, Pin 13.

If brought high for 4 clock cycles or more, the CS5501 is reset and upon returning low a full calibration cycle will begin. The state of SC1, SC2, and BP/$\overline{UP}$ when CAL is brought high determines the type and length of calibration cycle initiated (see Table 2). Also, a single CAL signal can be used to strobe the CAL pins high on several CS5501's to synchronize their operation. Any spurious glitch on this pin may inadvertnetly place the CS5501 in Calibration mode.

Other Control Input

$\overline{SLEEP}$ -Sleep, Pin 11.

When brought low, the CS5501 will enter a low-power state. When brought high again, the CS5501 will resume operation without the need to recalibrate. After $\overline{SLEEP}$ goes high again, the CS5501's output will settle to within +0.0007% of the analog input value within $1.3/f_{-3dB}$, where f_{-3dB} is the passband frequency. The $\overline{SLEEP}$ input can also be used to synchronize sampling and the output updates of several CS5501's.

Analog Inputs

VREF -Voltage Reference, Pin 10.

Analog reference voltage input.

AIN -Analog Input, Pin 9.

Power Supply Connections

VD+ -Positive Digital Power, Pin 15.
Positive digital supply voltage. Nominally +5 volts.

VD- -Negative Digital Power, Pin 6.
Negative digital supply voltage. Nominally -5 volts.

DGND -Digital Ground, Pin 5.
Digital ground.

VA+ -Positive Analog Power, Pin 14.
Positive analog supply voltage. Nominally +5 volts.

VA- -Negative Analog Power, Pin 7.
Negative analog supply voltage. Nominally -5 volts.

AGND -Analog Ground, Pin 8.
Analog ground.

SPECIFICATION DEFINITIONS

Linearity Error - The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full-Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSBs.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSBs.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSBs.

Bipolar Negative Full-Scale Error - The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The Ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSBs.

Positive Full-Scale Input Overrange - The absolute maximum positive voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Negative Full-Scale Input Overrange - The absolute maximum negative voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Offset Calibration Range - The CS5501 calibrates its offset to the voltage applied to the AIN pin when in system calibration mode. The first code transition defines Unipolar Offset when BP/$\overline{UP}$ is low and the mid-scale transition defines Bipolar Offset when BP/$\overline{UP}$ is high. The Offset Calibration Range specification indicates the range of voltages applied to AIN that the CS5501 can accept and still calibrate offset accurately. Units in volts.

Input Span - The voltages applied to the AIN pin in system-calibration schemes define the CS5501's analog input range. The Input Span specification indicates the minimum and maximum input spans from zero-scale to full-scale in unipolar, or from positive full scale to negative full scale in bipolar, that the CS5501 can accept and still calibrate gain accurately. Units in volts.

Ordering Guide

Model Number	Linearity Error (Max)	Temperature Range	Package
CS5501-JP	0.003%	0 to 70°C	20 Pin Plastic DIP
CS5501-KP	0.0015%	0 to 70°C	20 Pin Plastic DIP
CS5501-JS†	0.003%	0 to 70°C	20 Lead SOIC
CS5501-KS†	0.0015%	0 to 70°C	20 Lead SOIC
CS5501-AD	0.003%	-40 to +85°C	20 Pin Cerdip
CS5501-BD	0.0015%	-40 to +85°C	20 Pin Cerdip
CS5501-SD	0.003%	-55 to +125°C	20 Pin Cerdip
CS5501-TD	0.0015%	-55 to +125°C	20 Pin Cerdip

† Contact the factory for availability of Engineering Samples. Expected availability of production volumes: 2nd Half 1989.

Note: The CS5501 will also be offered in die form. Contact the factory for information.

3

APPENDIX A: APPLICATIONS

Parallel Interface

Figures A1 and A2 show two serial-to-parallel conversion circuits for interfacing the CS5501 in its SSC mode to 16- and 8-bit systems respectively. Each circuit includes an optional 74HCT74 flip-flop to latch $\overline{\text{DRDY}}$ and generate a level-sensitive interrupt.

Both circuits require that the parallel read process be synchronized to the CS5501's operation. That is, the system must not try to enable the registers' parallel output while they are accepting serial data from the CS5501. The CS5501's $\overline{\text{DRDY}}$ falls just prior to serial data transmission and returns high as the last bit shifts out. Therefore, the $\overline{\text{DRDY}}$ pin can be polled for a *rising* transition directly, or it can be latched as a level-sensitive interrupt.

With the $\overline{\text{CS}}$ input tied low the CS5501 will shift out every available sample (4kHz word rate with a 4MHz master clock). Lower output rates (and interrupt rates) can be generated by dividing down the $\overline{\text{DRDY}}$ output and applying it to $\overline{\text{CS}}$.

Totally asynchronous interfaces can be created using a *Shift Data* control signal from the system which enables the CS5501's $\overline{\text{CS}}$ input and/or the shift registers' S1 inputs. The $\overline{\text{DRDY}}$ output can then be used to disable serial data transmission once an output word has been fully registered.

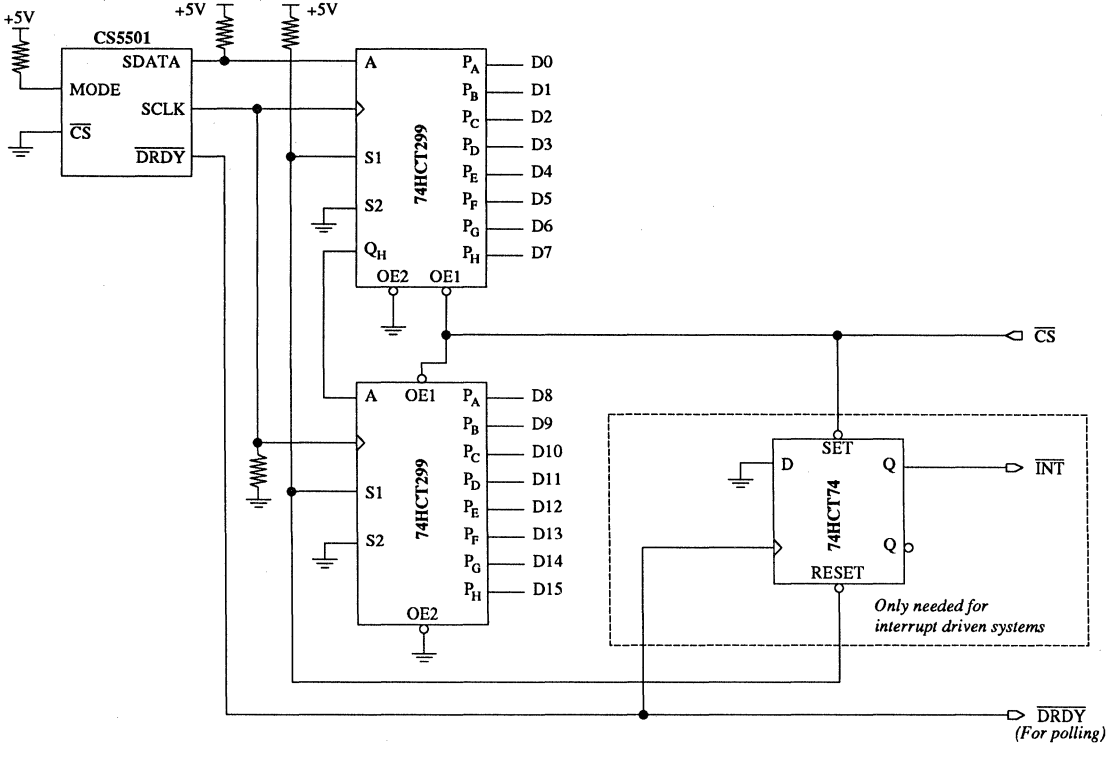


Figure A1. 16-bit Parallel Interface

In such asynchronous configurations the CS5501 is operated much like a successive-approximation converter with a *Convert* signal and a subsequent read cycle.

If it is required to latch the 16-bit data, then 2 74HC595 8-bit "shift register with latch" parts may be used instead of 74HC299's.

Serial Interfaces

Figures A3 to A8 offer both the hardware and software interfaces to several industry-standard microcontrollers using the CS5501's SEC and AC output modes. In each instance a system initialization routine is provided which configures the controller's I/O ports to accept the CS5501's serial data and clock outputs and/or generate its own serial clock. The routine also sets the CS5501 into a known state.

For each interface, a second subroutine is also provided which will collect one complete 16-bit output word from the CS5501. Figure A5 illustrates the detailed timing throughout the subroutine for one particular interface - the COPS family interface of Figure A4.

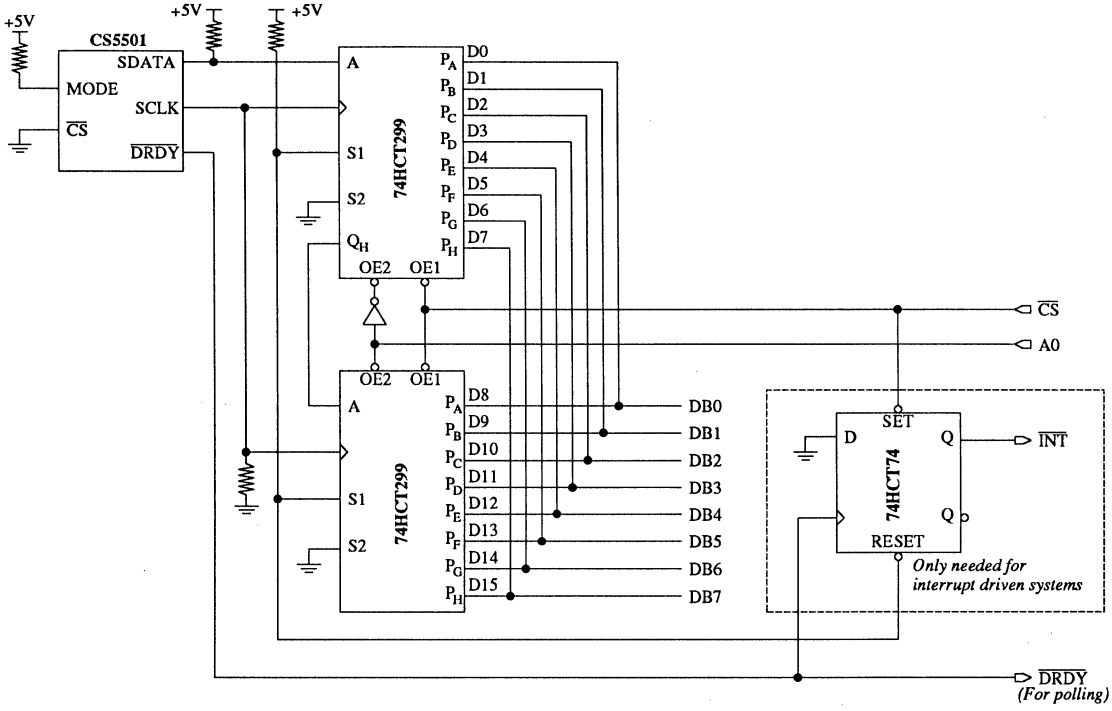


Figure A2. 8-Bit Parallel Interface

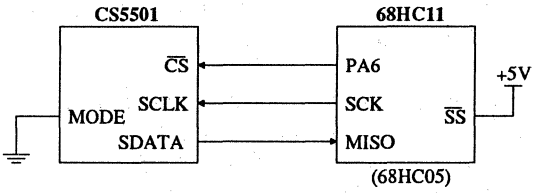


Figure A3. 68HC11/CS5501 Serial Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. Using 68HC11's SPI port. (Can use SCI and CS5501's Asynchronous mode.)
3. Maximum bit rate is 1.05 Mbps.

Assumptions:

1. PA6 used as $\overline{CS}$.
2. 68HC11 in single-chip mode.
3. Receive data via polling.
4. Normal equates for peripherial registers.
5. Data returned in register D.

Initial Code:

```
SPINIT: PSHA            ; Store temporary copy of A
        LDAA  #%x1xxxxx ; Bit 6 = 1, all others are don't cares
        STAA  PORTA     ; CS = 1, inactive; deselect CS5501
        LDAA  #$10      ;
        STAA  SPCR      ; Disable serial port
        LDAA  #%xx0110xx ; SS-input, SCK-output,
                        ;  MOSI-output, MISO-input
        STAA  DDRD      ; Data direction register for port D
        LDAA  #$50      ; Enable serial port, CMOS outputs,
        STAA  SPCR      ;  master, highest clock rate (int. clk/
        LDAA  SPSR      ;
        LDAA  SPDR      ; Bogus read to clr port and SPIF flag
        PULA            ; Restore A
        RTS             ;
```

Code to get word of data:

```
SP_IN:  LDAA  #%x0xxxxxx ;
        STAA  PORTA     ; CS = 0, active; select CS5501
        STAA  SPDR      ; Put data in serial port to start clk
WAIT1:  LDAA  SPSR      ; Get port status
        BPL   WAIT1     ; If SPIF (MSB) 0, no data yet, wait
        LDAA  SPDR      ; Put most significant byte in A
        STAA  SPDR      ; Start serial port for second byte
WAIT2:  LDAB  SPSR      ; Get port status
        BPL   WAIT2     ; If SPIF (MSB) 0, no data yet, wait
        LDAB  #%x1xxxxxx ;
        STAB  PORTA     ; CS = 1, inactive; deselect CS5501
        LDAB  SPDR      ; Put least significant byte in B
        RTS             ;
```

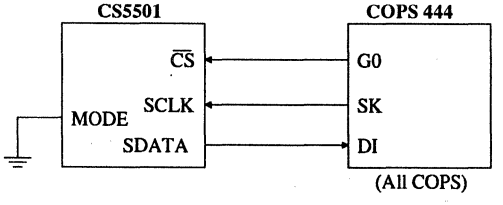


Figure A4. COPS/CS5501 Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. COPS 444 max baud = 62.5 kbps. (Others = 500 kbps)
3. See timing diagram for detailed timing.

Assumptions:

1. G0 used as $\overline{CS}$.
2. Register 0 (upper four nibbles) used to store 16-bit word.

Initial Code:

```
SPINIT: OGI   15        ; CS = 1, inactive; deselect CS5501
        RC              ; Reset carry, used in next
        XAS             ;  instruction to turn SK off
```

Code to get word of data:

```
SP_IN:  LBI   0,12      ; Point to start of data
                        ;  storage location
        SC              ; Set carry - enables SK in
                        ;  XAS instruction
        OGI   14        ; CS = 0, active; select CS5501
        LEI   0         ; Shift register mode, S0 = 0
        XAS             ; Start clocking serial port
        NOP             ;
        NOP             ; Wait for (first) M.S. nibble
GETNIB: NOP             ;
        XAS             ; Get nibble of data from SIO
        XIS             ; Put nibble in memory, inc. pointer,
        JP    GETNIB    ;  if overflow, jump around this inst.
        RC              ; Reset carry - disables SK in XAS
                        ;  instruction
        XAS             ; Bogus read - stops SK
        OGI   15        ; CS = 1, inactive; deselect CS5501
        RET             ;
```

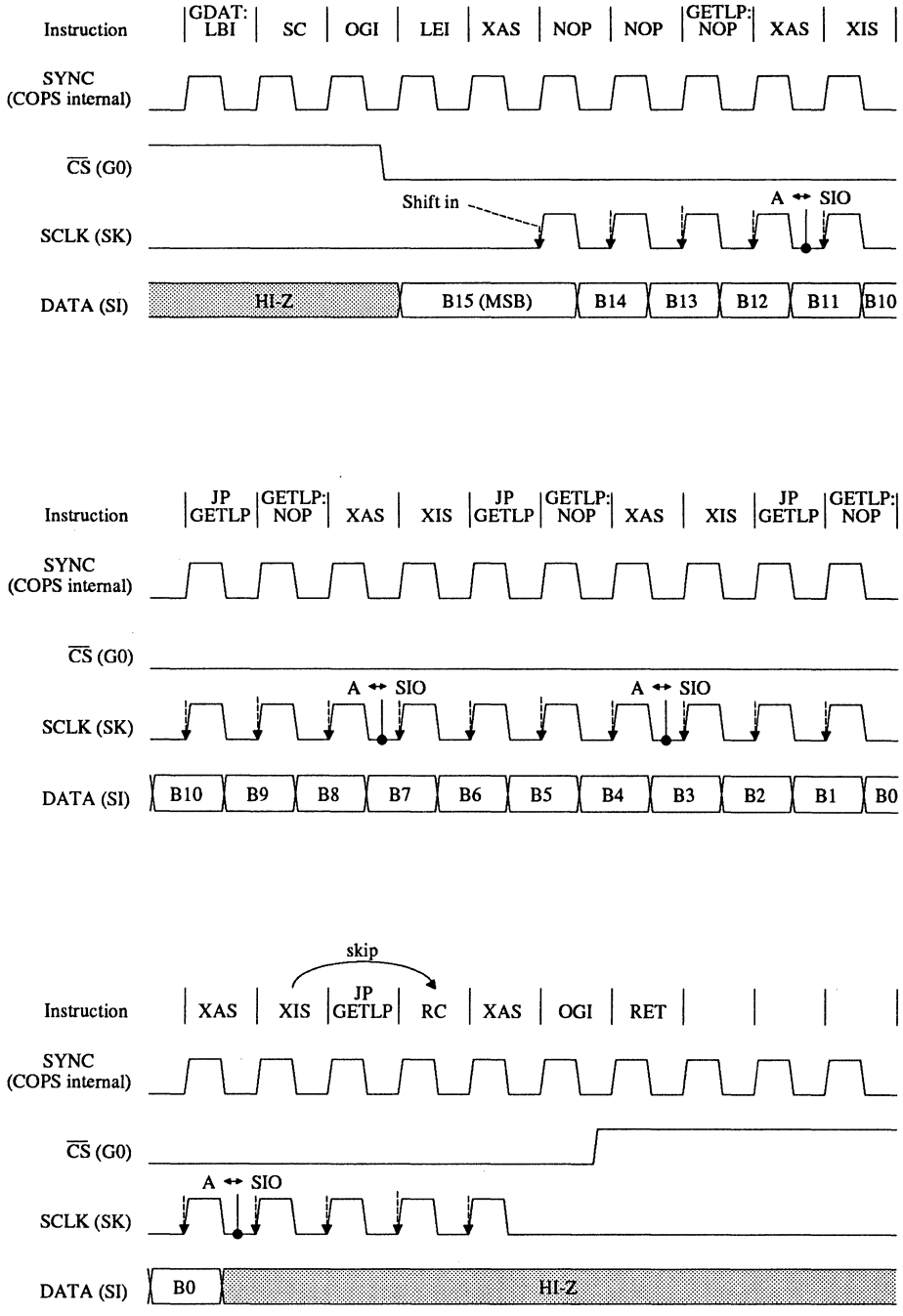


Figure A5. Serial Timing Example - COPS

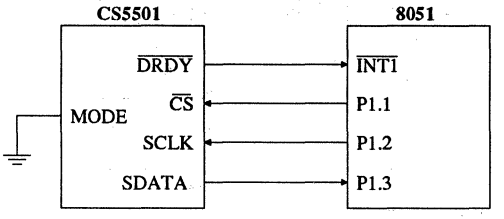


Figure A6. MCS51 (8051) /CS5501 Serial Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. Interrupt driven I/O on 8051 (For polling, connect DRDY to another port pin).

Assumptions:

1. INT1 external interrupt used.
2. Register bank 1, R6, R7 used to store data word, R7 MSbyte.
3. EA enabled elsewhere.

Initial Code:

```
CS      EQU   P1.1
SCLK    EQU   P1.2
DATA    EQU   P1.3
SPINIT: CLR   EX1       ; Disable INT1
        SETB  IT1       ; Set INT1 for falling edge triggered
        SETB  DATA      ; Set DATA to be input pin
        SETB  CS        ; CS = 1; deselect CS5501
        CLR   SCLK      ; SCLK low
        SETB  EX1       ; Enable INT1 interrupt
```

Code to get word of data:

```
        ORG 0003H
        LJMP  GETWD     ; Interrupt vector
GETWD:  PUSH  PSW       ; Save temp. copy
        PUSH  A         ; Save temp. copy
        MOV   PSW,#08   ; Set register bank 1 active
        MOV   R6,#8     ; number of bits in a byte
        CLR   CS        ; CS = 0; select CS5501
MSBYTE:SETB   SCLK      ; Toggle SCLK high
        MOV   C,DATA    ; Put bit of data into carry bit
        CLR   SCLK      ; Toggle SCLK low; next data bit
        RLC   A         ; Shift DATA bit into A register
        DJNZ  R6,MSBYTE ; Dec. R6, if not 0, get another bit
        MOV   R7,A      ; Put MSbyte into R7
        MOV   R6,#8     ; Reset R6 to number of bits in byte
LSBYTE:SETB   SCLK      ; Toggle SCLK high
        MOV   C,DATA    ; Put bit of data into carry bit
        CLR   SCLK      ; Toggle SCLK low; next data bit
        RLC   A         ; Shift DATA bit into A register
        DJNZ  R6,LSBYTE ; Dec. R6, if not 0, get another bit
        MOV   R6,A      ; Put LSbyte into R6
        SETB  CS        ; CS = 1; deselect CS5501
        POP   A         ; Restore original value
        POP   PSW       ; Restore original value
        RETI
```

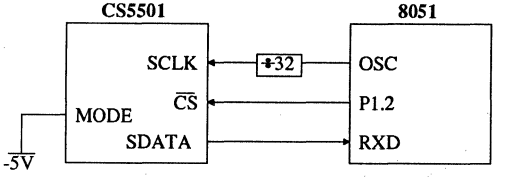


Figure A7. MCS51 (8051) /CS5501 UART Interface

Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. 8051 in mode 2, with OSC = 12 MHz, max baud = 375 kbps.

Assumptions:

1. P1.2 (port 1, bit 2) used as CS.
2. Using serial port mode 2, Baud rate = OSC/32.

(Assumptions cont.)

3. Word received put in A (ACC) and B registers, A = MSbyte.
4. No error checking done.
5. Equates used for peripheral names.

Initial Code:

```
SPINIT: SETB  SMOD      ; Set SMOD = 1, baud = OSC/32
        SETB  P1.2      ; CS = 1, inactive
        MOV   SCON,#1001000B    ; Enable serial port mode 2,
                        ;  receiver enabled, transmitter disable
        CLR   ES        ; Disable serial port interrupts (polling)
        RET             ;
```

Code to get word of data:

```
SP_IN:  CLR   P1.2      ; CS = 0, active; select CS5501
        JNB   RI,$      ; Wait for first byte
        CLR   RI        ;
        MOV   A,SBUF    ; Put most significant byte in A
        JNB   RI,$      ; wait for second byte
        CLR   RI        ;
        MOV   B,SBUF    ; Put least significant byte in B
        SETB  P1.2      ; CS = 1, inactive; deselect CS5501
        RET             ;
```

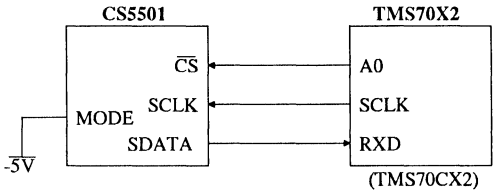


Figure A8. TMS70X2/CS5501 Serial Interface

Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. TMS70X2 in Isosynchronous mode.
3. TMS70X2 with 8 MHz master clock has max baud =1.0 Mbps.

Assumptions:

1. A0 used as $\overline{CS}$.
2. Receive data via polling.
3. Word received put in A and B upon return, A = MS byte.
4. No error checking done.
5. Normal equates for peripheral registers.

Initial Code:

```
SPINIT: DINT                    ;
        MOVP  %1,ADDR           ; A port is output
        MOVP  %1,APORT          ; A0 = 1, (CS is inactive)
        MOVP  %0,P17            ;
        MOVP  %>10,SCTLO        ; Resets port errors
        MOVP  %?x1x01101,SMODE  ; Set port for Isosync,
        MOVP  %?00x1110x,SCTLO  ;       8 bits, no parity
        MOVP  %07,T3DATA        ; Max baud rate
        MOVP  %?01000000,SCTL1  ; No multiprocessor;
                                ;       prescale = 4
        MOVP  %0,IOCNT1         ; Disable INT4 - will poll port
        PUSH  A                 ; Store original
        MOVP  RXBUF,A           ; Bogus read to clr receiver port flag
        POP   A                 ; Restore original
        EINT                    ;
        RET                     ;
```

Code to get word of data:

```
SP_IN:  MOVP  %0,APORT    ; CS active, select CS5501
WAIT1   BTJZP %2,SSTAT,WAIT1    ; Wait to receive first byte
        MOVP  RXBUF,A     ; Put most significant byte in reg. A
WAIT2   BTJZP %2,SSTAT,WAIT2    ; Wait to receive second byte
        MOVP  RXBUF,B     ; Put least significant byte in reg. B
        MOVP  %1,APORT    ; CS inactive, deselect CS5501
        RET               ;
```

3

INDEX

Semiconductor Corporation

CS5503

Low-Cost, 20-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering:
  6-Pole, Low-Pass Gaussian Filter with Corner Frequencies from 0.5 to 10Hz
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  Linearity Error: ±0.0003% FS
  Offset and Full-Scale Errors: ±4 LSB
  20-Bit No Missing Codes
- System Calibration Capability
- Flexible Serial Communications Port
  µC-Compatible Formats
  3-State Data and Clock Outputs
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  Sleep Mode for Portable Applications
- Evaluation Board Available

General Description

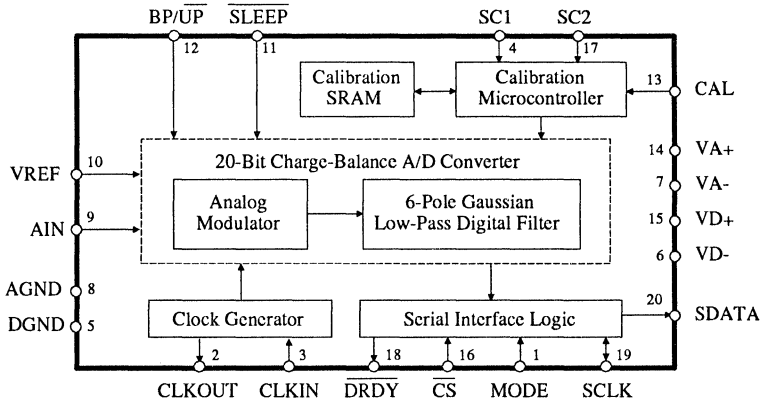
The CS5503 is a low-cost CMOS A/D converter which is ideal for measuring low-frequency signals representing physical, chemical, and biological processes. The CS5503 utilizes charge-balance techniques to achieve true 18-bit accuracy with up to 4kHz word rates at low cost, in a 20-pin DIP package.

The CS5503 continuously samples at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at a 4kHz rate. The filtering assumes a low-pass, 6-pole Gaussian response. Corner frequencies can be set from 0.5Hz to 10Hz, thus rejecting 50Hz and 60Hz frequencies and any noise at spurious frequencies.

The CS5503 includes on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of less than 4 LSB. The device can also be applied in system calibration schemes to null offset and gain errors in the input channel.

The CS5503's serial port offers two modes of operation, for direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers. The CS5503 is pin compatible with the 16-bit CS5501.

TABLE OF CONTENTS: Page 3-346 **ORDERING INFORMATION:** Page 3-345



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V; CLKIN = 4.096MHz; Bipolar Mode; MODE = +5V; R_{source} = 750Ω with a 1nF to AGND at AIN (see Note 1): unless otherwise specified.)

Parameter *		CS5503-J,K,L min	CS5503-J,K,L typ	CS5503-J,K,L max	CS5503-A,B,C min	CS5503-A,B,C typ	CS5503-A,B,C max	CS5503-S,T,U min	CS5503-S,T,U typ	CS5503-S,T,U max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125		°C
Accuracy											
Linearity Error	-J,A,S		0.0015	0.003		0.0015	0.003		0.0015	0.003	
T_{min} to T_{max}	-K,B,T		0.0007	0.0015		0.0007	0.0015		0.0007	TBD	±% FS
	-L,C,U		0.0003	TBD		0.0003	TBD		0.0003	TBD	
Differential Nonlinearity (No Missing Codes)	T_{min} to T_{max}		20			20			20		BITS
Full Scale Error	(Note 2)		± 4	± 16		± 4	± 16		± 4	± 16	LSB
Full Scale Drift	(Note 3)		± 19	TBD		± 19	TBD		± 37	TBD	LSB
Unipolar Offset	(Note 2)		± 4	± 16		± 4	± 16		± 4	± 16	LSB
Unipolar Offset Drift	(Note 3)		± 26	TBD		± 67	TBD		+48 -400	TBD	LSB
Bipolar Offset	(Note 2)		± 4	± 16		± 4	± 16		± 4	± 16	LSB
Bipolar Offset Drift	(Note 3)		± 13	TBD		± 34	TBD		+24 -200	TBD	LSB
Bipolar Negative Full Scale Error	(Note 2)		± 8	± 32		± 8	± 32		± 8	± 32	LSB
Bipolar Negative Full Scale Drift	(Note 3)		± 10	TBD		± 10	TBD		± 20	TBD	LSB
Noise (Referred to Output)			1.6			1.6			1.6		LSB rms
Power Supplies											
DC Power Supply Currents											
I_{A+}			2	3.2		2	3.2		2	3.2	mA
I_{A-}			2	3.2		2	3.2		2	3.2	mA
I_{D+}			1	1.5		1	1.5		1	1.5	mA
I_{D-}	(Note 4)		0.03	0.1		0.03	0.1		0.03	0.1	mA
Power Dissipation											
$\overline{SLEEP}$ High			25	40		25	40		25	40	mW
$\overline{SLEEP}$ Low	(Note 4)		10	20		10	20		10	40	uW
Power Supply Rejection											
Positive Supplies			70			70			70		dB
Negative Supplies	(Note 5)		75			75			75		dB
Analog Input											
Analog Input Range											
Unipolar			0 to +2.5			0 to +2.5			0 to +2.5		V
Bipolar			± 2.5			± 2.5			± 2.5		V
Input Capacitance			20			20			20		pF
DC Bias Current	(Note 1)		1			1			1		nA

* Refer to the Specification Definitions immediately following the Pin Description Section.

ANALOG CHARACTERISTICS (Continued)

CS5503-J,K,L,A,B,C,S,T,U								
System Calibration Specifications		Unipolar Mode min	typ	max	Bipolar Mode min	typ	max	Units
Positive Full Scale Calibration Range				VREF+0.1			VREF+0.1	V
Positive Full Scale Input Overrange				VREF+0.1			VREF+0.1	V
Negative Full Scale Input Overrange				-(VREF+0.1)			-(VREF+0.1)	V
Maximum Offset Calibration Range	(Note 6) (Note 7)			-(VREF+0.1)			-40% VREF to +40%VREF	V
Input Span	(Note 8)	80% VREF		200%VREF + 0.2	80% VREF		200%VREF + 0.2	V

Notes:
1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the CLKIN frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5503's source impedance requirements. For more information refer the text section *Analog Input Impedance Considerations*.
2. Applies after calibration at the temperature of interest.
3. Total drift over the specified temperature range since calibration at power-up at 25°C. This is guaranteed by design and /or characterization. Recalibration at any temperature will remove these errors.
4. All outputs unloaded. All inputs CMOS levels.
5. 0.1Hz to 10Hz. PSRR at 60 Hz will exceed 120 dB due to the benefit of the digital filter.
6. In unipolar mode the offset can have a negative value (-VREF) such that the unipolar mode can mimic bipolar mode operation.
7. The specifications for Input Overrange and for Input Span apply additional constraints on the offset calibration range.
8. For Unipolar mode, Input Span is the difference between full scale and zero scale. For Bipolar mode, Input Span is the difference between positive and negative full scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of ±(VREF + 0.1).

3

Specifications are subject to change without notice.

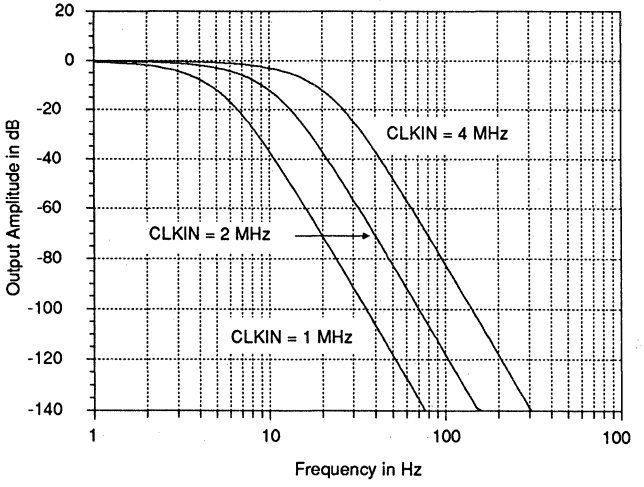
	Unipolar Mode			Bipolar Mode		
uV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.50	0.0000477	0.47	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.50	0.0000477	0.47
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.00	0.0003814	3.81	2.00	0.0001907	1.91

VREF=2.5V

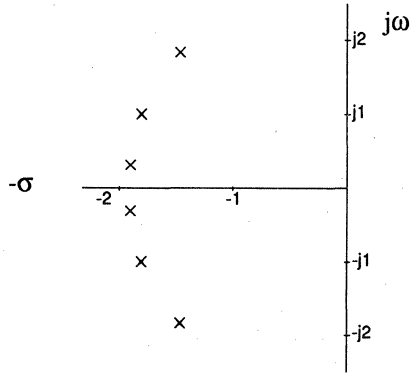
Unit Conversion Factors

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Sampling Frequency	f_s	CLKIN/256	Hz
Output Update Rate	f_{out}	CLKIN/1024	Hz
Filter Corner Frequency	f_{-3dB}	CLKIN/409,600	Hz
Settling Time to ±0.0007% FS (FS Step)	t_s	506,880/CLKIN	S



Frequency Response



$S_{1,2} = -1.4667 \pm j1.8199$

$S_{3,4} = -1.7559 \pm j1.0008$

$S_{5,6} = -1.8746 \pm j0.32276$

S-Domain Pole/Zero Plot (Continuous-Time Representation)

$$H(x) = [1 + 0.694x^2 + 0.241x^4 + 0.0557x^6 + 0.009664x^8 + 0.00134x^{10} + 0.000155x^{12}]^{-1/2}$$

where $x = f/f_{-3dB}$, f_{-3dB} = CLKIN /409,600, and f is the frequency of interest.

Continuous-Time Representation of 6-Pole Gaussian Filter

DIGITAL CHARACTERISTICS (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage (VD+ and VA+)	V_{MR}	2.0	-	-	V
High-Level Input Voltage All Except CLKIN	V_{IH}	2.0	-	-	V
High-Level Input Voltage CLKIN	V_{IH}	3.5	-	-	V
Low-Level Input Voltage All Except CLKIN	V_{IL}	-	-	0.8	V
Low-Level Input Voltage CLKIN	V_{IL}	-	-	1.5	V
High-Level Output Voltage (Note 9)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 10.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	1.0	2.5	3.0	V
Analog Input Voltage: (Note 11)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 10. All voltages with respect to ground.

11. The CS5503 can accept input voltages up to the analog supplies (VA+ and VA-). It will accurately convert and filter signals with noise excursions up to 100mV beyond |VREF|. After filtering, the CS5503 will output all 1's for any input above VREF and all 0's for any input below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Notes 12,13)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 12. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.

13. Transient currents of up to 100mA will not cause SCR latch-up.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Frequency: (Note 14)	Internal gate oscillator (See Table 1)	CLKIN	200	4096	4200	kHz
	Externally Supplied: Maximum -J,K,L		-	-	4200	
	-A,B,C		-	-	4200	
	-S,T,U		-	-	4200	
	Minimum (Note 15) -J,K,L		200	-	-	
	-A,B,C		200	-	-	
	-S,T,U		TBD	TBD	-	
CLKIN Duty Cycle		-	20	-	80	%
Rise Times:	Any Digital Input	t_{rise}	-	-	1.0	us
	Any Digital Output (Note 16)		-	20	-	ns
Fall Times:	Any Digital Input	t_{fall}	-	-	1.0	us
	Any Digital Output (Note 16)		-	20	-	ns
Set Up Times:	$\overline{SC1}$, $\overline{SC2}$ to CAL High	t_{scs}	0	-	-	ns
	$\overline{SLEEP}$ High to CLKIN High (Note 17)	t_{sls}	1	-	-	us
SSC Mode (Mode = VD+)						
Access Time:	$\overline{CS}$ Low to SDATA Out	t_{csd1}	3/CLKIN	-	-	ns
SDATA Delay Time	SCLK Falling to New SDATA bit	t_{dd1}	-	25	100	ns
SCLK Delay Time	(at 4.096 MHz) SDATA MSB bit to SCLK Rising	t_{cd1}	250	380	-	ns
Serial Clock (Out)	Pulse Width High (at 4.096 MHz)	t_{ph1}	-	240	300	ns
	Pulse Width Low	t_{pl1}	-	730	790	ns
Output Float Delay:	SCLK Rising to Hi-Z	t_{fd2}	-	1/CLKIN+100	1/CLKIN + 200	ns
Output Float Delay: (Note 18)	$\overline{CS}$ High to Output Hi-Z	t_{fd1}	-	-	4/CLKIN + 200	ns

Notes: 14. CLKIN must be supplied whenever the CS5503 is not in $\overline{SLEEP}$ mode. If no clock is present when not in $\overline{SLEEP}$ mode, the CS5503 can draw higher current than specified and possibly become uncalibrated.

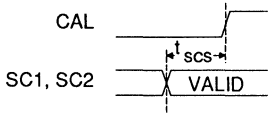
15. The CS5503 is production tested at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz
16. Specified using 10% and 90% points on waveform of interest.
17. In order to synchronize several CS5503's together using the $\overline{SLEEP}$ pin, this specification must be met.
18. If $\overline{CS}$ is returned high before all 20 data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

SWITCHING CHARACTERISTICS (continued) ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

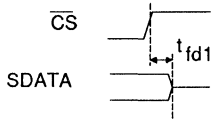
Parameter	Symbol	Min	Typ	Max	Units
SEC Mode (Mode = DGND)					
Serial Clock (In)	f_{sclk}	dc		4.2	MHz
Serial Clock (In) Pulse Width High	t_{ph2}	50	-	-	ns
Pulse Width Low	t_{pl2}	180	-	-	ns
Access Time: $\overline{CS}$ Low to Data Valid (Note 19)	t_{csd2}	-	80	160	ns
Maximum Data Delay Time (Note 20) SCLK Falling to New SDATA bit	tdd2	-	75	150	ns
Output Float Delay $\overline{CS}$ High to Output Hi-Z	t_{fd3}	-	-	250	ns
Output Float Delay SCLK Falling to Output Hi-Z	t_{fd4}	-	100	200	ns

Notes: 19. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 4 clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asychronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 4 CLKIN cycles plus 160ns after $\overline{CS}$ goes low.

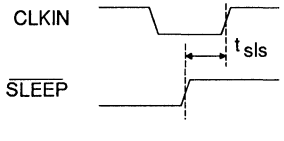
20. SDATA transitions on the falling edge of SCLK(i).



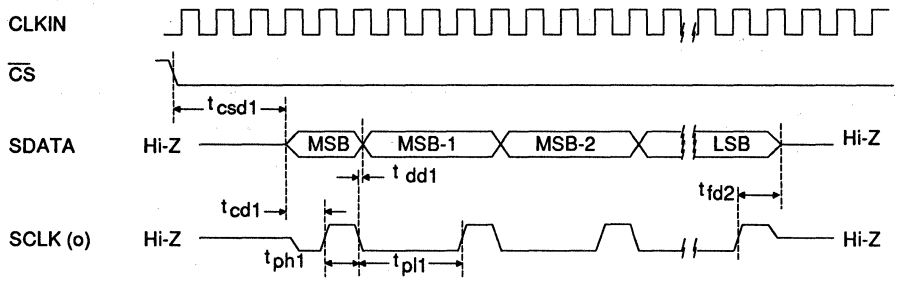
Calibration Control Timing



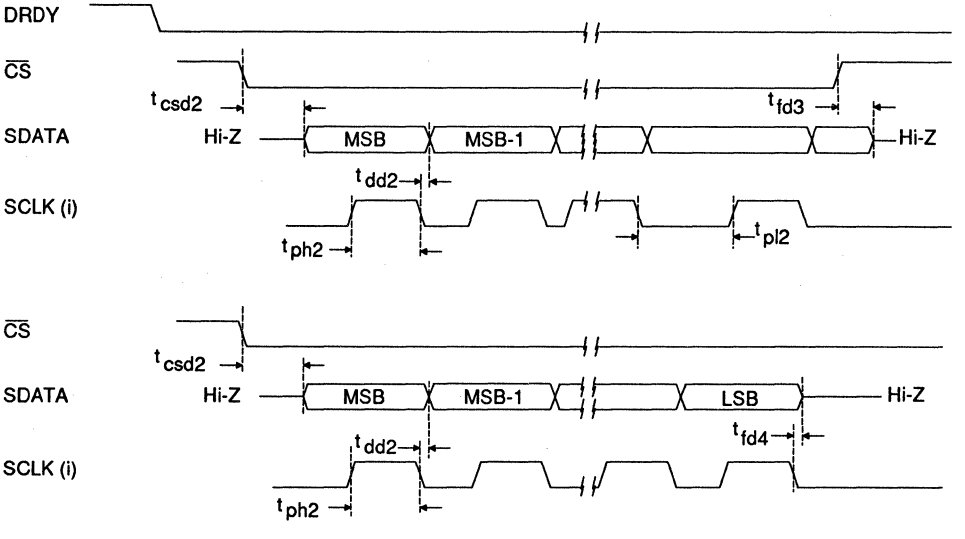
Output Data Access Timing SSC Mode (Note 18)



Sleep Mode Timing for Synchronization



SSC MODE Timing Relationships



SEC MODE Timing Relationships

GENERAL DESCRIPTION

The CS5503 is a monolithic CMOS A/D converter designed specifically for high resolution measurement of low-frequency signals. The device consists of a 20-bit charge-balance converter, calibration microcontroller with on-chip SRAM, and serial communications port.

The CS5503 A/D converter performs conversions continuously and updates its output port after each conversion (unless the serial port is active). Conversions are performed and the serial port is updated independent of external control. The CS5503 is capable of measuring either unipolar or bipolar input signals. The device is also capable of calibrating itself at any time to ensure measurement accuracy.

The CS5503 performs conversions at a rate determined by the CLKIN signal. CLKIN can be set by an external clock or with a crystal connected to the pins of the on-chip gate oscillator. CLKIN determines firstly, the rate at which the analog front end samples the analog input signal, secondly, the filter corner frequency of the on-chip digital filter, and thirdly, the output update rate of the serial output port.

The CS5503 design includes several self-calibration modes and two serial port interface modes to offer users maximum system design flexiblity.

The Delta-Sigma Conversion Method

The CS5503 A/D converter uses charge-balance techniques to achieve low-cost, high-resolution measurements. A charge-balance A/D converter consists of two basic blocks: an analog modulator and a digital filter. An elementary example of a charge-balance A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty cycle), which is then filtered (averaged) by the counter for higher resolution.

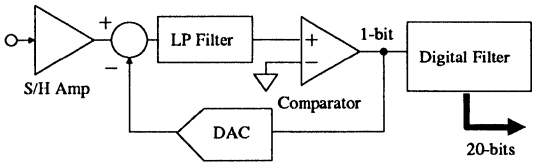
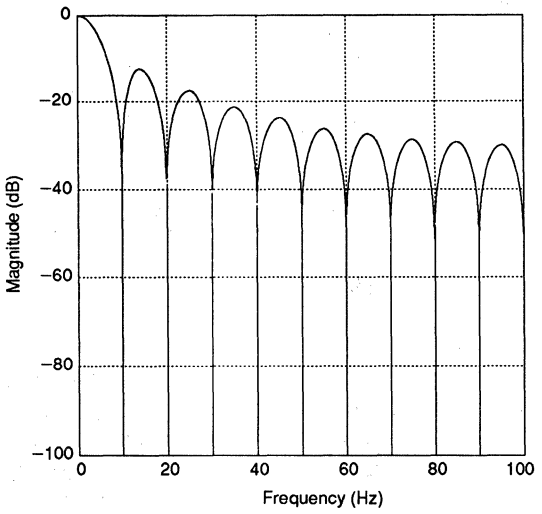


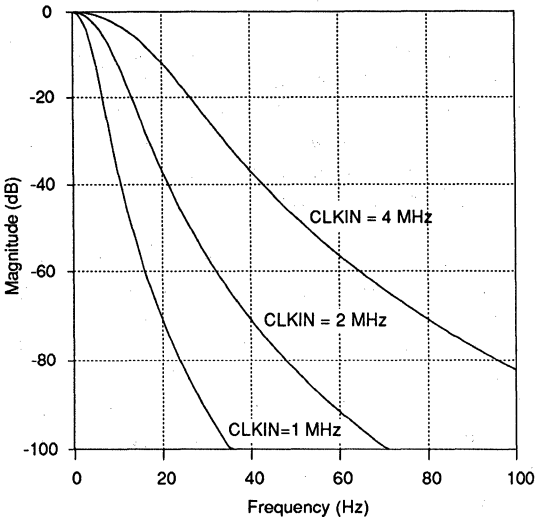
Figure 1. Charge Balance (Delta-Sigma) A/D Converter

The analog modulator of the CS5503 A/D converter is a multi-order delta-sigma modulator. The modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog feedback loop with high open loop gain (see Figure 1). The modulator samples and converts the input at a rate well above the bandwidth of interest. The 1-bit output of the comparator is sampled at intervals based on the clock rate of the part and this information (either a 1 or 0) is conveyed to the digital filter. The digital filter of the CS5503 is much more sophisticated than a simple counter. The filter on the chip has a 6-pole low pass Gaussian response which rolls off at 120 dB/decade (36 dB/octave). The corner frequency of the digital filter scales with the CLKIN signal frequency. In comparison, VFC's and dual slope converters offer (sin x)/x filtering for high frequency rejection (see Figure 2 for a comparison of the characteristics of these two filter types). When operating from a 1 MHz CLKIN signal, the digital filter in the CS5503 offers better than 120 dB rejection of 50 and 60 Hz line frequencies and does not require any type of line synchronization to achieve this rejection. It should be noted that the CS5503 will update its output port almost a 1000 times per second when operating from the 1 MHz clock. This is a much higher update rate (typically by a factor of at least 50 times) than either VFCs or dual-slope converters can offer.

For a more detailed discussion on the delta-sigma modulator see the Application note "Delta-Sigma A/D Conversion Technique Overview" in the application note section of the data book (DB 2.0).



a. Averaging (Integrating) Filter Response (t_{avg} = 100ms)



b. 6-Pole Gaussian Filter Response (CS5503)

Figure 2. Filter Responses

The application note discusses the delta-sigma modulator and some aspects of digital filtering.

OVERVIEW OF THE CS5503

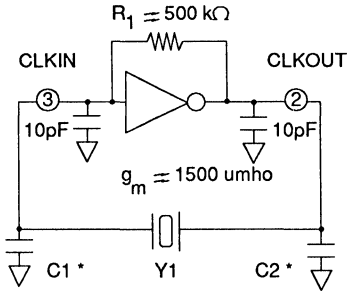
As shown in the block diagram on the front page of the data sheet, the CS5503 can be segmented into five circuit functions. The heart of the chip is the 20-bit charge balance A/D converter. The converter and all of the other circuit functions on the chip must be driven by a clock signal from the clock generator. The serial interface logic outputs the converted data. The calibration microcontroller along with the calibration SRAM (static RAM), supervises the calibration of the CS5503. Each of the segments of the CS5503 has control lines associated with it. The function of each of the pins is described in the pin description section of the data sheet.

Clock Generator

The CS5503 includes a gate which can be connected as a crystal oscillator to provide the CLKIN signal for the chip. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin. Figure 3 illustrates a simple model of the on-chip gate oscillator. The gate has a typical transconductance of 1500 µmho. The gate model includes 10 pF capacitors at the input and output pins. These capacitances include the typical stray capacitance of the pins of the device. The on-chip gate oscillator of the CS5503 is designed to properly operate without additional loading capacitors when using a 4.096 MHz (or 4.000 MHz) crystal. If other crystal frequencies or if ceramic resonators are used, loading capacitors may be necessary for reliable operation of the oscillator. Table 1 illustrates some typical capacitor values to be used with selected resonating elements.

CLKOUT (pin 2) can be used to drive one external CMOS gate for system clock requirements.

Caution: A clock signal should always be present whenever $\overline{\text{SLEEP}}$ is inactive ($\overline{\text{SLEEP}}$ = VD+). If no clock is provided to the part when not in $\overline{\text{SLEEP}}$, the part may draw excess current and



* See Table 1

Figure 3. On-chip Gate Oscillator Model

Resonators	C1	C2
Ceramic		
200 kHz	330pF	470pF
455 kHz	100pF	100pF
1.0 MHz	50pF	50pF
2.0 MHz	20pF	20pF
Crystals		
2.000 MHz	30pF	30pF
3.579 MHz	20pF	20pF
4.096 MHz	None	None

Table 1. Resonator Loading Capacitors

possibly even lose its calibration data. This is because the device utilizes dynamic refreshed logic internally.

Serial Interface Logic

The digital filter in the CS5503 computes a 20-bit digital word representative of the analog signal and places this data in the serial port. The CS5503 serial port can operate in two different serial interface modes depending upon the MODE pin selection.

The following serial output modes are available:

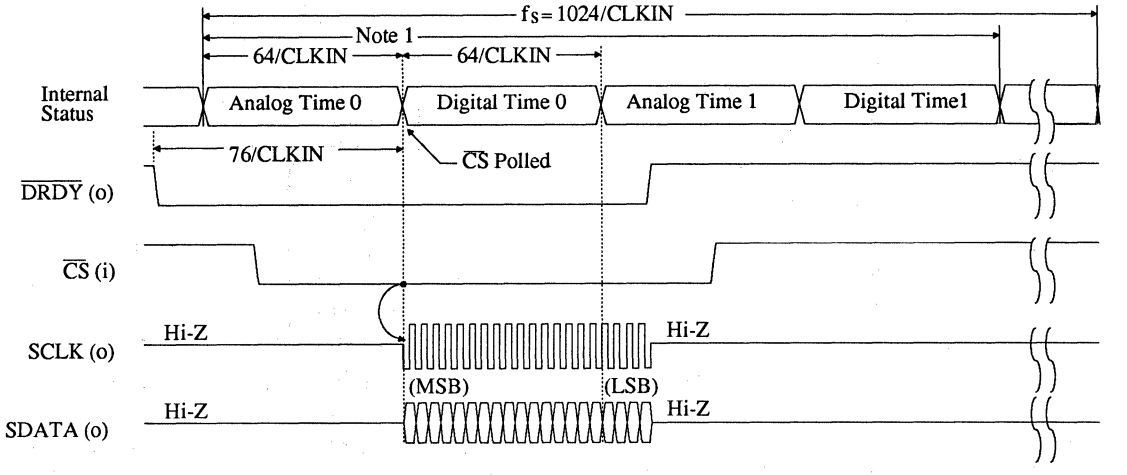
SSC (Synchronous Self-Clocking) mode;
MODE pin tied to VD+ (+5V).

SEC (Synchronous External Clocking) mode;
MODE pin tied to DGND.

The two serial interface modes are discussed below. See the Appendix of the CS5501 data sheet to see examples of how this type of port interface can be connected to serial-to-parallel registers and to microcontrollers (8051, 68HC11, COPS444, and TMS70X2).

Synchronous Self-Clocking Mode

When operated in the SSC mode (MODE pin tied to VD+), the CS5503 furnishes both serial output data (SDATA) and an internally-generated serial clock (SCLK). The timing for this mode is illustrated in Figures 4 and 5. In the CS5503, a filter cycle occurs every 1024 cycles of CLKIN. During each filter cycle the status of the $\overline{CS}$ is polled at eight specific times during the cycle. If $\overline{CS}$ is low when it is polled, the CS5503 begins clocking the data bits out, MSB first, at a SCLK output rate of CLKIN/4. Once transmission is complete, $\overline{DRDY}$ rises and both SDATA and SCLK outputs go into a high impedance state. A filter cycle begins each time $\overline{DRDY}$ falls. If the $\overline{CS}$ line is not active, $\overline{DRDY}$ will return high 1020 clock cycles after it falls. Four clock cycles later $\overline{DRDY}$ will fall to signal that the serial port has been updated with new data and that a new filter cycle has begun. The first $\overline{CS}$ polling during a filter cycle occurs 76 clock cycles after $\overline{DRDY}$ falls (the rising edge of CLKIN on which $\overline{DRDY}$ falls is considered clock cycle number one). Subsequent pollings of $\overline{CS}$ occur at intervals of 128 clock cycles thereafter (76, 204, 332, etc.). The $\overline{CS}$ signal is polled at the beginning of each of eight data output windows which occur in a filter cycle. To transmit data during any one of the eight output windows, $\overline{CS}$ must be low at least three CLKIN cycles before it is polled. If $\overline{CS}$ does not meet this set-up time, data will not be transmitted during the window time. Furthermore, $\overline{CS}$ is not latched internally and therefore must be held low during the entire data transmission to obtain all 20 bits of data.



Note 1: There are 16 analog and digital settling periods per filter cycle (4 are shown). Data can be output in the SSC mode in only 1 of the 8 digital time periods in each filter cycle.

Figure 4. Internal Timing

The eighth output window time overlaps the time in which the serial output port is to be updated. If the $\overline{CS}$ is recognized as being low when it is polled for the eighth window time, data will be output as normal, but the serial port will not be updated with new data until the next serial port update time. Under these conditions, the serial port will experience an update rate of only 2 kHz (CLKIN = 4.096 MHz) instead of the regular 4 kHz serial port update rate.

Upon completion of transmission of all 20 data bits the SCLK and SDATA outputs will go to a high impedance state even with $\overline{CS}$ held low. In the event that $\overline{CS}$ is taken high before all data bits are output, the SDATA and SCLK outputs will

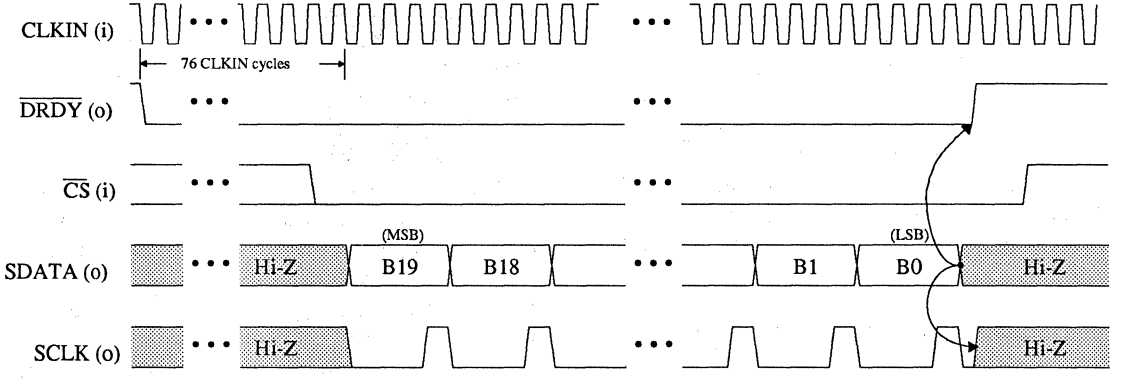


Figure 5. Synchronous Self-Clocking (SSC) Mode Timing

complete the current data bit output and go to a high impedance state when SCLK goes low.

Synchronous External Clocking Mode

When operated in the SEC mode (MODE pin tied to DGND), the CS5503 outputs the data in its serial port at a rate determined by an external clock which is input into the SCLK pin. In this mode the output port will be updated every 1024 CLKIN cycles. $\overline{DRDY}$ will go low when new data is loaded into the output port. If $\overline{CS}$ is not active, $\overline{DRDY}$ will return positive 1020 CLKIN cycles later and remain so for four CLKIN cycles. If $\overline{CS}$ is taken low it will be recognized immediately unless it occurs while $\overline{DRDY}$ is high for the four clock cycles. As soon as $\overline{CS}$ is recognized, the SDATA output will come out of its high-impedance state and present the MSB data bit. The MSB data bit will remain present until a falling edge of SCLK occurs to advance the output to the MSB-1 bit. If the $\overline{CS}$ and external SCLK are operated asynchronously to CLKIN, errors can result in the output data unless certain precautions are taken. If $\overline{CS}$ is activated asynchronously, it may occur during the four clock cycles when $\overline{DRDY}$ is high and therefore not be recognized immediately. To be certain that data misread errors will not result if $\overline{CS}$ occurs at this time, the SCLK input should not transition high to latch the MSB until four CLKIN cycles plus 160 ns after $\overline{CS}$ is taken low. This assures that $\overline{CS}$ will be recognized and the MSB bit will become stable before the SCLK transitions positive to latch the MSB data bit.

When SCLK returns low the serial port will present the MSB-1 data bit on its output. Subsequent cycles of SCLK will advance the data output. When all data bits are clocked out, $\overline{DRDY}$ will then go high and the SDATA output will go into a high impedance state. If the $\overline{CS}$ input goes low and all of the data bits are not clocked out of the port, filter cycles will continue to occur but the output serial port will not be updated with new data ($\overline{DRDY}$ will remain low). If $\overline{CS}$ is taken high at any time, the SDATA output pin will go to a high impedance state. If any of the 20 bits in the serial port have not been clocked out, they will remain available until $\overline{DRDY}$ returns high for four clock cycles. After this $\overline{DRDY}$ will fall and the port will be updated with a new 20 bit word. It is acceptable to clock out less than all 20 bits if $\overline{CS}$ is returned high to allow the port to be updated. Figure 6 illustrates the serial port timing in the SEC mode.

Linearity Performance

The CS5503, like other charge-balance converters, has very good differential linearity. The

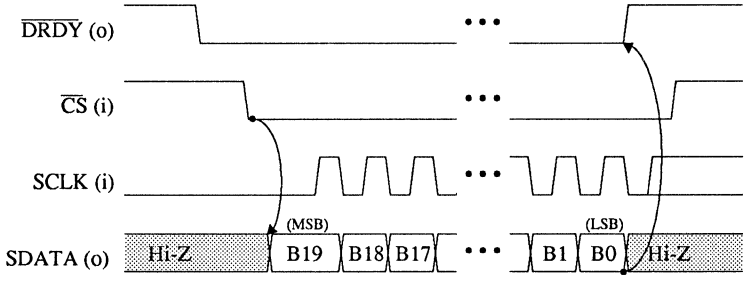


Figure 6. Synchronous External-Clocking (SEC) Mode Timing

part exhibits typically no missing codes to the 20-bit level.

The CS5503 has excellent integral linearity. The superb integral linearity in the CS5503 is accomplished with a well-designed charge-balance architecture. The device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To insure that the CS5503 achieves excellent performance over time and temperature, it uses digital calibration techniques to minimize offset and gain errors to typically within ± 4 LSB at 20 bits.

Converter Calibration

The CS5503 offers both self-calibration and system level calibration capability. To understand the CS5503 calibration features, a basic comprehension of the internal workings of the converter are helpful. As mentioned previously in this data sheet, the converter consists of two sections. First is the analog modulator which is a delta-sigma type charge-balance converter. This is followed by a digital filter. The filter circuitry is actually an arithematic logic unit (ALU) whose architecture and instructions execute the filter function. The modulator (explained in more detail in the applications note "Delta-Sigma Conversion Technique Overview") uses the VREF voltage connected to pin 10 to determine the magnitude of the voltages used in its feedback DAC. The modulator accepts an analog signal at its input and produces a data stream of 1's and 0's as its output. This data stream value can change (from 1 to 0 or vice versa) every 256 CLKIN cycles. As the input voltage increases the ratio of 1's to 0's out of the modulator increases proportionally. (The 1's density of the data stream out of the modulator therefore provides a digital representation of the analog input signal where the 1's density is defined as the ratio of the number of 1's to the number of 0's out of the modulator for a given period of time.) The 1's density output of the modulator is also a function of the voltage on the VREF pin. If the voltage on the VREF pin increases in value (say, due to temperature drift), and the analog input voltage into the modulator remains constant, the 1's density output of the modulator will decrease (less 1's will occur). The analog input into the modulator which is necessary to produce a given binary output code from the converter is ratiometric to the voltage on the VREF pin. This means that if VREF increases by one per cent, the analog signal on AIN must also increase by one per cent to maintain the same binary output code from the converter.

For a complete calibration to occur, the calibration microcontroller inside the CS5503 needs to record the data stream 1's density out of the modulator for two different input conditions. First, a "zero scale" point must be presented to the modulator. Then a "full scale" point must be presented to the modulator. In unipolar self-cal mode the zero scale point is AGND and the full scale point is the voltage on the VREF pin. The calibration microcontroller then remembers the 1's density out of the modulator for each of these points and calculates a slope factor (LSB/uV). This slope factor represents the gain slope for the input to output transfer function of the converter. In unipolar mode the calibration microcontroller determines the slope factor by dividing the span between the zero point and the full scale point by the total resolution of the converter (2^{20}) resulting in 1,048,578 segments. In bipolar mode the calibration microcontroller divides the span between the zero point and the full scale point into 524,288 segments. It then extends the measurement range 524,288 segments below the zero scale point to achieve bipolar measurement capability. In either unipolar or bipolar modes the calculated slope factor is saved and later used to calculate the binary output code when an analog signal is present at the AIN pin during measurement conversions.

System calibration allows the A/D converter to compensate for system gain and offset errors (see Figure 7). System calibration performs the same slope factor calculations as self-cal but uses

voltage values presented by the system to the AIN pin for the zero scale point and for the full scale point. Table 2 depicts the calibration modes available. Two system calibration modes are listed. The first mode offers system level calibration for system offset and for system gain. This is a two-step calibration. The zero scale point (system offset) must be presented to the converter first. The voltage that represents zero scale point must be input to the converter before the calibration step is initiated and must remain stable until the step is complete. The $\overline{DRDY}$ output from the converter will signal when the step is complete by going low. After the zero scale point is calibrated, the voltage representing the full scale point is input to the converter and the second calibration step is initiated. Again the voltage must remain stable thoughout the calibration step.

This two-step calibration mode offers another calibration feature. After a two-step calibration sequence (system offset and system gain) has been properly performed, additional offset calibrations can be performed by themselves to reposition the gain slope (the slope factor is not changed) to adjust its zero reference point to the new system zero reference value.

A second system calibration mode is available which uses an input voltage for the zero scale calibration point, but uses the VREF voltage as the full scale calibration point.

Whenever a system calibration mode is used, there are limits to the amount of offset and to the amount of span which can be accomodated. The range of input span which can be accomodated in either unipolar or bipolar mode is restricted to not less than 80% of the voltage on VREF and not more than 200% of (VREF + 0.1) V. The amount of offset which can be calibrated depends upon whether unipolar or bipolar mode is being used. In unipolar mode the system calibration modes can handle offsets as positive as 20% of VREF (this is restricted by the minimum span requirement of 80% VREF) or as negative as -(VREF + 0.1) V. This capability enables the unipolar mode of the CS5503 to be calibrated to mimic bipolar mode operation.

In the bipolar mode the system offset calibration range is restricted to a maximum of ±40% of VREF. It should be noted that the span restrictions limit the amount of offset which can be calibrated. The span range of the converter in bipolar mode extends an equidistance (+ and -) from the voltage used for the zero scale point. When the zero scale point is calibrated it must not cause either of the two endpoints of the bipolar transfer function to exceed the positive or the negative input overrange points (+(VREF + 0.1) V or -(VREF + 0.1) V). If the span range is set to a minimum (80% VREF) the offset voltage can move ±40% VREF without causing the end points of the transfer function to exceed the overrange points. Alternatively, if the span range is set to 200% of VREF, the input offset cannot

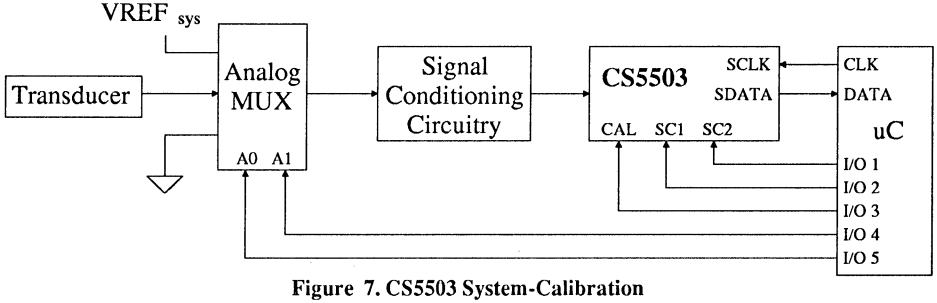


Figure 7. CS5503 System-Calibration

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence	Calibration Time
↴	0	0	Self-Cal	AGND	VREF	One Step	3,145,655/CLKIN
↴	1	1	System Offset & System Gain	AIN	-	1st Step	1,052,599/CLKIN
↴	0	1		-	AIN	2nd Step	1,068,813/CLKIN
↴	1	0	System Offset	AIN	VREF	One Step	2,117,389/CLKIN

* $\overline{DRDY}$ remains high throughout the calibration sequence. In Self-Cal mode (SC1 and SC2 low) $\overline{DRDY}$ falls once the CS5503 has settled to the analog input. In all other modes $\overline{DRDY}$ falls immediately after the calibration term has been determined.

Table 2. CS5503 Calibration Control

move more than +0.1 or - 0.1 V before an endpoint of the transfer function exceeds the input overrange limit.

Initiating Calibration

Table 2 illustrates the calibration modes available in the CS5503. Not shown in the table is the function of the BP/$\overline{UP}$ pin which determines whether the converter is calibrated to measure bipolar or unipolar signals. A calibration step is initiated by bringing the CAL pin (13) high for at least 4 CLKIN cycles to reset the part and then bringing CAL low. The states of SC1 (pin 4) and SC2 (pin 17) along with the BP/$\overline{UP}$ (pin 12) will determine the type of calibration to be performed. All three signals should be stable before the CAL pin is taken positive. The SC1 and SC2 inputs are latched when CAL goes high. The BP/$\overline{UP}$ input is not latched and therefore must remain in a fixed state thoughout the calibration and measurement cycles. Any time the state of the BP/$\overline{UP}$ pin is changed, a new calibration cycle must be performed to enable the CS5503 to properly function in the new mode.

When a calibration step is initiated, the $\overline{DRDY}$ signal will go high and remain high until the step is finished. Table 2 illustrates the number of clock cycles each calibration requires. Once a calibration step is initiated it must finish before a new calibration step can be executed. In the two step system calibration mode, the offset calibration step must be initiated before initiating the gain calibration step.

When a self-cal is completed $\overline{DRDY}$ falls and the output port is updated with a data word that represents the analog input signal at the AIN pin. When a system calibration step is completed, $\overline{DRDY}$ will fall and the output port will be updated with the appropriate data value (zero scale point, 00000[H]; full scale point, FFFFF[H]). In the system calibration mode, the digital filter must settle before the output code will represent the value of the analog input signal.

Tables 3 and 4 indicate the output code size and output coding of the CS5503 in its various modes. The calibration equations which represent

$$D_{OUT} = Slope\ (A_{IN} - Unipolar\ Offset) + 0.5\ LSB$$

a. Unipolar Calibration

$$D_{OUT} = Slope\ (A_{IN} - Bipolar\ Offset) + 2^{19} + 0.5\ LSB$$

b. Bipolar Calibration

Figure 8. CS5503 Calibration Equations

Cal Mode	Zero Scale	Gain Factor	1LSB	
			Unipolar	Bipolar
Self-Cal	AGND	VREF	$\frac{VREF}{1,048,576}$	$\frac{2VREF}{1,048,576}$
System Cal	SOFF	SGAIN	$\frac{SGAIN - SOFF}{1,048,576}$	$\frac{2(SGAIN - SOFF)}{1,048,576}$

Table 3. Output Code Size After Calibration

the transfer function of the CS5503 are shown in Figure 8.

Underrange And Overrange Considerations

The input signal range of the CS5503 will be determined by the mode in which the part is calibrated. Table 4 indicates the input signal range in the various modes of operation. If the input signal exceeds the full scale point the converter will output all ones. If the signal is less than the zero scale point (in unipolar) or more negative in magnitude than minus the full scale point (in bipolar) it will output all zeroes.

Note that the modulator-filter combination in the CS5503 is designed to accurately convert and filter input signals with noise excursions which extend up to 100 mV below the analog value which produces all zeros out or above the analog value which produces all ones out. Overrange noise excursions greater than 100 mV may increase output noise.

3

Input Voltage, Unipolar Mode			Input Voltage, Bipolar Mode	
System-Cal	Self-Cal	Output Codes	Self-Cal	System-Cal
>(SGAIN - 1.5 LSB)	>(VREF - 1.5 LSB)	FFFFF	>(VREF - 1.5 LSB)	>(SGAIN - 1.5 LSB)
SGAIN-1.5 LSB	VREF - 1.5 LSB	$\frac{FFFFF}{FFFFE}$	VREF - 1.5 LSB	SGAIN-1.5 LSB
(SGAIN-SOFF)/2 - 0.5 LSB	VREF/2 - 0.5 LSB	$\frac{80000}{7FFFF}$	AGND - 0.5 LSB	SOFF - 0.5 LSB
SOFF + 0.5 LSB	AGND + 0.5 LSB	$\frac{00001}{00000}$	-VREF + 0.5 LSB	-SGAIN + 2 SOFF + 0.5 LSB
<(SOFF + 0.5 LSB)	<(AGND + 0.5 LSB)	00000	<(-VREF + 0.5 LSB)	<(-SGAIN + 2 SOFF + 0.5 LSB)

Table 4. Output Coding

All pins of the CS5503 include diodes which clamp the input signals to the positive and negative supplies. If a signal on any pin (including AIN) exceeds the supply voltage (either + or -) a clamp diode will be forward biased. Under these fault conditions the CS5503 might be damaged. Under normal operating conditions (with the power supplies established), the device will survive transient currents through the clamp diodes up to 100 mA and continuous currents up to 10 mA. The drive current into the AIN pin should be limited to a safe value if an overvoltage condition is likely to occur. See the application note "Buffer Amplifiers for the CS501X Series of A/D Converters" for further discussion on the clamp diode input structure and on current-limiting circuits.

System Synchronization

If more than one CS5503 is included in a system which is operating from a common clock, all of the CS5503's can be synchronized to sample and output at exactly the same time. This can be accomplished in either of two ways. First, a single CAL signal can be issued to all the CS5503's in the system. To insure synchronization on the same clock signal the CAL signal should go low on the falling edge of CLKIN. Or second, a common $\overline{\text{SLEEP}}$ control signal can be issued. If the $\overline{\text{SLEEP}}$ signal goes positive with the appropriate set up time to CLKIN, all parts will be synchronized on the same clock cycle.

Analog Input Impedance Considerations

The analog input of the CS5503 can be modeled as illustrated in Figure 9. A capacitor of approximately 20 pF is used to dynamically sample the input signal. Every 64 CLKIN cycles the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) will be required from the input source to settle the voltage on the sample capacitor to its final value. The voltage at the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows 64 cycles of CLKIN for the voltage on the sample capacitor to settle to its final value. The equation which defines settling time is:

$$Vo = Vin\ [1 - e^{-t/RC}]$$

Where Vo is the final settled value, Vin is the value of the input signal, R is the value of the input source resistance, C is the 20 pF sample capacitor. The value of t is equal to 64/CLKIN.

From this basic equation the following equation can be developed which indicates the maximum acceptable source resistance (R_{SMAX}) for an error of V_e:

$$R_{Smax} = \frac{64}{CLKIN\ (20pF)\ \ln\ (100mV/V_e)}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of V_e is the maximum error voltage which is acceptable.

For a maximum error voltage (V_e) of 600 nV (1/4LSB at 20-bits), the above equation indicates that when operating from a 4.096 MHz CLKIN, source resistances up to 60 kΩ are acceptable. If higher input source resistances are desired the CLKIN rate can be reduced to yield a longer settling time for the 64 cycle period.

An RC filter may be added in front of the CS5503 to reduce high frequency noise (see Figure 14). With an external capacitor added (from AIN to AGND) the following equation will specify the maximum allowable source resistance:

$$R_{Smax} = \frac{64}{CLKIN\ (20pF+C_{ext})\ \ln\ [([20pF/\ (20pF+C_{ext})]100mV)\ /V_e]}$$

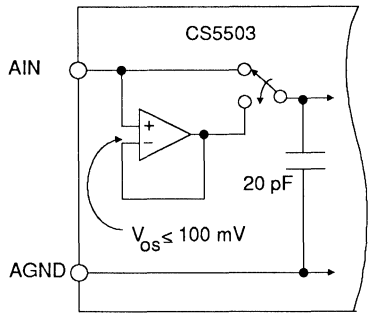


Figure 9. Analog Input Model

Analog Input Drift Considerations

The CS5503 analog input uses chopper-stabilization techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 10 indicates the typical offset drift due to temperature changes experienced after calibration at 25 °C. Drift is relatively flat up to about 75 °C. Above 75 °C leakage current becomes the dominant source of offset drift. Leakage currents approximately double with each 10 °C of temperature increase. Therefore the offset drift due to leakage current increases as the temperature increases. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples. In conclusion, the offset drift increases with temperature and is inversely proportional to the CLKIN rate. To minimize offset drift with increased temperature, higher CLKIN rates are desireable. At temperatures above 100 °C, a CLKIN rate above 1 MHz is recommended. The effects of offset drift due to temperature changes can be eliminated by recalibrating the CS5503 whenever the temperature has changed.

Gain drift within the converter depends predominately upon the temperature tracking of internal capacitors. Gain drift is not affected by leakage currents, therefore gain drift is significantly less than comparable offset errors due to temperature increases. The typical gain drift of the CS5503 is less than 40 LSB's over the specified temperature range.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. The CS5503 can be recalibrated at any temperature to remove the effects of these errors.

Integral and differential linearity are not significantly affected by temperature changes.

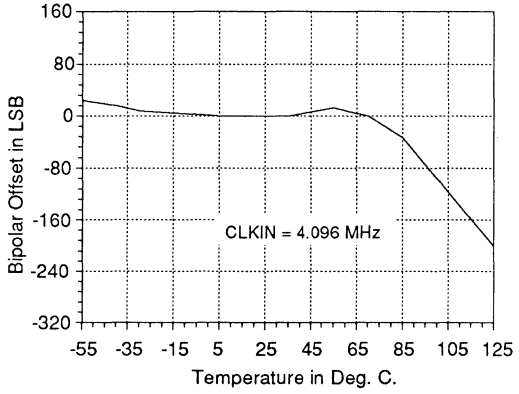


Figure 10. Typical Self-Cal Bipolar Offset vs. Temperature After Calibration at 25° C

Filtering

At the system level, the CS5503's digital filter can be modeled exactly like an analog filter with a few minor differences. Digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially over-range the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5503's analog modulator and digital filter reserve headroom such that the device can process signals with 100mV excursions above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

The digital filter's corner frequency occurs at CLKIN/409,600, where CLKIN is the CLKIN frequency. With a 4.096MHz clock, the filter corner is at 10Hz and the output register is updated at a 4kHz rate. The CLKIN frequency can be reduced with a proportional reduction in the filter corner frequency and in the update rate to the output register. A plot of the filter response is shown in the specification tables section of this data sheet.

The CS5503's internal digital filtering creates a 6-pole Gaussian relationship. With its corner frequency set at 10Hz for minimized settling time, the CS5503 offers approximately 55dB rejection at 60Hz to signals coming into either the AIN or VREF pins. With a 5Hz cut-off, 60Hz rejection increases to more than 90dB.

The digital filter (rather than the analog modulator) dominates the converter's settling for step-function inputs. Figure 11 illustrates the settling characteristics of the filter. The vertical axis is normalized to the input step size. The horizontal axis is in filter cycles. With a full scale input step (2.5 V in unipolar mode) the output will exhibit an overshoot of about 4 LSBs.

Anti-Alias Considerations

The digital filter in the CS5503 does not provide rejection around integer multiples of the oversampling rate [(N*CLKIN)/256, where N = 1,2,3,...]. That is, with a 4.096 MHz CLKIN the noise on the analog input signal within the narrow ± 10 Hz bands around the 16 kHz, 32 kHz, 48 kHz, etc., passes unfiltered to the digital output. Most broadband noise will be very well filtered because the CS5503 uses a very high oversampling ratio of 800 (16 kHz : 2x10 Hz). Broadband noise is reduced by:

$$e_{out} = e_{in} \sqrt{2f_{-3dB}/ f_s}$$

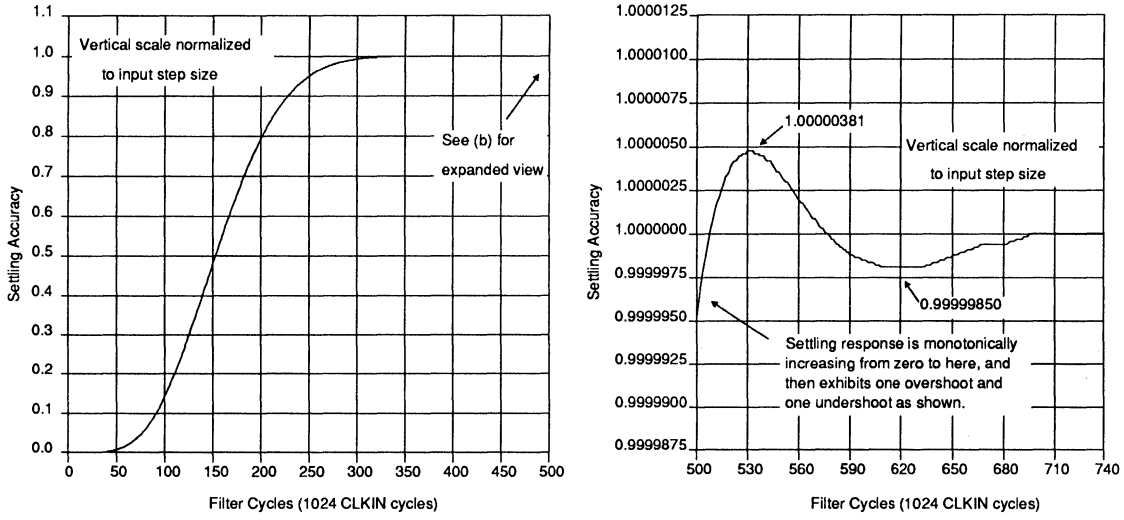
$$e_{out} = 0.035\ e_{in}$$

where e_{in} and e_{out} are rms noise terms referred to the input. Since f_{-3dB} equals CLKIN/409,600 and f_s equals CLKIN/256, the digital filter reduces white, broadband noise by 96.5% independent of the CLKIN frequency. For example, the CS5503 would reduce a typical operational amplifier's 50µV rms noise to 1.75µV rms, or 0.4 LSB's rms at the 20-bit level.

Simple high frequency analog filtering in the signal conditioning circuitry can aid in removing energy at multiples of the sampling rate.

Post Filtering

With a constant input voltage the output codes from the CS5503 will exhibit some variation due to noise. The converter itself exhibits (typically) 1.6 LSB rms noise (at 20 bits) in its output codes. Additional variation in the output codes can arise due to noise from the input signal source and from the voltage reference. Post filtering (digital averaging) will be necessary to achieve less than 1 LSB p-p noise at the 20-bit level. The CS5503 has peak noise less than the 18-bit level without additional filtering if care is exercised in the design of the voltage reference and the input signal conditioning circuitry. Noise in the bandwidth from dc to 10 Hz on both the AIN and VREF inputs should be minimized to insure maximum performance.



(a) Settling Time Due to Input Step Change **(b) Expanded Version of (a)**

Figure 11. Output Settling Time

As the amount of noise will be highly system dependent, a specific recommendation for post filtering for all applications cannot be stated. The following guidelines are helpful. Realize that the digital filter in the CS5503, like any other low pass filter, acts as an information storage unit. The filter retains past information for a period of time even after the input signal has changed. The implication of this is that immediately sequential 20-bit updates to the serial port contain highly correlated information. To most efficiently post filter the CS5503 output data, uncorrelated samples should be used. Samples which have sufficiently reduced correlation can be obtained if the CS5503 is allowed to execute 200 filter cycles between each subsequent data word collected for post filtering.

The character of the noise in the data will influence the post filtering requirements. As a general rule, averaging N uncorrelated data samples will reduce noise by $1/\sqrt{N}$. While this rule assumes that the noise is white (which is true for the CS5503 but not true for all real system signals between dc and 10 Hz), it does offer a starting point for developing a post filtering algorithm for removing the noise from the data. The algorithm will have to be empirically tested to see if it meets the system requirements. It is recommended that any testing include input signals across the entire input span of the converter as the signal level will affect the amount of noise from the reference input which is transferred to the output data.

Voltage Reference

The voltage reference applied to the VREF input pin defines the analog input range of the CS5503. The preferred reference is 2.5V, but the device can typically accept references from 1V to 3V. Input signals which exceed 2.6 V (+ or -) can cause some linearity degradation.

The circuitry inside the VREF pin is identical to that as seen at the AIN pin. The sample capacitor (see Figure 9) requires packets of charge from the external reference just as the AIN pin does. Therefore the same settling time requirements apply. Most reference IC's can handle this

dynamic load requirement without inducing errors. They exhibit sufficiently low output impedance and wide enough bandwidth to settle to within the necessary accuracy in the requisite 64 CLKIN cycles.

Noise from the reference is filtered by the digital filter in the CS5503, but the reference should be chosen to minimize noise below 10 Hz. The CS5503 typically exhibits 1.6 LSB rms noise in its measurements. This specification assumes a clean reference voltage. Many monolithic bandgap references are available which can supply 2.5 V for use with the CS5503. Many of these devices are not specified for noise, especially in the 0.1 to 10 Hz bandwidth. Some of these devices may exhibit noise characteristics which degrade the performance of the CS5503.

Power Supplies And Grounding

The CS5503 uses the analog ground connection, AGND, as a measurement reference node. It carries no power supply current. The AGND pin is to be used as the reference node for both the analog input signal and for the reference voltage which is input into the VREF pin.

The analog and digital supply pins to the CS5503 chip are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF capacitors if maximum performance from the CS5503 is expected. The System Connection Diagram for the CS5503 is illustrated at the end of this section of the data sheet (See Figure 14).

As a CMOS device, the CS5503 requires that the positive analog supply voltage always be greater than or equal to the positive digital supply voltage. If the voltage on the positive digital supply should ever become greater than the voltage on the positive analog supply, diode junctions in the CMOS structure which are normally reverse-biased will become forward biased. This may cause the part to draw high currents and experience permanent damage. The connections shown in Figure 14 eliminate this possibility.

To insure reliable operation of the CS5503, be certain that power is applied to the part before signals at AIN, VREF, or the logic input pins are present. If current is supplied into any pin before the chip is powered up, latch up may result. As a system, it is desirable to power the CS5503, the voltage reference, and the analog signal conditioning circuitry from the same primary source. If separate supplies are used, it is recommended that the CS5503 is powered up first. If a common power source is used for the analog signal conditioning circuitry as well as the A/D converter, this power source should be applied before application of power to the digital logic supply.

The CS5503 exhibits good power supply rejection for frequencies within the passband (dc to 10 Hz). Any small offset or gain error caused by long term drift of the power supplies can be removed by recalibration. Above 10 Hz the digital filter will provide additional rejection. When the benefits of the digital filter are added to the regular power supply rejection the effects of line frequency variations (60 Hz) on the power supplies will be reduced greater than 120 dB. If a dc-dc converter is used to generate the supply voltages for the CS5503, it should not operate at the sampling frequency of the CS5503 or at integer multiples thereof. At these frequencies the digital filter will not aid in power supply rejection. See Anti-Alias Considerations section of this data sheet.

The recommended system connection diagram for the CS5503 is illustrated in Figure 14. Note that any digital logic inputs which are to be unused should be tied to either DGND or the VD+ as appropriate. They should not be left floating; nor should they be tied to some other logic supply voltage in the system.

Power Up and Initialization

Upon power up, a calibration cycle must be initiated at the CAL pin to insure a consistent starting condition and to initially calibrate the device. The CAL pin must be strobed high for a minimum of 4 CLKIN cycles. The falling edge will initiate a calibration cycle. A simple power-on reset circuit can be built using a resistor and capacitor (see Figure 12). The resistor and capacitor values should allow for clock or oscillator startup time.

Due to the CS5503's low power dissipation and low temperature drift, no warm-up time is required to accommodate any self-heating effects. However, the voltage reference should have stabilized before calibration is initiated.

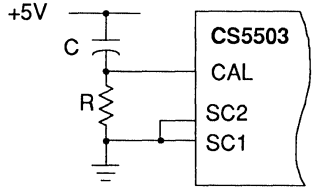


Figure 12. Power-On Reset Circuitry (Self-Calibration Only)

Sleep Mode

The CS5503 includes a sleep mode ($\overline{SLEEP}$ = DGND) which shuts down the internal analog and digital circuitry reducing power consumption to less than 10 µW. All calibration coefficients are retained in memory such that no time is required after "awakening" for recalibration. Still, the CS5503 will require time for the digital filter to settle before an accurate reading will occur after a rising edge on $\overline{SLEEP}$ occurs.

Battery Backed-Up Calibrations

The CS5503 uses SRAM to store calibration information. The contents of the SRAM will be lost whenever power is removed from the CS5503. Figure 13 shows a battery back-up scheme that can be used to retain the calibration memory during system down time and/or protect it against intermittent power loss. Note that upon loss of power, the CS5503's $\overline{SLEEP}$ input goes low, reducing power consumption to just 10 µW. Lithium cells of 3.6 V are available which average 1750 mA-hours before they drop below the typical 2 V memory-retention spec of the CS5503. Calibration memory could therefore be maintained for approximately 20 years down time, allowing one-time factory calibrations of the transducer and all electronics.

When $\overline{SLEEP}$ is active ($\overline{SLEEP}$ = DGND) both VD+ and VA+ must remain powered to no less than 2 V to retain calibration memory. The VD- and VA- voltages can be reduced to 0 V but must not be allowed to go above ground potential. The negative supply must exhibit low source impedance in the powered-down state as the current into the VA+ pin flows out the VA- pin. (AGND is only a reference node. No power supply current flows in or out of AGND.) Care should be taken to insure that logic inputs are maintained at either VD+ or DGND potential when $\overline{SLEEP}$ is low.

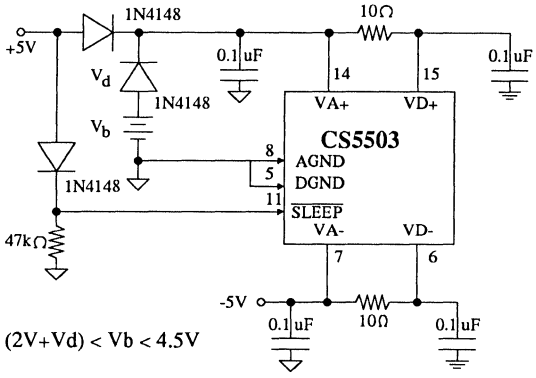


Figure 13. Example Calibration Memory Battery Back-up Circuit

Note that battery life could be shortened if the +5 V supply drops slowly during power-down. As the supply drops below the battery voltage but not yet below the logic threshold of the $\overline{\text{SLEEP}}$ pin, the battery will be supplying the CS5503 at full power (typically 3 mA). Faster transitions at the $\overline{\text{SLEEP}}$ pin can be triggered using a resistive divider or a simple resistor network to generate the $\overline{\text{SLEEP}}$ input from the +5 V supply.

Output Loading Considerations

To maximize performance of the CS5503, the output drive currents from the digital output lines should be minimized. It is recommended that CMOS logic gates (4000B, 74HC, etc.) be used to provide minimum loading. If it is necessary to drive an opto-isolator the outputs of the CS5503 should be buffered. An easy means of driving the LED of an optoisolator is to use a 2N7000 or 2N7002 low-cost FET.

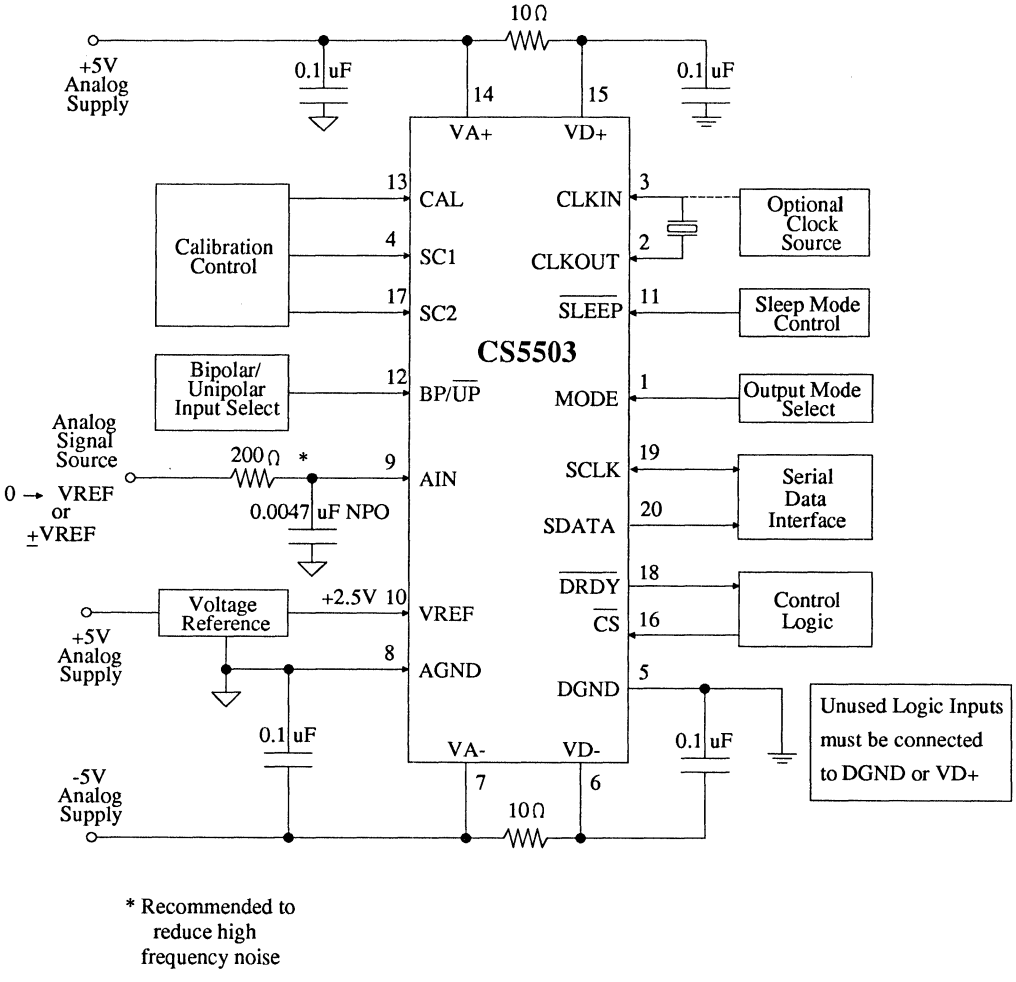
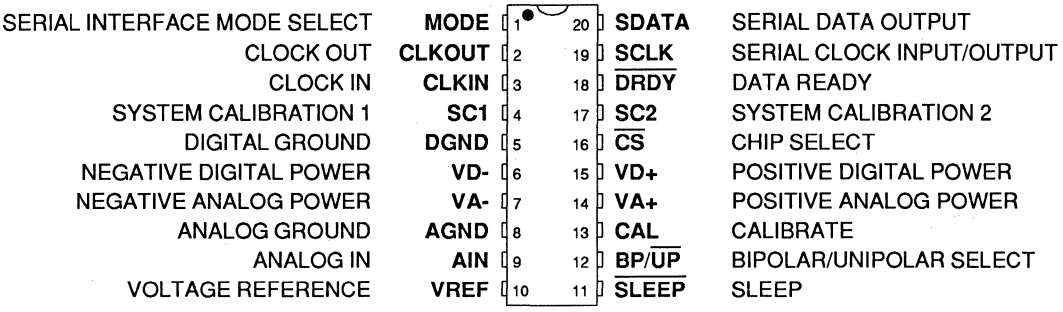


Figure 14. System Connection Diagram

PIN DESCRIPTIONS



*Pinout applies to both DIP and SOIC packages

Clock Generator

CLKIN; CLKOUT -Clock In; Clock Out, Pins 3 and 2.

A gate inside the CS5503 is connected to these pins and can be used with a crystal or ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. When not in SLEEP mode, a master clock (CLKIN) should be present at all times.

Serial Output I/O

MODE -Serial Interface Mode Select, Pin 1.

Selects the operating mode of the serial port. If MODE is tied to DGND, the CS5503 will operate in the SEC (Synchronous External-Clocking) mode, with the SCLK pin operating as an *input* and the output appearing MSB-first. If MODE is tied to VD+ (+5V), the CS5503 will operate in its SSC (Synchronous Self-Clocking) mode, with SCLK providing a serial clock *output* of CLKIN/4 (25% duty-cycle).

$\overline{\text{DRDY}}$ -Data Ready, Pin 18.

$\overline{\text{DRDY}}$ goes low every 1024 cycles of CLKIN to indicate that new data has been placed in the output port. $\overline{\text{DRDY}}$ goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when $\overline{\text{SLEEP}}$ is low.

$\overline{\text{CS}}$ -Chip Select, Pin 16.

An input which can be enabled by an external device to gain control over the serial port of the CS5503.

SDATA -Serial Data Output, Pin 20.

Data from the serial port will be output from this pin at a rate determined by SCLK and in a format determined by the MODE pin. It furnishes a high impedance output state when not transmitting data.

SCLK -Serial Clock Input/Output, Pin 19.

A clock signal at this pin determines the output rate of the data from the SDATA pin. The MODE pin determines whether the SCLK signal is an input or output. SCLK may provide a high impedance output when data is not being output from the SDATA pin.

Calibration Control Inputs

SC1; SC2 -System Calibration 1 and 2, Pins 4 and 17.

Control inputs to the CS5503's calibration microcontroller for calibration. The state of SC1 and SC2 determine which of the calibration modes is selected for operation (see Table 2).

BP/$\overline{UP}$ -Bipolar/Unipolar Select, Pin 12.

Determines whether the CS5503 will be calibrated to measure bipolar (BP/$\overline{UP}$ = VD+) or unipolar (BP/$\overline{UP}$ = DGND) input signals. Recalibration is necessary whenever the state of BP/$\overline{UP}$ is changed.

3

CAL -Calibrate, Pin 13.

If brought high for 4 clock cycles or more, the CS5503 is reset and upon returning low a full calibration cycle will begin. The state of SC1, SC2, and BP/$\overline{UP}$ when CAL is brought high determines the type and length of calibration cycle initiated (see Table 2). Also, a single CAL signal can be used to strobe the CAL pins high on several CS5503's to synchronize their operation. Any spurious glitch on this pin may inadvertently place the CS5503 in Calibration mode.

Other Control Input

$\overline{SLEEP}$ -Sleep, Pin 11.

When brought low, the CS5503 will enter a low-power state. When brought high again, the CS5503 will resume operation without the need to recalibrate. After $\overline{SLEEP}$ goes high again, the CS5503's output will require the filter to settle to obtain an accurate measure of the input signal. The $\overline{SLEEP}$ input can also be used to synchronize sampling and the output updates of several CS5503's.

Analog Inputs

VREF -Voltage Reference, Pin 10.

Analog reference voltage input.

AIN -Analog Input, Pin 9.

Power Supply Connections

VD+ -Positive Digital Power, Pin 15.

Positive digital supply voltage. Nominally +5 volts.

VD- -Negative Digital Power, Pin 6.

Negative digital supply voltage. Nominally -5 volts.

DGND -Digital Ground, Pin 5.
Digital ground.

VA+ -Positive Analog Power, Pin 14.
Positive analog supply voltage. Nominally +5 volts.

VA- -Negative Analog Power, Pin 7.
Negative analog supply voltage. Nominally -5 volts.

AGND -Analog Ground, Pin 8.
Analog ground.

SPECIFICATION DEFINITIONS

Linearity Error - The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Linearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full-Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSBs.

Unipolar Offset - The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSBs.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSBs.

Bipolar Negative Full-Scale Error - The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The Ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSBs.

Positive Full-Scale Input Overrange - The absolute maximum positive voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Negative Full-Scale Input Overrange - The absolute maximum negative voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Offset Calibration Range - The CS5503 calibrates its offset to the voltage applied to the AIN pin when in system calibration mode. The first code transition defines Unipolar Offset when BP/$\overline{UP}$ is low and the mid-scale transition defines Bipolar Offset when BP/$\overline{UP}$ is high. The Offset Calibration Range specification indicates the range of voltages applied to AIN that the CS5503 can accept and still calibrate offset accurately. Units in volts.

Input Span - The voltages applied to the AIN pin in system-calibration schemes define the CS5503's analog input range. The Input Span specification indicates the minimum and maximum input spans from zero-scale to full-scale in unipolar, or from positive full scale to negative full scale in bipolar, that the CS5503 can accept and still calibrate gain accurately. Units in volts.

Ordering Guide

Model Number	Linearity Error (Max)	Temperature Range	Package
CS5503-JP	0.0030%	0 to 70°C	20 Pin Plastic DIP
CS5503-KP	0.0015%	0 to 70°C	20 Pin Plastic DIP
CS5503-JS†	0.0030%	0 to 70°C	20 Lead SOIC
CS5503-KS†	0.0015%	0 to 70°C	20 Lead SOIC
CS5503-AD	0.0030%	-40 to +85°C	20 Pin Cerdip
CS5503-BD	0.0015%	-40 to +85°C	20 Pin Cerdip
CS5503-SD	0.0030%	-55 to +125°C	20 Pin Cerdip
CS5503-TD	0.0015%	-55 to +125°C	20 Pin Cerdip

† Contact the factory for availability of Engineering Samples. Expected availability of production volumes: 4Qtr 1989.

Note: Grades L, C, and U are expected to be available in 1990.

INDEX

Semiconductor Corporation

CS5505

Low-Cost, Four channel, 16 - bit A/D Converter

Features

- Offers superior performance to integrating A/D converters.
- Four channel pseudo- differential inputs
- On Chip Self-Calibration Circuitry
  Linearity Error: ±0.0015% FS Max
  16-Bit No Missing Codes (DNL ±1/8 LSB)
- Output data rates up to 60/second
- Flexible Serial Communications Port
  µC-Compatible Formats
  3-State Data and Clock Outputs
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 2mW
  10µW Sleep Mode for Portable Applications
- Available in 24 pin 0.3 in molded and hermetic DIP, and SOIC packages

General Description

The CS5505 is a low-cost CMOS A/D converter which is ideal for measuring low-frequency signals representing physical, chemical, and biological processes. The CS5505 utilizes charge-balance techniques to achieve true 16-bit accuracy with 20Hz word rates at very low cost.

The CS5505 continuously samples at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at a 20Hz rate. The user can randomly address any of the four pseudo-differential input channels and perform conversions on demand.

The on chip digital filter offers superior line rejection at 50 and 60Hz with the added advantage of spurious noise rejection at higher frequencies.

The CS5505 includes on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB.

The CS5505's serial port offers two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

ORDERING INFORMATION:
Contact Crystal Semiconductor

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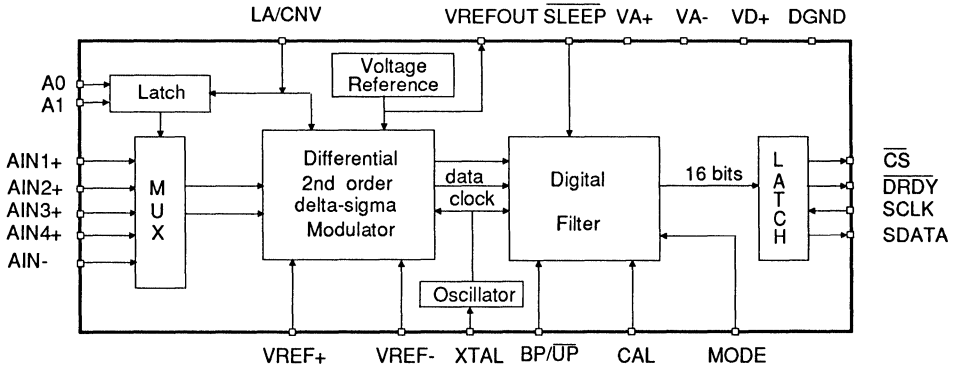


Preliminary Specification

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: 512 445-7581

•Notes•

Semiconductor Corporation

CS7820

High Speed 8-Bit A-to-D with Track and Hold

Features

- Completely Self-Contained
  - On-Chip Track and Hold
  - Microprocessor Interface
  - Internal Clock
  - Overrange Flag
- Fast Conversion: 1.36µs Max
- True 8-bit Accuracy over Temperature
  - No Trims Required
  - No Missing Codes
- Low Power Dissipation: 100mW Max
- Replaces ADC0820 and AD7820
- Single +5V Supply
- Improved Latch-up Resistance

General Description

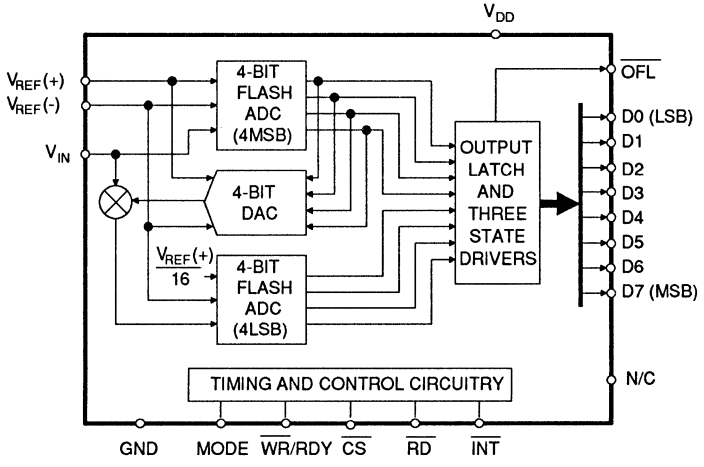
The CS7820 is a low-cost, easy to use, microprocessor compatible 8-bit analog-to-digital converter with on-chip track-and-hold function. Use of CMOS and half-flash techniques allow both high throughput rates (1.36µs max conversion time) and low power requirements (100mW max over the full Mil temperature range).

The input to the CS7820 is tracked and held by on-chip sampling circuitry, eliminating the need for an external track-and-hold amplifier for input signals slewing at less than 100mV/µs.

The CS7820 is designed to appear as a memory location or I/O port to a microprocessor without additional external interfacing logic. All of the data outputs use latched, three-state output buffers, allowing direct connection to a data bus or input port on a microprocessor system.

The CS7820 is pin compatible with the ADC0820 and AD7820.

ORDERING INFORMATION: Page 3-350



Preliminary Product Information This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

ANALOG CHARACTERISTICS

(V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V; RD-Mode; T_A = T_{MIN} to T_{MAX} unless otherwise stated.)

Parameter	CS7820-K,L min	CS7820-K,L typ	CS7820-K,L max	CS7820-B,C min	CS7820-B,C typ	CS7820-B,C max	CS7820-T,U min	CS7820-T,U typ	CS7820-T,U max	Units
Specified Temperature Range	0	to	+70	-40	to	+85	-55	to	+125	°C
Accuracy										
Resolution	8			8			8			Bits
Total Unadjusted Error -K/B/T			±1			±1			±1	LSB
(Note 1) -L/C/U			±1/2			±1/2			±1/2	LSB
No Missing Code Resolution	8			8			8			Bits
Reference Input										
Input Resistance	1.0		4.0	1.0		4.0	1.0		4.0	kΩ
$V_{REF}(+)$ Input Voltage Range	V_{REF} (-)		V_{DD}	V_{REF} (-)		V_{DD}	V_{REF} (-)		V_{DD}	V
$V_{REF}(-)$ Input Voltage Range	GND		V_{REF} (+)	GND		V_{REF} (+)	GND		V_{REF} (+)	V
Analog Input										
Voltage Range	GND-0.1		V_{DD}+0.1	GND-0.1		V_{DD}+0.1	GND-0.1		V_{DD}+0.1	V
Leakage Current (V_{IN} = 0V to 5V)			±3			±3			±3	uA
Capacitance (Note 2)		45			45			45		pF
Slew Rate, Tracking (Note 2)		0.2	0.1		0.2	0.1		0.2	0.1	V/us
Power Supply										
Supply Range for Specified Operation	4.75		5.25	4.75		5.25	4.75		5.25	V
Supply Current ($\overline{CS}$=$\overline{RD}$=0V)			15			20			20	mA
Power Dissipation		40			40			40		mW
Power Supply Sensitivity V_{DD}=5V±5%		±1/16	±1/4		±1/16	±1/4		±1/16	±1/4	LSB

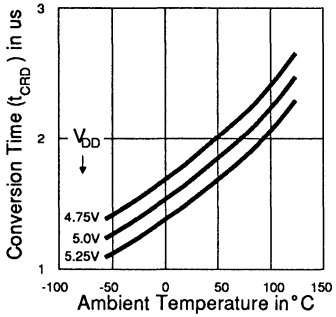
Notes: 1. Total unadjusted Error includes offset, full-scale and linearity errors.
2. Sample tested at 25°C to assure compliance.

Ordering Guide

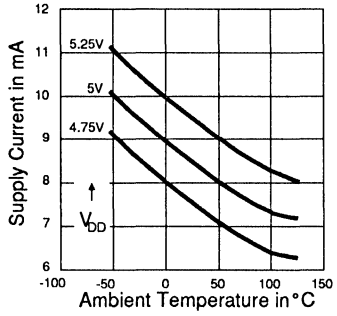
Model	Error	Temp Range	Package
CS7820-KP	± 1 LSB	0 to 70°C	20-Pin Plastic DIP
CS7820-LP	± 1/2 LSB	0 to 70°C	20-Pin Plastic DIP
CS7820-BD	± 1 LSB	-40 to 85°C	20-Pin CerDIP
CS7820-CD	± 1/2 LSB	-40 to 85°C	20-Pin CerDIP
CS7820-TD	± 1 LSB	-55 to 125°C	20-Pin CerDIP
CS7820-UD	± 1/2 LSB	-55 to 125°C	20-Pin CerDIP

Specifications are subject to change without notice.

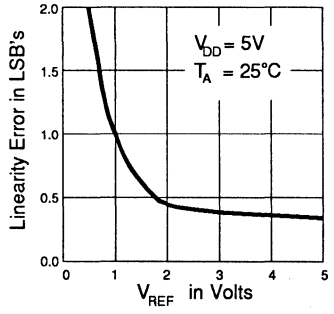
Typical Performance Characteristics



Conversion Time (RD Mode) vs. Temperature

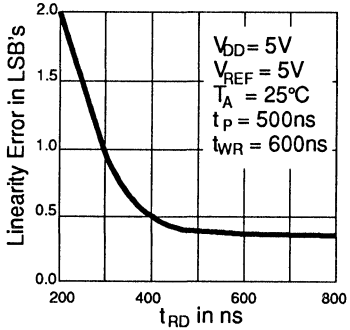


Power Supply Current vs. Temperature (not including reference ladder)

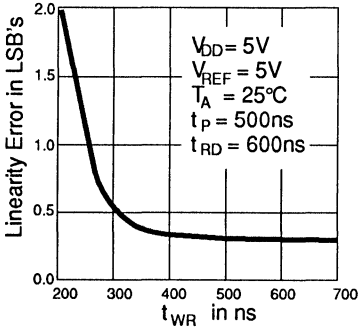


Accuracy vs. V_{REF} (V_{REF} = V_{REF} (+) - V_{REF} (-) and 1LSB = V_{REF} /256)

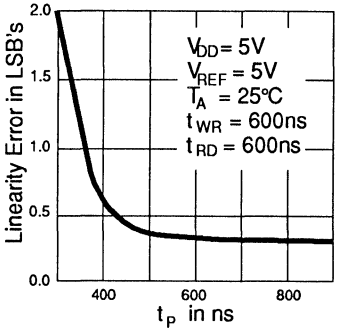
3



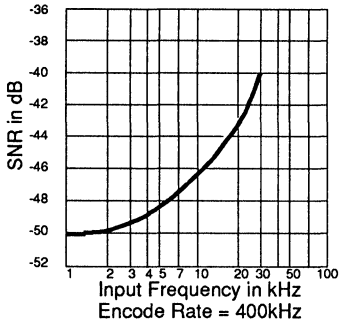
Accuracy vs. t_{RD}



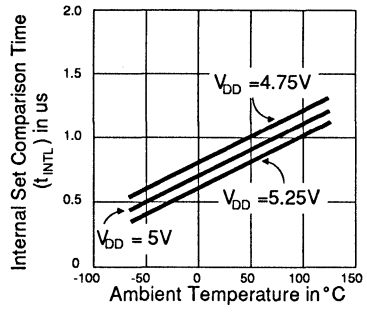
Accuracy vs. t_{WR}



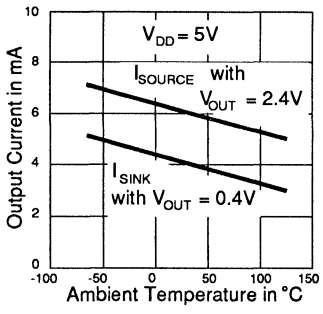
Accuracy vs. t_P



Signal-Noise Ratio vs. Input Frequency



Internal Time Delay (t_{INTL}) vs. Temperature

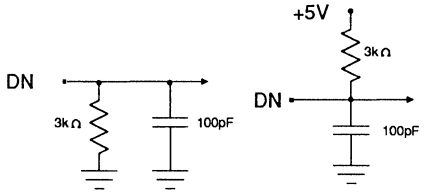


Output Current vs. Temperature

SWITCHING CHARACTERISTICS (V_{DD} = 5V; $V_{REF}(+)$ = 5V; $V_{REF}(-)$ = GND = 0V. (Note 6))

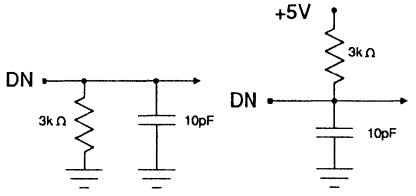
Parameter	Symbol	CS7820-K,L Min	CS7820-K,L Typ	CS7820-K,L Max	CS7820-B,C Min	CS7820-B,C Typ	CS7820-B,C Max	CS7820-T,U Min	CS7820-T,U Typ	CS7820-T,U Max	Units
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time T_A = 25°C	t_{CSS}	0			0			0			ns
$T_A = T_{MIN}$ to T_{MAX}		0			0			0			ns
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time T_A = 25°C	t_{CSH}	0			0			0			ns
$T_A = T_{MIN}$ to T_{MAX}		0			0			0			ns
$\overline{CS}$ to $\overline{RDY}$ Delay with T_A = 25°C	t_{RDY}			70			70			70	ns
a 2kΩ Pull-Up $T_A = T_{MIN}$ to T_{MAX}	(Note 3)			90			90			100	ns
Conversion Time, T_A = 25°C	t_{CRD}			1.6			1.6			1.6	us
RD Mode $T_A = T_{MIN}$ to T_{MAX}				2.0			2.0			2.5	us
Data Access Time, T_A = 25°C	t_{ACCO}		t_{CRD}+35			t_{CRD}+35			t_{CRD}+35		ns
RD Mode $T_A = T_{MIN}$ to T_{MAX}	(Note 4)		t_{CRD}+35			t_{CRD}+45			t_{CRD}+60		ns
$\overline{RD}$ to $\overline{INT}$ Delay, T_A = 25°C	t_{INTH}		125	175		125	175		125	175	ns
RD Mode $T_A = T_{MIN}$ to T_{MAX}	(Note 3)			225			225			225	ns
Data Hold Time T_A = 25°C	t_{DH}			60			60			60	ns
$T_A = T_{MIN}$ to T_{MAX}	(Note 5)			80			80			100	ns
Delay Time between T_A = 25°C	t_P	500			500			500			ns
Conversions $T_A = T_{MIN}$ to T_{MAX}		600			600			600			ns
Write Pulse Width T_A = 25°C	t_{WR}	0.6		50	0.6		50	0.6		50	us
$T_A = T_{MIN}$ to T_{MAX}		0.6		50	0.6		50	0.6		50	us
Conversion Time, T_A = 25°C	t_{CWR-RD}			1360			1360			1360	ns
WR/RD Mode $T_A = T_{MIN}$ to T_{MAX}				1525			1525			1550	ns
Delay Time between $\overline{WR}$ T_A = 25°C	t_{RD}	600			600			600			ns
and $\overline{RD}$ Pulses $T_A = T_{MIN}$ to T_{MAX}		700			700			700			ns
Data Access Time, WR-RD T_A = 25°C	t_{ACC1}			160			160			160	ns
Mode (Fig. 6) $T_A = T_{MIN}$ to T_{MAX}	(Note 4)			225			225			250	ns
$\overline{RD}$ to $\overline{INT}$ Delay T_A = 25°C	t_{RI}			140			140			140	ns
$T_A = T_{MIN}$ to T_{MAX}				200			200			225	ns
$\overline{WR}$ to $\overline{INT}$ Delay T_A = 25°C	t_{INTL}		700	1000		700	1000		700	1000	ns
$T_A = T_{MIN}$ to T_{MAX}	(Note 3)			1400			1400			1700	ns
Data Access Time, WR-RD T_A = 25°C	t_{ACC2}			70			70			70	ns
Mode (Fig. 5) $T_A = T_{MIN}$ to T_{MAX}	(Note 4)			90			90			110	ns
$\overline{WR}$ to $\overline{INT}$ Delay, Stand- T_A = 25°C	t_{IHWR}			100			100			100	ns
Alone Operation $T_A = T_{MIN}$ to T_{MAX}	(Note 3)			130			130			150	ns
Data Access Time T_A = 25°C	t_{ID}			50			50			50	ns
after $\overline{INT}$, Stand- $T_A = T_{MIN}$ to T_{MAX}				65			65			75	ns
Alone Operation											

Notes: 3. CL = 50pF.
4. Measured with the load shown in Fig. 1, and defined as the time for an output to cross 0.8V or 2.4V.
5. Measured with the load shown in Fig. 2, and defined as the time required for the data lines (D0 - D7) to change 0.5V.
6. Sample tested to ensure compliance.



a. High-Z to V_{OH} b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



a. V_{OH} to High-Z b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; $V_{DD} = 5V \pm 5\%$; $V_{REF}(+) = 5V$; $V_{REF}(-) = GND = 0V$; All measurements below are performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
Logic Inputs (CS, WR, RD)					
High-Level Input Voltage	V_{IH}	2.4			V
Low-Level Input Voltage	V_{IL}			0.8	V
High-Level Input Current ($\overline{CS}$, $\overline{RD}$)	I_{IH}			1	uA
High-Level Input Current (WR)	I_{IH}			3	uA
Low-Level Input Current	I_{IL}			-1	uA
Input Capacitance (Note 7)			5	8	pF
Logic Inputs (MODE)					
High-Level Input Voltage	V_{IH}	3.5			V
Low-Level Input Voltage	V_{IL}			1.5	V
High-Level Input Current	I_{IH}			200	uA
Low-Level Input Current	I_{IL}			-1	uA
Input Capacitance (Note 7)			5	8	pF
Logic Outputs (D0-D7, $\overline{OFL}$, $\overline{INT}$)					
High-Level Output Voltage (@ -360uA)	V_{OH}	4.0			V
Low-Level Output Voltage (@ 1.6mA)	V_{OL}			0.4	V
Output Current (Leakage on D0-D7)	I_{out}			±3	uA
Output Capacitance (Note 7)			5	8	pF

Note: 7. Sample tested at 25°C to ensure compliance.

ABSOLUTE MAXIMUM RATINGS (GND = 0V; All voltages with respect to ground.)

Parameter	Symbol	Min	Max	Units
Power Supply Voltage	V_{DD}	−0.3	10.0	V
Input Current, Any Pin Except Supply	I_{in}	-	±10	mA
Voltage, Any Pin Except Supply	V_{in}	-0.3	V_{DD} + 0.3	V
Ambient Operating Temperature	T_A	-55	125	°C
Storage Temperature	T_{STG}	-65	150	°C
Power Dissipation (Any Package) to 75 °C Derate above 75 °C			500 6	mW mW/ °C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

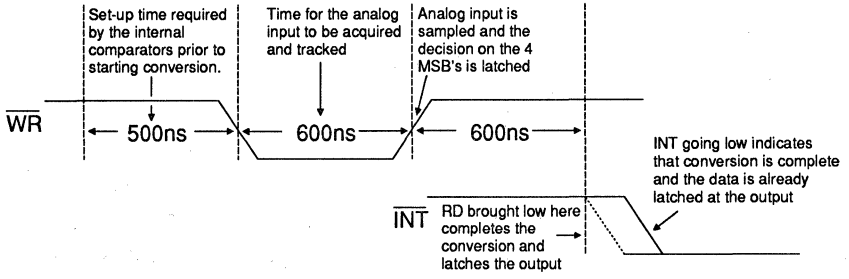


Figure 3. Basic Operation (WR-RD Mode)

GENERAL DESCRIPTION

The CS7820 generates an accurate 8-bit digital output representation of the analog input signal by making use of two 4-bit flash converters, and implementing a two-step conversion architecture. This approach achieves both high speed conversions and 8-bit accuracy without external user trims. The CS7820 also has an inherent track-and-hold input stage, which eliminates the need for an external track-and-hold in most applications.

The two-step flash architecture first converts the 4 MSB's (most significant bits.) These 4-bits of data drive an on-board DAC, whose output is subtracted from the analog input. The remainder is then fed into the second flash converter to generate the 4 LSB's (least significant bits.) The digital side of the CS7820 is designed for ease of operation and flexibility in use with microprocessors or in stand-alone operation.

BASIC OPERATION

The basic operating timing for the CS7820 in the WR-RD Mode is shown in Figure 3. A conversion is initiated by a falling edge on $\overline{WR}$, which causes the input stage to start acquiring and tracking the analog input. The MSB flash converter comparators track the input as long as $\overline{WR}$ stays low, with a minimum of 600 ns required to acquire the input signal. When $\overline{WR}$ returns high, the 4 bits of the MSB flash converter output are latched into the output buffers, and the LSB flash converter begins. $\overline{INT}$ goes low about 700 ns later, indicating that the 4 LSB's of data are latched into the output buffer, and that the full conversion has been completed. The output data word is then accessed by bringing $\overline{RD}$ low.

To control the conversion time externally, $\overline{RD}$ can be brought low as soon as 600 ns after $\overline{WR}$ goes high. This latches the 4 LSB's and outputs the data word on D0-D7. A minimum setup time of 500 ns is required after $\overline{INT}$ goes low before initiating another conversion (by $\overline{WR}$ going low.)

DIGITAL INTERFACE

The input level at the MODE pin determines the basic interface mode of the CS7820. A Logic Low input puts the converter in the RD mode,

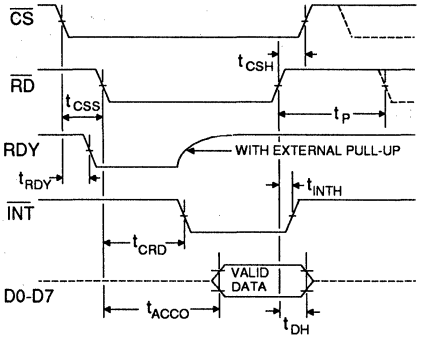


Figure 4. RD Mode

while a Logic High input puts the converter in the WR-RD mode.

RD Mode

The RD mode allows the user to control conversion and data access with the $\overline{RD}$ input (see Figure 4.) A conversion is initiated by bringing $\overline{RD}$ low, and it is kept low until output data appears. This mode is useful for microprocessors that can be put into a WAIT state, since the processor can use a single READ instruction to initiate conversion, wait, and read the output data.

In RD mode, pin 6 ($\overline{WR}$/RDY) provides a status output, RDY, which can be used to drive the WAIT or READY input of a microprocessor. There is no internal pull-up on RDY (it is an open drain output). RDY goes low after the falling edge of $\overline{CS}$ and then goes high impedance at the end of a conversion. An $\overline{INT}$ output pin is also available, which goes low at the end of a conversion and returns high on the rising edge of either $\overline{RD}$ or $\overline{CS}$.

WR-RD Mode

The WR-RD mode provides the fastest conversion time by allowing the user full control over the various stages in the conversion process. In this mode, pin 6 ($\overline{WR}$/RDY) is used as a WRITE input to the converter. With $\overline{CS}$ low, a falling edge on $\overline{WR}$ initiates a conversion. Various options are available for reading the output data.

Using internal delay. In this mode, the $\overline{INT}$ output is used to signal the processor to read the data (Figure 5.) $\overline{INT}$ goes low about 700 ns after the rising edge of $\overline{WR}$, indicating that the conversion has been completed and the data word is available in the output latch. To access D0-D7, $\overline{RD}$ is brought low with $\overline{CS}$ low. The rising edge of either $\overline{RD}$ or $\overline{CS}$ resets $\overline{INT}$.

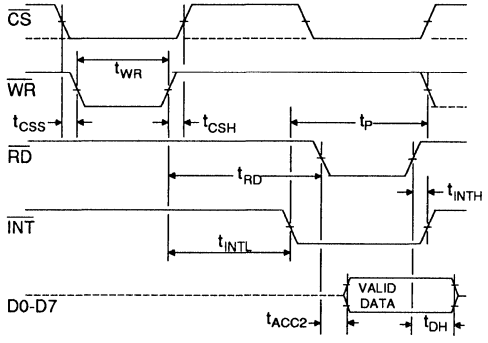


Figure 5. WR-RD Mode ($t_{RD} > t_{INTL}$)

Using external RD timing. In this mode, the $\overline{RD}$ input can be used to externally minimize conversion time (Figure 6.) This mode is useful in applications with critical timing, since the internal delay on $\overline{INT}$ can vary with supplies and temperature. (See the typical performance curves.) Bringing $\overline{RD}$ low before $\overline{INT}$ goes low completes the conversion and enables the output latch. This can be done as soon as 600 ns after the rising edge of $\overline{WR}$.

Pipelined operation. By tying $\overline{WR}$ and $\overline{RD}$ together, the CS7820 can be pipelined. With $\overline{CS}$ low, bringing $\overline{WR}$ and $\overline{RD}$ low together both initiates a new conversion and enables the output latch so that the user can read the results of the previous conversion.

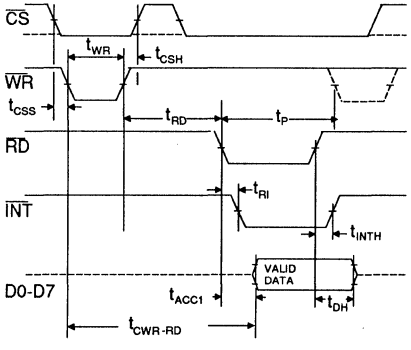


Figure 6. WR-RD Mode ($t_{RD} < t_{INTL}$)

Stand-Alone operation. The CS7820 can also be used in stand-alone operation, by tying $\overline{CS}$ and $\overline{RD}$ to ground. A conversion is initiated by bringing $\overline{WR}$ low, and the output data will be valid approximately 700 ns after the rising edge of $\overline{WR}$. (Figure 7.)

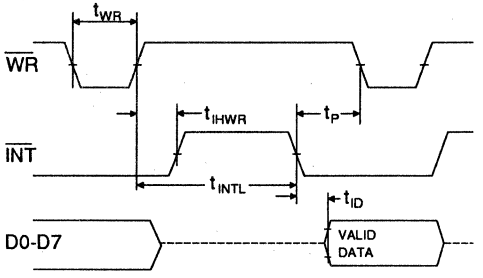


Figure 7. WR-RD Mode
Stand-Alone Operation ($\overline{CS}$ = $\overline{RD}$ = 0V)

ANALOG OPERATING INFORMATION

Reference and Input

The two reference inputs to the CS7820 define the zero to fullscale range of the converter. These are fully differential inputs. The negative reference input defines the analog input level that will generate an output data word of all zeroes, while the positive reference input defines the analog input level that will generate an output data word of all ones.

The analog input can span the range of the reference input range. Thus the sensitivity of the converter can be increased by reducing the span of the reference inputs (and making the size of each LSB smaller). Use of the reference structure also allows the analog input span to be offset from zero, as shown in Figure 12.

Although the analog input is not differential, the reference flexibility facilitates use in most measurement applications. The input and reference architecture also facilitates ratiometric applications.

Inherent Track-and-Hold

The equivalent input circuit for the CS7820 is shown in Figure 8a. The inherent sampling structure means that a wide variety of high speed input signals can be measured without requiring an external track-and-hold. Typically, input signals with slew rates below 200 mV/µs can be converted with full 8-bit accuracy. Faster input signals will start to degrade accuracy, because of input time constants and charge injection through the comparator input switches, but the degradation will occur less quickly than on traditional successive approximation converters.

The CS7820 tracks the analog input signal while $\overline{WR}$ is low, and holds the input signal approximately 100 ns after the rising edge of $\overline{WR}$. This is effectively the aperture delay of the inherent track-and-hold.

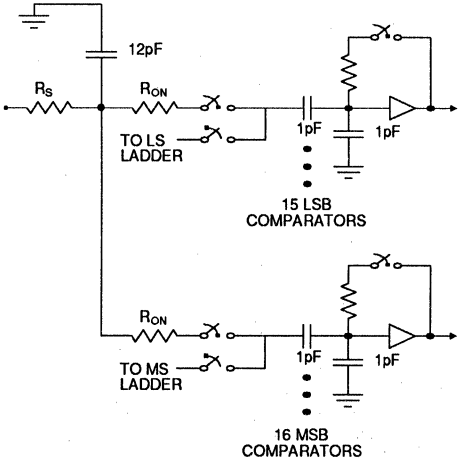


Figure 8a. CS7820 Equivalent Input Circuit

Input Current

The sampling input of the CS7820 provides a varying load for the input signal depending on the stage of the conversion cycle. (Refer again to Figure 8a.) When conversion starts ($\overline{WR}$ is brought low) the analog input is connected to the MSB and LSB flash converter inputs, effectively seeing thirty-one 1 pF capacitors. These capacitors need to be charged during the acquisition phase ($\overline{WR}$ held low) through the resistance of the internal analog switches, which range from about 2 kΩ to 5 kΩ. Stray capacitance adds about 12 pF to the input load. For large source resistances, Figure 8b approximates the load RC network. As the source impedance increases, the capacitors take longer to charge.

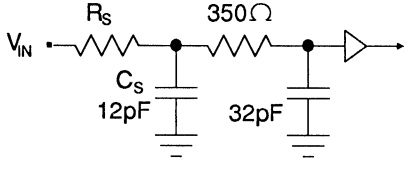


Figure 8b. CS7820 RC Network Model

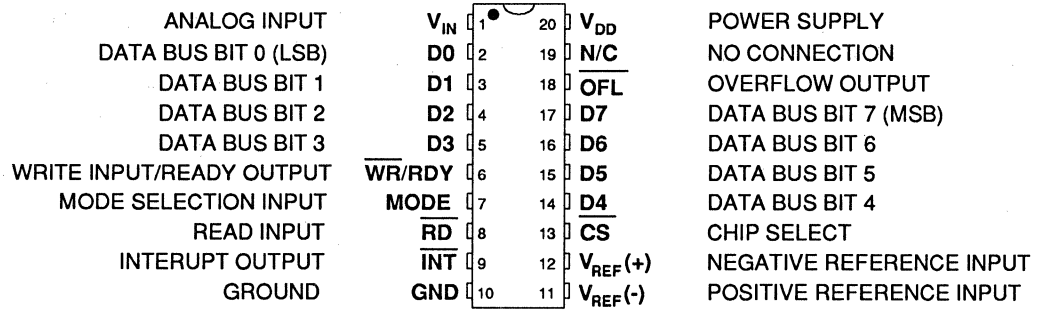
Input resistances up to 1 kΩ can be used without settling problems with the typical 45 pF input capacitance. For larger source resistances, the width of the $\overline{WR}$ pulse needs to be increased. This means that the RD mode may be inappropriate for applications with higher source resistances, since the acquisition time is internally set. Alternatively, an input buffer could be used to drive the analog input of the CS7820.

Input Filtering

Because the sampling input structure has a minimum 600 ns charging time while $\overline{WR}$ is held low, transients on the analog input will not normally degrade the converter's performance. It is therefore not necessary to filter the input to the CS7820 in most applications.

3

PIN DESCRIPTIONS



Analog and Reference Inputs

VIN -Analog Input, Pin 1

VREF(-) -Negative Reference Input, Pin 11

Lower limit of the reference span. Sets the voltage level for an output code of all zeroes.

VREF(+) -Positive Reference Input, Pin 12

Upper limit of the reference span. Sets the voltage level for an output code of all ones.

Digital Inputs and Outputs

D0 through D7 -Data Bus Outputs, Pins 2 thru 5 and 14 thru 17

Tri-state output pins. D0 (the LSB) is on Pin 2, ascending to D7 (the MSB) on pin 17.

$\overline{\text{WR/RDY}}$ -Write Input/ Ready Output, Pin 6

Depending on the mode of operation, acts as either an input pin to initiate conversions (WR-RD mode) or as an output status pin to indicate that the conversion is complete and the output data is ready (RD mode).

MODE -Mode Selection Input, Pin 7

Determines whether the device operates in the WR-RD mode or the RD mode. It has an internal pull-down circuit with a 50µA current source, so the default operating condition is the RD mode.

$\overline{\text{RD}}$ -Read Input, Pin 8

RD must be low to access data.

$\overline{\text{INT}}$ -Interrupt Output, Pin 9

INT going low indicates the conversion is complete.

$\overline{CS}$ - Chip Select Input, Pin 13

CS must be low for the device to accept $\overline{RD}$ or $\overline{WR}$ inputs.

$\overline{OFL}$ - Overflow Output, Pin 18

If the analog input is greater than $V_{REF}(+)$ -1/2 LSB, $\overline{OFL}$ will be low at the end of the conversion. This can be used to cascade devices for increased resolution. This output pin is not tri-state.

Power Supply and Ground

GND -Ground, Pin 10

V_{DD} -Power Supply, Pin 20

3

APPLICATIONS INFORMATION

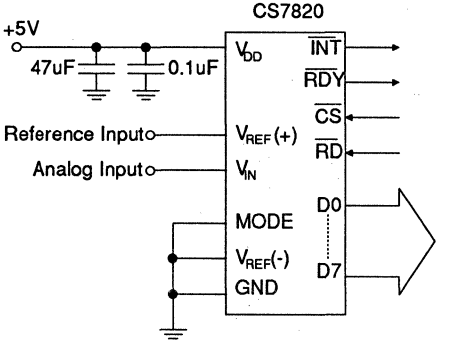


Figure 9. RD Mode, 8-Bit Resolution

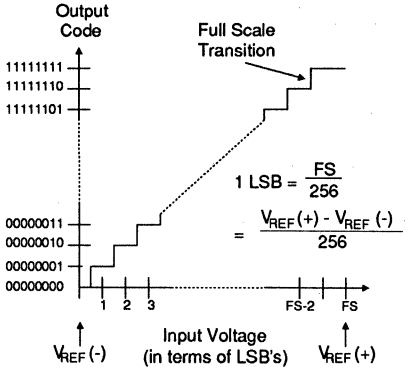


Figure 10. CS7820 Transfer Function

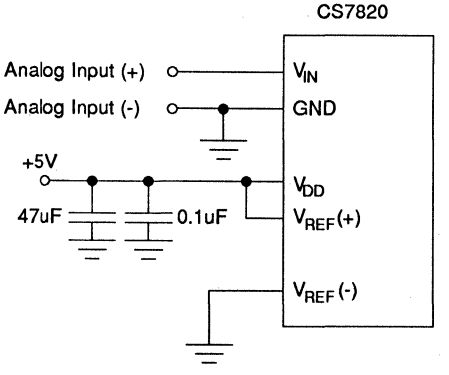


Figure 11. Using the Supply as Reference

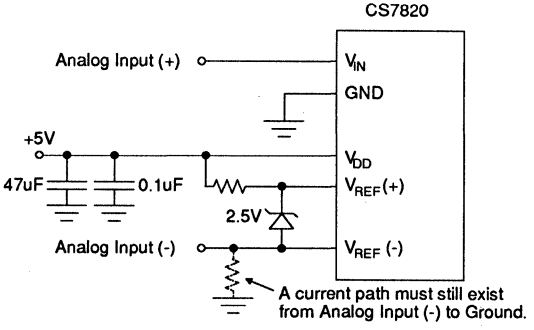


Figure 12. Input Not Referenced to Ground

INTRODUCTION

Crystal offers the digital audio industry a quantum improvement in digital-to-analog system integration, along with cost-effective performance enhancement. The CS4328 is industry's first complete stereo digital-to-analog output system. This 18-bit stereo D/A converter uses Crystal's well established oversampling A/D converter techniques.

The CS4328 includes the major system elements of 8X interpolation filter, 64X oversampling 18-bit D/A converter and a 95 dB dynamic range analog anti-imaging filter, all in one packaged, tested, solution. As with our A/D converters, the device features patented delta sigma architectures to maintain excellent distortion performance, even at low signal levels. The output anti-imaging filters are the first to be based on a mixed linear/switched capacitor architecture. This allows the benefit of bandwidth scaling proportionally to the system master clock, while retaining the low noise performance of linear filters. The CS4328 is therefore adjustable for both audio and voice band applications. The flexible digital interface mates with CD player circuitry, DAT recorders, DSP's or winchester disk drives.

CONTENTS

Semiconductor Corporation

CS4328

18-Bit, Stereo D/A Converter for Digital Audio

Features

- Complete Stereo DAC System
  - 8x Interpolation Filter
  - Delta-Sigma DAC
  - Analog Post Filter
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 95 dB Dynamic Range over the Audio Band
- 0.001 dB Passband Ripple
- Completely Filtered Line-Level Outputs
  - Linear Phase Filtering
  - Zero Phase Error Between Channels
  - No External Components Needed
- 16 or 18 bit Input Words
- Supports Multiple Input Formats

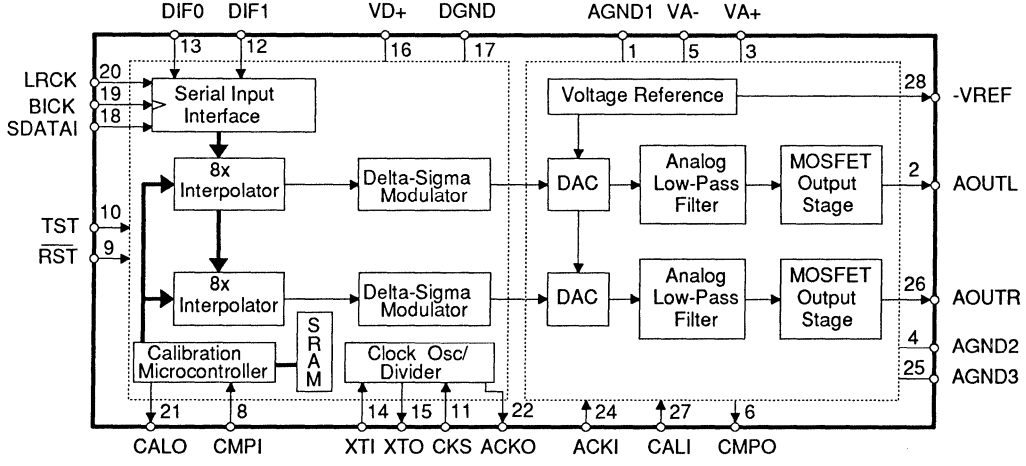
General Description

The CS4328 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4328 includes an 8× digital interpolation filter followed by a 64× oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultralinear analog low-pass filter. The total D/A system provides a linear phase response.

The CS4328 also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

To support various audio environments a clock select pin chooses between 256- and 384-times the input word rate for the master clock.

ORDERING INFORMATION:
Contact Crystal Semiconductor.



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

•Notes•

INTRODUCTION

As the industry's first monlithic 4-channel track-and-hold amplifier, the CS31412 frees-up board space and reduces system costs normally associated with sampling and multiplexing analog signals for conversion. The CS31412 takes a snapshot of four single-ended or two differential signals and stores the analog values in on-chip hold capacitors. An on-chip digital correction scheme calibrates all dc and dynamic errors, including hold pedestals, to less than 4 mV. Channel selection and calibration can be placed under software control using the microprocessor interface. Since the CS31412 can calibrate at any time or temperature, it ensures accuracy throughout its operating life.

The CS31412's fast 800 ns acquisition time and 12-bit accuracy make it ideal for processing high-frequency signals. In applications where fast sampling is not critical, the CS31412's 0.007 μV/ μs droop in the hold mode allows slower conversion of the channels without loss of accuracy. The CS31412 dissipates only 250 mW of power.

A complete single-channel track-and-hold, the CS3112, is also available. On-chip hold capacitors and calibration logic simplify use, and keep all dc and dynamic errors, including pedestal error, below 3.0 mV. This accuracy is ensured over time and temperature by easy user control of the calibration circuitry.

USER'S GUIDE

Device:	CS3112	CS31412
# of Track & Holds	1	4
Acquisition Time	800 ns	800 ns
Offset Voltage	1.8 mV	2.8 mV
Power Consumption	130 mW	250 mW
Package	14-Pin DIP	18-Pin DIP

CONTENTS

Semiconductor Corporation

CS3112

High Speed Precision Track and Hold

Features

- Completely Self-Contained On-Chip Hold Capacitor Microprocessor Interface
- Fast Acquisition: 800ns to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset, Including Hold Pedestal: 1.8 mV
- Low Droop Rate: 0.001uV/us
- Self-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 130 mW

General Description

The CS3112 is a high speed track and hold with 12-bit linearity. It is completely self-contained, including hold capacitor, output buffer, and calibration circuitry.

Aperture jitter of 100ps and acquisition time of 800ns to 0.01% provide excellent dynamic performance. An on-chip hold capacitor limits droop to 0.001 uV/us, and first order leakage compensation minimizes droop over the full operating temperature range.

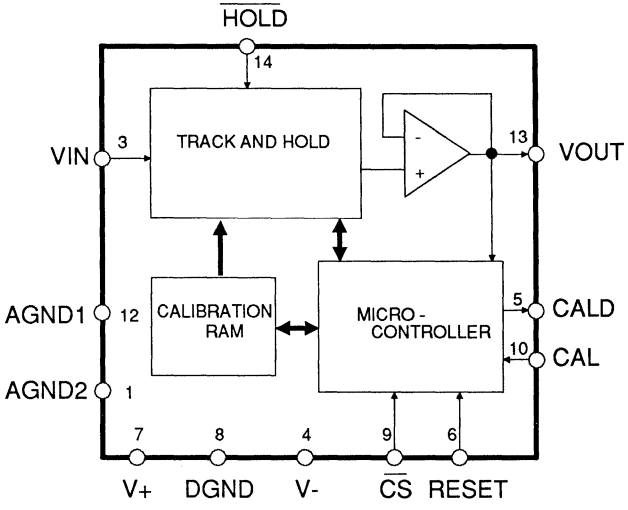
Advanced CMOS fabrication insures low power consumption and increased reliability.

The CS3112 can be controlled and monitored through its microprocessor interface, or can operate independently.

ORDERING INFORMATION:

Model	Acquisition Time	Temp. Range	Package
CS3112-KD2	2.0 µs	0 to 70 °C	14-pin CerDIP
CS3112-KD1	1.0 µs	0 to 70 °C	14-pin CerDIP
CS3112-BD1	1.0 µs	-40 to +85 °C	14-pin CerDIP
CS3112-TD1	1.0 µs	-55 to +125 °C	14-pin CerDIP

5



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25°C, V+ = +5.0V, V- = -5.0V, R_L = 10KΩ, C_L = 50pF, Analog Source Impedance = 40Ω, unless otherwise specified)

Parameter*	CS3112-K min	CS3112-K typ	CS3112-K max	CS3112-B min	CS3112-B typ	CS3112-B max	CS3112-T min	CS3112-T typ	CS3112-T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Accuracy										
Total Offset (Note 1) 25°C		−1.8	± 3.0		−1.8	± 3.0		−1.8	± 3.0	mV
T_{min} to T_{max}			± 3.5			± 3.5			± 3.5	mV
Offset Drift (Note 2) T_{min} to T_{max}		± 0.020			± 0.025			± 0.030		mV/°C
Tracking Offset			± 55			± 55			± 55	mV
Nonlinearity 25°C			± 0.7			± 0.7			± 0.7	mV
(Note 3) T_{min} to T_{max}		± 0.5			± 0.5			± 0.5		mV
Gain Error T_{min} to T_{max}		± 0.01			± 0.01			± 0.01		% FS
Dynamic Characteristics										
Acquisition Time -1		0.8	1.0		0.8	1.0		0.8	1.0	us
(6V step to 0.01%) -2		1.6	2.0							us
-1		0.6			0.6			0.6		us
(6V step to 0.1%) -2		1.2								us
Track to Hold Settling to 0.01%		0.5	0.8		0.5	0.8		0.5	0.8	us
Aperture Time		20			20			20		ns
Aperture Time Matching (Note 4)		2			2			2		ns
Aperture Jitter		100			100			100		ps
Droop Rate 25°C		± 0.001	± 0.1		± 0.001	± 0.1		± 0.001	± 0.1	uV/us
T_{min} to T_{max}			± 0.6			± 1.0			± 5.0	uV/us
Analog Input/Output										
Large Signal Bandwidth (6V p-p Input)		2.0			2.0			2.0		MHz
Small Signal Gain Bandwidth (60mV p-p Input)		2.5			2.5			2.5		MHz
Input Impedance (dc)		100			100			100		MΩ
Input Capacitance		5			5			5		pF
Input Bias Current		100			100			100		pA
Output Impedance at dc (Note 3)		0.1			0.1			0.1		Ω
Output Slew Rate		10			10			10		V/us
Noise (Note 5) Track Mode		50			50			50		uV_{rms}
Hold Mode		33			33			33		uV_{rms}
Power Supplies										
Supply Currents Positive		13	20		13	20		13	20	mA
Negative		−13	−20		−13	−20		−13	20	mA
Power Supply Rejection Ratio										
Positive (Note 6)		75			75			75		dB
Negative (Note 7)		60			60			60		dB

*Refer to Error Definitions at the end of this data sheet.

Specifications are subject to change without notice.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 8).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	V+	4.5	5.0	5.5	V
Negative	V-	- 4.5	−5.0	−5.5	V
Analog Input Voltage:	V_{IN}	- 3.0	-	3.0	V

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

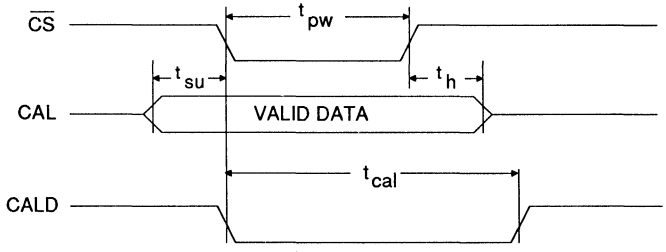
All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	1.7	-	V
Low-Level Input Voltage	V_{IL}	-	1.6	0.8	V
High-Level Output Voltage (Note 9)	V_{OH}	(V+) - 1.0V	-	-	V
Low-Level Output Voltage, Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

Parameter	Symbol	Min	Typ	Max	Units
CAL to $\overline{CS}$ Setup Time	t_{su}	20	5	-	ns
$\overline{CS}$ to CAL Hold Time	t_h	20	5	-	ns
$\overline{CS}$ Pulse Width	t_{pw}	100	50	-	ns
$\overline{CS}$ Low and CAL High to CALD High	t_{cal}	-	500	-	ms

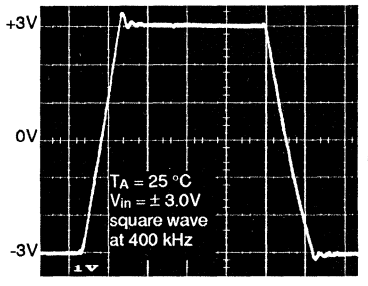
Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Applies over specified temperature range without recalibration since calibration at 25°C.
3. Applies over the input voltage range of -3.0V to +3.0V.
4. Part to part.
5. Total noise from dc to 1MHz.
6. With 300 mV_{p-p}, 1kHz ripple applied to V+.
7. With 300 mV_{p-p}, 1 kHz ripple applied to V-.
8. All voltages with respect to ground.
9. I_{out} = -100µA. This specification guarantees TTL compatability (VOH = +2.4V @ I_{out} = -40µA).



CS3112 Timing Diagram

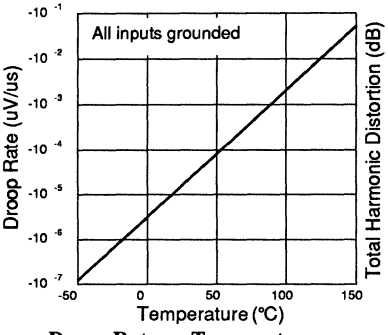
TYPICAL PERFORMANCE CHARACTERISTICS

(V+ = +5.0V, V- = -5.0V)

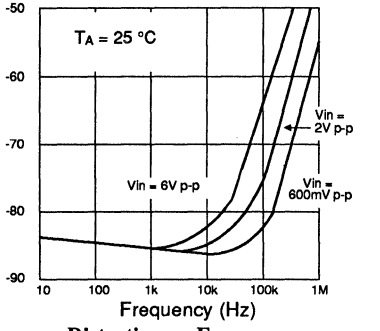


500 ns/div.

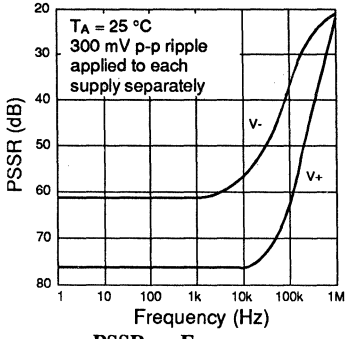
Full Scale Acquisition



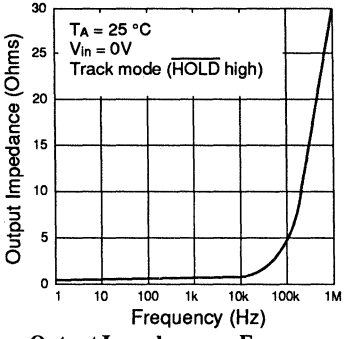
Droop Rate vs. Temperature



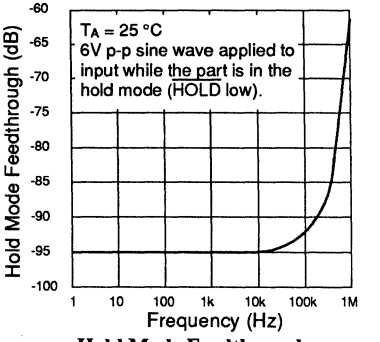
Distortion vs. Frequency



PSSR vs. Frequency



Output Impedance vs. Frequency



Hold Mode Feedthrough vs. Frequency

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	V+	−0.3	6.0	V
Negative	V-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 10)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	V- - 0.3	V+ + 0.3	V
Digital Input Voltage	V_{IND}	-0.3	V+ + 0.3	V
Ambient Operating Temperature	T_A	-55	125	°C
Storage Temperature	T_{STG}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 10. Transient currents of up to 100mA will not cause SCR latch-up. Maximum power supply pin current is ±100 mA.

GENERAL DESCRIPTION

The CS3112 consists of a complete track-and-hold amplifier with on-chip hold capacitor, an output buffer, and calibration circuitry. Use of an on-chip buffer isolates the track-and-hold amplifier from load conditions for optimal performance, and the calibration circuitry nulls out error sources. The CS3112 requires no external components or manual trims of any kind to achieve 12-bit performance.

The CS3112 can be controlled through its on-board microprocessor interface, or can be operated independently. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output.

Calibration

In the calibration mode, an internal microcontroller and special nulling circuitry reduce all errors at the VOUT pin. The controller disconnects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. This voltage is captured on the internal hold capacitor, and a DAC is adjusted to remove any error. Thus, all internal errors, including dc offset and dynamic errors due to charge injection (hold pedestal), are trimmed. During tracking, there may be up to ±55mV of offset.

At power-up, the user must calibrate the device. Calibration is achieved by bringing the CAL input high with $\overline{CS}$ low. (In the stand-alone mode, $\overline{CS}$ is grounded, so only the CAL pin needs to be pulsed.) Calibration can be similarly initiated during operation at any time, thus insuring accuracy under any conditions.

During the calibration cycle (which takes about 500ms to complete) the CALD pin remains low. During this period, any load on VOUT must remain constant; otherwise, errors could be introduced which might affect accuracy. If a new calibration is initiated before the current calibration is finished, the CS3112 will complete the current calibration before initiating the new one. CALD will go high when calibration is finished.

Digital Interface

The CS3112 includes a digital interface designed for maximum flexibility. In a microprocessor-controlled application, the $\overline{CS}$ control input is usually derived from a decoded address as well as write and strobe signals from the control bus (see Figure 1a). Calibration initiation thereby involves writing to the CS3112's address using a data bit to control CAL. For microprocessor-independent operation, $\overline{CS}$ is tied low and the digital inputs are controlled by externally-latched signals (see Figure 1b).

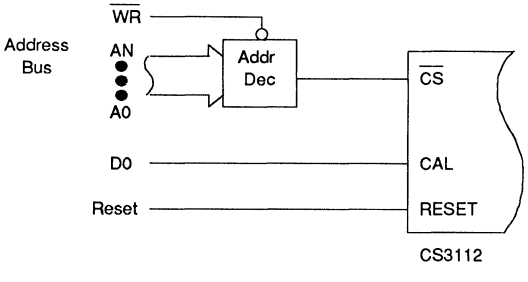


Figure 1a. CPU-Control

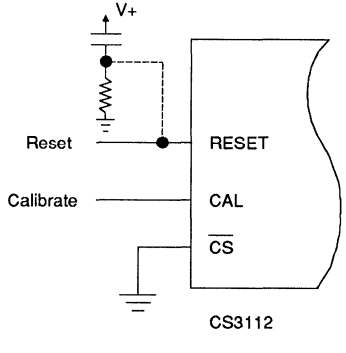


Figure 1b. Independent Control

The CS3112's CALD output can be used to generate an interrupt indicating that calibration has been completed. Alternatively, calibration status can be polled in software by connecting CALD to the data bus via a three-state buffer.

Reset

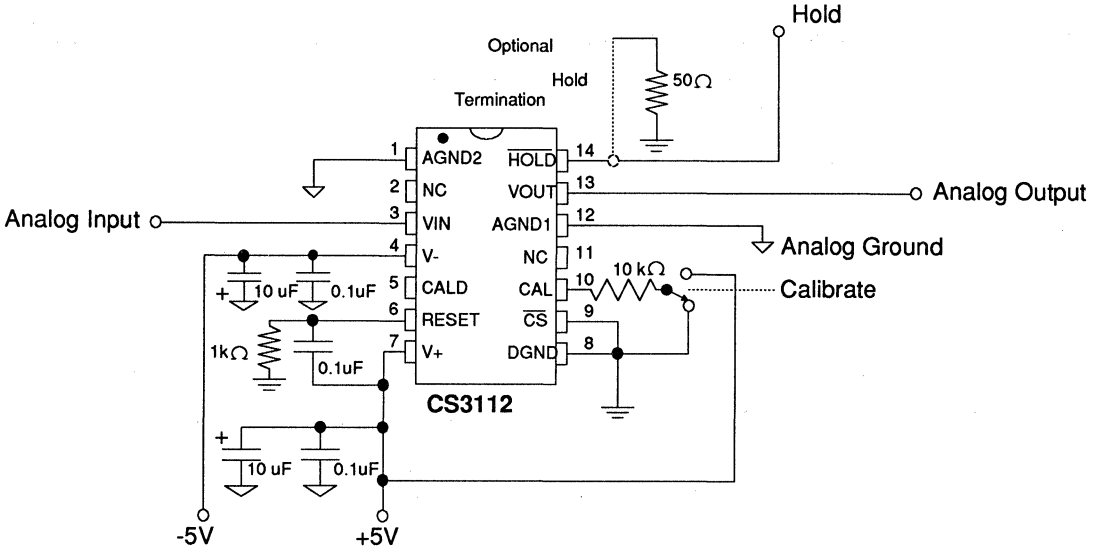
The CS3112 must be reset after power up to ensure correct operation. The CS3112 is reset when the RESET pin is high for at least 1µs. An RC network attached to the RESET pin will reset the part (See Figure 1b).

Power Supplies and Input Connections

The CS3112 uses the analog ground voltage (AGND1) only as a reference voltage. No signal or dc power currents flow through the AGND1 connection, and it is completely independent of DGND. Both the analog input and output are referenced to to the AGND1 pin internally, and this pin needs to be at the same potential as the entire system's analog ground plane to minimize offset errors induced by noise between the AGND1 pin and the system analog ground.

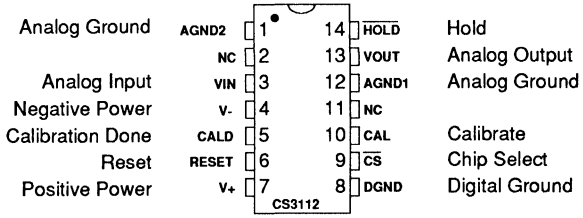
Decoupling should be performed between the V+, V- pins and AGND1 using 0.1µF ceramic capacitors. If significant low frequency noise is present on the supplies, 10µF tantalum capacitors are recommended in parallel with the 0.1µF capacitors. *The decoupling capacitors should be placed as close to the CS3112's power supply pins as possible.*

The signal source impedances which drive the input of the CS3112 should be minimized as much as possible. Low source impedance reduces the sensitivity of the input pin to picking up capacitively-coupled energy from logic level transitions, such as $\overline{\text{HOLD}}$ going low.



Simple Test Connections - Independent Operation

PIN DESCRIPTION



Analog Input and Output

VIN - Analog Input, PIN 3

Analog input to the track-and-hold amplifier.

VOUT - Analog Output , PIN 13

Buffered output from the track-and-hold.

Power Supplies

V+ - Positive Power, PIN 7

Most positive supply voltage. Nominally +5 volts.

V- - Negative Power, PIN 4

Most negative supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 8

Digital ground.

AGND1, AGND2 - Analog Ground, PIN 12, PIN 1

Analog ground reference.

Digital Inputs and Outputs

$\overline{\text{HOLD}}$ - Hold, PIN 14

A falling transition on this pin switches the track-and-hold amplifier to the hold mode. When brought high, the track-and-hold is switched to the track mode, and acquires and then tracks the input signal.

CAL - Calibrate, PIN 10

When taken high with $\overline{\text{CS}}$ low, initiates a full internal calibration.

CALD - Calibration Done, PIN 5

Indicates calibration status. If CALD is high the device has finished calibration. If CALD is low, the device is calibrating.

CS - Chip Select, PIN 9

Enables the CAL digital inputs.

RESET - Reset, PIN 6

The CS3112 must be reset after power up to ensure correct operation. Reset occurs when RESET is high.

NC - No Connect, PINS 2,11

No connection should be made to these pins.

ERROR DEFINITIONS

Total Offset

The difference between the analog input voltage and the voltage at the output pin after thehold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

Nonlinearity

The deviation from a straight line on the plot of output vs input. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

Gain Error

Calculated as the difference between the errors resulting from a -3V and a +3V dc input signal, relative to a 6V input range. Units in percent of full scale.

Acquisition Time

The time required after the negation of the hold command ($\overline{\text{HOLD}}$ high) for the track-and-hold amplifier to reach its final value to within a specified error band (±0.01% or ±0.1%). This determines the minimum time allowed before reassertion of the hold command. Units in microseconds.

Track-to-Hold Settling

The time required after the hold command is given for the output buffer amplifier to reach its final value to within a specified error band (±0.01%). Includes switch delay (aperture) time. Units in microseconds.

Aperture Time

The delay after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Droop Rate

The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

Large Signal Bandwidth

The frequency at which the output amplitude is 3dB below the input amplitude while tracking a full scale 6V p-p sine wave. Units in megahertz.

Small Signal Gain Bandwidth

The frequency at which the output amplitude is 3dB below the input amplitude while tracking a 60mV p-p sine wave. Units in megahertz.

•Notes•

Semiconductor Corporation

CS31412

4 Channel Simultaneous Track and Hold

Features

- Completely Self-Contained
  - Four Track-and-Hold Amplifiers
  - On-Chip Hold Capacitors
  - Two Output Buffer Amplifiers
  - Microprocessor Interface
- 800ns Acquisition Time to 0.01%
- Low Aperture Jitter: 100ps
- 12-Bit Linearity
- Total Offset Including Hold Pedestal: 2.8mV
- Low Droop Rate: 0.001uV/us
- Auto-Calibration Insures Accuracy Over Time and Temperature
- Low Power Dissipation: 250mW

General Description

The CS31412 is a four-channel track and hold capable of processing four single-ended or two differential inputs with 12-bit linearity. It consists of four track-and-hold amplifiers, an analog multiplexer, two output buffers, and a microprocessor interface.

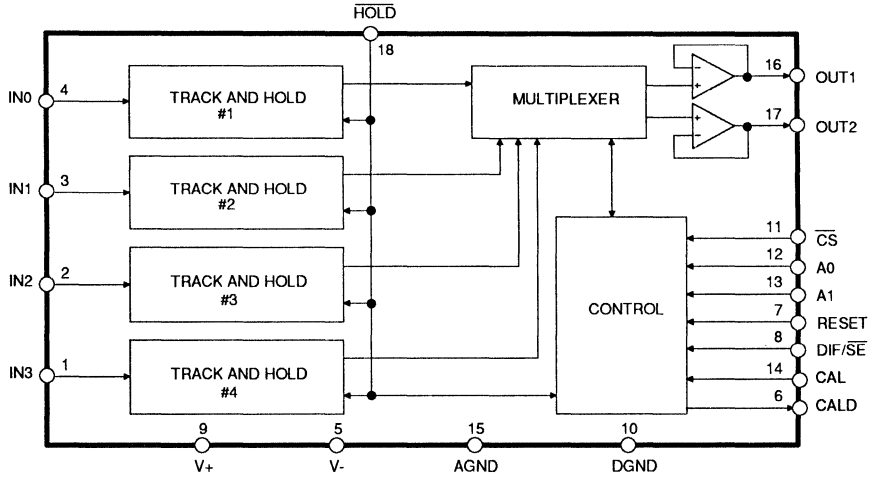
Controlled by a single $\overline{\text{HOLD}}$ input, the four track-and-hold amplifiers can simultaneously hold their outputs with only 100ps of aperture jitter and later acquire their inputs within 800ns to 0.01%. On-chip hold capacitors limit droop to 0.001uV/us, and first order leakage compensation minimizes droop over temperature.

The CS31412 can be configured, controlled, and monitored through its microprocessor interface, or can be operated independently of intelligent control.

ORDERING INFORMATION:

Model	Acquisition Time	Temp. Range	Package
CS31412-KC2	2.0 µs	0 to 70°C	18-pin Ceramic SB DIP
CS31412-KC1	1.0 µs	0 to 70°C	18-pin Ceramic SB DIP
CS31412-BC1	1.0 µs	-40 to +85°C	18-pin Ceramic SB DIP
CS31412-TC1	1.0 µs	-55 to +125°C	18-pin Ceramic SB DIP

5



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS

(T_A = 25°C, V+ = +5.0V, V- = -5.0V, R_L = 10kΩ, C_L = 50pF, Analog Source Impedance = 40Ω, unless otherwise specified)

Parameter*	CS31412-K min	CS31412-K typ	CS31412-K max	CS31412-B min	CS31412-B typ	CS31412-B max	CS31412-T min	CS31412-T typ	CS31412-T max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Accuracy										
Total Offset (Note 1) 25°C		−2.8	± 4.0		−2.8	± 4.0		−2.8	± 4.0	mV
T_{min} to T_{max}			± 4.5			± 5.0			± 5.0	mV
Total Offset Matching										
T_{min} to T_{max} Channels 0-2		0.25			0.25			0.25		mV
Channels 0-3		1.00			1.00			1.00		mV
Offset Drift (Note 2) T_{min} to T_{max}		± 0.020			± 0.025			± 0.030		mV/°C
Tracking Offset			± 55			± 55			± 55	mV
Nonlinearity (Note 3) 25° C			± 0.7			± 0.7			± 0.7	mV
T_{min} to T_{max}		± 0.5			± 0.5			± 0.5		mV
Gain Error (Note 3) 25° C		± 0.01			± 0.01			± 0.01		% FS
T_{min} to T_{max}		± 0.01			± 0.01			± 0.01		% FS
Dynamic Characteristics										
Acquisition Time										
(6V step to 0.01%) -1		0.8	1.0		0.8	1.0		0.8	1.0	us
-2		1.6	2.0							us
(6V step to 0.1%) -1		0.6			0.6			0.6		us
-2		1.2								us
Track to Hold Settling to 0.01%		0.5	0.8		0.5	0.8		0.5	0.8	us
Mux Output Settling Time										
(6V step to 0.01%) -1		1.3	1.5		1.3	1.5		1.3	1.5	us
-2		1.8	2.5							us
(6V step to 0.1%) -1		1.0			1.0			1.0		us
-2		1.5								us
Aperture Time		20			20			20		ns
Aperture Time Matching (Note 4)		2			2			2		ns
Aperture Jitter		100			100			100		ps
Interchannel Aperture Offset		100			100			100		ps
Droop Rate 25°C		± 0.001	± 0.1		± 0.001	± 0.1		± 0.001	± 0.1	uV/us
T_{min} to T_{max}			± 0.6			± 1.0			± 5.0	uV/us

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Applies over specified temperature range without recalibration since calibration at 25°C.
3. Applies over the input voltage range of -3.0V to +3.0V.
4. Part to part.

* Refer to *Error Definitions* at the end of this data sheet.

ANALOG CHARACTERISTICS (Continued)

Parameter*	CS31412-K min	typ	max	CS31412-B min	typ	max	CS31412-T min	typ	max	Units
Analog Input										
Large Signal Bandwidth (6V p-p Input)		2			2			2		MHz
Small Signal Gain Bandwidth (60mV p-p Input)		2.5			2.5			2.5		MHz
Output Slew Rate		10			10			10		V/us
Interchannel Isolation (Note 5)		90			90			90		dB
Input Impedance (dc)		100			100			100		MΩ
Input Capacitance		4			4			4		pF
Input Bias Current		100			100			100		pA
Analog Output										
Noise										
Track Mode (Note 6)		50			50			50		uV_{rms}
Hold Mode (Note 7)		33			33			33		uV_{rms}
Output Impedance at dc (Hold Mode) (Note 8)		0.1			0.1			0.1		Ω
Power Supplies										
Power Supply Currents										
Positive		25	45		25	45		25	45	mA
Negative		−25	−45		−25	−45		25	−45	mA
Power Supply Rejection Ratio										
Positive (Note 9)		75			75			75		dB
Negative (Note 10)		60			60			60		dB

Notes:
5. With a 100kHz input signal.
6. Total noise from dc to 1MHz.
7. Total noise from dc to 1MHz.
8. Applies over the input voltage range of -3V to +3V.
9. With 300mV p-p, 1kHz ripple applied to V+.
10. With 300mV p-p, 1kHz ripple applied to V-.

5

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

Parameter	Symbol	Min	Typ	Max	Units
A0, A1, DIF/$\overline{SE}$, CAL to $\overline{CS}$ Setup Time	t_{su}	20	5	-	ns
$\overline{CS}$ to A0, A1, DIF/$\overline{SE}$, CAL Hold Time	t_h	20	5	-	ns
$\overline{CS}$ Pulse Width	t_{pw}	100	50	-	ns
$\overline{CS}$ Low and CAL High to CALD High	t_{cal}	-	500	-	ms

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V+ = 5V±10%; V- = -5V±10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	1.7	-	V
Low-Level Input Voltage	V_{IL}	-	1.6	0.8	V
High-Level Output Voltage (Note 11)	V_{OH}	V+ -1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA

Note: 11. I_{out}=-100µA. This specification guarantees TTL compatability (VOH = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATION CONDITIONS (AGND, DGND = 0V, see note 12).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive	V+	4.5	5.0	5.5	V
Negative	V-	–4.5	–5.0	–5.5	V
Analog Input Voltage:	V_{IN}	–3.0	-	3.0	V

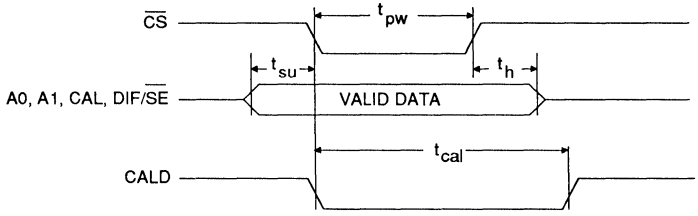
Note: 12. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, All voltages with respect to ground)

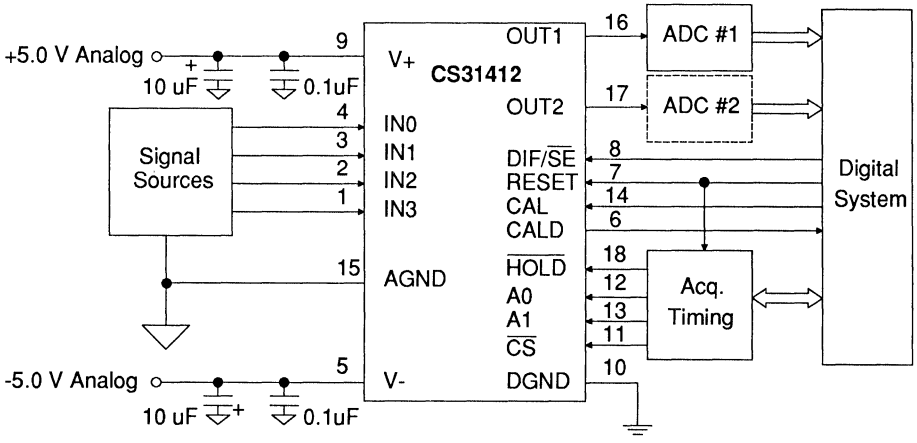
Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive	V+	− 0.3	6.0	V
Negative	V-	0.3	− 6.0	V
Input Current, Any Pin Except Supplies (Note 13)	I_{in}	-	±10	mA
Analog Input Voltage	V_{INA}	V- - 0.3	V+ + 0.3	V
Digital Input Voltage	V_{IND}	- 0.3	V+ + 0.3	V
Ambient Operating Temperature	T_A	- 55	125	°C
Storage Temperature	T_{stg}	- 65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Note: 13. Transient currents of up to 100mA will not cause SCR latch-up. Maximum power supply pin current is ±100 mA.



Timing Diagram



System Connection Diagram

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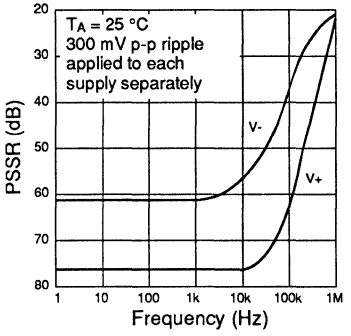
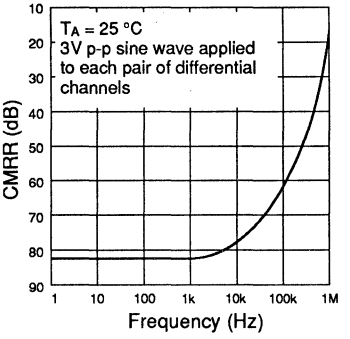
TYPICAL PERFORMANCE CHARACTERISTICS

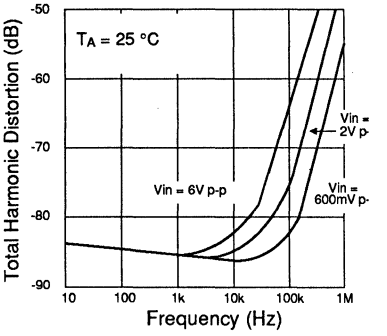
(V+ = +5.0V, V- = -5.0V)



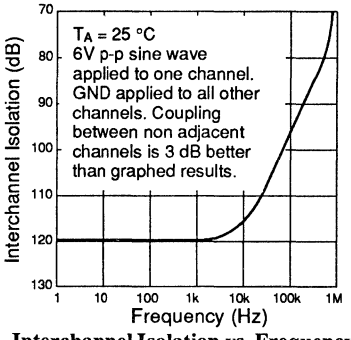
PSSR vs. Frequency



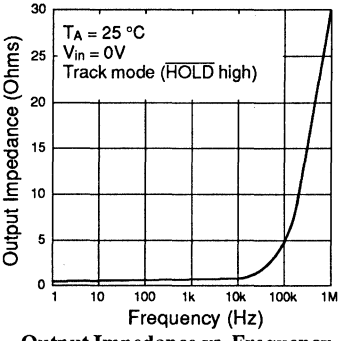
Differential Mode CMRR vs. Frequency



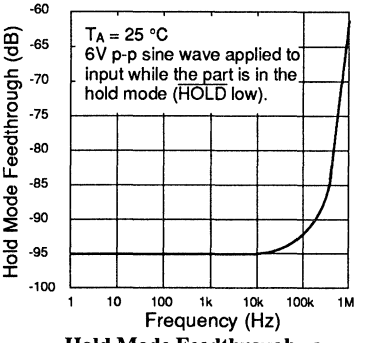
Distortion vs. Frequency



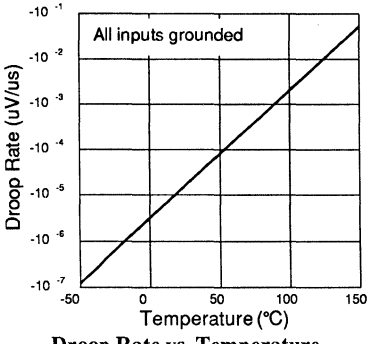
Interchannel Isolation vs. Frequency



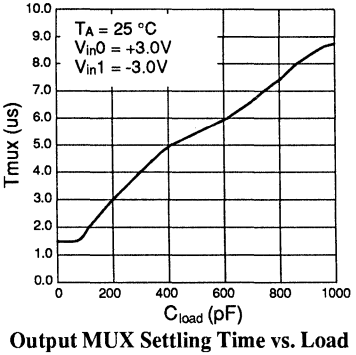
Output Impedance vs. Frequency



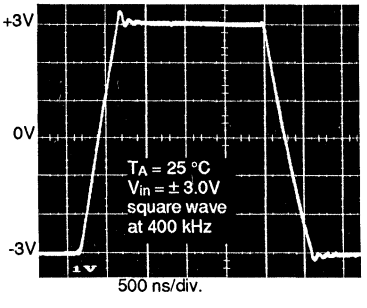
Hold Mode Feedthrough vs. Frequency



Droop Rate vs. Temperature



Output MUX Settling Time vs. Load Capacitance



Full Scale Acquisition

GENERAL DESCRIPTION

The CS31412 consists of four track-and-hold amplifiers with on-chip hold capacitors, an analog multiplexer, and two output buffers. The CS31412 requires no external components or manual trims, and thus eliminates the task of error budgeting several components with complex (and often hidden) error sources.

The CS31412 can handle either four single-ended or two differential analog signals. The device is controlled through its on-board microprocessor interface, or it can be operated independently of intelligent control. Unique auto-calibration circuitry nulls any dynamic or dc error introduced between the analog input pin and the buffer's output for each channel.

Analog Multiplexer

The analog multiplexer takes the outputs of the four track-and-hold amplifiers and passes the selected outputs to the OUT1 and OUT2 pins. When DIF/$\overline{SE}$ is low, the multiplexer is configured as a four-to-one multiplexer and each amplifier is treated as a single-ended analog input referenced to AGND. When DIF/$\overline{SE}$ is high, the multiplexer is configured as dual two-to-one multiplexers and the track-and-hold amplifiers are treated as two groups of two amplifiers which allows the CS31412 to process differential signals. This option can also be used to increase system throughput by using the CS31412 with two A/D converters (see System Throughput). Table 1 shows the multiplexer and buffer amplifier configurations as determined by the DIF/$\overline{SE}$ pin and the address pins, A0 and A1. In the differential mode, the A0 input should be tied low to avoid floating the output buffer amplifiers. In addition, the buffer amplifier at OUT2 in the single-ended mode does not float; its output remains within 50mV of AGND and must remain unconnected.

DIF/$\overline{SE}$	A1	A0	OUT1	OUT2
0	0	0	IN0	0V*
0	0	1	IN1	0V*
0	1	0	IN2	0V*
0	1	1	IN3	0V*
1	0	0	IN0	IN1
1	0	1	N/A**	N/A**
1	1	0	IN2	IN3
1	1	1	N/A**	N/A**

* AGND ± 50mV
** Indeterminate Output: A0 should be tied low in differential mode

Table 1. Truth Table of MUX Configurations

Calibration

The CS31412 features on-chip digital intelligence and measurement circuitry capable of calibrating all four input channels. For each channel, the device internally deselects the input signal and switches a known reference voltage (AGND) to the input of the track-and-hold amplifier. In the calibration mode, the CS31412 uses an internal microcontroller and special nulling circuitry to reduce all errors at the OUT1 and OUT2 pins. Thus, all internal errors including dc offsets and dynamic errors due to charge injection (hold pedestal) are trimmed. The output of the CS31412 is only corrected for offset during the hold mode ($\overline{HOLD}$ low). During tracking, each channel may have up to ± 55mV of offset.

The user must initiate a calibration to initially calibrate the device. This is achieved by bringing the CAL input high and $\overline{CS}$ low. Calibration can be similarly initiated during operation at any time thus insuring accuracy under any conditions. During the calibration cycle (which takes about 500 ms to complete) the CALD pin remains low. During this period, any load on OUT1 and OUT2 must remain constant; otherwise, errors could be introduced which might affect accuracy. If a new calibration is initiated before the current calibration is finished, the CS31412 will complete the current calibration before initiating the new one. CALD will go high when calibration is finished.

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The DIF/$\overline{SE}$ input to the CS31412 must be in the correct state when initiating a calibration since the offsets of the analog output buffers are also calibrated. If the part is switched between the single ended and differential modes during operation, a new calibration must be initiated to guarantee that the Total Offset specification is met.

Digital Interface

The CS31412 includes a digital interface designed for maximum flexibility. The digital inputs, A0, A1, CAL, and DIF/$\overline{SE}$, are internally gated with $\overline{CS}$. The input latches for the A0 and A1 inputs are level sensitive and latch on the rising edge of $\overline{CS}$. Any state changes on these pins while $\overline{CS}$ is low appear at the output(s). In a microprocessor-controlled application, the $\overline{CS}$ control input is usually derived from a decoded address as well as write and strobe signals off of the control bus (Figure 1a). Channel selection and calibration initiation thereby involve writing to the CS31412's address using data bits to control A0, A1, CAL, and DIF/$\overline{SE}$. For microprocessor-independent operation in single-ended mode, $\overline{CS}$ is tied low and the digital inputs are controlled by externally-latched signals (Figure 1b).

The CS31412's CALD output can be used to generate an interrupt indicating the CS31412 has completed calibration. Alternatively, calibration status can be polled in software by connecting CALD to the data bus via a 3-state buffer.

Reset

The CS31412 must be reset after power up to ensure correct operation. The reset function is invoked by bringing the RESET pin high for at least 1 µs. An RC network attached to the RESET pin will reset the part (See Figure 1b).

System Throughput

Throughput of the CS31412 varies depending on the number of input signals used. System timing diagrams which enable the throughput of the CS31412 to be calculated are shown in Figure 2. Table 2 is a listing of throughput times for the number of input channels used. These times assume that no time is required for A/D conversion. When the part is used in the differential mode, throughput time will be equal to the two channel throughput time.

Since one of the four channels must be connected to the output buffer, the Track-to-Hold settling time (t_{tth}) is included in the first channel's settling time (t_1). The address inputs A0, and A1 must be switched before the part is put in the hold mode ($\overline{HOLD}$ low) so that the first channel's output is valid at time (t_1). After the first output is settled,

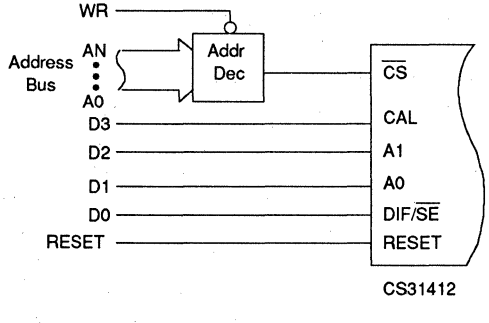


Figure 1a. CPU-Control

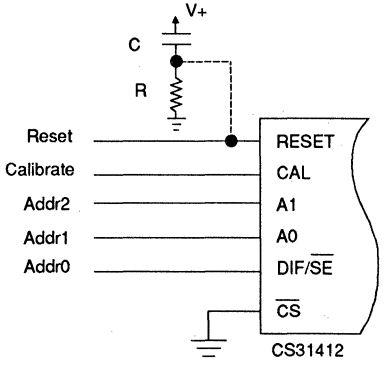


Figure 1b. CPU-Independent Control

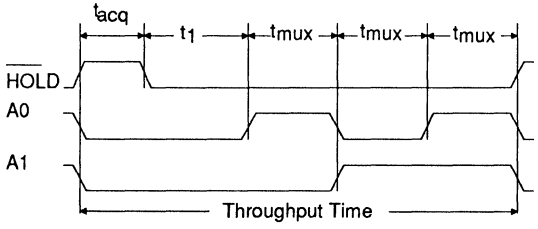
the addresses can be used to mux each of the other three channels to the output.

When interfacing the CS31412 with an A/D converter which includes an integrated sample/hold, such as Crystal's CS501X series, additional reduction in throughput time can be obtained by pipelining settling times. As soon as the A/D has captured the output of the CS31412, $\overline{HOLD}$ can be brought high and the CS31412 can acquire the new input signals and settle the first muxed channel while the A/D is converting. Likewise, output mux settling for all other other channels can be pipelined during conversion removing all of the CS31412's timing from the throughput equation. System throughput can therefore proceed at the ADC's maximum throughput. Using the CS31412 in the differential mode with two ADCs will reduce throughput time further because two channels can be converted simultaneously.

Power Supplies and Input Connections

The CS31412 uses the analog ground voltage (AGND) only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on AGND relative to the system's analog ground plane will result in offset errors. Therefore, the analog inputs should be referenced to the AGND pin which should be used as the entire system's analog ground. Decoupling should be performed between the V+, V- pins and AGND using 0.1uF ceramic capacitors. If significant low frequency noise is present on the supplies, 10µF tantalum capacitors are recommended in parallel with the 0.1uF capacitors. *The decoupling capacitors should be placed as close to the CS31412's power supply pins as possible.*

The signal source impedances which drive the four input channels of the CS31412 should be minimized as much as possible. Low source impedance reduces the sensitivity of the input pins to picking up capacitively-coupled energy from logic level transitions, such as $\overline{HOLD}$ going low.



t_{acq}: Acquisition Time
t_{tth}: Track to Hold Settling Time
t_{mux}: Mux Output Settling Time
t_1: First Channel Settling Time
$t_1 = \sqrt{t_{tth}^2 + t_{mux}^2}$

Figure 2. Four Channel Timing

Single Channel	Two Channels	Three Channels	Four Channels
2.70us	4.20us	5.71us	7.19us

Table 2. Throughput Time

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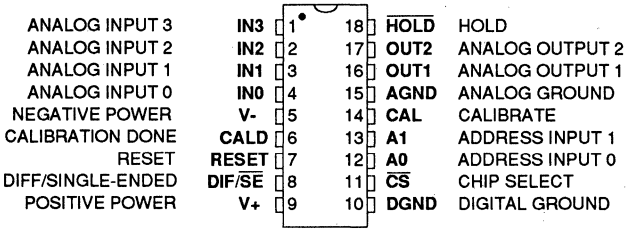
PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power, PIN 9
Most positive supply voltage. Nominally +5 volts.

V- - Negative Power, PIN 5
Most negative supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 10
Digital ground reference.

AGND - Analog Ground, PIN 15
Analog ground reference.

Analog Inputs

IN0; IN1; IN2; IN3 - Analog Inputs 0;1;2;3, PINS 4,3,2,1
Analog inputs to the four track and hold amplifiers.

Digital Inputs

$\overline{CS}$ - Chip Select, PIN 11
Enables the DIF/$\overline{SE}$, A0, A1, and CAL digital inputs.

RESET - Reset, PIN 7
The CS31412 must be reset to ensure correct operation. Reset occurs when RESET is high.

DIF/$\overline{SE}$ - Differential/Single-Ended Select, PIN 8

Configures the output multiplexer in either a single-ended or differential mode. It is latched on the rising edge of $\overline{CS}$, but usually tied high or low. If set low, the four analog inputs are routed through OUT1. If set high, IN0 and IN1 are paired as one differential signal and IN2 and IN3 are paired as a second.

A0; A1 - Address Input 0; Address Input 1, PINS 12, 13

Select which amplifier or amplifier pair is output on the OUT1 and OUT2 pins. A0 should be held low when DIF/$\overline{SE}$ is high to avoid floating the outputs.

CAL - Calibrate, PIN 14

When taken high with $\overline{CS}$ low, initiates a full internal calibration.

$\overline{HOLD}$ - Hold, PIN 18

A falling transition on this pin signals all four amplifiers to hold their inputs simultaneously. When brought high, the amplifiers acquire, and then track the input signal.

Analog Outputs

OUT1; OUT2 - Analog Output 1; Analog Output 2, PINS 16, 17

The buffered outputs from the multiplexer; OUT1 is always active and OUT2 is active only in the differential mode (DIF/$\overline{SE}$ high).

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Digital Outputs

CALD - Calibration Done, PIN 6

Indicates calibration status. If CALD is high the device has finished calibration. If CALD is low the device is calibrating.

ERROR DEFINITIONS

Total Offset - The difference between the analog voltage applied to the analog input (A0, A1, A2, or A3) and the signal that appears at the appropriate output pin (OUT1 or OUT2) after the hold command has been issued and all transients have settled. Applies only in the hold mode, not while tracking the analog inputs. Includes all internal offsets, including those due to charge injection (hold pedestals). Units in millivolts.

Nonlinearity - The deviation from a straight line on the plot of output vs input. Nonlinearity is specified as the change in *Total Offset* over the signal range of -3V to +3V. Units in millivolts.

Gain Error - Calculated as the difference between the *Total Offsets* resulting from -3V and +3V dc input signals relative to a 6V input range. Units in percent of full scale.

Acquisition Time - The time required after the negation of the hold command ($\overline{HOLD}$ high) for the track-and-hold amplifiers to reach their final values to within a specified error band (±0.01% or ± 0.1%). Measured internally at the inputs to the multiplexer, it determines the minimum time allowed before reassertion of the hold command. Indicates nothing about the outputs as measured at OUT1 or OUT2. Units in microseconds.

Track-to-Hold Settling - The time required after the hold command is given for each track and hold to reach its final value to within a specified error band (±0.01%). Includes switch delay (aperture) time but not multiplexer and output buffer settling. Units in microseconds.

MUX Output Settling - The time required after reconfiguring the multiplexer for the outputs at OUT1 and OUT2 to reach their final value to within a specified error band (±0.01% or ±0.1%). Measured from the falling edge of $\overline{CS}$ with A0 and A1 valid. Units in microseconds.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Interchannel Aperture Offset - The range of variation in aperture time between the four track-and-hold amplifiers for a given hold command. A measure of simultaneity. Units in picoseconds.

Droop Rate - The change in the output voltage over time while in the hold mode. Units in microvolts per microsecond.

Large Signal Bandwidth - The frequency at which the output amplitude while tracking a full scale 6Vp-p sine wave is 3dB below the input amplitude. Units in megahertz.

Small Signal Gain Bandwidth - The frequency at which the output amplitude while tracking a 60 mVp-p sine wave is 3dB below the input amplitude. Units in megahertz.

Interchannel Isolation - A measure of crosstalk between input channels while in the track mode. Units in decibels.

INTRODUCTION

Ideal for adaptive filtering applications, the CS7008 digitally programmable switched capacitor filter provides the user with complete software control over the filter response.

Virtually any audioband filter response of eighth order or below is obtained by writing digital configuration coefficients to on-chip registers through a standard microprocessor interface. The chip can also load itself by reading coefficients directly from memory. Accuracy of a filter response is typically within 1 percent of the calculated value (for corner frequencies) and dynamic range is a minimum of 72 dB. Bandwidth varies depending upon the transfer function implemented, but can extend from 0 to 50 kHz. Anti-aliasing, smoothing and input gain control are supported with on-chip uncommited operational amplifiers.

The user is provided instant feedback on filter performance in his system by the Crystal-ICE filter development system. The PC-based design tool includes filter synthesis software and an in-circuit hardware emulator.

USER'S GUIDE

Device:	CS7008
Frequency Range	5Hz to 20kHz
Dynamic Range	72 dB
Maximum Filter Order	8th
Power Dissipation	180 mW
Package	28 pin DIP

CONTENTS

Semiconductor Corporation

CS7008

Digitally Configurable Universal Filter

Features

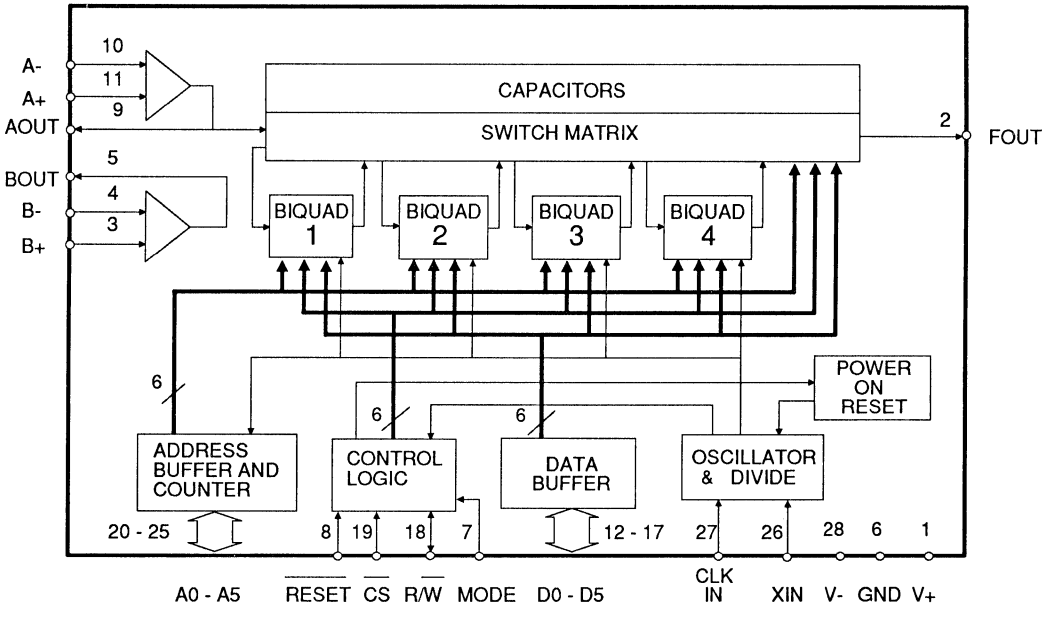
- Implements Even-Order Filters:
  To 50 kHz
  To 8th Order
- Same output pin for all filter types
- Digitally Programmable:
  Self Loading Mode
  µP bus Mode
- Filter can be changed in 30 µs for adaptive applications
- Two Uncommitted Op Amps for Input Antialiasing and Output Smoothing
- Supported by CRYSTAL-ICE Filter Development System CDS7000
- Readback capability

General Description

The CS7008 is fabricated in standard 3 micron digital CMOS. It achieves high levels of performance through Crystal's SMART *Analog*™ design techniques. The CS7008 is a digitally configurable switched capacitor filter capable of implementing virtually any even-order filter response of eighth order or below to 50 kHz. A microprocessor interface permits in-system reconfiguration of the filter resonse. Access to two op amps is also provided for use as input antialialsing and output smoothing filters if desired.

System design is greatly simplified by using the Crystal-ICE Filter Development System, CDS7000. The development system provides menu-driven software that aids in the design and optimization of filters and provides hardware to download the filter parameter to a CS7008 (for in-circuit verification of performance) or to an EPROM programmer or DOS Files. The development system consists of hardware and software for use with an IBM PC and provides in-circuit emulation of the CS7008.

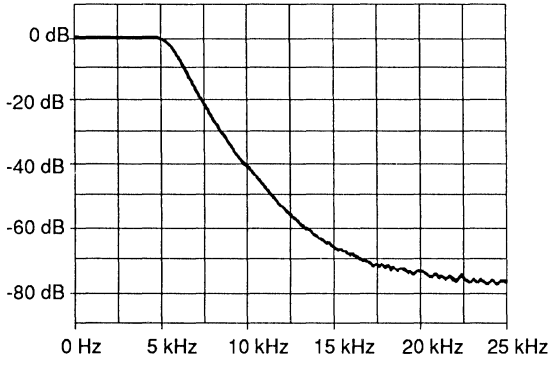
ORDERING INFORMATION: **Page 10-26**



ANALOG CHARACTERISTICS (T_A = T_{min} to T_{max}, V+ = 5.0V, V = -5.0V, GND = 0V; transfer functions shown in Figure 1; unless otherwise specified.)

Parameter	CS7008 min	CS7008 typ	CS7008 max	CS7008-I min	CS7008-I typ	CS7008-I max	CS7008-M min	CS7008-M typ	CS7008-M max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Filter										
Dynamic Range	72			72			72			dB
Output Noise			480			480			480	uV rms
Signal to THD (Note 1)	50	55		50	55		50	55		dB
Device to Device Phase Matching		±2			±2			±2		Degrees
Device to Device Gain Matching		±0.3			±0.3			±0.3		dB
DC Output Offset Filter #1		140			140			140		mV
Filter #2		-300			- 300			- 300		mV
Clock Feedthrough		40			40			40		mV p-p
Input Voltage Range	- 3.0		3.0	-3.0		3.0	- 3.0		3.0	V_{peak}
Output Voltage Swing THD = -50 dB	- 2.75		2.75	-2.75		2.75	- 2.75		2.75	V_{peak}
Auxiliary Amplifiers										
DC Open Loop Gain (Note 2)		78			78			78		dB
Gain Bandwidth Product (Note 2)		1.0			1.0			1.0		MHz
Input Offset Voltage		25			25			25		mV
Output Swing (Note 2)	- 3.5		3.5	- 3.5		3.5	- 3.5		3.5	V_{peak}
Output Short Circuit Current		0.5			0.5			0.5		mA
Common Mode Range (Note 2)	- 3.5		3.5	-3.5		3.5	- 3.5		3.5	V_{peak}
Common Mode Rejection Ratio (Note 3)		60			60			60		dB
Slew Rate (Note 4)		2.0			2.0			2.0		V/us
Power Supplies										
Power Suppply Currents										
Positive		13	25		13	25		13	25	mA
Negative		- 13	- 25		- 13	- 25		- 13	- 25	mA
Power Dissipation		130	250		130	250		130	250	mW

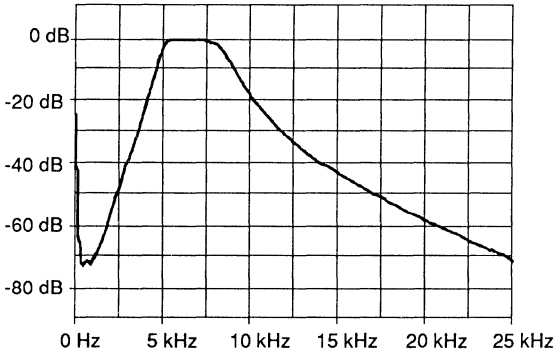
Notes: 1. V_{in} = ±2.75 Vpeak, at 500 Hz for Filter #1 and at 5 kHz for Filter #2.
2. R_L = 1 MΩ.
3. fo = 60 Hz.
4. R_L = 1 MΩ, C_L = 20 pF



Clock = 3MHz
CLKDIV = 2 (decimal)
F_S = 250 kHz
barr = 1317 (decimal)
conf = 1 (decimal) for each biquad

Capacitor Coefficients (Decimal):			
Biquad 1	Biquad 2	Biquad 3	Biquad 4
A = 318	A = 264	A = 201	A = 152
F = 318	F = 264	F = 169	F = 56
C = 72	C = 85	C =107	C =134
J = 6	J = 5	J = 5	J = 5
I = 6	I = 5	I = 5	I = 5
G = 72	G = 85	G = 107	G = 134

Filter #1: Low Pass Butterworth Filter



Clock = 3MHz
CLKDIV = 2 (decimal)
F_S = 250 kHz
barr = 1317 (decimal)
conf = 3 (decimal) for each biquad

Capacitor Coefficients (Decimal):			
Biquad 1	Biquad 2	Biquad 3	Biquad 4
A = 214	A = 126	A = 193	A = 153
F = 45	F = 27	C = 100	F = 79
C = 213	C = 127	F = 180	C = 143
H = 218	H = 367	H = 267	H = 333
I = 45	I = 45	I = 50	I = 50
G = 218	G = 367	G = 267	G = 333

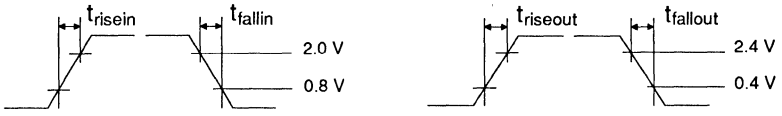
Filter #2: Band Pass Butterworth Filter

Figure 1. Production Test Filter Transfer Functions

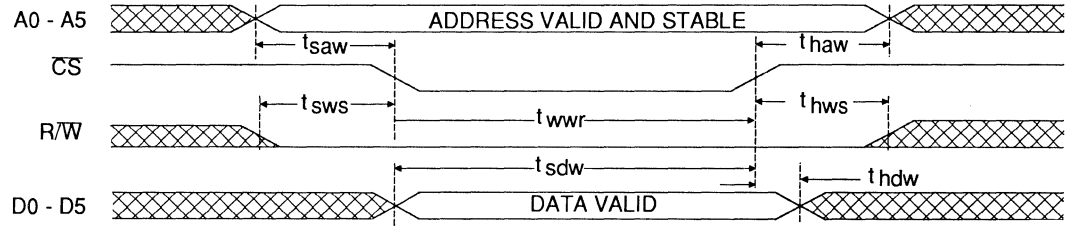
SWITCHING CHARACTERISTICS (TA = Tmin to T max, V+ = 5.0V ± 10%, V- = -5.0V ± 10%, GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
Output Rise Time	(Note 5)	t riseout		15	20	ns
Output Fall Time	(Note 5)	t fallout		15	20	ns
Input Rise Time		t risein		20	1000	ns
Input Fall Time		t fallin		20	1000	ns
Clock Specfications						
Maximum Oscillator Frequency		f_{osc}	4.0	10		MHz
Minimum Oscillator Frequency		f_{osc}		3		kHz
Oscillator Duty Cycle			40		60	%
Maximum Sampling Frequency		f_s	250	260		kHz
Minimum Sampling Frequency		f_s		5		Hz
Writing to the CS7008						
Address-Write Set-Up Time		t_{saw}	150			ns
Address-Write Hold Time		t_{haw}	10			ns
Write Pulse-Width Low		t_{wwr}	300			ns
Data-Write Set-Up Time	(Note 6)	t_{sdw}	300			ns
Data-Write Hold Time		t_{hdw}	10			ns
Write-Chip Select Set-Up Time		t_{sws}	0			ns
Write-Chip Select Hold Time		t_{hws}	0			ns
Reading from the CS7008						
Address-Read Set-Up Time		t_{sar}	0			ns
Address-Read Hold Time		t_{har}	10			ns
Read Enable to Read Stable Hold Time		t_{sres}	0			ns
Read Enable to Read Stable Hold Time		t_{hres}	0			ns
Read Strobe to Data Valid Delay		t_{dsdv}	500			ns
Read Strobe Data Valid Hold Time		t_{hsdv}	0			ns
Reading from External ROM						
Auto-Address to Write Set-Up	(Note 7)	t_{saaw}	1 MCC			ns
R/$\overline{W}$ Pulse Width		t_{rw}		2.5 MCC		ns
Data Valid After R/$\overline{W}$ Goes High		t_{dh}	0			ns
ROM Access Time	(Note 8)	t_a			2MCC	ns

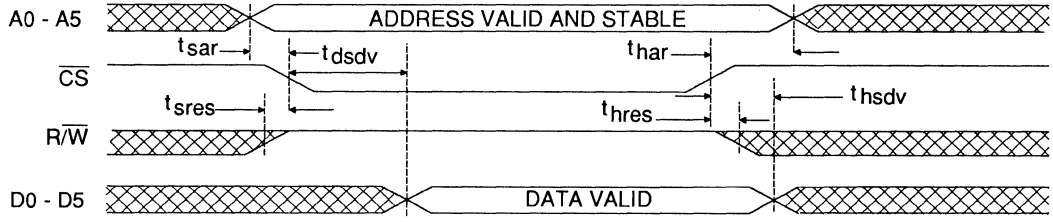
Notes: 5. 50 pF load (includes probe and jig capacitance).
6. Minimum time required for data to be valid while write pulse is low.
7. MCC = Master Clock Cycle = 250 ns with a 4 MHz Clock.
8. Maximum allowable ROM output delay .



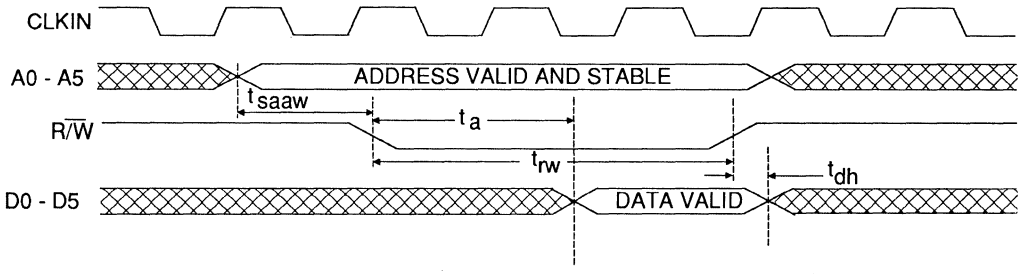
Rise and fall times



Writing to the CS7008



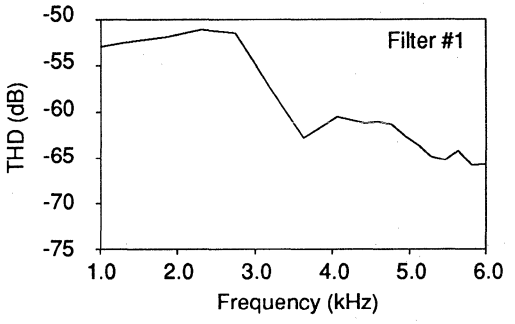
Reading from the CS7008



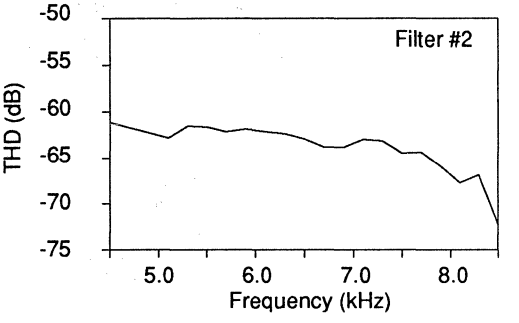
Reading from the external ROM

Figure 2. Switching Characteristics

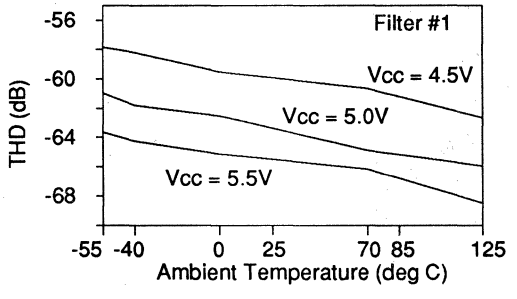
Typical Performance - Production Test Filters



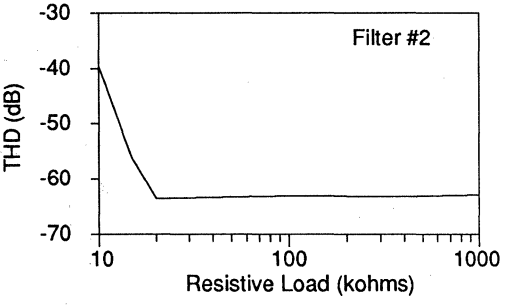
Total Harmonic Distortion vs. Frequency in Passband



Total Harmonic Distortion vs. Frequency in Passband

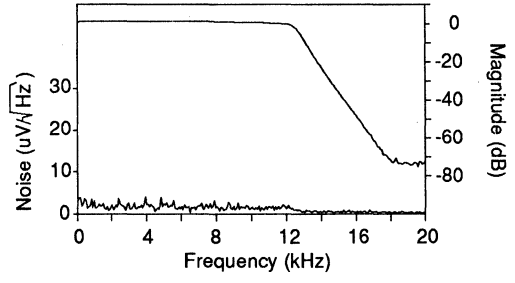


Total Harmonic Distortion vs. Temperature

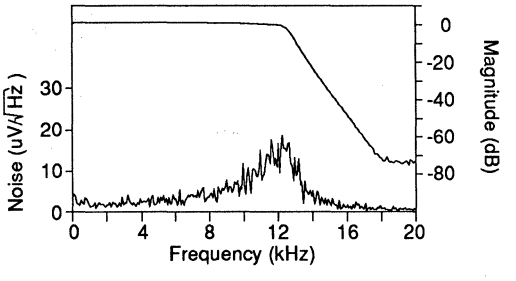


Total Harmonic Distortion at BOUT vs. Load

Performance Dependence on Biquad Ordering; Eighth Order Low Pass Filter

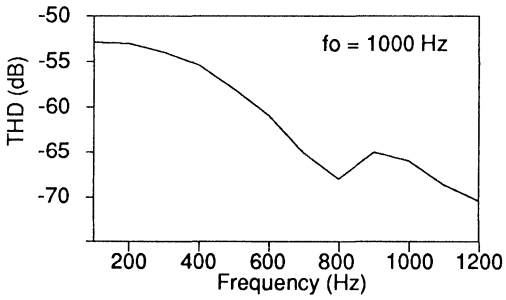


Attenuation and Noise vs. Frequency with High Q First

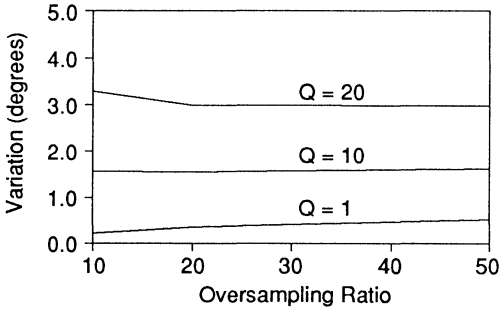


Attenuation and Noise vs. Frequency with Low Q First

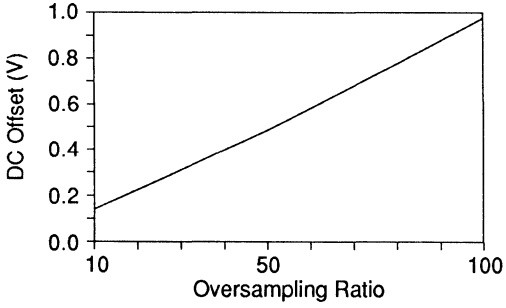
Typical Performance - Single Biquad



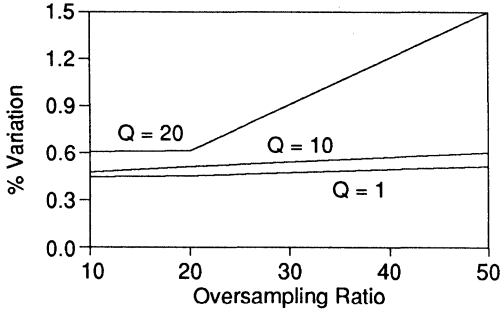
Total Harmonic Distortion vs. Frequency in Passband (Single-Biquad Low Pass Filter)



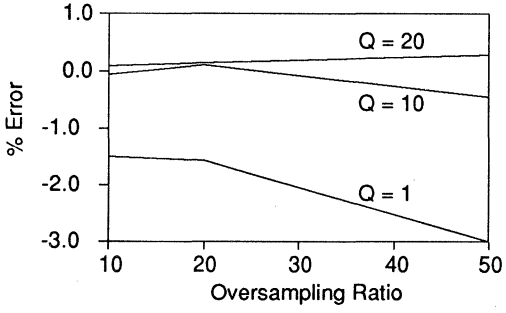
Unit-to-Unit Phase Variation vs. Oversampling Ratio



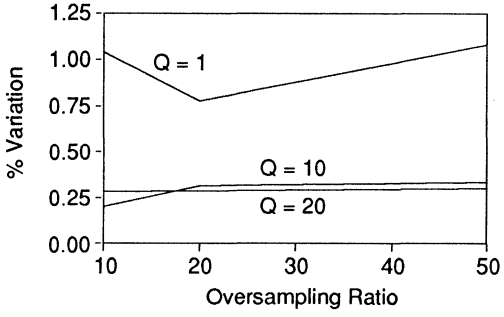
DC Offset vs. Oversampling Ratio



Unit-to-Unit Gain Variation vs. Oversampling Ratio



Center Frequency Accuracy vs. Oversampling Ratio



Unit-to-Unit Center Frequency Variation vs. Oversampling Ratio

Biquad #1			Biquad #2			Biquad #3			Biquad #4			Capacitor or Code	Byte	# of Bits	Comments
Binary	Hex	Dec	Binary	Hex	Dec	Binary	Hex	Dec	Binary	Hex	Dec				
000000	00	00	010000	10	16	100000	20	32	110000	30	48	A	Low	5	
000001	01	01	010001	11	17	100001	21	33	110001	31	49	A	High	6	
000010	02	02	010010	12	18	100010	22	34	110010	32	50	E/F	Low	5	
000011	03	03	010011	13	19	100011	23	35	110011	33	51	E/F	High	6	
000100	04	04	010100	14	20	100100	24	36	110100	34	52	CE/C	Low	5	CE - E Damping
000101	05	05	010101	15	21	100101	25	37	110101	35	53	CE/C	High	6	C - F Damping
000110	06	06	010110	16	22	100110	26	38	110110	36	54	conf		2	Configuration Byte
000111	07	07	010111	17	23	100111	27	39	110111	37	55				Not Used
001000	08	08	011000	18	24	101000	28	40	111000	38	56	J/H	Low	5	
001001	09	09	011001	19	25	101001	29	41	111001	39	57	J/H	High	6	
001010	0A	10	011010	1A	26	101010	2A	42	111010	3A	58	I	Low	5	
001011	0B	11	011011	1B	27	101011	2B	43	111011	3B	59	I	High	6	
001100	0C	12	011100	1C	28	101100	2C	44	111100	3C	60	G	Low	5	
001101	0D	13	011101	1D	29	101101	2D	45	111101	3D	61	G	High	6	

Table 1. Biquad Address Map

Binary	Hex	Dec	Code	Byte	# of Bits	Function
001110	0E	14				Not Used
001111	0F	15				Not Used
011110	1E	30	cdc		3	Clock Divide Code
011111	1F	31				Not Used
101110	2E	46				Not Used
101111	2F	47				Not Used
111110	3E	62	barr	Low	6	Biquad Arrangement
111111	3F	63	barr	High	5	Biquad Arrangement

Table 2. Mode Address Map

D1	D0	conf	J / H	E / F	CE / C	Comments
0	0	0	J	E	CE	J input cap. with E damping. CE = C + E *
0	1	1	J	F	C	J input cap. with F damping.
1	0	2	H	E	CE	H input cap. with E damping. CE = C + E *
1	1	3	H	F	C	H input cap. with F damping.

* See "Biquads" section for more information on CE/C.

Table 3. Biquad Configuration Codes: conf

D2	D1	D0	cdc	CLKDIV
0	0	0	0	1
0	0	1	1	2
0	1	0	2	4
0	1	1	3	8
1	0	0	4	16
1	0	1	5	32
1	1	0	6	64
1	1	1	7	128

Note: CLKDIV = 2^{cdc}

Oscillator Frequency = f_{OSC}

Sample Frequency = f_S

$$f_S = \frac{f_{OSC}}{6 \times CLKDIV}$$

Table 4. Clock Divide Codes: cdc

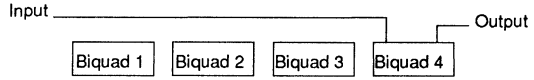
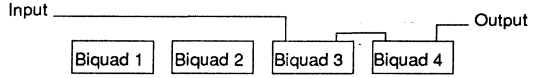
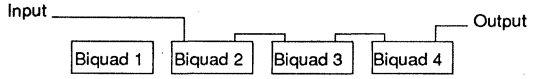
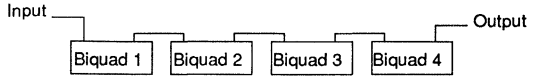
barr (low byte) Address 3E Binary	Hex	Dec	barr (high byte) Address 3F Binary	Hex	Dec	Configuration
000000	00	00	011000	18	24	
000000	00	00	010101	15	21	
101000	28	40	010100	14	20	
100101	25	37	010100	14	20	

Table 5. Biquad Arrangement Codes: barr

DIGITAL CHARACTERISTICS (TA = TMIN to TMAX; V+ = 5.0V±10%, V- = -5.0V±10%, GND = 0V; measurements perfomed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage Except Pins 7 & 27	V_{IH}	2.0			V
Pins 7 & 27 only		70% V+			V
Low-Level Input Voltage Except Pins 7 & 27	V_{IL}			0.8	V
Pins 7 & 27 only				30% V+	V
High-Level Output Voltage I_{out}= -100uA (Note 9)	V_{OH}	2.4			V
Low-Level Output Voltage I_{out}= 1.6mA (Note 9)	V_{OL}			0.4	V
Input Leakage Current				10	uA
Three-State Leakage Current		- 10		10	uA

Note: 9. Digital outputs will output CMOS logic levels into a CMOS load.

RECOMMENDED OPERATING CONDITIONS (Voltages with respect to GND = 0V.)

Parameter	Symbol	Min	Typ	Max	Units
Positive Supply	V+	4.5	5.0	5.5	Volts
Negative Supply	V-	- 4.5	- 5.0	- 5.5	Volts
Ambient Operating Temperature -P -ID -MD	T_A	0 -40 -55		+70 +85 +125	°C

ABSOLUTE MAXIMUM RATINGS (Voltages with respect to GND = 0V.)

Parameter	Symbol	Min	Max	Units
DC Supplies Positive Negative	V+ V-	- 0.3 + 0.3	+6.0 -6.0	Volts
Input Voltage	V_{in}	V- - 0.3	V+ + 0.3	Volts
Input Current, Any Pin (Note 10)	I_{in}		10	mA
Power Dissipation	P_D		500	mW
Ambient Operating Temperature -P -ID -MD	T_A	0 -40 -55	+70 +85 +125	°C
Storage Temperature	T_{stg}	- 65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

Note: 10. Transient currents of up to 100mA will not cause SCR latch up.

THEORY OF OPERATION

The CS7008 is a programmable universal filter consisting of four separate biquadratic filter sections, any one of which is independently programmable to implement high-pass, low-pass, band-pass, band-reject, or all-pass filter functions. Almost any even order (eighth order or below) filter to 50kHz can be obtained. The biquad filter sections can be cascaded using 1, 2, 3, or 4 sections to achieve 2nd, 4th, 6th, or 8th order filters. The CS7008 filter configurations can be completely reconfigured by a microprocessor in 30 µs or, in the self-program mode, sets of filter coefficients can be read by the CS7008 from an external memory (ROM, EPROM, etc.).

The basic schematic of a single biquad is shown in Figure 3. The input signal is sampled on capacitors G and H, and charge packets are passed through the remaining capacitors to the output. The filtering achieved by each biquad is a function of the ratios of the capacitors, the switching rate, and the configuration of the switches. A good description of how such biquads operate is given in chapter 6 of "Modern Filter Design" by M. S. Ghausi and K. R. Laker, published by Prentice-Hall.

In the CS7008 implementation of switched-capacitor biquads, two capacitors are fixed at a nominal capacitance value of 1024 (capacitors B and D in Figure 3). Each of the other capacitors can be programmed to take on values from 0 to 2047, (2^{11} possibilities). The programmable capacitors and programmable switch configurations allow full user control over gains, attenuation, cut-off frequencies, etc. For example, capacitors E and F in Figure 3 can be used to implement damping either in the output amplifier stage or around both amplifiers. (In subsequent sections of this data sheet, as well as in generic filter publications, these capacitors routinely show up in discussions of "E-damping" vs. "F-damping".)

6

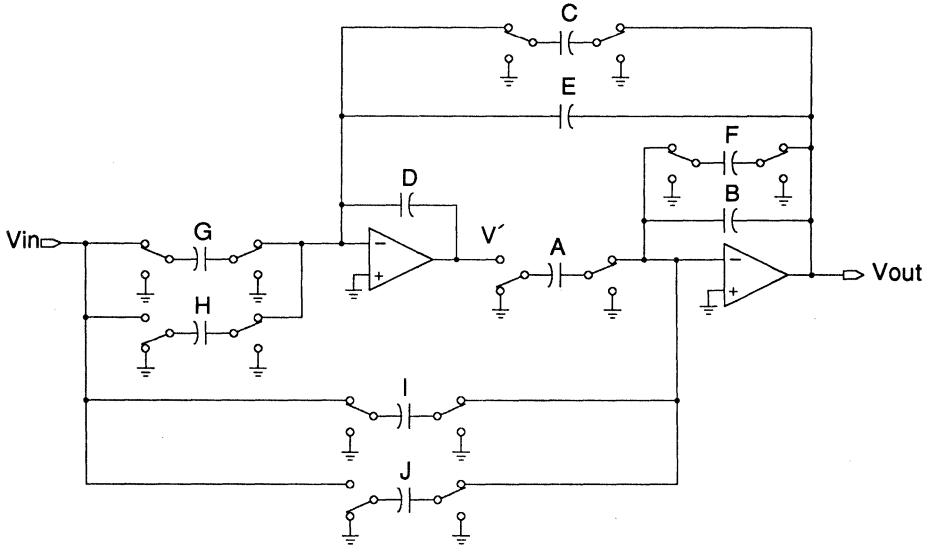


Figure 3. General Active Switched Capacitor Biquad Filter

Filter Development Support

Filter design is supported by the CRYSTAL-ICE (In-Circuit-Emulator) Filter Development System, the CDS7000. The CRYSTAL-ICE package includes software that generates the coefficients for the CS7008. The CDS7000 system also includes hardware for in-circuit testing of the filter design and a Crystal CDB7008 evaluation board to simplify testing. Software in the CDS7000 downloads filter designs to your EPROM programmer or DOS files. The user specifies the filter parameters in terms of transition frequencies and their respective magnitudes, and the system then generates the filter and provides an interface through which coefficients can be down-loaded to an in-circuit CS7008. CRYSTAL-ICE supports development of low-pass, high-pass, band-pass, and band-stop filters. Butterworth, Chebyshev I and II, and elliptic (Cauer) filter responses can be directly implemented.

The user can also enter his own transfer functions to implement any filters not directly supported by CRYSTAL-ICE (i.e. All-Pass, Telecom filters, etc.) As with the above filters, these can be down-loaded from CRYSTAL-ICE to the CS7008 to evaluate their performance.

Configuration Information

The CS7008 must be loaded with valid data before the filter will function. The data consists of a clock divide code, (cdc), capacitor coefficients, a configuration code for each biquad required, (conf), and a biquad arrangement code, (barr). Information on each of these parameters is provided in subsequent sections. Tables 1 and 2 show how the data must be arranged for loading into the CS7008.

Clock

As with any sampled data system, the maximum signal frequency that can be effectively sampled, processed, and reconstructed is the Nyquist frequency, $f_S/2$. As filter cutoff frequencies approach the Nyquist frequency, several things happen:

a) Sin(x)/x distortion increases and requires compensation,

b) Antialiasing and reconstruction filter complexity increases,

c) CS7008 coefficients are larger and coefficient truncation effects are minimized.

To minimize the unfavorable effects of sin(x)/x distortion, and reduce antialiasing and reconstruction filter complexity, the sampling frequency, f_S, should be at least 10 times higher than the signal's highest frequency of interest. Crystal recommends an oversampling ratio of 10 to 20. Such oversampling ratios usually provide acceptable capacitor values, negate sin(x)/x distortion, and reduce antialiasing filter complexity. Oversampling ratios of 100 or more should be avoided since they drive some capacitor values close to or equal to zero. This increases DC offset and, when equal to zero, could make the biquad unstable (output driven to one voltage rail).

When an acceptable f_S for a particular application has been determined, the required oscillator frequency, f_{osc}, can be derived from Equation 1.

$$fosc = fs \times 6 \times CLKDIV$$

Equation 1

The maximum sampling frequency for the CS7008 is 250 kHz. CLKDIV corresponds to the clock divide code, (cdc), which is loaded into the memory of the CS7008 and sets an internal clock divide. If the oscillator frequency exceeds 1.5 MHz, CLKDIV must be set so f_S does not exceed 250 kHz. Permissible CLKDIV's are; 1, 2,

4, 8, 16, 32, 64, and 128. The clock divide code is loaded at address 30 (1E hex). See Table 4 for more information. Note that for a given filter configuration, a change in f_S will result in a proportional change in the filter's pass band frequencies, but the filter Q will remain the same.

Signal Input and Output

To achieve optimum performance, the largest input signal amplitudes should be adjusted to approach the device's maximum input level. Such input signals take advantage of the dynamic range of the device, thereby maximizing the signal-to-noise ratio. An antialiasing filter may be required at the input, with enough attenuation to reject input frequency components at half the sampling frequency. The input op amp can be used to perform this low-pass filtering function.

The output signal is a 100% duty cycle Pulse Amplitude Modulated (PAM) staircase signal, constructed at the sampling frequency, f_S. The uncommitted output op amp can be configured as a smoothing filter for the output signal.

Data Input/Output

The CS7008 contains six address lines, A0 - A5, and six data lines, D0 - D5. Since the data bus is six bits, all references to a "byte" refer to a six bit byte. Some of the bytes needed to configure the CS7008 do not use all six bits. In these cases the unused bits are the most significant bits and are considered "don't cares" (x) when written. When reading from the CS7008, unused bits should be masked off.

The CS7008 can be loaded by a microprocessor or from external ROM by an automatic "self-programming" routine contained in the CS7008. The MODE pin determines whether the CS7008 is in the microprocessor mode (MODE = GND) or the self-programming mode (MODE = V+). In the self-programming mode, the CS7008 sequentially addresses an external ROM where filter coefficients are stored. The R/$\overline{W}$ pin is used to enable the ROM's outputs and an internally generated strobe clocks the data into the CS7008's registers.

In the self-programming mode, the CS7008 actually reads in the data three times and latches the data the third time. This feature was designed as an easy delay to avoid errors at power-on, when delays in power supplies getting to final levels could cause incorrect reads.

In the microprocessor mode, a microprocessor controls memory access. When R/$\overline{W}$ is at logic 0, data is clocked into the memory of the CS7008

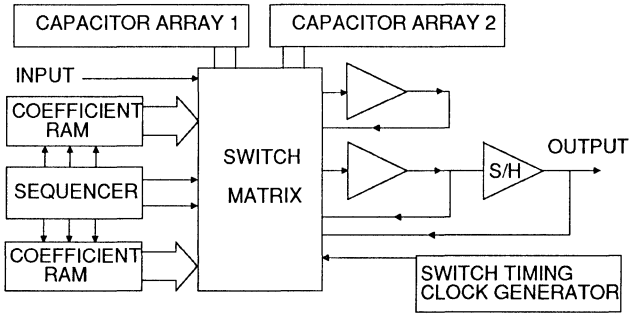


Figure 4. Block Diagram of a Single Biquad

on the negative transition of $\overline{CS}$ and is latched on the positive transition of $\overline{CS}$.

The CS7008 also has a readback feature that allows the user to read from the memory of the CS7008. This is accomplished by holding the read/write control pin, R/$\overline{W}$, at logic 1 and setting the chip select pin, $\overline{CS}$, to logic 0 as a strobe. Refer to the Timing Diagrams of Figure 2 for details. This feature is useful in calibration cycles for systems where verification is needed that sent and received data are the same.

Biquads

Each biquad consists of two capacitor arrays which are connected to two op amps through a series of switches, as shown by the block diagram in Figure 4. The capacitor coefficients determine the configuration of the capacitor array's switch matrix. As a signal is switched through a biquad, the desired value of capacitance is selected by the appropriate configuration of the switch matrix. After a charge has been switched through the selected capacitor, the capacitor array is grounded, discharging the array to prepare it for the next switch configuration.

Each biquad section is capable of implementing z-domain biquadratic transfer functions of the form:

$$H(z) = \frac{\gamma + \varepsilon z^{-1} + \delta z^{-2}}{1 + \alpha z^{-1} + \beta z^{-2}}$$

Equation 2

The circuit representing the general active-SC biquad used in the CS7008 is shown in Figure 3. The z-domain transfer function for this circuit is:

$$\frac{V_{out}}{V_{in}} = \frac{Az^{-1}(G-Hz^{-1}) + D(1-z^{-1})(I-Jz^{-1})}{Az^{-1}(C+E-Ez^{-1}) + D(1-z^{-1})(F+B-Bz^{-1})}$$

Equation 3

Note that Equation 3 is equivalent to Equation 2.

Equation 3 is solved to obtain the coefficients A through J. For optimal dynamic range, the signal level of both biquad op amps is important. Equation 4 gives the transfer function from the input to the output of the first op amp.

$$\frac{V'}{V_{in}} = \frac{(I-Jz^{-1})(C+E-Ez^{-1}) - (G-Hz^{-1})(F+B-Bz^{-1})}{Az^{-1}(C+E-Ez^{-1}) + D(1-z^{-1})(F+B-Bz^{-1})}$$

Equation 4

The dynamic range of both biquad op amps should be maximized by modifying the ratio of capacitor A to capacitor D so that the maximum voltage swing is achieved through the biquad (i.e., both op amps swing 5.5 V p-p, max).

Theoretically, capacitor groups C, D, E, G, H and A, B, F, I, J can be independently scaled without affecting the transfer function. In the CS7008, capacitors B and D are fixed at equivalent values of 1024; therefore, the two capacitor groups listed above must be normalized so that B and D are 1024. The remaining capacitors are programmed to 11 bit resolution allowing equivalent capacitor values to range from 0 to 2047.

If any of the equivalent capacitor values of the first group, (C, E, G, H), exceed the maximum value of 2047 when normalized, A can be scaled relative to D to achieve the transfer function. This dynamic range scaling causes V' (Figure 3) to increase with respect to V_{out}, so that gain in the first stage is greater than in the second stage. In this case, the input signal to the filter must be limited proportionately to prevent clipping at the output of the first op amp.

Figure 5 is an excerpt of Figure 3 showing the programmable capacitor A in detail. All of the programmable capacitors (A, C, E, F, G, H, and I) are of this form. The following illustrates how

to program a capacitor. In Figure 5, the numbers above the individual capacitors that make up A are the unit capacitor values (1024, 512, 256, etc.). The numbers below the capacitors are the individual bit positions (b10 = most significant bit, b0 = least significant bit). Figure 5 shows the switches programmed for a binary value of 10010001101 which, when adding the unit capacitor values, gives capacitor A the equivalent value of 1165 (= 1024 + 128 + 8 + 4 + 1). The equivalent value for a capacitor is the binary value, converted to decimal.

The 11 bit capacitor coefficients must be split into two bytes to load the CS7008. To load this capacitor, A, into biquad 1, the lower five bits, 01101 (decimal 13), would be loaded at address location 0 and the upper six bits, 100100 (decimal 36), would be loaded at address location 1. The Address Map in Table 1 lists all the address locations for all the capacitors in each biquad.

Possible configurations of the biquads in the CS7008 allow either E or F damping, and J or H input capacitors. Each biquad has a configuration byte, "conf", that determines how the memory locations E/F, CE/C, and J/H are to be used. The configuration codes and how they are used are shown in Table 3.

One biquad configuration requires additional consideration. If E damping is selected for a particular biquad, the value of the E capacitor must be added to the C capacitor for the biquad to function properly. For this case, the C capacitor is referred to as "CE", and is loaded into the memory location for CE/C (=CE). The value of the E capacitor must still be loaded into the E/F (=E) memory location. No special consideration is necessary for F damping, i.e., the values of C and F are loaded into locations for CE/C (=C) and E/F (=F) respectively. See Table 3 for more information on biquad configuration. More information regarding the transfer function in Equation 3 can be found in Chapter 6, section 6 of the text, "Modern Filter Design" by M. S. Ghausi and K. R. Laker, published by Prentice-Hall.

6

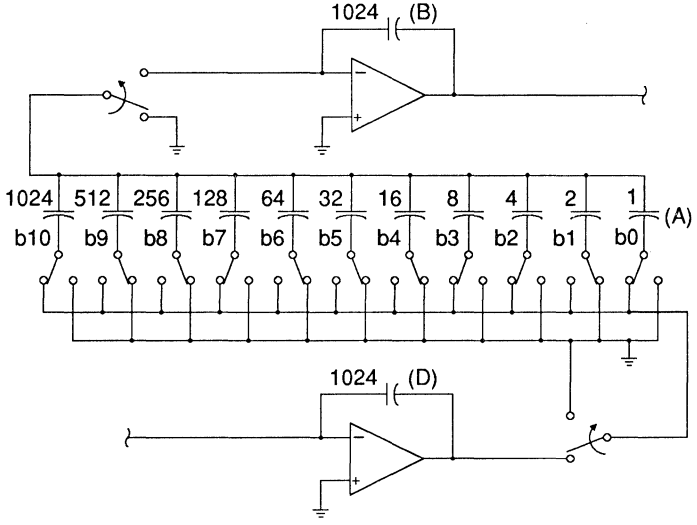


Figure 5. Equivalent Capacitor Arrangement

Cascaded Biquads (Biquad Arrangement Code)

The biquad sections can be cascaded allowing the user to define 2nd, 4th, 6th, or 8th order filters. Permissible biquad configurations are shown in Table 5. The biquad arrangement code, barr, is an 11 bit word which determines which biquad sections are connected between the analog input and the analog output, FOUT. The arrangement code is divided into two bytes located at address 62, barr-low byte, and 63, barr-high byte. Valid barr codes are given in Table 5. Basically, barr switches in 1, 2, 3, or 4 of the biquads as required by the filter implemented.

Certain filter implementations require biquad sections with gains exceeding unity. Excessive gain in one section could saturate the amplifiers, distorting the signal. In all cases, care must be taken in arranging biquad coefficient groups so signals do not clip. An example of this is a high Q, low-pass filter cascaded with a low Q, low-pass filter which has a lower cutoff frequency. In this situation, the biquad coefficient groups should be arranged so that the high gain of the high Q section(s) is preceded by the low Q, lower cutoff section(s) which attenuates the signal at those frequencies where gain is a problem in subsequent biquads. For filters of 6th order and below, the additional biquad(s) can be used in cascade for sin(x)/x compensation or phase linearization.

The typical performance curves on page 10-8 show how noise can vary depending on whether the high gain (High Q) biquad is before or after low gain biquads.

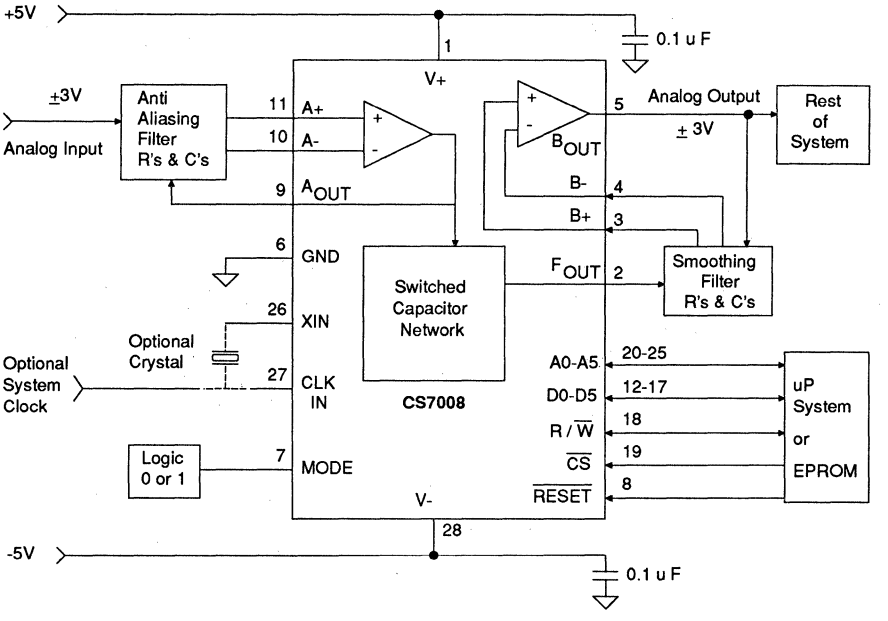


Figure 6. System Connection Diagram

Op Amps

Two op amps are provided in the CS7008. The output of op amp A is connected to the biquad filter input. This op amp must be used for signal input and can be configured for antialiasing and input gain. If no antialiasing or gain is needed, op amp A should be connected as a voltage follower. Op amp B is uncommitted and can be applied as the user wishes.

Power Supplies

Typical power supplies are V+ = +5 volts, V- = -5 volts and GND = 0 volts. Since the device's analog and digital grounds share the same pin, this pin should be isolated from all other digital grounds whenever possible, to prevent noise from interfering with the analog circuitry. Always decouple the V- and V+ power supply pins to the analog ground (GND) with 0.1 µF ceramic capacitors. These capacitors should be situated as close to the device as possible.

BASIC OPERATION

Figure 6 shows the basic connections for the CS7008. Minimal bypass decoupling is required, and we recommend 0.1 µF ceramic capacitors to ground, as close to the supply pins as feasible.

Op Amp A must be connected in the input stage. If no antialiasing of the input is required in a particular application, Op Amp A can be simply connected as a voltage follower.

Op Amp B may be used to filter, or smooth, the output of the switched capacitor filter. The output at Fout is a staircase shape, because of the sampling function inherent in this filter architecture. Using Op Amp B can filter out the high frequency components of the output at the transition steps.

In an application where the CS7008 is followed directly by an analog to digital converter, it may be preferable to not use Op Amp B, but to directly convert the sampled outputs at F_{out}. The limited drive capability of F_{out} may make it preferable to connect Op Amp B in a voltage follower configuration.

INPUT/OUTPUT AMP CONNECTIONS.

Figure 7 shows a simple Sallen and Key filter that can be implemented with Op Amp A for antialiasing or with Op Amp B for output smoothing. The specific resistors shown are those that are included on our CDB7008 evaluation board. This configuration yields a -3dB cut off of about 21 kHz, and provides adequate filtering in most applications with CS7008 sampling frequencies above 100 kHz.

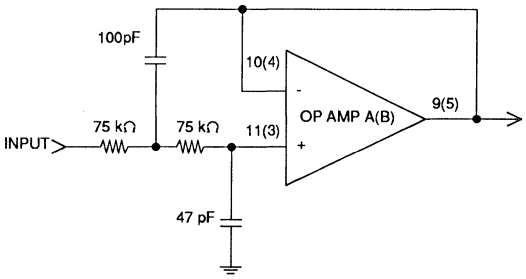


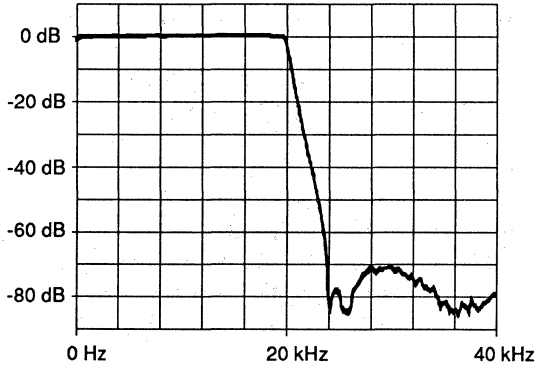
Figure 7. Typical Input/Output Amp Connections

TYPICAL CS7008 FILTERS

This section describes four typical filters implemented with the CS7008, showing the versatility and power of the part. All of these filters were developed using the CDS7000 Crystal ICE Filter Development System. The CS7008 uses the same output pin regardless of the filter type, unlike most switched capacitor filters. Switching from low-pass to band-stop is as simple as reprogramming the CS7008, with no changes needed in output pins or input attenuation.

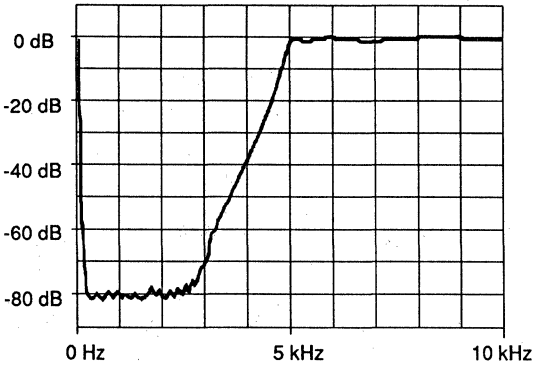
In the micro-processor mode on the CS7008, any complete filter can be loaded in 30µs. If the new filter to be implemented does not require changing every address in the CS7008, even less time is required to set up the new filter. Thus, in many systems where the CS7008 precedes an analog to digital converter, the filter can be changed between conversions, for real time adaptability.

Figures 8 to 11 were generated using a CS7008 in the CDB7008 evaluation board. The CDB7008 contains a CS7008 and a



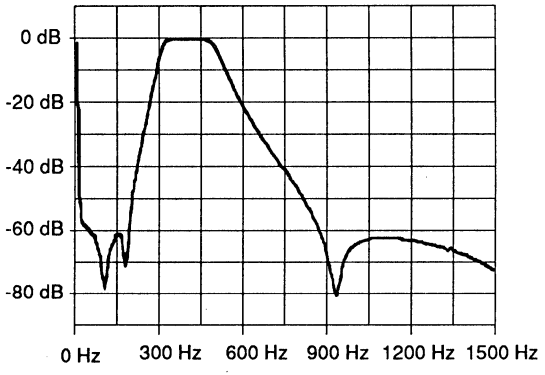
Inputs to Crystal ICE:			
TolC = 0.94406 (-0.5 dB)		TolR = 0.001 (-60dB)	
F1 = 20 kHz		F2 = 24 kHz	
Clkdiv = 2 (Clock = 3MHz)		Fs = 250 kHz	
Crystal ICE Outputs to CS7008 (Decimal):			
Biquad 1	Biquad 2	Biquad 3	Biquad 4
A = 351	A = 453	A = 465	A = 514
E = 344	E = 203	E = 177	E = 45
CE = 141	CE = 339	CE = 641	CE = 551
J = 19	J = 211	J = 496	J = 714
I = 19	I = 211	I = 496	I = 714
G = 133	G = 339	G = 464	G = 507
conf = 1	conf = 1	conf = 0	conf = 0
barr = 1317			
Q = 0.70	Q = 1.99	Q = 5.51	Q = 21.74

Figure 8. Low-Pass Elliptic Filter



Inputs to Crystal ICE:			
TolC = 0.89125 (-1.0 dB)		TolR = 0.001 (-60 dB)	
F1 = 3 kHz		F2 = 5 kHz	
Clkdiv = 8 (Clock = 3MHz)		Fs = 250 kHz	
Crystal ICE Outputs to CS7008 (Decimal):			
Biquad 1	Biquad 2	Biquad 3	Biquad 4
A =1430	A = 983	A = 600	A = 512
E = 585	E = 475	E = 213	E = 68
CE = 1438	CE = 825	CE = 762	CE = 569
J = 283	J = 1057	J = 881	J = 944
I = 283	I = 1057	I = 881	I = 944
G = 0	G = 0	G = 0	G = 0
conf = 0	conf = 1	conf = 0	conf = 0
barr = 1317			
Q = 0.75	Q = 1.96	Q = 4.27	Q = 14.13

Figure 9. High Pass Chebyshev I Filter



Inputs to Crystal ICE:			
TolC = 0.7071 (-3 dB)		TolR = 0.001 (-60 dB)	
F1 = 165 Hz		F2 = 300 Hz	
F3 = 500 Hz		F4 = 900 Hz	
Clkdiv = 64	(Clock = 3MHz)	Fs= 7.813 kHz	
Crystal ICE Outputs to CS7008 (Decimal):			
Biquad 1	Biquad 2	Biquad 3	Biquad 4
A = 335	A = 308	A = 402	A = 253
E = 487	E = 426	E = 184	E = 187
CE = 833	CE = 683	CE = 574	CE = 429
J = 122	J = 550	J = 32	J = 527
I = 122	I = 550	I = 32	I = 527
G = 200	G = 29	G = 133	G = 8
conf = 0	conf = 0	conf = 0	conf = 0
barr = 1317			
Q = 2.02	Q = 2.01	Q = 5.28	Q = 5.26

Figure 10. Band-Pass Chebyshev II Filter

preprogrammed ROM that includes 64 filters. A CDB7008 board is shipped with every CDS7000 Filter Development System, or it may be purchased seperately. All of the filters shown, with the exception of the low-pass elliptic filter, make use of the on-chip input antialiasing op amp and the output smoothing op amp.

Low-Pass Elliptic Filter

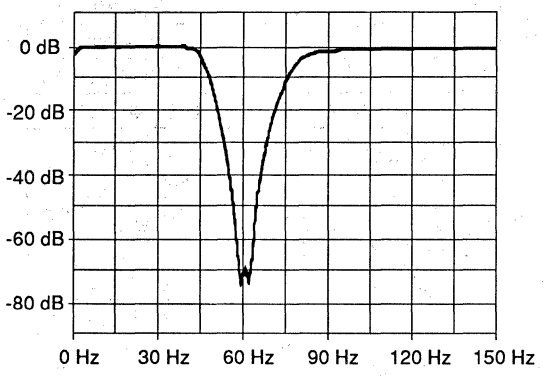
Low-pass filters are probably the most commonly used filters, often as antialiasing filters to reduce or eliminate frequency components at or above the Nyquist rate of an analog to digital converter system. A typical application using a 50kHz sampling A-to-D, with a Nyquist rate of 25kHz, requires that any frequency components at that frequency or above be attenuated before the signal is converted by the A-to-D to minimize aliasing.

Figure 8 shows the results of a low-pass elliptic filter using the CS7008. This filter exhibits passband ripple of less than 0.5dB, and has a cut-off frequency (-0.5dB point) of 20kHz. Stop-band attenuation, starting at 24kHz, is down at least 60dB. The results shown were achieved without using the input antialiasing op amp in the CS7008 (Op Amp A) or the output smoothing op amp (Op Amp B) because the design used in the CDB7008 would attenuate the corner of the elliptic low-pass. Using Op Amp A could increase attenuation at 24kHz, but would make it impossible to keep the cut-off frequency at 20kHz.

High-Pass Chebyshev I Filter

In some applications, users may want to reject input signals below a certain frequency that interfere with the frequency of interest. For example, harmonics are often small relative to the fundamental frequency, so that the fundamental needs to be attenuated to observe any harmonics generated by a system.

Figure 9 shows the results of programming the CS7008 as a high-pass filter, with a -1dB cut-off frequency of 5kHz, and with all inputs below 3kHz attenuated at least 60dB. This filter could



Inputs to Crystal ICE:			
TolC = 0.7071 (-3 dB)		TolR = 0.001 (-60 dB)	
F1 = 44 Hz		F2 = 57 Hz	
F3 = 63 Hz		Fs = 80 Hz	
Clkdiv = 128	(Clock = 800 kHz)	F4 = 1.042 kHz	
Crystal ICE Outputs to CS7008 (Decimal):			
Biquad 1	Biquad 2	Biquad 3	Biquad 4
A = 273	A = 413	A = 271	A = 493
E = 617	E = 498	E = 227	E = 205
CE = 980	CE = 870	CE = 511	CE = 650
J = 747	J =1162	J = 580	J =1654
I = 747	I =1162	I = 580	I =1654
G = 363	G = 372	G = 284	G = 445
conf = 0	conf = 0	conf = 0	conf= 0
barr = 1317			
Q = 1.81	Q = 1.81	Q = 4.51	Q = 4.50

Figure 11. Band-Stop Butterworth Filter

be useful in looking for harmonics generated by a 2.5kHz fundamental.

Band-Pass Chebyshev II Filter

Unlike many switched capacitor filters, the CS7008 can provide a band-pass filter implementation with a unity-gain transfer function at the center frequency. This means that the input amplitude does not have to be greatly reduced to prevent clipping of the signal, which in turn means that the dynamic range of the input is not reduced.

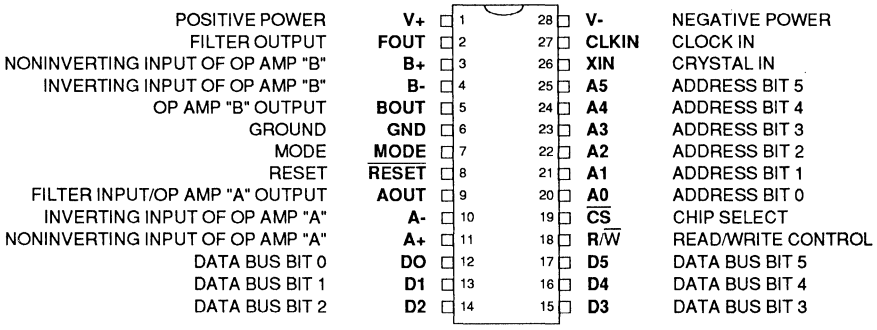
Figure 10 shows the results of programming the CS7008 to provide a band-pass filter with a center frequency at 400Hz. The -3dB cut-off frequencies are 300Hz and 500Hz, with input frequencies below 165Hz or above 900Hz attenuated by at least 60dB. With the flexibility to reprogram the CS7008 in a system, a series of such band-pass filters could be stored in system memory to allow the user to look at specific frequency bands, for example when doing vibration analysis.

Band-Stop Butterworth Filter

In the United States, 60Hz interference from AC lines is a standard problem to be overcome. In many other countries the problem frequency is 50Hz. The CS7008 can be used to notch out interference from either of these line frequencies, or many other sources of interference. By simply reprogramming the CS7008 from memory, it may be possible to make a universal system that can be easily plugged in anywhere in the world.

Figure 11 shows the results of programming a CS7008 to reject 60Hz interference. In this example, 44Hz and 80Hz are set as the -3dB frequencies, and any input components between 57Hz and 63Hz are attenuated by at least 60dB. The actual attenuation at 60 Hz is 71dB.

PIN DESCRIPTIONS



Power Supplies

V+ - Positive Power Supply, Pin 1

Most positive supply, typically +5 volts. Decouple with 0.1 µF ceramic capacitor to ground.

V– - Negative Power Supply, Pin 28

Most Negative Supply, typically -5 volts. Decouple with 0.1 µF ceramic capacitor to ground.

GND - Ground, Pin 6

Both analog and digital grounds are connected to this pin, which is typically held at 0 volts. This pin should be isolated from other digital grounds whenever possible to reduce noise in the analog circuits of the CS7008.

Oscillator

XIN, CLKIN - Oscillator Inputs, Pins 26 and 27.

A crystal connected across these pins sets the frequency of the internal oscillator. An externally generated clock may be connected to CLKIN, pin 27, which is CMOS compatible.

Op Amps

A– - Inverting Input of Op Amp A, Pin 10.

Inverting input of an op amp whose output is connected to the biquad filter input. This op amp is used to buffer signals to the CS7008 for filtering.

A+ - Noninverting Input of Op Amp A, Pin 11.

Noninverting input of an op amp whose output is connected to the biquad filter input. This op amp is used to buffer signals to the CS7008 for filtering.

AOUT - Output of Op Amp A, Pin 9.

This pin is also connected to the input of the biquad filter.

B– - Inverting Input of Op Amp B, Pin 4.

Inverting input of the uncommitted op amp.

B+ - Noninverting Input of Op Amp B, Pin 3.

Noninverting input of the uncommitted op amp.

BOUT - Output of Op Amp B, Pin 5.

Output of the uncommitted op amp.

Inputs

MODE - Pin 7.

Setting the CMOS compatible mode pin to V+ places the CS7008 in the self-programming mode. In the self-programming mode, the CS7008 executes an internal routine to read data from an external ROM upon power up or reset. Setting the mode pin to GND configures the CS7008 to be controlled by a microprocessor. In the self-programming mode (MODE = V+), the CS7008 goes through three complete read cycles on power up or reset, and latches data on the third read cycle.

$\overline{\text{RESET}}$ - Pin 8.

For normal operation, the $\overline{\text{RESET}}$ should be held at V+. Setting the $\overline{\text{RESET}}$ to GND will halt operation. If MODE = V+, the self-programming routine will be initiated when $\overline{\text{RESET}}$ returns to V+. If MODE = GND, normal operation will resume when $\overline{\text{RESET}}$ returns to V+. The filter function programmed into on-chip RAM is not affected by $\overline{\text{RESET}}$ when MODE = GND.

R/$\overline{\text{W}}$ - Read/Write Control, Pin 18.

A TTL compatible input/output used for memory access to the CS7008. When the CS7008 is in the microprocessor interface mode (MODE = GND), R/$\overline{\text{W}}$ serves as a write enable. When R/$\overline{\text{W}}$ is at a logic 0, data is clocked into the CS7008's memory on the negative transition of $\overline{\text{CS}}$, and is latched on the positive transition of $\overline{\text{CS}}$. Data can be read from the memory of the CS7008 by holding R/$\overline{\text{W}}$ at logic 1, and taking chip select, $\overline{\text{CS}}$, to logic 0.

In the self-programming mode (MODE = V+), R/$\overline{\text{W}}$ is used to enable the ROM's outputs and clock data into the CS7008's registers.

$\overline{CS}$ - Chip Select, Pin 19.

A TTL compatible input used for memory access. In the microprocessor interface mode (MODE = GND), $\overline{CS}$ goes low providing a strobe to clock data into the CS7008's data registers, provided R/$\overline{W}$ is at logic 0. Data is latched on the positive transition of $\overline{CS}$. The data bus is in a high-impedance state while $\overline{CS}$ is held high.

In the self-programming mode (MODE = V+), $\overline{CS}$ serves no function and should be tied to V+ with a 100 kΩ resistor. The necessary strobes are internally generated by the CS7008.

D0-D5 - Data Inputs, Pins 12 -17.

The data bus uses six pins, and is TTL compatible. It is bidirectional, allowing data to be transferred to and from memory. Pullup resistors must be used on the data pins if they are not continually driven (bus in high-impedance state). 20 kΩ resistors are adequate.

A0-A5 - Address Inputs, Pins 20 -25.

Six pins are used for the address bus, providing 64 TTL compatible addresses. This bus is bidirectional, allowing data to be written to the memory address specified on these pins when the CS7008 is in the microprocessor interface mode (MODE = GND). In the microprocessor mode pullup resistors must be used on the address pins if they are not continually driven (bus in high-impedance state). 20 kΩ resistors are adequate. In the self-programming mode, addresses are output to the external ROM.

6

Output

FOUT - Biquad Filter Output, Pin 2.

The filtered signal is reconstructed as a staircase waveform (100% duty cycle PAM), at the sampling frequency, f_S, and output at this pin.

Ordering Guide

Model	Temp Range	Package
CS7008-P	0° to 70°C	28-Pin Plastic DIP*
CS7008-ID	-40° to 85°C	28-Pin Hermetic Cerdip
CS7008-MD	-55° to 125°C	28-Pin Hermetic Cerdip

* A hermetic cerdip, designated CD7008-D, may be shipped in lieu of CS7008-P.

Semiconductor Corporation

CDS7000

CRYSTAL-ICE Filter Development System

Hardware Requirements:

- IBM PC or compatible with a minimum 256k of memory
- IBM high-resolution monochrome monitor or compatible
- Hercules monochrome graphics card or compatible
- 8087 math coprocessor

Software Requirements

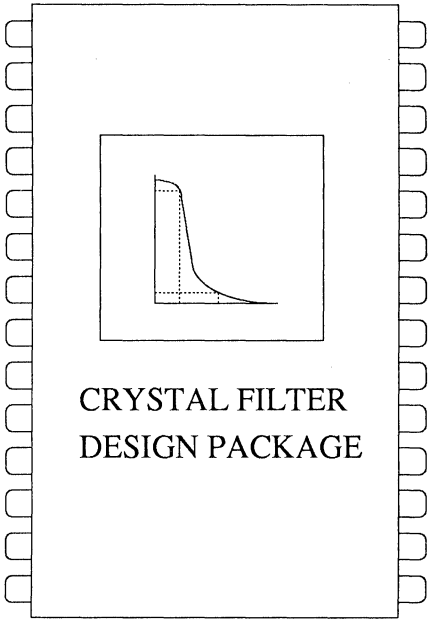
- PC-DOS or MS-DOS 2.1 or higher

General Description

The IBM PC based CDS7000, "Crystal-ICE" Filter Development System, consists of hardware and software which support filter development using the CS7008 Universal Filter. Crystal-ICE provides the designer with a quick and easy path from an initial understanding of a system's filtering requirements to a cost-effective hardware implementation of the needed filter. The menu-driven software supports filter synthesis from system specifications, direct entry of transfer functions, and filter modification at either the transfer function level or the circuit level. The in-circuit emulator (ICE) permits immediate feedback on the designed filter's performance in a system.

The CS7008 Universal Filter is fabricated in CMOS using Crystal's SMART *Analog*™ design techniques. It is a digitally configurable switched capacitor filter capable of providing virtually any audio-band, even-order filter response of eigth order or below.

ORDERING INFORMATION:CDS7000



Chapters 1 & 4 From the Crystal-Ice User's Manual

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

SECTION 1. - INTRODUCTION

The CRYSTAL-ICE Filter Development System from is a design tool which supports the CS7008 Universal Filter. The system features an In-Circuit Emulator or "ICE Probe", which will perform a specified filtering function in a circuit board designed to use the CS7008. The arduous mathematical effort required to design a filter is eliminated by using CRYSTAL-ICE. Filter transfer functions and the coefficients required to configure the CS7008 are generated by the filter development software provided with the system. Filter coefficients developed by the program are easily downloaded to the ICE Probe, which is plugged into the user's system or the CDB7008 evaluation board, where performance is evaluated. CRYSTAL-ICE makes it possible to design, test, and refine filters with unprecedented ease.

The CRYSTAL-ICE Filter Development System is shown in Figure 1-1. It consists of an ICE Probe, an interface system called the "ICE Box", interconnect cables, and the filter synthesis software. The ICE Probe contains a CS7008 and plugs directly into a 28 pin socket in the user's system or evaluation board. The analog pins of the CS7008 in the probe interface with the circuit board, while the address bus, data bus and control lines interface with the ICE Box. The ICE Box controls the interface between an IBM PC and the ICE Probe. The ICE Box accepts RS-232-C formatted data output from the COM port of the PC, converts it to the appropriate parallel format, and loads the CS7008 contained in the ICE Probe.

Filters are developed using CRYSTAL-ICE by responding to menus generated by the filter development software. The program will support design of low-pass, high-pass, bandpass, and band-stop filters. Each of these filter types can be implemented as Butterworth, Chebyshev I, Chebyshev II, or elliptic (Cauer) filter responses. The program generates even order filters up to eighth order, corresponding to the capabilities of the CS7008.

To design a filter, the user simply inputs the desired filter's channel objectives as prompted by the program, thereby defining a "Filter Template". The program calculates the z-domain biquadratic transfer functions for the selected filter implementation. The response of the filter developed by the program can be evaluated graphically by directing the program to display plots of decibels vs. frequency, magnitude vs. frequency, phase vs. frequency and pole-zero locations.

CRYSTAL-ICE can also display the z-domain biquadratic transfer functions. It is possible to modify these transfer functions, or enter new transfer functions, without using the filter synthesis portion of CRYSTAL-ICE. The transfer functions are used to calculate the normalized

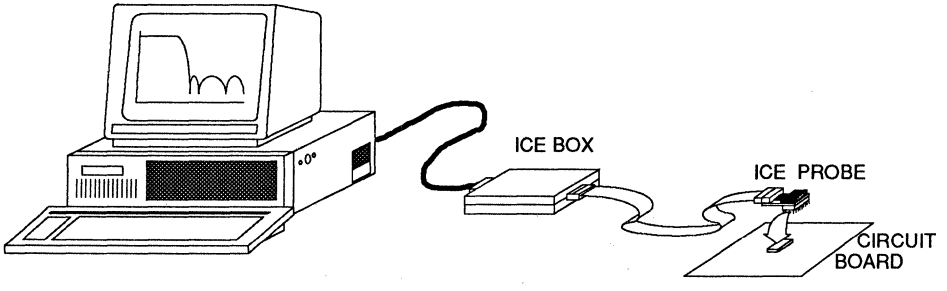


Figure 1-1. - Crystal-ICE Filter Development System

capacitor values which configure the CS7008. It is also possible to input and/or modify these capacitor values. The program will generate the CS7008 coefficients as well as the transfer function(s) that correspond to the capacitor values.

Once a desired filter response is obtained, all variables associated with that filter can be saved onto disk for later retrieval.

The CS7008 has two modes of operation. One mode allows a microprocessor to load the CS7008 coefficients, controlling its operation. In the second mode, the CS7008 reads coefficients directly from a user-defined memory upon power-up or reset. To support this mode, the CRYSTAL-ICE software can download coefficients directly to an EPROM Programmer via one of the COM ports on the PC.

The CRYSTAL-ICE software runs on an IBM PC or compatible, with a Hercules monochrome graphics card, an 8087 math coprocessor, an MS-DOS or PC-DOS operating system (version 2.1 or above), and a high-resolution monochrome monitor.

The ICE Box requires a +5 volt supply. The ICE Probe requires +5 and -5 volt supplies and a clock source which must be provided by the user's circuit board. This circuit board must also provide the analog interface for the CS7008. To assist the user in developing filters, a CDB7008 evaluation board is included with the ICE system. See Appendix C for more information on the CDB7008 evaluation board. If the CS7008 is removed from the CDB7008, and the ICE Probe inserted in its place, filters created by CRYSTAL-ICE can be immediately evaluated. The EPROM does not need to be removed since the ICE Probe doesn't connect any of the digital pins to the evaluation board. All other hardware and software required to implement a filter are provided with the ICE system.

1.1 In-Circuit Emulation and Interactive Design

The ICE Probe, which contains a CS7008, plugs into a 28 pin socket on a circuit board designed to accept the CS7008. The circuit board should include the analog interface for the CS7008, which consists of an antialiasing filter, a smoothing filter, an oscillator crystal or clock source, the signal inputs and outputs and the power supplies required by the CS7008. Directing the CRYSTAL-ICE program to load the CS7008 causes the coefficients generated by the program to be transferred to the CS7008 in the ICE Probe. Signals can then be applied to the circuit's inputs, and the performance of the filter in the circuit can be evaluated. Modifications to the filter response can be accomplished in minutes, and the results observed instantaneously. This iterative process can continue until the optimum filter response is achieved. The In-Circuit Emulator gives the designer the opportunity to evaluate all aspects of circuit performance before "freezing" a design.

CRYSTAL-ICE can also be used to develop coefficients for adaptive filter applications, since many different filters can easily be designed for a given system. Any filter supported by CRYSTAL-ICE can be generated in a matter of minutes.

Once the performance of a filter is satisfactory, the filter coefficients generated by CRYSTAL-ICE can be loaded into a (EP)ROM used to configure the CS7008 in its "self-program" mode, or stored in memory to be loaded into the CS7008 by a microprocessor.

The versatility of the CS7008 makes this development system very powerful. Literally millions of filters can be implemented using the CS7008 and the CRYSTAL-ICE system.

SECTION 4. - FILTER DEVELOPMENT

The CRYSTAL-ICE Filter Development software allows the user to design a filter by specifying a filter performance template. There are four kinds of filters supported by CRYSTAL-ICE: low-pass, high-pass, band-pass, and band-stop. CRYSTAL-ICE offers four possible implementations of these filters: Butterworth, Chebyshev I, Chebyshev II, and elliptic (Cauer). A synopsis of the features of these different filter implementations is given in the Filter Implementations section of Appendix A.

4.1 Using CRYSTAL-ICE to Design a Filter

Using CRYSTAL-ICE, a filter is designed by moving through a series of menus which allow the user to first specify a filter and then examine plots of the filter's theoretical performance. The main menus are arranged in the sequence shown in Figure 4-1. From each menu, select the desired item by typing the corresponding number and striking the Return key. The Back Space key can be used to delete an entry before striking the Return key. The ESCape key can be used in any menu, except the Filter Type menu, to regress one menu in the sequence. When in the Filter Template Menu or Filter Response Plots, the Tab key is used to move through the menu.

The Filter Type menu is the only menu from which the program can be terminated (to DOS). All other menus (except DOS Files and EPROM Programmer menus) allow you to return directly to the Filter Type menu to start a new filter design or terminate the program.

4.1.1 Printing Screens

There are two types of screens in the filter development software: text and graphics. The Filter Template and Filter Response Plots are graphics screens while all other screens are text. The "Print Screen" command shown on the filter response plots will cause a screen dump to occur. The software configures the PC to print graphics screens. If a print of a text screen is desired, the shift PrtSc key must be pressed and immediately followed by the ESCape key. If a graphics print has already started, pressing the ESCape key will stop the print.

4.2 Filter Type Menu

The first menu displayed by the program is the Filter Type menu, shown in Figure 4-2. To select the desired filter type, enter the corresponding number and hit the Return key. Notice that this menu provides direct access to the CS7008 Details menu. This allows those who have independently developed solutions for the biquad

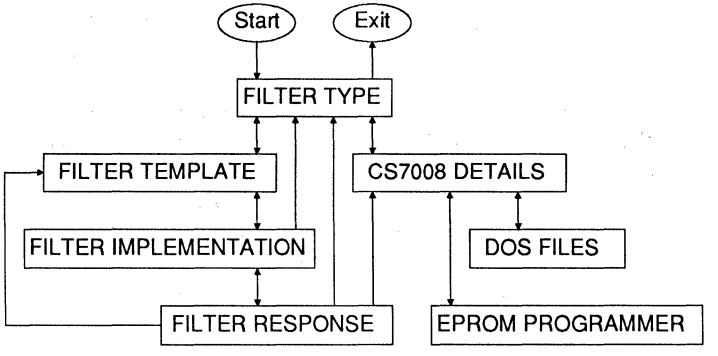


Figure 4-1. - Menu Arrangement

FILTER TYPE

1 - Low Pass
2 - High Pass
3 - Band Pass
4 - Band Stop
5 - CS7008 Details Menu
6 - Exit Program

Enter Selection:

Figure 4-2. - Filter Type Menu

equations or derived capacitor values to bypass the filter synthesis portion of the program. The use of the CS7008 Details menu for entering or changing filter parameters is described in greater detail in Section 6. When entering the CS7008 Details menu from the Filter Type menu, no calculations occur. If pre-calculated capacitor coefficients are desired, the CS7008 Details menu should be entered from the Filter Response menu.

4.3 Filter Template Menu

Once a filter type is selected, a diagram representing the filter type is displayed on the screen along with a list of parameters used to describe the filter's response. This is referred to as the Filter Template. The Filter Template for the low-pass filter, with all of the input options, is shown in Figure 4-3. The Tab key or Return key is used to enter new values or to move through the display if values already exist.

The first parameter entered is the scaling factor. The scaling factor determines whether frequencies used by the program will be input and displayed in hertz (select "H") or kilohertz (select "K"). When initially entered, the program will default to kilohertz if the Return or Tab key is struck. Once the scaling factor is entered, the remaining parameters required to specify a filter are displayed.

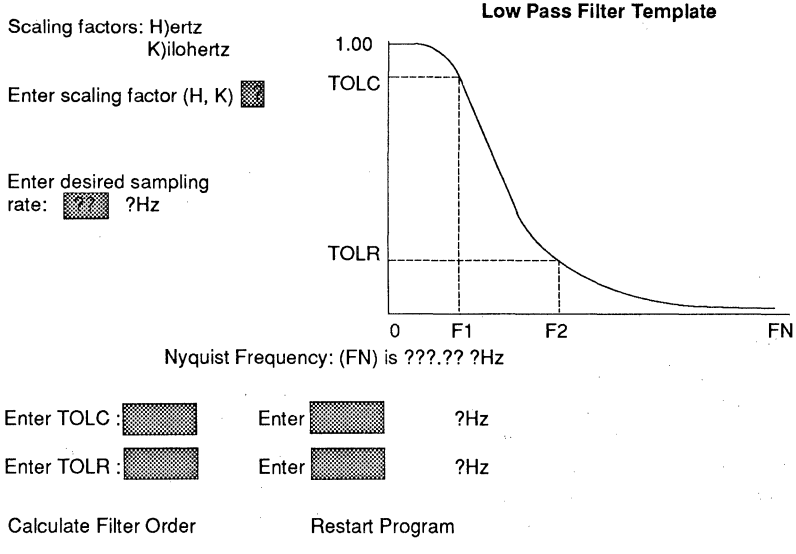


Figure 4-3. - Low Pass Filter Template

The next entry is the sampling rate. The sampling rate is determined by the oscillator or clock frequency input to the CS7008 and the clock divide code as given in Equation 1.

$$fosc = fs \times 6 \times CLKDIV$$

Equation 1.

When a sampling rate is entered, the program responds by displaying the Nyquist frequency. The Nyquist frequency equals one half of the sampling frequency (f_S), and is the highest frequency which can be filtered at the specified sampling rate. It is advisable to select a sampling frequency well in excess of the highest frequency of interest in the signal to be filtered. See Appendix A for more detailed information.

The filter's pass-band and rejection-band parameters are entered by specifying the cutoff- and rejection-amplitude tolerances, TOLC and TOLR, and their corresponding frequencies. TOLC and TOLR are entered in values normalized to one (i.e., these values must be less than 1, and greater than 0). If you prefer to think in decibels, the tolerances are easily converted from magnitude to decibels by using Equation 2.

$$TOL_{dB} = 20 \log_{10} TOL_{MAG.}$$

Equation 2.

The tolerances can be entered with resolutions to five digits to the right of the decimal point. Corner frequencies can be entered to accuracies of six significant digits. The maximum frequency entered must be less than the Nyquist frequency ($f_S/2$). If an inappropriate value is entered, the program will not accept the entry and will prompt you to enter a new value. The backspace key can be used while entering parameters to delete characters to the cursor's left.

Once all of the parameters have been entered, it is possible to modify any entry by using the Tab key to move through the display. The Tab key is also used to select the menu commands at the bottom of the display. The highlighted command is entered by striking the Return key. When a satisfactory set of parameters describing the filter template have been entered, select the "Calculate Filter Order" command. The program will determine the order required for each filter implementation, and display the Filter Implementation menu. An example is shown in Figure 4-4.

4.4 Filter Implementation Menu

```
                    FILTER IMPLEMENTATION
-------------------------------------------------------------
1 - Butterworth     EXCEEDS EIGHTH ORDER
2 - Chebyshev I     Order : 8
3 - Chebyshev II    Order : 8
4 - Elliptic        Order : 6
5 - Return to Filter Template
6 - Restart Program
Enter Selection:
```

Figure 4-4. - Filter Implementation Menu

If the filter order required for a particular implementation exceeds eight, the program will display "EXCEEDS EIGHTH ORDER" next to that filter implementation. If necessary, return to the Filter Template and change the parameters to reduce the filter order.

Selecting one of the filter implementations directs the program to calculate a z-domain transfer function for each biquad required. The program uses the transfer function to generate the plots offered on the Filter Response menu, which is shown in Figure 4-5.

4.5 Filter Response Menu

```
FILTER RESPONSE
---------------------------------------------
1 - Magnitude Plot
2 - Decibel Plot
3 - Phase Plot
4 - Pole-Zero Plot
5 - CS7008 Details Menu
6 - Return to Filter Template
7 - Return to Filter Implementation Menu
8 - Restart Program

Enter Selection:
```

Figure 4-5. - Filter Response Menu

From the Filter Response menu it is possible to return to the Filter Implementation menu to select a different implementation, or to go back to the Filter Template to change the filter's parameters. Each time the parameters are changed, the filter order and transfer functions are recalculated.

When viewing a plot, the Tab key is used to highlight the different menu items at the bottom of the screen such as "Modify Frequency Window" or "Print Screen". When the Return key is pressed, the highlighted menu item is entered. The graphs are plotted from 0 Hz to the Nyquist frequency (with the exception of the pole-zero plot). For filters with oversampling ratios which approach 20 (as recommended), the interesting portions of the plots occupy only a small portion of the whole plot. "Modify Frequency Window" allows expansion of any portion of the plot by reducing the range of frequencies plotted along the frequency axis. The beginning and ending frequencies for the plot, FLow and FHigh, can be specified, and those frequencies will be retained until a different filter template is specified.

Once the filter developed by the synthesis portion of the program is satisfactory, the next step is to calculate the actual capacitor values needed to configure the CS7008 and evaluate the in-circuit filter performance. To calculate the filter coefficients for the CS7008, select "CS7008 Details Menu" from the Filter Response menu. The program calculates the capacitor values and other information needed to configure the CS7008 from the transfer functions previously generated. Errors can occur when calculating capacitor values from ideal transfer functions. Some errors occur because the capacitor values required are larger than the permissible range of the CS7008 or the Q of the transfer function is excessively large. Appendix B, Section 3, describes these errors in detail. The above calculations will not occur when entering the CS7008 Details Menu from the Filter Type Menu.

4.6 CS7008 Details Menu

The CS7008 Details menu, shown in Figure 4-6, provides the capability to display and change both the coefficients of the filter transfer functions and the normalized capacitor values. The digital words used to configure the CS7008 can also be displayed. To load the digital words into the CS7008 on the ICE Probe, select "Load CS7008". This command directs the program to transfer its data to the ICE Box, which in turn loads the CS7008 in the ICE Probe. When downloading to the ICE Box, the ICE Probe must be powered or the following message will occur:

No Probe voltage sensed. Cannot download.
Press any key to continue

If this occurs, power up the ICE Probe and reselect "Load CS7008" from the CS7008 Details menu. Downloading should now work properly.

Item 3 on the CS7008 Details menu, View CS7008 Coefficients, displays the digital words (and corresponding addresses) for the capacitor

values shown in the Biquad Values menu. Data in the CS7008 Coefficients menu is formatted for the CS7008 as specified in the data sheet (Appendix D).

CS7008 DETAILS

1 - View H(z)
2 - View Biquad Values
3 - View CS7008 Coefficients
4 - Load CS7008
5 - EPROM Programmer
6 - DOS Files
7 - Restart Program

Enter Selection:

Figure 4-6. - CS7008 Details Menu

Select item 5 to download the filter data to an EPROM programmer. Item 6 allows the user to save or recall filter data from disk. Items 5 and 6 are explained in detail in Section 4.7 and 4.8 respectively.

With the exception of entering the clock divide code to be loaded into the CS7008, items 1 and 2 on the CS7008 Details menu are intended for individuals who are knowledgeable regarding switched capacitor biquad filters. The capabilities offered through items 1 and 2 are discussed in Section 6.

4.6.1 Changing the Clock Divide Code

The clock divide code is loaded into the memory of the CS7008, and determines the internal oscillator divide within the device. The clock divide code is initialized to a default value of one when the program is executed. It may be necessary to change the clock divide code depending on the particular application. For more information see the section on Oscillator, Sampling Frequency and Clock Divide in Appendix A.

To change the clock divide code, select "View Biquad Values". The Biquad Values menu displays the normalized biquad capacitor values for the specified filter. Select item 6 to change the clock divide. The program prompts you to enter the desired clock divide code. The clock divide codes that will be accepted by the CS7008 are 1, 2, 4, 8, 16, 32, 64, or 128. After the new clock divide code is entered, return to the CS7008 Details menu. Once changed, the clock divide code will remain at the selected value until a new value is entered by the user. Unless you intend to change the filter's transfer functions, be careful not to change any other parameter from this menu.

4.6.2 Suboptimal Dynamic Range Scaling

The transfer functions generated by the filter synthesis routines may require capacitors with normalized unit values exceeding 2047. In some cases it is possible to scale unit capacitor values and still achieve the desired filter. This capacitor scaling causes the gain through the affected biquad to increase. The maximum input signal to the filter must decrease to compensate for the gain. This process reduces the CS7008's dynamic range, which is why it is referred to as suboptimal dynamic range scaling.

Not all capacitors can be scaled. When possible, the filter development program will automatically scale capacitors, up to the point where the input is reduced to 5% of the maximum input voltage swing for the CS7008. When dynamic range scaling of capacitors in a biquad occurs, a warning is issued as shown in Figure 4-7. This warning directs the user to limit the dynamic range of the input signal by a specified amount.

**** Input Voltage Range reduced to 85% of maximum value. ****
Press any key to continue

Figure 4-7. - Input Voltage Reduction Warning

If more than one biquad requires dynamic range scaling, additional warnings will be issued. The input signal's voltage range should be limited to the smallest of the percentages displayed. The smallest percentage will be displayed at the top of the Biquad Values menu.

4.7 EPROM Programmer Menu

The CS7008 has two modes of operation. One mode will allow a microprocessor to load CS7008 coefficients, and thereby control its operation. In the other, a self-programming mode, the CS7008 will read coefficients from memory upon power-up or reset. To facilitate the use of this mode, the CRYSTAL-ICE Filter Development software supports downloading to an EPROM programmer via one of the COM ports on the PC. The EPROM programmer must support RS-232-C communications and either Intel Hex or Motorola S-Record data formats.

```
Format: Intel Hex                    Port: COM2
 BAUD: 1200    Data Bits: 7    Parity: Even    Stop Bits: 2

Start Address: 0          (0x0)

        :10000000000000000000000000000000000000000000F0
        :1000100006110611180301000B010B0118030100062
        :10002000140A040A1C0401001105110510C04000037
        :100030001F05150E021500000B070B070D062814EF
        :0000001FF

                              EPROM PROGRAMMER
                              ----------------------------------

                              1 - Load Programmer
                              2 - Change Start Address
                              3 - Change Port Parameters
                              4 - Return to CS7008 Details Menu

Enter Selection:
```

Figure 4-8. - EPROM Programmer Menu

The user must supply the cable to interface the PC and EPROM programmer. Section 3.3 lists the specifications for this interface cable.

The EPROM Programmer menu is accessed from the CS7008 Details menu and is shown in Figure 4-8. The default port parameters are listed on the top two lines of the screen. The filter coefficients are loaded into 64 successive locations with the start address being the first of the 64 locations. The lines between the start address and the menu contain the actual records to be downloaded.

4.7.1 Loading the EPROM Programmer

If item one, Load Programmer, is selected, the software will attempt to send the data through the COM port (listed at the top of the screen) to the programmer. If the attempt is unsuccessful, one of the following messages will appear:

COMx not responding (DSR inactive)
Press any key to continue

or:

COMx not responding (Time Out)
Press any key to continue

where x in COMx designates the port used. If either of these messages appear, verify that the EPROM programmer is powered, connected to that particular COM port, and waiting for data to be downloaded. See Appendix B, Section 4 for more information on these two errors.

If the EPROM programmer signals an error while downloading, verify that the port parameters displayed at the top of the screen are the same as the EPROM programmer's parameters.

4.7.2 Changing the Start Address

Item two from the menu, Change Start Address, allows the filter coefficients to be loaded into any set of adjacent addresses in the EPROM. Once "Change Start Address" is selected, a new address must be entered in decimal notation. The Tab key may be used to increment one filter length (64 bytes). Pressing the Return key enters the address and updates the records to reflect the new address.

4.7.3 Changing Port Parameters

Using menu item three, Change Port Parameters, almost any aspect of the port can be modified to suit the EPROM programmer used. Any modified parameter will remain in effect until the program is exited. When "Change Port Parameters" is selected, the bottom line of the screen will change as shown in Figure 4-9, and an enlarged cursor will blink to the right of the first parameter. The Tab key will change the value to the left of the cursor.

```
Format: Intel Hex          Port: COM2
 BAUD: 1200   Data Bits: 7   Parity: Even   Stop Bits: 2

Start Address: 0          (0x0)

        :10000000000000000000000000000000000000000000F0
        :1000100006110611180301000B010B0118030100062
        :10002000140A040A1C040100110511051C04000037
        :100030001F05150E021500000B070B070D062814EF
        :0000001FF
                          EPROM PROGRAMMER
                        ----------------------------
                        1 - Load Programmer
                        2 - Change Start Address
                        3 - Change Port Parameters
                        4 - Return to CS7008 Details Menu

<CR> - Save Value      <Tab> - Change Value      <ESC> - Exit
```

Figure 4-9. - Changing Port Parameters

Use the Tab key to "roll" through the available values until the appropriate one is displayed. Pressing the Return key (CR) will save the value and move the cursor on to the next parameter. The ESCape key will immediately cause an exit back to the initial EPROM Programmer menu. The parameter selected when the ESCape key is pressed will not retain a changed value (the Return key must be used first).

If the modified COM port parameter is the same as that of the ICE Box, then the cable for the EPROM programmer must replace the ICE Box cable on the PC. Before leaving the EPROM Programmer menu, the ICE Box must be reconnected to the COM port. In this instance, the following message will appear as a reminder:

ICE Box must be reconnected to COMx
Press any key to exit

where x in COMx indicates the port number. Below is a list of the port parameters with all their possible values:

Format: Intel Hex
Motorola S-Record

Port:
COM1
COM2
COM3*
COM4*

*IBM BIOS only supports two COM ports. If COM3 or COM4 exist, they must be BIOS compatible.

Baud:
150
300
600
1200
4800
9600

Data Bits:
7
8

Parity:
None
Even
Odd

Stop Bits:
1
2

4.8 DOS Files Menu

Once a desired filter is obtained, all the variables associated with that filter can be saved onto disk for later retrieval. The DOS Files menu is shown in Figure 4-10 and is accessed from the CS7008 Details menu. The top line on this screen displays the present working directory. The next line displays the most recent file read from or saved to disk. The file name will disappear if a new filter is calculated using the synthesis portion of the program. If no extension is given when reading from or saving to disk, a ".UF" is assumed.

Directory - C:\FILTER
File Name -

DOS FILES

1 - Read File
2 - Save File
3 - Change Directory
4 - Return to CS7008 Details Menu

Enter Selection:

Figure 4-10. - DOS Files Menu

4.8.1 Reading Files

When reading a file from disk, the program will prompt the user for a filename. Filenames must adhere to DOS standards. DOS device names may not be used for filenames. Consult the DOS manual for filename specifications. Errors can occur because of the following:

invalid disk specifier
invalid path specifier
invalid filename
file not found
invalid format in file

All errors are discussed in detail in Appendix B, Subsections 5 and 6.

4.8.2 Saving Files

When saving a file to disk, the program will prompt the user for a filename. In choosing the filename, the user must follow the same conventions as when reading files from disk. Errors can occur because of the following:

invalid disk specifier
invalid path specifier
invalid filename

Errors are discussed in detail in Appendix B, Subsections 5 and 6. If the file specified already exists, the program will ask for verification before replacing it.

4.8.3 Changing Directories

Changing the present working directory will allow a more orderly file structure since different filter projects may be kept in different directories. When changing directories, the new directory must already exist. New directories should be created using DOS prior to executing the CRYSTAL-ICE software. Changing directories will also allow changing disk drives. If no directory is given when changing drives, the current

directory for that particular drive is used. DOS remembers the current directory for each drive. The following errors can occur when changing directories:

invalid disk drive specifier
invalid path specifier

All errors are explained in detail in Appendix B, Subsections 5 and 6.

4.9 Menu Paths

Figures 4-11 thru 4-15 depict the possible paths from each of the main menus in the filter development program. These figures are intended to serve as a handy reference for understanding the menu structure used in the CRYSTAL-ICE filter development software.

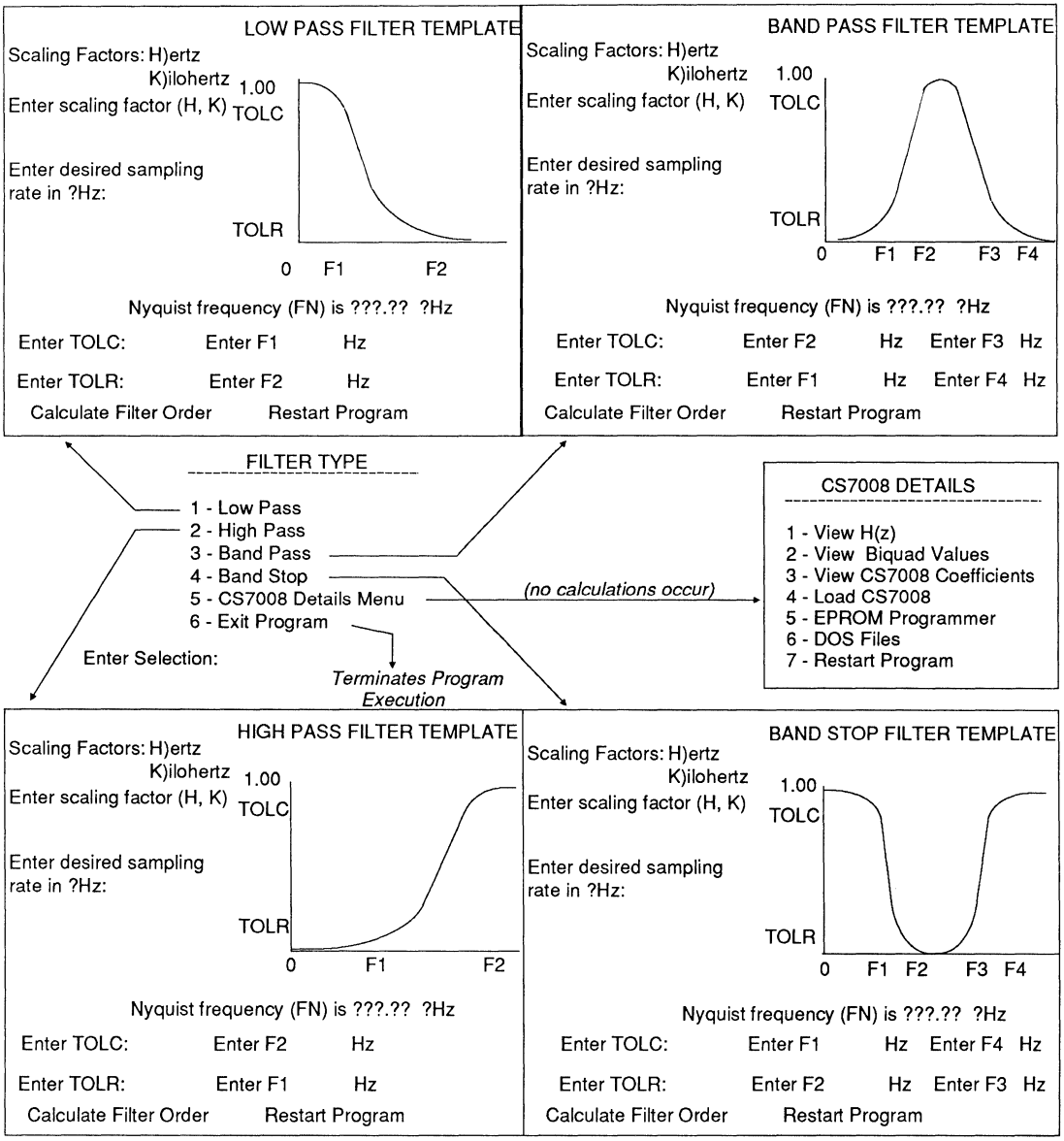


Figure 4-11. - Filter Type Menu Paths

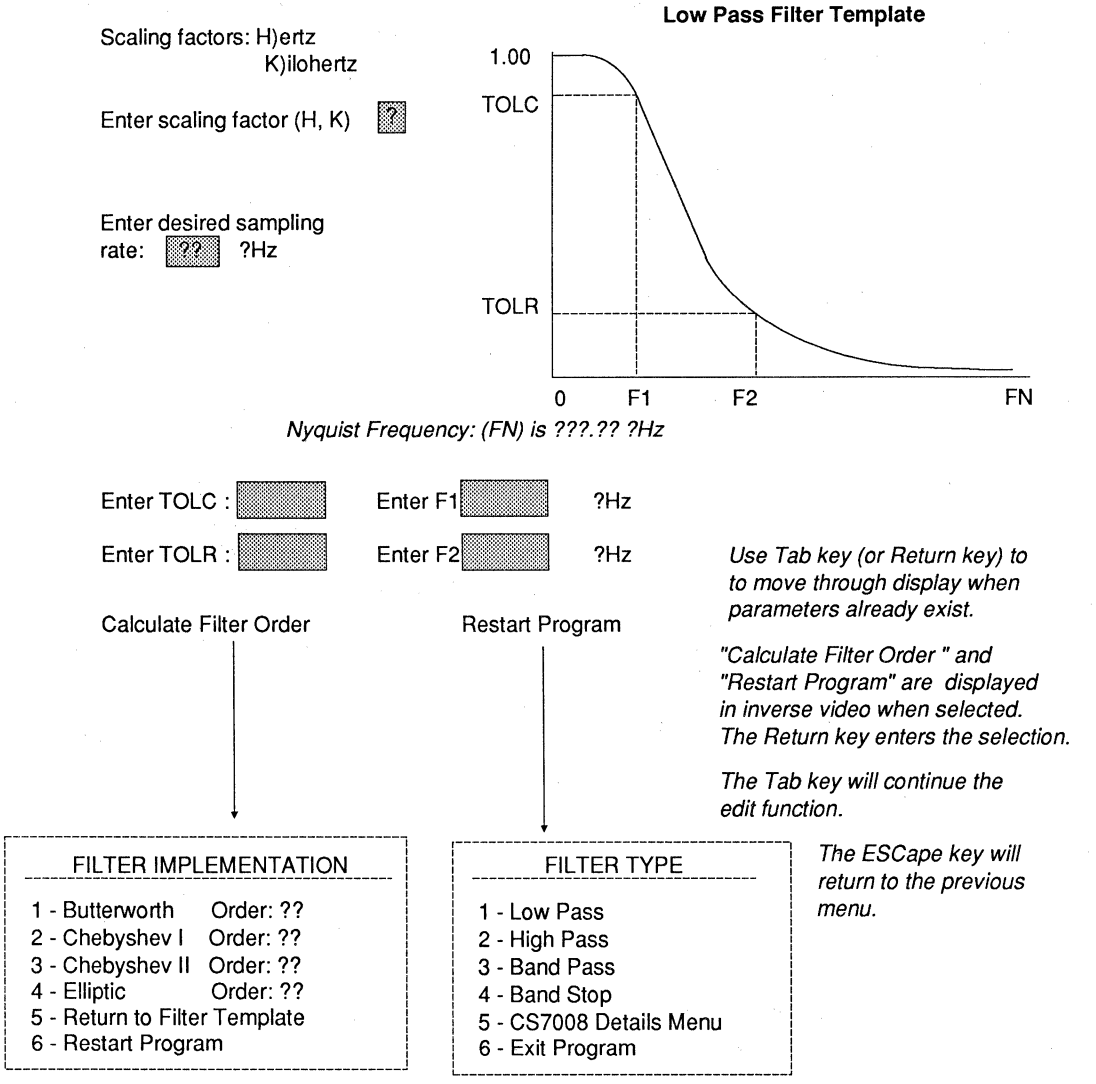


Figure 4-12. - Filter Template Paths

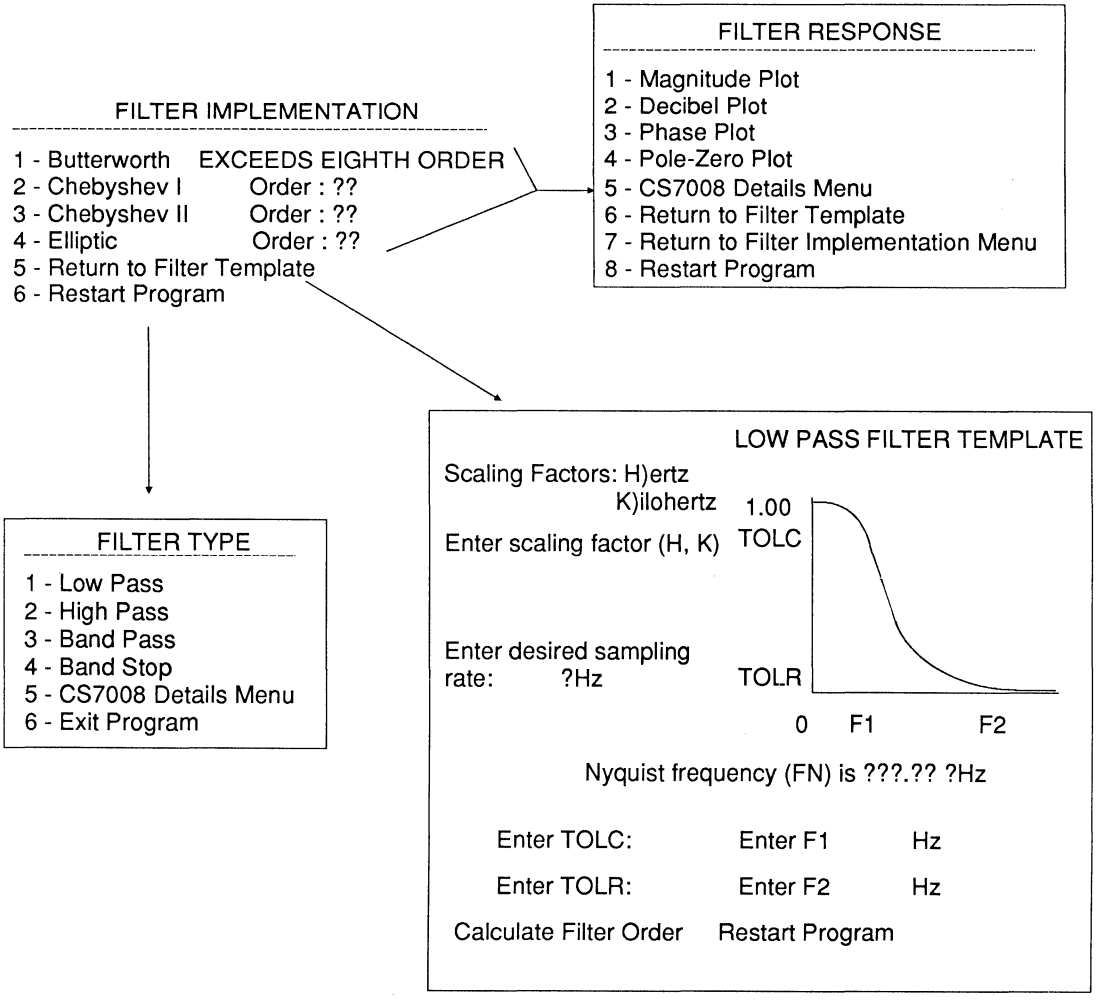


Figure 4-13. - Filter Implementation Menu Paths

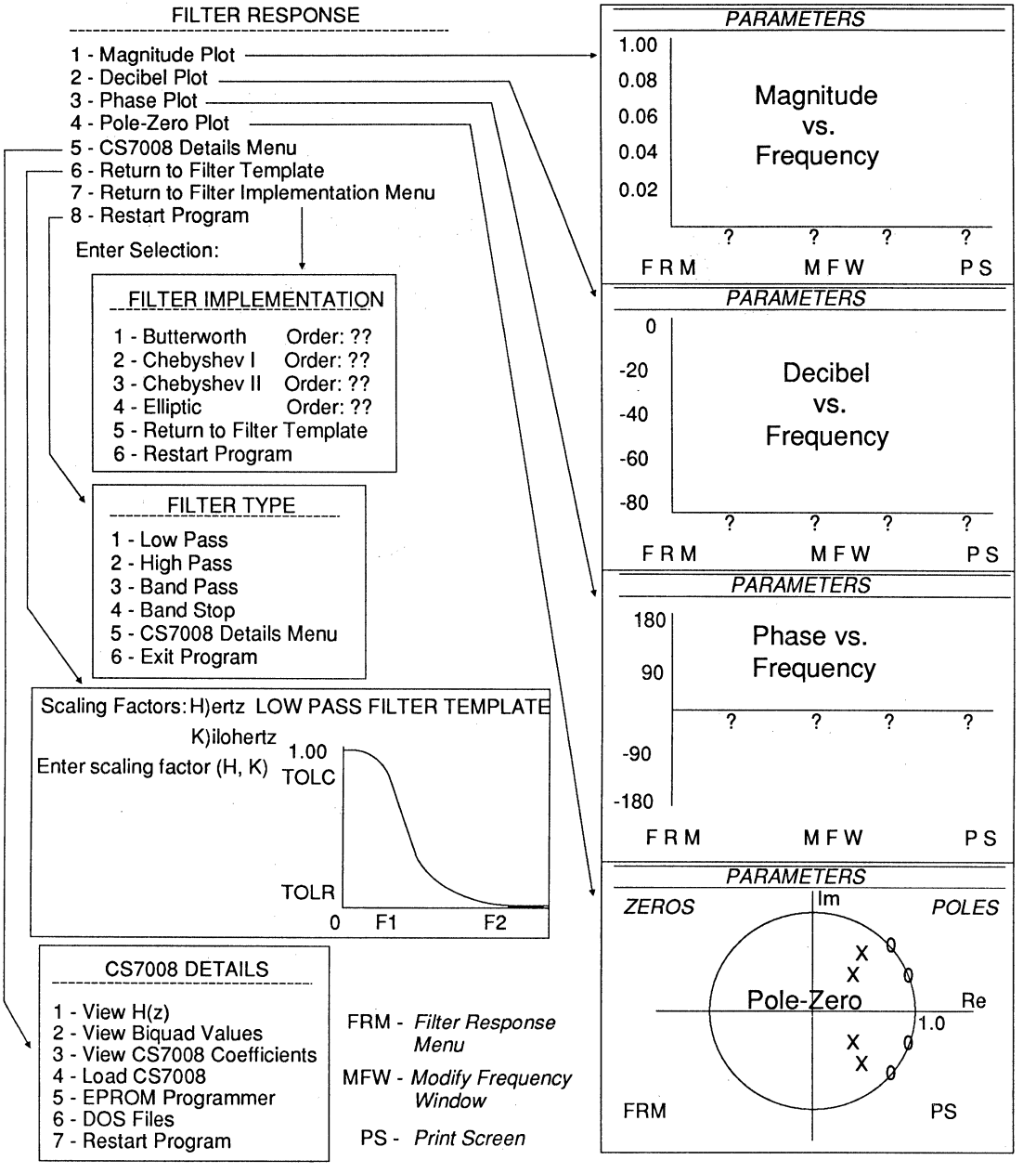


Figure 4-14. - Filter Response Menu Paths

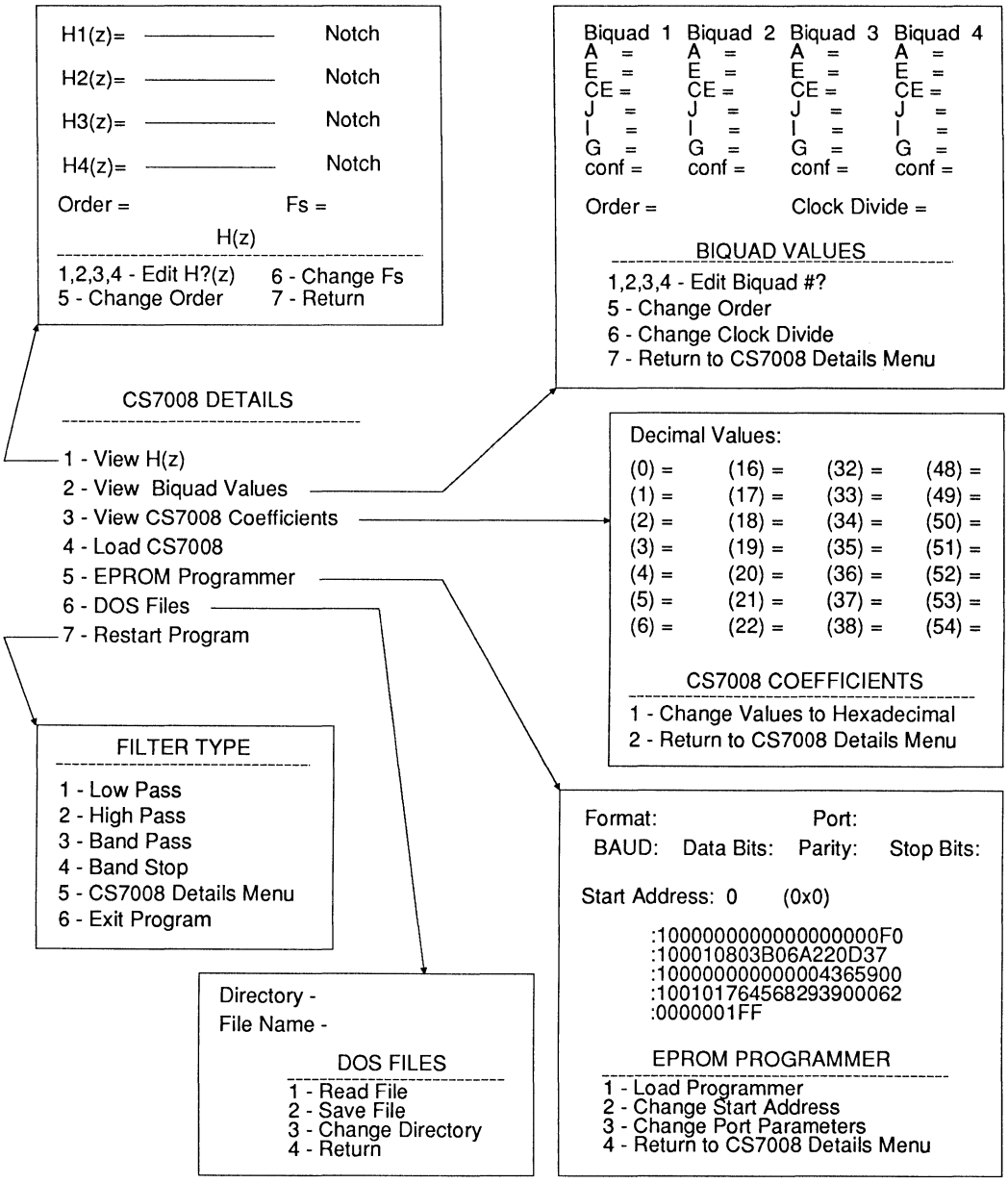


Figure 4-15. - CS7008 Details Menu

• Notes •

INTRODUCTION

Crystal offers two voltage references which complement our A/D converters. Designed to operate with the CS5412 12-bit 1MHz ADC, the CS3901 produces a stable, buffered ±1.5V and +3.0V. Particularly suitable for Crystal's successive approximation A/D converters, the CS3902 produces a very stable and accurate +4.5V

USER'S GUIDE

Device:	CS3901	CS3902
Output Voltage	±1.5 V, +3.0 V	+4.5 V
Input Voltage	± 5.0 V	+11 to +22 V
Tempco	-	±0.5 ppm /°C
Package	14 pin DIP	14 pin DIP

CONTENTS

Semiconductor Corporation

CS3901

± 1.5 V and 3.0 V Voltage Reference

Features

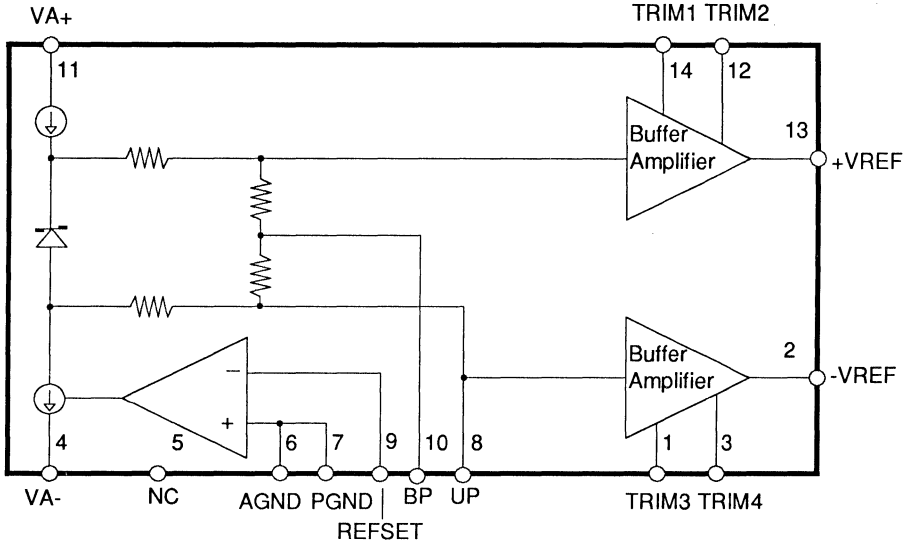
- High Accuracy
- Low Drift
- Excellent Stability
- Operates from ±5V
- + 3.0V or ± 1.5V outputs, jumper selectable
- Small package size - 14 Pin DIP

General Description

The CS3901 is a precision hybrid voltage reference for the CS5412 A/D Converter. The device offers jumper-selection options to provide either +3.0V or ± 1.5V outputs from ± 5V inputs. The voltage outputs do not require trimming, but trim pins are available if fine adjustments are desired. The outputs of the CS3901 provide low impedance, low noise and excellent temperature stability to insure optimum performance from the A/D converter. The unit is also compatible with other A/D converters where +3.0V or ±1.5V reference voltages are required.

ORDERING INFORMATION:

CS3901 - KC	0 °C to 70 °C
CS3901 - TC	- 55 °C to +125 °C



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Preliminary Product Information | This document contains data for a product under development. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25°C, VA+= 5V, VA- = -5V, VREF outputs unloaded)

Parameter	CS3901-K min	CS3901-K typ	CS3901-K max	CS3901-T min	CS3901-T typ	CS3901-T max	Units
Specified Temperature Range	0	–	70	−55	–	125	° C
Supply Voltage							
VA+	+ 4.85	+ 5.0	+ 5.5	+ 4.85	+ 5.0	+ 5.5	V
VA-	− 5.5	− 5.0	− 4.85	− 5.5	− 5.0	− 4.85	V
+VREF Voltage (REFSET = UP)		+ 3.0			+ 3.0		V
Deviation from +3.0V:							
at Ta = 25 °C	−350		+ 350	−350		+ 350	uV
at Ta = Tmin to Tmax	−700		+ 700	−700		+ 700	uV
+VREF Voltage (REFSET = BP)		+ 1.5			+ 1.5		V
Deviation from +1.5V:							
at Ta = 25 °C	−175		+ 175	−175		+ 175	uV
at Ta = Tmin to Tmax	−350		+ 350	−350		+ 350	uV
-VREF Voltage (REFSET = BP)		−1.5			−1.5		V
Deviation from -1.5V:							
at Ta = 25 °C	−175		+ 175	−175		+ 175	uV
at Ta = Tmin to Tmax	−350		+ 350	−350		+ 350	uV
Output Trim Range		± 5			± 5		mV
Output Impedance (Note 1)							
dc to 1000 Hz			10			10	milliohms
Output Noise dc to 1 MHz			100			100	uV (p-p)
Output Drive (Note 2)	5			5			mA
PSRR VA+ or VA- (Note 3)	70			70			dB
Long-Term Stability		25			25		ppm/1000 hr
Supply Current							
V+		+ 8	TBD		+ 8	TBD	mA
V-		− 8	TBD		− 8	TBD	mA

Note: 1. The output impedance at high frequencies will be dictated by the capacitors added external to the reference package.
2. The outputs are short circuit protected.
3. Tested with 100 mV_{P-P} 120 Hz applied to each supply input separately.

Specifications are subject to change without notice.

THEORY OF OPERATION

The CS3901 is a hybrid precision voltage reference circuit which uses a very low drift zener diode as a reference. The zener is biased with current sources at both anode and cathode to allow a "floating" reference. A resistor divider network is connected in parallel with the floating zener. Two tap points on the resistor network are made available at the pins of the device. Connecting either one of these tap points to the reference set (REFSET) pin of the device will cause the floating zener to establish an output voltage from the device.

Bipolar Output Configuration (±1. 5 V outputs)

When tap point BP (for bipolar) at pin 10 is connected to the REFSET pin, the floating zener and resistor divider network establish output voltages of +1.5 V at +VREF and -1.5 V at -VREF (see Figure 1 for the bipolar system connection). The hybrid contains amplifiers to buffer the resistor network divider voltages. The buffer amplifiers are capable of driving up to 5 mA minimum and of being loaded with up to 15 µF of capacitance without stability problems. The buffer output voltages do not require trimming but are trimmable if a 10k potentiometer is appropriately connected to the trim pins. The wiper of the pot should be connected to the -5 V supply. TRIM1 and TRIM2 are for trimming the positive output voltage. Moving the wiper of the pot toward TRIM2 will cause the positive output to increase in magnitude. TRIM3 and TRIM4 are for trimming the negative output voltage. Moving the wiper of the pot toward TRIM3 will cause the negative output to increase in magnitude.

Unipolar Output Configuration (+3.0 V output)

When tap point UP (for unipolar) is connected to the REFSET pin the floating zener and resistor divider network establishes an output voltage of +3.0 V at the +VREF output (see Figure 2 for unipolar connection). The -VREF output should be left disconnected when the device is configured to output +3.0 V.

Power Supply Connection

The CS3901 is designed to operate from ±5 V supplies. These inputs should be decoupled with 0.1 µF ceramic capacitors located near to the part. The PGND (power ground) pin is to be used for the power supply ground return. This pin is internally connected to the AGND (analog ground) pin.

CS3901/CS5412 System Combination

The CS3901 is designed to be used with the CS5412 A/D converter. The CS5412 A/D converter draws a high frequency dynamic current from the CS3901 outputs. To maintain low output impedance at high frequencies, the reference outputs from the CS3901 should be bypassed to AGND with a parallel combination of a 0.1 µF ceramic capacitor and a 3.3 µF tantalum capacitor. The capacitors should be located as near to the A/D converter input reference pins as possible. The AGND pin should be connected to the AGND pin of the A/D converter.

Care should be exercised in the selection of the tantalum capacitor in the output filter. It should be chosen to maintain a minimum of 3.3 µF over the operating temperature range in which you use the device. This will insure maximum performance from the CS5412 A/D converter.

A single CS3901 is capable of being used to supply reference voltages to several CS5412 A/D converters. If this is done the value of the capacitance on the VREF outputs of the reference needs to be increased accordingly. The buffered outputs of the CS3901 can be loaded with up to 15 µF of capacitance without causing stability problems.

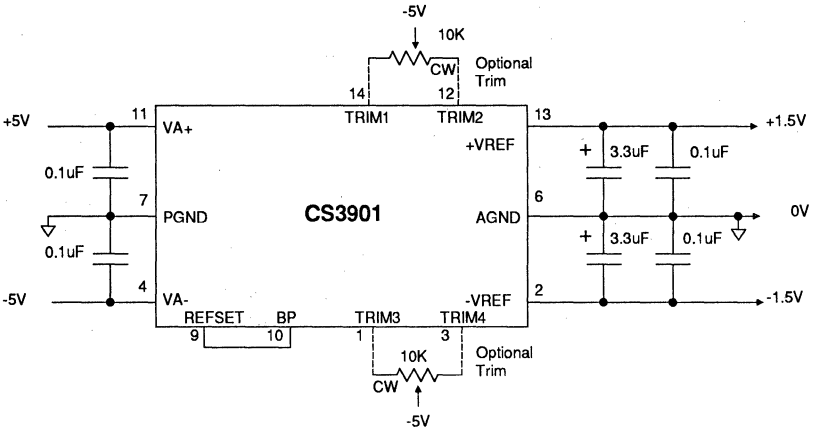


Figure 1. Bipolar Output Configuration

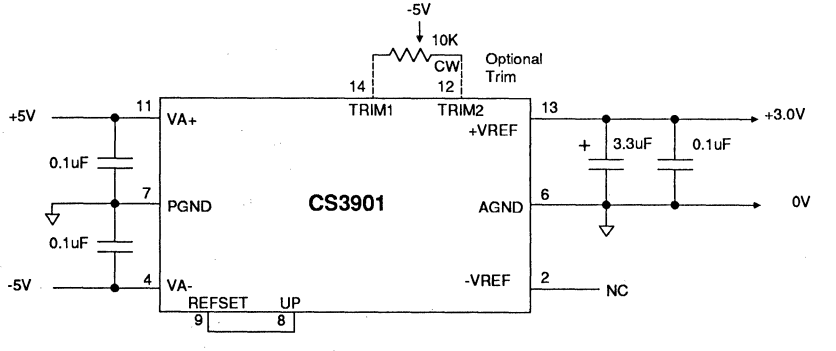
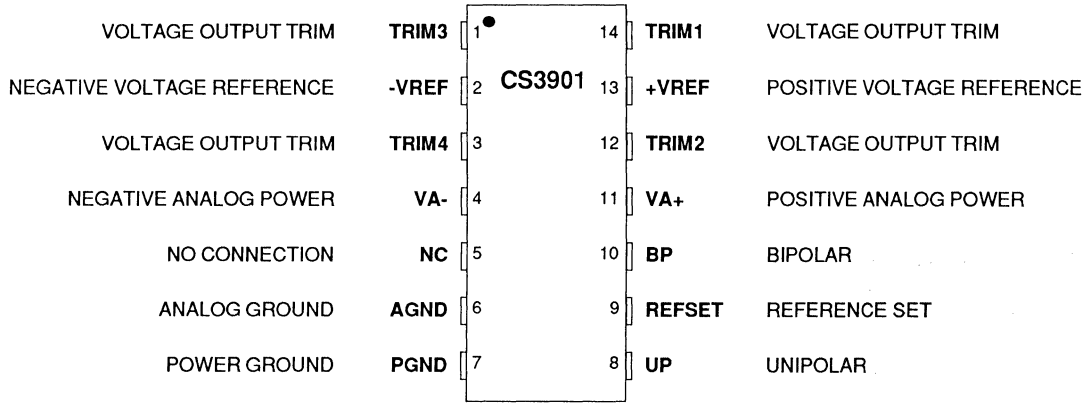


Figure 2. Unipolar Output Configuration

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 11

Positive analog power supply, nominally +5 V.

VA- - Negative Analog Power, PIN 4

Negative analog power supply, nominally -5 V.

PGND - Power Ground, PIN 7

The ground pin for the VA+ and VA- inputs. It is internally connected to AGND.

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Reference Control Pins

REFSET - Reference Set, PIN 9

This is a virtual ground node to which either the BP (bipolar) or the UP (unipolar) tap of the floating zener resistor divider network is connected to establish the appropriate output voltage from the reference.

BP - Bipolar, PIN 10

The BP (bipolar) pin provides access to a resistor network divider tap point on the floating zener reference. When the BP pin is connected to the REFSET pin the CS3901 will establish +1.5 V at the +VREF pin and -1.5 V at the -VREF pin.

UP - Unipolar, PIN 8

The UP (unipolar) pin provides access to a resistor network divider tap point on the floating zener reference. When the UP pin is connected to the REFSET pin the CS3901 will establish +3.0 V at the +VREF pin.

Reference Output Pins

+VREF - Positive Voltage Reference output, PIN 13

Provides a positive output reference voltage with respect to the AGND pin. The magnitude can be either +1.5 V in the bipolar reference mode or +3.0 V in the unipolar reference mode.

-VREF - Negative Voltage Reference output, PIN 2

Provides a negative output reference voltage with respect to the AGND pin. The magnitude is -1.5 V in the bipolar reference mode. The pin should be left disconnected when the CS3901 is used in the unipolar reference mode.

AGND - Analog Ground, PIN 6

Analog ground node for the voltage reference outputs. Connection should be made between this pin and the analog ground of the A/D converter.

Reference Trim Pins

TRIM1 - Voltage Output Trim, PIN 14

TRIM1 works in conjunction with TRIM2 to allow adjustment of the +VREF output voltage.

TRIM2 - Voltage Output Trim, PIN 12

See definition for TRIM1.

TRIM3 - Voltage Output Trim, PIN 1

TRIM3 works in conjunction with TRIM4 to allow adjustment of the -VREF output voltage.

TRIM4 - Voltage Output Trim, PIN 3

See definition for TRIM3.

Miscellaneous

NC - No Connection, PIN 5

Should be left unconnected.

Semiconductor Corporation

CS3902

+ 4.5V Precision Voltage Reference

Features

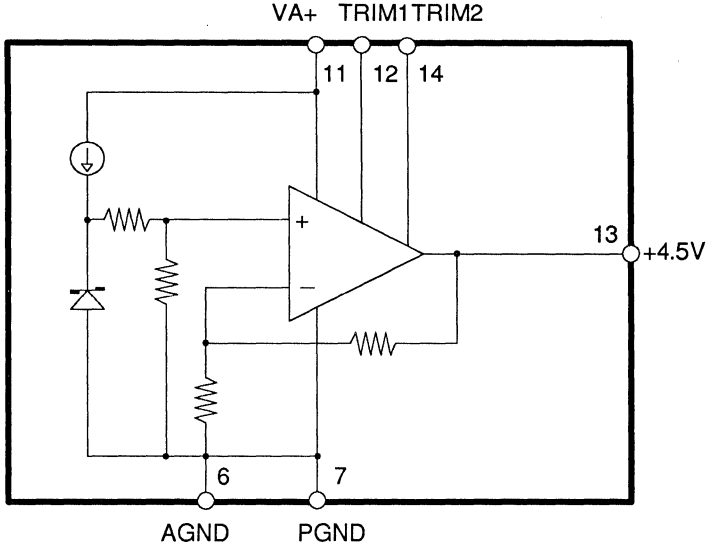
- Very High Accuracy: + 4.500V ± 0.4 mV
- Very Low Temperature Drift: ± 0.6 ppm / °C -55 °C to+125 °C
- Excellent Long-Term Stability: 25 ppm/1000 hours
- Excellent Line Regulation: 6 ppm/V Typ.
- Designed for use with CS5012, CS5014, CS5016, CS5101, and CS5102 A/D Converters
- 14 Pin DIP Package

General Description

The CS3902 is a precision voltage reference providing +4.500V from an input voltage of 11V to 22V. It offers very high accuracy without trimming and exhibits very low temperature drift: 1/50 LSB / °C at 16 bits. Long term stability of the CS3902 is excellent. The device is suitable for all Crystal Semiconductor Successive Approximation A/D Converters.

ORDERING INFORMATION:

Model	Initial Error	Thermal Drift	Temperature
CS3902-AC	800 µV	400 µV	-25 °C to +85 °C
CS3902-BC	400 µV	200 µV	-25 °C to +85 °C
CS3902-SC	800 µV	600 µV	-55 °C to +125 °C
CS3902-TC	400 µV	300 µV	-55 °C to +125 °C



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (VA+ = +15V, T_A = 25 °C, R_L = 10 kΩ unless otherwise specified)

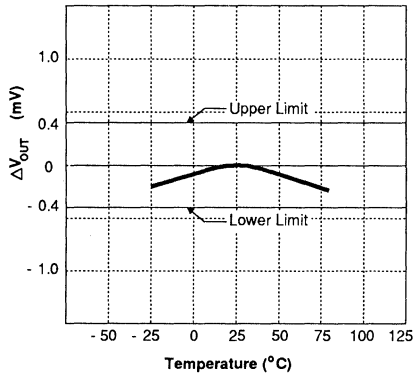
Parameter		CS3902A,B min	CS3902A,B typ	CS3902A,B max	CS3902S,T min	CS3902S,T typ	CS3902S,T max	Units
Specified Temperature Range		-25		85	-55		125	°C
Output Voltage		-	+ 4.5	-	-	+ 4.5	-	V
Output Voltage Errors								
Initial Error	-A,S	-	-	800	-	-	800	uV
	-B,T	-	-	400	-	-	400	uV
Warmup Drift		-	25	-	-	25	-	uV
T_{MIN} to T_{MAX} (Note 1)	-A,S	-	-	400	-	-	600	uV
	-B,T	-	-	200	-	-	300	uV
Long-Term Stability		-	25	-	-	25	-	ppm/1000 hrs.
Noise (.1 - 10 Hz)		-	5	-	-	5	-	uVp-p
Output Drive		10	-	-	10	-	-	mA
Regulation								
Line		-	30	100	-	30	100	uV/V
Load		-	30	-	-	30	-	uV/mA
Output Adjustment								
Range (Note 2)		-	10	-	-	10	-	mV
Temperature coefficient		-	4	-	-	4	-	uV/°C/mV
Power Supply Currents		-	5	7	-	5	7	mA

Notes:
1. Using the box method the specified value is the maximum deviation from the output voltage at 25 °C over the specified operating temperature range.
2. Optional Fine Adjust for approximately ±10mV
3. The 4.5V output is unloaded.

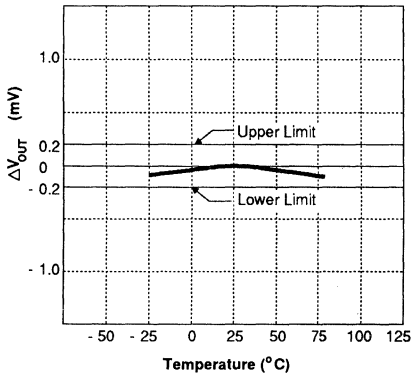
Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (VA+ =+15V,T_A = 25 °C, R_L = 10 kΩ unless otherwise specified)

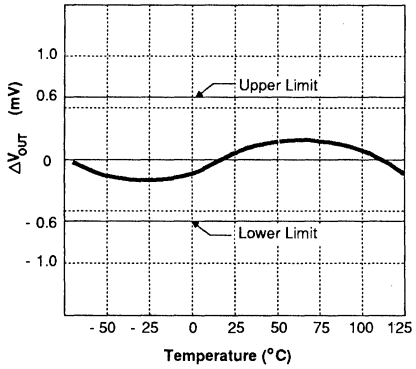
Parameter	CS3902A,B min	typ	max	CS3902S, T min	typ	max	Units
VA+	+ 11	-	+ 22	+ 11	-	+ 22	V
Operating Temperature	- 25	-	85	- 55	-	125	°C
Storage Temperature	- 65	-	150	- 65	-	150	°C
Short Circuit Protection	Continuous						-



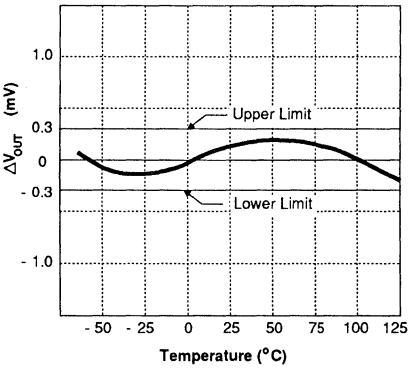
CS3902A



CS3902B



CS3902S



CS3902T

VOUT vs.Temperature Graphs

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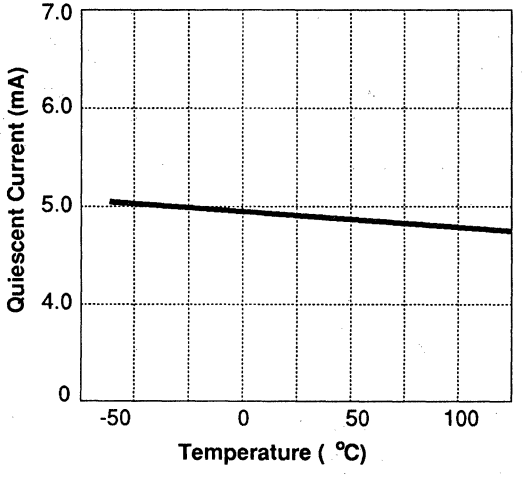
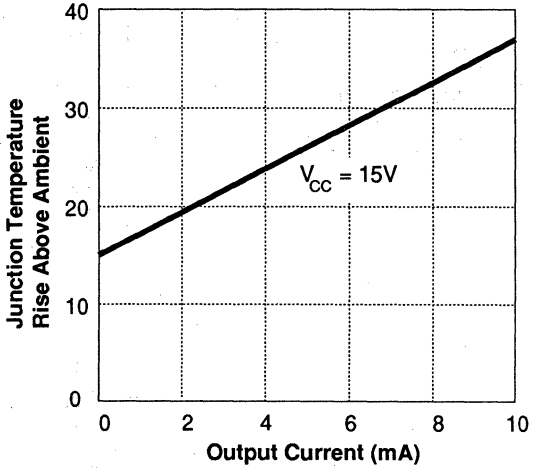
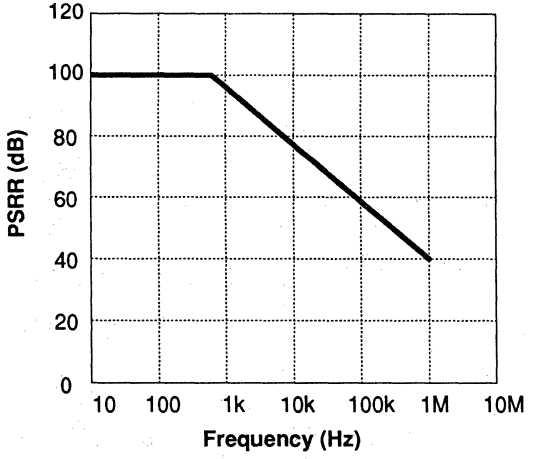


Quiescent Current vs. Temperature



Junction Temperature Rise vs. Output Current



PSRR vs. Frequency

Theory Of Operation

Figure 1 illustrates the internal configuration of the CS3902. An FET current source is used to bias a 6.3V zener diode. The zener voltage is divided by the resistor network R1 and R2. This voltage is then applied to the noninverting input of the operational amplifier which amplifies the voltage to produce a 4.500 V output. The gain is determined by the resistor elements R3 and R4: G =1 + R4/R3. The 6.3V zener diode is used because it is the most stable diode over time and temperature.

The current source provides a closely regulated zener current, which determines the slope of the reference's voltage vs. temperature function. By trimming the zener current a lower drift over temperature can be achieved. But since the voltage vs. temperature function is nonlinear, this method leaves a residual error over wide temperature ranges.

To remove this residual error, a nonlinear compenstion network of thermistors and resistors was developed. This proprietary network eliminates most of the nonlinearity in the voltage vs. temperature function. By then adjusting the slope, a very stable voltage over wide temperatuire range can be achieved. This network is less than 2% of the overall network resistance so it has a negligible effect on long term stability.

Application Information

Figure 2 shows the proper system connection of the CS3902 voltage reference. It is illustrated with the optional output trim potentiometer. Pay careful attention to the circuit layout to avoid noise pickup and voltage drops in the lines.

The CS3902 series voltage references have the ground terminal brought out on two pins (pin 6 and pin 7) which are connected together internally. This allows the user to achieve greater

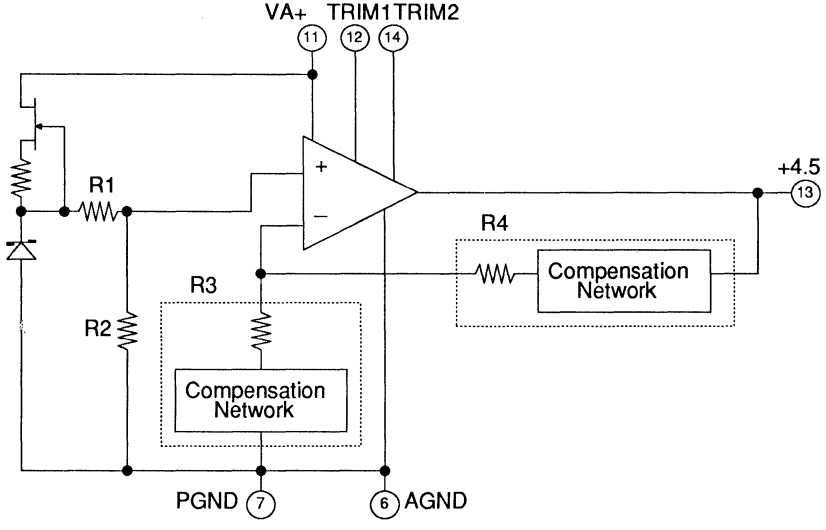


Figure 1. CS3902 Internal Configuration

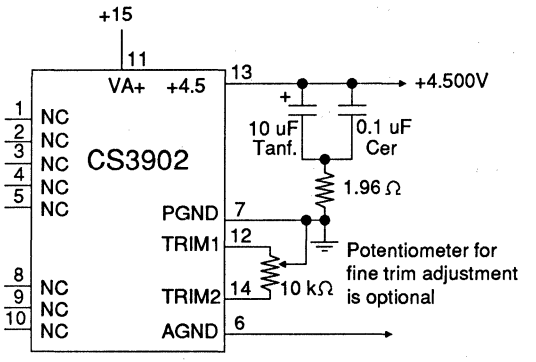
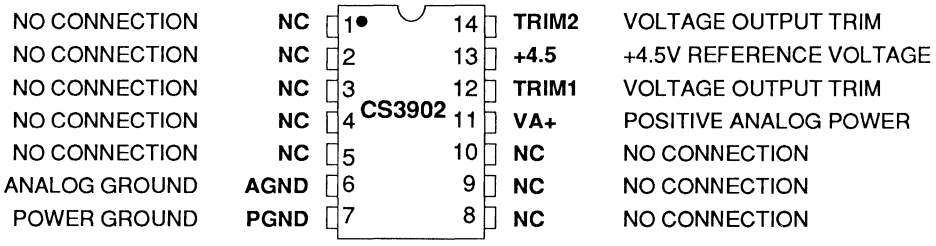


Figure 2. System Connection Diagram

accuracy when using a socket. Voltage references have a voltage drop across their power supply ground pin due to quiescent current flowing through the contact resistance. If the contact resistance was constant with time and temperature this voltage drop could be trimmed out. When the reference is plugged into a socket this source of error can be as high as 20 ppm. By connecting pin 7 to the power supply ground and pin 6 to a high impedance ground point in the measurement circuit the error due to the contact resistance can be eliminated. If the unit is soldered into place the contact resistance is sufficiently small that it doesn't affect performance.

See the application note "Voltage References for the CS501X/CS5101/CS5102/CS5126 Series of A/D converters" for discussion of the filtering components on the output of the CS3902.

PIN DESCRIPTION



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•Notes•

INTRODUCTION

The CS1232 compares the system power supply to an on-chip band gap voltage reference and signals if supplies fall below 4.6 volts. This permits the host microprocessor to gracefully power down the system before supplies fail. Critical system parameters can be saved in non-volatile memory for reinitialization when power supplies return to rated levels. The CS1232 also contains a watchdog timer and pushbutton reset circuit. The CS1232 is pin and functionally compatible with the Dallas Semiconductor DS1232

CONTENTS

Semiconductor Corporation

CS1232

Micromonitor

Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- 8-pin Mini-DIP or 16-pin SOIC
- Pin compatible with DS1232

General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

The power status (V_{CC}) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when V_{CC} goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after V_{CC} returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

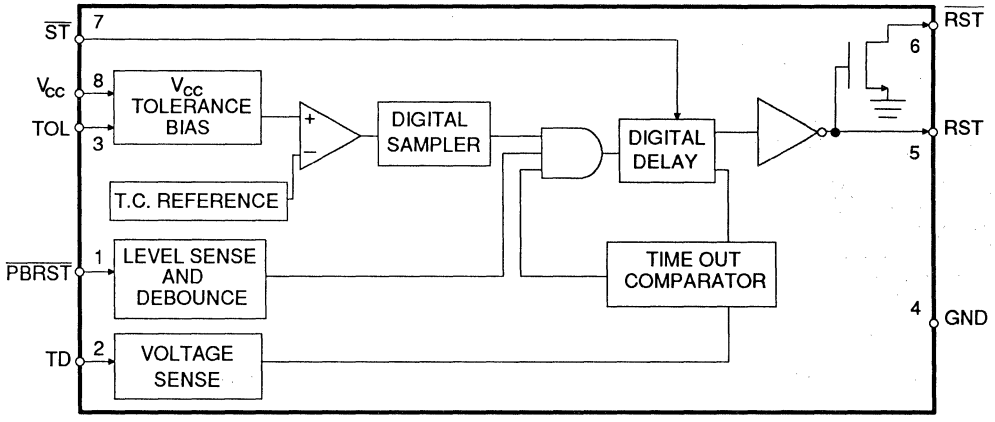
The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

A surface mount 16-pin SOIC is available, as well as an 8-pin Plastic DIP.

ORDERING INFORMATION:

Model	Temp. Range	Package
CS1232- P	0 °C to 70 °C	8-pin Plastic DIP
CS1232-IP	-40 °C to +85 °C	8-pin Plastic DIP
CS1232- S	0 °C to 70 °C	16-pin SOIC
CS1232-IS	-40 °C to +85 °C	16-pin SOIC



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

ANALOG CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5 to 5.5V)

Parameter	Symbol	min	typ	max	Units
V_{CC} Trip Point (TOL = GND) (Note 1)	V_{CCTP}	4.50	4.62	4.74	V
V_{CC} Trip Point (TOL = V_{CC}) (Note 1)	V_{CCTP}	4.25	4.37	4.49	V
Operating Current (Note 2)	I_{CC}	–	0.4	2.0	mA

Notes: 1. All Voltages Referenced To Ground
2. Measured with outputs open

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	min	typ	max	Units
Operating Temperature	CS1232		0	–	+ 70	°C
	CS1232-I		– 40	–	+ 85	°C
Supply Voltage (Note 1)		V_{CC}	4.5	5.0	5.5	V

DIGITAL CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5V to 5.5V)

Parameter	Symbol	min	typ	max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level (Note 1)	V_{IH}	2.0	–	V_{CC} +0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level (Note 1)	V_{IL}	– 0.3	–	+ 0.8	V
Output High Current @2.4 V RST only	I_{OH}	– 1.0	– 2.0	–	mA
Output Low Current @0.4 V RST, $\overline{RST}$	I_{OL}	2.0	3.0	–	mA
Input Leakage (Note 3)	I_{IL}	– 1.0	–	+ 1.0	uA
Input Capacitance T_A = 25 °C	C_{IN}	–	–	5	pF
Output Capacitance T_A = 25 °C	C_{OUT}	–	–	7	pF

Note: 3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 100 kΩ typical.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	min	typ	max	Units
Voltage on any Pin Relative to Ground	− 1.0	−	+7.0	V
Input Current	−	−	±10	mA
Storage Temperature	− 55	−	+125	°C
Soldering Temperature	260 °C for 10 Sec			

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

SWITCHING CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 5V ± 10%)

Parameter	Symbol	min	typ	max	Units
$\overline{PBRST}$ = V_{IL}	t_{PB}	20	−	−	ms
RESET Active Time	t_{RST}	250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	20	−	−	ns
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}	−	−	100	ns
V_{CC} Slew Rate from 4.75V - 4.25V	t_F	300	−	−	us
V_{CC} Detect to RST and $\overline{RST}$ (Note 4)	t_{RPU}	250	610	1000	ms
V_{CC} Slew Rate from 4.25V - 4.75V	t_R	0	−	−	ns
$\overline{ST}$ Pulse Period TD pin at Ground TD pin floating TD pin connected to V_{CC} (Note 5)	t_{TD}	 62.5 250 500	 − − −	 250 1000 2000	 ms ms ms

Note: 4. t_R = 5 µs

5. t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}.

6. $\overline{RST}$ is an N-channel open drain output.

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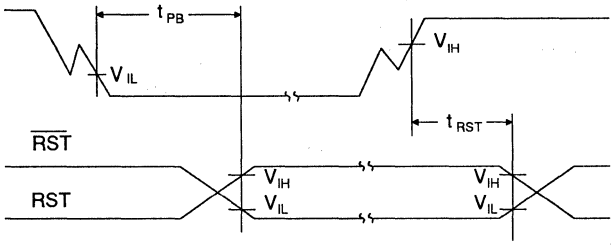
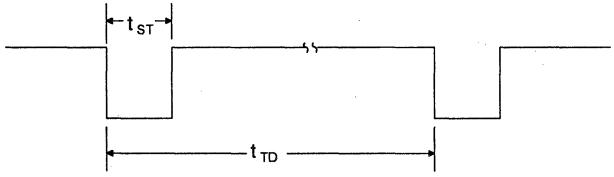
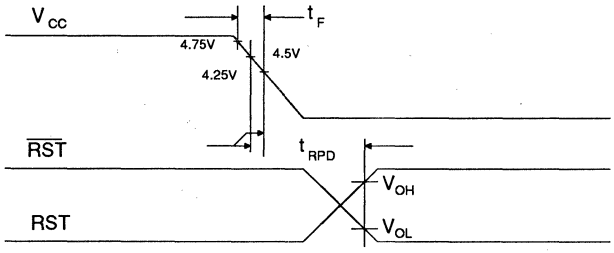


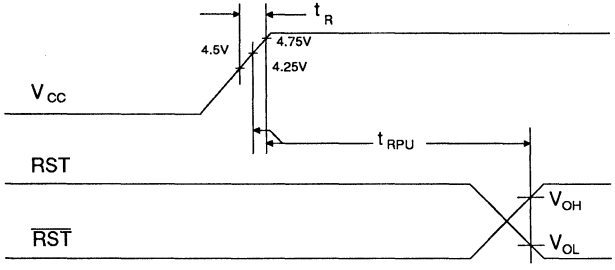
Timing Diagram—Pushbutton Reset



Timing Diagram—Strobe Input



Timing Diagram—Power Down



Timing Diagram—Power Up

POWER SUPPLY MONITOR

The CS1232 will detect out-of-tolerance power supplies for processor-based systems as well as warn of an impending power failure. The TOL digital input pin defines the threshold level for V_{CC}; when the V_{CC} level drops below the TOL defined level, the comparator outputs the signals RST and $\overline{RST}$. The threshold level is set to typically 4.37 V if TOL is connected to V_{CC}, and is set to typically 4.62 V if TOL is connected to GND. The processor is allowed to continue until the last possible moment that V_{CC} is valid. Upon return of power, RST and $\overline{RST}$ are active for 250 ms (minimum) to allow stabilization.

PUSHBUTTON RESET CONTROL

$\overline{PBRST}$ is normally connected to a reset pushbutton (see Figure 1). This active low signal is debounced and timed to generate signals of 250 ms (minimum) for RST and $\overline{RST}$. The delay begins when $\overline{PBRST}$ is released from from the low state. $\overline{PBRST}$ has an internal 100 kΩ pull-up resistor.

WATCHDOG TIMER

When RST and $\overline{RST}$ become inactive (normal CPU operation), the watchdog timer starts timing out, using the time set by TD. RST and $\overline{RST}$ are forced active when $\overline{ST}$ is not stimulated for this predetermined time. TD sets the time to be: 150 ms if TD is connected to ground, 600 ms is TD is not connected, or 1.2 seconds with TD connected to V_{CC}. RST and $\overline{RST}$ are driven active for 250 ms (minimum) if no high-to-low transition occurs on the $\overline{ST}$ input pin before time out. Microprocessor address signals, data signals, control signals, and output port bits can be used for the $\overline{ST}$ input pin. These signals cause the watchdog timer to be reset prior to time out indicating normal function of the microprocessor (see Figure 2).

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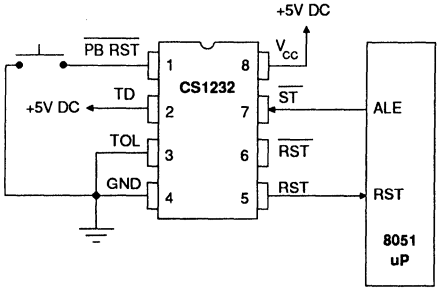


Figure 1. Pushbutton Reset

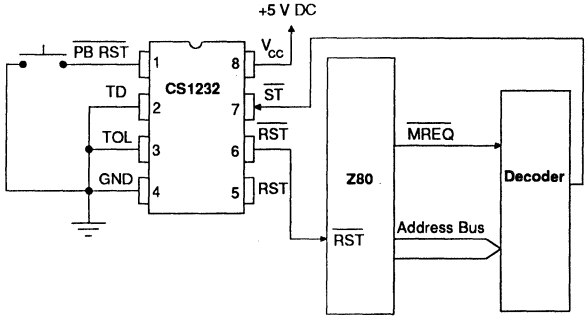


Figure 2. Watchdog Timer

PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	1	8	Vcc	+5 VOLT POWER
TIME DELAY SET	TD	2	7	$\overline{\text{ST}}$	STROBE INPUT
SELECTS Vcc DETECT LEVEL	TOL	3	6	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain
GROUND	GND	4	5	RST	RESET OUTPUT (Active High)

CS1232

NO CONNECTION	NC	1	16	NC	NO CONNECT
PUSH BUTTON RESET INPUT	$\overline{\text{PBRST}}$	2	15	Vcc	+5 VOLT POWER
NO CONNECT	NC	3	14	NC	NO CONNECTION
TIME DELAY SET	TD	4	13	$\overline{\text{ST}}$	STROBE INPUT
NO CONNECT	NC	5	12	NC	NO CONNECT
SELECTS Vcc DETECT LEVEL	TOL	6	11	$\overline{\text{RST}}$	RESET OUTPUT (Active Low, Open Drain
NO CONNECT	NC	7	10	NC	NO CONNECT
GROUND	GND	8	9	RST	RESET OUTPUT (Active High)

CS1232

INTRODUCTION

All Crystal products are available in die form. Here is a selection of currently available die data sheets.

SMART *Analog*™ ADC architectures achieve their accuracy through the inclusion of digital logic on-chip to ensure performance specifications. Self-calibrating ADCs, one family of circuits, incorporate a digital microcontroller to correct for linearity as well as gain and offset errors. Delta-Sigma oversampling ADCs, another family, sample the signal substantially faster than the system sampling rate and then digitally filter average many actual samples to obtain a highly accurate output at the system rate.

Analog performance of the device is therefore governed by digital functionality which is easily tested during the die manufacturing process at wafer probe. SMART *Analog*™ devices all include digital self-test modes to further enhance this thorough testability.

All die manufacturing activities maintain configuration control and traceability to the original wafer lot. Passivation thicknesses are controlled to meet military requirements and die storage is maintained in accordance with MIL STD 883, method 2010. Scribed and broken individual die are 100% inspected to the requirements of MIL STD 883, method 2010, test condition B. Shipment of die to Crystal customers is accomplished in waffle packs, each of which contain die from only one wafer lot.

CONTENTS

Semiconductor Corporation

CS1232-U

Micromonitor Die

Features

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatic restart after power failure
- Monitors pushbutton for external reset
- Monitors microprocessor power supply to be within 5% or 10% of 5 V
- No discrete components needed
- Pin compatible with DS1232

General Description

The CS1232 is a monitor for microprocessors which checks program execution, power source quality, and external reset status.

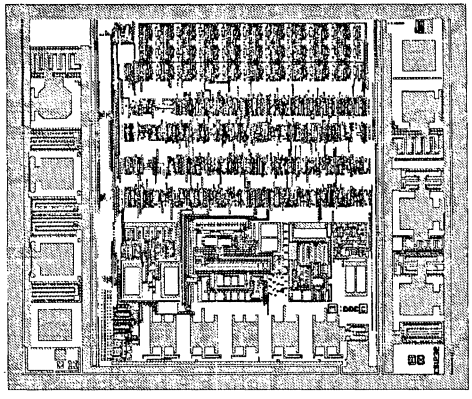
The power status (V_{CC}) is monitored by a comparator and a precision temperature-compensated reference. Reset is forced active by an internal signal when V_{CC} goes out-of-tolerance. Reset signals stay active for a minimum for 250 ms after V_{CC} returns to an in-tolerance condition. This allows both power supply and processor to stabilize.

The pushbutton reset control input is debounced and the active reset minimum pulse width of 250 ms is guaranteed.

The internal watchdog timer forces the reset signals active if the strobe input is not driven low prior to time out. The CS1232 timer can be set to operate at time out settings of approximately 150ms, 600ms, and 1.2 seconds.

ORDERING INFORMATION:

Model	Temp. Range
CS1232-U	0 °C to 70 °C



Dice Information The CS1232-U dice are functionally identical to packaged CS1232 devices. For general application information, refer to the packaged product data sheets.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5 to 5.5V)

Parameter	Symbol	min	typ	max	Units
V_{CC} Trip Point (TOL = GND) (Note 1)	V_{CCTP}	–	4.62	–	V
V_{CC} Trip Point (TOL = V_{CC}) (Note 1)	V_{CCTP}	–	4.37	–	V
Operating Current (Note 2)	I_{CC}	–	0.4	2.0	mA

Notes: 1. All Voltages Referenced To Ground
2. Measured with outputs open

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	min	typ	max	Units
Operating Temperature		0	–	+70	°C
Supply Voltage (Note 1)	V_{CC}	4.5	5.0	5.5	V

DIGITAL CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 4.5V to 5.5V)

Parameter	Symbol	min	typ	max	Units
$\overline{ST}$ and $\overline{PBRST}$ Input High Level (Note 1)	V_{IH}	2.0	–	V_{CC} +0.3	V
$\overline{ST}$ and $\overline{PBRST}$ Input Low Level (Note 1)	V_{IL}	−0.3	–	+ 0.8	V
Output High Current @2.4 V RST only	I_{OH}	−1.0	−2.0	–	mA
Output Low Current @0.4 V RST, $\overline{RST}$	I_{OL}	2.0	3.0	–	mA
Input Leakage (Note 3)	I_{IL}	−1.0	–	+ 1.0	uA
Input Capacitance T_A = 25 °C	C_{IN}	–	–	5	pF
Output Capacitance T_A = 25 °C	C_{OUT}	–	–	7	pF

Note: 3. $\overline{PBRST}$ is internally pulled up to V_{CC} with an internal impedance of 100 kΩ typical.

Specifications are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	min	typ	max	Units
Voltage on any Pin Relative to Ground	− 1.0	−	+7.0	V
Input Current	−	−	±10	mA
Storage Temperature	− 55	−	+125	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

SWITCHING CHARACTERISTICS (T_{MIN} to T_{MAX}, V_{CC} = 5V ± 10%)

Parameter	Symbol	min	typ	max	Units
$\overline{PBRST}$ = V_{IL}	t_{PB}	20	−	−	ms
RESET Active Time	t_{RST}	250	610	1000	ms
$\overline{ST}$ Pulse Width	t_{ST}	20	−	−	ns
V_{CC} Detect to RST and $\overline{RST}$	t_{RPD}	−	−	100	ns
V_{CC} Slew Rate from 4.75V - 4.25V	t_F	300	−	−	us
V_{CC} Detect to RST and $\overline{RST}$ (Note 4)	t_{RPU}	250	610	1000	ms
V_{CC} Slew Rate from 4.25V - 4.75V	t_R	0	−	−	ns
$\overline{ST}$ Pulse Period TD pin at Ground TD pin floating TD pin connected to V_{CC} (Note 5)	t_{TD}	 62.5 250 500	 − − −	 250 1000 2000	 ms ms ms

Note: 4. t_R = 5 µs
5. t_{TD} is the maximum elapsed time between $\overline{ST}$ pulses which will keep the watchdog timer from forcing RST and $\overline{RST}$ to the active state for a time of t_{RST}.
6. $\overline{RST}$ is an N-channel open drain output.

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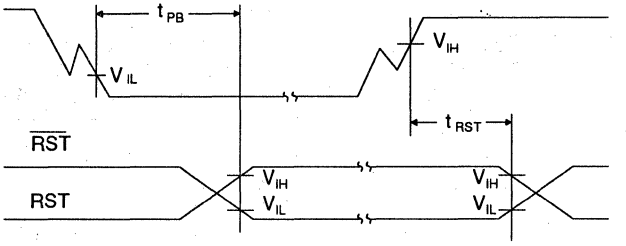
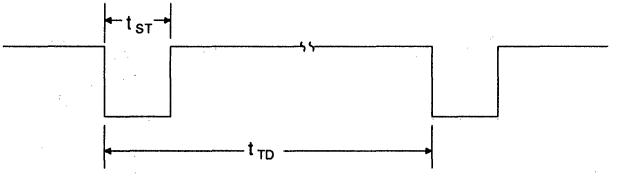
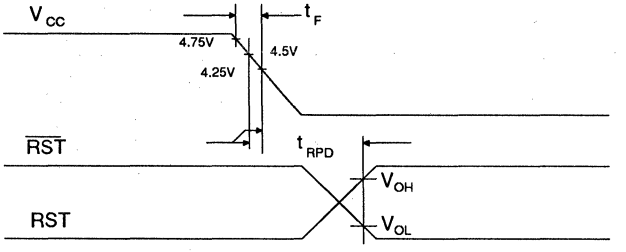


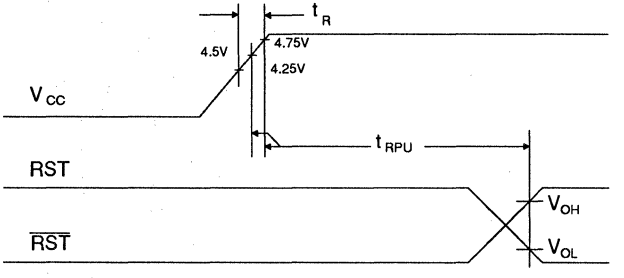
Timing Diagram—Pushbutton Reset



Timing Diagram—Strobe Input



Timing Diagram—Power Down



Timing Diagram—Power Up

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size: 0.061" by 0.069" (± 0.002").

2. The CS1232-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to V_{CC}.

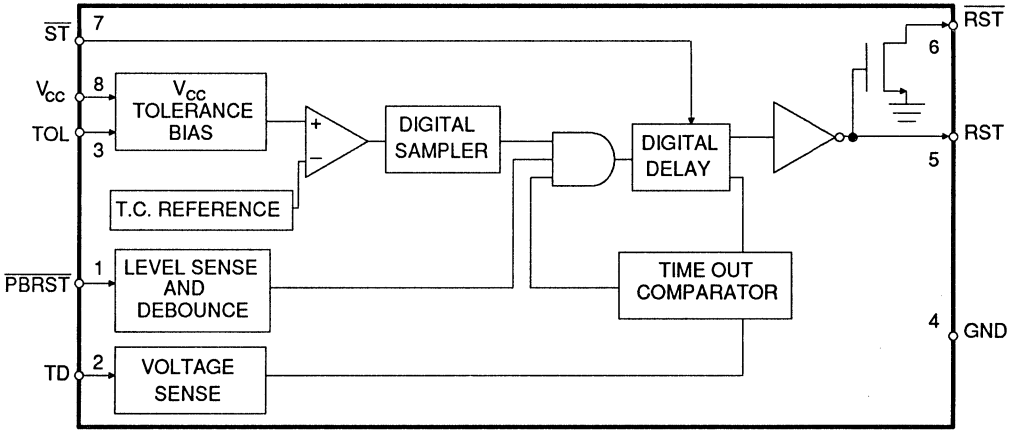
3. Die thickness shall be 0.0175" ± 0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 100.

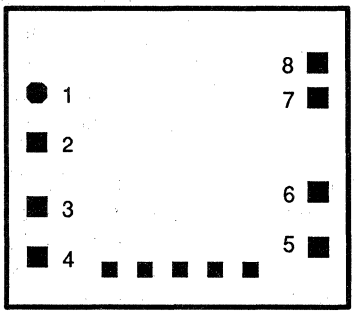
5. The cavity dimensions for each die within the waffle pack are 0.080" by 0.080" (Waffle Pack Type H20-080).

5. The CS1232-U requires no particular bonding sequence.

6. The CS1232 product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 3000V and 300 mA dc latch currents. This meets Crystal's minimum criteria of 2500V and 100 mA respectively. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.



Bonding Diagram for CS1232-U



1 -	$\overline{\text{PBRST}}$	5 -	RST
2 -	TD	6 -	$\overline{\text{RST}}$
3 -	TOL	7 -	$\overline{\text{ST}}$
4 -	GND	8 -	V_{CC}

Semiconductor Corporation

CS5012–U

12-Bit, 62.5 kHz Self-Calibrating A/D Converter Die

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Microprocessor Interface
  - Parallel and Serial Output
- True 12-Bit Precision
  - Linearity Error: ±1/4 LSB
  - No Missing Codes
  - S/(N+D): 73 dB
  - THD: 0.008 %
- 12 µs Conversion Time
  - Throughput Rates up to 62.5 kHz
- Low Power Consumption: 120 mW

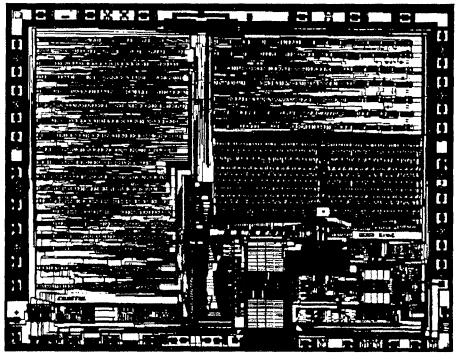
General Description

The CS5012 is a 12-bit monolithic CMOS analog-to-digital converter with 12 µs conversion time. On-chip self-calibration circuitry, which can be placed under intelligent control, achieves maximum nonlinearity of ±1/2 LSB and no missing codes. Superior linearity also leads to 73 dB S/(N+D) with peak harmonics below -87 dB. Offset and full-scale errors are similarly kept within 1/4 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5012 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75 µs to 0.01%, allowing throughput rates up to 62.5 kHz.

The CS5012's advanced CMOS construction provides low power consumption of 120 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION: Page 9-15



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Dice Information | CS5012-U dice are functionally identical to packaged CS5012 devices. For general application information, refer to the packaged product data sheet.

Crystal Semiconductor Corporation
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(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5 to 4.5V; Full-Scale Input Sinewave, 1 kHz; f_{clk} = 4 MHz for -12, 2 MHz for -24; f_s = 63 kHz for -12, 34 kHz for -24; Bipolar Mode ; Analog Source Impedance = 200Ω unless otherwise specified; Tmin to Tmax specs. apply after calibration at the temperature of interest.)

Parameter		CS5012-KU min	CS5012-KU typ	CS5012-KU max	CS5012-TU min	CS5012-TU typ	CS5012-TU max	Units
Specified Temperature Range		0		70	-55		125	°C
Probe Test Temperature			25			125		°C
dc Accuracy								
Linearity Error	T_{min} to T_{max}		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Differential Linearity	T_{min} to T_{max}		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Full Scale Error	T_{min} to T_{max}		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Unipolar Offset	T_{min} to T_{max}		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Bipolar Offset	T_{min} to T_{max}		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Bipolar Zero Error	T_{min} to T_{max}		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Noise (Note 1)	Unipolar Mode		45			45		uV_{rms}
	Bipolar Mode		90			90		uV_{rms}
Dynamic Performance								
Peak Harmonic or Spurious Noise								
T_{min} to T_{max}	1kHz Input		87			87		dB
	12kHz Input		83			83		dB
Total Harmonic Distortion			0.008			0.008		%
Signal-to-Noise Ratio								
T_{min} to T_{max}	0dB Input		73			73		dB
	-60dB Input		13			13		dB
Analog Input								
Aperture Time			25			25		ns
Aperture Jitter			100			100		ps
Input Capacitance (Note 2)	Unipolar Mode		275	375		275	375	pF
	Bipolar Mode		165	220		165	220	pF

Notes: 1. Wideband noise aliased into the baseband. Referred to the input.
2. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15 pF.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter		CS5012-KU min	typ	max	CS5012-TU min	typ	max	Units
Conversion & Throughput								
Conversion Time	-12			12.25			12.25	us
(Notes 3, 4)	-24			24.5			24.5	us
Acquisition Time	-12		3.0	3.75		3.0	3.75	us
(Note 4)	-24		4.5	5.25		4.5	5.25	us
Throughput	-12	62.5			62.5			kHz
(Note 4)	-24	33.6			33.6			kHz
Power Supplies								
Power Supply Currents (Note 5)								
I_{A+}			9	19		9	19	mA
I_{A-}			- 9	- 19		- 9	- 19	mA
I_{D+}			3	6		3	6	mA
I_{D-}			- 3	- 6		- 3	- 6	mA
Power Dissipation	(Note 5)		120	250		120	250	mW
Power Supply Rejection (Note 6)								
Positive Supplies			84			84		dB
Negative Supplies			84			84		dB

Notes:
3. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
4. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5012's internal conversion clock, interleave calibrate is disabled, and operation is from the full-rated external master clock.
5. All outputs unloaded. All inputs CMOS levels.
6. With 300 mV p-p, 1kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB.

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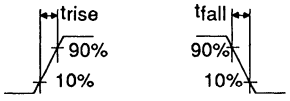
SWITCHING CHARACTERISTICS

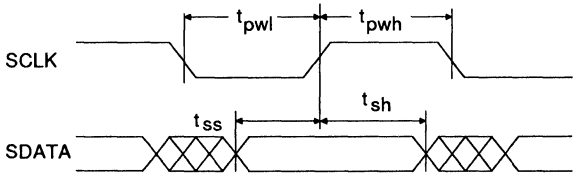
(T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Logic 0 = 0V; Logic 1 = VD+; C_L = 50 pF; BW = VD+)

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: KU, - 12	f_{CLK}	2	-	-	MHz
TU, - 12		1.75	-	-	
- 24		1	-	-	
Externally Supplied: - 12		100 kHz	-	4	
- 24		100 kHz	-	2	
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK}$+ 50	-	t_c	ns
Conversion Time	t_c	(Note 7)	-	(Note 7)	ns
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 8)	t_{epw}	$4/f_{CLK}$ - 20	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-KU	t_{ca}	-	90	120	ns
-TU		-	115	150	
$\overline{RD}$ Low to Data Valid					
-KU	t_{ra}	-	90	120	ns
-TU		-	115	150	
Output Float Delay: -KU	t_{fd}	-	90	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -TU			90	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK}$ - 50	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK}$ - 100	$2/f_{CLK}$	-	ns

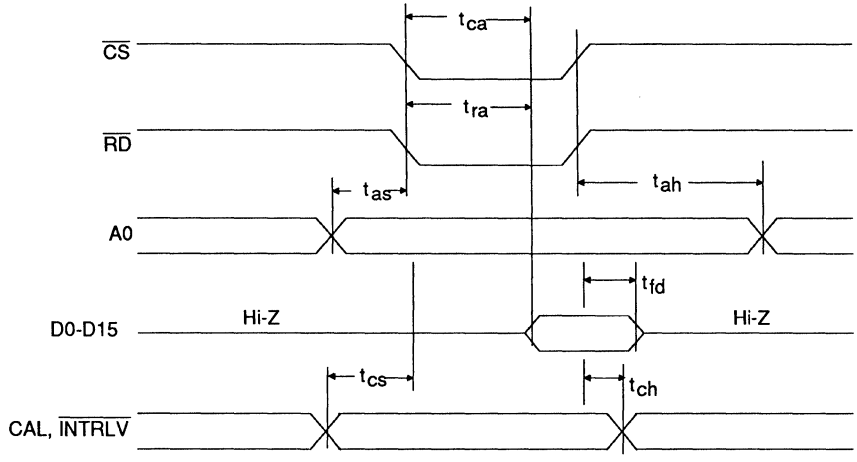
Notes: 7. See Table 1 in packaged product data sheet and master clock frequencies above.
8. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, It returns high within four master clock cycles from the start of a data read operation or a conversion cycle.



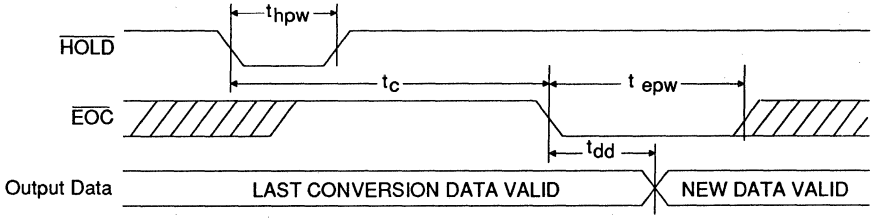
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

9

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 9)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 9. I_{out} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 10.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.0	2.5	VA+ - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	-	VREF	V
(Note 11)	Bipolar	V_{AIN}	-(VREF)	-	VREF	V

Notes: 10. All voltages with respect to ground.

11. The CS5012 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 12)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VD+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 12. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.270" by 0.337" (± 0.002").

2. The CS5012-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

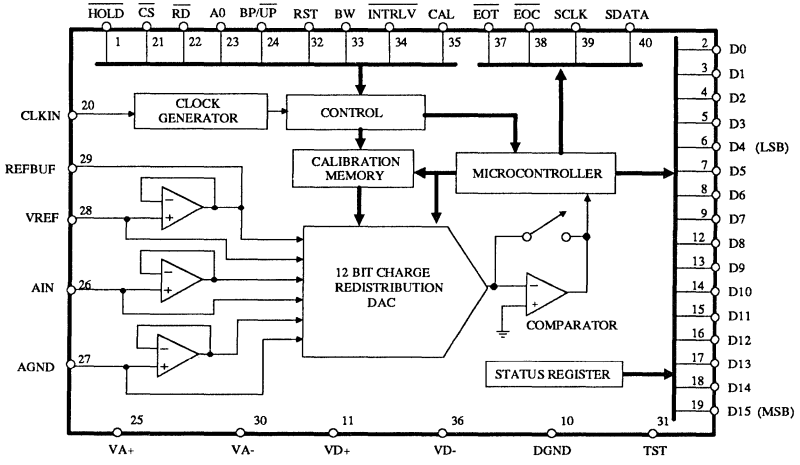
3. Die thickness shall be 0.0175" ±0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 16.

5. The cavity dimensions for each die within the waffle pack are 0.350" by 0.350".

5. The CS5012-U requires no particular bonding sequence.

6. The CS5012 product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 3000V and 300 mA dc latch currents. This meets Crystal's minimum criteria of 2500V and 100 mA respectively. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.

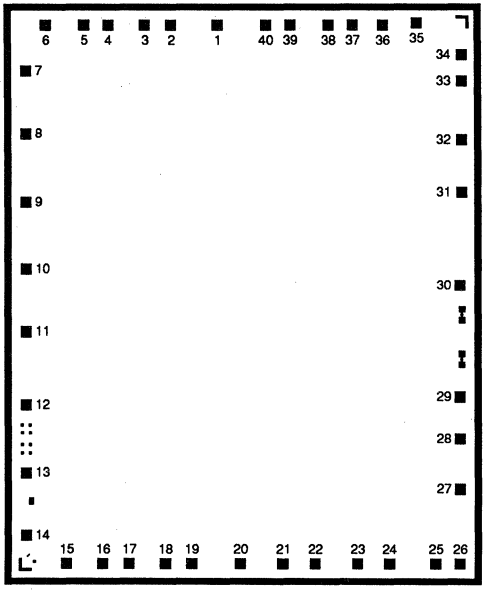


Block Diagram

ORDERING GUIDE

Model Number	Temperature Range	Throughput	Conversion Time
CS5012-KU12	0 to 70 °C	63 kHz	12 µs
CS5012-KU24	0 to 70 °C	34 kHz	24 µs
CS5012-TU12	-55 to 125 °C	63 kHz	12 µs
CS5012-TU24	-55 to 125 °C	34 kHz	24 µs

Bonding Diagram for CS5012-U



1	-	$\overline{\text{HOLD}}$	21	-	$\overline{\text{CS}}$
2	-	D0	22	-	$\overline{\text{RD}}$
3	-	D1	23	-	A0
4	-	D2	24	-	BP / $\overline{\text{UP}}$
5	-	D3	25	-	VA+
6	-	D4	26	-	AIN
7	-	D5	27	-	AGND
8	-	D6	28	-	VREF
9	-	D7	29	-	REFBUF
10	-	DGND	30	-	VA-
11	-	VD+	31	-	TST
12	-	D8	32	-	RST
13	-	D9	33	-	BW
14	-	D10	34	-	$\overline{\text{INTRLV}}$
15	-	D11	35	-	CAL
16	-	D12	36	-	VD-
17	-	D13	37	-	$\overline{\text{EOT}}$
18	-	D14	38	-	$\overline{\text{EOC}}$
19	-	D15	39	-	SCLK
20	-	CLKIN	40	-	SDATA

Semiconductor Corporation

CS5014–U

14-Bit, 56 kHz Self-Calibrating A/D Converter Die

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Microprocessor Interface
  - Parallel and Serial Output
- True 14-Bit Precision
  - Linearity Error: ±1/2 LSB
  - No Missing Codes
  - S/(N+D): 83 dB
  - THD: 0.003 %
- 14.25 µs Conversion Time
  - Throughput Rates up to 56 kHz
- Low Power Consumption: 120 mW

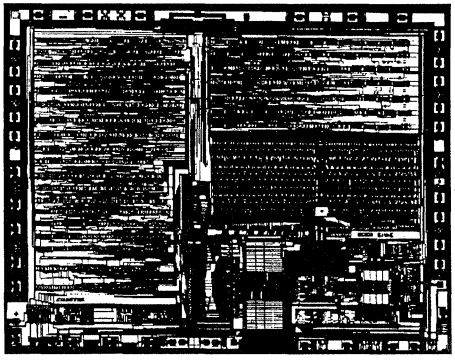
General Description

The CS5014 is a 14-bit monolithic CMOS analog-to-digital converter with 14.25 µs conversion time. On-chip self-calibration circuitry, which can be placed under intelligent control, achieves maximum nonlinearity of ±1/2 LSB and no missing codes. Superior linearity also leads to 83 dB S/(N+D) with peak harmonics below -96 dB. Offset and full-scale errors are similarly kept within 1/2 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5014 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75 µs, allowing throughput rates up to 56 kHz.

The CS5014's advanced CMOS construction provides low power consumption of 120 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION: Page 9-23



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Dice Information | CS5014-U dice are functionally identical to packaged CS5014 devices. For general application information, refer to the packaged product data sheets.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS

(T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V;
Full-Scale Input Sinewave, 1kHz; f_{clk} = 4MHz for -14, 2MHz for -28; f_s = 56kHz for -14, 30kHz for -28;
Bipolar Mode ; Analog Source Impedance = 200Ω unless otherwise specified)

Parameter		CS5014-KU min	CS5014-KU typ	CS5014-KU max	CS5014-TU min	CS5014-TU typ	CS5014-TU max	Units
Specified Temperature Range		0		70	-55		125	°C
Probe Test Temperature			25			125		°C
dc Accuracy								
Linearity Error	T_{min} to T_{max}		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Differential Linearity	T_{min} to T_{max} (Note 2)		± 1/4	± 1/2		± 1/4	± 1/2	LSB
Full Scale Error	T_{min} to T_{max}		± 1/2			± 1/2		LSB
Unipolar Offset	T_{min} to T_{max}		± 1/4			± 1/4		LSB
Bipolar Offset	T_{min} to T_{max}		± 1/4			± 1/2		LSB
Bipolar Zero Error	T_{min} to T_{max}		± 1/2			± 1/2		LSB
Noise (Note 3)	Unipolar Mode		45			45		uV_{rms}
	Bipolar Mode		90			90		uV_{rms}
Dynamic Performance								
Peak Harmonic or Spurious Noise								
T_{min} to T_{max}	1kHz Input		96			96		dB
	12kHz Input		91			91		dB
Total Harmonic Distortion			0.003			0.003		%
Signal-to-Noise Ratio								
T_{min} to T_{max}	0dB Input		83			83		dB
	-60dB Input		23			23		dB
Analog Input								
Aperture Time			25			25		ns
Aperture Jitter			100			100		ps
Input Capacitance (Note 4)	Unipolar Mode		275	375		275	375	pF
	Bipolar Mode		165	220		165	220	pF

Notes:
1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest.
2. Minimum Resolution for which no missing codes is guaranteed.
3. Wideband noise aliased into the baseband. Referred to the input.
4. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 10pF.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter	CS5014-KU min	CS5014-KU typ	CS5014-KU max	CS5014-TU min	CS5014-TU typ	CS5014-TU max	Units
Conversion & Throughput							
Conversion Time −14			14.25			14.25	us
(Notes 5, 6) −28			28.5			28.5	us
Acquisition Time −14		3.0	3.75		3.0	3.75	us
(Note 6) −28		4.5	5.25		4.5	5.25	us
Throughput −14	55.6			55.6			kHz
(Note 6) −28	29.6			29.6			kHz
Power Supplies							
Power Supply Currents (Note 7)							
I_{A+}		9	19		9	19	mA
I_{A-}		- 9	- 19		- 9	- 19	mA
I_{D+}		3	6		3	6	mA
I_{D-}		- 3	- 6		- 3	- 6	mA
Power Dissipation (Note 7)		120	250		120	250	mW
Power Supply Rejection (Note 8)							
Positive Supplies		84			84		dB
Negative Supplies		84			84		dB

Notes:
5. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
6. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5014's internal conversion clock, interleave calibrate is disabled, and operation is from the full-rated external master clock. A detailed discussion of conversion timing appears on page 9.
7. All outputs unloaded. All inputs CMOS levels.
8. With 300mV p-p, 1kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB.

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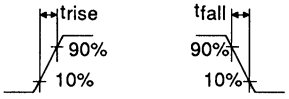
SWITCHING CHARACTERISTICS

($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Logic 0 = 0V; Logic 1 = VD+; C_L = 50pF; BW = VD+)

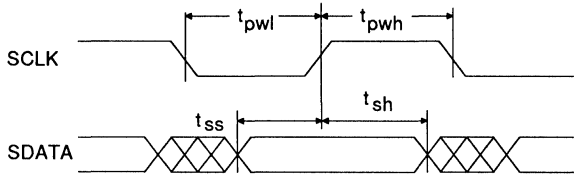
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:					
Internally Generated: KU, -14	f_{CLK}	2	-	-	MHz
TU, -14		1.75			
-28		1	-	-	
Externally Supplied: -14		100 kHz	-	4	
-28		100 kHz	-	2	
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input	t_{rise}	-	-	1.0	us
Any Digital Output		-	20	-	ns
Fall Times: Any Digital Input	t_{fall}	-	-	1.0	us
Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width	t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time	t_c	(Note 9)	-	(Note 9)	ns
Data Delay Time	t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width (Note 10)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low	t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low	t_{as}	20	10	-	
Hold Times:					
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid	t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid	t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid					
-KU	t_{ca}	-	90	120	ns
-TU		-	115	150	
$\overline{RD}$ Low to Data Valid					
-KU	t_{ra}	-	90	120	ns
-TU		-	115	150	
Output Float Delay: -KU	t_{fd}	-	90	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z -TU			90	140	
Serial Clock Pulse Width Low	t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High	t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising	t_{ss}	$2/f_{CLK} - 50$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA	t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

Notes: 9. See Table 1 and master clock frequencies above.

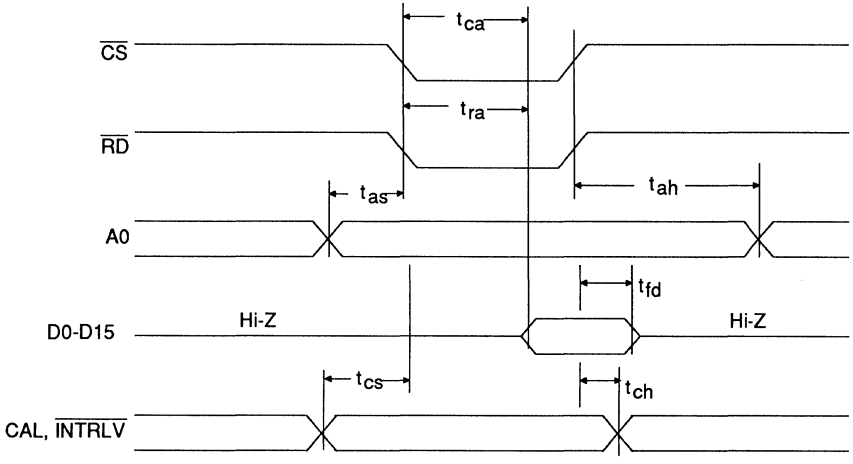
10. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, It returns high within four master clock cycles from the start of a data read operation or a conversion cycle.



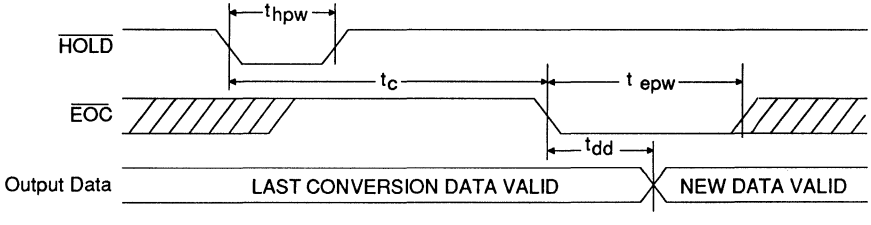
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

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Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 11)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 11. I_{out} = -100µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 12.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	5.5	V
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Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage:	Unipolar	V_{AIN}	AGND	-	VREF	V
(Note 13)	Bipolar	V_{AIN}	-(VREF)	-	VREF	V

Notes: 12. All voltages with respect to ground.
13. The CS5014 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 14)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VD+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 14. Transient currents of up to 100mA will not cause SCR latch-up.

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4. The maximum number of die per waffle pack carrier is 16.

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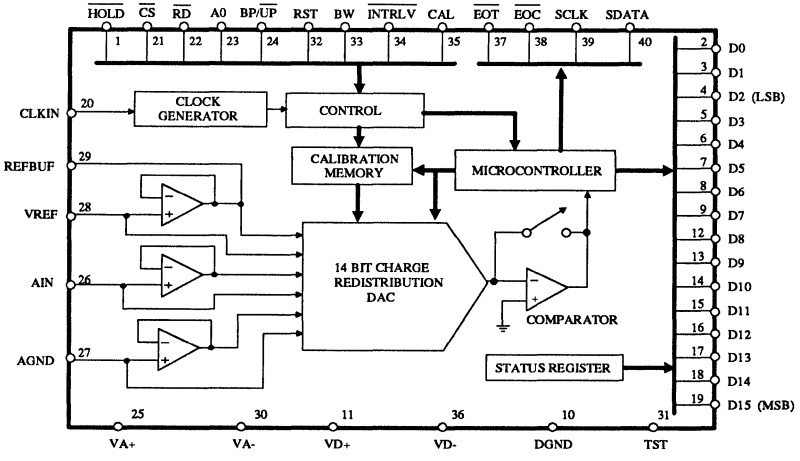
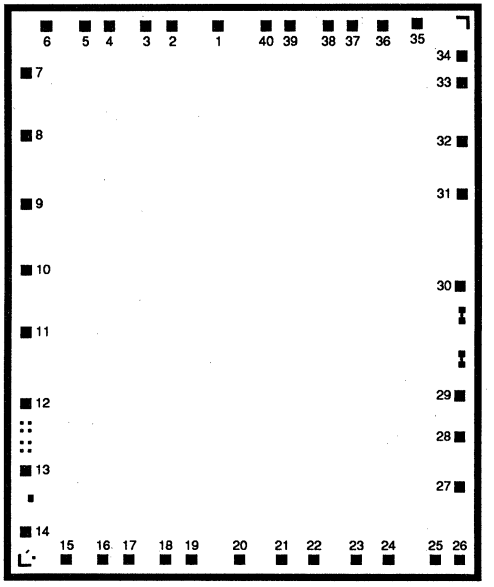


Block Diagram

ORDERING GUIDE

Model Number	Temperature Range	Throughput
CS5014-KU14	0 to 70 °C	56 kHz
CS5014-KU28	0 to 70 °C	30 kHz
CS5014-TU14	-55 to 125 °C	56 kHz

Bonding Diagram for CS5014-U



1	-	$\overline{\text{HOLD}}$	21	-	$\overline{\text{CS}}$
2	-	D0	22	-	$\overline{\text{RD}}$
3	-	D1	23	-	A0
4	-	D2	24	-	BP / $\overline{\text{UP}}$
5	-	D3	25	-	VA+
6	-	D4	26	-	AIN
7	-	D5	27	-	AGND
8	-	D6	28	-	VREF
9	-	D7	29	-	REFBUF
10	-	DGND	30	-	VA-
11	-	VD+	31	-	TST
12	-	D8	32	-	RST
13	-	D9	33	-	BW
14	-	D10	34	-	$\overline{\text{INTRLV}}$
15	-	D11	35	-	CAL
16	-	D12	36	-	VD-
17	-	D13	37	-	$\overline{\text{EOT}}$
18	-	D14	38	-	$\overline{\text{EOC}}$
19	-	D15	39	-	SCLK
20	-	CLKIN	40	-	SDATA

Semiconductor Corporation

CS5016–U

16-Bit, 50 kHz Self-Calibrating A/D Converter Die

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Microprocessor Interface
  - Parallel and Serial Output
- True 16-Bit Precision
  - Linearity Error: ±0.001% FS
  - No Missing Codes
  - S/(N+D): 92dB
  - THD: 0.001%
- 16.25µs Conversion Time
  - Throughput Rates up to 50kHz
- Low Power Consumption: 120mW

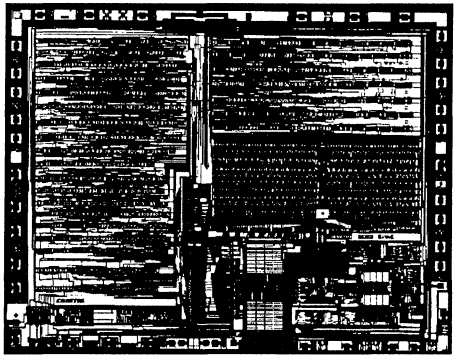
General Description

The CS5016 is a 16-bit monolithic CMOS analog-to-digital converter with 16.25µs conversion time. On-chip self-calibration circuitry, which can be placed under intelligent control, achieves typical nonlinearity of ±0.001% FS and no missing codes. Superior linearity also leads to 92dB S/(N+D) with peak harmonics below -100dB. Offset and full-scale errors are similarly kept within 1 LSB, eliminating the need for manual calibration of any kind. Unipolar and bipolar input ranges are digitally selectable.

The CS5016 consists of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input signal after each conversion within 3.75µs, allowing throughput rates up to 50kHz.

The CS5016's advanced CMOS construction provides low power consumption of 120mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION: Page 9-31



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Dice Information | CS5016-U dice are functionally identical to packaged CS5016 devices. For general application information, refer to the packaged product data sheets.

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ANALOG CHARACTERISTICS

(T_A = 25°C (note 1); VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V;
Full-Scale Input Sinewave, 1 kHz; f_{clk} = 4MHz for -16, 2MHz for -32; f_s = 50kHz for -16, 25kHz for -32;
Bipolar Mode; Analog Source Impedance = 200Ω unless otherwise specified.)

Parameter		CS5016-JU min	CS5016-JU typ	CS5016-JU max	CS5016-SU min	CS5016-SU typ	CS5016-SU max	Units
Specified Temperature Range		0		70	-55		125	°C
Probe Test Temperature			25			125		°C
dc Accuracy								
Linearity Error	T_{min} to T_{max}		0.001	0.003		0.001	0.003	% FS
Differential Linearity	T_{min} to T_{max} (Note 2)	16			16			Bits
Full Scale Error	T_{min} to T_{max}		±2			±2		LSB
Unipolar Offset	T_{min} to T_{max}		±1			±1		LSB
Bipolar Offset	T_{min} to T_{max}		±1			±1		LSB
Bipolar Zero Error	T_{min} to T_{max}		±2			±2		LSB
Noise (Note 3)	Unipolar Mode Bipolar Mode		35 70			35 70		uV_{rms} uV_{rms}
Dynamic Performance								
Peak Harmonic or Spurious Noise T_{min} to T_{max}	1kHz Input 12kHz Input		104 91			104 91		dB dB
Total Harmonic Distortion			0.001			0.001		%
Signal-to-Noise Ratio T_{min} to T_{max}	0dB Input -60dB Input		92 32			92 32		dB dB
Analog Input								
Aperture Time			25			25		ns
Aperture Jitter			100			100		ps
Input Capacitance (Note 4)	Unipolar Mode Bipolar Mode		275 165	375 220		275 165	375 220	pF pF

Notes:
1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest.
2. Minimum resolution for which no missing codes is guaranteed.
3. Wideband noise aliased into the baseband. Referred to the input.
4. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15 pF.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter		CS5016-JU min	CS5016-JU typ	CS5016-JU max	CS5016-SU min	CS5016-SU typ	CS5016-SU max	Units
Conversion & Throughput								
Conversion Time (Notes 5, 6)	–16			16.25			16.25	us
	–32			32.5			32.5	us
Acquisition Time (Note 6)	–16		3.0	3.75		3.0	3.75	us
	–32		4.5	5.25		4.5	5.25	us
Throughput (Note 6)	–16	50			50			kHz
	–32	26.5			26.5			kHz
Power Supplies								
Power Supply Currents (Note 7)								
I_{A+}			9	19		9	19	mA
I_{A-}			–9	–19		–9	–19	mA
I_{D+}			3	6		3	6	mA
I_{D-}			–3	–6		–3	–6	mA
Power Dissipation (Note 7)			120	250		120	250	mW
Power Supply Rejection (Note 8)								
Positive Supplies			84			84		dB
Negative Supplies			84			84		dB

Notes:
5. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
6. Conversion, acquisition, and throughput times depend on the master clock, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5016's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock.
7. All outputs unloaded. All inputs CMOS levels.
8. With 300mV p-p, 1kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6dB in the unipolar mode to 90dB.

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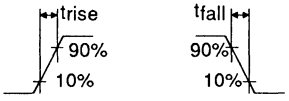
SWITCHING CHARACTERISTICS

($T_A = T_{min}$ to T_{max} ; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF; BW = VD+)

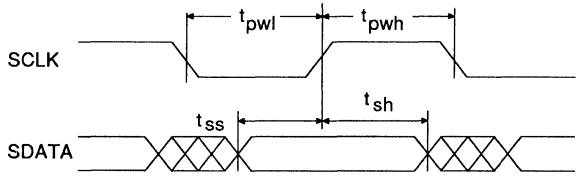
Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency:						
Internally Generated:	JU, -16	f_{CLK}	2	-	-	MHz
	SU, -16		1.75	-	-	
	-32		1	-	-	
Externally Supplied:	-16		100 kHz	-	4	
	-32		100 kHz	-	2	
Master Clock Duty Cycle		-	40	-	60	%
Rise Times: Any Digital Input		t_{rise}	-	-	1.0	us
Any Digital Output			-	20	-	ns
Fall Times: Any Digital Input		t_{fall}	-	-	1.0	us
Any Digital Output			-	20	-	ns
$\overline{HOLD}$ Pulse Width		t_{hpw}	$1/f_{CLK} + 50$	-	t_c	ns
Conversion Time		t_c	(Note 9)	-	(Note 9)	ns
Data Delay Time		t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width	(Note 10)	t_{epw}	$4/f_{CLK} - 20$	-	-	ns
Set Up Times: CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low		t_{cs}	20	10	-	ns
A0 to $\overline{CS}$ and $\overline{RD}$ Low		t_{as}	20	10	-	
Hold Times:						
$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid		t_{ah}	50	30	-	ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid		t_{ch}	50	30	-	
Access Times: $\overline{CS}$ Low to Data Valid						
	-JU	t_{ca}	-	90	120	ns
	-SU		-	115	150	
$\overline{RD}$ Low to Data Valid						
	-JU	t_{ra}	-	90	120	ns
	-SU		-	115	150	
Output Float Delay:	-JU	t_{fd}	-	90	110	ns
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	-SU			90	140	
Serial Clock Pulse Width Low		t_{pwl}	-	$2/f_{CLK}$	-	ns
Pulse Width High		t_{pwh}	-	$2/f_{CLK}$	-	
Set Up Times: SDATA to SCLK Rising		t_{ss}	$2/f_{CLK} - 50$	$2/f_{CLK}$	-	ns
Hold Times: SCLK Rising to SDATA		t_{sh}	$2/f_{CLK} - 100$	$2/f_{CLK}$	-	ns

Notes: 9. See *Analog Characteristics Table* (page 2) and master clock frequencies above.

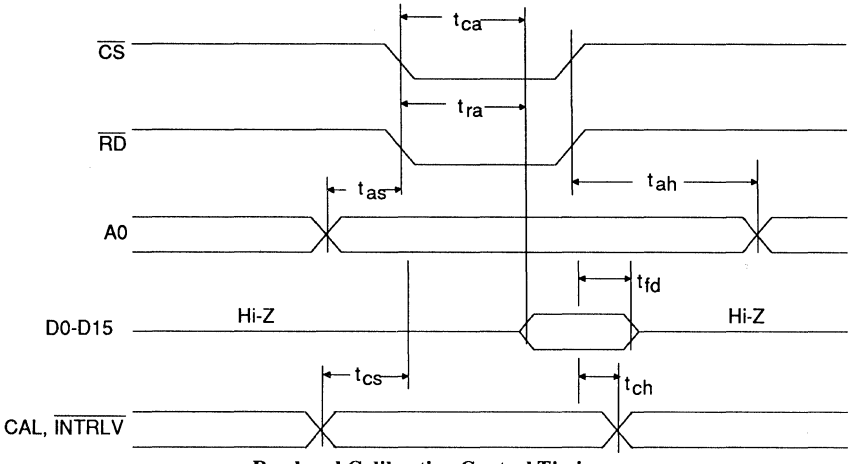
10. $\overline{EOC}$ remains low 4 master clock cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 master clock cycles from the start of a data read operation or a conversion cycle.



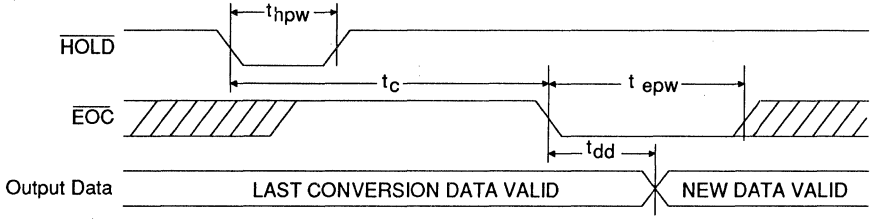
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 11)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 11. I_{out} = -100µA. This specification guarantees TTL compatability (VOH = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 12.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	VA+ - 0.5	V
Analog Input Voltage: (Note 13)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 12. All voltages with respect to ground.

13. The CS5016 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 14)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Note: 14. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guarateed at these extremes.

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.270" by 0.337" (± 0.002").

2. The CS5016-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

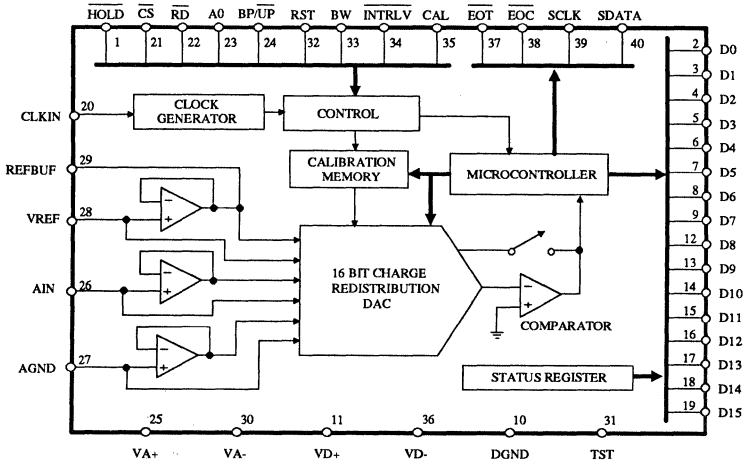
3. Die thickness shall be 0.0175" ± 0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 16.

5. The cavity dimensions for each die within the waffle pack are 0.350" by 0.350".

6. The CS5016-U requires no particular bonding sequence.

7. The CS5016 product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 3000V and 300mA dc latch currents. This meets Crystal's minimum criteria of 2500V and 100mA respectively. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.

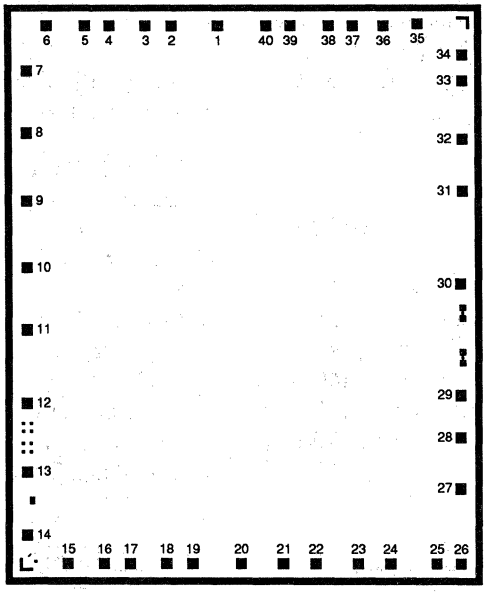


Block Diagram

ORDERING GUIDE

Model Number	Temperature Range	Throughput
CS5016-JU16	0 to 70°C	50kHz
CS5016-JU32	0 to 70°C	26.5kHz
CS5016-SU16	-55 to 125°C	50kHz

Bonding Diagram for CS5016-U



1	-	$\overline{\text{HOLD}}$	21	-	$\overline{\text{CS}}$
2	-	D0	22	-	$\overline{\text{RD}}$
3	-	D1	23	-	A0
4	-	D2	24	-	BP / $\overline{\text{UP}}$
5	-	D3	25	-	VA+
6	-	D4	26	-	AIN
7	-	D5	27	-	AGND
8	-	D6	28	-	VREF
9	-	D7	29	-	REFBUF
10	-	DGND	30	-	VA-
11	-	VD+	31	-	TST
12	-	D8	32	-	RST
13	-	D9	33	-	BW
14	-	D10	34	-	$\overline{\text{INTRLV}}$
15	-	D11	35	-	CAL
16	-	D12	36	-	VD-
17	-	D13	37	-	$\overline{\text{EOT}}$
18	-	D14	38	-	$\overline{\text{EOC}}$
19	-	D15	39	-	SCLK
20	-	CLKIN	40	-	SDATA

CRYSTAL
Semiconductor Corporation

CS5101-U

16-Bit, 100 kHz Serial-Output A/D Converter Die

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 90 dB; THD: 0.002%
- Linearity Error: ± 0.002% FS
- 8.1 µs Conversion Time with 16-bit No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption: 320 mW
  - Power-down Mode: 1 mW

General Description

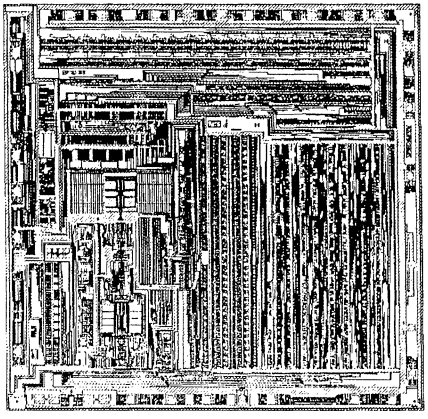
The CS5101 is a 16-bit monolithic CMOS analog-to-digital converter capable of 100 kHz throughput. On-chip self-calibration circuitry achieves nonlinearity of ±0.002% of FS and guarantees 16-bit no missing codes. Superior linearity also leads to 90 dB S/(N+D) with harmonics below 100 dB. Offset and full-scale errors are similarly kept within 2 LSB, eliminating the need for manual calibration.

The CS5101 consists of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, crystal oscillator, comparator, and serial communications port. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input after each conversion within 1.9 µs, allowing throughput rates up to 100 kHz.

The converter's 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION:

Model	Temp Range	Throughput (kHz)
CS5101-JU8	0°C to 70°C	100
CS5101-JU16	0°C to 70°C	50
CS5101-SU8	-55°C to +125°C	100
CS5101-SU16	-55°C to +125°C	50



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Dice Information | CS5101-U dice are functionally identical to packaged CS5101 devices. For general application information, refer to the CS5101 packaged product data sheet.

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ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; Full-Scale Input Sinewave, 1 kHz; f_{clk} = 4 MHz for –16, 8 MHz for –8; f_s = 50 kHz for –16, 100 kHz for –8; Bipolar Mode; FRN Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 200 Ω unless otherwise specified)

Parameter		CS5101 -JU min	CS5101 -JU typ	CS5101 -JU max	CS5101 -SU min	CS5101 -SU typ	CS5101 -SU max	Units
Specified Temperature Range			0 to +70			-55 to +125		°C
Probe Temperature			25			125		°C
Accuracy								
Linearity Error	(Note 1)		0.002			0.002		% FS
	(Note 3) Drift		±1/4			± 1/2		ΔLSB
Differential Linearity	(Note 2, 12)		16			16		Bits
Full Scale Error	(Note 1)		± 2			± 2		LSB
	(Note 3) Drift		± 1			± 2		ΔLSB
Unipolar Offset	(Note 1)		± 1			± 1		LSB
	(Note 3) Drift		± 1			± 2		Δ LSB
Bipolar Offset	(Note 1)		± 1			± 1		LSB
	(Note 3) Drift		± 1			± 2		Δ LSB
Bipolar Negative Full-Scale Error	(Note 1)		± 2			± 2		LSB
	(Note 3) Drift		± 1			± 2		Δ LSB
Dynamic Performance	(Bipolar Mode)							
Peak Harmonic or Spurious Noise								
1kHz Input	(Note 1)		100			100		dB
12kHz Input			88			88		dB
Total Harmonic Distortion			0.002			0.002		%
Signal-to-Noise Ratio								
0dB Input	(Note 1)		90			90		dB
-60dB Input			30			30		dB
Noise (Note 4)	Unipolar Mode		35			35		uV_{rms}
	Bipolar Mode		70			70		uV_{rms}

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Minimum resolution for which no missing codes is guaranteed over the specified temperature range.
3. Total drift over specified temperature range after calibration at power-up at 25 °C.
4. Wideband noise aliased into the baseband. Referred to the input.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

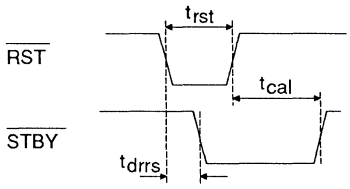
Parameter		Symbol	CS5101-JU min	CS5101-JU typ	CS5101-JU max	CS5101-SU min	CS5101-SU typ	CS5101-SU max	Units
Specified Temperature Range				0 to +70			-55 to +125		°C
Analog Input									
Aperture Time		-		25			25		ns
Aperture Jitter		-		100			100		ps
Input Capacitance (Note 5)	Unipolar Mode	-		320	425		320	425	pF
	Bipolar Mode			200	265		200	265	pF
Conversion & Throughput									
Conversion Time (Notes 6)	−8	t_c			8.12			8.12	us
	−16				16.25			16.25	us
Acquisition Time (Note 7)	−8	t_a			1.88			1.88	us
	−16				3.75			3.75	us
Throughput (Note 8)	−8	f_{tp}		100			100		kHz
	−16			50			50		kHz
Power Supplies									
Power Supply Current									
	Positive Analog	I_{A+}		21	25		21	25	mA
$\overline{\text{SLEEP}}$ High)	Negative Analog	I_{A-}		−21	−25		−21	−25	mA
	Positive Digital	I_{D+}		11	15		11	15	mA
(Note 9)	Negative Digital	I_{D-}		−11	−15		−11	−15	mA
Power Dissipation									
	($\overline{\text{SLEEP}}$ High)	P_{do}		320	400		320	400	mW
(Notes 9, 10)	($\overline{\text{SLEEP}}$ Low)	P_{ds}		1			1		mW
Power Supply Rejection									
(Note 11)	Positive Supplies	PSR		84			84		dB
	Negative Supplies			84			84		dB

Notes:
5. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
6. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of $\overline{\text{HOLD}}$ and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.
7. The CS5101 requires 6 clock cycles of coarse charge, followed by a minimum of 1.125 µs of fine charge FRN mode allows 9 clock cycles for fine charge which provides for the minimum 1.125 µs with an 8 MHz clock, however; in PDT, RBT, or SSC modes, at clock frequencies less than 8 MHz, fine charge may be less than 9 clock cycles. This reflects the typ. specification (6 clock cycles + 1.125 µs).
8. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described above.
9. All outputs unloaded. All inputs CMOS levels.
10. Power dissipation in the sleep mode applies with no master clock applied (CLKIN held high or low).
11. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB.

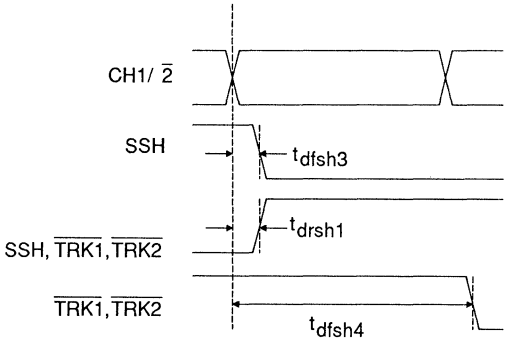
SWITCHING CHARACTERISTICS (TA=T_{MIN} to T_{MAX}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter			Symbol	Min	Typ	Max	Units
CLKIN Period	(Note 12)	-8 -16	t_{clk}	125 250	–	10,000 10,000	ns ns
CLKIN Low time			t_{clkl}	37.5	–	–	ns
CLKIN High time			t_{clkh}	37.5	–	–	ns
Crystal Frequency	(Note 13)	-8 -16	f_{xtal}	2.0 2.0	– –	8.0 4.0	MHz MHz
$\overline{SLEEP}$ Rising to Oscillator Stable		(Note 14)	–	–	2	–	ms
$\overline{RST}$ Pulse Width			t_{rst}	150	–	–	ns
$\overline{RST}$ to $\overline{STBY}$ Falling			t_{drrs}	–	100	–	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising			t_{cal}	–	11,528,160	–	t_{clk}
CH1/$\overline{2}$ edge to SSH falling		(Note 15)	t_{dfsh3}	–	40	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ rising		(Note 15)	t_{drsh1}	–	80	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ falling		(Note 15)	t_{dfsh4}	–	–	66 t_{clk} + 260	ns
$\overline{HOLD}$ to SSH Falling		(Note 16)	t_{dfsh2}	–	60	–	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, Falling		(Note 16)	t_{dfsh1}	66t_{clk}	–	68t_{clk} + 260	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, SSH Rising		(Note 16)	t_{drsh}	–	120	–	ns
$\overline{HOLD}$ Pulse Width			t_{hold}	130	–	64t_{clk}	ns
$\overline{HOLD}$ to CH1/$\overline{2}$ Edge		(Note 16)	t_{dhlri}	–30	–	64t_{clk}	ns
CLKIN Falling to $\overline{HOLD}$ Falling		(Note 17)	t_{cfh}	–	–	-10	ns
$\overline{HOLD}$ FALLING to CLKIN Falling		(Note 17)	t_{hcf}	55	–	–	ns

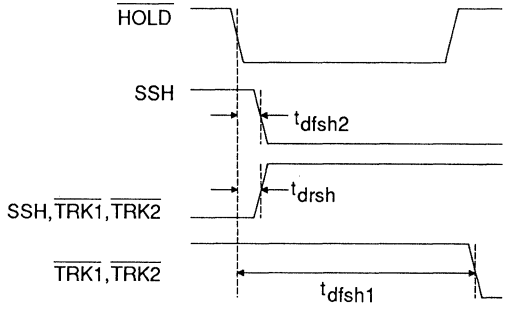
Note:
12. Clock speeds of less than 1MHz, at temperatures >100°C, will degrade DNL performance.
13. External loading capacitors are required to allow the crystal to oscillate.
14. With 8MHz crystal, two 10 pF loading capacitors and a 10 MΩ parallel resistor (see Figure 8).
15. These times are for FRN mode.
16. SSH only works correctly if $\overline{HOLD}$ falling edge is within ±30ns of CH1/$\overline{2}$ edge or if CH1/$\overline{2}$ edge occurs between 30 ns before $\overline{HOLD}$ rises to 64 t_{clk} after $\overline{HOLD}$ has fallen. These times are for SSC, PDT and RBT modes.
17. When $\overline{HOLD}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{HOLD}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{HOLD}$ is latched



Reset and Calibration Timing



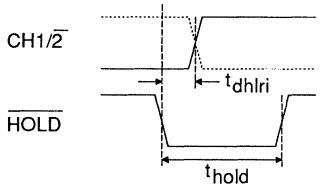
a. FRN mode



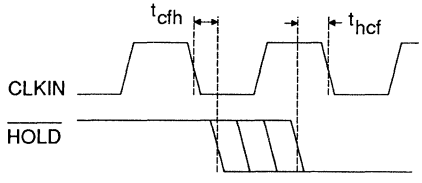
b. SSC, PDT, RBT mode

Control Output Timing

9



Channel Selection Timing



Start Conversion Timing

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Input Pulse Period	t_{sclk}	200	–	–	ns
SCLK Input Pulse Width Low	t_{sclkl}	50	–	–	ns
SCLK Input Pulse Width High	t_{sclkh}	50	–	–	ns
SCLK Input Falling to SDATA Valid	t_{dss}	–	100	150	ns
SCLK Output Pulse Width Low	t_{slkl}	–	$2t_{clk}$	–	t_{clk}
SCLK Output Pulse Width High	t_{slkh}	–	$2t_{clk}$	–	t_{clk}
SDATA valid before rising SCLK	t_{ss}	$2t_{clk}$ - 100	–	–	ns
SDATA valid after rising SCLK	t_{sh}	$2t_{clk}$ - 100	–	–	ns
$\overline{HOLD}$ falling to 1st falling SCLK	t_{hfs}	$6t_{clk}$	–	$8t_{clk}$ + 165	ns
CH1/$\overline{2}$ edge to 1st falling SCLK	t_{chfs}	–	$7t_{clk}$	–	t_{clk}
$\overline{HOLD}$ falling to SDATA Valid PDT mode	t_{dhs}	–	140	230	ns
$\overline{TRK1}$, $\overline{TRK2}$ Falling to SDATA Valid (Note 18)	t_{dts}	–	65	125	ns

Note: 18. Only valid tor $\overline{TRK1}$, $\overline{TRK2}$ falling when SCLK is low. If SCLK is high when $\overline{TRK1}$, $\overline{TRK2}$ fall, then SDATA is valid t_{dss} time after the next falling SCLKI.

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention (Note 19) Power Supply Voltage VA+ and VD+	V_{MR}	2.0	-	-	V
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 20)	V_{OH}	(VD+) - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 21)	I_{in}	-	-	60	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 19, VA- and VD- can be any value from zero to -5V for memory retention. Neither VA- or VD- should be allowed to go positive. AIN1, AIN2 or VREF must not be greater than VA+ or VD+. This parameter is guaranteed by characterization.

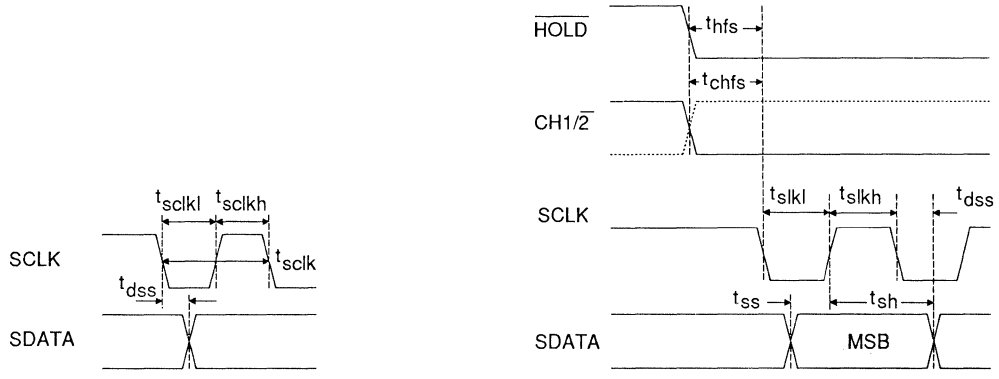
20. I_{OUT} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ Iout = -40 µA).
21. All digital inputs except CLKIN and SCLK have internal pull-up devices, nominally 200 kΩ.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 22.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage: (Note 23)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 22. All voltages with respect to ground.

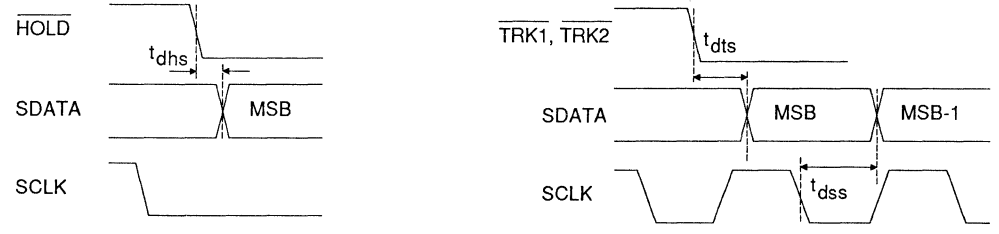
23. The CS5101 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.



a. SCLK input (RBT and PDT mode)

b. SCLK output (SSC and FRN modes)

Serial Data Timing



a. Pipelined Data Transmission (PDT) Mode

b. Register Burst Transmission (RBT) Mode

Data Transmission Timing

ABSOLUTE MAXIMUM RATINGS* (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 24)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	−0.3	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	−55	125	°C
Storage Temperature		T_{stg}	−65	150	°C

Note: 24. Transient currents of up to 100 mA will not cause SCR latch-up.

*WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

9

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document include information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.277" by 0.280" (± 0.002")

2. The CS5101-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

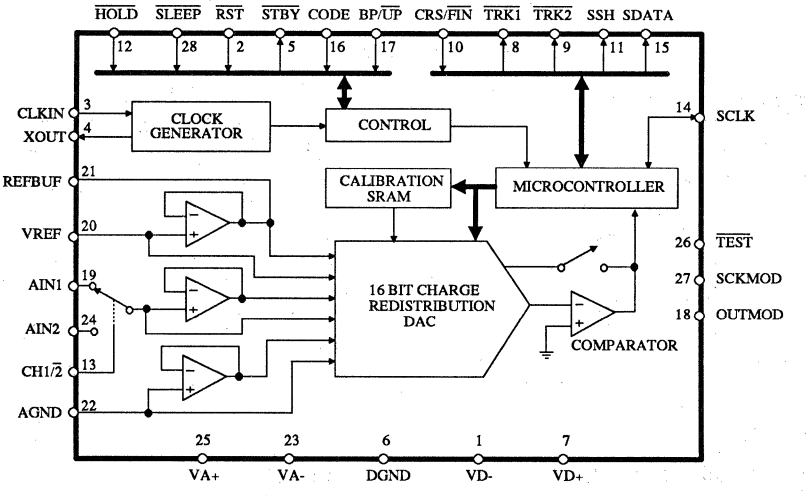
3. Die thickness shall be 0.0175" ±0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 25.

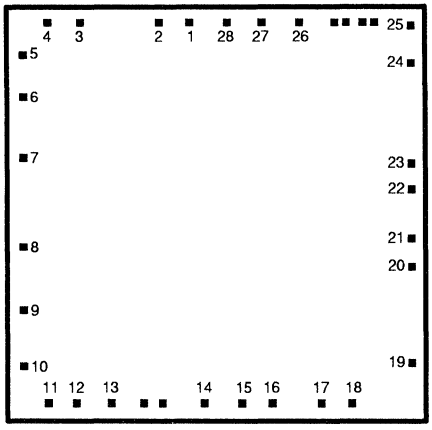
5. The cavity dimensions for each die within the waffle pack are .300" by .300" (Waffle Pack Type H20-300).

6. The CS5101-U requires no particular bonding sequence.

7. The CS5101-U product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 3000V and 300mA dc latch currents. This meets Crystal's minimum criteria of 2500V and 100mA respectively. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.



Bond Pad Locations for CS5101-U



1 - VD-
2 - $\overline{\text{RST}}$
3 - CLKIN
4 - XOUT
5 - $\overline{\text{STBY}}$
6 - DGND
7 - VD+
8 - $\overline{\text{TRK1}}$
9 - $\overline{\text{TRK2}}$
10 - CRS/$\overline{\text{FIN}}$
11 - $\overline{\text{SSH}}$
12 - $\overline{\text{HOLD}}$
13 - CH1/$\overline{2}$
14 - SCLK
15 - SDATA
16 - $\overline{\text{CODE}}$
17 - BP/$\overline{\text{UP}}$
18 - OUTMOD
19 - AIN1
20 - VREF
21 - REFBUF
22 - AGND
23 - VA-
24 - AIN2
25 - VA+
26 - $\overline{\text{TEST}}$
27 - SCKMOD
28 - $\overline{\text{SLEEP}}$

•Notes•

CRYSTAL
Semiconductor Corporation

CS5102-U

16-Bit, 20 kHz Serial-Output A/D Converter Die

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 90 dB; THD: 0.002%
- Linearity Error: ± 0.002% FS
- 40 µs Conversion Time with 16-bit No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption: 44 mW
  - Power-down Mode: 1 mW

General Description

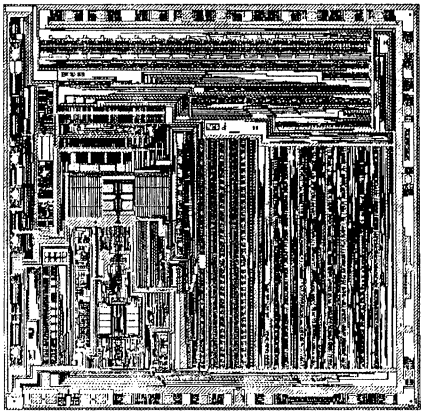
The CS5102 is a 16-bit monolithic CMOS analog-to-digital converter capable of 20 kHz throughput. On- chip self-calibration circuitry achieves nonlinearity of ±0.002% of FS and guarantees 16-bit no missing codes. Superior linearity also leads to 90 dB S/(N+D) with harmonics below 100 dB. Offset and full-scale errors are similarly kept within 2 LSB, eliminating the need for manual calibration of any kind.

The CS5102 consists of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, crystal oscillator, comparator, and serial communications port. The input track-and-hold, inherent to the device's sampling architecture, acquires the analog input after each conversion, allowing throughput rates up to 20 kHz.

The converter's 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION:

Model	Temp Range
CS5101-JU	0°C to 70°C
CS5101-SU	-55°C to +125°C



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Dice Information | CS5102-U dice are functionally identical to packaged CS5102 devices. For general application information, refer to the CS5102 packaged product data sheet.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; Full-Scale Input Sinewave, 200 Hz; CLKIN = 1.6MHz; f_s = 20 kHz; Bipolar Mode; SSC Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 200 Ω with 1000pF to AGND unless otherwise specified)

Parameter		CS5102 -JU min	CS5102 -JU typ	CS5102 -JU max	CS5102 -SU min	CS5102 -SU typ	CS5102 -SU max	Units
Specified Temperature Range			0 to +70			-55 to +125		°C
Probe Temperature			25			125		°C
Accuracy								
Linearity Error	(Note 1)		0.002			0.002		% FS
	(Note 3) Drift		± 1/4			± 1/2		ΔLSB
Differential Linearity	(Note 2, 12)		16			16		Bits
Full Scale Error	(Note 1)		± 2			± 2		LSB
	(Note 3) Drift		± 1			± 2		ΔLSB
Unipolar Offset	(Note 1)		± 1			± 1		LSB
	(Note 3) Drift		± 1			± 2		ΔLSB
Bipolar Offset	(Note 1)		± 1			± 1		LSB
	(Note 3) Drift		± 1			± 2		ΔLSB
Bipolar Negative Full-Scale Error	(Note 1)		± 2			± 2		LSB
	(Note 3) Drift		± 1			± 2		ΔLSB
Dynamic Performance	(Bipolar Mode)							
Peak Harmonic or Spurious Noise 100 Hz Input	(Note 1)		100			100		dB
Total Harmonic Distortion			0.002			0.002		%
Signal-to-Noise Ratio								
0dB Input	(Note 1)		90			90		dB
-60dB Input			30			30		dB
Noise (Note 4)	Unipolar Mode		35			35		uV rms
	Bipolar Mode		70			70		uV rms

Notes:
1. Applies after calibration at any temperature within the specified temperature range.
2. Minimum resolution for which no missing codes is guaranteed over the specified temperature range.
3. Total drift over specified temperature range after calibration at power-up at 25 °C.
4. Wideband noise aliased into the baseband. Referred to the input.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	CS5102-JU min	CS5102-JU typ	CS5102-JU max	CS5102-SU min	CS5102-SU typ	CS5102-SU max	Units
Specified Temperature Range				0 to +70			-55 to +125		°C
Analog Input									
Aperture Time		-		25			25		ns
Aperture Jitter		-		100			100		ps
Input Capacitance (Note 5)	Unipolar Mode	-		320	425		320	425	pF
	Bipolar Mode			200	265		200	265	pF
Conversion & Throughput									
Conversion Time	(Notes 6)	t_c			40.625			40.625	us
Acquisition Time	(Note 7)	t_a			9.375			9.375	us
Throughput	(Note 8)	f_{tp}	20			20			kHz
Power Supplies									
Power Supply Current									
	Positive Analog	I_{A+}		2.4	3.5		2.4	3.5	mA
$\overline{\text{SLEEP}}$ High)	Negative Analog	I_{A-}		−2.4	−3.5		−2.4	−3.5	mA
	Positive Digital	I_{D+}		2.5	3.5		2.5	3.5	mA
(Note 9)	Negative Digital	I_{D-}		−1.5	−2.5		−1.5	−2.5	mA
Power Dissipation									
	($\overline{\text{SLEEP}}$ High)	P_{do}		44	65		44	65	mW
(Notes 9, 10)	($\overline{\text{SLEEP}}$ Low)	P_{ds}		1			1		mW
Power Supply Rejection									
(Note 11)	Positive Supplies	PSR		84			84		dB
	Negative Supplies			84			84		dB

Notes:
5. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
6. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of $\overline{\text{HOLD}}$ and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.
7. The CS5102 requires 6 clock cycles of coarse charge, followed by a minimum of 5.625 µs of fine charge FRN mode allows 9 clock cycles for fine charge which provides for the minimum 5.625 µs with an 1.6 MI clock, however; in PDT, RBT, or SSC modes, at clock frequencies less than 1.6MHz, fine charge may be less than 9 clock cycles.
8. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described above.
9. All outputs unloaded. All inputs CMOS levels. See Table below for power dissipation vs. clock frequency
10. Power dissipation in the sleep mode applies with no master clock applied (CLKIN held high or low).
11. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB.

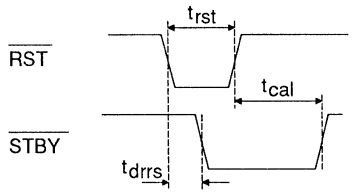
Typ. Power (mW)	CLKIN (MHz)
34	0.8
37	1.0
39	1.2
41	1.4
44	1.6

9

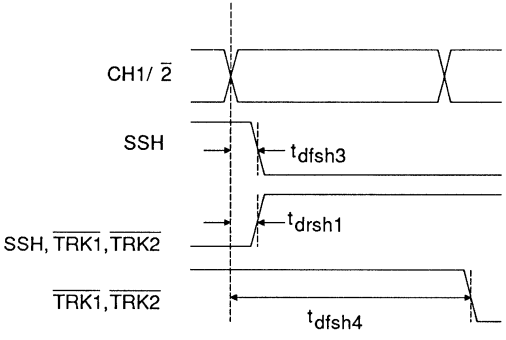
SWITCHING CHARACTERISTICS (TA=T_{MIN} to T_{MAX};
VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Period	(Note 12)	t_{clk}	1.25	–	10	us
CLKIN Low time		t_{clkl}	375	–	–	ns
CLKIN High time		t_{clkh}	375	–	–	ns
Crystal Frequency	(Note 13)	f_{xtal}	TBD	–	800	kHz
$\overline{SLEEP}$ Rising to Oscillator Stable	(Note 14)	–	–	20	–	ms
$\overline{RST}$ Pulse Width		t_{rst}	240	–	–	ns
$\overline{RST}$ to $\overline{STBY}$ Falling		t_{drrs}	–	100	–	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising		t_{cal}	–	2,882,040	–	t_{clk}
CH1/$\overline{2}$ edge to SSH falling	(Note 15)	t_{dfsh3}	–	40	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ rising	(Note 15)	t_{drsh1}	–	80	–	ns
CH1/$\overline{2}$ edge to SSH, $\overline{TRK1}$,$\overline{TRK2}$ falling	(Note 15)	t_{dfsh4}	–	–	66 t_{clk} + 260	ns
$\overline{HOLD}$ to SSH Falling	(Note 16)	t_{dfsh2}	–	60	–	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, Falling	(Note 16)	t_{dfsh1}	66t_{clk}	–	68t_{clk} + 260	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, SSH Rising	(Note 16)	t_{drsh}	–	120	–	ns
$\overline{HOLD}$ Pulse Width		t_{hold}	130	–	64t_{clk}	ns
$\overline{HOLD}$ to CH1/$\overline{2}$ Edge	(Note 16)	t_{dhlri}	-30	–	64t_{clk}	ns
CLKIN Falling to $\overline{HOLD}$ Falling	(Note 17)	t_{cfh}	–	–	-10	ns
$\overline{HOLD}$ FALLING to CLKIN Falling	(Note 17)	t_{hcf}	55	–	–	ns

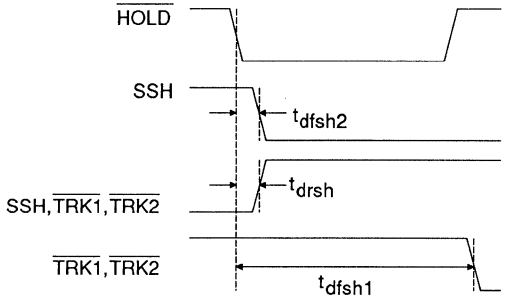
Note: 12. Clock speeds of less than 1.0 MHz, at temperatures >100°C, will degrade DNL performance.
13. External loading capacitors are required to allow the crystal to oscillate.
14. With a 1.6 MHz crystal, two 47 pF loading capacitors and a 10 MΩ parallel resistor (see Figure 8).
15. These times are for FRN mode.
16. SSH only works correctly if $\overline{HOLD}$ falling edge is within ±30ns of CH1/$\overline{2}$ edge or if CH1/$\overline{2}$ edge occurs between 30 ns before $\overline{HOLD}$ rises to 64 t_{clk} after $\overline{HOLD}$ has fallen. These times are for SSC, PDT, and RBT modes.
17. When $\overline{HOLD}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{HOLD}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{HOLD}$ is latched



Reset and Calibration Timing

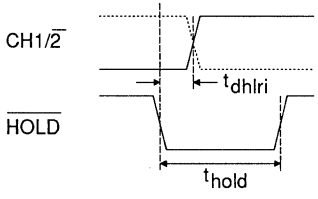


a. FRN mode

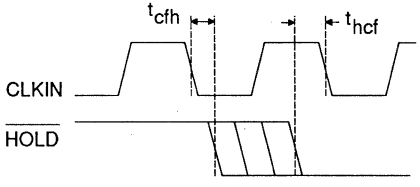


b. SSC, PDT, RBT mode

Control Output Timing



Channel Selection Timing



Start Conversion Timing

SWITCHING CHARACTERISTICS (Continued)

Parameter	Symbol	Min	Typ	Max	Units
SCLK Input Pulse Period	t_{sclk}	200	–	–	ns
SCLK Input Pulse Width Low	t_{sclkl}	50	–	–	ns
SCLK Input Pulse Width High	t_{sclkh}	50	–	–	ns
SCLK Input Falling to SDATA Valid	t_{dss}	–	100	150	ns
SCLK Output Pulse Width Low	t_{slkl}	–	$2t_{clk}$	–	t_{clk}
SCLK Output Pulse Width High	t_{slkh}	–	$2t_{clk}$	–	t_{clk}
SDATA valid before rising SCLK	t_{ss}	$2t_{clk}$ - 100	–	–	ns
SDATA valid after rising SCLK	t_{sh}	$2t_{clk}$ - 100	–	–	ns
$\overline{HOLD}$ falling to 1st falling SCLK	t_{hfs}	$6t_{clk}$	–	$8t_{clk}$ + 165	ns
CH1/$\overline{2}$ edge to 1st falling SCLK	t_{chfs}	–	$7t_{clk}$	–	t_{clk}
$\overline{HOLD}$ falling to SDATA Valid PDT mode	t_{dhs}	–	140	230	ns
$\overline{TRK1}$, $\overline{TRK2}$ Falling to SDATA Valid (Note 18)	t_{dts}	–	65	125	ns

Note: 18. Only valid tor $\overline{TRK1}$, $\overline{TRK2}$ falling when SCLK is low. If SCLK is high when $\overline{TRK1}$, $\overline{TRK2}$ fall, then SDATA is valid t_{dss} time after the next falling SCLKI.

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention (Note 19) Power Supply Voltage VA+ and VD+	V_{MR}	2.0	-	-	V
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 20)	V_{OH}	(VD+) - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current (Note 21)	I_{in}	-	-	60	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 19, VA- and VD- can be any value from zero to -5V for memory retention. Neither VA- or VD- should be allowed to go positive. AIN1, AIN2 or VREF must not be greater than VA+ or VD+. This parameter is guaranteed by characterization.

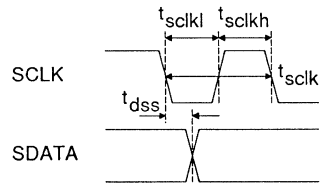
20. I_{OUT} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ Iout = -40 µA).
21. All digital inputs except CLKIN and SCLK have internal pull-up devices, nominally 200 kΩ.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 22.)

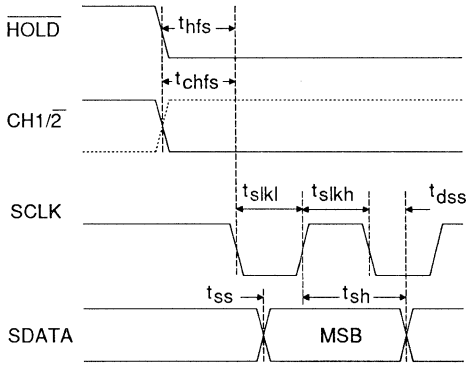
Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage: (Note 23)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 22. All voltages with respect to ground.

23. The CS5102 can accept input voltages up to the analog supplies (VA+ and VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode with binary coding (CODE=low).

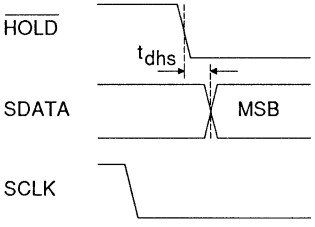


a. SCLK input (RBT and PDT mode)

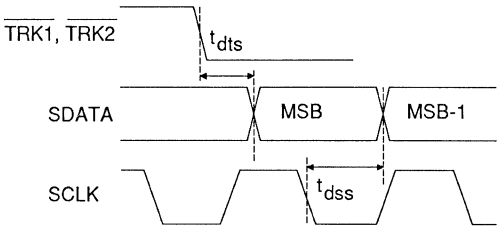


b. SCLK output (SSC and FRN modes)

Serial Data Timing



a. Pipelined Data Transmission (PDT) Mode



b. Register Burst Transmission (RBT) Mode

Data Transmission Timing

ABSOLUTE MAXIMUM RATINGS* (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	(VA+) + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 24)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage		V_{IND}	−0.3	(VD+) + 0.3	V
Ambient Operating Temperature		T_A	−55	125	°C
Storage Temperature		T_{stg}	−65	150	°C

Note: 24. Transient currents of up to 100 mA will not cause SCR latch-up.

*WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

9

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document include information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.277" by 0.280" (± 0.002")

2. The CS5102-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

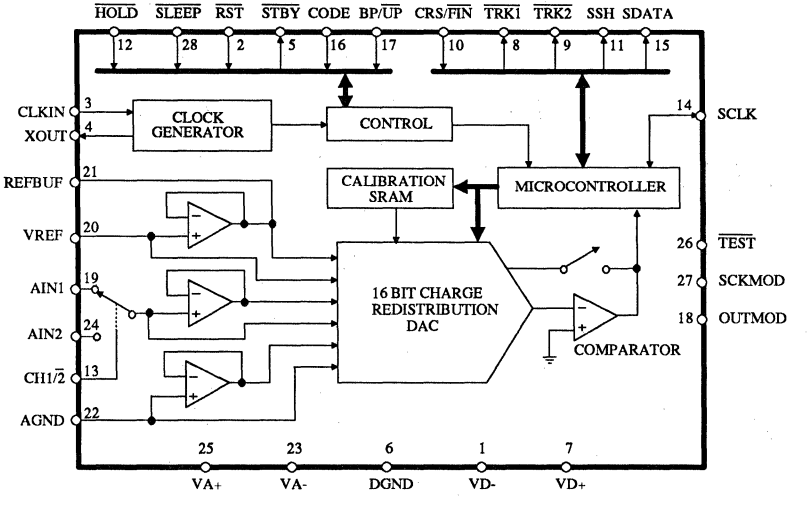
3. Die thickness shall be 0.0175" ±0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 25.

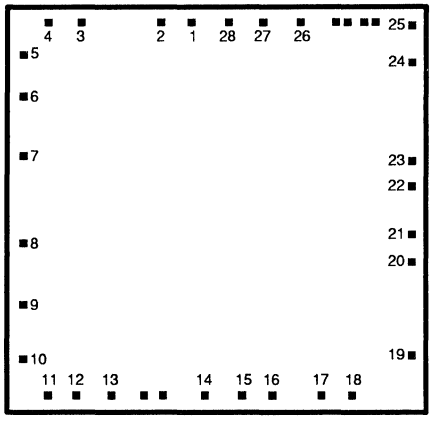
5. The cavity dimensions for each die within the waffle pack are .300" by .300" (Waffle Pack Type H20-300).

6. The CS5102-U requires no particular bonding sequence.

7. The CS5102-U product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 3000V and 300mA dc latch currents. This meets Crystal's minimum criteria of 2500V and 100mA respectively. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.



Bond Pad Locations for CS5102-U



1 - VD-
2 - $\overline{\text{RST}}$
3 - CLKIN
4 - XOUT
5 - $\overline{\text{STBY}}$
6 - DGND
7 - VD+
8 - $\overline{\text{TRK1}}$
9 - $\overline{\text{TRK2}}$
10 - CRS/$\overline{\text{FIN}}$
11 - $\overline{\text{SSH}}$
12 - $\overline{\text{HOLD}}$
13 - CH1/$\overline{2}$
14 - SCLK
15 - SDATA
16 - $\overline{\text{CODE}}$
17 - BP/$\overline{\text{UP}}$
18 - OUTMOD
19 - AIN1
20 - VREF
21 - REFBUF
22 - AGND
23 - VA-
24 - AIN2
25 - VA+
26 - $\overline{\text{TEST}}$
27 - SCKMOD
28 - $\overline{\text{SLEEP}}$

•Notes•

CRYSTAL
Semiconductor Corporation

CS5317-U

16-Bit, 20 kHz Oversampling A/D Converter Die

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track & Hold Amplifier
  - On-Chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

General Description

The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

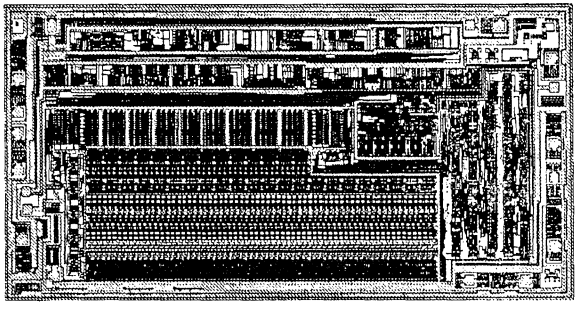
An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION:

CS5317-KU 0 to 70 °C
CS5317-TU -55 to 125 °C



9

Dice Information | CS5317-U dice are functionally identical to packaged CS5317 devices. For general application information, refer to the CS5317 packaged product data sheet.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ - T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; CLKIN = 4.9152 MHz in CLKOR mode; 1kHz Input Sinewave; with 1.2 kΩ, .01 µF antialiasing filter.)

Parameter		CS5317-KU min	CS5317-KU typ	CS5317-KU max	CS5317-TU min	CS5317-TU typ	CS5317-TU max	Units
Resolution			16			16		Bits
Specified Temperature Range			0 to 70			-55 to +125		°C
Probe Test Temperature			25			125		°C
Dynamic Performance								
Dynamic Range	(Note 1)		84			84		dB
Total Harmonic Distortion			80			80		dB
Signal to Intermodulation Distortion			84			84		dB
dc Accuracy								
Differential Nonlinearity	(Note 2)		± 0.4			± 0.4		LSB
Positive Full-Scale Error			± 150			± 150		mV
Positive Full-Scale Drift			± 500			± 500		uV/°C
Bipolar Offset Error			± 10			± 10		mV
Bipolar Offset Drift			± 50			± 50		uV/°C
Filter Characteristics								
Absolute Group Delay	(Note 3)		78.125			78.125		us
Passband Frequency	(Note 4)		5			5		kHz
Input Characteristics								
AC Input Impedance (1kHz)			80			80		kohms
Analog Input Full Scale Signal Level			± 2.75			± 2.75		V
Power Supplies								
Power Dissipation	(Note 5)		220	300		220	300	mW
Power Supply Rejection	VA+ (Note 6)		60			60		dB
	VA-		45			45		dB
	VD+		60			60		dB
	VD-		55			55		dB

Notes:
1. Measured over the full 0 to 9.6kHz band with a -20dB input and extrapolated to full-scale. Since this includes energy in the stopband above 5kHz, additional post-filtering at the CS5317's output can typically achieve 88dB dynamic range by improving rejection above 5kHz. This can be increased to 90dB by bandlimiting the output to 2.5kHz.
2. No missing codes is guaranteed by design.
3. Group delay is constant with respect to input analog frequency; that is, the digital FIR filter has linear phase. Group delay is determined by the formula D_{grp} = 384/CLKIN in CLKOR mode, or 192/CLKOUT in any mode.
4. The digital filter's frequency response scales with the master clock. Its -3dB point is determined by f_{-3dB} = CLKIN/977.3 in CLKOR mode, or CLKOUT/488.65 in any mode.
5. All outputs unloaded. All inputs CMOS levels.
6. With 300mV p-p, 1kHz ripple applied to each supply separately.

ANALOG CHARACTERISTICS (Continued)

Parameter	CS5317-KU min	CS5317-KU typ	CS5317-KU max	CS5317-TU min	CS5317-TU typ	CS5317-TU max	Units
Specified Temperature Range		0 to 70			-55 to +125		°C
Phase-Lock Loop Characteristics		-4V < PHDT = VCOIN < 3V					
VCO Gain Constant, Ko (Note 7)	-4	-10	-30	-4	-10	-30	M rad/Vs
VCO operating frequency	1.28		5.12	1.28		5.12	MHz
Phase Detector Gain Control, Kd	-5	-8	-12	-5	-8	-12	ua/rad
Phase Detector Prop. Delay (Note 8)		50	100		50	100	ns

Notes: 7. Over 1.28 MHz to 5.12 MHz VCO output range, where VCO frequency = 2 * CLKOUT.
8. Delay from an input edge to the phase detector to a response at the PHDT output.

DIGITAL CHARACTERISTICS ($T_A = T_{MIN} - T_{MAX}$; VA+ , VD+ = 5V ±10%; VA-, VD- = -5V ±10%)

All measurements performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 9)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 9. I_{out}=-100µA. This specification guarantees the ability to drive one TTL load (V_{OH}=2.4V @ I_{out}=-40µA.).

9

RECOMMENDED OPERATING CONDITIONS (DGND, AGND = 0 V)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies: (All voltages with respect to ground)	Positive Digital	VD+	4.5	5.0	5.5	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Master Clock Frequency (Note 10)		f_{clk}	0.10	-	5.12	MHz

Note: 10. Minimum clock speed 0.10 MHz guaranteed by characterization.

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A=T_{MIN}-T_{MAX};C_L= 50 pF; VD+ = 5V ±10%;VD- = -5V ±10%)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency: CLKIN						
	CLKG1 Mode	f_{clkg1}	-	-	20	kHz
	CLKG2 Mode	f_{clkg2}	-	-	10	kHz
	CLKOR Mode	f_{clkor}	-	-	5.12	MHz
Output Word Rate: $\overline{DOUT}$		f_{dout}	-	-	20	kHz
Rise Times:	Any Digital Input	t_{risein}	-	20	1000	ns
	Any Digital Output	$t_{riseout}$	-	15	20	ns
Fall Times:	Any Digital Input	t_{fallin}	-	20	1000	ns
	Any Digital Output	$t_{fallout}$	-	15	20	ns
CLKIN Duty Cycle						
CLKG1 and CLKG2 Modes	Pulse Width Low	t_{pwl1}	200	-	-	ns
	Pulse Width High	t_{pwh1}	200	-	-	ns
CLKOR Mode	Pulse Width Low	t_{pwl1}	45	-	-	ns
	Pulse Width High	t_{pwh1}	45	-	-	ns
$\overline{RST}$ Pulse Width Low		t_{pwr}	400	-	-	ns
Set Up Times:						
	$\overline{RST}$ High to CLKIN High	t_{su1}	40	-	-	ns
	CLKIN High to $\overline{RST}$ High	t_{su2}	40	-	-	ns
Propagation Delays:						
$\overline{DOE}$ Falling to Data Valid		t_{phl1}	-	-	150	ns
CLKIN Rising to $\overline{DOUT}$ Falling	(Note 11)	t_{phl2}	-	1	-	CLKOUT cycle
$\overline{DOE}$ Rising to Hi-Z Output		t_{plh1}	-	-	80	ns
CLKOUT Rising to $\overline{DOUT}$ Falling		t_{plh2}	-	-	60	ns
CLKOUT Rising to $\overline{DOUT}$ Rising		t_{plh3}	-	-	60	ns
CLKOUT Rising to Data Valid		t_{plh4}	-	-	100	ns
CLKIN Rising to CLKOUT Falling	(Note 12)	t_{plh5}	-	-	200	ns
CLKIN Rising to CLKOUT Rising	(Note 12)	t_{plh6}	-	-	200	ns

Notes: 11. CLKIN only pertains to CLKG1 and CLKG2 modes.
12. Only valid in CLKOR mode.

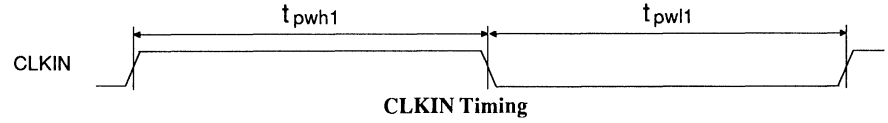
ABSOLUTE MAXIMUM RATINGS (DGND, AGND = 0 V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pad Except Supplies	(Note 13)	I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VD+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

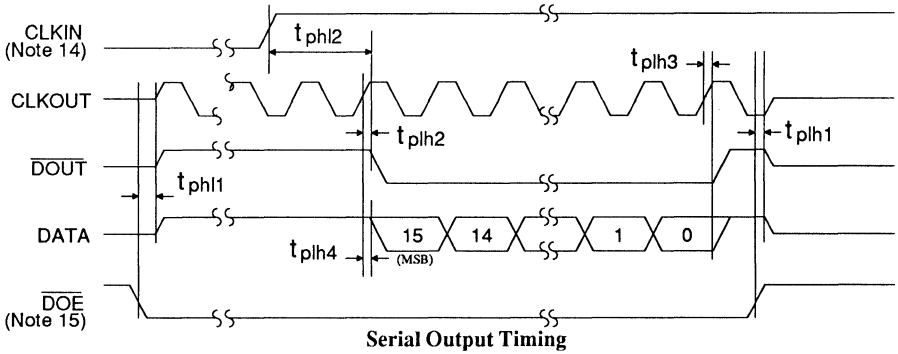
Note: 13. Transient currents up to 100mA will not cause SCR latch-up.

WARNING: Operating this device at or beyond these extremes may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

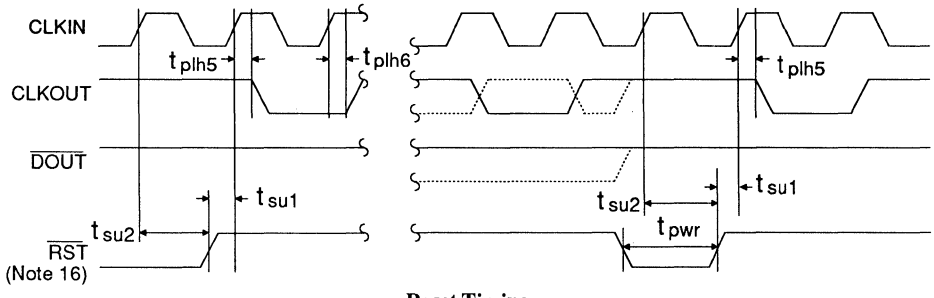
Rise and Fall Times



CLKIN Timing



Serial Output Timing



Reset Timing

Notes: 14. CLKIN only pertains to CLKG1 and CLKG2 modes.
15. If $\overline{DOE}$ is brought high during serial data transfer, CLKOUT, $\overline{DOUT}$, and DATA will immediately 3-state and the rest of the serial data is lost.
16. $\overline{RST}$ must be held high except in the clock override (CLKOR) mode where it can be used to align the phases of all internal clocks.

9

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.135" by 0.269" (± 0.002").

2. The CS5317-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

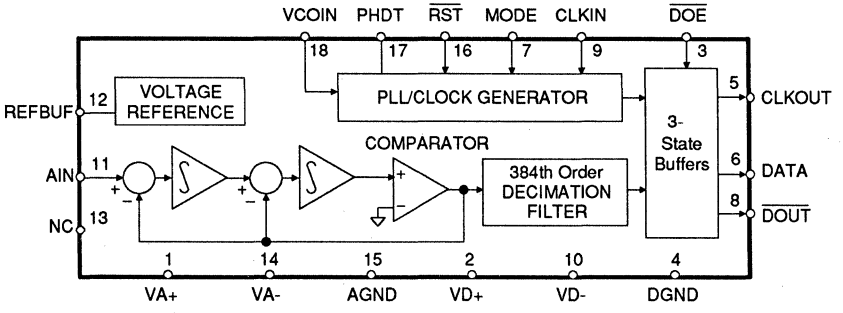
3. Die thickness shall be 0.0175" ±0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 28.

5. The cavity dimensions for each die within the waffle pack are 0.180" by 0.330". Exterior waffle pack dimensions are 2.0" by 2.0".

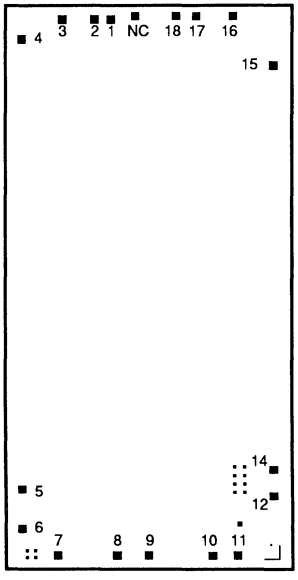
6. The CS5317-U requires no particular bonding sequence.

7. The CS317-U product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 1500V and 200mA dc latch currents.



Block Diagram

Bonding Diagram for CS5317-U



1	-	VA+	10	-	VD-
2	-	VD+	11	-	AIN
3	-	$\overline{\text{DOE}}$	12	-	REF BUF
4	-	DGND	13	-	NO CONNECT
5	-	CLKOUT	14	-	VA-
6	-	DATA	15	-	AGND
7	-	MODE	16	-	$\overline{\text{RST}}$
8	-	$\overline{\text{DOUT}}$	17	-	PHDT
9	-	CLKIN	18	-	VCOIN

•Notes•

Semiconductor Corporation

CS5412-U

12-Bit, 1MHz Self-Calibrating A/D Converter Die

Features

- Monolithic CMOS Sampling ADC
  On-Chip Track and Hold Amplifier
  Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  Typical Nonlinearity: 3/4 LSB
  No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.0125%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 750mW

General Description

The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acquisition and settling times as well as overlapped conversion cycles.

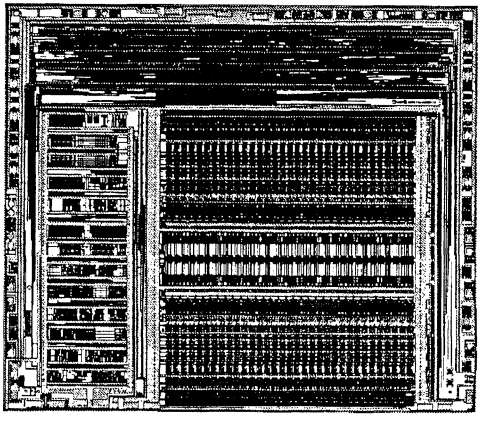
Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board for the packaged part is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

ORDERING INFORMATION:

CS5412-JU 0° to 70°C
CS5412-SU -55° to 125°C



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Dice Information	CS5412-U dice are functionally identical to packaged CS5412 devices. Refer to the CS5412 packaged product data sheet for general application information

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ANALOG CHARACTERISTICS (T_A = 25°C (Note 1); All VA+ pins, VD+ = 5V; All VA- pins, VD- = -5V; VREF+ = +1.5V; VREF- = -1.5V; f_{CLK} = 8MHz; 100 kHz Full Scale Input Sinewave; Continuous Convert Mode unless otherwise specified).

Parameter	CS5412-JU min	CS5412-JU typ	CS5412-JU max	CS5412-SU min	CS5412-SU typ	CS5412-SU max	Units
Resolution	12			12			Bits
Specified Temperature Range		0 to 70			-55 to +125		°C
Probe Test Temperature		25			125		°C
Dynamic Performance							
Peak Harmonic or Spurious Noise							
T_{min} to T_{max} (Note 1) 100kHz Input		82			82		dB
T_{min} to T_{max} (Note 1) 490kHz Input		70			70		dB
Total Harmonic Distortion		0.0125			0.0125		%
Signal-to-(Noise plus Distortion)							
T_{min} to T_{max} (Note 1) 0dB Input (Full Scale)		71			71		dB
T_{min} to T_{max} (Note 1) -40dB Input		32			32		dB
dc Accuracy							
Linearity Error (Note 1) Tmin to T_{max}		± 3/4			± 1		LSB
Differential Linearity (Note 1) Tmin to T_{max}		± 1/2			± 1/2		LSB
Full Scale Error T_{min} to T_{max}		± 2			± 3		LSB
Offset Error T_{min} to T_{max}		± 1.5			± 1.5		LSB

Notes: 1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest. Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter	CS5412-JU min	CS5412-JU typ	CS5412-JU max	CS5412-SU min	CS5412-SU typ	CS5412-SU max	Units
Analog Input							
Aperture Time		35			35		ns
Aperture Jitter		50			50		ps, rms
Input Bandwidth							
Small Signal, -3dB (Note 2)		4			4		MHz
Full Power, -3dB		3.5			3.5		MHz
Analog Input Impedance at dc		10			10		Mohms
Input Capacitance VREF- pin		50			50		pF
AIN, VREF+ pins		10			10		pF
Conversion & Throughput							
Conversion Time (Notes 3, 4)	1.25		2.75	1.25		2.75	us
Throughput Rate	0.5		1	0.5		1	MHz
Acquisition Time (Note 5)		400			400		ns
Power Supplies							
Power Supply Current (Note 6)							
I_{A+}		70	90		70	90	mA
I_{A-}		-70	-90		-70	-90	mA
I_{D+}		5	10		5	10	mA
I_{D-}		-5	-10		-5	-10	mA
Power Dissipation (Note 6)		750	1000		750	1000	mW
Power Supply Rejection at dc							
Positive Supplies		50			50		dB
Negative Supplies		50			50		dB

Notes:
2. Input 40 dB below full scale.
3. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{DRDY}$.
4. Applies to conversions triggered externally. In Continuous Convert mode throughput proceeds at one-eighth the master clock frequency with a fixed 10 clock cycle conversion time.
5. The internal track-and-hold returns to the track mode on the fourth master clock cycle after the start of a conversion cycle. It is guaranteed to acquire a full-scale step to 12-bit accuracy while operating at full throughput.
6. All outputs unloaded. All inputs CMOS levels.

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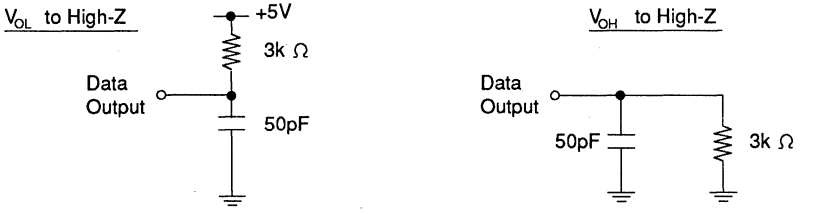
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF).

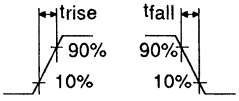
Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency:	f_{CLK}	4	-	8	MHz
Master Clock Duty Cycle	-	40	-	60	%
Rise Times: Any Digital Input (Note 7) Any Digital Output	t_{rise}	- -	- 20	1.0 -	us ns
Fall Times: Any Digital Input (Note 7) Any Digital Output	t_{fall}	- -	- 20	1.0 -	us ns
$\overline{HOLD}$/CLKIN Phase Relationship State 7 to $\overline{HOLD}$ Low $\overline{HOLD}$ Low to State 0 State 0 to $\overline{HOLD}$ High $\overline{HOLD}$ High to State 7	 t_{ha} t_{hb} t_{hc} t_{hd}	 62.5 0 75 30	 - - - -	 - - - -	 ns ns ns ns
Conversion Time (Note 8)	t_c	10	-	11	MCC*
$\overline{DRDY}$ Pulse Width	t_{dpw}	-	3	-	MCC*
Data Delay Time	t_{dd}	-	20	50	ns
Access Times: $\overline{CS}$ Low to Data Valid (Note 9) $\overline{RD}$ Low to Data Valid	t_{csa} t_{rda}	- -	55 55	110 110	ns ns
Output Float Delay: $\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	t_{fd}	-	40	110	ns
Cal Pulse Width: (Note 10) CAL high and $\overline{CS}$ Low	t_{csh}	2	-	-	MCC*
$\overline{RST}$ Pulse Width	t_{rpw}	2	-	-	MCC*

Notes:
7. $\overline{HOLD}$ and CLKIN should be driven with signals which have rise and fall times of 25 ns or faster.
8. Conversion time in the Continuous Convert mode is a fixed 10 clock cycles.
9. Data goes valid when both $\overline{CS}$ and $\overline{RD}$ are low simultaneously. Each access time assumes the other control input is already low or falls concurrently.
10. If CAL is brought low while $\overline{CS}$ is low, a calibration cycle will be initiated.

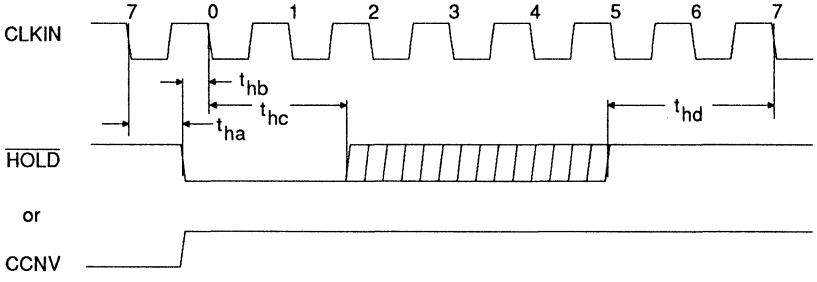
* MCC = Master Clock Cycles; 1 MCC = $1/f_{CLK}$

Float Delay Test Circuits

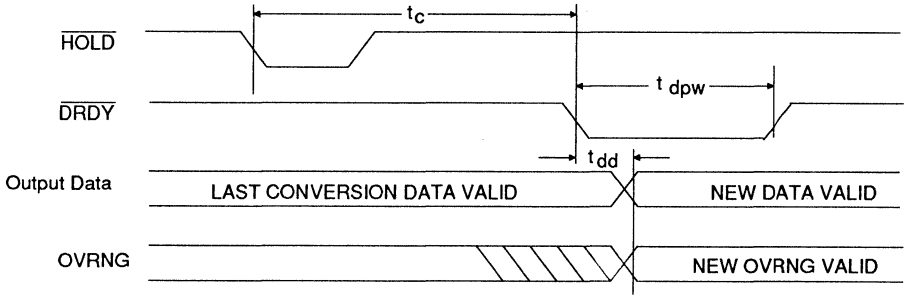




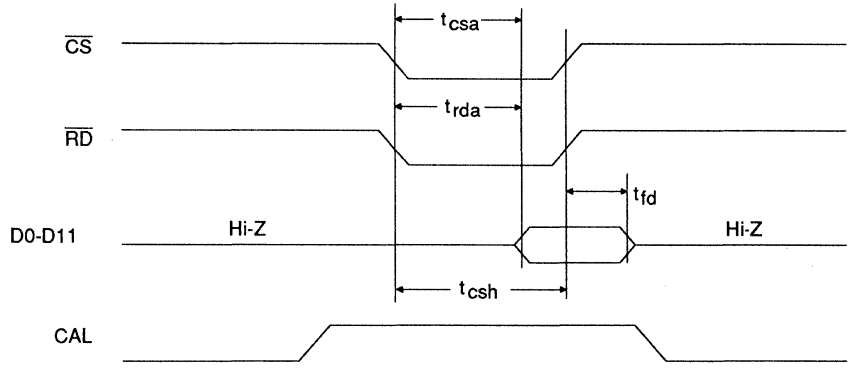
Rise and Fall Times



Hold/Master Clock Phase Relationship



Conversion Timing



Read and Calibration Control Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%) All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 11)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage (Note 11)	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 12)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-10	-	+10	uA
3-State Leakage Current	I_{OZ}	-10	-	+10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Note: 11. All pins except $\overline{HOLD}$ and CLKIN which accept only CMOS-compatible inputs (V_{IL} = 0.5V and V_{IH} = VD+ - 0.5V).
12. I_{out} = -100µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 13).

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	4.75	5.0	VA2+, VA5+	V
Negative Digital	VD-	−4.75	−5.0	−5.25	V
Positive Analog	VA1+ - VA5+	4.75	5.0	5.25	V
Negative Analog	VA1- - VA3-	−4.75	−5.0	−5.25	V
Analog Input Voltage	V_{AIN}	VREF-	-	VREF+	V
Analog Reference Voltages					
Unipolar Input Range	VREF+	2.0	-	3.0	V
	VREF-	-	AGND	-	V
Bipolar Input Range	VREF+	1.0	-	1.5	V
	VREF-	−1.0	-	−1.5	V

Notes: 13. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground).

Parameter	Symbol	Min	Max	Units
DC Power Supplies: Positive Digital	VD+	−0.3	VA2+,VA5+ + 0.3	V
Negative Digital	VD-	0.3	−6.0	V
Positive Analog (Note 14)	VA1+ - VA5+	−0.3	6.0	V
Negative Analog	VA1- - VA3-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Note 15)	I_{in}	-	+10	mA
Analog Input Voltage (AIN and VREF pins)	V_{INA}	VA1- - VA3- - 0.3	VA2+,VA5+ + 0.3	V
Digital Input Voltage	V_{IND}	−0.3	VA2+,VA5+ + 0.3	V
Ambient Operating Temperature	T_A	−55	125	°C
Storage Temperature	T_{stg}	−65	150	°C

Notes: 14. VA1+, VA3+, VA4+ must never exceed VA2+ and VA5+ by more than 0.3V.
15. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.374" by 0.348" (± 0.002").

2. The CS5412-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

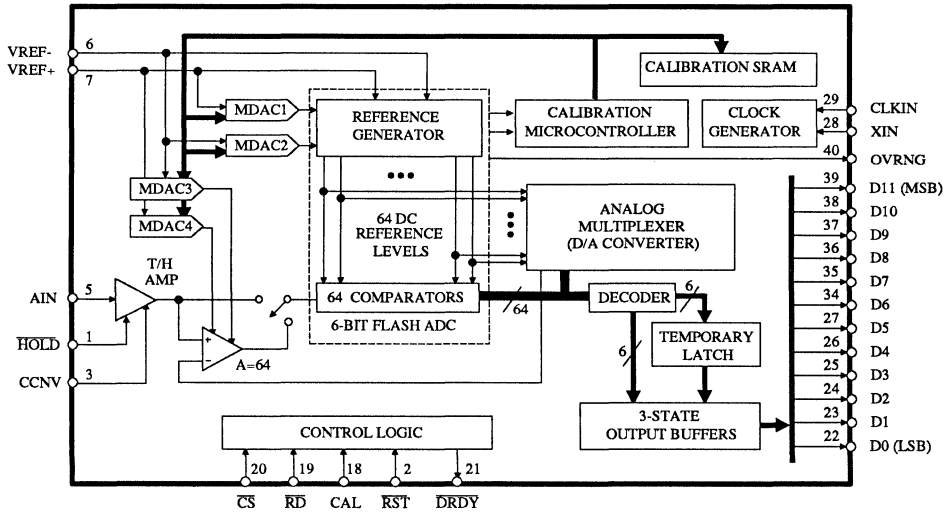
3. Die thickness shall be 0.0175" ±0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 9.

5. The cavity dimensions for each die within the waffle pack are 0.425" by 0.425". Exterior waffle pack dimensions are 2.0" by 2.0"

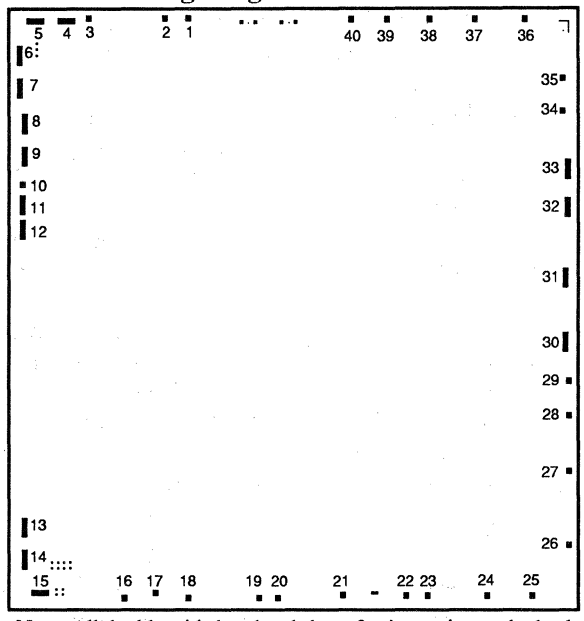
6. The CS5412-U requires no particular bonding sequence.

7. The CS5412-U product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 1000V and 200mA dc latch currents. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.



Block Diagram

Bonding Diagram for CS5412-U



Note: All double wide bond pads have 2 wires going to the lead

1	-	$\overline{\text{HOLD}}$	21	-	$\overline{\text{DRDY}}$
2	-	$\overline{\text{RST}}$	22	-	D0
3	-	CCNV	23	-	D1
4	-	AGND1	24	-	D2
5	-	AIN	25	-	D3
6	-	VREF-	26	-	D4
7	-	VREF+	27	-	D5
8	-	VAl+	28	-	XIN
9	-	VAl-	29	-	CLKIN
10	-	ANGD2	30	-	VD-
11	-	VA2+	31	-	VD+
12	-	VA3+	32	-	VA5+
13	-	VA2-	33	-	DGND
14	-	VA3-	34	-	D6
15	-	VA4+	35	-	D7
16	-	TST1	36	-	D8
17	-	TST2	37	-	D9
18	-	CAL	38	-	D10
19	-	$\overline{\text{RD}}$	39	-	D11
20	-	$\overline{\text{CS}}$	40	-	OVRNG

Semiconductor Corporation

CS5501-U

Low-Cost, 16-Bit Measurement A/D Converter Die

Features

- Monolithic CMOS ADC with Filtering
  6-Pole, Low-Pass Gaussian Filter
  Corner Frequencies from 0.1 to 10Hz
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  Linearity Error: ±0.003% FS
  Offset Error: ±1/4 LSB
  Full Scale Error: ±1/8 LSB
  16-Bit No Missing Codes (DNL ±1/8 LSB)
- System Calibration Capability
- Flexible Serial Communications Port
  UART- and µC-Compatible Formats
  3-State Data and Clock Outputs
- Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  10µW Sleep Mode for Portable Applications

General Description

The CS5501 is a low-cost CMOS A/D converter which is ideal for measuring low-frequency signals representing physical, chemical, and biological processes. The CS5501 utilizes charge-balance techniques to achieve true 16-bit accuracy with up to 4kHz word rates at very low cost.

The CS5501 continuously samples at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The filter has a low-pass, 6-pole Gaussian response with no overshoot in response to step functions. Corner frequencies can be set from 0.1Hz to 10Hz, thus rejecting 50Hz and 60Hz line frequencies and any noise at spurious frequencies.

The CS5501 includes on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/4 LSB. The device can also be applied in system calibration schemes to null offset and gain errors in the input channel.

The CS5501's serial port offers three modes of operation. In addition to a UART-compatible mode of asynchronous communication, there are two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

ORDERING INFORMATION:

Model	Temp. Range
CS5501-JU	0°C to 70°C
CS5501-SU	-55°C to +125°C

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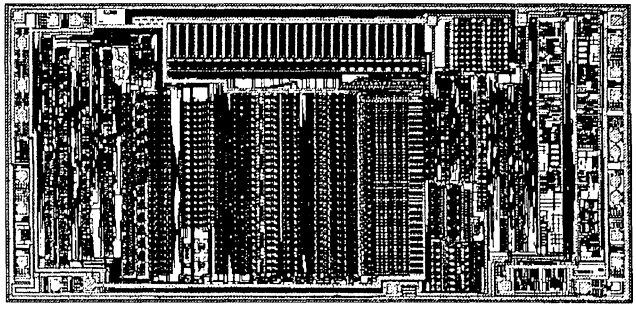

Dice Information | CS5501-U dice are functionally identical to packaged CS5501 devices. For general application information, refer to the CS5501 packaged product data sheet.

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ANALOG CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V; f_{CLK} = 4.096MHz; Bipolar Mode; MODE = VD+; R_{source} = 750Ω with a 1nF to AGND at AIN (see Note 1): unless otherwise specified.)

Parameter		CS5501-JU min	CS5501-JU typ	CS5501-JU max	CS5501-SU min	CS5501-SU typ	CS5501-SU max	Units
Specified Temperature Range			0 to +70			-55 to +125		°C
Probe Test Temperature			25			125		°C
Accuracy								
Linearity Error T_{min} to T_{max}	-J,A,S		0.003			0.003		±% FS
Differential Nonlinearity T_{min} to T_{max}			± 1/8			± 1/8		LSB
Full Scale Error	(Note 2)		± 0.13			± 0.13		LSB
Full Scale Drift	(Note 3)		± 1.2			± 2.3		LSB
Unipolar Offset	(Note 2)		± 0.25			± 0.25		LSB
Unipolar Offset Drift	(Note 3)		± 1.6			+3.0 -25.0		LSB
Bipolar Offset	(Note 2)		± 0.25			±0.25		LSB
Bipolar Offset Drift	(Note 3)		± 0.8			+1.5 -12.5		LSB
Bipolar Negative Full Scale Error	(Note 2)		± 0.5			±0.5		LSB
Bipolar Negative Full Scale Drift	(Note 3)		± 0.6			±1.2		LSB
Noise (Referred to Output)			1/10			1/10		LSB rms
Power Supplies								
DC Power Supply Currents								
I_{A+}			2	3.2		2	3.2	mA
I_{A-}			2	3.2		2	3.2	mA
I_{D+}			1	1.5		1	1.5	mA
I_{D-}	(Note 4)		0.03	0.1		0.03	0.1	mA
Power Dissipation								
$\overline{SLEEP}$ High			25	40		25	40	mW
$\overline{SLEEP}$ Low	(Note 4)		10	20		10	40	uW
Power Supply Rejection								
Positive Supplies			70			70		dB
Negative Supplies	(Note 5)		75			75		dB
Analog Input								
Analog Input Range								
Unipolar			0 to +2.5			0 to +2.5		V
Bipolar			± 2.5			± 2.5		V
Input Capacitance			20			20		pF
DC Bias Current	(Note 1)		1			1		nA

ANALOG CHARACTERISTICS (Continued)

CS5501-JU,SU								
System Calibration Specifications		Unipolar Mode min	typ	max	Bipolar Mode min	typ	max	Units
Positive Full Scale Calibration Range		-	-	VREF+0.1	-	-	VREF+0.1	V
Positive Full Scale Input Overrange		-	-	VREF+0.1	-	-	VREF+0.1	V
Negative Full Scale Input Overrange		-	-	-(VREF+0.1)	-	-	-(VREF+0.1)	V
Maximum Offset Calibration Range	(Note 6) (Note 7)	-	-	-(VREF+0.1)	-	-	-40% VREF to +40%VREF	V
Input Span	(Note 8)	80% VREF		200%VREF + 0.2	80% VREF		200%VREF + 0.2	V

Notes:
1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5501's source impedance requirements. For more information refer the text section *Analog Input Impedance Considerations*, in the CS5501 data sheet.
2. Applies after calibration at the temperature of interest.
3. Total drift over the specified temperature range since calibration at power-up at 25°C. This is guaranteed by design and /or characterization. Recalibration at any temperature will remove these errors.
4. All outputs unloaded. All inputs CMOS levels.
5. 0.1Hz to 10Hz. PSRR at 60 Hz will exceed 120 dB due to the benefit of the digital filter.
6. In unipolar mode the offset can have a negative value (-VREF) such that the unipolar mode can mimic bipolar mode operation.
7. The specifications for Input Overrange and for Input Span apply additional constraints on the offset calibration range.
8. For Unipolar mode, Input Span is the difference between full scale and zero scale. For Bipolar mode, Input Span is the difference between positive and negative full scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of ±(VREF + 0.1).

Specifications are subject to change without notice.

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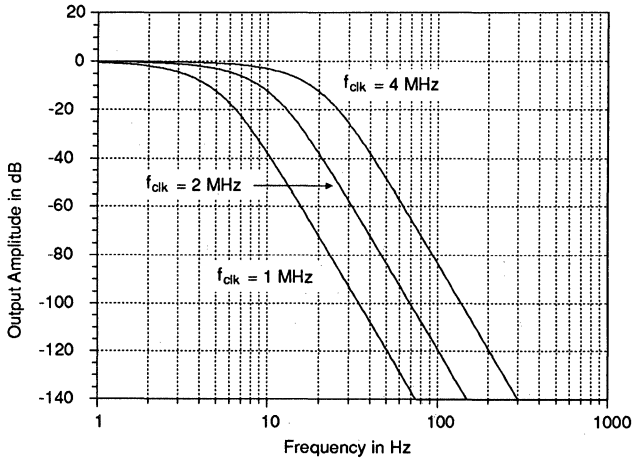
	Unipolar Mode			Bipolar Mode		
uV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

VREF=2.5V

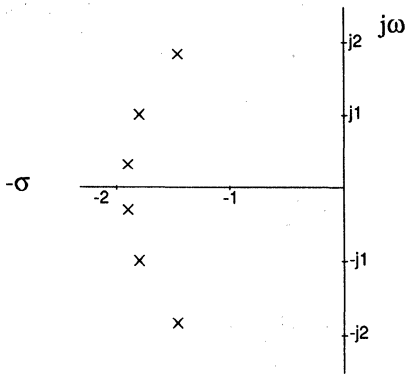
Unit Conversion Factors

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Sampling Frequency	f_s	f_{clk} / 256	Hz
Output Update Rate	f_{out}	f_{clk} /1024	Hz
Filter Corner Frequency	f_{-3dB}	f_{clk} /409,600	Hz
Settling Time to ±0.0007% FS (FS Step)	t_s	506,880/ f_{clk}	s



Frequency Response



$S_{1,2} = -1.4667 \pm j1.8199$

$S_{3,4} = -1.7559 \pm j1.0008$

$S_{5,6} = -1.8746 \pm j0.32276$

S-Domain Pole/Zero Plot (Continuous-Time Representation)

$$H(x) = [1 + 0.694x^2 + 0.241x^4 + 0.0557x^6 + 0.009664x^8 + 0.00134x^{10} + 0.000155x^{12}]^{-1/2}$$

where $x = f/f_{-3dB}$, $f_{-3dB} = f_{clk}/409{,}600$, and f is the frequency of interest.

Continuous-Time Representation of 6-Pole Gaussian Filter

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

All measurements below are performed under static conditions.

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage (VD+ and VA+)	V_{MR}	2.0	-	-	V
High-Level Input Voltage All Except CLKIN	V_{IH}	2.0	-	-	V
High-Level Input Voltage CLKIN	V_{IH}	3.5	-	-	V
Low-Level Input Voltage All Except CLKIN	V_{IL}	-	-	0.8	V
Low-Level Input Voltage CLKIN	V_{IL}	-	-	1.5	V
High-Level Output Voltage (Note 9)	V_{OH}	VD+ - 1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	uA
3-State Leakage Current	I_{OZ}	-	-	±10	uA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 10.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	−4.5	−5.0	−5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	−4.5	−5.0	−5.5	V
Analog Reference Voltage		VREF	1.0	2.5	3.0	V
Analog Input Voltage: (Note 11)	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 10. All voltages with respect to ground.

11. The CS5501 can accept input voltages up to the analog supplies (VA+ and VA-). It will accurately convert and filter signals with noise excursions up to 100mV beyond |VREF|. After filtering, the CS5501 will output all 1's for any input above VREF and all 0's for any input below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	−0.3	VA+ + 0.3	V
	Negative Digital	VD-	0.3	−6.0	V
	Positive Analog	VA+	−0.3	6.0	V
	Negative Analog	VA-	0.3	−6.0	V
Input Current, Any Pin Except Supplies (Notes 12,13)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	VA- - 0.3	VA+ + 0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA+ + 0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 12. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.

13. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

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SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency: (Note 14)	Internal gate oscillator (See Table 1)	f_{clk}	200	4096	4200	kHz
	Externally Supplied: Maximum		-	-	4200	kHz
	Minimum (Note 15)		200	40	-	kHz
Master Clock Duty Cycle		-	20	-	80	%
Rise Times:	Any Digital Input	t_{rise}	-	-	1.0	us
	Any Digital Output (Note 16)		-	20	-	ns
Fall Times:	Any Digital Input	t_{fall}	-	-	1.0	us
	Any Digital Output (Note 16)		-	20	-	ns
Set Up Times:	SC1, SC2 to CAL High	t_{scs}	0	-	-	ns
	$\overline{SLEEP}$ High to CLKIN High (Note 17)	t_{sls}	1	-	-	us
SSC Mode (Mode = VD+)						
Access Time:	$\overline{CS}$ Low to SDATA Out	t_{csd1}	$3/f_{clk}$	-	-	ns
SDATA Delay Time	SCLK Falling to New SDATA bit	t_{dd1}	-	25	100	ns
SCLK Delay Time (at 4.096 MHz)	SDATA MSB bit to SCLK Rising	t_{cd1}	250	380	-	ns
Serial Clock (Out)	Pulse Width High (at 4.096 MHz)	t_{ph1}	-	240	300	ns
	Pulse Width Low	t_{pl1}	-	730	790	ns
Output Float Delay:	SCLK Rising to Hi-Z	t_{fd2}	-	$1/f_{clk}$ +100	$1/f_{clk}$ + 200	ns
Output Float Delay: (Note 18)	$\overline{CS}$ High to Output Hi-Z	t_{fd1}	-	-	$4/f_{clk}$ + 200	ns

Notes: 14. A master clock must be supplied whenever the CS5501 is not in $\overline{SLEEP}$ mode. If no clock is present when not in $\overline{SLEEP}$ mode, the CS5501 can draw higher current than specified and possibly become uncalibrated.

15. The CS5501 is designed to operate at 40kHz, but is not production tested at this frequency. Instead, the part is tested at 200kHz to reduce production test time.

16. Specified using 10% and 90% points on waveform of interest.

17. In order to synchronize several CS5501's together using the $\overline{SLEEP}$ pad, this specification must be met.

18. If $\overline{CS}$ is returned high before all 16 data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

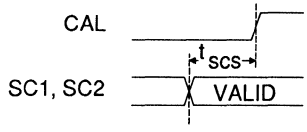
SWITCHING CHARACTERISTICS (continued) ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter	Symbol	Min	Typ	Max	Units
SEC Mode (Mode = DGND)					
Serial Clock (In)	f_{sclk}	0		4.2	MHz
Serial Clock (In) Pulse Width High	t_{ph2}	50	-	-	ns
Pulse Width Low	t_{pl2}	180	-	-	ns
Access Time: $\overline{CS}$ Low to Data Valid (Note 19)	t_{csd2}	-	80	160	ns
Maximum Data Delay Time (Note 20) SCLK Falling to New SDATA bit	tdd2	-	75	150	ns
Output Float Delay $\overline{CS}$ High to Output Hi-Z	t_{fd3}	-	-	250	ns
Output Float Delay SCLK Falling to Output Hi-Z	t_{fd4}	-	100	200	ns
AC Mode (Mode = VD-)					
Serial Clock (In)	f_{sclk}	0	-	4.2	MHz
Serial Clock (In) Pulse Width High	t_{ph3}	50	-	-	ns
Pulse Width Low	t_{pl3}	180	-	-	ns
Set-up Time $\overline{CS}$ Low to SCLK Falling	t_{css}	-	20	40	ns
Maximum Data Delay Time SCLK Falling to New Output Bit	t_{dd3}	-	90	180	ns
Output Float Delay (Note 21) SCLK Falling to Output Hi-Z	t_{fd5}	-	100	200	ns

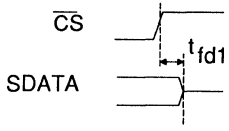
Notes: 19. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 4 clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asychronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 4 CLKIN cycles plus 160ns after $\overline{CS}$ goes low.

20. SDATA transitions on the falling edge of SCLK(i).

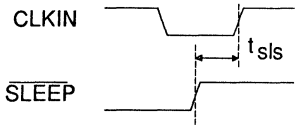
21. If $\overline{CS}$ is returned high after an 11-bit data packet is started, the SDATA output will continue to output data until the end of the second stop bit. At that time the SDATA output will go to high impedance.



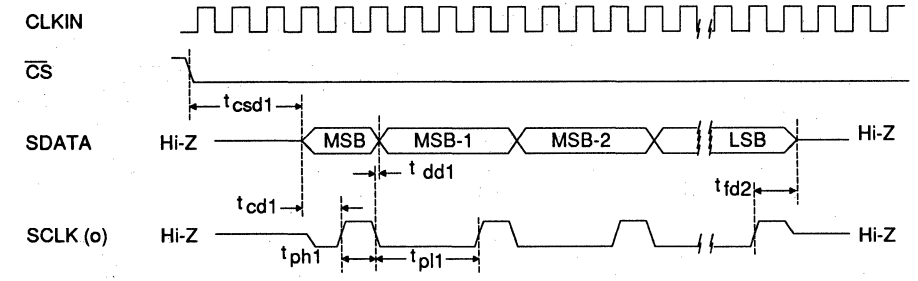
Calibration Control Timing



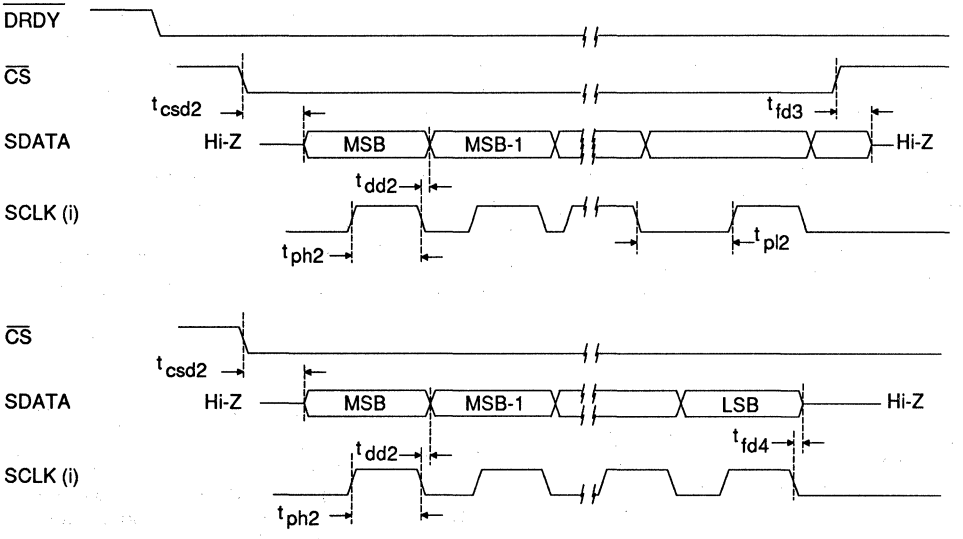
Output Data Access Timing SSC Mode (Note 18)



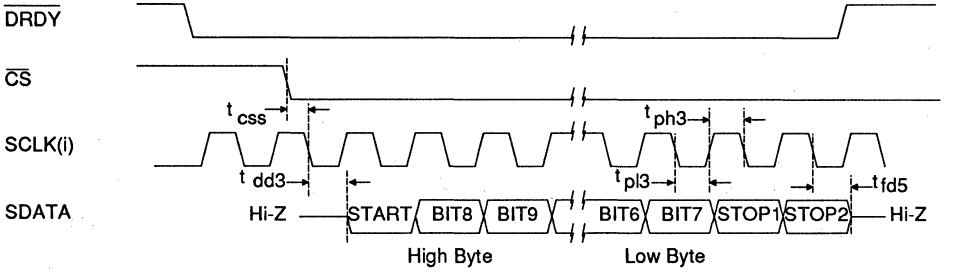
Sleep Mode Timing for Synchronization



SSC MODE Timing Relationships



SEC MODE Timing Relationships



AC MODE Timing Relationships

GENERAL INFORMATION

Crystal Semiconductor Procedure 42AA00007 outlines the General Requirements for Die Sales. The document includes information on wafer fabrication, manufacturing flow, screening/inspection procedures, packing, shipping, and change notification.

Assembly Information

1. Die size shall be 0.149" by 0.303" (± 0.002")

2. The CS5501-U is suited for die attach through either eutectic or adhesive means. When eutectic die attach is used, Crystal Semiconductor recommends either a 99.9% Au or 98% Au/2% Si preform of the appropriate size. The backside of the die should be electrically connected to VA+.

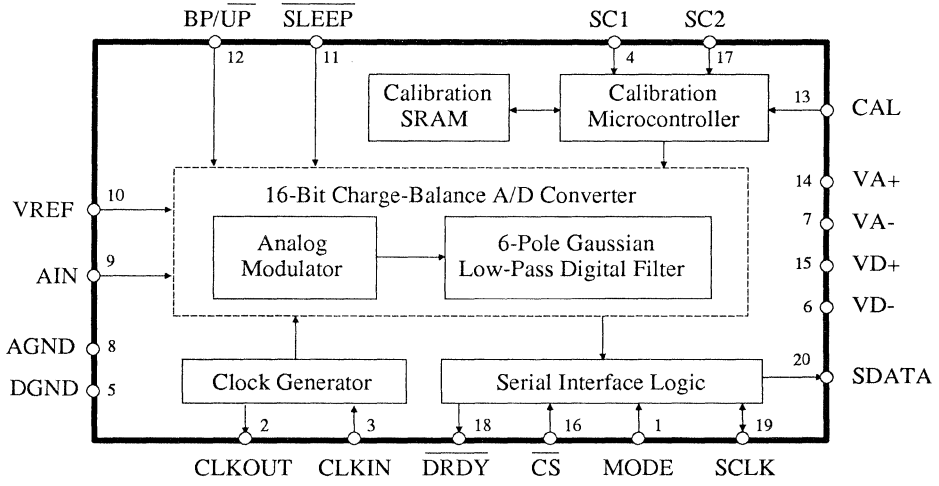
3. Die thickness shall be 0.0175" ±0.0035". If tighter tolerances are required, contact the factory.

4. The maximum number of die per waffle pack carrier is 28.

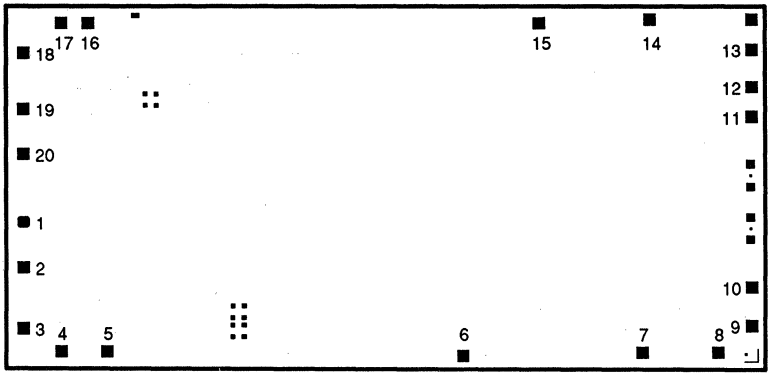
5. The cavity dimensions for each die within the waffle pack are .180" by .330" (Waffle Pack Type H20-179329).

6. The CS5501-U requires no particular bonding sequence.

7. The CS5501-U product qualification determined that each pin on the device can typically withstand electrostatic discharges up to 3000V and 300mA dc latch currents. This meets Crystal's minimum criteria of 2500V and 100mA respectively. Still, Crystal Semiconductor strongly recommends proper handling procedures and in-circuit application.



Bond Pad Locations for CS5501-U



1	- MODE	11	- $\overline{\text{SLEEP}}$
2	- CLKOUT	12	- BP/$\overline{\text{UP}}$
3	- CLKIN	13	- CAL
4	- SC1	14	- VA+
5	- DGND	15	- VD+
6	- VD-	16	- $\overline{\text{CS}}$
7	- VA-	17	- SC2
8	- AGND	18	- $\overline{\text{DRDY}}$
9	- AIN	19	- SCLK
10	- VREF	20	- SDATA

INTRODUCTION

Crystal Semiconductor is committed to supplying product to the military marketplace as a major long-term focus of our business.

All devices are designed to meet the extended temperature ranges required for military applications. The wafer fabrication and device assembly facilities used for Crystal standard production were selected for their proven capability to provide product processed to military requirements.

Wafer fab, packaging, and test facilities have all passed Crystal military audit. Our CAGE FSCM/MILSCAP number is 0A384.

USER'S GUIDE

Device: SMD#	CS5012 5962-89679	CS5014 5962-89674	CS5016 5962-89676	CS5412 TBA
Resolution (bits)	12	14	16	12
Conversion Time	12 µs	14 µs	16 µs	1.2 µs
Throughput	63kHz	56kHz	50kHz	1MHz
No Missing Codes	12	14	16	12
Signal-to-Noise plus Distortion	72dB	80dB	84dB	70dB

CONTENTS

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

This copy of the CS5012 SMD is for information only. Always obtain the current SMD directly from DESC. In addition, check with Crystal Semiconductor for any upcoming SMD upgrades and additions.

REV																												
PAGE																												
REV STATUS	REV																											
OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15												

Defense Electronics Supply Center Dayton, Ohio	PREPARED BY	MILITARY DRAWING This drawing available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY	
Original Date of drawing:	APPROVED BY	TITLE: Microcircuits, Linear, Micro-Processor Compatible, 12-bit Analog-to-Digital Converter, CMOS, Monolithic Silicon
	SIZE: CODE IDENT. NO. 67268	DWG NO. 5962-89679
AMSC N/A	REV	PAGE 1 OF 13

DISTRIBUTION STATEMENT A. Approved for public release; distribution unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89679	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit Function
01	CS5012	12-bit CMOS A/D converter, 12.25 µs

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .622" x .622" x .120"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Positive digital supply ($+V_D$) voltage range ..... -0.3 V dc to +6.0 V dc 2/
Negative digital supply ($-V_D$) voltage range ..... +0.3 V dc to -6.0 V dc
Positive analog supply ($+V_A$) voltage range ..... -0.3 V dc to +6.0 V dc
Negative analog supply ($-V_A$) voltage range ..... +0.3 V dc to -6.0 V dc
Analog ground (AGND) to digital ground (DGND) ..... ±0.5 dc
Input current, any pin except supplies ..... ±10 mA 3/
Analog input voltage (AIN and V_{REF} pins) ..... $-V_A$ 0.3 V dc to $+V_A$ + 0.3 V dc
Digital input voltage ..... -0.3 V dc to $+V_D$ + 0.3 V dc

1/ All voltages referenced to AGND and DGND tied together.

2/ In addition, $+V_D$ must not be greater than $+V_A$ + 0.3 V dc.

3/ Transient currents of up to 100 mA will not cause latch-up.

Storage temperature range	-65 °C to +150 °C
Lead temperature (soldering, 10 seconds)	260 °C
Junction temperature (T_J)	195 °C
Power dissipation, (P_D):	
Case Q	1500 mW
Case X	1100 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case Q	45 °C/W
Case X	60 °C/W

1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T_A)	-55 °C to +125 °C
Positive digital supply voltage ($+V_D$)	+4.5 V dc to $+V_A$ V dc 2/
Negative digital supply voltage ($-V_D$)	-4.5 V dc to -5.5 V dc
Positive analog supply voltage ($+V_A$)	+4.5 V dc to +5.5 V dc
Negative analog supply voltage ($-V_A$)	-4.5 V dc to -5.5 V dc
Digital ground (DGND)	0 V dc
Analog ground (AGND)	0 V dc
Digital input low voltage (V_{IL})	-0.3 V dc to +0.8 V dc
Digital input high voltage (V_{IH})	+2.0 V dc to $+V_D$
Analog reference input voltage (V_{REF}) range	+2.5 V dc to +4.5 V dc
Analog input voltage range:	
Unipolar mode	AGND to $+V_{REF}$
Bipolar mode	$-V_{REF}$ to $+V_{REF}$

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Resolution for which no missing codes is guaranteed	RES	1/	1, 2, 3	12		Bits
Integral linearity error	INL	1/ 2/	1, 2, 3		±0.5	LSB
Differential linearity error	DNL	1/ 2/	1, 2, 3		±0.5	LSB
Full-scale error	FSE	1/ 2/	1, 2, 3		±0.5	LSB
Full-scale error drift	$dFSE/d_t$	1/ 2/ 3/ 4/	2, 3,		±0.25	LSB
Unipolar offset error	VOFF	1/ 2/	1, 2, 3		±0.5	LSB
Unipolar offset error drift	$dVOFF/d_t$	1/ 2/ 3/ 4/	2, 3		±0.25	LSB
Bipolar offset error	BOFF	1/ 2/	1, 2, 3		±0.5	LSB
Bipolar offset error drift	$dBOFF/d_t$	1/ 2/ 3/ 4/	2, 3		±0.25	LSB
Bipolar negative full-scale error	BNFSE	1/ 2/	1, 2, 3		±0.5	LSB
Bipolar negative full-scale error drift	$dBNFSE/d_t$	1/ 2/ 3/ 4/	2, 3		±0.25	LSB
Peak harmonic or spurious noise	S/PN	1 kHz input, full scale amplitude, bipolar mode 1/ 2/	4, 5, 6	84		dB
		12 kHz input, full scale amplitude, bipolar mode 1/ 2/		80		
Signal to noise ratio	S/(N+D)	1kHz input, full scale amplitude, bipolar mode 1/ 2/	4, 5, 6	72		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroup	Limits Min	Limits Max	Unit
Analog input capacitance in fine charge mode	C_{IN}	Unipolar mode, $T_A = +25^{o}C$ 1/ 3/	4		375	pF
		Bipolar mode, $T_A = +25^{o}C$ 1/ 3/			220	
Digital input voltage (HOLD, CLKIN, CAL, INTRLV, BW, RST, BP/UP, A0, RD, CS)	V_{IH}	5/ 6/	1, 2, 3	2.0		V
	V_{IL}				0.8	
Digital input current	I_{IN}	5/ 6/	1, 2, 3		±10	µA
Digital output voltage (D0-D15, SDATA, SCLK, EDC, EOT)	V_{OL}	Logic "0", $I_{SINK} = -1.6mA$ 5/ 6/	1, 2, 3		0.4	V
	V_{OH}	Logic "1", $I_{SOURCE}=100\mu A$ 5/ 6/		$+V_D$ -1.0		
High impedance state output current	I_{OZ}	Pins D_0 to D_{15} only 5/ 6/	1, 2, 3		±10	µA
Conversion time	t_C	1/ 6/ 7/	9, 10, 11		12.25	µs
Acquisition time	t_{ACQ}	1/ 2/ 3/ 8/ $T_A = +25^{o}C$	9		3.75	µs
Throughput	t_{PUT}	1/ 2/ 6/	9, 10, 11	62.5		kHz
Positive analog supply current	I_{A+}	6/ 9/ $+V_A, +V_D = 5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		19.0	mA
Negative analog supply current	I_{A-}	6/ 9/ $+V_A, +V_D = 5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		19.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Positive digital supply current	I_D+	6/ 9/ $+V_A, +V_D = +5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		6.0	mA
Negative digital supply current	I_D-	6/ 9/ $+V_A, +V_D = +5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		6.0	mA
Master clock frequency 10/	f_{CLK}	$T_A = -55^{o}C$ Internally generated CLKIN = 0V dc $+V_D, +V_A = +4.5V$ $-V_D, -V_A = -4.5V$	11	1.75		MHz
HOLD pulse width	t_{HPW}	5/ 6/ 11/ (see figure 4)	9, 10,11	$1/f_{CLK}$ +50	t_C	ns
Data delay time	t_{DD}	5/ 6/ 11/ (see figure 4)	9, 10,11		100	ns
EOC pulse width	t_{EPW}	5/ 6/ 11/ (see figure 4)	9, 10,11	$4/f_{CLK}$ -20		ns
CAL, $\overline{INTRLV}$ to $\overline{CS}$ low setup time	t_{CS}	5/ 6/ 11/ (see figure 5)	9, 10,11	20		ns
A0 to $\overline{CS}$ and $\overline{RD}$ low setup time	t_{AS}	5/ 6/ 11/ (see figure 5)	9, 10,11	20		ns
CS or $\overline{RD}$ High to A0 invalid hold time	t_{AH}	5/ 6/ 11/ (see figure 5)	9, 10,11	50		ns
CS High to CAL, $\overline{INTRLV}$ invalid hold time	t_{CH}	5/ 6/ 11/ (see figure 5)	9, 10,11	50		ns
CS low to data valid access time	t_{CA}	$\overline{RD}$ = logic "0", 5/ 6/ 11/ (see figure 5)	9, 10,11		250 *	ns

See footnotes at end of table.

* This specification is currently being reduced to 150 ns. Please contact Crystal for the latest information.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
RD low to data valid access time	t_{RA}	$\overline{CS}$ = logic "0", 5/ 6/ 11/ (see figure 5)	9, 10, 11		250 *	ns
Output float delay	t_{FD}	5/ 6/ 11/ (see figure 5)	9, 10, 11		250 **	ns
SDATA to SCLK rising setup time	t_{SS}	5/ 6/ 11/ (see figure 6)	9, 10, 11	$2/f_{CLK}$ -50		ns
SCLK rising to SDATA hold time	t_{SH}	5/ 6/ 11/ (see figure 6)	9, 10, 11	$2/f_{CLK}$ -100		ns

1/ $+V_A$, $+V_D$ = +5.0 V; $-V_A$, $-V_D$ = -5.0 V; V_{REF} = +2.5 V dc or +4.5 V dc; f_{CLK} = 4 MHz; Analog source impedance = 200 ohms; Error tests are done after calibration at the temperature of interest.

2/ Synchronous sampling mode ($\overline{EOT}$ connected to $\overline{HOLD}$), interleave disabled.

3/ This parameter shall be measured only for initial characterization and after process or design changes which may affect this parameter.

4/ Total drift over $-55^{o}C$ to $+125^{o}C$ since calibration at power-up at $+25^{o}C$.

5/ $+V_A$, $+V_D$ = +5.0 V dc ± 10%; $-V_A$, $-V_D$ = -5.0 V dc ± 10%

6/ This parameter is guaranteed, if not tested, at $T_A = +25^{o}C$. This parameter is tested at $T_A = -55^{o}C$ and $+125^{o}C$.

7/ Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.

8/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.

9/ All outputs unloaded; All inputs swinging between $+V_D$ and 0 V dc.

10/ Externally supplied maximum clock frequency is 4 MHz. Analog parametric measurements are done with the maximum external clock (see footnote 1/).

11/ Inputs: logic "0" = 0 V, logic "1" = $+V_D$: C_L = 50 pF.

* This specification is currently being reduced to 150 ns. Please contact Crystal for the latest information

** This specification is currently being reduced to 140 ns. Please contact Crystal for the latest information.

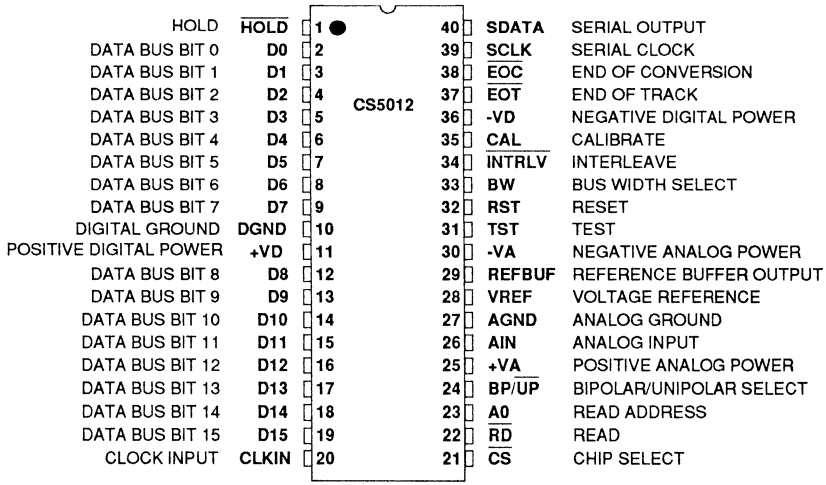

FIGURE 1. Terminal connections

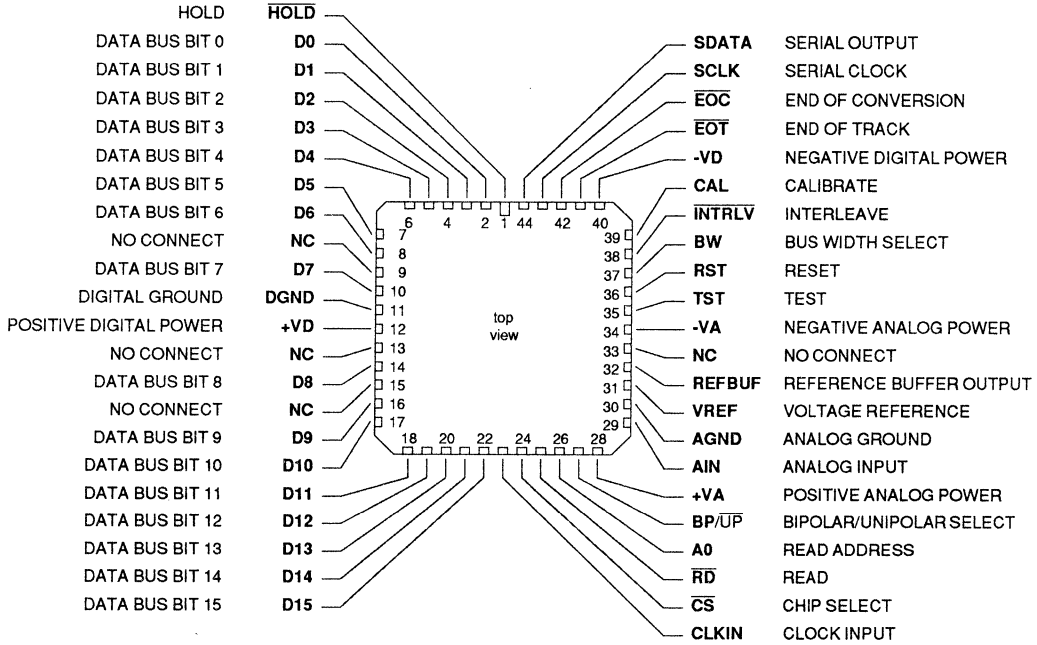

FIGURE 1. Terminal connections (continued)

HOLD	CS	CAL	INTRLV	RD	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with CS and HOLD low, or a software reset will result.

FIGURE 2. Truth table

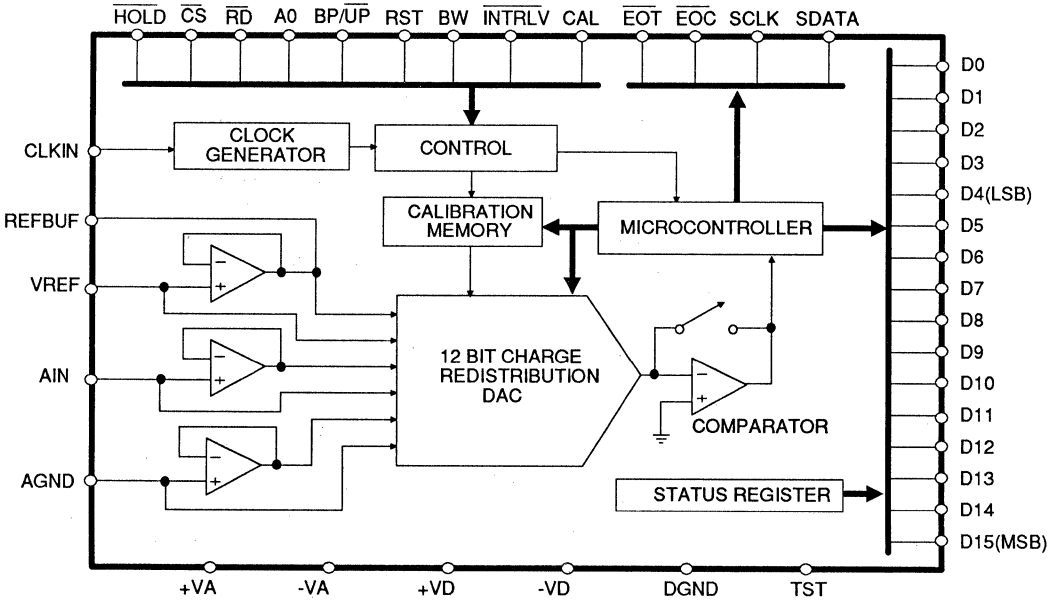

FIGURE 3. Block diagram

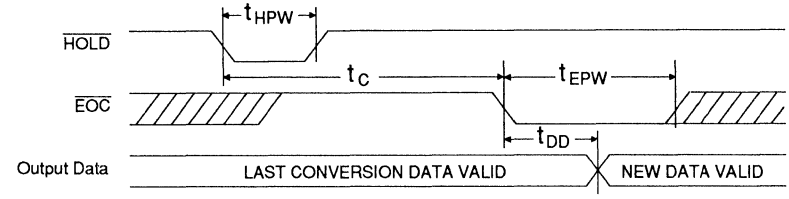

FIGURE 4. Conversion timing

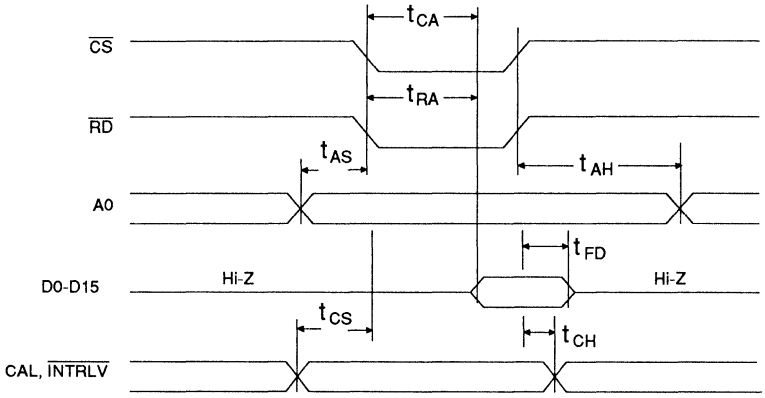

FIGURE 5. Read and calibration control timing

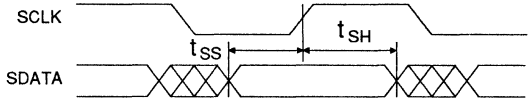

FIGURE 6. Serial output timing

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 4
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 9**, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3

* PDA applies to subgroup 1.
** Subgroup 9 guaranteed if not tested.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8967901QX	0A384	CS5012-TD12B	
5962-8967901XX	0A384	CS5012-TE12B	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0A384	Crystal Semiconductor P.O. Box 17847 4210 South Industrial Drive Austin TEXAS 78760

•Notes•

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

This copy of the CS5014 SMD is for information only. Always obtain the current SMD directly from DESC. In addition, check with Crystal Semiconductor for any upcoming SMD upgrades and additions.

REV																											
PAGE																											
REV STATUS	REV																										
OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15											

Defense Electronics Supply Center Dayton, Ohio	PREPARED BY	MILITARY DRAWING This drawing available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY	
Original Date of drawing:	APPROVED BY	TITLE: Microcircuits, Linear, Micro-Processor Compatible, 14-bit Analog-to-Digital Converter, CMOS, Monolithic Silicon
	SIZE: CODE IDENT. NO. 67268	DWG NO. 5962-89674
AMSC N/A	REV	PAGE 1 OF 13

DISTRIBUTION STATEMENT A. Approved for public release; distribution unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89674	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit Function
01	CS5014	14-bit CMOS A/D converter, 14.25 us

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, 0.662" x 0.662" x 0.120"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Positive digital supply ($+V_D$) voltage range ..... -0.3 V dc to +6.0 V dc 2/
Negative digital supply ($-V_D$) voltage range ..... +0.3 V dc to -6.0 V dc
Positive analog supply ($+V_A$) voltage range ..... -0.3 V dc to +6.0 V dc
Negative analog supply ($-V_A$) voltage range ..... +0.3 V dc to -6.0 V dc
Analog ground (AGND) to digital ground (DGND) ..... ±0.5 V dc
Input current, any pin except supplies ..... ±10 mA 3/
Analog input voltage (A_{IN} and V_{REF} pins) ..... $-V_A - 0.3$ V dc to $+V_A + 0.3$ V dc
Digital input voltage ..... -0.3 V dc to $+V_D + 0.3$ V dc
Storage temperature range ..... -65 °C to +150 °C
Lead temperature (soldering 10 seconds) ..... +260 °C
Junction temperature (T_J) ..... +195 °C
Power dissipation, (P_D)
  Case Q ..... 1500 mW
  Case X ..... 1100 mW
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA}):
  Case Q ..... +45°C/W
  Case X ..... +60°C/W

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition, $+V_D$ must not be greater than $+V_A + 0.3$ V dc.
3/ Transient currents of up to 100 mA will not cause latch-up.

1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T_A)	-55 °C to +125 °C
Positive digital supply voltage ($+V_D$)	+4.5 V dc to $+V_A$ V dc 2/
Negative digital supply voltage ($-V_D$)	-4.5 V dc to -5.5 V dc
Positive analog supply voltage ($+V_A$)	+4.5 V dc to +5.5 V dc
Negative analog supply voltage ($-V_A$)	-4.5 V dc to -5.5 V dc
Digital ground (DGND)	0 V dc
Analog ground (AGND)	0 V dc
Digital input low voltage (V_{IL})	-0.3 V dc to +0.8 V dc
Digital input high voltage (V_{IH})	+2.0 V dc to $+V_D$
Analog reference input voltage (V_{REF})	+4.5 V dc
Analog input voltage range: Unipolar mode	AGND to $+V_{REF}$
Bipolar mode	$-V_{REF}$ to $+V_{REF}$

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition, $+V_D$ must not be greater than $+V_A$ + 0.3 V dc.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}C \le T_A \le +125^{\circ}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Resolution for which no missing codes is guaranteed	RES	1/	1, 2, 3	14		Bits
Integral linearity error	INL	1/, 2/	1, 2, 3		±1.5 *	LSB
Differential linearity error	DNL	1/, 2/	1, 2, 3		±0.5	LSB
Full-scale error	FSE	1/, 2/	1, 2, 3		±1.0	LSB
Full-scale error drift	$dFSE/d_t$	1/, 2/, 3/, 4/	2, 3		±1.0	LSB
Unipolar offset error	VOFF	1/, 2/	1, 2, 3		±1.0 **	LSB
Unipolar offset error drift	$dVOFF/d_t$	1/, 2/, 3/, 4/	2, 3		±0.5	LSB
Bipolar offset error	BOFF	1/, 2/	1, 2, 3		±1.0 **	LSB
Bipolar offset error drift	$dBOFF/d_t$	1/, 2/, 3/, 4/	2, 3		±1.0	LSB
Bipolar negative full-scale error	BNFSE	1/, 2/	1, 2, 3		±1.5 ***	LSB
Bipolar negative full-scale error drift	$dBNFSE/d_t$	1/, 2/, 3/, 4/	2, 3		±1.0	LSB
Analog input capacitance in fine charge mode	C_{IN}	Unipolar mode $T_A = +25^{\circ}C$ 1/, 3/	4		375	pF
		Bipolar mode $T_A = +25^{\circ}C$ 1/, 3/			220	

See footnotes at end of table.

* An improved version is available with a specification of ±0.5 LSB. An SMD revision is under way.

** An improved version is available with a specification of ±0.75 LSB. An SMD revision is under way.

*** An improved version is available with a specification of ±1 LSB. An SMD revision is under way.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Peak harmonic or spurious noise	S/PN	1/, 2/ 1 kHz input, full scale amplitude, bipolar mode	4, 5, 6	85 *		dB
		1/, 2/ 12 kHz input, full scale amplitude, bipolar mode		80 **		
Signal to noise ratio	S/(N+D)		4, 5, 6	80 ***		dB
Digital input voltage (HOLD, CLKIN, CAL, INTRLV, BW, RST, BP/UP, A0, RD, CS)	V_{IH}	5/, 6/	1, 2, 3	2.0		V
	V_{IL}				0.8	
Digital input current	I_{IN}	5/, 6/	1, 2, 3		±10	µA
Digital output voltage (D0-D15, SDATA, SCLK, EOC, EOT)	V_{OL}	Logic "0", I_{SINK}=-1.6mA, 5/, 6/	1, 2, 3		0.4	V
	V_{OH}	Logic "1", I_{SOURCE}=100uA, 5/, 6/		(V_D) - 1.0		
High impedance state output current	I_Z	Pins D_0 to D_{15} only, 5/, 6/	1, 2, 3		±10	µA
Conversion time	t_C	1/, 6/, 7/	9, 10, 11		14.25	µs
Acquisition time	t_{ACQ}	T_A = +25°C 1/, 2/, 3/, 8/	9		3.75	µs
Throughput	t_{PUT}	1/, 2/, 6/	9, 10, 11	55.6		kHz
Positive analog supply current	$+I_A$	6/, 9/ $+V_A$,$+V_D$ = 5.5V $-V_A$,$-V_D$ = -5.5V	1, 2, 3		19.0	mA
Negative analog supply current	$-I_A$	6/, 9/ $+V_A$,$+V_D$ = 5.5V $-V_A$,$-V_D$ = -5.5V	1, 2, 3		19.0	mA

See footnotes at end of table

* An improved version is available with a specification of 94dB. An SMD revision is under way.

** An improved version is available with a specification of 84dB. An SMD revision is under way.

*** An improved version is available with a specification of 82dB. An SMD revision is under way.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \le T_A \le +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Positive digital supply current	$+I_D$	6/, 9/ $+V_A,+V_D = +5.5V$ $-V_A,-V_D = -5.5V$	1, 2, 3		6.0	mA
Negative digital supply current	$-I_D$	6/, 9/ $+V_A,+V_D = +5.5V$ $-V_A,-V_D = -5.5V$	1, 2, 3		6.0	mA
Master clock frequency 9/	f_{CLK}	$T_A = -55^{o}C$ Internally generated CLKIN = 0V dc $+V_D,+V_A = +4.5V$, $-V_D,-V_A = -4.5V$	11	1.75		MHz
$\overline{HOLD}$ pulse width	t_{HPW}	5/, 6/, 11/ (see figure 4)	9, 10, 11	$\frac{1}{f_{CLK}} + 50$	t_C	ns
Data delay time	t_{DD}	5/, 6/, 11/ (see figure 4)	9, 10, 11		100	ns
$\overline{EOC}$ pulse width	t_{EPW}	5/, 6/, 11/ (see figure 4)	9, 10, 11	$\frac{4}{f_{CLK}} - 20$		ns
CAL, $\overline{INTRLV}$ to $\overline{CS}$ low setup time	t_{CS}	5/, 6/, 11/ (see figure 5)	9, 10, 11	20		ns
A0 to $\overline{CS}$ and $\overline{RD}$ low setup time	t_{AS}	5/, 6/, 11/ (see figure 5)	9, 10, 11	20		ns
$\overline{CS}$ or $\overline{RD}$ High to A0 invalid hold time	t_{AH}	5/, 6/, 11/ (see figure 5)	9, 10, 11	50		ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ invalid hold time	t_{CH}	5/, 6/, 11/ (see figure 5)	9, 10, 11	50		ns
$\overline{CS}$ low to data valid access time	t_{CA}	$\overline{RD}$ = logic "0", 5/, 6/, 11/ (see figure 5)	9, 10, 11		250 *	ns

See footnotes at end of table.

* This specification is currently being reduced to 150 ns. Contact Crystal for the latest information.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{RD}$ low to data valid access time	t_{RA}	$\overline{CS}$ = logic "0", 5/, 6/, 11/ (see figure 5)	9, 10, 11		250 *	ns
Output float delay	t_{FD}	5/, 6/, 11/ (see figure 5)	9, 10, 11		250 **	ns
SDATA to SCLK rising setup time	t_{SS}	5/, 6/, 11/ (see figure 6)	9, 10, 11	$\frac{2}{f_{CLK}} - 50$		ns
SCLK rising to SDATA hold time	t_{SH}	5/, 6/, 11/ (see figure 6)	9, 10, 11	$\frac{2}{f_{CLK}} - 100$		ns

1/ $+V_A$, $+V_D$ = +5.0 V; $-V_A$, $-V_D$ = -5.0 V; V_{REF} = +4.5 V dc; f_{CLK} = 4 MHz; Analog source impedance = 200 ohms; Error tests are done after calibration at the temperature of interest.

2/ Synchronous sampling mode ($\overline{EOT}$ connected to $\overline{HOLD}$), Interleave disabled.

3/ This parameter shall be measured only for initial characterization, and after process or design changes which may affect this parameter.

4/ Total drift over $-55^{o}C$ to $+125^{o}C$ range since calibration at power-up at $+25^{o}C$.

5/ $+V_A$, $+V_D$ = +5.0 V dc $\pm$ 10%; $-V_A$, $-V_D$ = -5.0 V dc $\pm$ 10%

6/ This parameter is guaranteed, if not tested, at $T_A = +25^{o}C$.
This parameter is tested at $T_A = -55^{o}C$ and $+125^{o}C$.

7/ Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.

8/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.

9/ All outputs unloaded; All inputs swinging between $+V_D$ and 0 V dc.

10/ Externally supplied maximum clock frequency is 4MHz. Analog parametric measurements are done with the maximum frequency external clock (see footnote 1/).

11/ Inputs: logic "0" = 0 V, logic "1" = $+V_D$; C_L = 50 pF.

* This specificaiton is currently being reduced to 150 ns. Contact Crystal for the latest information.

** This specification is currently being reduced to 140 ns. Contact Crystal for the latest information.

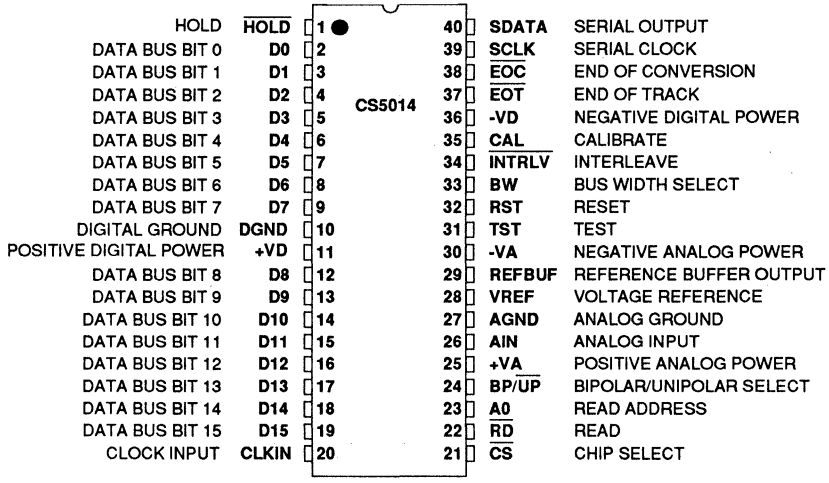

FIGURE 1. Terminal connections for Q Case outline.

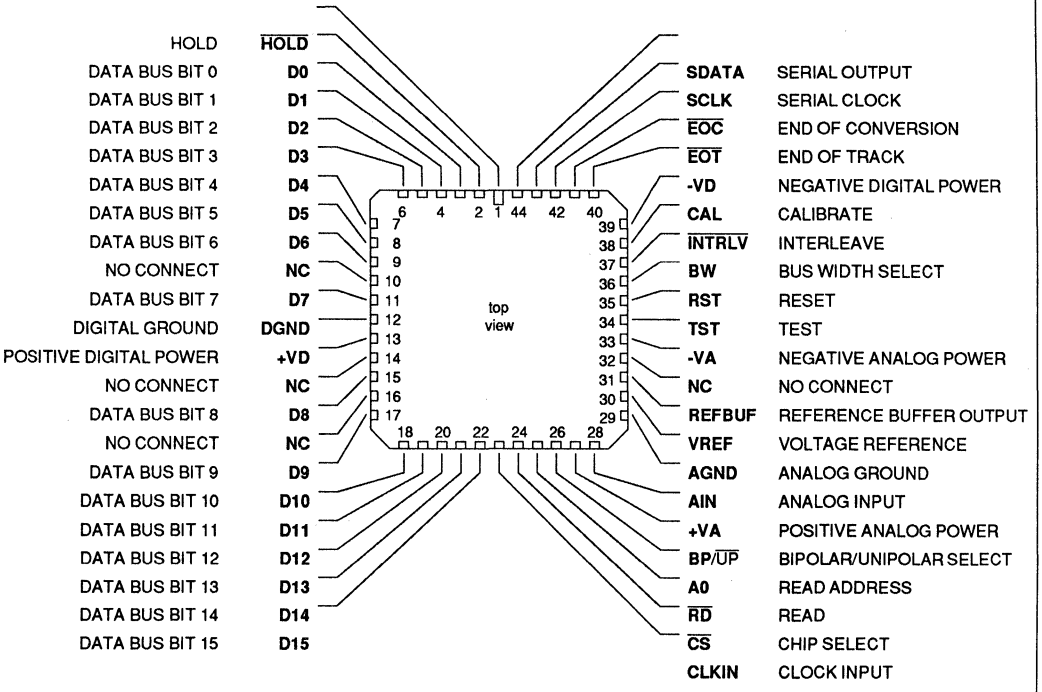

FIGURE 1. Terminal connections for X Case Outline.

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

FIGURE 2. Truth table

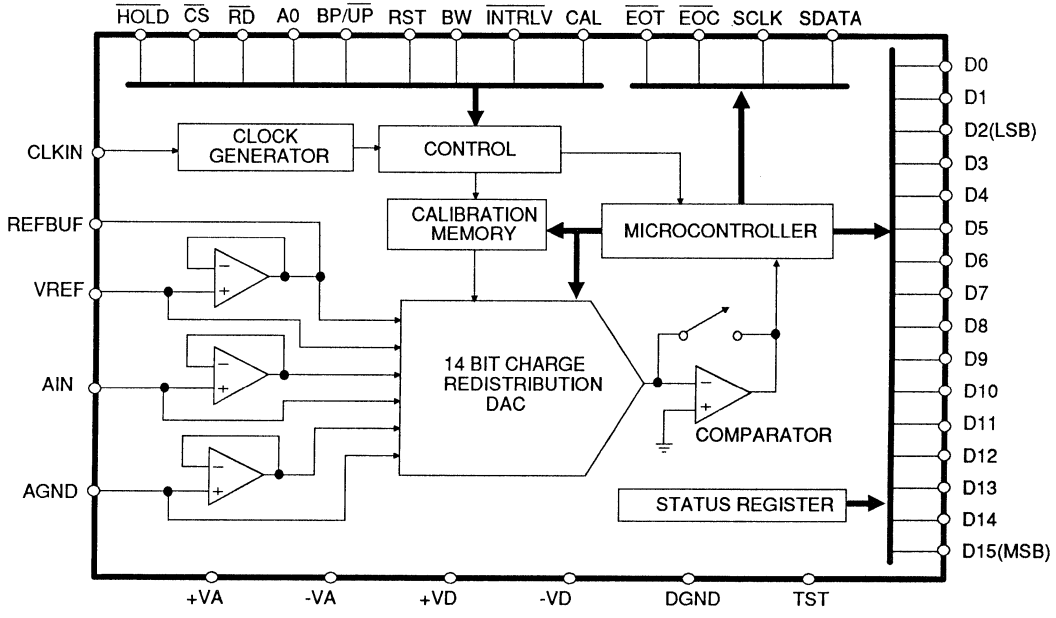

FIGURE 3. Block diagram

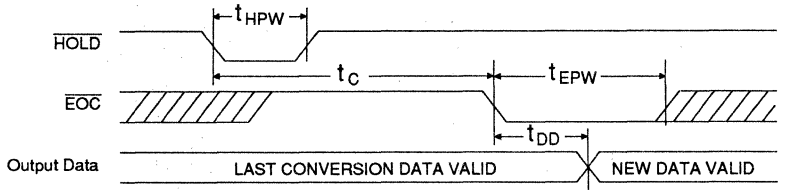

FIGURE 4. Conversion timing

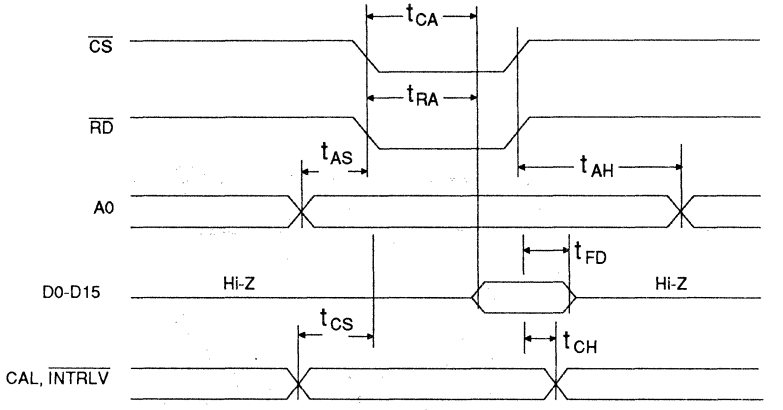

FIGURE 5. Read and calibration control timing

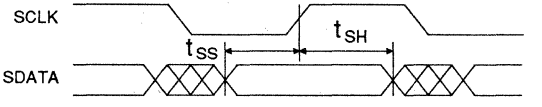

FIGURE 6. Serial output timing

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method) 5005, table I)
Interim electrical parameters (method 5004)	1, 4
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5,6, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 5 6, 10, 9**, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3

* PDA applies to subgroup 1.
** Subgroup 9 will be guaranteed if not tested.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8967401QX	0A384	CS5014-SD14B
5962-8967401XX	0A384	CS5014-SE14B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0A384	Crystal Semiconductor P.O. Box 17847 4210 South Industrial Drive Austin, Texas 78760

•Notes•

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

This copy of the CS5016 SMD is for information only. Always obtain the current SMD directly from DESC. In addition, check with Crystal Semiconductor for any upcoming SMD upgrades and additions.

REV																										
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Defense Electronics Supply Center Dayton, Ohio	PREPARED BY	MILITARY DRAWING This drawing available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY	
Original Date of drawing:	APPROVED BY	TITLE: Microcircuits, Linear, Micro-Processor Compatible, 16-bit Analog-to-Digital Converter, CMOS, Monolithic Silicon
	SIZE / CODE IDENT. NO. 67268	DWG NO. 5962-89676
AMSC N/A	REV	PAGE 1 OF 13

DISTRIBUTION STATEMENT A. Approved for public release; distribution unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit Function
01	CS5016	16-bit CMOS A/D converter, 16.25 us

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings 1/

Positive digital supply ($+V_D$) voltage range	-0.3 V dc to +6.0 V dc 2/
Negative digital supply ($-V_D$) voltage range	+0.3 V dc to -6.0 V dc
Positive analog supply ($+V_A$) voltage range	-0.3 V dc to +6.0 V dc
Negative analog supply ($-V_A$) voltage range	+0.3 V dc to -6.0 V dc
Analog ground (AGND) to digital ground (DGND)	$\pm$0.5 V dc
Input current, any pin except supplies	$\pm$10 mA 3/
Analog input voltage (AIN and VREF pins)	$-V_A$ - 0.3 V dc to $+V_A$ + 0.3 V dc
Digital input voltage	-0.3 V dc to $+V_D$ + 0.3 V dc
Storage temperature range	-65 °C to +150 °C
Lead temperature (soldering 10 seconds)	260 °C
Junction temperature (T_J)	195 °C
Power dissipation, Case Q (P_D)	1500 mW
Power dissipation, Case X (P_D)	1100 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case Q	45 °C/W
Case X	60 °C/W

1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T_A)	-55 °C to +125 °C
Positive digital supply voltage ($+V_D$)	+4.5 V dc to $+V_A$ V dc 2/
Negative digital supply voltage ($-V_D$)	-4.5 V dc to -5.5 V dc
Positive analog supply voltage ($+V_A$)	+4.5 V dc to +5.5 V dc
Negative analog supply voltage ($-V_A$)	-4.5 V dc to -5.5 V dc
Digital ground (DGND)	0 V dc
Analog ground (AGND)	0 V dc
Digital input low voltage (V_{IL})	-0.3 V dc to +0.8 V dc
Digital input high voltage (V_{IH})	+2.0 V dc to $+V_D$
Analog reference input voltage (VREF) range	+4.5 V dc
Analog input voltage range: Unipolar mode	AGND to +VREF
Bipolar mode	-VREF to +VREF

1/ All voltages referenced to AGND and DGND tied together.

2/ In addition, $+V_D$ must not be greater than $+V_A$ + 0.3 V dc.

3/ Transient currents of up to 100 mA will not cause latch-up.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Resolution for which no missing codes is guaranteed	RES	1/	1, 2, 3	16		Bits
Integral linearity error	INL	1/ 2/	1, 2, 3		±5.0 *	LSB
Full-scale error	FSE	1/ 2/	1, 2, 3		±4.0 **	LSB
Full-scale error drift	$dFSE/d_t$	1/ 2/ 3/ 4/	2, 3		±4.0	LSB
Unipolar offset error	VOFF	1/ 2/	1, 2, 3		±4.0 **	LSB
Unipolar offset error drift	$dVOFF/d_t$	1/ 2/ 3/ 4/	2, 3		±2.0	LSB
Bipolar offset error	BOFF	1/ 2/	1, 2, 3		±4.0 ***	LSB
Bipolar offset error drift	$dBOFF/d_t$	1/ 2/ 3/ 4/	2, 3		±3.0	LSB
Bipolar negative full-scale error	BNFSE	1/ 2/	1, 2, 3		±5.0 **	LSB
Bipolar negative full-scale error drift	$dBNFSE/d_t$	1/ 2/ 3/ 4/	2, 3		±3.0	LSB

See footnotes at end of table.

* An improved version is available with a specification of ±1.0LSB. An SMD revision is underway.

** An improved version is available with a specification of ±3.0LSB. An SMD revision is underway.

*** An improved version is available with a specificaiton of ±2.0LSB. An SMD revision is underway.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Peak harmonic or spurious noise	S/PN	1/ 2/ 1 kHz input, full scale amplitude, bipolar mode	4, 5, 6	92 *		dB
		1/ 2/ 12 kHz input, full scale amplitude, bipolar mode		82 **		dB
Signal to noise ratio	S/(N+D)	1/ 2/ 1 kHz input, full scale amplitude, bipolar mode	4, 5, 6	84 ***		dB
Analog input capacitance in fine charge mode	C_{IN}	Unipolar mode $T_A = +25^{o}C$ 1/ 3/	4		375	pF
		Bipolar mode $T_A = +25^{o}C$ 1/ 3/			220	
Digital input voltage ($\overline{HOLD}$, CLKIN, $\overline{CAL}$, $\overline{INTRLV}$, BW, $\overline{RST}$, BP/$\overline{UP}$, A0, $\overline{RD}$, $\overline{CS}$)	V_{IH}	5/ 6/	1, 2, 3	2.0		V
	V_{IL}				0.8	
Digital input current	I_{IN}	5/ 6/	1, 2, 3	-10	10	uA
Digital output voltage (D0-D15, SDATA, SCLK, $\overline{EOC}$, $\overline{EOT}$)	V_{OL}	Logic "0", I_{SINK}=-1.6mA, 5/, 6/	1, 2, 3		0.4	V
	V_{OH}	Logic "1", I_{SOURCE}=100uA, 5/,6/		$+V_D$ - 1.0		

See footnotes at end of table.

* An improved version is available with a specification of 100dB. An SMD revision is underway.

** An improved version is available with a specification of 85dB. An SMD revision is underway.

*** An improved version is available with a specification of 90dB. An SMD revision is underway.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
High impedance state output current	I_{OZ}	Pins D0 to D15 only, 5/ 6/	1, 2, 3		±10	uA
Conversion time	t_C	1/ 6/ 7/	9, 10, 11		16.25	us
Acquisition time	t_{ACQ}	$T_A = +25^{o}C$ 1/ 2/ 3/ 8/	9		3.75	us
Throughput	t_{PUT}	1/ 2/ 6/	9, 10, 11	50		kHz
Positive analog supply current	IA+	6/ 9/ $+V_A, +V_D = 5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		19.0	mA
Negative analog supply current	IA-	6/ 9/ $+V_A, +V_D = 5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		19.0	mA
Positive digital supply current	ID+	6/ 9/ $+V_A, +V_D = 5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		6.0	mA
Negative digital supply current	ID-	6/ 9/ $+V_A, +V_D = 5.5V$ $-V_A, -V_D = -5.5V$	1, 2, 3		6.0	mA
Master clock frequency 10/	f_{CLK}	Internally generated, CLKIN = 0 V dc, $+V_D$, $+V_A = 4.5V$, $T_A = -55^{o}C$, $-V_D$, $-V_A = -4.5V$	11	1.75		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics.- continued

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$ unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{HOLD}$ pulse width	t_{HPW}	5/ 6/ 11/ (see figure 4)	9, 10, 11	$1/f_{CLK}$ +50	t_C	ns
Data delay time	t_{DD}	5/ 6/ 11/ (see figure 4)	9, 10, 11		100	ns
$\overline{EOC}$ pulse width	t_{EPW}	5/ 6/ 11/ (see figure 4)	9, 10, 11	$4/f_{CLK}$ -20		ns
CAL, $\overline{INTRLV}$ to $\overline{CS}$ low setup time	t_{CS}	5/ 6/ 11/ (see figure 5)	9, 10, 11	20		ns
A0 to $\overline{CS}$ and $\overline{RD}$ low setup time	t_{AS}	5/ 6/ 11/ (see figure 5)	9, 10, 11	20		ns
$\overline{CS}$ or $\overline{RD}$ High to A0 invalid hold time	t_{AH}	5/ 6/ 11/ (see figure 5)	9, 10, 11	50		ns
$\overline{CS}$ High to CAL, $\overline{INTRLV}$ invalid hold time	t_{CH}	5/ 6/ 11/ (see figure 5)	9, 10, 11	50		ns
$\overline{CS}$ low to data valid access time	t_{CA}	$\overline{RD}$ = logic "0", 5/ 6/ 11/ (see figure 5)	9, 10, 11		250 *	ns
$\overline{RD}$ low to data valid access time	t_{RA}	$\overline{CS}$ = logic "0", 5/ 6/ 11/ (see figure 5)	9, 10, 11		250 *	ns
Output float delay	t_{FD}	5/ 6/ 11/ (see figure 5)	9, 10, 11		250 **	ns
SDATA to SCLK rising setup time	t_{SS}	5/ 6/ 11/ (see figure 6)	9, 10, 11	$2/f_{CLK}$ -50		ns
SCLK rising to SDATA hold time	t_{SH}	5/ 6/ 11/ (see figure 6)	9, 10, 11	$2/f_{CLK}$ -100		ns

See footnotes at end of table.

* This specification is currently being reduced to 150ns. Contact Crystal for the latest information.

** This specification is currently being reduced to 140ns. Contact Crystal for the latest information.

TABLE I. Electrical performance characteristics footnotes.

1/ $+V_A$, $+V_D$ = +5.0 V; $-V_A$, $-V_D$ = -5.0 V; VREF = +4.5 V dc; f_{CLK} = 4 MHz; Analog source impedance = 200 ohms; Error tests are done after calibration at the temperature of interest.

2/ Synchronous sampling mode ($\overline{EOT}$ connected to $\overline{HOLD}$), Interleave disabled.

3/ This parameter shall be measured only for initial characterization and after process or design changes which may affect this parameter.

4/ Total drift over -55°C to +125°C since calibration at power-up at +25°C.

5/ $+V_A$, $+V_D$ = +5.0 V dc ± 10%; $-V_A$, $-V_D$ = -5.0 V dc ± 10%

6/ This parameter is guaranteed, if not tested, at T_A = +25°C.
This parameter is tested at T_A = -55°C and +125°C.

7/ Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.

8/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.

9/ All outputs unloaded; All inputs swinging between $+V_D$ and 0 V dc.

10/ Externally supplied maximum clock frequency is 4MHz. Analog parametric measurements are done with the maximum external clock (see footnote 1/).

11/ Inputs: logic "0" = 0 V, logic "1" = $+V_D$; C_L = 50 pF.

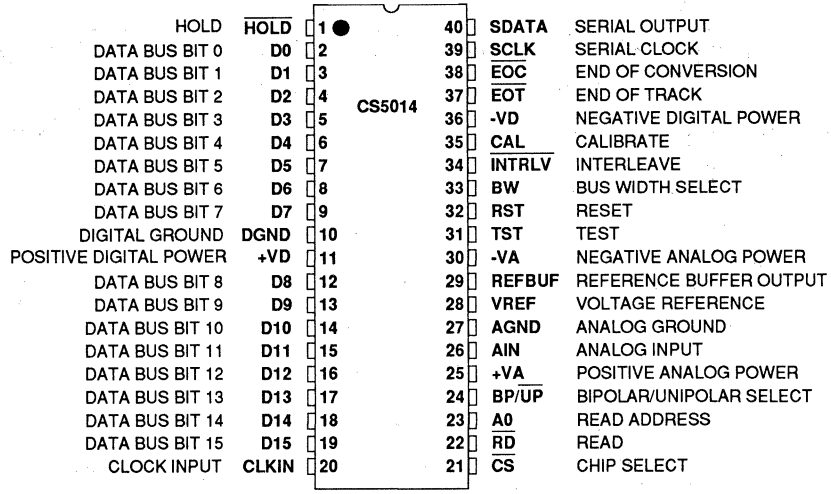

FIGURE 1. Terminal connections for Q case outline

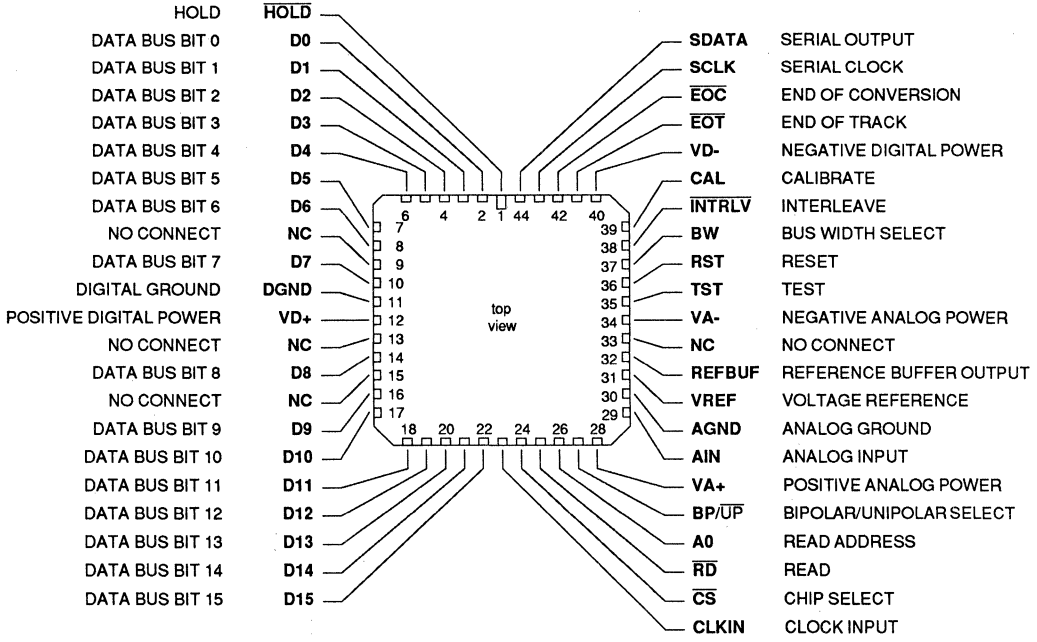

FIGURE 1. Terminal connections for X case outline

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

FIGURE 2. Truth table

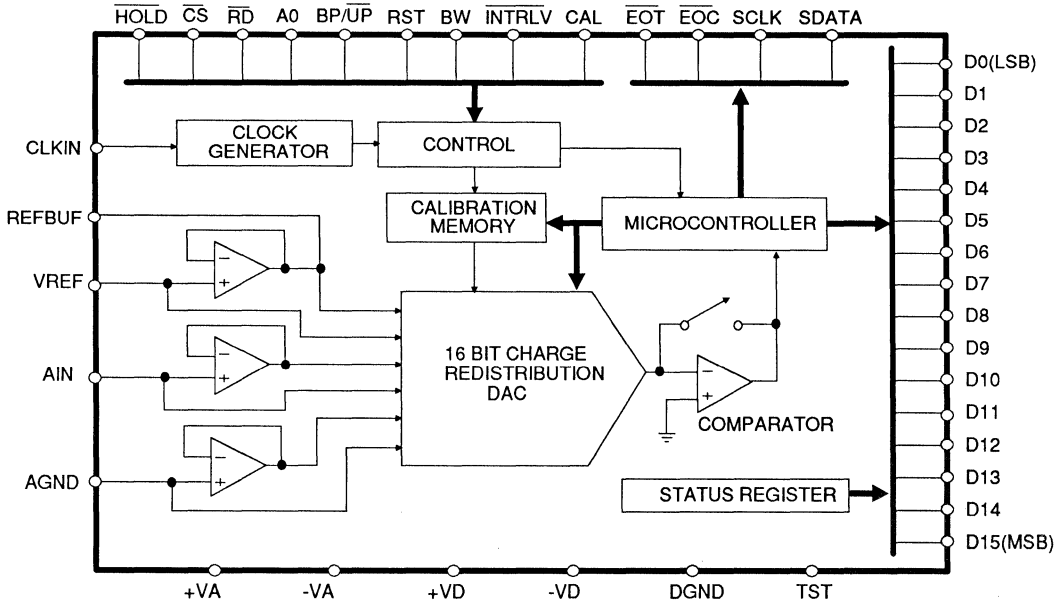

FIGURE 3. Block diagram

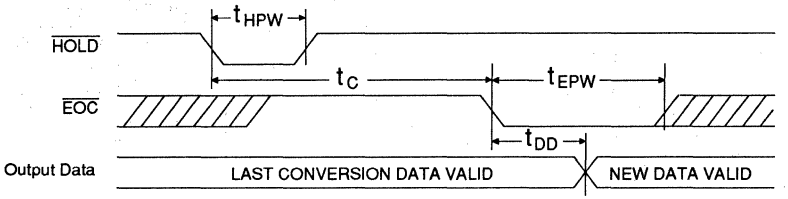

FIGURE 4. Conversion timing

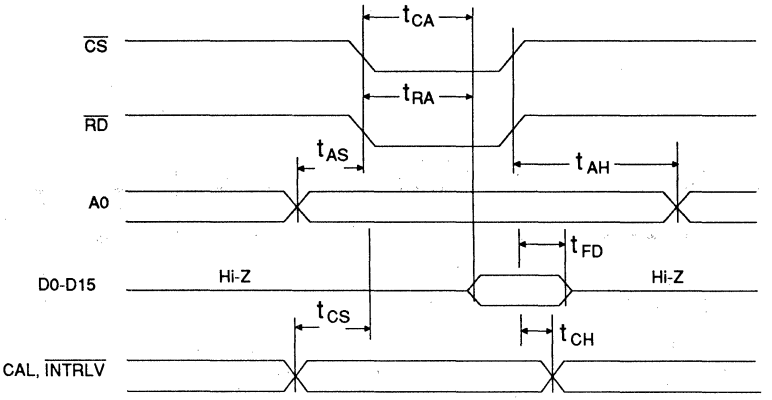

FIGURE 5. Read and calibration control timing

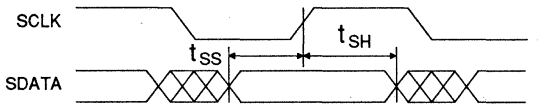

FIGURE 6. Serial output timing

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

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4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 4
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 9**, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3

* PDA applies to subgroup 1.
** Subgroup 9 will be guaranteed if not tested.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8967601QX	0A384	CS5016-SD16B
5962-8967601XX	0A384	CS5016-SE16B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0A384	Crystal Semiconductor P.O. Box 17847 4210 South Industrial Drive Austin TEXAS 78760

•Notes•

REVISIONS			
LTR.	DESCRIPTION	DATE	APPROVED

The CS5412 Standard Military Drawing is in development at Crystal and DESC. Contact Crystal or DESC for the latest information.

REV																												
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OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15												

Defense Electronics Supply Center Dayton, Ohio	PREPARED BY	MILITARY DRAWING This drawing available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY	
Original Date of drawing:	APPROVED BY	TITLE: Microcircuits, Linear, Micro-Processor Compatible, 12-bit Analog-to-Digital Converter, CMOS, Monolithic
	SIZE / CODE IDENT. NO. 14933	DWG NO. TO BE ASSIGNED
AMSC N/A	REV	PAGE 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

CRYSTAL5412	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Signal to (noise + distortion)	Linearity
01	CS5412-TC1	68 dB	±2.0 LSB
02	CS5412-SC1	65 dB	±3.0 LSB

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096"X.620"X.225") dual-in-line package.
X	C-J1 (44-lead, 0.658" SQ X.190"),J bend leaded chip carrier package.

1.3 Absolute maximum ratings.

Positive digital supply (VD+) voltage range	-0.3 V dc to +6.0 V dc	1/, 2/
Negative digital supply (VD-) voltage range	+0.3 V dc to -6.0 V dc	1/
Positive analog supply (VA+) voltage range	-0.3 V dc to +6.0 V dc	1/, 3/
Negative analog supply (VA-) voltage range	+0.3 V dc to -6.0 V dc	1/
Analog ground (AGND) to digital ground (DGND)	+XXX V dc	
Input current, any pin except supplies	±10 mA	4/
Analog input voltage (AIN and VREF pins)	VA- - 0.3 V dc to VA+ + 0.3 V dc	1/, 5/
Digital input voltage	-0.3 V dc to VA+ + 0.3 V dc	1/, 5/
Storage temperature range	-65 °C to +150 °C	
Lead temperature (soldering 10 seconds)	+260 °C	
Junction temperature (T_J)	+160 °C	
Power dissipation	1500 mW	
Thermal resistance (θ_{JA})	60 °C/W	

1.4 Recommended operating conditions.

Ambient operating temperature range (T_A)	-55 °C to +125 °C	
Positive digital supply voltage (VD+)	+4.5 V dc to VA+ V dc	1/, 5/
Negative digital supply voltage (VD-)	-4.5 V dc to -5.5 V dc	1/
Positive analog supply voltage (VA+)	+4.5 V dc to +5.5 V dc	1/
Negative analog supply voltage (VA-)	-4.5 V dc to -5.5 V dc	1/
Digital ground (DGND)	0 V dc	1/
Analog ground (AGND)	0 V dc	1/
Digital input low voltage (V_{IL})	-0.3 V dc to +0.8 V dc	1/
Digital input high voltage (V_{IH})	+2.0 V dc to VD+ + 0.5 V dc	1/
Analog input voltage range	VREF- TO VREF+	1/
Unipolar Analog reference input voltage (VREF) range:		
VREF+	+2.0 V dc to +3.0 V dc	1/
VREF-	AGND	
Bipolar Analog reference input voltage (VREF) range:		
VREF+	+1.0 V dc to +1.5 V dc	1/
VREF-	-1.0 V dc to -1.5 V dc	1/

1/ All voltages referenced to AGND and DGND tied together.

2/ In addition, VD+ must not be greater than VA2+ or VA5+ + 0.3 V dc.

3/ VA1+, VA3+, and VA4+ must never exceed VA2+ and VA5+ by more than 0.3 V.

4/ Transient currents of up to 100 mA will not cause latch-up.

5/ VA- = most negative of VA1- and VA3-,
VA+ = most positive of VA2+ and VA5+.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended ambient operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$		Group A subgroups	Limits		Unit
					Min	Max	
Resolution for which no missing codes is guaranteed				1, 2, 3	12		Bits
Integral linearity error	INL	1/	Device type 01	1, 2, 3		±2.0	LSB
			Device type 02			±3.0	
Differential linearity error	DNL	1/	Device type 01	1, 2, 3	-0.9	+1.25	LSB
			Device type 02			NMC	
Full-scale error	FSE	1/		1, 2, 3		±10	LSB
Offset error	OFF	1/, 2/		1, 2, 3		±4	LSB
Peak harmonic or spurious noise	S/PN	100 kHz input	Device type 01	4, 5, 6	75		dB
			Device type 02		75		
Signal to noise ratio	S/(N+D)	0 dB input (full-scale)	Device type 01	4, 5, 6	68		dB
			Device type 02		65		
Digital input capacitance	C_{IN}			4		10	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$	Group A subgroups	Limits		Unit
				Min	Max	
Input voltage ($\overline{RST}$, CCNV, CAL, $\overline{RD}$, $\overline{CS}$)	V_{IH}		1	2.0		V
	V_{IL}				0.8	
Input voltage ($\overline{HOLD}$, CLKIN)	V_{IH}		1	VD+ - 0.5		V
	V_{IL}				0.5	
Input current	I_{IN}		1	-10	10	uA
Output voltage (D0-D11, $\overline{DRDY}$, OVRNG)	V_{OL}	Logic "0", I_{SINK} = -1.6 mA	1		0.4	V
	V_{OH}	Logic "1", I_{SOURCE} = 100 uA		VD+ - 1.0		
High impedance state output current	I_Z	Pins D0 to D11 only.	1	-10	10	uA
Functional tests		See paragraph 4.3.1d.	7			
Conversion time	t_C	3/, 4/	9, 10, 11	1.25	1.375	us
Acquisition time	t_{ACQ}	5/	9, 10, 11		300	ns
Throughput	t_{PUT}	4/	9, 10, 11	1		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55^{o}C \leq T_A \leq +125^{o}C$	Group A subgroups	Limits		Unit
				Min	Max	
Positive analog supply current	IA+	1/, 6/	1, 2, 3		90	mA
Negative analog supply current	IA-	1/, 6/	1, 2, 3	90		mA
Positive digital supply current	ID+	1/, 6/	1, 2, 3		10	mA
Negative digital supply current	ID-	1/, 6/	1, 2, 3	10		mA
Power dissipation	P_D	1/, 6/	1, 2, 3		1000	mW
Master clock frequency	f_{CLK}	7/	9, 10, 11	3	8	MHz
State 7 to $\overline{\text{HOLD}}$ low	t_{HA}	7/ (See figure 4)	9, 10, 11	62.5		ns
$\overline{\text{HOLD}}$ low to state 0	t_{HB}	7/ (See figure 4)	9, 10, 11	0		ns
State 0 to $\overline{\text{HOLD}}$ high	t_{HC}	7/ (See figure 4)	9, 10, 11	75		ns
$\overline{\text{HOLD}}$ high to state 7	t_{HD}	7/ (See figure 4)	9, 10, 11	30		ns
$\overline{\text{DRDY}}$ pulse width	t_{DPW}	7/, 9/? (See figure 5)	9, 10, 11	3	3	MCC
Data delay time	t_{DD}	7/ (See figure 5)	9, 10, 11		50	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. (continued)

Test	Symbol	Conditions $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{CS}$ low to data valid access time	t_{CSA}	7/, 8/ (See figure 6)	9, 10, 11		110	ns
$\overline{RD}$ low to data valid access time	t_{RDA}	7/, 8/ (See figure 6)	9, 10, 11		110	ns
Output float delay ($\overline{CS}$ or $\overline{RD}$ high to high-Z)	t_{FD}	7/, 8/ (See figure 6)	9, 10, 11		110	ns
CAL pulse width (CAL and $\overline{CS}$ low)	t_{CSH}	7/, 9/ (See figure 6)	9, 10, 11	2		MCC
$\overline{RST}$ pulse width	t_{RPW}	7/, 9/	9, 10, 11	2		MCC

1/ All VA+, VD+ = +5.0 V; all VA-, VD- = -5.0 V; VREF+ = +1.5 V dc; VREF+ = +1.5 V dc; f_{CLK} = 8 MHz; 100 kHz input sinewave; Error tests are done after calibration at the temperature of interest.

2/ Worst case conditions: unipolar (VREF- = 0 V) or bipolar (VREF- = -1.5 V) input range.

3/ Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{DRDY}$.

4/ Applies for conversions triggered externally. In continuous convert mode throughput proceeds at 1/8 master clock frequency with a fixed 10 clock cycle conversion time.

5/ The internal track-and-hold returns to the track mode on the fourth master clock cycle after the start of a conversion cycle. It is guaranteed to acquire a full-scale step to 12-bit accuracy while operating at full throughput.

6/ All outputs unloaded. All inputs CMOS levels.

7/ Logic 0 = 0 V, Logic 1 = VD+; C_L = 50 pF.

8/ Data goes valid when both $\overline{CS}$ and $\overline{RD}$ are low simultaneously. Each access time assumes other control is already low or falls concurrently.

9/ MCC = 1 master clock cycle.

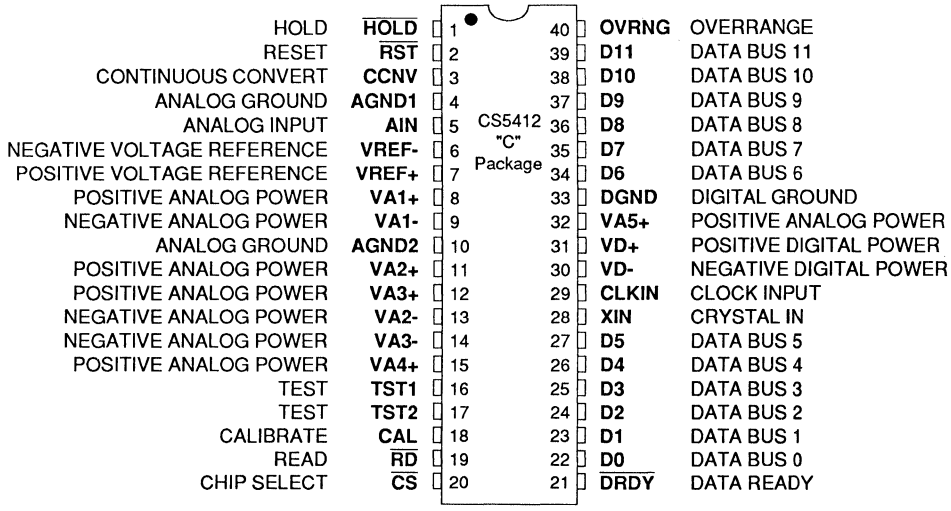
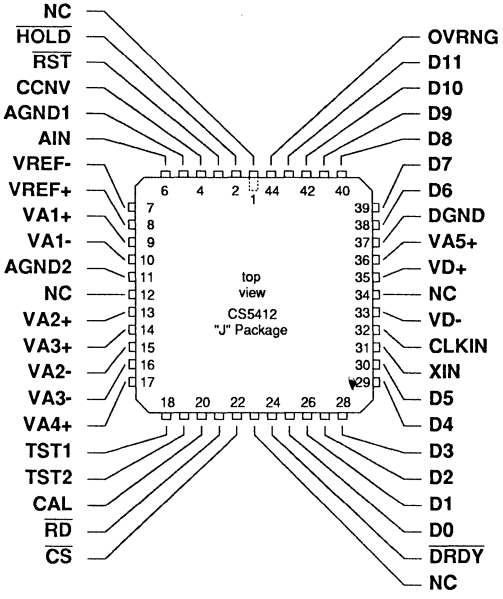


FIGURE 1. Terminal connections



MILITARY DRAWING	SIZE	CODE IDENT. NO. 14933	DWG NO. TO BE ASSIGNED
DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO		REV	PAGE 10-55

DESC FORM 193A
FEB 86

$\overline{CS}$	$\overline{RD}$	CCNV	$\overline{HOLD}$	CAL	$\overline{RST}$	Function
0	0	X	X	0	1	Read Output Data
*	1	X	X	*	1	High Impedance Data Bus
1	X	X	X	X	1	High Impedance Data Bus
*	X	1	1	*	1	Continuous Convert Mode
*	X	0	↓	*	1	Hold and Start Convert
X	X	X	X	X	0	Reset
0	X	X	X	1	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

FIGURE 2. Truth table

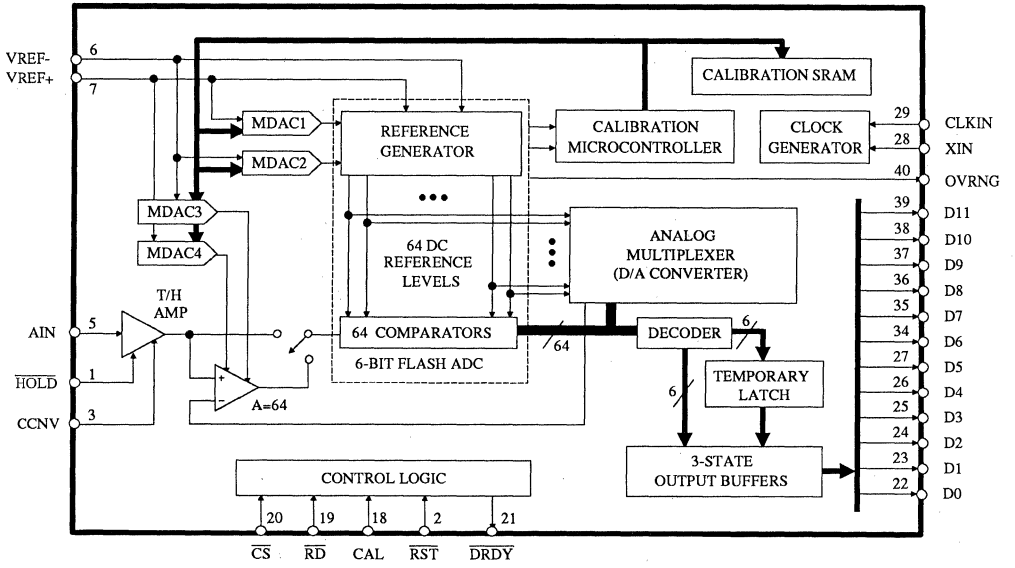


FIGURE 3. Block diagram

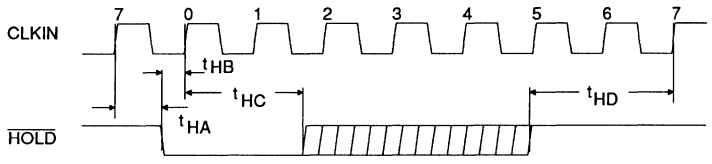


FIGURE 4. Conversion timing

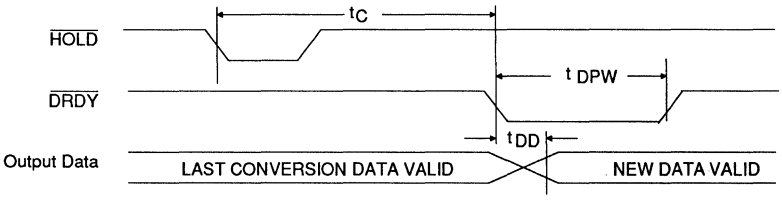


FIGURE 5. Read and calibration control timing

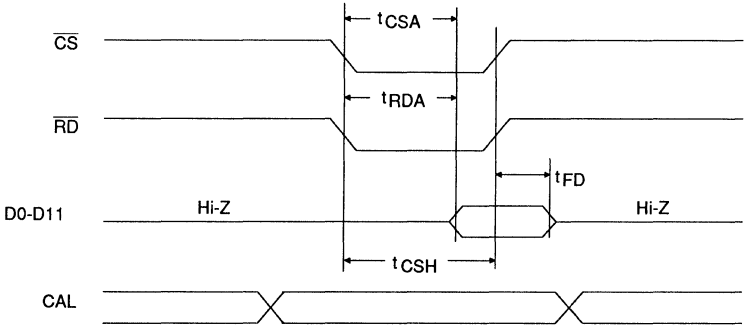


FIGURE 6. Serial output timing

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition or using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups , , and in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 tests shall verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition or using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	
Group A test requirements (method 5005)	
Groups C and D end-point electrical parameters (method 5005)	
Additional electrical subgroups for group C periodic inspections	

*PDA applies to subgroup 1.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/ .

OR

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source(s) of supply. An approved source of supply is listed (Approved sources of supply are listed) herein. Additional sources will be added as they become available. The vendor(s) listed herein has (have) agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
TBA 01	0A384	CS5412-TC1	
TBA 02	0A384	CS5412-SC1	
TBA 01	0A384	CS5412-TJ1	
TBA 02	0A384	CS5412-SJ1	

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0A384	Crystal Semiconductor P.O. Box 17847 4210 South Industrial Drive Austin, TX 78760

INTRODUCTION

High-quality evaluation boards are available to allow rapid evaluation of Crystal products, often freeing the customer from the task of initial breadboarding. The layout and grounding schemes may be used as quidelines for the customer's own system design. Isolation of system problems can be aided by comparison with the evaluation board operation.

USER'S GUIDE

Device:	Crystal Part Included	Basic Function
CDB31412	CS31412-KC1	Quad Sample/Hold
CDB5012	CS5012A-KP7	12-Bit 7 µs, 100kHz, A-to-D
CDB5014	CS5014-KP14	14-Bit, 14 µs, 55kHz, A-to-D
CDB5016	CS5016-KP16	16-Bit, 16 µs, 50kHz, A-to-D
CDB5101	CS5101-KP8	16-Bit, 8 µs, 100 kHz, A-to-D
CDB5102	CS5102-KP	16-Bit, 40 µs, 20kHz, A-to-D
CDB5126	CS5126-KP	Digital Audio A-to-D
CDB5317	CS5317-P	84 dB Voice-Band, A-to-D
CDB5324	CS5324-BL	120 dB, 500Hz, A-to-D
CDB5326	CS5326-KP	16-Bit, Digital Audio A-to-D
CDB5327	CS5327-KP	16-Bit, Digital Audio A-to-D
CDB5328	CS5328-KP	18-Bit, Digital Audio A-to-D
CDB5329	CS5329-KP	18-Bit, Digital Audio A-to-D
CDB5336	CS5336-KP	16-Bit, Digital Audio A-to-D
CDB5337	CS5337-KP	16-Bit, Digital Audio A-to-D
CDB5338	CS5338-KP	16-Bit, Digital Audio A-to-D
CDB5339	CS5339-KP	16-Bit, Digital Audio A-to-D
CDB5412	CS5412	12-Bit, 1 MHz, A-to-D
CDB5501	CS5501-KP	16-Bit, dc Measurement A-to-D
CDB5503	CS5503-KP	20-Bit, dc Measurement A-to-D
CDB7008	CS7008-C	Switched Cap Filter

CONTENTS

Semiconductor Corporation

CDB31412

CS31412 Evaluation Board

Features

- Industry Standard Header Connector
- BNC Connectors for Analog I/O's
- DIP-Switch Selectable
  Differential & Single-Ended Modes
  Analog Mux Configuration
- Push Button Reset and Calibration
- User Configurable Ground Planes

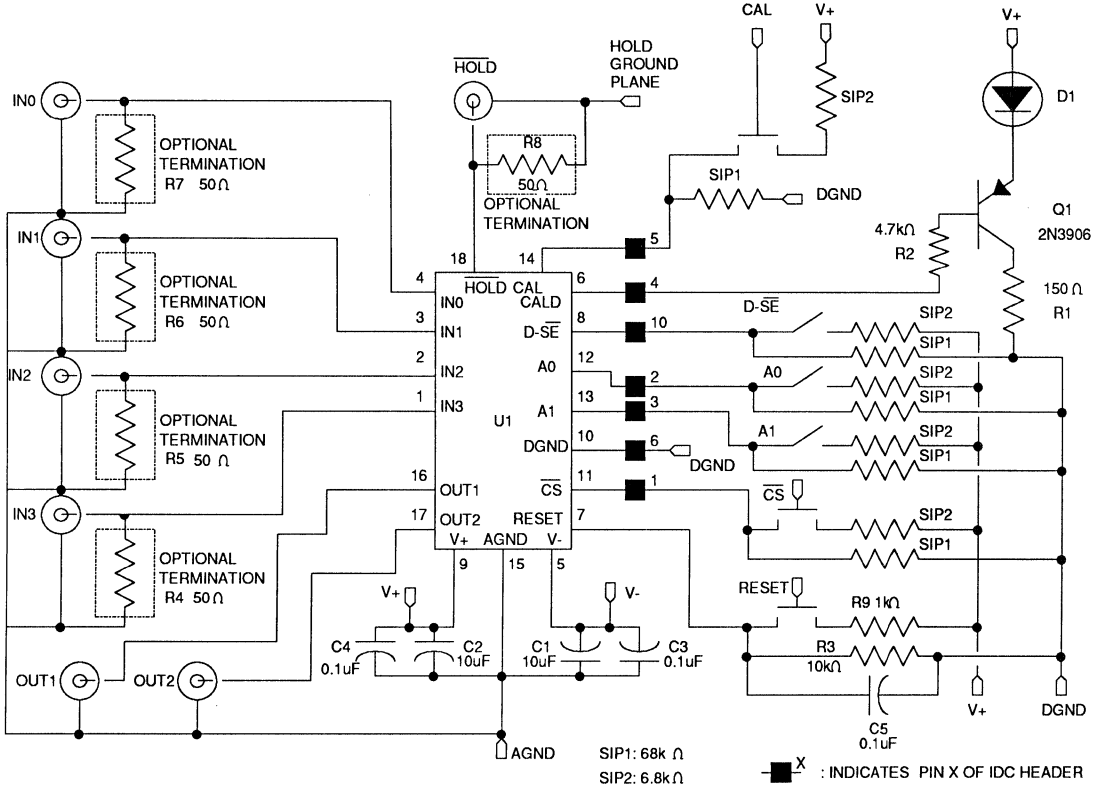
General Description

The CDB31412 Evaluation Board is designed to allow the user to quickly evaluate the performance of the CS31412 Simulaneous Track-and-Hold.

All analog inputs and outputs can be interfaced to the board with coaxial BNC connectors. Optional termination resistors can also be added.

A 10 pin IDC header is provided for microprocessor control.

ORDERING INFORMATION: CDB31412



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Analog Input and Output Connections

The four analog inputs to the CS31412 are connected to the CDB31412 via the BNC coaxial connectors labeled IN0, IN1, IN2, IN3. These inputs have locations reserved for termination resistors if they are needed. The analog outputs from the CS31412 are available at the BNC coaxial connectors labeled OUT1, and OUT2.

DIP-Switch Configuration

The input mode is controlled by the D-$\overline{SE}$ switch of DIP-switch SW4. If it is off, the part is in single-ended mode (4-to-1 mux). If it is on, the part is in the differential mode (dual 2-to-1 mux). After changing the differential mode switch position, the $\overline{CS}$ pushbutton must be depressed to internally latch the part. The CS31412 must be calibrated after switching between single-ended and differential modes.

The A1 and A0 switches of DIP-switch SW4 control the CS31412's output control mux. The chart below summarizes the DIP-switch configurations.

Reset and Calibration

The CS31412 will usually reset itself upon power-up. Since this function is not guaranteed, the chip must be reset upon power-up in system operation. The part can be reset on the CDB31412 board by momentarily depressing pushbutton SW3. To initiate a calibration, depress pushbutton SW1. The LED will turn on for approximately 500 ms, indicating that the part is being calibrated. Once the LED goes off, the CS31412 is ready for operation.

Microprocessor Interface

The CAL, $\overline{CS}$, A0, A1, and D-$\overline{SE}$ inputs and the CALD output are available at the 10 pin IDC header. The five inputs are pulled low through 68 kΩ resistors placing the CS31412 in a microprocessor independent mode. These inputs may be pulled high by the DIP-switches and pushbutton or by driving the 10-pin IDC header. When using the header to externally drive these inputs, the three DIP-switches controlling A0, A1, and D-$\overline{SE}$ must be in the off position so that no loading will occur. All remaining pins of the IDC header are tied to DGND and cannot be driven.

D-$\overline{SE}$	A1	A0	OUT1	OUT2
off	off	off	IN0	0.0V
off	off	on	IN1	0.0V
off	on	off	IN2	0.0V
off	on	on	IN3	0.0V
on	off	off	IN0	IN1
on	on	off	IN2	IN3

Figure 1. Dip-Switch Configuration

Decoupling

The CDB31412's decoupling scheme was designed to insure accurate evaluation of the CS31412's performance independent of the quality of the power supplies. Each supply is decoupled at the part with a 10 µF electrolytic capacitor to filter low-frequency noise and a 0.1 µF ceramic capacitor to handle higher frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

Ground Planes

The CDB31412 has three separate ground planes which may be interconnected by the user to simulate actual system conditions. When shipped from the factory, the analog ground plane, the digital ground plane, and the hold ground plane are separate. Jumpers J1, J2, J3, and J4 are used to interconnect these ground planes. Separate ground planes are the suggested configuration for best performance of the part. For more information on grounding, Application Note: "Suggested Grounding and Supply Arrangements for the CS31412" is recommended.

COMPONENT LIST

150 Ω resistor	R1
4.7 kΩ resistor	R2
10 kΩ resistor	R3
1 kΩ resistor	R9
68.0 kΩ sip resistor	SIP1
6.8 kΩ sip resistor	SIP2
0.1 µF capacitor	C3, C4, C5
10 µF capacitor	C1, C2
CS31412 Track/Hold	U1
2N3906 transistor	Q1
LED	D1
3 pos. SPST DIP switch	SW4
SPST pushbutton	SW1, SW2, SW3
10 pin header	P12
PC-mount BNC	P5, P6, P7, P8, P9, P10, P11
red banana jack	P1
black banana jack	P3, P4
green banana jack	P2
1" 4-40 spacer	POST1, POST2, POST3, POST4
3/8" 4-40 screw	SC1, SC2, SC3, SC4

• Notes •

Evaluation Board for CS5012, CS5014, CS5016 ADC's

Features

- Compatible with CS5012, CS5014, CS5016
- PC/uP-Compatible Header Connection
  - 16-Bit Parallel Data
  - End-of-Conversion Output
  - $\overline{CS}$, $\overline{RD}$, and A0 Control Inputs
- DIP-Switch Selectable:
  - Unipolar/Bipolar Input Range
  - Burst & Interleave Calibration Modes
  - Continuous Conversion
- Adjustable Voltage Reference
- Serial Data and Clock BNC Connections
- Operation from Internally-Generated or Externally-Supplied Master Clock

General Description

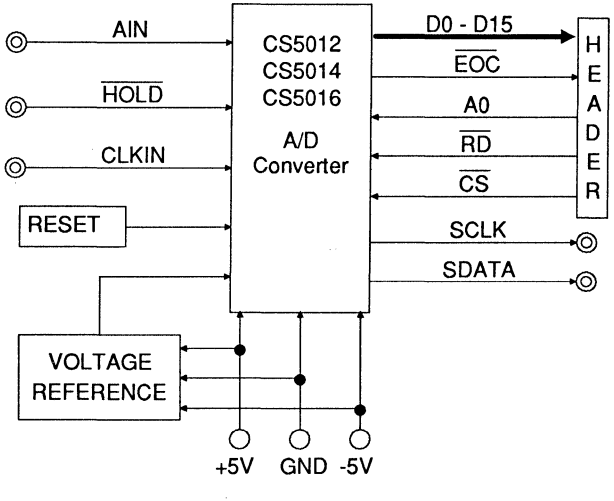
The CDB5012/4/6 is an evaluation board that eases the laboratory characterization of any of the CS5012, CS5014 and CS5016 A/D converters. The board can be easily reconfigured to simulate any combination of sampling, master clock, calibration, and input range conditions.

The converter's parallel output data are available at a 40 pin strip header allowing easy interfacing to PC's or microprocessor busses. Output data is also available in serial form at SCLK and SDATA coaxial BNC connectors.

Evaluation can also be performed over a wide range of input spans using the on-board reference circuitry. Furthermore, the CDB5012,4,6 features DIP-switch selectable unipolar/bipolar input ranges and two calibration modes: burst and interleave cal. Calibration can be initiated at any time by momentarily depressing a reset pushbutton.

ORDERING INFORMATION: CDB5012, CDB5014, CDB5016

Block Diagram



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Analog Input

The analog input to the A/D converter is supplied through the BNC coaxial connector labeled AIN. Analog input polarity is controlled by the first position switch on the DIP-switch, SW-1. If it is on, the input is unipolar ranging from GND to VREF. If the switch is off, the input range is bipolar with the magnitude of the reference voltage defining both zero- and full-scale (±VREF).

The A/D converter's internal analog input buffer requires a source impedance of less than 400 Ω at 1MHz for stability. Acquisition and throughput are specified assuming a dc source impedance of less than 200 Ω. Infinitely large dc source impedances can be accomodated by adding capacitance (typically 1000pF) from the analog input to ground. However, high dc source resistances degrade acquisition time and consequently throughput.

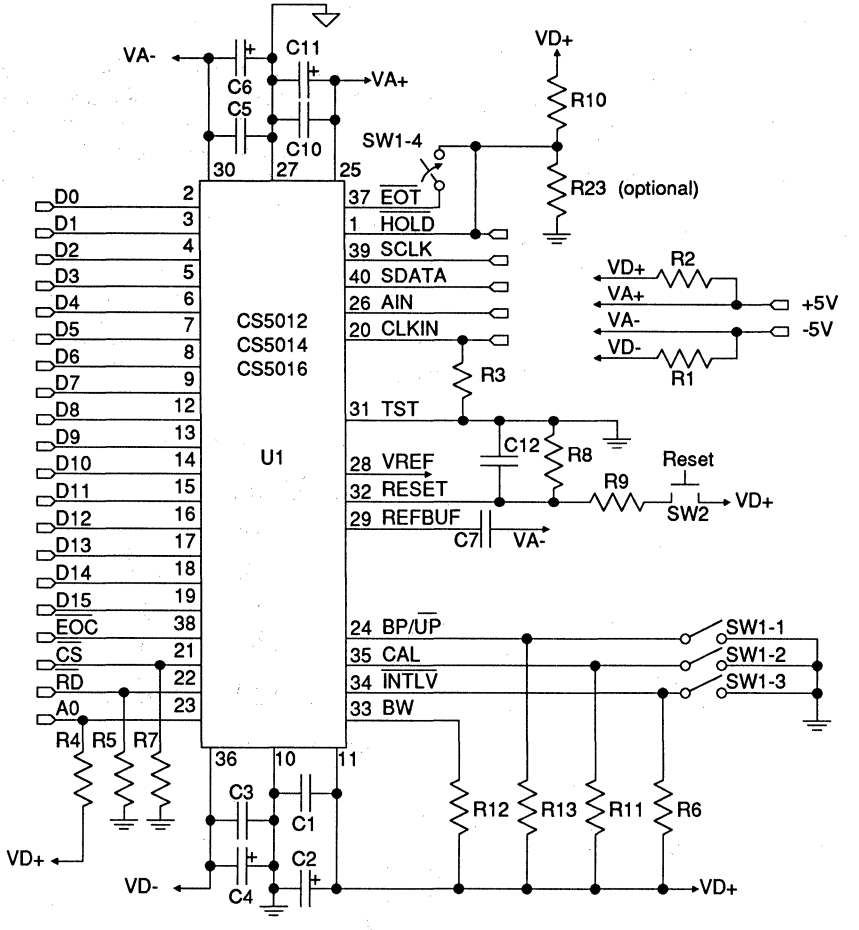


Figure 1. CDB5012,4,6 Schematic
(Reference Circuitry Appears in Figure 3)

	OFF	ON
Position 1	Bipolar	Unipolar
Position 2	Burst Cal	Normal Operation
Position 3	Normal	Interleaved Cal
Position 4	Normal	Continuous Conversion

Figure 2. DIP-Switch Definitions

Initiating Conversions

A negative transition on the converter's $\overline{\text{HOLD}}$ pin places the device's analog input into the hold mode and initiates a conversion cycle. On the CDB5012,4,6, this input can be generated by one of two means. First, it can be supplied through the BNC coaxial connector appropriately labeled $\overline{\text{HOLD}}$. Alternatively, switch position 4 of the DIP-switch can be placed in the on position, thus looping the converter's $\overline{\text{EOT}}$ output back to $\overline{\text{HOLD}}$. This results in continuous conversions at a fraction of the master clock frequency (see "synchronous operation" in the converter's data sheet).

The A/D converter's $\overline{\text{EOT}}$ output is an indicator of its acquisition status; it falls when the analog input has been acquired to the specified accuracy. If an external sampling clock is applied to the $\overline{\text{HOLD}}$ BNC connector, care must similarly be taken to obey the converter's acquisition and maximum sampling rate requirements. A more detailed discussion of acquisition and throughput can be found in the converter's data sheet.

The CDB5012,4,6 is shipped from the factory without the $\overline{\text{HOLD}}$ BNC input terminated for operation with an external sampling clock. However, location R23 is reserved for the insertion of a 51 Ω resistor to eliminate reflections of the incoming clock signal.

Voltage Reference Circuitry

The CDB5012,4,6 features an adjustable voltage reference which allows characterization over a wide range of reference voltages. The circuitry consists of a 2.5V voltage reference (1403) and an adjustable gain block with a discrete output stage (Figure 3). The output stage minimizes the output's headroom requirements allowing the reference voltage to come within 300mV of the positive supply.

The coarse and fine trim potentiometers are factory calibrated to a reference voltage of 4.5V (a table of output code values for a reference voltage of 4.5V appears in the CS5012,4,6 data sheets). When calibrating the reference, the voltage should be measured directly at the VREF input (pin 28) or at the ungrounded lead of decoupling capacitor C9.

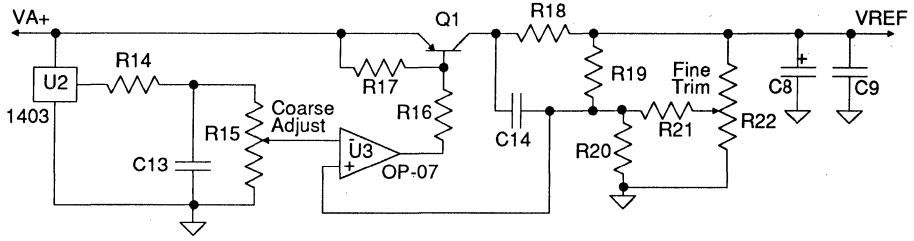


Figure 3. Voltage Reference Circuitry

Reset/Self-Calibration Modes

The A/D converter will usually reset itself upon power-up. Since this function is not guaranteed, the converter must be reset upon power-up in system operation. The converter can be reset on the CDB5012,4,6 board by momentarily depressing pushbutton SW-2 thus initiating a full calibration cycle; 1,443,840 master clock cycles later the converter is ready for normal operation.

The converters also feature two other modes of calibration: burst and interleave. Burst calibration can be initiated by moving switch position 2 on the DIP-switch to the off position. In this mode (CAL high), the A/D converter continually loops through calibration cycles until CAL returns low. Interleave can be initiated by setting switch position 3 to the on position. In the interleave mode ($\overline{\text{INTRLV}}$ low), the converter appends one small portion of a calibration cycle (20 master clock cycles) to each conversion cycle. Thus, a full calibration cycle completes every 72,192 conversion cycles.

A more detailed discussion of the converters' calibration modes and capabilities can be found in their data sheets.

Parallel Output Data/Microprocessor Interface

The converter's outputs D0-D15, its $\overline{\text{CS}}$, $\overline{\text{RD}}$, and A0 inputs, and its $\overline{\text{EOC}}$ output are available at the 40 pin header. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs are pulled low through 10 kΩ resistors placing the converter in a microprocessor-independent mode. Control input A0 is pulled up, insuring the converter's output word, rather than the status register, appears at the header.

The converter's 3-state output buffers and microprocessor interface can be exercised by driving the $\overline{\text{CS}}$ and/or $\overline{\text{RD}}$ inputs at the header. Similarly, the converter's 8-bit status register can be obtained on D0-D7 by driving A0 low.

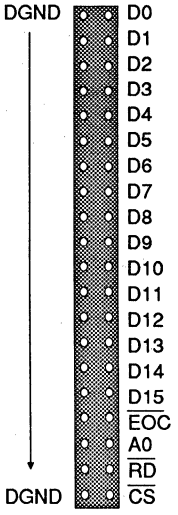


Figure 4. Header Pin Definitions

The converter's $\overline{\text{EOC}}$ and data outputs are not buffered on the CDB5012,4,6. Therefore, careful attention should be paid to the load presented by any cabling, especially if the 3-state output buffers are to be exercised at speed. Twisted ribbon cable is typically specified at 10pF/ft, so several feet can generally be accomodated.

Serial Output Data

Serial output data is available at the two BNC connections SCLK and SDATA. Data appears MSB first, LSB last, and is valid on the rising edge of SCLK.

Master Clock

The A/D converter operates from a master clock which can either be internally-generated or externally-supplied. For operation with an external clock, the BNC connector labeled CLKIN should be driven with a TTL clock signal. The CDB5012,4,6 is shipped from the factory with the CLKIN input terminated by a 51 Ω resistor to eliminate line reflections of the incoming

clock. If the CLKIN BNC input is left floating, this resistor pulls the converter's clock input down to ground, thus activating its internal oscillator.

Decoupling

The CDB5012,4,6's decoupling scheme was designed to insure accurate evaluation of the converter's performance independent of the quality of the power supplies. Each supply is decoupled at the converter with a 10µF electrolytic capacitor to filter low frequency noise and a 0.1µF ceramic capacitor to handle higher frequencies. The auto-zeroing action of the converter's comparator provides extremely good power supply rejection at low frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

COMPONENT LIST

10 Ω resistor	R1, R2
51 Ω resistor	R3
4.7 Ω resistor	R18
1 kΩ resistor	R9, R14
560 Ω resistor	R17
10 kΩ resistor	R4, R5, R6, R7, R8, R10, R11, R12, R13
2.43 kΩ resistor	R19, R20
3.3 kΩ resistor	R16
240 kΩ resistor	R21
50 kΩ potentiometer	R15
50 kΩ potentiometer	R22
0.068 µF capacitor	C14
0.1 µF capacitor	C1, C3, C5, C7, C9, C10, C12
10 µF capacitor	C2, C4, C6, C8, C11, C13
CS501X/511X A/D converter	U1
1403 2.5V reference	U2
OP07 op amp	U3
2N2907A transistor	Q1
4 pos. SPST DIP switch	SW1
N.O. SPST pushbutton	SW2
20 pin header	CON1
bulkhead BNC	CON2, CON3, CON4, CON5, CON6
red banana jack	CON7
black banana jack	CON8
green banana jack	CON9
1" 4-40 spacer	POST1, POST2, POST3, POST4, POST5, POST6
3/8" 4-40 screw	SC1, SC2, SC3, SC4, SC5, SC6

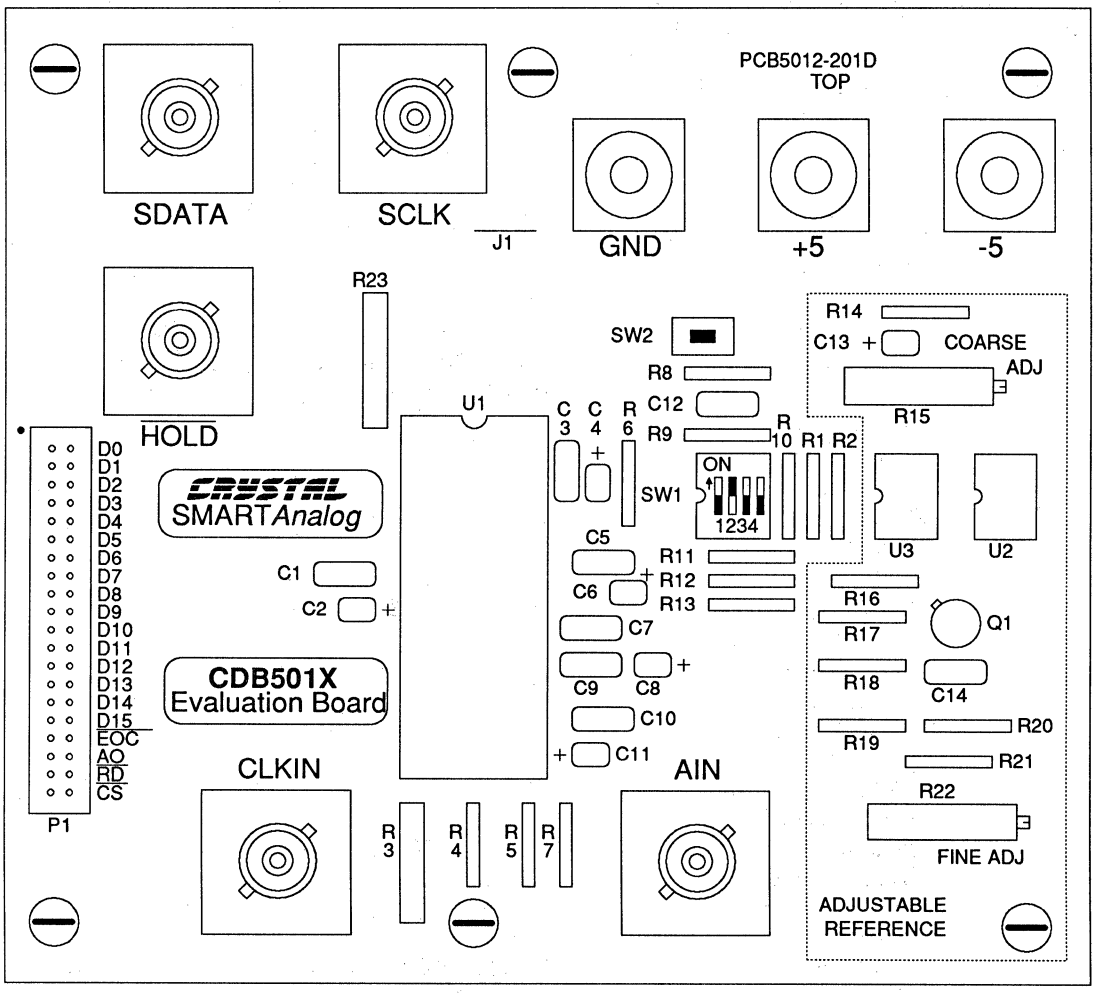


Figure 5. Board Layout

Semiconductor Corporation

CDB5101/5102/5126

Evaluation Board for CS5101 , CS5102 & CS5126

Features

- Serial to Parallel Conversion
- All Timing Signals Provided
- Adjustable Voltage Reference
- ± 5 V Regulators
- Digital and Analog Patch Areas

General Description

The CDB5101/5102/5126 Evaluation Board allows fast evaluation of the CS5101, CS5102 and/or CS5126 2-Channel, 16-bit Analog-to-Digital Converters.

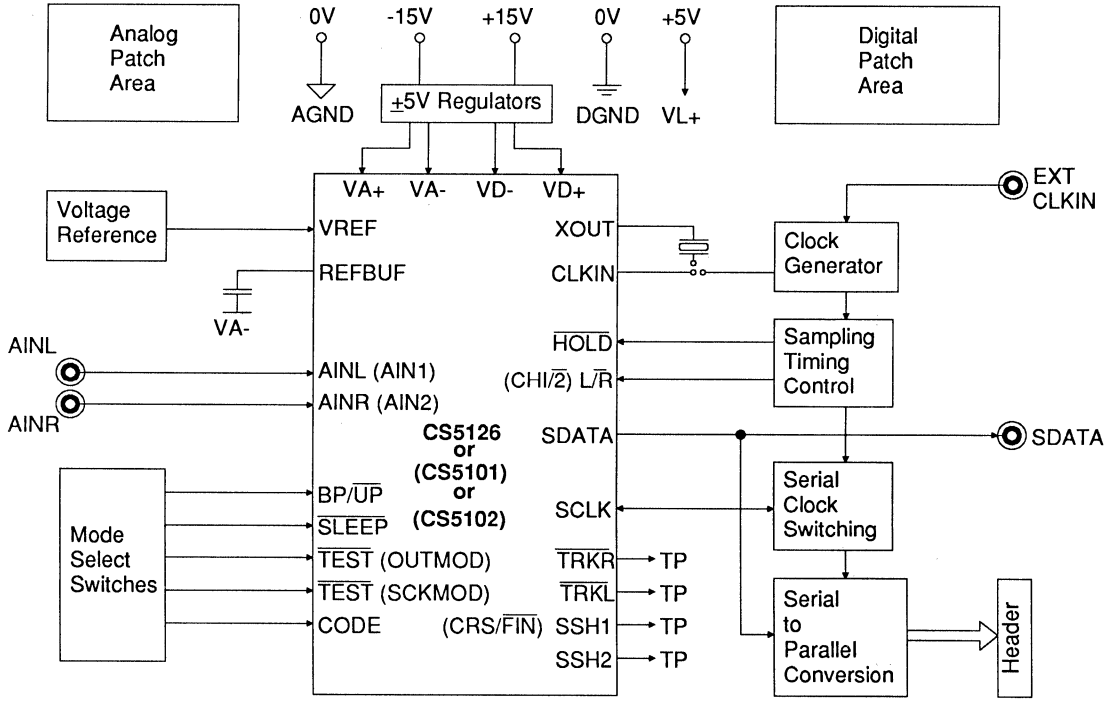
Analog inputs are via BNC connectors. Digital outputs are available both directly from the ADC in serial form, and in 16 bit parallel form.

An adjustable monolithic voltage reference is included.

Ordering Information

CDB5126
CDB5101
CDB5102

Block Diagram



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Power Supplies

Figure 1 shows the power supply arrangements. The analog section of the board is powered by ± 12/15 volts, which is regulated down to ± 5 V for the ADC. A separate +5 V digital supply is required to power the discrete logic. Be sure to switch on the ± 12/15 V at the same time as, or before, the + 5 V logic supply. This will make sure that the CLK and other logic signal are not driving the part before it is powered.

Analog Input

The analog input range is either $\pm V_{ref}$ in the bipolar mode or 0 V to $+V_{ref}$ in the unipolar mode. The voltage reference is factory set to the recommended value of +4.5 volts, so the typical input signal ranges become ± 4.5 volts or 0 V to +4.5 V.

The source driving the analog inputs should have a low (< 200 Ω at high frequency) output impedance. Be careful not to overdrive the inputs outside the power supplies of the ADC (± 5 V). Figure 2 shows the buffer circuit used at the Crystal factory to drive the ADC when performing FFT testing. See the CS5126 data sheet for example FFT test results.

Voltage Reference

As shown in Figure 3, an LT1019-5 voltage reference provides a stable 4.5 V reference for the ADC. An optional OP27 buffer filters out excess reference noise and provides a very low output impedance. To try the unbuffered LT1019-5 directly, solder in J2 and cut the VREF trace. Alternatively the shunt reference based reference schematic given in the CS5126 data sheet can be evaluated by adding it to the analog patch area.

A 5 volt reference can be used provided the supplies to the ADC are elevated to ± 5.3 volts. This can be done by inserting 22 Ω resistors in series with the regulator (U4 and U5) common leads.

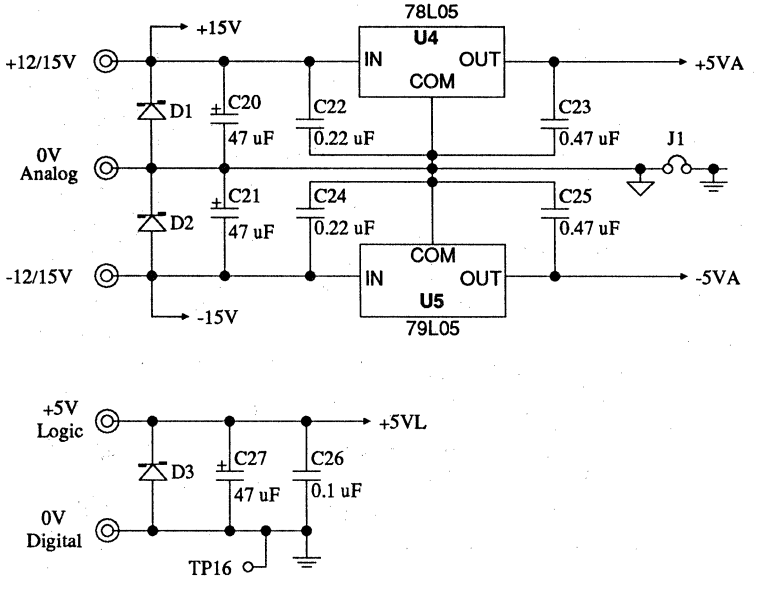


Figure 1. Power Supplies

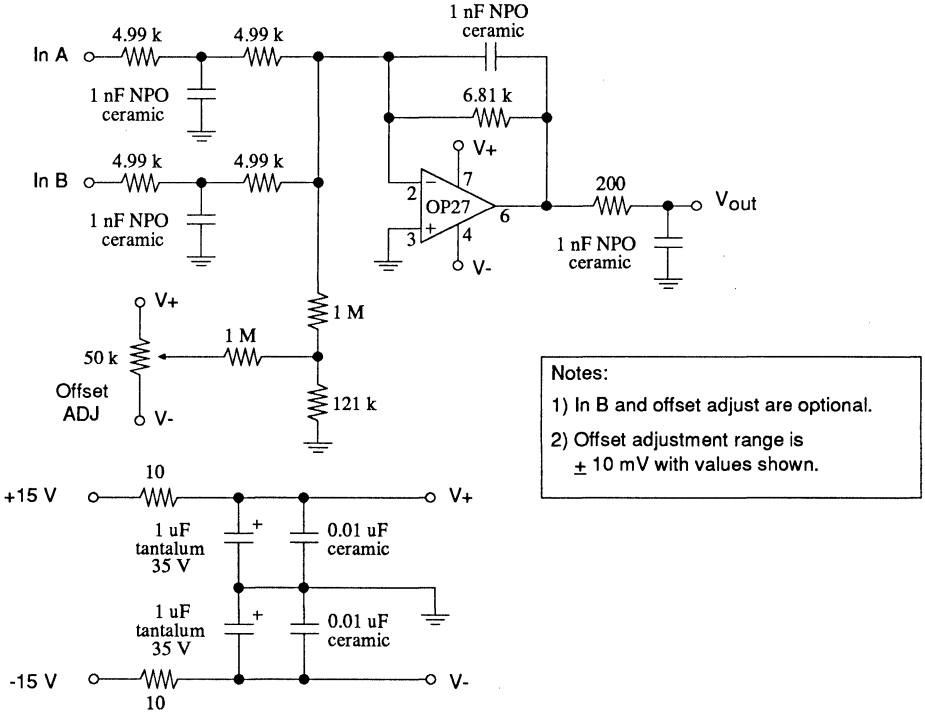


Figure 2. Example Input Buffer Circuit (not provided on the CDB5126/5101 evaluation board)

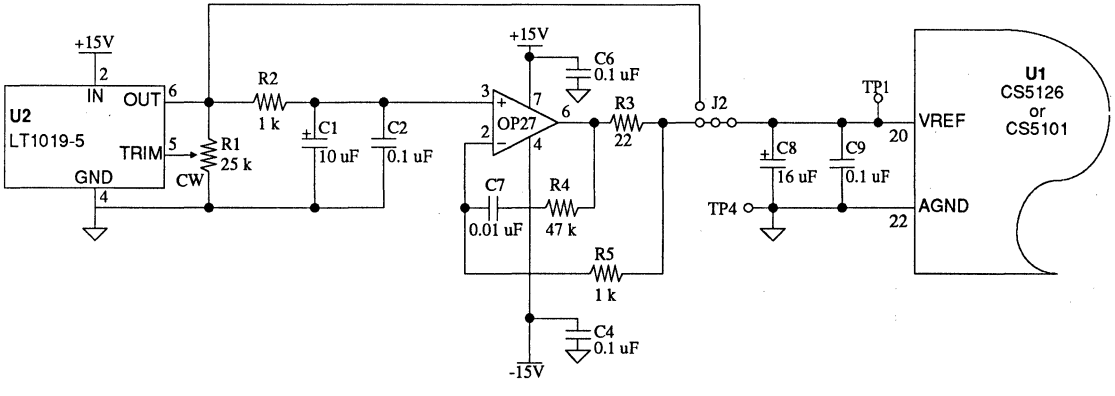


Figure 3. Voltage Reference

Master Clock

The CS5126 requires an external 24 MHz clock for a 96 kHz sample rate. A 24 MHz clock oscillator module (U6) is provided. An external clock can also be selected by P1, via a BNC connector. R15 is an optional 75 Ω terminating resistor for the external clock BNC.

The CS5101 requires an 8 MHz master clock for a 96 kHz sample rate. The CS5101 has an on-chip crystal oscillator. A CDB5101 comes assembled with an 8 MHz crystal in position XTL and a jumper installed at J3. R32, C33 and C34 are also installed on the CDB5101 as shown in Figure 4.

The CS5102 requires an 800kHz crystal or ceramic resonator for a 10kHz sample rate. The CDB5102 comes assembled with an 800 kHz ceramic resonator in position XTL. R32, C33 and C34 are installed on the CDB5102 as shown in Figure 4.

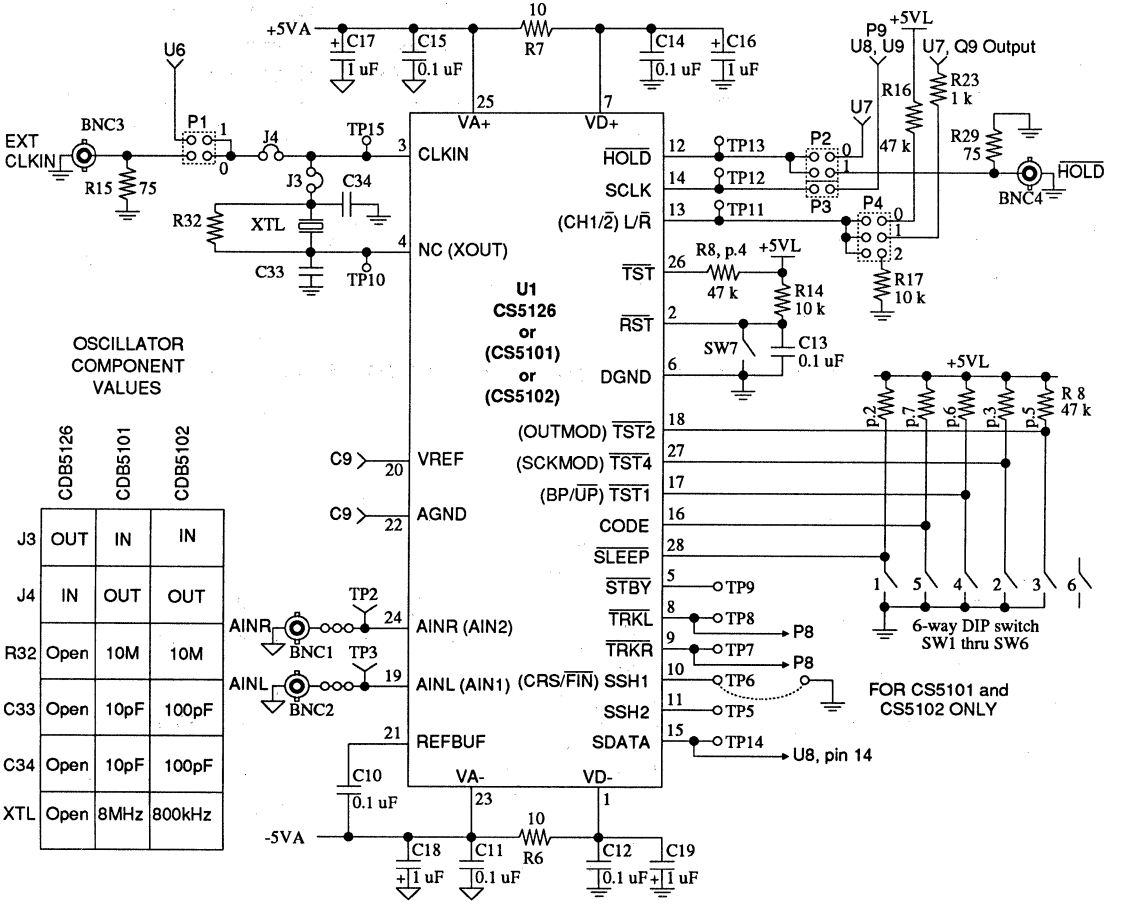


Figure 4. ADC Connections

Sampling Clock Generation Logic

The CS5126, and the CS5101 or CS5102 in PDT mode, requires an external serial clock to clock out the data. The CDB5126/5101/5102 board has the logic necessary to generate the master clock, $\overline{\text{HOLD}}$, L/$\overline{\text{R}}$, and SCLK to allow fast evaluation of the ADC. In most systems, these timing signals will be available from the main timing section, typically generated by a logic array of some variety. $\overline{\text{HOLD}}$ may be brought in externally via a BNC, optionally terminated by R29. SCLK and L/$\overline{\text{R}}$ select may be brought in externally via test points and removing jumpers.

Figure 5 shows the on-board clock generation circuitry. U7 (74HC4040) produces binary divided ratios of the 24 MHz master clock. Q4 generates a 1.5 MHz clock, which is used for SCLK. Q8 generates a 96 kHz clock, used for $\overline{\text{HOLD}}$, and Q9 generates a 48 kHz clock, optionally used to toggle L/$\overline{\text{R}}$ select. This set of clocks causes the CS5126 to continuously convert, generating a continuous stream of serial data bits. To correctly identify the last bit of each word, U12 produces a pulse only when Q4, Q5, Q6, Q7, Q8, and optionally Q9 are all high. This state is latched by U10A to prevent any glitches, and the resulting signal (attached to TP18) is used to latch the U8-U9 shift registers.

Serial to Parallel Conversion

Figure 6 shows the serial to parallel conversion circuit. Two 74HC595 shift register/latches connected in series with SDATA assemble 16-bit, parallel words, clocked by SCLK. As discussed above, the outputs are latched inside the 74HC595 at the end of each 16-bit word. The outputs are brought out to a 40-way header (P5). Only low capacitance, twisted pair, ribbon cable should be used.

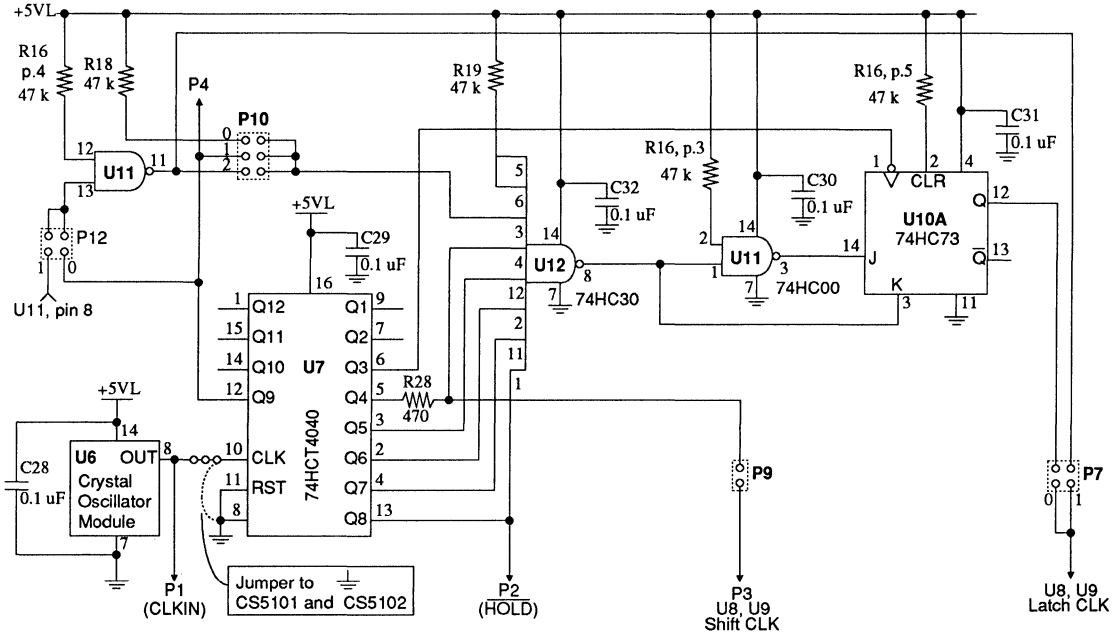


Figure 5. Timing Generator

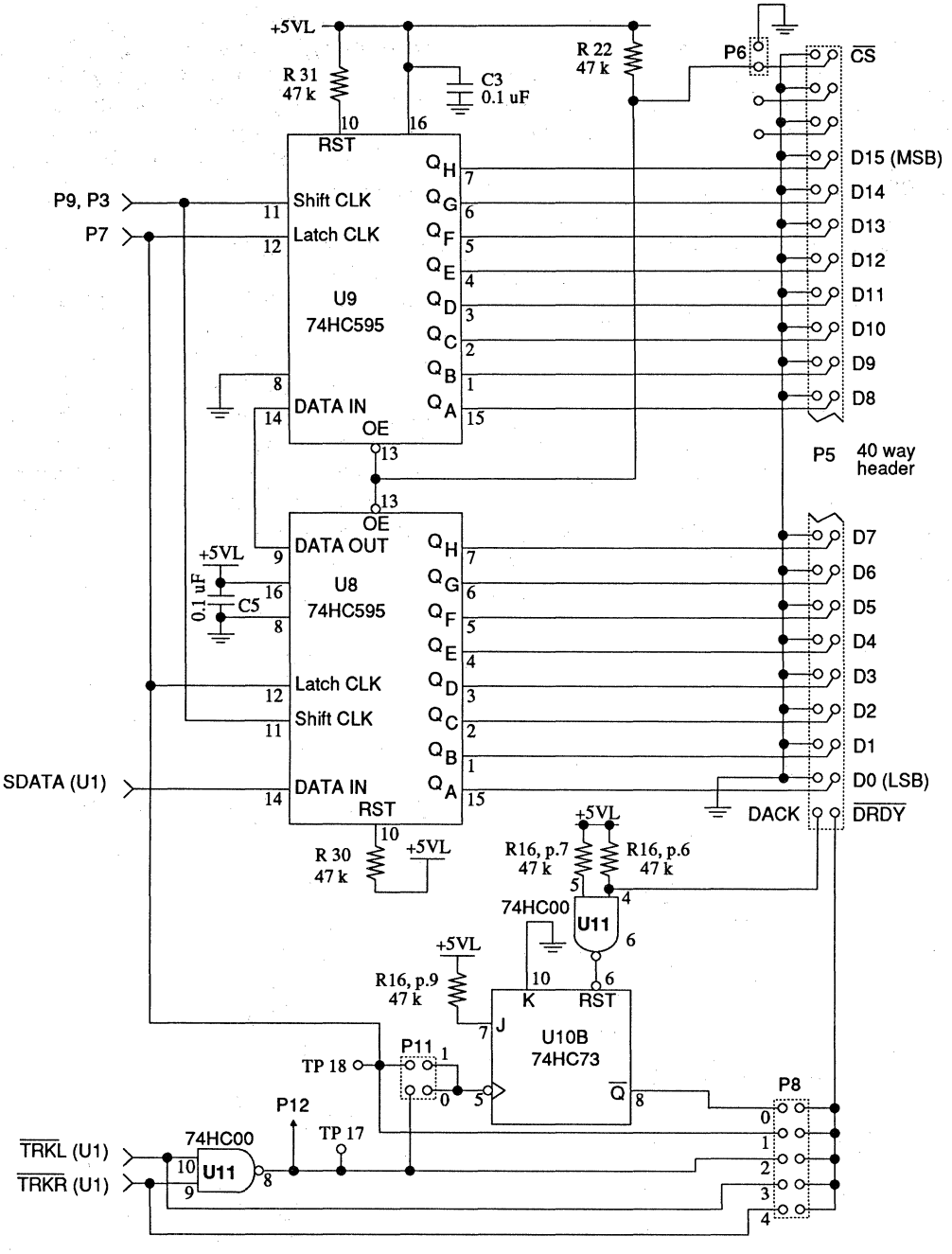


Figure 6. Serial to Parallel Converter

J1	-	Joins analog ground to digital ground on the board.
J2	-	Joins LT1019-5 reference directly to the VREF pin on the ADC. Before doing this, break the connection between R3 and the ADC VREF pin by using a twist drill to remove the central feedthrough. This option allows evaluation of different reference configurations.
J3	-	Connects the crystal to CLKIN on the ADC. Only used for CS5101.
J4	-	Connects an external clock to CLKIN on the ADC. Cut if using a crystal.

Table 1. Solder Link Options

P1	†	0 -	Select external clock via BNC connector
	*	1 -	Select on-board clock generated by U6.
P2	*	0 -	Select on-board generated $\overline{HOLD}$.
	†	1 -	Select external $\overline{HOLD}$ via BNC connector.
P3	*†		Connect SCLK to on-board shift registers.
P4	*†	0 -	Pull L/$\overline{R}$ select pin high, selecting the left channel only.
		1 -	Drive L/$\overline{R}$ select at 48 kHz from the on-board timing generator.
		2 -	Pull L/$\overline{R}$ select pin low, selecting the right channel only.
P6	*†		Connect the $\overline{OE}$ pins of the shift registers to ground. Permanently enables the 3-state output buffers.
P7	*	0 -	Connects the on-board Data Ready signal to the shift registers.
	†	1 -	Connects the NAND gate outputs (U11, pin 11) to the shift registers. Used in CS5101/CS5102 FRN mode.
P8	*†	0 -	Connects the latched on-board Data Ready signal to P5.
		1 -	Connects the un-latched on-board Data Ready signal to P5.
		2 -	Connects $\overline{TRKL}$ and $\overline{TRKR}$ *ANDED* together to P5.This signal can be used as an "End of Convert" indicator.
		3 -	Connects $\overline{TRKL}$ to P5.
		4 -	Connects $\overline{TRKR}$ to P5.
P9	*		Connects the on-board generated SCLK to the rest of the on-board circuitry. Not present in the CS5101/5102 FRN mode.
P10	*†	0 -	Causes the on-board Data Ready generating circuit to flag data ready every conversion.
		1 -	Causes the on-board Data Ready generating circuit to flag data ready every left conversion. P4 must be in position 1 for this to work.
		2 -	Causes the on-board Data Ready generating circuit to flag data ready every right conversion. P4 must be in position 1 for this to work.
P11	†	0 -	Connects $\overline{TRKL}$ & $\overline{TRKR}$ to U10B, the handshake flip-flop. Used in CS5101/CS5102 FRN mode.
	*	1 -	Connects the on-board data ready signal to U10B. Used for the CS5126.
P12	*	0 -	Allows selection of the $\overline{DRDY}$ signals for alternate channels.
	†	1 -	Connects the $\overline{TRKL}$ & $\overline{TRKR}$ to U11, pin 13. Used in the CS5101/CS5102 FRN mode.
*	*Factory default state for CS5126*		
†	*Factory default state for CS5101*/CS5102		

Table 2. Shorting Plug Selectable Options

U10B (74HC73) is used as a handshake flip-flop with the computer system attached to the evaluation board. The board brings $\overline{DRDY}$ low. The computer reads the data and then sets DACK momentarily high. This resets U10B for the next word. This handshake can be disabled by setting P8 jumper to position 1.

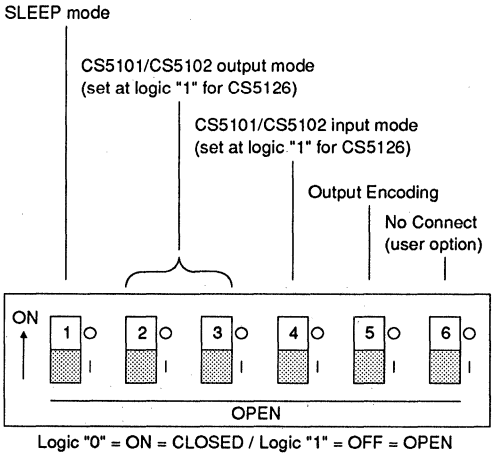


Figure 7. DIP switch configuration

Switch	Logic	Mode
1	0	SLEEP mode
	1	Normal mode
2, 3		CS5101/CS5102 output mode, set to "1" for CS5126
4	0	CS5101/CS5102 Unipolar input
	1	CS5101/CS5102 Bipolar input / CS5126 normal
5	0	Offset binary output code
	1	2's complement output code
6		Unconnected. Available for user's application

Table 3. DIP Switch Selection Options

Sw. 2	Sw. 3	CS5101/CS5102 Output Mode
1	1	(PDT) Pipelined Data Transmission
1	0	(RBT) Registered Burst Transmission
0	1	(SSC) Synchronous Self-Clocking
0	0	(FRN) Free Run

Table 4. CS5101/CS5102 Output Mode Options

DIP Switches

Figure 7 and Tables 3 and 4 show the DIP switch selectable options.

	CS5126	CS5101
TP1	VREF	VREF
TP2	AINR	AIN2
TP3	AINL	AIN1
TP4	AGND	AGND
TP5	SSH2	SSH
TP6	SSH1	CRS/$\overline{FIN}$
TP7	$\overline{TRKR}$	$\overline{TRK2}$
TP8	$\overline{TRKL}$	$\overline{TRK1}$
TP9	$\overline{STBY}$	$\overline{STBY}$
TP10	NC	XOUT
TP11	L/$\overline{R}$	CHI/$\overline{2}$
TP12	SCLK	SCLK
TP13	$\overline{HOLD}$	$\overline{HOLD}$
TP14	SDATA	SDATA
TP15	CLKIN	CLKIN
TP16	DGND	DGND
TP17	$\overline{TRKL}$ + $\overline{TRKR}$	
TP18	Latch Clock for the 74HC595 shift registers	

Table 5. CDB5126/5101/5102 Test Points

Test Points

Above is a list of the test points provided on the CDB5126/5101/5102 Evaluation Board.

Miscellaneous Hints on Using the Evaluation Board

Always hit the reset button after powering-up the board. The CS5126, CS5101 and CS5102 are self calibrating and require the reset signal to initiate the calibration procedure.

P4 controls the ADC input mux. This is used to set the mux to be continuously connected to one channel, or to be toggling between two channels. This is very useful for evaluating oversampled vs. regular sampling digital audio.

P10 controls the Data Ready pulses from the on-board logic. To cause every data sample to be read, select option 0. If you wish to read only every alternate sample, then select option 1 or 2, depending on whether you wish to read every left (1) channel value, or every right (2) channel value. This is useful for evaluating the part with a test system which does not separate alternate values.

CS5101/CS5102 Evaluation

The CS5101/CS5102 CRS/$\overline{\text{FIN}}$ pin (pin 10) must be pulled low for normal operation. The CDB5101 and the CDB5102 will be shipped with two wire jumpers added to the board. The first jumper is between U1 pin 10 (TP6) and DGND. If a CS5101/CS5102 is substituted for a CS5126 in a CDB5126 board, then add the TP6 to DGND jumper. If this is not done, the CS5101/CS5102 will not operate correctly. The second jumper, U7, pin 10, to DGND shorts the CMOS 74HCT4040 counter input to ground when the U6 oscillator module is not used.

The CS5101 and the CS5102 are most easily evaluated using the FRN mode (not present in CS5126). This is done by setting DIP switches 2 and 3 to "0" (ON). Since SCLK becomes output, P9 jumper needs to be removed to avoid contention. R28 (470 Ω) limits the current should P9 be left in by mistake. Similarly, the L/$\overline{\text{R}}$ select pin becomes an output, and P4 needs to be set to position 0. R23 (1 kΩ) limits the current should the jumper be left in position 1.

To use the 74HC595 shift registers to assemble parallel data in CS5101/CS5102 FRN mode, the P11 jumper needs to be moved to position 0. This connects the $\overline{\text{TRKL}}$ + $\overline{\text{TRKR}}$ signal to the Data Ready flip-flop. Also P12 jumper needs to be set to position 1. This generates the inverse of the $\overline{\text{TRKL}}$ + $\overline{\text{TRKR}}$ signal using U11. This inverse signal is then used to latch the shift registers by connecting P7 jumper to position 1. As an alternative to using the Data Ready handshake flip-flop, P8 jumper header allows the shift register latch clock, or the $\overline{\text{TRKL}}$ + $\overline{\text{TRKR}}$ signal, or $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ to be used to qualify the parallel data.

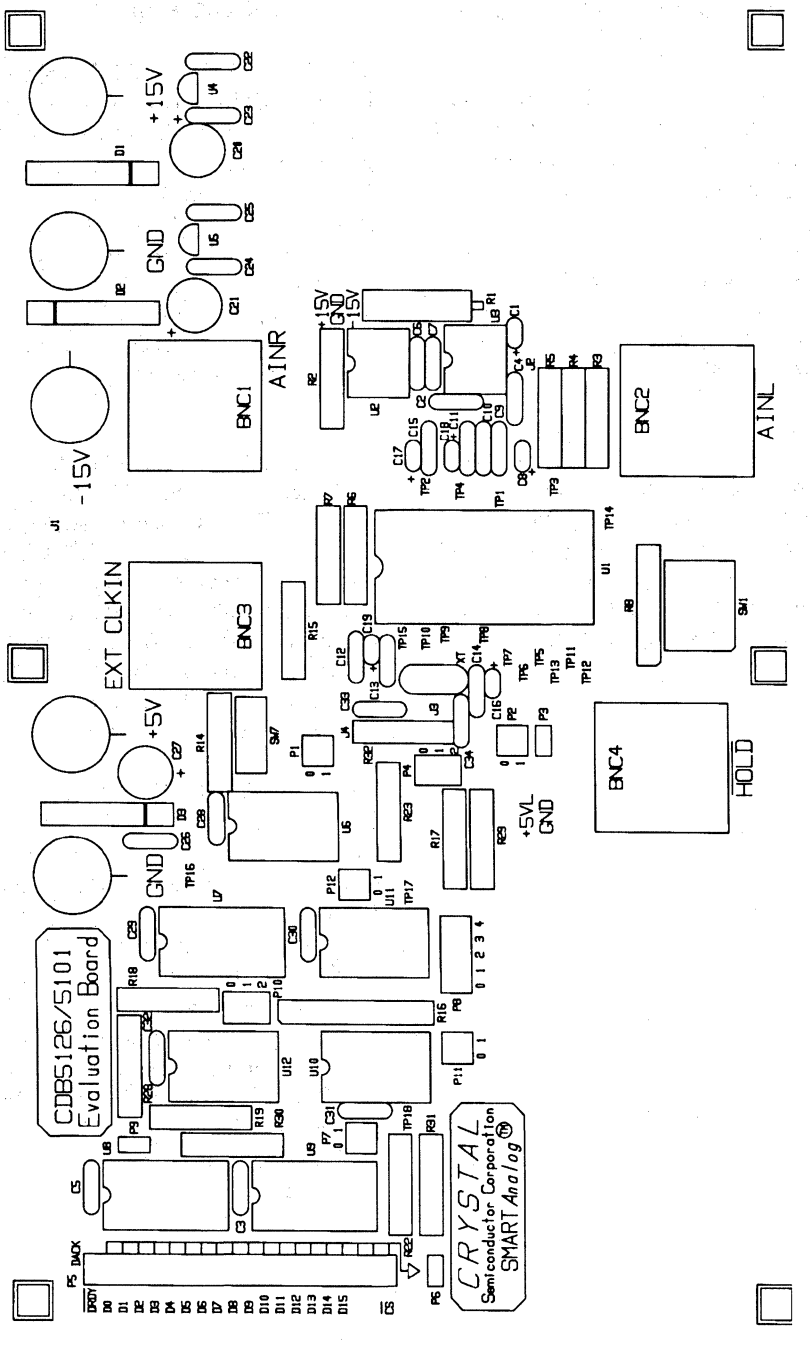


Figure 8. CDB5126/5101/5102 Component Layout

CDB5317 Evaluation Board

Features

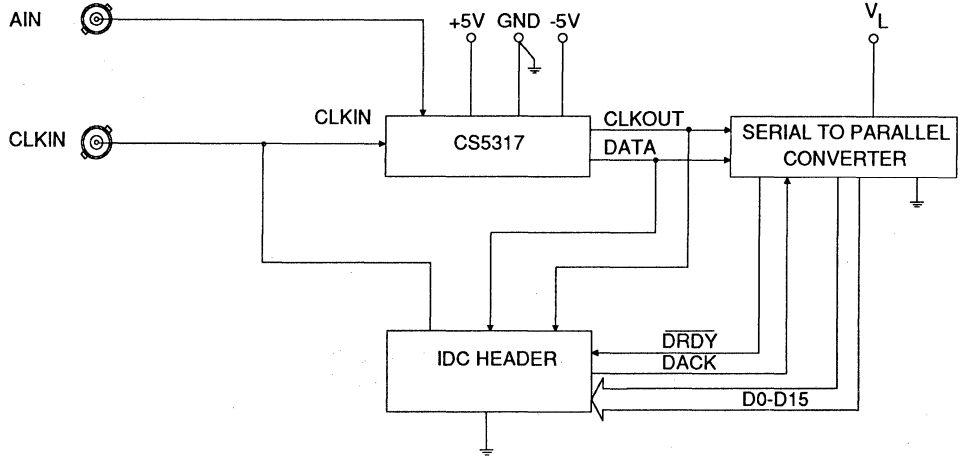
- Easy to Use Digital Interface
  Parallel 16 Bits With Clock
  Serial Output With Clock
- Multiple Operating Modes
  Including Two PLL Modes
- IDC Header used to access Parallel Data, Serial Data, and Clock Input and Output

General Description

The CDB5317 Evaluation Board is designed to allow the user to quickly evaluate performance of the CS5317 Delta-Sigma Analog-to-Digital Converter. All that is required to use this board is an external power supply, a signal source, a clock source, and an ability to read either serial or parallel 16 bit data words.

Ordering Information: CDB5317

Block Diagram



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GENERAL DESCRIPTION

The CDB5317 Evaluation Board is a stand-alone environment for easy lab evaluation of the CS5317 Delta-Sigma Analog-to-Digital Converter. Included on the board is a serial-to-parallel converter. The user can access output data in either parallel or serial form. When supplied with the necessary +5 V and -5 V power supplies, a CLKIN signal, and an analog signal source, the CDB5317 will provide converted data at the 40 pin header.

SUGGESTED EVALUATION METHOD

An efficient evaluation of the CS5317 using the CDB5317 may be accomplished as described below.

The following equipment will be required for the evaluation:

- The CDB5317 Evaluation Board.
- A power supply capable of supplying +5V and -5V.
- A clock source as the CLKIN signal of the CS5317.
- A spectrally pure sine wave generator such as the Krohn-Hite Model 4400A "Ultra-Low Distortion Oscillator".
- A PC equipped with a digital data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface".
- A software routine to collect the data and perform a Fast Fourier Transform (FFT).

The evaluation board includes filter components for the on-chip phase locked loop. The components are adequate for testing if the CLKIN signal has little or no phase-jitter. If the CDB5317 board is being tested as part of a system which generates a CLKIN which contains jitter, the PLL filter components may need to be optimized for your system (see the CS5317 data sheet).

Set-up for evaluation is straightforward. First decide the operating mode and place the jumper on the board for the proper selection. Then decide whether the filter components for the phase locked loop are adequate or whether they should be changed for your evaluation. The PLL will lock on a steady clock input with the filter as it is. Connect the necessary 5 V (CMOS compatible) CLKIN signal for the application. Use the sine-wave generator to supply the analog signal to the CDB5317. Apply the analog input and CLKIN signals only when the evaluation board is powered up. Converted data will then appear at the header on the CDB5317. The header should be connected to the digital data acquisition board in the PC through an IDC 40 pin connector and cable. The software routine should collect the data from the CDB5317 and run a standard 1024 point Fast Fourier Transform (FFT). Such an analysis results in a plot similar to Figure 1. This plot resulted from using a 1kHz input signal and a Blackman-Harris window for the FFT.

The signal to noise and signal to total harmonic distortion characteristics of the CS5317 may be easily measured in this way. The signal to total harmonic distortion value for a particular input is the ratio of the RMS value of the input signal and the sum of the RMS values of the harmonics shown in the diagram. The dynamic range of the CS5317 can be measured by reducing the input

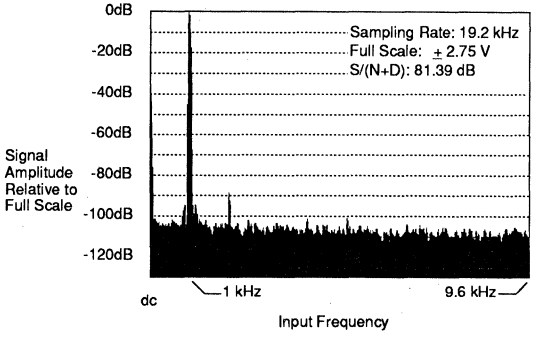


Figure 1. FFT Plot Example

amplitude so that distortion products become negligible. This allows an accurate measurement of the noise floor.

More complex analysis such as intermodulation distortion measurements can be accomplished with the addition of another sine-wave generator.

CIRCUIT DESCRIPTION

Figure 2 illustrates the CS5317 A/D converter IC circuit connections. The chip operates off of ±5V. These voltages are supplied from a power source external to the evaluation board. Binding posts are supplied on the board to connect the +5, -5, and ground power lines. A good quality low ripple, low noise supply will give the best performance. The +5 V supply can also be used for VL and should be connected between the VL board jack and the power supply, as opposed to connecting the VL jack straight to the +5V jack. The +5V jack is the positive power source for the CS5317 IC whereas the VL jack supplies power to all the digital ICs. Care should be taken that noise is not coupled between VL and +5V; however, supply noise is generally not a problem with the CS5317 since the on-chip decimation filter will remove any interference outside of its passband. The +5 and -5 V supply lines are fil-

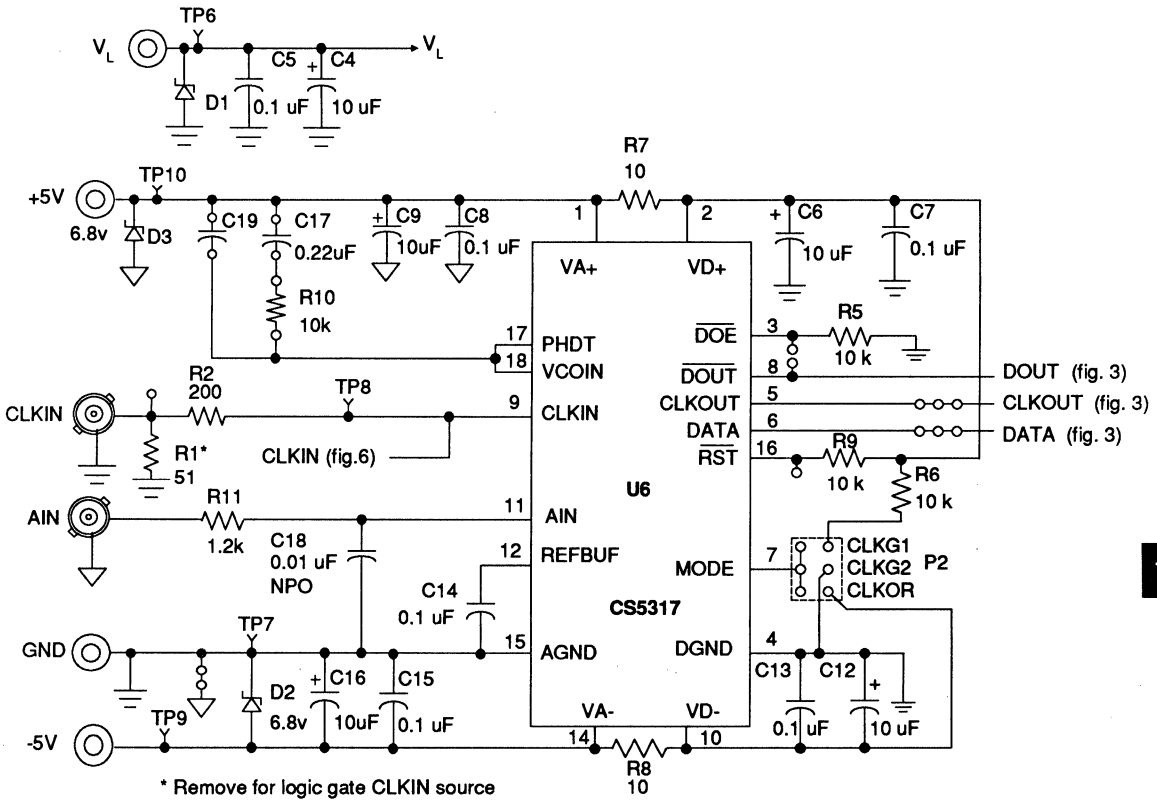


Figure 2. Analog-to-Digital Converter

tered on the board and then connected to the V_{A+} and V_{A-} supply pins of the chip. The +5 V and -5V are then connected by means of ten Ω resistors to the V_{D+} and V_{D-} pins respectively. Capacitive filtering is provided on all supply pins of the chip. In addition there is a 0.1 µF filter capacitor connected from the REFBUF pin of the chip to the V_{A-} supply pin.

To properly operate, the CS5317 chip requires an external (5 V CMOS compatible) clock. A BNC connector labelled CLKIN is provided to connect the off-board clock signal to the board. The CLKIN signal is also available on the 40 pin header connector. The CLKIN signal is one input to the phase detector of the on-chip phase locked loop of the CS5317.

Header connector P2 (see Figure 2) is provided to allow mode selection for the CS5317 chip. The mode selection works together with the CLKIN signal to set the sample rate and the output word rate of the CS5317. See the CS5317 data sheet for details on mode selection. Two of the available modes (CLKG1 and CLKG2) utilize the on-chip phase locked loop to step up the CLKIN frequency to obtain the necessary sample rate clock for the A/D converter. Another mode (the CLKOR mode) does not use the on-chip PLL but instead drives the sample function directly. The

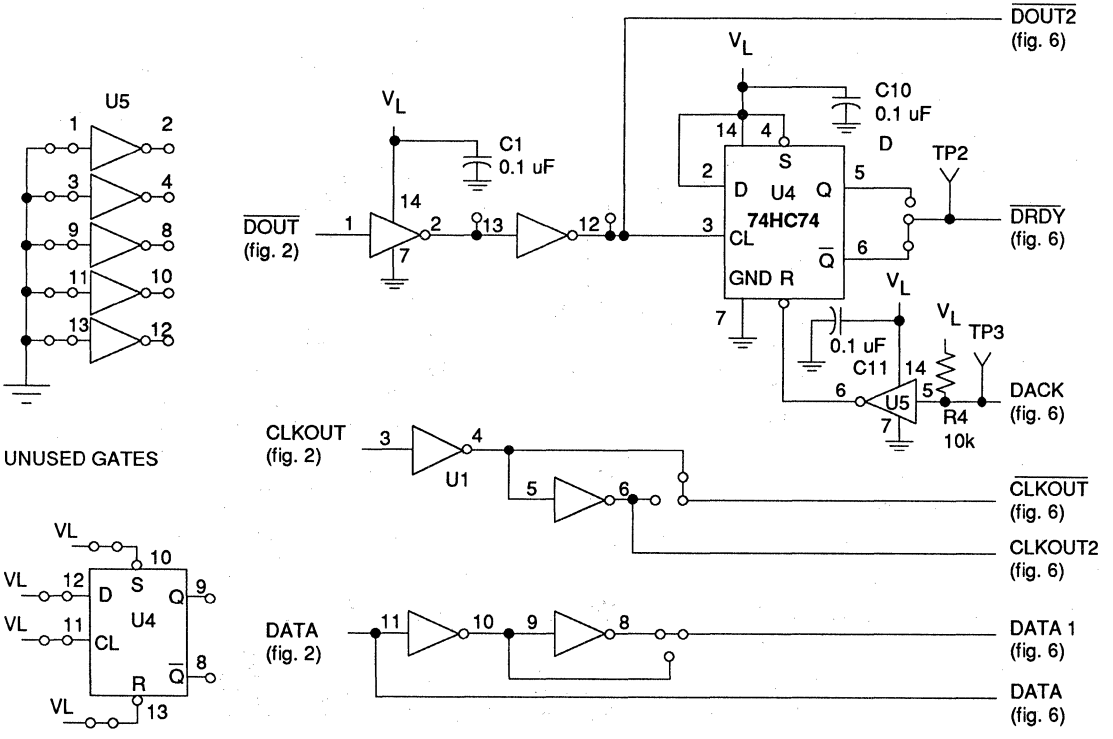
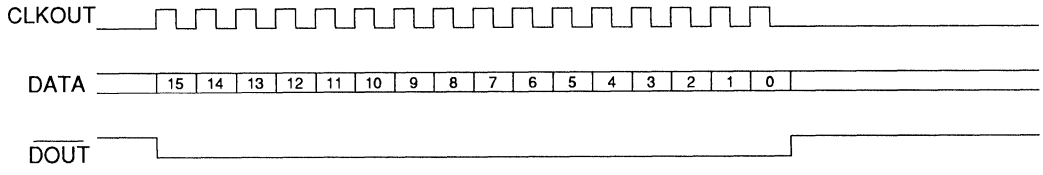


Figure 3. Buffers and Parallel Handshake Flip-Flop



Note: For a complete description of serial timing see the CS5317 Data Sheet

Figure 4 Serial Data Timing

two modes which use the phase locked loop will require appropriate low pass filter components on the Evaluation Board. The low pass filter components help determine the PLL control loop response, including its bandwidth and stability and therefore directly affect the transient response of the PLL control loop. Appropriate filter components should be installed if a particular dynamic response to changes of the CLKIN signal is desired.

The filter components which are installed on the board have been chosen for the following parameters: MODE: CLKG2; CLKIN: 7,200; N=512; damping factor: 1.0; Control loop -3 dB bandwidth: 2262 radians/second. These parameters yield R as 10 k Ω and C as 0.22 μF for the filter components.

The analog signal to be digitized is input to the AIN BNC connector. The digital output words from the CS5317 are buffered by HEX inverters as shown in Figure 3. The buffered versions of the CLKOUT and DATA signals are available on the header connector P1 in Figure 6. The serial data signals out of the CS5317 are illustrated in Figure 4. If remote control of the $\overline{\text{DOE}}$ line is desired, the trace on the PC Board can be opened and a wire connection can be soldered to the $\overline{\text{DOE}}$ input line. Remote control of the $\overline{\text{RST}}$ line of the CS5317 is also available if desired.

Figures 5 and 6 illustrate the serial to parallel shift registers including timing information. The DATA output signal from the CS5317 is input to the data input of the shift register. An inverted version of the CLKOUT signal is used to clock the DATA into the shift registers. The two 8-bit shift register ICs also include output latches. The

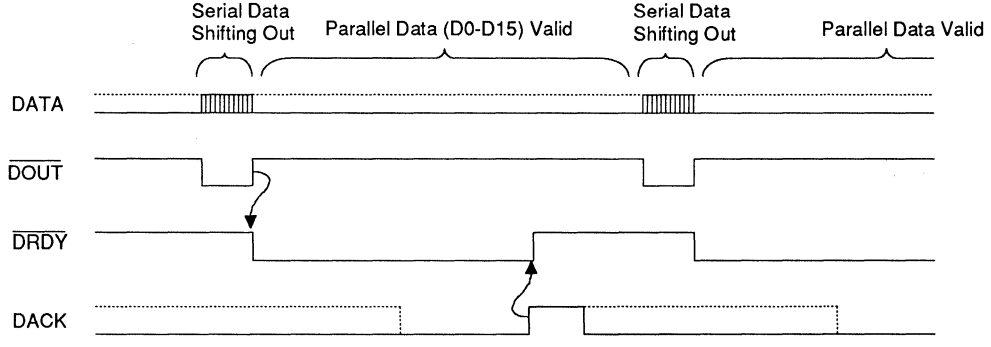


Figure 5. Parallel Data Timing

rising edge of the $\overline{DOUT}$ signal from the CS5317 is used to latch the data once it is input to the shift registers. The rising edge of $\overline{DOUT}$ is also used to toggle the $\overline{DRDY}$ flip flop (see Figure 3). The flip flop is used to signal a remote device whenever new data is latched into the output registers. The $\overline{DRDY}$ flip flop is reset whenever DACK occurs.

A component layout of the CDB5317 board is illustrated in Figure 7.

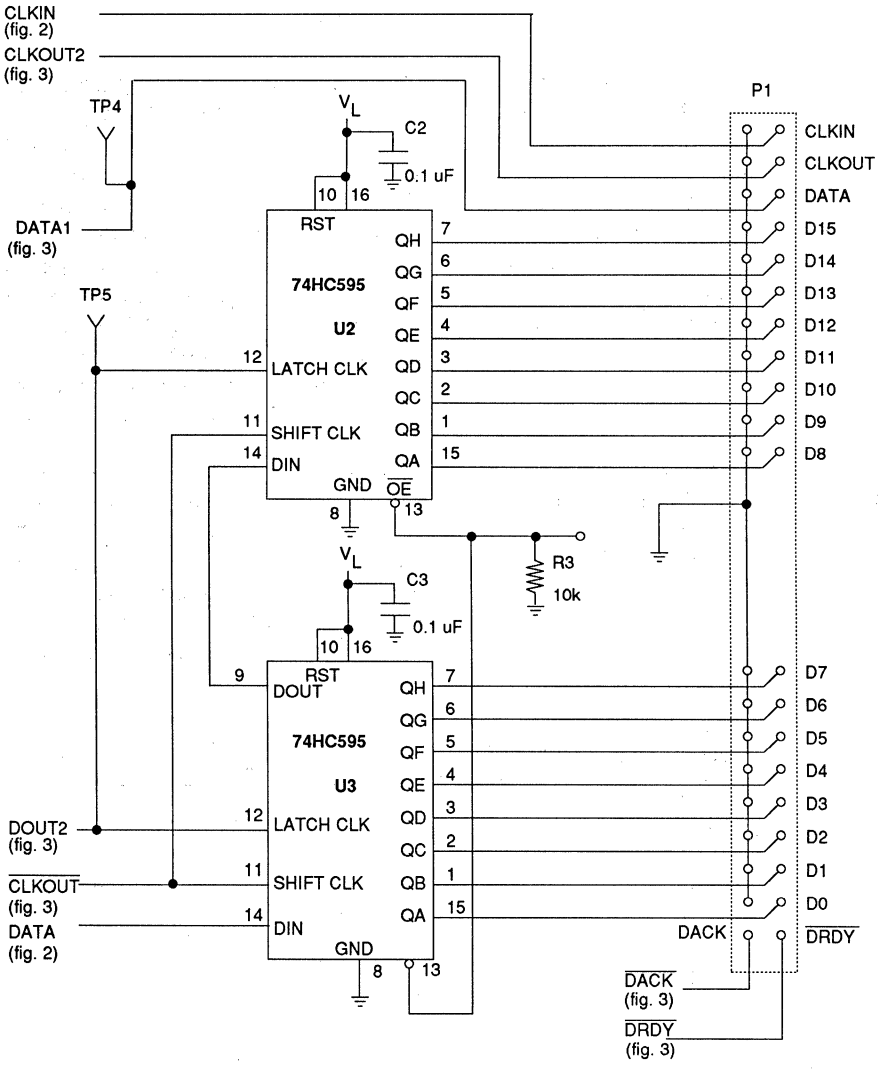


Figure 6.

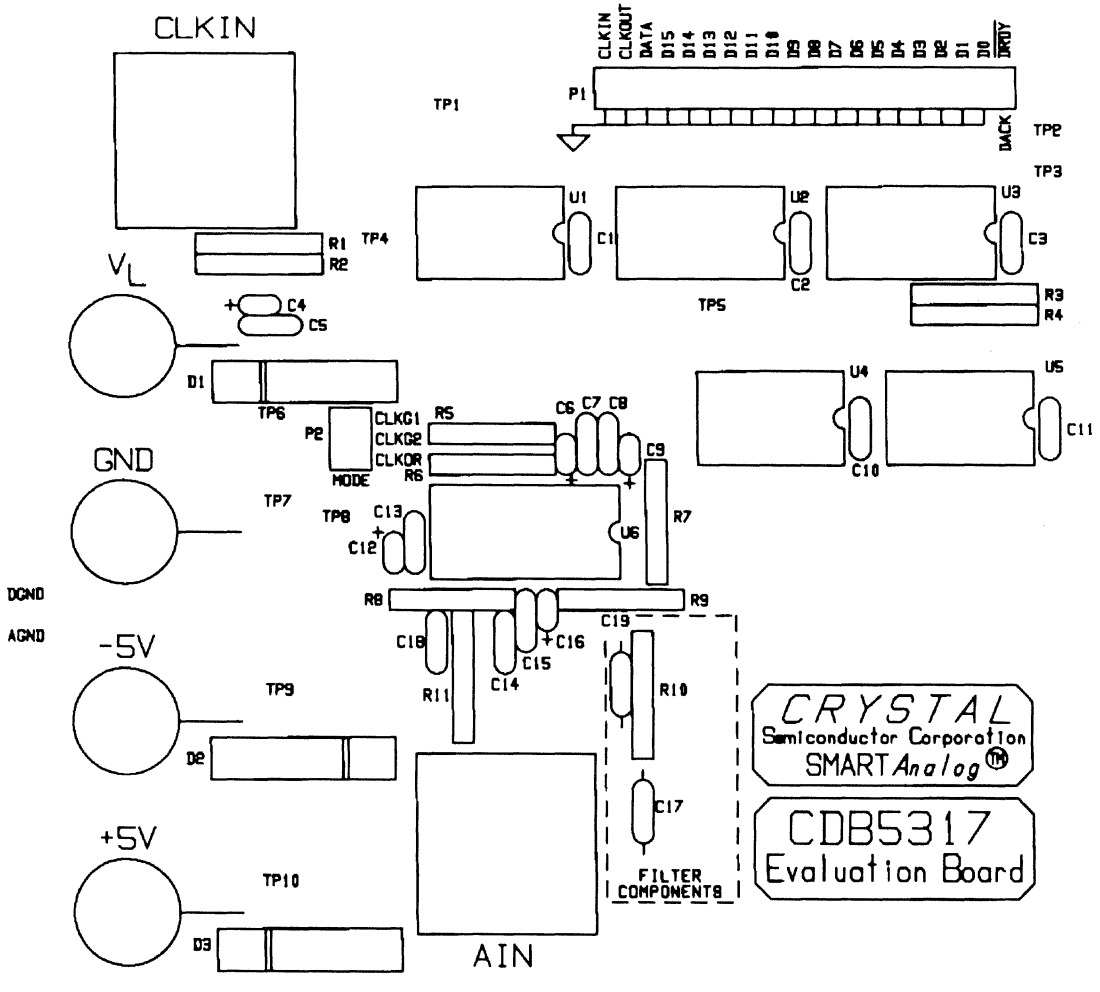


Figure 7. Bird's Eye View

•Notes•

Semiconductor Corporation

CDB5324

Evaluation Board for CS5324

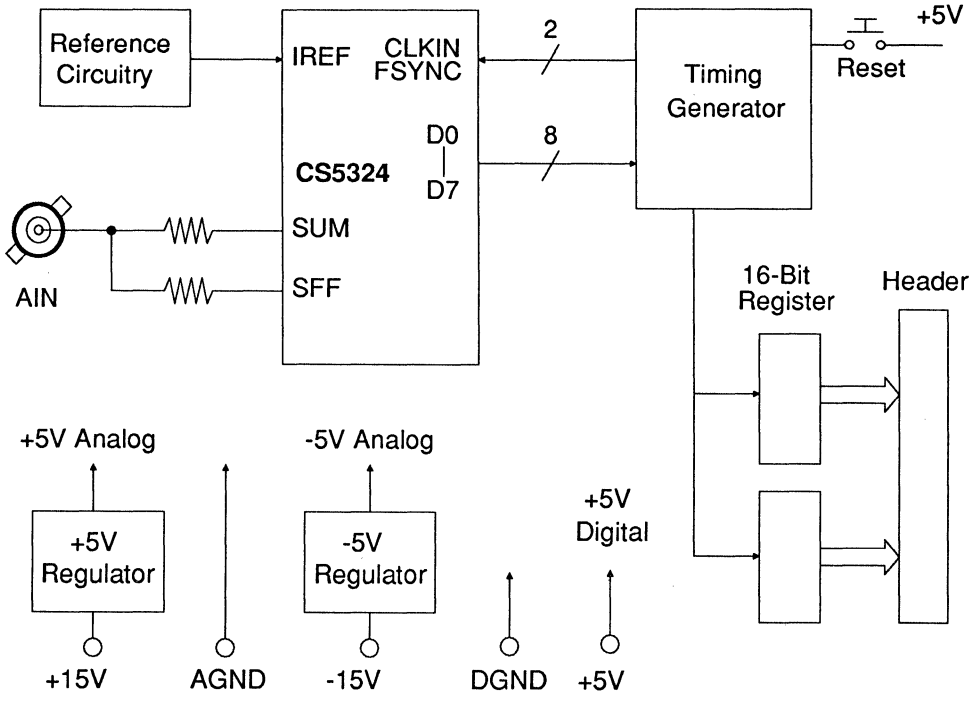
Features

- PC/µP-compatible Header Connection
  - 16 Bit Parallel Data
  - Three-State Output
  - Data Ready Signal
- Analog/Digital Patch Areas
- Analog BNC Input Connector

General Description

The CDB5324 is an evaluation board that allows the laboratory characterization of the CS5324 A/D converter. The CS5324 is a 120dB dynamic range, 500Hz bandwidth ADC intended for seismic applications. The board supports ±10 volt analog input signals and generates the timing signals which format the output data from the CS5324 into a single 16-bit parallel word.

Ordering Information: CDB5324



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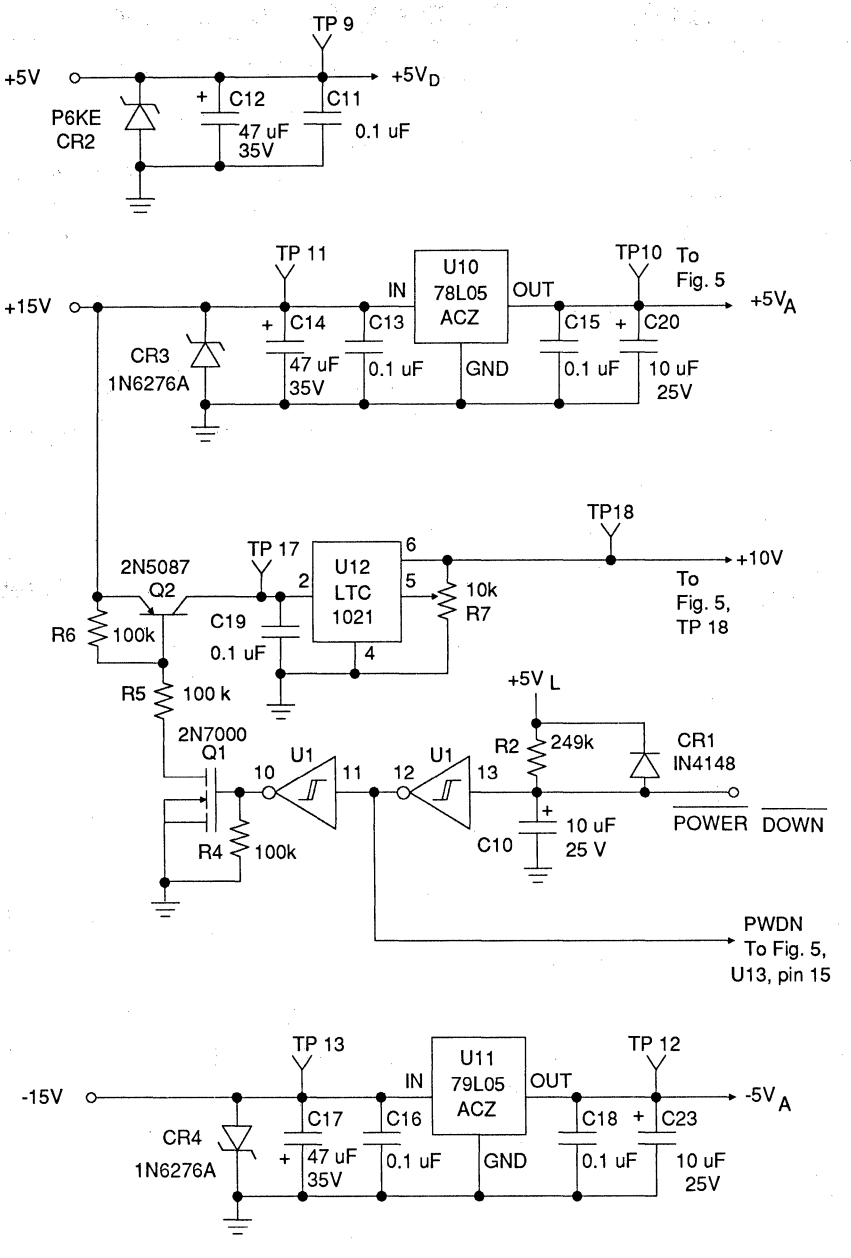


Figure 1. Voltage Regulators and +10V Reference

Power Supplies and Voltage Reference

The CDB5324 evaluation board requires three separate input voltages for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The +5V input supplies power to the digital logic portion of the board. The +15V and -15V inputs are regulated down to provide the +5V and -5V supplies necessary for the CS5324. Also included in Figure 1 is a start-up circuit which allows a power-down signal to turn off both the CS5324 and the supply current to the LTC1021 voltage reference. An RC delay is added as part of the start-up circuitry to insure the the +5V digital supply is present before the LTC1021 voltage reference is turned on. The FSYNC and CLKIN signals to the CS5324 must

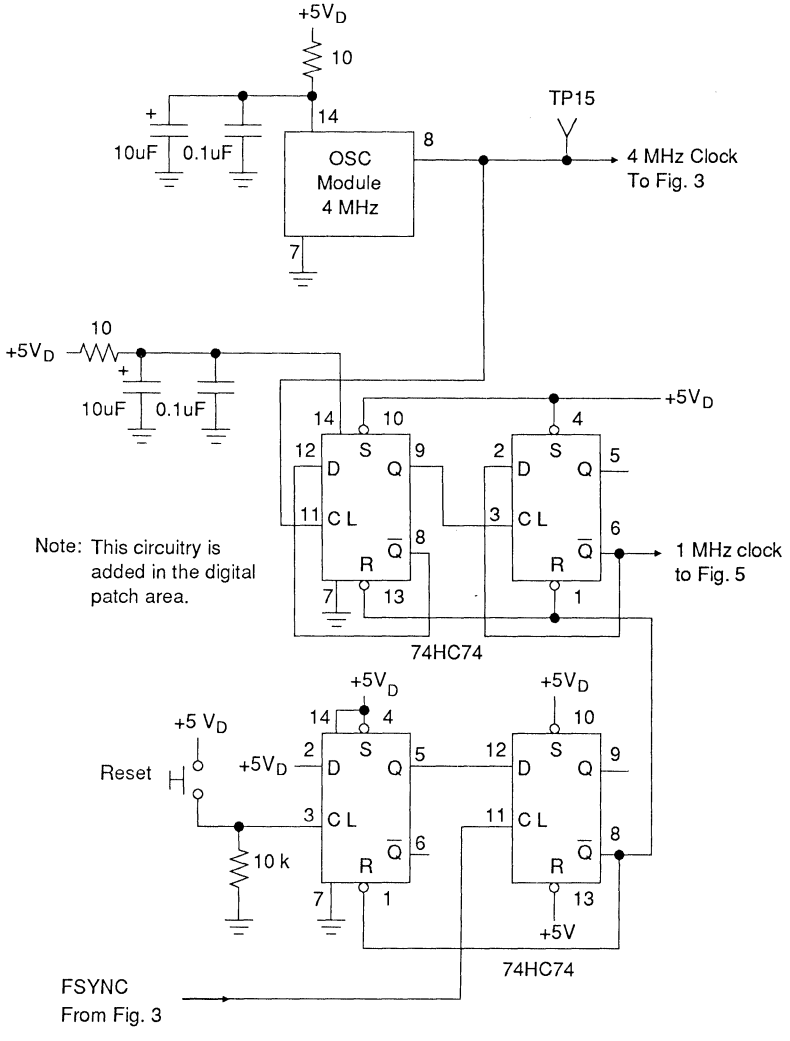


Figure 2. Clock Oscillator/Divider

be furnished by the digital logic whenever the voltage reference is turned on to insure proper start-up of the device. This start-up circuitry is provided on the evaluation board to insure proper start-up of the CS5324 while using separate laboratory supplies which may then be turned on in any sequence. This circuitry is not required if all of the supplies are activated at the same time.

Clock Oscillator/Divider

Figure 2 illustrates the oscillator and clock divider circuitry used to generate the 1 MHz clock for the CS5324 A/D converter. This circuitry is in the digital patch area of the circuit card. The 1 MHz clock to the CS5324 must have low jitter. Jitter on the clock of any high resolu-

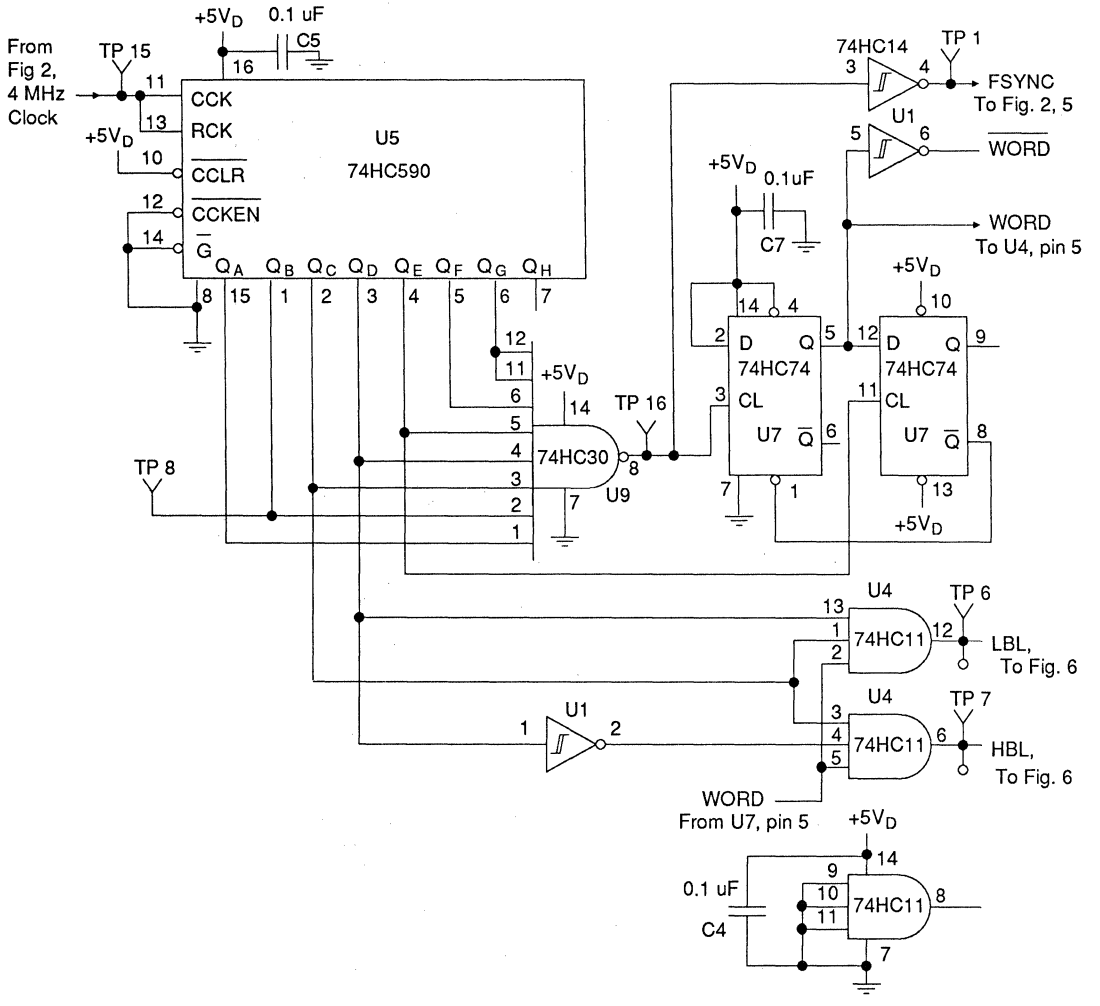


Figure 3. Timing Generator

tion A/D converter will reduce the signal-to-noise capability of the device.

Note that both the oscillator and the dual D flip-flop used to divide the oscillator output are individually decoupled from the +5V logic supply. The second dual D flip-flop pair are used to synchronize the 1 MHz from the dual D divider to be in phase with the 1 MHz out of the 74HC590 counter. This synchronization is necessary to insure that the other timing signals derived from the 74HC590 outputs have the proper phase relationship to the 1 MHz clock in the CS5324.

Reset

To insure synchronization of the 1 MHz clock to the CS5324 with the other clock signals in the system, the reset button in the digital patch area of the board must be activated after power is applied to the system.

Timing Generator

Figure 3 illustrates the logic circuitry which generates the timing signals used to latch the data coming out of the CS5324 A/D converter. The outputs from the 74HC590 counter are used to generate FSYNC, HBL (High Byte Latch), LBL (Low Byte Latch), and WORD. Figure 4 illustrates the timing relationships of these signals.

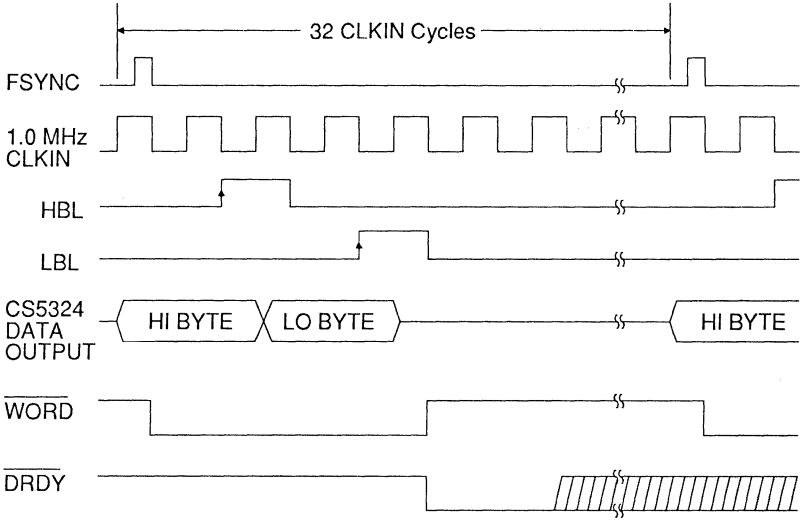


Figure 4. Timing Diagram

CS5324 A/D Converter

The connections to the CS5324 chip are illustrated in Figure 5. The analog and digital supply voltages are all decoupled close to the device. Included in the schematic are the discrete components used to develop the reference current and signal current inputs to the device. The AIN BNC is the signal input to the evaluation board. The input range is set for 20 volts p-p. Data from the CS5324 is output as two 8-bit bytes. These two bytes are latched into the output registers of Figure 6.

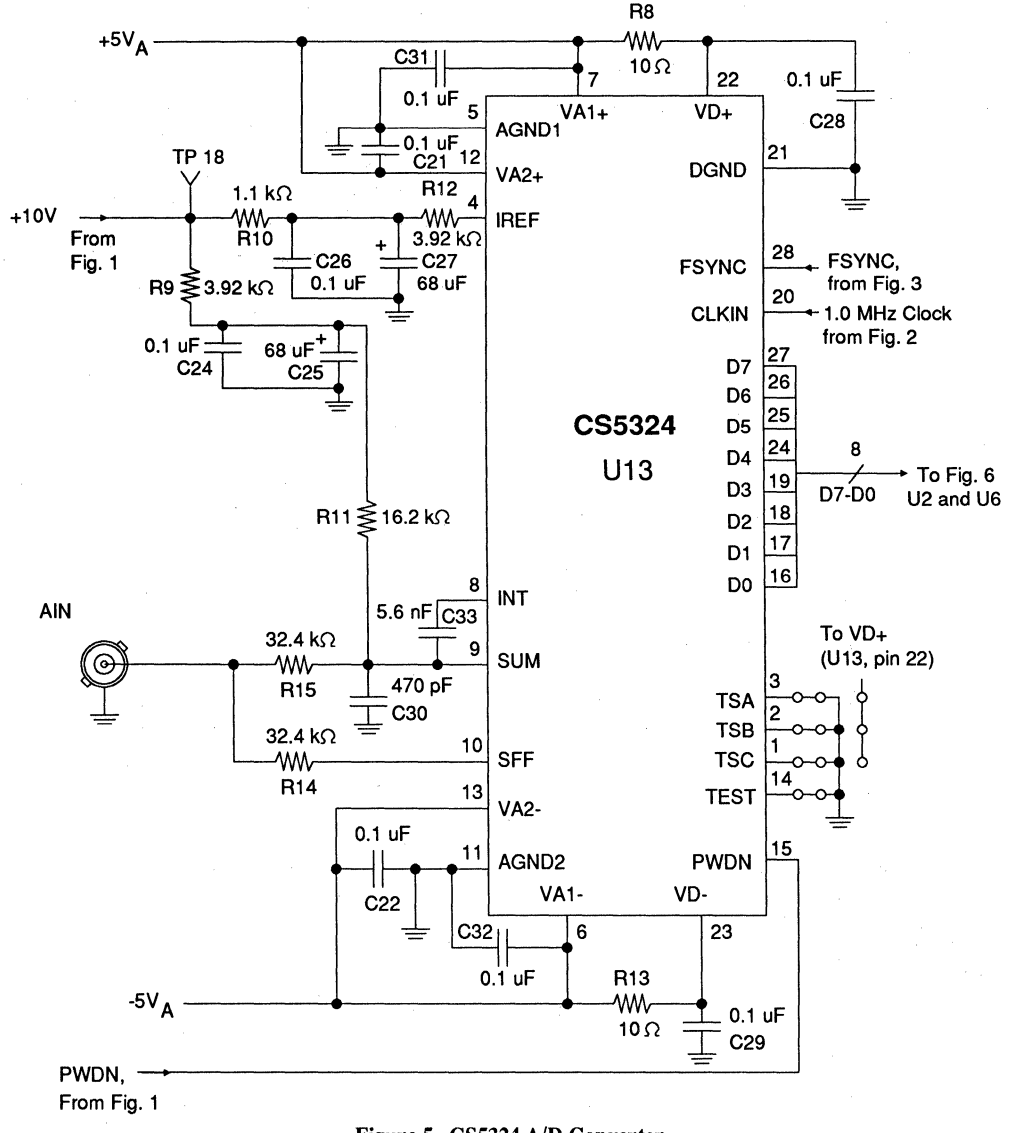


Figure 5. CS5324 A/D Converter

Output Registers/Header Connector

Data from the CS5324 A/D converter is latched into the two 74HC574 octal flip-flops by the HBL and LBL latch signals generated by the timing generator. The outputs of the 74HC574's are then connected to the 40-pin header Connector. Figure 7 identifies the pins on the 40-pin header. Note that each of the data output pins is adjacent to a ground pin on the header. In constructing a cable for interfacing to the evaluation board, twisted-pair ribbon cable (Beldon Vari-Twist 9V28040 or equivalent) should be used. Each twisted pair should include a ground line with the data signal as this minimizes radiated noise.

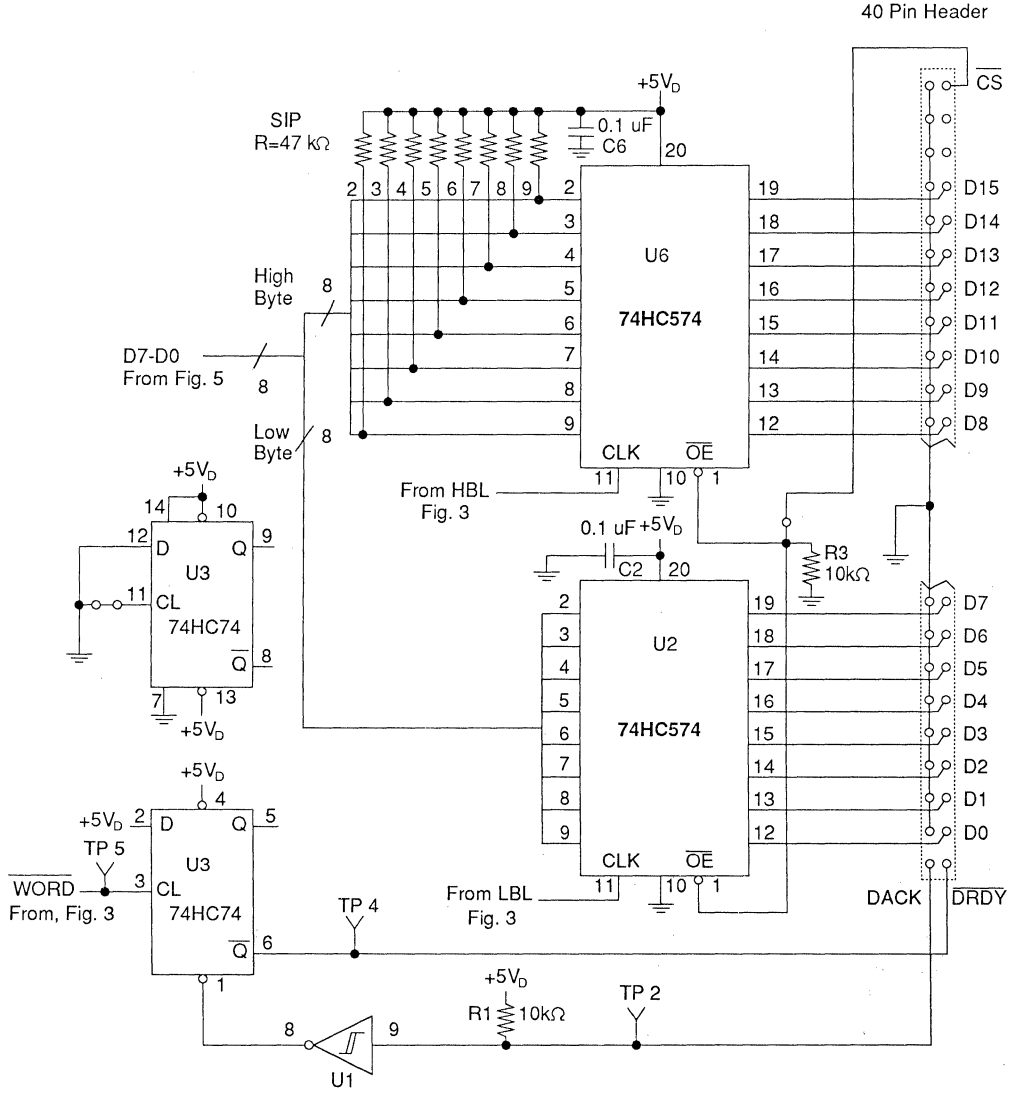


Figure 6. Output Registers/Header Connector

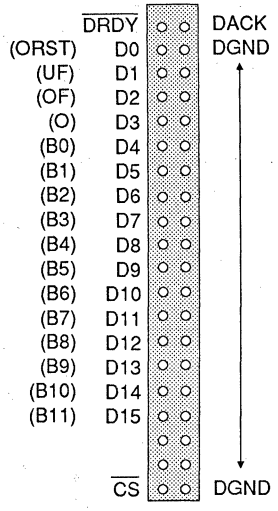


Figure 7. Header Pin Identification

Using the Evaluation Board

Connect the appropriate power supply voltages to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency (50/60 Hz) interference.

Connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter will exceed the capability of most signal generators, especially with respect to noise and line frequency interference.

Power-up the evaluation board and activate the reset button (located in the digital patch area). The ribbon cable to the 40-pin header should remain disconnected until after power is applied to the board. This is a requirement only if power can be sourced from the data collection equipment to the evaluation board. (In the event that current is sourced through the ribbon cable into the evaluation board, and then power is applied, the evaluation board circuitry may not start-up properly).

Data from the evaluation board must be processed using digital filter functions, such as those found in the Appendix of the CS5324 data sheet to achieve the full 120 dB dynamic range of the A/D.

Evaluation Board Performance

To evaluate the performance of the evaluation board will require a quality signal source. A Khron-Hite 4400A low distortion oscillator can be used if an additional narrowband filter is used to filter out the line frequency interference and broadband noise which is part of the oscillator signal. Note that when using the Khron-Hite oscillator with a 60 Hz line frequency, interference components at 60, 120, 180 and 240 Hz show up as well as the oscillator fundamental. These interference components are generally 105 to 115 dB below full scale and will therefore show up in an FFT plot of the A/D's performance.

With a pure signal source provided to the AIN BNC input, output words are collected and filtered. The resulting data is then windowed and submitted to the FFT algorithm. The results can then be plotted. Performance plots for the CS5324 can be found in the CS5324 data sheet.

Component Layout

Figure 8 illustrates the component layout of the CDB5324 evaluation board. Note that this layout does not include the components added in the digital patch area. The components in the digital patch area are indicated in schematic diagram of Figure 2.

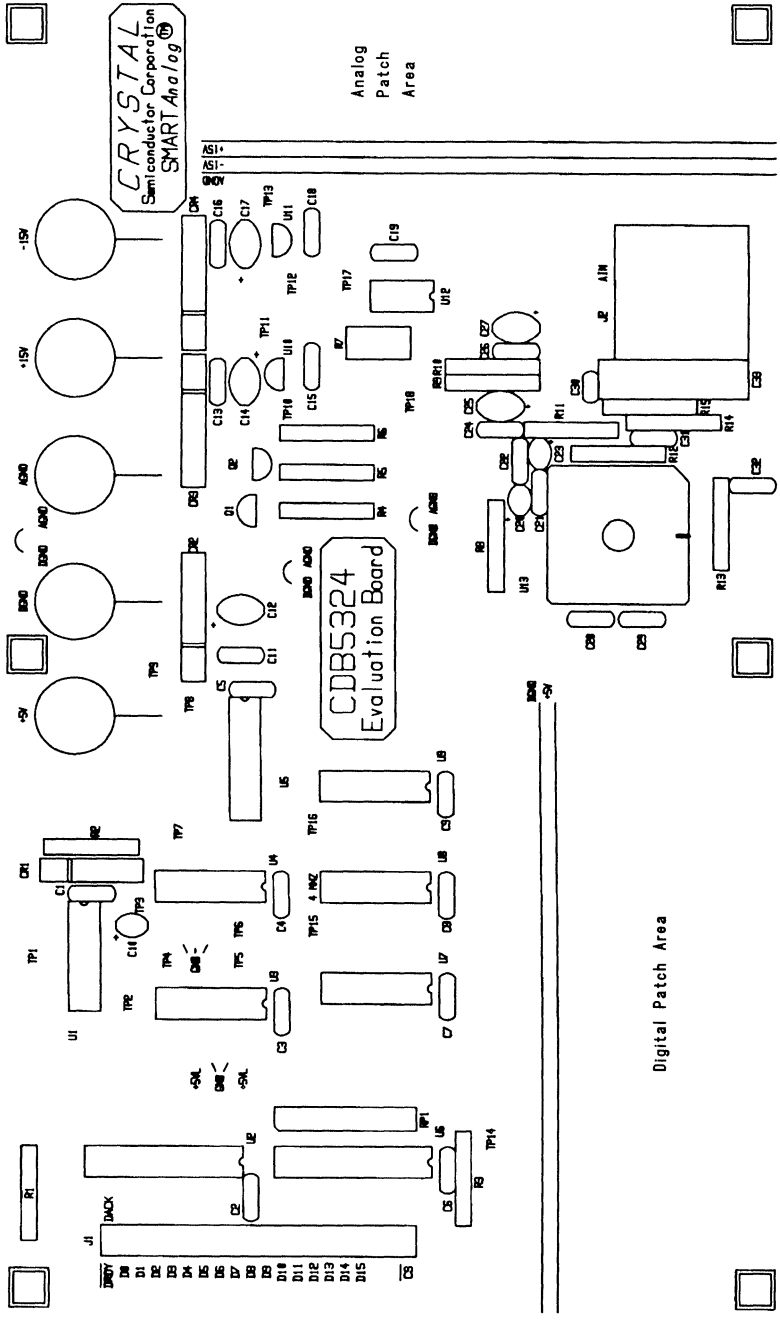


Figure 8. CDB5324 Component Layout

•Notes•

Semiconductor Corporation

CDB5326 CDB5327
CDB5328 CDB5329

Evaluation Board for CS5326, CS5327, CS5328 and CS5329

Features

- Demonstrates recommended layout and grounding arrangements
- Buffered Serial Output Interface
- Jumper Selectable 16 or 18-Bit Parallel Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

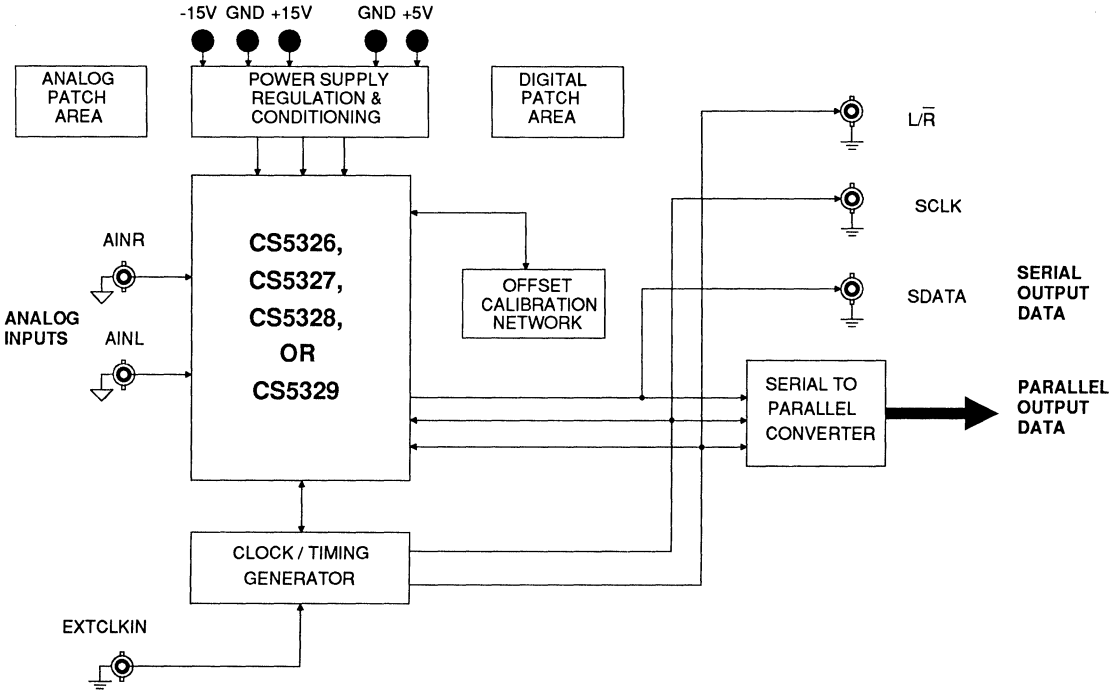
General Description

The CDB5326 and CDB5327 evaluation boards allow fast evaluation of the CS5326 and CS5327 16-bit, stereo A/D converters. The CDB5328 and CDB5329 evaluation boards allow fast evaluation of the CS5328 and CS5329 18-bit, stereo A/D converters. The boards generate all converter timing signals and provide both parallel and serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:

CDB5326, CDB5327, CDB5328, CDB5329



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Power Supply Circuitry

The schematic diagram in Figure 1 shows the evaluation board power supply circuitry. Power is supplied to the evaluation board by five binding posts. The ±5 Volt analog power supply inputs of the converter are derived from ±15 Volts using the voltage regulators U11 and U12. The +5 Volt digital supply for the converter and the discrete logic on the board is provided by the +5V and DGND binding posts. D1, D2 and D4 are transient suppressors which also provide protection from incorrectly connected power supply leads. C25-C28, C30 and C31 provide general power supply filtering for the analog supplies. As shown in Figure 2, C10-C13 provide localized decoupling for the converter VA+ and VA- pins. Note that C13 is connected between VA- and VA+ and not VA- and AGND. Space for a ferrite bead inductor, L1, has been provided so that the board may be modified to power the converter's VD1+ and VD2+ inputs directly from the VA+ supply. Note that the trace connecting VD+ to L1 must be broken before L1 may be installed. R5 and C7 low-pass filter the analog logic power supply pin, VL+. The evaluation board uses both an analog and a digital ground plane which are connected at a single point by J1. This ground plane arrangement isolates the board's digital logic from the analog circuitry.

Analog Inputs

As shown in Figure 2, the analog input signals are connected to the board via the BNC connectors labeled AINL and AINR (for the left and right channel inputs respectively). R1 and C1 provide antialiasing and optimum source impedance for the right analog input channel while R2 and C2 do so for the left channel. The ZEROR and ZEROL inputs are tied to the analog ground plane on the board as shipped from the factory, but space is provided for an optional RC section on each. These RC sections may be added to model the output impedance of the analog signal source for use during an offset calibration.

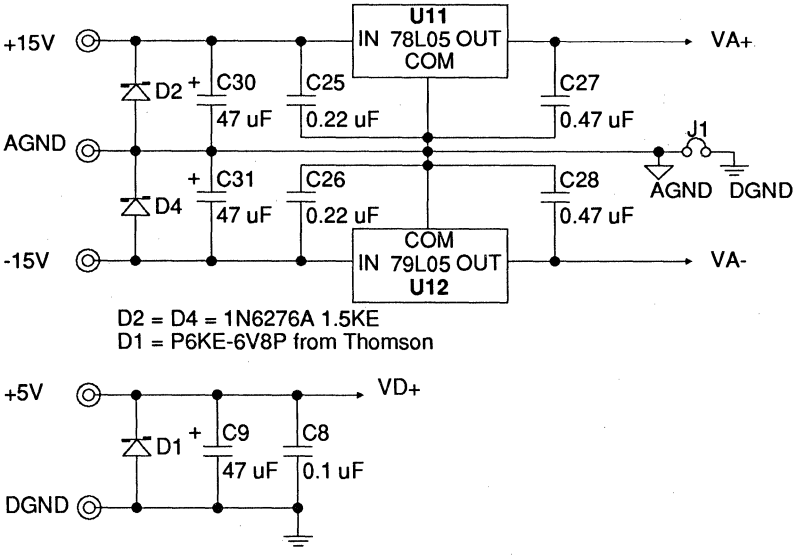


Figure 1. Power Supply Circuitry

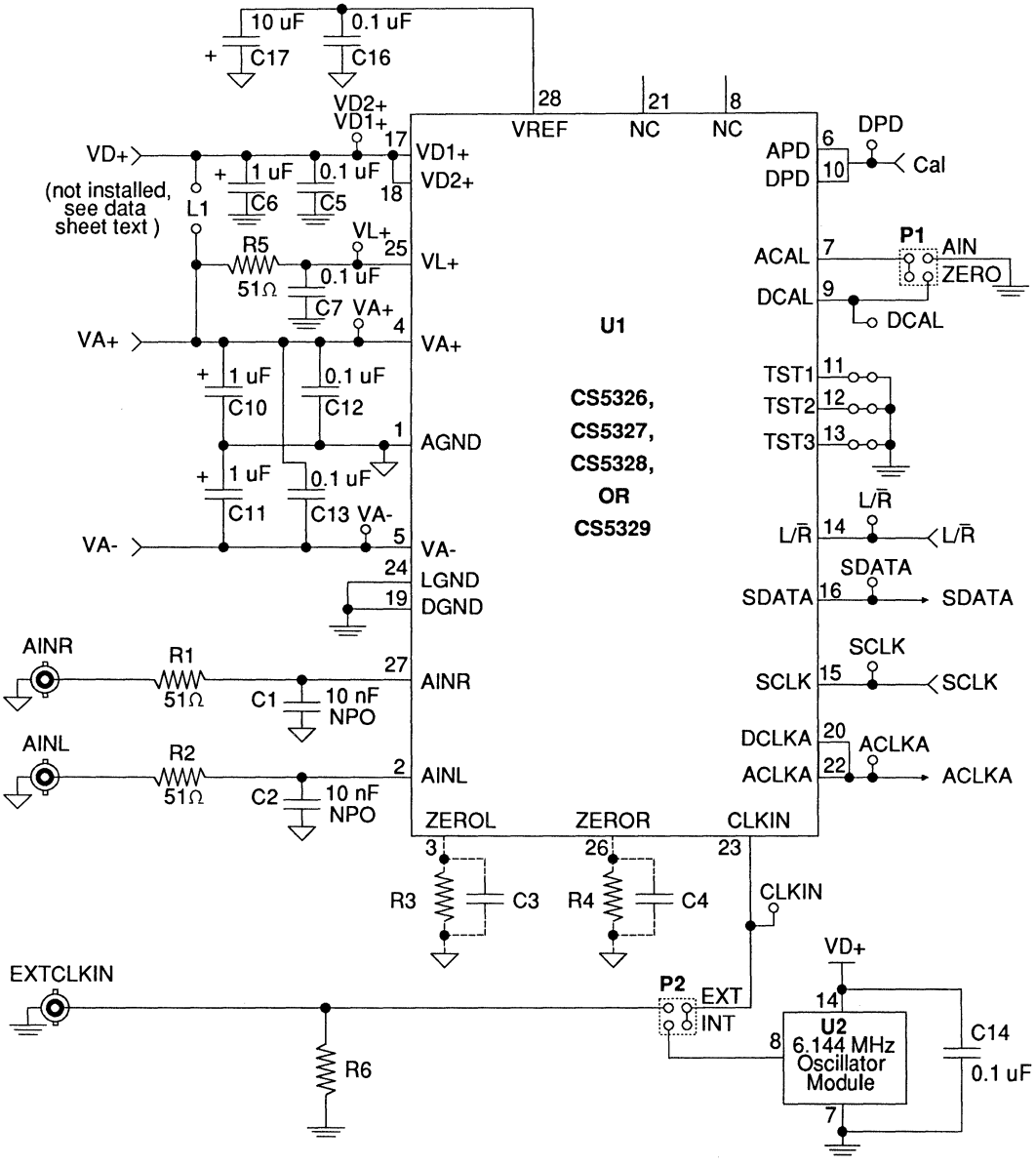


Figure 2. ADC Connections

Timing Generator

P2 selects the master clock source supplied to the CLKIN pin of the converter. As shipped from the factory, P2 is set to the "INT" position to select the 6.144 MHz clock signal provided by U2. An external master clock signal may be connected to the EXTCLKIN connector and selected by placing P2 in the "EXT" position. Note that R6, tied between EXTCLKIN and GND, is available for impedance matching an external clock source. As recommended in the converter's data sheet, SCLK is connected to $\overline{\text{ACLKA}}$ to clock data out of the converter at half the CLKIN frequency as shown in Figure 5. To generate the L/$\overline{\text{R}}$ signal, ACLKA is divided by 64 with the counter U3 shown in Figure 3. Since U3 is an asynchronous counter that advances on falling edges of ACLKA, U9A insures that L/$\overline{\text{R}}$ meets the t_{clr}, t_{aclr}, and t_{scklr} timing requirements specified in the converter's data sheet. The divide by 32 output of U3 is also used to generate the LCLK signal for the parallel output interface.

Parallel Output Interface

Figure 4 depicts the parallel output interface available on the evaluation board. This network assembles 16-bit or 18-bit words from the serial data output by the converter. P6 selects the word size which sould be set to "16" for use with the CS5326 and CS5327 and "18" for use with the CS5328 and CS5329. Each bit of serial data is clocked out of the converter on the rising edge of SCLK and shifted into the 24-bit shift register formed by U4, U5 and U10 on SCLK's falling edge. After all data bits for the selected channel have been shifted into U4, U5 and U10 the data is latched onto P5 by the rising edge of LCLK.

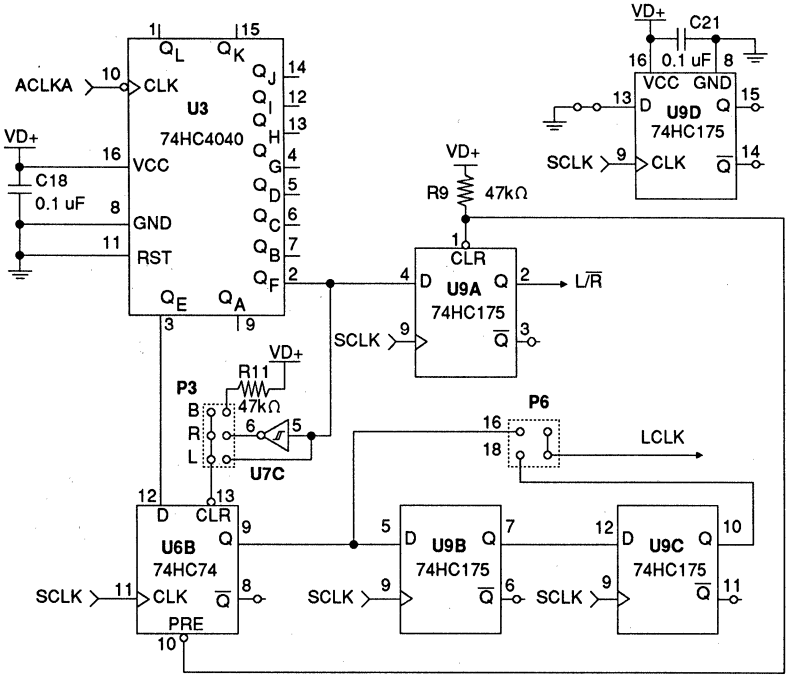


Figure 3. Timing Generator

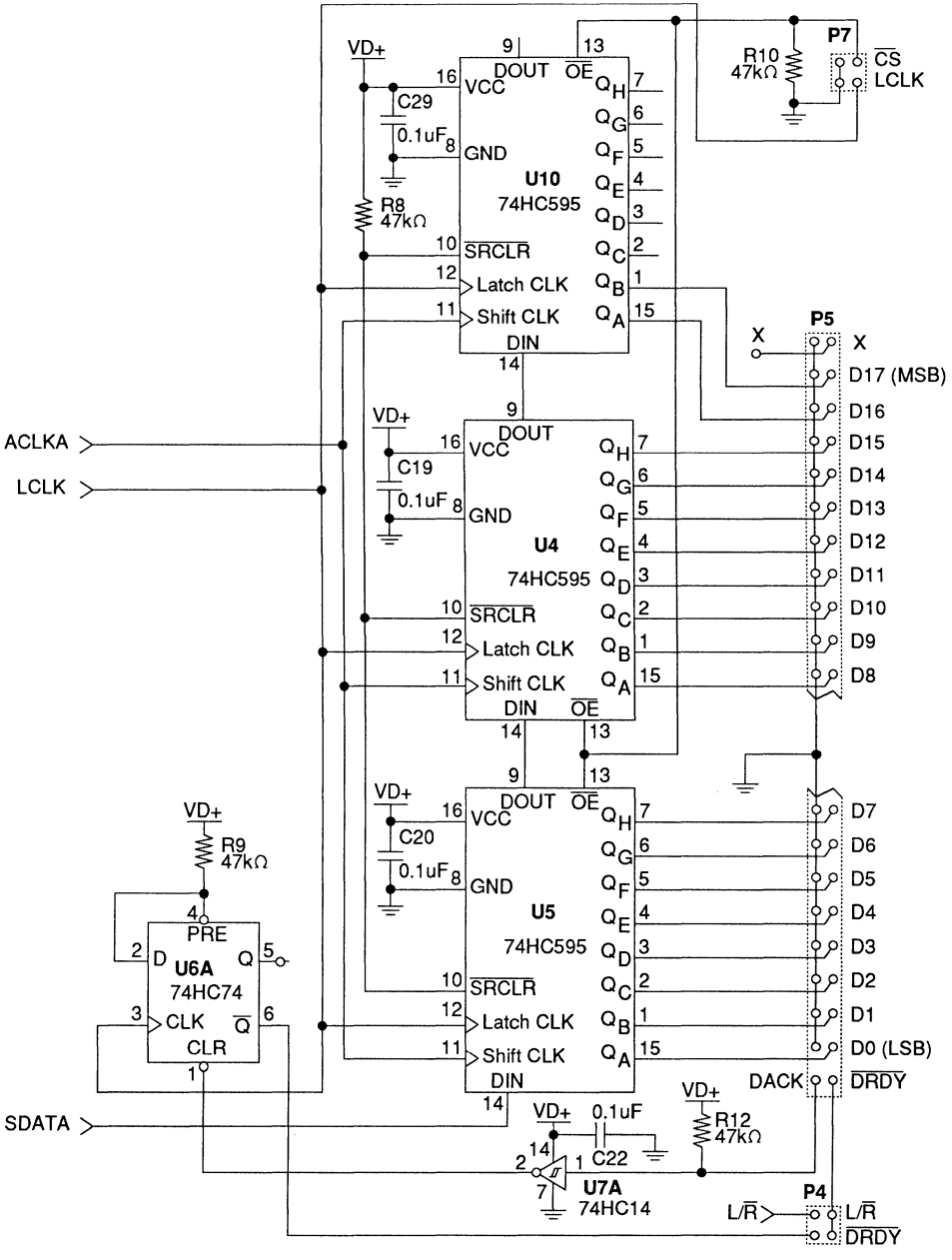


Figure 4. Parallel Output Interface

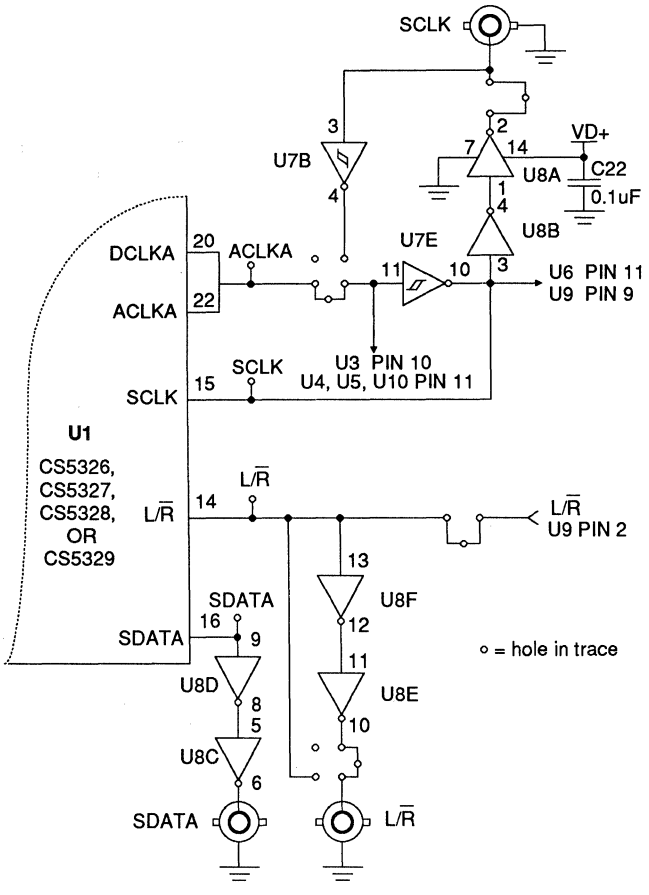


Figure 5. Serial Output Interface

P3 selects the channel whose output data will be converted to parallel form and presented on P5. With P3 in the "B" (both) position, parallel data from one channel will be presented first with data from the other channel presented subsequently. In the "L" (left) position, only left channel conversions will be presented, while in the "R" (right) position only right channel conversions are presented.

Two interface mechanisms are provided for reading the data from this port. With the first, the falling edge of LCLK is used to clock the parallel data into the digital signal processor. (LCLK may be jumpered from P7 to the "X" position of P5.) Alternatively, a handshake protocol implemented with DACK and $\overline{\text{DRDY}}$ may be used to transfer data to the signal processor. The fall of $\overline{\text{DRDY}}$ informs the digital signal processor that a new data word is available. The processor then reads the port and acknowledges the transfer by asserting DACK. Note that $\overline{\text{DRDY}}$ will not be asserted again unless DACK is momentarily brought high although new data will continue to be latched onto the port.

Serial Output Interface

The serial output interface is provided by the SDATA, SCLK, and L/$\overline{R}$ BNC connectors on the evaluation board. These outputs are buffered, as shown in Figure 5, in order to isolate the converter from the digital signal processor. Serial data is clocked out of the converter by the $\overline{ACLKA}$ signal at half of the master clock frequency. Note that in this configuration the serial output data is clocked out during the first part of each L/$\overline{R}$ cycle. After the data for the selected channel has been clocked out, zeros are clocked out during the remaining SCLK cycles before L/$\overline{R}$ changes state.

Offset Calibration Circuit

Figure 6, shows the optional offset calibration circuit provided on the evaluation board. Upon power-up, this circuit provides a pulse on the Analog to Digital Converter's DPD and APD pins initiating an offset calibration cycle. Releasing SW1 also initiates an offset calibration cycle. P1 selects the signal source used during offset calibration. In the "AIN" position, the AINL and AINR inputs are selected during calibration, while in the "ZERO" position, the ZEROL and ZEROR inputs are selected.

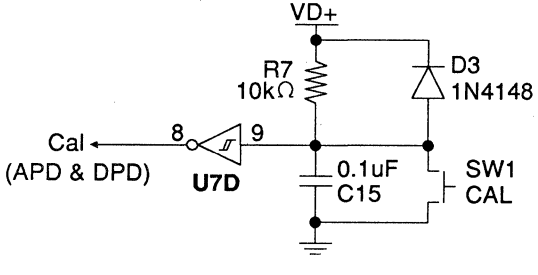


Figure 6. Offset Calibration Circuit

Configuring the Board for External Timing

An external master clock may be supplied to the board directly via the EXTCLKIN input. The board's SCLK and L/$\overline{R}$ connectors may also be configured to accept input signals. This is accomplished with a simple modification. As shown in Figure 5, holes (represented by hollow circles) in the SCLK and L/$\overline{R}$ traces have been added to accomodate installing jumper wires and to facilitate breaking traces. Drilling through the surface pad of one of these holes with a small twist drill effectively breaks the trace and allows it to be driven by another source attached at an adjacent hole. This technique can be used to connect the converter to externally generated SCLK and L/$\overline{R}$ signals during system development. Note that the SCLK trace must be broken at U8 pin 2 and U1 pin 22 before it may be configured as an input. Similarly, the L/$\overline{R}$ trace must be broken at U9 pin 2 and U8 pin 10 before the BNC connector may be configured as an input.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+15	input	+15 Volts from power supply
-15	input	-15 Volts from power supply
AGND	input	analog ground connection from power supply
+5	input	+5V for ADC VD1+ / VD2+ and discrete logic
DGND	input	digital ground connection from power supply
AINL	input	left channel analog input
AINR	input	right channel analog input
EXTCLKIN	input	external master clock input
L/$\overline{R}$	output	left /right channel signal
SDATA	output	serial output data
SCLK	output	serial output clock
P5	output	parallel output data
P7(LCLK)	output	latch clock for U4, U5, and U10 output registers
P7($\overline{CS}$)	input	output enable for U4, U5, and U10 output registers

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
P1	selects offset calibration input source	AIN	AINL and AINR selected during offset calibration
		*ZERO	ZEROL and ZEROR selected during offset calibration
P2	selects master clock source for CS5326 CLKIN	*INT	CLKIN provided by U2
		EXT	CLKIN provided by EXTCLKIN BNC
P3	selects channel for serial to parallel conversion	*L	left channel data presented on P5
		R	right channel data presented on P5
		B	left then right channel data alternately presented on P5
P4	selects L/$\overline{R}$ or $\overline{DRDY}$ as the output status signal presented on P5	*$\overline{DRDY}$	$\overline{DRDY}$ selected to signal the arrival of new data for the selected channel
		L/$\overline{R}$	L/$\overline{R}$ selected
P6	selects 16-bit or 18-bit parallel output word size	16	16-bit data on P5 (D15..D0) for CS5326 and CS5327
		18	18-bit data on P5(D17..D0) for CS5327 and CS5329

* Default setting from factory

Table 2. Jumper Selectable Options

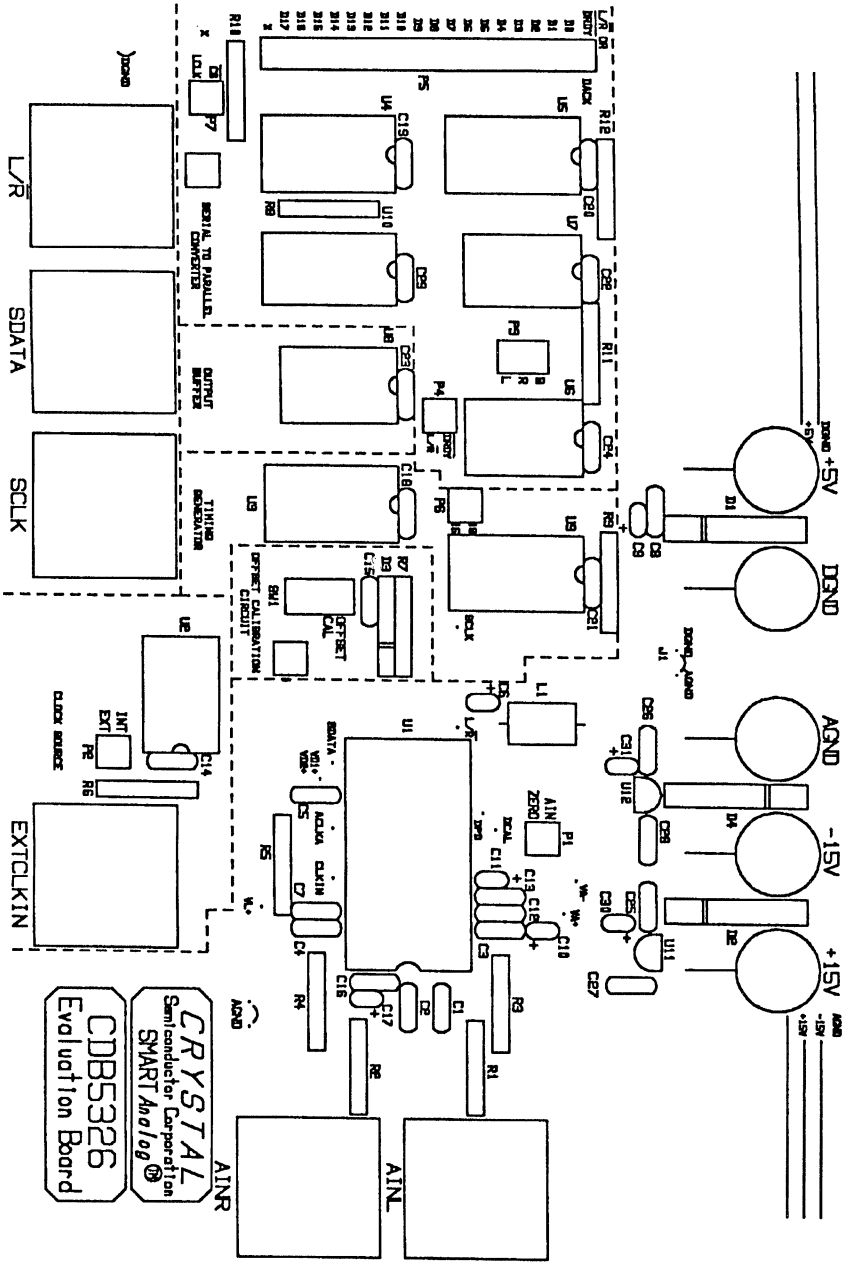


Figure 7. Board Layout

•Notes•

Semiconductor Corporation

CDB5336 CDB5337
CDB5338 CDB5339

Evaluation Board for CS5336, CS5337, CS5338 and CS5339

Features

- Demonstrates recommended layout and grounding arrangements
- Buffered Serial Output Interface
- Jumper Selectable 16 or 18-Bit Parallel Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

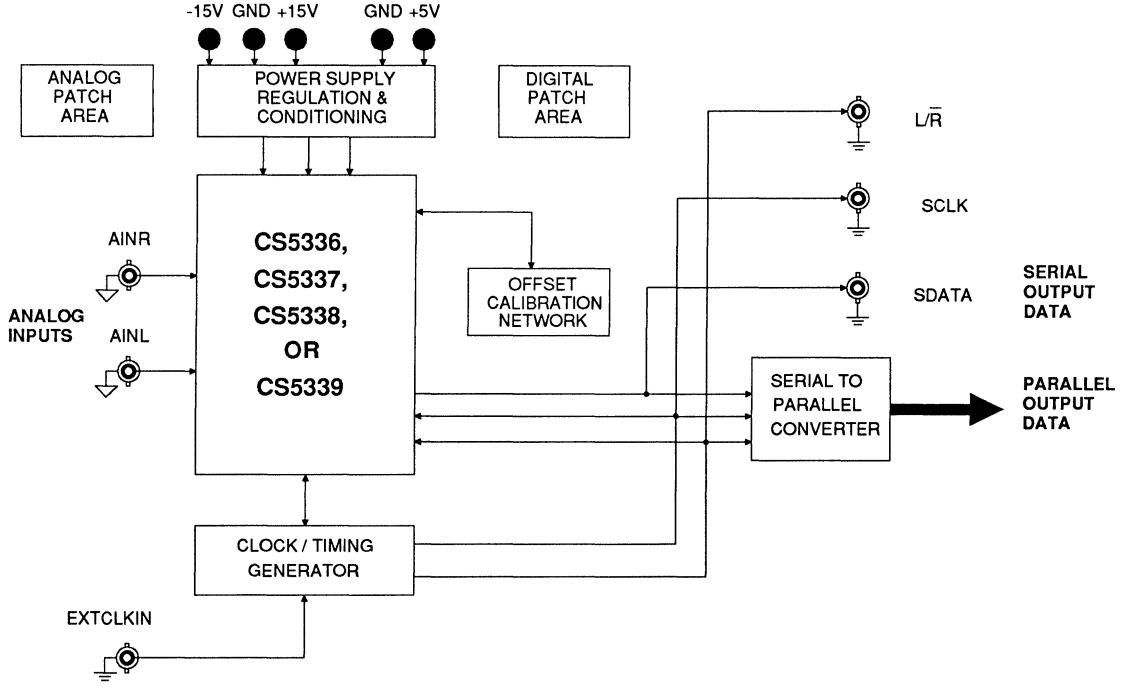
General Description

The CDB5336, CDB5337 CDB5338 and CDB5339 evaluation boards allow fast evaluation of the CS5336, CS5337, CS5338 and CS5339 16-bit, stereo A/D converters. The boards generate all converter timing signals and provide both parallel and serial output interfaces. Evaluation requires a digital signal processor, a low-distortion signal source, and a power supply.

The evaluation boards may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION:

CDB5336, CDB5337, CDB5338, CDB5339



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•Notes•

Semiconductor Corporation

CDB5412

CS5412 Evaluation Board

Features

- Throughout Rates to 1MHz
- Jumper Selectable
  Unipolar/Bipolar Input Range
  Continuous Conversion
- Buffered 12-Bit Data
- Optional Phase-Locked-Loop to Synchronize to Sampling Signal
- Adjustable Voltage Reference
- PC/uP-Compatible Header Connection

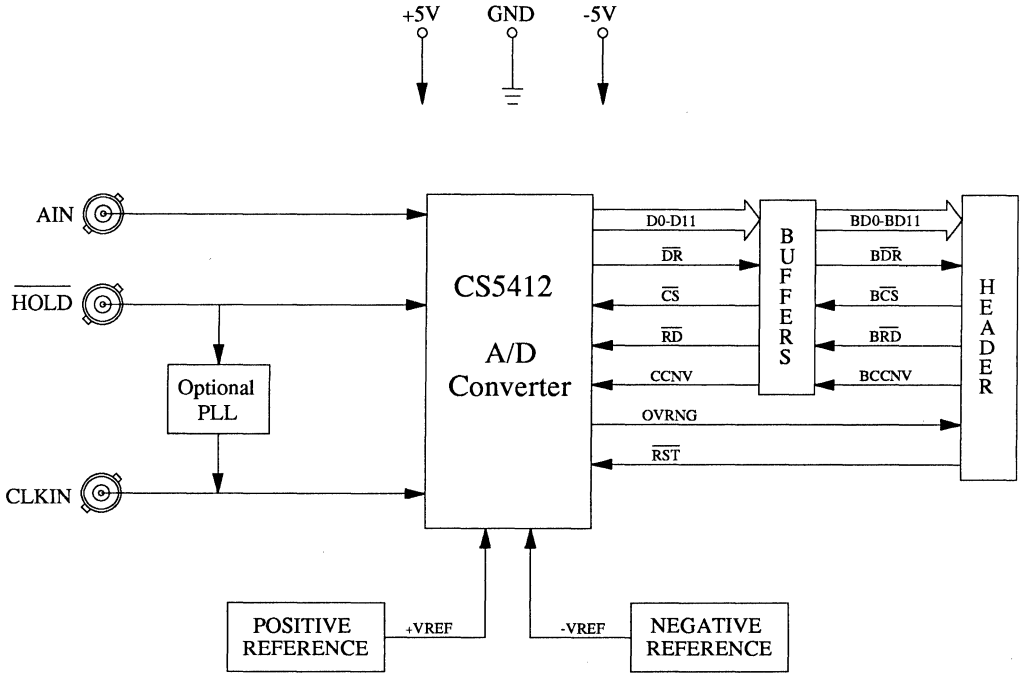
General Description

The CDB5412 is a completed, tested evaluation board for the CS5412 12-bit high-speed analog to digital converter. It includes a CS5412 and all of the components necessary to quickly and thoroughly verify the converter's performance under a wide variety of operating conditions.

On-board circuitry includes voltage references and clock circuitry, plus data buffers, so that the user need only supply power and an input signal to exercise the CS5412.

An on-board phase-locked-loop may be used to simulate systems that have a periodic sample clock not synchronized to a system clock, or where a clock 8 times the sampling clock is not available.

ORDERING INFORMATION: CDB5412



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Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 TWX: 910-874-1352

GENERAL DESCRIPTION

The CDB5412 Evaluation Board is a stand-alone environment for easy lab evaluation of the CS5412 High-Speed Analog-to-Digital Converter. Positive and negative references are included on the board and can be configured for ±1.5 volt bipolar or 0-to-3 volt unipolar operation. The digital output of the CS5412 is buffered and series terminated allowing the board to drive twisted-pair ribbon cable. The CDB5412 also includes an optional phase-locked-loop (PLL) that will generate the requisite master clock given a periodic sample clock. When supplied with the necessary +5 volt and -5 volt power supplies and an analog signal source, the CDB5412 will provide converted data at the 40 pin header.

The CDB5412 is designed to allow easy and thorough evaluation of the performance of the CS5412. The CDB5412 is a four layer board with one signal layer, two power planes, and a ground plane; the decoupling scheme is designed to insure accurate evaluation of the converter's performance for a wide variance in the quality of the power supplies.

The CDB5412 can also be used as a performance benchmark when designing your own system, and for ideas on appropriate layout schemes.

Before starting an evaluation, we strongly recommend reviewing the CS5412 data sheet. A thorough understanding of the CS5412 will make it easier to quickly and fully evaluate the part.

Suggested Evaluation Method

One efficient method of dynamically evaluating the CS5412 using the CDB5412 is to connect AIN to a spectrally pure sine wave and collecting a consecutive number of samples. FFT analysis can then be done on the samples to produce signal-to-noise and signal-to-distortion ratios.

Equipment needed consist of the following:

- CDB5412 Evaluation Board
- Good split power supply capable of supplying +5V and -5V.
- A spectrally pure sine wave generator such as the Krohn-Hite Model 4400A "Ultra-Low Distortion Oscillator"
- High-speed data storage
- Computer/PC capable of acquiring data from high-speed data storage
- A software routine to perform a Fast Fourier Transform (FFT)

The sine-wave generator supplies the analog signal, AIN, to the CDB5412. Converted data will appear at the header since the board is, by default, in the continuous convert mode.

The header is connected to the high-speed storage. This storage can consist of FIFO's, or static RAM and counters, or a logic analyzer with the ability to transfer data to a computer or PC. If FIFO's or static RAMs are employed, and a PC is the host computer, a data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface" can be used to transfer the data to the PC. If the input signal is not synchronized with the sample frequency so that an integer number of periods is acquired, the data must be windowed to avoid end point discontinuities. We use the Blackman-Harris window which forces the endpoints to zero. An FFT analysis on the resulting data will yield spectral information on the converter. Figure 1 graphically illustrates the results of such analysis. For Figure 1, 1024 consecutive samples were taken with the CDB5412 sampling a 100kHz sine wave input at 1 MHz. The samples were modified by the Blackman-Harris window before FFT analysis.

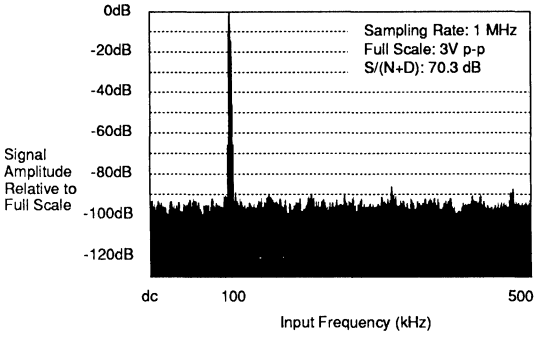


Figure 6. Typical CS5412 FFT Performance

References:
F.J. HARRIS, "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transfer", Proc. IEEE, Vol. 66, No. 1, Jan. 1978, pp. 51-83 .

G.D. BERGLAND & M.T. DOLAN, "Fast Fourier Transform Algorithms", Programs for Digital Signal Processing, IEEE Press: 0-87942-127-4, Section 1.2.

BOARD DESCRIPTION

MODES

Continuous Convert

The default mode for the CDB5412 is continuous convert (CCNV) active with the PLL inactive. Therefore, the CS5412 is always converting and the $\overline{\text{HOLD}}$ signal is not used. The part can be taken out of continuous convert mode in one of two ways, either by placing a strap jumper on J6 or by driving BCCNV at the stake header low. Once out of continuous convert mode, the $\overline{\text{HOLD}}$ signal must be driven. $\overline{\text{HOLD}}$ is described in greater detail in the "Inputs" section.

Unipolar/Bipolar

The CDB5412 board is factory calibrated for bipolar mode (AIN = ±1.5 Vpeak). In bipolar mode, strap jumpers are placed on J3 and J5 (both marked with a "B") which are located in the Negative Reference, Figure 2, and the Positive Reference, Figure 3.

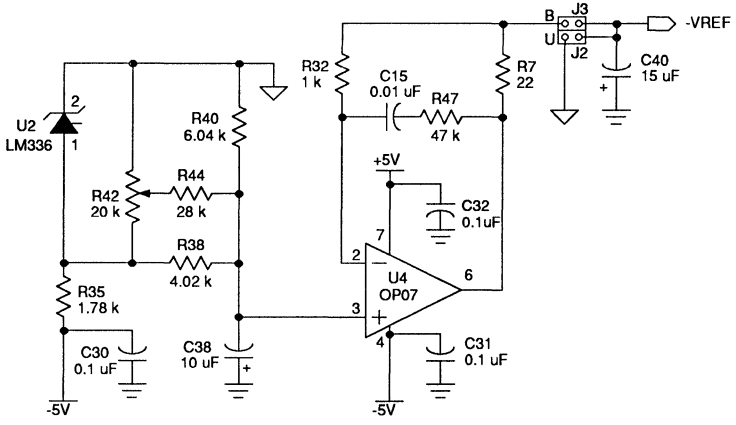


Figure 2. Negative Reference

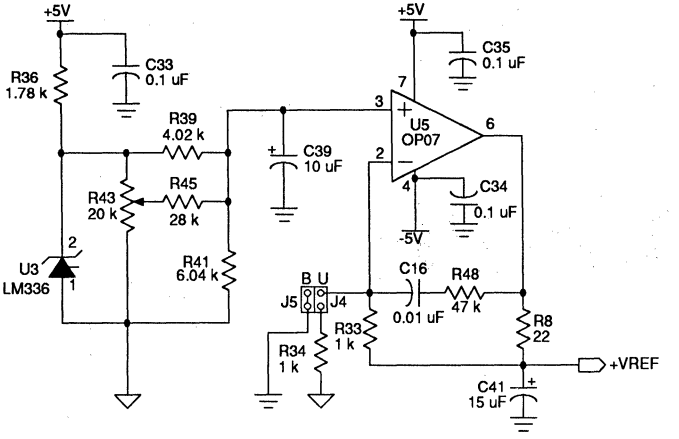


Figure 3. Positive Reference

To operate the board in unipolar mode (AIN = AGND to +3 Vpeak), move the strap jumpers to J2 and J4 (both marked with a "U"). The positive reference pot, R43, must be calibrated to +3.000 volts at +VREF (pin 7) of the CS5412 converter.

When receiving a new board, Crystal recommends that the reference voltages, +VREF and -VREF, be verified before operation. The pots located in their respective reference section may be tweaked to calibrate the voltage level which should be measured at the CS5412 converter.

Calibration

Since the Reset switch provides a means to calibrate the part, the CAL pin is hard-wired to ground through jumper J1. The reset signal is also available at the stake header and can be driven by any source that can drive a 1 kΩ resistor connected to +5 volts (see Figure 5).

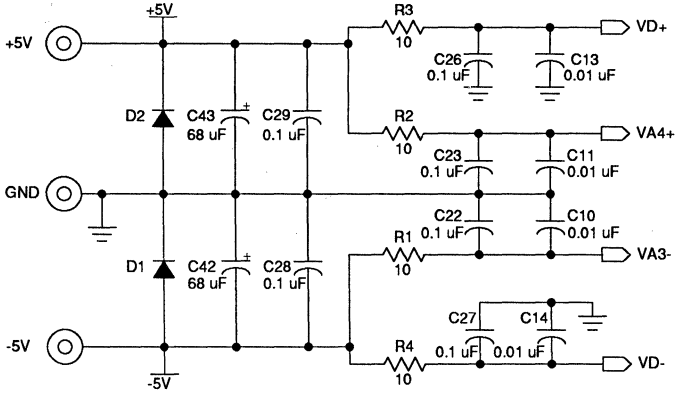


Figure 4. Power Supply

INPUTS

Power Supplies

A split supply should be used to generate +5 volts and -5 volts. These should be connected to their respective banana jacks on the board. A good quality low ripple, low noise supply will give the best performance.

Figure 4 depicts power supply decoupling for the CDB5412, along with decoupling for the digital supplies and the isolated analog supplies, both of which are low-pass filtered to prevent noise from coupling into the analog supplies. Since the digital supply is derived from the analog supply, the digital supply is guaranteed to be less than or equal to the analog supply as specified in the CS5412 data sheet.

Analog In -AIN

The factory setting for AIN is a shorting wire in R12 and an NPO capacitor, C3, to ground. If the input signal is noisy, the shorting wire should be

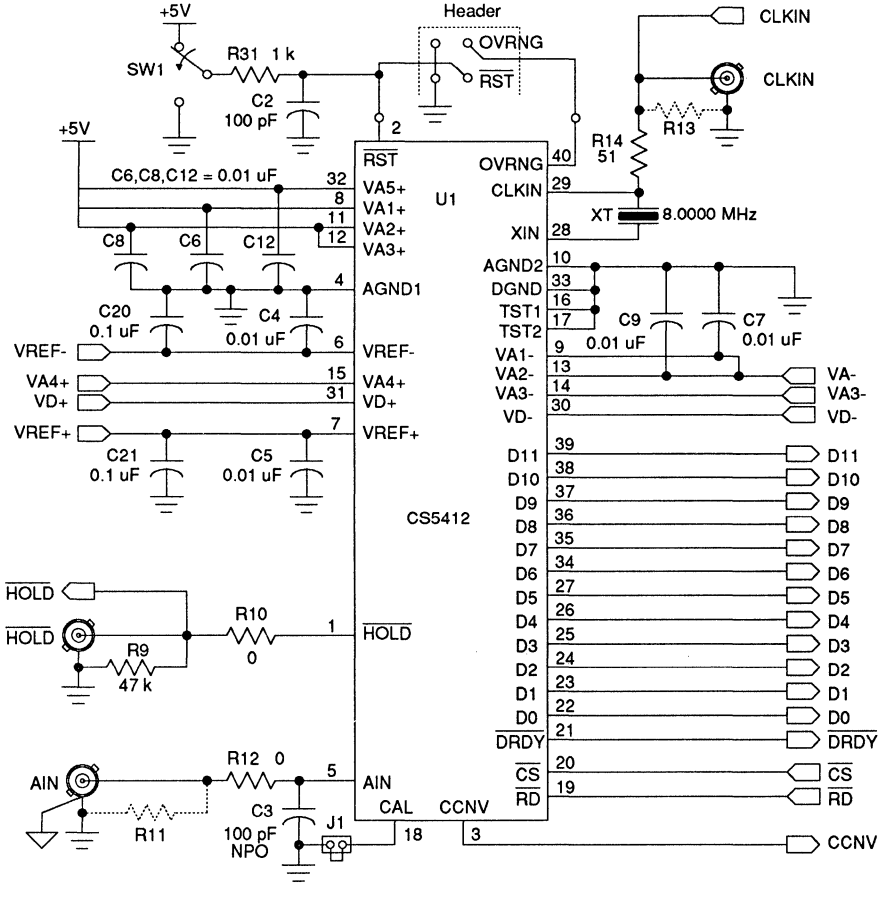


Figure 5. 5412 Flash A/D Converter

replaced with an appropriate resistor to low-pass filter the input noise.

In addition to the input filtering capability, R11 is available for impedance matching. If the source driving AIN has low impedance, an appropriate termination resistor should be soldered in R11. (see Figure 5.)

Clock -CLKIN

The CDB5412 has an 8.0000 MHz crystal installed at the factory which generates a sample frequency of 1 MHz. If another sample frequency is desired, either replace the crystal or remove the crystal from its socket and use the CLKIN BNC to generate other master clock frequencies. R14 provides series termination of 51 Ω. R13 may be used for parallel termination but must be left open for the crystal to oscillate (factory setting). CLKIN can also be generated by the on-board PLL. The PLL, when active, will generate a CLKIN frequency eight times the frequency of the $\overline{\text{HOLD}}$ signal. For more information on the PLL, see the "Phase-Locked- Loop" section.

Hold -$\overline{\text{HOLD}}$

As described in the Continuous Convert section, the CDB5412 is factory set not to use the $\overline{\text{HOLD}}$ input. Driving the $\overline{\text{HOLD}}$ input while the CS5412 is in the continuous convert mode will give erratic results. To use the $\overline{\text{HOLD}}$ signal, the CCNV signal must be driven low by placing a strap jumper on J6 or by driving the BCCNV signal at the stake header low. As described in the CS5412 data sheet, the $\overline{\text{HOLD}}$ signal must be modulo eight and synchronized to the master clock, CLKIN.

Since $\overline{\text{HOLD}}$ must not be left floating, the factory configuration is a shorting wire in R10 (series termination) and a 47k Ω resistor (R9) to ground. This configuration ties $\overline{\text{HOLD}}$ to ground (through R9) and provides fairly high impedance when driving $\overline{\text{HOLD}}$ externally.

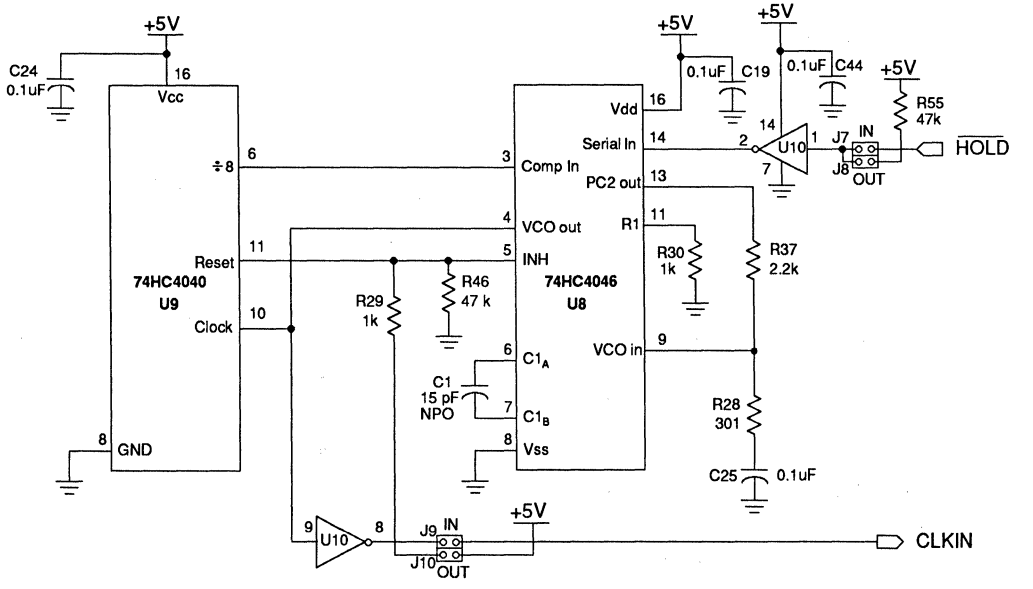


Figure 6. Phase-Locked-Loop

If the signal source used to drive $\overline{HOLD}$ is low impedance, R9 should be replaced with the appropriate resistor. R10 can provide series termination.

Phase-Locked-Loop - (PLL)

The CDB5412 contains an optional Phase- Locked-Loop (PLL) which can be used by systems containing a periodic sampling clock, $\overline{HOLD}$, but no master clock, CLKIN. The PLL generates a clock eight times the frequency of $\overline{HOLD}$ and the PLL drives the CLKIN pin.

The schematic for the PLL is shown in Figure 6. Shorting jumpers on J8 and J10 (both marked "OUT") disable the PLL (factory setting). To enable the PLL move the jumpers from J8 and J10 to J7 and J9 (both marked "IN"). Since the CLKIN pin is driven by the PLL, the on-board crystal should be removed and the CLKIN BNC must not be driven or loaded by an external source.

The PLL will not work with a sampling signal, $\overline{HOLD}$, that is not periodic. The PLL is designed to work with a $\overline{HOLD}$ signal range of 300 kHz to 1 MHz. To redesign the PLL for other frequencies see the National Semiconductor 74HC4046 PLL Data Sheet.

OUTPUTS

The 12 data bits output from the CS5412 are buffered as shown in Figures 7 and 8, which minimize loading of the converters outputs. Series resistors are then used to minimize ringing when connected to twisted-pair ribbon cable. The +5 volt supply for the buffers is derived from the analog supply using the same low-pass RC network used on the digital supplies of the CS5412.

Three of the signals at the stake header are inputs to the board (Figure 8). $\overline{BCS}$ and $\overline{BRD}$ are pulled

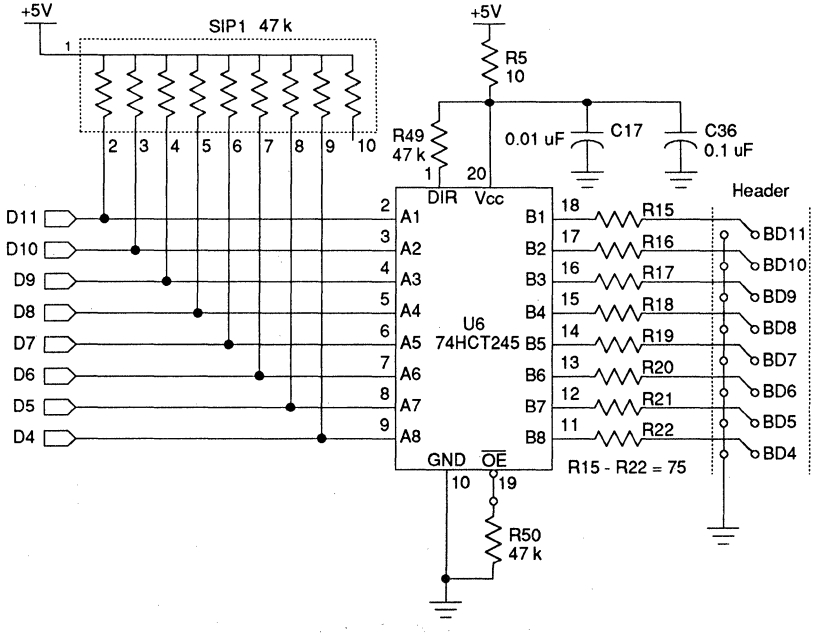


Figure 7. Upper Buffer

down to ground through a resistor allowing the CS5412 to continually output data as soon as it becomes available. The third input is a buffered continuous convert signal, BCCNV. By default this signal is pulled up to +5 volts through a resistor, which configures the CS5412 to convert at one eighth the master clock frequency. (The $\overline{\text{HOLD}}$ BNC must not be driven in this mode.)

The 20 stake header pins opposite the signal names are all tied to ground. Signals with a "B" prefix indicate buffered signals. The "X" and "Y" pins are unused and allow customization of the CDB5412 evaluation board.

Figure 9 illustrates the CDB5412 board layout to help in locating components.

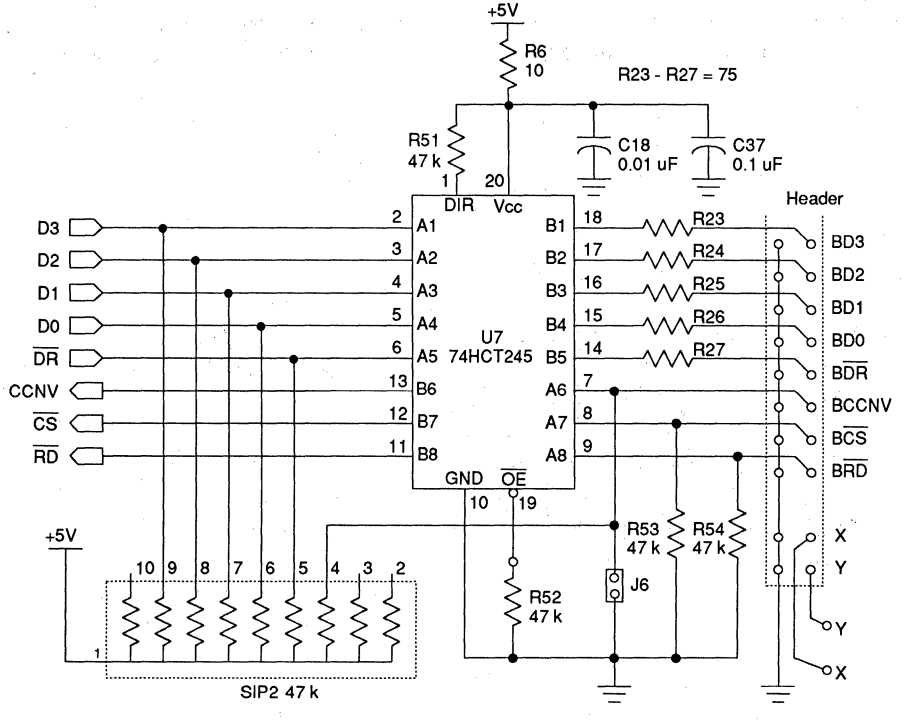


Figure 8. Lower Buffer

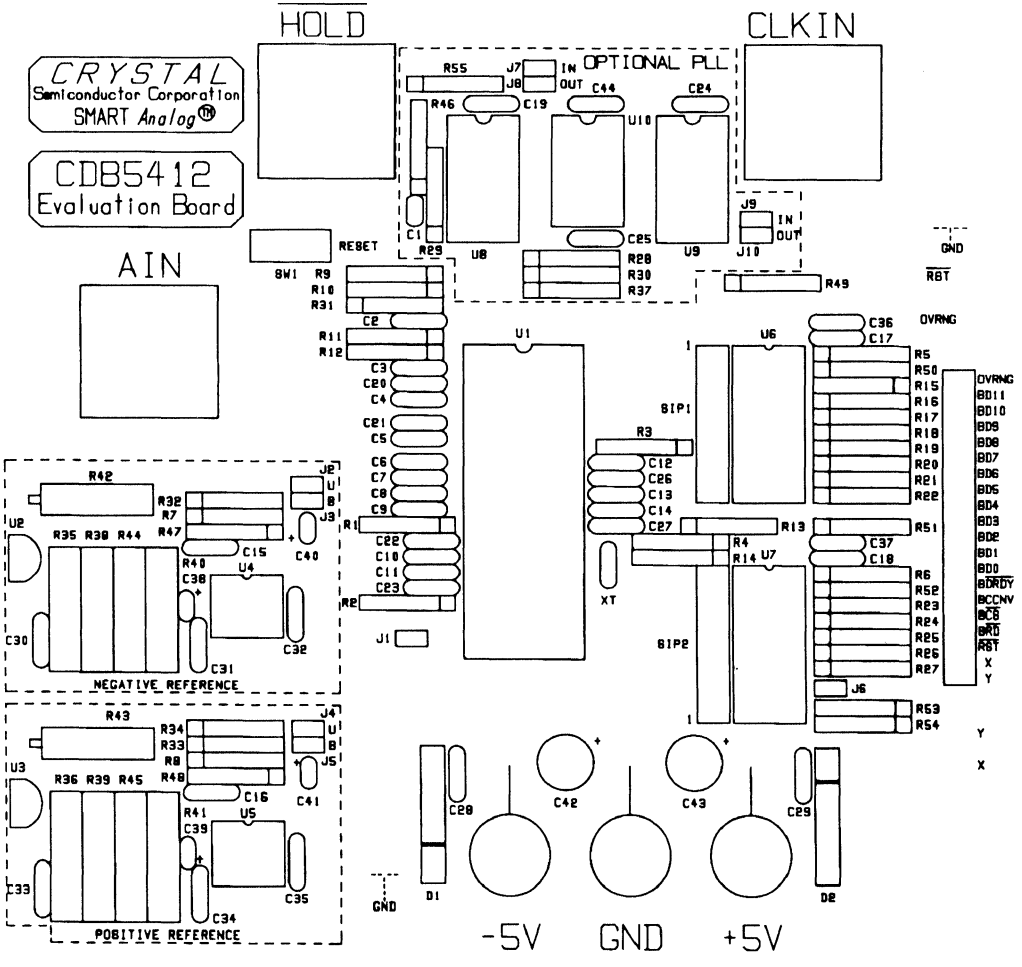


Figure 9. CDB5412 Board Layout

•Notes•

Semiconductor Corporation

CDB5501/CDB5503

CS5501 /CS5503 Evaluation Board

Features

- Operation with on-board clock generator, on-board crystal, or an off-board clock source.
- DIP switch selectable or micro port controllable:
  - Unipolar/Bipolar input range
  - Sleep Mode
  - All Cal Modes
- On-board Decimation Counter
- Multiple Data Output Interface Options:
  - RS-232 (CS5501)
  - Parallel Port (CS5501)
  - Micro Port (CS5501 & CS5503)

General Description

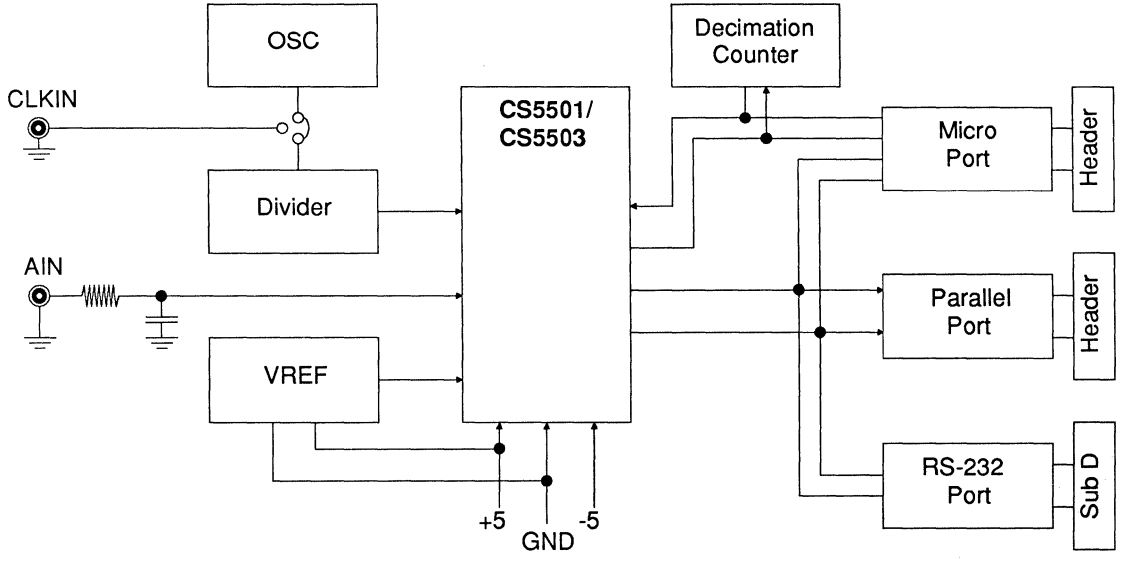
The CDB5501/CDB5503 is an evaluation board designed for maximum flexibility when evaluating the CS5501/CS5503 A/D converters. The board can easily be configured to evaluate all the features of the CS5501/CS5503, including changes in master clock rate, calibration modes, output decimation rates, and interface modes.

The evaluation board interfaces with most microcontrollers and allows full control of the features of the CS5501 or CS5503. DIP switch selectable control is also available in the event a microcontroller is not used. The evaluation board also offers computer data interfaces including RS-232 and parallel port outputs for evaluating the CS5501.

All calibration modes are selectable including Self-Cal, System Offset Cal, and System Offset and System Gain Cal. A calibration can be initiated at any time by pressing the CAL pushbutton switch.

ORDERING INFORMATION: CDB5501 or CDB5503

Block Diagram



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INTRODUCTION

The CDB5501/CDB5503 evaluation board provides maximum flexibility for controlling and interfacing to the CS5501/CS5503 A/D converters. The CS5501 or the CS5503 require a minimal amount of external circuitry. The devices can operate with a crystal (or ceramic resonator) and a voltage reference.

The evaluation board includes several clock source options, a 2.5 volt trimmable reference, and circuitry to support several data interface schemes. The board operates from +5 and -5 volt power supplies.

Evaluation Board Overview

The CDB5501/CDB5503 evaluation board includes extensive support circuitry to aid evaluation of the CS5501/CS5503. The support circuitry includes the following sections:

1) A clock generator which has an on-board oscillator and counter divider IC.
2) A 2.5 volt trimmable voltage reference.
3) A Decimation Counter.
4) A parallel output port (for CS5501 only).
5) An RS-232 interface (for CS5501 only).
6) A micro port (for CS5501 or CS5503).
7) DIP switch and CAL pushbutton.

Clock Generator

The CS5501/CS5503 can operate off its on-chip oscillator or an off-chip clock source. The evaluation board includes a 4.9152 MHz gate oscillator and counter-divider chain as the primary clock source for the CS5501/CS5503. The counter-divider outputs offer several jumper-selectable frequencies as clock inputs to the CS5501/CS5503. The 4.9152 MHz crystal frequency was chosen to allow the counter-divider chain to also provide the common serial data rates (1200, 2400, 4800, etc.) when the CDB5501 evaluation board is configured to provide RS-232 data output. If a different operating frequency for the CS5501/CS5503 is desired, three options exist. First, a BNC input is provided to allow an external CMOS (+5V) compatible clock to be used. Second, the crystal (Y1) in the on-board gate oscillator can be changed. Or, third, the on-chip oscillator of the CS5501/CS5503 can be used with a crystal connected in the Y2 position.

2. 5 Volt Reference

A 2.5 volt (LT1019CN8-2.5) reference is provided on the board. Potentiometer R9 allows the initial value of the reference to be accurately trimmed.

Decimation Counter

The CS5501/CS5503 updates its internal output register with a 16-bit word every 1024 clock cycles of the master clock. Each time the output register is updated the $\overline{DRDY}$ line goes low. Although output data is updated at a high rate it may be desireable in certain applications to activate the $\overline{CS}$ to read the data at a much lower rate. A decimation counter is provided on the board for this purpose. The counter reduces the rate at which the $\overline{CS}$ line of the CS5501 is activated by only allowing $\overline{CS}$ to occur at a sub-multiple of the $\overline{DRDY}$ rate.

Parallel Output Port (for CS5501 only)

The output data from the CS5501/CS5503 is in serial form. Some applications may require the data to be read in parallel format. Therefore the evaluation board includes two 8-bit shift registers with three-state outputs. Data from the CS5501 is shifted into the registers and then read out in 16-bit parallel fashion. The parallel port comes set up for 16-bit parallel output but can be reconfigured to provide two 8-bit reads. The parallel port supports the CS5501 only, since the CS5503 outputs 20-bit words.

RS-232 Port (for CS5501 only)

The CS5501 has a data output mode in which it formats the data to be UART compatible; each serial output byte is preceeded by a start bit and terminated with two stop bits. Serial data in this format is commonly transferred using the RS-232 data interface. Therefore the evaluation board includes an RS-232 driver and output connector. The CS5503 does not provide this output mode.

Micro Port

The CS5501/CS5503 was designed to be compatible with many micro-controllers. Therefore the evaluation board provides access to all of the data output pins and the control pins of the CS5501/CS5503 on header connectors.

DIP Switch and CAL Pushbutton

Although all of the control lines to the CS5501/CS5503 are available on header connectors at the edge of the board, it is preferable to not require software control of all of these pins. Therefore DIP switch control is provided on some of these control lines. The CAL input to the CS5501/CS5503 is made available at a header pin for remote control, but pushbutton control of CAL is also provided.

Jumper Selections

The evaluation board has many jumper selectable options. This table describes the jumper selections available.

P1 Selects between the on-board 4.9152 MHz oscillator (INT) or an external (EXT) clock source as the input to the clock generator/ divider chain.

P2 Allows any of the counter/divider output clock rates to be selected as the input clock to the CS5501/CS5503.

P3 Allows selection of baud rate clocks when the CS5501 is in the UART compatible mode. When using the on-board 4.9152 MHz standard baud rates between 1200 and 19,200 are available.

P4 Selects the divide ratio of the Decimation Counter.

P5 Selects one of the three available output data modes of the CS5501 or one of two available output data modes of the CS5503.

P9 Enables the output of the Decimation Counter to control the $\overline{CS}$ line of the CS5501/CS5503.

P11 Connects the baud clock from the on-board clock divider as the input to the SCLK pin of the CS5501/CS5503.

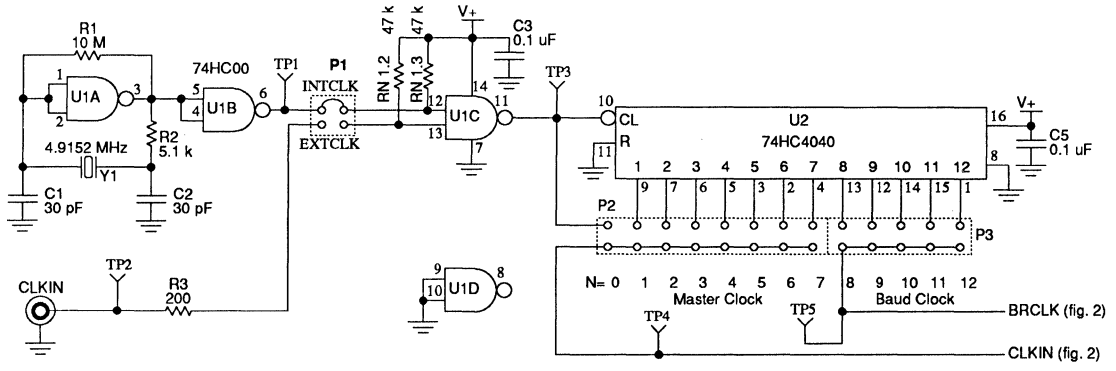


Figure 1. Clock Generator

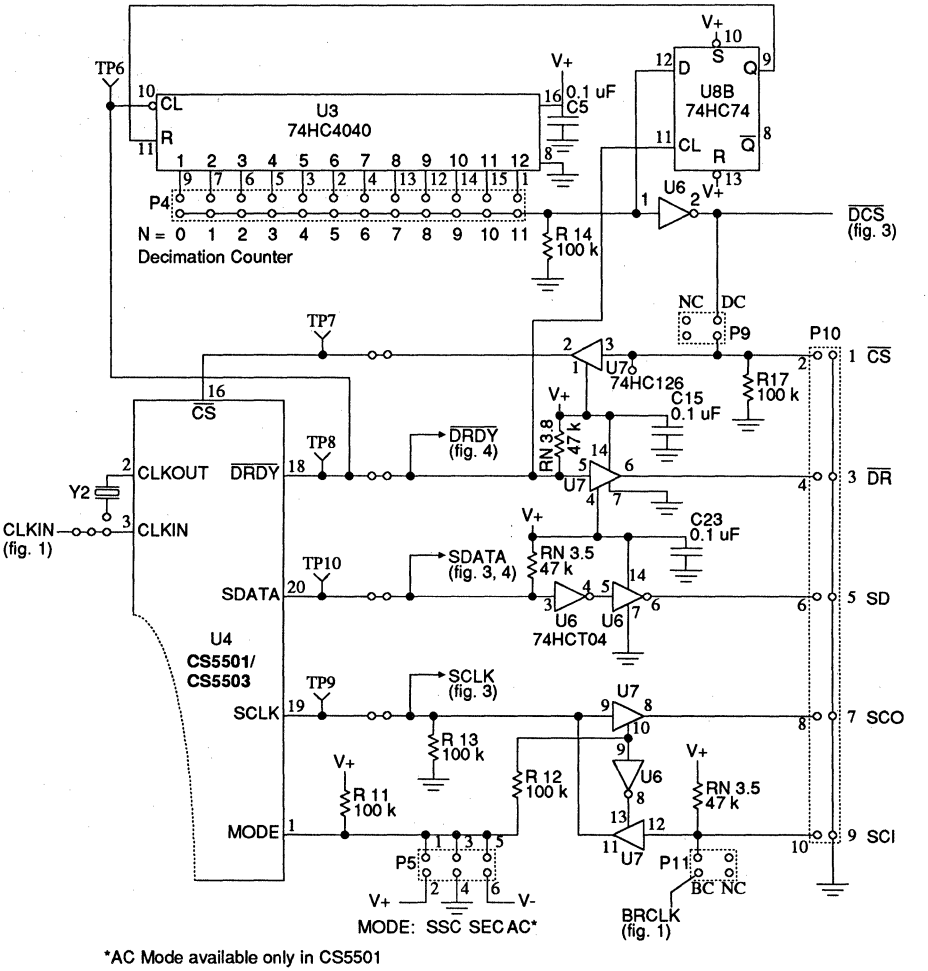
Clock Options

Several clock source options are available. These include:

1) an external clock (+5 V CMOS-Compatible);
2) an on-board 4.9152 MHz crystal oscillator with a 2^n divider (n = 1, 2, ...7);
3) a 4.096 MHz crystal.

Connector P1 allows jumper selection of either an external clock or the on-board 4.9152 MHz crystal oscillator (See figure 1 for schematic) as the clock source for the CLKIN signal on pin 3 of the CS5501/CS5503 (shown in figure 2).

If the EXT position is selected, a CMOS-compatible clock signal (5 volt supply) should be input to the BNC connector labelled CLKIN. If the INT position is selected the 4.9152 MHz oscillator output is input to counter/divider IC U2.



*AC Mode available only in CS5501

Figure 2. Decimation Counter / Microport

Table 1. Clock Generator

P-1	CLKIN Source to CS5501/CS5503
INT CLK	On-Board 4.9152 MHz OSC
EXT CLK	+5 CMOS CLKIN BNC

CLKIN Rate Selection (CLK/2^n) with INT CLK on P1 selected. CLK = 4.9152 MHz

P-2	CLKIN Rate
0	4.9152 MHz* +
1	2.4576 MHz
2	1.2288 MHz
3	614.4 kHz
4	307.2 kHz
5	153.6 kHz +
6	76.8 kHz +
7	38.4 kHz* +

* Exceeds CLKIN Specifications of CS5501.
\+ Exceeds CLKIN specifications of CS5503

In either case, the counter divides the input clock by 2^n where n = 0, 1, ...7. Any of the binary submultiples of the counter input clock can be input to the CS5501/CS5503 by jumper selection on connector P2.

The CS5501/CS5503 contains its own on-chip oscillator which needs only an external crystal to function. Ceramic resonators can be used as well although ceramic resonators and low frequency crystals will require loading capacitors for proper operation.

To test the oscillator of the CS5501/CS5503 with a crystal (Y2) a jumper wire near crystal Y2 must be opened and another jumper wire soldered into the appropriate holes provided to connect the crystal to the chip. Additional holes are provided on the board for loading capacitors.

Data Output from the CS5501/CS5503

The CS5501 has three available data output modes (The CS5503 has two available data output modes). The operating mode of the part is determined by the input voltage level to the MODE (pin 1) pin of the device. Once a mode is selected, four other pins on the device are involved in data output. The first of these is the $\overline{\text{DRDY}}$ pin (pin 18). It is an output from the chip which signals whenever a new data word is available in the internal output register of the CS5501/CS5503. Data can then be read from the register, but only when the $\overline{\text{CS}}$ pin (pin 16) is low.

When $\overline{\text{CS}}$ is low, data bits are output in serial form on the SDATA pin (pin 20). In one data output mode of the CS5501/CS5503 the chip provides an output data clock from the SCLK pin (pin 19). This output clock is synchronous with the output data and can be used to clock the data into an external register.

In the other two output data modes of the CS5501 the SCLK pin is an input for an external clock which determines the rate at which data bits appear at the SDATA output pin. In the CS5503 only one of these output data modes is available.

The signals necessary for reading data from the CS5501/CS5503 are all available on connector P10 as shown in figure 2.

Table 2. Data Output Mode

P-5	Data Output Mode
SSC	Synchronous Self-Clocking
SEC	Synchronous External-Clocking
AC*	Asynchronous Communications

* Available in CS5501 only.

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CS5501 /CS5503 Data Output Mode Selection

Connector P5 (see figure 2) allows jumper selection of any one of the three data output modes. These modes are:

1) SSC (Synchronous Self-Clocking);
2) SEC (Synchronous External Clocking);
3) AC (Asynchronous Communication). (AC mode is available only in the CS5501)

SSC (Synchronous Self-Clocking) Mode

The SSC mode is designed for interface to those microcontrollers which allow external clocking of their serial inputs. The SSC mode also allows easy connection to serial-to-parallel conversion circuitry.

In the SSC mode serial data and serial clock are output from the CS5501/CS5503 whenever the $\overline{CS}$ line is activated. As illustrated in figure 2, all of the signals are available at connector P10. If the $\overline{CS}$ signal is to be controlled remotely the jumper on P9 should be placed in the NC (No Connection) position. This removes the Decimation Counter output from controlling the $\overline{CS}$ line.

Data Output Interface: Parallel Port (for CS5501 evaluation only).

Whenever the CS5501 is operated in the SSC mode the 16-bit output data is clocked into two 8-bit shift registers. The registers have three-state parallel outputs which are available at P7 (see figure 3). A flip-flop (U8A) is used to signal the remote reading device whenever the registers are updated. The $\overline{PDR}$ (Parallel Data Ready) signal from the flip-flop is available on P7. The Q-bar output from the flip-flop locks out any further updates to the registers until their data is read and a DACK (Data ACKnowlege) signal is received from the remote device.

Activation of the $\overline{CS}$ line determines the rate at which the CS5501 will attempt to update the output shift registers. Data will be shifted into the registers only if a DACK signal has occurred since the last update.

The $\overline{CS}$ line can be controlled remotely at P10 or by the output of the Decimation Counter. If $\overline{CS}$ is controlled remotely, the Decimation divide jumper on P4 should be placed in the "0" position. This insures that the $\overline{DCS}$ signal will occur at the same rate $\overline{CS}$ is activated. The positive going edge of $\overline{DCS}$ toggles the U8A flip-flop which signals an update to the parallel port.

The parallel registers are set up to be read in 16-bit parallel fashion but can be configured to be read separately as two 8-bit bytes on an 8-bit bus. To configure the board for byte-wide reads, the byte-wide jumpers must be soldered in place. In addition, for proper "one byte at a time" address selection, a connection on the circuit board needs to be opened and a jumper wire soldered in the proper place to determine which register is to be read when A0 is a "1" and vice versa. See figure 3 for schematic details. The evaluation board component layout diagram, figure 7, indicates the location of the byte-wide jumpers and A0 address selection jumpers.

After data is read from the registers a DACK (Data Acknowledge) signal is required from the off-board controller to reset flip-flop U8A. This enables the registers to accept data input once again.

The DRB and CSB signals on connector P10 should be used to monitor and control the CS5501 output to the serial to parallel conversion registers. Be aware that an arbitrarily timed DACK signal may cause the output data registers to be enabled in the middle of an output word if the $\overline{CS}$ signal to the CS5501 is not properly sequenced. This will result in incorrect data in the output registers.

If the Decimation Counter is used to control the output of the CS5501 (Jumper on P9 in the DC position), the CSB signal on P10 can be

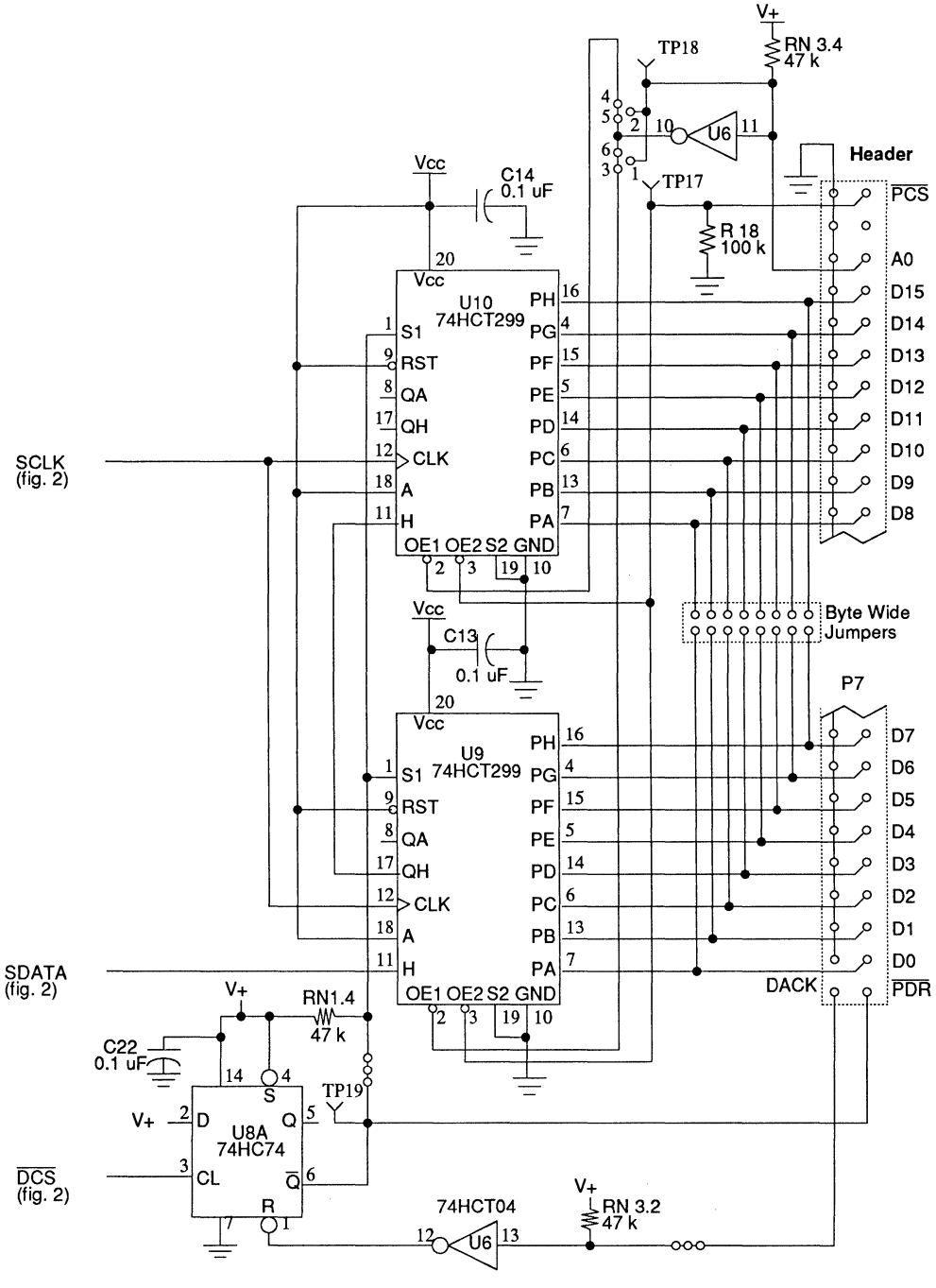

Figure 3. 16-Bit Parallel Port

monitored to signal when data into the output registers is complete ($\overline{DCS}$ returns high). The DACK signal is not needed in this mode and the lockout signal to the the S1 inputs of registers U9 and U10 may be disabled by removing the connection on the circuit board. A place is provided on the board for this purpose. A pull-up resistor is provided on the S1 inputs of the registers if the connection is opened.

SEC (Synchronous External Clocking) Mode

The SEC mode enables the CS5501/CS5503 to be directly interfaced to microcontrollers which output a clock signal to synchronously input serial data to an input port. The CS5501/CS5503 will output its serial data at the rate determined by the clock from the microcontroller.

Connector P10 allows a microcontroller access to the CS5501/CS5503 signal lines which are necessary to operate in the SEC mode.

The CSB (chip select bar $\overline{CS}$) signal allows the microcontroller to control when the CS5501/CS5503 is to output data. The $\overline{DRB}$ (data ready bar) signal on P10 indicates to the microcontroller when data from the CS5501/CS5503 is available. Clock from the microcontroller is input into SCI (serial clock input) and data output from the CS5501/CS5503 is presented to the SD (serial data) pin of the P10 connector. Note that the jumpers on connectors P9 and P11 must be in the NC (no connection) position to allow the microcontroller full control over the signals on P10.

Table 3. On-Board Baud Rate Generator

Baud Rate Clock Divider ($CLK/2^n$) with INT CLK on P1 selected. CLK = 4.9152 MHz

P-3	Baud Rate CLK Divider
8	19.2 kHz
9	9.6 kHz
10	4.8 kHz
11	2.4 kHz
12	1.2 kHz

On-Board Baud Rate Clock Input to CS5501/CS5503 SCLK Input.

P-11	SCLK Input to CS5501/CS5503
NC	No Connection
BC	Baud Clock

AC (Asynchronous Communication) Mode (for CS5501 evaluation only)

The AC mode enables the CS5501 to output data in a UART-compatible format. Data is output as two characters consisting of one start bit, eight data bits, and two stop bits each.

The output data rate can be set by a clock input to the SCI input at connector P10 (see figure 2). The jumper on P11 must be in the NC position. Alternatively an output data bit rate can be selected as a sub-multiple of the external CLKIN signal to the board or as a sub-multiple of the on-board 4.9152 MHz oscillator. Counter IC U2 divides its input by 2^n where n = 8, 9, ...12. One of these outputs can be jumper selected at connector P3 (see figure 1). For example, if the 4.9152 MHz oscillator is selected as the input to IC U2 then a 1200 baud rate clock can be selected with the jumper at n = 12. Table 3 indicates the baud rates available at connector P3 when the 4.9152 MHz oscillator is used. If the on-board baud clock is to be used, the jumper on connector P11 should be in the BC (Baud Clock) position.

Data Output Interface: RS-232 (for CS5501 evaluation only).

The RS232 port is depicted in figure 4. Sub-D connector P6 along with interface IC U11 provides the necessary circuitry to connect the CS5501 to an RS-232 input of a computer. For proper operation the AC (Asynchronous Communication) data output mode must be selected.

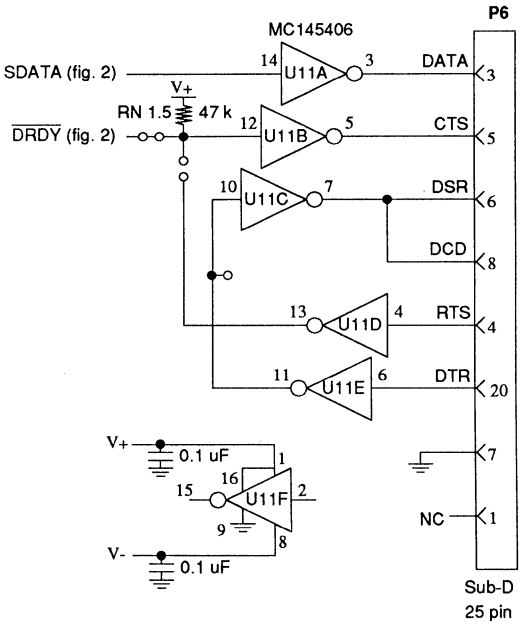

Figure 4. RS-232 Port

In addition, an appropriate baud clock needs to be input to the CS5501. See AC (Asynchronous Communication) mode mentioned earlier for an explanation of the baud rate clock generator and the data format of the output data in the AC mode.

The $\overline{DRDY}$ output from the CS5501 signals the CTS (Clear To Send) line of the RS-232 interface when data is available. The Decimation Counter can be used to determine how frequently output data is to be transmitted.

The RS-232 interface on the evaluation card is functionally adequate but it is not compliant with the EIA RS-232 standard. When the MC145406 RS-232 receiver/driver chip is operated off of ± 5 volt supplies rather than ± 6 volts (see the MC145406 data sheet for details) its driver output swing is reduced below the EIA specified limits. In practical applications this signal swing limitation only reduces the length of cable the circuit is capable of driving.

DECIMATION COUNTER

Each time a data word is available for output from the CS5501/CS5503, the $\overline{DRDY}$ line goes low, provided the output port was previously emptied. If the $\overline{DRDY}$ line is directly tied to the $\overline{CS}$ input of the CS5501/CS5503, the converter will output data every time a data word is presented to the output pin. In some applications it is desirable to reduce the output word rate. The rate can be reduced by lowering the rate at which the $\overline{CS}$ line to the chip is enabled. The CDB5501/CDB5503 evaluation board uses a counter, IC U3 for this purpose. It is known as a decimation counter (see figure 2). The outputs of the counter are available at connector P4. The counter accumulates 2^{n+1} counts (n = 0, 2, ...11) at which time the selected output enables the $\overline{CS}$ input to the CS5501/CS5503 (if the jumper in P9 is in the DC, Decimation Counter, position). The

Table 4. Decimation Counter Control

Decimation Counter Accumulates 2^{n+1} $\overline{DRDY}$ Pulses Before $\overline{CS}$ is Enabled.

P-4	2^{n+1}
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	256
8	512
9	1024
10	2048
11	4096

P-9	DC Output to $\overline{CS}$
NC	No Connection
DC	Decimation Counter

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Switch	ON	OFF
SW1-1	SC1 = 0	SC1 = 1
SW1-2	SC2 = 0	SC2 = 1
SW1-3	UNIPOLAR	BIPOLAR
SW1-4	SLEEP	AWAKE

Table 5. DIP Switch Selections

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence
⊥	0	0	Self-Cal	AGND	VREF	One Step
⊥	1	1	System Offset & System Gain	AIN	-	1st Step
⊥	0	1		-	AIN	2nd Step
⊥	1	0	System Offset	AIN	VREF	One Step

Table 6. Calibration Mode Table

"D" input to flip-flop U8B is enabled to a "1" at the same time $\overline{CS}$ goes low. When $\overline{DRDY}$ returns high flip-flop U8B is toggled and resets the counter back to zero which terminates the $\overline{CS}$ enable. The counter then accumulates counts until the selected output activates $\overline{CS}$ low once again.

DIP Switch Selections/Calibration Initiation

Several control pins of the CS5501/CS5503 can be level activated by DIP switch selection, or by microcontroller at P8, as shown in figure 5. DIP switch SW1 selections are depicted in tables 5 and 6. The CAL pushbutton is used to initiate a calibration cycle in accordance with DIP switch positions 1 and 2. The CAL pushbutton should be activated any time power is first applied to the board or any time the conversion mode (BP/$\overline{UP}$) is changed on the DIP switch. Remote control of the CAL signal is available on connector P8. Connector P8 also allows access to the DIP switch functions by a microcomputer/microcontroller. The DIP switches should be placed in the off position if off-board control of the signals on connector P8 is implemented.

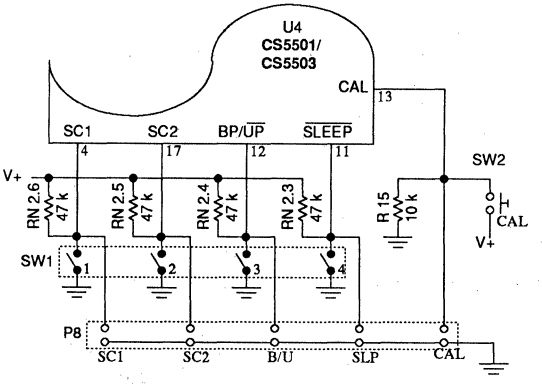


Figure 5. DIP Switch / Header Control Pin Selection

Voltage Reference

The evaluation board includes a 2.5 volt reference. Potentiometer R9 can be used to trim the reference output to a precise value.

Analog Input Range: Unipolar Mode

The value of the reference voltage sets the analog input signal range. In unipolar mode the analog input range extends from AGND to VREF. If the analog input goes above VREF the converter will output all "1's". If the input goes below AGND, the CS5501/CS5503 will output all "0's".

Analog Input Range: Bipolar Mode

The analog signal input range in the bipolar mode is set by the reference to be from +VREF to -VREF. If the input signal goes above +VREF, the CS5501/CS5503 will output all "1's". Input signals below -VREF cause the output data to be all "0's".

Analog Input: Overrange Precautions

In normal operation the value of the reference voltage determines the range of the analog input signal. Under abnormal conditions the analog signal can extend to be equal to the VA+ and VA- supply voltages. In the event the signal exceeds these supply voltages the input current should be limited to ± 10 mA as the analog input of the chip is internally diode clamped to both supplies. Excess current into the pin can damage the device. On the evaluation board, resistor R16 (see figure 6) does provide some current limiting in the event of an overrange signal which exceeds the supply voltage.

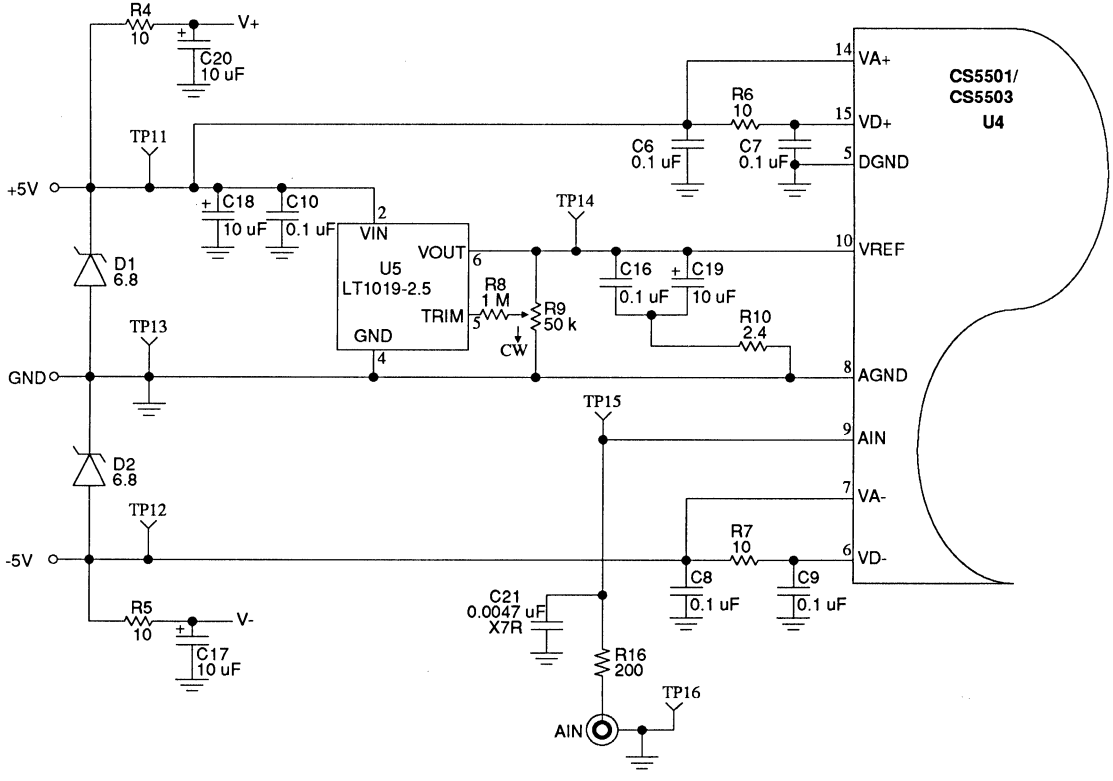


Figure 6. Voltage Reference / Analog Input

Oscilloscope Monitoring of SDATA

The output data from either the CS5501 or the CS5503 can be observed on a dual trace oscilloscope with the following hook-up. Set the evaluation board to operate in the SSC mode. Connect scope probes to TP9 (SCLK) and TP10 (SDATA). Use a third probe connected to TP8 ($\overline{\text{DRDY}}$) to provide the external trigger input to the scope (use falling edge of $\overline{\text{DRDY}}$ to trigger). With proper horizontal sweep, the SDATA output bits from the A/D converter can be observed. Note that if the input voltage to the CS5501 is adjusted to a mid-code value, the converter will remain stable on the same output code. This illustrates the low noise level of the CS5501. The CS5503 will exhibit a few LSB's of noise in its observed output in agreement with its noise specifications.

Evaluation Board Component Layout and Design Considerations

Figure 7 is a reproduction of the silkscreen component placement of the PC board.

The evaluation board includes design features to insure proper performance from the A/D converter chip. Separate analog and digital ground planes have been used on the board to insure good noise immunity to digital system noise.

Decoupling networks (R6, C7, and R7, C9 in figure 6) have been used to eliminate the possibility of noise on the power supplies on the digital section from affecting the analog part of the A/D converter chip.

The RC network (R10, C16 and C19) on the output of the LT1019-2.5 reference may not be needed in all applications. It has been included to insure the best noise performance from the reference .

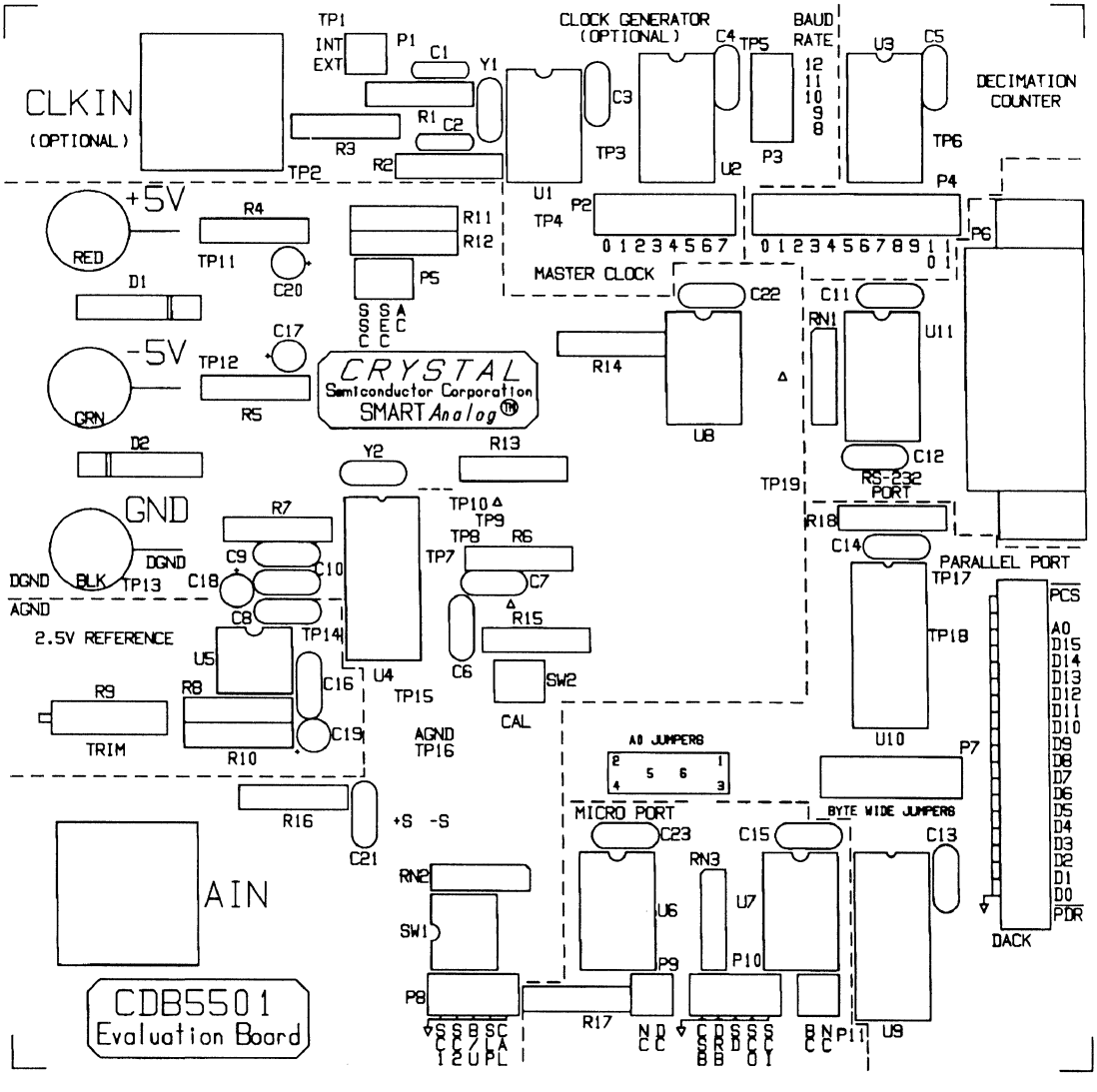


Figure 7. CDB5501/CDB5503 Component Layout

•Notes•

Semiconductor Corporation

CDB7008

CS7008 Evaluation Board

Features

- Up to 64 Different Filters On-Board
- Optional Input Antialiasing Filter
- Optional Output Smoothing Filter
- Operation from On-Board Crystal or Externally-Supplied Clock
- Supports Crystal-ICE Filter Development System

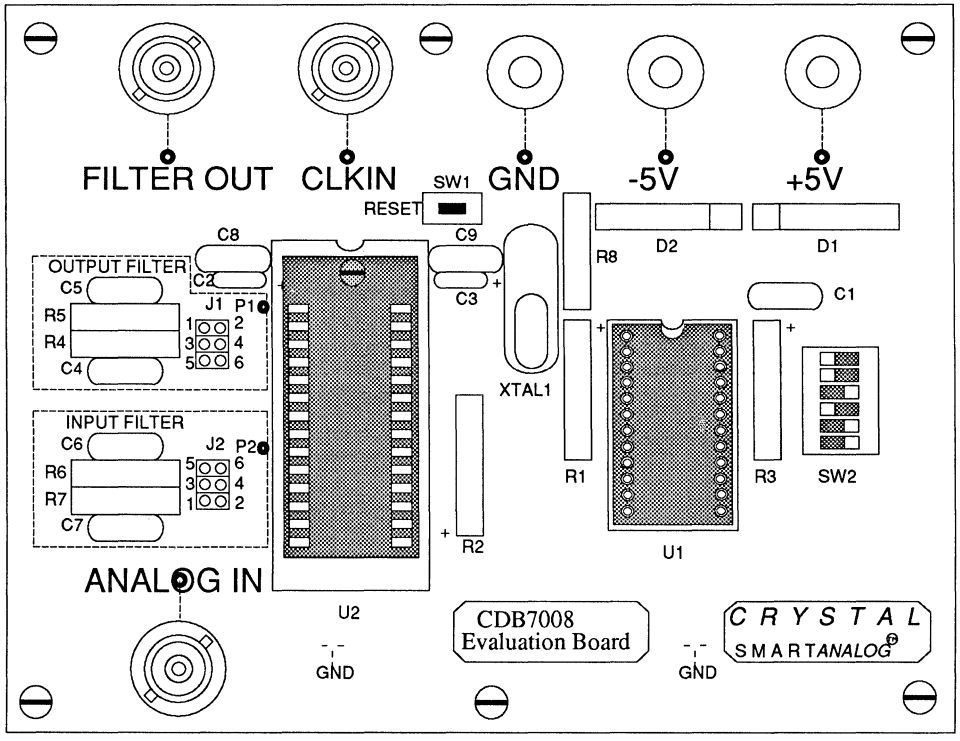
General Description

The CDB7008 allows the user to quickly verify the performance of the CS7008 Universal Filter under a wide variety of operating conditions. The on-board EPROM contains a large variety of filters that are DIP switch selectable and loaded into the CS7008 when RESET is pressed.

Jumpers on the input and output filters can be configured to provide antialiasing and smoothing, or the filters can be bypassed altogether.

ORDERING INFORMATION: CDB7008

Board Layout



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INTRODUCTION

The CDB7008 Evaluation Board is a demonstration/evaluation tool for the CS7008 Universal Filter. Up to 64 separate filter transfer functions can be stored in the board's EPROM and accessed using the DIP switches and the *RESET* switch. The EPROM contains a wide variety of filters but, by no means does it show an exhaustive set of all filters attainable by the CS7008.

The CS7008 socket is zero-insertion-force (ZIF) to allow the Crystal-ICE Probe to be inserted. With the CDB7008 and the Crystal-ICE Filter Development System, a custom filter can be designed, loaded into the ICE Probe, and evaluated immediately.

CIRCUIT DESCRIPTION

Figures 1 and 2 comprise the entire schematic for the CDB7008. The CS7008 is in the "self-loading" mode in which the part loads itself from an external EPROM. The DIP switch controls the upper six address bits of the EPROM thereby selecting the filter to be loaded. The RESET switch drives the reset pin on the CS7008 to -5 volts momentarily. The CS7008 recognizes 0.8 volts as a logic low, and will accept anything from 0.8 to the minus supply rail. This is to insure compatibility with an earlier version of the CS7008. When RESET returns high, the CS7008 starts reading coefficients out of the EPROM. Each filter is stored in 64 consecutive memory locations. The EPROM address location for a given filter is the filter number times 64. The fil-

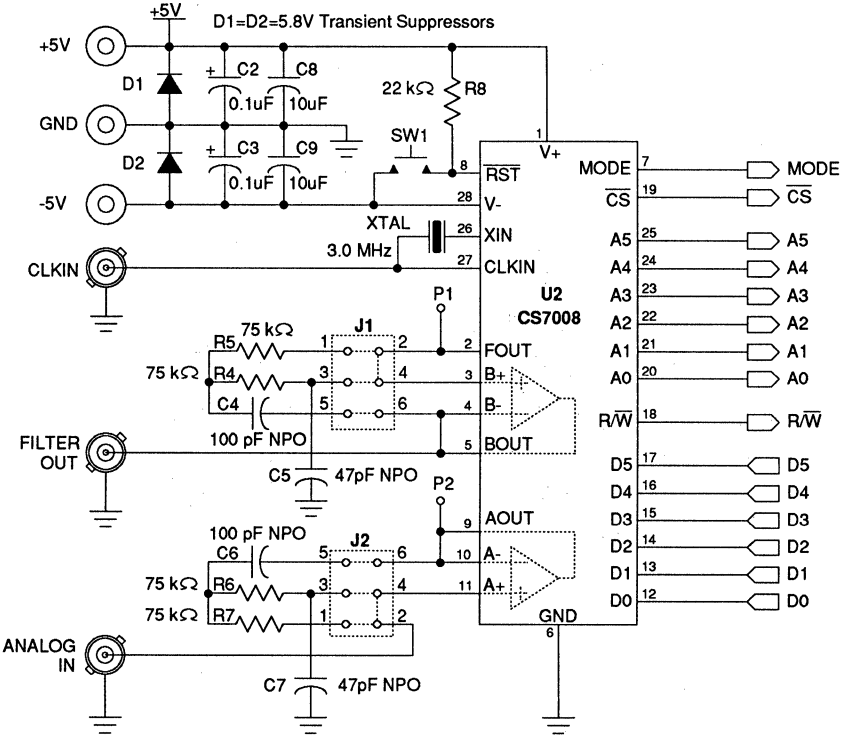


Figure 1. CS7008 Universal Filter

ter number for each filter is listed in the first column in Tables 1 and 2.

Analog In

ANALOG IN is the input for the signal to be filtered. The signal passes through op amp A on the CS7008. The op amp can be configured as an antialiasing filter or voltage follower. More information on the antialiasing filter can be found in the "Antialiasing & Smoothing Filters" section.

Filter Out

Once the signal is filtered by the CS7008, it passes through op amp B, located in the CS7008, which can be configured as a voltage follower or smoothing filter. More information on the smoothing filter can be found in the "Antialiasing & Smoothing Filters" section.

Clock In

The *CLKIN* BNC allows the use of clock frequencies other than the 3.0 MHz crystal located on the CDB7008. A CMOS-level clock on CLKIN will overdrive the crystal thereby changing the sample frequency of the EPROM filters. The new sample frequency can be calculated from the following formula,

$$f_S = \frac{f_{CLKIN}}{6 \times CLKDIV}$$

where CLKDIV is the CS7008 internal prescaler.

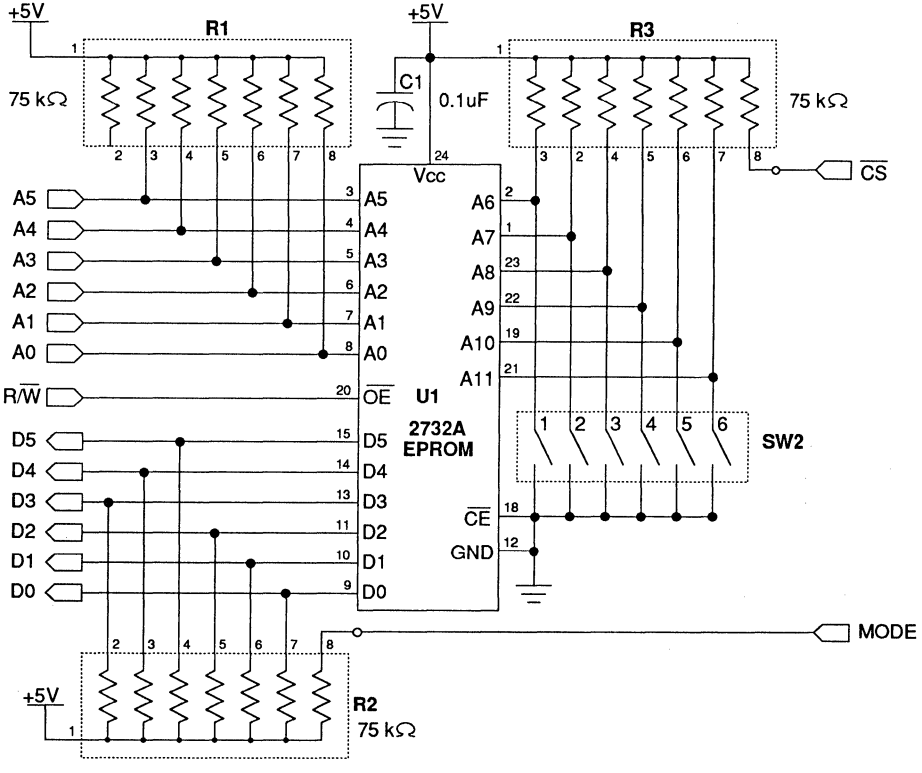


Figure 2. EPROM

Changing the sample frequency changes the filter corner frequency proportionally. Therefore, if the 3.0 MHz crystal is overdriven by a 1.5 MHz external square wave, the filter corner frequencies are halved. All filters and sample frequencies listed in Tables 1 & 2 assume the master clock is 3.0 MHz with the exception of the 60 Hz notch filter (#59) which needs an external master clock of 800 kHz. This generates a filter sample frequency of 1041.67 Hz.

Power Supplies

The CDB7008 Evaluation Board requires +5 volt and -5 volt power supplies to operate. The power supplies are connected to the appropriate banana jacks on the board. Each supply should be capable of sourcing or sinking 100 mA of current. The typical board power consumption is approximately 60 mA but will vary depending on output loading and whether the CS7008 is loading filter information or not.

EVALUATING THE CS7008

Setting Up a Demonstration System

A simple, yet effective, demonstration of the power and flexibility of the CDB7008 Evaluation Board requires only the necessary power supplies and a spectrum analyzer.

A +5 volt supply should be connected to the red banana jack marked *+5V*. A -5 volt supply should be connected to the green banana jack marked *-5V*. The ground for both supplies should be tied to the black banana jack marked *GND*. For best results, both supplies should be applied to the board simultaneously. This is easily done using a split supply with tracking outputs.

The spectrum analyzer is connected to the *ANALOG IN* and *FILTER OUT* BNC connectors. The spectrum analyzer should have a tracking generator output. This output is connected to *ANALOG IN*. *FILTER OUT* is connected to the spectrum analyzer's input. The CDB7008's output is not designed to operate with a 50 Ω or 75 Ω load, so the spectrum analyzer should be set to operate in a high impedance mode. Most analyzers can be set to 1 MΩ operation. The tracking generator should not be enabled until the evaluation board has been powered up. Since most Crystal-ICE generated filters have some gain, both the input and the output should be checked to guarantee that they are within the voltage limits specified in the CS7008 data sheet.

Selecting a filter

Filter selection is made using the on-board DIP switch and *RESET* button. As shown below, a "closed" (or "on") DIP switch is considered a 0, while an "open" (or "off") DIP switch is considered a 1. Tables 1 and 2 list all the available locations in the EPROM. The filter number is the decimal equivalent of the (binary) DIP switch setting. Momentarily depressing the *RESET* button will cause the CS7008 filter to load the selected coefficients and begin filtering to those characteristics.

```
DIP Switch:
  S6-S1: 000000 - All switches ON or CLOSED
         111111 - All switches OFF or OPEN
         110000 - S6 & S5 OPEN, S4-S1 CLOSED
```

Filter Bandwidth

The Nyquist criterion states that the usable bandwidth for a sampled data system is one half the sample frequency, termed the "base band". Any frequencies above half the sample frequency will alias into the base band. An antialiasing filter is normally used to reject any frequencies above half the sample frequency. Since the purpose of the CDB7008 evaluation board is to show a wide variety of filter configurations, the antialiasing filter starts attenuating the magnitude at approximately 21 kHz. Therefore, for lower sampling frequencies, the antialiasing filter may

not have any effect and input frequencies should be limited to one half the sample frequency. Tables 1 and 2 list the sample frequencies for all filters in the EPROM. These sample frequencies assume a master clock of 3.0 MHz.

Antialiasing & Smoothing Filters

Since the CS7008 is a switched-capacitor filter that samples the analog input, antialiasing and smoothing filters need to be addressed. The switched-capacitor filter sets the corner frequency of interest; therefore, the components used in the antialiasing and smoothing filters do not need to have tight tolerances.

As mentioned in the previous section, any input frequencies above half the sample frequency will alias into the base band. To prevent this from occurring, an antialiasing filter is used to reject frequencies above half the sample frequency. The antialiasing filter should be designed to have the most rejection at half the sample frequency. The CS7008 has an on-chip op amp (A) that the CDB7008 uses for antialiasing.

Because of the sampled nature of switched-capacitor filters, the output is a quantized or "staircase" version of the filtered input. A smoothing filter is used to smooth the output or attenuate the staircase energy. Since the CS7008 updates the output at the sample frequency, the smoothing filter should have as much attenuation as possible at the sample frequency. The CS7008 has another op amp (B) that the CDB7008 uses for smoothing.

Since the CDB7008 is designed to show a wide variety of filters, both antialiasing and smoothing real-time filters will not work with all EPROM filters. Both real-time filters are designed for unity gain with a cutoff frequency of 31 kHz. Filters that have a sample frequency of 125 kHz or greater can benefit from the on-board antialiasing and smoothing filters. The only exceptions are filters with corner frequencies near 21 kHz, as these filters will have some attenuation from the real-time filters. Tables 1 and 2 have a column labeled "AA/SM" which indicates the EPROM filters that should have the real-time filters bypassed in order to see the filter response. As shown below, a "Y" indicates the real-time filters will not affect the EPROM filter's response, while an "N" indicates the real-time filters should be bypassed because they affect the magnitude response. For sample frequencies lower than 125 kHz, the antialiasing filter is not very effective and input frequencies should be limited to half the sample frequency. Also, the smoothing filter will not attenuate much of the staircase energy for the lower sample frequencies.

AA/SM: Antialiasing/Smoothing Filters
Y - Yes, Both filters on board in use.
N - No, Both filters on board removed. (Op-amps used as voltage followers)

The antialiasing and smoothing filters are functional when jumpers are placed on J2 and J1 between pins 1 and 2, pins 3 and 4, and pins 5 and 6 (3 jumpers for each filter). The filters may be bypassed by placing one jumper between pins 2 and 4 which places the respective op amp in a voltage-follower configuration. On the CDB7008 the antialiasing filter is labeled "INPUT FILTER" and the smoothing filter is labeled "OUTPUT FILTER".

Design Methodology

Both the antialiasing and smoothing filters are Sallen & Key unity-gain low-pass configurations as shown in Figure 3. For the CDB7008 design, R1 = R2 = R. The following set of equations are valid for unity gain and equivalent resistances,

$$\omega_n = \frac{1}{R\sqrt{C_1C_2}}$$

$$Q = \sqrt{\frac{C_1}{4C_2}}$$

where ω_n is the natural frequency. On the CDB7008 evaluation board, C4 and C6 are equivalent to C_1 in Figure 3, and C5 and C7 are equivalent to C_2 in Figure 3. The board values produce a natural frequency ω_n of approximately 194,487 radians or 31 kHz but the magnitude is affected from about 21 kHz.

The antialiasing filter does not have to be unity gain. If the input voltage is less than the CS7008 maximum input voltage swing, as specified in the data sheet, the antialiasing filter can be designed to gain up the input thereby maximizing the signal-to-noise ratio.

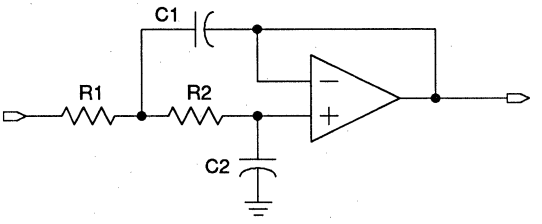


Figure 3. Sallen & Key Unity-Gain Filter

AVAILABLE FILTERS

The CDB7008 utilizes a 2732 4k×8 EPROM which can hold a maximum of 64 different filters. Tables 1 and 2 list all possible filter locations.

Crystal-ICE Filters

Filters in this category were created using the filter synthesis portion of the Crystal-ICE Filter Development System. This system allows you to create *and evaluate* filters in a matter of minutes. The first 32 filters in the CDB7008 evaluation board were created using Crystal-ICE. These filters are spread across the 0-20 kHz band and divided among four filter types: low-pass, high-pass, band-pass, and band-stop. Figure 6 illustrates the templates for all four filter types. The cutoff tolerance, TOLC, along with the appropriate frequency specifies the pass-band edge. The rejection tolerance, TOLR, along with the appropriate frequency specifies the stop-band edge. TOLC and TOLR specify the magnitude and are normalized to one. The formula to convert the normalized values to dB is:

$$TOL_{dB} = 20\,LOG_{10}(TOL)$$

Within each filter type are four implementations. Butterworth is maximally flat in the pass band and stop band, but has a slow transition band between the other two bands. Since no ripple exists in the pass band, TOLC is chosen to be the -3 dB (0.7071) cutoff point. By positioning the poles and zeros to create ripple in the pass or stop band, a steeper transition band can be obtained. Chebyshev I has ripple in the pass band whereas Chebyshev II has ripple in the stop band. Besides defining the pass-band edge, TOLC for Chebyshev I also defines the amount of ripple in the pass band; therefore, higher values than 0.7071 are used to reduce the ripple. For Chebyshev II, TOLR defines the stop-band ripple. Elliptic filters use ripple in both the pass and stop band to get the fastest transition band, so both TOLC and TOLR define ripple magnitudes.

Tweaked ICE Filters

As in the previous section, these filters were created with the synthesis portion of the Crystal-ICE Filter Development System, except that these were modified at the transfer function level.

The first two filters in this category have had their gain adjusted to 0 dB. When designing filters, gain is sometimes produced from capacitor rounding which causes inexact placement of poles and zeros. Most Crystal-ICE synthesized filters contain a little gain, whether positive or negative. This is a design phenomenon and can be corrected by removing gain at the transfer function level. Scaling down the numerator of the Z-domain transfer functions reduces the gain.

The next two filters have actually had gain added at the transfer function level. This is done in the

same way that gain was removed in the previous filters, except that the numerator's are scaled up.

In the band-stop filter #26, the lower pass band has peaking and both pass-band magnitudes are not equal. Reducing the gain alone would not solve this problem. Filter #36 corrects this problem by moving the zeros closer to the lower pass band thereby reducing the peaking and equalizing both pass-band magnitudes. Then the numerators are scaled down to remove excess gain.

The last two filters in this category show unique filters that can be created with the CS7008 to fit specialized applications.. The first is a fourth-order synchronously-tuned notch embedded in a fourth-order Chebyshev I low-pass filter as shown in Figure 4. The second is a double notch filter created by cascading two fourth-order elliptic band-stop filters with notch frequencies of 1 kHz and 1.5 kHz. This filter is shown in Figure 5.

Other Filters

This section covers filters that do not fit in the above category. They are created by taking poles and zeros in the S-domain, generating S-domain transfer functions, and converting those to Z-domain transfer functions using the bilinear transformation. Then the Z-domain transfer functions are entered into Crystal-ICE which calculates capacitor values and downloads these filter functions to the ICE Probe for testing.

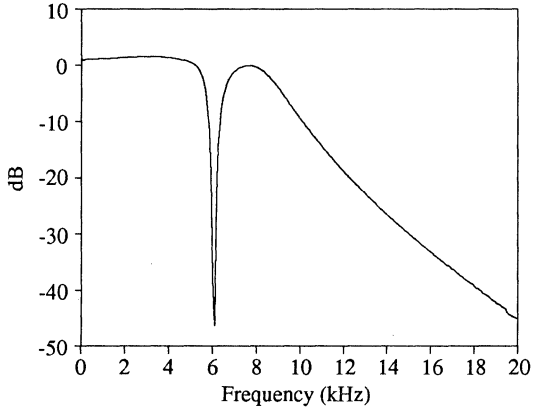


Figure 4. Low-Pass with Embedded Notch

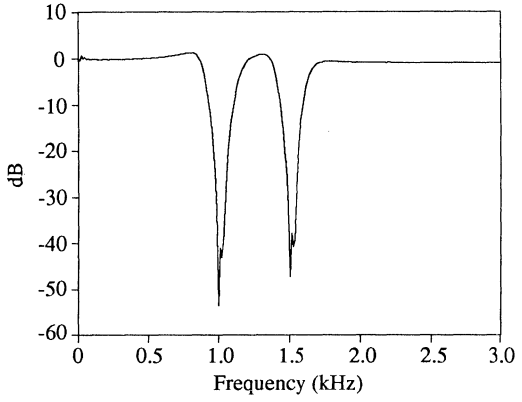


Figure 5. Double Notch

Although a Butterworth filter is optimized for a maximally flat magnitude, the Bessel filter is optimized for linear phase or flat group delay. The trade-off is a slower transition band than the Butterworth. The CDB7008 contains four Bessel filters (#40-43), three low-pass and one high-pass.

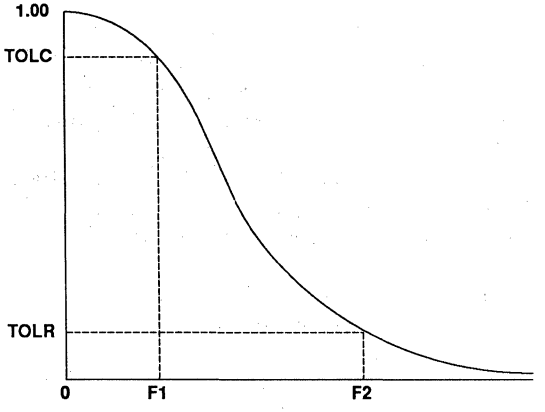
Crystal-ICE synthesized filters spread the poles through the pass band and, in some cases, spread the zeros through the stop band. These filters are termed "stagger-tuned" filters. Very narrow band-pass filters are not ideally suited to spreading the poles throughout the pass band. Narrow band-pass filters are more easily attainable with "synchronously-tuned" filters. These filters have all their poles and zeros at the same frequencies and control the "narrowness" of the pass band with the Q of each biquad. The evaluation board contains two "synchronously-tuned" band-pass filters (#46 & 47).

At times the phase of a filter must be modified without affecting the magnitude response. All-pass filters pass all frequencies (up to half the sample frequency for sampled-data filters such as the CS7008) with a phase shift at the pole frequency, and the group delay controlled by Q. The CDB7008 contains two all-pass filters (#48 & 49), one a second-order and the other a fourth-order.

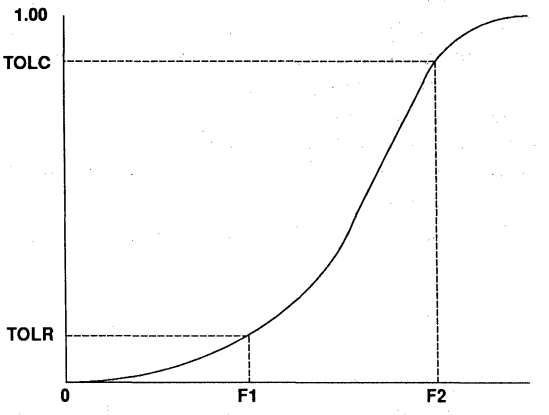
The last two filters in this category (#52 & 53) are telecommunications filters. The 1010 Hz notch filter is a synchronously-tuned 8th-order band-stop and the C-Message filter is a non-classical filter response.

Data Sheet Filters

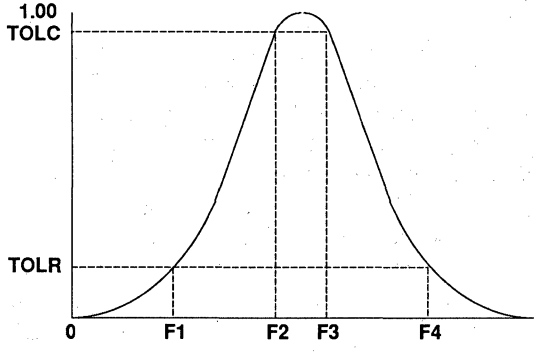
Since the CS7008 is a universal filter, it cannot be tested under every possible filter configuration. To provide some indication of filter performance,



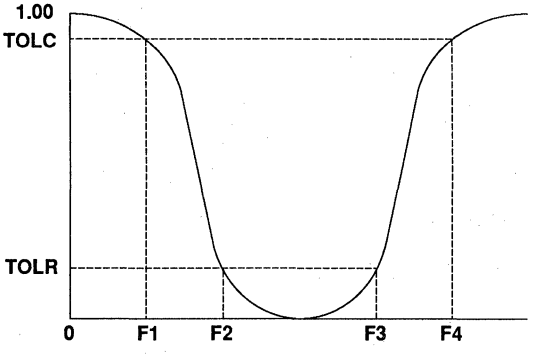
Low-Pass Filter Template



High-Pass Filter Template



Band-Pass Filter Template



Band-Stop Filter Template

Figure 6. Crystal-ICE Filter Templates

#	DIP Switch S6 - S1	Type	Impl.	TOLC	TOLR	F1	F2	F3	F4	Sample Frequency	AA/ SM
0	000000	LP	EL	0.99	0.001	400	600			3,906.25	Y
1	000001	LP	C1	0.99	0.001	700	1,200			7,812.5	Y
2	000010	LP	C2	0.7071	0.0001	1,000	1,900			31,250	Y
3	000011	LP	BW	0.7071	0.01	2,000	4,000			31,250	Y
4	000100	LP	C1	0.99	0.01	5,000	7,500			62,500	Y
5	000101	LP	EL	0.9886	0.003	9,000	11,000			125,000	Y
6	000110	LP	BW	0.7071	0.01	12,000	22,000			250,000	Y
7	000111	LP	C2	0.7071	0.0005	16,000	28,000			250,000	N
8	001000	HP	EL	0.9943	0.0001	60	110			3,906.25	Y
9	001001	HP	BW	0.7071	0.001	300	800			31,250	Y
10	001010	HP	C1	0.9772	0.001	1,100	2,000			31,250	Y
11	001011	HP	C2	0.7071	0.0001	2,000	4,000			62,500	Y
12	001100	HP	C1	0.99	0.01	4,000	7,000			125,000	Y
13	001101	HP	EL	0.99	0.0001	7,000	10,000			125,000	N
14	001110	HP	BW	0.7071	0.01	8,000	15,000			250,000	N
15	001111	HP	C2	0.7071	0.0001	9,000	17,000			250,000	N
16	010000	BP	BW	0.7071	0.0005	50	110	140	270	3,906.25	Y
17	010001	BP	C1	0.9772	0.003	160	300	500	900	7,812.5	Y
18	010010	BP	C2	0.7071	0.001	200	600	2,200	5,300	31,250	Y
19	010011	BP	EL	0.99	0.0001	1,000	2,500	4,000	10,000	62,500	Y
20	010100	BP	BW	0.7071	0.002	1,500	4,000	7,000	18,500	62,500	Y
21	010101	BP	C2	0.7071	0.0002	3,500	7,000	10,000	20,000	125,000	Y
22	010110	BP	C1	0.99	0.0008	4,000	10,000	16,000	40,000	250,000	N
23	010111	BP	EL	0.99	0.001	12,000	16,000	19,000	25,500	250,000	N
24	011000	BS	C2	0.7071	0.0003	140	210	230	320	3,906.25	Y
25	011001	BS	EL	0.9772	0.001	480	550	600	720	15,625	Y
26	011010	BS	BW	0.7071	0.001	900	990	1,010	1,100	31,250	Y
27	011011	BS	C1	0.9441	0.001	2,100	2,500	2,700	3,200	62,500	Y
28	011100	BS	C2	0.7071	0.0003	5,300	5,800	6,000	6,500	125,000	Y
29	011101	BS	BW	0.7071	0.001	7,000	10,000	11,000	16,000	125,000	N
30	011110	BS	C1	0.9441	0.001	12,100	14,000	14,500	17,000	250,000	N
31	011111	BS	EL	0.99	0.001	15,500	18,000	20,000	23,500	250,000	N

Filter Types:
- LP - Low-Pass
- HP - High-Pass
- BP - Band-Pass
- BS - Band-Stop

Filter Implementations:
- BW - Butterworth: Maximally flat
- C1 - Chebyshev I: Ripple in pass-band, steeper transition band than BW
- C2 - Chebyshev II: Ripple in stop-band, steeper transition band than BW
- EL - Elliptic (Cauer): Ripple in both bands, steepest transition band

Table 1. Crystal-ICE Generated Filters

two filters (#54 & 55) are chosen for production testing of the specifications in the CS7008 data sheet.

The last four filters are mentioned in the "Typical CS7008 Filters" section of the CS7008 data sheet.

The last of these filters, the 60 Hz Butterworth notch (#59), requires an external clock of 800 kHz to function properly.

#	DIP Switch S6 - S1	Filter Name	Description	Sample Frequency	AA/ SM
32	100000	#2 Gain Modified	Low-Pass Chebyshev II, Gain = 0 dB	31,250	Y
33	100001	#16 Gain Modified	Band-Pass Butterworth, Gain = 0 dB	3,906.25	Y
34	100010	#12 Gain Modified	High-Pass Chebyshev I, Gain = 1.5 dB	125,000	Y
35	100011	#21 Gain Modified	Band-Pass Chebyshev II, Gain = 2 dB	125,000	Y
36	100100	#26 Gain Modified	Band-Stop Butterworth, 0's and Gain modified	31,250	Y
37	100101				
38	100110	Low-Pass & Notch	Chebyshev I, fc = 8.8 kHz with 6 kHz notch	125,000	Y
39	100111	Double Notch	Two Elliptic 4th order notches, 1 & 1.5 kHz	31,250	Y
40	101000	1.5 kHz Low-Pass	Bessel response	31,250	Y
41	101001	7 kHz Low-Pass	Bessel response	250,000	Y
42	101010	12 kHz Low-Pass	Bessel response	250,000	Y
43	101011	8 kHz High-Pass	Bessel response	125,000	N
44	101100				
45	101101				
46	101110	2.4 kHz Band-Pass	Synchronously Tuned, each Q = 5	62,500	Y
47	101111	8 kHz Band-Pass	Synchronously Tuned, each Q = 8	250,000	Y
48	110000	2nd Order All-Pass	Fo = 3.5 kHz , Q = 0.7071	62,500	Y
49	110001	4th Order All-Pass	Fo = 15kHz, Q = 3 and Fo = 19 kHz, Q = 5	250,000	N
50	110010				
51	110011				
52	110100	1010 Hz Notch	Telecommunications filter	31,250	Y
53	110101	C-Message	Telecommunications filter	31,250	Y
54	110110	Prod. Low-Pass	Production test filter	250,000	Y
55	110111	Prod. Band-Pass	Production test filter	250,000	Y
56	111000	20 kHz Low-Pass	"Typical" filter in CS7008 Data Sheet	250,000	N
57	111001	5 kHz High-Pass	"Typical" filter in CS7008 Data Sheet	250,000	Y
58	111010	400 Hz Band-Pass	"Typical" filter in CS7008 Data Sheet	7,812.5	Y
59	111011	60 Hz Notch	"Typical" filter in CS7008 Data Sheet (Note 1.)	1,041.67	Y
60	111100	30 kHz Low-Pass	Elliptic response	250,000	N
61	111101	45 kHz High-Pass	Butterworth response	250,000	N
62	111110	60 kHz Band Pass	Chebyshev II response	250,000	N
63	111111				

Note 1. To get this filter CLKIN (master clock) must be driven with an 800 kHz square wave.

Table 2. Other Filters

Low Frequency Filters

The CS7008 is capable of filter corner frequencies as low as 0.1 Hz. With the on-board 3.0 MHz crystal, the lowest sample frequency is 3,906 Hz which generates too high an oversampling ratio for very low corner frequencies. The only low frequency filter directly implemented in the evaluation board is the 60 Hz notch filter (#59) which requires an external clock of 800 kHz.

Since all the filters scale with sample frequency, an external clock can overdrive the crystal, and lower corner frequencies can be obtained by lowering the external clock frequency below 3.0 MHz. As an example, consider filter number 2, a low-pass Chebyshev II with a corner frequency of 1 kHz. If the crystal is overdriven by an external clock frequency of 30 kHz, which is 100 times less than 3.0 MHz, the sample frequency would scale down by 100 to 312.5 Hz and the corner frequency would drop from 1000 Hz to 10 Hz.

High Frequency Filters

Similar to the low frequency filters, an external clock can be used to create higher frequency filters. The only restriction is that the sample frequency cannot exceed 250 kHz as specified in the CS7008 data sheet. Therefore, filters in the EPROM that already use a sample frequency of 250 kHz cannot be scaled higher.

The CDB7008 also contains three high-frequency filters (#60-62) that use a sample frequency of 250 kHz. The on-board antialiasing and smoothing filters *must* be bypassed for these filters to function properly.

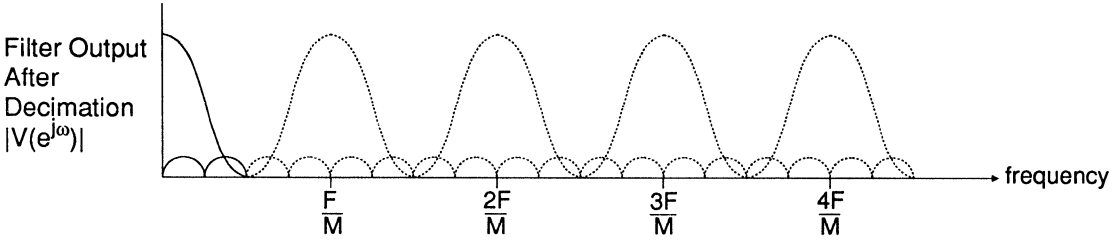
Since these filters have a low oversampling ratio, antialiasing and smoothing filters in a real system may need to be greater than second order. In these cases the on-chip op amps can be combined with external op amps to create higher order antialiasing and smoothing filters.

• Notes •

CONTENTS

Antialiasing Considerations for the CS5317

by
Nav Sooch



APPLICATION NOTE

ANTIALIASING CONSIDERATIONS FOR THE CS5317

Introduction:

Delta-Sigma A/D converters perform a rough A/D conversion at a high rate and digitally filter the output to obtain an accurate low frequency conversion. Since the input is initially sampled at a high rate and followed by a digital filter, the majority of antialias filtering is performed by the digital filter. However, aliasing problems due to decimation still remain. These aliasing issues can be addressed by analog and/or digital filters. In general, the antialias filtering requirements of the CS5317 are simpler than those of conventional A/D converters. This application note describes the aliasing properties of the CS5317 and provides examples of filtering options.

Note: Antialiasing requirements are a function of the desired signal bandwidth and out-of-band energy. For simplicity, a clock rate of 4.096 MHz has been chosen for this note. If the actual clock rate is different, all the frequency values in this

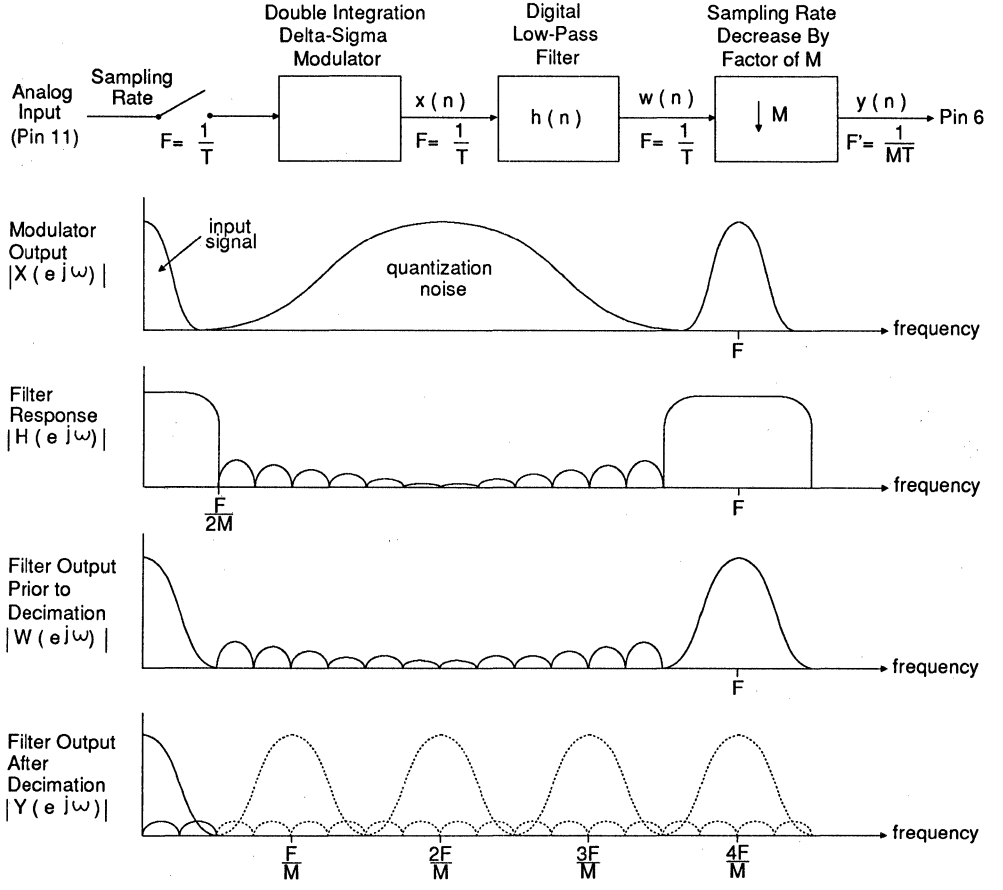


Figure 1. Block Diagram and Typical Spectra for Sampling Rate Reduction by a Factor of M

note should be scaled by (actual clock rate)/(4.096 MHz).

Initial Sampling:

The initial sampling of the analog input is done at 2.048 MHz. There is no internal filtering of frequencies at (2.048)n MHz + 8 kHz (where n = 1, 2, 3...). If signals in this band exist, an analog filter must attenuate them. Typically, a single-pole RC filter will suffice (see CS5317 data sheet).

Decimation:

The process of digitally converting the sampling rate of a signal from a given rate F to a lower rate F' is called decimation. The decimation process is shown graphically in the frequency domain in Figure 1. The delta-sigma modulator output, x(n), sampled at frequency F is fed into a low-pass filter with response h(n). The output of this filter is decimated by a factor M to a new sampling rate of F' = F/M.

The analog modulator on the CS5317 is followed by a digital filter that has the following frequency response:

$$\text{Mag} \mid H(e^{j\omega}) \mid = \left| \frac{\sin (N\pi f/f_S)}{N \sin (\pi f/f_S)} \right|^3 \qquad (1)$$

$$\text{where } N = 128 \text{ and } f_S = \frac{CLKIN}{2}$$

The digital filter's frequency response is plotted in Figure 2. The output rate of this digital filter is internally decimated to 16 kHz. Decimating to 16kHz implies that the output of the filter is effectively resampled at 16 kHz. Therefore, signals at multiples of 16 kHz will alias into the baseband after being attenuated according to the filter response defined in Equation 1. For example, an input tone at 28 kHz will be attenuated by 53.4 dB and will appear at 4 kHz in the output spectrum (2 (16 kHz) - 28 KHz = 4 kHz).

Table 1 shows the antialiasing rejection at a few key frequencies.

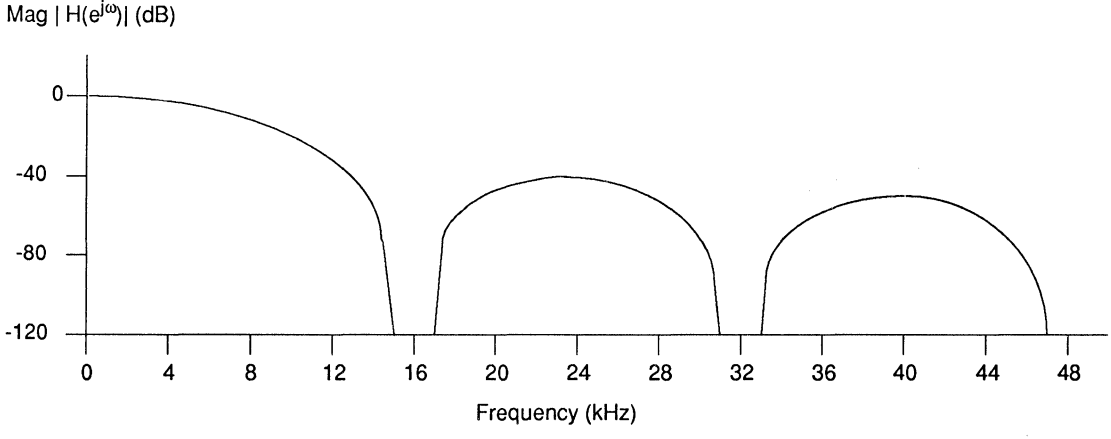


Figure 2. Low-Pass Filter Response

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Input Frequency (kHz)	Output Frequency (kHz)	Attenuation (dB)
10	6	19.6
12	4	31.4
14	2	51.4
18	2	57.9
20	4	44.7
24	8	40.4
28	4	53.4
34	2	74.5

Table 1. Antialiasing Rejection at Key Frequencies

Note that the worst case rejection into the 0-4 kHz band is 31.4 dB for input signals at 12 kHz. Also note that very little rejection is provided for signals that alias into the 4-8 kHz band.

ANTIALIASING STRATEGIES

One of the following three cases and associated antialiasing strategies should apply to any CS5317 application:

Case 1 -No Out of Band Energy

4 kHz Bandwidth:

If there is no incoming energy past 4 kHz, the digital output can be decimated to 8 kHz by simply dropping every other output sample. Incoming signals past 4 kHz can always be filtered by an analog filter prior to A/D conversion. Since the digital output is not filtered prior to decimation, the dynamic range will be 84 dB (see Data Sheet).

8 kHz Bandwidth:

When signals from 0 to 8 kHz are of interest, the incoming signals must be band-limited to 8 kHz. Since the CS5317 output rate is already at the Nyquist rate of 16 kHz, no further decimation is necessary. The dynamic range will be 84 dB.

Case 2 -Limited Out of Band Energy

Assume that the input signal has the following spectrum:

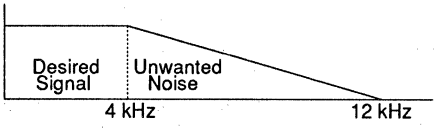


Figure 3. Limited Out of Band Energy

Two filtering methods are possible to prevent aliasing:

Analog Filter on Input

An analog filter can be used to remove the energy in the 4-12 kHz band prior to A/D conversion. The digital output of the CS5317 can be decimated to 8 kHz. If decimation is done without digital filtering, the dynamic range will be 84 dB (see Data Sheet).

Digital Filter on Output

Unwanted noise from 8 to 12 kHz will alias into the 4-8 kHz band after internal decimation in the CS5317. A digital filter can be used at the output of the CS5317 to remove energy in the 4-8 kHz band. The output of this external digital filter can be decimated to 8 kHz. In this case, the dynamic range will be 90 dB (see Data Sheet).

Case 3 -Lots of Out of Band Energy

Assume that the input signal has the following spectrum:

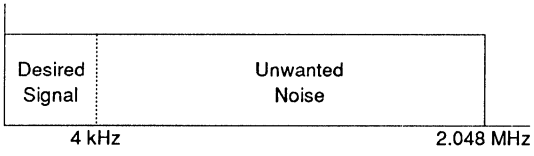


Figure 4. Lots of Out of Band Energy

The following filtering possibilities exist:

Analog Filter

An analog filter can be used to remove energy past 4 kHz. The digital output of the CS5317 can be decimated (drop every other sample) to 8 kHz. If decimation is done without a post digital filter, then the dynamic range will be 84 dB (see Data Sheet).

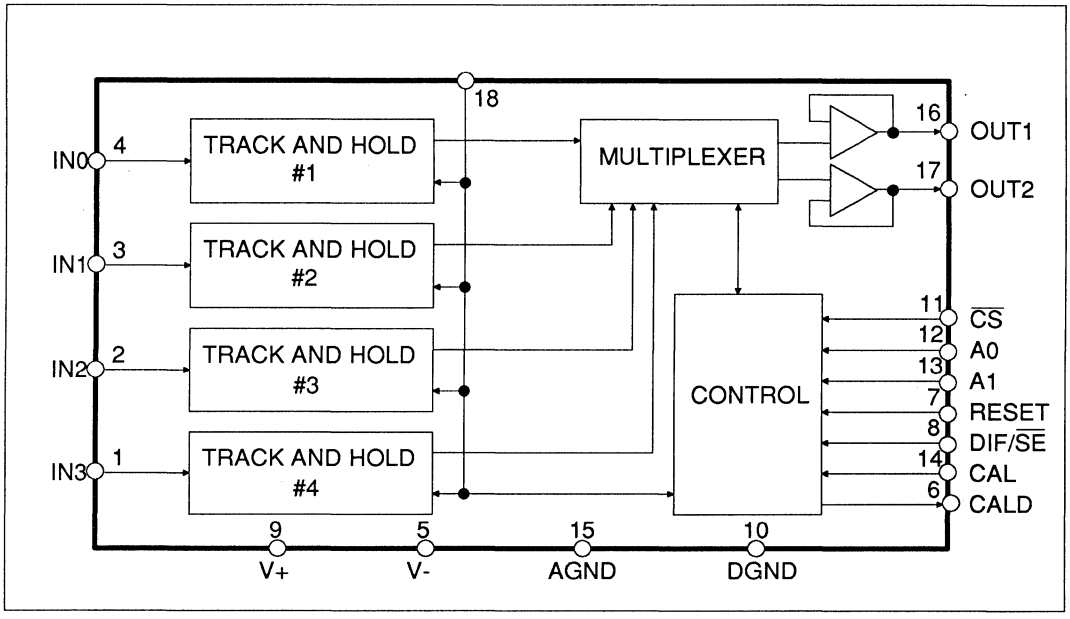
Analog and Digital filters

A combination of analog and digital filters can be used. The digital filter can remove signals that alias into the 4-8 kHz band. As seen from Table 1, the frequencies that alias into the 4-8 kHz band are 8-12 kHz, 20-28 kHz, 36-44 kHz, and so on. The internal decimation filter on the CS5317 provides a minimum rejection of 31.4 dB for components in the 12-20 kHz and 28-36 kHz bands. Note that the requirements on this analog filter are significantly relaxed compared to the filter in the analog alone option (i.e. the transition band for this analog filter is much wider). Since a digital filter is used to remove energy in the 4-8 kHz band, the dynamic range will be 90 dB (see Data Sheet).

• Notes •

Suggested Grounding and Supply Arrangements for the CS31412

by
Steven Harris



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APPLICATION NOTE

CS31412 Quad Track and Hold Amplifier Recommended Grounding and Supply Arrangements

The CS31412 connections fall into 6 classes: analog inputs, analog outputs, non time-critical digital inputs, digital outputs, power supplies, and the hold signal. The fundamental guideline to follow is to think carefully about the currents flowing due to the above 6 classes of signals, and keep them separate.

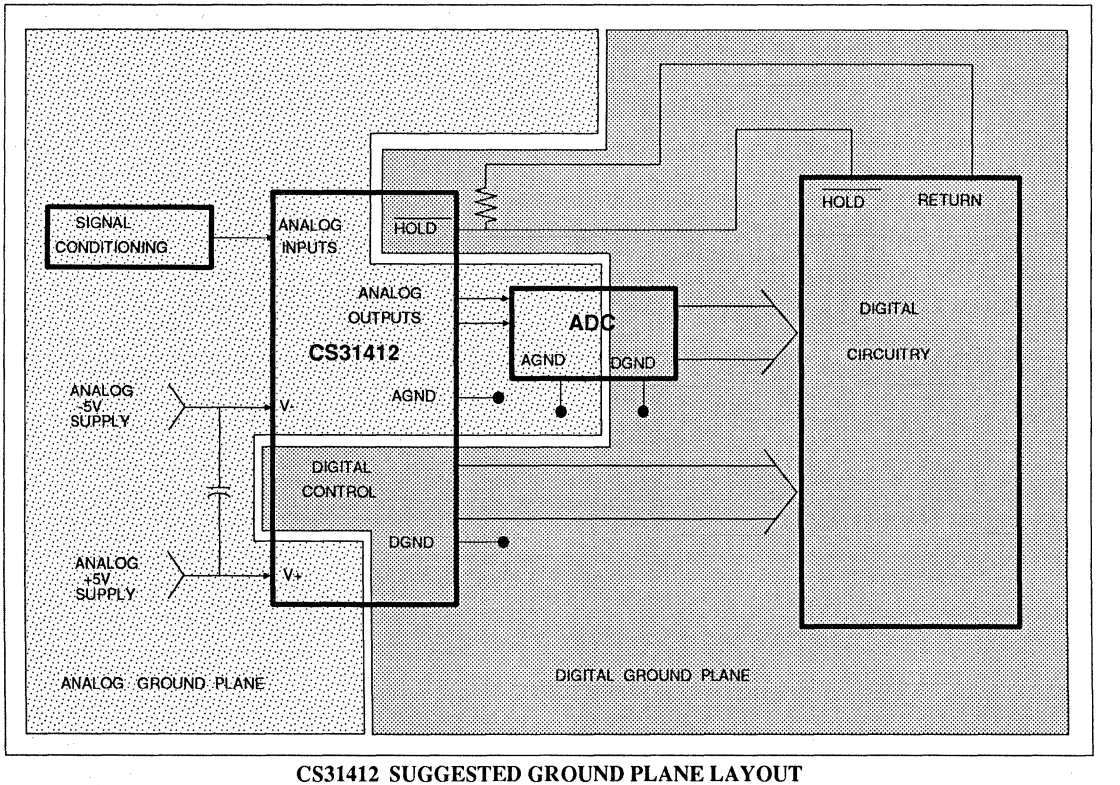
A good layout scheme will:

a) Keep digital signal noise from the analog output.

b) Obtain the best possible accuracy.
c) Minimize the aperture jitter.
d) Minimize power supply noise affecting the output.

The following guidelines will help to achieve these goals:

1) Have separate analog and digital grounds. Only join these grounds together at one place, typically either at the power supply or at the ADC.
2) Decouple the part with a 10µF/0.1µF capacitor combination connected between V+ and V-, as near to the part pins as possible
3) Group all of the non time-critical digital signal traces together and keep them separated from the analog signals. Also use digital ground traces to



CS31412 SUGGESTED GROUND PLANE LAYOUT

isolate this group of traces from the other signals.

4) The high input impedance of the part on the analog input pins results in a very small input current. Nevertheless, if termination resistors are used, the return currents for each resistor should be kept separate to avoid introducing crosstalk

5) Connect the loads to the analog outputs such that the return currents do not flow in any input related ground leads.

6) Typically the hold signal will be terminated to ground near to the CS31412. This gives a clean edge and also minimizes the absolute amplitude of the hold signal. Both the hold signal and its return current trace should be brought back to the pins of the part generating the signal.

The figure shows a possible ground plane layout, concentrating on the area around the CS31412.

Notes:

1) The CS31412 is grossly out of scale. It is enlarged to highlight the grounding around the sample hold.

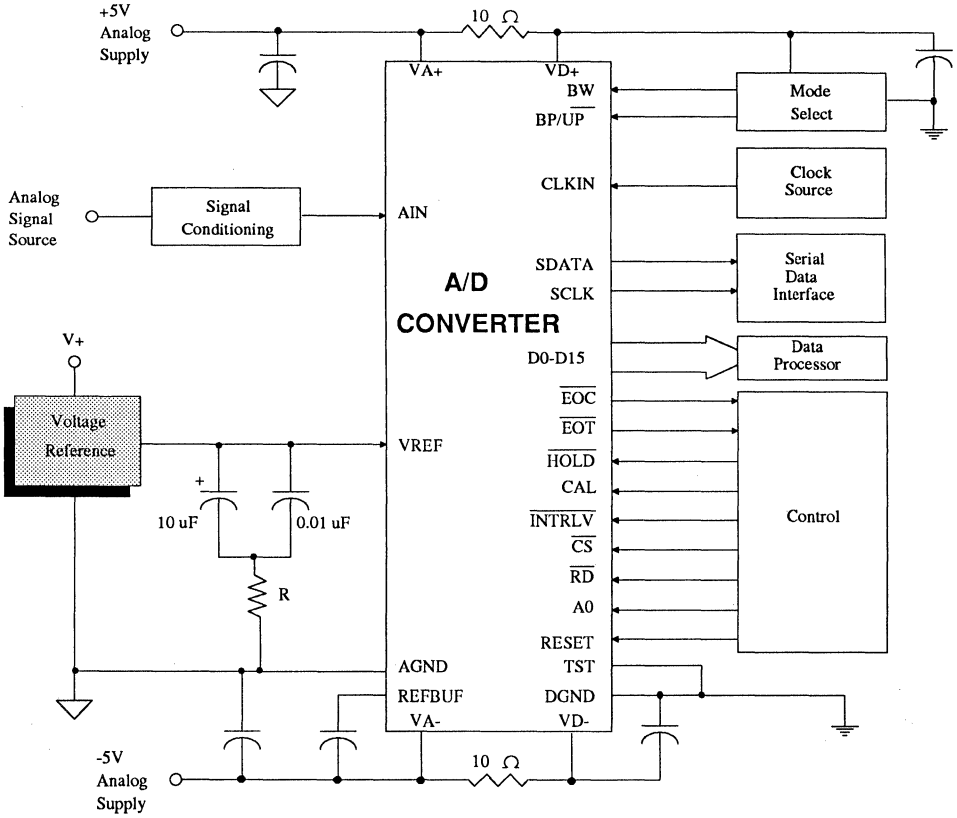
2) The Analog and Digital ground planes should be joined together at the ADC or at the power supplies.

• Notes •

Application Note

Voltage References for the CS5012 / CS5014 / CS5016 / CS5101/ CS5102 / CS5126 Series of A/D converters

by
Bruce Del Signore & Steven Harris



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INTRODUCTION

This application note discusses voltage references for use with Crystal Semiconductor's successive approximation series of A/D converters. Reference design considerations, a design example and suggested reference circuits are explained in detail.

Voltage references provide accurate voltages for use in data acquisition systems in order to establish a basis for conversion. In a data acquisition system, the value of the reference sets the gain of the A/D stage since the digital output corresponds to the ratio of the analog input signal to the reference voltage.

In static applications, information is contained in the signal amplitude, therefore the absolute value of the reference voltage is important. In many signal processing applications, information is contained in the frequency and phase of the signal. Here, absolute value is not as important as the stability of the reference voltage during conversion.

Zener-diode Reference

There are two major varieties of voltage references. The first is the zener-diode based reference which uses a reverse-biased zener diode operated in its breakdown region. Most reference zeners breakdown at voltages between 6.0 and 7.0V, which limits the minimum supply voltage necessary for operation. When the diode is supplied with a constant current, it has a constant voltage drop. Zener references use a zener diode and an integrated feedback amplifier which provides constant current, gain, and buffering for the zener diode.

Zener diodes exhibit two types of breakdown. The first is zener breakdown which has a negative temperature coefficient and is dominant at low current levels. The second, avalanche breakdown, occurs at higher current levels and has a positive temperature coefficient. At some specific current level, these two effects cancel each other and the temperature coefficient of the zener breakdown voltage is zero. As the ambient temperature changes, one of the breakdown mechanisms becomes dominant and the the reverse-biased diode voltage will exhibit a temperature coefficient.

Bandgap Reference

The second major type of reference is the bandgap reference. This reference uses the base-emitter voltage (V_{be}) of a bipolar transistor as a basis for operation. The V_{be} has a negative temperature coefficient (-2mV/°C). This negative temperature coefficient is balanced by a voltage with a positive temperature coefficient of the same magnitude. This voltage is usually obtained by using the difference of two V_{be}'s of transistors operating at different current densities. When both voltages are scaled and summed together, the result is a voltage which is less sensitive to temperature. The headroom required for bias and support circuitry is only a few volts over the output voltage.

Reference Specifications

Voltage references have six important specifications. These are absolute accuracy, temperature coefficient, long-term reference drift, power supply sensitivity, output impedance, and output noise.

Absolute or untrimmed accuracy is the difference between the actual output voltage and the ideal output voltage. It is specified in millivolts.

Temperature coefficient describes the drift in the output voltage with temperature. Since this drift is nonlinear, curve fitting is often used for all temperatures between those actually tested. Voltage references are available with temperature coefficients as low as 1 ppm/°C. Inexpensive references are available with 10 to 50 ppm/°C drift which is comparable to on-chip references of

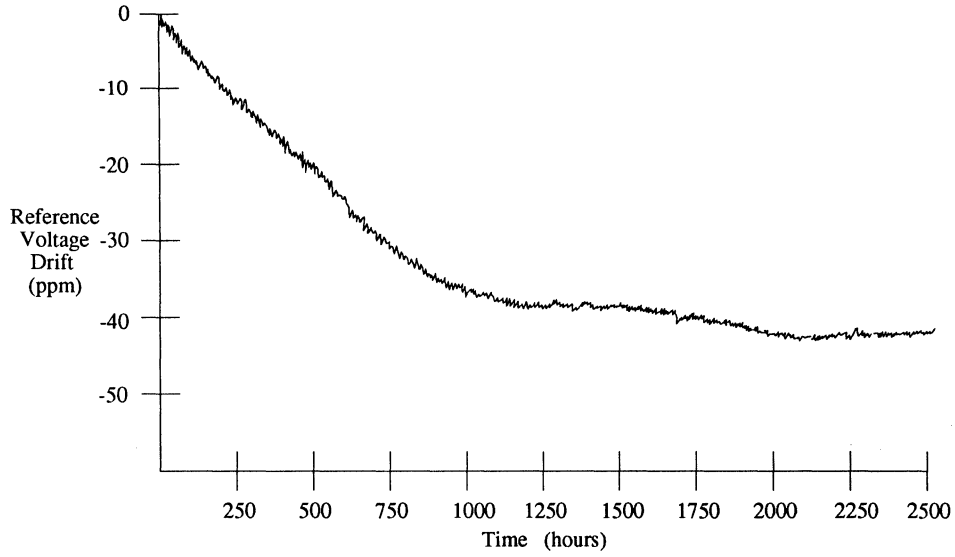


Figure 1. - Long Term Stability of a Typical Zener Reference

bipolar A/D converters. Temperature coefficient is specified in ppm/°C.

Long term stability is the drift in the reference voltage over time. Most references show minor deviations in voltage due to 1/f noise in circuit components. These deviations are usually small and are superimposed on a larger drift characteristic which is due to device aging. An example of this is seen in Figure 1. Long term drift is specified in ppm/1000 hrs.

Power supply sensitivity (line regulation) is the change in output voltage due to a change in power supply. Most references have good power supply rejection at dc, but ac power supply rejection is also important when power supplies are subject to high frequency coupling or noise spikes. PSRR (Power Supply Rejection Ratio) is the ratio of the change in power supply to the change in output voltage. It is specified in dB.

Output impedance is important because of the dynamic loads generated by successive-approximation A/D converters. When the reference is sourcing or sinking current, its output voltage will change due to non-zero output impedance. This impedance must be low enough at all frequencies of interest so the deviation in reference voltage when sourcing current is negligible. Output impedance is specified in ohms.

Output noise can lead to comparison errors in the A/D converter, and subsequently conversion errors. Reference noise is more evident with full scale inputs. It is specified in μV peak-to-peak.

Design Considerations

When interfacing a voltage reference to an A/D converter, the specifications should be robust enough so that the reference does not become a source of conversion error. During conversion, each capacitor of the calibrated capacitor array in the ADC is switched between VREF and AGND in a manner determined by the successive approximation algorithm. The charging and discharging of the array results in a current load at the reference. The ADC's include an internal buffer amplifier to minimize the external

reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. This buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer. The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the internal buffer. This creates an ac current load as the ADC sequences through conversions.

The reference circuitry must have a low enough output impedance to provide the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Also with CS5012,4,6 converters, bits are converted at a 1MHz rate with a full speed (4MHz) clock. The reference must settle within one microsecond so that it will be accurate before the next bit is converted. Signal amplitude dependent loading and conversion settling time require the output impedance of the reference to remain low from dc to at least 1MHz in order to ensure good converter performance.

The CS5012,4,6 series of converters can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. All CS5012,4,6 converters can actually accept reference voltages up to the positive analog supply. However, the internal buffer's offset may increase as the reference voltage approaches VA+. This increases external drive requirements at VREF. Allowing 250mV headroom for the internal reference buffer is recommended. If the supplies are regulated specifically for the converter, 5.0 volt references may be used if the supply voltages for the ADC are kept between ± 5.25 and ± 5.5 volts.

The magnitude of the current load presented to the external reference circuitry by the ADC's will vary with the master clock frequency. At full speed (4MHz clock), the ADC's require maximum load currents of 10µA peak-to-peak (1µA peak-to-peak typical). The voltage reference must supply this current and maintain adequate voltage regulation. The load currents scale proportionately with the master clock frequency. Slower clocks can be used to relax maximum output impedance specification of the reference.

When driving multiple A/D converters from the same reference circuit, load currents will scale proportionally to the number of converters. Distribute the required decoupling components such that each ADC is locally decoupled.

A reference with a maximum output impedance of 2 Ω will yield a maximum error of 20µV. This reference could drive a CS5016 (LSB=69µV with a 4.5V reference) and maintain approximately

Part # \ f_{clk}	4MHz	2MHz	1MHz	500kHz
CS5012 (Vref=4.5V)	27	54	108	216
CS5012 (Vref=2.5V)	15	30	60	120
CS5014 (Vref=4.5V)	7	14	28	56
CS5016 (Vref=4.5V)	2	4	8	16

All units in ohms

Table 1. - Maximum Output Impedance for ≈ 1/4 LSB Reference Deviation

1/4 LSB deviation during conversion. Similarly for the CS5014 (LSB=276µV with a 4.5V reference), and CS5012 (LSB=613µV with a 2.5V reference), maximum impedances of 7 and 15 Ω respectively will maintain adequate regulation. Table 1 defines maximum reference impedances allowed for each of the Crystal A/D's operating at different master clock frequencies in order to keep reference deviation approximately equal to 1/4 LSB.

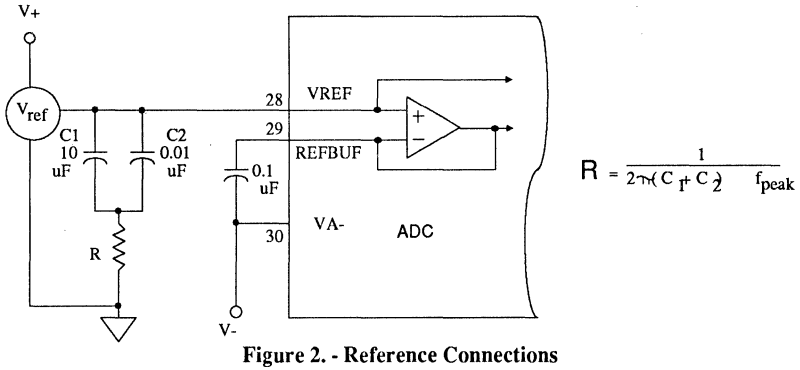
All precision references exhibit extremely low output impedance at dc. However, as frequency increases the impedance also increases. A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum where the reference impedance is too high.

For example, the impedance of an ideal 10µF capacitor drops below 1 Ω at frequencies greater than 16kHz. However, actual capacitors behave differently due to their physical structure. Tantalum-foil electrolytic capacitors begin to appear inductive at frequencies around 100kHz and as a result their impedance begins to rise at frequencies above this. Aluminum electrolytic capacitors appear inductive at frequencies around 10kHz. Ceramic-disk capacitors behave much closer to ideal and begin to appear inductive at frequencies around 5MHz, but 10µF ceramic-disk capacitors are quite rare. Therefore, a high-quality tantalum capacitor (10µF) in parallel with a smaller (0.1µF) ceramic capacitor is recommended. This combination yields low impedance up to frequencies around 50MHz.

Peaking

The presence of large capacitors on the output of some voltage references may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to reduce it.

Most commercially available references use an integrated op-amp to buffer the actual reference generator. External capacitive loading will degrade performance of this op-amp. This degradation can be analyzed using classical analysis techniques. The open loop gain of an ideal op-amp is primarily determined by the internal compensation capacitor which generates a left-half-plane-pole (LHPP) at a very low frequency. The effect of this pole is to reduce the open loop gain by 20dB per decade and to add a -90 degree phase shift to the open loop transfer characteristic. Adding a capacitive load to the output of the op-amp generates another LHPP at a frequency inversely proportional to the capacitor's value. An additional 20dB per decade reduction in gain and -90 degree phase shift result from the second LHPP.



$$R = \frac{1}{2\pi(C_1 + C_2)\, f_{peak}}$$

Figure 2. - Reference Connections

The unity gain bandwidth of an op-amp (f_0), is the frequency at which the open loop gain goes to unity. If the total phase shift reaches -180 degrees before f_0 is reached the op-amp will become unstable. The closed loop frequency response peaks at f_0. As the total open loop phase shift at f_0 approaches -180 degrees, the closed loop peak at f_0 approaches infinity. The point of critical damping is the point where the peaking is precisely zero. Any phase shift less than this results in no peaking, and phase shift greater than this results in increased peaking.

Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 2). This resistor adds a left-half-plane-zero (LHPZ) to the open loop characteristic of the op-amp. This zero increases the gain by 20dB per decade, and adds a +90 degree phase shift. The resulting reduction in total phase shift at f_0 reduces peaking in the closed loop characteristic. The equation in Figure 2 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

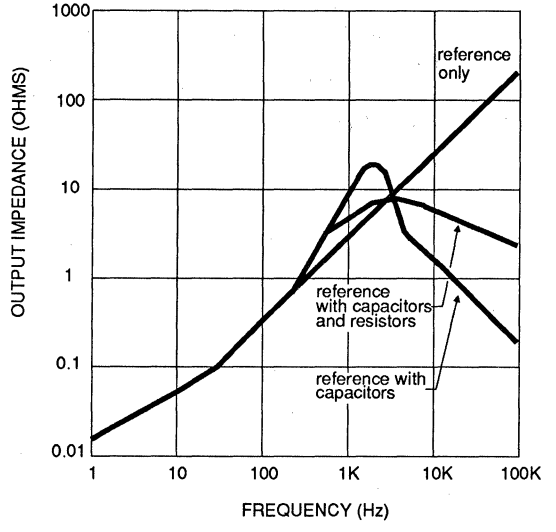


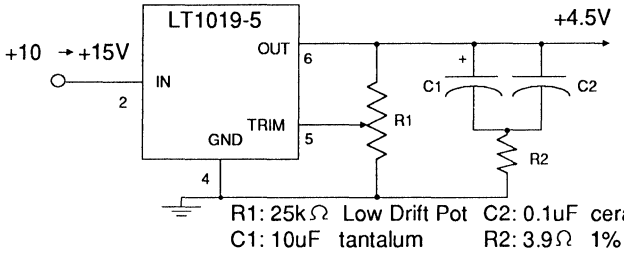
Figure 3. - Output Impedance Curves for LT1019-5

Design Example

Figure 3 shows the output impedance characteristic of an LT1019-5 reference trimmed to 4.5V. The three curves represent impedances of the stand-alone reference, the reference with a 10µF tantalum and a 0.1µF ceramic capacitor added in parallel to the output, and the reference with the capacitors and a 2.2 Ω resistor in series with them (See Figure 2). Without loading, the reference impedance rises above 100 Ω at 50kHz. Adding the capacitors, peaking can be seen, but the maximum impedance is about 13 Ω at 4kHz. As shown in Table 1, 13 Ω is sufficient for use with the 12-bit converters and for the 14 and 16-bit converters with slow master clocks. With the addition of the 2.2 Ω resistor, the peak is reduced to 6 Ω and the impedance approaches 2.2 Ω at high frequencies.

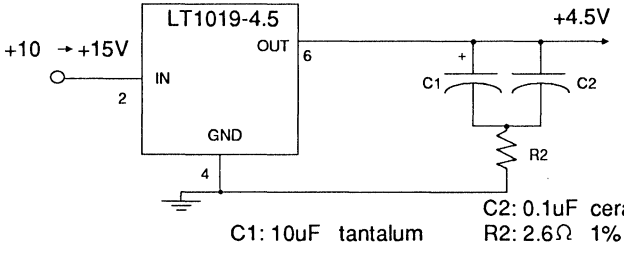
Suggested Voltage Reference Circuits

Nine reference circuits were characterized for use with the CS5012, CS5014, CS5016, CS5101, CS5102, CS5126 family of successive-approximation A/D converters. Important reference specifications such as output impedance and drift were measured for all references using standard test techniques. In addition, a Fast-Fourier Transform (FFT) test was performed to characterize the total dynamic performance of each reference circuit while driving a CS5016 converter. The same CS5016 was used for all tests yielding results which allow the comparison between different references. A summary of performance can be seen in the table at the end of this application note. During the FFT test, a pure sine wave is applied to the CS5016 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the waveform and distributes its energy among 512 "frequency bins". Distribution of energy in bins outside of the fundamental and dc can be attributed to errors in the A/D converter's performance, the reference, or the input sine wave.



Reference Type	Bandgap
Untrimmed Accuracy	2.5mV
Max Impedance	6.5Ω @3.2kHz
Total Output Drift	5ppm/ °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	250uV p-p
S / (N + D) (100Hz)	89dB
S / (N + D) (1kHz)	89dB

Figure 4. LT1019-5 Reference Trimmable to 4.5V



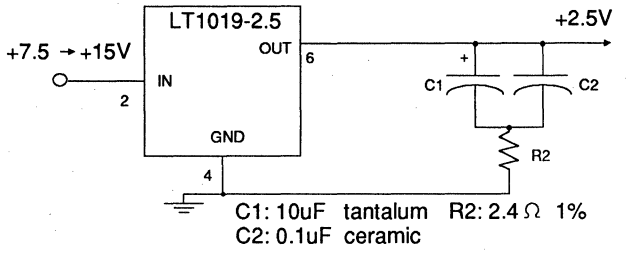
Reference Type	Bandgap
Untrimmed Accuracy	3.0mV
Max Impedance	3.1Ω @6.1kHz
Total Output Drift	5ppm/ °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	150uV p-p
S / (N + D) (100Hz)	91dB
S / (N + D) (1kHz)	90dB

Figure 5. LT1019-4.5 Reference

The result of the FFT test is the ratio of input signal amplitude to the combination of harmonic distortion and total integrated noise. It is referred to as S/(N+D) in all of the performance charts in Figures 4 to 10. This ratio is expressed in dB. If input sine wave distortion and the actual A/D converter's distortion and noise are assumed to be negligible, the S/(N+D) is due to the reference only. In reality, this assumption can not be made. In the case of the Great Reference (See Figure 11), performance matches or exceeds the capability of the test setup. S/(N+D) ratios of 72 and 82 dB are sufficient for the 12-bit and 14-bit converters. For the 16-bit converters, 88 to 94 dB is necessary.

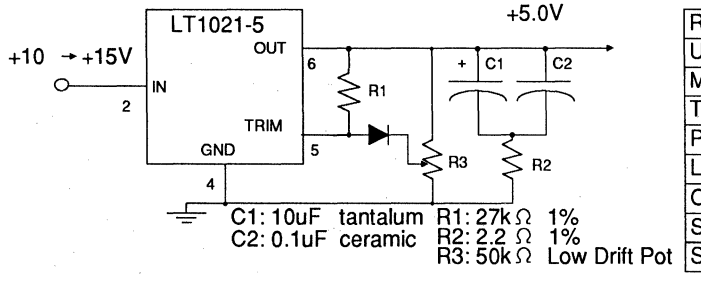
FFT tests were performed at 100Hz and 1kHz. The 100Hz test checks the output impedance of the reference chip itself which dominates at low frequencies. The 1kHz FFT test checks the output impedance at intermediate frequencies in the kHz range. The highest output impedance was seen in all references at these intermediate frequencies. Since the reference capacitors dominate the impedance at high frequencies, high frequency FFT tests were not necessary. Although not tested, the best reference is likely to yield the best DNL performance.

The least complicated reference circuit is the stand-alone reference chip with a passive compensation network. Its temperature drift and noise performance is equal to the reference chip itself since the compensation network does not change the dc output voltage. Keeping the output impedance low from dc to 1MHz is not trivial however, since there is no additional active circuitry added to perform this task. Five references were tested in the stand-alone configuration. Figures 4, 5, 6, 7, and 8 illustrate schematics and measured specifications for these references. All references are monolithic with the exception of the CS3902 reference which is a hybrid. Notice that the CS3902 and the LT1019-4.5 require no trimming for 4.5V operation. The calculated value of R2 in each of the references above will



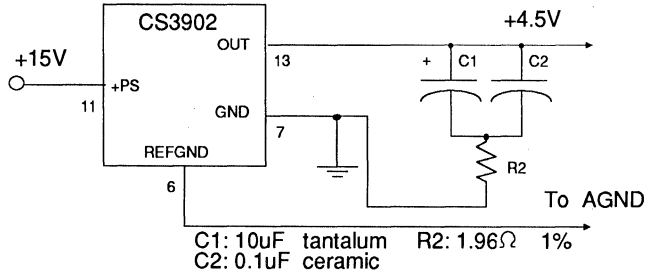
Reference Type	Bandgap
Untrimmed Accuracy	1.25mV
Max Impedance	4.0Ω @5.8kHz
Total Output Drift	5ppm/ °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100uV p-p
S / (N + D) (100Hz)	87dB
S / (N + D) (1kHz)	86dB

Figure 6. LT1019-2.5 Reference



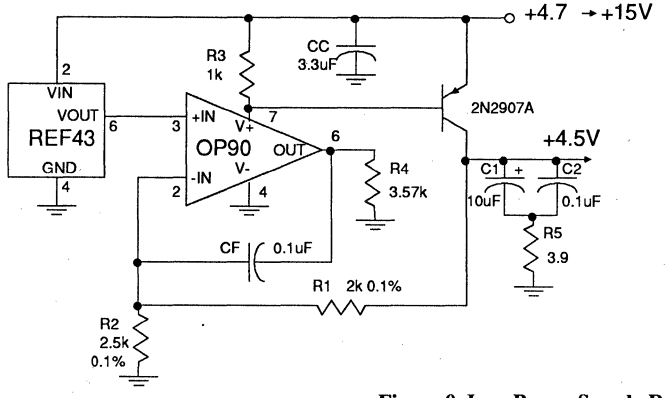
Reference Type	Zener
Untrimmed Accuracy	2.5mV
Max Impedance	3.8Ω @5.0kHz
Total Output Drift	3ppm/ °C
PSRR (50Hz to 500Hz)	86dB
Long Term Stability	15ppm/1000hr
Output Noise	60uV p-p
S / (N + D) (100Hz)	90dB
S / (N + D) (1kHz)	90dB

Figure 7. LT1021 Reference



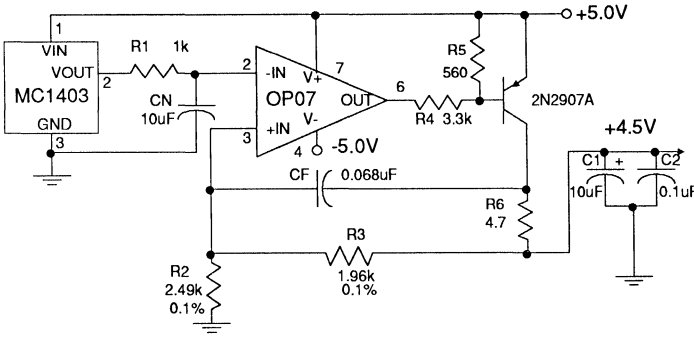
Reference Type	Zener
Untrimmed Accuracy	500uV
Max Impedance	2.5Ω@20kHz
Total Output Drift	0.5ppm/ °C
PSRR (50Hz to 500Hz)	100dB
Long Term Stability	6ppm/1000hr
Total Output Noise	80uV p-p
S / (N + D) (100Hz)	90dB
S / (N + D) (1kHz)	90dB

Figure 8. CS3902 Reference



Reference Type	Bandgap
Untrimmed Accuracy	1.5mV
Max Impedance	4.4Ω @ 1kHz
Total Output Drift	8.0ppm/ °C
PSRR (50Hz to 100Hz)	60dB
Long Term Stability	-
Output Noise (dc to 1MHz)	400uV p-p
S / (N + D) (100Hz)	88dB
S / (N + D) (1kHz)	88dB

Figure 9. Low Power Supply Reference



Reference Type	Bandgap
Untrimmed Accuracy	50mV
Max Impedance	6.9Ω@ 2kHz
Total Output Drift	25ppm/°C
PSRR (50Hz to 100Hz)	80dB
Long Term Stability	-
Output Noise (dc to 1MHz)	30uV p-p
S / (N + D) (100Hz)	90dB
S / (N + D) (1kHz)	90dB

Figure 10. Low Headroom Reference

change slightly between units. Since the actual variation is small, picking the closest 1% tolerance resistor to the calculated value should give similar performance for all references of a particular manufacturer's model.

Other stand-alone voltage references with similar specifications include the AD584, REF02, REF03, REF10, and REF43. When designing with these references, the equation shown in Figure 2 should be used to calculate the appropriate value of R2 for each type of reference.

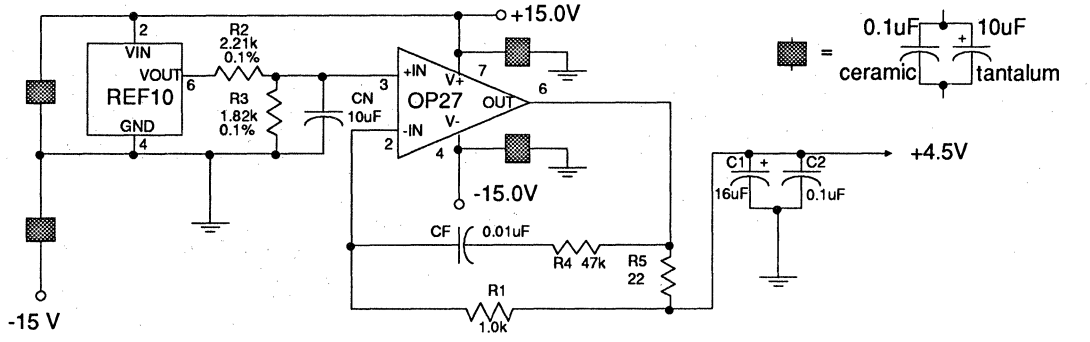
For applications which use ± 5.0 volt supplies, the reference in Figure 9 can be used. This reference circuit, designed by PMI, takes advantage of their new low power op-amp in a novel feedback configuration to achieve a 4.5 volt reference which operates from 4.7 to 15 volt supplies.

Since only a few microamps of quiescent current flows in the op-amp, it can be assumed that the only current flowing in R3 is the same as that flowing in R4. It can be shown that V6 = 3.57(Vin-V7). For an output of 4.5 volts, and a supply of 4.7 volts, the op-amp has a supply of approximately 4.0 volts and an output voltage of 2.14 volts. This output voltage is well within the maximum specification of the OP-90 op-amp. Other references can be substituted for the REF43 if different drift or noise specifications are required.

The reference shown in Figure 10 is a low noise reference with less than 30μV peak-to-peak of noise from dc to 1MHz. It uses a discrete output stage allowing Vref to come within 300mV of the positive supply. The filtering network R1,CN reduces the bandwidth of the reference and therefore reduces the total output noise. The OP-07 is a low noise op-amp which buffers the filtered reference. This op-amp contributes very little noise to the entire reference circuitry.

The temperature coefficient of this reference is primarily due to to the matching of the gain resistors R2 and R3, so low temperature drift resistors should be used. Long term drift is dominated by the MC1403's drift. Other 2.5 volt references can be used to improve this specification. The output voltage can be changed by adjusting R2 and R3 according to the following equation: Vref = Vout*((R2+R3)/R2). Resistors with 0.1% tolerance for R2 and R3 limit the reference's untrimmed accuracy only. Resistors with 1% or 5% tolerance can be used if untrimmed accuracy less than 50mV is not necessary. The supplies of the OP-07 should be bypassed with 0.1μF capacitors to ground.

The reference in Figure 11 exhibits very good noise, output impedance, and long term drift per-



Reference Type	Bandgap
Untrimmed Accuracy	25mV
Max Impedance	0.5Ω @ 3kHz
Total Output Drift	9ppm/°C

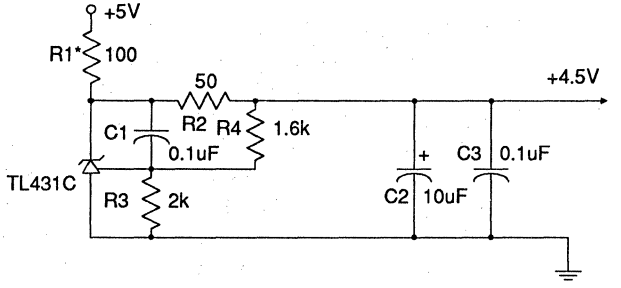
PSRR (50Hz to 100Hz)	95dB
Long Term Stability	50ppm/1000hr
Output Noise (dc to 1MHz)	5uV p-p
S / (N + D) (100Hz)	92dB
S / (N + D) (1kHz)	92dB

Figure 11. - Great Reference

formance. It can be used in applications which have ± 15 volt supplies available. The reference has noise less than 10μV peak-to-peak from dc to 1MHz. The filtering network R2, R3, and CN filters noise components greater than 10Hz from the output of the REF10 reference. The OP-27 is a very low noise op-amp with excellent input offset drift over time and temperature.

The temperature coefficient of this reference is primarily due to the matching of the voltage divider R2 and R3, assuming that an appropriate low leakage capacitor is chosen for CN. Matched, low temperature drift resistors should be used when absolute accuracy is required. Temperature drift of the reference chip plus input offset drift of the op-amp is about 9ppm/°C. Other 10 volt references can be used in place of the REF10.

The reference voltage can be changed by adjusting R2 and R3 according to the following equation. Vref = Vout*(R3/(R2+R3)).



* Can be operated from +12 or +15 volts if R1 is changed to 2K.

Reference Type	Bandgap
Untrimmed Accuracy	30mV
Max Impedance	50 Ω @600Hz
Total Output Drift	30ppm/ ℃
PSRR (50Hz to 500Hz)	85dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100uV p-p
S / (N + D) (100Hz)	92dB
S / (N + D) (1kHz)	91dB

Figure 12. -TL431 Shunt Reference

This circuit has no protection against accidentally applying ± 15V to the VREF pin. This could occur if the OP27 fails.

For applications where good dynamic performance is required, but only moderate dc accuracy, the TL431 shunt reference is an inexpensive solution. Figure 12 shows an example circuit, along with the excellent dynamic performance numbers.

Miscellaneous Applications Information

Noise from the voltage reference element may reduce system performance. Bandgap references tend to generate much more noise than zener diodes. To obtain the best noise performance from the reference element, it should be band-limited. Note the broadband noise for the LT1019-5 circuit (Figure 4, 250µV) versus the noise of a similar bandgap reference with additional circuitry to band-limit the noise as in the Great Reference (Figure 11, 10µV).

Thermal temperature gradients due to power dissipation on the voltage reference die can create output voltage shifts. Keeping the entire chip on an isothermal plane is helpful. Reference load conditions should be kept very close to those specified, or degraded temperature performance will result. Some references specify a thermal regulation in ppm/mW. This can be used to calculate voltage drift for a specific power dissipation due to loading.

Overall die temperature change can cause thermally induced output voltage variations which can exceed electrical effects. Shifts in power dissipation on the board level are the major contributor to this error. In critical applications, using a heat-sink is recommended to keep the reference temperature deviations small.

Thermocouple effects between package leads can also cause excessive output voltage drift and noise. Differences between materials in IC leads and PC-board traces can cause thermoelectric effects. Ambient air turbulence around the leads causes mismatches in the temperature between the package leads. The resulting thermoelectric voltage contributes to noise. Using dual in-line packages (DIPs) is recommended over using TO-5 type packages. The copper or Alloy 42 lead frames on DIPs are much less sensitive to thermocouple effects than the Kovar leads of the TO-5 packages. Using an enclosure such as a polysulfone shield which blocks the air flow over the reference package will also reduce the problem by reducing air movement around the package leads.

In reference circuits which have external gain setting resistors, tracking of the temperature coefficients of these resistors is vital. Wirewound resistors made of Evenohm or Mangamin have the lowest temperature coefficients. Ceramic film resistors such as Vishay are also good. Matching in resistor temperature coefficients as good as 0.4 ppm/°C can be achieved. Arranging these resistors in close proximity to one another also helps matching. SIP or DIP resistors by Beckman and Vishay exhibit the best matching since all resistors are processed on the same substrate.

Part #	Manufacturer	Telephone Number
CS3902	Crystal Semiconductor	(512) 445-7222
LT1019-5 LT1019-4.5 LT1019-2.5 LT1021-5	Linear Technology	(408) 432-1900
OP07 OP90 REF02 REF03 REF43 OP27 REF10	Precision Monolithics Inc.	(408) 727-9222
TL431	Texas Instruments	
TL431 MC1403	Motorola	

List of Manufacturers

Reference	Type	Untrimmed Accuracy	Maximum Impedance	Output Drift	PSRR (50Hz to 100Hz)
LT1019-5	Bandgap	2.5mV	6.5Ω @ 3.2kHz	5ppm/° C	90dB
LT1019-4.5	Bandgap	3.0mV	3.1Ω @ 6.1kHz	5ppm/ C	90dB
LT1019-2.5	Bandgap	1.25mV	4.0Ω @ 5.8kHz	5ppm/° C	90dB
LT1021-5	Zener	2.5mV	3.8Ω @ 5.0kHz	3ppm/° C	86dB
CS3902	Zener	500uV	2.5Ω @ 20kHz	0.5ppm/° C	100dB
Low Supply	Bandgap	1.5mV	4.4Ω @ 1kHz	8ppm/° C	60dB
Low Headroom	Bandgap	50mV	6.9Ω @ 2kHz	25ppm/° C	80dB
Great	Bandgap	25mV	0.5Ω @ 3kHz	9ppm/° C	95dB
TL431 Shunt	Bandgap	30mV	50Ω @ 600Hz	30ppm/° C	85dB

Reference	Long Term Stability *	Output Noise (dc to 1MHz)	S/(N+D) (100Hz)	S/(N+D) (1kHz)
LT1019-5	-	250uV p-p	89dB	89dB
LT1019-4.5	-	150uV p-p	91dB	90dB
LT1019-2.5	-	100uV p-p	87dB	86dB
LT1021-5	15ppm/1000hr	60uV p-p	90dB	90dB
CS3902	6ppm/1000hr	80uV p-p	90dB	90dB
Low Supply	-	400uV p-p	88dB	88dB
Low Headroom	-	30uV p-p	90dB	90dB
Great	50ppm/1000hr	10uV p-p	92dB	92dB
TL431 Shunt	-	100uV p-p	92dB	91dB

Performance Comparison Table

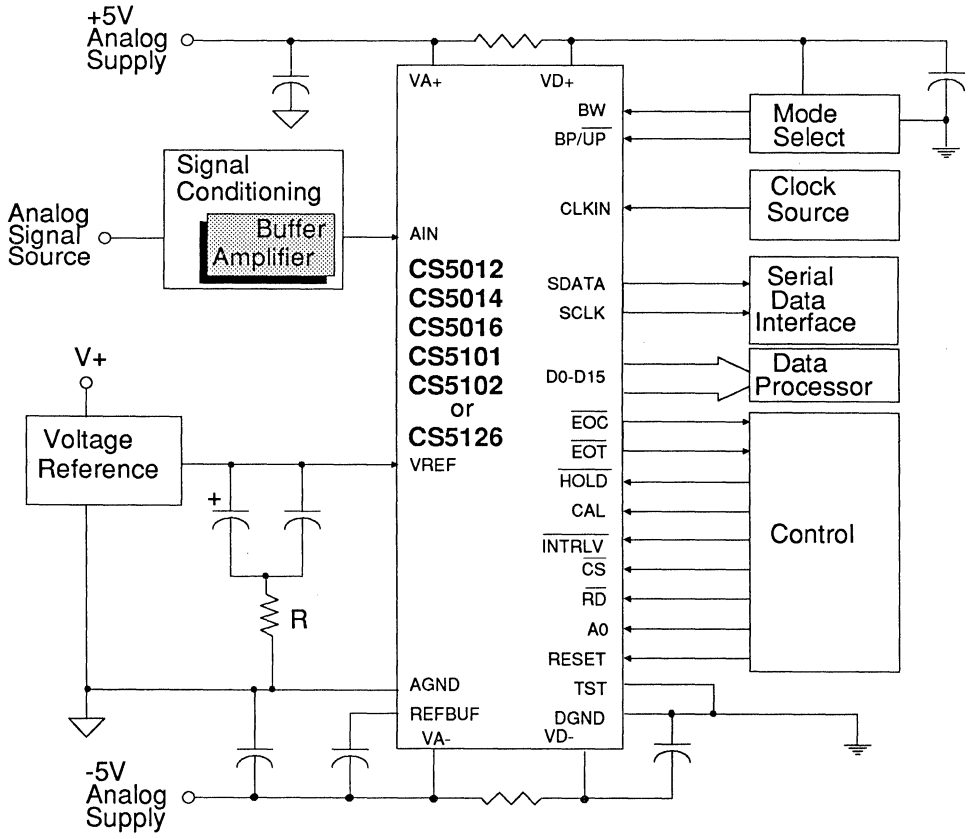
* Taken from reference data sheets. All other parameters were measured.

Application Note

Buffer Amplifiers for the CS5012/CS5014/CS5016/ CS5101/CS5102/CS5126 Series of A/D Converters

by

Jerome Johnston



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Introduction

This application note discusses buffer amplifiers for use with Crystal Semiconductor's CS5012, CS5014, CS5016, CS5101, CS5102 or CS5126 A/D converters. Amplifier design considerations are discussed and several circuits are proposed.

Signal Requirements for Analog to Digital Converters

Crystal Semiconductor is a source for a variety of monolithic A/D Converters. While the type of design configuration of the converters may differ, their uses could be classified into two general categories: those which require specifications in static measurement applications; and those which require specifications for signal processing or dynamic signal measurement applications.

The capability of a converter to achieve a stated static measurement requirement is generally defined by its linearity error specifications, both integral and differential, and by its offset error and gain error specifications. To assess the total error in a static measurement, the effects of temperature on the offset, gain, and linearity errors must also be investigated. In static measurement systems, these same error sources need to be scrutinized in the signal conditioning circuitry as well.

When a converter is used in dynamic signal measurement applications (generically known as "signal processing"), its signal measurement capability is indicated by specifications such as total harmonic distortion, signal to noise ratio, and signal to peak harmonic or spurious noise. Signal processing designers generally evaluate the error contribution of the signal conditioning circuitry in terms of these same parameters.

Signal conditioning circuitry generally includes all circuitry from the transducer or the signal source up to the A/D converter. This application note will concern itself primarily with the requirements of the amplifier which immediately precedes the A/D converter. This amplifier will be called a buffer amplifier.

In the design of an A/D converter system, the buffer amplifier can be a source of significant errors. The significance of these errors can only be assessed if the circuit configuration is thoroughly analyzed for its total error contribution. A thorough analysis requires a good understanding of amplifier specifications, of the limitations of the different circuit configurations, and of the benefits and limitations of feedback. A good place to begin is with a review of feedback theory.

I. OPERATIONAL AMPLIFIERS: Review Of Theory

Feedback Control Theory

The goal in using feedback is to establish a closed-loop system whose operating characteristics are primarily determined by the choice of the feedback elements. The extent to which this goal can be accomplished is explained by feedback control theory. Figure 1 illustrates the classical feedback control loop. The equations which

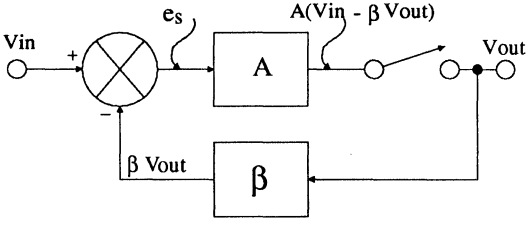


Figure 1. The Classic Feedback Control Loop

describe this control loop are directly applicable to the noninverting operational amplifier circuit.

The control loop consist of an input voltage differencing section whose output is amplified by a positive gain section. A fractional part of the signal output is then returned to the negative terminal of the differencing section though the feedback network. The input differencing section, indicated by the circle with the X in it, determines the difference in the signals at the (+) and (-) inputs. The difference is indicated by an error signal of the quantity:

$$e_S = (V_{in} - \beta V_{out})$$

Equation 1

which is then amplified by the open-loop voltage gain of the amplifier:

$$A (V_{in} - \beta V_{out}) = V_{out}$$

Equation 2

The amplifier open-loop gain is represented in Figure 1 by the box with the A in it. The feedback portion of the loop is represented by the box with the β in it. β is defined as the feedback attenuation factor and its value is that fractional part of the output voltage which is fed back to the input. Equation 2 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{A}{1 + A\beta}$$

Equation 3.

This is the key equation in the feedback system. Equation 3 indicates that the closed-loop gain is dependent upon both the open-loop gain and the feedback factor, β. The product, Aβ, in the denominator is called the loop gain. Its name comes from the gain seen by a signal propagating around the loop through both the A and β networks.

Equation 3 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{1}{\beta} \left[\frac{1}{1 + \frac{1}{A\beta}} \right]$$

Ideal Term Error Multiplier

Equation 4

In equation 4 the ideal term, 1/β, determines the ideal closed-loop gain of the system. The value of 1/β is determined by the elements chosen for the feedback path. The intent is for these elements to determine the closed-loop characteristics of the feedback system. To the extent that this is accomplished is dependent upon the magnitude of the loop gain Aβ. The greater the magnitude of Aβ, the more closely the error multiplier term approaches unity, therefore allowing the ideal term 1/β to determine the closed-loop gain of the system. Said another way, the magnitude of the loop gain Aβ is the primary factor which determines how closely the closed-loop performance of a feedback system is determined by the feedback elements. The term 1/β is known as the noise gain and also determines the gain seen by amplifier input referred noise and other input referred errors (such as offsets and drift parameters). The noise gain of the system is used to determine closed loop amplifier performance with respect to these error parameters, not the signal gain. The noise gain of the two basic op amp configurations will be discussed later in this application note.

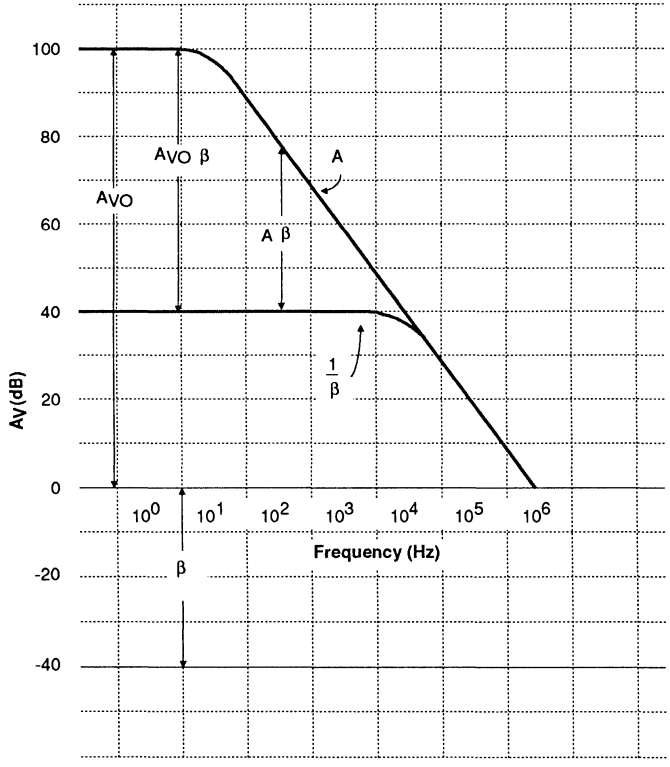


Figure 2. Bode plot illustrating the relationship of Avo, β, 1/β, and Avoβ.

Feedback and the Operational Amplifier Bode Plot

The feedback parameters which have been discussed can be depicted graphically on a Bode plot. Figure 2 depicts the relationship between open-loop gain, the feedback attenuation factor, noise gain, and loop gain as a function of frequency for the noninverting circuit.

The Bode diagram shows a typical plot of the open-loop gain characteristic of an operational amplifier. At very low frequencies a typical operational amplifier may have a dc open-loop gain, (Avo) near 100 dB. A large number of amplifiers use dominant pole frequency compensation which simplifies the compensation requirements for the user. The dominant pole, located between 0.1 and 100 Hz on various amplifiers, causes the open-loop gain characteristic (A) to decrease in magnitude at a 20 dB/decade rate as the frequency is increased. In Figure 2 the logarithm of the feedback attenuation factor (β) is shown to be negative as it is a reduction in signal amplitude. The loop gain, the product of Aβ, (or Avoβ at dc), is depicted in the figure as the sum (+100 dB plus -40 dB = 60 dB at very low frequency) of the open-loop gain and the feedback attenuation factor, or the difference (+100 dB - (+40 dB) = 60 dB) between the open-loop gain and the noise gain (1/β). From the figure, one can observe that as frequency increases, the loop gain (Aβ) decreases for a set value of β. To obtain a greater amount of loop gain at higher frequencies a designer must either

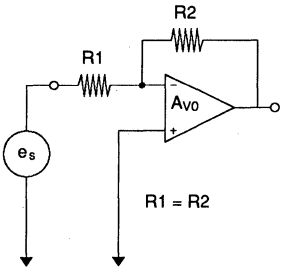


Figure 3A. Inverting: Gain of -1

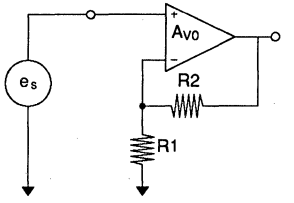


Figure 3B. Noninverting: Nonunity Gain

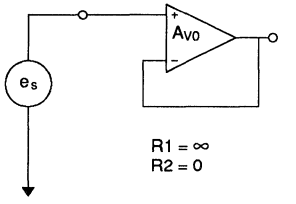


Figure 3C. Noninverting: Gain of +1

Closed Loop Signal Gain	$A_{CL} = \frac{-R2}{R1}\left[\frac{1}{1+\left[\frac{1}{A\beta}\right]}\right]$	$A_{CL} = \left[\frac{R1+R2}{R1}\right]\left[\frac{1}{1+\frac{1}{A\beta}}\right]$	$A_{CL} = 1\left[\frac{1}{1+\frac{1}{A\beta}}\right]$
Feedback Attenuation Factor	$\beta = \frac{R1}{R1+R2} = \frac{R}{2R} = 0.5$	$\beta = \frac{R1}{R1+R2}$	$\beta = 1$
Loop Gain	$A_{V0}\beta$		
Noise Gain	$\frac{1}{\beta} = \frac{1}{0.5} = 2$	$\frac{1}{\beta}$	$\frac{1}{\beta} = 1$
Closed Loop Corner Frequency	$f_c = \frac{f_u}{\lvert A_{CL}\rvert+1}$ note: $\lvert A_{CL}\rvert = \frac{1}{\beta} - 1$	$f_c = \frac{f_u}{\left[\frac{1}{\beta}\right]}$	$f_c = f_u$
Closed Loop Gain Stability	$\frac{\Delta A_{CL}}{A_{CL}} = \frac{\Delta A_{OL}}{A_{OL}}\left[\frac{1}{1+A\beta}\right]$		
Closed Loop Distortion and Nonlinearity	$THD_{CL} = THD_{OL}\left[\frac{1}{1+A\beta}\right]$		
Closed Loop Output Impedance	$Z_{CL} = Z_{OL}\left[\frac{1}{1+A\beta}\right]$		

Figure 3. Basic Circuit Configurations

increase the open-loop gain of the amplifier or increase the feedback factor, β (decrease the noise gain). Remember that both the open-loop gain and the feedback attenuation factor are not constant, but instead are functions of frequency. Therefore the value of the loop gain is a function of frequency as well. The quantity of loop gain at the operating frequency is the key measure of how closely an amplifier configuration approaches the ideal.

Amplifier Configurations and Feedback

Figure 3 provides an overview of the inverting and noninverting voltage amplifier configurations. General equations for various parameters of the configurations are given with special emphasis on the unity gain configuration. Signal gain is set by the choice of resistors, but the gain error (assuming perfectly accurate resistors) is a function of the loop gain in the error multiplier term as previously stated in our discussion on feedback. The unity gain noninverting amplifier is just a special case of choosing the value of resistor R1 as being infinite and R2 being zero. Notice that the feedback attenuation factor, β, as

$$\beta = \frac{R1}{R1+R2}$$

Equation 5

derived for both circuits yields the same equation: but for the unity gain inverting amplifier this results in a value of 0.5 whereas the unity gain noninverting amplifier results in a β of 1. These unequal values of β between the two unity-gain configurations yield further differences between the inverting and noninverting circuits. Loop gain for the unity-gain inverting circuit is half that of the noninverting unity-gain circuit. This results in the inverting circuit being more easily compensated for stability, but also yields greater errors in those parameters where loop gain is a factor. More will be said about these parameters later.

Reduced β for the inverting configuration results in greater noise gain (1/β). Error sources such as offset and noise are amplified by the noise gain and therefore the unity-gain inverting amplifier is more adversely affected by these error sources. Another negative factor of the unity-gain inverting stage is that its signal bandwidth is half that of the noninverting circuit with identical amplifiers. This bandwidth reduction is because bandwidth is a function of the noise gain, not the signal gain. Be aware of this fact when using low gain inverting stages.

The magnitude of the loop gain in a circuit affects many parameters in both the inverting and noninverting configurations. Closed loop gain stability is improved by increased loop gain as indicated in the equation:

$$\frac{\Delta A_{CL}}{A_{CL}} = \frac{\Delta A_{OL}}{A_{OL}} \left[\frac{1}{1 + A\beta} \right]$$

Equation 6

The effects of changes in the open-loop gain (such as a reduction due to increased temperature) are reduced proportionally to the amount of loop gain. Open loop distortion and nonlinearity are reduced by increased loop gain. This reduction in total harmonic distortion as indicated in the equation:

$$THD_{CL} = THD_{OL} \left[\frac{1}{1 + A\beta} \right]$$

Equation 7

The output impedance of a voltage amplifier is reduced with feedback as indicated in the equation:

$$Z_{CL} = Z_{OL}\left[\frac{1}{1+A\beta}\right]$$

Equation 8

The input impedance of both amplifier configurations benefit from increased loop gain. Although increased loop gain is desireable in both circuit configurations the effect of feedback on the two configurations is different.

The noninverting amplifier utilizes voltage ratio feedback which increases the differential input impedance seen by the input signal. But the differential input impedance of the amplifier is shunted by the common mode input impedance of the amplifier. Because the common mode impedance cannot be increased by the use of feedback it is usually the limiting factor in increasing the input impedance.

The inverting amplifier configuration uses transadmittance feedback which decreases the impedance at the summing node of the input and feedback resistors. This decrease in impedance improves the virtual ground characteristic of the amplifier. In the inverting configuration the effect of a good virtual ground enables the effective value of the input impedance seen by the signal source to be set by the input resistor.

In both configurations the improvements to the respective impedances depend on the magnitude of loop gain. As the magnitude of loop gain generally decreases with increased frequency, all of the parameters normally improved by loop gain tend to degrade as the signal frequency increases. All real-world amplifiers have finite open loop gain and finite bandwidth, both of which affect the amount of loop gain available to a designer. A designer must make a prudent choice of amplifier and of the circuit configuration to minimize the errors due to loop gain limitations.

Some Other Error Sources

There are many sources of error in a given amplifier configuration. As already discussed, limited loop gain is a source of gain error which can affect DC accuracy. In addition to the DC gain error, there are the various offset errors which are contributed dependent upon the characteristics of the chosen amplifier. Sources of offset errors are the input offset voltage of the amplifier, the input bias and the input offset currents of the amplifier, limited power supply rejection and limited common-mode rejection.

Which of these errors is dominant will depend upon the choice of amplifier and its application configuration. It is a routine procedure to calculate the contribution of each source of error and this should be done as a matter of course. A few comments on each of these sources of error is appropriate.

All amplifiers have input offset voltage and input bias currents which result in errors in signal measurement. The input bias currents flow through the resistances on the (+) and (-) leads of the amplifier and produce an offset voltage error at each input. These offset voltages, and the voltage offset of the amplifier itself, are then amplified by the circuit to produce an error in the output signal. To reduce the errors due to the bias currents the standard practice has been to balance the value of resistance at the inverting and noninverting inputs to an amplifier. The purpose of making these two resistances equal has been to enable the bias currents at both inputs to produce equivalent values of offset voltage which could then be rejected by the common mode capability of the amplifier. This practice is an acceptable method of reducing error due to the bias currents and is recommended except with modern

amplifier designs which have internal bias current compensation circuitry. The bias current compensation circuitry tends to reduce the bias currents an order of magnitude or more, to the extent that they are reduced to the same order of magnitude as the amplifier's input offset currents. Adding a resistor to one input to achieve equal resistances at the two inputs of these types of amplifiers is not recommended. The added resistance is not effective in reducing the error due to the bias currents, but it will add another source of thermal noise.

Initial offset errors as well as gain errors generally can be reduced to zero with initial system calibration adjustments at room temperature. The effects of temperature-induced offset drift and gain drift remain unless a method of ongoing correction or recalibration is used to remove these effects. This correction may be accomplished with a computer after the analog signals are digitized and is recommended when maximum accuracy of measurement is demanded.

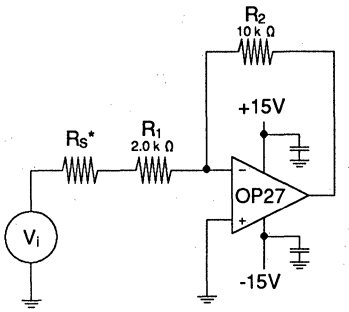
Even if the effects of temperature-induced offset errors are removed from the final data by software, it remains desirable to examine the total errors at each gain stage thoughout the system. Voltage offsets due to temperature drift can be removed in software, but may still consume a significant portion of the dynamic range available to the signal. This is especially true in 16-bit converter systems with wide temperature range requirements such as required by some military specifications (-55 to +125 ° C).

Limited power supply rejection and limited common mode rejection are two more sources of errors. Most commercially-available amplifiers are designed such that the offset voltages induced by power supply variations or common-mode signals are very small; but these errors can be significant when amplifying very low level signals with high gain. It is therefore recommended to examine the error contribution of each of these sources.

Figure 4a shows an inverting amplifier circuit. The operational amplifier and the circuit components have been chosen for illustration purposes. The errors in the circuit due to the various amplifier parameters will be examined. Not included are those errors due to the signal source impedance (the impedance is assumed to be zero), output loading (which reduces open loop gain), resistor tolerance and temperature coefficient, and component long term drift effects.

A table in Figure 4a contains a selected subset of specifications for a "generic" OP-27C. No specific manufacturer is implied. The subset of data is for the total error band of the stated parameters over the -55° to +125°C temperature range. Manufacturers do not always specify temperature drift coefficients in their component data sheets. Instead, the specification sheets contain a table of data for the amplifier at room temperature (25° C) along with a table showing the total error band of the various parameters over a stated temperature span (say 55° to 125° C). Usually the specification data tables are supplemented by supporting graphs which indicate typical drift characteristics for the various parameters. These graphs can be very informative. For example, graphs in the manufacturer's data sheets (see the Precision Monolithics or the Linear Technology data book) for the OP-27 indicate that input bias currents and input offset currents show much more drift at temperatures approaching -55° C than at temperatures above 25° C. Another graph indicates that the direction of the input offset voltage drift in the OP-27 is unpredictable.

The normal procedure to calculate the error contribution of each of the operational amplifier drift parameters is to multiply the rate of drift times the temperature span over which the circuit is to be subjected. These errors due to drift are then added to the initial errors of each of the parameters at the ambient operating temperature. Because amplifier manufacturers specify total



* Assumed to be zero.

$$R_e = \frac{R_2 R_1}{R_1 + R_2} = 1.667\ k\Omega$$

Ideal Signal Gain $= \frac{-R_2}{R_1} = -5$

Feedback Attenuation Factor $\beta = \frac{R_1}{R_1 + R_2} = \frac{1}{6}$

Noise Gain $= \frac{1}{\beta} = 6$

Closed Loop Bandwidth $f_c = \left[\frac{f_u}{|A_{CL}| + 1}\right] \frac{8 \times 10^6}{6} = 1.33\ MHz$

Generic OP-27 Specifications
Total Error Band for -55° to +125°C Temperature Span

		Typical	Worst Case
Input Offset Voltage	$V_{IO_{\Delta t}}$	70 µV	300 µV
Input Bias Current†	$I_{B_{\Delta t}}$	±35 nA	±150 nA
Large Signal Open Loop Gain	A_0	800×10^3 V/V	300×10^3 V/V
Power Supply Rejection Ratio	P.S.R.R.	4×10^{-6} V/V (108 dB)	51×10^{-6} V/V (86 dB)
Common Mode Rejection Ratio	C.M.R.R.	1.6×10^{-6} V/V (116 dB)	20×10^{-6} V/V (94 dB)

† Bias currents are usually of one polarity. Bias currents of both polarities indicate the use of bias current cancellation circuitry in the input stage.

Figure 4a. OP-27 Circuit and Total Error Band Specifications

Errors: -55 ° to 125 °C (Δt)

	Gain	Input Offset Voltage	Input Bias Current	P.S.R.	C.M.R.	Noise
$V_o = -V_i$	$\frac{R_2}{R_1}\left[\frac{1}{1 + \frac{1}{A0\beta}}\right]$	$+ V_{IO_{\Delta t}}\left[\frac{1}{\beta}\right] +$	$I_{B_{\Delta t}} R_1 \left[\frac{R_2}{R_1}\right] +$	$\frac{2\Delta V_{IO}}{\Delta V_{SUP}}\left[\frac{1}{\beta}\right] +$	$\frac{\Delta V_{IO}}{\Delta V_{CM}}\left[\frac{1}{\beta}\right] +$	Noise

$$V_o = -V_i \frac{R_2}{R_1}\left[\frac{1}{1 + \frac{1}{(300x10^3)\frac{1}{6}}}\right] + (\pm 300x10^{-6})(6) + (\pm 150x10^{-9})(2 x10^3)(5) + (2)(51x10^{-6})(100x10^{-3})(6) + \approx 0 + \text{Noise}$$

$$V_o = -.99998\ V_i \pm 1.8 \times 10^{-3}\ V \pm 1.5 \times 10^{-3}\ V \pm 61.2 \times 10^{-6}\ V \pm \approx 0 + \text{Noise}$$

Worst Case Error % Full Scale Output‡

0.002% + 0.040% + 0.033% + 0.00136% + ≈ 0% + Noise

‡ Based upon: 4.5 V FSO; 100 mV power supply change on each supply.

Figure 4b. Total Error Band Calculations

error band rather than drift rates, the method of computing the error contribution of each parameter must be modified. The equation in Figure 4b illustrates the errors calculated using the total error band specifications on the OP-27C in Figure 4a. The calculations indicate the relative contribution of each source of error in the worst case with the exception of noise, which is yet to be discussed. As can be seen from the numbers, real world amplifiers can contribute significant errors in a high precision data acquisition system due to their non-ideal characteristics.

Noise and its Effects on Measurement

Noise can have a significant detrimental effect in high precision data acquisition systems. Although one can encounter many different sources of noise and of interference in system design, only certain noises made by the components themselves will be discussed here. Thermal noise, also called Johnson noise, is fundamental to all components. The thermal noise in a resistor can be calculated by use of the formula:

$$e_n = \sqrt{(4kTBR)}$$

Equation 9

where k = 1.38 x 10^{-23} Joules/ degree K (Boltzman's constant), T = Absolute temperature of the resistor, B = the effective "brickwall" Bandwidth over which the noise is to be measured, in Hz, R = Resistance value.

The amount of noise generated by a resistor can be made easier to calculate by remembering that the amount of noise generated by a 1 kΩ resistor in a 1 Hz bandwidth is 4 nV rms. The amount of noise per $\sqrt{Hz}$ generated by any other valued resistor can be computed from this normalized value:

$$e_r = \frac{4nV}{\sqrt{(Hz)}} \sqrt{\frac{R}{1k\Omega}}$$

Equation 10

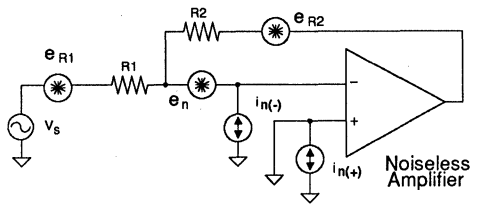
This noise value assumes a one Hz bandwidth. The noise within a wider bandwidth can be computed by:

$$e_R = \frac{4nV}{\sqrt{(Hz)}} \sqrt{\frac{R}{1k\Omega} B}$$

Equation 11

Components other than resistors generate thermal noise. The OP-27 monolithic amplifier is classified by its manufacturers as a low noise amplifier. It is optimized for low voltage noise and requires low source impedances to achieve good noise performance. A plot of the OP-27 noise voltage and noise current characteristics is given in the manufacturer's data sheet. The amplifier's noise is uniform across the higher frequencies, but increases at frequencies approaching DC. This increase is called flicker noise, or 1/f noise.

A thermal noise model of the circuit of Figure 4a is shown in Figure 5. Five noise sources are shown in the model. The amplifier has a voltage noise source e_n and two current noise sources; one associated with each input of the amplifier. Each of the amplifier current noise sources will generate a corresponding noise voltage which is a function of the impedance seen by the current noise source. In addition to the voltage and current noise sources, each of the resistors has a noise voltage source associated with it. The amount of noise contributed at the input of the amplifier by the each of the resistor noise sources is reduced by the loading of the other resistor. For example, consider noise source e_{R2} as having resistor R2 as its source impedance with resistor R1 acting as the load. The noise seen at the input



Noise Model of Amplifier in Figure 4a.

Effective Amplifier Bandwidth

OP-27 typical unity gain frequency = 8 MHz

$$\text{circuit bandwidth} = \frac{f_u}{|A_{CL}| + 1} = \frac{8 \times 10^6}{5 + 1} = 1.33 \text{ MHz}$$

$$\text{effective noise bandwidth B} = (1.33 \times 10^6)(1.57)^{\dagger} = 2.1 \text{ MHz}$$

† The effective noise bandwidth of a single pole, lowpass filter is 1.57 times greater than the 3 dB corner frequency.

Noise Sources of the Model

Amplifier Noise Voltage e_n max (f_0 = 1 kHz) 25 °C = 4.5 nV/$\sqrt{\text{Hz}}$

Amplifier Noise Current i_n max (f_0 = 1 kHz) 25 °C = 0.6 pA/$\sqrt{\text{Hz}}$

} From data sheet specifications

$$e_{R1} = \frac{4 \text{ nV}}{\sqrt{\text{Hz}}} \sqrt{\frac{2 \text{ k}}{1 \text{ k}}} = \frac{5.65 \text{ nV}}{\sqrt{\text{Hz}}}$$

$$e_{R2} = \frac{4 \text{ nV}}{\sqrt{\text{Hz}}} \sqrt{\frac{10 \text{ k}}{1 \text{ k}}} = \frac{12.6 \text{ nV}}{\sqrt{\text{Hz}}}$$

Equivalent Input Referred Noise (Thermal)

$$e_t = \sqrt{(e_n)^2 + \left[i_{n(-)} R_1 \left(\frac{R_2}{R_1}\right)\right]^2 + \left[i_{n(+)}(0)\right]^2 + \left[e_{R1}\left(\frac{R_2}{R_1 + R_2}\right)\right]^2 + \left[e_{R2}\left(\frac{R_1}{R_1 + R_2}\right)\right]^2}$$

$$e_t = \frac{9.1 \text{ nV}}{\sqrt{\text{Hz}}}$$

Total Output Noise (Thermal)

$$E_T = e_t \sqrt{B} \frac{1}{\beta} = \frac{9.1 \text{ nV}}{\sqrt{\text{Hz}}} \sqrt{2.1 \times 10^6} \frac{1}{1/6} = 79 \text{ µV rms}$$

Peak Noise will be much greater.

Figure 5. Noise Calculations

of the amplifier from source e_{R2} will be only that portion of its output which is developed across resistor R1 (assuming the input impedance of the op amp is very high). The noise generated by e_{R1} is reduced by the loading of resistor R2. The amount of noise generated at the input of the amplifier by each of the sources is tabulated in Figure 5. The two current sources each have the same value of current noise. Using the values of the noise sources, the effective input-referred voltage noise of the circuit has been calculated. It must be remembered that the noise sources are uncorrelated and therefore add in root-mean-square fashion. This equivalent noise source then represents the total input referred thermal noise. To obtain the value of the noise at the output of the amplifier which will be input to the A/D converter, the input referred noise is amplified by the noise gain of the amplifier while at the same time taking into consideration the effective noise bandwidth of the circuit.

Arriving at a value for the noise bandwidth of the OP-27 circuit is not as obvious as it might seem. If the noise gain of the circuit in Figure 4a is used to compute the 3 dB signal bandwidth the result will be 1.33 MHz. The effective noise bandwidth of a single pole filter is actually 1.57 times greater than the 3 dB corner frequency. But, above 1.33 MHz the OP-27 gain-phase characteristics are not those of a single pole system, but are more complex. The internal gain-phase compensation of the OP-27 will actually cause gain peaking in the circuit of Figure 4a. The gain peaking will occur at the point where the closed loop gain and open loop gain crossover. Also, at frequencies approaching the unity-gain-crossover of the OP-27, the amplifier gain will differ from the roll off of a single pole filter. The effects of the gain peaking and the complex gain-phase characteristics of the OP-27 above the 3 dB corner frequency make an accurate estimate of the resultant noise difficult. One can use the single pole filter characteristics and can approximate the noise bandwidth of the circuit as being 1.57 times the 1.33 MHz corner frequency (2.1 MHz), but the resultant noise calculation using this bandwidth will yield only a coarse approximation of the actual noise .

Using the assumption that the approximation is adequate, the noise at the output of amplifier has been calculated as shown in Figure 5. The calculated value is the amount of thermal noise in rms volts.

Thermal noise is both white and Gaussian. "White" describes the noise as having equal spectral density at all frequencies. "Gaussian" defines the probability density function which describes the amplitude characteristics of the noise. Gaussian noise follows the Normal Distribution. Therefore, once the rms value of the noise has been determined, the probability of occurance of any value greater than a particular amplitude can be determined. The peak (+ and -) noise associated with a stated probability of occurrence is indicated in the following table:

Probability of Having a higher Amplitude Occurrence	Peak to Peak Amplitude
10 %	3.29 x RMS
1 %	5.15 x RMS
0.1 %	6.58 x RMS
.001 %	7.78 x RMS

Since the peak noise can adversely affect A/D measurements it should be investigated by both analysis and measurement. Minimization of thermal noise in system design is accomplished with the application of three design principles. First, it is good practice to use the lowest resistor values possible (this assumes a voltage amplifier system) limited only by the constraints necessary to meet other system requirements. Second, choose an appropriate amplifier. Some amplifiers, such as the ubiquitous LM324, do not include noise

specifications in their data sheet. If low noise is a system requirement, amplifiers which have no noise specifications are not likely to be an appropriate choice. Also, choose an amplifier which is optimized to work with the source impedance requirements of the system. Bipolar-input amplifiers are generally optimized to work with low impedances as they have lower voltage noise than current noise while FET-input amplifiers are generally optimized for high impedances due to their lower current noise. The optimum choice of amplifier will depend not only on the amplifier, but its associated gain elements and circuit configuration. Analysis of the various possible configurations is necessary to disclose which will be optimum to meet design requirements. Third, one of the easiest ways to reduce the effects of noise is to restrict the bandwidth. System bandwidth should be restricted to only that amount necessary to meet system requirements. This should be done as a matter of good practice.

While only the effects of thermal noise have been discussed be aware of other noise sources (see the reference material at the end of this application note). Note that in the circuit of Figure 4a the effects of the 1/f noise were not investigated. If the system requirements demand the lowest noise possible the effects of the 1/f noise needs to be examined.

The example calculations on thermal noise were done at room temperature. An increase in temperature to 125° C will result in about 1.3 dB greater noise. Last of all, the calculated answers are only theoretical estimates. The calculations provide a theoretical minimum value but the final determinent of design should be in the evaluation of total system function and/or measurement of the actual amount of noise in the system. Remember that the value of the noise calculated provides only a reference point for the minimum amount of noise in the circuit; the actual amount present will never be less than the theoretical amount calculated, but can be more, due to other noise sources which have not been accounted for. For a more thorough discussion of noise as it applies to amplifier design see references 2 through 6 listed at the end of this application note.

Settling Time

Amplifier circuits have limitations which restrict just how quickly they can produce an accurate output signal at the application of a step change of the input signal. For small changes in signal amplitude, the ability of the amplifier to respond is dependent upon its 3 dB upper corner frequency. If the amplifier gain-phase characteristics approximate a single pole response above the 3 dB frequency the output signal will asymptotically approach a steady state output value Vs as defined by the equation:

$$Vo(t) = Vs \left[1-e^{\left(\frac{-t}{\tau_c}\right)}\right]$$

Equation 12

Where the time constant, τ_c, is given as a function of the corner frequency:

$$\tau_c = \frac{1}{2\pi f_c}$$

Equation 13

Settling time is defined as the elapsed time from when the input step voltage is applied until the output signal reaches and stays within a given error band of a steady state value.

If the input step change is large, the slew rate limit of the amplifier will restrict the speed at which its output can change. The limit at which an amplifier can slew is a function of how fast it can charge or discharge its compensation capacitor. The maximum frequency of a given

amplitude that can be faithfully reproduced by an amplifier with a stated slew rate is defined by the equation:

$$f_{max} = \frac{SR}{2\pi Vp}$$

Equation 14

where Vp is the peak output voltage.

When large changes of signal at the input occur, the settling time of the amplifier will be a combination of initial delay, slew rate limited excursion, and small signal settling time as indicated in Figure 6. Note that the small signal settling illustrated in Figure 6 is not that of a single pole system, but is instead representative of an actual wideband amplifier.

A first order approximation of settling time can be estimated for a circuit under the following conditions. First, the signal must not cause the amplifier to enter slew rate limiting. Second, the 3 dB corner frequency of the amplifier must be known and it's roll-off must be at 20dB/decade for at least a decade of frequency above the 3 dB corner frequency. Under these conditions the following equation yields a good approximation to the settling time:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{Vo}{Vs} - 1 \right|$$

Equation 15

where f is the 3dB frequency. To settle to 1/2 LSB at N bits (N = 16 in a 16-bit A/D) the equation can be written as:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{2^N - 0.5}{2^N} - 1 \right|$$

Equation 16

Which can be simplified to the following:

$$t = \frac{(1 + N)(0.11)}{f}$$

Equation 17

Settling time is not readily predicted in other circumstances. It varies with signal amplitude and is as much dependent upon the circuit configuration and circuit components (including things like stray capacitance) as it is upon the amplifier characteristics. An assessment of circuit settling time is often best be obtained from observation of the circuit under applicable conditions.

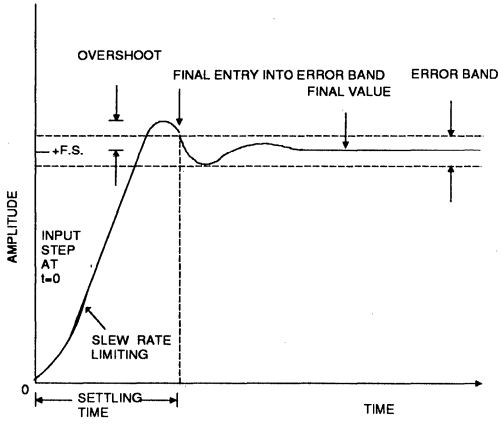
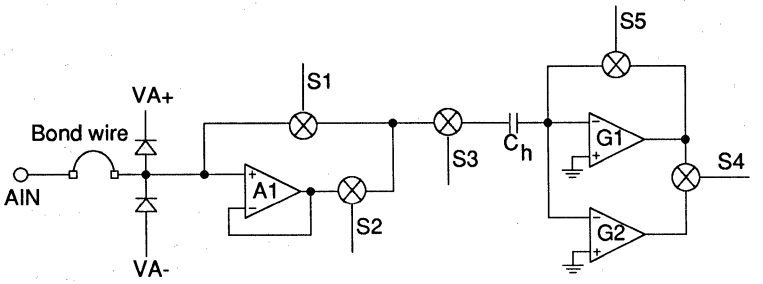


Figure 6.

II. THE CS5016 FAMILY A/D CONVERTER INPUT STRUCTURE

The analog input pin (AIN) of the CS5016 series converter acts as a load to the buffer amplifier output. A good understanding of the internal workings of this pin on the converter will help in the design of an appropriate buffer amplifier.

Figure 7a depicts a simplified circuit diagram of the circuitry internal to the A/D converter as seen from the AIN pin. From the metal pin of the



	S1	S2	S3	S4	S5
Coarse-charge	OFF	ON	ON	ON	ON
Fine-charge	ON	OFF	ON	OFF	ON
Conversion	OFF	OFF	OFF	OFF	OFF

C_h = C_A in Unipolar Mode
$C_{A/2}$ in Bipolar Mode

Figure 7a CS5016 Family Analog Signal Input Model

package a bond wire connects to the semiconductor chip. Clamp diodes on the chip connect to both of the supplies. Under abnormal conditions, excess signal amplitude may forward bias the diodes. The diodes protect the chip from voltage breakdown. Unless the current under such fault conditions is limited, the diodes may short out or the bonding wire may "blow its fuse". The current should be limited to under one hundred mA transient or under 10 mA steady state to eliminate any possibility of damage. Methods of limiting input current to the A/D converter are discussed below. Once the input signal travels beyond the protection circuitry, it sees a buffer amplifier A1, CMOS switches S1, S2, and S3, a hold capacitor C_h, and transconductance amplifiers G1 and G2. To accomplish a complete conversion cycle, the states of the CMOS switches are altered. These state changes cause the effective load at the AIN pin to change dynamically during the three different phases of the conversion cycle. These three phases are called coarse-charge, fine-charge and conversion. An understanding of the function of each of these three phases will explain the reasons for the dynamic change in loading. The conversion phase begins with the activation of the hold command ($\overline{\text{HOLD}}$ goes low).

When hold is activated, the "sample capacitor" of the track-and-hold section of the converter immediately traps a charge on the sample capacitor which is representative of the input signal. The binary representation of the value of the charge is then determined. The number of master clock cycles necessary for this determination to occur is a function of the number of bits of the converter and the particular mode of operation (loopback or asynchronous). The occurrence of the $\overline{\text{EOC}}$ (end of conversion) signal indicates that the conversion time is complete. The converter must then acquire a new sample of the input signal for the next conversion. The coarse-charge and fine-charge times accomplish this. First to occur is the coarse-charge phase. A buffered version of the analog input signal is first connected to the sample capacitor. The input impedance of the buffer is very high and therefore does not load the input signal source. The output of the buffer is connected via switches S2 and S3 to the sample capacitor (switch S1 is open). The buffer (Figure 7a, A1) furnishes the majority of the current necessary to charge the capacitor toward the new voltage value. The buffer therefore reduces the transient current demand from the signal source if the input signal has changed from the value previously stored on the sample capacitor. The sample capacitor is connected to the output of the buffer for six cycles of the master clock (CLKIN)

frequency. At the end of the six cycles the coarse-charge phase is complete. The sample capacitor is then directly connected to the analog input signal for the fine-charge phase (Switches S1 and S3 are closed, S2 is opened). Immediately before being connected for the fine-charge phase, the voltage on the sample capacitor may still differ slightly from the analog input value. This is due to the offset voltage of the buffer amplifier (A1). This offset voltage is typically 50 mV but may be up to 150 mV in the worst case. At the beginning of the fine-charge phase a small transient demand of current from the external signal source may occur as the capacitor charges to its final value. The fine-charge phase will last until the hold command becomes active again. In loopback mode the fine-charge phase lasts nine master clock cycles until the end of track ($\overline{EOT}$) signal reactivates the hold command. When the hold command is activated asynchronously, the fine-charge phase should last a minimum of nine master clock cycles and may continue indefinitely until the hold command is activated.

Simplified models of the impedances seen by the analog input signal are depicted in Figures 7b and 7c. For the conversion and coarse-charge phases, the impedance seen at the AIN pin is the input impedance of the buffer A1. This impedance is approximately 100 MΩ shunted by 15 pF. When

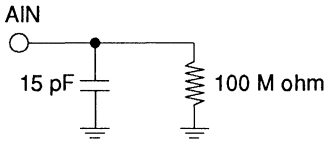
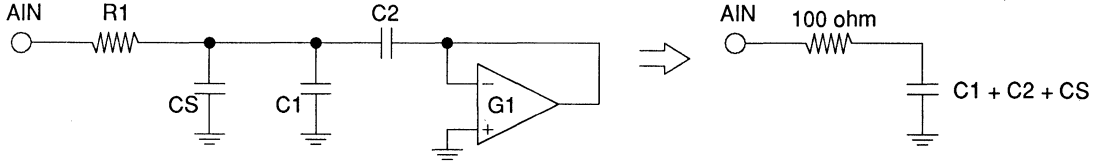


Figure 7b. Simplified Input Model During Coarse-charge / Conversion

in the coarse-charge phase the sample capacitor is charged by the buffer (A1) output. The speed at which the voltage on the sample capacitor can track the input signal is limited to the rate at which the buffer output current can charge the capacitor. The slew rate of the buffer is 5 V/µs when the converter is in unipolar mode and 10 V/µs when in the bipolar mode. The reason for the difference is that the sample capacitor in bipolar mode is only half the value of that in unipolar mode.

The simplified model of the impedance seen in fine-charge is that of Figure 7c. Resistor R1 is the effective resistances of the S1 and S3 CMOS analog switches of Figure 7a. The sample capacitor consists of C2, whereas capacitor C1 and CS are stray capacitance. G1 is a transconductance amplifier with an effective input resistance of about 35 Ω at DC. The slew rate in the fine-charge mode is limited to the rate at



	C1	C2	CS	R1	Gin
Unipolar	170 pF	170 pF	20 pF	100 ohm	35 ohm
Bipolar	85 pF	85 pF	30 pF	100 ohm	35 ohm

Figure 7c Simplified Input Model During Fine-charge.

which the output current of the transconductance amplifier G1 can charge capacitor C2. In unipolar mode the slew rate is 0.25 V/µs. In bipolar mode when the capacitance of C2 is less, the slew rate increases to 0.5 V/µs. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during the conversion cycle or during the coarse-charge cycle since at these times the slew rate of the converter input is faster. It should be noted that in fine-charge, any external impedance on the AIN pin becomes part of the total network and will contribute to the settling time response characteristics.

Also, Figure 7a shows that when switches S1 and S3 are turned on (S2 is off) in the fine-charge phase, the source impedance of the external circuitry connected to the AIN pin actually becomes part of the feedback network of amplifier G1. The external circuitry should offer an impedance less than 400 Ω at frequencies greater than 2 MHz or amplifier G1 may oscillate.

The input circuitry of the analog front end of the A/D converter uses CMOS analog switches which are similar to analog switches available in individual integrated circuits. The resistances of the CMOS switches, such as shown in Figure 7c, exhibit non-linear effects with changes in signal amplitude and frequency. These dynamic changes in switch characteristics are a source of distortion at high frequencies.

III. EXAMPLE BUFFER CIRCUITS

Buffer Circuit Test Method

Several example buffer circuits have been constructed and tested. Evaluation was restricted to dynamic testing at room temperature (25° C). The testing was performed using a CDB5016 evaluation board connected to an IBM compatible computer via a 16-bit parallel I/O card. Signal processing software developed at Crystal was used to evaluate the data. The signal source was a Khron-Hite 4400A Low Distortion Oscillator modified to produce low broadband noise per the article in Reference 1 (Reprints available from Crystal upon request). The oscillator was adjusted to the appropriate full-scale value for each circuit. A frequency of 1.5 kHz was chosen as the test frequency.

The output data from the A/D converter was processed to yield three indicators of dynamic performance. These are:

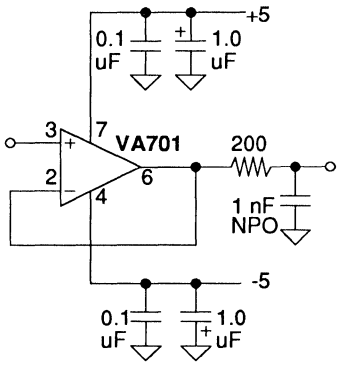
1) S/(N+D): The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (except DC), including distortion components.

2) S/D: The ratio of the rms signal value to the ratio of the rms sum of all harmonics.

3) S/PN: The ratio of the rms signal value to the rms value of the next largest spectral component below the Nyquist rate (except DC).

Benefits of an RC Isolation Network

All of the example circuits show an RC network coupling the output of the buffer to the input of the A/D converter. The 200 Ω resistor and 1 nF capacitor network enhance circuit operation in four ways. First, the network reduces the amount of broadband noise. Second, it decouples the input capacitance of the A/D converter from the amplifier. This reduces the possibility of the amplifier having stability problems driving a capacitive load. Third, the circuit isolates the output of the amplifier from the high frequency pulsed charge effects of the sampling front end of the A/D converter. And finally, the passive network offers a well-behaved low source impedance to the internal transconductance amplifier, satisfying its stability needs. The component values are chosen to have a time constant



Gain	1
Input	1.5kHz, ±3.5Vpk
VREF	3.5 V
S(N+D)	90.7 dB
S/D	100.0 dB
S/PN	103.0 dB

Figure 8 . VA701 Noninverting Amplifier

of 200 ns to provide appropriate settling time when the converter (16 bits) is sampling at 50 kHz. The NPO dielectric characteristic minimizes the effect of voltage coefficient of capacitance which can adversely affect performance at the 16-bit level. Other dielectrics may be adequate while some may result in non-linear capacitance with signal level and therefore introduce distortion. Empirical testing may be necessary to insure whether a given dielectric is adequate for a particular application.

± 5 Volt Supply Op Amp Circuits

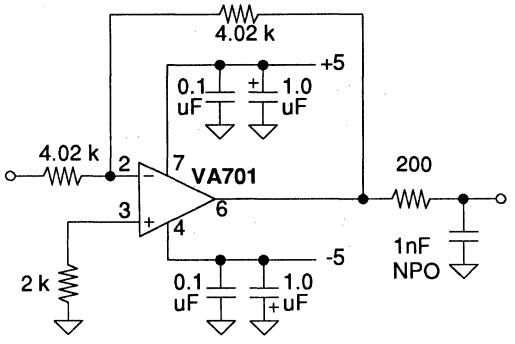
The first example circuit is a unity gain buffer circuit shown in Figure 8. The VA701 op amp (from VTC, Inc.) is designed for operation from ± 5 V power supplies. The input common mode range of the amplifier is specified as ± 3.5 V, therefore the reference voltage for the A/D converter was set to use +3.5 V as its full scale reference value. The circuit yields quite good results when the reduced signal level is considered.

The second circuit, Figure 9, configures the VA701 in the inverting mode. The minimum output voltage swing for the VA701 is specified as ± 3.5 V (2 kΩ load) with a typical range of ± 4.0 V. The voltage reference for the A/D converter was adjusted accordingly. The difference in the amplifier capability between the two signal levels was not very significant. The lower amplitude signal had more noise while the higher level signal had slightly more distortion.

± 15 Volt Supply Op Amp Circuits

Most precision operational amplifiers are specified for operation from ± 15 V supplies. Figure 10 shows an OP-27 used to reduce signal levels of ± 10 V to ± 4.5 V. The performance is excellent. Figure 11 then shows the OP-27 in the non-inverting configuration.

The performance levels being achieved with the OP-27 result from operating the amplifier well within its specifications for input range and output amplitude capability. The Signetics NE5534A worked equally well in both circuit configurations (Figures 10 and 11). Note that low value resistors are used to minimize the component noise in the circuits.



Gain	-1
Input	1.5kHz, ±3.5 Vpk
VREF	3.5 V
S/(N+D)	89.4 dB
S/D	97.6 dB
S/PN	99.6 dB

Gain	-1
Input	1.5kHz, ±4.0Vpk
VREF	4.0 V
S/(N+D)	90.0 dB
S/D	97.3 dB
S/PN	98.9 dB

Figure 9. VA701 Inverting Amplifier

If an OP-27 type amplifier is used, the inverting circuit is preferred for signal processing applications. This is because some brands of OP-27 amplifiers exhibit much higher distortion at frequencies above 10 KHz or so when used in the non-inverting configuration. It may be that the internal bias current cancellation circuitry does not track the input stage well when subjected to the rapidly-varying (high frequency) common mode voltages such as those experienced by the positive gain configuration.

Achieving ± 4.5 Volt Output with ± 5 Volt Supplies

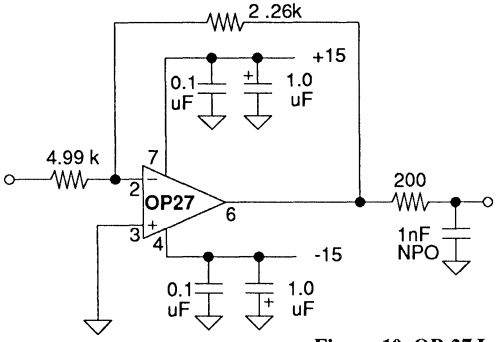
Some amplifier designs may require a minimum number of supplies, yet still want to take advantage of the full dynamic range of the A/D converter when using a 4.5 V reference. The Signetics NE5534A op amp, known to be excellent for audio use, can be combined with a discrete transistor output stage to yield excellent results when using only ± 5 V supplies. Figure 12 illustrates the NE5534A in the inverting configuration, reducing a ± 10 V signal to ± 4.5 V. The OP-27 (without the external compensation capacitor) yielded similar noise and distortion results but had slightly slower rise time when tested with a transient input.

An Instrumentation Amplifier Circuit

Some systems require an instrumentation amplifier front end. One instrumentation amplifier was tested; the AD625C from Analog Devices. The data sheet specifies a maximum nonlinearity of 0.001%. Although the device may have good static linearity, its dynamic performance was well below 16-bit performance. The AD625C, shown in Figure 13, was tested with two different gains. The instrumentation amplifier was tested with a gain of one, and then with a gain of nine. The gain of nine configuration is with the 5 k resistor connected to pins 2 and 15. The data indicates that the part actually has greater distortion (indicative of greater nonlinearity) in the lower gain configuration.

Signal Limiting Circuits

When utilizing op amps with ± 15 V supplies to drive A/D converters with ± 5 V supplies it is possible under certain input conditions for the

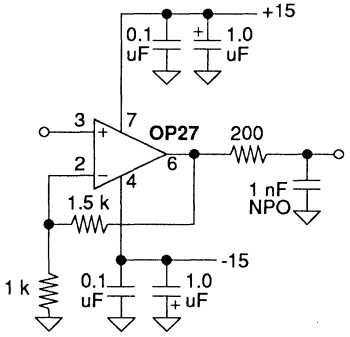


Gain	-0.45
Input	1.5kHz, ±10Vpk
VREF	4.5 V
S(N+D)	91.8 dB
S/D	100.5 dB
S/PN	102.6 dB

Figure 10. OP-27 Inverting Amplifier

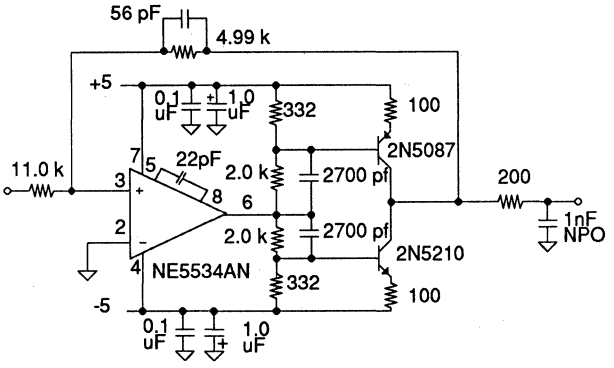
amplifier output voltage to attempt to exceed the supply rails of the converter. As described previously, the converter has protection diodes at the analog input and therefore will clamp the voltage whenever the signal forward biases the diodes. If high current amplifiers are used, excess current from the amplifier may damage the converter. If excess current is a possibility, then the voltage swing of the amplifier must be limited so as to not exceed the supplies of the converter; or some means of current-limiting must be used. Many amplifiers have current limiting circuitry as part of their output stage and will limit their output current if a fault condition exists. Even though the amplifier may protect itself in this manner it may not be desirable from a system performance point-of-view. System measurement accuracy can be degraded due to offset and gain errors which occur as a result of amplifier self-heating.

Several approaches to amplifier output limiting can be used. Zener or diode bounding circuits can be used. Some bounding circuits reduce the circuit gain by reducing the effective feedback resistance when an overvoltage signal exists. Others limit the signal by shunting it to ground when it exceeds the desired amplitude. Reference 6 documents some of these circuits and discusses their strengths and weaknesses.



Gain	+2.5
Input	1.5 kHz, ±1.8 Vpk
VREF	4.5 V
S(N+D)	90.7 dB
S/D	98.0 dB
S/PN	102.3 dB

Figure 11. OP27 Noninverting Amplifier



Gain	-0.45
Input	1.5 kHz,±10Vpk
VREF	4.5 V
S (N+D)	91.7 dB
S/D	99.7 dB
S/PN	103.3 dB

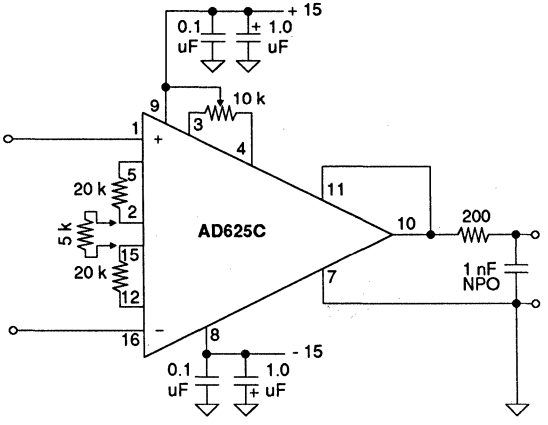
Figure 12. Op Amp with Transistor Buffer Stage

Voltage Clamping via the Compensation Pin

Figure 14 indicates a simple means of clamping available on some op amps. Illustrated is a Harris HA-2600 with diodes connected to its compensation pin (8). The ± 5 V supplies of the A/D converter provide the clamp voltage reference values for the diodes. The output stage of the HA-2600 has unity voltage gain but high current gain. The signal on pin 8 of the amplifier is a low current signal of identical amplitude to the output signal. Limiting of the output signal swing is accomplished by clamping the signal at pin 8 to the desired level. Even if the on voltage of the clamp diodes on the op amp exceed the on voltage of the clamp diodes inside the A/D, the 200 Ω resistor will limit the current to an acceptable level.

A Novel Method to Aid Current Limiting

Another method of protecting the A/D converter from excess signal conditions is illustrated in Figures 15 and 16. The circuits make use of addi-



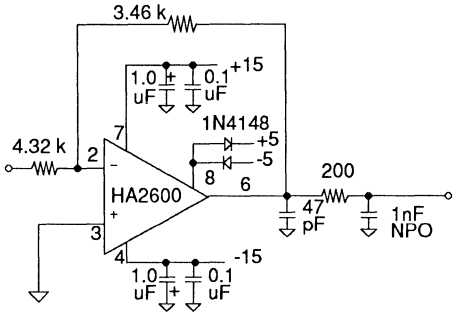
Gain	1
Input	1.5 kHz,±4.5 Vpk
VREF	4.5 V
S/(N+D)	73.1 dB
S/D	81.5 dB*
S/PN	83.7 dB*

* Primarily 2nd harmonic

Gain	9*
Input	1.5 kHz,±0.5 Vpk
VREF	4.5 V
S/(N+D)	74.1 dB
S/D	87.3 dB
S/PN	84.7 dB

* 5 K resistor connected

Figure 13. Instrumentation Amplifier

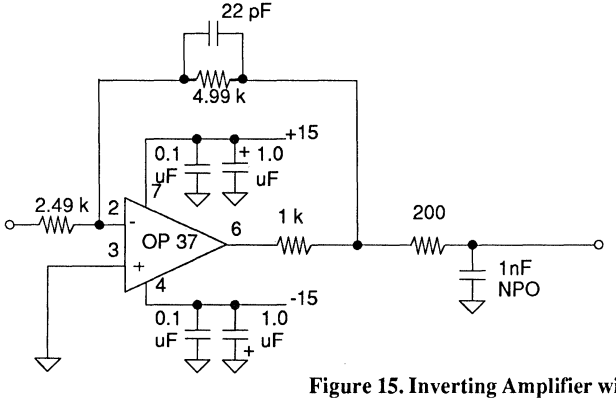


Gain	-0.8
Input	1.5 kHz, ±5.6Vpk
VREF	4.5 V
S/(N+D)	90.5 dB
S/D	97.0 dB
S/PN	98.1 dB

Figure 14. Compensation Pin Clamping

tional series resistance between the op amp and the converter to limit the amount of signal current available. The resistor is placed inside of the feedback loop of the amplifier where the loop gain of the circuit reduces the effect of the 1 kΩ resistor under normal operating conditions. When a fault condition exists, the signal output from the amplifier may attempt to exceed the power supply rails of the A/D converter. Under this condition the current into the A/D converter input will be limited to less than 10 mA by the 1 kΩ resistor.

The added 1 kΩ resistor increases the open loop output impedance of the circuit. This increase in output impedance adversely affects the effective open loop gain of the circuit when driving lower impedance loads. Therefore, it is desirable to take advantage of op amps with higher open loop gains. Decompensated op amps offer greater gain-bandwidth products but with the restriction that they are generally specified to be stable only with higher gain configurations. For example, the OP-37 is specified for operation with a minimum gain of 5 but offers higher open loop gain than the OP-27 (about 15 dB higher at 10 kHz). The circuits in Figures 15 and 16 take advantage of the added open loop gain of the OP-37 yet still meet the requirements for stability demanded by the amplifier. At low frequencies (below 10 kHz) the loop gain of the circuit reduces the effect of the 1 kΩ resistor significantly. At the same time the effective load to the amplifier output (including the 1 kΩ output resistor) is dominated by the feedback resistor. At high frequencies (above 1



Gain	-2
Input	1.5kHz, ±9Vpk
VREF	4.5 V
S/(N+D)	91.2 dB
S/D	97.9 dB
S/PN	99.2 dB

Figure 15. Inverting Amplifier with current limiting

MHz) the impedance of the 1 nF capacitor in the output filter begins to look like a short circuit therefore the load seen by the op amp circuit is dominated by the RC filter network. At the higher frequencies the open loop gain of the op amp is decreasing. The corresponding reduction in loop gain allows the effect of 1 kΩ resistor to begin to take effect, increasing the output impedance to the feedback node. The combined effect of the higher output impedance due to the 1 kΩ resistor and the loading effect of the 200 Ω resistor causes an effective loop gain reduction of about 200/(1000 + 200) or a factor of 6. This gain reduction in combination with the phase compensation of the feedback capacitor allows the circuit to maintain stability while it also provides current limiting under fault conditions.

This application note has discussed the making of a good buffer circuit and has illustrated several examples with relevant test data. For further information on design and dynamic testing of amplifier circuits refer to the following references.

List of References

1. Harris, Steven: "Dynamic techniques test high-resolution ADCs on PCs," Electronic Design, September 3, 1987. (Reprint available from Crystal Semiconductor)

2. "Minimization of Noise in Operational Amplifier Applications," AN15, Precision Monolithics, Inc.

3. "Explanation of Noise," AN164, Signetics, Inc.

4. Whitehead, Richard: "Operational Amplifier Noise Prediction," AN519, Harris Semiconductor.

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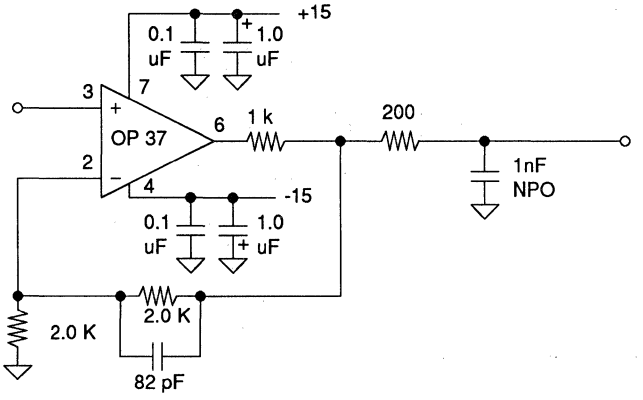
6. Frederiksen, Thomas: Intuitive Operational Amplifiers. McGraw-Hill, New York, 1988.

7. Roberge, James K.: Operational Amplifiers: Theory and Practice, John Wiley and Sons, New York, 1975.

8. Dostal, J.: Operational Amplifiers, Elsevier/North-Holland, New York, 1981



Gain	+2
Input	1.5 kHz,±2.25Vpk
VREF	4.5 V
S(N+D)	92.0 dB
S/D	100.4 dB
S/PN	102.8 dB

Figure 16. Noninverting Amplifier with Current Limiting

Application Note

A Collection of Application Hints for the CS501X Series of A/D Converters

By Jerome Johnston

- Jam ADC into Coarse Charge for High Slew Signals
- Single Control Input Acts as a "Start Convert" Command
- Synchronizing Multiple CS501X Series A/D Converters
- ±5V Input Signal Range Operation

A COLLECTION OF APPLICATION HINTS FOR THE CS501X SERIES OF A/D CONVERTERS

Here are several application hints which extend the flexibility of the CS501X series of A/D converters.

Jam ADC Into Coarse Charge For High Slew Signals

The CS501X family of A/D converters have within their capacitor-based architecture a track-and-hold function. Upon completing a conversion the A/D converter immediately begins to track the input signal. The design is such that the input signal is buffered (internal to the A/D) from the capacitor array for six cycles of the master clock. Then the buffer is bypassed and the array is directly connected to the AIN pin of the converter. This allows the converter to settle to its final value within the accuracy specifications. The period of time that the buffer is connected is known as the coarse charge time. The time when the buffer is bypassed to sample the input signal directly is known as fine charge time. Slew rate capability during coarse charge time is much greater than the slew rate in fine charge. Any step changes of the input signal should occur either prior to or during the coarse charge time. Under normal operation, once the converter has completed the coarse charge time and entered into the fine charge time it will stay in the fine charge state until the $\overline{\text{HOLD}}$ input goes low. When $\overline{\text{HOLD}}$ goes low the charge on the capacitor array is immediately trapped and conversion begins.

In applications which exhibit step changes in the input signal, it is not desireable that the converter remain waiting in the fine charge mode (with its slower slew rate capability). Extending the coarse

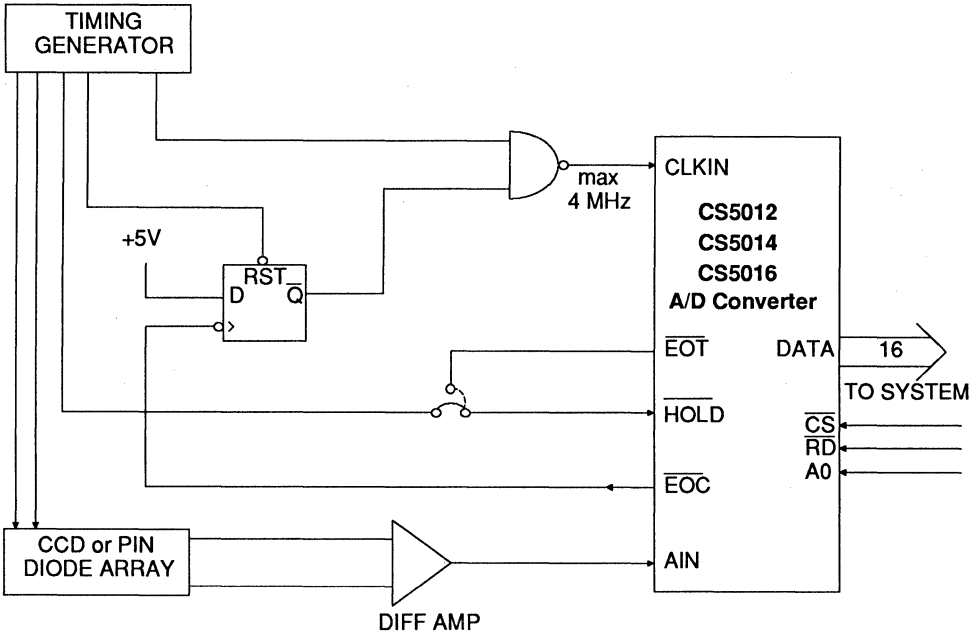


Figure 1. Sample Logic Jams Converter into High Slew Rate Mode

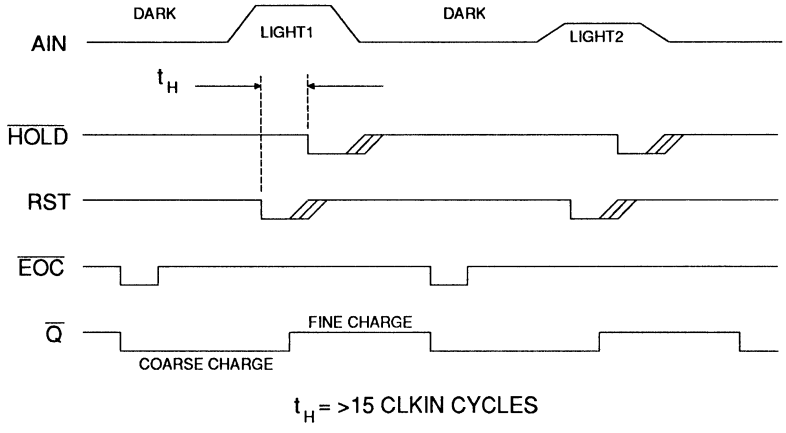


Figure 2. Extending Coarse Charge Time Allows Tracking of Dark to Light Transition

charge time allows the ADC to track high slew signals.

Figure 1 depicts the logic by which the master clock to the converter is stopped during the coarse charge time to lock the converter into coarse charge. At the end of each conversion the End of Conversion ($\overline{EOC}$) signal indicates the end of a conversion and the beginning of a coarse charge time. $\overline{EOC}$ falling toggles the flip-flop, causing its $\overline{Q}$ output to go low. This jams the NAND gate output high which locks the converter into the coarse charge mode until the timing generator circuitry resets the flip-flop.

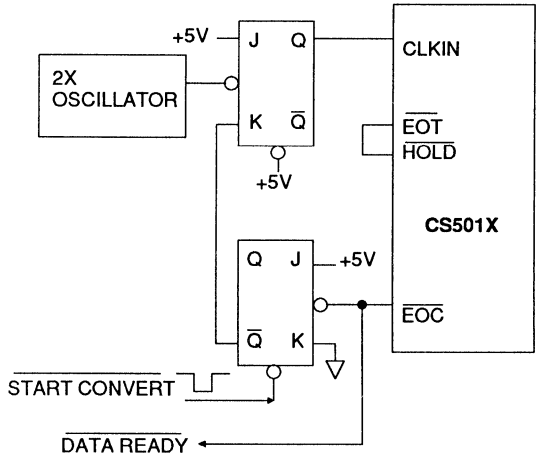


Figure 3.Coarse Charge Jamming with "StartConvert" Control

Figure 2 illustrates the timing of the various signals of the circuit in Figure 1. CCD or PIN diode array outputs exhibit step changes in their signal levels as each array element is selected for output. After each conversion the converter is stopped in the coarse charge mode until the video output signal from a particular element of the sensor array is stable. The clock to the A/D converter is then restarted. The converter then proceeds through the coarse and fine charge times and awaits a $\overline{HOLD}$ signal. If the $\overline{EOT}$ output of the converter is tied to the $\overline{HOLD}$ conversion will begin as soon as the track time is complete.

While this coarse charge jamming circuit is designed to operate with the CS501X series of converters, note that the CS5101 A/D converter offers a CRS/$\overline{FIN}$ (coarse/fine) pin as an input to allow user control of the tracking mode.

Creating a Single "Track, Hold, and Convert" Command

The coarse charge jamming circuitry of Figure 1 is altered to allow a single control line to initiate a sample and convert sequence. First, the $\overline{EOT}$ output from the converter must be directly tied to $\overline{HOLD}$ input. This connection will enable the converter to initiate a conversion upon completion of 9 clock cycles of fine charge (the minimum fine charge time necessary for adequate settling).

At the end of each conversion the $\overline{EOC}$ signal will toggle the flip-flop and lock the converter in coarse charge. The converter will track the input signal in the coarse charge mode until the "start convert" input resets the flip-flop to restart the clock. With $\overline{EOT}$ tied to $\overline{HOLD}$ the converter will proceed through coarse charge, fine charge, and conversion at which time it will stop and await another "start convert" command. Data in the output port will remain available until a new start convert command is issued.

Figure 3 illustrates an example of the "start convert" circuitry using a dual J-K flip-flop. Note that the input clock is twice that required by the converter and that the low time of "start convert" pulse should be less than the conversion time of the converter. The "start convert" signal should be held low during calibration.

Synchronizing Multiple CS501X Series A/D Converters

Simultaneous sampling of several channels is often required. For example, in measurements of the outputs of three-axis magnetometers or three-axis inclinometers it is desireable that all three signals be simultaneously sampled and then converted. Because the CS501X converters offer very good repeatibility from part to part they can yield very good channel to channel measurement correlation even though each channel is converting with its own A/D converter.

Figure 4 illustrates how multiple CS501X series converters can be synchronized, allowing simultaneous sampling. The circuit uses a flip-flop to synchronize a reset (RST) signal common to all of the A/D converters such that the reset signal goes low on a falling edge of the master clock (CLKIN) to each converter. A common $\overline{HOLD}$ command can then be connected to all of the converters to initiate simultaneous sampling. Or, if the synchronous loopback mode of sampling is desired, the $\overline{EOT}$ output from one of the converters can be input to the $\overline{HOLD}$ inputs of all of the converters.

When several converters are galvanically isolated from the digital processing system, synchronazation is useful. The data is passed across the isolation barrier in serial form. If several converters are in the system, normally both SDATA and SCLK signals from each converter are passed across the isolation barrier. However, if the converters are synchronized, the SDATA outputs of several converters can be clocked into serial to parallel registers on the digital side by sending a single SCLK signal across the barrier.

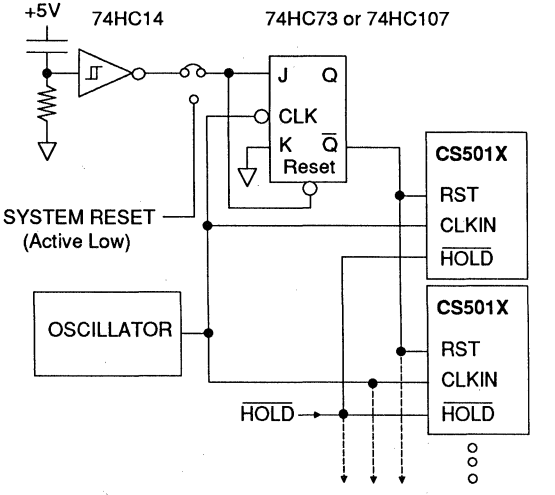


Figure 4. Controlled Reset for Synchronizatoin of Multiple Converters

± 5V Input Signal Range Operation

Some system specifications may require signal levels of ± 5 V. Operating the CS501X series of A/D converters with ± 5 V signals requires a 5 V reference and therefore the supplies have to be raised. The supplies should be adjusted to output voltages in the range from 5.3 to 5.5 volts. The positive and negative supplies should be of equal magnitude and the system connections recommended in the A/D converter data sheet should be maintained.

An easy means of achieving the proper supply voltages is to use LM317L and LM337L regulators. These devices are acceptable as the power requirements of the A/D converter are very low. See Figure 5 for the appropriate resistor values to set the regulator voltages. An alternative is to use LM78L05AC and LM79L05AC regulators with adjustment resistors to increase their output voltages. This is illustrated in Figure 6.

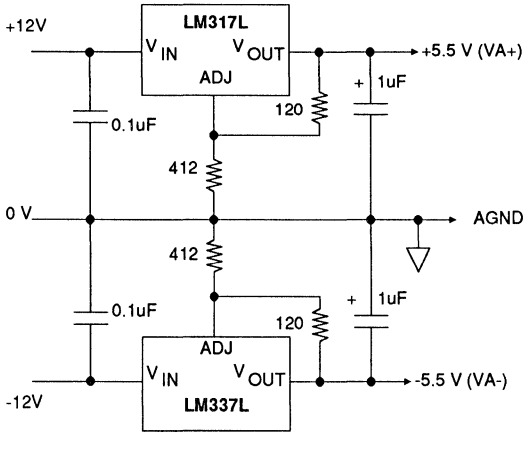


Figure 5. LM317L/LM337L Voltage Regulators

References which output 5 V require a minimum input voltage from 6.5 to 11 volts. This increased voltage is necessary to accommodate the 1 to 6 volt input to output voltage differential needed by the reference. Supply voltages of +12 V or +15 V are common. Care should be excercised to insure

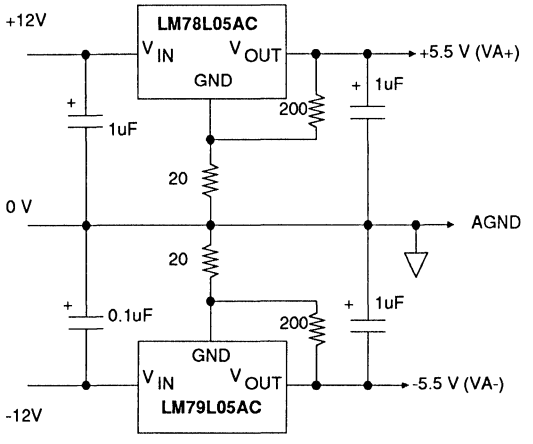


Figure 6. LM78L05/LM79L05 Voltage Regulators

that the voltage reference output does not source current into the A/D converter VREF pin before the power supplies on the A/D are established. One means of insuring this is to add an RC filter in front of the voltage reference as illustrated in Figure 7. This will delay the reference output until the regulated supplies (Figure 5 or 6) for the A/D are established.

With raised supply voltages on the A/D converter, the digital outputs will output logic 1's with a higher output voltage (V_{OH}). To accommodate this increase the digital logic in the system can use 74HC4049 or 74HC4050 logic level translators to restore the logic outputs back to the 5 V level. Alternatively, the logic system (if 74HC logic is used) can also use a supply voltage elevated to the value of the A/D supply. This problem is also eliminated if the ADC is isolated using opto-couplers.

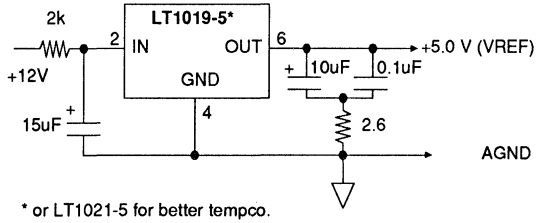


Figure 7. 5Volt Reference with RC Input Delay

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•Notes•

Application Note

CDB5501 to IBM-PC Serial Interface (using BASIC)

By Jerome Johnston and Steven Harris

The CDB5501 Evaluation Board supports easy evaluation of the CS5501 A/D converter. Included on the evaluation board is an RS-232 type line driver (MC145406) which allows the UART-compatible mode of the CS5501 to transmit data to an RS-232 port of a computer.

This application note documents the appropriate configuration of the CDB5501 board to interface to the RS-232 serial port of an IBM compatible computer. A Basic program listing to read the port and display the data in HEX format is included.

The CDB5501 has many jumper selection options. The jumpers should be placed in the following positions to configure the evaluation board in the proper operating mode for RS-232 transmission.

P1 INT CLK
P2 "1" (2.45 MHz clock)
P3 "12" (1200 baud)
P4 "1"
P5 AC mode
P9 "DC"
P11 "BC"

These jumper selections set the evaluation board to operate from the on-board 4.9152 MHz oscillator. The oscillator is divided by two to provide CLKIN signal to the CS5501 at 2.45 MHz. The CS5501 is operating in the Asynchronous Communication mode with an output rate at 1200 baud. The decimation counter is used to provide some "dead-time" between each transmission of two bytes of data.

To connect the DB-25 connector on the CDB5501 evaluation board to the serial input (RS-232 compatible) of the IBM compatible computer a cable must be provided. To insure proper operation the cable should provide straight-through connections for pins 2-8 and pin 20.

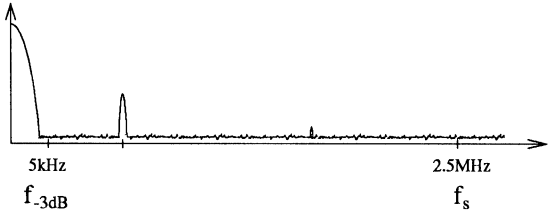
A program listing written in GW Basic is provided. The program reads the input data from the serial port of the computer and then displays the received binary information in HEX format on the computer screen. The software assumes the input is into communications port COM1. The software prompts for the baud rate. A baud rate of 1200 should be entered unless the CDB5501 jumper selection is modified to provide some other baud rate.

The Basic program is not complex. Lines 90-93 give some opening comments with line 94 prompting for the baud rate. Your reply will enter a baud rate for the text string defined in line 96. Line 96 defines a text string which sets up the data format and control line status of the COM1 serial port. In line 100 the text string is then used to open a data buffer for the port into which six bytes are read as defined in lines 150-340. Each character is then converted to HEX characters for display on the screen in line 350. Line 365 then prints the HEX characters on the screen. Use of the port is then terminated by closing the data buffer in line 370. Note that the buffer must be opened and closed to cause the serial port control lines to follow the proper sequence necessary to read each set of six characters. The program will cause the computer to continuously read the port unless line 380 is commented out or deleted. If line 380 is deleted, the program will read six characters and pause with a prompt to continue.

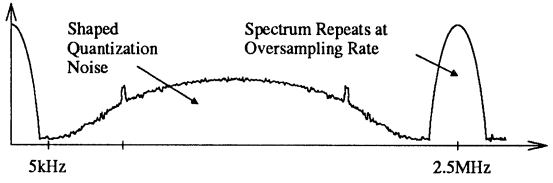
```
90    PRINT "5501COM - DISPLAYS SERIAL DATA FROM CDB5501"
92    PRINT "Crystal Semiconductor      VER1.0  5/8/88 Steve Harris"
93    PRINT "Uses COM1:"
94    INPUT "Baud rate ?",BR$
96    COMFIL$="COM1:"+BR$+",N,8,2,RS,CS,DS,CD"
100   OPEN COMFIL$ AS #1
150   FIELD 1,6 AS D$
300   GET #1,6
340   FOR N = 1 TO 6 STEP 1
350   PRINT HEX$(ASC(MID$(D$,N,1)));" ";
360   NEXT N
365   PRINT
370   CLOSE #1
372   FOR K = 1 TO 10
374   NEXT K
380   GOTO 100
400   INPUT "Quit OR Continue";A$
410   IF A$ = "Q" THEN GOTO 10000
420   GOTO 100
10000 END
```

Delta Sigma A/D Conversion Technique Overview

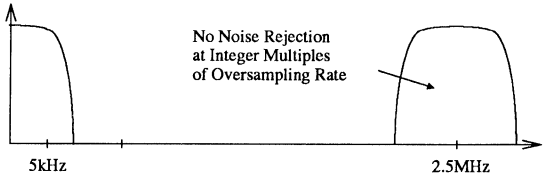
a. Analog Input Spectrum



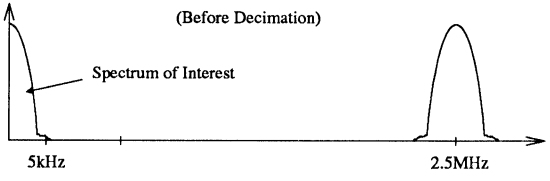
b. Modulator Digital Output Spectrum



c. Digital Filter Response



d. Digital Filter Output Spectrum



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SECTION A

OVERVIEW: DELTA-SIGMA MODULATION

Although developed over two decades ago, delta-sigma modulation has only recently achieved commercial implementation. The technique utilizes oversampling and digital filtering to achieve high performance in both A/D conversion and filtering at low cost. The advent of commercial delta-sigma converters is due in most part to recent advances in mixed analog-digital VLSI technology. Precision analog circuitry can now be integrated on the same chip with powerful digital filters.

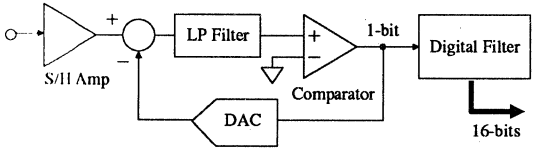


Figure A1. Delta-Sigma ADC

In a delta-sigma ADC, the same digital filter used in the A/D conversion process can perform system-level filtering with performance unachievable in analog form. Therefore, the first commercial delta-sigma converters have been targeted at applications demanding high-performance filtering (high-end modems, digital audio, geophysical exploration, etc).

This application note uses the CS5317 voice band A/D converter for examples. See the end of this application note for implementation details for the CS5317, CS5501, CS5326 A/D converters.

Fundamentals

A delta-sigma ADC consists of two basic blocks: an analog modulator and a digital filter (see Figure A1). The fundamental principle behind the modulator is that of a single-bit A/D converter embedded in an analog negative feedback loop with high open loop gain. The modulator loop oversamples and processes the analog input at a rate much higher than the bandwidth of interest. The modulator's output provides small packages of information (that is, 1-bit) at a very high rate and in a format that the digital filter can process to extract higher resolution (such as 16-bits) at a lower rate.

The delta-sigma converter's basic operation can be analyzed in either the time domain, or (more conventionally) in the frequency domain.

Time-Domain Analysis

The basic operation of a delta-sigma modulator can be understood more intuitively by demonstration. A simple, first-order modulator (that is, a conventional voltage-to-frequency converter) is shown in Figure A2. (Note: a modulator's order indicates the number of orders of analog filtering - or integration - in the loop). Full-scale inputs are ± 1V and three nodes are labeled V_1, V_2, and V_3. The output of the comparator, node V_3, is the output of the loop and is also converted by the 1-bit DAC into plus or minus full-scale (+1V or -1V).

At the differential amplifier, the +1V or -1V is subtracted from the analog input voltage. The result, the voltage at node V_1, is input to the integrator. The integrator acts as an analog accumulator; ie. the input voltage at node V_1 is added to the voltage on node V_2 which becomes the new voltage on node V_2. Node V_2 is then

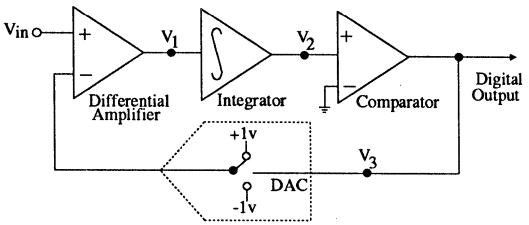


Figure A2. 1st-order Delta-Sigma Modulator

compared to ground. If it is greater than ground, node V_3 becomes +1V; if it is less than ground, V_3 becomes -1V. Each operation occurs once during each clock cycle.

In the example shown in Table A1, all nodes are initially set to zero, and the analog input voltage is assumed to be 0.6V. Since all nodes are identical in clock cycles two and seven, the period defined by cycles two to six will repeat if the analog input remains unchanged. The average value of modulator outputs (at node V_3) during that period, 0.6, yields a numerical representation of the analog input.

Clock Period	V_1	V_2	V_3	Period Avg
0	0	0	0	
1	0.6	0.6	1	
2	−0.4	0.2	1	
3	−0.4	−0.2	−1	
4	1.6	1.4	1	0.6
5	−0.4	1.0	1	
6	−0.4	0.6	1	
7	−0.4	0.2	1	
8	−0.4	−0.2	−1	

Table A1. Modulator Walk-Through

With conventional voltage-to-frequency converters a digital counter is used to extract the information in the VFC's 1-bit output. Pulses are counted over a specified period, effectively creating a digital averaging (or integrating) filter. The final count represents the average analog input value during the integrating period.

Advanced delta-sigma converters use higher-order modulators and more powerful digital filters. For example, the CS5317 uses a second-order modulator. The pattern of transitions in its 1-bit output provides more useful information regarding higher resolution at higher frequencies.

However, a more sophisticated digital filter than a counter is needed to interpret that information. A digital FIR filter is basically a rolling, weighted average of consecutive samples (see Appendix B). An averaging filter weights all samples equally. By applying a more sophisticated weighting function to the 1-bit signal, a digital FIR filter can assemble an N-bit output (with 2^N possible values) *without having to wait for 2^N samples.*

The Charge-Balance Name

Delta-sigma ADC's are also known by other names - sigma delta and charge-balance are two examples. The *Charge-Balance* name derives from the fact that the modulator tries to *balance* the analog input with the DAC's output in the negative feedback loop. The charge injected onto the integrator's capacitor from sampling the analog input (see Figure A2) is therefore balanced by the charge injected by the DAC's output. Modulators have been implemented in both switched-capacitor and continuous-time form.

Frequency-Domain Analysis

Since filtering plays a key role in a delta-sigma ADC, it is easier to understand the converter's operation by analyzing it in the frequency domain.

Overview

An A/D converter's resolution determines its dynamic range (or signal-to-noise ratio). Conversely, one can improve a converter's signal-to-noise ratio and thereby increase its effective resolution. The fundamental concept behind delta-sigma converters is to perform a simple, low-resolution A/D conversion and reduce the resulting "quantization noise" (without affecting the frequency band of interest) using analog and digital filtering.

Quantization Noise

The comparator in the delta-sigma modulator loop plays the role of a 1-bit A/D converter. Any A/D converter can represent a continuous analog input by one of only a *finite* number of codes, giving rise to an uncertainty, or quantization error, of up to ± 1/2 LSB. For a consecutive sequence of samples in a waveform, these quantization effects can be modeled as a random noise source under conditions commonly encountered in signal processing applications. (These conditions hold true for delta-sigma modulators). The rms value of the noise source relative to a full-scale input can be shown to equal - (6.02 N + 1.76) dB, for an N-bit resolution converter. Since this error "signal" is totally random (or uncorrelated with the input) it can be assumed to be white, with its energy spread uniformly over the band from dc to one-half the sampling rate.

As a 1-bit ADC, the comparator in a delta-sigma modulator offers (an almost comical) 7.78 dB signal-to-noise ratio. However, the input signal is grossly oversampled (2.5 MHz in the CS5317), thus spreading the quantization noise over a wide bandwidth (1.25 MHz). The noise density in the bandwidth of interest (5 kHz) is therefore reduced.

Noise Shaping

Analog filtering is used in the modulator loop to further reduce noise density in the frequency band of interest by shaping the quantization noise spectrum. The spectrum of the input signal, meanwhile, remains unaltered. Figure A3 shows a modulator loop with analog and digital circuit differences ignored. The comparator is simply shown as a (quantization) noise source, and the analog filtering, which is simply an integrator, assumes the filter response H(f). If the analog input equals zero, then

$$D_{out} = Q(n) - H(f)\, D_{out}$$

$$D_{out} = \frac{Q(n)}{1 + H(f)}$$

The quantization noise at the output is reduced by the open-loop gain of the integrator. At low frequency, the integrator is designed for high open-loop gain, so that quantization noise is reduced. As shown in Figure A4b, the integrator effectively pushes the quantization noise out of the bandwidth of interest and into higher frequencies. Digital lowpass filtering then removes the quantization noise at the higher frequencies without affecting the low-frequency spectrum of interest.

The spectral characteristics of the analog loop filtering dictates the delta-sigma converter's resolution/bandwidth ratio. Higher-order integrators improve noise shaping and allow for higher resolutions at wider bandwidths. The CS5317 uses a second-order modulator for superior noise shaping.

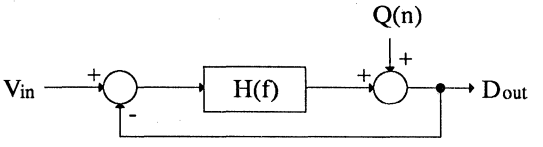


Figure A3. Analog Modulator Model

Digital Filtering

The spectral characteristics of the back-end digital filtering also affects the delta-sigma converter's resolution/bandwidth ratio. Faster roll-off and greater stopband rejection reduces residual quantization noise. Section B offers a detailed explanation of the theory behind digital filtering.

Anti-Alias Requirements

As shown in Figure A4, the input and digital filtering spectrum of any ADC repeats around integer multiples of its sampling rate. A delta-

sigma ADC thus does not provide noise rejection in the region around integer multiples of the sampling rate (± 5 kHz around 2.5 MHz, 5 MHz, 7.5 MHz...). If noise exists in the system in these narrow bands, analog filtering is needed to remove it at the converter's input otherwise it will alias and pass unfiltered to the converter's output.

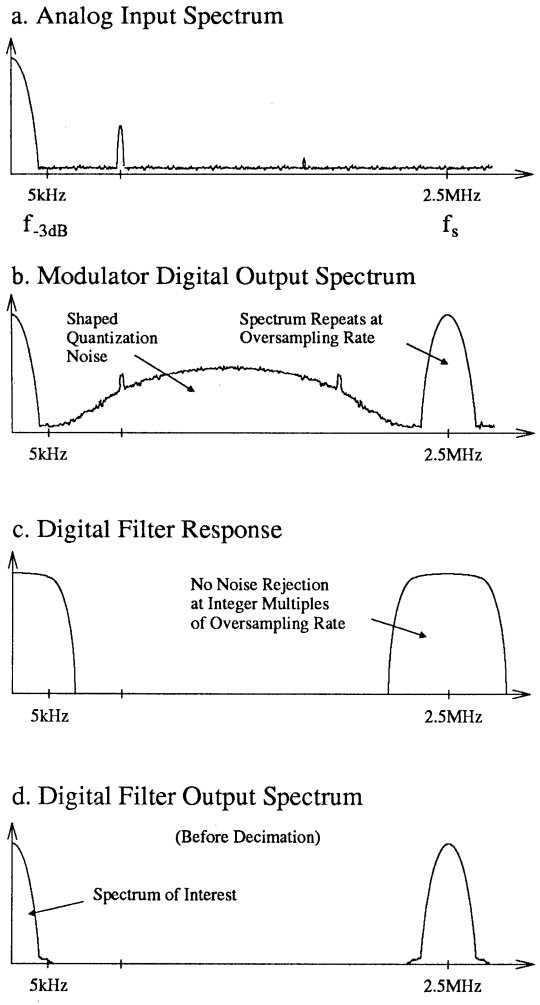


Figure A4. Delta-Sigma Spectral Analysis (Using frequencies taken from the CS5317 A/D Converter)

Since delta-sigma ADC's are grossly oversampled, anti-alias filtering requirements are often trivial. For instance, the CS5317 provides a factor of 500 of oversampling (2.5 MHz/5 kHz). A single-pole, passive RC filter at the CS5317's input is therefore sufficient in most applications.

Decimation

Even though the delta-sigma ADC oversamples and processes analog samples at a frequency well above the bandwidth of interest, it will generally offer its high-resolution output at a much-lower system sampling rate. Any reduction in sampling rate is termed *decimation.* The output can be further decimated at the system level by selectively reading a fraction of the available samples (for instance, every tenth sample). Independent of the decimation ratio, the converter's noise performance (and effective resolution) remains unchanged.

Conversion Accuracy/Performance

Like integrating ADC's and V/F converters, a delta-sigma ADC does not contain any source of nonmonotonicity and thereby offers "theoretically perfect" DNL with no missing codes. The ADC in the modulator is simply a comparator, and the DAC is the positive and negative voltage references. No precision ratio matching is needed as in other medium- or high-speed A/D conversion techniques such as successive-approximation. Useful resolution is limited only by residual quantization noise which, in turn, is determined by coarse analog and high-performance digital filtering.

Linearity error is limited only by imperfections in the input sample/hold. The CS5317 achieves typical nonlinearity of just ± 0.003 % through the use of high-quality on-chip silicon dioxide capacitors with low capacitor voltage coefficient.

SECTION B

OVERVIEW: DIGITAL FILTERING

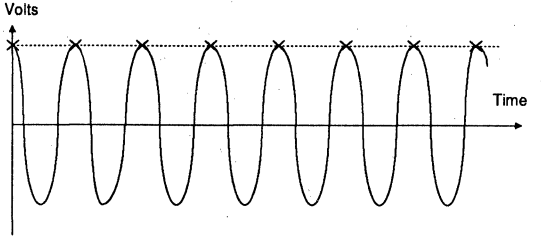
A conventional analog filter implements a mathematical equation using reactive components (capacitors and inductors). A digital filter can implement the same filter equation using two fundamental arithmetic operations: multiplication and addition (or accumulation). A digital filter considers a consecutive sequence of digitized samples a "waveform." It analyzes the relationship between samples, processes the data, and outputs an adjusted waveform.

Digital filters offer ideal stability, repeatability, and potentially perfect performance (linear phase, etc.). Digital filters also remain impervious to environmental conditions, thus providing superior reliability over time and temperature. The major difference compared to analog filters, though, is that digital filters operate on a signal in sampled form.

Sampled-Data Theory

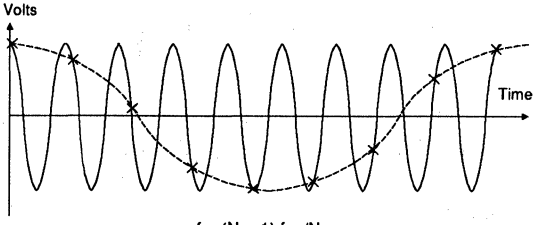
A fundamental phenomenon in sampled-data systems is an effect called "aliasing." Basically, *once an analog signal is sampled, its frequency components are no longer uniquely distinguishable.* Figure B1a shows a special case called "dc aliasing." If a signal is sampled precisely at its fundamental frequency, it will always be sampled at the same point on the waveform. It thus becomes indistinguishable from a dc input. Likewise, a signal at twice the sampling frequency (or any integer multiple of f_S) would appear as dc as well. Figure B1b illustrates a more general case of aliasing. Again, two signals at different frequencies become indistinguishable once sampled.

The effect of aliasing in the frequency domain is illustrated in Figure B2. The baseband spectrum (dc to one-half the sampling rate) also "appears" around integer multiples of the sampling rate, *and vice-versa.* In signal processing applications, anti-



f = f_S (sampling frequency)

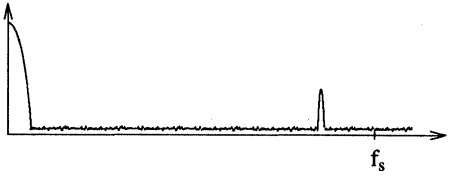
a. dc Aliasing



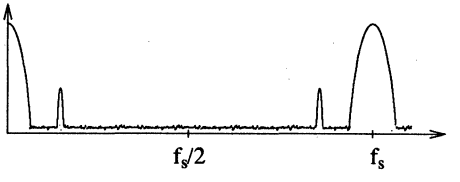
f = (N + 1) f_S /N

b. General Aliasing

Figure B1. Aliasing in Sampled-Data Systems



a. Continuous-Time Input Spectrum



b. Sampled-Data Spectrum

Figure B2. Sampled-Data Spectrum

alias filtering is used to bandlimit the analog signal before it is sampled. This removes out-of-band components which could be mistaken for important information in the band of interest.

Aliasing is critical in digital filtering. A digital filter is incapable of distinguishing signals in its passband from signals aliasing from around its sampling frequency. Its passband spectrum therefore repeats around integer multiples of the sampling frequency. Take for instance the case of dc aliasing shown in Figure B1a. A digital low-pass filter would treat the signal at f_S as a dc input and pass it with no attenuation. Similarly, if the filter would attenuate the lower-frequency signal in Figure B1b by 10 dB, the higher-frequency signal would receive the same 10 dB of attenuation. The higher-frequency signals in both cases could be selectively filtered only by analog anti-alias filtering *before the signal is sampled.*

Sampling rates are usually set high enough that analog anti-alias requirements become trivial (or perhaps eliminated). Higher oversampling ratios offer greater bandwidth to roll off between the passband and sampling frequency. Noise in the digital domain can be analyzed just as it is in the analog domain. Limiting a system's bandwidth will reduce noise and improve dynamic range.

Digital Filtering

The most popular digital filtering technique is averaging. A sequence of digital samples are simply collected and averaged to produce an output. This reduces noise by limiting the effective noise bandwidth. Averaging yields a (sin x)/x (or sinc) filter response as shown in Figure B3. The zeroes of infinite rejection (at f_S/N, $2f_S/N$, $3f_S/N$, etc.) can be strategically placed by selecting f_S and the number of samples averaged, N, to average over an integral number of periods of critical frequencies (50 Hz, 60 Hz, etc.). Of course, this same principle lies at the heart of integrating ADC's, but the averaging is done in analog form. In both cases greater dynamic range (or resolution) can be achieved by increasing integration time. The trade-off is bandwidth.

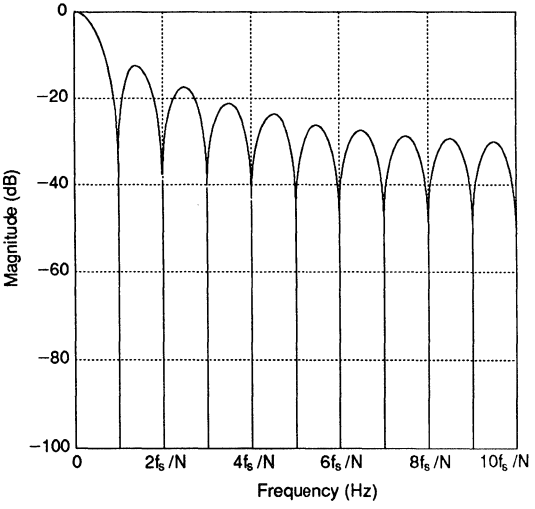


Figure B3. Averaging Filter Response

FIR Filters

Averaging is an elementary example of FIR, or *Finite Impulse Response*, digital filtering. Finite Impulse Response indicates that the filter considers only a *finite* number of inputs to calculate each output. The number of samples determines the *impulse response duration.* For example, a filter which averages ten samples has an impulse response duration of ten. Longer durations indicate more information is considered for each calculation, resulting in a more powerful filter response.

A digital filter's *impulse response* is what determines its filter function. It is basically a weighting function applied to the sequence of samples being considered. The averaging filter is an elementary example of an FIR filter because it uses equal weighting (weight = 1/N where N = # samples). More sophisticated impulse responses extract the information contained in the *relation-*

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ship between samples. Averaging filters ignore this information.

Figure B4 illustrates how an FIR filter actually implements the impulse response. The two basic operations are multiplication (indicated by ⊗) and addition - or accumulation - (indicated by Σ). Filter coefficients a_0 to a_3 represent the impulse response. The three unit delay elements insure that each output is calculated using the current input sample and the three previous samples. The filter's input, x(n), and output, y(n), are digital words of any length. (For the CS5317, x(n) is 1-bit and y(n) is 16-bits). Each digital output requires one complete *convolution.* For the 4th-order filter shown in Figure B4, one convolution consists of four multiplications and the accumulation of the four products.

FIR filters are often described in terms of *taps.* This terminology hails back to analog transversal filters, which were basically analog implementations of the filter in Figure B4. The analog delay elements were termed taps. The number of taps indicated the filter's impulse duration. The longer the duration, the more powerful the filter.

Decimation

Digital filters often operate with input sampling rates well above the bandwidth of interest. This serves to minimize analog anti-alias filtering requirements. The filter's output rate, however, is generally dropped to a more manageable system sampling rate. Any reduction in sampling rate is termed *decimation.*

To illustrate the decimation process lets return to averaging. A filter which collects ten samples and then averages them to produce one output *decimates by ten.* That is, for an input rate of f_S, the output rate is $f_S/10$. Alternatively, one could use a "rolling average." For each input sample received, an output would be calculated using that sample and the nine previous samples. The sampling rate would therefore remain at f_S with no decimation.

The 4th-order FIR filter in Figure B5 exhibits the same filter response as that in Figure B4, but decimates by a factor of four. In this case, only one multiplication is performed per input cycle. Without any delay elements, the accumulator needs four input cycles to complete one convolution. Output samples are therefore produced at $f_S/4$. Decimation clearly relaxes computational complexity.

Decimation does not affect overall signal-to-noise or dynamic range. For this reason, one can decimate the CS5317's 20 kHz output (by selectively reading a fraction of the available samples) without affecting the converter's noise. However, a digital signal is normally not decimated if additional filtering is to be used to increase dynamic range (and resolution). All noise energy in a

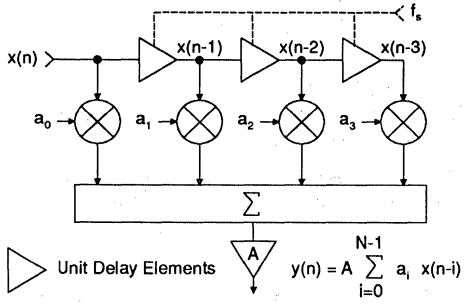

Figure B4. 4th-order FIR Filter

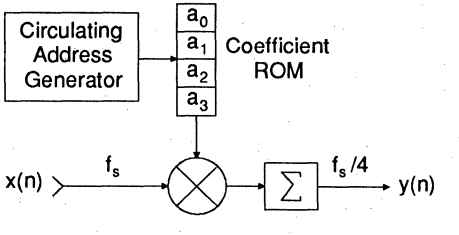

Figure B5. 4th-order FIR Filter with 4X Decimation

sampled signal lies between dc and one-half the sampling rate. Lower sampling rates therefore exhibit larger noise *densities* in the bandwidth of interest for a given amount of noise energy due to aliasing.

FIR Characteristics

The only source of inaccuracy in digital filters is rounding errors due to finite word lengths in the computations. If properly designed, a digital filter will not induce linearity, offset, or gain errors.

Aside from their simplicity, FIR filters' most popular characteristic is their ability to implement perfectly linear phase filters. The effect of every input sample on the output is always seen a *fixed* number of cycles later. This processing delay from input to output is termed the filter's *group delay*, and can be shown to equal one-half the impulse response duration.

Unfortunately, FIR filters can only implement zeroes, no poles. Roll-off is therefore limited. Of course, this limitation can be overcome by cascading FIR filters to produce an extraordinarily long impulse duration. (Fortunately stability is not an issue with FIR filters). The trade-off, though, is an extraordinarily long group delay.

IIR Filters

Infinite Impulse Response filters, on the other hand, can implement zeroes *and poles* to achieve high roll-off. Unlike FIR filters, which use previous inputs to calculate an output, IIR filters also utilize *historical output information* to calculate each new output. In this manner, IIR filters can implement mathematical filter equations with variables in the denominator (that is, poles).

The only drawback to IIR filters is their computational complexity. Since their computations use historical information on their past outputs, *each output must be calculated.* That is, unlike FIR filters an IIR filter cannot decimate to reduce computational complexity. Therefore, IIR filters generally operate with lower sampling rates.

The CS5317 Voice-band A/D Converter Implementation

The CS5317 uses oversampling, decimation, and FIR filtering to implement its digital filter. The CS5317 samples its analog input at 2.5 MHz (for a full-rated 5 MHz master clock). This high oversampling ratio of 500:1 (2.5 MHz sampling/5 kHz bandwidth) reduces external analog anti-alias requirements.

The FIR filter decimates the sampling rate from 2.5 MHz to 20 kHz to reduce computational complexity. The filter features an impulse response duration of 384 x 2.5 MHz and a decimation ratio of 128 (2.5 MHz:20 kHz). Since the filter does not decimate by 384 as shown in Figure B5, multiple convolutions must be in process concurrently. To achieve this, the CS5317 uses three accumulators working from a single 384-word coefficient memory. The three convolutions are spaced to begin and end 128 samples apart. Thus, a new 16-bit output sample becomes available every 128 input samples (for a decimation ratio of 128) whereas each 16-bit output is calculated using 384 input samples (for an impulse response duration of 384).

The CS5501 dc Measurement A/D Converter Implementation

The CS5501 uses oversampling, decimation, and both FIR and IIR filtering to implement its 6-pole Gaussian filter. The CS5501 samples its analog input at 16kHz (for a full-rated 4.096MHz master clock). This high oversampling ratio of 1600:1 (16kHz sampling/10Hz bandwidth) reduces *and most often eliminates* external analog anti-alias requirements.

The FIR filter is used to decimate the sampling rate from 16kHz to 4kHz to reduce computational complexity in the subsequent IIR filter. The FIR

filter response is not especially critical. Its only goal is to reject energy within ±10Hz bands around integer multiples of 4kHz, the IIR filter's sampling rate.

The IIR filter is needed to implement the poles in the 6th-order Gaussian filter and achieve high roll-off of 120dB/decade. Its baseband filter characteristics are shown on page 4. Note that the filter's entire frequency response can be scaled by adjusting the master clock. The converter's sampling rate simply scales accordingly. With its cut-off frequency set at 10Hz (4.096MHz master clock) for maximized settling, the CS5501 offers 55dB rejection at 60Hz. With a 5Hz cut-off, though, 60Hz rejection increases to greater than 90dB. Master clocks as low as 40.96kHz are acceptable, yielding cut-off frequencies as low as 0.1Hz.

The CS5326 Digital Audio A/D Converter Implementation

Linear-phase finite-impulse-response (FIR) filters are used for decimation. The 1-bit, 3.072 MHz outputs of the modulators are decimated in steps of 8, 4, and 2 to yield 16-bit, 48kHz results.

The decimation strategy includes two stages, FIR1 and FIR2, whose primary responsibility is attenuation of quantization noise prior to decimation and aliasing. Modulator out-of-band quantization noise spectral density is very high. FIR1 and FIR2 use 17 and 18-bit coefficients to attenuate this noise, and out-of-band input signals, into the converter noise floor. Filter orders are 27 and 30, respectively.

A third stage, FIR3, performs passband shaping and out-of-band signal attenuation. Passband frequency response errors introduced by the modulator, FIR1, and FIR2 are corrected by FIR3. Overall filter passband ripple is thus reduced to ±0.001dB from dc to 22kHz. The passband compensation function prevents the use of a half-band filter for FIR3. Data is truncated to 16 bits at the output, and this operation is the major noise contributor in the system.

FIR1, FIR2, and FIR3 also combine to provide antialiasing filtering. All analog input frequencies from 26kHz to 3046kHz are attenuated by at least 86dB. Phase response is precisely linear.

CS5326 to DSP56000 Interface

By Clif Sanchez

This application note describes the interface needed to connect the CS5326 to the Motorola DSP56000 Digital Signal Processor.

Since the CS5326 is a stereo delta-sigma oversampled analog-to-digital converter, it requires three clocks: a master clock to sample the analog input, a serial clock to shift out data, and a left/right clock to select the channel. The 74HC590 synchronous counter from TI, along with a couple of inverters, provide all the clocks that the CS5326 requires. The output previous to $L/\overline{R}$, Q_F, is used as a frame sync for the DSP56000 and connects to SC2 which is configured as FSr. For the DSP56000, the FSL bit must be set equal to zero.

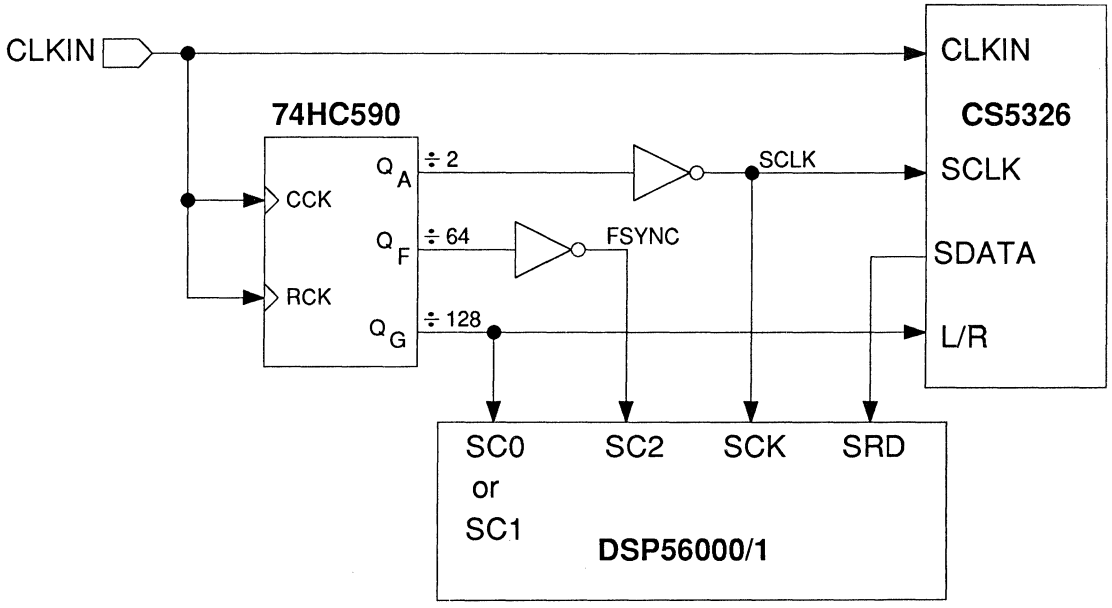

Figure 1. CS5326 to DSP56000 Connection Diagram

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If the DSP56000 serial port is in the synchronous mode, then the serial port transmit and receive sections used the same serial clock. This releases two pins, SC0 and SC1, and one can be configured as an input flag indicating the channel, left or right. They are latched in the DSP56000 at the same time as the MSB (see Figure 2) and can be used to synchronize left/right pairs.

If a synchronous counter is not available, a similar circuit can be constructed from a ripple counter and latch as shown in Figure 3. Since the D flip-flops provide inverted outputs, the output inverters are not needed. But the 74HC4040 ripple counter's clock must be inverted to give it enough time, one full clock instead of one half clock, to settle before the flip-flops latch the data.

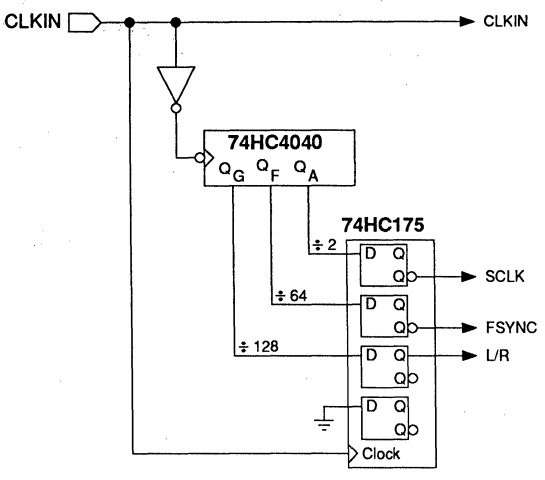


Figure 3. Alternate to 74HC590

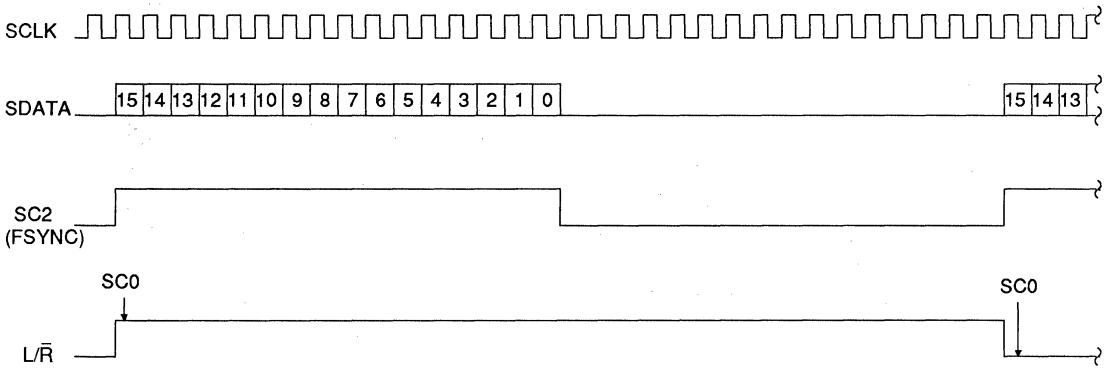
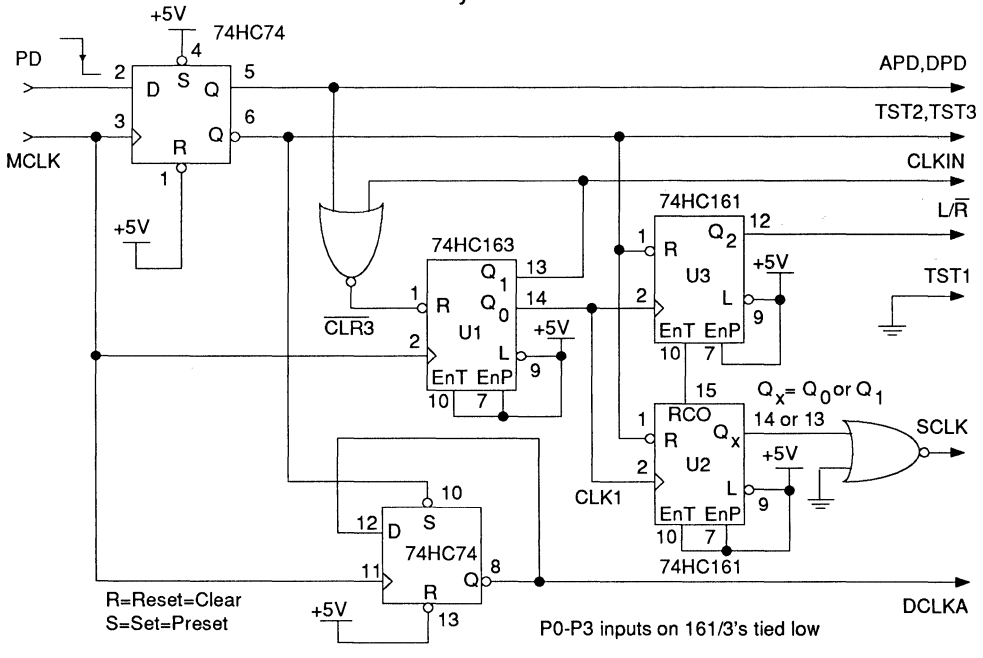


Figure 2. CS5326 to DSP56000 Timing Diagram

Application Note

CS5326/7/8/9 Low Frequency Operation

By Clif Sanchez



This circuit places the CS5326/7/8/9 in test mode 6 and provides clocks with the proper frequencies and relative phases to operate the converter at speeds lower than specification.

In normal operation (i.e., not in a test mode), the CS5326/7/8/9 utilizes a phase lock loop circuit to implement a 3X clock frequency multiplier, the output of which paces the digital filter/ decimators. The limited range of the PLL results in a lower bound to the speed of operation. The ACLKA output is normally connected to the DCLKA input, and it is this clock signal that is the input to the 3X frequency multiplier.

In test mode 6, the 3X multiplier is disabled, and the clock required for the digital filter/decimators is instead received directly on the DCLKA pin. The lower bound on the speed of operation is dramatically reduced (still non-zero due to internal dynamic logic), but the DCLKA signal frequency must be appropriately generated. The requisite frequency is 1.5X the frequency of the CLKIN signal. This ratio mimics the combination of the divide-by-two between CLKIN and ACLKA/DCLKA and the multiply-by-three between ACLKA/DCLKA and the filter/decimators' clock that occurs in normal operation.

The master clock signal MCLK is used to drive a divide-by-two counter to generate DCLKA and a divide-by-three counter to generate CLKIN, and to synchronize the PD (Power-Down) signal. The latter is used to appropriately reset the phase of

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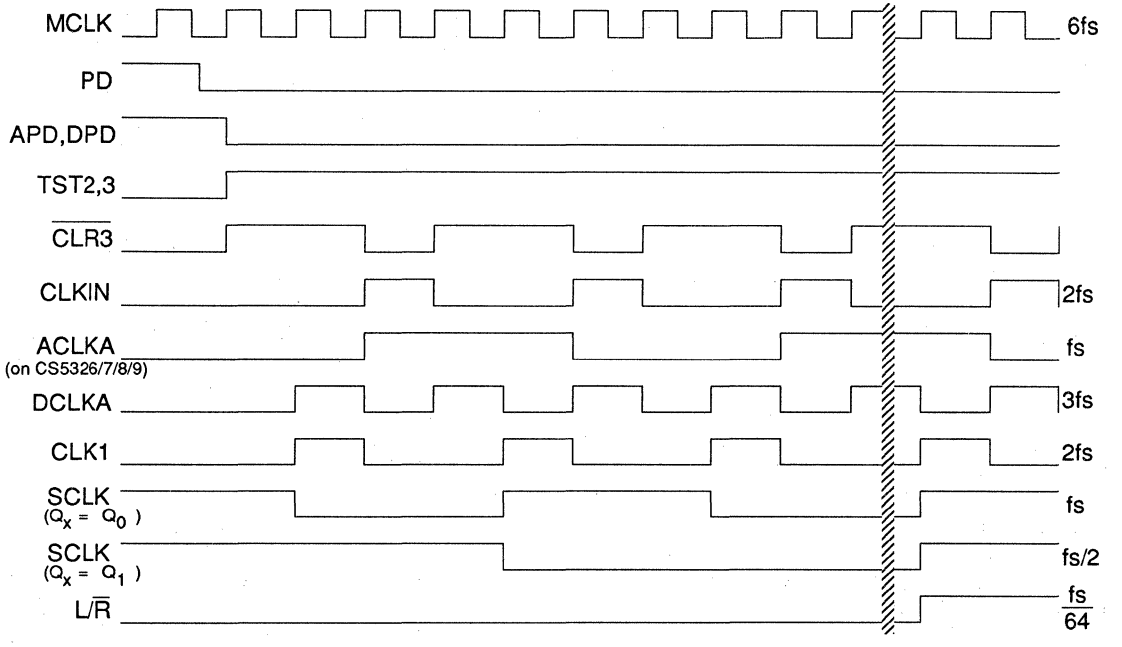
the counters as well as that of the delta-sigma modulators in the CS5326/7/8/9 (this is done through the use of the APD signal). In addition, when PD falls, the complementary output of the synchronizing flip-flop places the converter in test mode 6 through the use of the TST2 and TST3 pins. Note that the CS5326/7/8/9 should not be placed in test mode 6 in the absence of active clocks. In addition to powering down the analog section, APD is used to synchronize the start of ACLKA. DPD initiates an offset calibration and can be controlled seperately from APD. Since APD powers down the reference, DPD should only occur at the same time or (at any time) after APD is released. In test mode 6, *the serial data output during calibration is not all zeros.*

An additional divider is used to generate the SCLK and L/$\overline{R}$ signals which are derived from CLKIN. The SCLK signal may be an inversion of either Q0 or Q1. Using Q1, though, results in an SCLK frequency that can slightly raise the noise floor of the CS5326/7/8/9 through interference effects with the modulators. If receive circuitry speed permits, Q0 should be used to clock out the serial output data.

The resulting phases of the various clocks generated by this circuitry is such that rising SCLK edges and all L/$\overline{R}$ edges occur at falling edges of DCLKA, as can be seen by refering to the timing diagram. Furthermore, 1-bit data transfers between the modulators and the filter/decimators are correctlly timed. In normal mode, this transfer is synchronized by the ACLKA signal. In test mode 6, though, ACLKA is not used (and should be left open), and the correct timing is attained by setting the modulator phase with APD, as described above. As a check, it can be observed that falling edges of ACLKA occur at rising edges of DCLKA.



Notes:
1. $Q_X = Q_0$ is recommended for SCLK to avoid adverse analog interference effects caused by fs/2 signals.
2. L/R is a square wave with edges coincident with SCLK rising edges.
3. fs is analog sampling frequency.

An 18-Bit Dual Channel Oversampling Delta-Sigma A/D Converter, with 19-Bit Mono Application Example

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New York, October 1989

ABSTRACT

The architecture and performance of a stereo 18-bit delta-sigma analog-to-digital converter are discussed. This 28-pin device contains dual delta-sigma modulators and dual digital filters/decimators. Special emphasis is placed on applications examples using the A/D converter in various common audio environments including AES/EBU integrated circuits and digital signal processors. In addition, an example application is discussed in which the dual channel 18-bit part is configured as a single 19-bit A/D converter yielding a dynamic range of 100 dB.

0 INTRODUCTION

The benefits of using digital to store and process audio information are well documented[1]; however, the number of bits required to reproduce the analog signal to an acceptable level is still in flux. Consumer products are standardizing on the 16-bit level[2] while professional equipment manufacturers are asking for more[3,4].

Sec. 1 describes the architecture of the CS5328, a stereo 18-bit delta-sigma analog-to-digital (A/D) converter. Sec. 2 illustrates the performance of the A/D converter under a variety of test conditions. Also discussed is a 19-bit monaural example in which both input channels are tied together and the output words are summed, achieving a dynamic range of 100 dB over the 0-20 kHz audio band. Sec. 3 describes interfaces to common audio environments such as AES/EBU integrated circuits and the Philips I^2S bus, while Sec. 4 discusses DSP interfaces. Sec. 5 discusses a method of attaching the channel indication, left or right, as a tag to the end of the serial data stream.

1 ARCHITECTURE

The architecture of the CS5328, as seen in Figure 1, consists of two one-bit delta-sigma modulators[5] that oversample the analog input at a frequency that is 64 times the output word rate.

Each delta-sigma modulator is followed by a 3-stage FIR filter. Dividing the filtering function into three stages allows for an overall reduction in the number of required taps and incremental decimation to arrive at the output word rate. The output of each channel is latched and multiplexed on the SDATA pin under control of the L/$\overline{R}$ (left/$\overline{right}$) signal. L/$\overline{R}$ also starts the convolution for the FIR filters.

The digital filter response is illustrated in Figure 2 for a 48 kHz output word rate and has a stopband rejection of greater than 86 dB. Since the filter is digital, the frequency response will scale with clock frequency allowing the use of other sample frequencies. Table 1 lists the master clock frequency, passband edge, -3 dB point, and stopband edge for typical digital audio frequencies. An expanded view of the passband showing less than 0.001 dB passband ripple appears in Figure 3 while the transition band is expanded in Figure 4.

2 PERFORMANCE

To test the A/D converter, the analog input of a CDB5328 evaluation board[6] is driven with a signal generator having distortion lower than the A/D converter's noise floor. Any distortion produced from such a setup is assumed to be from the A/D converter[7]. For the FFT tests produced in this paper, the analog input is either a Krohn-Hite Model 4400A or a Brüel & Kjær Type 1051. The data is collected for 1024 consecutive samples. The FFT expects the sample set to be periodic; therefore, if the samples at each end of the sample set do not align exactly, the FFT will produce distortion products that don't exist in the analog input. If the A/D converter were synchronized to the analog input, the end points could be aligned, but to align to the 18-bit level is very difficult. Since the analog input is not synchronized to the A/D converter, the time-domain samples are windowed to avoid discontinuities at the end points. Windowing drives the end points to zero making the first point and last point is the sample set equal. The window is a minimum 5-term which widens the fundamental and harmonics, but doesn't affect the specifications being tested such as S/N+D and dynamic range[8]. Since the noise is uncorrelated, sample sets of points can be averaged to produce a plot in which the noise shape and low level harmonics are distinguishable. The noise spreads itself equally among the frequency bins while the fundamental, harmonics, and tones present, if any, remain unchanged. The data for this paper was gathered with a personal computer which also calculates the FFT[9].

2.1 CS5328 Results

A plot of 100 sample sets averaged, using the previously mentioned setup with an analog input at full scale, appears in Figure 5. A full-scale input is not the optimum test for digital audio since any excursions above full scale cause clipping and large distortions. Digital audio equipment usually defines -10 dB as a maximum signal level to guardband against clipping. A signal 10 dB below full scale would be a better test of an A/D converter for this environment. As can be seen from Figure 6, a -10 dB signal shows slightly better performance than the full scale signal and the harmonics are practically below the noise floor. In Figure 7 the input signal is 80 dB down from full scale and is considered a more difficult test of A/D converter performance[10]. On-chip dither minimizes tones that are normally associated with delta-sigma A/D converters. Figure 8 plots input signal level versus signal-to-(noise+distortion) for a 1, 10, and 20 kHz input signal. This plot illustrates the CS5328's lack of significant distortion for low signal levels over the entire audio band.

2.2 19-Bit Monaural Mode

The hardware illustrated in Figure 9 ties the two analog inputs together and adds the two 18-bit outputs, generating a 19-bit number. Utilizing the CDB5328 evaluation board, the serial data for each channel is shifted into the serial-to-parallel converter during the first 18 serial clocks after L/$\overline{R}$ changes state and is then latched on the parallel output. The serial-to-parallel converter has a separate shift register and latch so the parallel output is valid until the next parallel latch update. On the evaluation board, the left channel data is latched 14 serial clocks before L/$\overline{R}$ falls and the adder circuitry latches the left channel on the falling edge of L/$\overline{R}$. The right channel is latched on the evaluation board 14 serial clocks before L/$\overline{R}$ rises. The two 18-bit numbers propagate through the adder during the latter 14 serial clocks of the L/$\overline{R}$ low time and the 19-bit result is latched when L/$\overline{R}$ rises.

The FFT plot in Figure 10 shows an improvement of approximately 3 dB using summed channels over the single channel approach. The extra bit generates a 6 dB improvement since the signal level is doubled, but the noise from the second channel invokes a 3 dB penalty. Figure 11 illustrates a 19-bit FFT with the analog input down 60 dB. Notice the dynamic range for the 19-bit mono mode is 100 dB over the 0-20 kHz audio bandwidth.

3 TIMING IN AUDIO ENVIRONMENTS

In a typical audio environment such as CD, DAT, or digital audio workstations, the traditional analog front end consists of an 11th-order Chebyshev anti-aliasing filter[11], followed by a sample-and-hold (S/H), and completed by an A/D converter for each channel as shown in Figure 12a. The timing section is required to synchronize the S/H, A/D converter, output multiplexer, and digital signal processing system. If oversampling is utilized, the diagram would look more like Figure 12b in which oversampling by two decreases the anti-alias filter requirements to a 7th-order Butterworth[11]. This anti-aliasing filter provides better group delay characteristics than the traditional approach. In 2X oversampling the A/D converter and S/H must be capable of operating twice as fast as the traditional approach, and the timing section has to accommodate the decimation filter between the A/D converter and the system. Figure 12c shows the analog front end using the CS5328 that oversamples the analog input by 64 generating a sample frequency, Fs, of 64×OWR (output word rate). The CS5328 requires frequencies of 128×OWR for the master clock, 2×OWR for the serial data clock, and OWR for the L/$\overline{R}$ signal indicating the channel: left or right. The anti-aliasing filter requirements are minimized to a single pole passive filter and the group delay characteristics for this approach provide a flat delay over the entire passband. The high frequency clocks required are usually available for other system functions and can be derived from a 74HC590 synchronous counter.

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3.1 Philips I^2S Bus

The "inter-IC sound" bus is a digital audio interface as defined by Philips[12]. The I^2S interface uses word select, WS, (inverted L/$\overline{R}$) to indicate both the channel and start of data. The data is output on the falling edge of SCK one SCK cycle after WS changes state. In the configuration illustrated in Figure 13, the 74HC590 counter is considered the master since it provides the word select and serial

data clocks. The data output by the CS5328 must be delayed one SCLK cycle and is considered 32 bits in length with the receiving device ignoring unused bits as defined by the interface specifications.

3.2 Sony Digital Interface

Both the CX23033 and CXD1211 from Sony Corp. are digital transmitting chips designed to send data in a format similar to the AES/EBU specifications[13]. The CS5328 interface for these chips would be straightforward if the A/D converter was only 16 bits because both interface ICs provide a 16-bit MSB-first format. Figure 14 illustrates the circuitry needed to connect the CS5326, a 16- bit A/D converter, to the Sony chips. Since the CS5238 outputs 18 bits, the 24-bit format of both interface chips must be used, and that format only accepts data LSB first. If the interface chips allowed the specification of the MSB/LSB-first option separate from the 16-bit/24-bit option, the interface would be greatly simplified. Another feature of the interface chips is that the data must be right justified in the channel, whereas the data output from the CS5328 is left justified. Using the 16-bit format as an example, the 16 bits *preceding* LRCK ($L/\overline{R}$) changing state are latched for right-justified data, whereas the 16 bits *following* LRCK changing state are latched for left-justified data. Figure 15 illustrates a method of converting from MSB-first to LSB-first using three cascaded 74HC299 shift registers oscillating between channels. When the right channel is shifting into the shift registers from the A/D converter, the left channel is shifting out of the shift registers to the digital interface chip and vice versa. LRCK for the CXD1211 has the same polarity as the CS5328, high for the left channel and low for the right channel, whereas LRCK in the CX23033 has the opposite polarity. Figure 16 illustrates the flow of serial data for each channel. While the CS5328 is clocking left-channel data into the 24-bit shift register via pin 'A', the shift register is clocking the previous right-channel data out of the $Q_{H'}$ pin and through a multiplexer into the interface chip. In Figure 16b the shift register's shifting direction is reversed and still contains the left-channel data. When the CS5328 starts shifting right-channel data into the shift register via pin 'H', the left-channel data contained in the shift register is clocked out of the $Q_{A'}$ pin and through the multiplexer into the interface chip. The multiplexer is needed to select the appropriate output of the 24-bit shift register to input to the interface chip, whereas the two inputs to the shift register may be tied directly together. The shift register clocks are disabled for eight serial clock cycles since only 24 bits of the 32 bit-periods in a channel are stored. Since the CS5328 outputs zeros after the 18 data bits, the shift register stores six zeros. In the timing diagram shown in Figure 17, the 'z's reflect the stored zeros. All combinational logic can be programmed into a PAL for compactness. To configure the interface chips for the 24-bit format, MSBF is set to zero for the CXD1211, whereas the CX23033 is used in operation mode 1 or, if a microcontroller is present, mode 3 with control register bits D7 and D6 both set to one.

4 INTERFACING TO DIGITAL SIGNAL PROCESSORS

Digital signal processors are used extensively in digital audio environments[14]. Although the digital signal processors, DSPs, discussed below are not an exhaustive set of DSPs capable of handling greater than 16 bits, they do illustrate the circuitry needed to interface to common serial ports.

4.1 Motorola DSP56000

The interface for the DSP56000 is straightforward as shown in Figure 18 with the timing diagram appearing in Figure 19. The counter needed for the various timing signals on the CS5328 provides other divided outputs that can be used by the DSP56000. The counter output previous to L/$\overline{R}$, FSYNC, is twice the frequency of L/$\overline{R}$ and can be used to indicate the beginning of a word. This output will rise concurrently with L/$\overline{R}$ changing state; however, FSYNC will fall after the 16th data bit is output. This is not a concern since the DSP56000 only uses FSYNC to start a serial data transmission and stops transmission when the specified number of bits are received. The DSP56000's serial port is configured to receive 24 bits (WL1,WL0 = 1,1), normal operation (MOD = 0), continuous clock (GCK = 0), and word-length frame sync (FSL1 = 0). If the transmit and receive ports are synchronous (SYN = 1), L/$\overline{R}$ can be used as a serial port flag indicating the channel. Section 5 has more information on the serial port flag.

4.2 Texas Instruments TMS320C30

The TMS320C30 has an interface similar to the DSP56000, with the exception of serial port flags. Figure 20 shows the interface diagram and Figure 21 illustrates the timing. If L/$\overline{R}$ must be known to the DSP, one of the alternate methods described in Section 5 must be employed. The interface diverges from previous TI DSPs but has become more flexible in the process. For the serial port, the variable data rate mode with 24 or 32 bits is utilized. In this scenario, FSR goes active concurrently with the MSB of the data. (In fixed data rate mode, FSR goes active one CLKR cycle before data.) The DSP also inputs the programmed number of bits after FSR indicates the start of serial data transmission. The polarity of CLKR and FSR are programmable, thereby eliminating one inverter from the previous DSP interface.

4.3 AT&T DSP32/DSP32C

The DSP32 incorporates the data skewing technique utilized in the Philips I^2S interface although there is no provision for stereo. The delay is one ICK (serial data clock) cycle on the ILD pin. ILD is a word sync as opposed to an WS signal which indicates the channel: left or right. The DSP32 accepts 32 bits, whereas the DSP32C can accept 24 or 32 bits, and both latch data on the rising edge of ICK. As with the two previous DSPs, ILD is only used to start serial data transmission. Figure 22 shows the connection diagram while Figure 23 illustrates the timing.

5 CHANNEL INDICATION

Many systems do similar processing to both left and right channels; therefore, the DSP may not need to know which channel it is currently operating on. The channel indication, L/$\overline{R}$, may be connected to the A/D converter and digital out or D/A converter, thereby synchronizing the input and output, without connecting to the DSP. However, if the processing is different for each channel, the DSP must know which channel it is operating on. As this function is only needed at initialization, an interrupt line could be utilized, with the interrupt being disabled after synchronization is achieved. This method requires a dedicated interrupt line which is usually in short supply. Another common method is to map L/$\overline{R}$ to a memory location allowing the DSP to read that location while in the serial

port service routine, thereby determining the channel. This method requires address decode logic and a high impedance latch to connect L/$\overline{R}$ to the data bus. A third method connects L/$\overline{R}$ to a general purpose input pin on the DSP if any exist.

If the serial port transmitting and receiving sections are synchronous on the DSP56000 from Motorola, two pins are liberated and can be configured as serial port flags. One of these flags can be utilized to capture the L/$\overline{R}$ signal. As shown in Figure 19, the SC0 flag is latched concurrently with the MSB of the serial data. This flag can be tested on initialization to determine the channel.

Since all the DSP serial ports mentioned require a minimum of 24 bits, and the CS5328 is only 18 bits, 6 trailing bits are unused. If L/$\overline{R}$ is appended to the serial data, the DSP could read the lower bits which identify the channel. The DSP could subsequently mask the lower bits or ignore them since they appear as a DC offset at a minimum of the 19-bit level. The circuit in Figure 24 appends L/$\overline{R}$ to the serial data stream by ORing L/$\overline{R}$ with the zeros output after the 18-bit serial word. The alternate circuit provides a single-chip-package implementation that multiplexes between SDATA and L/$\overline{R}$. Since the CS5328 outputs 18 bits, a flip-flop is needed to delay the rising edge of the Q_F (which rises after the 16th bit) until the 19th bit. A benefit produced by this configuration is that a larger-divide output of the 74HC590 can delay the L/$\overline{R}$ "tag" information until later bit times making the DC offset less significant. Figure 24 shows two configurations for adding the L/$\overline{R}$ tag to the data. In the "bit-19 tag" configuration, the L/$\overline{R}$ tag immediately follows the data, whereas in the "bit-21 tag" configuration the tag doesn't appear until the 21st-bit position. Figure 25 illustrates timing for the "bit-21 tag" configuration. Notice that the left channel data is followed by two zeros, then twelve ones; therefore, the first "one" of the channel tag is in the 21st-bit position. If the DSP's serial port is configured for 32 bits, a "bit-25 tag" could be generated by using the Q_E output of the 74HC590 counter as the clock input to the flip-flop.

6 CONCLUSION

The architecture and performance of the CS5328 18-bit dual channel delta-sigma A/D converter were discussed along with detailed interface and timing diagrams to AES/EBU chips, the I^2S bus, and a number of DSPs. A method of adding a channel identifier to the serial data stream was also explored.

Low input signal levels were shown not to degrade performance, and an example application using both 18-bit channels to generate a single 19-bit part was shown to improve the dynamic range to 100 dB over the audio band.

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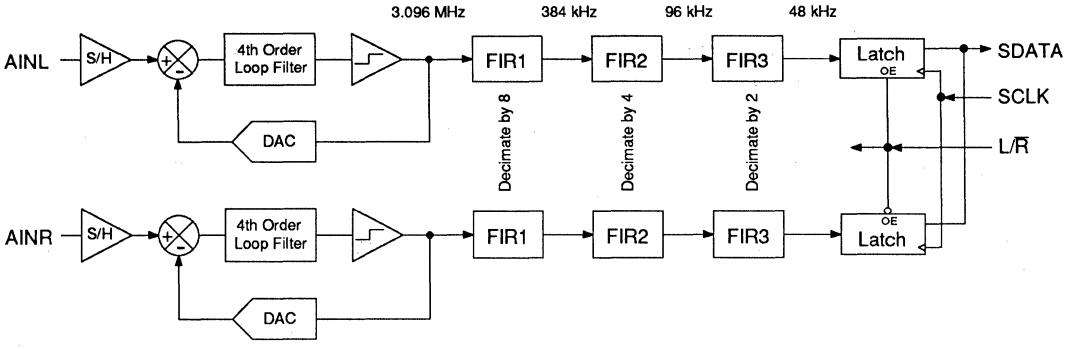


Figure 1. CS5328 Block Diagram

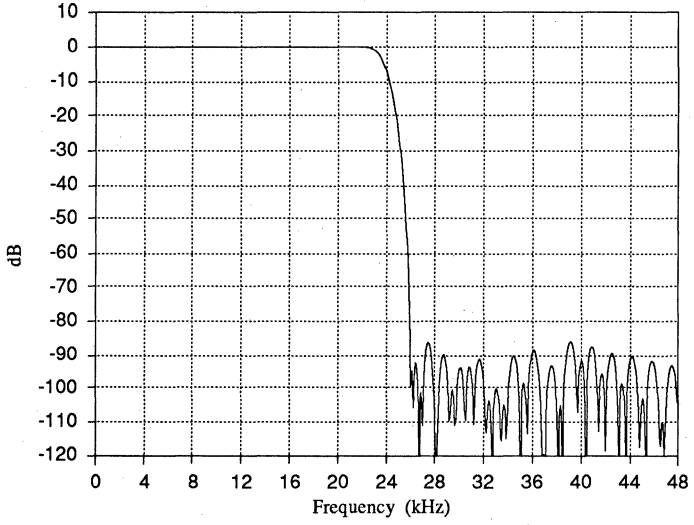


Figure 2. Frequency Response

Output Word Rate	CLKIN Frequency	Passband Edge	-3 dB Point	Stopband Edge
32 kHz	4.096 MHz	14.5 kHz	15.6 kHz	17.3 kHz
44.1 kHz	5.6448 MHz	20.0 kHz	21.6 kHz	23.9 kHz
48 kHz	6.144 MHz	21.8 kHz	23.5 kHz	26.0 kHz

Table 1. Audio Output Word Rates

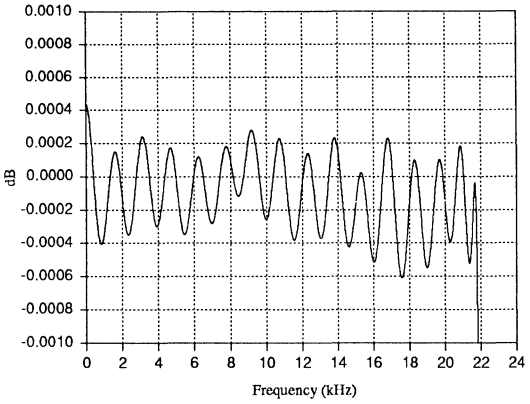


Figure 3. CS5328 Passband Ripple

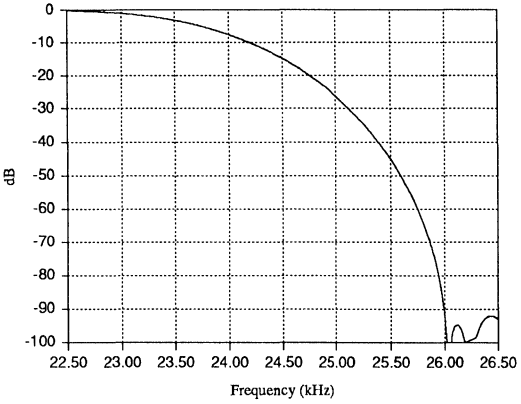


Figure 4. CS5328 Transition Band

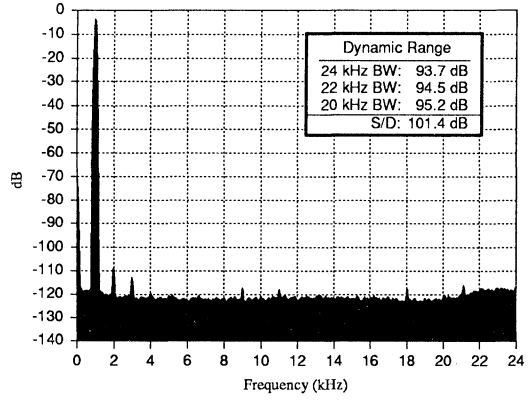


Figure 5. CS5328, Full Scale Analog Input

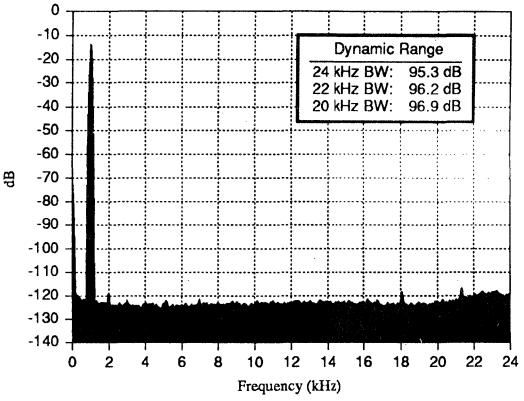


Figure 6. CS5328, -10dB Analog Input

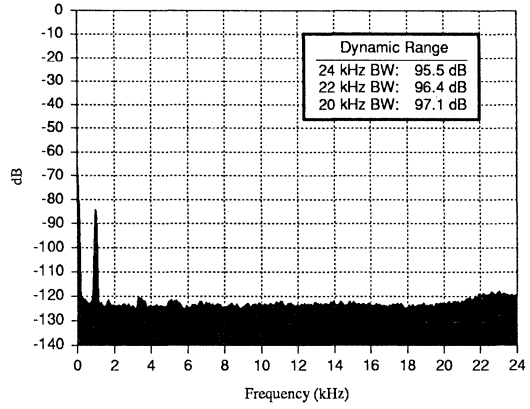


Figure 7. CS5328, -80 dB Analog Input

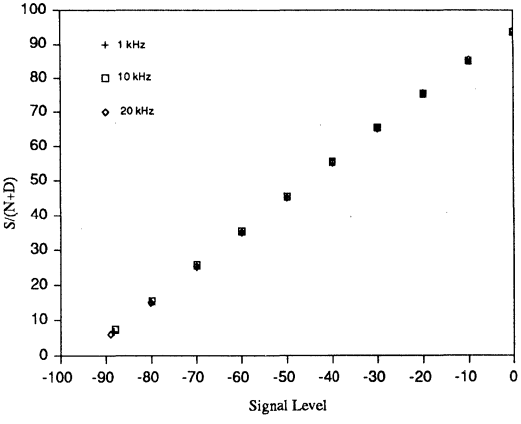


Figure 8. Signal-to-Noise vs. Signal Level

12

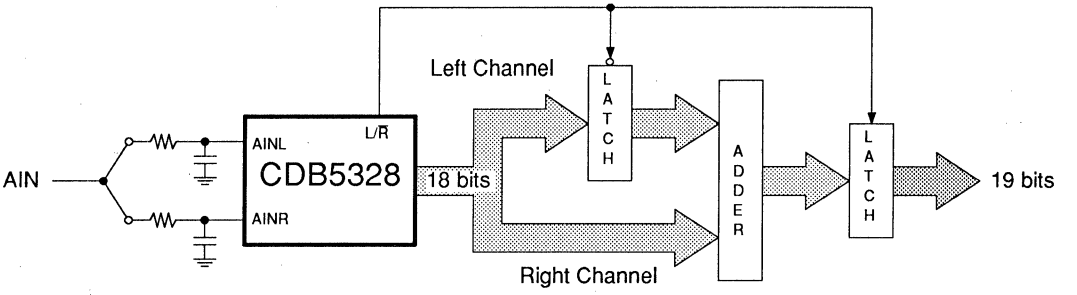


Figure 9. 19-Bit Hardware Configuration

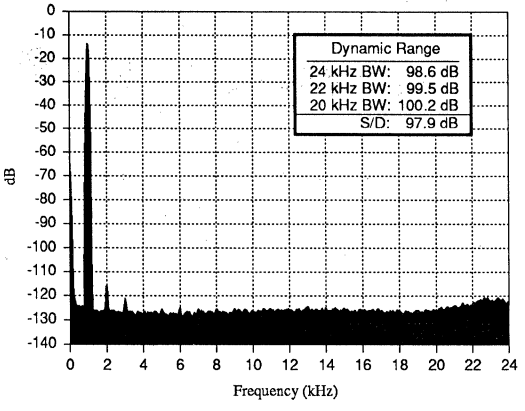


Figure 10. 19-Bit FFT, -10dB Analog Input

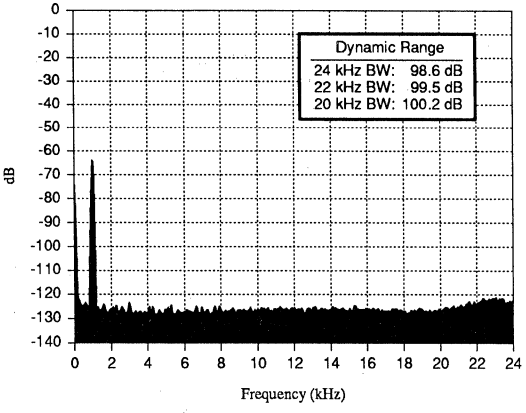
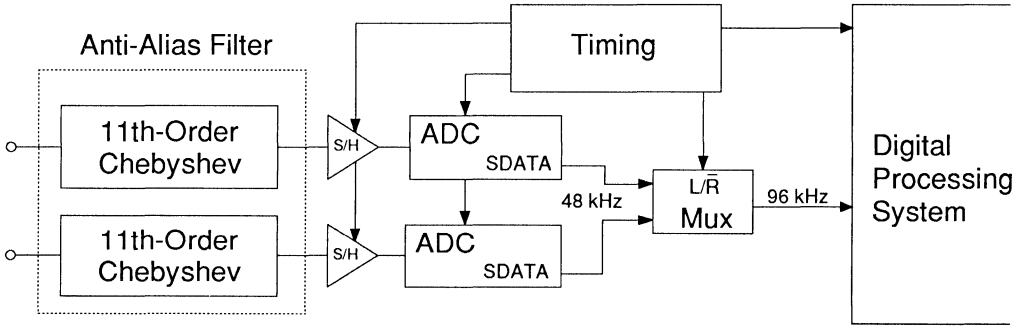
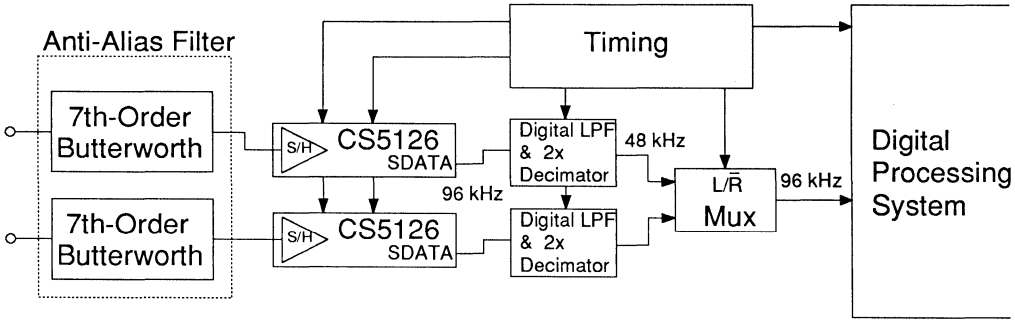


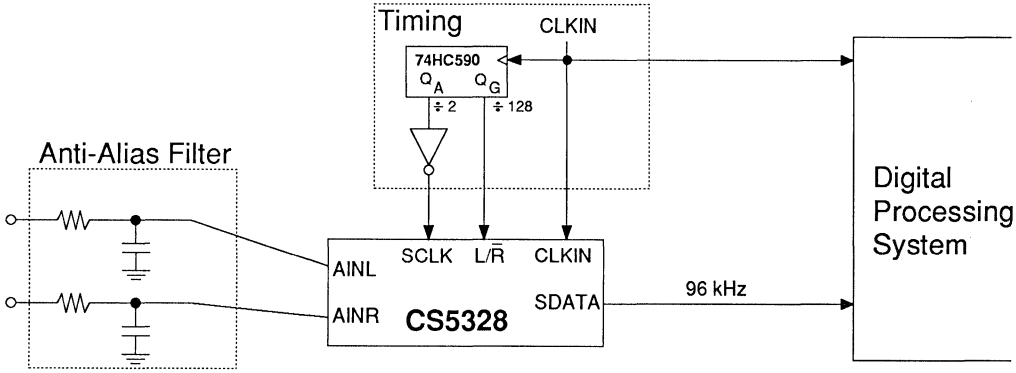
Figure 11. 19-Bit FFT, -60dB Analog Input



a. Traditional Approach



b. 2x Oversampling



c. 64x Oversampling

Figure 12. Analog Front End

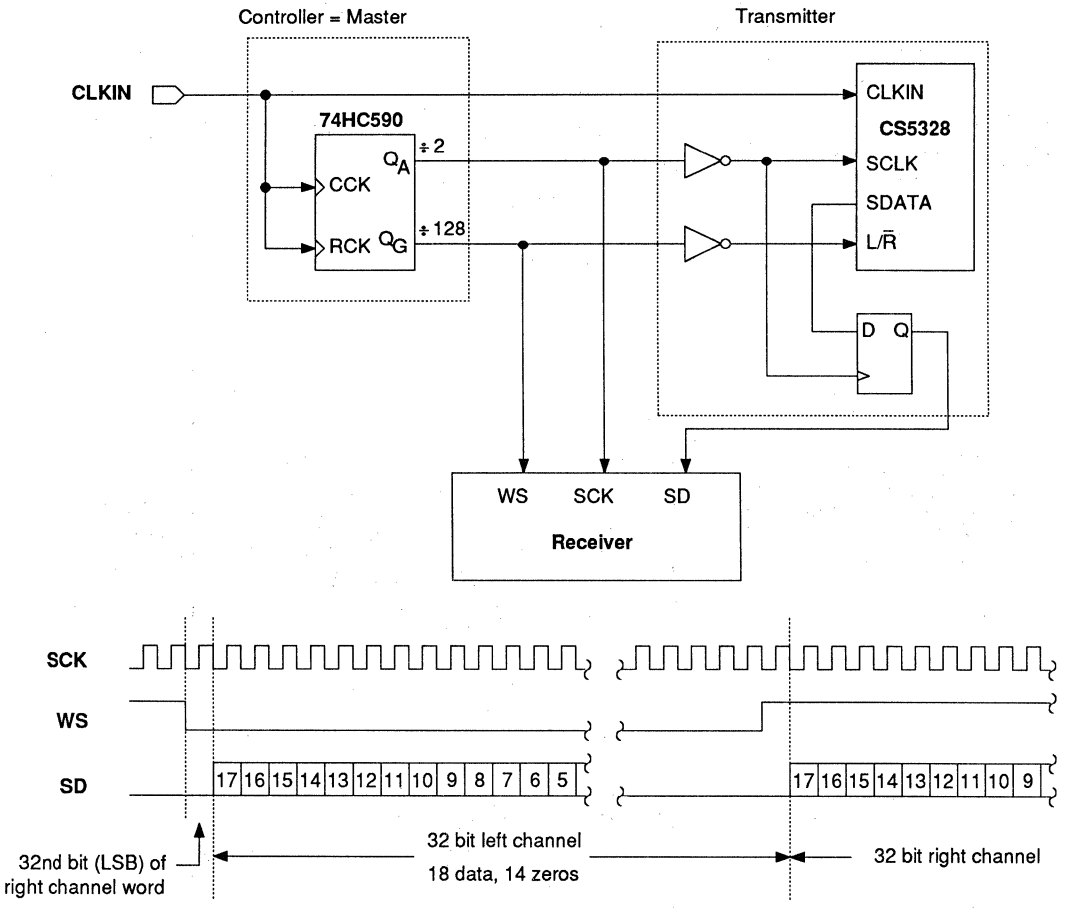


Figure 13. Philips I^2S Bus

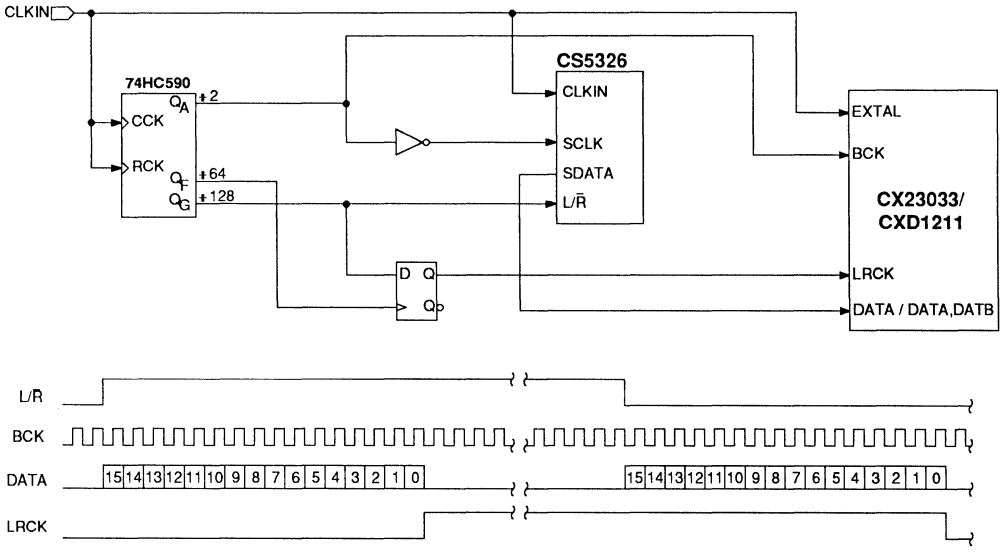


Figure 14. Sony Digital Interface, 16-bit Format

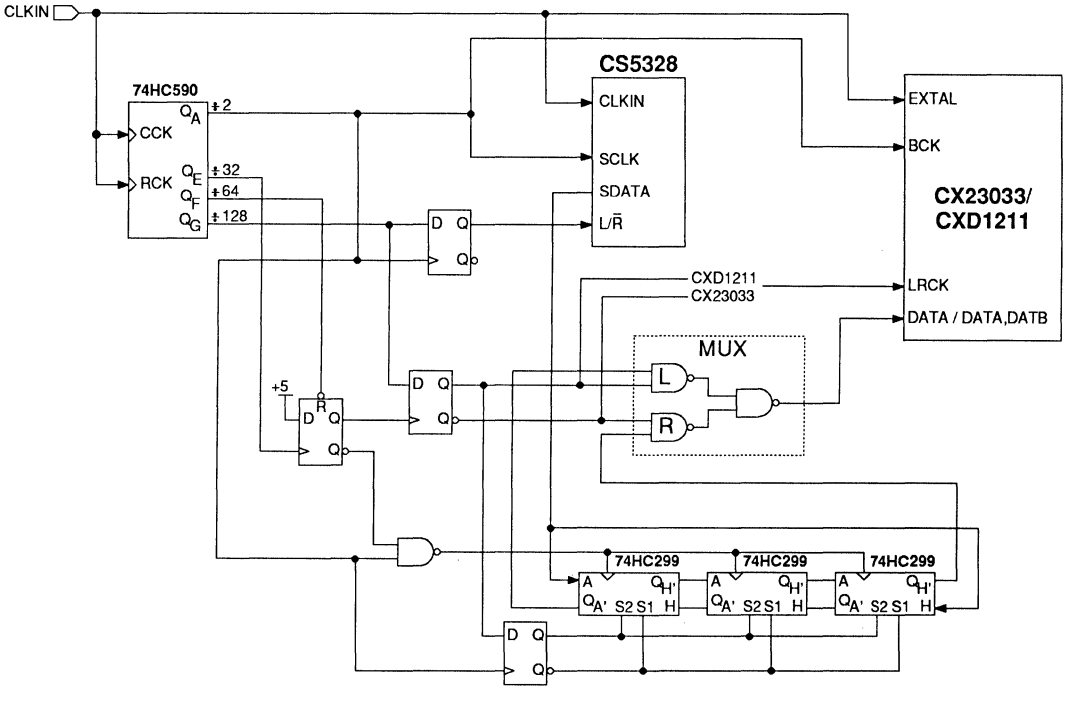
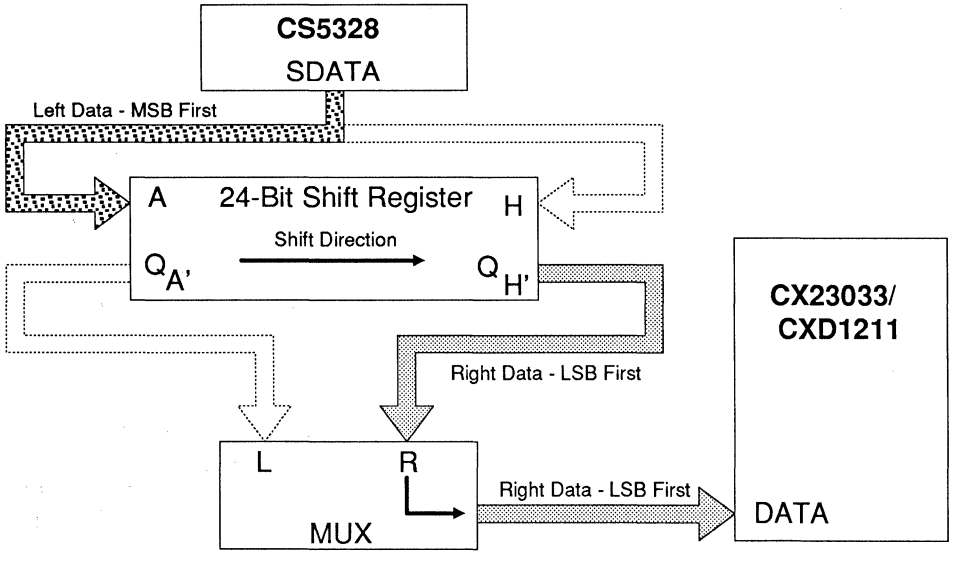
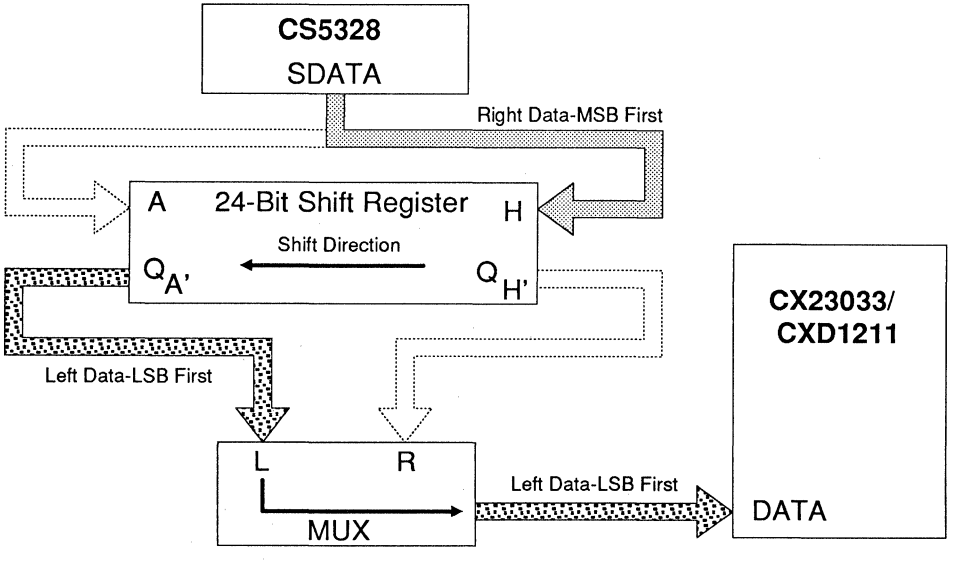


Figure 15. Sony Digital Interface, 24-Bit Format



a. First Channel



b. Second Channel

Figure 16. Sony Interface Serial Data Flow

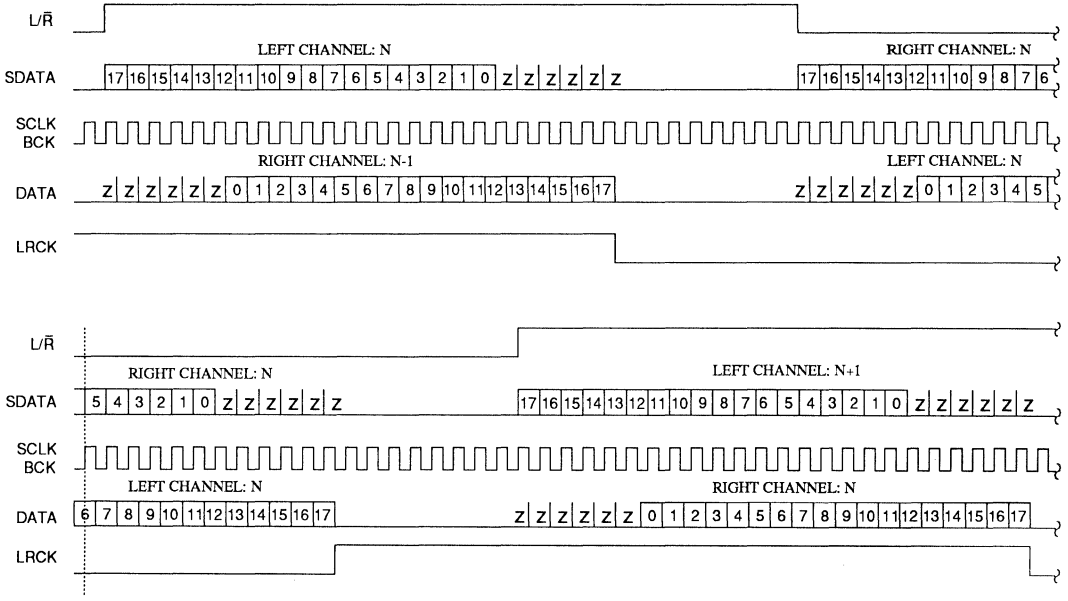


Figure 17. Sony Digital Interface Timing Diagram, 24-bit Format

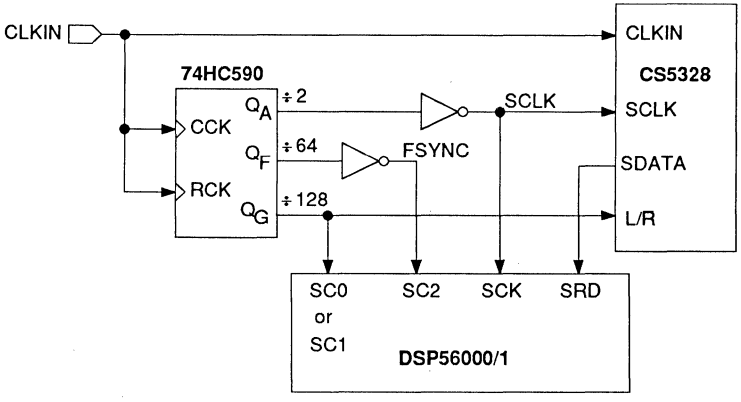


Figure 18. DSP56000 Connection Diagram

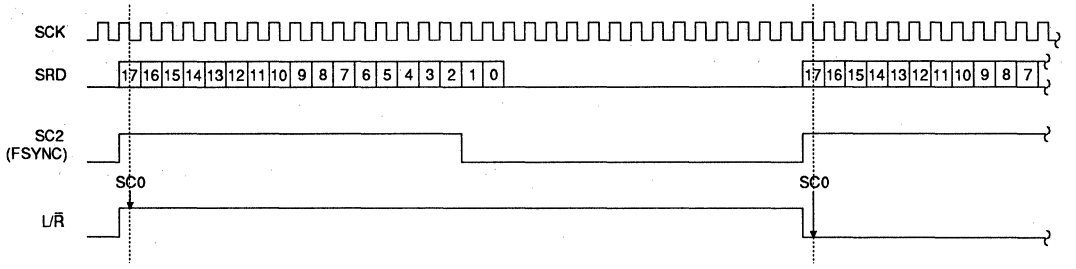


Figure 19. DSP56000 Timing Diagram

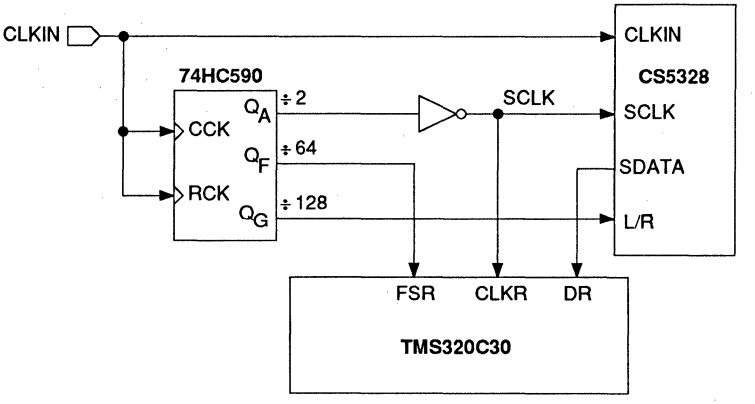


Figure 20. TMS320C30 Connection Diagram

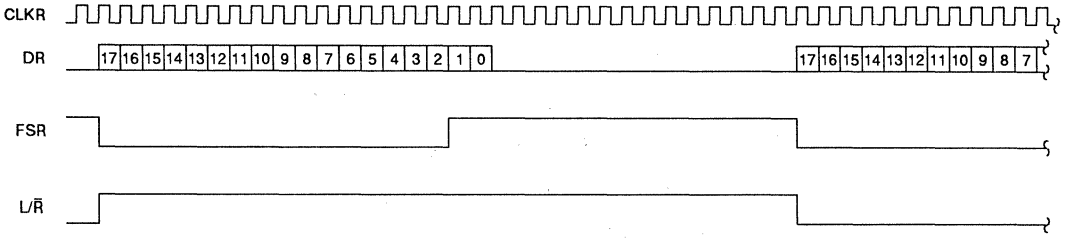


Figure 21. TMS320C30 Timing Diagram

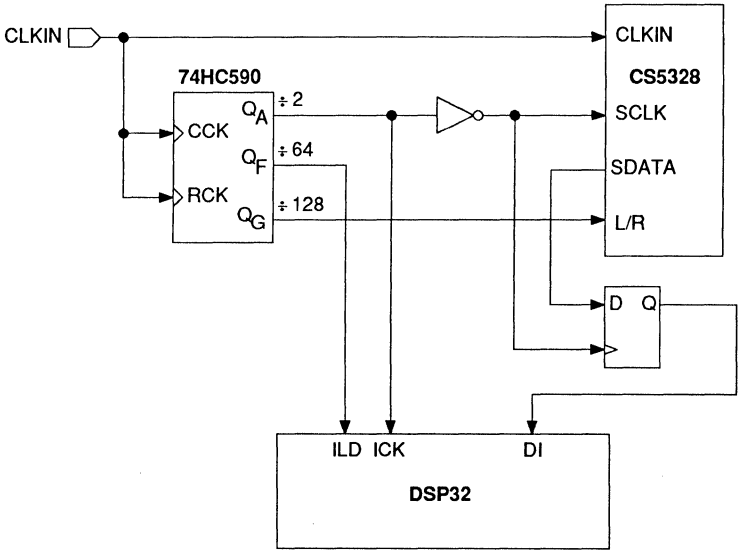


Figure 22. DSP32 Connection Diagram

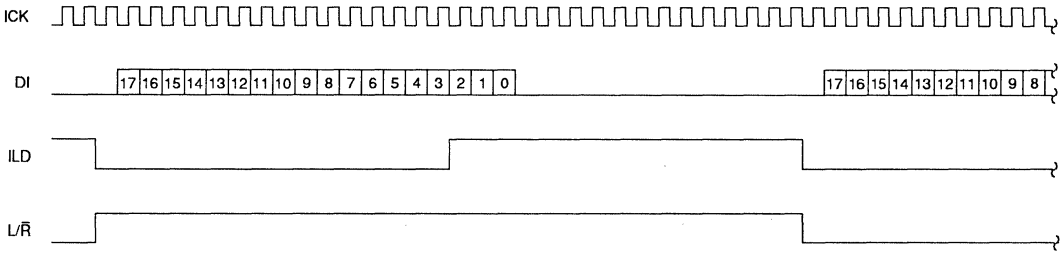


Figure 23. DSP32 Timing Diagram

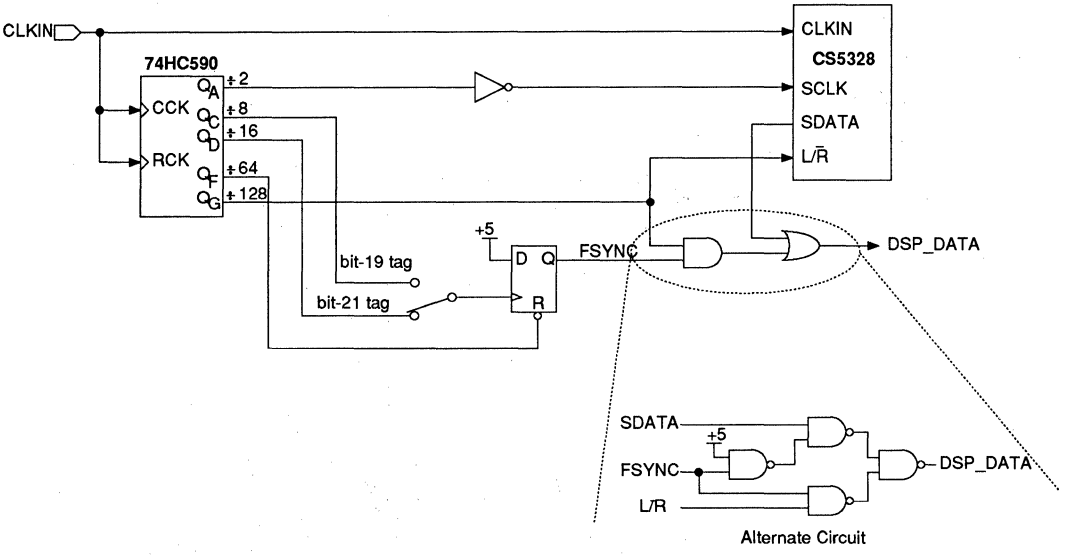
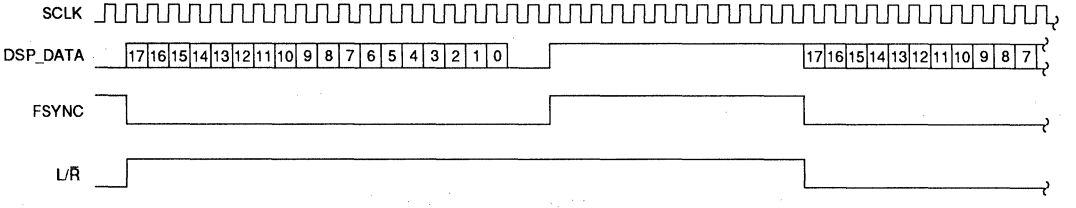
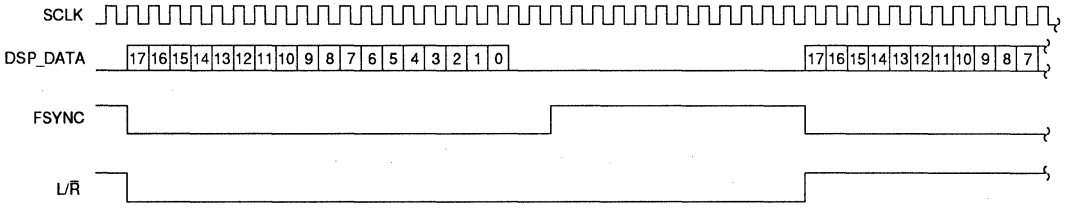


Figure 24. Channel Tag



a. Left Channel



b. Right Channel

Figure 25. Channel Tag Timing Diagram (bit-21 tag)

A Stereo 16-Bit Delta-Sigma A/D Converter for Digital Audio

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A two channel 16-bit A/D converter employing oversampling techniques has been developed. The device contains two fourth order delta-sigma modulators with 1-bit outputs, each followed by a digital finite impulse response filter/decimator. The analog inputs are sampled at 3.072 MHz and the digital words are output at 48 kHz.

0. INTRODUCTION

The emergence of digital audio has increased the demand for high performance A/D converters. Delta-sigma conversion has been gaining recognition as having advantages over more classical audio band conversion techniques. In particular, it obviates the need for sample and hold amplifiers, eases the design of anti-aliasing filters, and is free of differential non-linearity errors that distort low level signals.

This paper discusses the development of a two channel 16-bit audio band delta-sigma converter featuring a high degree of integration and suitable for use in stereo digital audio applications. Section 1 gives an overview of the concepts pertaining to delta-sigma conversion. The device architecture and a functional partitioning strategy are presented in Section 2 Sections 3 and 4 discuss design of the two major functional blocks, and measured results are presented in Section 5.

1. DELTA-SIGMA CONVERSION

1.1 Quantization Noise

Analog to digital conversion is a process that necessarily introduces errors into a signal due to quantization. The difference between the output of an otherwise perfect converter (or "quantizer") and that which might be expected of a converter with unlimited resolution can be modelled as an additive noise signal. The level of this "quantization noise" is reduced in converters of higher resolution with finer quantization levels, but nonetheless must remain non-zero. If the analog input is sufficiently large and/or if the input is sufficiently random, the spectrum of the quantization noise can be approximated as white [1] with its energy equally distributed between dc and $f_S/2$, where f_S is the sampling and conversion rate (it is assumed the signal is sampled before it is converted). The effective resolution of a converter can be increased by filtering the output and thereby reducing the level of the quantization noise. A commensurate reduction in the available signal bandwith must be accepted as a consequence of the filtering, but may prove acceptable if the conversion rate is high. The sampling and conversion of a signal at a rate much higher than the signal frequency is a technique termed "oversampling". The "oversampling ratio" is the ratio of the actual sampling rate to the Nyquist rate (i.e., twice the highest signal frequency of interest).

This process is illustrated in Figure 1, where an analog sinusoid of frequency f_O is converted to a digital, quantized sinusoid at a rate f_S by a linear

pulse-code modulation (PCM) converter. The input spectrum is shown in Figure 1A, and Figure 1B shows the effects of the quantization process with the addition of white noise (this and following spectra repeat at multiples of f_S, of course, due to the discrete time nature of the sampled signal). Processing by a digital filter with a baseband cutoff frequency of f_b as illustrated in Figure 1D yields the output spectrum in Figure 1E. The baseband cutoff frequency f_b is presumed to be equal to the highest signal frequency of interest. The remaining quantization noise voltage level will be lower than the original level by a factor of $\sqrt{f_S/2f_b}$ (the quantization noise *energy* is lowered directly by the oversampling ratio $f_S/2f_b$).

The utility of this technique when applied to audio signals with a baseband frequency of f_b = 20kHz is questionable. To obtain the equivalent of 16-bit performance from, say, a 12-bit converter, the 12-bit quantization noise would have to be lowered by 2^4=16. This would in turn require an oversampling ratio of $f_S/2f_b$ = 256, or f_S≅10MHz.

Delta-sigma conversion is a technique that employs oversampling to obtain high resolution (low quantization noise) digital signals from low resolution (high quantization noise) quantizers. As will be shown below, the delta-sigma converter contrasts with the previous example in that the quantization noise *at the output* of the low resolution quantizer is not white, but rather frequency "shaped", such that noise in the baseband ($f<f_b$) is suppressed at the expense of slightly higher out-of-band ($f>f_b$) noise. The power of digital filtering can then be applied to the resultant spectrum to pass the signal (and the residual baseband quantization noise) while rejecting the out-of-band quantization noise.

The converter consists of a modulator and a digital filter. As can be seen in Figure 2, embedded in the modulator is the low resolution N-bit quantizer, around which frequency dependent feedback is applied by means of a N-bit DAC and an analog filter. The analog filter has a frequency response of H(f). The analog input is

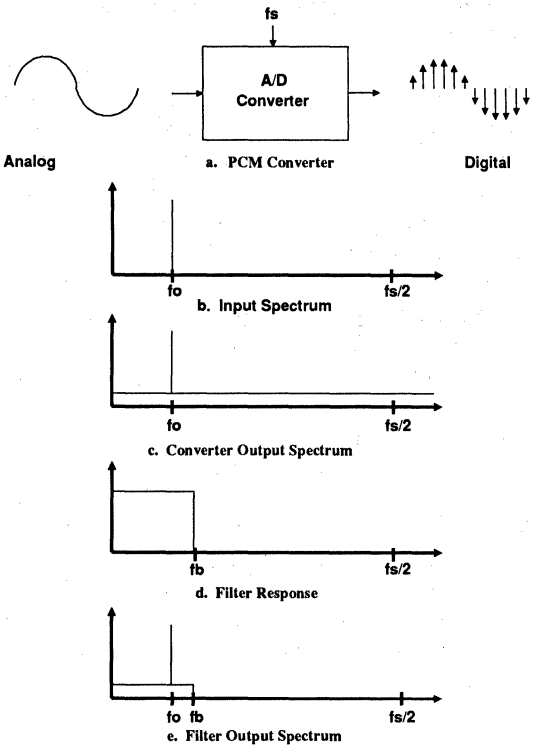

Figure 1. Increasing Resolution with Filtering

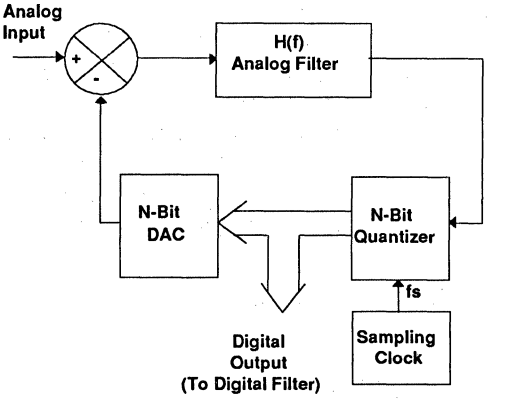

Figure 2. Delta-sigma modulator

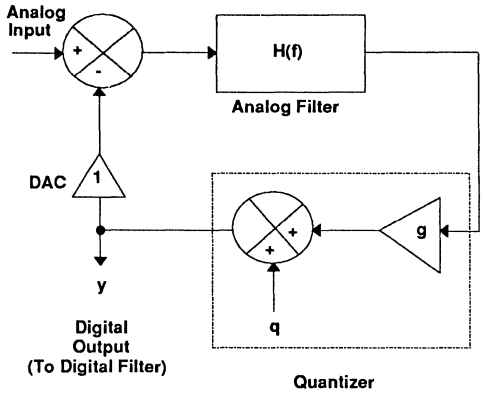

Figure 3. Linearized delta-sigma modulator

summed into the modulator loop at a point where, for frequencies with high loop gain, the output of the DAC will be substantially equal to the input. To the extent that the DAC faithfully reproduces the quantizer digital output, this signal, too, must be substantially representative of the analog input again, for frequencies with high loop gain.

1.2 Loop Analysis

The presence of the non-linear quantizer renders exact analysis of the loop difficult. A typical and useful approach is to linearize the quantizer by replacing it with a gain stage and a quantization noise source [2]. Again, the latter is only a contrivance to account for the difference between the quantized output and the amplified input. This is illustrated in Figure 3. The DAC has been replaced by a unity gain stage, as its function is irrelevant for analyzing the effects of quantization noise. Note, though, that non-idealities in the DAC can be the chief limitation to the modulator's performance [3].

The actual value of the gain g and the rms value of the quantization noise signal q need not be known to obtain an understanding of how the modulator shapes the quantization noise. It must be assumed, however, that successive values of the quantization error are uncorrelated — i.e., the quantization noise spectrum is white. The validity of this assumption is borne out empirically.

The modulator output signal y is a function of the analog input x and quantization noise q, as follows:

$$y = (x\text{-}y)\,\mathrm{H(f)}g + q$$

$$y\,[1 + \mathrm{H(f)}g] = x\mathrm{H(f)}g + q$$

$$y = \frac{\mathrm{H(f)}gx}{1 + \mathrm{H(f)}g} + \frac{q}{1 + \mathrm{H(f)}g}$$

If the loop gain $\mathrm{H(f)}g >> 1$, then

$$y \cong x + \frac{1}{\mathrm{H(f)}g}q$$

That is, the output will be the sum of the input and the quantization noise spectrally shaped by the inverse of the analog filter frequency response.

A glance at the approximate expression for y may lend hope to the prospect of reducing quantization noise by increasing the value of H at all frequencies. However, the effective value of g would change to compensate such a maneuver. Reducing q by introducing a higher resolution quantizer would indeed offer improved performance. But the most effective method of achieving lower baseband quantization noise (for a given oversampling rate) is the selection of filter function H(f) that possesses high in-band gain and high out-of-band attenuation, thereby shaping the quantization noise spectrum advantageously. Note that the poles of the filter are zeros of the noise transfer function.

1.3 Integrator

A simple integrator has the desired spectral qualities for a filter. A cascade of two integrators would appear more attractive, and indeed such a "second order" filter more effectively shifts quantization noise to out-of-band frequencies than the "first order" filter. Extension to higher order filters is problematic, though, due to stability considerations. A second-order design requires the placement of a single zero in the filter response to obtain a well-behaved modulator.

Higher- order filters can also have zeros included as an aid to stability, but even so they are conditionally stable due to the high phase shift at baseband frequencies. Conditionally stable loops can become unstable if a frequency independent gain parameter in the loop is reduced. The effective quantizer gain g is such a parameter and is subject to change under varying operating conditions. As such, stability of modulators with third and higher order filters is at risk. Nevertheless, the attractiveness of higher order filters has led to a number of solutions to the stability problem [4],[5]. The device discussed in this paper utilizes a fourth-order filter. Stability will be discussed below.

Another approach that leads to performance similar to higher-order modulators without the attendant stability question has been reported [6]. This architecture has cascaded lower order modulators, with successive modulators measuring the residual in-band quantization noise of previous modulators. The various modulator outputs are digitally processed to lower overall in-band noise. However, accurately matched components and high gain integrators are necessary to achieve the desired performance.

1.4 Filtering and Decimation

Once the quantization noise has been appropriately shaped, it remains the task of the digital filter to remove the out-of-band quantization noise. A straightforward approach of synthesizing a low pass filter with sufficient stopband attenuation and acceptable pass-band response would prove inefficient. Instead, a strategy of staged filtering and decimation can be adopted to ease the computational burden [7]. Decimation is the process of sampling a discrete time signal at a rate lower than its own. The advantage of decimation is that signal processing after decimation can proceed at the lower rate. As a sampling process, though, decimation is subject to the ill effects of aliasing.

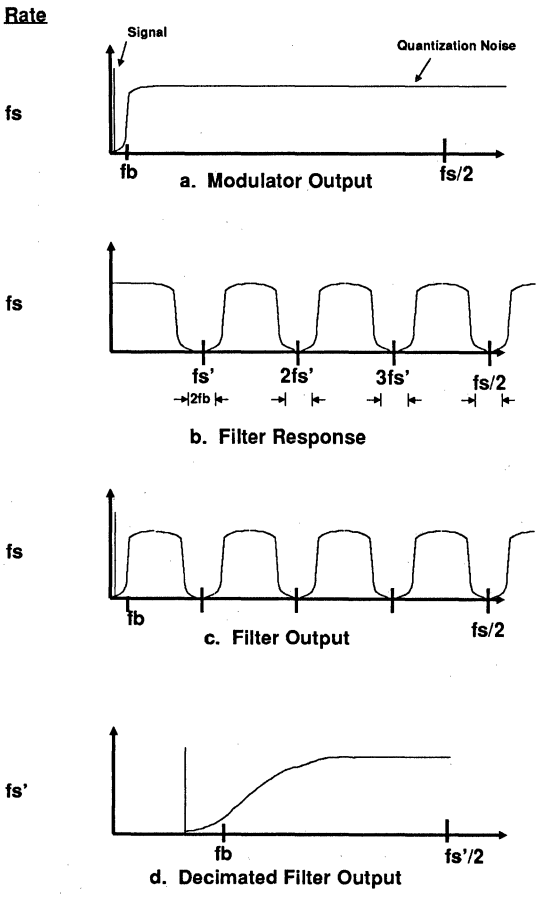

Figure 4. Filter Strategy

In this application, each stage of filtering need only reject signals that will be aliased into the baseband by the immediately subsequent decimation process, since later filter stages will reject signals aliased elsewhere. Figure 4 illustrates this approach. A signal with a spectrum characteristic of a modulator output signal is input to a filter at a rate f_S. The output of this filter is to be

decimated to a new rate f_S', where $f_S = Nf_S'$, before being processed further. Aliasing will occur throughout the spectrum, but only components within $\pm f_b$ of integer multiples of f_S' will get aliased into the baseband. A filter designed to have rejection only in these frequency "pockets" requires much less computation than one with rejection across the entire stop-band. As the sampling rate gets lower, of course, the pockets become proportionately wider and the filters become more complex. However, they can proceed with their computations at a more leisurely pace.

The final filter stage, operating at the slowest rate, can be a true low pass filter, eliminating the accumulated out-of-band quantization noise. In addition, it can "tweak" the frequency response of the pass-band if previous filter stages, the modulator, or even analog processing prior to the modulator have warped the response.

The need to reject the out-of-band quantization noise also represents a benefit. Namely, signals outside the baseband up to half the modulator sampling frequency do not get aliased by the modulator and are rejected by the digital filter. Indeed, spurious input signals approaching the sampling frequency do not get aliased into the baseband unless they are within $\pm f_b$ of f_S, and are likewise rejected. This characteristic can greatly relax analog anti-aliasing requirements and, for some applications, stands as one of the leading benefits of delta-sigma conversion.

2. ARCHITECTURE

2.1 Overall Architecture

The device described in this paper contains two delta-sigma converters suitable for stereo digital audio applications. It is packaged in a 28 pin dual-in-line package with a standard 0.600 inch wide footprint. The cavity of the package is occupied by two silicon dice. One die contains the two modulators, a voltage reference (the value of which determines full scale signal level), clocking circuitry, and a small amount of digital housekeeping circuitry. The second die contains the digital filter/decimators.

2.2 Reasons for Two Die

Partitioning of the system in such a fashion was motivated by the following considerations:

1) The complexity of the digital filter necessarily creates a large amount of electrical noise during normal operation. Placing this circuitry on a silicon substrate separate from the modulators eases the task of preventing this noise from interfering with the modulators' analog signal processing.

2) The great majority of the silicon area is occupied by the digital filter/decimators, and the manufacturing cost is dominated by this circuitry. Shrinking of the geometries comprising this circuitry as the product matures can lead to cost reductions without affecting performance. Shrinking of analog circuitry is risky and difficult; hence, the advantage of removing this circuitry from the more cost-sensitive digital die.

3) With separate die, different processes can be used to fabricate the analog and digital portions on the converters.

Regarding the last item, the digital die is manufactured using a standard 5V, 2 micron double-metal digital CMOS process. A 10V process was chosen for the analog die to allow more headroom for the analog signals. CMOS was chosen to support the switched capacitor design discussed in the next section. The selected process has 3 micron line widths, double polysilicon layers for capacitors, and a single metal layer.

2.3 Shared Functions

To a large extent, the two channels function independently. However, some circuit blocks are shared. On the analog die, all clocking is common between the two channels to facilitate simultaneous sampling of the left and right channel signals. Additionally, a single voltage reference

circuit is utilized by both channels. The voltage reference employs both lateral and vertical bipolar *npn* transistors (both of which are useful parasitics in this process) in a bandgap configuration. Its output is connected to a pin so that it can be capacitively bypassed to reduce crosstalk between the two channels. This capacitor and two simple RC anti-alias filters are all the external elements required of the device other than standard power supply decoupling elements.

The two digital filter/decimators also have common clocking. The various filter coefficients are stored in a single ROM which is accessed by both right and left channels.

3. MODULATOR

3.1 Major Characteristics

The major characteristics that need be determined in the design of a delta-sigma modulator are filter technology, oversampling ratio, quantizer resolution, and filter order.

3.2 Discrete Time Implementation

Although continuous time filters can be employed in the implementation of a delta-sigma modulator (sampling occurs at the quantizer only), three considerations dictated the choice of sampled data filters for use in the product. First is the ease with which sampled data filters can be integrated in comparison to continuous time filters. Second is that continuous time filters are sensitive to timing errors in the feedback of the modulator's DAC signal [3], whereas sampled data filters are not. Third, with proper design care sampled data circuits can provide greater isolation between channels in a stereo application since signal currents are transient. They can be made quite small at the sampling instances and are of no consequence at other times (both technologies are subject to capacitive crosstalk). Thus, sampled data switched capacitor technology was chosen for the design of the modulator.

3.3 Oversampling Ratio

The oversampling ratio is limited by the achievable settling time of analog components as well as the maximum computation rate of the digital filter. It is also preferable that the oversampling ratio be a factor of 2^N to ease applications. With a standard baseband of 24kHz, the oversampling ratio of 64 was chosen for a sampling rate of 3.072MHz. In a switched capacitor network each cycle is divided into two phases. With design margin, all modulator circuit blocks were designed to settle in 100ns to 0.1%.

3.4 1-bit Quantizer

As was mentioned in Section 1, higher resolution quantizers embedded in the modulator loop yield lower levels of in-band quantization noise. However, a 1-bit quantizer (i.e., a comparator) is simple to implement and minimizes the number of connections between the modulators and their digital filters. More importantly, a very attractive attribute of the use of a 1-bit quantizer is that errors in the 1-bit feedback DAC are not sources of distortion and/or excess noise, but only gain and offset errors [8]. Therefore, no precision components are necessary. Further, a one bit output simplifies the design of the first (and highest speed) digital filter stage.

3.5 Modulator Filter Order

The selection of a 1-bit quantizer operating at an oversampling rate of 64 requires at least a third order modulator filter to obtain 16-bit performance at the digital filter output. The addition of other noise sources (e.g., quantization effects in the digital filter) eliminated the candidacy of a third order filter. A fourth order modulator filter comprised of four cascaded integrators would provide sufficient rejection of baseband quantization noise. However, the modulator's baseband quantization noise can be rendered insignificant by optimization of a fourth order filter, as follows.

In Section 1 it was noted that the poles of the modulator filter are the zeros of the quantization noise transfer function. A filter with four cascaded integrators results in a noise transfer function with four zeros at dc. Lee and Sodini [9] found that spreading these zeros by application of local feedback around the integrators was effective in lowering the total baseband quantization noise output by the modulator. Optimal placement of all four zeros (two conjugate pairs) results in an 11dB improvement in baseband quantization noise rejection. Optimal placement of a single conjugate pair with two zeros left at dc results in a 10dB improvement.

Implementation of the two-conjugate-pair filter requires feedback to the input summing junction. This requirement has associated undesirable consequences (PSRR degradation, for example) and the two pair configuration offers little additional noise shaping improvement above the single pair. So, the single conjugate pair configuration was adopted.

3.6 Modulator Design

Figure 5 is a block diagram of the modulator. Coefficient b is fed back around the third and fourth integrators to form the conjugate pair of poles in the filter transfer function. The analog input is represented by x, and the single bit digital output is y (which is inverted and summed with x in analog form). The feedforward coefficients a_1 through a_4 are necessary (although not sufficient) for stable operation. The value of one coefficient is arbitrary. The value of the other three coefficients determine the location of filter zeros, but the effect of these on modulator operation is not easily predictable. Higher ratios of a_1 to a_4 lead to more stable, noisier operation.

3.7 Stability Considerations

As was mentioned in Section 1, low values of the "effective gain" of the quantizer (in this case comparator) g can lead to instability. Since the output levels of the comparator are fixed, and since in an unstable mode the integrator output levels can be expected to grow, any linearization

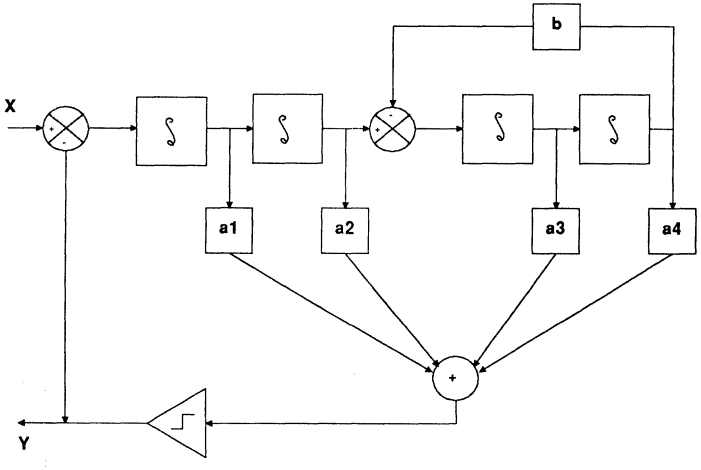

Figure 5. Modulator Block Diagram

criterion for evaluating g should lead to an ever decreasing value. Similarly, it would not be unreasonable to expect that large values of the input would lead to small effective values of g, initiating instability.

Simulation and laboratory experience has shown that the modulators do indeed exhibit this behavior. Fortunately, stable regions of operation also exist. The strategy adopted in the design of these modulators is to allow normal operation only well within the stable state space. Circuitry is provided to detect excessively high integrator levels as an indication of unstable operation. If such levels are detected, the integrators are reset to a stable condition. In practice, the reset circuitry is never utilized except at power-up (whereupon the modulator filter may or may not be in a stable state) or during periods when the input is excessively high. "Excessively high" means much higher than full scale, in which case the converter's digital output would be clipped and occasional modulator resets would be of no consequence. As the input returns to a level near full scale, the latest reset event leaves the modulator in a stable state.

3.8 Measured Spectra

Figure 6 shows a typical spectrum of a simulated modulator including a sinusoid input signal (very close to dc on the linear frequency scale) plus the quantization noise from dc to $f_S/2$. An expansion of the low frequency portion of this figure is shown in Figure 7. Here, the effect of the conjugate pair of quantization noise zeros is evident, as well as that of the pair at dc.

4. FILTER/DECIMATOR

4.1 Overall Architecture

Linear-phase finite-impulse-response (FIR) filters are used for decimation. The 1-bit, 3.072MHz outputs of the modulators are decimated in steps of 8, 4, and 2 to yield 16-bit, 48kHz results. A functional block diagram of the digital die appears in Figure 8. Timing, control, and coefficient ROMs (FIR2 and FIR3) are shared by the two channels. Left and right channel data paths operate independently. FIR2 and FIR3 use a per-channel multiplier/accumulator.

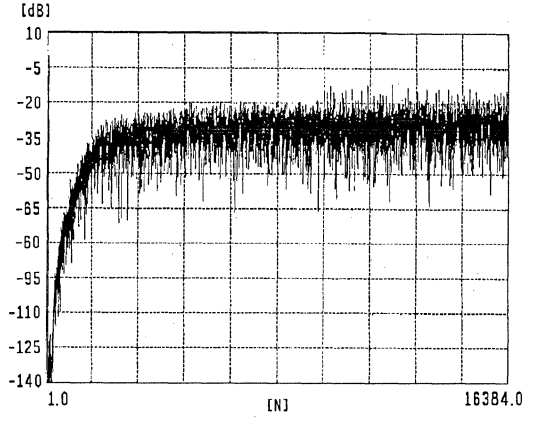

Figure 6. Simulated modulator output spectrum

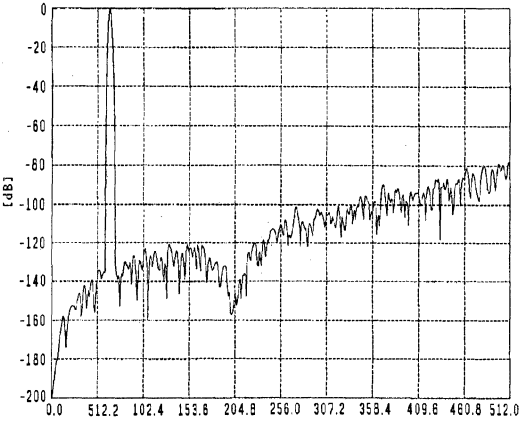

Figure 7. Expanded simulated modulator output spectrum

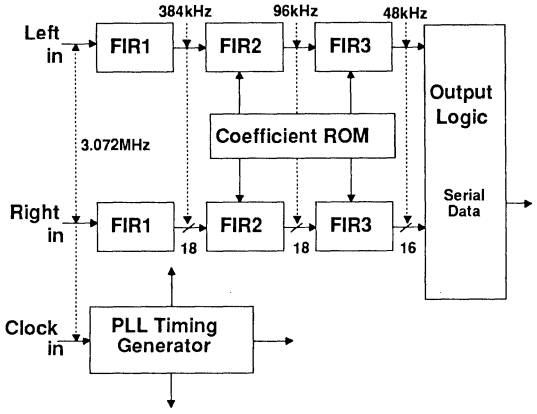

Figure 8. Filter/decimator block diagram

4.2 Decimation

The decimation strategy includes two stages, FIR1 and FIR2, whose primary responsibility is attenuation of quantization noise prior to decimation and aliasing. As Figure 6 shows, modulator out-of-band quantization noise spectral density is very high. FIR1 and FIR2 use 17 and 18-bit coefficients to attenuate this noise — and out-of-band input signals — into the converter noise floor. Filter orders are 27 and 30, respectively. Data is processed with 18-bit fixed point arithmetic.

4.3 Passband Shaping

FIR3 performs passband shaping and out-of-band signal attenuation. Passband frequency response errors introduced by the modulator, FIR1, and FIR2 are corrected by FIR3. Overall filter passband ripple is thus reduced to ±0.001dB from dc to 22kHz. The passband compensation function prevents the use of a half-band filter for FIR3. The filter has 124 non-zero, 18-bit coefficients. Again, data is processed with 18-bit fixed point arithmetic. Data is truncated to 16 bits at the output, and this operation is the major noise contributor in the system.

4.4 Antialiasing Filtering

As indicated in Section 1, FIR1, FIR2, and FIR3 also combine to provide antialiasing filtering. All analog input frequencies from 26kHz to 3046kHz are attenuated by at least 86dB. The magnitude response of the complete modulator/decimator from dc to 48kHz is shown in Figures 9 and 10. Phase response is precisely linear.

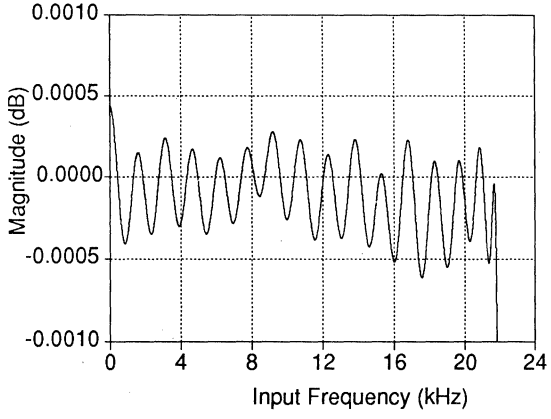

Figure 9. Filter passband ripple

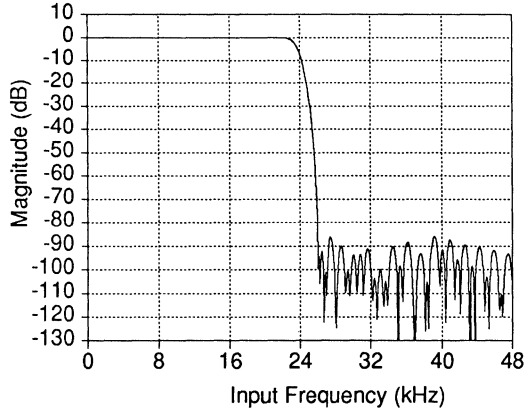

Figure 10. Filter frequency response

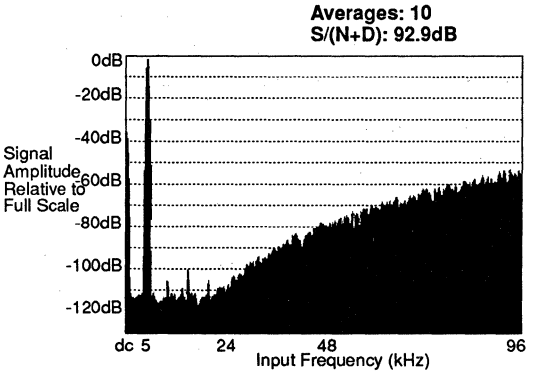

Figure 11. Partial 16K point FFT of modulator output

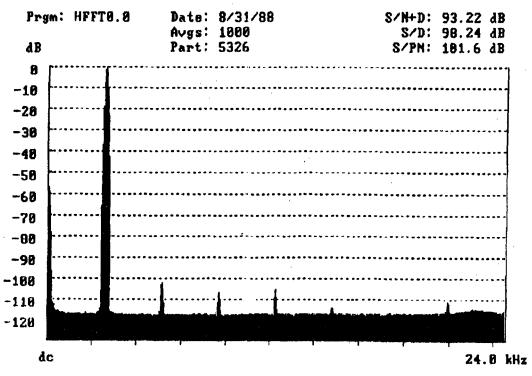

Figure 12. 1000 averaged FFTs of A/D converter output

5. RESULTS

5.1 Modulator Output

Testing of the key specification parameters was performed with the aid of Fast Fourier Transform (FFT) routines. Figure 11, for instance, shows the low frequency portion of an FFT performed on a modulator's single bit output. The quantization noise shaping is evident in this plot. Absent, however, is the null due to the conjugate pair noise shaping zeros that is visible in Figure 6. The quantization noise of the modulator is masked by the device's more classical noise mechanisms. Quantization noise can only be seen rising out of the thermal noise floor at frequencies above the audio band.

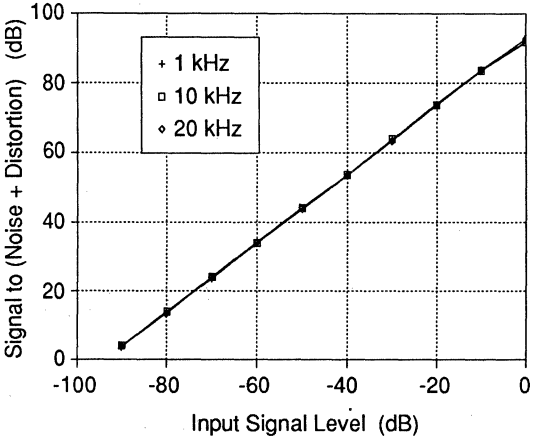

Figure 13. Signal-to-noise ratio versus signal level

5.2 Digital Filter Output

Figure 12 shows a plot of the result of an average of one thousand FFT's performed on the 16-bit words output by the digital filter. Averaging of numerous FFT's serves only to cosmetically smooth the noise floor and does not change the ratio of the signal to noise level. The width of the fundamental is due to the application of a low side-lobe window to the data stream [10].

In addition to the noise floor and the fundamental, dc and harmonic distortion components are visible. Close inspection reveals a 1/f noise corner in the area of 300Hz and a bump in the noise floor in the area of 23kHz. The latter is caused by the rising modulator quantization noise in concert with the falling digital filter characteristic.

Figure 13 is a plot of measured signal-to-noise plus distortion ratio versus signal level for 1kHz and 10kHz input frequencies. High-level performance appears slightly better for the 10kHz signal because all but the second-harmonic distortion components fall outside the baseband.

5.3 Specifications

Table 1 lists the key specifications and their measured values.

Oversampling ratio	64X
Signal-to-noise plus distortion	92 dB
Dynamic range	94 dB
Filter passband ripple	<0.001 dB
Filter stop-band rejection	>86 dB
Calibration error	5 LSB
Chanel-to-channel crosstalk	-103 dB at 20 kHz
Channel-to-channel gain mismatch	0.04 dB
Gain temperature coefficient	80 ppm/°C
PSRR	50 dB
Power dissipation	450 mW

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The Effects of Sampling Clock Jitter on Nyquist Sampling Analog-to-Digital Converters, and on Oversampling Delta Sigma ADC's.

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CONTENTS

DEFINITION OF PRELIMINARY PART TYPES

Before a part is in full production, Crystal will supply preliminary parts. There are two varieties:

I.Engineering Sample (ES)

Engineering sample "ES" is a product which has not been completely characterized or where qualification has not reached the first lot 500 hours read point. ES product will be assembled per manufacturing specs at qualified assembly sites. All units will be tested to a published data sheet and applicable errata sheet (if needed). Any ES units which are tested only at room temperature will receive a supplemental brand "25°". As soon as automated temperature testing is available for this device, all subsequent ES units will be 100% temperature tested.

The following premium - temperature product grades will always be 100% tested at temperature:

TELECOMMUNICATIONS - "M" grade
DATA ACQUISITION - "A", "B", "C", "S", "T", and "U" grades

II. Engineering Prototype (EP)

Engineering Prototype is an engineering prototype of a device which works sufficiently for beta site purposes.

DEFINITION OF DATA SHEET TYPES

Each product developed by Crystal will be supported by technical literature where the data sheets progress through the following levels of refinement:

I. Product Preview

This is a 1-to-4 page document which describes the main features and specifications for a product that is under development. Some specifications such as exact pin-outs may not be finalized at time of publication. The purpose of this document is to provide customers with advance product planning information.

II. Preliminary Product Information

This is the first document completely describing a new product. It contains an overview, specifications, timing diagrams, theory of operation, pin-out diagram, applications information, ordering guide and mechanical information. The numbers in this data sheet are based on prototype silicon performance and on worst-case simulation models. The specifications represent the designer's best estimate for the "real" numbers. Min and max values are included where possible. The purpose of this document is to provide system designers with technical information sufficiently detailed to guarantee that they can safely begin active development.

III. Final Data Sheet

This is an updated version of the preliminary data sheet reflecting actual production performance of the final product. Updates include tighter specifications, more min and max values, and any application information that has arisen during the early life of the part. The purpose of this document is to communicate the confirmed performance of products which have passed qualification, been fully characterized, and are in production.

RADIATION RESISTANCE PERFORMANCE

Crystal products are manufactured using 2 and 3 micron CMOS processes. While not able to withstand large doses of radiation, our products are suitable for operation in low to medium dose applications. Indeed, the self calibrating architecture of many of the A/D Converters is able to compensate for the effects of radiation.

Crystal will assist customers to test parts for radiation resistance by supplying free, data-logged parts. In exchange, we would like the parts returned to us, so that we can measure their post-radiation performance. In addition, we would like a copy of any report that is generated, along with permission to publish the report for other customer's information.

Several customer's have already undertaken radiation testing of our A/D Converters. Please contact the factory for the latest information and copies of the radiation performance reports.

RELIABILITY METHODS

I. CONCEPT OF RELIABILITY

In general terms, the reliability of a semiconductor device is defined as the measure of the functional stability of the device with respect to time. Expressed in a more quantitative sense, it is the probability that the device will operate with a specified performance over a specified period of time under a given set of conditions.

Reliability characteristics are usually stated in reverse terms as the loss of ability to function, or failure rate. The reliability performance of a device can best be summarized by the reliability life or "bathtub" curve (Figure 1). The reliability performance is characterized by three phases: infant mortality, useful life, and wearout. Infant mortality failures can be reduced by proper manufacturing controls and screening techniques. The useful life period is typically a long period of time where only occasional random failures occur. During this time the failure rate is usually very low. The final period is aptly named wearout. Using proper design guidelines and device applications, this period is shifted well beyond the lifetime required by the user.

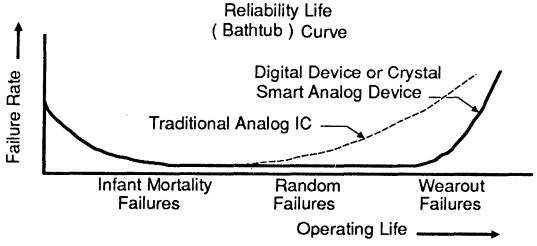

Figure 1.

An item of great importance in evaluating reported reliability characteristics is the definition of a failure. Crystal's definition of a failure is any device that fails to meet ANY data sheet parameter. Crystal's digital self-calibration techniques provide stable performance over temperature and life. Traditional Analog IC's and hybrids exhibit wearout mechanisms very early in the life of the product. One competitor's analog-to- digital converter's linearity error stability is specified at +/- .00075 % per 1000 hours at 25 °C. Stability degradation at 70 °C is unspecified and is likely to be accelerated greatly as temperature increases. The dashed line of Figure 1 is typical of the wearout seen in a competitor's Analog IC or hybrid. As you can see, wearout begins much earlier than a digital device or a mixed analog and digital chip utilizing Crystal's SMART analog design architecture and CMOS wafer technology.

II. CRYSTAL SEMICONDUCTOR RELIABILITY STRESSING

These stresses are done on every new product, assembly house or fabrication subcontractor. The Crystal acceptance criteria and goals are as described in Table 1 of the Quality and Reliability information in section 1 of this data book.

Accelerated Operating Life Stress

Accelerated operating life stressing is performed to accelerate thermally-activated failure mechanisms through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications. Some devices may be stressed at an even higher voltage level to further stress the oxides of the device. All devices used in life stress are sampled directly from the production flow with no special processing or pre-screening. Stressing is performed per MIL STD 883, method 1015, condition D (dynamic signals). These dynamic conditions simulate as much as possible actual operating conditions in an application.

Both infant mortality operating life stress (168 hrs at 125 °C) and long term operating life (typically 1000 hrs at 125 °C) are reported . Infant mortality life simulates approximately 6-8 months in the field at 70 °C and is reported as %/168 hrs. Long term life simulates the total failure seen in the field and is expressed in FITS (failures in time). 1 FIT = 1 failure per billion device-hours. Derating of long term operating life is done using Arrhenius thermal equations along with Weibull statistics. A 60 % upper confidence limit (UCL) and .7 electron volts (eV) activation energy are used in this calculation.

85 °C/85% R.H.

85 °C/ 85% R.H. is an environmental stress performed at a temperature of 85 °C and at a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated devices. A nominal-voltage static bias is applied, with minimum power consumption, to the device, to accelerate the electrolytic corrosion of the metallization. Failures are expressed in % /time with 168, 500, and 1000 hour cumulative results reported.

Autoclave

Autoclave is also an environmental stress which measures the moisture resistance of plastic encapsulated devices. Conditions for this test are 121 °C, 100% relative humidity, and 1 atmosphere of pressure (15 psig), with no bias applied to the circuit. Corrosion of the die is the expected failure mechanism. Stressing is usually performed for 144 hours. Failures are expressed in %/time with 48, 96, and 144 hour results reported.

Temperature Cycling

Temperature cycling typically accelerates the effects of the thermal expansion mismatch among the different components within a specific package and circuit. The stress is performed per MIL STD 883, method 1010, Condition C (-65 °C to +150 °C). Stressing is done in an air environment. A cycle consists of ten minutes at -65 °C, five minutes transfer time, and ten minutes at +150 °C. Stressing is typically performed for 1000 cycles. Failures are expressed in %/cycles, with 100, 500, and 1000 cycle results reported.

Thermal Shock

The objective of thermal shock is basically the same as that of temperature cycling - to exercise the difference in thermal expansion coefficients within the integrated circuit package and die. Thermal shock provides additional stress as the device is exposed to a rapid change in temperature, due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid environment. This test is performed per MIL STD 883, method 1011, Condition B (-55 °C to +125 °C). In one cycle of thermal shock, devices are placed in a flourocarbon bath cooled to -55 °C for five minutes, then transferred to an adjacent bath filled with flourocarbon at 125 °C for five minutes. Stressing is performed for 500 cycles. Failures are expressed in %/cycles, with results reported at 100, 200, and 500 cycles.

High Temperature Storage Life

Storage life is an environmental stress where temperature is the only stress. Stressing is performed per MIL STD 883, method 1008, Condition C. (150 °C). Stressing is performed to 1000 hours. Failures are expressed in %/hours, with results reported at 168, 500, and 1000 hours.

Electrostatic Discharge

Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device. This test is performed per MIL STD 883 method 3015, which simulates the resistance (1500Ω) and capacitance (100 pF) of the human body. Also the machine model test is performed with a 0Ω resistance and a capacitance of

200 pF to simulate, as its name implies, a typical insertion tool, handler, etc. that comes in contact with the leads of a semiconductor device.

Latchup

Latchup testing is performed to ascertain whether a device can sustain SCR latchup due to a DC current input. The pin being tested has a DC current forced to it with the device power supplies at nominal voltage and inputs at ground state. Susceptibility of each input is tested with both a positive and negative DC current forced into it. This test is performed per the standard test procedure recognized by JEDEC.

C dv/dt Latchup Testing

This test is performed to evaluate the susceptibility of a CMOS device's power pin to instantaneous ESD discharge into a power supply pin or a rapid ramp of a power pin during power up. Positive and negative pulses are supplied to the power supply pins with a change in voltage of greater than 500 V/μs and a 0 to 5 V risetime of less than 15 ns. Ground, V_{SS}, and the pin under test are connected to ground. The supply current is monitored for excessive current.

III. FAILURE RATE CALCULATIONS

Failures during typical reliability stressing generally are in the infant mortality and random failure sections of the "bathtub" curve. Thermally accelerated failure rates can be derated to actual operating conditions by commonly accepted mathematical models.

Operating life stress is usually reported in the derated form. That is, operating life is performed at 125 °C and results are reported for an equivalent time at a typical operating stress temperature for an application, generally 25 °C, 55 °C, or 70 °C. Failure rates for other temperatures are calculated using a computed acceleration factor.

There are many probability models used in reliability analysis for calculating failure rates. The simplest form of calculating a failure rate (F.R.) would be to divide the number of failures observed after test (N) by the number of device-hours of stress.

$$\text{F.R.} = \frac{N}{D \cdot H} \qquad (1)$$

where D is the number of devices stressed and H is the number of stress hours. If this number is multiplied by 10^9 we obtain the failure rate expressed as Failure In Time (FIT). FITS are expressed as failures per billion device operating hours.

$$\text{FITS} = (\text{F.R.})(10^9) \qquad (2)$$

However, using equation (1) allows only for a failure rate calculation at the stress temperature. In order to apply the equation to the desired use temperature we use the well-known Arrhenius relationship to determine the thermal acceleration factor, F_a. One hour of device operation at temperature T_1 is equivalent to F_a hours of operation at temperature T_2. The activation energy, EA, is an important parameter in the Arrhenius equation and is discussed below. The Arrhenius equation is:

$$F_a(T_1 \rightarrow T_2) = e^{-\frac{EA}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \qquad (3)$$

where k = Boltzman's Constant (8.63×10^{-5} eV/°K) and T_1 is the accelerated stress junction temperature and T_2 is the desired use operating junction temperature in degrees Kelvin.

Junction temperatures, T_1 and T_2, should be used in determining acceleration factors. This temper-

ture can be obtained from the equation below.

$$T_j = T_a + \theta_{ja}P_d \quad (4)$$

where T_a is the operating ambient temperature and θ_{ja} is the package thermal dissipation (°C/ W) and P_d is the device power dissipation.

Crystal utilizes a low power CMOS process which typically raises the junction temperature about 7 to 15 °C, whereas analog bipolar IC's and hybrids can have power dissipations in the 1 W range. These differences in device junction operating temperatures can greatly affect the acceleration factors. For example, let's calculate the acceleration factors of a device with a power dissipation of 1 watt packaged in a 40 pin ceramic package. This is equivalent to a junction temperature change from 160 °C to 60 °C and from Table 2 the acceleration factor is 277. A typical Crystal device junction temperature is 10 °C higher than the ambient which results in a junction temperature change from 135 °C to 35 °C. This results in an acceleration factor of 636, as shown in Table 2. By comparing the results in Table 2 one can see how derating to a lower use temperature or failing to consider junction temperature when calculating acceleration factors can result in greatly differing failure rates.

TEMPERATURE CHANGE	ACCELERATION FACTOR
125 --> 70 °C	26.3
125 --> 55 °C	77.5
125 --> 25 °C	933.0
135 --> 35 °C	636
160 --> 60 °C	277

TABLE 2
ACCELERATION FACTORS FOR DIFFERENT TEMPERATURES (E. A. = .7 eV)

E . A.	ACCELERATION FACTOR
1.0	106.0
.9	66.7
.8	41.7
.7	26.3
.6	16.4
.5	10.3
.4	6.5
.3	4.1

TABLE 3
ACCELERATED FACTORS FOR DIFFERENT ACTIVATION ENERGIES (125 ° C --> 70° C)

Table 3 compares acceleration factors for different activation energies. Using a 1.0 eV activation energy versus a .7 eV activation energy results in a factor of four increase in the acceleration factor. Crystal uses an activation energy of .7 eV, a conservative value, compared to the .8 eV to 1.0 eV used by other analog IC vendors.

We now take the failure rate equation (1) at accelerated temperatures expressed in FITS and factor in the acceleration factors from the Arrhenius relationships considering junction temperatures and arrive at the equation below.

$$FITS = \frac{10^9 N}{DHF_a} \quad (5)$$

Using composite Crystal data through the 1st quarter of 1988, a failure rate at 25°C can be calculated by substituting in equation (5) above:

N = 23
D•H = 5,371,036
Fa = 702 (Assuming .7 eV and stress temperature of 125°C, using junction temperature derating)

D•H is the summation of the devices stressed at each readpoint multipled by that number of stress hours.

Substituting we get:

$$FITS\ 25°C = \frac{(10^9)(23)}{(5{,}371{,}036)(702)} = 6.1$$

The Weibull distribution is often used for product life predictions because it can describe increasing and decreasing failure rates. Also the Weibull dis-

tribution has both a shape parameter, β, and a scaling parameter, α. This is very useful in accurately describing the shape and scaling of the "bathtub" curve. These more accurate descriptions of the failure rate of the Weibull distribution make this method superior to the uniform failure distribution described in Equation (1). The Weibull probability distribution function (PDF) f(t) is the probability of failure between time t and t + dt.

$$f(t) = \frac{\beta}{\alpha} t^{(\beta-1)} e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (6)$$

The Weibull PDF can also be expressed as a function of the Reliability function, R(t), and the instantaneous failure rate function, h(t), therefore:

$$f(t) = h(t)R(t) \qquad (7)$$

The Reliability function is found by integrating the Weibull PDF from t to ∞. This function is the probability that a device will survive to time t.

$$R(t) = \int_{t}^{\infty} f(t')dt' = e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (8)$$

The instantaneous failure rate function is the probability that a device will fail between time t and t+dt:

$$h(t) = -\frac{1}{R}\frac{dR}{dt} = \frac{\beta}{\alpha} t^{(\beta-1)} \qquad (9)$$

The Reliability function is used to calculate the shape parameter, β, and the time scale parameter, α. The shape parameter is the key function in shaping the infant mortality portion of the "bathtub" curve. A β of 1 indicates a uniform failure rate, $\beta > 1$ indicates wearout and $\beta < 1$ indicates a declining failure rate. To use Weibull statistics, failures that occur during operating life stresses are used to produce values of R(t). Failure times and R(t) values can be combined to estimate α and β. We first take the natural logarithm of both sides of equation (8).

$$\ln\left(\frac{1}{R(t)}\right) = \frac{t^{\beta}}{\alpha}$$

We again take the natural logarithm and obtain:

$$\ln\left[\ln\frac{1}{R(t)}\right] = \beta \ln(t) - \ln(\alpha) \qquad (10)$$

This last equation is now in the form of a linear function. Using linear regression techniques or Weibull plotting paper we obtain the Weibull shape and scale parameter. Most semiconductor manufacturers perform a burn-in screening on devices to insure that the end customer receives a population of devices that have minimal infant mortality and are from the useful life period of the reliability "bathtub" curve. It is very important to include this data for the entire lifetime of the device to obtain an accurate curve fit for obtaining α and β.

Once the parameters α and β for the Weibull distribution are known we utilize R(t) to calculate FITS. Crystal uses a 20 year lifetime in its FIT calculations and typically uses a 48 hour burn-in at 125 °C hence:

t_{20} = 20 yrs = 175,200 hours
t_1 = 48 hours

The number of devices that will fail in the twenty year lifetime following burn-in is given by:

$$N = D\,[R(t_1) - R(t_1 + t_{20})] \qquad (11)$$

where D is the total number of devices stressed. The number of device-hours accumulated in 20 years can be estimated by counting the devices surviving after 20 years.

$$DH \geq D \cdot R(t_1+t_{20}) \cdot t_{20} \qquad (12)$$

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Using equation (2) for expressed failures in FITS we obtain the equation below for a Weibull distribution

$$\text{FITS} \leq 10^9 \frac{D\,[\,R(t_1) - R(t_1 + t_{20})]}{D \cdot R(t_1 + t_{20}) \cdot (t_{20})}$$

$$= \frac{10^9\,[\,R(t_1) - R\,(t_1+t_{20})]}{R(t_1+\,t_{20}) \cdot (t_{20})} \qquad (13)$$

The above equation applies only at the stress temperature. In order to apply the equation to the desired use temperature we factor in the acceleration factors, F_a, from the Arrhenius relationship as it relates to time in the reliability function. Therefore in equation (12) above we replace $R(t_1 + t_{20})$ by $R(t_1 + t_{20}/Fa)$. Note that the device lifetime t_{20} is still 20 years but the reliability function must have the acceleration factor considered for derating to use temperature. Using composite Crystal data through the first quarter of 1988, and using from equation (10), $\beta = .19$ and $\alpha = 521$ and $Fa = 702$ yields a failure rate at 25 °C of 9.7 FITS.

This failure rate is a more accurate measure of Crystal reliability than that provided by the constant failure rate model of equation (5).

Reliability evaluations involve only samples of an entire population of devices. Therefore a confidence level, (CL), should be placed on the average failure rate. At any time a sample is stressed from a population there exists a finite chance of failures. If many separate samples were stressed from the same population and failure rates plotted, a normal distribution of failure rates would occur. Therefore, valid statistical methods for a normal distribution should be used to determine the desired CL. Confidence levels for reliability analysis are expressed in upper confidence levels (UCL), typically at 60% or 90% depending on the criticality of the device's application. The total sample size stressed is critical in defining the UCL. Therefore rather large sample sizes must be stressed to more accurately demonstrate the true failure rate. A larger spread will exist between the 50% and 90% UCL distribution for smaller sample sizes due to the greater probability that the sample stressed was not representative of the entire population.

Environmental stresses, such as autoclave, temperature cycling, thermal shock, storage life and 85 °C/85%R.H., usually have their actual results reported, due to the lack of widely recognized derating models. These are usually expressed as %failure / stress time. An example of this would be a temperature cycling failure rate expressed as %/ 1000 cycles. These failure rates should have a confidence level associated with the data given. For environmental stresses, Crystal publishes data with a 90% confidence level. To calculate this failure rate with confidence levels, the following binomial probability statistics calculations are made:

$$P_C = P_a + Z\frac{[P_a\,(100 - P_a)]^{1/2}}{n} \qquad (14)$$

where P_C is the failure rate with confidence level, P_a is the observed failure rate in percentage defective, n is the number of samples stressed, and Z is the value of the standard normal probability distribution associated with the desired confidence level. (Z = 1.28 for 90% UCL.) This calculation agrees with the widely accepted lot tolerance percent defective, LTPD, plans that are based on 90 % upper confidence.

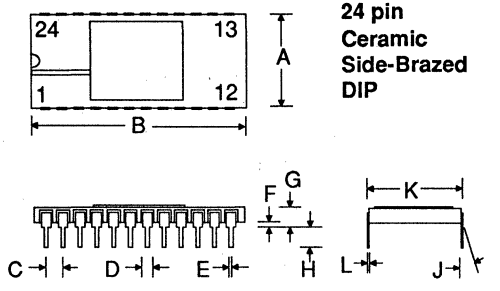
Of course it is not satisfactory to have accurate methods on reporting failure rates without having programs and methods in place to continuously improve the reliability of the product. Crystal uses methodologies in every level of the company to provide the highest possible quality and reliability standards of its products.

Using the reliability calculation methods of Maxim, an analog IC quality leader, Crystal achieves a failure in time (FIT) rate of 6.1 parts per billion operating hours. This compares favorably with Maxim's own performance of 6.8 FITs. Crystal's reliability is also established for devices requiring far greater analog accuracy than its competitors' products.

In summary Crystal Semiconductor uses conservative models that are accepted throughout the semiconductor industry to determine the reliability of its devices and has active programs in place to continuously improve the quality and reliability of its devices.

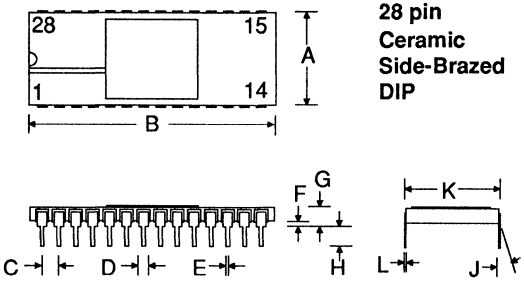
For further information on a summary of Crystal's methods of insuring high quality and reliability standards see the Quality and Reliability information in section 1 of this data book, or contact Crystal's Reliability and Quality Assurance Department at the factory.

MECHANICAL DATA



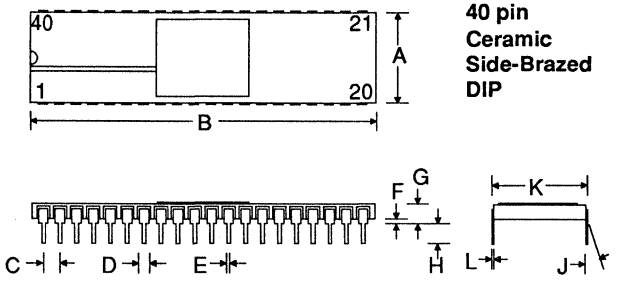
24 pin Ceramic Side-Brazed DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	27.64	33.53	1.088	1.320
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.67	4.32	0.105	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



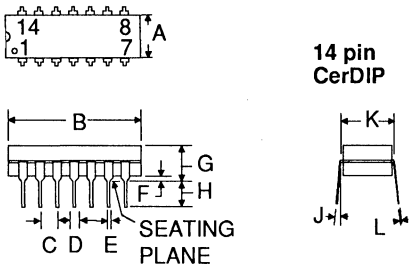
28 pin Ceramic Side-Brazed DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



40 pin Ceramic Side-Brazed DIP

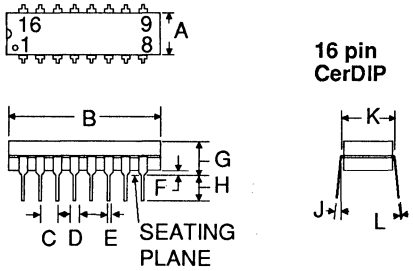
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.63	15.49	0.576	0.610
B	50.29	51.31	1.980	2.020
C	2.54 BSC		0.100 BSC	
D	0.76	1.52	0.030	0.060
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.65	0.590	0.616
L	0.20	0.30	0.008	0.012



14 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	19.05	19.94	0.750	0.785
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	-	15°	-	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.



16 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	19.05	19.94	0.750	0.785
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	-	15°	-	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
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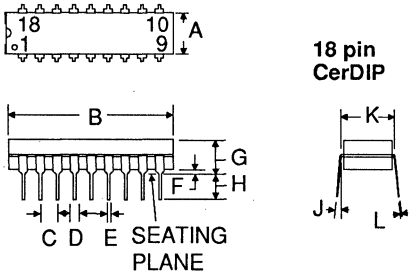

18 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	7.49	0.240	0.295
B	22.35	23.11	0.880	0.910
C	2.54 BSC		0.100 BSC	
D	1.40	1.78	0.055	0.070
E	0.38	0.53	0.015	0.021
F	0.51	1.02	0.020	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.32	0.115	0.170
J	0°	15°	0°	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION K TO CENTER OF LEADS WHEN FORMED PARALLEL.

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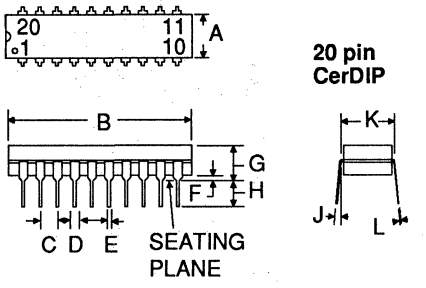

20 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.60	7.49	0.260	0.295
B	23.88	25.15	0.940	0.990
C	2.54 BSC		0.100 BSC	
D	1.40	1.65	0.055	0.065
E	0.38	0.56	0.015	0.022
F	0.25	1.02	0.010	0.040
G	3.81	5.08	0.150	0.200
H	2.92	4.06	0.115	0.160
J	0°	15°	0°	15°
K	7.62 BSC		0.300 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
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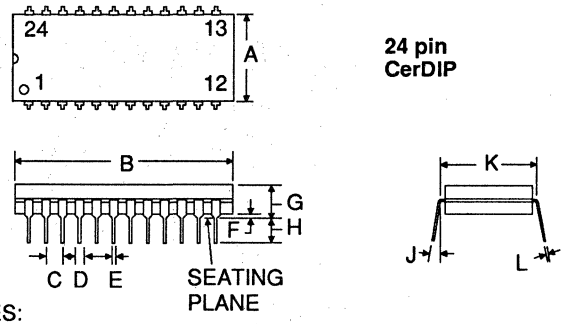

24 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.49	0.500	0.610
B	31.24	32.77	1.230	1.290
C	2.54 BSC		0.100 BSC	
D	1.27	1.52	0.050	0.060
E	0.41	0.51	0.016	0.020
F	0.51	1.27	0.020	0.050
G	4.06	5.59	0.160	0.220
H	2.92	4.06	0.115	0.160
J	0°	15°	0°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
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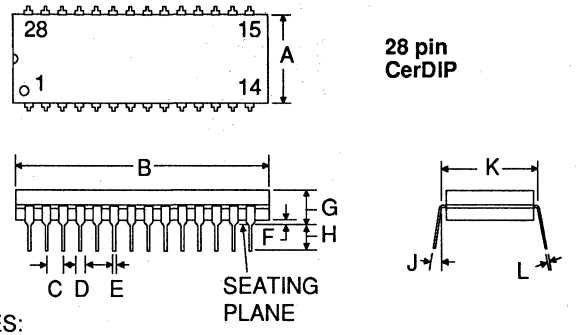

28 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	36.45	37.85	1.435	1.490
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
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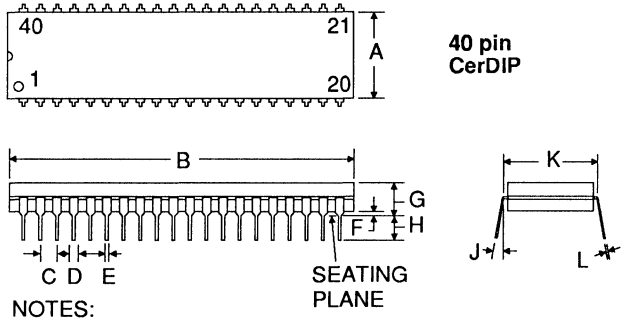

40 pin CerDIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.70	15.37	0.500	0.605
B	50.29	52.57	1.980	2.070
C	2.54 BSC		0.100 BSC	
D	1.27	1.65	0.050	0.065
E	0.38	0.56	0.015	0.022
F	0.51	1.27	0.020	0.050
G	4.06	5.84	0.160	0.230
H	2.92	4.06	0.115	0.160
J	5°	15°	5°	15°
K	15.24 BSC		0.600 BSC	
L	0.20	0.30	0.008	0.012

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
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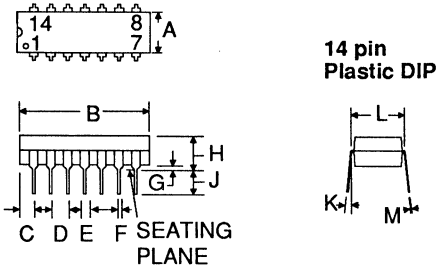
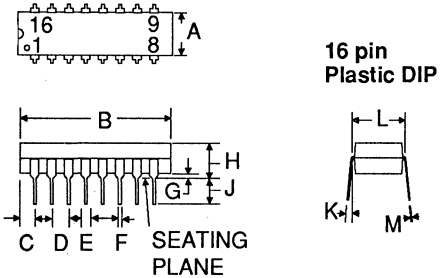


14 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.54	19.56	0.730	0.770
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

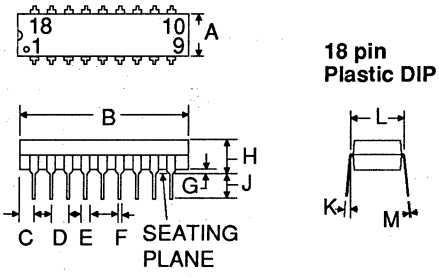


16 pin Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

13

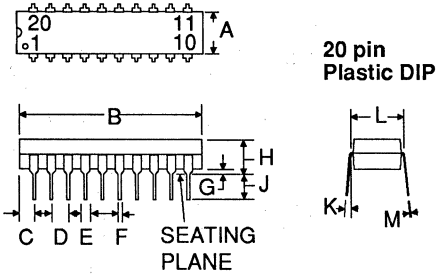


18 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	22.22	23.24	0.875	0.915
C	1.02	1.52	0.040	0.060
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.56	4.57	0.140	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

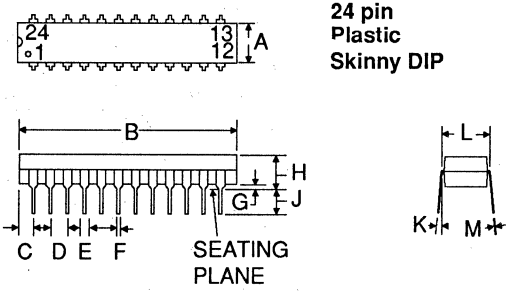


20 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	25.65	26.42	1.010	1.040
C	1.27	1.78	0.050	0.070
D	2.54 BSC		0.100 BSC	
E	1.27	1.78	0.050	0.070
F	0.38	0.56	0.015	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.79	3.56	0.110	0.140
K	0°	15°	0°	15°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

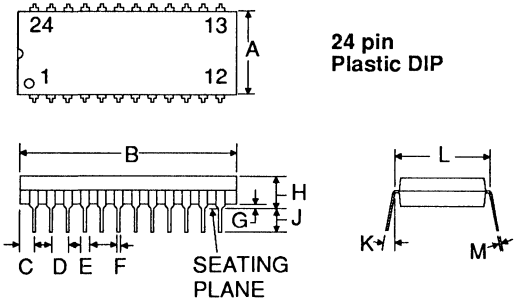


24 pin
Plastic
Skinny DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015

NOTES:

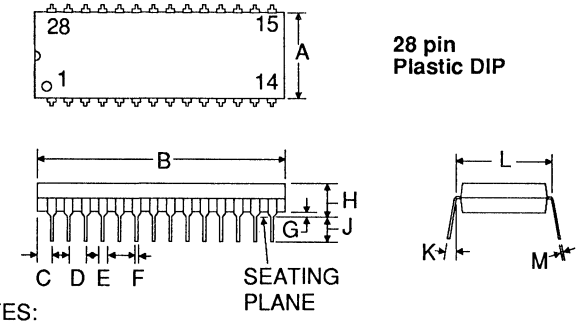
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



24 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

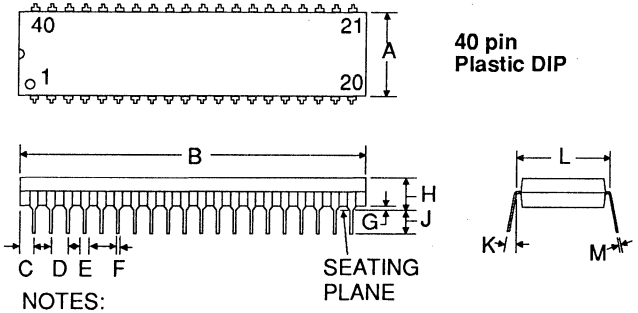
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



28 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

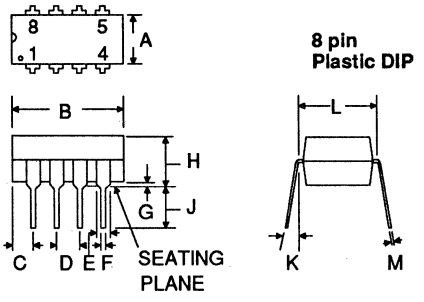


40 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	51.69	52.45	2.035	2.065
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

13

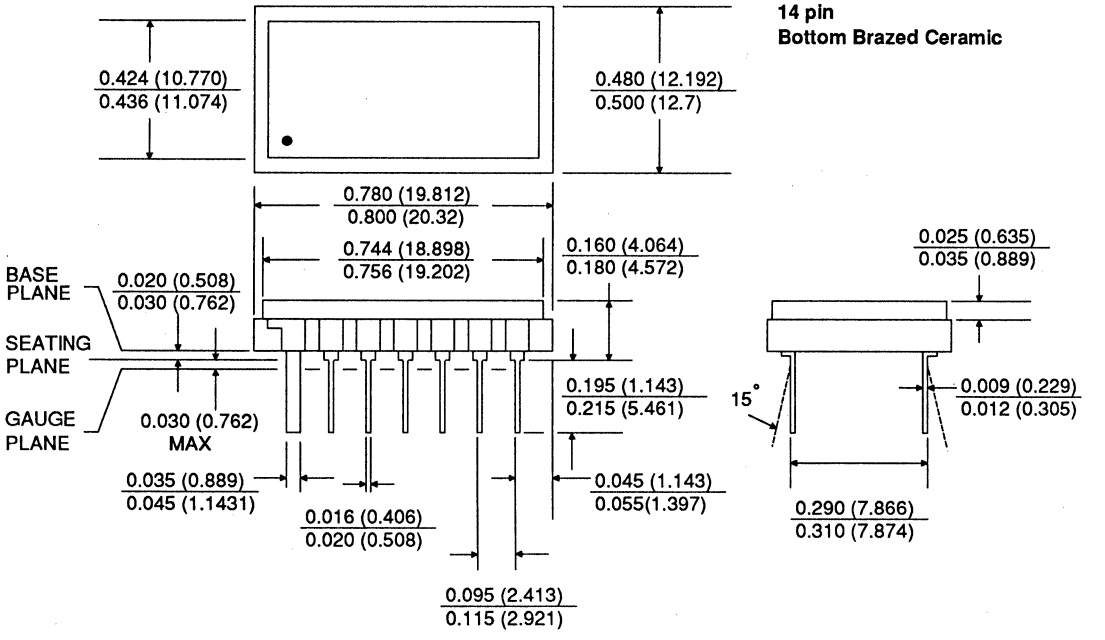


8 pin
Plastic DIP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

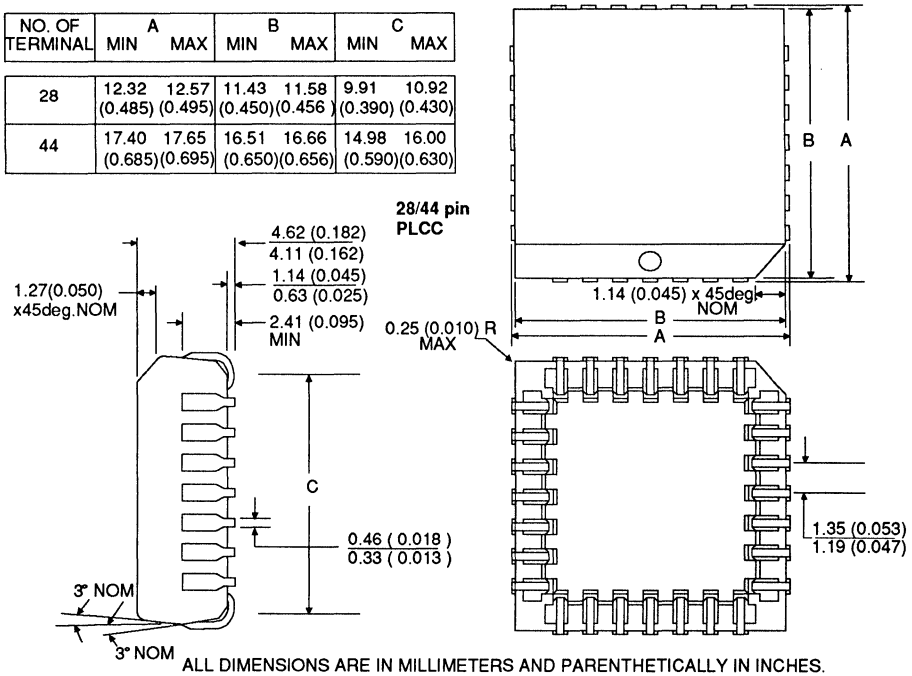
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



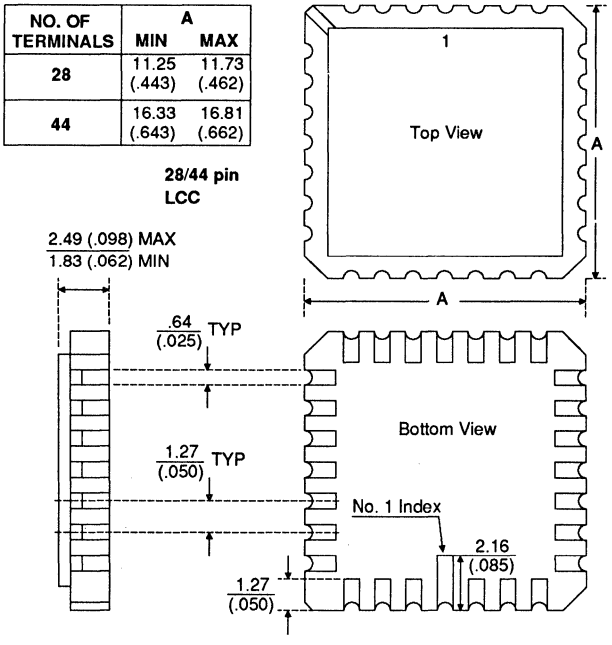
14 pin
Bottom Brazed Ceramic

NO. OF TERMINAL	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

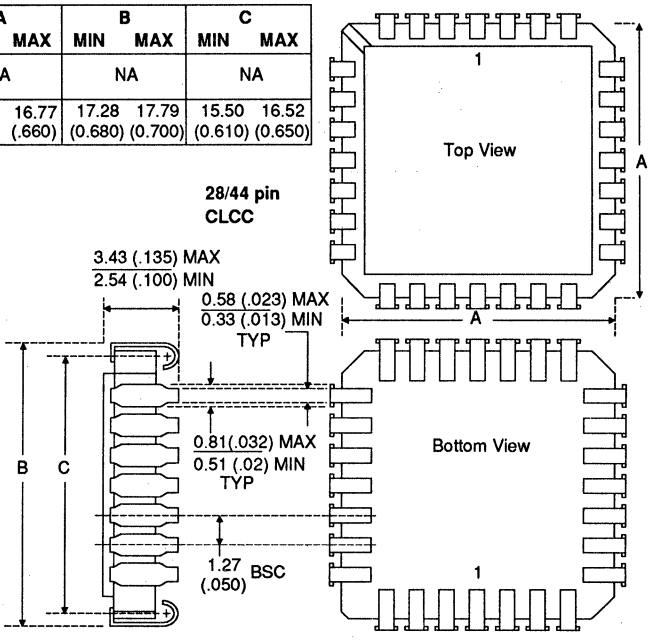
NO. OF TERMINALS	A MIN	A MAX
28	11.25 (.443)	11.73 (.462)
44	16.33 (.643)	16.81 (.662)



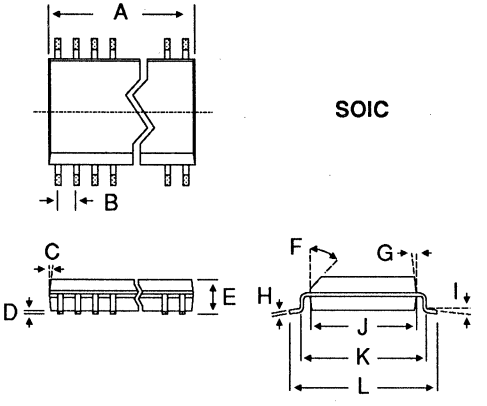
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

13

NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX	C MIN	C MAX
28	NA		NA		NA	
44	16.26 (.640)	16.77 (.660)	17.28 (0.680)	17.79 (0.700)	15.50 (0.610)	16.52 (0.650)



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



SOIC

pins	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	see table above			
B	1.27 BSC		0.050 BSC	
C	7° NOM		7° NOM	
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420

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