# TIMING TECHNOLOGY PRODUCTS

CYPRESS
IC DESIGNS DIVISION

TIMING TECHNOLOGY PRODUCTS

CYPRESS


# Timing Technology Products

# Data Book


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# Backgrounder

Founded in April 1983, Cypress Semiconductor Corporation produces high-performance integrated circuits for a range of growth markets. Cypress currently offers 250 products in 6 targeted product areas: static random access memories (SRAMs), programmable logic devices (PLDs), data communications, programmable read-only memories (PROMs), multichip modules, and timing technology devices. Cypress products address these markets as leaders in speed and functionality, taking advantage of the world's most advanced process technologies. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and test.

Cypress products all have one thing in common -- high performance. Cypress has built a reputation throughout the industry and with its customers for providing the highest-speed products in every market it enters. It continues to bring to market new, leading-edge products, produced with Cypress's CMOS (complementary metal-oxide semiconductor), BiCMOS, and Flash process technologies. Cypress has 0.8- and 0.65-micron CMOS and BiCMOS processes, a 0.5 micron BiCMOS process, and Flash at 0.65 micron. These process technologies allow Cypress to offer state-of-the-art products that provide the optimal balance of speed and power usage for any system. Development efforts are underway to further shrink the feature sizes of Cypress process technologies, thereby increasing speed, and decreasing die size and costs.

Cypress also offers a broad range of packaging options for its products, giving customers a variety of choices of cost, pin-out configurations, and temperature grades. In addition, all Cypress products are designed to meet or exceed the full temperature and functional requirements of military products. This means that Cypress builds products to military specifications as a matter of course.

Cypress's IC Designs Division, based in Kirkland, Washington, is the leading innovator in timing technology products. IC Designs products use frequency synthesis technology to offer a complete line of programmable clock oscillators for the world's leading personal computer manufacturers.

Frequency synthesis devices are built using phase-locked loops (PLLs), basic oscillators that are well known to analog circuit designers. In a frequency synthesis device, the entire functionality of a PLL is produced by a single monolithic integrated circuit. No external components are required, and sophisticated internal damping and filtering eliminate the adjustments that are often required in analog circuits. A frequency synthesis device behaves in the same way as a digital device, and can be incorporated into a circuit using familiar digital design principles and techniques.

Frequency synthesis technology was first applied to graphics cards in personal computers. Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), Video Graphics Array VGA, and other graphics systems write to the screen at different resolutions and intervals, and therefore require different reference frequencies. As these standards have proliferated, designs often call for as many as five different reference frequencies (i.e., five metal can oscillators) on a single board. Manufacturers of graphics boards have recognized the obvious cost and space advantages of frequency synthesis technology. The technology has found applications on computer motherboards as well.

As technology in the PC marketplace has become more complex, frequency synthesis technology has become an enabling technology -- the key to many new products and capabilities. The latest applications

for these devices include "green PCs," laptop computers, PentiumÀ) À-based and other high-performance systems, accelerator boards, multimedia video, and new generations of metal can oscillators.

IC Designs offers system logic products, graphic products, programmable products, and embedded crystal products. System logic products include clock generators for PC motherboards, workstations, laptops, and PC clones. Graphic products include a VGA clock generator, dual programmable clock generators for both graphics and ECL/TTL, and a low-voltage programmable graphics clock generator. IC Designs programmable products include both a programmable clock oscillator and a dual programmable clock oscillator. Embedded crystal products include the programmable products with embedded reference crystals, and QuiXTAL, the innovative, one-time programmable metal can oscillator.

IC Designs products are used widely in personal computers and mass storage systems. IC Designs clock oscillators control the intricate timing of all aspects of a computer system, including signals for the computer's central processing unit (CPU), keyboard, disk drives, system bus, serial port, and real-time clock. They replace all of the metal can oscillators used in the system.

IC Designs' QuiXTAL is a programmable metal can oscillator which replaces individual oscillators used to control timing signals in virtually every type of electronics equipment. QuiXTAL can be programmed in just one day to any frequency, providing users the ability to make last-minute frequency adjustments, speeding time to market. QuiXTAL takes frequency synthesis beyond the PC market, and addresses the broad market segments of electronic instrumentation, telecommunications equipment, and medical systems.

IC Designs products will be produced in Cypress's production facilities in San Jose, California; Round Rock, Texas; and Bloomington, Minnesota. Cypress's high-volume, low-cost manufacturing capability and IC Designs' expertise in timing technology are yielding new, faster products for this rapidly growing market.

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# Motherboard Frequency Synthesizers

# 1 – Motherboard Frequency Synthesizers 1

# ICD2023

## PC Motherboard Clock Generator

**Industry Standard Single-Chip Oscillator for 486/386/286 Personal Computer Motherboards**

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- 7 Independent Clock Outputs Handle all Clocking Requirements for Personal Computer Motherboards
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Programmable Frequency Range: 10 MHz – 80 MHz with 50% Duty Cycle
- Ideally Suited for PC Desktop and Laptop Computer Applications
- Sophisticated Internal Loop-Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- Battery Input Maintains 32.768 KHz Clock During Power-Down
- 3-State Oscillator Control Disables Outputs for Test Purposes
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 20-Pin SOIC Package Configuration

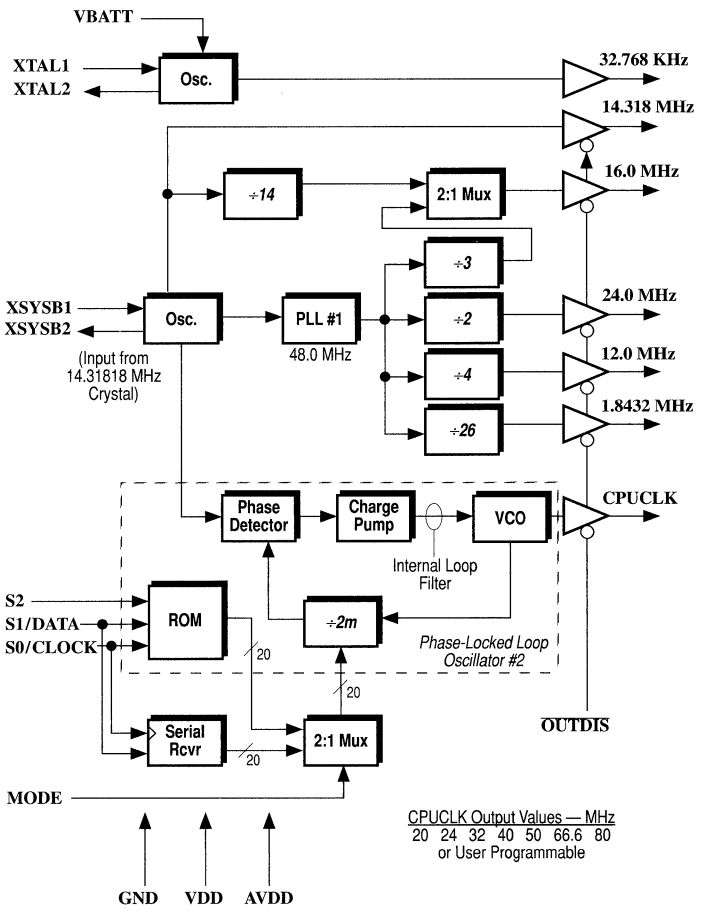


**Fig. 1: ICD2023 Block Diagram**

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# Introduction

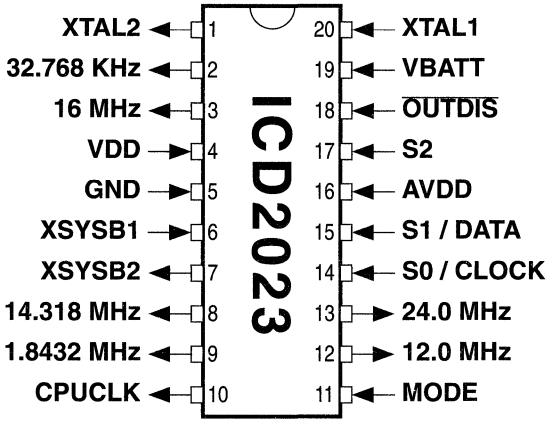


A modern personal computer motherboard often requires as many as six different crystal can oscillators. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of the oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2023 PC-AT Motherboard Clock Generator offers 2 oscillators, 2 phase-locked loops and 7 different outputs in a single package. Six of the outputs are of a fixed value while the seventh oscillator is fully user-programmable and may be changed "on the fly" to any desired frequency value between 10 MHz and 80 MHz. The ICD2023 is ideally suited for use in both existing designs (since it requires no support from the motherboard chip set and outputs 7 frequencies concurrently) and new designs which can utilize the programmable nature of this device.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions




## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | XTAL2 | Oscillator Output to a 32.768 KHz Parallel-Resonant Crystal |
| 2 | 32.768 KHz | 32.768 KHz Output |
| 3 | 16 MHz | 16 MHz Output |
| 4 | VDD | +5V to I/O Ring |
| 5 | GND | Ground |
| 6 | XSYSB1 | Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock Signal may be used as input if available. |
| 7 | XSYSB2 | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more information on crystal requirements, please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |

## Table 1: Signal Descriptions (Continued)

| Pin # | Signal | Function |
|---|---|---|
| 8 | 14.318 MHz | 14.31818 MHz Output |
| 9 | 1.8432 MHz | 1.8432 MHz Output |
| 10 | CPUCLK | CPUCLK Programmable Oscillator Output (See *Table 3: CPUCLK Output with MODE = 1* on page 9) |
| 11 | MODE | MODE=0, CPUCLK is in programmable mode<br>MODE=1, CPUCLK is in selection mode |
| 12 | 12.0 MHz | 12.0 MHz Output |
| 13 | 24.0 MHz | 24.0 MHz Output |
| 14 | S0 / CLOCK | MODE=0, S0 is serial clock input line for CPUCLK<br>MODE=1, S0 is select line for CPUCLK (Internal pull-up) |
| 15 | S1 / DATA | MODE=0, S1 is serial data input line for CPUCLK<br>MODE=1, S1 is select line for CPUCLK (Internal pull-up) |
| 16 | AVDD | +5 volts to Analog Core |
| 17 | S2 | MODE=0 & S2=1: CPUCLK=(14.31818 MHz) reference frequency<br>MODE=1, S2 is select line for CPUCLK (Internal pull-down) |
| 18 | $\overline{\text{OUTDIS}}$ | Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up for no-connect if 3-state operation is not needed.) |
| 19 | VBATT | +5V for battery backup operation |
| 20 | XTAL1 | Oscillator input from a 32.768 KHz crystal. For more information on crystal requirements, please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. |

# General Considerations

## Fixed Frequency Oscillator Operation

The following table describes each output:

**Table 2: Fixed Frequency Oscillator Outputs**

| Output Clock Function | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error | Notes |
|---|---|---|---|---|
| Real-Time Clock | 32.768 KHz | 32.768 KHz | 0 | Pass-through 32.768 KHz XTAL |
| System Bus | 14.318 | 14.318 | 0 | Pass-through 14.31818 MHz XTAL |
| Int. Bus Clock | 16.000 | 15.983 | 1058 | VCO = 47.94295 / 3 |
| Keyboard Clock | 12.000 | 11.987 | 1058 | VCO = 47.94295 / 4 |
| Floppy Disk Clock | 24.000 | 23.975 | 1058 | |
| Serial Port | 1.843 | 1.844 | 543 | |

## CPUCLK Programmable Oscillator: Selection Mode

CPUCLK is the programmable oscillator offering two modes of operation. The first mode uses three select lines to select one of 8 different preset frequencies, while the other mode allows the user to program any desired frequency between 10 MHz and 80 MHz. The two different modes are controlled by the MODE signal.

When MODE = 1, the selection lines can be changed to choose different frequencies. When this occurs, PLL #2 section will immediately seek the newly selected frequency as shown in the following table. During the transition period, the CPUCLK output will not glitch.

## Table 3: CPUCLK Output with MODE = 1

| S2 | S1 | S0 | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 20.000 | 20.0454 | 2272 |
| 0 | 0 | 1 | 24.000 | 23.9746 | 1058 |
| 0 | 1 | 0 | 32.000 | 32.0455 | 1422 |
| 0 | 1 | 1 | 40.000 | 40.0909 | 2272 |
| 1 | 0 | 0 | 50.000 | 49.9923 | 154 |
| 1 | 0 | 1 | 66.667 | 66.5962 | 57 |
| 1 | 1 | 0 | 80.000 | 80.1818 | 2272 |
| 1 | 1 | 1 | 100.000[a] | 99.8182 | 1818 |

a. Duty cycle specs not guaranteed above 80 MHz

## CPUCLK Programmable Oscillator: Serial Mode

When MODE = 0, CPUCLK enters its programmable mode. Signals S0 (clock) and S1 (data) become a serial interface, allowing a 20-bit number to be shifted in. The ICD2023 programmable oscillator (CPUCLK) requires a 20-bit programming word (W). This word contains 4 fields:

## Table 4: Programming Word Bit Fields

| Field | # of Bits | Notes |
|---|---|---|
| Index (I) | 4 | MSB (Most Significant Bits) |
| P Counter value (P') | 7 | |
| Mux (M) | 3 | |
| Q Counter Value (Q') | 6 | LSB (Least Significant Bits) |

If signal S2=1 and MODE=0, then the reference frequency (14.31818 MHz) is multiplexed to the CPUCLK output. This enables a glitch-free transition to the reference frequency while the VCO stabilizes.

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency = 14.31818 MHz.

The value of $f_{(VCO)}$ should be kept between 40 MHz and 80 MHz. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be multiplied up into the required range. The mux bits allow a post-divide of the higher VCO to bring the output to those desired values below 40 MHz.

**Table 5: Mux Bits $M_0$–$M_1$**

| $M_1$ | $M_0$ | Divisor |
|---|---|---|
| 0 | 0 | 16 |
| 0 | 1 | 4 |
| 1 | 0 | 2 |
| 1 | 1 | 1 |

The M2 mux bit is used to select which one of the two Phase-Locked Loops is to be utilized in the CPUCLK output. Normally, the PLL #2 section (see *Fig. 1: ICD2023 Block Diagram* on page 3) is used. However, if the desired output frequency requires $f_{(VCO)}$ to be set to 48 MHz, then PLL #1 section should be used. This both reduces power consumption (since only one VCO is activated) and eliminates the possibility of jitter which can arise when 2 VCOs of the same frequency beat (heterodyne) against each other.

**Table 6: Mux Bit $M_2$**

| $M_2$ | CPUCLK |
|---|---|
| 0 | PLL #2 |
| 1 | PLL #1 (48 MHz) |

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$, rather than to the desired output frequency.)

**Table 7: Index Field (I)**

| I | $f_{(VCO)}$ MHz |
|---|---|
| 0001 | 40.0 – 47.5 |
| 0010 | 47.5 – 52.2 |
| 0011 | 52.2 – 56.3 |
| 0100 | 56.3 – 61.9 |
| 0101 | 61.9 – 65.0 |
| 0110 | 65.0 – 68.1 |
| 0111 | 68.1 – 80.0 |
| 1111 | Turn off VCO |

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

## Programming Constraints

There are five primary programming constraints the user must be aware of:

$$f_{(REF)} = 14.31818\,MHz$$

$$200KHz \le \frac{f_{(REF)}}{Q} \le 1MHz$$

$$40MHz \le f_{(VCO)} \le 80MHz$$

$$3 \le Q \le 65$$

$$4 \le P \le 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the ***BitCalc*** program all of these constraints become transparent.

## ICD2023 Programming Example

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 40 MHz, double it to 79.0 MHz. Set M2, M1 and M0 to 0, 1 and 0, respectively. Set I to 0111. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

**Table 8: Possible P & Q values**

| P | Q | $f_{(VCO)}$ | Error (in ppm) |
|---|---|---|---|
| 69 | 25 | 79.0363 | 460 |
| 80 | 29 | 78.9969 | 40 |
| 91 | 33 | 78.9669 | 419 |

Choose (P, Q) = (80,29) as this results in the best accuracy (40 ppm).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \quad (4dH)$$

$$Q' = Q - 2 = 29 - 2 = 27 = 011011 \quad (1bH)$$

and the full programming word, W, is:

$$W = I, P', M, Q' = 0111, 1001101, 010, 011011 = 01111001101010011011 \quad (79a9bH)$$

A low-to-high transition on S0 is used to shift the programming word W into S1 as a serial bit stream, LSB first. (See the set-up and hold timing specifications elsewhere in this datasheet.) If more than 20 shifts are performed, only the last 20 data bits received will be retained.

## Output Frequency Accuracy

The accuracy of the ICD2023 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2023 are an integral fraction of the input reference frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2023 normally produces an output frequency within 0.1% of the target frequencies listed. This is more than sufficient to meet standard motherboard requirements. Specifics regarding accuracy are available from the output of the ***BitCalc*** program.

## 3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state all the clock output lines (except 32.768 KHz). This supports wired-or connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required.

## No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2023.

## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Notes *Power Feed and Board Layout Issues* on page 281 and *Minimizing Radio Frequency Emissions* on page 285 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2023 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2023 closest to the device requiring the highest frequency. If the high-frequency clocks must be routed to board extremes, the ICD2031 distributed "satellite" oscillators should be considered.

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is 14.31818 MHz, and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

## Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for motherboard designs.



## Temperature and Process Sensitivity

Because of its feedback circuitry, the IC DESIGNS is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the IC DESIGNS, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

## VBATT

The VBATT input powers the Real-Time Clock Oscillator (RTC). The backup power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable.

## Crystal Operation

The following diagram details the proper way to hook up the two reference crystals. See the IC DESIGNS Application Note titled *Crystal Oscillator Topics* on page 292 for specifics regarding recommended crystals.

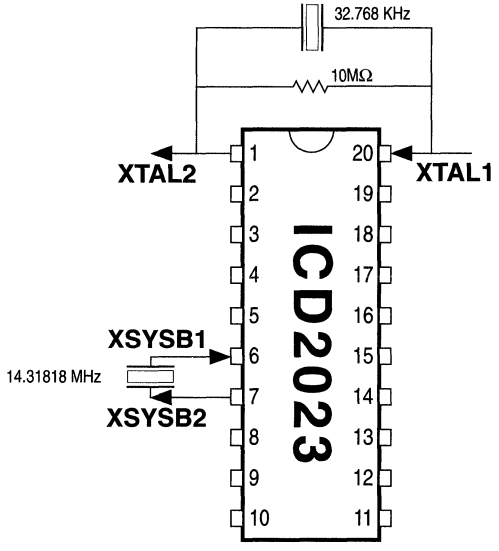



**Fig. 3: Crystal Schematic**

# Ordering Information

## Table 9: Order Codes

| Part Number | Package Type | Temperature Range | Clock Output Options |
|---|---|---|---|
| **ICD2023** | S = 20-Pin SOIC | C = Commercial[a] | 2 = CPUCLK ROM A, 16 MHz Output |

a. 0°C to +70°C

Example: order ICD2023SC–2 for the ICD2023, 20–pin SOIC, commercial temperature range device which utilizes the CPUCLK ROM Option A table of frequency decodes and provides a 16 MHz output on pin 3. Custom CPUCLK ROM decodes are available by special order.

# Device Specifications

## Electrical Data

### Table 10: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 375 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 11: DC Characteristics

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{BATT}$ | Backup battery voltage | 2.0 | 5.0 | Volts | typ. = 3.0 Volts |
| $V_{IH}$ | High-level input voltage | 2.0 | | Volts | |
| $V_{IL}$ | Low-level input voltage | | 0.8 | Volts | |
| $V_{OH}$ | High-level CMOS output voltage | 2.4 | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output voltage | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $I_{IH}$ | Input high current | | 150 | µA | $V_{IH} = V_{DD} - 0.5V$ |
| $I_{IL}$ | Input low current | | –250 | µA | $V_{IL}$ = 0.5V |
| $I_{OZ}$ | Output leakage current | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | 25 | 65 | mA | |
| $I_{DD-TYP}$ | Power supply current (typical) | | 40 | mA | CPUCLK = 66 MHz |
| $I_{BATT}$ | Backup battery current | | 50 | µA | $V_{BATT}$ = 3.0V |
| $I_{BATT-TYP}$ | Backup battery current (typical) | | 8 | µA | $C_L$ = 10pF |

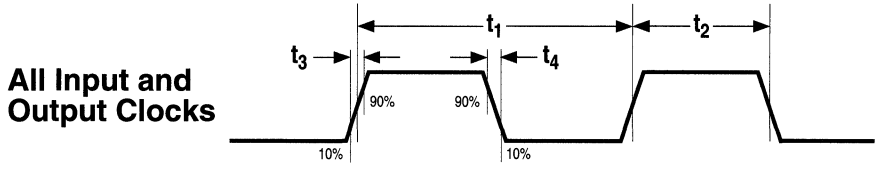
## Table 12: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | CPUCLK | Reference Oscillator Output | 10 | | 80 | MHz |
| $t_1$ | ref freq | Reference Oscillator nominal value | | | 14.318 | MHz |
| $t_2$ | duty cycle | Duty cycle for the output oscillators defined as $t_2 \div t_1$ | 40% | | 60% | |
| $t_3$ | rise time | Rise time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_4$ | fall time | Fall time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_5$ | set-up | Delay required after MODE goes low prior to starting the S0 clock line | | | 0 | ns |
| $t_6$ | cycle time | Minimum cycle time for the S0 clock | 200 | | | ns |
| $t_7$ | set-up | Time required for the data to be valid prior to the rising edge of S0 / CLOCK | 10 | | | ns |
| $t_8$ | hold | Time required for the data to remain valid after the rising edge of S0 / CLOCK | 5 | | | ns |
| $t_9$ | clk unstable | Time CPUCLK oscillator remains valid after MODE signal goes low | | | 0 | ns |
| $t_{10}$ | clk stable | Time required for the CPUCLK oscillator to become valid after last S0 clock | | | 10 | msec |
| $t_{11}$ | clk unstable | Time the output oscillators remain valid after the S0, S1 or S2 select signals change value | | | 0 | ns |
| $t_{12}$ | clk stable | Time required for the output oscillators to become valid after the S0, S1 or S2 select signals change value | | | 10 | msec |
| $t_{13}$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion | | | 12 | ns |
| $t_{14}$ | clk valid | Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high | | | 12 | ns |

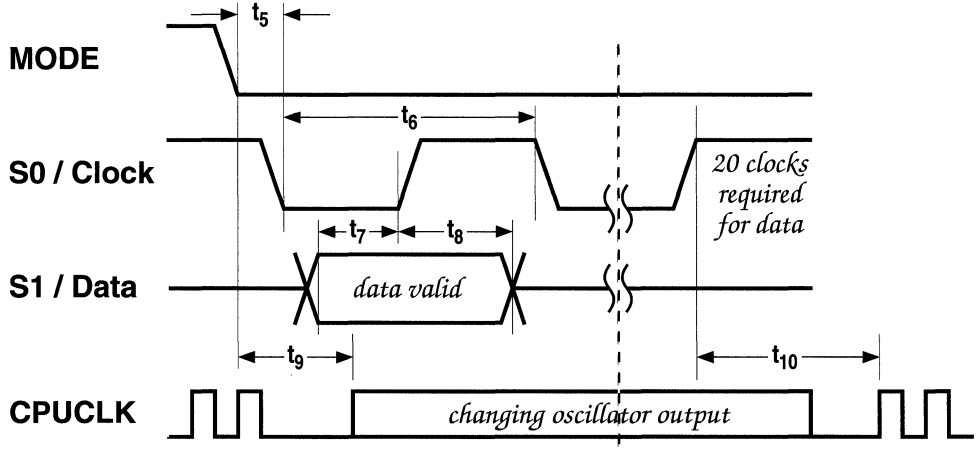
**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

## Timing Diagrams

### Fig. 4: Rise and Fall Times

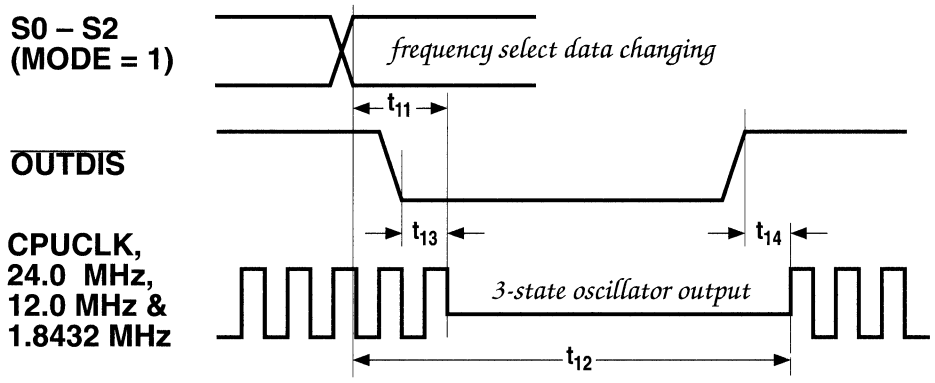



### Fig. 5: Serial Programming Timing



1

## Fig. 6: 3-State Timing



# Revision History / Credits

V2.7 (11/15/93) — Final Release Version

# ICD2025

## Motherboard Clock Generator

**Single-Chip Dual Oscillator for Personal Computer Motherboard Designs**

1

- 3 Independent Clock Outputs: Separate CPUCLK, SYSCLK and Buffered Reference Clock
- Ideally Suited for 386/486 Motherboard Applications
- Phase-Locked Loop Output Range of 1.843 MHz – 100 MHz
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 3-State Oscillator Control Disables Outputs for Test Purposes
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 16-Pin SOIC Package

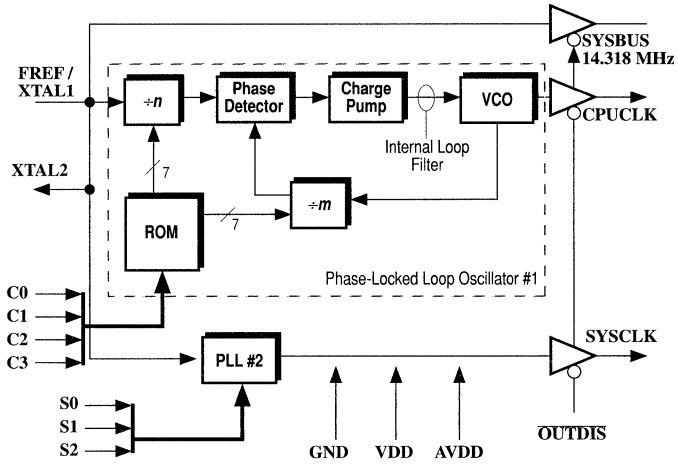



**Fig. 1: ICD2025 Block Diagram**

**Table 1: Available Frequencies**

| SYSCLK (MHz) | CPUCLK |
|---|---|
| 1.843 | 16.000 |
| 3.686 | 20.000 |
| 8.000 | 25.000 |
| 12.000 | 32.000 |
| 18.432 | 33.333 |
| 20.000 | 40.000 |
| 24.000 | 50.000 |
| 32.000 | 66.667 |
| | 80.000 |
| | 100.000 |

# Contents



# Figures



# Tables

# Introduction

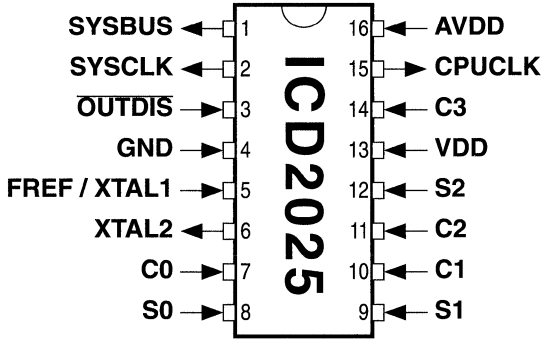
The emergence of new, highly integrated core logic chip sets has significantly simplified the clocking requirements of inexpensive PC-clone motherboards. The ICD2025 is intended to offer a low-cost approach to the generation of the necessary three clocks typically required.



While lower in cost than other IC DESIGNS motherboard devices which offer greater functionality, the ICD2025 still maintains the consistently high quality level our customers have come to expect: full temperature test, complete functional test and (still) the industry's only jitter screening test.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions



## Table 2: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | SYSBUS | Buffered Reference Frequency Output (14.31818 MHz) |
| 2 | SYSCLK | System Clock Oscillator Output (see *Table 4: SYSCLK Selection* on page 29) |
| 3 | $\overline{\text{OUTDIS}}$ | Output Disable (Enable 3-State Output) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation not needed). |
| 4 | GND | Ground |
| 5 | FREF / XTAL1 | Input Reference Oscillator (nominally 14.31818 MHz) A crystal may be used if a reference oscillator is not available. |
| 6 | XTAL2 | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |
| 7 | C0 | CPUCLK Selection Signal — Bit 0 (internal pull-up) |
| 8 | S0 | SYSCLK Clock Selection Signal — Bit 0 (internal pull-up) |
| 9 | S1 | SYSCLK Selection Signal — Bit 1 (internal pull-up) |
| 10 | C1 | CPUCLK Selection Signal — Bit 1 (internal pull-up) |
| 11 | C2 | CPUCLK Selection Signal — Bit 2 (internal pull-up) |
| 12 | S2 | SYSCLK Selection Signal — Bit 2 (internal pull-up) |
| 13 | VDD | +5V to I/O Ring |
| 14 | C3 | CPUCLK Selection Signal — Bit 3 (internal pull-down) |
| 15 | CPUCLK | CPU Clock Oscillator Output (see CPUCLK Selection Table) |
| 16 | AVDD | +5V to Analog Core |

# General Considerations

## CPU and System Clock Oscillator Selection

The output frequency value of the CPU clock oscillator (CPUCLK) is selected by the four CPU clock selection inputs: C0, C1, C2, and C3. This feature allows the ICD2025 to support different CPU speeds. The output frequency value of the system clock oscillator (SYSCLK) is selected by the three system clock selection inputs: S0, S1, and S2. The selection tables are shown below.

At any time during operation, the selection lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the 14.31818 MHz reference signal until the PLL settles to the new frequency. The timing for this transition is detailed in *Table 8: AC Characteristics* on page 34.

### Table 3: CPUCLK Selection

| C3 | C2 | C1 | C0 | Word | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 40.000 | 39.812 | 4734 |
| 0 | 0 | 0 | 1 | 1 | 80.000 | 79.623 | 4734 |
| 0 | 0 | 1 | 0 | 2 | 33.333 | 33.322 | 320 |
| 0 | 0 | 1 | 1 | 3 | 66.667 | 66.645 | 335 |
| 0 | 1 | 0 | 0 | 4 | 25.000 | 25.000 | 0 |
| 0 | 1 | 0 | 1 | 5 | 50.000 | 50.000 | 0 |
| 0 | 1 | 1 | 0 | 6 | 16.000 | 15.923 | 4848 |
| 0 | 1 | 1 | 1 | 7 | 32.000 | 31.846 | 4848 |
| 1 | 0 | 0 | 0 | 8 | 20.000 | 19.906 | 4734 |
| 1 | 0 | 0 | 1 | 9 | 100.000 | 99.840 | 1600 |
| 1 | 0 | 1 | 0 | 10 | 40.000 | 39.812 | 4734 |
| 1 | 0 | 1 | 1 | 11 | 80.000 | 79.623 | 4734 |
| 1 | 1 | 0 | 0 | 12 | 33.333 | 33.322 | 320 |
| 1 | 1 | 0 | 1 | 13 | 66.667 | 66.645 | 335 |
| 1 | 1 | 1 | 0 | 14 | 25.000 | 25.000 | 0 |
| 1 | 1 | 1 | 1 | 15 | 50.000 | 50.000 | 0 |

**Table 4: SYSCLK Selection**

| S2 | S1 | S0 | Word | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 18.432 | 18.431 | 62 |
| 0 | 0 | 1 | 1 | 20.000 | 20.003 | 167 |
| 0 | 1 | 0 | 2 | 24.000 | 23.998 | 80 |
| 0 | 1 | 1 | 3 | 1.843 | 1.843 | 144 |
| 1 | 0 | 0 | 4 | 12.000 | 11.999 | 80 |
| 1 | 0 | 1 | 5 | 8.000 | 8.001 | 167 |
| 1 | 1 | 0 | 6 | 3.686 | 3.687 | 144 |
| 1 | 1 | 1 | 7 | 32.000 | 32.005 | 167 |

## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at the higher system clock frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. It is important that the ground plane be nearly continuous with a minimum of cuts, holes, or breaks. Both analog and digital ground pins should go directly to this plane.

To produce an output of high spectral purity, additional supply noise precautions might be required, particularly in noisy environments. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and AVDD can help to filter noisy supply lines.

The designer should also avoid routing the two output traces of the ICD2025 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2025 closest to the device requiring the highest frequency. For more details concerning layout and power considerations, please see the IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281.

## Output Frequency Accuracy

The accuracy of the ICD2025 output frequencies depends on the target output frequencies. The tables within this document contain target frequencies which differ from the actual frequencies produced by the clock synthesizer.

The output frequencies of the ICD2025 are an integral fraction of the input (reference) frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2025 always produces an output frequency within 0.1% of the target frequencies listed, which is more than sufficient to meet standard system logic requirements. (Actual values are given in the tables.)

## 3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state the SYSCLK, CPUCLK and SYSBUF output lines. This supports procedures such as automated testing, where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up but should be tied to VDD if not used.

## No External Components Required

Under normal conditions no external components other than a reference crystal are required for proper operation of any of the internal circuitry of the ICD2025.

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is typically 14.31818 MHz (as derived from the PC system bus) and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.



The package leadframes are optimized for the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground-bounce and output crosstalk.

## Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough for system logic applications.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2025 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures the loop filter will track the same process variations as does the VCO. With the ICD2025, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

# Ordering Information

## Table 5: Order Codes

| Part Number | Package Type | Temperature Range |
|---|---|---|
| ICD2025 | S = 16-Pin SOIC DIP | C = Commercial[a] |

a. 0°C to +70°C

Example: order ICD2025PC for the ICD2025, 16-pin plastic SOIC, commercial temperature range device.

# Device Specifications

## Electrical Data

### Table 6: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 350 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 7: DC Characteristics

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2.0 | | Volts | |
| $V_{IL}$ | Low-level input voltage | | 0.8 | Volts | |
| $V_{OH}$ | High-level CMOS output voltage | 2.4 | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output voltage | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $I_{IH}$ | Input high current | | 150 | µA | $V_{IH}$ = 5.25V |
| $I_{IL}$ | Input low current | | –250 | µA | $V_{IH}$ = 0V |
| $I_{OZ}$ | Output leakage current | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | | 50 | mA | (@ hi freq) |
| $I_{ADD}$ | Analog Power Supply Current | | 6 | mA | |

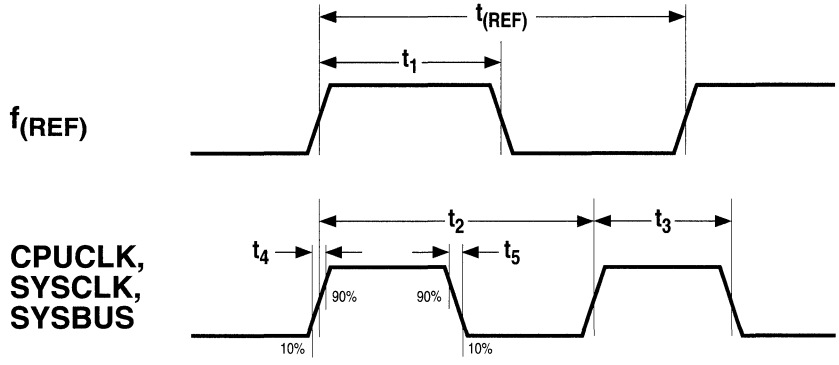
## Table 8: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value | 4 | 14.318 | 26 | MHz |
| $t_{(REF)}$ | reference clock period | $1 \div f_{(REF)}$ | 38.5 | 69.8 | 2500 | ns |
| $t_1$ | input duty cycle | Duty cycle for the input oscillator defined as $t1 \div t_{(REF)}$ | 25% | 50% | 75% | |
| $t_2$ | output period | CPUCLK oscillator value | 8.3<br>120 MHz | | 2857<br>350 KHz | ns |
| $t_3$ | output duty cycle | Duty cycle for the output oscillator defined as $t_3 \div t_2$ (measured at 2.5V) | 40% | | 60% | |
| $t_4$ | rise time | Rise time for the output oscillator into a 25pF load | | | 3 | ns |
| $t_5$ | fall time | Fall time for the output oscillator into a 25 pF load | | | 3 | ns |
| $t_6$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion | | | 12 | ns |
| $t_7$ | clk valid | Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high | | | 12 | ns |
| $t_{MUXREF}$ | clk stable | Time required for the output oscillators to become valid after C0–C3 or S0–S2 select signals change value | 3.4 | 5 | 6.9 | msec |
| $t_{freq1}$ | freq1 output | Old frequency output | | | | |
| $t_{freq2}$ | freq2 output | New frequency output | | | | |
| $t_A$ | $f_{(REF)}$ mux time | Time clock output remains high while output muxes to reference frequency | $\frac{t_{(REF)}}{2}$ | | $3\frac{t_{(REF)}}{2}$ | ns |
| $t_B$ | $t_{freq2}$ mux time | Time clock output remains high while output muxes to new frequency value | $\frac{t_{freq2}}{2}$ | | $3\frac{t_{freq2}}{2}$ | ns |

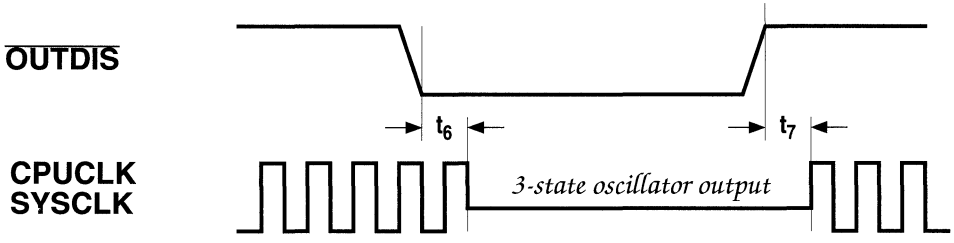
**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

## Timing Diagrams

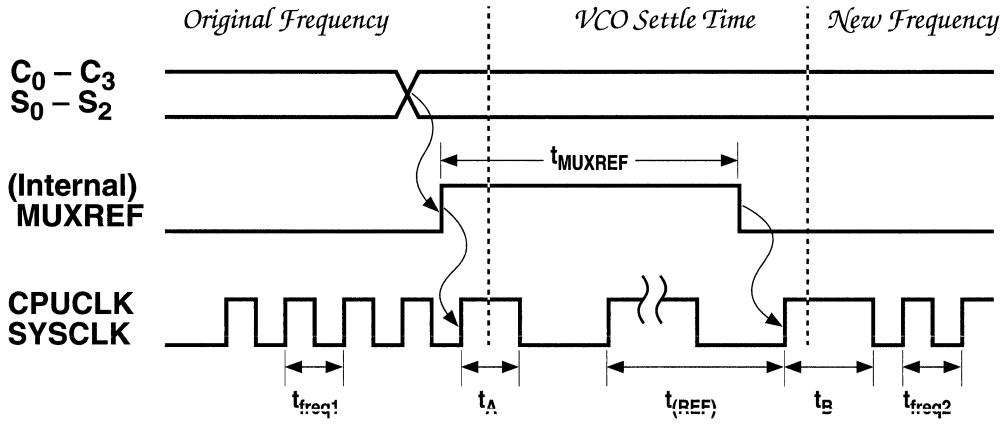
### Fig. 3: Rise and Fall Times




### Fig. 4: 3-StateTiming



## Fig. 5: Selection Timing



# Revision History / Credits

V1.4 (11/15/93) — Final Release Version

# ICD2027

## PC Motherboard Clock Generator

**Single-Chip Oscillator Ideally Suited for 486/386/286 Laptop/Notebook Computer Applications**

1

- 6 Clock Outputs Handle all Clocking Requirements for Personal Computer Motherboards
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Frequency Range from 760 KHz – 100 MHz with 50% Duty Cycle
- 2 Power-Down Modes — Hardware Pin and Programmable Software Mode
- Concurrent and Low Skew ÷1 and ÷2 CPUCLK Outputs
- Ideally Suited for PC Desktop, Laptop and Notebook Computer Applications
- Battery Input Maintains 32.768 KHz Clock During Power-Down
- 3-State Oscillator Control Disables Outputs for Test Purposes
- Sophisticated Internal Loop-Filter Requires no External Components
- 5V, Low-Power, High-Speed CMOS Technology
- Available in 20-Pin SOIC Package Configuration

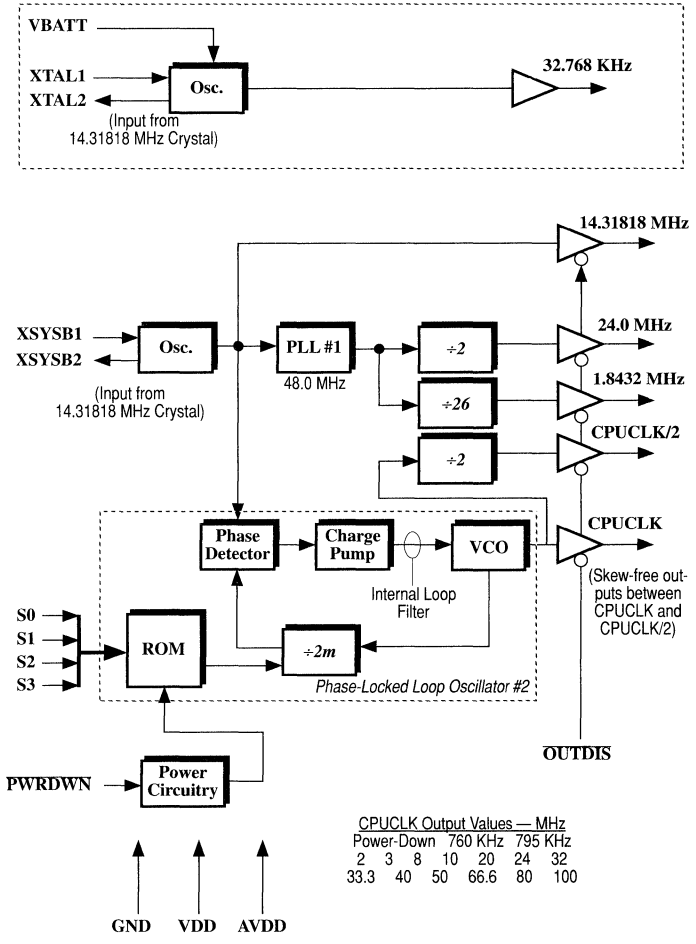



**Fig. 1: ICD2027 Block Diagram**

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# Figures



# Tables

# Introduction

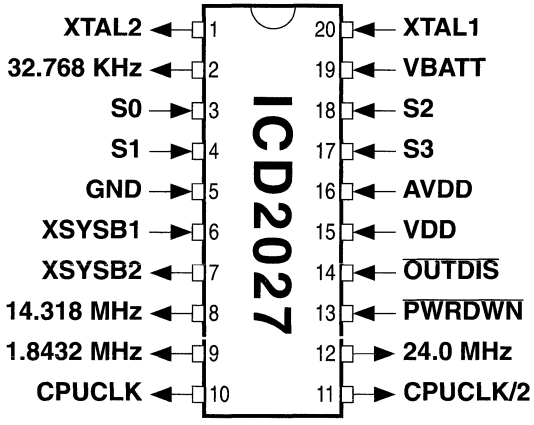


A modern personal computer motherboard often requires as many as six different crystal can oscillators per printed circuit board. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of the oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2027 PC Motherboard Clock Generator offers 2 oscillators, 2 phase-locked loops, and 6 different outputs in a single package. Four of the outputs are of a fixed value while the other two may be changed "on the fly" to any one of 16 preset frequency values between 760 KHz and 100 MHz. The ICD2027 is ideally suited for use in new laptop/notebook designs due to its dual power-down modes. The ICD2027 also requires no support from the motherboard chip set and outputs all 6 frequencies concurrently.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions




## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | XTAL2 | Oscillator Output to a 32.768 KHz Parallel-Resonant Crystal |
| 2 | 32.768 KHz | 32.768 KHz Output |
| 3 | S0 | Bit 0 (LSB) of S0–S3, used to select CPUCLK frequency (Internal pull-down) |
| 4 | S1 | Bit 1 of S0–S3, used to select CPUCLK frequency (Internal pull-down) |
| 5 | GND | Ground |
| 6 | XSYSB1 | Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock Signal may be used as input if available. |
| 7 | XSYSB2 | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |

## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 8 | 14.318 MHz | 14.31818 MHz Output |
| 9 | 1.8432 MHz | 1.8432 MHz Output |
| 10 | CPUCLK | CPUCLK Programmable Oscillator Output (See *Table 2: CPUCLK ROM Selection Outputs* on page 44) |
| 11 | CPUCLK/2 | Half the frequency of CPUCLK. Output is phase-coherent with the CPUCLK output. |
| 12 | 24.0 MHz | 24.0 MHz Output |
| 13 | $\overline{\text{PWRDWN}}$ | Used to select Power Down mode when signal is pulled low (Pull-down) |
| 14 | $\overline{\text{OUTDIS}}$ | Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation not needed.) |
| 15 | VDD | +5V to I/O Ring |
| 16 | AVDD | +5V to Analog Core. See *Power Feed and Board Layout Issues* on page 281. |
| 17 | S3 | Bit 3 (MSB) of S0–S3, used to select CPUCLK frequency (Internal pull-down) |
| 18 | S2 | Bit 2 of S0–S3, used to select CPUCLK frequency (Internal pull-down) |
| 19 | VBATT | +2V to +5V used for battery backup operation. |
| 20 | XTAL1 | Real-Time Clock Input Reference Oscillator (nominal 32.768 KHz). |

# General Considerations

## CPUCLK Oscillator Operation

CPUCLK is the selectable oscillator. It uses 4 select lines to select 1 of 16 different preset frequencies. (Reference Frequency = 14.31818 MHz)

### Table 2: CPUCLK ROM Selection Outputs

| S3 | S2 | S1 | S0 | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0.7950[a] | $f_{(REF)}$ / 18 | 0 |
| 0 | 0 | 0 | 1 | 0.7950 | $f_{(REF)}$ / 18 | 0 |
| 0 | 0 | 1 | 0 | 33.3000 | 33.2981 | 57 |
| 0 | 0 | 1 | 1 | 0.7600 | 0.7599 | 75 |
| 0 | 1 | 0 | 0 | 2.0000 | 2.0003 | 167 |
| 0 | 1 | 0 | 1 | 3.0000 | 2.9968 | 1057 |
| 0 | 1 | 1 | 0 | 8.0000 | 8.0013 | 167 |
| 0 | 1 | 1 | 1 | 10.0000 | 10.0227 | 2273 |
| 1 | 0 | 0 | 0 | 20.0000 | 20.0455 | 2273 |
| 1 | 0 | 0 | 1 | 24.0000 | 23.9747 | 1057 |
| 1 | 0 | 1 | 0 | 32.0000 | 32.0053 | 167 |
| 1 | 0 | 1 | 1 | 40.0000 | 40.0909 | 2273 |
| 1 | 1 | 0 | 0 | 50.0000 | 50.0000 | 0 |
| 1 | 1 | 0 | 1 | 66.6000 | 66.5962 | 57 |
| 1 | 1 | 1 | 0 | 80.0000 | 80.1818 | 2273 |
| 1 | 1 | 1 | 1 | 100.0000 | 99.8182 | 1818 |

a. Soft Power-Down Mode

NOTE: The select lines have internal pull-downs so that in a system power-down situation, the power-down mode is chosen in the CPUCLK table as the default. Therefore, upon power-up, one of the select lines must be pulled high.

## Fixed Frequency Oscillator Operation

The following table describes each output:

### Table 3: Fixed Frequency Oscillators

| Output Clock Function | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error | Notes |
|---|---|---|---|---|
| Real-Time Clock | 32.768 KHz | 32.768 KHz | 0 | Pass-through 32.768 KHz XTAL |
| System Bus | 14.31818 | 14.31818 | 0 | Pass-through 14.31818 MHz XTAL |
| Floppy Disk Clock | 24.00000 | 23.97470 | 1058 | |
| Serial Port | 1.84320 | 1.84420 | 1058 | |

## Power-Down Operation

There are two power-down modes within the ICD2027. The first is the hardware mode. When Pin 13 is pulled low ($\overline{\text{PWRDWN}}$ = 0), the part is immediately forced into its lowest power mode. This shuts down everything but the 32.768 KHz oscillator and its output. All power is now supplied by the VBATT input. For minimum power consumption in power-down mode, all select lines should be set low and $\overline{\text{OUTDIS}}$ should be set high.

The second mode is a programmable soft power-down mode. This mode shuts down the two phase-locked loops and all outputs except for the CPUCLK output, which runs at 795 KHz — a frequency sufficient to refresh dynamic RAMs.

### Table 4: Soft Power-Down Mode (S0–S3 = 0000)

| Output Signal | Status |
|---|---|
| 32.768 KHz | 32.768 KHz |
| CPUCLK | 795.00 KHz |
| CPUCLK/2 | (shutdown) |
| 14.318 MHz | (shutdown) |
| 1.8432 MHz | (shutdown) |
| 24.000 MHz | (shutdown) |

## 3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state all the clock output lines (except 32.768 KHz). This supports wired-or connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required.

## Skew-Free ÷2 on CPUCLK/2

The CPUCLK/2 output is available concurrently as a ÷2 of the desired CPUCLK output. The ÷2 output is also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 1 ns of skew between the two outputs, with 2 ns guaranteed worst case.

## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz. When designing with this device, it is best to locate the ICD2027 closest to the device requiring the highest frequency.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Notes *Power Feed and Board Layout Issues* on page 281 and *Minimizing Radio Frequency Emissions* on page 285 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2027 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency of 14.31818 MHz goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output fre-

quency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

## VBATT

The VBATT input powers the Real-Time Clock Oscillator (RTC). The backup power is typically a 3V lithium battery; however, any voltage between +2V and +5V is acceptable.

## Crystal Operation

The following diagram details the proper way to hook up the two reference crystals. See the IC DESIGNS Application Note titled *Crystal Oscillator Topics* on page 292 for specifics regarding recommended crystals.

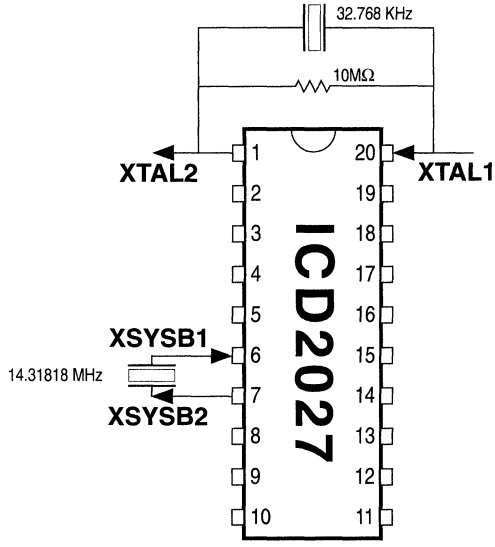



**Fig. 3: Crystal Schematic**

# Ordering Information

## Table 5: Order Codes

| Part Number | Package Type | Temperature Range | CPUCLK ROM Option |
|---|---|---|---|
| ICD2027 | S = 20-Pin SOIC DIP | C = Commercial[a] | 1 |

a. 0°C to +70°C

Example: order ICD2027SC–1 for the ICD2027, 20-pin plastic SOIC, commercial temperature range device which uses the standard CPUCLK ROM Option 1 table of frequency decodes. Custom CPUCLK ROM decodes are available by special order.

# Device Specifications

## Electrical Data

### Table 6: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 375 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 7: DC Characteristics

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2.0 | | Volts | |
| $V_{IL}$ | Low-level input voltage | | 0.8 | Volts | |
| $V_{OH}$ | High-level CMOS output voltage | 2.4 | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output voltage | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $V_{BATT}$ | Backup battery voltage | 2.0 | 5.0 | Volts | |
| $I_{IH}$ | Input high current | | 150 | µA | $V_{IH}$ = 5.25V |
| $I_{IL}$ | Input low current | | –250 | µA | $V_{IL}$ = 0V |
| $I_{OZ}$ | Output leakage current | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | 25 | 65 | mA | |
| $I_{DD-PD}$ | Soft power-down current | | 7.5 | mA | |
| $I_{BATT}$ | Backup battery current | | 15 | µA | typ. = 5 µA |

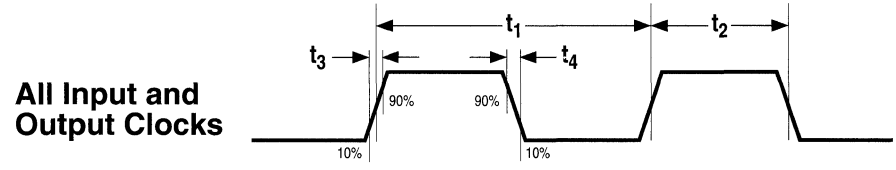
## Table 8: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_1$ | ref freq | Reference Oscillator nominal value | | | 14.318 | MHz |
| $t_2$ | duty cycle | Duty cycle for the output oscillators defined as $t_2 \div t_1$ | 40% | | 60% | |
| $t_3$ | rise time | Rise time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_4$ | fall time | Fall time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_5$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion | | | 12 | ns |
| $t_6$ | clk valid | Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high | | | 12 | ns |
| $t_7$ | CPUCLK/2 skew | Skew delay between the CPUCLK and the CPUCLK/2 outputs | | 1 | 2 | ns |
| $t_{(REF)}$ | reference period | $1 \div f_{(REF)}$ | | 69.8 | | ns |
| $t_{freq1}$ | freq1 output | Old frequency output | | | | |
| $t_{freq2}$ | freq2 output | New frequency output | | | | |
| $t_A$ | $f_{(REF)}$ mux time | Time clock output remains high while output muxes to reference frequency | $\frac{t_{(REF)}}{2}$ | | $3\frac{t_{(REF)}}{2}$ | ns |
| $t_B$ | $t_{freq2}$ mux time | Time clock output remains high while output muxes to new frequency value | $\frac{t_{freq2}}{2}$ | | $3\frac{t_{freq2}}{2}$ | ns |
| $t_{MUXREF}$ | | Time for VCO to settle between changes | | 6.2 | | msec |

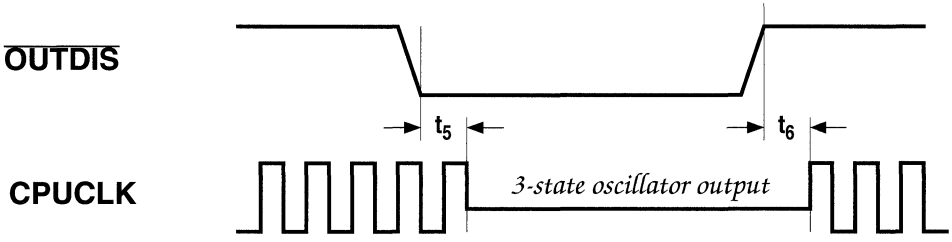
**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

## Timing Diagrams

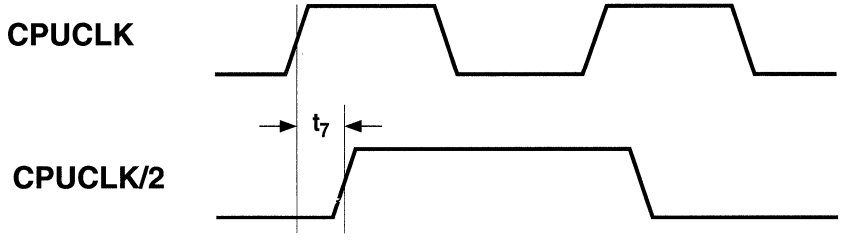
### Fig. 4: Rise and Fall Times



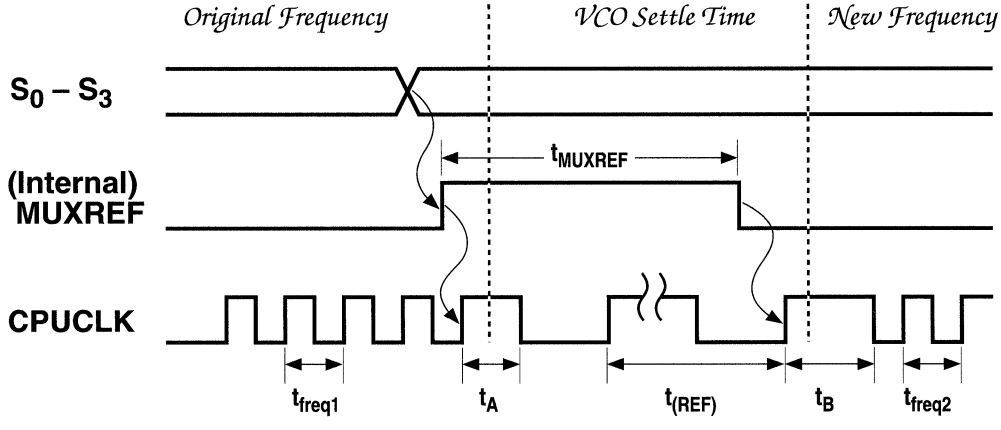

### Fig. 5: 3-StateTiming



## Fig. 6: CPUCLK Skew




## Fig. 7: Selection Timing



# Revision History / Credits

V1.7 (11/15/93) — Final Release Version

# ICD2028

## PC Motherboard Clock Generator

**Second-Generation Single-Chip Oscillator for Pentium™/486/386 PC Motherboards with 3.3V Support**

1

- 8 Independent Clock Outputs Handle all Clocking Requirements for Personal Computer Motherboards
- CPU Clock Frequency Range: 10 MHz – 100 MHz (5V) or 10 MHz – 80 MHz (3.3V) with User-Defined Duty Cycle
- 4 User-Configurable Outputs
- Skew-Free CPU Clock, CPU Clock ÷2 and Buffered CPU Clock Options
- Ideally Suited for PC Desktop Workstations
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Sophisticated Internal Loop-Filter Requires no External Components
- Battery Input Maintains 32.768 KHz Clock During Power-Down
- 3-State Oscillator Control Disables Outputs for Test Purposes
- 5V or 3.3V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 20-Pin SOIC Package Configuration

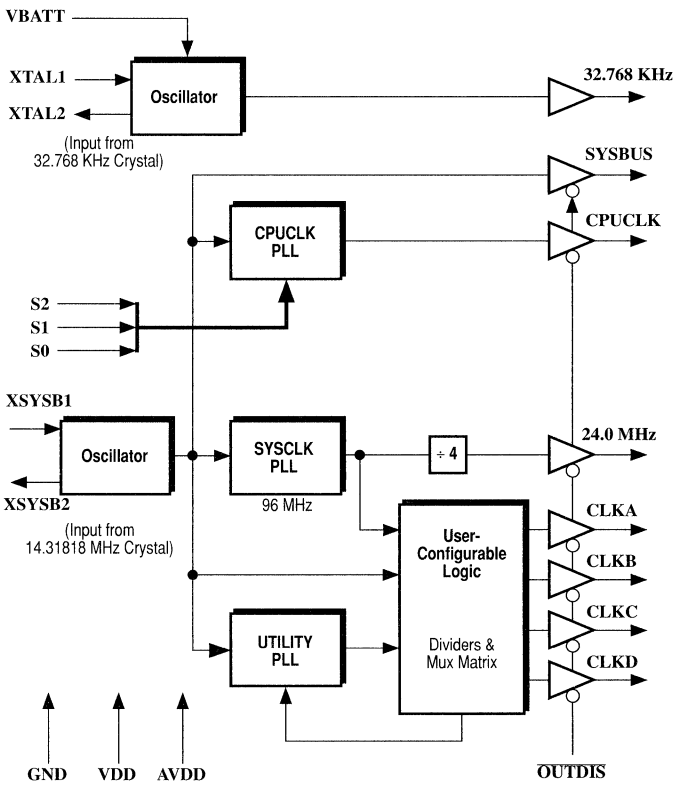



**Fig. 1: ICD2028 Block Diagram**

# Contents



# Figures



# Tables

# Introduction



A modern personal computer motherboard often requires as many as seven different crystal can oscillators. The System Logic Family of frequency synthesis parts from IC DESIGNS replaces the large number of oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2028 is a second-generation PC Motherboard Clock Generator built on the foundation of the industry-standard and most widely-used ICD2023. The ICD2028 offers most of the features of the ICD2023, as well as some important enhancements:

- An additional VCO
- An additional clock output
- Four customer-configured outputs
- A skew-free divided-by-two CPU clock
- An additional skew-free CPU clock
- User-definable CPUCLK output duty cycle
- 3.3V operation

Because today's PC desktop workstations must support a myriad of new requirements, and each company's implementation tends to be unique, the most important new features of the ICD2028 are its ability to tailor four of the outputs to the individual needs of today's system logic design engineer, and to configure the CPUCLK duty cycle for special microprocessor needs.

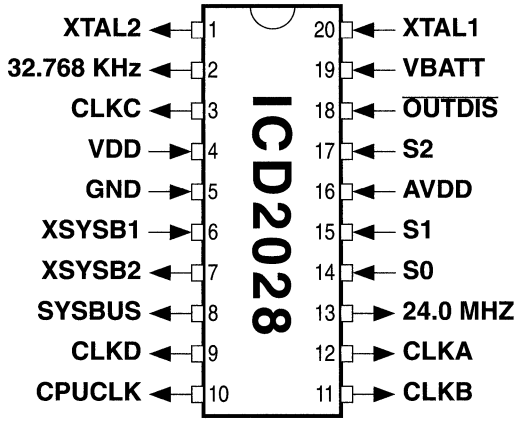
The ICD2028 was specifically designed to support such demanding clock requirements as:

- 486 & Pentium™ microprocessors both with and without clock doublers
- New single-chip system logic chip sets
- Ethernet Local Area Network controllers
- Super I/O Combo chips
- New High-Density floppy disk drive controllers

The ICD2028 consists of 2 crystal-controlled oscillators, 3 phase-locked loops, and 8 different outputs in a single package. To sum up, the greatest asset of the ICD2028 lies in its ability to serve as the single source of all clocking requirements in modern desktop workstations.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions




## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | XTAL2 | Oscillator output to a 32.768 KHz parallel-resonant crystal |
| 2 | 32.768 KHz | 32.768 KHz output |
| 3 | CLKC | User-configurable clock output<br>(See *User-Selectable Clock Options* on page 62 for values.) |
| 4 | VDD | +5V to I/O Ring |
| 5 | GND | Ground |
| 6 | XSYSB1 | Reference oscillator input for all phase-locked loops (nominally 14.31818 MHz). A PC System Bus Clock Signal may be used as input if available. |
| 7 | XSYSB2 | Oscillator Output to a reference crystal. For higher accuracy, a parallel-resonant crystal should be used. Assume CLOAD ≈ 17pF. For more information on crystal requirements, please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |

## Table 1: Signal Descriptions (Continued)

| Pin # | Signal | Function |
|---|---|---|
| 8 | SYSBUS | Buffered 14.31818 MHz crystal output |
| 9 | CLKD | User-configurable clock output<br>(See *User-Selectable Clock Options* on page 62 for values.) |
| 10 | CPUCLK | CPUCLK Programmable Oscillator Output<br>(See *CPU Clock Selection* on page 64 for values) |
| 11 | CLKB | User-configurable clock output<br>(See *User-Selectable Clock Options* on page 62 for values.) |
| 12 | CLKA | User-configurable clock output<br>(See *User-Selectable Clock Options* on page 62 for values.) |
| 13 | 24.0 MHz | 24.0 MHz output |
| 14 | S0 | Input Select line 0 for CPUCLK (internal pull-down) |
| 15 | S1 | Input Select line 1 for CPUCLK (internal pull-down) |
| 16 | AVDD | +5V to analog core |
| 17 | S2 | Input Select line 2 for CPUCLK (internal pull-down) |
| 18 | $\overline{\text{OUTDIS}}$ | Output Disable (3-state output enable) when signal is pulled low.<br>(internal pull-up for no-connect if 3-state operation is not needed) |
| 19 | VBATT | +2V to +5V for battery backup operation; powers 32.768 KHz oscillator. |
| 20 | XTAL1 | Oscillator input from a 32.768 KHz crystal. For more information on crystal requirements, please refer to the IC DESIGNS Application note *Crystal Oscillator Topics* on page 292. |

# Detailed Block Diagrams

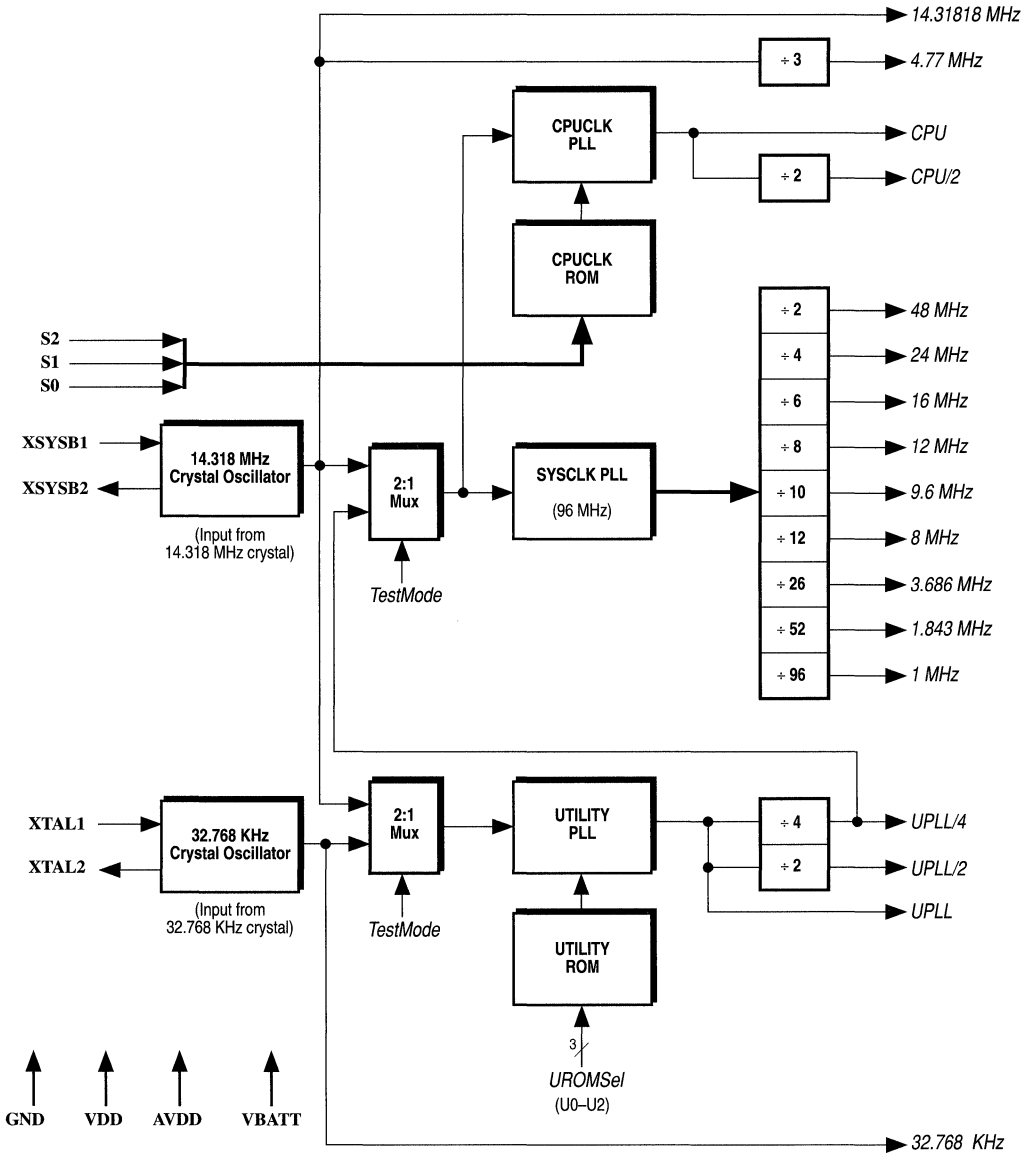



**Fig. 3: Inputs**

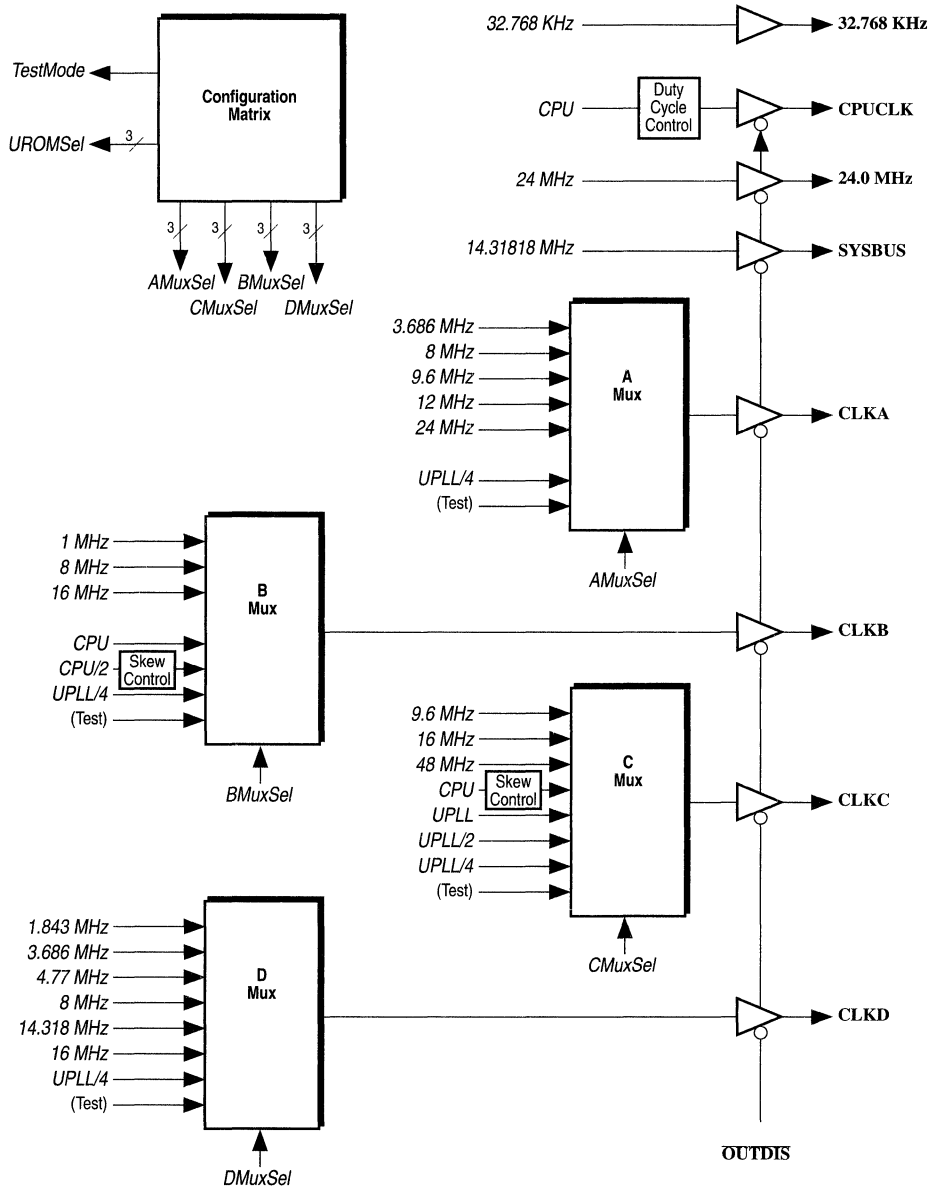



**Fig. 4: Outputs**

# User-Selectable Clock Options

## System & Utility Clock Selection

The heart of the ICD2028 is the rich set of frequencies which are generated internally, encompassing most known system logic motherboard requirements. From this set of outputs, the user may select four output frequencies.

Through a proprietary technique, IC DESIGNS can quickly configure samples of any desired output pin configuration. The configuration process involves no NRE (non-recurring engineering) charges or prototype delays, as is commonly associated with masked ROM changes. Samples of user-configured ICD2028s can generally be made available in 24 hours.

The following two tables list all the available internally generated system clocks on the CLKA, CLKB, CLKC and CLKD outputs, as well as the Utility PLL output.

### Table 2: System Clock Options

| Clock Function | Desired Frequency (MHz) | Actual Frequency (MHz) | PPM Error | Clock Source | Available on Pin(s) | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | CLKA | CLKB | CLKC | CLKD | SYSBUS | 24.0 MHz |
| SYSCLK PLL | 96.000 | 95.870 | 1361 | SYSCLK | | | | | | |
| | 48.000 | 47.935 | 1361 | SYSCLK/2 | | | √ | | | |
| Super Floppy | 32.000 | 31.957 | 1361 | SYSCLK/3 | √ | √ | | | | |
| Floppy Disk | 24.000 | 23.967 | 1361 | SYSCLK/4 | √ | | | | | √ |
| Internal Bus | 16.000 | 15.978 | 1361 | SYSCLK/6 | | √ | √ | √ | | |
| System Bus | 14.318 | 14.318 | 0 | $f_{REF}$ | | | | √ | √ | |
| Keyboard | 12.000 | 11.984 | 1361 | SYSCLK/8 | √ | | | | | |
| | 9.600 | 9.587 | 1361 | SYSCLK/10 | √ | | √ | | | |
| Bus Clock | 8.000 | 7.989 | 1361 | SYSCLK/12 | √ | √ | | √ | | |
| | 4.770 | 4.773 | 572 | $f_{REF}/3$ | | | | √ | | |
| Alt. Comm. Port | 3.686 | 3.687 | 242 | SYSCLK/26 | | √ | | √ | | |
| Serial Port | 1.843 | 1.844 | 242 | SYSCLK/52 | | | | √ | | |
| SCLK | 1.000 | 0.999 | 1361 | SYSCLK/96 | | √ | | | | |

## Table 3: Utility PLL Options

| Clock Function | ROM Source[1] | Desired Frequency (MHz) | Actual Frequency (MHz) | PPM Error | Clock Source[2] | Available on | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | CLKA | CLKB | CLKC | CLKD |
| Alt. Comm. Port | A & B | 18.432 | 18.431 | 62 | Utility PLL/4 | √ | √ | √ | √ |
| " | A & B | 36.864 | 36.862 | 62 | Utility PLL/2 | | | √ | |
| " | A & B | 73.728 | 73.723 | 62 | Utility PLL | | | √ | |
| Custom | A & B | 14.746 | 14.748 | 144 | Utility PLL/4 | √ | √ | √ | √ |
| " | A & B | 29.492 | 29.495 | 144 | Utility PLL/2 | | | √ | |
| " | A & B | 58.984 | 58.991 | 144 | Utility PLL | | | √ | |
| Ethernet | A & B | 20.000 | 20.000 | 0 | Utility PLL/4 | √ | √ | √ | √ |
| " | A & B | 40.000 | 40.000 | 0 | Utility PLL/2 | | | √ | |
| " | A & B | 80.000 | 80.000 | 0 | Utility PLL | | | √ | |
| Custom | A & B | 19.200 | 19.199 | 32 | Utility PLL/4 | √ | √ | √ | √ |
| " | A & B | 38.400 | 38.399 | 32 | Utility PLL/2 | | | √ | |
| " | A & B | 76.800 | 76.798 | 32 | Utility PLL | | | √ | |
| Super I/O–1 | B | 32.000 | 31.997 | 102 | Utility PLL/4 | √ | √ | √ | √ |
| " | B | 64.000 | 63.994 | 102 | Utility PLL/2 | | | √ | |
| " | B | 128.000 | 127.987 | 102 | Utility PLL | | | √ | |
| Super I/O–2 | B | 16.000 | 16.003 | 167 | Utility PLL/4 | √ | √ | √ | √ |
| " | B | 32.000 | 32.005 | 167 | Utility PLL/2 | | | √ | |
| " | B | 64.000 | 64.011 | 167 | Utility PLL | | | √ | |
| Shut VCO off | A & B | — | — | — | — | | | | |
| " | A & B | — | — | — | — | | | | |
| " | A & B | — | — | — | — | | | | |

1. Refers to ROM Options, of which there are currently 2 available: A and B.
2. Each clock function outputs 3 separate frequencies: UPLL, UPLL/2 and UPLL/4

## CPU Clock Selection

The output frequency of the CPU clock oscillator (CPUCLK) is selected by the Clock Selection Inputs S0–S2. This lets the ICD2028 support different microprocessor speed configurations. There are 2 ROM options: the second one supports speed options of some as yet unannounced microprocessors.

The selection lines can be changed at any time to select a new frequency. When this occurs, the internal phase-locked loop immediately seeks the new frequency. During the transition period (about 5 msec), the clock output is multiplexed glitch-free to the reference signal (14.318 MHz) until the PLL settles to the new frequency. The timing for this transition is detailed in *Table 11: AC Characteristics* on page 75.

### Table 4: CPUCLK Output — ROM Option A

| S2 | S1 | S0 | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 20.000 | 20.045 | 2272 |
| 0 | 0 | 1 | 24.000 | 23.967 | 1361 |
| 0 | 1 | 0 | 32.000 | 32.045 | 1422 |
| 0 | 1 | 1 | 40.000 | 40.091 | 2272 |
| 1 | 0 | 0 | 50.000 | 49.992 | 154 |
| 1 | 0 | 1 | 66.600 | 66.596 | 1058 |
| 1 | 1 | 0 | 80.000 | 80.182 | 2272 |
| 1 | 1 | 1 | 100.000 | 99.818 | 1822 |

### Table 5: CPUCLK Output — ROM Option B

| S2 | S1 | S0 | Desired Freq. (MHz) | Actual Freq. (MHz) | PPM Error |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 20.000 | 20.003 | 167 |
| 0 | 0 | 1 | 24.000 | 23.967 | 1359 |
| 0 | 1 | 0 | 60.000 | 59.974 | 429 |
| 0 | 1 | 1 | 40.000 | 40.007 | 167 |
| 1 | 0 | 0 | 50.000 | 50.000 | 0 |
| 1 | 0 | 1 | 66.600 | 66.645 | 331 |
| 1 | 1 | 0 | 80.000 | 80.013 | 167 |
| 1 | 1 | 1 | 100.000 | 99.840 | 1600 |

# Accuracy, Skew, Jitter and Duty Cycle Issues



## Skew-Controlled CPUCLK Signals

Both the CPUCLK and the CPUCLK/2 signals are available as multiple concurrent buffered outputs. Additionally, two of these buffered outputs are available with the outputs closely matched to the original CPUCLK in order to minimize the phase difference between the two outputs. Typical phase coherence is less than 1 ns of skew between the two outputs. The timings of these signal relationships are detailed in *Table 11: AC Characteristics* on page 75.

## Jitter Issues

Jitter, defined at 6σ (sigma), which corresponds to 3 ppm, is ±500 ps (no more than 3 of 1 million full oscillations should exceed the 500 ps spec). Jitter, defined at ±200 ps is .016%, or 160 ppm. The individual VCOs have a design characteristic of ±200 ps, and the above measurements show that, more than 99% of the time, we are able to adhere very tightly to the design goal.

IC DESIGNS believes that the amount of noise that this represents (500 ps) is not usually a problem. Graphics applications tend to be the worst case environment for noise and this specification is within acceptable limits for a very high resolution 185 MHz graphics system. For systems logic applications, jitter on the clock is generally not an issue at all.

## Output Frequency Accuracy

The accuracy of the ICD2028 output frequencies depends on the target output frequency. The output frequencies of the ICD2028 are an integral fraction of the input reference frequency, and are defined by the following equation (P & Q are 7-bit numbers):

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2028 normally produces an output frequency within 0.1% of the target frequencies listed. This is more than sufficient to meet standard motherboard requirements. Specifics regarding accuracy are shown in *Table 2: System Clock Options* on page 62, *Table 3: Utility PLL Options* on page 63, *Table 4: CPUCLK Output — ROM Option A* on page 64 and *Table 4: CPUCLK Output — ROM Option A* on page 64.

## CPUCLK Duty Cycle Configuration

Normally, the duty cycle for the CPUCLK is set to be as close as possible to 50% at the desired frequency. However, because of the plethora of new CPUs — some with clock doublers, some CMOS, some low-voltage — a 50% duty cycle is not always desired. Therefore, the ICD2028 contains a mechanism to adjust the duty cycle according to the user's requirements.

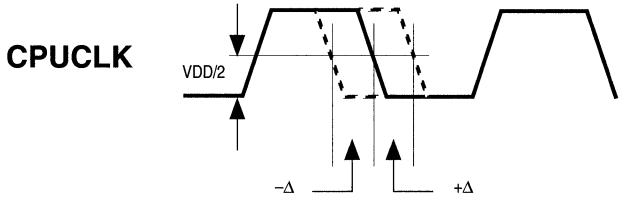



**Fig. 5: CPUCLK Duty Cycle**

The normal CPUCLK duty cycle is guaranteed to be within 50% ±5%, over the frequency range and into a 25pF load. All duty cycle measurements are made at the VDD/2 points of the waveform (CMOS thresholds). As shown in the timing diagram above, a user-defined skew can optionally be specified, which will advance or retard the edge of CPUCLK.

Examples of this use would include conversion from CMOS to TTL thresholds, or support for some of the new CPUs which specify minimum high and low times. All of these can be accommodated. Please note that only the CPUCLK output duty cycle (not CPUCLK/2) can be user-configured.

Please consult IC DESIGNS with your specific CPUCLK duty cycle requirements. For custom duty cycles, we will need to know the desired duty cycle percentage, the load and the desired frequency.

# Power Calculation

Actual current drain is a function of frequency and circuit loading. The operating current of a given output is given by the equation $I = C \cdot V \cdot f$, where $I$=current, $C$=load capacitance in pF (max. 25pF), $V$=output voltage in Volts (usually 5V for rail-to-rail CMOS pads) and $f$=output frequency in MHz.



To calculate total operating current, sum the following:

| | | |
|---|---|---|
| 32.768 KHz | ⇒ | $C_{32} \cdot V \cdot .032 \cdot 10^{-3}$ mA |
| 14.318 MHz | ⇒ | $C_{14} \cdot V \cdot 14.318 \cdot 10^{-3}$ mA |
| 24.0 MHz | ⇒ | $C_{24} \cdot V \cdot 24 \cdot 10^{-3}$ mA |
| CPUCLK | ⇒ | $C_{CPUCLK} \cdot V \cdot f_{CPUCLK} \cdot 10^{-3}$ mA |
| CLKA | ⇒ | $C_{CLKA} \cdot V \cdot f_{CLKA} \cdot 10^{-3}$ mA |
| CLKB | ⇒ | $C_{CLKB} \cdot V \cdot f_{CLKB} \cdot 10^{-3}$ mA |
| CLKC | ⇒ | $C_{CLKC} \cdot V \cdot f_{CLKC} \cdot 10^{-3}$ mA |
| CLKD | ⇒ | $C_{CLKD} \cdot V \cdot f_{CLKD} \cdot 10^{-3}$ mA |
| Internal | ⇒ | 17 mA |

This yields an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on the package type.

Some typical values:

**Table 6: Operating Current Typical Values**

| Frequency | Capacitive Load | Current (in mA) | |
|---|---|---|---|
| | | $V_{DD}$ = 5V | $V_{DD}$ = 3.3V |
| low | low | 20 | 13 |
| high | low | 35 | 23 |
| high | high | 65 | 43 |

# General Considerations

## VBATT

The VBATT input powers the Real-Time Clock Oscillator (RTC). The backup power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable.

## Crystal & External Reference Operation

The following diagrams detail the proper way to hook up reference crystals or metal cans. Please see the IC DESIGNS Application Notes titled *Crystal Oscillator Topics* on page 292 and *Externally Driven Crystal Oscillator* on page 295 for specifics regarding recommended crystals.

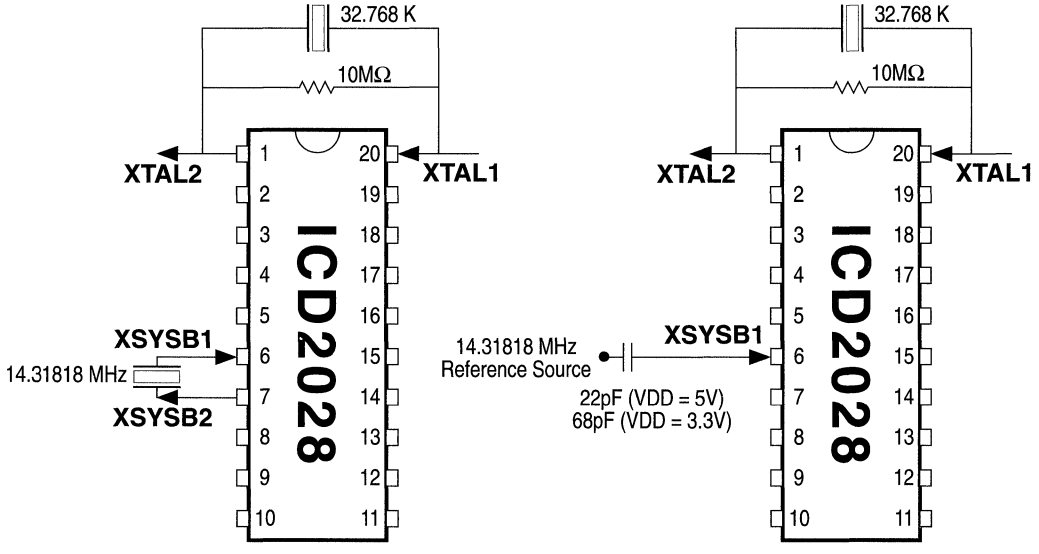



**Fig. 6: Crystal & External Reference Schematics**

NOTE: For highest accuracy, IC DESIGNS recommends the following crystals or their equivalents. These crystals are available from Fox Electronics.

Recommended 14.31818 MHz reference crystals:

- FPX 14.31818 30 / 50 / 0–70 / 16
- FD 14.31818 30 / 50 / 0–70 / 16

## 3.3V Considerations

The desired operating voltage for the ICD2028 (5V or 3.3V) must be specified when ordering . When operating at 3.3V, care must be taken not to connect 5V to any of the input pins, as latch-up may occur.

## 3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state all the clock output lines (except 32.768 KHz). This supports wired-or connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required.

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in *Fig. 7: Phase-Locked Loop Oscillator* on page 69. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up-and-down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

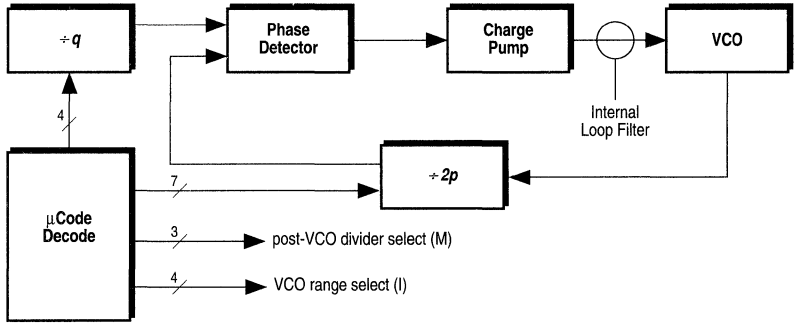



**Fig. 7: Phase-Locked Loop Oscillator**

## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin AVDD should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Please see the IC DESIGNS Application Notes *Power Feed and Board Layout Issues* on page 281 and *Minimizing Radio Frequency Emissions* on page 285 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2028 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2028 closest to the device requiring the highest frequency.

## FCC & Noise Issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note *Minimizing Radio Frequency Emissions* on page 285.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2028 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2028, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

# Ordering Information & Configuration Procedure

## Ordering Information



### Table 7: Order Codes

| Part Number | Package Type | Operating Range | Configuration Code |
|---|---|---|---|
| ICD2028 | S = 20-Pin SOIC DIP | C = 0°C to +70°C @ VDD = 5V | Standard Configurations –2, –4, –5 |
| | | | or |
| | | L = 0°C to +70°C @ VDD = 3.3V | IC DESIGNS assigned Custom Configuration Code |

Example: order ICD2028SC–2 for the ICD2028, 20-pin plastic SOIC, 5V operating range device which uses the standard configuration code –2 (486 compatibility with CPUCLK/2 support). See *Standard Configurations* on page 72 for details on the standard configurations.

Custom configurations are also available. To order a custom configuration, first copy and fill out the *ICD2028 Custom Configuration Order Form* on page 73, then fax it to IC DESIGNS (our fax number is 206/820–8959). We will then assign a unique ICD Configuration Code and fax it back to you, which can then be used to place the initial and future orders for that configuration.

Standard packaging is in a surface-mount configuration. The ICD2028 is also available in a through-hole DIP configuration by special order. Please consult IC DESIGNS for current availability and lead times.

## Standard Configurations

While the ICD2028 can easily be configured to the user's unique requirements, there are a few standard configurations available. These are defined as follows:

### Table 8: Standard Configurations

| Signal Name | Pin # | –2 | –4 | –5 |
|---|---|---|---|---|
| Reference Crystal | — | 14.318 MHz | 14.318 MHz | 14.318 MHz |
| Utility PLL | — | (Off) | (Off) | 32.000 MHz |
| CPUCLK Duty Cycle | — | 50% | 50% | 50% |
| ROM Option | — | A | B | B |
| CPUCLK | 10 | √ | √ | √ |
| SYSBUS | 8 | √ | √ | √ |
| 24.0 MHz | 13 | √ | √ | √ |
| CLKA | 12 | 12.000 MHz | 12.000 MHz | 12.000 MHz |
| CLKB | 11 | CPUCLK/2 | CPUCLK/2 | CPUCLK/2 |
| CLKC | 3 | 16.000 MHz | 16.000 MHz | 32.000 MHz (UPLL/4) |
| CLKD | 9 | 1.843 MHz | 1.843 MHz | 1.843 MHz |
| 32.768 KHz | 2 | √ | √ | √ |

–2 Compatible with most 486 chip sets, while adding skew-free CPUCLK/2 support.

–4 Supports Pentium™ requirements.

–5 Provides 486 support and Super I/O (32 MHz) support.

IC DESIGNS 12020 113th Ave. N.E. Kirkland, WA 98034–6920 TEL: 206/821–9202 FAX: 206/820–8959

# ICD2028 Custom Configuration Order Form

**Company Name** _____ **Contact** _____

**Telephone** _____ **Fax** _____

## Output Signals

***(All frequencies in MHz unless otherwise noted)***

(Circle one in each line, or fill in the blanks.)

**Operating Voltage (VDD & AVDD): 5V 3.3V**

**Dedicated Pins: 32.768 KHz 24.000**

**Reference Xtal & SYSBUS Output: 14.31818**

**CPUCLK** (Select desired ROM Option line below.)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **ROM Opt. A** | **[20.0** | **24.0** | **32.0** | **40.0** | **50.0** | **66.6** | **80.0** | **100.0]** |
| **ROM Opt. B** | **[20.0** | **24.0** | **60.0** | **40.0** | **50.0** | **66.6** | **80.0** | **100.0]** |

**CPUCLK: Duty Cycle** _____ % **Load** _____ pF **Frequency** _____ MHz
(default) (50%) (25pF) (10–100 MHz)

| **Utility PLL/4** | **18.432** | **14.746** | **20.000** | **19.200** | **32.000**[1] | **16.000**[1] | **OFF** |
|---|---|---|---|---|---|---|---|
| **CLKA** | **3.692** | **8.000** | **9.600** | **12.000** | **24.000** | **—** | **UPLL/4** |
| **CLKB** | **1.000** | **8.000** | **16.000** | **—** | **CPU**[2] | **CPU/2**[2] | **UPLL/4** |
| **CLKC** | **9.600** | **16.000** | **48.000** | **CPU**[2] | **UPLL** | **UPLL/2** | **UPLL/4** |
| **CLKD** | **1.843** | **3.686** | **4.770** | **8.000** | **14.318** | **16.000** | **UPLL/4** |

**IC DESIGNS Assigned Configuration Code** _____
(For IC DESIGNS use only)

DS V1.4 — 10/14/93

1. Only available with ROM Option B.
2. Skew-controlled to CPUCLK output.

# Device Specifications

## Electrical Data

### Table 9: Absolute Maximum Ratings

| Name | Description | Min | Max 5V (3.3V) | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | VDD + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 425 (150) | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5% (+3.3V ±10%); 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 10: DC Characteristics

| Name | Description | Min 5V (3.3V) | Max 5V (3.3V) | Units | Conditions |
|---|---|---|---|---|---|
| $V_{BATT}$ | Backup battery voltage | 2.0 (2.0) | 5.25 (3.6) | Volts | typ. = 3.0 Volts |
| $V_{IH}$ | High-level input | 2.0 | $V_{DD}$ + 0.3 | Volts | Except crystal pads |
| $V_{IL}$ | Low-level input | –0.3 | 0.8 (0.6) | Volts | Except crystal pads |
| $V_{OH}$ | High-level CMOS output | $V_{DD}$ – 0.5 | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $V_{OH-32}$ | 32.768 KHz high-level output | $V_{BATT}$ – 0.5 | | Volts | $I_{OH}$ = –0.5 mA |
| $V_{OL-32}$ | 32.768 KHz low-level output | | 0.4 | Volts | $I_{OL}$ = 0.5 mA |
| $I_{IH}$ | Input high current | | 150 | µA | $V_{IH}$ = $V_{DD}$ – 0.5V |
| $I_{IL}$ | Input low current | | –250 | µA | $V_{IH}$ = +0.5V Volts |
| $I_{OZ}$ | Output leakage current | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | 20 (13) | 85 (45) | mA | typ. = 35 (23)[1] |
| $I_{BATT}$ | Backup battery current | | 15 | µA | typ. = 5 µA |

1. CPUCLK = 66 MHz

## Table 11: AC Characteristics

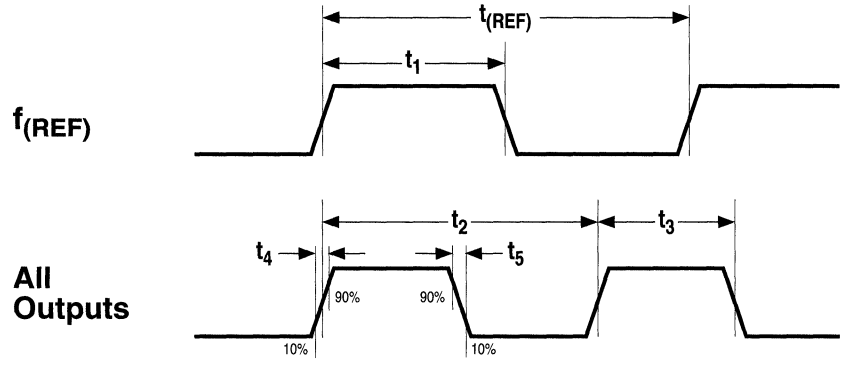
| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value | | 14.318 | | MHz |
| $t_{(REF)}$ | reference clock period | $1 \div f_{(REF)}$ | | 69.8 | | ns |
| $t_1$ | input duty cycle | Duty cycle for input oscillator, defined as $t_1 \div t_{(REF)}$ | 25% | 50% | 75% | |
| $t_2$ | output period | PLL oscillator ranges 5V<br>(see tables under *User-Selectable Clock Options* on page 62 for details)<br>3.3V | 8.3<br>120 MHz<br>12.5<br>80 MHz | | 2857<br>350 KHz<br>2857<br>350 KHz | ns |
| $t_3$ | output duty cycle[1] | Duty cycle for output pads, defined as $t_3 \div t_2$ as measured @ CMOS $V_{TH}$ of $V_{DD} \div 2$ | 40% | | 60% | |
| $t_4$ | rise time | Output oscillator rise time (25pF load) | | | 3 | ns |
| $t_5$ | fall time | Output oscillator fall time (25pF load) | | | 3 | ns |
| $t_6$ | 3-state | Time for output oscillators to enter 3-state mode after $\overline{\text{OUTDIS}}$ goes low | | | 12 | ns |
| $t_7$ | clk valid | Time for output oscillators to exit 3-state mode after $\overline{\text{OUTDIS}}$ goes high | | | 12 | ns |
| $t_8$ | buffered CPUCLK skew | Skew delay between CPUCLK and buffered CPUCLK outputs, as measured @ CMOS $V_{TH}$ of $V_{DD} \div 2$ | CLKC<br>CLKB | < .25<br>< .25 | 1<br>1 | ns<br>ns |
| $t_9$ | CPUCLK/2 skew | Skew delay between CPUCLK and CPUCLK/2 outputs, as measured @ CMOS $V_{TH}$ of $V_{DD} \div 2$ | | < .25 | 1 | ns |
| $t_{freq1}$ | freq1 output period | Original frequency output | | | | |
| $t_{freq2}$ | freq2 output period | New frequency output | | | | |
| $t_A$ | $f_{(REF)}$ mux time | Time clock output remains high or low while output muxes to reference frequency | $\frac{t_{(REF)}}{2}$ | | $3\frac{t_{(REF)}}{2}$ | ns |
| $t_B$ | $t_{freq2}$ mux time | Time clock output remains high or low while output muxes to new frequency value | $\frac{t_{freq2}}{2}$ | | $3\frac{t_{freq2}}{2}$ | ns |
| $t_{MUXREF}$ | | Time for VCO to settle between changes | | 6.6 | | msec |

1. Custom CPUCLK duty cycle may be special ordered.

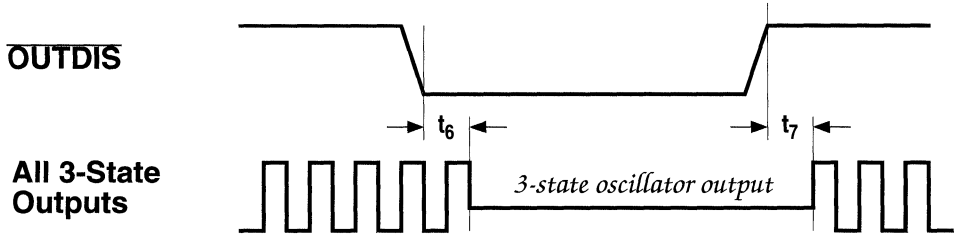
**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

## Timing Diagrams

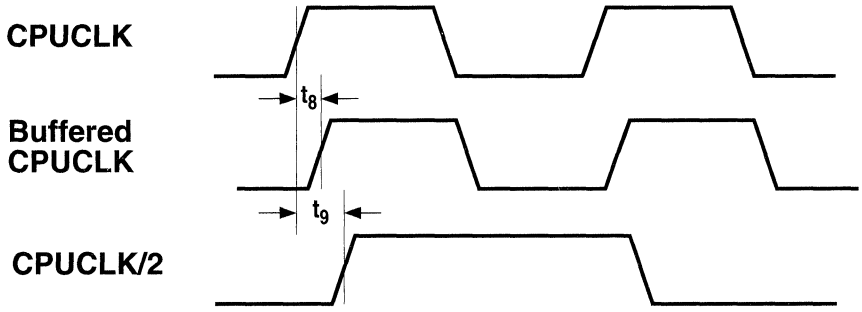
### Fig. 8: Rise and Fall Times



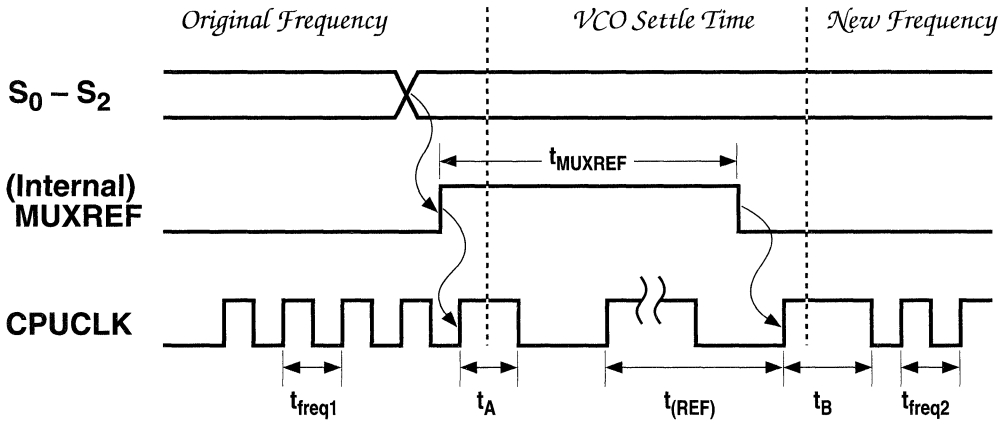

### Fig. 9: 3-State Timing



## Fig. 10: CPUCLK Skew




## Fig. 11: Selection Timing



# Revision History / Credits

V1.2 (3/4/93) — Preliminary release
V1.4 (11/15/93) — Final Release Version

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# ICD2093

## "Super-Buffer" Clock Generator

**Single-Chip Oscillator for Use with Pentium™ Processor Based & Other High-Performance Systems**



- **Selectable CPU Clock Provides 8 2X or 1X outputs which Handle all Pentium™ Processor Clocking Requirements**
- **Less than 250 ps Total Skew Between Hi-Drive (48 mA), Hi-Load (50pF) CPU Clock Outputs**
- **4 Fixed Outputs: 14.31818 MHz (2), 16 MHz and either 24 or 32 MHz Handle all other System Clocking Requirements**
- **CPU Clock Frequency Range: 10 MHz – 100 MHz with 50% Duty Cycle**
- **Optional Power-Down Mode Supports "Green" Spec**
- **3-State Oscillator Control Disables Outputs for Test Purposes**
- **Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal**
- **Sophisticated Internal Loop-Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters**
- **5V Operation**
- **Low-Power, High-Speed CMOS Technology**
- **Available in 24-Pin SOIC Package Configuration**

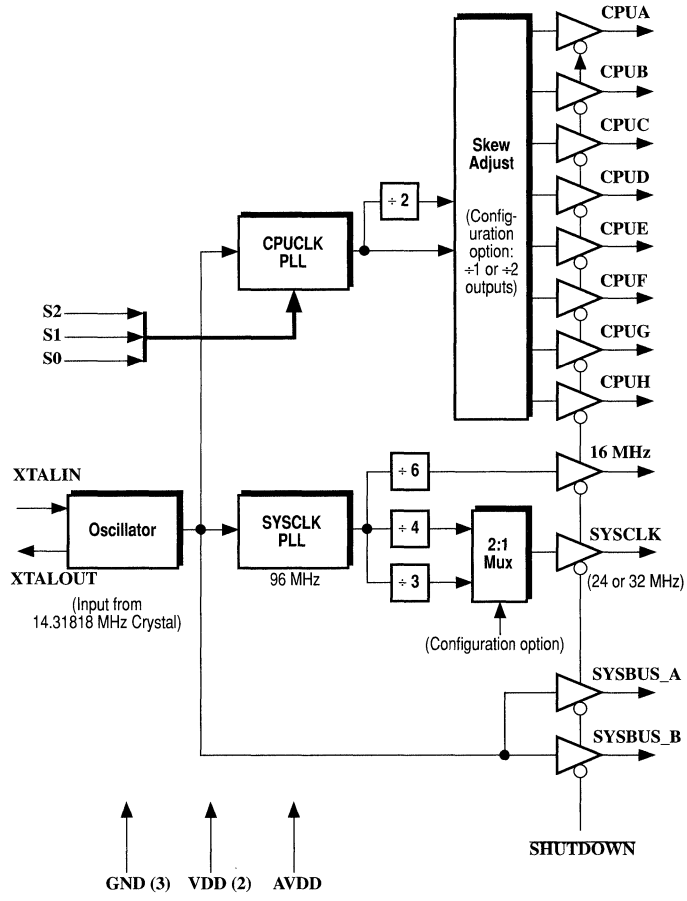


**Fig. 1: ICD2093 Block Diagram**

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# Contents



# Figures



# Tables

# Introduction



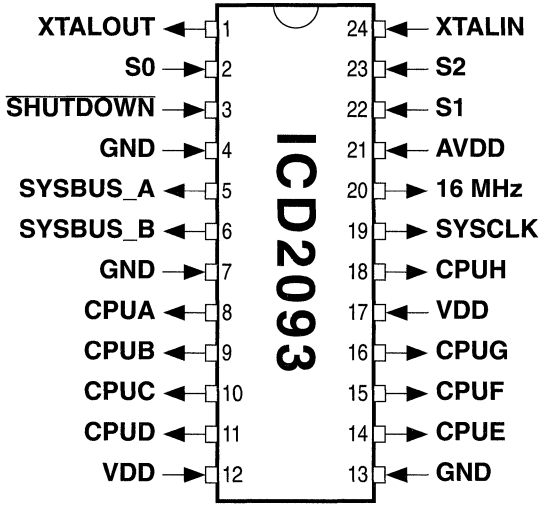
Today's high-end personal computers require a CPU system clock which exhibits a large drive capability (high fanout) without degradation in rise & fall times. The classical solution has been to distribute and buffer this clock. The ICD2093 handles this problem by providing 8 1X or 2X CPU Clock outputs with extremely low skew between outputs.

The ICD2093 also supplies the other clocks required in a high-performance system: the system I/O clocks and the system bus clocks.

The ICD2093 consists of 1 crystal controlled oscillator, 2 phase-locked loops, and 12 different outputs in a single package.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions




## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | XTALOUT | Oscillator Output to a 14.31818 MHz Parallel-Resonant Crystal |
| 2 | S0 | CPU Clock ROM Select Line — Bit 0 (LSB) |
| 3 | $\overline{\text{SHUTDOWN}}$ ($\overline{\text{OUTDIS}}$) | When pulled low, shuts down oscillator, PLL and all dynamic logic. Can be made Output Disable (3-State Output Enable) via configuration option. Internal pull-up for no-connect if shutdown operation is not needed. |
| 4 | GND | Ground |
| 5 | SYSBUS_A | 14.31818 MHz Output |
| 6 | SYSBUS_B | 14.31818 MHz Output |
| 7 | GND | Ground |

## Table 1: Signal Descriptions (Continued)

| Pin # | Signal | Function |
|---|---|---|
| 8 | CPUA | CPU Clock Output A (1X or 2X)[a] |
| 9 | CPUB | CPU Clock Output B (1X or 2X)[a] |
| 10 | CPUC | CPU Clock Output C (1X or 2X)[a] |
| 11 | CPUD | CPU Clock Output D (1X or 2X)[a] |
| 12 | VDD | +5V to I/O Ring |
| 13 | GND | Ground |
| 14 | CPUE | CPU Clock Output E (1X or 2X)[a] |
| 15 | CPUF | CPU Clock Output F (1X or 2X)[a] |
| 16 | CPUG | CPU Clock Output G (1X or 2X)[a] |
| 17 | VDD | +5V to I/O Ring |
| 18 | CPUH | CPU Clock Output H (1X or 2X)[a] |
| 19 | SYSCLK | 24 MHz or 32 MHz Output |
| 20 | 16 MHz | 16 MHz Output |
| 21 | AVDD | +5V to Analog Core |
| 22 | S1 | CPU Clock ROM Select Line — Bit 1 |
| 23 | S2 | CPU Clock ROM Select Line — Bit 2 (MSB) |
| 24 | XTALIN | Oscillator input from a 14.31818 MHz crystal. For more information on crystal requirements, please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. |

a. All the CPU outputs can be 1X, or 2X, or any mix of the two (the outputs of each type are contiguous).

# Clock Operation

## CPUCLK Oscillator

The output frequency of the CPU clock oscillator (CPUCLK) is selected by the Clock Selection Inputs S0–S2. This lets the ICD2093 support different microprocessor speed configurations. There are 2 ROM options.

The selection lines can be changed at any time to select a new frequency. When this occurs, the internal phase-locked loop immediately and monotonically seeks the new frequency in the 33.333 MHz – 80 MHz range.

### Table 2: CPUCLK ROM Selection Outputs

| S2 | S1 | S0 | Desired Frequency (MHz) | Actual CPUCLK (MHz) | Actual CPU/2 (MHz) | VCO Frequency (MHz) | PPM Error |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 20.000 | 20.003 | 10.002 | 80.013 | 167 |
| 0 | 0 | 1 | 33.333 | 33.322 | 16.661 | 66.645 | 331 |
| 0 | 1 | 0 | 60.000 | 60.000 | 30.000 | 120.000 | 0 |
| 0 | 1 | 1 | 40.000 | 40.006 | 20.003 | 80.013 | 167 |
| 1 | 0 | 0 | 50.000 | 50.114 | 25.057 | 100.227 | 2267 |
| 1 | 0 | 1 | 66.667 | 66.818 | 33.409 | 133.636 | 2270 |
| 1 | 1 | 0 | 80.000 | 80.013 | 40.006 | 160.026 | 167 |
| 1 | 1 | 1 | 100.000 | 100.227 | 50.114 | 100.227 | 2267 |

## Fixed Frequency Oscillator Operation

The following table lists the available fixed frequency outputs:

### Table 3: SYSCLK Outputs

| Desired Frequency (MHz) | Actual Frequency (MHz) | | PPM Error | |
|---|---|---|---|---|
| | Option -1 | Option -2 | Option -1 | Option -2 |
| 24.000 | 23.993 | 23.967 | 1359 | 307 |
| 32.000 | 31.990 | 31.957 | 1359 | 307 |

# Design Considerations

## Skew Issues



The ICD2093 offers eight CPUCLK ÷1 or ÷ 2 outputs, CPUA–CPUH. These outputs have been optimized to minimize skew between any two CPUA–CPUH outputs.

The standard drive on all CPU outputs is 48 mA, with a 3 ns rise and fall time when driving 50pF.

To minimize skew, output loads should be balanced and the printed circuit board trace lengths should be equal. The high-performance output driver of the ICD2093 requires the engineer to observe proper transmission line techniques, including termination, when designing for the ICD2093. (See *Termination* on page 86 for suggestions on proper termination.)

The following table estimates the incremental skew (in addition to worst-case specification) caused by unbalanced loading. The table includes data for driving both TTL loads and CMOS threshold loads. There are 2 normalized measurements given: all loads normalized to 0pF, and all loads at 30pF (the latter being a more realistic operating assumption).

**Table 4: Estimated Skew vs. Load**

| Load | Threshold Volts | Rising Edge ( ns ) | | Falling Edge ( ns ) | |
|---|---|---|---|---|---|
| | | Normalized at 0pF | Normalized at 30pF | Normalized at 0pF | Normalized at 30pF |
| 50pF | 2.5 | 1.10 | 0.38 | 1.03 | 0.33 |
| | 1.4 | 0.72 | 0.22 | 1.31 | 0.44 |
| 40pF | 2.5 | 0.92 | 0.20 | 0.88 | 0.18 |
| | 1.4 | 0.62 | 0.12 | 1.09 | 0.22 |
| 30pF | 2.5 | 0.72 | 0.00 | 0.70 | 0.00 |
| | 1.4 | 0.50 | 0.00 | 0.87 | 0.00 |
| 20pF | 2.5 | 0.52 | -0.20 | 0.50 | -0.20 |
| | 1.4 | 0.35 | -0.15 | 0.62 | -0.25 |
| 10pF | 2.5 | 0.30 | -0.42 | 0.28 | -0.42 |
| | 1.4 | 0.20 | -0.30 | 0.32 | -0.55 |
| 0pF | 2.5 | 0.00 | -0.72 | 0.00 | -0.70 |
| | 1.4 | 0.00 | -0.50 | 0.00 | -0.87 |

# Termination

The ICD2093 provides fast rise and fall times on its outputs to drive large loads. These fast rise and fall times require the PCB designer to observe proper transmission line techniques. Proper termination is *especially* important.

There are three principal techniques for proper termination. The optimum choice depends on individual requirements.

### Series Termination

The main drawback of this technique is that $C_L$ adversely affects rise & fall times.

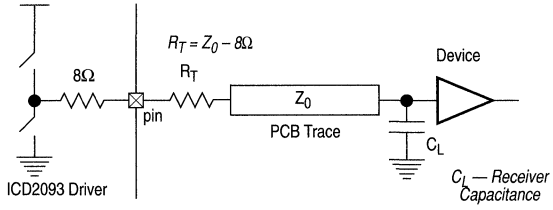



**Fig. 3: Series Termination**

### Parallel Termination

The main drawback of this technique is that it consumes power.

VT = VDD ÷ 2 for minimum power. (NOTE: VT should not equal receiver threshold. TTL systems often set VT at 3V using Thevenin equivalent circuit.) See example divider in diagram below.

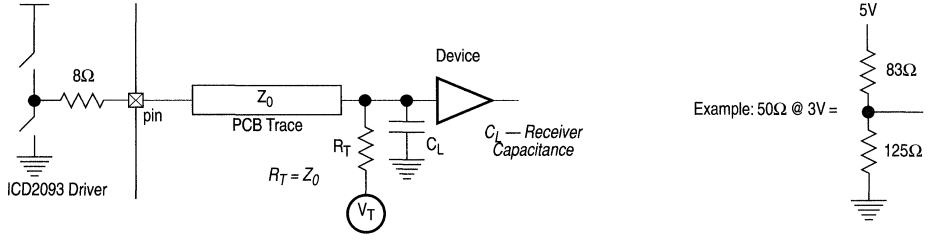



**Fig. 4: Parallel Termination**

### AC Termination

The main drawback of this technique is that it is not as good at high frequencies.

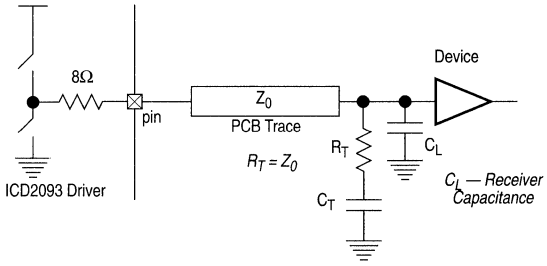



**Fig. 5: AC Termination**

### Jitter

To reduce jitter induced by $V_{DD}$ and GND noise, minimize output loads. Also, provide low impedance power and ground connections with adequate bypass. Analog $V_{DD}$ (AVDD) requires a high-quality, low noise power supply.

# Power Calculation

Actual current drain is a function of frequency and circuit loading. The operating current of a given output is given by the equation $I = C \cdot V \cdot f$, where $I$=current, $C$=load capacitance in Farads (max. 50pF), $V$=output voltage in Volts (usually 5V for rail-to-rail CMOS pads) and $f$=output frequency in Hertz.

To calculate total operating current, sum the following:

| | | |
|---|---|---|
| ***SYSBUS_A*** | ⇒ | $C_{14} \cdot V \cdot 14.318$ |
| ***SYSBUS_B*** | ⇒ | $C_{24} \cdot V \cdot 14.318$ |
| ***CPUA*** | ⇒ | $C_{CLKA} \cdot V \cdot f_{CLKA}$ |
| ***CPUB*** | ⇒ | $C_{CLKB} \cdot V \cdot f_{CLKB}$ |
| ***CPUC*** | ⇒ | $C_{CLKC} \cdot V \cdot f_{CLKC}$ |
| ***CPUD*** | ⇒ | $C_{CLKD} \cdot V \cdot f_{CLKD}$ |
| ***CPUE*** | ⇒ | $C_{CLKE} \cdot V \cdot f_{CLKE}$ |
| ***CPUF*** | ⇒ | $C_{CLKF} \cdot V \cdot f_{CLKF}$ |
| ***CPUG*** | ⇒ | $C_{CLKG} \cdot V \cdot f_{CLKG}$ |
| ***CPUH*** | ⇒ | $C_{CLKH} \cdot V \cdot f_{CLKH}$ |
| ***Internal*** | ⇒ | .06 A (60 mA) |

This yields an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on the package type.

Some typical values:

## Table 5: Operating Current Typical Values

| Frequency | Capacitive Load | Current ( mA ) |
|---|---|---|
| 66.6 MHz | 30pF | 115 mA |

# General Considerations

## Crystal & External Reference Operation



The following diagrams detail the proper way to hook up reference crystals or metal cans. Please see the IC DESIGNS Application Notes titled *Crystal Oscillator Topics* on page 292 and *Externally Driven Crystal Oscillator* on page 295 for specifics regarding recommended crystals.

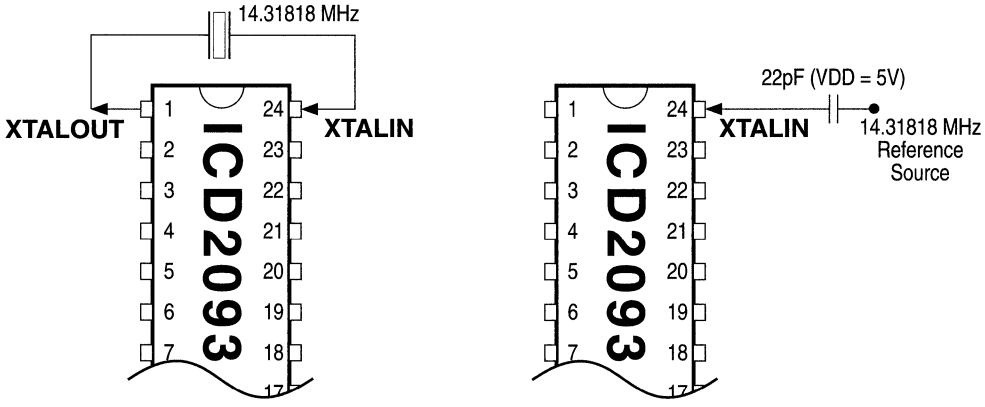



**Fig. 6: Crystal & External Reference Schematics**

NOTE: For highest accuracy, IC DESIGNS recommends the following crystals or their equivalents. These crystals are available from Fox Electronics.

Recommended 14.31818 MHz reference crystals:

- FPX 14.31818 30 / 50 / 0–70 / 16
- FD 14.31818 30 / 50 / 0–70 / 16

## Power-Down Operation

In the power-down state, the oscillator, PLL and all dynamic logic is shut down.

Note: during shutdown, the internal PLLs are turned off. Upon restarting, there will be a 5 msec interval during which the VCOs stabilize. See *Fig. 13: Power-Down Timing* on page 97 for further timing information.

## 3-State Output Operation (Optional)

If the $\overline{\text{OUTDIS}}$ configuration option is chosen, then the $\overline{\text{SHUTDOWN}}$ pin becomes an $\overline{\text{OUTDIS}}$ pin, which, when pulled low, will 3-state all the clock output lines. This supports wired-or connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required. The output pads contain weak pull-down resistors.

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in *Fig. 7: Phase-Locked Loop Oscillator* on page 90. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up-and-down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

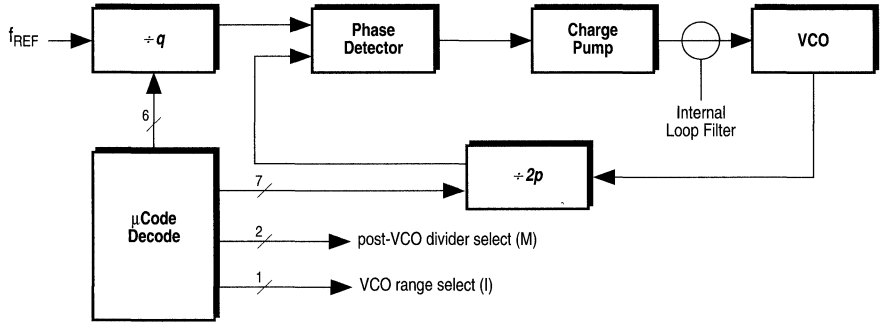



**Fig. 7: Phase-Locked Loop Oscillator**

## PC Board Routing Issues

A full low-impedance power and ground plane layout is required both under and around the IC package. AVDD requires a clean filtered supply; VDD must be low impedance with adequate bypass. The analog power pin AVDD should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply

lines. Please see the IC DESIGNS Application Notes *Power Feed and Board Layout Issues* on page 281 and *Minimizing Radio Frequency Emissions* on page 285 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2093 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.



When designing with this device, it is best to locate the ICD2093 closest to the device requiring the highest frequency.

## FCC & Noise Issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note *Minimizing Radio Frequency Emissions* on page 285.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate ground buses for the core and output circuitry are used.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2093 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2093, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

# Ordering Information

## Table 6: ICD2093 Configuration Options

| Signal / Pin | Option -1 | Option -2 |
|---|---|---|
| CPUA | ÷2 | ÷2 |
| CPUB | ÷2 | ÷2 |
| CPUC | ÷2 | ÷1 |
| CPUD | ÷2 | ÷1 |
| CPUE | ÷2 | ÷1 |
| CPUF | ÷2 | ÷1 |
| CPUG | ÷2 | ÷1 |
| CPUH | ÷1 | ÷1 |
| Pin 3 | $\overline{\text{OUTDIS}}$ | $\overline{\text{SHUTDOWN}}$ |
| SYSCLK | 24 MHz | 24 MHz |

## Table 7: Order Information

| Part Number | Package Type | Temperature Range | Clock Output Options |
|---|---|---|---|
| **ICD2093** | S = 24-Pin SOIC | C = Commercial[a] | Standard Configuration -1 |

a. 0°C to +70°C

Example: order ICD2093SC-1 for the ICD2093, 24-pin plastic SOIC, commercial temperature range device which uses the standard configuration code -1 (SYSCLK = 24 MHz, Power-Down not enabled, one ÷1 CPU clock and seven ÷2 CPU clocks).

Custom configurations are also available. To order a custom configuration, call IC DESIGNS.

# Device Specifications

## Electrical Data

### Table 8: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | VDD + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +140 | °C |
| $P_{DISS}$ | Power dissipation | | 1000 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 9: DC Characteristics

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input | 2.0 | $V_{DD}$ + 0.3 | Volts | Except crystal pads |
| $V_{IL}$ | Low-level input | –0.3 | 0.8 | Volts | Except crystal pads |
| $V_{OH}$ | High-level CMOS output | $V_{DD}$ – 0.5 | | Volts | $I_{OH}$ = –48 mA[a] |
| $V_{OL}$ | Low-level output | | 0.5 | Volts | $I_{OL}$ = 48 mA[a] |
| $I_{IH}$ | Input high current | | 150 | µA | $V_{IH}$ = $V_{DD}$ – 0.5V |
| $I_{IL}$ | Input low current | | –250 | µA | $V_{IL}$ = +0.5V Volts |
| $I_{OZ}$ | Output leakage current | –10 | 150 | µA | (3-state) |
| $I_{DDA}$ | Supply current to core | | 18 | mA | 1CPU @ 66 MHz<br>7CPU @ 33 MHz |
| $I_{DD}$ | Power supply current | | 130 | mA | |
| $C_L$ | Total cap. load / CPU output | | 50[a, b] | pF | |

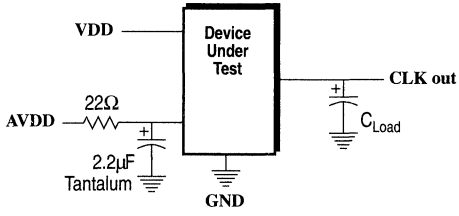
a. Option -2 has half the output drive capability: $I_{OH}$ = -24 mA, $I_{OL}$ = 24 mA, $C_L$ = 25pF
b. Maximum load on all CPU outputs can exceed the maximum specifications.
**NOTE:** Input SHUTDOWN is pulled up to $V_{DD}$ via an internal resistance.

## Table 10: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value | | 14.318 | | MHz |
| $t_{(REF)}$ | reference clock period | $1 \div f_{(REF)}$ | | 69.84 | | ns |
| $t_1$ | input duty cycle | Duty cycle for input oscillator, defined as $t_1 \div t_{(REF)}$ | 25% | 50% | 75% | |
| $t_2$ | output period | | 10<br>100 MHz | | 100<br>10 MHz | ns |
| $t_3$ | output duty cycle | Duty cycle for output pads, defined as $t_3 \div t_2$ as measured @ CMOS $V_{TH}$ of $V_{DD} \div 2$ (Special screening required for 100 MHz) | 40% | | 60% | |
| $t_4$ | rise time | Output oscillator (50pF load @ 10 MHz) | | | 3.5 | ns |
| $t_5$ | fall time | Output oscillator (50pF load @ 10 MHz) | | | 3 | ns |
| $t_6$ | skew | Leading edge skew from CPUx to CPUy if ÷1 & ÷2 and $C_L$ = 50pF | | | 500 | ps |
| $t_8$ | skew | Leading edge skew from CPUx to CPUy if ÷1 & ÷1 or ÷2 & ÷2 and $C_L$ = 50pF | | | 250 | ps |
| $t_{VCO}$ | VCO settle time | Time for VCO to transition smoothly and monotonically from the original to the new frequency | | | 5 | msec |
| $t_{10}$ | 3-state | Time for output oscillators to enter 3-state mode after $\overline{OUTDIS}$ goes low | | | 20 | ns |
| $t_{11}$ | clk valid | Time for output oscillators to exit 3-state mode after $\overline{OUTDIS}$ goes high | | | 20 | ns |
| $t_{12}$ | SYSBUS skew | Leading edge skew | | | 500 | ps |
| $t_{13}$ | SYSBUS skew | Trailing edge skew | | | 500 | ps |
| $t_{14}$ | power-down | Time to invoke power-down option | | | 20 | ns |
| $t_{15}$ | power-up | Time to revoke power-down option | | | 20 | ns |

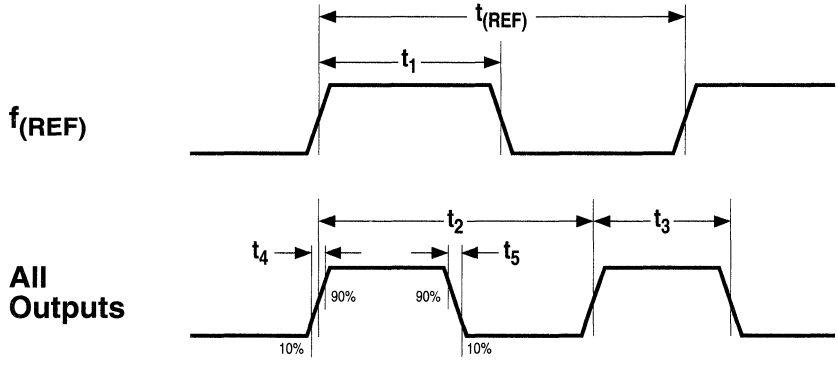
**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

## Test Circuit

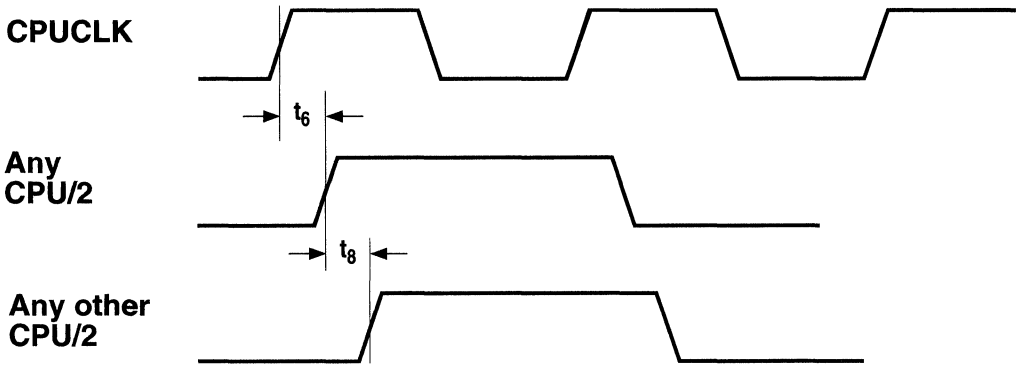



## Timing Diagrams

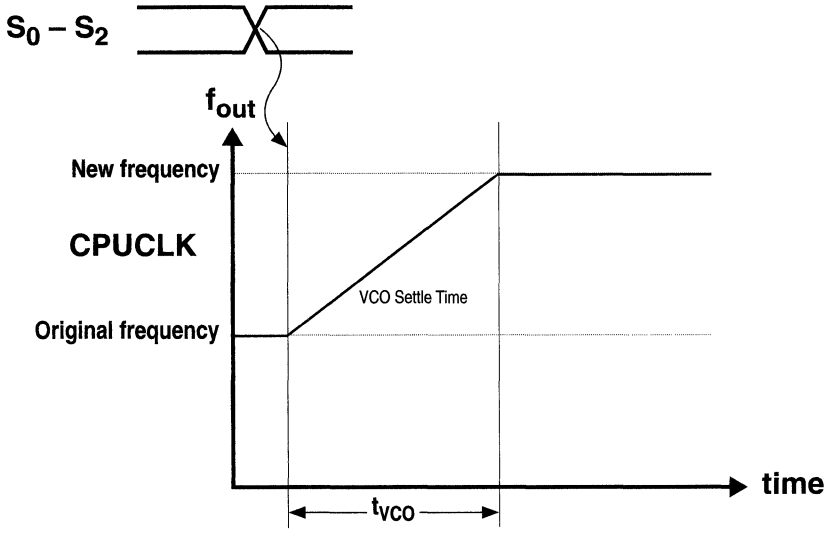
### Fig. 8: Rise and Fall Times



## Fig. 9: CPUCLK Skew

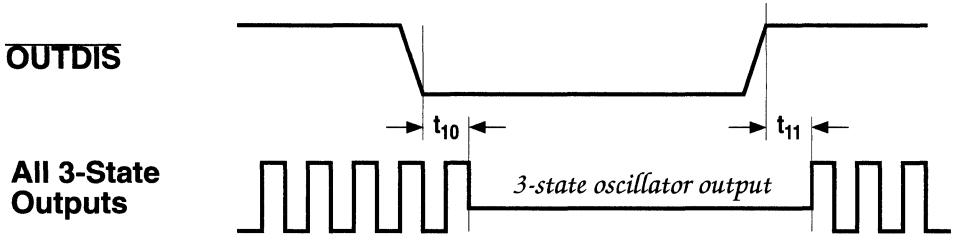



## Fig. 10: Selection Timing

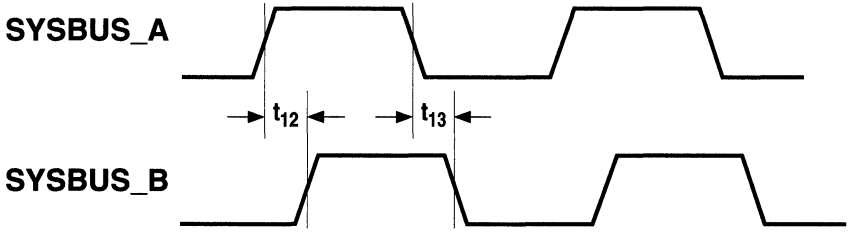



(Valid for all transitions except CPUCLK = 10 MHz ⟹ 100 MHz)

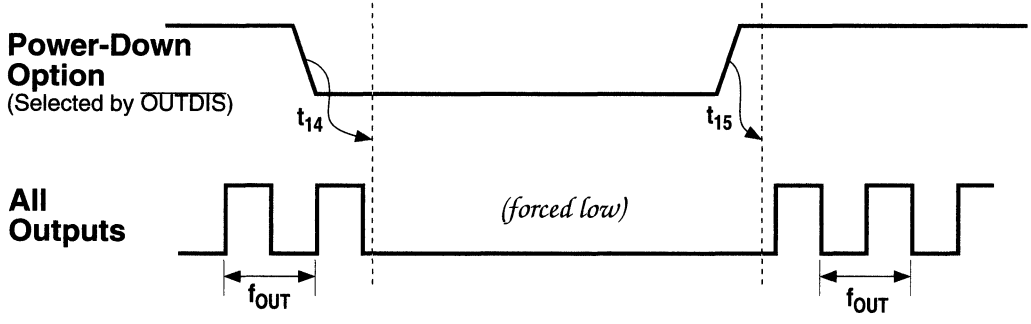
## Fig. 11: 3-State Timing



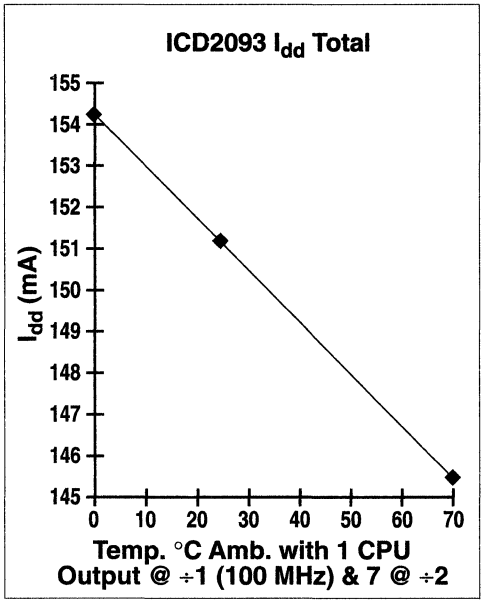

## Fig. 12: SYSBUS Skew

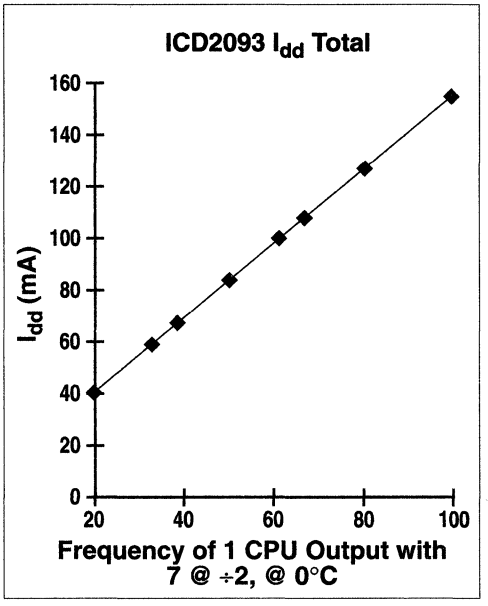


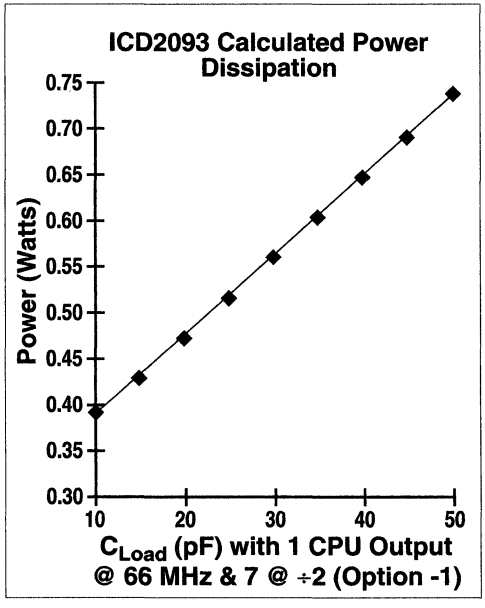

## Fig. 13: Power-Down Timing

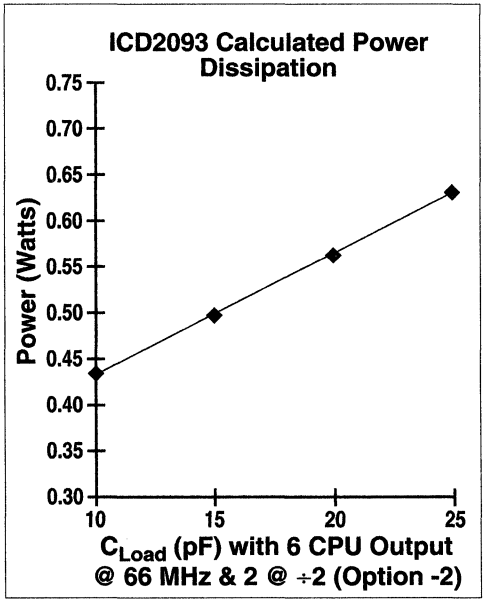


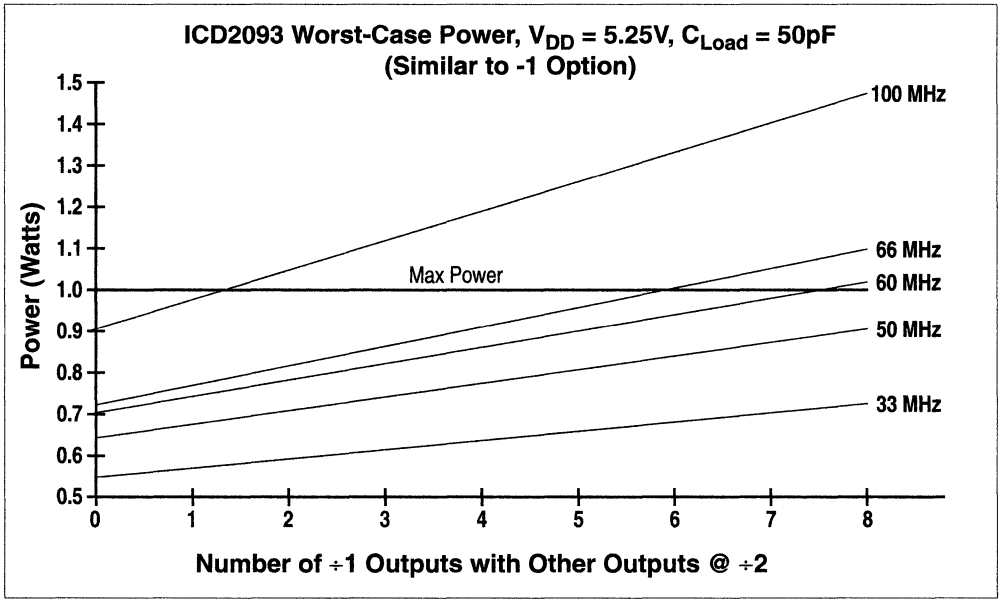
## Typical Performance Characteristics

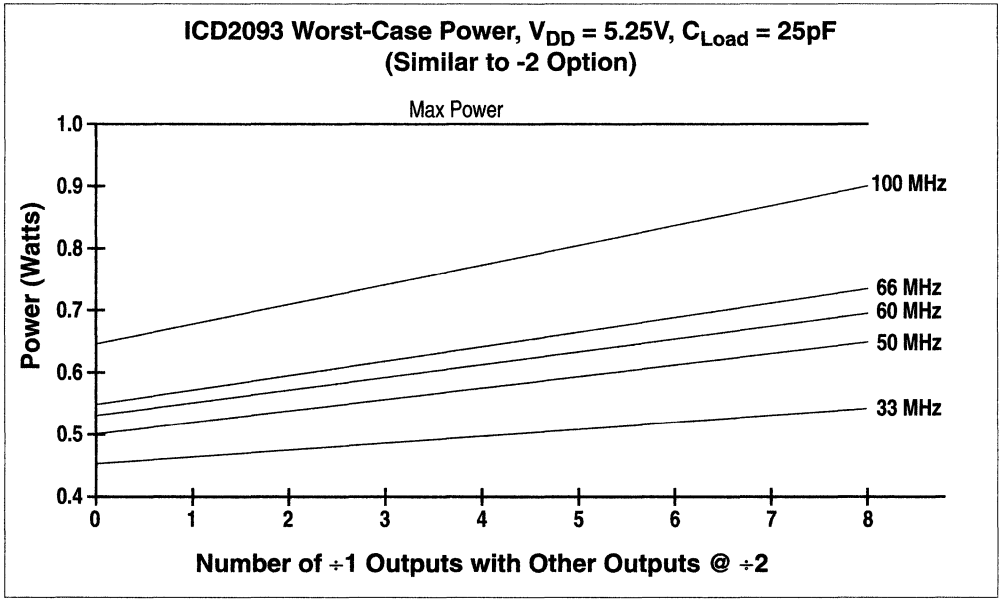



ICD2093 Worst-Case Power, $V_{DD}$ = 5.25V, $C_{Load}$ = 50pF
(Similar to -1 Option)
Power (Watts)
1.5
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
Max Power
100 MHz
66 MHz
60 MHz
50 MHz
33 MHz
0
1
2
3
4
5
6
7
8
Number of ÷1 Outputs with Other Outputs @ ÷2


ICD2093 Worst-Case Power, $V_{DD}$ = 5.25V, $C_{Load}$ = 25pF
(Similar to -2 Option)
Max Power
Power (Watts)
1.0
0.9
0.8
0.7
0.6
0.5
0.4
100 MHz
66 MHz
60 MHz
50 MHz
33 MHz
0
1
2
3
4
5
6
7
8
Number of ÷1 Outputs with Other Outputs @ ÷2

# Revision History / Credits

V1.0 (3/29/93) — Preliminary release
V1.3 (11/15/93) — Final Release Version

# Low-Power System Logic

2

# 2 – Low-Power System Logic 101

# ICD2029

## PC Notebook/Subnotebook/Palmtop Clock Generator

**Second-Generation Single-Chip Oscillator for Portable 3.3V & 5V Personal Computers**



- 8 Independent Clock Outputs Handle all Clocking for Portable Personal Computers
- Upward Compatible with Industry Standard ICD2028
- 4 User-Configurable Outputs
- CPU Clock Frequency Range: 196 KHz – 80 MHz (100 MHz @ 5V) with User-Defined Duty Cycle
- Skew-Free CPU Clock, CPU Clock ÷2 and Buffered CPU Clock Options
- Multiple Power-Down Modes with Suspend & Shutdown Capabilities
- Serially Cascadable Allows Direct Use with ICD2063 & another ICD2029
- Full Intel Clock Specification Compliance
- Supports Ethernet & SCSI Timing Specifications
- PLL Oscillator Input Derived from Single 14.31818 MHz or 20 MHz Crystal
- 32 KHz Reference Option Achieves Lowest Power in Industry
- Battery Input Runs 32.768 KHz Clock During Power-Down
- 3-State Oscillator Control Disables Outputs for Testing
- 3.3V & 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 20-Pin SOIC Package Configuration

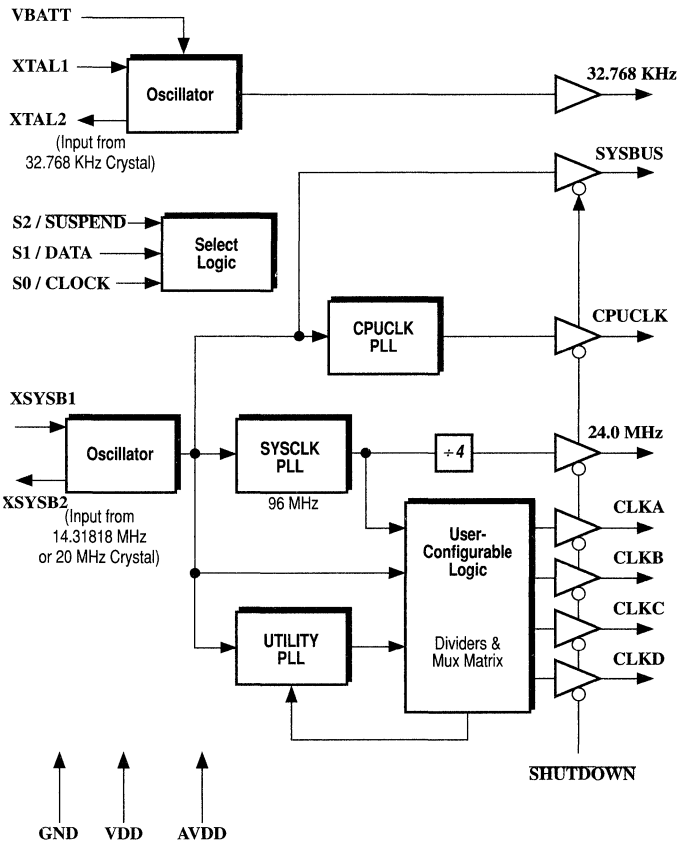



**Fig. 1: ICD2029 Block Diagram**

# ICD20291

## PC Notebook/Subnotebook/Palmtop Clock Generator

**Second-Generation Single-Chip Oscillator for Portable 3.3V & 5V Personal Computers**



- 8 Independent Clock Outputs Handle all Clocking for Portable Personal Computers
- Upward Compatible with Industry Standard ICD2028; Plug Compatible with ICD2029
- Multiple Power-Down Modes with Suspend & Shutdown Capabilities
- 4 User-Configurable Outputs
- CPU Clock Frequency Range: 196 KHz – 80 MHz (100 MHz @ 5V)
- Low Skew CPU Clock, CPU Clock ÷2 and Buffered CPU Clock Options
- Full Intel Clock Specification Compliance
- Supports Ethernet & SCSI Timing Specifications
- PLL Oscillator Input Derived from Single 14.31818 MHz or 20 MHz Crystal (Other Frequencies Available on Request)
- Battery Input Runs 32.768 KHz Clock During Power-Down
- 3-State Oscillator Control Disables Outputs for Testing
- 3.3V & 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 20-Pin SOIC Package Configuration

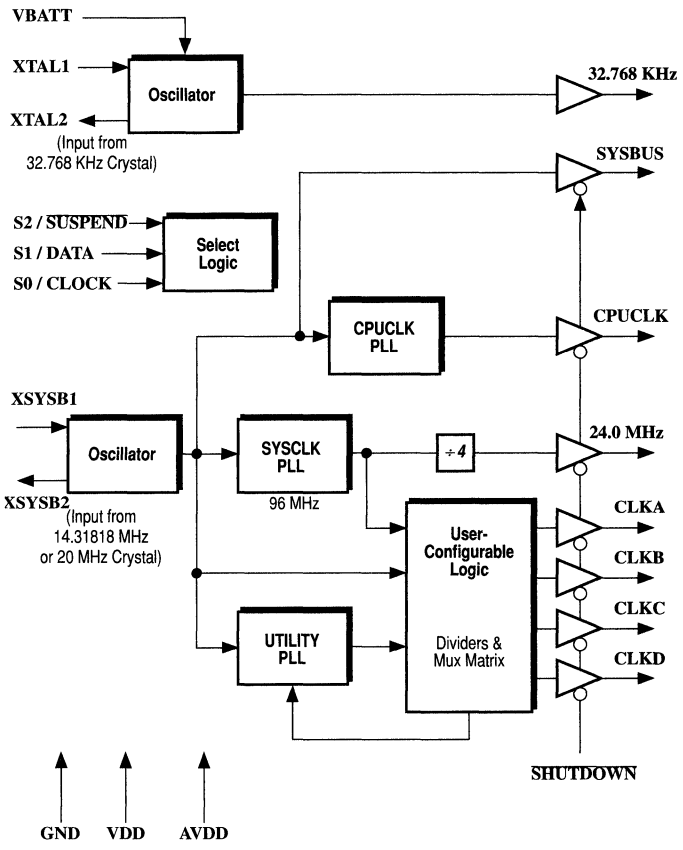



**Fig. 2: ICD20291 Block Diagram**

# Graphics Frequency Synthesizers

3

# 3 – Graphics Frequency Synthesizers 107

# ICD2042A

## Dual VGA Clock Generator

**Single-Chip Dual Oscillator for Personal Computer Graphics Boards**
**Handles Frequency Requirements of Popular VGA/XGA/8514 Chip Sets**

- 3 Independent Clock Outputs — Separate Pixel and Memory Clocks and Buffered Reference Clock
- Phase-Locked Loop Output Range of 350 KHz – 120 MHz
- Phase-Locked Loop Oscillator Input Derived from PC System Bus or from Single 14.31818 MHz Crystal
- Ideally Suited for VGA, XGA and 8514 Graphics Applications
- Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 3-State Oscillator Control Disables Outputs for Test Purposes
- "Change-on-the-Fly" Frequency Selection Supports Most Popular VGA/8514 Chip Sets
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 16-Pin SOIC Package

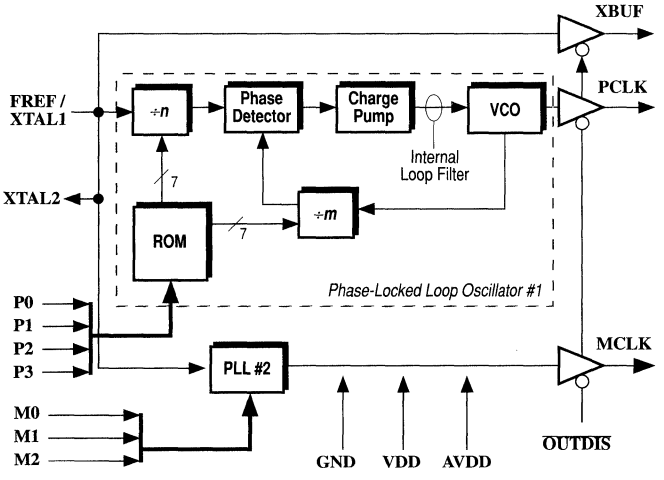



**Fig. 1: ICD2042A Block Diagram**

# Contents



# Figures



# Tables

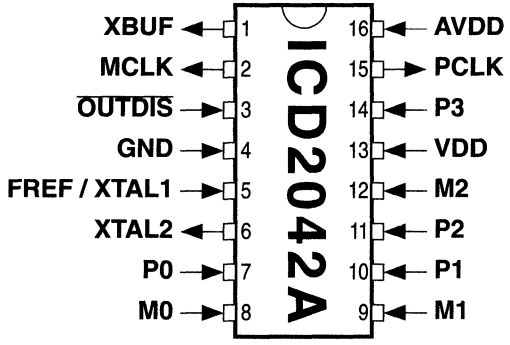
# Introduction

The proliferation of video standards, support for various monitors, increasing screen resolutions, and different memory speeds present in the DOS graphics community often require as many as six different crystal can oscillators per PC board. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of these oscillators required to build such multi-function graphic boards as EGA, VGA, Super VGA, and 8514. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2042A Dual VGA Clock Generator supports new designs using the newer graphic chip sets which generate output frequency select information. The ICD2042A features two independent clock outputs for the pixel clock and the memory clock which are chosen via select lines. Additional features include 3-stateable outputs and direct support for popular graphics chip set selection decodes.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions



## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | XBUF | Buffered Reference Frequency Output |
| 2 | MCLK | Memory Clock Oscillator Output (see *Table 2: Memory Clock ROM Decode Options* on page 115) |
| 3 | $\overline{\text{OUTDIS}}$ | Output Disable (Enable 3-State Output) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation not needed). |
| 4 | GND | Ground |
| 5 | FREF / XTAL1 | Input Reference Oscillator (nominally 14.31818 MHz.) A crystal may be used if a reference oscillator is not available. |
| 6 | XTAL2 | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |
| 7 | P0 | Input Pixel Clock Selection Signal — Bit 0 (internal pull-up) |
| 8 | M0 | Input Memory Clock Selection Signal — Bit 0 (internal pull-up) |
| 9 | M1 | Input Memory Clock Selection Signal — Bit 1 (internal pull-up) |
| 10 | P1 | Input Pixel Clock Selection Signal — Bit 1 (internal pull-up) |
| 11 | P2 | Input Pixel Clock Selection Signal — Bit 2 (internal pull-up) |
| 12 | M2 | Input Memory Clock Selection Signal — Bit 2 (internal pull-up) |
| 13 | VDD | +5V to I/O Ring |
| 14 | P3 | Input Pixel Clock Selection Signal — Bit 3 (internal pull-down) |
| 15 | PCLK | Pixel Clock Oscillator Output |
| 16 | AVDD | +5V to Analog Core (Special Order: bond VDD to AVDD internally.) |

# General Considerations

## Design Recommendations

The ICD2061A, with its ability to program the output frequencies, is recommended for designs in which a fixed ROM would be inconvenient and/or the desired volume does not warrant a custom ROM.

The ICD2042A is currently a custom order only.

## Pixel and Memory Clock Oscillator Selection

The output frequency value of the pixel clock oscillator (PCLK) is selected by the four pixel clock selection inputs: P0, P1, P2, and P3. This feature allows the ICD2042A to support different video configurations. The output frequency value of the memory clock oscillator (MCLK) is selected by the three memory clock selection inputs: M0, M1, and M2. The selection table is *Table 2: Memory Clock ROM Decode Options* on page 115.

At any time during operation, the selection lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transition period, the clock output will multiplex glitch-free to the reference signal until the PLL settles to the new frequency.

Normally, the MCLK select lines are hard-wired during manufacturing to correspond to the desired memory speed. A different memory clock frequency output may be generated by changing the memory select lines of the ICD2042A. The timing for this transition is detailed in *Table 6: AC Characteristics* on page 120.

## Table 2: Memory Clock ROM Decode Options

| M2 | M1 | M0 | Word | 2042–23 | 2042–24 | 2042–27 |
|---|---|---|---|---|---|---|
| | | | | (Frequencies in MHz) | | |
| 0 | 0 | 0 | 0 | 48.000 | 48.000 | 40.000 |
| 0 | 0 | 1 | 1 | 39.800 | 39.800 | 41.000 |
| 0 | 1 | 0 | 2 | 66.000 | 66.000 | 41.500 |
| 0 | 1 | 1 | 3 | 50.000 | 50.000 | 42.000 |
| 1 | 0 | 0 | 4 | 56.644 | 56.644 | 42.500 |
| 1 | 0 | 1 | 5 | 32.000 | 32.000 | 43.000 |
| 1 | 1 | 0 | 6 | 44.000 | 44.000 | 44.000 |
| 1 | 1 | 1 | 7 | 39.800 | 39.800 | 48.000 |



## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at the higher pixel clock frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. It is important that the ground plane be nearly continuous with a minimum of cuts, holes, or breaks. Both analog and digital ground pins should go directly to this plane.

To produce an output of high spectral purity, additional supply noise precautions might be required, particularly in noisy environments. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and AVDD can help to filter noisy supply lines.

The designer should also avoid routing the two output traces of the ICD2042A in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2042A closest to the device requiring the highest frequency. For more details concerning layout and power considerations, please see the IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281.

## Output Frequency Accuracy

The accuracy of the ICD2042A output frequencies depends on the target output frequencies. The tables within this document contain target frequencies which differ from the actual frequencies produced by the clock synthesizer.

The output frequencies of the ICD2042A are an integral fraction of the input (reference) frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2042A always produces an output frequency within 0.1% of the target frequencies listed, which is more than sufficient to meet standard display requirements. [Actual values are available from the factory.]

## 3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state the MCLK, PCLK and XBUF output lines. This supports wired-or connections between external clock lines (example: the Feature Connector external clock) and allows for procedures such as automated testing, where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up, but should be tied to VDD if not used.

## No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2042A.

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is typically 14.31818 MHz (as derived from the PC system bus) and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up-and-down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

The package leadframes are optimized for the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground-bounce and output crosstalk.

## Stability and "Bit-Jitter"



The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2042A is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures the loop filter will track the same process variations as does the VCO. With the ICD2042A, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

# Ordering Information

## Table 3: Order Codes

| Part Number | Package Type | Temperature Range | Pixel Clock ROM Option |
|---|---|---|---|
| ICD2042A | S = 16-Pin SOIC | C = Commercial[a] | Custom Order Only |

a. 0°C to +70°C

# Device Specifications

## Electrical Data

### Table 4: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 350 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 5: DC Characteristics

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2.0 | | Volts | |
| $V_{IL}$ | Low-level input voltage | | 0.8 | Volts | |
| $V_{OH}$ | High-level CMOS output voltage | $V_{DD}$ – 0.4 | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output voltage | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $I_{IH}$ | Input high current | | 150 | µA | $V_{IH} = V_{DD}$ |
| $I_{IL}$ | Input low current | | –250 | µA | $V_{IL}$ = 0V |
| $I_{OZ}$ | Output leakage current | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | | 50 | mA | (@ high frequency) |
| $I_{ADD}$ | Analog power supply current | | 6 | mA | |

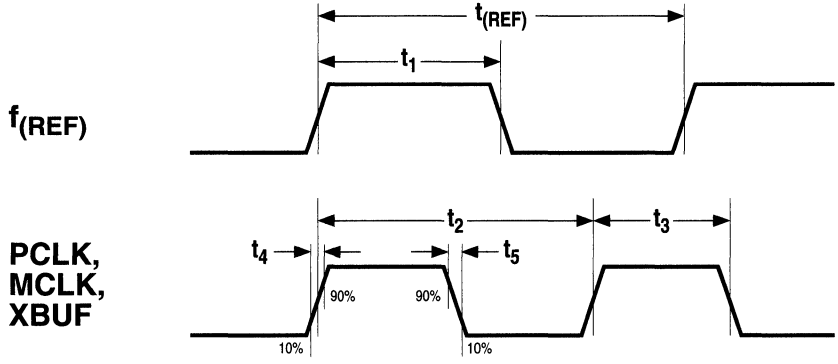
## Table 6: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value (Different reference frequencies require a custom ROM; standard parts use 14.31818 MHz, unless otherwise stated.) | 4 | 14.318 | 25 | MHz |
| $t_{(REF)}$ | reference clock period | $1 \div f_{(REF)}$ | 40 | 69.8 | 250 | ns |
| $t_1$ | input duty cycle | Duty cycle for the input oscillator defined as $t_1 \div t_{(REF)}$ | 25% | 50% | 75% | |
| $t_2$ | output period | CPUCLK oscillator value | 8.3 (120 MHz) | | 2857 (350 KHz) | ns |
| $t_3$ | output duty cycle | Duty cycle for the output oscillator defined as $t_3 \div t_2$ measured at 2.5V | 40% | | 60% | |
| $t_4$ | rise time | Rise time for the output oscillator into a 25pF load | | | 3 | ns |
| $t_5$ | fall time | Fall time for the output oscillator into a 25pF load | | | 3 | ns |
| $t_6$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion | | | 12 | ns |
| $t_7$ | clk valid | Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high | | | 12 | ns |
| $t_{MUXREF}$ | clk stable | Time required for the output oscillators to become valid after P0–3 or M0–2 select signals change value | 3.4 | 5 | 6.9 | msec |
| $t_{freq1}$ | freq1 output | Old frequency output | | | | |
| $t_{freq2}$ | freq2 output | New frequency output | | | | |
| $t_A$ | $f_{(REF)}$ mux time | Time clock output remains high while output muxes to reference frequency | $\frac{t_{(REF)}}{2}$ | | $3\frac{t_{(REF)}}{2}$ | |
| $t_B$ | $t_{freq2}$ mux time | Time clock output remains high while output muxes to new frequency value | $\frac{t_{freq2}}{2}$ | | $3\frac{t_{freq2}}{2}$ | |

**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

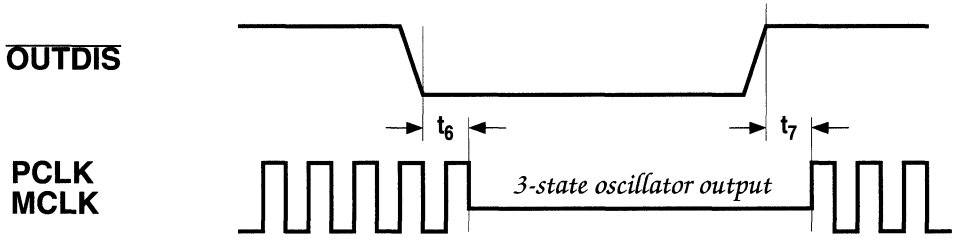
## Timing Diagrams

### Fig. 3: Rise and Fall Times

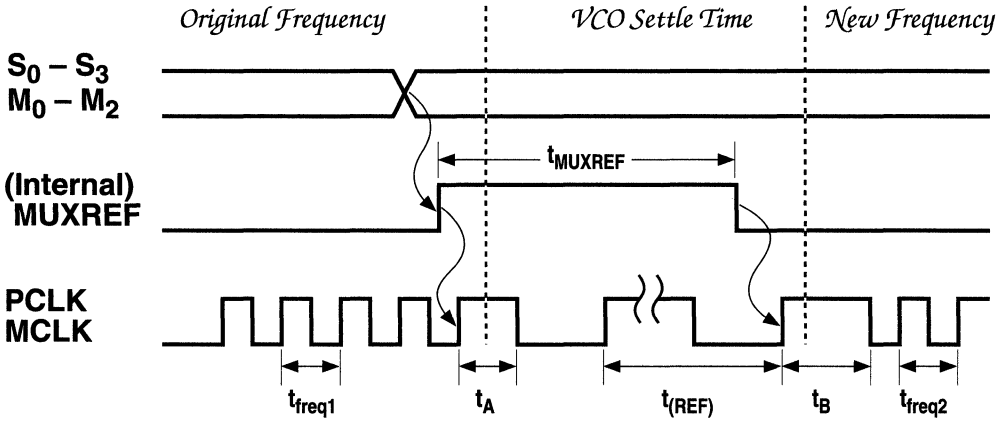





### Fig. 4: 3-StateTiming



## Fig. 5: Selection Timing



# Revision History / Credits

V2.4 (11/15/93) — Final Release Version

# ICD2061A

## Dual Programmable Graphics Clock Generator

**Single-Chip Dual Programmable Oscillator Handles All Frequency Requirements of Popular Graphics Chip Sets**

- 2nd Generation Dual Oscillator Graphics Clock Generator
- 2 Independent Clock Outputs from 390 KHz – 120 MHz
- Individually Programmable Oscillators Using a Highly Reliable Manchester-Encoded 21-Bit Serial Data Word
- 2-Pin Serial Programming Interface Allows Direct Connection to most Graphics Chip Sets with no External Hardware Required
- 2 Advanced Power-Down Capabilities
- 3-State Oscillator Control Disables Outputs for Test Purposes
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Sophisticated Internal Loop-Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 16-Pin SOIC Package Configuration

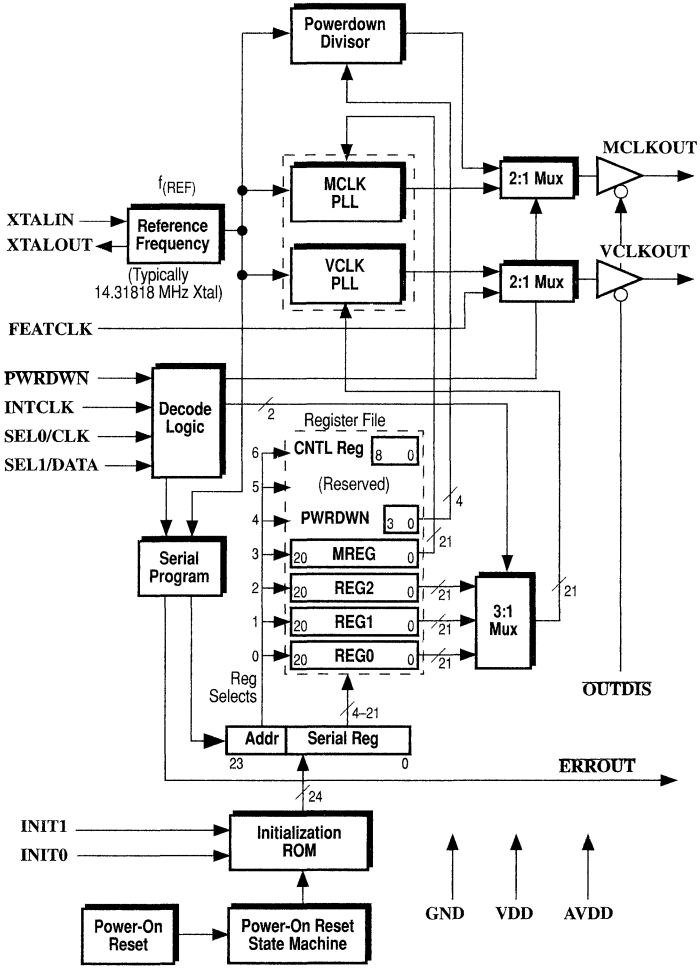



**Fig. 1: ICD2061A Block Diagram**

# Contents

## Figures



## Tables



3

# Introduction

The ICD2061A Dual Programmable Graphics Clock Generator features a fully programmable set of clock oscillators which can handle all frequency requirements of most graphics systems. The ICD2061A offers the selection ease of ROM-based clock chips, while also offering the versatility of serial programmed frequency synthesizers. It features advanced power-down capabilities, making it ideally suited for the portable computer market. The ICD2061A has extended frequency range and improved voltage/temperature stability when compared to first-generation frequency synthesizers.

The ICD2061A Dual Programmable Graphics Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 390 KHz and 120 MHz. The ICD2061A is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators.

Being able to change the output frequency dynamically adds a whole new degree of freedom for the electrical engineer heretofore unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

While primarily designed for the graphics subsystem market, the programming versatility of the ICD2061A makes it ideal wherever two variable, yet highly accurate, clock sources are required.

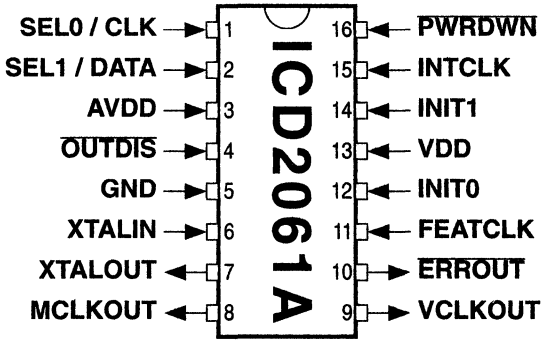
## ICD2061A Changes from the ICD2061

The ICD2061A revision of the ICD2061 is a complete mask redesign which includes feature enhancements as well as minor bug fixes. The following major modifications have been implemented:

- **Increased Frequency Resolution** — 3 additional bits have been added to the CNTL Register to allow an optional pre-divide by 2 on the P Counter. Full upward compatibility with existing software is maintained.
- **Reduced Power Consumption** — By dynamically switching in a weak pull-up when the user pulls the $\overline{\text{PWRDWN}}$ pin low, the power consumption of the ICD2061A in Power-down Mode 2 has been reduced to $^1/_4$ that of the ICD2061 (less than 50 µA).
- **Glitch-Free Transitions** — Reprogramming the MCLK and the active VCLK registers is now glitch-free; the Reference Frequency is automatically multiplexed to the appropriate output pin during the transition period.
- **Extended Low-Frequency Range** — The lower frequency limit has been extended to 390 KHz as a result of the addition of a ÷128 value to the Post-VCO Divide Register.
- **Enhanced VCO** — The redesigned VCOs generate 30% less jitter than those of previous versions.
- **New Index Table** — The new VCOs require a change in the Index Table values.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions



## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | SEL0 / CLK | Bit 0 (LSB) of frequency select logic, used to select oscillator frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.) |
| 2 | SEL1 / DATA | Bit 1 (MSB) of frequency select logic, used to select oscillator frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.) |
| 3 | AVDD | +5V to Analog Core |
| 4 | $\overline{\text{OUTDIS}}$ | Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect.) |
| 5 | GND | Ground |
| 6 | XTALIN | Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock signal may be used as input if available. |
| 7 | XTALOUT | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |
| 8 | MCLKOUT | Memory Clock out |
| 9 | VCLKOUT | Video Clock out |
| 10 | $\overline{\text{ERROUT}}$ | Error Output: a low signals an error during serial programming. |
| 11 | FEATCLK | External clock input (Feature Clock) (Internal pull-up allows no-connect.) |
| 12 | INIT0 | Select power-up initial conditions (LSB) (Internal pull-down allows no-connect.) |
| 13 | VDD | +5V to I/O Ring |
| 14 | INIT1 | Select power-up initial conditions (MSB) (Internal pull-down allows no-connect.) |
| 15 | INTCLK | Selects the Feature Clock external clock input as VCLKOUT output (Internal pull-up allows no-connect.) |
| 16 | $\overline{\text{PWRDWN}}$ | Power-down pin (active low) (Internal pull-up allows no-connect if power-down operation not required. See *Power Management Issues* on page 145 for specific details concerning the use of this pin.) |

# Register Definitions

## Register File

The Register File consists of the following registers and their selection addresses:

**Table 2: Register Addressing**

| Address | Register | Usage |
|---|---|---|
| 000 | REG0 | Video Clock Register 1 |
| 001 | REG1 | Video Clock Register 2 |
| 010 | REG2 | Video Clock Register 3 |
| 011 | MREG | Memory or I/O Timing Clock |
| 100 | PWRDWN | Divisor for Power-Down mode |
| 101 | (Reserved) | |
| 110 | CNTL Reg | Control Register |

All register values are preserved in power-down mode.

## Power-On Reset and Register Initialization

The ICD2061A Clock Synthesizer has several of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three VGA registers are initialized based on the state of the INIT1 and INIT0 pins at power-up. Also, the Memory Clock is initialized based on the INIT pins.

The Power-On Reset Function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with VDD if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as follows (all frequencies in MHz):

**Table 3: Register Initialization — ROM Option 1**

| INIT1 | INIT0 | MREG | REG0 | REG1 | REG2 |
|---|---|---|---|---|---|
| | | (Frequencies in MHz) | | | |
| 0 | 0 | 32.500 | 25.175 | 28.322 | 28.322 |
| 0 | 1 | 40.000 | 25.175 | 28.322 | 28.322 |
| 1 | 0 | 50.350 | 40.000 | 28.322 | 28.322 |
| 1 | 1 | 56.644 | 40.000 | 50.350 | 50.350 |



## Register Selection

The Video Clock output is controlled not only by the SEL0 & SEL1 bits, but also by the $\overline{\text{PWRDWN}}$ and $\overline{\text{OUTDIS}}$ signals. Additionally, the Clock Synthesizer is multiplexed with an external frequency input (FEATCLK) which corresponds to the IBM VGA Feature Clock standard. The following table shows the VCLKOUT selection criteria:

**Table 4: VCLKOUT Selection**

| OUTDIS | PWRDWN | INTCLK | SEL1 | SEL0 | VCLKOUT |
|---|---|---|---|---|---|
| 0 | X | X | X | X | High-Z |
| 1 | 0 | X | X | X | Forced High |
| 1 | 1 | X | 0 | 0 | REG0 |
| 1 | 1 | X | 0 | 1 | REG1 |
| 1 | 1 | 0 | 1 | 0 | FEATCLK |
| 1 | 1 | 1 | 1 | X | REG2 |
| 1 | 1 | X | 1 | 1 | REG2 |

The Memory Clock output is controlled by the $\overline{\text{PWRDWN}}$ and $\overline{\text{OUTDIS}}$ signals as indicated below:
MCLKOUT Selection

**Table 5: MCLKOUT Selection**

| $\overline{\text{OUTDIS}}$ | PWRDWN | MCLKOUT |
|---|---|---|
| 0 | X | High-Z |
| 1 | 1 | MREG |
| 1 | 0 | PWRDWN[a] |

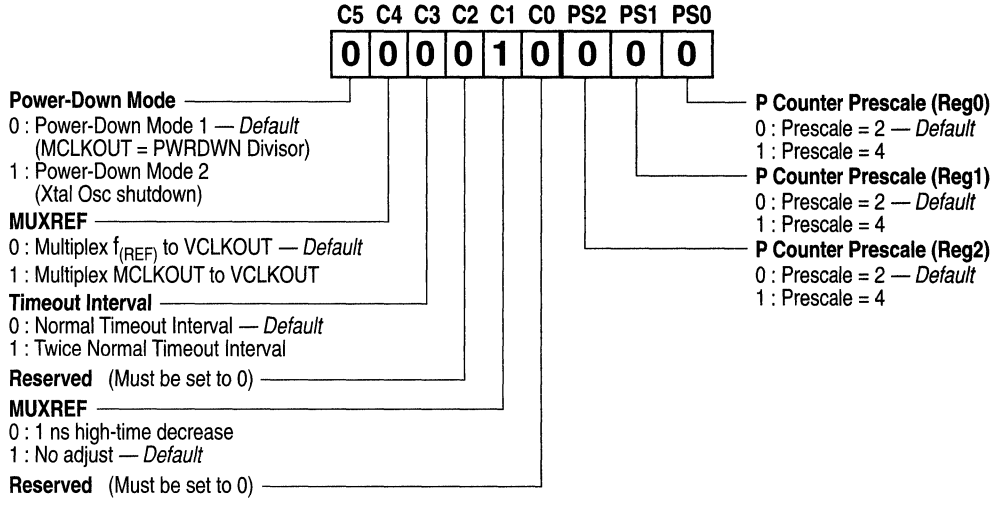
a. Power-Down Mode (1 or 2) is determined by the setting of bit C5 in the CNTL Reg. See *Control Register Definition* on page 135.

The Clock Select pins SEL0 & SEL1 have a dual purpose. When these pins are performing serial down-load, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins SEL0 & SEL1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f_{(REF)}$ for an additional timeout interval to give the VCO time to settle to its new value. [The timeout interval in both cases is approximately 5 msec — see the timeout interval spec in *AC Characteristics* on page 153.]

When a new frequency is being set for MCLK, or if the active VCLK register is reprogrammed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent after the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See *AC Characteristics* on page 153 for further details).

## Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined as follows:




## Fig. 3: Control Register

**Duty Cycle Adjust** — This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the Threshold Voltage $V_{TH}$ is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

**Timeout Interval** — The Timeout Interval is normally defined as in the *AC Characteristics* on page 153. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the Timeout Interval is doubled.

**MUXREF** — This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

**Power-Down Mode** — This control bit determines which Power-Down Mode the $\overline{\text{PWRDWN}}$ pin will implement. The default (Power-Down Mode 1) forces the MCLKOUT signal to be a function of the PWRDWN register. Power-Down Mode 2 turns off the crystal oscillator and disables all outputs. There is a more detailed description in the section entitled *Power Management Issues* on page 145.

**P Counter Prescale** (REG0, REG1, REG2) — These control bits determine whether or not to prescale the P Counter value, which allows "fine tuning" the output frequency of the respective register. Prescaling is explained in more detail in various sections of this Datasheet.

# Serial Programming Architecture

The ICD2061A programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (See *Fig. 1: ICD2061A Block Diagram* on page 125.) contains several components: a Serial Unlock Decoder (containing the Unlocking Mechanism and Manchester Decoder), a Watchdog Timer, the Serial Data Register (Serial Reg) and a Demultiplexer to the Register File.

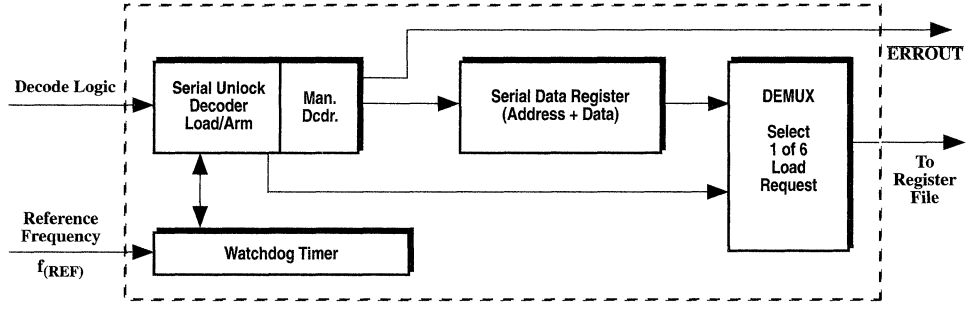



**Fig. 4: Serial Program Block Diagram — Detail**

## Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in the following timing diagram:

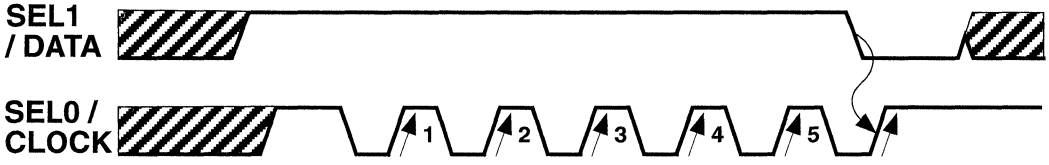



**Fig. 5: Unlock Sequence**

The initial unlock sequence consists of at least five low-to-high transitions of CLK with DATA high, followed immediately by a single low-to-high transition of CLK with DATA low. Following this unlock sequence, the encoded serial data is clocked into the Serial Data Register (Serial Reg).

NOTE: The ICD2061A may not be serially programmed when in Power-Down Mode.

## Watchdog Timer

Following any transition of CLK or DATA, the Watchdog Timer is reset and begins counting. Throughout the entire programming process, the Watchdog Timer ensures that successive edges of CLK or DATA do not violate the timeout specification (of 2 msec — see *AC Characteristics* on page 153.). If a timeout does occur, the Lock Mechanism is rearmed and the current data in the Serial Data Register (Serial Reg) is ignored.

Since the VCLK registers are selected by the SEL0 or SEL1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. [Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.]



## Serial Data Register

The serial data is clocked into the Serial Data Register (Serial Reg) in the following order:

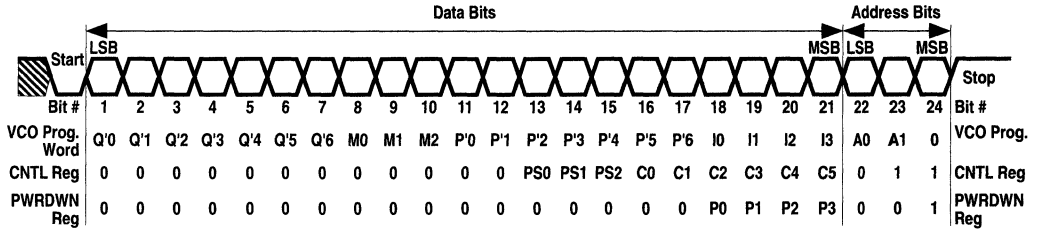



**Fig. 6: Serial Data Timing**

The serial data is sent using a modified Manchester encoded data format. This is defined as follows:

1 — An individual data bit is sampled on the rising edge of CLK.

2 — The complement of the data bit must be sampled on the previous falling edge of CLK.

3 — The Setup and Hold Time requirements must be met on both CLK edges.

4 — The unlock sequence, start, and stop bits are not Manchester encoded.

For specifics on timing, see *Fig. 14: Serial Programming Timing* on page 157.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4

fields: D[20:17] = Index; D[16:10] = P'; D[9:7] = Mux; D[6:0] = Q'. [See *Programming the ICD2061A* on page 140 for more details on the VCO data word.] For the other registers with fewer than 21 bits (PWRDWN, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The Unlocking Mechanism then automatically rearms itself following the load. Only when the Watchdog Timer has timed out are the SEL0 & SEL1 Selection Pins permitted to return to their normal register select function.

Note that the Serial Data Register (Serial Reg) which receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command which passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data Register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the Unlocking Mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the Serial Buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the Unlocking Mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the Unlocking Mechanism is rearmed, the Serial Counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

## ERROUT Operation

The ERROUT signal is used to report when a program error has been detected internally by the ICD2061A. The signal stays active until the next unlock sequence.

The following circuit shows the basic mechanism used to detect valid and erroneous serial data:

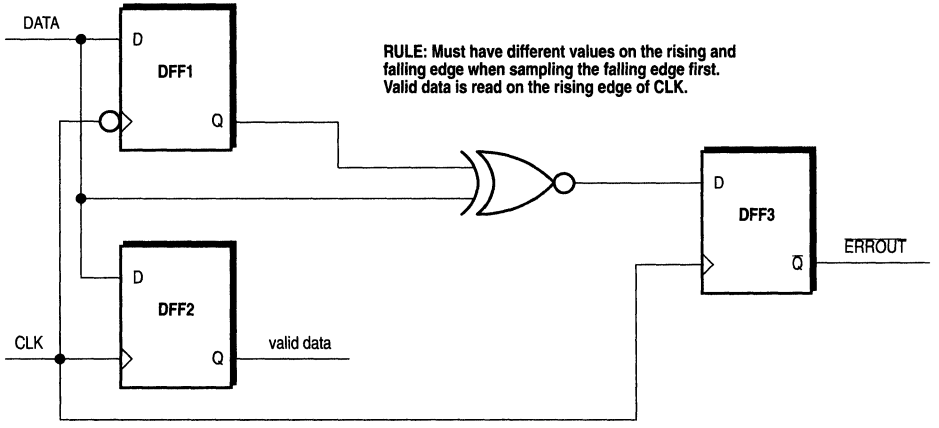



**Fig. 7: Modified Manchester Decoder Circuit**

The ERROUT signal is invoked for any of the following error conditions: incorrect start bit; incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

NOTE: If there is no input pin available on the target VGA controller chip to monitor ERROUT, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming accuracy.

# Programming the ICD2061A

The desired output frequency is defined via a serial interface, with a 21–bit number shifted in. The ICD2061A has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

## Table 6: Programming Word Bit Fields

| Field | # of Bits | Notes |
|---|---|---|
| Index (I) | 4 | MSB (Most Significant Bits) |
| P Counter value (P') | 7 | |
| Mux (M) | 3 | |
| Q Counter Value (Q') | 7 | LSB (Least Significant Bits) |

The frequency of the Programmable Oscillator f(VCO) is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 60 MHz; typically 14.31818 MHz)

NOTE: If a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of $f_{(VCO)}$ must remain between 50 MHz and 120 MHz inclusive. Therefore, for output frequencies below 50 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux Field (M) as follows:

## Table 7: Post-VCO Divisor

| M | Divisor |
|---|---|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 100 | 16 |
| 101 | 32 |
| 110 | 64 |
| 111 | 128 |



The Index Field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (This table is referenced to the VCO frequency, $f_{(VCO)}$, rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running.

When the Index Field is set to **1111**, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, one doesn't want the two VCOs to run at integral multiples of each other; therefore, if one does want the clocks to run at $2^n$ (n = 0, 1, 2 .. 7) multiples of each other, this is done by turning off the VCLK VCO and multiplexing the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

## Table 8: Index Field (I)

| I | VCLK $f_{VCO}$ (MHz) | MCLK $f_{VCO}$ (MHz) |
|---|---|---|
| 0000 | 50.0 – 51.0 | 50.0 – 51.0 |
| 0001 | 51.0 – 53.2 | 51.0 – 53.2 |
| 0010 | 53.2 – 58.5 | 53.2 – 58.5 |
| 0011 | 58.5 – 60.7 | 58.5 – 60.7 |
| 0100 | 60.7 – 64.4 | 60.7 – 64.4 |
| 0101 | 64.4 – 66.8 | 64.4 – 66.8 |
| 0110 | 66.8 – 73.5 | 66.8 – 73.5 |
| 0111 | 73.5 – 75.6 | 73.5 – 75.6 |
| 1000 | 75.6 – 80.9 | 75.6 – 80.9 |
| 1001 | 80.9 – 83.2 | 80.9 – 83.2 |
| 1010 | 83.2 – 91.5 | 83.2 – 91.5 |
| 1011 | 91.5 – 100.0 | 91.5 – 100.0 |
| 1100 | 100.0 – 120.0 | 100.0 – 120.0 |
| 1101 | 100.0 – 120.0 | 100.0 – 120.0 |
| 1110 | Turn off VCLK | 100.0 – 120.0 |
| 1111 | Mux MCLK to VCLK | 100.0 – 120.0 |

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

## Programming Constraints

There are five primary programming constraints the user must be aware of:

$$1\ \text{MHz} \leq f_{(REF)} \leq 60\ \text{MHz}$$

$$200\ \text{KHz} \leq \frac{f_{(REF)}}{Q} \leq 1\ \text{MHz}$$

$$50\ \text{MHz} \leq f_{(VCO)} \leq 120\ \text{MHz}$$

$$3 \leq Q \leq 129$$

$$4 \leq P \leq 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the ***BitCalc*** program, these constraints become transparent.



## Programming Example — Prescaling = 2 (default)

The following is an example of the calculations ***BitCalc*** performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 50 MHz, double it to 79.0 MHz. Set M to 001. Set I to 1000. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

**Table 9: P & Q Value Pairs**

| P | Q | $f_{(VCO)}$ ( MHz ) | Error ( ppm ) |
|---|---|---|---|
| 69 | 25 | 79.0363 | 460 |
| 80 | 29 | 78.9969 | 40 |
| 91 | 33 | 78.9669 | 419 |

Choose (P, Q) = (80,29) for best accuracy (40 PPM).

Therefore:

$$P' = P-3 = 80-3 = 77 = 1001101 \text{ (4dH)}$$

$$Q' = Q-2 = 29-2 = 27 = 0011011 \text{ (1bH)}$$

and the full programming word, W, is:

$$W = I, P', M, Q' = 1000, 1001101, 001, 0011011 = 10001001101001011011 \text{ (11349bH)}$$

The programming word W is then sent as a serial bit stream, LSB first. Appropriate address bits and start & stop bits must also be included as defined in the Serial Programming Scheme section.

## Programming Example — Prescaling = 4

Assume the desired VCLKOUT frequency is 100 MHz. The table below compares the results of using the default prescaling value of 2 and the optional prescaling value of 4:

**Table 10: Prescale Values**

| Prescale | Actual Frequency ( MHz ) | P | Q | PPM Err |
|---|---|---|---|---|
| 2 | 99.84028 | 129 | 37 | 1600 |
| 4 | 99.99998 | 110 | 63 | 0 |

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2) — which involves loading a Control Word (taking care to preserve the current values of the other Control Bits) — before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)

2. Program the VCO (load a Program Word)

NOTE: Care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

# Power Management Issues

## Power-Down Mode 1

The ICD2061A contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling the PWRDWN signal low and having the proper CNTL Reg bit set to zero), both VCOs are shut down, the VCLKOUT output is forced high, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The Power-down MCLKOUT value is determined by the following equation:

$$\mathbf{MCLKOUT_{Power\text{-}Down} = f_{(REF)} \div (PWRDWN\ Reg\ Divisor\ Value)}$$

The Power-Down Register divisor is determined according to the following 4-bit word programmed into the PWRDWN Register:



### Table 11: PWRDWN Register Programming

| PWRDWN bits P3 P2 P1 P0 | PWRDWN Register Value | Power-Down Divisor | $MCLKOUT_{Power\text{-}Down}$ ($f_{(REF)}$ = 14.31818 MHz) |
|---|---|---|---|
| 0 0 0 0 | 0 | N/A | N/A |
| 0 0 0 1 | 1 | 32 | 447.4 KHz |
| 0 0 1 0 | 2 | 30 | 477.3 KHz |
| 0 0 1 1 | 3 | 28 | 511.4 KHz |
| 0 1 0 0 | 4 | 26 | 550.7 KHz |
| 0 1 0 1 | 5 | 24 | 596.6 KHz |
| 0 1 1 0 | 6 | 22 | 650.8 KHz |
| 0 1 1 0 | 7 | 20 | 715.9 KHz |
| **1 0 0 0** | **8 (default)** | **18** | **795.5 KHz** |
| 1 0 0 1 | 9 | 16 | 894.9 KHz |
| 1 0 1 0 | A | 14 | 1.023 MHz |
| 1 0 1 1 | B | 12 | 1.193 MHz |
| 1 1 0 0 | C | 10 | 1.432 MHz |
| 1 1 0 1 | D | 8 | 1.790 MHz |
| 1 1 1 0 | E | 6 | 2.386 MHz |
| 1 1 1 1 | F | 4 | 3.580 MHz |

On Power-Up, the value of the PWRDWN Register is loaded with a default value of 8 (1000 binary), which yields an MCLKOUT frequency of 795 KHz (14.31818 / 18). The default mode is Power-Down Mode 1.

NOTE: The ICD2061A may not be serially programmed when in Power-Down Mode.

## Power-Down Mode 2

If there is no need for any output during power-down operation, then an alternate power-down mode is available, which will completely shut down all outputs and the reference oscillator, yet still preserve all register contents. This results in the absolute least power consumption.

Power-Down Mode 2 is invoked by first programming the Power-Down bit in the CNTL Reg, and then pulling the $\overline{\text{PWRDWN}}$ pin low.

## The $\overline{\text{PWRDWN}}$ Pin

This pin has a standard internal pull-up during normal operation. When the user pulls it down to invoke power-down Mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which significantly reduces power consumption. If, after pulling this pin low, the pin is allowed to float, the weak pull-up will gradually cause the signal to rise, enabling the normal pull-up, and will eventually turn the device back on.

## Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I = C \bullet V \bullet f$, where

$I$ = current (in mA),

$C$ = load capacitance (max. 25pF),

$V$ = output voltage (usually 5V), and

$f$ = output frequency (in MHz).

To calculate total operating current, sum the following terms:

VCLKOUT $\Rightarrow$ $C \bullet V \bullet f_{(VCLK)}$

MCLKOUT $\Rightarrow$ $C \bullet V \bullet f_{(MCLK)}$

Internal $\Rightarrow$ 12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on package type.

## Table 12: Typical Values

| Frequency | Capacitive Load | Current ( mA ) |
|---|---|---|
| low | low | 15 |
| high | low | 40 |
| high | high | 65 |

When in Power-Down Mode 1, and using a 14.31818 MHz reference crystal, the power consumption should not exceed 7.5 mA. In Power-Down Mode 2, the power consumption should not exceed 50 µA.

# Circuit Operation

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown below. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

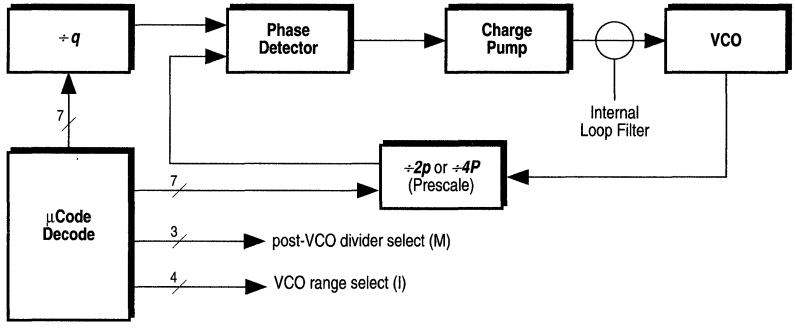



**Fig. 8: Phase-Locked Loop Oscillator**

## Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphics designs.

## Frequency Range

The output frequency range of both Phase-Locked Loop sections is 390 KHz – 120 MHz.

## Output Disable

When the $\overline{\text{OUTDIS}}$ pin is asserted (active low), all the output pins except XTAL OUT and $\overline{\text{ERROUT}}$ enter a high impedance mode, to support automated board testing.

## External Clock Input (Feature Connector Compatibility)

To maintain backward compatibility to the VGA feature connector standard, the Video Clock output VCLKOUT can multiplex between the clock synthesizer output and the external clock input FEATCLK. This multiplexing is controlled by the INTCLK input signal and appropriate decode of selection signals (SEL0, SEL1). See the section on Register Definitions for more information.



## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2061A in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2061A closest to the device requiring the highest frequency.

## FCC & Noise issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note *Minimizing Radio Frequency Emissions* on page 285.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on opposite sides of the die. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2061A is inherently stable over temperature, voltage and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2061A, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

# Ordering Information

## Table 13: Order Codes

| Part Number | Package Type | Temperature Range | Chip Options |
|---|---|---|---|
| ICD2061A | S = 16-Pin SOIC DIP | C = Commercial[a] | –1<br><br>(Other ROM options by special order.) |

a. 0°C to +70°C



Example: order ICD2061ASC–1 for the ICD2061A, 16-pin plastic SOIC, commercial temperature range device with the initial frequencies shown in *Table 3: Register Initialization — ROM Option 1* on page 133.

# Device Specifications

## Electrical Data

### Table 14: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 350 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 15: DC Characteristics

| Name | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2.0 | | | Volts | |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | Volts | |
| $V_{OH}$ | High-level CMOS output voltage | 2.4 | | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output voltage | | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $I_{IH}$ | Input high current | | | 150 | µA | $V_{IH} = V_{DD}$ |
| $I_{IL}$ | Input low current | | | –250 | µA | $V_{IH}$ = 0.5V |
| $I_{OZ}$ | Output leakage current | | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | 15 | | 65 | mA | |
| $I_{DD-TYP}$ | Power supply current (typical) | | 35 | | mA | @ 60 MHz |
| $I_{ADD}$ | Analog power supply current | | | 10 | mA | |
| $I_{PD1}$ | Power-down current (Mode 1) | | 6 | 7.5 | mA | |
| $I_{PD2}$ | Power-down current (Mode 2) | | 25 | 50 | µA | |

## Table 16: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value (Note: for references of other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.) | 1 | 14.318 | 60 | MHz |
| $t_{(REF)}$ | reference period | $1 \div f_{(REF)}$ | 16.6 | | 1000 | ns |
| $t_1$ | input duty cycle | Duty cycle for the input oscillator defined as $t_1 \div t_{(REF)}$ | 25% | 50% | 75% | |
| $t_2$ | output clock periods | Output oscillator values | 8.33<br>120 MHz | | 2564<br>390 KHz | ns |
| $t_3$ | output duty cycle | Duty cycle for the output oscillators (NOTE: duty cycle is measured at CMOS threshold levels. At 5V, $V_{TH}$ = 2.5V.) | 40% | | 60% | |
| $t_4$ | rise times | Rise time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_5$ | fall times | Fall time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_{freq1}$ | freq1 output | Old frequency output | | | | |
| $t_{freq2}$ | freq2 output | New frequency output | | | | |
| $t_A$ | $f_{(REF)}$ mux time | Time clock output remains high while output muxes to reference frequency | $\frac{t_{(REF)}}{2}$ | | $3\frac{t_{(REF)}}{2}$ | ns |
| $t_{timeout}$ | timeout interval | Internal interval for serial programming and for VCO changes to settle. [If the interval is too short, see the *Timeout Interval* paragraph on page 135.] | 2 | 5 | 10 | msec |
| $t_B$ | $t_{freq2}$ mux time | Time clock output remains high while output muxes to new frequency value | $\frac{t_{freq2}}{2}$ | | $3\frac{t_{freq2}}{2}$ | ns |
| $t_6$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{OUTDIS}$ signal assertion | 0 | | 12 | ns |
| $t_7$ | clk valid | Time for the output oscillators to recover from 3-state mode after $\overline{OUTDIS}$ signal goes high | 0 | | 12 | ns |
| $t_8$ | Power-Down | Time for Power-Down Mode of operation to take effect | | | 12 | ns |
| $t_9$ | Power-Up | Time for recovery from Power-Down Mode of operation | | | 12 | ns |

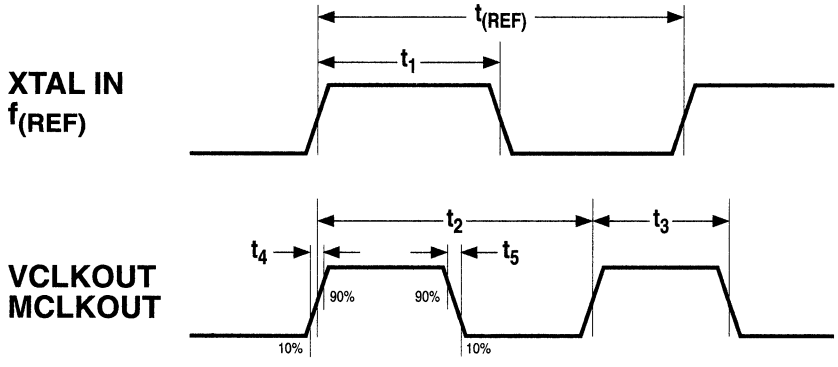
## Table 16: AC Characteristics (Continued)

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{10}$ | MCLKOUT high | Time for MCLKOUT to go high after PWRDWN is asserted high | 0 | | $t_{PWR-DWN}$ | ns |
| $t_{11}$ | MCLKOUT delay | Delay of MCLKOUT prior to $f_{MCLK}$ signal at output | $\frac{t_{MCLK}}{2}$ | | $3\frac{t_{MCLK}}{2}$ | ns |
| $t_{serclk}$ | | Clock period of serial clock | $2 \cdot t_{(REF)}$ | | 2 | msec |
| $t_{HI}$ | | Minimum high time | $t_{(REF)}$ | | | ns |
| $t_{LO}$ | | Minimum low time | $t_{(REF)}$ | | | ns |
| $t_{SU}$ | | Setup time | 20 | | | ns |
| $t_{HD}$ | | Hold time | 10 | | | ns |
| $t_{ldcmd}$ | | Load command | 0 | | $t_1 + 30$ | ns |

**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

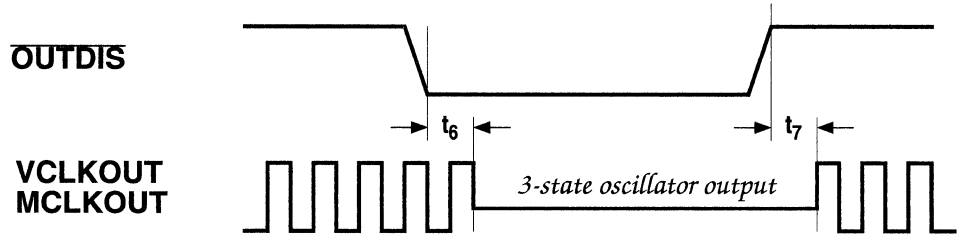
## Timing Diagrams

### Fig. 9: Rise and Fall Times

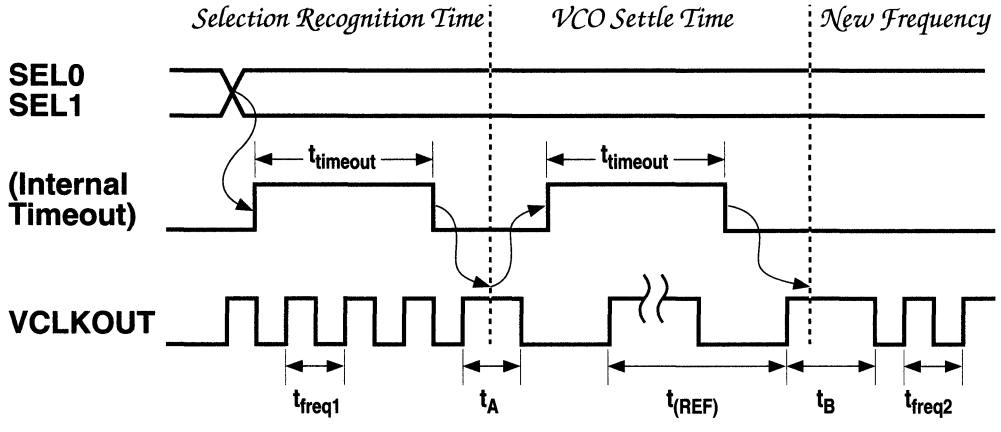




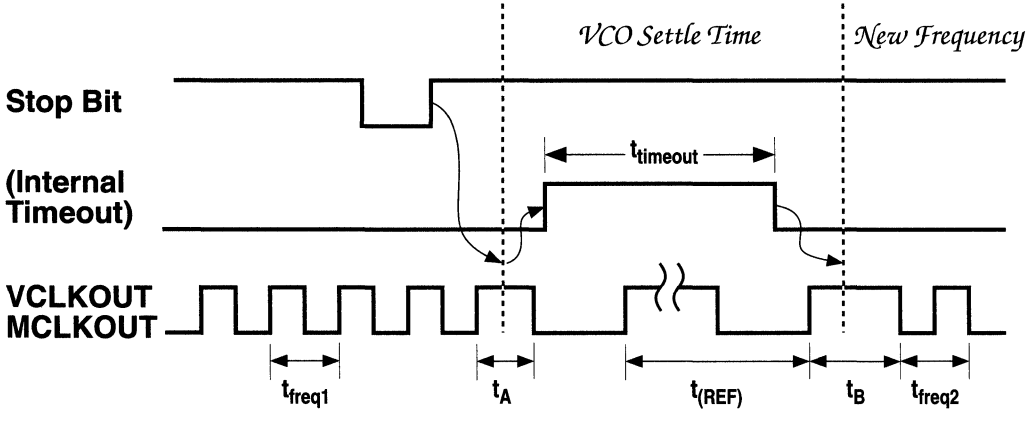

### Fig. 10: 3-State Timing



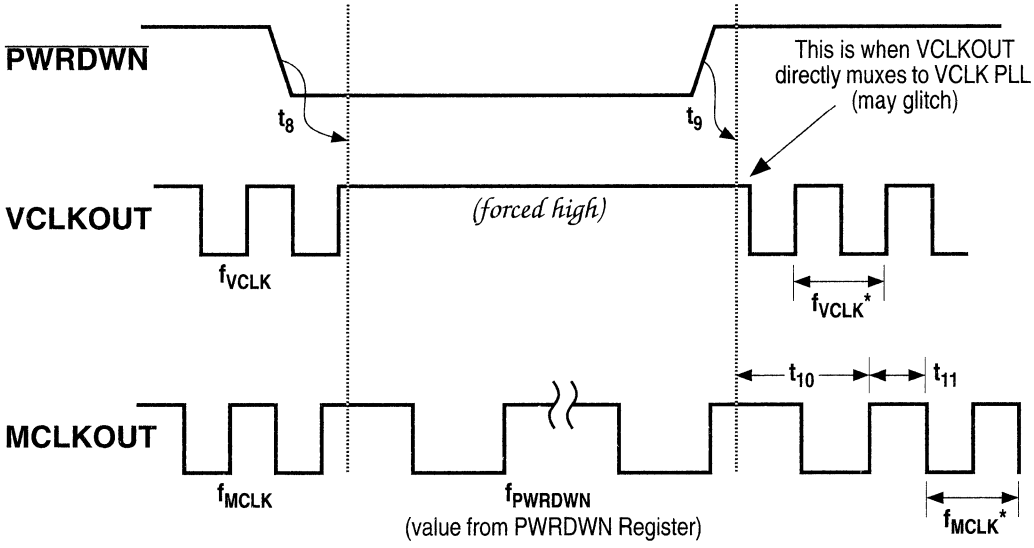
## Fig. 11: Selection Timing




## Fig. 12: MCLK & Active VCLK Register Programming Timing

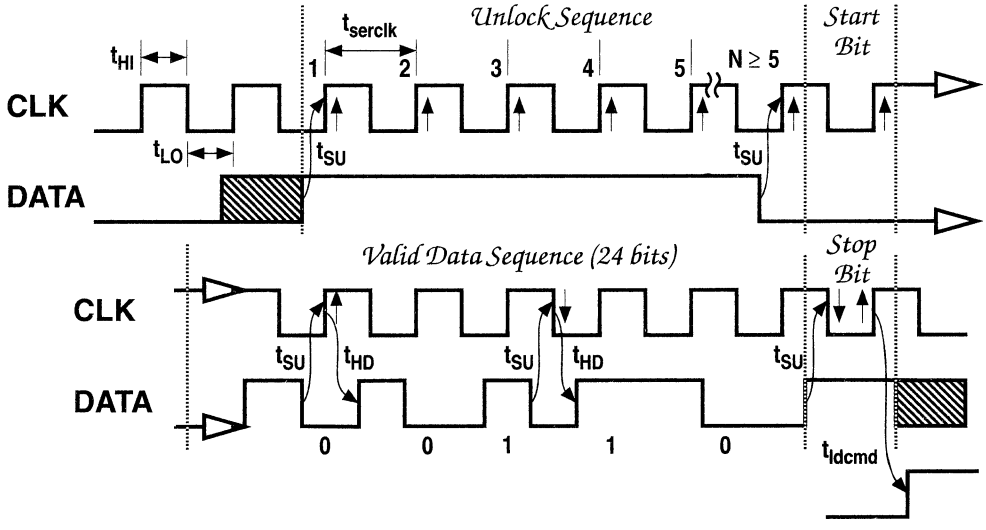


## Fig. 13: Soft Power-Down Timing (Mode 2)




* It takes 2–10 msec after Soft Power-Down to guarantee lock of VCLKOUT & MCLKOUT PLLs

## Fig. 14: Serial Programming Timing



# Revision History / Credits

V2.5 (11/15/93) — Final Release Version

# ICD2062B

## Dual Programmable ECL/TTL Clock Generator

**Single-Chip Dual Programmable Oscillator Handles All Frequency Requirements of High-Performance Graphic Systems**

- 2nd Generation Dual Oscillator Graphics Clock Generator
- PECL Video Outputs: 508 KHz–165 MHz
- TTL Outputs: 508 KHz–120 MHz
- Individually Programmable Oscillators Using a Highly Reliable Manchester-Encoded 21-Bit Serial Data Word
- 2-Pin Serial Programming Interface Allows Direct Connection to Most Graphics Chip Sets with no External Hardware Required
- Programmable Video Clock Dividers Allow for Easy Interface to most RAMDACs and VRAMs
- 3-State Oscillator Control Disables Outputs for Test Purposes
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Sophisticated Internal Loop-Filter Requires no External Components
- Low-Power, High-Speed, 5V CMOS Technology
- Available in 20-Pin SOIC Package Configuration

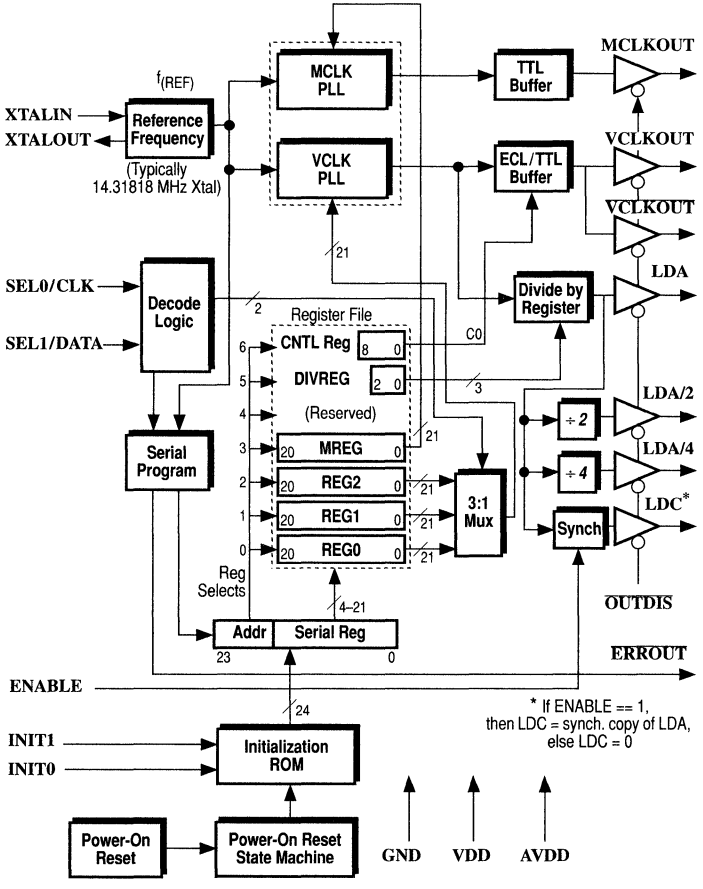



**Fig. 1: ICD2062B Block Diagram**

# Contents

## Figures



## Tables

# Introduction

The ICD2062B is a clock generator for high-resolution video displays. It uses a low-frequency (and low-cost) reference crystal to produce the following: a 10 KH compatible complementary ECL oscillator signal for high-speed video RAMDACs, a high-speed TTL oscillator signal for video RAMs and system logic operation, and the requisite load, control and clock signals to control the loading of data between the CRT controller, VRAM and RAMDACs.

The ICD2062B Dual Programmable Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value in the range 508 KHz to 165 MHz (VCLKOUT) and 508 KHz to 120 MHz (MCLKOUT). The ICD2062B is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators, particularly where the application requires expensive complementary ECL oscillators.

The Video Clock output may be programmatically divided — by 1, 2, 3, 4, 5 or 8 — in order to generate the Load Signal, which is further divided by 2 and 4 for clocking video timing logic. A second Load Signal may be synchronously gated in order to enable starting and stopping the clocking of video RAMs. The ICD2062B can also configure the pipeline delay of certain RAMDACs (such as the Bt457/458) to a fixed pipeline delay.

Being able to change the output frequency dynamically adds a new degree of freedom for the electrical engineer heretofore unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

## ICD2062A vs. ICD2062B

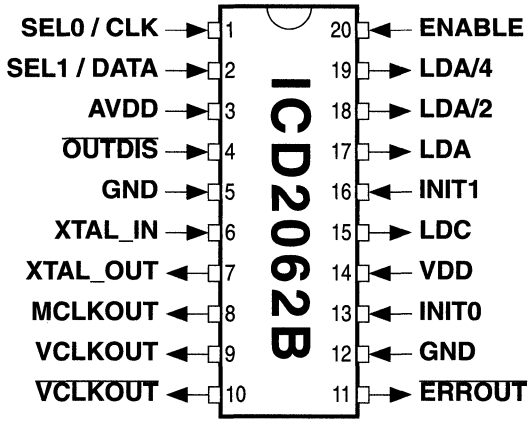
The ICD2062B revision of the ICD2062A is a complete mask redesign which includes feature enhancements as well as minor bug fixes. The following points detail the differences between the two versions:

The ICD2062B offers the following new features:

- **New VCO** — The primary difference between the A and B versions is the design of the internal VCO. The ICD2062B video VCO has been redesigned to support frequencies up to 165 MHz (see above);
- **Higher Upper Frequency Limit (VCLKOUT)** — 165 MHz;
- **New Register Initialization ROM** — A new ROM allows the ICD2062B to be initialized to higher default frequencies;
- **More Load Clock divisors** — the ICD2062B Load Clock divisors of 1, 2, 3, 4, 5 & 8.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions




## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | SEL0 / CLK | Bit 0 (LSB) of frequency select logic, used to select oscillator frequencies. Clock Input in serial programming mode. (Internal pull-down) |
| 2 | SEL1 / DATA | Bit 1 (MSB) of frequency select logic, used to select oscillator frequencies. Data Input in serial programming mode. (Internal pull-down) |
| 3 | AVDD | +5V to Analog Core |
| 4 | $\overline{\text{OUTDIS}}$ | Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation not required.) |
| 5 | GND | Ground |
| 6 | XTAL_IN | Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock signal may be used as input if available. |

## Table 1: Signal Descriptions (Continued)

| Pin # | Signal | Function |
|---|---|---|
| 7 | XTAL_OUT | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |
| 8 | MCLKOUT | Memory Clock out |
| 9 | VCLKOUT | Differential clock output. Connect directly to RAMDAC CLOCK inputs. Can drive 4 RAMDACs. |
| 10 | $\overline{\text{VCLKOUT}}$ | Output levels equivalent to 10 KH ECL circuit operating from single supply. $\overline{\text{VCLKOUT}}$ is skew-free. |
| 11 | $\overline{\text{ERROUT}}$ | Error Output: a low signals an error during serial programming. |
| 12 | GND | Ground |
| 13 | INIT0 | Select power-up initial conditions (LSB) (Internal pull-down) |
| 14 | VDD | +5V to I/O Ring |
| 15 | LDC | Load output (TTL compatible). When ENABLE is high, has same timing as LDA output. Can drive up to 4 capacitive loads without buffering. |
| 16 | INIT1 | Select power-up initial conditions (MSB) (Internal pull-down) |
| 17 | LDA | Skew-free Load Outputs (TTL compatible). Generated by dividing VCLKOUT by Div Register (1, 2, 3, 4, 5 or 8). Each output can drive up to 4 capacitive loads without buffering. |
| 18 | LDA/2 | Generated by dividing LDA by two |
| 19 | LDA/4 | Generated by dividing LDA by four. |
| 20 | ENABLE | Synchronous load enable input. Internally synched to LDA, used to start/stop LDC output synchronously. If ENABLE is low, LDC is held low; when high, LDC is free-running. |

# Register Definitions

## Register File

The Register File consists of the following registers and their selection addresses:

**Table 2: Register Addressing**

| Address | Register | Usage |
|---|---|---|
| 000 | REG0 | Video Clock Register 1 |
| 001 | REG1 | Video Clock Register 2 |
| 010 | REG2 | Video Clock Register 3 |
| 011 | MREG | Memory or I/O Timing Clock |
| 100 | (Reserved) | |
| 101 | DIVREG | Load Divisor Register |
| 110 | CNTL Reg | Control Register |

## Register Selection

Video clock output is controlled not only by the SEL0 & SEL1 bits, but also by the $\overline{\text{OUTDIS}}$ signal, as follows:

**Table 3: VCLKOUT Selection**

| $\overline{\text{OUTDIS}}$ | SEL1 | SEL0 | VCLKOUT |
|---|---|---|---|
| 0 | X | X | High-Z |
| 1 | 0 | 0 | REG0 |
| 1 | 0 | 1 | REG1 |
| 1 | 1 | X | REG2 |

The Memory Clock output is controlled by the $\overline{\text{OUTDIS}}$ signal as indicated below:

**Table 4: MCLKOUT Selection**

| $\overline{\text{OUTDIS}}$ | MCLKOUT |
|---|---|
| 0 | High-Z |
| 1 | MREG |

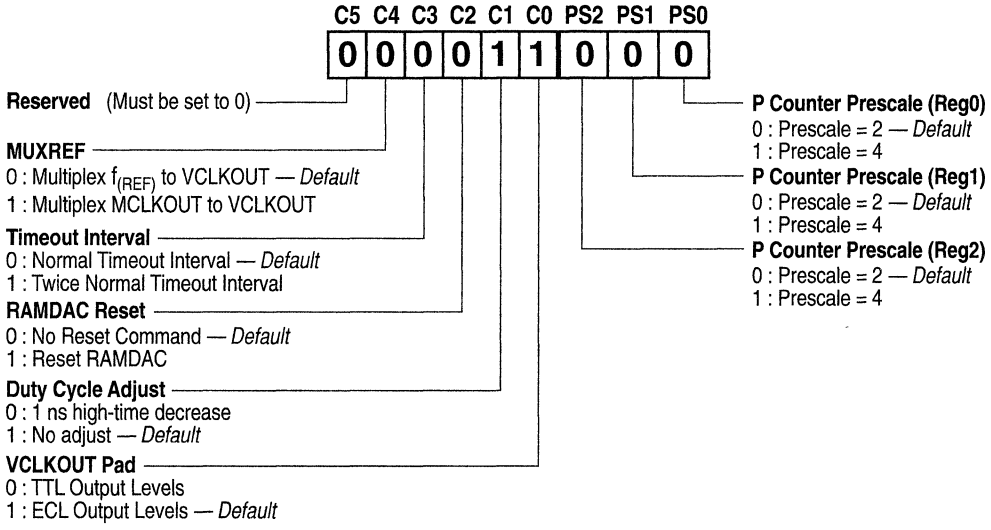
The Clock Select pins SEL0 & SEL1 have a dual purpose. When these pins are performing serial down-load, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins SEL0 & SEL1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f_{(REF)}$ for an additional timeout interval to give the VCO time to settle to its new value. (The timeout interval in both cases is approximately 5 msec — see the timeout interval spec in *Table 17: AC Characteristics* on page 189.)



When a new frequency is being set for MCLK, or if the active VCLK register is being programmed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent from the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See *Table 17: AC Characteristics* on page 189 for further details.).

## Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined as follows:




### Fig. 3: Control Register

**MUXREF** — This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphic controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

**Timeout Interval** — The Timeout Interval is normally defined as in *Table 17: AC Characteristics* on page 189. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, the timeout may be too short. If this control bit is set, the Timeout Interval is doubled.

**RAMDAC Reset** — This control bit, when set, will cause the ICD2062B to issue a RAMDAC reset sequence, which is required by some specific RAMDACs (such as the Bt457/458). For more specifics on this operation, refer to the Section *Internal RESET Sequence* on page 181. NOTE: This operation will only take place the first time this bit is set.

**Duty Cycle Adjust** — This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the Threshold Voltage $V_{TH}$ is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

**VCLKOUT Pad** — This control bit determines whether the VCLKOUT Pad is at ECL or TTL levels. The default is ECL levels. When in TTL mode, the $\overline{\text{VCLKOUT}}$ Pad is nonfunctional, and remains 3-stated.

**P Counter Prescale** (REG0, REG1, REG2) — These control bits determine whether or not to pre-scale the P Counter value, which allows "fine tuning" the output frequency of the respective register. Prescaling is explained in more detail elsewhere in this Datasheet.

## Divide Register Definition

The output signals LDA, LDA/2, LDA/4, and LDC are all a function of the VCLK VCO value divided by the division factor stored in the Divide Register (DIVREG). The maximum LDA & LDC output is 100 MHz.



### Table 5: DIVREG Division Factors

| D2 | D1 | D0 | Division Factor | Clock Low (cycles) | Clock High (cycles) | Device Version |
|---|---|---|---|---|---|---|
| 1 | 0 | X | ÷1 | 1/2 | 1/2 | A & B |
| 1 | 1 | X | ÷2 | 1 | 1 | A & B |
| 0 | 0 | 0 | ÷3 | 1 | 2 | B |
| 0 | 0 | 1 | ÷4 | 2 | 2 | B[a] |
| 0 | 1 | 0 | ÷5 | 2 | 3 | B |
| 0 | 1 | 1 | ÷8 | 4 | 4 | B |

a. Default on power-up

## Register Initialization

The ICD2062B Clock Synthesizer has several of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three pixel clock registers are initialized based on the state of the INIT1 and INIT0 pins at power-up. Also, the Memory Clock is initialized based on the INIT pins.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with VDD if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as follows:

### Table 6: Register Initialization

| INIT1 | INIT0 | MREG | REG0 | REG1 | REG2 |
|---|---|---|---|---|---|
| | | (Frequencies in MHz) | | | |
| 0 | 0 | 32.500 | 25.175 | 28.322 | 28.322 |
| 0 | 1 | 40.000 | 25.175 | 28.322 | 28.322 |
| 1 | 0 | 50.350 | 110.000 | 135.000 | 165.000 |
| 1 | 1 | 56.644 | 110.000 | 135.000 | 185.000 |

# Serial Programming Architecture

The ICD2062B programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual function of clock selection and serial programming. The Serial Program Block (See *Fig. 1: ICD2062B Block Diagram* on page 159) contains several components: a Serial Unlock Decoder (containing the Unlocking Mechanism and Manchester Decoder), a Watchdog Timer, the Serial Data Register (Serial Reg) and a Demultiplexer to the Register File.

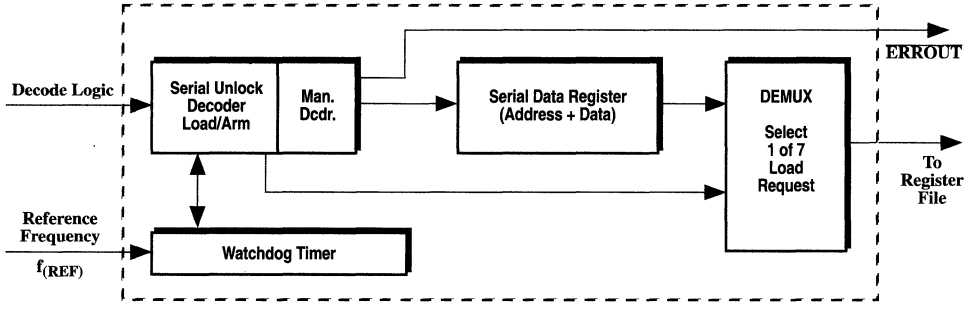



**Fig. 4: Serial Program Block Diagram — Detail**

## Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence detailed in the following timing diagram:

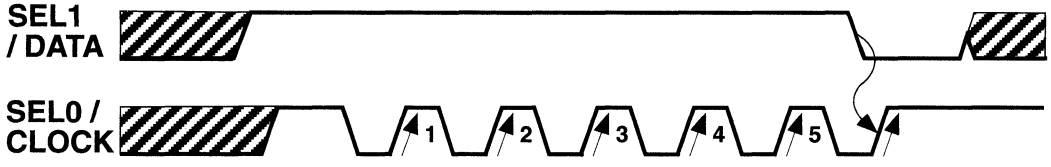



**Fig. 5: Unlock Sequence**

The initial unlock sequence consists of at least five low-to-high transitions of CLK with DATA high, followed immediately by a single low-to-high transition of CLK with DATA low. Following this unlock sequence, the encoded serial data is clocked into the Serial Data Register.

## Watchdog Timer

Following any transition of CLK or DATA, the Watchdog Timer is reset and begins counting. Throughout the entire programming process, the Watchdog Timer ensures that there is a transition on clock or data within the timeout specification (of 2 msec — see *Table 17: AC Characteristics* on page 189). If a timeout does occur, the Lock Mechanism is rearmed and the current data in the Serial Data Register is lost.

Since the VCLK registers are selected by the SEL0 or SEL1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of SEL0 or SEL1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. [Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.]

## The Serial Data Register

Serial data is clocked into the Serial Data Register in the following order:

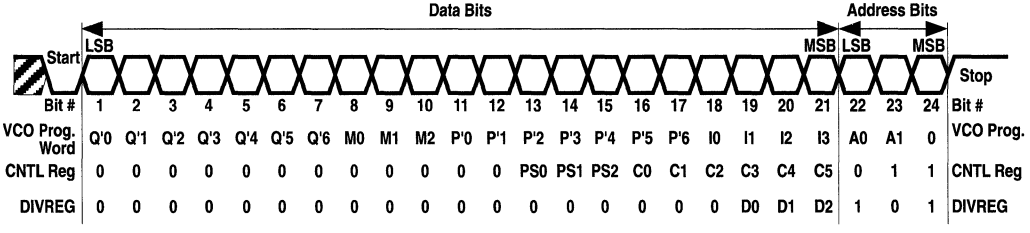



**Fig. 6: Serial Data Timing**

The serial data is sent using a modified Manchester encoded data format. This is defined as follows:

1 — An individual data bit is sampled on the rising edge of CLK.
2 — The complement of the data bit must be sampled on the previous falling edge of CLK.
3 — The Setup and Hold Time requirements must be met on both CLK edges.
4 — The unlock sequence, start, and stop bits are not Manchester encoded.

For specifics on timing, see *Fig. 18: Serial Programming Timing* on page 193.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10] = P'; D[9:7] = Mux; D[6:0] = Q'. [Refer to *Programming the ICD2062B* on page 174 for more details on the VCO data word.] For the other registers having fewer

than 21 bits (DIVREG, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last address bit, a stop bit or Load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The Unlocking Mechanism then automatically rearms itself following the load. Only when the Watchdog Timer has timed out are the SEL0 & SEL1 pins permitted to return to their normal clock select function.

Note that the Serial Data Register (Serial Reg) which receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command which passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Reg has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the Unlocking Mechanism rearmed, and an error issued. The device counts the serial data clock edges to know exactly when the Serial Buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the Unlocking Mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the Unlocking Mechanism is rearmed, the Serial Counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.



### $\overline{\text{ERROUT}}$ Operation

The $\overline{\text{ERROUT}}$ signal is used to announce when a program error has been detected internally by the ICD2062B. The signal remains low until the next unlock sequence.

The following circuit shows the basic mechanism used to detect erroneous serial data:

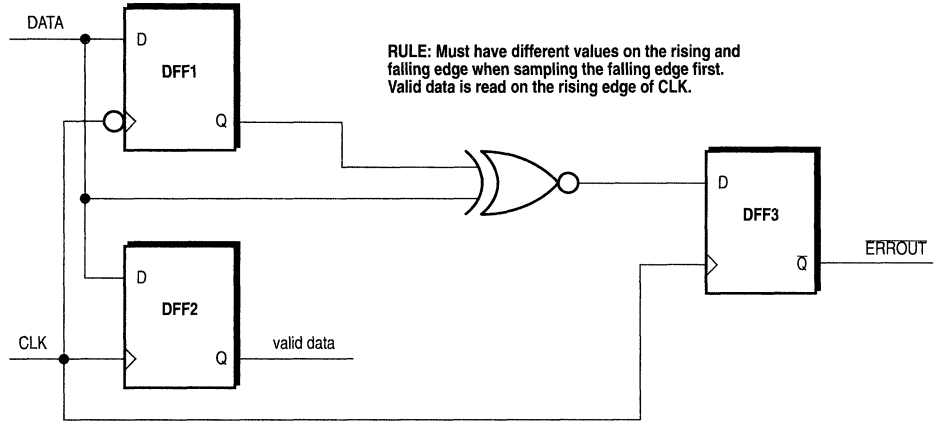



**Fig. 7: Modified Manchester Decoder Circuit**

The $\overline{\text{ERROUT}}$ signal is invoked for any of the following error conditions: incorrect start bit; incorrect Manchester encoding; incorrect length of data word; incorrect stop bit.

NOTE: If there is no input pin available on the target VGA controller chip to monitor $\overline{\text{ERROUT}}$, a software routine which counts VSYNC pulses to measure output frequency may be used as a determination of programming success.

# Programming the ICD2062B

The desired output frequency is defined via a serial interface, with a 21–bit number shifted in. The ICD2062B has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

## Table 7: Programming Word Bit Fields

| Field | # of Bits | Notes |
|---|---|---|
| Index (I) | 4 | MSB (Most Significant Bits) |
| P Counter value (P') | 7 | |
| Mux (M) | 3 | |
| Q Counter Value (Q') | 7 | LSB (Least Significant Bits) |

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 60 MHz; typically 14.31818 MHz).

NOTE: If a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of $f_{(VCO)}$ must remain between a minimum and maximum frequency. These limits vary depending on the clock (MCLK or VCLK). See *Table 10: Programming Constraints* on page 177 for the actual boundary frequencies in each case. For output frequencies below the minimum, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

**Table 8: Post-VCO Divisor**

| M | Divisor |
|---|---|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 100 | 16 |
| 101 | 32 |
| 110 | 64 |
| 111 | 128 |



The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from *Table 9: Index Field (I)* on page 176. (Note that this table is referenced to the VCO frequency, $f_{(VCO)}$, rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running. When the Index Field is programmed to **1111**, VCLK is turned off and both channels run from the same MCLK VCO.

When the Index Field is set to **1111**, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, one doesn't want the two VCOs to run at integral multiples of each other; therefore, if one does want the clocks to run at $2^n$ (n = 0, 1, 2 .. 7) multiples of each other, this is done by turning off the VCLK VCO and multiplexing the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

## Table 9: Index Field (I)

| I | VCLK $f_{VCO}$ (MHz) | MCLK $f_{VCO}$ (MHz) |
|---|---|---|
| 0000 | 65.0 – 70.7 | • Reserved • |
| 0001 | 70.7 – 77.8 | 52.0 – 55.0 |
| 0010 | 77.8 – 85.6 | 55.0 – 60.0 |
| 0011 | 85.6 – 88.0 | 60.0 – 68.0 |
| 0100 | 88.0 – 94.2 | 68.0 – 70.0 |
| 0101 | 94.2 – 96.8 | 70.0 – 75.0 |
| 0110 | 96.8 – 106.5 | 75.0 – 80.0 |
| 0111 | 106.5 – 111.7 | 80.0 – 84.5 |
| 1000 | 111.7 – 117.2 | 84.5 – 90.0 |
| 1001 | 117.2 – 122.8 | 90.0 – 95.0 |
| 1010 | 122.8 – 135.1 | 95.0 – 100.0 |
| 1011 | 135.1 – 148.6 | 100.0 – 104.0 |
| 1100 | 148.6 – 160.0 | 104.0 – 110.0 |
| 1101 | 160.0 – 165.0 | 110.0 – 120.0 |
| 1110 | Turn off VCLK | 110.0 – 120.0 |
| 1111 | Mux MCLK > VCLK | 110.0 – 120.0 |

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

## Programming Constraints

There are five primary programming constraints the user must be aware of:

**Table 10: Programming Constraints**

| Parameter | Minimum | Maximum |
|---|---|---|
| $f_{(REF)}$ | 1 MHz | 60 MHz |
| $f_{(REF)} \div Q$ | 200 KHz | 1 MHz |
| $f_{(VCO)}$ | VCLK: 65 MHz<br>MCLK: 52 MHz | VCLK: 165 MHz<br>MCLK: 120 MHz |
| Q | 3 | 129 |
| P | 4 | 130 |



The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the aforementioned ***BitCalc*** program, these constraints become transparent.

## Programming Example — Prescaling = 2 (default)

The following is an example of the calculations ***BitCalc*** performs:

For the ICD2062B, derive the proper programming word for a 39.5 MHz VCLK output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 52 MHz, double it to 79.0 MHz. Set M to **001**. Set I to **0010**. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

**Table 11: P & Q Value Pairs**

| P | Q | $f_{VCO}$ (MHz) | Error ( ppm ) |
|---|---|---|---|
| 69 | 25 | 79.0363 | 460 |
| 80 | 29 | 78.9969 | 40 |
| 91 | 33 | 78.9669 | 419 |

Choose (P, Q) = (80,29) for best accuracy (40 ppm).

Therefore:

$$\mathbf{P' = P-3 = 80-3 = 77 = 1001101}\ (4dH)$$

$$\mathbf{Q' = Q-2 = 29-2 = 27 = 0011011}\ (1bH)$$

and the full programming word, W, is:

$$\mathbf{W = I, P', M, Q' = 0010,1001101,001,0011011 = 00101001101001011011}\ (05349bH)$$

The programming word W is then sent as a serial bit stream, LSB first. Appropriate address bits and start & stop bits must also be included as defined in the section *Serial Programming Architecture* on page 171.

## Programming Example — Prescaling = 4

Assume the desired VCLKOUT frequency is 100 MHz. The table below compares the results of using the default prescaling value of 2 and the optional prescaling value of 4:

**Table 12: Prescale Values**

| Prescale | Actual Frequency (MHz) | P | Q | Error ( ppm ) |
|---|---|---|---|---|
| 2 | 99.84028 | 129 | 37 | 1600 |
| 4 | 99.99998 | 110 | 63 | 0 |

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2) — which involves loading a Control Word (taking care to preserve the current values of the other Control Bits) — before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1.Set the Prescale Bits (load a Control Word)

2.Program the VCO (load a Program Word)

Note: Care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

# RAMDAC/VRAM Interface

## Interfacing to the RAMDAC

The figure below shows how to interface the ICD2062B to a RAMDAC. The part should be located as close to the RAMDAC as possible. Termination resistors are needed on the VCLKOUT outputs, and should be located as close as possible to the RAMDAC. For specific information, please refer to the IC DESIGNS Application Note *ECL Outputs* on page 289.

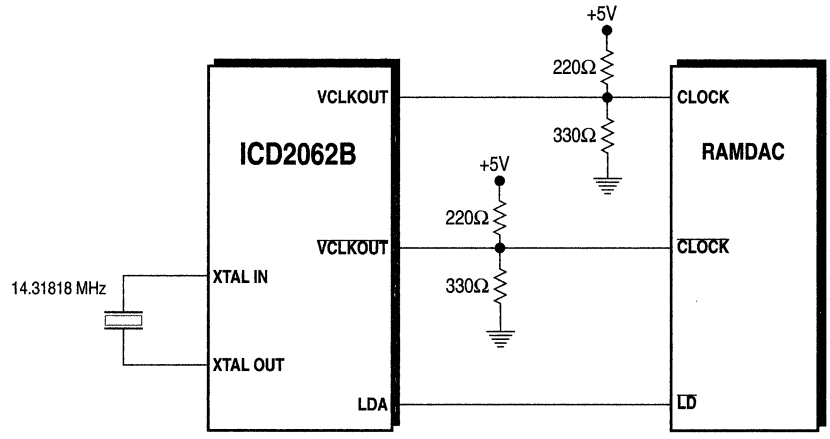



**Fig. 8: ICD2062B to RAMDAC Interface Example**

The ICD2062B may drive the CLOCK inputs of up to four RAMDACs, if they are located physically adjacent to each other. In this case, only 2 sets of termination resistors should be used, and these should be located nearest the farthest RAMDAC from the ICD2062B.

## Typical ICD2062B Usage

The DIVREG Register holds the divisor, which can be 1, 2, 3, 4, 5 or 8, by which the pixel clock is divided to generate the load signals: LDA, LDA/2 and LDA/4.

The ENABLE input is synchronized internally to LDA; it may be used to start and stop the LDC output synchronously. When ENABLE is low, LDC is held low. When ENABLE is high, then LDC will be free-running and in phase with LDA. This allows the video DRAM shift registers to be non-clocked during the retrace intervals.

NOTE: For fanouts > 4, LDC needs to be buffered.

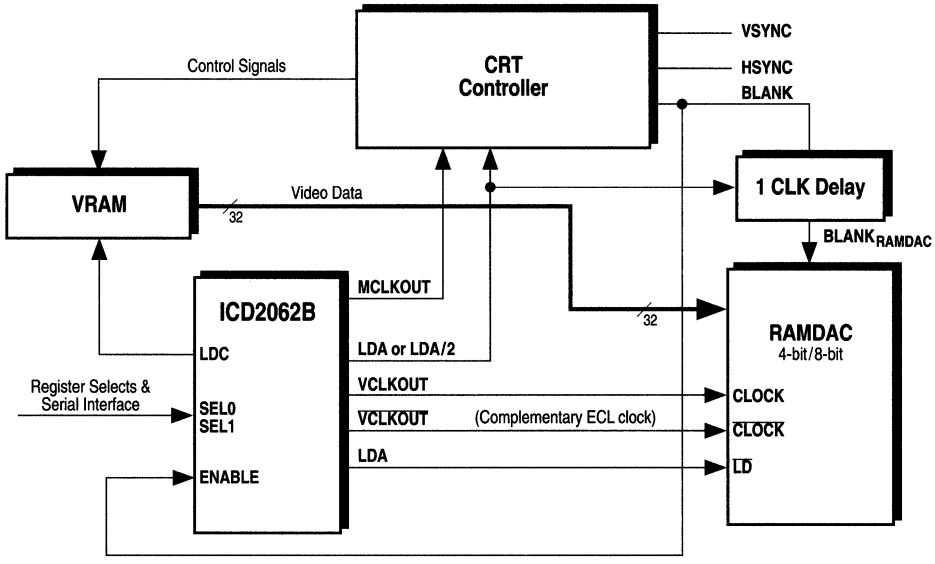



**Fig. 9: ICD2062B Typical Interface Circuit**

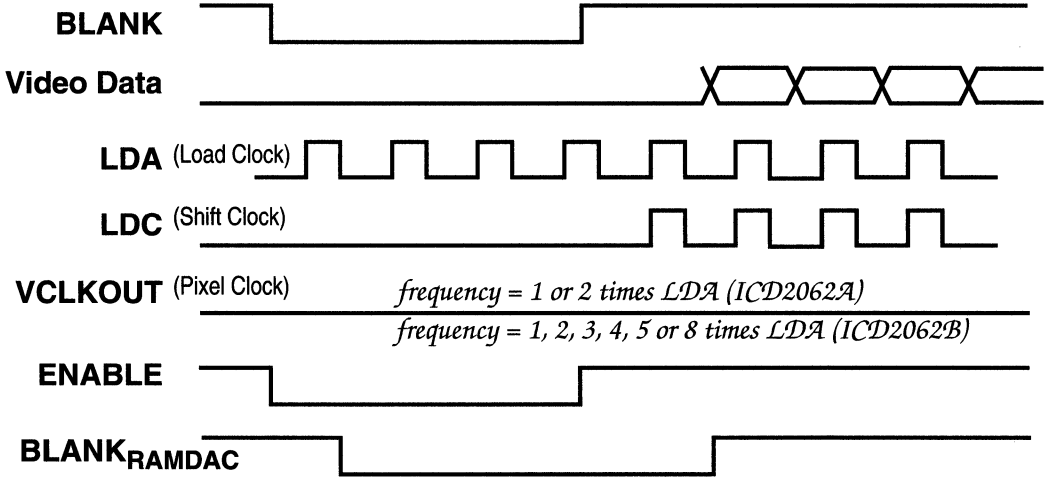



**Fig. 10: Timing Diagram for Interface Circuit**

## Internal RESET Sequence

The internal RESET signal allows the ICD2062B to set the RAMDAC pipeline delay to a specific cycle count, depending on the RAMDAC. Reset takes place the first time the CNTL Register's Reset Bit is set. Following the rising edge of LDA/4 after the Reset Bit is set, the VCLKOUT and $\overline{\text{VCLKOUT}}$ outputs are stopped high and low, respectively; at the next rising edge of LDA/4, these outputs are again allowed to be free-running. The figure below shows the operation of the internal RESET signal:

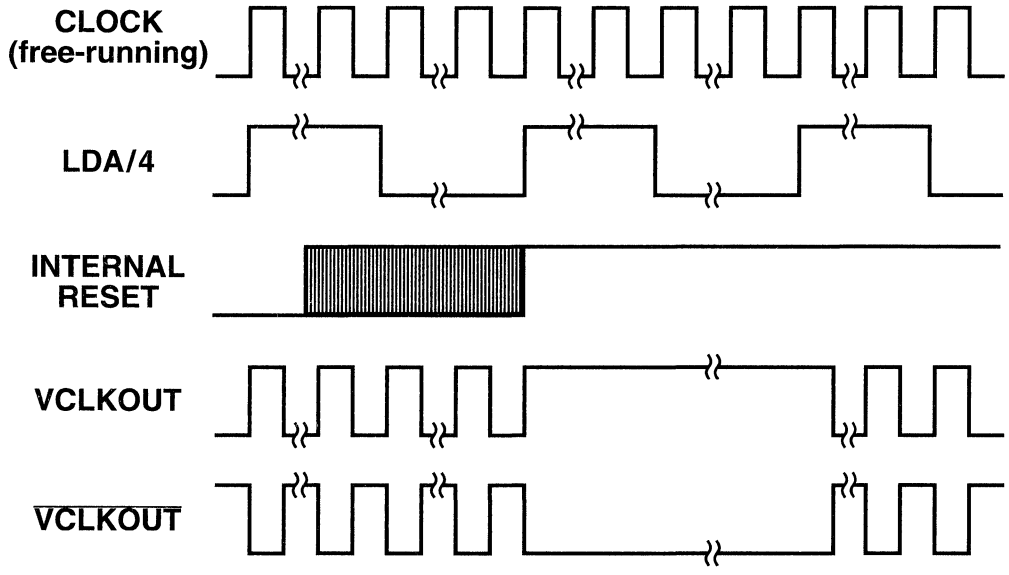



**Fig. 11: Internal RESET Timing**

# Power Management Issues

## Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: I = C • V • f, where:

I = current,

C = load capacitance (max. 25pF),

V = output voltage (usually 5V for TTL pads, 1.5V for ECL pads), and

f = output frequency (in MHz).

To calculate total operating current, sum the following:

| | | |
|---|---|---|
| MCLKOUT | ⇒ | $C \cdot V \cdot f_{(MCLKOUT)}$ |
| VCLKOUT | ⇒ | $C \cdot V \cdot f_{(VCLKOUT)}$; (ECL pad, V = 1.5V) |
| $\overline{\text{VCLKOUT}}$ | ⇒ | $C \cdot V \cdot f_{(\overline{VCLKOUT})}$; (ECL pad, V = 1.5V) |
| LDA | ⇒ | $C \cdot V \cdot f_{(LDA)}$ |
| LDA/2 | ⇒ | $C \cdot V \cdot f_{(LDA/2)}$ |
| LDA/4 | ⇒ | $C \cdot V \cdot f_{(LDA/4)}$ |
| LDC | ⇒ | $C \cdot V \cdot f_{(LDC)}$ |
| Internal | ⇒ | 12 mA |

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on package type.

Typical values:

**Table 13: Typical Current Drain Values**

| Frequency | Capacitive Load | Current ( mA ) |
|---|---|---|
| low | low | 15 |
| high | low | 50 |
| high | high | 100 |

# Circuit Operation

## Circuit Description

The ICD2062B is designed to use an inexpensive TTL crystal and to generate the high-frequency ECL clock signals required by RAMDACs. The VCLKOUT and $\overline{\text{VCLKOUT}}$ signals interface directly with the RAMDAC CLOCK and $\overline{\text{CLOCK}}$ inputs. Output levels of the complementary ECL pads are compatible with 10 KH ECL circuitry operating from a single +5V power supply.

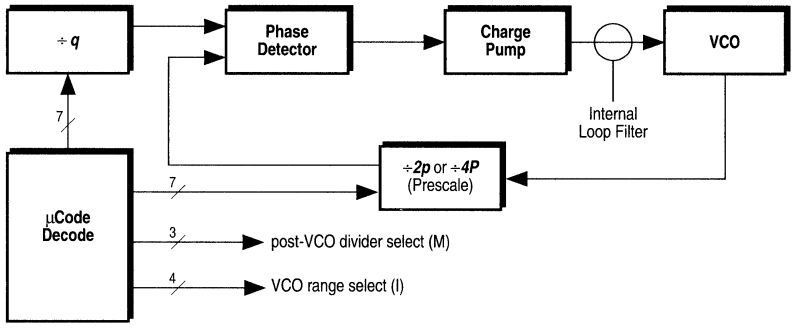



**Fig. 12: Phase-Locked Loop Oscillator**

Each oscillator block is a classical phase-locked loop connected as shown above. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

## Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphic designs.

## Frequency Range

The frequency ranges for the video and memory clock outputs are as follows:

VCLKOUT: 508 KHz – 185 MHz

MCLKOUT: 508 KHz – 120 MHz

## Output Disable

When the $\overline{\text{OUTDIS}}$ pin is asserted (active low), all the output pins except XTAL OUT and $\overline{\text{ERROUT}}$ enter a high impedance mode, to support automated board testing.

# PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. For optimum noise immunity, it is highly recommended that the ICD2062B be used with a voltage regulator or Zener diode attached to the AVDD line. A less expensive (and less effective) alternative is to utilize an RC power filter as follows: the analog power pin (AVDD) is bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281 for more details and for illustrative schematics.



The designer should also avoid routing any of the output traces of the IC DESIGNS in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2062B closest to the device requiring the highest frequency.

## FCC & Noise issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note *Minimizing Radio Frequency Emissions* on page 285.

## ECL Design Issues

Please refer to the IC DESIGNS Application Note *ECL Outputs* on page 289.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on opposite sides of the die. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2062B is inherently stable over temperature, voltage and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2062B, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

# Ordering Information

## Table 14: Order Codes

| Part Number | Package Type | Temperature Range | Speed Options |
|---|---|---|---|
| **ICD2062B** | S = 20-Pin SOIC DIP | C = Commercial[a] | –1: 135 MHz<br>–2: 165 MHz |

a. 0°C to +70°C



Example: order ICD2062BSC-2 for the ICD2062B, 20–pin plastic SOIC, commercial temperature range device with a top Video Clock frequency range of 165 MHz.

# Device Specifications

## Electrical Data

### Table 15: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 790 / 1050 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 16: DC Characteristics

| Name | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2.0 | | | Volts | |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | Volts | |
| $V_{OH(ECL)}$ | ECL High-level output[a] | $V_{DD}$ – 1.0 | | $V_{DD}$ – 0.8 | Volts | |
| $V_{OL(ECL)}$ | ECL Low-level output | $V_{DD}$ – 2.0 | | $V_{DD}$ – 1.6 | Volts | |
| $V_{OH(TTL)}$ | TTL High-level output[b] | 2.4 | | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL(TTL)}$ | TTL Low-level output | | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $I_{IH}$ | Input high current | | | 150 | µA | $V_{IH}$ = 5.25V |
| $I_{IL}$ | Input low current | | | –250 | µA | $V_{IL}$ = 0V |
| $I_{OZ}$ | Output leakage current | | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | 15 | | 150 / 200 | mA | A / B |
| $I_{DD-TYP}$ | Power supply current (typical) | | 45 | | mA | @ 60 MHz |
| $C_{OUT(ECL)}$ | ECL Output Capacitance | | | 10 | pF | |

a. ECL outputs: VCLKOUT, $\overline{\text{VCLKOUT}}$
b. TTL outputs: MCLKOUT, LDA, LDA/2, LDA/4, LDC, $\overline{\text{ERROUT}}$

## Table 17: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value (Note: for references of other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.) | 1 | 14.318 | 60 | MHz |
| $t_{(REF)}$ | reference clock period | $1 \div f_{(REF)}$ | 16.6 | | 1000 | ns |
| $t_1$ | input duty cycle | Duty cycle for the input oscillator defined as $t_1 \div t_{(REF)}$ | 25% | 50% | 75% | |
| $t_2$ | output clock periods | Output oscillator values – ECL – | 6.1<br>165 MHz | | 1970<br>508 KHz | ns |
| | | – TTL – | 8.3<br>120 MHz | | 1970<br>508 KHz | |
| $t_3$ | output duty cycle | Duty cycle for the output oscillators (NOTE: for non-ECL outputs, the duty cycle is measured at CMOS threshold levels. At 5V, $V_{TH}$ = 2.5V.) | 40% | | 60% | |
| $t_4$ | rise times | Rise time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_5$ | fall times | Fall time for the output oscillators into a 25pF load | | | 3 | ns |
| $t_{skew\text{-}ECL}$ | | Skew between the VCLKOUT complementary outputs | | | 1 | ns |
| $t_{freq1}$ | freq1 output | Old frequency output | | | | |
| $t_{freq2}$ | freq2 output | New frequency output | | | | |
| $t_A$ | $f_{(REF)}$ mux time | Time clock output remains high while output muxes to reference frequency | $\frac{t_{(REF)}}{2}$ | | $3\frac{t_{(REF)}}{2}$ | |
| $t_{timeout}$ | timeout interval | Internal interval for serial programming and for VCO changes to settle. If the interval is too short, see the timeout interval section in the control register definition. | 2 | 5 | 10 | msec |
| $t_B$ | $t_{freq2}$ mux time | Time clock output remains high while output muxes to new frequency value | $\frac{t_{freq2}}{2}$ | | $3\frac{t_{freq2}}{2}$ | |
| $t_6$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{OUTDIS}$ signal assertion | 0 | | 12 | ns |
| $t_7$ | clk valid | Time for the output oscillators to recover from 3-state mode after $\overline{OUTDIS}$ signal goes high | 0 | | 12 | ns |

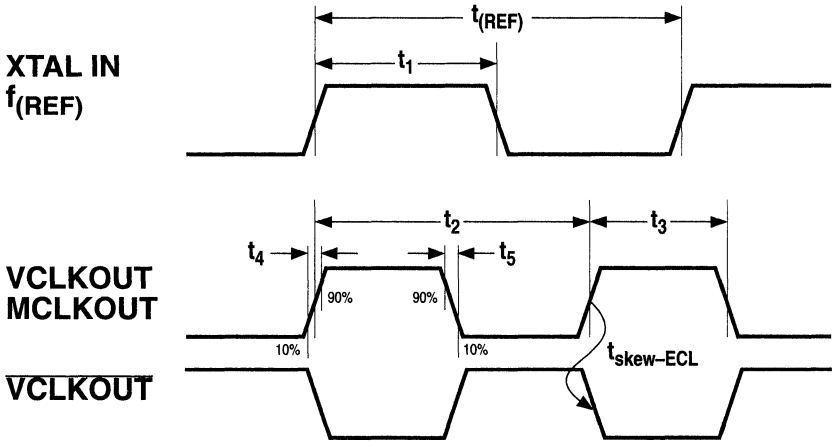
## Table 17: AC Characteristics (Continued)

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{LD}$ | Load Clock period | Maximum LDA & LDC period | 10 | | | ns |
| $t_{SKEW-LDA}$ | | VCLKOUT to LDA output skew | 2 | | 6 | ns |
| $t_{SKEW-LDA/2}$ | | LDA to LDA/2 output skew | 0 | 1 | 2 | ns |
| $t_{SKEW-LDA/4}$ | | LDA to LDA/4 output skew | 0 | 1 | 2 | ns |
| $t_{SKEW-LDC}$ | | LDA to LDC output skew | 0 | 1 | 2 | ns |
| $t_{EN-SU}$ | | ENABLE setup time to LDA | 12 | | | ns |
| $t_{EN-HD}$ | | ENABLE hold time to LDA | 0 | | | ns |
| $t_{serclk}$ | | Clock period of serial clock | $2 \cdot t_{(REF)}$ | | 2 | msec |
| $t_{HI}$ | | Minimum high time of serial clock | $t_{(REF)}$ | | | ns |
| $t_{LO}$ | | Minimum low time of serial clock | $t_{(REF)}$ | | | ns |
| $t_{SU}$ | | Setup time | 20 | | | ns |
| $t_{HD}$ | | Hold time | 10 | | | ns |
| $t_{ldcmd}$ | | Load command | 0 | | $t_1 + 30$ | ns |

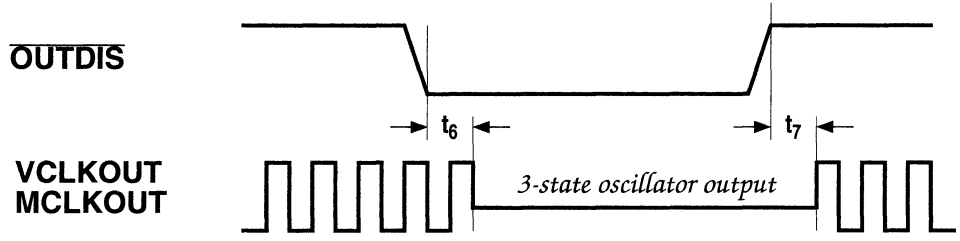
**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

## Timing Diagrams

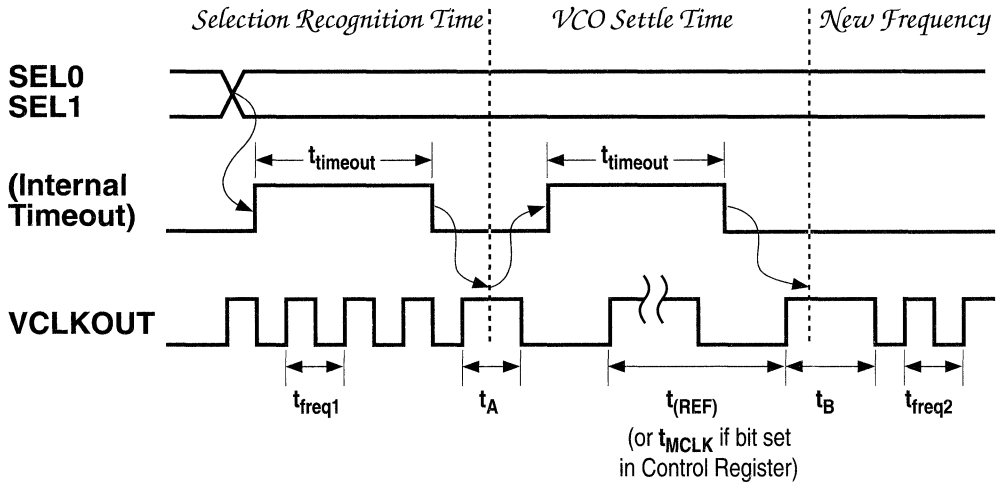
### Fig. 13: Rise and Fall Times



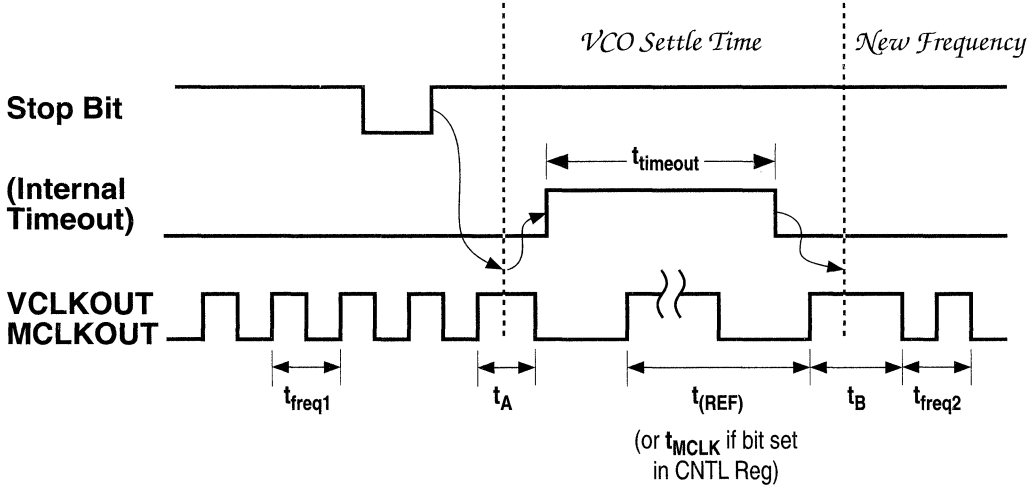

### Fig. 14: 3-State Timing



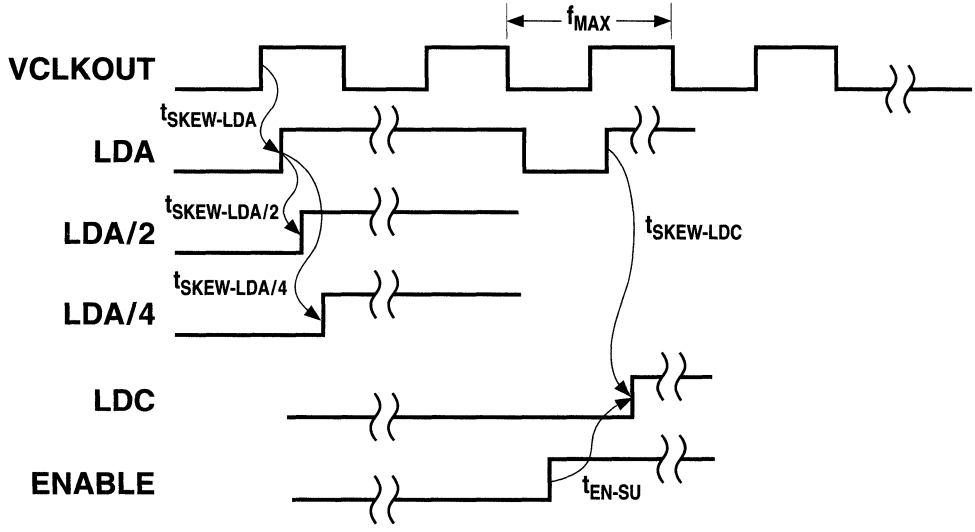
## Fig. 15: Selection Timing



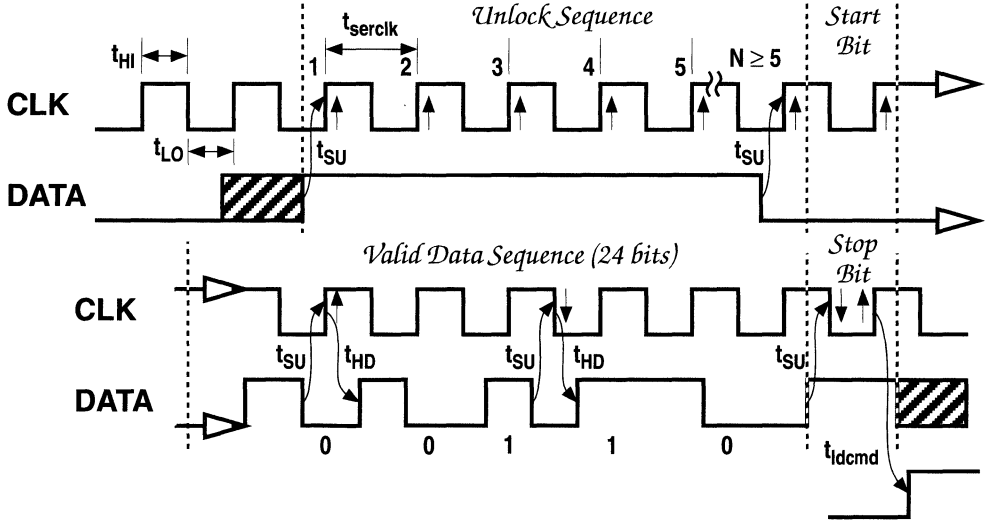

## Fig. 16: MCLK & Active VCLK Register Programming Timing



## Fig. 17: RAMDAC / VRAM Interface Timing




## Fig. 18: Serial Programming Timing



# Revision History / Credits

V2.6 (11/15/93) — Final Release Version

# ICD2063

## Programmable Graphics Clock Generator

**3.3V/5V Single-Chip Dual Programmable Oscillator Handles All Frequency Requirements of Popular Graphics Chip Sets**

- 2nd Generation Dual Oscillator Graphics Clock Generator
- Compatible with the ICD2061A
- 2 Independent Clock Outputs:
  VCLK Output —
  390 KHz – 135 MHz
  (100 MHz — 3.3V)
  MCLK Output —
  312 KHz – 100 MHz
  (80 MHz — 3.3V)
- Individually Programmable Oscillators Using a Highly Reliable Manchester-Encoded 21-Bit Serial Data Word
- 2-Pin Serial Programming Interface Allows Direct Connection to most Graphics Chip Sets with no External Hardware Required
- 2 Advanced Power-Down Capabilities
- 3-State Oscillator Control Disables Outputs for Test Purposes
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- 3.3V & 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 16-Pin SOIC Package Configuration

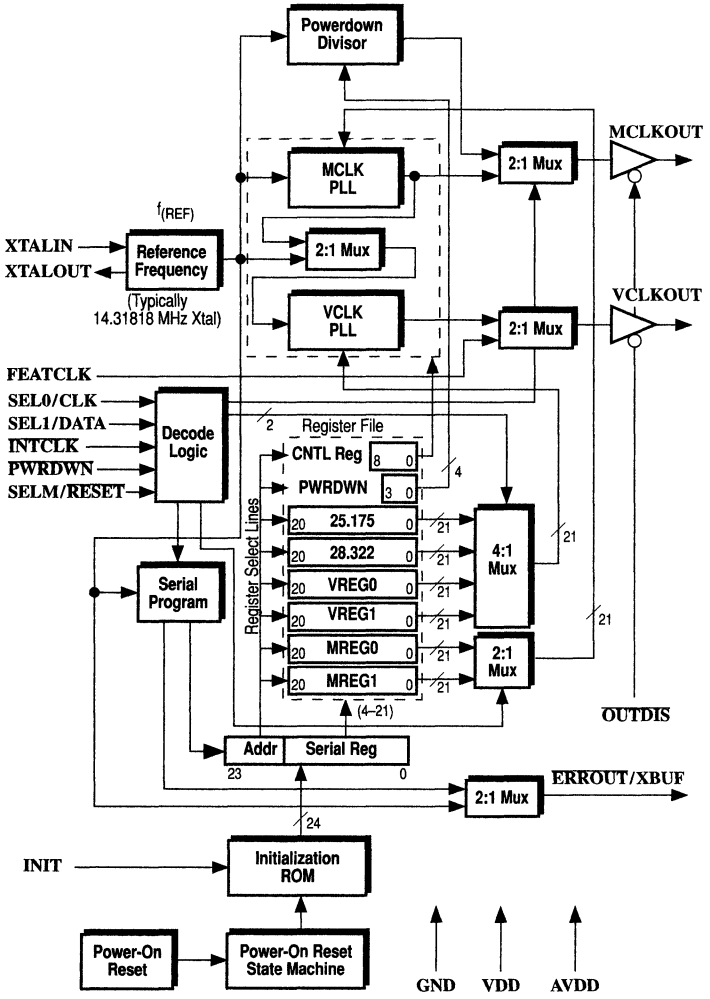



**Fig. 1: ICD2063 Block Diagram**

# Contents

## Figures



## Tables

# Introduction

The ICD2063 Dual Programmable Graphics Clock Generator features a fully programmable set of clock oscillators which can handle all frequency requirements of most graphics systems. The ICD2063 offers the selection ease of ROM-based clock chips, while also offering the versatility of serial programmed frequency synthesizers. It features both 3.3V & 5V operation with advanced power-down capabilities, making it ideally suited for the portable computer market. The ICD2063 has extended frequency range and improved voltage/temperature stability when compared to first-generation frequency synthesizers.

The ICD2063 Dual Programmable Graphics Clock Generator offers 2 fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between limits which depend on selected modes and operating voltage. The ICD2063 is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators or less functional ROM-based clock synthesizers.

While primarily designed for the graphics subsystem market, the programming versatility of the ICD2063 makes it ideal wherever two variable, yet highly accurate, clock sources are required.

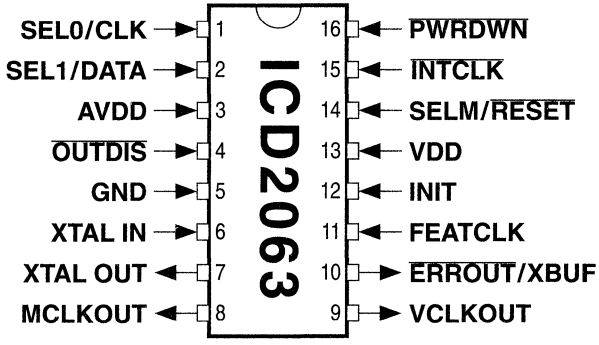
## ICD2063 Changes from the ICD2061A

The ICD2063 revision of the ICD2061A is a complete mask redesign which includes many feature enhancements. The following major modifications have been implemented:

- **3.3V Operation** — The ICD2063 supports 3.3V operation in addition to 5V operation.
- **Expanded Register Set** — There are now 4 Video Registers and 2 Memory Registers. This allows better support for Windows NT drivers.
- **Expanded VCO range** — The upper frequency limit has been increased to 135 MHz.
- **No Index Field Required** — The Serial Word now treats the Index Field (Mode Field) as a "Don't Care" bit region, for complete software compatibility with the ICD2061A.
- **Buffered Crystal Output** (Optional) — XBUF Output may be specified, replacing the ERROUT signal.
- **Smooth Frequency Transition** — the two phase-locked loops now transition smoothly from one frequency to another.
- **No MUXREF Required** — The necessity for the MUXREF procedure has been eliminated by the smooth frequency transition. For compatibility with the ICD2061A, there is an option which multiplexes a known output during frequency transitions. New to the ICD2063 is that the VCLK VCO is muxed to the MCLK output. See *MUXREF Option* on page 223 for details.
- **Virtually Infinite Frequency Resolution** — The MCLK Phase-Locked Loop Output can be multiplexed to the VCLK PLL Reference Input, thus enabling virtually infinite frequency resolution, at the expense of slightly higher jitter specification. See *Extended VCLK Frequency Precision* on page 214
- **Reduced Register Initialization ROM** — The former INIT2 pin now selects between the 2 memory registers MREG0 & MREG1.
- **Hardware Reset** (Optional) — A hardware reset is available as an option, replacing the memory selection signal.
- **Cascade Option with ICD2029** — This is the most comprehensive clock solution for portable computers available today.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions




## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | SEL0/CLK | Bit 0 (LSB) of frequency select logic, used to select oscillator frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.) |
| 2 | SEL1/DATA | Bit 1 of frequency select logic, used to select oscillator frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.) |
| 3 | AVDD | +5V or 3.3V to Analog Core |
| 4 | $\overline{\text{OUTDIS}}$ | Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect.) |
| 5 | GND | Ground |
| 6 | XTAL IN | Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock signal may be used as input if available. (For more specifics on crystal requirements, please refer to the IC DESIGNS Application Note *Externally Driven Crystal Oscillator* on page 295.) |
| 7 | XTAL OUT | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.) |

## Table 1: Signal Descriptions (Continued)

| Pin # | Signal | Function |
|---|---|---|
| 8 | MCLKOUT | Memory Clock output |
| 9 | VCLKOUT | Video Clock output |
| 10 | $\overline{\text{ERROUT}}$/ XBUF | Error Output: a low signals an error in the Serial Programming Word –OR– Buffered Crystal Reference Output (selectable via configuration option) |
| 11 | FEATCLK | External clock input (Feature Clock) (Internal pull-up allows no-connect.) |
| 12 | INIT | Selects state of initialization ROM during power-up. See *Table 3: Register Initialization ROM* on page 203. (This pin has no internal pull-up or pull-down: it must be tied high or low externally.) |
| 13 | VDD | +5V or 3.3V to I/O Ring |
| 14 | SELM/$\overline{\text{RESET}}$ | Selectable via configuration option:<br>SELM — Selects 1 of 2 Memory Clock Output (MCLKOUT) frequencies (See *Register Selection* subsection *MCLKOUT* on page 204.)<br>$\overline{\text{RESET}}$ — Hardware RESET control signal (See *Power-On Reset, RESET and Register Initialization* on page 202.) |
| 15 | $\overline{\text{INTCLK}}$ | Selects the Feature Clock external clock input as VCLKOUT output. (Internal pull-up allows no-connect.) (See *Table 4: VCLKOUT Selection* on page 203.) |
| 16 | $\overline{\text{PWRDWN}}$ | Power-down pin (active low) (Internal pull-up allows no-connect if power-down operation not required. See *Power Management Issues* on page 215 for specific details concerning the use of this pin.) |

# Register Definitions

## Register File

The Register File consists of the following registers and their respective addresses in the Serial Data Register:

**Table 2: Register Addressing**

| A2 | A1 | A0 | Register | Usage |
|---|---|---|---|---|
| 0 | 0 | 0 | 25.175 MHz | Fixed Video Clock Frequency |
| 0 | 0 | 1 | 28.322 MHz | Fixed Video Clock Frequency |
| 0 | 1 | 0 | VREG0 | Programmable Video Clock Register 0 |
| 0 | 1 | 1 | MREG0 | Programmable Memory Clock Register 0 |
| 1 | 0 | 0 | PWRDWN | Divisor for Power-Down mode |
| 1 | 0 | 1 | VREG1 | Programmable Video Clock Register 1 |
| 1 | 1 | 0 | CNTL | Control Register |
| 1 | 1 | 1 | MREG1 | Programmable Memory Clock Register 1 |

All register values are preserved in power-down mode.

## Power-On Reset, $\overline{\text{RESET}}$ and Register Initialization

The ICD2063 Clock Synthesizer initializes all of its registers to a known state upon power-up. This is implemented by the Power-On initialization circuitry. Two Video Clock registers and two Memory Clock registers are initialized based on the state of the INIT pin at power-up.

The Power-On Reset Function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pin must be strapped to VDD or GND.

If the $\overline{\text{RESET}}$ option on pin 14 is chosen, then this pin, when pulled low, forces the equivalent of a Power-On Reset operation: the registers are reloaded with the contents of the initialization ROM (depending on the state of the INIT pin).

The various registers are initialized as follows:

**Table 3: Register Initialization ROM**

| INIT Pin | 25.175 | 28.322 | VREG0 | VREG1 | MREG0 | MREG1 |
|---|---|---|---|---|---|---|
| | (Frequencies in MHz) | | | | | |
| 0 | 25.175 | 28.322 | 36.000 | 44.900 | 40.000 | 40.000 |
| 1 | 25.175 | 28.322 | 40.000 | 65.000 | 45.000 | 45.000 |

## Register Selection

### VCLKOUT



The Video Clock output is controlled not only by the SEL0, SEL1 and $\overline{\text{INTCLK}}$ pins, but also by the $\overline{\text{PWRDWN}}$ and $\overline{\text{OUTDIS}}$ signals. Additionally, the Clock Synthesizer may be multiplexed with an external frequency input (FEATCLK) which corresponds to the IBM VGA Feature Clock standard. The table below shows the VCLKOUT selection criteria:

**Table 4: VCLKOUT Selection**

| $\overline{\text{OUTDIS}}$ | $\overline{\text{PWRDWN}}$ | $\overline{\text{INTCLK}}$ | SEL1 | SEL0 | VCLKOUT |
|---|---|---|---|---|---|
| 0 | X | X | X | X | High-Z |
| 1 | 0 | X | X | X | Forced Low |
| 1 | 1 | X | 0 | 0 | 25.175 MHz |
| 1 | 1 | X | 0 | 1 | 28.322 MHz |
| 1 | 1 | 0 | 1 | 0 | FEATCLK |
| 1 | 1 | 1 | 1 | 0 | VREG0 |
| 1 | 1 | X | 1 | 1 | VREG1 |

The Clock Select pins SEL0 & SEL1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins SEL0 & SEL1 are functioning as register selects, a timeout interval is required to determine whether the user desires register selection or serial programming. At the end of the timeout interval — and if serial programming was not started — new register selection occurs, at which point the frequency changes to the new value. See the section *Serial Programming Architecture* on page 206 for selection & transition details.

### MCLKOUT

The Memory Clock output (MCLKOUT) is selected by PWRDWN, OUTDIS and by — depending on which configuration is chosen — either the SELM input or the SEL0 & SEL1 inputs, as shown in the following two tables.

If the Memory Select option on pin 14 is chosen, then the SELM input is available to set MCLKOUT, and the decode is defined as follows:

**Table 5: MCLKOUT Selection (Memory Select Mode)**

| OUTDIS | PWRDWN | SELM | MCLKOUT |
|---|---|---|---|
| 0 | X | X | High-Z |
| 1 | 0 | X | PWRDWN or low (depending on mode) |
| 1 | 1 | 0 | MREG0 |
| 1 | 1 | 1 | MREG1 |

If the RESET option is chosen, then MCLKOUT and VCLKOUT are both selected using the SEL0 & SEL1 pins (MREG1 can *only* be selected when VREG1 is selected):

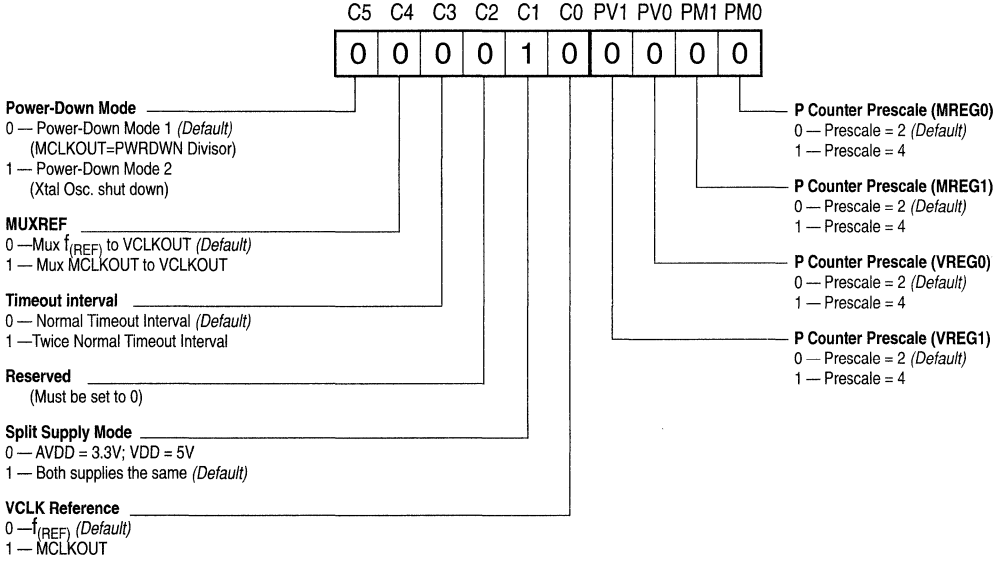
**Table 6: MCLKOUT Selection (Reset Mode)**

| OUTDIS | PWRDWN | INTCLK | SEL1 | SEL0 | VCLKOUT | MCLKOUT |
|---|---|---|---|---|---|---|
| 0 | X | X | X | X | High-Z | High-Z |
| 1 | 0 | X | X | X | Forced Low | PWRDWN or low (depending on mode) |
| 1 | 1 | X | 0 | 0 | 25.175 MHz | MREG0 |
| 1 | 1 | X | 0 | 1 | 28.322 MHz | MREG0 |
| 1 | 1 | 0 | 1 | 0 | FEATCLK | MREG0 |
| 1 | 1 | 1 | 1 | 0 | VREG0 | MREG0 |
| 1 | 1 | X | 1 | 1 | VREG1 | MREG1 |

See the section *Frequency Transition Options* on page 221 for more specifics.

## Control Register Definition

The Control Register (CNTL) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined as follows:




## Fig. 3: Control Register

**VCLK Reference** — This control bit determines whether the VCLK VCO uses $f_{(REF)}$ or the MCLK output as a reference. Refer to *Extended VCLK Frequency Precision* on page 214 for more details.

**Split Supply Mode** — This control bit allows mixing 3.3V (AVDD) and 5V (VDD) supplies. The default is for both to be the same (5V or 3.3V). The alternative is: AVDD = 3.3V, VDD = 5V. See *3.3 Volt & 5 Volt Issues* on page 218 for more details. The purpose is to maintain duty cycle at 50%.

**Timeout Interval** — The Timeout Interval is normally defined as in *Table 22: AC Characteristics* on page 231. It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the Timeout Interval is doubled.

**MUXREF (MUXREF Mode only)** — This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to use $f_{(REF)}$, but some graphic controllers cannot run that slow. This bit, when set, allows MCLK to be used as an alternative frequency.

**Power-Down Mode** — This control bit determines which Power-Down Mode the $\overline{\text{PWRDWN}}$ pin will implement. The default (Power-Down Mode 1) forces the MCLKOUT signal to be a function of the PWRDWN register. Power-Down Mode 2 turns off the crystal oscillator and disables all outputs. There is a more detailed description in the section *Power Management Issues* on page 215.

**P Counter Prescale** (VREG0, VREG1, MREG0, MREG1) — These control bits determine whether or not to prescale the P Counter value, which allows "fine tuning" the output frequency of the respective register. Prescaling is explained in more detail in *Prescaling Example* on page 213.

# Serial Programming Architecture

The ICD2063 programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (See *Fig. 1: ICD2063 Block Diagram* on page 195) contains several components: a Serial Unlock Decoder (containing the Unlocking Mechanism and Manchester Decoder), a Watchdog Timer, the Serial Data Register (Serial Reg) and a Demultiplexer to the Register File.

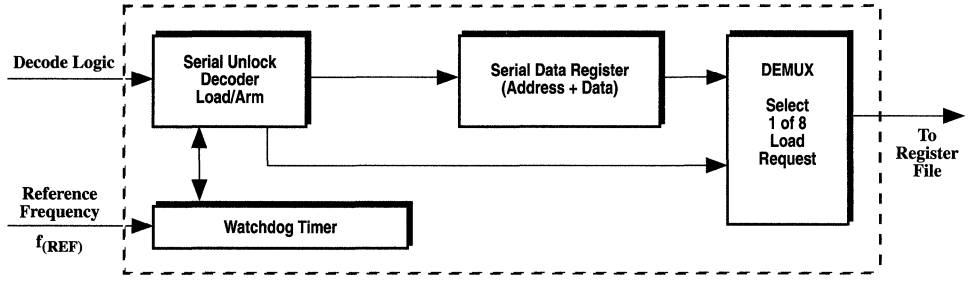



**Fig. 4: Serial Program Block Diagram — Detail**

## Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in the following timing diagram:

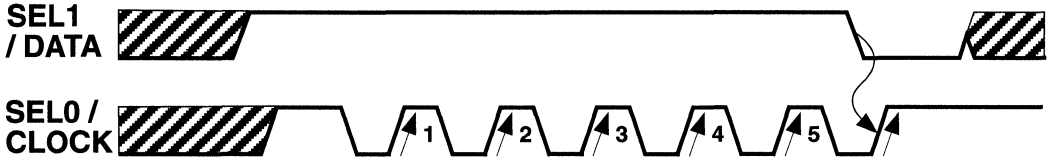



**Fig. 5: Unlock Sequence**

The initial unlock sequence consists of at least five low-to-high transitions of CLK with DATA high, followed immediately by a single low-to-high transition of CLK with DATA low. Following this unlock sequence, the encoded serial data is clocked into the Serial Data Register (Serial Reg).

NOTE: The ICD2063 may not be serially programmed when in Power-Down Mode.

## Watchdog Timer

Following any transition of CLK or DATA, the Watchdog Timer is reset and begins counting. Throughout the entire programming process, the Watchdog Timer ensures that there is a transition on clock or data within the timeout specification (of 2 msec — see *Table 22: AC Characteristics* on page 231). If a timeout does occur, the Lock Mechanism is rearmed and the current data in the Serial Data Register (Serial Reg) is ignored.

Since the VCLK registers are selected by the SEL0–SEL1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of SEL0 & SEL1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. [Note that there is a latency amounting to the duration of the Watchdog Timer before any new register selections take effect.]



## The Serial Data Register

The serial data is clocked into the Serial Data Register (Serial Reg) in the following order:

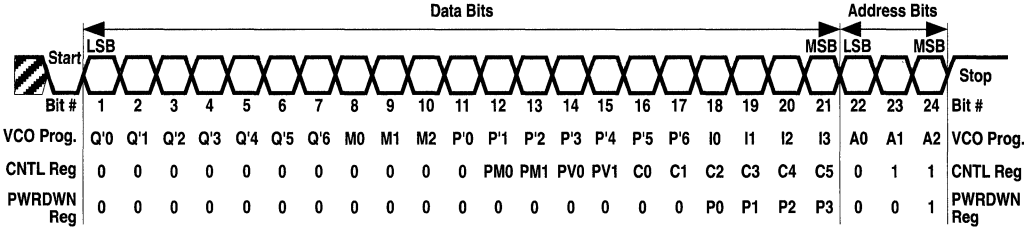



**Fig. 6: Serial Data Timing**

The serial data is sent using a modified Manchester encoded data format. This is defined as follows:

1 — An individual data bit is sampled on the rising edge of CLK.

2 — The complement of the data bit must be sampled on the previous falling edge of CLK.

3 — The Setup and Hold Time requirements must be met on both CLK edges.

4 — The unlock sequence, start, and stop bits are not Manchester encoded.

For specifics on timing, see *Fig. 20: Serial Programming Timing* on page 236.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (VREG0–1, MREG0–1), the data is made up of 4 fields: D[21:18] = Mode (formerly Index); D[17:11] = P'; D[10:8] = Post-VCO Divider; D[7:1] = Q'. [See *Programming the ICD2063* on page 210 for more details on the VCO data word.] For the other registers with fewer than 21 bits (PWRDWN, CNTL), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data Register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or load command is issued by bringing DATA high and toggling CLK high-to-low and low-to-high. The Unlocking Mechanism then automatically rearms itself following the load. Only when the Watchdog Timer has timed out are the SEL0–SEL1 Selection Pins permitted to return to their normal register select function.

Note that the Serial Data Register (Serial Reg) which receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command which passes the Serial Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data Register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the Unlocking Mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the Serial Buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the Unlocking Mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the Unlocking Mechanism is rearmed, the Serial Counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

## ERROUT Operation

The ERROUT signal is used to report when a program error has been detected internally by the ICD2063. The signal stays active until the next unlock sequence.

The following circuit shows the basic mechanism used to detect valid and erroneous serial data:

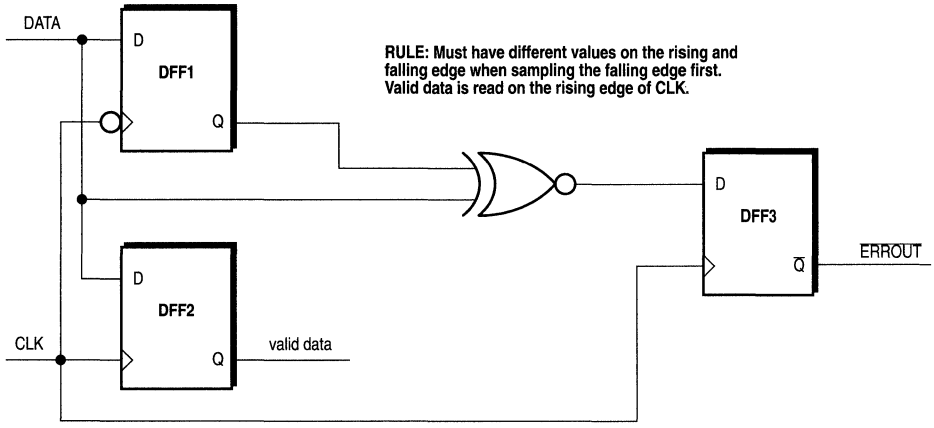



**Fig. 7: Modified Manchester Decoder Circuit**

The ERROUT signal is invoked for any of the following error conditions: incorrect start bit; incorrect Manchester encoding; incorrect length of data word; incorrect stop bit; timeout.

**NOTE 1:** If there is no input pin available on the target VGA controller chip to monitor ERROUT, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming success.

**NOTE 2:** The ERROUT signal is an order option. If the XBUF option is chosen instead, then ERROUT is not available, and the user may want to implement the above technique to verify that the desired programming did indeed take place correctly.

# Programming the ICD2063

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2063 has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields:

## Table 7: Programming Word Bit Fields

| Field | # of Bits | Notes |
|---|---|---|
| Mode (I) | 4 | MSB (Most Significant Bits) |
| P Counter value (P') | 7 | |
| Post-VCO Divider (M) | 3 | |
| Q Counter value (Q') | 7 | LSB (Least Significant Bits) |

The frequency of the Programmable Oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3$$

$$Q' = Q - 2$$

$$f_{(VCO)} = (\text{Prescale} \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (1 MHz – 60 MHz; typically 14.31818 MHz)
and Prescale = 2 or 4 (default is 2, defined by CNTL Reg).

**NOTE:** If a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The following table lists the various limits for $f_{(VCO)}$:

## Table 8: VCO Frequency Ranges

| | 5 Volt Operation | 3.3 Volt Operation |
|---|---|---|
| **VCLK PLL** | 50 MHz – 135 MHz | 50 MHz – 100 MHz |
| **MCLK PLL** | 40 MHz – 100 MHz | 40 MHz – 80 MHz |

For lower output frequencies, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Post-VCO Divider Field (M) as follows:

**Table 9: Post-VCO Divider (M)**

| M2 | M1 | M0 | Divisor |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | 32 |
| 1 | 1 | 0 | 64 |
| 1 | 1 | 1 | 128 |



The Mode Field (I), formerly the Index Field, is included for historical reasons to preserve software compatibility with the ICD2061A. In the ICD2063, it is only used for a few special circumstances, as detailed in the following paragraphs.

**Table 10: Mode Field**

| I3 | I2 | I1 | I0 | VCLK VCO | MCLK VCO |
|---|---|---|---|---|---|
| all others | | | | Ignored | Ignored |
| 1 | 1 | 1 | 0 | VCLK VCO is turned off and output is forced low | Ignored [a] |
| 1 | 1 | 1 | 1 | VCLK is turned off and both channels run from the same MCLK VCO | Ignored [a] |

a. In MUXREF Mode, the memory clock cannot be changed — neither by the selects nor by reprogramming — because the VCLK is shut down and the MCLK is multiplexed to VCLK.

The Mode Field was included to allow turning off the VCLK VCO and optionally multiplexing the MCLK VCO over, then dividing down to the desired frequency. This will significantly reduce heterodyne jitter and is useful if the frequencies are $2^n$ multiples.

When the Index Field is set to **1111**, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, one doesn't want the two VCOs to run at integral multiples of each other; therefore, if one does want the clocks to run at $2^n$ (n = 0, 1, 2 .. 7) multiples of each other, this is done by turning off the VCLK VCO and multiplexing the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

The MCLK VCO completely ignores the Mode Field values. For new designs, IC DESIGNS recommends setting the Mode Field to 0000.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

## Programming Constraints

The following are the primary programming constraints the user must be aware of:

$$1\ \text{MHz} \le f_{(REF)} \le 60\ \text{MHz}$$

$$200\ \text{KHz} \le \frac{f_{(REF)}}{Q} \le 1\ \text{MHz}$$

VCLK:

$$50\ \text{MHz} \le f_{(VCO)} \le 135\ \text{MHz (5V)}$$

$$50\ \text{MHz} \le f_{(VCO)} \le 100\ \text{MHz (3.3V)}$$

MCLK:

$$40\ \text{MHz} \le f_{(VCO)} \le 100\ \text{MHz (5V)}$$

$$40\ \text{MHz} \le f_{(VCO)} \le 80\ \text{MHz (3.3V)}$$

$$3 \le Q \le 129$$

$$4 \le P \le 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the aforementioned ***BitCalc*** program, these constraints become transparent.

## Programming Example

The following is an example of the calculations ***BitCalc*** performs. This example assumes that Prescaling = 2, which is the default value.

Derive the proper programming word for a 39.5 MHz VCLKOUT frequency, using 14.31818 MHz as the reference frequency and with VDD = 5V:

Since 39.5 MHz < 50 MHz, double it to 79.0 MHz. Set M to 001. Since I is a "Don't Care", set it to 0000. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7587$$

Several choices of P and Q are available:

**Table 11: Possible P & Q Values**

| P | Q | $f_{(VCO)}$ ( MHz ) | Error ( ppm ) |
|---|---|---|---|
| 69 | 25 | 79.0363 | 460 |
| 80 | 29 | 78.9969 | 40 |
| 91 | 33 | 78.9669 | 419 |



Choose (P, Q) = (80,29) for best accuracy (40 ppm).

Therefore:

**P' = P – 3 = 80 – 3 = 77 = 1001101** (4dH)

**Q' = Q – 2 = 29 – 2 = 27 = 0011011** (1bH)

and the full programming word, W, is:

**W = I, P', M, Q' = 0000, 1001101, 001, 0011011= 00001001101001011011** (01349bH)

The programming word **W** is then sent as a serial bit stream, LSB first. Appropriate address bits and start/stop bits must also be included as defined in *Serial Programming Architecture* on page 206.

## Prescaling Example

For most users, the resolution of the ICD2063 in its default modes is sufficient. For those cases demanding greater precision, Prescale can be set to 4. This section provides an example.

Assume the desired VCLKOUT frequency is 100 MHz. The table below compares the results of using the default prescaling value of 2 and the optional prescaling value of 4:

**Table 12: Effect of Prescaling**

| Prescale | Desired Frequency | Actual Frequency | P | Q | ppm Error |
|---|---|---|---|---|---|
| 2 | 100 MHz | 99.84028 MHz | 129 | 37 | 1600 |
| 4 | 100 MHz | 99.99998 MHz | 110 | 63 | 0 |

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0–2 (corresponding to REG0–2) — which involves loading a Control Word (taking care to preserve the current values of the other Control Bits) — before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

NOTE: Care must be taken not to change the Prescale Bit of the currently active register: the results will be unpredictable at best, and it could cause the VCO to go out of lock.

## Extended VCLK Frequency Precision

An optional mode set in the CNTL Register allows the VCLK PLL to use the MCLK PLL as its reference frequency instead of $f_{(REF)}$. The advantage is that, by proper tuning of the input reference, very fine frequency control is possible on the output of VCLK, yielding virtually infinite frequency precision.

Just about any desired value can be achieved with worst-case precision of less than 5 ppm.

The reference frequency oscillator is used to drive the MCLK PLL, which is then fed internally to the VCLK PLL to generate the desired signal. However, please note the following:

- **No usable MCLK output** — This method essentially uses two PLLs to derive a single output, so that the MCLK output will probably be meaningless. Therefore, this method is probably not suited to normal VGA graphics applications.
- **Some increased jitter** — The trade-off associated with deriving the VCLK PLL reference from another PLL is that the MCLK+VCLK combination will tend to exhibit more jitter than a single PLL with a crystal-controlled reference — but the jitter should stay below 1 ns.
- **More challenging programming model** — Another trade-off of having 21 bits each to define both the reference frequency and the output is that it makes finding the optimum 2 programming words an iterative process. To aid in these calculations, IC DESIGNS strongly recommends using ***BitCalc***, a utility designed to help in this analysis.

# Power Management Issues

## Power-Down Mode 1

The ICD2063 contains a mechanism to reduce the quiescent power when stand-by operation is desired. In Power-Down Mode 1 (invoked by pulling the $\overline{\text{PWRDWN}}$ signal low and having the proper CNTL Register bit set to zero), both VCOs are shut down, the VCLKOUT output is forced low, and the MCLKOUT output is set to a user-defined low-frequency value to refresh dynamic RAM.

The Power-down MCLKOUT value is determined by the following equation:

$$\text{MCLKOUT}_{\text{Power-Down}} = f_{(\text{REF})} / (\text{PWRDWN Reg Divisor Value})$$

The Power-Down Register divisor is determined according to the following 4–bit word programmed into the PWRDWN Register:



### Table 13: PWRDWN Register Programming

| PWRDWN Bits $P_3$ $P_2$ $P_1$ $P_0$ | PWRDWN Register Value | Power-Down Divisor | $\text{MCLKOUT}_{\text{Power-Down}}$ ($f_{(\text{REF})}$ = 14.31818 MHz) |
|---|---|---|---|
| 0 0 0 0 | 0 | N/A | (Test Mode) |
| 0 0 0 1 | 1 | 32 | 447.4 KHz |
| 0 0 1 0 | 2 | 30 | 477.3 KHz |
| 0 0 1 1 | 3 | 28 | 511.4 KHz |
| 0 1 0 0 | 4 | 26 | 550.7 KHz |
| 0 1 0 1 | 5 | 24 | 596.6 KHz |
| 0 1 1 0 | 6 | 22 | 650.8 KHz |
| 0 1 1 1 | 7 | 20 | 715.9 KHz |
| **1 0 0 0** | **8 (default)** | **18** | **795.5 KHz** |
| 1 0 0 1 | 9 | 16 | 894.9 KHz |
| 1 0 1 0 | A | 14 | 1.023 MHz |
| 1 0 1 1 | B | 12 | 1.193 MHz |
| 1 1 0 0 | C | 10 | 1.432 MHz |
| 1 1 0 1 | D | 8 | 1.790 MHz |
| 1 1 1 0 | E | 6 | 2.386 MHz |
| 1 1 1 1 | F | 4 | 3.580 MHz |

On Power-Up, the value of the PWRDWN Register is loaded with a default value of 8 (1000 binary), which yields an MCLKOUT frequency of 795 KHz (14.31818 / 18). The default mode is Power-Down Mode 1.

**NOTE:** The ICD2063 may not be serially programmed when in Power-Down Mode.

## Power-Down Mode 2

If there is no need for any output during power-down operation, then an alternate power-down mode is available, which will completely shut down all outputs and the reference oscillator, yet still preserve all register contents. This results in the absolute least power consumption.

Power-Down Mode 2 is invoked by first programming the Power-Down bit in the CNTL Register, and then pulling the $\overline{\text{PWRDWN}}$ pin low.

The XTALIN pin is forced low; therefore if an external reference clock is used instead of a crystal, it must be stopped low.

## The $\overline{\text{PWRDWN}}$ Pin

This pin has a standard internal pull-up during normal operation. When the user pulls it down to invoke power-down Mode 1 or 2, the normal pull-up resistor is dynamically switched to a weak pull-up, which significantly reduces power consumption. If, after pulling this pin low, the pin is allowed to float, the weak pull-up will gradually cause the signal to rise and will eventually turn the device back on.

## Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: $I = C \bullet V \bullet f$, where

I = current,
C = load capacitance (max. 25pF),
V = output voltage (usually 5V or 3.3V), and
f = output frequency (in MHz).

To calculate total operating current, sum the following terms:

| | | |
|---|---|---|
| VCLKOUT | $\Rightarrow$ | $C \bullet V \bullet f_{(VCLK)}$ |
| MCLKOUT | $\Rightarrow$ | $C \bullet V \bullet f_{(MCLK)}$ |
| XBUF (if used) | $\Rightarrow$ | $C \bullet V \bullet f_{(REF)}$ |
| Internal | $\Rightarrow$ | 12 mA @ 5V; 8 mA @ 3.3V |

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on package type.

Typical values:

## Table 14: Typical Current Drain Values

| Frequency | Capacitive Load | Current ( mA ) | |
|---|---|---|---|
| | | 5 Volts | 3.3 Volts |
| low | low | 15 | 10 |
| high | low | 40 | 26 |
| high | high | 65 | 44 |

When in Power-Down Mode 1, and using a 14.31818 MHz reference crystal, the power consumption should not exceed 7.5 mA @ 5V or 5 mA @ 3.3V. In Power-Down Mode 2, the power consumption should not exceed 50 µA @ 5V or 35 µA @ 3.3V.

# 3.3 Volt & 5 Volt Issues

The use of 3.3 Volts as a supply voltage greatly reduces the power consumption of portable systems. However, for the foreseeable future, some peripherals may be unable to run at 3.3 Volts. This implies that the ICD2063 might have to function in mixed 5V/3.3V systems. The following discussion will attempt to address the various issues involved in mixed supply usage of the ICD2063.

## VDD & AVDD

The ICD2063 has two isolated power leads: VDD and AVDD. Each supply may be independently run at either 3.3V or at 5V. The VDD rail supplies power to the I/O pad ring and core. All outputs and inputs are referenced to this voltage input. The device has a 4-Volt Detector which determines the pad's operating voltage and adjusts the threshold for the input pins. This guarantees that at either voltage, the inputs maintain TTL compatibility. If the voltage dynamically changes on the VDD line (for instance going from 5V to 3.3V), the thresholds will be maintained properly.

The AVDD pin supplies power to the VCO core. Since the VCO needs to know what the supply voltage is, a second 4-Volt Detector is placed on AVDD to set the VCO operation properly. If the voltage dynamically changes on the AVDD line (again, say from 5V to 3.3V), the VCOs will lose lock momentarily when the 4-Volt detector triggers, and will re-lock to the desired value after a brief settling time. (*Fig. 8: Effect of Supply Voltage Change to Clock Output* on page 219) This time should be less then 5 msec. This period of instability could cause a glitch in the output.

If a system requires dynamically changing from 5V to 3.3V and back (for example some docking stations), and proper glitch-free output must be maintained during the transition period, then the AVDD supply line should remain at 3.3 Volts while the VDD pin can float to the desired levels. If this split mode is to be used, then the control bit, **Split Supply Mode**, should be properly set. (See *Control Register Definition* on page 205 for more details.) Also note that, in this mode, the frequency range is limited to the narrower 3.3V values.

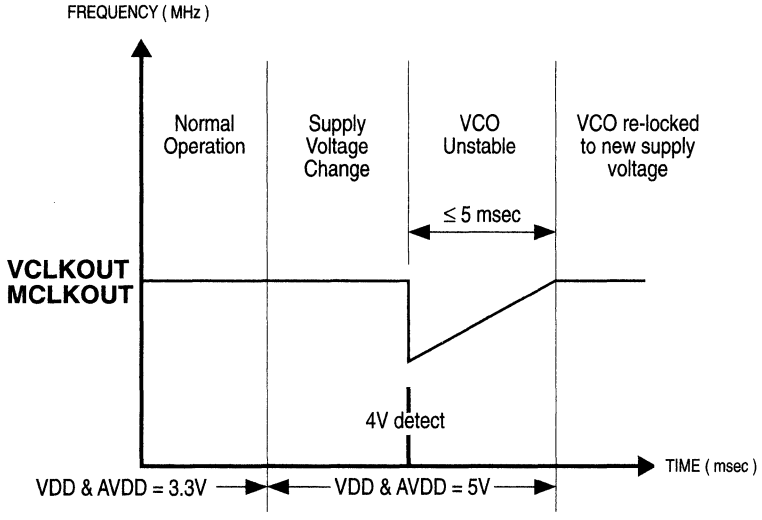



**Fig. 8: Effect of Supply Voltage Change to Clock Output**

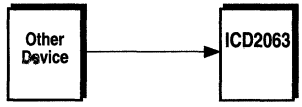
## Mixed Voltage Interfaces

The other issue which must be addressed is interfacing the ICD2063 into mixed-voltage systems. The following 2 tables depict the various configurations:

**Table 15: ICD2063 Driving other Devices**

| ICD2063 → Other Device | | Status |
|---|---|---|
| 5V | 5V | OK |
| 3.3V | 5V | OK if driving TTL inputs; if driving CMOS inputs, then ICD2063 output will appear to have a low duty cycle. |
| 5V | 3.3V | Potential latch-up problems with other devices; will work if other device's input will accept $V_{IH}$ = VDD +2V. |
| 3.3V | 3.3V | OK |

## Table 16: Other Devices Driving ICD2063

|  | | Status |
|---|---|---|
| 5V | 5V | OK |
| 3.3V | 5V | OK |
| 5V | 3.3V | TTL outputs only; input to ICD2063 must not exceed VDD + 0.3V |
| 3.3V | 3.3V | OK |

# Frequency Transition Options

The ICD2063 may be configured for one of two frequency transition options: the Smooth Transition Option or the MUXREF Option (for compatibility with the ICD2061A).

## Smooth Transition Option

Upon changing VCLK or MCLK, either by reprogramming the active register or by selecting a new register, the output will transition in one of two basic ways, depending on the post-divide values (Post-divide is used to divide down the VCO output to frequencies below the normal VCO operating range):

- **Normal Operation** — If the post-divide value (M) is the same for both frequencies (original and target), then the output will transition smoothly and linearly from the original to the target frequency, with no overshoot.



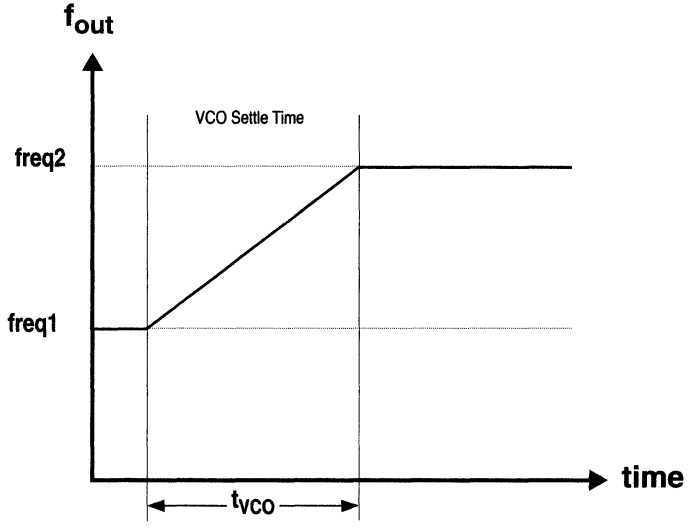



**Fig. 9: Frequency Transition**
**Smooth Mode: Normal Operation**

- **Post-Divide Operation** — If the post-divide value (M) differs between the original and target frequencies, then the output behaves somewhat differently, but will never exceed the greater of the original and target frequencies.

  1. If the post-divide value decreases (say from ÷2 to ÷1), then there is, first, a smooth transition to the target frequency ÷2; second, the post-divide is changed, resulting in an instantaneous transition to the target frequency.
  2. If the post-divide value increases (say from ÷1 to ÷2), then post-divide is, first, immediately set to the new value, resulting in an instantaneous transition to an output frequency that is half the original; second, there is a smooth transition from this frequency to the target frequency.

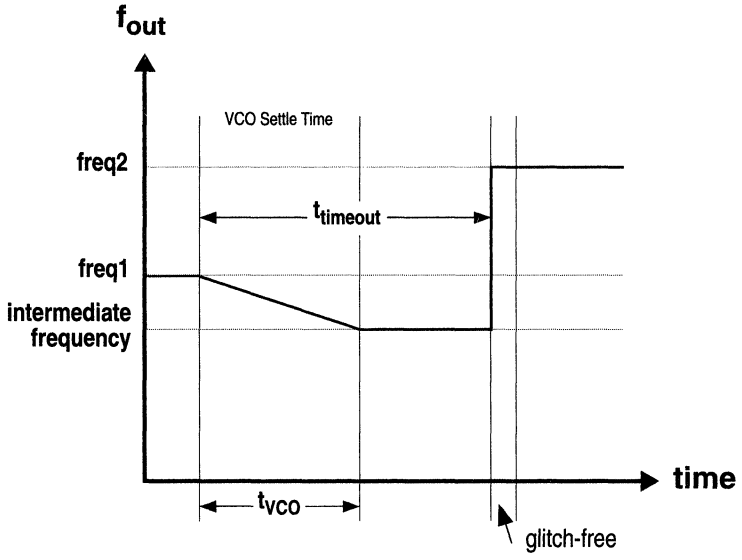
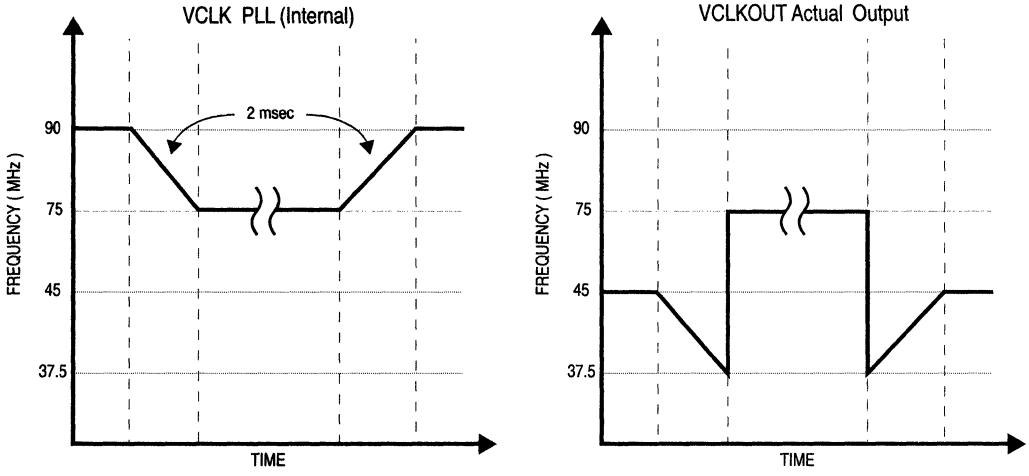



**Fig. 10: Frequency Transition**
**Smooth Mode: Post-Divide 'M' Values Differ**




**EXAMPLE: 45 MHz ⇒ 75 MHz ⇒ 45 MHz**

**Fig. 11: Smooth Frequency Transition Example**

## MUXREF Option

The other option for frequency transition is to multiplex the output of the VCO undergoing change to some alternate stable frequency until the VCO has settled to the new frequency value. This option preserves compatibility with the earlier ICD2061A.

In general, any changes to the VCLK VCO will result in the Reference Frequency ($f_{(REF)}$) being multiplexed to the output. However, since most video controllers now use the MCLK output as their principal clock source, and since an $f_{(REF)}$ of 14.31818 MHz is in many cases too slow for proper operation of the VGA chip, changes to the MCLK VCO will result in the VCLKOUT signal being multiplexed to the MCLK output.

The following five cases detail specifics about operation with the MUXREF option during frequency transitions.

### Case 1: MCLK PLL Transition — Reprogramming of the Active Register

When a new frequency is being set for the active MCLK register, then a glitch-free multiplexing to the VCLKOUT signal is performed. For more details, see *Fig. 16: Active MCLK & VCLK Register Programming Timing (MUXREF Mode)* on page 234.

### Case 2: VCLK PLL Transition — Reprogramming of the Active Register

When a new frequency is being set for the active VCLK register, then a glitch-free multiplexing to the reference signal $f_{(REF)}$ is performed. For more details, see *Fig. 16: Active MCLK & VCLK Register Programming Timing (MUXREF Mode)* on page 234.

### Case 3: MCLK PLL Transition — Changing Register Selects

When a new MCLK frequency is being set by the register selects, then a glitch-free multiplexing to the VCLKOUT signal is performed. For more details, see *Fig. 17: Selection Timing (MUXREF Mode)* on page 234.

### Case 4: VCLK PLL Transition — Changing Register Selects

When a new VCLK frequency is being set by the register selects, then a glitch-free multiplexing to the reference signal ($f_{(REF)}$) is performed. For more details, see *Fig. 17: Selection Timing (MUXREF Mode)* on page 234.

### Case 5: VCLK & MCLK PLL Transition — Changing Register Selects

If the Reset Option is configured and the select sequence is chosen which results in a coincident change in both MCLK and VCLK registers (i.e., selects go from being *11* or go to being *11*), then first a new MCLK frequency is set with a glitch-free multiplexing to the current VCLKOUT signal, followed by the new VCLK frequency being set with a glitch-free multiplexing to the reference signal ($f_{(REF)}$) being performed. For more details, see *Fig. 18: VCLK & MCLK Selection Timing (Concurrent Change)* on page 235.

# General Considerations

## Operation with the ICD2029

A powerful feature of the ICD2063 is the ability to use it with other clock generators which are Serially Cascadable compatible (such as the ICD2029 PC Motherboard Clock Generator).

The combination of these 2 clock generators will provide the most comprehensive timing generation and power-down options currently available for portable computers. The advantage of Serially Cascadable support is that the ICD2029 can be directly programmed via the same resources that drive the ICD2063.



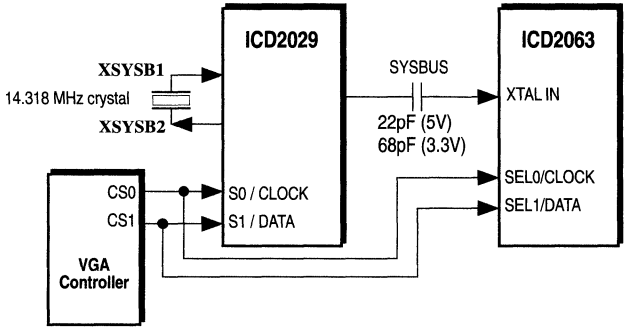



**Fig. 12: Cascading the ICD2063 & the ICD2029**

For more details on this operation, pleases refer to the ICD2029 Datasheet.

## Phase-Locked Loop Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown below. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO either to go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output fre-

quency. This up and down movement of the variable frequency will quickly lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

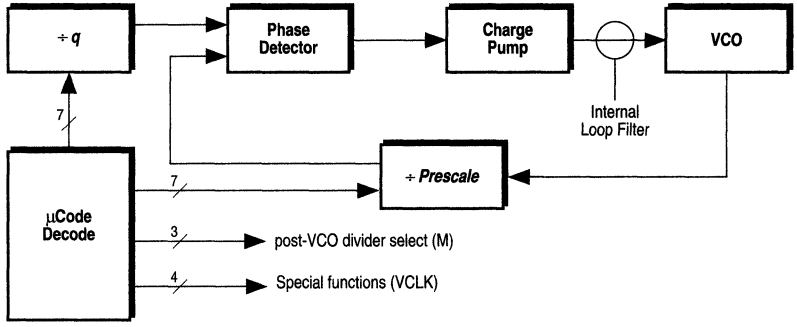



**Fig. 13: Phase-Locked Loop Oscillator**

## Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphics designs.

## Frequency Range

The following table lists the various frequency limits for each output:

**Table 17: Frequency Ranges**

| | 5 Volt Operation | 3.3 Volt Operation |
|---|---|---|
| VCLKOUT | 390 KHz – 135 MHz | 390 KHz – 100 MHz |
| MCLKOUT | 312 KHz – 100 MHz | 312 KHz – 80 MHz |

## Output Disable

When the $\overline{\text{OUTDIS}}$ pin is asserted (active low), all the output pins except XTAL OUT enter a high impedance mode, to support automated board testing.

## External Clock Input (Feature Connector Compatibility)

To maintain backward compatibility to the VGA feature connector standard, the Video Clock output VCLKOUT can multiplex between the clock synthesizer output and the external clock input FEATCLK. This multiplexing is controlled by the INTCLK input signal and appropriate decode of selection signals (SEL0, SEL1). See the section *Register Selection* on page 203 for more information.

## XBUF — Buffered Crystal Reference Output Option



A buffered crystal oscillator output is optionally available as a user-configurable option on pin 10 ($\overline{\text{ERROUT}}$/XBUF). Its output is identical to the reference frequency. Selection of this option replaces the $\overline{\text{ERROUT}}$ function.

## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Note *Power Feed and Board Layout Issues* on page 281 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2063 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2063 closest to the device requiring the highest frequency.

## FCC & Noise Issues

A conscious design effort was made to achieve the optimum rise & fall times at the output pads in order to produce acceptable signals at the clock destinations when operating at high frequencies. Unfortunately, the production of the squarest possible square waves can lead to the generation of high-energy odd harmonics, which can result in extraneous emissions.

For techniques on how to design with this device while taking FCC emission issues into consideration, please refer to the IC DESIGNS Application Note, *Minimizing Radio Frequency Emissions* on page 285.

## Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on opposite sides of the die. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate power and ground buses for the analog and digital circuitry are used.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2063 is inherently stable over temperature, voltage and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2063, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

# Ordering Information

## Table 18: Configuration Options

| Option | Choices | –1 | –2 | –3 |
|---|---|---|---|---|
| **Pin 10 Function** | ERROUT –or– XBUF | XBUF | ERROUT | ERROUT |
| **Pin 14 Function** | RESET –or– SELM | SELM | RESET | SELM |
| **Frequency Transition** | Smooth –or– MUXREF | Smooth | MUXREF | Smooth |



## Table 19: Order Codes

| Part Number | Package Type | Temperature Range | Chip Options |
|---|---|---|---|
| **ICD2063** | S = 16-Pin SOIC DIP | C = Commercial[a] | –1, –2, –3 |

a. 0°C to +70°C

Example: order ICD2063SC–1 for the ICD2063, 16–pin plastic DIP, commercial temperature range device with the initial frequencies shown in *Table 3: Register Initialization ROM* on page 203.

# Device Specifications

## Electrical Data

### Table 20: Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ & $AV_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 375 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ & $AV_{DD}$ = +5V ±5% (+3.3V ±10%); 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 21: DC Characteristics

| Name | Description | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ & $A_{VDD}$ | Supply voltage relative to GND[a]<br>390 KHz – 100 MHz<br>390 KHz – 120 MHz<br>390 KHz – 135 MHz | <br>3.0<br>4.5<br>4.75 | | <br>3.6<br>5.5<br>5.5 | Volts | VCLK specs shown (MCLK low end = 312 KHz) |
| $V_{IH}$ | High-level input voltage | 2.0 | | $V_{DD}$+0.3 | Volts | |
| $V_{IL}$ | Low-level input voltage | –0.3 | | 0.8 | Volts | |
| $V_{OH}$ | High-level CMOS output voltage | $V_{DD}$ – 0.5 | | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output voltage | | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $I_{IH}$ | Input high current | | | 150 | µA | $V_{IH}$ = $V_{DD}$ – 0.5V |
| $I_{IL}$ | Input low current | | | –250 | µA | $V_{IH}$ = 0.5V |
| $I_{OZ}$ | Output leakage current | | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | 15 / 10 | | 65 / 44 | mA | 5V / 3.3V |
| $I_{DD-TYP}$ | Power supply current (typical) | | 35 / 24 | 80 / 50 | mA | 5V / 3.3V (60 MHz) |
| $I_{ADD}$ | Analog power supply current | | | 10 | mA | |
| $I_{PD1}$ | Power-down current (Mode 1) | | 6 / 4 | 7.5 / 5.0 | mA | 5V / 3.3V |
| $I_{PD1}$ | Power-down current (Mode 2) | | 25 / 20 | 50 / 35 | µA | 5V / 3.3V |

a. For transition between 3.3V and 5V operation, refer to *3.3 Volt & 5 Volt Issues* on page 218.

## Table 22: AC Characteristics

| Symbol | Name | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $f_{(REF)}$ | reference frequency | Reference Oscillator nominal value (NOTE: for references other than 14.31818 MHz, the pre-loaded ROM frequencies will not be accurate.) | | 1 | 14.318 | 60 | MHz |
| $t_{(REF)}$ | reference period | $1 \div f_{(REF)}$ | | 16.6 | | 1000 | ns |
| $t_1$ | input duty cycle | Duty cycle for the input oscillator, defined as $t_1 \div t_{(REF)}$ | | 25% | 50% | 75% | |
| $t_2$ | output clock periods | VCLK output values | $V_{DD}$ = 5V | 7.41 (135 MHz) | | 2564 (390 KHz) | ns |
| | | | $V_{DD}$ = 3.3V | 10.0 (100 MHz) | | | |
| | | MCLK output values | $V_{DD}$ = 5V | 10.0 (100 MHz) | | 3205 (312 KHz) | |
| | | | $V_{DD}$ = 3.3V | 12.5 (80 MHz) | | | |
| $t_3$ | output duty cycle | Duty cycle for the output oscillators NOTE: measured at CMOS threshold levels ($V_{DD} \div 2$) [@ 5V, $V_{TH}$ = 2.5V] | | 40% | | 60% | |
| $t_4$ | rise times | Rise time for the output oscillators into a 25pF load. | | | | 3 | ns |
| $t_5$ | fall times | Fall time for the output oscillators into a 25pF load. | | | | 3 | ns |
| $t_{freq1}$ | freq1 output | Old frequency output | | | | | |
| $t_{freq2}$ | freq2 output | New frequency output | | | | | |
| $t_A$ | $f_{(REF)}$ mux time | Time clock output remains low while output muxes to reference frequency | | $\frac{t_{(REF)}}{2}$ | | $3\frac{t_{(REF)}}{2}$ | ns |
| $t_{timeout}$ | timeout interval | Internal interval for special programming, and for VCO changes to settle. (If the interval is too short, read about the timeout interval in the *Control Register Definition* on page 205.) | | 2 | 5 | 10 | msec |
| $t_B$ | $t_{freq2}$ mux time | Time clock output remains low while output muxes to new frequency value | | $\frac{t_{freq2}}{2}$ | | $3\frac{t_{freq2}}{2}$ | ns |
| $t_6$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion | | 0 | | 12 | ns |
| $t_7$ | clock valid | Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high | | 0 | | 12 | ns |

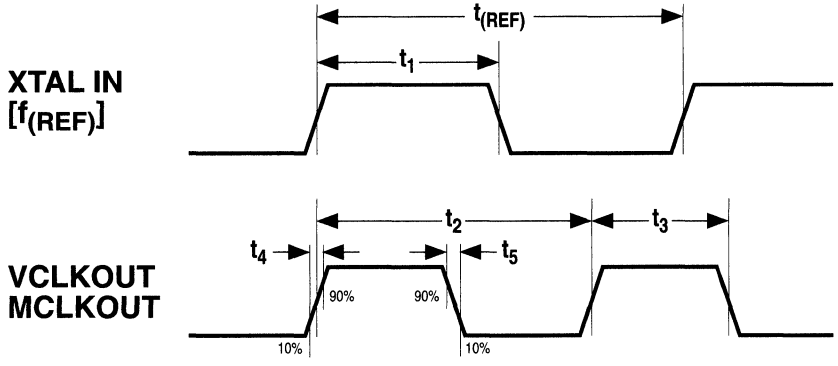
## Table 22: AC Characteristics (Continued)

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_8$ | Power-Down | Time for Power-Down Mode to take effect | | | 12 | ns |
| $t_9$ | Power-Up | Time to recover from Power-Down Mode | | | 12 | ns |
| $t_{10}$ | MCLKOUT high | Time for MCLKOUT to go low after PWRDWN is asserted high | 0 | | $\frac{1}{t_{PWRDWN}}$ | ns |
| $t_{11}$ | MCLKOUT delay | Delay of MCLKOUT prior to $f_{MCLK}$ signal at output | $\frac{t_{MCLK}}{2}$ | | $3\frac{t_{MCLK}}{2}$ | ns |
| $t_{serclk}$ | | Clock period of serial clock | $2 \bullet t_{(REF)}$ | | 2 | msec |
| $t_{SU}$ | | Setup time | 20 | | | ns |
| $t_{HD}$ | | Hold time | 10 | | | ns |
| $t_{ldcmd}$ | | Load command time | 0 | | $t_1 + 30$ | ns |

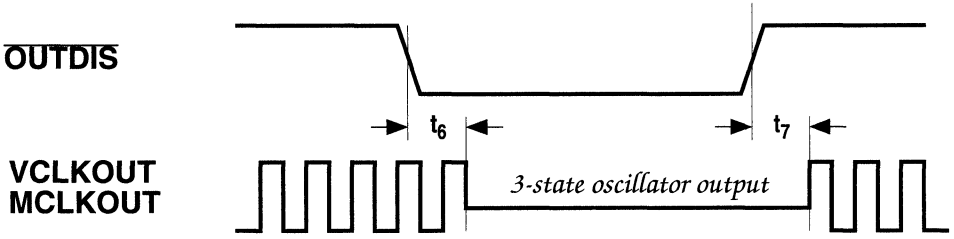
**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

## Timing Diagrams

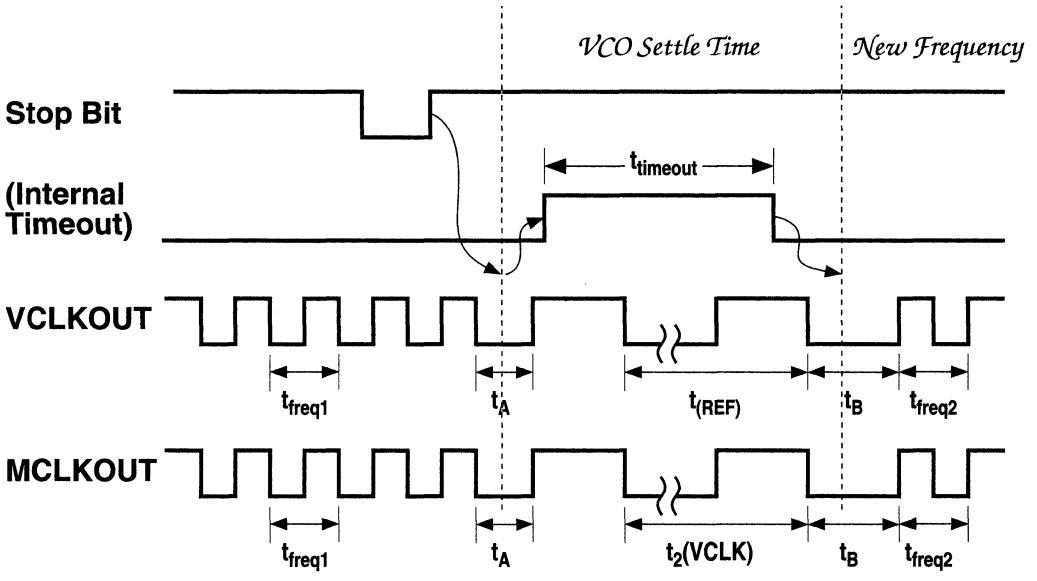
### Fig. 14: Rise and Fall Times



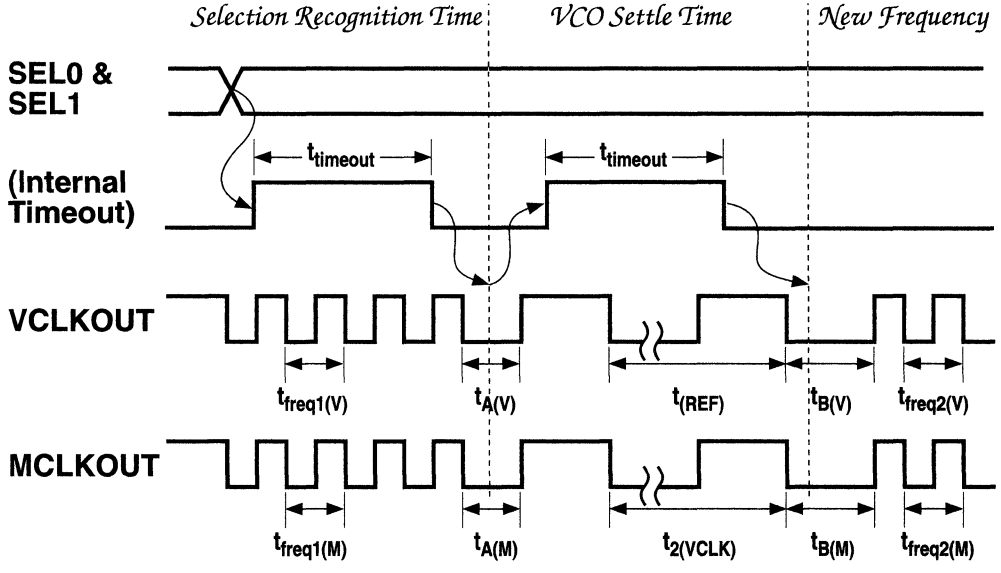

### Fig. 15: 3-StateTiming



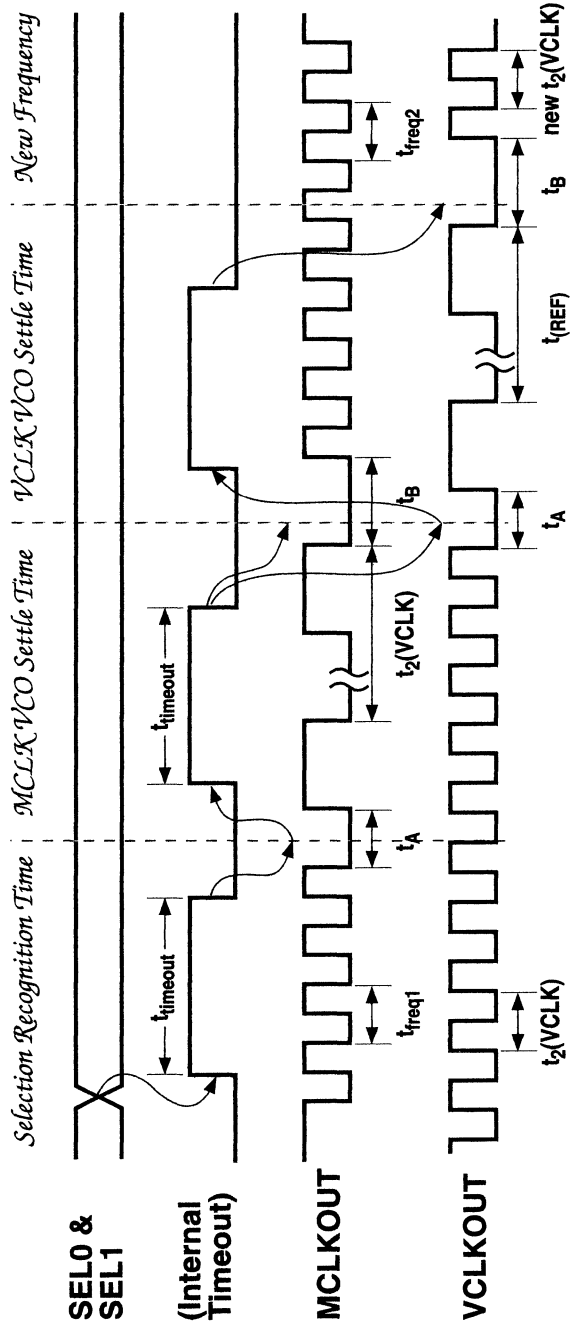
## Fig. 16: Active MCLK & VCLK Register Programming Timing (MUXREF Mode)



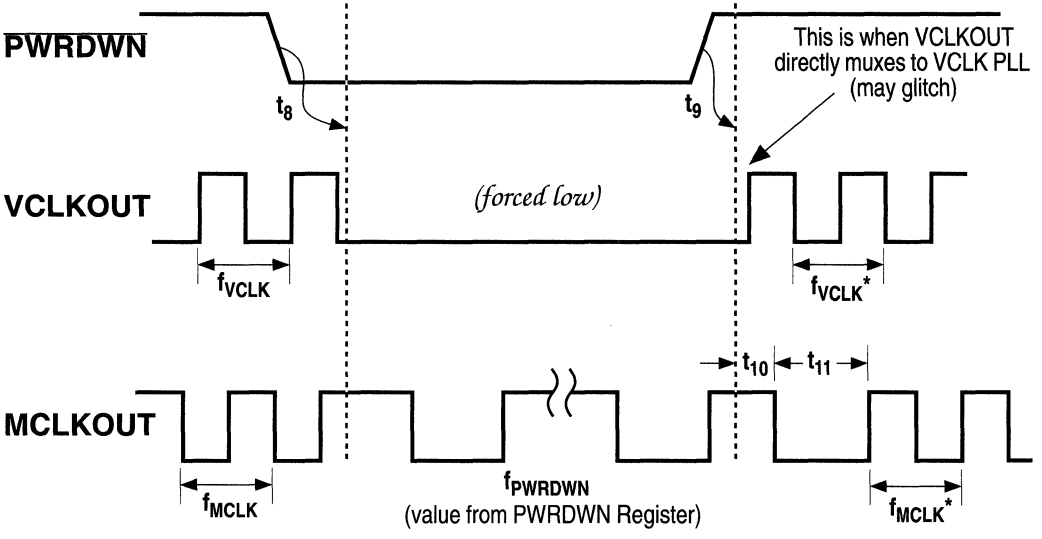

## Fig. 17: Selection Timing (MUXREF Mode)



## Fig. 18: VCLK & MCLK Selection Timing (Concurrent Change)

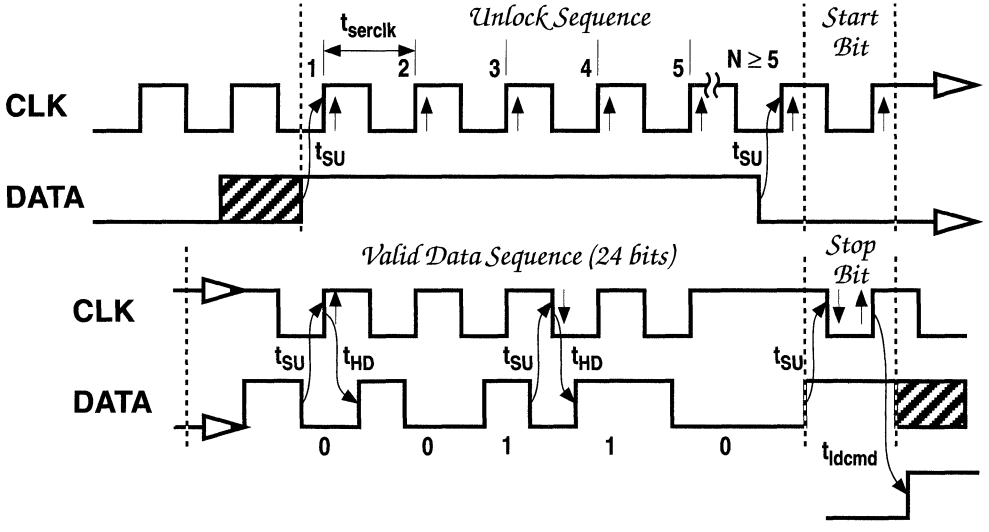


## Fig. 19: Soft Power-Down Timing




* It takes 5 msec after Soft Power-Down to guarantee lock of VCLKOUT & MCLKOUT PLLs

## Fig. 20: Serial Programming Timing



# Revision History / Credits

V1.2 (11/15/93) — Preliminary Release

# Programmable Products

4

# 4 – Programmable Products 239

# ICD2051

## Dual Programmable Clock Oscillator

**Single-Chip Programmable Oscillator Replaces Traditional Can Oscillators in Multi-Frequency or Variable Frequency Environments**

- **2 Independent Clock Outputs Ranging from 320 KHz – 120 MHz**
- **Individually Programmable Oscillators Using a 22–bit Serial Word**
- **Low-Skew ÷1 and ÷2 Outputs, plus ÷4 CLKA Output**
- **Phase-Locked Loop Oscillator Input Derived from External Low-Frequency Reference Clock (1 MHz – 60 MHz) or External Crystal (2 MHz – 24 MHz)**
- **3-State Oscillator Control Disables Outputs for Test Purposes (Optional)**
- **Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters**
- **5V Operation**
- **Low-Power, High-Speed CMOS Technology**
- **Available in 16-Pin SOIC Package Configurations**

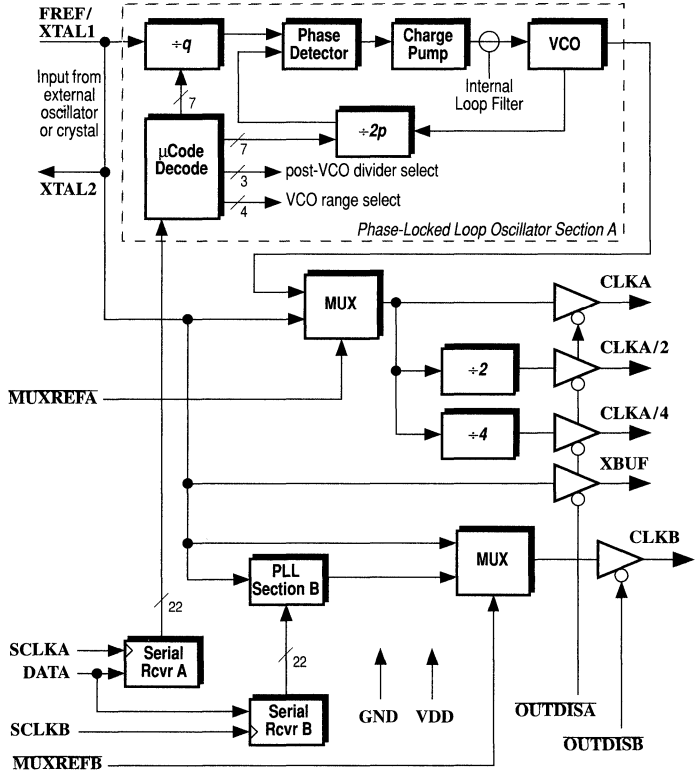



**Fig. 1: ICD2051 Block Diagram**

# Contents



# Figures



# Tables

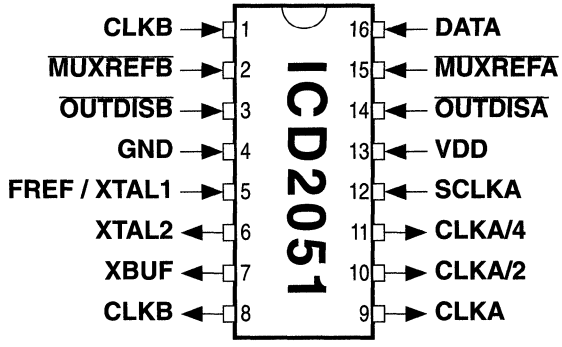
# Introduction

The ICD2051 Programmable Clock Generator offers 2 fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value between 320 KHz and 120 MHz. The ICD2051 is ideally suited for any design where one or more multiple or varying frequencies are required, replacing more expensive metal can oscillators.

The capability to change the output frequency dynamically adds a whole new degree of freedom for the electrical engineer heretofore unavailable with existing crystal oscillator devices. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption or speeding it up can mean faster operation; graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

# Pin & Signal Descriptions

## Fig. 2: Pin Descriptions



## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | SCLKB | SCLKB is the serial clock input line for CLKB. |
| 2 | $\overline{\text{MUXREFB}}$ | $\overline{\text{MUXREFB}}$ = 0, CLKB equals input reference frequency.<br>$\overline{\text{MUXREFB}}$ = 1, CLKB equals programmed frequency.<br>This is used if glitch-free frequency changes are required. |
| 3 | $\overline{\text{OUTDISB}}$ | Output Disable (3-State Output Enable) when signal is pulled low.<br>(Internal pull-up allows no-connect if 3-state operation is not required.) |
| 4 | GND | Ground |
| 5 | FREF / XTAL1 | Input Reference Oscillator derived from available reference signal or attached crystal. (see XTAL2) |
| 6 | XTAL2 | Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator is used.) |
| 7 | XBUF | Buffered Crystal Oscillator Output. CMOS/TTL compatible. |
| 8 | CLKB | CLKB Programmable Oscillator Output |
| 9 | CLKA | CLKA Programmable Oscillator Output |
| 10 | CLKA/2 | CLKA divided by 2.<br>Note that this output has low skew with respect to the CLKA output. |
| 11 | CLKA/4 | CLKA divided by 4. |
| 12 | SCLKA | SCLKA is the serial clock input line for CLKA. |
| 13 | VDD | +5V |
| 14 | $\overline{\text{OUTDISA}}$ | Output Disable when signal is pulled low.<br>(Internal pull-up allows no-connect if 3-state operation is not required.) |
| 15 | $\overline{\text{MUXREFA}}$ | $\overline{\text{MUXREFA}}$ = 0, CLKA equals input reference frequency.<br>$\overline{\text{MUXREFA}}$ = 1, CLKA equals programmed frequency.<br>This is used if glitch-free frequency changes are required. |
| 16 | DATA | Serial data input line for both programmable clock oscillators. |

# General Considerations

## Programming the ICD2051

The desired output frequency is defined via a serial interface, with a 22-bit number shifted in. The ICD2051 has two programmable oscillators (CLKA and CLKB), requiring a 22-bit programming word (W) to be loaded into each channel independently. This word contains 5 fields:

**Table 2: Programming Word Bit Fields**

| Field | # of Bits | Notes |
|---|---|---|
| Index (I) | 4 | MSB (Most Significant Bits) |
| P Counter value (P') | 7 | |
| Reserved (R) | 1 | normally set to logic 1 |
| Mux (M) | 3 | |
| Q Counter Value (Q') | 7 | LSB (Least Significant Bits) |

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency (between 1 MHz – 60 MHz)

The value of $f_{(VCO)}$ must remain between 40 MHz and 120 MHz inclusive. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

## Table 3: Mux Field (M)

| M | Divisor |
|---|---|
| 000 | 1 |
| 001 | 2 |
| 010 | 4 |
| 011 | 8 |
| 100 | 16 |
| 101 | 32 |
| 110 | 64 |
| 111 | 128 |

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$ rather than to the desired output frequency.)

## Table 4: Index Field (I)

| I | $f_{VCO}$ (MHz) |
|---|---|
| 0000 | 40.0 – 42.5 |
| 0001 | 42.5 – 47.5 |
| 0010 | 47.5 – 53.5 |
| 0011 | 53.5 – 58.5 |
| 0100 | 58.5 – 62.5 |
| 0101 | 62.5 – 68.5 |
| 0110 | 68.5 – 69.0 |
| 0111 | 69.0 – 82.0 |
| 1000 | 82.0 – 87.0 |
| 1001 | 87.0 – 92.0 |
| 1010 | 92.0 – 92.1 |
| 1011 | 92.1 – 105.0 |
| 1100 | 105.0 – 115.0 |
| 1101 | 115.0 – 120.0 |
| 1110 | 115.0 – 120.0 |
| 1111 | 115.0 – 120.0 |

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

## Programming Constraints

There are five primary programming constraints the user must be aware of:

$$1\text{MHz} \leq f_{(REF)} \leq 60\text{ MHz}$$

$$200\text{ KHz} \leq \frac{f_{(REF)}}{Q} \leq 1\text{ MHz}$$

$$40\text{ MHz} \leq f_{(VCO)} \leq 120\text{ MHz}$$

$$3 \leq Q \leq 129$$

$$4 \leq P \leq 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the ***BitCalc*** program, these constraints become transparent.

## ICD2051 Programming Example

The following is an example of the calculations ***BitCalc*** performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 40 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0111. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

**Table 5: P & Q Value Candidates**

| P | Q | $f_{(VCO)}$ ( MHz ) | Error ( ppm ) |
|---|---|---|---|
| 69 | 25 | 79.0363 | 460 |
| 80 | 29 | 78.9969 | 40 |
| 91 | 33 | 78.9669 | 419 |

Choose (P, Q) = (80,29) for best accuracy (40 ppm).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \text{ (4dH)}$$

$$Q' = Q - 2 = 29 - 2 = 27 = 0011011 \text{ (1bH)}$$

and the full programming word, W, is:

$$W = I, P', R, M, Q' = 0111, 1001101, 1, 001, 0011011 = 01111001101100100 11011 \text{ (1e6c9bH)}$$

A low-to-high transition on SCLKA/SCLKB (depending on appropriate channel) is used to shift the programming word W into DATA as a serial bit stream, LSB first. (See the set-up and hold timing specifications elsewhere in this datasheet.) If more than 22 shifts are performed, then only the last 22 data bits received will be retained.

## Glitch-Free Frequency-Modification Procedure

When changing to a new frequency, there is a period of time when the output signal will be in transition and may glitch due to changes in the post divider. For applications where it is critical that the output clock not glitch and always maintain some known value, the $\overline{\text{MUXREFA}}$ and $\overline{\text{MUXREFB}}$ inputs must be used. Under normal operation, $\overline{\text{MUXREF(X)}}$ is high and the output clocks are at the programmed value. When $\overline{\text{MUXREF(X)}}$ is brought low, the reference clock is now multiplexed to the associated output clock. The output remains at this fixed frequency while the programmed frequency seeks its new value.

When programming the ICD2051, use the MUXREF inputs in the following manner:

1. Set $\overline{\text{MUXREF(X)}}$ to a low state. This will set the output to the reference frequency. The transition is guaranteed to be glitch-free. (See the timing specifications.)
2. Shift in the desired output frequency value via a 22-bit word (as defined above) using the appropriate SCLK and DATA lines.
3. After the last bit is shifted in, the VCO will settle to the new state (within .01% of the actual output frequency) within 10 msec.
4. Set $\overline{\text{MUXREF(X)}}$ to a high state. This will set the output to the new programmed frequency. The transition is guaranteed to be glitch-free. (See *Fig. 4: Serial Programming Timing* on page 257.)

## Skew-Free ÷2 on CLKA

The CLKA output is available concurrently as ÷1, ÷2 and ÷4 values of the desired output. The ÷1 and ÷2 outputs are also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 2 ns of skew between the two outputs, with 1 ns or less available as an order option.

## Output Frequency Accuracy

The accuracy of the ICD2051 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2051 are integrally related to the input reference frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2051 generally produces an output frequency within 0.1% of the desired output frequency. Specifics regarding accuracy (ppm) are given for any desired output frequency as part of the ***BitCalc*** program output.

## 3-State Output Operation

The $\overline{\text{OUTDISA}}$ or $\overline{\text{OUTDISB}}$ signal, when pulled low, will 3-state the clock output line (CLKA or CLKB respectively). This supports wired-or connections between external clock lines, and allows for procedures where the clock must be disabled, such as automated testing. The output disable signals contain internal pull-ups; they may be left unconnected if 3-state operation is not required.



## No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2051.

## Layout & Power Conditioning Considerations

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The power pin should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin.

The designer should also avoid routing any of the output traces of the ICD2051 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies. When designing with this device, it is best to locate the ICD2051 closest to the device requiring the highest frequency.

A clean power supply is important, particularly at the higher frequencies. For best results, use either a +12V supply through a +5V Zener diode or a 3-pin +5V voltage regulator.

If a +12V supply is not available, then we recommend using a low-pass filter consisting of a capacitor and a 22Ω resistor. This method works quite well, but it has one drawback which must be allowed for, namely that there will be a frequency-dependent voltage drop across the resistor. The ICD2051 can operate over a very wide frequency range (300 KHz – 120 MHz), and operating power consumption depends on the frequency, ranging from a minimum of around 15 mA for very low frequencies on up to 100 mA at the top end. This results in a large frequency-dependent voltage drop across the RC circuit.

Thus, if the ICD2051 is to be used over a wide frequency range, use the voltage regulator method, running the device at the normal supply specification of +5V. If, on the other hand, the device is to be used over a narrow frequency range, and if the total power consumption is determined not to cause more than a 0.25V change across the RC filter (see the following section), then the filter method may be used.

## Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: I = C • V • f, where I=current, C=load capacitance (max. 25pF), V=output voltage (usually 5V), and f=output frequency (in MHz).

To calculate total operating current, sum the following:

XBUF $\Rightarrow$ $C \cdot V \cdot f_{(REF)}$
CLKA $\Rightarrow$ $C \cdot V \cdot f_{(CLKA)}$
CLKA/2 $\Rightarrow$ $C \cdot V \cdot f_{(CLKA/2)}$
CLKA/4 $\Rightarrow$ $C \cdot V \cdot f_{(CLKA/4)}$
CLKB $\Rightarrow$ $C \cdot V \cdot f_{(CLKB)}$
Internal $\Rightarrow$ 12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5–10pF loading, depending on package type.

Typical values:

**Table 6: Typical Load Current Values**

| Frequency | Load | Current ( mA ) |
|---|---|---|
| low | none | 15 |
| high | none | 40 |
| high | high | 100 |

## Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

## Minimized Parasitic Problems

All of the ICD2051 families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, both the synthesis blocks are physically separated into discrete elements, with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCOs are separated from the digital logic. Finally, separate ground buses for the analog and digital circuitry are used.



## Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for graphics designs (which tend to be the most demanding applications with regard to bit-jitter).

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2051 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2051, no manufacturing "tweaks" to external filter components are required as is the case with external filters.

# Ordering Information

## Table 7: Order Codes

| Part Number | Package Type | Temperature Range |
|---|---|---|
| ICD2051 | S = 16-Pin SOIC DIP | C = Commercial[a] |

a. 0°C to +70°C

Example: order ICD2051SC for the ICD2051, 16-pin plastic SOIC, commercial temperature range device.

# Device Specifications

## Electrical Data

### Table 8: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction temperature | | +125 | °C |
| $P_{DISS}$ | Power dissipation | | 525 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

4

### Table 9: DC Characteristics

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2.0 | | Volts | |
| $V_{IL}$ | Low-level input voltage | | 0.8 | Volts | |
| $V_{OH}$ | High-level CMOS output voltage | 2.4 | | Volts | $I_{OH}$ = –4.0 mA |
| $V_{OL}$ | Low-level output voltage | | 0.4 | Volts | $I_{OL}$ = 4.0 mA |
| $I_{IH}$ | Input high current | | 150 | µA | $V_{IH}$ = 5.25V |
| $I_{IL}$ | Input low current | | –250 | µA | $V_{IL}$ = 0V |
| $I_{OZ}$ | Output leakage current | | 10 | µA | (3-state) |
| $I_{DD}$ | Power supply current | 15 | 100 | mA | |
| $I_{DD-TYP}$ | Power supply current (typical) | | 50 | mA | typ @ 50 MHz |

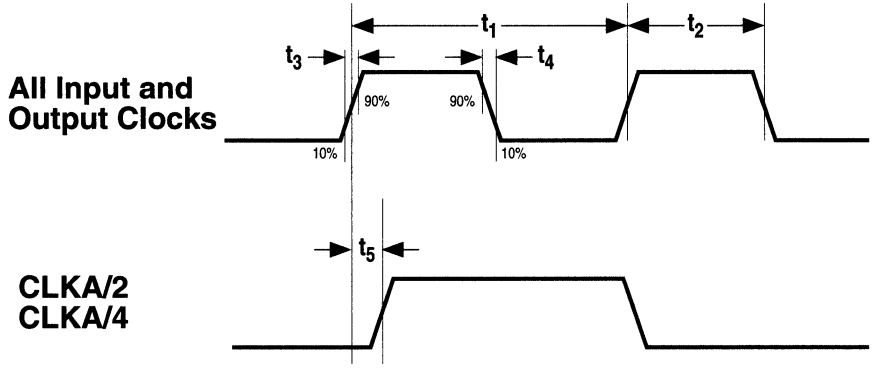
## Table 10: AC Characteristics

| Symbol | Name | Description | Min | Max | Units |
|---|---|---|---|---|---|
| $t_1$ | ref freq | Reference Oscillator nominal value | 1 | 60 | MHz |
| $t_2$ | duty cycle | Duty cycle for the output oscillators defined as $t_2 \div t_1$ | 40% | 60% | |
| $t_3$ | rise time | Rise time for the output oscillators into a 25pF load | | 3 | ns |
| $t_4$ | fall time | Fall time for the output oscillators into a 25pF load | | 3 | ns |
| $t_5$ | CLKA/2/4 skew | Skew delay between the CLKA output and the CLKA/2 & CLKA/4 outputs | | 2 | ns |
| $t_6$ | set-up | Delay required after MUXREF goes low prior to starting the SCLK clock line | $t_{freq1}$ | | ns |
| $t_7$ | cycle time | Minimum cycle time for the SCLK clock | $2 \div t_1$ | | ns |
| $t_{7H}$ | high time | Minimum high time for the SCLK clock | $1 \div t_1$ | | ns |
| $t_{7L}$ | low time | Minimum low time for the SCLK clock | $1 \div t_1$ | | ns |
| $t_8$ | clk stable | Time required for CLKA or CLKB oscillator to become valid after last SCLK clock | | 10 | msec |
| $t_9$ | set-up | Time required for the data to be valid prior to the rising edge of SCLK | 10 | | ns |
| $t_{10}$ | hold | Time required for the data to remain valid after the rising edge of SCLK | 5 | | ns |
| $t_{11}$ | transition | Time for CLKA or CLKB to go high after assertion of MUXREF | 0 | $t_{freq1}$ | ns |
| $t_{12}$ | transition | Delay of CLKA or CLKB prior to valid $t_{(REF)}$ signal at output | $\frac{t_{(REF)}}{2}$ | $3\frac{t_{(REF)}}{2}$ | ns |
| $t_{13}$ | transition | Time for CLKA or CLKB to go high after release of MUXREF | 0 | $t_{(REF)}$ | ns |
| $t_{14}$ | transition | Delay of CLKA or CLKB prior to valid $t_{freq2}$ signal at output | $\frac{t_{freq2}}{2}$ | $3\frac{t_{freq2}}{2}$ | ns |
| $t_{15}$ | 3-state | Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion | | 12 | ns |
| $t_{16}$ | clk valid | Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high | | 12 | ns |

**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

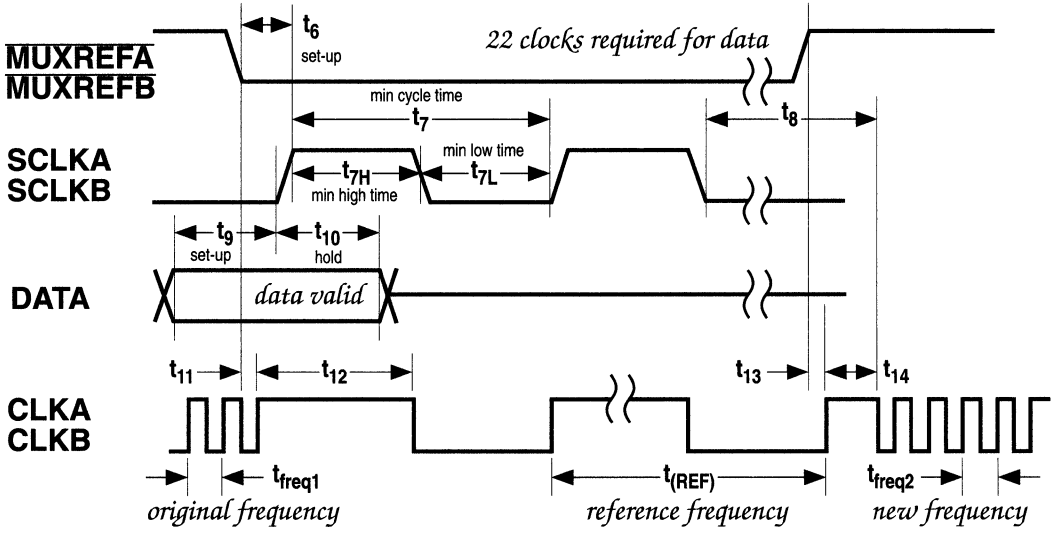
## Timing Diagrams

### Fig. 3: Rise and Fall Times

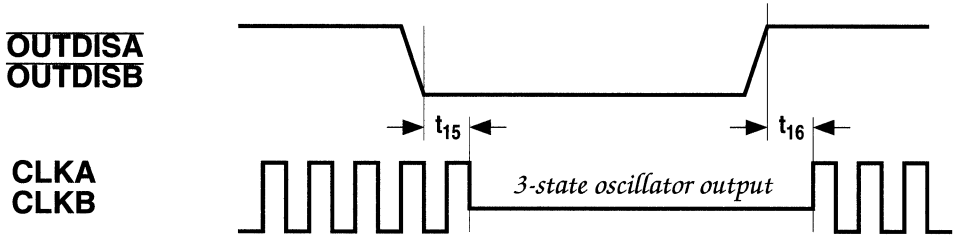





### Fig. 4: Serial Programming Timing



## Fig. 5: 3-StateTiming



# Revision History / Credits

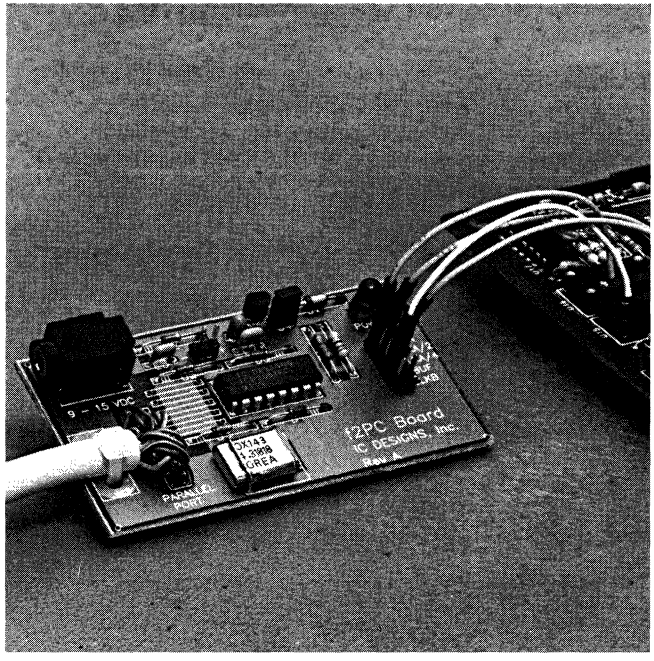
V2.5 (11/15/93) — Final Release Version

# f2PC Board

## High-Performance Frequency Generator

**Low-Cost High-Performance Frequency Generator Module for Your PC**

- **Accelerates System Design and Testing**
- **Programmable Frequency Range: 320 KHz – 120 MHz**
- **Emulates any Crystal Can Oscillator: Supplied Cable Provides Plug-In Compatibility**
- **Single- and Dual-Frequency Capability**
- **3-State Capability**
- **Controlled through Parallel Port of any DOS-Compatible Personal Computer**
- **Supplied Configuration Control Program to Set Frequencies**
- **Uses ICD2051 Dual Programmable Oscillator Chip**
- **Excellent Vehicle to Evaluate IC DESIGNS Frequency Synthesis Technology**



## General

The f2PC Board is an inexpensive yet highly accurate frequency generator which attaches directly to the parallel port of a DOS-compatible PC. Designed for the engineering lab bench, the f2PC Board delivers output frequencies from 320 KHz to 120 MHz. The f2PC Board can be used to prototype unusual or high-frequency crystal can oscillators which are expensive or hard to find — or it can function as a variable-frequency oscillator to test the operational limits of a prototype system.

## Emulates any Crystal Can Oscillator

The f2PC Board acts as an in-circuit emulator for any crystal can oscillator; its emulator cable plugs directly into the 4-pin footprint of the crystal can on the system board. The f2PC Board emulates both single- and dual-frequency crystal cans, including those with 3-state capabilities. Using the f2PC Configuration Control Program, one simply specifies the desired target frequency and the f2PC board automatically outputs that value to the system under test.

## Single-Chip Dual Oscillator Saves PCB Real Estate

At the heart of the f2PC Board is the ICD2051 Dual Programmable Oscillator device, a single-chip dual-frequency synthesizer. Using a single input frequency as a reference, it produces four output frequencies from two independently programmable oscillators (CLKA and CLKB). The ICD2051 is available as a catalog component from IC DESIGNS in a 16-pin SOIC package. Because it requires no external filter components, the ICD2051 takes up minimal real estate on a printed circuit board.

## Highly Accurate Frequency Synthesis

The output frequencies ($F_{out}$) synthesized by the ICD2051 are directly related to the input reference frequency $f_{(REF)}$ as follows:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where P and Q represent integers. For any programmed output frequency, the f2PC Board will always produce a highly accurate value well within 0.1% (1000 ppm) of the target.

## f2PC Board Product Contents

System Hardware — PCB and I/O Cables

- One (1) f2PC Board (3.1" x 1.7")
- One (1) parallel port host cable (6' long)
- One (1) 4-pin crystal can emulator cable (3" long)

System Software — Configuration Control Program (F2PC.EXE)

- 3.5" System Disk
- 5.25" System Disk

Documentation

- f2PC Board User's Guide
- ICD2051 Dual Programmable Oscillator Datasheet

## f2PC Board General Specifications



| | |
|---|---|
| *Technology* | Voltage-controlled oscillator with phase-locked loop and integrated loop filter |
| *I/O buffers* | CMOS |
| *Programming method* | 22-bit serial word |
| *Power supply* | Regulated: 5 VDC (±5%) — via emulator cable<br>Unregulated: 9–15 VDC — via wallbug |
| *Operating temperature range* | 0°C – 70°C |
| *Reference frequency* | 14.31818 MHz (external crystal) |
| *Dual channel outputs (all with 3-state control)* | Channel A: CLKA, CLKA/2, CLKA/4<br>Channel B: CLKB |
| *Output frequency range (CLKA and CLKB)* | 320 KHz – 120 MHz |
| *Accuracy*[a] | $f_{(OUT)} = 2 \times f_{(REF)} \times \frac{P}{Q}$ |
| *Host requirements* | Any IBM PC or compatible computer with parallel port |

a. P and Q are 7-bit counters. The f2PC Board normally produces an output frequency within 0.1% (1000 ppm) of the desired output frequency.

# Revision History / Credits

V1.3 (11/15/93) — Final Release Version

# QuiXTAL Embedded Crystal Products

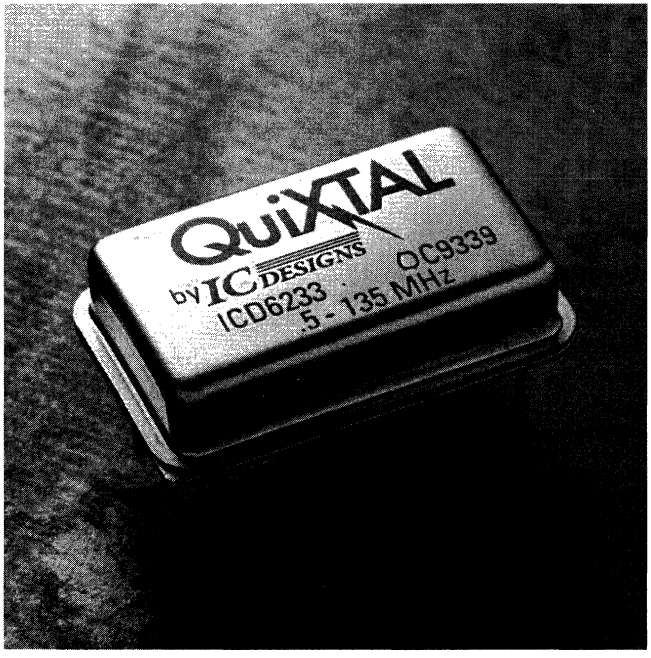
# 5 – QuiXTAL Embedded Crystal Products 265

# ICD6233

## One-Time Programmable Clock Oscillator

**HCMOS/TTL Metal Can Oscillator with One-Time Frequency Programmability**

- Industry Standard Package Footprint
- Frequency can be Programmed One Time to Values in a Wide Frequency Range (600 KHz – 120 MHz)
- Example Applications:
  - Replace Custom-Frequency Metal Can Oscillators
  - Reduce Time to Market
  - Prototype with Custom Frequencies
- Output can be 3-Stated
- Output Enabled if Pin 1 Left Floating
- Grounded Metal Cover Reduces EMI
- Internal Bypass Capacitors — no External Components Required
- Reduces Inventory Needs
- Drives 80386, 80486 & 68030 (10 TTL or 50pF)
- Sophisticated Internal Loop-Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 5V Operation CMOS Technology which Drives HCMOS and TTL Levels
- Available in 14-Pin Metal Can



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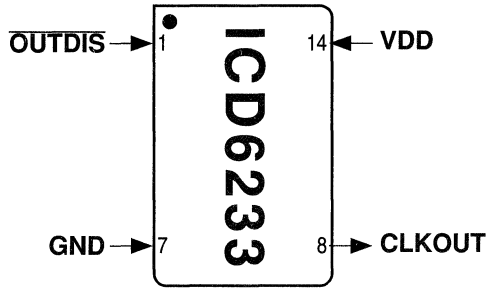
# Tables

# Introduction

The ICD6233 may be programmed one time for an output in the range of 600 KHz to 120 MHz. At manufacturing time, the desired output frequency is programmed by blowing an internal fuse-link PROM.

# Pin & Signal Descriptions

## Fig. 1: Pin Descriptions




## Table 1: Signal Descriptions

| Pin # | Signal | Function |
|---|---|---|
| 1 | $\overline{\text{OUTDIS}}$ –or– N.C. | 3-State disable CLKOUT; floats high (output enable) if No Connection |
| 7 | GND | Ground |
| 8 | CLKOUT | Clock Oscillator Output |
| 14 | VDD | +5 Volts |

# Ordering Information

## Table 2: Order Codes

| Part Number | Package Type | Temperature Range | Clock Output Options |
|---|---|---|---|
| ICD6233 | M = 14-Pin Metal Can | C = Commercial[a] | |

a. 0°C to +70°C

**NOTE:** Call IC DESIGNS at (800) 669-0557 and specify desired frequency (600 KHz – 120 MHz) and output (TTL or CMOS).

# Device Specifications

## Electrical Data

### Table 3: Absolute Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage relative to GND | 4.75 | 5.25 | Volts |
| $V_{IN}$ | Input voltage with respect to GND | –0.5 | $V_{DD}$ + 0.5 | Volts |
| $T_{STOR}$ | Storage temperature | –55 | +125 | °C |
| $T_{SOL}$ | Max soldering temperature (10 sec) | | +260 | °C |
| $P_{DISS}$ | Power dissipation | | 375 | mWatts |

**NOTE:** Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

**OPERATING RANGE:** $V_{DD}$ = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

### Table 4: DC Characteristics

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | | 5.0 | mA | $V_{DD}$ = Max, 3-state |
| $V_{OH}$ | Output High Voltage | 2.4 | | V | $I_{OH}$ = -4.0 mA |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 4.0 mA |
| $V_{IH}$ | Input High Voltage | 2.0 | | V | |
| $V_{IL}$ | Input Low Voltage | | 0.8 | V | |
| $I_{IH}$ | Input High Current | | 100.0 | µA | $V_{IH}$ = $V_{DD}$ |
| $I_{IL}$ | Input Low Current | | -250.0 | µA | $V_{IL}$ = +0V |
| $I_{OZ}$ | Output Leakage | | 10.0 | µA | 3-state |

## Table 5: AC Characteristics

| Symbol | Name | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_2$ | output period | 5V operation | 7.4<br>135 MHz | | 1666.7<br>600 KHz | ns |
| $t_3$ | output duty cycle | Duty cycle for output pads<br>($t_3 \div t_2$ @ CMOS $V_{TH}$ of $V_{DD} \div 2$) | 40 | | 60 | % |
| $t_4$ | rise time | Output oscillator rise time | | | 3.5 | ns |
| $t_5$ | fall time | Output oscillator fall time | | | 3.0 | ns |
| $t_7$ | power-up | Time for output to become valid | | 10 | 15 | msec |

**NOTE:** Input capacitance is typically 10pF, except for the crystal pads.

# Revision History / Credits

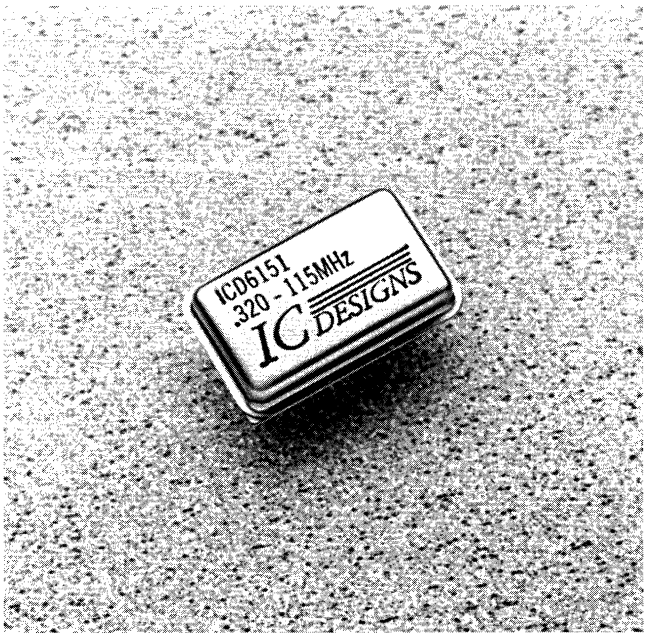
V1.1 (11/15/93) — Final Release Version

# ICD6151

## Dual Programmable Clock Oscillator

**Single-Chip Dual Programmable Oscillator Replaces Traditional Can Oscillators in Multi-Frequency or Variable Frequency Environments**

- 2 Independent Programmable Clock Outputs (A & B) Ranging from 320 KHz – 115 MHz
- Individually Programmable Oscillators Using a 22–bit Serial Word
- Low-Skew ÷1, ÷2 and ÷4 CLKA Outputs, as well as Reference Frequency (XBUF)
- Glitch-Free Frequency Transitions
- HCMOS Levels
- 3-State Enable/Disable
- Low Power Consumption Makes Device Ideal for Power and Space Critical Applications
- Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- 5 Volt Operation
- Available in 14-Pin Metal Can

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# ICD6053

## 3-State HCMOS Programmable Clock Oscillator

**Single-Chip Programmable Oscillator Replaces Traditional Can Oscillators in Variable Frequency Environments**

- **Frequency Range: 360 KHz – 120 MHz**
- **Programmable Oscillator Using a 2-Wire Serial Interface**
- **Glitch-Free Frequency Transition**
- **Low Power Consumption Makes Device Ideal for Power and Space Critical Applications**
- **Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters**
- **HCMOS Levels**
- **3-State Enable/Disable**
- **5V Operation**
- **Available in 14-Pin Metal Can**


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# Application Notes

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# Figures



# Tables

# Power Feed and Board Layout Issues

## Introduction

The IC DESIGNS monolithic oscillator family offers new approaches to PC board clock generation. Outputs can be changed "on the fly" from below 1 MHz to above 120 MHz (depending on the device); some devices have multiple output channels.

The benefits can only be realized, though, if adequate attention is paid to grounding, layout and bypass issues. Guidelines for these issues are covered in this Application Note.

## Ground Plane

Ground is an extremely important circuit reference, but at VHF frequencies, a routing trace will normally not reference exactly the same voltage at different points along its length.

Ground planes perform well at high frequencies. The 100% metal area inhibits the appearance of noise voltage. On a 2-layer board, IC DESIGNS requires a ground plane on the component side, with routing on the solder side.

"Cutting out" the plane around the chip is theoretically justified, since it isolates noise appearing across the plane; however, such noise is usually low enough to make a local cut-out unnecessary.

All ground pins on the chip (analog and digital) should be tied directly to this plane.

## Supply Bypass Values



With the chip ground established, the next issue is applying power. The supply should be as clean and quiet as possible, since supply variations affect oscillators and reduce output purity.

Some IC DESIGNS products include both analog and digital power pins. More noise can be tolerated on digital than on analog power, since the analog power feeds the synthesizer core.

At a digital power pin, high-frequency noise will be reduced sufficiently with an ordinary 0.1µF ceramic bypass capacitor. The bypass should be located very close to the chip, i.e., within 0.1" to 0.2".

With analog power pins or devices with a single power pin, a parallel combination of low and high value capacitors yields the best results (2.2µF/0.1µF, or 2.2µF/.01µF), because the capacitors are then resonant at different frequencies.

## Supply Filters

Supply bypass suppresses high-frequency noise to a degree, but noise at kiloHertz frequencies can still pose a problem. Disk drives, for example, can cause supply shifts that degrade output purity.

To deal with these problems, IC DESIGNS recommends some form of power supply filtering.

One fairly basic technique is to use a 22Ω resistor in series in conjunction with a 2.2µF tantalum capacitor to ground. This RC filter will attenuate lower-frequency noise. The tantalum capacitor should be paralleled by a smaller one (see *Supply Bypass Values* on page 281). This method works well if the pin draws a moderate current (such as analog $V_{DD}$ pins); at currents in the 25 mA range or above, supply drop may be a problem unless special arrangements have been made with IC DESIGNS.

Another technique involves drawing from a +12V supply. Such a supply has inherently lower noise, and if it is fed to a Zener diode through a series resistor, the supply noise rejection is very high. A possible combination is a 5.1V 1N5231B and a 180Ω resistor. Bypass to ground should be included just as with the 22Ω series resistor. (See *Table 1: Recommended Bypass Diagram* on page 283 and *Bypass Diagram Examples* on page 284.)

The most effective technique is to install a three-terminal regulator such as a 78L05, operating from +12V. With suitable bypass capacitors, virtually no noise will get through from DC to high frequencies.

## Sockets

Sockets are often necessary during development, and the IC DESIGNS synthesizers are tolerant of them. But for production boards, sockets are not recommended, since extra lead length leads to more noise and reduces output signal purity.

## Placement

After the power conditioning parts are tightly placed, the next important consideration is to place the synthesizer near the devices to be clocked.

Even though the IC DESIGNS part produces a clean signal, it will not remain so if transmitted carelessly. Long routings lead to ringing, phase shift and level variations. IC DESIGNS recommends placing the part with a maximum run of 3–4 inches, less if possible. It is also important to isolate the output trace(s) as much as possible from parallel signal runs.

### Table 1: Recommended Bypass Diagram

| Device | Fig. 1 | Fig. 2 | Fig. 3 |
|---|---|---|---|
| ICD2023 | √ | | √ |
| ICD2025 | √ | | √ |
| ICD2027 | √ | | √ |
| ICD2028 | √ | | √ |
| ICD2042A | √ | | √ |
| ICD2051 | | √ | |
| ICD2061A | √ | | √ |
| ICD2062A/B | √ | | √ |

## Bypass Diagram Examples

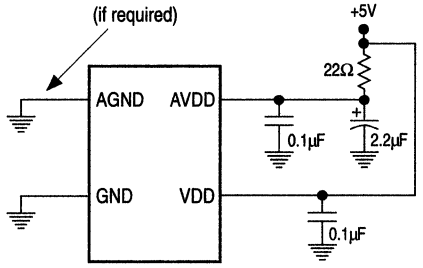


**Fig. 1: Separate Analog/Digital Supply Devices**

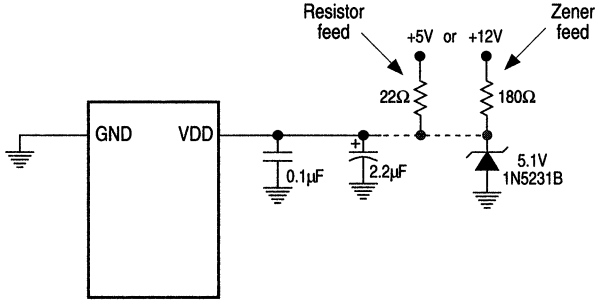


**Fig. 2: Combined Analog/Digital Supply Devices**

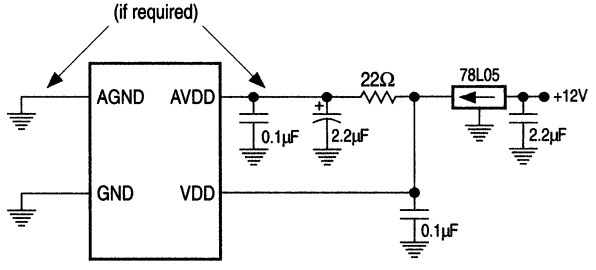


**Fig. 3: Using a Three-Terminal Regulator**

# Minimizing Radio Frequency Emissions

## Introduction

The United States stringently tests all new electronic products for RF emissions through FCC Part 15. As digital clock signals approach broadcast frequencies (The FM radio band is 88-108 MHz), proper attention to design and layout becomes increasingly important.

## Harmonics and their Suppression

Much of the difficulty lies in the square-wave nature of digital clock signals. It is usually not the fundamental, but rather the odd harmonics, which radiate the most. This means that an 80 MHz design might fail, not at 80 MHz, but rather at 240 MHz. These higher frequencies are difficult to predict, and so a solution can only be found by repeated testing of various design techniques. These techniques will minimize radiation of the higher-frequency harmonics.

## Good Design Practice

Good power supply bypassing and tight layout technique are important: bypass capacitors tight against the power pins; ground connections directly contacting a full ground plane. Please refer to the individual data sheets, as well as to the Application Note titled *Power Feed and Board Layout Issues* on page 281.

It is good practice to load oscillators as lightly as possible. Load capacitance increases switching currents and increases emissions from the power supply. One should never deliberately add output capacitance.



Possibly the most important technique is to limit the trace length of the highest-frequency signal, which should run 1–2" at most; every additional inch makes a trace a more effective antenna. This effect may be modest at frequencies in the 10–20 MHz range, but might cause failure with 50–100 MHz clocks.

It is crucial that the system be on a ground plane. Traces make much poorer antennae if they lie over a continuous sheet of ground. Unfortunately, two-sided boards are more likely to fail emissions testing.

## Output Series Loading

Output harmonics can be reduced by adding series resistance or a ferrite bead. The added impedance reduces the harmonics in the output signal, also improving the termination of reflected signals in the output. Since ferrite beads are more expensive, a series resistor could be tried first. This should be at least 22Ω, more if circumstances allow—keeping in mind that too much resistance (greater than 150Ω) can lead to unacceptably low logic levels. To check this, take the series-R, estimate the capacitive load C, and verify the following:

$$F_{clock} \leq \frac{1}{(2\pi \cdot R_{series} \cdot C_{load})}$$

The above is just a general guideline. One can also observe the final digital clock waveform by using low-capacitance active probes, raise R until failure occurs, then use a significantly lower value.

One should place series loads by the clock generator, since they are largely ineffective farther down the trace length. REMEMBER: these parts are usually not necessary, but it is good strategy to include them if RF testing becomes a problem.

## Product Level Enhancements

If the problem is unaffected by board-level changes, one can often improve the product cabinetry. For example, plastic panels can be made conductive with a spray coating, keypads can be shielded.

Emissions often travel through the power supply and out via the power cord. A large internal ferrite bead on the power feeds may get the device through testing. The test lab staff can often help with such quick fixes.

## Concluding remarks

Above all, keep in mind that the clock generator by itself neither passes nor fails emissions. Passing or failure is based on cumulative performance, including bypass, board layout, supply wiring, product packaging, output frequencies and application.

Careful procedure and good design practice will ensure that compliance is attained.

## Typical Implementation (Using ICD2023 as Example)

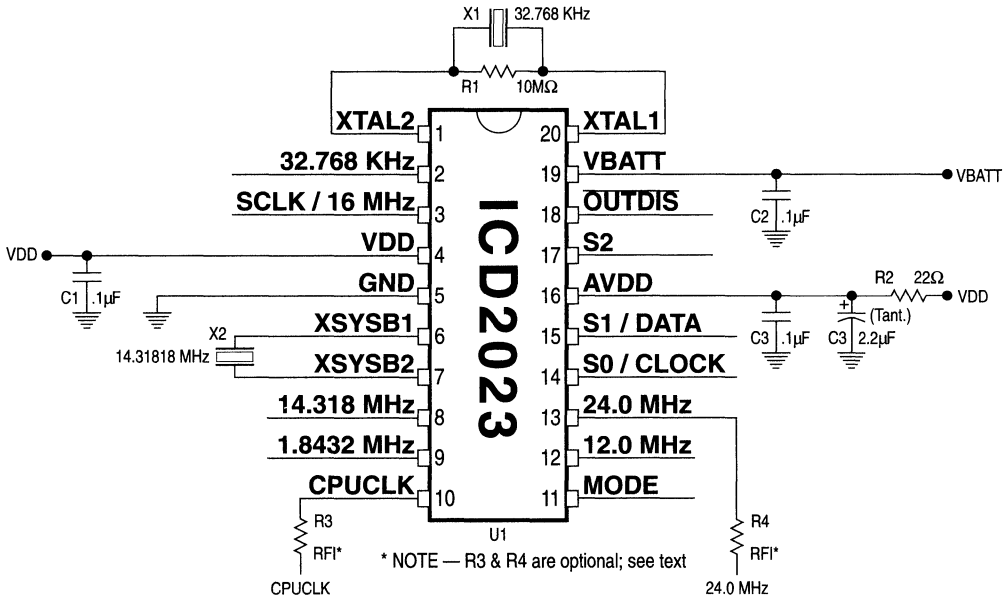


**Fig. 4: Schematic Diagram**

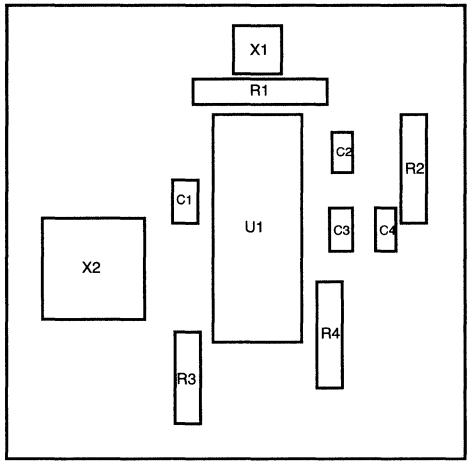


**Fig. 5: Parts Layout**

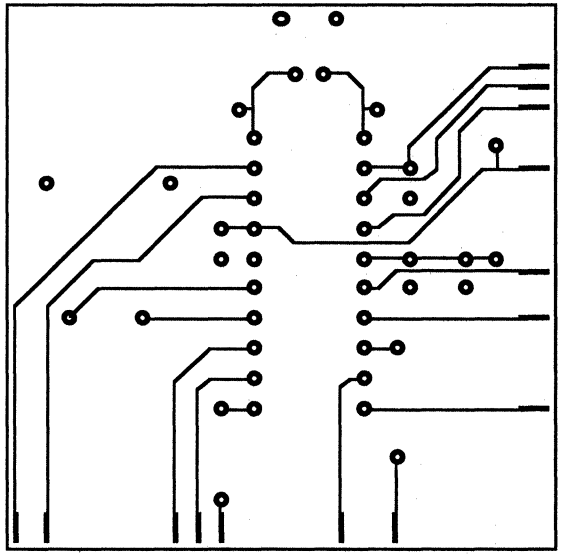

Fig. 6: PC Board (Back)

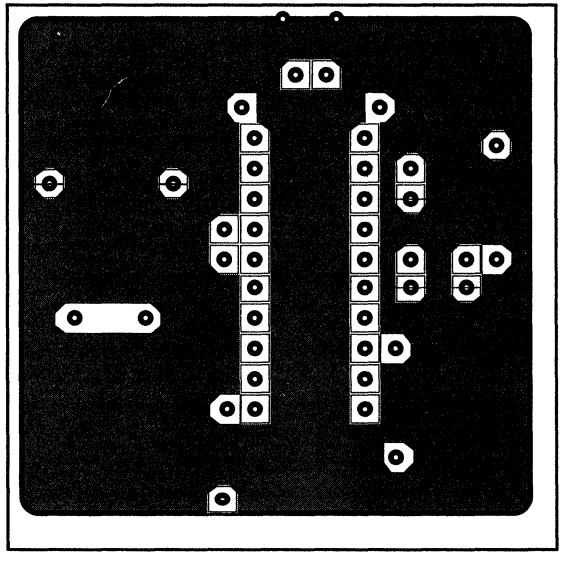

Fig. 7: PC Board (Front)

# ECL Outputs

## Introduction

The IC DESIGNS oscillator family features ECL-compatible outputs in products such as the ICD2062. These outputs allow clocking at frequencies above 160 MHz, with all the inherent advantages of differential ECL signal transmission.

This Application Note covers the principal advantages of using ECL outputs and makes recommendations concerning layout and wiring methods for parts such as the ICD2062.

## Power Supplies (PECL vs. ECL)

The ECL VDD and VEE pins have traditionally been powered from a –5.2V supply, $V_{DD}$ being grounded and $V_{EE}$ set at –5.2V — the intent is to achieve the lowest $V_{DD}$ noise by grounding the $V_{DD}$ pins. In more recent designs, however, ECL is often used with +5.0V instead of –5.2V. Since $V_{DD}$ noise is not a major concern, this permits the use of a standard logic supply. This Application Note will focus on +5.0V ECL designs (sometimes called PECL).

## ECL Advantages

As clock speeds rise beyond 100 MHz, the advantages of using ECL become more obvious. Most of these advantages involve the use of differential signal transmission.

Differential signals are less susceptible to ground noise problems, as all noise becomes common-mode. Single-ended CMOS is much more susceptible, since ground bounce and other noise affect logic thresholds, degrading noise immunity. ECL signals remain unaffected, since noise rides on both signals as an average level. Logic levels are also less critical, since the threshold is a differential zero volts, which can tolerate significant signal attenuation. Differential circuits also tend to generate less noise in the power supply.

ECL is designed with termination resistors which allow high-frequency signals to propagate with minimal overshoot and reflection.

These advantages are most pronounced in a bipolar implementation, but many of the same benefits can be realized in CMOS designs.

## Pad Structure

Referring to *Fig. 8: Differential ECL Output Driver* on page 291, transistors Q1 and Q2 form differential ECL output drivers. Unlike single-ended outputs (See *Fig. 9: Single-Ended Output Driver* on page 291), N-type transistors are not required, since termination resistors are always present and serve as pull-downs.

The ECL output drive logic guarantees that, when Q1 switches ON, Q2 switches OFF (and vice-versa), A complementary logic state is always maintained, assuring a constant supply draw in either output state.

## Logic Levels

The differential logic swings are approximately 4.5V to 3.0V. This is more than adequate, since bipolar ECL is typically 4.3V to 3.2V. If the termination resistors are reduced from the 220Ω/330Ω suggested values, the high-side swing can be reduced somewhat.

## Output Routing and Board Layout Issues

ECL signals maintain their integrity over long routing distances. A 100 MHz single-ended trace should be limited to a few inches, but ECL can travel several feet at that frequency. This is due to ECL's termination resistors at the receiving devices.

For good signal integrity, ECL traces are laid out in pairs, with a small separation (about a trace width); this results in a characteristic impedance of 100–150Ω. This transmission line layout also helps minimize RF emissions, since the differential signal fields cancel when closely routed over a ground plane.

The clock generator must be bypassed at the supply pins, as should the parts to be clocked. Terminating resistors should also be bypassed separately if they are not located near a bypass capacitor.

## Terminating Resistor Values

The 220Ω/330Ω values represent a trade-off between low power draw and best high-frequency performance. For frequencies above 80 MHz, they may pull down too weakly, resulting in inadequate signal swing. These values can go as low as 68Ω/100Ω at 160 MHz (always maintaining an approximate 2:3 ratio). Low values work satisfactorily at both low and high frequencies, the only drawback being a higher current drain.

## Summary

A general overview of ECL logic has been presented, with emphasis on the interface of ECL logic to +5V powered CMOS clock generators. Should additional support be required, contact IC DESIGNS for assistance.

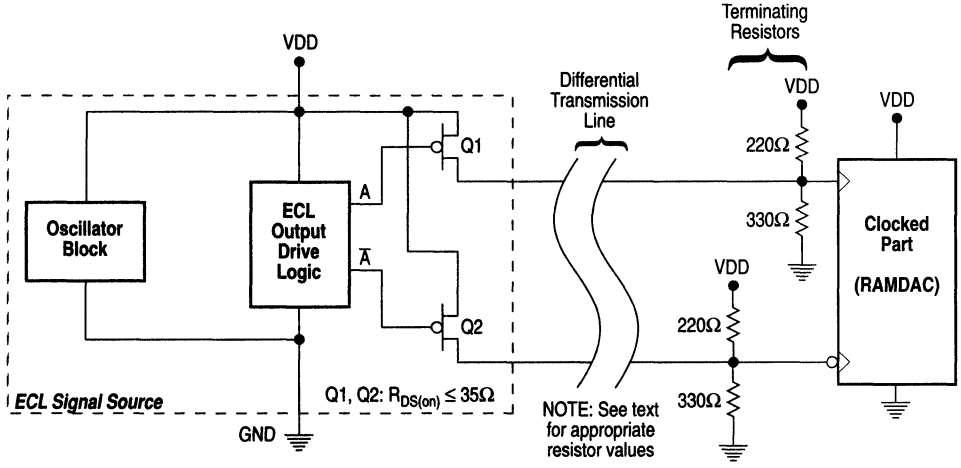


**Fig. 8: Differential ECL Output Driver**



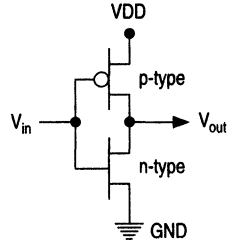


**Fig. 9: Single-Ended Output Driver**

# Crystal Oscillator Topics

## Parallel vs. Serial Resonant Oscillator Circuits

All frequency synthesis components from IC DESIGNS require a reference frequency, usually provided by a quartz crystal. The on-board crystal oscillators are parallel-resonant designs. Although most oscillator circuits are designed to use parallel-resonant crystals, most inexpensive "off-the-shelf" crystals are series-resonant devices. Accordingly, many oscillator applications (such as CPU clock/timer designs) often run about 0.05% too fast.

When a crystal is manufactured, the manufacturing specs must specify the type of oscillator circuit in which it is intended to be used. The two types will result in a difference in the output frequency of approximately 500 ppm (0.05%). To guarantee accurate output, the spec must therefore take this difference into account when the crystal is manufactured.

For maximum accuracy, a parallel-resonant crystal of the proper specification will be required. Whether or not the extra cost is justified depends on the application. In many cases, an error of 0.05% is acceptable; in applications such as time-keeping, however, it often is not.

## Specifying a Custom Parallel-Resonant Crystal

To order a specially made crystal, the correct spec to give the vendor is parallel-resonant, plus a value for the load capacitance presented by the oscillator. As an example, the correct specification crystal oscillator would read as follows:

Type = Parallel-resonant
Freq = 14.31818 MHz
$C_{load}$ = 17pF

As an alternative to a custom crystal, parallel-resonant crystals with a specified $C_{load}$ = 20pF may be available from dealer stock. Such a crystal may be a viable alternative to a custom crystal, offering only slightly less accuracy at lower unit cost.

# Accuracy Considerations for Time-Keeping in PC Design

Time-keeping is a stringent application, where a 50 ppm error in reference frequency produces a real-time clocking error of 2 minutes per month. In many personal computer applications, both 32.768 KHz and 14.31818 MHz are used for time-keeping. Highly accurate values of both these frequencies are therefore required.

Most IC DESIGNS frequency synthesis components produce a 14.31818 MHz signal on one or more output pins. However, as previously pointed out, the accuracy of these outputs will depend upon proper specification of the 14.31818 MHz reference crystal by the designer. Correctly specifying the reference crystal is therefore important in time-keeping applications.

Some IC DESIGNS components also offer an additional output from an on-board 32.768 KHz oscillator. This oscillator is designed to work with an industry-standard 32.768 KHz crystal specified as parallel-resonant, $\mathbf{C_{load}}$ **= 12pF** and is readily available from dealer stock, so the resulting output should always be accurate enough for time-keeping applications.

# Selecting a High-Accuracy Reference Crystal

## Background

Our monolithic oscillator products deliver a wide range of output frequencies, replacing many individual quartz oscillators. And yet, *one* quartz crystal is needed to set the reference frequency, usually 14.31818 MHz. In this section, the emphasis is on maximizing the accuracy of the reference. Specific part numbers will be named, and a worst-case analysis performed.

## Changing Requirements

IC DESIGNS' earliest design-ins did not specifically recommend a parallel-resonant crystal instead of the more common (but less suitable) series-resonant type. Such designs tended to have error rates of 500–600 ppm.

This was acceptable at the time because VGA monitors can tolerate a pixel frequency deviation of 1% from nominal (10,000 ppm!), so reference accuracy was not an major factor.

Today, however, IC DESIGNS' expanding product line targets many time-critical applications, such as Ethernet systems, where the reference frequency must be held within ±100 ppm over the operating temperature range.

### Crystal Specifics

Earlier in this App Note, we recommend specifying a parallel-resonant crystal, with load capacitance ($C_{load}$) of 17–20pF. Here are some specific part numbers for surface-mount devices:

- **Fox Crystal # FPX143-20** — With $C_{load}$ = 20pF, it is close enough to our 17pF spec to be only 35 ppm high. If a tighter initial accuracy is desired, one can add two external load capacitors to ground, or specify a different load capacitance. Telephone: (813) 693-0099.
- **Epson America # MA-506 14.318M-B** — This sells off-the-shelf with $C_{load}$ = 16pF. In our lab, we find them to be nominally on target; they are the best off-the-shelf match available. Telephone: (310) 782-0770.

### Drive Level Precautions

Any quartz crystal is subject to mechanical failure if oscillated at an excessive voltage level. For a CMOS amplifier, the drive level is around 700µW. However, the parts are tested at 100µW; fortunately, a maximum rating exists of 1000–2000µW.

DO NOT use any crystal which does not have a 1000µW rating! It may drift excessively, or even become a delayed failure mechanism.

### Ethernet Error Budget Analysis

We can guarantee ±100 ppm worst case with the Epson #MA-506 14.318M-B. This is important for products like the ICD2028. To verify this, one simply adds up the relevant sources of error in an error budget (This is true for any crystal.):

| SOURCE OF ERROR | AMOUNT |
|---|---|
| Crystal frequency tolerance | ± 50 ppm |
| Crystal temperature tolerance | ± 30 |
| ICD2028 frequency tolerance | ± 05 |
| ICD2028 temperature tolerance | ± 06 |
| ICD2028 supply tolerance | ± 03 |
| | ± 94 ppm |

Since this is close to the limits, one can also look at a (well respected) "Monte Carlo Analysis," which says that, if a number of uncorrelated variables are changing randomly, it is not reasonable to add up the individual worst-case figures to come up with an aggregate worst-case value.

Instead, if one has n variables, X1, X2, ... Xn, all varying randomly and independently, then the overall variation is:

$$X_{total} = \sqrt{X_1^2 + X_2^2 + \ldots + X_n^2}$$

According to this calculation, the design will remain within 59 ppm, which will be trouble-free in production.

# Externally Driven Crystal Oscillator

## Introduction

Most IC DESIGNS products include a reference oscillator. XIN and XOUT pins interface the crystal to an on-chip amplifier and loading capacitors.

In many cases, the part is not tied to a crystal, but is instead driven from an external signal source. In such cases, it is recommended that the signal be coupled via a small series capacitor.

This document describes the benefits of a coupling capacitor, as well as other associated considerations.

## Benefit: Reduced Loading of the Signal Source

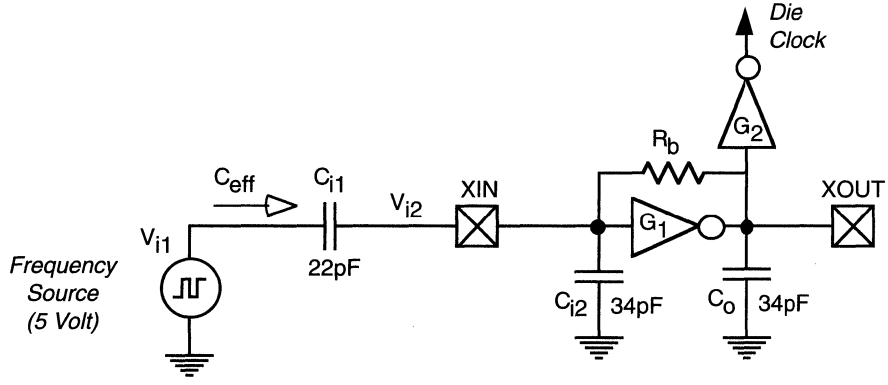


**Fig. 10: Reduced Signal Source Loading**

As can be seen, the two internal capacitors are each 34pF; if $C_i1$ is not present, this means that the frequency source effectively drives $C_{eff}$ = 34pF, where $C_{eff}$ is the effective load capacitance seen by the driver.

Adding $C_{i1}$ makes $C_{eff}$ a series combination of $C_{i1}$ and $C_{i2}$, which reduces $C_{eff}$ according to the formula:

**Equation 1:**
$$C_{eff} = \frac{C_{i1} \cdot C_{i2}}{C_{i1} + C_{i2}}$$

Substituting $C_{i1}$ = 22pF and $C_{i2}$ = 34pF results in a $C_{eff}$ of 13.4pF

In the above example, $C_{eff}$ is reduced by 62%, which results in less loading of the frequency source, less power supply noise and thus improved signal transition times.

## Consideration: Reduced Signal Amplitude

The only penalty is reduced signal amplitude at XIN according to the formula:

**Equation 2:** $$V_{i2} = V_{i1} \cdot \frac{C_{i1}}{C_{i1} + C_{i2}}$$

Substituting $C_{i1}$ = 22pF, $C_{i2}$ = 34pF and $V_{i1}$ = $5V_{PP}$ results in a $V_{i2}$ of $2.0V_{PP}$.

In the example above, the amplitude has been reduced to $2V_{PP}$ at XIN, but this is not a problem, since the linear inverter $G_1$ biases and re-amplifies the signal.

## Benefit: Restoration of Duty Cycle

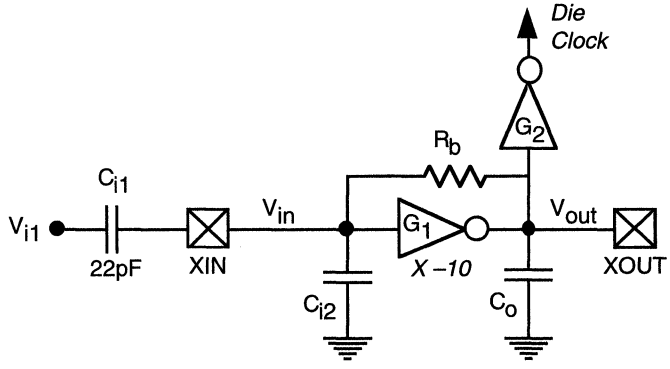


**Fig. 11: Duty Cycle Restoration**

In the above schematic, $G_2$ buffers the XOUT signal for use on the die. $G_1$ and $G_2$ have matched characteristics. The inverting gain is roughly 10, and biasing for $V_{in} = V_{out}$ is close to $V_{DD} \div 2$.

The matched characteristics and the R-C components work to restore the duty cycle, the mechanism being the AC gain of roughly –10 and its effect on DC biasing. The XOUT DC level is fed back to XIN via resistor $R_b$. The resultant feedback loop is stable with a gain of 10, regulating the average DC level of XOUT.

The restored duty cycle can be seen after it has been through $G_2$; on most devices, this is the XBUF pin.

## Proof of Performance

The above has been seen to work well at various design-ins. Rather than attempting a rigorous mathematical proof, however, we have opted for substantiating the performance in a conceptual manner. Some proof is needed, since a sharp square wave at XOUT would not be duty-cycle regulated. $G_2$ could not alter the timing of steep transients.

For duty cycle regulation to occur, the waveform at XOUT must be "well-rounded". This is achieved by the load capacitor $C_o$ and by the high output impedance of $G_1$ (which is approximately 1KΩ).

If the waveform at XOUT has a duty cycle in the vicinity of 50% (about 35–65%), and if it is well-rounded, then the output waveform will be biased up or down by the feedback biasing effects.

The regulation is not perfect, but in practice the output remains close to 50% over a wide variation in input waveform values.

## Consideration: Capacitor Value

Duty cycle regulation is reduced by $G_1$ saturating near $V_{DD}$ or Ground. To keep $G_1$ linear as much as possible, $C_{i1}$ should not be too large; a smaller $C_{i1}$ reduces signal amplitude, thus improving linearity. Values in the range 10–22pF may be used, although at 10pF, the signal may become noise corrupted. For best results, one should keep the part well bypassed and locate $C_{i1}$ as close as possible to the XIN pin.

## Consideration: 3V Input Waveform

Sometimes the reference signal is part of a 3V system, with an IC DESIGNS part running on 5V; this is another situation in which capacitor coupling is recommended. With the device and the reference driver powered by 5V, good results can be obtained with $C_{i1}$ = 22pF. The resultant amplitude at XIN is 2VPP.

If the input signal amplitude is $3V_{PP}$, IC DESIGNS prefers to maintain a 2VPP amplitude at XIN. The pertinent formula is *Equation 2:* on page 296, which calculates reduced signal amplitude.

Using $C_{i1}$ = 68pF, $C_{i2}$ = 34pF and $V_{i1}$ = 3VPP, this yields a value of $V_{i2}$ = 2VPP.

Thus, we recommend a value of 68pF. The designer should verify the waveforms with an oscilloscope, making any needed design-specific changes.

# Revision History / Credits

V1.6 (11/15/93) — Final Release Version

# Quality Assurance and Reliability

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# Contents

# Introduction

IC DESIGNS is an industry leader in frequency synthesis technology and custom-designed programmable clock generators for personal computers and mass storage systems. This achievement has been the result of creative design and emphasis on product excellence. Now a division of Cypress Semiconductor, IC DESIGNS gains added support for product excellence. Cypress Semiconductor is a leader in the design, development and manufacture of a broad line of high-performance digital integrated circuits, using proprietary 0.65- and 0.8-micron CMOS and BiCMOS technologies.

Cypress corporate views for quality and reliability are shared by IC DESIGNS. Product excellence does not occur by merely following the industry norms: it begins by being better than one's competitors, with better designs, processes, controls and materials.

Some of the techniques used to ensure product excellence are the following:

- Product reliability is built into every product design, starting from initial design conception.
- Product quality is built into every step of the manufacturing process by the use of statistical process control and inspections at critical process steps.
- Quality inspections and reliability performance checks are performed on finished product to ensure that finished product quality requirements are met.
- Field data test results are encouraged and tracked so that accelerated testing can be correlated to actual use experiences.

## Product Design and Development

The design and development process at IC DESIGNS follows defined procedures. These procedures assure that each step of the product development cycle results in a product that provides customer satisfaction at an acceptable price, while at the same time building in the highest quality and reliability.

## Product Qualification Testing

The quality of each new product is verified by qualification testing in three areas:

a) **Process Qualification:** Extensive qualification testing is performed by the silicon foundry. Step stress testing on standard evaluation circuits processed with the particular wafer fabrication flow is reported quarterly.

b) **Die/Design Qualification:** All product designs are qualified by IC DESIGNS. Reliability is verified by subjecting devices to high-temperature operating-life test, electrostatic discharge susceptibility and latch-up resistance.

c) **Package Qualification:** All packages used with IC DESIGNS' products are subjected to an initial qualification consisting of a full spectrum of electrical and environmental stress tests. Periodic monitoring is performed to ensure quality and reliability.

## Product Quality

Customer satisfaction and continuous quality improvement are the primary goals of the quality program at IC DESIGNS. The IC DESIGNS Quality Management System has been designed to meet the program requirements of MIL-Q-9858 and ISO 9001. Key objectives of the System are to:

- achieve, maintain and continuously improve the quality of IC DESIGNS' products in relationship to the requirements for quality;
- improve the quality of its own operations, so as to meet all the customer's stated and applied needs;
- provide confidence to internal management that the requirements are being met and maintained, and that quality improvement is taking place;
- provide confidence to the customer that the requirements for quality are being, and will be, fulfilled in the finished product.

## Subcontractor Manufacturing Controls

Since the manufacture of IC DESIGNSs products is carried out by wafer fabrication and assembly subcontractors, an essential part of the Quality Management System consists of ensuring that processing adheres to the high quality and reliability standards required by that system. The IC DESIGNS Subcontractor Manufacturing Controls Specification establishes standards which the subcontractors must agree to uphold. The requirements of this specification apply to: procurement of raw materials, process documentation, use of statistical process control, assembly process monitoring, quality conformance testing, handling of nonconforming material and corrective action procedures. With these controls, and with the pre-qualification auditing of new subcontractors prior to their inclusion on the Approved Suppliers List, the customer is assured of high-quality products.

## Product Reliability Monitoring

In addition to qualification testing, ongoing process monitoring programs are conducted to ensure that all products comply with the established goals for reliability. Usually, these evaluations consist of operating life test and humidity & temperature cycling. The testing is summarized each quarter and is available to customers.

Statistical process control of assembly operations is summarized each month. This control data is generated for each process in the assembly flow. In addition, reliability monitoring is conducted on a sample basis, where devices are subjected to autoclave, temperature cycle, dye penetration, vapor phase and lead integrity.

## Electrostatic Discharge Susceptibility

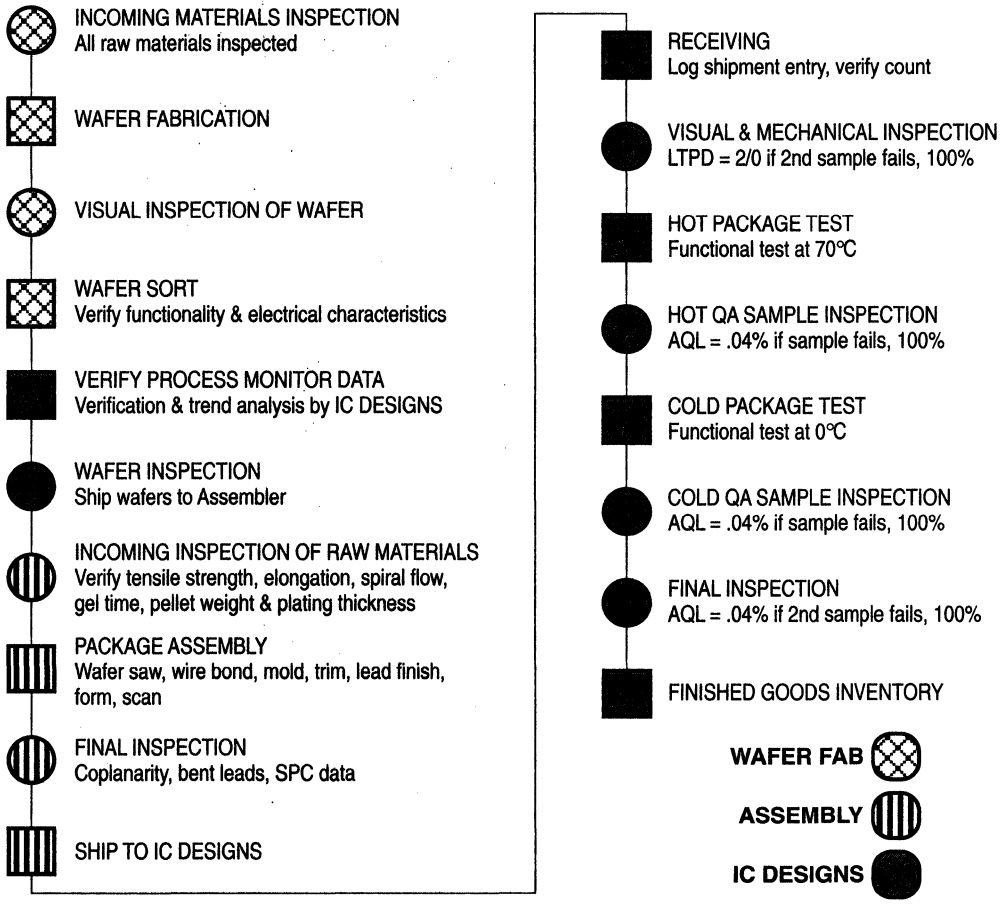
Electrostatic discharge (ECD)-induced failure has been a generic problem for many high-performance MOS and bipolar products. Although MOS technology experienced oxide reliability failures in its earliest years, this problem has largely been eliminated by means of improved oxide growth techniques and a better understanding of the ESD problem. The effort to protect adequately against ESD failures is per-

turbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress and IC DESIGNS have developed ESD protective circuitry specific to 1.2-, 0.8-, 0.65- and 0.5-micron CMOS process technology.

IC DESIGNS products are designed to withstand voltage and energy levels found during a typical electrostatic discharge event. However, the user is cautioned to always use the accepted ESD grounding and handling procedures when removing devices from ESD-protected packaging and during subsequent handling.

## Product Flow Chart

Manufacturing and test operations applicable to IC DESIGNS products are diagrammed on the following flow chart. Quality control inspections are represented by circles, while manufacturing and test operations are represented by squares.



## General Testing Philosophy

This is a summary of the methods which IC DESIGNS uses to guarantee the AC and DC characteristics specified in the datasheets included in this publication.

The following parameters are guaranteed by production testing (wafer sort and final test) with proprietary PC-based testers designed and supported by IC DESIGNS:

| Name | Description |
|---|---|
| $I_{DD}$ | Power Supply Current |
| $t_2$ | Output Period |
| $t_3$ | Output Duty Cycle |
| $I_{OZ}$ | Output Leakage Current |
| $V_{IH}$ | Input High Voltage |
| $I_{PD}$ | Power-Down Current |
| $I_{BATT}$ | Battery Stand-by Current |
| $V_{IL}$ | Input Low Voltage |
| $I_{IH}$ | Input High Current |
| $I_{IL}$ | Input Low Current |

The following parameters are tested initially and after any design or process changes that may affect these parameters:

| Name | Description |
|---|---|
| $C_{IN}$ | Input Capacitance |
| $t_{(REF)}$ | Reference Clock Period |
| $t_4$ | Output Rise Time |
| $t_5$ | Output Fall Time |
| $t_6$, $t_8$ | Leading Edge Skew |
| $t_{VCO}$ | Settle Time |
| $t_{14}$ | Time to invoke power-down option |
| $t_{15}$ | Time to revoke power-down option |
| $V_{OH}$ | High-Level CMOS Output |
| $V_{OL}$ | Low-Level Output |

# Revision History / Credits

V1.4 (11/15/93) — Final Release Version

# Package Information

# Contents

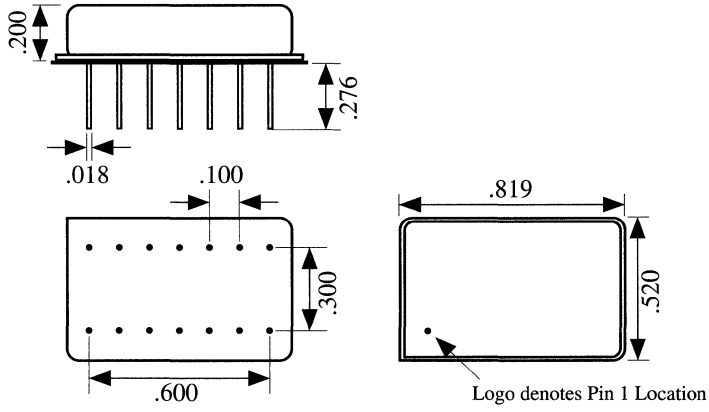


# Tables

# 14-Pin Packages

## Table 1: 14-Pin Metal Can Outline

**Package** (Lead Count = 14)



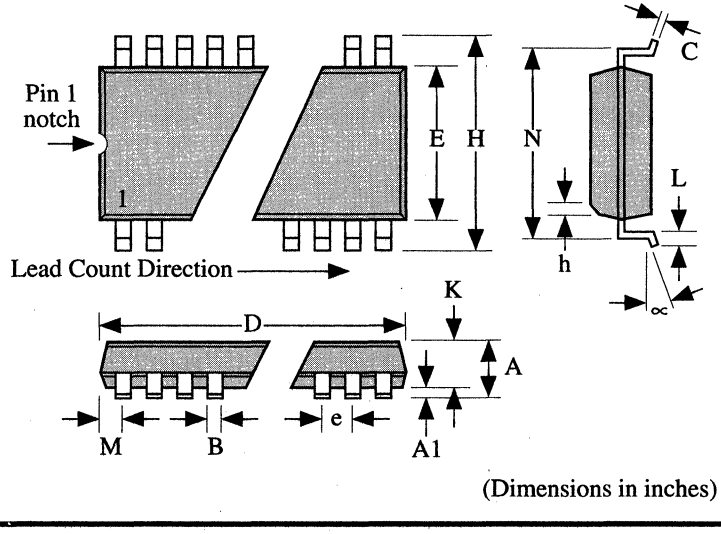

(Dimensions in inches)

# 16-Pin Packages

## Table 2: 16-Pin SOIC Outline

| Symbol | MIN | MAX |
|---|---|---|
| A | .099 | .104 |
| A1 | .004 | .009 |
| B | .014 | .019 |
| C | .010 | REF |
| D | .405 | .410 |
| E | .294 | .299 |
| e | .050 | TYP |
| H | .402 | .419 |
| h | .025 x | 45° |
| L | .030 | .040 |
| ∝ | 0° | 8° |
| K | .088 | .098 |
| M | .020 | .030 |
| N | .335 | .351 |

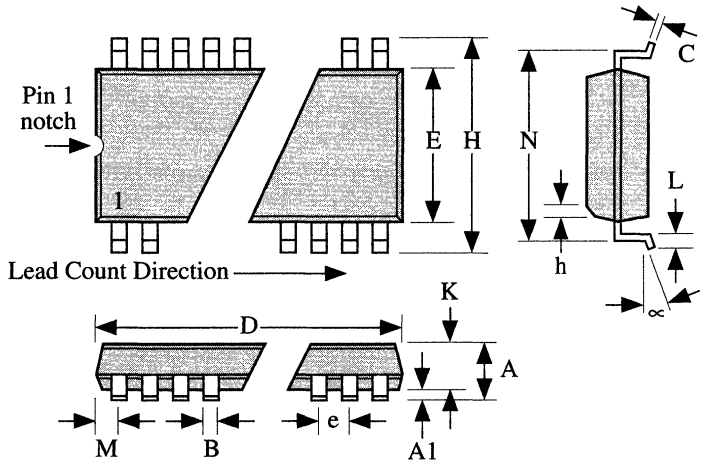
Package (Lead Count = 16)



# 20-Pin Packages

## Table 3: 20-Pin SOIC Outline

| Symbol | MIN | MAX | Package (Lead Count = 20) |
|---|---|---|---|
| A | .099 | .104 | |
| A1 | .004 | .009 | |
| B | .014 | .019 | |
| C | .010 | REF | |
| D | .505 | .512 | |
| E | .294 | .299 | |
| e | .050 | TYP | |
| H | .402 | .419 | |
| h | .025 x 45° | | |
| L | .030 | .040 | |
| ∝ | 0° | 8° | |
| K | .088 | .098 | |
| M | .020 | .030 | |
| N | .335 | .351 | |

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# Revision History / Credits

V1.4 (11/15/93) — Final Release Version

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(516) 757–1606
FAX: (516) 757–1636

Reagan/Compar
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Rochester, NY 14624
(716) 271–2230
FAX: (716) 381–2840

Reagan/Compar
214 Dorchester Ave., #3C
Syracuse, NY 13203
(315) 432–8232
FAX: (315) 432–8238

Reagan/Compar
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Ste. 2211
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(513) 890–2150
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3645 Warrensville Center Rd. #244
Shaker Heights, OH 44122
(216) 491–9177
FAX: (216) 491–9102

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Northwest Marketing Associates
6975 S. W. Sandburg Rd, Ste. 330
Beaverton, OR 97223
(503) 620–0441
FAX: (503) 684–2541

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2801 West Chester Pike
Broomall, PA 19008
(215) 356–5300
FAX: (215) 356–8710

KW Electronic Sales, Inc.
4068 Mt. Royal Blvd., Ste. 110
Allison Park, PA 15101
(412) 492–0777
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Electronic Technical Sales
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Caparra Heights Station
San Juan, P.R. 00922
(809) 798–1300
FAX: (809) 798–3661

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Sierra Technical Sales
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Suite 103
Draper, UT 84020
(801) 571–8195
FAX: (801) 571–8194

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Bellevue, WA 98005
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### Wisconsin

Micro Sales Inc.
210 Regency Court
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Waukesha, WI 53186
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### Cypress Semiconductor International—Europe

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FAX: (39) 69—496—888

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Interporto di Torino
Proma Strada n. 5/B
10043 Orbassano, Italy
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FAX: (39) 11—397—58—10

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Braemac Pty. Ltd.
10—12 Prospect Street, Box Hill
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1810 Wemmel, Limburg
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FAX: (33) 99 50 11 28

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FAX: (49) 711 7655181

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Metronik GmbH
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Telex: 921123
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SASCO GmbH
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Telex: 2165623
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FAX: (852) 7–805-871

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Telex: 845 2696 or 8055
(Attn: ICTP–705)
FAX: 80–586–872

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Tel Aviv 61 210, Israel
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Telex: 33400 VITKO
FAX: (972) 3–544–2085

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Telex: 330869 DEMICO I
FAX: (39) 29–52–19–12

Silverstar Ltd. SPA
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20126 Milano, Italy
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Teles: 33 2189 SIL 7I
FAX: (39) 2 66101359

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FAX: (81) 3–3506–3497

CTC Components Systems Co. Ltd.
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Miyamae–Ku, Kawasaki–Shi,
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FAX: (81) 44–877–4268

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FAX: (81) 3–3814–1414

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FAX: (81) 3–3264–3419

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FAX: (81) 3–3490–7274

Japan Electronics
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FAX: (81) 6–330–6814

Ryoyo Electro Corporation
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Chuo–ku, Tokyo 104 Japan
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FAX: (822) 888–7040

superCHIP Inc.
6th Floor, KyungJin Bldg. 161–17
Sansung-dong, Kangnam-ku
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FAX: (822) 558–1875

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Telex: 59418 INTRA NL
FAX: (31) 40–83–23–00

### Norway

Avnet Nortec Electronics A/S
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Telex: 77546 NENAS N
FAX: (47) 66–84–65–45

### Singapore

Electec PTE Ltd.
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#04–21, Singapore 1233
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FAX: (65) 294–7623

### Spain

ATD Electronica
Avda. de la Industria No. 32
Nave 17, 2B, 28100 Alcobendas
Madrid, Spain
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### Sweden

TH:s Elektronik AB
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Arrendevägen 36
S163 03 SPÅNGA, Sweden
Tel: (46) 8 362 970
Telex: 111 45 tenik s
FAX: (46) 8 761 3065

### Switzerland

Basix für Elektronik A. G.
Hardturmstrasse 181
CH–8010 Zurich, Switzerland
Tel: (41) 1–276–11–11
Telex: 822762 BAEZ CH
FAX: (41) 1–276–14–48

### Taiwan R.O.C.

Prospect Technology Corp.
5F, No. 348, Section 7
Cheng-Teh Rd.
Taipei, Taiwan
Tel: (886) 2–820–5353
Telex: 14391 PROSTECH
FAX: (886) 2–820–5731

### United Kingdom

Ambar Components Ltd.
17 Thame Park Road
Thame, Oxfordshire
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Telex: 837427
FAX: (44) 844–26–17–89

Arrow Electronics (UK) Ltd.
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Cambridge Road
Bedford MK42 OLF, U.K.
Tel: (44) 234 270272
FAX: (44) 234 214674

Pronto Electronic System Ltd.
City Gate House
Eastern Avenue, 399–425
Gants Hill, Ilford,
Essex, U. K. IG2 6LR
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(916) 624–9744

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San Diego, CA 92121
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Waterbury, CT 06705
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Wilmington, MA 01887
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Commack, NY 11725
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