EXAR DATABOOK

- USICs
- ASICs

TELECOMMUNICATIONS CIRCUITS

DATA COMMUNICATION & PERIPHERAL CIRCUITS

INDUSTRIAL CIRCUITS

INSTRUMENTATION & INTERFACE CIRCUITS

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DATABOOK

EXAR Corporation 750 Palomar Avenue, Sunnyvale, California 94086

EXAR

Commitment to Excellence and Reliability

One of the founding principles of EXAR has been to provide our customers with unsurpassed service and quality. Today, every individual at EXAR has taken this principle as a personal commitment, assuring that quality and reliability are built into all our products from inception to realization.

For more than a decade, this commitment to excellence has allowed EXAR to establish itself as a dependable supplier to industry leaders in the telecommunications, data communications, computer peripherals, and industrial control markets. As an ASIC (Applications Specific Integrated Circuit) manufacturer, EXAR brings years of accumulated engineering expertise in the design of USIC (User Specific Integrated Circuit) for customers with unique requirements. EXAR's ASSP (Application Specific Standard Product), USIC and GPSP (General Purpose Standard Product), along with our linear and digital applications support, allow us to offer a total solution to your system requirements.

I am certain that our commitment and dedication to quality, technology, and service will develop an outstanding long term relationship with you, our valued customer.

Nob Hatta
President

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EXAR

Section 1 – Cross References and Ordering Information

APPLICATION SPECIFIC STANDARD PRODUCTS (ASSP'S) CROSS REFERENCE

MODEMS - COMPETITION (NOT PIN COMPATIBLE UNLESS SPECIFIED)

EXAR Devices	AMI	Fairchild	Rockwell	Silicon Systems	Texas Instruments	Micro Power	Motorola	AMD
XR-212ACS	S35212A S35213	uA212A	R212DP	212A/103 SSI291 SSI213	TMS99532A TMS99534	MP7246 MP7247		AMDAC12
XR-212AS	S35212A S35213	uA212A	R212DP	212A/103 SSI291 SSI213	TMS99532A TMS995331	MP7246 MP7247		AMD79C12
XR-2123A						MP7253 (COMPATIBLE)		
XR-14412							MC14412 (COMPATIBLE)	

FILTERS (PIN COMPATIBLE)

EXAR Devices	AMI	Reticon	National	Maxim	Harris	Sierra	Mitel	
XR-2120								
XR-2103 XR 1000/8 XR-1010		5630/5631	MF4 50/100 MF10	MF10	MF10			
XR-2126 XR-2127 XR-2128	35212 35212A	5632/A 5632/B				SC11000 SC11005 SC11001		
XR-2129								

COMPUTER PERIPHERALS (PIN COMPATIBLE)

EXAR Devices	Motorola	Texas Instruments	Cherry	National	SSI			
XR-3470	MC3470	MC3470	CS3470					
XR-3471 XR-117 XR-2247	MC3471	MC3471	CS3471 CS117		SSI117			
XR-2917 XR-3447 XR-3448			CS570*	LM2917	SSI570*			
XR-3464				DP8464				

*Slight modification of PC board required, not an exact replacement

TELECOMMUNICATION PRODUCTS CROSS REFERENCE

TELECOMMUNICATION (PIN COMPATIBLE)

EXAR	Rohm	Mitel	Mostek	Sharp	Toshiba	PMI	Cherry	
XR-T8205	BA6565	ML8205			TA31002P		CS8205	
XR-T6425	BA6571							
XR-T5992	BU8992		MK50992	LR40992				
XR-T5990	BU6562							
XR-C277						RPT82		

Industry-wide Product Cross Reference

EXAR DEVICES	Fairchild	Intersil	Motorola	National	Raytheon	Signetics	Silicon General	Sprague	Texas Instruments
082 083 084									TL082 TL083 TL084
146 246 346 346-2				LM146 LM246 LM346 LM346-2	LM146 LM246 LM346				
494 495									TL494 TL495
555 1555 556 1556 558 559 567	UA555 UA556	NE555 NE556	MC1455 MC3456	LM555 LM556 LM567	RC555 RC556	NE555 NE1555 NE556 NE1556 NE558 NE559 NE567	SG555 SG556		SN72555
1310 1468 1488 1489A 1524 1525A 1527A 1543	 UA1488 UA1489		MC1310 MC1468 MC1488 MC1489A	LM1310 LM1488 LM1489A LM1524	 RC1488 RC1489A	MC1310 MC1488 MC1489A SG1524	 SG1468 SG1488 SG1489A SG1524 SG1525A SG2527A SG1543	ULN2110	SN76115N MC1488 SN75188 SN75189A SG1524
2001 2002 2003 2004 2011 2012 2013 2014	UA9665 UA9666 UA9668		MC1411 MC1412 MC1416			ULN2001 ULN2003 ULN2004	SG2001 SG2002 SG2003 SG2004 SG2011 SG2012 SG2013 SG2014	ULN2001 ULN2002 ULN2003 ULN2004 ULN2011 ULN2012 ULN2013 ULN2014	
2201 2202 2203 2204 2207 2211 2240	UA9665 UA9666 UA9667 UA9668 UA2240	 CL8240	MC1411 MC1412 MC1413 MC1416		 RC2207 RC2211	ULN2001 ULN2002 ULN2003 ULN2004	SG2001 SG2002 SG2003	ULN2001 ULN2002 ULN2003 ULN2004	ULN2001 SN75466 ULN2002 SN75467 ULN2003 SN75468 ULN2004 SN75469 UA2240
2524 2525A 2527A 2543 2567				LM2524	 RC2567	SG2524	SG2524 SG2525A SG2527A SG2543		
2917 3403 3470A 3471	UA3403		 MC3740A MC3471	LM2917	RC3403				MC3403 MC3470A MC3471
3503 3524 3525A 3527A 3543	UA3503			LM3524	RC3503	SG3524	SG3503 SG3524 SG3525A SG3527A SG3543		MC3503 SG3524
4136 4151 4194 4195	UA4136 UA4151				RC4136 RC4151 RC4194 RC4195		 SG4194		RC4136
4558 4739 4741	UA4558 UA739	 LM348	MC4558 MC4741	LM1458 LM348	RC4558 RC4739 HA4741-5	MC1458	SG1458		RC4558 SN72558
5532 5533 5534					RC5532 RC5533 RC5534	NE5532 NE5533 NE5534			NE5532 NE5533 NE5534
6118 6128						NE594		ULN6118 ULN6128	
8038		ICL8038							
13600 14412			 MC14412	LM13600	LM13600	NE5517			

NUMERIC INDEX

PRODUCT ORDERING INFORMATION

Part Identification

XR	XXXXX
Manufacturer's Prefix	Basic Type

Grade

M = Military
N = Prime Electrical
P = Prime Electrical
C = Commercial

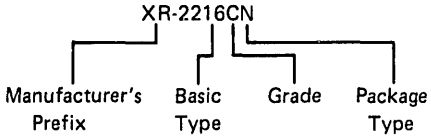
F = 4.75 V to 15 V
V = 4.75 V to 6 V
K = Kit

Operating Voltage Ranges

Package Type

N = Ceramic Dual-in-Line
P = Plastic Dual-in-Line
MD = Plastic SOIC (Surface Mount)
Q = Quad Package

Example



Definition of Symbols:

M = Military Grade Part, Ceramic Package Only. are guaranteed to operate over military temperature range. Consult factory for level of high rel screening.
N = Prime Grade Part, Ceramic Package
P = Prime Grade Part, Ceramic Package

N, P, CN, and CP parts are electrically identical and operate over 0°C to +70°C unless otherwise stated. In addition, N and P parts generally have operating parameters more tightly controlled than the CN or CP parts.

For details, consult EXAR Sales Headquarters or your Sales/Technical Representatives.

ORDER ENTRY:

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EXAR

Section 2 – Telecommunication Products

PCM Line Receiver & Clock Recovery Circuit

GENERAL DESCRIPTION

The XR-T5650 is a monolithic bipolar IC designed for PCM type line receiver applications operating at T1. T148C, T1C and 2 M bit/s data rates. It provides all the active circuitry required to perform automatic line build out (ALBO), threshold detection, positive and negative data and clock recovery.

Clock recover using a crystal filter instead of an LC tank circuit is also available as XR-T5750.

FEATURES

On Chip Positive and Negative Data, Clock Recovery
Less than 10 ns Sampling Pulse over the Operating Range
Double Matched ALBO Ports
Single 5.1 V Power Supply
2 M Bit/s Capability

APPLICATIONS

T1 PCM Line Receiver
T148C Line Receiver
T1C PCM Line Receiver (requires external amplifier)
General Purpose Bipolar Line Receiver
HDB3 Line Receiver
B8ZS Line Receiver

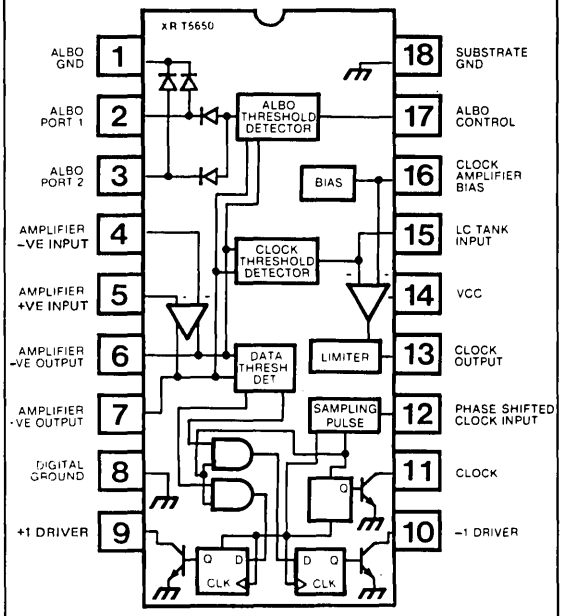
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40° to +85°C
Supply Voltage	-0.5 to +10 V
Supply Voltage Surge (10 ms)	+25 V
Input Voltage (except Pins 2,3,4,17)	-0.5 to 7 V
Input Voltage (Pins 2,3,4,17)	-0.5 to +0.5 V
Data Output Voltage (Pins 10,11)	20 V
Voltage Surge (Pins 5,6,10,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5650	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-T5650 is designed for interfacing T1, T148C and 2 Mbit/s PCM carrier lines on plastic or pulp insulated cables. It can also be used at T1C rate (3.152 M bit/s) with external gain. Since it outputs plus and minus ones on a bipolar pulse stream together with the clock, it can be used to interface systems having different line codes like AMI, AMI-B8ZS or AMI-HDB3.

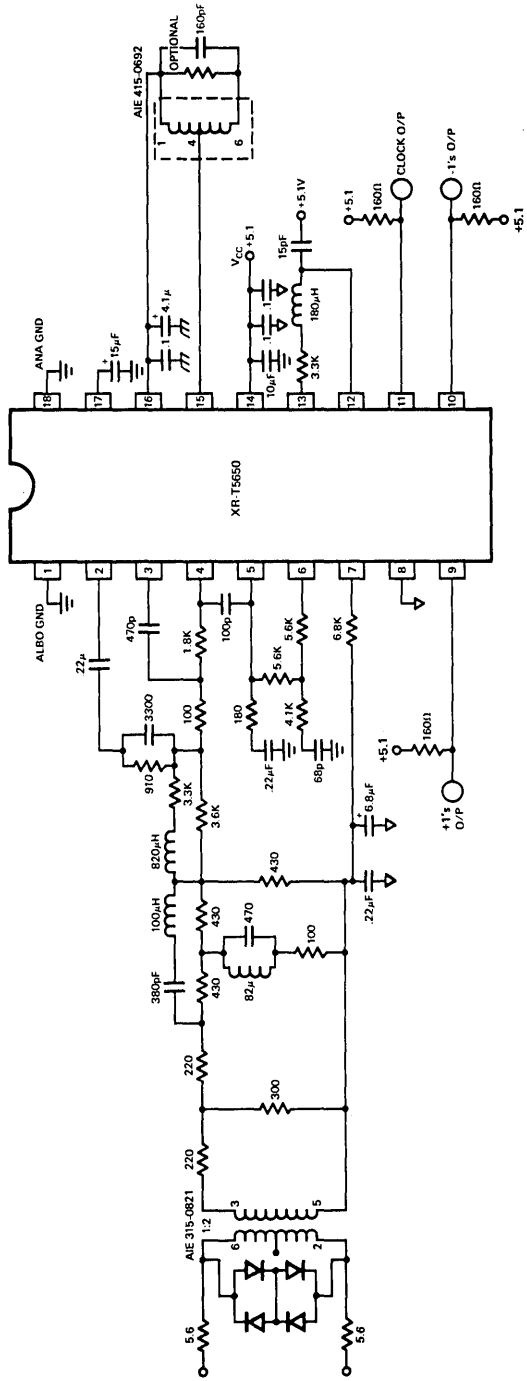
The XR-T5650 is a modified version of XR-T5620 PCM repeater IC. It contains all the active circuitry needed to build a PCM line receiver up to 6300 ft. cable length. The preamplifier, the clock amplifier, threshold detectors, data latches and output drivers are similar to the ones on XR-T5620. Clock extraction is done by means of an LC tank circuit.

In addition to plus and minus one outputs, a synchronous clock signal is made available at Pin 11 by deleting one of the ALBO ports on XR-T5620 thus leaving two matched ALBO ports. All outputs have high current open collector transistors.

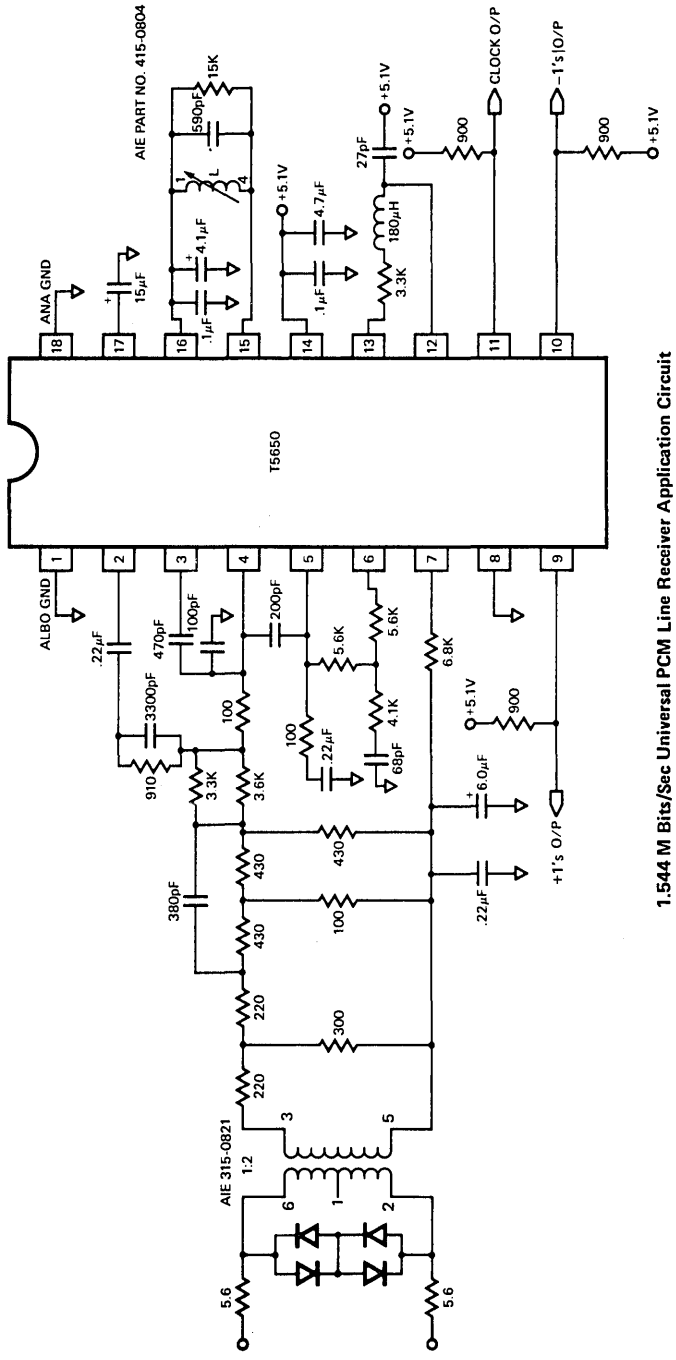
ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.1 V ± 5%, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Supply Current		26	34	mA	ALBO Off
	Clock & Data Output					
	Output Leakeage Current		0	100	µA	$V_{pull\text{-}up}$ = 15 V
	Amplifier Pin Voltages	2.4	2.9	3.4	V	At DC Unity Gain
	Amplifier Output					
	Offset Voltage	-50	0	50	mV	R_S = 8.2 kΩ
	Voltage Swing	2.2			V	Measured Differentially from Pin 7 to Pin 6
	Amplifier Input					
	Bias Current			5	µA	
	ALBO on Current	3			mA	
	Drive Current		1		mA	
AC CHARACTERISTICS						
	Pre Amplifier					
	AC Gain @ 1 MHz		50		dB	
	Input Impedance	20			kΩ	
	Output Impedance			200	Ω	
	Clock Amplifier					
	AC Gain		32		dB	
	-3 dB Bandwidth	10			MHz	
	Delay		10		ns	
	Output impedance			200	Ω	
	ALBO					
	Off Impedance	20			kΩ	
	On Impedance			25	Ω	
CLOCK DATA OUTPUT BUFFERS						R_L = 130Ω, $V_{pull\text{-}up}$ = 5.1 V ± 5%
	Rise Time		30		ns	
	Fall Time		30		ns	
	Output Pulse Width		244		ns	
	Sample Pulse Width		10		ns	
	V_{OL}		0.7		V	
	I_L sink		35		mA	
THRESHOLDS						
	ALBO	1.4	1.5	1.6	V	
	Clock Drive Current Peak		1.0		mA	At $V_O = V_{ALBO}$ Threshold
CLOCK THRESHOLD						
	% of ALBO	63	69	75	%	
DATA THRESHOLD						
	% of ALBO	40	46	52	%	



1.544 M Bits/Sec Universal PCM Line Receiver Application Circuit
Random Pattern – Max. Cable Loss 36 dB



1.544 M Bits/Sec Universal PCM Line Receiver Application Circuit
Maximum Cable Loss 25 dB

B8ZS/AMI Transcoder

GENERAL DESCRIPTION

The XR-T5670 is an LSI CMOS integrated circuit which performs the B8ZS or AMI transmission coding and receiving decoding functions with error detection. It is intended for DS1 (1.544 Mbits/s) PCM transmission applications, but can operate at clock frequencies up to 16 MHz. The device is packaged in a 16 Pin CERDIP package and the operating temperature is between -40°C to +85°C.

FEATURES

B8ZS Coding and Decoding for Data Rates up to 6 Mbits/s to AT&T Technical Advisory 69
B8ZS/AMI Transmission Coding/Reception Decoding with Code Error Detection
All Transmitter and Receiver Inputs/Outputs are TTL Compatible
Internal Loop Test Capability
Single 5 V ± 10% Supply Rail

APPLICATIONS

AMI Encoding/Decoding
B8ZS Encoding/Decoding

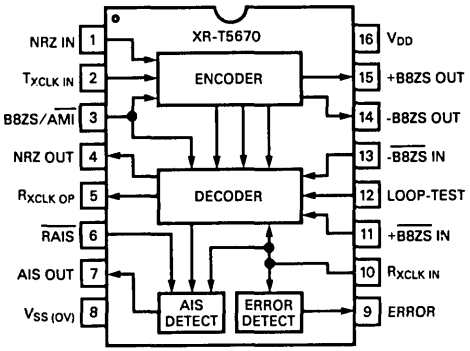
ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (V_{DD})	-0.3 to 7.0 V
Input Voltage Range (V_{IN})	-0.3 to V_{DD} + 0.3 V
Input Protection Current (I_D)	±10 mA
Storage Temperature Range	-55°C to 150°C
Operating Temperature Range	
Ceramic	-40°C to +85°C
Plastic	0°C to 70°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5670CP	Plastic	0°C to 70°C
XR-T5670CN	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

Coder

Binary data in "NRZIN" is clocked into the coder by a synchronous transmission clock "TXCLKIN" on the falling edge. The "+B8ZS" and "-B8ZS" output signals appear 8.5 clock cycles later to allow for the insertion of extra pulses due to sequences of eight consecutive zeros. These two signals are full width data and will be mixed with the "TX CLKIN" at the input of an external line driver to produce bipolar B8ZS signals for transmission.

Decoder

Received half width data on "+$\overline{\text{B8ZSIN}}$" and "-$\overline{\text{B8ZSIN}}$" are locked into the decoder on the rising edge of the received clock "RXCLKIN". The "NRZOUT" binary data output occurs on eight clock cycles later. Received signals not consistant with B8ZS coding rules are detected as errors. The error output "ERROR" is active high during one "RXCLKIN" clock period.

AIS (Alarm Indication Signal)

If the decoder inputs received a continuous of ones (all marks) over two consecutive periods of the external reset signal "$\overline{\text{RAIS}}$", the "AISOUT" output will be set high and latched in that state until one or more zeros are received when the next reset signal "$\overline{\text{RAIS}}$" occurs.

The number of received zeros required to reset "AISOUT" over two consectuive periods of "$\overline{\text{RAIS}}$" can be mask programmed to two or three.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = -40°C$ to $+85°C$, $V_{DD} = 4.5$ to 5.5 V, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DYNAMIC CHARACTERISTICS						
T_{XCLKIN}	Clock Input Frequency			6	MHz	
R_{XCLKIN}	Clock Input Frequency			6	MHz	
t_{s1}	Data Set-Up Time	55			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{h1}	Data Hold Time	25			ns	NRZIN to T_{XCLKIN} See Figure 6
t_{pd1}	Data Propagation Delay Time			65	ns	T_{XCLKIN} to B8ZS OUT See Figures 3 and 6, Note 1
t_{s2}	Data Set-Up Time	55			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{h2}	Data Hold Time	0			ns	B8ZSIN to R_{XCLKIN} See Figure 7, Loop Test = 0
t_{pd2}	Data Propagation Delay Time			90	ns	R_{XCLKIN} to NRZOUT See Figures 4 and 7, Note 2 Loop Test = 0
t_{pd3}	Clock Delay Time			50	ns	R_{XCLKIN} to $R_{XCLKOUT}$ See Figure 8, Loop Test = 0
t_{s3}	RAIS = 0 Set-Up Time	30			ns	RAIS to R_{XCLKIN} See Figure 7
t_{h3}	RAIS= 0 Hold Time	30			ns	RAIS to R_{XCLKIN}
STATIC CHARACTERISTICS, $V_{DD} = 5.0$ V						
I_{DD}	Quiescent Device Current			100	µA	
	Operating Current			4	mA	Input Clock Frequency = 2.0MHz
V_{DD}	Supply Voltage	4.5	5	5.5	V	
V_{IN}	Input Voltage 0	0		5.0	V	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2			V	
V_{OL}	Output Low Voltage			0.1	V	$I_{OL} = 0$
V_{OH}	Output High Voltage	4.9			V	$I_{OH} = 0$
I_{OL}	Output Low Current	1.6			mA	$V_{OL} = 0.4$ V
I_{OH}	Output High Current	-1			mA	$V_{OH} = 4.6$ V
I_{IL}	Input Low Current			-10	µA	$V_{IL} = 0$ V
I_{IH}	Input High Current			10	µA	$V_{IH} = 5$ V

Note 1: The encoded B8ZS OUT are delayed by 8½ clock periods from NRZIN.
Note 2: The decoded NRZOUT are delayed by 7½ clock periods from B8ZS IN.

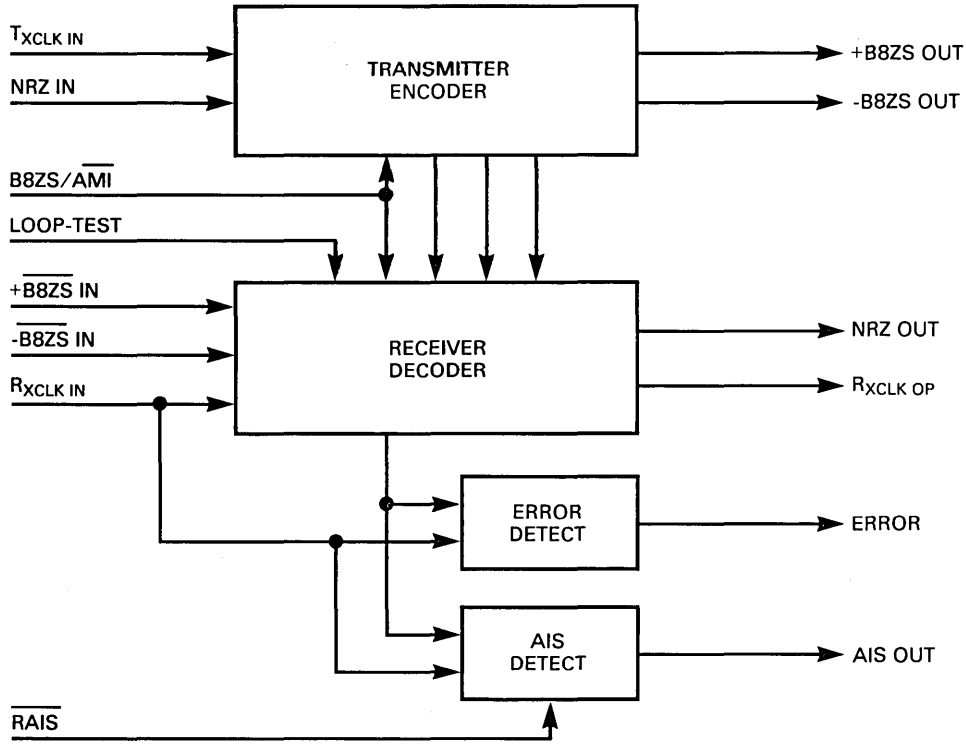


Figure 1. XR-T5670 Block Diagram

Loop Test

When the Loop Test control input is set high, a test mode is made in which the "+B8ZSOUT" and "-B8ZSOUT" are internally connected to the decoder inputs. The external B8ZS inputs and the "RXCLKIN" are disabled, and the "TXCLKIN" is used to control the decoder timing. The "NRZOUT" signals correspond to the "NRZIN" input, but delayed by approximately 16 clock periods.

B8ZS/AMI

To operate the XR-T5670 in AMI mode, the B8ZS/AMI control input is driven low. In this mode, two consecutive pulses of the same polarity at the decoder inputs will be detected and flagged as an error at the "ERROR" output.

Definition of B8ZS Code Used in XR-T5670 Transcoder

With B8ZS coding, each block of eight consecutive zeros is removed and the B8ZS code is inserted. If the pulse preceding the inserted code is transmitted as a positive pulse (+), the inserted code is 000+−0−+. Bipolar violations occur in the fourth and seventh bit position of the inserted code. If the pulse preceeding the inserted code is a negative pulse (−), the inserted code is 000−+0+−. Bipolar violations again occur in the fourth and seventh bit positions as illustrated in Figure 2.

Binary Signal	1	0	0	0	0	0	0	0	0
B8ZS Signal	+1	0	0	0	+1	−1	0	−1	+1
or	−1	0	0	0	−1	+1	0	+1	−1

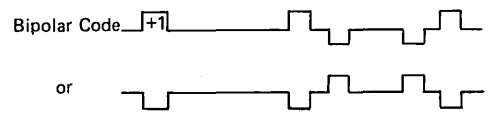


Figure 2. B8ZS Code

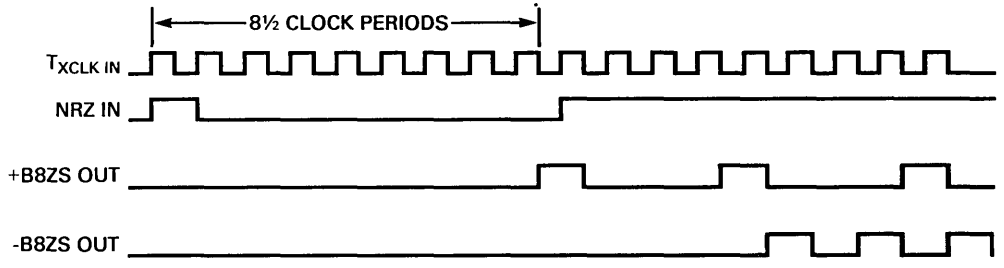


Figure 3. Encoder Waveforms

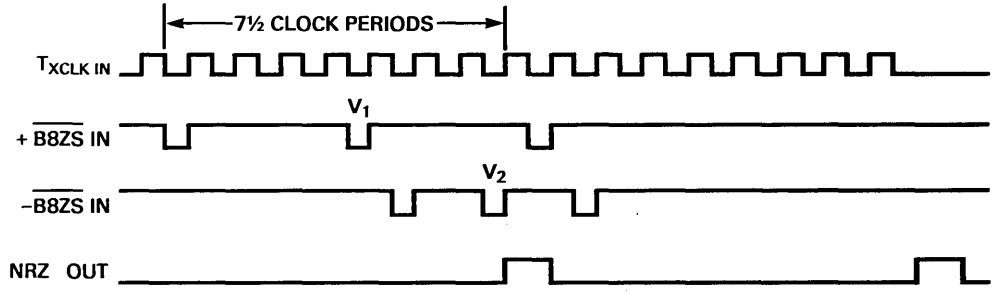


Figure 4. Decoder Waveforms

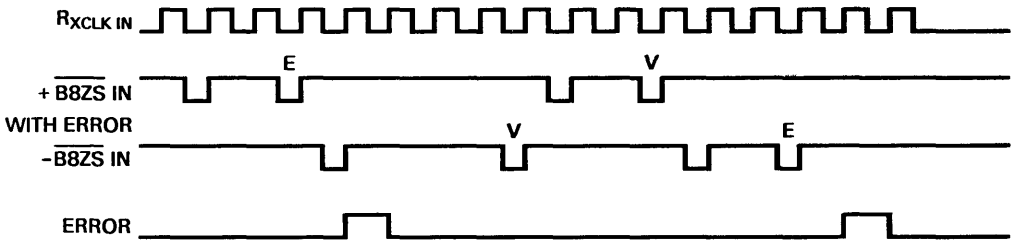


Figure 5. B8ZS Error Output Waveforms

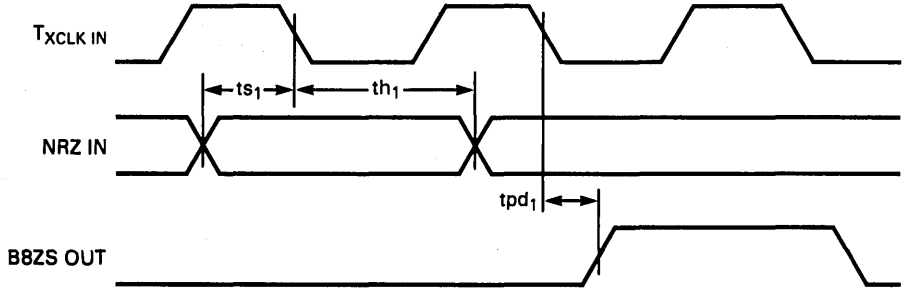


Figure 6. Encoder Timing Relationship

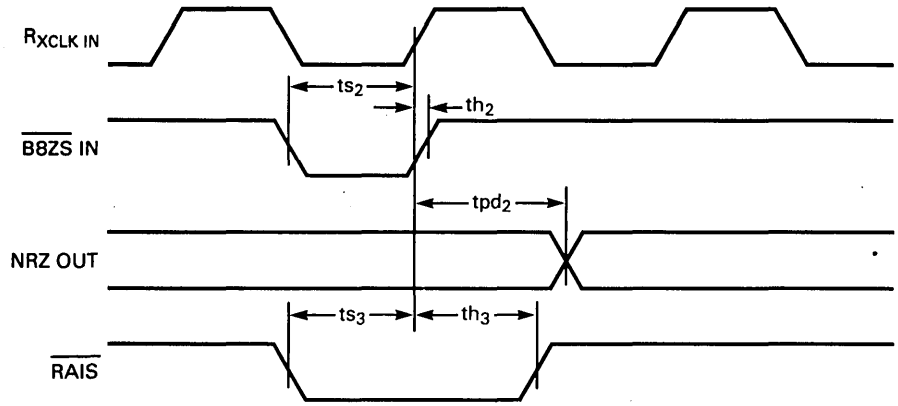


Figure 7. Decoder Timing Relationship

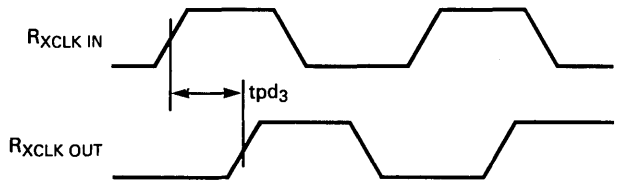


Figure 8. $R_{XCLK\ IN}$ to $R_{XCLK\ OUT}$ Relationship

Dual Line Driver

GENERAL DESCRIPTION

The XR-T5675 is a bipolar monolithic dual line driver designed to drive PCM lines up to a 10 Mbits/s rate. The device is powered from a single 5 V ± 5% source. Its current consumption is 14 mA typical and the output can be pulled up to 20 V dc. The XR-T5675 is packaged in a standard 8 pin DIL plastic or ceramic package, and its temperature of operation is between 0°C to +70°C.

FEATURES

50 mA Output Drive Current Capability
Low Current Consumption (18 mA Max.)
High Speed Switching
Dual Matched Driver Outputs
High Output Voltage
TTL or DTL Compatible Inputs

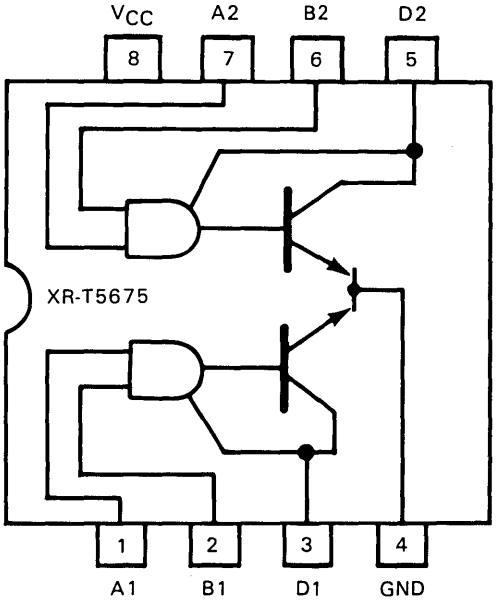
APPLICATIONS

T1, T1C, T2, 2048K and 8448K b/s PCM Line Driver
LAN Line Driver
Relay Driver
LED/Lamp Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	+7.0 V
Input Voltage (Pin 1,2,6,7)	−0.2 V to +V_{CC}
Output Pull-up Voltages (Pin 3,5)	+35.0 V
Power Dissipation	
Ceramic	700 mW
Plastic	600 mW
Storage Temperature	−65°C to 150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5675CP	Plastic	0°C to +70°C
XR-T5675CN	Ceramic	0°C to +70°C

SYSTEM DESCRIPTION

Figure 1 contains the Functional Block Diagram of the XR-T5675. The circuit consists of two AND logic gates with their outputs internally connected to the bases of the output transistors. The low level outputs are clamped at 1 VBE to ground to insure non-saturating operation for fast switching.

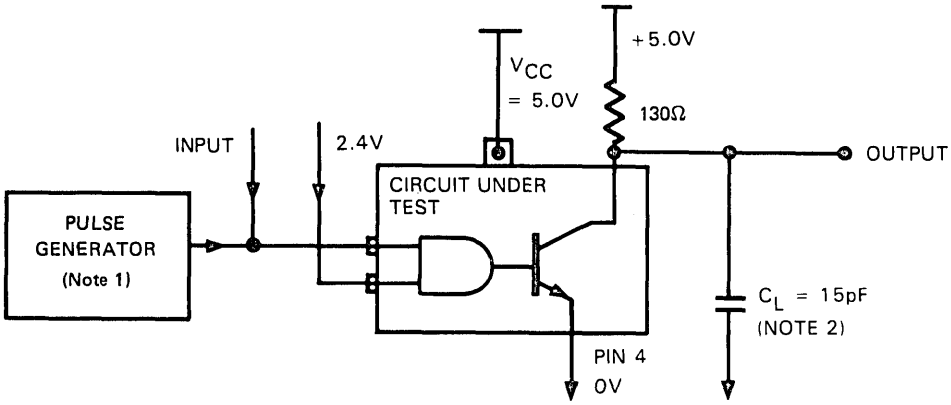
A	B	OUTPUT (D)
L	L	H (OFF)
L	H	H (OFF)
H	L	H (OFF)
H	H	L (ON)

Truth Table - XR-T5675
H = H Level, L = Low Level

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0 V, T_A = 0°C to +70°C, unless specified otherwise.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CC}	Supply Voltage	8	4.75	5.0	5.25	V	
V_{IH}	High Level Input Voltage	1,2,6,7	2.2			V	I_{OL} = 50 mA V_{OL} = 0.95 V
V_{IL}	Low Level Input Voltage	1,2,6,7			0.8	V	
I_{IH}	High Level Input Current	1,2,6,7			40	μA	V_{IH} = 2.7 V, Pins 3 & 5 Open
I_{IL}	Low Level Input Current	1,2,6,7			−1.2	mA	V_{IL} = 0.4 V, Pins 3 & 5 Open
V_{OL}	Low Level Output Voltage	3,5	0.6		0.95	V	V_{IH} = 2.2 V, I_{OL} = 50 mA
I_{OL}	Low Level Output Current	3,5			50	mA	V_{IH} = 2.2 V, V_{OL} = 0.95 V
I_{OH}	High Level Leakage Current	3,5			100	μA	Pins 3 & 5, Pull-up to +20 V
I_{CCH}	Supply Current Output High	8			3.0	mA	Pins 3 & 5 Open
I_{CCL}	Supply Current Output Low	8		14.0	18.0	mA	Pins 3 & 5 Open
SWITCHING CHARACTERISTICS, V_{CC} = 5.0 V ±5%, T_A = +25°C							
t_{pLH}	Propagation Delay, Low to High	3,5		15		ns	See Figure 2
t_{pHL}	Propagation Delay, High to Low	3,5		15		ns	
t_{rise}	Rise Time	3,5		15	24	ns	
t_{fall}	Fall Time	3,5		10	24	ns	
	Output Pulse Imbalance			2.5		ns	At 50% Output Level



NOTE 1. PULSE GENERATGOR FREQUENCY = 2.0 MHz, Z_{OUT} = 50Ω

NOTE 2. CL INCLUDED — PROBE AND JIG CAPACITANCE

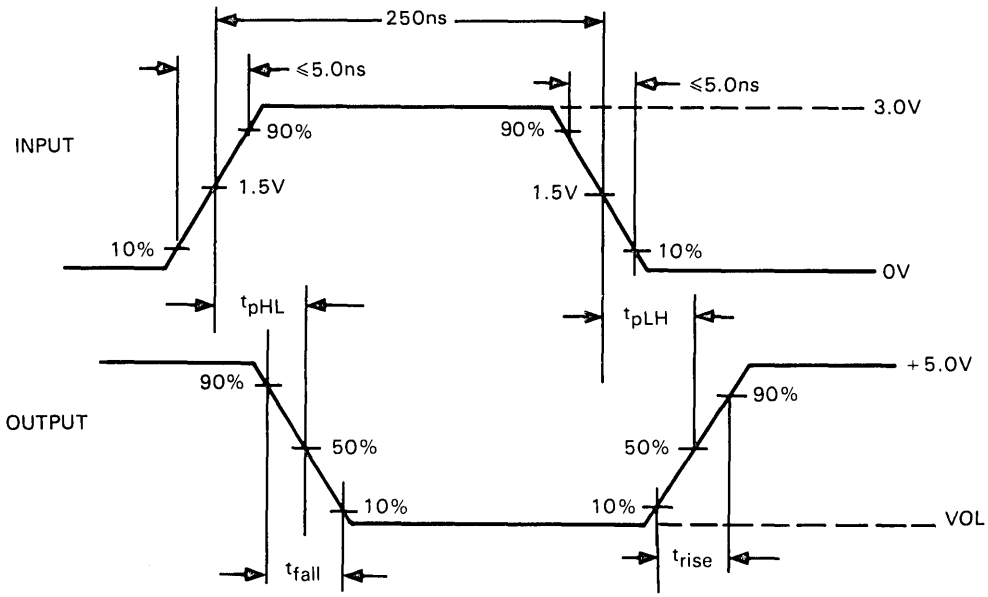
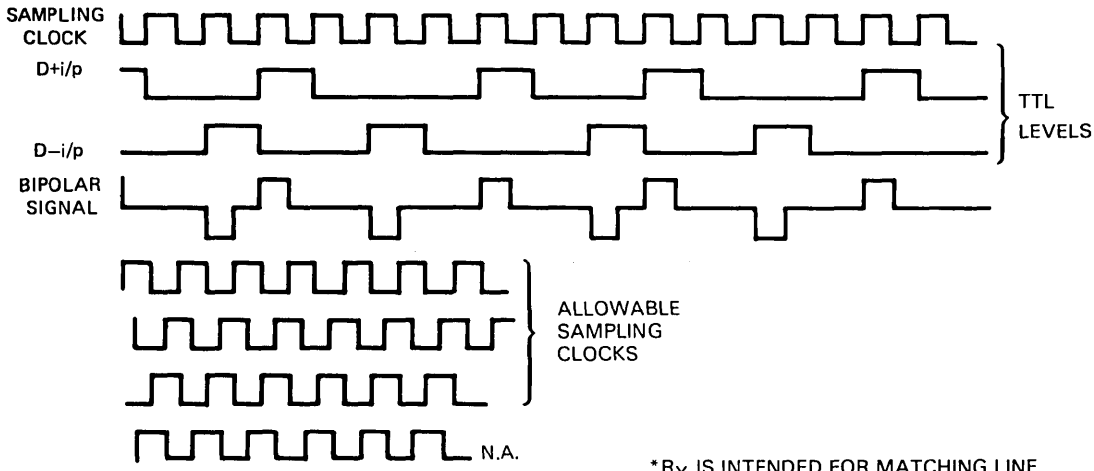
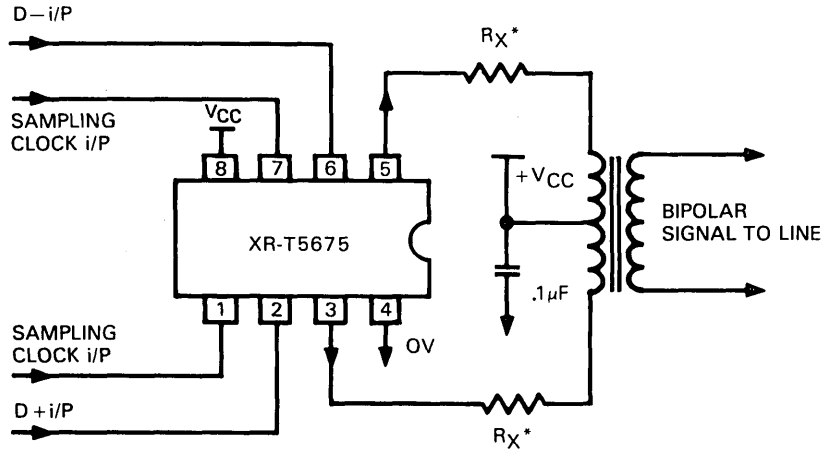


FIGURE 2. AC TEST CIRCUITS AND SWITCHING WAVEFORMS



*R_X IS INTENDED FOR MATCHING LINE IMPEDANCE, BUT ITS FINAL VALUE MAY BE DETERMINED BY THE OUTPUT SIGNAL AMPLITUDE REQUIRED.



IN THE CASE WHERE D+ AND D– ARE HALF WIDTH SIGNALS, PIN 1 AND PIN 7 SHOULD BE TIED TOGETHER AND RETURNED TO +5.0V VIA A 1K RESISTOR

FIGURE 3. XR-T5675 PCM LINE DRIVER APPLICATION CIRCUIT

PCM Line Interface Chip

GENERAL DESCRIPTION

The XR-T5680 is a PCM line interface chip. It consists of both transmit and receive circuitry in a DIL 18 pin package. The maximum bit rate the chip can handle is 10 M Bits/s and the signal level to the receiver can be attenuated by −10 dB cable loss at half the bit rate. Total current consumption is between 27-46 mA at +5.0 V.

FEATURES

Single +5.0 V Supply
Receiver Input Can Be Either Balanced or Unbalanced
Up to 10 MBits/s Operation
TTL Compatible Interface

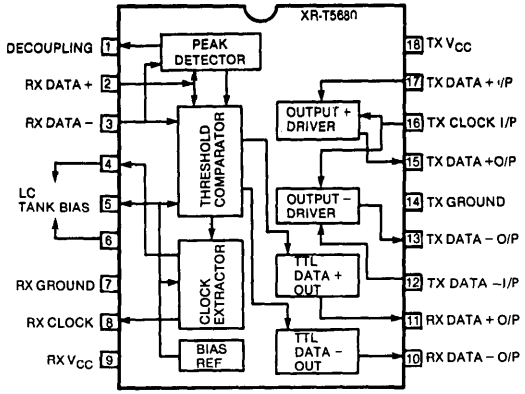
APPLICATIONS

T1, T1C, T148C, T2, 2048 & 8448 KBits/s
PCM Line Interface
CPI
DMI

ABSOULTE MAXIMUM RATINGS

Supply Voltage	+20 V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5680	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The incoming bipolar PCM signal which is attenuated and distorted by the cable is applied to the threshold comparator and the peak detector. The peak detector generates a DC reference for the threshold comparator for data and clock extraction. A tank circuit tuned to the appropriate frequency is added to the later operation. The clock signal, data + data − all go through a similar level shifter to be converted into TTL level to be compatible for digital processing.

In the transmit direction, the output drivers consist of two identical TTL inputs with open collector output stages. The maximum low level current these output stages can sink is 40.0 mA. With full width data applied to the inputs together with a synchronized clock. The output will generate a bipolar signal when driving a centre-tapped transformer. A typical circuit diagram to XR-T5680 is shown in Figure 1, and the DC characteristics are indicated in the Electrical Characteristics chart.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0 V, T_A = 0° - 70°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DC Supply	+4.75	+5.0	+5.25	V	
Supply Current		35.0	46.0	mA	Output Drivers Opens
Tank Drive Current	1.5	2.0	2.5	mA	Measured at Pin 4
*Clock Output/Low Level		0.4	0.8	V	Measured at Pin 8, I_{OL} = 1.0 mA
*Clock Output/High Level	3.0	3.6		V	Measured at Pin 8 I_{OH} = −400μA
*Data Output/Low Level		0.4	0.8	V	Measured at Pins 10,11 I_{OL} = 1.0 mA
*Data Output/High Level	3.0	3.6		V	Measured at Pins 10,11 I_{OH} = −400μA
Output Driver/Low Level	0.6		0.95	V	Measured at Pins 13,15 I_{OL} = 40 mA
Output Driver Current Sink			40	mA	Measured at Pins 13,15 V_{OL} = 0.95 V
Output Driver Rise Time		20	25	ns	Measured at Pins 13,15 with 150Ω Pull-up to +5.0 V CL = 15 pF
Output Driver Fall Time		20	25	ns	Measured at Pins 13,15 with 150Ω Pull-up to +5.0 V CL = 15 pF

*These output terminals are LS-TTL compatible.

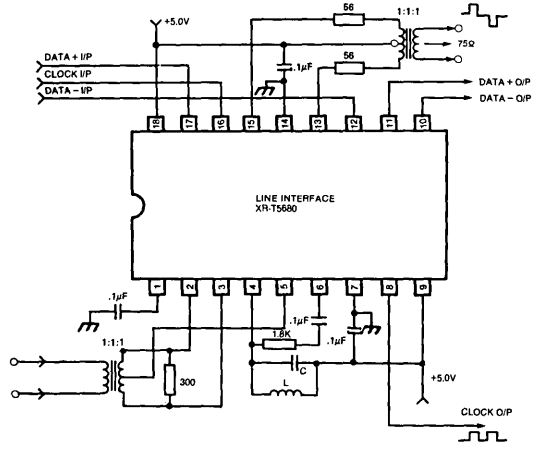


Figure 2. A recommended Circuit Diagram

PCM Transceiver Chip

GENERAL DESCRIPTION

The XR-T5681 is a PCM transceiver chip. It consists of both transmit and receive circuitry in a CERDIP 18 pin package. The transceiver is designed for short line application (<—10 dB) such as in digital multiplexed interfacing and digital PBX environments. The maximum frequency of operation is 3 MBits/s so it covers T1, T148C, and Europe's 2.048 MBit/s PCM system. The device is designed to operate over the temperature range of 0°C to +70°C.

FEATURES

Single +5.0 V Supply
Receiver Can Accept Either Balanced or Unbalanced Inputs
TTL Compatible Interface
Transmitter and Receiver in One Package

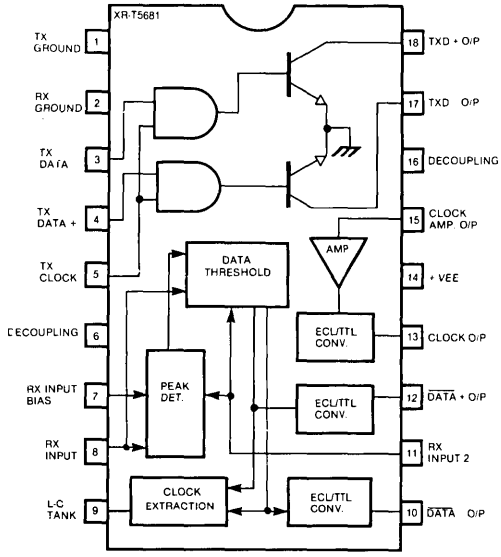
APPLICATIONS

T1, T148C, and 2.048 MBits/s PCM Line Interface
CPI
DMI

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+20 V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5681	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The functions of the circuit terminals are defined in the Functional Block Diagram. At the receive direction, the incoming bipolar signal which has been attentuated and distorted by the cable is applied to the input of the peak detector. The variable threshold voltage produced by the peak detector controls the data comparator for P and N rails signal extractions. Timing information is obtained by means of a full wave rectifier and an L-C resonant circuit tuned at the appropriate frequency. All data and clock outputs are LSTTL compatible.

At the transmitter, the outputs have two identical non-saturating open collector stages which can drive the output line transformer directly with a maximum current of 40 mA. Full width, TTL compatible, P and N rail signals at the inputs and a 50% duty cycle TTL clock are needed to form the bipolar line signal at the secondary of the transformer. The output signal conforms to CCITT G.703 recommendation. A circuit diagram connected for 2048 K bits/s line interface application is shown in Figure 1.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0 V, T_A = 0°C - +70°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DC Supply	+4.75	+5.0	+5.25	V	
Supply Current		35.0	46.0	mA	T_X Drivers Open
Tank Drive Current	1.5	2.0	2.5	mA	Measured at Pin 9,
Clock O/P/Low Level		0.3	0.8	V	Measured at Pin 13, I_{OL} = 1.0 mA
Clock O/P/High Level	3.0	4.3		V	Measured at Pin 13, I_{OH} = 400μA
Data O/P/Low Level		0.4	0.8	V	Measured at Pins 10,12, I_{OL} = 1.0 mA
Data O/P/High Level	3.0	4.5		V	Measured at Pin 10,12, I_{OH} = 400μA
Transmitter O/P/Low Level	0.6		0.95	V	Measured at Pin 13,15, I_{OL} = 40 mA
Transmitter O/P/Current Sink			40	mA	Measured at Pin 13,15, V_{OL} = 0.95V
Transmitter O/P/Rise Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to +5.0 V, CL = 15 pF
Transmitter O/P/Fall Time		20	30	ns	Measured at Pin 13,15 with 150Ω Pull-up to +5.0 V, CL = 15 pF

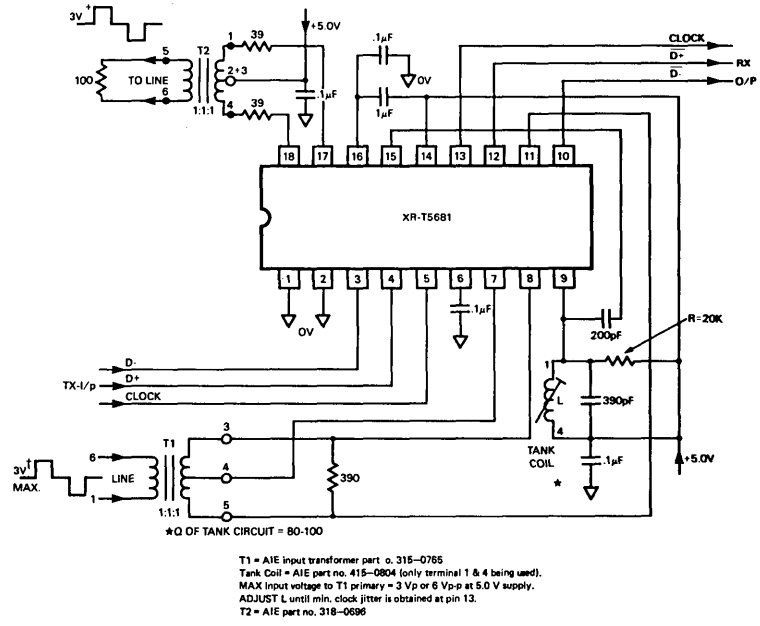


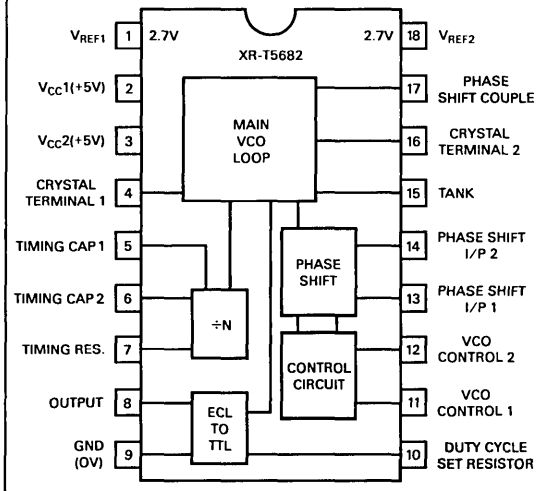
Figure 2. Circuit Connection Diagram for 2048Kbits/s operating

Voltage Controlled Crystal Oscillator

GENERAL DESCRIPTION

The XR-T5682 is a bipolar monolithic voltage controlled crystal oscillator IC designed for general purpose crystal phase locked loop (PLL) and particularly in data rate conversion, jitter reduction, and down multiplexing applications in PCM systems operating at 1.536, 1.544 and 2.048 M/bits/s data rates. It is packaged in 18 pin CERDIP and can operate from 4.75 to 5.25 volts.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Single +5V Circuit
Built-in Programmable Analog Divider
TTL Compatible Clock Signal Output
Adjustable Duty Cycle of the Output Clock Squarewave
Uses Phase Lead/Lag Capacitor and Inductor Instead of a Varactor Diode to Control Frequency

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5682	Ceramic	0°C to 70°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Lead Soldering (10 Seconds)	300°C

SYSTEM DESCRIPTION

The XR-T5682 uses phase lead and lag components rather than a varactor diode to control the frequency of oscillations. A filter crystal, at least twice the desired frequency, is used in series oscillation mode. The generated signal is fed back through a phase shift control circuit to sustain and change the frequency of oscillations. An analog divide by N circuit which consists of an astable mutlivibrator is provided to obtain the desired clock rate. The frequency of oscillations of the astable multivibrator can be changed externally by means of a resistor and a capacitor to obtain the required number of divisions. An ECL to TTL convertor circuit is designed to provide a TTL compatible clock signal, the duty cycle of which is adjustable with an external resistor tied either to V_{CO} or Ground.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C at a supply voltage of V_{CC} = 4.75 V to 5.25 V_{DC}, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	
I_{CC}	Supply Current	20	35	45	mA	
V_{REF}	Referene Voltage	2.5	2.7	2.9	V	Pin 13
V_{REF}	Reference Voltage	2.5	2.7	2.9	V	Pin 14
V_{REF}	Reference Voltage	2.5	2.7	2.9	V	Pin 1 and 18
V_{OH}	Output High Voltage	4			V	Pin 8
V_{OL}	Output Low Voltage			0.8	V	
I_{TANK}	Tank Circuit Current	1.4	1.73	2.3	mA	Pin 15
I_{TIMING}			1	3	mA	Pin 7
G_C	VCO Convertion Gain	350	650	1000	Hz/V	
	Clock Duty Cycle	25	50	75	%	Adjustable

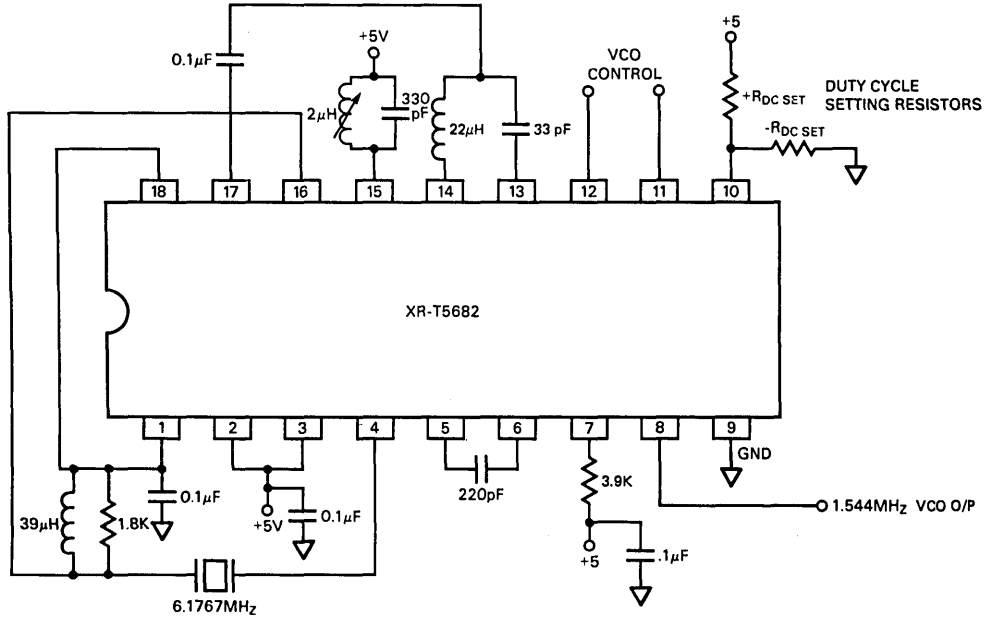


Figure 1. Typical 1.544 M/bits/s Application Circuit

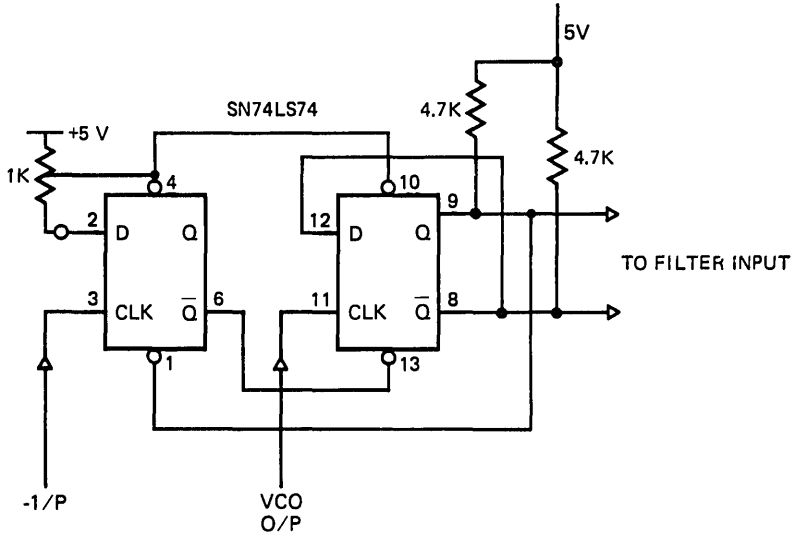


Figure 2. Recommended Phase Detector

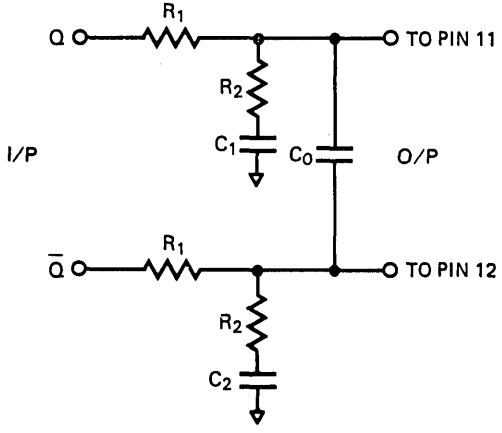


Figure 3. Phase Lag Filter

PCM Line Receiver & Clock Recovery Circuit

GENERAL DESCRIPTION

The XR-T5750 is a monolithic bipolar IC designed for PCM line receiver applications operating at T1, T148C, T1C and 2 Mbit/s data rates. It provides all the active circuitry required to perform automatic line build out (ALBO), threshold detection, positive and negative data and clock recovery using a crystal filter.

Clock recovery using an LC tank circuit instead of a crystal filter is also available as XR-T5650.

FEATURES

On Chip Positive and Negative Data, Clock Recovery
Less than 10 ns Sampling Pulse Over the Operating Range
Double Matched ALBO Ports
SIngle 5.1 V Power Supply
2 M Bit/s Capability
Clock Recovery using Crystal Filter

APPLICATIONS

T1 PCM Line Receiver
T148C LIne Receiver
T1C PCM Line Receiver (requires external amplifier)
General Purpose Bipolar Line Receiver
HDB3 Line Receiver
B8ZS Line Receiver

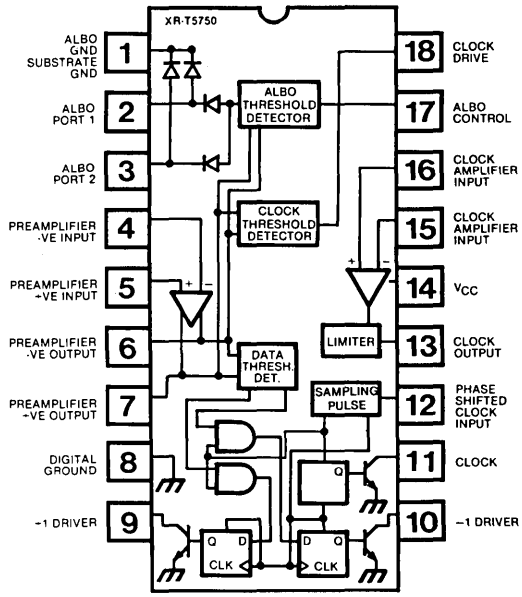
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to +10 V
Supply Voltage Surge (10 ms)	+25 V
Input Voltage (except Pins 2,3,4,17)	-0.5 to 7 V
Input Voltage (Pins 2,3,4,17)	-0.5 to +0.5 V
Data Output Voltage (Pins 10,11)	20 V
Voltage Surge (Pins 5,6,10,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5750	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-T5750 is designed for interfacing T1, T148C and 2 Mbit/s PCM carrier lines on plastic or pulp insulated cables. It can also be used at T1C rate (3.152 M bit/s) with external gain. Since it outputs plus and minus ones on a bipolar pulse stream together with the clock, it can be used to interface systems having different line codes like AMI, AMI-B8ZS or AMI-HDB3.

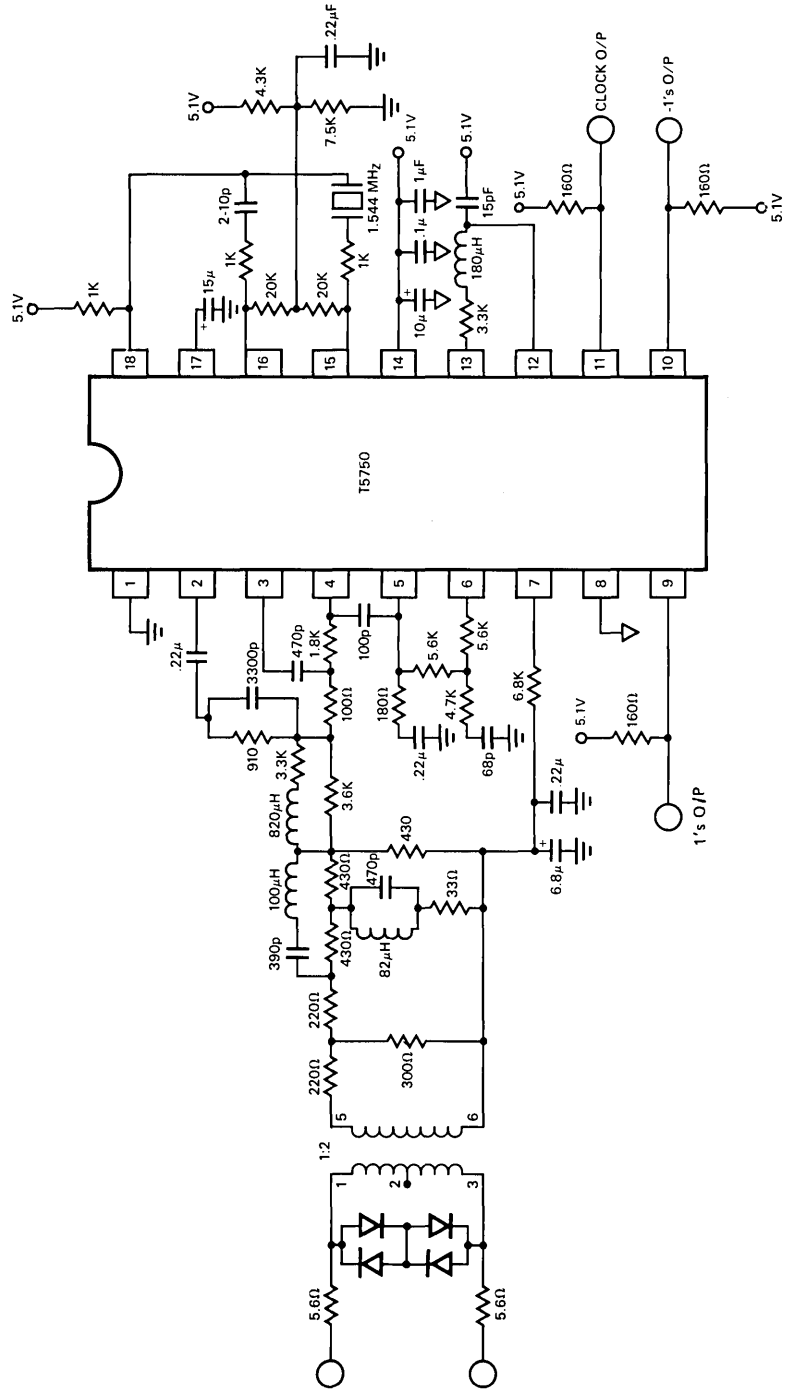
The XR-T5750 is a modified version of XR-T5720 PCM repeater IC. It contains all the active circuitry needed to build a PCM line receiver up to 6300 ft. cable length. The preamplifier, the clock amplifier, threshold detectors, data latches and output drivers are similar to the ones on XR-T5720. Clock extraction is done by means of a crystal filter circuit.

In addition to plus and minus one outputs, a synchronous clock signal is made available at Pin 11 by deleting one of the ALBO ports on XR-T5720 thus leaving two matched ALBO ports. All outputs have high current open collector transistors.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.1 V ± 5%, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Supply Current		24	30	mA	ALBO Off
	Clock & Data Output					
	Output Leakeage Current		0	100	µA	$V_{pull\text{-}up}$ = 15 V
	Amplifier Pin Voltages	2.4	2.9	3.4	V	At DC Unity Gain
	Amplifier Output					
	Offset Voltage	-50	0	50	mV	R_S = 8.2 kΩ
	Voltage Swing	2.2			V	Measured Differentially from Pin 7 to Pin 6
	Amplifier Input					
	Bias Current			5	µA	
	ALBO on Current	3			mA	
	Drive Current		1		mA	
AC CHARACTERISTICS						
	Pre Amplifier					
	AC Gain @ 1 MHz		50		dB	
	Input Impedance	20			kΩ	
	Output Impedance			200	Ω	
	Clock Amplifier					
	AC Gain		32		dB	
	-3 dB Bandwidth	10			MHz	
	Delay		10		ns	
	Output impedance			200	Ω	
	ALBO					
	Off Impedance	20			kΩ	
	On Impedance			25	Ω	
CLOCK, DATA OUTPUT BUFFERS						R_L = 130Ω, $V_{pull\text{-}up}$ = 5.1 V ± 5%
	Rise Time		30		ns	
	Fall Time		30		ns	
	Output Pulse Width		244		ns	
	Sample Pulse Width		10		ns	
	V_{OL}		0.7		V	
	I_L sink		35		mA	
THRESHOLDS						
	ALBO	1.4	1.5	1.6	V	
	Clock Drive Current Peak		1.0		mA	At V_O = V_{ALBO} Threshold
CLOCK THRESHOLD						
	% of ALBO	63	68	75	%	
DATA THRESHOLD						
	% of ALBO	40	46	52	%	



T5750 1.544 M BITS/S HIGH $\bar{Q}$ PCM LINE RECEIVER APPLICATION CIRCUIT

Section 2 – Telecommunication Products

Monolithic PCM Repeater

GENERAL DESCRIPTION

The XR-C240 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rate on T1-type PCM lines.

The XR-C240 monolithic IC is packaged in a hermetic 16-Pin DIP package, and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

Compared to conventional repeater designs using discrete components, the XR-C240 monolithic repeater IC offers greatly improved reliability and performance, along with significant savings in power consumption and system cost.

FEATURES

Contains all Active Components of PCM Repeater
On-Chip ALBO Port
High-Current Output Drivers
Low-Power Consumption
Increased Reliability over Discrete Designs
2 Megabit Operation Capability

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 M Bit/s Systems

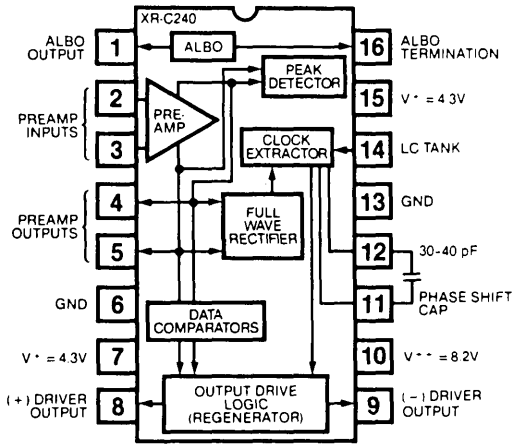
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to 10 V
Input Voltage (Except Pin 1,16)	-0.5 to +7 V
Input Voltage (Pin 7,16)	-0.5 to +0.5 V
Data Output Voltage (Pin 8,9)	+20 V
Voltage Surge (Pin 2,3,8,9) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C240	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-C240 contains all the active circuits required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier automatic line build out (ABLO), clock and data threshold detector circuits contained within the XR-C240. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO ports and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by driving an injection locked oscillator tuned to 1.544 MHz. The oscillator's sinusoidal waveform is amplified and phase shifted by 90 degrees with the help of a capacitor between Pins 11 and 12.

Data is sampled and stored in the output data latches by an internally generated sampling pulse. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

(Measured at 25°C with V++ = 8.2V, V+ = 4.3V, unless specified otherwise.)

PARAMETERS	LIMITS		UNIT	CONDITIONS
	MIN.	MAX.		
Supply Voltage:				
V++	7.79	8.61	V	Measured at Pin 10
V+	4.085	4.515	V	Measured at Pins 7 and 15
Supply Current:				
I_A	1.1	2.5	mA	
I_B	6	11	mA	Supply = 8.2V
Total Current	7.9	13.5	mA	
Preamplifier				
Input Offset Voltage, V_{OS}		15	mV	
Open Loop Differential Gain, A_O	50	54	dB	
Input Bias Current, I_B		4	μA	
Input Offset Current, I_{OS}		2	μA	
Input Impedance, R_{in}	50		kΩ	
Comparator Thresholds				
Peak Detector (ALBO) Threshold	±1.3	±1.6	V	Measured Differentially Across Pins 4 and 5
Full-Wave Rectifier Threshold	±0.9	±1.15	V	
Data Threshold	±0.28	±0.48	V	
Clock Extractor Section				
Tank Drive Impedance	50		kΩ	At Pin 14
Tank Drive Current				
"Zero" Signal Current	12	24	μA	
"One" Signal Current	80	220	μA	
Recommended Tank Q	100			
Phase Shifter Offset Voltage	-18	+18	mV	Voltage applied to Pins 7 and 14 to reduce differential voltage across Pins 11 and 12 to zero.
Output Drive Section				
				Voltage levels referenced to Pin 7
Output Voltage Swing	3.0		V	R_L = 100 Ω
Low Output Voltage	0.65	0.95	V	Referenced to Pin 7, I_L = 30 mA
Output Leakage Current		50	μA	
Output Pulse				
Maximum Pulse Width Error		±30	ns	
Rise and Fall Times		80	ns	

High-Performance PCM Repeater

GENERAL DESCRIPTION

The XR-C262 is a high-performance monolithic repeater IC for pulse-code modulated (PCM) telephone lines. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rates on T1-type PCM lines.

The XR-C262 operates with a single 6.8 volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock-extractor section of XR-C262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to their "off" state automatically, when there is no input signal present.

FEATURES

Contains all Necessary Active Components of a PCM Repeater
Uses L-C Tank for Clock Recovery
Low-Voltage Operation (6.8 volts)
Low-Current Drain (13 mA, typical)
High-Current Bipolar Output Drivers
On-Chip ALBO Equalizer
Automatic Zero-Input Shutdown
Increased Reliability Over Discrete Designs
2 Megabit Operation Capability

APPLICATIONS

PCM Repeater for T1 Systems
Repeater for 2 Megabit PCM Systems

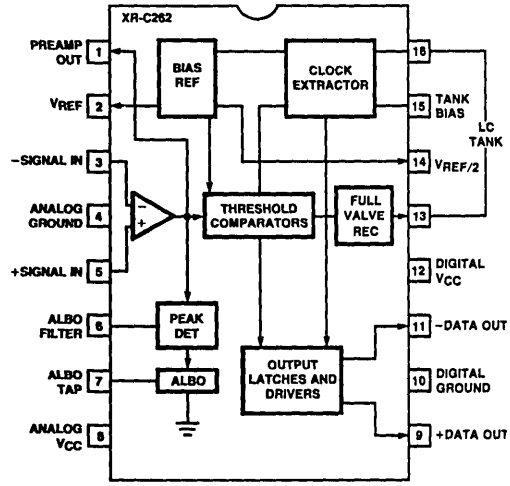
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
Supply Voltage	−0.5 to +10 V
Input Voltage (Except Pin 6,7)	−0.5 to +7 V
Input Voltage (Pin 6,7)	−0.5 to +0.5 V
Data Output Voltage (Pin 9,11)	+20 V
Voltage Surge (Pin 3,5,9,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262	Ceramic	−40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-C262 contains all the active functions required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the peamplifier automatic line build out (ALBO), clock and data threshold detector circuits contained within the XR-C262. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO port and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544 MHz.

Data is sampled and stored in the output data latches. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurrence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 6.8 V, T_A = −40°C to +85°C.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	−15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
Comparator Thresholds					Measured at Pin 1 relative to Pin 14
ALBO Threshold	0.75	0.9	1.1	V	
Clock Threshold	0.323	0.4	0.517	V	
Data Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					Measured at Pins 9 and 11
Output High Swing	5.9	6.8		V	R_L = 400 Ω
Output Low Swing	0.6	0.7	0.9	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	294	324	354	nsec	
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

High-Performance PCM Repeater

GENERAL DESCRIPTION

The XR-C262Z is a high-performance monolithic repeater IC for pulse-code modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rate on T1-type PCM lines.

The XR-C262Z operates with a single 6.8 volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock-extractor section of XR-C262Z uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to their "off" state automatically, when there is no input signal present.

FEATURES

Contains all Necessary Active Components of a PCM Repeater
Uses L-C Tank for Clock Recovery
Low-Voltage Operation (6.8 volts)
Low-Current Drain (13 mA, typical)
High-Current Bipolar Output Drivers
On-Chip ALBO Port
Automatic Zero-Input Shutdown
Increased Reliability Over Discrete Designs
2 Megabit Operation Capability
Pin-to-Pin Compatible with XR-C262 with Improved Switching Characteristics

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 M Bit/s Systems

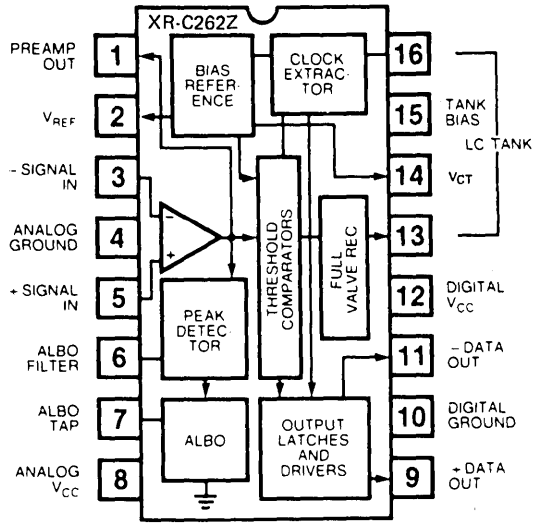
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to +10 V
Input Voltage (Except Pin 6,7)	-0.5 to +7 V
Input Voltage (Pin 6,7)	-0.5 to +0.5 V
Data Output Voltage (Pin 9,11)	+20 V
Voltage Surge (Pin 3,5,9,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262Z	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-C262Z contains all the active functions required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary, the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10^{-6}, the max allowable repeater to repeater spacing is about 6300 feet.

Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier automatic line build out (ALBO), clock and data threshold detector circuits contained within the XR-C262Z. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO ports and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544 MHz.

Data is sampled and stored in the output data latches. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 6.8 V, T_A = −40°C to +85°C, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
SUPPLY CURRENT					
Digital Current	6	10	13	mA	Measured at Pin 12
Analog Current	1.5	3.5	5	mA	Measured at Pin 8
Total Current		13	15	mA	
PREAMPLIFIER					
Input Offset Voltage	−15		+15	mV	Measured between Pins 3 & 5
Open Loop Gain	58	69	76	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.8	V	Measured at Pin 1
CLOCK RECOVERY SECTION					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			4.0	V	Measured at Pin 13
Clock Bias	3.8	4		V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
COMPARATOR THRESHOLDS					
ALBO Threshold	0.75	0.9	1.1	V	Measured at Pin 1 relative to Pin 14
Clock Threshold	0.323	0.4	0.517	V	
Data Threshold	0.323	0.4	0.517	V	
INTERNAL REFERENCE VOLTAGES					
Reference Voltage	5.0	5.45	5.65	V	Measured at Pin 2
Divider Center Tap	2.5	2.78	2.85	V	Measured at Pin 14
ALBO SECTION					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	3	mA	Drive Current available at Pin 6
OUTPUT DRIVER SECTION					Measured at Pins 9 & 11
Output High Swing	5.9	6.8		V	R_L = 400Ω
Output Low Swing	0.5	0.7	1.0	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	298	324	350	nsec	
Output Rise Time			80	nsec	
Output Fall Time			80	nsec	
Pulse Width Unbalance			15	nsec	

Low-Voltage PCM Repeater

GENERAL DESCRIPTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rate on T1-type PCM lines. It is packaged in a hermetic 16-Pin CERDIP package and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system, including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltage (6.3 volts and 4.3 volts) with a supply current of less than 13 mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance, along with significant savings in power consumption and system cost.

The XR-C277-5F is an improved version of XR-C277 with an internal feedback that improved the phase gain margin which enables the system to be more stable and less sensitive to PC board layouts.

Other versions of the XR-C277-5F are XR-C277-F and XR-C277-FL. XR-C277-F is an AC tested device of XR-C277-5F at 2Mbit while XR-C277-FL is the equivalen at 1.544 Mbit.

FEATURES

Contains all the Active Components of a PCM Repeater
Low-Voltage Operation (6.3 volts)
Low-Power Dissipation (13 mA)
On-Chip ALBO Port
High-Current Output Drivers
Increased Reliability over Discrete Designs
2 Megabit Operation Capability
Pin-Compatible with XR-C240

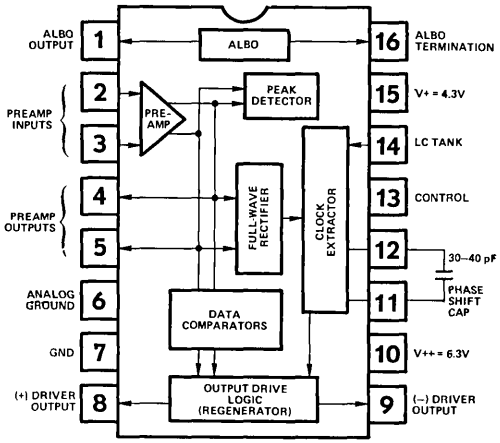
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to +10 V
Input Voltage (Except Pin 1,16)	-0.5 to +7 V
Input Voltage (Pin 1,16)	-0.5 to +0.5 V
Data Output Voltage (Pin 8,9)	20 V
Voltage Surge (Pin 2,3,8,9) (10 msec only)	50 V

SYSTEM DESCRIPTION

The XR-C277 contains all the active circuits required to build one side of a T1 or 2 M bit/s PCM repeater. T1 is the most widely used PCM transmission system, operating at 1.544 M bit/s. It can operate on either pulp or plastic insulated twisted pair cables. Although the cable gauge may vary the total cable loss should not exceed 36 dB at 772 kHz. For a 22 gauge pulp insulated cable and a bit error rate (BER) of less than 10-6 the max allowable repeater to repeater spacing is about 6300 feet.

FUNCTIONAL BLOCK DIAGRAM



Bipolar PCM signal is attenuated and dispersed in time as it travels along a transmission cable. This signal, when received, is amplified and reconstructed by the preamplifier automatic line build out (ALBO), clock and data threshold detector circuits contained within the XR-C277. Amplitude equalization and frequency spectrum shaping is achieved through the variable impedance of the ALBO port and its associated ALBO network.

Incoming pulse stream is full wave rectified and timing information is extracted by the clock threshold detector. Clock recovery is then achieved by pulsing a tank circuit tuned to 1.544 MHz. Either injection locking or pulsed tank type clock extraction are possible with the XR-C277. By grounding Pin 13, the circuit works in the injection lock mode. Floating (open) Pin 13 switches the XR-C277 to an pulse tank mode. The oscillator's sinusoidal waveform is amplified and phase shifted by 90 degrees with the help of a capacitor between Pins 11 and 12.

Data is sampled and stored in the output data latches by an internally generated sampling pulse. Buffer drivers are then enabled to produce precisely timed output pulses whose width and time of occurence are controlled by the regenerated clock signal.

ELECTRICAL CHARACTERISTICS

Test Conditions: +25°C, V++ = 6.3V ±5%, V+ = 4.4V ±5%, unless specified otherwise.

PARAMETERS	LIMITS			UNITS	CONDITIONS
	MIN.	TYP.	MAX.		
Supply Current					
I_A		3.5		mA	Measured at Pin 10
I_B		7.5		mA	Measured at Pin 15
Total Current	8	11	13	mA	(I_C + I_B)
Preamplifier					
Input Offset Voltage		1.5	15	mV	Measured at Pins 2 and 3
Input Bias Current		0.3	4	µA	Measured at Pins 2 and 3
Voltage Gain	44	48	51	dB	Single-ended Gain
Preamp Output Swing					Measured at Pins 4 and 5
High Swing	3.45	3.6	3.75	V	Maximum Voltage Swing
Low Swing	1.25	1.4	1.55	V	Minimum Voltage Swing
Output DC Level	2.47	2.55	2.72	V	
ALBO Section					
ALBO "Off" Voltage		10	75	mV	Measured from Pin 1 and 16 to Ground
ALBO "On" Voltage	0.6	0.87	1.1	V	Measured at Pin 1
ALBO "On Voltage	1.2	1.5	2.1	V	Measured at Pin 16
ALBO Threshold	1.35	1.50	1.65	V	Measured Differentially Across Pins 4 and 5
Differential Threshold	-75		+75	mV	Threshold Difference for Polarity Reversal at Pins 4 and 5
ALBO "On" Impedance		5	10	Ω	Measured at Pin 1
ALBO "Off" Impedance	20	50		kΩ	Measured at Pin 1
Comparator Thresholds					
Clock Threshold	68	73	78	%	% of ALBO Threshold
Data Threshold	47	50	53	%	% of ALBO Threshold
Clock Extractor					
Oscillator Current	10	14	20	µA	
Tank Drive Impedance		50		kΩ	
Recommended OSC. Q	100				
$I_{injection}/I_{OSC.}$	6.0	7	7.5		Ratio of Current Q_{1B} to Current in Q_{1A}
Output Driver					
Low Output Voltage	0.65	0.75	0.95	V	Measured at Pins 8 and 9 I_L = 15 mA
Output "Off" Current		5	100	µA	V_{out} = 20V
Output Pulse					
Max. Pulse Width Error			±30	n sec	
Rise Time			80	n sec	
Full Time			80	n sec	

APPLICATIONS

PCM Repeater for T1 Systems
PCM Repeater for 2 M Bit/s Systems

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C277	Ceramic	-40°C to +85°C
XR-C277-5F	Ceramic	-40°C to +85°C
XR-C277-F	Ceramic	-40°C to +85°C
XR-C277-FL	Ceramic	-40°C to +85°C

T1C PCM Repeater Chip Set

GENERAL DESCRIPTION

The IC pair, XR-C587 and XR-C588, provides all the active circuitry needed to form one side of a T1C PCM Repeater (3.152 MBits/sec). Each chip is packaged in a 16-Pin CERDIP package, with an operating temperature range of -40°C to +85°C. The supply voltage range is 6.0 to 6.8 V_{DC}, with a typical supply current for the pair of 16 mA.

The XR-C587 contains an amplifier, three ALBO ports, and an npn transistor. The amplifier is a modified version of the amplifier in Exar's XR-C262 T1 repeater chip. This amplifier has its own ground pin for isolation, as well as for eliminating the amplifier current drain if only the XR-C587 ALBO diodes and/or the transistor are used. Each of the three ALBO ports has a separate ground and one common drive input. Any number, up to three, can be used while eliminating current in any not used. The npn transistor is provided for incidental uses.

The XR-C588 contains a preamplifier, an ALBO drive output, a voltage reference, comparators, a clock recovery circuit, ECL latches and two output drivers. The XR-C588 is a modified version of XR-C262 for T1C performance. The amplifiers in the XR-C587 and XR-C588 are the same. The clock driver output is modified to drive a crystal and has higher gain. Both inputs to the clock amplifier are available. The clock amplifier may be biased, both from the center tap voltage (Pin 14), and the clock bias voltage (Pin 7).

Two options for the clock comparator threshold voltage are provided. Option 1 is 65% of ALBO threshold, and Option 2 is 50% (the same as C262).

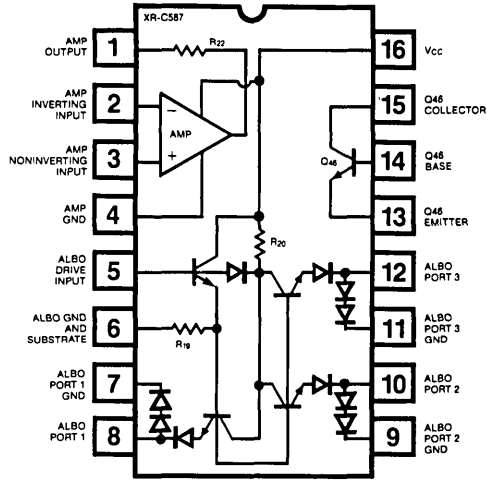
FEATURES

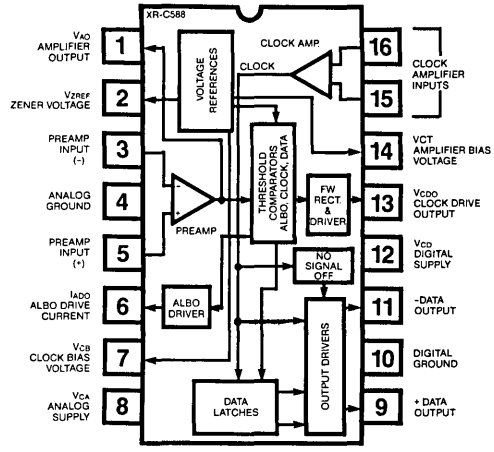
Modified Preamplifier with Improved Phase Margin
Separate Grounds for Preamplifier and ALBO Ports
Crystal Drive Capability for High Q Operation
Optional Clock Comparator Threshold Levels (50% & 65%)

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage	-0.5V to 10V
Digital Supply Voltage	-0.5V to 10V
Differential Input Voltage	-5V to 5V
Output Voltage	-0.5V to 20V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Lead Soldering (10 seconds)	300°C

FUNCTIONAL BLOCK DIAGRAMS





ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C587	Ceramic	-45°C to +85°C
XR-C588	Ceramic	-45°C to +85°C

ELECTRICAL CHARACTERISTICS – XR-C587/C588

Test Conditions: T_A = -40°C to +85°C, at a supply voltage of V_{CC} = 6.0V to 6.8V dc, Unless otherwise specified.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
SUPPLY					
Supply Voltage	6.0	6.4	6.8	V dc	
Supply Current	2.3	2.7	3.3	mA	All ALBO Pins open V_{CC} = 6.3V
ALBO Bias Current	200	280	360	mA	ALBO Grounds open ALBO drive pin at 3.5V (≈ 5 $V_{BE's}$)
AMPLIFIER					
DC open-loop gain	54	60	68	dB	1V p-p output level, R_L = 4 kΩ
AC gain at 1 MHz	34			dB	returned to V_{CM} = 2.7V
Corner Frequency		110		kHz	
Input Offset Voltage	-15	0	+15	mV	R_S = 10 kΩ to both inputs
Input Bias Current		1	4	μA	
Output Sink Current	300	400	500	μA	
ALBO					
One Common Drive Input, Three Ports, Each With Its Own Ground					
Max ALBO Current	2.5	4.5	6	mA	Total current to Ground through all ALBO Ground Pins, Drive input returned to V_{CC} = 6.0V through 51 kΩ.
ALBO Current Mismatch	-5	0	+5	%	Measured with 1 mA nominal level in each ALBO Ground Pin.
ALBO Port Voltage	1.2V	1.45	1.7V	V dc	Two V_{BE} above Ground, 1 mA in each Port.
ALBO OFF Impedance	10			kΩ	Drive input and ALBO Ground Pins Grounded Frequency = 1.5 MHz
SINGLE TRANSISTOR					
Beta (β)	75	150	400		V_{CE} = 6.8V, I_C = 100 mA
Leakage	0.01	1	5	μA	V_{CEO} = 6.8V

ELECTRICAL CHARACTERISTICS – XR-C588

Test Conditions: T_A = -40°C to +85°C, at a supply voltage of $V_{CC} = V_{CA} = V_{CD}$ = 6.0V to 6.8V dc, Unless otherwise specified.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
SUPPLY CURRENTS					
I_{CA}, V_{CA} Supply Current	1.8	3.5	5	mA	V_{CA} is Analog Supply Voltage
I_{CD}, V_{CD} Supply Current	5	8	12	mA	V_{CD} is Digital Supply Voltage Outputs off, $V_{AO} = V_{CT}$
I_{CCT}, $I_{CA} + I_{CD}$	7	12.5	14.5	mA	Outputs off, $V_{AO} = V_{CT}$
AMPLIFIER					
Same specification as amplifier in C587					V_{AO} = Amplifier Output Voltage
VOLTAGE REFERENCES					
V_{zref}, Zener Voltage	5.0	5.4	5.65	Volts	No external loading
V_{CT}, Center Tap Voltage	2.35	2.70	2.90	Volts	No external loading
V_{CB}, Clock Bias	3.5	4.0	4.3	Volts	No external loading
THRESHOLD VOLTAGES					
ALBO Comparator					
V_{APD}^+, ALBO + peak detector voltage	.75	.9	1.05	Volts	V_{AO} measured w/respect to V_{CT}, with I_{ADO} = 100 µA
V_{APD}^-, ALBO - peak detector voltage	-.75	-.9	-1.05	Volts	
$V_{APD}^+ - V_{APD}^-$	-50	0	50	mV	
Data Comparators					
V_{DT}^+, + data threshold	42	48	53	% of V_{APD}^+	V_{AO} varied, clock drive input = 3.152 MHz sine wave at .5V pp. Detect onslaught of output pulses at 3.152 MHz, measure V_{AO}.
V_{DT}^-, - data threshold	42	48	53	% of V_{APD}^-	Same as for V_{DT}^+
$V_{DT}^+ - V_{DT}^-$	30	0	30	mV	
Clock Comparator					
V_{CLK}^+, + clock threshold	*57/42	62/48	67/53	% of V_{APD}^+	V_{AO} varied, detect 100 mV change in V_{CDO}.
V_{CLK}^-, - clock threshold	*57/42	62/48	67/53	% of V_{APD}^-	
$V_{CLK}^+ - V_{CLK}^-$	35/30	0/0	35/30	mV	

* Upper limits are for Option 1, lower limits are for Option 2.

ELECTRICAL CHARACTERISTICS – XR-C588 (Continued)

Test Conditions: T_A = -40°C to +85°C, at a supply voltage of $V_{CC} = V_{CA} = V_{CD}$ = 6.0V to 6.8V dc, Unless otherwise specified.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CLOCK DRIVE OUTPUT V_{CDO}					
A_{CD}+, gain from V_{AO} to V_{CDO}	-2.7	-3.0	-3.3	V/V	V_{AO} changed from V_{CLK}+ to (V_{CLK}+ + .5V) measure change in V_{CDO}.
A_{CD}-	2.7	3.0	3.3	V/V	V_{AO} changed from V_{CLK}- to (V_{CLK}- - .5V) measure change in V_{CDO}.
A_{CD}+/A_{CD}-	-1.1	-1.0	-.9		
V_{CDO} High	-1.8	-1.5	-1.1	V	V_{CDO} measured w/respect to V_{CC}. V_{AO}=V_{CT}
V_{CDO}+ Low			-3.2	V	V_{CDO} measured w/respect to V_{CC}. V_{AO} = V_{CT} + 1.5 volts.
V_{CDO}- Low			-3.2	V	V_{CDO} measured w/respect to V_{CC}. V_{AO} = V_{CT} – 1.5 volts.
CLOCK AMPLIFIER					
V_{CACM}, Clock input Common Mode Bias Voltage	2.35		4.3	V	V_{CT} or V_{CB} can be used as V_{CACM}
Input Offset Voltage	-15		15	mV	
Input Bias Current		1	4	μA	
ALBO DRIVE I_{ADO}					
I_{ADO} Max	.7	1.5	3.0	mA	V_{AO} at V_{CT} ± 1.5 volts I_{ADO} measured to Gnd.
I_{ADO} Off			10	μA	V_{AO} = V_{CT}, I_{ADO} measured to Gnd.
OUTPUT DRIVER					
I_O± Leak		100		μA	Output off and returned to 20 volts.
V_{OL}±	.5	.8	1.0	Volts	I_{LOAD} = 15 mA
V_{OL}+ - V_{OL}-	-80	0	+80	mV	I_{LOAD} = 15 mA
T_{OPW}±, output pulse width	143	159	175	nsec	50% Pts. R_L = 350Ω
T_{OPW}+ - T_{OPW}-	-10	0	10	nsec	
T_{RT}±, Rise time			40	nsec	R_L = 350Ω 20% to 80% Pts.
T_{FT}±, Fall time			40	nsec	R_L = 350Ω 20% to 80% Pts.
NO SIGNAL PROTECTION					With no clock signal, Output will be off.

PRINCIPLES OF OPERATION

T1C is a digital line system operating at 3.152 Mbits/sec, very similar, in principle, to the T1 line system. It provides 48 digitally encoded and time division multiplexed voice channel repeaters containing 2 regenerators which have the approximate spacing of 6300 ft. Power is provided by a simplex arrangement with a line current of 120 mA. Two regenerators share a common power supply. Basic repeater functions, namely reshaping, retiming and regenerating, are performed for cable losses from 6 to 54 dB, as measured at 1.576 MHz.

The bipolar PCM signal, which is attenuated and distorted due to transmission medium, is applied to a preamplifier through a pulse-shaping network. This network, and the variolosser diodes, forms the ALBO circuitry which provides attenuation and shaping to automatically adjust for varying cable characteristics.

A feedback network is used around the preamplifier for gain equalization, as well as to reject out-of-band noise. The output of the preamplifier is controlled to swing between two established peak levels, and drives a set of data comparators which are internally biased from a voltage reference and precision voltage divider network. The preamplifier output is sliced at various voltage levels to eliminate the effects of baseline noise. This output is full wave rectified, and applied to a crystal time extraction circuit. The sinusoidal wave shape from the time extraction circuit is differentially coupled to a clock slicer block to produce the internal square wave clock signal.

The regeneration of data is achieved through a pair of data comparators and ECL latches. The data slicing levels are set to ± 50% of the preamplifier output peak voltages ECL latch outputs and clock signal are then gated to produce two precisely timed output data signals. The positive and negative data paths are separate but identical in design.

A zero input protection circuit is provided for the dual task of preventing the output switches from latching in an ON state, as well as reducing the likelihood of output pulses with no input signal.

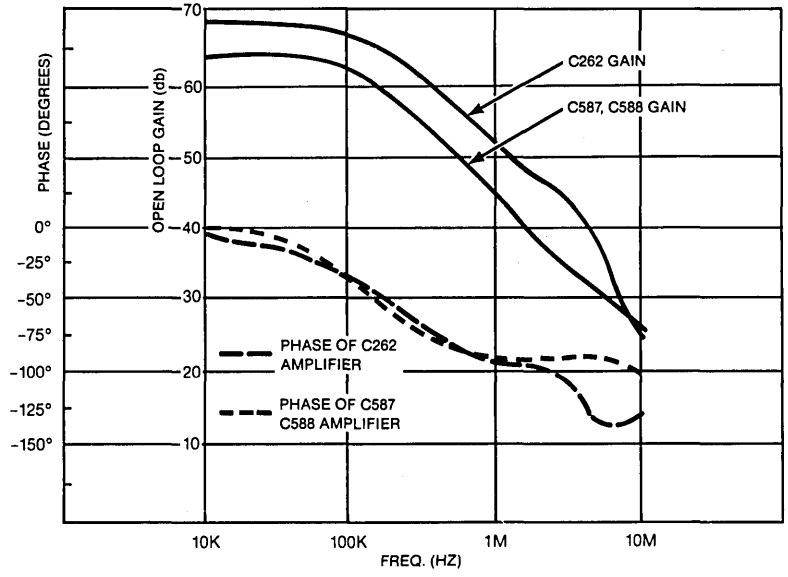


Figure 1: Bode Plot of C262 and C587/C588 Amplifiers.

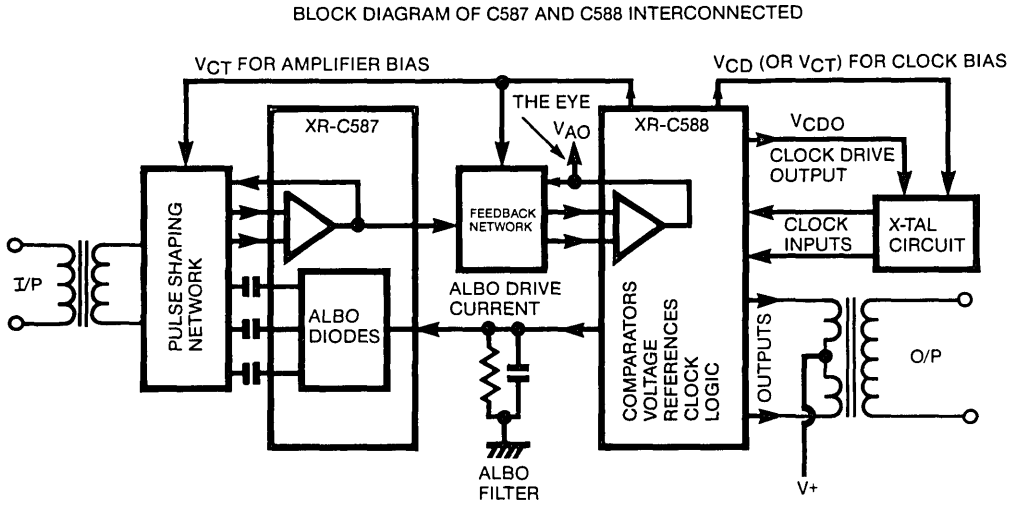


Figure 2: Block Diagram of C587/C588 Interconnected.

T1, T148C, & 2 M Bit/s PCM Line Repeater

GENERAL DESCRIPTION

The XR-T5600/T5620 is a bipolar monolithic repeater IC designed for PCM carrier systems operating at 1.544 M bit/s (T1), 2 M bit/s, or 2.37 M bit/s (T148C). It provides all of the active circuits required for one side of a PCM repeater. A crystal filter clock extraction version of XR-T5600/T5620 is available as XR-T5700/T5720.

FEATURES

Single 5.1 V Power Supply
Less than 10 ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports
2 M Bit/s Capability

APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
European 2 M Bit/s PCM Repeater
T1C PCM Repeater (requires external preamplifier)

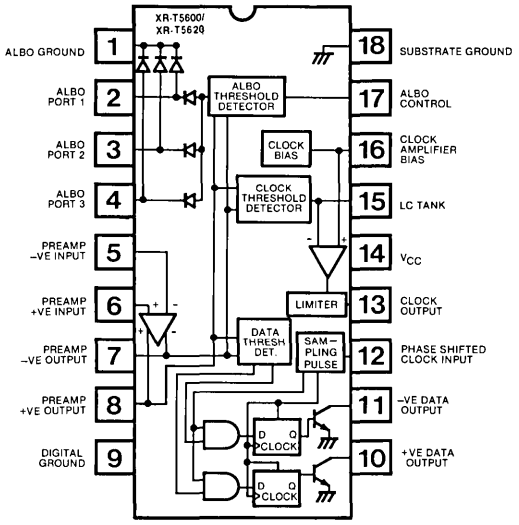
ORDERING INFORMATION

Part Number	Package	Operation Temperature
XR-T5600	Plastic	−40°C to 85°C
XR-T5620	Plastic or Ceramic	−40°C to 85°C

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to +10 V
Supply Voltage Surge (10 ms)	+25 V
Input Voltage (except Pin 2,3,4,17)	-0.5 to 7 V
Input Voltage (Pin 2,3,4,17)	-0.5 to +0.5 V
Data Output Voltage (Pin 10, 11)	20 V
Voltage Surge (Pin 5,6,10,11) (10 msec only)	50 V

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-T5600/T5620 performs most of the functions required for one side of a PCM repeater operating at 2 M bit/s or similar baud rate. The integrated circuit amplifies the received positive and negative pulses and feeds them into Automatic Line Build-out (ALBO), clock and data threshold detectors, see Figure 1. The ALBO threshold detector ensures that the received pulses at Pins 7 and 8 have the correct amplitude and shape. This is carried out by controlling the gain and frequency shaping of the ALBO network with three variable impedance ALBO ports.

The clock threshold detector extracts timing information from the pulses received at Pins 7 and 8 and passes it into the external tank coil at Pin 15. The sinusoidal-type waveform is amplified into a square wave at Pin 13, and forwarded through an external phase shift network into Pin 12. This waveform provides the data sampling pulse which opens latches into which the data from the data threshold detectors is passed. The resulting pulses are stored for half a bit period (normally 488 ns) in the latches. They appear as half-width output pulses at Pins 10 and 11.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5.1\ V \pm 5\%$, unless specified otherwise (see Figure 1).

PARAMETERS	PINS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Current	14		22	30	mA	
Data Output Leakage Current	10,11		0	100	μA	$V_{pull\text{-}up} = 15\ V$, $V_{CC} = 5.35\ V$
ALBO Port Off Voltage	2,3,4		0	0.1	V	
Amplifier Pin Voltage	5,6,7,8	2.4	2.9	3.4	V	
DYNAMIC CHARACTERISTICS AMPLIFIER						
Output Offset Voltage		-50	0	50	mV	$R_S = 8.2\ k\Omega$
AC Gin @ 1 MHz		47	50	53	dB	
Input Impedance		20			kΩ	
Output Impedance				200	Ω	
ALBO						
ALBO Off Impedance		20		25	kΩ	
ALBO On Imepdance				25	Ω	
THRESHOLDS						
ALBO Threshold		1.4	1.5	1.6	V	
Clock Threshold as % of ALBO Threshold		68		80	%	
DATA Threshold as % of ALBO Threshold		42		49	%	
Clock Drive Current		0.7		1.4	mA	At $V_O = V_{ALBO}$ Threshold
OUTPUT STAGES						$R_L = 130\Omega$, $V_{pull\text{-}up} = 5.1 \pm 5\%$
Output Pulse Rise Time				40	ns	
Output Pulse Fall Time				40	ns	
Output Pulse Width		224	244	264	ns	
Output Pulse Width Differential		-10		+10	ns	
Buffer Gate Voltage (Low)		0.65		0.95	V	
Buffer Gate Voltage Differential		-0.15		0.15	V	

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise stated, all characteristics shall apply over the operating temperature range of -40°C to +85°C with V_{CC} = 5.1 V ± 5%, all voltages referred to ground = 0 V.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL (Ref. Figure 2)							
I_S	Supply Current	14		22	30	mA	
I_{LD}	Data Output Leakage Current	10,11		6	100	µA	From V_S (See Note 1)
	Amplifier Pin Voltages	5,6,7,8	2.4	2.9	3.4	V	
	ALBO Ports Off Voltage	2,3,4		0	0.1	V	

Note: 1. V_S = 15 V, V_{CC} = 5.35 V

AMPLIFIER (Ref. Figure 2, Only Pins 1, 9, 10...18 connected)							
	Input Offset Voltage	5 & 6	-10		+10	mV	R_S = 8.2 kΩ (See Note 1)
	Input Bias Current	5 & 6	0		5	µA	R_S = 8.2 kΩ (See Note 1)
	Input Offset Current	5 & 6	-1		1	µA	R_S = 8.2 kΩ (See Note 1)
	Output Offset Voltage	7 & 8	-50	0	50	mV	R_S - 8.2 kΩ (See Note 1)
	Common Mode Rejection Ratio	7 & 8	30			dB	V_{CC} ±10%
	Output Voltage Swing	7 & 8	2.2			V	

Note: 1. R_S = Source Resistance

CLOCK AMPLIFIER (Ref. Figure 2, Disconnect Pin 15 from Pin 16)							
	Input Offset Voltage	15 & 16	0.5		6	mV	R_S = 10 kΩ (See Note 1)
	Input Bias Current	15 & 16			10	µA	T = 25°C
	Max. Output Voltage	13	0.7			V	
	Min. Output Voltage	13	0.7			V	
	Max./Min. Output Voltage Difference	–	0.7		50	mV	

Notes:
1. R_S = Source resistance, Pin 15 positive with respect to Pin 16
2. Pin 15 = Pin 16 = 3.6 V
3. Pin 15 = 2.6 V, Pin 16 = 3.6 V
4. Pin 15 = 4.6 V, Pin 16 = 3.6 V
5. Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
ALBO (Ref. Figure 2)							
	On Current	1	3			mA	V_8-V_7 = ± 1.75 V
	Drive Current	17	0.4		1.4	mA	V_8-V_7 = ± 1.75 V
	Resistance Pin 17 to Ground		35	50	70	kΩ	Not Powered

DYNAMIC CHARACTERISTICS

AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain @ 1 MHz	5 to 8	47	50	53	dB	
Z_{in}	Input Impedance	5	20			kΩ	(See Note 1)
Z_{out}	Output Impedance	7,8			200	Ω	(See Note 2)

Notes: 1. At 1 MHz, AC ground Pins 7 and 8, disconnect 51 Ω resistor, allow for in-circuit R,C
2. At 1 MHz, use Figure 2

CLOCK AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain	15, 16 to 13	32			dB	(See Note 1)
BW	-3 dB Bandwidth	15, 16 to 13	10		mHz		(See Note 2)
t_d	Delay	15 to 13	8		12	ns	(See Note 3)
Z_{out}	Output Impedance	13			200	Ω	(See Note 4)

Notes: 1. Remove dc offset, at 2.048 MHz, Pin 13 = 1 V pk-pk sine wave
2. Remove dc offset, Pin 13 = 1 V pk-pk sine wave
3. Remove dc offset, Pin 15 = 2 V pk-pk sine wave; delay from Pin 15 negative-going zero crossover to Pin 13 positive edge
4. Remove dc offset, at 2.048 MHz

ALBO (Ref. Figure 2)							
	Off Impedance	2,3,4	20			kΩ	(See Note 1)
	Intermediate Impedance Difference	2,3,4			5	%	(See Note 2)
	On Impedance	2,3,4			25	Ω	(See Note 3)
	Transconductance	7/8 to 1			0.03	dB	(See Note 4)

Notes: 1. At 1 MHz, allow for in-circuit R,C
2. At 1 MHz, V_8-V_7 adjusted for current at Pin 1 = 100 μA
3. At 1 MHz, V_8-V_7 adjusted for ± 1.75 V
4. At 1 MHz, change in V_8-V_7 for current at Pin 1 = 10 μA to 100 μA

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
THRESHOLD VOLTAGES (Ref. Figure 3)							
	ALBO Threshold +ve	8-7	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold -ve	7-8	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold Difference	–	-5	0	5	%	(See Note 3)
	Clock Drive on Current (peak) +ve	18		1.0	1.4	mA	(See Note 4)
	Clock Drive on Current (peak) -ve	18		1.0	1.3	mA	(See Note 5)
	Clock Drive on Current Difference	–	-5	0	5	%	(See Note 3)
	Clock Threshold +ve	87	68		80	%	(See Notes 1, 6, 8)
	Clock Threshold -ve	7-8	68		80	%	(See Notes 1, 7, 8)
	Clock Threshold Difference	–	-5	0	5	%	(See Note 3)
	Data Threshold +ve	8-7	44	46	48	%	(See Notes 1,8,9,11)
	Data Threshold -ve	7-8	44	46	48	%	(See Notes 1,8,10,11)
	Data Threshold Difference	–	-3	0	3	%	(See Note 3)

Notes: 1. Pk/pk voltage at Pins 7 and 8 of a 1 MHz sine wave derived through amplifier and measured differentially
2. Pk/pk voltage at Pins 7 and 8 adjusted for current at Pin 1 = 3 mA
3. Calculation only
percentage difference calculated from $\left(\frac{\text{higher value}}{\text{lower value}} - 1\right) \times 100$ %
4. V_8-V_7 adjusted to ALBO threshold +ve voltage, ref. Pin 16 = 3.6 V
5. V_7-V_8 adjusted to ALBO threshold -ve voltage, ref. Pin 16 = 3.6 V
6. V_8-V_7 adjusted to peak current at Pin 18 = ½ (clock drive on current peak +ve)
7. V_7-V_8 adjusted to peak current at Pin 18 = ½ (clock drive on current peak -ve)
8. Figure taken as a percentage of lower ALBO threshold
9. V_8-V_7 increased until 1 MHz PRF on counter at Pin 10
10. V_7-V_8 increased until 1 MHz PRF on counter at Pin 11
11. With 2,048 MHz 2 V pk-pk sine wave to Pin 15 with 180 μH in parallel with 36 Ω to Pin 16 = 3.6 V

OUTPUT STAGES (Ref. Figure 3. Use 180 μH inductor between Pins 15 and 16. Apply 2.048 MHz 2V pk/pk to Pin 15.)							
t_r	Output Pulse Rise Time +ve	10			40	ns	10% - 90%
t_r	Output Pulse Rise Time -ve	11			40	ns	10% - 90%
t_f	Output Pulse Fall Time +ve	10			40	ns	10% - 90%
t_f	Output Pulse Fall Time -ve	11			40	ns	10% - 90%
t_W	Output Pulse Width +ve	10	224	244	264	ns	at 50%
	Output Pulse Width -ve	11	224	244	264	ns	at 50%
Δt_W	Output Pulse Width Difference	–	-10		10	ns	
V_{OL}	Buffer Gate Voltage (low) +ve	10	0.65		0.95	V	
V_{OL}	Buffer Gate Voltage (low) -ve	11	0.65		0.95	V	
ΔV_{OL}	Buffer Gate Voltage Difference	–	-0.15		0.15	V	

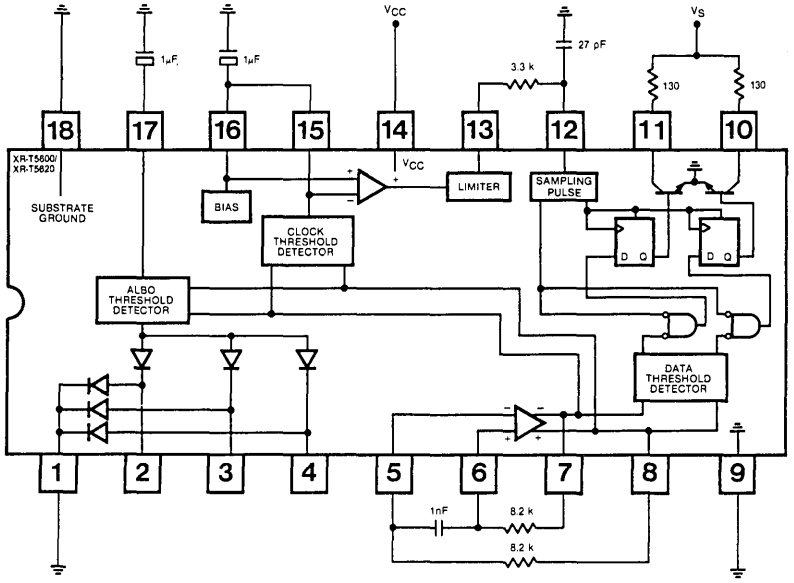


Figure 2. D.C. Parameter Test Circuit

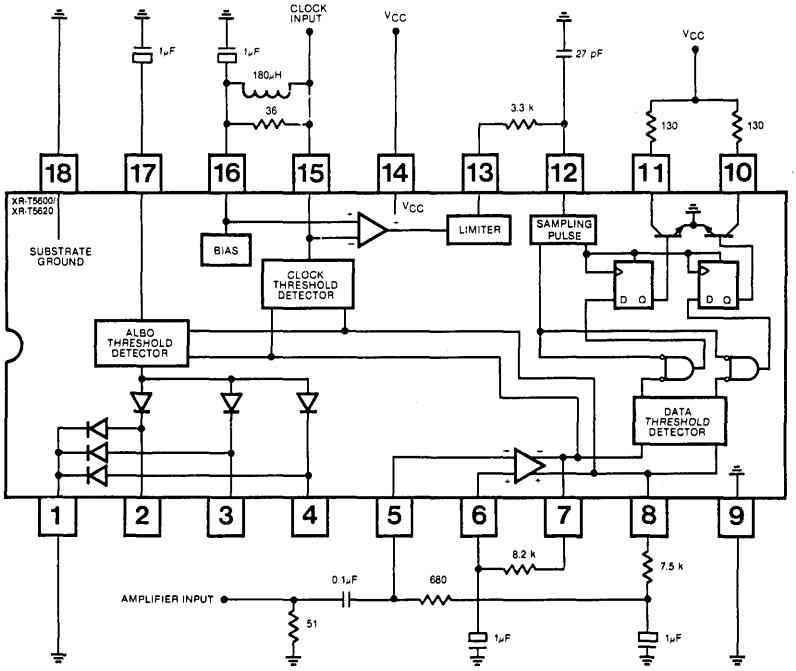


Figure 3. A.C. Parameter Test Circuit

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
SAMPLE PULSE WIDTH (Ref. Figure 4, Cy = 27 pF)							
	Sample Pulse Width			10		ns	(See Notes 1...5)

Notes:
1. The sample pulse width is the period during which the output latches are opened to accept a signal above the data hold at Pin 7 or 8 and cause a half-width output pulse at Pin 11 or 10 respectively.
2. Sample pulse width is specified with a 2.048 MHz TTL waveform at clock input (Pin 15) and a 2,400 MHz Schottky TTL waveform at amplifier input in the circuit of Figure 4. Figure 7 shows the relevant IC waveforms.
3. Monitor the frequency of coincident output pulses at Pins 10 and 11 either directly or through ouput circuit to frequency counter.
4. Sample pulse width = X ns + (0,1 x measured frequency in kHz) ns where X is the mean rise/fall times of the waveform at Pin 8 between 25% and 75%.
5. X to be within the range of 10 nx < X < 12 ns. THis requires HF layout techniques with the amplifier operated closed loop.

SAMPLE PULSE GENERATOR INPUT WAVEFORM (pin 12 - Ref. Figure 4, Cy = 40 pF)							
	Output Pulse Frequency	10,11	1,024 -100 ppm	1,024	1,024 +100 ppm	MHz	(See Note 1)

Note: 1. With 2,048 MHz ±100 ppm TTLwaveform at clock input. With half of above waveform frequency at amplifier input.

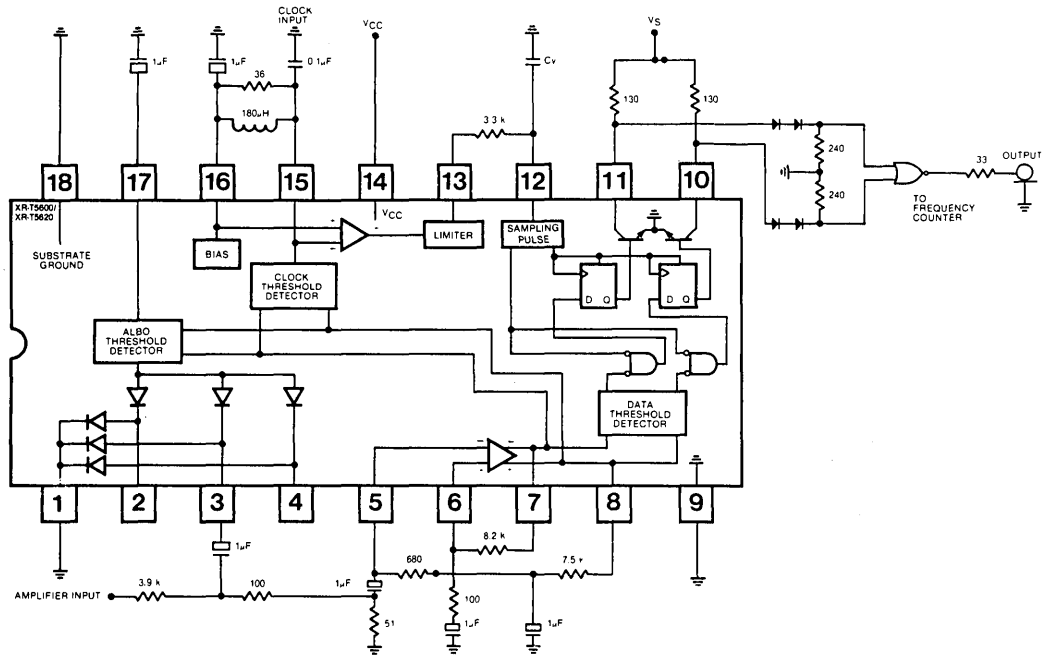


Figure 4. Sampling Pulse Test Circuit

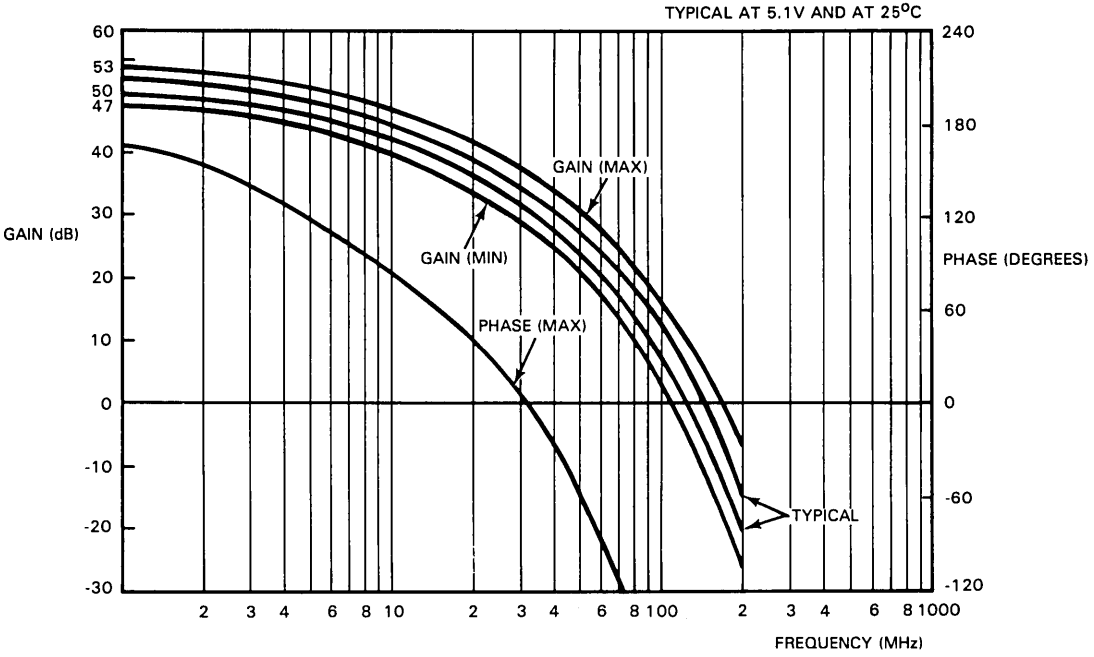


Figure 5. Typical and Limiting Values of Gain and Phase

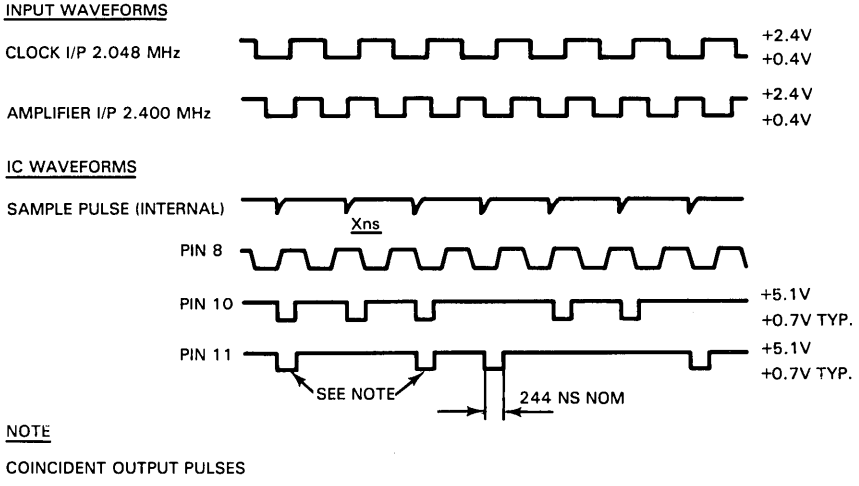
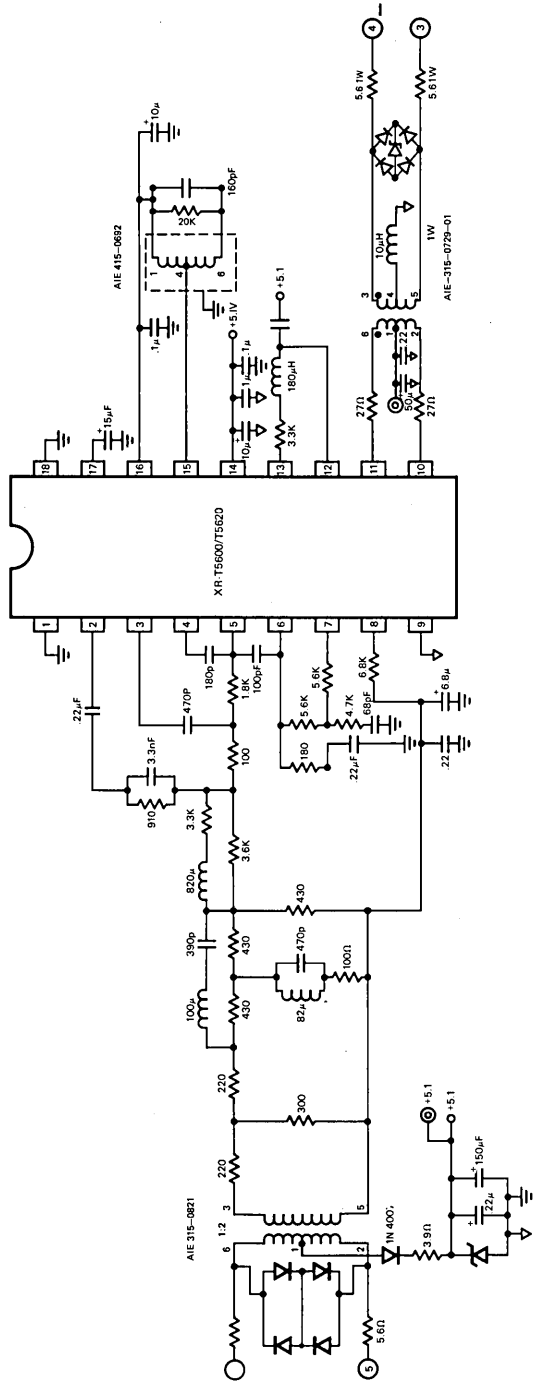
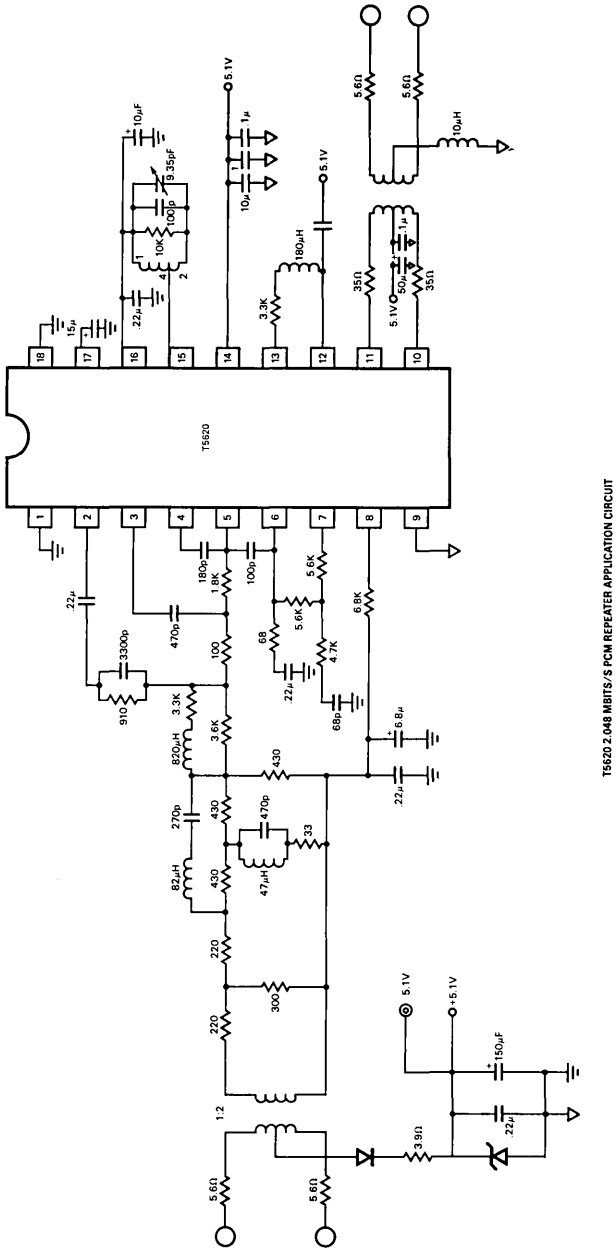


Figure 6. IC Waveforms for Measuring Sampling Pulse Width



T5600/T5620 1.544 M BITS/SEC REPEATER APPLICATION CIRCUIT



T5620 2.048 MBITS/S PCM REPEATER APPLICATION CIRCUIT

T1, T148C, & 2 M Bit/s PCM Line Repeater

GENERAL DESCRIPTION

The XR-T5700/T5720 is a bipolar monolithic repeater IC that provides all the active circuits required for one side of a PCM repeater. The IC is designed for clock extraction by using a crystal filter.

The primary applications of XR-T5700 are T1 (1.544 M bit/s), T148C (2.37 M bit/s), and European 2 M bit/s PCM repeater.

A tank circuit clock extraction version of XR-T5700-T5720 is available as XR-T5600/T5620.

FEATURES

Crystal Clock Extraction
Single 5.1 V Power Supply
Less than 10 ns Sampling Pulse over the Operating Range
Triple Matched ALBO Ports

APPLICATIONS

T1 PCM Repeater
T148C PCM Repeater
T1C PCM Repeater (requires external preamplifier)
European 2 M Bit/s PCM Repeater

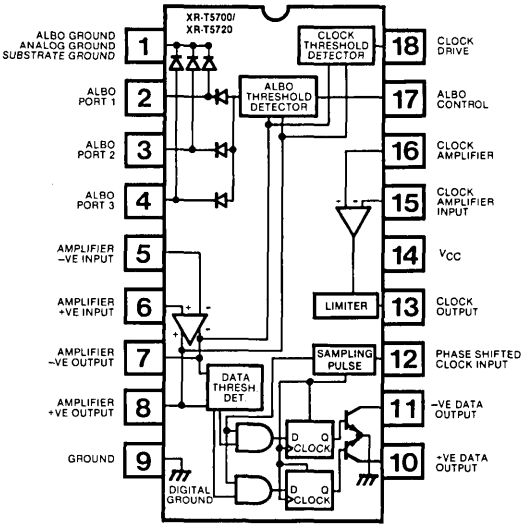
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C
Supply Voltage	-0.5 to +10 V
Supply Voltage Surge (10 ms)	+25 V
Input Voltage(except Pins 2,3,4,17)	-0.5 to 7 V
Input Voltage (Pins 2,3,4,17)	-0.5 to +0.5 V
Data Output Voltage (Pins 10, 11)	20 V
Voltage Surge (Pins 5,6,10,11) (10 msec only)	50 V

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5700/T5720	Ceramic	-40°C to +85°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-T5700/T5720 performs most of the functions required for one side of a PCM repeater operating at 2 M bit/s or similar baud rate. The integrated circuit amplifies the received positive and negative pulses and feeds them into Automatic Line Build-out (ALBO), clock and data threshold detectors, see Figure 1. The ALBO threshold detector ensures that the received pulses at Pins 7 and 8 have the correct amplitude and shape. This is carried out by controlling the gain and frequency shaping of the ALBO network with three variable impedance ALBO ports.

The clock threshold detector extracts timing information from the pulses received at Pins 7 and 8 and passes it into open collector Pin 18. A crystal filter is connected from Pin 18 to clock amplifier input Pins 16 and 15. The sinusoidal-type waveform is amplified into a square wave at Pin 13, and forwarded through an external phase shift network into Pin 12. This waveform provides the data sampling pulse which opens latches into which the data from the data threshold detectors is passed. The resulting pulses are stored for half a bit period (normally 488 ns for 2 M bit/s) in the latches. They appear as half-width output pulses at Pins 10 and 11.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5.1\ V \pm 5\%$, unless specified otherwise (see Figure 1).

PARAMETERS	PINS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Current	14		22	30	mA	
Data Output Leakage Current	10,11		0	100	μA	$V_{pull\text{-}up} = 15\ V$, $V_{cc} = 5.35\ V$
ALBO Port Off Voltage	2,3,4		0	0.1	V	
Amplifier Pin Voltage	5,6,7,8	2.4	2.9	3.4	V	
DYNAMIC CHARACTERISTICS AMPLIFIER						
Output Offset Voltage		-50	0	50	mV	$R_S = 8.2\ k\Omega$
AC Gin @ 1 MHz		47	50	53	dB	
Input Impedance		20			kΩ	
Output Impedance				200	Ω	
ALBO						
ALBO Off Impedance		20		25	kΩ	
ALBO On Imepdance				25	Ω	
THRESHOLDS						
ALBO Threshold		1.4	1.5	1.6	V	
Clock Threshold as % of ALBO Threshold		68		80	%	
DATA Threshold as % of ALBO Threshold		42		49	%	
Clock Drive Current		0.7		1.4	mA	At $V_O = V_{ALBO}$ Threshold
OUTPUT STAGES						$R_L = 130\Omega$, $V_{pull\text{-}up} = 5.1 \pm 5\%$
Output Pulse Rise Time				40	ns	
Output Pulse Fall Time				40	ns	
Output Pulse Width		224	244	264	ns	
Output Pulse Width Differential		-10		+10	ns	
Buffer Gate Voltage (Low)		0.65		0.95	V	
Buffer Gate Voltage Differential		-0.15		0.15	V	

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise stated, all characteristics shall apply over the operating temperature range of -40°C to +85°C with V_{CC} = 5.1 V ± 5%, all voltages referred to ground = 0 V.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS (Ref. Figure 2)							
I_S	Supply Current	14		22	30	mA	
I_{LD}	Data Output Leakage Current	10,11			100	µA	from V_S (See Note 1)
	Amplifier Pin Voltages	5,6,7,8	2.4	2.9	3.4	V	
	ALBO Ports Off Voltage	2,3,4		0	0.1	V	

Note 1: V_S = 15V, V_{CC} = 5.35 V

AMPLIFIER (Ref. Figure 2, Only Pins 1, 9, 10...18 Connected)							
	Input Offset Voltage	5 & 6	-10		+10	mV	R_S = 8, 2 kΩ (See Note 1)
	Input Bias Current	5 & 6	0		5	µA	R_S = 8, 2 kΩ (See Note 1)
	Input Offset Current	5 & 6	-1		1		R_S = 8, 2 kΩ (See Note 1)
	Output Offset Voltage	7 & 8	-50	0	-50	mV	R_S = 8, 2 kΩ (See Note 1)
	Common Mode Rejection Ratio	7 & 8	30			dB	Vcm ± 0, 3 V
	Power Supply Rejection Ratio	7 & 8	30			dB	Vcc ± 10
	Output Voltage Swing	7 & 8	2.2			V	

Note 1: R_S = Source Resistance

CLOCK AMPLIFIER (Ref. Figure 2 Disconnect Pin 15 from Pin 16)							
	Input Offset Voltage	15 & 16	0.5		6	mV	R_S = kΩ (See Note 1)
	Input Bias Current	15 & 16			10	µA	T = 25°C
	Max. Output Voltage	13	0.7			V	
	Min. Output Voltage	13	0.7			V	
	Max./Min. Output Voltage Difference	–			50	mV	

Notes:
1. R_S = Source resistance, Pin 15 positive with respect to Pin 16.
2. Pin 15 = Pin 16 = 3.6 V
3. Pin 15 = 2.6 V, Pin 16 = 3.6 V
4. Pin 15 = 4.6 V, Pin 16 = 3.6 V
5. Calculation only

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
ALBO (Ref. Figure 2)							
	On Current	1	3			mA	V_8-V_7 = ±1.75 V
	Drive Current	17	0.4		1.4	mA	V_8-V_7 = ±1.75 V
	Resistance Pin 17 to GN		35	50	70	kΩ	Not Powered

DYNAMIC CHARACTERISTICS

AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain @ 1 mHz	5 to 8	47	50	53		
Z_{in}	Input Impedance	5	20			kΩ	(See Note 1)
Z_{out}	Output Impedance	7, 8			200	Ω	(See Note 2)

Notes: 1. At 2 MHz, AC ground Pins 7 and 8, disconnect 51 Ω resistor. Allow for in-circuit R, C.
2. At 1 MHz, use Figure 2.

CLOCK AMPLIFIER (Ref. Figure 3)							
Ao	AC Gain	15,16 to 13	32			dB	(See Note 1)
BW	-3 dB Bandwidth	15, 16 to 13	10			MHz	(See Note 2)
	Delay	15, 16 to 13	8		12	ns	(See Note 3)
	Output Impedance	13			200	Ω	(See Note 4)

Notes: 1. Remove dc offset, at 2.048 MHz, Pin 13 = 1 V pk-pk sine wave
2. Remove dc offset, Pin 13 = 1 V pk-pk sine wave
3. Remove dc offset, Pin 15 = 2 V pk-pk sine wave. Delay from Pin 15 negative-going zero crossover to Pin 13 positive edge.
4. Remove dc offset, at 2.048 MHz

ALBO (Ref. Figure 2)							
	Off Impedance	2,3,4	20			kΩ	(See Note 1)
	Intermediate Impedance Difference	2,3,4,			5		(See Note 2)
	On Impedance	2,3,4			25	M	(See Note 3)
	Transconductance	7,8 to 1			0.03	dB	(See Note 4)

Notes: 1. At 1 MHz, allow for in-curcuit R,C
2. At 1 MHz, V_8-V_7 adjusted for current at Pin 1 = 100 μA
3. At 1 MHz, V_8-V_7 adjusted for ± 1.75 V
4. At 1 MHz, change in V_8-V_7 for current at Pin 1 = 10 μA to 100 μA

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
THRESHOLD VOLTAGES (Ref. Figure 3)							
	ALBO Threshold +ve	8-7	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold -ve	7-8	1.4	1.5	1.6	V	(See Notes 1 & 2)
	ALBO Threshold Difference	–	-5	0	5		(See Note 3)
	Clock Drive on Current (Peak) +ve	18	0.65	1.0	1.4	mA	(See Note 4)
	Clock Drive on Current (Peak) -ve	18	0.65	1.0	1.3	mA	(See Note 5)
	Clock Drive on Current Difference	–	-5	0	5		(See Note 3)
	Clock Threshold +ve	8-7	68		80		(See Notes 1, 6, 8)
	Clock Threshold -ve	7-8	68		80	%	(See Notes 1, 7, 8)
	Clock Threshold Difference	–	-5	0	5	%	(See Note 3)
	Data Threshold +ve	8-7	44	46	48	%	(See Notes 1, 8, 9, 11)
	Data Threshold -ve	7-8	44	46	48	%	(See Notes 1, 8, 10, 11)
	Data Threshold Difference	–	-3	0	3	%	(See Note 3)

Notes:
1. Pk/pk voltage at Pins 7 and 8 of a 1 MHz sine wave derived through amplifier and measured differentially
2. Pk/pk voltage at Pins 7 and 8 adjusted for current at Pin 1 = 3 mA
3. Calculation only

$$\text{percentage difference calculated from} \left(\frac{\text{higher value}}{\text{lower value}} - 1 \right) \times 100 \quad \%$$

4. V_8-V_7 adjusted to ALBO threshold +ve voltage (ref. Pin 16 = 3.6 V)
5. V_7-V_8 adjusted to ALBO threshold -ve voltage (ref. Pin 16 = 3.6 V)
6. V_8-V_7 adjusted to peak current at Pin 18 = ½ (clock drive on current peak +ve)
7. V_7-V_8 adjusted to peak current at Pin 18 = ½ (clock drive on current peak -ve)
8. Figure taken as a percentage of lower ALBO threshold
9. V_8-V_7 increased until 1 MHz PRF on counter at Pin 10
10. V_7-V_8 increased until 1 MHz PRF on counter at Pin 11
11. With 2.048 MHz 2 V pk-pk sine wave to Pin 15 with 180 μH in parallel with 36 Ω to Pin 16 = 3.6 V

	OUTPUT STAGES (Ref. Figure 3. Use 180 μH inductor between Pins 15 and 16. Apply 2.048 MHz 2V pk/pk to Pin 15.)						
t_r	Output Pulse Rise Time +ve	10			40	ns	10% - 90%
t_r	Output Pulse Rise Time -ve	11			40	nx	10% - 90%
t_f	Output Pulse Fall Time +ve	10			40	ns	10% - 90%
t_f	Output Pulse Fall Time -ve	11			40	ns	10% - 90%
t_W	Output Pulse Width +ve	10	244	244	264	ns	at 50%
t_W	Output Pulse Width -ve	11	244	244	264	ns	at 50%
Yt_W	Output Pulse Width Difference	–	-10		10	ns	
V_{OL}	Buffer Gate Voltage (low) +ve	10	0.65		0.95	V	
V_{OL}	Buffer Gate Voltage (low) -ve	11	0.65		0.95	V	
bV_{OL}	Buffer Gate Voltage Difference	–	-0.15		0.15	V	

Note: 1. Calculation only

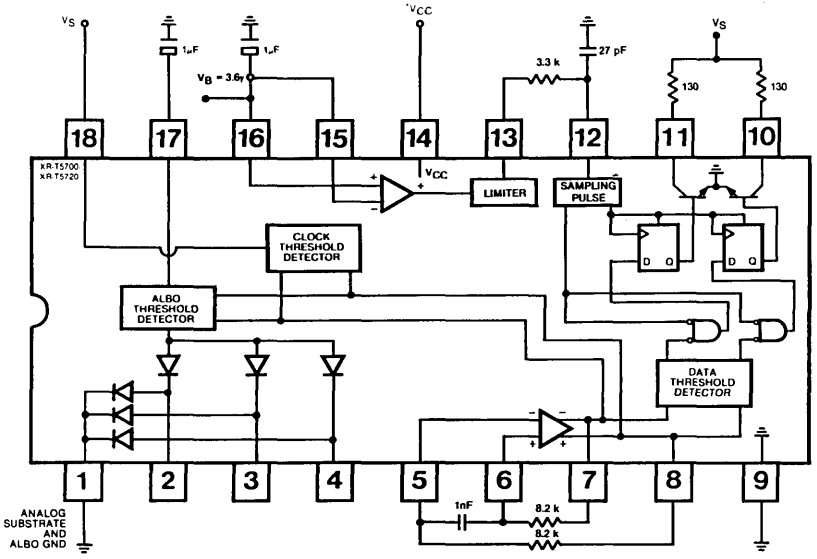


Figure 2. DC Parameter Test Circuit

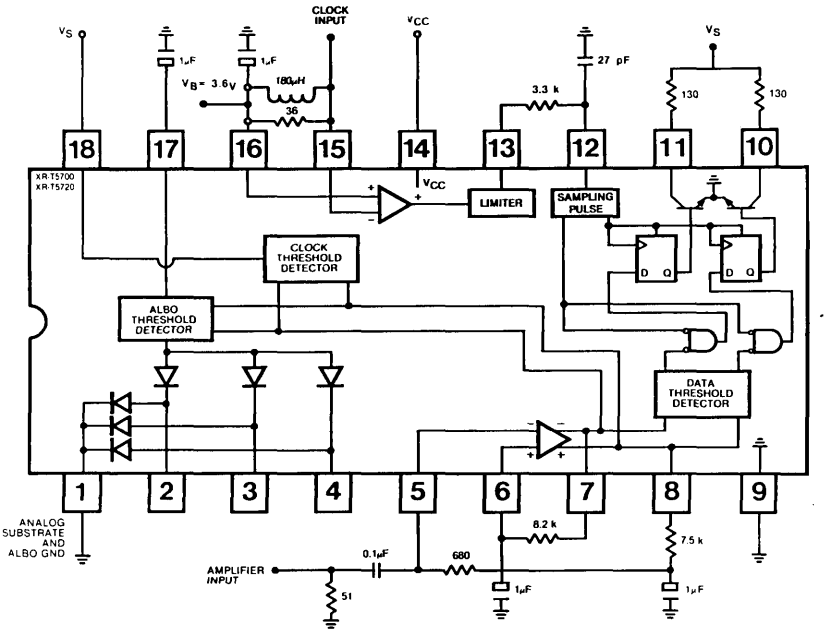


Figure 3. AC Parameter Test Circuit

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
SAMPLE PULSE WIDTH (Ref. Figure 4. Cy = 27 pF)							
	Sample Pulse Width	–		10	20	ns	(See Notes 1...5)

Notes:
1. The sample pulse width is the period during which the output latches are opened to accept a signal above the data threshold at Pin 7 or 8 and cause a hlaf-width output pulse at Pin 11 or 10 respectively.
2. Sample pulse width is specified with a 2,048 MHz TTL waveform at clock input (Pin 15) and a 2,400 MHz Schottky TL waveform at amplifier input in the circuit of Figure 5. Figure 7 shows the relevant IC waveforms.
3. Monitor the frequency of coincident output pulses at Pins 10 and 11 either directly or through output circuit to frequency counter.
4. Sample pulse width = Xns + (0,1 x measured frequency in kHz ns where x is the mean rise/fall times of the waveform at Pin 8 between 25% and 75%.
5. X to be within the range 10 ns < X < 12 ns. This requires HF layout techniques with the amplifier operated closed loop.

SAMPLE PULSE GENERATOR INPUT WAVEFORM (Pin 12 Ref. Figure 4, Cy = 40 pF)							
	Output Pulse Frequency	10,11	1,024 -100 ppm	1,024	1,024 +100 ppm	MHz	(See Note 1)

Note: 1. Width 2,048 MHz ± 100 ppm TTL waveform at clock input with half of above waveform frequence at amplifier input.

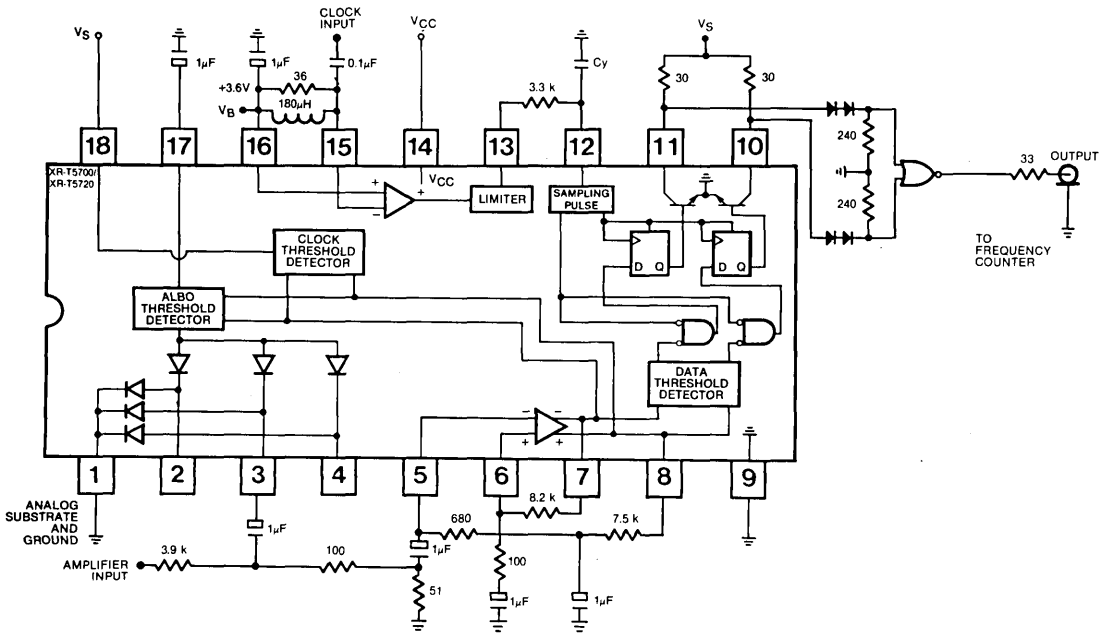


Figure 4. Sampling Pulse Test Circuit

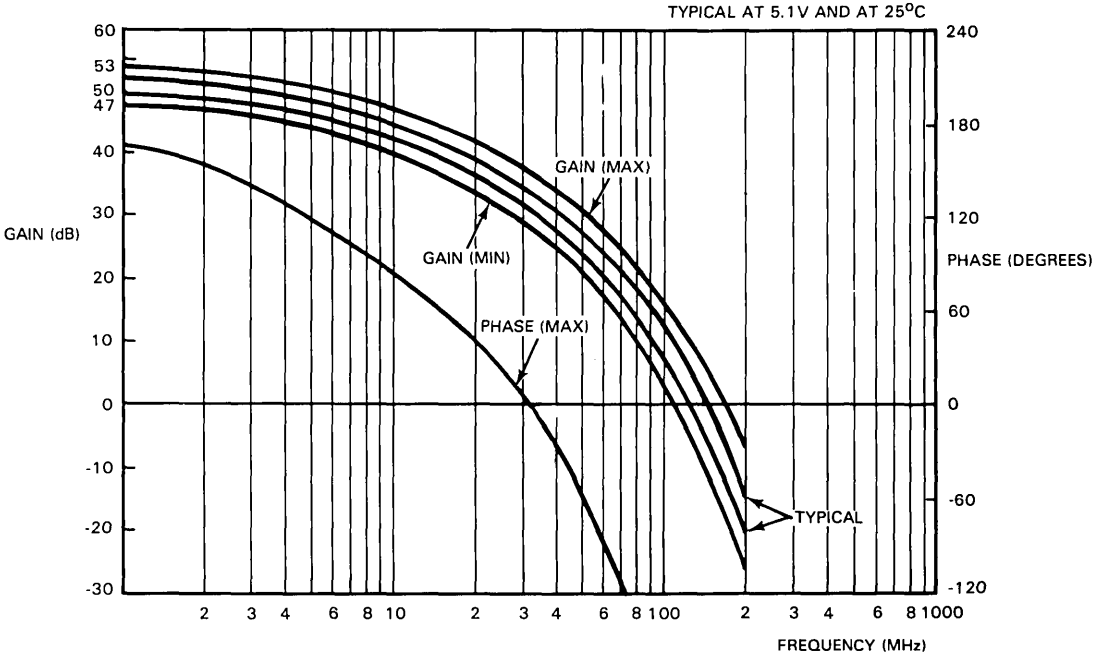


Figure 5. Typical and Limiting Values of Gain and Phase

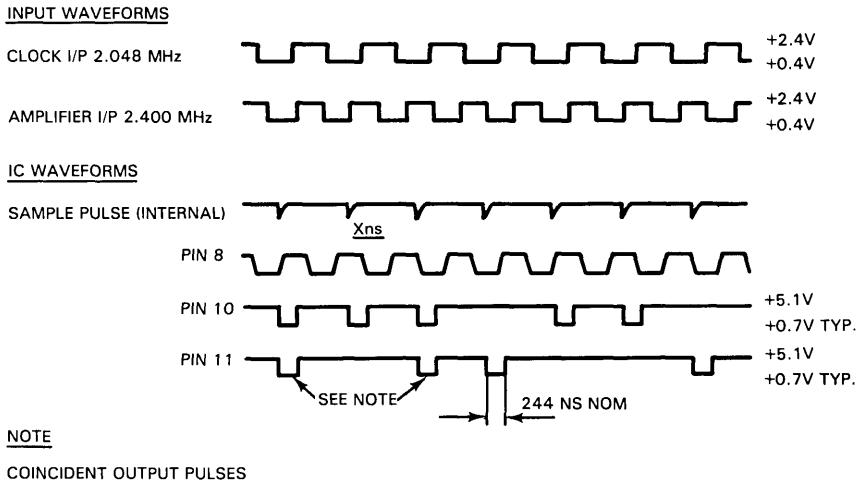
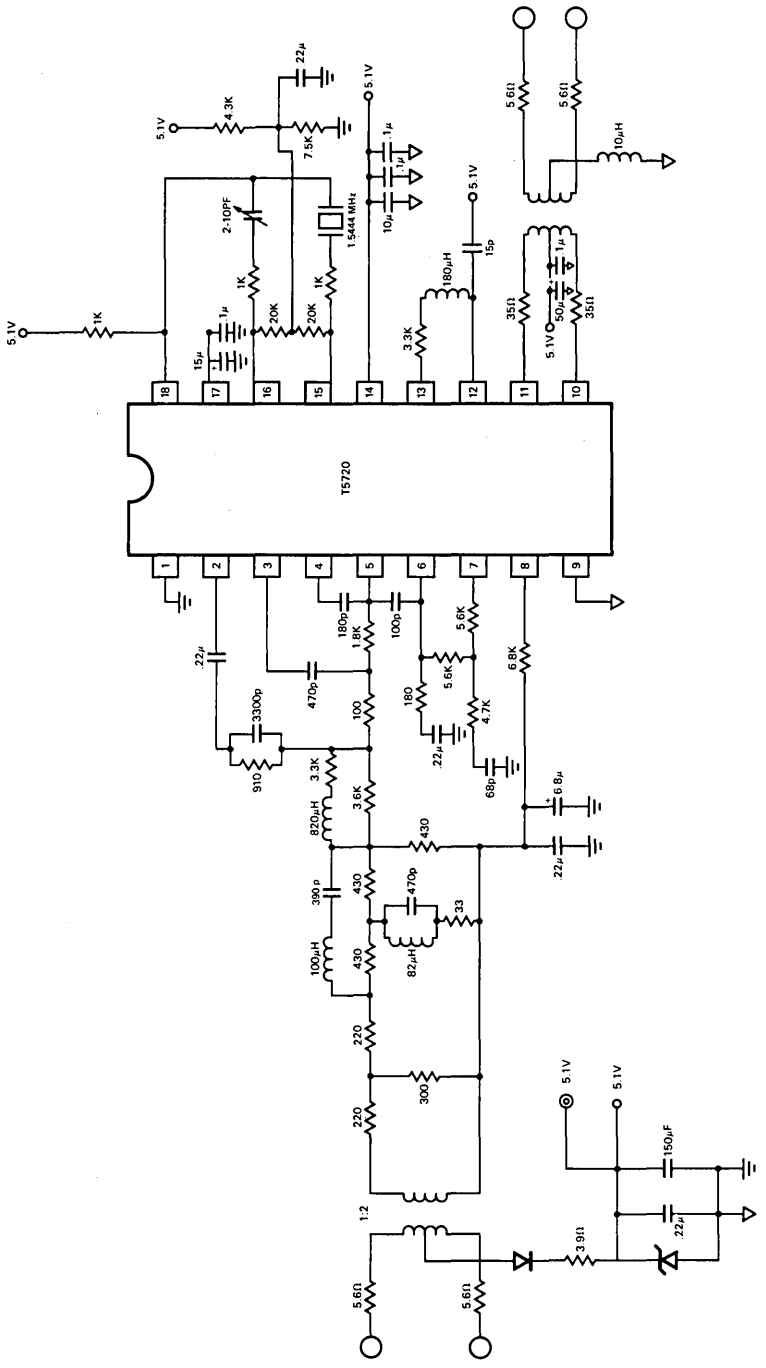


Figure 6. IC Waveforms for Measuring Sampling Pulse Width



T5720 1.544 MBITS/S HIGH Q PCM REPEATER APPLICATION CIRCUIT

Section 2 – Telecommunication Products

Speakerphone Audio Circuit

GENERAL DESCRIPTION

The XR-T6420-1 is a monolithic integrated circuit for use in high performance speakerphone systems. It is designed to be used with the XR-T6421 Speakerphone Control Circuit.

The XR-T6420-1 contains the audio paths comprising the following: Two variable gain cells, a microphone amplifier, a transmitting amplifier, a receive amplifier, and a speaker amplifier.

FEATURES

Two Matched Variable Gain Cells
Internal Microphone Amplifier
Independent Control of Transmitting and Receiving Levels
External Control of Gains and Frequency Response

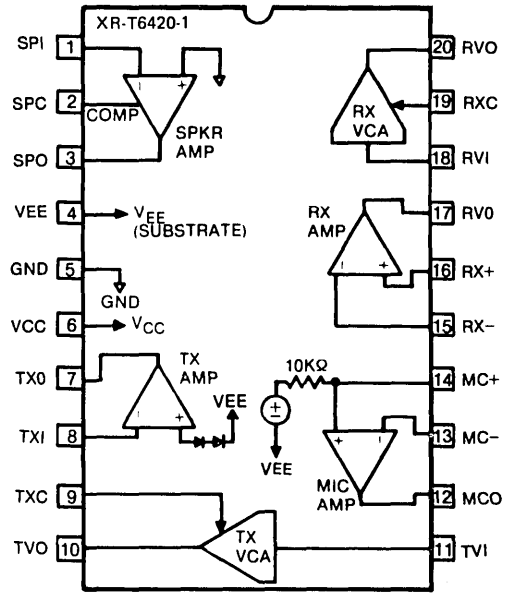
APPLICATIONS

Speakerphones
Intercoms
Voltage Controlled Amplifiers

ABSOLUTE MAXIMUM RATINGS/

Power Supply ($V_{CC} - V_{EE}$)	+20 V
Power Dissipation	1 W
Derate Above +25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Any Input Voltage	V_{CC} – 0.5 V to V_{EE} + 0.5 V
Storage Temperature	-55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6420-1CN	Ceramic	0°C to 70°C
XR-T6420-1CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The speakerphone concept essentially requires that only one direcction of sound transmission be permitted at any time. This restraint is brought about by the large gains required to provide loudspeaker volume and high microphone sensitivity. Owing to the inevitable acoustic coupling between loudspeaker and microphone, plus imperfections in the hybrid 2 to 4 wire conversion, it is necessary to lower the gain in either the transmitting or receiving path at any one time to avoid regeneration.

The XR-T6420-1 and XR-T6421 chip set enables the system designer to make a highly adaptive, high performance speakerphone. The XR-T6421 provides for all sensing and control functions, while the XR-T6420-1 contains all audio paths needed to switch the gain in either path and provide interfacing between the system and line.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V, unless specified otherwise.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{CC} Minimum	+4.5			V	
V_{EE} Minimum	-6			V	
I_{CC}	15	22	30	mA	
I_{GND}	-1	−.1	1	mA	
MICROPHONE AMPLIFIER					
V_{IN}	1.7	2	2.25	V	Referenced to V_{EE}
V_{OFFSET}		2	5	mV	
I_{bias}		1	5	μA	
A_{OL}	40	50		dB	
R_{IN}		10		kΩ	Typical Input Impedance to GND
SPEAKER AMPLIFIER					
V_{OFFSET}		4	10	mV	
I_{bias}		-3	-10	μA	
A_{OL}	60	70		dB	
Swing	−4.9		4.8		
TRANSMIT AMPLIFIER					
Vpin 8	.8	1.3	1.5	V	Referenced to V_{EE}
I_{source} (Pin 7)	1			mA	
I_{sink} (Pin 7)	−1			mA	
RECEIVE AMPLIFIER					
Differential Mode Gain	−4	-1	0	dB	
Common Mode Gain		-30	−28	dB	
V_{OUT} (Pin 17)		-2.7		V	
TRANSMIT VCA					
V_{OUT} (Pin 10)	−2.1	-1.9	−1.5	V_{DC}	
Gain Maximum	6	8	13	dB	
V_{OUT} Maximum		1		Vp-p	
RECEIVE VCA					
V_{OUT} (Pin 20)	1.2	1.5	1.7	V_{DC}	
Gain Maximum	2	4	7	dB	
V_{OUT} Maximum		1		Vp-p	

PRINCIPLES OF OPERATION

Power Supply – Normal operation is with two supplies. V_{CC} is the highest potential and V_{EE} is the lowest, with the ground pin in between. The circuit can be operated from a single supply if the ground pin is connected to a low impedance source of approximately half the supply voltage.

Microphone Amplifier – The microphone amplifier is an operational amplifier with the noninverting input internally biased to approximately V_{EE} + 2 Volts. The noninverting input impedance is nominally 10.3 Kohms. Gain and frequency response can be set by external components using the noninverting configuration for the op amp. The amplifier has an emitter follower output, therefore, needs an external pull down resistor to V_{EE}. This resistor is selected low in value in order to prevent slewing of the output waveform due to capacitance.

Transmit VCA – This VCA provides a voltage dependent gain, given in Figure 2. The input, referred to V_{EE}, has a nominal impedance of 14.8 Kohms. The output is also referred to V_{EE} and is buffered by an emitter follower.

Transmit Amplifier – This amplifier is a Darlington Common Emitter Amplifier with a Class A output stage. Pin 8 is approximately 1.1 Volt above V_{EE}. Gain is set by the input and feedback resistor. To increase the output swing, the output DC level is determined using a resistor from Pin 8 to V_{EE}.

Receive Amplifier – This amplifier has a high impedance differential input and a fixed gain of one. The inputs must be referred to a voltage greater than V_{EE} + 1.5 V. The output is at a fixed DC level with a Class A output stage.

Receive VCA – This VCA provides a voltage dependent gain, given in Figure 3. The input is referenced to V_{EE} and has a nominal impedance of 14Kohms. The output is referred to ground and is buffered by an emitter follower.

Speaker Amplifier – This is an operational amplifier with the noninverting input referred to ground through a 1.8 Kohm resistor. The gain is externally set using the input and feedback resistor. The amplifier can be compensated by a capacitor from the output to Pin 2 or from Pin 2 to ground. The output is capable of sourcing or sinking 4 mA.

CIRCUIT DESCRIPTION

Pin 1 - SPI – Inverting input to speaker amplifier.

Pin 2 - SPC – Speaker amplifier compensation

Pin 3 - SPO – Speaker amplifier output.

Pin 4 - V_{EE} – Negative DC supply pin (usually -5 to -10 V).

Pin 5 - GND – Ground pin reference for circuit. Can be used with ($V_{CC} - V_{EE}$)/2 external reference.

Pin 6 - V_{CC} – Positive DC supply voltage, usually +5 to +10 V.

Pin 7 - T_{XO} – Output of transmit amplifier.

Pin 8 - T_{XI} – Input of transmit amplifier.

Pin 9 - T_{XC} – Control voltage of transmit VCA. Transfer function of VCA is:

$$\frac{T_{VO}}{T_{VI}} = 2\,(1 + \exp\,(T_{XD} - Vpin\ 5/VT))^{-1}$$

where $V_T = \frac{KT}{q} \cong 26$ mV at +25°C

Pin 10 - T_{VO} – Output of transmit VCA. Output is an emitter follower.

Pin 11 - T_{VI} – Input of transmit VCA. Input impedance is nominally 14.9 Kohms.

Pin 12 - MCO – Output of microphone amplifier.

Pin 13 - MC- – Inverting input of microphone amplifier.

Pin 14 - MC+ – Noninverting input of microphone amplifier. Input impedance is nominally 10.3 K ohms.

Pin 15 - R_{X-} – Inverting input to receive amplifier. Input is high impedance.

Pin 16 - R_{X+} – Noninverting input to receive amplifier. Input is high impedance.

Pin 17 - R_{XO} – Output of receive amplifier. Output DC level is nominally 0 volts.

Pin 18 - R_{VI} – Input to receive VCA. Input impedance is nominally 14 K ohms.

Pin 19 - R_{XC} – Control voltage of receive VCA. Transfer function of VCA is:

$$\frac{R_{VO}}{R_{VI}} = (1 + \exp\,((\ Vpin\ 5 - R_{XC})/VT))^{-1}$$

where $V_T = \frac{KT}{q} \cong 26$ mV at 25°C

Pin 20 - R_{VO} – Output of receive VCA. Output is an emitter follower.

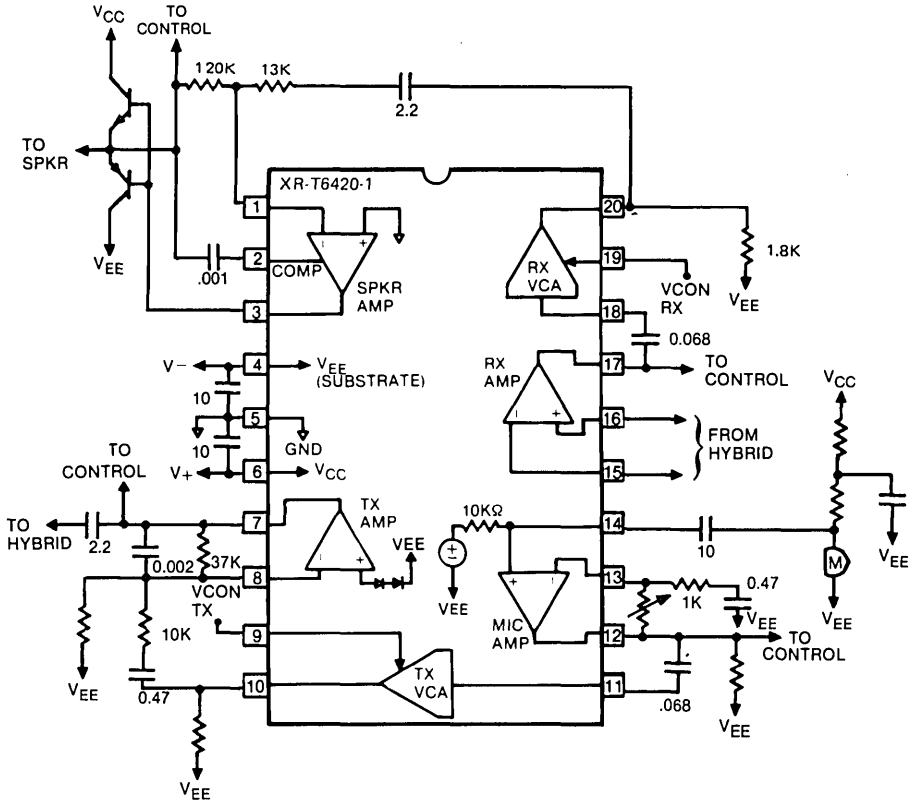


Figure 1. Typical Application Schematic

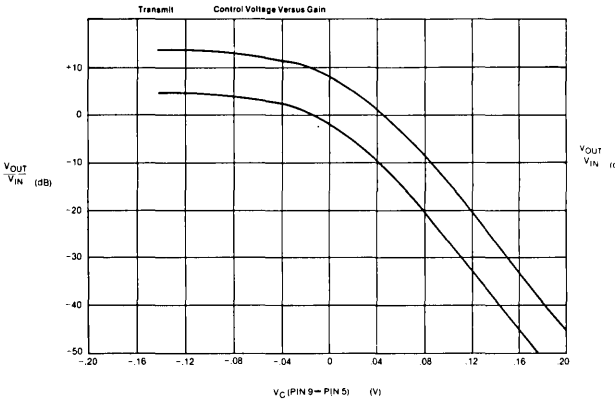


Figure 2. Transmit Control Voltage vs. Gain

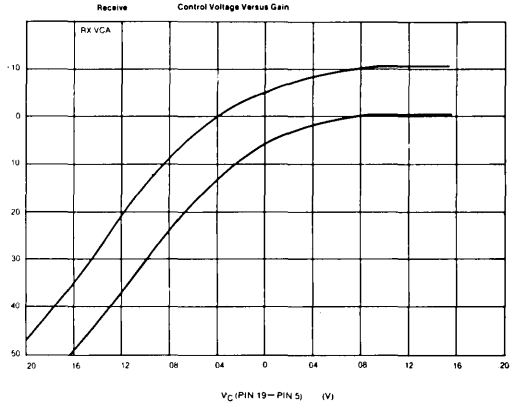


Figure 3. Receive Control Voltage vs. Gain

Speakerphone Audio Circuit

GENERAL DESCRIPTION

The XR-T6420-2 is a monolithic integrated circuit for use in high performance speakerphone systems. It is designed to be used with the XR-T6421 Speakerphone Control Circuit.

The XR-T6420-2 contains the audio paths comprising the following: Two variable gain cells, a microphone amplifier, a transmitting amplifier, a receive amplifier, and a speaker amplifier. Mute and enable control logic of the variable gains cells is provided internally.

FEATURES

Two Matched Variable Gain Cells
Internal Microphone Amplifier
Independent Control of Transmitting and Receiving Levels
External Control of Gains and Frequency Response
Enable and Mute Logic Pins

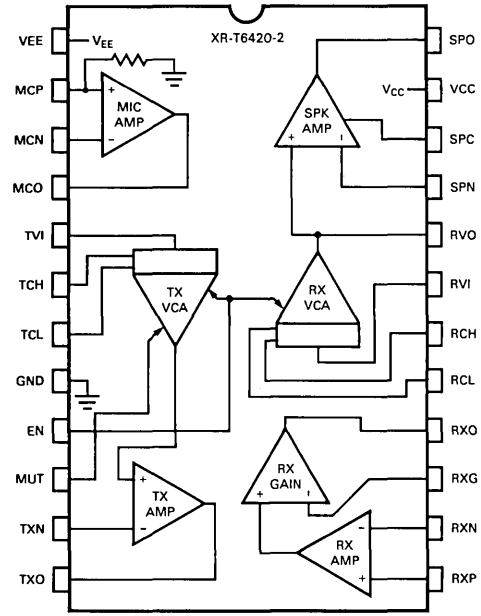
APPLICATIONS

Speakerphones
Intercoms
Voltage Controlled Amplifiers

ABSOLUTE MAXIMUM RATINGS

Power Supply ($V_{CC} - V_{EE}$)	+30 V
Power Dissipation	1 W
Derate Above +25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Any Input Voltage	V_{CC} – 0.5 V to V_{EE} + 0.5 V
Storage Temperature	-55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6420-2CN	Ceramic	0°C to 70°C
XR-T6420-2CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The speakerphone concept essentially requires that only one direction of sound transmission be permitted at any time. This restraint is brought about by the large gains required to provide loudspeaker volume and high microphone sensitivity. Owing to the inevitable acoustic coupling between loudspeaker and microphone, plus imperfections in the hybrid 2 to 4 wire conversion, it is necessary to lower the gain in either the transmitting or receiving path at any one time to avoid regeneration.

The XR-T6420-2 and XR-T6421 chip set enables the system designer to make a highly adaptive, high performance speakerphone. The XR-T6421 provides for all sensing and control functions, while the XR-T6420-2 contains all audio paths needed to switch the gain in either path and provide interfacing between the system and line.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = +5$ V, $V_{EE} = -5$ V, unless specified otherwise.

PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	3			V	
V_{EE}	3			V	
I_{CC}		4.9	8	mA	Pin 23
MICROPHONE AMPLIFIER					
V_{IN}		5	25	mV	Pin 2
R_{IN}		20		kΩ	Pin 2
V_{OFFSET}			5	mV	
I_{BIAS}		−.2	−0.5	μA	
Open Loop Gain	80			dB	
SPEAKER AMPLIFIER					
R_{IN}		10		kΩ	Pin 20
V_{OFFSET}			5	mV	
I_{BIAS}		−.2	-0.5	μA	
Open Loop Gain	80			dB	
I_{SOURCE}, I_{SINK}	100			mA	$R_{LOAD} = 10Ω$
V_{OUT} High	V_{CC} −1.6			V	$R_{LOAD} = 5kΩ$
V_{OUT} Low	V_{EE} +.8			V	$R_{LOAD} = 5kΩ$
TRANSMIT AMPLIFIER					
I_{BIAS}		−.2	−0.5	μA	
Open Loop Gain		90		dB	
RECEIVE AMPLIFIER					
I_{BIAS}		1.2	2	μA	Pin 13, Pin 14
Differential Mode Gain	−3	−1		dB	Pins 15 and 16 Shorted
Common Mode Gain	−40	−60		dB	Pins 15 and 16 Shorted
I_{BIAS}		−.2	−.5	μA	Pin 15
Open Loop Gain		90		dB	
VCAs TRANSMIT AND RECEIVE					
V_{OUT} DC			.3	V	Pins 11 and 20
Maximum Gain	−2		+2	dB	f = 1kHz, Pins 5 and 19
I_{BIAS} Control			.5	μA	Pins 6, 7, 17 and 18
MUTE AND ENABLE LOGIC					
I_{SOURCE}		−10	−20	μA	
Trip Voltage		V_{CC} −2.8	V_{CC} −2.1	V	

PRINCIPLES OF OPERATION

Power Supply

Normal operation is with two supplies. V_{CC} is the highest potential and V_{EE} is the lowest. The circuit can be operated from a single supply if the ground pin is connected to a low impedance source of approximately one half the supply voltage.

Microphone Amplifier

The microphone amplifier is an operational amplifier with the positive input internally connected to the ground pin through a 20 K ohm nominal resistance. Gain and frequency responses are set using external components.

Transmit Voltage Controlled Amplifier (T_X VCA)

The output of the microphone amplifier is normally capacitively coupled into the T_X VCA. The input impedance is nominally 10 K ohm. The gain of the T_X VCA is dependent upon the voltage difference between the TCH and TCL inputs on pins 6 and 7. The output is internally connected to the transmit amplifier.

Transmit Amplifier

This is an operational amplifier with a class AB output stage. Gain and frequency response are set with external components. This amplifier is used to drive the hybrid interface network.

Receive Amplifier

The input on pins 13 and 14 is a high input impedance differencing amplifier. The output is internally referenced to the ground pin and connected to the positive input of an operational amplifier. The gain and frequency response of the amplifier can be adjusted using external components on pins 15 and 16. This amplifier is normally connected to the hybrid interface network to detect the receive signal while rejecting the transmit signal.

Receive Voltage Controlled Attenuator (R_X VCA)

The output of the receive amplifier is capacitively coupled to the R_X VCA input on pin 19. The R_X VCA's input impedance is a nominal 10 Kl ohm. The gain of the R_X VCA is dependent upon the voltage difference between the RCH and RCL inputs on pins 17 and 18. The output of the R_X VCA is internally referenced to the ground pin through a 10 Kl ohm resistance and connected to the positive input of the speaker amplifier on pin 20.

Speaker Amplifier

This is an operational amplifier with a class AB power output stage. Gain and frequency response are set using external components. Depending on the load driven, compensation may be necessary using pin 22.

PIN DESCRIPTIONS

Pin 1 - V_{EE} – Negative DC supply.

Pin 2 - MCP – Microphone amplifier noninverting input. Internally connected to ground with a 20 K ohm resistance.

Pin 3 - MCN – Microphone amplifier inverting input.

Pin 4 - MCO – Microphone amplifier output.

Pin 5 - TVI – Transmit voltage controlled amplifier input. Input impedance is 10 K ohm.

Pin 6 - TCH – Transmit VCA gain control pin; high reference. Used with pin 7 to control VCA gain according to Figure 1.

Pin 7 - TCL – Transmit VCA gain control pin; low reference. Used with pin 6 to control VCA gain.

Pin 8 - GND –Ground reference pin for circuit.

Pin 9 - ENABLE – Active high; internally pulled high. When pulled low, causes an internal 200 mV difference between the gain control pins for both VCAs effectively causing minimum gain in both.

Pin 10 - MUTE – Internally pulled high. When pulled low, causes only the transmit VCA to be minimum gain.

Pin 11 - T_XN – Transmit amplifier inverting input.

Pin 12 - T_XO – Transmit amplifier output.

Pin 13 - R_XP – Receive amplifier positive input. High input impedance, must be DC referenced externally.

Pin 14 - R_XN – Receive amplifier negative input. Must be DC referenced to same source as pin 13.

Pin 15 - R_XG – Receive amplifier inverting input.

Pin 16 - R_XO – Receive amplifier op amp output.

Pin 17 - RCL – Receive VCA gain control pin low reference used with pin 18 to control VCA gain according to Figure 1.

Pin 18 - RCH – Receive VCA gain control pin; high reference used with pin 17 to control gain of VCA.

Pin 19 - RVI – Receive VCA input. Input impedance is 10 K ohm.

Pin 20 - RVO – Receive VCA output. Impedance is 10 K ohm to ground.

Pin 21 - SPN – Speaker amplifier inverting input.

Pin 22 - SPC – Speaker amplifier compensation.

Pin 23 - V_{CC} – Positive DC supply.

Pin 24 - SPO – Speaker amplifier output.

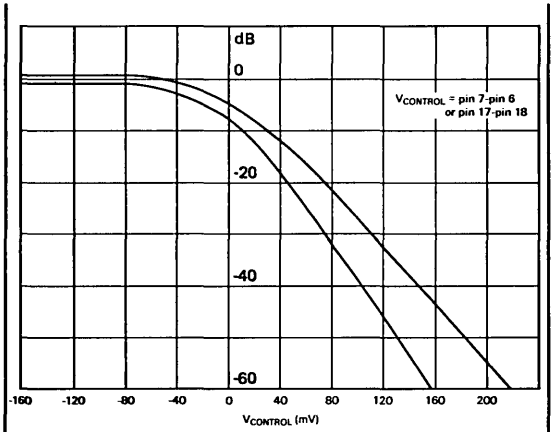


Figure 1. VCA Gain Characteristics

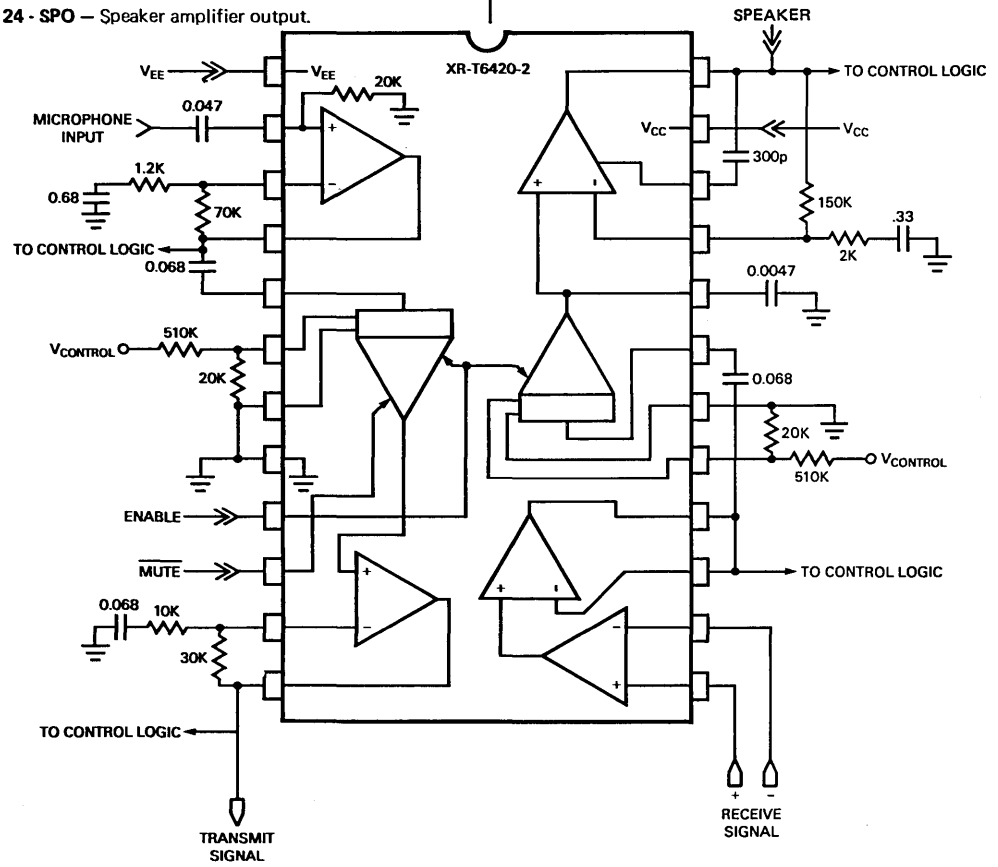


Figure 2. Typical Application Schematic

Speakerphone Control IC

GENERAL DESCRIPTION

The XR-T6421 is a monolithic integrated circuit for use in high performance speakerphone systems. It is designed to provide all control functions for the XR-T6420-1 or XR-T 6420-2 speakerphone audio circuit.

The XR-T6421 contains the level sensors and logic necessary to change the attenuation in the transmitting or receiving path in order to avoid acoustic feedback.

Circuitry is included to detect bacground noise level and provide a preset amount of attenuation in each path when no voice is present.

FEATURES

Low Current
Background Noise Detection and Suppression
External Control of Attach and Decay Time Constants
Independent Control of Gain and Frequency Response
Provides Three Level Control of Transmit & Receive Paths

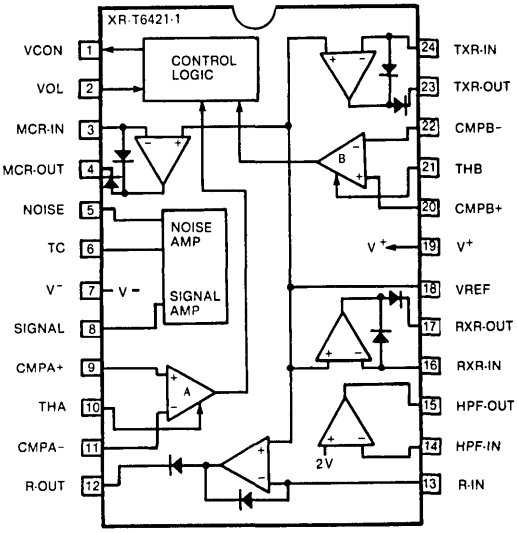
APPLICATIONS

Speakerphones
Intercoms
Voice Operated Switches

ABSOLUTE MAXIMUM RATINGS

Power Supply	20 V
Power Dissipation	1 W
Derate Above +25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Any Input Voltage	V_{CC} +0.5 V to V_{EE} -0.5 V
Storage Temperature	-55 °C to 150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6421CN	Ceramic	0°C to 70°C
XR-T6421CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The speakerphone concept essentially requires that only one direction of sound transmission be permitted at any time. This restraint is brought about by the large gains required to provide loudspeaker volume and high microphone sensitivity. Owing to the inevitable acoustic coupling between loudspeaker and microphone, plus imperfections in the hybrid 2 to 4 wire conversion, it is necessary to lower the gain in either the transmitting or receiving path at any one time to avoid regeneration.

The XR-T6420-1 and XR-T6421 chip set enables the system designer to make a highly adaptive, high performance speakerphone. The XR-T6421 provides for all sensing and control functions, while the XR-T6420-1 contains all audio paths needed to switch the gain in either path and provide interfacing between the system and line.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 10V$, unless specified otherwise.

PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage Range	5		20	V	
Supply Current		1.4	3	mA	$V_{CC} = 10$ V
V_{REF}	1.85	2.1	2.25	V	
RECTIFIERS					
V_{OUT}	1.9	2.1	2.27	V	VAC = 0
V_{OUT} (High Level)		5.0		V	
V_{OFFSET} 1	-5		5	mV	Vpin 4 - Vpin 12
V_{OFFSET} 2	-5		5	mV	Vpin 17 - Vpin 23
A_{OL}	45			dB	
I_{bias}		0.2		µA	
HPF					
V_{OUT} DC	2.3	2.6	2.9	V	
Maximum Isource (Pin 15)		1.0		mA	
Maximum Isink (Pin 15)		1.0		mA	
A_{OL}	32			dB	
I_{bias}		0.25		µA	
VOICE CIRCUITRY					
Noise Amplifier Offset V6 - V5	-3		12	mV	V_{IN} =
Signal Offset V8 - V18			15	mV	V_{IN} =
Signal Gain	.8	1	1.2		$\frac{\text{Vpin 8 - Vpin 18}}{\text{Vpin 5 - Vpin 6}}$
CONTROL OUTPUT					
V_{CON} High	V_{CC}-.9		V_{CC}-.5	V	
V_{CON} Idle	4.9	5	5.1	V	20 kΩ to 5 V
V_{CON} Low Minimum			95	V	
V_{CON},V_{OL} Offset	50		250	mV	
COMPARATORS					
I_{bias}		1		µA	
Offset	5		17	mV	$V_{POS} - V_{NEG}$

PRINCIPLES OF OPERATION

Rectifiers – All four rectifiers are operational amplifiers with the noninverting input connected to V_{REF}. The circuit contains the diodes internally to provide the function of a negative peak detector. Using the typical application schematic of Figure 1, the "gain" of the rectifier is R2/R1. The output is then filtered using another RC network. The attack time is given by R3.C and the decay time by (R2 + R3).C.

High Pass Filter – This is a simple gain stage with a class AB output stage. Pin 14 is about 2.6 V above V^-. This amplifier is normally used as a high pass filter to reduce line induced hum from the detection circuitry.

Noise Control Circuitry – This function provides a signal on Pin 8 related to the difference between Pins 5 and 6. Pin 5 is usually connected to the filter network of the microphone rectifier. This signal represents the speech plus noise from the microphone. Pin 6 has an external RC network and functions as a detector for the noise level. The output on Pin 8 is the difference between Pins 5 and 6, referenced to V_{REF}.

Comparators – Both comparators have internally generated offset of -10mVolts nominally. With no difference between the inputs, the output will be in the low state. The amount of offset can be increased by connecting a resistor between the threshold adjust pin and V^-.

Control Logic – The purpose of the logic is to derive the three speakerphone states, depending on Comparators A and B. The three states are:

1) Transmit → Pin 1 = V^+ -0.7V
2) Receive → Pin 1 ≅ Pin 2 + 0.1V
3) Idle → Pin 1 is High Impedance.

The truth table for the logic is:

Comparator		State
A	B	
0	0	Idle
0	1	Receive
1	0	Transmit
1	1	Idle

CIRCUIT DESCRIPTION

Pin 1 - V_{CON} – Provides three voltage states depending on input conditions. The first is a low impedance voltage about equal to V^+ -.7 Volt. The second state is a low impedance voltage equal to voltage on Pin 2. The third state is a high impedance state.

Pin 2 - V_{OL} – A high impedance input used to modify the control voltage (Pin 1) when in the low state.

Pin 3, 4 - MCR – Negative peak detector usually connected to microphone amplifier output. Gain, attack, and delay times are externally set.

Pin 5 - NOISE – High impedance input used to buffer speech plus noise input from microphone rectifier.

Pin 6 - TC – External RC network determines response to background noise level. RC network determines rise time, internal circuitry will discharge network if Pin 6 > Pin 5.

Pin 8 - SIGNAL – Provides voltage proportional to Pin 5, Pin 6 output impedance is nominally 36 K ohms.

Pin 9, 11 - CMP A – Used to compare signal level to level of speaker signal.

Pin 10 - TH A – Used to increase offset of comparator A. With TH A open, offset is approximately -10 mV.

Pin 12, 13 - R – Negative peak detector normally connected to speaker amplifier. Gain, attack, and decay times are externally set.

Pin 14, 15 - HPF – Inverting amplifier, normally connected as a high pass filter to reject low frequencies from received signals into the control circuitry.

Pin 16, 17 - R_XR – Negative peak detector normally connected after line receive amplifier. Gain, attack, and decay times are externally set.

Pin 18 - V_{REF} – Internal 2 Volt reference.

Pin 20, 22 - CMP B – Used to compare transmitted and received signal levels.

Pin 21 - TH B – Used to increase offset of comparator B with TH B open, offset is approximately -10 mV.

Pin 23, 24 - T_XR – Negative peak detector normally connected to transmit amplifier. Gain, attack, and decay times are externally set.

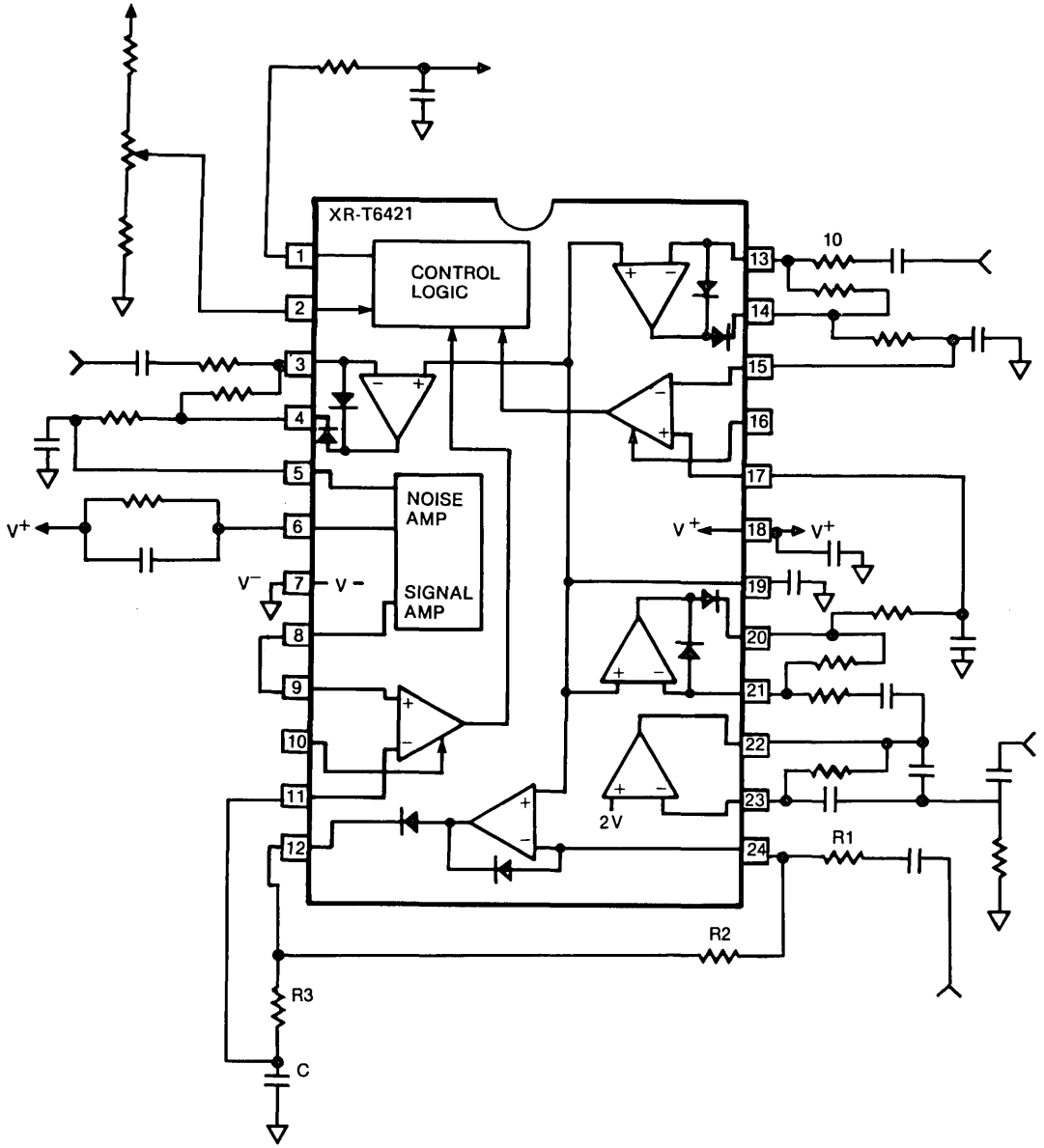


Figure 1. Typical Application Schematic

Speakerphone IC

GENERAL DESCRIPTION

The XR-T6425 speakerphone IC is a low cost solution for the implementation of a hands-free telephone. It is a convenient way of carrying on conversation without using the handset, while the user is talking into a microphone and listening from a loudspeaker located on the desk. It is ideal for hands-free conference calls.

The XR-T6425 contains most of the circuits to eliminate singing and excessive background noise in a single chip solution.

FEATURES

Low Operating Voltage (4.5 V)
Single Chip Speakerphone
No External Adjustments
Smooth T/R Switching
Background Noise Detection and Suppression
On-chip Hybrid Circuit

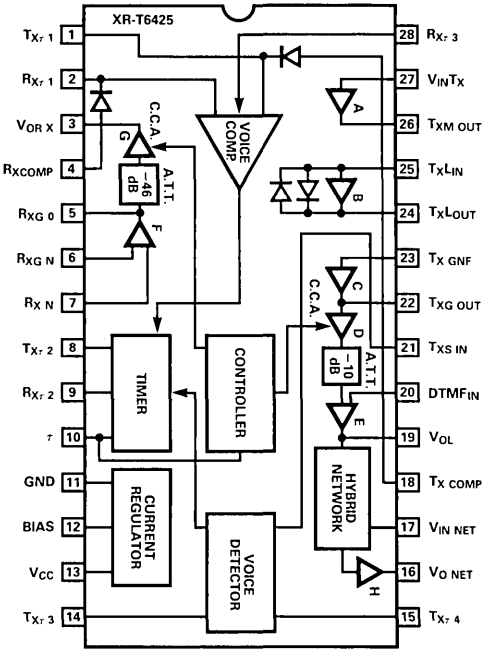
APPLICATIONS

Speakerphones
Intercoms
Voice Operated Switches

ABSOLUTE MAXIMUM RATINGS

Power Supply	16 V
Power Dissipation	700 mW
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T6425CN	Ceramic	0°C to 70°C
XR-T6425CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T6425 single chip speakerphone IC is designed to operate from the phone line and allows hands-free operation. The chip contains most of the necessary circuits to reduce external component count and performs half-duplex operation. The internal circuits consist of a transmitter, receiver and control logic. DTMF input is provided for Touch Tone operation. An adjustable threshold circuit is provided to separate voice from ambient noise.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = 5$ V, f = 1 kHz, unless otherwise specified.

SYMBOL	PARAMETERS	TYPICAL VALUE	UNIT	CONDITIONS
V_{CC}	Operating Voltage	4.5 - 6.5	V	
I_C	Operating Current	8.0	mA	No Input of T/R Signal
R_{XS}	Receiving Sensibility	–64	dBm	
T_{XS}	Transmitting Sensibility	–74	dBm	
G_{VRX}	Receiving Gain	–22.5	dB	Receiving Mode
G_{VTX}	Transmitting Gain	44	dB	Transmitting Mode
V_{INLIM}	Mic Input Level	–55	dBm	THD = 1%
Att_{RX}	Receving Loss	–50	dB	Receiving Transmitting Relative Value
Att_{TX}	Transmitting Loss	–50	dB	Transmitting Receiving Relative Value

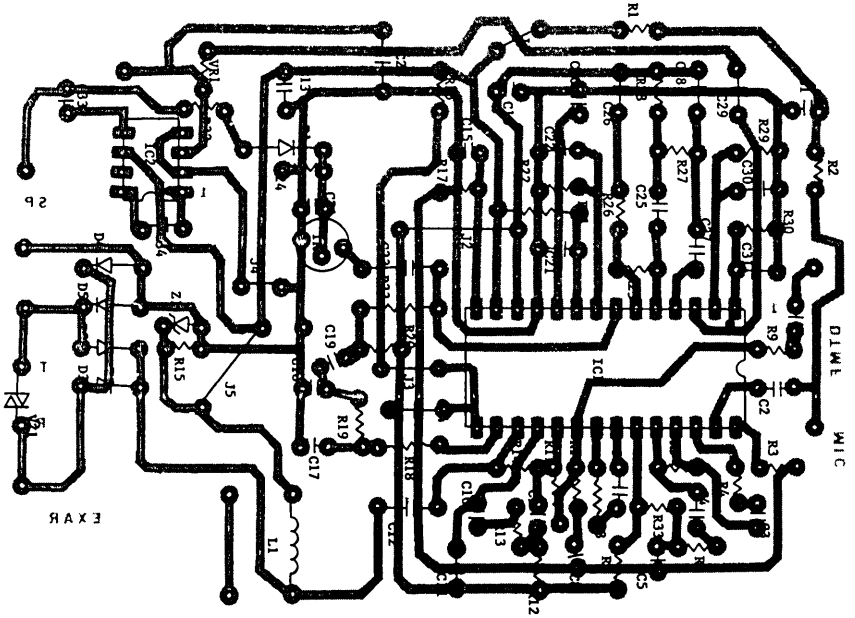


Figure 1. Circuit Board Layout

PIN DESCRIPTIONS

Pin	Symbol	Description
1	$TX_{\tau 1}$	Transmitter stabilization time constant.
2	$RX_{\tau 1}$	Receiver stabilization time constant.
3	$V_O RX$	Receiver output.
4	R_X COMP	T/R comparator input for receiver.
5	$R_X G_O$	Receive buffer output.
6,7	R_{XGN},R_{XIN}	Receive buffer inputs.
8	$TX_{\tau 2}$	Transmitter holding time constant.
9	$RX_{\tau 2}$	Receiver holding time constant.
10	τ	T/R switching time constant
11	GND	Ground
12	BIAS	Mid-point of the supply voltage ($V_{CC}/2$).
13	V_{CC}	Most positive voltage.
14	$TX_{\tau 3}$	Voice rectifier time constant.
15	$TX_{\tau 4}$	Ambient noise and voice discriminator time constant.
16	V_{ONE}	Hybrid network output.
17	V_{IN} NET	Hybrid network input.
18	T_X COMP	T/R comparator input for transmitter.
19	V_{OL}	Transmit signal output.
20	DTMFIN	DTMF input terminal.
21	T_{XS} IN	Voice detector output.
22	T_{XG} OUT	Transmit amplifier output.
23	TXG NF	Transmit amplifier input.
24	$T_X L_{OUT}$	Transmit limiter amplifier output.
25	$T_X L_{IN}$	Transmit limiter amplifier input.
26	$T_X M_{OUT}$	Transmit buffer output.
27	$V_{IN} T_X$	Transmit buffer input.
28	$RX_{\tau 3}$	Receiver stabilizer.

FUNCTION DESCRIPTIONS

Transmitting Sections

The transmit path is divided into five sections: buffer, limiter, bandpass filter and amplifier, current control attenuator and mixer.

Buffer

The buffer is used to do impedance matching and gives 9 dB gain to signal.

Limiter

The output of the buffer is fed to limiting amplifier to increase the signal level. The gain can be set with two external resistors R_4, R_5 to obtain proper signal level.

Bandpass Filter and Amplifier

Filtering is performed in this section to eliminate unwanted signals. Gain of 20 dB is set for this section and output of this amplfier is capacitor coupled to control lgoic to eliminate DC components for decision making.

Current Control Attenuator

The current control attenuator is used to do smooth switching between transmitter and receiver to perform half-duplex operation.

Mixer

Additional input is provided for DIMF signaling and driving transmitting signals to telephone line through impedance matched resistance R_{14} (680Ω), and simultaneously inputs to the hybrid network for cancelling signals to receiving circuit.

Receiving Section

Incoming signals are amplified by AMP H and AMP F after passing through hybrid network. The result is fed to current control attenuator to control output level.

Ambient Noise and Voice Discrimination Section

This section discriminates voice signals from ambient noises of input signals from microphone at transmtting mode and gives the instruction signals to keep transmitting mode or changes the mode to T/R signal attenuator circuit through timer circuit.

Controller Section

This section compares transmit signal level (pin 18) with receive signal level (pin 4) according to the time settled by C_{31}, R_{30}, C_{30}, R_{29}, the result is applied to the timer circuit which is triggered with the resistor value of R_3 connected from Pin 28 to Ground.

Timer Section

This section generates the signals to T/R signal attenuator circuit and provides the time constant for T/R switching.

Transmit time constant is set by pin 8, receive time constant is set by pin 9, and T/R switching time constant is determined by pin 10. Pin 10 outputs 2.5V at transmit mode and +1.2V at receive mode.

Hybrid Network

Hybrid network is used to attenuate transmit signal going to the receive path. Equivalent circuit is shown below.

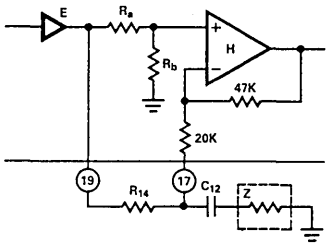


Figure 2. Equivalent Circuit

TIMING CALCULATIONS

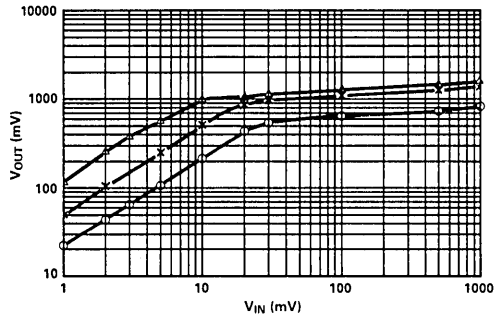
Transmit Rise Time = $C_{22} \times 10^4$	4.7 μF, τ = 47 ms
Transmit Hold Time = $C_{22} \times R_{22}$	4.7 μF, 470K, τ = 2.2S
Receive Rise Time = $C_{21} \times 10^3$	.47 μF, τ = .47 ms
Receive Hold Time = $C_{21} \times R_{21}$	.47 μF, 470K, τ = .22S

DESCRIPTION OF AMPLIFIERS

Type	Application	Gain	Remarks
A	TX amplifier	0 dB	For the impedance conversion (emitter-follower microphone) (Zin = 20 kΩ)
B	TX amplifier	R5/R 4	Negative input limiter amplifier, clamping at $\frac{1\ VF}{\sqrt{2}}$ of Pin 24 output. (V0 = 700 mVrms)
C	TX amplifier	20 dB	Fixed gain amplifier.
D	TX amplfier	TX: 20 dB ST: −5 dB RX: −23 dB	Gain varies with transmitting (TX), receiving (RX) and standby (ST).
E	TX amplifier	R11/R10	Output gain - the signal applied as a negative input when DTMF is used.
F	RX amplifier	R25/R26	Differential input amplifier. Its output is connected to C.C.A. (amp G) through pin 5 and ATT.
G	RX amplifier	TX: −23 dB ST: −5 dB RX: 20 dB	Gain varies with transmitting (TX), receiving (RX) and standby (ST).
H	RX amplifier	7.5 dB	For the network loss correction of receving (RX) side.

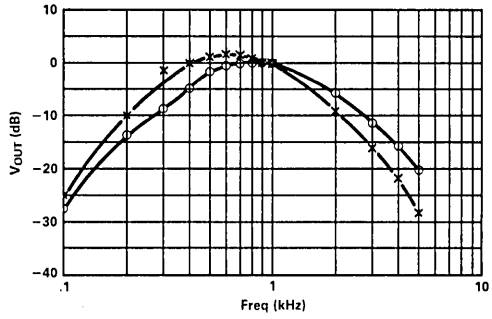
TYPICAL CHARACTERISTICS

XR-T6425 RECEIVING ALC CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



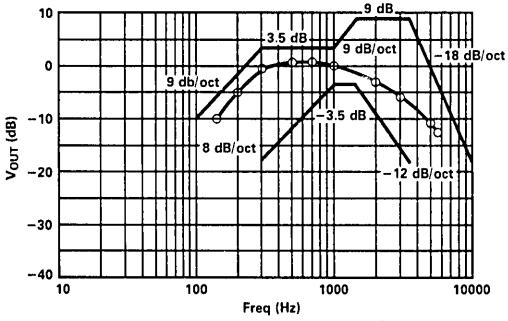
△ C × B ○ A

XR-T6425 RECEIVING FREQUENCY CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



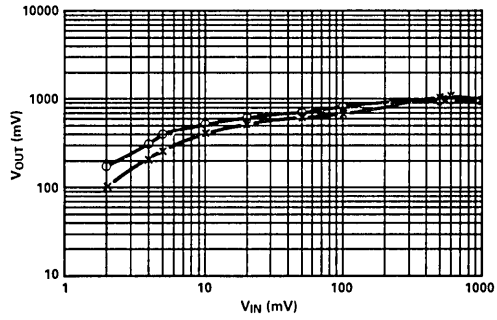
× BEFORE MOUNTING C32 ○ AFTER MOUNTING C32

XR-T6425 TRANSMITTING FREQUENCY CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



❋ INDICATION VALUES OF M3

XR-T6425 MICROPHONE AMPLIFIER LIMITER CHARACTERISTICS
V_{CC} = 5.6V, APPLYING 12V BETWEEN L1 AND L2



× INDICATION VALUES OF M2 ○ INDICATION VALUES OF M3

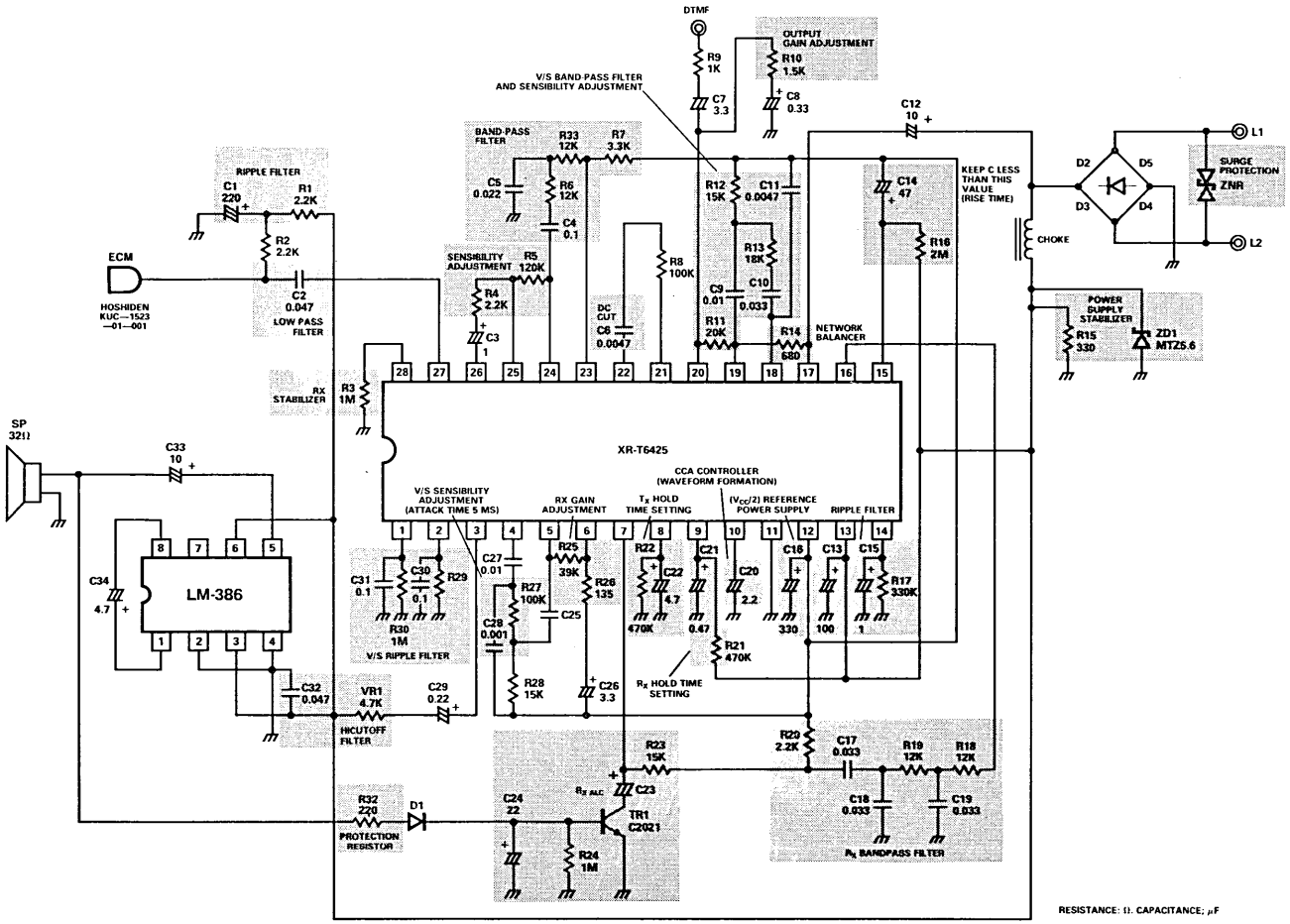


Figure 3. Typical Line Powered Application Circuit

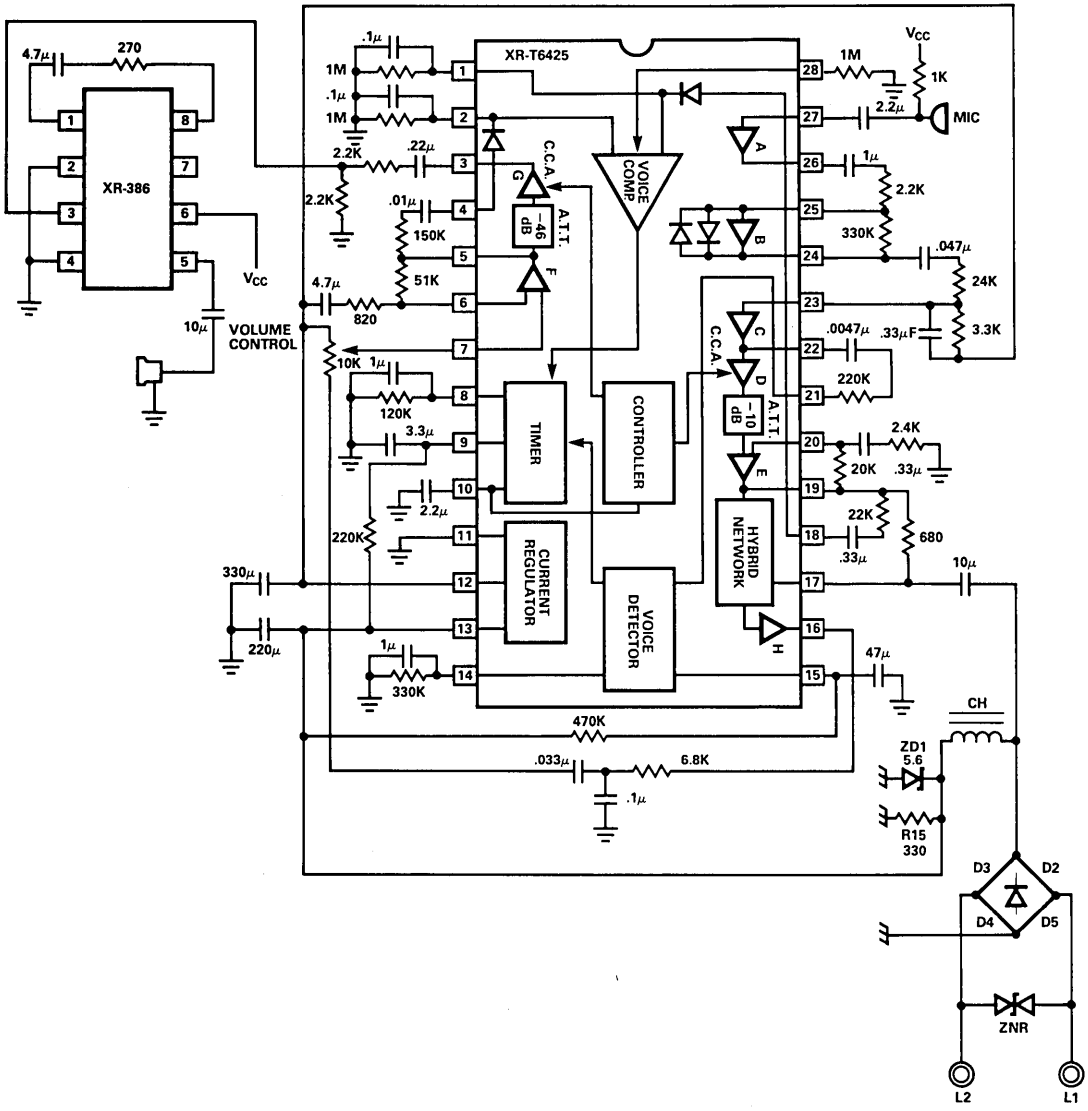


Figure 4. Simplified Application Schematic

Section 2 – Telecommunication Products

Single Chip Pulse/Tone Dialer

GENERAL DESCRIPTION

The XR-T5990 Single Chip Pulse/Tone Dialer is a silicon gate CMOS technology circuit which performs both pulse and tone functions.

It is designed to operate directly from the telephone line or on a separate small power supply. A 17 digit buffer is provided for redial feature.

FEATURES

Pin Selectable Pulse/Tone Dialing
Low Standby Current
17 Digit Redial Buffer
Uses TV Crystal Standard 3.58 MHz or Ceramic Resonator to Provide High Accuracy and Stability
3.5 Second Pause Timer
Regulated Tone Amplitude
Pin Selectable Dialing Rate (10 pps/20 pps)
Pin Selectable Break Ratio (63%/66%)
Interface Directly to a Standard Telephone Push Button or Calculator Type X-Y Keyboard
Generates 12 Standard Tone Pairs
Single Tone and Dual Tone Capability

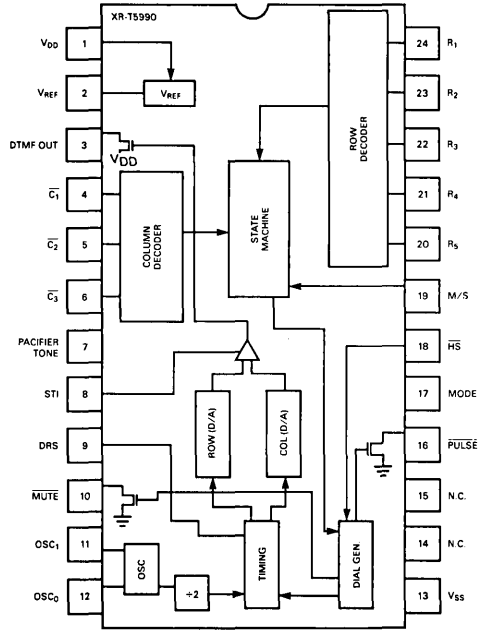
APPLICATIONS

Electronic Telephones
Smart Auto Dialers (modems)
Electronic Banking
Security Controller
Radio Communications

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{DD}	6 V
Operating Temperature	0°C to 70°C
Input Voltage	$-.3 \leq V_{IN} \leq V_{DD} +.3$
Maximum Power Dissipation	500 mW

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5990CP	Plastic	0°C to 70°C
XR-T5990CN	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T5990 Pulse/Tone Dialer is a CMOS integrated circuit that can provide recall of previously entered numbers as well as perform the normal dialing function. Dialing is interchangeable from pulse to tone or vice versa, capable of inserting 3.5 second pause between digits for PABX dialing.

The XR-T5990 dialer is capable of dialing * and # functions in tone mode and ignore in pulse mode. Selectable dialing rate is provided for rapid dialing.

ELECTRICAL CHARACTERISTICS

Test Conditions:

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS 0 °C ≤ T ≤ 70 °C, V_{DD} = 3.5 V						
V_{DD}	DC Operating Voltage	2.5		6	V	
V_{REF}	Magnitude of (V_{DD}-V_{REF})	1.5	2.5	3.5	V	
V_M	Memory Retention Voltage	1.5			V	
I_{OP}	DC Operating Current			4.2	mA	V_{DD} = 3.5 V, Outputs Unloaded
I_S	DC Standby Current			1.5 500	µA nA	V_{DD} = 3.5 V, Outputs Unloaded V_{DD} = 2.5 V, Outputs Unloaded
I_{ML}	Mute Sink Current			10	mA	V_{DD} = 3.5 V, V_{OUT} = .5 V
I_P	Pulse Sink Current			20	mA	V_{DD} = 3.5 V, V_{OUT} = .5 V
K_L	Keyboard "0" Logic Level	V_{SS}		20% of V_{DD}	V	
K_H	Keyboard "1" Logic Level	80% of V_{DD}		V_{DD}	V	
K_{PU}	Keyboard Pull-up Resistance		100		KΩ	
K_{PD}	Keyboard Pull-down Resistance		4		KΩ	
H_{SRU}	Hookswitch Pull-up Resistance		100		KΩ	
Cf_{osc}	Oscillator Stability			.05	%	V_{DD} 2.5 to 3.5 V
S_F	Keyboard Scanning Frequency		932		Hz	
dB_{CR}	Ration of Column to Row Tone		2	3	dB	
%DIS	Distortion		6	7	%	
V_{OR}	Single Tone Row Frequency Amplitude		212		mVRms	R_L = 330Ω
V_{OC}	Single Tone Column Frequency Amplitude		311		mVRms	R_L = 330Ω
T_{DB}	Keyboard Debound Time	11.8			ms	
K_T	Keydown	40			ms	
R_T	Tone Load Resistor	120		400	Ω	

PIN AND FUNCTION DESCRIPTIONS

Pin	Number

Supplies V_{DD}, V_{SS} 1,13

Power Supply Inputs – The device is designated to operate from 2.5 to 6 volts.

V_{REF} 2

The V_{REF} output provides a negative reference voltage relative to V_{DD}, which defines minimum operating voltage. In a typical application, this pin is simply tied to V_{SS}.

Keyboard Inputs

C_1, C_2, C_3 4,5,6
R_1, R_2, R_3, R_4, R_5 24,23,22,21,20

These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row to column input must go to V_{SS} or connect with each other.

Oscillator

OSC_{IN}, OSC_{OUT} 11,12

These pins are provided to connect external crystal or ceramic resonator. The device contains the necessary parasitic capacitances and feedback resistor on chip so that is is only necessary to connect a standard 3.58 MHz TV crystal.

Dialing Rate 9

DRS

Dialing Rate is programmable by connecting this pin to V_{DD} or V_{SS}. The rate is 20 pps when connected to V_{DD} and 10 pps when connected to V_{SS}.

Mark/Space 19

M/S

Mark/Space ratio may be selected by connecting the pin to V_{DD} or V_{SS}.

M/S Pin (19)	MARK	SPACE
V_{SS}	37%	63%
V_{DD}	34%	66%

$\overline{\text{Mute}}$ 10

This N-channel open drain output is designed to drive external bipolar transistor to mute the receiver during dialing.

$\overline{\text{Dial Pulse Out}}$ 16

An output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space", and "high" otherwise.

Mode Select 17

State of this pin selects the proper dialing mode. Tone dialing is selected by connecting this pin to V_{SS}.

Hookswitch 18

$\overline{\text{HS}}$

This input detects the state of the hookswitch contact. The XR-T5990 will accept key inputs when this pin is at low state (off hook).

Single Tone Inhibit 8

$\overline{\text{STI}}$

Single tone output can be inhibited when this pin is connected to V_{SS}.

Tone Out 3

This N-channel open drain output is designed to drive external transistor.

Pacifier Tone Output 7

PT

The XR-T5990 provides a pacifier tone output to provide audio feedback to the user that a key has been depressed. The output is a 1800 Hz tone that can be capacitvely coupled into the telephone receiver.

This option is provided in dial pulse mode only.

FUNCTIONAL DESCRIPTION

Keyboard

The XR-T5990 employs a scanning technique to determine a key closure. This permits interface to DPCT keyboard with common connected to V_{SS} or SPST switch matrix connecting row to column.

A logic interface is also possible as shown in Figure 1.

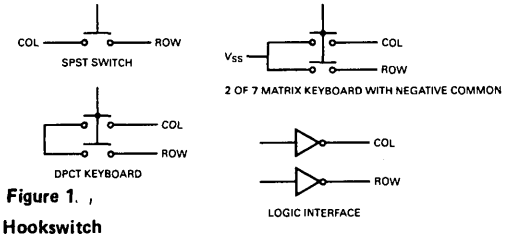


Figure 1. ,

Hookswitch

The XR-T5990 will enter in off hook mode when hookswitch is pulled low. This state enables the device to accept a valid key and enable the oscillator.

Mute Output

The mute output turns on (pulls to the V_{SS} supply) at the beginning of the mark, and turns off (goes to an open circuit) following the last interdigit pause. A small delay is provided to overlap mute output from the end of the last interdigit pause.

Redial

The last number dialed is retained in the memory, and therefore can be redialed out by going off hook and pressing the redial key.

Dialing will start when the key is depressed and finish after the entire number is dialed out unless an access pause is detected. If this is the case, the dialing will stop, and resume again after 3.5 seconds. During redial mode, tone will be on for 70 ms and off for 70 ms.

Normal Dialing

Normal dialing can start after going off hook, since the device is designed in a FIFO arrangement, digitas can be entered at a rate considerably faster than the output rate. Digits can be entered approximately once every 65 ms. Pauses may be entered when required in the dial sequences by pressing pause key which provides access pause for future redial.

During normal tone dialing, tone will go out at 70 ms burst. Continuance single tone can be generated by depressing two digit keys in the appropriate row or appropriate column.

CIRCUIT DESCRIPTION

The XR-T5990 is capable of generating 12 standard tones in the tone mode. Low group frequencies consist of 697, 770, 852, 941 Hz and the high group consists of three frequencies 1209, 1336, and 1477 Hz

A keyboard arranged in a row, column format is used for number entry. When a push button corresponding to a digit is pushed, one appropriate row frequency, and one appropriate column frequency are selected. The appropriate row and column frequencies in the keyboard arrangement are shown below.

Active Input	Specified Frequency
R_1	697
R_2	770
R_3	852
R_4	941
C_1	1209
C_2	1336
C_3	1477

Table 1.

C_1	C_2	C_3	
1	2	3	R_1
4	5	6	R_2
7	8	9	R_3
*	0	#	R_4

Table 2.

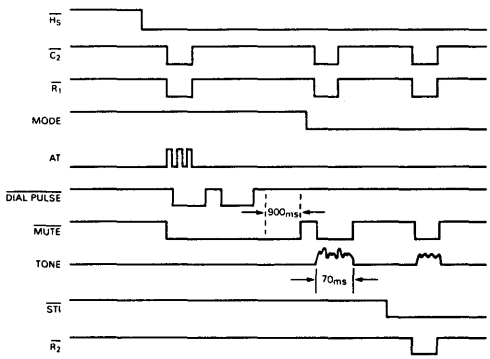


Figure 2. XR-T5990 Timing Diagram

OPERATING DESCRIPTION

Normal Dialing	Tone or Dial Pulse Output
Off Hook, D1 , D2 , ... DN	D1 D2 D3 . . . . . DN
Normal Dialing using Pause Function	
Off Hook, D1 PA D2 . . . . . DN	D1 D2 D3 . . . . . DN
Redial	
On Hook, Off Hook, RD	D1 D2 D3 . . . . . DN
Dialing will halt for 3.5 seconds when a pause is detected.	D1 3.5 sec D2 . . . . . DN
Redial and Normal Dialing Combination	
On Hook, Off Hook, RD , D18 , D19 , D20 . DN	D1 . . . D17 D18 . . . . . DN

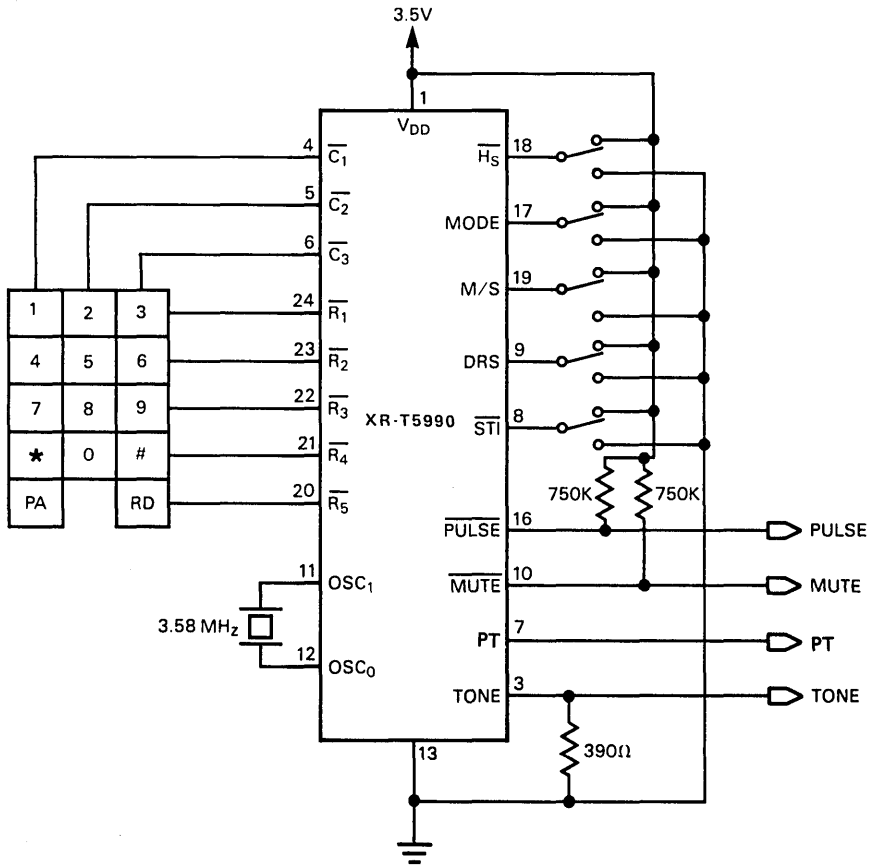


Figure 3. XR-T5990 Test Circuit

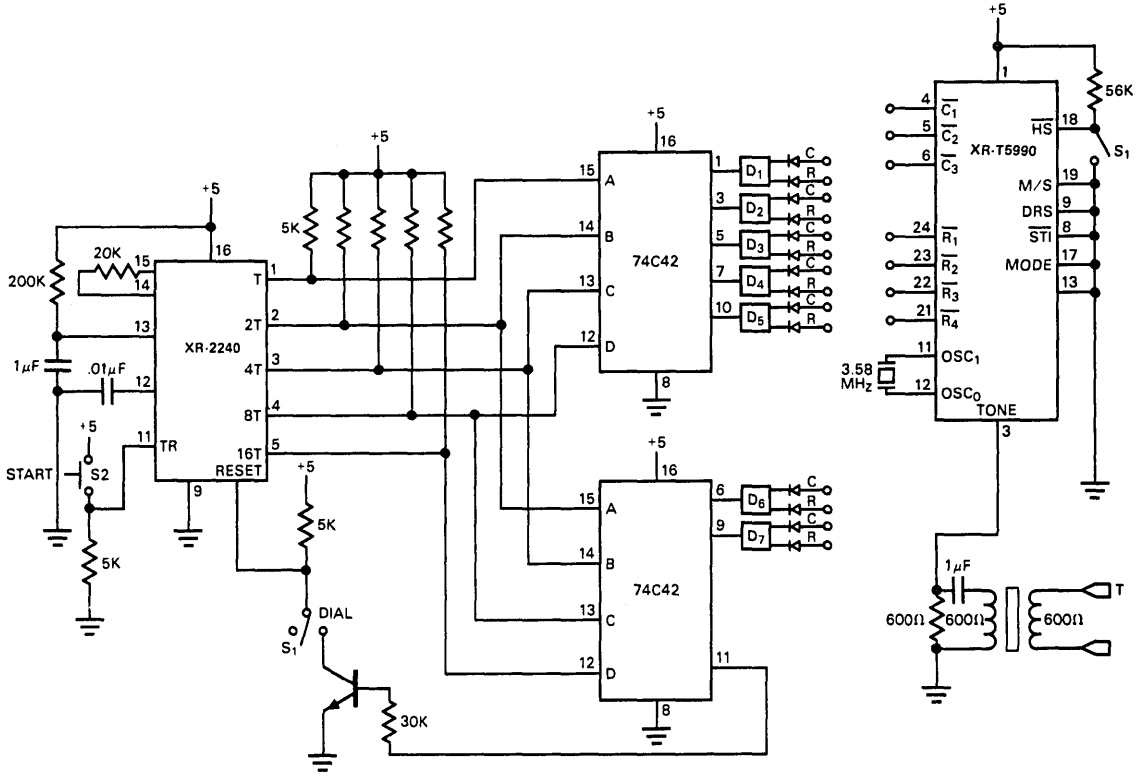
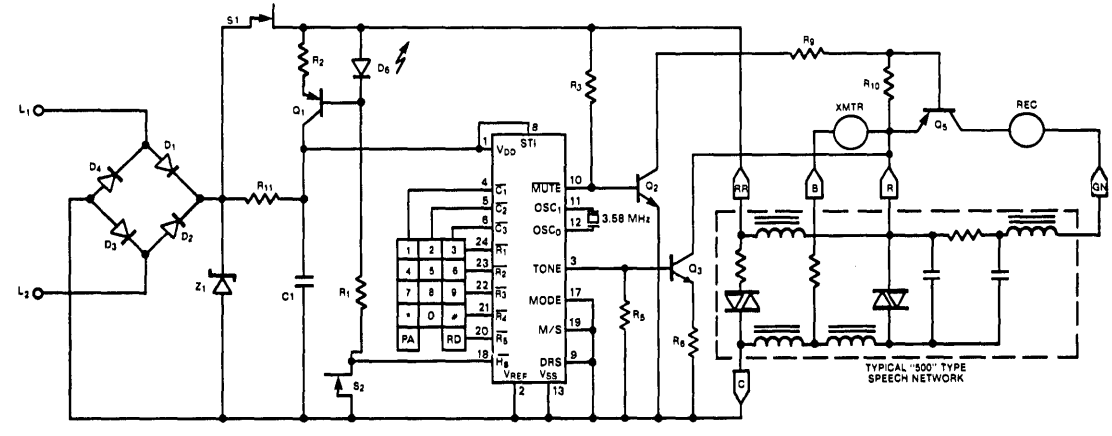
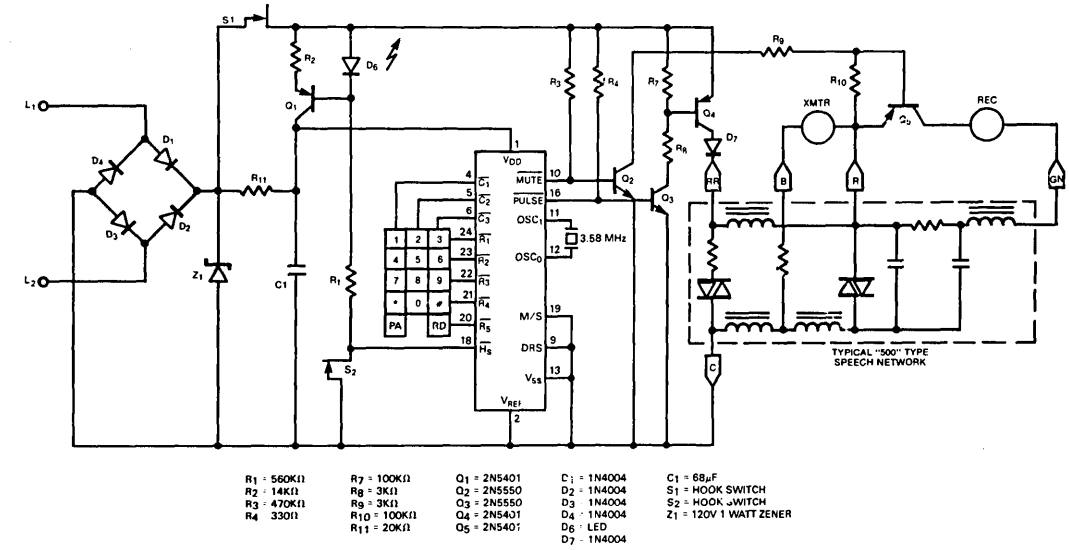


Figure 4. Typical Application Circuit for Auto Dialer Modem



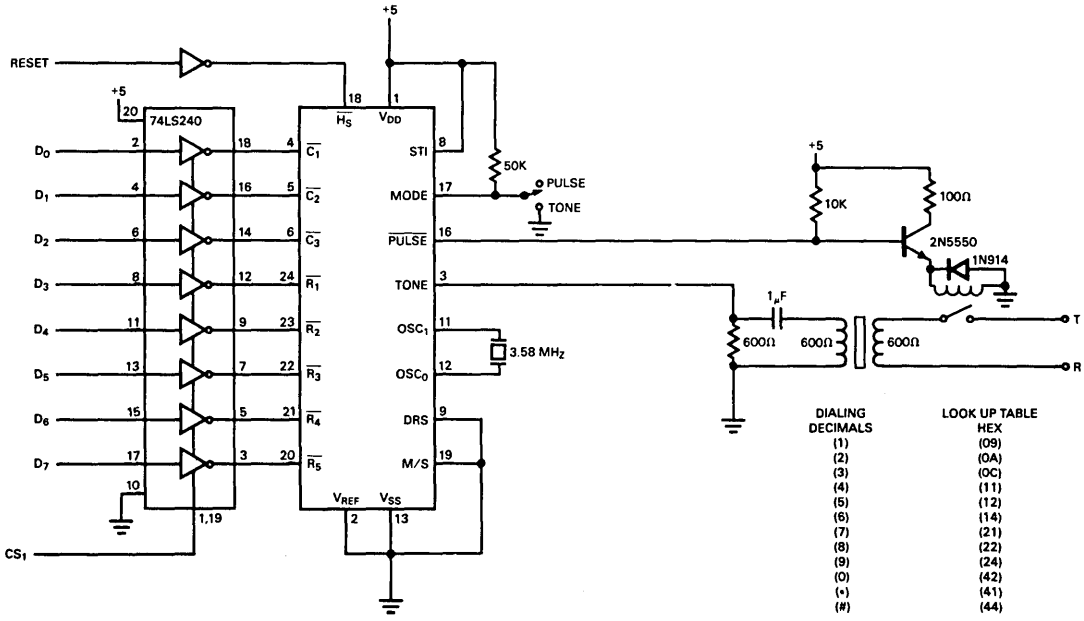
R1 = 560KΩ
R2 = 14KΩ
R3 = 470KΩ
R5 = 330Ω
R6 = 120KΩ
R9 = 3KΩ
R10 = 100KΩ
R11 = 20KΩ
Q1 = 2N5401
Q2 = 2N5550
Q3 = 2N5550
Q5 = 2N5401
D1 1N4004
D2 - 1N4004
D3 - 1N4004
D4 - 1N4004
D6 - LED
C1 68μF
S1 - HOOK SWITCH
S2 HOOK SWITCH
Z1 120V 1 WATT ZENER

Figure 5. Typical Tone Dialing Application Circuit



R1 = 560KΩ
R2 = 14KΩ
R3 = 470KΩ
R4 = 330Ω
R7 = 100KΩ
R8 = 3KΩ
R9 = 3KΩ
R10 = 100KΩ
R11 = 20KΩ
Q1 = 2N5401
Q2 = 2N5550
Q3 = 2N5550
Q4 = 2N5401
Q5 = 2N5401
C1 = 1N4004
D2 = 1N4004
D3 = 1N4004
D4 = 1N4004
D6 = LED
D7 = 1N4004
C1 = 68μF
S1 = HOOK SWITCH
S2 = HOOK SWITCH
Z1 = 120V 1 WATT ZENER

Figure 6. Typical Pulse Dialing Application Circuit



DIALING DECIMALS	LOOK UP TABLE HEX
(1)	(09)
(2)	(0A)
(3)	(0C)
(4)	(11)
(5)	(12)
(6)	(14)
(7)	(21)
(8)	(22)
(9)	(24)
(0)	(42)
(•)	(41)
(#)	(44)

Figure 7. Typical Microprocessor Interface Circuit

Pulse Dialer

GENERAL DESCRIPTION

The XR-T5992 pulse dialer is a silicon gate CMOS integrated circuit which converts push-button inputs into pulses to simulate a rotary telephone dial.

It is designed to operate directly from the telephone line and to meet telephone specifications. A 17 digit buffer is provided for redialing feature. The XR-T5992 is available in a 18 pin package.

FEATURES

Direct Telephone Line Operation
Redial with Either a * or # Input
Pin Selectable Mark/Space and Dialing Rate
Inexpensive RC Oscillator
Interface Directly to a Standard Telephone
Push-button or Calculator Type X-Y Keyboard
Mute Driver on Chip
Pin-to-pin Compatible with MK50992

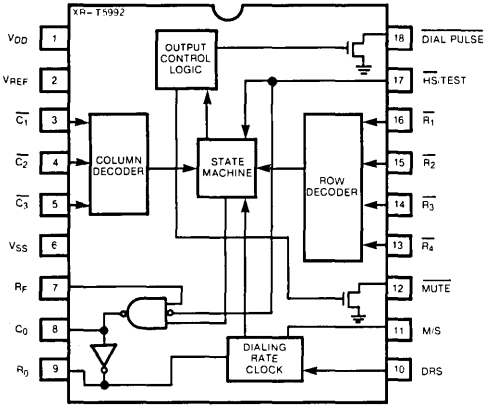
APPLICATIONS

Electronic Telephones
Smart Modems (Auto Dialer)
Security Controller

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V^+	6.2 Volts
Operating Temperature	0°C to 70°C
Input Voltage	$-.3 \leq V_{IN} \leq V_{DD} +.3$
Maximum Power Dissipation	500 mW

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5992CP	Plastic	0°C to 70°C
XR-T5992CN	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T5992 Pulse Dialer is a CMOS integrated circuit that can provide recall of previously entered numbers as well as perform the normal dialing function. It is capable of receiving keys faster than dialing rate. XR-T5992 is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone line. Selectable dialing rate is provided for rapid dialing.

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS: $0°C \leq T \leq 70°C$						
V_{DD}	DC Operating Voltage	2.5		6.0	V	
V_{REF}	Magnitude of ($V_{DD}-V_{REF}$)	1.5	2.5	3.5	V	I Supply = 150 μA
I_{OP}	DC Operating Current		100	150	μA	
I_{MR}	Memory Retention Current		.7	2.5	μA	
I_{ML}	Mute Sink Current	.5	2.0		mA	V_{DD} = 2.5 V, V_O = .5 V
I_{MH}	Mute Source Current	.5	2.0		mA	V_{DD} = 2.5 V, V_O = 2.0 V
I_P	Pulse Sink Current	1.0	4.0		mA	V_{DD} = 2.5 V, V_O = .5 V
K_L	Keyboard "0" Logic Level	V_{SS}		20% of V_{DD}	V	
K_H	Keyboard "1" Logic Level	80% of V_{DD}		V_{DD}	V	
K_{RU}	Keyboard Pull-up Resistance		100		KΩ	
K_{RD}	Keyboard Pull-down Resistance		4.0		KΩ	
HS_{RU}	Hookswitch Pull-up Resistance		100		KΩ	
f_{OSC}	Oscillator Frequency		4.0		KHz	
Δf_{OSC}	Oscillator Stability		±4		%	V_{DD} = 2.5 to 3.5 V
T_{DB}	Keyboard Debounce Time		10		ms	
T_{MO}	Mute Overlap Pulse		5		ms	
S_F	Keyboard Scanning Frequency		500		Hz	

PIN AND FUNCTION DESCRIPTIONS

Pin	Number
Supplies V_{DD}, V_{SS}	1, 6

Power Supply Inputs — The device is designed to operate from 2.5 to 6 volts.

V_{REF}	2

The V_{REF} output provides a negative reference voltage relative to V_{DD}, which defines minimum operating voltage. In a typical application this pin is simply tied to V_{SS}.

Keyboard Inputs	
C_1, C_2, C_3	3, 4, 5
R_1, R_2, R_3, R_4	16, 15, 14, 13

These inputs are open when the keyboard is inactive. When a key is pushed, an appropriate row and column input must go to V_{SS} or connect with each other.

A logic interface is also possible as shown in Figure 2.

Oscillator and keyboard scanning starts when a key is pressed.

Oscillator	
R_f, C_O, R_O	7, 8, 9

These pins are provided to connect external resistors and capacitor to form an R-C oscillator.

Dialing Rate Select	
DRS	10

Dialing rate is programmable by connecting this pin to V_{DD} or V_{SS}. The rate is .20 pps when connected to V_{DD}, and 10 pps when connected to V_{SS}.

Mark/Space Select	
M/S	11

Mark/Space ratio may be selected by connecting the pin to V_{DD} or V_{SS}.

M/S Pin (11)	Mark	Space
V_{DD}	34%	66%
V_{SS}	40%	60%

Mute	12

This N-channel open drain output is designed to drive an external bipolar transistor to mute the receiver during dialing.

Dial Pulse Out	18

Output drive is provided to turn on a transistor at the dial pulse rate. The normal output will be "low" during "space", and "high" otherwise.

Hookswitch/Test	17

This input detects the state of the hookswitch contact. The XR-T5992 will accept key inputs when this pin is at low state (off hook).

FUNCTIONAL DESCRIPTION

V_{REF}

The V_{REF} output provides a reference voltage that tracks internal parameters of the XR-T5992. V_{REF} provides a negative voltage reference to the V_{DD} supply. Its magnitude will be approximately 0.6 volt greater than the minimum operating voltage of each particular XR-T5992. For normal use this pin is connected to V_{SS}.

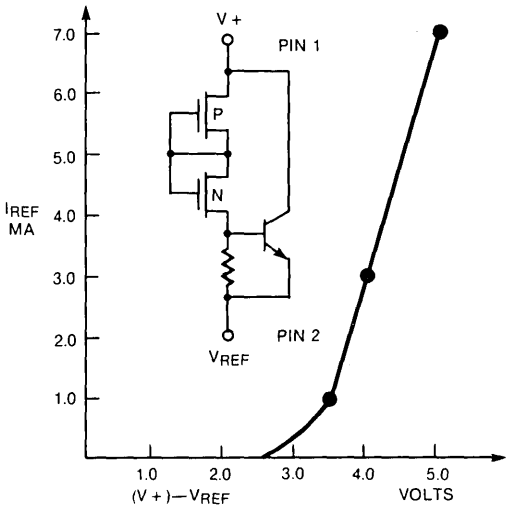


Figure 1. V_{REF} Typical I-V Characteristics

Keyboard

The XR-T5992 employs a scanning technique to determine a key closure. This permits interface to a DPCT keyboard with common connected to V_{SS} or SPST switch matrix connecting rows to columns.

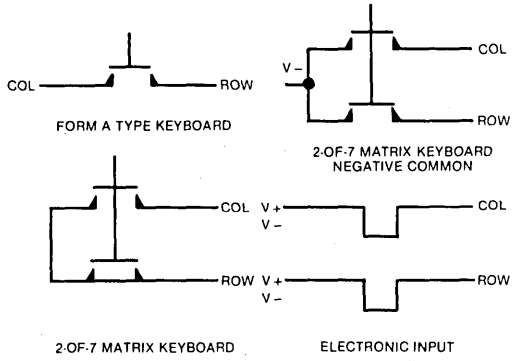


Figure 2. Keyboard Configurations

Oscillator

The device contains an oscillator circuit that requires three external components: two resistors and one capacitor. All internal timing is derived from this master timebase. For a dialing rate of 10 pps, the oscillator should be adjusted to 4000 Hz. Typical values of external components are R_f = 2MΩ, R_O = 220 KΩ, C_O = 390 pF.

The oscillator frequency can be determined by the following equation:

$$T=RC\ [\ 1.386\ +(3.5KC_S)/C\ -2(2K/(K+1))LN\ (K/1.5K+.5))]$$

where C_S is the pad capacitance on pin 7 optimum stability occurs with the ration $K = R_F/R_O$ equals 10.

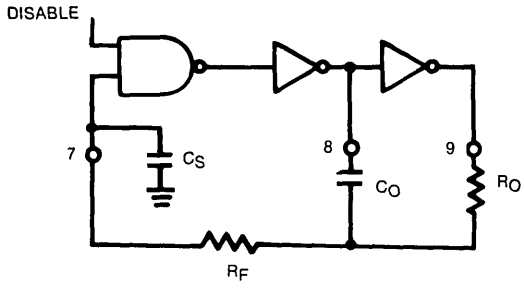


Figure 3. Oscillator Circuit

On Hook/Test

The hookswitch input of XR-T5992 has a 100 KΩ pull-up to the positive supply. A positive input or allowing the pin to float sets the circuit in its on hook, or test mode. Switching the XR-T5992 to on hook while it is outpulsing causes the remaining digits to be outpulsed at 100x the normal rate. This feature provides a means of rapidly testing the device.

$\overline{\text{Off}}$ Hook

The XR-T5992 will enter in off hook mode when hookswitch is pulled low. This state enables the device to accept a valid key and to turn the oscillator on.

$\overline{\text{Mute}}$ Output

The mute output turns on (pulls to the V_{SS} supply) at the beginning of the interdigit pause, and turns off (goes to an open circuit) following the last break. A small delay is provided to overlap mute output from the end of last break.

$\overline{\text{Pulse}}$ Output

The pulse output is an open drain N-channel transistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by disconnecting and connecting the network.

The XR-T5992 pulse out is an open circuit during mark and pulls to the V_{SS} during break.

Redial

The last number dialed is retained in the memory and therefore can be redialed by going off hook and pressing the * or # key. Dial pulsing will start when the key is depressed and finish after the entire number is dialed.

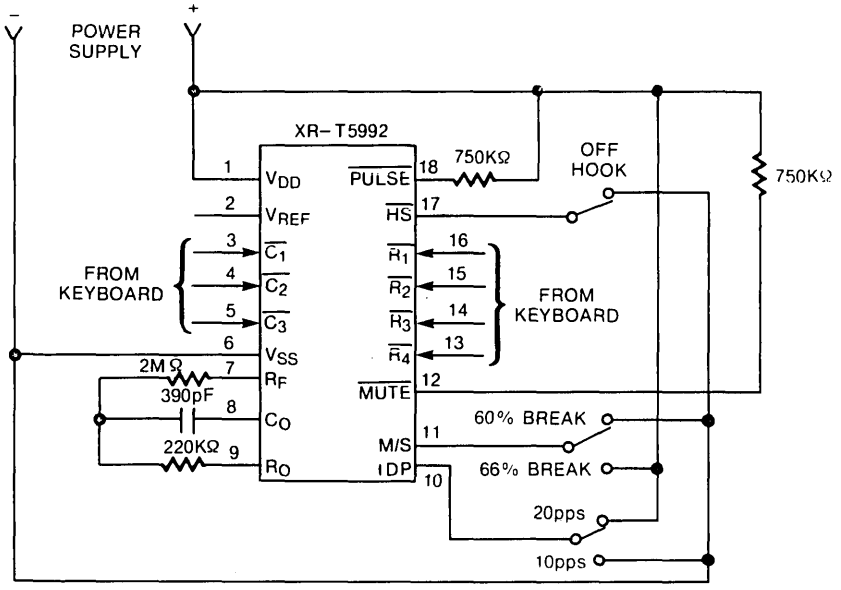


Figure 4. Test Configuration

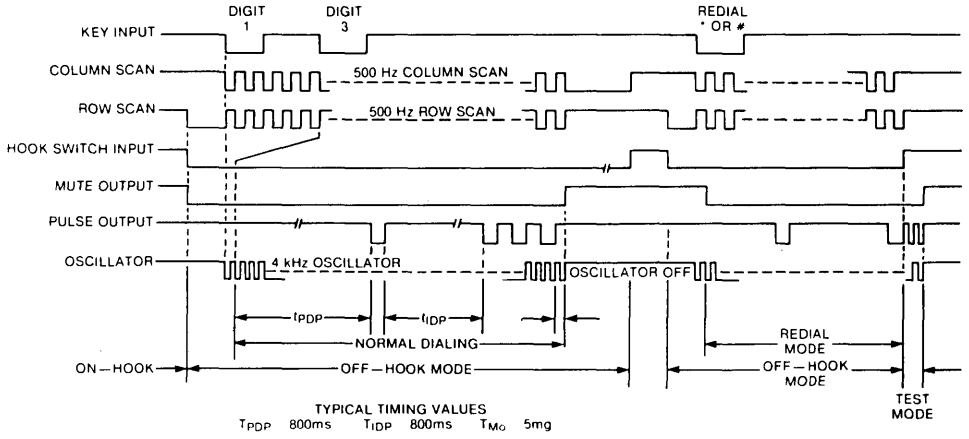
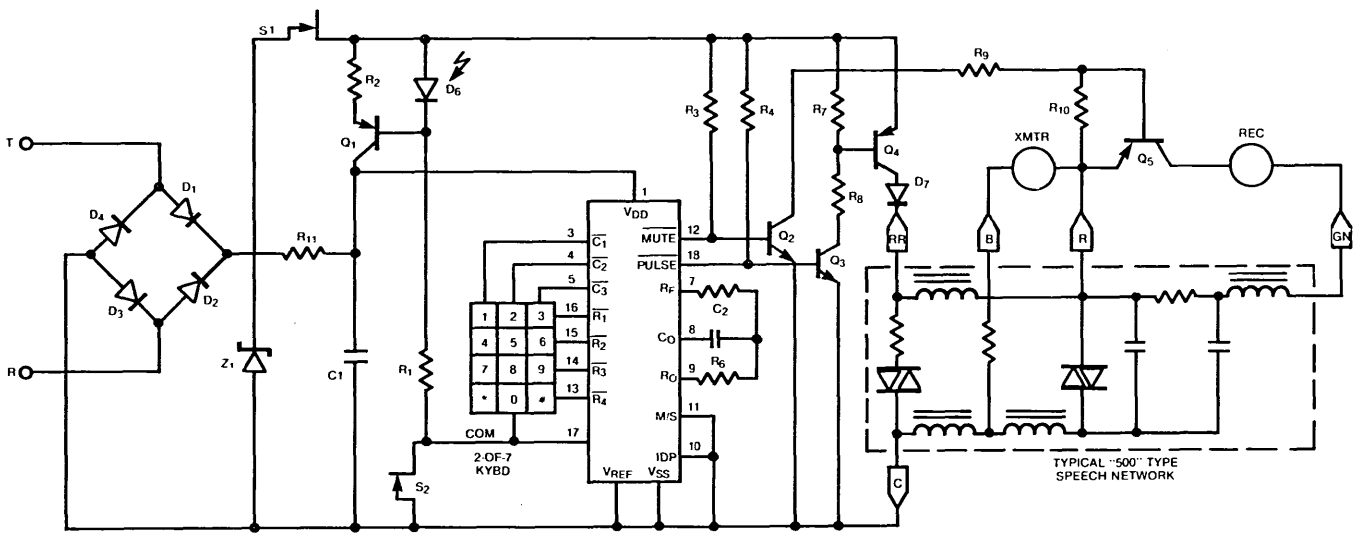


Figure 5. Timing Characteristics



R1 = 560kΩ
R2 = 1.4kΩ
R3 = 470kΩ
R4 = 330kΩ
R5 = 2MΩ
R6 = 220kΩ
R7 = 100kΩ
R8 = 3kΩ
R9 = 3kΩ
R10 = 100kΩ
R11 = 20MΩ
Q1 = 2N5401
Q2 = 2N5550
Q3 = 2N5550
Q4 = 2N5401
Q5 = 2N5401
D1 = 1N4004
D2 = 1N4004
D3 = 1N4004
D4 = 1N4004
D6 = LED
D7 = 1N4004
C1 = 68μ (Low Leakage)
C2 = 390pF
S1 = HOOK SWITCH
S2 = HOOK SWITCH
Z1 = 120-volt, 1-watt zener

Figure 6. Typical Application Schematic

Speech Network

GENERAL DESCRIPTION

The XR-T5995 Speech Network is a monolithic integrated circuit specifically designed for implementing a low cost telephone set circuit. It is designed to use a electrodynamic microphone and electromagnetic receiver to replace a carbon microphone and telephone network hybrid.

FEATURES

Interfaces with Inexpensive Condenser Electret Microphone, Electromagnetic Receiver
Low Voltage CMOS Process to Operate from 20 mA to 100 mA Loop Current
Minimum External Component Counts
Uses Inexpensive and Non-critical External Components
A DTMF Input for Tone Dialing
External Mute Capability

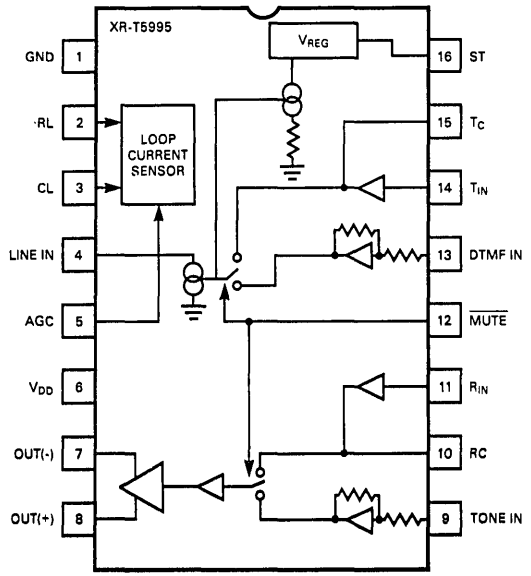
APPLICATIONS

Low Cost Telephone Set
Trimline Phone
Line Monitor

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{DD}	15 V
Operating Temperature	0°C to 70°C
Power Dissipation	1100 mW
Storage Temperature	-55°C to 125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5995CP	Plastic	0°C to 70°C
XR-T5995CN	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T5995 Speech Network contains all the necessary circuits to perform hybrid operation. (On board microphone, receiver amplifier and driver, external muting for tone dialing or pulse dialing.) A DTMF is provided to interface to Touch Tone dialing.

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_L	Operating Voltage	2.7		9	V	I = 20 –100 mA
I_L	Operating Current	15		100	mA	
GT	Transmitter Gain	39.5	43.5	47.5	dB	V_{IN} = 3 mV, f = 1 KHz
DT	Transmit Distortion		2.5	6	%	V_L = 1.2 Vp/p, f = 1 KHz
NT	Transmit Noise Level		–76		dB	V_M = 0
O_T	Transmit Output		2.3		Vp/p	
GR	Receiver Gain	–14.8	–10.8	–6.8	dB	V_L = 100 mV, f = 1 KHz
D_R	Receive Distortion		2.7	6	%	V_R = .3 Vp/p, f = 1 KHz
N_R	Receive Noise Level		–78		dB	V_L = 0 V
OR	Receiver Output Level			.6	Vp/p	
Z_{NET}	Network Impedance	350		750	Ω	V_L = .5 Vp/p, f = 1 KHz
ST	Side Tone	5	8		dB	
GDT	DTMF Gain	10	14	18	dB	V_{DT} = .03 V, f = 1 KHz
GAT	Audible Tone Gain	–7	–3	+1	dB	
Z_T	Transmit Input Impedance		12		KΩ	
Z_R	Receive Input Impedance		100		Ω	

PIN AND FUNCTION DESCRIPTIONS

Pin	Number
GND	1

Most negative supply terminal.

R_L, C_L	2,3

Current sense input, allows loop loos compensation for receiving or transmitting amplifiers.

LINE IN	4

To hold DC current and AC input impedance matching seen on the phone line.

AGC	5

Automatic gain control unit to set transmit and receive amplifier gain and attenuation on different line loop currents.

V_{DD}	6

Most positive regulated supply terminal.

OUT (–1), OUT (+)

Differential output driver, used to drive a speaker or an electromagnetic receiver.

TONE IN	9

External pacifier tone input, to provide audio feedback to the user that a key has been depressed in dial pulse mode.

R_C, R_{IN}	10,11

Input, output of receiving amplifier.

MUTE	12

External mute input is provided to mute the line receive amp and to insert the tone to the receiver.

DTMF IN	13

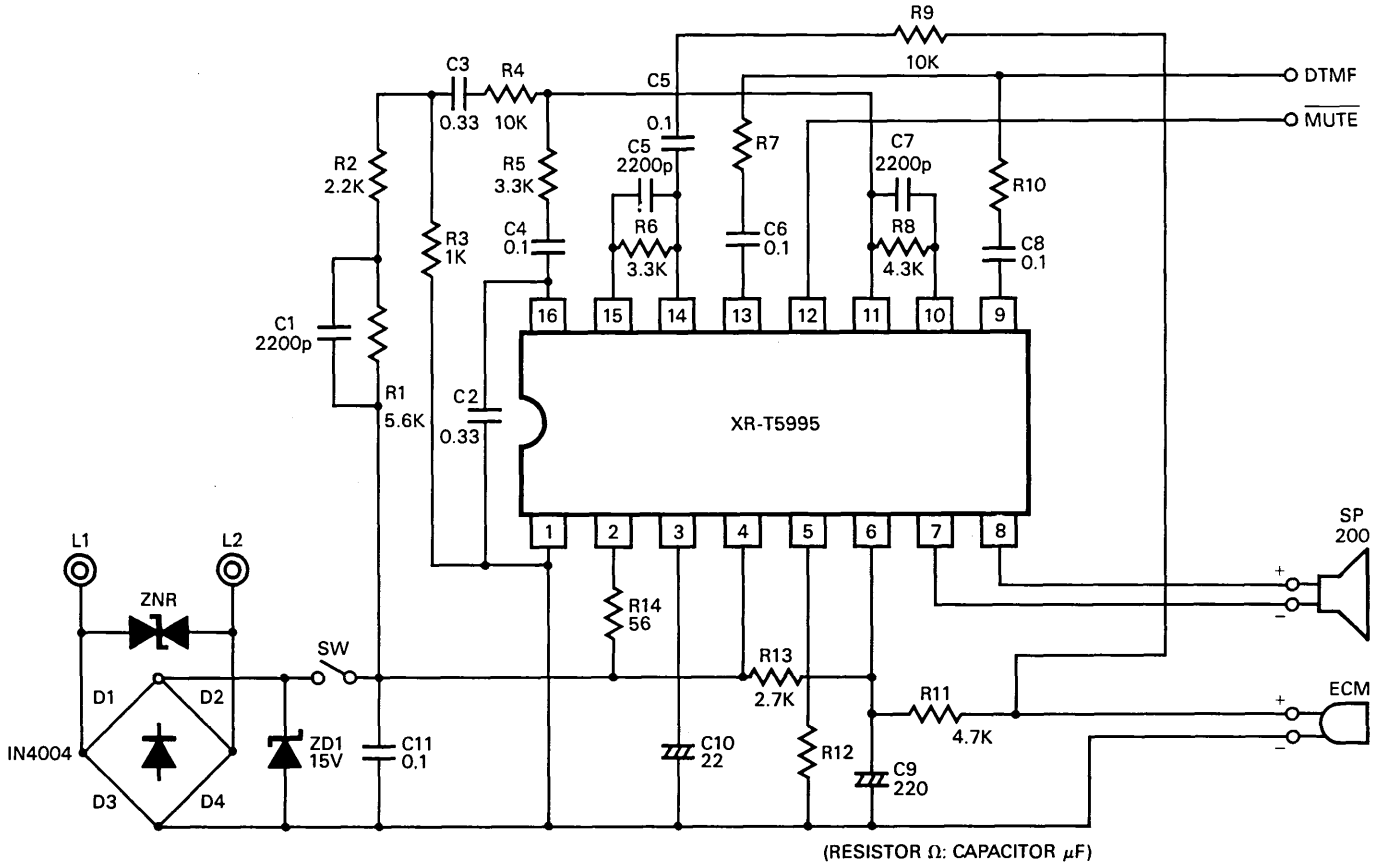
This input is used with a Touch Tone dialer to insert the DTMF signal to the line.

T_{IN}, T_C	14,15

Microphone input, output to transmitting amplifier.

ST	16

Sidetone compensation input.


R9
10K
C3
0.33
R4
10K
C5
DTMF
MUTE
0.1
C5
2200p
R7
C7
2200p
R10
R2
2.2K
R5
3.3K
R3
1K
C4
0.1
R6
3.3K
C6
0.1
R8
4.3K
C8
0.1
C1
2200p
R1
5.6K
C2
0.33
16
15
14
13
12
11
10
9
XR-T5995
1
2
3
4
5
6
7
8
SP
200
L1
L2
ZNR
SW
R14
56
R13
2.7K
R11
4.7K
ECM
D1
D2
IN4004
D3
D4
ZD1
15V
C11
0.1
C10
22
R12
C9
220
(RESISTOR Ω: CAPACITOR μF)

2-96

Tone Ringer

GENERAL DESCRIPTION

The XR-T8205 Tone Ringer is primarily intended as a replacement for the mechanical telephone bell. The device can be powered directly from telephone AC ringing voltage or from a separate DC supply. An adjustable trigger level is provided with an external resistor.

The XR-T8205 is designed for nominal 15 volt operation and is available in an 8 pin DIL package.

FEATURES

Low Supply Current
Operates Directly From Telephone Line
Provides Single or Dual Tone Frequencies to Simulate Mechanical Bell
Operates from 15 to 30 Volts
Pin-to-Pin Compatible with MITEL ML8205

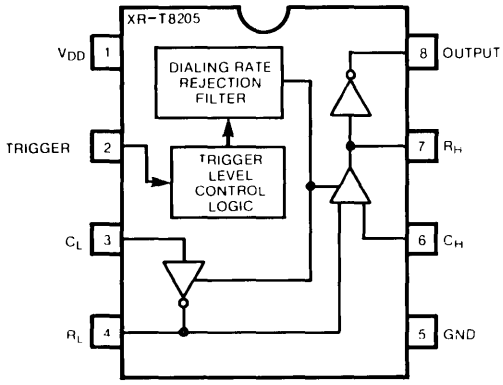
APPLICATIONS

Electronic Telephones
Alarm or Other Alerting Devices
Power Line Indicator
Toys

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to 70°C
Supply Voltage	30 V
Input Voltage	$-.3\ V \leq V_{IN} \leq V_{DD} + .3\ V$

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T8205CP	Plastic	0°C to 70°C
XR-T8205P	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-T8205 Tone Ringer consists of two oscillator circuits, a dial reject filter and an amplifier to drive high impedance audio transformer or plezo-electric transducers.

The power supply control circuit provides the hysteresis required to ensure positive triggering of the device and to prevent transient triggering due to dial pulsing.

As the power supply voltage to the XR-T8205 is increased up to the supply initiation voltage (V_{SI}), oscillation begins. The low frequency oscillator oscillates at a rate of F_L controlled by an external resistor and capacitor, connected between Pins 3 and 4. The output of F_L is internally connected to the switching threshold cicuitry of the high frequency oscillator.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 17 V T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{DD}	Operating Supply Voltage	15	17	30	V	
I_D	Operating Current	.7	1.2		mA	No Load
I_S	Supply Initiation Current	1.4	2.5	4.2	mA	No Load, R_T = 6.8 kΩ
I_T	Trigger Current	10	20	1000	μA	
V_o	Output Voltage	17	19	21	V	No Load, V_{DD} = 21 V
Δf_o	Oscillator Frequency Tolerance			10	%	

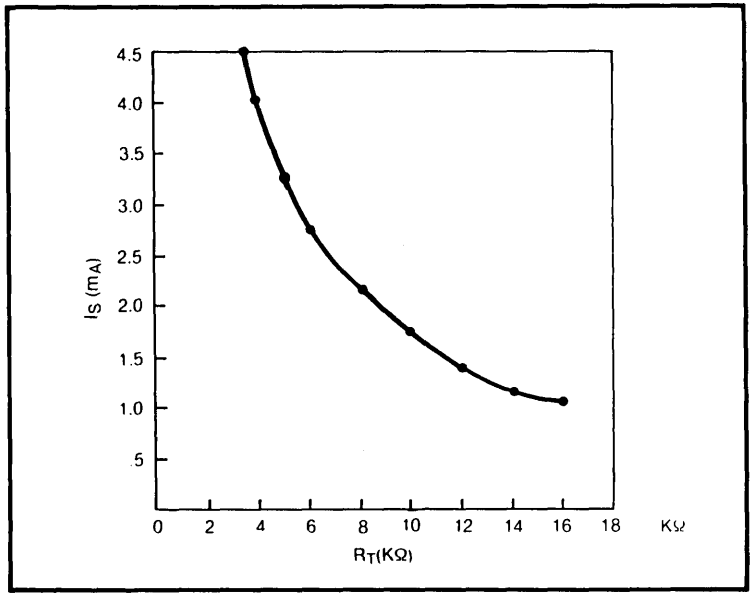


Figure 1. Supply Initiation Current (I_S) VS R_T

PIN AND FUNCTION DESCRIPTION

Pin	Number

Supplies

V_{DD}, GND 1, 5

Power supply inputs — the device is designed to operate from 15 to 30 volts.

Trigger In 2

This pin is provided to adjust power supply initiation current.

Rate Oscillator 3, 4

R_L, C_L Low frequency oscillator external components. Oscillation rate is determined using the relation $F_L = 1/(1.234\ R_L C_L)$ where R is the value of the resistor connected between Pin 3 and 4, and C is the value of the capacitor connected between Pin 3 to Ground.

Ringing Oscillator 6, 7

C_H, R_H High frequency oscillator external components. When the output of the rate oscillator is high, the high frequency oscillator oscillates at its normal rate, describes by the relation $F_H = 1/(1.515\ R_H C_H)$ where R is the value of the resistor connected between Pins 6 and 7, and C is the value of the capacitor connected between Pin 6 to Ground. When the output of rate oscillator is low, high frequency oscillator oscillation changes to $F_H = 1.25\ F_L$.

Output 8

The output amplifier of the XR-T8205 is capable of driving a wide range of load impedances, when driven from a low source impedance power supply.

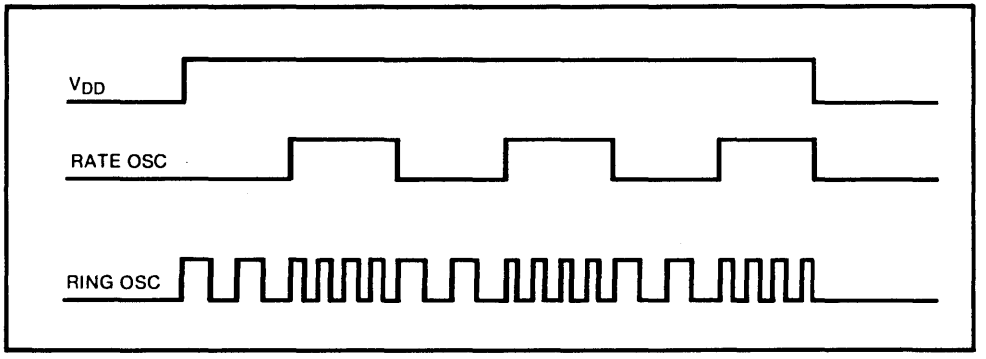


Figure 2. Ring and Rate Oscillator Relationship

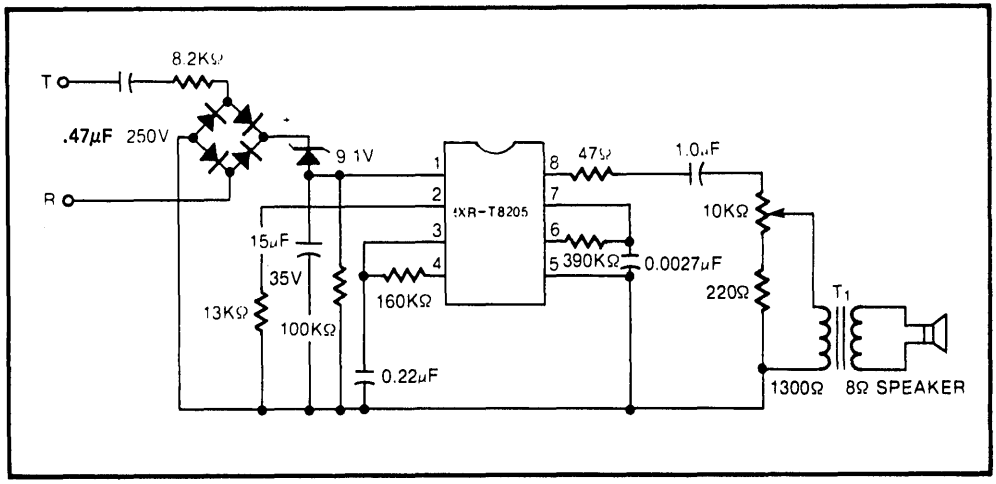


Figure 3. Typical Line Powered Tone Ringer Circuit

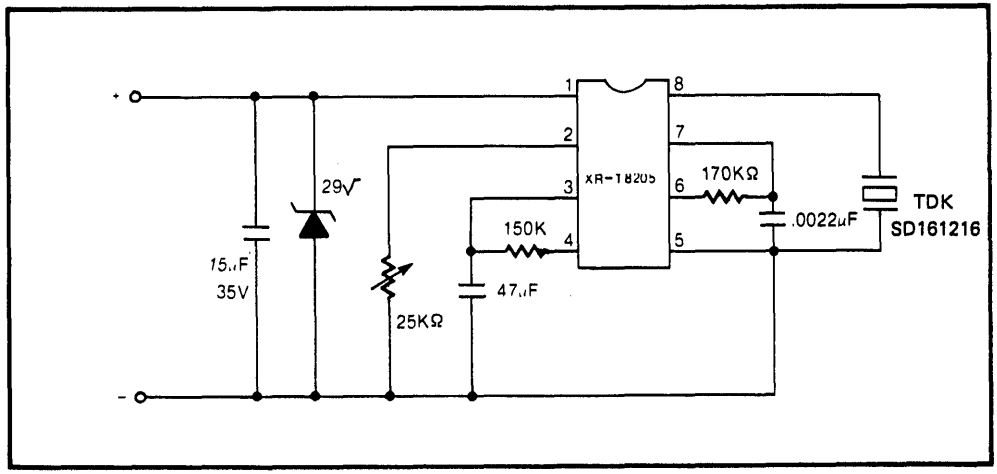


Figure 4. Typical Tone Ringer Circuit
Using Piezo-Electric

EXAR

Section 3 – Data Communication Circuits

Modem Basics

GENERAL INFORMATION

The **modem** or **mod**ulator/**dem**odulator serves as the interconnecting link for digital equipment to communicate over telephone or other wire media. As shown in Figure 1 the modem encodes (modulates) incoming binary data into signals suited for transmission over the available media.

Conversely on the opposite end, the other modem decodes (demodulates) the received signals from the line. In this figure, Rxd_2 (received data) would be identical to that of Txd_1 and Rxd_1 equal to Txd_2. That is a properly operating modem receiving an encoded signal would reproduce at its output exactly what the transmitting modem had at its Txd input. The modem initiating the "conversation" is termed the **originate** and the receive modem the **answer**. Figure 1 illustrates modems which have the ability to communicate both directions, which when able to do simultaneously is known as **full-duplex** operation. This same communication in both directions but only one direction at a time is **half-duplex** operation. Communication in only one direction is **simplex** operation. These modes of operation can be likened to a television for simplex, a CB which has to be keyed to talk for half duplex and a telephone for full duplex where both parties can talk at once.

Modem speeds of transmitting and receiving are specified in **BPS** (bits per second). This term describes the number of binary data bits that can be transmitted per second. For low speed modems, **baud rate** is interchangeably used in place of BPS. **Low** speed modems are usually those with 0 to 1200 BPS, **medium** speed for 2400 to 9600 BPS, and those above 9600 BPS **high** speed. Most modems are generally classified according to which **Bell** (US) or **CCITT** (European) standard they conform to. This standard indicates the modem speed, operation and encoding technique used. Figure 2 shows the most popular low and medium speed standards used.

MODULATION TECHNIQUES

Many types of encoding formats are used in modems, with the speed of the modem and type of media usually the determining factors. here the two most popular will be discussed, FSK and PSK.

FSK or frequency shift keying, illustrated in Figure 2, encodes binary data into two discrete frequencies.

STANDARD	SPEED	OPERATION	ENCODING TECHNIQUE
103	0-300 BPS	Full-Duplex	FSK
201	1200 BPS	Half-Duplex	PSK
202	1200 BPS	Half-Duplex	FSK
212A	0-300	Full-Duplex	FSK
	1200		PSK
	(A)		
V.21	0-300 BPS	Full-Duplex	FSK
V.22	1200 BPS	Full-Duplex	PSK
V.23	1200 BPS	Half-Duplex	FSK
	75 BPS		
V.26	2400 BPS	Half-Duplex	PSK
	(B)		

Figure 2. Popular Bell (A) and CCITT (B) Standards

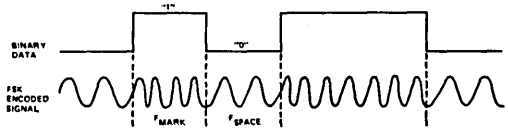


Figure 3. FSK Encoding

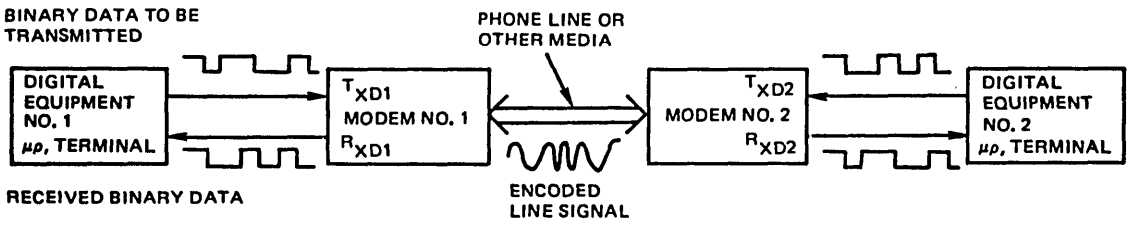


Figure 1. Modem System Block Diagram

The pair of frequencies used in the FSK scheme are chosen to be within the bandwidth of the media used. For example; the telephone line has a bandpass characteristic with the low frequency cutoff of about 300 Hz and a high frequency cutoff of about 3 kHz. For the telephone line the FSK frequencies would have to both fall within its 300 Hz to 3 kHz frequency restriction. With the FSK scheme the higher frequency is known as the **Mark** frequency and the lower the **Space.** The placing of the frequencies, as mentioned, strongly depends on the media bandwidth, however, the spacing between the mark and space frequencies also depends on the demodulation techniques used. For PLL (Phase-Locked Loop), demodulation, described in subsequent sections, the following relationships must be met:

A. For wide mark-space deviations (close to 2 to 1)
   fmark-fspace = $\Delta f \geq$ baud rate (BPS) X .83

B. For narrow spacing
   fmark - fspace = $\Delta f \geq$ baud rate (BPS) X .67

In full-duplex systems two mark/space frequency pairs must be used, one for answer mode and another for originate. This is necessary because of the simultaneous two way communication for full-duplex operation. The phase of the frequencies, one relative to the next, of mark to space or space to mark transitions can be either coherent or noncoherent. **Coherent** indicating that the phase is continuous on frequency transitions or the phase of the "new" frequency takes over where the "old" left off. **Noncoherent** indicating the phase of the new frequency has no relationship to that of the old. Here again the demodulation technique used being the determining factor of the necessity of phase coherency. PLL demodulation is one popular scheme requiring phase coherent FSK signals.

The other popular encoding scheme used is **PSK** or phase shift keying. Here a constant carrier frequency is used with the relative phase of it indicating the "value" of the binary data bit. Because the relative and not absolute phase of the carrier is important, most PSK schemes are **DPSK** or dibit PSK. DPSK measures the phase of the carrier in two successive bit frames in order to determine the phase change. Figure 4 illustrates PSK encoding, with Figure 5 listing the phase shifts and dibit values of two popular PSK modems.

PSK operates in either **SYNC** (synchronous) or **ASYN** (asynchronous) formats. Sync systems use a transmit clock from the digital equipment to clock data out and maintain synchronization. In this format the data stream itself has no synchronizing information. In ASYNC systems, there is no timing signal from the digital equipment to the modem. Here synchronization and timing information is derived from start and stop bits placed in the data stream bracketing each character. Timing is maintained by the modem inserting or removing stop bits. Figure 6 illustrates a terminal connected to a SYNC system in (A) and ASYNC system in (B). Different character lengths are used, with Bell 212A having options for 9 or 10 bit lengths, or 7 or 8 data bits each with one start and one stop bit.

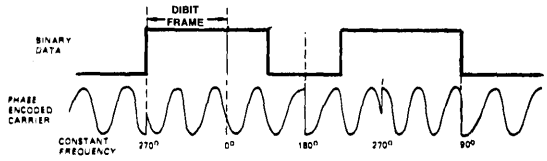


Figure 4. PSK Encoding

STANDARD	BELL 212A/V.22			BELL 201/V.26			
Phase Shift	0°	+90°	−90°	+180°	45°	135°	225°	315°
Dibit Value	01	00	11	10	00	01	11	10

Figure 5. Popular Phase Shifts and Dibit Values

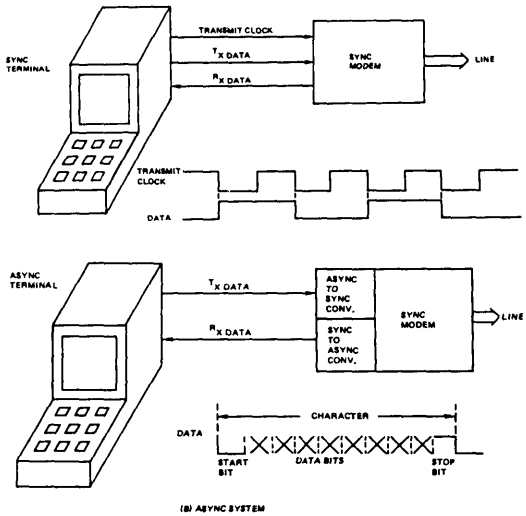


Figure 6. SYNC and ASYNC Formats

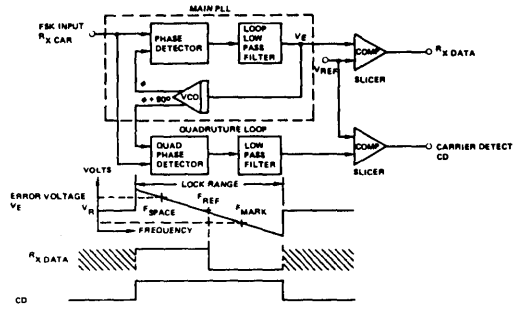


Figure 7

DEMODULATION TECHNIQUES

Once data has been encoded onto a carrier, Txcar, by the modulator in either FSK or PSK formats, the receiving modem (answer mode) must decode or demodulate this received carrier, Rxcar. For FSK encoding, analog and digital techniques are used for demodulation. Popular analog schemes often employ PLL type demodulation. Using this method, illustrated in Figure 7, a PLL locks to the incoming FSK frequencies and produces two different DC error voltages at the phase detector output. These voltages are compared to a reference to indicate whether the incoming frequencies lie above or below a reference frequency, or whether they are mark (high) or space (low) frequencies.

A second phase detector (quadrature) is often added whose output, when filtered and sliced, produces a carrier detector (**CD**) output. This output is active only when the PLL is in lock, allowing an indication when valid data is present at Rx data.

PSK demodulators typically employ one of two popular schemes, differential digital or coherent demodulation techniques. The differential scheme examines zero crossings to determine carrier phase. With coherent demodulators internal PLL's are used to lock and to determine the phase of the incoming carrier. Coherent schemes usually provide better overall performance, but at the sacrifice of higher circuit complexity and cost.

The demodulator affects and determines several key parameters of the modem. The demodulation process adds several degradations to the other originally transmitted data. One, **Bias distortion**, illustrated in Figure 8, is easiest seen in an alternating 0,1,0,1... data pattern. This pattern should have equal times for each bit, high (1) and low (0) ($T_{1t} = T_{0t}$).

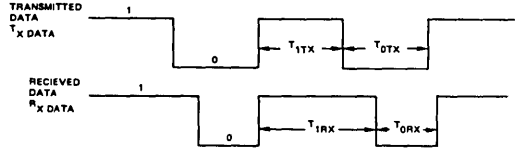


Figure 8. Bias Distortion

Bias distortion describes how far from equal the received data, Rx_{data}, high and low times are:

$$\text{Bias distortion (\%)} = \left[(.5)\frac{T1RX}{T1PX + T0RX}\right] 100$$

Output jitter is another parameter describing the quality of the demodulation process. Illustrated in Figure 9 again with an alternating 0,1,0,1... data pattern.

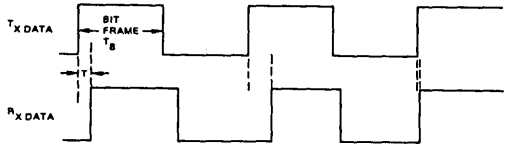


Figure 9

The output jitter is usually specified in percent, indicating what percentage of the bit frame the peak to peak jitter is.

$$\text{Jitter (\%)} = \left[\frac{Tmaximum - Tminimum}{T_b}\right] 100$$

FILTER REQUIREMENTS

Filters in modems serve two functions; to filter the modulator output for band limiting and filtering of the received carrier (Rxcar) before the demodulator. Figure 10 illustrates these filter functions.

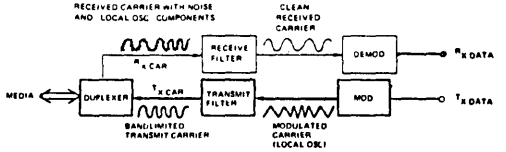


Figure 10. Transmit/Receive Filtering

The transmit filter is typically a lowpass or bandpass structure. As this filter is used to bandlimit the modulated carrier, it is usually of low order (low number of poles to zeros). The complexity is defined by the frequency spectrum generated by the modulator and how well this has to be confined on the media. For example; telephone lines have restrictions as to the amplitude of frequency even above its narrow 3 kHz band width (see FCC requirements).

The receive filter serves two functions: remove noise from the received signal and more importantly remove any local modulator signal which gets mixed with the receiver carrier. Figure 11 illustrates the function of the receive filter.

An additional block (duplexer) must be considered when specifying the receive filter. The duplexer acts to channel the received carrier from the media to the demodulator, A, and channel the transmit carrier to the media, B (four to two wire conversion). Imperfections in the duplexer allow some of the Txcar to get into the Rxcar, C. Therefore, to maintain a good **S/N** (signal to noise) ratio at the demodulator input, Rxcar, the receive filter must remove this unwanted local Txcar. An example illustrates the consideration in terminating the complexity of the receive filter. In this case, an FSK, Bell 103 Type, modem is examined, as shown in Figure 11, with the following requirements:

Demodulator: fmark = 2225 Hz; fspace = 2025 Hz,

$$fc = \frac{2225\ Hz - 2025\ Hz}{2} = 2125\ Hz$$

Rxcar dynamic range = −10 dBm to −48 dBm

s/n at Rxcar = 15 dB

Modulator: fmark = 1270 Hz, fspace = 1070 Hz, fc = 1170 Hz

Txcar (B) = −9 dBm

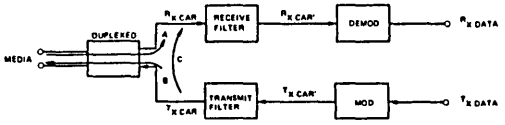


Figure 11. Modem Signal Paths

Because of line impedance variations, 600Ω ± 100Ω or more (telephone lines), the duplexer may only be able to maintain 10 dB of Txcar ejection to the receive filter input. Rxcar will contain more than -19 dBm of Txcar and at a minimum, Rxcar = 54 dB [Path (A) has a 6 dB loss due to termination]. If the receive filter has 0 dB passband gain, to achieve a 15 dB s/n ratio at Rxcar the Txcar "bleed through" (Path C) attenuation is calculated as follows:

at Rxcar: Signal = 54 dBm

Txcar (C) = -54 dBm -15 dBm = -69 dBm

Attenuation = -10 dBm - (-69 dBm) = 50 dB

The filter requirements are illustrated in Figure 12.

Other requirements to consider are filter bandwidth, which optimally is set close to the FSK baud rate, or here 300 Hz (small bandwidths can alter the transmitted carrier's spectrum). The phase response or specifically group delay within the passband can degrade the quality of the Rx data in terms of jitter. The **group delay (GD)** is a measure of the difference in time it takes for a mark or space frequency to pass through the filter. It is calculated by taking the first derivative of phase, with respect to frequency:

$$GD = \frac{d\theta}{df}$$

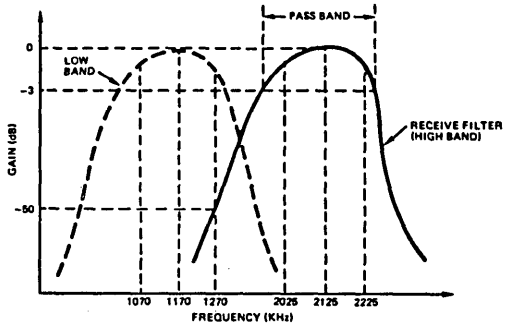


Figure 12. 103 FSK Receive Filter

Typical differential group delay values for the 103 example are 50 - 300 us over the pass band.

For full or half-duplex modems the receive filter can be used for transmit filtering of the opposite band, shown in Figure 13 (mode switching).

An additional filtering requirement for many modems must be considered. This is the second harmonic con-

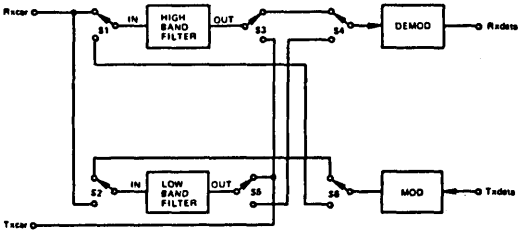


Figure 13. Mode Switching

tent of the transmitted local carrier. An example of problems caused by the term are seen in the FSK 103 type modem. If the local modulator is transmitting 1070 Hz, the second harmonic content (2140 Hz) falls right in the receive filter's passband. Therefore, the transmit filter must attenuate this harmonic content to an acceptable level.

PHONE LINE INTERFACING

The phone line interfacing has to couple the Txcar onto the line while removing the Rxcar and channeling it to the receiver. Figure 14 shows a simple acoustical connection which uses the telephone's internal carbon microphone and speaker.

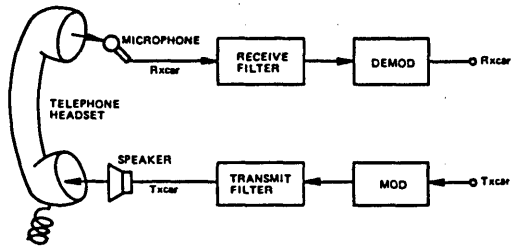


Figure 14. Acoustical Coupling

In this connection the telephone headset itself acts as the duplexer or 2 to 4 wire converter. Attenuation of Txcar to Rxcar should be infinite, but mechanical transmission or bleed through may occur and should be considered.

Typically acoustical coupling is only used for FSK type modems with low data rates, 1200 BPS and down. This is because of the poor quality carbon microphones found in most telephones.

The other coupling configuration is the direct connect, typically design **DAA** (Direct Access Arrangements). The DAA, shown in Figure 15, serves to:

1. Provide DC isolation between modem and telephone line-T_1.

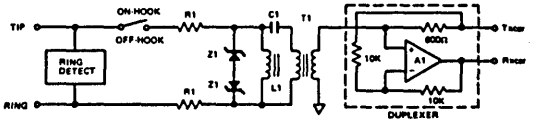


Figure 15

2. Provide a ring detect to control the on/off hook switch—may be manual.

3. Provide a DC current path during off—hook to "hold" the Line—L1. This current is monitored by the telephone company to indicate when someone is connected to the line.

4. Provide transient protection—R_1/Z_1.

A hybrid transformer is often used in place of the differentially connected op amp to perform the duplexer function, shown in Figure 16.

The hybrid transformer, T_1, provides better Txcar bleedthrough attenuation (typically 20 dB) but at additional expense over the op amp duplexer.

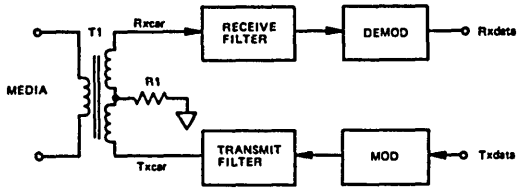


Figure 16

COMPLETE MODEM SPECIFICATIONS

Line signals received by the modem are often greatly changed by the media from the originally transmitted signal at the originating modem. With telephone communications Bell specifies five different lines which appear in standard dial-up lines as shown in Figure 17. Since which line will appear is totally unknown, the worst case line (Bell 3002) is generally used for modem evaluation.

From Figure 17 it can be seen that severe amplitude variations can occur on received line signals. Typically modems should function with received line signals from 0 to -45 dBm (2.2V to 12.3 mVp-p).

Group delay also can experience large changes. Figure 18 shows the general shape of the group delay characteristics as a function of frequency. Medium to high speed modems (PSK encoding) generally use some kind of equalization to compensate for group delay variations. The dotted line in Figure 18 illustrates a compromise line equalization to flatten the effective group delay variation.

Direct connection to the telephone line requires FCC approval as specified in Part 68 of the FCC regulations. One of the main requirements of this FCC regulation is the maximum in-band power levels over frequency bands not only within the 300 to 3000 Hz line bandwidth, but also above it be restricted to given levels. Figure 19 shows the maximum power levels to be put on the line.

Because modems communicate over vast distances often automatically operated, test facilities are often added. These test facilities are used to test the local modem as well as the distant one. Figure 20 illustrates these functions.

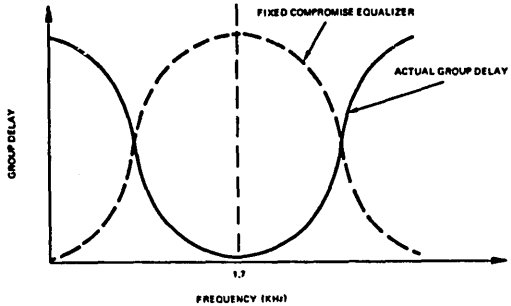


Figure 18. Group Delay Characteristics

Frequency (KHz)	3.995 to 4.005	4 to 10	10 to 25	25 to 40	Above 50
Maximum Power Level (dBm)	−18	−16	−24	−36	−50

Figure 19. FCC Phone Line Restrictions

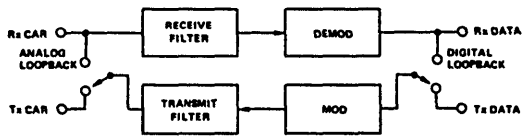


Figure 20. Test Facilities

BELL SCHEDULE	3002	C1	C2	C4	DCS-S#
Attenuation Characteristic (referenced to 1000 Hz)	300 to 3000 Hz −3 to +12 dB	300 to 2700 Hz −2 to +6 dB	300 to 3000 Hz −2 to +6 dB	300 to 3200 Hz −2 to +6 dB	300 to 3000 Hz −1 to +3 dB
Envelope Delay Distortion (max. μsec)	800 to 2600 Hz 1750 μsec	1000 to 2400 Hz 1000 μsec	1000 to 2600 Hz 500 μsec	1000 to 2600 Hz 300 μsec	1000 to 2600 Hz 100 μsec
		800 to 2600 Hz 1750 μsec	600 to 2600 Hz 1500 μsec	800 to 2800 Hz 500 μsec	600 to 2600 Hz 300 μsec
			500 to 2800 Hz 3000 μsec	600 to 3000 Hz 1500 μsec	500 to 2800 Hz 600 μsec
				500 to 3000 Hz 3000 μsec	

Figure 17. Bell Dial-up Line Characteristics

EXAR CROSS REFERENCE TO MODEM TYPE

XR PART NUMBER	FUNCTION	STANDARD	
		BELL	CCITT
XR-210	FSK Mod or Demod	103, 212A (FSK), 202, NS	V.21, V.23, NS
XR-2211	FSK Demod	103, 212A (FSK), 202, NS	V.21, V.23, NS
XR-2206	FSK Mod	103, 212A (FSK), NS	V.21, V.23, NS
XR-2207	FSK Mod	103, 212A (FSK), NS	V.21, V.23, NS
XR-14412	FSK Mod/Demod	103	V.21
XR-2103	FSK Filter	103	
XR-2120	PSK/FSK Filter	212A, 103	V.22 (needs 1800 Hz notch)
XR-2121	PSK/FSK Modulator	212A	V.22 (no guard tone generator)
XR-2122	PSK/FSK Demodulator	212A	V.22
XR-2123	PSK Mod/Demod	212A (PSK), 201	V.22, V.26, NS
XR-2125	Data Buffer	212A	

NS = Non Standard

EXAR MODEM SUPPORT CIRCUITS

XR PART NUMBER	FUNCTION
LINE INTERFACE	
XR-1488	Quad Line Driver
XR-1489	Quad Line Receiver
OPERATIONAL AMPLIFIERS	
XR-082/083	Dual Bipolar JFET Operational Amplifier
XR-084	Quad Bipolar JFET Operational Amplifier
XR-094	Quad Programmable Bipolar JFET Operational Amplifier
XR-095	Quad Programmable Bipolar JFET Operational Amplifier
XR-096	Quad Programmable Bipolar JFET Operational Amplifier
XR-146/246/346	Programmable Quad Operational Amplifier
XR-1458/4558	Dual Operational Amplifier
XR-3403/3503	Quad Operational Amplifier
XR-4136	Quad Operational Amplifier
XR-4202	Programmable Quad Operational Amplifier
XR-4212	Quad Operational Amplifier
XR-4739	Dual Low-Noise Operational Amplifier
XR-4741	Quad Operational Amplifier
TONE DECODERS	
XR-567/567A	Monolithic Tone Decoder
XR-L567	Micropower Tone Decoder
XR-2567	Dual Monolithic Tone Decoder

Bell 212A Type Modulator

GENERAL DESCRIPTION

The XR-2121 is designed to provide the complete modulator function for a Bell 212A type modem. The circuit accepts a synchronous serial data stream and generates either a 300 BPS frequency shift keyed (FSK) or a 1200 BPS differential phase shift keyed (DPSK) carrier signal. An on-board digital-to-analog converter provides a synthesized sine wave output. Also provided on the transmitted carrier output is an inverting amplifier with external feedback resistor to provide a carrier amplitude adjust.

The XR-2121 contains an internal 17 bit scrambler. This scrambler which is used during DPSK operation has a disable input for sending non-scrambled carriers.

A 1200 Hz transmit clock output is provided for 1200 BPS operation, although the XR-2121 will also accept an external transmit clock. For test or other purposes, a 600 Hz baud clock output is also supplied.

The XR-2121 is constructed using silicon gate CMOS technology. The main clock frequency input is 1.8432 MHz. The XR-2121, available in a 22 Pin (0.4 inch wide) package, is designed to operate from +5 volt and -5 volt power supplies.

FEATURES

Bell 212A Compatible
1200 BPS DPSK
300 BPS FSK
Digital Modulation Techniques for DPSK
External Transmit Clock Input
600 Hz Dibit Clock Output
Complete Scrambler Function with Disable Input
Transmit Carrier Level Adjust
1.8432 MHz Clock
±5 Volt Operation

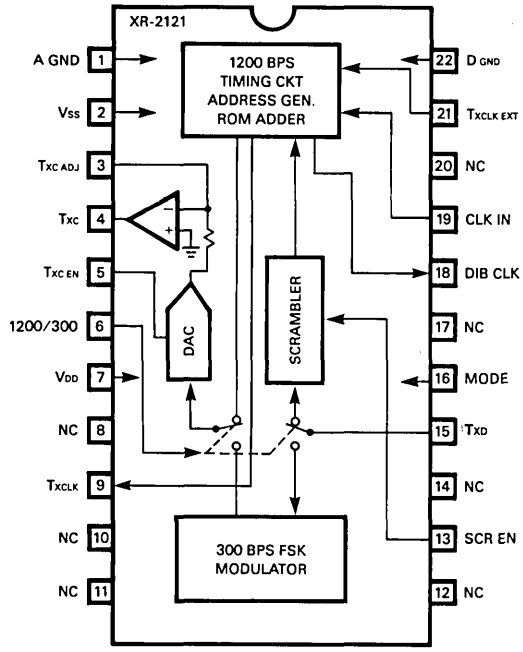
APPLICATIONS

Bell 212A Type Modulator
Bell 103 Type Modulator

ABSOLUTE MAXIMUM RATINGS

Power Supply	
V_{DD}	-0.3 to +7V
V_{SS}	+0.3 to -7V
Input Voltage	V_{SS} -0.3V to V_{DD} +0.3V
DC Input Current	±10 mA
Power Dissipation	1.0 W
Derate Above 25°C	5 mW/°C
Storage Temperature Range	-65°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2121CN	Ceramic	0°C to 70°C
XR-2121CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2121 basically has two types of operation, 1200 BPS DPSK or 300 BPS FSK. For 1200 DPSK the XR-2121 generates carrier frequencies of 1200 Hz or 2400 Hz, depending on mode selection (originate or answer). The carrier frequencies are imposed with phase shifts to carry the data to be transmitted (T_{XD}) over the telephone network. The phase shifts correspond to the incoming data grouped in pairs (dibits) and are one of four values — 0°, 90°, −90°, 180°.

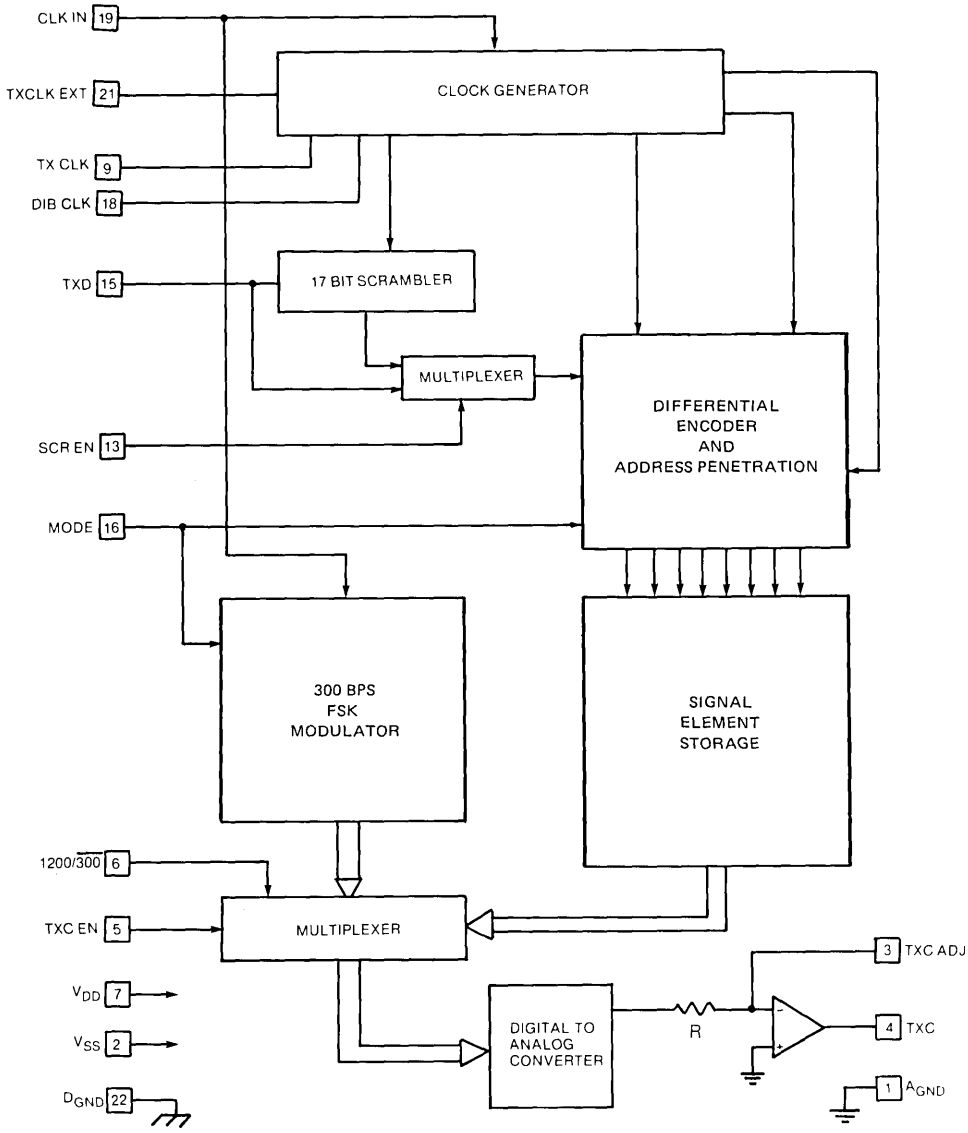
During 300 BPS FSK operation, the XR-2121 generates one of two pairs of frequencies to represent the T_{XD}. These pairs are either 1070 Hz/1270 Hz or 2025 Hz/2225 Hz depending on mode selection.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V ±5%, V_{SS} = -5 V ±5%, CLK IN = 1.8432 MHz ±0.01%, T_A = 0°-70°C unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{DD}	Positive Supply Current		2.5	4	mA	
I_{SS}	Negative Supply Current		-1.5	-2.5	mA	
DIGITAL INPUTS/OUTPUTS						
V_{OH}	Output High Voltage	2.4			V	I_O = 1 mA
V_{OL}	Output Low Voltage		0.4	0.8	V	I_O = -1.5 mA
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
I_{OH}	Output Drive Current	0.5	1.5		mA	V_{OH} = 3.5 V
I_{OL}	Output Drive Current	2.0	4.0		mA	V_{OL} = 0.5 V
I_{IN}	Input Current			10	μA	
ANALOG SECTION						
V_{TXC}	Transmit Carrier Amplitude		-4		dBM	R_{EXT} = 10k
V_{TXC2H}	Transmit Carrier Amplitude 2nd Harmonic Content		-40		dB	$R_L \geq$ 10k

3



EQUIVALENT SCHEMATIC DIAGRAM

PRINCIPLES OF OPERATION

The XR-2121 is designed to perform all the necessary functions for the modulator section of a Bell 212A type modem. It has been specifically designed to operate with the XR-2120 filter, XR-2122 demodulator, and XR-2125 data buffer to form the complete Bell 212A type modem signal processor. This data sheet will cover just the XR-2121 and its functions with Application Note AN-28 covering the complete system.

The XR-2121 has two basic types of operation; that of a 1200 BPS differential phase shift keyed (DPSK) or 300 BPS frequency shift keyed (FSK) modulator.

The 1200 BPS section of the XR-2121 converts a serial synchronous data stream (T_{XD}) into a DPSK encoded carrier suited for transmission over a standard telephone switched network. The incoming data, T_{XD}, is clocked into the XR-2121 by either an internally generated transmit clock, T_X CLK, or an externally applied clock, T_X CLK EXT. The internal T_X CLK is derived from the main 1.8432 MHz clock, and is precisely 1200 Hz. If an external transmit clock is applied to the T_X CLK EXT input, T_X CLK will become phase locked to T_X CLK EXT. Figure 1 shows the relationship between T_{XD} and T_X CLK (1A) and T_X CLK and T_X CLK EXT (1B).

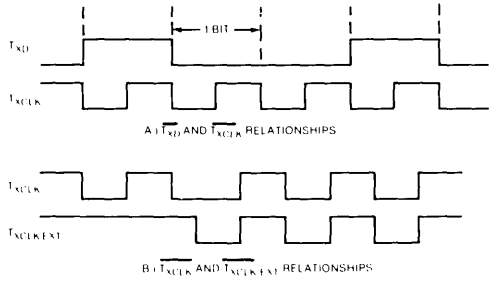


Figure 1. Transmit Data & Clock Relationships

As seen in Figure 1, data is clocked into the XR-2121 on the falling edge of T_X CLK.

1200 BPS data entering the XR-2121 is passed through a scrambler circuit, as shown in Figure 2.

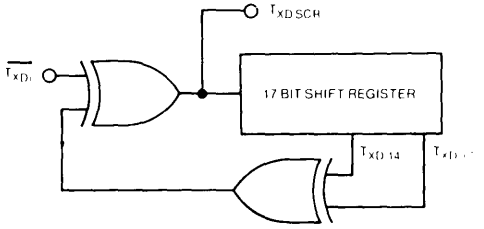


Figure 2. 17 Bit Psuedo Random Scrambler

The output of the scrambler produces a psuedo-random output which can be described by the following equation:

$$T_{XD\,SCR} = T_{XDI} \oplus T_{XD-14} \oplus T_{XD-17}$$

$\oplus$ = exclusive – or operation

The main purpose of the scrambler is to assure that the transmitted carrier will not have extended periods of 0° phase shifts. This condition would cause the receiving modem's demodulator to loose lock and be unable to extract clock information from the received carrier. This condition is discussed further within the XR-2122 data sheet.

The scrambled data is fed into the actual modulator section of the XR-2121. This section phase encodes a constant frequency carrier to represent the incoming serial data, T_{XD}.* This type of phase encoding phase shift the carrier every two data bits. Figure 3 shows the relationship between the transmitted data, its clock, and the resultant phase encoded carrier. As seen in this figure, although the data rate is 1200 BPS, the baud rate is only 600. This is because phase changes only occur every two data bits or dibits. Table 1 gives the phase changes for the four possible dibit values.

*The transmit carrier frequencies for 1200 BPS operation are either 1200 Hz for originate mode or 2400 Hz for answer mode.

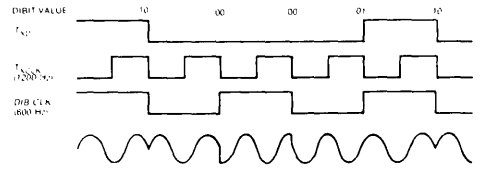


Figure 3. $\overline{T_X\ CLK}/\overline{T_{XC}}$ Timing

DIBIT	PHASE CHANGE
0 0	+90°
0 1	0°
1 0	180°
1 1	−90°

Table 1. Carrier Phase Change vs Dibit Value

It should be noted that the phase changes are relative values. That is, each phase change as shown in Table 1 is relative to the previous carrier phase.

Figure 3 shows the T_{XC} being phase shifted, however, the XR-2121 does not introduce abrupt changes as shown there. This figure was drawn in this fashion for clarity. The XR-2121 uses digital echo modulation techniques. This technique allows incremental or slowly changing phase changes. Using this method also allows precise shaping of the frequency spectrum. The spectrum analyzer photograph in Figure 4 shows the carrier spectrum for each carrier frequency. It can be seen from the photo that separation of about 40 dB between the two spectrums is possible even before bandpass filtering. The frequency spectrums are designed for square root raised cosine shaping.

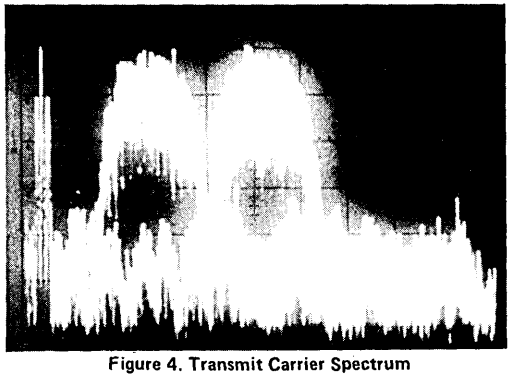


Figure 4. Transmit Carrier Spectrum

For 300 BPS operation frequency shift keying, FSK, encoding techniques are used. For this operation bit asynchronous serial data is fed into the XR-2121 data input. Being asynchronous, no transmit clock is used. The scrambler is bypassed for 300 BPS operation.

FSK encoding uses pairs of frequencies to represent input data changes. Figure 4 shows the incoming data, T_{XD}, and carrier output relationships.

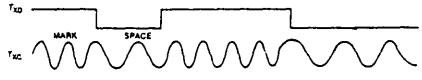


Figure 5. FSK Data Carrier Relationships

The pairs of frequencies used for the two different modes are shown in Table 2. The higher frequency in each pair is known as the mark frequency with lower the space.

MODE	CARRIER FREQUENCIES (MARK/SPACE)
Answer	2225 Hz/2025 Hz
Originate	1270 Hz/1070 Hz

Table 2. FSK Carrier Frequencies

Unlike 1200 BPS operation, for 300 BPS, the baud rate is the same as the data rate, 300. This is of course because every input data change causes a carrier frequency shift.

The outputs of both 1200 BPS and 300 BPS sections are fed into a multiplexer which routes the proper one to the output section depending on speed selection. The output circuitry consists of a seven bit digital-to-analog converter (DAC) and an output operational amplifier. The op amp is configured as an inverting amplifier with the DAC feeding an input resistor and the feedback resistor placed externally. This allows T_{XC} amplitude adjustment at this point. Pin 5, T_{XC} EN, can be used to disable transmission if desired.

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	AGND	This is analog or signal ground. It should not carry logic or heavy currents.
2	V_{SS}	Power input for the negative power supply which is typically -5.0 volts.
3	TXCADJ	This is the inverting input of the output op amp. A resistor (R_{EXT}) from this pin to pin 4 (T_{XC}) sets the output amplitude of the T_{XC} (see Figure 6).
4	T_{XC}	This is the transmit carrier output.
6	1200/$\overline{300}$	Speed select input to set either 1200 BPS DPSK or 300 BPS FSK operation.
7	V_{DD}	Power input for the positive power supply which is typically +5.0 volts.
9	TXCLK	The transmit clock is output on this pin. It is internally generated from the main clock input (pin 19) and is used internally to clock T_{XD} into the XR-2121.

13	SCR EN	The data scrambler can be enabled or disabled by this pin during 1200 BPS operation.
15	$\overline{TXD}$	This is the serial data input.
16	MODE	Answer or originate modes are selected by this pin.
18	DIB CLK	The 600 Hz dibit clock is output on this pin. It may be used during system testing such as digital loopback to provide an alternating 1010... data pattern.
19	CLK IN	This is the main clock input and should be 1.8432 MHz ±0.01%.
21	$\overline{TXCLK\ EXT}$	An external transmit clock may be applied to this input during 1200 BPS operation ∓0.01%.
22	DGND	This is the ground for the logic circuitry of the XR-2121.

CONTROL INPUTS

Table 3 gives logic conditions for the various control inputs of the XR-2121.

PIN	NAME	FUNCTION LOGIC HIGH	LOGIC LOW
5	TXC EN	Carrier Enabled	Carrier Disabled
6	1200/$\overline{300}$	1200 BPS Operation	300 BPS Operation
13	SCR EN	Scrambler Enabled	Scrambler Disabled
16	MODE	Answer	Originate

Table 3. Control Input Conditions

APPLICATIONS

A typical connection of the XR-2121 is shown in Figure 6.

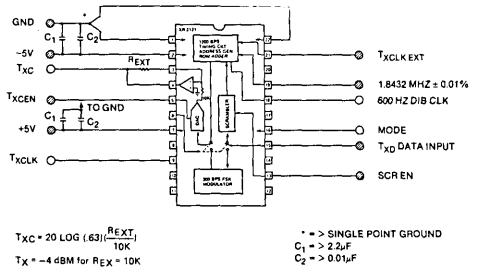


Figure 6. XR-2121 Typical Connection

The synchronous data stream is fed into T_{XD} with the T_{XC} output being either a DPSK or FSK encoded carrier. In a complete system the T_{XC} would go to the transmit filter input. Application Note AN-28 shows the XR-2121 in a complete modem signal processor.

Several output waveforms have been included to help understand the XR-2121 operation. Figure 6 shows frequency spectrums for FSK for both answer and originate modes. It can be seen to consist of two 300 Hz wide spectrums centered around 1170 Hz and 2125 Hz. Figure 7 and 8 show the higher harmonic contents of the FSK spectrums. These figures show the second harmonic content to be more than 50 dB down from the fundamental. This is very desirable in the originate mode as second harmonics not attenuated by the transmit filter will pass unattenuated through the receive and cause degraded performance.

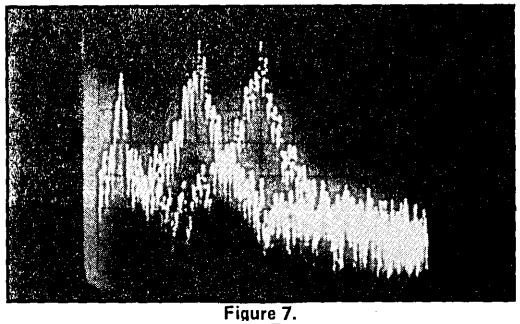


Figure 7.

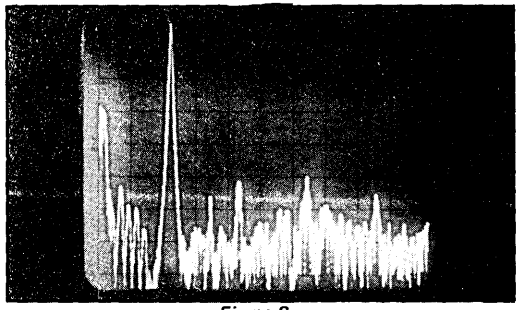


Figure 8.

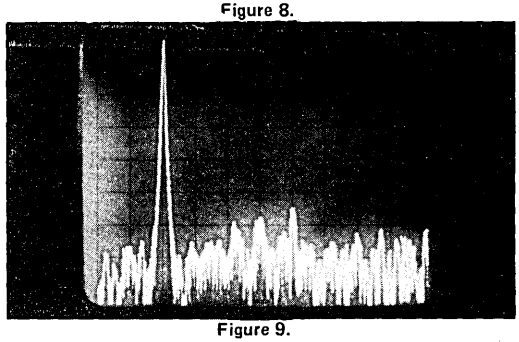


Figure 9.

Figure 9 and 10 show the carrier being enabled and disabled using the $T_{XC\ EN}$ pin (pin 5) for PSK and FSK respectively. It shows about 10 ms necessary for the carrier to be either fully enabled and settled, or disabled. These photos were taken with a transmit filter similar to the XR-2120 at the output of the XR-2121 to produce a clearer picture.

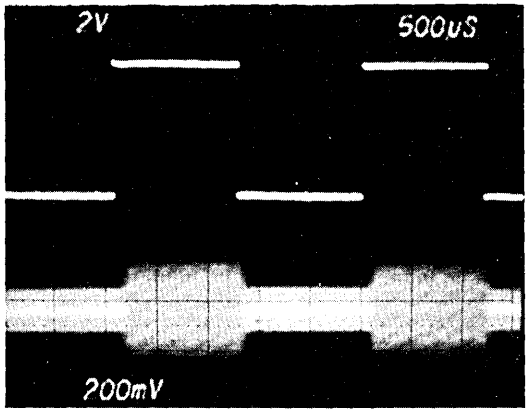


Figure 10.

For further application information on the XR-2121, Application Note AN-28 shows a complete modem signal processor utilizing the XR-2121 with the XR-2120 filter, XR-2122 demodulator, and XR-2125 data buffer.

Bell 212A Handshake

The Bell 212A modem specifications require auto speed selection on auto answer modems. Auto speed selection requires detection and decoding of the Bell 212A handshake protocol. This detection and decoding is automatically performed by the XR-2122, Bell 212A type demodulator. Some additional logic / circuitry is required to perform the handshake properly. This logic / circuitry may be digital, analog, or microprocessor-based.

Figure 12A and 12B illustrates the timing requirements for the Bell 212A handshake.

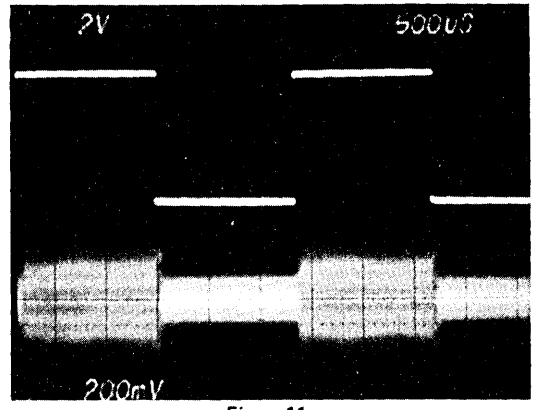
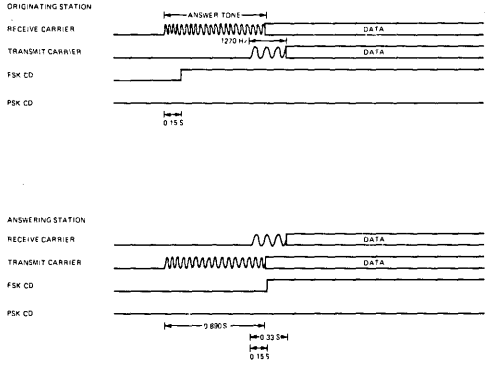


Figure 11.



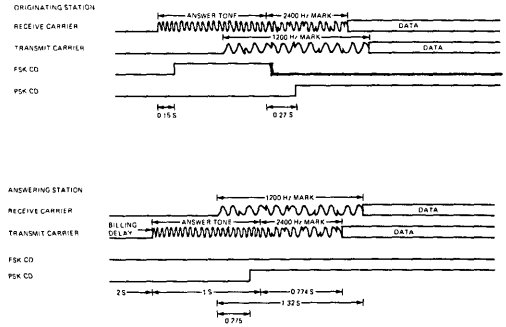


Figure 12A. Figure 12B. V.22 Handshake (with V.25 Auto Answer)

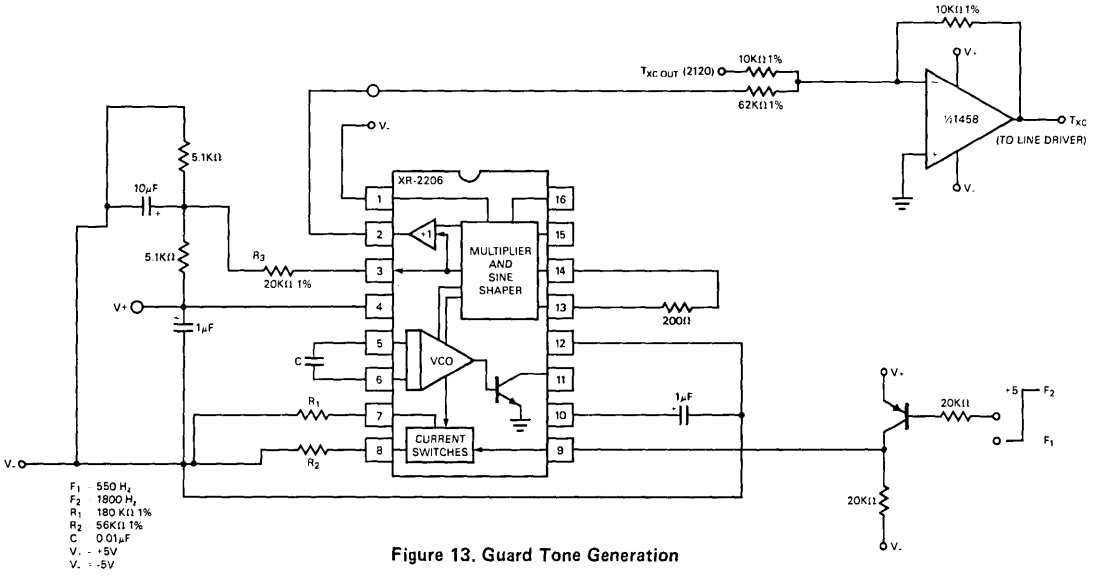


Figure 13. Guard Tone Generation

V.22 Guard Tone Generation

Figure 13 illustrates implementation of the V.22 guard tone generation. V.22 specifies use of the 1800 Hz guard tone in conjunction with the Originate carrier. The 550 Hz guard tone is a national option. Specifications for guard tone generation require the amplitude of the guard tone to be 6 ±1 dBM lower than the transmitted carrier which is typically 9 dBM. The circuit of Figure 13 allows choice of implementation of either guard tone via TTL logic levels: 5 V giving 1800 Hz and 0 V producing 550 Hz. The 20 kΩ resistor to pin 3 sets the voltage at pin 2 to 1.2 V peak. This voltage is then summed and attenuated at the line driver (XR-1458) to give the -16 dBM output required.

Transmit Output Amplifier

To ensure transmit amplitude accuracy for the XR-2121, an external amplifier is recommended. The input to this amplifier should be from pin 3, $T_{XC\ ADJ}$. Figure 14 shows a typical implementation of this transmit amplifier.

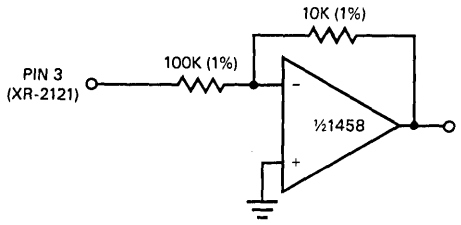


Figure 14. Transmit Carrier Output Amplifier

Bell 212A Type Demodulator

GENERAL DESCRIPTION

The XR-2122 is designed to perform the complete Bell 212A type modem demodulator function. Both 1200 BPS differential phase shift keyed (DPSK) and 300 BPS frequency shift keyed carrier demodulation is performed by the XR-2122. The 1200 BPS portion utilizes coherent demodulation, while the 300 BPS uses phase-locked loop techniques. For 1200 BPS operation, an internal 17 bit descrambler provides the descrambled output with the non-descrambled output also available.

Automatic speed selection is performed by a handshake circuit. Carrier detect outputs are supplied for FSK data, PSK data, and conventional energy detection.

A non-committed operational amplifier is supplied to provide receive carrier sensitivity tailoring. An automatic gain control circuit (AGC) assures wide dynamic input carrier range.

The XR-2122 is constructed using silicon gate CMOS technology. The XR-2122 is designed to operate off of a 1.8432 MHz clock input. Available in a 28 Pin package, the XR-2122 is designed for +5 volt and -5 volt power supplies.

FEATURES

Bell 212A Compatible
1200 BPS DPSK Coherent Demodulation
300 BPS FSK Demodulation
Eye Diagram Output
Internal 17 Bit Descrambler
Non-descrambled Demodulation Output Available
FSK, PSK and Energy-type Carrier Detect Outputs
Automatic Speed Selection
Non-committed Op Amp for Input AGC Amplifier
AGC Input Circuit for Wide Dynamic Range

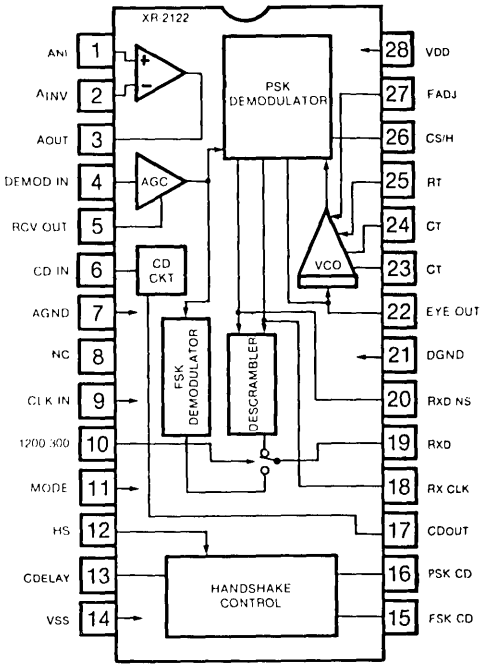
APPLICATIONS

Bell 212A Type Demodulator
Bell 103 Type Demodulator

ABSOLUTE MAXIMUM RATINGS

Power Supply	
V_{DD}	-0.3 to 7 V
V_{SS}	0.3 to -7 V
Input Voltage	V_{SS} -0.3V to V_{DD} +0.3V
DC Input Voltage	±10 mA
Power Dissipation	750 mW
Derate Above 25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2122CN	Ceramic	0°C to 70°C
XR-2122CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

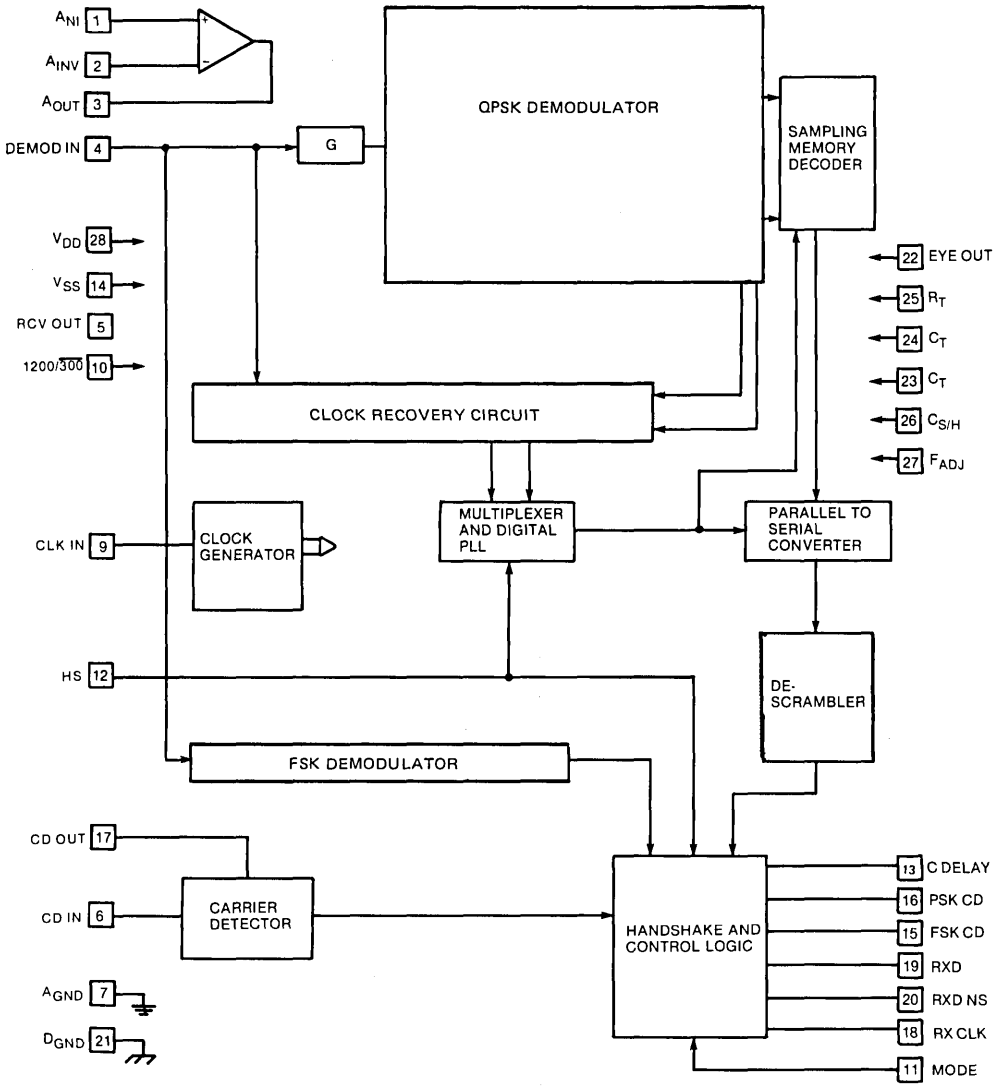
The XR-2122 provides two basic types of operation; demodulation for either 1200 BPS DPSK or 300 BPS FSK encoded incoming carriers. For either speed, the incoming carrier is passed through a gain stage (uncommitted op amp) and an AGC circuit to condition the signal. For 1200 BPS, the signal is processed using coherent demodulation techniques (Costas Loop).

For 300 BPS, a digital phase-locked loop type of demodulator is used providing low bias and jitter distortion without adjustments.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V ± 5%, V_{SS} = -5 V ± 5%, T_A = 0-70°C, CLK IN = 1.8432 MHz ± .01%, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{DD}	Quiescent Positive Supply Current		8	12	mA	Normal Operation
I_{SS}	Quiescent Negative Supply Current		-8	-12	mA	Normal Operation
DIGITAL CHARACTERISTICS						
I_{IN}	Input Current			10	µA	$V_{IN} = V_{DD}$ or GND
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 µA
V_{OL}	Output Loss Voltage		0.4	0.8		I_{OL} = 2 mA
ANALOG CHARACTERISTICS (Circuit Configuration of Figure 11)						
A_{VG}	Amplifier Open Loop Gain		60		dB	
$V_{DEMOD\ IN}$	Typical Input Voltage to DEMOD IN		-6		dBM	
$Z_{DEMOD\ IN}$	DEMOD IN Input Impedance		15		KΩ	
$Z_{CD\ IN}$	CD IN Input Impedance		50		KΩ	
CD ON	CD On Level		-32	-30.5	dBM	
CD OFF	CD Off Level	-35.5	-34		dBM	
$T_{d\ CD}$	CD Off/On Delay Time	10	17	24	ms	
$T_{dlh\ FSK}$	FSK CD Off/On Delay Time	105	150	205	ms	
$T_{dhl\ FSK}$	FSK CD On/Off Delay Time	10	17	24	ms	
$T_{dlh\ PSK}$	PSK CD Off/On Delay Time	200	270	350	ms	C Delay = 0.47 µF
$T_{dhl\ PSK}$	PSK CD On/Off Delay Time	10	17	24	ms	
f_{VCO}	VCO Frequency Answer Mode Originate Mode		 4.8 9.6		 KHz Khz	



EQUIVALENT SCHEMATIC DIAGRAM

PRINCIPLES OF OPERATION

The XR-2122 is designed to perform the complete demodulator function in a Bell 212A type modem system. It has been specifically designed to complement the XR-2120 filter, XR-2121 modulator, and XR-2125 data buffer to form a four chip Bell 212A type modem signal processor. This four chip set is known as the XR-212AS and is covered in depth in Application Note AN-28. This data sheet will deal specifically with the XR-2122 and its functions.

The XR-2122 performs two different types of demodulation; 300 BPS frequency shift keyed (FSK) and 1200 BPS differential phase shift keyed (DPSK) encoded carriers.

First consider the 1200 BPS type of demodulation. For this demodulator operation, the XR-2122 accepts a DPSK encoded carrier (R_{XC}) typically from the telephone switched network, and demodulates it to produce a serial received data output. This serial data stream is synchronous, that is a clock, R_X CLK, is used for synchronization purposes.

The DSPK encoded receive carrier, R_{XC}, is first applied to an automatic gain control circuit, AGC. This circuit, shown in Figure 1, provides a constant voltage output for a wide dynamic range input signal.

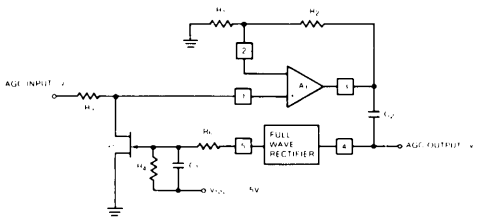


Figure 1. AGC Circuit

Operation of the AGC is as follows. V_O is internally set to about 1.5 volt peak-to-peak. The gain (non-inverting) of A_1 is set by R_2 and R_1, and is R_2/R_1 for $R_2 >> R_1$. With the gain of A_1 set and a constant V_O, the input voltage to A_1's non-inverting input will be a constant voltage: $V_{NI} = (V_O) \div (R_2/R_1)$. FET Q_1 acts as a variable resistor to form a voltage divider with R_3 for the input signal. Q_1's resistance is controlled by the feedback path from A_1's output, through C_2, the full-wave rectifier and filter network R_4-R_5-C_1. The feedback will control the resistance of Q_1 in such a way that the voltage divider action it produces with R_3 will produce the precise voltage at V_{NI} of A_1, which, when multiplied by A_1's gain, will produce the correct V_O. Values are given in the applications section for a typical circuit which will accept an input dynamic range of -40 dBM to 0 dBM.

The output of the AGC, which is really a constant amplitude R_{XC}, is fed to two different circuits. One is for carrier recovery and one for clock recovery. The carrier recovery circuit is a Costas Loop. The error voltage outputs of the Costas Loop are fed to a sampling memory decoder which will produce dibits, or pairs of bits, which are extracted from each R_{XC} phase change. Figures A, B, and C show the eye diagram at the output of the Costas Loop with the receive clock, R_X CLK. The eye diagram is the prime indicator of demodulation quality in a cohert type demodulator. The R_X CLK sets the point where the eye is sampled, which should be at the point of zero intersymbol interference, or, in other words, at the eye's maximum opening. The three photographs were taken at Pin 22, eye out, with a complete modem signal processor utilizing the XR-2121 modulator, XR-2120 filter, and XR-2125 data buffer. The eye opening, or quality of demodulation, changes with different line (telephone) quality. The three photos show the eye and R_X CLK for:

A) Back-to-back operation, or two modems directly tied together, A1 is originate and A2 is answer mode.
B) A 3002, C2 conditioned phone line. B1 is originate and B2 is answer mode.
C) A 3002 C0 unconditioned phone line. C1 is originate and C2 is answer mode.

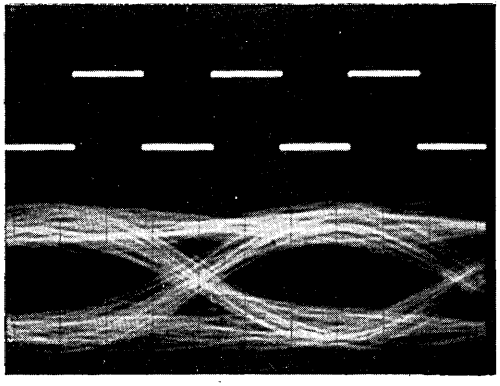


Figure. A1

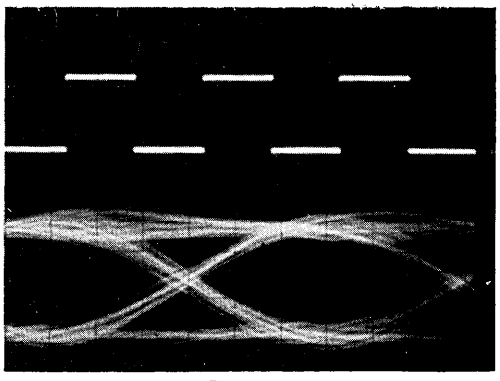


Figure. A2

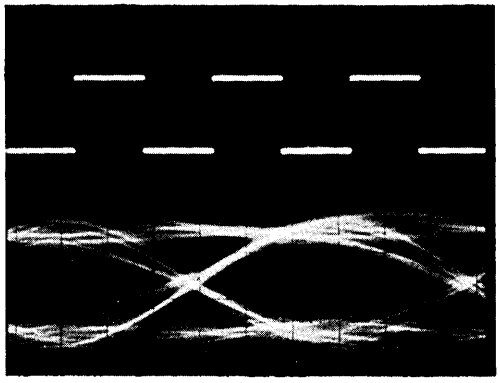


Figure. B1

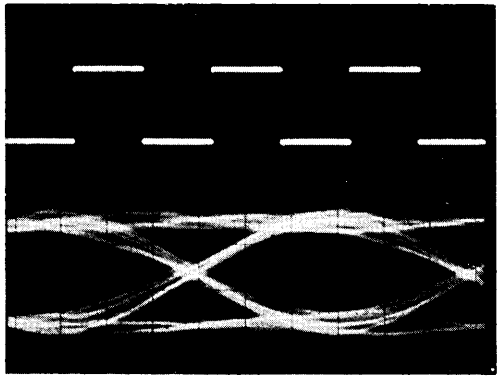


Figure. B2

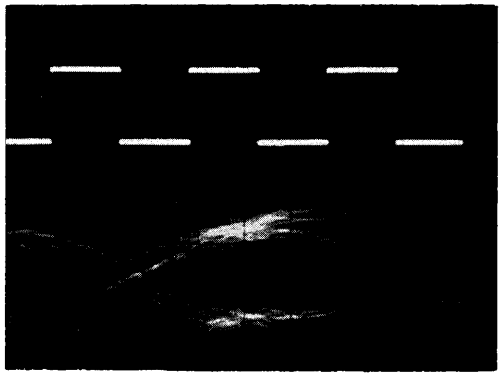


Figure. C1

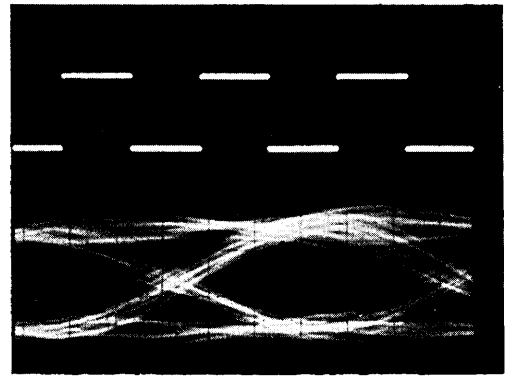


Figure. C2

More information is given on this subject in Application Note AN-28. DPSK encoding introduces a phase shift to a constant frequency carrier every two data bits, or dibits (see XR-2121 modulator data sheet). Table 1 shows the four possible dibits for phase changes of R_{XC}. The XR-2122 conversely produces two data bits for each phase change. The two carrier frequencies are 1200 Hz and 2400 Hz; Table 2 shows the Mode/Frequency convention.

R_X CAR PHASE SHIFT	OUTPUT DIBIT
90°	0 0
0°	0 1
180°	1 0
-90°	1 1

Table 1. Dibit Values for R_{XC} Phase Changes

MODE	RECEIVE CARRIER FREQUENCY
Answer	1200 Hz
Originate	2400 Hz

Table 2. Carrier Frequency Assignments

The mode is controlled by a logic level on pin 10. The dibits are returned to serial form by a parallel to serial converter. Next, the serial data stream is descrambled; the circuitry for this function is shown in Figure 2.

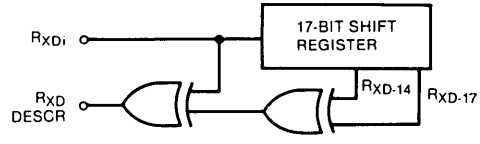


Figure 2. 17 Bit Psuedo Random Descrambler

The descrambler is necessary as all Bell 212A type modems use a scrambled data format for the 1200 BPS speed. This is used to insure that certain data patterns which would cause few, or no phase changes, ever exist. The output of the descrambler can be described by:

$$R_{XD\ DESCR} = R_{XDI}\ (1 \oplus R_{XD\ -14} \oplus R_{XD\ -17})$$

For timing purposes during 1200 BPS operation, a clock must be extracted from the received carrier, R_{XC}. This clock represents a baud period and is 600 Hz. It is used internally for sampling and multiplied by two, 1200 Hz, and output on pin 18, R_X CLK. The timing relationship between R_X CLK and output data, R_{XD}, is shown in Figure 3.

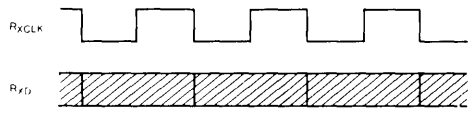


Figure 3. R_{XD}/R_X CLK Relationships

As seen in Figure 3, R_{XD} changes on the falling edge of R_X CLK.

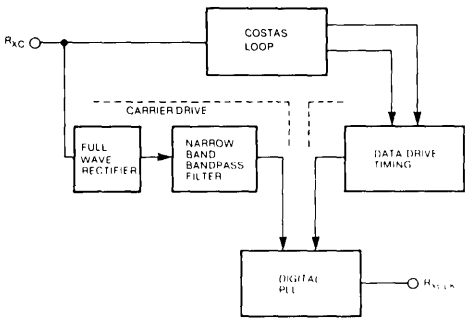


Figure 4. Timing Recovery Circuit

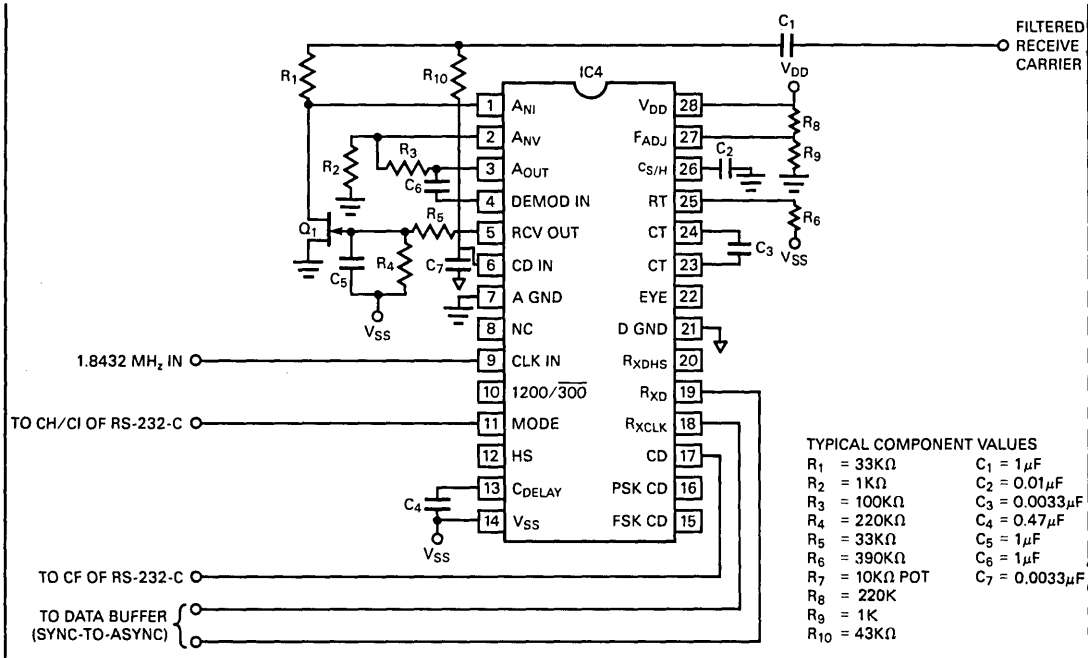
Clock recovery is accomplished from both the received carrier, R_{XC}, and data drive timing. Initially, the clock is recovered from R_{XC} for quick response and then assisted by the Costas Loop for data drive. A digital phase-locked loop, PLL, locks the two types of R_X CLK's together for a more stable clock. This clock is used internally for sampling and timing, and outputted on pin 18, R_X CLK, for sampling use externally.

The demodulation for the 300 BPS operation accepts an FSK encoded carrier and produces an asynchronous serial data output. Since it is asynchronous, no R_X CLK is used. The R_{XC} from the AGC output is fed to a digital phase-locked loop, PLL. The error voltage of the PLL is low pass filtered using switched capacitor filter techniques and compared against a reference voltage to produce the demodulated output.

The output of the two demodulators, FSK and DPSK, are fed into a handshake and control logic section. The primary purpose of this section is to decide whether the incoming carrier, RXC, is FSK or DPSK encoded, or, in other words, which speed the carrier modulation is: 300 BPS or 1200 BPS. This produces an auto speed control circuit. During the initial handshake routine, the XR-2122 will first look for an FSK R_{XC}. It does this by an FSK mark sensor which looks for five consecutive errors. If this condition occurs, operation will automatically be switched to 1200 BPS DPSK. The handshake circuit produces three carrier detect, CD, outputs; an FSK CD (pin 15), PSK CD (pin 16), and an energy level type CD (pin 17) which will respond to all in-band signals.

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	A_{NI}	This is the input op amp non-inverting input. This op amp is typically used in the AGC circuit.
2	A_{INV}	The inverting input of the input op amp.
3	A_{OUT}	The output of the input op amp.
4	DEMOD	The input to both 300 BPS and 1200 BPS demodulators. Also the AGC output.
5	R_{CV} OUT	This pin is used to drive the gate of an external FET used in the AGC circuit.
6	CD IN	The input to the carrier detect circuitry.
7	A_{GND}	Analog ground for the linear circuitry of the XR-2122. This ground should not carry logic current to avoid ground noise.
9	CLK IN	The master clock input, typically 1.8432 MHz ±0.01%.
10	1200/$\overline{300}$	Speed select input for selecting 1200 BPS DPSK or 300 BPS FSK operation.
11	MODE	Mode selection for answer or originate mode.
12	HS	Handshake enable/disable input. The handshake is primarily an auto speed selection circuit with a full description with the text section.
13	C_{DELAY}	Provides carrier detect turn-off and turn-on timing programming.



TYPICAL COMPONENT VALUES

R_1 = 33KΩ	C_1 = 1μF
R_2 = 1KΩ	C_2 = 0.01μF
R_3 = 100KΩ	C_3 = 0.0033μF
R_4 = 220KΩ	C_4 = 0.47μF
R_5 = 33KΩ	C_5 = 1μF
R_6 = 390KΩ	C_6 = 1μF
R_7 = 10KΩ POT	C_7 = 0.0033μF
R_8 = 220K	
R_9 = 1K	
R_{10} = 43KΩ	

FIGURE 11. TYPICAL CONNECTION DIAGRAM

14	V_{SS}	Power supply input for the negative power supply. This supply is -5.0 ± 0.25 volts and should be well by-passed with decoupling capacitors.
15	FSK CD	This is the FSK CD output.
16	PSK CD	Provides the DPSK CD output.
17	CD	The energy-type CD output.
18	R_X CLK	Receive clock output which is a 1200 Hz square wave derived from the incoming DPSK encoded carrier, R_X CLK. Used for external timing of R_{XD}.
19	R_{XD}	Serial receive data output for either 1200 BPS DPSK or 300 BPS FSK.
20	R_{XD} NS	This provides a receive data output before the internal descrambler.
21	D_{GND}	The ground for the digital logic of the XR-2122. This pin should be connected to A_{GND} at the power supply - single point ground.
22	EYE	The Costas Loop eye diagram output is available at this pin.
23/24	C_T	The Costas Loop voltage controlled oscillator, VCO, timing capacitor is connected between these pins.
25	R_T	The Costas Loop VCO timing resistor.
26	$C_{S/H}$	Sample and hold capacitor is connected between this pin and analog ground, A_{GND}.
27	F_{ADJ}	Costas Loop VCO fine tuning input.
28	V_{DD}	Power supply input for the positive supply. This supply is +5.0 ± 0.25 volts and should be well bypased with decoupling capacitors.

CONTROL INPUTS

Table 3 gives logic conditions for the various control inputs of the XR-2122.

PIN	NAME	FUNCTION LOGIC HIGH	LOGIC LOW
10	1200/$\overline{300}$	1200 BPS DPSK Operation	300 BPS FSK Operation
11	MODE	Answer Originate	Originate
12	HS	Handshake Function/Enable	Handshake Function/Disabled

Table 3. Control Input Conditions

APPLICATIONS

The XR-2122 is shown in a typical connection in Figure 11.

In a complete modem system the received carrier, R_{XC}, would come from the receive filter such as the XR-2120. For the XR-2122 it would be either a FSK or DPSK encoded carrier typically from the telephone network. The data output, R_{XD}, would be either a 300 BPS serial bit asynchronous or 1200 BPS serial synchronous data stream. In a full application (AN-28), the R_{XD} output would go through the XR-2125 data buffer. For the 1200 BPS operation, the data buffer will convert the XR-2122 synchronous data into a character asynchronous format with a character length of 9 or 10 bits.

The input signal range of the R_{XC} is -40 dBM to 0 dBM for the AGC values given.

Figure 13 shows R_8 and R_9 replaced by potentiometer P_1.

Potentiometer P_1 adjusts an internal DC offset in the Costas Loop, or 1200 BPS section of the XR-2122. For optimum system performance, it should be adjusted for maximum eye opening at pin 22, EYE OUT (see Figure 12). Figure 13 shows the test set-up for observing the eye output of 1200 BPS and determining the demodulation quality.

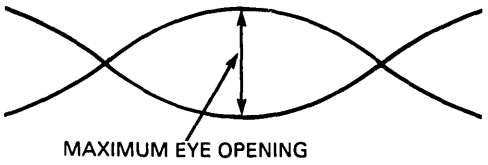


Figure 12. Eye Diagram Characteristics

Further, more complete applications information on the XR-2122 is given in Application Note AN-28 which covers the device used in a complete system.

Bell 212A Handshake Protocol

The XR-2122 performs the sensing for the Bell 212A handshake protocol. With the handshake pin, pin 12, pulled high (+5 V), the XR-2122 will perform energy and sensing and indication, and auto speed adjust. These functions can be utilized to complete the Bell 212A handshake. Timing parameters are illustrated in Figure 14A and 14B.

Since the XR-2122 will change speeds internally, overriding the speed selection pin (pin 10), the designer must provide a means for selecting the required handshake protocol carrier from the modulator, the XR-2121. This selection can be achieved in hardware or software.

3

Addendum:

Handshake:

The handshake pin (HS), pin 12, must be low when the device is first powered up. The reason for this is that at power up, the digital portions of the XR-2122 will reset to an initial state. The HS pin being high will prevent this from occurring. It is best to have the HS pin low for 2 seconds to allow the reset to completely finish.

AGC:

The requirements for the AGC Field Effect Transistor that is tied to pin 1 (A_{N1}) is as follows:

V_{GS} (gate-source cut-off voltage) =
−0.8 V minimum, −4.0 V maximum
$V_{DS(on)}$ (drain-source on voltage =
0.5 V at I_D = 5 mA maximum
$r_{ds(on)}$ (drain-source on resistance) =
60 ohms maximum
BV_{GSS} (gate-source breakdown voltage =
−30 V minimum

The 2N4681 meets these requirements and is used for all demonstrations in EXAR's labs.

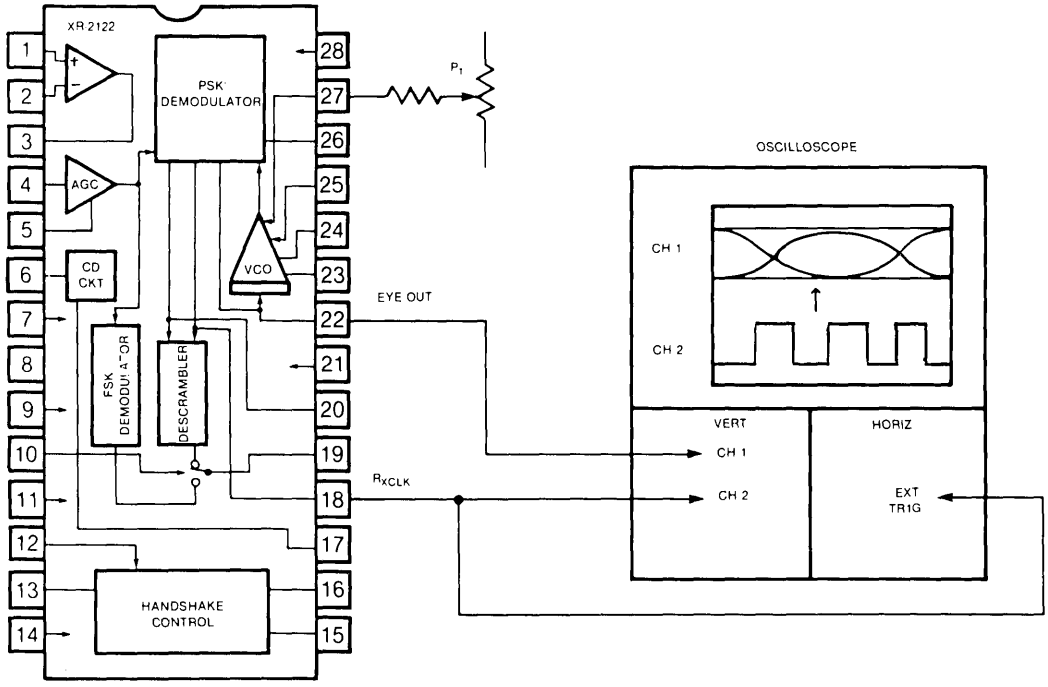


Figure 13. Set-up for Eye Diagram Output

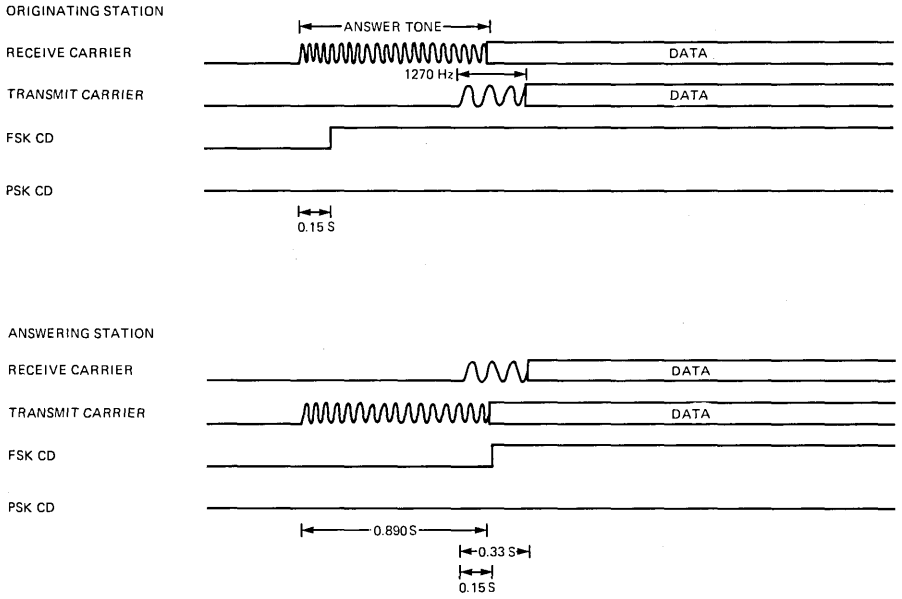


Figure 14A. 212A Handshake 300 BPS

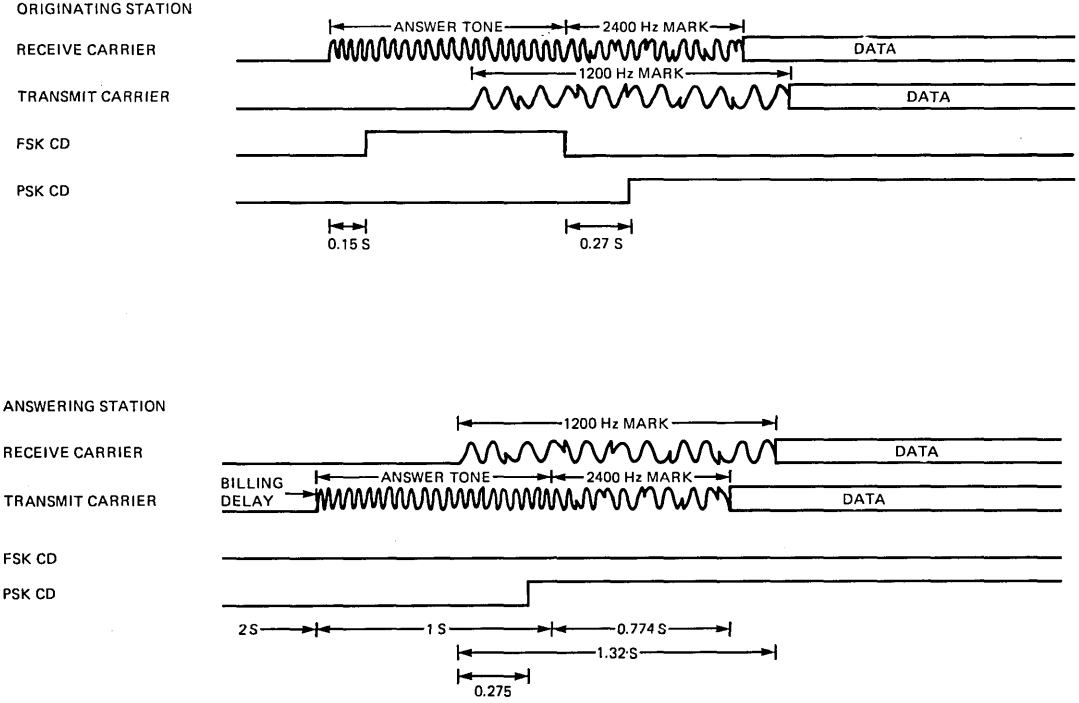


Figure 14B. 212A Handshake 1200 BPS

PSK Modulator/Demodulator

GENERAL DESCRIPTION

This series of devices provide the modulator and demodulator for phase-shifted keyed modulated signals. The devices have an on-chip digital-to-analog converter, allowing digital external programming of Bell 212A, CCITT V.22 or V.26 functions.

The XR-2123 provides the modulator and demodulator functions. It is adequate for Bell 212A (1200 BPS only) and Bell 201 standards. The XR-2123 requires a synchronous-to-asynchronous converter and scrambler-descrambler for the digital portion of the modem for 212A applications. Level shifters and filtering is required for the analog portion.

The XR-2123A provides the ±7 Hz carrier capture range needed for V.22 and V.26. It is externally identical to the XR-2123.

The XR-2123 and XR-2123A utilize CMOS technology for power operation while providing single 5 volt operation. Both devices come in a 28 pin DIL pin package in either plastic or ceramic.

FEATURES

Single +5 Volt Operation
Low Power Consumption (typ. 10 mw)
1200 BPS Full Duplex
2400 BPS Half Duplex
Programmable for US or European Standards (CCITT)
Dibit PSK (DPSK) Operation
Cyrstal Controlled
Synthesized Sine Wave Modulator Output
Adjustable Modulator Output Amplitude
Input Protection

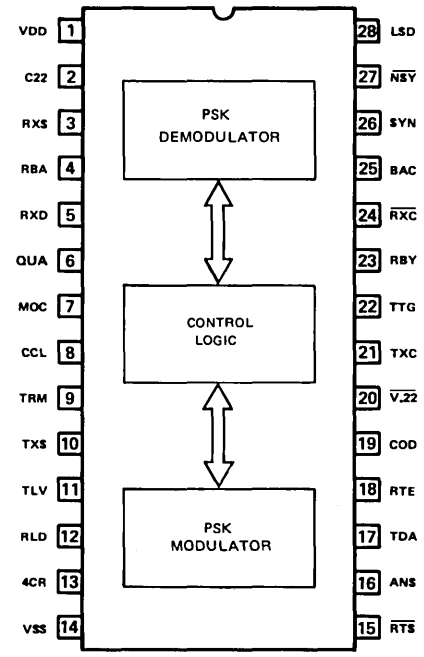
APPLICATIONS

Bell Standard 201 or 212A Modems
CCITT Standard V.22 or V.26 Modems

ABSOLUTE MAXIMUM RATINGS

Power Supply	5.5 V
Power Dissipation	1.0 W
Derate Above 25°C	5 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
All Input Voltage	-0.5 V to (V_{DD} to 0.5 V)
DC Current Into Any Input	± mA

FUNCTIONAL BLOCK DIAGRAMS



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2123CN	Ceramic	0°C to +70°C
XR-2123CP	Plastic	0°C to +70°C
XR-2123ACN	Ceramic	0°C to +70°C
XR-2123ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2123 and XR-2123A provide the complete modulation and demodulation of DPSK modem systems. The modulator transmits a sampled sine wave in dibit phase-shifted keyed format (DPSK). The phase shifts and carrier frequencies are controlled with logic inputs. With these controls, a Bell 212A/CCITT V.22 or a Bell 201/CCITT V.26 can be created.

The XR-2123 and XR-2123A require a separate scrambler/descrambler and synchronous-to-asynchronous converter.

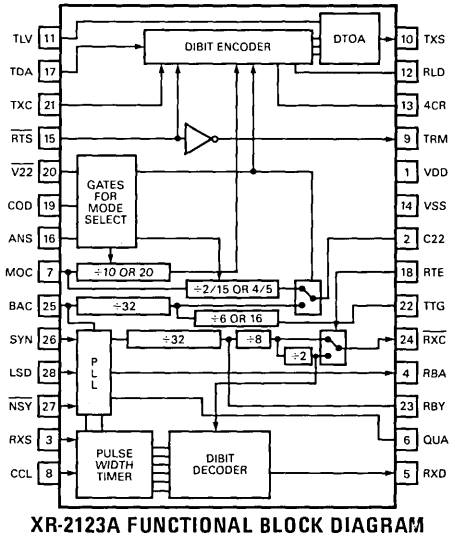
ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5V, V_{SS} = 0V, T_j = 0°C to 70°C

Digital Inputs: RXS, MOC, CCL, $\overline{RTS}$, ANS, TDA, RTE, COD $\overline{V22}$, TXC, BAC, SYN, $\overline{NSY}$, LSD

Digital Outputs: C22, RBA, RXD, QUA, TBA, 4CR, TTG, RBY, $\overline{RXC}$

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 MA
V_{OH}	Output High Voltage	4.6			V	I_{OH} = 1.0 MA
V_{IL}	Input Low Voltage	-0.5		11	V	
V_{IH}	Input High Voltage	3.5		5	V	
I_{IL}	Input Leakage Current				pA	
I_{DD}	Power Supply Current		2.5	4	MA	
C_I	Input Capacitance					
t_R	Low to High Logic Transition Time		20		nS	C_L = 10 pF
t_F	High to Low Logic Transition Time		20		nS	C_L = 10 pF
V_{TXS}	Transmitted Carrier Signal Level		-9		dBm	$V_{PIN\ 11}$ = 1 V



XR-2123A FUNCTIONAL BLOCK DIAGRAM

THEORY OF OPERATION

A system using a XR-2123 or XR-2123A would require both additional analog and digital circuitry. The digital circuitry required for the XR-2123, XR-2123A is a scrambler/descrambler which is a pseudo-random pattern generator. Figure 1 showns a hardware approach of doing the scrambler/descrambler. If the modem is intended to be operated asynchronously, a synchronous-to-asynchronous converter is needed. With the XR-2123 or XR-2123A the XR-2125 can be used. If additional features are desired, a microprocessor can be used to implement both the scrambler/descrambler and the synchronous-to-asynchronous converter.

A counter circuit is needed to provide the baud clock (BAC), which needs to be synchronized with the 4.608 MHz master clock (MOC).

The analog portion of the modem circuit consists of two parts, the bit carrier recovery and the baud carrier recovery. The bit carrier occurs at either 1200 or 2400 Hz. A modem filter, such as the XR-2120, can be used to remove out-of-band signals. The signal is passed through an automatic gain control (AGC), and then through a level shifter. The signal from the level shifter is applied to Pin 3 of the XR-2123 or XR-2123A (RXS).

The baud carrier recovery is similar. After the AGC, the signal is applied to a precision full wave rectifier. The baud rate is always 600 Hz for Bell 212A (1200 BPS) or V.22. By rectifying the signal, the 600 Hz carrier appears as an amplitude modulation. After the rectifier, the signal is applied to a 600 Hz bandpass filter with an approximate Q of 20. The phase shift through this portion is very important. It must be -180° of phase shift from input to output. This is to place the baud clock in the correct reference with the recovered bit carrier. This signal is then level-shifted and applied to Pin 26, SYN. Figure 2 shows the signals after the XR-2120 after the full wave precision rectifier, after the 600 Hz bandpass filter, and after the level-shifter.

Bell 201/CCITT standard V.26 implementation with the XR-2123A requires an additonal filter and a mixer stage in the analog portion. V.26/201 is a synchronous data transmission and does not require a synchronous-to-asynchronous converter. A scrambler/descrambler is also not required, making the digital portion of the modem circuit very simple. A counter circuit to divide down the 4.608 MHz clock (MOC) for the baud clock (BAC) is the only digital circuit needed.

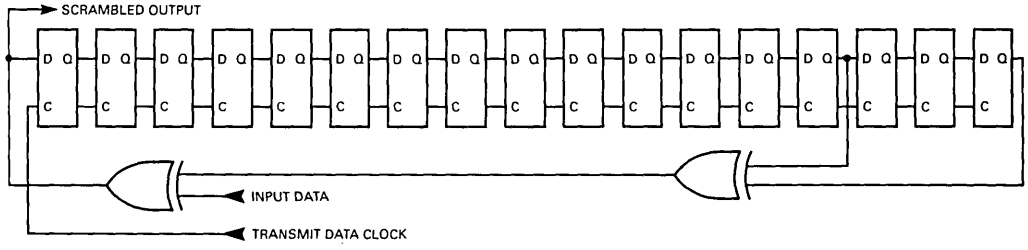


Figure 1A. Scrambler

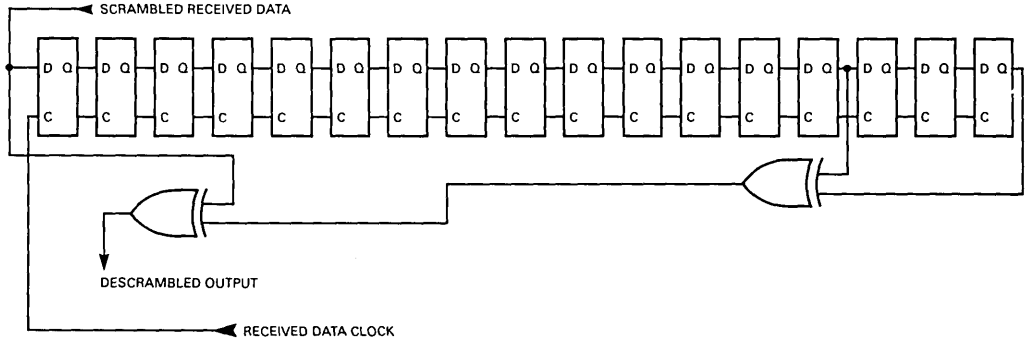


Figure 1B. Descrambler

The receive portion of the analog circuit will be discussed first. The received signal is filtered through an 1800 Hz bandpass filter with −3 dB points at 760 and 2860 Hz. This can be constructed with discrete components or with a programmable filter. After the filter, the signal is passed through an automatic gain control (AGC), A mixer is then used to bring the 1800 Hz received signal up to 9 kHz. This signal is filered through a 9 kHz bandpass filter. This filter should have a Q of approximately 9. The signal is limited and applied to Pin 3, RXS.

The baud carrier can be seen as a amplitude modulation on the 9 kHz signal. This is filtered off using a 1200 Hz bandpass filter. The Q of this filter should be approximately 2. The phase shift through this filter is very important. At 1200 Hz, the phase of the output referenced to the input should be −90°. After the 1200 Hz bandpass filter, the signal is applied to a level shifter and applied to Pin 26, SYN.

Figure 3 shows the signal after the mixer, after the 9000 Hz filter and after the 1200 Hz filter. Figure 4 shows one method of utilizing the XR-2123A for a V.26/ 201 modem. To create the optional 75 baud reverse direction, the XR-2206 and XR-2211 can be used.

The transmit output, Pin 10, of the XR-2123A or XR-2124 requires a low pass filter with a −3 dB point of 3500 Hz. Either the XR-1008 low pass filter or a discrete component filter can be used.

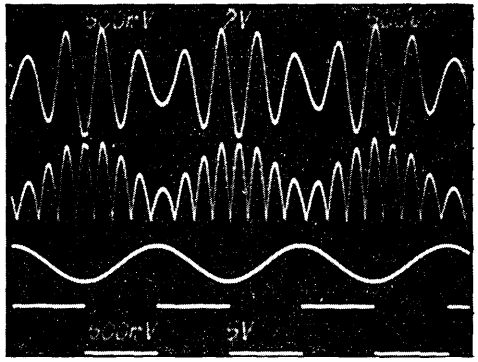


Figure 2. Showing received signal after the XR-2120, after full wave precision recitifier, after the 600 Hz bandpass filter, and after the level shifter.

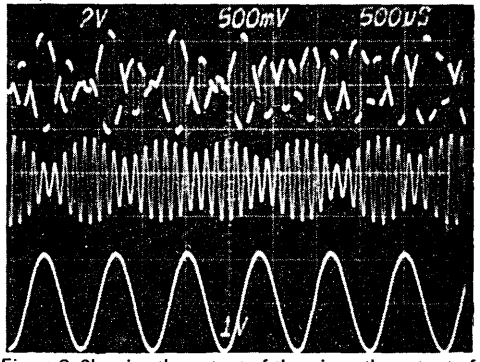


Figure 3. Showing the output of the mixer, the output of the 9000 Hz filter, and the output of the 1200 Hz bandpass filter (baud clock recovery).

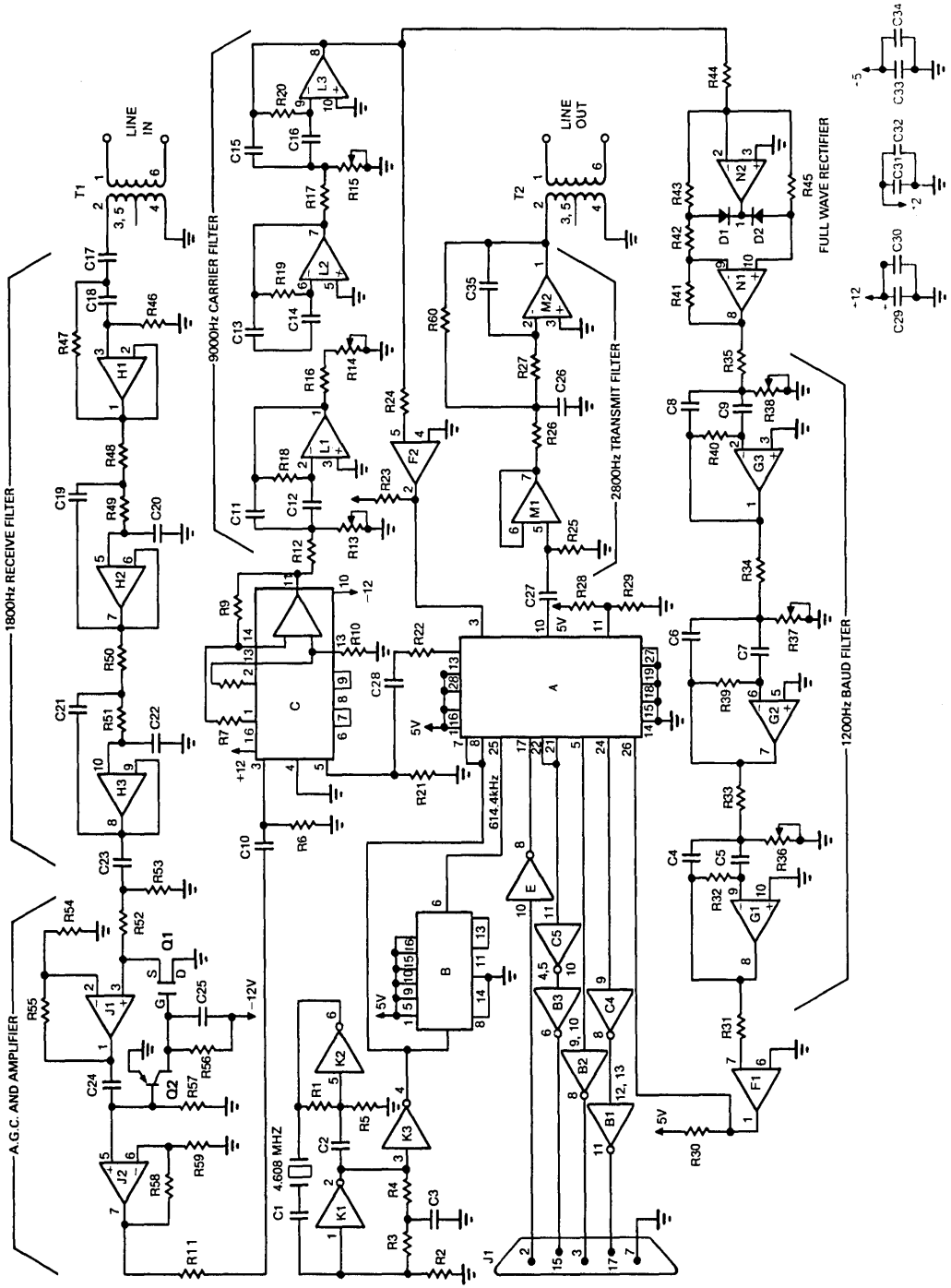


Figure 4. CCITT V.26 2400 BPS Modem Application Schematic

INTEGRATED CIRCUITS

A	XR-2123	EXAR
B	XR-1488	EXAR
C	XR-2208	EXAR
D	DM-74193	National
E	XR-1489	EXAR
F	LM-339-N	Texas Instruments
G	XR-4741	EXAR
H	XR-4741	EXAR
J	XR-1458	EXAR
K	F-7404	Fairchild
L	XR-4741	EXAR
M	XR-1458	EXAR
N	XR-4741	EXAR

CAPACITORS

C1	82 pf	C19	.01 μf
C2	.0022 μf	C20	.001 μf
C3	.033 μf	C21	.01 μf
C4	033 μf	C22	100 pf
C5	.033 μf	C23	2.2 μf
C6	.033 μf	C24	2 μf
C7	.033 μf	C25	10 μf
C8	.033 μf	C26	.033 μf
C9	.033 μf	C27	1 μf
C10	.1 μf	C28	.1 μ
C11	.0033 μf	C29	4.7 μf
C12	.0033 μf	C30	.1 μf
C13	.0033 μf	C31	4.7 μf
C14	.0033 μf	C32	.1 μf
C15	.0033 μf	C33	4.7 μf
C16	.0033 μf	C34	.1 μf
C17	.1 μf	C35	.0068 μf
C18	.1 μf		

RESISTORS

R1	1.2K	R21	2K	R41	10K
R2	2.2K	R22	100K	R42	10K
R3	2.2K	R23	10K	R43	10K
R4	2.2K	R24	10K	R44	10K
R5	2.2K	R25	1M	R45	10K
R6	2K	R26	3.32K	R46	5.76K
R7	24K	R27	2.2K	R47	2.74K
R8	24K	R28	1K	R48	2.61K
R9	50K	R29	1K	R49	75K
R10	50K	R30	10K	R50	7.87K
R11	200K	R31	10K	R51	249K
R12	43.2K	R32	82.2K	R52	120K
R13	1K POT	R33	29.1K	R53	10K
R14	1K POT	R34	29.1K	R54	1K
R15	1K POT	R35	29.1K	R55	68K
R16	43.2K	R36	500Ω POT	R56	1M
R17	43.2K	R37	500Ω POT	R57	10K
R18	109K	R38	500Ω POT	R58	4.7K
R19	109K	R39	82.2K	R59	1K
R20	109K	R40	82.2K	R60	6.8K

TRANSISTORS

Q1	2N4861	Q2	2N4403

TRANSFORMERS

T1	T2220
T2	T2220

DIODES

D1	IN914
D2	IN914

CONNECTOR

J1	RS232

Figure 4A. V.26 2400 BPS Modem System Components List

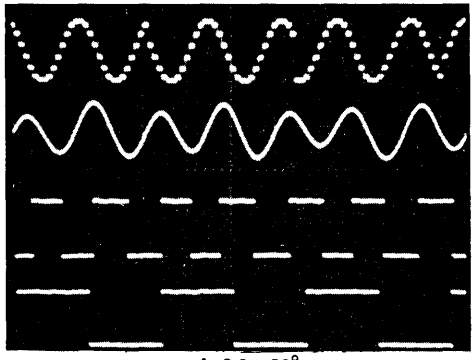
Modulation

The data to be modulated is applied to Pin 17, TDA. This must be synchronized to the transmitter bit timing clock, Pin 22, TTG. This internally creates a dibit signal which then selects the amount of phase shift needed to be encoded properly. This is coherent phase modulation which means the only phase reference is the phase of the signal before the transition.

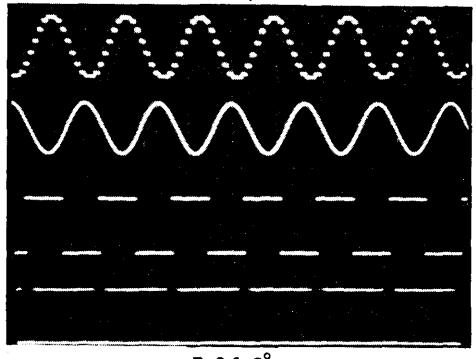
To encode the data, a counter, which accesses the digital-to-analog converter, is preset to a particular point depending on the phase change needed. Figure 5 shows four possible phase shifts with the four bit patters (00, 01, 10, 11) and the ouput of the XR-2120 filter. It should be noted that the baud rate stays at 600 Hz whether in originate (2400 Hz carrier) or in answer mode (1200 Hz data carrier).

The amplitude of the transmitted signal is controlled by the TLV, transmitter level, Pin 11. This is a DC input, typically set for 0.8 VDC. The input draws approximately 15 μA, and can be controlled with a resistor divider or a digital-to-analog converter for adapting to poor lines. Figure 6 shows the relationship between V_{TLV} and V_{TXS}.

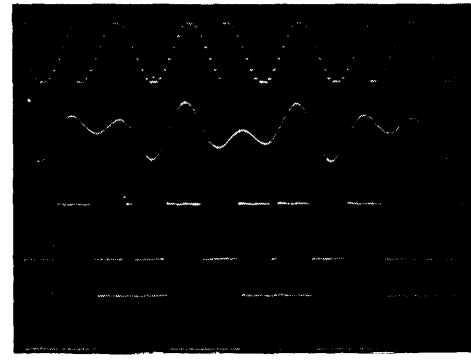
Figure 5. TXS, Transmit Output Output of 2120, Output of Limiter Recovered Baud Clock



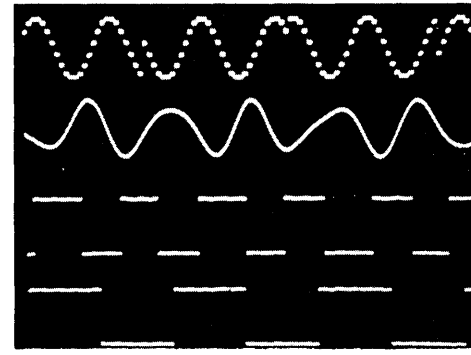
A. 0 0; +90°



B. 0 1; 0°



C. 1 0; 180°



D. 1 1; 270°

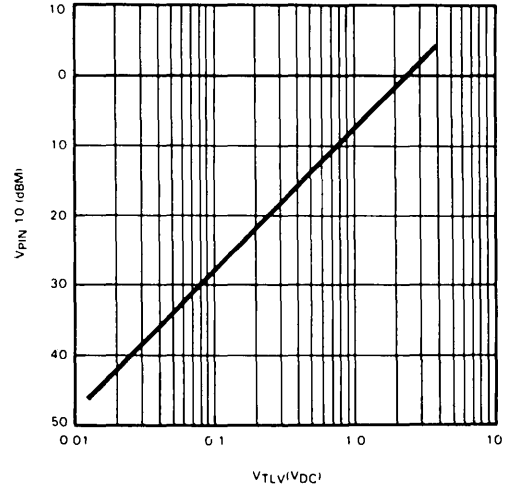


Figure 6. TXS vs. VTLV

Demodulation

The demodulator uses a pulse width measuring technique which compares the pattern received on RXS within the window set by the baud clock, applied to the synchronizer pin, SYN This is a coherent demodulation technique, so no reference phase is needed. The carrier clock, CCL, is used to time the widths of the received pulses. As it was shown in Figure 5, the phase changes produce a distinctive pulse pattern. The clock frequency applied to the carrier clock pin, CCL, is changed for each carrier frequency used. The greater the carrier frequency, the greater the carrier clock frequency.

The V.26 demodulation is the same internally. With a 1800 Hz bit carrier and a 1200 Hz phase carrier, only 1½ cycles of the 1800 Hz carrier exist within the window created by the baud clock. This does not provide enough pulses to provide an accurate measurement. Also, the baud clock is not easily recovered with the received waveform. When the received signal is mixed up to 9000 Hz, the phase carrier appears as an amplitude modulation. This can be easily detected with the full wave precision rectifier and a 1200 Hz bandpass filter.

The quality pin, Pin 6, on the XR-2123A is error jitter of the phase-lock loop. It is latched so that it remains high a minimum of approximately 1 ms. This can be used as an indication of the quality of the line in use. If the quality pin is high often, the possibility of errors is greater.

The received bit timing clock is used to synchronize the data at Pin 5, RXD. This clock is found on Pin 24, RXC. Figure 7 shows the relationship between $\overline{RXC}$ and RXD. If the XR-2125 was used, $\overline{RXC}$ is tied to Pin 9, RXC IN, and RXD is tied to RXD IN, Pin 10.

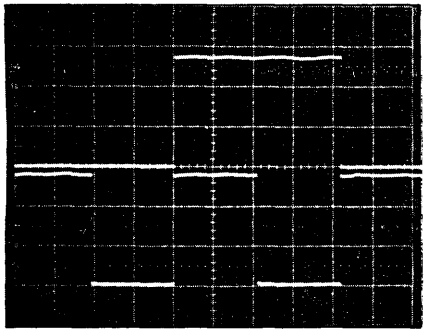


Figure 7. Top Trace RXD, Bottom Trace $\overline{RXC}$

PIN DESCRIPTIONS

Pin	Name	Description
1	VDD	+5 V_{DC} ±0.25 V
2	C22	Carrier clock for Bell 212/V.22. This output clock is used by the demodulator for timing the pulse widths of the received signal. When in the originate mode, the frequency of the pin is 614.4 kHz. When the XR-2123 or XR-2123A is set in the answer mode, the frequency at this pin is 1.2288. This allows the counter circuit in the demodulator to arrive at the same total count for a given baud rate. This pin is controlled by V.22, ANS, and COD pins on the device as shown.

	V.22	ANS	COD	C.22
1200 Hz	0	1	1	1.2288 MHz
2400 Hz	0	1	0	0.6144 MHz
See Select Mode	1	X	X	9600 Hz Mode

When V.22 is high, C.22 produces a 9600 Hz clock. This clock is not normally used for V.26 and is NOT applied to Pin 8, CCL.

3	TXS	Received signal input. This is the received signal input after level shifting (0-5 V). This signal carries the bit data.
4	RBA	Received baud timing. This output provides a clock at the baud rate chosen. For V.22 and Bell 212, it is at 600 Hz. For V.26, it is at 1200 Hz. It is derived from BAC and also phase locked to the signal applied to Pin 26, SYN.
5	RXD	Received data. This output is the demodulated data from the signals applied to pins 3 and 26 (RXS and SYN respectively).

6 2123/A	QUA	The quality of demodulation. This pin shows the amount of error in the timing relationship between SYN and RBA. If the recovered baud carrier has too much noise, this pin will be high for a minimum of approximtely 1 ms. Please read the demodulation section of this data sheet for more detail.
7	MOC	Modulator clock input. This is the master clock. For V.22, Bell 212A and V.26, this clock is 4.608 MHz.
8	CCL	Carrier clock. This input is for the clock which measures the time that RXS, Pin 3, is high within one window. This input is always 512 times the received bit carrier. For example if f_{RXS} = 1200 Hz f_{CCL} = 614.4 kHz f_{RXS} = 2400 Hz f_{CCL} = 1.228 MHz f_{RXS} = 9000 Hz f_{CCL} = 4.608 MHz For V.22 and Bell 212 applications, CCL is applied from the output C.22, Pin 2, of the device. When V.26 is needed, CCL is tied to the master clock, Pin 7. The received frequency of 9000 Hz for V.26 is explained in the demodulation section.
9	TRM	Transmit mode. This output indicates the state of the modulator. When high, the device is transmitting. When low, carrier output is clamped. It is controlled by Pin 15, $\overline{RTS}$. When $\overline{RTS}$ is low, TRM is high. When $\overline{RTS}$ is high, TRM is low.
10	TXS	Transmitted signal. This is the output of the internal digital-to-analog converter. The modulated 8-level sine wave can be seen at this pin. This output is usually applied to the XR-2120 modem filter.
11	TLV	Transmitter level. This input controls the amplitude of the transmitter output, Pin 10. It typically draws approximately 15 μA and can be adjusted using a resistor divider circuit. Although not critical, this input should be relatively free of any AC component since it will cause an amplitude modulation of the TXS output.
12	RLD	Received data. This tells the terminal that the data to be transmitted has been received by the modem. It is at the baud rate of the mode the device is set in. It is counted down from BAC, Pin 25. When RLD goes high, this marks the end of the dibit set.

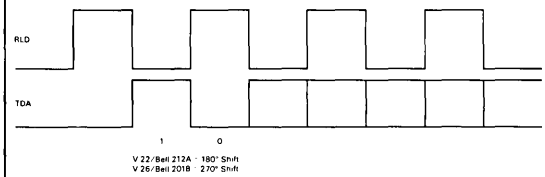


Figure 8. RLD Timing

13	4CR	Four times the carrier frequency. This output is used for the V.26 mixer in the demodulator circuit. For V.22 and Bell 212A it is not used.
14	V_{SS}	Ground.
15	$\overline{RTS}$	Request to send. This input controls the transmitter output and the TRM, transmit mode output. The following chart describes the possibilities:

RTS	TRM	TXS
0	1	carrier
1	0	clamped to DC level

16	ANS	Answer tone. This input controls the frequency of the transmitter output. It is used along with $\overline{V.22}$ and COD. The details about using this pin is found under those two pins.
17	TDA	Transmitted data. This input is where data to be transmitted is applied. It should be synchronized to the transmit clock, Pin 22, TTG. By comparing the data applied to this pin and Pin 12, RLD, the various phase shifts can be predicted for troubleshooting purposes.

18 RTE — Rate. Control $\overline{RXC}$, Pin 24, and Pin 22, TTG. When set at a logic 1 level, the frequency at the two outputs is twice what is normally seen there. The block diagram shows the dividers controlled by RTE.

19 COD
20 $\overline{V22}$ V.22 mode
ANS answer tone — Code. These three inputs determine the mode of the modulator and demodulator of the device. Also, with these pins the 2100 Hz tone for handshaking can be created. The following truth table applies to these pins:

$\overline{V.22}$	ANS	COD	APPLICATION
0	0	0	Transmit and receive at 2400 Hz (high ch.) This is for analog loop back.
0	0	1	Transmit and receive at 1200 Hz (low ch.) This is for analog loop back.
0	1	0	Transmit at 2400 Hz (high ch.) Receive at 1200 Hz (low ch.)
0	1	1	Transmit at 1200 Hz (low ch.) Receive at 2400 Hz (high ch.)
1	0	0	Answer Tone at
1	0	1	2100 Hz.
1	1	0	V.26 mode Phase shifts have an initial 90° skew.
1	1	1	V.26 mode Phase shifts have an initial 45° skew.

21 TXC — Transmitter bit timing. This input is usually tied to Pin 22, TTG, timing for transmitter. For V.22/Bell 212A (1200 BPS), the frequency at Pin 21 is 1200 Hz. For V.26, the frequency is 2400 Hz. Note: this assumes that Pin 18, RTE, is low in both cases.

22 TTG — Timing for transmitter. This output is applied to pin 21 for all standard uses (V.22, Bell 212A, Bell 201, and V.26). It is counted down from BAC clock input. Please read the descriptions for TXC and RTE for details.

23 RBY — Received byte timing. This output is a square wave at a frequency 16 times the received baud timing. It is not normally used.

24 $\overline{RXC}$ — Received bit timing. This output is synchronized to the recovered baud carrier. It is usually used to perform the asynchronous-to-synchronous conversion.

25 BAC — Baud clock. This input is used to create the modulation and demodulation baud clock. Internal countdown circuitry sets the baud rate at either 600 Hz or 1200 Hz. For V.22/Bell 212A operation, a 307.2 kHz clock is applied to BAC. For V.26 operation, a 614.4 kHz clock is applied.

26 SYN — Synchronization. This input is where the recovered baud carrier is applied. This clock is internally applied to a phase lock loop which has BAC as the local oscillator. The error voltage is shown as the difference between $\overline{RXC}$ and RBA. This error output can be found on the quality pin, QUA, Pin 6.

27 $\overline{NSY}$ — New synchronization. This input will force the received data output to a high state. The synchronization takes place when the $\overline{NSY}$ pin is changed from high to low.

28 LSD — Line signal detector. When high, the receiver is operating normally. When this input is low, the receiver is clamped. This can be tied through an inverter to the signal applied to the $\overline{NSY}$ input.

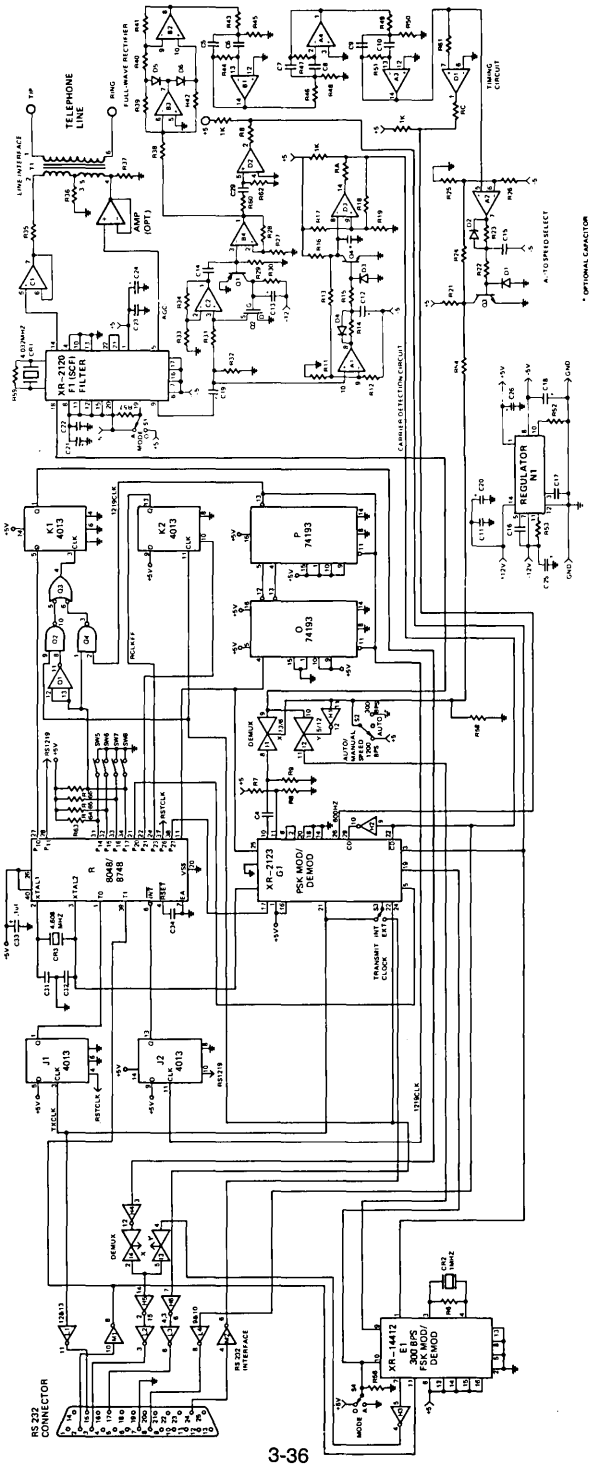


Figure 9. Bell 212A Modem Application Schematic

Data Buffer

GENERAL DESCRIPTION

The XR-2125 is a logic circuit designed to perform the data buffer function for Bell 212A Type Modem Systems. Both asynchronous to synchronous and synchronous to asynchronous conversion are performed at nominal data rates of 1200 bits per second. The XR-2125 is selectable for character lengths of 9 or 10 bits. Separate enable/disable inputs are supplied for async to sync and sync to async converter sections. These inputs allow the same data lines to be used for asynchronous or synchronous operation.

The receive data buffer section (sync to async) accepts input sync data (typically from the modem demodulator) at 1200 BPS and converts it to a 1219 BPS async data format. The transmit data buffer (async to sync) accepts input async format data with a data rate of 1200 BPS +1%, -2.5% and it is synchronized to 1200 BPS, which is typically sent to the modulator. This section also provides break signal automatic extension.

The XR-2125 is constructed using silicon gate CMOS technology for low power operation. Operation is designed for an input clock frequency of 1.8432 mHz. The XR-2125, available in a 14 Pin package, is designed for single 5 volt operation.

FEATURES

Bell 212A Compatible
Asynchronous to Synchronous Conversion
Synchronous to Asynchronous Conversion
Independent Disable Input for
  Receiver and Transmitter Sections
1.8432 MHz Clock
Break Signal Automatic Extension for Transmitter
1200 BPS +1%, -2.5% Operation
Single 5 Volt Operation

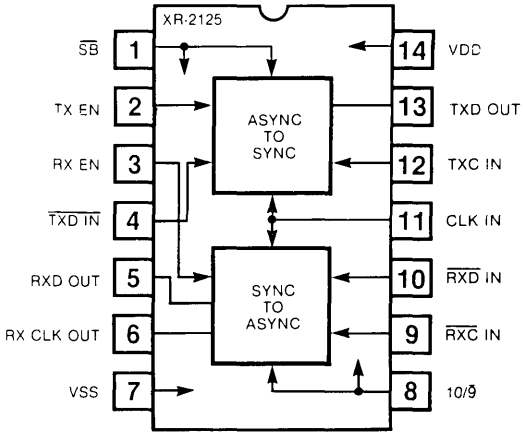
APPLICATIONS

Bell 212A Data Buffer

ABSOLUTE MAXIMUM RATINGS

Power Supply	-0.3 to +7.0 V
Input Voltage	-0.3 to V_{DD} +0.3
DC Input Current (any input)	±10 mA
Power Dissipation	250 mW
Storage Temperature Range	-65°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2125CN	Ceramic	0°C to 70°C
XR-2125CP	Plastic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2125 provides the complete interface between synchronous and character - asynchronous data systems. The synchronous side consists of two data lines, T_{XD} and R_{XD}, each with their respective clocks, T_{XC} and R_{XC}. The synchronous portion is designed for data rates of 1200 ± .01% BPS. The asynchronous side handles data oriented in characters where the actual data bits are bracketed by a start and stop bit. Character lengths are 9 or 10 bit (7 or 8 data bits), pin selectable.

To perform this interface, the XR-2125 consists of two main sections: synchronous to asynchronous (receive section) converter to reinsert stop bits deleted by the sending modem. The other section is the a synchronous to synchronous converter (transmit section) to add or delete stop bits to correct the transmit data rate to 1200 BPS. This section also extends the break signal to two character lengths plus three bits when it comes in at a shorter period.

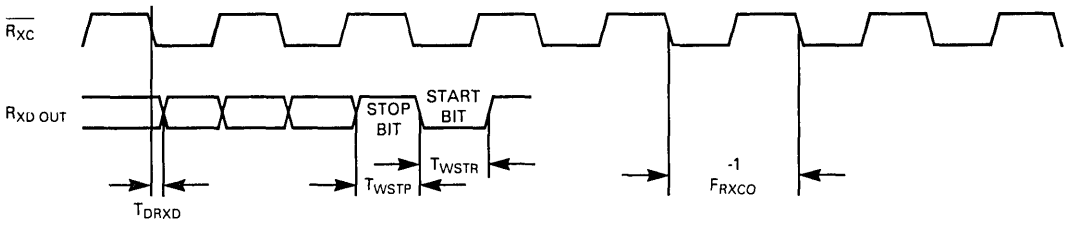
A standby mode is included to put the XR-2125 in a low supply current, non-operative, mode on command.

ELECTRICAL CHARACTERISTICS

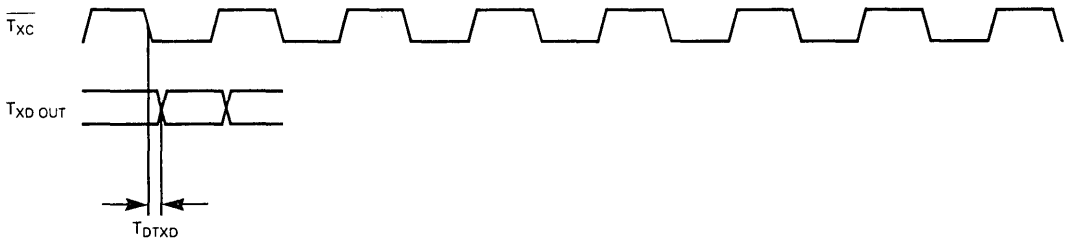
Test Conditions: V_{DD} = 5 V ± 5%, T_A = 0-70°C, CLK IN = 1.8432 MHz ±0.01%, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
DC CHARACTERISTICS						
V_{OL}	Output Low Voltage		0.05	0.8	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OM} = −400 µA
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.4			V	
I_{OL}	Output Low Current		2		mA	
I_{OH}	Output High Current			−400	µA	
I_{IN}	Input Current			±10	µA	V_{IN} = 0 - V_{DD}
I_{DD}	Supply Current Quiesent		100	250	µA	
I_{DD}	Supply Current Standby			10	µA	
AC CHARACTERISTICS: $f_{TXC\ IN}$ = 1200 ±0.01% Hz, $f_{RXC\ IN}$ = 1200 ±0.01% Hz.						
t_{wstr}	Start Bit Width		820		µs	
t_{wstp}	Stop Bit Width 9 Bit Character 10 Bit Character		 938 951		 µs µs	 Reinserted Stop Bits and (n) (820 µs) long
f_{txd}	TXD in Bit Rate	1170	1200	1212	BPS	
t_{dtxd}	TXD Out Delay Time			200	ns	C_L = 50 pf; 10/$\overline{9}$ = Hi
t_{drxd}	RXD Out Delay Time			200	ns	10/9 = Hi
f_{rxco}	RXC Out Frequency		1219		Hz	

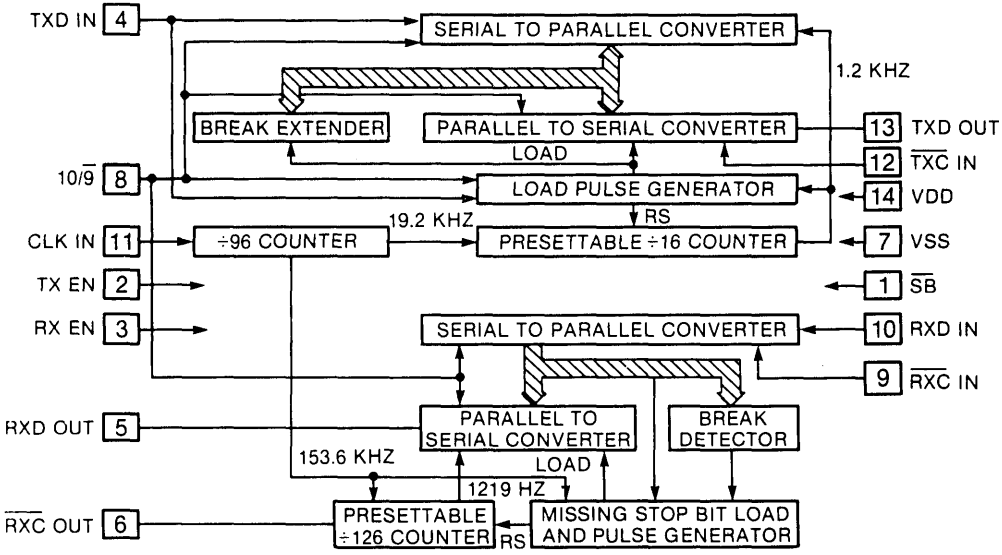
RECEIVE TIMING



TRANSMIT TIMING



TRANSMIT AND RECEIVE TIMING CHARACTERISTICS



EQUIVALENT SCHEMATIC DIAGRAM

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	$\overline{SB}$	This pin places the XR-2125 in a non-operative, low quiesent current mode.
2	T_{XEN}	An enable input for the transmitter section (async to sync). When enabled, async to sync conversion is performed on $T_{XD\ IN}$. When disabled, the data on $T_{XD\ OUT}$ will be identical to that of $T_{XD\ IN}$ (flow through mode) In Bell 212A type modem applications the sync to async will be disabled for 300 BPS FSK operation and for 1200 BPS synchronous operation.
3	$R_{X\ EN}$	An enable input for the receiver section (sync to async). When enabled, sync to async conversion is performed on $R_{XD\ IN}$. When disabled, the data on $R_{X\ OUT}$ will be identical to that of $R_{XD\ IN}$ (flow through mode). In Bell 212A type modem applications the sync to async will be disabled for 300 BPS FSK operation and for 1200 BPS synchronous operation.
4	$T_{XD\ IN}$	The transmitter data input. This is a serial data stream with a data rate of 1200 BPS +1%/-2.5% (T_{X} EN active).
5	$R_{XD\ OUT}$	The asynchronous serial data out-from the sync to async converter (R_{X} EN active). The data rate of this signal is 1219 BPS.
6	$R_{X\ CLK\ OUT}$	Received clock output.
7	V_{SS}	Ground pin.
8	$10/\overline{9}$	Asynchronous character length selection input. Ten bit (start bit, 8 data bits and a stop bit) or nine bit (7 data bits) can be selected.
9	$\overline{RXC}$ IN	The receive clock input, which typically is supplied by the demodulator (XR-2122). The frequency should be 1200 Hz ± 0.01%.
10	$\overline{RXD}$ IN	The synchronous serial data input which is typicall from the demodulator data output (R_{XD} of the XR-2122). The data rate of this signal is 1200 BPS ± 0.01%.
11	CLK IN	Master clock input of 1.8432 Hz ± 0.01%.
12	$\overline{TXC}$ IN	The transmit clock input which is typically supplied by the modulator (XR-2121). The frequency should be 1200 Hz ± 0.01%.
13	$\overline{TXD}$ OUT	The synchronous serial data output which typically goes to the modulator input (XR-2121). The data rate of this signal is 1200 BPS ± 0.01%.
14	V_{DD}	This pin provides the input for the positive power supply which should be +5 ± 0.25 volts.

CONTROL INPUTS

Table 1 gives the logic conditions for the various control inputs of the XR-2125.

PIN	NAME	FUNCTION LOGIC HIGH	FUNCTION LOGIC LOW
1	$\overline{SB}$	Normal Operation	Standby Mode
2	T_{XEN}	Transmitter Enabled	Transmitter Disabled
3	R_{XEN}	Receiver Enabled	Receiver Disabled
8	$10/\overline{9}$	10 Bit Character	9 Bit Character

Table 1. Control Input Conditions

PRINCIPLES OF OPERATION

The XR-2125 performs the complete asynchronous to synchronous and synchronous to asynchronous conversion on the serial transmit and receive data paths in a Bell 212A type modem. This conversion allows the synch modulator/demodulator such as the XR-2121/XR-2122 to communicate with the async DTE. The async format is character type as shown in Figure 1.

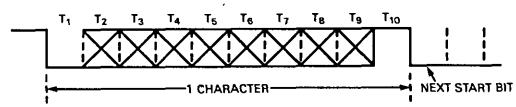


Figure 1. Async Character

Figure 1 shows each character starting with a start bit (T1) followed by either 7 or 8 data bits (8 shown → T2 - T9) and ending by a stop bit T10) this makes a total character length of either 9 or 10 bits, which the XR-2125 can be selected for by pin 8, 10/9.

The XR-2125 can also provide "flow through" operation by disabling the transmit and receive sections using pins 2 and 3, T_{XEN} and R_{XEN}. This mode would be used for 1200 BPS sync mode or 300 BPS bit async operation.

Figure 2 illustrates a typical connection of the XR-2125. Pins 2 and 3 (T_{XEN} and R_{XEN}) are used to toggle the XR-2125 into the high speed asynchronous mode. The main function of the XR-2125 is to synchronize asyn-chronous data (1200 BPS + 1% - 2.5%) from the DTE to synchronous data (1200 BPS) for the modulator, and to take synchronous demodulated data (1200 BPS) and conver it to the 1219 BPS asynchronous format for the DTE.

The break detector serves to distinguish between an actual break character and two consecutive nulls with the stop bit deleted. It forces reinsertion of the stop bit between the nulls and passes

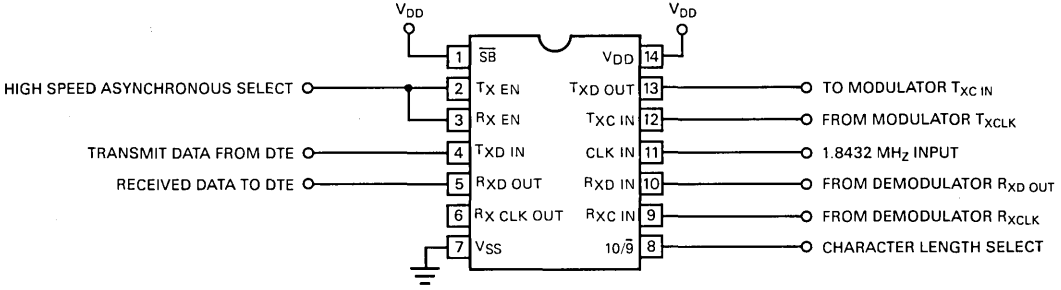


Figure 2. Typical Connection XR-2125

FSK Modem System

GENERAL DESCRIPTION

The XR-14412 contains all the necessary circuitry to construct a complete FSK modulator/demodulator (MODEM) system. Included is circuitry for pin-programmable frequency bands, either U.S. or foreign (CCITT) standards for low-speed MODEMS. The XR-14412 provides T^2L-compatible inputs and outputs. Included in the XR-14412 are features for self-testing and an echo suppression tone generator. The XR-14412 utilizes complementary MOS technology for low-power operation.

FEATURES

Simplex, Half-Duplex, and Full-Duplex Operation
Crystal Controlled
Answer or Originate Modes
Single Supply Operation
Self-test Mode
Selectable Data Rates—300, or 600 bps
T^2L- or CMOS-Compatible Inputs and Outputs
Echo Suppressor Disable Tone Generator
U.S. or Foreign (CCITT) Compatible

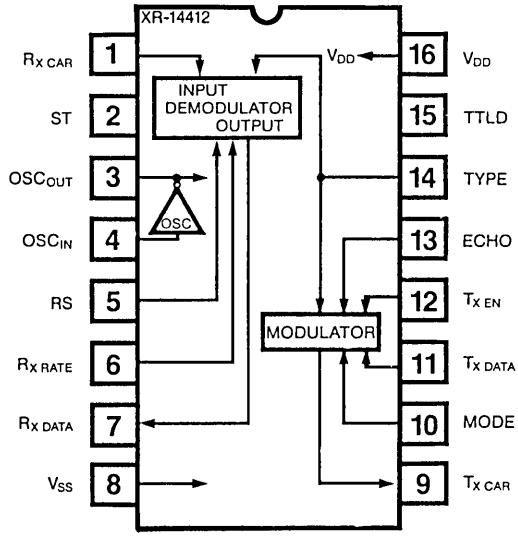
APPLICATIONS

Stand-Alone MODEMS
Remote Terminals
Acoustical Couplers
Built-in MODEMS

ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-14412F	15V
XR-14412V	6V
Any Input Voltage	V_{DD} + .5V to V_{SS} − .5V
Output Current from any Pin (Except Pins 7 or 8)	10 mA
Output Current from Pin 7 or 8	35 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Ceramic Package	1000 mW
Derate Above T_A = +25°C	8.0 mW/°C
Plastic Package	625 mW
Derate Above T_A = +25°C	5.0 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Voltage Range
XR-14412FP	Plastic	4.75V to 15V
XR-14412VP	Plastic	4.75V to 6V
XR-14412FN	Ceramic	4.75V to 15V
XR-14412VN	Ceramic	4.75V to 6V

SYSTEM DESCRIPTION

The XR-14412 is basically comprised of two main components; the FSK modulator and demodulator. The modulator serves to convert or encode incoming binary data into two discrete frequencies. The pair of frequencies generated are determined by which standard (US or CCITT), and mode (answer or originate), are selected. These frequencies are within a range suitable for transmission over the telephone lines. The demodulator performs the opposite function by decoding the received pairs of frequencies into binary data. It also responds to those frequencies selected by the standard and mode selected. All functions within the XR-14412 are digital and controlled by a master clock. This clock is generated by an external crystal connected between the OSC_{IN} and OSC_{OUT} pins. As well as being used internally by the 14412, the clock may be used to clock other circuitry by using the OSC_{OUT} pin.

XR-14412

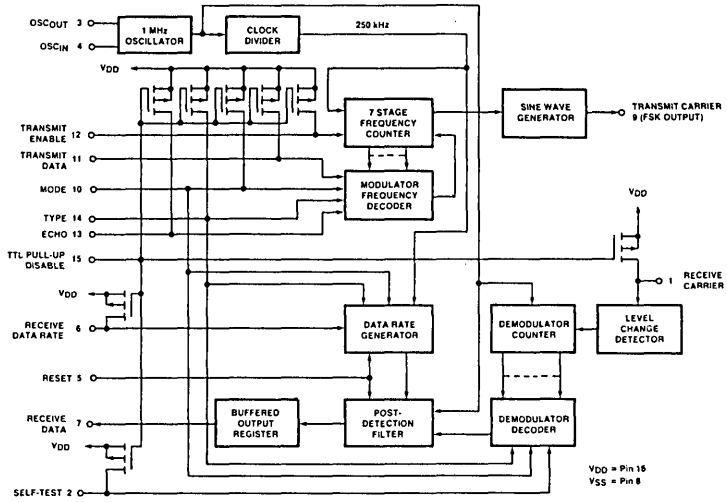
ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	V_{DD}** Vdc	−40°C MIN	−40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNIT
V_{OL}	Output Voltage "0" Level	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
	$V_{IN} = V_{DD}$ or 0	10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
V_{OH}	"1" Level	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
	$V_{IN} = 0$ or V_{DD}	10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
V_{IL}	Input Voltage* "0" Level									Vdc
	(V_O = 4.5 or 0.5 Vdc)	5.0	—	1.5	—	2.25	1.5	—	1.5	
	(V_O = 9.0 or 1.0 Vdc)	10	—	3.0	—	4.50	3.0	—	3.0	
	(V_O = 13.5 or 1.5 Vdc)	15	—	4.0	—	6.75	4.0	—	4.0	
V_{IH}	"1" Level									Vdc
	(V_O = 0.5 or 4.5 Vdc)	5.0	3.5	—	3.5	2.75	—	3.5	—	
	(V_O = 1.0 or 9.0 Vdc)	10	7.0	—	7.0	5.50	—	7.0	—	
	(V_O = 1.5 or 13.5 Vdc)	15	11.0	—	11.0	8.25	—	11.0	—	
	Pins 12, 15	5 to 15	0.75	—	0.8	2.0	—	0.85	—	
I_{OH}	Output Drive Current									mAdc
	(V_{OH} = 2.5) (Pin 7)	5	−0.62	—	−0.5	−1.5	—	−0.35	—	
	(V_{OH} = 9.5)	10	−0.62	—	−0.5	−1.0	—	−0.35	—	
	(V_{OH} = 13.5)	15	−1.8	—	−1.5	−3.6	—	−1.1	—	
I_{OL}	(V_{OL} = 0.4)	4.75	2.3	—	2.0	4.0	—	1.6	—	mAdc
	(V_{OL} = 0.5)	10	5.3	—	4.5	10	—	3.6	—	
	(V_{OL} = 1.5)	15	15	—	13	35	—	10	—	
I_{IN}	Input Current (Pin 15 = V_{DD})	—	—	—	—	—	±0.00001	±0.1	—	—	μAdc
I_P	Input Pull-up Resistor Source Current (Pin 15 = V_{SS}, V_{IN} = 2.4 Vdc) Pin 1,2,5,6,10,11,12,13,14	5	285	—	250	460	—	205	—	μAdc
C_{IN}	Input Capacitance	—	—	—	—	5.0	—	—	—	pF
I_T	Total Supply Current (Pin 15 = V_{DD})	5	—	4.5	—	1.1	4.0	—	3.5	mAdc
		10	—	13	—	4.0	12	—	11	
		15	—	27	—	8.0	25	—	23	
ACC	Modulator/Demodulator Frequency Accuracy (Excluding Crystal)	5 to 15	—	—	—	0.5	—	—	—	%
V_{2H}	Transmit Carrier Output 2nd Harmonic	5 to 10	—	—	−20	−26	—	—	—	dB
		10 to 15	—	—	−25	−32	—	—	—	
V_{OUT}	Transmit Carrier Output Voltage (R_L = 100 kΩ) (Pin 9)	5	—	—	0.2	0.30	—	—	—	V_{RMS}
		10	—	—	0.5	0.85	—	—	—	
		15	—	—	1.0	1.5	—	—	—	
t_{TLH}, t_{THL}	Receive Carrier Rise and Fall Times (Pin 1)	5	—	15	—	—	15	—	15	ns
		10	—	5.0	—	—	5.0	—	5.0	
		15	—	4.0	—	—	4.0	—	4.0	

*DC Noise Immunity (V_{IL},V_{IH}) is defined as the maximum voltage change from an ideal "0" or "1" input level, that the circuit will withstand before accepting an erroneous input.

**Note: Only 5-Volt specifications apply to XR-14412VP devices.

EQUIVALENT SCHEMATIC DIAGRAM



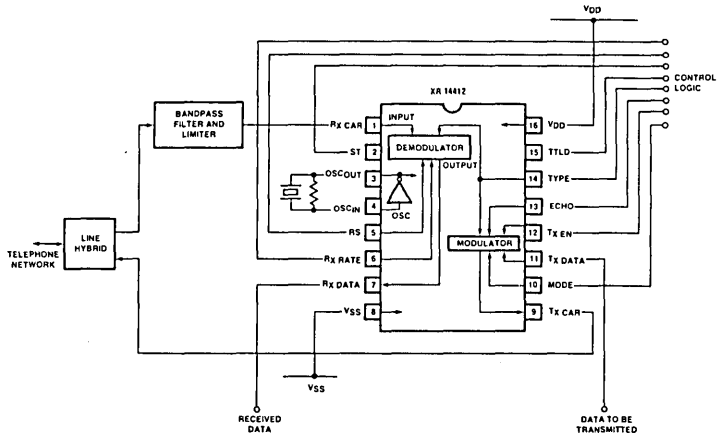


Figure 1. Typical Connection of the XR-14412 in a Complete Modem System

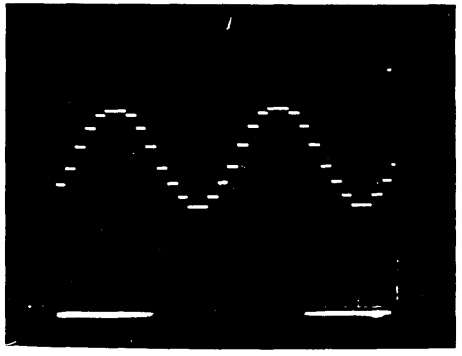


Figure 2. Transmit Carrier Sine Wave

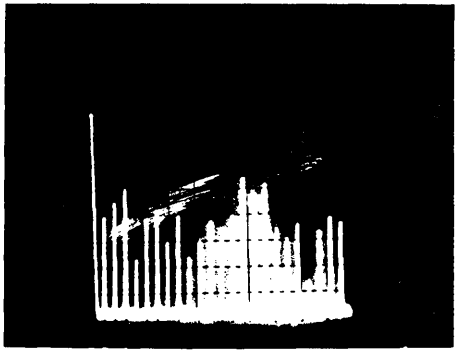


Figure 3. Typical Transmit Carrier Frequency Spectrum

PRINCIPLES OF OPERATION

Figure 1 shows the typical connection for the XR-14412 as a modem system. The system has four main component blocks. They are FSK modulator and demodulator, which are contained in the XR-14412, the bandpass filter, and the line hybrid. The function of each block is as follows:

Line Hybrid: This block acts to direct received FSK information to the bandpass filter and demodulator, while the FSK modulated carrier is directed to the telephone network.

Bandpass Filter and Limiter: Received FSK information is filtered by this block to remove extraneous signals received from the telephone network. The local transmitter carrier is also filtered out. The limiter stage is used to provide the XR-14412 with a TTL- or CMOS-compatible signal.

Modulator: This block, contained in the XR-14412, converts serial binary data into an FSK-encoded carrier signal. The carrier frequency is controlled by the mode and type inputs. Input data must be TTL- or CMOS-compatible. The output of the modulator is a digitally synthesized sine wave (see Fig. 2), with its harmonic content shown in Fig. 3.

Demodulator: This is used to convert an FSK-encoded carrier signal into serial data. The rate at which data can be received and decoded is controlled by the R_X rate and type control inputs.

Description of Control Inputs—Refer to Figure 1 and Table 1.

Type (Pin 14): This input is used to select either U.S. or CCITT operating frequencies.

Transmit Data ($T_{X\ DATA}$, Pin 11): This is the input for binary serial data.

Transmit Carrier ($T_{X\ CAR}$, Pin 9): This output provides a digitally synthesized sine wave derived from a 1 MHz crystal oscillator. The carrier frequency is controlled by the type and mode inputs.

Transmit Enable ($T_{X\ ENABLE}$, Pin 12): This pin is used to enable and disable the modulator, or $T_{X\ CAR}$, output.

Mode (Pin 10): In conjunction with the type input, the carrier frequencies are selected with this input.

Echo (Pin 13): This input is used to program the modulator to produce a 2100-Hz tone for disabling line echo suppressors.

Receive Data ($R_{X\ DATA}$, Pin 7): This is the binary data output resulting from demodulating the FSK-encoded receive carrier.

Receive Carrier ($R_{X\ CAR}$, Pin 1): The FSK-encoded receive carrier is fed into this input. The input signal must have either TTL or CMOS logic levels with a duty cycle of 50% ± 4%.

Receive Data Rate ($R_{X\ RATE}$, Pin 6): This input is used to adjust the demodulator for the incoming data rate.

Self-Test (ST, Pin 2): When a high level (ST = "1") is placed on this input, the demodulator is switched to the modulator frequency and demodulates the transmitted FSK signal.

Reset (R_S, Pin 5): This input can be used to disable the demodulator. With reset at logic "1", the demodulator output is forced high, logic "1". For normal operation, reset is tied low, logic "0".

Crystal (OSC_{IN}, OSC_{OUT}, Pin 4, Pin 3, respectively): A 1.0 MHz crystal is connected between these two pins for utilizing the on-chip oscillator. An external oscillator can also be used by feeding it into the OSC_{IN}, Pin 4, input. In the crystal mode, external parasitic capacitance, including crystal shunt capacitance, must be less than 9 picofarads at Pin 4.

TTL Pull-Up Disable (TTLD, Pin 15): All of the inputs to the XR-14412 have on-chip pull-up resistors. These pull-up resistors may be disabled when interfacing to CMOS logic by taking the TTLD input to a logic "1". For TTL logic interfacing, TTLD is tied to a logic "0".

APPLICATIONS

Figure 4 shows the XR-14412 connected as a 300-baud FSK modem. Amplifiers A_1 – A_3 are connected as bandpass filters to remove extraneous signals picked up from the phone line as well as local oscillator isolation. A_4 is connected as a comparator to provide limiting to the received carrier and provide the necessary square wave for Pin 1, $R_{X\ CAR}$, input. A_5 acts as a line hybrid. It provides amplification to the received carrier while attenuating the local oscillator, trying to go toward the bandpass filter. A_6 is simply used to buffer the $T_{X\ CAR}$, Pin 9, output of the XR-14412.

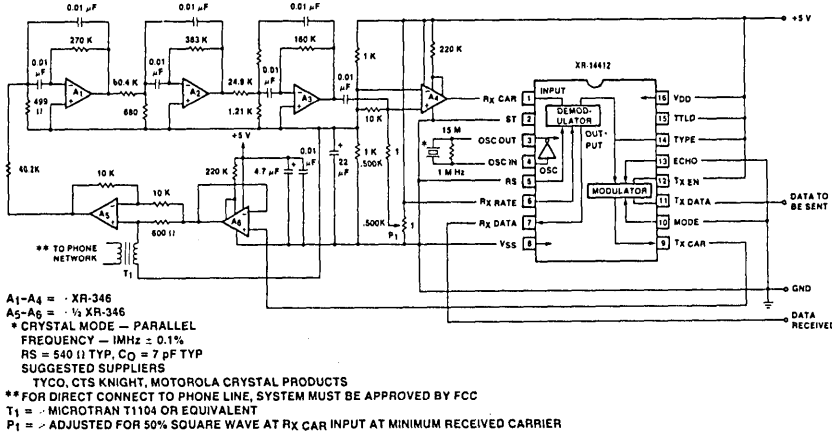
The configuration as shown is for answer mode, as the mode pin is at a logic "0". This circuit will work over a received carrier range of −10 dBm to −40 dBm.

Figure 5 shows a connection using the two spare amplifiers from the XR-346 to provide a carrier detect output. Here A_7 acts to amplify and peak detect the received carrier from the output of the bandpass filter. This voltage is then fed to A_8, connected as a comparator, to provide a logic output for carrier detect indication.

Table 1. Input/Output Controls

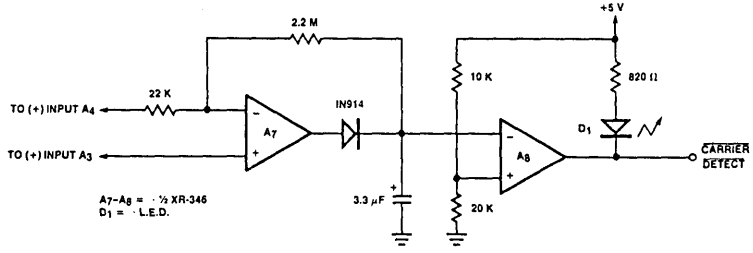
INPUTS					OUTPUTS				
TX ENABLE (12)	RX RATE (6)	MODE (10)	TYPE (14)	ECHO (13)	STANDARD	MODE	TX DATA	TX CARRIER	BAUD RATE
1	0	1	1	0	US	ORIGINATE	MARK 1	1270 Hz	600 bps
1	0	1	1	0	US	ORIGINATE	SPACE 0	1070 Hz	600 bps
1	0	0	1	0	US	ANSWER	MARK 1	2225 Hz	600 bps
1	0	0	1	0	US	ANSWER	SPACE 0	2025 Hz	600 bps
1	1	1	1	0	US	ORIGINATE	MARK 1	1270 Hz	300 bps
1	1	1	1	0	US	ORIGINATE	SPACE 0	1070 Hz	300 bps
1	1	0	1	0	US	ANSWER	MARK 1	2225 Hz	300 bps
1	1	0	1	0	US	ANSWER	SPACE 0	2025 Hz	300 bps
1	1	1	0	0	CCITT	CHANNEL 1	MARK 1	980 Hz	300 bps
1	1	1	0	0	CCITT	CHANNEL 1	SPACE 0	1180 Hz	300 bps
1	1	0	0	0	CCITT	CHANNEL 2	MARK 1	1650 Hz	300 bps
1	1	0	0	0	CCITT	CHANNEL 2	SPACE 0	1850 Hz	300 bps
1	X	0	0	1	CCITT	CHANNEL 2	— 1	2100 Hz	—
0	X	X	X	X	—	—	— —	NO OUTPUT	—

1 — Input or output is at a digital high, refer to Electrical Characteristics for exact value.
0 — Input or output is at a digital low, refer to Electrical Characteristics for exact value.
X — Can be either a 1 or a 0.



A1–A4 = · XR-346
A5–A6 = · ½ XR-346
* CRYSTAL MODE — PARALLEL
FREQUENCY — 1MHz ± 0.1%
RS = 540 Ω TYP, C_O = 7 pF TYP
SUGGESTED SUPPLIERS
TYCO, CTS KNIGHT, MOTOROLA CRYSTAL PRODUCTS
** FOR DIRECT CONNECT TO PHONE LINE, SYSTEM MUST BE APPROVED BY FCC
T1 = · MICROTRAN T1104 OR EQUIVALENT
P1 = ⌿ ADJUSTED FOR 50% SQUARE WAVE AT RX CAR INPUT AT MINIMUM RECEIVED CARRIER

Figure 4. Complete 300 Baud, Answer Mode, FSK Modem



A7–A8 = · ½ XR-346
D1 = · L.E.D.

Figure 5. Carrier Detect Circuit

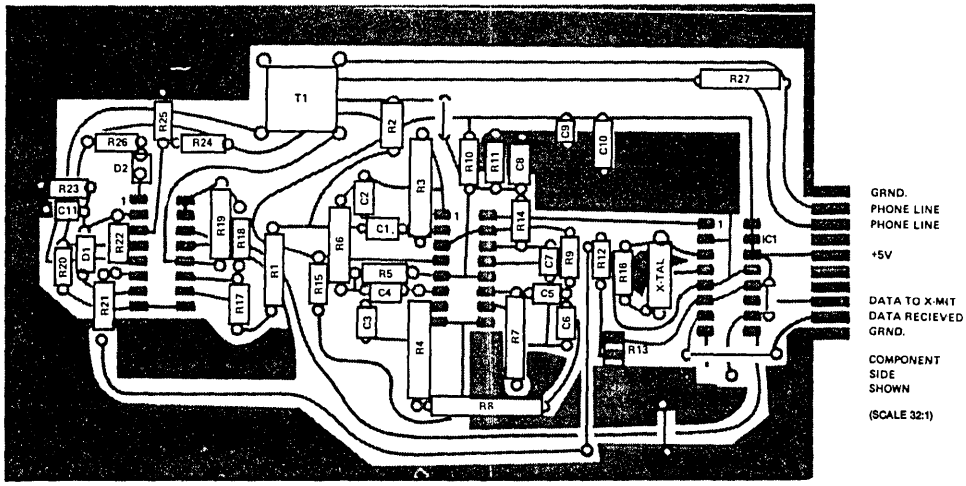


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Figure 6. Complete FSK Modem Printed Circuit Board Layout (Circuit Shown in Figure 4)

Table 2. Parts List for 300 Baud MODEM.

*1% tolerance; all other resistors are 1/4W, 10%; all capacitors are 10%.
Resistors are in ohms and capacitors are in μF.

	ANSWER	ORIGINATE		ANSWER	ORIGINATE
*R1	40.2K	47.5K	R24	20K	20K
*R2	499	191	R26	500	500
*R3	270K	357K	*R27	600	600
*R4	383K	270K			
*R5	680	160	C1–C6	.01	.01
*R6	60.4K	39.4K	C7	.1	.1
*R7	160K	160K	C8	22	22
*R8	24.9K	20K	C9	.01	.01
*R9	1.21K	360	C10	4.7	4.7
R10–R11	1K	1K	C11	3.3	3.3
R12	500K	500K			
R13	500K Pot	500K Pot	D1	IN914	IN914
R14	10K	10K	D2	LED	LED
R15	220K	220K			
R16	15M	15M	T1	Microtran	Microtran
R17–R18	10K	10K		T1104	T1104
*R19	600	600			
R20	220K	220K	CRYSTAL	1 MHz ± .1%	1 MHz ± .1%
R21	22K	22K			
R22	2.2M	2.2M	A1–A8	XR-346	XR-346
R23	3.0K	3.0K			
R24	20K	20K	MODEM IC_1	XR-14412VP	XR-14412VP
R25	30K	30K			

Section 3 – Data Communication Circuits

FSK Modem Filter

GENERAL DESCRIPTION

The XR-2103 is a Monolithic Switched-Capacitor Filter designed to perform the complete filtering function necessary for a Bell 103 Compatible Modem. The XR-2103 is specifically intended for use with the XR-14412 Modulator/Demodulator to form a complete stand alone two-chip modem. In addition to complete high and low bandpass filters, the XR-2103 contains internal mode switching, auto-zeroing limiter and dedicated duplexer op amp. An on board carrier detect circuit is also included to complete the overall system. Designed for crystal-controlled operation, the XR-2103 operates from a 1.0 MHz crystal or external clock. Buffered clock output is provided for the XR-14412. A self-test circuit is included.

The XR-2103, available in a 20 pin package, utilizes CMOS technology for low power operation with a supply voltage range from 4.75V to 6V.

FEATURES

Single 5 Volt Operation
Complete On Board Output Active Filters
Low Supply Current
Internal Answer/Originate Mode Switching
Programmable Input Receive Gain
Carrier Detect Output
Active Duplexer

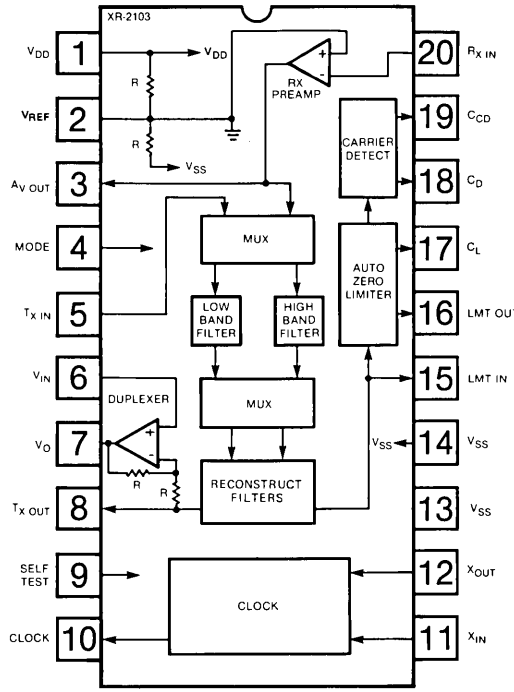
APPLICATIONS

Bell 103 Transmit/Receive Filtering
Complement to XR-14412 or Other
Modulators/Demodulators

ABSOLUTE MAXIMUM RATINGS

Power Supply	16V
Power Dissipation Plastic Package	650 mW
Derate Above 25°C	5.0 mW/°C
Power Dissipation Ceramic Package	1.0 W
Derate Above 25°C	8.0 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Any Input Voltage	(V_{DD} + 0.5V) to (V_{SS} -0.5V)

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2103CP	Plastic	0°C to 70°C
XR-2103CN	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

The XR-2103 internally consists of four main signal blocks. They are: input and output multiplexers to route the transmit and receive signals to the proper filter and output, according to the mode input; high and low band filters, 6 poles each, to perform precise bandpass filtering; output RC active filters to perform output reconstruction and filtering; carrier detection circuit for system interfacing.

An input amplifier with programmable gain is provided for the receive signals. The XR-2103 contains an internal clock oscillator which accepts either a crystal or an external oscillator of 1 MHz.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5V, V_{SS} = 0V, X_{IN} = 1.0 MHz, T_A = 25°C, unless specified otherwise.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
V_{DD}	Power Supply Voltage Range	4.75		6	V	V_{SS} = 0
I_{DD}	Power Supply Current		7	10	mA	V_{DD} = 5V
ANALOG SECTION						
RECEIVE AMPLIFIER						
V_{OS}	Offset Voltage	-150		150	mV	
A_{OL}	Open Loop Gain		80		dB	R_L = 100k
I_B	Input Bias Current		1		pA	
SR	Slew Rate		2		V/μs	
	Output Swing	3	4.5		Vp-p	R_L = 100k to GND (Pin 2)
DUPLEXER						
	Isolation		44		dB	R_2 = Line Resistance = 600Ω
	Output Swing	3	4.5		Vp-p	
V_{OS}	Offset Voltage	-150		150	mV	
LIMITER						
	Output Symetery		±1.5	±2.0	%	C_c = 0.1 μf, from 50% Duty Cycle
	Output Swing		4		Vp-p	R_L = 1 meg
	Output Current		100		μA	R_L = 1k
CARRIER DETECT						
V_{th}	Threshold Voltage		-48		dBm	Receive Amplifier Gain =24 dB
	Hysteresis	2	4	6	dB	
t_{on}	Turn On Time		≥100		msec	C_{cd} = 0.1 μf, V_{in} = 48 dBm, Gain = 24 dB
t_{off}	Turn Off Time		≤100		msec	
LOW BAND FILTER						
f_o	Center Frequency	1160	1170	1180	Hz	
BW	Bandwidth		500		Hz	
V_{fs}	Full Scale Input		2.5		Vp-p	
A_r	Pass Band Gain	3	4	5	dB	
DR	Dynamic Range		50		dB	
PSRR	Power Supply Rej.		15		dB	f = 2 KHz
	Pass Band Ripple			2	dB	p-p 1070 Hz-1270 Hz
	High Band Rejection	40			dB	2025 Hz-2225 Hz
GD	Differential (Group) Delay		200	500	μs	1070 Hz-1270 Hz
	Clock Feedthrough		-60		dBV	62.5 kHz
HIGH BAND FILTER						
f_o	Center Frequency	2105	2125	2145	Hz	
BW	Bandwidth		500		Hz	
V_{fs}	Full Scale Input		2.5		Vp-p	
A_r	Pass Band Gain	3	4	5	dB	
DR	Dynamic Range		50		dB	
PSRR	Power Supply Rej.		18		dB	f = 1 kHz
	Pass Band Ripple			2	dB	p-p 2025 Hz - 2225 Hz
	Low Band Rejection	40			dB	1070 Hz - 1270 Hz
GD	Differential (Group) Delay		200	500	μs	2025 Hz - 2225 Hz
	Clock Feedthrough		-60		dBV	62.5 kHz
TRANSMIT						
V_{OS}	DC Offset Voltage	-150		+150	mV	
	Output Swing	2.2			Vp-p	R_2 = Line Resistance = 600Ω
	Output Current		1.2		mA	
DIGITAL CMOS LOGIC LEVELS (V_{DD} = 5V, V_{SS} = 0 V)						
V_{ih}	Input Voltage		2.75	3.5	V	'1' Level
V_{il}	Input Voltage	1.5	2.25		V	'0' Level
I_{oh}	Output Current	0.5	1.5		mA	'1' Level CLK OUT
I_{ol}	Output Current	1.0	5.0		mA	'0' Level CLK OUT
I_{oh}	Output Current	0.1	1.5		mA	'1' Level X OUT
I_{ol}	Output Current	0.2	0.9		mA	'0' Level X OUT

OPERATING PRINCIPLES

The XR-2103 contains all the filtering and multiplexing functions necessary for a Bell 103 type (300 baud) FSK modem. A complete modem requires only the XR-2103, the XR-14412, and telephone line interfacing hardware. A description of the main functional blocks follows.

Bandpass Filtering: Two six pole, 500 Hz bandwidth switched capacitor filters, designed for Bell 103 standard center frequencies of 1170 Hz (low band) and 2125 Hz (high band), constitute the main portion of the device. Both filters feature +4 dB passband gain, 50 dB dynamic range, and more than 40 dB opposite band rejection. Filter response curves are depicted in Figure 3. On board multiplexing allows using these filters for both transmitting and receiving. Active low pass filters reconstruct the time sampled output signals, characteristic of switched capacitor filters, and attenuate the unwanted energy above 15 kHz.

Duplexer: An operational amplifier is employed as an active two to four wire converter (duplexer). The two phone wires are "split" into transmit and receive components for proper processing; the transmit output from Pin 8 is applied to the lines through a resistor and the received signal is drawn from the line and routed into a preamplifier. Transmit energy appears as a common mode signal, hence does not appear on the duplexer output. The received signal, meanwhile, is amplified by two. Isolation is maximized when the transmit injection resistor (between Pins 6 and 8) is equal in magnitude to the phone line impedance (600 Ω nominal). Transmit signal levels are typically -9 dBm.

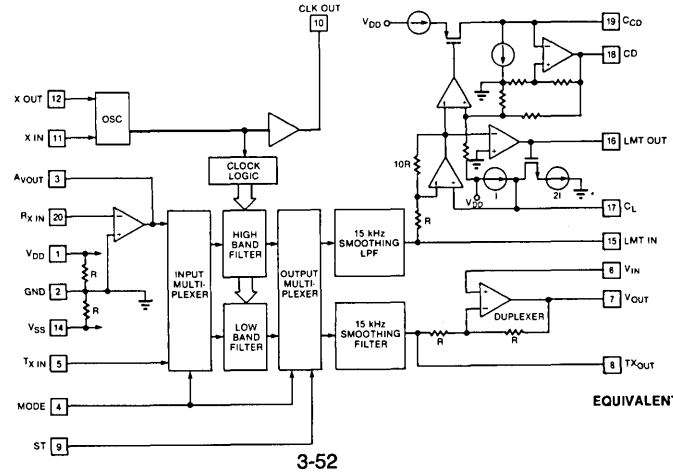
Received Carrier Amplifier: An operational amplifier, with its inverting input on Pin 20 and output on Pin 3, serves as a received carrier amplifier. Duplexer output (Pin 7) is routed to Pin 20 through a 100 kΩ or larger resistor. Gain, typically 5 (14 dB), equals the ratio of the feedback resistor (Pin 3 to Pin 20) to the input resistor (Pin 7 to Pin 20). The non-inverting input is internally biased to one half supply. The amplifier features open loop gain of 80 dB, output swings of 4.5 Vp-p, and a slew rate of 2V/μs. This pin-out allows flexible signal processing capabilities: for example, an input low pass filter for eliminating aliasing is easily achieved.

Auto-Zeroing Limiter: An automatic offset zeroing comparator (limiter) compensates for errors caused by system offset voltages and currents, and converts the received carrier into an accurate 50% duty cycle waveform. The resultant square wave on Pin 16 is at digital logic levels and can interface directly with the modulator/demodulator circuit.

Carrier Detector: An on board carrier detection circuit simplifies total system interfacing. Carrier detect output (Pin 18) pulls low when a suitable signal is received. With 14 dB of gain in the receiver preamplifier, the threshold level is -38 dBM and has 4 dB of hysteresis. Turn on/off delay time is externally programmable by a capacitor from Pin 19 to ground. A 0.1 μF unit yields 100 ms; delay is directly proportional to capacitance.

Clocking: Filter frequency accuracy is directly related to the clock frequency. The device operates within specifications with a 1 MHz clock, provided by either a 1 MHz crystal or by sharing the 1 MHz clock signal from the XR-14412. The device will operate at other clock frequencies, but the filter center frequencies will differ. The crystal and a parallel 10 MΩ resistor are attached between Pins 11 and 12. The crystal should be series resonant with a shunt capacitance less than 9 pF. Pin 10 is the buffered clock output for interconnection with other devices.

Self Test: An on board self test diagnostic activates an analog loop-back mode: the transmit carrier is routed through the proper filter and back through the receive limiter, allowing performance verification of all systems. T_X OUT and R_X IN are disabled when self test is high.



EQUIVALENT SCHEMATIC DIAGRAM

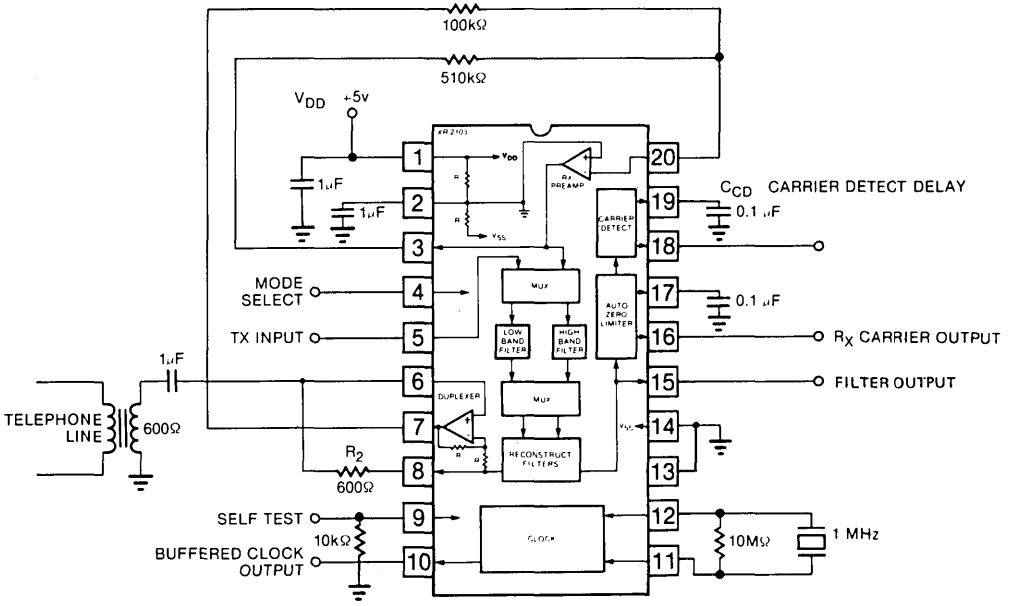


Figure 1. Basic Applications Circuit

Carrier detect threshold is -38dBm in this configuration.

LOGIC INPUT \ STATE	0	1
MODE	ANSWER	ORIGINATE
ST	NORMAL OPERATION	SELF TEST MODE

Figure 2. Control Inputs

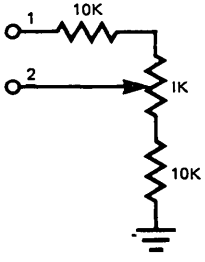


Figure 3. Reference Voltage Trimming for Performance Optimization

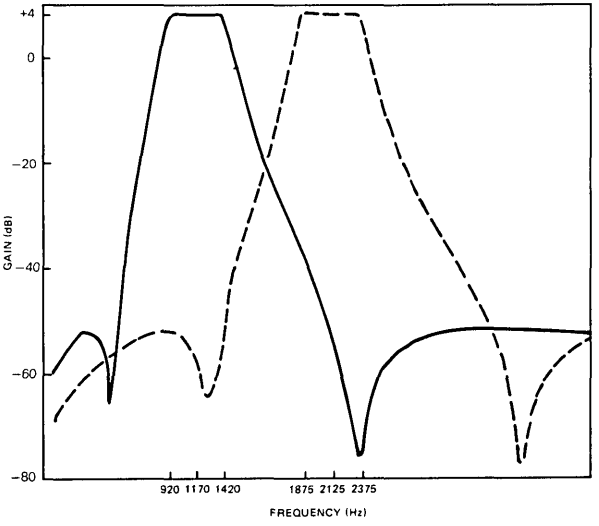


Figure 4. Filter Characteristics

APPLICATIONS

The Bell 103 compatible modem of Figure 5 consists of the XR-2103 FSK modem filter and the XR-14412 FSK modulator/demodulator. Designed for full duplex 300 baud operation, the circuit requires only telephone line and computer interfacing. The entire system uses a single 5V supply, and performs both answer and originate functions. Answer/Originate selection is controlled by the mode input; low inputs select answer, high selects originate.

The telephone line is connected via an isolation transformer to the duplexer input (Pin 6) of the XR-2103. A resistor, equal to the line resistance, attaches from Pin 6 to the transmit output (Pin 8) and couples the transmit signal to the line. The received signal is removed from the line via the duplexer (also called a "two to four wire converter" or "hybrid"). Duplexer output is coupled through the receive carrier preamplifier into the multiplexer, where the proper band pass filter is selected. Transmit energy is seen as a common mode signal and does not appear on the duplexer output.

If the system is in the originate mode (mode pin pulled high), the received signal passes through the high band filter. Then, the sampled signal is reconstructed by an on board RC active low pass filter and is fed into the limiter and carrier detect circuit. Carrier detect output (Pin 18) pulls low after a 100 ms delay, controlled by the 0.1 μF capacitor on the C_{CD} pin (Pin 19). The limiter circuit compensates for circuit imperfections (offset voltages, etc.), and outputs a 50% duty cycle waveform to the demodulator input (Pin 1) of the XR-14412. The demodulated data appears on Pin 7 of the XR-14412.

Transmit data is applied to the modulator input (Pin 11) of the XR-14412. Depending on mode, answer or originate, the data modulates either the high or low band. The modulated signal exits Pin 9 and is applied to the transmit multiplexer input (Pin 5) of the XR-2103; is filtered, reconstructed, and sent into the duplexer and the phone line.

One shared time base is employed: here, the oscillator of the XR-2103 serves both devices. Buffered output is routed from Pin 10 of the XR-2103 into Pin 4 of the XR-14412.

With suitable telephone line coupling and data system interfacing, this modem realizes its goals of high performance and reliability at low cost.

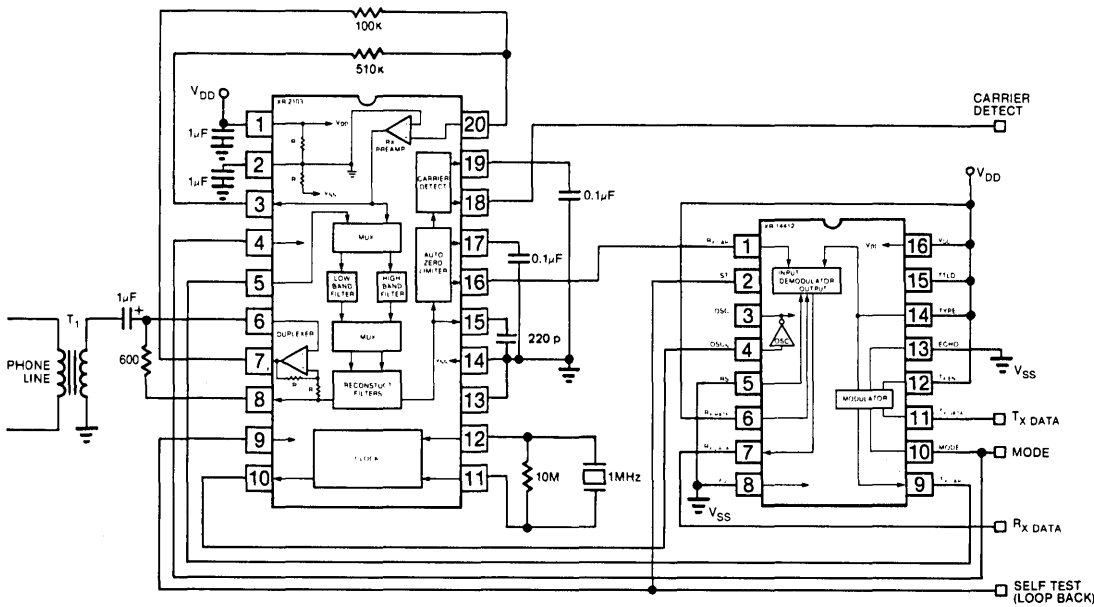


Figure 5. Bell 103 Compatible Modem

PSK Modem Filter

GENERAL DESCRIPTION

The XR-2120 is a self-contained bandpass filter set designed for realization of Bell 212A compatible 1200 bits/sec PSK modems. The XR-2120 utilizes CMOS technology and switched capacitor circuit techniques to minimize external components to a single crystal or frequency source. Contained in the device are two complete bandpass filters centered around the Bell standard 1200 Hz and 2400 Hz send and receive frequencies. These filters also provide compromise line equalization. Additional features included are digitally programmable transmit and receive gains as well as input anti-aliasing and complete output smoothing filters. Separate V_{SS} pins for transmit, receive, and digital sections are provided to minimize crosstalk.

The XR-2120 features guaranteed filter group delay specifications, within ±100μS of nominal. The XR-2120C is a relaxed version of the XR-2120 with group delay specified within ±150μS. The devices are available in a 22 pin (0.4 inch wide) plastic or ceramic package, and operate over a wide range of supply voltages.

FEATURES

On-board Crystal Oscillator With Buffered Output
Internal Anti-aliasing Filters
Complete On-board Output Active Filters
Digitally Programmable Transmit and Receive Gains
MODE Input Internally Switches Filters
for Answer/Originate
Single or Split Supply Operation
Center Frequencies Movable with Input Clock
High-Impedance Inputs (100 kΩ min)
1% Center Frequency Accuracy
Separate CLK IN and CLK OUT Pins

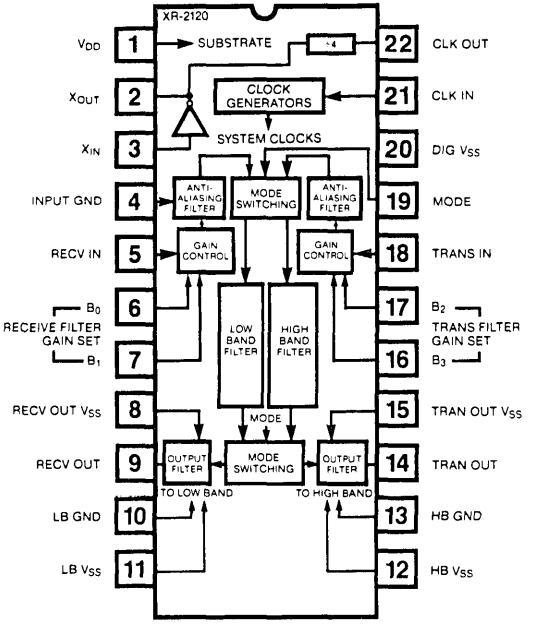
APPLICATIONS

Bell 212A Transmit/Receive Filtering
Answer Back Signal Filtering

ABSOLUTE MAXIMUM RATINGS

Power Supply	16V
Power Dissipation, Plastic	1.0W
Derate Above 25°C	5 mW/°C
Power Dissipation, Ceramic	1.3W
Derate Above 25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Any Input Voltage	(V_{DD} + 0.5V) to (V_{SS} - 0.5V)

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2120CN	Ceramic	0°C to +70°C
XR-2120CP	Plastic	0°C to +70°C
XR-2120N	Ceramic	0°C to +70°C
XR-2120P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2120 is comprised of four main signal blocks: The digitally programmable gain amplifier, an input anti-aliasing switched capacitor filter, switched capacitor bandpass filters at 1200 Hz and 2400 Hz, and output RC active filters. These sections serve to: (1) amplify and condition incoming signals, (2) remove noise which can cause aliasing problems in the bandpass filters, (3) provide very precise bandpass filtering and phase compensation, and (4) perform output reconstruction and filtering. To perform these necessary filtering and phase compensation functions, a total of 48 poles are used in the XR-2120.

The programmable gain stages provide 4 selectable gains for transmit or receive. Separate clock output and input pins are provided for flexibility.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = 5 V, V_{SS} = −5 V, X_{IN} = 4.032 MHz (CLK IN = 1.008 MHz), T_A = 25°C, unless otherwise specified. Input gain = 0 dB (B1/B3 = B0/B2 = 0).

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL SECTION						
CLK OUT	CLK OUT Drive Capability			50	pF	
I_I	Digital Input Current	−1.0		1.0	μA dc	
V_{IL}	Digital Input Voltage	V_{SS}		V_{SS}+2	V	For "0" Level
V_{IH}		V_{DD}-2		V_{DD}	V	For "1" Level
ANALOG SECTION						
f_{OL}	Filter Center	1190	1200	1210	Hz	Low Band
f_{OH}	Frequencies	2380	2400	2420	Hz	High Band
BW	3 dB Bandwidth	900	950		Hz	Either Band
R_i	Input Impedance	100k			Ohms	
C_i	Input Capacitance			10	pF	
f_{SI}	Anti-Aliasing Filter Sampling Frequency		504		kHz	
f_{SB}	High/Low Band Sampling Frequency		126		kHz	
	Tran/Recv Output Drive Capability	10k		50	Ohms pF	
	Output Clock Feedthrough			2	mV rms	at 126 kHz
e_{o100}	Output Noise		160		μV rms	In Passbands (100 Hz BW)
e_{o1000}	Output Noise		700		μVrms	In Passbands (1kHz BW)
ei_{range}	Dynamic Range of Filters		70		dB	Note 1
Vo_{sw}	Output Voltage Swing	6.0	6.8		V pp	Note 2
2ndHarm	2nd Harmonic Content		-60		dB	f_{IN} = 1200 Hz Referenced to Fundamental
T_{SW}	Mode Switching		10		ms	
I_{DD}	Supply Current		9	27	mA	
V_{SUP}	Supply Voltage Range	±4.75 9.5	±5 10	±7.5 15.0	V V	Dual Supplies V_{DD} Reference to V_{SS}
A_V	Passband Gain					Input Gain = 0 dB
	Low Band	3.2	4.2	5.2	dB	1200 Hz
		−1.4	0	1.4	dB	900 - 1500 Hz (Note 3)
	High Band	2.8	3.8	4.8	dB	2400 Hz
		−1.7	0	1.7	dB	2100 - 2500 Hz (Note 3)
		0	1.2	2.2	dB	2500 - 2800 Hz (Note 3)

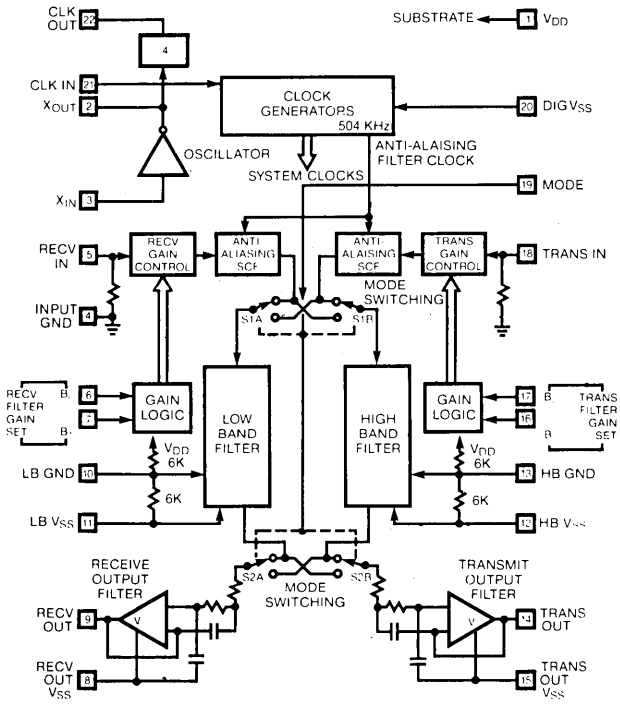
Note 1 Dynamic range is defined as $ei_{range} = 20 \text{ Log } (Vo_{sw}/e_o)$.
Note 2 Vo_{sw} is the maximum output swing before output clipping occurs.
Note 3 Gain measurements are relative to passband center frequency gain normalized to 0 dB.

ELECTRICAL CHARACTERISTICS Continued

FILTER RESPONSE

SYMBOL	PARAMETER	XR-2120			XR-2120C			UNIT	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
GD	Group Delay Low Band Filter	5060	5160	5260	5010	5160	5310	μs	900 Hz (See Figure 7)
		5100	5200	5300	5050	5200	5350	μs	1kHz
		5160	5260	5360	5110	5260	5410	μs	1.1kHz
		5200	5300	5400	5150	5300	5450	μs	1.2kHz
		5215	5315	5415	5165	5315	5465	μs	1.3kHz
		5255	5355	5455	5205	5355	5505	μs	1.4kHz
		5260	5360	5460	5210	5360	5510	μs	1.5kHz
	High Band Filter	5270	5370	5470	5220	5370	5520	μs	2.1kHz (See Figure 8)
		5040	5140	5240	4990	5140	5290	μs	2.2kHz
		5140	5240	5340	5090	5240	5390	μs	2.3kHz
		5015	5115	5215	4965	5115	5265	μs	2.4kHz
		5000	5100	5200	4950	5100	5250	μs	2.5kHz
		4920	5020	5120	4870	5020	5170	μs	2.6kHz
		4800	4900	5000	4750	4900	5050	μs	2.7kHz

EQUIVALENT SCHEMATIC DIAGRAM



PRINCIPLES OF OPERATION

Figure 1 shows the typical connection for the XR-2120 in a split supply configuration. In this mode, Pins 4, 10, and 13, are simply tied to ground. For single supply operation, Pins 10 and 13 internally bias to half supply and should be externally bypassed with 2.2 μF capacitors. Pin 4 does not internally dc bias, however, Pin 10 or 13 can provide it with a half supply bias point. In this connection, a 10 kΩ resistor should be used between Pin 4, and Pin 10 or 13, with Pin 4 bypassed with a 2.2 μF capacitor.

Signal flow is illustrated as shown in Figure 2. The transmit or receive signal will follow a path through four internal blocks. First it passes through a digitally programmable gain stage. The gain, as a function of a 2-Bit digital input, is shown in Figure 3. Next, the signal passes through a two-pole anti-aliasing low-pass filter at 12 kHz. This is used to remove noise around the main filter switching frequency of 126 kHz. The anti-aliasing filter is also a sampled-data filter, but is switched at a much higher rate of 504 kHz. It is necessary, therefore, to ensure that wideband noise above 252 kHz is not present at the inputs. In noisy environments a single noise pole RC filter at 30 kHz is usually sufficient for filtering input noise. The third signal block is the main bandpass filtering section at 1200 Hz or 2400 Hz, depending on the mode selected. The last section is the output smoothing filter; a two-pole RC active filter used to reconstruct the signal from its sampled data form.

The mode input pin is used to direct the transmit and receive signals to the appropriate filter section. Figure 4 shows mode selection logic convention.

The XR-2120 is designed to be operated with a 4.032 MHz crystal between the X_{IN} and X_{OUT} pins. The 4.032 MHz is divided by four and output on the CLK OUT pin, Pin 22. For normal operation, the CLK OUT is tied to the CLK IN pin, Pin 21; however, the bandpass center frequencies can be decreased by providing a divider between these two pins. An external CLK can be used by inputing a 1.008 MHz clock into the CLK IN pin, or a 4.032 MHz clock into the X_{IN} pin.

Figure 5 shows circuitry suitable for translating TTL signals to the CMOS levels required by all XR-2120 digital inputs. The amplitude and group delay characteristics of the XR-2120 are shown in Figures 6 through 8.

The XR-2120 may also be used in CCITT V.22 applications by adding guard tone notch filters as shown in Figure 9 or 10. This type of filter, when used with the XR-2120, will produce at least 60 dB of attenuation to either 550 Hz or 1800 Hz signals.

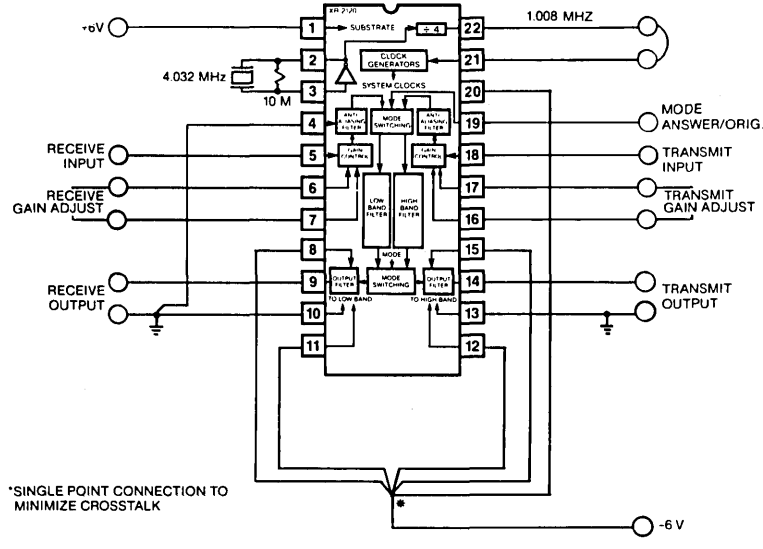


Figure 1: Typical Split Supply Connection.

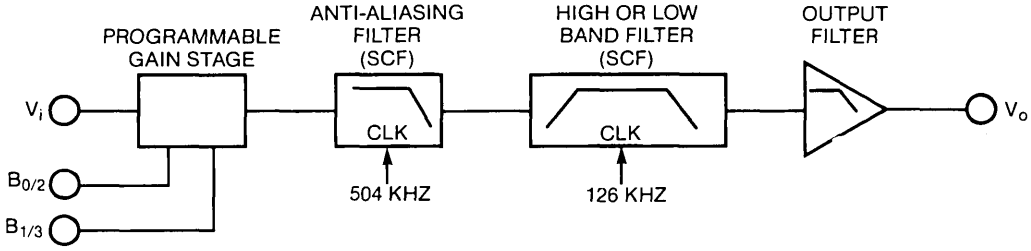


Figure 2: Signal Path

B1 / B3	B0 / B2	INPUT GAIN (dB)	
0	0	0	
0	1	6	
1	0	10	1 = Logic High
1	1	14	0 = Logic Low

Figure 3: Gain Programming (Nominal Gain Shown in Fig. 6)

MODE PIN	TRANSMIT	RECEIVE	TERMINOLOGY
1	Low Band	High Band	Originate
0	High Band	Low Band	Answer

Figure 4: Mode Selection Logic

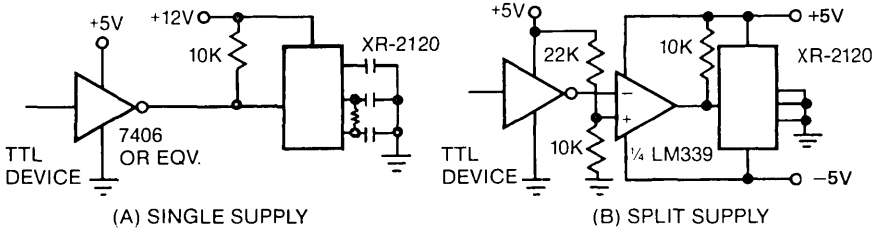


Figure 5: **TTL Interfacing of Digital Inputs.**

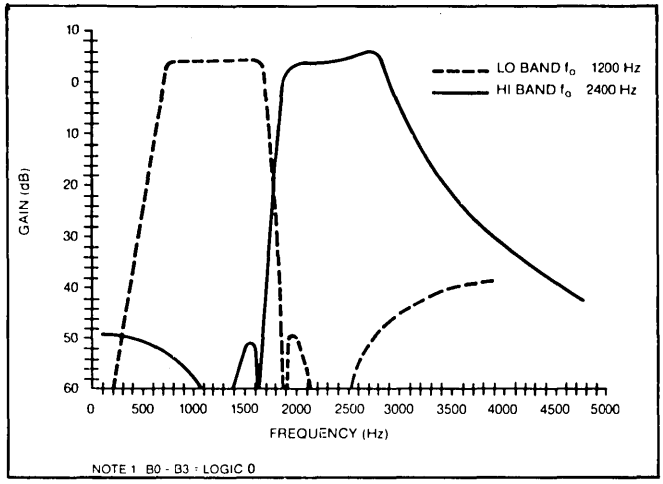


Figure 6: High and Low Band Amplitude Response.

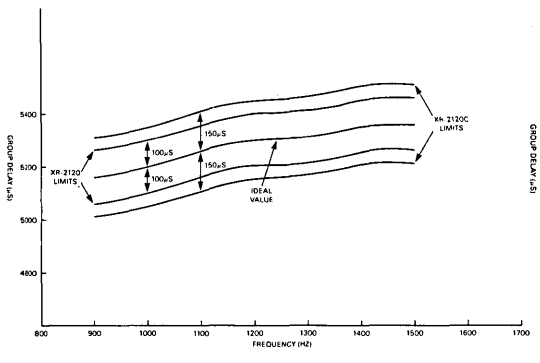


Figure 7: Low Band Group Delay Characteristics

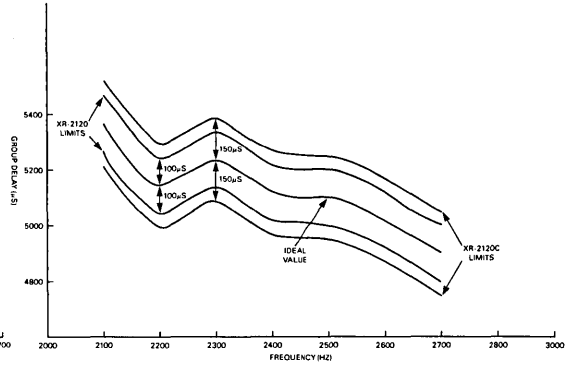


Figure 8: High Band Group Delay Characteristics

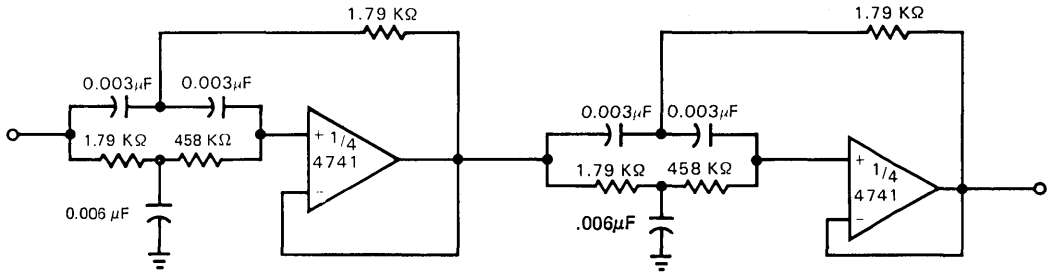


Figure 9. V.22 1800 Hz Notch Filter

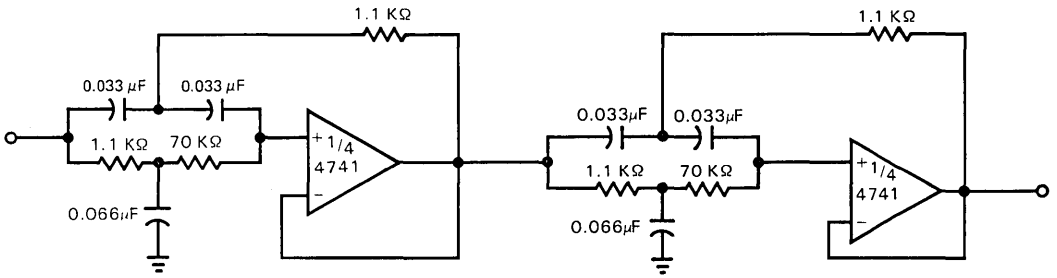


Figure 10. V.22 550 Hz Notch Filter

Bell 212A/CCITT V.22 Modem Filters

GENERAL DESCRIPTION

The XR-2126/2127/2128/2129 modem filters are monolithic CMOS switched capacitor filters designed for use in full duplex 1200 BPS modems. They meet all the filtering functions of the Bell 212A and CCITT V.22 modem specifications. They include the low band (centered at 1200 Hz) and high band (centered at 2400 Hz) filters with full channel compromise equalization and output smoothing filters for both bands.

For CCITT V.22 applications, a notch filter is included that can be selected for either 550 Hz or 1800 Hz and provide greater than 55 dB of rejection at these frequencies. Also included in these devices are two uncommitted operational amplifiers which can be used for input anti-aliasing filtering or for additional gain, and additional equalization for Worst Case Line (3002, C_O) conditions.

The XR-2126 is pin and function compatible to the AMI S35212 while the XR-2127 is pin and function compatible to the AMI S35212A. The XR-2128 is an enchanced version of the XR-2126 and XR-2127. Like the S35212 and S35212A, the high band filter in the XR-2126, XR-2127 and XR-2128 can be scaled down by a factor of 6 so it can be used to monitor Call Progress tones in smart modems. And, like the S35212A, the XR-2127 and XR-2128 have analog loop back mode for testing the functions of the modem.

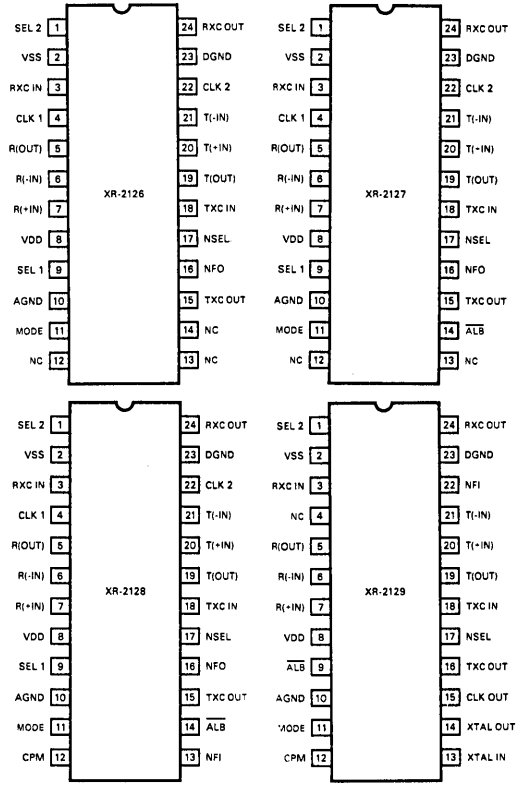
The XR-2128 contains two additional control pins, CPM (Pin 12) and NFI (Pin 13), that allow more accurate Call Progress Monitoring and easier V.22 implementation without the need for external multiplexers and smoothing filters. The CPM pin scales the low band filter by a factor of 2.5 for better centering over the Call Progress frequency range of 300 to 660 Hz, allowing the unscaled high band filter to be used for monitoring the modem answer tone.

The XR-2129 is an EXAR version of the 212A/V.22 modem filter. All the features of the XR-2126/2127/2128 except the clock frequencies are provided. The XR-2129 operates from a 1.8432 MHz crystal with an onboard clock oscillator. It also features a 1.8432 MHz buffered clock output and 10 dB of gain in the receive path. When used with the XR-2121 modulator, XR-2122 demodulator, and XR-2125 buffer, and a small amount of external circuitry, all the functions needed to realize the Bell 212A modem are in place.

APPLICATIONS

Bell 212A Modem Filtering
CCITT V.22 / V.22bis Modem Filtering
Bell 103 Modem Filtering
Other Modem Filter Applications

FUNCTIONAL BLOCK DIAGRAMS



FEATURES

Bell 212A/CCITT V.22 Compatible Transmit and Receive Filters with Full Channel Compromise Equalization
Selectable V.22 Notch Filters Included (550 Hz/1800 Hz)
Built-in Call Progress Mode/Enhanced Call Progress Mode
Analog Loop Back Capability
Phone Line Status Monitor Capability (Bypass Mode)
Additional Equilization for Worst Case Line (3002, C_O) Conditions
On-chip Transmit and Receive Output Smoothing Filters
Two Uncommitted Operational Amplifiers
Choice of Clock Frequencies:
153.6 KHz or 1.2288 MHz/2.4576 MHz on XR-2126, XR-2127, XR-2128
1.8432 MHz Crystal with On-Chip Clock Oscillator on XR-2129
TTL/CMOS Compatible Digital Inputs

ABSOLUTE MAXIMUM RATINGS

Power Supply	12V (±6V)
Power Dissipation, Plastic	1.0W
Derate Above 25°C	5 mW/°C
Power Dissipation, Ceramic	1.3W
Derate Above 25°C	7 mW/°C
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to 150°C
Any Input Voltage	(V_{DD} +0.5V) to (V_{SS} −0.5V)

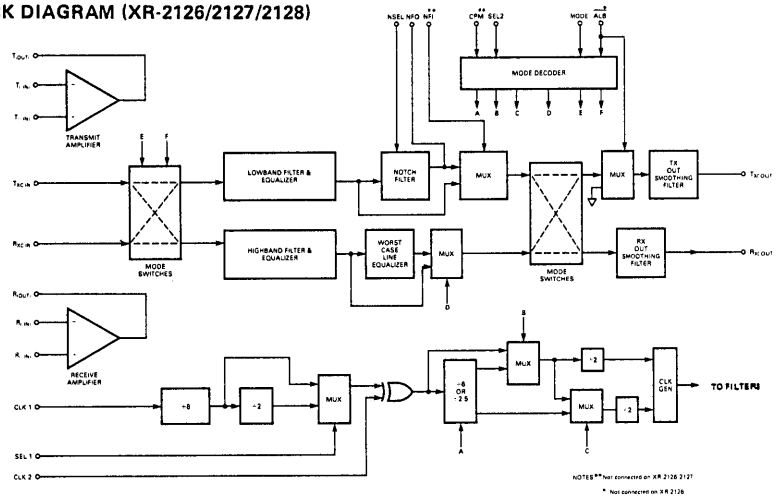
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2126CN	Ceramic	0°C to 70°C
XR-2126CP	Plastic	0°C to 70°C
XR-2127CN	Ceramic	0°C to 70°C
XR-2127CP	Plastic	0°C to 70°C
XR-2128CN	Ceramic	0°C to 70°C
XR-2128CP	Plastic	0°C to 70°C
XR-2129CN	Ceramic	0°C to 70°C
XR-2129CP	Plastic	0°C to 70°C

All devices are also available in Surface Mount Packages. Consult factory for complete information.

3

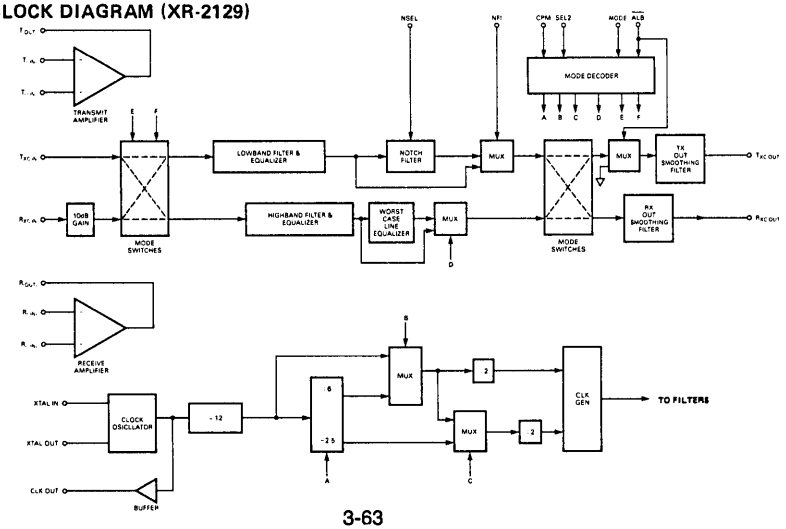
BLOCK DIAGRAM (XR-2126/2127/2128)



Note: CLK 1, $\overline{ALB}$, CLK 2 have internal pull-up to VDD

Note: SEL 2, SEL 1, MODE, CPM, NFI have internal pull-down to ground

BLOCK DIAGRAM (XR-2129)



DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 0°C to 70°C, V_{DD} = +5V ±5%, V_{SS} = −5V ±5%, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	Quiescent Current		15		mA	
I_{SS}	Quiescent Current		15		mA	
V_{IH}	High Level Input Voltage, Digital Signal Pins		2.5		V	Note 1
V_{IL}	Low Level Input Voltage, Digital Signal Pins		0.8		V	Note 2
V_{OH}	High Level Output Voltage	2.6			V	
V_{OL}	Low Level Output Voltage			0.5	V	

AC ELECTRICAL CHARACTERISTICS

Test Conditions: 25°C, V_{DD} = +5V, V_{SS} = −5V, unless specified otherwise.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
	Low Band Center Frequency	1190	1200	1210	Hz	
	High Band Center Frequency	2380	2400	2420	Hz	
	Adjacent Channel Rejection					
	Low Band	55	65		dB	
	High Band	55	75		dB	
	3 dB Bandwidth		950		Hz	
	Pass Band Gain at Center Frequency	−.5		+.5	dB	1200 Hz, 2400 Hz
	Crosstalk		65		dB	
	Dynamic Range		70		dB	
	Total Harmonic Distortion		0.3		%	
	Output Noise		1	2	mVrms	In Passband
	Stop Band Rejection					
	Low Band Filter		30		dB	At 500 Hz
			25		dB	At 1800 Hz
			75		dB	At 2400 Hz
			43		dB	At 4000 Hz
	High Band Filter		55		dB	At 500 Hz
			95		dB	At 1200 Hz
			25		dB	At 1800 Hz
			35		dB	At 4000 Hz
	NFI = High		65		dB	At 550 Hz, NSEL = Low
			65		dB	At 1800 Hz, NSEL = High
	Group Delay					
	Low Band Filter		5160		µsec	At 900 Hz
			5300		µsec	At 1200 Hz
			5360		µsec	At 1500 Hz
	High Band Filter		5370		µsec	At 2100 Hz
			5110		µsec	At 2400 Hz
			4900		µsec	At 2700 Hz
	Output Voltage Swing		8.0		Vp-p	

Note 1: $V_{in} > V_{IH}$ is a logic 1.
Note 2: $V_{in} < V_{IL}$ is a logic 0.

The following table lists EXAR filters and their pin compatible counterparts.

EXAR	Counterpart	
XR-2126	AMI	S35212
	Reticon	RM5632A
XR-2127	AMI	S35212A
	Sierra	SC11005
XR-2128	Sierra	SC11001
XR-2129	none	

PIN DESCRIPTIONS

Pin	Name	Desciption/Function
1	SEL 2	Call Progress mode selection; SEL 2 logic 0 for normal operation, SEL 2 logic 1 scales down the high band filter by 6 for Call Progress Monitoring.
2	VSS	Negative supply voltage (typically −5V).
3	RXC IN	Receive signal input.
4	CLK 1	Clock input 1 on XR-2126/2127/2128; 2.4576 MHz with SEL 1 logic 1 or 1.2288 MHz with SEL 1 logic 0, TTL or CMOS compatible.
	NC	No connection on XR-2129.
5	R(OUT)	Receive uncommitted operational amplifier output.
6	R(−IN)	Inverting input of the receive uncommitted operation amplifier.
7	R(+IN)	Non-inverting input of the receive uncommitted operational amplifier.
8	VDD	Positive supply voltage (typically +5V).
9	SEL 1	Selects clock frequency into Pin 4 on XR-2126/2127/2128; logic 0 for 1.2288 MHz, logic 1 for 2.4576 MHz.
	$\overline{\text{ALB}}$	Analog loop back on XR-2129; logic 1 for normal operation, logic 0 to internally loop back TXC OUT to RXC OUT with no signal (MUTE) on TXC OUT.
10	AGND	Analog ground.
11	MODE	Originate/Answer mode selection; logic 0 for Originate, logic 1 for Answer.
12	NC	No connection on XR-2126/2127.
	CPM	Enhanced Call Progress Mode selection on XR-2128 and XR-2129; CPM logic 0 for normal operation; CPM logic 1 scales down the low band filter by 2.5 for enhanced Call Progress Monitoring.
13	NC	No connection on XR-2126/2127.
	NFI	Notch filter insert pin on XR-2128; logic 0 for notch filter bypass (Bell 212A), logic 1 for inserting 550 Hz/1800 Hz notch (V.22).
	XTAL IN	XR-2129 only. On chip oscillator for input requiring 1.8432 MHz crystal connected across XTAL OUT and XTAL IN.
14	NC	No connection on XR-2126.
	$\overline{\text{ALB}}$	Analog loop back on XR-2127 and XR-2128. Same as Pin 9 on XR-2129.
	XTAL OUT	XR-2129 only. Unbuffered oscillator output.
15	TXC OUT	Transmit output signal on XR-2126, XR-2127, XR-2128.
	CLK OUT	1.8432 MHz buffered clock output on XR-2129.
16	NFO	Buffered notch filter output on XR-2126, XR-2127, XR-2128
	TXC OUT	Transmit output signal on XR-2129. Same as Pin 15 on XR-2126/2127/2128.
17	NSEL	Notch filter selection; logic 0 for 550 Hz, logic 1 for 1800 Hz.
18	TXC IN	Transmit input signal.
19	T(OUT)	Transmit uncommitted operational amplifier output.
20	T(+IN)	Non-inverting input of the transmit uncommitted operation amplifier.
21	T(−IN)	Inverting input of the transmit uncommitted operational amplifier.
22	CLK 2	Clock input 2 on XR-2126/2127/2128. 153.6 KHz TTL or CMOS clock.
	NFI	Notch filter insert pin on XR-2129, same as Pin 13 on XR-2128.
23	DGND	Digital ground.
24	RXC OUT	Receive output signal.

PRINCIPLES OF OPERATION

Low Band Filter

The low band filter is a 20th order switched capacitor filter consisting of a 10th order bandpass filter centered at 1200 Hz and a 10th order allpass filter centered at 1200 Hz. The allpass filter is a delay equalizer that provides compensation for the pass band group delay variation in the low band filter and half of the compromise line characteristics. See Figure 1 for the group delay response and Figure 2 for amplitude response.

In the Originate mode, the low band is used in the transmit path and in the Answer mode, it is used in the receive path. When analog loop back is used in the Originate mode, the low band filter will be in the test loop. In Call Progress Monitoring mode with SEL 2 (Pin 1) at logic 1, and CPM (Pin 12) at logic 0, the center frequency of the filter will be shifted down by a factor of 6 to 250 Hz. If CPM (Pin 12) is logic 1, then the center frequency will be scaled down by 2.5 to 480 Hz. This allows the precision dial tone of 350 Hz/440 Hz to pass, as well as audible ringing at 440 Hz/480 Hz and the busy tone and the precision reorder tone of 480 Hz/620 Hz.

High Band Filter

The high band filter is a 20th order switched capacitor filter consisting of a 10th order bandpass filter and a 10th order allpass filter centered at 2400 Hz. The allpass filter is a delay equalizer that provides compensation for the pass band group delay variation in the high band filter and half of the compromise line characteristics. See Figure 3 for the group delay response of the high band filter and Figure 2 for amplitude response.

In the Answer mode, the highband filter is used in the transmit path. In the Originate mode, it is used in the receive path.

When analog loop back is used in the Answer mode, the high band filter will be in the test loop. In Call Progress Monitoring mode with SEL 2 (Pin 1) at logic 1 and CPM (Pin 12) at logic 0, the center frequency will be scaled down by a factor of 6 to 400 Hz. If Pin 1 is at logic 0 or Pin 12 is at logic 1 this filter operates in the normal data mode.

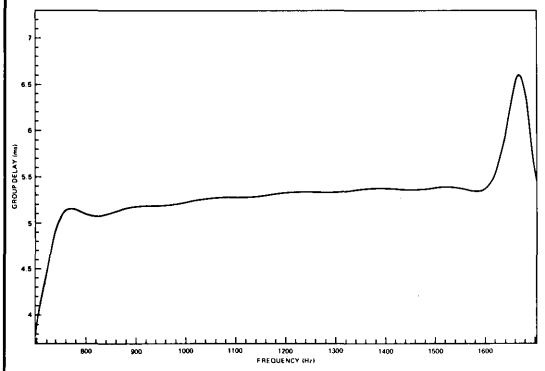


Figure 1. Low Band Group Delay Characteristics

In the XR-2129, a 10 dB gain is built into the receive filter path.

Transmit and Receive Output Smoothing Filters

The transmit and receive output smoothing filters are 2nd order, active RC, low pass filters that reconstruct the time sampled output signals characteristic of switched capacitor filters.

V.22 Notch Filter

The V.22 notch filter is a 4th order switched capacitor notch filter cascaded with the low band filter. The notch frequency of the filter is at 550 Hz when NSEL (Pin 17) is logic 0 and is shifted to 1800 Hz when NSEL is logic 1. In the XR-2128 and XR-2129, the notch filter is bypassed in the low band filter if NFI pin is logic 0. On the XR-2126/ 2127/ 2128, the notch filter output will always be available at Pin 16 (NFO). On the XR-2129, the NFO pin is not available; the notch filter will appear on Pin 24 (RXC OUT) if (NFI) is logic 1.

Worst Case Line Equalizer

The worst case line equalizer is an optional fixed compromise (amplitude and delay) equalizer designed for worst case line conditions (3002, C_O) in the high band receive mode. The equalizer is inserted in the high band receive path in operating modes 14 and 16 (see Table I).

Uncommitted Operational Amplifiers

Two uncommitted operational amplifiers are provided on all four versions of the modem filters. These are the transmit and receive amplifiers. They can be used as input anti-aliasing filters or as gain stages.

Analog Loop Back Test

When $\overline{ALB}$ (Pin 14) on XR-2127, XR-2128 and (Pin 9) on XR-2129 is logic 0, the modem transmit signal, TXC OUT (internally) is looped back to the modem through the RXC OUT pin with no signal present (MUTE) on TXC OUT (output pin). If the low band filter is to be tested, the MODE pin should be logic 0 and logic 1 if the highband filter is to be tested. The receive output smoothing filter will always be in the test loop regardless of the MODE level.

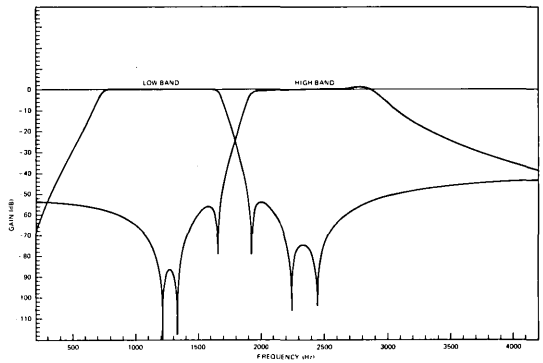


Figure 2. Low and High Band Amplitude Response

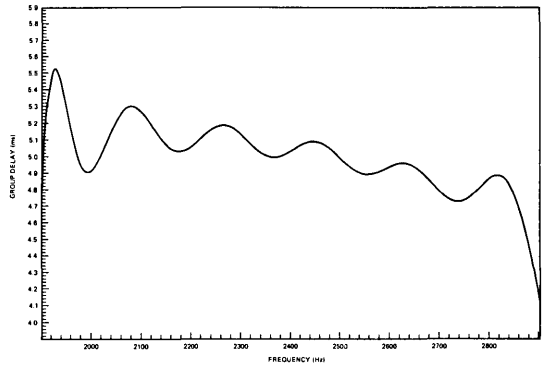


Figure 3. High Band Group Delay Characteristics

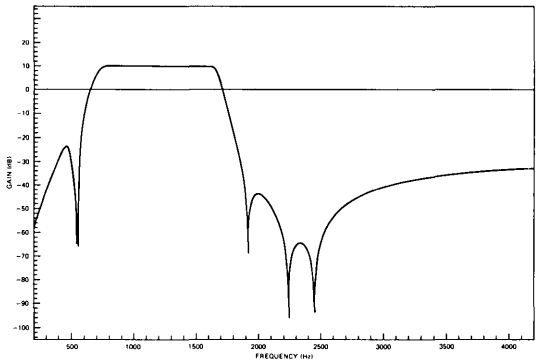


Figure 4A. XR-2129 with 500 Hz Notch

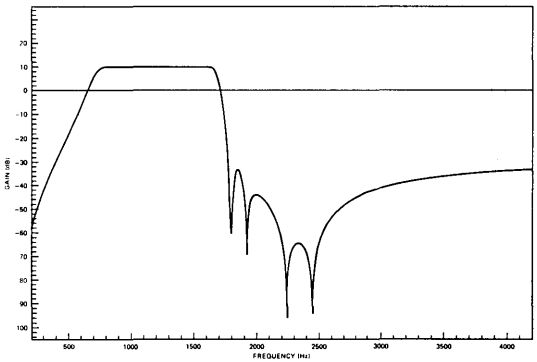


Figure 4B. XR-2129 with 1800 Hz Notch

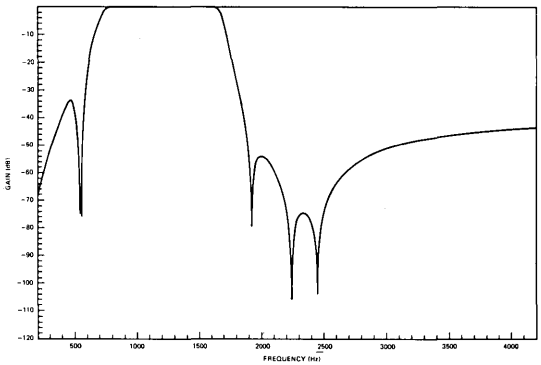


Figure 5A. XR-2126/2127/2128 with 500 Hz Notch

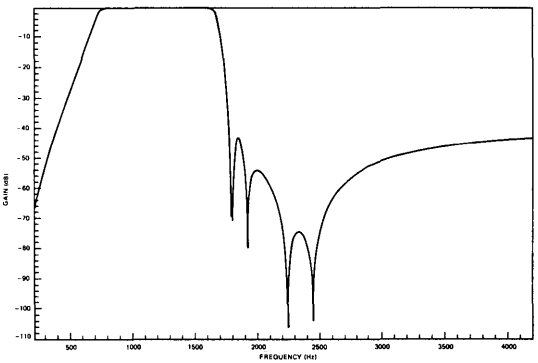


Figure 5B. XR-2126/2127/2128 with 1800 Hz Notch

Originate/Answer Mode Selection

When MODE (Pin 11) is logic 0, the modem filter operates in the Originate mode, transmitting in the low band and receiving in the high band. If MODE is logic 1, the modem filter operates in the answer mode; transmitting in the high band and receiving in the low band.

Transmit Squelch in Call Progess Mode

If CPM (Pin 12) is logic 1, the input of the transmit smoothing filter will be disconnected and shorted to ground, muting the transmitter. In the handshake sequence of the Bell 212A modem, this feature can be used to eliminate the transmit signal output.

Phone Line Status Monitor

If the logic levels on the control pins are shown in operation 15 (Table 1), the low band and high band filters will be bypassed; TXC OUT will be connected to TXC IN and RXC OUT will be connected to RXC IN. This feature can be used to monitor the status of the phone line. The output smoothing filters will always be in the TXC OUT and RXC OUT paths.

Clock Selection (Note 1)

On the XR-2126/2127/2128, SEL 1 (Pin 9) is used to select the internal clock divider (÷8/÷16) depending on the external clock frequency. SEL 1 is set at logic 0 for a 1.2288 MHz input clock and at logic 1 for a 2.4576 MHz clock on CLK 1 (Pin 4). A 153.6 KHz clock input is provided on CLK 2 (Pin 22). If used, CLK 1 (Pin 4) and SEL 1 (Pin 9) should be left open.

On the XR-2129, neither of these clock options are available. Instead, the device operates from an on chip clock oscillator which requires an external 1.8432 MHz crystal. Also available on the XR-2129, is a buffered 1.8432 MHz clock output on Pin 15.

TABLE I OPERATING MODES

OPERATION	CPM	SEL 2	$\overline{ALB}$	MODE	NFI	NSEL	TXC IN	TXC OUT	RXC IN	RXC OUT
0	0	0	1	0	0	X	L	L	H	H
1	0	0	1	1	0	X	H	H	L	L
2	0	0	0	0	0	X	L	MUTE	–	L
3	0	0	0	1	0	X	H	MUTE	–	H
4	0	1	1	0	X	X	L/6	L/6	H/6	H/6
5	0	1	1	1	X	X	H/6	H/6	L/6	L/6
6	0	1	0	0	X	X	L/6	L/6	H/6	L/6
7	0	1	0	1	X	X	H/6	H/6	L/6	H/6
8	1	0	1	0	X	X	–	MUTE	H	H
9	1	X	1	1	X	X	–	MUTE	L/2.5	L/2.5
10	1	X	0	0	X	X	–	MUTE	L/2.5	L/2.5
11	1	0	0	1	X	X	H	MUTE	–	H
12	0	0	1	1	1	0	H	H	L	L+ 550 Hz Notch
13	0	0	1	1	1	1	H	H	L	L+ 1800 Hz Notch
14	0	0	1	0	1	0	L	L	H	H+ WCL EQ
15	0	0	1	0	1	1	–	TXC IN	–	RXC IN
16	0	0	0	1	1	X	H	MUTE	–	H+ WCL EQ
17	0	0	0	0	1	0	L	MUTE	–	L+ 550 Hz Notch
18	0	0	0	0	1	1	L	MUTE	–	L+ 1800 Hz Notch

Note: MUTE means no signal present on transmitter output.
L refers to low band filter with center frequency of 1200 Hz.
H refers to high band filter with center frequency of 2400 Hz.
– means no filter connection.
+ means connection to both filters.
X means "don't care" condition.
N refers to Notch
Mode 15 is filter bypass mode where low band and high band filters are bypassed to monitor status of phone line.
WCL EQ is the Worst Case Line equalizer.

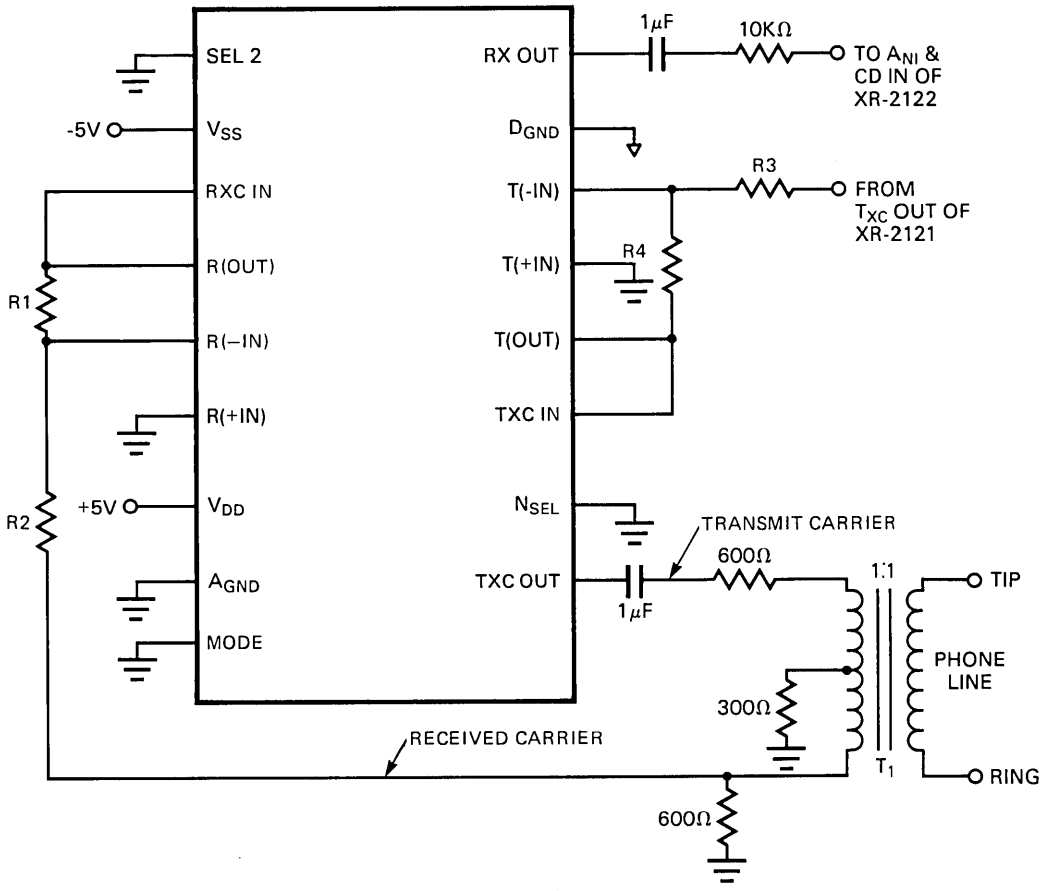


Figure 6. XR-2126/2127/2128/2129 Typical Connection

Normal Call Progress/Enhanced Call Progress

When SEL 2 (Pin 1) and CPM (Pin 12) are logic 0, the modem filter operates in the normal modem data mode. If either pin is logic 1, the modem filter operates in the Call Progress Monitoring mode. If SEL 2 is logic 1, and CPM is logic 0, the low band and high band filters will be scaled down by a factor of 6. If CPM is logic 1, the low band filter will be scaled down by a factor of 2.5 and, depending on the mode on MODE (Pin 11) and ALB (Pin 14), RXC OUT will either be the output of the scaled low band filter (L/2.5) or the unscaled high band filter.

Note 1: When using CLK1, CLK2 may be left open, tied to logic 1, or tied to logic 0. When using CLK2, CLK1 may be floated, tied to logic 1, or tied to logic 0.

TYPICAL APPLICATIONS

XR-2126/2127/2128/2129

The XR-2126 through XR-2129 have a number of common functions. Figure 6 shows typical connection of these functions by their mnemonic. The receive amplifier gain is set by $\frac{R1}{R2}$

and transmit amplifier gain is $\frac{R4}{R3}$

SEL 2

SEL 2 (pin 1) allows the sampling clock of the high band filter to be divided down by 6. This reduction of the sampling frequency provides filtering for the Call Progress Monitoring tones. SEL 2 is taken to a logic 1 for Call Progress Monitoring, and is returned to a logic 0 for normal high band filtering. When used in conjunction with the XR-2122 Bell 212A Type Demodulator, Call Progress Tones can be detected by the Energy Carrier Dectect pin of the XR-2122 (pin 17, CD OUT) and the tone identified by its cadence or interruption rate. This is the method used by most Call Progress Decoder ICs. It is assumed that a processor will monitor the Energy Carrier Detect pin of the XR-2122 and a look-up table will be available to match cadence with tone.

DESCRIPTIONS OF INPUTS AND OUTPUTS

VSS

VSS (pin 2) is the negative supply line to the IC. In most modem applications this will be −5 V.

RXC IN

RXC IN (pin 3) is the filter input for the received signal. This signal may be taken directly from the secondary side of the DAA isolation transformer, or may pass through a gain/anti-aliasing stage.

ROUT, R(−IN), R (+IN)

ROUT (pin 5), R(−IN) (pin 6), and R(+ IN) (pin 7) are respectively the output, inverting input, and non-inverting input of an additional onboard op amp. Figure 6 shows this op amp with gain setting resistors R_1 and R_2. This amplifier may also be used in an anti-aliasing filter. The cut off frequency is chosen to be approximately ¼ of the sampling frequency.

VDD

VDD (pin 8) is the positive supply line to the IC. In most modem applications, this will be 5 V DC.

AGND

AGND (pin 10) is the analog ground line of the IC. It should be connected to all other analog circuitry in a system design.

MODE

MODE (pin 11) sets the mode of operation for the filters. The filters consist of a high band filter with a center frequency at 2400 Hz and a low band filter with a center frequency at 1200 Hz. MODE is used to place the proper filter (2400 Hz or 1200 Hz center frequency) in the proper signal path (transmit or receive). Answer mode (MODE logic 1), places the low band filter in the receive path and the high band filter is the transmit path. Originate mode (MODE logic 0) places the high band filter in the receive path and the low band filter in the transmit path.

TXC OUT

TXC OUT (pin 15 for XR-2126/2127/2128 and pin 16 for XR-2129) provides the smoothed transmit signal output. This is typically taken through a 1 μF capacitor and into the secondary of an isolation transformer which represents a 1200 Ω load.

NSEL

NSEL (pin 17) is used to select one of two notch filters which are available for CCITT V.22 mode filtering. A logic 0 on NSEL selects the 550 Hz filter while a logic 1 on NSEL selects the 1800 Hz filter. Both notch filters are in the low band path and are used to attenuate the feedthrough of the transmitted guard tone through the transformer and into the Answer modem's received carrier input to a level much lower than the received carrier. (See Figures 4 and 5.)

TXC IN

TXC IN (pin 18) is the filter input for the transmitted signal.

This signal may be taken directly from TXC OUT (pin 4) of the XR-2121 Bell 212A Type Modulator.

T(OUT), T(+ IN), T(−IN)

T(OUT) (pin 19), T(+ IN) (pin 20), and T(− IN) (pin 21) are respectively the output, non-inverting input, and inverting input of an additional onboard op amp. Figure 6 shows this op amp with gain setting resistors R_3 and R_4. This op amp may also be used in an anti-aliasing filter. This cut off frequency is chosen to be approximately ¼ of the sampling frequency.

DGND

DGND (pin 23) is the digital ground line of the IC. It should be connected, single point, to all other digital circuitry in a system design.

RXC OUT

RXC OUT (pin 24) provides the smoothed received signal output. This is typically taken through a 1μF capacitor to the AGC circuit and CD IN of the XR-2122 Bell 212A Demodulator.

XR-2126

The XR-2126 has four features in addition to those common to the other members of this filter family. They are CLK 1, SEL 1, NFO, and CLK 2.

CLK 1

CLK 1 (pin 4) is one of two clock inputs for the XR-2126. Either clock input may be used (CLK 1 or CLK 2). CLK 1 will accept either a 2.4576 MHz input or a 1.2288 MHz input, depending on the state (logic 1 or logic 0 respectively) of SEL 1.

SEL 1

SEL 1 (pin 9) selects either the 2.4576 MHz clock or the 1.2288 MHz clock for input on pin 4, CLK 1.

NFO

NFO (pin 16) is the notch filter output.

CLK 2

CLK 2 (pin 22) takes a 153.6 KHz TTL or CMOS clock input.

XR-2127

The XR-2127 has five functions in addition to those common to the other members of this filter family. They are CLK 1, SEL 1, $\overline{\text{ALB}}$, NFO, and CLK 2.

CLK 1

CLK 1 (pin 4) is one of two clock inputs for the XR-2127. Either clock input may be used (CLK 1 or CLK 2). CLK 1 will accept either a 2.4576 MHz input or a 1.2288 MHz input, depending on the state (logic 1 or logic 0 respectively) of SEL 1.

SEL 1

SEL 1 (pin 9) selects either the 2.4576 MHz clock or the 1.2288 MHz clock for input on pin 4, CLK 1.

$\overline{\text{ALB}}$

$\overline{\text{ALB}}$ (pin 14) selects the Analog Loop Back mode when logic 0. A logic 1 on $\overline{\text{ALB}}$ allows normal operation.

NFO

NFO (pin 16) is the notch filter output.

CLK 2

CLK 2 (pin 22) takes a 153.6 KHz TTL or CMOS clock input.

XR-2128

The XR-2128 has seven functions in addition to those common to the other members of this filter family. They are CLK 1, SEL 1, CPM, NFI, $\overline{\text{ALB}}$, NFO, CLK 2.

CLK 1

CLK 1 (pin 4) is one of two clock inputs for the XR-2128. Either clock input may be used (CLK 1 or CLK 2) CLK 1 will accpet either a 2.4576 MHz input or a 1.2288 MHz input, depending on the state (high or low respectively) of SEL 1.

SEL 1

SEL 1 (pin 9) selects either the 2.4576 MHz clock or the 1.2288 MHz clock for input on pin 4, CLK 1.

CPM

CPM (pin 12) selects normal low band filter operation and divides by 2.5 for Call Progress Monitoring use. Logic is TTL with a logic 0 for normal low band operation and a logic 1 for low band divided by 2.5 for enhanced Call Progress Monitoring.

NFI

NFI (pin 13) selects the low band filter path. With NFI logic 1, the notch filter (550 Hz or 1800 Hz) selected by NSEL (pin 17) is inserted in the low band filter signal path. With NFI logic 0, the signal bypasses the notch filters.

$\overline{\text{ALB}}$

$\overline{\text{ALB}}$ (pin 14) selects the Analog Loop Back mode when logic 0. A high on $\overline{\text{ALB}}$ allows normal operation.

NFO

NFO (pin 16) is the notch filter output.

CLK 2

CLK 2 (pin 22) takes a 153.6 KHz TTL or CMOS clock.

XR-2129

The XR-2129 is designed specifically for use with the XR-212AS chip set (XR-2125, XR-2121, and XR-2122 excluding the XR-2120). This part requires no division of the 1.8432 MHz clock oscillator frequency. A 1.8432 MHz crystal is connected between XTAL IN and XTAL OUT (pins 13 and 14 respectively). Figure 7 shows the XR-212AS chip set using the XR-2129 in place of the XR-2120 to complete the Bell 212A Modem Signal Processor.

The XR-2129 has six functions in addition to those common to the other members of this filter family. They are $\overline{\text{ALB}}$, CPM, XTAL IN, XTAL OUT, CLK OUT, NFI.

$\overline{\text{ALB}}$

$\overline{\text{ALB}}$ (pin 9) selects the Analog Loop Back mode when logic 0. A logic 1 on $\overline{\text{ALB}}$ allows normal operation.

CPM

CPM (pin 12) is used to select either normal low band operation (fo = 1200 Hz) or low band divided by 2.5 (fo = 480 Hz). Logic is TTL with a logic 0 for normal low band operation and a logic 1 for low band divided by 2.5 for Call Progress Monitoring.

XTAL IN, XTAL OUT

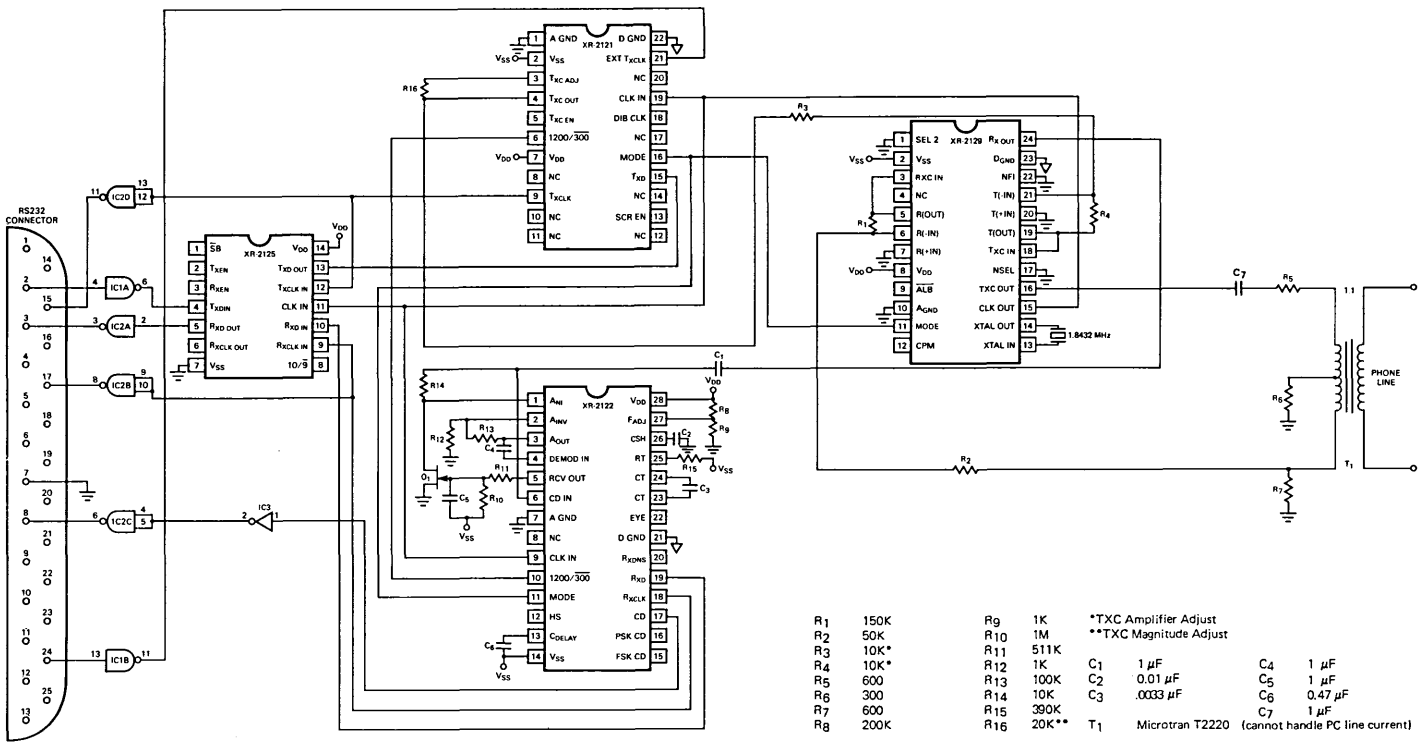
XTAL IN (pin 13) and XTAL OUT (pin 14) are the oscillator nodes across which a 1.8432 MHz crystal must be connected for operation. This 1.8432 MHz crystal is the same frequency crystal required for operation of the XR-2121, XR-2122, and XR-2125. The buffered output from this onboard oscillator is available from CLK OUT (pin 15). XTAL OUT (pin 14) offers the unbuffered oscillator output.

CLK OUT

CLK OUT (pin 15) provides the buffered output from the onboard oscillator. It can be used to drive other circuitry requiring a 1.8432 MHz clock.

NFI

NFI (pin 22) selects the low band filter path. With NFI logic 1, the notch filter (550 Hz or 1800 Hz) selected by NSEL (pin 17), is inserted in the low band filter signal path. With NFI logic 0, the notch filters are bypassed by the signal.



R_1	150K	R_9	1K	*TXC Amplifier Adjust	
R_2	50K	R_{10}	1M	**TXC Magnitude Adjust	
R_3	10K*	R_{11}	511K		
R_4	10K*	R_{12}	1K	C_1 1 μF	C_4 1 μF
R_5	600	R_{13}	100K	C_2 0.01 μF	C_5 1 μF
R_6	300	R_{14}	10K	C_3 .0033 μF	C_6 0.47 μF
R_7	600	R_{15}	390K		C_7 1 μF
R_8	200K	R_{16}	20K**	T_1 Microtran T2220 (cannot handle PC line current)	
				Q_1 2N4961	
				IC1 XR-1489	Resistors - 10%
				IC2 XR-1488	Capacitors - 20%
				IC3 CD-4069	

Figure 7. XR-212AS Bell 212A Modem Utilizing the XR-2129 Modem Filter

Section 3 – Data Communication Circuits

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

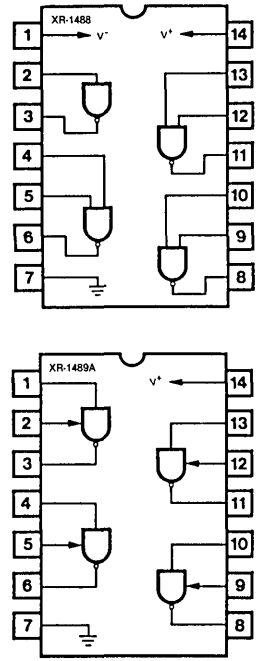
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.

XR-1488/1489A

ELECTRICAL CHARACTERISTICS

Test Conditions: (V^+ = +9.0 ±1% Vdc, V^- = −9.0 ±1% Vdc, T_A = 0°C to +70°C, unless otherwise noted)

PARAMETERS	XR-1488 LIMITS MIN	TYP	MAX	UNITS	CONDITIONS
Forward Input Current		1.0	1.6	mA	V_{in} = 0 Vdc
Reverse Input Current			10	μA	V_{in} = +5.0 Vdc
Output Voltage High				Vdc	V_{in} = 0.8 Vdc, R_L = 3.0 kΩ
V^+ = +9.0 Vdc, V^- = −9.0 Vdc	+6.0	+7.0			
V^+ = +13.2 Vdc, V^- = −13.2 Vdc	+9.0	+10.5			
Output Voltage Low				Vdc	V_{in} = 1.9 Vdc, R_L = 3.0 kΩ
V^+ = +9.0 Vdc, V^- = −9.0 Vdc	−6.0	−7.0			
V^+ = +13.2 Vdc, V^- = −13.2 Vdc	−9.0	−10.5			
Positive Output Short-Circuit Current	+6.0	+10	+12	mA	
Negative Output Short-Circuit Current	−6.0	−10	−12	mA	
Output Resistance V^+ = V^- = 0	300			Ohms	$\|V_O\|$ = ±2.0 V
Positive Supply Current (R_l = ∞)				mA	
V_{in} = 1.9 Vdc, V^+ = +9.0 Vdc		+15	+20		
V_{in} = 0.8 Vdc, V^+ = +9.0 Vdc		+4.5	+6.0		
V_{in} = 1.9 Vdc, V^+ = +12 Vdc		+19	+25		
V_{in} = 0.8 Vdc, V^+ = +12 Vdc		+5.5	+7.0		
V_{in} = 1.9 Vdc, V^+ = +15 Vdc			+34		
V_{in} = 0.8 Vdc, V^+ = +15 Vdc			+12		
Negative Supply Current (R_L = ∞)				mA	
V_{in} = 1.9 Vdc, V^- = −9.0 Vdc		−13	−17		
V_{in} = 0.8 Vdc, V^- = −9.0 Vdc		0	0		
V_{in} = 1.9 Vdc, V^- = −12 Vdc		−18	−23		
V_{in} = 0.8 Vdc, V^- = −12 Vdc		0	0		
V_{in} = 1.9 Vdc, V^- = −15 Vdc			−34		
V_{in} = 0.8 Vdc, V^- = −15 Vdc			−2.5		
Power Dissipation				mW	
V^+ = 9.0 Vdc, V^- = −9.0 Vdc			333		
V^+ = 12 Vdc, V^- = 12 Vdc			576		
Switching Characteristics (V^+ = +9.0 ±1% Vdc, V^- = −9.0 ±1% Vdc, T_A = +25°C)					
Propagation Delay time (t_{pd}^+)		150	200	ns	Z_L = 3.0k and 15 pF
Fall Time		45	75	ns	Z_L = 3.0k and 15 pF
Propagation Delay Time (t_{pd}^-)		65	120	ns	Z_L = 3.0k and 15 pF
Rise Time		55	100	ns	Z_L = 3.0k and 15 pF

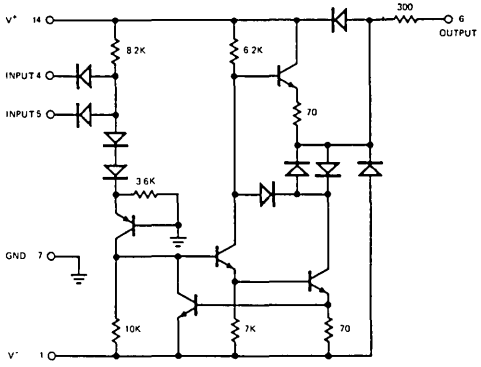
ELECTRICAL CHARACTERISTICS

Test Conditions: Response control pin is open. (V^+ = +5.0 Vdc ±1%, T_A = 0°C to +75°C, unless otherwise noted)

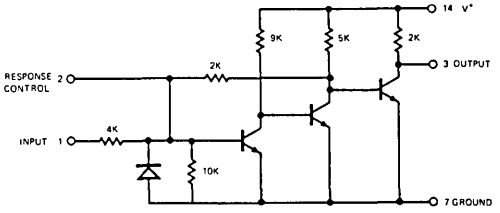
PARAMETERS	XR-1489 LIMITS MIN	TYP	MAX	UNITS	CONDITIONS
Positive Input Current V_{in} = +25 Vdc V_{in} = +3.0 Vdc	 3.6 0.43		 8.3	mA	
Negative Input Current V_{in} = −25 Vdc V_{in} = −3.0 Vdc	 −3.6 −0.43		 − 8.3	mA	
Input Turn-On Threshold Voltage T_A = +25°C, V_{OL} ≤0.45 V	1.75	1.95	2.25	Vdc	
Input Turn-Off Threshold Voltage T_A = +25°C, V_{OH} ≥2.5 V	0.75	0.8	1.25	Vdc	I_L = −0.5 mA
Output Voltage High V_{in} = 0.75 V Input Open Circuit	 2.6 2.6	 4.0 4.0	 5.0 5.0	Vdc	I_L = −0.5 mA
Output Voltage Low		0.2	0.45	Vdc	V_{in} = 3.0 V, I_L = 10 mA
Output Short-Circuit Current		3.0		mA	
Power Supply Current		20	26	mA	V_{in} = +5.0 Vdc
Power Dissipation		100	130	mW	V_{in} = +5.0 Vdc
Switching Characteristics (V^+ = 5.0 Vdc ±1%, T_A = +25°C)					
Propagation Delay Time (t_{PLH})		25	85	ns	R_L = 3.9 kΩ
Rise Time		120	175	ns	R_L = 3.9 kΩ
Propagation Delay Time (t_{PHL})		25	50	ns	R_L = 390 kΩ
Fall Time		10	20	ns	R_L = 390 kΩ

EQUIVALENT SCHEMATIC DIAGRAMS

XR-1488



XR-1489A



EXAR

Section 4 – Computer Peripheral Circuits

Hard Disk Read/Write

GENERAL DESCRIPTION

The XR-117 is a high speed head interface integrated circuit for hard disk drives, performing both read and write functions. The XR-117 is compatible with 3½" to 14" single and multiple platter drives, and features high bandwidth, large dynamic range, and low noise. Several packaging options extend usefulness to applications requiring two, four, or six center-tapped read/write heads; multiple devices are easily cascaded for drives with more heads.

The XR-117, manufactured with a high speed bipolar process, operates on +5 V and +12 V.

FEATURES

Complete Head Interfacing Functions, Read and Write
High Bandwidth and Dynamic Range
Low Noise
Available in Two, Four, and Six Head Versions
Easily Cascaded for Larger Systems
Power Monitor with Automatic Disable
TTL Compatible Inputs

APPLICATIONS

Single or Multiple Platter Hard Disk Drives

ABSOLUTE MAXIMUM RATINGS

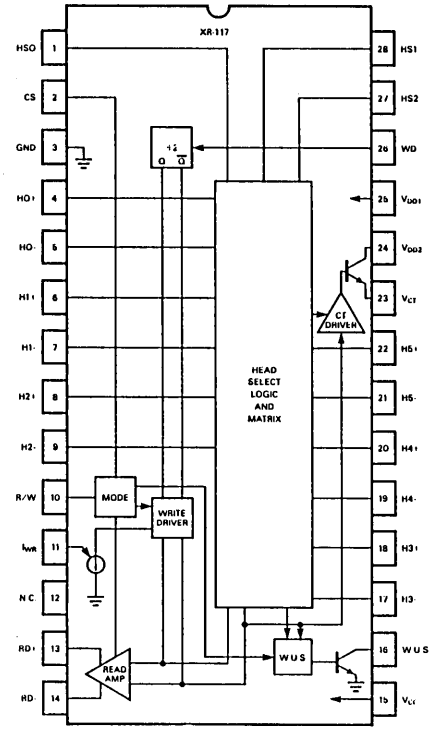
V_{DD1} and V_{DD2}	15 V
V_{CC}	6 V
Digital Inputs	−0.3 V to V_{CC} +0.3 V
Write Current	60 mA
Junction Temperature	150°C
Storage Temperature	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-117-2CP	Plastic	0°C to 70°C
XR-117-4CP	Plastic	0°C to 70°C
XR-117-6CP	Plastic	0°C to 70°C
XR-117-xCN	Ceramic	0°C to 70°C
XR-117-xCQ*	Surface Mount Quad	0°C to 70°C
XR-117-xMD*	Surface Mount	0°C to 70°C
XR-117-x *	PLCC	0°C to 70°C

x = 2, 4, or 6, depending on number of heads required
* = contact factory for availability

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

Four major blocks comprise the XR-117: a multiplexer for head selection, write data control circuitry, read signal amplifiers and buffers, and a power supply monitor that disables the device whenever improper supply voltages are present. Designed for six read/write heads, the XR-117 is also available in smaller packages for systems requiring only two or four heads. The 30 MHz minimum bandwidth facilitates data rates exceeding 25 Mbits per second.

Less than 2 $nV/\sqrt{Hz}$ (nominal) noise allows error free operation with small input signals. Up to 50 mA of write current output means the disk signal can be large, further enhancing the readback signal-to-noise ratio for very low error rates.

Cascading multiple XR-117s is accomplished by alternately enabling and disabling devices via the chip select (CS) pin. Guaranteed write current tolerances allow close write matching between devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 12$ V, $V_{CC} = 5$ V, $R_W = 3.1$ kΩ, $L_h = 10$ μH, $R_d = 750$ Ω, C_L (R_{D+}, R_{D-}), ≤ 20 pF, Data Rate = 5 MHz.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
DC CHARACTERISTICS						
I_{CC}	Supply Current			25	mA	V_{CC} = 5.5 V, Read or Idle Mode
				30	mA	V_{CC} = 5.5 V, Write Mode
I_{DD}	Supply Current			25	mA	V_{DD} = 13.2 V, Idle Mode
				50	mA	V_{DD} = 13.2 V, Read Mode
				30	mA	V_{DD} = 13.2 V, Write Mode, I_W = 0 mA
P_D	Power Dissipation			400	mW	V_{CC} - 5.5 V, V_{DD} = 13.2 V, Idle Mode
				600	mW	Read Mode
				700	mW	Write Mode, I_W = 50 mA, R_{CT} = 130 Ω
				1050	mW	Write Mode, I_W = 50 mA, R_{CT} = 0 Ω
V_{CT}	Center Tap Voltage		4.0		V	
			6.0		V	
WUS	Write Unsafe Output					
V_{OL}	Saturation Voltage		0.1	0.5	V	I_{OL} = 8 mA
I_{OH}	Leakage Current			100	μA	V_{OH} = 5 V
DIGITAL INPUTS						
V_{IL}	Input "Low" Voltage			0.8	V	
V_{IH}	Input "High" Voltage	2.0			V	
I_{IL}	Input Current, Low	−0.4			mA	
I_{IH}	Input Current, High			100	μA	
WRITE CHARACTERISTICS						
	Write Current Accuracy	−5		+5	%	Note 1
I_W	Recommended Write Current Range	10	45	50	mA	
	Differential Head Voltage Swing	5.7	10		Vpeak	
	Unselected Differential Head Current			2	mApeak	
	Differential Output Capacitance			15	pF	
	Differential Output Resistance	10			kΩ	
	WD Rate (Transisition Frequency)	125	500	625	kHz	
K_I	Current Source Factor		20			$K_I = I_W$/(Current through R_W)

READ CHARACTERISTICS						
A_V	Differential Voltage Gain	80	100	120	V/V	V_{in} = 1 mVp-p @ 300 kHz $R_{L+} = R_{L-}$ = 1 kΩ
R_{in}	Differential Input Resistance	2			kΩ	
C_{in}	Differential Input Capacitance			23	pF	f = 5 MHz
e_{ni}	Input Noise Voltage		1.5	2.1	$nV/\sqrt{Hz}$	L_h = 0, R_h = 0, BW = 15 MHz
BW	Bandwidth	30	55		MHz	−3dB point $\|Zs\| < 5\Omega$, V_{in} = 1 mVp-p
I_B	Input Bias Current			45	μA	
CMRR	Common Mode Rejection Ratio	50			dB	$V_{CM} = V_{CT}$ + 100 mVp-p at 5 MHz
PSRR	Power Supply Rejection Ratio	45			dB	100 mVp-p at 5 MHz Superimposed on V_{DD1}, V_{DD2}, or V_{CC}
	Channel Separation	45			dB	Unselected Channel: V_{in} = 100 mVp-p at 5 MHz Selected Channel: V_{in} = 0 V
	Output Offset Voltage	−480	± 50	480	mV	
V_{CM}	Common Mode Output Voltage	5	6	7	V	
SWITCHING CHARACTERISTICS						
R/W	Read to Write		0.1	1	μS	**Note 2**
	Write to Read		0.1	1	μS	Note 3, Note 4
CS CS	Start-Up Delay		0.1	1	μS	Delay to 90% of I_W or to 90% of 100 mV 10 MHz read signal envelope.
	Inhibit Delay		0.1	1	μS	Note 4
	Head Switching Delay		0.1	1	μS	Note 3 Switching between any heads.
WUS	Write Unsafe Safe to Unsafe	1.6	2.5	8.0	μS	I_W = 50 mA, See Fig. 1, TD1
	Unsafe to Safe		0.2	1	μS	I_W = 20 mA, See Fig. 2, TD2
I_W	Head Current					
	Propagation Delay		4	25	nS	L_h = 0 μH, R_h = 0 Ω, Note 5,
	Asymmetry			2	nS	Note 6 See Fig. 1, TD3
	Rise or Fall Time		9	20	nS	10% to 90% or 90% to 10% points

Note 1: Error from $I_W = \frac{140}{R_W}(\frac{V}{\Omega})$
Note 2: Delay to 90% of I_W
Note 3: Delay to 90% of 100 mVp-p 10 MHz read single envelope
Note 4: Delay to 90% decay of I_W
Note 5: From 50% points
Note 6: Input WD has 50% duty cycle and 1 nS rise and fall times.

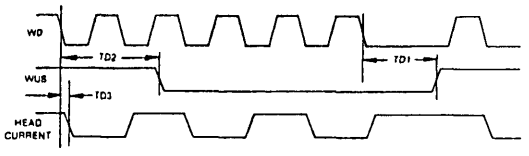


Figure 1. Write Mode Timing Diagram

CAUTION: This device may be damaged by electrostatic discharge. ESD precautions should be taken.

PRINCIPLES OF OPERATION

Write Mode

Before writing may begin, both chip select ($\overline{CS}$) and Read/Write (R/W) must be pulled low. The desired head, selected by HS0 to HS2, is driven by a differential current sink of magnitude I_W set by R_{IW}. Input data is applied to a falling edge triggered toggle flip-flop, which in turn selects the active side of the center tapped write head.

Current is sourced through the center tap driver, V_{CT}, which is "high" in the write mode. Write unsafe (WUS) signals the disk controller whenever one of six error conditions exist and writing should be discontinued. The six faults are: open head, open center tap, no write current, write data frequency too low, device unselected, and writing attempted while the device is in the read mode.

Read Mode

Pulling R/W high enables the data readback mode. A low noise, high gain differential amplifier increases the weak signal amplitude and provides low output impedance.

APPLICATIONS INFORMATION

As will all high frequency, high gain systems, layout is critical. Lead lengths should be minimized and supplies should be well bypassed. The XR-117 is available in small outline surface mount and flat-pak packages facilitating installation near the drive heads. Its high frequency characteristics lead to a certain degree of electrostatic discharge (ESD) susceptability, so static reducing precautions should be taken.

Write Mode Design Considerations

Write current, I_W, typically between 20 mA and 50 mA, is determined by a single resistor, R_{IW}.

$$R_{IW} = \frac{140{,}000}{I_W}$$

where I_W is in mA and R_{IW} is in ohms.

The V_{CC} supply monitor disables writing when V_{CC} drops below about 4 V.

Device power dissipation is reduced by a resistor, R_{CT}, connecting V_{DD2} to the +12 V supply. Some of the center tap driver voltage drop then is across the resistor.

With the nominal 12 V supply, R_{CT}, is calculated as

$$R_{CT} = 130\ (\frac{55}{I_W})$$

where R_{CT} is in ohms and I_W is in milliamperes.

Internal dissipation reduction is primarily a consideration with high write current levels and small outline packages. For low write currents, R_{CT} may be deleted, with V_{DD2} directly connected to the supply.

In addition to the individual head damping resistors, a ferrite bead around the V_{CT} line to the heads will further reduce overshoot and ringing in extreme conditions.

Write unsafe (WUS) pulls high whenever one or more of six write error conditions exist. Four conditions; open head, open center tap, no write current and write data transition rate too low, are detected with a differential capacitor charge/discharge circuit. Device unselected and read mode digital conditons also force WUS high.

After removal of the fault condition, two negative write data transitions are required to clear WUS. This output is for indication only, intended for signaling a controller, and does not directly impede device operation. A pull-up resistor of about 2 kΩ is necessary for operation of this open collector output.

Read Mode Design Considerations

The read amp has a fully differential input and output and provides approximately 100 V/V gain. Its 30 MHz minimum bandwidth and low noise characteristics (1.5nV/$\sqrt{Hz}$ typical) provide substantial margins in most drives. The ouput should be AC coupled to delete the approximately 6 V output common mode voltage. Best results are obtained by limiting load capacitance to 20 pF and load current to 100 μA.

Floppy Disk Write Amplifier

GENERAL DESCRIPTION

The XR-2247/2247A is a write amplifier designed to provide the complete interface between write data signals and tunnel-erase magnetic heads. Although primarily intended for floppy disk drive systems, the XR-2247/2247A can also be used in other magnetic media systems such as tape drives. To minimize external part count for dual head systems, complete head switching is does internally with emitter-coupled PNP transistors in the XR-2247 and diodes (which offer improved broadband noise characteristics) in the XR-2247A. Write and erase currents are each externally programmable with a single resistor. Also included is circuitry for inner track write current compensation. To prevent false write current outputs during power-on, an inhibit input has been provided. Erase turn-on and turn-off times are each externally programmable.

The XR-2247/2247A, available in a 22-Pin DIP, operates from a single power supply and provides TTL compatible inputs.

FEATURES

Fully Programmable Write and Erase Currents
Fully Programmable Erase Turn-on/Turn-off Times
Internal Head Switching for Dual Head Drives
Single Supply Operation
Inner Track Write Current Compensation
Inhibit Input
TTL Compatible Inputs
Low External Parts Count

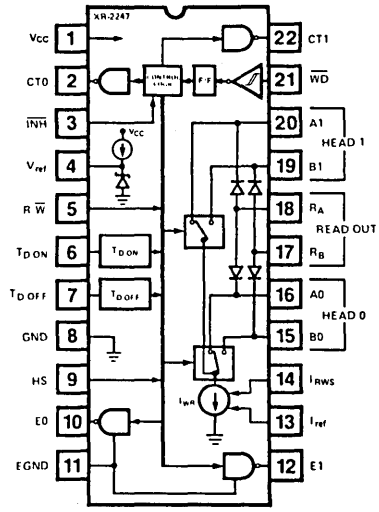
APPLICATIONS

Floppy Disk Drives
Single/Dual Head Systems
Magnetic Tape Write Amplifier

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (Pin 1)	16 V dc
Input Voltage (all digital inputs)	−0.2V to +16 V dc
Reference Current (Pin 4)	10 mA dc
Output Current (Pins 2, 10, 12, 22)	100 mA dc
Storage Temperature	−55°C to +150°C
Operating Junction Temperature	150°C
Power Dissipation	750 mW
Derate Above 25°C	6.5 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2247CN	Ceramic	0°C to +70°C
XR-2247CP	Plastic	0°C to +70°C
XR-2247ACN	Ceramic	0°C to +70°C
XR-2247ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2247/2247A accepts a serial binary data stream input. With the write mode selected, negative transitions of this input signal will alternately provide write current to each half of the head. The XR-2247/2247A provides two sets of current outputs for dual head drives, with the head select (HS) control determining which is active. The write current is externally programmed with a resistor between the internal voltage reference and the current setting input. Two high-current open-collector outputs provide the erase coil drive. Turn-on and turn-off delay circuitry is provided for these outputs, with the delay externally programmed.

An inhibit input ($\overline{INH}$) is provided to disable the outputs to prevent false writing during power-on. With the read mode selected, internal head switching channels the proper head to the read outputs.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 12V, R_{ref} = 10 kΩ, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
I_{CC}	Power Supply Current	–	13	20	mA	V_{CC} = 9V to 16V
V_{CC}	Power Supply Range	9	12	16	V	
DIGITAL INPUT VOLTAGE						
V_{IH}	High Level Voltage	2.0	–	–	V	
V_{IL}	Low Level Voltage	–	–	0.8	V	
DIGITAL INPUT CURRENTS						
I_{IH}	High Level Current	–	0.1	4.0	μA	V_I = 2.4V
I_{IL}	Low Level Current	–	15	100	μA	
CT0 or CT1 OUTPUTS						
V_{CTH}	Output High Voltage	9.5	10.2	–	V	I_{out} = 100 mA
V_{CTL}	Output Low Voltage	–	0.1	0.2	V	I_{out} = 1 mA
E0 or E1 OUTPUTS						
I_{OL}	Output High Leakage	–	0.01	20	μA	V_{CC} = 16V
V_{OEL}	Output Low Voltage	–	1.0	1.5	V	I_{out} = 100 mA
$T_{D\ ON}$	Erase Turn-on Delay	0.45	0.5	0.55	mS	R_{D1} = 4.55 KΩ, C_{D1} = 0.1 μF
$T_{D\ OFF}$	Erase Turn-off Delay	0.9	1.0	1.1	mS	R_{D2} = 9.54 KΩ, C_{D2} = 0.1 μF
CURRENT SOURCE						
V_{ref}	Reference - Pin 4	8.0	8.5	9.0	V	I_{ref} = 1 mA
		7.8	8.2	8.8	V	I_{ref} = 10 mA
V_{mir}	I_{ref} Input Voltage - Pin 13	0.65	0.80	0.95	V	I_{ref} = 1 mA
I_{WRL}	Write Current Off Leakage — Pins 15, 16, 19, 20	–	0.03	15	μA	
V_{comp}	Current Sink Compliance — Pins 15, 16, 19, 20	7	–	12	V	
I_{WR}	Write Current w/o I_{RWS} — Pins 15, 16, 19, 20	3.7	4.1	4.5	mA	I_{RWS} = Low
I_{WRS}	Write Current with I_{RWS} — Pins 15, 16, 19, 20	5.1	5.7	6.3	mA	I_{RWS} = High
ΔI_{WR}	Difference in Write Current	–	–	40	μA	I_{RWS} = Low (Note 1)
READ OUTPUT						
e_{no}	Differential Noise Voltage at Read Output —					
	2247	–	4	–	μV_{rms}	BW = 10 Hz to 1.0 MHz
	2247A	–	1	–	μV_{rms}	I_B = 200 μA

Note 1: Difference = $|(I_{PIN\ 15,16} - I_{PIN\ 19,20})|$

AC SWITCHING CHARACTERISTICS

Test Conditions: Test Circuit of Figure 4, V_{CC} = 12V, T_A = 25°C, I_{RWS} = 0.4V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{d1}	Delay from R/$\overline{W}$ going low through 0.8V to CT0 or CT1 going high through 9.0V.	–	0.11	–	μs	R/$\overline{W}$ signal at Pin 5: f = 50 KHz, 50% duty cycle, amplitude = 0.4V to 2.4V See Figure 1
t_{d2}	Delay from R/$\overline{W}$ going low through 0.8V to A0, A1, B0, or B1 settling to final value.	–	0.40	–	μs	
t_{d3}	Delay from R/$\overline{W}$ going high through 2.0V to A0, A1, B0, or B1 settling to final value.	–	0.20	–	μs	
t_{d4}	Delay from R/$\overline{W}$ going low through 0.8V to V_{ref} going high through 8.0V.	–	0.13	–	μs	
t_{d5}	Delay from R/$\overline{W}$ going high through 2.0V to V_{ref} going low through 1.0V.	–	3.50	–	μs	
t_{d6}	Delay from HS going high through 2.0V to CT0 going high through 9.0V.	–	0.12	–	μs	HS signal at Pin 9: f = 50 KHz, 50% duty cycle, amplitude = 0.4V to 2.4V See Figure 1
t_{d7}	Delay from HS going high through 2.0V to CT1 going low through 1.0V.	–	0.11	–	μs	
t_{d8}	Delay from HS going low through 0.8V to CT0 going low through 1.0V.	–	0.10	–	μs	
t_{d9}	Delay from HS going low through 0.8V to CT1 going high through 9.0V.	–	0.20	–	μs	
t_{10}	$\overline{WD}$ low hold time.	150	–	–	ns	See Figure 1
t_{11}	$\overline{WD}$ high hold time.	500	–	–	ns	
t_{d12}	Delay from $\overline{WD}$ going low through 1.4V to A0 or A1 turning on through 50%.	–	75	–	ns	See Figure 3
t_{d13}	Delay from $\overline{WD}$ going low through 1.4V to B0 or B1 turning off through 50%.	–	75	–	ns	
t_{d14}	Delay from $\overline{WD}$ going low through 1.4V to A0 or A1 turning off through 50%.	–	75	–	ns	
t_{d15}	Delay from $\overline{WD}$ going low through 1.4V to B0 or B1 turning on through 50%.	–	75	–	ns	
t_{16}	Turn-on time, 10% to 90%, of A0 or A1	–	50	–	ns	
t_{17}	Turn-on time, 10% to 90%, of B0 or B1	–	50	–	ns	
t_{18}	Turn-off time, 90% to 10%, of A0 or A1	–	50	–	ns	
t_{19}	Turn-off time, 90% to 10%, of B0 or B1	–	50	–	ns	

PRINCIPLES OF OPERATION

The functions of the input and output pins are as follows:

Head Select — HS (Pin 9): The head select input makes a selection between head 0 and head 1. It channels the proper drive signals to the CT and E pins.

Read/Write — R/$\overline{W}$ (Pin 5): This input selects read data when high, and write data when low.

Write Data — $\overline{WD}$ (Pin 21): Digital data to be written to the head is fed into this pin. Data is alternately written to A0, B0 or A1, B1 on negative transitions of $\overline{WD}$.

I_{RW} Select — I_{RWS} (Pin 14): This pin is used to provide a digital control for the amount of current written to the head. It is used to provide inner track compensation. When low, the head current is that dictated, by R_{ref}. When driven high, the head current is increased by 40%.

V_{ref} (Pin 4), I_{ref} (Pin 13): A resistor, R_{ref}, connected between these pins control the write current. With I_{RWS} low, the write current is approximately five times the R_{ref} current, and seven times with I_{RWS} high.

Center Tap 0 — CT0 (Pin 2), Center Tap 1 - CT1 (Pin 22): These pins are high-current outputs used to apply V_{CC} to the center taps of the head. With R/$\overline{W}$ low, both CT outputs are in the high state.

Erase 0 — E0 (Pin 10), Erase 1 — E1 (Pin 12): These pins provide high-current open-collector outputs for supplying erase current to the head. With R/$\overline{W}$ low, the erase output selected by HS will be low with the other open. With R/$\overline{W}$ high, both E0 and E1 will be open or high impedance outputs.

A0 (Pin 16), B0 (Pin 15): These pins provide the write current to the head. A0 is connected to one side of the head, with B0 connected to the other. They provide out-of-phase drive to each end of the head write coil. These outputs are selected when HS is low.

A1 (Pin 20), B1 (Pin 19): These outputs provide the same current-sink drive as A0/B0, except to the other head when HS is high.

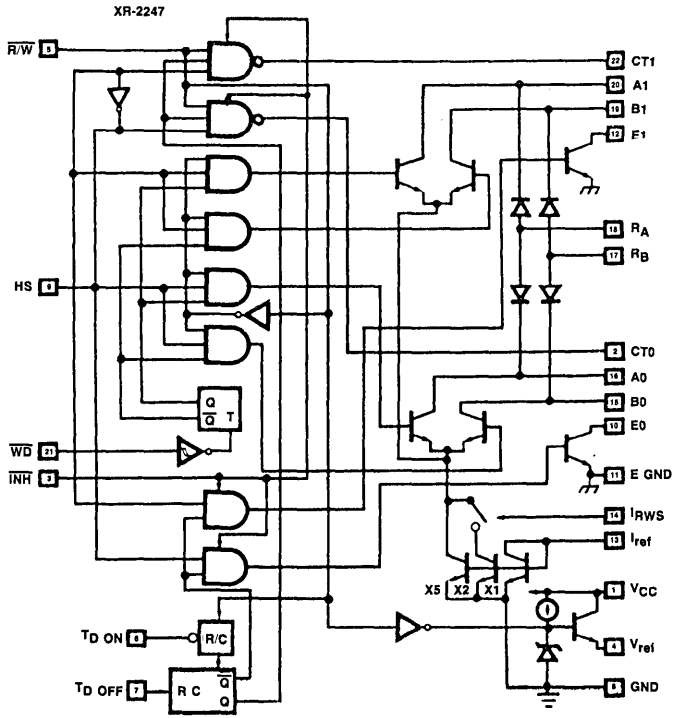
R_A (Pin 18), R_B (Pin 17): These are read signal outputs to be connected to the read amplifier inputs. With R/$\overline{W}$ high, the head selected by HS will be connected to these pins.

$\overline{Inhibit}$ — $\overline{INH}$ (Pin 3): When active (low), this input will turn off both erase and center taps to avoid erroneous outputs during power-on.

T_D ON (Pin 6), T_D OFF (Pin 7): The resistor, R_D, and capacitor, C_D, combination of these pins will set the turn-on and turn-off times of the erase outputs. Figure 5 shows the connection of these components, with section 3 of the applications information describing the time as a function of R_D and C_D.

4

EQUIVALENT SCHEMATIC DIAGRAM



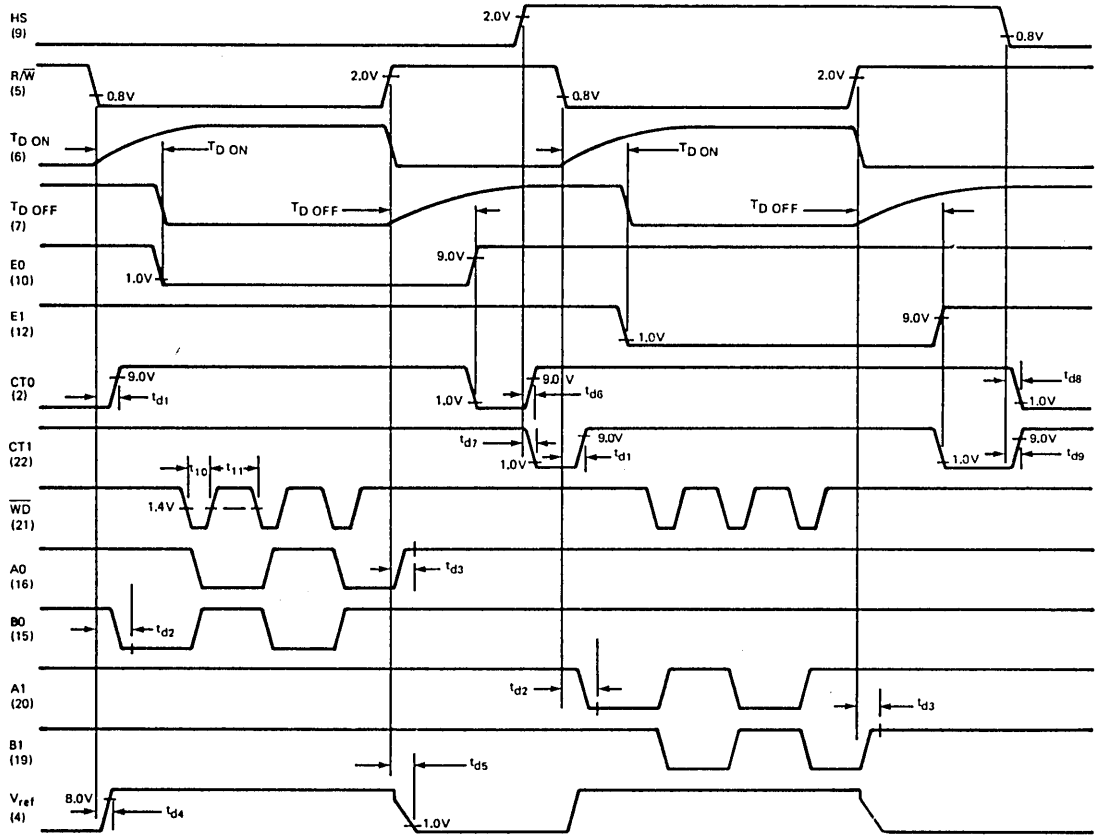


Figure 1. Timing Diagram

INPUT			OUTPUT				
$\overline{INH}$	R/$\overline{W}$	HS	CT0	CT1	E0	E1	V_{ref}
1	0	0	H	H	Low	Open	H
1	0	1	H	H	Open	Low	H
1	1	0	L	H	Open	Open	L
1	1	1	H	L	Open	Open	L
0	–	–	L*	L*	Open	Open	H

*High impedance

Figure 2. Truth Table

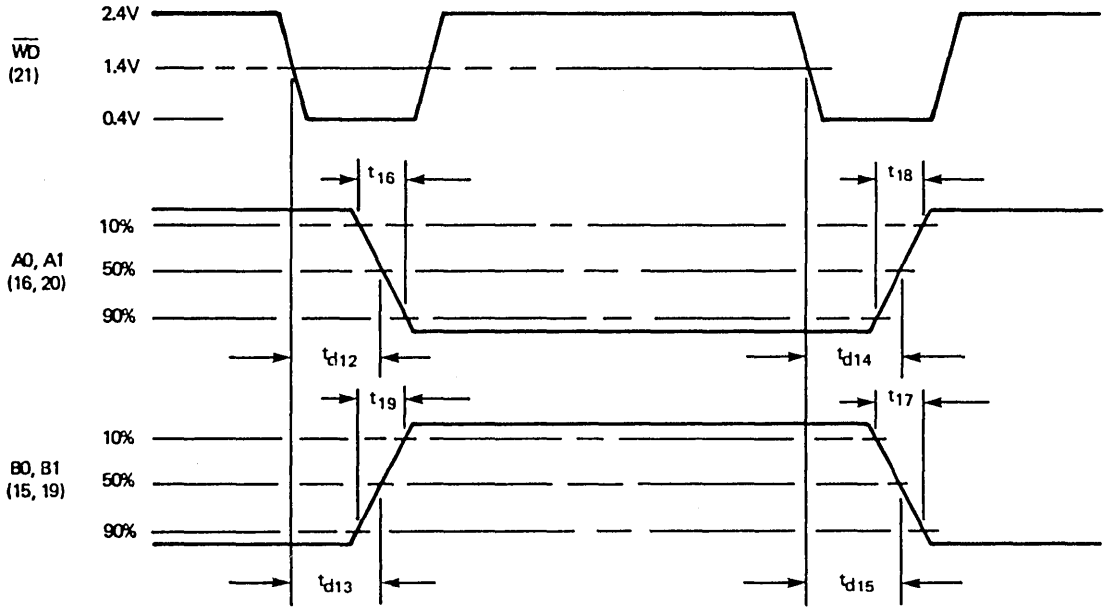


Figure 3. Write Current Output Characteristics

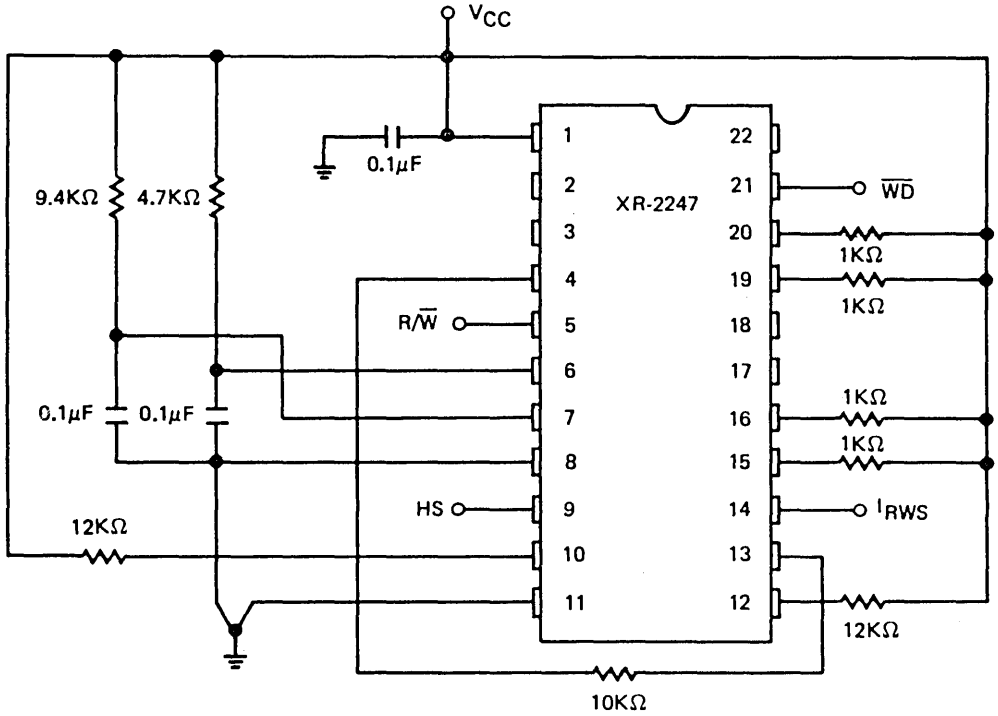


Figure 4. Test Circuit for AC Switching Characteristics

APPLICATIONS INFORMATION

A typical dual head connection of the XR-2247 in a floppy disk system is shown in Figure 5. Referring to Figure 5 and the electrical characteristics, the external components are calculated as follows:

1) Write Current, I_{WR}

$$I_{WR} = (5.3)\left(\frac{V_{ref} - V_{mir}}{R_{ref}}\right) \quad I_{RWS} = \text{Low}$$

Given I_{WR} = 4.1 mA, R_{ref} = 10 kΩ
I_{ref}, the current into Pin 13, should not exceed 2.0 mA.

2) Erase Current, I_E

$$I_E = \frac{V_{CTH} - V_{OEL}}{R_E} \approx \frac{V_{CC} - 2V}{R_E}$$

Given I_E = 50 mA and V_{CC} = 12V, R_E = 200Ω ½ W

3) Erase Delay Time, $T_{D\ ON}$ and $T_{D\ OFF}$

$T_{D\ ON} \approx 1.1\ (R_{D1} \times C_{D1})$
$T_{D\ OFF} \approx 1.05\ (R_{D2} \times C_{D2})$

Given $T_{D\ ON}$ = 0.5 ms and $T_{D\ OFF}$ = 1.0 ms,

R_{D1} = 4.55 kΩ, R_{D2} = 9.54 kΩ
$C_{D1} = C_{D2}$ = 0.1 μF

Control of the erase outputs can also be done from an external source by grounding Pin 6 and driving Pin 7 directly. The selected erase output will be on when Pin 7 is low and off when Pin 7 is high. This input is not TTL compatible, however, with the threshold voltage being approximately ⅔ V_{CC}.

4) Resistors R_{WD} are used to damp any ringing that may occur when the write current transitions are applied to the head. Their value is determined by the head characteristics and the desired damping.

R_{RD} is used to provide additional damping in the read mode if this is desired. Usually, R_{RD} is only used with the XR-2247A where the head switching diodes make the total read damping resistance approximately $R_{RD}//R_{WD}$. In the XR-2247, the transistors used for head switching act to buffer R_{RD} from the head.

Resistors R_B are used to bias the head switching network in the read mode and their value is selected to provide currents in the 100 μA to 300 μA range.

5) When in the read mode, digital signals appearing along the $\overline{WD}$ line (Pin 21) can couple externally through stray capacitances into the read signal coming from the head. It is recommended that $\overline{WD}$ be held low while reading.

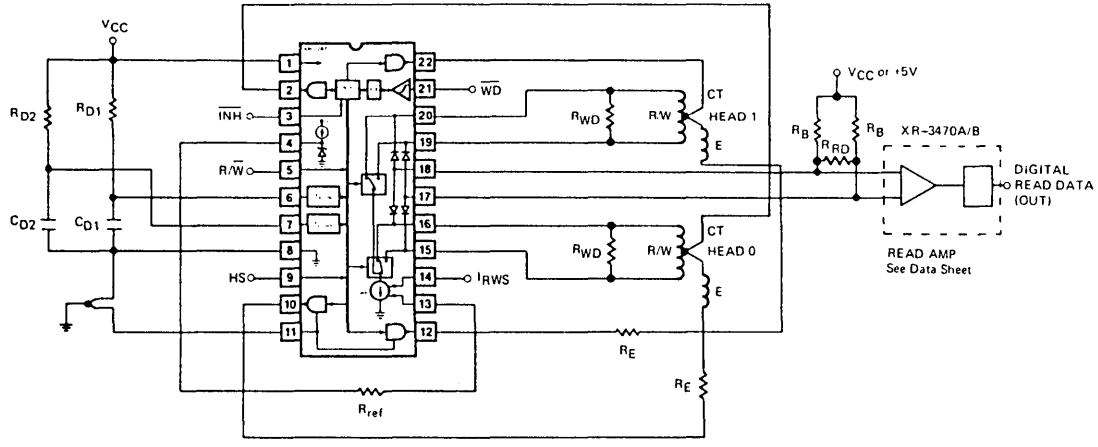


Figure 5. Typical Dual Head Floppy Disk System

Floppy Disk Read/Write

GENERAL DESCRIPTION

The XR-3448 Floppy Disk Read/Write is a single 28 Pin monolithic solution for double-sided floppy disk drives. The device is compatible with 8", 5¼", and 3½" drives, providing all read and write functions and offering improved performance over industry standard dual chip sets, with lower external parts count. Schmitt trigger inputs and separate analog and power grounds aid noise and crosstalk immunity. Both pre and post amplifiers, plus an AGC, allow reliable operation with input signals ranging from 0.5 mV to 25mV.

The XR-3448 is available in standard or small outline 28 Pin packages. Control, write inputs, and read outputs are TTL compatible. The device operates from +12 V and +5 V supplies. The pinout is specially designed for similarity to the SSI-570 Read/Write, and in many applications, the XR-3448 acts as an improved version of that device.

FEATURES

All Read/Write Functions on a Single Chip
Schmitt Trigger Inputs for Noise Immunity
TTL Compatible
Power Up and Low Voltage Inhibit
Low Peak Shift – No Trimming Necessary
On Board AGC
Wide Read Dynamic Range
Low External Parts Count
All Delays RC Programmable
Separate Power and Signal Ground
Tunnel or Straddle Erase Compatibility

APPLICATIONS

Single or Dual Head Floppy Disk Drive Systems

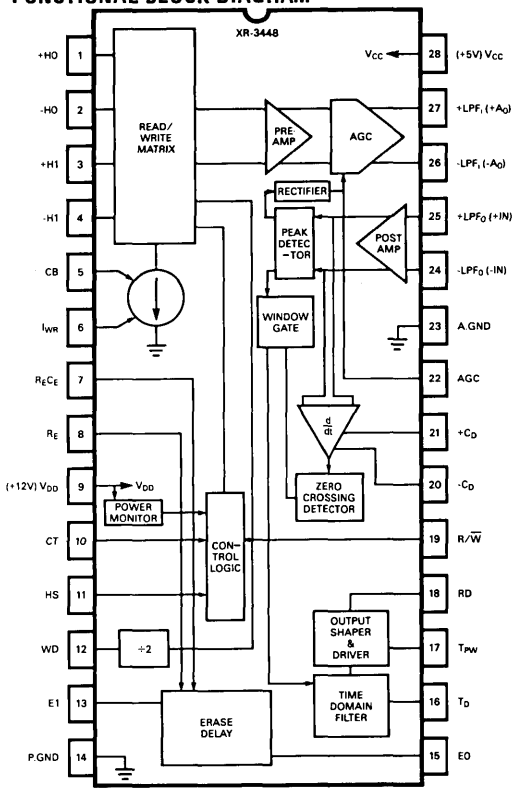
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
Pin 28 (5 V)	7 V
Pin 9 (12 V)	15 V
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	150°C
Power Dissipation (28 Pin DIL)	800 mW
Derate Above 25°C	6.5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3448CP	Plastic	0°C to +70°C
XR-3448CN	Ceramic	0°C to +70°C
XR-3448MD	Small Outline	0°C to +70°C
XR-3448CQ	Quad Surface Mount	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-3448 Floppy Disk Read/Write is a high performance single chip solution for all standard floppy disk drives. TTL compatible control and interface levels, and +12 V and +5 V operation allows easy system implementation with standard components. An on-board voltage monitor, with hysteresis, supervises device voltage and disables all operation during power up and down. Dual grounds, one for the digital levels, the other for low level signals, and the use of ECL processing logic eliminates digital crosstalk and jittering coupled back into the read heads.

Read error reduction performance is greatly enhanced by the window gating logic that qualifies data pules and eliminates errors generated by noise or discontinuities during shouldering. A time domain filter further reduces errors caused by nonlinearities about data peaks. Together, these systems allow improved performance margins over simpler floppy disk read devices.

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 12$ V, $V_{CC} = 5$ V, $R_W = 430\Omega$, $R_{ED} = 10k$, $C_E = 0.05\mu F$, $R_{EH} = 10k\Omega$, $C_D = 100$ pF, $R_D = 200\Omega$, $C_{TD} = 100$ pF, $R_{TD} = 10k\Omega$, $C_{PW} = 330$ pF, $R_{PW} = 10k\Omega$, Output Load = $1k\Omega$ to V_{CC}, V_{IN} (preamp) = DC coupled 10 mVp-p sine wave, V_{IN} (postamp) = AC coupled 200 mVp-p sine wave, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{CC}	Recommended Power Supply Voltage	4.5	5	5.5	V	
V_{DD}	Recommended Power Supply Voltage	10.8	12	13.2	V	
I_{CC}	Power Supply Current (5 V)		30 33	35 40	mA mA	Read Mode Write Mode
I_{DD}	Power Supply Current (12 V)		17 22	22 25	mA mA	Read Mode Write Mode, $I_E = 0$
POWER SUPPLY MONITOR						
V_{CC}	Power Up Threshold Power Down Threshold	3.0 2.3	3.5 2.6	4.0 3.0	V V	
V_{DD}	Power Up Threshold Power Down Threshold	7.9 6.5	8.6 7.5	9.2 8.0	V V	
LOGIC INPUTS						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IL}	Input Low Current			−400	μA	$V_{IL} = 0.4$ V
I_{IH}	Input High Current			20	μA	$V_{IH} = 2.4$ V
DATA OUTPUT						
V_{OL}	Output Low Voltage			0.5	V	$I_{OL} = 4$ mA
V_{OH}	Output High Voltage	2.7			V	$I_{OH} = 400\mu A$
T_{PW}	Pulse Width Accuracy	−20	±5	20	%	$R_{PW} = 10k\Omega$ $C_{PW} = 330$ pF
R_{PW}	Recommended Resistor Range	5		25	kΩ	
C_{PW}	Recommended Capacitor Range	100		620	pF	
TIMERS						
	Erase Delay Accuracy Erase Hold Accuracy	−15 −15	±5 ±5	15 15	% %	Error from $T_{ED} = R_{ED} C_E$ Error from $T_{EH} = (R_{ED}+R_{EH})C_E$
R_{ED}/R_{EH}	Recommended Resistor Value	5		30	kΩ	
C_E	Recommended Capacitor Value	0.01		0.068	μF	
	Time Domain Filter Accuracy	−15	±5	15	%	$R_{TD} = 10k$, $C_{TD} = 100$ pF
R_{TD}	Recommended Resistor Value	1		15	kΩ	
C_{TD}	Recommended Capacitor Value	51		330	pF	

ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 12$ V, $V_{CC} = 5$ V, $R_W = 430\Omega$, $R_{ED} = 10k$, $C_E = 0.05\mu F$, $R_{EH} = 10k\Omega$, $C_D = 100$ pF, $R_D = 200\Omega$, $C_{TD} = 100$ pF, $R_{TD} = 10k\Omega$, $C_{PW} = 330$ pF, $R_{PW} = 10k\Omega$, Output Load = $1k\Omega$ to V_{CC}, V_{IN} (preamp) = DC coupled 10 mVp-p sine wave, V_{IN} (postamp) = AC coupled 200 mVp-p sine wave, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
READ MODE						
PREAMP						
A_V	Differential Voltage Gain		300		V/V	f = 250 kHz, V_{CT} = 1.5 V Pin 22 Shorted to Ground
BW	Bandwidth	5	15		MHz	−3 dB Point
	Gain Flatness	−1.0		1.0	dB	f = 0 to 1.5 MHz
Z_{IN}	Differential Input Impedance	10	30		kΩ	f = 250 kHz
AGC						
	Dynamic Range		12		dB	For 3 dB Output Variation
R_{AGC}	Recommended Resistor Range	3.3	10	25	kΩ	
C_{AGC}	Recommended Capacitor Range	0.01	0.1	1	μF	
POSTAMPLIFIER & DIFFERENTIATOR						
A_V	Differential Voltage Gain	4	4.5	6	V/V	f = 250 kHz
BW	Bandwidth	5	15		MHz	−3 dB Point
	Gain Flatness	−1.0		1.0	dB	
WRITE MODE						
V_{CT}	Center Tap Output ON Voltage	V_{DD} −2.5	V_{DD} −2	V_{DD} −1.3	V	$R_E = 150\Omega$
V_E	Erase Output ON Voltage		0.5	1.0	V	$R_E = 150\Omega$
	Unselected Head Erase Leakage			100	μA	V_{EO}, V_{E1} = 12 V, $R_E = 150\Omega$
I_W	Recommended Write Current Range	3		10	mA	$R_W = 680\Omega$ to 180Ω
	Write Current Accuracy	−5	±0.2	5	%	CB = 0
	Write Current Unbalance	−1	±0.01	1	%	Head 0 to Head 1
CB	Current Boost Factor	1.25	1.30	1.35		CB = 1

4

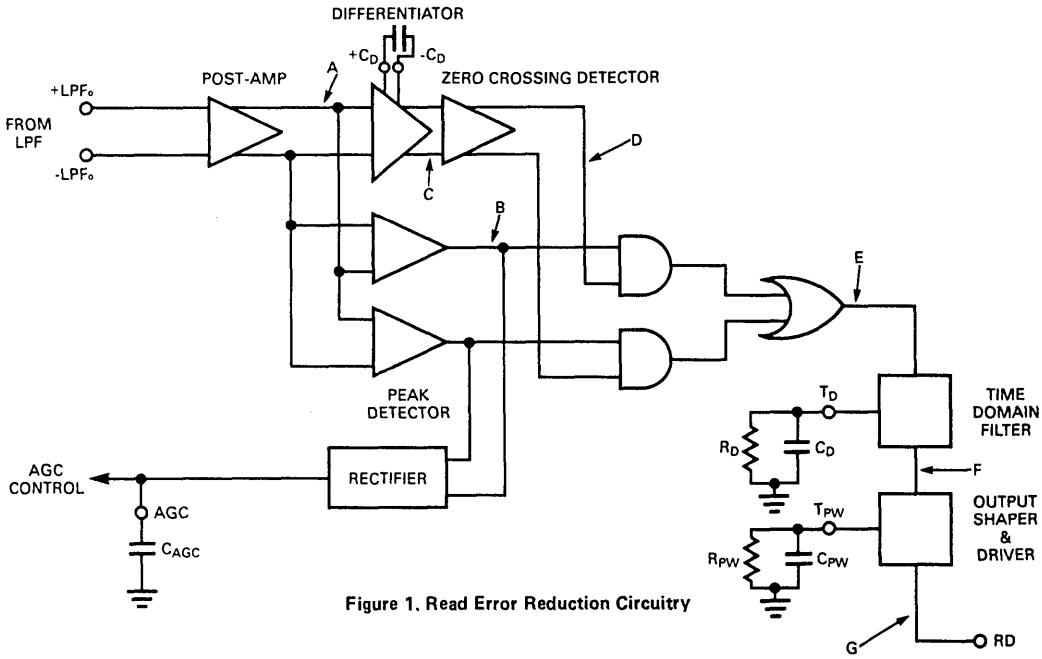


Figure 1. Read Error Reduction Circuitry

PRINCIPLES OF OPERATION

Write Mode

In the write mode, R/W (Pin 19) is held low. Data is applied to the input Schmitt trigger (Pin 12), goes through a toggle flip-flop, and into the write matrix. The proper magnetic head is selected by the matrix, depending on the level at HS (Pin 11). Both head center taps are connected to CT (Pin 10) which sources the current sunk by the proper transistor (Pin 1, 2, 3, or 4).

Write current is controlled by the resistor, R_{IW}, on I_{WR} (Pin 6); when CB (Pin 5) is pulled high, write current is boosted 30%. Tunnel erase delay and hold times are set by a capacitor and two resistors on $R_E C_E$ (Pin 7) and R_E (Pin 8). Straddle erase heads are accommodated by eliminating C_E.

Read Mode

Pulling R/W high selects data readback mode. The dual error reduction system employed by the XR-3448 greatly diminishes read error rates. The read signal is routed through a diode multiplexer into a low noise preamplifier. This output is routed to an automatic gain control (AGC) circuit which lowers peak shift: for most systems, external peak shift adjustment is unnecessary across an input dynamic range from 500 μV to 25 mV. The AGC compresses a 20 dB input variation down to a 5 dB output range. AGC response time is affected by the RC at the AGC pin (Pin 22). The compressed signal is applied to a low pass filter (LPF) which attenuates high frequency noise. A post-amplifier compensates for LPF insertion losses and drives both the Peak Detector and Active Differentiator (see Figure 1) with waveform A, shown in Figure 2. The Peak Detector is a comparator-like device that produces output whenever data input is above a threshold level (see Figure 2B). This output is employed as the Gating Logic enable. Rectified peak detector output is returned to the AGC as the control signal.

The Active Differentiator computes the first derivative of the input signal, producing waveform C of Figure 2. Zero Crossing Detector output toggles (Figure 2D) at zero crossings, which correspond to data peaks – one crossing per datum. Hysteresis in the detector aids noise immunity. The Window Gating Logic effectively provides an AND function: output (Figure 2E) appears only when (1) the Zero Crossing Detector sees a crossing, and (2) the Peak Detector sees a data peak. Spurious signals, therefore, do not cause output.

Noise and system nonlinearities however, occasionally produce closely spaced false outputs. Further error reduction is provided by a time domain filter following the gating logic. Adjacent pulses, occurring before the minimum time delay set by a resistor and capacitor on T_d (Pin 16), are ignored (Figure 2E). Since nonlinearities occur in pairs, a valid data pulse mixed with two invalid pulses still provides one meaningful output – exactly as desired. Output pulse width is determined by an RC on T_{pw} (Pin 17), which feeds the output driver with TTL level constant width pulses. The data appears at RD (Pin 18), as shown in Figure 2G.

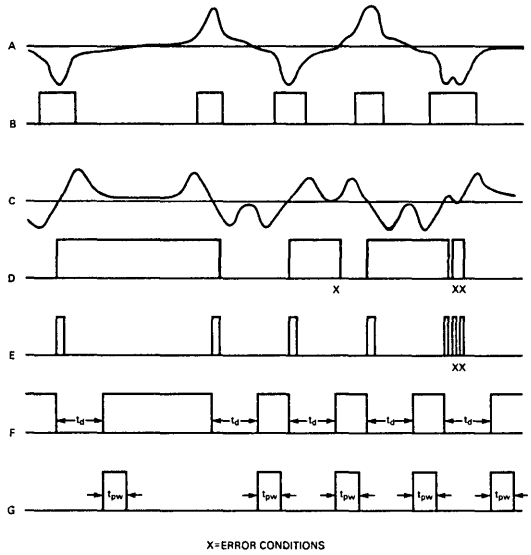


Figure 2. Read Waveforms

APPLICATIONS INFORMATION

The applications circuit of Figure 4 may be customized to match the available magnetic head, interface pulse widths, write currents, AGC times, data transfer rates, etc. Table 1 gives recommended component values and ranges.

DESIGN INSTRUCTIONS

AGC:

The AGC time constant is set by the resistor and capacitor on Pin 22. The time must be short enough that initial data does not overdrive the amplifiers, yet long enough that noise and offset levels between data bits do not register as output. Delay time is determined by:

$$T = R_{AGC}\, C_{AGC}$$

For most applications at 500 kB data rate, a time of 1 ms, using R_{AGC} = 10 kΩ and C_{AGC} = 0.1μF.

LPF

The LPF is strongly dependent on head type and other system and circuit considerations. Constant gain and phase to f = (baud rate/2) is tantamount to proper performance. Avoiding driver saturation requires that the filter current is less than 2.8 mA. The postamplifier inputs are DC biased internally. Blocking capacitors should isolate the DC level from the AGC output; optimum transient response characteristics occur when the capacitors are before the filter, directly after the AGC output.

Active Differentiator

The differentiation function requires a capacitor network across Pins 20 and 21. The dominant component, capacitor C_D, is optimum when its current slew rate is maximized. This occurs when

$$C_D = \frac{1\ \text{mA}}{(A_{VD})\,(E_P)\,(\omega_{max})\,(A_F)}$$

Where A_{VD} is the gain of the amplifier
E_P is the maximum expected input voltage
ω_{max} is the maximum operating frequency in radians/sec of the system
A_F is the gain of the filter network

If C_D is greater than the maximum value calculated above, peak shifting will occur.

When C_D is the only component employed, a pole is produced by C_D and the effective output resistance of Q1 and Q2 (See Figure 3), R_O. This pole lies at

$$\omega_p = \frac{1}{2R_O\, C_D}$$

where R_O is typically 40Ω.

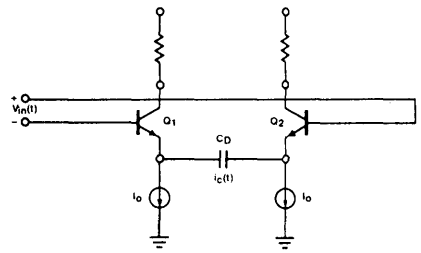


Figure 3. Simplified Active Differentiator Section

Perfect differentiation requires a phase shift of 90°. This suggests ω_p should approach ∞ since

$$\theta = \arctan\,(\omega_p/\omega_O)$$

where ω_O = operating frequency.

A large ω_p, however, produces a large noise bandwidth; a reasonable compromise sets ω_p at 10 ω_{max}. This produces a phase shift of approximately 84° and limits the noise bandwidth. The design criteria is now given by

$$\omega_{max} = \frac{1}{20(R_O C_D)}$$

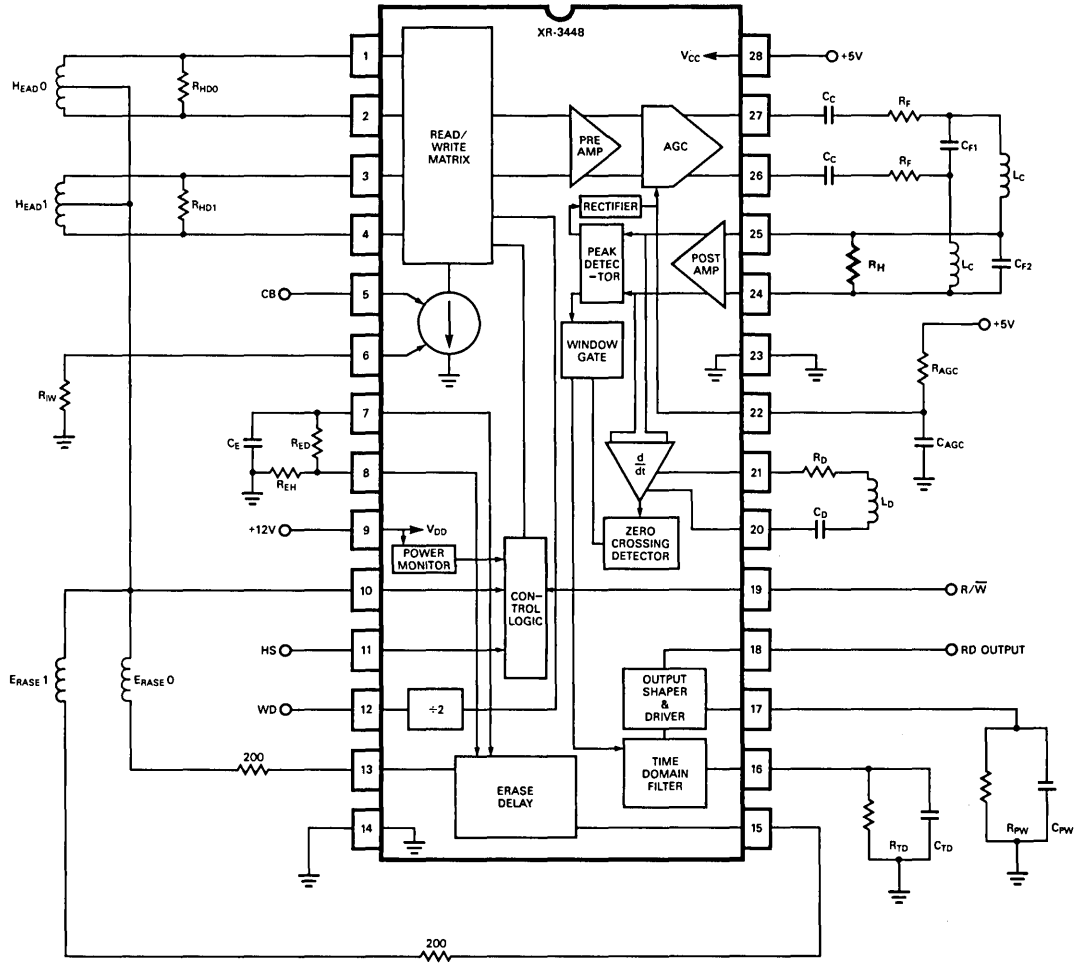


Figure 4. XR-3448 Typical Application

For maximum gain applications delete R_{AGC} and C_{AGC} and ground pin 22.

TABLE I

TYPICAL COMPONENT VALUES

Component	Typical Value	Recommended Range	Component	Typical Value
R_{IW}	560Ω	180 - 680Ω	R_H	1.5kΩ
R_{E0}, R_{E1}	280Ω	100 - 680Ω	C_C	.022μF
R_{ED}, R_{EH}	10kΩ	5k - 30kΩ	R_F	470Ω
C_E	.047μF	0.01 - 0.068μF	C_{F1}	.001μF
R_{PW}	10k	5k - 25kΩ	C_{F2}	470pF
C_{PW}	100 pF	51 pF - 1000 pF	L_C	680μH
C_{TD}	100pF	51 pF - 330 pF	R_D	200Ω
R_{AGC}	6.81k	3.3k - 25kΩ	C_D	1000pF
C_{AGC}	1μF	.01μF - 1μF	L_D	56μH

Often, R_O is too low, creating a pole at a frequency greater than 10 ω_{max}. In this case, a resistor R_D, in series with C_D gives the equation:

$$\omega_{max} = \frac{1}{20(R_D + R_O)\, C_D}$$

This allows a degree of flexibility in selecting the noise bandwidth, as shown in Figure 5.

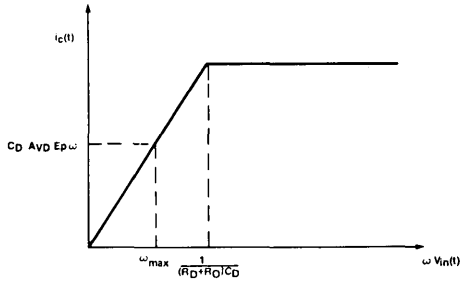


Figure 5: Differentiator Response for C_D and R

A series inductor, L_D, will further reduce noise bandwidth by introducing another pole. When selected for 10 ω_{max}, as shown in Figure 6, L_D is given by

$$L_D = \frac{1}{100(\omega_{max})^2 C_D}$$

The damping ratio, δ, should be between 0.3 and 1 where

$$\delta = \frac{(R_O + 0.5\, R_D)\, C_D}{2\sqrt{L_D C_D}}$$

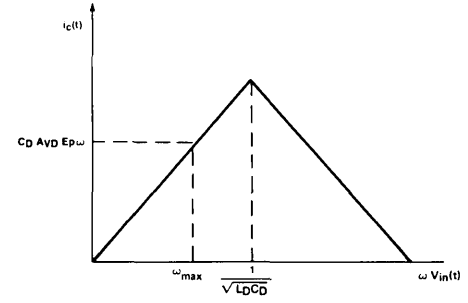


Figure 6: Differentiator Response with R_D, C_D, and L.

Peak Shift Adjustment

For the majority of applications, the inherent low peak shift of the XR-3448 requires no improvement. However, an additional trim can be implemented if necessary. The arrangement shown in Figure 7 will eliminate the current imbalance in the differentiator and reduce comparator offset voltages. The potentiometer is adjusted for symmetrical output with sinusoidal input.

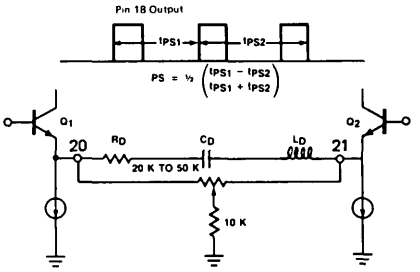


Figure 7. Nulling Network to Minimize Peak Shift (PS)

Time Doman Filter

Filter time, t, is determined by the maximum period of expected distortion, Δt, and the maximum operating frequency, f_{max}.

Determination of R and C involves the following considerations:

$$t = 0.215\, R_{TD}\, C_{TD} + 200\ nS$$

where R_{TD}: 1 kΩ ≤ R ≤ 15kΩ, and C_{TD}: 51pF ≤ C ≤ 330 pF

Output Shaper

The output shaper determines the pulse width of the data signal. Resistor and capacitor ranges follow the same guidelines as presented in the Time Domain Filter above. Pulse width is:

$$t = 0.215\, R_{PW}\, C_{PW} + 120\ nS$$

where R_{PW}: 5kΩ ≤ R ≤ 30kΩ, and C_{TD}: 100 pF ≤ C ≤ 620 pF.

Damping Resistors

Head damping resistors should be optimized for writing. Their value depends entirely on the head employed and the desired damping coefficient.

Write Current

A current mirror uses the internal voltage reference and a resistor from Pin 6 to ground for write current programming. The resistor value is determined by

$$R_{IW}\ (k\Omega) = \frac{2.35V}{I_{WR}\ (mA)}$$

Write current increases by 30% over this value when CB (Pin 5) is held at a high TTL logic level.

Additional write current steps, if necessary, are implemented as shown in Figure 8. In Figure 8(a), TTL logic lines and reistors vary current output. Figure 8(b) shows the resistive ladder method, with transistors selectively switching resistors. The varying resistance on Pin 6 causes varying write currents.

$$I_W\ (mA) = \frac{2.35V}{R_{IW}\ (total)\ (k\Omega)}$$

These method work for any number of control lines. CB (Pin 5) is still active, and will multiply current by 1.3 whenever held high.

Write Erase Resistors

Erase current is limited by series resistors from E0 and E1 to the respective erase heads. Resistor values may be approximated by:

$$R_E = \frac{V_{CT} - V_{SAT}}{I_{ERASE}}$$

For typical I_{ERASE} = 50 mA, V_{CT} = 10.5 V, and V_{SAT} = 500 mV, R_E = 200 Ω.

Erase Delay Time

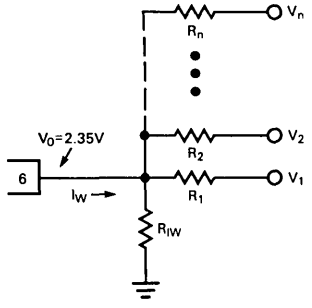
Tunnel erase delays are provided by the XR-3448. Both Erase Delay Time, T_{ED}, which controls erase initiation and Erase Hold Time, T_{EH}, which delays erase release, are controlled by a simple RC circuit. In the configuration of Figure 1, T_{ED} is calculated as:

$$T_{ED} = R_{ED}\ C_E$$

and T_{EH} is determined by

$$T_{EH} = (R_{ED} + R_{EH})\ C_E$$

Suggested resistor values range between 5kΩ and 30kΩ. C_E should range from 0.01μF to 0.068μF.

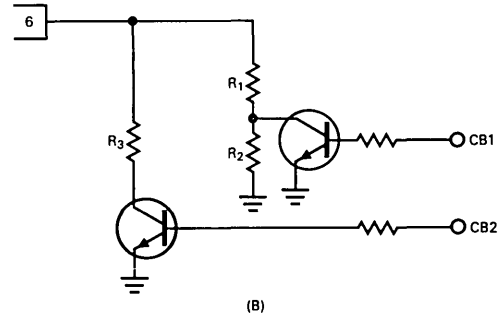


$$I_W = \frac{V_0}{R_{IW}} - \left(\frac{V_1 - V_0}{R_1}\right) - \left(\frac{V_2 - V_0}{R_2}\right) - \cdots - \left(\frac{V_n - V_0}{R_n}\right)$$

WHERE V_0 = 2.35V AND V_1 THROUGH V_n ARE LOGIC LEVELS.

(A)

CB1	CB2	R_{IW} (eff)
0	0	$R_1 + R_2$
0	1	$R_3 // R_1 + R_2$
1	0	R_1
1	1	$R_3 // R_1$



(B)

Figure 8. Obtaining Additional Write Current Steps: (A) TTL Lines and Resistors Increase and Decrease I_W. (B) Transistors Switch Resistors to Increase I_W.

Floppy Disk Read Amplifier

GENERAL DESCRIPTION

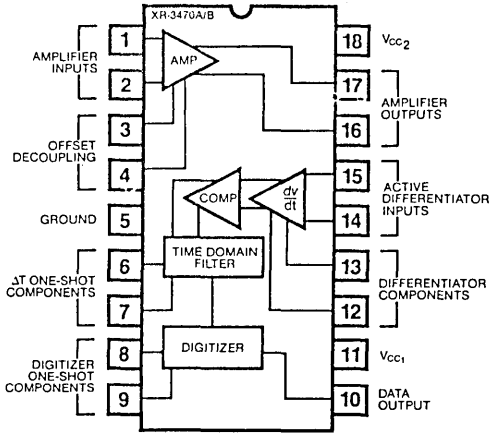
The XR-3470A/3470B is read amplifier system designed primarily for use in a floppy disk drive system. It is designed to perform the complete readback function, by accepting the readback signal from a magnetic head and converting it into digital output pulses. To perform this function, the circuit contains a high-frequency amplifier, an active differentiator, a zero-crossing detector, and a time domain filter.

The XR-3470A/3470B is suited for systems with data transfer rates up to 3 megabaud. High input sensitivity allows operation with signal levels as low as 1.4 mV pp, which gives it the flexibility to be used for single or double density floppy disk systems.

The XR-3470A/3470B offers improvements (over the standard 3470) of lower peak shift and power part-to-part input amplifier gain variations.

The XR-3470A/3470B, available in an 18 Pin DIP, is powered by +5 and +12 volt power supplies.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Complete Floppy Disk Read Amplifier	
Low Input Voltage detection	1.4 mV pp
Low Peak Shift 3470A	2% Max
3470B	4% Max
Low Amplifier Gain Variation	100 V/V Min
	130 V/V Max
High Amplifier Frequency Response	10 MHz, Min.

APPLICATIONS

Single/Double Density Floppy Disk Read Amplifier
Magnetic Read Amplifier

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage (Pin 11)	7 V dc
Power Supply Voltage (Pin 18)	16 V dc
Input Voltage (Pins 1 and 2)	−2V to +7 V dc
Output Voltage (Pin 10)	−2V to +7 V dc
Operating Ambient Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Operating Junction Temperature	150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3470ACN	Ceramic	0°C to +70°C
XR-3470ACP	Plastic	0°C to +70°C
XR-3470BCN	Ceramic	0°C to +70°C
XR-3470BCP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-3470A/3470B contains four internal signal blocks. Their functions are as follows: **Input Amplifier** — This section receives an input directly from the magnetic head. It provides a nominal gain of 110 V/V, with gain select pins to reduce gain or tailor it for ac response. The amplifier has differential inputs and outputs. **Active Differentiator** — This circuit differentiates the signal from the amplifier which causes a zero-crossing for each peak of the readback signal. The time constant and response of this section is externally set. **Zero-Crossing Detector** — This function is performed by a voltage comparator. It produces complementary outputs for the internal digital section. **Digital Section** — This section consists of 2 one-shots and other control circuitry. The one-shots are used to prevent false outputs, and set the output pulse width.

ELECTRICAL CHARACTERISTICS

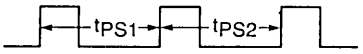
Test Conditions: T_A = 0°C to 70°C; V_{CC1} = 4.75V to 5.25V; V_{CC2} = 10V to 14V; unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GAIN AMPLIFIER SECTION						
A_{VD}	Differential Voltage Gain	100	110	130	V/V	f = 200 kHz, V_{ID} = 5 mV (RMS)
I_{IB}	Input Bias Current	—	−10	−25	μA	
V_{ICM}	Input Common Mode Range Linear Operation	−0.1	—	1.5	V	5% max THD
V_{ID}	Differential Input Voltage Linear Operation	—	—	25	mV pp	5% max THD
V_{OD}	Output Voltage Swing Differential	3.0	4.0	—	V pp	
I_O	Output Source Current, Toggled	—	8.0	—	mA	
I_{OS}	Output Sink Current	2.8	4	—	mA	Pins 16 and 17
R_I	Small Signal Input Resistance	100	250	—	kΩ	T_A = 25°C
R_O	Small Signal Output Resistance Single-Ended	—	15	—	Ω	T_A = 25°C, V_{CC1} = 5V V_{CC2} = 12V
BW	Bandwidth, −3 dB	10.0	—	—	MHz	T_A = 25°C, V_{CC1} = 5V V_{ID} = 2 mV (RMS), V_{CC2} = 12V
CMRR	Common Mode Rejection Ratio	50	—	—	dB	T_A = 25°C, f = 100 kHz A_{VD} = 40 dB, V_{CC1} = 5V V_{IN} = 200 mV pp, V_{CC2} = 12V
PSSR1	V_{CC1} Supply Rejection Ratio	50	—	—	dB	T_A = 25°C, A_{VD} = 40 dB 4.75 < V_{CC1} < 5.25, V_{CC2} = 12V
PSSR2	V_{CC2} Supply Rejection Ratio	60	—	—	dB	T_A = 25°C, A_{VD} = 40 dB 10 < V_{CC2} < 14V, V_{CC1} = 5V
V_{DO}	Differential Output Offset	—	—	0.4	V	T_A = 25°C, V_{ID} = V_{IN} = 0V
V_{CO}	Common Mode Output Offset	—	3.0	—	V	V_{ID} = V_{IN} = 0V Differential and Common Mode
e_n	Differential Noise Voltage Referred to Input	—	15	—	μV (RMS)	BW = 10 Hz to 1.0 MHz T_A = 25°C
ACTIVE DIFFERENTIATOR SECTION						
I_{OD}	Differentiator Output Sink Current	1.0	1.4	—	mA	Pins 12 and 13, V_{OD} = V_{CC1}
PS	Peak Shift 3470A	—	—	2.0	%	f = 250 kHz, V_{ID} = 1V pp
	3470B	—	—	4.0	%	I_{CAP} = 500 μA V_{CC1} = 5V, V_{CC2} = 12V See Figure 2
R_{ID}	Differentiator Input Resistance Differential	—	30	—	kΩ	T_A = 25°C
R_{OD}	Differentiator Output Resistance Differential	—	40	—	Ω	T_A = 25°C
DIGITAL SECTION						
V_{OH}	Output Voltage High Logic Level	2.7	—	—	V	Pin 10, V_{CC1} = 4.75V I_{OH} = −0.4 mA, V_{CC2} = 12V
V_{OL}	Output Voltage Low Logic Level	—	—	0.5	V	Pin 10, V_{CC1} = 4.75V I_{OL} = 8.0 mA, V_{CC2} = 12V
t_{TLH}	Output Rise Time	—	—	20	ns	Pin 10
t_{THL}	Output Fall Time	—	—	25	ns	Pin 10
$t_{1A,B}$	Timing Range Mono #1	500		4000	ns	t_{1A},t_{1B}
E_{t1}	Timing Accuracy Mono #1	85	—	115	%	R_1 = 6.4 kΩ, C_1 = 200 pF (Note 1)
t_2	Timing Range Mono #2	150	—	1000	ns	
E_{t2}	Timing Accuracy Mono #2	85	—	115	%	R_2 = 1.6 kΩ, C_2 = 200 pF (Note 2)
I_{CC1}	V_{CC1}, Power Supply Current	—	25	40	mA	
I_{CC2}	V_{CC2}, Power Supply Current	—	3	10	mA	

1. Accuracy guaranteed for R_1 and C_1 in range
   1.5 kΩ < R_1 < 10 kΩ
   150 pF < C_1 < 680 pF

2. Accuracy guaranteed for R_2 and C_2 in range
   1.5 kΩ < R_2 < 10 kΩ
   100 pF < C_2 < 800 pF

$$PS = \frac{1}{2}\left(\frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}}\right) \text{ at Pin 10}$$



I_{CAP} = current into Pin 12

Figure 2.

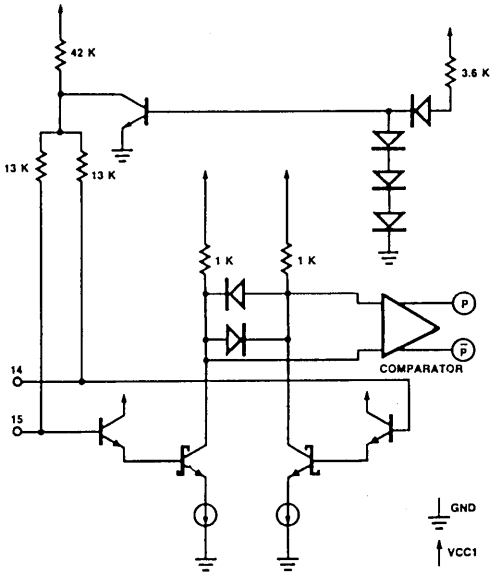
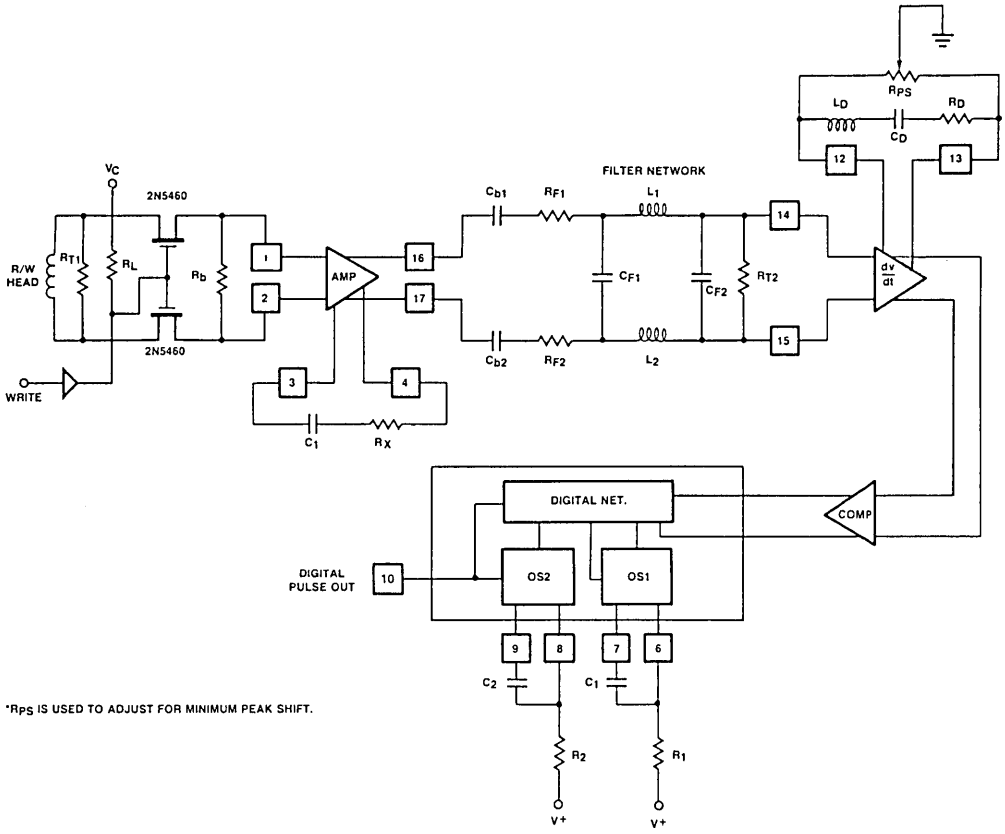


Figure 3. Active Differentiator and Zero Crossing Detector



*RPS IS USED TO ADJUST FOR MINIMUM PEAK SHIFT.

Figure 4. Generalized Circuit Connection for Floppy Disk Read System

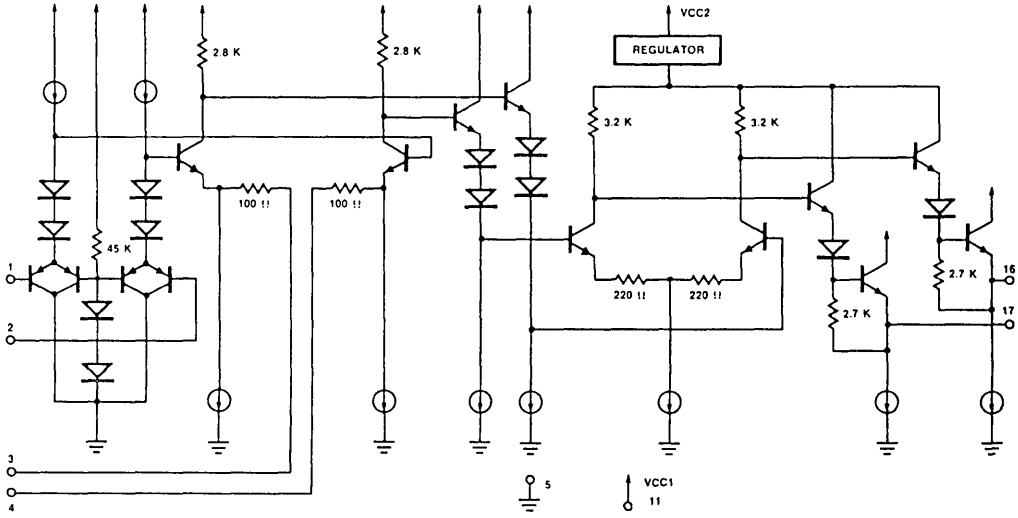


Figure 5. Input Amplifier

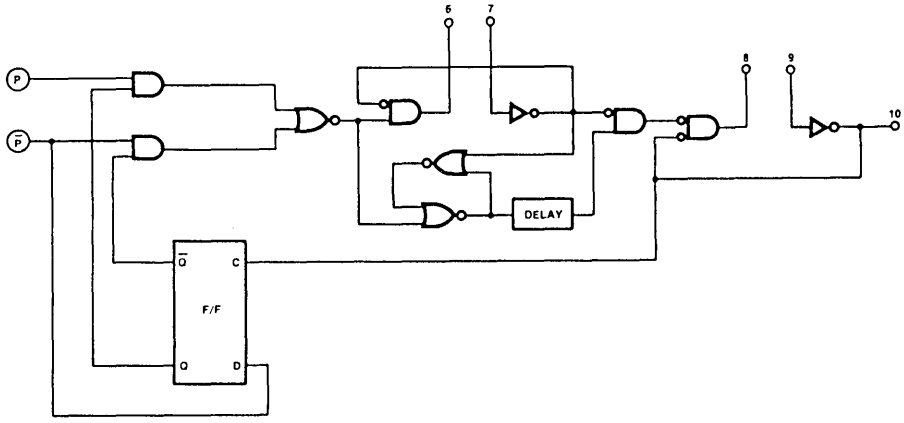


Figure 6. Digital Section

R/W HEAD COUPLING

When switching from the write channel to the read channel, one must be careful not to present a differential voltage to the inputs of the amplifier, for this will result in an amplified swing at the output of the amplifier, which will cause peak shifting at the digital output. A balanced diode network or FET switches, as shown in Figure 4, may be used to overcome this problem.

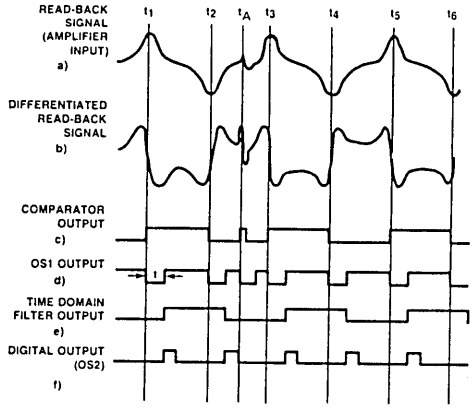


Figure 7a-f. Waveforms Through the XR-3470A/3470B

AMPLIFIER STAGE

The amplifier stage will typically amplify the read back signal by a factor of 110. In order to eliminate any offset between the amplifier stages, a capacitor, C_1, should be inserted between Pins 3 and 4. If the input signal to the amplifier is to be above 25 mV, clamping of the amplifier may occur. To reduce the gain, a resistor R_X may be inserted in series with C_1 between Pins 3 and 4. The graph in Figure 8 shows a plot of normalized gain vs R_X.

It should be noted that capacitor C_1 with R_X and the resistance looking into Pins 3 and 4, will create a pole at approximately

$$\omega p = \frac{1}{(R_X + 250)\, C_1}$$

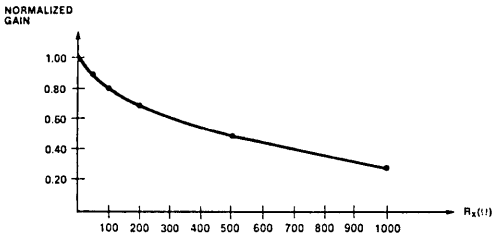


Figure 8. Normalized Gain vs R_X for Amplifier Stage

so C_1 should not be made too low. C_1 = 0.1 μF is nominal for most floppy disk applications.

FILTER NETWORK

The filter network, between the XR-3470A/3470B amplifier stage and differentiator stage, is subject to several system and circuit considerations.

The filter network, first and foremost, must be designed to pass all frequencies up to 1/2 the maximum baud rate, with a constant gain and phase shift. This frequency can be stated as f_{max}, where

$$f_{max} = 1/2\ (\text{Baud rate})_{max}$$

In order to avoid saturation of the amplifier current sources, the current into the filter must not exceed 2.8 mA. In order to meet this condition the impedance of the filter must be governed by the following constraint

$$Z_{min} > \frac{(A_{VD}\, E_P)_{max}}{2.8\ \text{mA}}$$

where A_{VD} is the gain of the amplifier
E_p is the maximum peak voltage of the input signal

The differentiator inputs are dc biased internally. This implies that the dc level from the amplifier stage must be blocked in order not to disturb these levels. Therefore blocking capacitors, C_{b1} and C_{b2}, should be placed before the differentiator inputs. In order to keep the transient response to a minimum it is best to place the dc blocking capacitors before the filter network.

ACTIVE DIFFERENTIATOR

The amplified filtered read back signal is fed into the active differentiator. Here, the peaks of the read back signal are transformed into zero crossings as shown by Figures 7a and 7b.

In order to perform the differentiator function a capacitor C_D is needed across Pins 12 and 13. The selection of C_D for accurate zero crossing is optimized by maximizing current slew rate through C_D, which occurs when

$$C_D = \frac{1\ \text{mA}}{(A_{VD}\, E_P \omega)_{max}\, A_F}$$

Where A_{VD} is the gain of the amplifier
E_p is the maximum expected input voltage
ω is the maximum operating frequency in radians/sec of the system
A_F is the gain of the filter network

If C_D is greater than the maximum value calculated above, peak shifting will occur.

As can be seen from Figure 9; the capacitor C_D and the effective output resistance, R_O of transistors Q1 and Q2 produce a pole given by

$$\omega_p = \frac{1}{2R_OC_D}$$

where R_O is typically 40Ω.

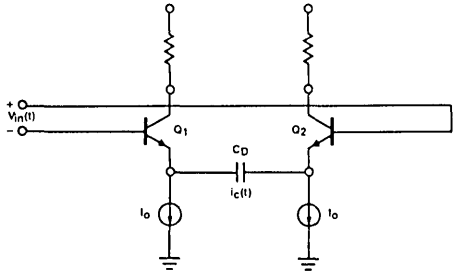


Figure 9. Simplified Active Differentiator Section

In order to obtain a phase shift approaching 90° for perfect differentiation ω_p would have to approach ∞ since

$$\theta = \tan^{-1}(\omega_p/\omega_o)$$

$$\omega_o = \text{operating frequency}$$

It must be considered, however, that making ω_p as high as possible also produces a noise bandwidth as high as possible.

In order to come to a reasonable compromise ω_p should be selected to be ten times the maximum expected operating frequency.

$$\omega_p = 10\,\omega_{max}$$

where ω_{max} is the maximum operating frequency of the system in radians/sec.

Doing this produces a phase shift of approximately 84°, while limiting the noise bandwidth. The design criteria is now given by

$$\omega_{max} = \frac{1}{20R_OC_D}$$

It may be that R_O is too low, creating a pole at a higher frequency than 10 ω_{max}. If this is so one can insert a resistor R_D in series with C_D, giving the equation

$$\omega_{max} = \frac{1}{20RC_D}$$

where $R = R_O + 0.5R_D$

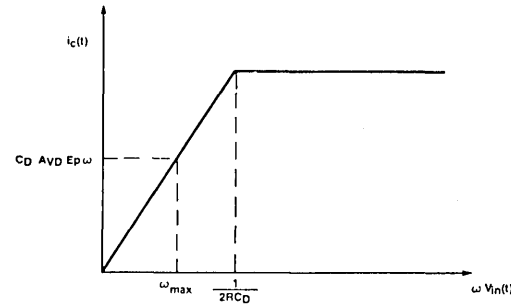


Figure 10. Differentiator Response for C_D and R

In order to reduce the noise bandwidth further a second pole can be introduced at 10 ω_{max} by placing an inductor in series with C_D and R_D, where L_D is given by

$$L_D = \frac{1}{100(\omega_{max})^2\,C_D}$$

The damping ratio, δ, should be between .3 and 1 where

$$\delta = \frac{(R_O + 0.5R_D)\,C_D}{2\sqrt{L_DC_D}}$$

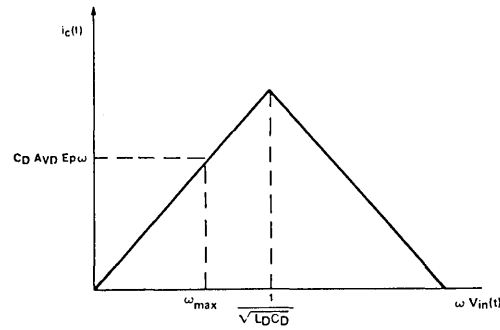


Figure 11. Differentiator Response with R_D, C_D, and L

PEAK SHIFT CONSIDERATIONS

The arrangement shown in Figure 12 will eliminate the current imbalance in the differentiator, and offset in the comparator, thus minimizing the peak shift at the digital output. The potentiometer is adjusted with a minimum sinusoidal Epω at the input, for symmetrical digital waveform at the digital output, Pin 10.

ZERO CROSSING DETECTOR

The differentiated output signals from the active differentiator are run into a comparator. Since the outputs of the active differentiator are 180° out of phase, the comparator will produce an output pulse whenever the differentiated signal crosses zero. This is shown in Figures 7b and 7c.

MONOSTABLE #1 (OS1)

This one shot is used to prevent false digital outputs due to noise at zero crossings as shown at time t_A, in Figure 7a. The adjustment of the one shot is done via external components R_1 and C_1 where

$$1.5\ K < R_1 < 10\ K$$
$$0.150\ pF < C_1 < 680\ pF$$
$$\text{and } t = R_1C_1\ (0.625) + 0.2\ \mu sec$$

The value of t is determined by the maximum period of expected distortion, ΔT, and the maximum operating frequency

$$\text{where } \Delta T < t < \frac{1}{4f_{max}} - \frac{\Delta T}{2}$$

The one shot is triggered on the rising and falling edge of the comparator output as can be seen in Figures 7c and 7d. The time domain filter will change state on the rising edge of OS1's output if and only if the pulse width of the comparator output is greater than the time of OS1's pulse, t. This is shown in Figures 7c, 7d, and 7e.

MONOSTABLE #2 (OS2)

This one shot is used to adjust the pulse width of the digital output pulses at Pin 10. The adjustment of this one shot is done via external components R2 and C2 where

$$1.5\ K < R2 < 10\ K$$
$$150\ pF < C2 < 680\ pF$$

The pulse width of the output pulse is given by

$$t_O = R_2C_2\ (0.625)$$

This one shot is triggered on the rising and falling edges of the time domain filter output, as shown on Figures 7e and 7f, giving the corresponding digital pulses for the peaks of the read back signal, shifted by OS1's time, t, as can be seen from Figures 7a, 7d, and 7f.

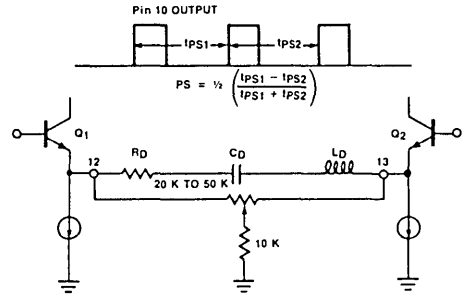


Figure 12. Nulling Network to Minimize Peak Shift (PS)

Floppy Disk Write Amplifier

GENERAL DESCRIPTION

The XR-3471 is a write amplifier designed to provide the complete interface between write data signals and tunnel and straddle erase magnetic heads. Although primarily intended for floppy disk drive systems, the XR-3471 can also be used in other magnetic media systems such as tape drives. Write and erase currents are each externally resistor programmable. Also included is circuitry for inner track write current compensation.

The XR-3471, available in a 20 pin DIP or small outline package, provides TTL compatible inputs. Tunnel erase delays are determined by external reistors and capacitors.

FEATURES

Fully Programmable Write & Erase Currents
Fully Programmable Erase Turn-on/Turn-off Times
(Tunnel and Straddle Erase Compatibility)
Inhibit Output
TTL Compatible Inputs
Direct Replacement for Motorola MC3471

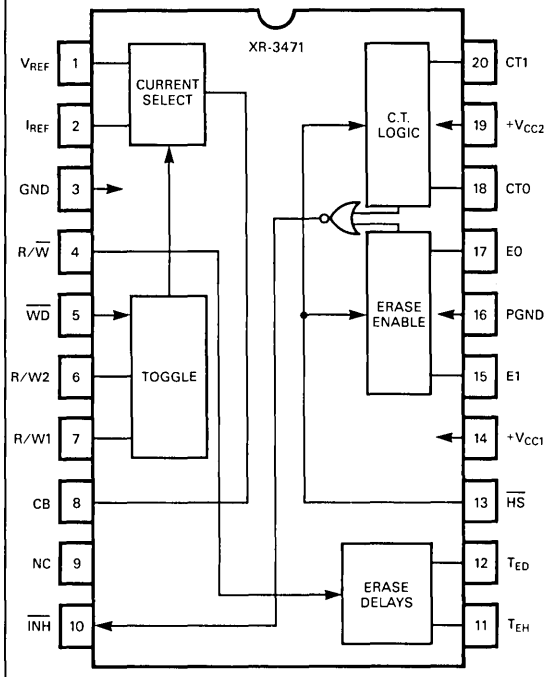
APPLICATIONS

Floppy Disk Drives
Magnetic Tape Write Amplifier

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{CC} 2	30 V dc
V_{CC} 1	7.0 V dc
Input Voltage (All Digital Inputs)	−0.2 V to +5.75 V dc
Output Current	100 mA dc
Storage Temperature	-55°C to +150°C
Power Dissipation	
Plastic Package	650 mW
Derate Above 25°C	5.0 mW/°C
Ceramic Package	1 W
Derate Above 25°C	8.0 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3471CN	Ceramic	0°C to +70°C
XR-3471CP	Plastic	0°C to +70°C
XR-3471MD	Small Outline	0°C to +70°C

SYSTEM DESCRIPTION

The XR-3471 accepts a serial binary data stream input. With the write mode selected, negative transitions of this input signal will alternately provide write current to each half of the head. The write current is externally programmed with a resistor between the internal voltage reference and the current setting input. A high-current open collector output provides the erase coil drive. Turn-on and turn-off delay circuitry is provided, with the delay externally programmed.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 10.8 to 26.4 V, unless specified otherwise. Typicals given for V_{CC1} = 5.0 V, V_{CC2} = 12 V and T_A = 25°C, unless noted otherwise.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL INPUT VOLTAGES							
I_{CC2} I_{CC2}	Power Supply Current			17 7.5	60 30	mA	V_{CC1} V_{CC2}
V_{IH}	High Level Input Voltage	4,8,13	2.0			V	V_{CC1} = 4.5 V
V_{IL}	Low Level Input Voltage	4,8,13			0.8	V	V_{CC1} = 5.5 V
V_{IK}	Input Clamp Voltage	4,5,8,13		−0.87	−1.5	V	I_{IK} = −12 mA
$V_{T(+)}$	Positive Threshold	5	1.5	1.75	2.0	V	V_{CC1} = 5.0 V
$V_{T(-)}$	Negative Threshold	5	0.7	0.98	1.3	V	V_{CC1} = 5.0 V
V_{HTS}	Hysteresis		0.4	0.76		V	$V_{T(+)} - V_{T(-)}$
DIGITAL INPUT CURRENTS							
I_{IH}	High Level Input Current	4,5,8,13		0.1	40	μA	V_{CC1} = 5.5 V, V_{CC2} = 26.4 V, V_I = 2.4 V
I_{IL}	Low Level Input Current	4,5,8,13 4 4 5 8,13		 0.36 0.76 0.46 0.39	−1.6	mA	V_{CC1} = 5.5 V, V_{CC2} = 26.4 V V_{CC2} = 12 V V_{CC2} = 24 V V_{CC1} = 5.0 V V_{CC1} = 5.0 V
DIGITAL OUTPUT LEVEL ($\overline{INHIBIT}$)							
I_{OH}	High Level Output Current	10			100	μA	V_{OH} = 7.0 V, V_{CC1} = 4.5 V
V_{OL}	Low Level Output Voltage	10			0.5	V	I_{OL} = 4.0 mA, V_{CC1} = 4.5 V
CENTER-TAP and ERASE OUTPUTS							
V_{OH}	Output High Voltage	18,20	V_{CC2} −1.5 V	V_{CC2} −1.0		V	I_{OH} = −100 mA V_{CC1} = 4.5 V_{CC2} = 10.8 to 26.4 V
V_{OL}	Output Low Voltage	18,20		 70 70	 150 150	mV	I_{OL} = 1.0 mA V_{CC2} = 12 V V_{CC2} = 24 V
I_{OH}	Output High Leakage	15,17		0.01	100	μA	V_{OH} = 24 V, V_{CC1} = 4.5 V, V_{CC2} = 24 V
V_{OL}	Output Low Voltage			 0.27 0.27	 0.60 0.60	 V V	I_{OL} = 90 mA, V_{CC1} = 4.5 V V_{CC2} = 12 V V_{CC2} = 24 V

4

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 10.8 to 26.4 V, unless specified otherwise. Typicals given for V_{CC1} = 5.0 V, V_{CC2} = 12 V and T_A = 25°C, unless noted otherwise.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
CURRENT SOURCE							
V_{REF}	Reference Voltage	1		5.7		V	
V_{DEG}	Degauss Voltage	1		1.0		V	Voltage Pin 1—Voltage Pin 2
V_F	Bias Voltage	2		0.7		V	
I_{OH}	Write Current Off Leakage	6,7		0.03	15	μA	V_{OH} = 30 V
V_{SAT}	Saturation Voltage	6,7		0.85	2.7	V	V_{CC2} = 12 V
ΔI_{RW}	Current Sink Compliance	6,7		15	40	μA	$V_{6,7}$ = 4.0 V to 24 V
I_{RA}	Average Value Write Current	6,7					Note 2
			2.91	3.0	3.09	mA	R_W = 10k, CB = Low
			5.64	5.89	6.14	mA	R_W = 5.0k, CB = Low
CB	Current Boost		31.3	33.3	35.5	%	R_W = 10k, CB = High
ΔI_{RW}	Difference in Write Current $I_{R/W2} - I_{R/W1}$	6,7					
				0.003	0.015	mA	R = 10k, IWRS = Low
				0.005	0.030	mA	R = 5.0k, IWRS = Low

Note 2 $I_{AVG} = \frac{I_{R/W1} + I_{R/W2}}{2}$

AC SWITCHING CHARACTERISTICS

Test Conditions: V_{CC1} = 5.0 V, T_A = 25°C, V_{CC2} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA, unless specified otherwise (refer to Figure 1).

PARAMETERS	F_{IN} Note 4	MIN	TYP	MAX	UNIT
1. Delay from Head Select going through 0.8 V to CT0 going high through 20 V.	HS, Pin 13		1.6	4.0	µs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS		2.1	4.0	µs
3. Delay from Head Select going high through 2.4 V to CT0 going low through 1.0 V.	HS		1.7	4.0	µs
4. Delay from Head Select going high through 2.4 V to CT1 going high through 20 V.	HS		1.4	4.0	µs
5. Delay from R/W going low through 0.8 V to CT0 going low through 1.0 V.	R/W, Pin 4		1.3	4.0	µs
6. Delay from R/W going low through 0.8 V to CT1 going high through 20 V.	R/W, Pin 4		0.8	4.0	µs
7. Delay from R/W going low through 0.8 V to CT0 going high through 20 V.	R/W, Pin 4		0.75	4.0	µs
8. Delay from R/W going low through 0.8 V to CT1 going low through 1.0 V.	R/W, Pin 4		1.2	4.0	µs
9. After R/W goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	R/W, Pin 4	20	750		ns
10. After R/W goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	R/W, Pin 4	20	1200		ns
11. After R/W goes high, delay from R/W2 turning off through 10% to CT0 going low through 2.0 V.	R/W, Pin 4	20	1200		ns
12. After R/W goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	R/W, Pin 4	20	600		ns
13. After R/W goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	R/W, Pin 4	20	750		ns
14. After R/W goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	R/W, Pin 4	20	750		ns
15. After R/W goes low, fall time (10-90%) of R/W1.	R/W, Pin 4		5.0	200	ns
16. After R/W goes low, fall time (10-90%) of R/W2	R/W, Pin 4		5.0	200	ns
17 Set-up time, HS going low before R/W going low.	R/W, Pin 4	4.0			µs
18. Write Data low Hold Time.	WD, Pin 5	200			ns
19. Write Data high Hold Time.	WD, Pin 5	500			ns
20. Delay from R/W going high through 2.0 V to R/W1 turning off through 10% of on value.	R/W, Pin 4		3.9		µs
21. Delay from R/W going low through 0.8 V to inhibit going low 0.5 V (Note 5).	R/W, Pin 4		0.08	4.0	µs
22. After R/W goes high, delay from R/W1 turning off through 10% to inhibit going high, through 1.5 V (10k pull-up on inhibit) (Note 5)	R/W, Pin 4	20	750		ns
23. After R/W goes high, delay from E1 going high through 23 V to inhibit going through 1.5 V (10k pull-up on inhibit) (Note 5).	R/W, Pin 4	20	750		ns

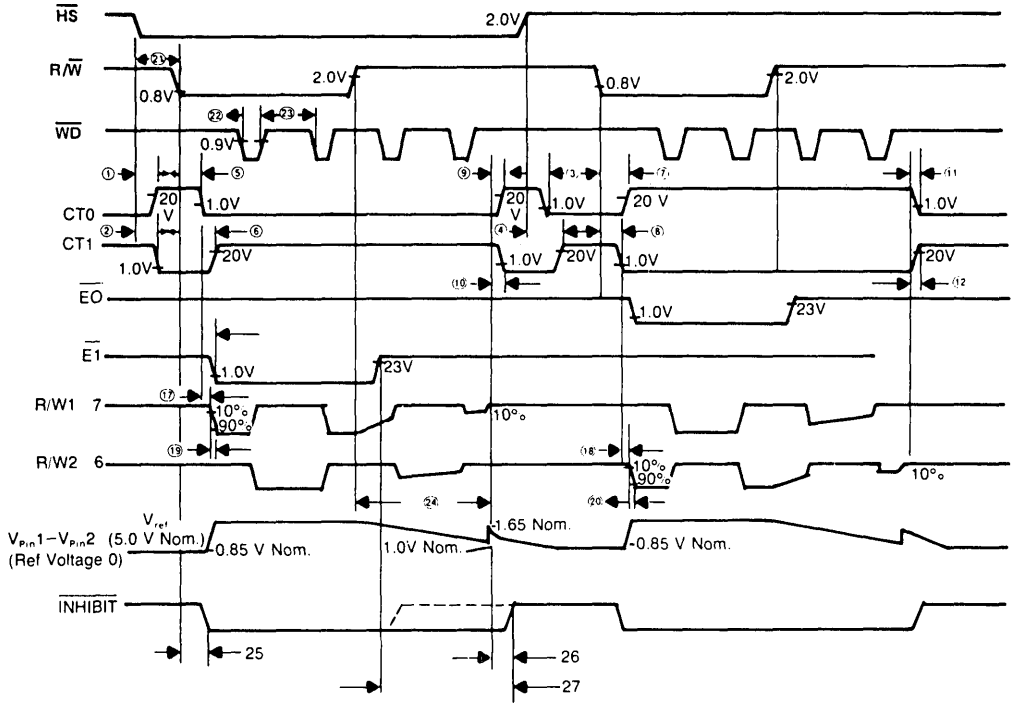


Figure 1. AC Timing Diagram

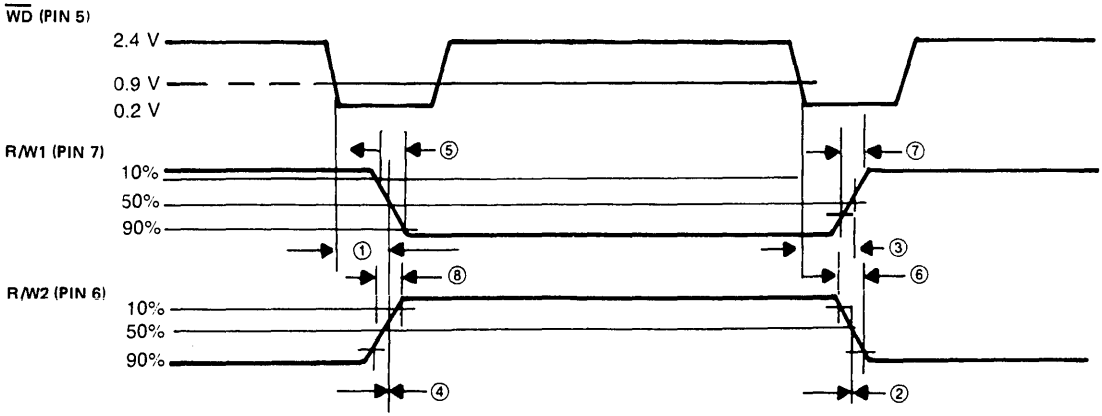


Figure 2. R/W1 and R/W2 Relationship

AC CHARACTERISTICS Continued

Test Conditions: V_{CC1} = 5.0 V, T_A = 25°C, V_{CC2} = 24 V, R/W = 0.4 V, unless specified otherwise (refer to Figure 2).

	PARAMETERS (Note 6)	MIN	TYP	MAX	UNIT
1.	Delay from Write Data going low through 0.9 V to R/W1 turning on through 50%.		85		ns
2.	Delay skew difference of R/W1 turning off and R/W2 turning on through 50% after Write Data going low through 0.9 V.	−40	1.0	40	ns
3.	Delay from Write Data going low through 0.9 V to R/W1 turning off through 50%.		80		ns
4.	Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after WD going low through 0.9 V.	−40	1.0	40	ns
5.	Rise time, 10 to 90% of R/W1.		1.7	200	ns
6.	Rise time, 10 to 90% of R/W2		1.7	200	ns
7.	Fall time, 90 to 10% of R/W1		12	200	ns
8.	Fall Time, 90 to 10% of R/W2.		12	200	ns

Note 3 Test numbers refer to encircled number in Figure 1.

Note 4 AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 13	50 kHz	0.4 to 2.4 V	50%
R/W, Pin 4	50 kHz	0.4 to 2.4 V	50%
WD, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

Note 5 26 or 27, whichever produces the longer delay, will control inhibit.

Note 6 Test numbers refer to encircled numbers in Figure 2. f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

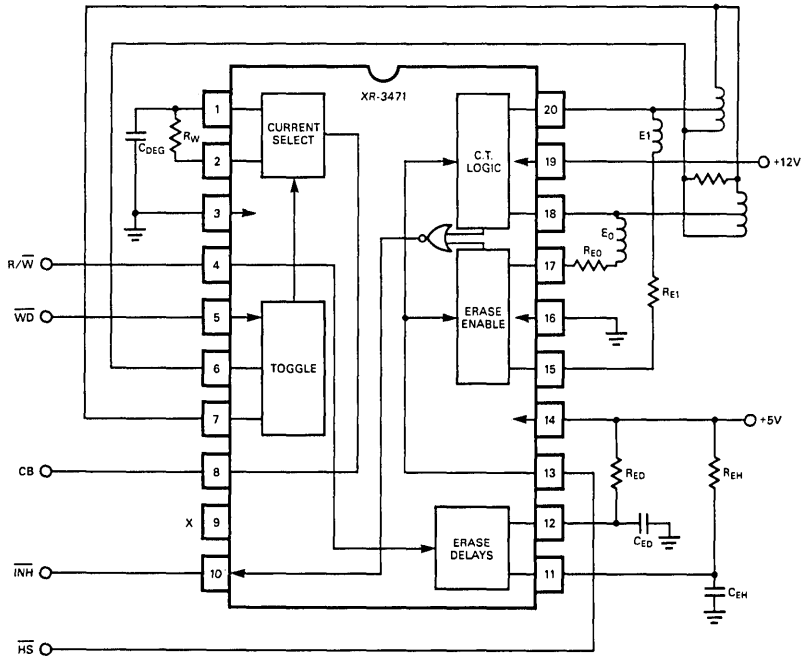


Figure 3. XR-3471 Typical Application Schematic

PIN DESCRIPTION TABLE

NAME	SYMBOL	PIN	DESCRIPTION
Head Select	HS	13	Head Select input selects between head I/O pins center-tap, erase, and read write. A HIGH selects Head 0 and a LOW selects Head 1.
Read/Write Select	R/W	4	This input selects the write mode when LOW, the read mode when HIGH.
Write Data	W/D	5	Write Data input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
Current Boost	CB	8	Current Boost selects the amount of write current used. When LOW, the current equals the value according to the external resistor. When HIGH, the current equals the low current +33%.
V_{ref} I_{ref}	V_{ref} I_{ref}	1 2	A resistor between these pins sets the write current. A 10 k resistor produces 3 mA of write current.
Center-tap 0	CT0	18	Center-tap 0 output is connected to the center tap Head 0. It will be pulled to GND or V_{CC2} (+12 or +24) depending on mode and head selection.
Erase 0	E0	17	Erase 0 will be LOW for writing on Head 0, and floating for other conditions.
Center-tap 1	CT1	20	Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to GND or V_{CC2} (+12 or +24) depending on mode and head selection.
Erase 1	E1	15	Erase 1 will be LOW for writing on Head 1, and floating for other conditions.
R/W1 R/W2	R/W1 R/W2	7 6	These pins are the differential outputs, connected directly to the magnetic heads.
	V_{CC1}	14	+5 V Power
	V_{CC2}	19	+12 V or +24 V Power
	PGND	16	Coil grounds
	GND	3	Reference and logic ground
T_{ED} ON	T_{ED}	12	Erase turn on delay control (RC or logic).
T_{EH} OFF	T_{EH}	11	Erase Hold (turn off delay) control (RC or logic).
INHIBIT	INH	10	Inhibit is an open collector output pulled low whenever the leads are in the write, degauss, or erase mode. Inhibit is used for step or read inhibit.

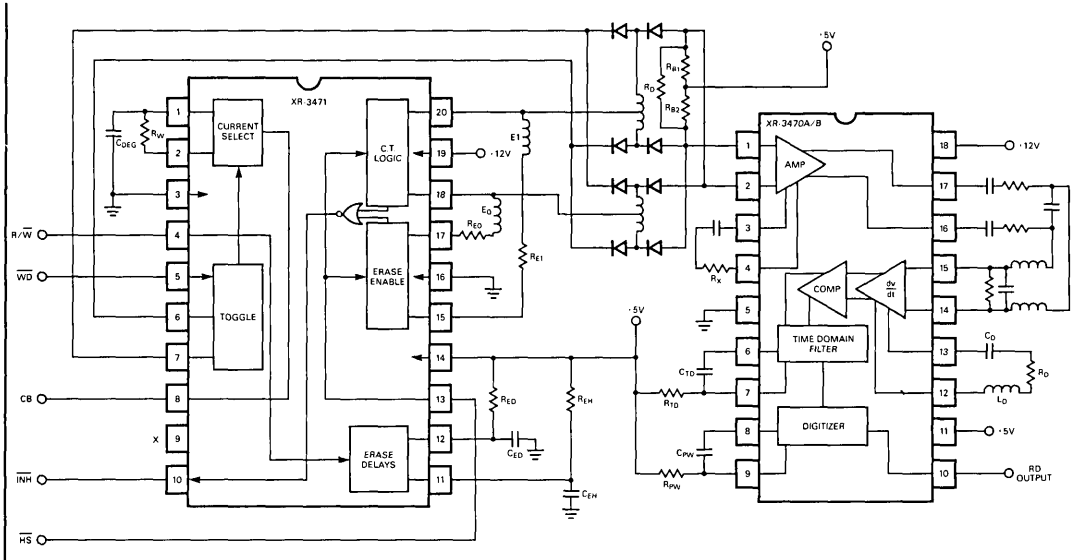


Figure 4. Dual Head Floppy Drive Using the XR-3470 and XR-3471

TYPICAL APPLICATIONS

The XR-3471 is designed for use with the XR-3470 Read Amplifier. A complete dual head floppy disk signal processing chain includes the XR-3470, XR-3471, and a head selection switching matrix. Figure 3 shows the XR-3471 in a typical application. Figure 4 shows the XR-3470 and the XR-3471 in a complete floppy drive.

Component Selection

Write current is set by R_W. Figure 5 shows the relationship between I_W and R_W.

Erase current is limited by external resistors, R_{E0} and R_{E1}.

$$I_E \approx \frac{V_{CC2} - 1.5\ V}{R_E}$$

Tunnel erase delay times are determined by external resistors and capacitors. Erase delay, the time between the write mode is selected and erase current flows equals

$$T_{ED} = R_{ED}\, C_{ED}$$

Erase Hold, the time between the end of writing and cessation of erasure is found as

$$T_{EH} = R_{EH}\, C_{EH}$$

In Figure 4, the head selection is performed by standard switching diodes. C_{DEG} controls degaussing times and may be omitted in systems not requiring degaussing. The reader is directed to the XR-3470 data sheet for a discussion of read circuit component selection.

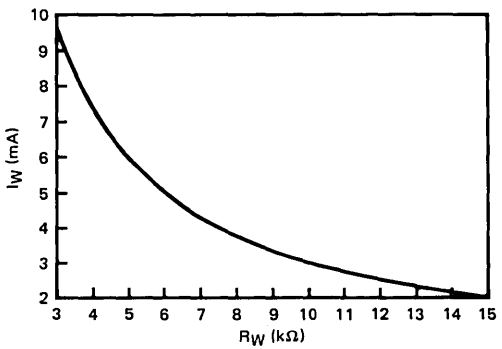


Figure 5. Write Current Dependence on R_W

EXAR

Section 5 – Industrial Circuits

Fundamentals of Operational Amplifiers

The "ideal" operational amplifier can be defined as a voltage-controlled voltage amplifier circuit which offers infinite voltage gains with an infinite input impedance, zero output impedance, and infinite bandwidth. The advantage of such an idealized block of gain is that one can perform a large number of mathematical "operations", or generate a number of circuit functions by applying passive feedback around the amplifier.

The key features of operational amplifier application can be illustrated using the simple feedback circuit of Figure 1, and assuming that the operational amplifier has infinite gain and infinite input impedance. Then, the following two conditions have to be satisfied:

a) Since the voltage gain is infinite, the net voltage across the input terminals of the operational amplifier must be zero, if the operational amplifier output voltage is to be finite. In the circuit of Figure 1, this causes the inverting input terminal of the operational amplifier to behave as a "virtual ground".

b) Since the input impedance of the ideal operational amplifier is infinite, no input current is drawn by the operational amplifier, the total current going into the circuit node connected to the inverting input of the operational amplifier (node Q in Figure 1) must be equal to the total current coming out, i.e.:

$$I_S = -I_F \text{ and } \frac{V_{IN}}{R_S} = -\frac{V_O}{R_F} \qquad (1)$$

Solving for the overall voltage gain, one obtains:

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_S} \qquad (2)$$

Because of this property, the noninverting input of an operational amplifier is often referred to as its "summing input".

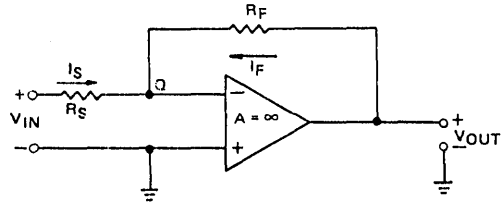


Figure 1. The "Ideal" Operational Amplifier as a Feedback Amplifier

In the case of actual operational amplifiers, both the voltage gain and the input impedance are quite high, but still finite. Figure 2 shows the same basic feedback circuit assuming that the amplifier now has a finite input resistance, R_{IN}, and a finite voltage gain A. For simplicity, the output impedance of the operational amplifier is assumed to be negligible. The overall voltage gain of the circuit can now be expressed as:

$$A_V = V_{OUT}/V_{IN} = -\frac{R_F}{R_S}\left[\frac{1}{1+\frac{1}{A}(1+R_F/R_S+R_F/R_{IN})}\right] \qquad (3)$$

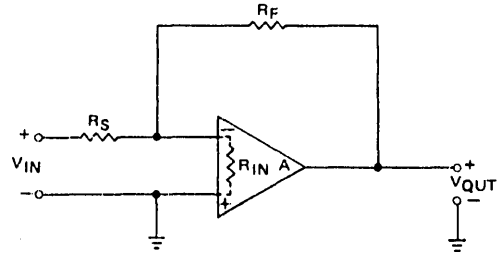


Figure 2. Basic Feedback Configuration Using an Operational Amplifier With Finite Input Impedance and Gain

It should be noted that, for large values of R_{IN}, as the voltage gain increases (i.e. $A \rightarrow \infty$), this expression rapidly converges to that given in equation 2; and the circuit performance becomes solely determined by the external components.

In addition to having finite gain and input impedance, an actual operational amplifier circuit also has finite input bias currents as well as input offset voltage and currents. A more complete model of a practical operational amplifier is shown in Figure 3 where I_B indicates the finite input bias currents; V_{io} and I_{io} represent the voltage and current offsets associated with the circuit and R_O is the output resistance. Due to non-zero values of V_{io} and I_{io} in a practical operational amplifier circuit, $V_{OUT} \neq 0$ for $V_{IN} = 0$.

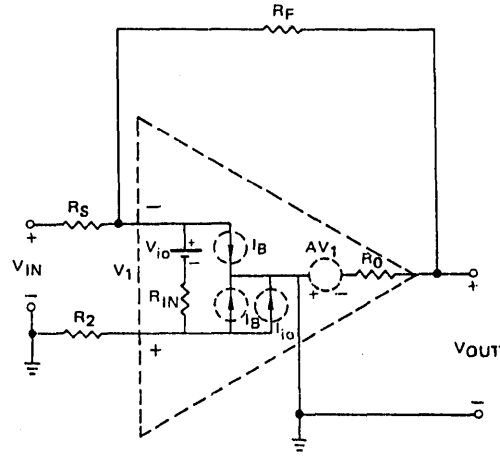


Figure 3. Equivalent Circuit of a Practical Operational Amplifier Showing the Effects of Finite Input Impedance, Current and Voltage Offsets

Definitions of Operational Amplifier Terms

Since the operational amplifier has become a universal building block for circuit and system design, a number of widely accepted design terms have evolved which describe the comparative merits of various operational amplifiers. Some of these terms are defined below:

Input Offset Voltage: The input voltage which must be applied across the input terminals to obtain zero output voltage.

Input Offset Current: The difference of the currents into the two input terminals with the output at zero volts.

Input Bias Current: The average of the two input currents.

Input Common-Mode Range: Maximum range of input voltage that can be simultaneously applied to both inputs without causing cutoff or saturation of amplifier gain stages.

Common-Mode Rejection Ratio: Ratio of the differential open-loop gain to the common-mode open-loop gain.

Supply Voltage Rejection Ratio: Input offset voltage change per volt of supply voltage change.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Full-Power Bandwidth: Maximum frequency over which the full output voltage swing can be obtained.

Unity-Gain Bandwidth: Frequency at which the open loop voltage gain is equal to unity.

Slew Rate: The maximum time rate of change of the output voltage, for a voltage step applied to the input. It is normally measured at the zero crossing point of the output voltage swing with the amplifier frequency compensated for unity gain.

Overload Recovery Time: Time required for the output stage to return to active region, when driven into hard saturation.

Gain Margin: The amount by which the voltage gain is below the unity (0 dB) level, at the frequency where the excess phase shift across the amplifier is exactly 180°. It is measured in decibels, and must be positive for unconditional stability.

Phase Margin: 180° minus the excess phase shift at the Frequency where the magnitude of the open loop voltage gain is equal to unity. It is measured in degrees and must be positive for unconditional stability.

Basic Applications of Operational Amplifiers

The general usefulness of the operational amplifier stems from the fact that when used in a feedback loop, its overall performance and transfer characteristics are determined almost totally by the choice of feedback components. To be universally useful in such an application, the "ideal" operational amplifier should exhibit infinite gain, infinite input impedance and infinite bandwidth. Although these are all idealized characteristics, the practical monolithic operational amplifiers closely approximate these features, particularly for low frequency applications.

The availability and the low-cost of the integrated operational amplifier makes it an extremely versatile building block for analog system or equipment design. Therefore, it is mandatory that the circuit designer be familiar with the fundamental applications of operational amplifiers. This section of Exar's Operational Amplifier Data Book is intended to familiarize the designer with some of the simple but fundamental circuit configurations using IC operational amplifiers. The discussion is slanted toward the practical applications of operational amplifiers, as controlled by the external feedback circuitry. The particular operational amplifier parameters will be discussed as they effect the circuit performance and accuracy.

The integrated operational amplifiers shown in the figures are for the most part internally compensated, so frequency stabilization components are not shown: however, other amplifiers using external compensation may be utilized to achieve greater operating speed in many circuits.

The Inverting Amplifier

The basic operational amplifier circuit is shown in Figure 1. This circuit gives closed-loop gain of R_2/R_1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R_1. The closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only cautions to be observed are that R_3 should be chosen to be equal to the parallel combination of R_1 and R_2 to minimize the offset voltage error due to bias current; and that there will be a DC offset voltage error due to bias current; and that there will be a DC offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier; however, the contribution due to input bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment, the source resistance for both inputs should be equal. In this case, the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances, and offset current causes the main error for high source resistances.

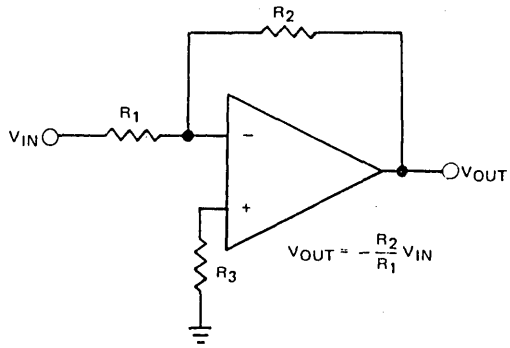


Figure 1. Inverting Amplifier

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R_3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak-to-peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the combined gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously, the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where feedback network attenuation is high, i.e., the amount of feedback around the amplifier is low. The compensation trade-off for a particular connection is stability versus bandwidth. Larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

The Non-Inverting Amplifier

Figure 2 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of ($R_1 + R_2$) to R_1. Its closed-loop 3-dB bandwidth is equal to the amplifier unity-gain frequency divided by the closed-loop gain.

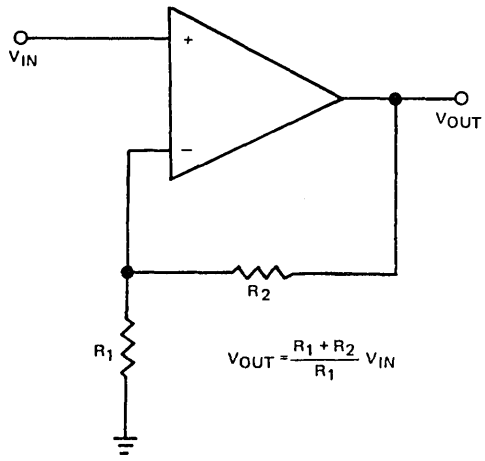


Figure 2. Non-Inverting Amplifier

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain (open-loop gain/closed-loop gain). In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance. To minimize the output error due to the input bias current of the operational amplifier, ($R_1 + R_2$) should be chosen equal to the source impedance of the input signal. Applications cautions are the same for this amplifier as for the inverting amplifier with one exception: the amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.

The Unity-Gain Buffer

The unity-gain buffer is shown in Figure 3. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common-mode rejection, whichever is less. Input impedance is a misleading concept in a DC coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance.

The cautions to be observed in applying this circuit are as follows: the amplifier must be compensated for unity-gain operation, and the output swing of the amplifier may be limited by the amplifier common-mode range. The input signal swing should not exceed the input common-mode range, since this may cause a latch-up condition.

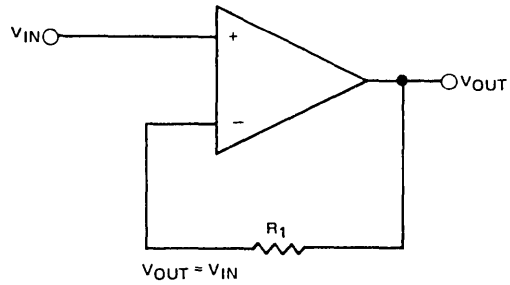


Figure 3. Unity-Gain Buffer

Summing Amplifier

The summing amplifier, a special case of the inverting amplifier, is shown in Figure 4. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of any input of this circuit is equal to the inverse ratio of the appropriate input resistor to the feedback resistor, R_4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in Figure 1 by assuming the input resistor to be the parallel combination of R_1, R_2, and R_3. Application cautions are the same as those for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of this bandwidth as is discussed in the section describing the simple inverting amplifier.

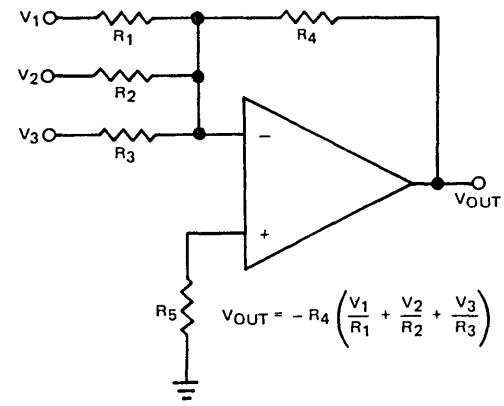


Figure 4. Summing Amplifier

The advantage of this circuit is that there is no interaction between inputs, therefore, operations such as summing and weighted-averaging are implemented very easily.

The Difference Amplifier

The difference amplifier is the complement of the summing amplifier and allows the subtraction of two voltages or, as a special case, the cancellation of a single common to the two inputs. This circuit is shown in Figure 5 and is useful as a computational amplifier, in making a differential to single-ended conversion, or in rejecting an unwanted common-mode signal.

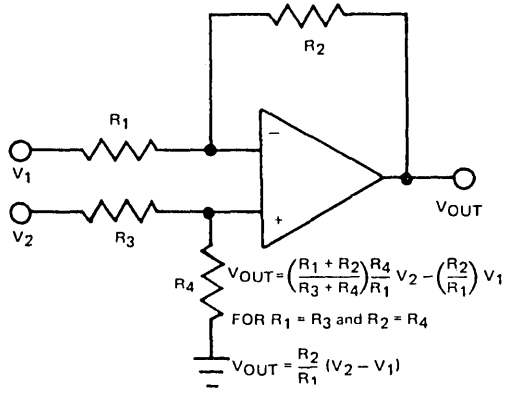


Figure 5. Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal: inverting input impedance is the same as for the inverting amplifier of Figure 1 and the noninverting input impedance is the sum of R_3 and R_4. Gain for either input is the ratio of R_1 to R_2 for the special case of a differential input single-ended output where $R_1 = R_3$ and $R_2 = R_4$. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

Differentiator Circuit

The basic principle of a differentiator circuit is shown in the simplified connection diagram of Figure 6. However, although mathematically accurate, this particular connection is not directly useful in practice because it is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator made up of the resistor R_3 and the capacitor C_3 is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity-gain.

A practical differentiator which corrects the high frequency noise problem is shown in Figure 7. Here both the stability and noise problems are corrected by addition of two additional components, R_1 and C_2. R_2 and C_2 form a 6 dB per octave high frequency roll-off in the feedback network, and R_1C_1 form a 6 dB per octave roll-off network in the input network for a total high frequency roll-off of 12 dB per octave, to reduce the effect of high frequency input and amplifier noise. In addition R_1C_1 and R_2C_2 form lead networks in the feedback loop which, if placed below the amplifier unity-gain frequency, provide 90° phase lead to compensate the 90° phase lag of R_2C_1 and prevent loop instability.

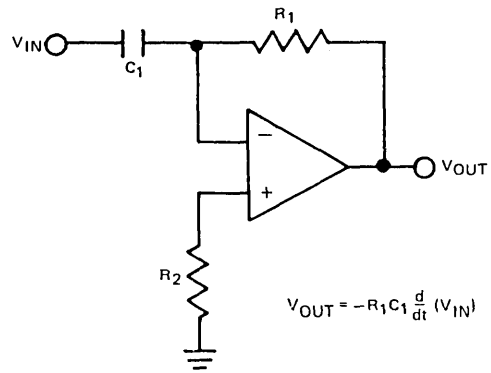


Figure 6. Basic Differentiator Connection

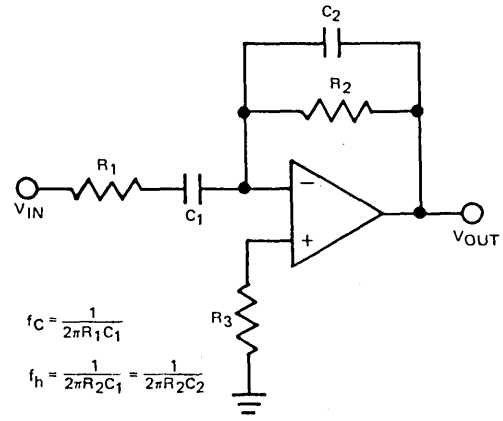


Figure 7. Practical Differentiator Circuit

Integrator Circuit

Figure 8 shows the basic circuit connection for performing the mathematical operation of integration. This circuit is essentially a low-pass filter with a constant frequency roll-off of −6 dB per octave.

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as the double-pole, single-throw switch S_1. When S_1 is in position 1, the amplifier is connected in unity-gain configuration, and capacitor C_1 is discharged, setting an initial condition of zero volts. When S_1 is in posi-

tion 2, the amplifier is connected as an integrator, and its output will be the time-integral of the input voltage.

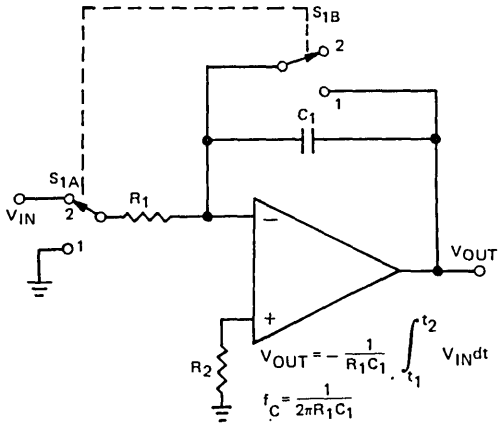


Figure 8. The Integrator Circuit

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity-gain operation and R_2 must equal R_1 for minimum error due to bias current.

Simple Low-Pass Filter

The simple low-pass filter is shown in Figure 9. This circuit has a 6 dB per octave roll-off after a closed-loop 3-dB point defined by f_C. Gain below this corner frequency is defined by the ratio of R_3 to R_1. The circuit may be considered as an AC integrator at frequencies well above f_C; however, the time domain response is that of a single RC rather than an integral.

A gain vs. frequency plot of circuit response is shown in Figure 10 to illustrate the difference between this circuit and the true integrator. Note that the frequency response is flat for frequencies below f_C

$$\text{where } f_C = \frac{1}{2\pi R_3 C_1}$$

Current-to-Voltage Converter

Current may be measured in two ways with an operational amplifier: the current may be converted into a voltage with a resistor and then amplified or it may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage converter avoids both of these problems.

The current-to-voltage converter is shown in Figure 11. The input current is fed directly into the summing note, and the amplifier output voltage changes to extract the same current from the summing node through R_1. The

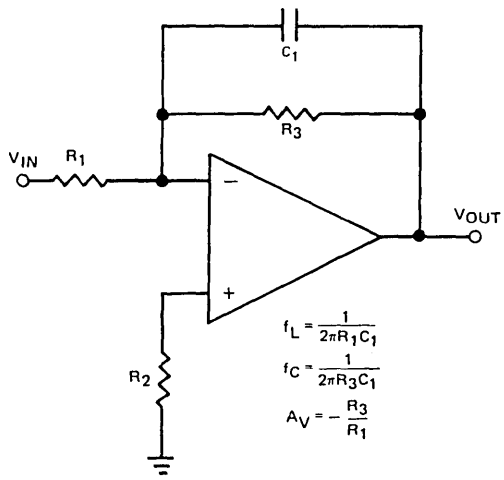


Figure 9. A Simple Low-Pass Filter Circuit

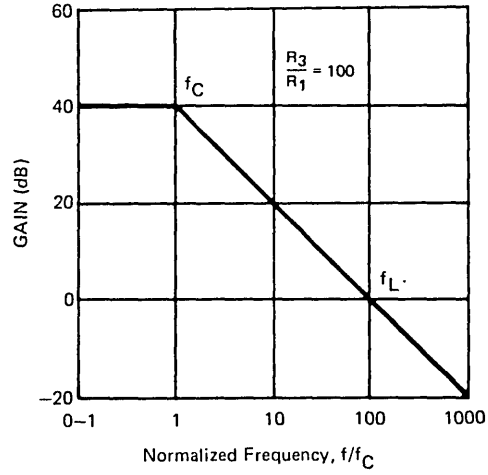


Figure 10. Frequency Response of the Simple Low-Pass Filter

scale factor of this circuit is R_1 volts per ampere of current. The only conversion error in this circuit is the bias current of the operational amplifier input which is summed algebraically with the input current, I_{IN}. The main design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation.

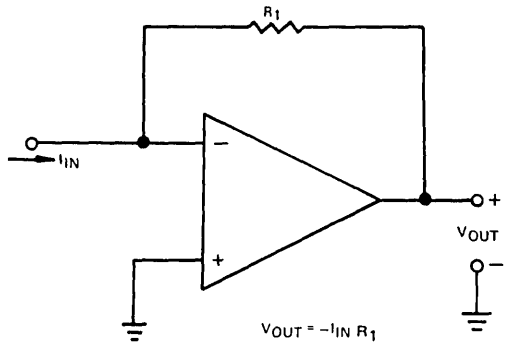


Figure 11. Operational Amplifier as a Current-to-Voltage Converter

Voltage Controlled Current-Source

Figures 12, 13, and 14 show three simple circuit configurations for voltage-controlled constant-current stages. The circuit of Figure 12 is a basic current-sink circuit which uses a pair of Darlington connected NPN transistors external to the operational amplifier. Assuming that the base current of T_1 is negligible compared to the controlled current I_0, the current of the output transistors is equal to V_{IN}/R_1.

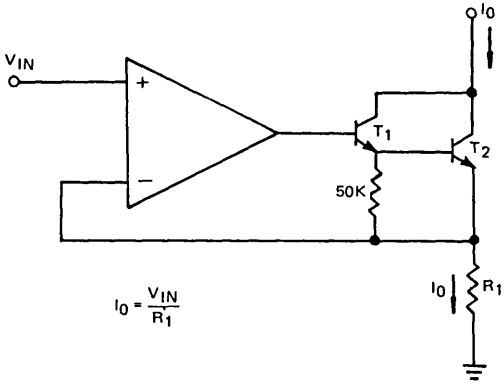


Figure 12. Voltage-Controlled Current-Sink Circuit

Figure 13 shows a current-source circuit which uses a composite connection of external PNP and NPN transistors and produces a constant output current which is proportional to the net voltage drop across the sensing resistor, R_1.

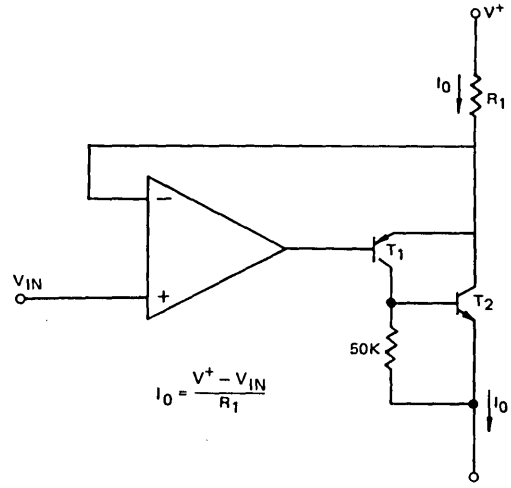


Figure 13. Voltage-Controlled Current-Source Circuit

Figure 14 shows an alternate approach to obtaining a voltage-controlled current source which does not require additional active devices. The circuit provides an output current proportional to the input voltage V_{IN}. If the resistors R_1 through R_4 are chosen to be equal and much larger than R_5, then the output current is:

$$I_{OUT} = V_{IN}/R_5$$

The above expression assumes that the current through R_3 is much smaller than I_0.

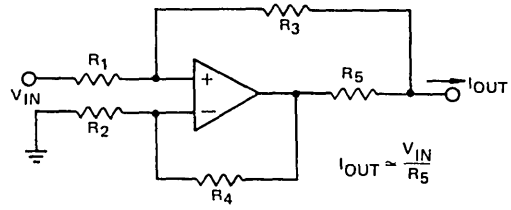


Figure 14. A Voltage-Controlled Current Source Circuit Which Does Not Require External Active Devices

This circuit can supply an output current of either polarity, up to the maximum positive or negative output current available from the operational amplifier. The maximum voltage compliance of the output is limited by the output swing of the operational amplifier minus the voltage drop across the sensing resistor, R_5.

Triangle Wave Oscillator

A constant amplitude triangular wave generator is shown in Figure 15. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency. This entire circuit can be built inexpensively, using a dual operational amplifier IC, such as the XR-4558.

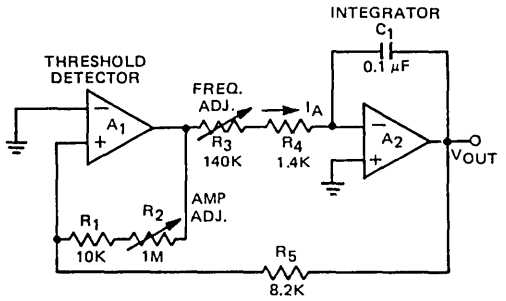


Figure 15. A Simple Triangle Wave Oscillator

The generator embodies an integrator as a ramp generator and a threshold detector with hysteresis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a Schmitt trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the noninverting input which is determined by the attenuation of the feedback loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When this is done, the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R_3 and R_4 causing the current I_A to flow.

The integrator then generates a negative-going ramp with a rate of I_A/C_1 volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state, and supplies a negative current, I_B, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of I_B/C_1 volts per second until its output equals the positive trip point of the threshold detector, where the detector again changes output state and the cycle repeats.

Triangular wave frequency is determined by R_3, R_4 and C_1 and the positive and negative saturation voltages of the amplifier A_1. Amplitude is determined by the ratio of R_5 to the combination of R_1 and R_2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A_1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes.

The integrator section should be compensated for unity-gain. The detector section may require compensation if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to the input bias current for maximum symmetry; and offset voltage should be small with respect to peak output voltage swing.

Choosing the Right Op Amp

Because of its versatility and ease of application, the op-amp is often the easiest active component to design into the circuit. However, once the initial "paper design" is accomplished, the user is faced with the key question: which op-amp is the best choice for the particular application? The availability of a very wide choice of IC op-amps of varying part numbers, types and features does not make the answer to this question an easy one. If the op-amp characteristics are not carefully considered, the total system performance may be degraded: similarly if each op-amp is overspecified with an excessive amount of "overkill" for the particular application, then the system cost will increase unnecessarily. The key selection criteria is finding the lowest cost operational amplifier which will be sufficient to meet the system performance requirements. This section provides a brief summary of various classes of IC op-amps, their features and key applications, to assist the user in choosing the most cost-effective operational amplifier for his application.

General Purpose Op-Amps

A wide variety of op-amp applications such as low-frequency amplifiers, active filters, voltage-to-current converters and voltage regulators are most economically accomplished using the low-cost general purpose IC op-amps. These op-amps are almost all variations of the basic 741-type op-amp, and offer significant cost savings over any special-purpose op-amps. They are commercially available in single, dual or quad versions. The dual and quad op-amps are particularly cost-effective for applications such as active filters which require a multiplicity of op-amps. The cost per op-amp is usually lower if one can use multiple op-amp IC's rather than single op-amps.

The single and dual general purpose op-amps are available in both internally compensated and uncompensated versions. The quad op-amps are almost invariably internally compensated, to reduce the IC package pin count. Most general purpose IC op-amps have comparable electrical characteristics, namely open loop gain of $\geq$ 20 mV/V, small-signal unity gain bandwidth of 1 to 2 MHz and a slew rate of $\approx 1V/\mu sec$.

Exar manufactures a wide choice of dual or quad general purpose op-amps. All of these op-amps are internally compensated to make them cost-effective and reduce the external parts count. Exar's general purpose op-amps recommended for most applications are XR-1458 and XR-4558 for duals, and XR-4136, XR-4212 and XR-4741 for quad op-amps.

Ground Sensing Op-Amps

These types of op-amps have an input stage common-mode range which extends all the way to the negative supply rail. This is obtained by using Darlington-connected PNP transistors at the input stage of the op-amp. The key advantage of this class of op-amps is that they can be operated with a single positive supply, and still be able to detect or sense small signals near ground potential. The particular circuit recommended for this application is Exar's XR-3403 quad operational amplifier.

Programmable Op-Amps

Programmable op-amps allow the user to "program" or set the operating current levels within the IC op-amp by means of an external setting resistor, and thus be able to trade-off power dissipation for slew-rate or signal bandwidth. These circuits are normally available in quad form, where the power levels of all or some of the op-amps in the package can be programmed by one or two external setting resistors. The key areas of applications for programmable op-amps are active filters and telecommunication channel filters where the user is normally concerned with power dissipation. These op-amps can also be programmed to operate at micro-power levels, by the choice of external setting resistors.

The programmable quad operational amplifiers are available with either one or two separate setting controls. Those with a single setting control have all four of the operational amplifiers programmed from same current setting control. Those with two setting controls have the four op-amps on the chip programmed either in groups of two, or in groups of one and three op-amps. The advantage of partitioned programming is that some of the op-amps in the IC package can be operated at a different power or bandwidth level than the rest of the op-amps in the same chip. For example, in an active filter application, the three op-amps performing the filtering can be operated at a low-power level, yet the fourth op-amp which may be serving as an output buffer can be operated at a higher power level to provide load-drive capability.

Exar offers the broadest product line of programmable op-amps in the industry: The XR-4202, XR-146 and the XR-346-2 families of op-amps are all-bipolar programmable quad op-amp circuits. The XR-4202 offers a single current-setting control for all of the four op-amps on the chip; the XR-146 and the XR-346-2 offer partitioned programming of the four op amps. The XR-094 and XR-095 families are programmable FET-input quad op-amps which have the same pin configuration as the XR-146 and the XR-346-2 families, respectively. These programmable FET-input quad op-amps are fabricated using Exar's ion-implanted bipolar/FET or BIFET process technology which combines matched junction FETs and high-performance bipolar transistors on the same chip.

FET-Input Op-Amps

Finite input impedance or input bias currents associated with conventional bipolar op-amps can be a problem in specific applications such as sample-hold circuits or signal sensing applications from high-

impedance signal source such as transducer systems. For such applications, op-amps with junction-FET input stages offer significant performance advantages since they offer input resistances of the order of 10^{12} ohms, and input bias currents in the low pico-ampere range. Another unique feature of FET-input op-amps is their high slew-rate and wide bandwidth. For example, most FET-input op-amps offer slew-rates in excess of 10 V/μsec and unity gain bandwidth of 3 MHz.

The FET-input op-amps offer somewhat higher offset voltages and input noise than all-bipolar op-amps.

Exar offers a wide selection of FET-input dual and quad op-amps which are manufactured using Exar's ion-implanted BIPOLAR/FET process. The XR-082/XR-083 are dual op-amps; the XR-084 is a quad FET-input op-amp. The XR-094 and the XR-095 are programmable quad FET-input op-amps. Because of their low power capability, the programmable JFET op-amps are particularly suitable for low-power active filter designs.

Low Noise Op-Amps

These op-amps are particularly suited for audio amplifier and mixer applications, where low noise is of prime importance. The noise characteristics of an op-amp are determined by the noise generated at the input stage, since the noise generated at this point is amplified by the full open-loop gain of the amplifier. In most cases, input noise voltages of 10 nV/$\sqrt{\text{Hz}}$ or less is required to be suitable for high quality or professional audio signal processing applications. Such low noise characteristics are normally obtained by careful device design and manufacturing processing of the IC chips. In general, all-bipolar operational amplifiers tend to have better low noise characteristics than the FET-input op-amps. Exar manufactures a number of low noise op-amp circuits uniquely suited to audio applications. Among Exar's family of low noise op-amps, the XR-5534 operational amplifier, and its dual versions, the XR-5532 and the XR-5533 offer the best noise performance.

Low Distortion Op-Amps

In addition to low noise characteristics, another key performance requirement for audio applications is low distortion. The distortion characteristics of op-amps are normally determined by the design of the output stage as well as the amplifier bandwidth characteristics. The total harmonic distortion (THD) is made up of three components: (a) intermodulation distortion; (b) cross-over distortion which depends on output stage design, and (c) slew-induced distortion which occurs when the output of the op-amp is forced to slew faster than its slew-rate.

The cross-over distortion can be avoided by using op-amps which have class-AB, rather than class-B type output stages. All of Exar's op-amps fall into this category.

To avoid slew-induced distortion, one should ensure that the slew rate of the amplifier is never exceeded during the excursions of the input signal. The high-speed operational amplifiers such as Exar's XR-5533 or XR-5534 op-amps which have slew rates in excess of 10 V/μsec with a power bandwidth of 200 kHz can easily cover the entire audio frequency range without introducing slew-induced distortion.

Dual Bipolar JFET Operational Amplifier

GENERAL DESCRIPTION

The XR-082/XR-083 family of dual bipolar JFET operational amplifiers are designed to offer higher performance than conventional bipolar op amps. Each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. These operational amplifier circuits are fabricated using ion-implantation technology which combines well-matched junction JFETs and high-performance bipolar transistors on the same monolithic chip.

The XR-082 of family of dual bipolar JFET op amps are packaged in 8-pin dual-in-line packages. The XR-083 family of op amps offer independent offset adjustment for each of the individual op amps on the same chip, and are available in 14-pin dual-in-line packages.

FEATURES

Direct Replacement for TL082/TL083
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short Circuit Protection
High Input Impedance . . JFET Input Stage
Internal Frequency Compensation
Latch-Up-Free Operation
High Slew Rate . . 13 V/μs, Typical

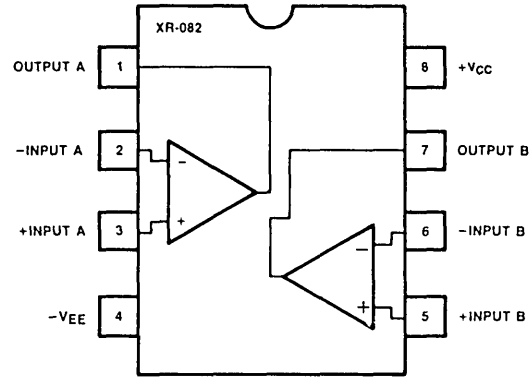
APPLICATIONS

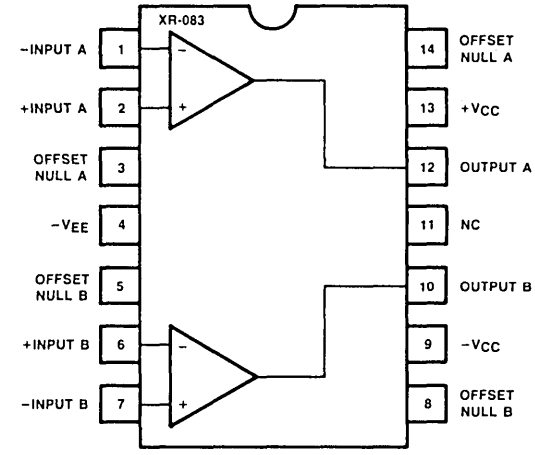
Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 1)	±15V
Output Short Circuit Duration (Note 2)	Indefinite
Package Power Dissipation:	
Plastic Package	625 mW
Derate Above T_A = +25°C	5.0 mW°C
Ceramic Package	750 mW
Derate Above T_A = +25°C	6.0 mW/°C
Storage Temperature Range	−65°C to + 150°C

FUNCTIONAL BLOCK DIAGRAMS





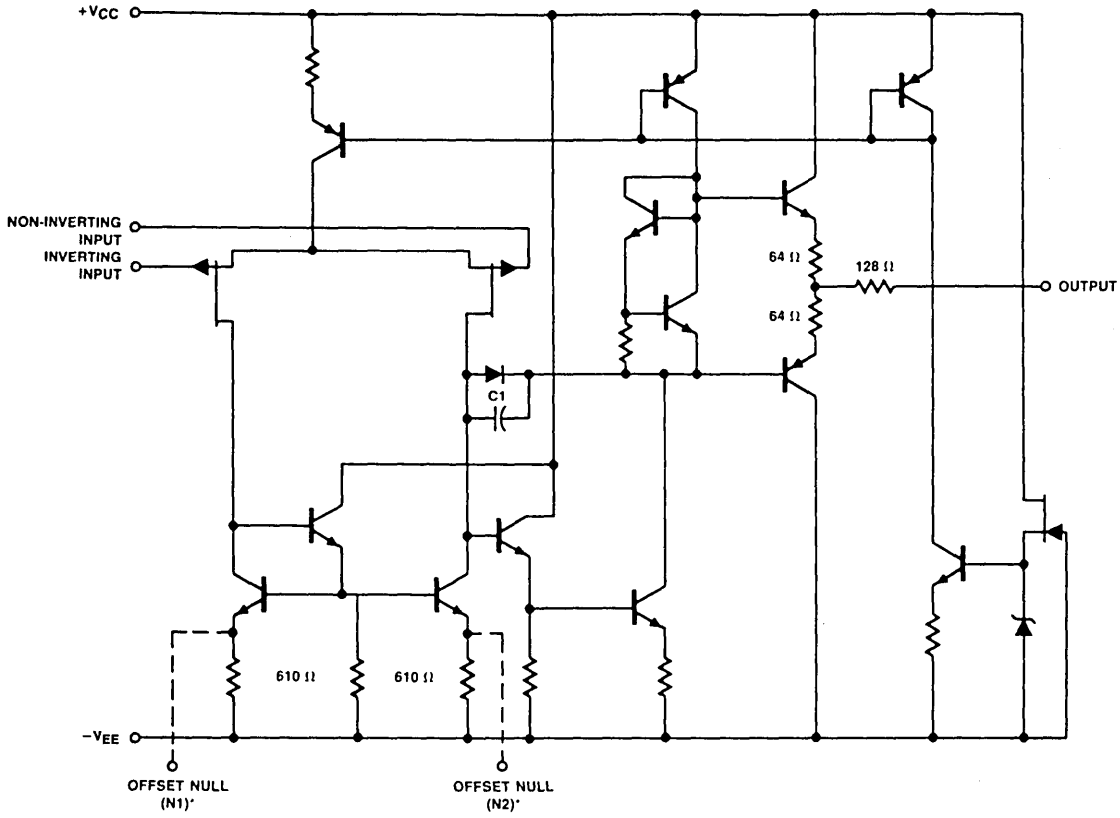
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-082M/XR-083M	Ceramic	−55°C to +125°C
XR-082N/XR-083N	Ceramic	−25°C to + 85°C
XR-082P/XR-083P	Plastic	−25°C to + 85°C
XR-082CN/XR-083CN	Ceramic	0°C to + 70°C
XR-082CP/XR-083CP	Plastic	0°C to + 70°C

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = ±15V, unless otherwise specified.

		XR-082M/ XR-083M			XR-082/ XR-083			XR-082C/ XR-083C				
SYMBOL	PARAMETERS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	CONDITIONS
V_{OS} V_{OS}	Input Offset Voltage		3	6 9		3	6 9		5	15 20	mV mV	R_S = 50Ω R_S = 50Ω, T_A = Full Range
$\Delta V_{OS}/\Delta T$	Offset Voltage Temp. Coef.		10			10			10		µV/°C	R_S = 50Ω, T_A = Full Range
I_B	Input Bias Current		30	200		30	200		30	400	pA	
I_B	Input Bias Current Over Temp.			50			20			20	nA	T_A = Full Range
I_{OS}	Input Offset Current		5	100		5	100		5	200	pA	
	Input Offset Current Over Temp.			20			10			5	nA	T_A = Full Range
I_{CC}	Supply Current (per amplifier)		1.4	2.8		1.4	2.8		1.4	2.8	mA	No Load, No Input Signal
V_{ICM}	Input Common Mode Range	±12			±12			±10			V	
A_{VOL}	Voltage Gain	50 25	200		50 25	200		25 15	200		V/mV	R_L ≥ 2 kΩ, V_O = ±10V T_A = Full Range
V_{OPP}	Max. Output Swing (peak-to-peak)	24 24	27		24 24	27		24 24	27		V	R_L ≥ 10 kΩ T_A = Full Range
R_{IN}	Input Resistance		10^{12}			10^{12}			10^{12}		Ω	
BW	Unity-Gain Bandwidth		3			3			3		MHz	
CMRR	Common-Mode Rejection	80	86		80	86		70	76		dB	R_S ≤ 10 kΩ
PSRR	Supply-Voltage Rejection	80	86		80	86		70	76		dB	
	Channel Separation		120			120			120		dB	A_V = 100, Freq. = 1 kHz
dV_{OUT}/DT	Slew Rate		13			13			13		V/µS	A_V = 1, R_L = 2 kΩ, C_L = 100 pF, V_1 = 10V
T_R T_O	Rise Time Overshoot		0.1 10			0.1 10			0.1 10		µsec %	A_V = 1, R_L = 2 kΩ C_L = 100 pF, V_1 = 20 mV
E_N	Equivalent Input Noise Voltage		20			20			20		nV/√Hz	R_S = 100Ω f = 1 kHz

Note 1: For Supply Voltage less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.



EQUIVALENT SCHEMATIC DIAGRAM

Quad Bipolar JFET Operational Amplifier

GENERAL DESCRIPTION

The XR-084 quad bipolar JFET operational amplifier is designed to offer higher performance than conventional bipolar quad op amps. Each of the four op amps on the chip is closely matched in performance characteristics, and each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. The XR-084 JFET input quad op amp is fabricated using ion-implanted bipolar JFET technology which combines well-matched JFETs and high-performance bipolar transistors on the same monolithic integrated circuit.

FEATURES

Direct Replacement for TL084
Same Pin Configuration as XR-3403, LM324
High-Impedance JFET Input Stage
Internal Frequency Compensation
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short Circuit Protection
Latch-Up-Free Operation
High Slew Rate . . . 13 V/μS, Typical

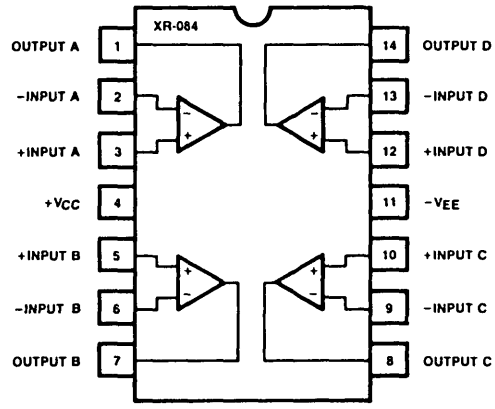
APPLICATIONS

Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 1)	±15V
Output Short Circuit Duration (Note 2)	Indefinite
Package Power Dissipation:	
Plastic Package	625 mW
Derate Above T_A = +25°C	5.0 mW/°C
Ceramic Package	750 mW
Derate Above T_A = +25°C	6.0 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-084M	Ceramic	−55°C to +125°C
XR-084N	Ceramic	−25°C to + 85°C
XR-084P	Plastic	−25°C to + 85°C
XR-084CN	Ceramic	0°C to + 70°C
XR-084CP	Plastic	0°C to + 70°C

SYSTEM DESCRIPTION

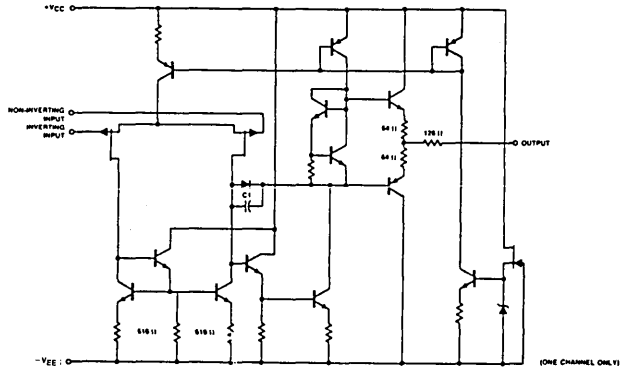
The XR-084 is a quad JFET input operational amplifier featuring extremely high input resistance, low input bias and offset currents, large common mode voltage range, and large output swing range. Unity gain bandwidth is 3 MHz and slew rate is 13V/μS. The devices are unity gain compensated.

XR-084

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = ±15, unless otherwise specified.

		XR-084M			XR-084			XR-084C				
SYMBOL	**PARAMETERS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
V_{OS} V_{OS}	Input Offset Voltage		3	6 9		3	6 9		5	15 20	mV mV	R_S = 50Ω R_S = 50Ω, T_A = Full Range
$\Delta V_{OS}/\Delta T$	Offset Voltage Temp. Coef.		10			10			10		µV/°C	R_S = 50Ω, T_A = Full Range
I_B	Input Bias Current		30	200		30	200		30	400	pA	
I_B	Input Bias Current Over Temp.			50			20			20	nA	T_A = Full Range
I_{OS}	Input Offset Current		5	100		5	100		5	200	pA	
	Input Offset Current Over Temp.			20			10			5	nA	T_A = Full Range
I_{CC}	Supply Current (per amplifier)		1.4	2.8		1.4	2.8		1.4	2.8	mA	No Load, No Input Signal
V_{ICM}	Input Common Mode Range	±12			±12			±10			V	
A_{VOL}	Voltage Gain	50 25	200		50 25	200		25 15	200		V/mV	R_L ≥ 2 kΩ, V_O = ±10V T_A = Full Range
V_{OPP}	Max. Output Swing (peak-to-peak)	24 24	27		24 24	27		24 24	27		V	R_L ≥ 10 kΩ T_A = Full Range
R_{IN}	Input Resistance		10^{12}			10^{12}			10^{12}		Ω	
BW	Unity-Gain Bandwidth		3			3			3		MHz	
CMRR	Common-Mode Rejection	80	86		80	86		70	76		dB	R_S ≤ 10 kΩ
PSRR	Supply-Voltage Rejection	80	86		80	86		70	76		dB	
	Channel Separation		120			120			120		dB	A_V = 100, Freq. = 1 kHz
DV_{OUT}/DT	Slew Rate		13			13			13		V/µS	A_V = 1, R_L = 2 kΩ C_L = 100 pF, V_1 = 10V
T_R T_O	Rise Time Overshoot		0.1 10			0.1 10			0.1 10		µsec %	A_V = 1, R_L = 2 kΩ C_L = 100 pF, V_1 = 20 mV
E_N	Equivalent Input Noise Voltage		20			20			20		nV/√Hz	R_S = 100Ω f = 1 kHz

Note 1: For Supply Voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.



EQUIVALENT SCHEMATIC DIAGRAM

Quad Programmable Bipolar JFET Operational Amplifiers

GENERAL DESCRIPTION

The XR-094 and XR-095 bipolar JFET input quad programmable operational amplifiers consist of four independent, high gain, internally compensated amplifiers. Two external resistors (R_{SET}) allow the user to program supply current, slew-rate, and input noise without the usual sacrifice of gain bandwidth product. For example, the user can trade-off slew-rate for supply current or optimize the noise figure for a given source impedance. Except for the two programming pins at the end of the package, the XR-094 and XR-095 pin-out is the same as the popular 324, 3403, 124, 148 and 4741 operational amplifiers.

In the case of the XR-094, three of the op amps on the chip share a common programming pin; and the fourth op amp is programmed separately. In the case of the XR-095, each pair of op amps share a common programming pin.

FEATURES

Same Pin Configuration as LM-346
High-Impedance FET Input Stage
Internal Frequency Compensation
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short-Circuit Protection
High Slew-Rate . . . 13 V/μs, Typical
Programmable Electrical Characteristics

APPLICATIONS

Total Supply Current = 5.6 mA (I_{SET}/320 μA)
Slew Rate = 13 V/μs (I_{SET}/320 μA)
I_{SET} = Current into set terminal

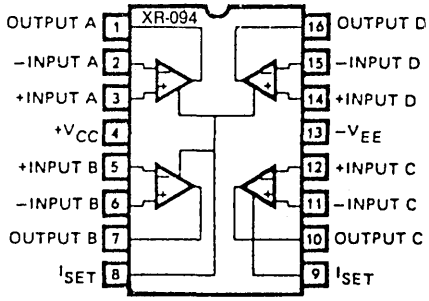
$$I_{SET} = \frac{V_{CC} - (V_{EE} - 0.6V)}{R_{SET}}$$

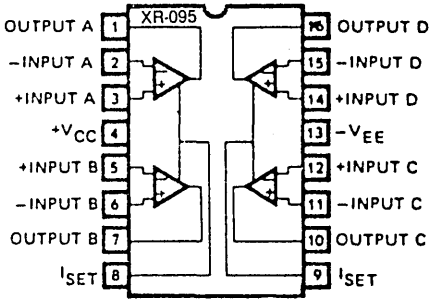
Note. I_{SET} must be $\leq$ 400μA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 1)	±15V
Output Short-Circuit Duration (Note 2)	Indefinite
Package Power Dissipation:	
Plastic Package	625 mW

FUNCTIONAL BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS (Continued)

Derate Above T_A = +25°C	5.0 mV/°C
Ceramic Package	750 mW
Derate Above T_A = +25°C	6.0 mW/°C
Storage Temperature Range	−65°C to +150°C

Note 1: For Supply Voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

ORDERING INFORMATION

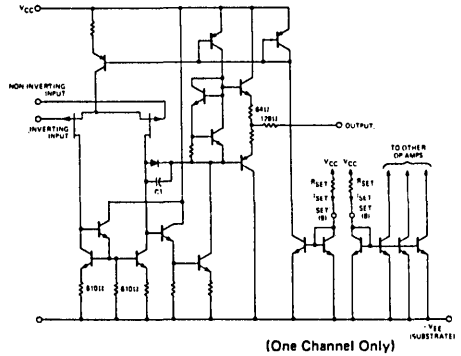
Part Number	Package	Operating Temperature
XR-094/XR-095N	Ceramic	−25°C to +85°C
XR-094/XR-095P	Plastic	−25°C to +85°C
XR-094/XR-095CN	Ceramic	0°C to +70°C
XR-094/XR-095CP	Plastic	0°C to +70°C

XR-094/095

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = ±15V, unless otherwise specified.
I_{SET} = 320 μA.

PARAMETERS	XR-094/095			XR-094/095C			UNITS	SYMBOL	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
Input Offset Voltage		3	6 9		5	15 20	mV mV	V_{OS} V_{OS}	R_S = 50Ω, T_A = 25°C R_S = 50Ω, T_A = Full Range
Offset Voltage Temp. Coef.		10			10		μV/°C	$\Delta V_{OS}/\Delta T$	R_S = 50Ω, T_A = Full Range
Input Bias Current		80	600 20		80	800 20	pA nA	I_B	T_A = 25°C T_A = Full Range
Input Offset Current		40	300 10		40	500 5	pA nA	I_{OS}	T_A = 25°C T_A = Full Range
Supply Current (per amplifier)		1.4	2.8		1.4	2.8	mA	I_{CC}	No Load, No Input Signal
Input Common Mode Range	±12			±10			V	V_{ICM}	
Voltage Gain	50 25	200		25 15	200		V/mV	A_{VOL}	R_L ≥ 2KΩ, V_O = ±10V T_A = 25°C T_A = Full Range
Max. Output Swing (peak-to-peak)	24 24	27		24 24	27		V	V_{OPP}	R_L ≥ 10 KΩ T_A = 25°C T_A = Full Range
Input Resistance		10^{12}			10^{12}		Ω	R_{in}	T_A = 25°C
Unity-Gain Bandwidth		3			3		MHz	BW	T_A = 25°C
Common-Mode Rejection	80	86		70	76		dB	CMRR	R_S ≤ 10 KΩ
Supply-Voltage Rejection	80	86		70	76		dB	PSRR	
Channel Separation		120			120		dB		A_V = 100, Freq. = 1 kHz
Slew Rate		13			13		V/μS	dV_{out}/dt	A_V = 1, R_L = 2 KΩ C_L = 100 pF, V_1 = 10V
Rise Time Overshoot		0.1 10			0.1 10		μsec %	t_r t_o	A_V = 1, R_L = 2 KΩ C_L = 100 pF, V_1 = 20 mV
Equivalent Input Noise Voltage		18			18		nV/√Hz	e_n	R_S = 100Ω f = 1 kHz



(One Channel Only)

EQUIVALENT SCHEMATIC DIAGRAM

Quad Programmable Bipolar JFET Operational Amplifier

GENERAL DESCRIPTION

The XR-096 monolithic circuit contains four independently programmable JFET operational amplifiers in a single IC package. Each of the four op amp sections on the chip has its own external bias terminal; thus its performance characteristics and power dissipation can be independently controlled, without effecting the other op amp sections on the chip. The respective bias-setting resisters, R_{SET}, connected to the programming terminals of the circuit allow one to trade-off power dissipation for slew-rate, without sacrificing the gain-bandwidth product of the circuit. These individual bias terminals can also be used to switch the op amp sections "on" and "off", and thus, multiplex between various op amp channels on the same chip.

FEATURES

Programmable Version of XR-084
Independent Programming of All Four Op Amps
Programmable for Micropower Operation
High-Impedance JFET Input Stage
Internal Frequency Compensation
Low Input Bias and Offset Currents

APPLICATIONS

Total Supply Current = 5.6 mA (I_{SET}/320 μA)
Slew-Rate = 13 V/μs (I_{SET}/320 μA)
I_{SET} = Current into set terminal

$$I_{SET} = \frac{V_{CC} - (V_{EE} - 0.6V)}{R_{SET}}$$

Note. I_{SET} must be $\leq$ 400μA

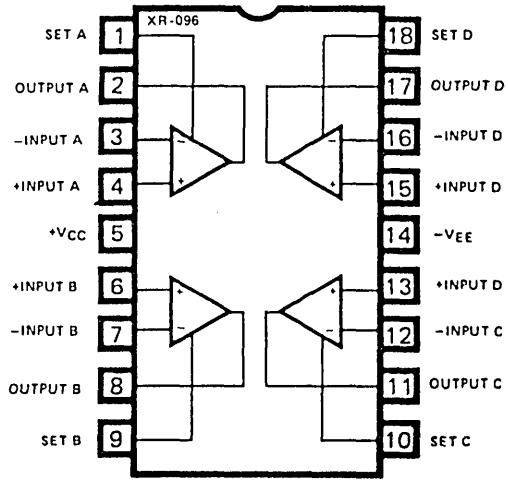
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage Range (Note 1)	±15V
Output Short-Circuit Duration (Note 2)	Indefinite
Package Power Dissipation:	
Plastic Package	625 mW
Derate Above T_A = +25°C	5.0 mV/°C
Ceramic Package	750 mW
Derate Above T_A = +25°C	6.0 mW/°C
Storage Temperature Range	−65°C to +150°C

Note 1: For Supply Voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-096N	Ceramic	−25°C to +85°C
XR-096P	Plastic	−25°C to +85°C
XR-096CN	Ceramic	0°C to +70°C
XR-096CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-096 is a quad independently programmable JFET input operational amplifier featuring extremely high input resistance, low input bias and offset current, large common mode voltage range, and large output swing range. Unity gain bandwidth is 3 MHz, and slew rate is 13V/μS. The devices are unity gain compensated.

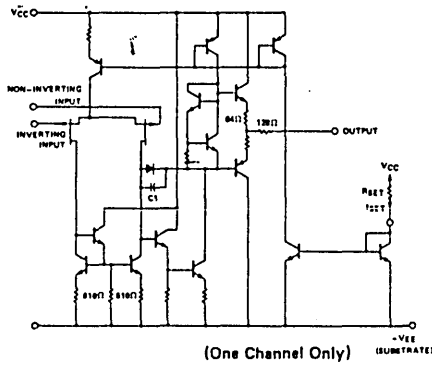
Each of the form amplifiers may be independently "programmed"-rebiased-by connecting a resistor from the bias adjust pin to the positive supply. Bias current may range up to 400 μA, thus affording the designer flexibility along the power consumption/speed curve.

XR-096

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = ±15V, unless otherwise specified.
I_{SET} = 320 μA.

PARAMETERS	XR-096			XR-096C			UNITS	SYMBOL	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
Input Offset Voltage		3	6 9		5	15 20	mV mV	V_{OS} V_{OS}	R_S = 50Ω, T_A = 25°C R_S = 50Ω, T_A = Full Range
Offset Voltage Temp. Coef.		10			10		μV/°C	$\Delta V_{OS}/\Delta T$	R_S = 50Ω, T_A = Full Range
Input Bias Current		80	600 20		80	800 20	pA nA	I_B	T_A = 25°C T_A = Full Range
Input Offset Current		40	300 10		40	500 5	pA nA	I_{OS}	T_A = 25°C T_A = Full Range
Supply Current (per amplifier)		1.4	2.8		1.4	2.8	mA	I_{CC}	No Load, No Input Signal
Input Common Mode Range	±12			±10			V	V_{iCM}	
Voltage Gain	50 25	200		25 15	200		V/mV	A_{VOL}	R_L ≥ 2KΩ, V_O = ±10V T_A = 25°C T_A = Full Range
Max. Output Swing (peak-to-peak)	24 24	27		24 24	27		V	V_{OPP}	R_L ≥ 10 KΩ T_A = 25°C T_A = Full Range
Input Resistance		10^{12}			10^{12}		Ω	R_{in}	T_A = 25°C
Unity-Gain Bandwidth		3			3		MHz	BW	T_A = 25°C
Common-Mode Rejection	80	86		70	76		dB	CMRR	R_S ≤ 10 KΩ
Supply-Voltage Rejection	80	86		70	76		dB	PSRR	
Channel Separation		120			120		dB		A_V 100, Freq. = 1 kHz
Slew Rate		13			13		V/μS	dV_{out}/dt	A_V = 1, R_L = 2 KΩ C_L = 100 pF, V_1 = 10V
Rise Time Overshoot		0.1 10			0.1 10		μsec %	t_r t_o	A_V = 1, R_L = 2 KΩ C_L = 100 pF, V_1 = 20 mV
Equivalent Input Noise Voltage		18			18		nV/√Hz	e_n	R_S = 100Ω f = 1 kHz



(One Channel Only)

EQUIVALENT SCHEMATIC DIAGRAM

Programmable Quad Operational Amplifiers

GENERAL DESCRIPTION

The XR-146 family of quad operational amplifiers contain four independent high-gain, low-power, programmable op-amps on a monolithic chip. The use of external bias setting resistors permit the user to program gain-bandwidth product, supply current, input bias current, input offset current, input noise and the slew rate.

The basic XR-146 family of circuits offer partitioned programming of the internal op-amps where one setting resistor is used to set the bias levels in the three op-amps, and a second bias setting is used for the remaining op-amp. Its modified version, the XR-346-2 provides a separate bias setting resistor for each of the two op-amp pairs.

FEATURES

Programmable
Micropower operation
Low noise
Wide power supply range
Class AB output
Ideal pin out for biquad active filters
Overload protection for input and output
Internal frequency compensation

APPLICATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current $\cong$50 nA (I_{SET}/10 μA)

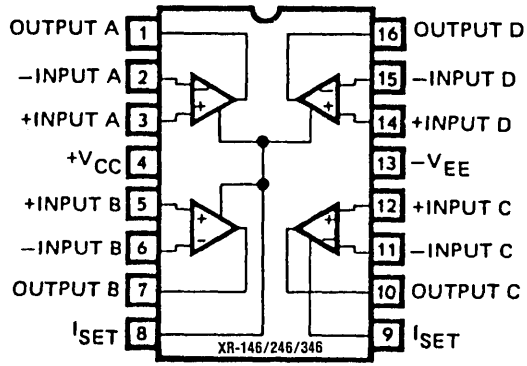
I_{SET} = Current into pin 8, pin 9 (see schematic)

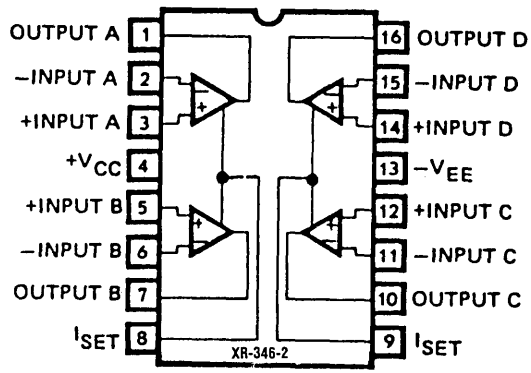
$$I_{SET} = \frac{V+ - V- - 0.6V}{R_{SET}}$$

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-146	±22V
XR-246/346	±18V
Differential Input Voltage (Note 1)	
XR-146/246/346	±30V
Common Mode Input Voltage (Note 1)	
XR-146/246/346	±15V
Power Dissipation (Note 2)	
XR-146	900 mW
XR-246/346	500 mW
Output Short Circuit Duration (Note 3)	
XR-146/246/346	Indefinite
Maximum Junction Temperature	
XR146	150°C
XR-246	110°C
XR-346	100°C

FUNCTIONAL BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS (continued)

Storage Temperature Range	
XR-146/246/346	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-146M	Ceramic	−55°C to +125°C
XR-246N	Ceramic	−25°C to +85°C
XR-246P	Plastic	−25°C to +85°C
XR-346/ 346-2CN	Ceramic	0°C to +70°C
XR-346/ 346-2CP	Plastic	0°C to +70°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_S = ±15V, I_{SET} = 10 μA)

PARAMETERS	XR-146			XR-246/346			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage		0.5	5		0.5	6	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input Offset Current		2	20		2	100	nA	V_{CM} = 0V
Input Bias Current		50	100		50	250	nA	V_{CM} = 0V
Supply Current (4 Op-Amps)		1.4	2.0		1.4	2.5	mA	
Large Signal Voltage Gain	100	1000		50	1000		V/mV	R_L = 10 kΩ, ΔV_{OUT} = ±10V
Input CM Range	±13.5	±14		±13.5	±14		V	
CM Rejection Ratio	80	100		70	100		dB	$R_S \leq$ 10 kΩ
Power Supply Rejection Ratio	80	100		74	100		dB	$R_S \leq$ 10 kΩ
Output Voltage Swing	±12	±14		±12	±14		V	$R_L \leq$ 10 kΩ
Short-Circuit Current	5	20	30	5	20	30	mA	
Gain Bandwidth Product	0.8	1.2		0.5	1.2		MHz	
Phase Margin		60			60		Deg	
Slew Rate		0.4			0.4		V/μs	
Input Noise Voltage		28			28		nV/√Hz	f = 1 kHz
Channel Separation		120			120		dB	R_L = 10 kΩ, ΔV_{OUT} = 0V to +12V
Input Resistance		1.0			1.0		MΩ	
Input Capacitance		2.0			2.0		pF	

The following specifications apply over the Maximum Operating Temperature Range

Input Offset Voltage		0.5	6		0.5	7.5	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input Offset Current		2	25		2	100	nA	V_{CM} = 0V
Input Bias Current		50	100		50	250	nA	V_{CM} = 0V
Supply Current (4 Op-Amps)		1.5	2.0		1.5	2.5	mA	
Large Signal Voltage Gain	50	1000		25	1000		V/mV	R_L = 10 kΩ, ΔV_{OUT} = ±10V
Input CM Range	±13.5	±14		±13.5	±14		V	
CM Rejection Ratio	70	100		70	100		dB	$R_S \leq 50\Omega$
Power Supply Rejection Ratio	76	100		74	100		dB	$R_S \leq 50\Omega$
Output Voltage Swing	±12	±14		±12	±14		V	$R_L \geq$ 10 kΩ

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V, I_{SET} = 1 μA)

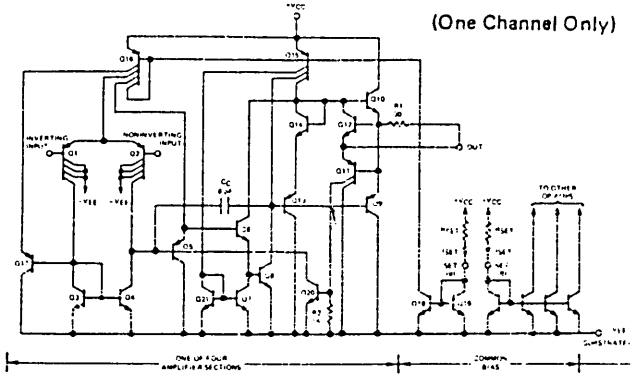
Input Offset Voltage		0.5	5		0.5	6	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input Bias Current		7.5	20		7.5	100	nA	V_{CM} = 0V
Supply Current (4 Op-Amps)		140	250		140	300	μA	
Gain Bandwidth Product	80	100		50	100		kHz	

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_S = ±1.5V, I_{SET} = 10 μA)

Input Offset Voltage		0.5	5		0.5	7	mV	V_{CM} = 0V, $R_S \leq 50\Omega$
Input CM Range	±0.7			±0.7			V	
CM Rejection Ratio		80			80		dB	$R_S \leq 50\Omega$
Output Voltage Swing	±0.6			±0.6			V	$R_L \geq$ 10 kΩ

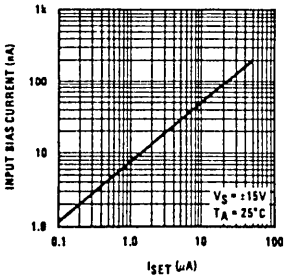
EQUIVALENT SCHEMATIC DIAGRAM

(One Channel Only)

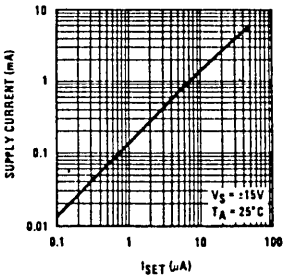


TYPICAL PERFORMANCE CHARACTERISTICS

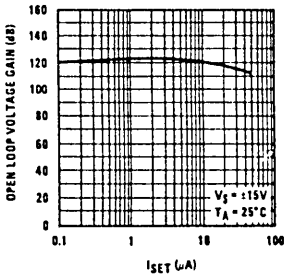
Input Bias Current vs I_{SET}



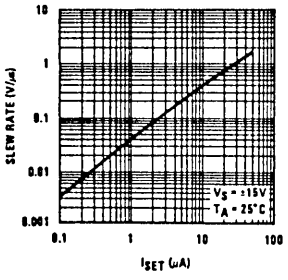
Supply Current vs I_{SET}



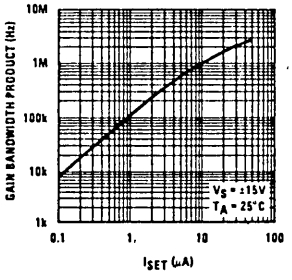
Open Loop Voltage Gain vs I_{SET}



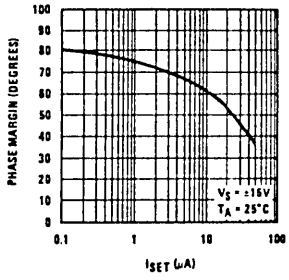
Slew Rate vs I_{SET}



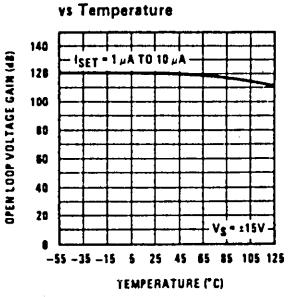
Gain Bandwidth Product vs I_{SET}



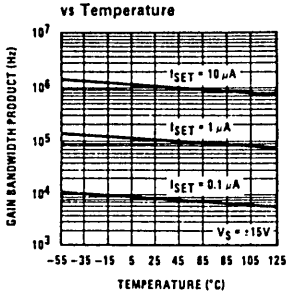
Phase Margin vs I_{SET}



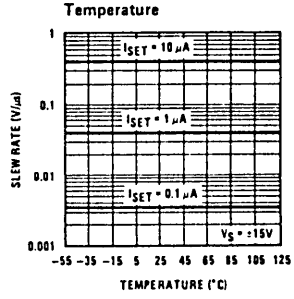
Open Loop Voltage Gain vs Temperature



Gain Bandwidth Product vs Temperature

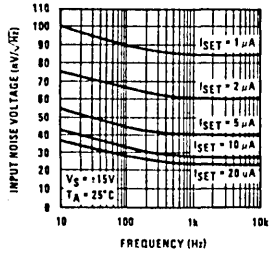


Slew Rate vs Temperature

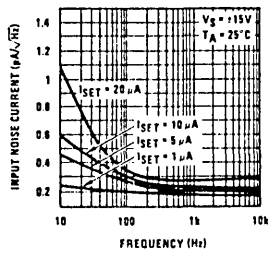


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

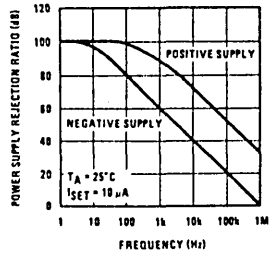
Input Noise Voltage vs Frequency



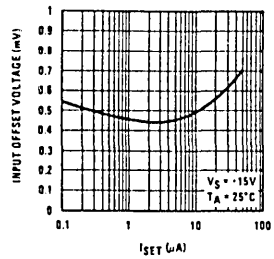
Input Noise Current vs Frequency



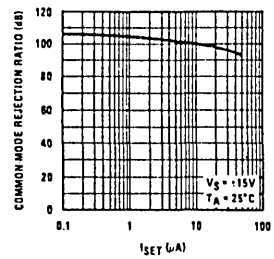
Power Supply Rejection Ratio vs Frequency



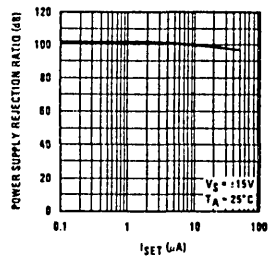
Input Offset Voltage vs I_{SET}



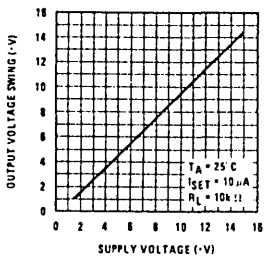
Common-Mode Rejection Ratio vs I_{SET}



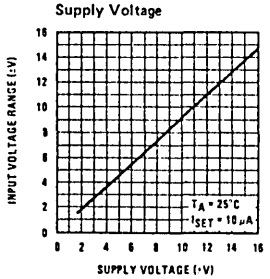
Power Supply Rejection Ratio vs I_{SET}



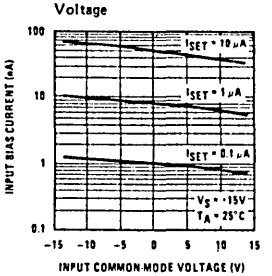
Output Voltage Swing vs Supply Voltage



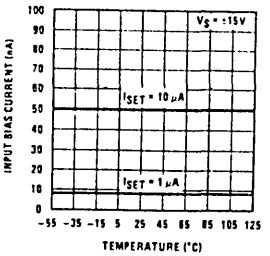
Input Voltage Range vs Supply Voltage



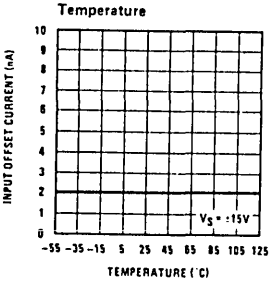
Input Bias Current vs Input Common-Mode Voltage



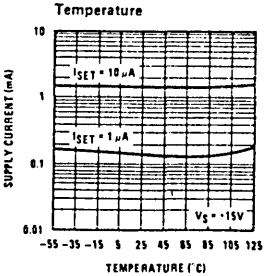
Input Bias Current vs Temperature



Input Offset Current vs Temperature



Supply Current vs Temperature



Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θjA, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta jA$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should be simultaneously shorted as the maximum junction temperature will be exceeded.

Dual Operational Amplifier

GENERAL DESCRIPTION

The XR-1458/4558 is a pair of independent internally compensated operational amplifiers on a single silicon chip, each similar to the popular 741, but with a power consumption less than one 741. Good thermal tracking and matched gain-bandwidth products make these Dual Op-amps useful for active filter applications.

FEATURES

Direct Pin-for-Pin Replacement for MC1458, RC4558, N5558
Low Power Consumption — 50 mW typ. and 120mW max.
Short-Circuit Protection
Internal Frequency Compensation
No Latch-Up
Wide Common-Mode and Differential Voltage Ranges
Matched Gain-Bandwidth

APPLICATIONS

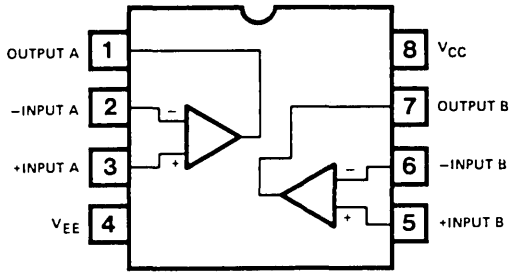
Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-4558CP	±18V
Input Voltage (Note 1)	±15V
Common Mode Voltage Range	V_{EE} to V_{CC}
Output Short-Circuit Duration (Note 2)	indefinite
Differential Input Voltage	±30V
Internal Power Dissipation (Note 3)	
Plastic Package:	500 mW
Storage Temperature Range:	−65°C to +150°C
Operating Temperature Range:	0°C to +70°C

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 2: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature of +75°C ambient temperature for XR1458/4558.
Note 3: Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C for XR1458/4558.

FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1458CN	Ceramic	0°C to +70°C
XR-1458CP	Plastic	0°C to +70°C
XR-4558CN	Ceramic	0°C to +70°C
XR-4558CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-1458 and XR-4558 are dual general purpose op amps featuring better performance than industry standard devices such as the 741; bandwidth, slew rate, and input resistance are greatly improved. Internal protection circuitry includes latch-up elimination, short circuit current limiting, and internal compensation.

The two amplifiers are completely independent, sharing bias circuitry only.

XR-1458/4558

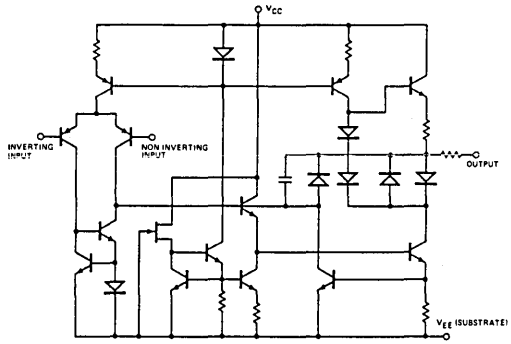
ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = +25°C, ±15V, unless otherwise specified.

PARAMETERS	XR1458/4558CP MIN	TYP	MAX	UNITS	SYMBOLS	CONDITIONS
Input Offset Voltage		0.5	6.0	mV	$\|V_{io}\|$	$R_S \leq 10$ KΩ
Input Offset Current		5	200	nA	$\|I_{io}\|$	
Input Bias Current		40	500	nA	$\|I_b\|$	
Input Resistance	0.3	5		MΩ	R_{in}	
Large Signal Voltage Gain	20	300		V/mV	A_{VOL}	$R_L \geq 2$ KΩ V_{out} = ±10V
Output Voltage Swing	±12 ±10	±14 ±13		V V	V_{out} V_{out}	$R_L \geq 10$ KΩ $R_L \geq 2$ KΩ
Input Voltage Range	±12	±14		V	V_{iCM}	
Common Mode Rejection Ratio	70	90		dB	CMRR	$R_S \leq 10$ KΩ
Supply Voltage Rejection Ratio		30	150	μV/V	PSRR	$R_S \leq 10$ KΩ
Power Consumption		50	170	mW	P_i	
Transient Response (unity gain) Risetime Overshoot		 0.13 5		 μs %	 t_r t_o	V_{in} = 20 mV R_L = 2 KΩ $C_L \leq 100$ pF
Unity Gain Bandwidth		3.0		MHz	BW	
Slew Rate (unity gain)		1.0		V/μs	dV_{out}/dt	$R_L \geq 2$ KΩ
Channel Separation (open loop)		120		dB		f = 10 kHz R_S = 1 KΩ
(Gain of 100)		105		dB		f = 10 kHz R_S = 1 KΩ

The following specifications apply for 0°C ≤ T_A ≤ +70°C for XR4558CP

Input Offset Voltage			7.5	mV	$\|V_{io}\|$	$R_S \leq 10$ kΩ
Input Offset Current			300	nA	$\|I_{io}\|$	
Input Bias Current			800	nA	I_b	
Large-Signal Voltage Gain	15			V/mV	A_{VOL}	$R_S \geq 2$ KΩ V_{out} = ±10V
Output Voltage Swing	±10			mV	V_{out}	$R_L \geq 2$ KΩ
Power Consumption		 90 120	 150 200	 mW mW	 P_i P_i	V_S = ±15V T_A = High T_A = Low



EQUIVALENT SCHEMATIC DIAGRAM

Quad Operational Amplifiers

GENERAL DESCRIPTION

The XR-3403 and XR-3503 are quad operational amplifiers specifically designed for single supply operation. All four amplifiers are similar in characteristics to industry standard op amps like the 741. The XR-3403 is available in both ceramic and plastic packages; the XR-3503 is available in a 14 pin ceramic package with guaranteed performances across the military temperature range.

FEATURES

Short Circuit Protected Outputs
Class AB Output Stage for Minimal Crossover Distortion
True Differential Input Stage
Single Supply Operation: 3.0 to 36 Volts
Split Supply Operation: ±1.5 to ± 18 Volts
Low Input Bias Currents: 500 nA Max
Four Amplifiers per Package
Internally Compensated
Similar Performance to Popular 741
Direct Pin-for-Pin Replacement for MC3403/3503, LM324 and RC4137

APPLICATIONS

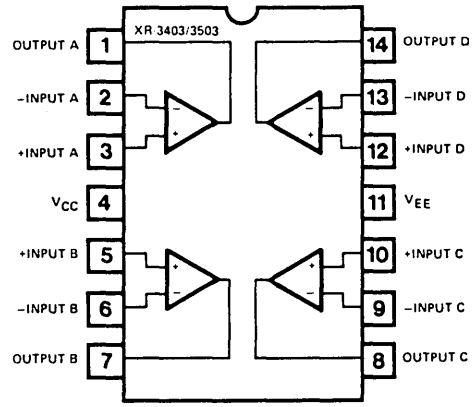
Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages	
Single Supply	36V
Split Supplies	±18V
Input Differential Voltage Range with Split Power Supply	±30V
Input Common Mode Voltage Range*	±15V
Package Power Dissipation:	
Plastic Package	625 mW
Derate above T_A = +25°C	5.0 mV/°C
Ceramic Package	750 mW
Derate above T_A = +25°C	6.0 mW/°C
Storage Temperature Range	−65°C to +150°C

*For Supply Voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3503M	Ceramic	−55°C to +125°C
XR-3403CN	Ceramic	0°C to +70°C
XR-3403CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-3403 is an array of four independent operational amplifiers, each with true differential inputs. The device has electrical characteristics similar to the popular 741. However, the XR-3403 has several distinct advantages over standard operational amplifier types in single supply applications. The XR-3403 can operate at supply voltages as low as 3.0 volts or as high as 36 volts with quiescent currents about one-fifty of those associated with the 741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

XR-3403/3503

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +15V, V_{EE} = 15V, T_A = +25°C unless otherwise noted.

PARAMETERS	XR-3503M			XR-3403C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage		2.0	5.0 6.0		2.0	10 12	mV	$T_A = T_{high}$ to T_{low}[1]
Input Offset Current		30	50 200		30	50 200	nA	$T_A = T_{high}$ to T_{low}
Large Signal Open-Loop Voltage Gain	 50 25	 200 300		 20 15	 200		V/mV	$V_O = \pm 10V$ R_L = 2.0 KΩ $T_A = T_{high}$ to T_{low}
Input Bias Current		−200 −300	−500 −1500		−200	−500 −800	nA	$T_A = T_{high}$ to T_{low}
Output Impedance		75			75		Ω	f = 20 Hz
Input Impedance	0.3	1.0		0.3	1.0		MΩ	f = 20Hz
Output Voltage Swing	±12 ±10 ±10	±13.5 ±13		±12 ±10 ±10	±13.5 ±13		V	R_L = 10 KΩ R_L = 2.0 KΩ R_L = 2.0 KΩ $T_A = T_{high}$ to T_{low}
Input Common Mode Voltage Range	+13V-V_{EE}	+13.5V-V_{EE}		+13V-V_{EE}	+13.5V-V_{EE}		V	
Common Mode Rejection Ratio	70	90		70	90		dB	R_S < 10 KΩ
Power Supply Current (V_O = 0)		2.8	4.0		2.8	7.0	mA	$R_L = \infty$
Individual Output Short-Circuit Current[2]	±20	±30	±45	±10	±20	±45	mA	
Positive Power Supply Rejection Ratio		30	150		30	150	μV/V	
Negative Power Supply Rejection Ratio		30	150		30	150	μV/V	
Average Temperature Coefficient of Input Offset Current		50			50		pA/°C	$T_A = T_{high}$ to T_{low}
Average Temperature Coefficient of Input Offset Voltage		10			10		μV/°C	$T_A = T_{high}$ to T_{low}
Power Bandwidth		9.0			9.0		kHz	A_V = 1, R_L = 2.0 KΩ V_o = 20V (p-p) THD = 5%
Small Signal Bandwidth		1.0			1.0		MHz	A_V = 1, R_L = 10 KΩ V_o = 50 mV
Slew Rate		0.6			0.6		V/μs	A_V = 1, V_i = −10V to +10V
Rise Time		0.6			0.6		μs	A_V = 1, R_L = 10 KΩ V_o = 50 mV
Fall Time		0.6			0.6		μs	A_V = 1, R_L = 10 KΩ V_o = 50 mV
Overshoot		20			20		%	A_V = 1, R_L = 10 KΩ V_o = 50 mV
Phase Margin		60			60		Degrees	A_V = 1, R_L = 2.0 KΩ C_L = 200 pF
Crossover Distortion		1.0			1.0		%	(V_{in} = 30 mV p-p V_{out} = 2.0V p-p F = 10 kHz)

[1] T_{high} = +125°C for XR-3503M, +70°C for XR-3403C
T_{low} = −55°C for XR-3503M, 0°C for XR-3403C

[2] Not to exceed maximum package power dissipation.
[3] Output will swing to ground.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V, V_{EE} = Gnd, T_A = +25°C, unless otherwise noted.

PARAMETERS	XR-3503M			XR-3403C				CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	
Input Offset Voltage		2.0	5.0		2.0	10	mV	
Input Offset Current		30	50		30	50	nA	
Input Bias Current		−200	−500		−200	−500	nA	
Large Signal Open Loop Voltage Gain	20	200		20	200		V/mV	R_L = 2.0 KΩ
Power Supply Rejection Ratio			150			150	μV/V	
Output Voltage Range[3]	3.5 V_{CC} − 1.5V			3.5 V_{CC} − 1.5V			Vp-p	R_L = 10 KΩ V_{CC} = 5.0V R_L = 10 KΩ 5.0V ≤ V_{CC} ≤ 30V
Power Supply Current		2.5	4.0		2.5	7.0	mA	
Channel Separation		−120			−120		dB	f = 1.0 kHz to 20 kHz (Input Referenced)

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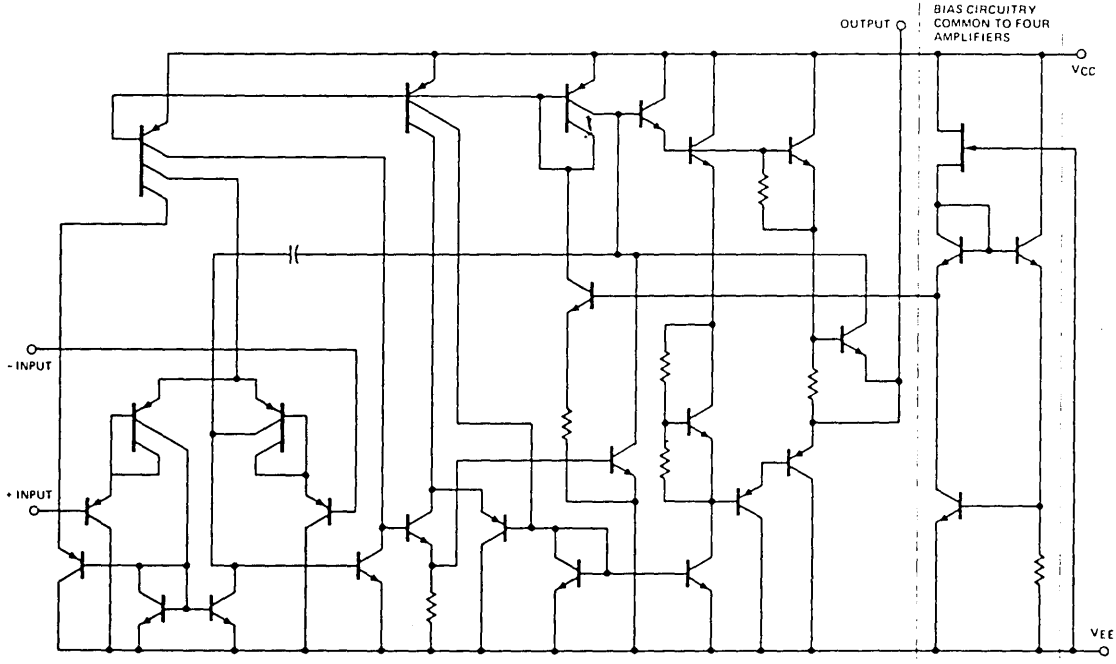


EQUIVALENT SCHEMATIC DIAGRAM

Quad Operational Amplifier

GENERAL DESCRIPTION

The XR-4136 is an array of four independent internally compensated operational amplifiers on a single silicon chip, each similar to the popular 741. Good thermal tracking and matched gain-bandwidth products make these Quad Op-amps useful for active filter applications.

FEATURES

Direct Pin-for-Pin Replacement for RC4136 and RM4136
Short-Circuit Protection
Internal Frequency Compensation
No Latch-Up
Wide Common-Mode and Differential Voltage Ranges
Matched Gain-Bandwidth

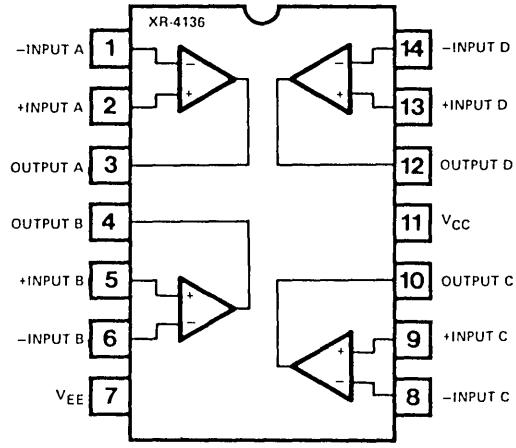
APPLICATIONS

Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-4136M	±22V
XR-4136C	±18V
Common Mode Voltage Range	V_{EE} to V_{CC}
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	±30V
Internal Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range:	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4136M	Ceramic	−55°C to +125°C
XR-4136CN	Ceramic	0°C to +70°C
XR-4136CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-4136 is a quad operational amplifier featuring similar characteristics to standard 741-type devices. As all four are monolithic, they have matched characteristics, including thermal tracking and gain bandwidth products.

ELECTRICAL CHARACTERISTICS

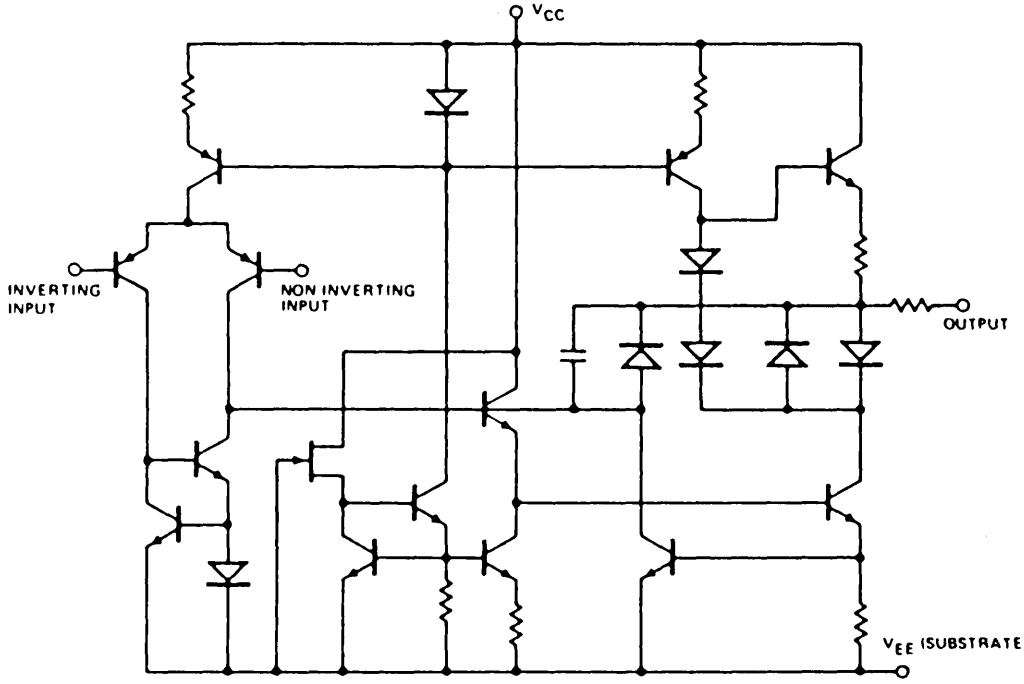
Test Conditions: $T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETERS	XR4136M MIN	XR4136M TYP	XR4136M MAX	XR4136C MIN	XR4136C TYP	XR4136C MAX	UNITS	SYMBOLS	CONDITIONS
Input Offset Voltage		.5	5.0		.5	6.0	mV	$\|V_{io}\|$	$R_S \leq 10$ KΩ
Input Offset Current		5.0	200		5.0	200	nA	$\|I_{io}\|$	
Input Bias Current		40	500		40	500	nA	$\|I_b\|$	
Input Resistance	0.3	5.0		0.3	5.0		MΩ	R_{in}	
Large Signal Voltage Gain	50	300		20	300		V/mV	A_{VOL}	$R_L \geq 2$ KΩ $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		±12	±14		V	V_{out}	$R_L \geq 10$ KΩ
	±10	±13		±10	±13		V	V_{out}	$R_L \geq 2$ KΩ
Input Voltage range	±12	±14.0		±12	±14.0		V	V_{iCM}	
Common Mode Rejection Ratio	70	105		70	105		dB	CMRR	$R_S \leq 10$ KΩ
Supply Voltage Rejection Ratio		10	150		10	150	μV/V	PSRR	$R_S \leq 10$ KΩ
Power Consumption		210	340		210	340	mW	P_i	
Transient Response (unity gain) Risetime Overshoot		 .13 5.0			 .13 5.0		 μs %	 t_r t_o	$V_{in} = 20$ mV $R_L = 2$ KΩ $C_L \leq 100$ pF
Unity Gain Bandwidth	2.0	3.0			3.0		MHz	BW	
Slew Rate (unity gain)		1.5			1		V/μs	dV_{out}/dt	$R_L \geq 2$ KΩ
Channel Separation (open loop)		105			105		dB		f = 10 KHz $R_S = 1$ KΩ
(Gain of 100)		105			105		dB		f = 10 KHz $R_S = 1$ KΩ
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for XR-4136M: $0°C \leq T_A \leq +70°C$ for XR-4136C									
Input Offset Voltage			6.0			7.5	mV	$\|V_{io}\|$	$R_S \leq 10$ KΩ
Input Offset Current			500			300	nA	$\|I_{io}\|$	
Input Bias Current			1500			800	nA	I_b	
Large-Signal Voltage Gain	25			15			V/mV	A_{VOL}	$R_L \geq 2$ KΩ $V_{out} = \pm 10V$
Output Voltage Swing	±10			±10			V	V_{out}	$R_L \geq 2$ KΩ
Power Consumption		180 240	300 400		100 240	300 400	mW mW	P_i P_i	$V_S = \pm 15V$ T_A = High T_A = Low
Output Short-Circuit Current		45			45		mA	I_{SC}	

TYPICAL PARAMETER MATCHING:

Test Conditions: $T_A = +25°C$, $V_S = \pm 15V$ unless otherwise noted

PARAMETERS	XR4136M TYP	XR4136C TYP	UNITS	SYMBOLS	CONDITIONS
Input Offset Voltage	±1.0	±2.0	mV	$\|V_{io}\|$	$R_S \geq 10$ KΩ
Input Offset Current	±7.5	±7.5	nA	$\|I_{io}\|$	
Input Bias Current	±15	±15	nA	I_b	
Voltage Gain	±0.5	±1.0	dB	A_{VOL}	$R_S \geq 2$ KΩ



1/4 of XR-4136

EQUIVALENT SCHEMATIC DIAGRAM

Programmable Quad Operational Amplifier

GENERAL DESCRIPTION

The XR-4202 is an array of four independent operational amplifiers on a single silicon chip. The operating current of the array is externally controlled by a single resistor or current source, allowing the user to trade-off power dissipation for bandwidth.

FEATURES

Programmable
Micropower Operation
Wide Input Voltage and Common Mode Range
Internal Frequency Compensation
No Latch-Up
Matched Parameters
Short-Circuit Protection

APPLICATIONS

The following approximate relations are useful for design:

Gain-Bandwidth Product	≈	50 I_{SET}	(kHz)
Power Supply Current	≈	30 I_{SET}	(μA)
Slew Rate	≈	20 I_{SET}	(V/ms)

Where: I_{SET} is in μA

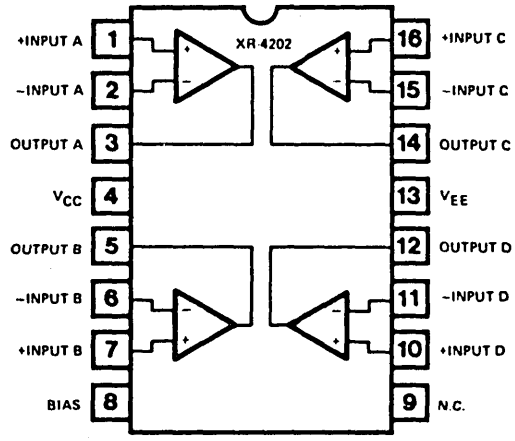
$$I_{SET} = \frac{V_{EE} - V_{BE}}{R_{SET}}$$

WHERE V_{BE} DIODE VOLTAGE ≈ 0.65V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±30V
Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Common Mode Range	V_{EE} to V_{CC}
Short Circuit Duration	Indefinite
Storage Temperature	−60°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4202N	Ceramic	−40°C to +85°C
XR-4202P	Plastic	−40°C to +85°C

SYSTEM DESCRIPTION

The XR-4202 is a quad independently programmable operational amplifier featuring improved performance over industry standard devices such as the 741. Amplifier bias currents can be "programmed" by a single resistor to Pin 8. Bias currents can range from less than 1μA, thus affording the designer flexibility along the device speed/power consumption trade off curve.

ELECTRICAL CHARACTERISTICS

Test Conditions: High Power Mode (V_S = ±15V, I_{SET} = 75 μA and T_A = +25°C, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Short Circuit Current	5	17	30	mA	I_{SC}	0°C≤ T_A≤70°C
Supply Current	0.8	1.7	6.0	mA	I_S	Note 3
Input Offset Voltage		0.8	5.0	mV	V_{io}	R_S≤10 KΩ
Input Bias Current		80	500	nA	I_b	
Input Off-set Current		10	200	nA	I_{io}	
Input Resistance	0.1	0.6		MΩ	R_{in}	
Input Common Mode Voltage Range	12	±14		±V	V_{iCM}	
Common Mode Rejection Ratio	70	110		dB	CMRR	
Voltage Supply Rejection Ratio		15	150	μV/V	PSRR	
Large Signal Voltage Gain	74	88		dB	A_{VOL}	R_L = 3 KΩ; ΔV_O = ±10 V
Output Voltage Swing	±10	±13.6		±V	V_{out}	R_L = 3 KΩ
Gain-Bandwidth Product		3.5		MHz	f_1	
Phase Margin		45		Deg.		
Rise Time		70		ns	t_R	ΔV_O = ±20 mV
Overshoot		20		%	t_o	ΔV_O = ±20 mV
Channel Separation		120 105		dB dB		Any amp. pair: freq. = 1 Hz, R_L = 3 K Ω Any amp. pair: freq. = 10 KHz, R_L = 3 K Ω
Slew Rate		1.5		V/μs	dV_{out}/dt	
Input Voltage Noise		25		nV/√Hz	e_n	Bandwidth 100 Hz to 10 KHz

Note: Short circuit may be taken to either supply line or ground on only one amplifier at a time.

ELECTRICAL CHARACTERISTICS

Test Conditions: High Power Mode (V_S = ±15V, I_{SET} = 75 μA and T_A = −55°C to +125°C)

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Input Offset Voltage		0.8	10	mV	V_{io}	R_S ≤10 KΩ
Input Bias Current		80	1500	nA	I_b	
Input Offset Current		10	200	nA	I_{io}	
Large Signal Voltage Gain	68	88		dB	A_{vol}	R_L 3 KΩ ΔV_O = ±10 V

ELECTRICAL CHARACTERISTICS

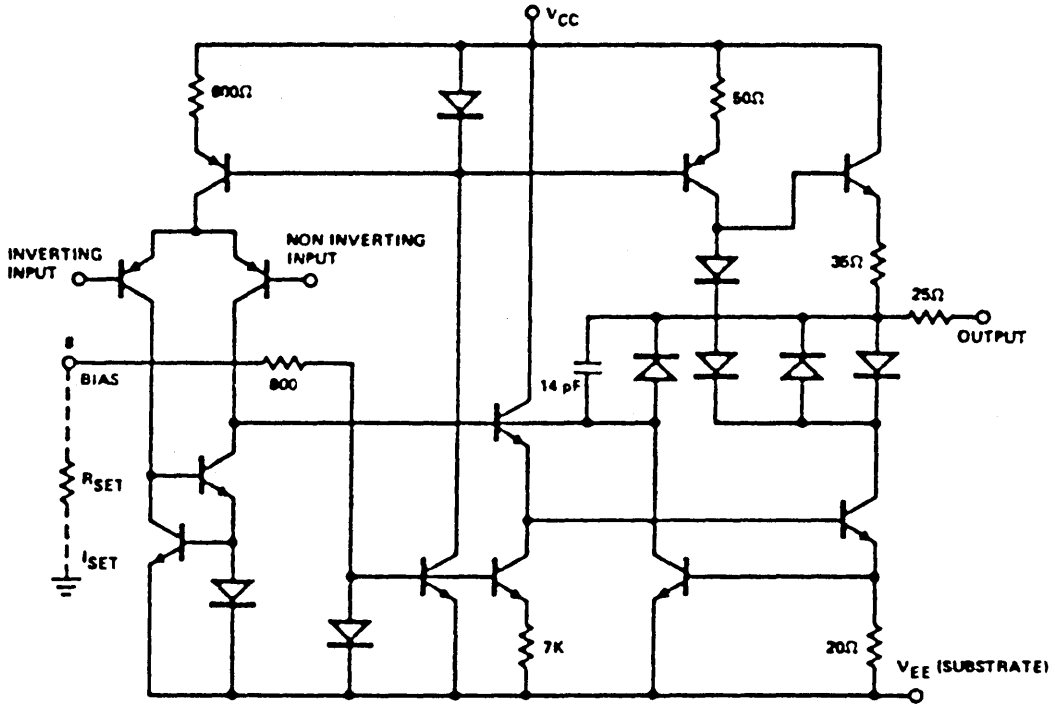
Test Conditions: Micropower Mode (I_{SET} = 1 μA, V_S = ±1.5V)

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Supply Current			100	μA	I_S	Note 3
Input Bias Current			200	nA	I_B	
Input Offset Current			20	nA	I_{OS}	
Input Offset Voltage		0.5	5	mV	V_{os}	$R_S \leq$ 10 KΩ
Input Resistance	0.5			MΩ	R_{in}	
Input Common Mode Voltage Range	0.3	±0.8		±V	V_{iCM}	
Common Mode Rejection Ratio	60	100		dB	CMRR	
Voltage Supply Rejection Ratio		20	200	μV/V	PSRR	
Large Signal Voltage Gain	66	80		dB	A_{vol}	$R_L \geq$ 100 KΩ
Gain-Bandwidth Product		50		kHz	GBW	
Phase Margin		75		Deg.		
Slew-Rate		20		V/ms	dV_{out}/dt	
Rise Time		7		μs	t_R	ΔV_O = ±20 mV
Overshoot		0		%	t_o	ΔV_O = ±20 mV
Channel Separation		120 120		dB dB		Freq. = Hz: R_L = 20 KΩ, ΔV_O = ±0.5 V Freq. = 1 KHz: R_L = 10 KΩ, ΔV_O = ±0.5V
Equivalent Input Voltage Noise		200		nV√Hz	e_n	Bandwidth = 100 Hz to 10 KHz

PARAMETER MATCHING (I_{SET} = 75 μA (2))

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Input Offset Voltage		1		±mV	V_{os}	$R_S \leq$ 10 KΩ
Input Bias Current		10		±nA	I_B	
Input Offset Current		2		±nA	I_{os}	
Gain-Bandwidth Product		100		±KHz	f_1	
Slew Rate		0.2		±V/μs	dV_o/dt	

NOTES: 1. All tests refer to a single op amp unless otherwise specified.
2. Tests apply for parameter matching between any op amp pair.
3. Tests apply to four op amps and bias network.



EQUIVALENT SCHEMATIC DIAGRAM

Quad Operational Amplifier

GENERAL DESCRIPTION

The XR-4212 is an array of four independent internally compensated operational amplifiers on a single silicon chip, each similar to the popular 741, but with a power consumption less than one 741. Good thermal tracking and matched gain-bandwidth products make these Quad Op-amps useful for active filter applications.

FEATURES

Same Pinout as MC3403 and LM324
Low Power Consumption—50 mW typ. and 120mW max.
Short-Circuit Protection
Internal Frequency Compensation
No Latch-Up
Wide Common-Mode and Differential Voltage Ranges
Matched Gain-Bandwidth

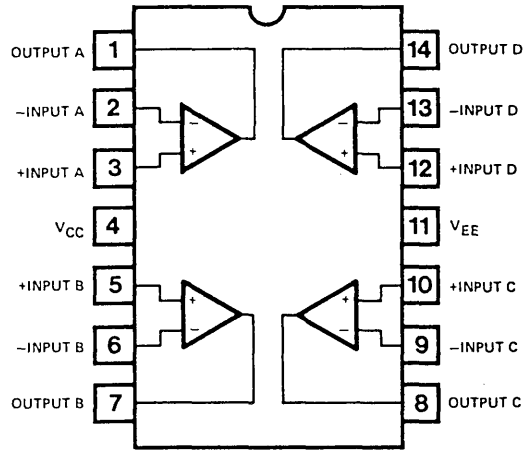
APPLICATIONS

Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-4212M	±22V
XR-4212C	±18V
Common Mode Voltage	V_{EE} to V_{CC}
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	±30V
Internal Power Dissipation	
Ceramic Package:	750 mW
Derate above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range:	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4212M	Ceramic	−55°C to +125°C
XR-4212CN	Ceramic	0°C to +70°C
XR-4212CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-4212 is a quad operational amplifier featuring improved performance over industry standard devices such as the 741.

XR-4212

ELECTRICAL CHARACTERISTICS

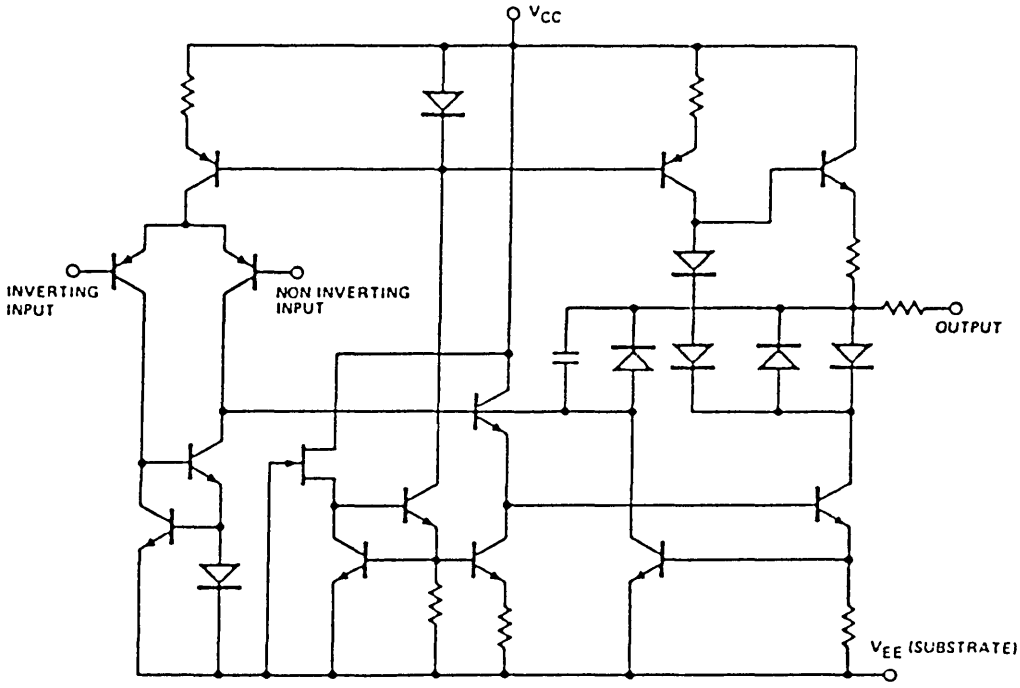
Test Conditions: $T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETERS	XR-4212M			XR-4212C			UNITS	SYMBOLS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
Input Offset Voltage		1	5.0		1	6.0	mV	$\|V_{io}\|$	$R_S \leq 10$ KΩ
Input Offset Current		10	50		10	50	nA	$\|I_{io}\|$	
Input Bias Current		80	500		80	500	nA	$\|I_b\|$	
Input Resistance	0.3	1.8		0.3	1.8		MΩ	R_{in}	
Large Signal Voltage Gain	20	60		5	40		V/mV	A_{VOL}	$R_L \geq 2$ KΩ $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		±12	±14		V	V_{out}	$R_L \geq 10$ KΩ
	±10	±12		±10	±12		V	V_{out}	$R_L \geq 2$ KΩ
Input Voltage Range	±12	±13.5		±12	±13.5		V	V_{iCM}	
Common Mode Rejection Ratio	70	105		70	105		dB	CMRR	$R_S \leq 10$ KΩ
Supply Voltage Rejection Ratio		10	150		10	150	μV/V	PSRR	$R_S \leq 10$ KΩ
Power Consumption		50	120		50	120	mW	P_i	
Transient Response (unity gain) Risetime Overshoot		 0.07 20			 0.07 20		 μs %	 t_r t_o	$V_{in} = 20$ mV $R_L = 2$ KΩ $C_L \leq 100$ pF
Unity Gain Bandwidth	2.0	3.0			3.0		MHz	BW	
Slew Rate (unity gain)		1.6			1.6		V/μs	dV_{out}/dt	$R_L \geq 2$ KΩ
Channel Separation (open loop)		120			120		dB		f = 10 KHz $R_S = 1$ KΩ
(Gain of 100)		105			105		dB		f = 10 KHz $R_S = 1$ KΩ
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for XR-4212M: $0°C \leq T_A \leq +70°C$ for XR-4212C									
Input Offset Voltage			6.0			7.5	mV	$\|V_{io}\|$	$R_S \leq 10$ KΩ
Input Offset Current			200			200	nA	$\|I_{io}\|$	
Input Bias Current			1500			800	nA	I_b	
Large-Signal Voltage Gain	20			5			V/mV	A_{VOL}	$R_L \geq 2$ KΩ $V_{out} = \pm 10V$
Output Voltage Swing	±10			±10			V	V_{out}	$R_L \geq 2$ KΩ
Power Consumption			150 200			150 200	mW mW	P_i P_i	$V_S = \pm 15$ V T_A = High T_A = Low
Output Short-Circuit Current	5	17	35	5	17	35	mA	I_{SC}	

TYPICAL PARAMETER MATCHING:

Test Conditions: $T_A = +25°C$, $V_S = \pm 15V$ unless otherwise noted

PARAMETERS	XR-4212M TYP	XR-4212C TYP	UNITS	SYMBOLS	CONDITIONS
Input Offset Voltage	±1.0	±2.0	mV	$\|V_{io}\|$	$R_S \geq 10$ KΩ
Input Offset Current	±7.5	±7.5	nA	$\|I_{io}\|$	
Input Bias Current	±15	±15	nA	I_b	
Voltage Gain	±0.5	±1.0	dB	A_{VOL}	$R_S \geq 2$ KΩ



1/4 of XR-4212

EQUIVALENT SCHEMATIC DIAGRAM

Dual Low Noise Operational Amplifier

GENERAL DESCRIPTION

The XR-4560 is a dual low noise, wide bandwidth operational amplifier ideal for active filter applications. The device is similar to the XR-1458/4558, with greatly enhanced slew rate, bandwidth, and guaranteed noise characteristics.

Pin for pin compatibility allows direct substitution for industry standard dual op amps where the low noise and wide bandwidth of the XR-4560 is imperative.

FEATURES

High Gain, Low Input Noise
Internally Compensated
Wide Small Signal Bandwidth
Interchangeable with General Purpose Dual Op Amps

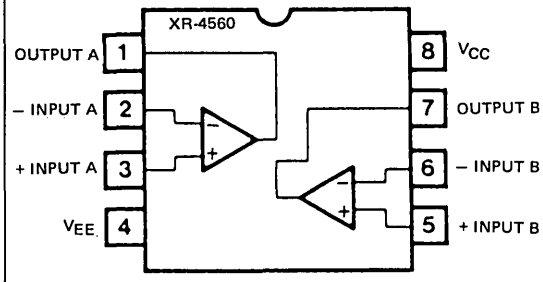
APPLICATIONS

High Gain, Low Noise Amplifier
High Performance Active Filter
Small Signal Amplifier
Servo Control System
Telephone Channel Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Power Dissipation	500 mW
Derate Above at 25°C	5 mW/°C
Operating Temperature	0°C to +70°C
Storage Temperature	-55°C to +125°C
Differential Input Voltage	±30 V
Common Mode Range	V_{EE} to V_{CC}

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4560CP	Plastic	0°C to 70°C
XR-4560CN	Ceramic	0°C to 70°C
XR-4560MD	SO-8	0°C to 70°C

SYSTEM DESCRIPTION

The XR-4560 dual op amp offers guaranteed low noise and a 10 MHz small signal bandwidth. Slew rate typically exceeds 4 V/μS. Internal protection circuitry includes latch-up elimination, short circuit current limiting, and internal compensation.

The two amplifiers are completely independent, sharing only power supply connections.

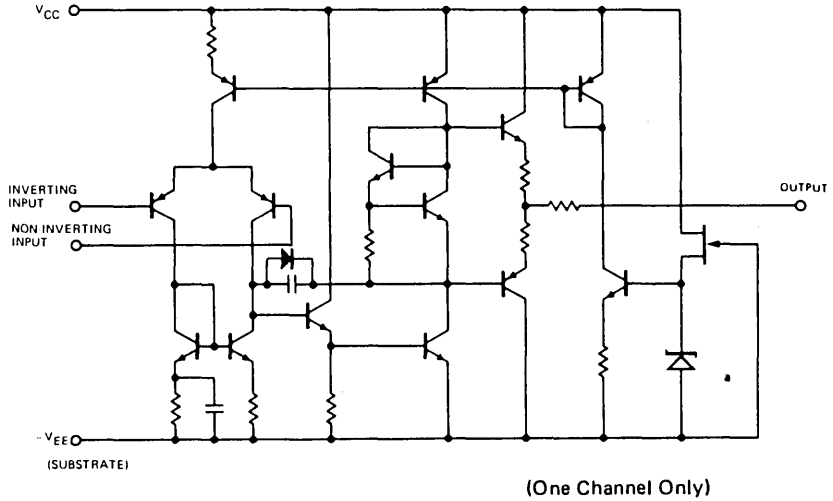
ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{CC} = +15$ V, $V_{EE} = -15$ V, unless specified otherwise.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
V_{OS}	Input Offset Voltage		0.5	6.0	mV	$R_S \leq 10K\Omega$
I_{OS}	Input Offset Current		5	200	nA	
I_B	Input Bias Current		50	500	nA	
R_{in}	Input Resistance		5		MΩ	
A_V	Open Loop Gain	86	100		dB	$R_L \geq 2K\Omega$
	Output Voltage Swing	±12 ±10	±14 ±13		V V	$R_L \geq 10K\Omega$ $R_L \geq 2K\Omega$
V_{ICM}	Common Mode Range	±12	±14		V	
CMRR	Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10K\Omega$
PSRR	Supply Voltage Rejection Ratio		30	150	μV/V	$R_S \leq 10K\Omega$
S_R	Slew Rate		4.0		V/μs	$A_V = 1$, $R_L \geq 2K\Omega$
BW	Unity Gain Bandwidth		10		MHz	$A_V = 1$
P_i	Power Consumption		50		mW	$R_L = \infty$
	Channel Separation		100		dB	$A_V = 100$
e_n	Input Noise Voltage			2.2	μV	f = 10 Hz to 30 kHz Circuit of Figure 7

5

EQUIVALENT SCHEMATIC DIAGRAM



(One Channel Only)

TYPICAL CHARACTERISTICS

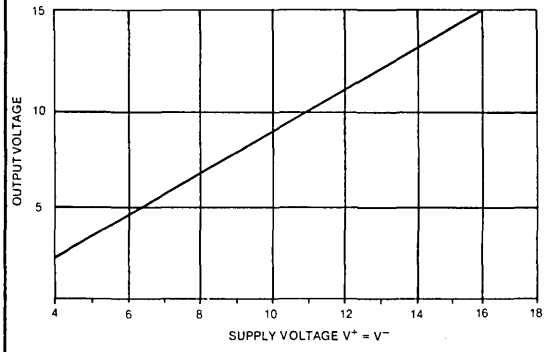


Figure 1. Output Voltage Swing vs Supply Voltage

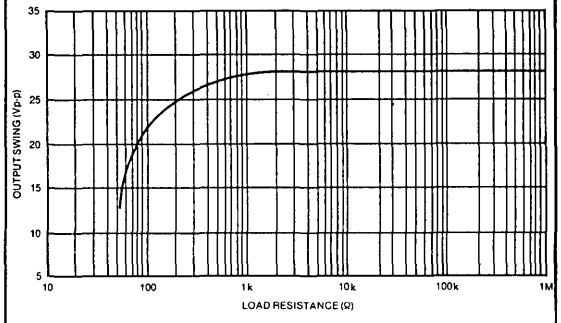


Figure 2. Loaded Output Voltage Swing

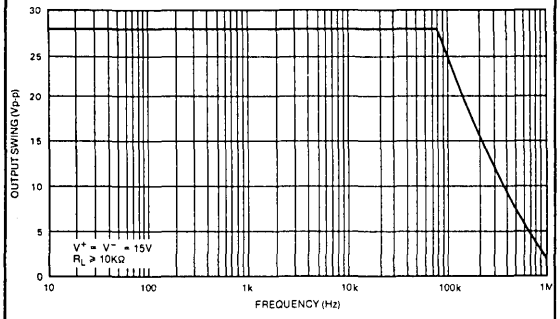


Figure 3. Large Signal Frequency Response

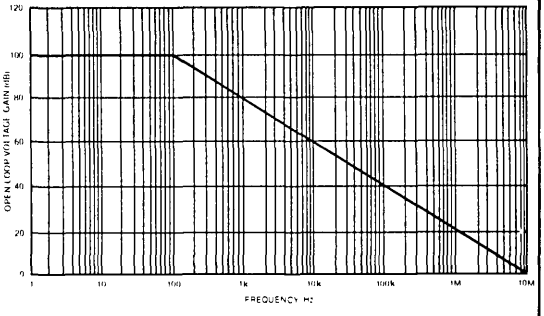


Figure 4. Open Loop Gain

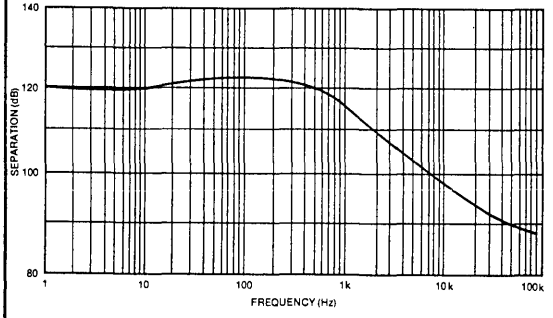


Figure 5. Channel Separation vs Frequency

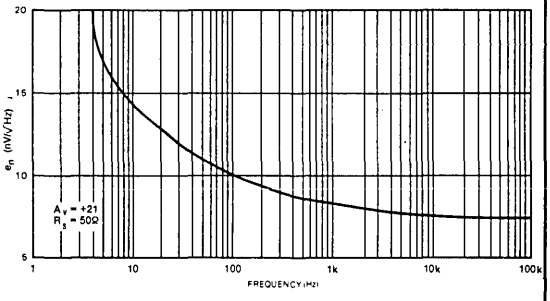


Figure 6. Input Noise Voltage Spectral Density

Noise measurements made on a Quantek 2173-2181 noise analyzer with the XR-4560 in a standard noninverting circuit with A_V = 21.

TYPICAL APPLICATIONS

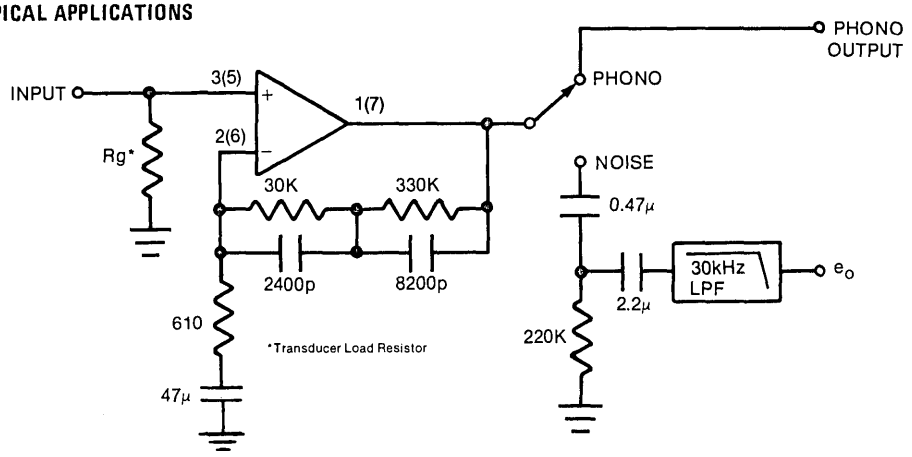


Figure 7. RIAA Equalized Phonograph Preamplifier (One Channel) & Broadcast Noise Test Circuit

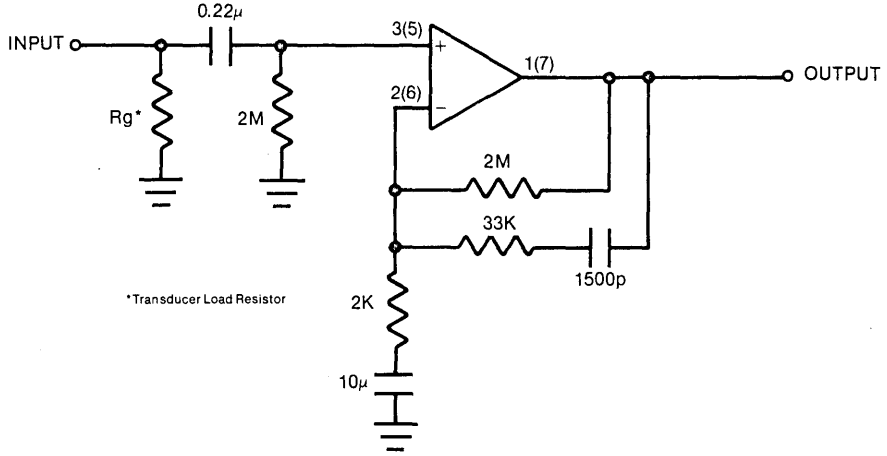


Figure 8. NAB Equalized Tape Playback Preamplifier (One Channel)

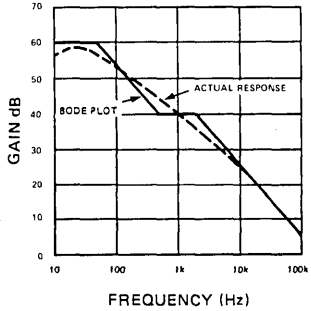


Figure 9. RIAA-Type Phonograph Equalization

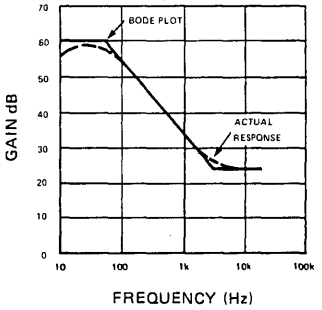


Figure 10. NAB-Type Tape Player Equalization

Dual Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The XR-4739 is a monolithic dual op amp featuring low noise and a large gain bandwidth product. The device is ideal for preamplifiers, signal processing equipment, and active filters.

FEATURES

Internally Compensated Replacement for μA 739 and MC1303
Signal-to-Noise Ratio 76dB (RIAA 10 mV ref.)
Channel Separation 125dB
Unity Gain Bandwidth 3MHz
Output Short-circuit Protected
0.1% Distortion at 8.5V RMS Output into 2KΩ Load

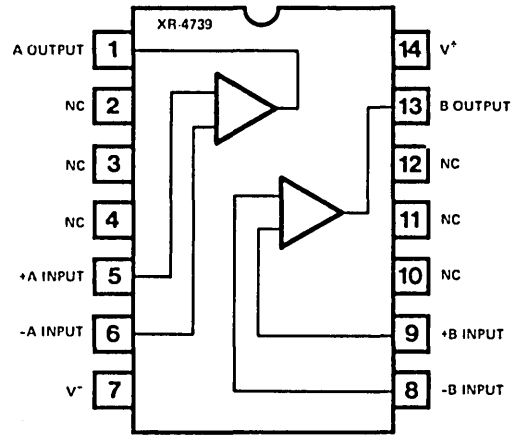
APPLICATIONS

Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60s)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4739CN	Ceramic	0°C to +70°C
XR-4739CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-4739 dual low-noise operational amplifier is fabricated on a single silicon chip using the planar epitaxial process. It was designed primarily for preamplifiers in consumer and industrial signal processing equipment. The device is pin compatible with the μA739 and MC1303, however, compensation is internal. This permits a lowered external parts count and simplified application.

The XR-4739 is available in a ceramic or molded dual inline 14 Pin package, and operates over the commercial temperature range from 0°C to +70°C.

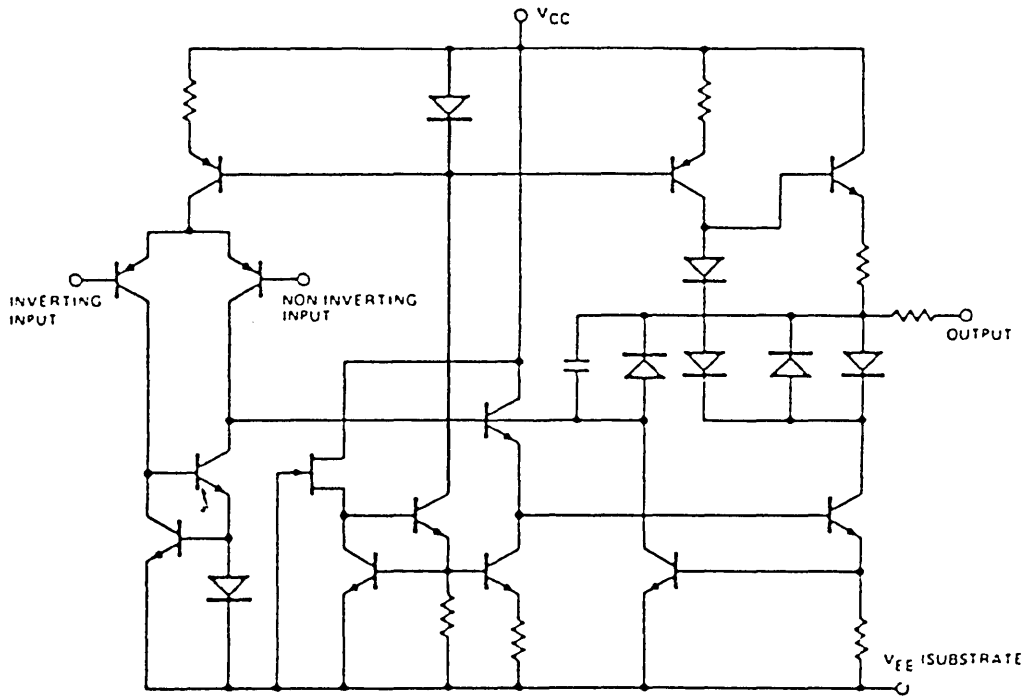
ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = ±15V, unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
Input Offset Voltage		2.0	6.0	mV	$R_S \leq 10$ kΩ
Input Offset Current		5.0	200	nA	
Input Bias Current		40	500	nA	
Input Resistance	0.3	5.0		MΩ	
Large-Signal Voltage Gain	20	60		K	$R_L \geq 2$ kΩ V_{out} = ±10V
Output Voltage Swing	±12 ±10	±14 ±13		V V	$R_L \geq 10$ kΩ $R_L \geq 2$ kΩ
Input Voltage Range	±12	±14		V	
Common Mode Rejection Ratio	70	100		dB	$R_S \leq 10$ kΩ
Supply Voltage Rejection Ratio		10	150	μV/V	$R_S \leq 10$ kΩ
Power Consumption		40	120	mW	
Transient Response (unity gain) Risetime		0.15		μs	V_{in} = 20 mV R_L = 20 kΩ $C_L \leq 100$ pF
Transient Response (unity gain) Overshoot		10		%	V_{in} = 20 mV R_L = 2 kΩ $C_L \leq 100$ pF
Slew Rate (unity gain)		1.0		V/μs	$R_L \geq 2$ kΩ
Broadband Noise Voltage		2.5		μV_{RMS}	B_W = 10 Hz-30 KHz R_S = 1 kΩ
Channel Separation		125		dB	f = 1.0 kHz A_V = 40 dB R_S = 1 kΩ
The following specifications apply for 0°C ≤ T_A ≤ 75°C unless otherwise specified.					
Input Offset Voltage		3.0	7.5	mV	$R_S \leq 10$ kΩ
Input Offset Current		7.0	300	nA	
Input Bias Current		50	800	nA	
Large-Signal Voltage Gain	15,000	200,000			$R_L \geq 2$ kΩ V_{out} = ±10V
Output Voltage Swing	±10	±13		V	$R_L \geq 2$ kΩ
Power Consumption		100 110	150 200	mW mW	V_S = ±15V T_A = 70°C T_A = 0°C

Notes:

1. Rating applies for ambient temperatures below +75°C
2. For supply voltages less than 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be ground, typically 45 mA. Rating applies to +125°C ambient temperature.



EQUIVALENT SCHEMATIC DIAGRAM

½ of XR-4739

Quad Operational Amplifier

GENERAL DESCRIPTION

The XR-4741 is an array of four independent internally-compensated operational amplifiers on a single silicon chip, each similar to the popular 741. Each amplifier offers performance equal to or better than the 741 type in all respects. It has high slew rate, superior bandwidth, and low noise, which makes it excellent for audio amplifiers or active filter applications.

FEATURES

Short-Circuit Protection
Internal Frequency Compensation
No Latch-Up
Wide Common-Mode and Differential Voltage Ranges
Matched Gain-Bandwidth

High Slew Rate	1.6V/μS(Typ)
Unity Gain-Bandwidth	3.5 MHz(Typ)
Low Noise Voltage	9 nV$\sqrt{Hz}$
Input Offset Current	60 nA(Typ)
Input Offset Voltage	.5 mV(Typ)
Supply Range	±2V to ±20V

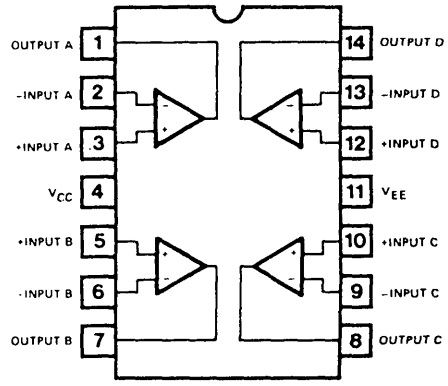
APPLICATIONS

Buffer Amplifiers
Summing/Differencing Amplifiers
Instrumentation Amplifiers
Active Filters
Signal Processing
Sample and Differencing
I to V Converters
Integrators
Simulated Components
Analog Computers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
XR-4741	±20
Common Mode	
Voltage	V_{EE} to V_{CC}
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	±30V
Internal Power Dissipation	
Ceramic Package:	880 mW
Derate above T_A = +25°C	5.8 mW/°C
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range:	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4741M	Ceramic	−55°C to +125°C
XR-4741CN	Ceramic	0°C to +70°C
XR-4741CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

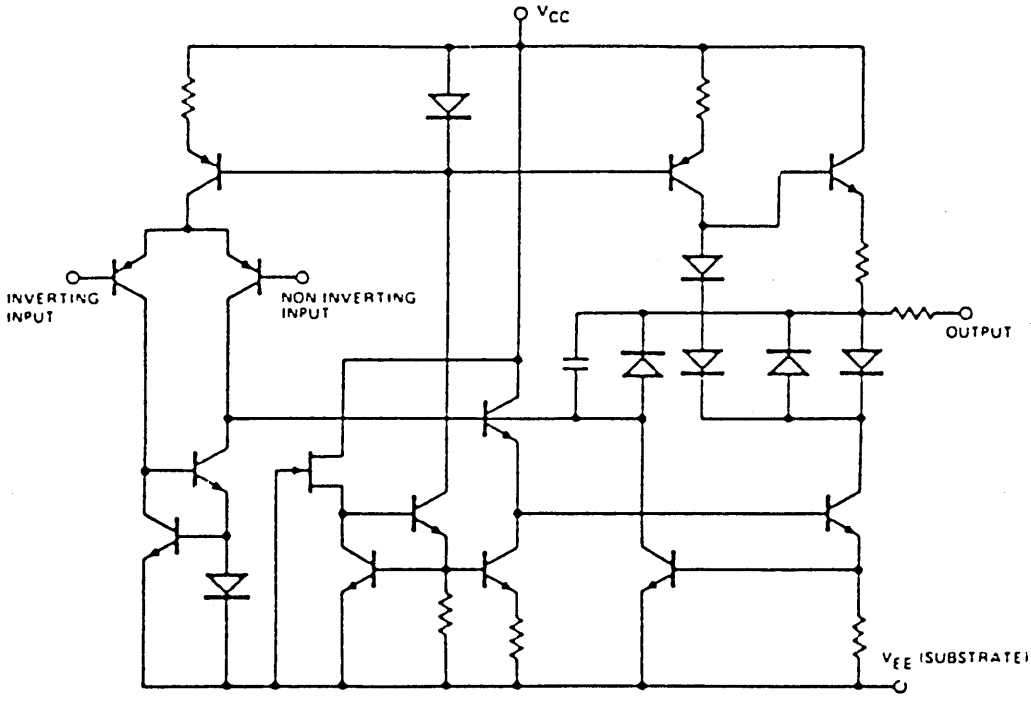
The XR-4741 is a quad independently programmable operational amplifier featuring improved performance over industry standard devices such as the 741. Amplifier bias currents can be "programmed" by a single resistor to Pin 8. Bias currents can range from less than 1 μA to over 75 μA, thus affording the designer flexibility along the device speed/power consumption trade off curve.

XR-4741

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = +25°C, V_S = ±15 V unless otherwise specified.

PARAMETERS	XR-4741M			XR-4741C			UNITS	SYMBOLS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
Input Offset Voltage		0.5	3.0		1.0	5.0	mV	$\|V_{io}\|$	$R_S \leq 10$ KΩ
Input Offset Current		10	30		10	50	nA	$\|I_{io}\|$	
Input Bias Current		60	200		60	300	nA	$\|I_b\|$	
Differential Input Resistance		5			5		MΩ	R_{in}	
Input Noise Voltage (f = 1 kHz)		9			9		nV/√Hz		
Large Signal Voltage Gain	50	100		25	50		V/mV	A_{VOL}	$R_L \geq 2$ KΩ $V_{out} = \pm 10$V
Output Voltage Swing	±12 ±10	±13.7 ±12.5		±12 ±10	±13.7 ±12.5		V V	V_{out} V_{out}	$R_L \geq 10$ KΩ $R_L \geq 2$ KΩ
Full Power Bandwidth		25			25		kHz		
Output Resistance		300			300		Ω		
Input Voltage Range	±12	±13.5		±12	±13.5		V	V_{iCM}	
Common Mode Rejection Ratio	80	100		80	100		dB	CMRR	$R_S \leq 10$ KΩ
Supply Voltage Rejection Ratio		10	100		10	100	μV/V	PSRR	$R_S \leq 10$ KΩ
Power Consumption			150			210	mW	P_i	
Transient Response (unity gain)									$V_{in} = 20$ mV $R_L = 2$ KΩ
Risetime		.07			.07		μs	t_r	$C_L \leq 100$ pF
Overshoot		20			20		%	t_o	
Unit Gain Bandwidth		3.5			3.5		MHz	BW	
Slew Rate (unity gain)		1.6			1.6		V/μs	dV_{out}/dt	$R_L \geq 2$ KΩ
Channel Separation (open loop)		120			120		dB		f = 10 KHz $R_S = 1$ KΩ
(Gain of 100)		105			105		dB		f = 10 KHz $R_S = 1$ KΩ
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for XR-4741M; $0°C \leq T_A \leq +70°C$ for XR-4741C									
Input Offset Voltage		4.0	5.0		5.0	6.5	mV	$\|V_{io}\|$	$R_S \leq 10$ KΩ
Input Offset Current			75			100	nA	$\|I_{io}\|$	
Input Bias Current			325			400	nA	I_b	
Input Voltage Range	±12			±12			V		
Common Mode Rejection Ratio	74			74			db		
Large-Signal Voltage Gain	25			15			V/mV	A_{VOL}	$R_L \geq 2$ KΩ $V_{out} = \pm 10$V
Output Voltage Swing	±10	±12.5		±10	±12.5		V	V_{out}	$R_L = 2$ KΩ
	±12.0	±13.7		±12	±13.7				$R_L \geq 10$ KΩ $V_S = \pm 15$V
Power Consumption			150			150	mW	P_i	T_A = High
			200			200	mW	P_i	T_A = Low
Supply Voltage Rejection Ratio		100	μV/V		100	μV/V			
Output Short-Circuit Current	±5	±15		±5	±15		mA	I_{SC}	



1/4 of XR-4741

EQUIVALENT SCHEMATIC DIAGRAM

Dual Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The XR-5532 dual low-noise operational amplifier is especially designed for applications in high quality professional audio equipment. The low-noise, wide bandwidth and output drive capability make it ideally suited for instrumentation and control circuits as well as active filter design.

The XR-5532A is the specially screened version of the XR-5532, with guaranteed noise characteristics.

FEATURES

Pin for Pin Replacement for Signetics NE 5532
Wide Small-Signal Bandwidth: 10 MHz
High-Current Drive Capability
(10V rms into 600Ω at VS = ±18V)
High Slew Rate: 9 V/μs 140
Wind Power-Bandwidth: 140 kHz
Very Low Input Noise: 5 nV/√Hz
Wide Supply Range: ±3V to ±20V

APPLICATIONS

High Quality Audio Amplification
Telephone Channel Amplifier
Servo Control Systems
Low-Level Signal Detection
Active Filter Design

ABSOLUTE MAXIMUM RATINGS

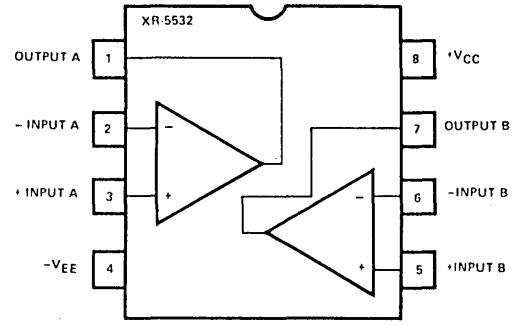
Power Supply	±22V
Input Common-Mode Range	$-V_{EE}$ to $+V_{CC}$
Differential Input Voltage (Note 1)	±0.5V
Power Dissipation (Package Limitation)	
Ceramic Package 8-Pin	600 mW
Derate Above TA = 25°C	8 mW/°C
Storage Temperature	−60°C to +150°C

Note 1: Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10 mA.

Note 2: Output may be shorted to ground at $V_{CC} = V_{EE} =$ 15V, $T_A = 25°C$. Temperature and/or voltages must be limited to ensure dissipation rating is not exceeded.

Note 3: Operation near the absolute maximum ratings will exceed the power dissipation of the package.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5532N	Ceramic	0°C to +70°C
XR-5532P	Plastic	0°C to +70°C
XR-5532AN	Ceramic	0°C to +70°C
XR-5532AP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-5532 and XR-5532A are dual monolithic operational amplifiers featuring low noise and very large gain bandwidth products. The devices have low output resistance and can drive 10 Vrms into 600Ω. Input noise is 100% tested on the XR-5532A, and is typically only 5 nV/√Hz. The small signal bandwidth is 10 MHz and slew rate exceeds 9 V/μS. Supply voltage may range from ± 3V to ± 18V.

XR-5532/5532A

ELECTRICAL CHARACTERISTICS

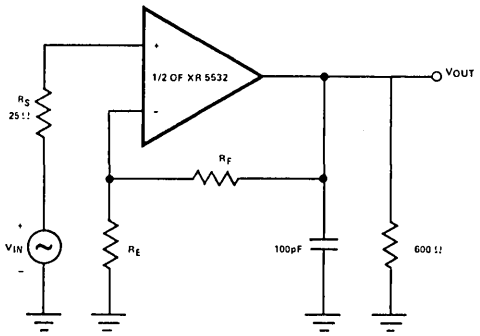
Test Conditions: T_A = 25°C, V_{CC} = V_{EE} = 15V unless otherwise specified.

PARAMETERS	XR-5532A			XR-5532			UNITS	SYMBOL	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
DC CHARACTERISTICS									
Input Offset Voltage		0.5	4 5		0.5	4 5	mV mV	V_{OS}	T_A = 25°C T_A = Full Range
Input Offset Current		10	150 200		10	150 200	nA nA	I_{OS}	T_A = 25°C T_A = Full Range
Input Bias Current		200	800 1000		200	800 1000	nA nA	I_B	T_A = 25°C T_A = Full Range
Large Signal Voltage Gain	25 15	100		25 15	100		V/mV V/mV	A_{VOL}	$R_L \geq 600\Omega$, V_O = ±10V T_A = 25°C T_A = Full Range
Supply Current		8	16		8	16	mA	I_{CC}	R_L = Open
Output Swing	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V	V_{OUT}	$R_L \geq 600\Omega$ V_{CC} = V_{EE} = 15V V_{CC} = V_{EE} = 18V
Output Short Circuit Current		38			38		mA	I_{SC}	(Note 2)
Input Resistance	30	300		30	300		kΩ	R_{IN}	
Common-Mode Range	±12	±13		±12	±13		V	V_{iCM}	
Common-Mode Rejection	70	100		70	100		dB	CMRR	
Power Supply Rejection		10	100		10	100	μV/V	PSRR	
Channel Separation		110			110			dB	f = 1 kHz, R_S = 5 KΩ
AC CHARACTERISTICS									
Transient Response Rise Time Overshoot		 20 10			 20 10		 nsec %	 t_r t_0	Voltage Follower R_L = 600Ω V_{IN} 100 MV_{pp}, C_L = 100 pF
AC Gain		2.2			2.2		V/mV		f = 10 kHz
Unity-Gain Bandwidth		10			10		MHz	BW	C_L = 100 pF
Slew Rate		9			9		V/μsec		
Power Bandwidth		140			140		kHz	f_p	V_{OUT} = ±10V RL = 600Ω
Output Resistance		.3			.3		Ω	R_{OUT}	A_V = 30 dB Closed loop f = 10 kHz R_L = 600Ω
NOISE CHARACTERISTICS									
Input Noise Voltage		8 5	10 6		8 5		nV/√Hz nV/√Hz	e_n	f_0 = 30 kHz f_0 = 1 kHz
Input Noise Current		2.7 .7			2.7 .7		pA/√Hz pA/√Hz	i_n	f_0 = 30 Hz f_0 = 1 kHz

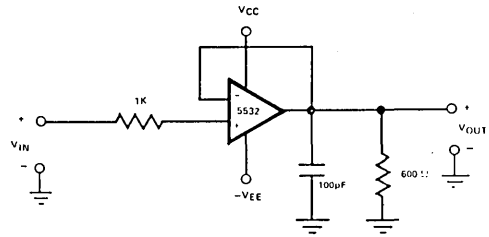
5

TEST CIRCUITS

CLOSED LOOP FREQUENCY RESPONSE

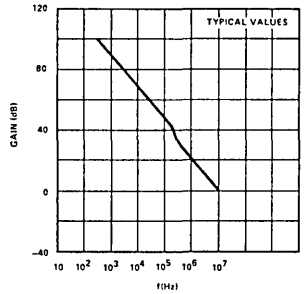


VOLTAGE FOLLOWER

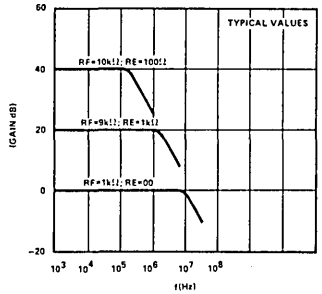


TYPICAL PERFORMANCE CHARACTERISTICS

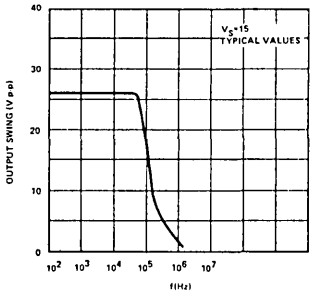
OPEN LOOP FREQUENCY RESPONSE



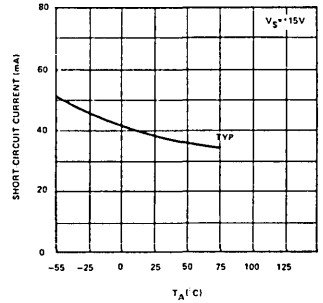
CLOSED LOOP FREQUENCY RESPONSE



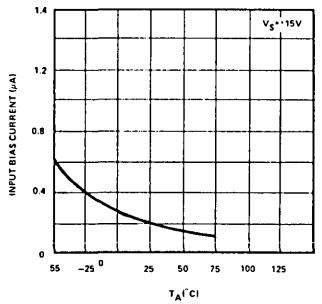
LARGE-SIGNAL FREQUENCY RESPONSE



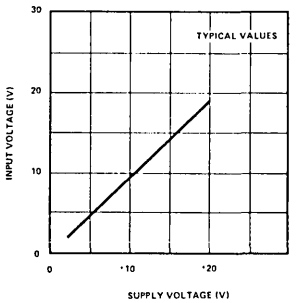
OUTPUT SHORT-CIRCUIT CURRENT



INPUT BIAS CURRENT

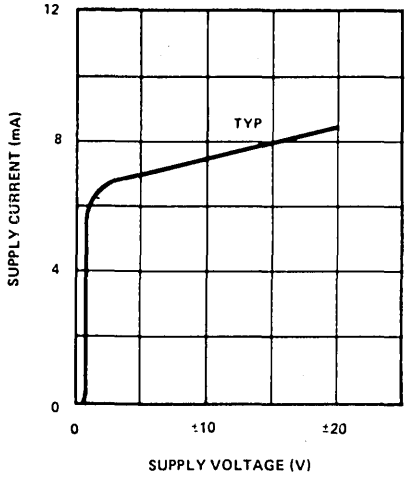


INPUT COMMON MODE VOLTAGE RANGE

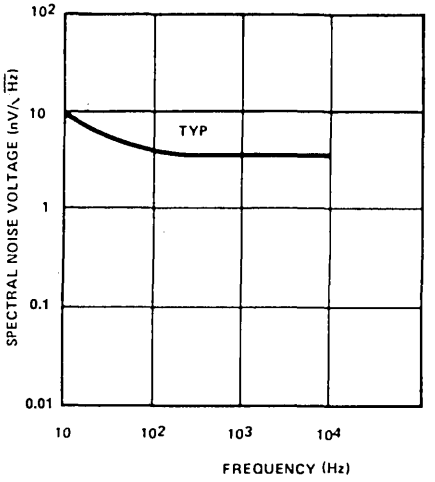


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SUPPLY CURRENT



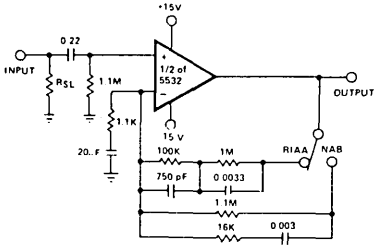
INPUT NOISE VOLTAGE DENSITY



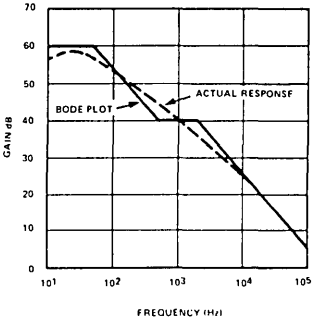
5

TYPICAL APPLICATION

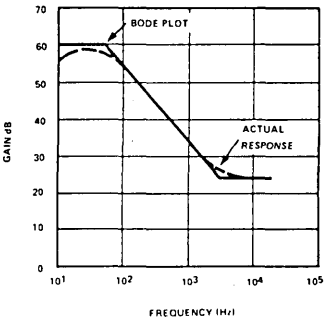
PREAMPLIFIER–RIAA/NAB COMPENSATION



*SELECT TO PROVIDE SPECIFIED TRANSDUCER LOADING
OUTPUT NOISE 0.8 mV rms (WITH INPUT SHORTED)
ALL RESISTOR VALUES ARE IN OHMS

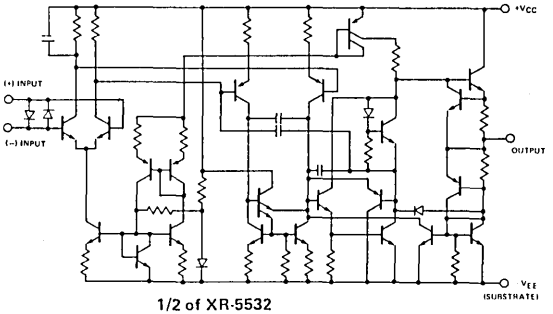


BODE PLOT OF RIAA EQUALIZATION AND THE RESPONSE REALIZED IN AN ACTUAL CIRCUIT USING THE XR 5533



BODE PLOT OF NAB EQUALIZATION AND THE RESPONSE REALIZED IN THE ACTUAL CIRCUIT USING THE XR 5533.

EQUIVALENT SCHEMATIC DIAGRAM



1/2 of XR-5532

Dual Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The XR-5533 dual low-noise operational amplifier is especially designed for applications in high quality professional audio equipment. The low-noise, wide bandwidth and output drive capability make it ideally suited for instrumentation and control circuits as well as active filter design.

The XR-5533A is the specially screened version of the XR-5533 with guaranteed worst-case noise specifications.

FEATURES

Direct Replacement for Signetics SE/NE 5533
Wide Small-Signal Bandwidth: 10 MHz
High-Current Drive Capability
(10V rms into 600Ω at $V_S = \pm 18V$)
High Slew Rate: 13 V/μs
Wide Power-Bandwidth: 200 kHz
Very Low Input Noise: 4 nV/√Hz

APPLICATIONS

High Quality Audio Amplification
Telephone Channel Amplifier
Servo control Systems
Low-Level Signal Detection
Active Filter Design

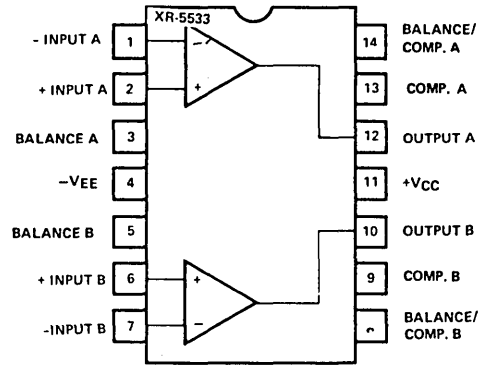
ABSOLUTE MAXIMUM RATINGS

Power Supply	±22V
Input Common-Mode Range	$-V_{EE}$ to $+V_{CC}$
Differential Input Voltage (Note 1)	±0.5V
Short Circuit Duration (Note 2)	Indefinite
Power Dissipation (Package Limitation)	
Ceramic Package 14-Pin	750 mW
Plastic Package 14-Pin	600 mW
Derate Above $T_A = 25°C$	5 mW/°C
Storage Temperature	−60°C to +150°C

Note 1: Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10 mA.

Note 2: Output may be shorted to ground at $V_{CC} = V_{EE} = 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-5533AN	Ceramic	0°C to +70°C
XR-5533AP	Plastic	0°C to +70°C
XR-5533N	Ceramic	0°C to +70°C
XR-5533P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-5533 and XR-5533A are dual monolithic operational amplifiers featuring low noise and very large gain bandwidth products. The devices have low output resistance and can drive 10 Vrms into 600Ω. Input noise is 100% tested on the XR-5533A, and is typically only 4 nV/√Hz. The small signal bandwidth is 10 MHz and slew rate exceeds 13 V/μS.

XR-5533/5533A

ELECTRICAL CHARACTERISTICS

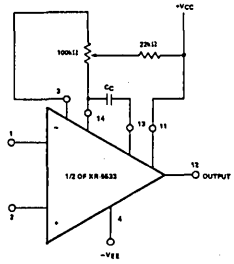
Test Conditions: T_A = 25°C, V_{CC} = V_{EE} = 15V unless otherwise specified.

PARAMETERS	XR-5533A			XR-5533			UNITS	SYMBOL	CONDITIONS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
DC CHARACTERISTICS									
Input Offset Voltage		0.5	4 5		0.5	4 5	mV mV	V_{OS}	T_A = 25°C T_A = Full Range
Input Offset Current		20	300 400		20	300 400	nA nA	I_{OS}	T_A = 25°C T_A = Full Range
Input Bias Current		500	1500 2000		500	1500 2000	nA nA	I_B	T_A = 25°C T_A = Full Range
Large Signal Voltage Gain	25 15	100		25 15	100		V/mV V/mV	A_{VOL}	$R_L \geq 600\Omega$, $V_O = \pm 10V$ T_A = 25°C T_A = Full Range
Supply Current (Each Amplifier)		4	8		4	8	mA	I_{CC}	R_L = Open
Output Swing	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V	V_{OUT}	$R_L \geq 600\Omega$ V_{CC} = V_{EE} = 15V V_{CC} = V_{EE} = 18V
Output Short Circuit Current		38			38		mA	I_{SC}	(Note 2)
Input Resistance	30	100		30	100		kΩ	R_{IN}	
Common-Mode Range	±12	±13		±12	±13		V	V_{iCM}	
Common-Mode Rejection	70	100		70	100		dB	CMRR	
Power Supply Rejection		10	100		10	100	μV/V	PSRR	
Channel Separation		110			110			dB	f = 1 kHz, R_S = 5 kΩ
AC CHARACTERISTICS									
Transient Response Rise Time		20			20		nsec	t_r	Voltage Follower R_L = 600Ω, C_C = 22 pF
Overshoot		20			20		%	t_o	C_L = 100 pF V_{IN} = 50 mV
AC Gain									f = 10 kHz
		6 2.2			6 2.2		V/mV V/mV		C_C = 0 C_C = 22 pF
Unity-Gain Bandwidth		10			10		MHz	BW	C_C = 22 pF, C_L = 100 pF
Slew Rate		13 6			13 6		V/μsec V/μsec		C_C = 0 C_C = 22 pF
Power Bandwidth		95 200			95 200		kHz kHz	f_p	V_{OUT} = ±10V, C_C = 22 pF C_C = 0 pF
NOISE CHARACTERISTICS									
Input Noise Voltage		5.5 3.5	7 4.5		7 4		nV/√Hz nV/√Hz	e_n	f_0 = 30 Hz f_0 = 1 kHz
Input Noise Current		1.5 0.4			2.5 0.6		pA/√Hz pA/√Hz	i_n	f_0 = 30 Hz f_0 = 1 kHz
Broadband Noise Figure		0.9			0.9		dB	R_N	F_S = 5 kΩ f = 10 Hz to 20 kHz

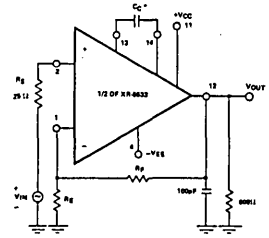
5

TEST CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT

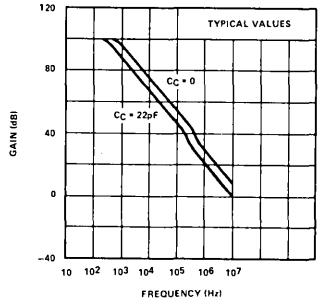


CLOSED LOOP FREQUENCY RESPONSE

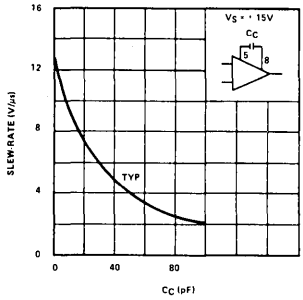


TYPICAL PERFORMANCE CHARACTERISTICS

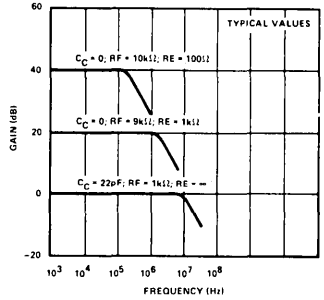
OPEN LOOP FREQUENCY RESPONSE



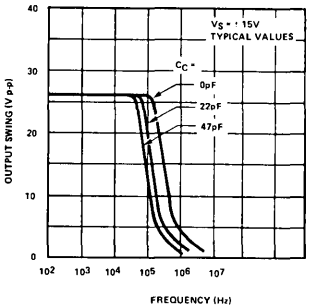
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



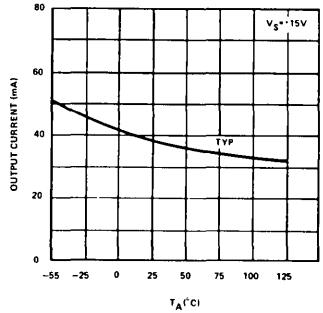
CLOSED LOOP FREQUENCY RESPONSE



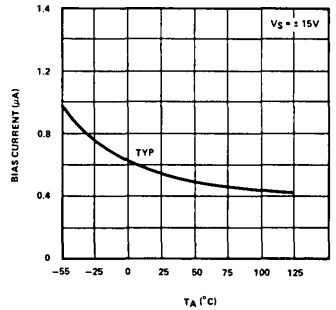
LARGE-SIGNAL FREQUENCY RESPONSE



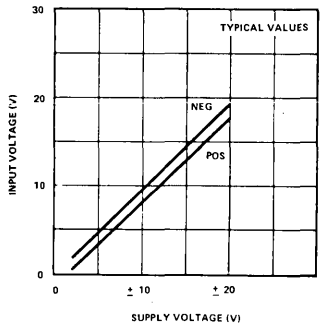
OUTPUT SHORT-CIRCUIT CURRENT



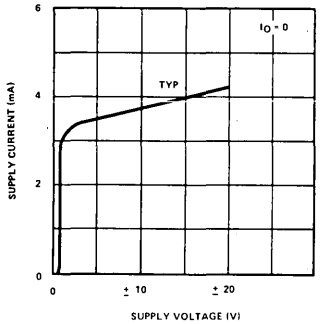
INPUT BIAS CURRENT



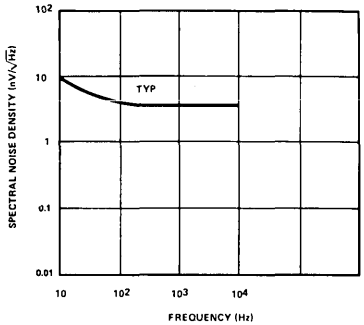
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT PER OP-AMP



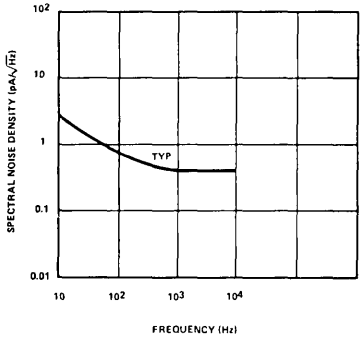
INPUT NOISE VOLTAGE DENSITY



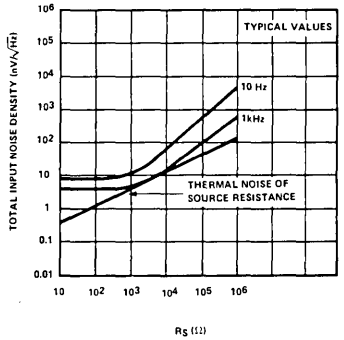
XR-5533/5533A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

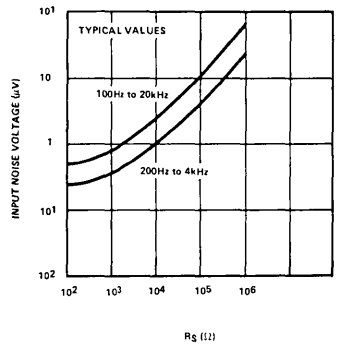
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

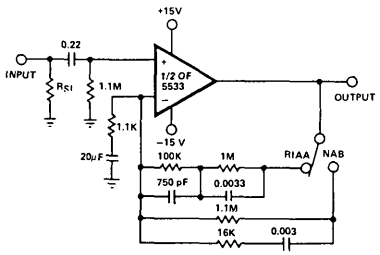


BROADBAND INPUT NOISE VOLTAGE

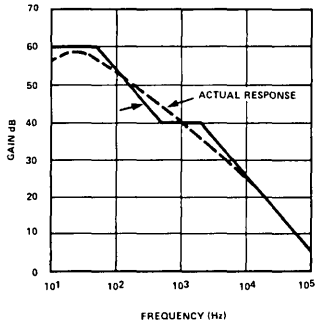


TYPICAL APPLICATION

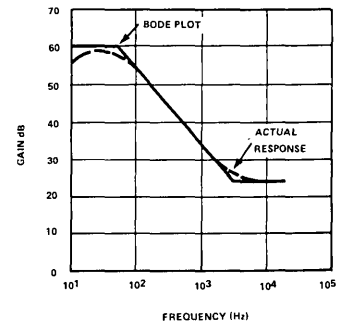
PREAMPLIFIER–RIAA/NAB COMPENSATION



*SELECT TO PROVIDE SPECIFIED TRANSDUCER LOADING
OUTPUT NOISE > 0.8 mV rms (WITH INPUT SHORTED)
ALL RESISTOR VALUES ARE IN OHMS.

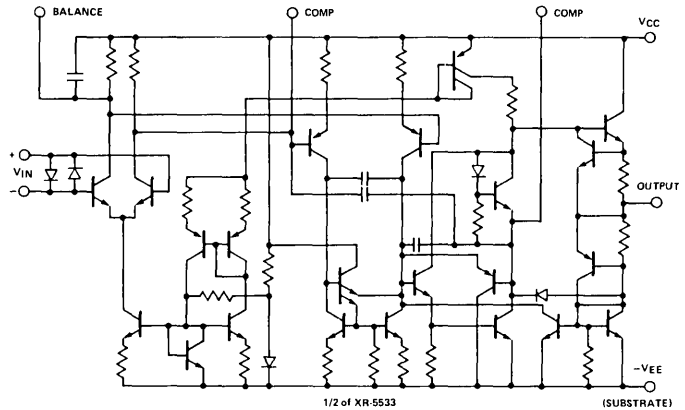


BODE PLOT OF RIAA EQUALIZATION AND THE RESPONSE REALIZED IN AN ACTUAL CIRCUIT USING THE XR-5533.



BODE PLOT OF NAB EQUALIZATION AND THE RESPONSE REALIZED IN THE ACTUAL CIRCUIT USING THE XR-5533

EQUIVALENT SCHEMATIC DIAGRAM



Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The XR-5534 is a high performance low-noise operational amplifier especially designed for application in high quality and professional audio equipment. It offers five-fold improvement in noise characteristics, output drive capability and full-power bandwidth over conventional 741-type op amps. The op amp is internally compensated for gain equal to, or higher than, three. The frequency response can be optimzed with an external compensation capacitor for various applications such as operating in unity gain mode or driving capacitive loads.

The XR-5534A is a specially-screened version of the XR-5534, with guaranteed noise specifications.

FEATURES

Direct Replacement for Signetics NE/SE 5534
Wide Small-Signal Bandwidth: 10 MHz
High-Current Drive Capability
(10V rms into 600Ω at $V_S = \pm 18V$)
High Slew Rate: 13 V/μs
Wide Power-Bandwidth: 200 kHz typ.
Very Low Input Noise: 4 nV/√Hz typ.

APPLICATIONS

High Quality Audio Amplification
Telephone Channel Amplifiers
Servo Control Systems
Low-Level Signal Detection
Active Filter Design

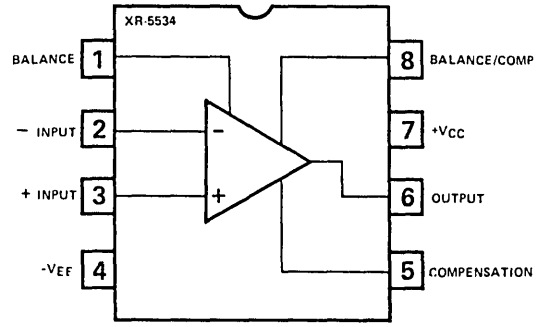
ABSOLUTE MAXIMUM RATINGS

Power Supply	±22 V
Input Common-Mode Voltage	$+V_{CC}$ to $-V_{EE}$
Differential Input Voltage (Note 1)	±0.5 V
Power Dissipation (Package Limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate Above +24°C	2.5 mW/°C
Short Circuit Duration (Note 2)	Indefinite
Storage Temperature	−60°C to +150°C

Note 1: Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10 mA.

Note 2: Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
5534AM	Ceramic	−55°C to +125°C
5534M	Ceramic	−55°C to +125°C
5534ACN	Ceramic	0°C to +70°C
5534CN	Ceramic	0°C to +70°C
5534ACP	Plastic	0°C to +70°C
5534CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-5534 and XR-5534A are monolithic operational amplifiers featuring low noise and a very large gain bandwidth product. The devices offer low output resistance and can drive 10 Vrms into 600Ω. Input noise is 100% tested on the XR-5534A, and is typically only 4 nV/√Hz. The small signal bandwidth is 10 MHz and slew rate exceeds 13 V/μS.

Reverse parallel diodes provide input protection; maximum differential input voltage is 0.7 V. Balance pins are provided to zero offset voltage. The device is internally compensated for gains ≥3 and provides external compensation pins for unity gain applications. Supply voltage may range from ±3V to ±20V.

XR-5534/5534A

ELECTRICAL CHARACTERISTICS

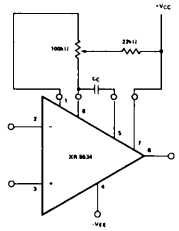
Test Conditions: T_A = 25°C, V_{CC} = V_{EE} = 15V, unless otherwise specified.

PARAMETERS	XR-5534M/5534AM			XR-5534AC/XR-5534C			UNITS	SYMBOL	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
DC CHARACTERISTICS									
Input Offset Voltage		0.5	2 3		0.5	4 5	mV mV	V_{OS}	T_A = 25°C T_A = Full Range
Input Offset Current		10	200 500		20	300 400	nA nA	I_{OS}	T_A = 25°C T_A = Full Range
Input Bias Current		400	800 1500		500	1500 2000	nA nA	I_B	T_A = 25°C T_A = Full Range
Large Signal Voltage Gain	 50 25	 100		 25 15	 100		 V/mV V/mV	A_{VOL}	$R_L \geq 600\Omega$, V_O = ±10V T_A = 25°C T_A = Full Range
Supply Current		4	6.5		4	8	mA	I_{CC}	R_L = Open
Output Swing	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V	V_{OUT}	$R_L \geq 600\Omega$ V_{CC} = V_{EE} = 15V V_{CC} = V_{EE} = 18V
Output Short Circuit Current		38			38		mA	I_{SC}	(Note 2)
Input Resistance	50	100		30	100		kΩ	R_{IN}	
Common-Mode Range	±12	±13		±12	±13		V	V_{ICM}	
Common-Mode Rejection	80	100		70	100		dB	CMRR	
Power Supply Rejection		10	50		10	100	μV/V	PSRR	
AC CHARACTERISTICS									
Transient Response									Voltage Follower
Rise Time		20			20		nSec	t_r	$R_L \geq 600\Omega$, C_C = 22 pF
Overshoot		20			20		%	t_0	C_L = 100 pF
AC Gain		 6 2.2			 6 2.2		 6 2.2	 V/mV V/mV	f = 10 kHz C_C = 0 C_C = 22 pF
Unity-Gain Bandwidth		10			10		MHz	BW	C_C = 22 pF, C_L = 100 pF
Slew Rate		13 6			13 6		V/μsec V/μsec		C_C = 0 C_C = 22 pF
Power Bandwidth		95 200			95 200		kHz kHz	f_p	V_{OUT} = ±10V, C_C = 22 pF C_C = 0
NOISE CHARACTERISTICS									
PARAMETERS	XR-5534A			XR-5534			UNITS	SYMBOL	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
Input Noise Voltage		5.5 3.5	7 4.5		7 4		nV/√Hz nV/√Hz	e_n	f_O = 30 Hz f_O = 1 kHz
Input Noise Current		1.5 0.4			2.5 0.6		pA/√Hz pA/√Hz	i_n	f_O = 30 Hz f_O = 1 kHz
Broadband Noise Figure		0.9					dB	F_N	R_S = 5 kΩ f = 10 Hz to 20 kHz

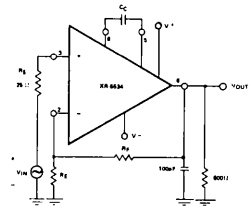
5

TEST CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT

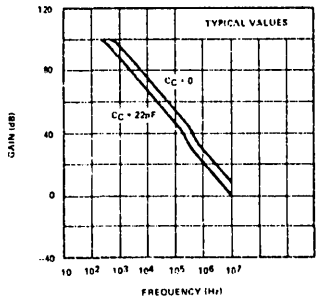


CLOSED LOOP FREQUENCY RESPONSE

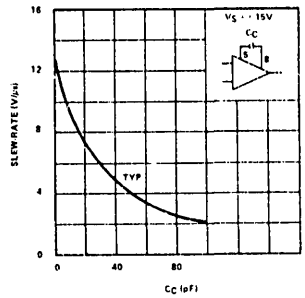


TYPICAL PERFORMANCE CHARACTERISTICS

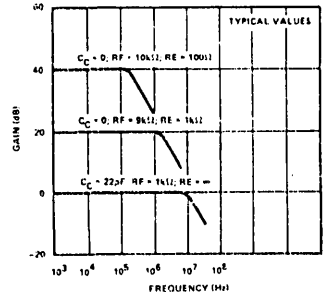
OPEN LOOP FREQUENCY RESPONSE



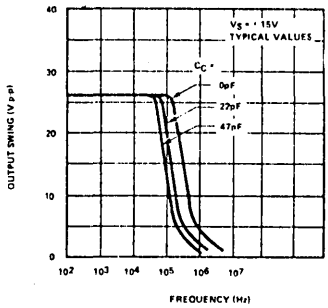
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



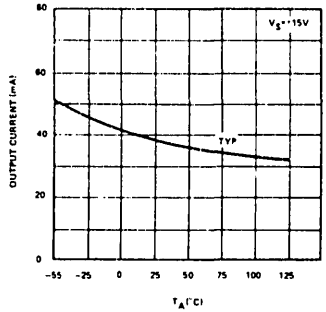
CLOSED LOOP FREQUENCY RESPONSE



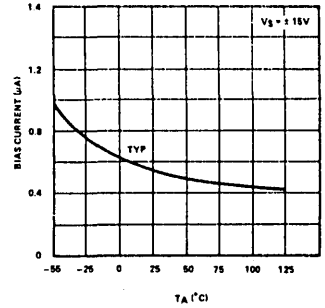
LARGE-SIGNAL FREQUENCY RESPONSE



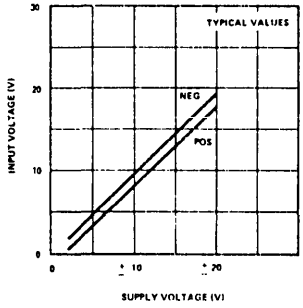
OUTPUT SHORT-CIRCUIT CURRENT



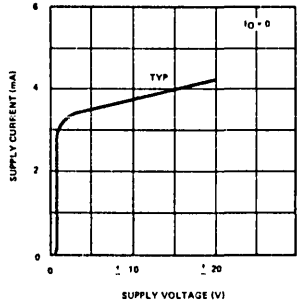
INPUT BIAS CURRENT



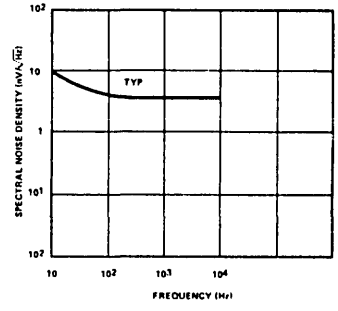
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT



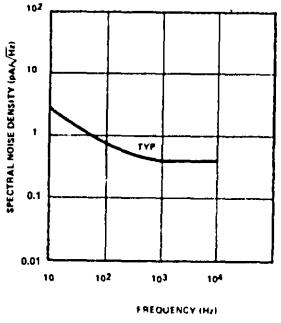
INPUT NOISE VOLTAGE DENSITY



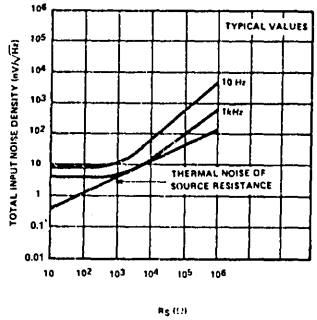
XR-5534/5534A

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

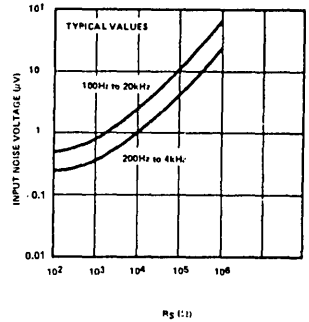
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

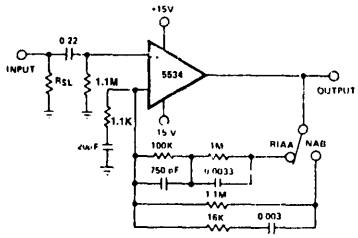


BROADBAND INPUT NOISE VOLTAGE

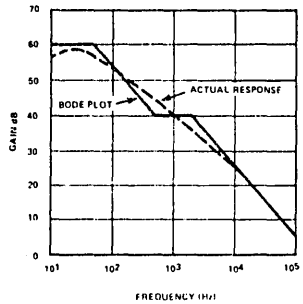


TYPICAL APPLICATION

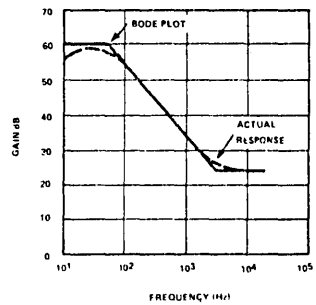
PREAMPLIFIER–RIAA/NAB COMPENSATION



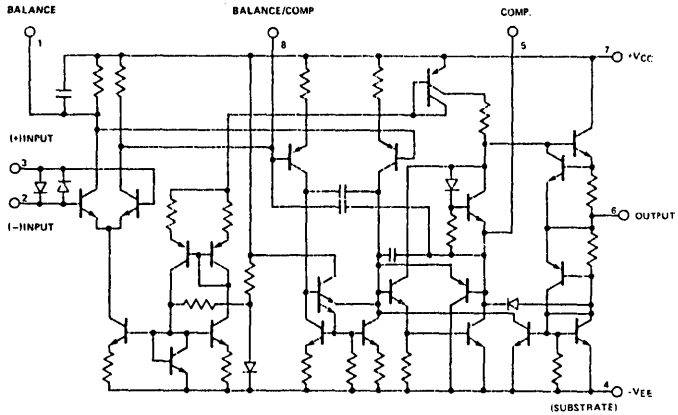
*SELECT TO PROVIDE SPECIFIED TRANSDUCER LOADING
OUTPUT NOISE = 0.8 mV rms (WITH INPUT SHORTED)
ALL RESISTOR VALUES ARE IN OHMS



BODE PLOT OF RIAA EQUALIZATION AND THE RESPONSE REALIZED IN AN ACTUAL CIRCUIT USING THE XR-5534.



BODE PLOT OF NAB EQUALIZATION AND THE RESPONSE REALIZED IN THE ACTUAL CIRCUIT USING THE XR-5534.



EQUIVALENT SCHEMATIC DIAGRAM

Section 5 – Industrial Circuits

Fundamentals of IC Timers

Monolithic timing circuits or *timers* find a wide variety of applications in both linear and digital signal processing. In a large number of industrial control or test sequencing applications, these circuits provide direct and economical replacement for mechanical or electromechanical timing devices.

Monolithic timers generate precise timing pulses, or time delays whose length or repetition rate is determined by an external timing resistor, R, and a timing capacitor, C. The timing interval is proportional to the external (RC) product, and can be varied from microseconds to minutes, days or months, by the choice of the external R and C. Integrated circuit timers can be classified into two categories, based on their principle of operation:

1. **One-Shot or Single-Cycle Timers:** These timer IC's operate by charging an external capacitor with a current set by an external resistor. Upon triggering, the charging cycle happens only *once* during the timing interval. The total timing interval, T, is the time duration necessary for the voltage across the capacitor to reach a threshold value.

2. **Multiple-Cycle or Timer/Counters:** These timer circuits charge and discharge the external timing capacitor, not once, but a *multiple number of times* during the timing interval. The number of times the capacitor is charged and discharged is set by means of a pre-set count, N, stored in a binary counter included on the chip. Thus, the resulting time interval is proportional to N times the external (RC) product.

Both the one-shot and the timer/counter type IC's can be operated in either their monostable or free-running (i.e., self-triggering) mode. They can also be used for sequential timing, clock generation, as well as for pulse-position or pulse-width modulation, as outlined in Table I.

Precision Timing
Time-Delay Generation
Sequential Timing
Pulse Generation/Shaping
Pulse-Position Modulation
Pulse-Width Modulation
Missing-Pulse Detection
Sweep Generation
Pulse Counting
Clock Generation

Table 1. Typical Applications of Monolithic Timers

ONE-SHOT OR SINGLE-CYCLE TIMERS

One-shot or single-cycle timers operate by charging a timing capacitor through an external resistor or a current source. The simplest form of the one-shot type timer is the "exponential-ramp generator" circuit shown in Figure 1. Normally all the components except the R and the C shown in the Figure are internal to the IC, and the switch S_1 is a grounded-emitter NPN transistor included in the IC chip.

The operation of the circuit can be briefly explained as follows: In the rest, or reset condition, the switch S_1 is closed; and the voltage across the capacitor is clamped to ground. The timing cycle is initiated by applying an external trigger pulse to "set" the flip-flop and to open the switch S_1 across the timing capacitor. The voltage across the capacitor rises exponentially toward the supply voltage, V_{CC}, with a time-constant of RC. When this voltage level reaches an internally set threshold voltage, V_{REF}, the voltage comparator changes state, resets the flip-flops, closes the switch S_1, and end the timing cycle. The output is taken from either the Q or $\overline{Q}$ terminal of the flip-flop and corresponds to a timing pulse of duration T, where:

$$T = RC \ln \left[\frac{V_{CC}}{V_{CC} - V_{REF}} \right] \quad (1)$$

Normally, the internal threshold voltage, V_{REF}, is generated from the supply voltage by means of a resistor divider as shown in Figure 1. Then, V_{REF} is equal to a fraction of the supply voltage:

$$V_{REF} = V_{CC} \left[\frac{R_2}{R_1 + R_2} \right] \quad (2)$$

and the basic timing equation becomes independent of the supply voltage:

$$T = RC \ln \left[1 + \frac{R_2}{R_1} \right] \quad (3)$$

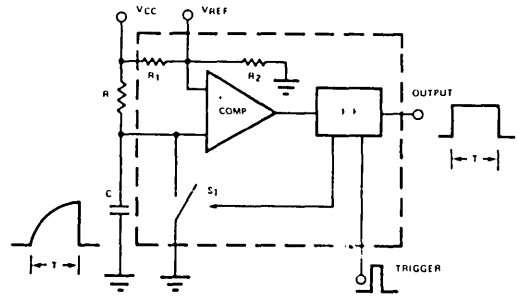


Figure 1. Exponential-Ramp Type Timing Circuit

Since the resistors R_1 and R_2 are inside the IC, their ratio is set by the design of the IC, and is normally accurate to within ±1%. Thus, virtually all the accuracy of the timing interval is determined by the external R and C.

An alternate approach to the design of one-shot timers is the "linear-ramp generator" circuit, shown in Figure 2. This circuit operates on a principle similar to that of the basic exponential timer, except the timing capacitor C is now charged *linearly* with a constant current, I, and generates a linear-ramp waveform with a constant slope of (I/C). The constant-current is in turn controlled by an external control voltage, V_C, applied to the current source. The total timing interval, T, is the time necessary for the voltage across C to rise from ground to V_{REF}, at a constant slope of (I/C), or:

$$T = (V_{REF})(C/I) \qquad (4)$$

Normally, V_{REF} and V_C (and consequently I) would be derived from V_{CC} by means of resistor-dividers; therefore, they would be both proportional to V_{CC}. Thus, the effects of supply voltage variations cancel, and the basic timing equation for the linear-ramp type timer circuit of Figure 2 becomes

$$T = \alpha RC$$

where α is a constant of proportionality set by the internal resistor-dividers within the IC, and R and C are the external timing components.

The exponential-ramp type timing circuit of Figure 1 is inherently simpler and more accurate than the linear-ramp type circuit. However, the latter has the advantage of providing a linear voltage across the capacitor which is proportional to the *elapsed-time* during the timing cycle and can be used as a "linear sweep" or time-base signal for oscilloscope or X-Y recorder displays.

Normally, the internal threshold reference, V_{REF}, of one-shot IC's is available as a package terminal and can be modulated by an external input signal. This permits the user to modulate or vary the timing interval by means of an external control signal. This feature can also be used for generating pulse-width modulated (PWM), or pulse-position modulated (PPM) signals, or allows the timer circuit to be used as a voltage-controlled oscillator.

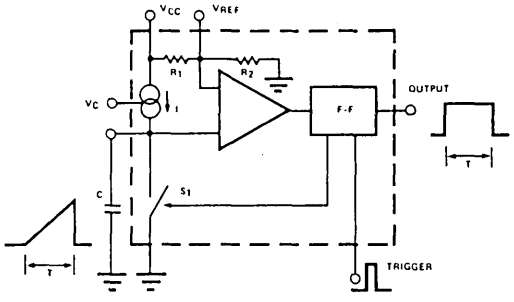


Figure 2. Block Diagram of a Linear-Ramp Type Timer Circuit

PRACTICAL LIMITATIONS OF ONE-SHOT TIMERS

The accurate timing intervals which can be obtained from commercially available one-shot type timer IC's are limited to the range of several micro-seconds to several minutes. For generating very short timing pulses (in the few micro-second range) the internal time delays associated with the switching speeds of the comparator, the flip-flop and the discharge transistor (i.e., the switch S_1) may contribute additional timing errors. Similarly, for long time delays (in the several minute range) which require large values of R and C, the input bias current of the comparator, and the leakage currents associated with the timing capacitor, or the internal discharge transistor, may limit the timing accuracy of the circuit.

In general, for timing applications requiring time delays in excess of several minutes, the multiple-cycle or timer/counter type timer circuits provide a more economical and practical solution than the one-shot type IC timers.

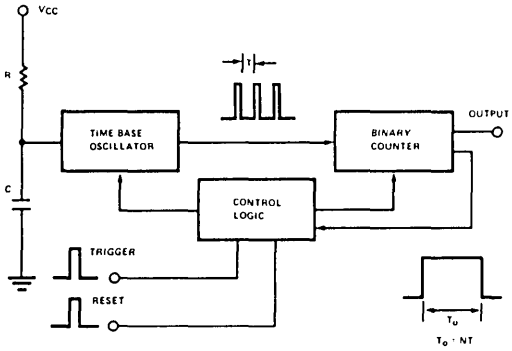


Figure 3. Simplified Block Diagram of a Timer/Counter

TIMER/COUNTER CIRCUITS

The timer/counter, or multiple-cycle timing circuits use the combination of a time-base oscillator and a binary counter to generate the desired time delay. Figure 3 shows a simplified block diagram of a timer/counter IC, which is made up of three basic blocks: (1) a time-base oscillator; (2) a binary counter; and (3) a control flip-flop.

With reference to the simplified block diagram of Figure 3, the principle of operation of a timer/counter can be explained as follows: when the circuit is at rest, or reset condition, the time-base oscillator is disabled, and the counter is reset to zero. Once the circuit is triggered, the time-base oscillator is activated and produces a series of timing pulses whose repetition rate is proportional to external timing resistor R, and the capacitor

C. These timing pulses are then counted by the binary counter; and when a pre-programmed count is reached, the binary-counter resets the control flip-flops, stops the time-base oscillator and ends the timing cycle. The total timing interval, T_0, is then proportional to N times the (RC) product, where N is the pre-programmed count.

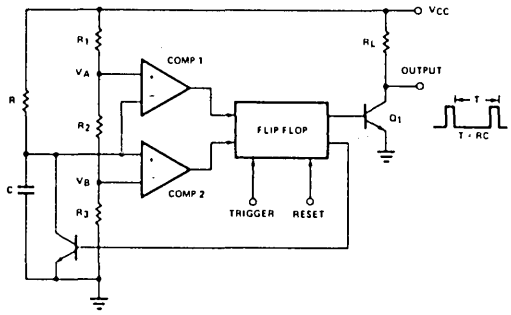


Figure 4. Simplified Schematic of a Time-Base Oscillator Circuit

Time-Base Oscillator: The time-base oscillator used in most of the timer/counter IC's is derived from the simple exponential-ramp type timer circuit. Figure 4 shows the simplified circuit diagram of such an oscillator. The timing components, R and C, are external to the chip. The operation of such an oscillator can be described as follows: when the circuit is at rest the flip-flop is latched in its reset state, and the transistor Q_1 is "off", the external capacitor C is fully charged to a voltage approximately equal to V_{CC}. When the circuit is triggered, the flip-flop is unlatched and set, which causes the discharge transistor Q_1 to turn "on" and discharge C rapidly. When the voltage across C discharges to the voltage level V_B, the comparator #2 changes state, resets the flip-flop and turns Q_1 "off". Then, C charges toward V_{CC} with a time constant set by the external R and C. When the voltage across it reaches the upper threshold, V_A, comparator #1 changes state and sets the flip-flop again, and discharges C back to the lower threshold level. V_B. In this manner, the circuit continues to oscillate, with the voltage level across C exponentially rising to V_A, then rapidly decaying to V_B, and then repeating its cycle. The output of the circuit is a sequence of narrow pulses, with a repetition rate T, given as:

$$T = RC \ln \left[1 + \frac{R_2}{R_1}\right] \qquad (6)$$

where R_1 and R_2 are the internal bias resistors setting up the threshold levels V_A and V_B. The train of output pulses coming out of the time-base oscillator are counted by the binary counter; and when a given count, N, is reached, the control flip-flop is latched in its reset condition until the next trigger input to the circuit.

In most timer/counter designs, it is convenient to set the ratio of resistors R_1 and R_2 such that:

$$\frac{(R_1 + R_2)}{R_1} = e = 2.718 \ldots \qquad (7)$$

where "e" is the base of the natural logorithm. This makes the period of the time-base oscillator directly equal to 1.0 RC and simplifies the selection of external R or C values for a given timer setting.

UNIQUE FEATURES OF TIMER/COUNTERS

The combination of a stable time-base oscillator and a programmable binary counter on the same IC chip offer some unique application and performance features. Some of these are outlined below:

Generating Long Delays with Small Capacitors: For a given time delay setting, the timer/counter would require a timing capacitor, C, that is N times smaller than that needed for the "one-shot" type timer, where N is the count programmed into the binary counter. Since large-value, low-leakage capacitors are quite expensive, this technique may provide substantial cost savings for generating long time delays in excess of several minutes.

Generating Ultra-Long Delays by Cascading: When a cascading two timer/counters, one cascades the counter stages of both timers. Since the second timer/counter further divides down the counter output of the first timer, the total available count is increased *geometrically*, rather than arithmetically. For example, if one timer/counter gives a time delay of NRC, two such timer/counters cascaded will produce a time delay of N^2 RC where N is the count setting of the binary counter. Thus, a cascade of two timer/counter IC's, each with an 8-bit binary counter, can produce a time delay in excess of 32,000 RC.

Generating Multiple Delays From Same RC Setting: By using a programmable binary counter, whose total count can be programmed between a minimum count of 1, to a maximum count of N, one can obtain N different time intervals from the same external RC setting.

Easy to Set or Calibrate: Although timer/counters are normally used for generating long time delays or intervals, their accuracy characteristics are only determined by the characteristics of the time-base oscillator. The counter section does not affect the over-all timing accuracy. Thus, time setting or calibration for long interval timing can be done quickly, without waiting for the entire timing cycle, by setting the accuracy of the time-base oscillator.

Choosing the Right IC Timer

Because of its versatility, the monolithic IC timer offers a very wide range of applications in circuit or system design. However, during the design phase, once the "paper design" is accomplished, the user is faced with the key question: which IC timer is the best choice for a given application? If the performance characteristics and the limitations of the timer IC is not carefully considered, the total system performance may be degraded; similarly, if the timing function is overspecified with an excessive amount of "overkill", particularly with regards to its stability and accuracy requirements, then the system cost will increase unnecessarily.

The key selection criteria in choosing the right timer for the job is finding the monolithic IC which will result in the lowest system cost (including the external components) for a given performance requirement.

A very large majority of applications for IC timers can be classified into one of the four categories listed below:

- Interval or Event Timing
- Pulse Generation and Shaping
- Oscillation or Clock-Generation
- Ramp Generation

These categories of applications are discussed in more detail in the following sections, with the particular emphasis on "choosing the right IC timer" for the particular application.

INTERVAL OR EVENT TIMING

In such an application one uses the IC timer either to control the *time interval* between events, or the *duration* of an event. A typical example of such application would be to control the opening or closing of an electromechanical relay or sequencing of indicator lights.

General Purpose Timing: Most timing applications fall within the time interval range of a few microseconds to several minutes. For such applications the basic one-shot timer, such as the XR-555, is often the best choice, based on its low cost and versatility.

Low-Power Timing: Many timing applications involving battery-operated or portable equipment, require a low-power timer which can perform the general purpose timing functions with a minimum amount of power dissipation. The XR-L555 Micropower Timer IC, which operates with less than 1 mW of power dissipation and with supply voltages as low as 2.7 volts, is especially designed for such applications.

Long Interval Timing: For timing applications requiring interval timing in the minutes, hours, or days range, the timer/counter IC's present the most economical approach, since they can produce long time delays using a small value capacitor. For such an application of the low-cost XR-2242 Long Range Timer, which operates on the timer/counter principle, is the most cost-effective circuit.

Sequential Timing: Many timing applications require *sequencing* of timing functions, i.e., one timer completes its operation and initiates the next timer, and so on. Since these applications require a multiplicity of timer circuits, they are best served by dual-timer IC's, such as the XR-556 or the XR-2556.

Delayed Timing: Certain timing applications require that the start of the timing pulse be delayed by a specific time from the occurrence of the trigger. This can be easily accomplished by using a dual-timer, such as the XR-556, where one section of the dual-timer can be used to set the initial "delay" subsequent to the trigger; and the second section can be used to generate the actual timing pulse.

Event Counting: In such an application, one needs to keep an accurate count of "events" which are normally a series of incoming pulses. This function can be easily performed with a programmable timer/counter IC, such as the XR-2240, where the binary counter section can be programmed to count a given number of input pulses and stop the count, and/or reset the circuit when the programmed count is reached. In the case of the XR-2240, the existing count in the counters is displayed in a 8-bit parallel binary-format.

Digitally-Programmed Timing: Some timing applications may require that the timing interval be digitally programmable, without switching additional precision resistors and capacitors into the circuit. Such a function can be easily achieved by using a programmable timer/counter, such as the XR-2240, where output duration can be programmed from 1.0 RC to 255 RC, in 1 RC increments, where R and C are the external timing components.

PULSE GENERATION AND SHAPING

A popular class of applications for the one-shot type timers is pulse shaping or stretching. Some specific examples of such applications and the recommended types of IC timers for each are given below.

Pulse Stretching: In such an application the IC timer is operated in its monostable mode and is triggered by an input series of pulses, whose repetition period is *longer* than that timing period of the IC. The output from the timer will then have the same repetition rate as the input pulse train, except that each output pulse will now have a uniform duration or length, as set by the RC time constant of the timer. The two IC's best suited to this application are the XR-555 and the XR-320. The XR-555 has the advantage of low unit price, whereas the XR-320 has the advantage of being able to trigger on *either* positive- or negative-going edge of the input pulses.

Delayed-Pulse Generation: In this application it is necessary to convert the input pulse train to a different pulse sequence which has the *same* repetition rate but a *different* duration and a *different* phase. This function can

be accomplished with a dual-timer circuit, such as the XR-556 or the XR-2556, where the first timer which is triggered by the input signal, sets the phase difference or "delay" between the input and the output pulse sequence; and the second timer which is triggered at the trailing-edge of the first one, sets the output pulse-width.

Pulse Blanking: In this application it is necessary to selectively "interrupt" or "blank-out" a pulse train. Such an application can be performed using a dual-timer IC, such as the XR-556, where one section of the timer can be operated as a "pulse-stretcher" triggered by the input pulse train; and the second timer section can be triggered by a separate timing signal and serve as an enable/disable control for the first timer, thus interrupting or "blanking" its output during its timing interval.

Pulse-Width Modulation: In certain timing applications it is necessary to modulate the pulse-width of an output pulse sequence, without affecting its repetition rate. Such a requirement can be met by a one-shot timer, such as the XR-555, operating in its monostable mode and being triggered by a fixed-frequency input pulse-train. The width of the output pulses from the timer IC can be modified without affecting the repetition rate, by simply applying a control-voltage to the modulation terminal of XR-555.

Pulse-Position Modulation: This application requires the generation of a pulse sequence whose pulse-width is constant (and usually very narrow) and, whose repetition rate is modulated. Such a function can be easily implemented using a dual-timer IC, such as the XR-556, where the second timer generates the narrow output pulses when triggered by the output of the first timer. The first timer section is then operated in its free-running (i.e., astable) mode and its frequency is then externally modulated by applying a control-voltage to its modulation terminal.

OSCILLATION OR CLOCK-GENERATION

IC Timers can be operated in their free-running or "self-triggering" mode, to generate periodic timing pulses. Since the output pulse-width or the frequency can be controlled by the choice of external resistors and capacitors. These circuits make excellent low-cost clock oscillators, for a number of digital systems. Some of these applications are outlined below.

Clock Generator: In such applications, the IC is used to generate a fixed-frequency output waveform with nearly 50% duty cycle. The XR-555 timer, whose output duty-cycle can be controlled by the choice of two external resistors, is ideally suited for such an application, for clock frequencies up to 300 kHz.

High-Current Oscillator: Certain oscillator applications require that the circuit output should be able to source or sink high load currents ($\geq$ 100 mA) in order to drive electromechanical relays or capacitive loads. The XR-555 Timer IC, which can provide up to 200 mA of current drive, is well suited for such applications.

Micropower Oscillator: Battery operated or remote-controlled instruments often require a low-power clock oscillator. The XR-L555 Micropower Timer, which operates with less than 1 mW of power drain, is the recommended choice for such applications, since it dissipates 1/15th the power of the conventional 555-type timer.

Voltage-Controlled Oscillator: Voltage-controlled oscillator (VCO) circuits find a wide range of applications in phase-locked loop systems. The XR-555 (or its low-power/low-voltage version of the XR-L555) which has a separate modulation terminal (Pin 5) can be used as a VCO by applying the proper control voltage to its modulation terminal and operating the IC in its self-triggering mode.

Low-Voltage Oscillator: Low threshold CMOS logic circuits normally require stable clock oscillators which can operate with a single 3 volt supply. The XR-L555 Micropower Timer which can operate with supply voltages as low as 2.7 volts is particularly suited for such applications.

Ultra-Low Frequency Oscillator: Certain battery operated or remote-controlled equipment require a stable ultra-low frequency clock oscillator, whose frequency can be as low as one cycle per day. The XR-2242 Long-Range Timer circuit which produces a square-wave output with a period of 256 RC, when operating in its free-running mode, is a very cost-effective replacement for such an oscillator.

Digitally-Programmed Oscillator: In certain applications it may be necessary to program the frequency of an oscillator by means of a binary control signal, without switching additional resistors or capacitors into the circuit. The XR-2240 Programmable Timer/Counter, when operating in its delayed-trigger mode (see Exar Application Note AN-07) can be used in such an application to generate an output frequency whose period is equal to (N + 1)RC, where N is the binary count which can be digitally programmed by an external 8-bit binary signal, to be any integer between 1 and 255.

Binary Pattern Generator: In certain test instrumentation design, it is necessary to generate a pseudorandom binary data pattern, which would then repeat itself periodically. The XR-2240 Programmable Timer/Counter which provides eight separate "open-collector" outputs, can perform such a function by selective shorting of one or more of its outputs to a common pull-up resistor.

Tone-Burst Generator: Some instrumentation applications require the generation of a certain tone or frequency signal, at periodic intervals. This function can be accomplished using a dual-timer IC, such as the XR-556 or the XR-2556, where one of the timer sections would operate as a keyed oscillator which is turned "on" and "off" by the other timer section. The output of the first timer section will then be a "tone-burst", which will be present only during the timing cycle of the second timer.

RAMP GENERATION

In a number of timing applications, it is necessary to generate an analog voltage which is proportional to the time elapsed during the timing cycle. This function is particularly useful for generating linear sweep voltage for oscilloscope or X-Y recorder display applications and it can be accomplished either *linearly* or *digitally*, as described below.

Linear Ramp Generator: A linear ramp can be obtained by charging a timing capacitor with a constant-current source. Since the XR-320 Timer IC operates on such a principle, it is ideally suited for this application. Upon triggering, the XR-320 produces a positive-going ramp at its current-source output (Pin 3). This ramp starts from the ground level and rises up to a voltage level approximately equal to 80% of the supply voltage, during the timing interval. Since the current-source output at Pin 3 is a high impedance terminal, the sweep or linear ramp signal at this point should be buffered by a high impedance op amp connected as a voltage follower.
amp connected as a voltage follower.

Digital Ramp Generator: In certain applications, a digitally generated "staircase" voltage is preferred over a linear ramp signal. Such a digital ramp signal can be generated using the XR-2240 Programmable Timer/Counter, along with an external resistor ladder and a current-summing op amp. The digital ramp signal is particularly useful for analog-to-digital conversion or digital sample-and-hold applications.
tions.

Monolithic Timing Circuit

GENERAL DESCRIPTION

The XR-320 monolithic timing circuit is designed for use in instrumentation and digital communications equipment, and for a wide variety of industrial control and special testing applications. In many cases, this circuit provides a monolithic replacement for mechanical or electromechanical timing devices.

The XR-320 timing circuit generates precise timing pulses (or time delays) whose repetition rate (or length) is determined by an external timing resistor, R, and timing capacitor, C. The timing period is exactly equal to 2RC and can be continuously varied from 1 μsec to 1 hour. The circuits can be operated in a monostable or free-running (self-triggering) mode. They can be used for sequential timing and sweep generation, and also for pulse-position and pulse-width modulation.

The XR-320 integrated circuit is comprised of a stable internal bias reference, a precision current source, a voltage comparator, a flip-flop, a timing switch, and a pair of output logic drivers. The high current output at pin 12 can sink or source up to 100 milliamps of current.

FEATURES

Wide Timing Range: 1 μsec to 1 hour
High Accuracy: 1%
Excellent Temperature Stability: 100 ppm/°C
Wide Supply Voltage Range: 4.5V to 18V
Triggering with Positive or Negative-Going Pulses
Programmable
  Resistor Programming: 3 decades
  Capacitor Program: 9 decades
Logic Compatible Outputs
High Current Drive Capability: 100 mA

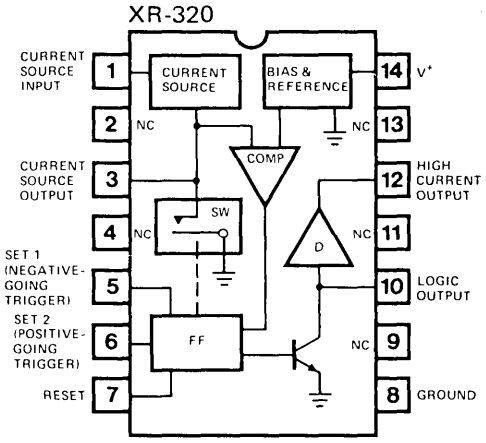
APPLICATIONS

Precision Timing
Time-Delay Generation
Sequential Timing
Pulse Generation/Shaping
Pulse-Position Modulation
Pulse-Width Modulation
Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Internal Power Dissipation	750 mW
Plastic Package:	625 mW
Derate above T_A = +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-320P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-320 is an extremely versatile monolithic timer capable of delays ranging from 1 μsec to 1 hour. It works with both positive and negative triggering, and features both normally high and normally low outputs. An on board current source, programmable by an external resistor, changes the timing capacitor. This produces a true ramp function and allows accurate timing intervals equal to 2 RC.

Positive going triggering is applied to Pin 6; negative triggering is applied to Pin 5. After a trigger pulse is applied, the open collector output (Pin 10) will go high and the high current output (Pin 12) switches into the current sink mode. At timeout, the open collector pulls low, and can sink 10 mA; the high current output goes high and can source 100 mA. Utilizing the high current output requires a pull-up resistor from Pin 10 to $+V_{CC}$. The resistor must limit current to no more than 10 mA; 1 mA is sufficient. Timing is interrupted and the device is reset when Pin 7 is grounded. Astable operation is attained by tying the negative going (falling) trigger (Pin 5) to the timing capacitor (Pin 3). In this configuration, the device will automatically retrigger itself upon completion of the timing interval.

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = 12V ±5%, Test Circuit of Figure 2, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-320 MIN	XR-320 TYP	XR-320 MAX	UNITS	CONDITIONS
Supply Voltage	4.5		18	V_{dc}	
Quiescent Supply Current					
V+ = 5V		2.0	3.5	mA	
V+ = 12V		6.0	7.0	mA	
V+ = 18V		10.0	12.5	mA	
Timing Cycle Supply Current					
V+ = 5V		2.5	4.0	mA	
V+ = 12V		6.5	8.0	mA	
V+ = 18V		12.0	14.0	mA	
Timing Accuracy					
V+ = 5V		1.0	5.0	%	
V+ = 12V		1.0	5.0	%	
V+ = 18V		1.0	5.0	%	
Temperature Drift		100		ppm/°C	
Timing vs. Supply Voltage		0.1	0.5	%/V	
Stand-by Voltage (Pin 3)		0.7		V	
Comparator Threshold Voltage (Pin 3)					
V+ = 5V		2.4		V	
V+ = 12V	4.5	5.2	6.0	V	
V+ = 18V		8.4		V	
Current Source Input Voltage (Pin 1)					
V+ = 5V		4.15		V	
V+ = 12V	9.0	9.75	10.6	V	
V+ = 18V		16.15		V	
Trigger Voltage					
Set (Pin 5)		1.0	1.5	V	See Figure 11
Set 2 (Pin 6)	0.5	1.4		V	See Figure 12
Reset (Pin 7)		0.7	1.5	V	
Trigger Current					
Set 1 (Pin 5)		10		μA	
Set 2 (Pin 6)		60		μA	
Reset (Pin 7)		30		μA	
Output 1 (Pin 10) (Normally low)					
"Low" Voltage		0.1		V	
"High" Voltage	4.0	5.0		V	
Rise Time		140		nsec	
Fall Time		50		nsec	
Output 2 (Pin 12) (Normally high)					
"High" Voltage		10.4		V	I_{source} = 100 mA
"Low" Voltage		1.5		V	I_{sink} = 100 mA
Rise Time		100		nsec	
Fall Time		40		nsec	

DEFINITIONS

Timing Accuracy: the timing error solely introduced by the XR-320, defined in per cent as:

$$100 \times \frac{\text{measured timing pulse length} - \text{2 RC based on actual component values}}{\text{2 RC based on actual component values}} \%$$

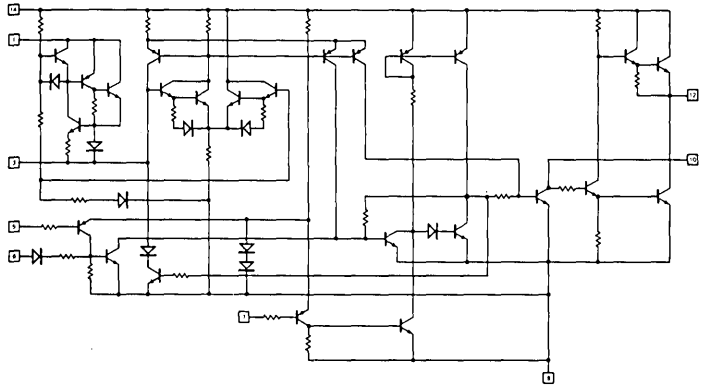
Timing vs Supply Voltage: the maximum timing drift over the power supply range of 5 to 18 volts referenced to 12 volt operation, defined in per cent per volt as:

$$\frac{100}{15} \times \frac{\text{max. timing pulse length over 5 to 18 volt supply} - \text{min. timing pulse length over 5 to 18 volt supply}}{\text{timing pulse length with 12 volt supply}} \%/V$$

Stand-by Voltage: the voltage between pin 3 and ground in reset condition.

Comparator Threshold Voltage (Pin 3): the voltage at which the internal comparator triggers the flip-flop and the timing capacitor discharges.

Trigger Voltage: the DC voltage level applied to each set or reset terminal which causes the output to change state.



EQUIVALENT SCHEMATIC DIAGRAM

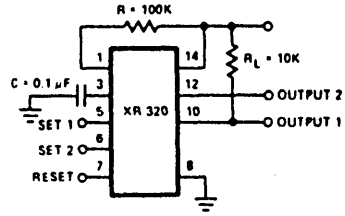


Figure 1. Test Circuit

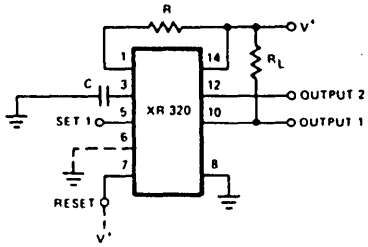


Figure 2. Monostable Operation, Negative Trigger

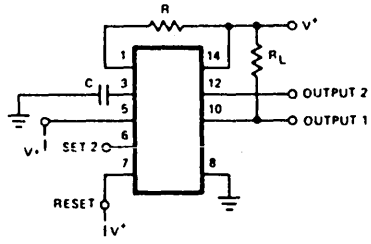


Figure 3. Monostable Operation, Positive Trigger

OPERATING INSTRUCTIONS

Figures 2 and 3 show typical connections for the XR-320. Only three external components are required for basic operation: the resistor R and capacitor C which determine the time delay (2RC); and an external load resistor, R_L. The circuit provides two independent logic outputs: a medium current output (up to 10 mA) at pin 10, and a high current output (up to 100 mA) at pin 12. The output at pin 10 is of the "bare-collector" type which requires an external pull-up resistor, R_L, connected between this terminal and V^+ for proper circuit operation.

With no trigger pulse applied, the output at pin 10 is in a low state near ground potential; and the output at pin 12 is in a high state, near V^+. The circuit is triggered by the application of a negative-going pulse to pin 5 or a positive-going pulse to pin 6. At that instant, the output levels change state such that pin 10 becomes high and pin 12 low. The outputs will remain in this (switched) state until the delay time, T = 2RC, expires, at which time the outputs will return to their original state. In this mode of operation, the trigger input can be activated repeatedly without further influencing the time cycle, i.e., once the circuit is triggered it becomes immune to subsequent triggering until the entire timing cycle is completed.

For reliable operation, the trigger pulse width must he shorter than the output pulse width. Although many units will function when this rule is not observed, proper operation cannot be guaranteed.

Figure 4 shows the waveforms at various circuit locations for a negative-going trigger applied to pin 5. A similar set of waveforms is displayed in Figure 5 for a positive-going pulse applied to pin 6. The timing cycle can be reset at any time by simply grounding pin 7.

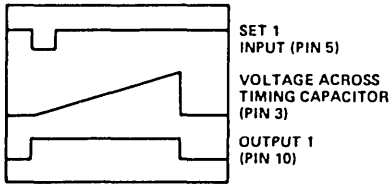


Figure 4. Waveforms for Negative-Going Trigger

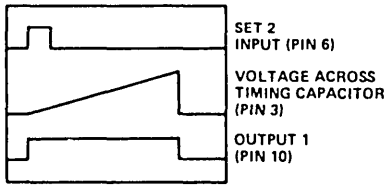


Figure 5. Waveforms for Positive-Going Trigger

DESCRIPTION OF CIRCUIT CONTROLS

TIMING RESISTOR (PIN 1)

Timing resistor, R, is connected between pin 1 and V+, pin 14. For maximum timing accuracy, R should be in the range 6 kΩ ≤ R ≤ 1 MΩ. See Figure 6 for the minimum and maximum values for R for various supply voltages.

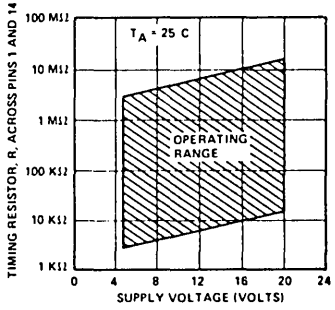


Figure 6. Operating Range as a Function of Timing Resistor and Supply Voltage

TIMING CAPACITOR (PIN 3)

Timing capacitor, C, is connected between pin 3 and ground. The time delay, T, is equal to 2RC in seconds. NOTE: A timing error can result due to the leakage current of the timing capacitor. When a capacitor with a relatively low insulation resistance (e.g. a high-valued electrolytic) is used as the timing capacitor, the resulting delay time will be much longer than 2RC because of the associated leakage current.

SET 1 — NEGATIVE TRIGGER (PIN 5)

A negative-going pulse applied to pin 5 will cause the outputs to change state. Output 1, pin 10, which is normally low will go high, Output 2, pin 12, which is normally high will go low. See Figure 11 for additional details. When not used, pin 5 should be connected to V+ to avoid false triggering.

By grounding or applying a negative pulse to the reset (Pin 7), the timing cycle is automatically interrupted and the outputs return to their original state. When the reset function is not in use, it is recommended that it be connected to V+ to avoid any possibility of false resetting.

SET 2 — POSITIVE TRIGGER (PIN 6)

A positive-going pulse applied to pin 6 will cause the outputs to change state. The normally low output at pin 10 will go high, and the normally high output at pin 12 will go low. See Figure 12 for additional details. When not used, pin 6 should be grounded to avoid false triggering.

ADDITIONAL APPLICATIONS

FREE-RUNNING MODE

By shorting pins 3 and 5, the XR-320 will operate in a "free-running" or self-triggering mode. In this mode of operation, the circuit functions as a stable clock pulse generator with a repetition rate of approximately 1/(2RC). The circuit connection and free-running frequency in this application are shown in Figure 7. Note that one cycle is not precisely equal to 2RC because of capacitor discharge time. Typical waveforms for self-triggered operation are shown in Figure 8.

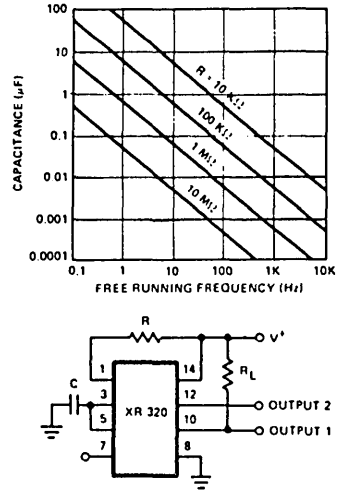


Figure 7. Free-Running Operation

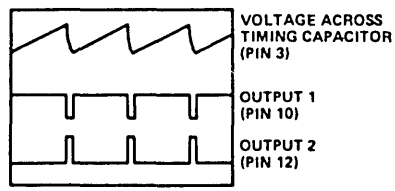


Figure 8. Waveforms for Self-Triggered Operation

SWEEP GENERATION

In self-triggered operation, the waveform across the timing capacitor (at pin 3) is a linear ramp as shown in Figure 8. The waveform at pin 3 can be used as a highly linear sweep voltage with a total nonlinearity of less than 1%.

PULSE-WIDTH MODULATION

For this application, the XR-320 should be connected as shown in Figure 9.

The modulation input is applied to pin 1 through coupling capacitor, C_C. The input signal modulates the current through the timing resistor, R, and, in turn, changes the width of the output timing pulses. The resistor R_M, in series with the signal source, is used to control the amount of modulation for a given input signal level.

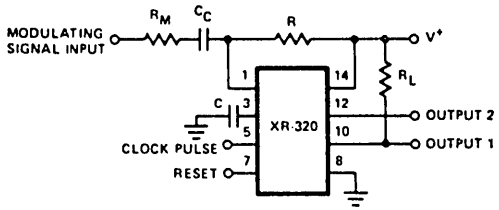


Figure 9. Circuit Connection for Pulse-width Modulation

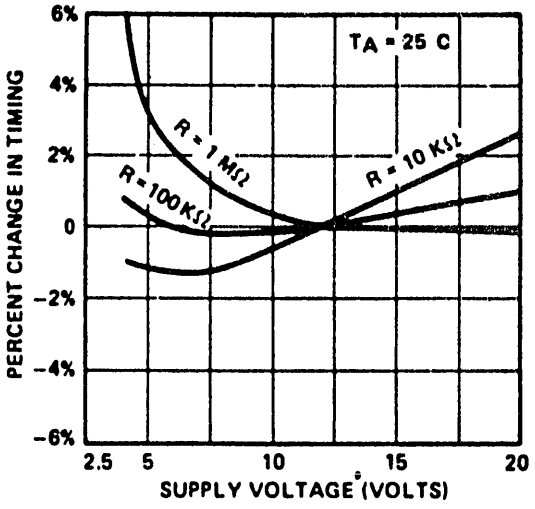


Figure 10. Change in Timing vs. Supply Voltage

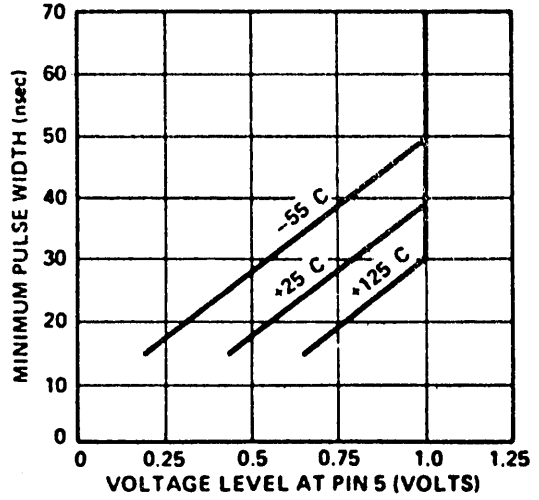


Figure 11. Minimum Pulse Width for Triggering at Pin 5

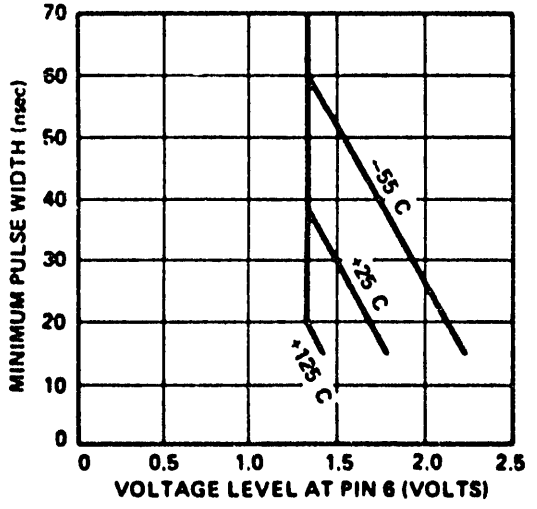


Figure 12. Minimum Pulse Width for Triggering at Pin 6

Timing Circuit

GENERAL DESCRIPTION

The XR-555 monolithic timing circuit is a highly stable controller capable of producing accurate timing pulses. It is a direct, pin-for-pin replacement for the SE/NE 555 timer. The circuit contains independent control terminals for triggering or resetting if desired.

In the monostable mode of operation, the time delay is controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are accurately controlled with two external resistors and one capacitor (as shown in Figure 2).

The XR-555 may be triggered or reset on falling waveforms. Its output can source or sink up to 200 mA or drive TTL circuits.

FEATURES

Direct Replacement for SE/NE 555
Timing from Microseconds Thru Hours
Operates in Both Monostable and Astable Modes
High Current Drive Capability (200 mA)
TTL and DTL Compatible Outputs
Adjustable Duty Cycle
Temperature Stability of 0.005%/°C

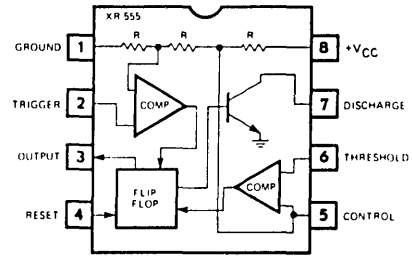
APPLICATIONS

Precision Timing
Pulse Generation
Sequential Timing
Pulse Shaping
Clock Generation
Missing Pulse Detection
Pulse-Width Modulation
Frequency Division
Pulse-Position Modulation
Appliance Timing

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature	−65°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-555M	Ceramic	−55°C to +125°C
XR-555CN	Ceramic	0°C to +70°C
XR-555CP	Plastic	0°C to +70°C

5

SYSTEM DESCRIPTION

The XR-555 is an industry standard timing circuit capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage, which may range from 4.5 V to 18 V. The output stage can source or sink 200 mA.

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operations (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, which provides a timing interval of 1.1 RC. As the reference is related to V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-555 is high during the timing interval, and pulls low at timeout. It is triggered and reset on falling waveforms. The control voltage input (Pin 5) may serve as a pulse width modulation point.

For applications requiring dual matched 555-type timers, see the XR-556 and XR-2556. For low voltage and/or low power drain applications, consider the XR-L555 and XR-L556 devices.

XR-555

ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.)

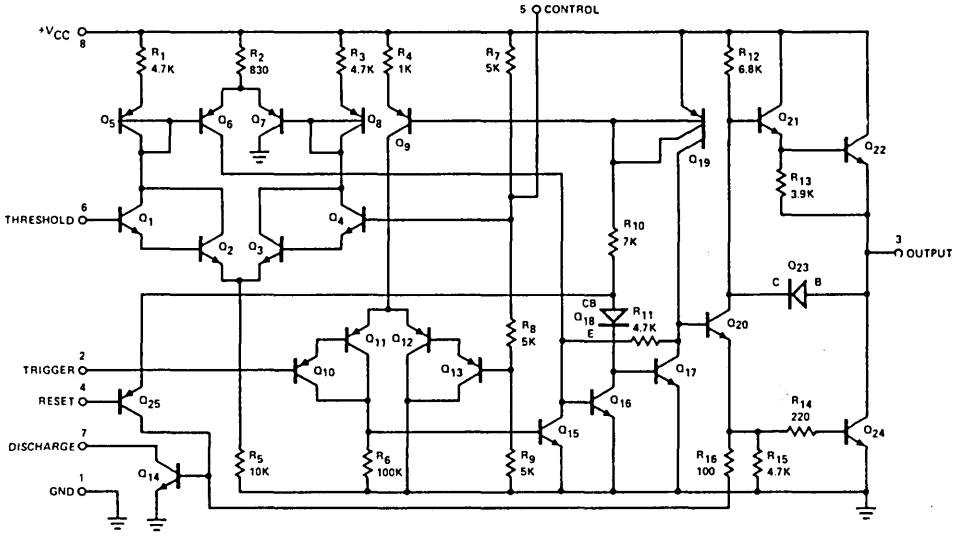
PARAMETERS	XR-555M			XR-555C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Supply Voltage	4.5		18	4.5		16	V	
Supply Current		3 10	5 12		3 10	6 15	mA mA	Low State Output (Note 1) V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞
Timing Error (Monostable) Initial Accuracy Drift with Temperature Drift with Supply Voltage		 0.5 30 0.05	 2.0 100 0.2		 1.0 50 0.1	 3.0 0.5	 % ppm/°C %/V	R_A, R_B = 1 KΩ to 100 KΩ Note 2, C = 0.1 μF 0°C ≤ T_A ≤75°C
Timing Error (Astable) Initial Accuracy (Note 2) Drift with Temperature Drift with Supply Voltage		 1.5 90 0.15			 2.25 150 0.3		 % ppm/°C %/V	R_A, R_B = 1 KΩ to 100 KΩ C = 0.1 μF V_{CC} = 15V
Threshold Voltage	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V	V_{CC} = 15V V_{CC} = 5V
Trigger Voltage	1.45 4.8	1.67 5.0	1.9 5.2		1.67 5.0		V V	V_{CC} = 5V V_{CC} = 15V
Trigger Current		0.5	0.9		0.5	2.0	μA	
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	Trigger Input High
Reset Current		0.4	1.0		0.4	1.5	mA	
Threshold Current		0.1	0.25		0.1	0.25	μA	(Note 3)
Control Voltage level	2,7 9.4	3.33 10.0	4.0 10.6	2.4 8.8	3.33 10.0	4.2 11.2	V V	V_{CC} = 5V V_{CC} = 15V
Output Voltage Drop (Low)		 0.10 0.05 0.1 0.4 2.0 2.5	 0.25 0.2 0.15 0.5 2.2		 0.3 0.25 0.1 0.4 2.0 2.5	 0.35 0.25 0.75 2.5	 V V V V V V	V_{CC} = 5V I_{sink} = 8.0 mA I_{sink} = 5.0 mA V_{CC} = 15V I_{sink} = 10 mA I_{sink} = 50 mA I_{sink} = 100 mA I_{sink} = 200 mA
Output Voltage Drop (High)	 3.0 13	 3.3 13.3 12.5		 2.75 12.75	 3.3 13.3 12.5		 V V V	I_{source} = 100 mA V_{CC} = 5V V_{CC} = 15V I_{source} = 200 mA V_{CC} = 15V
Turn Off Time (Note 4)		0.5	0.2		0.5		μs	V_{RESET} High
Rise Time of Output		100	200		100	300	nsec	
Fall Time of Output		100	200		100	300	nsec	
Discharge Transistor Leakage		20	100		20	100	nA	

Note 1: Supply current when output is high is typically 1.0 mA less.

Note 2: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 3: This will determine the maximum value of R_A + R_B for 15V operation. The maximum total R = 20 megohms and for 5V operation, the maximum R_T = 3.4 megohms.

Note 4: Time measured from a positive-going input pulse from 0 to 0.8 × V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.



EQUIVALENT SCHEMATIC DIAGRAM

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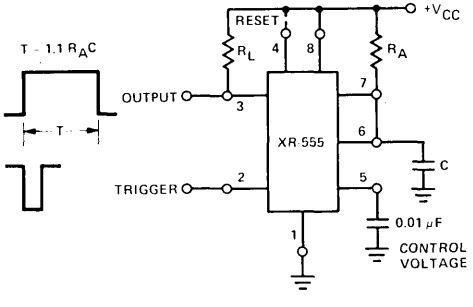


Figure 1. Monostable (One-Shot) Circuit

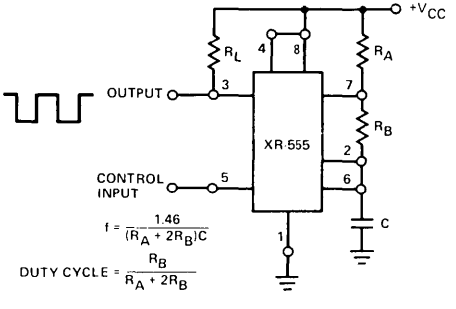


Figure 2. Astable (Free-Running) Circuit

Micropower Timing Circuit

GENERAL DESCRIPTION

The XR-L555 is a stable micropower controller capable of producing accurate timing pulses. It is a direct replacement for the popular 555-timer for applications requiring very low power dissipation. The XR-L555 has approximately 1/15th the power dissipation of the standard 555-timer and can operate down to 2.7 volts without sacrificing such key features as timing accuracy and frequency stability. At 5-volt operation, typical power dissipation of the XR-L555 is 900 microwatts.

The circuit contains independent control terminals for triggering or resetting if desired. In the monostable mode of operation, the time delay is controlled by one external resistor and one capacitor. For astable operation as an oscillator the free-running frequency and the duty cycle are accurately controlled with two external resistors and one capacitor as shown in Figure 2. The XR-L555 is triggered or reset on falling waveforms. Its output can source up to 100 mA or drive TTL circuits.

Because of its temperature stability and low-voltage (2.7V) operation capability, the XR-L555 is ideally suited as a micropower clock oscillator or VCO for low-power CMOS systems. It can operate up to 1500 hours with only two 300 mA-Hr batteries.

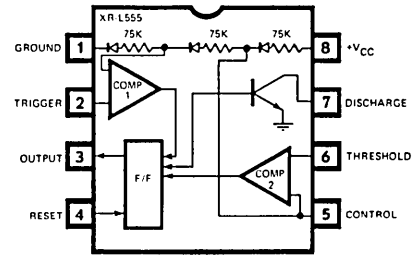
FEATURES

Pin Compatible with Standard 555 Timer
Less than 1 mW Power Dissipation (V+ = 5V)
Timing from Microseconds to Minutes
Over 1000-Hour Operation with 2 Batteries
Low Voltage Operation (V+ = 2.7V)
Operates in Both Monostable and Astable Modes
CMOS TTL and DTL Compatible Outputs

APPLICATIONS

Battery Operated Timing
Micropower Clock Generator
Pulse Shaping and Detection
Micropower PLL Design
Power-On Reset Controller
Micropower Oscillator
Sequential Timing
Pulse Width Modulation
Appliance Timing
Remote-Control Sequencer

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Storage Temperature	−65°C to +125°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L555M	Ceramic	−55°C to +125°C
XR-L555CN	Ceramic	0°C to +70°C
XR-L555CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-L555 is a micropower timing circuit similar to the industry standard 555-type timer. It is capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage which may range from 2.7 V to 15 V. The output stage can source 50 mA.

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operation (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-L555 is high during the timing interval. It is triggered and reset on falling waveforms. The control voltage input (Pin 5) may serve as a pulse width modulation point.

For applications requiring dual L555-type timers, see the XR-L556.

ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{CC} = +5V, unless otherwise specified.)

PARAMETERS	XR-L555M †			XR-L555C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Supply Voltage	2.7		15	2.7		15	V	
Supply Current		150	300		190	500	μA	Low State Output V_{CC} = 5V, R_L = ∞
Timing Error								R_A, R_B = 1 KΩ to 100 KΩ
Initial Accuracy		0.5	2.0		1.0		%	C = 0.1 μF
Drift with Temperature		30	100		50		ppm/°C	0°C ≤ T_A ≤ 75°C
Drift with Supply Voltage		0.05			0.05		%/V	
Threshold Voltage		2/3			2/3		x V_{CC}	
Trigger Voltage	1.45 4.8	1.67 5.0	1.9 5.2		1.67 5.0		V V	V_{CC} = 5V V_{CC} = 15V
Trigger Current		0.5			0.5		μA	
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	
Reset Current		0.1			0.1		mA	
Threshold Current		0.1	0.25		0.1	0.25	μA	
Control Voltage Level	2.90 9.6	3.33 10.0	3.80 10.4	2.60 9.0	3.33 10.0	4.00 11.0	V	V_{CC} = 5V V_{CC} = 15V
Output Voltage Drop (Low)		0.1	0.3		0.25	0.35	V	I_{sink} = 1.5 mA
Output Voltage Drop (High)								I_{source} = 10 mA
	3.0	3.3		2.75	3.3		V	V_{CC} = 5V
	13	13.3		12.75	13.3		V	V_{CC} = 15V
								I_{source} = 100 mA
		12.5			12.5		V	V_{CC} = 15V
Rise Time of Output		100			100		nsec	
Fall Time of Output		100			100		nsec	
Discharge Transistor Leakage		0.1			0.1		μA	

† Tested only at 25°C

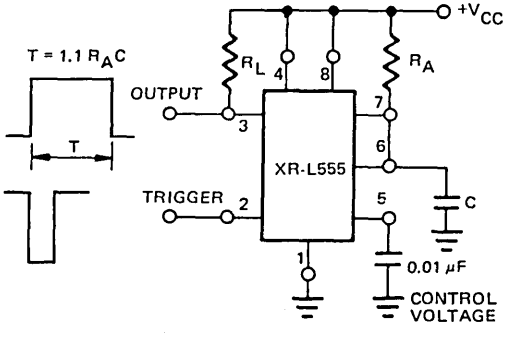


Figure 1. Monostable (One-Shot) Circuit

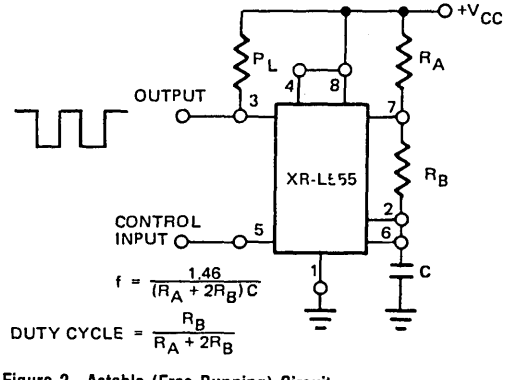


Figure 2. Astable (Free-Running) Circuit

XR-L555

CHARACTERISTIC CURVES

GENERAL CHARACTERISTICS

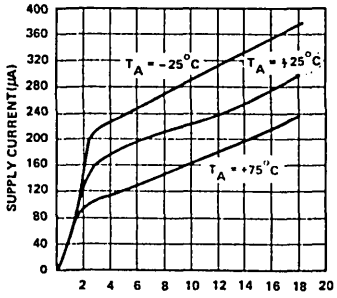


Figure 3. Supply Current as a Function of Supply Voltage

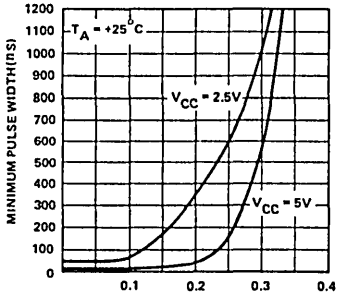


Figure 4. Minimum Pulse-Width Required for Triggering

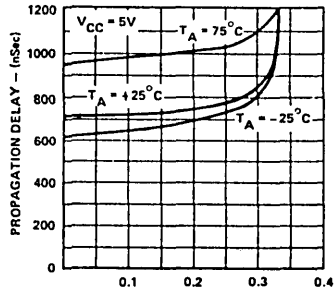


Figure 5. Propagation Delay as a Function of Voltage Level of Trigger Pulse

MONOSTABLE OPERATION

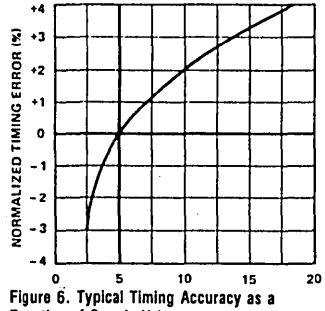


Figure 6. Typical Timing Accuracy as a Function of Supply Voltage

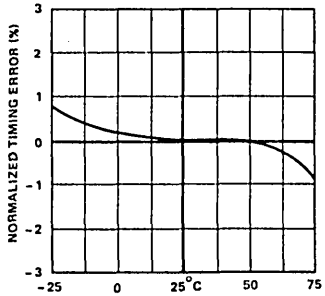


Figure 7. Typical Timing Accuracy as a Function of Temperature (V_{CC} = 51V, R_A = 100KΩ, C = 0.01 μF)

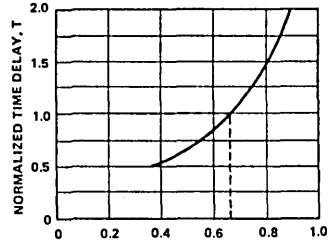


Figure 8. Normalized Time Delay as a Function of Control Voltage

ASTABLE OPERATION

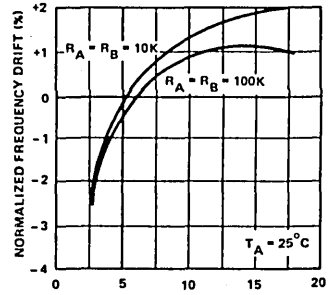


Figure 9. Typical Frequency Stability as a Function of Supply Voltage

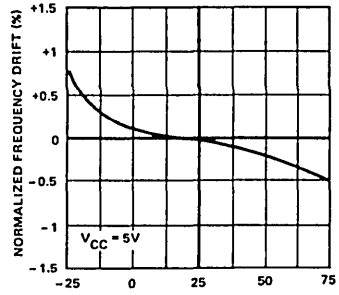


Figure 10. Typical Frequency Stability as a Function of Temperature (R_A = R_B = 10KΩ, C = 0.1 μF)

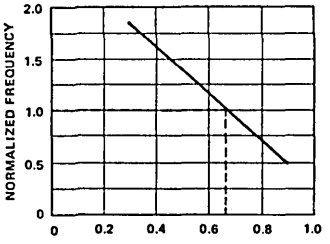


Figure 11. Normalized Frequency of Oscillation as a Function of Control Voltage

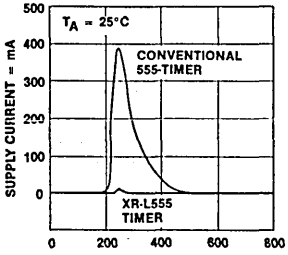


Figure 12. Comparison of Supply Current Transient of Conventional 555-Timer with XR-L555 Micropower Timer

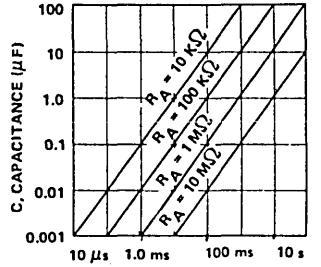


Figure 13. Timing Period, T, as a Function of External R-C Network

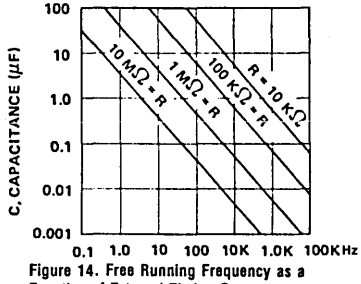


Figure 14. Free Running Frequency as a Function of External Timing Components (Note: R = R_A + 2R_B)

FEATURES OF XR-L555

The XR-L555 micropower timer is, in most instances, a direct pin-for-pin replacement for the conventional 555-type timer. However, compared to conventional 555-timer, it offers the following important performance features:

Reduced Power Dissipation: The current drain is 1/15th of the conventional 555-timer.

No Supply Current Transients: The conventional 555-timer can produce 300 to 400 mA of supply current spikes during switching. The XR-L555 is virtually transient-free as shown in Figure 12.

Low-Voltage Operation: The XR-L555 operates down to 2.7 volts of supply voltage, vs. 4.5V minimum operating voltage needed for conventional 555-timer. Thus, the XR-L555 can operate safely and reliably with two 1.5V batteries.

Proven Bipolar Technology: The XR-L555 is fabricated using conventional bipolar process technology. Thus, it is immune to electrostatic burn-out problems associated with low-power timers using CMOS technology.

APPLICATIONS INFORMATION

MONOSTABLE (ONE-SHOT) OPERATION

The circuit connection for monostable, or one-shot operation of the XR-L555 is shown in Figure 1. The internal flip-flop is triggered by lowering the trigger level at pin 2 to less than 1/3 of V_{CC}. The circuit triggers on a negative-going slope. Upon triggering, the flip-flop is set to one side, which releases the short circuit across the capacitor and also moves the output level at pin 3 toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_A C$. A high impedance comparator is referenced to 2/3 V_{CC} with the use of three equal internal resistors. When the voltage across the capacitor reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, and the output level moves toward ground, and the timing cycle is completed.

The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

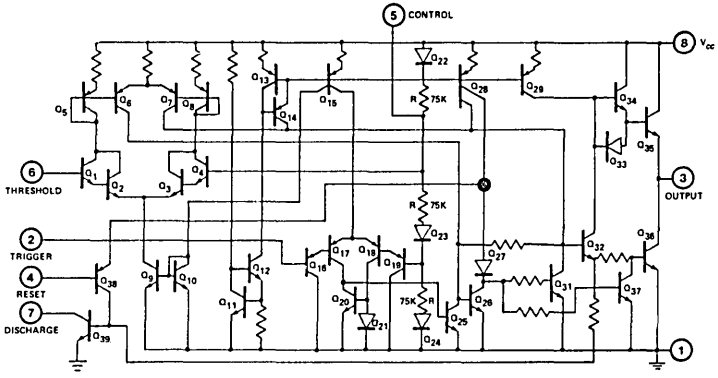
$$T = 1.1\ R_A C$$

The time delay varies linearly with the choice of R_A and C as shown by the timing curves of Figure 13. For proper operation of the circuit, the trigger pulse-width *must be* less than the timing period.

Once the circuit is triggered it is immune to additional trigger inputs until the present timing-period has been completed. The timing-cycle can be interrupted by using the reset control (pin 4). When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged, i.e. "low". The reset pin should be connected to $+V_{CC}$ when not used to avoid the possibility of false triggering.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 2. The external capacitor charges to 2/3 V_{CC} through the parallel combination of R_A and R_B, and discharges to 1/3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with an exponential waveform. The oscillations can be keyed "on" and "off" using the reset control. The frequency of oscillation can be readily calculated from the equations in Figure 2 and Figure 14.



EQUIVALENT SCHEMATIC DIAGRAM

Dual Timer

GENERAL DESCRIPTION

The XR-556 dual timing circuit contains two independent 555-type timers on a single monolithic chip. It is a direct, pin-for-pin replacement for the SE/NE 556 dual timer. Each timer section is a highly stable controller capable of producing accurate time delays or oscillations. Independent output and control terminals are provided for each section as shown in the functional block diagram.

In the monostable mode of operation, the time delay for each section is precisely controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle of each section are accurately controlled with two external resistors and one capacitor.

The XR-556 may be triggered or reset on falling waveforms. Each output can source or sink up to 150 mA or drive TTL circuits. The matching and temperature tracking characteristics between each timer section of the XR-556 are superior to those available from two separate timer packages.

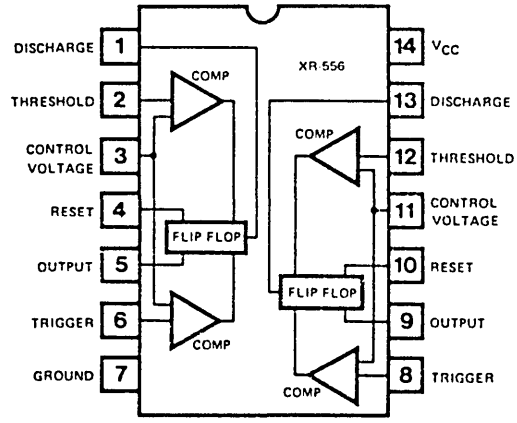
FEATURES

Direct Replacement for SE/NE 556
Replaces Two 555-Type Timers
TTL Compatible Pinouts
Timing from Microseconds Thru Hours
Excellent Matching Between Timer Sections
Operates in Both Monostable and Astable Modes
High Current Drive Capability (150 mA each output)
TTL and DTL Compatible Outputs
Adjustable Duty Cycle
Temperature Stability of 0.005%/°C

APPLICATIONS

Precision Timing
Pulse Generation
Sequential Timing
Pulse Shaping
Time Delay Generation
Clock Pattern Generation
Missing Pulse Detection
Pulse-Width Modulation
Frequency Division
Clock Synchronization
Pulse-Position Modulation
Appliance Timing

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

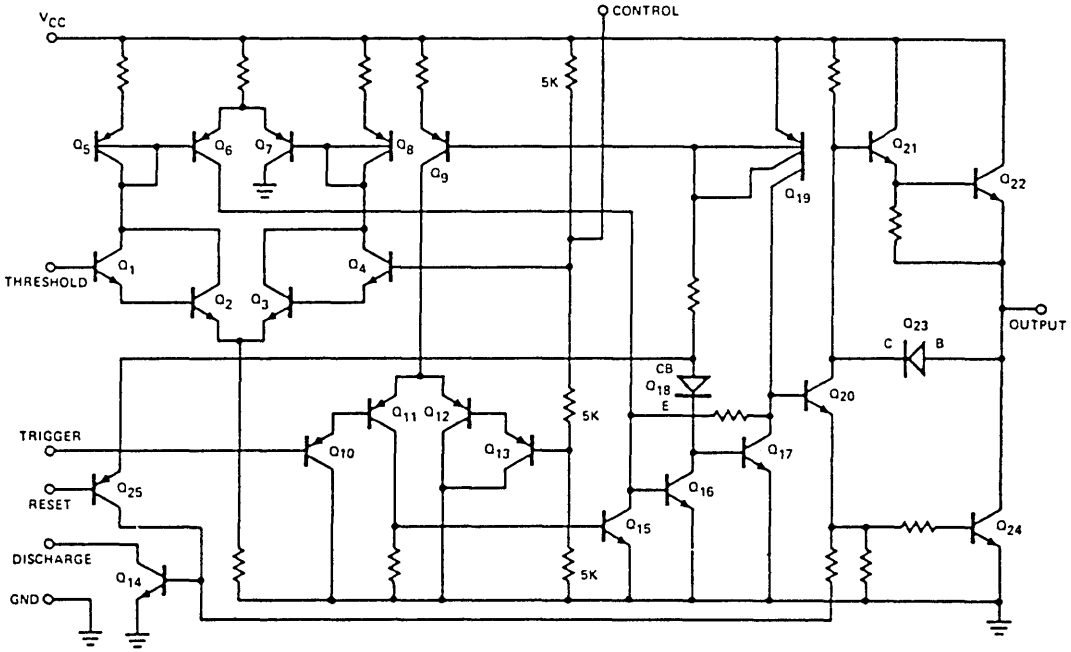
Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-556M	Ceramic	−55°C to +125°C
XR-556CN	Ceramic	0°C to +70°C
XR-556CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-556 is an industry standard dual timing circuit capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage, which may range from, 4.5 V to 18 V. The output stage can source or sink 150 mA. Each timer section is fully independent and similar to 555-type devices.



EQUIVALENT SCHEMATIC DIAGRAM

SYSTEM DESCRIPTION (continued)

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operation (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, which produces a timing interval of 1.1 RC. As the reference is related to V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-556 is high during the timing interval, and pulls low at timeout. It is triggered and reset on falling waveforms. The control voltage inputs (Pins 3 and 11) may serve as pulse width modulation points. Matching between sections is typically better than 0.05% initially, with temperature drift tracking to ±10 ppm/°C and supply voltage drift tracking to 0.1%/V. For low voltage and/or low power drain applications, consider the XR-L556.

XR-556

ELECTRICAL CHARACTERISTICS

Test Conditions: (Each timer section, T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.)

PARAMETERS	XR-556M			XR-556C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Supply Voltage	4.5		18	4.5		16	V	
Supply Current (Each Timer Section)								Low State Output, Note 1
		3	5		3	6	mA	V_{CC} = 5V, R_L = ∞
		10	11		10	14	mA	V_{CC} = 15V, R_L = ∞
Total Supply Current (Both Timer Sections)								Low State Output, Note 1
		6	10		6	12	mA	V_{CC} = 5V, R_L = ∞
		20	22		20	28	mA	V_{CC} = 15V, R_L = ∞
Timing Error (Monostable)								Timing, R = 1 KΩ to 100 KΩ
Initial Accuracy		0.5	1.5		.75	3	%	Note 2, C = 1.0 μF
Drift with Temperature		30	100		50		ppm/°C	0°C ≤ T_A ≤ 75°C
Drift with Supply Voltage		0.05	0.2		0.1	0.5	%/V	
Timing Error (Astable)								R_A, R_B = 1 KΩ to 100 KΩ
Initial Accuracy (Note 2)		1.5			2.25		%	C = 0.1 μF
Drift with Temperature		90			150		ppm/°C	V_{CC} = 15V
Drift with Supply Voltage		0.15			0.3		%/V	
Threshold Voltage	9.4	10.0	10.6	8.8	10.0	11.2	V	V_{CC} = 15V
	2.7	3.33	4.0	2.4	3.33	4.2	V	V_{CC} = 5V
Trigger Voltage								
	1.45	1.67	1.9		1.67		V	V_{CC} = 5V
	4.8	5.0	5.2	4.5	5.0	5.6	V	V_{CC} = 15V
Trigger Current		0.5	0.9		0.5	2	μA	V_{TRIG} = 0V
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	V_{TRIG} High
Reset Current		0.4	1		0.4	1.5	mA	V_{RESET} = 0V
Threshold Current		0.03	0.1		0.03	0.1	μA	Note 3
Control Voltage Level								
	2.90	3.33	3.80	2.60	3.33	4.00		V_{CC} = 5V
	9.6	10.0	10.4	9.0	10.0	11.0		V_{CC} = 15V
Output Voltage Drop (Low)								V_{CC} = 5V
		0.10	0.25		0.3		V	I_{sink} = 8.0 mA
		0.05	0.20		0.25	0.35	V	I_{sink} = 5.0 mA
								V_{CC} = 15V
		0.1	0.15		0.1	0.25	V	I_{sink} = 10 mA
		0.4	0.5		0.4	0.75	V	I_{sink} = 50 mA
		2.0	2.25		2.0	2.75	V	I_{sink} = 100 mA
		2.5			2.5		V	I_{sink} = 200 mA
Output Voltage Drop (High)								I_{source} = 100 mA
	3.0	3.3		2.75	3.3		V	V_{CC} = 5V
	13	13.3		12.75	13.3		V	V_{CC} = 15V
								I_{source} = 200 mA
		12.5			12.5		V	V_{CC} = 15V
Rise Time of Output		100	200		100	300	nsec	
Fall Time of Output		100	200		100	300	nsec	
Matching Characteristic								Note 4
Initial Timing Accuracy		0.05	0.1		0.1	0.2	%	
Timing Drift with Temperature		±10			±10		ppm/°C	
Drift with Supply Voltage		0.1	0.2		0.2	0.5	%/V	

Note 1: Supply current when output is high is typically 1.0 mA less.
Note 2: Tested at V_{CC} = 5V and V_{CC} = 15V.
Note 3: This will determine the maximum value of R_A + R_B for 15V operation. The maximum total R = 10 megohms, and for 5V operation, the maximum R = 3.4 megohms.
Note 4: Matching characteristics refer to the difference between performance characteristics of each timer section.

Micropower Dual Timer

GENERAL DESCRIPTION

The XR-L556 dual timer contains two independent micropower timer sections on a monolithic chip. It is a direct replacement for the conventional 556-type dual timers, for applications requiring very low power dissipation. Each section of the XR-L556 dual timer is equivalent to Exar's XR-L555 micropower timer. The circuit dissipates only 1/15th of the stand-by power of conventional dual timers and can operate down to 2.5 volts without sacrificing such key features as timing accuracy and stability. At 5 volt operation, typical power dissipation of the dual-timer circuit is less than 2 mW; and it can operate in excess of 500 hours with only two 300 mA-Hr NiCd batteries.

The two timer sections of the circuit have separate controls and outputs, but share common supply and ground terminals. Each output can source up to 100 mA of output current or drive TTL circuits.

FEATURES

Replaces two XR-L555 Micropower Timers
Pin Compatible with Standard 556-Type Dual Timer
Less than 1 mW Power Dissipation per Section (V_{CC} = 5V)
Timing from Microseconds to Minutes
Over 500-Hour Operation with 2 NiCd Batteries Low Voltage Operation (V_{CC} = 2.5V)
Operates in Both Monostable and Astable Modes
CMOS TTL and DTL Compatible Outputs
Introduces No Switching Transients

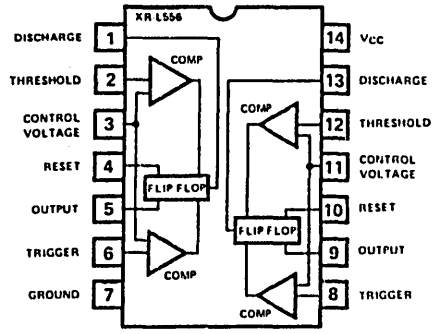
APPLICATIONS

Battery Operated Timing
Micropower Clock Generator
Pulse Shaping and Detection
Micropower PLL Design
Power-On Reset Controller
Micropower Oscillator
Sequential Timing
Pulse-Width Modulation
Appliance Timing
Remote-Control Sequencer

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L556 M	Ceramic	−55°C to +125°C
XR-L556 CN	Ceramic	0°C to +70°C
XR-L556 CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-L556 is a micropower version of the industry standard XR-556 timing circuit, capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage, which may range from 2.5 V to 15 V. The output stage can source 100 mA. Each timer section is fully independent and similar to the XR-L555.

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operation (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, which produces a timing interval of 1.1 RC. As the reference is related to V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-L556 is high during the timing interval. It is triggered and reset on falling waveforms. The control voltage inputs (Pins 3 and 11) may serve as pulse width modulation points.

XR-L556

ELELTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°DC, V_{CC} = +5V, unless otherwise specified)

PARAMETERS	XR-L556M			XR-L556C			UNITS	CONDITION
	MIN	TYP	MAX	MIN	TYP	MAX		
Supply Voltage	2.5		15	2.7		15	V	
Supply Current (Each Timer Section) Total Supply Current (Both Timer Sections)		150 300	300 600		200 400	500 1000	 μA μA	Low State Output V_{CC} = 5V, R_L = ∞
Timing Error Initial Accuracy Drift with Temperature Drift with Supply Voltage		 0.5 50 0.5	 200 		 1.0 50 0.5	 	 % ppm/°C %/V	R_A, R_B = 1 KΩ to 100 KΩ C = 0.1 μF 0°C ≤ T_A ≤ 70°C Monostable Operation
Threshold Voltage		2/3			2/3		X V_{CC}	
Trigger Voltage	1.45 4.8	1.67 5.0	1.9 5.2		1.67 5.0		V V	V_{CC} = 5V V_{CC} = 15V
Trigger Current		20			20		nA	
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V	
Reset Curerent		10			10		μA	
Threshold Current		10	50		20	100	nA	
Control Voltage Level	2.90 9.6	3.33 10.0	3.80 10.4	2.60 9.0	3.33 10.0	4.00 11.0	V V	V_{CC} = 5V V_{CC} = 15V
Output Voltage Drop (Low)		0.1	0.3		0.15	0.35	V	I_{sink} = 1.5 mA
Output Voltage Drop (High)	 3.0 13	 3.3 13.3 12.5	 	 2.75 12.75	 3.3 13.3 12.5	 	 V V V	I_{source} = 10mA V_{CC} = 5V V_{CC} = 15V I_{source} = 100 mA V_{CC} = 15V
Rise Time of Output		200			200		nsec	
Fall Time of Output		100			100		nsec	
Discharge Transistor Leakage		0.1			0.1		μA	

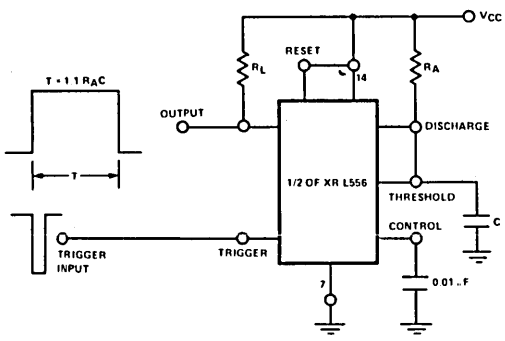


Figure 1. Monostable (One-Shot) Circuit

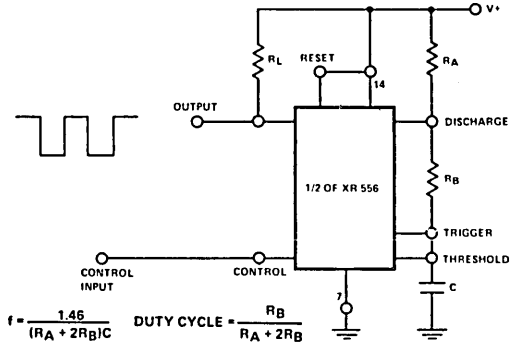


Figure 2. Astable (Free-Running) Circuit

CHARACTERISTIC CURVES

GENERAL CHARACTERISTICS

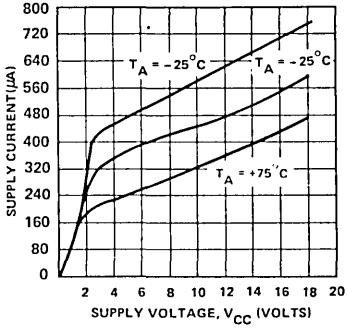


Figure 3. Total Supply Current as a Function of Supply Voltage

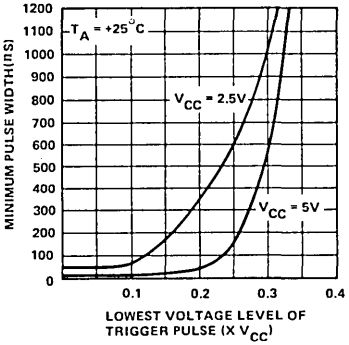


Figure 4. Minimum Pulse-Width Required for Triggering

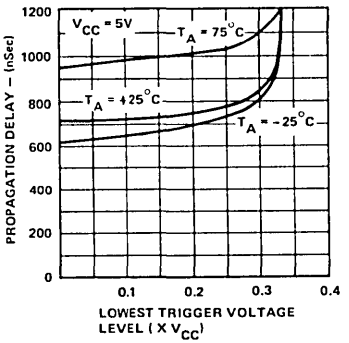


Figure 5. Propagation Delay as a Function of Voltage Level of Trigger Pulse

MONOSTABLE OPERATION

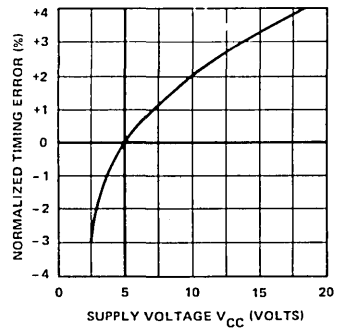


Figure 6. Typical Timing Accuracy as a Function of Supply Voltage

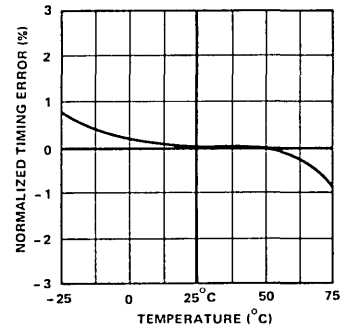


Figure 7. Typical Timing Accuracy as a Function of Temperature (V_{CC} = 5V, R_A = 100KΩ, C = 0.01μF)

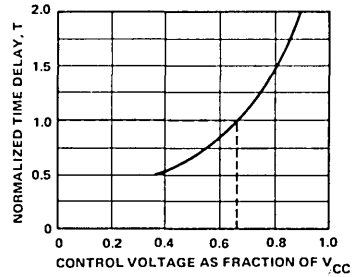


Figure 8. Normalized Time Delay as a Function of Control Voltage

ASTABLE OPERATION

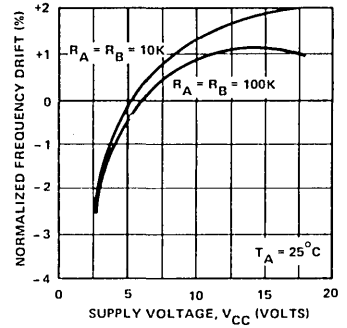


Figure 9. Typical Frequency Stability as a Function of Supply Voltage

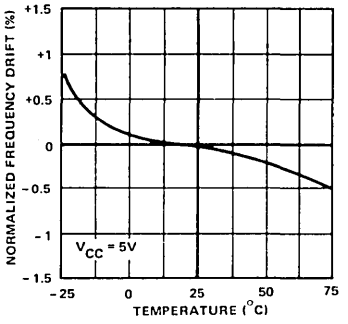


Figure 10. Typical Frequency Stability as a Function of Temperature ($R_A = R_B$ = 10KΩ, C = 0.1μF)

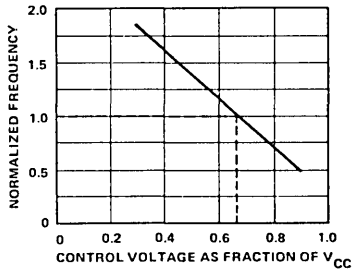


Figure 11. Normalized Frequency of Oscillation as a Function of Control Voltage

XR-L556

FEATURES OF XR-L556

The XR-L556 micropower dual timer is, in most instances, a direct pin-for-pin replacement for the conventional 556-type dual timer. However, compared to conventional 556-timer, it offers the following important performance features:

Reduced Power Dissipation: The current drain is 1/15th of the conventional 556-type dual timer.

No Supply Current Transients: The conventional 556-timer can produce 300 to 400 mA of supply current spikes during switching of either one of its timer sections. The XR-L556 is virtually transient-free as shown in Figure 12.

Low-Voltage Operation: The XR-L556 operates down to 2.7 volts of supply voltage, vs. 4.5V minimum operating voltage needed for conventional 556-timer. Thus, the XR-L556 can operate safely and reliably with two 1.5V NiCd batteries.

Proven Bipolar Technology: The XR-L556 is fabricated using conventional bipolar process technology. Thus, it is immune to electrostatic burn-out problems associated with low-power timers using CMOS technology.

PRINCIPLES OF OPERATION

MONOSTABLE (ONE-SHOT) OPERATION

The circuit connection for monostable, or one-shot operation is one of the timer sections of the XR-L556 is shown in Figure 1. The internal flip-flop is triggered by lowering the trigger level to less than 1/3 of V_{CC}. The circuit triggers on a negative-going slope. Upon triggering, the flip-flop is set, which releases the short circuit across the capacitor and also moves the output level toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_A C$. A comparator is referenced to 2/3 V_{CC} with the use of three equal internal resistors. When the voltage across the capacity reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, the output level moves toward ground and the timing cycle is completed. The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

$$T = 1.1\ R_A C$$

This time delay varies linearly with the choice of R_A and C as shown by the timing curves of Figure 13. For proper operation of the circuit, the trigger pulse-width *must be* less than the timing period.

Once the circuit is triggered it is immune to additional trigger inputs until the present period has been completed. The timing-cycle can be interrupted by using the reset control. When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged

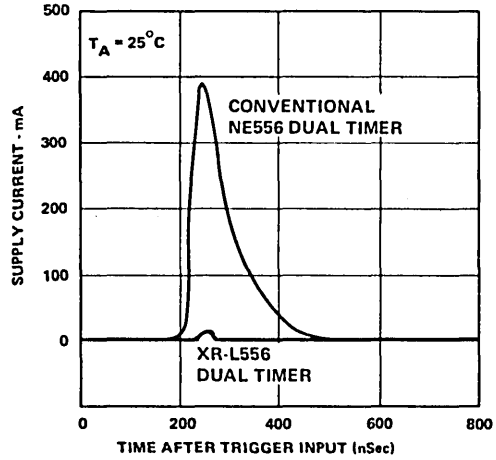


Figure 12. Comparison of Supply Current Transient of Conventional NE556 Dual Timer with XR-L556 Micropower Dual Timer

i.e. "low". The reset pin should be connected to $+V_{CC}$ when not used to avoid the possibility of false triggering.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 2. The external capacitor charges to 2/3 V_{CC} through the series combination of R_A and R_B, and discharges to 1/3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with an exponential waveform. The output level at pin 5 (or 9) is high during the charging cycle, and goes low during the discharge cycle. The charge and the discharge times are independent of supply voltage. The oscillations can be keyed "on" and "off" using the reset controls (pin 4 or 10).

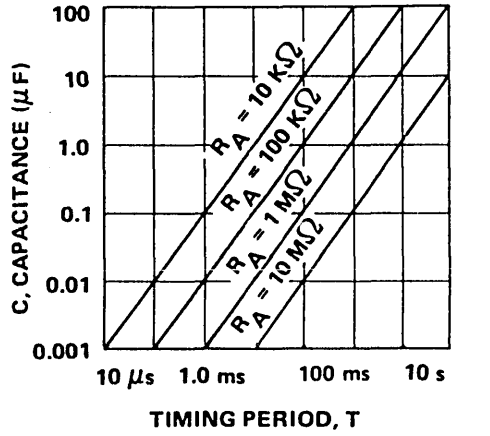


Figure 13. Timing Period, T, as a Function of External R-C Network

The charge time (output high) is given by:

$$t_1 = 0.695\ (R_A + R_B)C$$

The discharge time (output low) by:

$$t_2 = 0.695\ (R_B)C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\ ((R_A + 1R_B)C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \text{ and}$$

may be easily found as shown in Figure 14.

The duty cycle D, is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

APPLICATIONS INFORMATION

INDEPENDENT TIME DELAYS

Each timer section of the XR-L556 can operate as an independent timer to generate a time delay, T, set by the respective external timing components. Figure 15 is a circuit connection where each section is used separately in the monostable mode to produce respective time delays of T_1 and T_2, where:

$$T_1 = 1.1\ R_1C_1 \text{ and } T_2 = 1.1\ R_2C_2$$

SEQUENTIAL TIMING (DELAYED ONE-SHOT)

In this application, the output of one timer section (Timer 1) is capacitively coupled to the trigger terminal of the second, as shown in Figure 16. When Timer 1 is triggered at pin 6, its output at pin 5 goes "high" for a time duration $T_1 = 1.1\ R_1C_1$. At the end of this timing cycle, pin 5 goes "low" and triggers Timer 2 through the capacitive coupling, C_C, between pins 5 thru 8. Then, the output at pin 9 goes "high" for a time duration

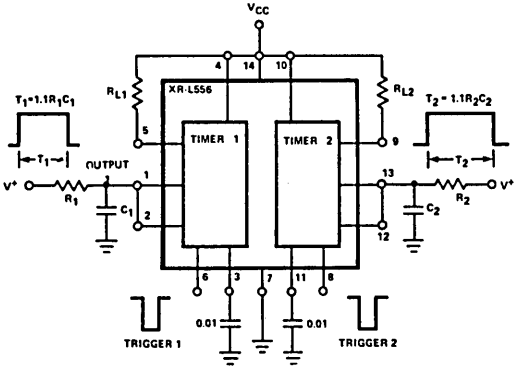


Figure 15. Generation of Two Independent Time Delays

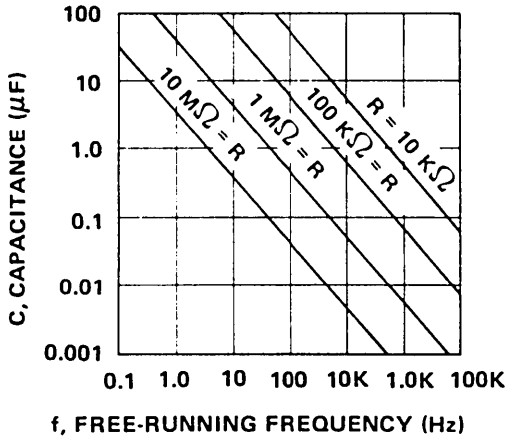


Figure 14. Free Running Frequency as a Functionof External Timing Components (Note: $R = R_A + 2R_B$)

$T_2 = 1.1\ R_2C_2$. In this manner, the unit behaves as a "delayed one-shot" where the output of Timer 2 is delayed from the initial trigger at pin 6 by a time delay of T_1

KEYED OSCILLATOR

One of the timer sections of the XR-L556 can be operated in its free-running mode, and the other timer section can be used to key it "on" and "off". A recommended circuit connection is shown in Figure 17. Timer 2 is used as the oscillator section, and its frequency is set by the resistors R_A, R_B and the capacitor C_2. Timer 1 is operated as a monostable circuit, and its output is connected to the reset terminal (pin 10 of Timer 2).

When the circuit is at rest, the logic level at the output of Timer 1 is "low"; and the oscillations of Timer 2 are inhibited. Upon application of a trigger signal to Timer 1, the logic level at pin 1 goes "high" and the oscillator section (Timer 2) is keyed "on". Thus, the output of Timer 2 appears as a tone burst whose frequency is set by R_A, R_B and C_2, and whose duration is set by R_1 and C_1 of Figure 17.

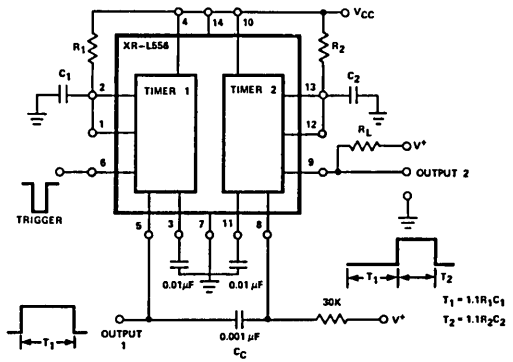


Figure 16. Sequential Timing

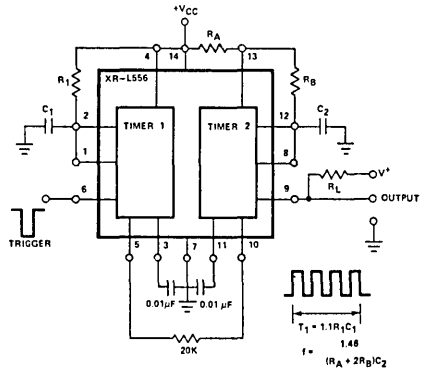


Figure 17. Keyed Oscillator

FREQUENCY DIVIDER AND PULSE SHAPER

If the frequency of the input is known, each timer section of the XR-L556 can be used as a frequency divider by adjusting the length of its timing cycle. If the timing interval T_1 (= 1.1 R_1C_1) is larger than the period of the input pulse trigger, then only those input pulses which are spaced more than 1.1 R_1C_1 will actually trigger the circuit.

The output frequency is equal to (1/N) times the input frequency. The division factor N is in the range:

$$\frac{T}{T_P} - 1 < N < \frac{T}{T_P}$$

where T_P is the period of the input pulse signal.

Since the two timer sections of the XR-L556 are electrically independent, each can be used as a frequency divider. Thus, if the trigger terminals of both timer sections are connected to a common input, the XR-L556 can produce two independent outputs at frequencies f_1 and f_2:

$$f_1 = f_2/N_1 \text{ and } f_2 = f_2 = f_S/N_2$$

Where N_1 and N_2 are the division factors for respective timer sections, set by external resistors and capacitors at pins (1, 2) and (12, 13).

Frequency division can be performed by 1/2 of the XR-L556. The remaining timer section can be used as a "pulse-shaper" to adjust the duty cycle of the output waveform. As seen in Figure 18, Timer 1 is used as the frequency divider section and Timer 2 is used as the pulse shaper.

The output of Timer 1 (pin 5) triggers Timer 2, which produces an output pulse whose frequency is the same as the output frequency of Timer 1, and whose duty cycle is controlled by the timing resistor and capacitor of Timer 2. The duty cycle of the output of Timer 2 (pin 9) can be adjusted from 1% to 99% by varying the value of R_2.

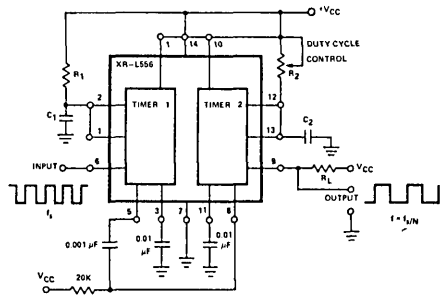


Figure 18. Frequency Divider and Pulse-Shaper

MICROPOWER OSCILLATOR WITH INDEPENDENT FREQUENCY AND DUTY CYCLE ADJUSTMENT

If Timer 1 is operated in its astable mode and Timer 2 is operated in its monostable mode, as shown in Figure 19, then an oscillator with fixed frequency and variable duty cycle results.

Timer 1 generates a basic periodic waveform that is then used to trigger Timer 2. If the time delay, T_2, of Timer 2 is chosen to be less than the period of oscillations of Timer 1, then the output at pin 9 has the same frequency as Timer 1, but has its duty cycle determined by the timing cycle of Timer 2. The output duty cycle can be adjusted over a wide range (from 1% to 99%) by adjusting R_2.

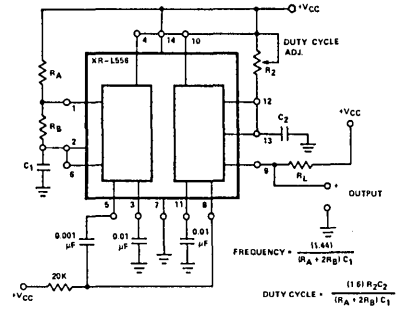
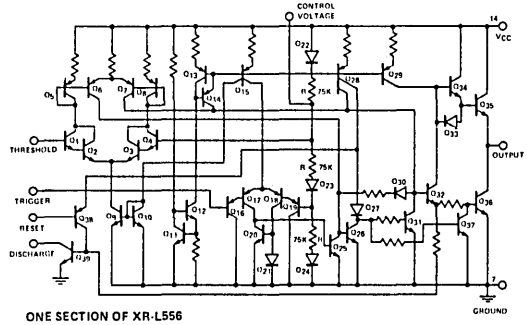


Figure 19. Micropower Oscillator with Fixed Frequency and Variable Duty-Cycle



EQUIVALENT SCHEMATIC DIAGRAM

Quad Timing Circuits

GENERAL DESCRIPTION

The XR-558 and the XR-559 quad timing circuits contain four independent timer sections on a single monolithic chip. Each of the timer sections on the chip are entirely independent, and each one can produce a time delay from microseconds to minutes, as set by an external R-C network. Each timer has its separate trigger terminal, but all four timers in the IC package share a common reset control.

Both the XR-558 and the XR-559 quad timer circuits are "edge-triggered" devices, so that each timer section can be cascaded, or connected in tandem, with other timer sections, without requiring coupling capacitors.

The XR-558 is designed with open-collector outputs; each output can sink up to 100 mA. The XR-559 is designed with emitter-follower outputs. Each output can source up to 100 mA of load current. The outputs are normally at "low" state, and go to "high" state during the timing interval.

FEATURES

Four Independent Timer Sections
High Current Output Capability
  XR-558: 100 mA sinking capability/output
  XR-559: 100 mA sourcing capability/output
Edge Triggered Controls
Output Stage Independent of Trigger Condition
Wide Supply Range: 4.5 V to 16 V

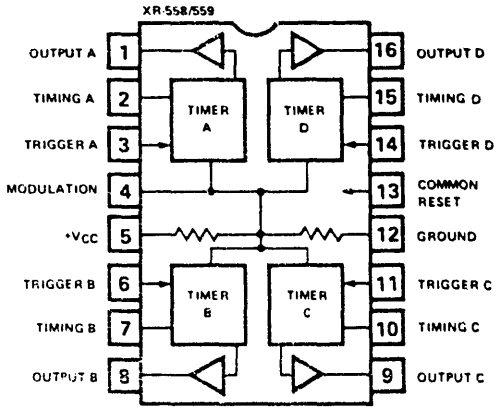
APPLICATIONS

Precision Timing
Pulse Shaping
Clock Synchronization
Appliance Timing

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25"	6 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25"C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-558M	Ceramic	−55°C to +125°C
XR-558CN	Ceramic	0°C to +70°C
XR-558CP	Plastic	0°C to +70°C
XR-559M	Ceramic	−55°C to +125°C
XR-559CN	Ceramic	0°C to +70°C
XR-559CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-558 and XR-559 are easy to use quad timers capable of operation with supply voltages between 4.5 V and 18 V. Each section has independent timing and triggering, and can operate over intervals ranging from the low microseconds up through several minutes. The devices are triggered on falling waveforms and are immune to long trigger pulses. When the reset pin (Pin 13) is held below 0.8 V, all four outputs are set low and all triggers are disabled. Timing period accuracy is typically better than 1%, independent of V_{CC}, and drift is better than 150 ppm/°C and 0.5%/V. The timing period, in seconds, equals R times C.

The XR-558 features open collector outputs, capable of sinking 100 mA, that are driven low during the timing interval. The XR-559 has emitter followers, active upon timeout, capable of sourcing 100 mA. The XR-558 sinks load current from $+V_{CC}$, the XR-559 sources load current to ground.

ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise noted.)

	XR-558M/XR-559M			XR-558C/XR-559C				
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Supply Voltage	4.5		18	4.5		16	V	
Supply Current								V_{CC} = V_{RESET} = 15V
XR-558 Family		21	32		27	36	mA	Outputs Open
XR-559 Family		9	16		12	18	mA	Outputs Open
Timing Accuracy								R = 2 kΩ to 100 kΩ
Initial Accuracy		1	3		2		%	C = 1 μF
Drift with Temperature		150			150		ppm/°C	
Drift with Supply Voltage		0.1			0.1		%/V	
Trigger Characteristics								See Note: 1
Trigger Voltage	0.8	1.5	2.4	0.8	1.5	2.4	V	V_{CC} = 15V
Trigger Current		5	30		10	100	μA	$V_{TRIGGER}$ = 0V
Reset Characteristics								
Reset Voltage	0.8	1.5	2.4	0.8	1.5	2.4	V	See Note: 2
Reset Current		50	300		50		μA	
Threshold Characteristics								Measured at Timing Pins
Threshold Voltage		0.63			0.63		X V_{CC}	(Pins 2, 7, 10 or 15)
Threshold Leakage		15			15		nA	
XR-558 Output Characteristics								See Note: 3
Output Voltage		0.1	0.2		0.1	0.4	V	I_L = 10 mA
Output Voltage		0.7	1.5		1.0	2.0	V	I_L = 100 mA
Output Leakage		10			10		nA	Output High Condition
XR-559 Output Characteristics								See Note: 4
Output Voltage	13	13.6		12.5	13.3		V	I_L = 10 mA, V_{CC} = 15V
Output Voltage	12.5	13.3		12.0	13.0		V	I_L = 100 mA, V_{CC} = 15V
Propagation Delay								
XR-558 Family		1.0			1.0		μsec	
XR-559 Family		0.4			0.4		μsec	
Output Rise-time		100			100		nsec	I_L = 100 mA
Output Fall-time		100			100		nsec	I_L = 100 mA

NOTES:

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The XR-558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.
4. The XR-559 output structure is a darlington emitter follower which requires a pull down resistor to ground to source current. The output is normally low and sources current only when switched high.

DESCRIPTION OF CIRCUIT OPERATION

The XR-558/559 quad timing circuits are designed to be used in timing applications ranging from few microseconds up several hours. They provide cost-effective alternative to single-timer IC's in applications requiring a multiplicity of timing or sequencing functions.

Each quad-timer circuit contains four independent timer sections, where each section can generate a time delay set by its own resistor and capacitor, external to the IC. All four timing sections can be used simultaneously, or can be interconnected in tandem, for sequential timing applications. For astable operation, two sections of the quad-timer IC can be interconnected to provide an oscillator circuit whose duty-cycle can be adjusted from close to zero, to nearly 100%.

The generalized test and evaluation circuit for both the XR-558 and the XR-559 quad timer circuits is shown in Figure 1. Note that, the only difference between the two circuit types is the structure of the output circuitry.

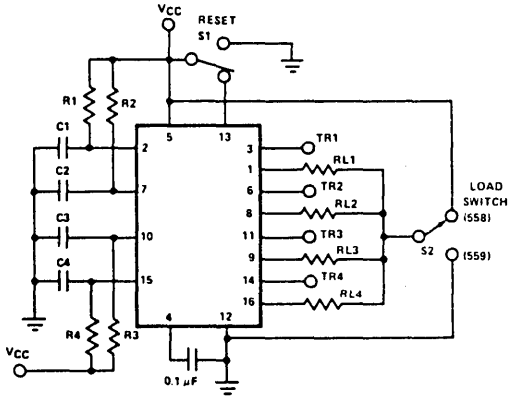


Figure 1. Generalized Test and Evaluation Circuit for XR-558/ XR-559 Quad Timer Circuits

MONOSTABLE OPERATION

In the monostable, or one-shot mode of operation, it is necessary to supply two external components, a resistor and a capacitor, for each section of the timer IC. The timing terminals of those timer-sections not being used can be left open-circuited. The time period is equal to the external RC product. A plot of the timing period, T, as a function of the external R-C combination is shown in Figure 2.

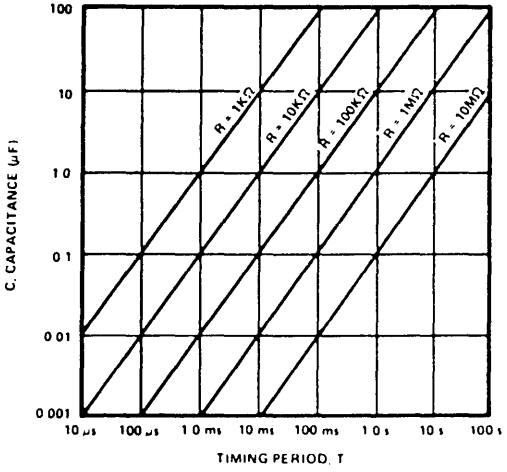


Figure 2. Timing Period, T, as a Function of External R-C Combination (Note: T = 1.0 RC)

ASTABLE OPERATION

For astable, or free-running, operation of the quad timer circuits, it is desirable to cross-couple two of the timer sections on the chip, as shown in Figure 3. In this circuit configuration, the outputs of each section are direct-coupled to the opposite trigger input. Thus, the "high" and "low" half-periods of the output can be set by the external R-C products, as R_1C_1 and R_2C_2, respectively. The frequency of oscillation, and the output duty-cycle are given as:

The frequency of oscillation can be externally controlled by applying a control-voltage to the control terminal (pin 4). Since the control terminal is common to all the timer sections, the duty cycle of the output waveform is not effected by the modulation voltage; thus the circuit can function as a variable-frequency, fixed duty-cycle oscillator.

The frequency of oscillation increases as the voltage at the control terminal (pin 4) is lowered below its open-circuit value.

$$\text{Frequency of Oscillation} = \frac{1}{R_1 C_1 + R_2 C_2}$$

$$\text{Output Duty-Cycle} = \frac{R_2 C_2}{R_1 C_1 + R_2 C_2}$$

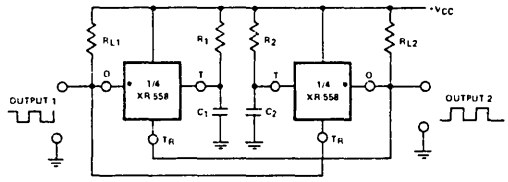


Figure 3. Typical Circuit Connection for Astable Operation Using Two Timer-Sections. (Note: For XR-559, R_{L1} and R_{L2} are Connected from Outputs to Ground.)

OUTPUT STRUCTURE

The XR-558 family of quad timers have "open-collector" NPN-type output stages. Each output can individually sink up to 100 mA of load current. However, with more than one output active, the total current capability is limited by the power-dissipation rating of the IC package (see Absolute Maximum Ratings). In the normal operation of the circuit, each output will require a pull-up resistor to $+V_{CC}$. The output is normally "low" state (i.e. sinking current) when the timer is at reset; and goes to "high" state during the timing cycle.

The XR-559 family of quad timers have Darlington NPN "emitter-follower" type outputs. Each output can source up to 100 mA, during its "high" state. The total amount of output current, available from all outputs, is limited by the package power dissipation rating. For normal operation of the circuit, a pull-down resistor is required from each output to ground. The output of XR-559 is normally low (i.e. at "off-state"), and goes to "high" state when the circuit is triggered.

TRIGGER INPUTS

Each timer section of the quad-timer IC's has its own trigger input. The trigger level is set at nominally +1.5 V, and the trigger input is *edge-triggered* on the falling edge of an input trigger pulse. In other words, for proper triggering, the trigger signal must first go "high" and then go "low". If both the trigger and the reset controls are activated, the reset control overrides the trigger input.

RESET INPUT

The reset control (pin 13) is common to all four timer section and resets all of the timer sections simultaneously.

The reset voltage must be brought below 0.8 V to insure reset condition. When reset is activated, all the outputs go to "low" state. While the reset is active, the trigger inputs are inhibited. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

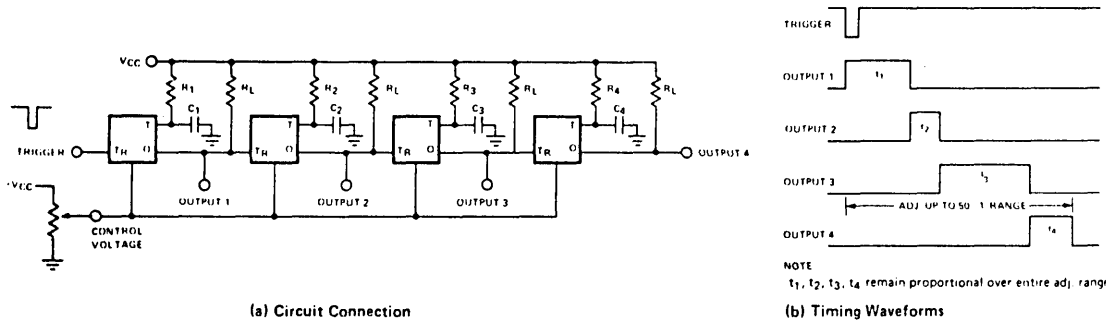
CONTROL VOLTAGE

The control voltage terminal (pin 4) is common to all four timer sections of the XR-558 or the XR-559. This terminal allows the internal threshold voltages of all four timer sections to be modulated, and thus provides the control of the pulse-width or the duty-cycle of the output waveforms. The range of this control voltage is from 0.5 V to $+V_{CC}$ minus 1 Volt. This range provides an over-all timing variation of approximately 50:1. Since the time period of each timer section is proportional to the control voltage, all four timing periods can be simultaneously varied, and their relative ratios remain unchanged over the adjustment range.

APPLICATIONS EXAMPLE

Sequential Timer:

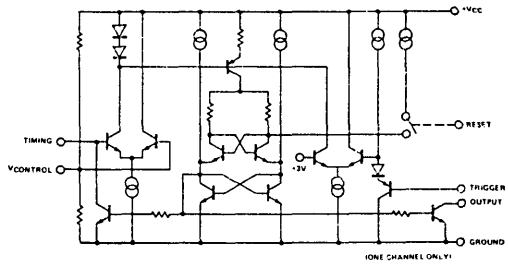
Figure 4 shows a typical application for the quad-timer in sequential timing application. For illustration purposes, the XR-558 is used in the example. Note that, when triggered, the circuit produces four sequential time delays, where the duration of each output is independently controlled by its own R-C time constant. Yet, all four outputs can be modulated over a 50:1 range, and remain proportional over this entire range. Since each timer section is edge-triggered, the sections can be cascaded by direct coupling of respective outputs and trigger inputs.



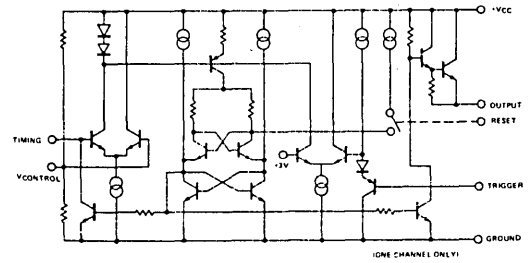
(a) Circuit Connection

(b) Timing Waveforms

Figure 4. Using the XR-558 as a Four-Stage Sequential Timer with Voltage Control Capability



XR-558 EQUIVALENT SCHEMATIC



XR-559 EQUIVALENT SCHEMATIC

Dual Timing Circuit

GENERAL DESCRIPTION

The XR-2556 dual timing circuit contains two independent 555-type timers on a single monolithic chip. Each timer section is a highly stable controller capable of producing accurate time delays or oscillations. Independent output and control terminals are provided for each section as shown in the functional block diagram.

In the monostable mode of operation, the time delay for each section is precisely controlled by one external resistor and one capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle of each section are accurately controlled with two external resistors and one capacitor.

The XR-2556 may be triggered or reset on falling waveforms. Each output can source or sink up to 200 mA or drive TTL circuits. The matching and temperature tracking characteristics between each timer section of the XR-2556 are superior to those available from two separate timer packages.

FEATURES

Replaces Two 555-Type Timers
TTL Compatible Pinouts (Gnd—Pin 7, V_{CC}—Pin 14)
Timing from Microseconds Thru Hours
Excellent Matching Between Timer Sections
Operates in Both Monostable and Astable Modes
High Current Drive Capability (200 mA each output)
TTL and DTL Compatible Outputs
Adjustable Duty Cycle
Temperature Stability of 0.005%/°C
Normally ON and Normally OFF Outputs

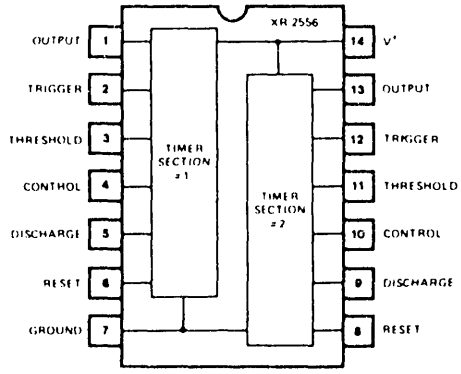
APPLICATIONS

Precision Timing
Pulse Generation
Sequential Timing
Pulse Shaping
Time Delay Generation
Clock Pattern Generation
Missing Pulse Detection
Pulse-Width Modulation
Frequency Division
Clock Synchronization
Pulse-Position Modulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation	
Ceramic Dual-In-Line	750 mW
Derate above T_A = 25°C	5 mW/°C
Plastic Dual-In-Line	625 mW
Derate above T_A = 25°C	5 mW/°C
Storage Temperate Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2556M	Ceramic	−55°C to +125°C
XR-2556CN	Ceramic	0°C to +70°C
XR-2556CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2556 is a high output dual timing circuit similar to the popular 555-type timer, capable of both monostable and astable operation with timing intervals ranging from low microseconds up through several hours. Timing is independent of supply voltage, which may range from 4.5 V to 18 V. The output stage can source or sink 200 mA. Each timing section is fully independent.

In the monostable (one shot) mode, timing is determined by one resistor and capacitor. Astable operation (oscillation) requires an additional resistor, which controls duty cycle. An internal resistive divider provides a reference voltage of 2/3 V_{CC}, which produces a timing interval of 1.1 RC. As the reference is related to V_{CC}, the interval is independent of supply voltage; however, for maximum accuracy, the user should ensure V_{CC} does not vary during timing.

The output of the XR-2556 is high during the timing interval and pulls low at timeout. It is triggered and reset on falling waveforms. The control voltage inputs (Pins 4 and 10) may serve as pulse width modulation points. Matching between sections is typically better than 0.2% initially with temperature drift tracking to ±10 ppm/°C.

For low voltage and/or low power drain applications consider the XR-L556.

XR-2556

ELECTRICAL CHARACTERISTICS

Test Conditions: (Each timer section, T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified.)

PARAMETERS	XR-2556M			XR-2556C			UNITS	FIGURE	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
Supply Voltage	4.5		18	4.5		16	V	7	
Supply Current (Each Timer Section)		3 10	5 12		3 10	6 15	mA mA	7	Low State Output, Note 1 V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞
Total Supply Current (Both Timer Sections)		6 20	10 24		6 20	12 30	mA mA	7	Low State Output V_{CC} = 5V, R_L = ∞ V_{CC} = 15V, R_L = ∞
Timing Error Initial Accuracy Drift with Temperature Drift with Supply Voltage		0.5 30 0.05	2.0 100 0.1		1.0 50 0.05		% ppm/°C %/V	 13 12	R_A, R_B = 1 kΩ to 100kΩ Note 2, C = 0.1 μF
Threshold Voltage		2/3			2/3		x V_{CC}		
Trigger Voltage	1.45 4.8	1.67 5.0	1.9 5.2		1.67 5.0		V V	6	V_{CC} = 5V V_{CC} = 15V
Trigger Current		0.5			0.5		μA		
Reset Voltage	0.4	0.7	1.0	0.4	0.7	1.0	V		
Reset Current		0.1			0.1		mA		
Threshold Current		0.1	0.25		0.1	0.25	μA		Note 3
Control Voltage Level	2.90 9.6	3.33 10.0	3.80 10.4	2.60 9.0	3.33 10.0	4.00 11.0			V_{CC} = 5V V_{CC} = 15V
Output Voltage Drop (Low)		 0.10 0.1 0.4 2.0 2.5	 0.25 0.15 0.5 2.2		 0.25 0.1 0.4 2.0 2.5	 0.35 0.25 0.75 2.5	 V V V V V V	 9 11	 V_{CC} = 5V I_{sink} = 8.0 mA I_{sink} = 5.0 mA V_{CC} = 15V I_{sink} = 10 mA I_{sink} = 50 mA I_{sink} = 100 mA I_{sink} = 200 mA
Output Voltage Drop (High)	 3.0 13	 3.3 13.3 12.5		 2.75 12.75	 3.3 13.3 12.5		 V V V	8	 I_{source} = 100 mA V_{CC} = 5V V_{CC} = 15V I_{source} = 200 mA V_{CC} = 15V
Rise Time of Output		100			100		nsec		
Fall Time of Output		100			100		nsec		
Matching Characteristics Initial Timing Accuracy Timing Drift with Temperature		0.2 ±10	0.6		0.2 ±10		% ppm/°C		Note 4

Note 1: Supply current when output is high is typically 1.0 mA less.
Note 2: Tested at V_{CC} = 5V and V_{CC} = 15V.
Note 3: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20 meg-ohms.
Note 4: Matching characteristics refer to the difference between performance characteristics of each timer section.

PRINCIPLES OF OPERATION

Figure 2 is the functional block diagram for each timer section of the XR-2556. These sections share the same V^+ and ground leads, but have independent outputs and control terminals. Therefore, each timer section can operate independently of the other. The timing cycle of each section is determined by an external resistor-capacitor network.

MONOSTABLE (ONE-SHOT) OPERATION

When operating either timer section of the XR-2556 in the monostable mode, a single resistor and a capacitor are used to set the timing cycle. The discharge and threshold terminals are also interconnected in this mode, as shown in Figure 3.

Referring to Figure 2, monostable operation of the XR-2556 is explained as follows: the external timing capacitor C is held discharged by the internal transistor, T_O. The internal flip-flop is triggered by lowering the trigger levels (pins 2 or 12) to less than 1/3 V_{CC}. The circuit triggers on a *negative-going* slope. Upon triggering, the flip-flop is set to one side, which releases the short circuit across the capacitor and also moves the output level at pins 1 or 13 toward V_{CC}. The voltage across the capacitor, therefore, starts increasing exponentially with a time constant $\tau = R_A$. A high impedance comparator is referenced to 2/3 V_{CC} with the use of three equal interval resistors. When the voltage across the capacitor reaches this level, the flip-flop is reset, the capacitor is discharged rapidly, and the output level moves toward ground, and the timing cycle is completed.

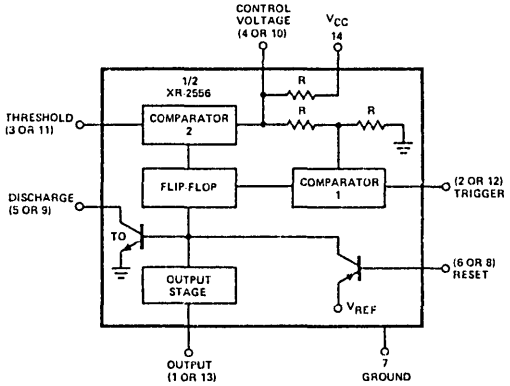


Figure 2. Functional Diagram of One Timer Section

Once the circuit is triggerd it is immune to additional trigger inputs until the present timing-period has been completed. The timing-cycle can be interrupted by using the reset control (pins 6 or 8). When the reset control is "low", the internal discharge transistor is turned "on" and prevents the capacitor from charging. As long as the reset voltage is applied, the digital output level will remain unchanged, i.e. "low". The reset pin should be connected to V^+ when not used to avoid the possibility of false triggering.

Figure 4 shows the waveforms during the monostable timing cycle. The top waveform is the trigger pulse; the

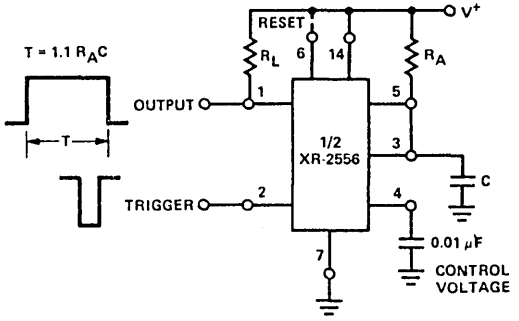


Figure 3. Monostable (One-Shot) Circuit

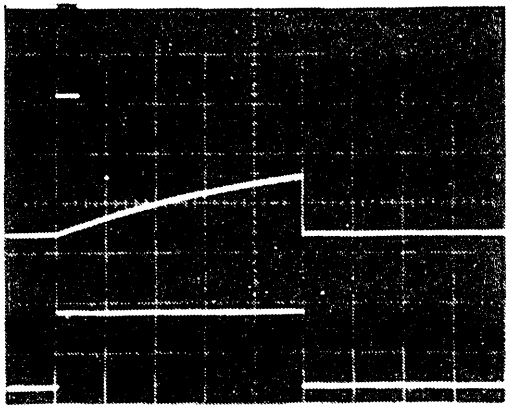


Figure 4. Monostable Waveforms
Top: Trigger Input
Middle: Exponential Ramp across Timing Capacitor
Bottom: Output Logic Level

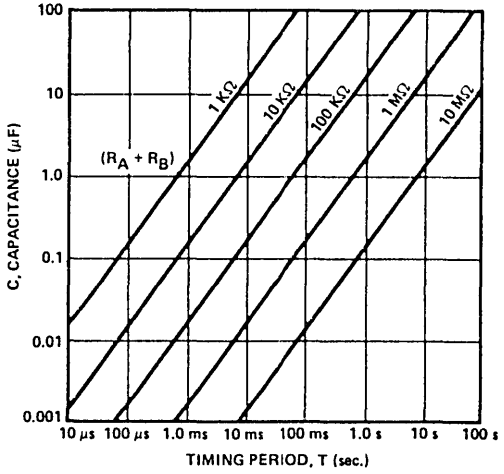


Figure 5. Timing Period, T, as a Function of External R-C Network

TYPICAL CHARACTERISTICS (Each Timer Section)

middle is the exponential ramp across the timing capacitor. The bottom waveform is the output logic state (at pins 1 or 13) during the timing cycle. For proper operation of the circuit, the trigger pulse-width must be less than the timing period.

The duration of the timing period, T, during which the output logic level is at a "high" state is given by the equation:

$$T = 1.1\ R_A C$$

This time delay varies linearly with the choice or R_A and C as shown by the timing curves of Figure 5.

ASTABLE (SELF-TRIGGERING) OPERATION

For astable (or self-triggering) operation, the correct circuit connection is shown in Figure 15. The external capacitor charges to 2/3 V_{CC} through the parallel combination of R_A and R_B, and discharges to 1.3 V_{CC} through R_B. In this manner, the capacitor voltage oscillates between 1/3 V_{CC} and 2/3 V_{CC}, with the exponential waveform as shown in Figure 16. The output level at pin 1 (or 13) is high during the charging cycle, and goes low during the discharge cycle. The charge and the discharge times are independent of supply voltage. The oscillations can be keyed "on" and "off" using the reset controls (pin 6 or 8)

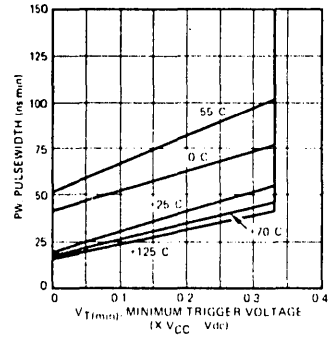


Figure 6. Trigger Pulse Width

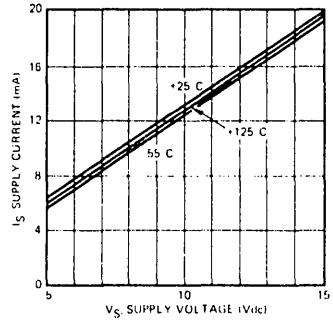


Figure 7. Supply Current (Both Timer Sections)

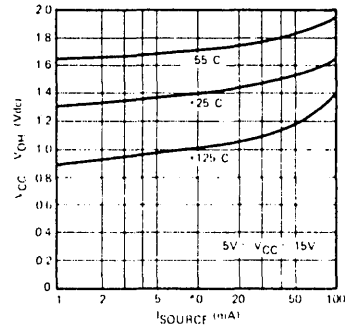


Figure 8. High Output Voltage

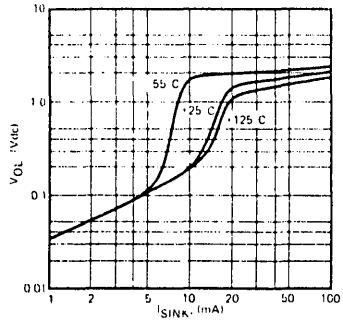


Figure 9. Low Output Voltage
V_{CC} = 5.0 Vdc

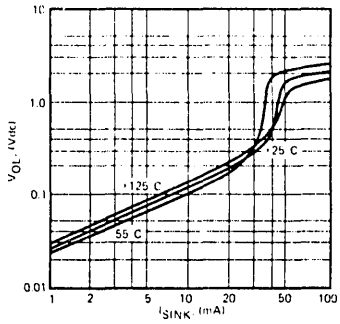


Figure 10. Low Output Voltage
V_{CC} = 10 Vdc

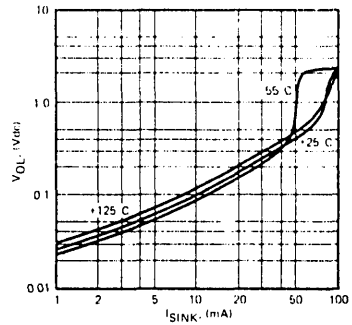


Figure 11. Low Output Voltage
V_{CC} = 15 Vdc

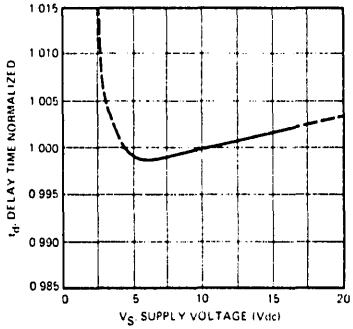


Figure 12. Delay Time vs. Supply Voltage

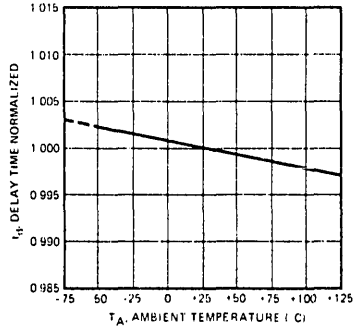


Figure 13. Delay Time vs. Temperature

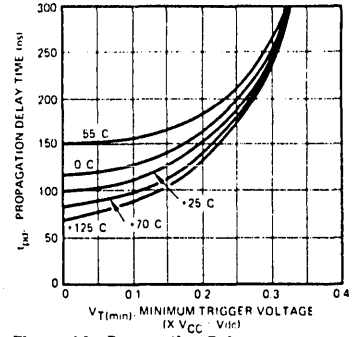


Figure 14. Propagation Delay vs. Trigger Voltage

The charge time (output high) is given by:

$$t_1 = 0.695\,(R_A + R_B)C$$

The discharge time (output low) by:

$$t_2 \approx 0.695\,(R_B)C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\,(R_A + 2R_B)C$$

The frequency of oscillation is then:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \text{ and}$$

may be easily found as shown in Figure 17.

The duty cycle, D, is given by:

$$D = \frac{R_B}{R_A + 2R_B}$$

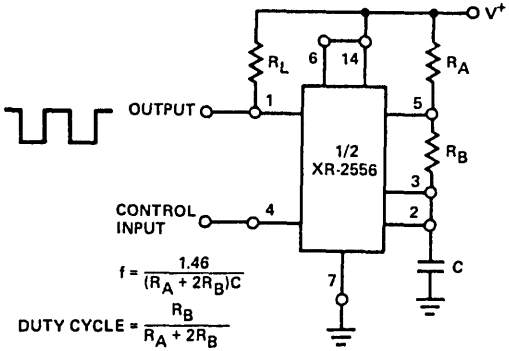


Figure 15. Astable (Free-Running) Circuit

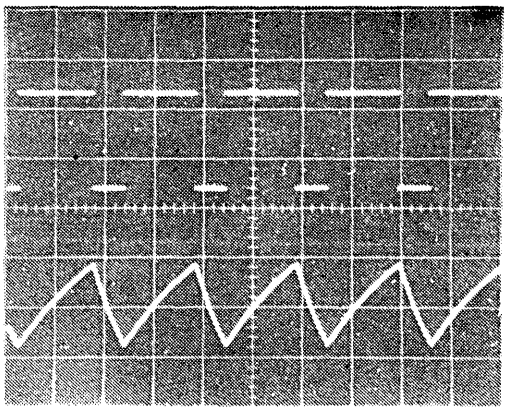


Figure 16. Astable Waveforms
Top: Output Waveform
Bottom: Waveform Across Timing Capacitor

To obtain the maximum duty cycle, R_A must be as small as possible; but it must also be large enough to limit the discharge current (pin 5 current) within the maximum rating of the discharge transistor (200 mA).

DESCRIPTION OF CIRCUIT CONTROLS

OUTPUT (PINS 1 or 13)

The output logic level is normally in a "low" state, and goes "high" during the timing cycle. Each output of the XR-2556 is a "totem pole" type capable of sinking or sourcing 200 mA of load current (see Figure 18).

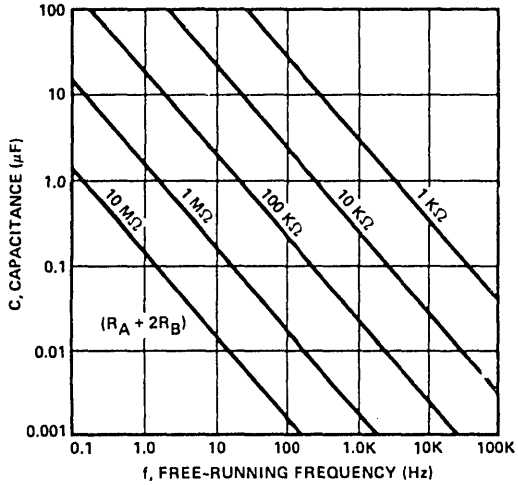


Figure 17. Free Running Frequency as a Function of External Timing Components

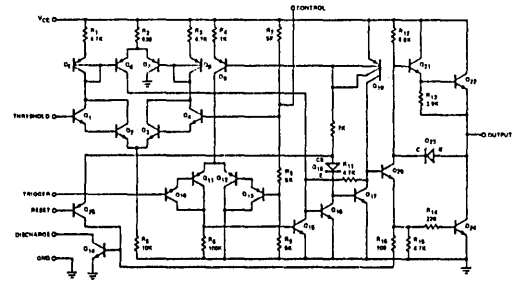


Figure 18. Circuit Schematic—1/2 of XR-2556

TRIGGER (PINS 2 OR 12)

The timing cycle is initiated by lowering the dc level at the trigger terminal below 1/3 V_{CC}. Once triggered, the circuit is immune to additional triggering until the timing cycle is completed.

THRESHOLD (PINS 3 or 11)

The timing cycle is completed when the voltage level at the trigger terminal reaches 2/3 V_{CC}. At this point, Comparator #2 of Figure 2 changes state, resets the internal flip-flop, and initiates the discharge cycle.

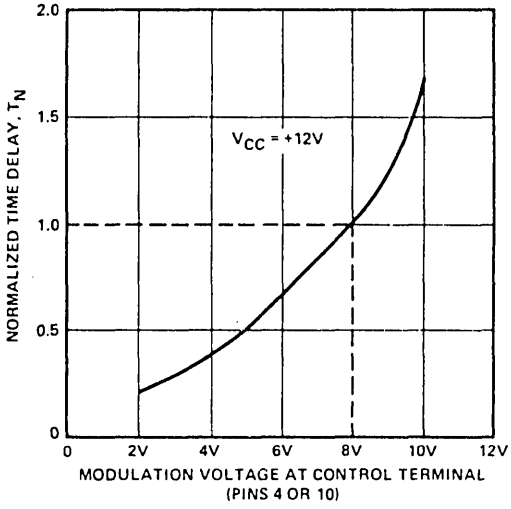


Figure 19. Normalized Time Delay vs. Modulation Voltage

CONTROL OR FM (PINS 4 OR 10)

The timing cycle or the frequency of oscillation can be controlled or modulated by applying a dc control voltage to pin 4 or 10. This terminal is internally biased at 2/3 V_{CC}. The control signal for frequency modulation or pulse-width modulation is applied to this terminal. Figure 19 shows the variation of the timing period, T, as a function of dc voltage at the control terminal. When not in use, the control terminals should be ac grounded through 0.01 μF decoupling capacitors.

DISCHARGE (PINS 5 OR 9)

This terminal corresponds to the collector of the discharge transistor, T_Q, of Figure 2. During the charging cycle, this terminal behaves as an open-circuit; during discharge, it becomes a low impedance path to ground.

RESET (PINS 6 OR 8)

The timing cycle can be interrupted by grounding the reset terminal. When the reset signal is applied, the output goes "low" and remains in that state while the rest voltage is applied. When the reset signal is removed, the output remains "low" until re-triggered. When not used, the reset terminals should be connected to V_{CC} in order to avoid any possibility of false triggering. When the timing circuits are operated in the astable mode, the reset terminals can be used for "on" and "off" keying of the oscillations. (See Figure 22).

APPLICATIONS INFORMATION

INDEPENDENT TIME DELAYS

Each timer section of the XR-2556 can operate as an independent timer to generate a time delay, T, set by the respective external timing components. Figure 20 is a circuit connection where each section is used separately in the monostable mode to produce respective time delays of T_1 and T_2, where:

$$T_1 = 1.1\ R_1C_1 \text{ and } T_2 = 1.1\ R_2C_2$$

SEQUENTIAL TIMING (DELAYED ONE-SHOT)

In this application, the output of one timer section (Timer 1) is capacitively coupled to the trigger terminal of the second, as shown in Figure 21. When Timer 1 is triggered at pin 2, its output at pin 1 goes "high" for a time duration $T_1 = 1.1\ R_1C_1$. At the end of this timing cycle, pin 1 goes "low" and triggers Timer 2 through the capacitive coupling, C_C, between pins 1 and 12. Then, the output at pin 13 goes "high" for a time duration $T_2 = 1.1\ R_2C_2$. In this manner, the unit behaves as a "delayed one-shot" where the output of Timer 2 is delayed from the initial trigger at pin 2 by a time delay of T_1.

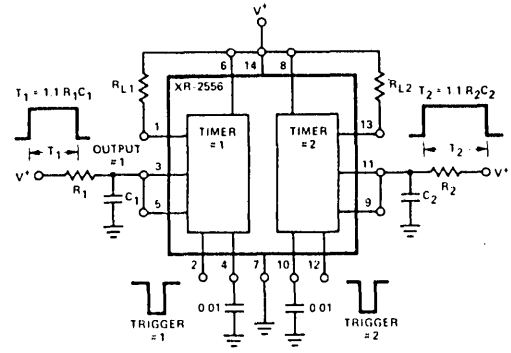


Figure 20. Generation of Two Independent Time Delays

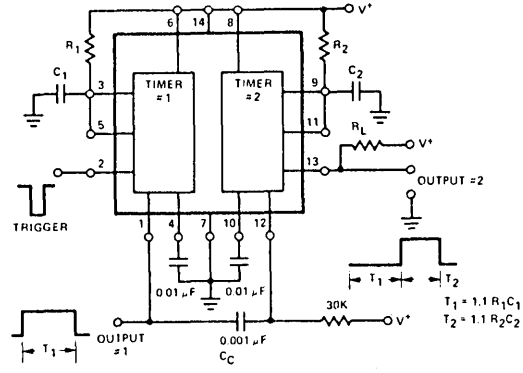


Figure 21. Sequential Timing

KEYED OSCILLATOR

One of the timer sections of the XR-2556 can be operated in its free-running mode, and the other timer section can be used to key it "on" and "off". A recommended circuit connection is shown in Figure 22. Timer 2 is used as the oscillator section, and its frequency is set by the resistors R_A, R_B and the capacitor C_2. Timer 1 is operated as a monostable circuit, and its output is connected to the reset terminal (pin 8) of Timer 2.

When the circuit is at rest, the logic level at the output of Timer 1 is "low"; and the oscillations of Timer 2 are inhibited. Upon application of a trigger signal to Timer 1, the logic level at pin 1 goes "high" and the oscillator section (Timer 2) is keyed "on". Thus, the output of Timer 2 appears as a tone burst whose frequency is set by R_A, R_B and C_2, and whose duration is set by R_1 and C_1 of Figure 22.

FREQUENCY DIVIDER

If the frequency of the input is known, each timer section of the XR-2556 can be used as a frequency divider by adjusting the length of its timing cycle. If the timing interval T_1 ($= 1.1\ R_1C_1$) is larger than the period of the input pulse trigger, then only those input pulses which are spaced more than $1.1\ R_1C_1$ will actually trigger the circuit.

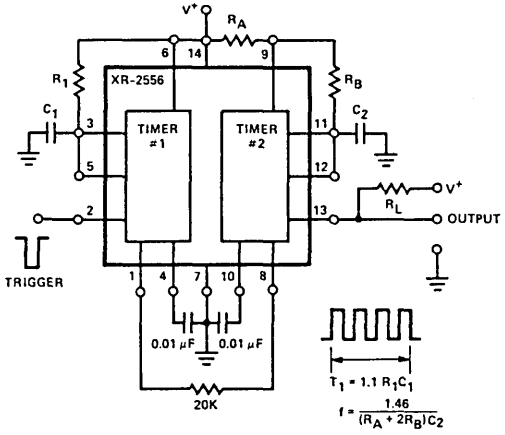


Figure 22. Keyed Oscillator

The output frequency is equal to (1/N) times the input frequency. The division factor N is in the range:

$$\left(\frac{T}{T_P} - 1\right) < N < \frac{T}{T_P}$$

where T_P is the period of the input pulse signal.

Figure 23 shows the circuit waveforms for divide-by-five operation for one of the timer sections of the XR-2556. In this case, the timing period of the circuit is set to be approximately 4.5 times the period of the input pulse.

Since the two timer sections of the XR-2556 are electrically independent, each can be used as a frequency divider. Thus, if the trigger terminals of both timer sections are connected to a common input, the XR-2556 can produce two independent outputs at frequencies f_1 and f_2:

$$f_1 = f_S/N_1 \text{ and } f_2 = f_S/N_2$$

where N_1 and N_2 are the division factors for respective timer sections, set by external resistors and capacitors at pins (3, 5) and (9, 11).

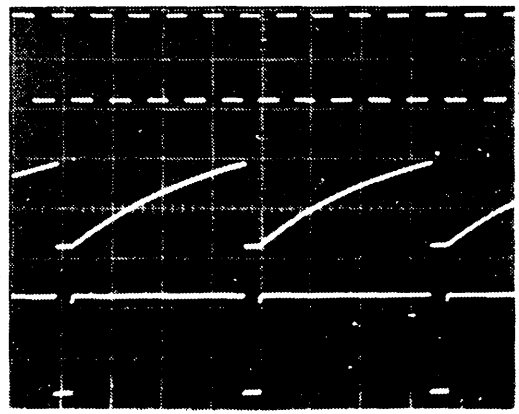


Figure 23. Frequency Divider Waveforms
Top: Input Pulse Train (f = 5 kHz)
Middle: Waveforms Across Timing Capacitor
Bottom: Output Waveform (f = 1 kHz)

FREQUENCY DIVIDER AND PULSE SHAPER

Frequency division can be performed by 1/2 of the XR-2556. The remaining timer section can be used as a "pulse-shaper" to adjust the duty cycle of the output waveform. As seen in Figure 24, Timer 1 is used as the frequency divider section and Timer 2 is used as the pulse-shaper.

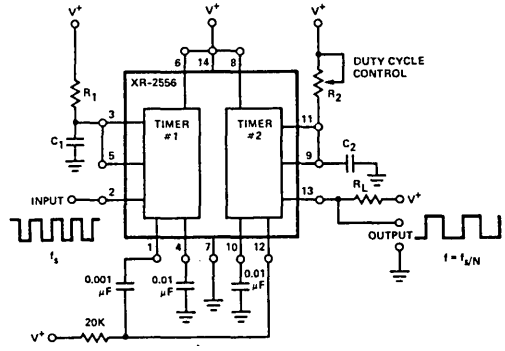


Figure 24. Frequency Divider and Pulse-Shaper

The output of Timer 1 (pin 1) triggers Timer 2, which produces an output pulse whose frequency is the same as the output frequency of Timer 1, and whose duty cycle is controlled by the timing resistor and capacitor of Timer 2. The duty cycle of the output of Timer 2 (pin 13) can be adjusted from 1% to 99% by varying the value of R_2.

Figure 25 shows the circuit waveforms in this application. The top waveform is the input signal of frequency f_S applied to the trigger input (pin 2) of Timer 1. The middle waveform is the output of Timer 1 for divide-by-three operation; and the bottom waveform is the pulse-shaped output obtained from Timer 2 (pin 13).

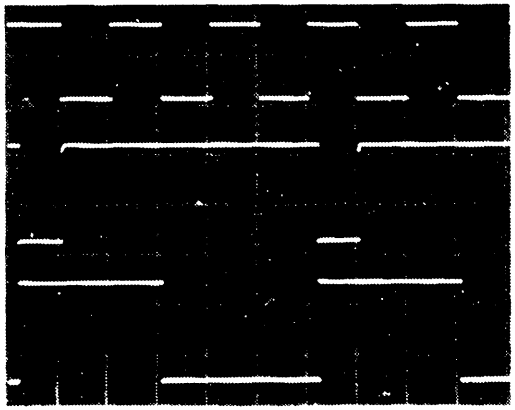


Figure 25. Frequency Divider and Pulse-Shaper Waveforms
Top: Input Signal (f_S = 9 kHz)
Middle: Output at Pin 1 for Divide-by-3
Bottom: Variable Duty Cycle Output at Pin 13

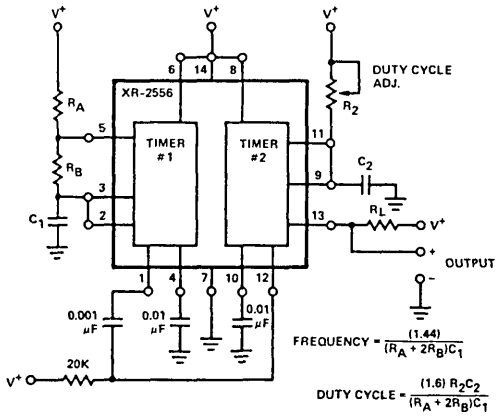


Figure 26. Fixed Frequency Oscillator With Variable Duty Cycle

FIXED-FREQUENCY, VARIABLE DUTY CYCLE OSCILLATOR

If Timer 1 is operated in its astable mode and Timer 2 is operated in its monostable mode, as shown in Figure 26, then an oscillator with fixed frequency and variable duty cycle results.

Timer 1 generates a basic periodic waveform that is then used to trigger Timer 2. If the time delay, T_2, of Timer 2 is chosen to be less than the period of oscillations of Timer 1, then the output at pin 13 has the same frequency as Timer 1, but has its duty cycle determined by the timing cycle of Timer 2. The output duty cycle can be adjusted over a wide range (from 1% to 99%) by adjusting R_2.

The frequency and the duty cycle of the output waveform are given as:

$$\text{Frequency} = \frac{1.44}{(R_A + 2R_B)C_1}$$

$$\text{Duty Cycle} = \frac{(1.6)\,R_2C_2}{(R_A + 2R_BC_1)}$$

OSCILLATOR WITH SYNCHRONIZED OUTPUTS

The circuit of Figure 26 can also be used as an oscillator with synchronized multiple frequency outputs. Timer 1 generates an output at frequency f_1 at pin 1, as set by resistor R_A, R_B, and C_1. Timer 2 is used as a frequency divider by setting its timing cycle, T_2, to be larger than the period of Timer 1 (see section on frequency division). The resulting output of Timer 2 (pin 13) is at frequency f_2 given as:

$$f_2 = f_{1/N}$$

where N is the divider ratio set by the external R-C networks as described by Figures 23 and 24.

PULSE-WIDTH MODULATION

For pulse-width modulation, one-half of the XR-2556 is connected as shown in Figure 27. The circuit operates in its monostable mode and is triggered with a continuous pulse train. Output pulses are generated at the same rate as the input pulse train, except the output pulse-width is determined by the timing components R_1 and C_1.

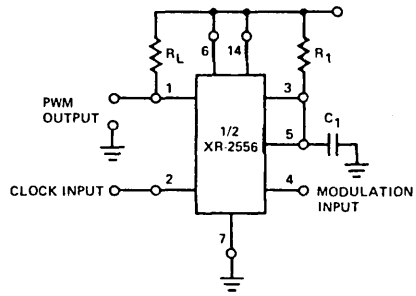


Figure 27. Pulse-Width Modulation

In this mode of operation, the duration of the timing cycle (i.e., the output pulse-width) can be modulated by applying a modulation input to the control voltage terminals (pins 4 or 10). The control characteristics associated with the modulation terminals are depicted in Figure 19. Figure 28 shows the actual circuit waveforms generated in this manner.

When using the XR-2556 for pulse-width modulation, an external clock signal is not necessary, since one section can be operated in its astable mode (see Figure 15) and serve as the clock generator. Figure 29 is the recommended connection for such an application. In this case, Timer 2 is used as the clock generator, and Timer 1 is used as the pulse-width modulator section.

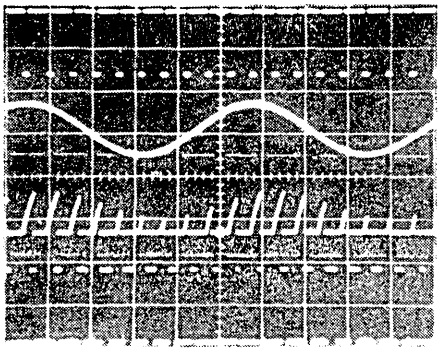


Figure 28. Pulse-Width Modulation Waveforms
a) Clock Input at Pin 2
b) Modulation Input at Pin 4
c) Capacitor Voltage at Pin 3
d) Pulse-Width Modulated Output at Pin 1

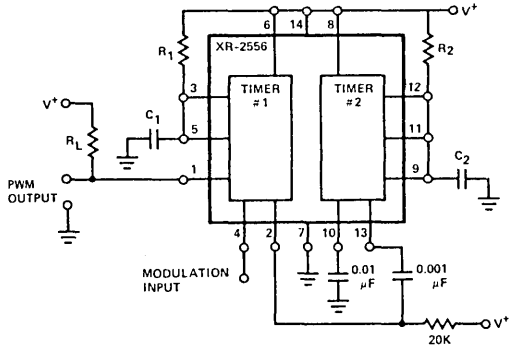


Figure 29. Pulse-Width Modulation With Internal Clock

PULSE-POSITION MODULATION

When a timer section of the XR-2556 is operated in its astable mode (see Figure 15), the period of the output pulse train can be varied by applying a modulation voltage to the corresponding modulation control terminal. In this manner, the repetition rate of the output pulse train can be varied, resulting in a pulse-position modulated output. Typical transfer characteristics between the timing cycle and the modulation voltage are given in Figure 19.

LOGIC "AND" AND "OR" CONNECTION OF OUTPUTS

The individual outputs (pins 1 and 13) of the XR-2556 can be interconnected as shown in Figure 30 to perform logic "or" and "and" functions. Since the output of each timer section is a high-current "totem-pole" type, external diodes are needed to avoid current flow from one output into the other.

Referring to Figure 30(a), the output logic level "P" would read "high" when either one of the outputs at pins 1 or 13 is "high." For Figure 30(b), the output will read "high" only when both outputs at pins 1 and 13 are "high".

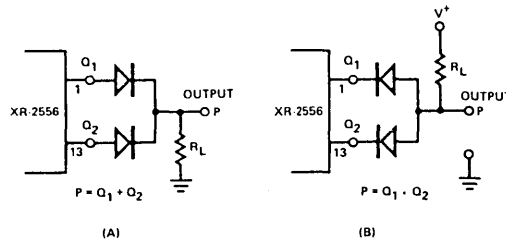
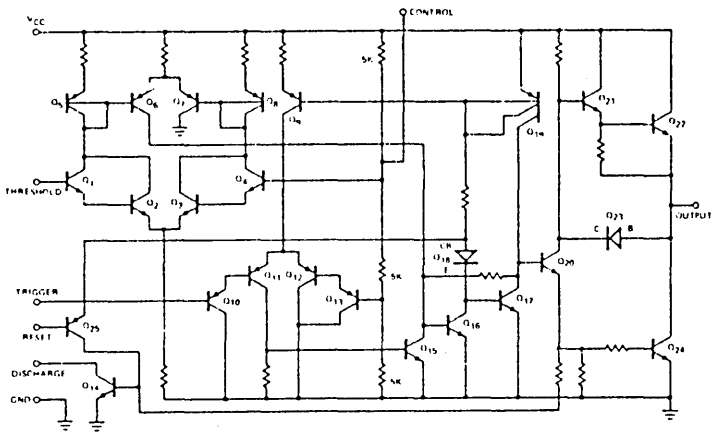


Figure 30. Logic "OR" and "AND"



One section of XR-2556

EQUIVALENT SCHEMATIC DIAGRAM

Programmable Timer/Counter

GENERAL DESCRIPTION

The XR-2240 Programmable Timer/Counter is a monolithic controller capable of producing ultra-long time delays without sacrificing accuracy. In most applications, it provides a direct replacement for mechanical or electromechanical timing devices and generates programmable time delays from micro-seconds up to five days. Two timing circuits can be cascaded to generate time delays up to three years.

As shown in Figure 1, the circuit is comprised of an internal time-base oscillator, a programmable 8-bit counter and a control flip-flop. The time delay is set by an external R-C network and can be programmed to any value from 1 RC to 255 RC.

In astable operation, the circuit can generate 256 separate frequencies or pulse-patterns from a single RC setting and can be syncronized with external clock signals. Both the control inputs and the outputs are compatible with TTL and DTL logic levels.

FEATURES

Timing from micro-seconds to days
Programmable delays: 1RC to 255 RC
Wide supply range; 4V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
External Sync and Modulation Capability
Excellent Supply Rejection: 0.2%/V

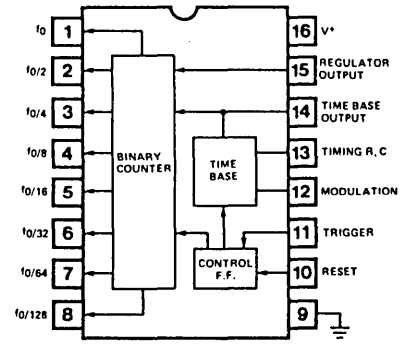
APPLICATIONS

Precision Timing	Frequency Synthesis
Long Delay Generation	Pulse Counting/Summing
Sequential Timing	A/D Conversion
Binary Pattern Generation	Digital Sample and Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mw/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Operating Temperature	
XR-2240M	−55°C to +125°C
XR-2240C	0°C to +70°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2240M	Ceramic	−55°C to +125°C
XR-2240N	Ceramic	0°C to +70°C
XR-2240CN	Ceramic	0°C to +70°C
XR-2240P	Plastic	0°C to +70°C
XR-2240CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2240 is a combination timer/counter capable of generating accurate timing intervals ranging from microseconds through several days. The time base works as an astable multivibrator with a period equal to RC. The eight bit counter can divide the time base output by any integer value from 1 to 255. The wide supply voltage range of 4.5 to 15 V, TTL and DTL logic compatibility, and 0.5% accuracy allow wide applicability. The counter may operate independently of the time base. Counter outputs are open collector and may be wire-OR connected.

The circuit is triggered or reset with positive going pulses. By connecting the reset pin (Pin 10) to one of the counter outputs, the time base will halt at timeout. If none of the outputs are connected to the reset, the circuit will continue to operate in the astable mode. Activating the trigger terminal (Pin 11) while the timebase is stopped will set all counter outputs to the low state and start the timebase.

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2240 MIN	XR-2240 TYP	XR-2240 MAX	XR-2240C MIN	XR-2240C TYP	XR-2240C MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current								
Total Circuit		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Counter Only		1			1.5		mA	See Figure 3
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
	6.0	6.3	6.6	5.8	6.3	6.8	V	$V^+ = 15V$, See Figure 4
TIME BASE SECTION								See Figure 2
Timing Accuracy*		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ $0°C \le T \le 75°C$
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \ge 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1\ k\Omega$, $C = 0.007\ \mu F$
Modulation Voltage Level								Measured at Pin 12
	3.00	3.50	4.0	2.80	3.50	4.20	V	V^+ 5V
		10.5			10.5		V	$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measures at Pin 11, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time**		1			1		μsec.	
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time**		0.8			0.8		μsec.	
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$
								Measured at Pin 14
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10\ pF$
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \le 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$

*Timing error solely introduced by XR-2240, measured as % of ideal time-base period of $T = 1.00\ RC$.

**Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at pin 1.

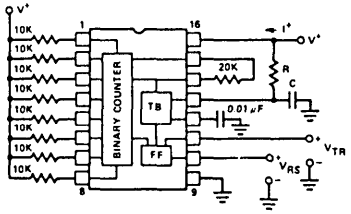


Figure 2. Generalized Test Circuit

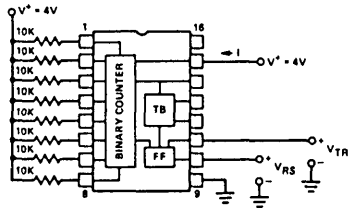


Figure 3. Test Circuit for Low-Power Operation (Time-Base Powered Down)

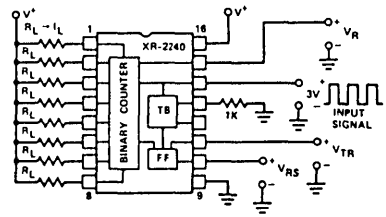


Figure 4. Test Circuit for Counter Section

PRINCIPLES OF OPERATION

The timing cycle for the XR-2240 is initiated by applying a positive-going trigger pulse to pin 11. The trigger input actuates the time-base oscillator, enables the counter section, and sets all the counter outputs to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to pin 10.

Figure 5 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is at reset state, both the time-base and the counter sections are disabled and all the counter outputs are at "high" state.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal, as shown in Figure 6, with S_1 closed. In this manner, the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit would operate in its astable or free-running mode, subsequent to a trigger input.

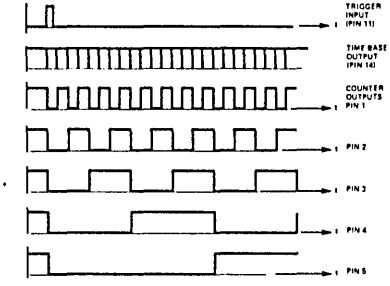


Figure 5. Timing Diagram of Output Waveforms

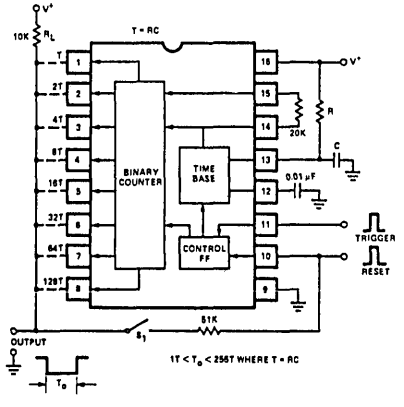


Figure 6. Generalized Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

PROGRAMMING CAPABILITY

The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 6. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1+16+32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_O \leq 255T$, where T = RC.

TRIGGER AND RESET CONDITIONS

When power is applied to the XR-2240 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously trigger overrides reset.

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 5.

The counter outputs can be used individually, or can be connected together in a "wired-or" configuration, as described in the Programming section.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈1.4V) above ground.

Minimum pulse widths for reset and trigger inputs are shown in Figure 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 13). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 16. Recommended sync pulse widths and amplitudes are also given in the figure.

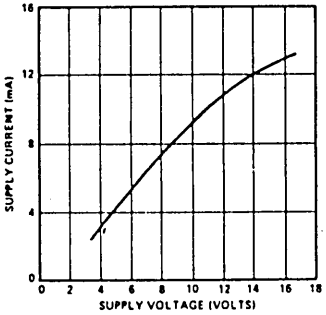


Figure 7. Supply Current vs. Supply Voltage in Reset Condition (Supply Current Under Trigger Condition is ≈0.7 mA less)

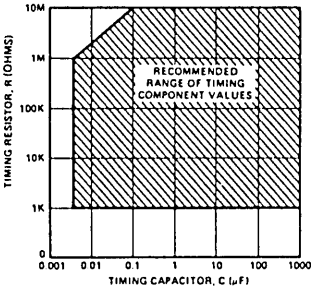


Figure 8. Recommended Range of Timing Component Values.

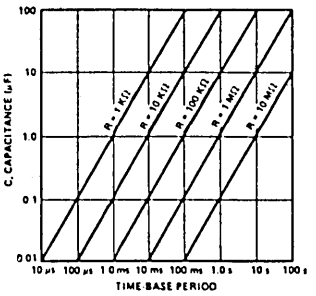


Figure 9. Time-Base Period, T, as a Function of External RC

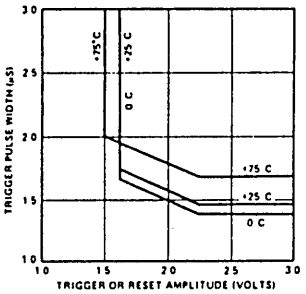


Figure 10. Minimum Trigger and Reset Pulse Widths at Pins 10 and 11

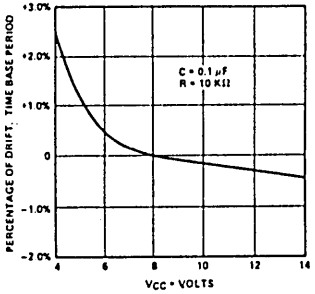


Figure 11. Power Supply Drift

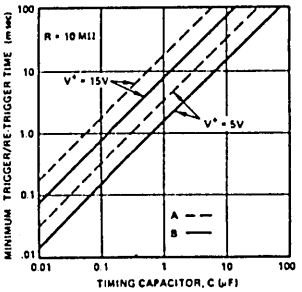


Figure 12.
A) Minimum Trigger Delay Time Subsequent to Application of Power
B) Minimum Re-trigger Time, Subsequent to a Reset Input

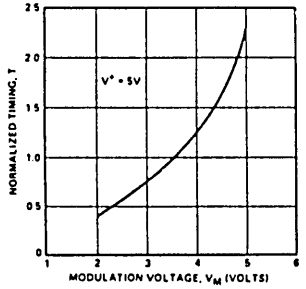
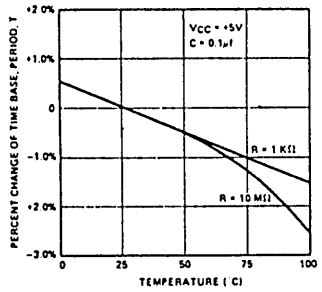


Figure 13. Normalized Change in Time-Base Period As a Function of Modulation Voltage at Pin 12



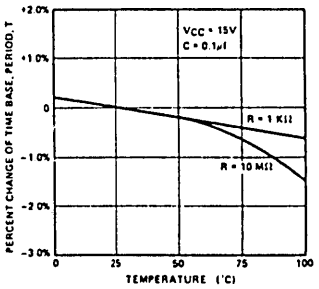


Figure 14. Temperature Drift of Time-Base Period, T

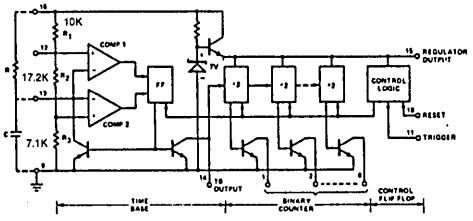


Figure 15. Simplified Circuit Diagram of XR-2240

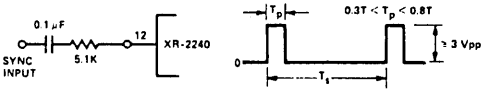


Figure 16. Operation with External Sync Signal.
(a) Circuit for Sync Input
(b) Recommended Sync Waveform

HARMONIC SYNCHRONIZATION

Time-base can be synchronized with *integer multiples or harmonics* of input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = RC = (T_S/m) \text{ where}$$

$$m \text{ is an integer, } 1 \leq m \leq 10.$$

Figure 17 gives the typical pull-in range for harmonic synchronization, for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than $\pm 4\%$ of time-base frequency.

TIMING TERMINAL (PIN 13)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period $T = 1.0\ RC$.

TIME-BASE OUTPUT (PIN 14)

Time-Base output is an open-collector type stage, as shown in Figure 15 and requires a 20 KΩ pull-up resistor to Pin 15 for proper operation of the circuit. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 5.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses applied to pin 14. The trigger threshold for the counter section is $\approx +1.5$ volts. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

Note:

Under certain operating conditions such as high supply voltages ($V^+ > 7V$) and small values of timing capacitor ($C < 0.1\ \mu F$) the pulse-width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300 pF capacitor from pin 14 to ground.

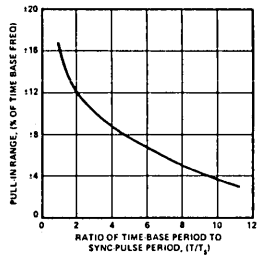


Figure 17. Typical Pull-In Range for Harmonic Synchronization

REGULATOR OUTPUT (PIN 15)

This terminal can serve as a V^+ supply to additional XR-2240 circuits when several timer circuits are cascaded (See Figure 20), to minimize power dissipation. For circuit operation with external clock, pin 15 can be used as the V^+ terminal to power-down the internal time-base and reduce power dissipation. The output current shall not exceed 10 mA.

When the internal time-base is used with $V^+ \leq 4.5V$, pin 15 should be shorted to pin 16.

APPLICATIONS INFORMATION

PRECISION TIMING (Monostable Operation)

In precision timing applications, the XR-2240 is used in its monostable or "self-resetting" mode. The generalized circuit connection for this application is shown in Figure 18.

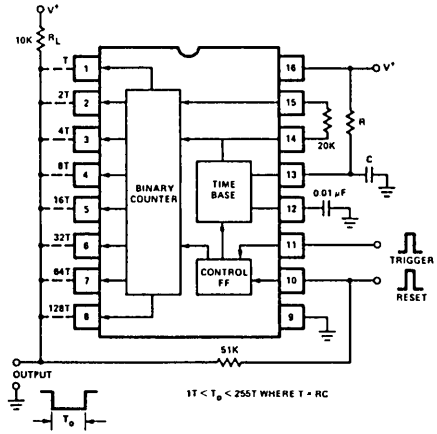


Figure 18. Circuit for Monostable Operation (T_0 = NRC where $1 \leq N \leq 255$)

The output is normally "high" and goes to "low" subsequent to a trigger input. It stays low for the time duration T_0 and then returns to the high state. The duration of the timing cycle T_0 is given as:

$$T_0 = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at pin 13 (See Figure 9). N is an integer in the range of:

$$1 \leq N \leq 255$$

as determined by the combination of counter outputs (pins 1 through 8) connected to the output bus, as described below.

PROGRAMMING OF COUNTER OUTPUTS: The binary counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-or" connection where

the combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be summed by simply shorting them together to a common output bus as shown in Figure 18. For example if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, would be 32T. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1+16+32)\,T = 49T$. In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be: $1T \leq T_O \leq 255T$.

ULTRA-LONG DELAY GENERATION

Two XR-2240 units can be cascaded as shown in Figure 19 to generate extremely long time delays. In this application, the reset and the trigger terminals of both units are tied together and the time base of Unit 2 disabled. In this manner, the output would normally be high when the system is at reset. Upon application of a trigger input, the output would go to a low stage and stay that way for a total of $(265)^2$ or 65,536 cycles of the time-base oscillator.

PROGRAMMING: Total timing cycle of two cascaded units can be programmed from $T_O = 256RC$ to $T_O = 65{,}536RC$ in 256 discrete steps by selectively shorting any one or the combination of the counter outputs from Unit 2 to the output bus.

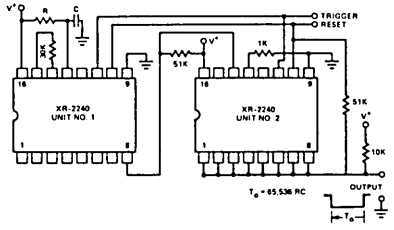


Figure 19. Cascaded Operation for Long Delay Generation

LOW-POWER OPERATION

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption, by using the circuit connection of Figure 20. In this case, the V+ terminal (pin 16) of Unit 2 is left open-circuited, and the second unit is powered from the regulator output of Unit 1, by connecting pin 15 of both units.

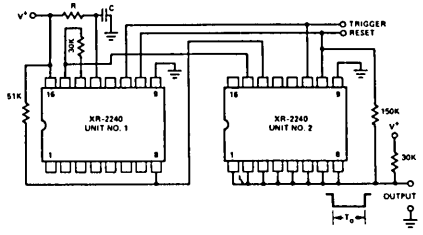


Figure 20. Low-Power Operation of Cascaded Timers

ASTABLE OPERATION

The XR-2240 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 21. In the circuit connection of Figure 21(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 21(a) is essentially the same as that of Figure 6, with the feedback switch S_1 open.

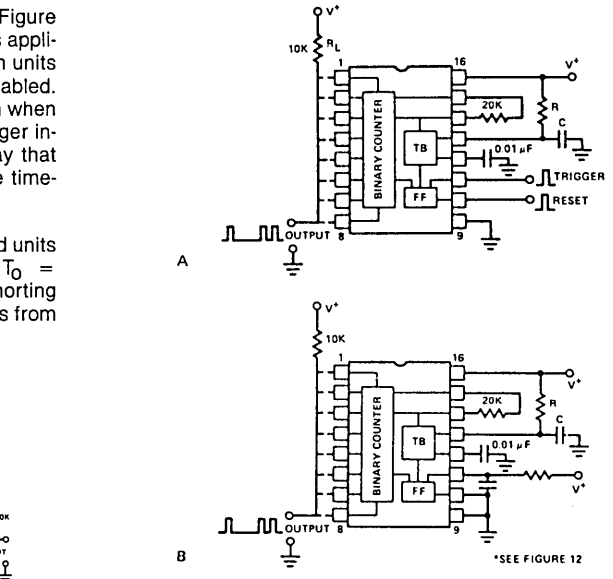


Figure 21. Circuit Connections for Astable Operation
(a) Operation with External Trigger and Reset Controls
(b) Free-running or Continuous Operation

The circuit of Figure 21(b) is designed for continuous operation. The circuit self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected to generate complex pulse patterns.

BINARY PATTERN GENERATION

In astable operation, as shown in Figure 21, the output of the XR-2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 5 which shows the phase relations between the counter outputs. Figure 22 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected

to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

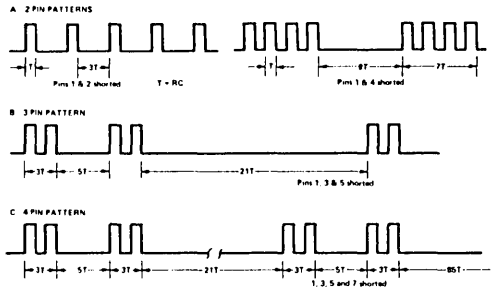


Figure 22. Binary Pulse Patterns Obtained by Shorting Various Counter Outputs

OPERATION WITH EXTERNAL CLOCK

The XR-2240 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 23. The internal time-base can be deactivated by connecting a 1 KΩ resistor from pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be ≥ 1 μS.

For operation with supply voltages of 6V or less, the internal time-base section can be powered down by open-circuiting pin 16 and connecting pin 15 to V+. In this configuration, the internal time-base does not draw any current, and the over-all current drain is reduced by ≈3 mA.

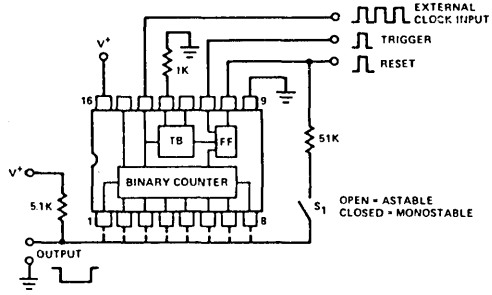


Figure 23. Operation with External Clock

FREQUENCY SYNTHESIZER

The programmable counter section of XR-2240 can be used to generate 255 discrete frequencies from a given time base setting using the circuit connection of Figure 24. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) T where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 4 are connected together to the output bus, the total count is: N = 1 + 4 + 8 = 13; and the period of the output waveform is equal to (N + 1) T or 14T. In this manner, 256 different frequencies can be synthesized from a given time-base setting.

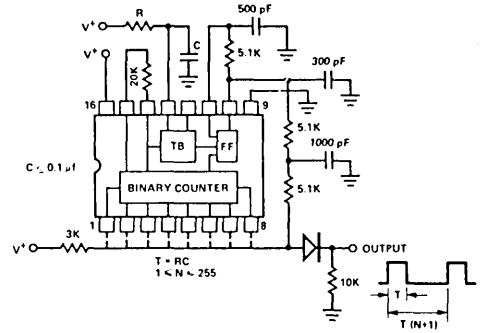


Figure 24. Frequency Synthesis from Internal Time-Base

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the XR-2240 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 25. (See Figures 16 and 17 for external sync waveform and harmonic capture range.) If the time base is synchronized to $(m)^{th}$ harmonic of input frequency where $1 \leq m \leq 10$, as described in the section on "Harmonic Synchronization", the frequency f_O of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_O = f_R \frac{m}{(N + 1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leq N \leq 255$, the circuit of Figure 25 can produce 1500 separate frequencies from a single fixed reference.

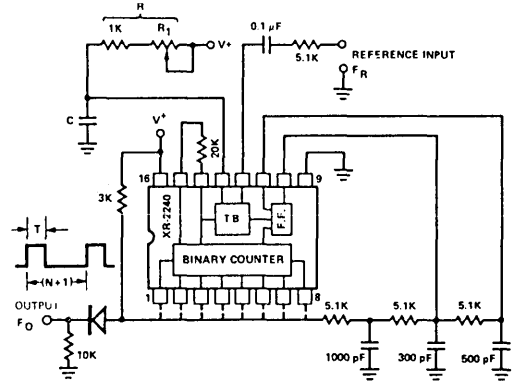


Figure 25. Frequency Synthesis by harmonic Locking to an External Reference

One particular application of the circuit of Figure 25 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external R-C to set m = 10 and setting N = 5, one can obtain a 100 Hz output frequency synchronized to 60 Hz power line frequency.

STAIRCASE GENERATOR

The XR-2240 Timer/Counter can be interconnected with an external operational amplifier and a precision resistor ladder to form a staircase generator, as shown in Figure 26. Under reset condition, the output is low. When a trigger is applied, the op. amp. output goes to a high state and generates a negative going staircase of 256 equal steps. The time duration of each step is equal to the time-base period T. The staircase can be stopped at any desired level by applying a "disable" signal to pin 14, through a steering diode, as shown in Figure 26. The count is stopped when pin 14 is clamped at a voltage level less than 1.4V.

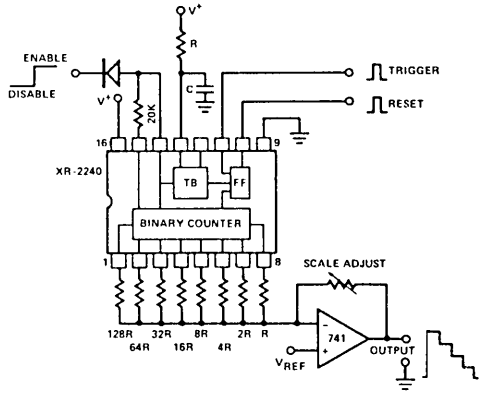


Figure 26. Staircase Generator

DIGITAL SAMPLE/HOLD

Figure 27 shows a digital sample and hold circuit using the XR-2240. The principle of operation of the circuit is similar to the staircase generator described in the previous section. When a "strobe" input is applied, the RC low-pass network between the reset and the trigger inputs of XR-2240 causes the timer to be first reset and then triggered by the same strobe input. This strobe input also sets the output of the bistable latch to a high state and activates the counter.

The circuit generates a staircase voltage at the output of the op. amp. When the level of the staircase reaches that of the analog input to be sampled, comparator changes state, activates the bistable latch and stops the count. At this point, the voltage level at the op. amp. output corresponds to the sampled analog input. Once the input is sampled, it will be held until the next strobe signal. Minimum re-cycle time of the system is ≈6 msec.

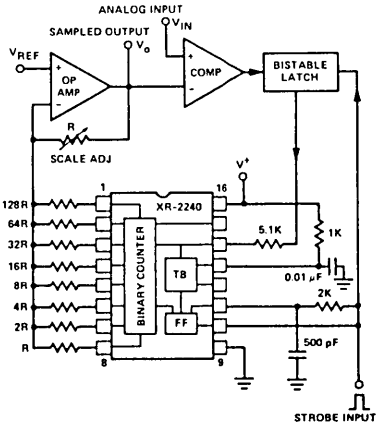


Figure 27. Digital Sample and Hold Circuit

ANALOG-TO-DIGITAL CONVERTER

Figure 28 shows a simple 8-bit A/D converter system using the XR-2240. The operation of the circuit is very similar to that described in connection with the digital sample/hold system of Figure 15. In the case of A/D conversion, the digital output is obtained in parallel format from the binary counter outputs, with the output at pin 8 corresponding to the most significant bit (MSB). The re-cycle time of the A/D converter is ≈6 msec.

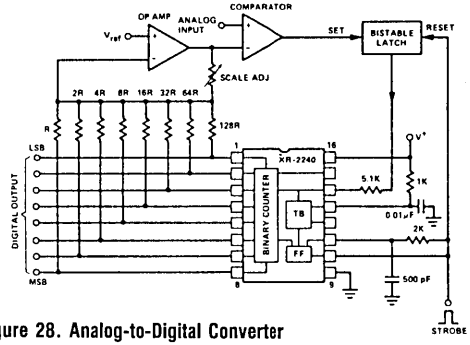
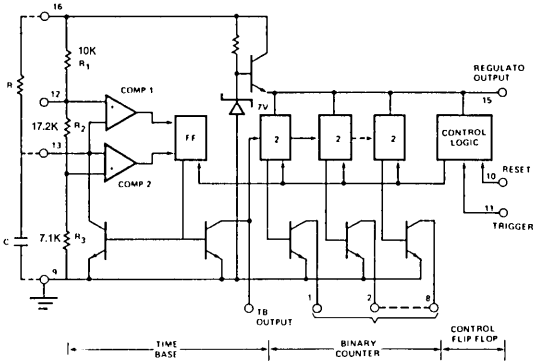


Figure 28. Analog-to-Digital Converter



EQUIVALENT SCHEMATIC DIAGRAM

Long Range Timer

GENERAL DESCRIPTION

The XR-2242 is a monolithic timer/controller capable of producing ultra-long time delays from milliseconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 8 bit binary counter and a control flip-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 128 RC. If two circuits are cascaded, a total time delay of $(128)^2$ or 16,384 RC is obtained.

Three output pins are provided on the device: the time base (RC) on Pin 8, 2 RC on Pin 2, and the counter output (128 RC) on Pin 3.

FEATURES

Timing from micro-seconds to days
Wide supply range: 4.5V to 15V
TTL and DTL compatible outputs
High accuracy: 0.5%
Excellent Supply Rejection: 0.2%/V
Monostable and Astable Operation

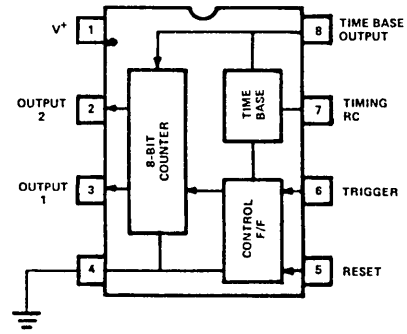
APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Temperature Range	
Operating	
XR-2242M	−55°C to +125°C
XR-2242C	0°C to +70°C
Storage	−65° to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2242M	Ceramic	−55°C to +125°C
XR-2242CN	Ceramic	0°C to +70°C
XR-2242CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The timing cycle for the XR-2242 is initiated by applying a positive-going trigger pulse to Pin 6. The trigger input actuates the time-base oscillator, enables the counter section, and sets the output to "low" state. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to Pin 5.

In monostable timer applications the output terminal (Pin 3) is connected back to the reset terminal. In this manner, after 128 clock pulses are applied to the circuit, this output goes to "high" state and resets the circuit thus completing the timing cycle. Thus, subsequent to triggering, the output at Pin 3 will produce a total timing pulse of 128 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at Pin 2 produces a square-wave output with the period of 2 RC.

If the output at Pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25°C$, $R = 10\ k\Omega$, $C = 0.1\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2242M			XR-2242C			UNIT	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage	4		15	4		15	V	
Supply Current		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
TIME BASE SECTION								See Figure 3
Timing Accuracy*		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ $0°C \le T \le 70°C$
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \ge 8$ Volts
Max Frequency	100	130			130		kHz	$R = 1\ k\Omega$, $C = C = 0.007\ \mu F$
Recommended Range of Timing Components								See Figure 5
Timing Resistor, R	0.001		10	0.001		5	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	Low-Leakage Capacitor Required.
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 6, $V_{RS} = 0$
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time**		1			1		μsec.	
Reset								Measured at Pin 5, $V_{TR} = 0$
Reset Threshold		1.4	2.0		1.4	2.0	V	
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time**		0.8			0.8		μsec.	
COUNTER								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.5	1.0			1.0		MHz	$V_{RS} = 0$, $V_{TR} = 5V$
Input:								
Impedance		20			20		kΩ	
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 2 and 3
Rise Time		180			180		nsec.	$R_L = 3K\Omega$, $C_L = 10$ pF
Fall Time		180			180		nsec.	
Sink Current	3	5		2	4		mA	$V_{OL} \le 0.4V$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} \le 15V$

*Timing error solely introduced by XR-2242, measured as % of ideal time-base period of T = 1.00 RC.

**Propagation delay from application of trigger (or reset) input to corresponding state change in first stage counter output at pin 2.

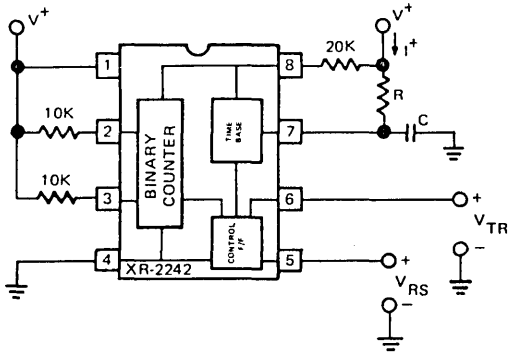


Figure 3. Generalized Test Circuit

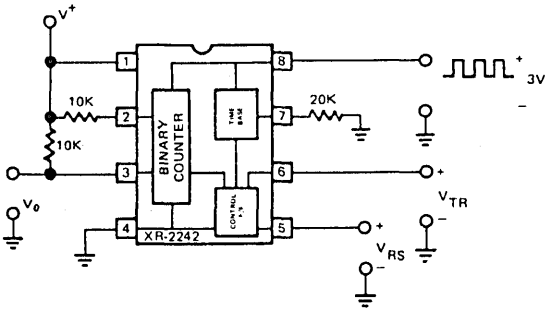


Figure 4. Test Circuit for Counter Section

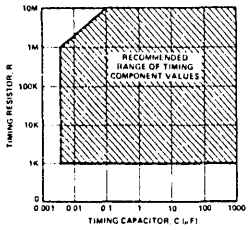


Figure 5. Recommended Range of Timing Component Values

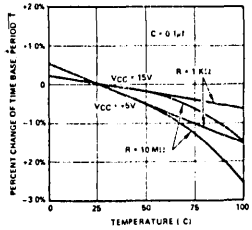


Figure 6. Temperature Drift of Time-Base Period, T

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 2 AND 3)

The binary counter outputs are buffered "open-collector" type stages. Each output is capable of sinking ≈ 5 mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 7.

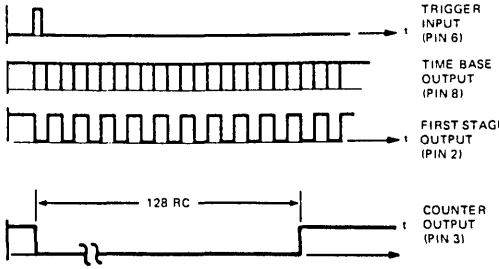


Figure 7. Timing Diagram of Output Waveforms

Basic circuit connection for timing applications is shown in Figure 8. Subsequent to a positive trigger pulse applied to pin 6, the timing output at pin 3 goes to a "low" state and will stay low for a total time duration T_0 = 128 RC, where R and C are the timing components connected to pin 7. If the switch S_1 is *open,* then the output at pin 3 would alternately change state every T_0 interval of time, and the circuit would operate in its "astable" mode. If the switch S_1 is *closed,* the circuit

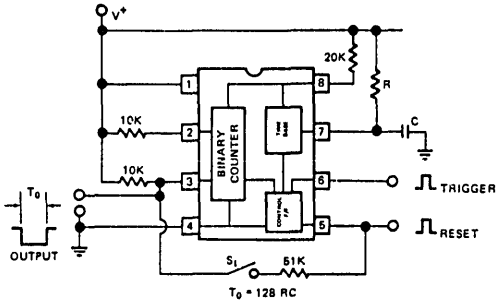


Figure 8. Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

will reset itself and complete its timing cycle after a time interval of T_0, when the output at pin 3 goes to a "high" state. This corresponds to the "monostable" mode of operation.

RESET AND TRIGGER INPUTS (PINS 5 AND 6)

The circuit is reset or triggered with positive-going control pulses applied to pins 5 and 6. The threshold level for these controls is approximately two diode drops (≈ 1.4V) above ground.

Minimum pulse widths for reset and trigger inputs, minimum trigger delay time and minimum re-trigger delay time are shown in Figures 9 and 10. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Note: In noisy operating environment, 0.01 μF capacitors to ground are recommended from reset and trigger terminals.

When power is applied with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset.

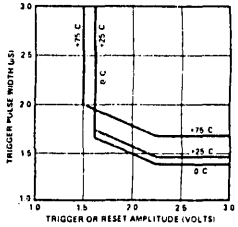


Figure 9. Minimum Trigger and Reset Pulse Widths at Pins 5 and 6

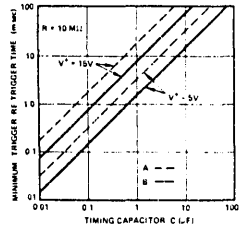


Figure 10. Trigger and Retrigger Delay Time

(A) Minimum Trigger Delay Time Subsequent to Application of Power

(B) Minimum Re-trigger Time, Subsequent to a Reset Input

TIMING TERMINAL (PIN 7)

The time-base period T is determined by the external R-C network connected to this pin. When the time-base is triggered, the waveform at pin 7 is an exponential ramp with a period T = 1.0 RC.

TIME-BASE OUTPUT (PIN 8)

Time-base output is an open-collector type stage, as shown in Figure 1 and requires a 20 KΩ pull-up resistor to Pin 1 (V^+) for proper operation of the circuit. At reset state, the time-base output is at "high" stage. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 7.

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ASTABLE OPERATION

The XR-2242 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 5) from the counter output (pin 3). Two typical circuit connections for this mode of operation are shown in Figures 11 and 12. In the circuit connection of Figure 11, the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 5, the circuit reverts back to its rest state. The circuit of Figure 11 is essentially the same as that of Figure 8, with the feedback switch S_1 open.

The circuit of Figure 12 is designed for continuous operation. The circuit self-triggering automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

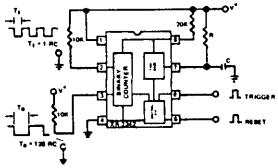


Figure 11. Astable Operation with External Trigger and Reset Controls

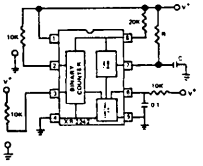


Figure 12. Free-running Operation Self-Triggered When Power Supply is Turned On

OPERATION WITH EXTERNAL CLOCK

The XR-2242 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 8. The internal time-base can be de-activated by connecting a 1 KΩ resistor from pin 7 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width must be ≥ 1 μS.

CASCADED OPERATION:

a) Ultra-Long Delay Generation:

Ultra-long time delays, up to one-year duration, can be generated by cascading two XR-2242 timers as shown in Figure 13. In this configuration, the counter section of Unit 2 is cascaded with the counter output of Unit 1, to provide a total count of 32,640 clock cycles before the output (pin 3 of Unit 2) changes state. In the application circuit of Figure 13, the output (pin 3) of Unit 1 is directly connected to the time-base output (pin 8) of Unit 2, through a common pull-up resistor. In this manner, the counter section of Unit 2 is triggered every time the output of Unit 1 makes a *positive-going* transition. The time-base section of Unit 2 is disabled by connection pin 7 of Unit 2 to ground through a 1 KΩ resistor. The reset and trigger terminals of both units are connected together for common controls. If an additional XR-2242 were cascaded with Unit 2 of Figure 13, the total available time delay can be extended to (1.065) (10^9) RC. With an external RC = 0.1 sec, this would correspond to a time delay of 3.4 years.

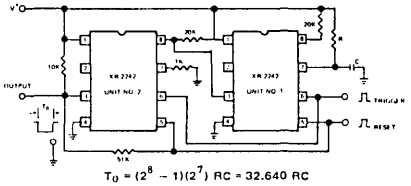


Figure 13. Cascaded Operation of Two XR-2242 Timer Circuits

b) Sequential Timing:

Two XR-2242 timers can be cascaded to produce sequential or delayed-timing pulses as shown in Figure 14. In this configuration, the second timer is triggered by the first timer, subsequent to the completion of its timing cycle. Thus, the triggering of Unit 2 is delayed by a time interval, T_1 (= 128 R_1C_1) corresponding to the timing cycle of Unit 1.

The output of Unit 2, which is normally at "high" state will stay high for a duration of T_1 = 128 R_1C_1, subsequent to the application of a trigger pulse; then go to a low state for a duration of T_2 = 128 R_2C_2 corresponding to the timing interval of Unit 2; and finally revert back to its rest state after the completion of the entire timing sequence.

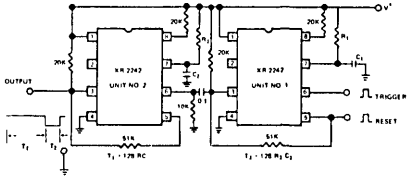
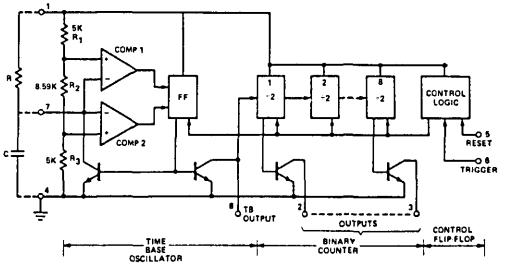


Figure 14. Sequential Timing Using Two XR-2242 Timer Circuits



EQUIVALENT SCHEMATIC DIAGRAM

Micropower Long Range Timer

GENERAL DESCRIPTION

The XR-2243 is a monolithic Timer/Controller capable of producing ultra-long time delays from micro-seconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals up to one year. The circuit is comprised of an internal time-base oscillator, an 11-bit binary counter and a control flop-flop. For a given external R-C network connected to the timing terminal, the circuit produces an output timing pulse of 1024 RC. If the two circuits are cascaded, a total time delay of $(1024)^2$ or 1,048,576 RC is obtained.

The XR-2243 long range timer was designed for low power operation. Its supply current requires less than 100 μA in standby or reset mode. Normal operation requires less than 1mA.

The timing cycle is initiated by applying a positive going pulse to the trigger input, Pin 6. The time-base oscillator generates timing pulses with its period, T, equal to 1 RC. These clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to Pin 5.

In monostable timer applications, the output terminal (Pin 3) is connected to the reset terminal, Pin 5. In this manner, after 1024 clock pulses are counted, this output goes to "high" state and resets the circuit, thus completing the timing cycle. Therefore, after triggering, the output at Pin 3 will produce a total timing pulse of 1024 RC before the circuit resets itself to complete the timing cycle. During the timing interval, the secondary output at Pin 2 produces a square-wave output with the period of 2 RC.

If the output at Pin 3 is not connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

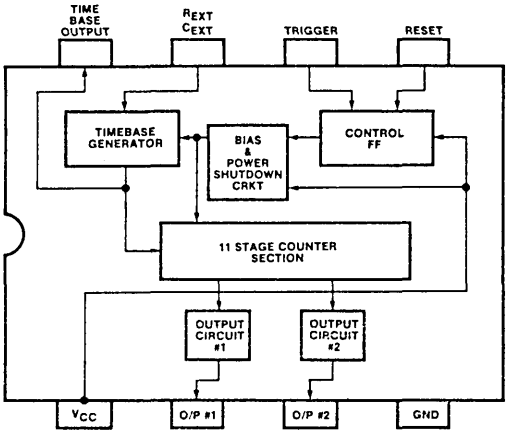
APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator
Battery Powered Applications

FEATURES

High Output Current Sink Capability
Timing from Micro-seconds to Days
Wide Supply Range: 2.2V to 15V
TTL and DTL Compatible Outputs

FUNCTIONAL BLOCK DIAGRAM



High Accuracy: 0.5%
Excellent Supply Rejection
Monostable and Astable Operation
Micro Power Consumption-Standby Operation
Low Power Consumption-Normal Operation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18 Volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic package	300 mW
Derate above +25°C	2.5 mW/°C
Temperature Range	
Operating	
XR-2243C	0°C to +70°C
Storage	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2243CN	Ceramic	0°C to +70°C
XR-2243CP	Plastic	0°C to +70°C

PRINCIPLES OF OPERATION

The ultra-long time delay micropower timer, in simplest block diagram terms, consists of a timing section followed by a counter section and a control flip-flop.

The main functional portion of the circuit is the time base section. It is a relaxation oscillator whose period

ELECTRICAL CHARACTERISTICS

Test Conditions: See Figure 3, $V^+ = 5V$, $T_A = 25°C$, $R = 22\ k\Omega$, $C = 0.047\ \mu F$, unless otherwise noted.

PARAMETERS	XR-2243C MIN	XR-2243C TYP	XR-2243C MAX	UNIT	CONDITIONS
Supply Voltage	2.7		15	V	
Supply Current		45	95	μA	V_{CC} = 2.7V V_{TR} = 0V V_{RS} = 5V
Standby		80	135	μA	V_{CC} = 5V
		250	415	μA	V_{CC} = 15V
Operating		900	1000	μA	V_{CC} = 5V V_{TR} = 5V V_{RS} = 0V
		750	900	μA	V_{CC} = 2.7V
		1250	1500	μA	V_{CC} = 15V
Time Base Section					
Timing Accuracy*		0.5	3	%	V_{CC} = 2.7V V_{TR} = 5V V_{RS} = 0V
Temperature Drift		80	125	ppm/°C	V_{CC} = 5V
		150	225	ppm/°C	V_{CC} = 15V 0°C ≤ T_A ≤ 70°C
		300	650	ppm/°C	V_{CC} = 8V
Supply Drift		0.30	1.0	%/V	
Maximum Frequency	25	35		kHz	
Recommended Range of Timing Components					
Timing Resistor, R	0.005		10	mΩ	
Timing Capacitor, C	0.005		1000	μF	
Trigger/Reset Controls					
Trigger					Measures at Pin 6, V_{RS} = 0
Trigger Threshold		1.4	2.0	V	
Trigger Current		22	30	μA	V_{RS} = 0, V_{TR} = 2V
Impedance		25		kΩ	
Response Time					
Reset					
Reset Threshold		1.4	2.0	V	
Reset Current		22	30	μA	V_{TR} = 0, V_{RS} = 2V
Impedance		25		kΩ	
Response Time					
Counter Section					See Figure 4, $V^+ = 5V$
Max. Toggle Rate		100	250	kHz	V_{RS} = 0, V_{TR} = 5V Measured at Pin 8
Input:					
Impedance		15		kΩ	
Threshold		1.4		V	
Output:					
Sink Current		10		mA	$V_{OL} \leq 0.4V$
Leakage Current		0.01		μA	$V_{OH} \leq 15V$

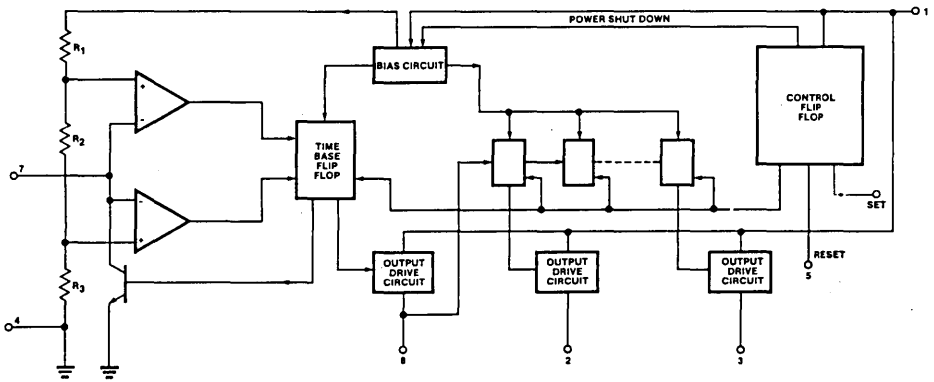


Figure 1. Simplified Circuit Schematic

of oscillation is determined by the external R and C values. The timing section is followed by an I^2L counter, which consists of eleven binary stages, with high current drive capability output stages from the first and the last. A third subsection of the circuit is the control logic circuit consisting of a flip-flop that is set and reset by Pins 6 and 5, respectively. This section controls the resetting of all counter stages, and starting the timing circuit upon application of a positive-going trigger pulse. The control logic also activates the power shut down circuit when a reset pulse is received, or when the timing cycle is completed. The power shut down circuit turns off the bias line to the time base and I^2L counters to reduce the standby power.

CONTROL FLIP-FLOP

The logic flip-flop circuit controls the time/counter, as well as the internal power, to reduce standby current consumption to approximately 100μA. Upon command, by a positive-going trigger pulse applied to Pin 6, the control logic circuit will first establish the upper and lower threshold voltages and then setup all internal current sources, biasing the time base and counter sections.

The circuit will automatically reset itself when power is first applied. Once triggered, the circuit is immune to additional trigger pulses until it is reset. A reset pin terminates the timing cycle by resetting the internal logic and shuts off the internal bias circuitry.

TIME BASE OSCILLATOR

The time base oscillator is a simple exponential ramp type timer circuit. The timing components, R and C, are external to the chip. The operation of such an oscillator can be described as follows: when the circuit is at rest the flip-flop is latched in its reset state, the discharge transistor is "off", and the external capacitor, C, is fully charged to a voltage approximately equal to V_{CC}. When the circuit is triggered, the flip-flop is unlatched and set, which causes the discharge transistor to turn "on" and discharge C rapidly. When the voltage across C discharges to the voltage level V_{th-}, the upper comparator changes state, resets the flip-flop and turns the discharge transistor "off". Then, C charges toward V_{CC} with a time constant set by the external R and C. When the voltage across it reaches the upper threshold, V_{th+}, the comparator changes state, sets the flip-flop again, and discharges C back to the lower threshold level, V_{th-}. In this manner, the circuit continues to oscillate with the voltage level across C exponentially rising to V_{th+}, then rapidly decaying to V_{th-} and then repeating this cycle until the timing period ends.

COUNTER SECTION (Pin 8)

The counter consists of eleven stages connected in a "ripple counter" configuration. The operating injector currents are set from a bus of 1.2 volts. This current is supply independent. Pin 8, which is time based o/p, is also the counter section input.

I^2L counters are D-type flip-flops with their $\overline{Q}$ output internally connected to their D input; basically, they form a divide by 2 block. With eleven stages, one could create delays of 1024 RC in a monostable mode of operation. The counters change state on the falling edge of the clock pulses.

When the trigger pulse is applied, the internal power line which is supplying voltage for I^2L circuitry (I^2L_{VCC}) is set up first, a Schmitt trigger circuit with a built in delay ensures the application of an internal set pulse, right after the power for the I^2 section is made available. The counters are all set to "1" and are ready to count with the incoming falling edges of clock impulses.

OUTPUT SECTIONS (Pins 2 and 3)

The output sections are designed such that they can handle 10mA load currents @ V_{OL} = 300mV. Both of the transistors in this section are operating in a non-saturated mode because of the clamping action. This ensures faster operation and also decreases the need of high base drive at full load operation.

The timing cycle for the circuit is initiated by applying a positive-going trigger to the set, or trigger pin, (Pin 6) of the device. The trigger pulse actuates the time base oscillator, enables the counter section, and sets the outputs to "low" state. The time base oscillator generates timing pulses with its period, T = 1RC. These timing or clock pulses are counted by the binary counter section. The timing cycle is completed when a positive-going reset pulse is applied to the reset pin (Pin 5).

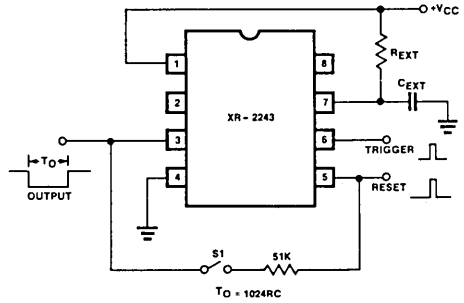


Figure 2. Typical Operation Diagram

ASTABLE AND MONOSTABLE MODE

Figure 2 shows the basic connection diagram for astable and monostable modes. When switch S_1 is open, the circuit is in its astable mode of operation. Upon the application of a trigger pulse, the time base oscillator resumes the timing cycles. Until the application of a reset pulse, the circuit will keep on working while generating a square wave at the last stage output, whose frequency is 1/2048 of the time base oscillator frequency. When switch S_1 is closed, the circuit is in its monostable mode of operation, with the last stage being connected to the reset input via an external resistor. This way, when a trigger pulse is applied, and the time base resumes its timing cycle, the last stage output will go low with the first pulse generated by the time

base generator, and will stay low for 1024 pulses. With the arrival of the 1024th pulse, the last output will go to a high state since it is coupled to the reset input (see Figure 3). When this stage goes high, the timing cycle is completed.

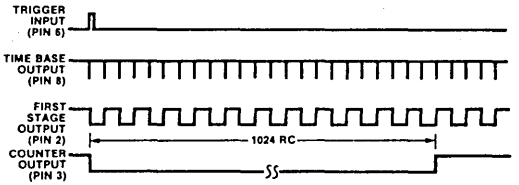


Figure 3. Timing Diagram of Output Waveforms

CASCADED MODE

The cascaded mode of operation allows the generation of ultra-long time delays. When several XR-2243 circuits are cascaded, such that their counter sections are connected in series, the total count available increases geometrically rather than arithmetically. Since one XR-2243 is capable of generating a total of 1024 RC time delay, where R and C are the external timing components, then when two such timers are cascaded, they will produce $(1024)^2$ RC and three will produce $(1024)^3$ RC time delay, and so on. Thus, one can easily achieve time delays in the range of days, months, or years, simply by cascading two or three such counter/timer circuits.

Figure 4 shows the basic connection for cascaded operation. Unit 2's time base is disabled by grounding Pin 7 to ground via 1 kΩ resistor. The last stage output of Unit 1 is connected to the input of the counter section of Unit 2. When the circuit is triggered, Unit 1 will resume generating a frequency whose period $T = R_{ext}C_{ext}$. The output of Unit 1 will change state every 1024 pulses. Since these pulses are supplied to Unit 2, the circuit will stop the timing cycle after 1024 pulses are generated by Unit 1. Therefore, a time delay of $(1024)^2$ RC is generated.

SEQUENTIAL TIMING APPLICATIONS

Figure 5 shows the basic connections for sequential timing applications. In this mode of operation, Unit 2's trigger input is connected to Unit 1's last output, while each unit's reset input is connected to their last output via external resistors. This way, Unit 1 will generate a time delay 1024 R_1C_1 upon the application of a trigger pulse. Once 1024 R_1C_1 seconds have elapsed, Unit 2 will be triggered, generating in its turn a delay equal to 1024 R_2C_2 seconds; therefore, resulting in an overall time delay of 1024 R_1C_1 + 1024 R_2C_2.

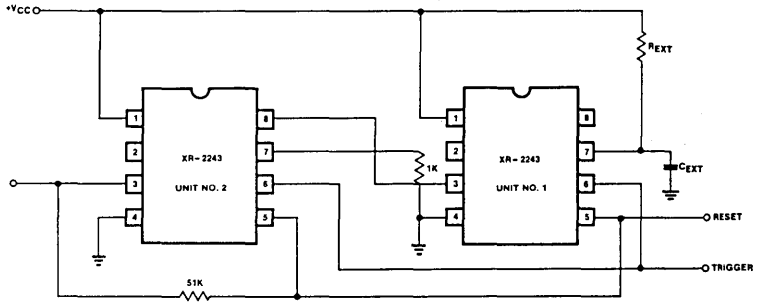


Figure 4. Cascaded Operation of Two XR-2243 Timer Circuits

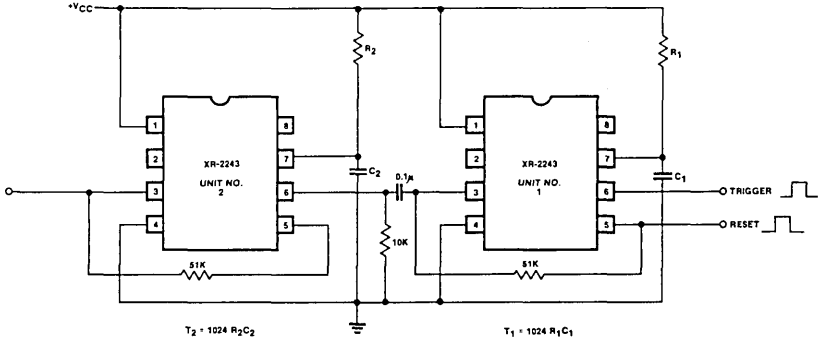


Figure 5. Sequential Timing Using XR-2243 Timer Circuits

Both linear ramp waveforms have pk-pk amplitudes of $2V_{BE}$. Their frequency of oscillation, f_o, can be determined from the formula

$$f_o = \frac{I_1}{4V_{BE}C_o}.$$

And f_o can be controlled by variation of charging-current I_1 via control voltage V_C. A subtraction of one output ramp voltage from the other, by use of a simple differential amplifier, obtains the linear triangular waveform.

Symmetry of triangle and square-wave outputs may be adjusted by replacement of one of the two current sources in Figure 2 by I_2, where $I_2 \neq I_1$. Then the duty cycle of the output waveforms becomes the following:

$$\text{Duty Cycle} = 50\frac{I_1}{I_2}\%.$$

The duty cycle of the output may be varied over a wide range by varying the ratio of the currents I_1 and I_2.

Wave-Shaping Techniques

The most useful waveform in signal processing applications is the sine wave. In the design of function generators, sinusoidal output is normally obtained by passing a triangular wave through a wave shaping circuit. In most discrete-component generators, wave-shaping involves a diode-resistor or a transistor-resistor ladder network. Introduction of a finite number of "break points" on the triangle wave changes it to a lower distortion sine wave.

Although this method can also be adapted to monolithic circuits, it is not as practical because it requires extremely tight control of resistor values and diode characteristics. A simpler, and more practical, sine shaper for monolithic circuits employs the "gradual cutoff" characteristics of a basic differential gain stage, as in Figure 3.

Reduction of the emitter = degeneration resistance, R_E, allows either transistor Q_3 or Q_4 to be brought near their cutoff point when the input triangle waveform reaches its peaks. For the proper choice of the input amplitude and bias-current levels, the transfer characteristics at the peaks of the input triangle waveform become logarithmic rather than linear. Thus, the peaks of the triangle become rounded, and the output appears as a low distortion sine wave.

Use of this technique permits output harmonics to be reduced to less than 0.5% with only a single adjustment. The low distortion is possible because the technique relies on component matching rather than their absolute values. Since monolithic ICs can be designed readily for close matching, this wave-shaping is ideally suited to monolithic design.

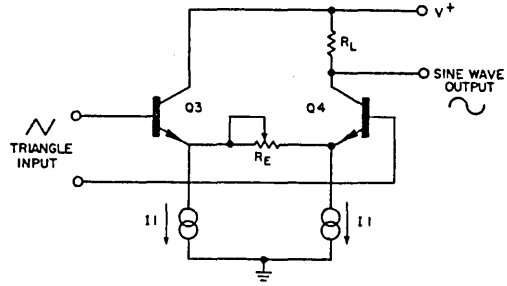


Figure 3. Conversion of triangle to sine wave employs a differential gain stage, which avoids dependence on absolute values of components.

Section 5 – Industrial Circuits

Pulse-Width Modulating Regulator

GENERAL DESCRIPTION

The XR-494 is a monolithic pulse width modulating regulator designed to contain all the blocks necessary for a switching regulator. Included in a 16 pin dual in-line package is a voltage reference, oscillator, control logic, error amplifiers, and dual uncommitted outputs. This device can be used for switching regulators of either polarity, polarity converters, transformer coupled DC to DC converters, transformerless voltage doublers, and many other power control applications. The XR-494M is fully specified for operation over the full military temperature range from −55°C to +125°C, while the XR-494CN and XR-494CP are designed for commercial applications over 0°C to +70°C.

FEATURES

Complete PWM Power Control Circuitry
Uncommitted Outputs for 200-mA Sink or Source
Output Control Selects Single-Ended or Push-Pull Operation
Internal Circuitry Prohibits Double Pulse at Either Output
Variable Dead Time Provides Control Over Total Range
Internal Regulator Provides a Stable 5-V Reference Supply
Circuit Architecture Provides Easy Synchronization

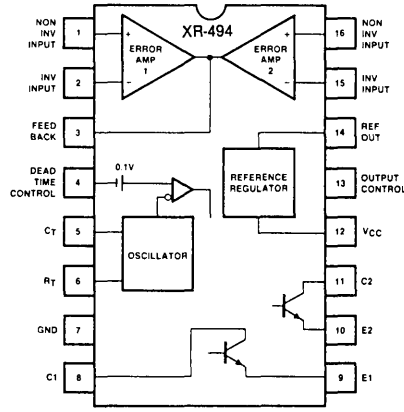
APPLICATIONS

Pulse-Width Modulated Power Control Systems
Switching Regulators

ABSOLUTE MAXIMUM RATINGS, T_A = 25°C

Amplifier Input Voltages	V_{CC} + 0.3 Volts
Output Current	250 mA
Supply Voltage	41 Volts
Collector Output Voltage	41 Volts
Power Dissipation	
Total, at or below 25°C	1000 mW
Ceramic Package	
Derate above +28°C	8.2 mW/°C
Plastic Package	
Derate above +41°C	9.2 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-494M	Ceramic	−55°C to +125°C
XR-494CN	Ceramic	0°C to +70°C
XR-494CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip in the XR-494. The device is primarily designed for power supply control and contains a on-chip five volt regulator, two error amplifiers, an adjustable oscillator, dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transistors. Single ended or push-pull output operation may be selected through the output control function. The XR-494 architecture prohibits the possibility of either output being pulsed twice during push-pull operation. The internal amplifiers's circuitry allows for a common-mode input voltage range of −0.3 volt to V_{CC} −2 volts. The dead time control comparator provides approximately 5% dead time unless the dead time control is externally driven. The on-chip oscillator may be used to drive the common XR-494 circuitry and provide a sawtooth input for associated control circuitry in synchronous multiple-rail power supplies, or may be bypassed by terminating R_T (Pin 6) to the reference output and providing a sawtooth input to C_T (Pin 5).

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-494 MIN	XR-494 TYP	XR-494 MAX	UNIT	CONDITIONS
Reference Section					
Output Voltage (V_{ref})	4.75	5.0	5.25	V	I_O = 1mA
Input Regulation		2.0	25.0	mV	V_{CC} = 7V to 40V
Output Regulation		1	15	mV	I_O = 1 to 10mA
Output Voltage Change with Temperature		0.2	1	%	ΔT_A = Min to Max
Short Circuit Output[1] Current	10	35	50	mA	V_{ref} = 0
Oscillator Section					
Frequency		10		kHz	C_T = 0.01 μF, R_T = 12kΩ
Standard Deviation[2] of Frequency		10		%	V_{CC}, C_T, R_T, T_A; all values constant
Frequency Change with Voltage		0.1		%	V_{CC} = 7V to 40V
Frequency Change with Temperature			2	%	C_T = 0.01μF, R_T = 12kΩ, ΔT_A = Min to Max
Dead Time Control Section (See Figure 2)					
Input Bias Current (Pin 4)		−2	−10	μA	V_I = 0 to 5.25V
Maximum Duty Cycle (each output)	45			%	V_I = 0 (Pin 4)
Input Threshold Voltage (Pin 4)		3	3.3	V	Zero Duty Cycle, Maximum Duty Cycle = 0V Min
Error-Amplifier Sections					
Input Offset Voltage		2	10	mV	V_O (Pin 3) = 2.5V
Input Offset Current		25	250	nA	V_O (Pin 3) = 2.5V
Input Bias Current		0.2	1	μA	V_O (Pin 3) = 2.5V
Common-Mode Input Voltage Range	−0.3 to V_{CC} −2			V	V_{CC} = 7V to 40V
Open Loop Voltage Amplification	70	95		dB	ΔV_O = 3V, V_O = 0.5V to 3.5V
Unity Gain Bandwidth		800		kHz	
Common-Mode Rejection Ratio	65	80		dB	V_{CC} = 40V
Output Sink Current (Pin 3)	0.3	0.7		mA	V_{ID} = −15mV to −5V, V (Pin 3) = 0.7V
Output Source Current (Pin 3)	-2			mA	V_{ID} = 15mV to 5V, V (Pin 3) = 3.5V
Output Section					
Collector Off-State Current		2	100	μA	V_{CE} = 40V, V_{CC} = 40V
Emitter Off-State Current			−100	μA	V_{CC} = V_C = 40V, V_E = 0, XR-494M Max = −150μA
Collector-Emitter Saturation Voltage Common-Emitter		1.1	1.3	V	V_E = 0, I_C = 200mA, XR-494M Max = 1.5V
Emitter-Follower		1.5	2.5	V	V_C = 15V, I_E = −200mA
Output Control Input Current			3.5	mA	V_I = V_{ref}
PWM Comparator Section					
Input Threshold Voltage (Pin 3)		4	4.5	V	Zero Duty Cycle
Input Sink Current (Pin 3)	0.3	0.7		mA	V (Pin 3) = 0.7V
Total Device					
Standby Supply Current		6	10	mA	V_{CC} = 15V, Pin 6 at V_{ref}
		9	15	mA	V_{CC} = 40V, All Other Inputs and Outputs Open
Average Supply Current		7.5		mA	V = 2V (Pin 4)

5

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	XR-494M		XR-494CN XR-494CP		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltages, V_I	−0.3	V_{CC} −2	−0.3	V_{CC} −2	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Current into feedback terminal		0.3		0.3	mA
Timing capacitor, C_T	0.47	10,000	0.47	10,000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Oscillator frequency	1	300	1	300	kHz
Operating free-air temperature, T_A	−55	125	0	75	°C

SWITCHING CHARACTERISTICS T_A = 25°C

PARAMETER	MIN.	TYP.[1]	MAX.	UNIT	TEST CONDITIONS
Output Voltage Rise Time Output Voltage Fall Time		100 25	200 100	ns ns	Common-Emitter Configuration, See Figure 1
Output Voltage Rise Time Output Voltage Fall Time		100 40	200 100	ns ns	Emitter-Follower Configuration, See Figure 2

1. All typical values except for temperature coefficients are at T_A = 25°C.

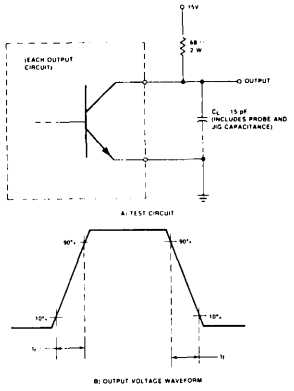


Figure 1. Common-Emitter Configuration

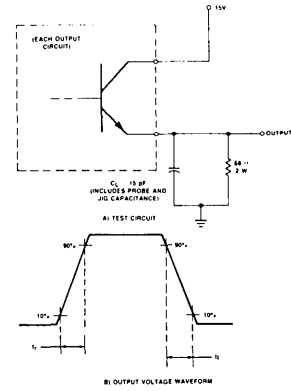


Figure 2. Emitter-Follower Configuration

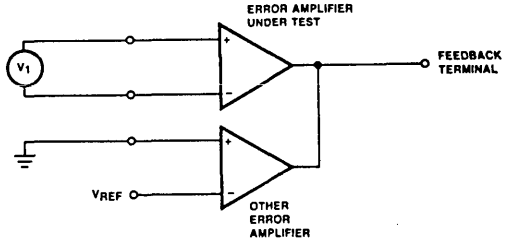
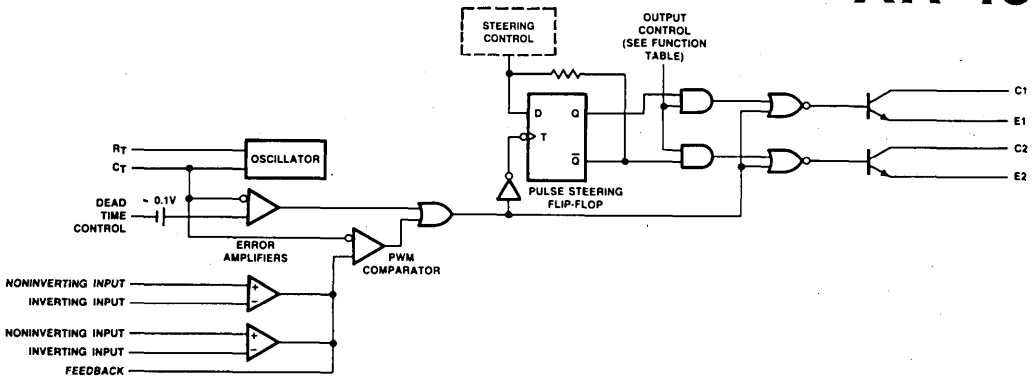


Figure 3. Error-Amplifier Characteristics

FUNCTION TABLE

INPUTS	
OUTPUT CONTROL	OUTPUT FUNCTION
Grounded	Single-ended or parallel output
At V_{ref}	Normal push-pull operation
At V_{ref}	PWM Output at Q1
At V_{ref}	PWM Output at Q2



EQUIVALENT SCHEMATIC DIAGRAM

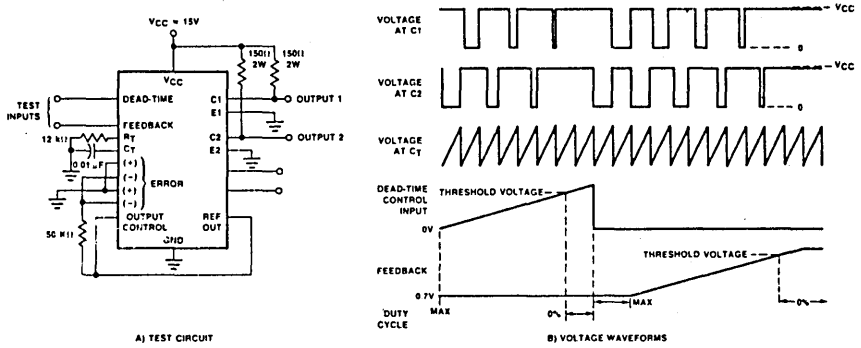
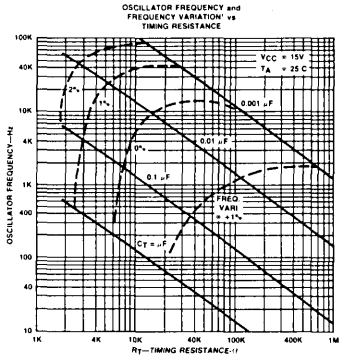


Figure 4. Dead-Time and Feedback Control



[1] Frequency variation is the change in oscillator frequency that occurs over the full temperature range.

Figure 5. Oscillator Frequency and Frequency Variation[1] vs Timing Resistance

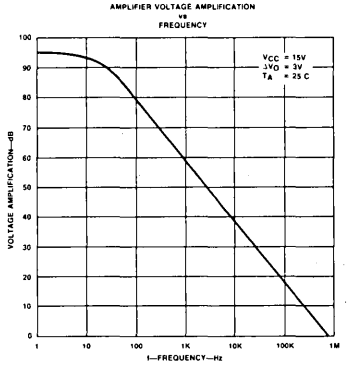


Figure 6. Amplifier Voltage Amplification vs Frequency

Pulse-Width Modulating Regulator

GENERAL DESCRIPTION

The XR-495 is a monolithic pulse width modulating regulator designed to contain all blocks necessary for a switching regulator. Included in the 16 pin dual in-line packages is a voltage reference, oscillator, control logic, error amplifiers, and dual uncommitted outputs. This device can be used for switching regulators of either polarity, polarity converters, transformer coupled DC to DC converters, transformerless voltage doublers, and many other power control applications. A 39V zener diode allows operation with supply voltages exceeding 40V. The XR-495M is fully specified for operation over the full military temperature range from −55°C to +125°C, while the XR-495CN and XR-495CP are designed for commercial applications over 0°C to +70°C.

FEATURES

Complete PWM Power Control Circuitry
Uncommitted Outputs for 200-mA Sink or Source
Output Control Selects Single-Ended or Push-Pull Operation
Internal Circuitry Prohibits Double Pulse at Either Output
Variable Dead Time Provides Control Over Total Range
Internal Regulator Provides a Stable 5-V Reference Supply
Circuit Architecture Provides Easy Synchronization
On-Chip 39-V Zener
External Control of Output Steering

APPLICATIONS

Pulse-Width Modulated Power Control Systems
Switching Regulators

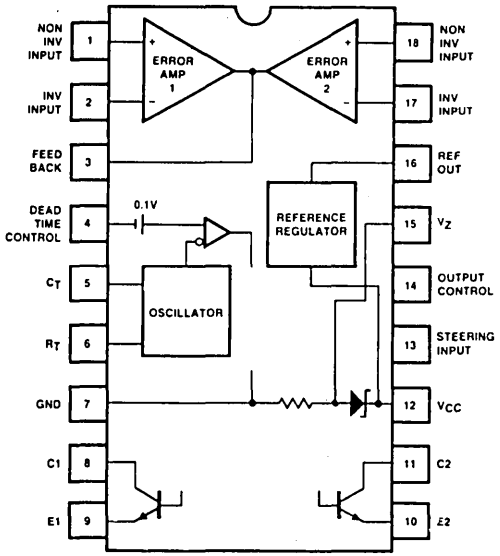
ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-495M	Ceramic	−55°C to +125°C
XR-495CN	Ceramic	0°C to +70°C
XR-495CP	Plastic	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS, T_A = 25°C

Amplifier Input Voltages	V_{CC} + 0.3 Volts
Output Current	250 mA
Supply Voltage	41 Volts
Collector Output Voltage	41 Volts
Power Dissipation	
Total, at or below 25°C	1000 mW
Ceramic Package	
Derate above +28°C	8.2 mW/°C
Plastic Package	
Derate above +41°C	9.2 mW/°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip in the XR-495. The device is primarily designed for power supply control and contains a on-chip five volt regulator, two error amplifiers, an adjustable oscillator, dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transistors. Single ended or push-pull output operation may be selected through the output control function. The XR-495 architecture prohibits the possibility of either output being pulsed twice during push-pull operation. The internal amplifier's circuitry allows for a common-mode input voltage range of −0.3 volt to V_{CC} −2 volts. The dead time control comparator provides approximately 5% dead time unless the dead time control is externally driven. The on-chip oscillator may be used to drive the common XR-495 circuitry and provide a sawtooth input for associated control circuitry in synchronous multiple-rail power supplies, or may be bypassed by terminating R_T (Pin 6) to the reference output and providing a sawtooth input to C_T (Pin 5).

The XR-495 also contains an on-chip 39 volt zener diode for high voltage applications where V_{CC} is greater than 40 volts, and an output steering control that overrides the internal control of the pulse steering flip-flop.

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, unless specified otherwise.

PARAMETERS	XR-495 MIN	XR-495 TYP	XR-495 MAX	UNIT	CONDITIONS
Reference Section					
Output Voltage (V_{ref})	4.75	5.0	5.25	V	I_O = 1mA
Input Regulation		2.0	25.0	mV	V_{CC} = 7V to 40V
Output Regulation		1	15	mV	I_O = 1 to 10mA
Output Voltage Change with Temperature		0.2	1	%	ΔT_A = Min to Max
Short Circuit Output[1] Current	10	35	50	mA	V_{ref} = 0
Oscillator Section					
Frequency		10		kHz	C_T = 0.01 μ, R_T = 12kΩ
Standard Deviation[2] of Frequency		10		%	V_{CC}, C_T, R_T, T_A; all values constant
Frequency Change with Voltage		0.1		%	V_{CC} = 7V to 40V
Frequency Change with Temperature			2	%	C_T = 0.01μF, R_T = 12kΩ, ΔT_A = Min to Max
Dead Time Control Section (See Figure 2)					
Input Bias Current (Pin 4)		−2	−10	μA	V_I = 0 to 5.25V
Maximum Duty Cycle (each output)	45			%	V_I = 0 (Pin 4)
Input Threshold Voltage (Pin 4)		3	3.3	V	Zero Duty Cycle, Maximum Duty Cycle = 0V Min
Error-Amplifier Sections					
Input Offset Voltage		2	10	mV	V_O (Pin 3) = 2.5V
Input Offset Current		25	250	nA	V_O (Pin 3) = 2.5V
Input Bias Current		0.2	1	μA	V_O (Pin 3) = 2.5V
Common-Mode Input Voltage Range	−0.3 to V_{CC} −2			V	V_{CC} = 7V to 40V
Open Loop Voltage Amplification	70	95		dB	ΔV_O = 3V, V_O = 0.5V to 3.5V
Unity Gain Bandwidth		800		kHz	
Common-Mode Rejection Ratio	65	80		dB	V_{CC} = 40V
Output Sink Current (Pin 3)	0.3	0.7		mA	V_{ID} = −15mV to −5V, V (Pin 3) = 0.7V
Output Source Current (Pin 3)	−2			mA	V_{ID} = 15mV to 5V, V (Pin 3) = 3.5V
Output Section					
Collector Off-State Current		2	100	μA	V_{CE} = 40V, V_{CC} = 40V
Emitter Off-State Current			−100	μA	V_{CC} = V_C = 40V, V_E = 0, XR-494M Max = −150μA
Collector-Emitter Saturation Voltage Common-Emitter		1.1	1.3	V	V_E = 0, I_C = 200mA, XR-494M Max = 1.5V
Emitter-Follower		1.5	2.5	V	V_C = 15V, I_E = −200mA
Output Control Input Current			3.5	mA	V_I = V_{ref}
PWM Comparator Section					
Input Threshold Voltage (Pin 3)		4	4.5	V	Zero Duty Cycle
Input Sink Current (Pin 3)	0.3	0.7		mA	V (Pin 3) = 0.7V
Total Device					
Standby Supply Current		6	10	mA	V_{CC} = 15V, Pin 6 at V_{ref}
		9	15	mA	V_{CC} = 40V, All Other Inputs and Outputs Open
Average Supply Current		7.5		mA	V = 2V (Pin 4)

1. Duration of the short circuit should not exceed one second.
2. Standard deviation is a measure of the statistical distribution about the mean as derived from the formula σ =.

SWITCHING CHARACTERISTICS T_A = 25°C

PARAMETER	MIN	TYP[1]	MAX.	UNIT	TEST CONDITIONS
Output Voltage Rise Time		100	200	ns	Common-Emitter Configuration,
Output Voltage Fall Time		25	100	ns	See Figure 1
Output Voltage Rise Time		100	200	ns	Emitter-Follower Configuration,
Output Voltage Fall Time		40	100	ns	See Figure 2

1. All typical values except for temperature coefficients are at T_A = 25°C.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	XR-495M		XR-495CN XR-495CP		UNIT
	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}	7	40	7	40	V
Amplifier input voltages, V_I	−0.3	$V_{CC}-2$	−0.3	$V_{CC}-2$	V
Collector output voltage, V_O		40		40	V
Collector output current (each transistor)		200		200	mA
Current into feedback terminal		0.3		0.3	mA
Timing capacitor, C_T	0.47	10,000	0.47	10,000	nF
Timing resistor, R_T	1.8	500	1.8	500	kΩ
Oscillator frequency	1	300	1	300	kHz
Operating free-air temperature, T_A	−55	125	0	75	°C

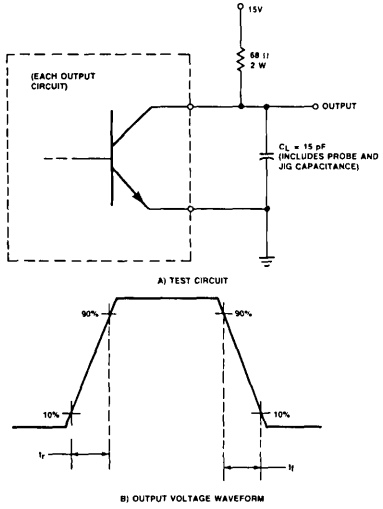


Figure 1. Common-Emitter Configuration

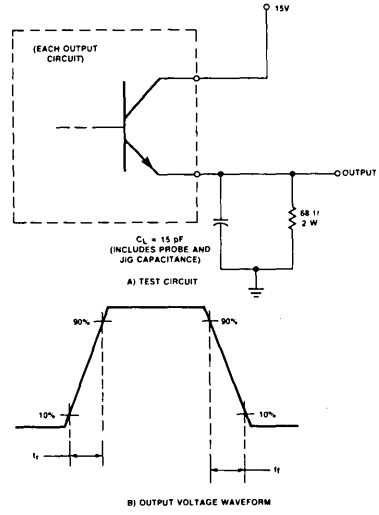
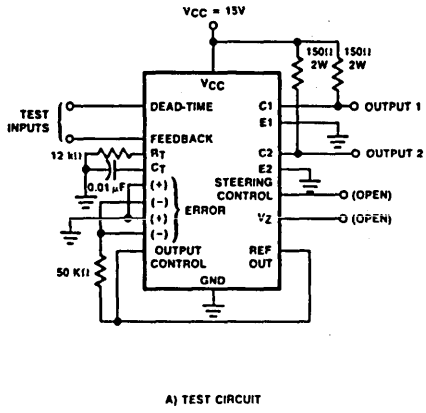


Figure 2. Emitter-Follower Configuration



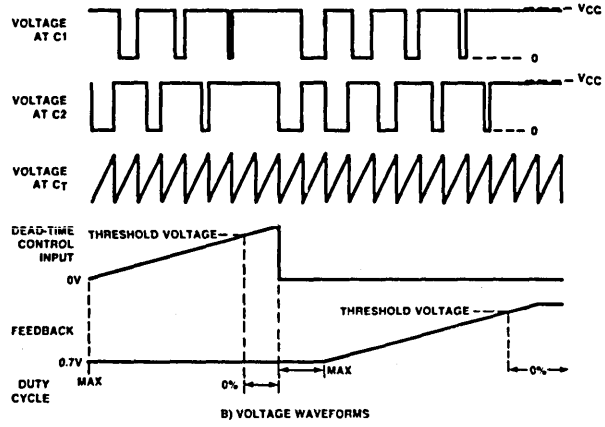
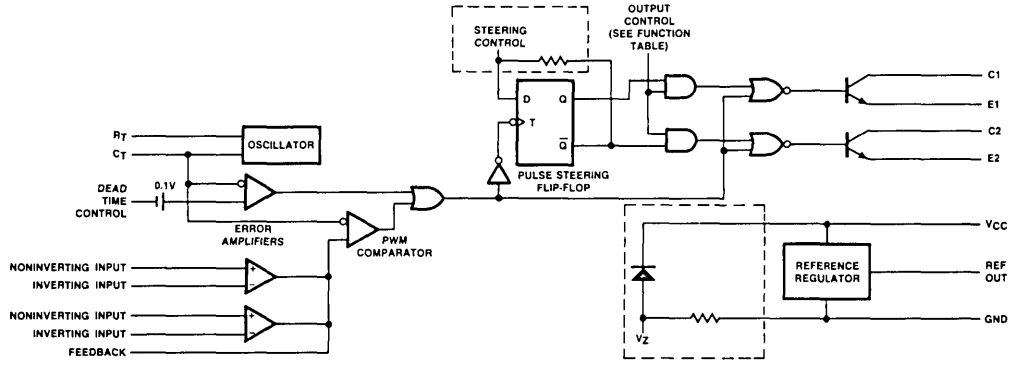


Figure 3. Dead-Time and Feedback Control



EQUIVALENT SCHEMATIC DIAGRAM

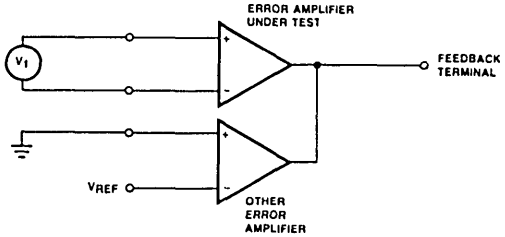
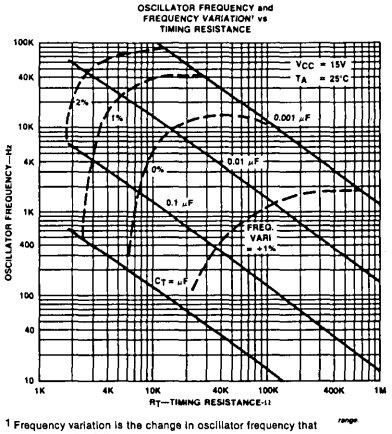


Figure 4. Error Amplifier Characteristics

FUNCTION TABLE

INPUTS		OUTPUT FUNCTION
OUTPUT CONTROL	STEERING INPUT	
Grounded	Open	Single-ended or parallel output
At V_{ref}	Open	Normal push-pull operation
At V_{ref}	$V_I < 0.4V$	PWM Output at Q1
At V_{ref}	$V_I > 0.4V$	PWM Output at Q2



[1] Frequency variation is the change in oscillator frequency that occurs over the full temperature range.

Figure 5. Oscillator Frequency and Frequency Variation[1] vs Timing Resistance

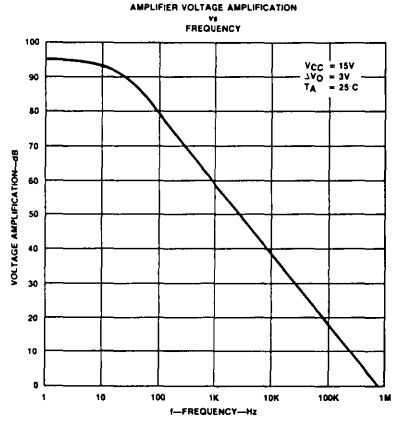


Figure 6. Amplifier Voltage Amplification vs Frequency

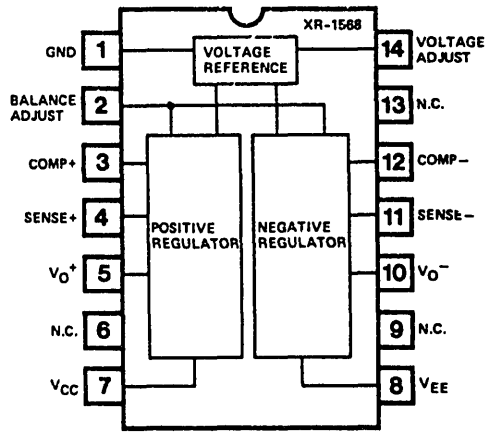
Dual-Polarity Tracking Voltage Regulator

GENERAL DESCRIPTION

The XR-1468/1568 is a dual polarity tracking voltage regulator, internally trimmed for symmetrical positive and negative 15V outputs. Current output capability is 100 mA, and may be increased by adding external pass transistors. The device is intended for local "on-card" regulation, which eliminates the distribution problems associated with single point regulation.

The XR-1468CN and XR-1568N are guaranteed over the 0°C to 70°C commercial temperature range. The XR-1568M is rated over the full military temperature range of −55°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Internally Set for ±15V Outputs
±100 mA Peak Output Current
Output Voltages Balanced Within 1% (XR-1568)
0.06% Line and Load Regulation
Low Stand-By Current
Output Externally Adjustable from ±8 to ±20 Volts
Externally Adjustable Current Limiting
Remote Sensing

ORDERING INFORMATION

Part Number	Temperature	Output Offset	Package
XR-1568M	−55°C to +125°C	±150 mV max	Ceramic
XR-1568N	0°C to +70°C	±150 mV max	Ceramic
XR-1468CN	0°C to +70°C	±300 mV max	Ceramic

APPLICATIONS

Main Regulation in Small Instruments
On-Card Regulation in Analog and Digital Systems
Point-of-Load Precision Regulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	±30 Volts
Minimum Short-Circuit Resistance	4.0 Ohms
Load Current, Peak	±100 mA
Power Dissipation	
Ceramic (N) Package	1.0 Watt
Derate Above +25°C	6.7 mW/°C
Operating Temperature	
XR-1568M	−55°C to +125°C
XR-1568/XR-1468C	0°C to +70°C
Storage Temperature	−65°C to +150°C

SYSTEM DESCRIPTION

The XR-1468/1568 is a dual polarity tracking voltage regulator combining two separate regulators with a common reference element in a single monolithic circuit, thus providing a very close balance between the positive and negative output voltages. Outputs are internally set to ±15 Volts but can be externally adjusted between ±8.0 to ±20 Volts with a single control. The circuit features ±100 mA output current, with externally adjustable current limiting, and provision for remote voltage sensing.

ELECTRICAL CHARACTERISTICS

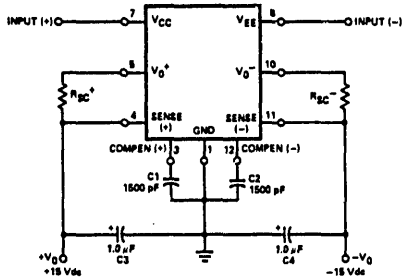
Test conditions: (V_{CC} = +20V, V_{EE} = −20V, C1 = C2 = 1500 pF, C3 = C4 = 1,0 μF, $R_{SC}^+ = R_{SC}^-$ = 4.0Ω. $I_L^+ = I_L^-$ = 0, T_C = +25°C unless otherwise noted.)

PARAMETERS	XR-1468C			XR-1568			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	14.5	15	15.5	14.8	15	15.2	Vdc
Input Voltage	—	—	30	—	—	30	Vdc
Input-Output Voltage Differential	2.0	—	—	2.0	—	—	Vdc
Output Voltage Balance	—	±50	±300	—	±50	±150	mV
Line Regulation Voltage (V_{in} = 18V to 30V) (T_L† to T_H)††	 — —	 — —	 10 20	 — —	 — —	 10 20	mV
Load Regulation Voltage (I_L = 0 to 50 mA, T_J = constant) (T_A = T_L to T_H)	 — —	 — —	 10 30	 — —	 — —	 10 30	mV
Output Voltage Range	8.0	—	20	8.0	—	20	Vdc
Ripple Rejection (f = 120 Hz)	—	75	—	—	75	—	dB
Output Voltage Temperature Stability (T_L to T_H)	—	0.3	1.0	—	0.3	1.0	%
Short-Circuit Limit (R_{SC} = 10 ohms)	—	60	—	—	60	—	mA
Output Noise Voltage (BW = 10 Hz − 10 kHz)	—	100	—	—	100	—	μV(rms)
Positive Standby Current (V_{in} = +30V)	—	2.4	4.0	—	2.4	4.0	mA
Negative Standby Current (V_{in} = −30V)	—	1.0	3.0	—	1.0	3.0	mA
Long-Term Stability	—	0.2	—	—	0.2	—	%/kHr

†T_L = 0°C for XR-1468C/1568
= −55°C for XR-1568M

††T_H = +70°C for XR-1468C/1568
= +125°C for XR-1568M

T_J = Junction Temp.
T_C = Case Temp.



C1 and C2 should be located as close to the device as possible. A 0.1 μF ceramic capacitor may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

C3 and C4 may be increased to improve load transient response and to reduce the output noise voltage. At low temperature operation, it may be necessary to bypass C4 with a 0.1 μF ceramic disc capacitor.

Figure 1. Basic 50 mA Regulator

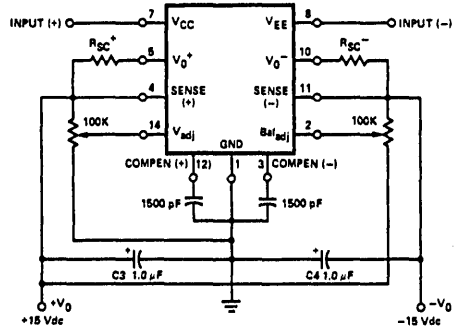


Figure 2. Voltage Adjust and Balance Adjust Circuit

Pulse-Width Modulating Regulator

GENERAL DESCRIPTION

The XR-1524 family of monolithic integrated circuits contain all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The XR-1524 is specified for operation over the full military temperature range of −55°C to +125°C, while the XR-2524 and XR-3524 are designed for commercial applications of 0°C to +70°C.

FEATURES

Direct Replacement for SG-1524/2524/3524
Complete PWM power control circuitry
Single ended or push-pull outputs
Line and load regulation of 0.2%
1% maximum temperature variation
Total supply current less than 10 mA
Operation beyond 100 kHz

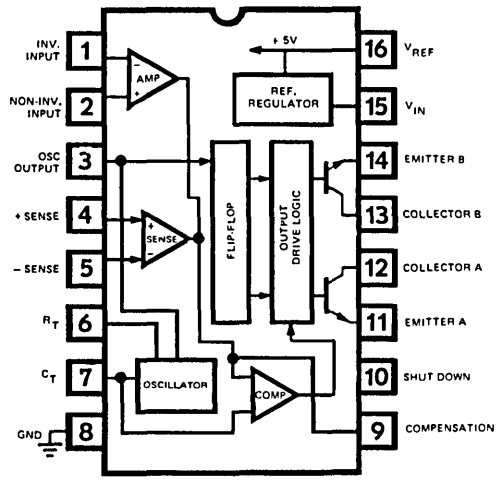
APPLICATIONS

Switching Regulators
Pulse-width Modulated Power Control Systems

ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Output Current (each output)	100 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	8 mW/°C
Plastic Package	625 mW/°C
Derate above +25°C	5 mW/°C
Operating Temperature Range	
XR-1524	−55°C to +125°C
XR-2524/XR-3524	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1524M	Ceramic	−55°C to +125°C
XR-2524N	Ceramic	0°C to +70°C
XR-2524P	Plastic	0°C to +70°C
XR-3524N	Ceramic	0°C to +70°C
XR-3524P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-1524/2524/3524 pulse width modulating regulator is a complete monolithic switching regulator. An internal 5V reference, capable of supplying up to 50 mA to external loads, provides an on board operating standard. The oscillator frequency and duty cycle are adjusted by an external RC network. Regulation is controlled by an error amplifier which, combined with the sense amplifier, also allows current limiting and remote shutdown functions. The outputs of the XR-1524/2524/3524 are two identical NPN transistors with both emitters and collectors uncommitted. Each output transistor has antisaturation circuitry for fast response and local current limiting set at 100 mA.

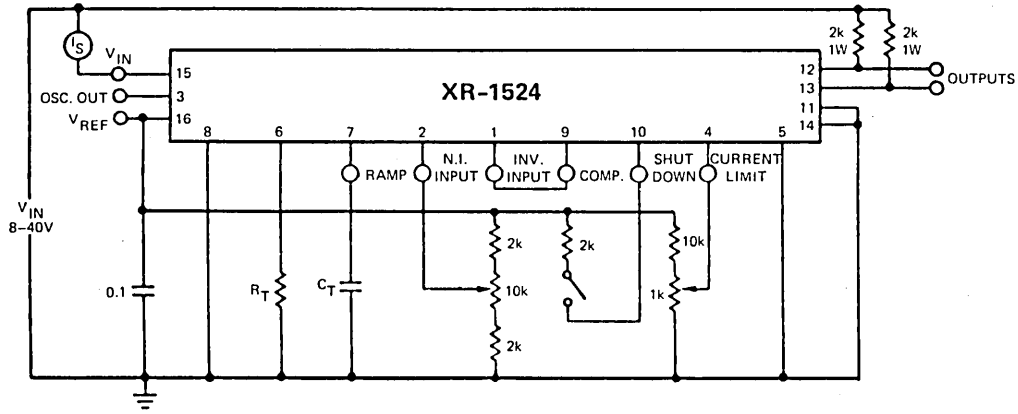
ELECTRICAL SPECIFICATIONS

Test Conditions: T_A = −55°C to +125°C for the XR-1524 and 0°C to +70°C for the XR-2524 and XR-3524, V_{IN} = 20V, and f = 20 kHz, unless specified otherwise.

PARAMETERS	XR-1524/ XR-2524			XR-3524			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
REFERENCE SECTION								
Output Voltage	4.8	5.0	5.2	4.6	5.0	5.4	V	
Line Regulation		10	20		10	30	mV	V_{IN} = 8 to 40 Volts
Load Regulation		20	50		20	50	mV	I_L = 0 to 20 mA
Ripple Rejection		66			66		dB	f = 120 Hz, T_A = 25°C
Short Circuit Current Limit		100			100		mA	V_{REF} = 0, T_A = 25°C
Temperature Stability		0.3	1		0.3	1	%	Over Operating Temperature Range
Long Term Stability		20			20		mV/khr	T_A = 25°C
OSCILLATOR SECTION								
Maximum Frequency		300			300		kHz	C_T = .001 μF, R_T = 2 KΩ
Initial Accuracy		5			5		%	R_T and C_T constant
Voltage Stability			1			1	%	V_{IN} = 8 to 40 Volts, T_A = 25°C
Temperature Stability			2			2	%	Over Operating Temperature Range
Output Amplitude		3.5			3.5		V	Pin3, T_A = 25°C
Output Pulse Width		0.5			0.5		μS	C_T = .01 mfd, T_A = 25°C
ERROR AMPLIFIED SECTION								
Input Offset Current			2		2		μA	
Input Offset Voltage		0.5	5		2	10	mV	V_{CM} = 2.5 Volts
Input Bias Current		2	10		2	10	μA	V_{CM} = 2.5 Volts
Open Loop Voltage Gain	72	80		60	80		dB	
Common Mode Voltage	1.8		3.4	1.8		3.4	V	T_A = 25°C
Common Mode Rejection Ratio		70			70		dB	T_A = 25°C
Small Signal Bandwidth		3			3		MHz	A_V = 0 dB, T_A = 25°C
Output Voltage	0.5		3.8	0.5		3.8	V	T_A = 25°C
COMPARATOR SECTION								
Duty Cycle	0		45	0		45	%	% Each Output On
Input Threshold		1			1		V	Zero Duty Cycle
Input Threshold		3.5			3.5		V	Max. Duty Cycle
Input Bias Current		1			1		μA	
CURRENT LIMITING SECTION								Pin 9 = 2V with Error Amplifier
Sense Voltage	190	200	210	180	200	220	mV	Set for Max. Out, T_A = 25°C
Sense Voltage Temp. Coef.		0.2			0.2		mV/°C	
Common Mode Voltage	−1		+1	−1		+1	V	
OUTPUT SECTION (Each Output)								
Max. Collector-Emitter Voltage	40			40			V	
Collector Leakage Current		0.1	50		0.1	50	μA	V_{CE} = 40V
Saturation Voltage		1	2		1	2	V	I_C = 50 mA
Emitter Output Voltage	17	18		17	18		V	V_{IN} = 20V
Rise Time		0.2			0.2		μS	R_C = 2 KΩ, T_A = 25°C
Fall Time		0.1			0.1		μS	R_C = 2 KΩ, T_A = 25°C
TOTAL STANDBY CURRENT (Excluding oscillator charging current, error and current limit dividers, and with outputs open)		8	10		8	10	mA	V_{IN} = 40V

5

OPEN LOOP TEST CIRCUIT



DESCRIPTION OF CIRCUIT OPERATION

VOLTAGE REFERENCE SECTION

The internal voltage reference and regulator section provides a 5-volt reference output at pin 16. This voltage also serves as a regulated voltage source for the internal timing and control circuitry. This regulator may be bypassed for operation from a fixed 5-volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5-volt source for other circuitry. It will provide up to 50 mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 2.

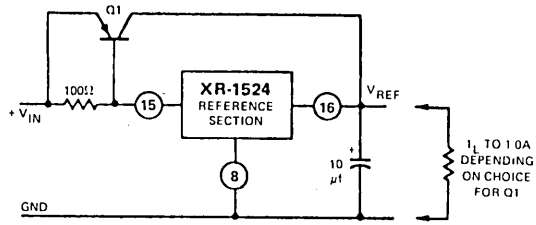


Figure 2. Using the Internal Regulator as 5V Power Supply for External Circuitry

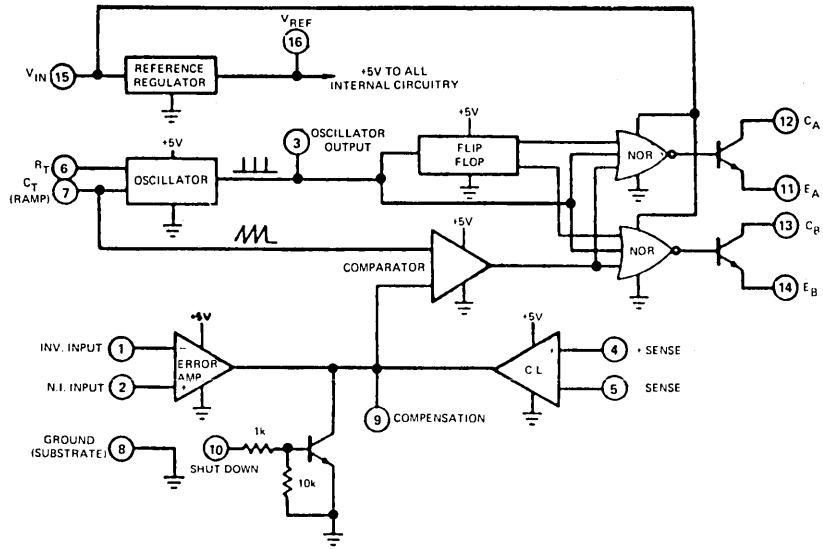


Figure 1. Detailed System Block Diagram of XR-1524

OSCILLATOR SECTION

The oscillator section in the XR-1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6V ÷ R_T and should be kept within the range of approximately 30 μA to 2 mA, i.e., 1.8K < R_T < 100K.

The oscillator period is approximately T = R_TC_T where T is in microseconds when R_T = ohms and C_T = microfarads.

The use of Figure 3 allows the selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0 – 90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 – 45% and the overall frequency is 1/2 that of the oscillator.

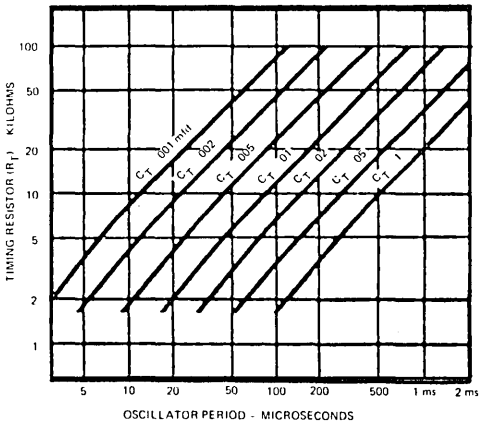


Figure 3. Oscillator Period as a Function of R_T and C_T

The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 4. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (≈ 100 pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 μF.

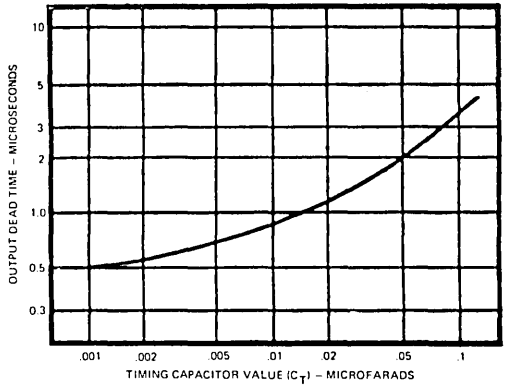


Figure 4. Output Stage Dead Time as a Function of the Timing Capacitor Value

If it is desired to synchronize the XR-1524 to an external clock, a pulse of ≈ +3 volts may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more XR-1524 circuits must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T (slave) = 1/2 C_T (master). Then connecting pin 3 on all units together will insure that the master output pulse – which occurs first and has a wider pulse width – will reset the slave units.

ERROR AMPLIFIER SECTION

The error amplifier is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high-impedance node (R_L ≈ 5 MΩ). The gain is

$$A_V = g_m R_L = \frac{8\, I_C\, R_L}{2kT} \approx .002\, R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 5.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 5 show the uncompensated amplifier with a single pole at approximately 200 Hz and a unity gain cross-over at 5 MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50 KΩ plus .001 μF.

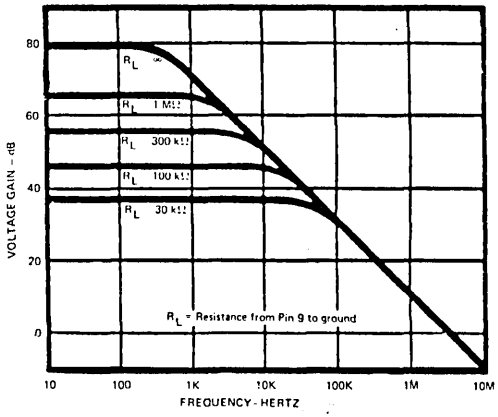


Figure 5. Error Amplifier Frequency Response as a Function of External Resistor, R_L, at Pin 9

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200 μA can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5-volt reference voltage must be divided down as shown in Figure 6. The error amplifier may also be used in fixed duty cycle applications by using the unit gain configuration shown in the open loop test circuit.

CURRENT LIMITING CONTROLS

The current limiting circuitry of the XR-1524 is shown in Figure 7.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1,

$$\text{Threshold} = V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2) = I_1 R_2 \simeq 200 \text{ mV}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300 Hertz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

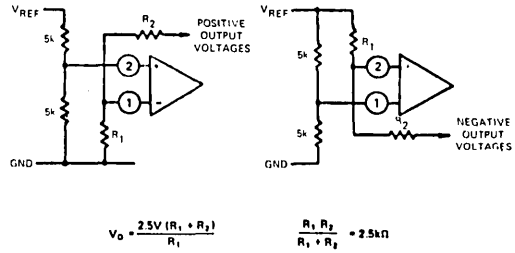


Figure 6. Error Amplifier Biasing Circuits. *(Note: Change in Input Connections for Opposite Polarity Outputs)*

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 15.) Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal, i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 8. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

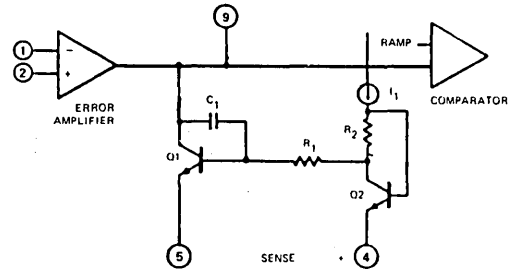


Figure 7. Current Limiting Circuitry of the XR-1524

OUTPUT CIRCUITS

The outputs of the XR-1524 are two identical NPN transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry for fast response, and current limiting set for a maximum output current of approximately 100 mA. The availability of both collectors and emitters allows maximum versatility to enable driving either NPN or PNP external transistors.

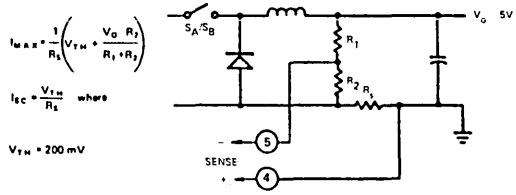


Figure 8. Foldback Current Limiting Can Be Used to Reduce Power Dissipation Under Shorted Output Conditions

In considering the application of the XR-1524 to voltage regulator circuitry, there are a multitude of output configurations possible. In general, however, they fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

Examples of each category are shown in Figures 9, 10 and 11. In each case, the switches indicated can be either the output transistors in the XR-1524 or added external transistors according to the load current requirements.

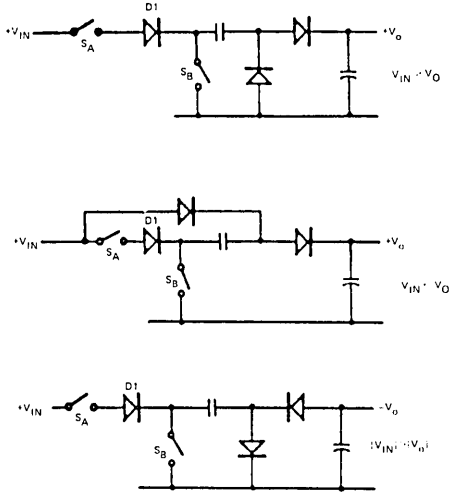


Figure 9. Capacitor-Diode Coupled Voltage Multiplier Output Stages. *(Note: Diode D1 is Necessary to Prevent Reverse Emitter-Base Breakdown of Transistor Switch S_A)*

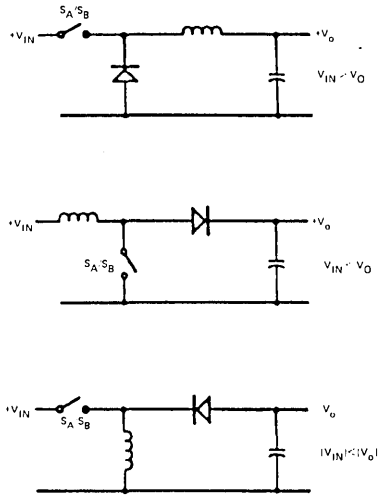
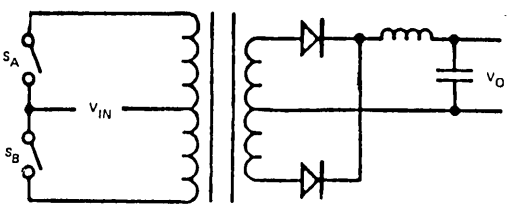
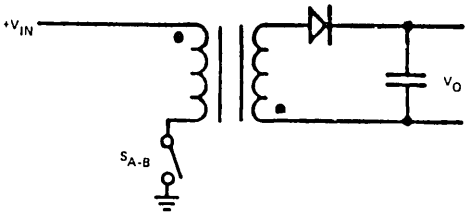


Figure 10. Single-ended Inductor Circuits Where the Two Outputs of the XR-1524 are Connected in Parallel



(a) Push-Pull



(b) Flyback

Figure 11. Push-Pull and Flyback Connections for Transformer-Coupled Outputs

5

DEADBAND CONTROL

The XR-1524 pulse width modulating regulator provides two outputs which alternate in turning on for push-pull inverter applications. The internal oscillator sends a momentary blanking pulse to both outputs at the end of each period to provide a deadband so that there cannot be a condition when both outputs are on at the same time. The amount of deadband is determined by the width of the blanking pulse appearing on pin 3 and can be controlled by any one of the four techniques described below:

Method 1: For 0.2 to 2.0 microseconds, the deadband is controlled by the timing capacitor, C_T, on pin 7. The relationship between C_T and deadband is shown in Figure 4. Of course, since C_T also helps determine the operating frequency, the range of control is somewhat limited.

Method 2: For 0.5 to 5.0 microseconds, the blanking pulse may be extended by adding a small capacitor from pin 3 to ground. The value of the capacitor must be less than 1000 pF or triggering will become unreliable.

Method 3: For longer and more well-controlled blanking pulses, a simple one-shot latch similar to the circuit shown in Figure 12 should be used.

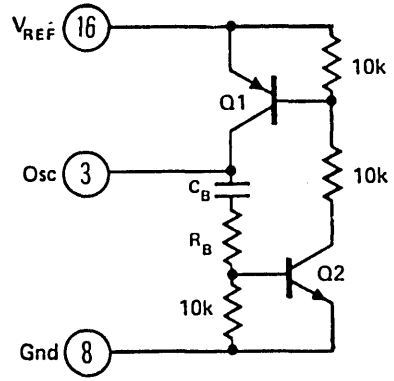


Figure 12. Recommended External Circuitry for Long Duration Blanking Pulse Generation (Method 3 of Deadband Control. *Note: For 5 μsec blanking, choose C_B = 200 pF, R_B = 10 KΩ)*

When this circuit is triggered by the oscillator output pulse, it will latch for a period determined by C_BR_B providing a well-defined deadband.

Another use for this circuit is as a buffer when several other circuits are to be synchronized to one master oscillator. This one-shot latch will provide an adequate signal to insure that all the slave circuits are completely reset before allowing the next timing period to begin.

Note that with this circuit, the blanking pulse holds off the oscillator so its width must be subtracted from the overall period when selecting R_T and C_T

Method 4: Another way of providing greater deadband is just to limit the maximum pulse width. This can be done by using a clamp to limit the output voltage from the error amplifier. A simple way of achieving this clamp is with the circuit shown in Figure 13.

This circuit will limit the error amplifier's voltage range since its current source output will only supply 200 μA. Additionally, this circuit will not affect the operating frequency.

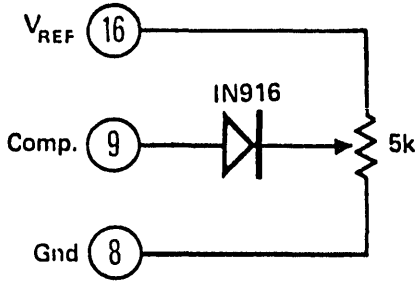


Figure 13. Using a Clamp Diode to Control Deadband (Method 4 of Deadband Control)

APPLICATIONS INFORMATION

POLARITY CONVERTING REGULATOR

The XR-1524 pulse width modulating regulator can be interconnected as shown in Figure 14. The component values shown in the figure are chosen to generate a -5 volt regulated supply voltage from a +15 volt input. This circuit is useful for an output current of up to 20 mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

FLYBACK CONVERTER

Figure 15 shows the application of XR-1524 in a low-current DC-DC converter, using the flyback converter principle (see Figure 11b). The particular values given in the figure are chosen to generate ±15 volts at 20 mA from a +5 volt regulated line. The reference generator in the XR-1524 is unused. The reference is provided by the input voltage. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

SINGLE ENDED REGULATOR

The XR-1524 operates as an efficient single-ended pulse width modulating regulator, using the circuit connection shown in Figure 16. In this configuration, the two output transistors of the circuit are connected in parallel by shorting pins (12, 13) and (11, 14) together, respectively, to provide for effective 0 – 90% duty-cycle modulation. The use of an output inductance requires an R-C phase compensation on pin 9, as shown in the figure.

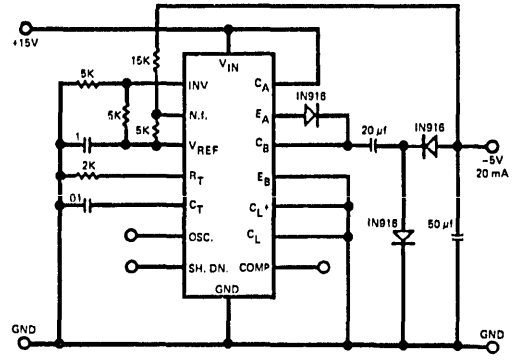


Figure 14. Circuit Connection for Polarity Converting Regulator (V_{in} = +15V, V_{out} = −5V)

PUSH-PULL CONVERTER

The circuit of Figure 17 shows the use of XR-1524 in a transformer-coupled DC-DC converter with push-pull outputs (see Figure 11a). Note that the oscillator must be set at twice the desired output frequency as the XR-1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done in the primary. This causes the pulse/width to be reduced automatically if the transformer saturation occurs.

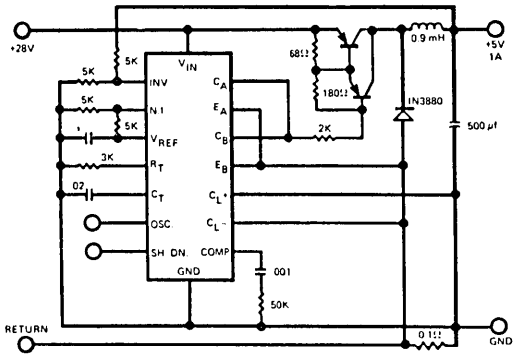


Figure 16. Conventional Single-Ended Regulator Connection (V_{in} = +28V, V_o = +5V, I_{out} ≤ 1 Amp)

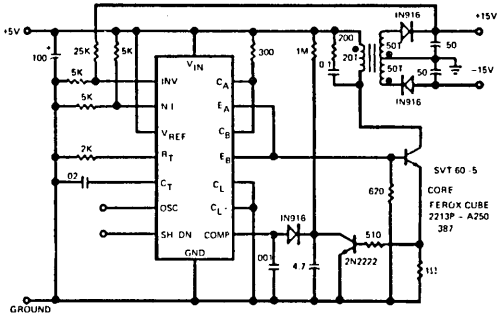


Figure 15. A Low-Current DC-DC Converter Using Flyback Principle (V_{out} = ±15V, V_{in} = +5V, I_L ≤ 20 mA)

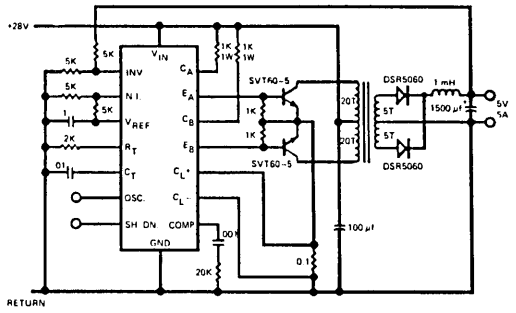


Figure 17. A High-Current DC-DC Converter with Push-Pull Outputs (V_{in} = +28V, V_o = +5V, I_o ≤ 5A)

Pulse-Width Modulating Regulators

GENERAL DESCRIPTION

The XR-1525A/1527A is a series of monolithic integrated circuits that contain all of the control circuitry necessary for a pulse-width modulating regulator. Included in the 16-Pin dual-in-line package is a voltage reference, an error amplifier, a pulse-width modulator, an oscillator, under-voltage lockout, soft-start circuitry, and output drivers.

The XR-1525A/2525A/3525A series features NOR logic, giving a LOW output for an OFF state. The XR-1527A/2525A/3527A series features OR logic, giving a HIGH output for an OFF state.

FEATURES

8V to 35V Operation
5.1V Reference Trimmed to ±1%
100 Hz to 500 kHz Oscillator Range
Separate Oscillator Sync Terminal
Adjustable Deadtime Control
Internal Soft-Start
Input Under-voltage Lockout
Latching PWM to Prevent Double Pulsing
Dual Source/Sink Output Drivers
  Capable of Over 200 mA
Power-FET Drive Capability

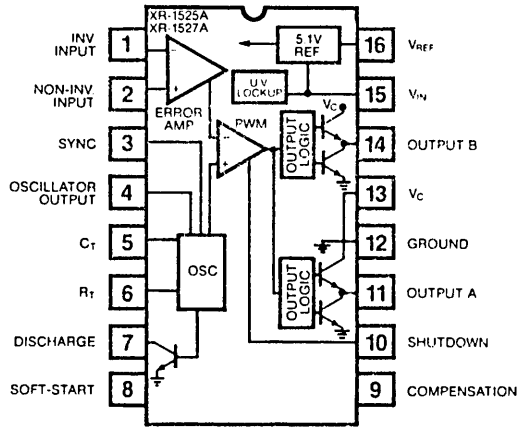
APPLICATIONS

Power Control Systems
Switching Regulators
Industrial Controls

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+ V_{IN})	+40V
Collector Supply Voltage (V_C)	+40V
Logic Inputs	−0.3V to 5.5V
Analog Inputs	−0.3V to +V_{IN}
Output Current, Source or Sink	500 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate above T_A = +25°C	8.0 mW/°C
Plastic Package	625 mW
Derate above T_A = +25°C	5.0 mW/°C
Operating Junction Temperature (T_J)	+150°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1525A/27M	Ceramic	−55°C to +125°C
XR-2525A/27AN	Ceramic	−25°C to +85°C
XR-2525A/27AP	Plastic	−25°C to +85°C
XR-3525A/27CN	Ceramic	0°C to +70°C
XR-3525A/27CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The on-chip 5.1-volt reference is trimmed to ±1% initial accuracy, and the common-mode input range of the error amplifier is extended to include the reference voltage. Deadtime is adjustable with a single external resistor. A sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external clock. A positive-going signal applied to the shutdown pin provides instantaneous turnoff of the outputs. The under-voltage lockout circuitry keeps the output drivers off, and the soft-start capacitor discharged, for an input voltage below the required value. The latch on the PWM comparator insures the outputs are active only once per oscillator period, thereby eliminating any double pulsing. The latch is reset with each clock pulse.

The output drivers are totem-pole designs capable of sinking and sourcing over 200 mA.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{IN} = +20V, T_J = Full operating temperature range, unless otherwise specified.

PARAMETERS	XR-1525A/2525A XR-1527A/2527A			XR-3525A XR-3527A			UNIT	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
VOLTAGE REFERENCE SECTION								
Output Voltage	5.05	5.10	5.15	5.00	5.10	5.20	V	T_J = 25°C
Line Regulation		10	20		10	20	mV	V_{IN} = 8V to 35V
Load Regulation		20	50		20	50	mV	I_L = 0 to 20 mA
Temperature Stability (2)		20	50		20	50	mV	T_J = Full Operating Range
Total Output Variation (2)	5.00		5.20	4.95		5.25	V	Line, Load and Temperature
Output Short Circuit Current		80	100		80	100	mA	T_J = 25°C, V_{ref} = 0V
Output Noise Voltage (2)		40	200		40	200	μV rms	T_J = 25°C, 10 Hz ≤ f ≤ 10 kHz
Long Term Stability (2)		20	50		20	50	mV/kHR	T_J = 125°C
OSCILLATOR SECTION (Note 3)								
Initial Accuracy (2,3)		±2	±6		±2	±6	%	T_J = 25°C, f = 40 kHz
Temperature Stability (2)		±3	±6		±3	±6	%	T_J = Full Operating Range
Input Voltage Stability (2,3)		±0.3	±1		±1	±2	%	V_{IN} = 8V to 35V
Minimum Frequency			100			100	Hz	R_T = 150 kΩ, C_T = 0.1 μF
Maximum Frequency	400			400			kHz	R_T = 2 kΩ, C_T = 1 nF
Current Mirror	1.7	2.0	2.2	1.7	2.0	2.2	mA	I_{RT} = 2 mA
Clock Amplitude (2,3)	3.0	3.5		3.0	3.5		V	
Clock Pulse Width (2,3)	0.3	0.5	1.0	0.3	0.5	1.0	μsec	T_J = 25°C, R_D = 0Ω
Sync Threshold	1.2	2.0	2.8	1.2	2.0	2.8	V	
Sync Input Current		1.0	2.5		1.0	2.5	mA	Sync Voltage = 3.5V
ERROR AMPLIFIER SECTION (V_{CM} = 5.1V)								
Input Offset Voltage		0.5	5.0		2	10	mV	
Input Bias Current		1	10		1	10	μA	
Input Offset Current			1			1	μA	
DC Open-Loop Gain	60	75		60	75		dB	R_L ≥ 10 MΩ
Gain Bandwidth Product (2)	1	2		1	2		MHz	T_J = 25°C
Output Low Voltage		0.2	0.5		0.2	0.5	V	
Output High Voltage	3.8	5.6		3.8	5.6		V	
Common-Mode Rejection Ratio	60	75		60	75		dB	V_{CM} = 1.5V to 5.2V
Supply Voltage Rejection Ratio	50	60		50	60		dB	V_{IN} = 8V to 35V
PULSE-WIDTH MODULATING COMPARATOR								
Minimum Duty Cycle			0			0	%	
Maximum Duty Cycle	45	49		45	49		%	
Input Threshold (3)	0.6	0.9		0.6	0.9		V	Zero Duty Cycle
Input Threshold (3)		3.3	3.6		3.3	3.6	V	Maximum Duty Cycle
Input Bias Current (2)		0.05	1.0		0.05	1.0	μA	
SOFT-START SECTION								
Soft-Start Current	25	50	80	25	50	80	μA	$V_{shutdown}$ = 0V
Soft-Start Voltage		0.4	0.6		0.4	0.6	V	$V_{shutdown}$ = 2V
Shutdown Input Current		0.4	1.0		0.4	1.0	mA	$V_{shutdown}$ = 2.5V
OUTPUT DRIVERS (Each Output) V_C = 20V								
Output Low Voltage		0.2	0.4		0.2	0.4	V	I_{sink} = 20 mA
Output Low Voltage		1.0	2.0		1.0	2.0	V	I_{sink} = 100 mA
Output High Voltage	18	19		18	19		V	I_{source} = 20 mA
Output High Voltage	17	18		17	18		V	I_{source} = 100 mA
Under-voltage Lockout	6	7	8	6	7	8	V	V_{comp} and V_{SS} = High
Collector Leakage (4)			200			200	μA	V_C = 35V
Rise Time (2)		100	600		100	600	nsec	T_J = 25°C, C_L = 1 nF
Fall Time (2)		50	300		50	300	nsec	T_J = 25°C, C_L = 1 nF
Shutdown Delay (2)		0.2	0.5		0.2	0.5	μsec	V_{SD} = 3V, C_S = 0, T_J = 25°C
TOTAL STANDBY CURRENT								
Supply Current		14	20		14	20	mA	V_{IN} = 35V

Note 2: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
Note 3: Tested at f = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0Ω).
Note 4: Applies to XR-1525A/2525A/3525A only, due to polarity of output pulses.

PRINCIPLES OF OPERATION

The different control blocks within the XR-1525A/1527A function as follows:

Voltage Reference Section

The internal voltage reference circuit of the XR-1525A/1527A is based on the well-known "band-gap" reference, with a nominal output voltage of 5.1 volts, internally trimmed to ±1% accuracy. It is short circuit protected and is capable of providing up to 20 mA of reference current. A simplified circuit schematic is shown in Figure 7.

Oscillator Section

The sawtooth oscillator derives its frequency from an external timing resistor/capacitor pair. The timing resistor, R_T, determines the charging current into the timing capacitor, C_T. The magnitude of this current is approximately given by:

$$\frac{V_{ref} - 2V_{BE}}{R_T} \approx \frac{3.7V}{R_T}$$

where R_T may range from 2 kΩ to 150 kΩ. In general, temperature stability is maximized with lower values of R_T. The current source charging C_T creates a linear ramp voltage which is compared to fixed thresholds within. When the capacitor voltage reaches +3.3 volts, the oscillator output (Pin 4) goes high, turning ON the discharge transistor. The capacitor is discharged through the deadtime resistor, R_D. When the voltage on C_T falls to +1.0 volt, the oscillator output goes low, the discharge transistor is turned OFF, and the capacitor is charged through the constant current source as another cycle starts. With large values of R_D (500Ω, maximum), deadtime is increased. The actual operating frequency is thus a function of the charge and discharge times. Figure 2 shows how charge time is related to R_T and C_T, with R_D = 0Ω. Deadtime is a function of R_D and C_T, and can vary between 0.5 to 7 μsec, with R_D = 0Ω, as shown in Figure 3. The equivalent circuit schematic of the oscillator section is shown in Figure 8.

A unit can be synchronized to an external source by selecting its free-running oscillator period to be 10% longer than the period of the external source. A positive-going pulse of at least 300 nsec wide should be applied to the sync terminal for reliable triggering; however, it should not exceed the free-running pulse width by more than 200 nsec. The amplifier of the pulse should be kept between 2 and 5 volts. Multiple units can be synchronized to each other by connecting all C_T pins, and oscillator output pins together; R_T pins and discharge pins on slave oscillators must be left open.

Error Amplifier

The error amplifier of the XR-1525A/1527A is a differential input transconductance amplifier. Its common-mode range covers the reference voltage. Its open-loop gain, typically 75 dB, can be reduced by a load resistor on Pin 9. To ensure proper operation, the output load should be limited to 50 kΩ or greater. An equivalent circuit schematic of the error amplifier is shown in Figure 9.

Soft-Start Circuitry

The soft-start function is provided to achieve controlled turn-on of the pulse-width modulator. When power is applied to the device, the external capacitor, $C_{soft-start}$, on Pin 8 is charged by a 50 μA constant current source. The ramp voltage appearing on this capacitor is fed into the pulse-width modulator, which gradually increases its output duty cycle from zero to the prescribed value. When the shutdown terminal is raised to a positive value, an internal transistor turns ON, and discharges the capacitor, C_S, causing the PWM to turn OFF. When the shutdown terminal is open or pulled low, the transistor turns OFF, and C_S begins charging as before. The turn-on time (time required to charge C_S to +2.7 volts) can be approximated as:

$$T_C \text{ (msec)} = 54\ C_S$$

where C_S is in μF.

Output Section

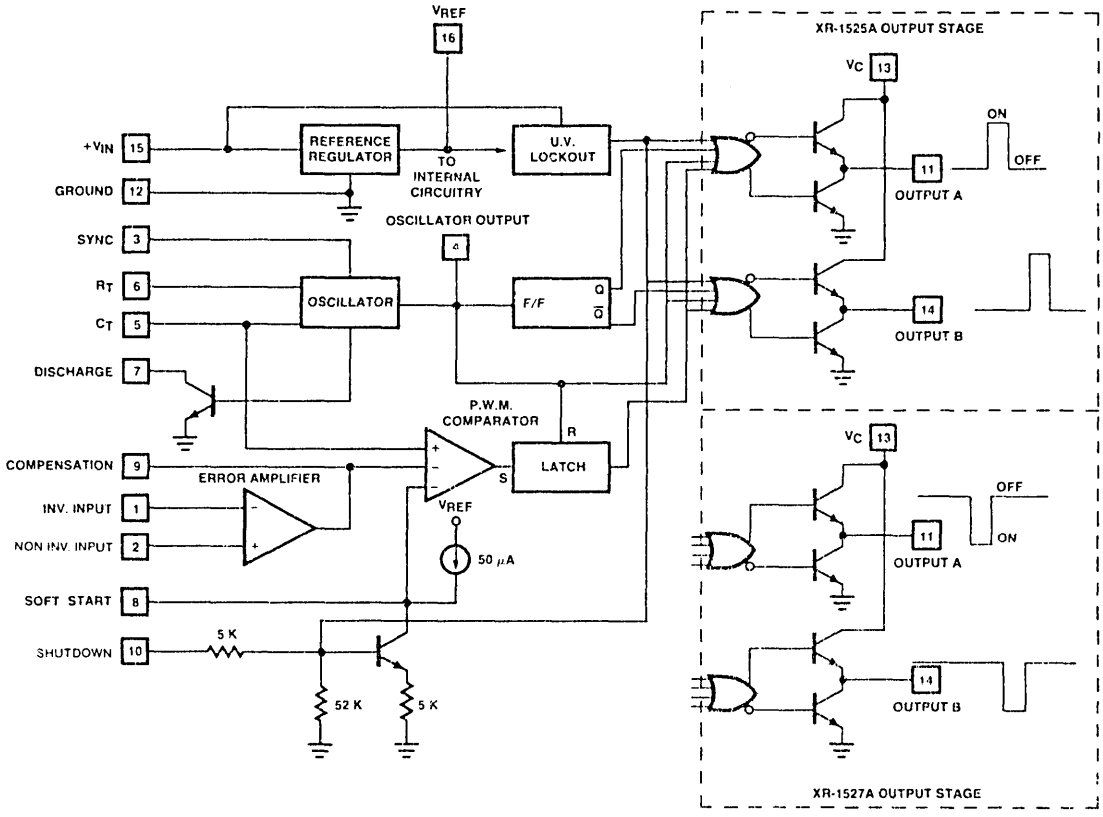
The output drivers of the XR-1525A/1527A are totem-pole designs capable of sinking and sourcing 200 mA. The low source impedance in the high or low states provides ideal interfacing with bipolar as well as FET power transistors. Either push-pull or single-ended output configurations are possible with separate collector supply terminals. The equivalent schematic of the output drivers is shown in Figure 10.

RECOMMENDED OPERATING CONDITIONS

Note 1: Range over which the device is functional and parameter limits are guaranteed.

Collector Supply Voltage (V_C)	+4.5V to +35V
Sink/Source Load Current (Steady State)	0 to 100 mA
Sink/Source Load Current (Peak)	0 to 400 mA
Reference Load Current	0 to 20 mA
Oscillator Frequency Range	100 Hz to 400 kHz
Oscillator Timing Resistor	2 kΩ to 150 kΩ
Oscillator Timing Capacitor	0.001 μF to 0.1 μF
Deadtime Resistor Range	0 to 500Ω

EQUIVALENT SCHEMATIC DIAGRAM



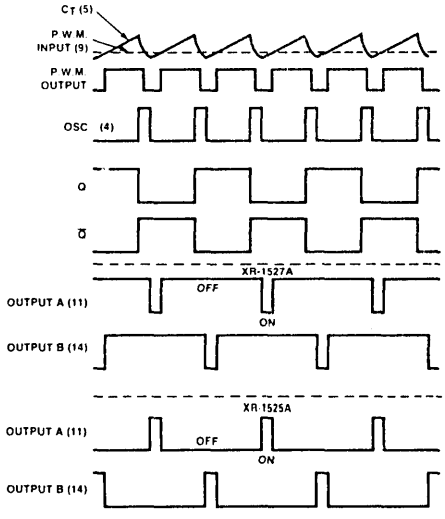


Figure 1: Typical Waveforms—XR-1525A/1527A

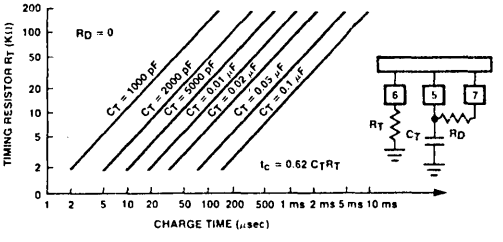


Figure 2. Oscillator Charge Time vs R_T and C_T

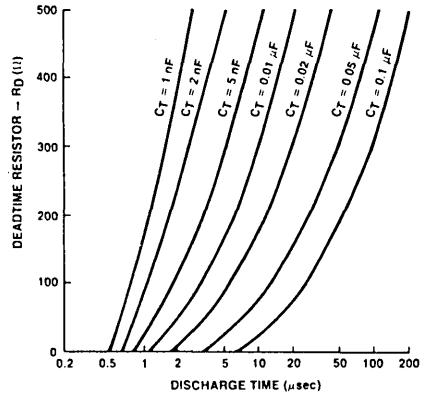


Figure 3. Oscillator Discharge Time vs R_D and C_T

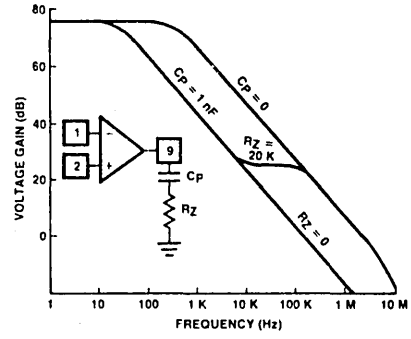


Figure 4. Error Amplifier Open-Loop Frequency Response.

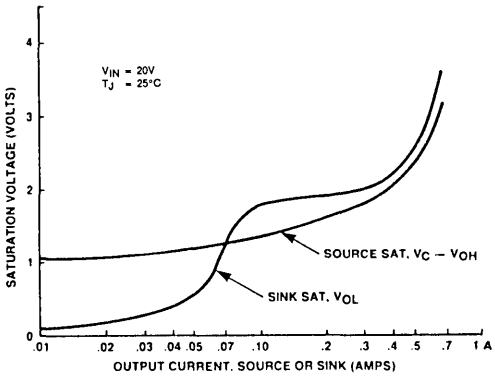


Figure 5. Output Saturation Characteristics

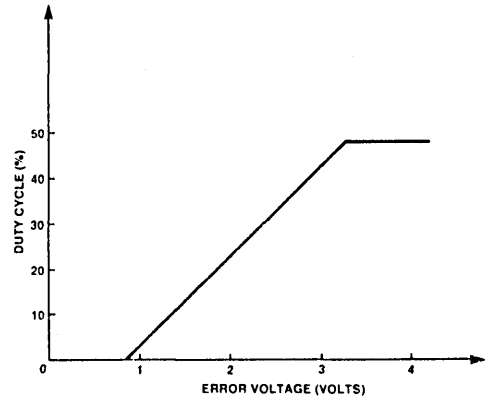


Figure 6. Output Duty Cycle vs Error Voltage

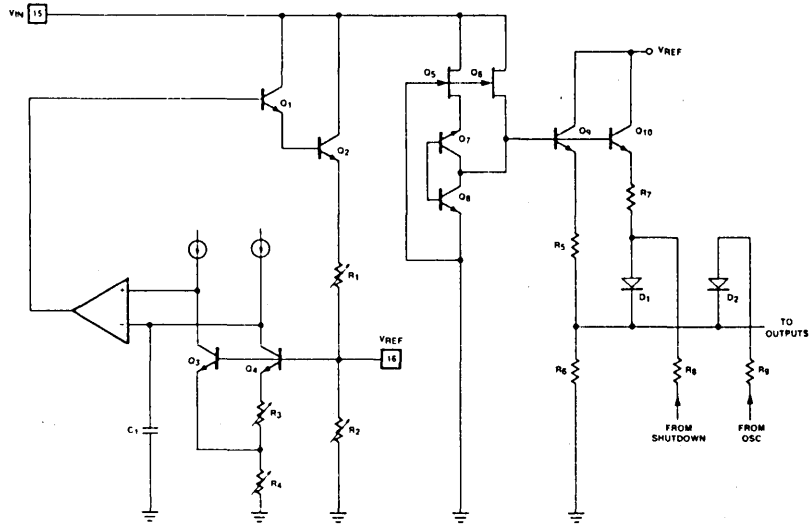


Figure 7. Equivalent Schematic of Voltage Reference Section

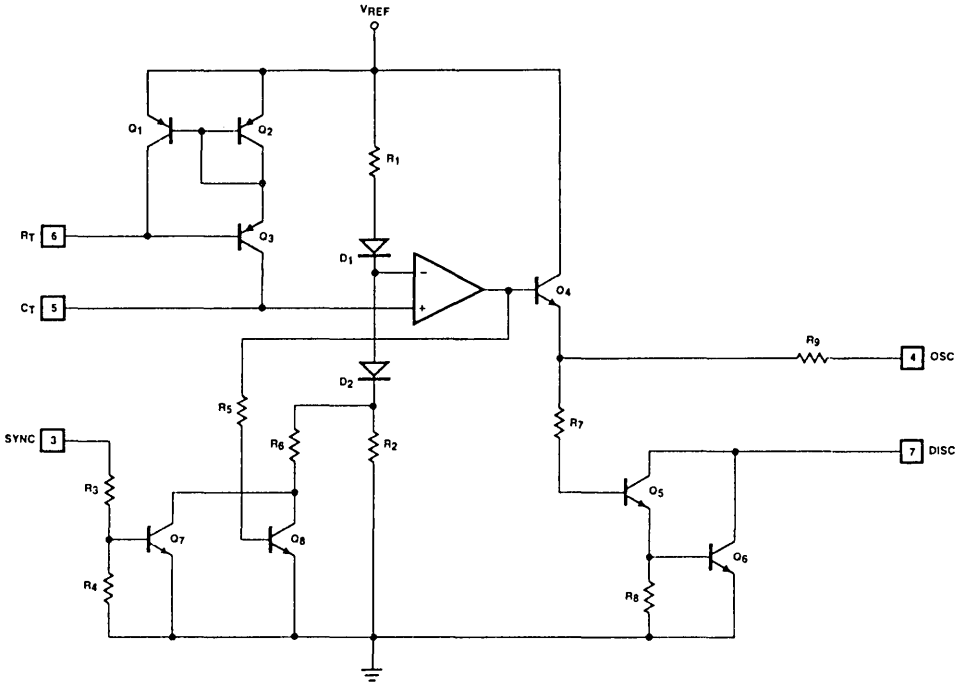


Figure 8. Equivalent Schematic of the Oscillator Section

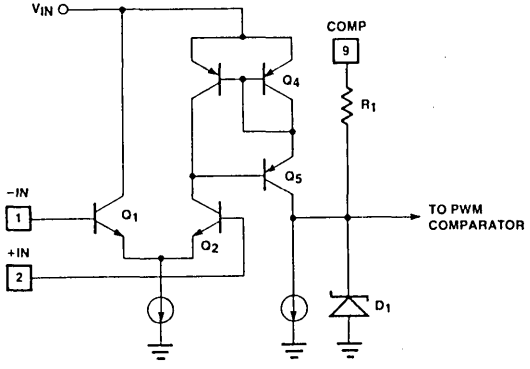


Figure 9. Equivalent Schematic of Error Amplifier Section

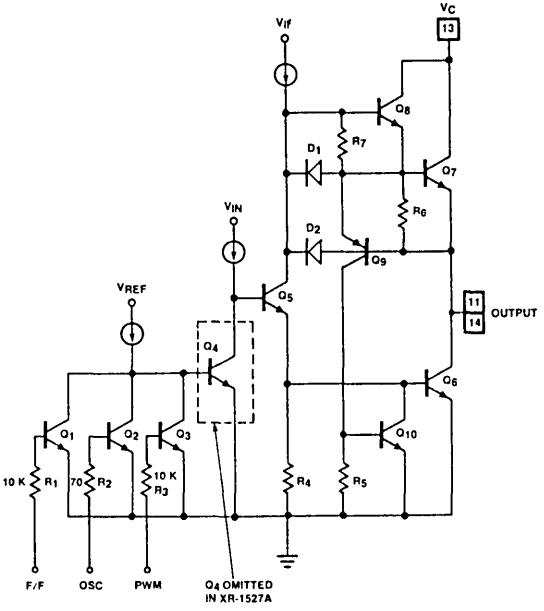


Figure 10. Equivalent Schematic of Output Drivers

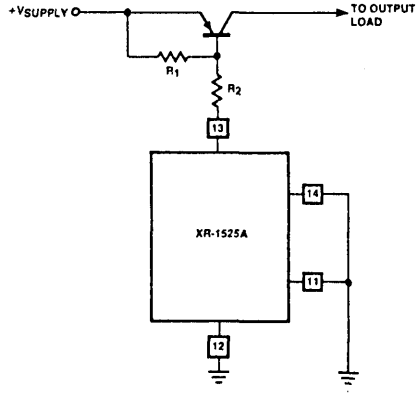


Figure 11. Single-Ended Output for XR-1525A

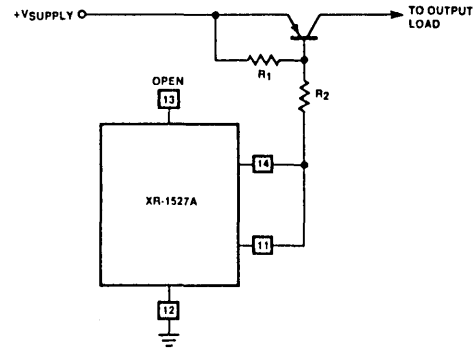


Figure 12. Single-Ended Output for XR-1527A

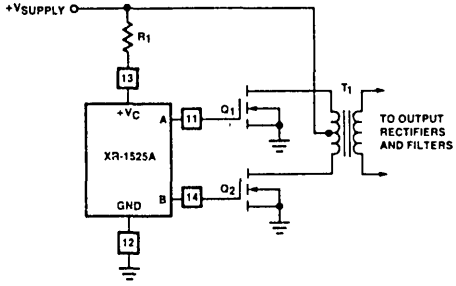


Figure 13. Push-Pull Outputs with XR-1525A

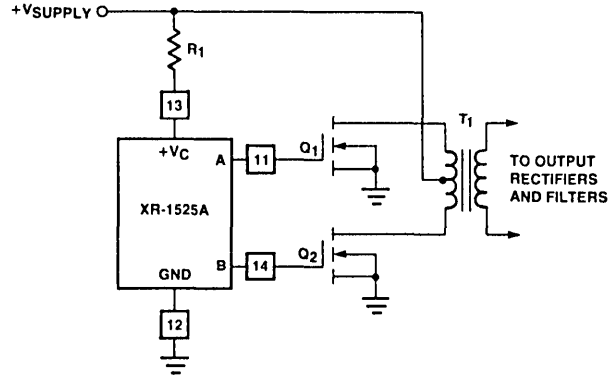


Figure 14. Power FET Push-Pull Outputs with XR-1525A

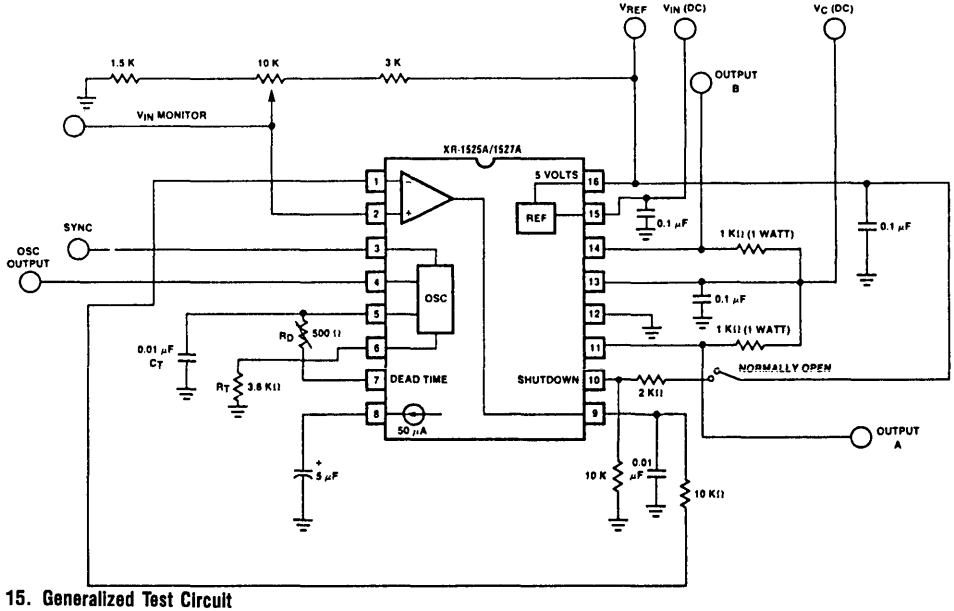


Figure 15. Generalized Test Circuit

Power Supply Output Supervisory Circuit

GENERAL DESCRIPTION

The XR-1543/2543/3543 are monolithic integrated circuits that contain all the functions necessary to monitor and control the output of a power supply system. Included in the 16-Pin dual-in-line package is a voltage reference, an operational amplifier, voltage comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage sensing, under-voltage sensing and current limiting, with provisions for triggering an external SCR "crowbar."

The internal voltage reference on the XR-1543 is guaranteed for an accuracy of ± 1% to eliminate the need for external potentiometers. The entire circuit may be powered from either the output that is being monitored or from a separate bias voltage.

FEATURES

Over-Voltage Sensing Capability	
Under-Voltage Sensing Capability	
Current Limiting Capability	
Reference Voltage Trimmed	±1%
SCR "Crowbar" Drive	300 mA
Programmable Time Delays	
Open Collector Outputs and Remote Activation Capability	
Total Standby current	Less than 10 mA

APPLICATIONS

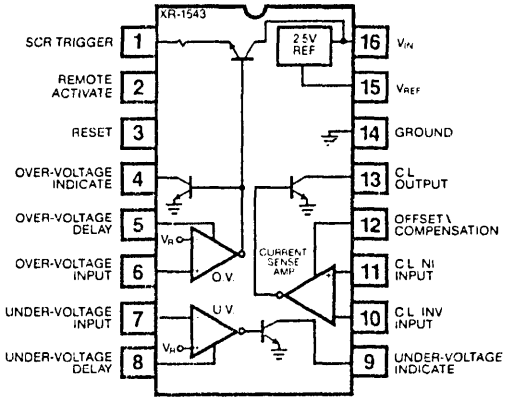
DC/DC Converters
Switch Mode Power Supplies
Power Line Monitors
Linear Power Supplies

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage, V_{IN}	40V
Sense Inputs	V_{IN}
SCR Trigger Current (Note 1)	300 mA
Indicator Output Voltage	40V
Indicator Output Sink Current	50 mA
Power Dissipation (Ceramic)	1000 mW
Derate Above T_A = +25°C	8 mW/°C
Power Dissipation (Plastic)	625 mW
Derate Above T_A = +25°C	5 mW/°C
Operating Junction Temperature (T_J)	+150°C
Storage Temperature Range	−65°C to +150°C

Note 1: At higher input voltages, a dissipation limiting resistor, R_G, is required.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1543M	Ceramic	−55°C to +125°C
XR-2543N	Ceramic	−25°C to +85°C
XR-3543N	Ceramic	0°C to +70°C
XR-3543P	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

An output supervisory circuit, such as the XR-1543, is used to control and monitor the performance of a power supply. In many systems, it is crucial that the supply voltage is always within some minimum and maximum level, to guarantee proper performance, and to prevent damage to the system. If the supply voltage is out of tolerance, it is often desirable to shut down the system or to have some form of indication to the operator or system controller. As well as protecting the system, the power supply sometimes needs to be protected under short circuit and current overload situations. By providing an SCR "crowbar" on the output of a power supply, it can be shut off under certain fault conditions as well.

The over-voltage sensing circuit (O.V.) can be used to monitor the output of a power supply and provide triggering of an SCR, when the output goes above the prescribed voltage level. The under-voltage sensing circuit (U.V.) can be used to monitor either the output of a power supply or the input line voltage.

XR-15/25/3543

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{IN} = 10V, T_A = full operating temperature range, unless otherwise specified. Refer to Figure 9 for component designation.

PARAMETERS	XR-1543/2543 MIN	XR-1543/2543 TYP	XR-1543/2543 MAX	XR-3543 MIN	XR-3543 TYP	XR-3543 MAX	UNIT	CONDITIONS
Input Voltage Range	4.5		40	4.5		40	V	T_A = 25°C to max
Input Voltage Range	4.7		40	4.7		40	V	T_A = min to max
Supply Current		7	10		7	10	mA	T_A = 25°C, V_{IN} = 40V
REFERENCE VOLTAGE SECTION (Pins 15 and 16)								
Output Voltage	2.48	2.50	2.52	2.45	2.50	2.55	V	T_A = 25°C
Output Voltage	2.45		2.55	2.40		2.60	V	T_A = min to max
Line Regulation		1	5		1	5	mV	V_{IN} = 5 to 30V
Load Regulation		1	10		1	10	mV	I_{ref} = 0 to 10 mA
Short Circuit Current		15			15		mA	V_{ref} = 0V
Temperature Stability		50			50		ppm/°C	
SCR TRIGGER SECTION (Pins 1, 2, and 3)								
Peak Output Current	100	200	400	100	200	400	mA	V_{IN} = 5V, R_G = 0Ω, V_O = 0
Peak Output Voltage	12	13		12	13		V	V_{IN} = 15V, I_O = 100 mA
Output OFF Voltage		0	0.1		0	0.1	V	V_{IN} = 40V
Remote Activate Current		0.4	0.8		0.4	0.8	mA	Pin 2 = GND
Remote Activate Voltage		2	6		2	6	V	Pin 2 = Open
Reset Current		0.4	0.8		0.4	0.8	mA	Pin 2 = GND, Pin 3 = GND
Reset Voltage		2	6		2	6	V	Pin 2 = GND, Pin 3 = Open
Output Current Slew Rate		400			400		mA/μs	T_J = 25°C, R_L = 50Ω, C_D = 0
Propagation Delay Time (From Pin 2)		300			300		nsec	T_J = 25°C, R_L = 50Ω C_D = 0, Pin 2 = 0.4V
Propagation Delay Time (From Pin 6)		500			500		nsec	T_J = 25°C, R_L = 50Ω, C_D = 0, Pin 6 = 2.7V
COMPARATOR SECTIONS (Pins 4, 5, 6, 7, 8, and 9)								
Input Threshold (Input Voltage Rising on Pin 6 and	2.45	2.50	2.55	2.40	2.50	2.60	V	T_J = min to max
Falling on Pin 7)	2.40		2.60	2.35		2.65	V	T_J = 25°C
Input Hysteresis		25			25		mV	
Input Bias Current		0.3	1.0		0.3	1.0	μA	Sense input = 0V
Delay Saturation		0.2	0.5		0.2	0.5	V	
Delay High Level		6	7		6	7	V	
Delay Charging Current	200	250	300	200	250	300	μA	V_D = 0V
Indicate Saturation Voltage		0.2	0.5		0.2	0.5	V	I_L = 10 mA
Indicate Leakage Current		0.01	1.0		0.01	1.0	μA	V_{out} = 40V
Propagation Delay Time		400			400		nsec	C_D = 0 Pin 6 = 2.7V Pin 7 = 2.3V
Propagation Delay Time		10			10		msec	C_D = 1 μF T_J = 25°C
CURRENT LIMIT AMPLIFIER SECTION (Pins 10, 11, 12, and 13)								
Input Voltage Range	0		$V_{IN}-3V$	0		$V_{IN}-3V$	V	
Input Bias Current		0.3	1.0		0.3	1.0	μA	Pin 12 = Open, V_{CM} = 0V
Input Offset Voltage		0	10		0	15	mV	Pin 12 = Open, V_{CM} = 0V
Input Offset Voltage	80	100	120	70	100	130	mV	Pin 12 = 10 kΩ to GND
Common Mode Rejection Ratio	60	70		60	70		dB	V_{IN} = 15V, 0≤ V_{CM} ≤ 12V
Open Loop Gain	72	80		72	80		dB	V_{CM} = 0V, Pin 12 = Open
Output Saturation Voltage		0.2	0.5		0.2	0.5	V	I_L = 10 mA
Output Leakage Current		0.01	1.0		0.01	1.0	μA	V_{out} = 40V
Small Signal Bandwidth		5			5		MHz	T_J = 25°C, Av = 0 dB
Propagation Delay Time		200			200		nsec	T_J = 25°C, $V_{overdrive}$ = 100 mV

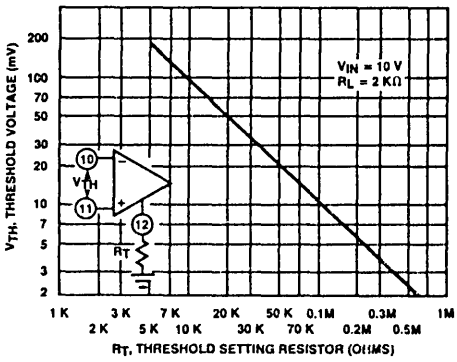


Figure 1. Typical Current Threshold (V_{TH}) vs. Threshold Setting Resistor (R_T)

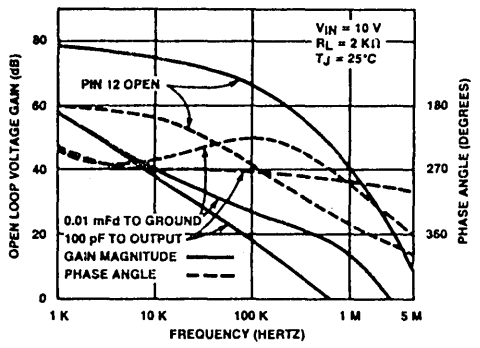


Figure 2. Current Limiting Amplifier—Frequency Response

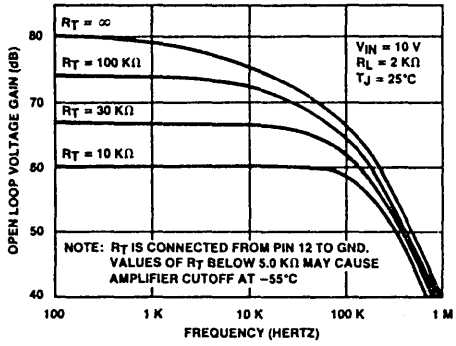


Figure 3. Current Limiting Amplifier Gain vs. Threshold Setting Resistor (R_T

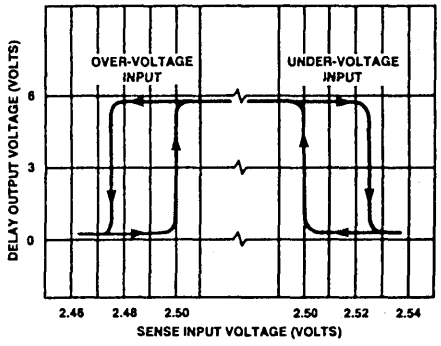


Figure 4. Over-Voltage and Under-Voltage Comparator Hysteresis

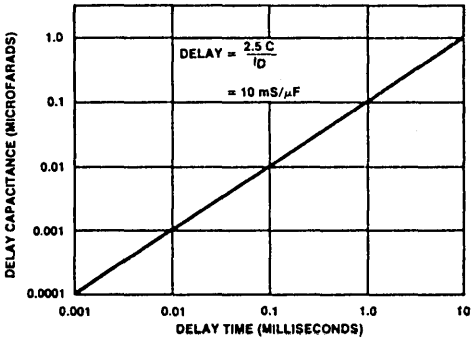


Figure 5. Comparator Activation Delay vs. Capacitor Value

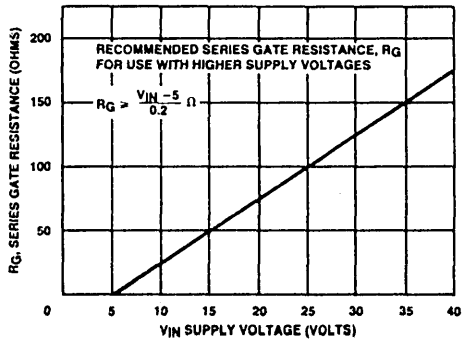


Figure 6. SCR Trigger—Series Gate Resistance (R_G) vs. Input Voltage

PRINCIPLES OF OPERATION

The internal control blocks of the XR-1543 operate as follows:

Voltage Reference Section

The internal voltage reference circuit of the XR-1543 is based on the well-known "band-gap reference" with a nominal output voltage of 2.50 volts, internally trimmed to give an accuracy of ± 1% at 25°C. It is capable of providing a stable output voltage over a wide input voltage range. Furthermore, its performance is guaranteed for changes in line and load conditions. The accuracy of the output voltage is guaranteed to ± 2% maximum for the XR-1543/2543, and ± 4% maximum for the XR-3543, over the entire operating temperature range.

The output of the reference circuit is capable of providing up to 10 mA of current for use as a reference for external circuitry. The primary function of this circuit is to provide a very accurate and stable reference input for the under-voltage and over-voltage comparators, thereby enabling very precise monitoring of line and output voltages without potentiometers.

Comparator Section

The under-voltage and over-voltage sensing comparators of the XR-1543 are identical except for the input polarities. Each section is made up of two comparators in series whose inputs are referenced to 2.50 volts. The delay terminal between the comparators requires an external capacitor to ground for programmable time delays on the output.

When an out-of-tolerance situation occurs, the first comparator activates a current source which then charges the external capacitor at a constant rate. This ramp voltage is then compared to the reference voltage by the second comparator which activates the output indicating circuit. With no external capacitor, the overall time delay from sense input to output is approximately 0.5 μsec. The charging current for the capacitor, C_D, is approximately 250 μA which results in the following relationship:

$$\text{Time delay} = 10\ C_D\ (\text{msec})$$

where C_D is in μF.

The output npn transistors are capable of sinking 10 mA with saturation voltage of less than 0.4 volts. The outputs can be "wired OR'd" to provide a single output indicator.

Current Sensing Amplifier

The operational amplifier used in the XR-1543 is a high-gain, externally compensated amplifier with open collector outputs. The pnp input stage provides for a wide input common mode range extending from ground to approximately 3 volts below the positive supply. With a 2 kΩ pull-up resistor, the open-loop voltage gain is 72 dB minimum with a unity gain bandwidth beyond 5 MHz. The operational amplifier may be used as a comparator or, if linear amplification is required, external compensation may be added for stable performance over a wide frequency range.

The input offset voltage of this amplifier is specified for 10 mV maximum; however, it may be programmed externally for thresholds up to 200 mV. By connecting a resistor, R_T, from Pin 12 to ground, the input threshold voltage can be varied. For most current sensing applications, the required threshold polarity calls for a positive voltage on the inverting input. Reducing the impedance on Pin 12 also lowers the overall voltage gain of the amplifier, which makes this pin a convenient point to apply frequency compensation. This can be accomplished by either connecting C_1 to the output, or C_2 to ground as shown in Figure 8. The diode, D_1, and the resistor, R_C, are used only if it is necessary to increase the frequency response by operating the output at a higher current and/or isolating the load from R_C and C_1, when the amplifier is off.

SCR Trigger Section

The SCR trigger sectionof the XR-1543 is connected to the output of the over-voltage comparator and is capable of handling 300 mA. The circuit also provides for remote activation of the output as well as a reset terminal. When an over-voltage situation occurs, the output of the sensing comparator goes low, turning "on" the over-voltage indicate transistor. At the same time, the comparator drives an npn Darlington pair which provides 300 mA to activate an external SCR crowbar.

A remote activation circuit is included to allow the user to activate the SCR crowbar in other than an over-voltage situation. When this terminal, Pin 2, is grounded, it forces the output of the comparator low which activates the output circuitry in the same manner as the over-voltage comparator does.

Another function of this circuit is to provide the capability to latch the O.V. indicate and SCR trigger outputs "on", after a fault is sensed. This is done by connecting the remote activate terminal (Pin 2) to the O.V. indicating terminal (Pin 4). When an O.V. condition occurs, Pin 2 is pulled low, which in turn holds the outputs in the "on" condition until the reset terminal is externally grounded, removing the latch and turning "off" the outputs. If the external connection is not made, the high current output will be activated only as long as a fault condition exists. When the fault condition disappears, the outputs will be disabled. The thresholds for both remote activation and reset terminals are approximately 1.2 volts.

EQUIVALENT SCHEMATIC DIAGRAM

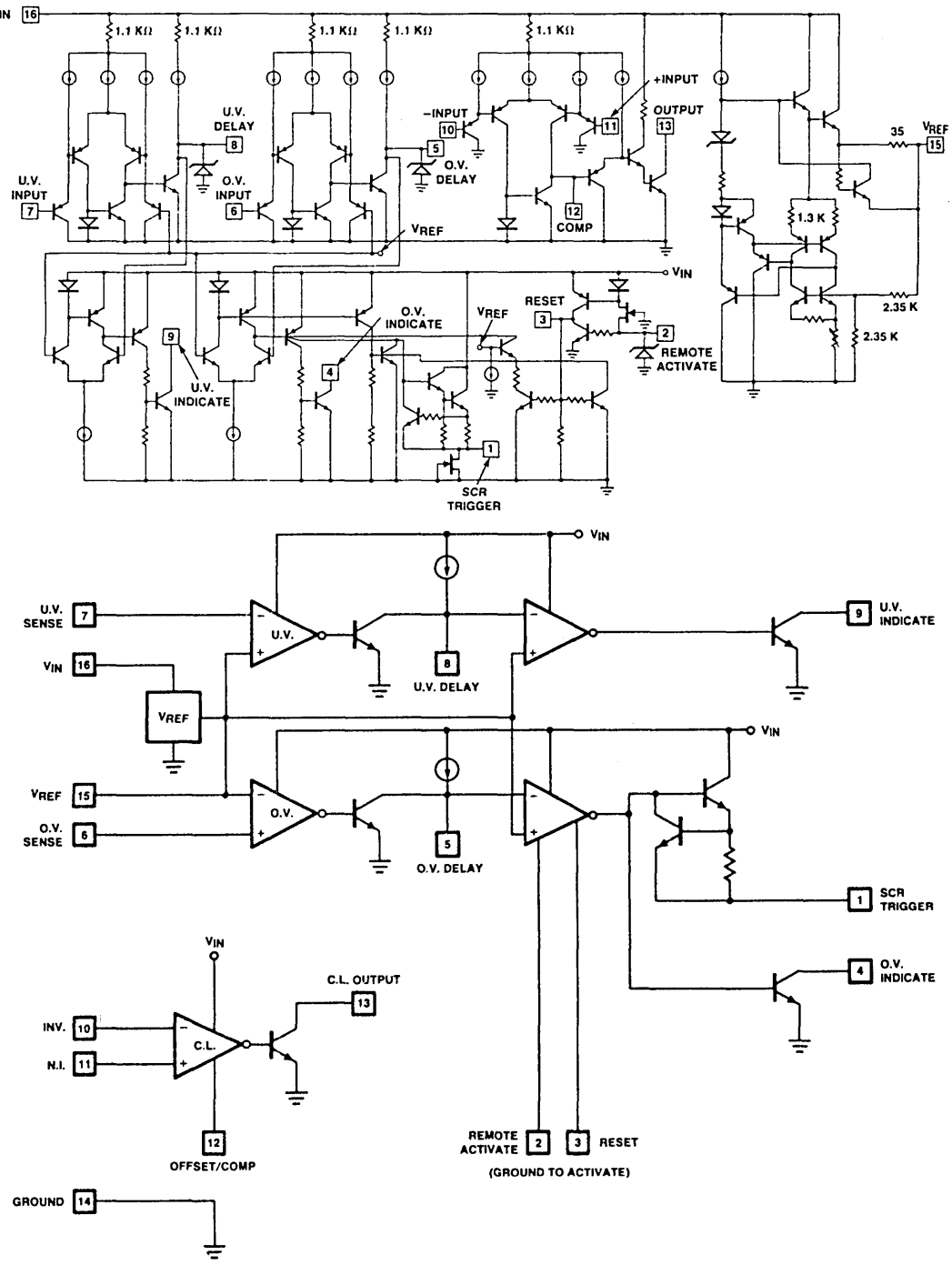


Figure 7. XR-1543 Block Diagram

APPLICATIONS INFORMATION

A typical application of the XR-1543 is to monitor a single power supply output voltage as shown in Figure 9. In this circuit, both over- and under-voltage sensing and current-limiting functions are performed. The circuit shown is powered from an external bias capable of supplying 10 mA in addition to the activation current for the SCR trigger. With Pin 2 tied to Pin 4, a latch has been provided such that when an over-voltage situation occurs, the o.v. indicator and SCR trigger are activated and held until the reset terminal is externally grounded.

In powering an SCR from supply voltages greater than 5 volts, an external resistor, R_G, is required on Pin 1 to limit the power dissipation for the XR-1543. Although the XR-1543 is capable of handling 300 mA of current, its power dissipation must be kept below the absolute maximum ratings.

In this circuit, current-limiting is performed by sensing the voltage drop across the resistor, R_{SC}, in the positive supply line. The threshold for the amplifier is externally set by the resistor, R_T

The values of the external components used in Figure 9 are calculated as follows:

1. Current limiting threshold, $V_{TH} \approx \frac{1000}{R_T}$
2. C_1 is determined by the loop dynamics.
3. Peak current to load,

$$I_p \approx \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}}\left(\frac{R_2}{R_2 + R_3}\right)$$

4. Short circuit current,

$$I_{SC} = \frac{V_{TH}}{R_{SC}}$$

5. Low output voltage limit,

$$V_O \text{ (low)} = \frac{2.5(R_4 + R_5 + R_6)}{R_5 + R_6}$$

6. High output voltage limit,

$$V_O \text{ (high)} = \frac{2.5(R_4 + R_5 + R_6)}{R_6}$$

7. Voltage sensing delay, $T_D = 10{,}000\ C_D$
8. SCR trigger power limiting resistor,

$$R_G > \frac{V_{IN} - 5}{0.2}$$

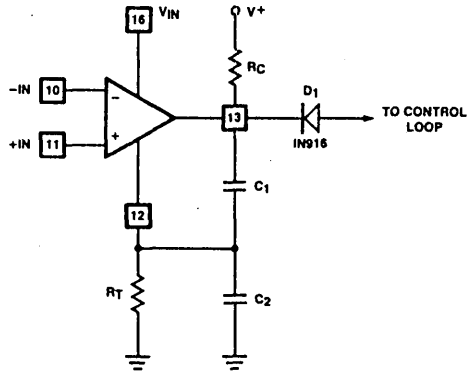


Figure 8. Current Limiting Amplifier Connections for Threshold Control and Frequency Compensation

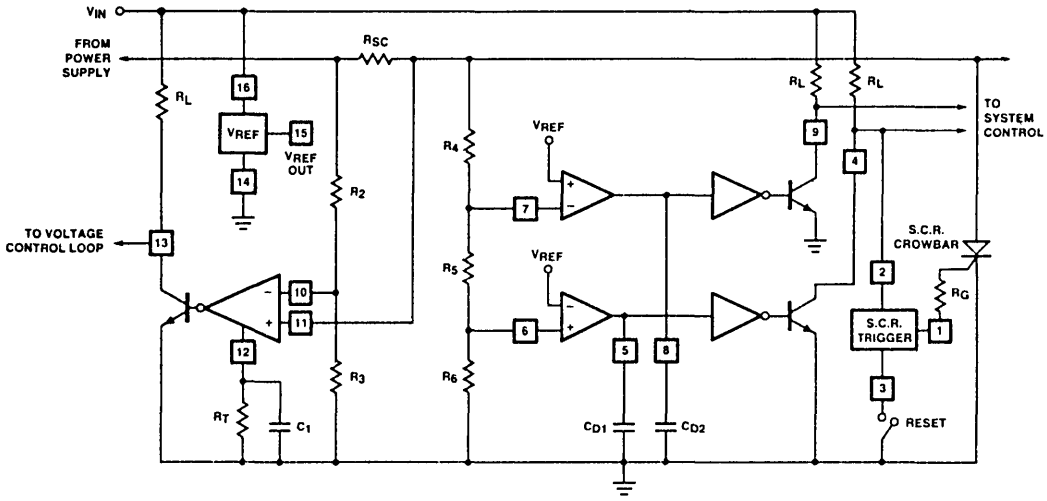


Figure 9. Typical Connection for Linear Foldback Current Limiting as well as Over-Voltage and Under-Voltage Protection.

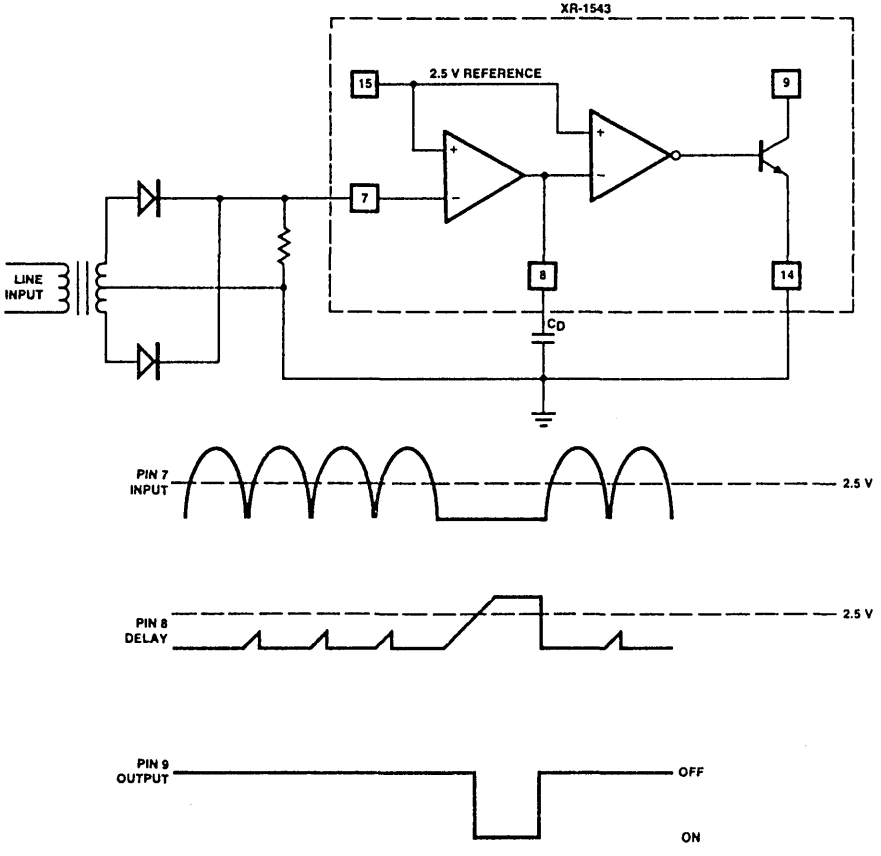


Figure 10. XR-1543—Input Line Monitor Circuit

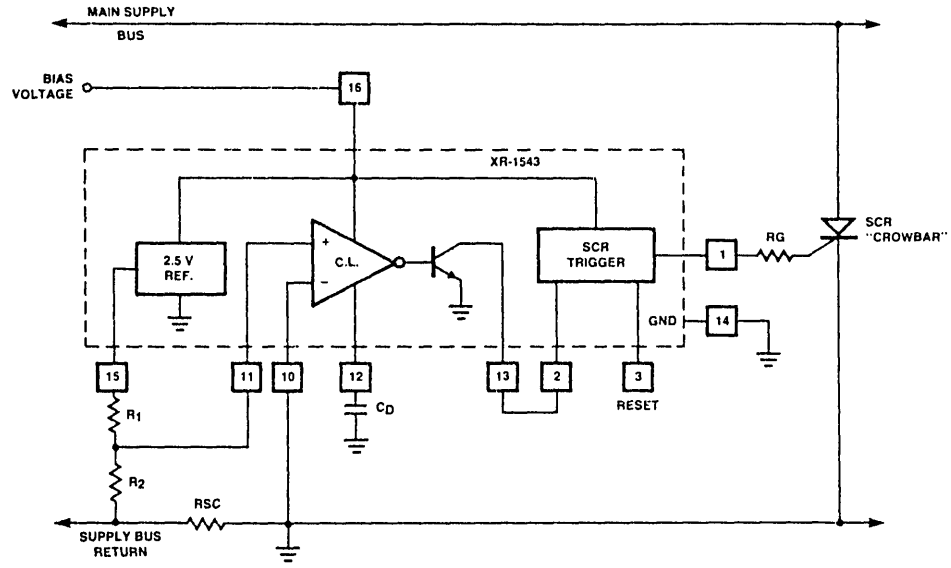


Figure 11. XR-1543—Over Current Shutdown Circuitry

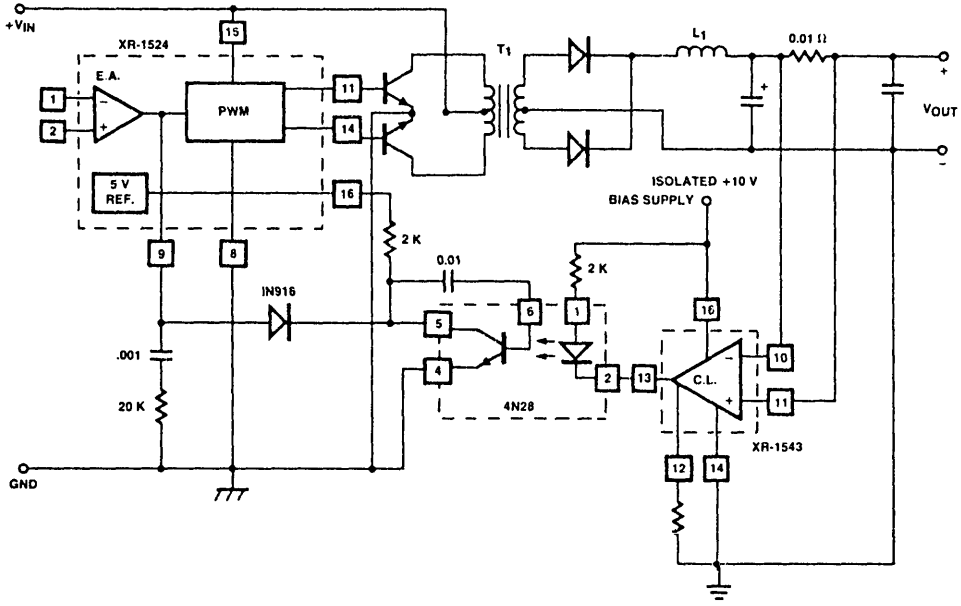


Figure 12. XR-1543 - DC Converter with Isolated Current Limiting

Pulse-Width Modulator Control System

GENERAL DESCRIPTION

The XR-2230 is a high-performance monolithic pulse width modulator control system. It contains all the necessary control blocks for designing switch mode power supplies, and other power control systems. Included in the 18-Pin dual-in-line package are two error amplifiers, a sawtooth generator, and the necessary control logic to drive two open-collector power transistors. Also included are protective features, such as adjustable dead-time control, thermal shutdown, soft-start control, and double-pulse protection circuitry.

The device provides two open-collector output transistors which are driven 180° out-of-phase, and are capable of sinking 30 mA. These outputs can be used to implement single-ended or push-pull switching regulation of either polarity in transformerless or transformer-coupled converters.

FEATURES

Thermal Shutdown
Adjustable Dead-time
Dual Open-Collector
  30 mA Output Transistors
Double-Pulse Protection Circuit
Soft-Start Control
High-Speed Remote Shut-Down Input
Two High-Performance Error Amplifiers
  with ±5V Input Common-Mode Range

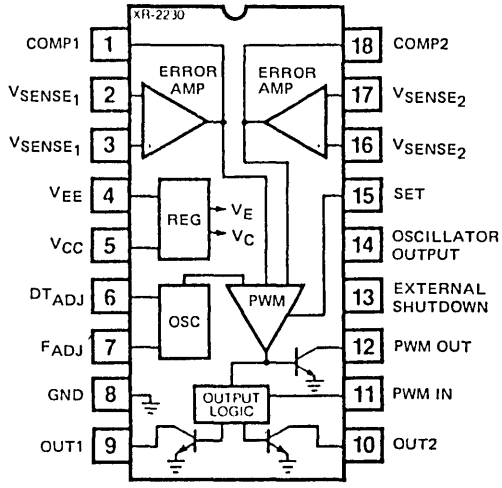
APPLICATIONS

Switching Regulators
Motor-Speed Controllers
Pulse-Width Modulated Control Systems

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	−0.5 to +18V
Negative Supply Voltage	+0.5 to −18V
Input Voltage	−18 to +18V
Output Voltage	−0.5 to +18V
Power Dissipation ($T_A \leq 25°C$)	400 mW
Operating Temperature	−10°C to +85°C
Storage Temperature	−55°C to +125°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2230CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2230 PWM circuit contains two high-performance error amplifiers with wide input common-mode range, and large voltage gains. Typically, one amplifier (Pins 16, 17, 18) is used for current sensing and the other (Pins 1, 2, 3) is used as an error amplifier to sense the output voltage. The XR-2230 requires a split supply between ±8 volts and ±15 volts, however, it can be operated from a single supply with proper external biasing on the ground pin and input pins of the error amplifiers. The output drivers capable of sinking 30 mA at a saturation voltage of about 0.3V can be used in a push-pull configuration, or can be paralleled for a single-ended configuration with a duty cycle between 0% to over 90%.

The XR-2230 features a self-protecting thermal-shutdown circuitry which turns off the output drivers when the junction temperature exceeds 130°C. The on-board regulator stabilizes the oscillator frequency to 0.1%/V for reliable performance.

XR-2230

ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = +12V, V_{EE} = -12V, f_{OSC} = 20 kHz, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
SUPPLY SECTION						
V_{CC}	Positive Supply Voltage	+10			V	
V_{EE}	Negative Supply Voltage			−10	V	
I_{CC}	Positive Supply Current	7.0	11.0	15.0	mA	
I_{EE}	Negative Supply Current	−2.0	−6.0	−2.0	mA	
OSCILLATOR SECTION						
f_{OSC}	Frequency Range	10		100	kHz	
	Initial Accuracy			15	%	R_T = 30 kΩ, C_T = 4700 pF
	Supply Voltage Stability		0.1		%/V	V_{CC} = +10V ≈ +15V
	Low Supply Voltage	−20		+20	%	V_{CC} = +18V, V_{EE} = −8V
	Temperature Stability		0.01		%/°C	
V_{OSC}	Sawtooth Peak Voltage	3.0	3.5	4.0	V	
δ	Duty Cycle Range	10		90	%	f_{OSC} = 20 kHz
VOLTAGE ERROR AMPLIFIER						
V_{OS}	Input Offset Voltage		2	10	mV	
I_{BIAS}	Input Bias Current		−.5	−30	μA	
A_{VO}	Open-Loop Gain	60	90		dB	
f_{-3dB}	Closed-Loop Bandwidth		25		kHz	A_{VCL} = 40 dB
CMMR	Common-Mode Rejection Ratio	60			dB	V_{ICM} = ±4.5V
V_{OM}	Output Voltage Swing	±5			V	R_L = 10 kΩ, V_{CC} = +8V, V_{EE} = −8V
SR	Slew Rate	2	4		V/μs	A_{VCL} = 14 dB, R_F = 10 kΩ
	Input Voltage Range		±5		V	
CURRENT ERROR AMPLIFIER						
V_{OS}	Input Offset Voltage		4	20	mV	
I_{BIAS}	Input Bias Current		−1.0	−60	μA	
A_{VO}	Open-Loop Gain	60	90		dB	
$f_{-3\ dB}$	Closed-Loop Bandwidth		25		kHz	A_{VCL} = 40 dB
CMRR	Common-Mode Rejection Ratio	60	90		dB	V_{ICM} = ±4.5V
V_{OM}	Output Voltage Swing	±5			V	R_L = 10 kΩ
		±4			V	V_{CC} = +8V, V_{EE} = −8V
SR	Slew Rate	4	8		V/μs	A_{ACL} = 14 dB, R_F = 10 kΩ
	Input Voltage Range		±5		V	
MODULATOR SECTION						
	Set Input Open Voltage	3.1	3.6	4.1	V	
	(Pin 15)	2.8	3.3	4.3	V	V_{CC} = +8V, V_{EE} = −8V
	Modin Input Open Voltage	3.1	3.6	4.1	V	
	(Pin 11)	2.8	3.3	4.3	V	V_{CC} = +8V, V_{EE} = −8V
	Inhibit Input Current (Pin 13)	−50	−10		μA	
t_d	Inhibit Propagation Delay		60		ns	
	Out1, Out2, Output Voltage			0.3	V	I_O = 30 mA, T_A = 25°C
	(Pins 9 and 10)			0.4	V	T_A = −10 ≈ +85°C
	Low Supply Voltage			0.3	V	I_O = 27 mA, T_A = 25°C
t_f	Out1, Out2 Fall Time		30		ns	
	Modout Output Voltage			0.3	V	I_O = 16 mA, T_A = 25°C
	(Pin 12)			0.4	V	T_A = −10 ≈ +85°C
	Under Low Supply Voltage			0.3	V	I_O = 24 mA, T_A = 25°C
	Oscillator Output Voltage			0.4	V	I_O = 3 mA, T_A = 25°C
	(Pin 14)			0.6	V	T_A = −10 ≈ +85°C
	Thermal Shutdown Temp.		130		°C	

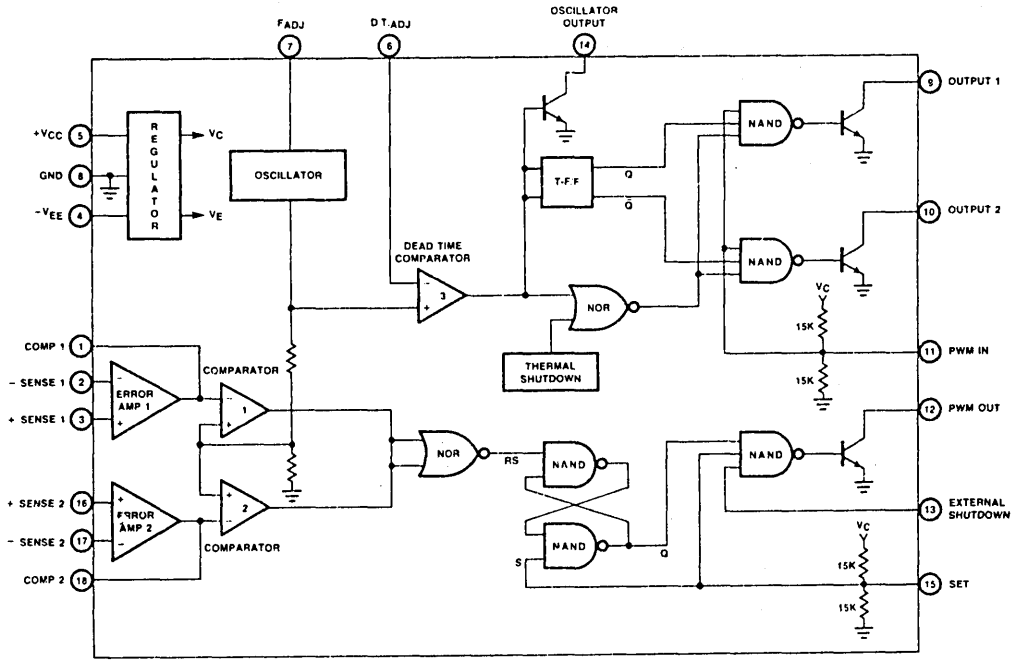


Figure 1. Equivalent Schematic Diagram

PRINCIPLES OF OPERATION

The heart of the XR-2230 is the sawtooth generator. As seen in Figure 1, this sawtooth drives one input of each of the three system comparators. Comparators one and two have their other inputs tied to the outputs of the error amplifiers. These comparators will now produce, at their outputs, square waves which will have a duty cycle proportional to the voltage at the inputs to the error amplifiers, or pulse width information. The pulse width information is fed into the NOR gate and used to provide the reset information to the pulse-width modulation flip-flop (PWM). The PWM flip-flop information is fed in to the NAND gate with the external shutdown and PWM flip-flop set input. The information from the NAND gate drives an open-collector transistor to provide the pulse-width modulation output, Pin 12. The PWM output will be a square wave with a frequency set by the sawtooth generator, and a duty cycle equal to either comparator, one or two, whichever is shorter. If the external shutdown, Pin 13 is driven low, the PWM output will remain low or go to zero duty cycle. The set input of the PWM flip-flop, Pin 15, is normally connected to the buffered sawtooth generator output, Pin 14, so that a reset pulse is provided every cycle. Each output transistor is driven by a three input NAND gate. These inputs consist of:

1. Pulse width information from the PWM input, Pin 11, which is used to control the off time of the output transistors. The PWM input is normally tied to the PWM output so that the output transistor's off time is a function of the error amplifier's input voltage.

2. Pulse-steering information from flip-flop two, which will determine which output transistor receives the PWM input signal. Flip-flop two will toggle once every cycle of the sawtooth generator's output, which will make the output transistor's toggle frequency one-half that of the sawtooth generator's.

3. Information from dead-time and thermal shutdown circuitry. The dead-time is an externally adjustable time between one output transistor turning off and the other turning on. This is used to protect external circuitry. This dead-time is controlled by an external voltage applied to Pin 6, which is internally compared with the sawtooth waveform. The thermal shutdown circuitry will drive the input to the NAND gate low, if the junction temperature exceeds 130°C. This will make both outputs low.

The circuit control blocks and functions operate as follows:

Error Amplifiers—These are high-gain op amps which are used to sense output conditions, voltage and current, and provide a dc voltage to comparators one and two. This will in turn adjust the PWM output duty cycle and ultimately that of the output transistors to correct for errors in the output voltage or overcurrent conditions. The amplifier's outputs are provided for tailoring the closed-

loop gain or frequency response of the system. Figure 2 shows the relationship between output duty cycle, Pins 11 and 12 connected, and the voltage at Pins 1 or 18. Amplifier two is approximately twice as fast as Amplifier one, and should, therefore, be used to sense output current.

External Shutdown, Pin 13—A low level signal applied to this pin will turn both outputs on. If not used, this input should be left open-circuited. The impedance at this node is approximately 1 MΩ.

Oscillator Output, Pin 14—This is an open-collector output which will be a square wave with a frequency set by the sawtooth generator. The duty cycle of this output will vary from 10 to 90%, and is a function of the dead-time setting. This pin is normally connected to Pin 15, set to provide reset pulses for the PWM flip-flop.

Set, Pin 15—This is the set input for the PWM flip-flop. A low-going signal at this pin will cause the flip-flop to be reset. The impedance at this pin is approximately 7.5 kΩ. This pin is normally connected to the oscillator output, Pin 14.

PWM Out, Pin 12—This is an open-collector output which provides a square wave with a duty cycle determined by the error amplifiers. This output is normally connected to PWM IN, Pin 11.

PWM In, Pin 11—This is the input which controls the duty cycle of the output transistors. A low level on this pin will drive both output transistors on. The impedance into this pin is approximately 7.4 kΩ.

Output Transistors, Pins 9 and 10—These pins provide the open-collector output transistors which are capable of sinking 30 mA, typically. They are alternately turned off, 180° out-of-phase, at a rate equal to one-half the frequency of the oscillator.

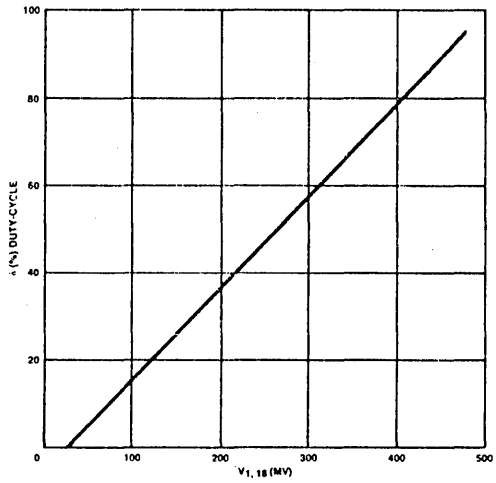


Figure 2. Modulation Duty Cycle vs Error Voltage

F_{ADJ}, Pin 7—A resistor, R_{ext} to $+V_{CC}$, and a capacitor, C_{ext}, to ground from this pin, set the frequency of the sawtooth and oscillator output, by the relationship:

$$F_{OSC} = \frac{2.68}{R_{ext} \times C_{ext}}$$

The sawtooth waveform a signal varying from zero volts to +5V, will be present at Pin 7. Normal values of R_{ext} will range from 1 kΩ to 100 kΩ. Figure 3 shows the oscillator period as a function of various R_{ext} and C_{ext} values.

The dead-time (minimum time from one output turning on to the other turning off) is controlled by the voltage applied to Pin 6.

Dead-time Control, Pin 6—Figure 4 shows output deadtime as a function of $V_{PIN\ 6}$. The maximum duty cycle of each output is also controlled by the dead-time, and may be determined by the following expression:

$$\text{Duty Cycle Max (\%)} = \left(1 - \frac{.35}{V_{PIN\ 6}}\right) \times 50\%$$

$$V_{PIN\ 6} < 3.5V$$

The impedance into this pin is approximately 10 kΩ.

APPLICATIONS INFORMATION

The soft-start function may be implemented as shown in Figure 7. This configuration will reduce the output duty cycle to zero, and gradually increase to its normal operating point, whenever power is applied to the circuit, or after an external shutdown command has been given. This is used to keep the magnetics in the circuit from saturating.

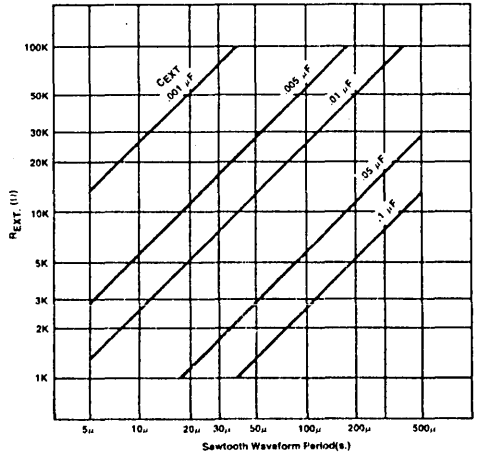


Figure 3. Oscillation Period vs R_{EXT} and C_{EXT}

The time for the duty cycle to start will be approximately equal to $R_1 \times C_1$.

A typical step-down switching regulator configuration is shown in Figure 8. Only one output transistor is used, so that the maximum duty cycle will be limited to 45%. If a larger duty cycle range is needed, the two outputs may be externally NOR'd as shown in Figure 9. This configuration will allow up to 90% duty cycles.

Figure 10 shows a detailed timing diagram of circuit operation.

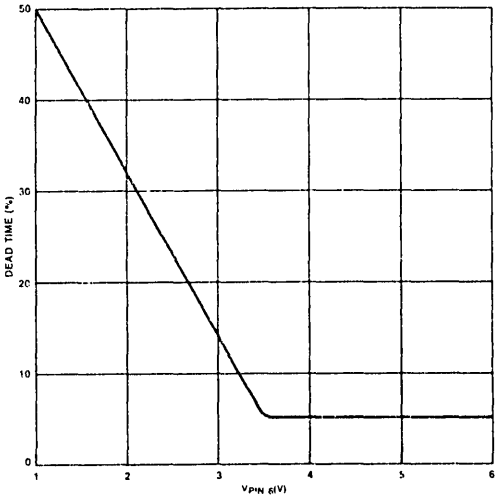


Figure 4. Dead Time vs Dead Time Adjustment Voltage

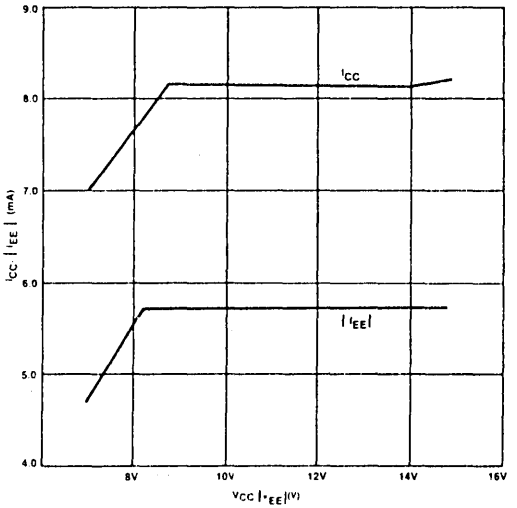


Figure 5. Supply Current vs Supply Voltage

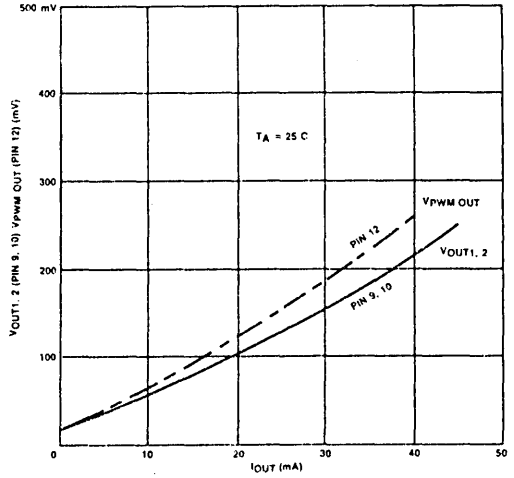


Figure 6. Output Saturation Voltage vs Load Current

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION	UNIT
V_{CC}	Positive Supply Voltage	$+10 \approx +15$	V
V_{EE}	Negative Supply Voltage	$-10 \approx -15$	V
R_R	Minimum Feedback Resistance	10	kΩ
A_V	Minimum Voltage Gain	14 5	dB V/V

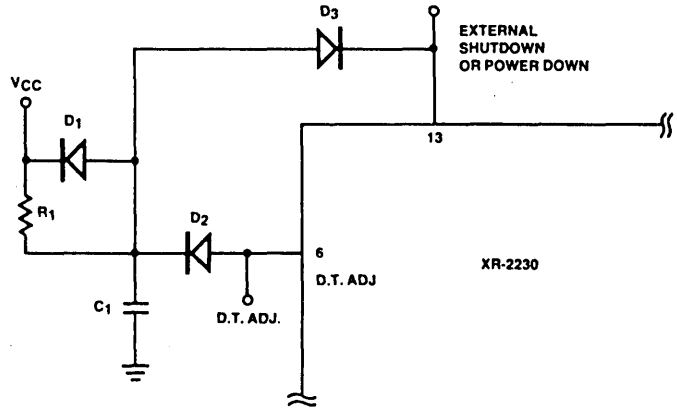


Figure 7. Soft Start Connection

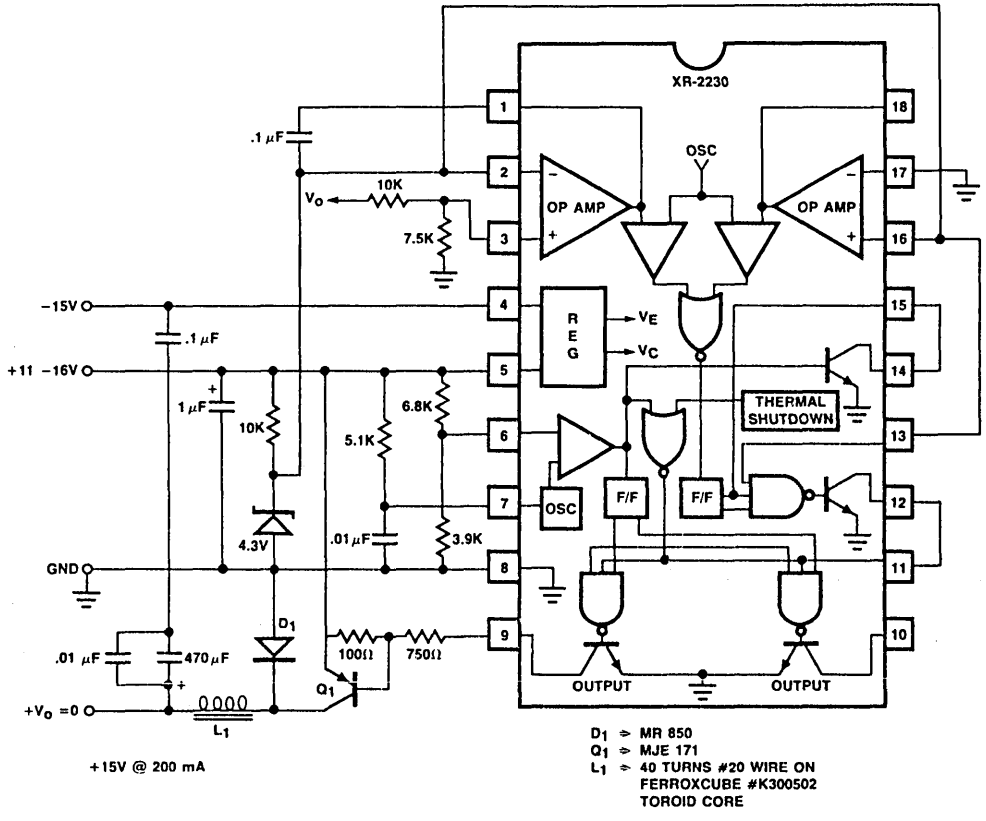


Figure 8. +10V Step-Down Regulator

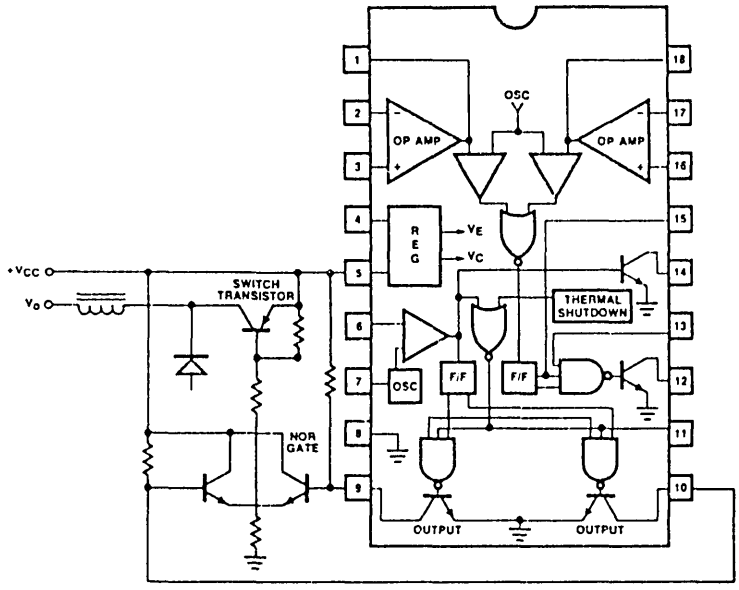


Figure 9. Outputs Nor'd for up to 90% Duty Cycle's

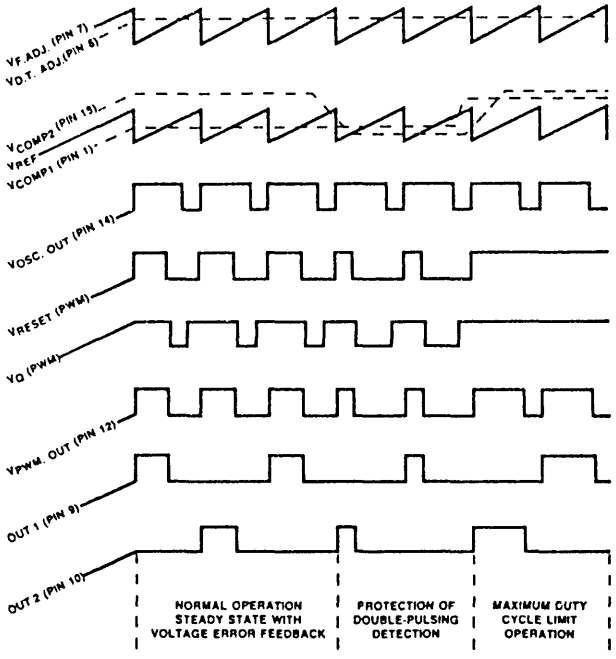


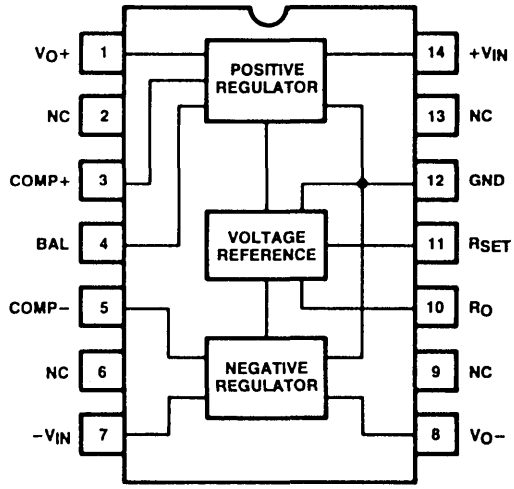
Figure 10. Timing Waveform Diagram

Dual-Tracking Voltage Regulator

GENERAL DESCRIPTION

The XR-4194 is a dual-polarity tracking regulator designed to provide balanced or unbalanced positive and negative output voltages at currents of up to 200 mA. A single resistor can be used to adjust both outputs between the limits of ±50mV and ±42 V. The device is ideal for local on-card regulation, which eliminates the distribution problems associated with single-point regulation. The XR-4194 is available in a 14-pin ceramic dual-in-line package, which has a 900 mW rating.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for RM/RC 4194
Both Outputs Adjust with Single Resistor
Load Current to ±200 mA with 0.2% Load Regulation
Low External Parts Count
Internal Thermal Shutdown at T_J = 175°C
External Adjustment for ± V_O Unbalancing

APPLICATIONS

On-Card Regulation
Adjustable Regulator

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4194CN	Ceramic DIP	0°C to +70°C
XR-4194M	Ceramic DIP	−55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Input Voltage ± V to Ground	
XR-4194M	±45 V
XR-4194CN	±35 V
Input/Output Voltage Differential	±45 V
Power Dissipation at T_A = 25°C	900 mW
Load Current	30 mA
Operating Junction Temperature Range	
XR-4194M	−55°C to +150°C
XR-4194CN	0°C to +125°C
Storage Temperature Range	−65°C to +150°C

SYSTEM DESCRIPTION

The XR-4194 is a dual polarity tracking voltage regulator. An on board reference, set by a single resistor, determines both output voltages. Tracking accuracy is better than 1%. Non-symmetrical output voltages are obtained by connecting a resistor to the balance adjust (Pin 4). Internal protection circuits include thermal shutdown and active current limiting.

ELECTRICAL CHARACTERISTICS

Test Conditions: $\pm 5 \leq V_{OUT} \leq V_{MAX}$; XR-4194M $-55°C \leq +125°C$; XR-4194CN $0°C \leq T_J \leq +70°C$

$-55°C \leq T_J \leq +125°C$	XR-4194M			XR-4194CN				
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Line Regulation		0.02	0.1		0.02	0.1	$\%V_{OUT}$	$\Delta V_{IN} = 0.1\ V_{IN}$
Load Regulation		0.001	0.0025		0.001	0.004	$\%V_O$/mA	XR-4194CN, M: I_L = 5 to 100 mA
TC of Output Voltage		0.002	0.020		0.003	0.015	%/°C	
*Stand-by Current Drain from		+0.3	+1.0		+0.3	+1.5	mA	$V_{IN} = V_{MAX}$, V_O = 0V
to		−1.2	−2.0		−1.2	−2.0		$V_{IN} = V_{MAX}$, V_O = 0V
Input Voltage Range	±9.5		±45	±9.5		±35	V	
Output Voltage Scale Factor	2.45	2.5	2.55	2.38	2.5	2.62	KΩ/V	R_{SET} = 71.5 K, T_J = 25°C
Output Voltage Range	0.05		+42	0.05		±32	V	R_{SET} = 71.5 K
Output Voltage Tracking			1.0			2.0	%	
Ripple Rejection		70			70		dB	f = 120 Hz, T_J = 25°C
Input-Output Voltage Differential	3.0			3.0			V	I_L = 50mA
Output Short Circuit Current		300			300		mA	V_{IN} = ±30 V Max
Output Noise Voltage		250			250		μV RMS	C_L = 4.7 μF, V_O = ±15 V, f = 10 Hz to 100 KHz
Internal Thermal Shutdown		175			175		°C	

* $\pm I_{Quiescent}$ will increase by 50 $\mu A/V_{OUT}$ on positive side and 100 $\mu A/V_{OUT}$ on negative side.

THERMAL CHARACTERISTICS

	XR-4194M			XR-4194CN			
PARAMETERS	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**CONDITIONS**
Power Dissipation			900 mW 2.2 W			900 mW 2.2 W	T_A = 25°C T_C = 25°C
Thermal Resistance Junction to Ambient Junction to Case		128°C/W 55°C/W			128°C/W 55°C/W		

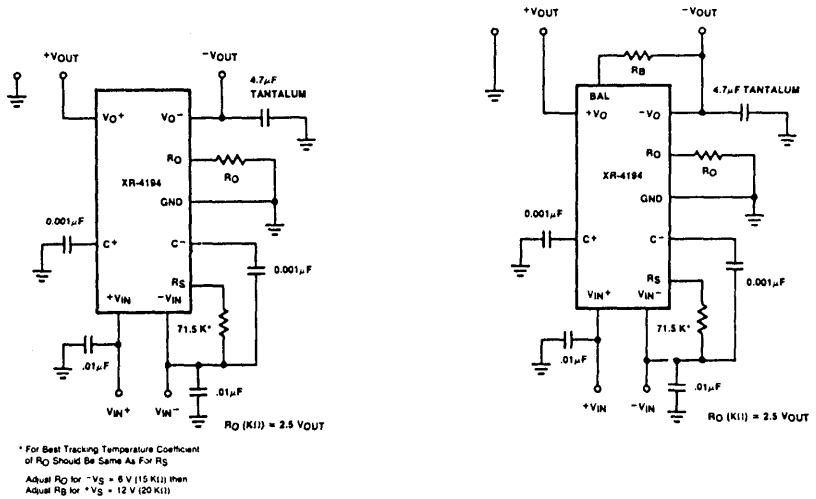
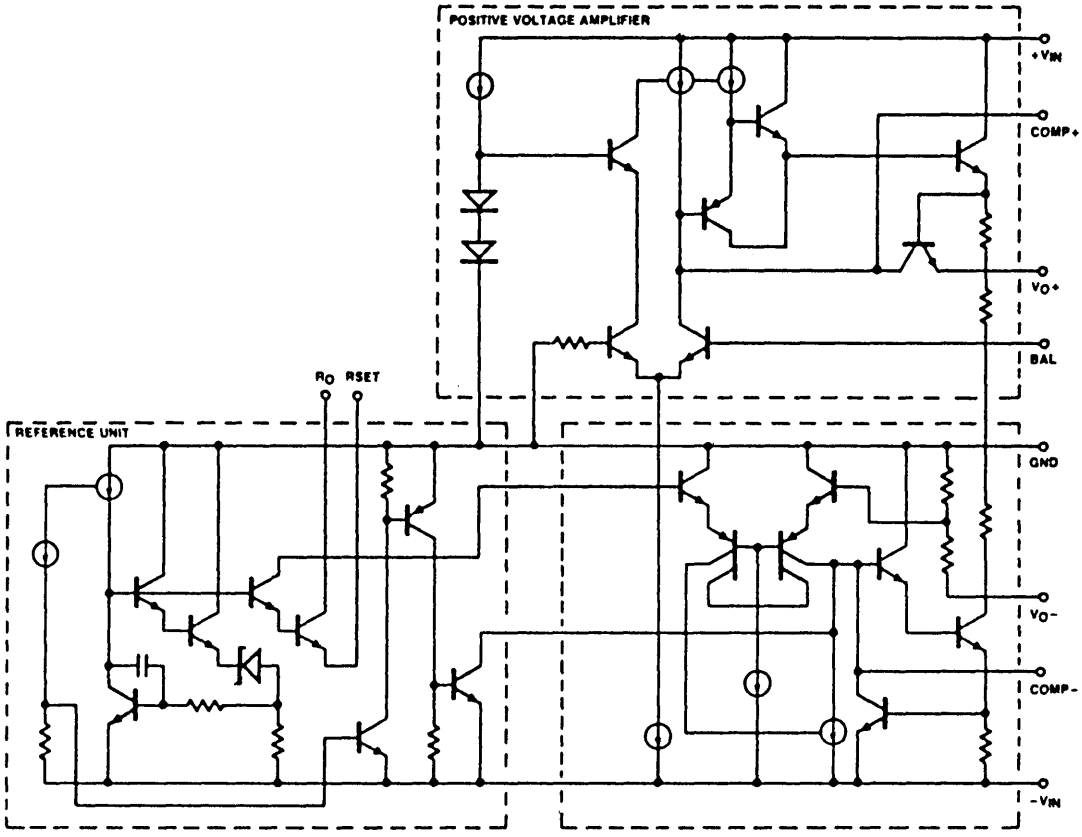


Figure 2. Typical Applications

XR-4194



EQUIVALENT SCHEMATIC DIAGRAM

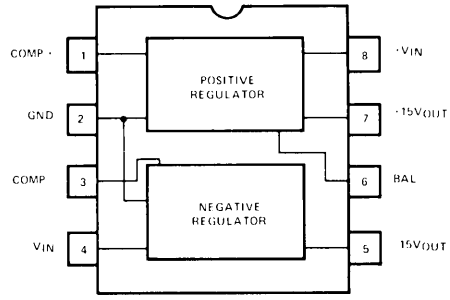
±15V Dual-Tracking Voltage Regulator

GENERAL DESCRIPTION

The XR-4195 is a dual-polarity tracking regulator designed to provide balanced positive and negative 15V output voltages at currents of up to 100mA.

The device is ideal for local "on-card" regulation, which eliminates the distribution problems associated with single-point regulation. Intended for ease of application, the XR-4195 requires only two external components for operation.

FUNCTIONAL BLOCK DIAGRAM



5

FEATURES

Direct Replacement for RM/RC 4195
±15V Operational Amplifier Power
Thermal Shutdown at T_j = +175°C
Output Currents to 100mA
As a Single Output Regulator, it may be used with up to +50V Output
Available in 8-Pin Plastic Mini-DIP
Low External Parts Count

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4195CP	Dip	0°C to +70°C

APPLICATIONS

Operational Amplifier Supply
On-Card Regulation
Regulating High Voltage

ABSOLUTE MAXIMUM RATINGS

Input Voltage ±V to Ground	±30 V
Power Dissipation at T_A = 25°C	600 mW
Load Current	100 mA
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	−65°C to +150°C

SYSTEM DESCRIPTION

The XR-4195 is a dual polarity tracking voltage regulator, internally trimmed to ±15V. Only output capacitors are required for operation. Internal protection circuits include thermal shutdown and active current limiting. The device may be configured as a single output high voltage regulator by adding a voltage divider between an output pin, the device ground (Pin 2) and system ground.

XR-4195

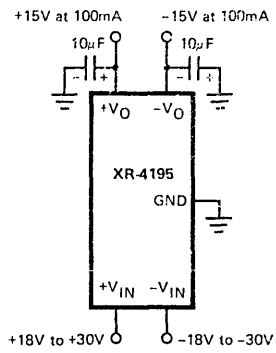
ELECTRICAL CHARACTERISTICS

Test Conditions: (I_L = 1mA, V_{CC} = ±20V, C_L = 10μF unless otherwise specified)

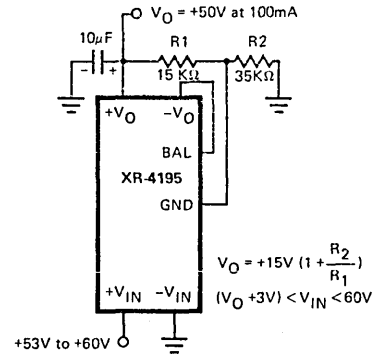
PARAMETERS	XR-4195CP			UNITS	CONDITIONS
	MIN	TYP	MAX		
Line Regulation		2	20	mV	V_{IN} = ±18 to ±30V
Load Regulation		5	30	mV	I_L = 1 to 100 mA
Output Voltage Temperature Stability		0.005	0.015	%/°C	
Standby Current Drain		±1.5	±3.0	mA	V_{IN} = ±30V, I_L = 0mA
Input Voltage Range	18		30	V	
Output Voltage	14.5	15	15.5	V	T_j = +25°C
Output Voltage Tracking		±50	±300	mV	
Ripple Rejection		75		dB	f = 120 Hz, T_j = +25°C
Input-Output Voltage Differential	3			V	I_L = 50mA
Short-Circuit Current		220		mA	T_j = +25°C
Output Noise Voltage		60		μV RMS	T_j = +25°C, f = 100 Hz to 100 kHz
Internal Thermal Shutdown		175		°C	

THERMAL CHARACTERISTICS

PARAMETERS	XR-4195CP			CONDITIONS
	MIN	TYP	MAX	
Power Dissipation			0.6W	T_A = 25°C T_C = 25°C
Thermal Resistance		210°C/W		θJ-C θJ-A

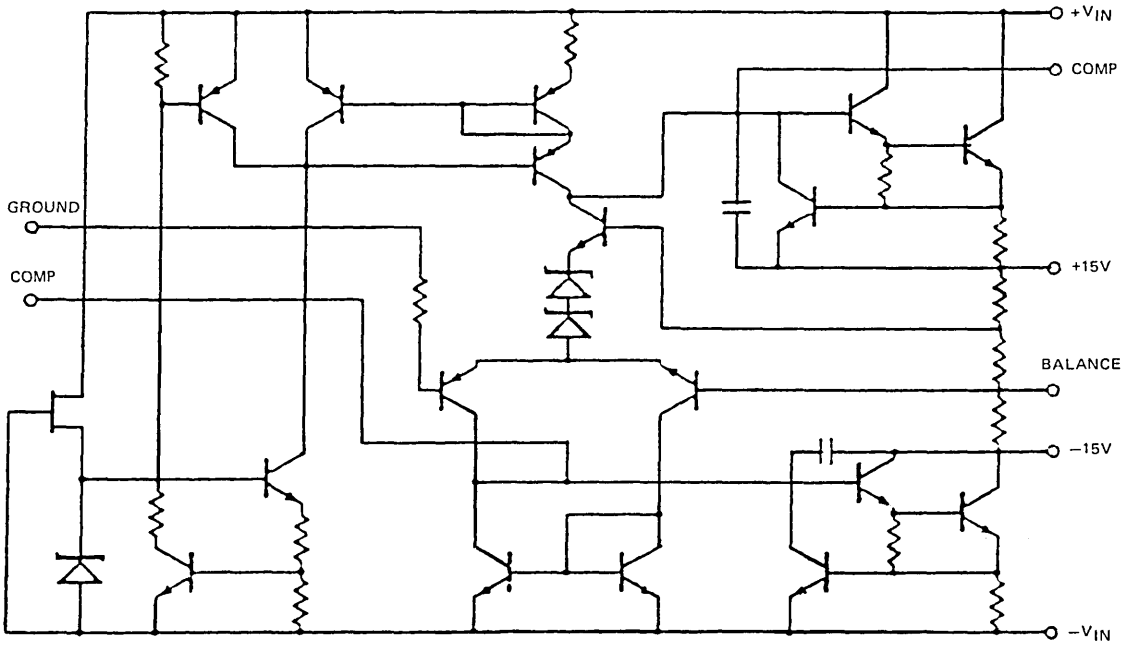


Balanced Output



Positive Single Supply

TYPICAL APPLICATIONS



EQUIVALENT SCHEMATIC DIAGRAM

EXAR

Section 6 – Instrumentation Circuits

Fundamentals of Monolithic Waveform Generation and Shaping

Waveform or function generators find a wide range of applications in communications and telemetry equipment, as well as for testing and calibration in the laboratory. In most of these applications, commercially-available monolithic IC oscillators and function generators provide the system designer with a low-cost alternative to conventional, non-integrated units costing several hundred dollars or more.

The fundamental techniques of waveform generation and shaping are well suited to monolithic IC technology. In fact, monolithic integrated circuits offer some inherent advantages to the circuit designer, such as the availability of a large number of active devices and close matching and thermal tracking of component values. By making efficient use of the capabilities of integrated components and the batch-processing advantages of monolithic circuits, it is now possible to design integrated waveform generator circuits that can provide a performance comparable to that of complex discrete generators, at a very small fraction of the cost. This article provides a brief review of the fundamental principles of monolithic waveform generation and wave-shaping methods.

Basics of IC Waveform Generation

Essentially a waveform generator is a stable oscillator circuit that outputs well-defined waveforms; and, these can be externally modulated or swept over a frequency range. A waveform generator usually consists of four sections: (1) an oscillator to generate the basic periodic waveform; (2) a wave-shaper; (3) an optional modulator section to provide AM capability, and (4) an output buffer amplifier to provide the necessary load drive.

Figure 1 shows a simplified generator using the four functional blocks. Each block can be built readily in monolithic form with established linear IC technology. Hence fabrication of all four blocks on a single monolithic chip has evolved as a natural extension of earlier circuits.

The oscillator, usually a relaxation type, can generate linear, triangle or ramp waveforms. The usual technique involves constant-current charging and discharging of an external timing capacitor. Figure 2 shows a typical, though simplified, example: an emitter-coupled multivibrator circuit, which can generate a square wave as well as a triangle or a linear ramp output.

The circuit's operation is as follows: At any given time, either Q_1 and D_1 or Q_2 and D_2 are conducting such that capacitor C_O is alternately charged and discharged by constant-current I_1. The output across D_1 and D_2 corresponds to a symmetrical square wave, having a pk-pk amplitude of $2V_{BE}$, or twice the transistor base-emitter voltage drop. Output V_A, constant when Q_1 is on, becomes a linear ramp with a slope equal to $-I_1/C_O$ goes off. Except for a half cycle delay, output $V_B(t)$ is the same as $V_A(t)$.

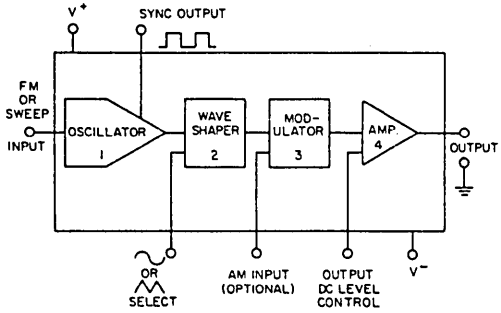


Figure 1. Basically, a waveform generator consists of four sections. Each section can be built readily in monolithic form with established IC technology.

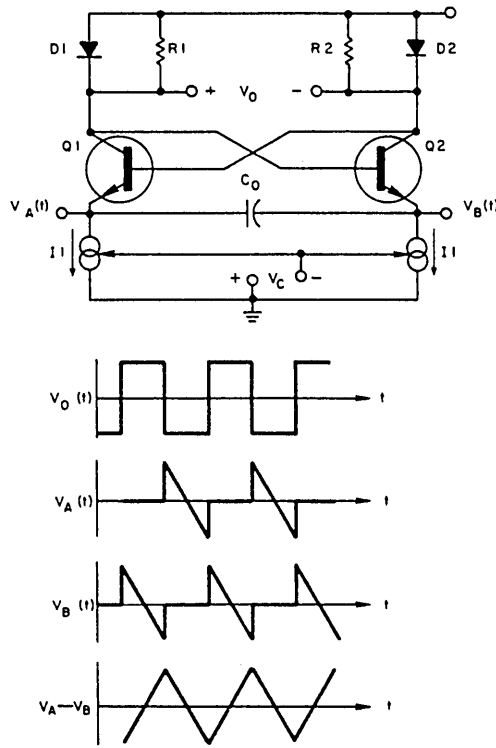


Figure 2. A simple oscillator circuit can be used to generate square, ramp and triangle waveforms.

Choosing The Right IC Oscillator

At the onset of his design, the user of monolithic oscillator products is faced with the key question of choosing the oscillator or the function generator best suited to his application. The broad line of function generator products offered by Exar covers a wide range of applications. It is often difficult to determine at a glance the best circuit for a given application. The purpose of this section is to review some of the key performance requirements, from an applications point of view, and help answer the question. "What is the best IC oscillator for the job?"

Sine Wave Generation

In evaluating the output characteristics of sinusoidal IC oscillators, total harmonic distortion (THD) of the output waveform is usually the key performance criteria. In a number of voice-grade telecommunication or laboratory applications, sine wave distortion of 2% to 3% may be tolerable. However, for audio-quality signals, distortion level of 1% or less is required. Furthermore, it is desirable that the output distortion should be relatively independent of the output amplitude, frequency or temperature changes; and that the distortion level be minimized with a minimum amount of external adjustments.

Exar manufactures three separate families of IC oscillators which provide sinusoidal output waveforms. These are the XR-205, XR-2206 and the XR-8038. All of these circuits require external trimming to minimize the output distortion. In the case of XR-205, the untrimmed distortion is about 5%; in the case of the XR-2206 and the XR-8038, untrimmed distortion is typically less than 2%, and can be reduced to 0.5% with additional trimming.

For low frequency sine wave generation (below 100 kHz), the XR-2206 and the XR-8038 are the recommended circuits. The XR-8038 has a fixed output level, whereas the XR-2206 offers separate output dc level and amplitude adjustment capability.

AM Generation

Linear modulation of output amplitude by means of an analog control signal is a desirable feature for telemetry and data transmission applications. In monolithic IC oscillators, this capability is normally obtained by including a four-quadrant transconductance multiplier on the IC chip. Both the XR-205 and the XR-2206 circuits have such a feature included on the chip and can be used for generating sinusoidal AM signals. They can operate both in suppressed-carrier or conventional double-sideband AM generator mode. For operation with frequencies below 100 kHz, the XR-2206 has superior performance characteristics over the XR-205.

FM Generation

Essentially all of Exar's IC oscillator circuits can be used for generating frequency-modulated waveforms. For small frequency deviations (i.e., ±5% or less) about the center frequency, all of these oscillators have FM nonlinearity of 0.1% or less. However, if wider FM deviations are required the XR-2209, XR-2207 and the XR-2206 offer the best FM linearity.

FSK Generation

Frequency-shift keying (FSK) is widely used in digital communications, particularly in data-interface or acoustical-coupler type MODEM systems. In monolithic IC oscillators, FSK capability is obtained by using a current-controlled oscillator and keying its control current between two or more programmed levels which are set by external resistors. This results in output waveforms which are phase-continuous during the frequency transitions between the "mark" and "space" frequencies.

The XR-2207 can produce four discrete frequencies, set by one external capacitor and four setting resistors. Frequency keying between these four frequencies is achieved by a two-bit binary logic input. The circuit produces both triangle and square wave outputs. The XR-2206 produces two discrete frequencies, f_1 and f_2, and has a one-bit keying logic input. The key advantage of XR-2206 over the XR-2207 in FSK MODEM design is the availability of a sinusoidal output waveform.

Exar has compiled a comprehensive application note describing the use of both of these IC products in the design of FSK MODEM systems. This application note entitled "Stable FSK MODEMs Featuring the XR-2207, XR-2206 and the XR-2211" is also included in this Data Book.

Laboratory Function Generator

One of the main applications for oscillators is for laboratory or test instrumentation or calibration where a variety of different output waveforms are required. Most such applications require both AM/FM modulation capability, linear frequency sweep and sinusoidal output. The circuit which fits this application best is the XR-2206 since it has all the fundamental features of a complete function generator system costing upwards of several hundred dollars.

A comprehensive description of building a self-contained laboratory-quality function generator system using the XR-2206, Application Note AN-14, is included in this Data Book.

Phase-Locked Loop Design

The current-controlled or voltage-controlled oscillator (VCO) is one of the essential components of a phase-locked loop (PLL) system. The key requirement for this application is that the oscillator should have a high degree of frequency stability and linear voltage or current-to-frequency conversion characteristics. Sinusoidal output, although often useful, is generally not required in this application.

Although all of Exar's IC oscillators can be used as a VCO in designing PLL systems, the XR-2207 or its low-cost and simplified version, the XR-2209, are often the best suited devices for this application. For additional information refer to Application Note AN-06, entitled "Precision PLL System Using the XR-2207 and the XR-2208," which is included in this Data Book.

Sweep Oscillator

A sweep oscillator is required to have a large linear sweep range. Among Exar's function generators, the XR-2207 and the XR-2206 have the widest linear sweep range (over 1000:1), and are best suited for such an application.

By using a linear ramp output from the XR-2207 to sweep the frequency of the XR-2206, one can build a two-chip sweep oscillator system which has a 2000:1 sweep range and sinusoidal output.

Low-Cost General Purpose Oscillator

In many digital design applications, one needs a stable, low-cost oscillator IC to serve as the system clock. For such applications, the XR-2209 precision oscillator is a logical design choice since it is a simple, low-cost oscillator circuit and offers 20 ppm/°C frequency stability.

The monolithic timer circuits, such as the XR-555, or its micropower version, the XR-L555, can also be used as low-cost, general purpose oscillators by operating them in their free-running, i.e., self-triggering, mode.

Ultra-Low Frequency Oscillator

In certain applications such as interval-timing or sequencing, stable, ultra-low frequency oscillators which can operate at frequencies of 0.01 Hz or lower are required. Among Exar's oscillator circuits, the IC most suited to such an application is the XR-8038 since it can operate with a polarized electrolytic capacitor as its timing component. All other oscillator circuits described in this book require non-polar timing capacitors, and therefore are not as practical as the XR-8038 for ultra-low frequency operation.

An alternate approach to obtaining stable ultra-low frequency oscillators is to use the XR-2242 counter/timer as an oscillator in its free-running mode. Such a circuit generates a square wave output with a frequency of (1/256 RC) where R and C are the external timing components.

Monolithic Waveform Generator

GENERAL DESCRIPTION

The XR-205 is a highly versatile, monolithic waveform generator designed for diverse applications in communication and telemetry equipment, as well as in systems design and testing. It is a self-contained, totally monolithic signal generator that provides sine, square, triangle, ramp and sawtooth output waveforms, which can be both amplitude and frequency modulated.

The circuit has three separate sections: a voltage-controlled oscillator (VCO) which generates the basic periodic waveforms; a balanced modulator which provides amplitude or phase modulation; a buffer amplifier section which provides a low impedance output with high current drive capability.

FEATURES

High Frequency Operation
AM and FM Capabilities
Sine, Triangle, Square, Sawtooth, Ramp and Pulse Waveforms
Wide Supply Range 8 V to 26 V
Split Supply Capability

APPLICATIONS

Waveform Generation

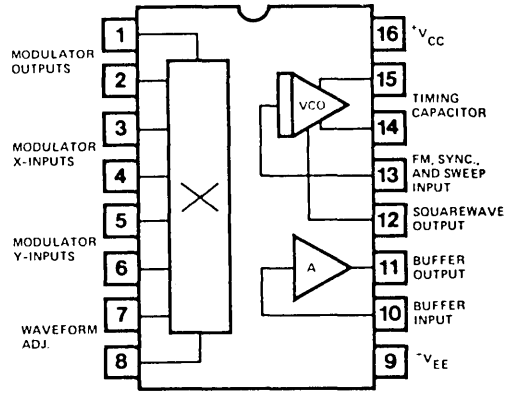
Sinewave	Sawtooth
Triangle	Ramp
Square	Pulse

AM Generation Double Sideband Suppressed Carrier
FM Generation
Sweep Generation
Tone Burst Generation
Simultaneous AM/FM
Frequency-Shift Keyed (FSK) Signal Generation
Phase-Shift Keyed (PSK) Signal Generation
On-Off Keyed Oscillation
Clock Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Temperature	
Storage	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-205	Ceramic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-205 is a high frequency monolithic function generator capable of sine, square, triangle, ramp, sawtooth, and pulse waveforms with frequencies ranging to 4 MHz. Operating frequency is determined by a single capacitor and may be externally swept over a 10:1 range. Duty cycle is variable from 10% to 90%. Amplitude modulation, up to 100%, is accomplished using the modulator X inputs (Pins 3 and 4). The on board buffer amplifier features 50Ω output resistance and 20 mA output capability. The XR-205 operates with either single or split supplies.

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = 12V (single supply) T_A = 25°C, f - 10 kHz, R_L = 3 kΩ, unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I — General Characteristics					
Supply Voltage:					
Single Supply	8		26	Vdc	See Figure 1
Split Supply	±5		±13	Vdc	See Figures 2 and 3
Supply Current	8	10	12	mA	w/o buffer amp
Frequency Stability:					
Power Supply		0.2	0.5	%/V	$\|V_{CC} - V_{EE}\| > 10V$
Temperature		300	600	ppm/°C	Sweep input open circuit
Frequency Sweep Range	7:1	10:1			See Figure 7
Output Swing:					
Single Ended	2	3		Vpp	Measured at pin 1 or 2
Differential	4	6		Vpp	Measured across 1 and 2
Output Diff. Offset Voltage		0.1	0.4	Vdc	Measured across 1 and 2
Amplitude Control Range		60		dB	Controlled by R_Q (see Figure 1)
Buffer Amplifier Output Resistance		50		ohms	R_L = 750Ω
Output Current Swing	±6	±10		mA	
II — Output Waveforms					
Sinusoidal:					
Upper Frequency Limit	2	4		MHz	Measured at Pin 11
Peak Output Swing	2	3		Vpp	S_1, S_3 closed, S_2 open
Distortion (THD)		2.5	4	%	closed S_2 open
Triangle:					
Peak Swing	2	4		Vpp	Measured at Pin 11
Non-Linearity		±1		%	S_1, S_2 open, S_3 closed
Asymmetry		±1		%	f = 10 kHz
Sawtooth:					
Peak Swing	2	3		Vpp	See Figure 1, S_2 closed;
Non-Linearity		1.5		%	S_2 and S_3 closed
Ramp:					
Peak-Swing	1	1.4		Vpp	See Figure 1, S_2 and S_3 open
Non-Linearity		1		%	pin 10 shorted to pin 15
Squarewave (Low Level):					
Output Swing	0.5	0.7		Vpp	See Figure 1, S_2 and S_3 open,
Duty Cycle Asymmetry		q±1	±4	%	pin 10 shorted to pin 12
Rise Time		20		ns	10 pF connected from pin 11
Fall Time		200		ns	to ground
Squarewave (High Level):					
Peak Swing	2	3		Vpp	See Figure 3, S_2 open
Duty Cycle Asymmetry		±1	±4	%	
Rise Time		80		ns	10 pF connected from pin 11
Fall Time		60		ns	to ground
Pulse Output:	2	3		Vpp	See Figure 3, S_2 closed
Peak Swing	2	3		Vpp	See Figure 3, S_2 closed
Rise Time		80		ns	
Fall Time		60		ns	
Duty Cycle Range		20-80		%	Adjustable (see Figure 6)
III — Modulation Characteristics (sine, triangle and squarewave):					
Amplitude Modulation:					
Double Sideband					
Modulation Range		0-100		%	See Figure 2
Linearity		0.5		%	for 30% modulation
Sideband Symmetry		1.0		%	
Suppressed Carrier					
Carrier Suppression		52		dB	f < 1 MHz
Frequency Modulation:					
Distortion		0.3		%	See Figure 2 (±10 frequency deviation)

TEST CIRCUITS

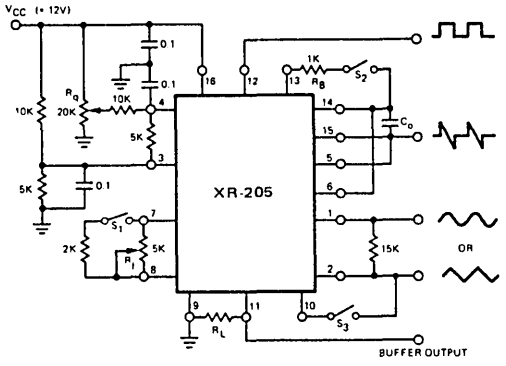


Figure 1. Test Circuit for Single-Supply Operation

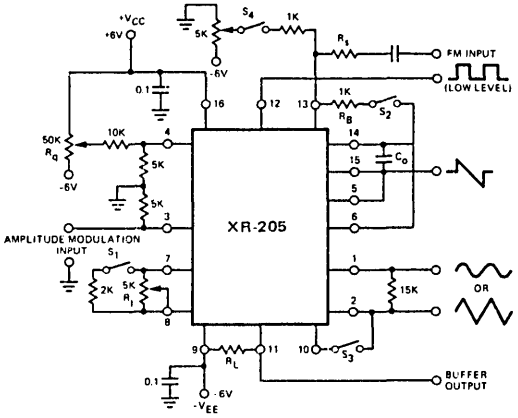


Figure 2. Test Circuit for Split-Supply Operation and AM/FM Modulation

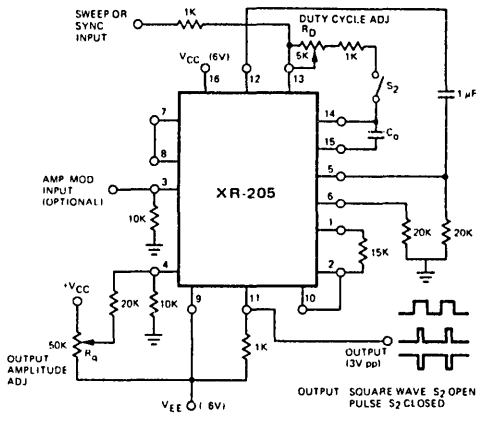


Figure 3. Test Circuit for High-Level Pulse and Squarewave Output

DESCRIPTION OF CIRCUIT CONTROLS

(Refer to functional block diagram)

TIMING CAPACITOR (PINS 14 AND 15)

The oscillator frequency is inversely proportional to the value of the timing capacitor, C_O, connected between pins 14 and 15. With the sweep input open circuited, frequecy f_O can be approximated as: $f_O = 400/C_O$ where f_O is in Hz and C_O is in microforads. (See Figure 4.)

MODULATOR Y-INPUTS (PINS 5 AND 6)

These inputs are normally connected to the oscillator outputs. For sinewave or trianglewave outputs, they are dc coupled to pins 14 and 15 (see Figure 1); for high-level squarewave or pulse output, ac coupling is used as shown in Figure 3.

MODULATOR X-INPUTS (PINS 3 AND 4)

Modulator output (at pins 1 or 2) is proportional to a dc voltage applied across these inputs - (see Figure 5). These inputs can be used for amplitude modulation or, as an output amplitude control. The phase of the output voltage is reversed if the polarity of the dc bias across pins 3 and 4 is reversed; therefore these inputs can be used for phase-shift keyed (PSK) modulation.

MODULATOR OUTPUTS (PINS 1 AND 2)

All of the high level output waveforms are obtained at these terminals. The output waveforms appear differentially between pins 1 and 2. The terminals can, therefore, be used for either in-phase or out-of-phase outputs. Normally, a 15 KΩ load resistor should be connected between these terminals to prevent the output from saturating or clipping at large output voltage swings. This output has a high output impedance and should be buffered.

LOW LEVEL SQUAREWAVE OUTPUT (PIN 12)

The output at this pin is a symmetrical squarewave with 0.7V amplitude and 20 ns rise time. It can be used directly as an output waveform, or amplified to a 3 Vpp signal level using the modulator section of the XR-205 as an amplifier (see Figure 3).

SWEEP OR FM INPUT (PIN 13)

The oscillator frequency increases linearly with an increasing *negative* voltage, V_S, applied to this terminal. Normally a series resistor, R_S ($R_S \approx$ approx. 1 KΩ) is connected in series with this terminal to provide current limiting and linear voltage-to-frequency transfer characteristics. The frequency derivation (for any given modulation level) is inversely proportional to R_S. Typical sweep characteristics of the circuit are shown in Figure 7. For proper operation of the circuit with R_S = 1 KΩ, the sweep voltage, V_S, must be within range: $(V_{SO} - 6) > V_S > (V_{SO} + 1)$ where V_{SO} is the open circuit voltage at pin 13. The frequency of oscillation can also be synchronized to an external source by applying a sync

pulse to this terminal. For R_S = 1 KΩ, a sync pulse of 0.1V to 1V amplitude is recommended.

WAVEFORM ADJUSTMENT (PINS 7 AND 8)

The shape of the output waveform at pins 1 and 2 is controlled by a potentiometer, R_j, connected between these terminals as shown in Figure 1. For sinewave outputs at pins 1 and 2, the value of R_j is adjusted to minimize the harmonic content of the output waveform. This adjustment is independent of frequency and *needs to be done only once.* The output can be converted to a symmetrical triangle waveform by increasing the effective resistance across these terminals. This can be done without changing the potentiometer setting, by opening the switch S_2 as shown in Figures 1-3.

BUFFER INPUT AND OUTPUT (PINS 10 AND 11)

The buffer amplifier can be connected to any of the circuit outputs (pins 1, 2, 12, 14 or 15) to provide low output impedance and high current drive capability. *For proper operation of the buffer amplifier, pin 11 must be connected to the most negative potential in the circuit, with an external load resistor* R_L *(0.75 KΩ <* R_L *< 10 KΩ).* The maximum output current at this pin must not exceed 20 mA.

DUTY CYCLE ADJUSTMENT

The duty-cycle of the *output waveforms* can be adjusted by connecting a resistor R_B across pins 13 and 14, as shown in Figures 1-3. With switch S_2 open, the output waveform will be symmetrical. Duty cycle is reduced as R_B is decreased. (See Figure 6.)

ADDITIONAL GAIN CONTROL

For amplitude modulated output signals, the dc level across pins 3 and 4 is fixed by the modulation index required. In this case, the output amplitude can be controlled without effecting the modulation by connecting a potentiometer between pins 1 and 2.

ON-OFF KEYING

The oscillator can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 1 KΩ, oscillations will stop if the applied potential at pin 13 is raised 3 volts above its open-circuit value.

OUTPUT WAVEFORMS

TRIANGLE OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switches S_1 and S_2 open.

SINEWAVE OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switch S_2 open and S_1 closed. The output waveform is adjusted for minimum harmonic distortion using trimmer resistor R_j connected across pins 7 and 8. Sinusoidal output is obtained from pins 1 or 2 (or pin 11 if the buffer amplifier is used). The amplitude of the output waveform is controlled by the differential dc voltage appearing between pins 3 and 4. This bias can be controlled by potentiometer R_Q. for a differential bias between these terminals of ±2 volts or greater, the output amplitude is maximum and equal to approximately 3 volts p-p.

SAWTOOTH OUTPUT

The circuit is connected as shown in Figures 1 or 2, with switch S_1 open and S_2 closed. Closing S_2 places resistor R_B across pins 13 and 14. This changes the duty cycle of the triangle output and converts it to a sawtooth waveform. The polarity of the sawtooth can be changed by reversing the polarity of the dc bias across pins 3 and 4. If S_1 is closed, the linear sawtooth waveform is converted to the sinusoidal sawtooth waveform of Figure 9A.

RAMP OUTPUT (FIGURE 9B)

For ramp outputs, switch S_3 of Figure 1 or 2 is opened, and pin 10 is shorted to pin 14. This results in a 1.4 volt p-p ramp output at pin 11. The duty cycle of this ramp can be controlled by connecting R_B across pins (13-14) or (13-15).

SQUAREWAVE AND PULSE OUTPUTS

For squarewave outputs, the circuit is connected as shown in Figure 3, with S_2 open. The output can be converted to a pulse by closing S_2. The duty cycle of the pulse output is controlled by potentiometer R_D. The amplitude and polarity of either the pulse or squarewave output can be controlled by potentiometer R_Q.

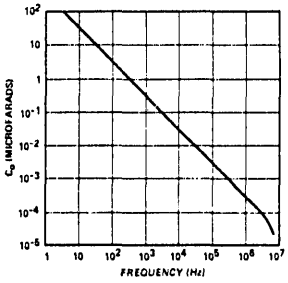


Figure 4. Frequency as a Function of C_0 Across Pins 14 and 15

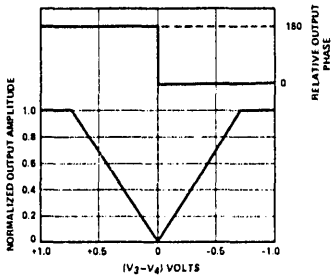


Figure 5. Modular Section Phase and Amplitude Transfer Characteristics

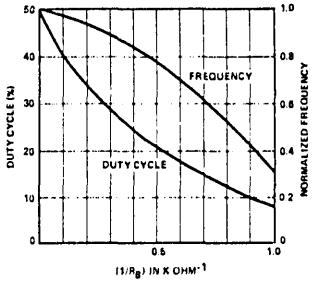


Figure 6. Duty-Cycle and Frequency Variation as a Function of Resistor R_B Connected Across Pins 13 and 14

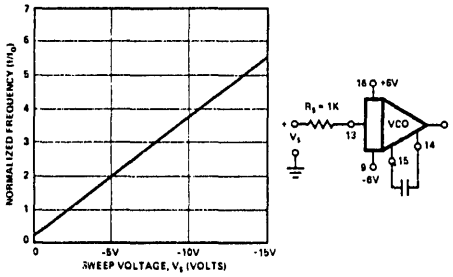


Figure 7. Normalized Frequency vs. Sweep Voltage

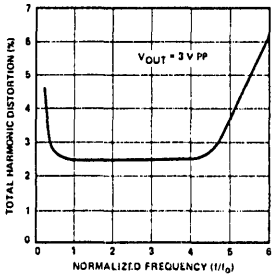


Figure 8. Sinusoidal Output Distortion as a Function of Frequency Sweep

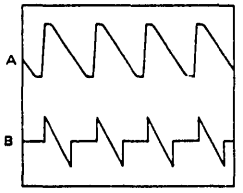
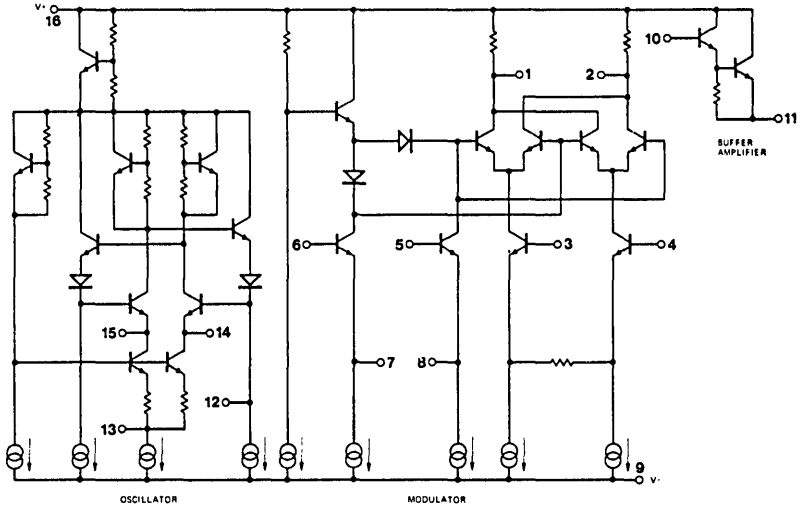


Figure 9. Sinusoidal Sawtooth and Linear Ramp Outputs



EQUIVALENT SCHEMATIC DIAGRAM

Monolithic Function Generator

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range, with an external control voltage, having a very small affect on distortion.

FEATURES

Low-Sine Wave Distortion	0.5%, Typical
Excellent Temperature Stability	20 ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Low-Supply Sensitivity	0.01%V, Typical
Linear Amplitude Modulation	
TTL Compatible FSK Controls	
Wide Supply Range	10V to 26V
Adjustable Duty Cycle	1% to 99%

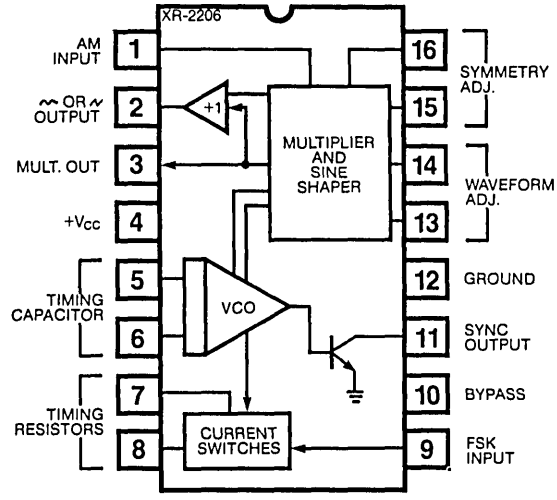
APPLICATIONS

Waveform Generation
Sweep Generation
AM/FM Generation
V/F Conversion
FSK Generation
Phase-Locked Loops (VCO)

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750 mW
Derate Above 25°C	5 mW/°C
Total Timing Current	6 mA
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2206M	Ceramic	−55°C to +125°C
XR-2206N	Ceramic	0°C to +70°C
XR-2206P	Plastic	0°C to +70°C
XR-2206CN	Ceramic	0°C to +70°C
XR-2206CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO actually produces an output frequency proportional to an input current, which is produced by a resistor from the timing terminals to ground. The current switches route one of the timing pins current to the VCO controlled by an FSK input pin, to produce an output frequency. With two timing pins, two discrete output frequencies can be independently produced for FSK Generation Applications.

XR-2206

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = 12V$, $T_A = 25°$, $C = 0.01\ \mu F$, $R_1 = 100\ k\Omega$, $R_2 = 10\ k\Omega$, $R_3 = 25\ k\Omega$ unless otherwise specified. S_1 open for triangle, closed for sine wave.

PARAMETERS	XR-2206M			XR-2206C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Single Supply Voltage	10		26	10		26	V	
Split-Supply Voltage	±5		±13	±5		±13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10\ k\Omega$
OSCILLATOR SECTION								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000\ pF$, $R_1 = 1\ k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50\ \mu F$, $R_1 = 2\ M\Omega$
Frequency Accuracy		±1	±4		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability		±10	±50		±20		ppm/°C	$0°C \leq T_A \leq 70°C$, $R_1 = R_2 = 20\ k\Omega$
Supply Sensitivity		0.01	0.1		0.01		%/V	$V_{LOW} = 10V$, $V_{HIGH} = 20V$, $R_1 = R_2 = 20\ k\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ $R_1 = 1\ k\Omega$, f_L @ $R_1 = 2\ M\Omega$
Sweep Linearity								
10:1 Sweep		2			2		%	$f_L = 1$ kHz, $f_H = 10$ kHz
1000:1 Sweep		8			8		%	$f_L = 100$ kHz, $f_H = 100$ kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	μF	See Figure 4.
Timing Resistors: R_1 & R_2	1		2000	1		2000	k Ω	
Triangle Sine Wave Output								See Note 1, Figure 2.
Triangle Amplitude		160			160		mV/k Ω	Figure 1, S_1 Open
Sine Wave Amplitude	40	60	80		60		mV/k Ω	Figure 1, S_1 Closed
Max. Output Swing		6			6		V p-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Amplitude Stability		4800			4800		ppm/°C	See Note 2.
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	$R_1 = 30\ k\Omega$
With Adjustment		0.4	1.0		0.5	1.5	%	See Figures 6 and 7.
Amplitude Modulation								
Input Impedance	50	100		50	100		k Ω	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		V p-p	Measured at Pin 11.
Rise Time		250			250		nsec	$C_L = 10$ pF
Fall Time		50			50		nsec	$C_L = 10$ pF
Saturation Voltage		0.2	0.4		0.2	0.6	V	$I_L = 2$ mA
Leakage Current		0.1	20		0.1	100	μA	$V_{11} = 26V$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 2.
Note 2: For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

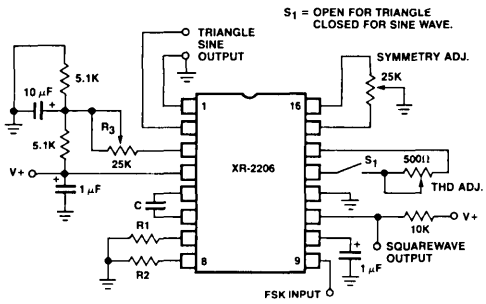


Figure 1. Basic Test Circuit.

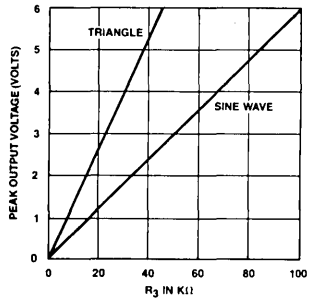


Figure 2. Output Amplitude as a Function of the Resistor, R_3, at Pin 3.

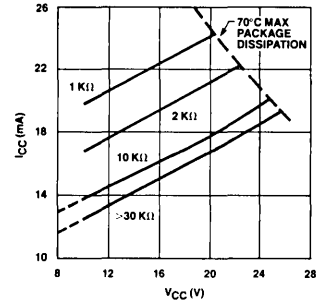


Figure 3. Supply Current versus Supply Voltage, Timing, R.

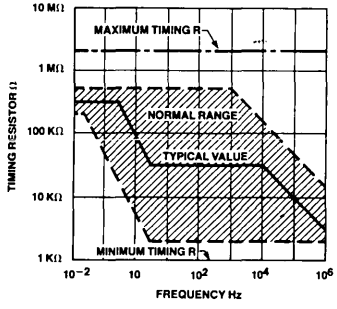


Figure 4. R versus Oscillation Frequency.

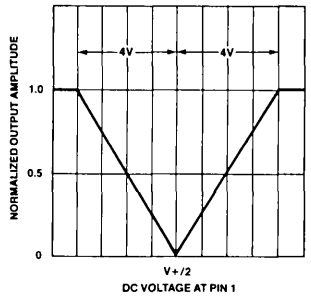


Figure 5. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1).

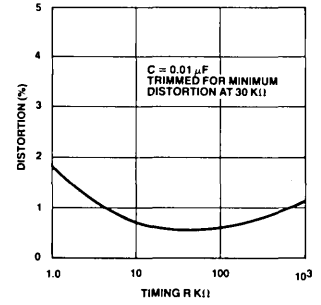


Figure 6. Trimmed Distortion versus Timing Resistor.

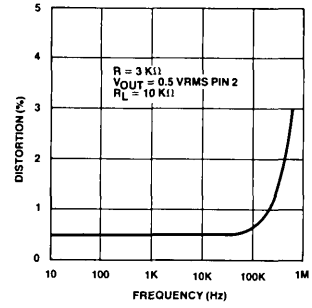


Figure 7. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

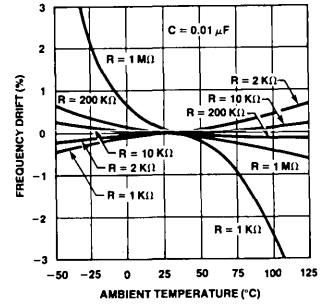


Figure 8. Frequency Drift versus Temperature.

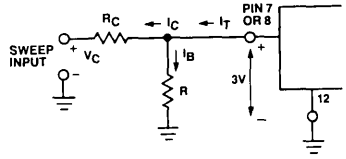


Figure 9. Circuit Connection for Frequency Sweep.

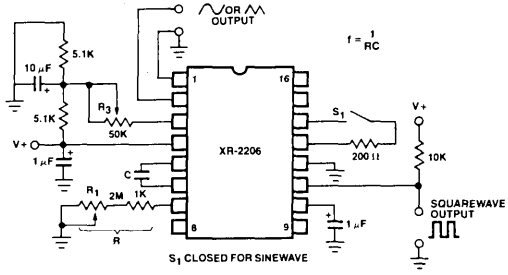


Figure 10. Circuit for Sine Wave Generation without External Adjustment. (See Figure 2 for Choice of R_3).

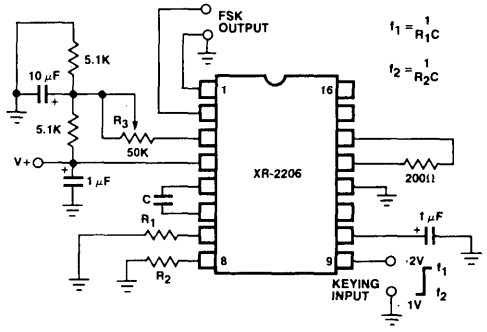


Figure 12. Sinusoidal FSK Generator.

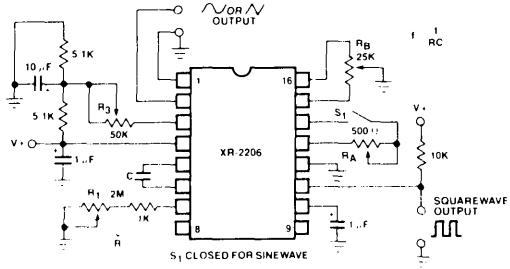


Figure 11. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing—See Figure 2.)

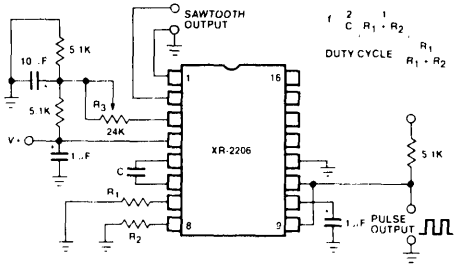


Figure 13. Circuit for Pulse and Ramp Generation.

Frequency-Shift Keying:

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in Figure 12. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage $\geq$2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is $\leq$1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2, as:

$$f_1 = 1/R_1C \text{ and } f_2 = 1/R_2C$$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^-.

Output DC Level Control:

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In Figures 10, 11 and 12, Pin 3 is biased midway between V^+ and ground, to give an output dc level of $\approx V^+/2$.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment:

Figure 10 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is <2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 10 can be converted to split-supply operation, simply by replacing all ground connections with V^-. For split-supply operation, R_3 can be directly connected to ground.

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to $\approx$0.5% by additional adjustments as shown in Figure 11. The potentiometer, R_A, adjusts the sine-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at midpoint and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of Figures 10 and 11 can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 12 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted by the choice of timing resistors, R_1 and R_2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^-.

Pulse and Ramp Generation

Figure 13 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 11), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99% by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1 kΩ to 2 MΩ.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_o, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in Figure 4. Temperature stability is optimum for 4 kΩ < R < 200 kΩ. Recommended values of C are from 1000 pF to 100 μF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320\ I_T\ (\text{mA})}{C\ (\mu\text{F})} \text{ Hz}$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12 Frequency varies linearly with I_T, over a wide range of current values, from 1 μA to 3 mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in Figure 9. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC}\left(1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right)\right) \text{Hz}$$

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f/\partial V_C = -\frac{0.32}{R_C C} \text{ Hz/V}$$

CAUTION: For safety operation of the circuit, I_T should be limited to ≤ 3 mA.

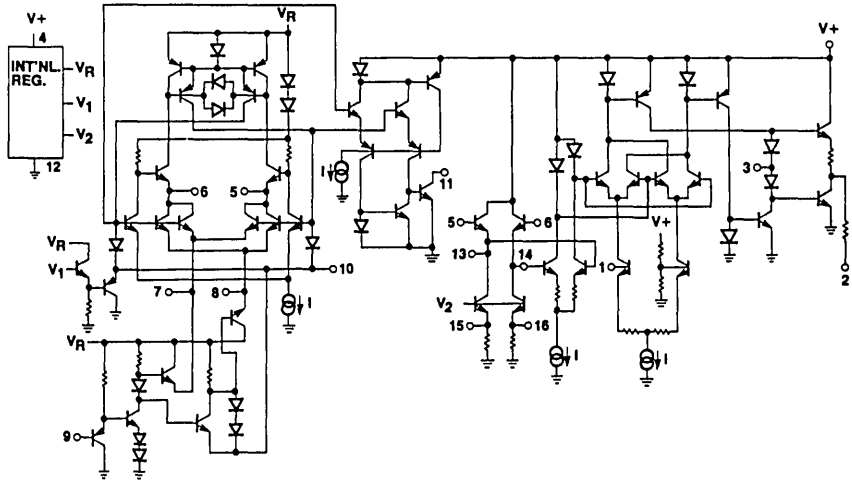
Output Amplitude:

Maximum output amplitude is inversely proportional to the external resistor, R_3, connected to Pin 3 (see Figure 2). For sine wave output, amplitude is approximately 60 mV peak per kΩ of R_3; for triangle, the peak amplitude is approximately 160 mV peak per kΩ of R_3. Thus, for example, R_3 = 50 kΩ would produce approximately ±3V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100 kΩ. Output amplitude varies linearly with the applied voltage at Pin 1, for values of dc bias at this pin, within ±4 volts of $V^+/2$ as shown in Figure 5. As this bias level approaches $V^+/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB.

CAUTION: AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of V^+.



EQUIVALENT SCHEMATIC DIAGRAM

Voltage-Controlled Oscillator

GENERAL DESCRIPTION

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Adjustable Duty Cycle (0.1% to 99.9%)
Two or Four Level FSK Capability
Wide Sweep Range (1000:1 Min)
Logic Compatible Input and Output Levels
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.1%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

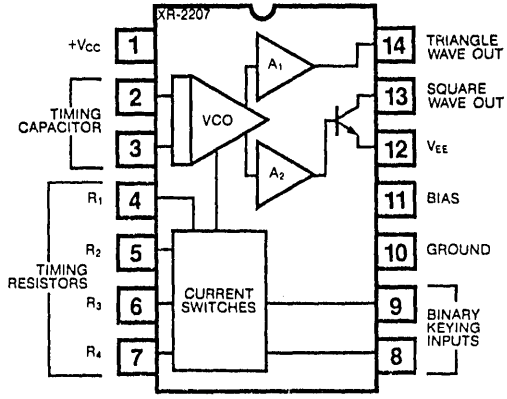
APPLICATIONS

FSK Generation
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Plastic package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR2207M	Ceramic	-55°C to +125°C
XR2207N	Ceramic	0°C to +70°C
XR2207P	Plastic	0°C to +70°C
XR2207CN	Ceramic	0°C to +70°C
XR2207CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2207 utilizes four main functional blocks for frequency generation. These are a voltage controlled oscillator (VCO), four current switches which are activated by binary keying inputs, and two buffer amplifiers for triangle and squarewave outputs. The VCO is actually a current controlled oscillator which gets its input from the current switches. As the output frequency is proportional to the input current, the VCO produces four discrete output frequencies. Two binary input pins determine which timing currents are channelled to the VCO. These currents are set by resistors to ground from each of the four timing terminals.

The triangle output buffer provides a low impedance output (10Ω TYP) while the squarewave is an open-collector type. A programmable reference point allows the XR-2207 to be used in either single or slip supply configurations.

XR-2207

ELECTRICAL CHARACTERISTICS

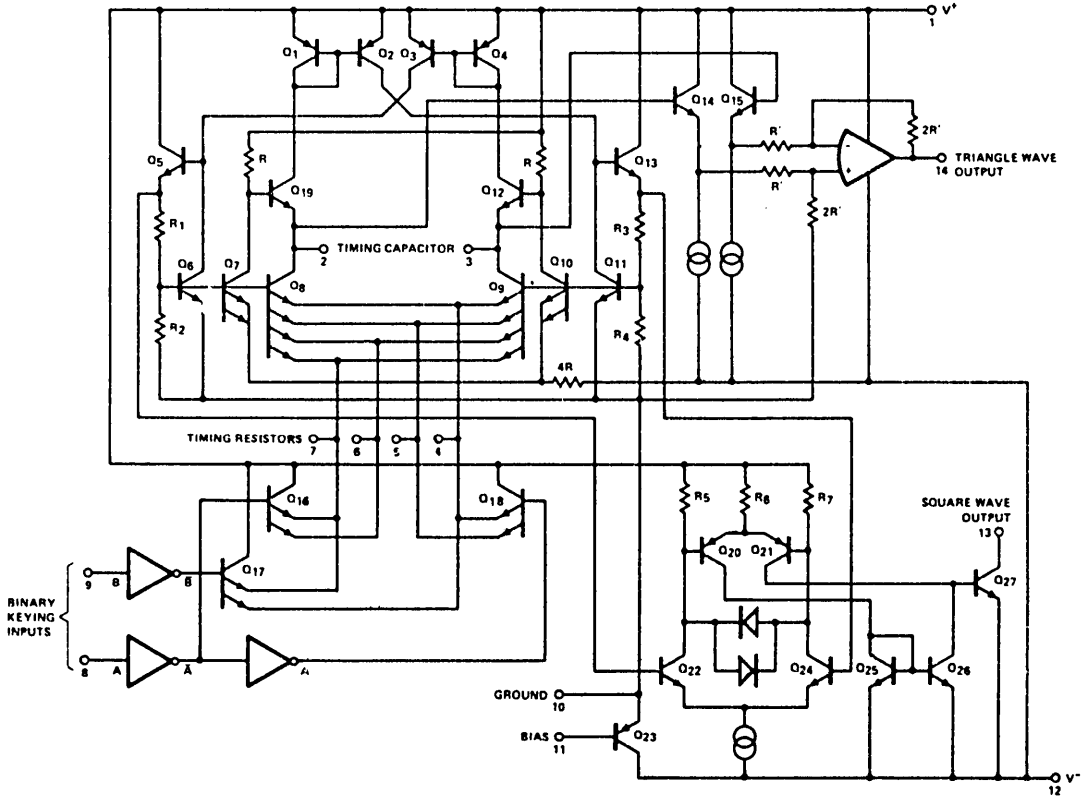
Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, $C = 5000$ pF, $R_1 = R_2 = R_3 = R_4 = 20$ KΩ, $R_L = 4.7$ KΩ, Binary Inputs grounded, S_1 and S_2 closed unless otherwise specified.

PARAMETERS	XR-2207/XR-2207M			XR-2207C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage								
Single Supply	8		26	8		26	V	See Figure 3
Split Supplies	±4		±13	±4		±13	V	
Supply Current								
Single Supply		5	7		5	8	mA	Measured at pin 1, S_1 and S_2 open See Figure 2
Split Supplies								
Positive		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open
Negative		4	6		4	7	mA	Measured at pin 12, S_1, S_2 open
OSCILLATOR SECTION — FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	0.5	1.0		0.5	1.0		MHz	$C = 500$ pF, $R_3 = 2$ KΩ
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50$ μF, $R_3 = 2$ MΩ
Frequency Accuracy		±1	±3		±1	±5	% of f_o	
Frequency Matching		0.5			0.5		% of f_o	
Frequency Stability								
Temperature		20	50		30		ppm/°C	$0°C < T_A < 70°C$
Power Supply		0.15			0.15		%/V	
Sweep Range	1000:1	3000:1			1000:1		f_H/f_L	$R_3 = 1.5$ KΩ for f_{H1} $R_3 = 2$ MΩ for f_L
Sweep Linearity							%	$C = 5000$ pF
10:1 Sweep		1	2		1.5			$f_H = 10$ kHz, $f_L = 1$ kHz
1000:1 Sweep		5			5			$f_H = 100$ kHz, $f_L = 100$ Hz
FM Distortion		0.1			0.1		%	±10% FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	KΩ	See Characteristic Curves
Impedance at Timing Pins		75			75		Ω	Measured at pins 4, 5, 6, or 7
DC Level at Timing Terminals		10			10		mV	
BINARY KEYING INPUTS								
Switching Threshold	1.4	2.2	2.8	1.4	2.2	2.8	V	Measured at pins 8 and 9, Referenced to pin 10
Input Impedance		5			5		KΩ	
OUTPUT CHARACTERISTICS								
Triangle Output								Measured at pin 13
Amplitude	4	6		4	6		V_{pp}	
Impedance		10			10		Ω	
DC Level		+100			+100		mV	Referenced to pin 10
Linearity		0.1			0.1		%	From 10% to 90% to swing
Squarewave Output								Measured at pin 13, S_2 closed
Amplitude	11	12		11	12		V_{pp}	
Saturation Voltage		0.2	0.4		0.2	0.4	V	Referenced to pin 12
Rise Time		200			200		nsec	$C_L \leq 10$ pF
Fall Time		20			20		nsec	$C_L \leq 10$ pF

PRECAUTIONS

The following precautions should be observed when operating the XR-2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the *total current* drawn from pins 4, 5, 6, and 7 be limited to ≤6 mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10 mA.
2. Terminals 2, 3, 4, 5, 6, and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. The keying logic pulse amplitude should not exceed the supply voltage.



EQUIVALENT SCHEMATIC DIAGRAM

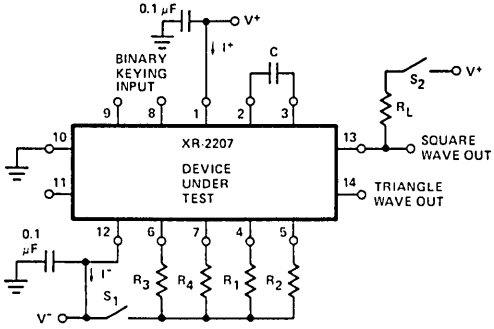


Figure 1. Test Circuit For Split Supply Operation

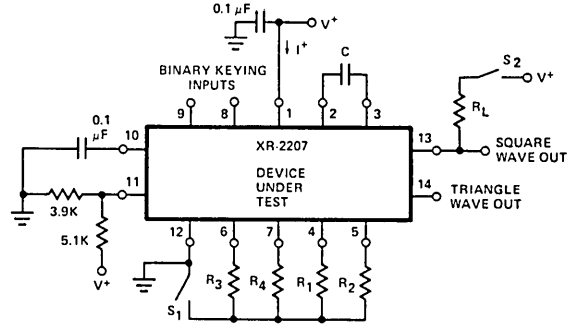


Figure 2. Test Circuit For Single Supply Operation

PRINCIPLES OF OPERATION

TIMING CAPACITOR (PINS 2 AND 3)

The oscillator frequency is inversely proportional to the timing capacitor, C, as indicated in Figure 8. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100 pF to 100 μF. The capacitor should be non-polar.

TIMING RESISTORS (PINS 4, 5, 6, AND 7)

The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 2 KΩ to 2 MΩ; however, for optimum temperature and power supply stability,

recommended values are 4 KΩ to 200 KΩ (see Figures 4, 5, and 7). To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noisy environments, unused or deactivated timing terminals should be bypassed to ground through 0.1 μF capacitors.

SUPPLY VOLTAGE (PINS 1 AND 12)

The XR-2207 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced (see Figures 3 and 4). Performance is optimum for ±6V, or 12V single supply operation.

BINARY KEYING INPUTS (PINS 8 AND 9)

The internal impedance at these pins is approximately 5 KΩ. Keying levels are <1.4V for "zero" and >3V for "one" logic levels referenced to the dc voltage at pin 10 (see Figure 8).

BIAS FOR SINGLE SUPPLY (PIN 11)

For single supply operation, pin 11 should be externally biased to a potential between $V^+/3$ and $V^+/2$ volts (see Figure 2). The bias current at pin 11 is nominally 5% of the total oscillation timing current, I_T.

GROUND (PIN 10)

For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be ac grounded through a 1 μF bypass capacitor. During split supply operation, a ground current of $2I_T$ flows out of this terminal, where I_T is the total timing current.

SQUAREWAVE OUTPUT (PIN 13)

The squarewave output at pin 13 is a "open-collector" stage capable of sinking up to 20 mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1 KΩ to 100 KΩ.

TRIANGLE OUTPUT (PIN 14)

The output at pin 14 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10Ω and is internally protected against short circuits.

BYPASS CAPACITORS

The recommended value for bypass capacitors is 1 μF, although larger values are required for very low frequency operation.

SPLIT SUPPLY OPERATION

Figure 1 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R_1 through R_4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in the logic table (Table 1). If a single timing resistor is activated, the frequency is 1/RC. Otherwise, the frequency is either $1/(R_1 \| R_2)C$ or $1/(R_3 \| R_4)C$.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5 KΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $V^+/2$.

The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6 volt supplies. For operation with unequal supply voltages, see Figure 3.

Note: For Single-Supply Operation, Logic Levels are Referenced to Voltage at Pin 10

SINGLE SUPPLY OPERATION

The circuit should be interconnected as shown in Figure 11 for single supply operation. Pin 12 should be grounded, and pin 11 biased from V^+ through a resistive divider to a value of bias voltage between $V^+/3$ and $V^+/2$. Pin 10 is bypassed to ground through a 1 μF capacitor.

For single supply operation, the dc voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

For a fixed frequency of $f_3 = 1/R_3C$, the external circuit connections can be simplified as shown in Figure 11b.

Table 1
Logic Table for Binary Keying Controls

LOGIC LEVEL		SELECTED TIMING PINS	FREQUENCY	DEFINITIONS
8	9			
0	0	6	f_1	$f_1 = 1/R_3C$, $\Delta f_1 = 1/R_4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C$, $\Delta f_2 = 1/R_1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	1 = >3 V

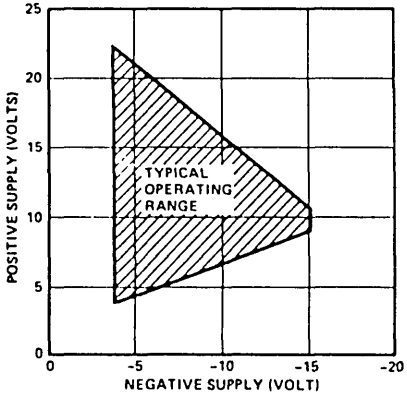


Figure 3. Typical Operating Range For Split Supply Voltage

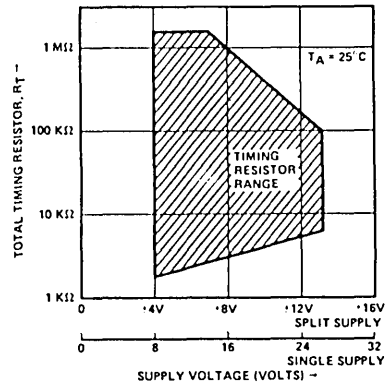


Figure 4. Recommended Timing Resistor Value vs. Power Supply Voltage*

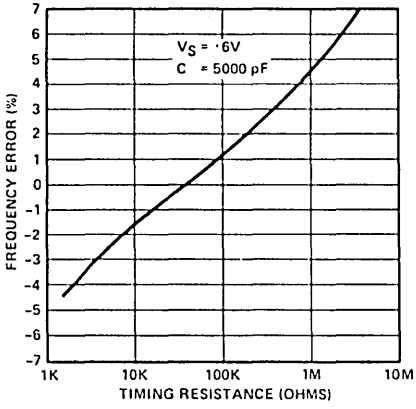


Figure 5. Frequency Accuracy vs. Timing Resistance

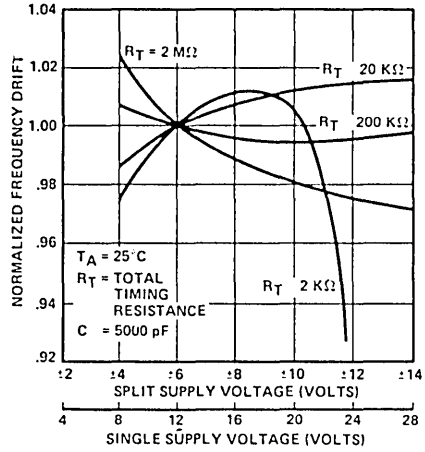


Figure 6. Frequency Drift vs. Supply Voltage

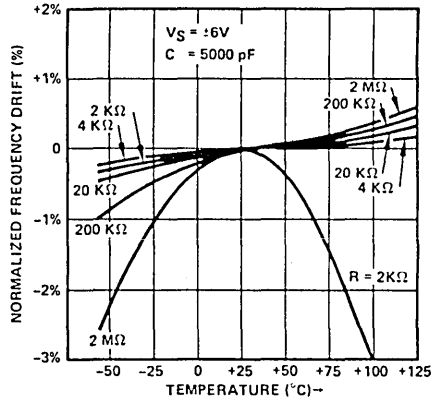


Figure 7. Normalized Frequency Drift With Temperature

LOGIC LEVEL		SELECTED TIMING PINS	FREQUENCY	
A	B			DEFINITIONS
0	0	6	f_1	$f_1 = 1/R_3C, \Delta f_1 = 1/R_4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C, \Delta f_2 = 1/R_1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	1 => 3V

Figure 8. Logic Table For Binary Keying Controls. Note: For Single-Supply Operation, Logic Levels are Referenced to Voltage at Pin 10

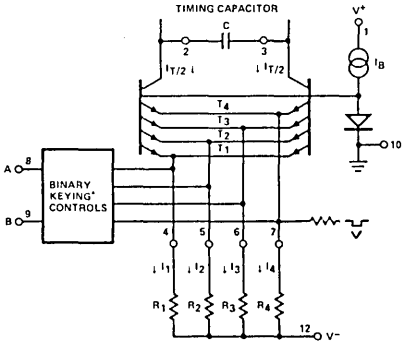


Figure 9. Simplified Schematic of Frequency Control Mechanism

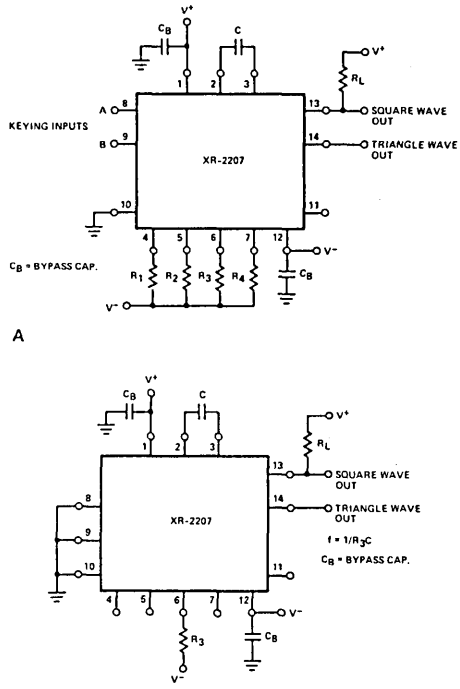


Figure 10. Split-Supply Operation: (a) General (b) Fixed Frequency

FREQUENCY CONTROL (SWEEP AND FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figures 12 & 13.

For split supply operation, a *negative* control voltage, V_C, applied to the circuits of Figures 15 & 16 causes the total timing current, I_T, and the frequency, to increase.

As an example, in the circuit of Figure 12, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation, normally $f = \frac{1}{R_3C}$, is now proportional to the control voltage, V_C, and determined as:

$$f = \frac{1}{R_3C}\left[1 - \frac{V_C R_3}{R_C V-}\right] \text{Hz}$$

The frequency f will increase as the control voltage is made more negative. If $R_3 = 2\ M\Omega$, $R_C = 2\ K\Omega$, C = 5000 pF, then at 1000: 1 frequency sweep would result for a negativ sweep voltage $V_C \simeq V^-$.

The voltage to frequency conversion gain, K, is controlled by the series resistance R_C and can be expressed as:

$$K = \frac{\Delta f}{\Delta V_C} = -\frac{1}{R_C C V-} \text{ Hz/volt}$$

The circuit of Figure 12 can operate both with positive and negative values of control voltage. However, for positive values of V_C with small (R_C/R_3) ratio, the direction of the timing current I_T is reversed and the oscillations will stop.

Figure 13 shows an alternate circuit for frequency control where two timing pins, 6 and 7, are activated. The frequency and the conversion gain expressions are the same as before, except that the circuit would operate only with negative values of V_C. For $V_C > 0$, pin 7 becomes deactivated

and the frequency is fixed at $f = \frac{1}{R_3C}$.

CAUTION

For operation of the circuit, total timing current I_T must be less than 6 mA over the frequency control range.

DUTY CYCLE CONTROL

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

Figure 14 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0,0" and the "1,0" logic states given in Figure 11. Timing pin 5 is activated when the output is "high," and the timing pin is activated when the squarewave output goes to a low state.

The duty cycle of the output waveforms is given as:

$$\text{Duty Cycle} = \frac{R_2}{R_2 + R_3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R_2 + R_3}\right]$$

The frequency can be modulated or swept without changing the duty cycle by connecting R_2 and R_3 to a common control voltage V_C, instead of to V^- (see Figure 15). The sawtooth and the pulse output waveforms are shown in Figure 15.

ON-OFF KEYING

The XR-2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1 Hz) residual oscillations in the "off" state due to internal bias currents. If this effect is undesirable, it can be eliminated by connecting a 10 MΩ resistor from pin 3 to V^+.

TWO-CHANNEL FSK GENERATOR (MODEM TRANSMITTER)

The multi-level frequency shift-keying capability of XR-2207 makes it ideally suited for two-channel FSK generation. A recommended circuit connection for this application is shown in Figure 16.

For two-channel FSK generation, the "mark" and "space" frequencies of the respective channels are determined by the timing resistor pairs (R_1, R_2) and (R_3, R_4). Pin 8 is the "channel-select" control in accord with Figure 11. For a "high" logic level at pin 8, the timing resistors R_1 and R_2 are activated. Similarly, for a "low" logic level, timing resistors R_3 and R_4 are enabled.

The "high" and "low" logic levels at pin 9 determine the respective high and low frequencies within the selected FSK channel.

Recommended component values for various commonly used FSK frequencies are given in Table 1. When only a single FSK channel is used, the remaining channel can be deactivated by connecting pin 8 to either V^+ or ground. In this case, the unused timing resistors can also be omitted from the circuit.

The low and high frequencies, f_1 and f_2, for a given FSK channel can be fine tuned using potentiometers connected in series with respective timing resistors. In fine tuning the frequencies, f_1 should be set first with the logic level at pin 9 in a "low" level.

Typical frequency drift of the circuit for 0°C to 75°C operation is ±0.2%. Since the frequency stability is directly related to the external timing components, care must be taken to use timing components with low temperature coefficients.

FSK TRANSCEIVER (FULL-DUPLEX MODEM)

The XR-2207 can be used in conjunction with the XR-210, FSK demodulator, to form a full-duplex FSK transceiver, or modem. A recommended circuit connection for this application is shown in Figure 20. Table 1 shows the recommended component values for 300-Baud (103-type) and 1200-Baud (202-type) Modem applications.

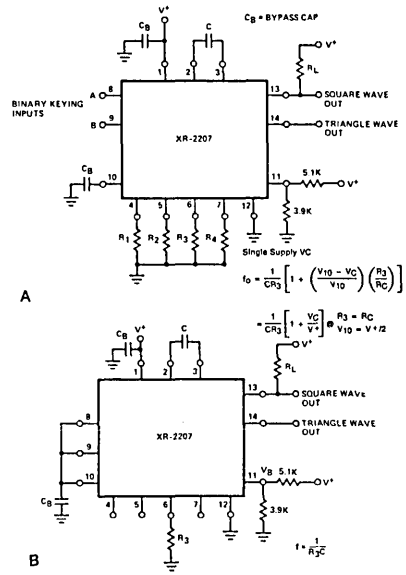


Figure 11. Single Supply Operation:
(a) General
(b) Fixed Frequency

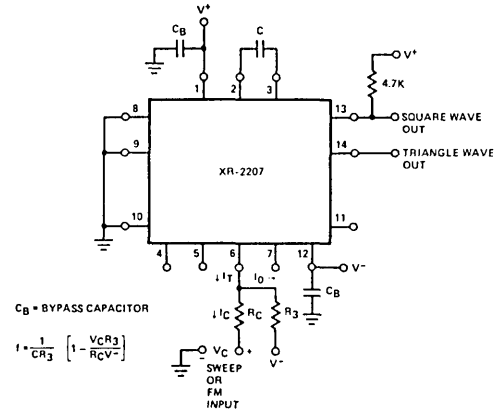


Figure 12. Frequency Sweep Operation

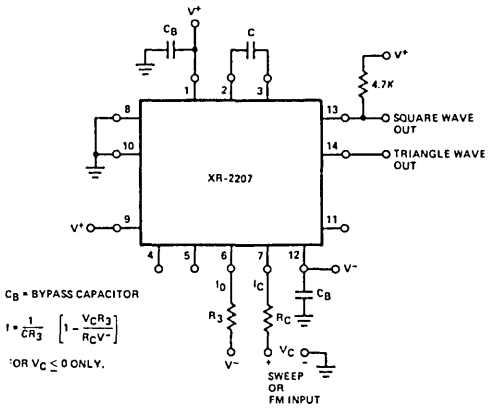


Figure 13. Alternate Frequency Sweep Operation

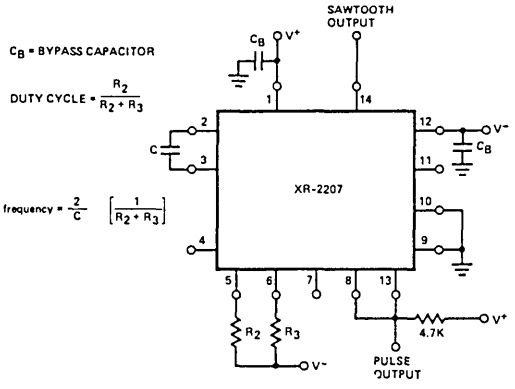


Figure 14. Sawtooth and Pulse Outputs

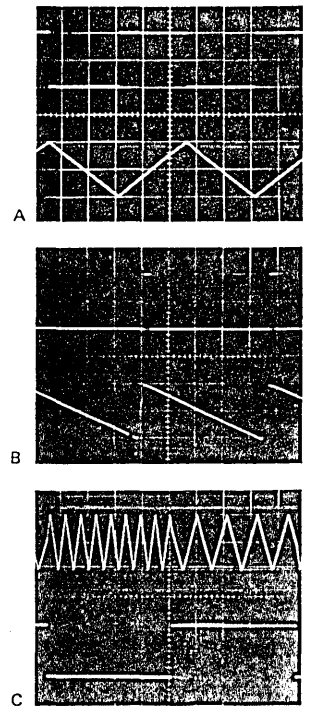


Figure 15. Output Waveforms:
(a) Squarewave and Triangle Outputs
(b) Pulse and Sawtooth Outputs
(c) Frequency-Shift Keyed Output
Top: FSK Output With $f_2 = 2f_1$
Bottom: Keying Logic Input

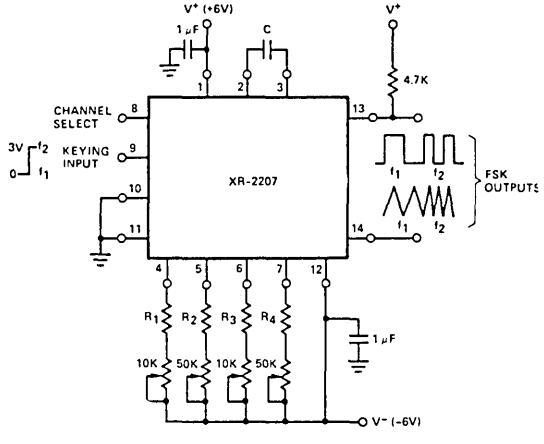


Figure 16. Multi-Channel FSK Generation

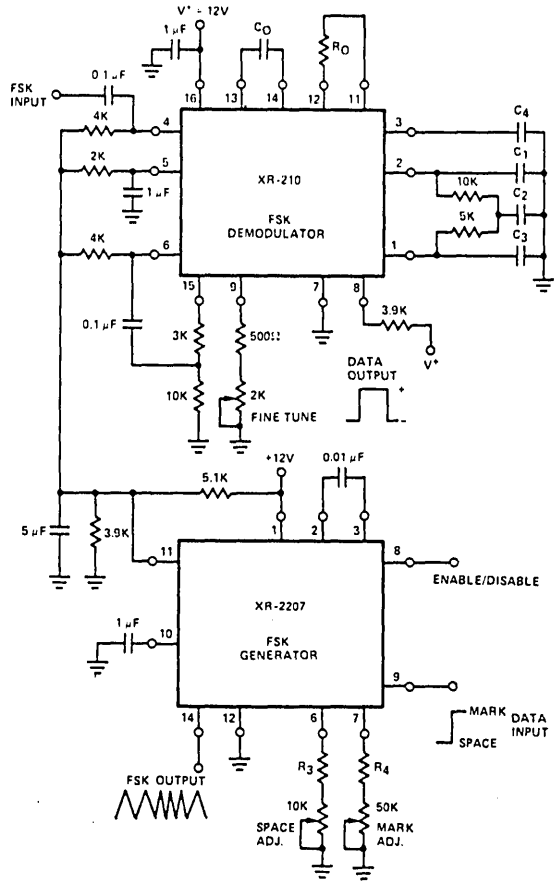


Figure 17. Full Duplex FSK Modem Using XR-210 and XR-2207 (See Table 1 For Component Values)

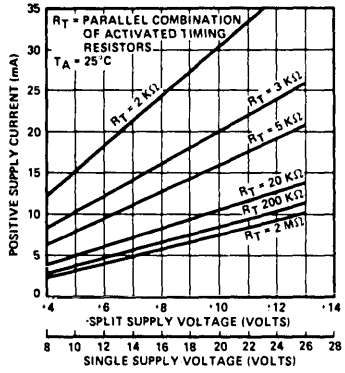


Figure 18. Positive Supply Current, I^+ (Measured at Pin 1) vs. Supply Voltage*

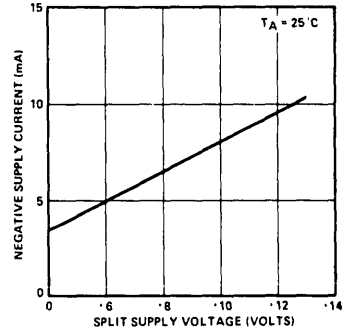


Figure 19. Negative Supply Current, I^- (Measured at Pin 12) vs. Supply Voltage

***Note: R_T = Parallel Combination of Activated Timing Resistors**

Precision Oscillator

GENERAL DESCRIPTION

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. The frequency is set by an external RC product. It is ideally suited for frequency modulation, voltage to frequency or current to frequency conversion, sweep or tone generation as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR-2208.

FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Wide Sweep Range (1000:1 Min)
Wide Supply Voltage Range (±4V to ±13V)
Low Supply Sensitivity (0.15%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

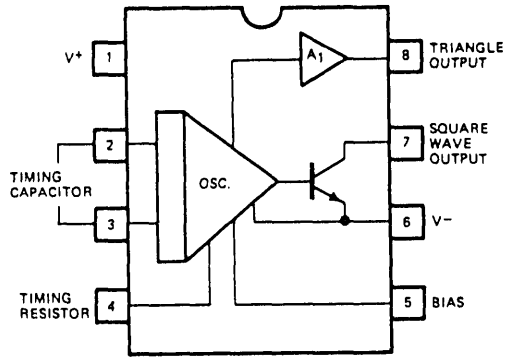
APPLICATIONS

Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
FM and Sweep Generation

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above +25°C	2.5 mW/°C
Operating Temperatue Range	
XR-2209M	−55°C to +125°C
XR-2209C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2209M	Ceramic	−55°C to +125°C
XR-2209CN	Ceramic	0°C to +70°C
XR-2209CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2209 precision oscillator is comprised of three functional blocks: a variable frequency oscillator which generates the basic periodic waveforms and two buffer amplifiers for the triangle and the squarewave outputs. The oscillator frequency, set by an external capacitor, C, and the timing resistor, R, operates over 8 frequency decades, from 0.01 Hz to 1 MHz. With no sweep signal applied, the frequency of oscillation is equal to 1/RC.

The XR-2209 has a typical drift specification of 20 ppm/°C. Its frequency can be linearly swept over a 1000:1 range with an external control signal. Output duty cycle is adjustable from less than 1% to over 99%. The device may operate from either single or split supplies from 8 V to 26 V (±4 V to ±13 V).

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, C = 5000 pF, R - 20 KΩ, R_L = 4.7 kΩ. S_1 and S_2 closed unless otherwise specified.

PARAMETERS	XR-2209M			XR-2209C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage								
Single Supply	8		26	8		26	V	See Figure 2
Split Supplies	±4		±13	±4		±13	V	See Figure 1
Supply Current								
Single Supply		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open See Figure 2
Split Supplies								
Positive		5	7		5	8	mA	Measured at pin 1, S_1, S_2 open
Negative		4	6		4	7	mA	Measured at pin 4, S_1, S_2 open
OSCILLATOR SECTION — FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	0.5	1.0		0.5	1.0		MHz	C = 500 pF, R = 2 KΩ
Lowest Practical Frequency		0.01			0.01		Hz	C = 50 μF, R = 2 MΩ
Frequency Accuracy		±1	±3		±1	±5	% of f_o	
Frequency Stability								
Temperature		20	50		30		ppm/°C	0°C < T_A < 70°C
Power Supply		0.15			0.15		%/V	
Sweep Range	1000:1	3000:1			1000:1		f_H/f_L	R = 1.5 KΩ for f_{H1} R = 2 MΩ for f_L
Sweep Linearity							%	C = 5000 pF
10:1 Sweep		1	2		1.5			f_H = 10 kHz, f_L = 1 kHz
1000:1 Sweep		5			5			f_H = 100 kHz, f_L = 100Hz
FM Distortion		0.1			0.1		%	±10% FM Deviation
Recommended Range of Timing Resistors	1.5		2000	1.5		2000	KΩ	See Characteristic Curves
Impedance at Timing Pin		75			75		Ω	Measured at pin 4
OUTPUT CHARACTERISTICS								
Triangle Output								Measured at pin 8
Amplitude	4	6		4	6		Vpp	
Impedance		10			10		Ω	
Linearity		0.1			0.1		%	10% to 90% of swing
Squarewave Output								Measured at pin 7, S_2 closed
Amplitude	11	12		11	12		Vpp	
Saturation Voltage		0.2	0.4		0.2	0.4	V	Referenced to pin 6
Rise Time		200			200		nsec	$C_L \leq$ 10 pF, R_L = 4.7 KΩ
Fall Time		20			20		nsec	$C_L \leq$ 10 pF

PRECAUTIONS

The following precautions should be observed when operating the XR-2209 family of integrated circuits:

1. Pulling excessive current from the timing terminal will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the *total current* drawn from pin 4 be limited to ≤6 mA.
2. Terminals 2, 3, and 4 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. Triangle waveform linearity is sensitive to parasitic coupling between the square and the triangle-wave outputs (pins 7 and 8). In board layout or circuit wiring care should be taken to minimize stray wiring capacitances between these pins.

DESCRIPTION OF CIRCUIT CONTROLS

TIMING CAPACITOR (PINS 2 and 3)

The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value

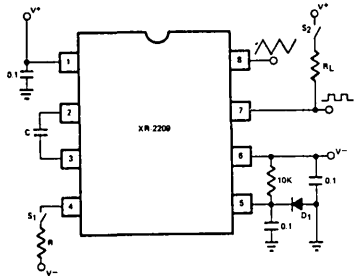


Figure 1. Test Circuit for Split Supply Operation (D_1 = 1N 4148 or Equivalent)

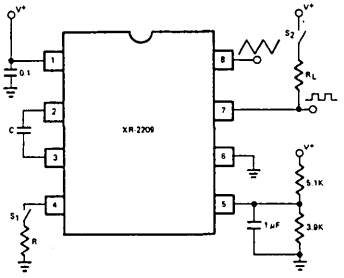


Figure 2. Test Circuit for Single Supply Operation

CHARACTERISTIC CURVES

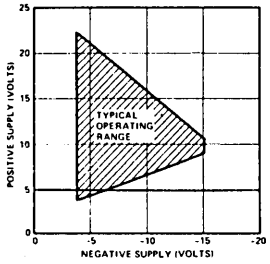


Figure 3. Typical Operating Range For Split Supply Voltage

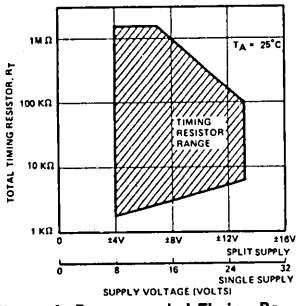


Figure 4. Recommended Timing Resistor Value vs. Power supply Voltage*

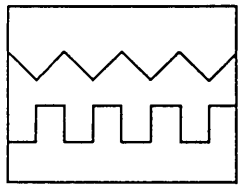


Figure 5. Output Waveforms
Top: Triangle Output (Pin 8)
Bottom: Squarewave Output (Pin 7)

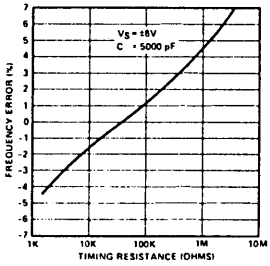


Figure 6. Frequency Accuracy vs. Timing Resistance

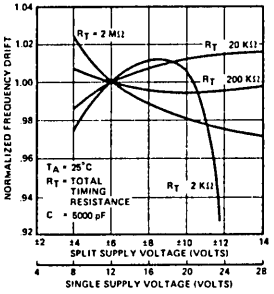


Figure 7. Frequency Drift vs. Supply Voltage

*Note: R_T = Timing Resistor at Pin 4

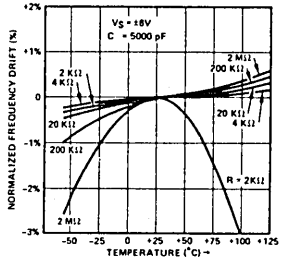


Figure 8. Normalized Frequency Drift With Temperature

RECOMMENDED CIRCUIT CONNECTIONS

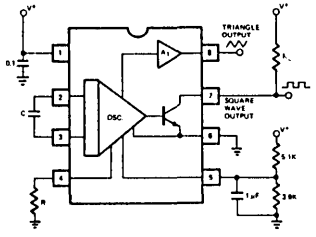


Figure 9. Circuit Connection for Single Supply Operation

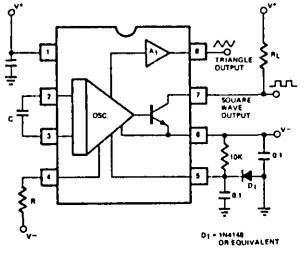


Figure 10. Generalized Circuit Connection for Split Supply Operation

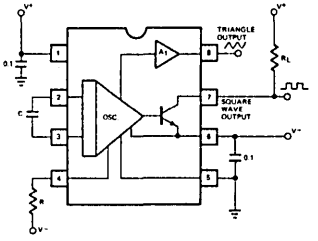


Figure 11. Simplified Circuit Connection for Split Supply Operation With V_{CC} = V_{EE} > ±7V *(Note: Triangle wave output has +0.6V offset with respect to ground.)*

by physical size and leakage current considerations. Recommended values range from 100 pF to 100 μF. The capacitor should be non-polar.

TIMING RESISTOR (PIN 4)

The timing resistor determines the total timing current, I_T, available to charge the timing capacitor. Values for the timing resistor can range from 1.5 KΩ to 2 MΩ; however, for optimum temperature and power supply stability, recommended values are 4 KΩ to 200 KΩ (see Figures 4, 7, and 8). To avoid parasitic pick up, timing resistor leads should be kept as short as possible.

SUPPLY VOLTAGE (PINS 1 AND 6)

The XR-2209 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced (see Figures 3 and 4). Performance is optimum for ±6V, or 12V single supply operation.

BIAS FOR SINGLE SUPPLY (PIN 5)

For single supply operation, pin 5 should be externally biased to a potential between $V^+/3$ and $V^+/2$ volts (see Figure 9). The bias current at pin 5 is nominally 5% of the total oscillation timing current, I_T, at pin 4. This pin should be bypassed to ground with 0.1 μF capacitor.

SQUAREWAVE OUTPUT (PIN 7)

The squarewave output at pin 7 is a "open-collector" stage capable of sinking up to 20 mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1 KΩ to 100 KΩ.

TRIANGLE OUTPUT (PIN 8)

The output at pin 8 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 8 has a very low output impedance of 10Ω and is internally protected against short circuits.

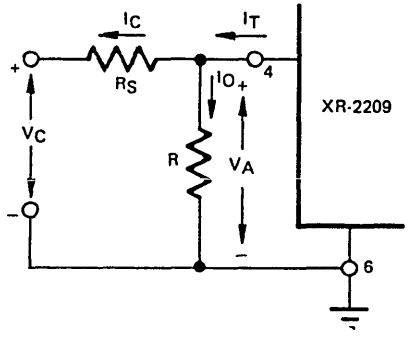


Figure 12. Frequency Sweep Operation

OPERATING INSTRUCTIONS

SPLIT SUPPLY OPERATION

The recommended circuit for split supply operation is shown in Figure 10. Diode D_1 in the figure assures that the triangle output swing at pin 8 is symmetrical about ground. This circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs at ±6V supplies. See Figure 3 for operation with unequal supplies.

Simplified Connection

For operation with split supplies in excess of ±7 volts, the simplified circuit connection of Figure 11 can be used. This circuit eliminates the diode D_1 used in Figure 10; however the triangle wave output at pin 8 now has a +0.6 volt DC offset with respect to ground.

SINGLE SUPPLY OPERATION

The recommended circuit connection for single-supply operation is shown in Figure 9. Pin 6 is grounded; and pin 5 is biased from V^+ through a resistive divider as shown in the figure, and is bypassed to ground with a 1 μF capacitor.

For single supply operation, the DC voltage at the timing terminal, pin 4, is approximately 0.6 volts above V_B, the bias voltage at pin 5.

The frequency of operation is determined by the timing capacitor C and the timing resistor R, and is equal to 1/RC. The squarewave output is obtained at pin 7 and has a peak-to-peak voltage swing equal to the supply voltage. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5 KΩ) to V^+. The triangle waveform obtained at pin 8 is centered about a voltage level V_O where:

$$V_O = V_B + 0.6V$$

where V_B is the bias voltage at pin 5. The peak-to-peak output swing of triangle wave is approximately equal to $V^+/2$.

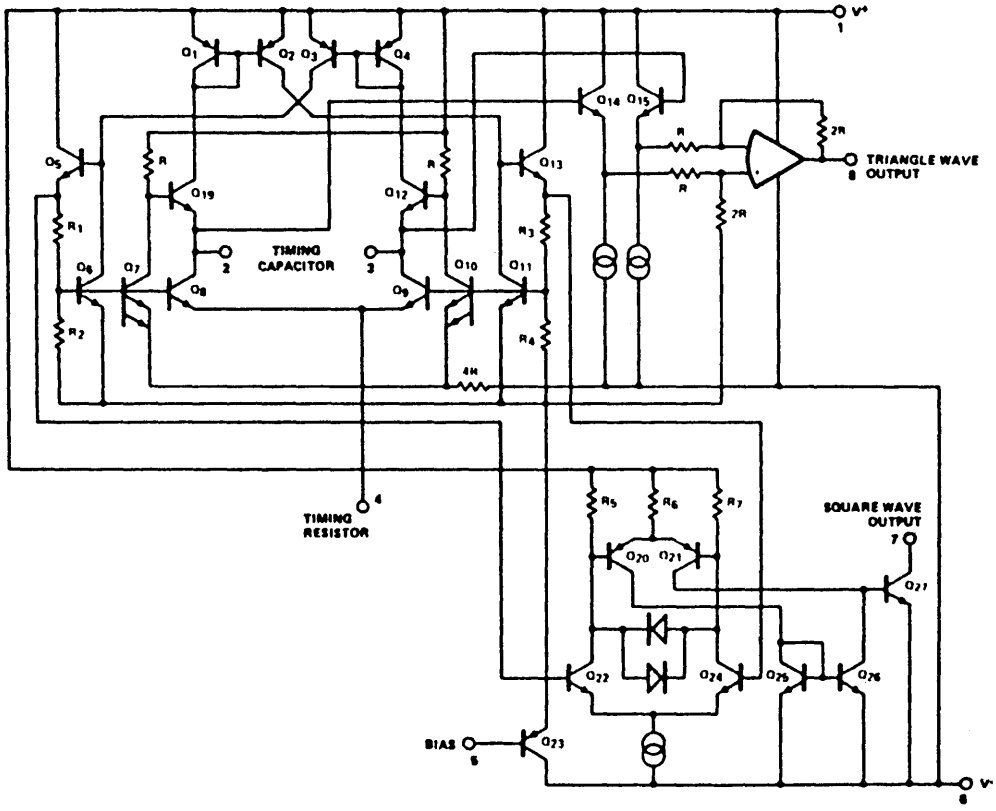
FREQUENCY CONTROL (SWEEP AND FM)

The frequency of operation is proportional to the *total* timing current I_T drawn from the timing pin, pin 4. This timing current, and the frequency of operation can be modulated by applying a control voltage, V_C, to the timing pin, through a series resistor, R_S, as shown in Figure 12. If V_C is negative with respect to V_A, the voltage level at pin 4, then an additional current I_O is drawn from the timing pin causing I_T to increase, thus increasing the frequency. Conversely, making V_C higher than V_A causes the frequency to decrease by decreasing I_T.

The frequency of operation, is determined by:

$$f = f_o\left[1 + \frac{R}{R_S} - \frac{V_C}{V_A}\frac{R}{R_S}\right]$$

where $f_o = 1/RC$.



EQUIVALENT SCHEMATIC DIAGRAM

Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038 is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth and pulse waveforms with a minimum number of external components and adjustments. Its operating frequency can be selected over nine decades of frequency, from 0.001 Hz to 1 MHz by the choice of external R-C components. The frequency of oscillation is highly stable over a wide range of temperature and supply voltage changes. The frequency control, sweep and modulation can be accomplished with an external control voltage, without affecting the quality of the output waveforms. Each of the three basic waveforms, i.e., sinewave, triangle and square wave outputs are available simultaneously, from independent output terminals.

The XR-8038 monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance. It can be readily interfaced with a monolithic phase-detector circuit, such as the XR-2208, to form stable phase-locked loop circuits.

FEATURES

Direct Replacement for Intersil 8038
Low Frequency Drift—50 ppm/°C Max.
Simultaneous Sine, Triangle and Square-Wave Outputs
Low Distortion—THD ≃ 1%
High FM and Triangle Linearity
Wide Frequency Range—0.001 Hz to 1 MHz
Variable Duty-Cycle—2% to 98%

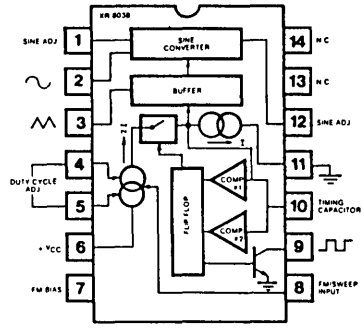
APPLICATIONS

Precision Waveform Generation Sine, Triangle, Square, Pulse
Sweep and FM Generation
Tone Generation
Instrumentation and Test Equipment Design
Precision PLL Design

ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic package	750 mW
Derate above +25°C	6.0 mW/°C
Plastic package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038M	Ceramic	−55°C to +125°C
XR-8038N	Ceramic	0°C to +70°C
XR-8038P	Plastic	0°C to +70°C
XR-8038CN	Ceramic	0°C to +70°C
XR-8038CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-8038 precision waveform generator produces highly stable and sweepable square, triangle and sine waves across nine frequency decades. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, a buffer amplifier and a sine wave converter. Three identical frequency waveforms are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7%, with Pin 1 open and 8 kΩ from Pin 12 to Pin 11 ($-V_{EE}$ or ground). Sine wave distortion may be improved by including two 100 kΩ potentiometers between V_{CC} and V_{EE} (or ground), with one wiper connected to Pin 1 and the other connected to Pin 12.

Frequency sweeping or FM is accomplished by applying modulation to Pins 7 and 8 for small deviations, or only to Pin 8 for large shifts. Sweep range typically exceeds 1000:1.

The square wave output is an open collector transistor; output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typically 1/3 of the supply, and sine wave output reaches 0.22 V_S.

XR-8038

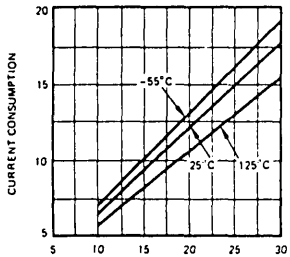
ELECTRICAL CHARACTERISTICS

Test Conditions: $V_S = \pm 5V$ to $\pm 15V$, $T_A = 25°C$, $R_L = 1\ M\Omega$, $R_A = R_B = 10\ k\Omega$, $C_1 = 3300\ pF$, S_1 closed, unless otherwise specified. See Test Circuit of Figure 1.

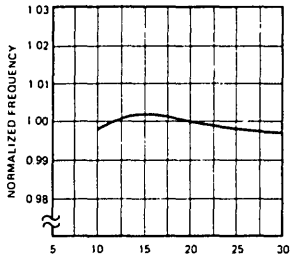
PARAMETERS	XR-8038M/XR-8038			XR-8038C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage, V_S								
Single Supply	10		30	10		30	V	
Dual Supplies	±5		±15	±5		±15	V	
Supply Current		12	15		12	20	mA	$V_S = \pm 10V$. See Note 1.
FREQUENCY CHARACTERISTICS (Measured at Pin 9)								
Range of Adjustment								
Max. Operating Frequency		1			1		MHz	$R_A = R_B = 500\Omega$, $C_1 = 0$, $R_L = 15\ k\Omega$
Lowest Practical Frequency		0.001			0.001		Hz	$R_A = R_B = 1\ M\Omega$, $C_1 = 500\ \mu F$
Max. FM Sweep Frequency		100			100		kHz	
FM Sweep Range		1000:1			1000:1			S_1 Open. See Notes 2 and 3.
FM Linearity		0.1			0.2		%	S_1 Open. See Note 3.
Range of Timing Resistors	0.5		1000	0.5		1000	kΩ	Values of R_A and R_B
Temperature Stability								
XR-8038M		20	50	—	—	—	ppm/°C	
XR-8038		50	100	—	—	—	ppm/°C	
XR-8038C	—	—	—		50		ppm/°C	
Power Supply Stability		0.05			0.05		%/V	See Note 4.
OUTPUT CHARACTERISTICS								
Square-Wave								Measured at Pin 9.
Amplitude	0.9	0.98		0.9	0.98		x V_S	$R_L = 100\ k\Omega$
Saturation Voltage		0.2	0.4		0.2	0.5	V	$I_{sink} = 2\ mA$
Rise Time		100			100		nsec	$R_L = 4.7\ k\Omega$
Fall Time		40			40		nsec	$R_L = 4.7\ k\Omega$
Duty Cycle Adj.	2		98	2		98	%	
Triangle/Sawtooth/Ramp								Measured at Pin 3.
Amplitude	0.3	0.33		0.3	0.33		x V_S	$R_L = 100\ k\Omega$
Linearity		0.05			0.1		%	
Output Impedance		200			200		Ω	$I_{out} = 5\ mA$
Sine-Wave Amplitude	0.2	0.22		0.2	0.22		x V_S	$R_L = 100\ k\Omega$
Distortion								
Unadjusted		0.7	1.5		0.8	3	%	$R_L = 1\ M\Omega$. See Note 5.
Adjusted		0.5			0.5		%	$R_L = 1\ M\Omega$

Note 1: Currents through R_A ad R_B not included.
Note 2: $V_S = 20V$, f = 10 kHz, $R_A = R_B = 10k\Omega$.
Note 3: Apply sweep voltage at Pin 8. $(2/3\ V_S + 2V) \leq V_{sweep} \leq V_S$
Note 4: $10V \leq V_S \leq 30V$ or $\pm 5V \leq V_S \leq \pm 15V$.
Note 5: 81 kΩ resistor connected between Pins 11 and 12.

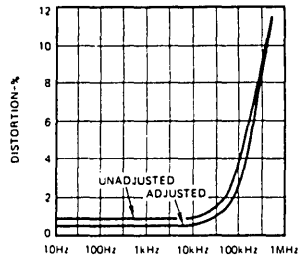
CHARACTERISTIC CURVES



Supply Voltage
Power Dissipation vs. Supply Voltage



Supply Voltage
Frequency Drift vs. Power Supply



Sinewave THD vs. Frequency

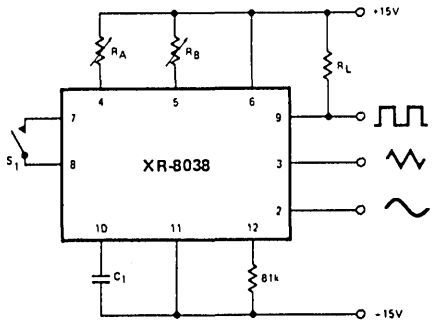


Figure 1. Generalized Test Circuit

WAVEFORM ADJUSTMENT

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 2. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the "Low" state of the square wave.

The magnitude of the triangle waveform is set at 1/3 V_{CC}; therefore, the duration of the rising portion of the triangle is:

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{CC} \times R_A}{1/5 \times V_{CC}} = \frac{5}{3} R_A \times C$$

The duration of the falling portion of the triangle and the sinewave, and the "Low" state of the square wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\, V_{CC}}{\frac{2}{5} \times \frac{V_{CC}}{R_B} - \frac{1}{5} \times \frac{V_{CC}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 2b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorted together, as shown in Figure 2c. This connection, however, carries an inherently larger variation of the duty-cycle.

With two separate timing resistors, the *frequency* is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3} R_A C \left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = 0.3/RC \text{ (for Figure 2a)}$$

If a single timing resistor is used (Figures 2b and c), the frequency is

$$f = 0.15/RC$$

The frequency of oscillation is independent of supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear function of the supply voltage and thus their effects cancel.

DISTORTION ADJUSTMENT

To minimize *sine-wave* distortion the 81 kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 3. This configuration allows a reduction of sine-wave distortion close to 0.5%

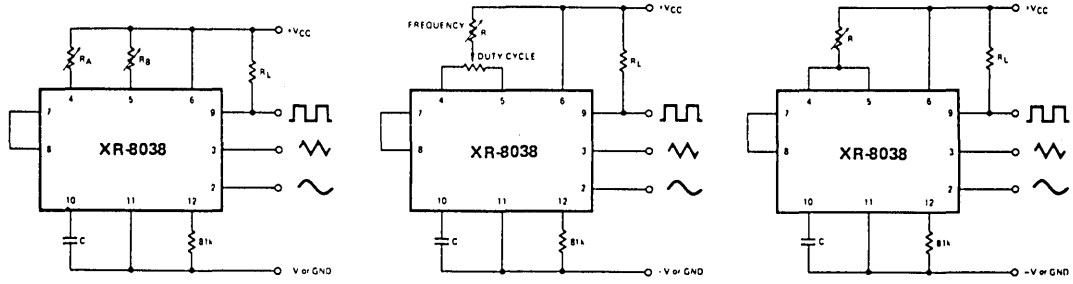


Figure 2. Possible Connections for the External Timing Resistors.

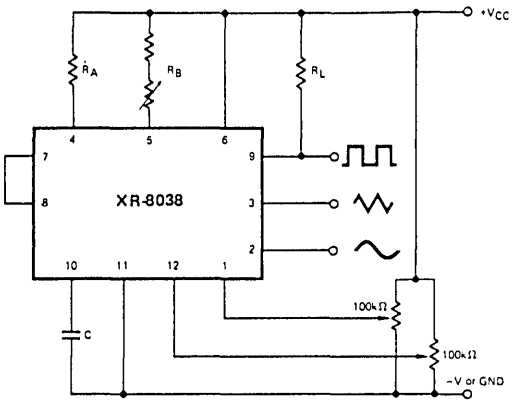


Figure 3. Connection to Achieve Minimum Sine-Wave Distortion.

SELECTING TIMING COMPONENTS

For any given output frequency, there is a wide range of RC combinations that will work. However certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 0.1 μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (1 > 5 mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will be obtained for charging currents of 1 μ to 1 mA. If pins 7 and 8 are shorted together the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times V_{CC}}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{V_{CC}}{5R_A}$$

A similar calculation holds for R_B.

When the duty cycle is greater than 60%, the device may not oscillate every time, unless:

1) the rise times of the V+ is 10x slower than $R_A \cdot C_T$.

2) a 0.1μF capacitor is tied from Pin 7 and 8 to ground.

NOTE: This is only needed if the duty cycle is powered up with $R_A >> R_B$.

SINGLE-SUPPLY AND SPLIT-SUPPLY OPERATION

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between $+V_{CC}$ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output will be TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a higher supply voltage.

FREQUENCY MODULATION AND SWEEP

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from $+V_{CC}$). By altering this voltage, frequency modulation is performed.

For small deviations (e.g., ±10%) the modulating signal can be applied directly to pin 8 by merely providing ac coupling with a capacitor, as shown in Figure 4a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance. Without it (i.e. terminals 7 and 8 connected together), the input impedance is 8kΩ); with it, this impedance increases to (R + 8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 4b). In this way the entire bias for the current sources is created by the modulating signal and a very large (e.g., 1000:1) sweep range is obtained (f = 0 at V_{sweep} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept from V_{CC} to 2/3 V_{CC} −2V.

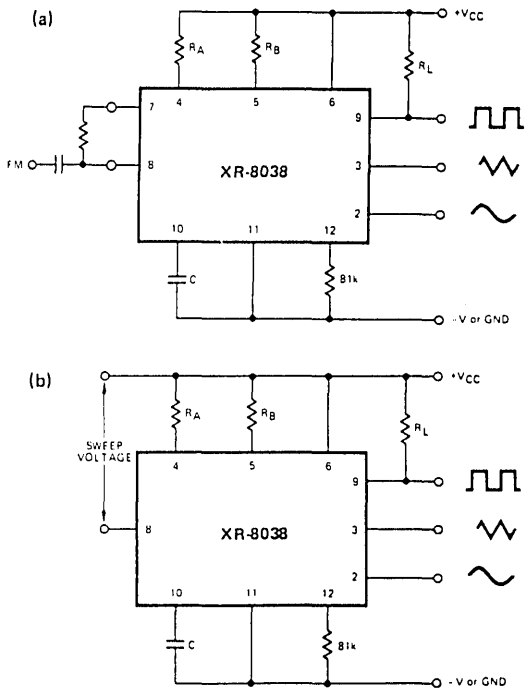


Figure 4. Connections for Frequency Modulation (a) and Sweep (b).

Precision Waveform Generator

GENERAL DESCRIPTION

The XR-8038A is a precision waveform generator IC capable of producing sine, square, triangular, sawtooth, and pulse waveforms, with a minimum number of external components and adjustments. The 8038A allows the elimination of the external distortion adjusting resistor which greatly improves the temperature drift of distortion, as well as lowering external parts count. Its operating frequency can be selected over nine decades of frequency, from 0.001 Hz to 1 MHz, by the choice of external R-C components. The frequency of oscillation is highly stable over a wide range of temperature and supply voltage changes. The frequency control, the sweep, and the modulation can be accomplished with an external control voltage, without affecting the quality of the output waveforms. Each of the three basic waveform outputs, (i.e., sine, triangle and square) are simultaneously available from independent output terminals.

The XR-8038A monolithic waveform generator uses advanced processing technology and Schottky-barrier diodes to enhance its frequency performance. It can be readily interfaced with a monolithic phase-detector circuit, such as the XR-2228 to form stable phase-locked circuits.

FEATURES

Low Frequency Drift 50 ppm/°C, Typical
Simultaneous Sine, Triangle, and Square Wave Outputs
Low Distortion THD 1%
High FM and Triangle Linearity
Wide Frequency Range 0.001 Hz to 1 MHz, Typical
Variable Duty Cycle 2% to 98%
Low Distortion Variation with Temperature

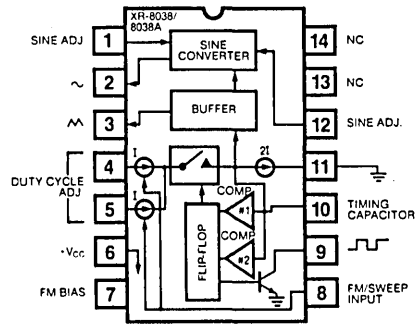
APPLICATIONS

Precision Waveform Generation
Sweep and FM Generation
Tone Generation
Instrumentation and Test Equipment Design
Precision PLL Design

ABSOLUTE MAXIMUM RATINGS

Power Supply	36V
Power Dissipation (package limitation)	
Ceramic Package	750 mW
Derate Above +25°C	6.0 mW/°C
Plastic Package	625 mW
Derate Above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-8038AM	Ceramic	−55°C to +125°C
XR-8038AN	Ceramic	0°C to +70°C
XR-8038AP	Plastic	0°C to +70°C
XR-8038ACN	Ceramic	0°C to +70°C
XR-8038ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-8038A precision waveform generator produces highly stable and sweepable square, triangle, and sine waves across nine frequency decades. The XR-8038A is an advanced version of the XR-8038, with improved sine distortion temperature drift. The device time base employs resistors and a capacitor for frequency and duty cycle determination. The generator contains dual comparators, a flip-flop driving a switch, current sources, a buffer amplifier, and a sine wave convertor. Three identical frequency outputs are simultaneously available. Supply voltage can range from 10V to 30V, or ±5V to ±15V with dual supplies.

Unadjusted sine wave distortion is typically less than 0.7% with the sine wave distortion adjust pin (Pin 1) open. Distortion levels may be improved by including a 100kΩ potentiometer between the supplies, with the wiper connected to Pin 1.

Frequency sweeping or FM is accomplished by applying modulation to Pins 7 and 8 for small deviations, or only Pin 8 for large shifts. Sweep range typically exceed 1000:1.

The square wave output is an open collector transistor; output amplitude swing closely approaches the supply voltage. Triangle output amplitude is typically 1/3 of the supply, and sine wave output reaches $0.22V_S$.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_S = ±5V to ±15V, T_A = 25°C, R_L = 1 MΩ, R_A = R_B = 10 kΩ, C_1 = 3300 pF, S_1 closed, unless otherwise specified.

PARAMETERS	XR-8038AM			XR-8038AC			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Supply Voltage, V_S								
Single Supply	10		30	10		30	V	
Dual Supplies	±5		±15	±5		±15	V	
Supply Current		12	15		12	20	mA	V_S = ±10V (Note 1)
FREQUENCY CHARACTERISTICS (Measured at Pin 9)								
Range of Adjustment								
Max. Operating Frequency		1			1		MHz	R_A = R_B = 500Ω, C_1 = 0, R_L = 15 kΩ
Lowest Practical Frequency		0.001			0.001		Hz	R_A = R_B = 1 MΩ, C_1 = 500 μF
Max. FM Sweep Frequency		100			100		kHz	
FM Sweep Range		1000:1			1000:1			S_1 Open (Note 2 & 3)
FM Linearity		0.1			0.2		%	S_1 Open (Note 3)
Range of Timing Resistors	0.5		1000	0.5		1000	kΩ	Values of R_A and R_B
Temperature Stability								
XR-8038AM		50	100	—	—	—	ppm/°C	T_A = −55°C to +125°C
XR-8038AC					20		ppm/°C	T_A = 0°C to +70°C
Power Supply Stability		0.05			0.05		%/V	(Note 4)
OUTPUT CHARACTERISTICS								
Square-Wave								Measured at Pin 9
Amplitude	0.9	0.98		0.9	0.98		× V_S	R_L = 100 kΩ
Saturation Voltage		0.2	0.4		0.2	0.5	V	I_{sink} = 2 mA
Rise Time		100			100		nsec	R_L = 4.7 kΩ
Fall Time		40			40		nsec	R_L = 4.7 kΩ
Duty Cycle Adjustment	2		98	2		98	%	
Triangle/Sawtooth/Ramp								Measured at Pin 3
Amplitude	0.3	0.33		0.3	0.33		× V_S	R_L = 100 kΩ
Linearity		0.05			0.1		%	
Output Impedance		200			200			I_{out} = 5 mA
Sine-Wave Amplitude	0.2	0.22		0.2	0.22		× V_S	R_L = 100 kΩ
Distortion								
Unadjusted		0.7	1.5		0.8	3	%	R_L = 1 MΩ (Note 5 & 6)
Adjusted		0.5			0.5		%	R_L = 1 MΩ (Note 5 & 6)
ΔTHD/ΔT		0.5			0.3		%	

Note 1: Currents through R_A ad R_B not included.
Note 2: V_S = 20V, f = 10 kHz, R_A = R_B = 10kΩ.
Note 3: Apply sweep voltage at Pin 8. 2/3 $V_S \leq V_{sweep} \leq V_S$N.
Note 4: 10V ≤ V_S ≤ 30V or ±5V ≤ V_S ≤ ±15V.
Note 5: Pin 12 open circuited (No 81 kΩ resistor as standard 8038).
Note 6: Triangle duty cycle set to 50%, use R_A and R_B.

Section 6 – Instrumentation Circuits

Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency buffer amplifier, and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing application. As shown in the functional block diagram, for maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected, with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/buffer amplifier combination extends the small signal 3-db bandwidth to 8-MHz and the transconductance bandwidth to 100 MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability. The XR-2208 operates over a 0°C to 70°C temperature range. The XR-2208M is specified for operation over the military temperature range of −55°C to +125°C.

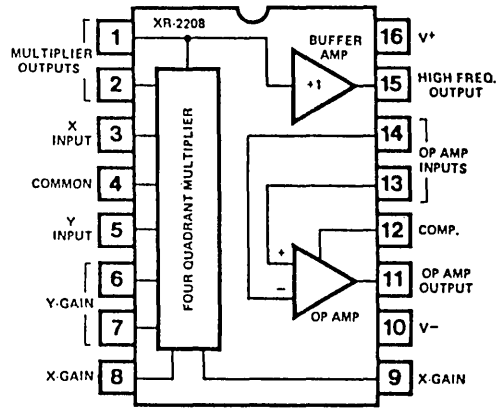
FEATURES

Maximum Versatility
  Independent Multiplier, Op Amp, and Buffer
Excellent Linearity (0.3% typ.)
Wide Bandwidth
  3 dB B.W.—8 MHz typ.
  3° Phase Shift B.W.—1.2 MHz typ.
  Transconductance B.W.—100 MHz typ.
Simplified Offset Adjustments
Wide Supply Voltage Range (±4.5V to ±16V)

APPLICATIONS

Analog Computation
  Multiplication
  Division
  Squaring
  Square-Root
Signal Processing
  AM Generation
  Frequency Doubling
  Frequency Translation
  Synchronous AM Detection
  Triangle-to-Sinewave Converter
  AGC Amplifier
  Phase Detector
Phase-Locked Loop (PLL) Applications
  Motor Speed Control
  Precision PLL
  Carrier Detection
  Phase-Locked AM Demodulation

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply V+	+18 Volts
V−	−18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2208M	Ceramic	−55°C to +125°C
XR-2208N	Ceramic	0°C to +70°C
XR-2208P	Plastic	0°C to +70°C
XR-2208CN	Ceramic	0°C to +70°C
XR-2208CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2228 multiplier/detector contains a four quadrant multiplier and a fully independent operational amplifier. The four quadrant multiplier has fully differential X and Y inputs and outputs. Both inputs have 3 MHz dynamic response and 100 MHz transconductance bandwidth. The operational amplifier features high gain and a large common mode range. The device is powered by 4.5V to 16V split supplies.

For higher frequency applications, consider the XR-2208.

XR-2208

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = ±15V, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-2208/ XR-2208M			XR-2208C			UNITS	FIGURES	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
I. GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	Vdc		See Figure 11
Supply Current		4	7		5	8	mA	2	Measured at Pin 16
II. MULTIPLIER SECTION									
Non-linearity									No external offset trim
(Output Error									
in % of Full Scale)		0.3	0.5		0.5	1.0	%	3	V_Y = ±10V, −10V < V_X < +10V
		0.3	0.5		0.5	1.0	%		V_X = ±10V, −10V < V_Y < +10V
		0.7	1.0		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
									f = 50 Hz
Feedthrough									
a) With Offset Adj.									
X-input		45	80		70	120	mVp-p		V_X = 20 Vp-p V_Y = 0
Y-input		60	100		90	150	mVp-p		V_Y = 20 Vp-p, V_X = 0
b) No Offset Adj.									
X-input		120			200		mVp-p		V_X = 20 Vp-p, V_X = 0
Y-input		120			200		mVp-p		V_Y = 20 Vp-p, V_X = 0
Temperature Coefficient of Scale Factor		±0.07			±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note 1)
Input Bias Current									
X, Y input		2	6		3	8	μA	2	I_3,I_5 of Figure 2
Common input		4	12		6	16	μA	2	I_4 of Figure 2
Input Resistance	0.5	1.0			1.0		MΩ	2	Measured looking into Pin 3 or Pin 5
Output Offset Voltage		50	80		80	140	mV	2	Measured across Pins 1 and 2
Avg. Temp. Drift		0.5			0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response								5	See Definition Section
3-dB Bandwidth									
X-input	6	8		6	8		MHz		
Y-input	3	4		3	4		MHz		
3° Phase-Shift Bandwdith		1.2			1.2		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		6			6		kΩ		Measured looking into Pins 1 or 2
III. BUFFER AMPLIFIER									
Output Impedance		200			200		Ω	5	Measured looking into Pin 15
Gain		1.0			1.0				
IV. OPERATIONAL AMPLIFIER									
Input Offset Voltage		1	3		2	6	mV	6	R_S < 50Ω
Temperature Coefficient of Input Offset Voltage		6	20		9	30	μV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Input Offset Current		4	75		10	100	nA	6	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	6	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	6	$R_L \ge 2K$, V_O = ±10V, f = 20 Hz
Differential Input Resistance	0.5	3			3		MΩ	6	
Output Voltage Swing	±10	±12		±10	±12		V		$R_L \ge 2K$, $T_{LOW} \le T_A \le T_{HIGH}$
Input Common	+12	+14		+12	+14				
Mode Range	−10	−12		−10	−12		V	6	
Common Mode Rejection	70	90		70	90		dB	6	f = 20 Hz
Output Resistance		2			2		kΩ	6	
Slew Rate		0.5			0.5		V/μs	7	Gain = 1, $R_L \ge 2K$ $C_L \le 100$ pF
									C_C = 20 pF
Power Supply Sensitivity		30			30		μV/V	6	$R_S \le 10K$

Note 1: T_{LOW} = −55°C, T_{HIGH} = +125°C for XR-2208M T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2208/XR-2208C

CAUTION: *When using only the op amp or only the multiplier section of the XR-2208, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 3, 4 and 5.*

6

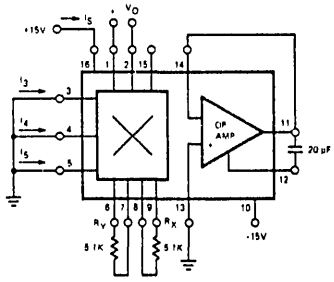


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage.

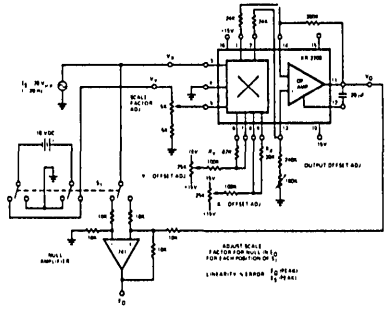


Figure 2. Linearity Test Circuit

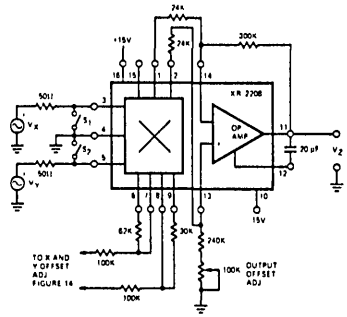


Figure 3. Test Circuit for Feedthrough Measurement. X-Input Feedthrough = V_Z with S_1, open, S_2 closed. Y-Input Feedthrough = V_Z with S_1, closed, S_2 open.

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_Z = K[(V_X + \phi_X)(V_Y + \phi_Y)] + \phi_O$$

where ϕ_X and ϕ_Y are the offset voltages associated with the respective inputs, ϕ_O is the offset voltage of the output, V_Z is the multiplier output, V_X and V_Y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_Z, is related to the X and Y inputs as $V_Z = K(V_X \cdot V_Y)$. The scale factor K has the dimensions of (volts)$^{-1}$ and can be adjusted externally.

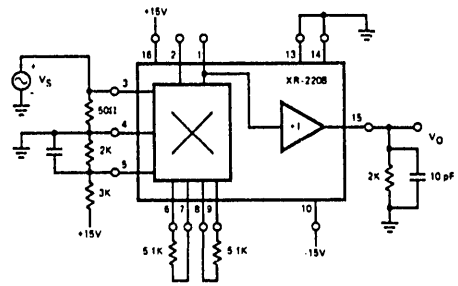


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (For Y-Input, reverse connections between Pin 3 and 5).

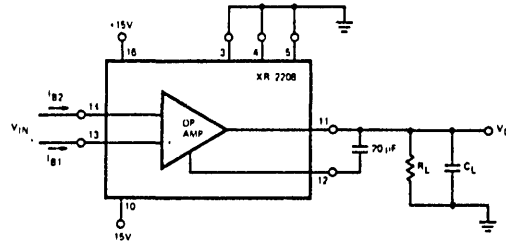


Figure 5. Test Circuit for Op Amp DC Parameters

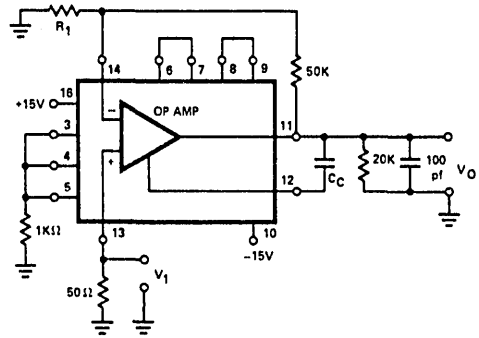


Figure 6. Op Amp AC Test Circuit

TYPICAL CHARACTERISTIC CURVES

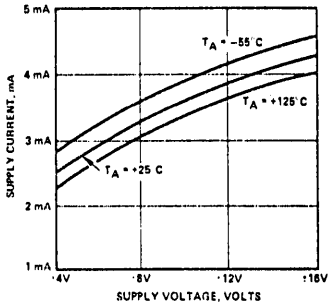


Figure 7. Supply Current vs Supply Voltage

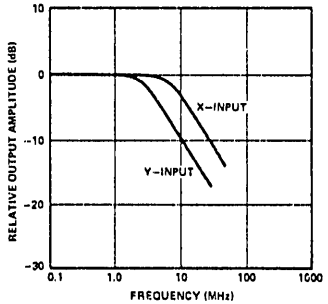


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 15—See Fig. 4).

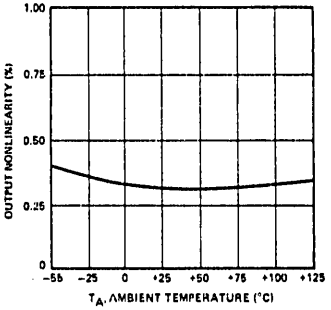


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2).

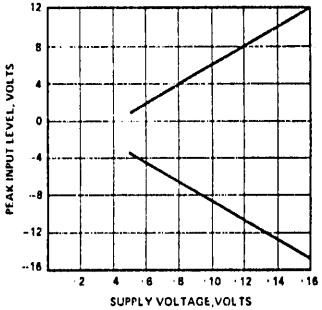


Figure 10. Multiplier Input Dynamic Range vs Power Supply

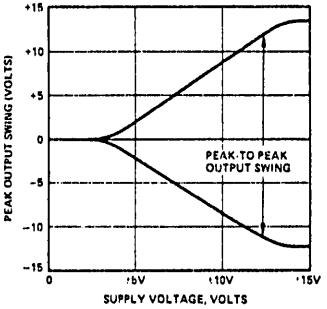


Figure 11. Op Amp Output Swing vs Power Supply

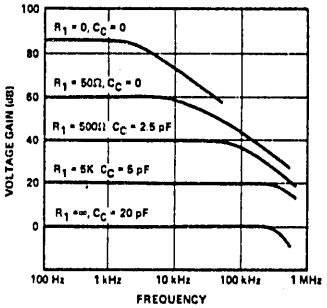


Figure 12. Op Amp Frequency Response

In most arithmetic applications the multiplier and op amp sections of the XR-2208 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_o}{V_x V_y}\right)\left(\frac{V_z}{V_o}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14, V_o is the multiplier output across pins 1 and 2, and V_z is the op amp output at pin 11. With reference to Figure 14, these gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_x R_y}\,(\text{volts})^{-1}; \quad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kΩ.

Thus, overall scale factor K can be adjusted by varying R_x, R_y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

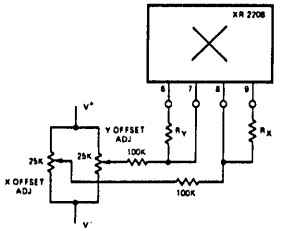


Figure 13. Offset Adjustment

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier bandwidth" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth:* Frequency where the multiplier output is 3-dB below its low frequency (f = 20 Hz) level.

b) *3° Phase Shift Bandwidth:* Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth:* Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth:* Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

DESCRIPTION OF CIRCUIT CONTROLS

MULTIPLIER INPUTS (PINS 3, 4, AND 5)

The X and Y inputs to the multiplier are applied to pins 3 and 5 respectively. The third input (pin 4) is common to both X and Y portions of the multiplier, and in most applications serves as a "reference" or ground terminal. The typical bias current at the multiplier inputs is 3 μA for the X- and Y- inputs and 6 μA for the "common" terminal. In circuit applications such as "synchronous AM detection" or "frequency doubling" where the same input signal is applied to both X and Y inputs, pin 4 can be used as the input terminal since it is common to both X and Y sections of the multiplier.

MULTIPLIER OUTPUTS (PINS 1 AND 2)

The differential output voltage, V_O, across these terminals is proportional to the linear product of voltages V_X and V_Y applied to the inputs. V_O can be expressed as:

$$V_O \approx \left(\frac{25}{R_X R_Y}\right)\left(V_X V_Y\right)$$

where all voltages are in volts and the resistors are in kΩ. R_X and R_Y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply. One of the multiplier outputs (pin 1) is internally connected to the unity-gain buffer amplifier input for high-frequency applications.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 2 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_Z, is then obtained from the op amp output at pin 11, as shown in Figure 14.

X AND Y GAIN ADJUST (PINS 6, 7, 8, 9)

The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_X and R_Y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \approx \frac{25}{R_X R_Y} \quad (\text{volts})^{-1}$$

where R_X and R_Y are in kΩ.

X AND Y OFFSET ADJUST (PINS 7 AND 8)

Two of the gain-control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP INPUTS (PINS 13 AND 14)

Pin 13 is the non-inverting and pin 14 the inverting inputs for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 2). **Note: When the op amp section is not used, these terminals should be grounded.**

OP AMP COMPENSATION (PIN 12)

The op amp section can be compensated for unconditional stability with a 20 pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP OUTPUT (PIN 11)

This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10 mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2208 output, with the op amp inputs being connected to the multiplier outputs.

BUFFER AMPLIFIER OUTPUT (PIN 15)

The buffer amp is internally connected to the multiplier section. The buffer amp has unity voltage gain, and provides a low-impedance output at pin 15 for the multiplier section. The buffer amp is particularly useful for high frequency operation since it minimizes the capacitive loading effects at the multiplier outputs.

The buffer amplifier is activated by connecting a load resistor, R_1, from pin 15 to ground. When it is not used, pin 15 can be left open circuited. However, since the buffer amplifier output is a low impedance point, reasonable care should be taken to avoid burnout due to accidental short circuits. The maximum dc current drawn from pin 15 should be limited to 10 mA. The dc voltage at pin 15 is typically 4.5 volts below V+.

APPLICATIONS INFORMATION

PART I: ARITHMETIC OPERATIONS

Multiplication

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 15 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply OV to both inputs and adjust the output offset to OV using the output offset control.

2. Apply 20V p-p at 50 Hz to the X-input and OV to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.

3. Apply 20V p-p to the Y-input and OV to the X-input. Trim X-offset adjust for minimum peak-to-peak output.

4. Repeat step 1.

5. Apply +10V to both inputs and adjust scale factor for V_O = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

Squaring Circuit

The recommended circuit connection for squaring applications is shown in Figure 15. This circuit is the same as the basic multiplier circuit with both inputs tied together, except only one input offset adjustment is necessary. Trimming procedure for the squaring circuit is as follows:

1. Apply 0 volts to the input and adjust the output offset to zero.

2. Apply 1.0V to the input and adjust the Y-offset until V_O = 0.10V.

3. Apply 10V to the input and adjust the scale factor until V_O = +10V.

4. Apply −10V to the input and check that V_O = +10V. If not, repeat steps 1 through 3. Some compromise may be necessary in scale factor adjustments given in steps 3 and 4.

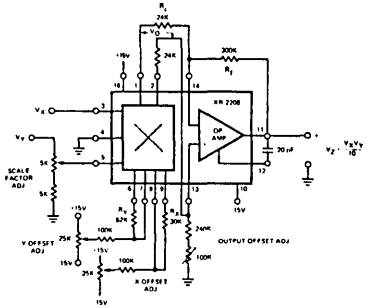


Figure 14. Multiplication Circuit

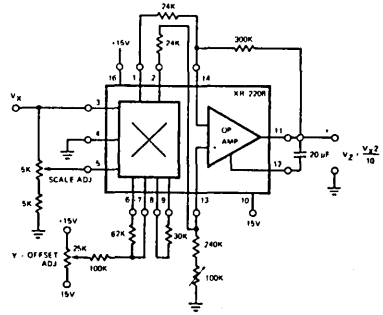


Figure 15. Squaring Circuit

Dividing Circuit

Recommended circuit connection for performing analog division is shown in Figure 16. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, V_O = +10 V_Z/V_X where V_X < 0 and V_Z can have either sign. Positive values of V_X are not allowed, since this will reverse the polarity of the feedback loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2208, and is common to all analog division circuits. The divide circuit is trimmed as follows:

1. Apply V_Z = 0 and trim the output offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

2. Keeping V_Z = 0, and applying V_X = −10V, trim the Y-offset adjust until V_O = 0.

3. Let V_Z = V_X and/or V_Z = $-V_X$ and trim the X-offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

4. Repeat steps 1 and 2 if step 3 required a large initial adjustment.

5. Keeping V_Z = V_X, adjust the scale factor trim for V_O = −10V as V_X is varied from −1V to −10V.

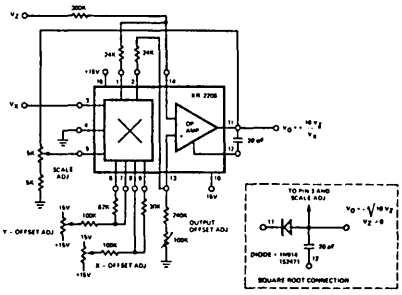


Figure 16. Dividing Circuit

Square Root Circuit

This is essentially the dividing circuit with the X input tied to the output. Thus, the voltage on the Z input is divided by the output voltage, i.e. the output is proportional to the square root of the input. A diode is included in series with the output to prevent a latchup condition which would result if V_Z were allowed to go negative. The square root circuit may be trimmed as a divider by disconnecting the X-input from the output, keeping V_Z > 0 and V_X < 0. The square root circuit may also be trimmed in the closed-loop mode by the following procedure:

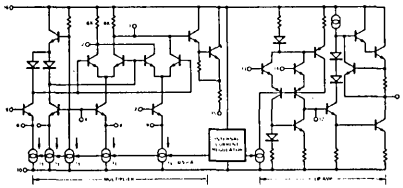
1. Apply V_Z = +0.10V and trim the output offset adjust for V_O = −0.316V.

2. Apply V_Z = +0.9V and trim the X-offset adjust for V_O = −3.0V.

3. Apply V_Z = +10V and trim the scale factor adjust for V_O = −10V.

4. Repeat steps 1 through 3 until desired accuracy is achieved.

EQUIVALENT SCHEMATIC DIAGRAM



PART II: SIGNAL PROCESSING

AM GENERATION

Figure 17 is the recommended circuit connection for generating double side-band (DSB) or suppressed carrier AM signals. Modulation and carrier inputs are applied to the X and Y inputs respectively. The carrier level at the output can be adjusted by the dc voltage applied to pin 3. For suppressed carrier operation, the carrier feedthrough can be further reduced by using the X and Y offset adjustments. In this application, the unity-gain buffer amplifier section will provide a low impedance output if desired. If the buffer amp is not used, pin 15 should be open circuited to reduce power dissipation.

Typical carrier suppression without offset adjustment is 40 dB for frequencies up to 1 MHz, and 30 dB for frequencies up to 10 MHz. For low frequency applications (f < 10 kHz), carrier suppression can be reduced to 60 dB by using the offset adjustment controls.

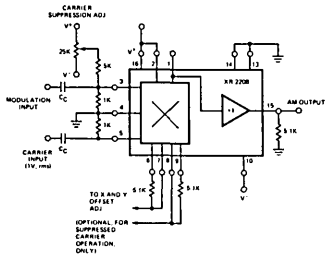


Figure 17. AM Generation

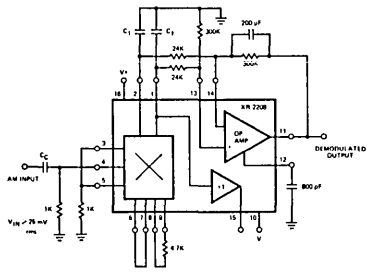


Figure 18. Synchronous AM Detector.

SYNCHRONOUS AM DETECTION

Figure 18 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100 MHz. The AM input signal is applied to the multiplier "common" terminal (pin 4). The Y-gain terminals are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥ 50 mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, at pins 1 and 2 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

TRIANGLE-TO-SINEWAVE CONVERSION

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2208. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 3). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave. For the component values shown in Figure 19, the recommended input signal level at pin 3 is ≈ 300 mV pp in order to obtain a 2V pp sine wave output at pin 15. This waveform can be further amplified using the op amp section to provide high level (10V pp), low distortion output at pin 11.

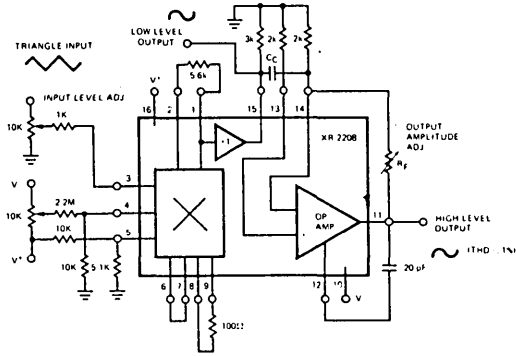


Figure 19. Triangle-to-Sine Converter

PHASE DETECTION

The multiplier section can be used as a phase detector. A recommended circuit connection is shown in Figure 20. The reference input is applied to pin 5, and the input signal whose phase is to be detected is applied to pin 3. The differential dc voltage, V_ϕ, at the multiplier outputs (pins 1 and 2) is related to the phase difference, ϕ, between the two input signals, V_1 and V_2, as:

$$V_\phi = K_d \cos \phi$$

where K_d is the phase detector conversion gain. For input signals ≥50 mV rms, K_d is ≈2V/radian and is independent of signal amplitude. For lower input amplitudes, K_d decreases linearly with the decreasing input level. The capacitors C_1 at pins 1 and 2 provide a low-pass filter with a time constant $T_1 = R_1 C_1$, where R_1 = 6 kΩ is the internal impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2208 to further amplify the output voltage, V_ϕ. The XR-2208 is suitable for phase detection for input frequencies up to 100 MHz.

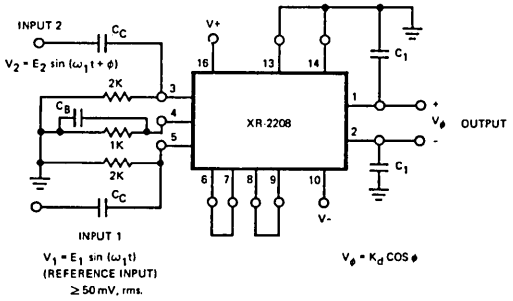


Figure 20. Phase-Detector Circuit

PART III: PHASE-LOCKED LOOP APPLICATIONS

MOTOR SPEED CONTROL

A motor speed control where the frequency of the motor is "phase-locked" to the input reference frequency, f_r, is shown in Figure 21. The multiplier section of the XR-2208 is used as a phase-comparator, comparing the phase of the tachometer output signal with the phase of the reference input. The resulting error voltage across pins 1 and 2 is low-pass filtered by capacitors C_1 and amplified by the op amp section. This error signal is then applied to the motor field-winding to phase-lock the motor speed to the input reference frequency.

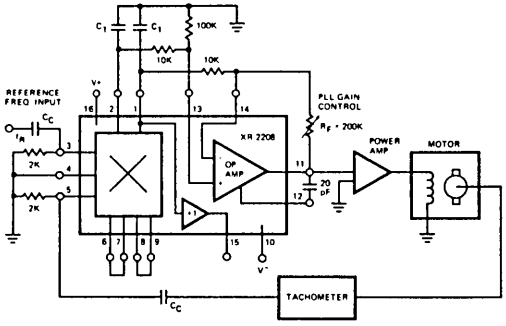


Figure 21. Motor Speed Control Circuit

PRECISION PLL

A precision phase-locked loop may be constructed using an XR-2207 voltage controlled oscillator and an XR-2208. (See Figure 22.) Due to the excellent temperature stability and wide sweep range of the XR-2207 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2208 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30 ppm/°C.

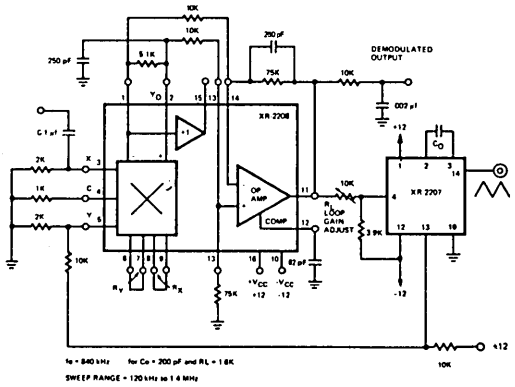


Figure 22. Precision PLL

PHASE-LOCKED AM AND CARRIER DETECTION

The XR-2208 can be used as a "quadrature detector" in conjunction with monolithic PLL circuits to perform phase-locked AM demodulation and for carrier-level detection. Figure 23 shows a recommended circuit connection for such applications. The XR-210 or XR-215 monolithic PLL circuits can be adjusted to lock on the desired input AM signal and re-generate the unmodulated carrier. This carrier frequency appears across the timing capacitor, C_O, of the PLL and is used as the "reference input" to the XR-2208 multiplier. The AM signal is applied simultaneously to the PLL input and to the XR-2208 multiplier input (pin 3), as shown in Figure 23.

The demodulated signal is then low-pass filtered by capacitor C_1 at the multiplier output, and can be amplified further to the desired audio level by using the op amp section of the XR-2208.

In the carrier detector applications, the op amp is used as a voltage comparator and produces a "high" or "low" level logic signal at the op amp output when the input carrier level reaches a detection threshold level set by an external potentiometer. The output from the carrier detector can then be used to enable the "logic-output" stage of the XR-210 FSK modem.

The phase-locked AM or carrier detector system of Figure 23 shows a high degree of frequency selectivity, as determined by the monolithic PLL "capture" bandwidth.

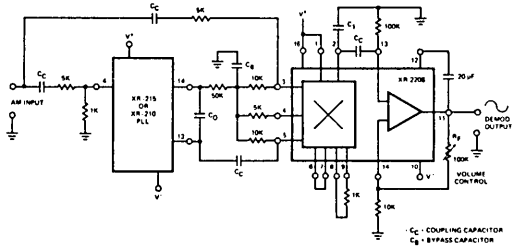


Figure 23. Phase-Locked AM Demodulation or Carrier Detection

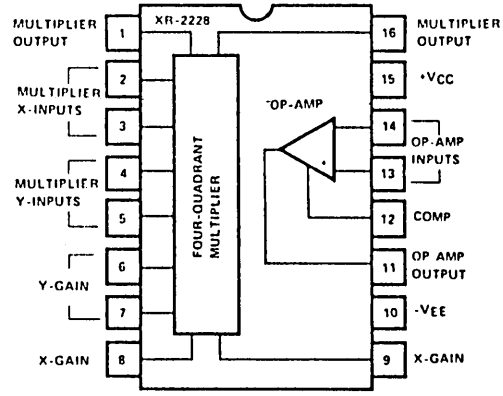
Monolithic Multiplier/Detector

GENERAL DESCRIPTION

The XR-2228 is a monolithic multiplier/detector circuit especially designed for interfacing with integrated phase-locked loop (PLL) circuits, to perform synchronous AM detection and triangle-to-sinewave conversion. It combines a four-quadrant analog multiplier (or modulator) and a high-gain operational amplifier in a single monolithic circuit.

As shown in the equivalent schematic diagram, the four-quadrant multiplier section is designed with fully differential X- and Y-inputs and differential outputs. For maximum versatility, the multiplier and the operational amplifier sections are not internally connected. The operational amplifier can also function as a pre-amplifier for low-level input signals, or as a post-detection amplifier for synchronous demodulation, phase-detection or for sine-shaper applications.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Independent Multiplier and Op Amp Sections
Differential X and Y Inputs
Interfaces with all PLL and VCO Circuits
Wide Common Mode Range
Wide Transconductance Bandwidth (100 MHz, Typ.)
Wide Supply Voltage Range (±4.5V to ±16V)

APPLICATIONS

Phase-Locked Loop Design
Phase Detection
Synchronous AM Detection
AM Generation
Triangle-to-Sinewave Conversion
Frequency Translation

ABSOLUTE MAXIMUM RATINGS

Power Supply	±18 Volts
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mW/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2228M	Ceramic	−55°C to +125°C
XR-2228N	Ceramic	−40°C to +85°C
XR-2228P	Plastic	−40°C to +85°C
XR-2228CN	Ceramic	0°C to +70°C
XR-2228CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2228 multiplier/detector contains a four quadrant multiplier and a fully independent operational amplifier. The four quadrant multiplier has fully differential X and Y inputs and outputs. Both inputs have 3 MHz dynamic response and 100 MHz transconductance bandwidth. The operational amplifier features high gain and a large common mode range. The device is powered by 4.5V to 16V split supplies.

For higher frequency applications, consider the XR-2208.

XR-2228

ELECTRICAL CHARACTERISTICS

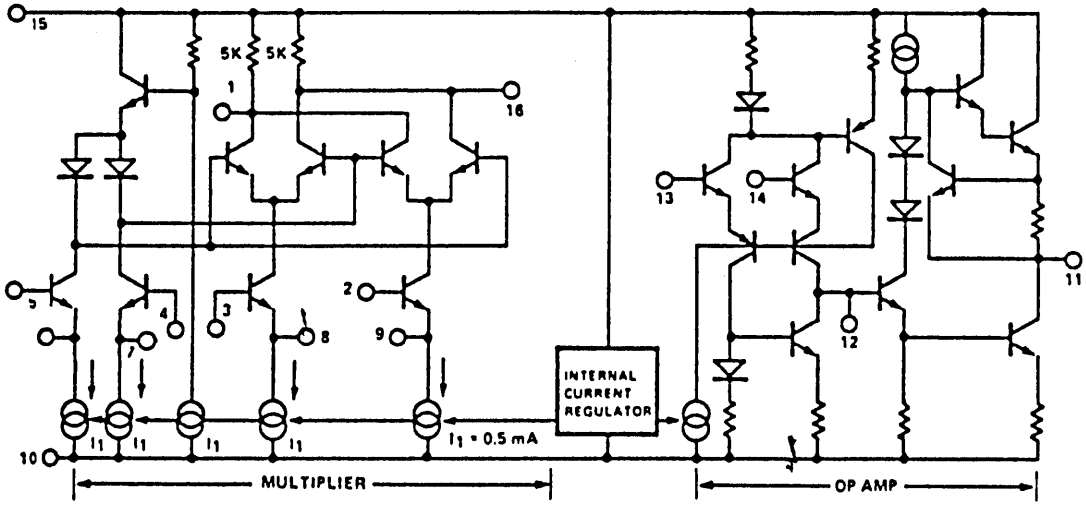
Test Conditions: Supply Voltage = ±15V, T_A = 25°C, unless otherwise specified.

PARAMETERS	XR-2228M			XR-2228/XR-2228C			UNITS	FIGURES	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX			
I. GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	V dc		See Figure 11
Supply Current		4	7		5	8	mA	1	Measured at Pin 15
II. MULTIPLIER/MODULATOR SECTION									
Non-linearity									No external offset trim
(Output Error in % of Full Scale)		0.3	0.5		0.5	1.0	%	2	V_y = ±10V, −10V < V_x < +10V
		0.3	0.5		0.5	1.0	%		V_x = ±10V, −10V < V_y < +10V
		0.7	1.0		0.8		%		$T_{LOW} \leq T_A \leq T_{HIGH}$ (Note 1)
									f = 50 Hz
Feedthrough									
a. With Offset Adj.									
X-input		45	80		70	120	mVp-p	3	V_X = 20 Vp-p V_y = 0
Y-input		60	100		90	150	mVp-p		V_y = 20 Vp-p, V_X = 0
b. No Offset Adj.									
X-input		120			200		mVp-p		V_X = 20 Vp-p, V_X = 0
Y-input		120			200		mVp-p		V_y = 20 Vp-p, V_X = 0
Temperature Coefficient of Scale Factor		±0.07			±0.07		%/°C		$T_{LOW} \leq T_A \leq T_{HIGH}$ (Note 1)
Input Bias Current									
X or Y inputs		2	6		3	8	μA	1	Measured at Pins 2, 3, 4 or 5.
Input Resistance	0.5	1.0			1.0		MΩ	2	Measured at Pins 2, 3, 4 or 5.
Output Offset Voltage		50	80		80	140	mV	2	Measured across Pins 1 and 16
Avg. Temp. Drift		0.5			0.5		mV/°C		$T_{LOW} \leq T_A \leq T_{HIGH}$
Dynamic Response								4	See Definition Section
3-dB Bandwidth									
X-input	1	3		1	3		MHz		
Y-input	1	3		1	3		MHz		
3° Phase-Shift Bandwidth		1			1		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		5			5		kΩ		Measured looking into Pins 1 or 16
III. OPERATIONAL AMPLIFIER SECTION									
Input Offset Voltage		1	3		2	6	mV	5	R_S < 50Ω
Temp. Coef. of Input Offset Voltage		6	20		9	30	μV/°C		$T_{LOW} \leq T_A \leq T_{HIGH}$
Input Offset Current		4	75		10	100	nA	5	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	5	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	5	$R_L \geq 2K$, V_O = ±10V, f = 20 Hz
Differential Input Resistance	0.5	3			3		MΩ	5	
Output Voltage Swing	±10	±12		±10	±12		V		$R_L \geq 2K$, $T_{LOW} \leq T_A \leq T_{HIGH}$
Input Common Mode Range	+12	+14		+12	+14		V	5	
	−10	−12		−10	−12				
Common Mode Rejection	70	90		70	90		dB	5	f = 20 Hz
Output Resistance		2			2		kΩ	5	
Slew Rate		0.5			0.5		V/μs	5	Gain = 1, $R_L \geq 2K$, $C_L \leq 100$ pF C_C = 20 pF
Power Supply Sensitivity		30			30		μV/V	5	$R_S \leq 10K$

Note 1: T_{LOW} = −55°C, T_{HIGH} = +125°C for XR-2228M T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2228C
T_{LOW} = −40°C, T_{HIGH} = +85°C for XR-2228

CAUTION: *When using only the op amp or only the multiplier section of the XR-2228, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 2, 3, 4 and 5.*

6



EQUIVALENT SCHEMATIC DIAGRAM

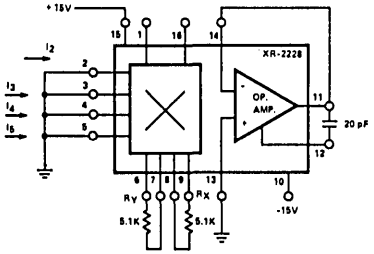


Figure 1. Test Circuit for Quiescent Supply Current, Multiplier Input Bias and Output Offset Voltage

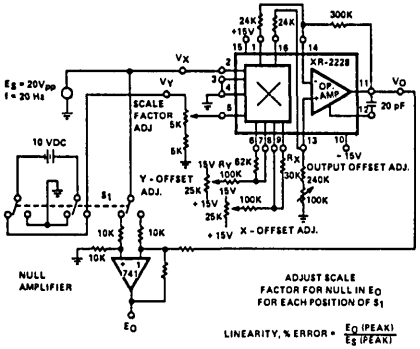


Figure 2. Linearity Test Circuit

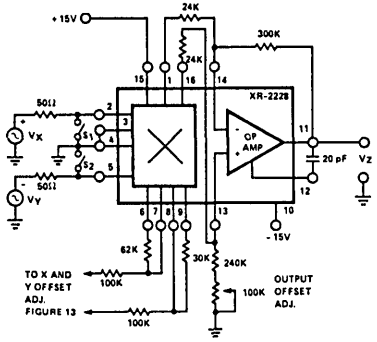


Figure 3. Test Circuit for Feedthrough Measurement. X-Input Feedthrough = V_Z with S_1, open S_2 closed. Y-Input Feedthrough = V_Z with S_1 closed, S_2 open.

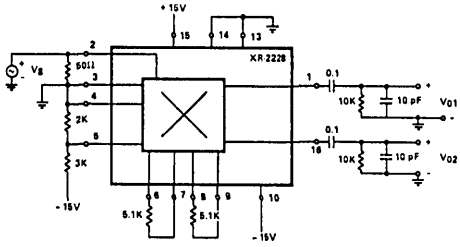


Figure 4. Test Circuit for Multiplier Small-Signal Bandwidth for X-Input (For Y-Input, reverse connections between Pins 2 and 5)

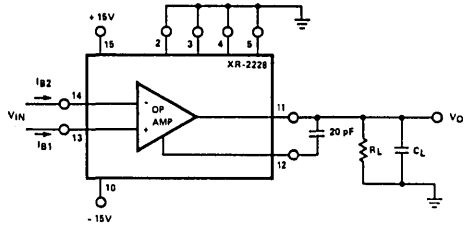


Figure 5. Test Circuit for Op Amp DC Parameters

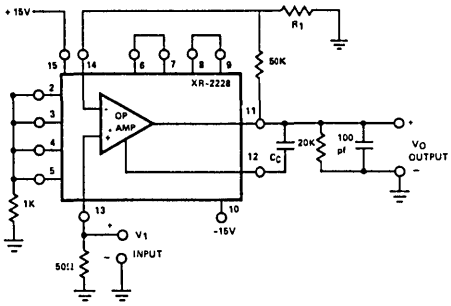


Figure 6. Op Amp AC Test Circuit

DEFINITION OF MULTIPLIER TERMS

NONLINEARITY: Nonlinearity is the maximum deviation of the output voltage from a straight-line transfer function. It is measured separately for the X and Y inputs and is specified as (%) of full scale output.

FEEDTHROUGH: The amount of peak-to-peak output voltage present with one input grounded and a specified peak-to-peak input applied to the other input. Feedthrough is a function of multiplier offsets and can be minimized by offset adjustment (see Figure 13).

OFFSET VOLTAGES: A four-quadrant analog multiplier has three separate offsets: the X and Y input offsets and the output offset. The transfer function of a practical multiplier with scale factor K can be written as:

$$V_Z = K[(V_X + \phi_X)(V_Y + \phi_Y)] + \phi_O$$

where ϕ_X and ϕ_Y are the offset voltages associated with the respective inputs, ϕ_O is the offset voltage of the output. V_Z is the multiplier output, V_X and V_Y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

TYPICAL CHARACTERISTICS CURVES

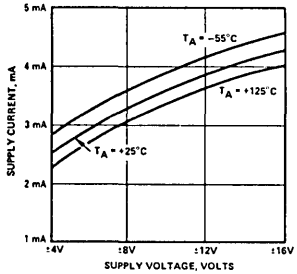


Figure 7. Supply Current vs Supply Voltage

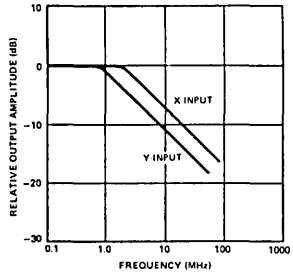


Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 16—See Fig. 4)

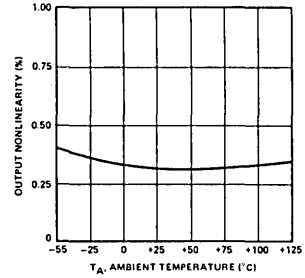


Figure 9. Temperature Dependence of Output Nonlinearity for X or Y Inputs (See Figure 2)

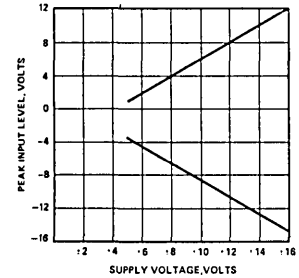


Figure 10. Multiplier Input Dynamic Range vs Power Supply

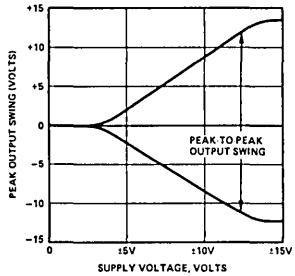


Figure 11. Op Amp output Swing vs Power Supply

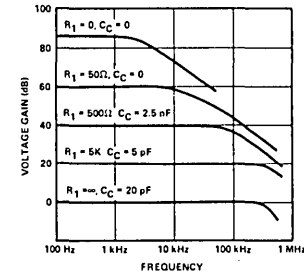


Figure 12. Op Amp Frequency Response

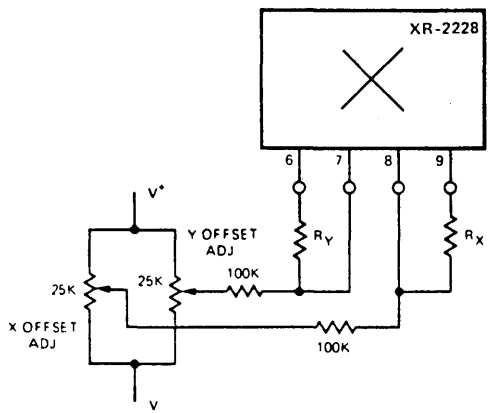


Figure 13. Offset Adjustment

where ϕ_X and ϕ_Y are the offset voltages associated with the respective inputs, ϕ_O is the offset voltage of the output. V_Z is the multiplier output, V_X and V_Y are the multiplier inputs. As shown in Figures 13 and 14, each of these offset voltages can be nulled to zero by external adjustments.

SCALE FACTOR, K: The constant of proportionality that relates the multiplier output to the X and Y inputs. If the offset terms are neglected, the multiplier output, V_Z, is related to the X and Y inputs as $V_Z = K(V_X \cdot V_Y)$. The scale factor K has the dimensions of $(volts)^{-1}$ and can be adjusted externally.

In most arithmetic applications the multiplier and op amp sections of the XR-2228 are interconnected as shown in Figure 14. In such applications, over-all scale factor K can be written as:

$$K = (K_m)(K_a) = \left(\frac{V_O}{V_X Y_X}\right)\left(\frac{V_Z}{V_O}\right)$$

where K_m is the gain constant of the multiplier section, and K_a is the gain of the op amp stage in Figure 14. V_O is the multiplier output across pins 1 and 16, and V_Z is the op amp output at pin 11. With reference to Figure 14, the gain constants can be expressed as:

$$K_m \simeq \frac{25}{R_X R_Y}\,(volts)^{-1}; \quad K_a \simeq \frac{R_f}{6 + R_i}$$

where all resistors are in kilo-ohms.

Thus, overall scale factor K can be adjusted by varying R_X, R_Y, R_f. For fine adjustment of the scale factor, K, an additional potentiometer can be included into the circuit, as shown in Figure 14.

INPUT DYNAMIC RANGE: The maximum peak signal which can be applied to the X or Y inputs for a given supply voltage without impairing linearity. (See Figure 10).

MULTIPLIER BANDWIDTH: Depending on the particular application, a different definition of "multiplier bandwidth" may be used. The most commonly accepted definitions are:

a) *3-dB Bandwidth*: Frequency where the multiplier output is 3-dB below its low frequency (f = 20 Hz) level.

b) *3° Phase Shift Bandwidth*: Frequency where the net phase shift across the multiplier is equal to 3°.

c) *1% Absolute Error Bandwidth*: Frequency where the phase vector error between the actual and ideal output vectors is equal to 1%. This frequency is reached when the net phase shift across the multiplier is equal to 0.01 radian or 0.57°.

d) *Transconductance Bandwidth*: Frequency where the transconductance of the multiplier drops 3-dB below its low frequency value. This bandwidth defines the frequency range of operation for phase-detector and synchronous AM detector applications.

DESCRIPTION OF CIRCUIT CONTROLS

MULTIPLIER INPUTS (PINS 2, 3, 4 AND 5): These four terminals provide the differential inputs to the X- and Y-sections of the multiplier, respectively. The output will be a linear product of the two voltages, V_X and V_Y, applied differentially across pins (2,3) and (4,5). Typical input bias current at the multiplier inputs is approximately 3 μA, for each of the four inputs. In circuit applications requiring single-ended, rather than differential, input signals, pins 3 and 4 can be shorted together and connected to a common bias point.

MULTIPLIER OUTPUTS (PINS 1 AND 16): The differential output voltage, V_O, across these terminals is proportional to the linear product of voltages V_X and V_Y applied to the inputs. V_O can be expressed as:

$$V_O \approx \left(\frac{25}{R_X R_Y}\right)(V_X V_Y)$$

where all voltages are in volts and the resistors are in kΩ. R_X and R_Y are the gain control resistors for X and Y sections of the multiplier.

The common-mode dc potential at the multiplier outputs is approximately 3 volts below the positive supply.

In most analog computation operations, such as multiplication, division, etc., pins 1 and 16 are dc coupled to the op amp inputs (pins 13 and 14). The final output, V_Z, is then obtained from the op amp output at pin 11, as shown in Figures 14 and 15.

X AND Y GAIN ADJUST (PINS 6, 7, 8, 9): The gains of the X and Y sections of the multiplier are inversely proportional to resistors R_X and R_Y connected across the respective gain terminals. The multiplier conversion gain, K_m, can be expressed as:

$$K_m \cong \frac{25}{R_X R_Y}\ (\text{volts})^{-1}$$

where R_X and R_Y are in kΩ.

X AND Y OFFSET ADJUST (PINS 7 AND 8): Two of the gain-control terminals, pins 7 and 8, are also used for adjusting X and Y offsets. Figure 13 shows the typical adjustment circuitry which can be connected to these pins to null-out input offsets.

OP AMP INPUTS (PINS 13 AND 14): Pin 13 is the noninverting and pin 14 the inverting inputs for the op amp section. In most multiplier applications, these terminals are connected to the multiplier outputs (pins 1 and 16). **Note: When the op amp section is not used, these terminals should be grounded.**

OP AMP COMPENSATION (PIN 12): The op amp section can be compensated for unconditional stability with a 20 pF capacitor connected between pin 12 and pin 11. For op amp voltage gains greater than unity, this compensation capacitance can be reduced to improve slew rate and small signal bandwidth as shown in Figure 12.

OP AMP OUTPUT (PIN 11): This terminal serves as the output for the op amp section. It is internally protected against accidental short circuit conditions, and can sink or source 10 mA of current into a resistive load. In most multiplier applications, pin 11 is the actual XR-2228 output, with the op amp inputs being connected to the multiplier outputs.

APPLICATIONS INFORMATION

PART I: ARITHMETIC OPERATIONS

MULTIPLICATION

For most multiplication applications, the multiplier and op amp sections are interconnected as shown in Figure 14 to provide a single-ended analog output with a wide dynamic range. The circuit of Figure 14 provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K = 0.1. The trimming procedure for the circuit is as follows:

1. Apply 0V to both inputs and adjust the output offset to 0V using the output offset control.

2. Apply 20V p-p at 50 Hz to the X-input and 0V to the Y-input. Trim the Y-offset adjust for minimum peak-to-peak output.

3. Apply 20V p-p to the Y-input and 0V to the X-input. Trim X-offset adjust for minimum peak-to-peak output.

4. Repeat step 1.

5. Apply +10V to both inputs and adjust scale factor for V_O = +10V. This step may be repeated with different amplitudes and polarities of input voltages to optimize accuracy over the entire range of input voltages, or over any specific portion of input voltage range.

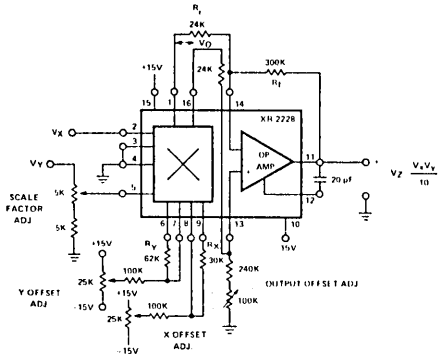


Figure 14. Multiplication Circuit

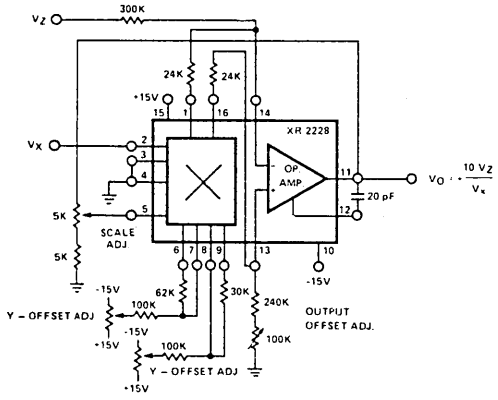


Figure 15. Dividing Circuit

DIVIDING CIRCUIT

Recommended circuit connection for performing analog division is shown in Figure 15. This circuit uses the multiplier in the feedback path of the op amp. For the circuit shown, $V_O = +10\ V_Z/V_X$ where $V_X < 0$ and V_Z can have either sign. Positive values of V_X are not allowed, since this will reverse the polarity of the feedback loop, causing positive feedback and latchup.

This latchup mode is nondestructive to the XR-2228, and is common to all analog division circuits. The divider circuit is trimmed as follows:

1. Apply V_Z = 0 and trim the output offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

2. Keeping V_Z = 0, and applying V_X = −10V, time the Y-offset adjust until V_O = 0.

3. Let $V_Z = V_X$ and/or $V_Z = -V_X$ and trim the X-offset adjustment for constant output voltage as V_X is varied from −1V to −10V.

4. If step 3 requires a large initial adjustment, repeat steps 1, 2 and 3.

5. Keeping $V_Z = V_X$, adjust the scale factor trim for V_O = −10V as V_X is varied from −1V to −10V.

PART II: ANALOG SIGNAL PROCESSING

PHASE DETECTION

The multiplier section of the XR-2228 can be used as a linear phase-discriminator. A recommended circuit connection for this application is shown in Figure 16. In this case, the reference input (input 1) is applied to pin 2, and the input signal whose phase is to be detected (input 2) is applied to pin 5. For input signal amplitudes ≥50 mV rms, the differential output voltage, V_O across pins 1 and 16 is directly proportional to the phase difference, ϕ, between the two input signals. It can be expressed as

$$V_O(\phi) = 5\left(\frac{2\phi}{\pi} - 1\right)$$

Where ϕ is the phase difference expressed in radians.

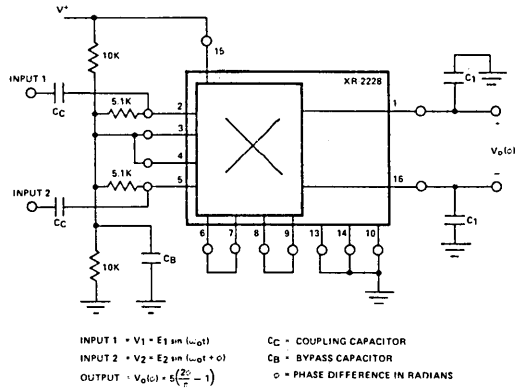


Figure 16. Phase-Detector Circuit

The capacitors C_1 at pins 1 and 16 provide a low-pass filter with a time constant $T_1 = R_1 C_1$, where $R_1 = 5$ kΩ is the international impedance level at these pins.

If needed, the phase conversion gain can be increased by using the op amp section of the XR-2228 to further amplify the output voltage, $V_O(\phi)$. The XR-2228 is suitable for phase detection of input frequencies up to 100 MHz.

SYNCHRONOUS AM DETECTION

Figure 17 is a typical circuit connection for synchronous AM detection for carrier frequencies up to 100 MHz. The AM input signal is applied to the multiplier X- and Y-input terminals (pins 3 and 4) simultaneously.

The Y-gain terminals (pins 6 and 7) are shorted, and this section of the multiplier serves as a "limiter" for input signals ≥50 mVrms; the X-section of the multiplier operates in its linear mode. The low-pass filter capacitors, C_1, and at pins 1 and 16 are used to filter the carrier feedthrough. If desired, the op amp section can be used as an audio preamplifier to increase the demodulated output amplitude.

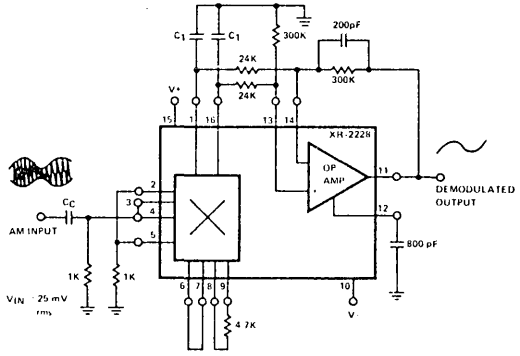


Figure 17. Synchronous AM Detector

PRECISION PHASE-LOCKED LOOP DESIGN

A precision phase-locked loop may be constructed using an XR-2209 voltage controlled oscillator and an XR-2228. (See Figure 18.) Due to the excellent temperature stability and wide sweep range of the XR-2209 this PLL circuit exhibits especially good stability of center frequency and wide lock range. In this application the XR-2228 serves as a phase comparator and level shifter. Resistor R_L adjusts the loop gain of the PLL, thus varying the lock range. Tracking range may be varied from about 1.5:1 up to 12:1. For large values of R_L, temperature stability of center frequency is better than 30 ppm/°C.

TRIANGLE-TO-SINEWAVE CONVERSION

A triangular input can be converted into a low distortion (THD < 1%) sinusoidal output with the XR-2228. A recommended connection for this application is shown in Figure 19. The triangle input signal is applied to the X-input (pin 2). The multiplier section rounds off the peaks of this input and converts it to a low distortion sine wave.

For the component values shown in Figure 19, the recommended input signal level at pin 2 is ≅300 mV pp, in order to obtain a 2V pp signal at pins 1 or 16, with R_X set at approximately 100Ω. The dc level at pin 5 can be used for adjusting the output amplitude, or providing amplitude modulation. The sensitivity of the output amplitude to the dc voltage level at pin 5 is inversely proportional to the external resistor across pins 6 and 7.

If higher amplitude output signal is required, the op amp section of XR-2228 can be used to provide additional amplification.

PHASE-LOCKED AM DETECTION

The XR-2228 can be used in conjunction with any one of the commercially available monolithic phase-locked loop (PLL) IC's to provide phase-locked AM detection. In this manner, frequency-selective detection capabilities of PLL circuits can be extended to AM signals.

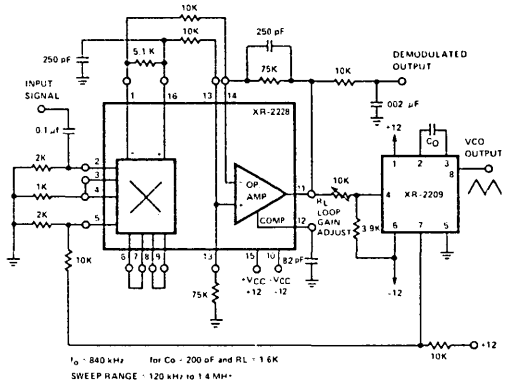


Figure 18. Precision PLL

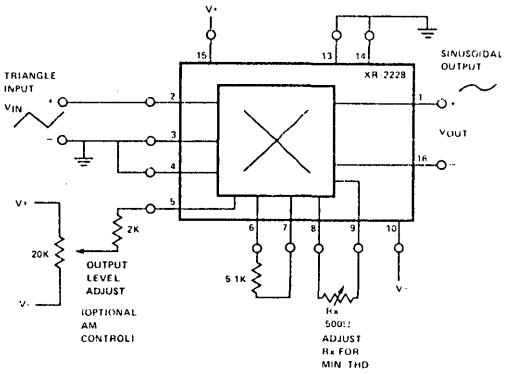


Figure 19. Triangle-to-Sinewave Converter

Figure 20 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit is useful as a phase-locked AM detector for carrier frequencies up to 20 MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate "quadrature" output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (pins 13 and 14) of XR-215. The Y-input of the XR-2228 is operated with maximum gain, since the Y-gain control terminals (pins 6 and 7) are shorted together. This causes the triangular waveform across the timing capacitor, C_0, to be converted to an effective "quadrature" drive.

The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X-inputs of the XR-2228, are biased at approximated one-half of V_{CC}, by means of an external resistive divider.

In Figure 20, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier.

The Y-input of the XR-2228 is operated in its switching mode, with the Y-gain terminals (pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; the output of the multiplier, at pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal. In the circuit, R_X sets the amplifier demodulation gain, C_3 serves as the low-pass post-detection filter.

A detailed description of the circuit operation, and the design equations for calculating the external component values are given in Exar's Application Note AN-13, entitled "Frequency Selective AM Detection using Monolithic Phase-Locked Loops."

PHASE-LOCKED LOOP TONE DETECTION

The XR-2228 multiplier/detector can be used in conjunction with the XR-210 or the XR-215 high-frequency PLL circuits, to provide high-frequency tone or carrier-detect systems. The generalized circuit connection for such an application is given in Figure 21. The circuit, as shown, can operate with a single power supply, from 10V, to 20V, or with split supplies in the range of ±5V to ±10V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 21 to ground.

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used and to the X-input terminal (pin 2) of the XR-2228.

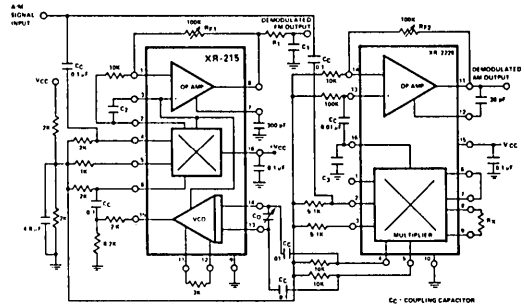


Figure 20. Phase-Locked AM Detection Using XR-215 Monolithic PLL and XR-2228 Multiplier/Detector

The Y-inputs (pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at pins 13 and 14 of the PLL IC) which is AC coupled to pins 4 and 5 of the XR-2228 multiplier input. the differential DC voltage level at the multiplier output terminals (pins 1 and 16) is offset by means of an external resistor, R_A. This initial offset causes the op amp output of the XR-2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 21, the op amp output (pin 11) would be at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (i.e., near $+V_{CC}$) when the PLL circuit is "locked" on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

The filter capacitor, C_A, connected across pins 1 and 16 of the multiplier outputs, serves as the post-detection low-pass filter. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

A detailed description of the principle of operation of the circuit of Figure 21 is given in Exar's Application Note AN-12 entitled: "Designing High Frequency Phase-Locked Loop Carrier-Detector Circuits".

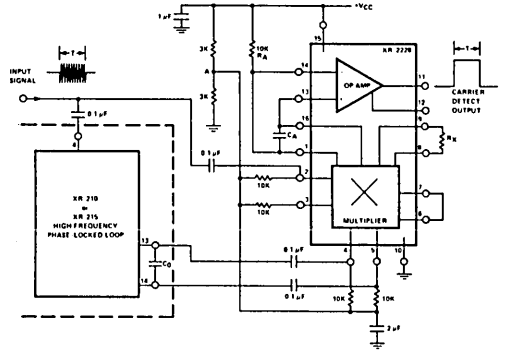


Figure 21. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone or Carrier-Detector Application

Section 6 – Instrumentation Circuits

Fundamentals of Phase-Locked Loops

The phase locked loop provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 1, the PLL in its most basic form is a feedback system comprised of three basic functional blocks: a phase comparator, low-pass filter and voltage controlled oscillator (VCO).

The basic principle of operation of a PLL can briefly be explained as follows: With no input signal applied to the system, the error voltage V_d is equal to zero. The VCO operates at a set frequency, f_o, which is known as the free-running frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to synchronize, or lock, with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

Two key parameters of a PLL system are its lock and capture ranges. They can be defined as follows:

Lock range: The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the tracking or holding range. Lock range increases as the over-all gain of the PLL is increased.

Capture range: The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It decreases as the filter bandwidth is reduced.

The lock and the capture ranges of a PLL can be illustrated with reference to Figure 2, which shows the typical frequency-to-voltage characteristics of a PLL. In the figure, the input is assumed to be swept slowly over a broad frequency range. The vertical scale corresponds to the loop error voltage.

In the upper part of Figure 2, the loop frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency f_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input, causing a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of the VCO voltage-to-frequency conversion gain, and goes through zero as $f_s = f_o$. The loop tracks the input until the input frequency reaches f_2, corresponding to the upper edge of the lock range. The PLL then loses lock, and the error voltage drops to zero.

If the input frequency is now swept slowly back, the cycle repeats itself as shown in the lower part of Figure 2. The loop recaptures the signal at f_3 and traces it down to f_4. The frequency spread between (f_1, f_3) and (f_2, f_4) corresponds to the total capture and lock ranges of the system; that is, $f_3 - f_1$ = capture range and $f_2 - f_4$ = lock range. The PLL responds only to those input signals sufficiently close to the VCO frequency, f_o, to fall within the "lock" or "capture" range of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about f_o.

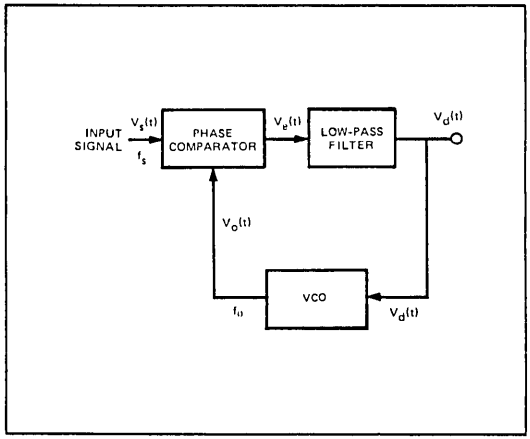


Figure 1. The basic phase locked loop consists of three functional blocks: a phase comparator, a low pass filter and a voltage-controlled oscillator.

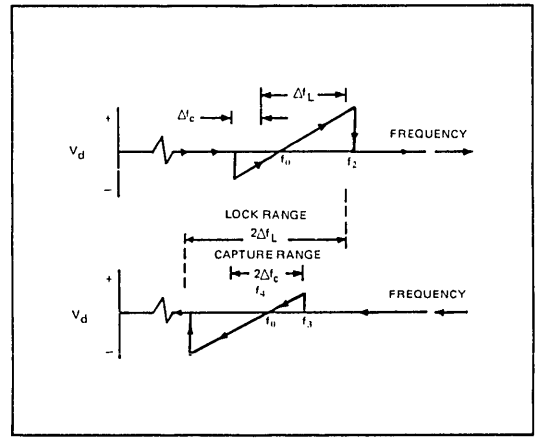


Figure 2. Typical PLL frequency-to-voltage transfer characteristics are shown for increasing (upper diagram) and decreasing (lower diagram) input frequency.

Applications of PLL IC's

The basic concept of the phase locked loop (PLL) has been around since the early 1930's and has been used for a variety of applications in instrumentation and space telemetry. However, before the advent of monolithic integration, cost and complexity considerations limited its use to precision measurements requiring very narrow bandwidths. In the past few years, the advantages of monolithic integration have changed the phase locked loop from a specialized design technique to a general-purpose building block. Therefore, what is "new" at this point is not the concept of the PLL, but its availability in a low-cost self contained monolithic IC package.

In many ways, this is similar to the case of the monolithic operational amplifier, which, until less than a decade ago, was an expensive building block. Today, with the advent of monolithic technology, it has become a basic building block in nearly every system design. The monolithic phase locked loop also offers a similar potential. In fact, many of the applications of the PLL outlined in this article become economically feasible *only* because the PLL is now available as a low-cost IC building block.

Today, over a dozen different integrated PLL products are available from a number of IC manufacturers. Some of these are designed as "general-purpose" circuits, suitable for a multitude of uses; others are intended or optimized for special applications such as tone detection, stereo decoding and frequency synthesis. This article is intended as a brief survey of the expanding field of monolithic phase locked loops. Its purpose is to familiarize the reader with their individual characteristics, capabilities and applications.

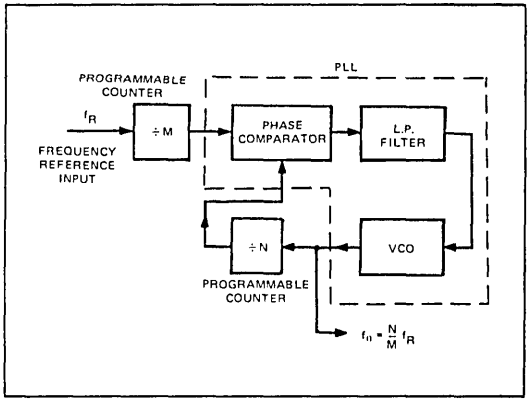


Figure 3. A frequency multiplier/divider can be constructed using a phase locked loop.

Applications for PLLs Abound

As a versatile building block, the PLL covers a wide range of applications. Some of the more important are the following:

FM demodulation: In this application, the PLL is locked on the input FM signal, and the loop-error voltage, $V_d(t)$ in Figure 1 (see Box), which keeps the VCO in lock with the input signal, represents the demodulated output. Since the system responds only to input signals within the capture range of the PLL, it also provides a high degree of frequency selectivity. In most applications the quality of the demodulated output (i.e., its linearity and signal/noise ratio) obtained from a PLL is superior to that of a conventional discriminator.

FSK demodulation: Frequency-shift keyed (FSK) signals are commonly used to transmit digital information over telephone lines. In this type of modulation, the carrier signal is shifted between two discrete frequencies to encode the binary data. When the PLL is locked on the input signal, tracking the shifts in the input frequency, the error voltage in the loop, $V_d(t)$, converts the frequency shifts back to binary logic pulses.

Signal conditioning: When the PLL is locked on a noisy input signal, the VCO output duplicates the frequency of the desired input but greatly attenuates the noise, undesired sidebands and interference present at the input. It is also a tracking filter since it can track a slowly varying input frequency.

Frequency synthesis: The PLL can be used to generate new frequencies from a stable reference source by either frequency multiplication and division, or by frequency translation. Figure 3 shows a typical frequency multiplication and division circuit, using a PLL and two programmable counters. In this application, one of the counters is inserted between the VCO and phase comparator and effectively divides the VCO frequency by

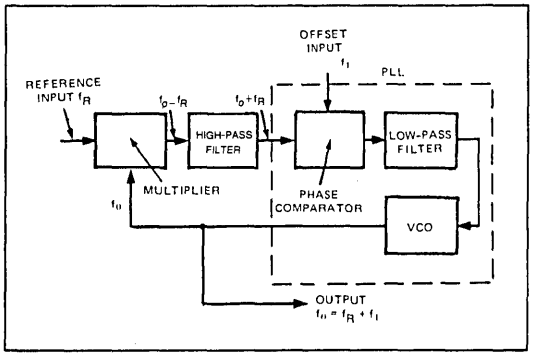


Figure 4. Frequency translation can be accomplished with a phase locked loop by adding a multiplier and an additional low-pass filter to the basic PLL.

the counter's modulus N. When the system is in lock, the VCO output is related to the reference frequency, f_R, by the counter moduli M and N as:

$$f_O = \left(\frac{N}{M}\right) f_R$$

By adding a multiplier and an additional low-pass filter to a PLL (Figure 4), one can form a frequency translation loop. In this application, the VCO output is shifted from the reference frequency, f_R, by an amount equal to the offset frequency, f_1, i.e., $f_O = (f_R + f_1)$.

Data synchronization: The PLL can be used to extract synchronization from a composite signal, or can be used to synchronize two data streams or system clocks to the same frequency reference. Such applications are useful in PCM data transmission, regenerative repeaters, CRT scanning and or drum memory read-write synchronization.

AM detection: The PLL can be converted to a synchronous AM detector with the addition of a non-critical phase-shift network, an analog multiplier and a low-pass filter. The system block diagram for this application is shown in Figure 5.

In this application, as the PLL tracks the carrier of the input signal, the VCO regenerates the unmodulated carrier and feeds it to the reference input of the multiplier section. In this manner, the system functions as a synchronous demodulator with the filtered output of the multiplier representing the demodulated audio information.

Tone detection: In this application, the PLL is again connected as shown in Figure 5. When a signal tone is present at the input, within a frequency band corresponding to the capture range of the PLL, the output dc voltage is shifted from its tone-absent level. This shift is easily converted to a logic signal by adding a threshold detector with logic-compatible output levels.

Motor speed control: Many electromechanical systems, such as magnetic tape drives and disc or drum head drivers, require precise speed control. This can be

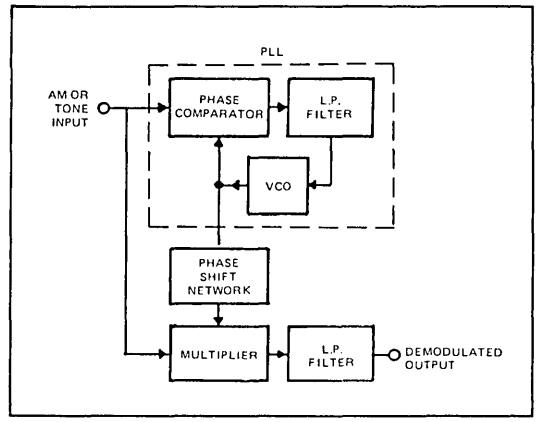


Figure 5. AM and tone detection are possible by adding three functional blocks to the basic phase locked loop.

achieved using a PLL system, as shown in Figure 6. The VCO section of the monolithic PLL is separated from the phase-comparator and used to generate a voltage controlled reference frequency, f_R. The motor shaft and the tachometer output provide the second signal, frequency f_M, which is compared to the reference frequency. The controller is a power amplifier which drives the speed-control windings of the motor. Thus, the motor and tachometer combination essentially functions as a VCO which is phase locked to the voltage controlled reference frequency, f_R.

Stereo decoding: In commercial FM broadcasting, suppressed carrier AM modulation is used to superimpose the stereo information on the FM signal. To demodulate the complex stereo signal, low-level pilot tone is transmitted at 19 kHz (1/2 of actual carrier frequency). The PLL can be used to lock onto this pilot tone, and regenerate a coherent 38 kHz carrier which is then used to demodulate the complete stereo signal. A number of highly specialized monolithic circuits have been developed for this application. A typical example of monolithic stereo decoder circuits using the PLL principle is the XR-1310 stereo demodulator IC.

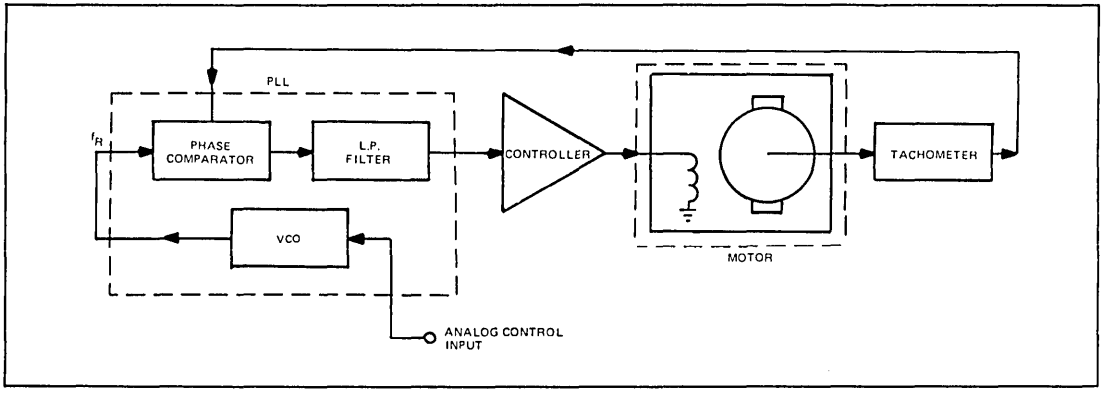


Figure 6. Very precise motor speed control is possible with a phase locked loop system of this type.

Choosing the Right PLL Circuit

At the onset of his design, the user of monolithic PLL products is faced with the key question of choosing the phase-locked loop IC best suited to his application. The broad line of PLL products offered by Exar cover a wide range of applications. It is often difficult to determine a a glance the best circuit for a given application. The purpose of this section is to review some of the key performance requirements, from an applications point of view, and help answer the question, "What is the best PLL product for the job?"

Table 2 gives a brief listing of some of the major classes of PLL applications, and lists the recommended circuits for each. A further discussion of the key performance parameters associated with each application are also listed below.

FM demodulation: Essentially all the PLL circuits listed in Table 1 can be used for FM demodulation. However, it is often possible to narrow the choice down to 2 or 3 circuits, based on the particular performance criteria. In general, there are three key performance parameters which should be examined:

- ☐ Quality of demodulated output: This is normally measured in terms of the output level, distortion, and signal/noise ratio for a given FM deviation.
- ☐ VCO frequency range and frequency stability: For reliable operation, VCO upper frequency limit (see Table 1) should be at least 20% above the FM carrier frequency. VCO frequency stability is important, especially if a narrow-band filter is used in front of the PLL, or multiple input channels are present. If the VCO exhibits excessive drift, the PLL can drift out of the input signal band as the ambient temperature varies.
- ☐ Detection threshold: This parameter determines minimum signal level necessary for the PLL to lock and demodulate an FM signal of given deviation.

In most FM demodulation applications, it is also desirable to control the amplitude of the demodulated output. This feature is provided in some of the PLL circuits (such as the XR-215 and the XR-2212) by means of a variable-gain amplifier contained on the chip.

For low-frequency FM detection (below 300 kHz carrier frequency) the XR-2212 is recommended because of its versatility and temperature stability. For FM demodulation at frequencies above 300 kHz, the XR-215 offers the best performance because of its high frequency capability.

FSK decoding: Frequency-shift keying used in digital communications is very similar to analog FM modulation. Therefore, any PLL IC can be used for FSK decoding, provided that its input sensitivity and the tracking range are sufficient for a given FSK signal deviation. Some of the basic requirements and desirable features for a PLL used in FSK decoding are:

- ☐ Center frequency stability.
- ☐ Logic compatible output.
- ☐ Control of VCO conversion gain.

Center frequency stability is essential to insure that the VCO frequency range stays within the signal band over the operating temperature range. A logic compatible output is desirable to avoid the need for an external voltage comparator (slicer) to square the output pulses. It is particularly convenient if the output conforms to RS-232C standard, thereby eliminating the need for a separate line-driver circuit. Control of the VCO's conversion gain allows the circuit to be used for both large deviation FSK signals (such as 1200 baud operation) as well as for small deviation (75 baud) FSK signals.

For FSK decoding at low frequencies (i.e., below 300 kHz) the XR-2211 is by far the optimum circuit to use because of its frequency stability and carrier-detect capability. For FSK detection at higher frequencies (up to 10 MHz) the XR-210 is the recommended circuit.

Frequency synthesis: This application requires a PLL circuit with the loop opened between the VCO output and the phase comparator input, so that an external frequency divider can be inserted into the feedback loop of the PLL. This requirement is satisfied by XR-S200, XR-210, XR-215 and the XR-2212 PLL circuits.

For frequency synthesis at low frequencies (i.e., with maximum output frequency less than 300 kHz) the XR-2212 is by far the best suited circuit since it has the best VCO stability and interfaces easily with all logic families. For operation above 300 kHz, either the XR-210 or the XR-215 PLL IC's can be used for frequency synthesis; however the XR-215 offers the highest frequency capability.

Signal conditioning: Most signal conditioning applications require very narrow-band operation of the PLL. This in turn may require the use of active filters within the loop (between the phase detector and the VCO). The PLL circuits which allow active filers to be inserted into the loop are the XR-S200 and the XR-2212. Both of these circuits already contain an op. amp. on the chip for active filtering. For low frequencies (i.e. below 300 kHz) the XR-2212 is the best suited circuit because of its adjustable tracking bandwidth and excellent frequency stability. For higher frequencies the XR-S200 is the recommended circuit.

Tone decoding: The PLL circuits especially designed for this application are the XR-567, the XR-L567, the XR-2567 and the XR-2211. The XR-2211 offers the highest frequency stability, and independent control of system bandwidth and response time, among the three circuits. The XR-567 has a relatively high input threshold (≈20 mV, rms) and may require input preamplification; however it requires fewer external components that the XR-2211. The XR-2567, which contains two independent 567-type tone decoders on the same chip may be more economical to use in multiple-tone detection systems.

FSK Modulator/Demodulator

GENERAL DESCRIPTION

The XR-210 is a highly versatile monolithic phase-locked loop system, especially designed for data communications. It is particularly well suited for FSK modulation/demodulation (MODEM) applications, frequency synthesis, tracking filters, and tone decoding. The XR-210 operates over a power supply range of 5V to 26V, and over a frequency band of 0.5 Hz to 20 MHz. The circuit can accommodate analog signals between 300 μV and 3V, and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range	0.5 Hz to 20 MHz
Wide Supply Voltage Range	5V to 26V
Digital Programming Capability	
RS-232C Compatible Demodulator Output	
DTL, TTL and ECL Logic Compatibility	
Wide Dynamic Range	300 μV to 3V
ON-OFF Keying & Sweep Capability	
Wide Tracking Range	$\pm$1% to $\pm$50%
Good Temperature Stability	200 ppm/°C
High-Current Logic Output	50 mA
Independent "Mark" and "Space" Frequency Adjustment	
VCO Duty Cycle Control	

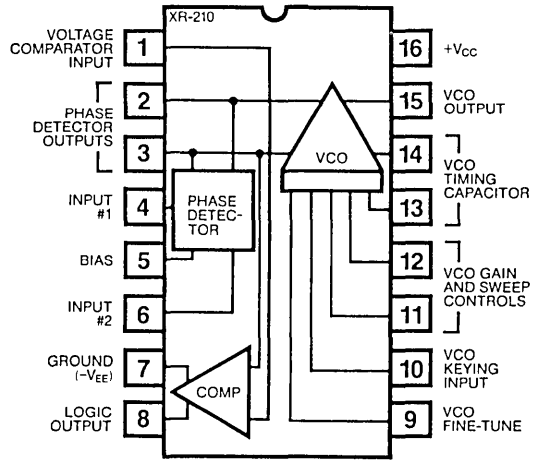
APPLICATIONS

Data Synchronization
Signal Conditioning
FSK Generation
Tone Decoding
Frequency Synthesis
FSK Demodulation
Tracking Filter
FM Detection
FM and Sweep Generation
Wideband Discrimination

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 Volts
Power Dissipation	750 mW
Derate Above +25°C	6.0 mW/°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-210M	Ceramic	−55°C to +125°C
XR-210CN	Ceramic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-210 is made up of a stable wide-range voltage-controlled oscillator (VCO), exclusive OR gate type phase detector, and an analog voltage comparator. The VCO, which produces a square wave as an output, is either used in conjunction with the phase detector to form a phase-locked loop (PLL) for FSK demodulation and tone detection or as a generator in FSK modulation schemes. The phase detector when used in the PLL configuration produces a differentional output voltage with a 6 KΩ output impedance, which when capacitively loaded forms a single pole loop filter. The voltage comparator is used to sense the phase detector output and produces the output in the FSK demodulation connection.

XR-210

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = 12V (single supply), T_A = +25°C, Test circuit of Figure 1 with C_0 = 0.02 μF, S_1, S_2, S_5 closed, S_3, S_4, S_6, S_7 open, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
GENERAL CHARACTERISTICS						
V_{CC}	Supply Voltage					
	Single Supply	5		26	V dc	See Figure 1
	Split Supply	±2.5		±13	V dc	See Figure 2
I_{CC}	Supply Current	9	12	16	mA	See Figure 1, S_2 open
f_{UL}	Upper Frequency Limit	15	20		MHz	See Figure 1, S_1 open, S_4 closed
f_{LL}	Lowest Practical Operating Frequency		0.5		Hz	C_O = 500 μF
VCO SECTION						
	Stability					
T_C	Temperature		200	500	ppm/°C	f = 10 kHz, $V^+ \geq$ 10V, 0 < T_A < 75°C
PSR	Power Supply		0.05	0.5	%/V	10V < V^+ < 24V
f_{SW}	Sweep Range	5:1	8:1			S_3 closed, S_4 open, 0 < V_S < 6V See Figure 5, V^+ = 12V
V_O	Output Voltage Swing	1.5	2.5		V p-p	S_5 open
DC	Duty Cycle Asymmetry		±1	±3	%	S_5 open
T_R	Rise Time		20		ns	10 pF to ground at Pin 15, S_5 open
T_F	Fall Time		40		ns	10 pF to ground at Pin 15, S_5 open
PHASE DETECTOR SECTION						
K_D	Conversion Gain		2		V/rad	V_{in} > 50 mV rms, see Figure 8
Z_O	Output Impedance		6		kΩ	Measured looking into Pin 2 or 3
V_{OOS}	Output Offset Voltage		35	150	mV	Measured across Pin 1 and 3, V_{in} = 0, S_5 open
VOLTAGE COMPARATOR SECTION						
A_{VOL}	Open Loop Voltage Gain	66	80		dB	f = 20 Hz
Z_{IN}	Input Impedance	0.5	2		MΩ	Measured looking into Pin 1
V_{OS}	Input Offset Voltage		1		mV	
I_B	Input Bias Current		80		nA	
CMRR	Common Mode Rejection		90		dB	
LOGIC OUTPUT SECTION						
SR	Slew Rate		15		V/μsec	R_L = 3 kΩ, C_L = 10 pF, S_2 closed
I_{OL}	"1" Output Leakage Current		0.02	10	μA	V_O = +24V
V_{OL}	"0" Output Voltage		0.2	0.4	V	I_L = 10 mA
I_{SINK}	Current Sink Capability	30	50		mA	$V_O \leq$ 1V

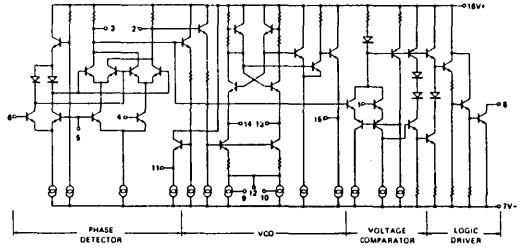
PRINCIPLES OF OPERATION

Description of Controls

Phase-Detector Inputs (Pin 4 and 6):
One input to the phase detector is used as the signal input; the remaining input should be ac coupled to the VCO output (Pin 15), to complete the PLL (see Figure 1). For split supply operation, these inputs are biased from ground as shown in Figure 2.

Phase-Detector Bias (Pin 5):
This terminal should be dc biased as shown in Figures 1 and 2, and ac grounded with a bypass capacitor. The

EQUIVALENT SCHEMATIC DIAGRAM



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bias resistor in series with this pin should be half as large as those in series with Pin 4 and 6.

Phase-Detector Outputs (Pin 2 and 3):
The low-frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase-detector inputs (Pin 4 and 6). These differential phase-detector outputs are internally connected to the VCO control terminals. Pin 3 is also internally connected to the reference input of the voltage comparator section.

In normal use, the low-pass loop-filter capacitor, C_1, is connected between Pin 2 and 3. The 6 kΩ impedances of the two outputs add to 12 kΩ in the single-pole RC low-pass loop filter. Pin 2 is externally connected to the voltage comparator input (Pin 1) through an RC low-pass filter.

Frequency-Keying Input (Pin 10):
The VCO frequency can be varied between two discrete frequencies, f_1 and f_2, by connecting an external resistor, R_X, to this terminal. Referring to Figure 6, the VCO frequency is proportional to the sum of currents, I_1 and I_2, through the transistors, T_1 and T_2, on the monolithic chip. These transistors are biased from a fixed internal reference. The current, I_1, is set internally, and is partially controllable by the fine-tune adjustment, R_T. The current, I_2, is set by the external resistor, R_X, connected between Pin 10 and Pin 7. For any C_O setting, the VCO frequency, f_2, with R_X connected to Pin 10, can be expressed as:

$$f_2 = f_1 \left(1 + \frac{0.3}{R_X}\right) \text{ Hz}$$

where f_1 is the frequency with Pin 10 open-circuited, and R_X is in kΩ. Note that f_2 can be fine-tuned to a desired value by the proper choice of R_X.

VCO Sweep Input (Pin 12):
The VCO frequency can be swept over a broad range by applying an analog sweep voltage, V_S to Pin 12 (see Figure 5). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 5. The VCO temperature dependence is minimal when the sweep input is not used, and should be left open-circuited.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5 mA or less, under all operating conditions.

VCO Conversion Gain (Pin 11):
The VCO voltage-to-frequency conversion gain, K_O, is inversely proportional to the value of the external gain-control resistor, R_O, connected across Pin 11 and 12.

Fine Tune Control (Pin 9):
For a given choice of timing capacitor, C_O, the VCO frequency can be further fine-adjusted to a desired frequency, f_1, by means of a trimmer resistor, R_T, connected from Pin 9 to Pin 7, as shown in Figure 6. The fine tuned VCO frequency, f_1, is related to R_T as:

$$f_1 \approx \frac{220}{C_0}\left(1 + \frac{0.1}{R_T}\right) \text{ Hz}$$

where C_O is in μF, and R_T is in kΩ.

VCO Timing Capacitor (Pin 13 and 14):
The VCO free-running frequency, f_0, is inversely proportional to the timing capacitor, C_O, connected between Pin 13 and 14. With Pin 9 and 10 open-circuited, the VCO frequency is related to C_O as:

$$f_0 \approx \frac{220}{C_0} \text{ Hz}$$

where C_O is in μF.

VCO Output (Pin 15):
The VCO produces approximately a 2.5V p-p square wave output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to Pin 7 through a 10 kΩ resistor to increase the output current drive capability. For high-voltage operation (V_{CC} > 20V), a 20 kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output, for short-circuit protection.

Using the frequency-keying control, the VCO frequency can also be stepped in a binary manner by applying a logic signal to Pin 10, as shown in Figure 6. For high-level logic inputs, the transistor, T_2, is turned off, R_X is effectively switched out of the circuit, and the VCO frequency is shifted from f_2 to f_1.

Voltage Comparator Input (Pin 1):
This pin provides the signal input to the voltage comparator section. The comparator section is normally used for post-demodulation slicing and pulse shaping. Normally, Pin 1 is connected to Pin 2 through a 15K external resistor, as shown in Figures 1 and 2. The input impedance level at this pin is approximately 2 MΩ.

Logic Driver Output (Pin 8):
This pin provides a binary logic output corresponding to the polarity of the input signal, at the voltage comparator inputs. It is a bare-collector type stage with high-current sinking capability.

Definition of Terms

Phase-Detector Gain, K_d:
K_d is the output voltage from the phase detector per radian of phase difference at the phase-detector inputs (Pin 4 and 6). K_d is proportional to the input signal for low-level inputs (≤25 mV rms), and is constant at high-input levels (see Figure 8).

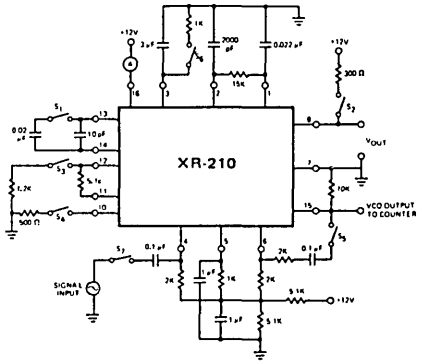


Figure 1. Test Circuits for Single Supply Operation

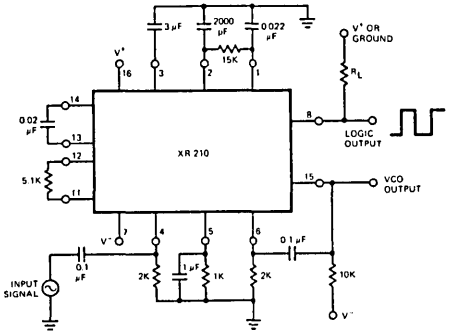


Figure 2. Test Circuit for Split Supply Operation

VCO Conversion Gain, K_O:

$$K_O \approx \frac{700}{C_O R_O} \quad \text{(radians/sec)/volt}$$

where C_O is in μF and R_O is in $k\Omega$. For most applications, recommended values for R_O range from 1 $k\Omega$ to 10 $k\Omega$.

When the XR-210 is connected as a PLL, its lock range can be controlled by varying the VCO gain control resistor, R_O, across Pin 11 and 12. For input signals greater than 30 mV rms, the PLL loop-gain is independent of signal amplitude, but is inversely proportional to R_O. Figure 7 shows the dependence of lock range, $\pm\Delta f_L$, on R_O.

Lock Range ($\Delta\omega_L$):
The range of frequencies in the vicinity of f_o over which the PLL can maintain lock with an input signal. If saturation or limiting does not occur, the lock range is equal to the loop gain; i.e., $\Delta\omega_L = K_T = K_d K_O$.

Capture Range ($\Delta\omega_C$):
The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the acquisition range. It is always smaller than the lock range, and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L \, |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C)|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

APPLICATIONS INFORMATION

FSK Demodulation

Figure 3 shows a generalized circuit connection for FSK demodulation. The circuit is connected as a PLL

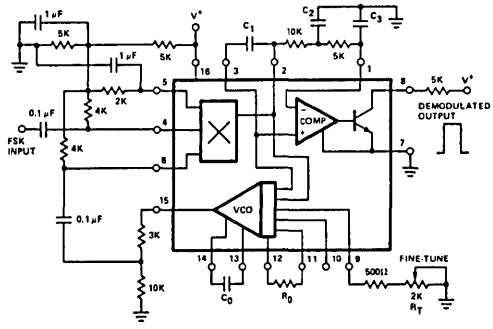


Figure 3. Circuit Connection for FSK Demodulation (Single Supply)

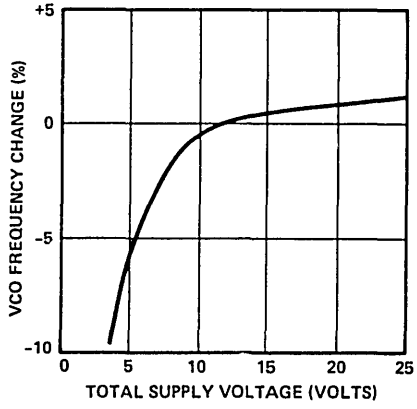
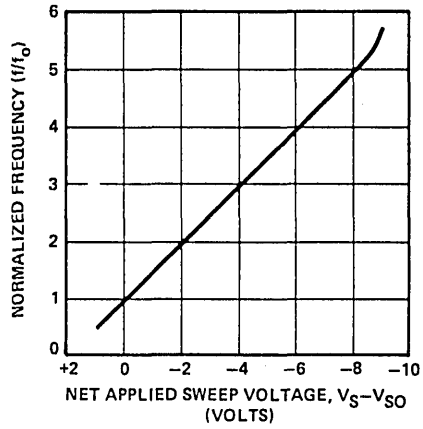
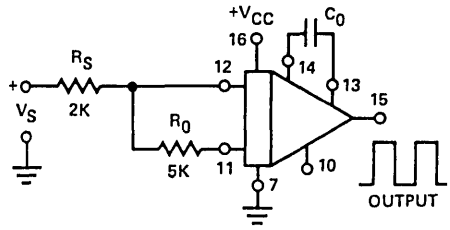


Figure 4. VCO Frequency Variation as a Function of Supply Voltage





(NOTE: $V_{SO} \approx V_{CC} - 5V$ = Open Circuit Voltage at pin 12)

Figure 5. Frequency Sweep Characteristics as a Function of Net Applied Sweep Voltage (Pin 10 Open)

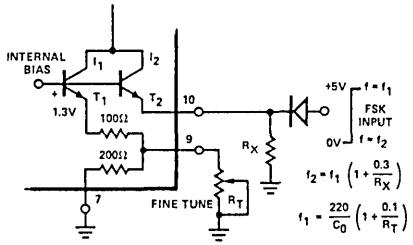


Figure 6. VCO Fine-Tune (Pin 9) and Frequency-Keying (Pin 10) Controls

system, by ac coupling the VCO output (Pin 15) to Pin 6. The FSK input is applied to Pin 4. When the input frequency is shifted, corresponding to a data bit, the polarity of the dc voltage across the phase-detector outputs (Pin 2 and 3) is reversed. The voltage comparator and the logic driver section convert this dc level shift to a binary pulse. The capacitor, C_1, serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. The timing capacitor, C_0, and fine-tune adjustments are used to set the VCO frequency, f_o, midway between the mark

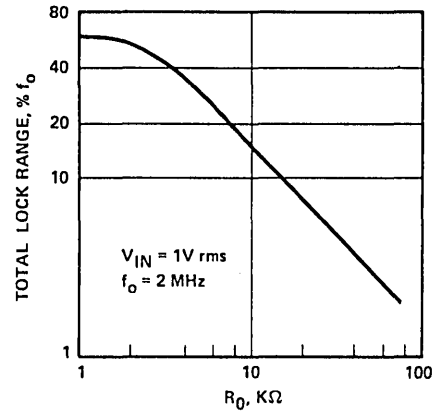


Figure 7. Total Lock Range, $\pm \Delta f_L$, versus VCO Gain Control Resistor, R_0

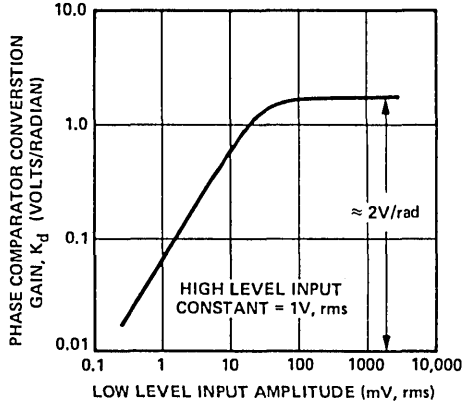


Figure 8. Phase Detector Conversion Gain, K_d, versus Input Amplitude

and space frequencies of the input signal. Typical component values for 300 baud (103-type) and 1200 baud (202-type) MODEM applications are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070 Hz	R_0 = 5.1 kΩ, C_0 = 0.22 μF
f_2 = 1270 Hz	$C_1 = C_2$ = 0.047 μF, C_3 = 0.033 μF
High Band: f_1 = 2025 Hz	R_0 = 8.2 kΩ, C_0 = 0.1 μF
f_2 = 2225 Hz	$C_1 = C_2 = C_3$ = 0.033 μF
1200 Baud	
f_1 = 1200 Hz	C_1 = 0.033 μF, C_3 = 0.02 μF
f_2 = 2200 Hz	C_2 = 0.01 μF

Monolithic Phase-Locked Loop

The XR-215 is a highly versatile monolithic phase-locked loop (PLL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM or FSK demodulation, frequency synthesis and tracking filter applications. The XR-215 can operate over a large choice of power supply voltages ranging from 5 V to 26 V and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL, and ECL logic families.

FEATURES

Wide Frequency Range: 0.5 Hz to 35 MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
DTL, TTL and ECL Logic Compatibility
Wide Dynamic Range: 300 μV to 3V
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from $\pm 1\%$ to $\pm 50\%$
High-Quality FM Detection: Distortion 0.15%
Signal/Noise 65dB

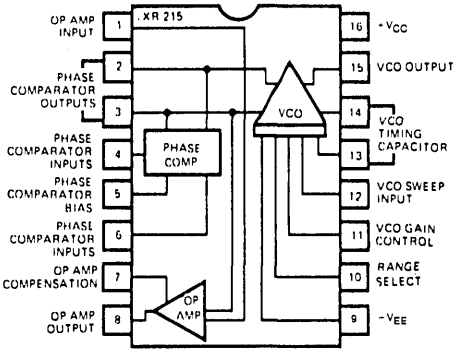
APPLICATIONS

FM Demodulation
Frequency Synthesis
FSK Coding/Decoding (MODEM)
Tracking Filters
Signal Conditioning
Tone Decoding
Data Synchronization
Telemetry Coding/Decoding
FM, FSK and Sweep Generation
Crystal Controlled Detection
Wideband Frequency Discrimination
Voltage-to-Frequency Conversion

ABSOLUTE MAXIMUM RATINGS

Power Supply	26 volts
Power Dissipation	750 mW
Derate above +25°C	5 mW/°C
Temperature	
Storage	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-215CN	Ceramic	0°C to 70°C

SYSTEM DESCRIPTION

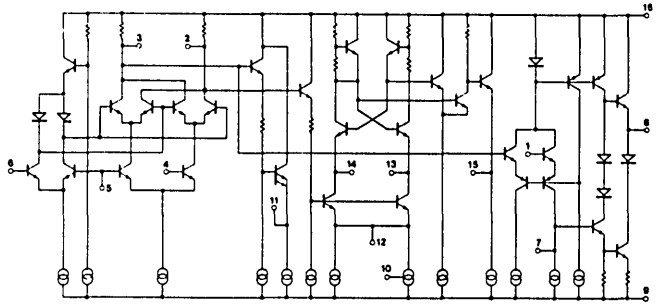
The XR-215 monolithic PLL system consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and a high speed operation amplifier. Figure 1 depicts the functional block diagram of the circuit. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self-contained PLL System is formed by simple AC coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals.

The VCO section has frequency sweep, on-off keying, sync, and digital programming capabilities. Its frequency is highly stable and is determined by a single exernal capacitor. The operational amplifier can be used to for audio preamplification in FM detector applications or as a high speed sense amplifier (or comparator) in FSK demodulation.

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = 12V (single supply), T_A = 25°C, Test Circuit of Figure 2 with C_0 = 100 pF, (silver-mica) S_1, S_2, S_5, closed, S_3, S_4 open unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I—GENERAL CHARACTERISTICS					
SUPPLY VOLTAGE					
Single Supply	5		26	V dc	See Figure 2
Split Supply	±2.5		±13	V dc	See Figure 3
Supply Current	8	11	15	mA	See Figure 2
Upper Frequency Limit	20	35		MHz	See Figure 2, S_1 open, S_4 closed
Lowest Practical Operating Frequency		0.5		Hz	C_0 = 500 µF
VCO SECTION:					
Stability:					
Temperature		250	600	ppm/°C	See Figure 2, 0°C ≤ T_A ≤ 75°C
Power Supply		0.1		%/V	V^+ > 10V
Sweep Range	5:1	8:1			S_3 closed, S_4 open, $0 < V_S < 6V$
					See Figure 9, C_0 = 2000 pF
Output Voltage Swing	1.5	2.5		V_{p-p}	S_5 open
Rise Time		20		ns	
Fall Time		20		ns	10 pF to ground at Pin 15
PHASE COMPARATOR SECTION:					
Conversion Gain		2		V/rad	V_{in} > 50 mV rms (See characteristic curves)
Output Impedance		6		kΩ	Measured looking into Pins 2 or 3
Output Offset Voltage		20	100	mV	Measured across Pins 2 and 3 V_{in} = 0, S_5 open
OP AMP SECTION:					
Open Loop Voltage Gain	66	80		dB	S_2 open
Slew Rate		2.5		V/µ sec	A_V = 1
Input Impedance	0.5	2		MΩ	
Output Impedance		2		kΩ	
Output Swing	7	10		V_{p-p}	R_L = 30 kΩ from Pin 8 to ground
Input Offset Voltage		1		mV	
Input Bias Current		80		nA	
Common Mode Rejection		90		dB	
II—SPECIAL APPLICATIONS					
A) FM Demodulation					
Test Conditions: Test circuit of Figure 4, V^+ = 12V, input signal = 10.7 MHz FM with Δf = 75 kHz, f_{mod} = 1 kHz.					
Detection Threshold		0.8	3	mV rms	50Ω source
Demodulated Output Amplitude	250	500		mV rms	Measured at Pin 8
Distortion (THD)		0.15	0.5	%	
AM Rejection		40		dB	V_{in} = 10 mV rms, 30% AM
Output Signal/Noise	55	65		dB	
B) Tracking Filter					
Test Conditions: Test circuit of Figure 5, V^+ = 12V, f_0 = 1 MHz, V_{in} = 100 mV rms, 50Ω source.					
Tracking Range (% of f_0)	±30	±50			See Figures 5 and 25
Discriminator Output $\frac{\Delta V_{out}}{\Delta f/f_0}$		50		mV/%	Adjustable — See applications information



EQUIVALENT SCHEMATIC DIAGRAM

DESCRIPTION OF CIRCUIT CONTROLS

PHASE COMPARATOR INPUTS (PINS 4 AND 6)

One input to the phase comparator is used as the signal input; the remaining input should be ac coupled to the VCO output (pin 15) to complete the PLL (see Figure 2). For split supply operation, these inputs are biased from ground as shown in Figure 3. For single supply operation, a resistive bias string similar to that shown in Figure 2 should be used to set the bias level at approximately $V_{CC}/2$. The dc bias current at these terminals is nominally 8 μA.

PHASE COMPARATOR BIAS (PIN 5)

This terminal should be dc biased as shown in Figures 2 and 3, and ac grounded with a bypass capacitor.

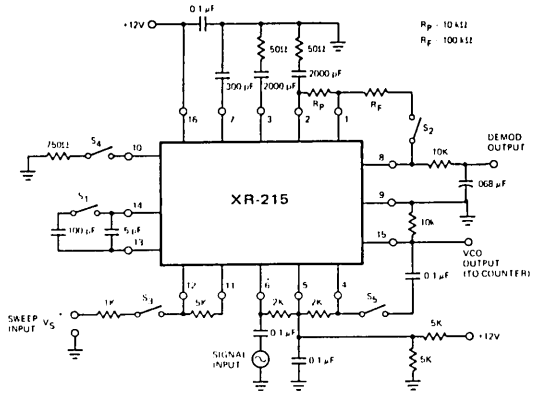


Figure 2. Test Circuit For Single Supply Operation

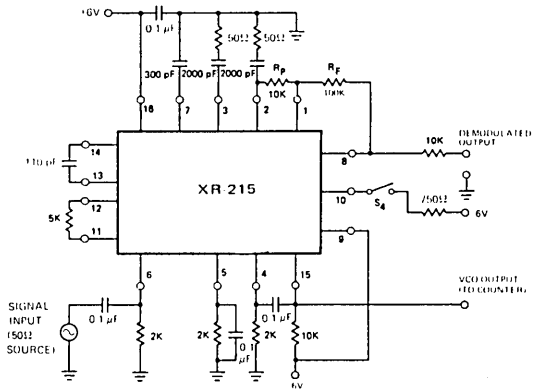


Figure 3. Test Circuit For Split-Supply Operation

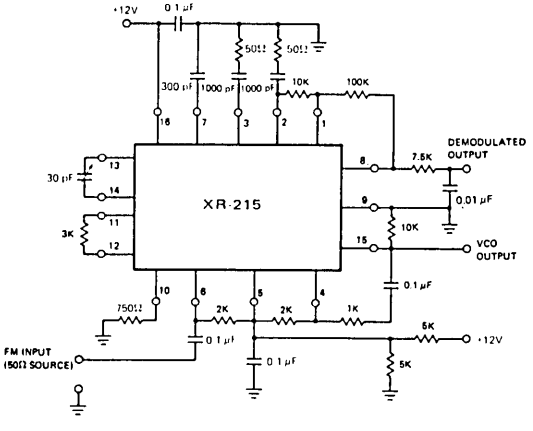


Figure 4. Test Circuit For FM Demodulation

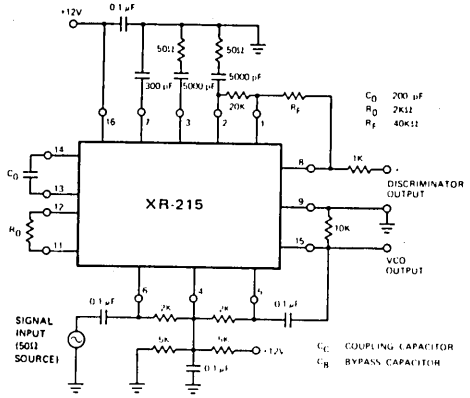


Figure 5. Test Circuit For Tracking Filter

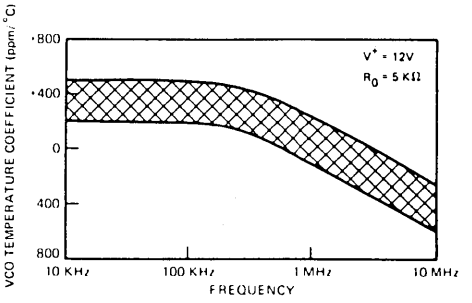


Figure 6. Typical VCO Temperature Coefficient Range as a Function of Operating Frequency (pin 10 open)

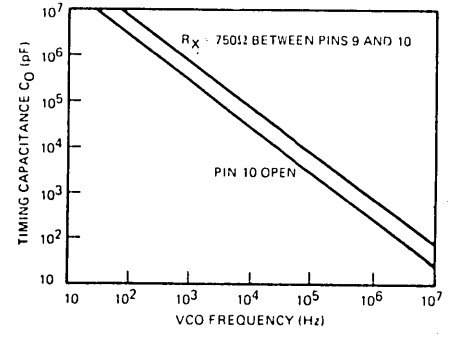


Figure 7. VCO Free Running Frequency vs Timing Capacitor

PHASE COMPARATOR OUTPUTS (PINS 2 AND 3)

The low frequency (or dc) voltage across these pins corresponds to the phase difference between the two signals at the phase comparator inputs (pins 4 and 6). The phase comparator outputs are internally connected to the VCO control terminals (see Figure 1). One of the outputs (pin 3) is internally connected to the *non-inverting* input of the operational amplifier. The low-pass filter is achieved by connecting an RC network to the phase comparator outputs as shown in Figure 14.

VCO TIMING CAPACITOR (PINS 13 AND 14)

The VCO free-running frequency, f_0, is inversely proportional to timing capacitor C_0 connected between pins 13 and 14. (See Figure 7).

VCO OUTPUT (PIN 15)

The VCO produces approximately a 2.5 V_{p-p} output signal at this pin. The dc output level is approximately 2 volts below V_{CC}. This pin should be connected to pin 9 through a 10 kΩ resistor to increase the output current drive capability. For high voltage operation (V_{CC} >

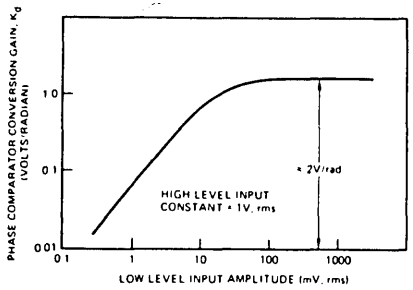


Figure 8. Phase Comparator Conversion Gain, K_d, versus Input Amplitude

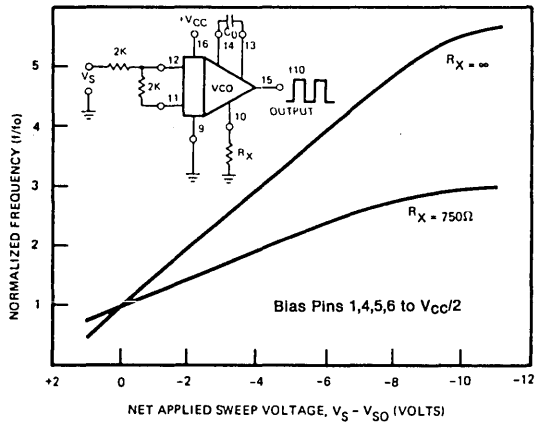


Figure 9. Typical Frequency Sweep Characteristics as a Function of Applied Sweep Voltage

(Note: $V_{SO} \approx V_{CC}$ - 5V = Open Circuit Voltage at pin 12)

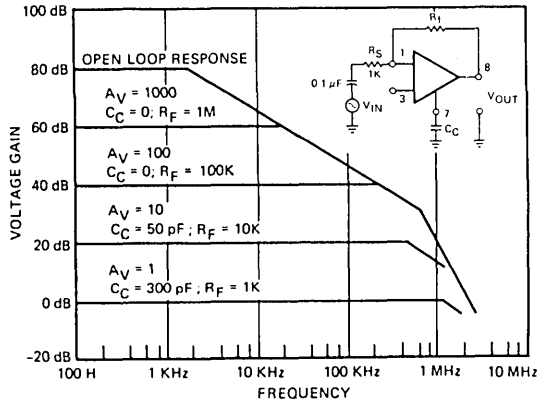


Figure 10. XR-215 Op Amp Frequency Response

20V), a 20 kΩ resistor is recommended. It is also advisable to connect a 500Ω resistor in series with this output for short circuit protection.

VCO SWEEP INPUT (PIN 12)

The VCO Frequency can be swept over a broad range by applying an analog sweep voltage, V_S, to pin 12 (see Figure 9). The impedance level looking into the sweep input is approximately 50Ω. Therefore, for sweep applications, a current limiting resistor, R_S, should be connected in series with this terminal. Typical sweep characteristics of the circuit are shown in Figure 9. The VCO temperature dependence is minimum when the sweep input is not used.

CAUTION: For safe operation of the circuit, the maximum current, I_S, drawn from the sweep terminal should be limited to 5 mA or less under all operating conditions.

ON-OFF KEYING: With pin 10 open circuited, the VCO can be keyed off by applying a positive voltage pulse to the sweep input terminal. With R_S = 2 kΩ, oscillations will stop if the applied potential at pin 12 is raised 3 volts above its open-circuit value. When sweep, sync, or on-off keying functions are not used, R_S should be left open circuited.

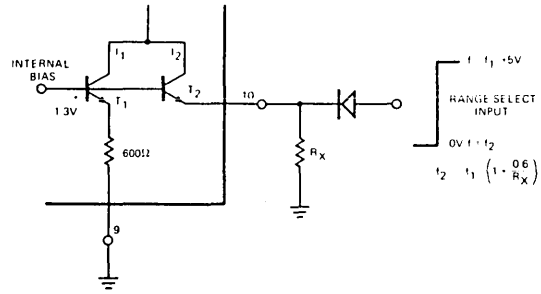


Figure 11. Explanation of VCO Range-Select Controls

RANGE-SELECT (PIN 10)

The frequency range of the XR-215 can be extended by connecting an external resistor, R_X, between pins 9 and 10. With reference to Figure 11, the operation of the range-select terminal can be explained as follows: The VCO frequency is proportional to the sum of currents I_1 and I_2 through transistors T_1 and T_2 on the monolithic chip. These transistors are biased from a fixed internal reference. The current I_1 is set internally, whereas I_2 is set by the external resistor R_X. Thus, at any C_0 setting, the VCO frequency can be expressed as:

$$f_o = f_1 \left(1 + \frac{0.6}{R_X}\right)$$

where f_1 is the frequency with pin 10 open circuited and R_X is in kΩ. External resistor R_X ($\approx$ 750Ω) is recommended for operation at frequencies in excess of 5 MHz.

The range select terminal can also be used for fine tuning the VCO frequency, by varying the value of R_X. Similarly, the VCO frequency can be changed in discrete steps by switching in different values of R_X between pins 9 and 10.

DIGITAL PROGRAMMING

Using the range select control, the VCO frequency can be stepped in a binary manner, by applying a logic signal to pin 10, as shown in Figure 11. For high level logic inputs, transistor T_2 is turned off, and R_X is effectively switched out of the circuit. Using the digital programming capability, the XR-215 can be time-multiplexed between two separate input frequencies, as shown in Figures 18 and 19.

AMPLIFIER INPUT (PIN 1)

This pin provides the inverting input for the operational amplifier section. Normally it is connected to pin 2 through a 10 kΩ external resistor (see Figure 2 or 3).

AMPLIFIER OUTPUT (PIN 8)

This pin is used as the output terminal for FM or FSK demodulation. The amplifier gain is determined by the external feedback resistor, R_F, connected between pins 1 and 8. Frequency response characteristics of the amplifier section are shown in Figure 10.

AMPLIFIER COMPENSATION (PIN 7)

The operational amplifier can be compensated by a single 300 pF capacitor from pin 7 to ground. (See Figure 10).

BASIC PHASE-LOCKED LOOP OPERATION

PRINCIPLE OF OPERATION

The phase-locked loop (PLL) is a unique and versatile circuit technique which provides frequency selective tuning and filtering without the need for coils or inductors. As shown in Figure 12, the PLL is a feedback system comprised of three basic functional blocks: phase comparator, low-pass filter and voltage-controlled oscillator (VCO). The basic principle of operation of a PLL can be briefly explained as follows: with no input signal applied to the system, the error voltage V_d, is equal to zero. The VCO operates at a set frequency, f_o, which is known as the "free-running" frequency. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input frequency, f_s, is sufficiently close to f_o, the feedback nature of the PLL causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

A LINEARIZED MODEL FOR PLL

When the PLL is in lock, it can be approximated by the linear feedback system shown in Figure 13. ϕ_S and ϕ_O are the respective phase angles associated with the input signal and the VCO output, F(s) is the low-pass filter response in frequency domain, and K_d and K_o are the conversion gains associated with the phase comparator and VCO sections of the PLL.

DEFINITION OF XR-215 PARAMETERS FOR PLL APPLICATIONS

VCO FREE-RUNNING FREQUENCY, f_0

The VCO frequency with no input signal. It is determined by selection of C_0 across pins 13 and 14 and can be increased by connecting an external resistor R_X between pins 9 and 10. It can be approximated as:

$$f_o = \frac{200}{C_0}\left(1 + \frac{0.6}{R_X}\right)$$

where C_0 is in μF and R_X is in kΩ. (See Figure 7).

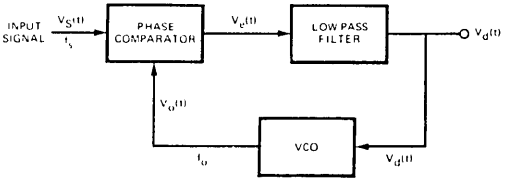


Figure 12. Block Diagram of a Phase-Locked Loop

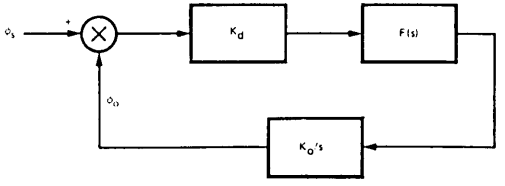


Figure 13. Linearized Model of a PLL as a Negative Feedback System

PHASE COMPARATOR GAIN K_d

The output voltage from the phase comparator per radian of phase difference at the phase comparator inputs (pins 4 and 6).

VCO CONVERSION GAIN K_o

The VCO voltage-to-frequency conversion gain is determined by the choice of timing capacitor C_0 and gain control resistor, R_0 connected externally across pins 11 and 12. It can be expressed as

$$K_o \approx \frac{700}{C_0 R_0} \text{ (radians/sec)/volt}$$

where C_0 is in μF and R_0 is in kΩ. For most applications, recommended values for R_0 range from 1 kΩ to 10 kΩ.

LOCK RANGE ($\Delta\omega_L$)

The range of frequencies in the vicinity of f_o, over which the PLL can maintain lock with an input signal. It is also known as the "tracking" or "holding" range. If saturation or limiting does not occur, the lock range is equal to the loop gain, i.e. $\Delta\omega_L = K_T = K_d K_o$.

CAPTURE RANGE ($\Delta\omega_C$)

The band of frequencies in the vicinity of f_o where the PLL can establish or acquire lock with an input signal. It is also known as the "acquisition" range. It is always smaller than the lock range and is related to the low-pass filter bandwidth. It can be approximated by a parametric equation of the form:

$$\Delta\omega_C \approx \Delta\omega_L |F(j\Delta\omega_C)|$$

where $|F(j\Delta\omega_C|$ is the low-pass filter magnitude response at $\omega = \Delta\omega_C$. For a simple lag filter, it can be expressed as:

$$\Delta\omega_C \approx \sqrt{\frac{\Delta\omega_L}{T_1}}$$

where T_1 is the filter time constant.

AMPLIFIER GAIN A_V

The voltage gain of the amplifier section is determined by feedback resistors R_F and R_P between pins (8,1) and 2,1) respectively. (See Figures 2 and 3). It is given by:

$$A_V = \frac{-R_F}{R_1 + R_P}$$

where R_1 is the 6 kΩ internal impedance at pin 2, and R_P is the external resistor between pins 1 and 2.

LOW-PASS FILTER

The low-pass filter section is formed by connecting an external capacitor or RC network across terminals 2 and 3. The low-pass filter components can be connected either between pins 2 and 3 or, from each pin to ground. Typical filter configurations and corresponding filter transfer functions are shown in Figure 14 where R_1 (6 kΩ) is the internal impedance at pins 2 and 3.

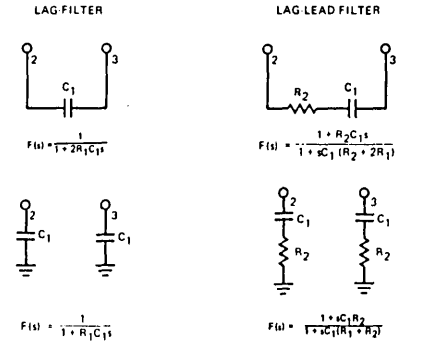


Figure 14.

APPLICATIONS INFORMATION

FM DEMODULATION

Figure 15 shows the external circuit connections to the XR-215 for frequency-selective FM demodulation. The choice of C_0 is determined by the FM carrier frequency (see Figure 7). The low-pass filter capacitor C_1 is determined by the selectivity requirements. For carrier frequencies of 1 to 10 MHz, C_1 is in the range of 10 C_0 to 30 C_0. The feedback resistor R_F can be used as a "volume-control" adjustment to set the amplitude of the demodulated output. The demodulated output amplitude is proportional to the FM deviation and to resistors R_0 and R_F. For $\pm 1\%$ FM deviation it can be approximated as:

$$V_{OUT} \approx R_0 R_F \left(1 + \frac{0.6}{R_X}\right) \text{ mV, rms}$$

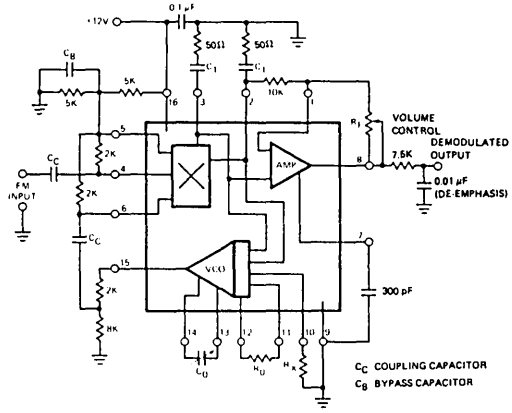


Figure 15. Circuit Connection for FM Demodulation

Note that for 300 Baud operation the circuit can be time-multiplexed between high and low bands by switching the external resistor R_X in and out of the circuit with a control signal, as shown in Figure 11.

FSK GENERATION

The digital programming capability of the XR-215 can be used for FSK generation. A typical circuit connection for this application is shown in Figure 21. The VCO frequency can be shifted between the mark (f_2) and space (f_1) frequencies by applying a logic pulse to pin 10. The circuit can provide two separate FSK outputs: a low level (2.5 V_{p-p}) output at pin 15 or a high amplitude (10 V_{p-p}) output at pin 8. The output at each of these terminals is a symmetrical squarewave with a typical second harmonic content of less than 0.3%.

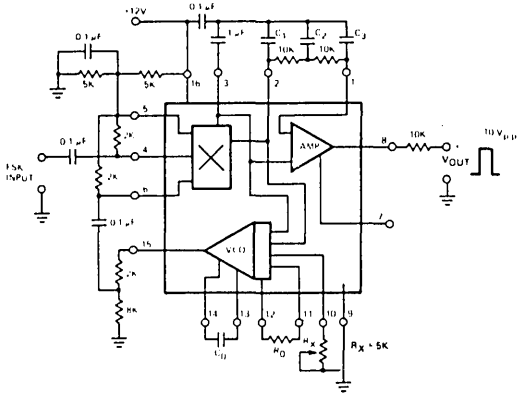


Figure 20. Circuit Connection for FSK Demodulation

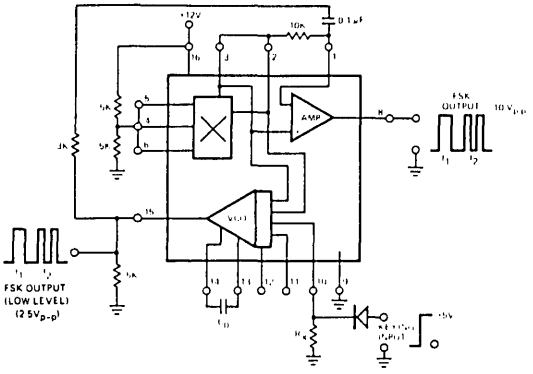


Figure 21. Circuit Connection For FSK Generation

FREQUENCY SYNTHESIS

In frequency synthesis applications, a programmable counter or divide-by-N circuit is connected between the VCO output (pin 15) and one of the phase detector inputs (pins 4 or 6), as shown in Figure 22. The principle of operation of the circuit can be briefly explained as

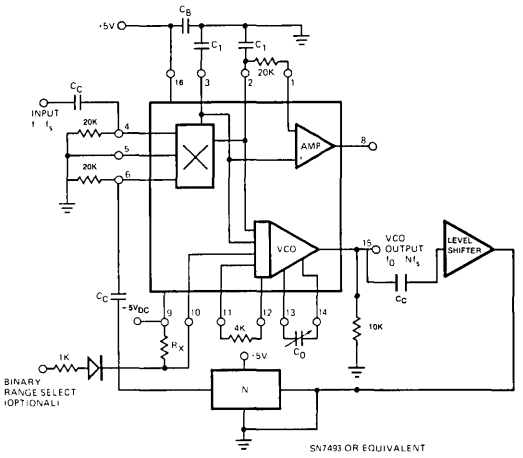


Figure 22. Circuit Connection For Frequency Synthesis

follows: The counter divides down the oscillator frequency by the programmable divider modulus, N. Thus, when the entire system is phase-locked to an input signal at frequency, f_S, the oscillator output at pin 15 is at a frequency (Nf_S), where N is the divider modulus. By proper choice of the divider modulus, a large number of discrete frequencies can be synthesized from a given reference frequency. The low-pass filter capacitor C_1 is normally chosen to provide a cut-off frequency equal to 0.1% to 2% of the signal frequency, f_S.

The circuit was designed to operate with commercially available monolithic programmable counter circuits using TTL logic, such as MC4016, SN5493 or equivalent. The digital or analog tuning characteristics of the VCO can be used to extend the available range of frequencies of the system, for a given setting of the timing capacitor C_0.

Typical input and output waveforms for N = 16 operation with f_S = 100 kHz and f_0 = 1.6 MHz are shown in Figure 23.

TRACKING FILTER/DISCRIMINATOR

The wide tracking range of the XR-215 allows the system to track an input signal over a 3:1 frequency range,

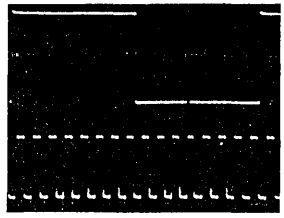


Figure 23. Typical Input/Output Waveforms For N = 16
Top: Input (100 kHz)
Bottom: VCO Output (1.6 MHz)
Vertical Scale 1 V/cm

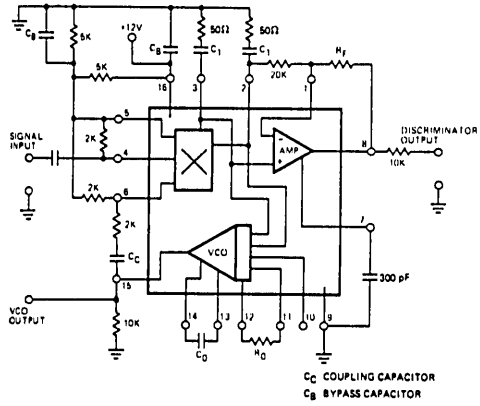


Figure 24. Circuit Connection For Tracking Filter Applications

centered about the VCO free running frequency. The tracking range is maximum when the binary range-select (pin 10) is open circuited. The circuit connections for this application are shown in Figure 24. Typical tracking range for a given input signal amplitude is shown in Figure 25. Recommended values of external components are: 1 kΩ < R_0 < 4 kΩ and 30 C_0 < C_1 < 300 C_0 where the timing capacitor C_0 is determined by the center frequency requirements (see Figure 7).

The phase-comparator output voltage is a linear measure of the VCO frequency deviation from its free-running value. The amplifier section, therefore, can be used to provide a filtered and amplified version of the loop error voltage. In this case, the dc output level at pin 15 can be adjusted to be directly proportional to the difference between the VCO free-running frequency, f_0, and the input signal, f_S. The entire system can operate as a "linear discriminator" or analog "frequency-meter" over a 3:1 change of input frequency. The discriminator gain can be adjusted by proper choice of R_0 or R_F. For the test circuit of Figure 24, the discriminator output is approximately (0.7 R_0R_F) mV per % of frequency deviation where R_0 and R_F are in kΩ. Output non-linearity is typically less than 1% for frequency deviations up to ±15%. Figure 27 shows the normalized output characteristics as a function of input frequency, with R_0 = 2 kΩ and R_F = 36 kΩ.

CRYSTAL-CONTROLLED PLL

The XR-215 can be operated as a crystal-controlled phase-locked loop by replacing the timing capacitor with a crystal. A circuit connection for this application is shown in Figure 26. Normally a small tuning capacitor (≈ 30 pF) is required in series with the crystal to set

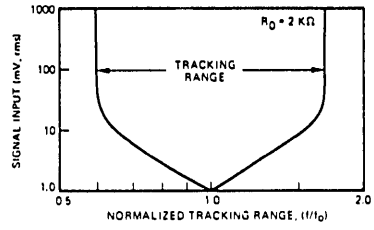


Figure 25. Tracking Range vs Input Amplitude (Pin 10 Open Circuited)

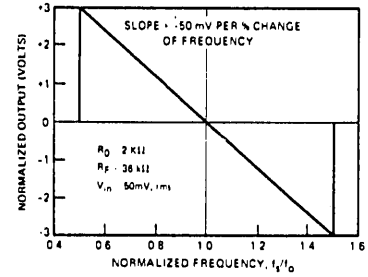


Figure 26. Typical Discriminator Output Characteristics For Tracking Filter Applications

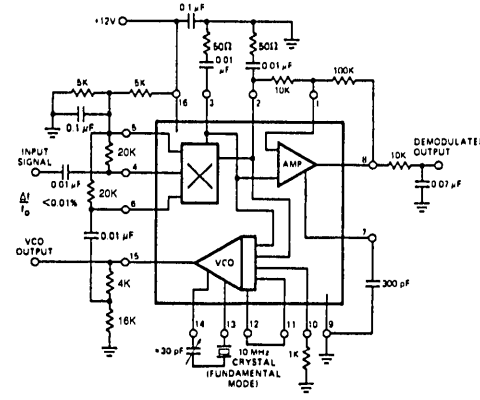


Figure 27. Typical Circuit Connection For Crystal-Controlled FM Detection

the crystal frequency. For this application the crystal should be operated in its fundamental mode. Typical pull-in range of the circuits is ±1 kHz at 10 MHz. There is some distortion on the demodulated output.

where all resistors are in kΩ and R_X is the range extension resistor connected across pins 9 and 10. For circuit operation below 5 MHz, R_X can be open circuited. For operation above 5 MHz, $R_X \approx 750\Omega$ is recommended.

Typical output signal/noise ratio and harmonic distortion are shown in Figures 16 and 17 as a function of FM deviation, for the component values shown in Figure 4.

MULTI-CHANNEL DEMODULATION

The ac digital programming capability of the XR-215 allows a single circuit be time-shared or multiplexed between two information channels, and thereby selectively demodulate two separate carrier frequencies. Figure 18 shows a practical circuit configuration for time-multiplexing the XR-215 between two FM channels, at 1 MHz and 1.1 MHz respectively. The channel-select logic signal is applied to pin 10, as shown in Figure 18 with both input channels simultaneously present at the PLL input (pin 4). Figure 19 shows the demodulated output as a function of the channel-select pulse where the two inputs have sinusoidal and triangular FM modulation respectively.

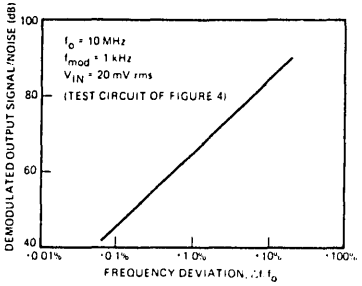


Figure 16. Output Signal/Noise Ratio as a Function of FM Deviation

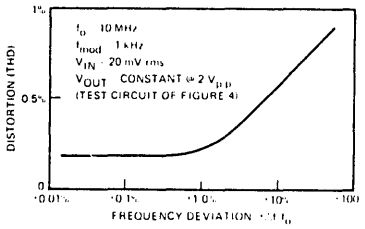


Figure 17. Output Distortion as a Function of FM Deviation

FSK DEMODULATION

Figure 20 contains a typical circuit connection for FSK demodulation. When the input frequency is shifted, corresponding to a data bit, the dc voltage at the phase comparator outputs (pins 2 and 3) also reverses polarity. The operational amplifier section is connected as a comparator, and converts the dc level shift to a binary output pulse. One of the phase comparator outputs (pin

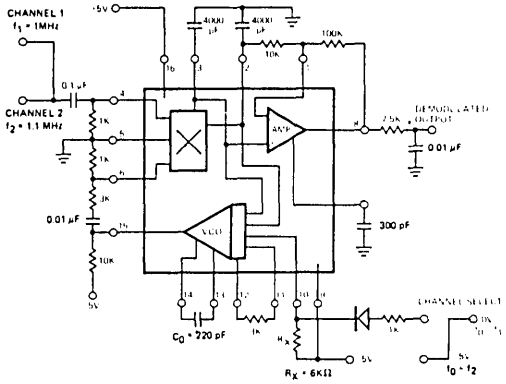


Figure 18. Time-Multiplexing XR-215 Between Two Simultaneous FM Channels

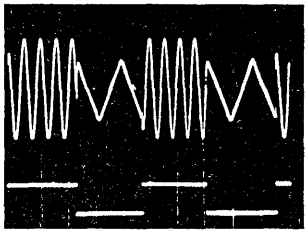


Figure 19. Demodulated Output Waveforms for Time-Multiplexed Operation

Top: Demodulated Output
Sinewave - Channel 1
Triangle Wave - Channel 2

Bottom: Channel Select Pulse

3) is ac grounded and serves as the bias reference for the operational amplifier section. Capacitor C_1 serves as the PLL loop filter, and C_2 and C_3 as post-detection filters. Range select resistor, R_X, can be used as a fine-tune adjustment to set the VCO frequency.

Typical component values for 300 baud and 1200 baud operation are listed below:

OPERATING CONDITIONS	TYPICAL COMPONENT VALUES
300 Baud	
Low Band: f_1 = 1070 Hz	R_0 = 5 kΩ, C_0 = 0.17 μF
f_2 = 1270 Hz	$C_1 = C_2$ = 0.047 μF, C_3 = 0.033 μF
High Band: f_1 = 2025 Hz	R_0 = 8 kΩ, C_0 = 0.1 μF
f_2 = 2225 Hz	$C_1 = C_2 = C_3$ = 0.033 μF
1200 Baud	R_0 = 2 kΩ, C_0 = 0.12 μF
f_1 = 1200 Hz f_2 = 2200 Hz	$C_1 = C_3$ = 0.003 μF, C_2 = 0.01 μF

FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides ratio metric operation for low system performance variations with power supply changes.

The XR-2211 is available in 14 pin DIP ceramic or plastic packages specified for commercial or military temperature ranges.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20 V
DTL/TTL/ECL Logic Compatibility	
FSK Demodulation, with Carrier Detection	
Wide Dynamic Range	2 mV to 3 V rms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

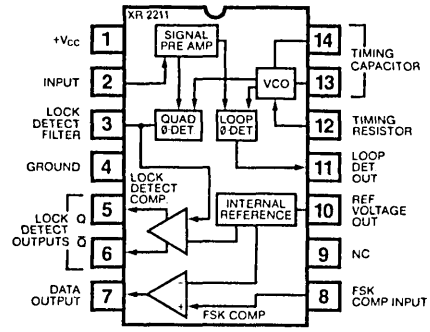
APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	
Ceramic Package	750 mW
Derate Above T_A = +25°C	6 mV/°C
Plastic Package	
Derate Above T_A = +25°C	5.0 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	−55°C to +125°C
XR-2211CN	Ceramic	0°C to +70°C
XR-2211CP	Plastic	0°C to +70°C
XR-2211N	Ceramic	−40°C to +85°C
XR-2211P	Plastic	−40°C to +85°C

SYSTEM DESCRIPTION

The main PLL within the XR-2211 is constructed from an input preamplifier, analog multiplier used as a phase detector, and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that input signals above typically 2mV RMS are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (unfiltered) produces sum and difference frequencies of the input and the VCO output, f input + f input (2f input) and f input - f input (0 Hz) when the phase detector output to remove the "sum" frequency component while passing the difference (DC) component to drive the VCO. The VCO is actually a current controlled oscillator with its nominal input current (f_0) set by a resistor (R_0) to ground and its driving current with a resistor (R_1) from the phase detector.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produced both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator).

XR-2211

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, $C = 5000$ pF, $R_1 = R_2 = R_3 = R_4 = 20$ kΩ, $R_L = 4.7$ kΩ. Binary Inputs grounded, S_1 and S_2 closed, unless otherwise specified.

PARAMETER	XR-2211/2211M			XR-2211C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Current		4	7		5	9	mA	$R_0 \geq 10$ kΩ. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = 1/2$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1$V. See Fig. 7.
		0.2			0.2		%/V	$V^+ 5 \pm 0.5$V. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2$ kΩ, $C_0 = 400$ pF
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2$ MΩ, $C_0 = 50$ μF
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	kΩ	
Recommended Range	15		100	15		100	kΩ	See Figs. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	Measured at Pin 11.
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current	100	150			150		μA	
Output Impedance		1			1		MΩ	
Maximum Swing		11			11		V pp	
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		kΩ	
Input Signal								
Voltage Required to								
Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTIONS								
Input Impedance		2			2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100			100		nA	
Voltage Gain	55	70		55	70		dB	$R_L = 5.1$ kΩ
Output Voltage Low		300			300		mV	$I_C = 3$ mA
Output Leakage Current		0.01			0.01		μA	$V_O = 12$V
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	AC Small Signal
Maximum Source Current		80			80		μA	

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 2) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, Pin 3 can be left open circuited.

Lock Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

Lock Detect Complement, $\overline{Q}$ (Pin 6): The output at Pin 6 is the logic complement of the lock detect output at Pin 5. This output is also an open collector type stage which can sink 5 mA of load current at low or "on" state.

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (Pin 11). This data filter is formed by R_F and C_F of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

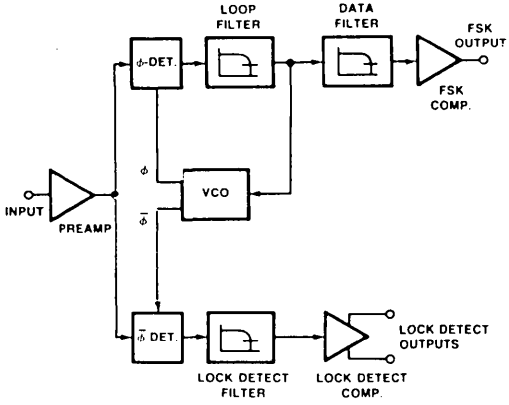


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: $V_R = V+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at Pins 5, 8, 11 and 12. Pin 10 *must* be bypassed to ground with a 0.1 μF capacitor for proper operation of the circuit.

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (see Figure 2). With no input signal, or with no phase error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

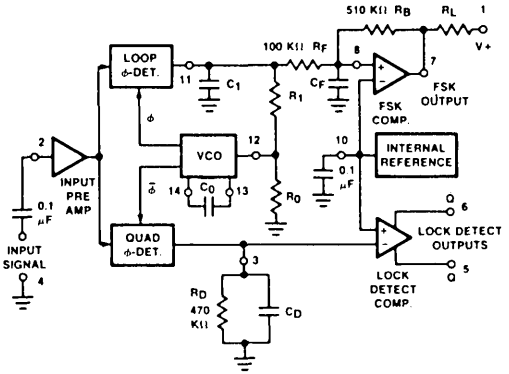


Figure 2. Generalized Circuit Connection for FSK and Tone Detection

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ see Figure 8).

This terminal is a low impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200 pF to 10 μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 9).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjust-

ment purposes, VCO free-running frequency can be measured at Pin 3 (with C_D disconnected), with no input and with Pin 2 shorted to Pin 10.

DESIGN EQUATIONS

(See Figure 2 for definition of components.)

1. VCO Center Frequency, f_0:

   $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 10):

   $V_R = V+/2 - 650$ mV

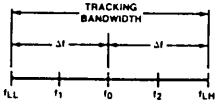
3. Loop Low-Pass Filter Time Constant, τ:

   $\tau = R_1C_1$

4. Loop Damping, ζ:

   $$\zeta = 1/4\sqrt{\frac{C_0}{C_1}}$$

5. Loop Tracking Bandwidth, $\pm \Delta f/f_0$:
   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τF:
   $\tau F = R_FC_F$

7. Loop Phase Detector Conversion Gain, $K\phi$: ($K\phi$ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase detector input):

   $K\phi = 02V_R/\pi$ volts/radian

8. VCO Conversion gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 11):

   $K_0 = -1/V_RC_0R_1$ Hz/volt

9. Total Loop Gain, K_T:

   $K_T = 2\pi K\phi K_0 = 4/C_0R_1$ rad/sec/volt

10. Peak Phase Detector Current I_A:

    $I_A = V_R$ (volts)/25 mA

APPLICATIONS INFORMATION

FSK DECODING:

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 KΩ) from Pin 7 to Pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table 1.

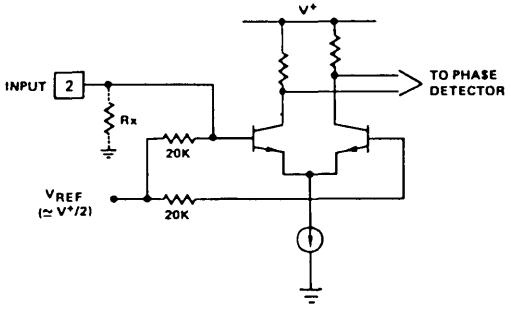
Design Instructions:

The circuit of Figure 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f_0:

$$f_O = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R_0, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary.



$$V_{IN\ MINIMUM\ (PEAK)} \approx V+ \left[\frac{10K}{R_X + 20K}\right] \pm 2.8\ mV$$

Figure 3. Desensitizing Input Stage

The recommended value is $R_0 \equiv 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Figure 6:

$C_0 = 1/R_0f_0$

d) Calculate R_1 to give a Δf equal to the mark space deviation:

$R_1 = R_0[f_0/(f_1 = f_2)]$

e) Calculate C_1 to set loop damping. (See design equation No. 4.):

Normally, $\zeta \approx 1/2$ is recommended.

Then: $C_1 = C_0/4$ for $\zeta = 1/2$

f) Calculate Data Filter Capacitance, C_F:

For R_F = 100 KΩ, R_B = 510 KΩ, the recommended value of C_F is:

$C_F \approx 3/(\text{Baud Rate})\ \mu F$

Note: All calculated component values except R_0 can be rounded to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Figure 9.)

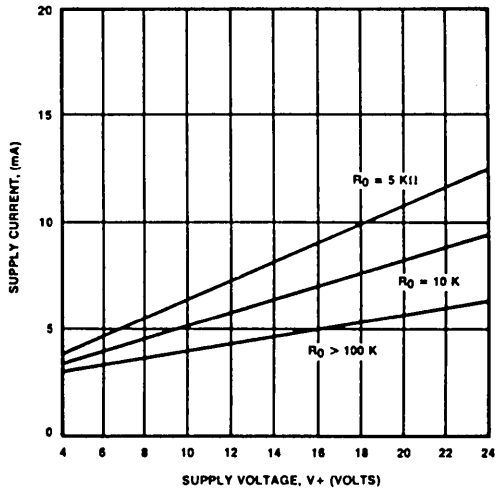


Figure 4. Typical Supply Current vs V+ (Logic Outputs Open Circuited)

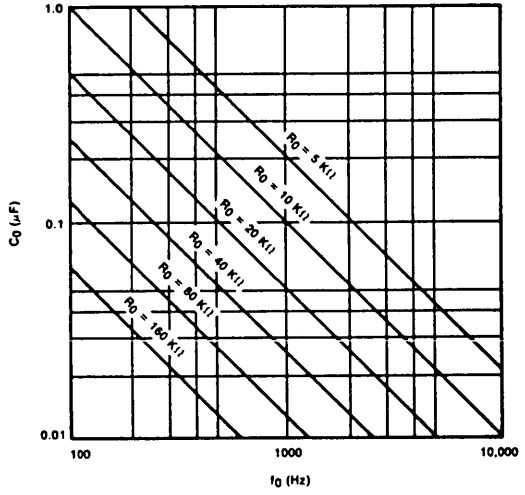


Figure 5. VCO Frequency vs Timing Resistor

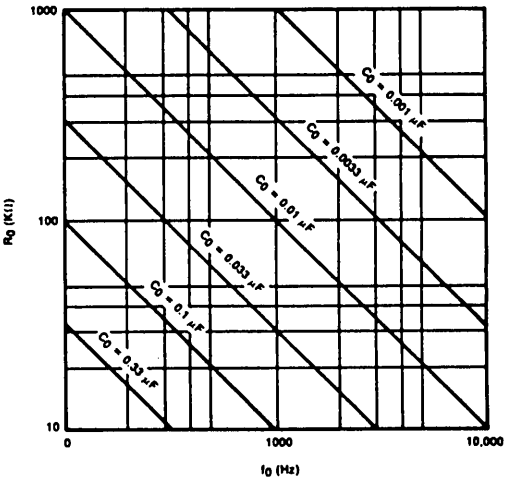


Figure 6. VCO Frequency vs Timing Capacitor

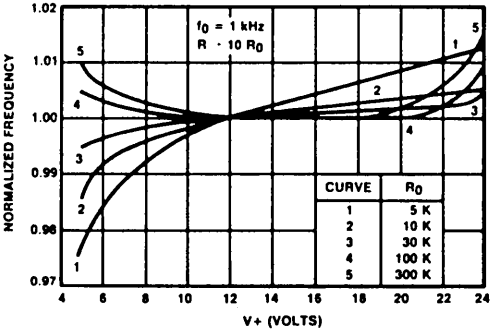


Figure 7. Typical f_0 vs Power Supply Characteristics

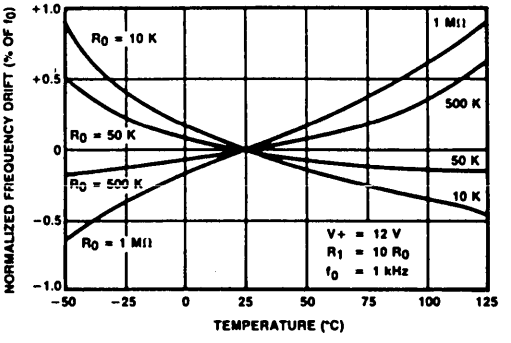


Figure 8. Typical Center Frequency Drift vs Temperature

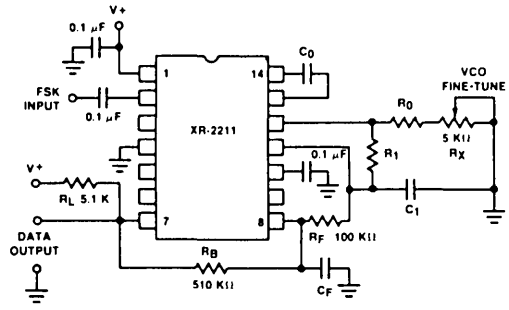


Figure 9. Circuit Connection for FSK Decoding

Design Example:

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0: f_0 (1110 + 1170) (1/2) = 1140 Hz

Step 2: Choose R_0 - 20 KΩ (18 KΩ fixed resistor in series with 5 KΩ potentiometer)

Step 3: Calculate C_0 from Figure 6: C_0 = 0.044 μF

Step 4: Calculate R_1: R_1 = R_0 (2240/60) = 380 KΩ

Step 5: Calculate C_1: C_1 = C_0/4 = 0.011 μF

Note: All values except R_0 can be rounded to *nearest* standard value.

Table 1. Recommended Component Values for Commonly Used FSK Bands. (See Circuit of Figure 9.)

FSK BAND	COMPONENT VALUES
300 Baud f_1 = 1070 Hz F_2 = 1270 Hz	C_O = 0.039 μF C_F = 0.005 μF C_1 = 0.01 μF R_O = 18 KΩ R_1 = 100 KΩ
300 Baud f_1 = 2025 Hz f_2 = 2225 Hz	C_O = 0.022 μF C_F = 0.005 μF C_1 = 0.0047 μF R_O = 18 KΩ R_1 = 200 KΩ
1200 Baud f_1 = 1200 Hz f_2 = 2200 Hz	C_O = 0.027 μF C_F = 0.0022 μF C_1 = 0.01 μF R_O = 18 KΩ R_1 = 30 KΩ

FSK DECODING WITH CARRIER DETECT:

The lock detect section of XR-2211 can be used as a carrier detect option, for FSK decoding. The recommended circuit connection for this application is shown in Figure 10. The open collector lock detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output will be disabled at "low" state, until there is a carrier within the detection band of the PPL, and the Pin 6 output goes "high," to enable the data output.

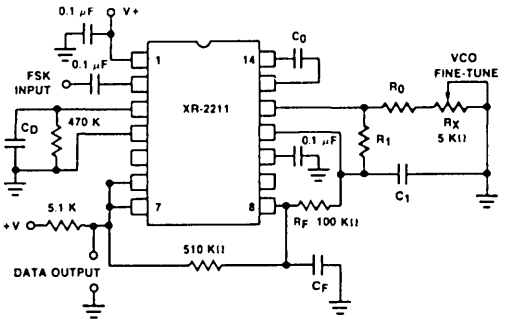


Figure 10. External Connectors for FSK Demodulation with Carrier Detect Capability

Note: Data Output is "Low" When No Carrier is Present.

The minimum value of the lock detect filter capacitance C_D is inversely proportional to the capture range, ± Δf_C. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_C > \Delta f/2$. For R_D = 470 KΩ, the approximate minimum value of C_D can be determined by:

C_D (μF) ≥ 16/capture range in Hz.

With values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output.

TONE DETECTION:

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

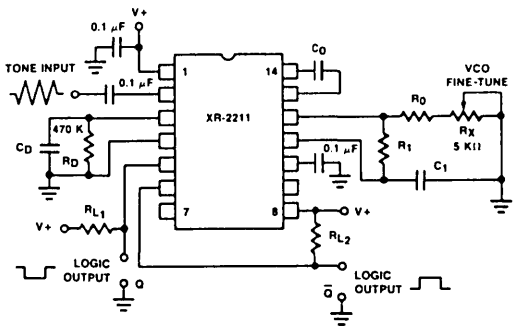


Figure 11. Circuit Connection for Tone Detection

Both logic outputs at Pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Figure 11.

With reference to Figures 2 and 11, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions:

The circuit of Figure 11 can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input, the tone frequency, f_S, these parameters are calculated as follows:

a) Choose R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary.

b) Calculate C_0 to set center frequency, f_0 equal to f_S (see Figure 6): $C_0 = 1/R_0 f_S$

c) Calculate R_1 to set bandwidth $\pm\Delta f$ (see design equation No. 5):

$R_1 = R_0(f_0/\Delta f)$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

d) Calculate value of C_1 for a given loop damping factor;

$C_1 = C_0/16\,\zeta^2$

Normally $\zeta \approx 1/2$ is optimum for most tone detector applications, giving $C_1 = 0.25\,C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470 KΩ, C_D must be:

$C_D(\mu F) \geq$ (16/capture range in Hz)

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1 kHz ± 20 Hz:

a) Choose R_0 = 20 KΩ (18 KΩ in series with 5 KΩ potentiometer).

b) Choose C_0 for f_0 = 1 kHz (from Figure 6): C_0 = 0.05 μF.

c) Calculate R_1: $R_1 = (R_0)(1000/20)$ = 1 MΩ.

d) Calculate C_1: for ζ = 1/2, C_1 = 0.25, C_0 = 0.013 μF.

e) Calculate C_D: C_D = 16/38 = 0.42 μF.

f) Fine-tune center frequency with 5 KΩ potentiometer, R_X.

LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Figure 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post-detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 12.

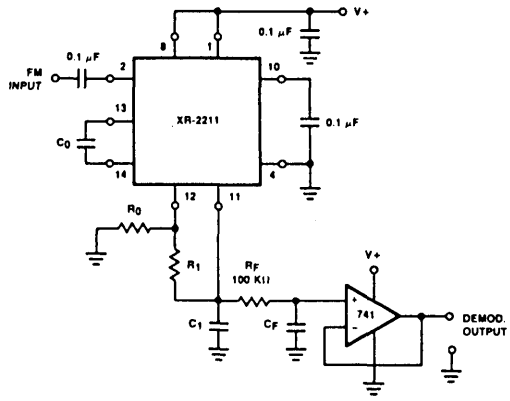


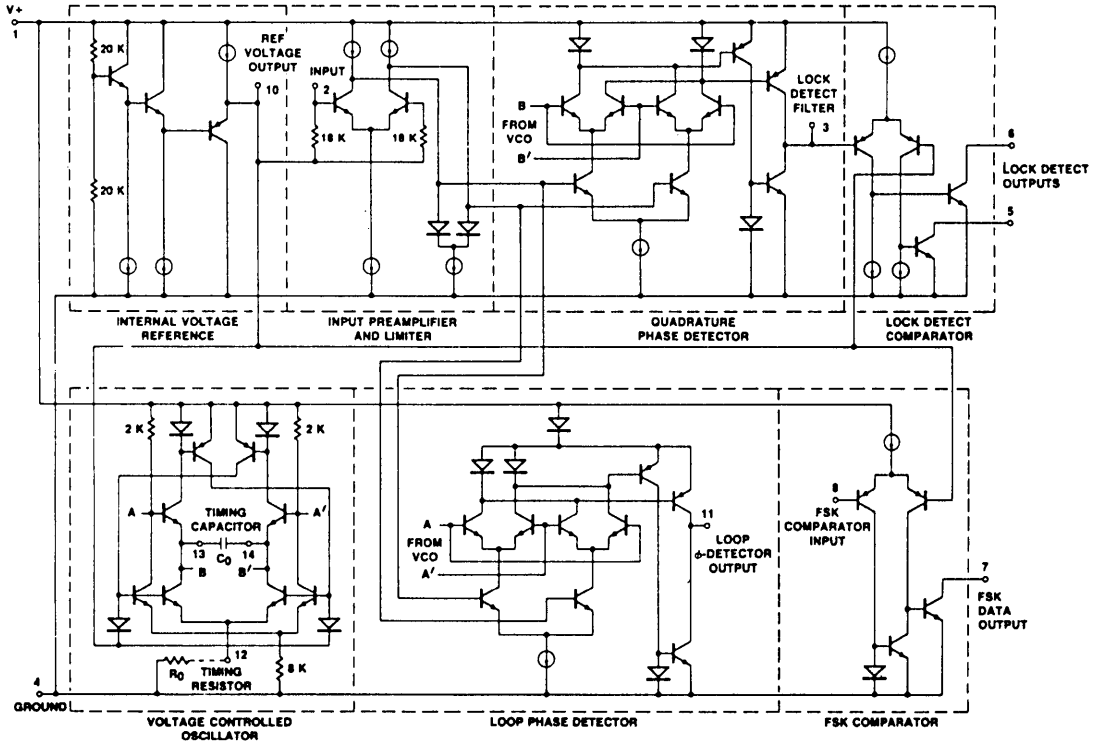
Figure 12. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section on Design Equation for Component Values.)

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$V_{out} = R_1\,V_R/100\,R_0$ Volts/% deviation

where V_R is the internal reference voltage (V_R = V+/2 − 650 mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on design equations.

EQUIVALENT SCHEMATIC DIAGRAM



6

Precision Phase-Locked Loop

GENERAL DESCRIPTION

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communications and control system applications. Its on board reference and uncommitted operational amplifier, together with a typical temperature stability of better than 20 ppm/°C, make it ideally suited for frequency synthesis, FM detection, and tracking filter applications. The wide input dynamic range, large operating voltage range, large frequency range, and ECL, DTL, and TTL compatibility contribute to the usefulness and wide applicability of this device.

FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DTL/TTL/ECL Logic Compatibility	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, Typ.

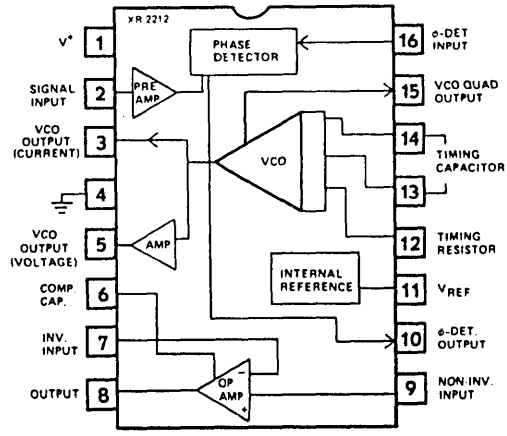
APPLICATIONS

Frequency Synthesis
Data Synchronization
FM Detection
Tracking Filters
FSK Demodulation

ABSOLUTE MAXIMUM RATINGS

Power Supply	18V
Input Signal Level	3 Vrms
Power Dissipation	
Ceramic Package:	750 mW
Derate Above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate Above T_A = +25°C	5 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2212M	Ceramic	−55°C to +125°C
XR2212CN	Ceramic	0°C to +70°C
XR-2212CP	Plastic	0°C to +70°C
XR-2212N	Ceramic	−40°C to +85°C
XR-2212P	Plastic	−40°C to +85°C

SYSTEM DESCRIPTION

The XR-2212 is a complete PLL system with buffered inputs and outputs, an internal reference, and an uncommited op amp. Two VCO outputs are pinned out; one sources current, the other sources voltage. This enables operation as a frequency synthesizer using an external programmable divider. The op amp section can be used as an audio preamplifier for FM detection or as a high speed sense amplifier (comparator) for FSK demodulation. The center frequency, bandwidth, and tracking range of the PLL are controlled independantly by external components. The PLL output is directly compatible with MOS, DTL, ECL, and TTL logic families as well as microprocessor peripheral systems.

The precision PLL system operates over a supply voltage range of 4.5 V to 20 V, a frequency range of 0.01 Hz to 300 kHz, and accepts input signals in the range of 2 mV to 3 Vrms. Temperature stability of the VCO is typically better than 20 ppm/°C.

XR-2212

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +12V$, $T_A = +25°C$, $R_0 = 30\ k\Omega$, $C_0 = 0.033\ \mu F$, unless otherwise specified. See Figure 2 for component designation.

PARAMETERS	XR-2212/2212M			XR-2212C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply Voltage	4.5		15	4.5		15	V	
Supply Current		6	10		6	12	mA	$R_0 \geq 10\ K\Omega$. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = \infty$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1$ V. See Fig. 7.
		.2			.2		%/V	$V^+ = 5 \pm 0.5$ V. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2\ K\Omega$, $C_0 = 400$ pF
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2\ M\Omega$, $C_0 = 50\ \mu F$
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	KΩ	
Recommended Range	15		100	15		100	KΩ	See Fig. 7 and 8.
OSCILLATOR OUTPUTS								
Voltage Output								Measured at Pin 5.
Positive Swing, V_{OH}		11			11		V	
Negative Swing, V_{OL}	.8	.4			.5		V	
Current Sink Capability		1			1		mA	
Current Output								Measured at Pin 3.
Peak Current Swing	100	150			150		μA	
Output Impedance		1			1		MΩ	
Quadrature Output								Measured at Pin 15.
Output Swing		0.6			0.6		V	
DC Level		0.3			0.3		V	Referenced to Pin 11.
Output Impedance		3			3		KΩ	
LOOP PHASE DETECTOR SECTION								Measured at Pin 10.
Peak Output Current	±150	±200	±300	±100	±200	±300	μA	
Output Offset Current		±1			±2		μA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 11.
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		KΩ	
Input Signal to Cause Limiting		2	10		2		mVrms	
OP AMP SECTION								
Voltage Gain	55	70		55	70		dB	$R_L = 5.1\ K\Omega$, $R_F = \infty$
Input Bias Current		0.1	1		0.1	1	μA	
Offset Voltage		±5	±20		±5	±20	mV	
Slew Rate		2			2		V/μsec	
INTERNAL REFERENCE								Measured at Pin 11.
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	
Output Impedance		100			100		Ω	

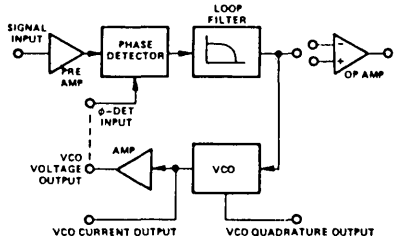


Figure 1. Functional Block Diagram of XR-2212 Precision PLL System

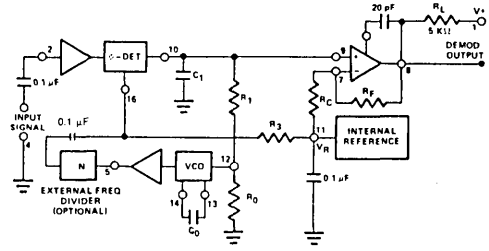


Figure 2. Generalized Circuit Connection for FM Detection, Signal Tracking or Frequency Synthesis

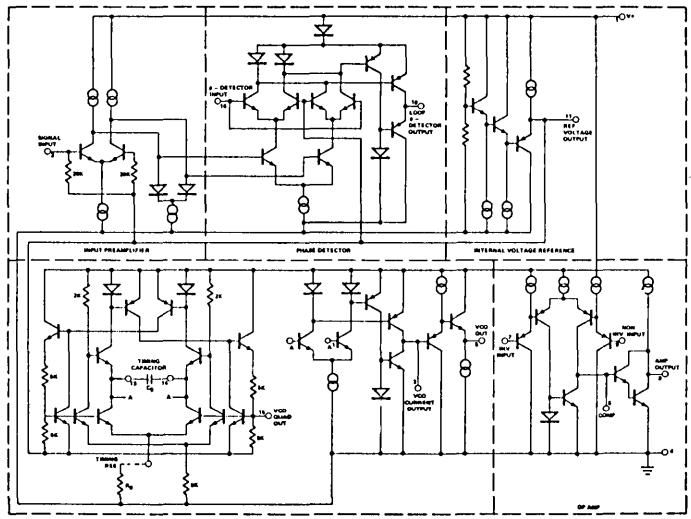


Figure 3. Simplified Circuit Schematic of XR-2212

TYPICAL CHARACTERISTICS

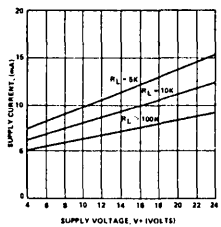


Figure 4. Typical Supply Current vs V+ (Logic Outputs Open Circuited)

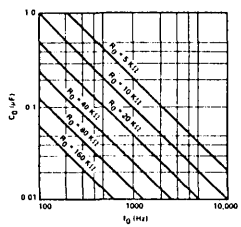


Figure 5. VCO Frequency vs Timing Resistor

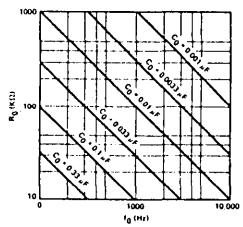


Figure 6. VCO Frequency vs Timing Capacitor

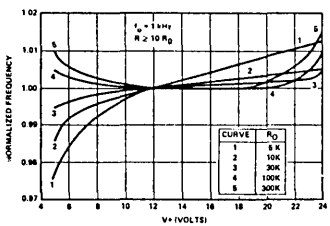


Figure 7. Typical f_0 vs Power Supply Characteristics

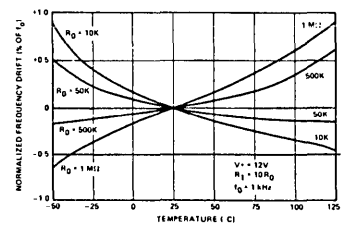


Figure 8. Typical Center Frequency Drift vs Temperature

DESCRIPTION OF CIRCUIT CONTROLS

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV to 5V peak-to-peak.

VCO Current Output (Pin 3): This is a high impedance (MΩ) current output terminal which can provide ±100 μA drive capability with a voltage swing equal to V+. This output can directly interface with CMOS or NMOS logic families.

VCO Voltage Output (Pin 5): This terminal provides a low-impedance (≈ 50Ω) buffered output for the VCO. It can directly interface with low-power Schottley TTL. For interfacing with standard TTL circuits, a 750Ω pull-down resistor from pin 5 to ground is required. For operation of the PLL without an external divider, pin 5 can be dc coupled to pin 16.

Op Amp Compensation (Pin 6): The op amp section is frequency compensated by connecting an external capacitor from pin 6 to the amplifier output (pin 8). For unity-gain compensation a 20 pF capacitor is recommended.

Op Amp Inputs (Pins 7 and 9): These are the inverting and the non-inverting inputs for the op amp section. The common-mode range of the op amp inputs is from +1V to (V+ − 1.5) volts.

Op Amp Output (Pin 8): The op amp output is an open-collector type gain stage and requires a pull-up resistor, R_L, to V+ for proper operation. For most applications, the recommended value of R_L is in 5 kΩ to 10 kΩ range.

Phase Detector Output (Pin 10): This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 10 (see Figure 2). With no input signal, or with no phase-error within the PLL, the dc level at Pin 10 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

Reference Voltage, V_R (Pin 11): This pin is internally biased at the reference voltage level, V_R:V_R = V+/2—650 mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 10, 12 and 16. Pin 1 *must* be bypassed to ground with a 0.1 μF capacitor, for proper operation of the circuit.

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ (see Figure 8).

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 10).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200 pF to 10 μF.

VCO Quadrature Output (Pin 15): The low-level (≈0.6 Vpp) output at this pin is at quadrature phase (i.e. 90° phase-offset) with the other VCO outputs at pins 3 and 5. The dc level at pin 15 is approximately 300 mV above V_R. The quadrature output can be used with an external multiplier as a "lock detect" circuit. In order not to degrade oscillator performance, the output at pin 15 must be buffered with an external high-impedance low-capacitance amplifier. When not in use, pin 15 should be left open-circuited.

Phase Detector Input (Pin 16): Voltage output of the VCO (pin 5) or the output of an external frequency divider is connected to this pin. The dc level of the sensing threshold for the phase detector is referenced to V_R. If the signal is capacitively coupled to pin 16, then this pin must be biased from pin 11, through an external resistor, R_B ($R_B \approx 10$ KΩ). The peak voltage swing applied to pin 16 *must not* exceed (V+ − 1.5) volts.

PHASE-LOCKED LOOP PARAMETERS:

Transfer Characteristics:

Figure 9 shows the basic frequency to voltage characteristics of XR-2212. With no input signal present, filtered phase detector output voltage is approximately equal to the internal reference voltage, V_R, at pin 11. The PLL can track an input signal over its tracking bandwidth, shown in the figure. The frequencies f_{TL} and f_{TH} represent the lower and the upper edge of the tracking range, f_0 represents the VCO center frequency.

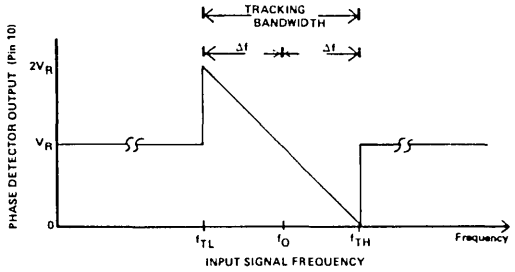


Figure 9. Phase Detector Output Voltage (Pin 10) as a Function of Input Signal Frequency. Note: Output Voltage is Referenced to Internal Reference Voltage V_R at Pin 11

Design Equations:

(See Figure 2 and Figure 9 for definition of components.)

1. VCO Center Frequency, f_0: $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 11)

   $V_R = V+/2 - 650\ mV$

3. Loop Low-Pass Filter Time Constant, τ: $\tau = R_1C_1$

4. Loop Damping, ζ: $\zeta = 1/4\sqrt{\frac{NC_0}{C_1}}$

   where N is the external frequency divider modular (See 2). If no divider is used, N = 1.

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$: $\Delta f/f_0 = R_0/R_1$

6. Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase-detector input) $K_\phi = -2V_R/\pi$ volts/radian

7. VCO Conversion Gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 10. It is the reciprocal of the slope of conversion characteristics shown in Figure 9). $K_0 = -1/V_RC_0R_1$ Hz/volt

8. Total Loop Gain, K_T:

   $K_T = 2\pi K_\phi K_0 = 4/C_0R_1$ rad/sec/volt

9. Peak Phase-Detector Current, I_A; available at pin 10.

   $I_A = V_R$ (volts)/25 mA

APPLICATION INFORMATION

FM DEMODULATION:

XR-2212 can be used as a linear FM demodulator for both narrow-band and wide-band FM signals. The generalized circuit connection for this application is shown in Figure 10, where the VCO output (pin 5) is directly connected to the phase detector input (pin 16). The demodulated signal is obtained at phase detector output (pin 10). In the circuit connection of Figure 10, the op amp section of XR-2212 is used as a buffer amplifier to provide both additional voltage amplification as well as current drive capability. Thus, the demodulated output signal available at the op amp output (pin 8) is fully buffered from the rest of the circuit.

In the circuit of Figure 10, R_0C_0 set the VCO center frequency, R_1 sets the tracking bandwidth, C_1 sets the low-pass filter time constant. Op amp feedback resistors R_F and R_C set the voltage gain of the amplifier section.

Design Instructions:

The circuit of Figure 10 can be tailored to any FM demodulation application by a choice of the external components R_0, R_1, R_C, R_F, C_0 and C_1. For a given FM center frequency and frequency deviation, the choice of these components can be calculated as follows, using the design equations and definitions given on page 1-34, 1-35 and 1-36.

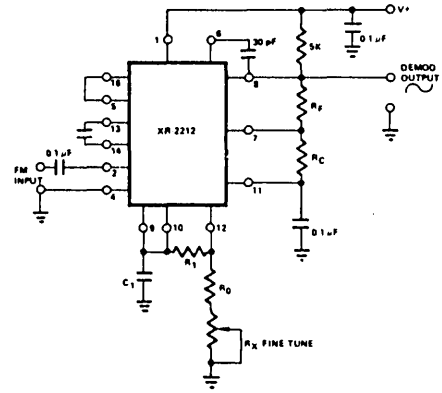


Figure 10. Circuit Connection for FM Demodulation

a) Choose VCO center frequency f_0 to be the same as FM carrier frequency.

b) Choose value of timing resistor R_0, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is $R_0 \cong 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

c) Calculate value of C_0 from design equation (1) or from Figure 6:

$$C_0 = 1/R_0f_0$$

d) Choose R_1 to determine the tracking bandwidth, Δf (see design equation 5). The tracking bandwidth, Δf, should be set significantly wider than the maximum input FM signal deviation, Δf_{SM}. Assuming the tracking bandwidth to be "N" times larger than Δf_{SM}, one can re-unite design equation 5 as:

$$\frac{\Delta f}{f_0} = \frac{R_0}{R_1} = N\frac{\Delta f_{SM}}{f_0}$$

Table I lists recommended values of N, for various values of the maximum deviation of the input FM signal.

% Deviation of FM Signal ($\Delta f_{SM}/f_0$)	Recommended value of Bandwidth Ratio, N ($N = \Delta f/\Delta f_{SM}$)
1% or less	10
1 to 3%	5
1 to 5%	4
5 to 10%	3
10 to 30%	2
30 to 50%	1.5

TABLE I

Recommended values of bandwidth ratio, N, for various values of FM signal frequency deviation. (Note: N is the ratio of tracking bandwidth Δf to max. signal frequency deviation, Δf_{SM}).

e) Calculate C_1 to set loop damping (see design equation 4). Normally, $\zeta = 1/2$ is recommended. Then, $C_1 = C_0/4$ for $\zeta = 1/2$.

f) Calculate R_C and R_F to set peak output signal amplitude. Output signal amplitude, V_{out}, is given as:

$$V_{out} = \left(\frac{\Delta f_{SM}}{f_0}\right)\left(V_R\right)\left(\frac{R_1}{R_0}\right)\left[\frac{R_C + R_F}{R_C}\right]$$

In most applications, $R_F = 100\ K\Omega$ is recommended; then R_C, can be calculated from the above equation to give desired output swing. The output amplifier can also be used as a unity-gain voltage follower, by open circuiting R_C (i.e., $R_C = \infty$).

Note: All calculated component values except R_0 can be rounded-off to the nearest standard value, and R_0 can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Figure 10.)

Design Example:

Demodulator for FM signal with 67 kHz carrier frequency with ±5 kHz frequency deviation. Supply voltage is +12V and required peak output swing is ±4 volts.

Step a) f_0 is chosen as 67 kHz.

Step b) Choose $R_0 = 20\ K\Omega$ (18 KΩ fixed resistor in series with 5 KΩ potentiometer).

Step c) Calculate C_0; from design Eq. (1).

$C_0 = 746$ pF

Step d) Calculate R_1. For given FM deviation, $\Delta f_{SM}/f_0 = 0.0746$, and N = 3 from Table I.

Then:

$R_0/R_1 = (3)(0.0746) = 0.224$

or:

$R_1 = 89.3\ K\Omega$.

Step e) Calculate $C_1 = (C_0/4) = 186$ pF.

Step f) Calculate R_C and R_F to get ±4 volts peak output swing: Let $R_F = 100\ K\Omega$. Then,

$R_C = 80.6\ K\Omega$.

Note: All values except R_0 can be rounded-off to nearest standard value.

FREQUENCY SYNTHESIS

Figure 11 shows the generalized circuit connection for frequency synthesis. In this application an external frequency divider is connected between the VCO output (pin 5) and the phase-detector input (pin 16). When the circuit is in lock, the two signals going into the phase-detector are at the same frequency, or $f_S = f_1/N$ where N is the modulus of the external frequency divider. Conversely, the VCO output frequency, f_1 is equal to Nf_S.

In the circuit configuration of Figure 11, the external timing components, R_0 and C_0, set the VCO free-running frequency; R_1 sets the tracking bandwidth and C1 sets the loop damping, i.e., the low-pass filter time constant (see design equations).

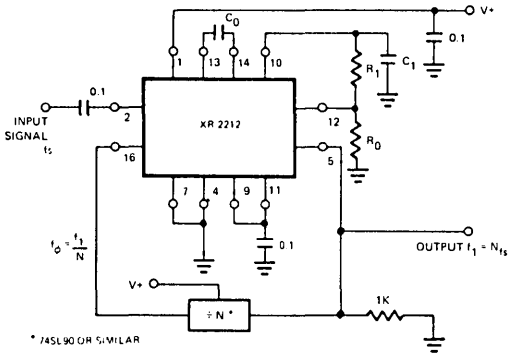


Figure 11. Circuit Connection for Frequency Synthesizer

The total tracking range of the PLL (see Figure 9), should be chosen to accommodate the lowest and the highest frequency, f_{max} and f_{min}, to be synthesized. A recommended choice for most applications is to choose a tracking half-bandwidth Δf, such that:

$$\Delta f \approx f_{max} - f_{min}.$$

If a fixed output frequency is desired, i.e. N and f_S are fixed, then a ±10% tracking bandwidth is recommended. Excessively large tracking bandwidth may cause the PLL to lock on the harmonics of the input signals; and the small tracking range increases the "lock-up" or acquisition time.

If a variable input frequency and a variable counter modulus N is used, then the maximum and the minimum values of output frequency will be:

$$f_{max} = N_{max}\,(f_S)_{max} \text{ and } f_{min} = N_{min}\,(f_S)_{min}.$$

Design Instructions:

For a given performance requirement, the circuit of Figure 11 can be optimized as follows:

a) Choose center frequency, f_0, to be equal to the output frequency to be synthesized. If a range of output frequencies is desired, set f_0 to be at mid-point of the desired range.

b) Choose timing resistor R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary. R_0 can be fine tuned with a series potentiometer, R_X.

c) Choose timing capacitor, C_0 from Figure 6 or Equation 1.

d) Calculate R_1 to set tracking bandwidth (see Figure 9, and design equation 5). If a range of output frequencies are desired, set R_1 to get:

$$\Delta f = f_{max} - f_{min}.$$

If a single fixed output frequency is desired, set R_1 to get:

$$\Delta f = 0.1\ f_0.$$

e) Calculate C_1 to obtain desired loop damping. (See design equation 4). For most applications, $\zeta = 1/2$ is recommended, thus:

$$C_1 = NC_0/4$$

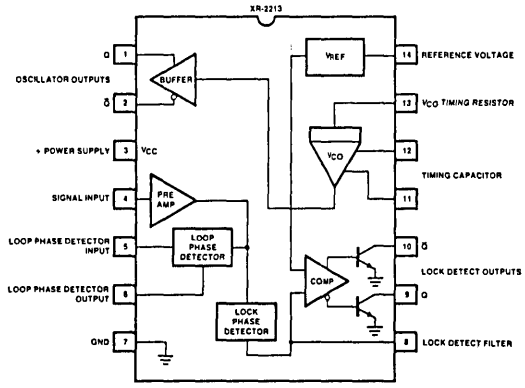
Note: All component values except R_0 can be rounded-off to nearest standard value.

Precision Phase-Locked Loop/Tone Decoder

GENERAL DESCRIPTION

The XR-2213 is a highly stable phase-locked loop (PLL) system designed for control systems and tone detection applications. It combines the features of the XR-2211 and XR-2212 into a single monolithic IC. The circuit consists of a high stability VCO, input preamplifier, phase detector, quadrature phase detector, and high gain voltage comparator. Initial VCO frequency accuracy and supply rejection are an order of magnitude better than industry standards like the 567 decoder. An on board reference contributes to reliable operation and complementary outputs aid applicability.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5 V to 15 V
Uncommitted V_{CO} Q and $\overline{Q}$ Outputs	
Wide Dynamic Input Voltage Range	2mV to 3 V RMS
Excellent V_{CO} Stability	20 PPM/°C Typ.

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2213CN	Ceramic	0°C to + 70°C
XR-2213CP	Plastic	0°C to + 70°C
XR-2213N	Ceramic	−40°C to + 85°C
XR-2213P	Plastic	−40°C to + 85°C

APPLICATIONS

Tone Detection
Frequency Synthesis
FM Detection
Tracking Filters

ABSOLUTE MAXIMUM RATINGS

Power Supply	15 V
Input Signal Level	3 V RMS
Power Dissipation	
Ceramic Package:	750 mW
Derate Above T_A = +25°C	6 mW/°C
Plastic Package:	625 mW
Derate Above T_A = +25°C	5 mW/°C
Storage Temperature	−55°C to +150°C

SYSTEM DESCRIPTION

The XR-2213 is a complete PLL system including circuitry enabling dedicated tone detection capability over a frequency range of 0.01 Hz to 300 kHz. Supply voltage may range from 4.5 V to 15 V.

The input preamplifier has a dynamic range of 2 mV to 3 Vrms. The high stability VCO, with buffered complementary outputs, typically features better than 20 ppm/°C temperature drift and 0.05%/V supply rejection. An on board voltage reference is provided, and can sink 2 mA. The complementary lock detect outputs are each capable of sinking more than 7 mA. All system parameters are independantly determined by external components.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +12V, T_A = +25°C, R_0 = 10 kΩ, C_0 = 0.1 μF, unless otherwise specified. See Figure 2 for component designation.

PARAMETERS	XR-2213/2213M			XR-2213C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL								
Supply voltage	4.5		15	4.5		15	V	
Supply current		9	11		9	12	mA	$R_O \geq 10K\Omega$
OSCILLATOR SECTION								
Frequency accuracy		±1	±3		±1		%	Deviation from $f_O = \frac{1}{R_O C_O}$ $R_1 = x$
Frequency stability								
Temperature		20	50		20		PPM/°C	
Power supply		0.05	0.5		0.05		%/V	V^+ = 12V ± 1V
Upper frequency limit	100	300			300		kHz	R_O = 8.2KΩ, C_O = 400pF
Timing resistor R_O								
operating range	5		2000				KΩ	
Recommended range	10		100				KΩ	
OSCILLATOR OUTPUT								
Voltage output								
Positive swing	9.5	11.5		2.5	4.5		V	$I_L \leq 100\mu A$
Negative swing		0.4	0.8		0.4	0.8	V	I_L = 2mA
LOOP PHASE DETECTOR SECTION								
Peak output current	±150	±200		±100	±200		μA	
Output offset current		±1			±2		μA	
Output impedance		1			1		MΩ	
Maximum swing	±4	±5		±4	±5		V	Referenced to V_{REF}
INPUT PREAMP SECTION								
Input impedance		20			20		KΩ	
Input signal to cause limiting		2	10		2		MV_{RMS}	
Internal Reference								
Voltage level	4.9	5.3	5.7	4.75	5.3	5.85	V	
Output impedance		100			100		Ω	

PRINCIPLES OF OPERATION

Figure 2 shows the standard connection for tone detection. The input signal at Pin 4 is amplified and squared-up by the preamp before it is fed to the loop phase detector. The V_{CO} Q output provides the other loop phase detector input. The V_{CO} provided in the XR-2213 is actually a current controlled oscillator, ICO. The input to the ICO, Pin 13, is internally biased at V_{REF}, with the current drawn from this pin controlling the frequency of operation of the ICO. The resistor R_0 from Pin 13 to ground will provide a constant current which will be made up of the current from Pin 13 and the current from R_1 or the phase detector output. The phase detector output, filtered by C_1, will provide a voltage to R_1, which is proportional to the phase difference between the input frequency and the ICO frequency. The relationship between this voltage and phase difference is shown in Figure 3. If the phase difference is 90°, Pin 6 will be at V_{REF}, and therefore there will be no current flow in R_1 with all of the current in R_0 coming from Pin 13. This point is defined as the center frequency, f_0, of the PLL and is calculated by:

$$*f_0 = \frac{1}{R_0 C_0}$$

If the input frequency is increased, the phase shift will decrease causing the voltage at Pin 6 to decrease. Current will now flow from Pin 13 to both R_0 and R_1, causing an increase in ICO input current and thus an output frequency increase. If the phase detector swings all the way to 0 volts, the current in R_1, will be:

$$I_{R_1} = \frac{V_{REF}}{R_1}$$

*This condition will also occur if no input signal is applied to Pin 4.

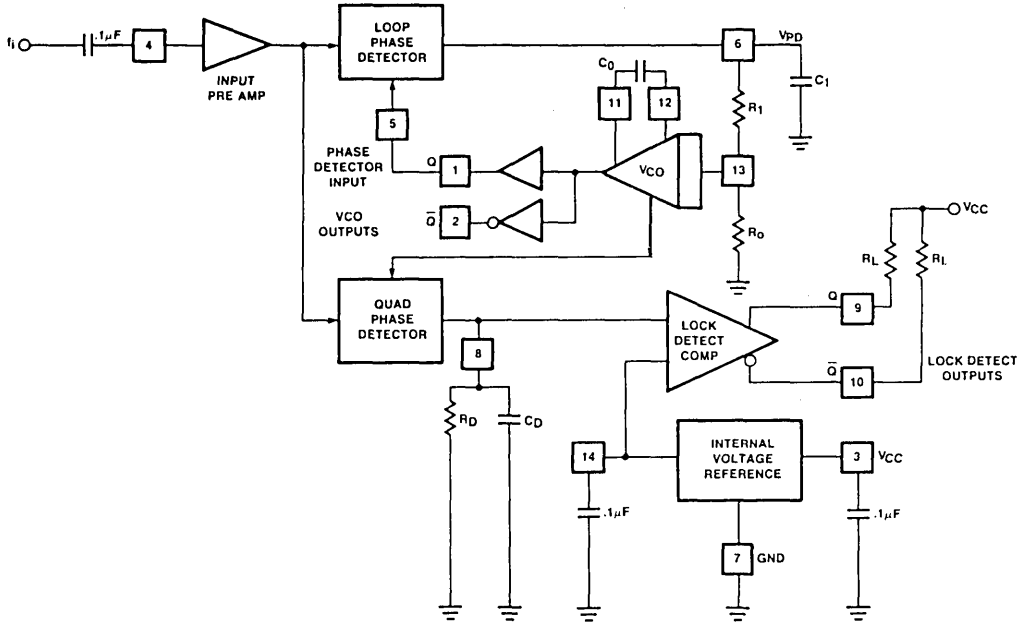


Figure 2. Generalized Circuit Connection for Tone Detection

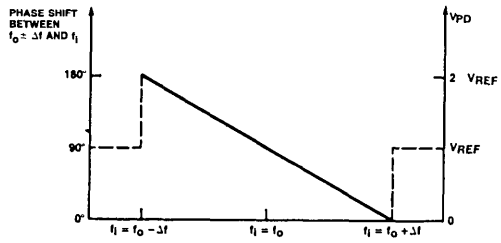


Figure 3. PLL Input/Output Relationships

At f_0, the current from Pin 13 was:

$$I_{13} = \frac{V_{REF}}{R_0}$$

If the ratio of Pin 13 current at f_0 and the change, Δ, from f_0 is written, the tracking range can be determined:

$$\frac{\Delta f_L}{f_0} = \frac{\frac{V_{REF}}{R_1}}{\frac{V_{REF}}{R_0}} = \frac{R_0}{R_1} \text{ or } \Delta f_L = \frac{R_0}{R_1}$$

If the input frequency was decreased, Δf will have the same magnitude in the opposite direction. The tracking range of the PLL will then be:

$$f_0 \pm \Delta f$$

The capture range of the PLL, which is always less than the tracking range, is described by:

$$\Delta W_C = 2\pi\Delta f_C = \sqrt{\frac{\Delta W_L}{\tau}}$$

$\tau = R_1C_1$ loop time constant
f_C = capture range

$$\Delta f_C = \sqrt{\frac{\Delta f_L}{2\pi R_1 C_1}}$$

The internal voltage reference provides a voltage equal to:

$$V_{REF} = \frac{V_{CC}}{2} - .7\ V$$

This reference can sink up to 2 mA, but source only 100 μA.

The quadrature phase detector will provide a high level, $-V_{CC}$, at Pin 8 whenever a frequency within the PLL capture range is present at Pin 4. This will drive the lock-detect outputs for a tone-detection indication. The response of the lock-detect section can be controlled by the capacitor, C_D, from Pin 8 to ground. The minimum value of C_D is calculated by the formula:

$$C_D\ (\mu F) \geq \frac{16}{f_c} \quad f_c = \text{capture range in Hz}$$

R_D = 470 K_Q is suitable for most applications.

The input to the phase detector may be directly connected to the V_{CO} output in the stand-alone connection. If the V_{CO} is not connected to the phase detector, the signal driving this pin must have sufficient amplitude to drive the pin above and below a voltage equal to V_{REF}. For low level signals, Pin 5 should be connected to V_{REF} through a 10 KΩ resistor and the signal capacitively coupled to Pin 5. The impedance into Pin 5 is approximately 100 KΩ and this pin is clamped for swings above V_{REF} +2 V.

DESIGN EQUATIONS

Refer to Figure 2 for component definitions.

1. V_{CO} center frequency, f_0:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

2. Internal voltage reference, V_{REF}:

$$V_{REF} = \frac{V_{CC}}{2} - .7 \text{ V} \quad \text{V}$$

3. Loop tracking range, $\pm \Delta f_L$:

$$\Delta f_L = f_0 \frac{R_0}{R_1} \text{ Hz}$$

4. Loop low-pass filter time constant, τ:

$$\tau = R_1 C_1 \text{ sec.}$$

5. Loop damping, ζ:

$$\zeta = \frac{1}{4}\sqrt{\frac{C_0}{C_1}}$$

6. Loop phase detector conversion gain, K_ϕ:

$$K_\phi = -\frac{2\,V_{REF}}{\pi} \frac{\text{volts}}{\text{radian}}$$

7. V_{CO} conversion gain, K_0:

$$K_0 = -\frac{1}{V_{REF}\, C_0 R_1} \frac{\text{Hz}}{\text{volt}}$$

8. Total loop gain, K_T:

$$K_T = K_0 K_\phi = \frac{4}{C_0 R_1} \text{ Hz}$$

9. Loop capture range, $\pm \Delta f_C$:

$$\Delta f_C = \sqrt{\frac{\Delta f_L}{2\pi R_1 C_1}} \text{ Hz}$$

10. Lock detect filter capacitor:

$$C_D = \frac{16}{f_C} \mu\text{F}$$

APPLICATIONS INFORMATION

Figure 2 shows the XR-C453 connected for tone detection. The input signal is capacitively coupled to Pin 4 and may range from 2 mV to 3 V RMS. The V_{CO} Q output is directly connected to the phase detector input, Pin 5. The detection bandwidth is set by the ratio of R_0 and R_1 and the loop time constant, τ. This corresponds to the capture range of the PLL. The lock-detect output, Pins 9 and 10, will give an active high and low indication when a tone in the detection bandwidth is present.

DESIGN EXAMPLE:

20 kHz tone detector with a ±1 kHz detection band.

A. Choose R_0 = 15 KΩ, 12 KΩ resistor plus 5Ω potentiometer.

B. Calculate $C_0 = \frac{1}{f_0 R_0} .0033\ \mu\text{F}$

C. Calculate $C_1 = \frac{C_0}{4} \simeq .001\ \mu\text{F}$

D. Calculate $R_1 = f_0 \frac{R_0}{\Delta f_C} = 300\ \text{K}\Omega$

E. Calculate $C_D = \frac{16}{f_C} \simeq 0.01\ \mu\text{F}$

F. Fine tune f_0 with R_X, 5 K potentiometer.

The complete circuit is shown in Figure 4.

Figure 5 shows the connection for a frequency synthesizer. Here an input frequency of 10 kHz produces an output frequency of 40 kHz. The V_{CO} center frequency, f_0, is set for 40 kHz. The divide by four will then provide the phase detector input with 10 kHz. The lock range is set to approximately 10% of f_0. For larger divider ratios, C_1 should be increased to minimize phase jitter.

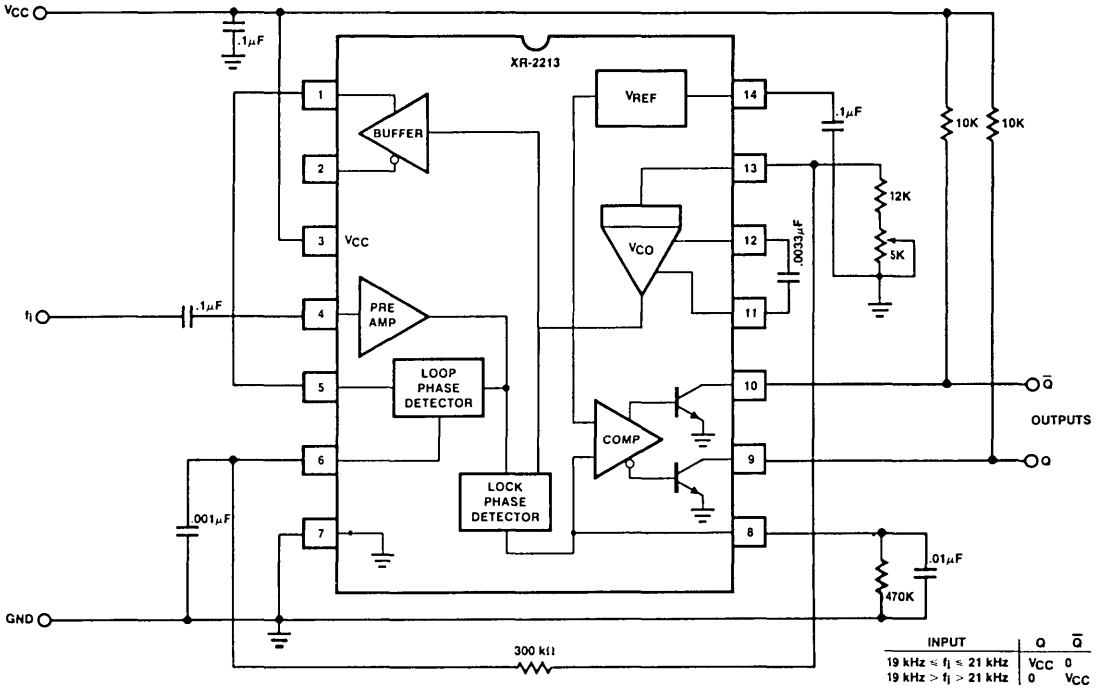


Figure 4. Tone Detector

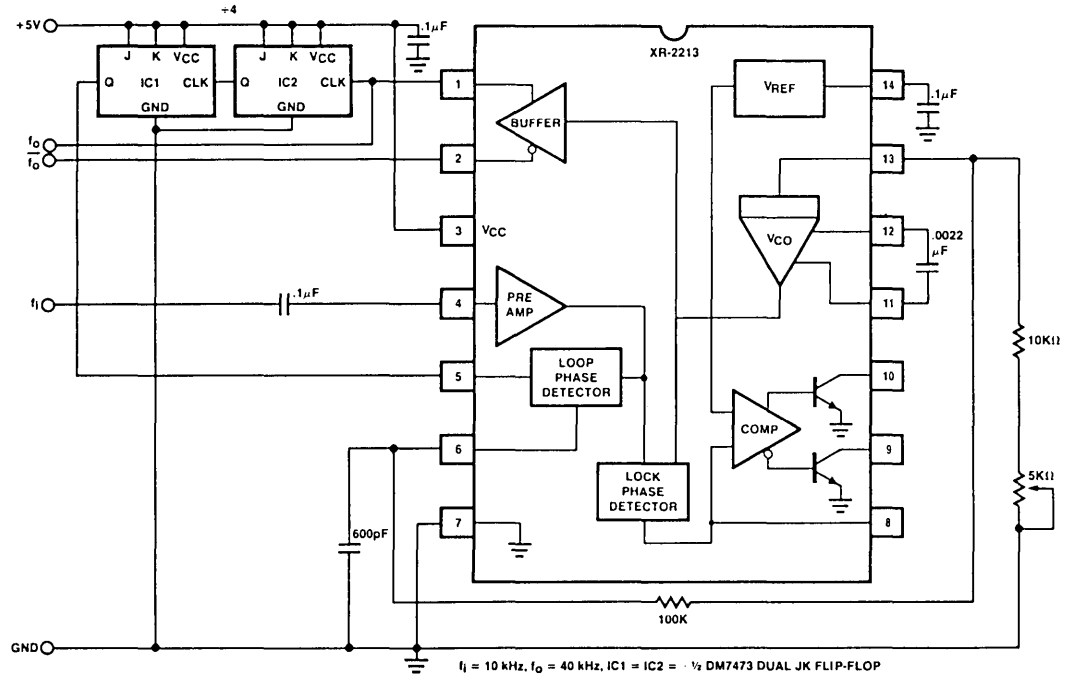


Figure 5. Frequency Synthesizer

Section 6 – Instrumentation Circuits

Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-567 is a monolithic phase-locked loop system designed for general purpose tone and frequency decoding. The circuit operates over a wide frequency band of 0.01 Hz to 500 kHz and contains a logic compatible output which can sink up to 100 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

The circuit consists of a phase detector, low-pass filter, and current-controlled oscillator which comprise the basic phase-locked loop; plus an additional low-pass filter and quadrature detector that enables the system to distinguish between the presence or absence of an input signal at the center frequency.

FEATURES

Bandwidth adjustable from 0 to 14%.
Logic compatible output with 100 mA current sinking capability
High stable center frequency.
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false signals
High rejection of out-of-band signals and noise
Frequency range adjustable over 20:1 range by external resistor.

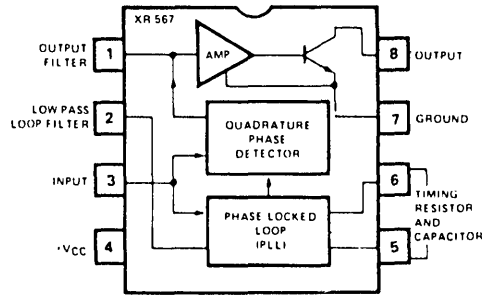
APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate Above +25°C	2.5 mW/°C
Temperature	
Operating	
XR-567M	−55°C to +125°C
XR-567CN/567CP	0°C to +70°C
Storage	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567M	Ceramic	−55°C to +125°C
XR-567CN	Ceramic	0°C to +70°C
XR-567CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-567 monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection on in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in-band signal triggers the device.

In applications requiring two or more 567-type devices, consider the XR-2567 dual tone decoder. Where center frequency accuracy and drift are critical, compare the XR-567A. Investigate employing the XR-L567 in low power circuits.

XR-567

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, T_A = 25°C, unless otherwise specified. Test circuit of Figure 2.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range	4.75		9.0	V dc	
Supply Current					
Quiescent XR-567M		6	8	mA	R_L = 20kΩ
XR-567C		7	10	mA	R_L = 20 kΩ
Activated XR-567M		11	13	mA	R_L = 20 kΩ
XR-567C		12	15	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} + 0.5	V	
CENTER FREQUENCY					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 9
0 < T_A < 70°C		±60		ppm/°C	See Figure 9
−55 < T_A < +125°C		±140		ppm/°C	See Figure 9
Supply Voltage					
XR-567M		0.5	1.0	%/V	f_o = 100 kHz
XR-567C		0.7	2.0	%/V	f_o = 100 kHz
DETECTION BANDWIDTH					
Largest Detection Bandwidth					
XR-567M	12	14	16	% of f_o	f_o = 100 kHz
XR-567C	10	14	18	% of f_o	f_o = 100 kHz
Largest Detection Bandwidth Skew					
XR-567M		1	2	% of f_o	
XR-567C		2	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
INPUT					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, f_i = f_o
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140 kHz
OUTPUT					
Output Saturation Voltage		0.2	0.4	V	I_L = 30 mA, V_{in} = 25 mV rms
		0.6	1.0	V	I_L = 100 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON-OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω

DEFINITION OF XR-567 PARAMETERS

CENTER FREQUENCY f_0

f_0 is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground f_0 can be approximated by

$$f_0 \approx \frac{1}{R_1 C_1}$$

where R_1 is in ohms and C_1 is in farads.

DETECTION BANDWIDTH (BW)

The *detection bandwidth* is the frequency range centered about f_0, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_0, can be determined by the approximation

$$BW = 1070 \sqrt{\frac{V_i}{f_0 C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance at pin 2 in μF.

LARGEST DETECTION BANDWIDTH

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

DETECTION BAND SKEW

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_0. It is defined as $(f_{max} + f_{min} - 2 f_0)/f_0$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls).

DESCRIPTION OF CIRCUIT CONTROLS

OUTPUT FILTER — C_3 (Pin 1)

Capacitor C_3 connected from pin 1 to ground forms a simple low-pass *post detection* filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3 C_3$, where R_3 (4.7 kΩ) is the internal impedance at pin 1.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, it is recommended that C_3 be $\geq 2\,C_2$, where C_2 is the loop filter capacitance at pin 2.

If the value of C_3 becomes too large, the *turn-on* or *turn-off* time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector (see Functional Block Diagram) may cause a false logic level change at the output. (Pin 8)

The average voltage (during lock) at pin 1 is a function of the inband input amplitude in accordance with the given transfer characteristic.

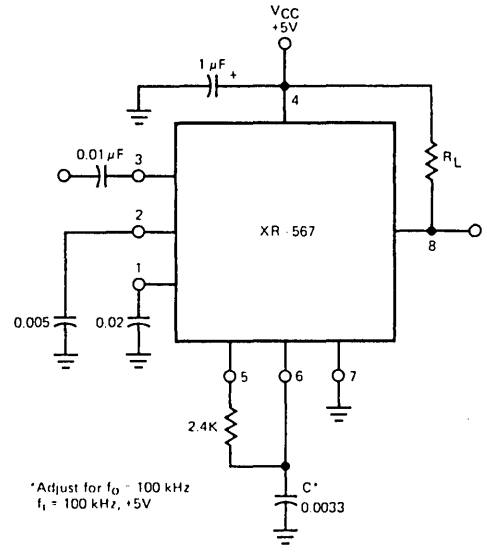


Figure 2. XR-567 Test Circuit

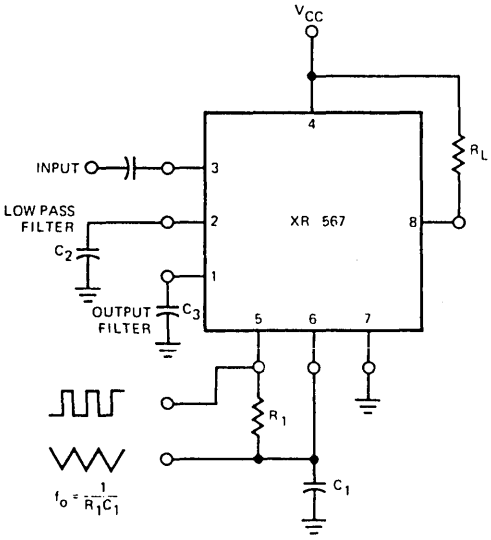


Figure 3. XR-567 Connection Diagram

TYPICAL CHARACTERISTIC CURVES

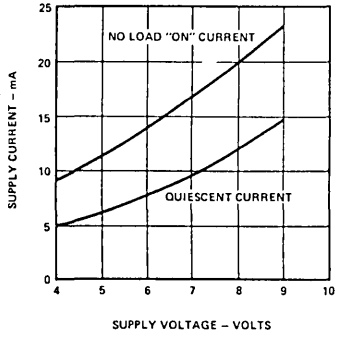


Figure 4. Supply Current Versus Supply Voltage

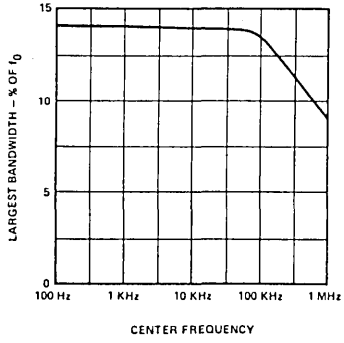


Figure 5. Largest Detection Bandwidth Versus Operating Frequency

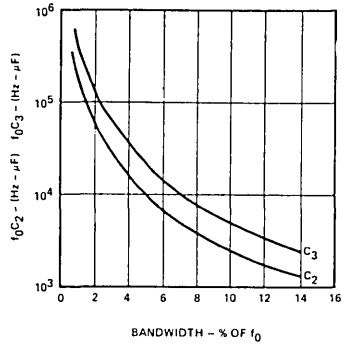


Figure 6. Detection Bandwidth as a Function of C_2 and C_3

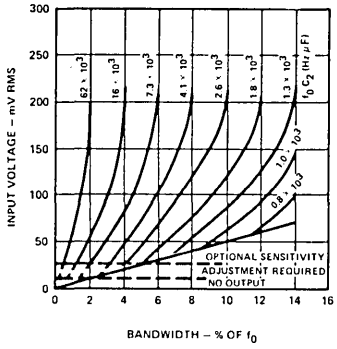


Figure 7. Bandwidth Versus Input Signal Amplitude (C_2 in μF)

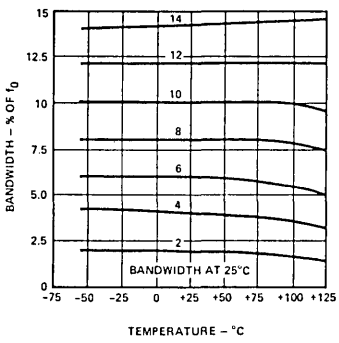


Figure 8. Bandwidth Variation with Temperature

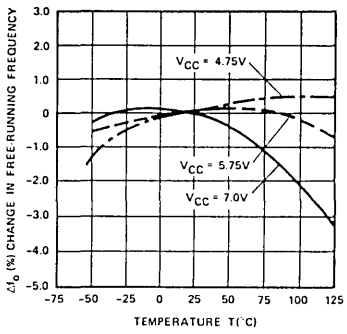


Figure 9. Frequency Drift with Temperature

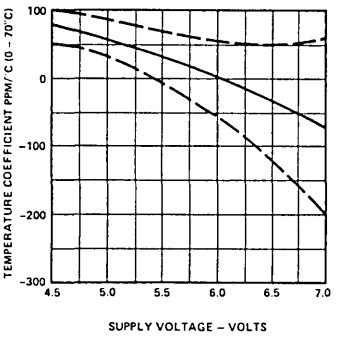


Figure 10. Temperature Coefficient of Center Frequency (Mean and S.D.)

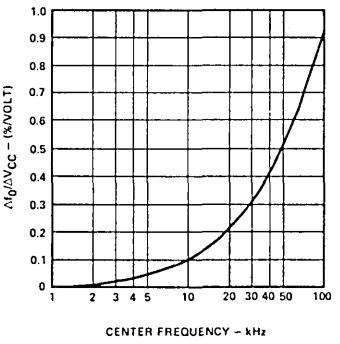


Figure 11. Power Supply Dependence of Center Frequency

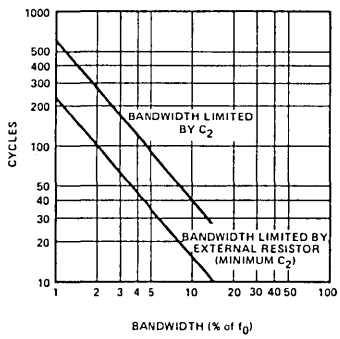


Figure 12. Greatest Number of Cycles Before Output

LOOP FILTER — C_2 (Pin 2)

Capacitor C_2 connected from pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-567. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at pin 2.

The selection of C_2 is determined by the detection bandwidth requirements, as shown in Figure 6. For additional information see section on "Definition of XR-567 Parameters".

The voltage at pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

INPUT (Pin 3)

The input signal is applied to pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 20 kΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between pins 5 and 6, and capacitor C_1 from pin 6 to ground, as shown in Figure 3.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

LOGIC OUTPUT (Pin 8)

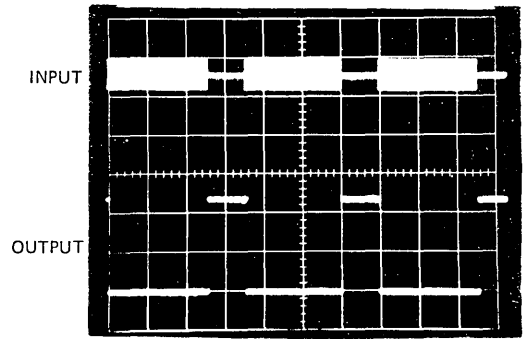
Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, "base-collector" power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from pin 8 to the positive supply.

When an in-band signal is present, the output transistor at pin 8 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤ 20 volts.

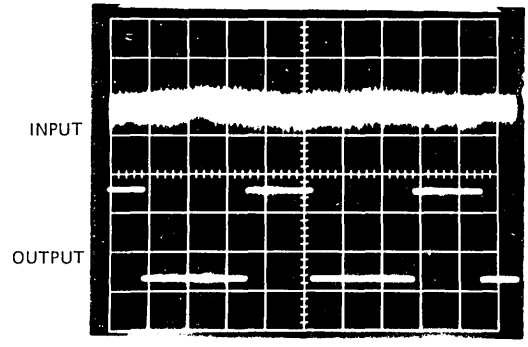
OPERATING INSTRUCTIONS

SELECTION OF EXTERNAL COMPONENTS

A typical connection diagram for the XR-567 is shown in Figure 3. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.



Response to 100 mV rms tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = –6 dB R_L = 100 ohms

Noise Bandwidth = 140 Hz

Figure 13. Typical Response

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2kΩ ≤ R_1 ≤ 20 kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 7. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires V_i > 200 mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_oC_2 product.

3. Capacitor C_3 sets the ·nd edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value of C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

PRINCIPLE OF OPERATION

The XR-567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature AM detector, a voltage comparator, and an output logic driver. The four sections are internally interconnected as shown in Figure 1.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic driver is a "bare collector" transistor stage capable of switching 100 mA loads.

The logic output at pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at pin 8 goes to a "low" state.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R_1 and C_1 connected to pins 5 and 6, as shown in Figure 3. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2; and the output response speed is controlled by the output filter capacitor, C_3.

OPTIONAL CONTROLS

PROGRAMMING

Varying the value of resistor R_1 and/or capacitor C_1 will change the center frequency. The value of R_1 can be changed either mechanically or by solid state switches. Additional C_1 capacitors can be added by grounding them through saturated npn transistors.

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud.

$$C_2 = \frac{130}{f_o},\ C_3 = \frac{260}{f_o}\ \mu F$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 14 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

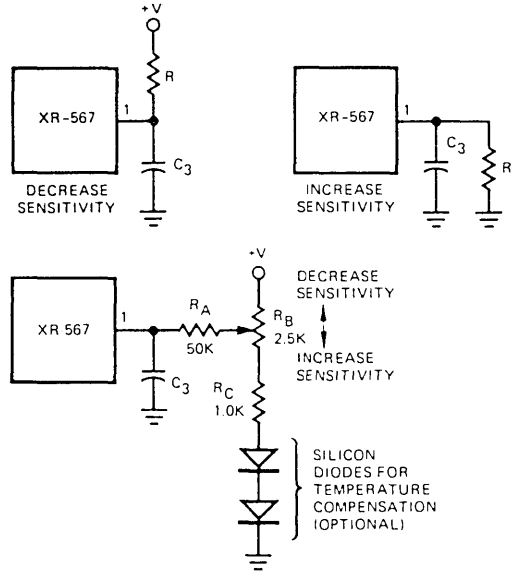


Figure 14. Optional Sensitivity Connections

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (pin 1) or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 15. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

SKEW ADJUSTMENT

The circuits shown in Figure 16 can be used to change the position of the detection band (capture range) with-

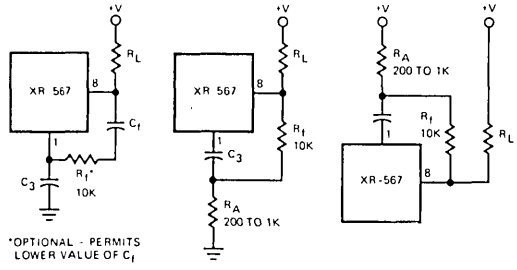


Figure 15. Methods of Reducing Chatter

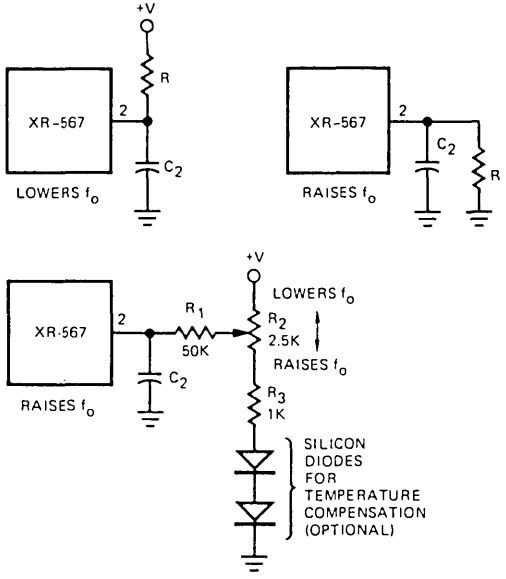


Figure 16. Connections to Reposition Detection Band

in the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

OUTPUT LATCHING

In order to latch the output of the XR-567 "on" after a signal is received, it is necessary to include a feedback resistor around the output stage, between pin 8 and pin 1, as shown in Figure 17. Pin 1 is pulled up to unlatch the output stage.

BANDWIDTH REDUCTION

The bandwidth of the XR-567 can be reduced by either increasing capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 18 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. The reduced impedance level at pin 2 will require a larger value of C_2 for a given cut-off frequency.

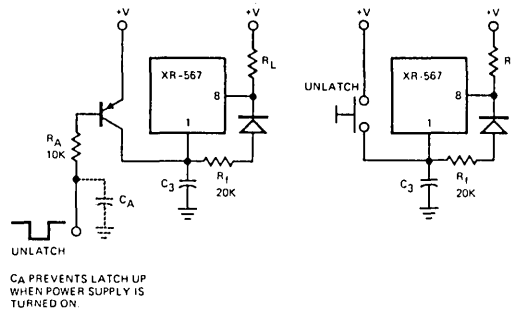
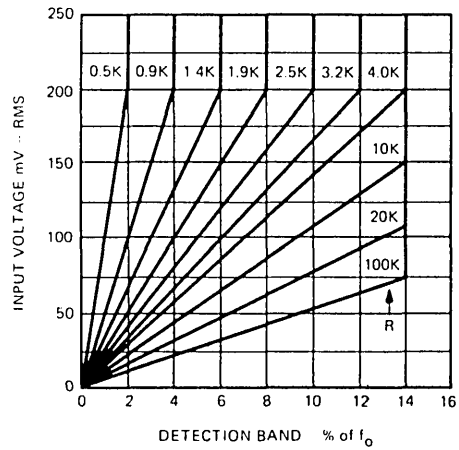
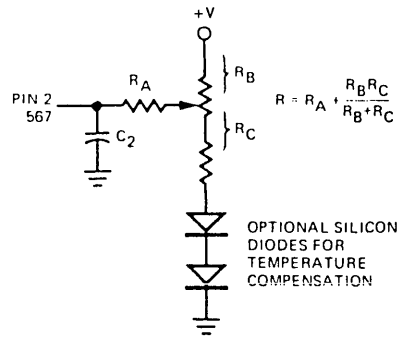


Figure 17. Output Latching





$$\frac{130}{f_o}\left(\frac{10K + R}{R}\right) < C_2 < \frac{1300}{f_o}\left(\frac{10K + R}{R}\right)$$

NOTE: ADJUST CONTROL FOR SYMMETRY OF DETECTION BAND EDGES ABOUT f_o.

Figure 18. Bandwidth Reduction

PRECAUTIONS

1. The XR-567 will lock on signals near (2n + 1) f_0 and produce an output for signals near (4n + 1) f_0, for n = 0,1,2 - etc. Signals at 5 f_0 and 9 f_0 can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-567 in a reduced bandwidth mode of operation at input levels less than 200 mV rms results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 12.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-567 in the high input level mode, above 200 mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit components from subharmonic signals so that the circuit becomes sensitive to signals at $f_0/3$, $f_0/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

ADDITIONAL APPLICATIONS

DUAL TIME CONSTANT TONE DECODER

For some applications it is important to have a tone decoder with narrow bandwidth and fast response time. This can be accomplished by the dual time constant tone decoder circuit shown in Figure 19. The circuit has two low-pass loop filter capacitors, C_2 and C'_2. With no input signal present, the output at pin 8 is high, transistor Q_1 is off, and C'_2 is switched out of the circuit. Thus the loop low-pass filter is comprised of C_2, which can be kept as small as possible for minimum response time.

When an in-band signal is detected, the output at pin 8 will go low, Q_1 will turn on, and capacitor C'_2 will be switched in parallel with capacitor C_2. The low-pass filter capacitance will then be $C_2 + C'_2$. The value of C'_2 can be quite large in order to achieve narrow bandwidth. Notice that during the time that no input signal is being received, the bandwidth is determined by capacitor C_2.

NARROW BAND FM DEMODULATOR WITH CARRIER DETECT

For FM demodulation applications where the bandwidth is less than 10% of the carrier frequency, an XR-567

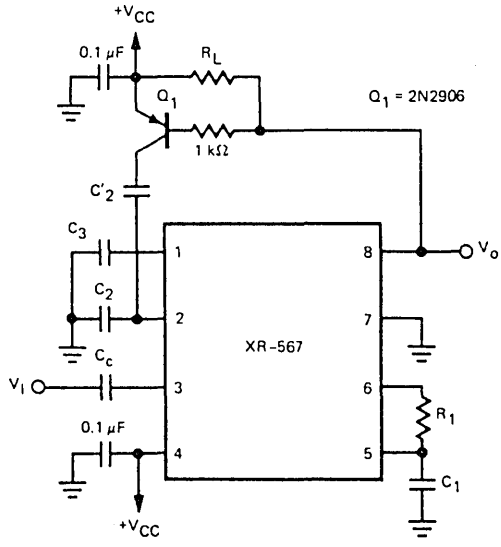


Figure 19. Dual Time Constant Tone Decoder

can be used to detect the presence of the carrier signal. The output of the XR-567 is used to turn off the FM demodulator when no carrier is present, thus acting as a squelch. In the circuit shown, an XR-215 FM demodulator is used because of its wide dynamic range, high signal/noise ratio and low distortion. The XR-567 will detect the presence of a carrier at frequencies up to 500 kHz.

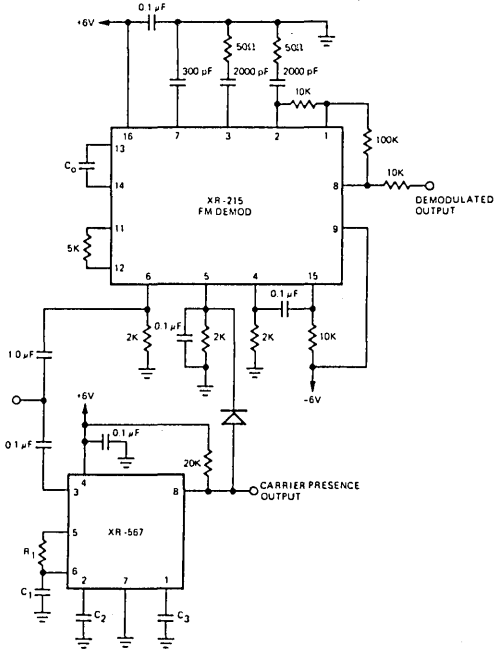


Figure 20. Narrow Band FM Demodulator with Carrier Detect

DUAL TONE DECODER

In dual tone communication systems, information is transmitted by the simultaneous presence of two separate tones at the input. In such applications two XR-567 units can be connected in parallel, as shown in Figure 21 to form a dual tone decoder. The resistor and capacitor values of each decoder are selected to provide the desired center frequencies and bandwidth requirements.

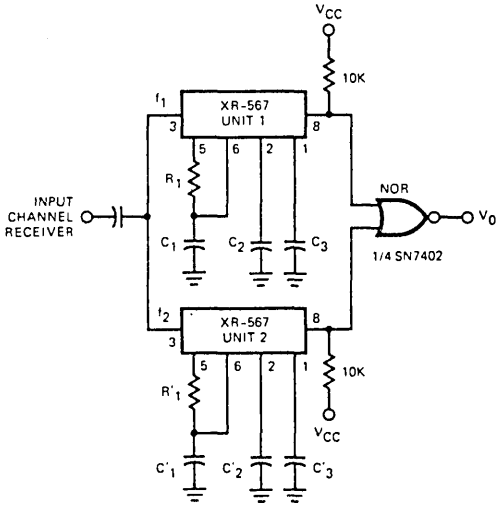


Figure 21. Dual Tone Decoder

PRECISION OSCILLATOR

The current-controlled oscillator (CCO) section of the XR-567 provides two basic output waveforms as shown in Figure 22. The squarewave is obtained from pin 5, and the exponential ramp from pin 6. The relative phase relationships of the waveforms are also provided in the figure. In addition to being used as a general purpose oscillator or clock generator, the CCO can also be used for any of the following special purpose oscillator applications:

1. **High-Current Oscillator**

   The oscillator output of the XR-567 can be amplified using the output amplifier and high-current logic output available at pin 8. In this manner, the circuit can switch 100 mA load currents without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 23. The oscillator frequency can be modulated over ±6% in frequency by applying a control voltage to pin 2.

2. **Oscillator with Quadrature Outputs**

   Using the circuit connection of Figure 24 the XR-567 can function as a precision oscillator with two separate squarewave outputs (at pins 5 and 8, respectively) that are at nearly quadrature phase with each other. Due to the internal biasing arrangement the actual phase shift between the two outputs is typically 80°.

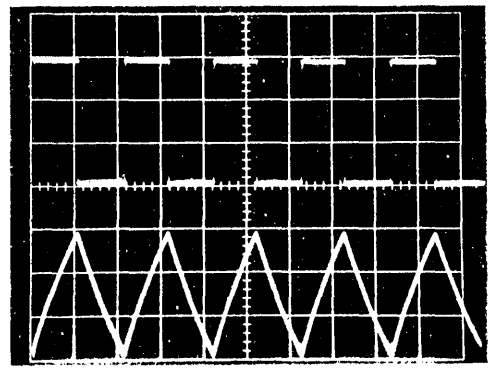


Figure 22. Oscillator Output Waveform Available From CCO Section.
Top: Square Wave Output at Pin 5:
Amplitude = (V+ −1.4V), pp.,
Avg. Value = V+/2
Bottom: Exponential Triangle Wave at Pin 6:
Amplitude = 1V pp., Avg. Value = V+/2

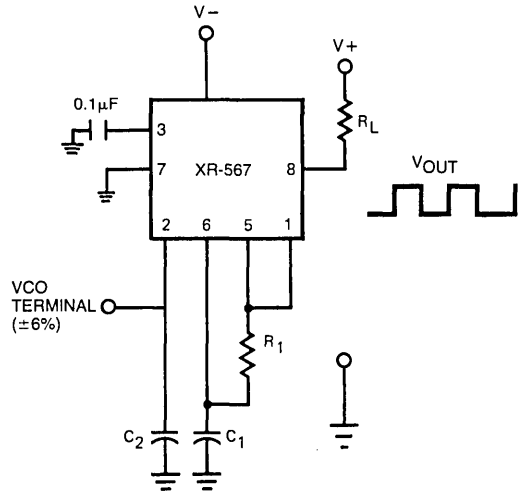


Figure 23. Precision Oscillator to Switch 100 mA Loads

3. **Oscillator with Frequency Doubled Output**

   The CCO frequency can be doubled by applying a portion of the squarewave output at pin 5 back to the input at pin 3, as shown in Figure 25. In this manner, the quadrature detector functions as a frequency doubler and produces an output of 2 f_0 at pin 8.

FSK DECODING

XR-567 can be used as a low speed FSK demodulator. In this application the center frequency is set to one of

the input frequencies, and the bandwidth is adjusted to leave the second frequency outside the detection band. When the input signal is frequency keyed between the *in-band* signal and the *out-band* signal, the logic state of the output at pin 8 is reversed. Figure 26 shows the FSK input ($f_2 = 3\ f_1$) and the demodulated output signals, with $f_0 = f_2 = 1$ kHz. The circuit can handle data rates up to $f_0/10$ baud.

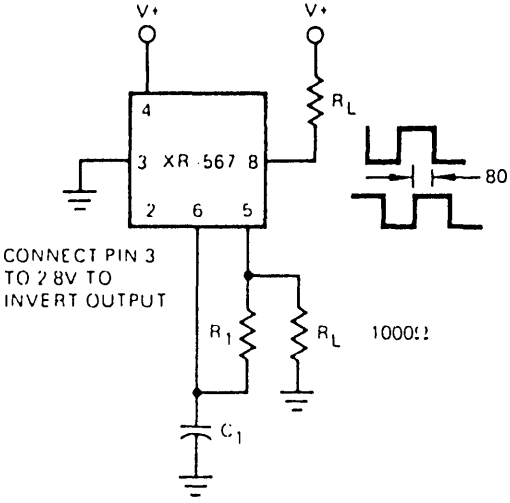


Figure 24. Oscillator with Quadrature Output

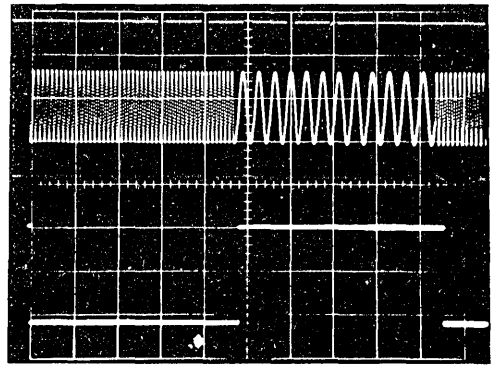
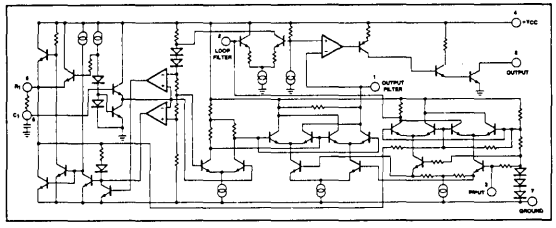


Figure 26. Input and Output Waveforms for FSK Decoding
Top: Input FSK Signal ($f_2 = 3f_1$)
Bottom: Demodulated Output



EQUIVALENT SCHEMATIC DIAGRAM

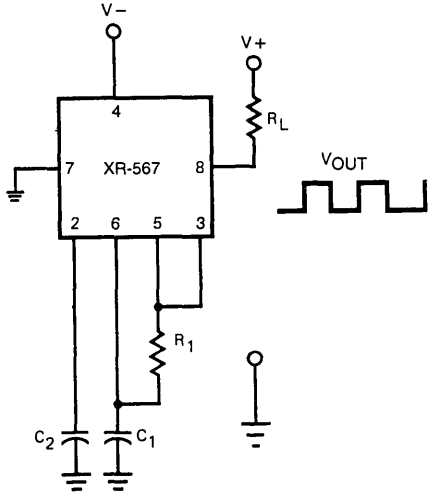


Figure 25. Oscillator with Double Frequency Output

Precision Tone Decoder

GENERAL DESCRIPTION

The XR-567A provides all the necessary circuitry for constructing a variety of tone detectors and frequency decoders. Phase-locked loop circuit techniques are used to provide operation from 0.01 Hz tp 500 kHz. The circuit also features an input preamp, a high-current logic output, and programmable output delay.

The XR-567A, available in an 8-Pin DIL package, is designed to offer improved frequency accuracy and drift characteristics over the standard industry 567. These changes offer improved overall circuit performance, while reducing initial circuit adjustments.

FEATURES

Programmable Detection Bandwidth	0% to 14%
Logic Output	100 mA
Wide Center Frequency Range	0.01 Hz to 500 kHz
High Rejection of Out-of-Band Signals and Noise	
Direct Replacement for standard 567	
Inherent immunity to out-of-band signals & noise	

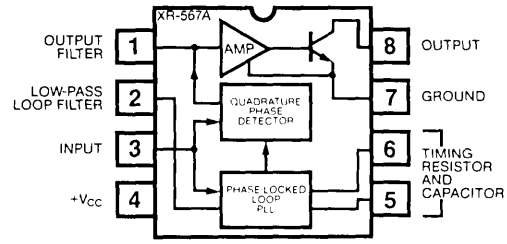
APPLICATIONS

Tone Detection
Touch-Tone® Decoding
Communications Paging
Ultrasonic Remote Control
Precision Oscillator
Wireless Intercom
Carrier-Tone Transceiver
FSK Demodulation
Dual Time Constant Tone Detector

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate above 25°C	2.5 mW/°C
Operating Temperature Range	
XR-567AM	−55°C to +125°C
XR-567ACN/ACP	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-567AM	Ceramic	−55°C to +125°C
XR-567ACN	Ceramic	0°C to +70°C
XR-567ACP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-567A is an improved version of the popular 567 tone decoder. Center frequency accuracy is guaranteed by design modifications and testing to 5%, and is typically better than 2%. Temperature drift of the center frequency is also improved. Thus, in most applications, no trimming is required.

The XR-567A monolithic tone decoder consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output capable of sinking 100 mA.

The input signal is applied to Pin 3 (20 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6 and can typically reach 500 kHz. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accompliished with a capacitor on Pin 2; bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 4 is $+V_{CC}$ (4.75 to 9V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is open collector output, pulling low when an in band signal triggers the device.

XR-567A

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25° C, unless otherwise specified.

PARAMETER:	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range	4.75		9.0	Vdc	
Supply Current					
Quiescent XR-567AM		6	8	mA	R_L = 20 kΩ
Quiescent XR-567AC		7	10	mA	R_L = 20 kΩ
Activated XR-567AM		11	13	mA	R_L = 20 kΩ
Activated XR-567AC		12	15	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC} +0.5	V	
CENTER FREQUENCY					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	
0 < T_A < 70°C		±60		ppm/°C	
−55 < T_A < +125°C		±120		ppm/°C	
Supply Voltage					
XR-567AM		0.5	1.0	%/V	f_o = 100 kHz
XR-567AC		0.7	2.0	%/V	f_o = 100 kHz
Initial Accuracy		±2.0	±5.0	%	f_o = 80 kHz
Center Frequency		1.06			f = 1/Rc
DETECTION BANDWIDTH					
Largest Detection Bandwidth					
XR-567AM	12	14	16	% of f_o	f_o = 100 kHz
XR-567AC	10	14	18	% of f_o	f_o = 100 kHz
Largest Detection Bandwidth Skew					
XR-567AM		1	2	% of f_o	
XR-567AC		2	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±1	±2	%/V	V_{in} = 300 mV rms
INPUT					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, f_i = f_o
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	B_n = 140 kHz
OUTPUT					
Output Saturation Voltage		0.2	0.4	V	I_L = 30 mA, V_{in} = 25 mV rms
		0.6	1.0	V	I_L = 100 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON/OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω

6

Micropower Tone Decoder

GENERAL DESCRIPTION

The XR-L567 is a micropower phase-locked loop (PLL) circuit designed for general purpose tone and frequency decoding. In applications requiring very low power dissipation, the XR-L567 can replace the popular 567-type decoder with only minor component value changes. The XR-L567 offers approximately 1/10th the power dissipation of the conventional 567-type tone decoder, without sacrificing its key features such as the oscillator stability, frequency selectivity, and detection threshold. Typical quiescent power dissipation is less than 4 mW at 5 volts. It operates over a wide frequency band of 0.01 Hz to 60 kHz and contains a logic compatible output which can sink up to 10 milliamps of load current. The bandwidth, center frequency, and output delay are independently determined by the selection of four external components.

FEATURES

Very Low Power Dissipation (≈4 mW at 5V).
Bandwidth Adjustable from 0 to 14%.
Logic Compatible Output with 10 mA Current Sinking Capability.
Highly Stable Center Frequency.
Center Frequency Adjustable from 0.01 Hz to 60 kHz.
Inherent Immunity to False Signals.
High Rejection of Out-of-Band Signals and Noise.
Frequency Range Adjustable Over 20:1 Range by External Resistor.

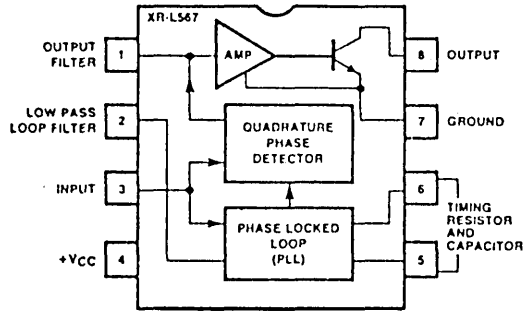
APPLICATIONS

Battery-Operated Tone Detection
Touch-Tone® Decoding
Sequential Tone Decoding
Communications Paging
Ultrasonic Remote-Control
Telemetry Decoding

ABSOLUTE MAXIMUM RATINGS

Power Supply	10 volts
Power Dissipation (package limitation)	
Ceramic Package	385 mW
Plastic Package	300 mW
Derate Above +25°C	2.5 mW/°C
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-L567CN	Ceramic	0°C to +70°C
XR-L567CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-L567 monolithic circuit consists of a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase-locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. The device has a normally high open collector output.

The input signal is applied to Pin 3 (100 kΩ nominal input resistance). Free running frequency is controlled by an RC network at Pins 5 and 6. A capacitor on Pin 1 serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 2; band-width and skew are also dependant upon the circuitry here. Pin 4 is $+V_{CC}$ (4.75 to 8V nominal, 10V maximum); Pin 7 is ground; and Pin 8 is the open collector output, pulling low when an in-band signal triggers the device.

The XR-L567 is pin-for-pin compatible with the standard XR-567-type decoder. Internal resistors have been scaled up by a factor of ten, thereby reducing power dissipation and allowing use of smaller capacitors for the same applications compared to the standard part. This scaling also lowers maximum device center frequency and load current sinking capabilities.

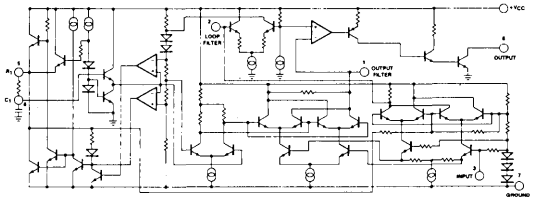
XR-L567

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V. T_A = 25°C, unless otherwise specified. Test Circuit of Figure 1.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
General					
Supply Voltage Range	4.75		8.0	V	
Supply Current					
Quiescent		0.6	1.0	mA	R_L = 20 kΩ
Activated		0.8	1.4	mA	R_L = 20 kΩ
Center Frequency					
Highest Center Frequency	10	60		kHz	
Center Frequency Drift					
Temperature T_A = 25°C		−35		ppm/°C	See Figures 10 and 11
0 < T_A < 70°C		−150		ppm/°C	See Figures 10 and 11
Supply Voltage		0.5	3.0	%/V	f_o = 10 kHz, V_{CC} = 5.25 ± 0.5V
Detection Bandwidth					
Largest Detection Bandwidth	10	14	18	% of f_o	f_o = 10 kHz
Largest Detection Bandwidth Skew		2	3	% of f_o	See Figure 13 for Definition
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
Inputs					
Input Resistance		100		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 10 mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 10 mA, f_i = f_o
Greatest Simultaneous Outband					
Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband					
Noise Ratio		−6		dB	B_n = 140 kHz
Outputs					
Output Saturation Voltage		0.2	0.4	V	I_L = 2 mA, V_{in} = 25 mV rms
		0.3	0.6	V	I_L = 10 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest On/Off Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 1 kΩ
Output Fall Time		30		ns	R_L = 1 kΩ

EQUIVALENT SCHEMATIC DIAGRAM



PRINCIPLES OF OPERATION

The XR-L567 is a frequency selective tone decoder system based on the phase-locked loop (PLL) principle. The system is comprised of a phase-locked loop, a quadrature am detector, a voltage comparator, and an output logic driver.

When an input tone is present within the pass-band of the circuit, the PLL synchronizes or "locks" on the input signal. The quadrature detector serves as a lock indicator: when the PLL is locked on an input signal, the dc voltage at the output of the detector is shifted. This dc level shift is then converted to an output logic pulse by the amplifier and logic driver. The logic output at Pin 8 is an "open-collector" NPN transistor stage capable of switching 10 mA current loads.

The logic output at Pin 8 is normally in a "high" state, until a tone that is within the capture range of the decoder is present at the input. When the decoder is locked on an input signal, the logic output at Pin 8 goes to a "low" state.

Figure 3 shows the typical output response of the circuit for a tone-burst applied to the input, within the detection band.

The center frequency of the detector is set by the free-running frequency of the current-controlled oscillator in the PLL. This free-running frequency, f_o, is determined by the selection of R_1 and C_1 connected to Pins 5 and 6, as shown in Figure 2. The detection bandwidth is determined by the size of the PLL filter capacitor, C_2 (see Figure 10); and the output response speed is controlled by the output filter capacitor, C_3.

DEFINITION OF DEVICE PARAMETERS

Center Frequency f_0

f_o is the free-running frequency of the current-controlled oscillator with no input signal. It is determined by resistor R_1 between Pins 5 and 6, and capacitor C_1 from Pin 6 to ground. f_o can be approximated by

$$f_o \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

Detection Bandwidth (BW)

The largest *detection bandwidth* is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a logic zero state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass loop filter at Pin 2. Typical dependence of detection bandwidth on the filter capacitance and the input signal amplitude is shown in Figures 10 and 11, or may be calculated by the approximation

$$BW\ (\%) \approx 338 \sqrt{\frac{V_i\ (RMS)}{f_o(Hz) \cdot C_2\ (\mu F)}}$$

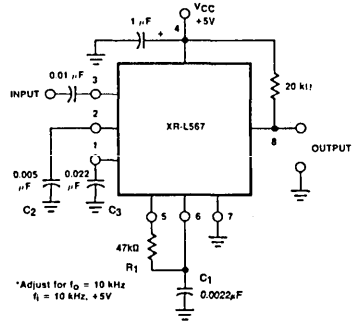


Figure 1. XR-L567 Test Circuit

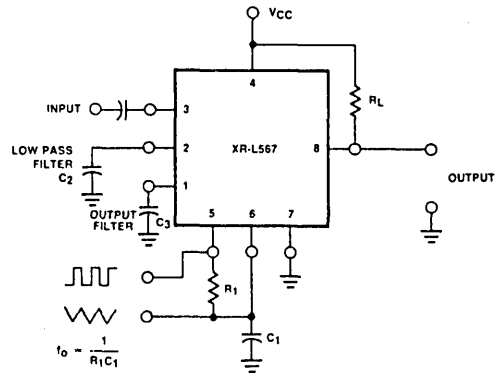


Figure 2. XR-L567 Generalized Connection Diagram

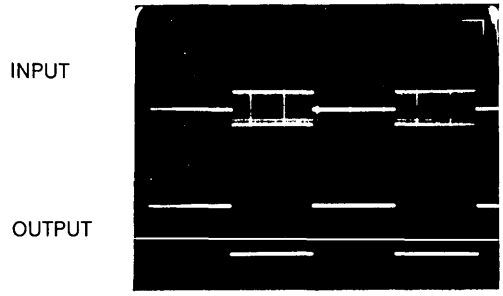
Largest Detection Bandwidth

The largest detection bandwidth is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero stage at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

Detection Band Skew

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_o. This parameter is graphically illustrated in Figure 4. In the figure, f_{min} and f_{max} correspond to the lower and the upper ends of the largest detection band, and f_1 corresponds to the apparent center of the detection band, and is defined as the arithmetic average of f_{min} and f_{max} and f_o is the free-running frequency of the XR-L567 oscillator section. The bandwidth skew, Δf_x, is the difference between these frequencies. Normalized to f_o, this bandwidth skew can be expressed as:

$$\text{Bandwidth Skew} = \frac{\Delta f_x}{f_o} = \frac{(f_{max} + f_{min} - 2f_o)}{2f_o}$$



Response to 100 mV rms tone burst.
R_L = 1K ohms

Figure 3. Typical Output Response to 100 mV Input Tone-Burst

If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

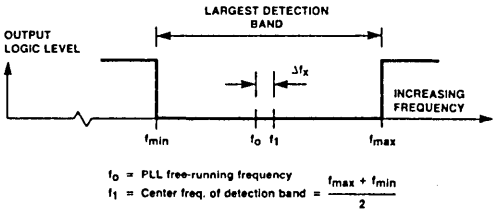


Figure 4. Definition of Bandwidth Skew

DESCRIPTION OF CIRCUIT CONTROLS

Input (Pin 3)

The input signal is applied to Pin 3 through a coupling capacitor. This terminal is internally biased at a dc level 2 volts above ground, and has an input impedance level of approximately 100 kΩ.

Timing Resistor R_1 and Capacitor C_1 (Pins 5 and 6)

The center frequency of the decoder is set by resistor R_1 between Pins 5 and 6, and capacitor C_1 from Pin 6 to ground, as shown in Figure 2.

Pin 5 is the oscillator squarewave output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 5 kΩ load may be driven from this point. The voltage at Pin 6 is an exponential triangle waveform with a peak-to-peak amplitude of ≈ (V_{CC} – 1.3)/3.5 volts and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 6 to avoid disturbing the temperature stability or duty cycle of the oscillator.

Loop Filter—C_2 (Pin 2)

Capacitor C_2 connected from Pin 2 to ground serves as a single pole, low-pass filter for the PLL portion of the XR-L567. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (100 kΩ) is the impedance at Pin 2.

The selection of C_2 is determined by the detection bandwidth requirements, as shown in Figure 10. For additional information see section on "Definition of Device Parameters."

The voltage at Pin 2, the phase detector output, is a linear function of frequency over the range of 0.95 f_o to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

Output Filter—C_3 (Pin 1)

Capacitor C_3 connected from Pin 1 to ground forms a simple low-pass post *detection* filter to eliminate spurious outputs due to out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (47 kΩ) is the internal impedance at Pin 1.

If the value of C_3 becomes too large, the *turn-on* or *turn-off* time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, the delay may be desirable as a means of suppressing spurious outputs. Conversely, if the value of C_3 is too small, the beat rate at the output of the quadrature detector may cause a false logic level change at the output (Pin 8).

The average voltage (during lock) at Pin 1 is a function of the in-band input amplitude in accordance with the given transfer characteristic.

Logic Output (Pin 8)

Terminal 8 provides a binary logic output when an input signal is present within the pass-band of the decoder. The logic output is an uncommitted, open-collector power transistor capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from Pin 8 to the positive supply.

When an in-band signal is present the output transistor at Pin 8 saturates with a collector voltage of less than 0.6V at full rated output current of 10 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+, higher than the V_{CC} supply. For safe operation, V+ ≤15 volts.

OPERATING INSTRUCTIONS

Selection of External Components

A typical connection diagram for the XR-L567 is shown in Figure 2. For most applications, the following procedure will be sufficient for determination of the external components R_1, C_1, C_2, and C_3.

1. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 20 kΩ ≤ R_1 ≤ 200 kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

2. Low-pass capacitor, C_2, can be determined from the Bandwidth versus Input Signal Amplitude graph of Figure 10. One approach is to select an area of operation from the graph, and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires V_i > 200 mV rms. Then, as noted on the graph, bandwidth will be controlled solely by the f_oC_2 product.

3. Capacitor C_3 sets the band edge of the low-pass filter which attenuates frequencies outside of the detection band and thereby eliminates spurious outputs. If C_3 is too small, frequencies adjacent to the

detection band may switch the output stage off and on at the beat frequency, or the output may pulse off and on during the turn-on transient. A typical minimum value for C_3 is 2 C_2.

Conversely, if C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage across C_3 passes the threshold value.

Precautions

1. The XR-L567 will lock on signals near (2n + 1) f_o and produce an output for signals near (4n + 1) f_o, for n = 0,1,2—etc. Signals at 5 f_o and 9 f_o can cause an unwanted output and should, therefore, be attenuated before reaching the input of the circuit.

2. Operating the XR-L567 in a reduced bandwidth mode of operation at input levels less than 200 mV rms results in maximum immunity to noise and out-band signals. Decreased loop damping, however, causes the worst-case lock-up time to increase, as shown by the graph of Figure 13.

3. Bandwidth variations due to changes in the in-band signal amplitude can be eliminated by operating the XR-L567 in the high input level mode, above 200 mV. The input stage is then limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. In addition, the limited input stage will create in-band components from subharmonic signals so that the circuit becomes sensitive to signals at $f_o/3$, $f_o/5$ etc.

4. Care should be exercised in lead routing and lead lengths should be kept as short as possible. Power supply leads should be properly bypassed close to the integrated circuit and grounding paths should be carefully determined to avoid ground loops and undesirable voltage variations. In addition, circuits requiring heavy load currents should be provided by a separate power supply, or filter capacitors increased to minimize supply voltage variations.

OPTIONAL CONTROLS

Programming

Varying the value of resistor R_1 and/or capacitor C_1 will change the center frequency. The value of R_1 can be changed either mechanically or by solid state switches. Additional C_1 capacitors can be added by grounding them through saturated npn transistors.

Speed of Response

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transients becomes greater. Thus maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies where f_o is Hz.

$$C_2 = \frac{13}{f_o}, C_3 = \frac{26}{f_o} \mu F$$

The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_o/10$ baud. In situations where minimum turn-off is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 5 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

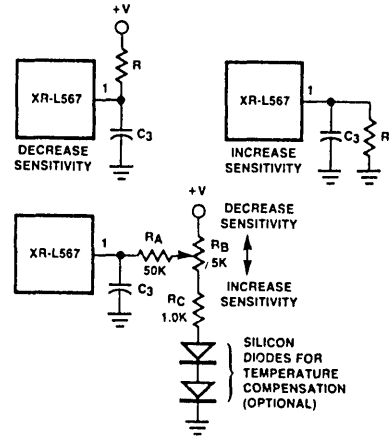


Figure 5. Adjustable Sensitivity Connections

Chatter

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, logic may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input (Pin 1) or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

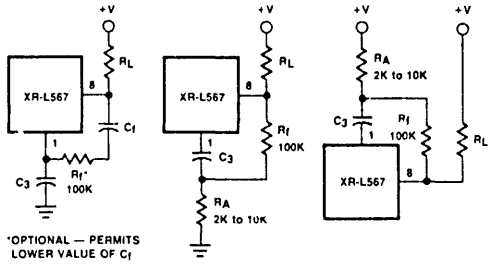


Figure 6. Methods of Reducing Chatter

Skew Adjustment

The circuits shown in Figure 7 can be used to change the position of the detection band (capture range) within the largest detection band (lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

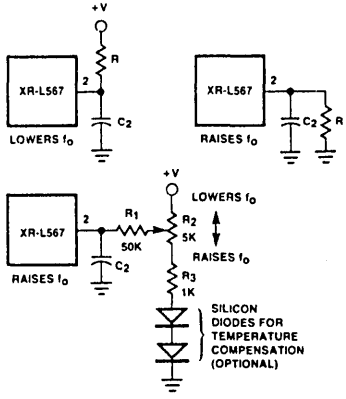


Figure 7. Detection Band Skew Adjustment

CHARACTERISTIC CURVES

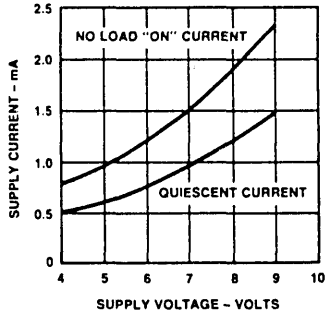


Figure 8. Supply Current Versus Supply Voltage

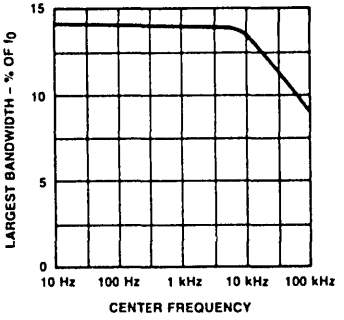


Figure 9. Largest Detection Bandwidth Versus Operating Frequency

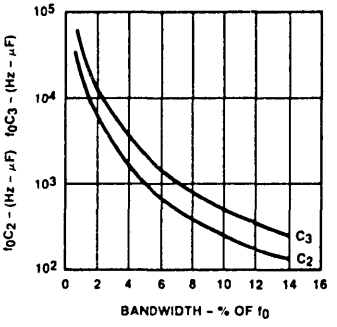


Figure 10. Detection Bandwidth as a Function of C_2 and C_3

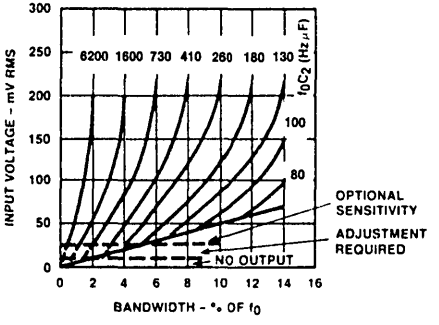


Figure 11. Bandwidth Versus Input Signal Amplitude (C_2 in μF)

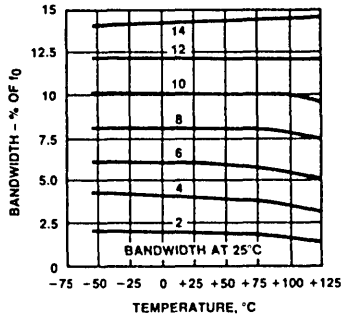


Figure 12. Bandwidth Variation With Temperature

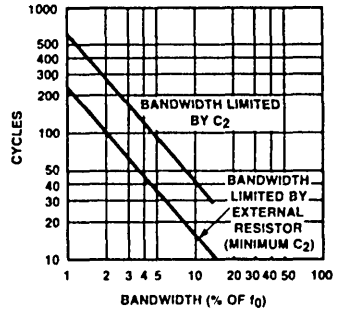


Figure 13. Greatest Number of Cycles Before Output

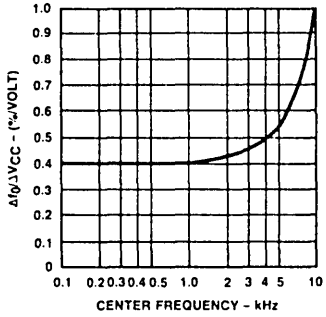


Figure 14. Power Supply Dependence of Center Frequency

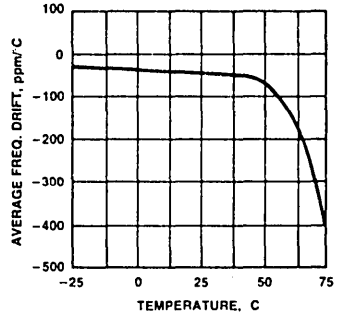


Figure 15. Typical Center Frequency Drift With Temperature (V^+ = 5V, R_1 = 80 kΩ, f_0 = 1 kHz)

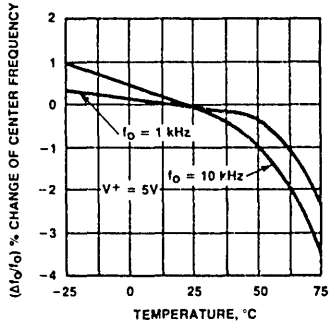


Figure 16. Typical Frequency Drift as a Function of Temperature

Dual Monolithic Tone Decoder

GENERAL DESCRIPTION

The XR-2567 is a dual monolithic tone decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone decoder packages.

The XR-2567 operates over a frequency range of 0.01 Hz to 500 kHz. Supply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic compatible output that can sink more than 100 mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free-running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

FEATURES

Replaces two 567-type decoders
Excellent temperature tracking between decoders
Bandwidth adjustable from 0 to 14%
Logic compatible outputs with 100 mA sink capability
Center frequency matching (1% typ.)
Center frequency adjustable from 0.01 Hz to 500 kHz
Inherent immunity to false triggering
Frequency range adjustable over 20:1 range by external resistor.

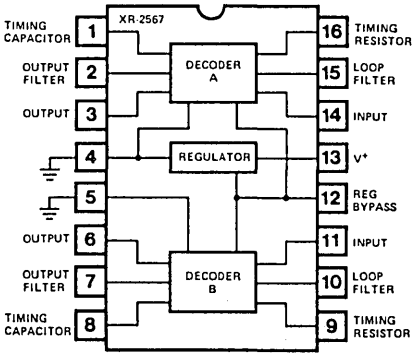
APPLICATIONS

Touch-Tone® Decoding
Sequential Tone Decoding
Dual-Tone Decoding/ Encoding
Communications Paging
Ultrasonic Remote-Control and Monitoring
Full-Duplex Carrier-Tone Transceiver
Wireless Intercom
Dual Precision Oscillator
FSK Generation and Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	
With Internal Regulator	14V
Without Regulator (Pins 12 and 13 shorted)	10V
Power Dissipation	
Ceramic Package	750 mW
Derate Above +25°C	6 mW/°C
Plastic Package	625 mW/°C
Derate Above +25°C	5.5 mW/°C

FUNCTIONAL BLOCK DIAGRAM



Operating Temperature	
XR-2567M	−55°C to +125°C
XR-2567C	0°C to +70°C
Storage Temperature	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Temperature Range
XR-2567CN	Ceramic	0°C to +70°C
XR-2567CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2567 dual monolithic tone decoder consists of two independant 567-type circuits and an on board voltage regulator. Each decoder has a phase detector, low pass filter, and current controlled oscillator which comprise the basic phase locked loop, plus an additional low pass filter and quadrature detector enabling detection of in-band signals. Both devices have normally high open collector outputs capable of sinking 100 mA.

The input signal is applied to Pin 14 (device A) or Pin 11 (device B), both with 20 kΩ nominal input resistance. Free running frequency is controlled by an RC network at Pins 1 and 16 (device A) or Pins 8 and 9 (device B). A capacitor on Pin 2 (A), or Pin 7 (B) serves as the output filter and eliminates out-of-band triggering. PLL filtering is accomplished with a capacitor on Pin 15 (A), or Pin 10 (B); bandwidth and skew are also dependant upon the circuitry here. Bandwidth is adjustable from 0% to 14% of the center frequency. Pin 13 is $+V_{CC}$ (4.75 to 12V nominal, 14V maximum); Pin 7 is ground; and Pin 3 (A) or Pin 6 (B) is the open collector output, pulling low when an in-band signal triggers the device.

Voltage supplies below 7V necessitate bypassing the internal regulator. This is accomplished by shorting Pin 12 to V_{CC}; for supplies over 7V, a bypass capacitor of at least 1 μF should AC ground Pin 12.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, T_A = 25° C, unless otherwise specified.Test circuit of Figure 2, S_1 closed unless otherwise specified.

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
GENERAL					
Supply Voltage Range					
Without Regulator	4.75		7	V_{dc}	See Figure 5, S_1 closed.
With Internal Regulator	6.5		12	V_{dc}	See Figure 5, S_1 open.
Supply Current (both decoders)					See Figure 7, 8
Quiescent XR-2567M		12	16	mA	R_L = 20 kΩ
XR-2567C		14	20	mA	R_L = 20 kΩ
Activated XR-2567M		22	26	mA	R_L = 20 kΩ
XR-2567C		24	30	mA	R_L = 20 kΩ
Output Voltage			15	V	
Negative Voltage at Input			−10	V	
Positive Voltage at Input			V_{CC}+0.5	V	
CENTER FREQUENCY (each decoder section)					
Highest Center Frequency	100	500		kHz	
Center Frequency Stability					
Temperature T_A = 25°C		35		ppm/°C	See Figure 14
0° < T_A < +70°C		±60		ppm/°C	See Figure 14
−55° < T_A < +125°C		±140		ppm/°C	See Figure 14
Supply Voltage					
Without Regulator					
XR-2567M		0.5	1.0	%/V	f_o = 100 kHz
XR-2567C		0.7	2.0	%/V	f_o = 100 kHz
With Internal Regulator					
XR-2567M		0.05		%/V	f_o = 100 kHz, V_{CC} = 9V
XR-2567C		0.1		%/V	f_o = 100 kHz, V_{CC} = 9V
DETECTION BANDWIDTH (each decoder section)					
Largest Detection Bandwidth					
XR-2567M	12	14	16	% of f_o	f_o = 100 kHz
XR-2567C	10	14	18	% of f_o	f_o = 100 kHz
Largest Detection Bandwidth Skew					
XR-2567M		1	2	% of f_o	
XR-2567C		1	3	% of f_o	
Largest Detection Bandwidth Variation					
Temperature		±0.1		%/°C	V_{in} = 300 mV rms
Supply Voltage		±2		%/V	V_{in} = 300 mV rms
INPUT (each decoder section)					
Input Resistance		20		kΩ	
Smallest Detectable Input Voltage		20	25	mV rms	I_L = 100 mA, f_i = f_o
Largest No-Output Input Voltage	10	15		mV rms	I_L = 100 mA, f_i = f_o
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6		dB	
Minimum Input Signal to Wideband Noise Ratio		−6		dB	Noise BW = 140 kHz
OUTPUT (each decoder section)					
Output Saturation Voltage		0.2	0.4	V	I_L = 30 mA, V_{in} = 25 mV rms
		0.6	1.0	V	I_L = 100 mA, V_{in} = 25 mV rms
Output Leakage Current		0.01	25	μA	
Fastest ON-OFF Cycling Rate		f_o/20			
Output Rise Time		150		ns	R_L = 50Ω
Output Fall Time		30		ns	R_L = 50Ω
MATCHING CHARACTERISTICS					
Center Frequency Matching		1		%	f_o = 10 kHz
Temperature Drift Matching		±20		ppm/°C	0°C < T_A < 70°C
		±50		ppm/°C	−55°C < T_A < 125°C

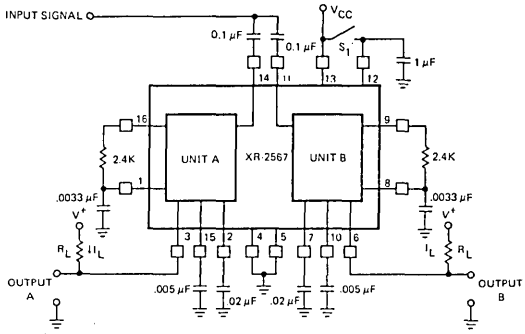
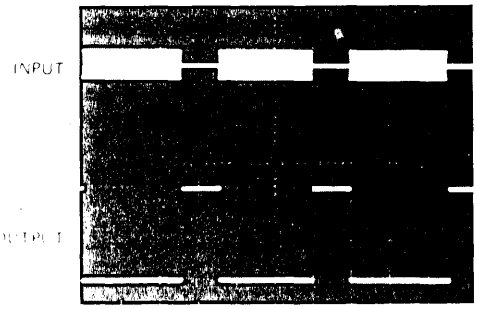


Figure 2. Test Circuit



Response to 100 mV rms tone burst.
R_L = 100 ohms.

Figure 3. XR-2567 Typical Response

DEFINITIONS OF XR-2567 PARAMETERS

f_o is the *free-running frequency* of the current-controlled oscillator of the PLL with no input signal. It is determined by resistor R_1 and capacitor C_1; f_o can be approximated by

$$f_o \approx \frac{1}{R_1 C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

The *detection bandwidth* is the frequency range centered about f_o, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a "logic zero" state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the low-pass bandwidth filter. The bandwidth of the filter, as a percent of f_o, can be determined by the approximation

$$BW \approx 1070 \sqrt{\frac{V_i}{f_o C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance in μF at Pins 10 or 15.

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency, f_o. It is defined as $(f_{max} + f_{min} - 2f_o)/f_o$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

DESCRIPTION OF CIRCUIT CONTROLS

INPUT (Pins 11 and 14)

The input signal is applied to Pins 14 and/or 11 through a coupling capacitor, C_C. These terminals are internally biased at a dc level 2 volts above ground and they have an input impedance level of approximately 20 kΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (Pins 1, 8, 9, and 16)

The center frequency, f_o, of each decoder section is set by a resistor R_1 and a capacitor C_1. R_{1A} is connected between Pins 1 and 16 in decoder section A, and R_{1B} between Pins 8 and 9 of decoder section B. C_{1A} is connected from Pin 1 to ground, and C_{1B} from Pin 8 to ground, as shown in Figure 4. R_1 and C_1 should be selected for the desired center frequency by the expression $f_o \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that 2 kΩ ≤ R_1 ≤ 20 kΩ, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

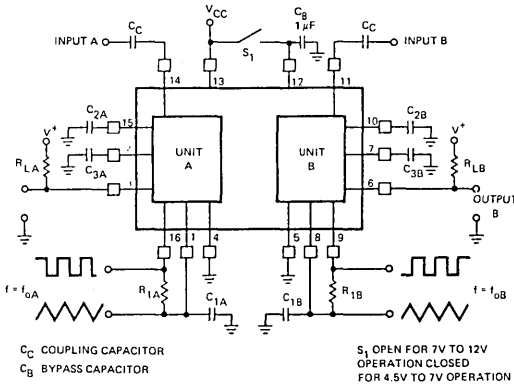


Figure 4. Circuit Connection Diagram

For decoder section A, the oscillator output can be obtained at either Pin 1 or 16. Pin 16 is the oscillator squarewave output which has a magnitude of approximately V_{CC} – 1.4V and an average dc level of $V_{CC}/2$. A 1 kΩ load may be driven from this point. The voltage at

TYPICAL CHARACTERISTICS

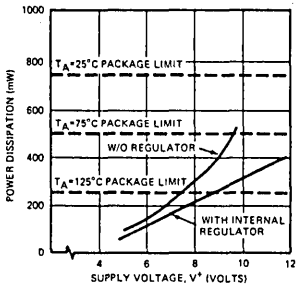


Figure 5. Internal Power Dissipation vs. Supply Voltage. Both Units Activated, R_L = 20 k

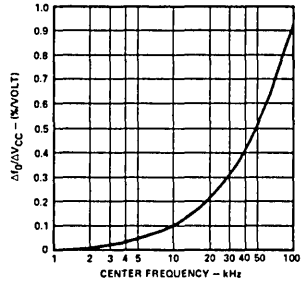


Figure 6. Power Supply Dependence of Center Frequency

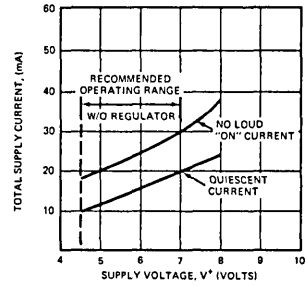


Figure 7. Total Supply Current vs. Supply Voltage for Operation Without Internal Regulator (Pins 12 and 13 Shorted)

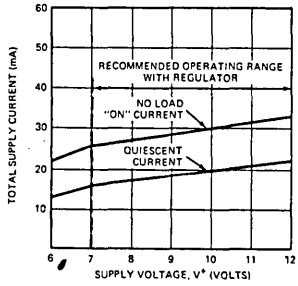


Figure 8. Total Supply Current vs. Supply Voltage for Operation with Internal Regulator (Pins 12 and 13 Not Connected)

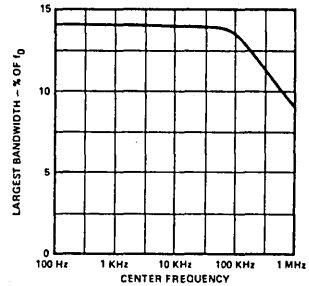


Figure 9. Largest Detection Bandwidth

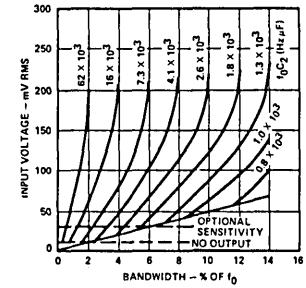


Figure 10. Bandwidth vs. Input Signal Amplitude (C_2 in μF)

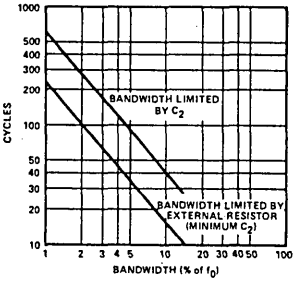


Figure 11. Greatest Number of Cycles Before Output

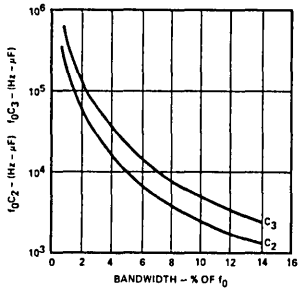


Figure 12. Detection Bandwidth as a Function of C_2 and C_3

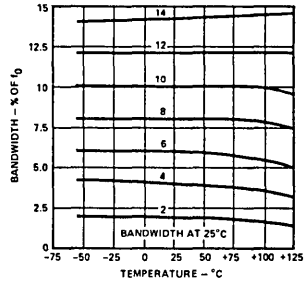


Figure 13. Bandwidth Variation With Temperature

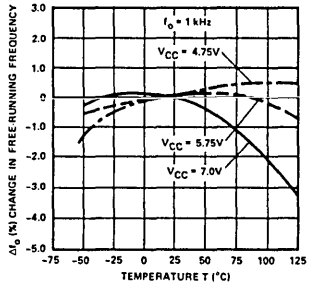


Figure 14. Frequency Drift With Temperature

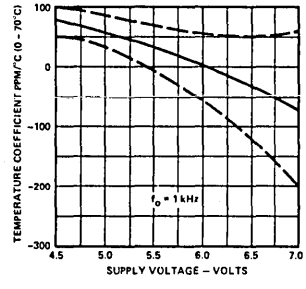


Figure 15. Temperature Coefficient of Center Frequency (Mean and S.D.)

pin 1 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to Pin 1 to avoid disturbing the temperature stability or duty cycle of the oscillator. For section B, Pin 9 is the squarewave output and Pin 8 the exponential triangle waveform output.

LOOP FILTER, C_2 (Pins 10 and 15)

Capacitors C_{2A} and C_{2B} connected from Pins 15 and 10 to ground are the single-pole, low-pass filters for the PLL portion of decoder sections A and B. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 kΩ) is the impedance at Pins 10 or 15. The selection of C_2 is determined by the detection bandwidth requirements and input signal amplitude as shown in Figures 10 and 12. One approach is to select an area of operation from the graph and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_oC_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200$ mV rms. Then, as noted in Figure 10, bandwidth will be controlled solely by the f_oC_2 product. (For additional information, see Optional Controls Section, "Speed of Response" and "Bandwidth Reduction".)

Pins 10 and 15 correspond to the PLL phase detector outputs of sections A and B, respectively. The voltage level at these pins is a linear function of frequency over the range of 0.95 to 1.05 f_o, with a slope of approximately 20 mV/% frequency deviation.

OUTPUT FILTER, C_3 (Pins 2 and 7)

Capacitors C_{3A} and C_{3B} connected from Pins 2 and 7 to ground form low-pass post detection filters for sections A and B respectively. The function of the post detection filter is to eliminate spurious outputs caused by out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3 (4.7 k) is the internal impedance at Pins 2 or 7.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, a minimum value for C_3 is $2C_2$, where C_2 is the loop filter capacitance for the corresponding decoder section. If C_3 is smaller than $2C_2$, then frequencies adjacent to the detection band may switch the output stage "off" and "on" at the beat frequency, or the output may pulse "off" and "on" during the turn-on transient.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, this delay may be desirable as a means of suppressing spurious outputs. (For additional information, see Optional Controls Section, "Speed of Response" and "Chatter".)

LOGIC OUTPUT (Pins 3 and 6)

Output terminals 3 and 6 provide a binary logic output when an input signal tone is present within the detection-band of each respective decoder section. The logic outputs are uncommitted "bare-collector" power transistors capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from V_{CC} to Pins 3 or 6.

When an in-band signal is present, the output transistor at Pins 3 or 6 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V+ higher than the V_{CC} supply. For safe operation, V+ ≤ 15 volts.

REGULATOR BY-PASS (Pin 12)

This pin corresponds to the output of the voltage regulator section. For circuit operation with a supply voltage greater than 7V, Pin 12 should be ac grounded with a bypass capacitor ≥ 1 μF. For circuit operation over a supply voltage range of 4.5 to 7V, the voltage regulator section is not required; Pin 12 should be shorted to V_{CC}.

GROUND TERMINALS (Pins 4 and 5)

To eliminate parasitic interaction, each decoder section has a separate ground terminal. The internal regulator shares a common ground with decoder section A (Pin 4).

Independent ground terminals also allow additional flexibility for split supply operation. Pin 4 can be used as V−, and Pin 5 as ground, as shown in Figure 16. When the circuit is operated with split supplies, the positive supply should always be >6V, and the dc potential across Pins 13 and 14 should not exceed 15 volts.

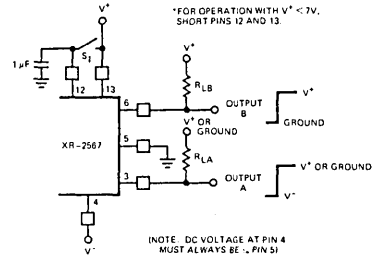


Figure 16. Split-Supply Operation Using Independent Ground Terminals of Units A and B. Unit A Operates Between V+ and V−; Unit B Operates Between V+ and Ground

OPTIONAL CONTROLS

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus, maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_0/10$ baud.

$$C_2 = \frac{130}{f_0}, C_3 = \frac{260}{f_0}$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 17 can be used to bring the quiescent C_3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

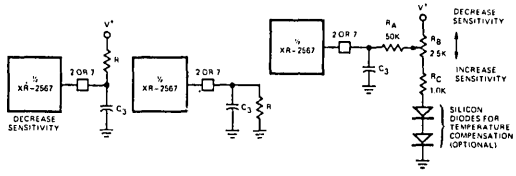


Figure 17. Optional Connections for Sensitivity Control

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, "logic" may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input or, by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 18. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

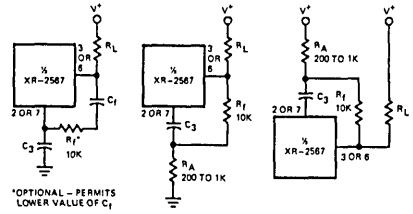


Figure 18. Methods of Reducing Chatter

SKEW ADJUSTMENT

The circuits shown in Figure 19 can be used to change the position of the detection band (capture range) within the largest detection band (or lock range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

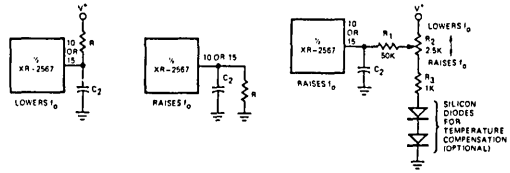


Figure 19. Connections to Reposition Detection Band

OUTPUT LATCHING

After a signal is received, the output of either decoder section can be latched "on" by connecting a 20 kΩ resistor and diode from the "output" terminal to the "output filter" terminal as shown in Figure 20. The output stage can be unlatched by raising the voltage level at the output filter terminal.

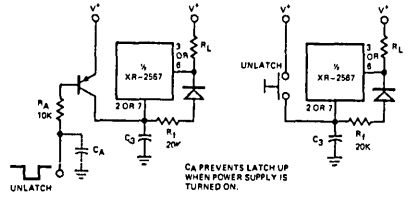
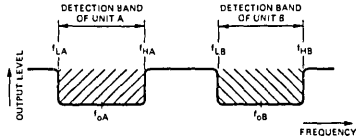


Figure 20. Output Latching

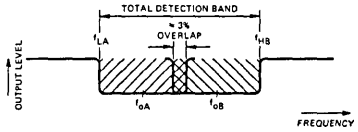
POSITIONING OF DETECTION BANDS

Figure 21 defines the respective band-edge and band-center frequencies for sections A and B of the dual tone decoder.

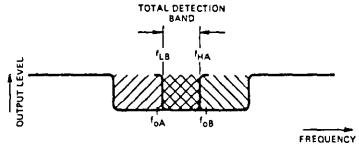
Frequencies f_L and F_H with appropriate subscripts refer to the low and the high band-edge frequencies for decoder sections A and B, and f_o is the center frequency.



(a) Independent Detection of Two Separate Tones



(b) Addition of Detection Bandwidth for Wide-Band Detection



(c) Subtraction of Bandwidths for Narrow-Band Detection

Figure 21. Positioning of Detection Bands

The two sections can be interconnected to form a single tone detector with an overall detection bandwidth equal to the sum or the difference of the detection bands for the two individual detector sections. For example, if the individual decoder sections are interconnected as shown in Figure 25, then the total detection bandwidth would be approximately equal to the sum of the respective bandwidths as shown in Figure 21(b). Similarly, if the decoders are interconnected as shown in Figure 23, then the overall detection band would be equal to the difference, or the overlap, between the respective bandwidths as shown in Figure 21(c).

BANDWIDTH REDUCTION

The bandwidth of each decoder can be reduced by either increasing the loop filter capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

Figure 22 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation. Bandwidth reduction can also be obtained by subtracting overlapping bandwidths of the two decoder sections (see Figures 21(c) and 23).

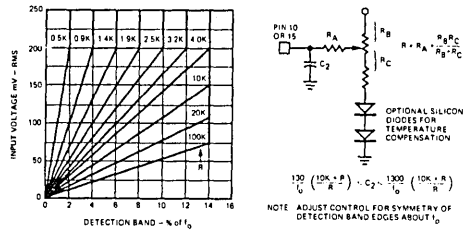


Figure 22. Bandwidth Reduction

APPLICATIONS

DUAL-TONE DETECTION

In most dual-tone detection systems, the decoder output is required to change state only when *both* input tones are present simultaneously. This can be implemented by setting the detection bandwidth of each of the XR-2567 decoder sections to cover one of the input tones; and then connecting the respective outputs through a NOR gate, as shown in Figure 23. In this case, the output of the NOR gate will be "high" only when both input tones are present simultaneously.

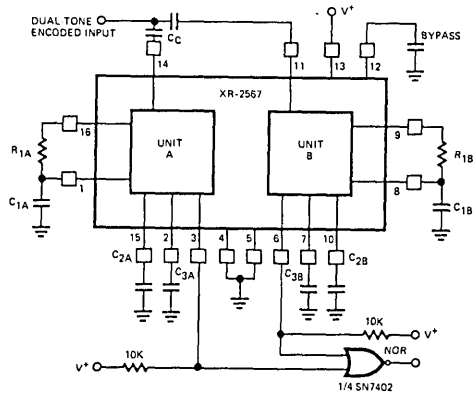


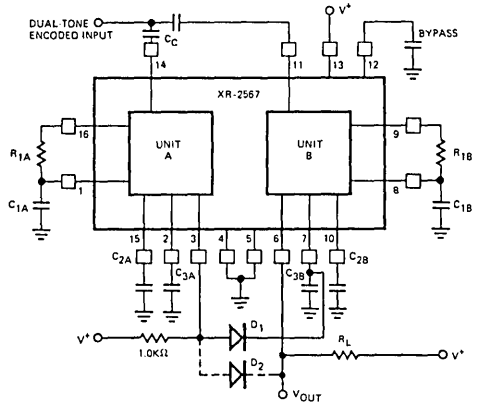
Figure 23. Connection for Decoding Dual-Tone Encoded Input Signals

Figure 24 shows additional circuit configurations which can be used for decoding multiple-tone input signals. In Figure 24(a), the output of Unit A is connected to the output filter (Pin 7) of Unit B through the diode D_1. *If no input tone is present within the detection-band of Unit A,* then its output (pin 3) is "high", which keeps diode D_1 conducting and "disables" Unit B by keeping its output (pin 6) "high". *If an input tone is present within the detection-band of Unit A,* Pin 3 is low, diode D_1 is reverse biased, and decoder B is no longer disabled. If under these conditions an input signal is present within the detection-band of Unit B, then its output at Pin 6 would be "low". Thus, the output at Pin 6 is "low" only

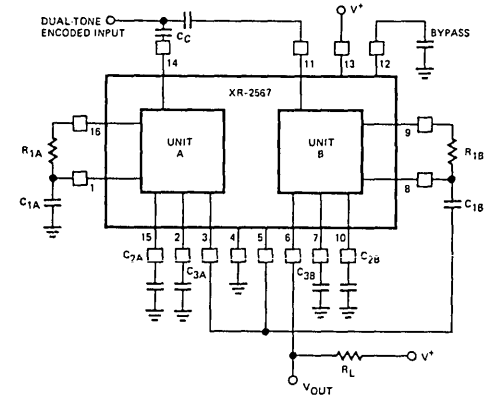
when input tones within the detection-band of A and B are present simultaneously.

The dual-tone decoder circuit of Figure 24(b) makes use of the split-ground feature of the XR-2567. The output terminal of Unit A is used as a "switch" in series with the ground terminal (Pin 5) of Unit B. If the input tone A is not present, Pin 3 is at its high-impedance state, and the ground terminal of Unit B is open-circuited. When the input tone A is present, Pin 3 goes to a low-impedance state and Unit B is activated. In this manner, the output of Unit B will be "low" *only* when both tones A and B are present.

In the circuit connection of Figure 24(b), Unit B does not draw any current until it is activated. Therefore, its power dissipation in a stand-by condition is lower than other dual-tone decoder configurations. However, due to finite series resistance between Pin 3 and ground when Unit B is activated, the output current sink capability is limited to ≤ 10 mA.



(a)



(b)

Figure 24. Additional Dual-Tone Decoding Circuits

SEQUENTIAL TONE DECODING

Dual-tone decoder circuits can also be used for sequential tone decoding where one tone must be present before the other for the circuit to operate. This can be achieved by making the output filter capacitance, C_3, of one of the sections large with respect to the other. For example, in the circuits of Figures 24(a) and 24(b), if C_{3A} is chosen to be much larger than C_{3B} ($C_{3A} \geq C_{3B}$), then Unit A will remain "on" and activate B for a finite time duration after tone A is terminated. Thus, the circuit will be able to detect the two tones only if they are present sequentially, with tone A preceding tone B.

The circuit of Figure 24(a) can also be modified for sequential tone decoding by addition of a diode, D_2, between pins 3 and 6. Once activated by Unit A, Unit B will stay "on" as long as tone B is present, even though tone A may terminate. Once tone B disappears, the circuit is reset to its original state and would require tone A to be present for activation.

HIGH-SPEED NARROW-BAND TONE DECODER

The circuit of Figure 23 can be used as a narrow-band tone decoder by overlapping the detection bands of Units A and B (see Figure 21(c)). The output of the NOR gate will be high only when an input signal is present within the overlapping portions of the detection band. To maintain uniform response within the pass-band, the input signal amplitude should be ≥ 80 mV rms. For minimum response time, PPL filter capacitors C_{2A} and C_{2B} should be:

$$C_{2A} = C_{2B} \cong \frac{130}{f_O\,(Hz)}\,\mu F$$

Under this condition, the worst-case output delay is ≈10 to 14 cycles of the input tone.

The practical matching and tracking tolerances of individual units limit the minimum bandwidth to ≈4% of f_O.

WIDE-BAND TONE DECODER

Figure 25 is a circuit configuration for increasing the detection bandwidth of the XR-2567 by combining the respective bandwidths of individual decoder sections. If the detection bands of each section are located adjacent to each other as shown in Figure 21(b), and if the two outputs (pins 3 and 6) are shorted together, then the resulting bandwidth is the sum of individual bandwidths. In this manner, the total detection bandwidth can be increased to 24% of center frequency. To maintain uniform response throughout the pass band, the input signal level should be ≥80 mV, rms, and the respective pass-bands of each section should have ≈3% overlap at center frequency.

TONE TRANSCEIVER

The XR-2567 can be used as a full-duplex tone transceiver by using one section of the unit as a tone detector and the remaining section as a tone generator. Since both sections operate independently, the circuit

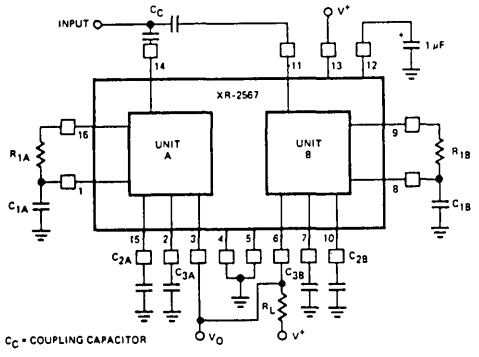


Figure 25. Wide-Band Tone Detection

can transmit and receive simultaneously. A recommended circuit connection for transceiver applications is shown in Figure 26. In this case, Unit A is utilized as the receiver, and Unit B is used as the transmitter. The transmitter section can be keyed "on" and "off" by applying a pulse to pin 8 through a disconnect diode D_1. The oscillator section of Unit B will be keyed "off" when the keying logic level at pin 8 is at a "low" state.

The output of the transmitter section (Unit B) can also be frequency modulated over a +6% deviation range by applying a modulation signal to pin 10.

HIGH CURRENT OSCILLATOR

The oscillator output of each section of XR-2567 can be amplified using the high current logic driver sections of the circuit. In this manner, each section of the circuit can switch 100 mA loads, without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 27. The oscillator frequency can be modulated over ±6% of f_O by applying a control voltage to pins 15 or 10.

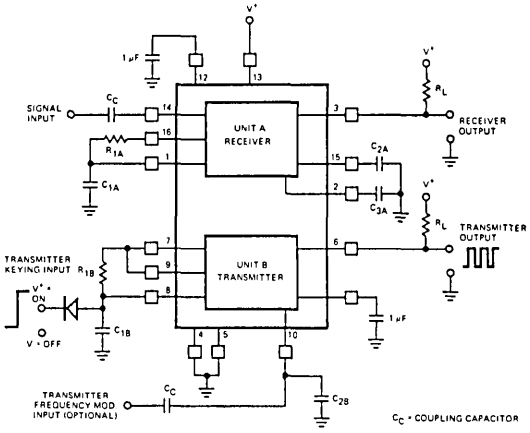


Figure 26. Tone Transceiver

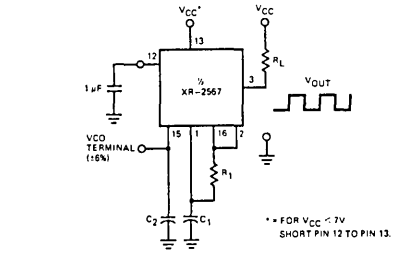


Figure 27. Precision Oscillator with High Current Output Capability

6

EXAR

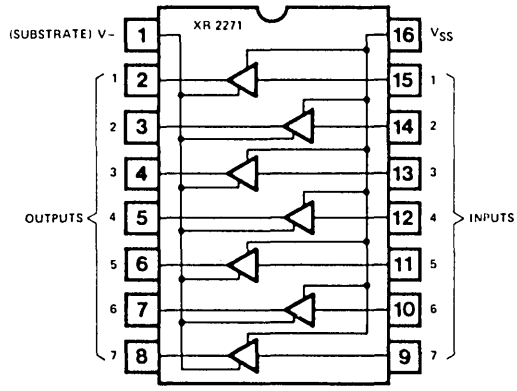
Section 7 – Interface Circuits

Fluorescent Display Driver

GENERAL DESCRIPTION

The XR-2271 is a monolithic 7-digit or 7-segment display driver designed to interface MOS logic with fluorescent displays. It features active high logic and low input current. Each XR-2271 is capable of driving seven digits or segments of a display panel and provides complete input and output isolation. Since the output pull up resistors are incorporated on chip, no external parts are required to interface fluorescent displays.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Active High Logic
Low Input Current
Complete Input Output Isolation
Output Pull Up Resistors On Chip
No External Parts Required To Drive
Fluorescent Displays

APPLICATIONS

Fluorescent Display Driver
MOS Logic/High-Voltage Interface

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2271CN	Ceramic	0°C to +70°C
XR-2271CP	Plastic	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{SS} – V –	50V Max.
Input to V –	50V Max.
Outputs to V –	50V Max.
I_{SS}	20 mA Max.
Power Dissipation $T_A \leq 25°C$	625 mW Max.
Derate above 25°C	5 mW/°C
Storage Temperature	–65°C to +150°C

SYSTEM DESCRIPTION

The XR-2271 fluorescent display driver requires no additional components to interface seven segment fluorescent displays to MOS Logic. The output is an emitter follower and can switch up to 50V at 20 mA. All inputs are protected to 50V and pull up resistors are integrated onto the device.

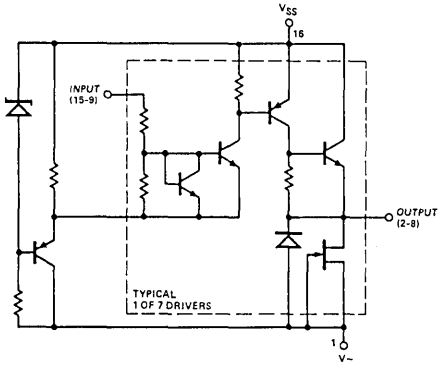
ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{SS} = 0V, V− = −40V, Note 2)

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Logical "1" Input Voltage	−1.2		0	V	V_{in} on	V_O = −2.0V I_O = −7.5 mA
Logical "0" Input Voltage			−6	V	V_{in} off	V_O = V− +2V
Logical "1" Input Current		0.25	0.8	mA	I_{in} on	V_{in} = −1.2V V_O = −2.0V
Logical "0" Input Current	−50	0 −90	50	μA μA	I_{in} off	V_O = V− +2V V_{in} = −6V V_{in} = −15V
Logical "1" Output Voltage	−2.0	−0.9	0	V	V_O on	V_O on
Logical "0" Output Voltage		−40	−38	V	V_O off	V_{in} = −6V
Output Pull Down Resistance		45		KΩ	R_O	V_{in} = −6V Note 3
Output Pull Down Current		350		μA	I_S	V_O = −5V V_{in} = −6V Note 3
Power Supply Current		−1.2 −7	−1.4 −12.0	mA mA	I—off I—on	All inputs −6V All inputs −1.2V

AC Parameters (T_A = +25°C, Test Circuit Figure 2)

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Output on Delay Time		1	5	μS	t_d	C_L = 25 pF R_L = 10 KΩ
Output on Rise Time		0.5	2	μS	t_r	C_L = 25 pf R_L = 10K
Output off Storage Time		0.8	5	μS	t_s	C_L = 25 pF R_L = 10 KΩ
Output off Fall Time		0.6 2	2.0 25	μS μS	t_f	C_L = 25 pF R_L = 10K R_L = ∞

Note 1. The "Absolute Maximum Ratings" are those values beyond which the device may be damaged.
Note 2. All voltages measured with respect to V_{SS} unless otherwise noted. Positive current flow is into a device pin.
Note 3. The output pull down resistance is an N channel junction FET. For $V_O \approx V-$ it is resistive, and for $|V_O - (V-)| > 20V$, it is current sink.



EQUIVALENT SCHEMATIC DIAGRAM

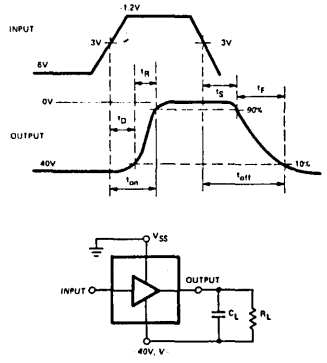


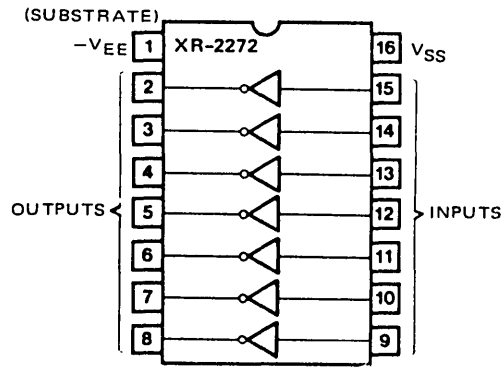
Figure 2. XR-2271 AC Parameter Test Circuit

High-Voltage 7-Digit Display Driver

GENERAL DESCRIPTION

The XR-2272 is a monolithic high voltage display driver array specifically designed to drive gas-filled digit displays. The circuit is made up of seven independent digit driver sections in the same monolithic package. Its main application is to act as buffer interface between MOS outputs and the anodes of a gas discharge panel. The XR-2272 is particularly well suited to interfacing with Panaplex II type displays.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Active Low Inputs
High Breakdown Voltage
Low Power Dissipation
Complete Input-Output Isolation
On-Chip Pull-Up Resistors
Versatility for Display Interface

APPLICATIONS

Gas Discharge Display Driver
Panaplex Display Driver
MOS Logic to High-Voltage Interface

ABSOLUTE MAXIMUM RATINGS

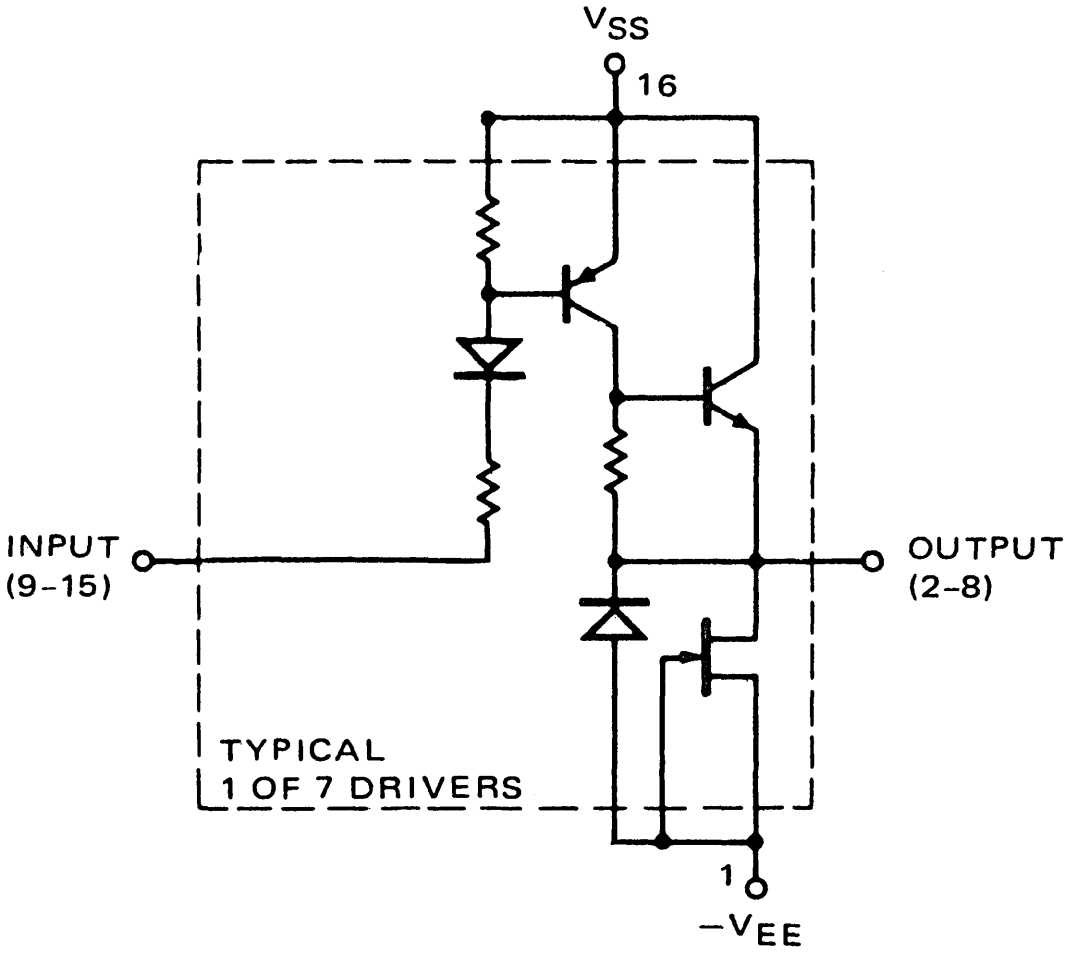
Supply Voltage ($-V_{EE}$)	−75V Max.
Output on Current Each Output	−20 mA Max.
Output on Current All Combined	−50 mA Max.
Positive Supply Current I_{SS}	60 mA Max.
Input Current	±3 mA Max.
Input Voltage	$-V_{EE}$, Min., V_{SS}, Max.
Package Power Dissipation, 25°C	625 mW (Plastic)
Derating above 25°C	5 mW/°C
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to 150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2272CN	Ceramic	0°C to +70°C
XR-2272CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2272 high voltage display driver features seven independent sections, each capable of switching −75 V at up to 20 mA. Each has active low inputs and monolithic pull-up resistors. The output is an emitter follower.



EQUIVALENT SCHEMATIC DIAGRAM

XR-2272

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{SS} = 0V, V− = −60V, Note 1)

PARAMETERS	MIN	TYP	MAX	UNITS	SYMBOL	CONDITIONS
Input Off Voltage		−1.8	−1.2	V	V_{in}off	I_O = −5 μA
Input Off Current		−20		μA	I_{in}off	V_{in} = −1.2V I_O = −5 μA
Input On Voltage			−6	V	V_{in} on	V_O = −1.4V I_O = −15 mA
Input On Current	−600	−250	−100	μA	I_{in} on	V_O = −1.4V I_O = −15 mA
Output Off Voltage		−60	−48	V	V_O off	V_{in} = −1.2V
Output On Voltage	−1.4	−0.9	0	V	V_O on	V_{in} = −6V I_O = −15 mA
Output Pull Down Resistance		45		KΩ	R_O	V_{in} = −6V Note 2
Output Pull Down Current		350		μA	I_S	V_O = −5V V_{in} = −6V Note 2
Supply Current Off State		1	150	μA	I^-	All inputs at −1.2V
One Segment On		0.35	2	mA	I^-	One input at −6V
All Segments On		2.2	6	mA	I^-	All inputs at −6V

AC Parameters (T_A = +25°C, Test Circuit Figure 2)

Output on Delay Time		1	5	μS	t_d	C_L = 25 pF R_L = 10 KΩ
Output on Rise Time		0.5	2	μS	t_r	C_L = 25 pF R_L = 10 K
Output off Storage Time		0.8	5	μS	t_s	C_L = 25 pF R_L = 10 KΩ
Output off Fall Time		0.6 2	2.0 25	μS μS	t_f	C_L = 25 pF R_L = 10K R_L = ∞

Note 1. All voltages measured with respect to V_{SS} unless otherwise noted. Positive current flow is into a device pin.

Note 2. The output pull down resistance is an N-Channel junction FET. For $V_O \approx V-$ it is resistive, and for $|V_O - (V-)| > 20V$, it is a current sink.

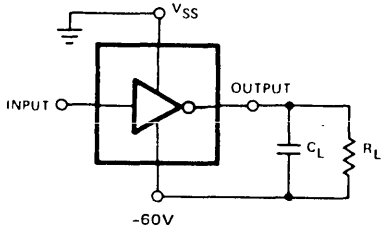


Figure 2. XR-2272 AC Parameter Test Circuit

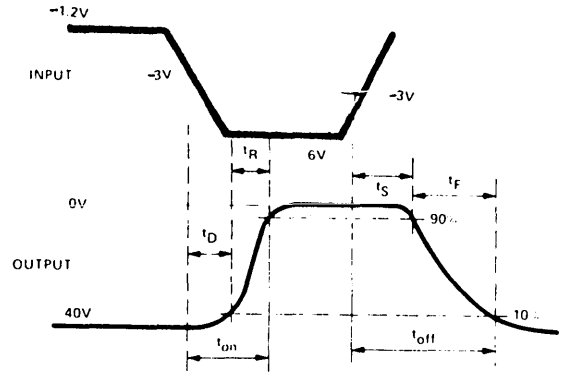


Figure 3. AC Test Waveforms

High-Voltage AC Plasma Display Drivers

GENERAL DESCRIPTION

The XR-2284 and the XR-2288 are high voltage display driver arrays especially designed for interfacing with ac plasma display systems. The XR-2284 contains four independent driver channels, whereas its dual version, the XR-2288, contains eight driver channels. Each driver array can be used for either the segment or the column (or digit) drive, and several arrays can be "stacked" together to drive a large number of display segments.

All four channels of the XR-2284 are driven by a common ac toggle voltage; however, the XR-2288 has two independent toggle inputs, one for each of the four channels in the IC. The XR-2284 and the XR-2288 are designed for 360 volt ac plasma systems and have minimum stand-off voltages of 90 volts. The XR-2284C and the XR-2288C are designed for 240 volt plasma systems, and have minimum stand-off voltages of 60 volts.

The circuits can operate with ac toggle frequencies up to 200 kHz, and each driver channel can sink or source 100 mA of capacitive load current. For proper operation, the substrate terminals of all drivers must be grounded through an external disconnect diode, D_X, as shown in the schematic diagram.

FEATURES

High Stand-off Voltage
- 90 V minimum for XR-2284/XR-2288
- 60 V minimum for XR-2284C/XR-2288C

Very Low AC Standby Power
- (≈25 mW/channel at 100 kHz)

Zero DC Standby Power
100 mA Output Drive Capability
TTL and CMOS Compatible Inputs
Digital or Segment Drive Capability

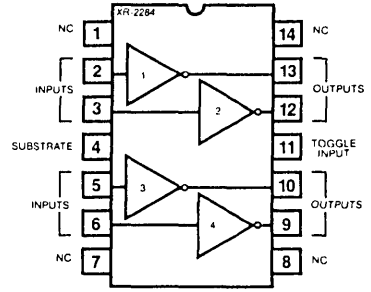
APPLICATIONS

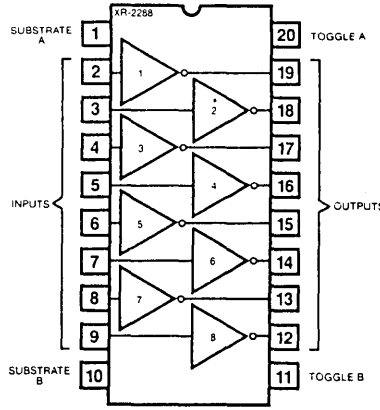
High Voltage AC Plasma Panels
High Voltage Pulsed Displays
Pulsed AC Switching

ABSOLUTE MAXIMUM RATINGS

Toggle Input Voltage	
XR-2284P/XR-2288P	±90V peak
XR-2284CP/XR-2288CP	±60B peak

FUNCTIONAL BLOCK DIAGRAMS





Power Dissipation	
XR-2284P/XR-2284CP	625 mW
XR-2288P/XR-2288CP	900 mW
Derate above +25°C	5 mW/°C
Storage Temperature	−65°C to 150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2284P	Plastic	0°C to 70°C
XR-2284CP	Plastic	0°C to 70°C
XR-2288P	Plastic	0°C to 70°C
XR-2288CP	Plastic	0°C to 70°C

7

XR-2284/2288

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, with external diode D_X = IN4002 or equivalent, T_A = 25°C, unless otherwise specified. (See operating precautions.)

PARAMETERS	XR-2284/XR-2288 MIN	XR-2284/XR-2288 TYP	XR-2284/XR-2288 MAX	XR-2284C/XR-2288C MIN	XR-2284C/XR-2288C TYP	XR-2284C/XR-2288C MAX	UNIT	SYMBOL	CONDITIONS
Maximum Toggle Voltage	±90			±60			V_{pp}	V_T	Peak-to-peak AC voltage- See Figure 3.
Output Current Capability									
Max Sourcing Current	100	150		100	120		mA	I_{source}	12% Duty Cycle
Max Sinking Current	100	120		100	120		mA	I_{sink}	12% Duty Cycle
Output Voltage									See Figure 4.
High Output) (selected)		(V_T-4)			(V_T-4)		V_{peak}	V_{OHS}	
High Output (non-selected)		4V			4V			V_{OHN}	
Low output		$(-V_T+2)$			$(-V_T+2)$		V_{peak}	V_{OL}	
Maximum Toggle Frequency	200			100	200		kHz	f_T	
High-Level Input	2	1.4		2	1.4		V	V_{IH}	
Low-Level Input		1.2	0.8		1.2	0.8	V	V_{IL}	
Input Current		8	16		8	16	mA	I_{IN}	See Figure 3.
Switching Characteristics									See Figure 4.
Rise Delay		500			500		nsec	t_{rd}	
Fall Delay (selected)		500			500		nsec	t_{fds}	
Fall Delay (non-selected)		500			500		nsec	t_{fdn}	

IMPORTANT OPERATING PRECAUTIONS

1. External diode D_X with reverse breakdown voltage $\geq V_T$ *must* be included in all circuit applications. This diode decouples or "floats" the IC from the circuit ground during the negative excursions of the toggle voltage, V_T.

2. the rise and fall times of toggle voltages, V_T, *must* be held to a value such that output current of each channel does not exceed 100 mA. This can be done by limiting the slewrate of toggle voltage to:

$$\left(\frac{dV_T}{dt}\right)_{max} \leq \frac{100\ mA}{C_L},$$

where C_L is the *total* load capacitance, including the capacitance of the display elements, driven by the particular output.

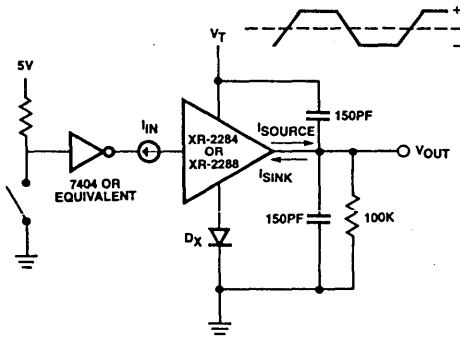


Figure 1. Generalized Test Circuit

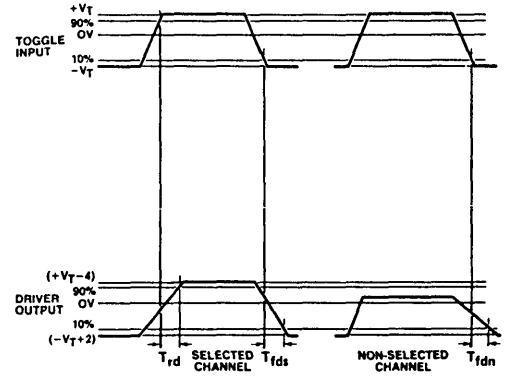


Figure 2. Typical Timing Waveforms

FUNDAMENTALS OF AC PLASMA DISPLAYS

Ac plasma display offer significant advantages over other alpha-numeric displays such as fluorescent or LED type panels. Some of these advantages are the low cost of the display itself, its wide viewing angle, and the ease of formatting in the selection of display segments and digits. Plasma systems typically require high voltage (200V or higher) ac drivers operating at relatively high frequencies (100 kHz and up). Although the plasma display panel is a capacitive load and does not draw dc current, the display driver output is required to provide a high output drive current (typically 50 to 100 mA), during the rising and the falling edges of the toggle voltage, so that the driver output can still follow the ac toggle voltage at high frequencies.

The ac plasma displays normally require a net voltage in excess of 200 volts across the display to turn it on. In practice, this is achieved by "pulsing" the display with two out-of-phase toggle voltages (V_T), such that a net peak-to-peak voltage of $2V_T$ appears across the selected display portion to make it turn on. Thus, in controlling the plasma display, one must control the amplitude of two peak-to-peak toggle swings, one on the "segment-side" and the other on the "digit-side" of the display, where each toggle swing is equal to only one-half of the total voltage swing needed to light up the display. For example, for 240 volt ac plasma display systems, the toggle voltage used (V_T) would be 120 volts; and for 360 volt display systems, 180 volt toggle voltage will be needed.

PRINCIPLES OF OPERATION

The XR-2284 and the XR-2288 ac plasma display driver circuits control the drive voltage applied to the segment or the digit section of an ac plasma panel.

Figure 3 shows the timing waveforms associated with the ac plasma driver circuit, for the case of a 360 volt display system (i.e., $V_T = \pm 90V = 180V$ pp). In normal operation, all of the driver channels are driven by a common ac toggle voltage (V_T) shown in Figure 3(a). When the control input to a driver channel, V_{in}, is at "high" state, as shown in Figure 3(b), its output would be clamped nearly to ground and would follow the negative excursions of the toggle voltage, V_T. This produces only 1/2 of the required peak-to-peak voltage across the particular display segment, which is *not* enough to light it. However, if V_{in} is at a "low" state, the driver output, V_{out}, would be enabled and follow closely the peak-to-peak excursions of the toggle voltage. This would then cause the nearly full peak-to-peak swing of the ac drive to appear across the selected display segment.

It should be noted that due to the external blocking diode D_X of Figure 1, the monolithic IC substrate is completely decoupled from ground during the negative excursion of the toggle voltage and the internal diode, D_2, of the schematic diagram causes the output to follow the toggle voltage within one diode drop. In this manner, the IC has to withstand only *one-half* of the total ac signal swing, or the *one-fourth* of the total voltage appearing across the entire plasma panel.

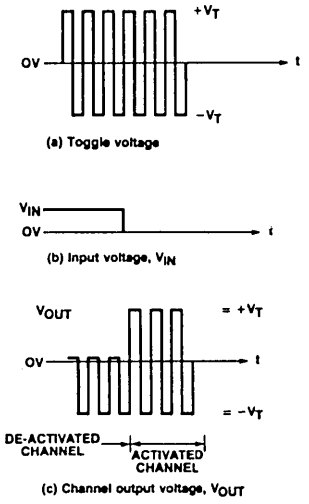


Figure 3. Timing Diagram of Circuit Waveforms

CIRCUIT DESCRIPTION

Both the XR-2284 and the XR-2288 are multichannel driver circuits, packaged in 14 and 20-pin dual-in-line IC packages respectively. The XR-2284 is a four-channel display driver, whereas the XR-2288 is an eight-channel circuit, made up of *two* four-channel driver chips in the same dual-in-line package. Thus, the XR-2288 has two toggle voltage and substrate inputs; one for each of the two four-channel IC chips sharing the same package.

The equivalent circuit diagram for a typical driver channel is shown in the schematic. All the channels have their own independent inputs and outputs, but share a common toggle or clock input and a common substrate or ground connection. The circuit is designed as a series connection of two controlled-switches, or SCR's. The transistors, Q_3 and Q_2, form one of the controlled-switches, and Q_1 and Q_4, form the second controlled-switch. The internal junction capacitance, C_j, causes

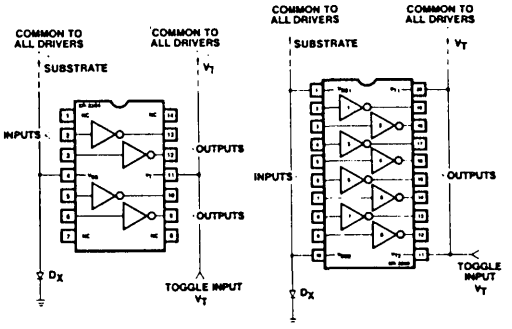


Figure 4. Generalized Connection Diagram XR-2284 and XR-2288.

the respective controlled-switches to be turned on during the positive and negative edges of the toggle input, V_T.

An external diode, D_X with a brekdown voltage $\geq V_T$, is used to "float" the substrate or decouple it from ground during the negative excursions of the toggle voltage. This external decoupling diode is common to all channels, and can serve more than one IC package, as shown in Figure 4. In this manner, many driver IC's, either of the four-channel (XR-2284) or the eight-channel (XR-2288) type, can be "stacked" to drive a large number of display segments or columns, with only one common blocking diode and a common toggle input, as shown in the Figure 4.

Under dc conditions, i.e., with no ac toggle drive, the driver IC's do not dissipate any appreciable standby power. However, when the ac toggle voltage, V_T, is applied and a particular channel is enabled, then the corresponding output can follow the peak-to-peak toggle voltage and sink or source up to 100 mA of capacitive load current to the plasma panel.

APPLICATIONS

Driving Seven-Segment Displays

Figure 5 illustrates a four digit, seven-segment plasma display panel with decimal point. The entire display can be driven by one XR-2288 driver for the segment side and one XR-2284 driver for the digit side. The segment and the digit drivers each must have their external disconnect diode, D_X, as shown in the figure. The segment and the digit sides of the display are driven by out-of-phase toggle signals, V_T and $\overline{V_T}$, which cause a total firing voltage of four V_T to appear across the enabled display segment. Segments not enabled will have a net voltage of three V_T across them. The peak-to-peak

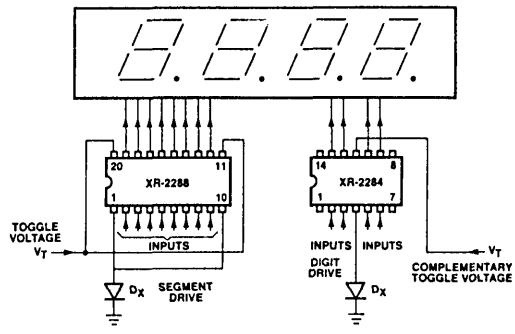


Figure 5. Typical Circuit Connection for Driving 7-Segment 4-Digit Display with Decimal Point

swing of the toggle voltage, V_T, is chosen so that the firing voltage, V_f, necessary for the display to light up, falls into the range of:

$$3\,V_T < V_f < 4\,V_T.$$

In this manner, only the selected and enabled display cells will have an energizing voltage $\geq V_f$.

Driving Alpha-Numeric Displays

Figure 6 shows the circuit connection for driving an eight digit, 16-segment alpha-numeric display. The number of digits can be increased by connecting additional XR-2284 or XR-2288 driver arrays into the digit side. These additional arrays can be directly "stacked" using the same external disconnect diode, D_X, and the same toggle voltage drive lines already present on the digit side.

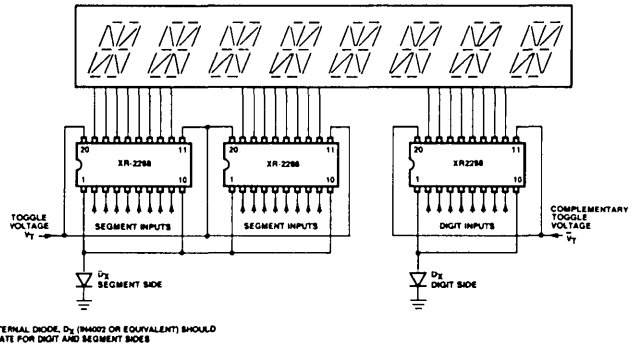
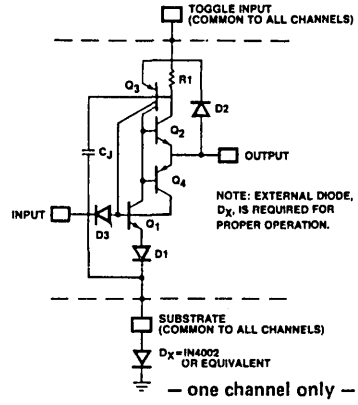


Figure 6. Circuit Configuration for Driving 16-Segment Alpha-Numeric Display Panel

EQUIVALENT SCHEMATIC DIAGRAM

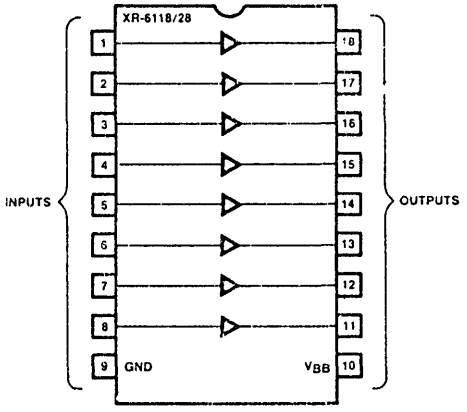


Fluorescent Display Drivers

GENERAL DESCRIPTION

The XR-6118 and the XR-6128 are high-voltage display driver arrays which are designed to interface between low-level digital logic and vacuum fluorescent displays. Each circuit consists of eight independent signal channels comprised of Darlington output stages and common-emitter type inputs. All stages on the chip share common power supply and ground connections. Both device types are capable of driving digits and/or segments of fluorescent displays, and all of the eight outputs can be activated simultaneously.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Sprague UDN-6118A, UDN-6128A, and UDN-6118P-2 (60V)
Digit or Segment Drive Capability
Low Input Current
Integral Output Pulldown Resistors
Low Power
High Output Breakdown Voltage

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-6118P	Plastic	0°C to +70°C
XR-6128P	Plastic	0°C to +70°C
XR-6118P-2	Plastic	0°C to +70°C

7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{BB}	85V
Output Voltage, V_{OUT}	85V
Input Voltage, V_{IN}	20V
Output Current, I_{OUT}	40 mA
Power Dissipation, ($T_A \leq 25°C$)	1 W
Derate Above 25°C	8 mW/°C
Operating Temperature	0°C to +85°C
Storage Temperature	−55°C to +150°C

SYSTEM DESCRIPTION

The XR-6118 and XR-6128 fluorscent display drivers can switch up to 85V and 40 mA. Inputs are protected to 20V. The XR-6118 is compatible with TTL, Schottky TTL, DTL and 5 Volt CMOS logic families. The XR-6128 is intended for use with PMOS or CMOS logic families operating with supply voltages of 6V to 15V. The two device types differ only in their input threshold levels (See Figure 1). With either device type, the output load is activated when the inputs are pulled toward positive supply. Output pulldown resistors are included on the die.

XR-6118/6128

ELECTRICAL CHARACTERISTICS

Test Conditions: (T_A = 25°C, V_{BB} = 80V) Full Temp. Range 0°C to +70°C, XR-6118A only.

SYMBOL	PARAMETERS	XR-6118A			XR-6128A			UNIT	CONDITIONS
		MIN	TYP	MAX	MIN	TYP	MAX		
I_{CEX}	Output Leakage Current			15			15	μA	V_{IN} = 0.4 V
V_{OUT}	Output ON Voltage	77			77			V	I_{OUT} = 25 mA V_{IN} = 2.4 V (XR-6118) V_{IN} = 4 V (XR-6128)
	Input On Voltage	2.4		15	4.0		15	V	I_{OUT} = 25 mA
	Input ON Current			650			1150	μA	V_{IN} = 5 V (XR-6118) V_{IN} = 15 V (XR-6128)
I_{BB}(OFF)	Supply Current Off Condition			100μA			100	μA	ALL Inputs Open
I_{BB}(ON)	On Condition			9			9	mA	V_{IN} = 2.4 V (XR-6118) (ALL Inputs)
I_{OUT}	Output Pulldown Current			1100			1100	μA	ALL Inputs Open V_{OUT} = 80 V

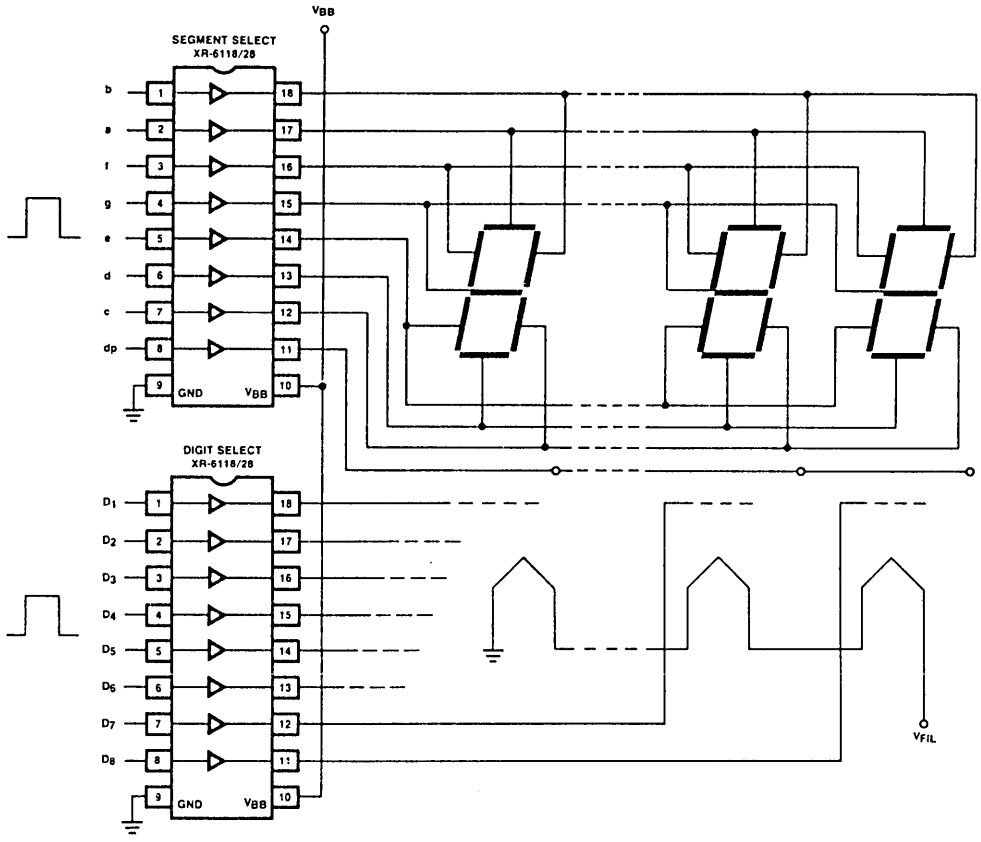
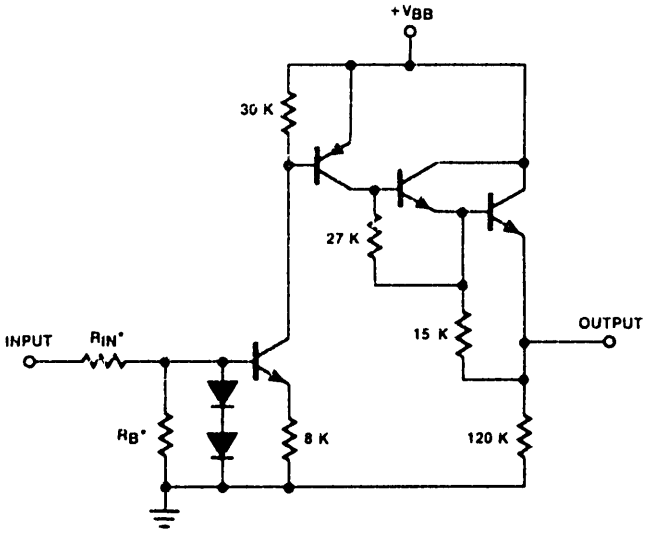


Figure 2. Typical Multiplexed Fluorescent Display Drive Application



One of Eight Stages

(*) For XR-6118
R_{IN} = 10 K, R_B = 30 K
For XR-6128:
R_{IN} = R_B = 20 K

EQUIVALENT SCHEMATIC DIAGRAM

Section 7 – Interface Circuits

High-Voltage, High-Current Darlington Transistor Arrays

GENERAL DESCRIPTION

The XR-2001/2002/2003/2004 are high-voltage, high-current Darlington transistor arrays consisting of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA are allowed, which makes the arrays ideal for driving tungsten filament lamps. The outputs may be paralleled to achieve high load current capability although each driver has a maximum continuous collector current rating of 500 mA. The arrays are directly price competitive with discrete transistor alternatives.

FEATURES

Peak Inrush Current Capability of 600 mA.
Internal Protection Diodes for Driving Inductive Loads
Excellent Noise Immunity
Direct Compatibility with Most Logic Families
Opposing Pin Configuration Eases Circuit Board Layout

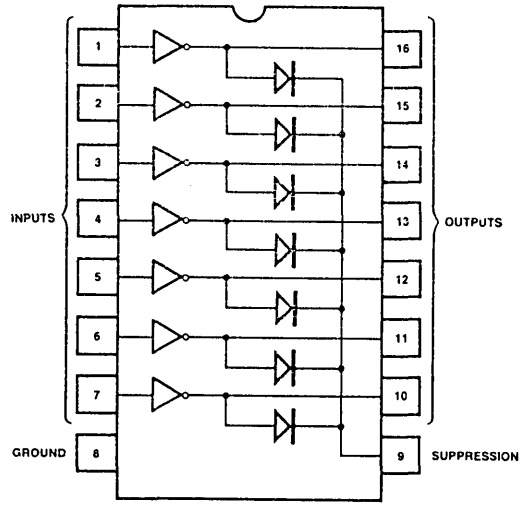
APPLICATIONS

Relay Drivers
High Current Logic Drivers
Solenoid Driver

ABSOLUTE MAXIMUM RATINGS T_A = 25°C

Output Voltage, V_{CE}	50V
Input Voltage, V_{IN}	30V
Continuous Collector Current, I_C (Each Driver)	500mA
Continuous Base Current, I_B (Each Driver)	25mA
Power Dissipation, P_D (Each Driver)	1.0W
(Total Package)	See graph
Derate Above 25°C	16 mW/°C
Storage Temperature Range	−55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2001CN	Ceramic	0°C to +70°C
XR-2002CN	Ceramic	0°C to +70°C
XR-2003CN	Ceramic	0°C to +70°C
XR-2004CN	Ceramic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2001 interfaces with bipolar digital logic (with external current limiting), or with CMOS or PMOS directly.

The XR-2002 was specifically designed to interface with 14V to 25V PMOS devices.

The XR-2003 permits operation directly with CMOS or TTL operating at a supply voltage of 5 volts. Interface requirements beyond the scope of standard logic buffers are easily handled by the XR-2003.

The XR-2004 requires less input current than the XR-2003 and the input voltage is less than that required by the XR-2002. The XR-2004 operates directly from PMOS or CMOS outputs using supply voltages of 6 to 15 volts.

ELECTRICAL CHARACTERISTICS

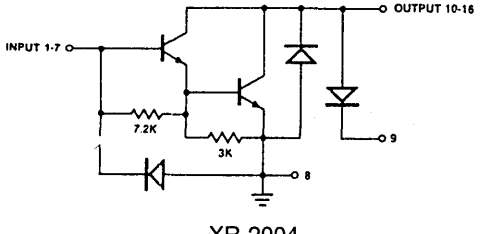
Test Conditions: T_A 25°C, unless otherwise specified.

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current			100	µA	V_{CE} = 50 V, T_A = 70°C
	XR-2002			500	µA	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6V
	XR-2004			500	µA	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1V
V_{CE}	Collector-Emitter Saturation Voltage		1.25	1.6	V	I_C = 350mA, I_B = 500µA
			1.1	1.3	V	I_C = 200mA, I_B = 350µA
			0.9	1.1	V	I_C = 100mA, I_B = 250µA
I_{IN}	Input Current (on)					
	XR-2002		0.85	1.25	mA	V_{IN} = 17V
	XR-2003		0.93	1.35	mA	V_{IN} = 3.85V
	XR-2004		0.35	0.5	mA	V_{IN} = 5V
			1.0	1.45	mA	V_{IN} = 12V
I_{IN}	Input Current (off)	50	65		µA	I_C = 500µA, T_A = 70°C
V_{IN}	Input Voltage					
	XR-2002			13	V	V_{CE} = 2 V, I_C = 300mA
	XR-2003			2.4	V	V_{CE} = 2 V, I_C = 200mA
				2.7	V	V_{CE} = 2 V, I_C = 250mA
				3.0	V	V_{CE} = 2 V, I_C = 300mA
	XR-2004			5.0	V	V_{CE} = 2 V, I_C = 125mA
				6.0	V	V_{CE} = 2 V, I_C = 200mA
				7.0	V	V_{CE} = 2 V, I_C = 275mA
				8.0	V	V_{CE} = 2 V, I_C = 350mA
h_{FE}	D-C Forward Current Transfer Ratio					
	XR-2001	1000				V_{CE} = 2 V, I_C = 350mA
C_{IN}	Input Capacitance		15	30	pF	
I_R	Clamp Diode Leakage Current			50	µA	V_R = 50V
V_F	Clamp Diode Forward Voltage		1.7	2.0	V	I_F = 350mA
t_{PLH}	Turn-On Delay		0.25	1.0	µS	0.5 E_{IN} to 0.5 E_{OUT}
t_{PHL}	Turn-Off Delay		0.25	1.0	µS	0.5 E_{IN} to 0.5 E_{OUT}

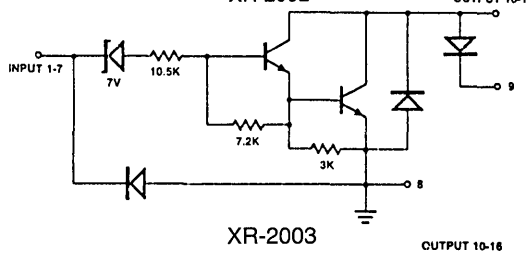
7

SCHEMATIC DIAGRAMS (One of 7 Identical Drivers is shown for each device.)

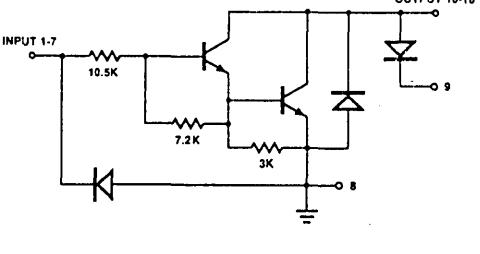
XR-2001



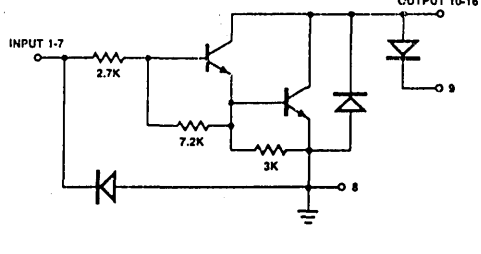
XR-2002



XR-2004



XR-2003



XR-2001/2/3/4

CHARACTERISTIC CURVES

(a) XR-2002 (b) XR-2004 (c) XR-2003

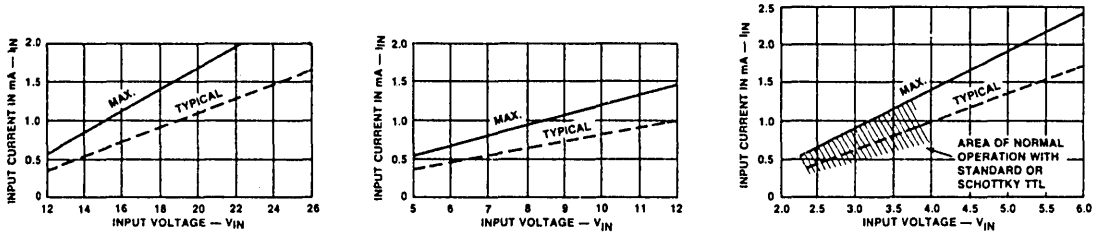


Figure 1. Input Current as a Function of Input Voltages

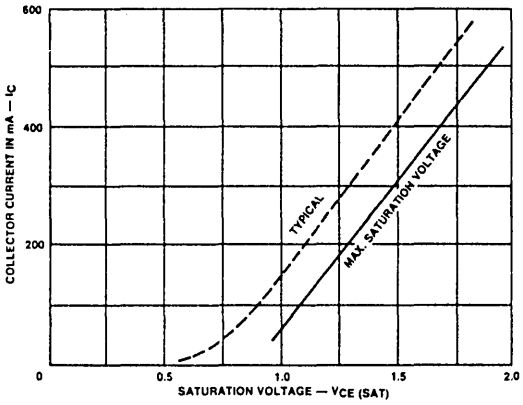


Figure 2. Collector Current as a Function of Saturation Voltage.

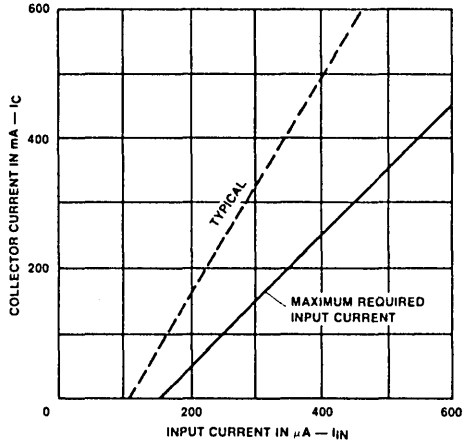


Figure 3. Collector Current as a Function of Input Current

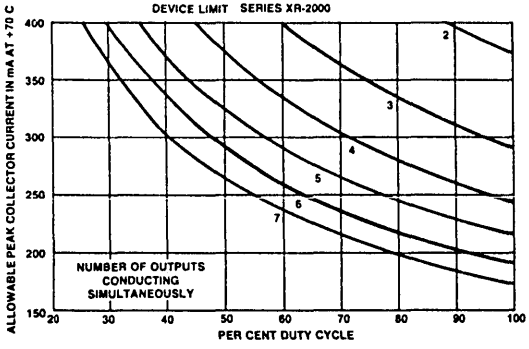


Figure 4. Peak Collector Current as a Function of Duty Cycle and Number of Outputs

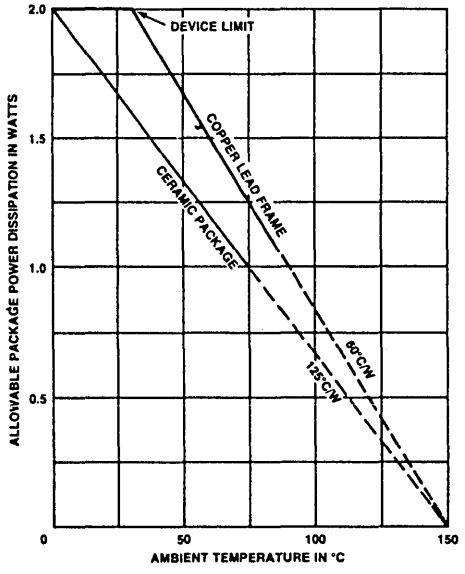


Figure 5. Allowable Average Power Dissipation as a Function of Ambient Temperature

TYPICAL APPLICATIONS

XR-2002

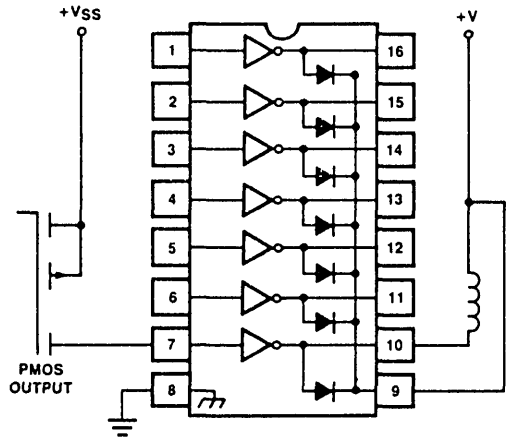


Figure 6. PMOS to Load

XR-2003

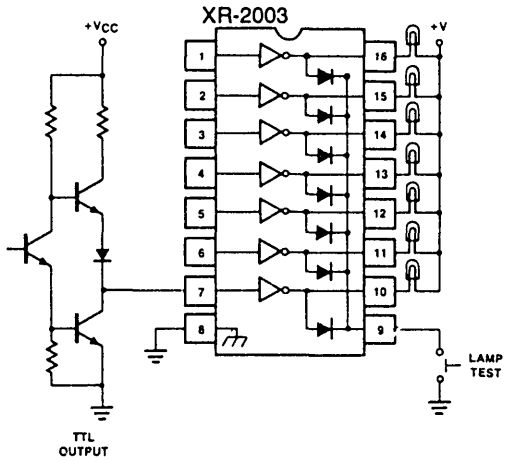


Figure 7. TTL to Load

XR-2004

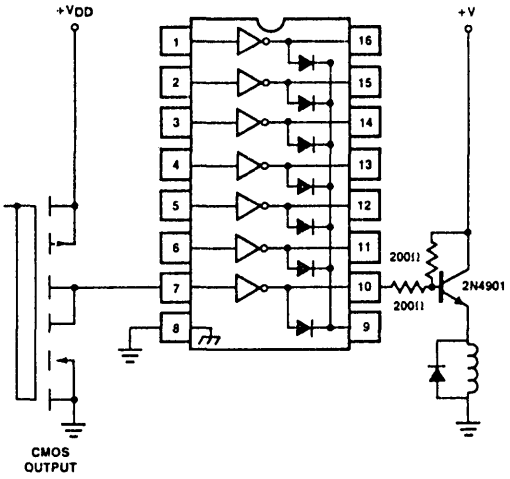


Figure 8. Buffer for Higher Current Loads

XR-2003

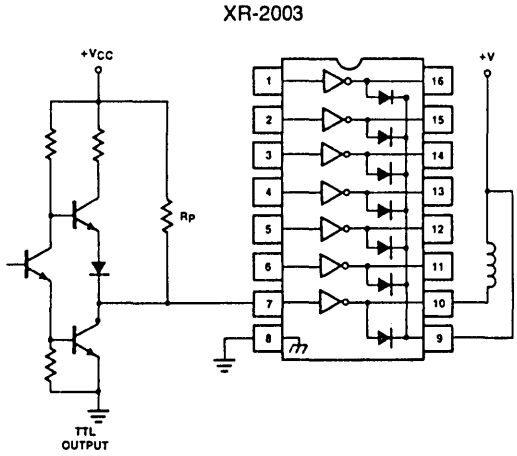


Figure 9. Use of Pull-up Resistors to Increase Drive Current

7

High-Voltage, High-Current Darlington Transistor Arrays

GENERAL DESCRIPTION

The XR-2011/2012/2013/2014 are high-voltage, high-current Darlington transistor arrays consisting of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral protection diodes for driving inductive loads. Peak inrush currents of up to 750 mA are allowed, which makes the arrays ideal for driving tungsten filament lamps. The outputs may be paralleled to achieve higher load current capability although each driver has a maximum continuous collector current rating of 600 mA. The arrays are directly price competitive with discrete transistor alternatives.

FEATURES

Peak Inrush Current Capability of 750 mA
Internal Protection Diodes for Driving Inductive Loads
Excellent Noise Immunity
Direct Compatibility with Most Logic Families
Opposing Pin Configuration Eases Circuit Board Layout

APPLICATIONS

Relay Drive
High Current Logic Driver

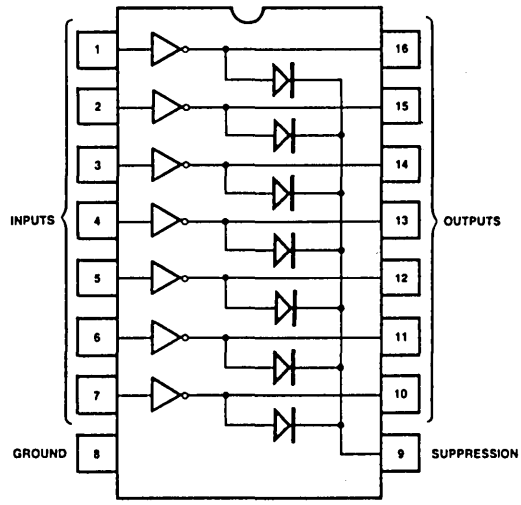
ABSOLUTE MAXIMUM RATINGS T_A = 25°C

Output Voltage, V_{CE}	50V
Input Voltage, V_{IN}	30V
Continuous Collector Current, I_C (Each Driver)	600 mA
Continuous Base Current, I_B (Each Driver)	25 mA
Power Dissipation, P_D (Each Driver)	1.0 W
(Total Package)	See graph
Derate Above 25°C	16.67 mW/°C
Storage Temperature Range	−55°C to +150°C

ORDERING INFORMATION

Part Number	Package Type	Operating Temperature
XR-2011 CN	Ceramic	0°C to +70°C
XR-2012 CN	Ceramic	0°C to +70°C
XR-2013 CN	Ceramic	0°C to +70°C
XR-2014 CN	Ceramic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2011 device is a general purpose array to be used with bipolar digital logic (with external current limiting), or with CMOS or PMOS directly. Output pins opposite input pins facilitates circuit board layout.

The XR-2012 was specifically designed to interface with 14 to 25 volt PMOS devices. The input current is limited to a safe value by a Zener diode and resistor in series.

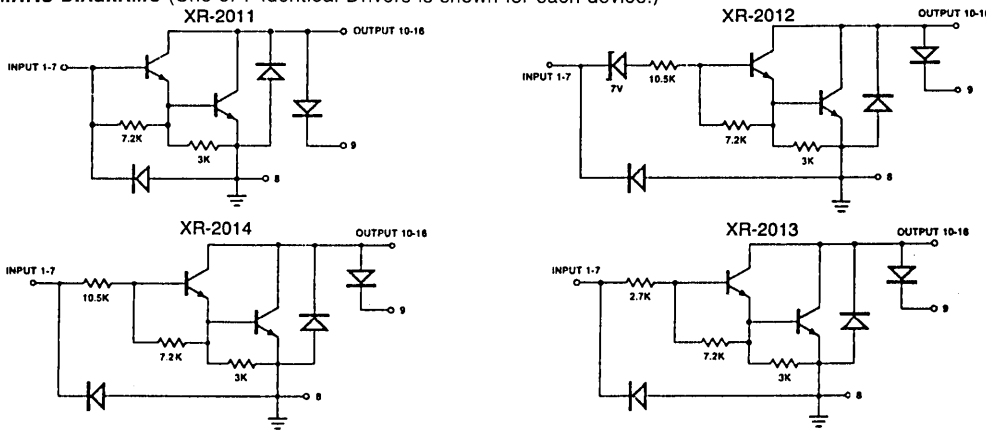
A 2.7 kΩ series base resistor to each Darlington pair in the XR-2013 permits operation directly with CMOS or TTL operating with a 5 volt supply. Interface requirements beyond the scope of standard logic buffers are easily handled by the XR-2013.

The XR-2014 requires less input current than the XR-2013 and the input voltage is less than that required by the XR-2012. The XR-2014 has a 10.5 kΩ series input resistor, permitting operation directly from PMOS or CMOS outputs using supply voltages of 6 to 15 volts.

ELECTRICAL CHARACTERISTICS (T_A 25°C unless otherwise noted)

SYMBOL	PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current XR-2012 XR-2014			100 500 500	μA μA μA	V_{CE} = 50 V, T_A = 70°C V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6V V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1V
V_{CE}	Collector-Emitter Saturation Voltage		1.7 1.3 1.1	1.9 1.6 1.3	V V V	I_C = 500mA, I_B = 600μA I_C = 350mA, I_B = 500μA I_C = 200mA, I_B = 350μA
I_{IN}	Input Current (on) XR-2012 XR-2013 XR-2014		 0.82 0.93 0.35 1.0	 1.25 1.35 0.5 1.45	 mA mA mA mA	 V_{IN} = 17V V_{IN} = 3.85V V_{IN} = 5V V_{IN} = 12V
I_{IN}	Input Current (off)	50	65		μA	I_C = 500μA, T_A = 70°C
V_{IN}	Input Voltage XR-2012 XR-2013 XR-2014			 17 2.7 3.0 3.5 7.0 8.0 9.5	 V V V V V V V	 V_{CE} = 2 V, I_C = 500mA V_{CE} = 2 V, I_C = 250mA V_{CE} = 2 V, I_C = 300mA V_{CE} = 2 V, I_C = 500mA V_{CE} = 2 V, I_C = 275mA V_{CE} = 2 V, I_C = 350mA V_{CE} = 2 V, I_C = 500mA
h_{FE}	D-C Forward Current Transfer Ratio XR-2011	 1000				 V_{CE} = 2 V, I_C = 350mA
C_{IN}	Input Capacitance		15	30	pF	
I_R	Clamp Diode Leakage Current			50	μA	V_R = 50V
V_F	Clamp Diode Forward Voltage		2.1	2.5	V	I_F = 500mA
t_{PLH}	Turn-On Delay		0.25	1.0	μS	0.5 E_{IN} to 0.5 E_{OUT}
t_{PHL}	Turn-Off Delay		0.25	1.0	μS	0.5 E_{IN} to 0.5 E_{OUT}

SCHEMATIC DIAGRAMS (One of 7 Identical Drivers is shown for each device.)



CHARACTERISTIC CURVES

(a) XR-2012 (b) XR-2014 (c) XR-2013

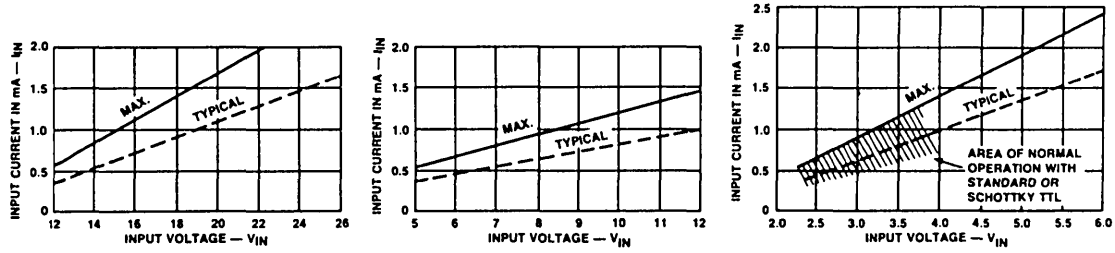


Figure 1. Input Current as a Function of Input Voltages

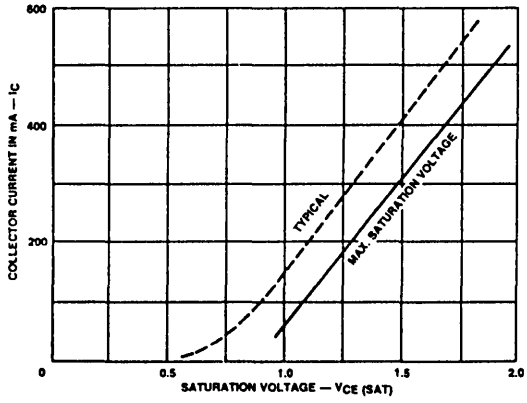


Figure 2. Collector Current as a Function of Saturation Voltage

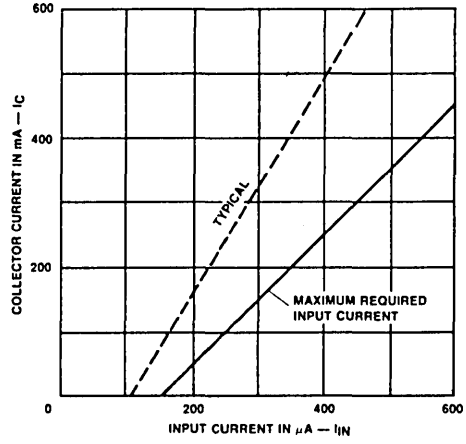


Figure 3. Collector Current as a Function of Input Current

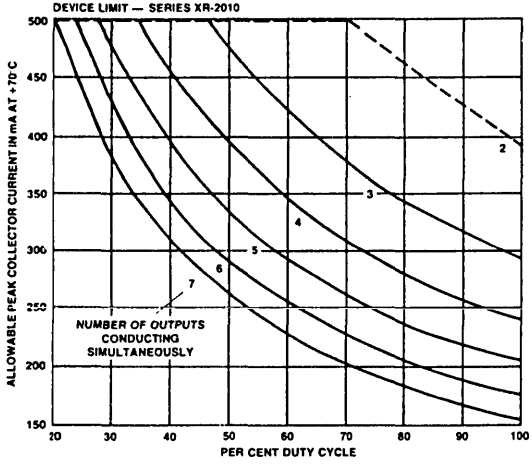


Figure 4. Peak Collector Current as a Function of Duty Cycle and Number of Outputs

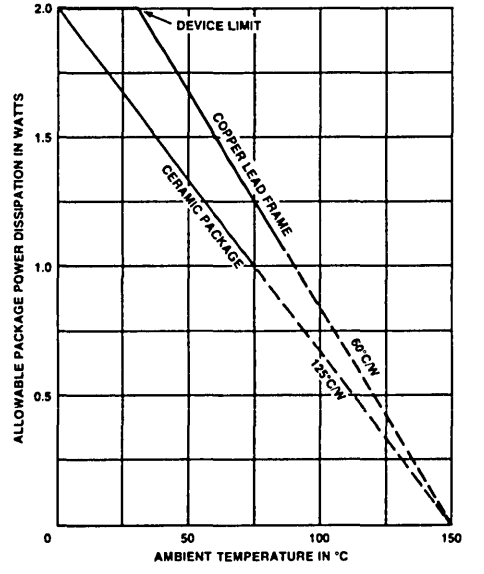


Figure 5. Allowable Average Power Dissipation as a Function of Ambient Temperature

TYPICAL APPLICATIONS

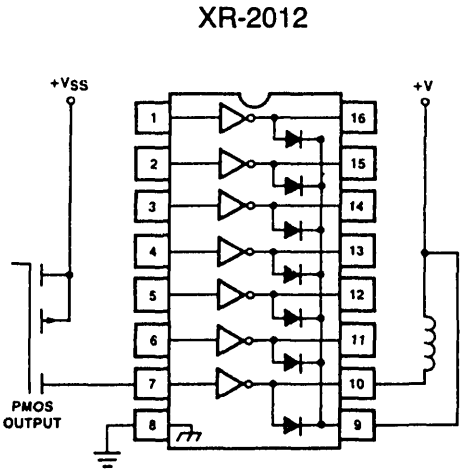


Figure 6. PMOS to Load

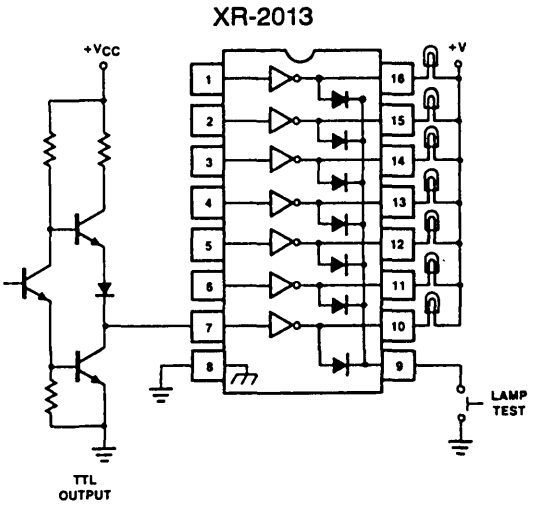


Figure 7. TTL to Load

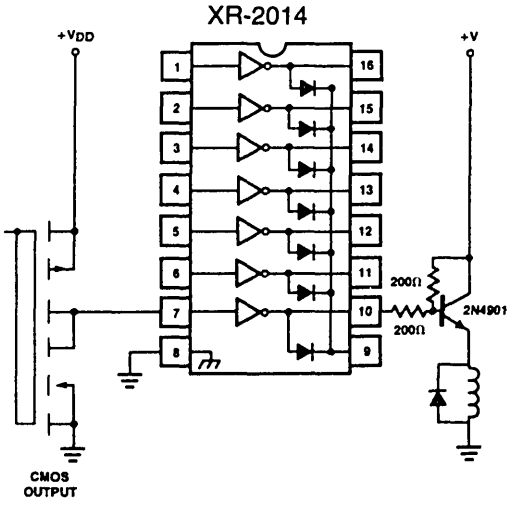


Figure 8. Buffer for Higher Current Loads

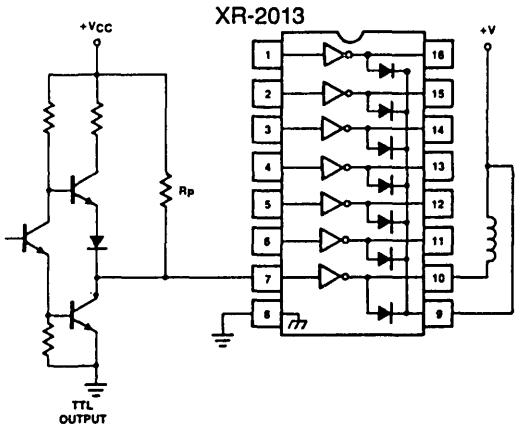


Figure 9. Use of Pull-up Resistors to Increase Drive Current

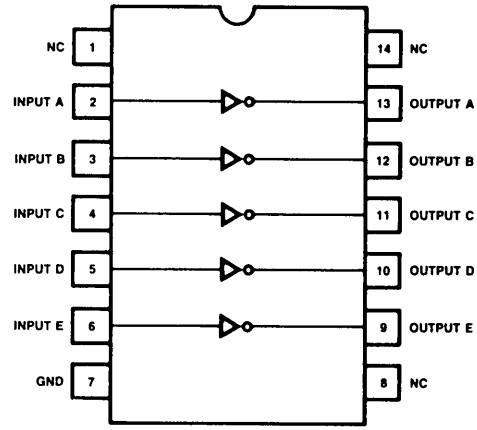
7

Hammer Driver

GENERAL DESCRIPTION

The XR-2200 is an array of five Darlington transistor pairs which are capable of driving high-current loads such as solenoids, relays, and LED's. Each of the five circuits contained on the XR-2200 is capable of sinking up to 400 mA. The XR-2200 was specifically designed for use with 14 V to 25 V PMOS devices.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Output Capability of 400 mA for Each Driver
Drivers may be used in parallel for increased output drive capability.
Input is directly compatible with PMOS outputs

APPLICATIONS

Printing Calculator Hammer Driver
High Current LED Driver
Solenoid and Relay Driver
Tungsten Lamp Driver
High Current Switch

ORDERING INFORMATION

Part Number	Package Type	Operating Temperature
XR-2200 CP	Plastic	−25°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Collector to Base Voltage	30V
Collector to Emitter Voltage	30V
Emitter to Base Voltage	5.5V
Collector Current	450 mA
Input Terminal Breakdown Voltage (plus)	30V
Input Terminal Breakdown Voltage (minus)	−0.5V
Power Dissipation	550 mW

SYSTEM DESCRIPTION

The XR-2200 hammer driver contains five Darlington connected transistor pairs, each capable of switching 30V. All five emitters are connected to a common ground (Pin 7). With a guaranteed current gain of 2000, each section of the XR-2200 can sink 400 mA.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Power Supply Voltage			26	Vdc	
Output Leakage Current			100	μA	V_{CE} = 26 V, V_{IN} = 0 V
Output Current One Driver			400	mA	
Output Current 5 Drivers					See Figure 2
Output Saturation Voltage			2.2	Vdc	I_{OUT} = 400 mA V_{IN} = 17 V I_{OUT} = 200 mA V_{IN} = 17 V
Current Gain	2000				V_{CE} = 3 V I_{OUT} = 200 mA
Input Current		0.7		mA	V_{IN} = 17 V I_{OUT} = 0 mA

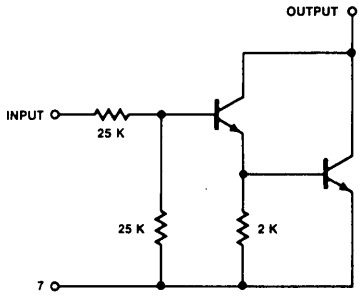


Figure 1. Schematic Diagram (1 of 5 Circuits Shown)

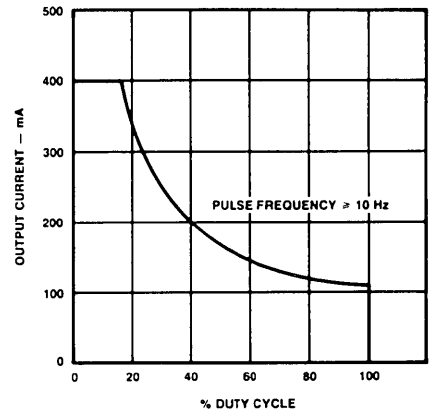


Figure 2. Maximum Permissible Output Current per Driver vs Duty Cycle with 5 Drivers Pulsed Simultaneously.

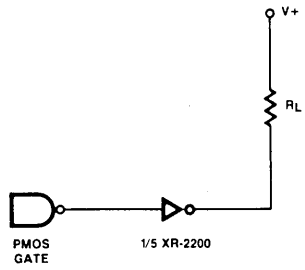


Figure 3. Circuit Connection for Driving Non-Inductive Loads

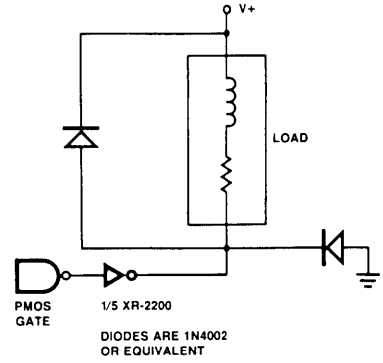


Figure 4. Circuit Connection for Driving Inductive Loads. NOTE: The XR-2200 may be damaged if the diodes are omitted when driving an inductive load.

High-Voltage, High-Current Darlington Transistor Arrays

GENERAL DESCRIPTION

The XR-2201, XR-2202, XR-2203, and XR-2204 Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a single monolithic substrate. All units feature open-collector outputs and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA are allowable, making them also ideal for driving tungsten filament lamps. Although the maximum continuous collector current rating is 500mA for each driver, the outputs may be paralleled to achieve higher load current capability.

FEATURES

High Peak Current Capability—600mA
Internal Protection Diodes for Driving Inductive Loads
Directly Compatible with TTL, CMOS, PMOS, and DTL Logic Families
Exact Replacement for Sprague Types ULN-2001A, ULN-2002A, ULN-2003A, and ULN2004A

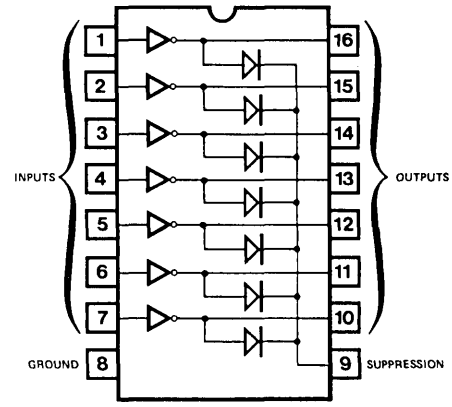
APPLICATIONS

Relay Drivers
Solenoid Drivers
High Current Inverters

ABSOLUTE MAXIMUM RATINGS T_A = 25°C

Output Voltage, V_{CE}	50V
Input Voltage, V_{IN}	30V
Emitter-Base Voltage, V_{EBO}	6V
Continuous Collector Current, I_C (Each Driver)	500mA
Continuous Base Current, I_B (Each Driver)	25mA
Power Dissipation, P_D (Each Driver)	1.0W
(Total Package)	2.0W
Derate Above 25°C	16.67 mW/°C
Storage Temperature Range	−55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2201CP	Plastic	0°C to +85°C
XR-2202CP	Plastic	0°C to +85°C
XR-2203CP	Plastic	0°C to +85°C
XR-2204CP	Plastic	0°C to +85°C

SYSTEM DESCRIPTION

The XR-2201 is compatible with most common logic forms, including PMOS, CMOS, and TTL. It requires a current-limiting resistor placed in series with the input to limit base current to less than 25mA.

The XR-2202 is designed for direct compatibility with 14V-25V PMOS devices.

The XR-2203 is compatible with TTL or CMOS operating at 5 volts. Each input has a series base resistor to limit the input current to a safe value.

The XR-2204 is designed for direct operation from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V.

With all four devices, the load should be connected between the driver output and $+V_{CC}$. For protection from transient voltage spikes, Pin 9 should be connected to $+V_{CC}$.

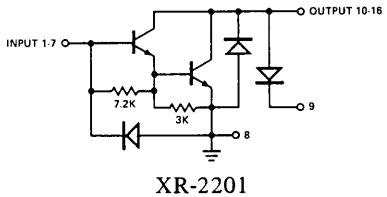
ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C unless otherwise noted

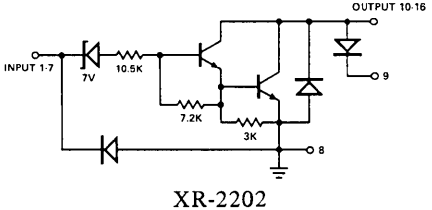
PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Output Leakage Current			100	μA	V_{CE} = 50 V, T_A = 70°C
XR-2202			500	μA	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6V
XR-2204			500	μA	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1V
Collector-Emitter Saturation Voltage		1.25	1.6	V	I_C = 350mA, I_B = 500μA
		1.1	1.3	V	I_C = 200mA, I_B = 350μA
		0.9	1.1	V	I_C = 100mA, I_B = 250μA
Input Current					
XR-2202		0.85	1.3	mA	V_{IN} = 17V
XR-2203		0.93	1.35	mA	V_{IN} = 3.85V
XR-2204		0.35	0.5	mA	V_{IN} = 5V
		1.0	1.45	mA	V_{IN} = 12V
Input Current	50	65		μA	I_C = 500μA, T_A = 70°C
Input Voltage					
XR-2202			13	V	V_{CE} = 2V, I_C = 300mA
XR-2203			2.4	V	V_{CE} = 2V, I_C = 200mA
			2.7	V	V_{CE} = 2V, I_C = 250mA
			3.0	V	V_{CE} = 2V, I_C = 300mA
XR-2204			5.0	V	V_{CE} = 2V, I_C = 125 mA
			6.0	V	V_{CE} = 2V, I_C = 200mA
			7.0	V	V_{CE} = 2V, I_C = 275mA
			8.0	V	V_{CE} = 2V, I_C = 350mA
D-C Forward Current Transfer Ratio XR-2201	1000				V_{CE} = 2V, I_C = 350mA
Input Capacitance		15	30	pF	
Turn-On Delay		1.0	5	μS	0.5 E_{IN} to 0.5 E_{OUT}
Turn-Off Delay		1.0	5	μS	0.5 E_{IN} to 0.5 E_{OUT}
Clamp Diode Leakage Current			50	μA	V_R = 50V
Clamp Diode Forward Voltage		1.7	2	V	I_F = 350mA

7

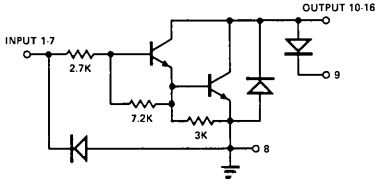
SCHEMATIC DIAGRAMS (One of 7 Identical Drivers is shown for each device.)



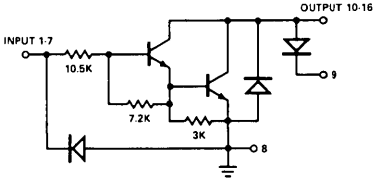
XR-2201



XR-2202



XR-2203



XR-2204

EXAR

Section 8 – Special Function Circuits

Multi-Function PLL System

GENERAL DESCRIPTION

The XR-S200 integrated circuit is a highly versatile, multipurpose circuit that contains all of the essential functions of most communication system designs on a single monolithic substrate. The function contained in the XR-S200 include: 1. a four quadrant analog multiplier, 2. a high frequency voltage controlled oscillator (VCO) and 3. a high performance operational amplifier.

The three functions can be used independently, or directly interconnected in any order to perform a large number of complex circuit functions, from phase-locked loops to the generation of complex waveforms. The XR-S200 can accommodate both analog and digital signals, over a frequency range of 0.1 Hz to 30 MHz, and operate with a wide choice of power supplies extending from ±3 volts to ±30 volts.

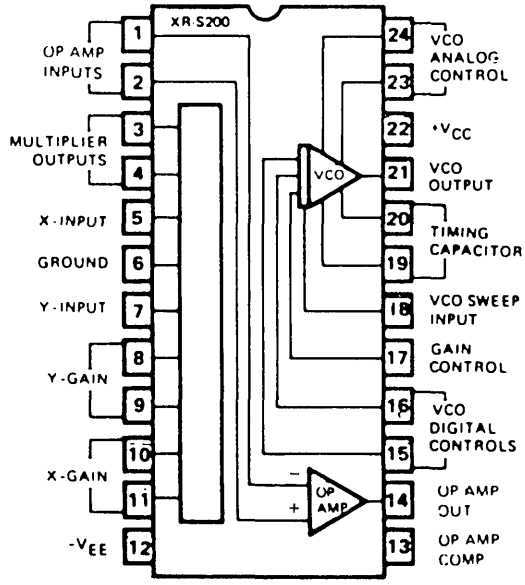
FEATURES

Wide VCO Frequency Range	0.1 Hz to 30 MHz
Wide Supply Voltage Range	±3V to ±30 V
Uncommitted Inputs and Outputs for Maximum Flexibility	
Large Input Dynamic Range	

APPLICATIONS

Phase-locked loops
FM demodulation
  Narrow and wideband FM
  Commercial FM-IF
  TV sound and SCA detection
FSK detection (MODEM)
PSK demodulation
Signal conditioning
Tracking filters
Frequency synthesis
Telemetry coding/decoding
AM detection
  Quadrature detectors
  Synchronous detectors
Linear sweep & AM generation
  Crystal controlled
  Suppressed carrier
  Double sideband
Tone generation/detection
Waveform generation
  Single/square/triangle/sawtooth
Analog multiplication

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply	30 Volts
Power Dissipation	900 mW
Derate above +25°C	5 mW/°C
Temperature	
Operating	−55°C to +125°C
Storage	−65°C to +150°C
Input Signal Level, V_S	6 V,p-p

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-S200	Ceramic	0°C to +70°C

ELECTRICAL SPECIFICATIONS (T = 25°C, V_{SUPPLY} = ±10V)

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
MULTIPLIER SECTION: See Figure 2, R_X = R_Y = 15k, Pins 1, 2, 6, 23, 24 Grounded.					
Output Offset Voltage		±40	±120	mV	$V_X = V_Y = 0$, $V_{IO} = \lvert V_3 - V_4 \rvert$
Input Bias Current		5	15	μA	Measured at pins 5 and 7
Input Offset Current		0.1	1.0	μA	Measured at pins 5 and 7
Linearity					
(Output error, %		1.0		%	$-5 < V_X < +5$, V_Y = ±5V
of full scale)		1.5		%	$-5 < V_Y < +5$, V_X = ±5V
Scale Factor, K_M		0.1		–	$K_M = 25/R_XR_Y$ (Adjustable)
Input Resistance	0.3	1.0		MΩ	f = 20 Hz, Measured at pins 5 and 7
3 dB Bandwidth	3	6		MHz	$C_L \leq 5$ pF
Phase detection B.W.	50	100		MHz	$R_X = R_Y = 0$
Differential Output Swing	±4	±6		V p-p	Measured across pins 3 and 4
Output Impedance					
Single Ended		6		kΩ	Measured at pins 3 and 4
Differential		12		kΩ	
OPERATIONAL AMPLIFIER SECTION: See Figure 10 and 11, R_L = 20k, C_L = 550 pF.					
Input Bias Current		0.08	0.5	μA	
Input Offset Current		0.02	0.2	μA	
Input Offset Voltage		1.0	6.0	mVdc	
Differential Input Impedance					Open loop, f = 20 Hz
Resistance	0.4	2.0		MΩ	
Capacitance		1.0		pF	
Common Mode Range		±8		V	
Common Mode Rejection	70	90		dB	f = 20 Hz
Open Loop Voltage Gain	66	80		dB	
Output Impedance		2		kΩ	
Output Voltage Swing	±7	±9		V	$R_L \geq 20$ kΩ
Power Supply Sensitivity		30		μV/V	$R_S \leq 10$ kΩ
Slew Rate		2.5		V/μsec	A_V = 1, C_L = 10 pF
VCO SECTION: See Figure 11, R_L = 10k, f_o = 1 MHz.					
Upper Frequency Limit	15	30		MHz	C_o = 10 pF
Sweep Range	8:1	10:1		–	f_o = 10 kHz, See Figure 14
					Digital Controls Off
Linearity					
(distortion for		.2	1.0	%	Digital Controls Off
Δf/f = 10%)					
Frequency Stability					$V_{CC} > 8V$, f_o = 1 MHz
Power Supply		0.08	0.5	%/V	Sweep Input Open
Temperature		300	650	ppm/°C	
Analog Input Impedance					Measured at pins 23 and 24
Resistance	0.1	0.5		MΩ	
Capacitance		1.5		pF	
Output Amplitude		3		V p-p	Squarewave
Output Rise Time		15		ns	C_L = 10 pF, R_L = 5 kΩ
Fall Time		20		ns	
Input Common Mode Range	+6	+8		Vdc	
	−4	−6		Vdc	

CAUTION: When using only some of the blocks within the XR-S200, the input terminals to the unused section must be grounded (for split-supply operation); or connected to an ac ground biased at $V^+/2$ (for single supply operation).

8

XR-S200

XR-S200 ANALOG MULTIPLIER SECTION

The analog multiplier in the XR-S200 (Figure 2) provides linear four-quadrant multiplication over a broad range of input signal levels. It also serves as a balanced modulator, phase comparator, or synchronous detector. Gain is externally adjustable. Nonlinearity is less than 2% of full scale output.

TYPICAL APPLICATIONS OF MULTIPLIER SECTION

- Analog multiplication/division
- Phase detection
- Balanced modulation/demodulation
- Electronic gain control
- Synchronous detection
- Frequency doubling

ANALOG MULTIPLICATION

The XR-S200 multiplier section can be combined with the amplifier section to perform analog multiplication without the need for dc level shifting between input and output. The amplifier functions as an operational amplifier with a single-ended output at ground level when connected as shown in Figure 3.

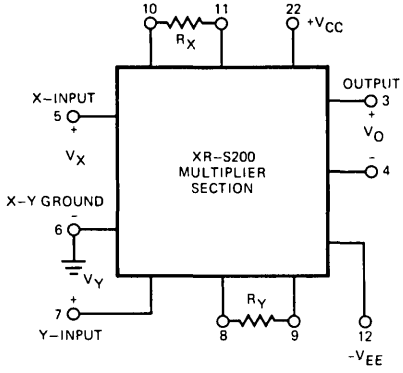


Figure 2. XR-S200 Multiplier Section

PHASE COMPARATOR

For phase comparison, a low-level reference signal is normally applied to one input and a high-level reference or carrier signal to the other input, as in Figure 4. The signal may be applied to either the X or Y input, since the response is symmetrical.

If the two inputs, $V_R(t)$ and $V_S(t)$ are at the same frequency, then the dc voltage at the output of the phase comparator can be related to the phase angle ϕ between the two signals as

$$V_\phi = K_\phi \cos\phi$$

where K_ϕ is the conversion gain in volts per radian (Figure 5). For phase comparator applications, one input is

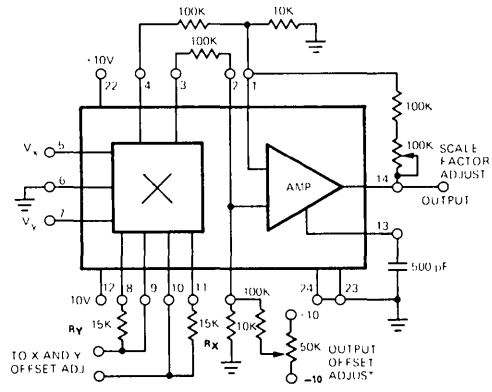


Figure 3. Analog Multiplication

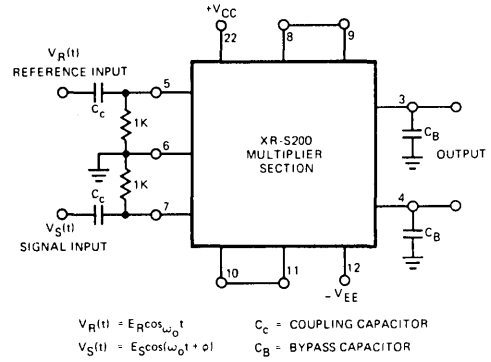


Figure 4. XR-S200 Multiplier Section as a Phase Comparator

normally a high level reference signal and the other input a low level information signal. Since the XR-S200 multiplier section offers symmetrical response with respect to the X and Y inputs, either input can be used as the carrier or signal input. For low input levels, the conversion gain is proportional to the input signal amplitude. For high level inputs, (V_S > 40 mV, rms) K_ϕ is constant and approximately equal to 2V/rad.

SUPPRESSED-CARRIER AM

The multiplier generates suppressed-carrier AM signals when connected as in Figure 6. Again, the symmetrical response allows the X or Y inputs to be used interchangeably as the carrier or modulation inputs. The X and Y offset adjustments optimize carrier suppression. Gain control resistors R_X and R_Y typically range from 1 KΩ to 10 KΩ, depending on input signal amplitudes. The values shown give approximately 60 dB carrier suppression at 500 kHz and 40 dB at 10 MHz.

DOUBLE-SIDEBAND AM GENERATION

The connection for double-sideband AM generation is shown in Figure 7. The dc offset adjustment on the modulation input terminal sets the carrier output level, while the dc offset of the carrier input governs symmetry of the output waveform. The modulation input can also be used as a linear gain control (AGC), to control amplification with respect to the carrier input signals.

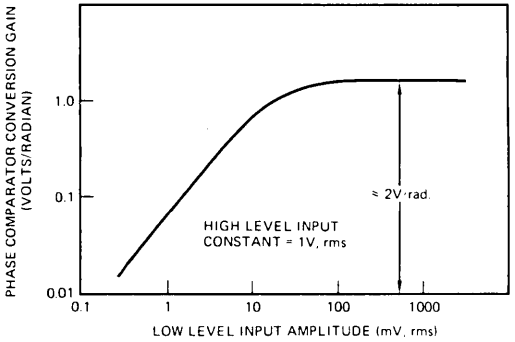


Figure 5. Phase Comparator Conversion Gain Versus Input Amplitude

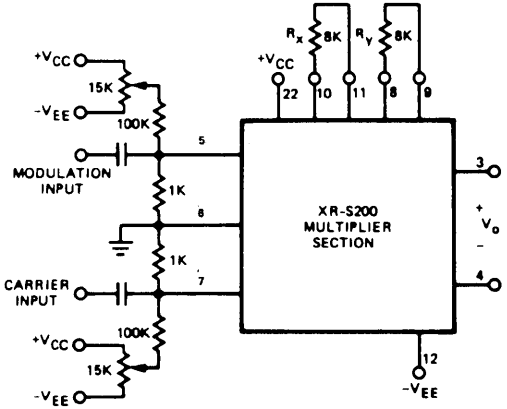


Figure 6. Suppressed Carrier Modulation Using XR-S200 Multiplier Section

FREQUENCY DOUBLING

Figure 8 shows how to double a sinusoidal input signal of frequency f_S to produce a low-distortion sinewave output of $2f_S$. Total harmonic distortion is less than 0.6% with an input of 4V, p-p, at 10 kHz and an output of 1V, p-p, at 20 kHz. The multiplier's X and Y offsets are nulled as shown to minimize the output's harmonic content.

SYNCHRONOUS AM DETECTION

A typical synchronous AM detector is shown in Figure 9. The signal is applied to the multiplier common input and the X and Y inputs are grounded. Since the Y input

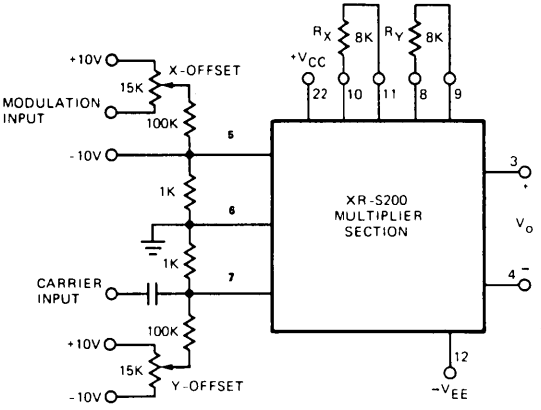


Figure 7. Double Sideband Amplitude Modulation Using XR-S200 Multiplier Section

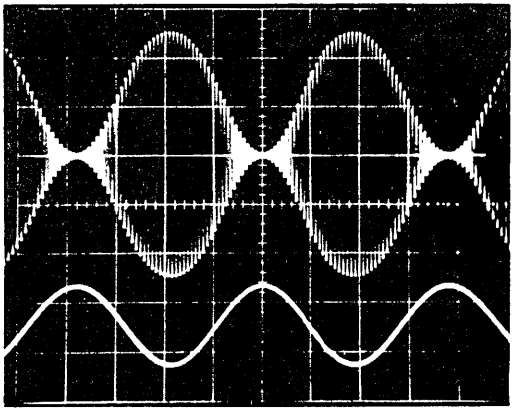


Figure 7-1. AM Modulation, 95% AM, f_c = 50 kHz, f_m = 1 kHz

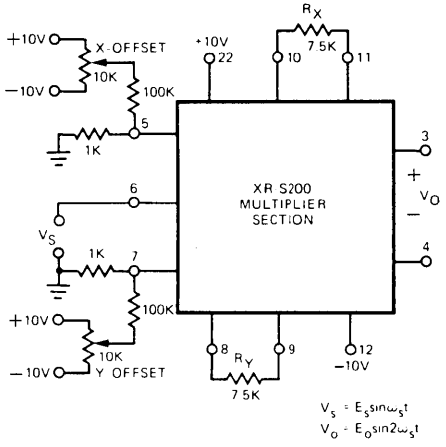


Figure 8. Multiplier Section as Frequency Doubler

operates at maximum gain with R_Y = 0, the detector gain and demodulated output linearity are determined by R_X. An R_X range of 1 KΩ to 10 KΩ is recommended for carrier amplitudes of 100 mV, p-p; or greater. The multiplier output can be low-pass filtered to obtain the demodulated output. Figure 9-1 shows the carrier and modulated waveforms for a 30% modulated input signal with a 10 MHz carrier and 1 kHz modulation.

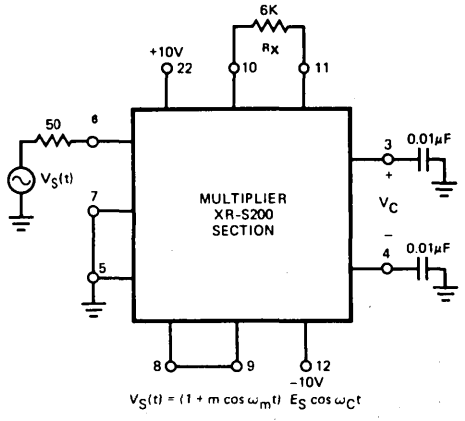


Figure 9. Synchronous AM Detector

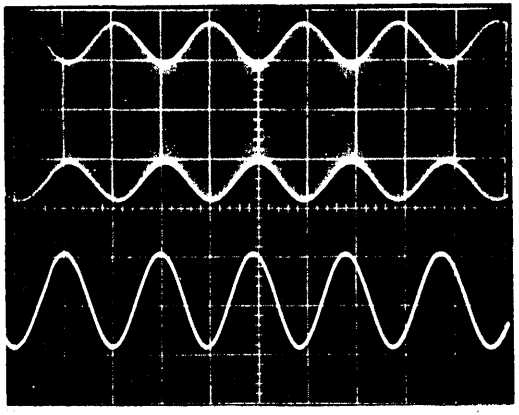


Figure 9-1. Synchronous AM Demodulation

XR-S200 AMPLIFIER SECTION

This multi-purpose function (Figure 10) can be used as a general-purpose operational amplifier, high-speed comparator, or sense amplifier. It features an input impedance of 2 megohms, high voltage gain, and a slew rate of 2.5V/microsecond. The frequency response curves for the amplifier section are also shown in Figure 10.

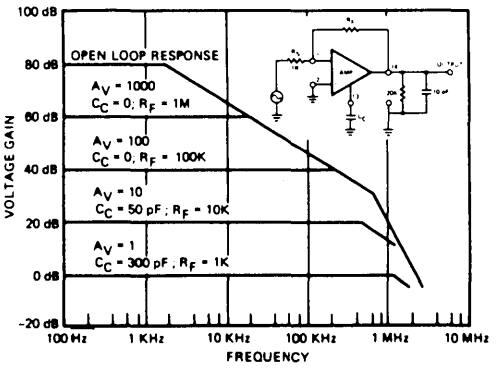


Figure 10. Amplifier Section Frequency Response

XR-S200 OSCILLATOR SECTION

The voltage-controlled oscillator section, (Figure 11) is an exceptionally versatile design capable of operating from a fraction of a cycle to in excess of 40 MHz. Frequencies can be selected and controlled by three methods, and used in various combinations for different applications:

1. External timing capacitor C_0 tunes the VCO to a center frequency between 0.1 Hz and 40 MHz. The free-running frequency is inversely proportional to C_0. (see Figure 12)

2. Two digital control inputs allow four discrete frequencies to be selected at any center frequency. The digital inputs convert the logic signal voltages to internal control currents. (see Figure 13)

3. A sweep voltage, applied through a limiting resistor R_S is used for frequency sweeping, on-off keying, and synchronization of the VCO to a sync pulse. (see Figure 14)

The voltage-to-frequency conversion of the VCO section is highly linear. In addition, the conversion gain can be controlled through the analog control input. Gain is inversely proportional to R_0. When the digital controls are also used, gain decreases as the frequency is stepped up.

The VCO interfaces easily with ECL or TTL logic. It can be converted to a highly stable crystal-controlled oscillator by simply substituting a crystal in place of the timing capacitor, C_0.

Typical performance characteristics of the VCO section are shown in Figures 12, 13, and 14.

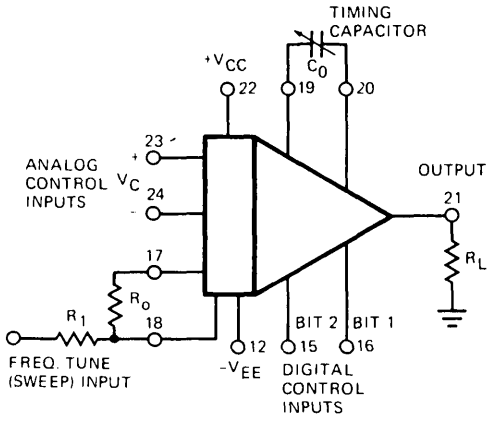


Figure 11. XR-S200 Oscillator Section

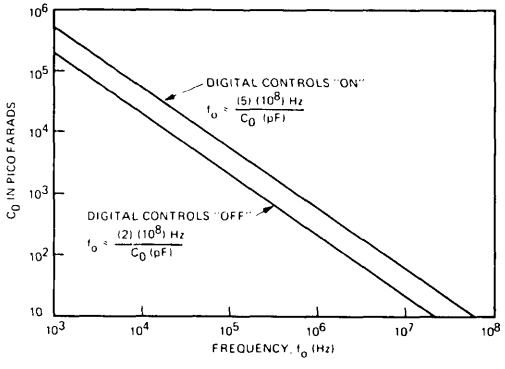


Figure 12. VCO Frequency as a Function of Timing Capacitor, C_0

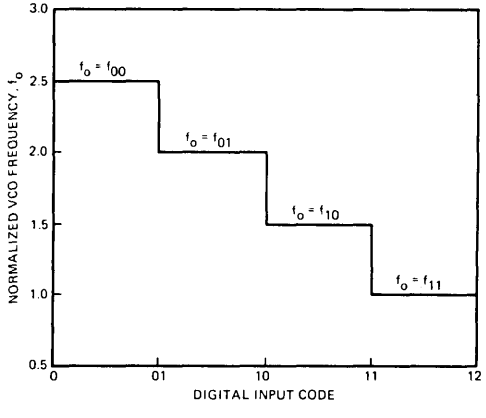


Figure 13. VCO Digital Tuning Characteristics

EXPLANATION OF VCO DIGITAL CONTROLS

The VCO frequency is proportional to the total charging current, I_T, applied to the timing capacitor. As shown in Figure 15, I_T is comprised of three separate components: I_0, I_1, and I_2, which are contributed by transistors T_0, T_1, and T_2, respectively. With pins 15 and 16 open circuited, these currents are interrelated as

$$I_0 = I_1 = 2I_2$$

Currents I_1 and I_2 can be externally controlled through pins 16 and 15 respectively. By increasing the dc level at either of these pins, T_1 or T_2 can be turned "off" and I_1 or I_2 can be reduced to zero. With reference to Figure 15, this can be done by applying a 3 volt logic pulse to these pins, through disconnect diodes D_1 and D_2. In this manner, the VCO frequency can be stepped in four discrete intervals, over a frequency range of 2.5:1, as shown in Figure 13.

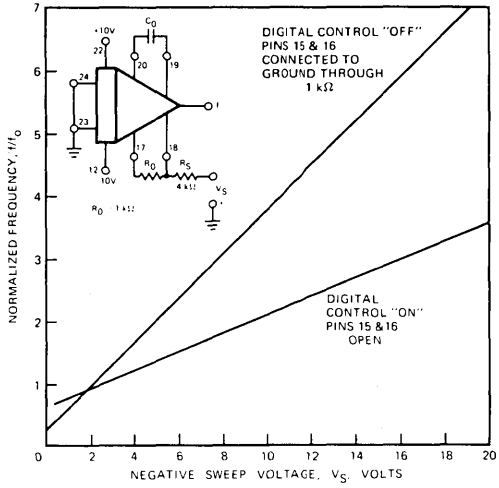


Figure 14. Voltage Sweep Characteristics

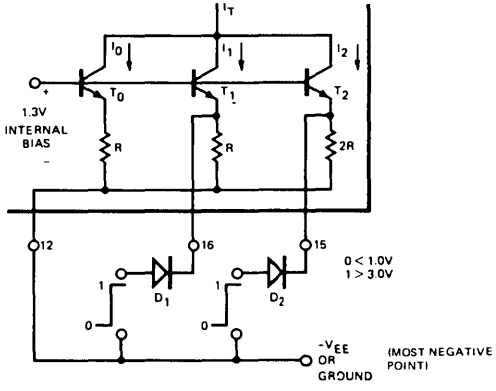


Figure 15. Explanation of VCO Digital Controls

TYPICAL APPLICATIONS OF VCO SECTION

- Voltage/frequency conversion
- Phase-locked loops
- Frequency synthesis
- Signal conditioning
- Carrier generation
- Synchronization
- Sweep and FM generator
- Crystal oscillator
- Waveform generator
- Keyed oscillator

APPLICATIONS OF THE XR-S200 SYSTEM

PHASE-LOCKED LOOP

A self-contained phase-locked loop is formed by connecting the XR-S200 as outlined in Figure 16.

In most PLL applications, the amplifier is available for functions useful outside the loop, since the phase comparator (multiplier section) and VCO provide sufficient conversion gain. In this case, the amplifier gain does not enter the PLL gain expression. Assuming unity dc gain for the filter, the PLL loop gain is $K_T = K_\phi K_O$ where K_ϕ and K_O are the multiplier and VCO conversion gains, respectively.

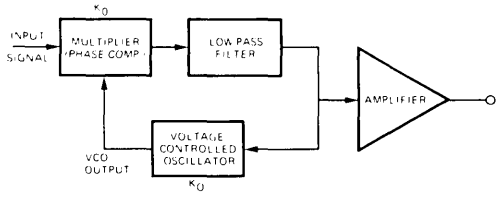


Figure 16. XR-S200 as a Phase-Locked Loop

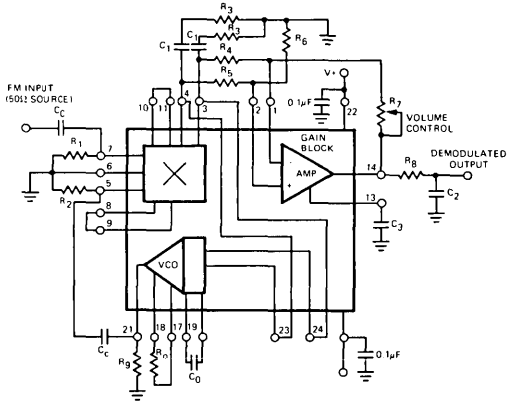


Figure 17. Circuit Connection for FM Detection

FREQUENCY-SELECTIVE FM DEMODULATION

For FM demodulation, the PLL connection is used (Figure 17.) The multiplier, with its gain terminals shorted, serves as the phase detector, and the VCO and filter govern the operating frequencies.

The gain block is used as an audio preamplifier to set the demodulated output signal level. Volume is controlled by the variable feedback resistor R_7. If R_6 equals R_7, the dc output level will be very close to ground, for circuit operation with split power supplies. C_3 is the amplifier's compensation capacitor. R_8 and C_2 set the output de-emphasis time constant T_D, which is normally 75 μsec. for commercial FM applications (f_O = 10.7 MHz).

FSK DETECTION

FSK signals are detected and demodulated with the PLL connection, as well. It is shown in Figure 18 as a monolithic MODEM suitable for Bell 103 or 202 type data sets operating at data rates to 1800 baud. An input frequency shift corresponding to a data bit causes the multiplier's dc voltage output to reverse polarity. The dc level is changed to a binary output pulse by the gain block, connected as a voltage comparator.

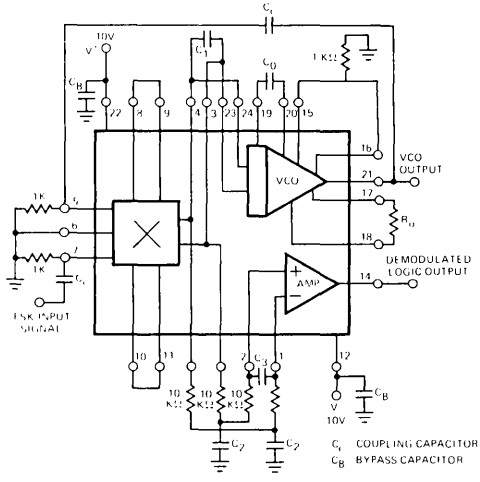


Figure 18. FSK Detection

FREQUENCY SYNTHESIZER

Frequency synthesis is performed in Figure 19 by a phase-locked loop closed with a programmable counter or digital divide-by-N circuit inserted into the feedback loop. The VCO frequency is divided by N, so that when the circuit locks to an input signal at frequency f_S, the

oscillator output is Nf_S. A large number of discrete frequencies can be synthesized from a given reference frequency by changing N.

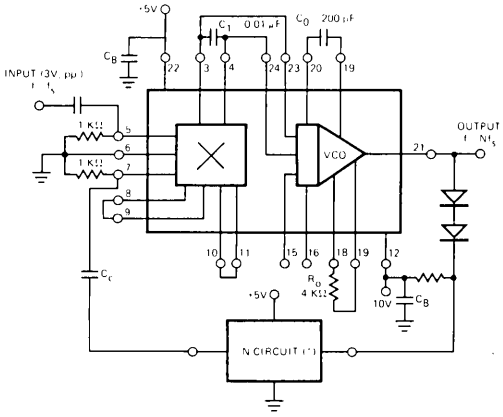


Figure 19. Frequency Synthesizer

TRACKING FILTER AND WIDEBAND DISCRIMINATOR

In tracking filter applications, the XR-S200 again forms a PLL system (Figure 20). When the PLL locks on an input signal, it functions as a "frequency-filter" and produces a filtered version of the input signal frequency at the VCO output. Since it can track the input over a broad range of frequencies around the VCO free-running frequency, it is also called a "tracking filter". The system can track input signals over a 3:1 frequency range.

WAVEFORM GENERATOR

The XR-S200 can also be interconnected to form a versatile waveform generator. The typical circuit shown in Figure 21 generates the basic periodic square (or sawtooth) waveform. The multiplier section, connected as a linear differential amplifier, convert the differential sawtooth waveform input into a triangle wave output at pins

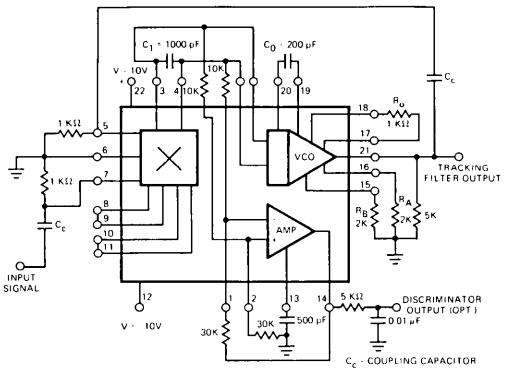


Figure 20. Recommended Circuit Connection for Tracking Filter Application (f_0 = 1 MHz)

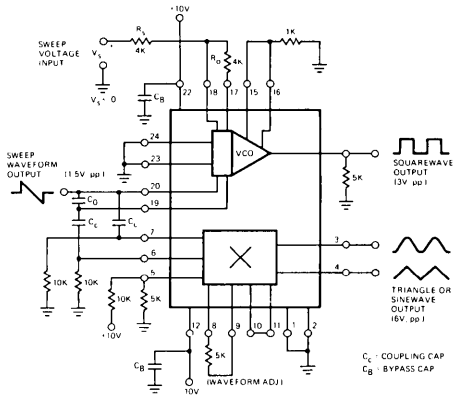


Figure 21. Waveform Generator Typical Circuit Connection Diagram

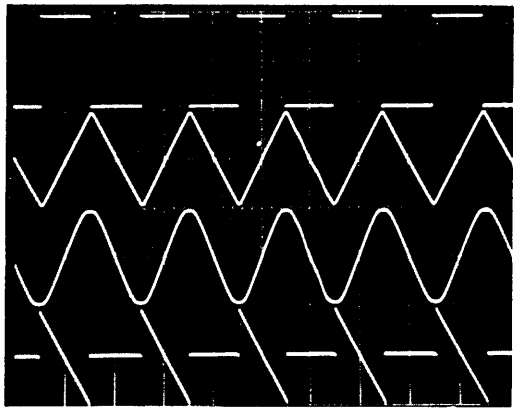


Figure 21-1. Basic Waveforms Available from XR-S200

3 and 4. The waveform adjustment pot across pins 8 and 9 can be used to round the peaks of the triangle waveform and convert it to a low distortion sinewave (THD < 2%). Terminals 3 and 4 can be used either differentially or single endedly to provide both in-phase and out-of-phase output waveforms.

The output frequency can be swept or frequency modulated by applying the proper analog control input to the circuit. For linear FM modulation with relatively small frequency deviation ($\Delta f/f < 10\%$) the modulation input can be applied across terminals 23 and 24. For large deviation sweep inputs, a negative going sweep voltage, V_S, can be applied to pin 18.

This allows the frequency to be voltage-tuned over approximately a 10:1 range in frequency. The digital control inputs (15 and 16) can be used for frequency-shift-keying (FSK) applications. They can be disabled by connecting them to ground through a current-limiting resistor.

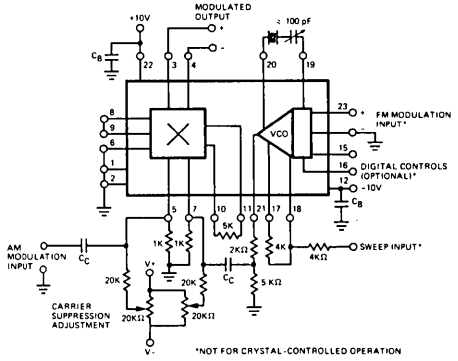


Figure 22. Circuit Connection for AM/FM or Crystal-Controlled AM Generator Application

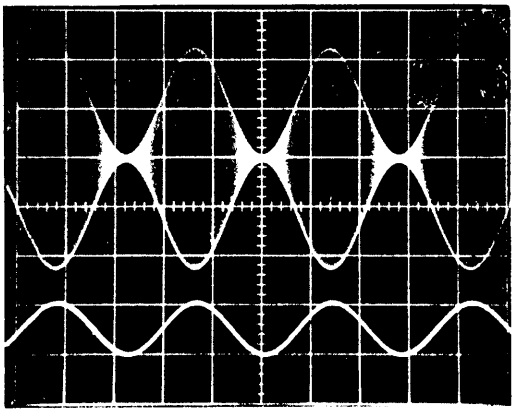


Figure 22-1. Double Sideband AM Output Waveform $f_{carrier}$ = 3.688 MHz f_{mod} = 1 kHz (90% modulation)

AM & FM SIGNAL GENERATION

The oscillator and multiplier sections can be interconnected as a general purpose radio-frequency signal generator with AM, FM and sweep capability as shown in Figure 22.

The oscillator section can be used as a voltage-tuned, variable frequency oscillator, or as a highly stable carrier or reference generator by connecting a reference crystal across terminals 19 and 20. In this case, a small capacitor (typically 10 to 100 pF) fine tunes the crystal frequency. The multiplier section introduces the amplitude modulation on the carrier signal generated by the VCO. The balanced nature of the multiplier allows suppressed carrier as well as double sideband modulation (Figures 22-1 and 22-2). Typical carrier suppression is in excess of 40 dB for frequencies up to 10 MHz.

If a timing capacitor is used instead of a crystal, the oscillator section can provide highly linear FM or frequency sweep. The digital control terminals of the oscillator are used for frequency-shift-keying.

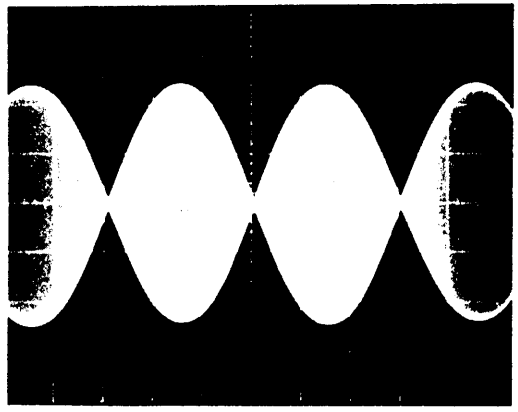
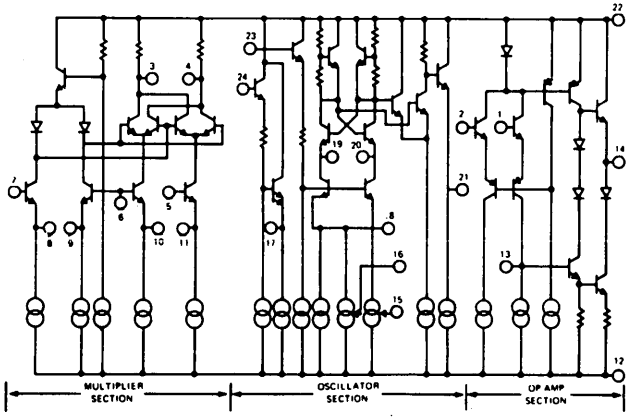


Figure 22-2. Suppressed Carrier AM Output Waveform $f_{carrier}$ = 3.688 MHz f_{mod} = 1 kHz



EQUIVALENT SCHEMATIC DIAGRAM

Stereo Demodulator

GENERAL DESCRIPTION

The XR-1310 is a unique FM stereo demodulator which uses phase-locked techniques to derive the right and left audio channels from the composite signal. Using a phase-locked loop to regenerate the 38 kHz subcarrier, it requires no external L-C tanks for tuning. Alignment is accomplished with a single potentiometer.

FEATURES

Requires No Inductors
Low External Part Count
Simple, Noncritical Tuning by Single Potentiometer Adjustment
Internal Stereo/Monaural Switch with 100 mA Lamp Driving Capability
Wide Dynamic Range: 600 mV (RMS) Maximum Composite Input Signal
Wide Supply Voltage Range: 8 to 14 Volts
Excellent Channel Separation
Low Distortion
Excellent SCA Rejection

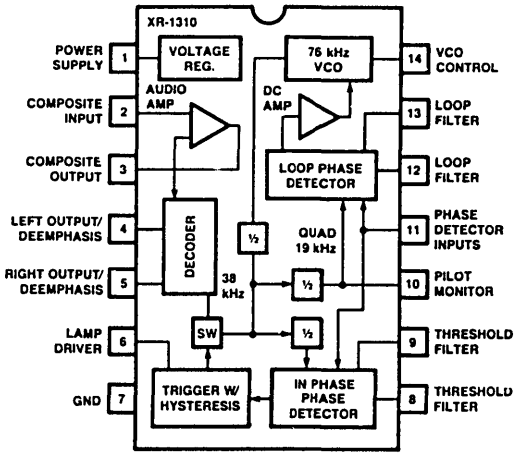
APPLICATIONS

FM Stereo Demodulation
Stereo Indicator

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)	
Power Supply Voltage	14V
Lamp Current (nominal rating, 12 V lamp)	75 mA
Power Dissipation (package limitation)	625 mW
Derate above T_A = +25°C	5.0 mW/°C
Operating Temperature Range (Ambient)	−40 to +85°C
Storage Temperature Range	−65 to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1310CP	Plastic	−40°C to +85°C

SYSTEM DESCRIPTION

The XR-1310 is a complete stereo demodulator specifically designed for transforming a composite FM stereo signal into its left and right channel components.

The composite FM stereo input signal, from the receiver detector, is applied to the buffer amplifier, Pin 2. Buffered output (gain = 1) is applied to the L+R, L−R decoder.

The VCO of the PLL runs at 76 kHz, four times the 19 kHz pilot frequency. Free-running frequency is set by the parallel RC circuit on Pin 14. The VCO output drives a controlled switch which allows demodulation. When the PLL is locked, the lamp driver open collector output (Pin 6) can sink up to 100 mA.

Left and right channel outputs are taken from Pins 4 and 5 respectively. De-emphasis is performed by the RC circuit here; slightly higher gain is possible by increasing the resistor size, but the RC product should remain constant.

XR-1310

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise noted; V_{CC}* = +12 Vdc, T_A = +25°C, 560 mV (RMS) (2.8 Vp-p) standard multiplex composite signal with L or R channel only modulated at 1.0 kHz and with 100 mV (RMS) (10% pilot level), using circuit of Figure 1.

PARAMETERS	MIN	TYP	MAX	UNIT
Maximum Standard Composite Input Signal (0.5% THD)	2.8			Vp-p
Maximum Monaural Input Signal (1.0% THD)	2.8			Vp-p
Input Impedance		50		kΩ
Stereo Channel Separation (50 Hz — 15 KHz)	30	40		dB
Audio Output Voltage (desired channel)		485		mV (RMS)
Monaural Channel Balance (pilot tone "off")			1.5	dB
Total Harmonic Distortion		0.3		%
Ultrasonic Frequency Rejection 19 kHz 38 kHz		34.4 45		dB
Inherent SCA Rejection (f = 67 kHz; 9.0 kHz beat note measured with 1.0 kHz modulation "off")		80		dB
Stereo Switch Level (19 kHz input for lamp "on") Hysteresis	13	 6	20	mV (RMS) dB
Capture Range (permissable tuning error of internal oscillator, reference circuit values of Figure 1)		±3.5		%
Operating Supply Voltage (loads reduced to 2.7 kΩ for 8.0-volt operation)	8.0		14	Vdc
Current Drain (lamp "off")		13		mAdc

*Symbols conform to JEDEC Engineering Bulletin No. 1 where applicable.

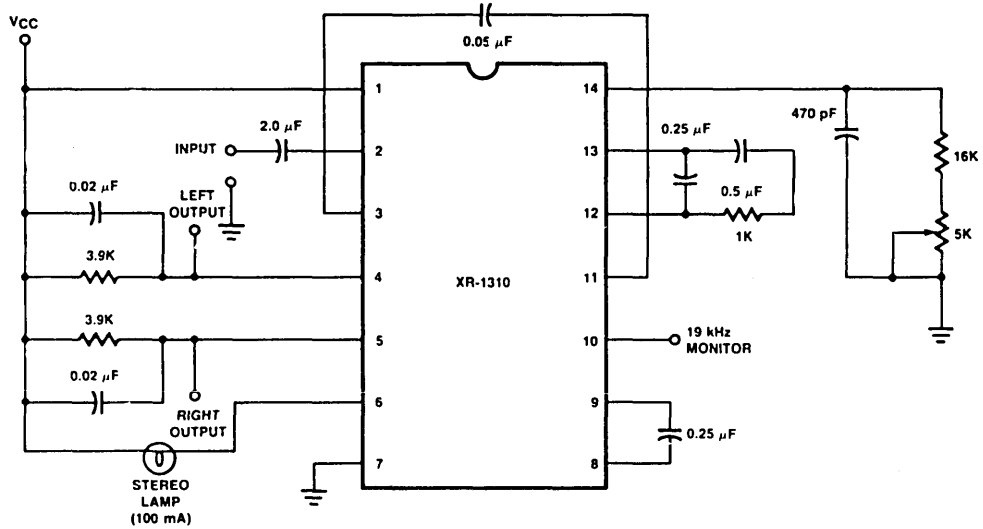


Figure 1. Typical Application

Monolithic Compandor

GENERAL DESCRIPTION

The XR-2216 is a monolithic audio frequency compandor designed to compress or expand the dynamic range of speech or other analog signals transmitted through telecommunication systems. The monolithic circuit can be connected as either a compressor or an expander, the choice being determined by the external circuitry.

FEATURES

Functions as either a Compressor or an Expander
Wide Dynamic Range: 60 dB
Wide Supply Range: 6 to 20 Volts
Excellent Transfer Function Tracking
Low Power Supply Drain
Controlled Attack and Release Times
Low Noise and Low Distortion

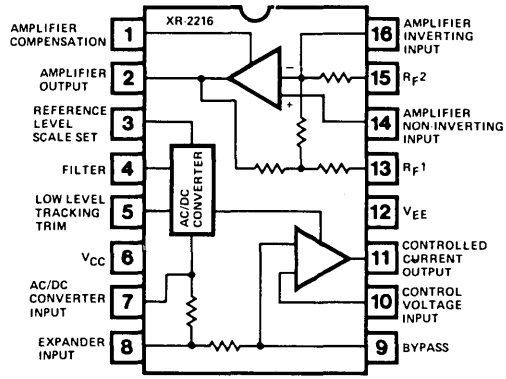
APPLICATIONS

Telephone Trunk—Line Compandor
Speech/Data Compression and Expansion
Telecommunication Systems
Mobile Communications
Model Data Processing

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20V
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mW/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature	−60°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package (16 Pin DIP)	Operating Temperature
XR-2216CN	Ceramic	−40°C to +60°C
XR-2216CP	Plastic	−40°C to +60°C

SYSTEM DESCRIPTION

The XR-2216 is comprised of four basic blocks: (1) an internal voltage reference; (2) an AC/DC converter which converts AC signal input to a DC current level; (3) an impedance converter whose impedance level is a function of a DC control signal; and (4) a high gain operational amplifier.

The XR-2216 is designed to accommodate a wide range of system configurations. It can be operated with positive or negative single supply systems, or dual power supplies over a power supply range of 6 volts to 20 volts.

XR-2216

ELECTRICAL CHARACTERISTICS

Test Conditions: V_C = +12V, T_A = 25°C

COMPANDOR

PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
Power Supply Voltage	6		20	VDC	
Nominal Power Supply Voltage	12		18	VDC	
Power Supply Current, No Signal Input			3	mA	
Gain Change Over Frequency Tolerance	−1		+1	dB	300 ~ 3500 Hz
Distortion Measured at −4 dB* Input Level at 1 KHz		3		% THD	
Attack Time Measured at −10 dB Input Level			5	ms	To 90% of Final Value
Decay Time Measured at −10 dB Input Level			5	ms	To 10% of Final Value
Transfer Characteristics** Compandor Output With Input Levels of:					
−4 dBm	3.5	+6	7.5	dBm	
−8 dBm	−0.5	+2	3.5	dBm	
−10 dBm	−1.5	0	+1.5	dBm	
−14 dBm (reference)		−4		dBm	
−24 dBm	−15.5	−14	−12.5	dBm	
−34 dBm	−25.5	−24	−22.5	dBm	
−44 dBm	−36.5	−34	−32.5	dBm	
−54 dBm	−49	−44	−42.5	dBm	
−64 dBm	−59	−54	−52.5	dBm	

COMPRESSOR

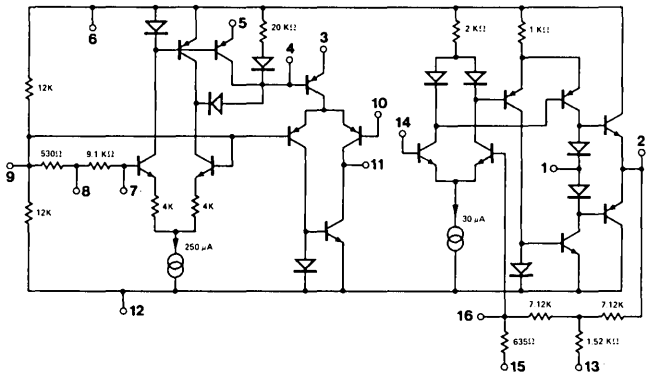
PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
Input Impedance	50			k ohm	
Output Impedance			50	ohm	
Output Signal Level for −10 dBm Input at 1 KHz		−10		dBm	
Output Voltage Swing	0			dB	
Output Noise, Input AC Grounded			30	dBrnc	
Compressor Transfer Characteristics** Compressor Output With Input Levels of:					
−4 dBm		−7		dBm	
−8 dBm		−9		dBm	
−10 dBm		−10		dBm	
−14 dBm (reference)		−12		dBm	
−24 dBm		−17		dBm	
−34 dBm		−22		dBm	
−44 dBm		−27		dBm	
−54 dBm		−32		dBm	
−64 dBm		−37		dBm	

EXPANDER

PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
Input Impedance	50			k ohm	
Output Impedance			50	ohm	
Output Signal Level for −10 dBm		0		dBm	
Output Voltage Swing	+8			dB	
Output Noise Input AC Grounded			+5	dBrnc	
Expander Transfer Characteristics** Expander Input Levels Required for Output of:					
+6 dBm		−7		dBm	
+2 dBm		−9		dBm	
0 dBm		−10		dBm	
−4 dBm (reference)		−12		dBm	
−14 dBm		−17		dBm	
−24 dBm		−22		dBm	
−34 dBm		−27		dBm	
−44 dBm		−32		dBm	
−55 dBm		−37		dBm	

Notes: *0 dBm = 0.775 Vrms (1 mW across 600 ohm load) **Recommended transfer characteristics.

EQUIVALENT SCHEMATIC DIAGRAM



CIRCUIT DESCRIPTION

The analog signal compressor/expander or "compandor" circuits are among the most fundamental building blocks in telecommunication systems. These circuits are intended to compress or expand the dynamic range of speech or other analog signals transmitted through telecommunication systems.

Figure 1 shows the simplified block diagram of a typical speech transmission system, using the compression/expansion or "companding" technique. The dynamic range of the input signal is first compressed at the transmitting end; then transmitted through the system, and finally expanded back to the original amplitude at the receiving end. Thus, the "compressor" and the "expander" sections of a compandor system perform reciprocal functions. In a bi-directional transmission system, there is a compandor at each end of the line which compresses the out-going signal, or expands the incoming signal by an equal amount.

Figure 2 shows the typical transfer characteristics of compressor and expander circuits commonly used in telecommunication systems. In the compressor, the output amplitude varies 1 dB for every 2 dB change of input amplitude; the reverse is true for the expander.

The functional block diagram of XR-2216 compandor is shown on Page 1, in terms of the monolithic circuit package. The XR-2216 is designed to be connected as *either* a compressor or an expander, the choice being determined by the external circuitry. The monolithic system is comprised of four basic blocks: (1) an internal voltage reference; (2) an ac/dc converter which converts ac signal input to a dc current level; (3) an impedance converter whose impedance level is a function of a dc control signal; and (4) a high gain operational amplifier.

The XR-2216 is designed to accommodate a wide range of system configurations It can be operated with positive, or negative, single-supply systems, or with balanced power supplies, over a power supply range of 6 volts to 20 volts.

Some of its key features are: low external component count, excellent transfer function, tracking, low power supply drain, controlled attack and release times, low noise and low distortion.

EXPANDER (Figure 3)

Figure 3 shows the external circuit connections and components necessary to operate XR-2216 as an expander. An input signal is applied to Pin 7 which is the

AC/DC converter input. The AC/DC converter converts the AC signal input to a dc current level which in turn controls the transconductance of the impedance converter. Part of the input signal is applied to the impedance converter by connecting Pins 8 and 10. Thus the signal current at Pin 11 is proportional to the product of the input signal and its average value.

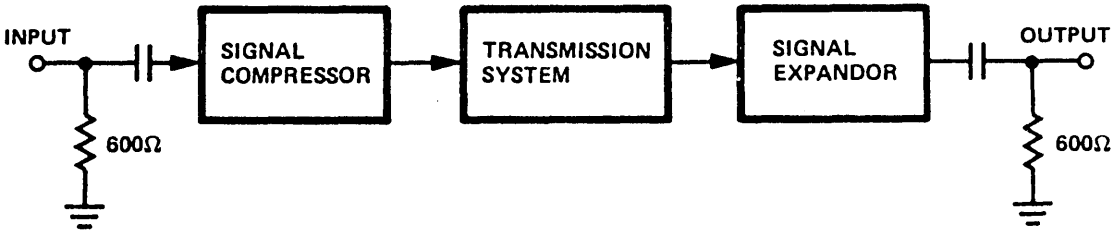


Figure 1. Simplified Block Diagram of a Speech Transmission System Using Companding Technique

The output signal current is then fed to the operational amplifier by connecting Pins 11 and 16, and the output signal voltage is directly proportional to the signal current flowing into Pin 16. The output signal of the expander is available at Pin 2. In this operation, the reference level is set by the trim pot R1, and the trim pot R2 provides a means for trimming low level tracking.

In the connection of Figure 3, the input signals of −37 dBm to −7 dBm are expanded to 60 dB output range with up to 0 dBm power matched output to 600Ω load.

COMPRESSOR (Figure 4)

Figure 4 shows the typical circuit connection for compressor operation. It is just a non-inverting voltage amplifier whose input level is proportional to the product of the incoming signal and the impedance of the impedance converter which is inversely proportional to the amplifier output. Consequently, the output signal at Pin 2 is proportional to square root of the input signal.

In this operation, just like expander operation, the reference level is set by the trim pot R1 and low level tracking is adjusted by the trim pot R2. In the connection of Figure 4, the output change is 1 dB for 2 dB input change. The output range can be adjusted to −37 dBm to −7 dBm for input signals of 60 dB dynamic range.

Note: Attack and Decay Times:

The speed with which gain changes to follow changes in input signal levels is determined by the capacitor C1 and the resistor R1. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the impedance converter. In an expander and compressor application, this would lead to a 3rd harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion.

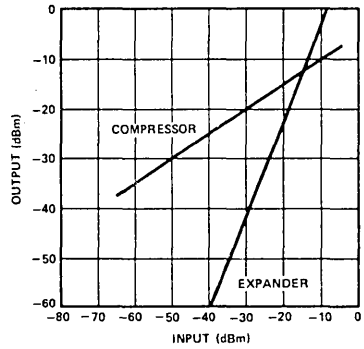


Figure 2. Transfer Characteristics of Compressor a Expander Circuits

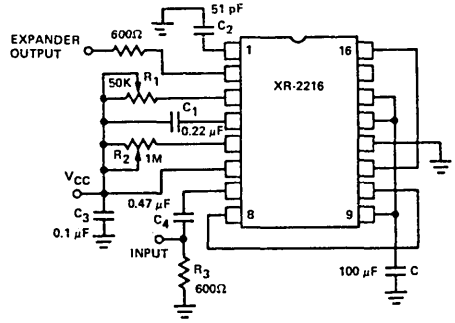


Figure 3. External Connections for Operation Expander

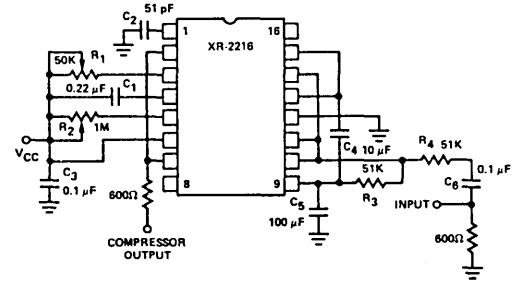


Figure 4. External Connections for Compressor Operation

TYPICAL PERFORMANCE CURVES

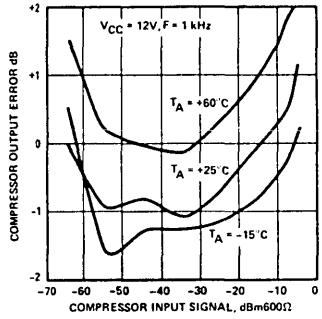


Figure 5. XR-2216 Compressor Output Error vs. Input Signal Amplitude

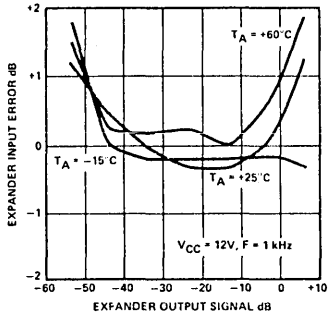


Figure 6. XR-2216 Expander Input Error vs. Output Signal Amplitude

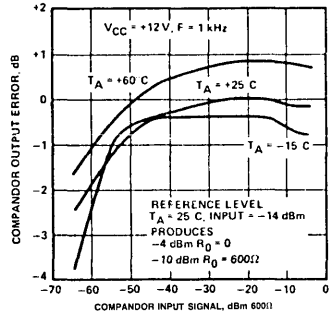


Figure 7. XR-2216 Compandor Tracking Error vs. Input Signal

Pulse-Proportional Servo Circuit

GENERAL DESCRIPTION

The XR-2264 and 2265 are Monolithic circuits designed for use in pulse-proportional servo systems. They have been specifically designed for Radio Control applications. These devices are capable of controlling positions in direct proportion to the width of input pulses. The 2264 can interface directly with servo motors requiring up to 350mA of drive current. The 2265 with open collector outputs can drive relays, optical couplers and triacs, directly. Both the 2264 and 2265 can drive external PNP transistors for applications requiring high current output drive.

The XR-2264 or 2265, combined with a servo motor and a feedback potentiometer form a closed-loop system. These devices have internal one-shot multivibrators. The pulse width of this one-shot is controlled by the servo potentiometer. When an input pulse is applied, the motor is turned "on" in the direction necessary to make the internal one-shot pulse width equal to the incoming pulse width. Because the transfer characteristics of the XR-2264 and 2265 can be controlled by the selection of external components, it can be used in many industrial and radio controlled servo-system applications.

FEATURES

Wide Supply Voltage Range (3.0V to 6.0V)
Bi-directional Operation with Single Supply
Separately-Adjustable Dead Band and Pulse Stretching
2264 - 350mA Source and Sink on chip.
500mA with External PNP
2265 - 500mA Sink Capability on chip.
500mA Sink or Source Capability with external PNP

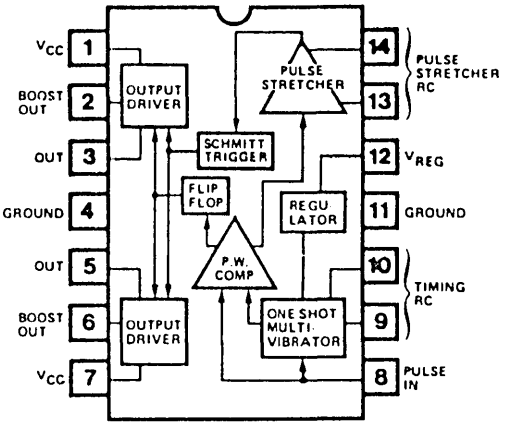
APPLICATIONS

Remote Control Toys
Robotics Applications

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Power Dissipation	550 mW
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2264 CP	Plastic Dual-In-Line	−10°C to +50°C
XR-2265 CP		

SYSTEM DESCRIPTION

Figure 3 shows the circuit connection diagram for the XR-2264. The external component values shown are selected for a pulse width range of 1 to 2 msec, a frame time of 12.5 msec, and a dead band* that is suitable for use with small radio-controlled servos. However, with a proper choice of external components, the characteristics of these devices can be adapted to provide optimum performance for a broad range of hobby and industrial servo control applications.

The shaft of potentiometer R_2 is connected to the servo output shaft; the voltage on the wiper provides positional feedback to the one-shot multivibrator of the XR-2264 or 2265. The one-shot pulse width range is set by the product of R_1 and C_1; R_1 should be kept in the range of 8KΩ to 16KΩ. For operation over a range of pulse widths

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V, T_A = 25°C

PARAMETERS	LIMIT			UNITS	CONDITIONS
	MIN	TYP	MAX		
Supply Voltage	3.2	5.0	6.5	V	
Supply Current		4.5	10.0	mA	Measured into Pins 1 & 7
Regulated Output Voltage	2.0	2.2	2.4	V	Voltage at Pin 12
Input Current		0.1		mA	
Input Voltage Range	2.4		6.0	V	
Pulse Timing Error			±300	μSec	Initial Setting 1.07 sec; Curcuit of Figure 3

OUTPUT CHARACTERISTICS

DEVICE	PARAMETER	LIMIT			UNITS	CONDITIONS
		MIN	TYP	MAX		
2264	Output Current Range	0		500	mA	I sink
	Output Current Range	0		350	mA	I source
	V_{CE}			0.25	V	I sink 500mA
	V_{CE} (V_{CC} − V_{OH})			1	V	I source 350mA
2265	Output Current Range	0		500	mA	I sink
	V_{CE}			0.25	V	I sink 500mA

of less than 2 to 1, the value of potentiometer R_2 may be reduced; the value of the 2.2KΩ resistor to ground should be increased by about the same amount.

The voltage on C_2 provides the input signal for the Schmitt trigger. In order for the motor to be driven, pin 14 must remain low, long enough to pull C_2 down to the lower threshold via R_3. The motor will be turned off only after pin 14 has turned off and C_2 has charged to the upper Schmitt trigger threshold through R_4. Thus, the dead band is controlled by C_2 (R_3 + R_i) where R_i is the "on" resistance at Pin 14. The pulse stretching is controlled by the product of C_2 and R_4. Figure 4 shows the effect of R_3 and R_4 upon the dead band and pulse-stretching performance of the XR-2264 with C_2 = 0.22μF.

**Note: The "Dead band" is the narrow region about a given shaft position which 2264 will not produce a Stretched Pulse large enough to drive the motor. Some dead band width is necessary because the motor shaft has inertia; otherwise, the motor would never stop "hunting" its target position.*

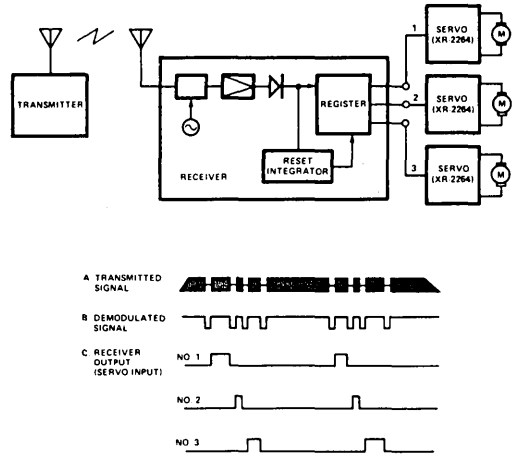
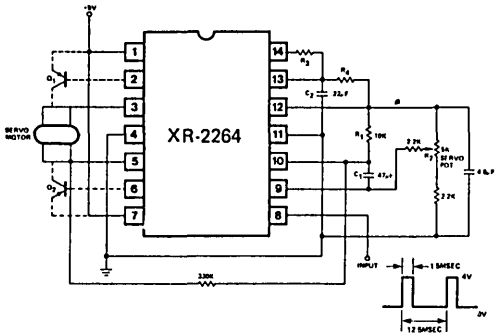


Figure 2. Radio Control System



*NOTE: XR-2264 Q_1 and Q_2 optional; only needed for Servos requiring 500mA drive current.
**NOTE: XR-2265 Q_1 and Q_2 needed if output current source is required.

Figure 3. Connection Diagram of XR-2264 and XR-2265 Servo Control IC

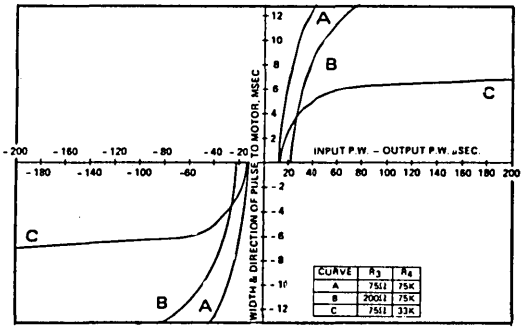


Figure 4. XR-2264 and XR-2265 Output vs. Input Showing Dead Band. Circuit of Figure 3

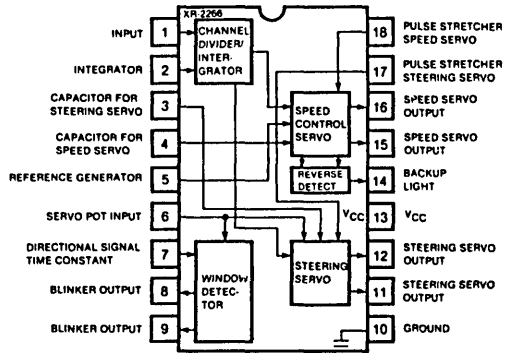
8

Monolithic Servo Controller

GENERAL DESCRIPTION

The XR-2266 is a monolithic servo controller specifically designed for radio controlled model cars. The device is capable of controlling speed in forward or reverse, direction of turn, backup lights, and turn signals with programmable flash rate. Supply voltage may range from 3.5V to 9V.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Internal Channel Divider
Internal Steering Servo with Direct Drive for Servomotor and Turn Signal Indicators
Directional Signal Time Constant Externally Settable
Variable Speed Control with Direct Drive for Backup Lights
Wide Supply Range (3.5 - 8.0 volts)
Steering and Speed Servos Independently Programmed

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2266	Plastic	0°C to +70°C

APPLICATIONS

Radio Controlled Cars

SYSTEM DESCRIPTION

The XR-2266 is a monolithic servo controller system specifically designed for radio-controlled model cars. The integrated circuit is a self-contained system made up of two servo controller channels: one controls the direction and speed of travel, the other provides the steering function. The circuit contains an internal channel separator section which automatically steers the incoming control signal to the appropriate servo controller channel.

The entire servo controller system is available in an 18-Pin dual-in-line package, with terminals provided for accessory controls such as turn indicator signals and backup lights. The entire system is fabricated on a monolithic chip, using low-power integrated injection logic (I^2L) technology along with precision analog circuitry. It operates with supply voltages in the range of 3.5 volts to 8 volts.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	9V
Power Dissipation	1100 mW
Derate above T_A = 25°C	6 mW/°C
Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 6 Volts T_A = 25°C unless otherwise specified

PARAMETERS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
Supply Current		30		mA	
Operating Supply Range	3.5	6.0	8.0	V	
Input Threshold		0.7		V	
Reference Generator Output Current		100		μA	Measured at Pin 6
Directional Detector					
Pin 5 Voltage		55		%	Voltage at Pin 6 (Blinker "off")
Pin 5 Voltage		61		%	Voltage at Pin 6 (Pin 8 Blinker "on")
Pin 5 Voltage		48		%	Voltage at Pin 6 (Pin 9 Blinker "on")
Output Current			100	mA	
Steering SERVO					
Output Soruce Current		350		mA	Pin 11 or 12
Output Sink Current		350		mA	Pin 11 or 12
Reverse Detector					
Output Current			100	mA	Pin 14
Speed Control Servo					
Output HIGH Voltage		V_{CC} – 1V		V	Pin 15 or 16
Output Low Voltage		0.2		V	Pin 15 or 16
Output Impedance		700		Ω	PIn 15 or 16

PRINCIPLES OF OPERATION

The theory of operation can be explained with reference to the block diagram of Figure 2 and the timing diagram of Figure 3. The direction and speed information are encoded onto a carrier by either Amplitude Modulation (illustrated Curve A) or Frequency Modulation (not shown). This signal is received and demodulated into Waveform B. The timing of Waveform B is as follows: T_F is the frame time and determines the frequency with which the servos are controlled. T_S is a space pulse used to separate the channel information of T_1 and T_2. The width of T_1 and T_2 contain the steering and speed information respectively.

Waveform B is applied to the input of the XR-2266. This signal is integrated into Waveform C which is then squared to form D. Waveform D is used as a reset to the channel divider circuit. The channel divider circuit triggers on the leading edge of the input signal and generates two outputs; one for steering and the other for the speed control; Waveforms E and F, respec''vely.

Waveform E is applied to the input of Servo No. 1 which serves as the positional control for the steering wheel. The servo pot on the linkage forms a closed loop system with the servoamplifier to position the front wheels to the required position. The servo pot is also connected to the directional indicator circuit which determines whether the wheels are turned enough to enable the blinker lights.

Waveform F is the input to the variable speed control servo. This servo determines the error between the input signal and the preset nominal value and applies drive to the motor proportional to this difference. A detection circuit has also been built into the IC to detect when the car is going in reverse and turn on the backup lights.

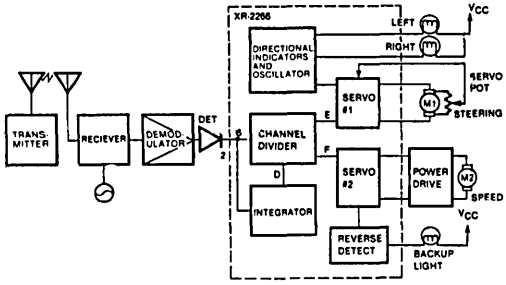


Figure 2. Radio Controlled System Block Diagram

SYSTEM BLOCKS

The XR-2266 is comprised of three independent systems internally connected as in Figure 4 to perform the complete car function. These blocks are the channel divider, steering servo and a speed control circuit. (While a total understanding of these circuits is not necessary a fundamental knowledge of the operation of each block will be an asset to any servo design.)

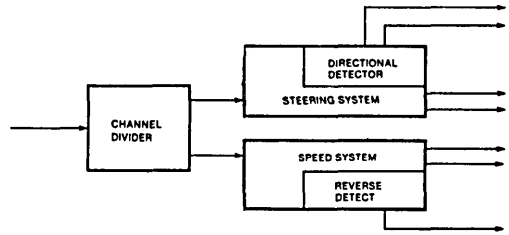


Figure 4. Three Primary Systems of XR-2266

Channel Divider: The function of the channel divider is to decode the channel information from the demodulated input signal and to synchronize the receiver to the transmitter. The synchronization is required to assure that the decoded input is applied to the correct servo. The generation of the synchronization signal is illustrated in Figure 3 and can be explained as follows: The input signal B is integrated by the RC time constant on pin 2 to form waveform C. This integrated signal is then squared to form the synchronization signal D. This signal resets the channel divider when high, guaranteeing that the first input be directed to the channel one servo and the second input be directed to the channel two servo, as illustrated by waveforms E and F, respectively. The width of the input signals is determined by the time interval between two successive positive going edges of waveform B. After the channel two input ends, the integrator charges up to the reset level and enables channel one for the next rising edge of the input signal. The time constant for the integrator is externally set by the RC time constant on pin 2. It is recommended that the time constant be chosen such that the reset occurs midway between the input frame time.

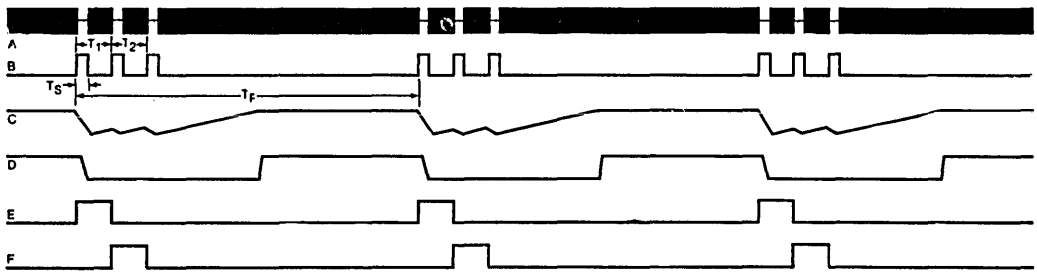


Figure 3. Timing Diagram

Steering Servo: The block diagram of the steering servoamplifier is illustrated in Figure 5. The primary function of this block is to control the position of the front wheels of the car in direct proportion to the input pulse width. The XR-2266 has the additional feature of being able to detect the magnitude and direction of the position of the wheels from their center position and if it is greater than an externally preset amount, to activate a blinker circuit for the appropriate turn-direction. The operation of the steering servoamplifier can be explained with reference to the block diagram of Figure 5 and timing diagram Figure 6. On the leading edge of the input signal an internal one-shot is triggered. The one-shot generates an output pulse whose width is directly proportional to the present position of the shaft of the servomotor. The position information is supplied via the servo pot. The width of these two pulses are then compared and two error signals are generated; one is the directional error which is used to determine the output drive direction and the other is the magnitude error which is applied to the pulse stretcher section which determines whether the error was of sufficient magnitude to enable the output driver stage. If the dead band is exceeded, the error pulse of several microseconds is then stretched to several milliseconds of output drive. The dead band is required to assure that the motor does not oscillate about its center point. The XR-2266 has internal driver transistors that are capable of sinking or sourcing 350 mA. The positional information from the servo pot is also applied to a window comparator and the output of this circuit determines the deviation of the steering wheel from its center position. If this is greater than the preset amount, the blinker signals are activated. The time constant of the blinkers is set by the capacitor on pin 7. The blinker outputs are open collector type capable of sinking 100 mA each.

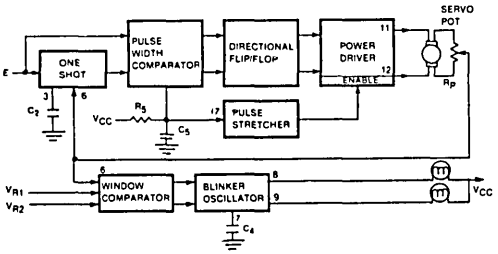


Figure 5. Steering Servo System

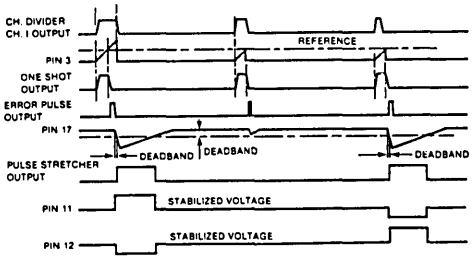


Figure 6. Timing Diagram

Speed Control Circuit: The channel two output Waveform F from the channel divider, as shown in Figure 7, is applied to the input of the speed control servo. This circuit is similar to the steering control servo with the exception that it is operated in an open loop configuration. Thus, the duty cycle of the output drive increases until a maximum drive is reached. The drive characteristics for the speed control are set independently of the steering by an RC time constant on pin 18. Due to the high power motors required for speed control, an external driver transistor must be used. A typical connection for these transistors is illustrated in Figure 7. The speed control amplifier also features an additional output for the backup lights. This output is obtained from the directional logic which determines whether the car is going in the forward or reverse direction. The motor terminals could also be reversed and the output used to drive the front headlights when the car is going forward. The output for the driver lamps is an open collector transistor and is capable of sinking 100 mA. Since this is an open collector output, care should be taken to avoid any possible shorting to the V_{CC} pin, as this will damage the device.

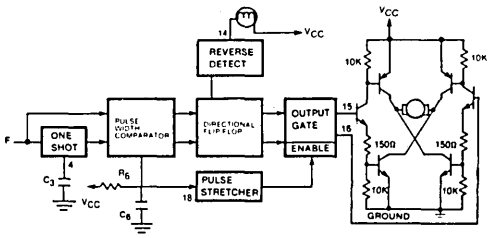


Figure 7. Speed Control Servo System with Connection for External Driver Transistors

DESCRIPTION OF CONTROLS

Input (Pin 1): The demodulated output from the receiver is applied to this pin. The threshold for the input is approximately 0.7V. It is recommended that a 0.0022 μF capacitor be connected from this point to ground to eliminate any RF signal at the input.

Reset Integrator (Pin 2): The function of this pin is to synchronize the servo control to the transmitter. This assures that the steering and speed control signals are not interchanged. The time constant used for this circuit is dependent upon the frame time of the input signal. For a 15 millisecond frame, the value for R_1 is 510K and for C_1, 0.1 μF. Other frame rates may be used, in which case the RC time constant may be determined by the following equation:

$$R_1C_1 = [T_F - X(T_N)]/2 \ln [V_{CC}/(V_{CC} - .66)]$$

where

T_F = Frame Time
X = Number of Servos
T_N = Nominal Pulse Width for Servos
V_{CC} = Nominal Supply Voltage

Timing Cap for Steering Servo (Pin 3): The capacitor on this pin is used to determine the nominal one-shot time constant for the steering control. The capacitor value is chosen by the following equation:

$$C_2 = T_N/(R_2 + R_P/2)$$

where R_2 is a 1K potentiometer and R_p is the servo pot, nominally 5K. This yields 0.47 μF for C_2. R_F is a damping resistor that provides a momentum feedback to prevent the servo from overshooting. The recommended values for R_F are 100K to 700K, depending on the required loop damping.

Timing Cap for Speed Control (Pin 4): This capacitor determines the nominal one-shot time constant for the speed control servo. The capacitor value is determined by:

$$C_3 = 1.3\ T_N/(R_P + R_2)$$

Reference Generator (Pin 5): Pin 5 is used to generate the reference level for the speed and steering servos and also control the degree of turning before the directional indicators are activated. This pin is directly connected to one end of the servo pot with the other connected to a 1K pot or fixed resistor to ground. This 1K pot is used to adjust the dead time for the directional indicators. In noisy environments, pin 5 should be bypassed to ground via a 0.001 μF capacitor.

Steering Positional Input (Pin 6): The wiper of the servo pot is connected to this pin to supply the positional information to the one-shot of the steering servo. In noisy environments this pin should be bypassed to ground via a 0.002 μF capacitor.

Directional Signal Time Constant (Pin 7): The capacitor connected to this pin determines the time constant for the directional indicators. The ratio of 'ON' to 'OFF' is approximately 2:1 and the frequency is determined by:

$$F(Hz) = 81/C_4\ (\mu F)$$

Outputs for Directional Indicators (Pin 8 & 9): These pins are used to drive the directional signal indicators. These are open collector outputs that can sink a maximum current of 100 mA.

Steering Motor Drive (Pin 11 & 12): These outputs connect directly to the steering servomotor and are capable of sinking or sourcing 350 mA.

Output for Backup Lights (Pin 14): This terminal is activated when the car is driving in the *reverse* direction. This is an open collector output with a maximum current of 100 mA.

Note: by reversing the motor leads, this terminal could be used to control front headlights when the car is moving forward.

Output for Speed Control (Pin 15 & 16): These pins are used to drive an external power bridge to control the speed of the car. A typical connection is illustrated in Figure 7.

Pulse Stretcher (Pin 17 & 18): The RC time constant on pin 17 and pin 18 is used to set the dead band and the maximum drive pulse to the steering servo and speed control servo, respectively. The dead band time is determined by:

$$T_{dB} = (51.4)(C)$$

The maximum drive time is determined by:

$$T_{MD} = RC1n\ [(V_{CC} - .73e^{-(1x10^{-6}/C)})/(V_{CC} - .66)]$$

Power Supply (Pin 13 & 10): The battery should be connected from pin 13 (V_{CC}) to pin 10 (ground). The operating power supply range is 3.5 to 9 volts. A 100 μF capacitor is recommended across the power supply terminals.

APPLICATION EXAMPLE

The method for determining the component values for any servo application can be obtained by the following design rules. These equations will yield values suitable for proper operation and can later be adjusted to suit particular applications. For the example chosen, the frame time is 15 ms and the pulse width is nominally 1.4 ms with a deviation of 500 μs. Dead band is chosen to be 30 μs and 80 μs for the steering and speed control sections, respectively. The servo pot is a 5K pot and the operating supply voltage is 6 volts.

Procedure:

1. To determine the time constant of the integrator on pin 2, use the following formula with R_1 assumed to be between 100K and 1M. In this example we set C_1 = 0.1 μF and calculate R_1.

   $$R_1 = [T_F - X(T_N)]/2C_1 1n[V_{CC}/(V_{CC} - .66)]$$

   This yields $R_1 \approx 510K$

2. C_3 and R_2 setting (using a 1K pot) is determined by the following: First approximate R_2 to be one half of its value and solve for C_3.

   $$C_3 = 1.3T_N/(R_p + R_2/2)$$

   $$C_3 \approx .33\ \mu F$$

   $$C_3 = 0.25\ \mu F$$

   Select nearest standard value for C_3 and calculate R_2 value

   $$R_2 = (1.3T_N/C_3) - R_p$$

   $$R_2 \approx 515\Omega$$

3. C_2 is determined by the following: Use value for R_2 as calculated above.

   $$C_2 = T_N/(R_2 + R_p/2)$$

   $$C_2 \approx .47\ \mu F$$

4. C_4 determines the blinker frequency, for a frequency of 2 times per second.

$$C_4(Hz) = 81/F(Hz)$$

$$C_4 \approx 47.0\ \mu F$$

5. C_5 determines the dead band time for the steering servo for most car applications. This is chosen to be approximately 30 μs. Solving for C_5 yields:

$$C_5 = T_{dB}/51.4$$

$$C_5 \approx .47\ \mu F$$

6. R_5 is selected via the formula

$$R_5 = T_{MD}/[C1n(V_{CC} - .73e^{-(1x10^{-6}/4C)})/V_{CC} - .66)]$$

$$R_5 = 910K$$

7. C_6 is chosen with the same formula as C_5 except dead band is set to approximately 80 μs. This gives the system better speed control.

$$C_6 = T_{dB}/51.4 = 1\mu F$$

8. R_6 is chosen via the same equation as R_5.

$$R_6 = T_{MD}/[C1n(V_{CC} - .73e^{-(1x10^{-6}/C)})/V_{CC} - .66)]$$

$$R_6 = 430K$$

9. Set R_F = 510K. To adjust value see Table I.

The complete circuit with the calculated values is illustrated in Figure 8. The circuit layout is illustrated in Figure 9.

Table I lists the recommended values for the servo application outlined above and describes the result if improper values are used.

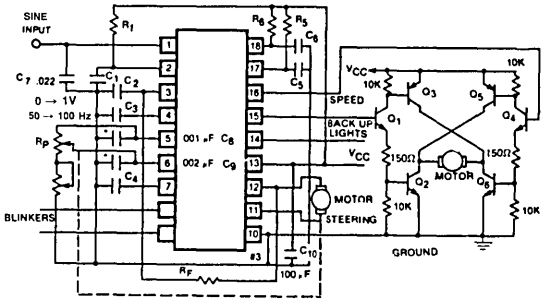


Figure 8. Typical Application Schematic

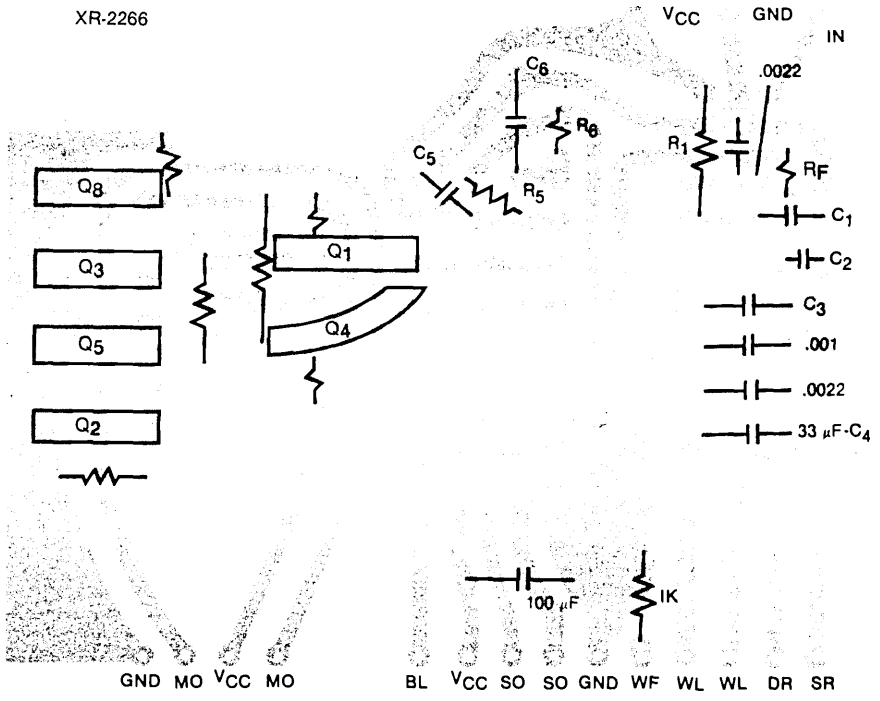


Figure 9. Printed Circuit Board Layout (4x)

8

TABLE I

COMPONENT NUMBER	VALUES	EFFECTS
R_1 510K	Small	The integrator rise time becomes too fast and the fall time becomes too slow. Therefore, the integrator may reset too soon.
	Large	The integrator rise time becomes too slow and the integrator may not reset before the next input.
	Recommended	200K — 700 K carbon film R25 series.
R_F 510K	Small	Too much negative feedback occurs, causing the response of the servo to be too slow.
	Large	Almost no negative feedback occurs and a large positional overshoot results.
	Recommended	100K — 800K should be selected by the actual test results (dependent upon motor gears and linkage used). Carbon film R25 series.
R_5 910K	Small	The pulse stretcher gain becomes too small and this reduces output drive time causing wheels to turn slowly.
	Large	The pulse stretcher gain becomes too large and the motor tends to oscillate (hunt) about its position.
	Recommended	500K — 1M, largely dependant upon the value of C_5, frame time and maximum deviation of the input pulse width. The equation for determining the nominal value is given in the "Description of Controls" section for pins 17 and 18.
R_6 430K	Small	The pulse stretcher gain becomes too small and the maximum speed of the car is reduced.
	Large	The pulse stretcher gain becomes too large and the car speed becomes hard to control. It is either 'ON' full, or 'OFF'.
	Recommended	400K — 700K, depending on the value of the capacitor; since this is for the speed, the dead band width is set larger and pulse stretcher gain is set high. Carbon film R25 series.
R_p 5K	Recommended	This is the servo pot connected to the steering linkage, a B type volume potentiometer is recommended.
R_2 1K	Recommended	This potentiometer is used to set both the neutral position for the speed control and the range of operation for the directional indicators. A temperature stable carbon type is recommended.
C_1 0.1 μF	Small	The charging time tends to be short and the discharging time constant tends to be long, therefore, the integrator may reset too soon.
	Large	The charging time tends to become long and the integrator may not reset before the next input.
	Recommended	If R_1 = 510K, C_1 should be between 0.047 μF to 0.22 μF. Mylar recommended.

COMPONENT NUMBER	VALUES	EFFECTS
C_2 0.47 μF	Small	The width of the one-shot for the steering servo becomes too small and the front wheels may turn fully in one direction.
	Large	The width of the one-shot for the steering servo becomes too large and the front wheels may turn fully in one direction.
	Recommended	If the nominal input width is 1.4 ms, 0.47 μF is recommended. For operation with other conditions, see "Description of Controls" section for pin 3. Tantalum type is recommended.
C_3 0.33 μF	Small	The width of the one-shot for the speed control servo becomes too small and drive occurs in only one direction.
	Large	The width of the one-shot for the speed control servo becomes too large and drive occurs only in one direction.
	Recommended	If the nominal input width is 1.4 ms, 0.33 μF is recommended. For operation with other conditions, see "Description of Controls" section for pin 4. Tantalum type is recommended.
C_4 33 μF	Recommended	This capacitor determines the direction signal time constant. The capacitor value is determined by the equation in the "Description of Controls" section for pin 7.
C_5 0.47 μF	Small	Dependent upon the value of R_5. Generally the pulse stretcher gain becomes smaller, thus, slowing down the general speed and making acute turns slower. This also decreases dead band causing hunting about its position.
	Large	Depending on the value of R_5, the pulse stretcher gain becomes extremely large and although turning speed improves, the hunting condition becomes worse. This also increased dead band causing the motor to jump position.
	Recommended	In case of R_5 = 910K, 0.1 μF to 0.68 μF is suitable. Tantalum type is recommended.
C_6 1 μF	Small	Depending on the value of R_6, the pulse stretcher gain becomes smaller and you cannot achieve 100% drive; also, the dead band is reduced and the neutral position on the stick may be eliminated.
	Large	The pulse stretch gain increases causing rapid increase in speed, once the dead band is exceeded; also, the dead band increases causing a long amount of neutral position in the control stick.
	Recommended	In case of R_2 = 430K, 0.68 to 2.2 μF is suitable. Tantalum type is recommended.
C_7 2200 pF	Recommended	As mentioned in the "Description of Controls" section for pin 2, this value should be between 0.001 and 0.01 μF. Ceramic or mylar is the best choice.
C_8 1000 pF	Recommended	As mentioned in the "Description of Controls" section for pin 5, this value should be between 0.01 and 0.001 μF. Ceramic or mylar are recommended.
C_9	Recommended	Same as above.
C_{10} 100 μF	Recommended	As mentioned in the "Description of Controls" section for pin 10 and 13, this capacitor helps to stabilize the power supply when the car is running. If operation becomes intermittent, this value should be increased. Recommended 10 to 470 μF tantalum.

Frequency-to-Voltage Converter

GENERAL DESCRIPTION

The XR-2917 Frequency-to-Voltage Converter is a high accuracy converter consisting of input comparator with 40 mV hysteresis, charge pump, Zener regulator, and output op amp and transistor. Designed for tachometer and motor control applications, it features excellent linearity and high current output.

Output voltage is a simple function of the Zener regulator voltage (V_Z), a resistor (R_1) and capacitor (C_1) which are connected to the charge pump, and the input frequency (f_{in}). Ripple reduction is implemented by addition of one capacitor (C_2) which is used to achieve frequency doubling. The output transistor can swing to ground, sink a load current of 40 mA, and offers a maximum V_{CE} of 28 V. Stable and accurate frequency to voltage or current conversion is ensured by the on-chip Zener regulator which is connected across the power leads. The Zener may be used with any supply voltage (up to 28 V) when a suitable resistor is connected between the Zener and the supply.

The XR-2917 may be operated with a ground referenced input or differential tachometer input with uncommitted op amp inputs. The ground referenced configuration is most basic, allowing the realization of single speed, frequency switching, and buffered frequency-to-voltage or current conversion applications. Differential input configurations allow the tachometer to be floated, while uncommitted op amp inputs free the op amp for implementation of active filter conditioning of the tachometer output.

The XR-2917, available in a 14 Pin DIP, operates from a single power supply of up to 28 V.

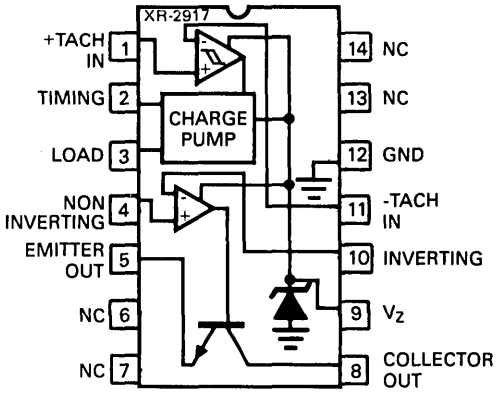
FEATURES

Design Simplicity: $V_{OUT} = f_{in} \times V_Z \times R_1 \times C_1$
Frequency Doubling to Decrease Output Ripple
On-Chip Zener for Functional Stability
Excellent Linearity
Floating Output Drive Transistor Provides 40 mA Source or Sink
Ground Referenced Tachometer Input Which Interfaces Directly with Variable Reluctance Magnetic Pickups.

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2917CN	Ceramic	0°C to +70°C
XR-2917CP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAM



SYSTEM DESCRIPTION

The XR-2917 converts an input frequency to a proportional output voltage. Differential inputs provide hysteresis for excellent noise rejection and the capability of setting the comparator's input switching level. Inputs should not be taken below ground without some lead resistance.

The output of the comparator is fed into a charge pump where current is pumped through a timing capacitor (C_1). This same current is mirrored in the load resistor (R_1) where a filter capacitor (C_2) may be used to integrate current pulses and provide a proportional voltage across the load resistor. The result is a voltage across the load resistor which is a function of the supply voltage, input frequency, timing capacitor, and load resistor:

$$V_{R_1} = V_Z \times f_{in} \times C_1 \times R_1$$

The size of the integrating capacitor (C_2) is dependent only on the requirements of response time and output ripple.

The output op amp and transistor are then used to buffer the output drive capability of the part. Thus, the final conversion equation is:

$$V_O = V_Z \times f_{in} \times C_1 \times R_1 \times K$$

where K is the gain provided by the tachometer section, and is typically unity.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +12 V, T_A = 25°C, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
TACHOMETER						
V_T	Threshold Voltage	±10	±15	±40	mV	V_{IN} = 250 mV @ 1 KHz
V_H	Hysteresis Voltage		30		mV	
V_{OS}	Input Offset Voltage		3.5	10	mV	
I_B	Input Bias Current		0.1	1	μA	V_{IN} = ±50 mV_{DC}
V_{OH}	Minimum High Level Output Voltage		5.1		V	V_{IN} = +125 mV_{DC}
V_{OL}	Maximum Low Level Output Voltage		1.2		V	V_{IN} = -125 mV_{DC}
I_T, I_L	Charge Pump Currents (Timing, Load Pins)	140	180	240	μA	V_T = V_L = 6.0 V
I_{OL3}	Output Leakage Current (Pin 3)			0.1	μA	I_T = 0 V, V_T = 0 V
	Linearity		0.3	1.0	%	Note 1
K	Gain Constant	0.9	1.0	1.1		
OP AMP COMPARATOR						
V_{OS}	Input Offset Voltage		3	10	mV	V_{IN} = 6.0 V
I_B	Input Bias Current		50	500	nA	V_{IN} = 6.0 V
V_{CM}	Input Common Mode Voltage	0		V_{CC}-1.5V	V	
A_O	Open Loop Voltage Gain		200		V/mV	
I_{SI}	Output Transistor Sink Current	40	50		mA	V_C = 1.0 V
I_{SO}	Output Transistor Source Current		10		mA	V_E = V_{CC} -2.0 V
V_{SAT}	Transistor Saturation Voltage		0.1	0.5	V	I_{SI} = 5 mA
				1.0	V	I_{SI} = 20 mA
			1.0	1.5	V	I_{SI} = 50 mA
ZENER REGULATOR						
V_Z	Zener Voltage		7.56		V	R_{DROP} = 470Ω
r_Z	Equivalent Zener Reistance		10.5	15	Ω	
	Temperature Stability		+1		mV/°C	
DEVICE CHARACTERISTICS						
I_S	Supply Current		3.8	6	mA	

Note 1: Non-linearity is the deviation of V_{OUT} @ f_{in} = 5 KHz from the line defined by V_{OUT} @ f_{in} = 1 KHz and V_{OUT} @ f_{in} = 10 KHz with C_1 = 0.001 μF, R_1 = 68 kΩ, and C_2 = 0.22 μF.

APPLICATIONS

Frequency-to-Voltage Conversion
Speedometers
Breaker Point Dwell Meters
Tachometers
Speed Sensing and Control
Governors
Touch, Contact, or Delay Switching

ABSOLUTE MAXIMUM RATINGS (R_{DROP} = 470 Ω)

Power Supply Voltage (Pin 9)	28 V dc
Input Voltage Range	
Tachometer	0.0 V to +28 V dc
Op Amp and Output Transistor	0.0 V to +28 V dc
Supply Current	25 mA
Storage Temperature Range	-55°C to 150°C
Operating Junction Temperature	150°C
Power Dissipation	500 mW
Derate Above 25°C	5.3 mW/°C

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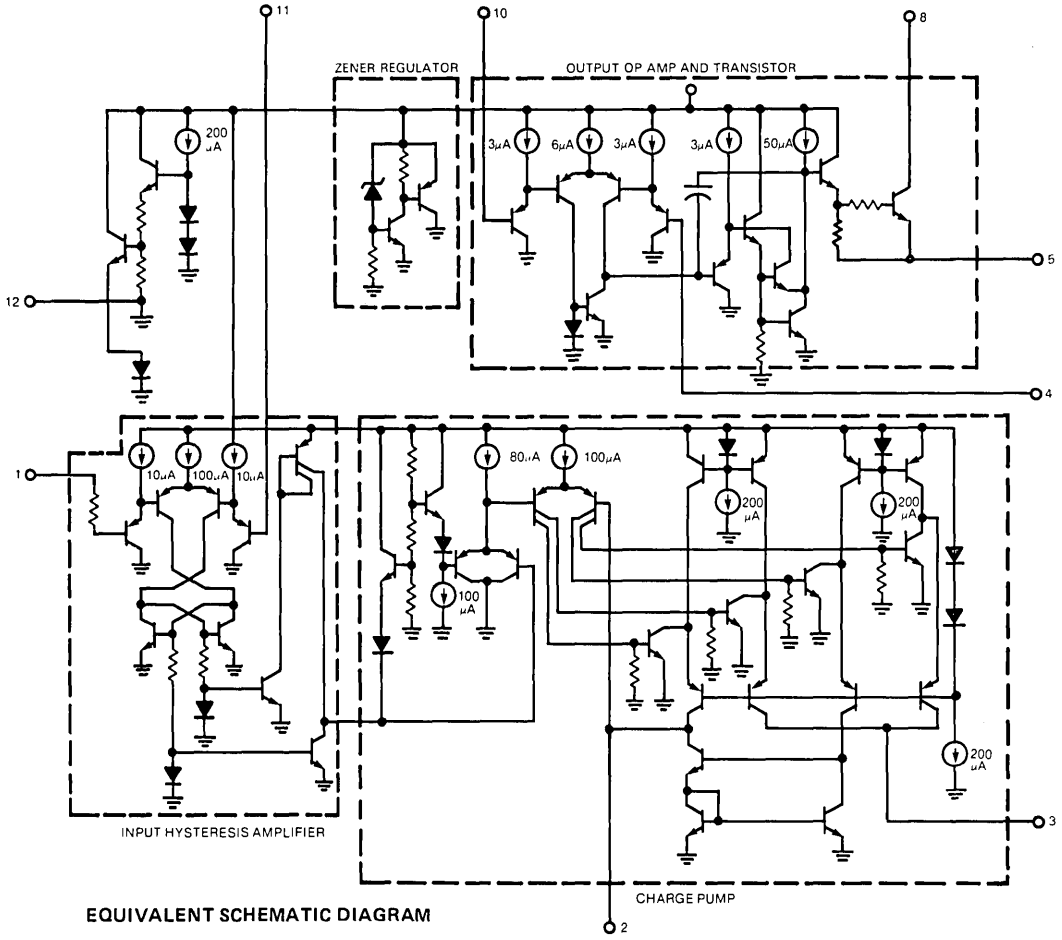


EQUIVALENT SCHEMATIC DIAGRAM

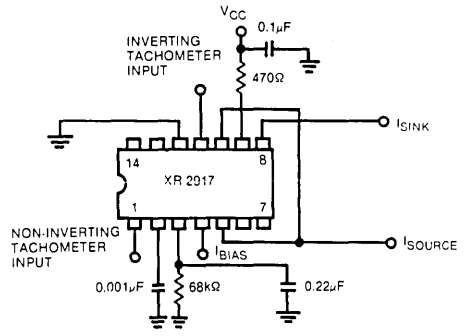
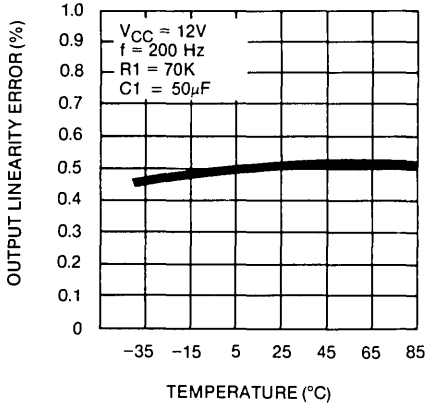


Figure 1. Test Circuit

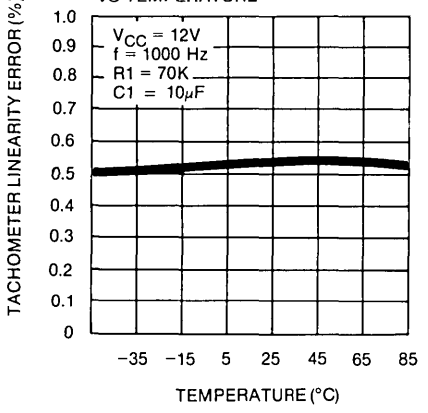
TYPICAL CHARACTERISTICS

R_{DROP} = 470 Ω, V_{CC} = 12 V, unless noted.

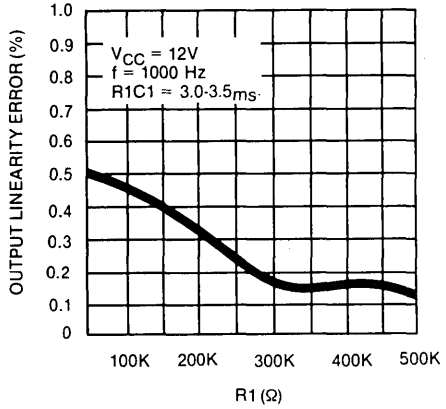
TACHOMETER LINEARITY VS TEMPERATURE



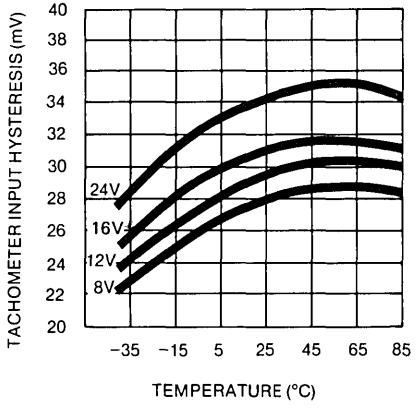
TACHOMETER LINEARITY VS TEMPERATURE



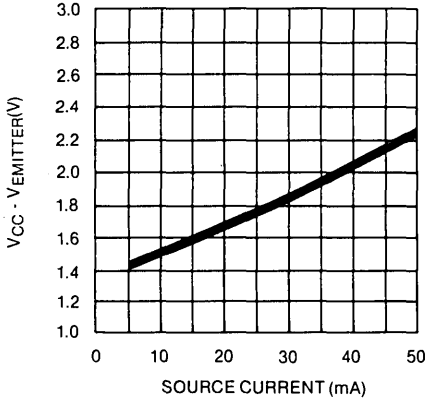
TACHOMETER LINEARITY VS R1



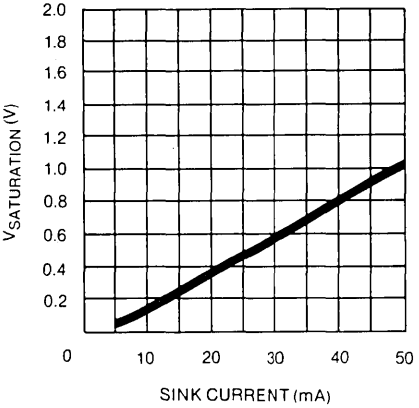
TACHOMETER INPUT HYSTERESIS VS TEMPERATURE



OP AMP OUTPUT TRANSISTOR CHARACTERISTICS (25°C)



OP AMP OUTPUT TRANSISTOR CHARACTERISTICS



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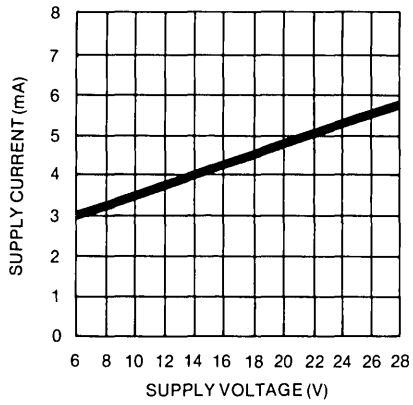
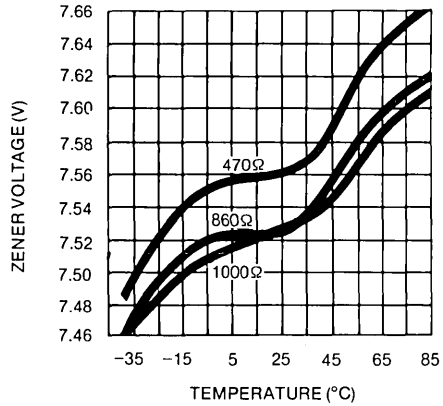
TYPICAL CHARACTERISTICS

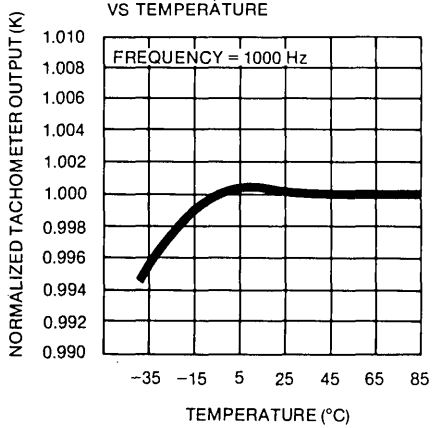
TOTAL SUPPLY CURRENT



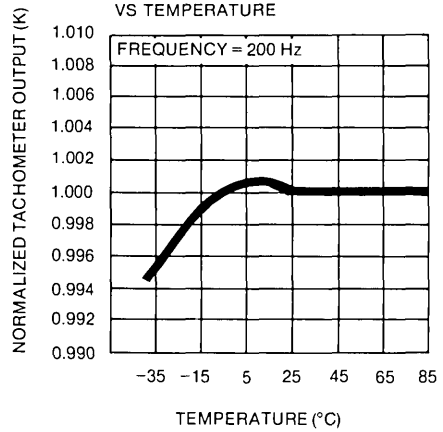
ZENER VOLTAGE VS TEMPERATURE



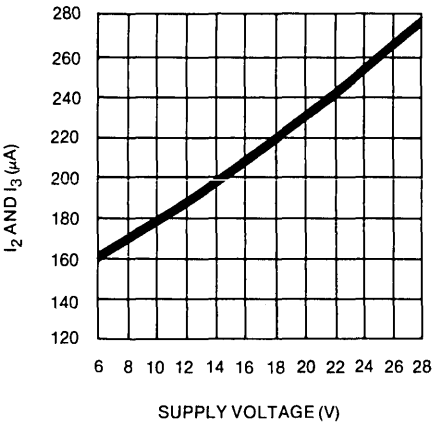
NORMALIZED TACHOMETER OUTPUT VS TEMPERATURE



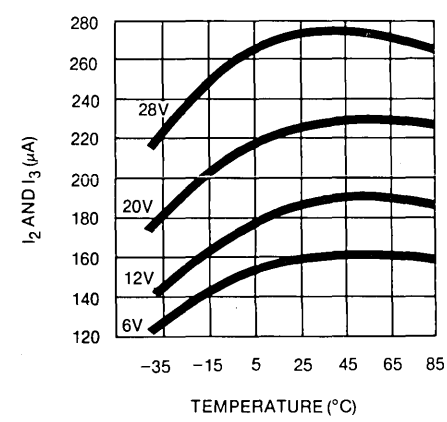
NORMALIZED TACHOMETER OUTPUT VS TEMPERATURE



TACHOMETER CURRENTS I_2 AND I_3 VS SUPPLY VOLTAGE



TACHOMETER CURRENTS I_2 AND I_3 VS TEMPERATURE



PRINCIPLES OF OPERATION

Figure 1 shows the typical connection for the XR-2917 as a frequency-to-voltage/current converter. The system consists of a tachometer section, Zener regulator, charge pump, and output op amp and transistor. Input may be differential or ground referenced single-ended, and output current may be sourced or sunk through the output transistor.

When using the XR-2917 in the differential mode, inputs to the tachometer front-end should be protected by introducing some current limiting resistance in the input lead.

Timing Capacitor

The timing capacitor, C_1, also provides compensation for the charge pump. As such, it must be larger than 100 pF to ensure accurate operation. Values of C_1 smaller than this can cause an error current through the current mirror of the charge pump and thus through R_1.

Load Resistor

There is an additional constraint placed on the load resistor, R_1. Since the output voltage is determined at Pin 3, then

$$V_{OUT} = R_1 I_3 \qquad (1)$$

I_3 is easily determined from the relationship

$$I_3 = I_2 = VZ \times f_{in} \times C_1$$

Combining these two results gives the simplified design equation

$$V_{OUT} = V_Z \times f_{in} \times R_1 \times C_1 \qquad (2)$$

Thus, R_1 must be chosen to achieve maximum V_{OUT} for f_{in}.

Filter Capacitor

The choice of C_2 is dependent upon the ripple voltage allowable at the output of the transistor emitter, Pin 4. Since C_1 is used to set the current through R_1, and R_1 is chosen to satisfy the equation

$$V_{OUT}_{MAX} = R_1 I_3 \qquad (3)$$

and

$$V_{ripple} = \frac{V_Z}{2} \times \frac{C_1}{C_2} \times \left(1 - \frac{V_Z f_{in} C_1}{I_3} \right)_{pp} \qquad (4)$$

Maximum Input Frequency

The maximum input frequency is determined once C_1 has been chosen. It is determined by the relation

$$f_{in}_{max} = \frac{I_2}{C_1 \times V_Z} \qquad (5)$$

Response Time

It should be noted that the time necessary for V_{OUT} to stabilize to a new voltage is a function of C_2, thus as C_2 increases, so does the response time of V_{OUT}.

Zener Regulator

The on-board Zener provides a stable source voltage to the XR-2917's internal systems, so that accurate conversion is possible independent of substantial supply voltage variations. A drop resistor should be placed between the raw supply and the Zener such that the current supplied to the part is equal to the current required at the average supply voltage. As an example, with a raw supply which varies from 9 V to 15 V (an average V_{SUPPLY} of 12 V), a current of approximately 3.8 mA is required. This can be accomplished using a drop resistor, R_{DROP} of 470 Ω. Following this procedure will minimize the Zener's voltage variation.

DESCRIPTION OF INPUTS AND OUTPUTS

Pin	Name	Description
1	+ TACH IN	The non-inverting input to the tachometer input comparator.
2	TIMING	The timing pin for the charge pump. A timing capacitor is required.
3	LOAD	The load pin where the output voltage is generated. An RC combination is typically required here.
4	NON-INVERTING	The non-inverting input pin of the output op amp.
5	EMITTER OUT	The emitter of the output drive transistor.
6	NC	No connection.
7	NC	No connection.
8	COLLECTOR OUT	The collector of the output drive transistor.
9	V_Z	The Zener regulator voltage, and the pin through which the part is connected to the supply voltage.
10	INVERTING	The inverting input pin of the output op amp.

8

11	- TACH IN	The inverting input to the tachometer input comparator.
12	GND	Ground
13	NC	No connection.
14	NC	No connection.

APPLICATIONS

Frequency-to-Voltage Convertor

The basic frequency-to-voltage function of the XR-2917 is illustrated in Figure 2. An input frequency is applied to Pin 1.

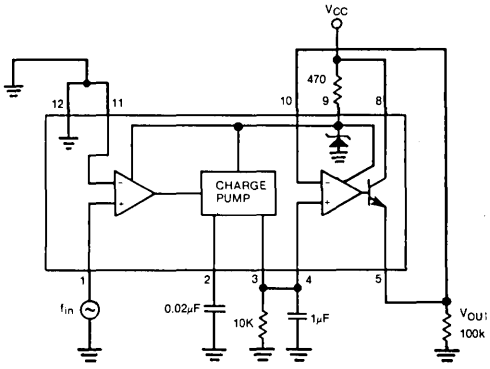


Figure 2. Frequency-to-Voltage Converter

The maximum output voltage is

$$V_{OUT\ MAX} = R_1 I_3 = (10K)(170\mu A) = 1.7V$$

where $I_3 = 170\ \mu A$ if $V_{CC} = 12$ V, and

$$f_{in\ max} = \frac{I_2}{C_1 \times V_Z} = \frac{170\mu A}{(0.02\mu F) \times (7.6\ V)} = 1.12\ KHz$$

The ripple voltage is given by

$$V_r = \frac{V_Z}{Z} \times \frac{C_1}{C_2} \times \left(1 - \frac{V_Z f_{in} C_1}{I_3}\right)_{pp}$$

or

$$V_r = [0.076 \times (1 - f_{in} \times 0.0009)]_{pp}$$

Figure 3 shows the relationship of both V_{OUT} and V_r to f_{in}. V_{OUT} and V_r are not of the same scale.

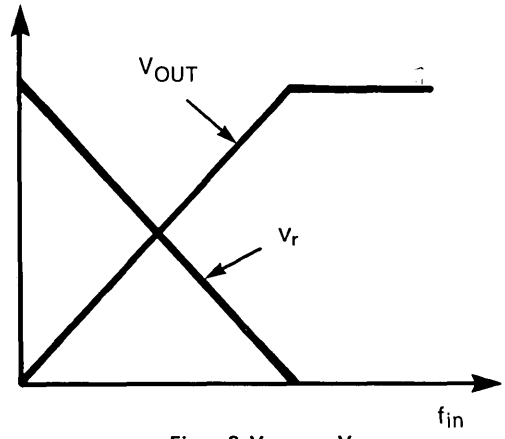


Figure 3. V_{OUT} vs. V_r

A tachometer can be realized by providing the input frequency via a variable reluctance magnetic pick-up. The maximum output voltage and input frequency, and the output ripple voltage may be determined from equations 3 and 5, and equation 4 respectively.

Metering of the output can be performed by sensing current through a current meter in series with the output transistor collector or by taking the voltage off of the emitter.

Separation of the input comparator's inverting input from ground allows the designer to connect a diode to ground to protect the input from transients.

The availability of the output op amp input pins further provides the designer with the opportunity to filter the signal and reduce output ripple.

Speed Switch

Some applications may require a method of determing an overspeed condition for switching purposes. Figure 4 illustrates the basic speed switch configuration. The two 5K ohm resistors from pin 9 to 10 and pin 10 to 11/12 bias the output amplifier a ½ V_Z. When the voltage at pin 4 is greater than ½ V_Z, the output of the amplifier will go high and switch the output transistor into saturation. Once in saturation, current will flow through the load. The output transistor is the "switch."

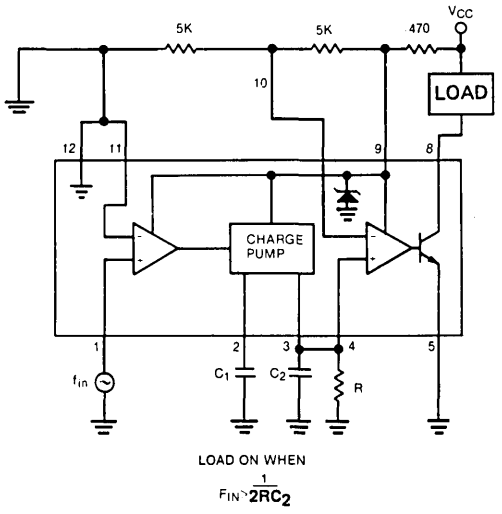


Figure 4. Basic Speed Switch Configuration

From equation 2, it can be shown that the output transistor will switch off when the input frequency (f_{in}) goes below $(2\ RC_2)^{-1}$. This configuration can be adjusted to trip the switch at any fractional frequency of $(RC_2)^{-1}$ by adjusting the voltage divider which is between pins 9 and 10, and pins 10 and 11/12. As an example, to trigger at $(3\ RC_2)^{-1}$, place at 5K ohm resistor between pins 10 and 11/12, and a 10K ohm resistor between pins 9 and 10.

A remote speed switch can be implemented by placing a current sensing resistor between the base and emitter of a transistor. The resistor will be in series with the supply line to the XR-2917; and the load to be switched will be in series with this switch transistor's collector and the supply voltage. When the voltage drop across the resistor equals 700 mV, the transistor will turn on and pull current through the load (see Figure 5).

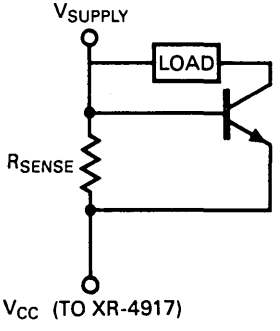


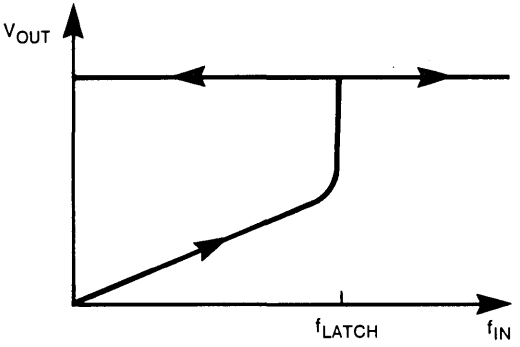
Figure 5. Remote Speed Switch

Since the XR-2917 draws approximately 5 mA as biased with the 470 ohm resistor, and the output transistor can sink about 40 mA, then

$$R_{sense} = \frac{0.7V}{(40+5)mA} = 16\Omega$$

A ¼ watt resistor will suffice, while the transistor should be chosen to pass the required load current. The collector of the output transistor should be connected between the 470 ohm resistor and R_{sense}. The trip voltage is a function of V_Z and is set as before.

An overspeed latch can be realized using a configuration similar to that of Figure 4. The latch requires that the load be voltage controlled, thus be connected between the emitter of the output transistor and ground. Pins 3, 4, and 5 should be tied together thus creating a positive feedback situation which pulls the output, non-inverting input, and load voltages up to the maximum output voltage of the part: this voltage is a function of output transistor current (see Typical Performance Characteristics). The output of the overspeed latch appears in Figure 6.



RESET IS PERFORMED BY REMOVING V_{CC}

Figure 6. V_{OUT} vs. f_{IN}

The trip frequency is set as before, If R_1 is the resistor between pins 9 and 10, and R_2 is the resistor between pins 10 and 11/12, then

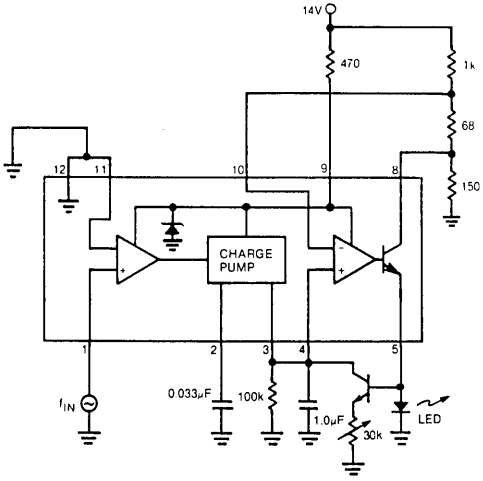
$$f_{latch} = \left(\frac{R_2}{R_1+R_2}\right)(RC)^{-1}$$

A variation of the overspeed latch is the overspeed indicator of Figure 7. In this case

$$f_{trigger} = \left[\left(\frac{68+150}{68+150+1K}\right)(14/7.56)\right]\left[(100K)(.033\mu)\right]^{-1}$$

and the trigger frequency can be adjusted at R and C_2 or by using the voltage divider.

8



FLASHING BEGINS AT $f_{IN} \geq 100$ Hz AND INCREASES WITH FREQUENCY INCREASES.

Figure 7. Overspeed Indicator

When the voltage at pin 4 exceeds that set by the divider off pin 10, the LED turns on. The transistor whose base is connected to the anode of the LED will turn on and discharge the capacitor at pin 4 and turn off the LED.

A delay switch can be implemented by removing resistor R from pins 3/4 inFigure 4. Choosing C_2 such that

$$C_2 = 2\ n\ C_1$$

Current will not flow through the load until n consecutive input cycles have occured.

Capacitance Meter

Figure 8 is a capacitance meter. The range of the meter can be adjusted by adjusting R_1 in the equation

$$C_X = (2.2 \times 10^{-3})\ (V_{OUT}/R_1)$$

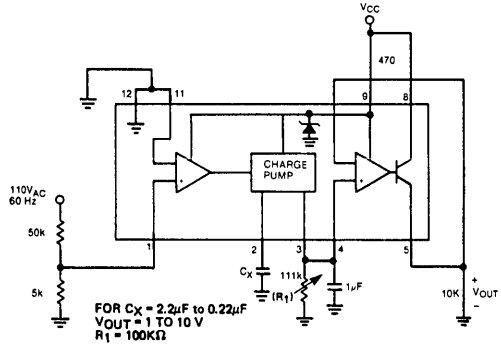


Figure 8. Capacitance Meter

Hysteresis

Figure 9 illustrates one method of providing hysteresis. The magnitude of hysteresis is given by

$$\left(\frac{2K}{2K + 195K}\right) V_{REF}$$

or

$$V_{HYSTERESIS} = 0.01\ V_{REF}$$

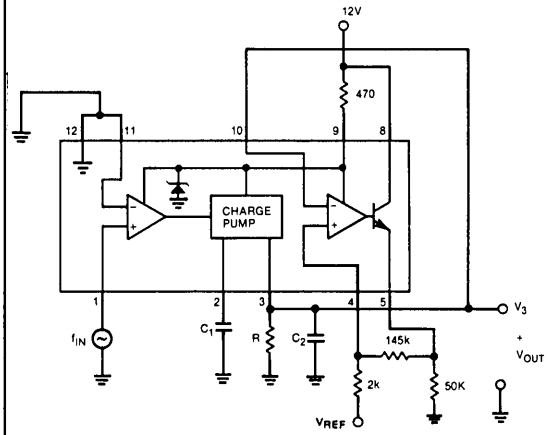


Figure 9. Hysteresis

Shifting Response of Output Voltage

Figure 10 illustrates a simple method of shifting the output voltage up by a constant value, V_{SHIFT}. The output voltage for this circuit is given by

$$V_{OUT} = (V_Z \times f_{in} \times R_1 \times C_1) + V_{SHIFT}$$

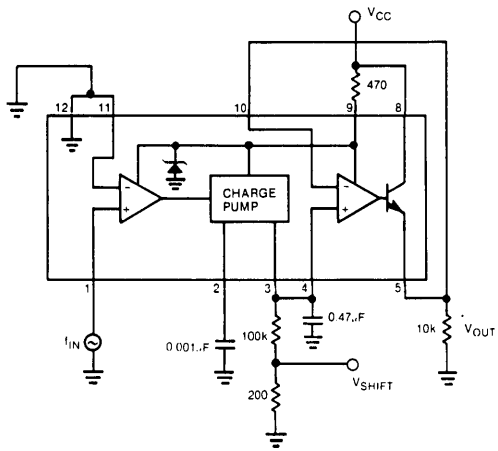


Figure 10. Shifting Output Voltage

A method of delaying the output response to the input frequency is shown in Figure 11. There will be no change in the output voltage until

$$f_{in} = (V_Z \times R_1 \times C_1)\text{-}1$$

At this point, equation 2 is valid.. Using the voltage divider between pins 8 and 5, and 5 and ground, one may change the level at which the output voltage will begin to react.

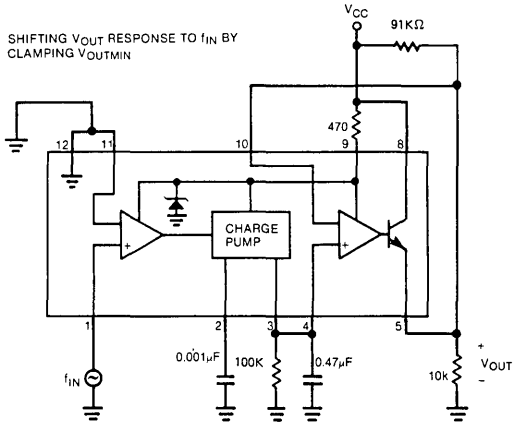


Figure 11. Delaying V_{OUT} Response to f_{in}

This circuit will not react until

$$f_{in} = \left(\frac{V_{CC}}{10}\right)(V_Z \times R_1 \times C_1)^{-1}$$

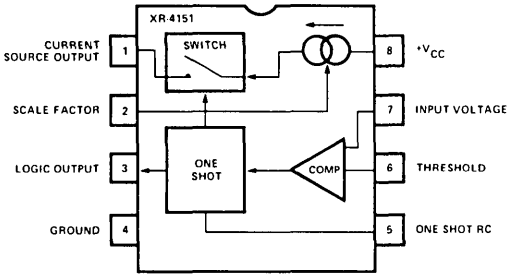
8

Voltage-to-Frequency Converter

GENERAL DESCRIPTION

The XR-4151 is a device designed to provide a simple, low-cost method for converting a DC voltage into a proportional pulse repetition frequency. It is also capable of converting an input frequency into a proportional output voltage. The XR-4151 is useful in a wide range of applications including A/D and D/A conversion and data transmission.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Single Supply Operation (+8V to +22V)
Pulse Output Compatible With All Logic Forms
Programmable Scale Factor (K)
Linearity ±0.05% Typical–Precision Mode
Temperature Stability ±100% ppm/°C Typical
High Noise Rejection
Inherent Monotonicity
Easily Transmittable Output
Simple Full Scale Trim
Single-Ended Input, Referenced to Ground
Also Provides Frequency-to-Voltage Conversion
Direct Replacement for RC/RV/RM-4151

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4151P	Plastic	−40°C to +85°C
XR-4151CP	Plastic	0°C to +70°C

APPLICATIONS

Voltage-to-Frequency Conversion
A/D and D/A Conversion
Data Transmission
Frequency-to-Voltage Conversion
Transducer Interface
System Isolation

ABSOLUTE MAXIMUM RATINGS

Power Supply	22V
Output Sink Current	20 mA
Internal Power Dissipation	500 mW
Input Voltage	−0.2V to +V_{CC}
Output Short Circuit to Ground	Continuous

SYSTEM DESCRIPTION

The XR-4151 is a precision voltage to frequency convertor featuring 0.05% conversion linearity, high noise rejection, monotonicity, and single supply operation from 8V to 22V. An RC network on Pin 5 sets the maximum full scale frequency. Input voltage on Pin 7 is compared with the voltage on Pin 6 (which is generally controlled by the current source output, Pin 1). Frequency output is proportioned to the voltage on Pin 7. The current source is controlled by the resistance on Pin 2 (nominally 14kΩ) with I = 1.9 V/R. The output is an open collector at Pin 3.

ELECTRICAL CHARACTERISTICS

Test Conditions: (V_{CC} = 15V, T_A = +25°C, unless otherwise specified)

	LIMITS				
PARAMETERS	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
Supply Current	2.0 2.0	3.5 4.5	6.0 7.5	mA mA	8V<V_{CC}<15V 15V<V_{CC}<22V
Conversion Accuracy Scale Factor	0.90	1.00	1.10	kHz/V	Circuit of Figure 3, V_I = 10V R_S = 14. Ok
Drift with Temperature	–	±100	–	ppm/°C	Circuit of Figure 3, V_I = 10V
Drift with V_{CC}	–	0.2	1.0	%/V	Circuit Figure 3, V_I = 1.0V 8V< V_{CC}< 18V
Input Comparator Offset Voltage Offset Current Input Bias Current Common Mode Range (Note 1)	 – – – 0	 5 ±50 –100 0 to V_{CC}–2	 10 ±100 –300 V_{CC}–3.0	 mV nA nA V	
One-Shot Threshold Voltage, Pin 5 Input Bias Current, Pin 5 Reset V_{SAT}	 0.63 – –	 .667 –100 0.15	 0.70 –500 0.50	 x V_{CC} nA V	 Pin 5, 1 = 2.2mA
Current Source Output Current Change with Voltage Off Leakage	 – – –	 138.7 1.0 1	 – 2.5 50.0	 μA μA nA	 Pin 1, V = 0, R_S = 14.0kΩ Pin 1, V = 0V to V = 10V Pin 1, V = 0V
Reference Voltage	1.70	1.9	2.08	V	Pin 2
Logic Output V_{SAT} V_{SAT} Off Leakage	 – – –	 0.15 0.10 .1	 0.50 0.30 1.0	 V V μA	 Pin 3, 1 = 3.0mA Pin 3, 1 = 2.0mA

Note 1: Input Common Mode Range includes ground.

PRINCIPLES OF OPERATION

SINGLE SUPPLY MODE VOLTAGE-TO-FREQUENCY CONVERTER

In this application, the XR-4151 functions as a stand-alone voltage-to-frequency converter operating on a single positive power supply. Refer to the functional block diagram and Figure 3, the circuit connection for single supply voltage-to-frequency conversion. The XR-4151 contains a voltage comparator, a one-shot, and a precision switched current source. The voltage comparator compares a positive input voltage applied at pin 7 to the voltage at pin 6. If the input voltage is higher, the comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T, the logic output will go low and the current source will turn on with current I. At the end of the one shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge Q = I_OT into the network R_B–C_B. If this charge has not increased the voltage V_B such that V_B > V_I, the comparator again fires the one-shot and the current source injects another lump of charge, Q, into the R_B–C_B network. This process continues until V_B > V_I. When this condition is achieved, the current source remains off and the voltage V_B decays until V_B is again equal to V_I. This completes one cycle. The VFC will now run in a steady state mode. The current source dumps lumps of charge into the capacitor C_B at a rate fast enough to keep V_B ≥ V_I. Since the discharge rate of capacitor C_B is proportional to V_B/R_B, the frequency at which the system runs will be proportional to the input voltage.

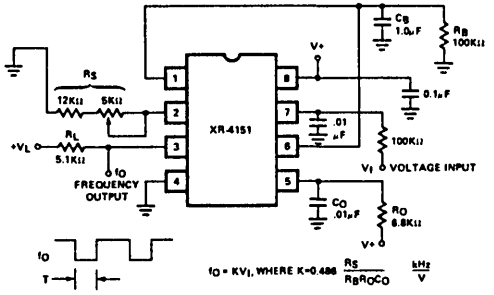


Figure 3. Voltage-to-Frequency Converter

TYPICAL APPLICATIONS

SINGLE SUPPLY VOLTAGE-TO-FREQUENCY CONVERTER

Figure 3 shows the simplest type of VFC that can be made with the XR-4151. The input voltage range is from 0 to +10V, and the output frequency is from 0 to 10 kHz. The full scale frequency can be tuned by adjusting R_S, the output current set resistor. This circuit has the advantage of being simple and low in cost, but it suffers from inaccuracy due to a number of error sources. Linearity error is typically 1%. A frequency offset will also be introduced by the input comparator offset voltage. Also, response time for this circuit is limited by the passive integration network R_B C_B. For the component values shown in Figure 3, response time for a step change input from 0 to +10V will be 135 msec. For applications which require fast response time and high accuracy, use the circuit of Figure 4.

PRECISION VOLTAGE-TO-FREQUENCY CONVERTER

In this application (Figure 4) the XR-4151 is used with an operational amplifier integrator to provide typical linearity of 0.05% over the range of 0 to −10V. Offset is adjustable to zero. Unlike many VFC designs which lose linearity below 10mV, this circuit retains linearity over the full range of input voltage, all the way to 0V.

Trim the full scale adjust pot at V_I = −10V for an output frequency of 10kHz. The offset adjust pot should be set for 10Hz with an input voltage of −10mV.

The operational amplifier integrator improves linearity of this circuit over that of Figure 3 by holding the output of the source, Pin 1, at a constant 0V. Therefore, the linearity error due to the current source output conductance is eliminated. The diode connected around the op-amp prevents the voltage at pin 7 of the XR-4151 from going below 0. Use a low-leakage diode here, since any leakage will degrade the accuracy. This circuit can be operated from a single positive supply if an XR-3403 ground-sensing op-amp is used for the integrator. In this case, the diode can be left out. Note that even though the circuit itself will operate from a single supply, the input voltage is necessarily negative. For operation above 10kHz, bypass pin 6 of the XR-4151 with .01μF.

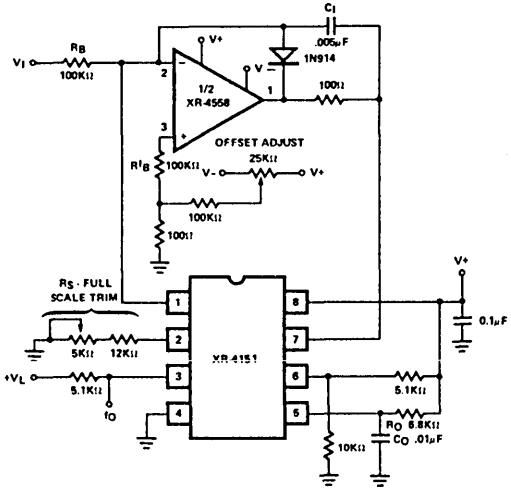


Figure 4. Precision Voltage-to-Frequency Converter

FREQUENCY-TO-VOLTAGE CONVERSION

The XR-4151 can be used as a frequency-to-voltage converter. Figure 5 shows the single-supply FVC configuration. With no signal applied, the resistor bias networks tied to pins 6 and 7 hold the input comparator in the off state. A negative going pulse applied to pin 6 (or positive pulse to pin 7) will cause the comparator to fire the one-shot. For proper operation, the pulse width must be less than the period of the one-shot, T = 1.1 R_0 C_0. For a 5V p-p square-wave input the differentiator network formed by the input coupling capacitor and the resistor bias network will provide pulses which correctly trigger the one-shot. An external voltage comparator can be used to "square-up" sinusoidal input signals before they are applied to the XR-4151. Also, the component values for the input signal differentiator and bias network can be altered to accommodate square waves with different amplitudes and frequencies. The passive integrator network R_B C_B filters the current pulses from the pin 1 output. For less output ripple, increase the value of C_B.

For increased accuracy and linearity, use an operational amplifier integrator as shown in Figure 6, the precision FVC configuration. Trim the offset to give −10mV out with 10Hz in and trim the full scale adjust for −10V out with 10kHz in. Input signal conditioning for this circuit is necessary just as for the single supply mode and the scale factor can be programmed by the choice of component values. A tradeoff exists between the amount of output ripple and the response time, through the choice or integration capacitor C_I. If C_I = 0.1 μf the ripple will be about 100mV. Response time constant τR = R_B C_I. For R_B = 100 kΩ and C_I = 0.1 μf, τR = 10msec.

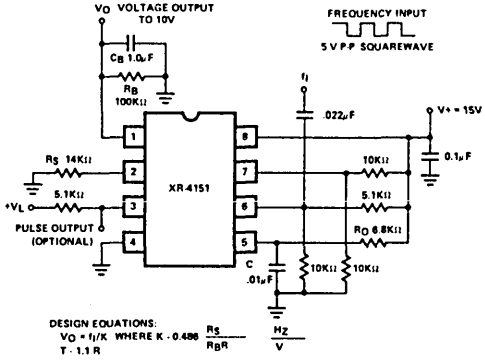


Figure 5. Frequency-to-Voltage Converter

PRECAUTIONS

1. The voltage applied to comparator input pins 6 and 7 should not be allowed to go below ground by more than 0.3 volt.

2. Pins 3 and 5 are open-collector outputs. Shorts between these pins and $+V_{CC}$ can cause overheating and eventual destruction.

3. Reference voltage terminal pin 2 is connected to the emitter of an NPN transistor and is held at approximately 1.9 volts. This terminal should be protected from accidental shorts to ground or supply voltages. Permanent damage may occur if the current in pin 2 exceeds 5mA.

4. Avoid stray coupling between pins 5 and 7; it could cause false triggering. For the circuit of Figure 3, bypass pin 7 to ground with at least 0.01μf. This is necessary for operation above 10kHz.

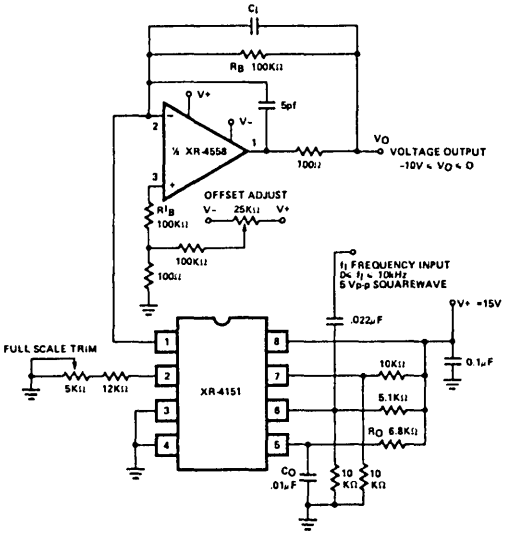


Figure 6. Precision Frequency-to-Voltage Converter

PROGRAMMING THE XR-4151

The XR-4151 can be programmed to operate with a full scale frequency anywhere from 1.0Hz to 100kHz. In the case of the VFC configuration, nearly any full scale input voltage from 1.0V and up can be tolerated if proper scaling is employed. Here is how to determine component values for any desired full scale frequency.

1. Set R_S = 14kΩ or use a 12k resistor and 5k pot as shown in the figures. (The only exception to this is Figure 4.)

2. Set $T = 1.1\ R_0C_0 = 0.75[1/fo]$ where fo is the desired full scale frequency. For optimum performance make 6.8kΩ $> R_0 >$ 680kΩ and 0.001μf $< C_0 <$ 1.0μf.

3. a) For the circuit of Figure 3 make $C_B = 10^{-2}$ [1/fo] Farads.

   Smaller values of C_B will give a faster response time, but will also increase the frequency offset and nonlinearity.

   b) For the active integrator circuit make

   $C_I = 5 \times 10^{-5}$ [1/fo] Farads.

   The op-amp integrator must have a slew rate of at least 135×10^{-6} [$1/C_1$] volts per second where the value of C_1 is in Farads.

4. a) For the circuit of Figure 4 keep the values of R_B and R_B as shown and use an input attenuator to give the desired full scale input voltage.

   b) For the precision mode circuit of Figure 4, set $R_B = V_{IO}/100\mu A$ where V_{IO} is the full scale input voltage.

   Alternately, the op-amp inverting input (summing node) can be used as a current input with the full scale input current $I_{IO} = -100\mu A$.

5. For the FVC's, pick the value of C_B or C_I to give the optimum tradeoff between the response time and output ripple for the particular application.

DESIGN EXAMPLE

I. Design a precision VFC (from Figure 5) with fo = 100kHz and $V_{IO} = -10V$.

1. Set R_S = 14.0kΩ

2. $T = 0.75\ [1/10^5] = 7.5\mu$sec

   Let R_0 = 6.8kΩ and C_0 = 0.001μf.

3. $C_I = 5 \times 10^5\ [1/10^5] = 500$pf.

   Op-amp slew rate must be at least

   $SR = 135 \times 10^6\ [1/500pf] = 0.27V/\mu$sec

4. R_B = 10V/100μA = 100kΩ.

II. Design a precision VFC with fo = 1Hz and V_{IO} = 10V.

1. Let R_S = 14.0kΩ

2. $T = 0.75\ [1/1] = 0.75$ sec

   Let R_0 = 680kΩ and C_0 = 1.0μf.

3. $C_I = 5 \times 10^{-5}\ [1/1]F = 50\mu$f.

4. R_B = 100kΩ.

III. Design a single supply FVC to operate with a supply voltage of 9V and full scale input frequency fo = 83.3 Hz. The output voltage must reach at least 0.63 of its final value in 200msec. Determine the output ripple.

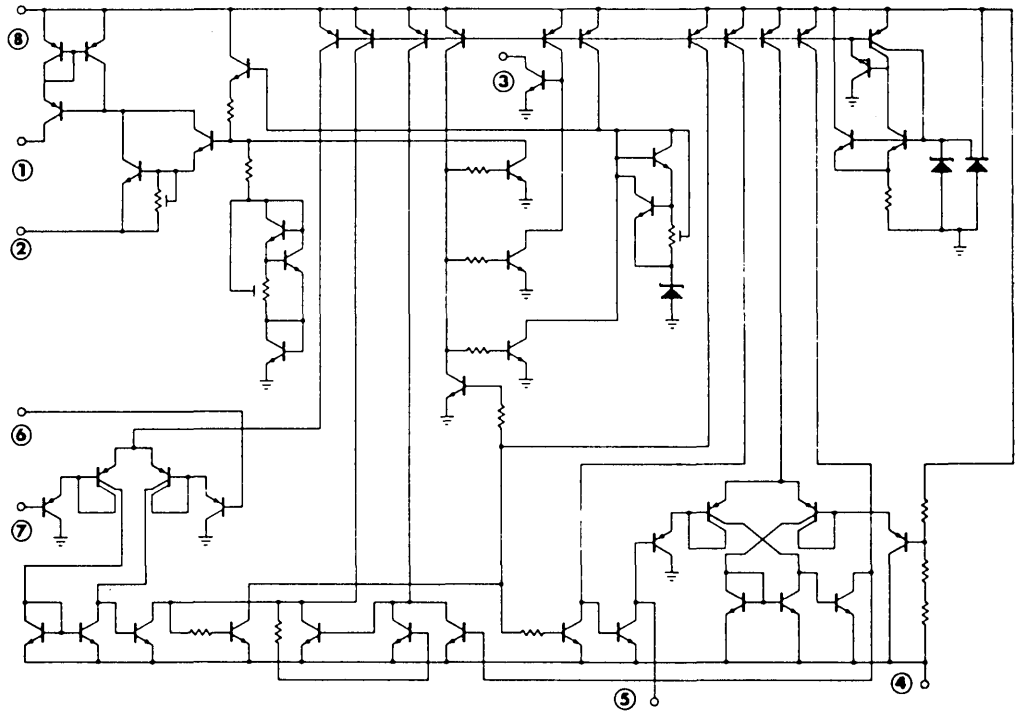
1. Set R_S = 14.0kΩ
2. T = 0.75 [1/83.3] = 9msec

   Let R_0 = 82kΩ and C_O = 0.1 μf.
3. Since this FVC must operate from 8.0V, we shall make the full scale output voltage at pin 6 equal to 5.0V.
4. R_B = 5V/100μA = 50kΩ.
5. Output response time constant is $\tau R \leq 200$ msec
   Therefore-

   $C_B \leq \tau_R/R_B = (200 \times 10^{-3})/(50 \times 10^3) = 4\mu f$

   Worst case ripple voltage is

   $V_R = (9mS \times 135\mu A) / 4\mu f = 304mV.$



EQUIVALENT SCHEMATIC DIAGRAM

8-Bit Microprocessor Compatible Digital-To-Analog Converter

GENERAL DESCRIPTION

The XR-9201 is a monolithic 8-Bit μP compatible digital-to-analog converter with differential current outputs. It contains an internal data latch, making it suitable for interfacing with microprocessors. The chip contains a stable voltage reference (2.0 V Nominal) which is externally adjustable and can be used as a reference for other D/A and A/D converters.

The XR-9201 features non-linearity of ± ½ LSB maximum (±.19% of full scale current). The internal voltage reference maintains a temperature coefficient of 50 ppm/°C.

FEATURES

8-Bit Resolution	
Input Data Latches	
Internal Voltage Reference	
Microprocessor Compatible	
Non Linearity	± ½ LSB Maximum
Full Scale Current Stability	±50 ppm/°C
Reference Voltage Stability	±50 ppm/°C
Differential Current Outputs	
TTL Compatible	

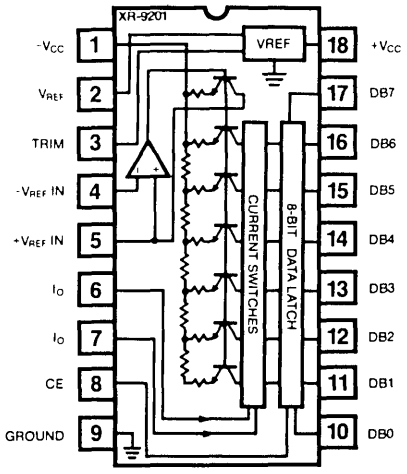
APPLICATIONS

Bipolar and Unipolar D/A Conversion
A/D Conversion
Test Equipment
Measuring Instruments
Programmable Current Source
Programmable Voltage Source

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ Positive Supply Voltage	+6V
$-V_{CC}$ Negative Supply Voltage	−8.5V
Logic Input Voltages	0 to +6V
Power Dissipation	500 mW
Derate Above 25°C	5 mW/°C
Storage Temperature	−55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-9201 CP	Plastic	0° to +70°C

SYSTEM DESCRIPTION

To convert the output currents of the digital-to-analog converter to a voltage, an operational amplifier can be used as shown in Figure 12.

Care must be taken in selecting an operational amplifier to be used in D/A conversion. For accurate conversion, the operational amplifier should have low input offset voltage, low input bias and offset currents, and fast settling times. Input offset voltage contributes a DC error on the output and should be properly nulled. Input bias current contributes to the D/A converter current flowing through the feedback resistor, R_{FB}, and also causes a DC error on the output voltage. This error can be reduced by the addition of a resistor equal in value to R_{FB} from the noninverting input to ground. Settling time is important because it rules how fast the output reaches its prescribed voltage level. The OP-01 is suitable for D/A converter applications producing negligible errors.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, $-V_{CC}$ = −7V, T_A = 25°C, I_{REF} = 1.0 mA, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
	Resolution	8	8	8	Bits	
	Monotonicity	8	8	8	Bits	
	Non-linearity			±0.5 ±0.19	LSB %I_{FS}	
$+V_{CC}$	Positive Supply Voltage	4.5	5.0	5.5	V	
$-V_{CC}$	Negative Supply Voltage	−7.7	−7.0	−6.3	V	
V_{IH}	Data Input and Chip Enable "High" Voltage	2.0			V	
V_{IL}	Data Input and Chip Enable "Low" Voltage			0.8	V	
I_{IH}	Data Input and Chip Enable "High" Current			500	μA	
I_{IL}	Data Input and Chip Enable "Low" Current			±20	μA	
I_{FS}	Full Scale Output Current	1.914	1.992	2.070	mA	I_{REF} = 1.000 mA
I_{ZO}	Zero Scale Output Current			±10	μA	
TC_{IFS}	Full Scale Current Temperature Sensitivity		±50		ppm/°C	0°C ≤ T_A ≤ 75°C
I_{FSS}	Full Scale Symmetry			±10	μA	
V_{REF}	Internal Reference Voltage	2.005	 2.000	1.990	V	R_{ADJ} = 50 KΩ R_{ADJ} = 0 Ω R_{ADJ} = 6 Ω
TC_{REF}	V_{REF} Temperature Stability		±50		ppm/°C	V_{REF} = 2.00 V
$+I_{CC}$	Positive Supply Current		15	25	mA	
$-I_{CC}$	Negative Supply Current	−25	−15		mA	
	Positive Output Voltage Compliance		+5.0		V	
	Negative Output Voltage Compliance		−1.0		V	
	Maximum Full Scale Current		3		mA	
t_S	Settling Time		600		nsec	
t_{SU}	Data Set-up Time		170		nsec	
t_H	Data Hold Time		40		nsec	
t_W	Minimum Chip Enable (CE) Pulse Width		170		nsec	
t_D	Propagation Delay Time		500		nsec	

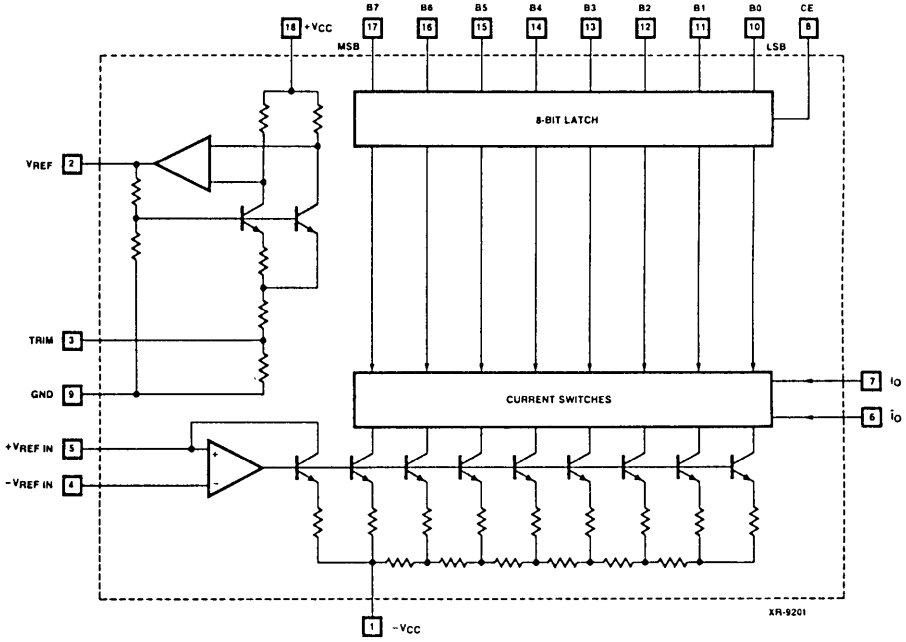


Figure 2. Functional Block Diagram

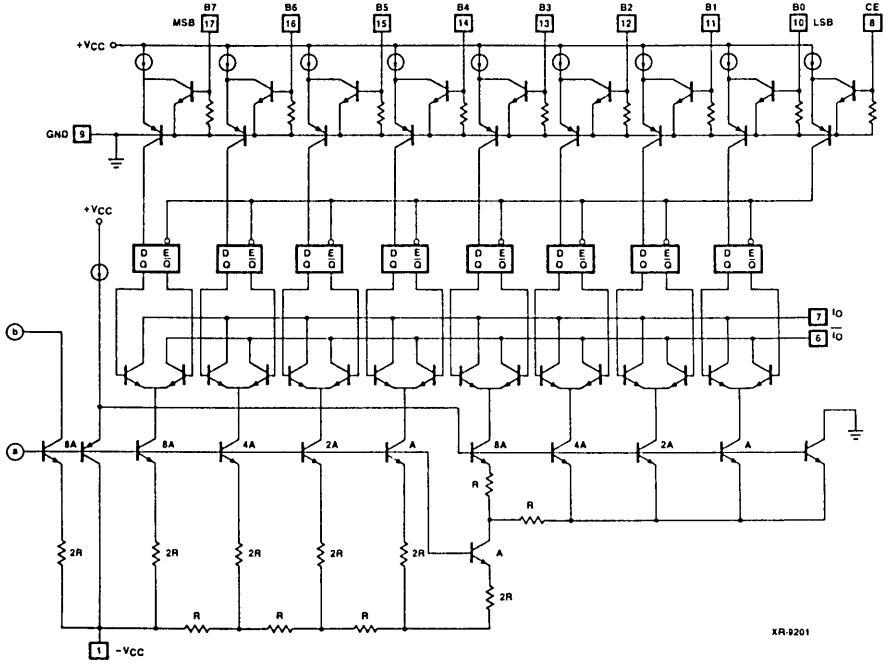


Figure 3A. Equivalent Circuit of Data Latches and Current Switches

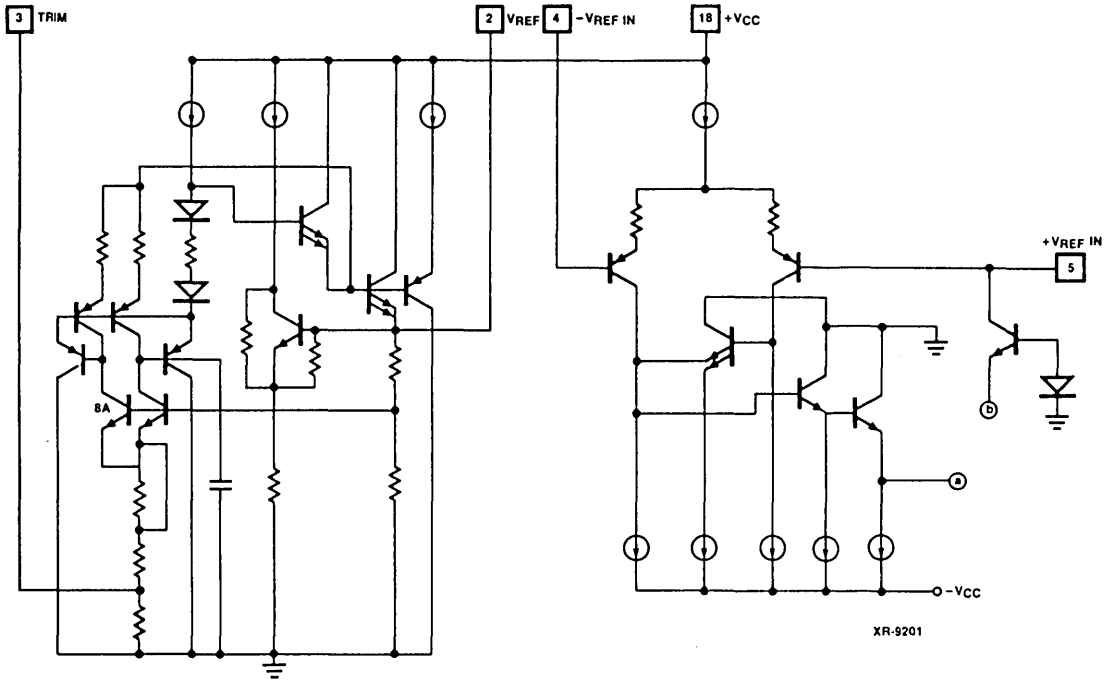


Figure 3B. Equivalent Circuit of Voltage Reference and Input Amplifier

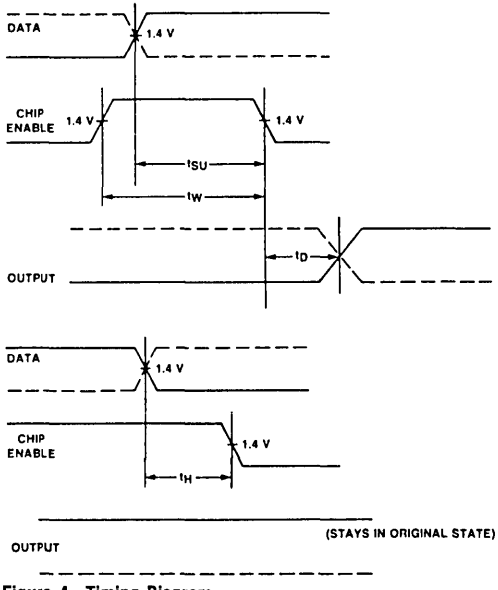


Figure 4. Timing Diagram

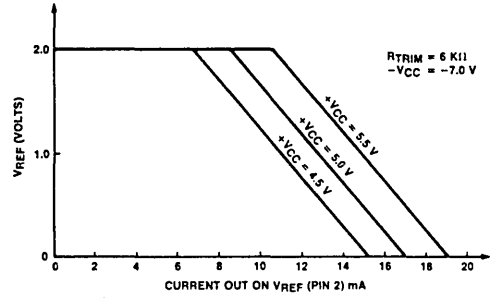


Figure 5. V_{REF} vs. Current Output

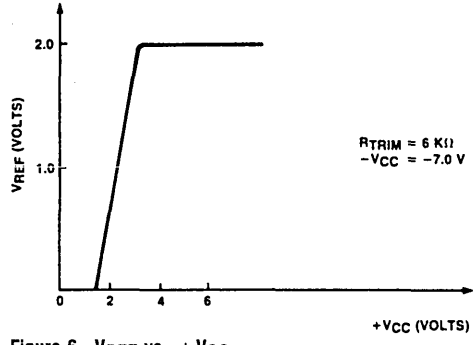


Figure 6. V_{REF} vs. $+V_{CC}$

DEFINITIONS OF SWITCHING PARAMETERS

Settling Time (t_S): Time required for output to reach its final value (to within ±.19% of full scale output) after data is applied to the inputs. Chip enable, CE, is held "high."

Data Set-Up Time (t_{SU}): Minimum time required for data to be present at the inputs while CE is "high", in order to obtain valid output data. It is measured from when proper data is applied to the inputs to when CE goes "low".

Data Hole Time (t_h): Maximum time required for data to be present at the inputs before CE goes "low", in order to obtain valid output data. It is measured from when the input data changes state to when CE goes "low", and still obtain valid output data of the previous input state. Data hold time indicates that the input data does not have to be present during the latter part of the CE high state, and still have valid output data.

Chip Enable Pulse Width (t_W): Minimum pulse width required for chip enable signal in order to obtain valid output data.

Propagation Delay Time (t_d): Time required for output to reach its final value (50%) after CE is applied. It is measured from the falling edge of the CE pulse to 50% of the output pulse under minimum data set-up time conditions.

DESCRIPTION OF PIN CONTROLS

V_{REF} (PIN 2): Internal voltage reference output provides +2.00 V Nominal voltage. Can be used as reference voltage for other circuitry. Maximum output current capability is approximately 9 mA with V^+ = 5.0 V.

TRIM (PIN 3): V_{REF} can be adjusted by connecting a 10 KΩ potentiometer between the trim pin and ground. Temperature stability is optimized for V_{REF} = 2.00 V to 10–50 ppm/°C.

$-V_{REF}$ IN (PIN 4): This pin is tied to ground through a resistor, R, equal in value to that of Pin 5 and V_{REF}.

$+V_{REF}$ IN (PIN 5): Reference voltage is connected to this pin using a resistor, R, to provide the reference current, I_{REF}, for the D/A converter. Either the internal V_{REF} (Pin 2) or an external V_{REF} can be connected to this pin. I_{REF} is approximately equal to V_{REF}/R. Maximum value for I_{REF} is about 1.5 mA before internal saturation occurs.

$\overline{I_O}$ (PIN 6): Complement output current.

I_O (PIN 7): Output current. The sum of $\overline{I_O}$ and I_O is always equal to the full scale output current (I_{FS}).

CE (PIN 8): Chip enable pin controls the input data into the internal data latch. The latch is transparent in the "high" state.

DB0–DB7 (PIN 10–17): Data input pins. DB0 corresponds to the LSB. DB7 corresponds to the MSB.

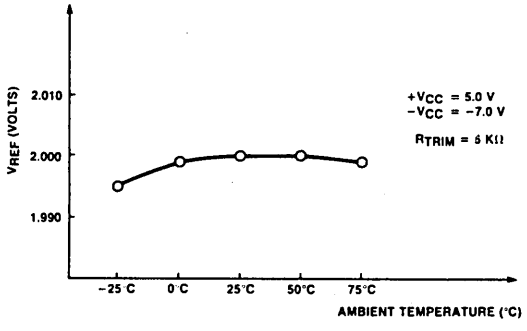


Figure 7. V_{REF} vs. Temperature

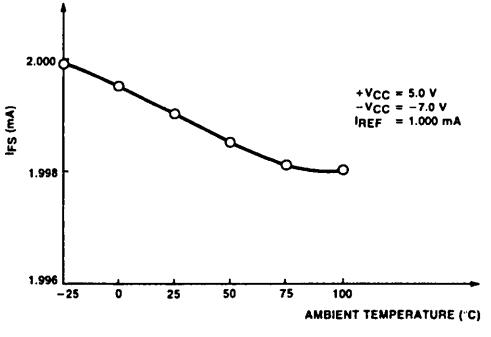


Figure 8. I_{FS} vs. Temperature

PRINCIPLES OF OPERATION

Figure 10 shows the basic configuration of the XR-9201 D/A converter. The input data bits to the chip can be latched (stored) in the D/A by controlling the chip enable (CE) pin. When CE is "high" (>2.0 volts), the latch is transparent and data bits present are passed through the latch and directly control the D/A converter switches. When CE is "low" (<0.8 volts), the data bits within the latch are retained and remain there until CE goes "high" again. When CE is "low", the data bits at the inputs are ignored until CE goes "high". This interval latch provides a useful interface with microprocessors.

The output currents, I_O and $\overline{I}_O$, are related to I_{REF} as follows:

$$I_O = 2\,I_{REF}\left[\frac{b_7}{2}+\frac{b_6}{4}+\frac{b_5}{8}+\frac{b_4}{16}+\frac{b_3}{32}+\frac{b_2}{64}+\frac{b_1}{128}+\frac{b_0}{256}\right]$$

Where: b_n = 1 if Bit N is "High"
= 0 if Bit N is "Low"
b_7 = MSB (Pin 17)
b_0 = LSB (Pin 10)

$\overline{I}_O$ is the complement current output of I_O. For all possible input data combinations,

$I_O + \overline{I}_O = I_{FS}$ = full scale output current.

where $I_{FS} = 2\,I_{REF}\left(\frac{255}{256}\right)$

The XR-9201 D/A converter contains an internal reference voltage (V_{REF}) with nominal value of 2.00V using a 6 KΩ resistor to ground. V_{REF} can be adjusted using a 10 KΩ potentiometer tied between Pin 3 and ground. For maximum temperature stability, V_{REF} should be set to 2.00V. The maximum output current capability of V_{REF} is about 9 mA (see Figure 5) and can be used to provide a reference voltage for other DACs, as well as other circuitry.

The reference current (I_{REF}) for the D/A converter is established by a resistor, R, connected between V_{REF} and Pin 5 (+V_{REF} IN), or between an external reference source and Pin 5, and is approximately given as:

$$I_{REF} = \frac{V_{REF}}{R}$$

For $I_{REF} \leq 1$ mA. The maximum I_{REF} allowed is about 1.5 mA beyond which saturation occurs in the internal circuitry. To balance the internal operational amplifier, a resistor equal to R must be placed between Pin 4 (−V_{REF} IN) and ground.

NOTE:
When operating the XR-9201 D/A converter with an operational amplifier, care must be taken with the PC board layout. Specifically, connection between the current output terminals, I_O and $\overline{I}_O$, and the operational amplifier inputs needs to be as short as possible so as to minimize capacitance at the node. Oscillations on the operational amplifier output may result with long wires. A capacitor in the feedback loop of the operational amplifier can reduce these oscillations.

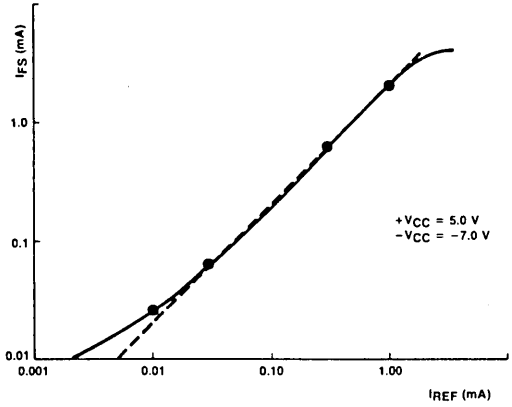


Figure 9. I_{FS} vs. I_{REF}

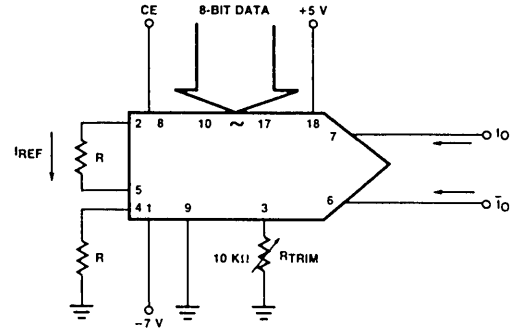


Figure 10. Basic Configuration

ZERO AND FULL SCALE ADJUSTMENTS

Figure 13 shows a circuit for zero and full scale adjustments. It allows the output voltage to be nulled with zero scale input conditions (0000,0000). This is done by shorting out R_{FB} and adjusting the VOS adjust potentiometer of the operational amplifier until the output reads zero volts. This is performed with all digital bits set to zeros. If $\overline{I}_O$ is the output being used, then all digital bits are set to ones and the zero scale is adjusted.

For full scale adjustment, all digital inputs are set to ones and the I_{REF} potentiometer, from Pin 2 to Pin 5, is adjusted until the output is at the desired voltage level (e.g., output is adjusted to 10.000 volts for nominal 9.960 volts output).

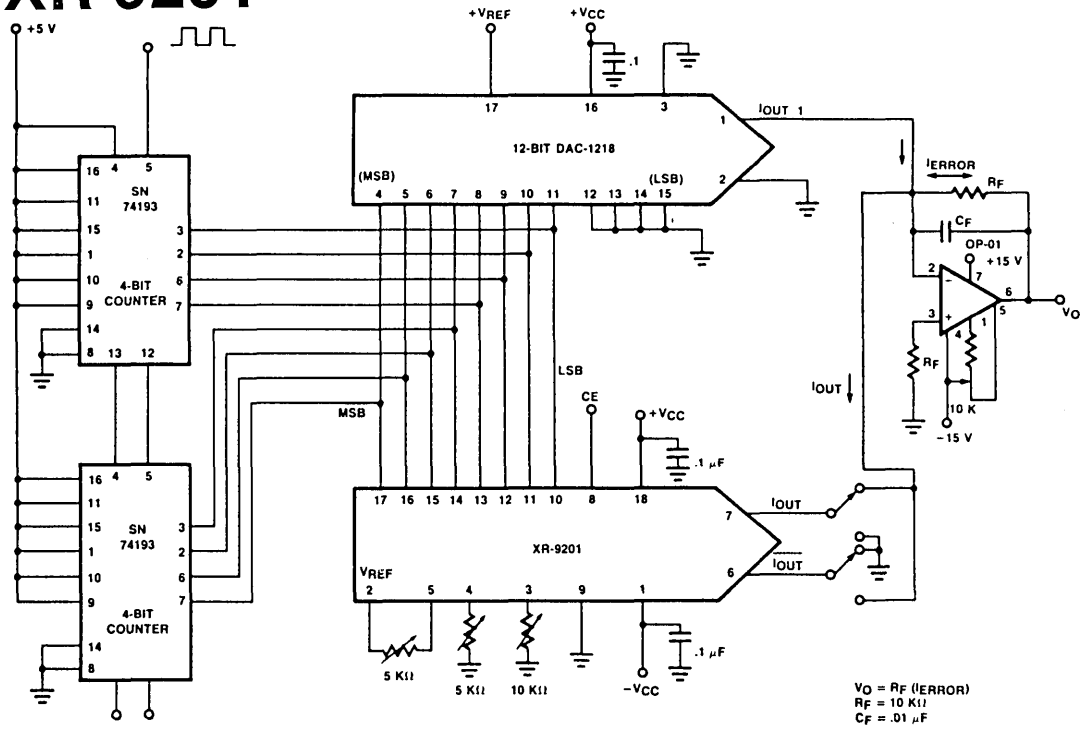
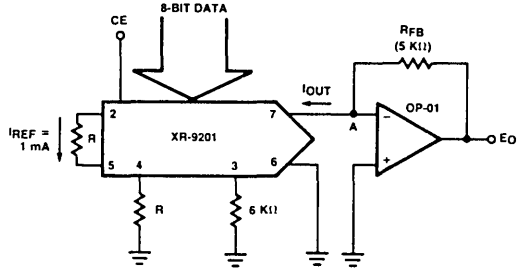


Figure 11. Relative Accuracy Test Circuit



0 V ≤ E_O ≤ 10 V FOR R_{FB} = 5 KΩ, I_{REF} = 1 mA

$I_{FS} = 2(I_{REF})\ (255/256)$

FOR OPERATION WITH NEGATIVE LOGIC D/A CONVERSION, I.E. ZERO FULL SCALE (0000 0000) CORRESPONDING TO FULL SCALE OUTPUT, CONNECT THE INVERTING INPUT OF OP AMP TO I_O (PIN 6) AND CONNECT I_O (PIN 7) TO GROUND.

Figure 12. Digital-to-Analog Conversion: Unipolar Operation

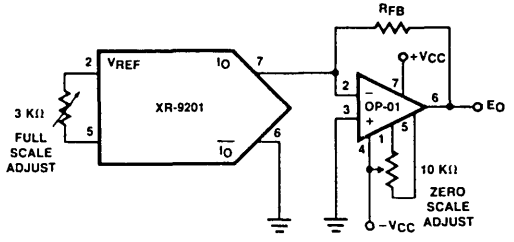


Figure 13. Full Scale and Zero Scale Adjustment

Table 1. Unipolar Operation — Input/Output Relationship

	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	I_O (mA)	E_O (V)
Positive Full Scale	1	1	1	1	1	1	1	1	1.992	9.960
Pos. Full Scale – LSB	1	1	1	1	1	1	1	0	1.984	9.922
Pos. Full Scale – MSB	0	1	1	1	1	1	1	1	0.992	4.961
Zero Full Scale + LSB	0	0	0	0	0	0	0	1	0.008	0.039

Table 2. Bipolar Operation: Input/Output Relationship

	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	E_1 (V)	E_0 (V)
Full Scale Output	1	1	1	1	1	1	1	1	0.000	10.00
Full Scale – LSB	1	1	1	1	1	1	1	0	0.016	9.921
Zero Scale + MSB	1	0	0	0	0	0	0	0	1.984	0.078
Full Scale – MSB	0	1	1	1	1	1	1	1	2.000	0.000
Zero Scale + LSB	0	0	0	0	0	0	0	1	3.968	–9.844
Zero Scale	0	0	0	0	0	0	0	0	3.984	–9.922

BIPOLAR OUTPUT OPERATION

Figure 14 shows a basic bipolar output operation. For full scale input (1111,1111) the output voltage is equal to 1.0V. For zero scale input (0000,0000), output voltage is equal to –1.0V. Due to the internal circuitry of the XR-9201, the current output terminals should not be pulled below approximately –1.0 volt. Therefore the circuit shown in Figure 14 would not function for E_O less than –1.0V. For bipolar operation with larger output voltages, the circuit shown in Figure 15 is recommended. Note that the current outputs, I_O and $\overline{I_O}$, are held at zero volts for all digital inputs for greater accuracy.

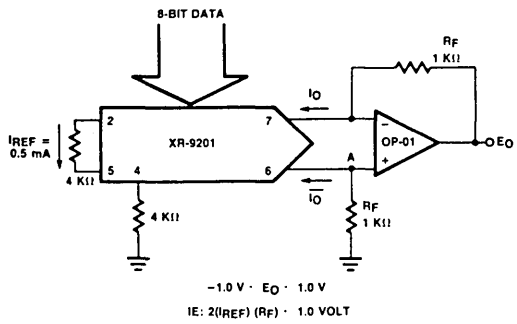


Figure 14. Digital-to-Analog Conversion — Bipolar Operation

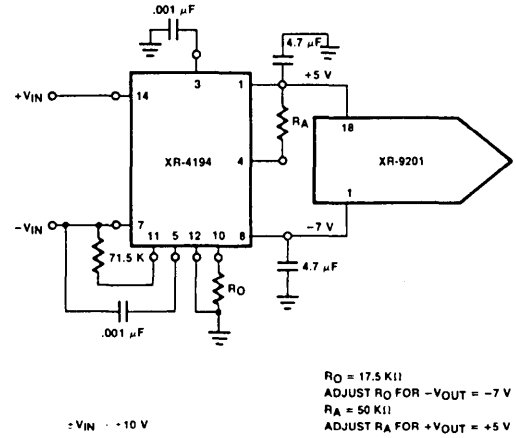
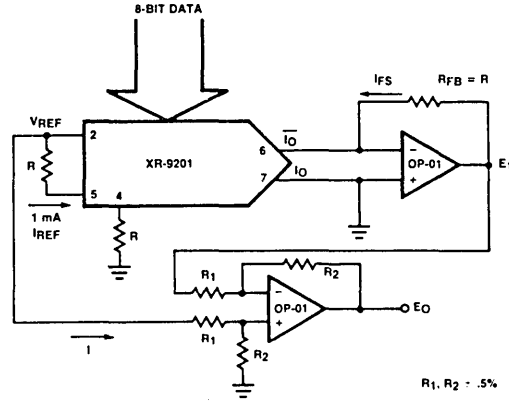


Figure 15. Digital-to-Analog Conversion — Bipolar Operation



$$E_O = \frac{R_2}{R_1}\left(V_{REF} \cdot E_1\right)$$

V_{REF} = 2 V, R = 2 K, R_{FB} = 2 K, R_2 = 50 K, R_1 = 10 K

NOTE: (I + I_{REF}) MUST BE LESS THAN 6 mA FOR PROPER OPERATION.

Figure 16. Regulated Supplies for XR-9201

Dual Operational Transconductance Amplifier

GENERAL DESCRIPTION

The XR-13600 is a dual operational transconductance (Norton) amplifier with predistortion diodes and non-committed Darlington buffer outputs.

The device is especially suitable for electronically controllable gain amplifiers, controlled frequency filters, an other applications requiring current or voltage adjustments.

FEATURES

Direct Replacement for LM-13600 and LM-13600 A
Transconductance Adjustable Over 4 Decades
Excellent Transconductance-Control Linearity
Uncommitted Darlington Output Buffers
On-Chip Predistortion Diodes
Excellent Matching Between Amplifiers
Wide Supply Range: ±2V to ±18V

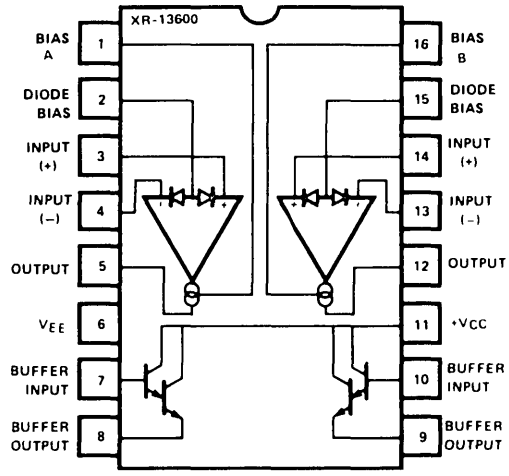
APPLICATIONS

Current-Controlled Amplifiers
Current-Controlled Impedances
Current-Controlled Filters
Current-Controlled Oscillators
Multipliers/Attenuators
Sample and Hold Circuits
Electronic Music Synthesis

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (See Note 1)	±22 V
Power Dissipation (T_A = 25°C, see Note 2)	625 mW
Derate Above 25°C	5 mW/°C
DC Input Voltage	$+V_{CC}$ to $-V_{EE}$
Differential Input Voltage	±5 V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_B)	2 mA
Output Short Circuit Duration	Indefinite
Buffer Output Current (Note 3)	20 mA
Storage Temperature Range	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-13600AP	Plastic	0°C to + 70°C
XR-13600CP	Plastic	0°C to + 70°C

SYSTEM DESCRIPTION

The XR-13600 consists of two programmable transconductance amplifiers with high input impedance and push-pull outputs. The two amplifiers share common supplies but otherwise operate independently. Each amplifier's transconductance is directly proportional to its applied bias current. To improve signal-to-noise performance, predistortion diodes are included on the inputs; the use of these diodes results in a 10 dB improvement referenced to 0.5% THD. Independent Darlington emitter followers are included to buffer the outputs.

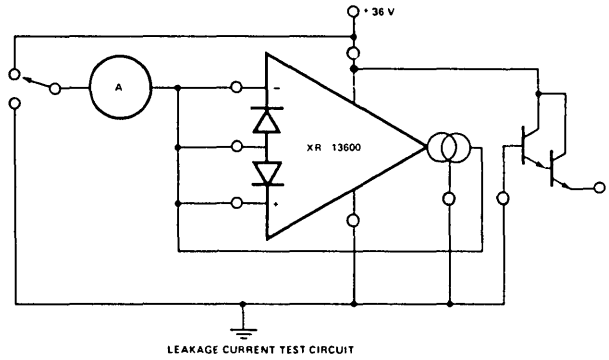
XR-13600

ELECTRICAL CHARACTERISTICS

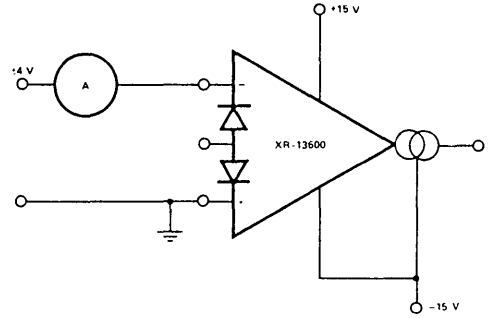
Test Conditions: T_A = +25°C, Supply Voltage = ±15V, unless otherwise specified.

PARAMETERS	XR-13600A			XR-13600C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
Input Offset Voltage (V_{OS})		0.4	2		0.4	5	mV	
			5				mV	Over Temperature Range
		0.3	2		0.3	5	mV	I_B = 5μA
V_{OS} Including Diodes		0.5	2		0.5	5	mV	Diode Bias Current (I_D) = 500 μA
Input Offset Change		0.1	3		0.1		mV	5μA ≤ I_B ≤ 500μA
Input Offset Current		0.1	0.6		0.1	0.6	μA	
Input Bias Current		0.4	5		0.4	5	μA	T_A = 25°C
		1	7		1	8	μA	Over Temperature Range
Forward Transconductance (g_m)	7700	9600	12000	6700	9600	13000	μmho	T_A = 25°C
	4000			5400			μmho	Over Temperature Range
g_m Tracking		0.3			0.3		dB	
Peak Output Current	3	5	7		5		μA	RL = 0, I_B = 5μA
	350	500	650	350	500	650	μA	RL = 0, I_B = 500μA
	300			300			μA	RL = 0, Over Specified Temp Range
Peak Output Voltage								
Positive	+12	+14.2		+12	+14.2		V	RL = ∞, 5 μA ≤ I_B ≤ 500 μA
Negative	−12	−14.4		−12	−14.4		V	RL = ∞, 5 μA ≤ I_B ≤ 500 μA
Supply Current		2.6			2.6		mA	I_B = 500 μA, Both Channels
V_{OS} Sensitivity								
Positive		20	150		20	150	μV/V	Δ V_{OS}/Δ V +
Negative		20	150		20	150	μV/V	Δ V_{OS}/Δ V −
CMRR	80	110		80	110		dB	
Common Mode Range	±12	±13.5		±12	±13.5		V	Referred to Input (Note 5)
Channel Separation		100			100		dB	20 Hz < f < 20 KHz
Diff. Input Current		0.02	10		0.02	100	nA	I_B = 0, Input = ±4 V
Leakage Current		0.2	5		0.2	100	nA	I_B = 0 (refer To Test Circuit)
Input Resistance	10	26		10	26		KΩ	
Open Loop Bandwidth		2			2		MHz	
Slew Rate		50			50		V/μSec	Unity Gain Compensated
Buff. Input Current		0.4	5		0.4	5	μA	(Note 5)
Peak Buffer Output Voltage	10			10			V	(Note 5)

TEST CIRCUITS



LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

Note 1. For selections to a supply voltage above ±22 V, contact factory.

Note 2. For operating at high temperatures, the device may be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.

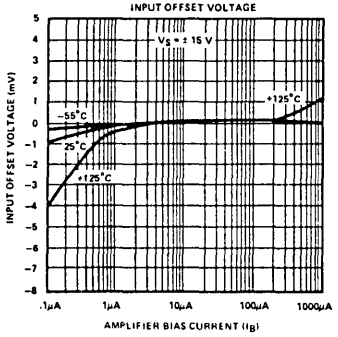
Note 3. Buffer output current should be limited so as to not exceed package dissipation.

Note 4. These specifications apply for V_{CC} = V_{EE} = 15V, T_A = 25°C, amplifier bias current (I_B) = 500 μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

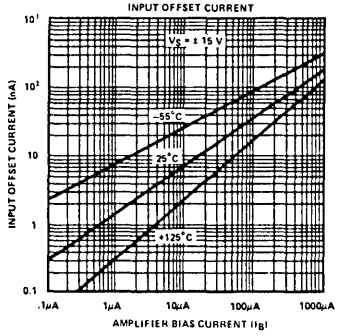
Note 5. These specifications apply for V_{CC} = V_{EE} = 15 V, I_B = 500 μA, R_{OUT} = 5 kΩ connected from the buffer output to $-V_{EE}$ and the input of the buffer is connected to the transconductance amplifier output.

TYPICAL PERFORMANCE CHARACTERISTICS

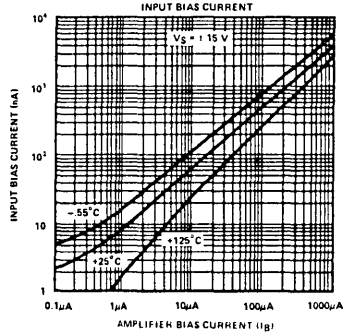
INPUT OFFSET VOLTAGE



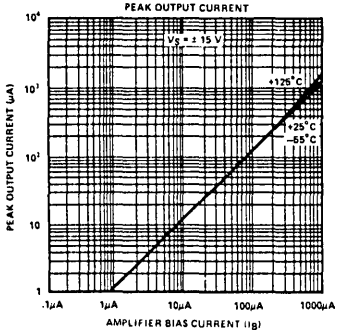
INPUT OFFSET CURRENT



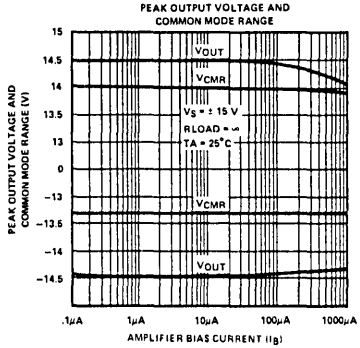
INPUT BIAS CURRENT



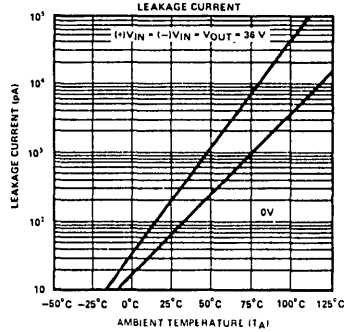
PEAK OUTPUT CURRENT



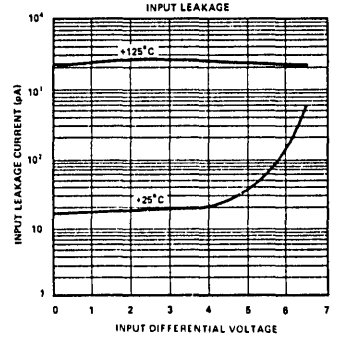
PEAK OUTPUT VOLTAGE AND COMMON MODE RANGE



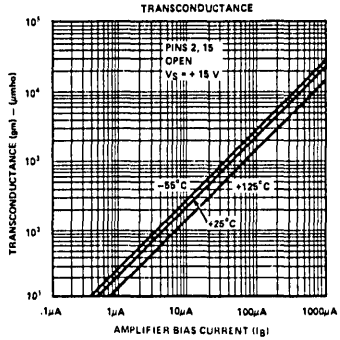
LEAKAGE CURRENT



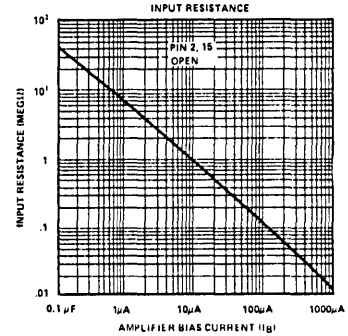
INPUT LEAKAGE



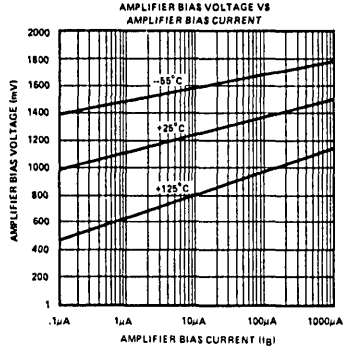
TRANSCONDUCTANCE



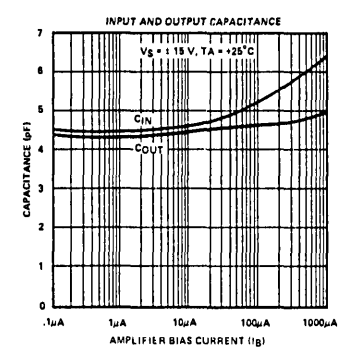
INPUT RESISTANCE



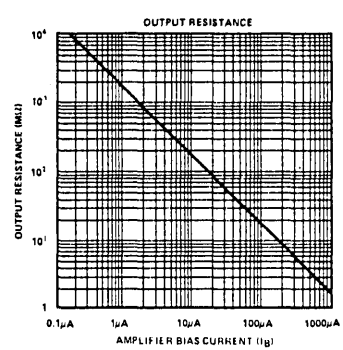
AMPLIFIER BIAS VOLTAGE VS AMPLIFIER BIAS CURRENT



INPUT AND OUTPUT CAPACITANCE

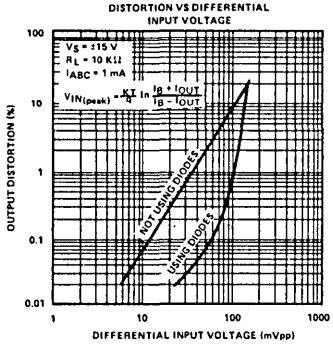


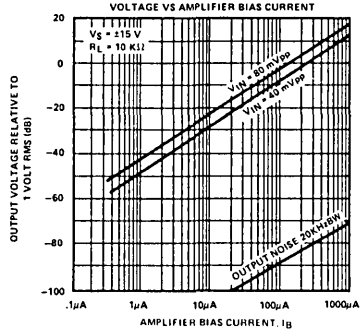
OUTPUT RESISTANCE

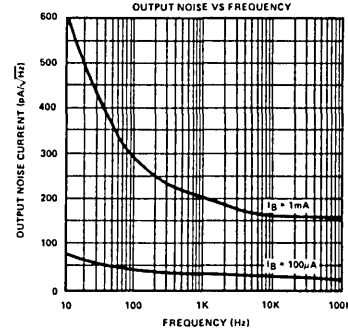


8

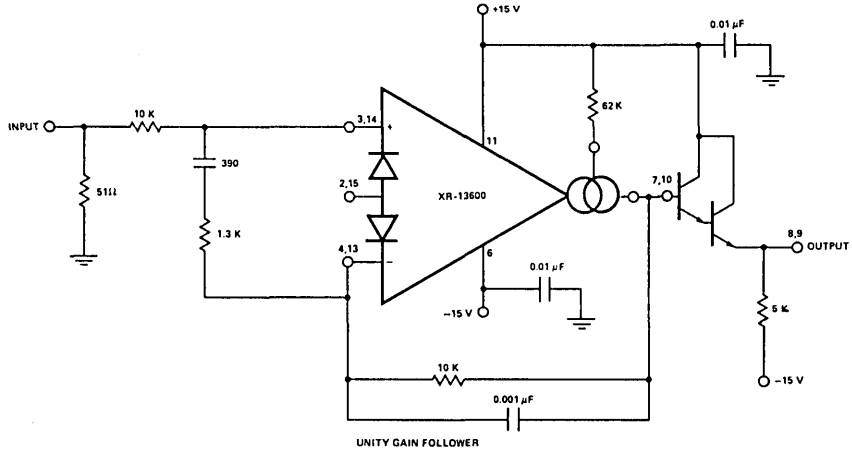
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)







TYPICAL CIRCUIT CONNECTION



CIRCUIT DESCRIPTION

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \qquad (1)$$

where V_{IN} is the differential input voltage, KT/q is approximately 26 mV at 25° C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_B;

$$I_4 + I_5 = I_B \qquad (2)$$

where I_B is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the 1n function can be approximated as:

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \qquad (3)$$

$$I_4 \approx I_5 \approx \frac{I_B}{2}$$

$$V_{IN}\left[\frac{(I_B)(q)}{2KT}\right] = I_5 - I_4 \qquad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN}\left[\frac{(I_B)(q)}{2KT}\right] = I_{OUT} \qquad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_B.

LINEARIZING DIODES

For differential voltages greater than a few millivolts, Equation 3 is no longer accurate, and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is the form of current I_S. Since the sum of I_4 and I_5 is I_B and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_B}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_B}{2} + \frac{I_{OUT}}{2}$$

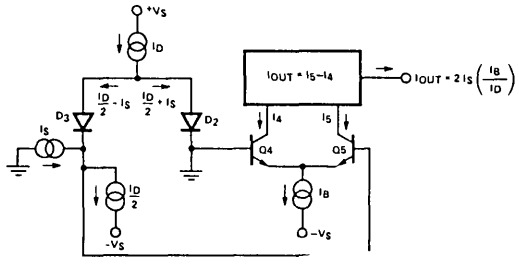


Figure 1. Linearizing Diodes

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{KT}{q} 1n \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} 1n \frac{\frac{I_B}{2} + \frac{I_{out}}{2}}{\frac{I_B}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2I_B}{I_D}\right) \text{ for } |I_S| < \frac{I_D}{2} \qquad (6)$$

Notice that in deriving Equation 6, no approximations have been made and there are no temperature dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

CONTROLLED IMPEDANCE BUFFERS

The upper limit of transconductance is defined by the maximum value of I_B (2 mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_B, a buffer which has very low input bias current is desirable. A FET follower satisfies the low input current requirement, but is some what non-linear for large voltage wing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_B, the buffer's input current is minimal. At higher levels of I_B, transistor Q_3 biases up to Q_{12} with a current proportional to I_B for fast slew rate.

APPLICATIONS

VOLTAGE CONTROLLED AMPLIFIERS (VCA)

Figure 2 shows how the linearizing diodes can be used in a voltage controlled amplifier. To understand the input biasing, it is best to consider the 13 KΩ resistor as a current source and use a Therenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

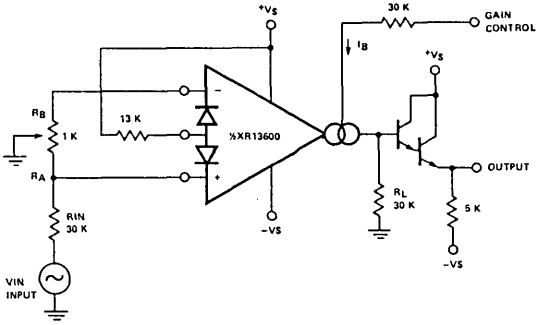


Figure 2. Voltage Controlled Amplifier (VCA) Circuit

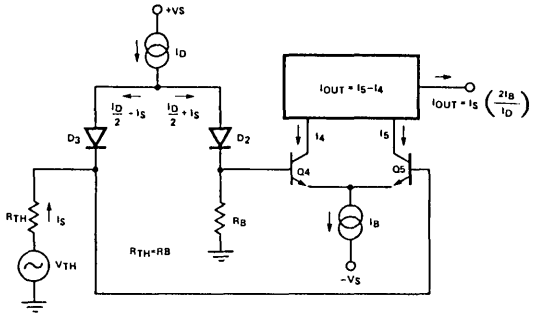


Figure 3. Equivalent VCA Input Circuit

For optimum signal-to-noise performance, I_B should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2) until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

8

XR-13600

STEREO VOLUME CONTROL

The circuit of Figure 4 uses the excellent matching of the two XR-13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. Rp is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived from Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_B \text{ (mA)}$$

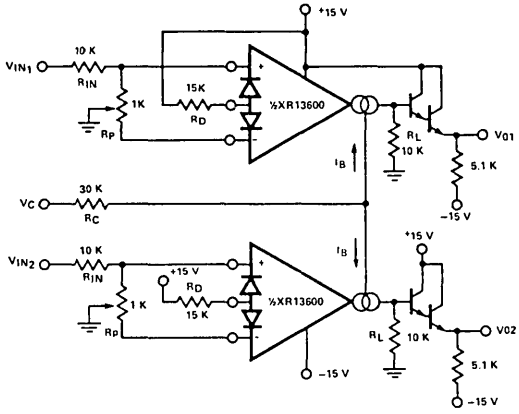


Figure 4. Stereo Volume Control

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D}(I_B) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V = 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C/2(V + 1.4\ V)$ into I_O. The circuit of Figure 6 adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that V_O = OV for V_{IN2} = OV. R_M also serves as the load resistor for I_O.

Noting that the gain of the XR-13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_B, Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

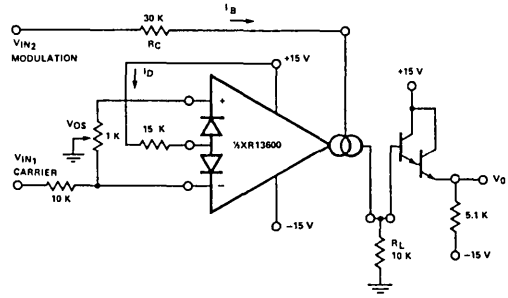


Figure 5. Amplitude Modulator

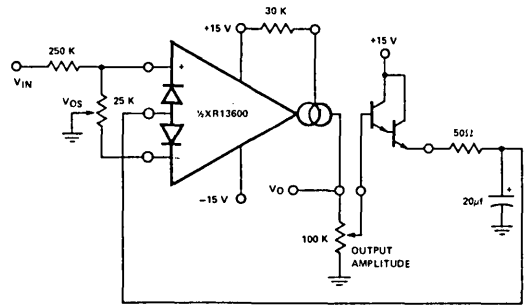


Figure 6. Four-Quadrant Multiplier

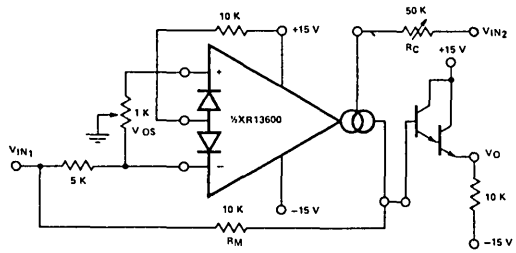


Figure 7. AGC Amplifier

VOLTAGE CONTROLLED RESISTORS (VCR)

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at R_X generates a V_{IN} to the XR-13600 which is then multiplied by the gm of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2\ I_B$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the XR-13600 input.

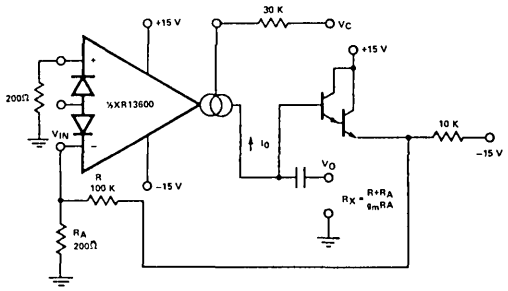


Figure 8. Voltage Controlled Resistor, Single-Ended

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the nose performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the XR-13600.

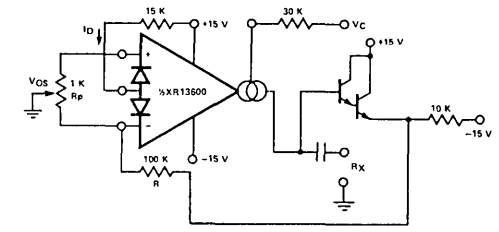


Figure 9. Voltage Controlled Resistor with Linearizing Diodes

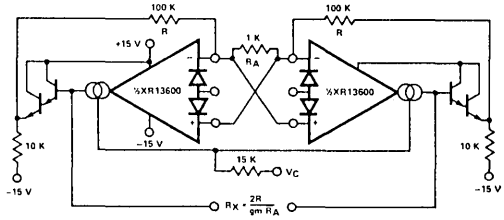


Figure 10. Floating Voltage Controlled Resistor

VOLTAGE CONTROLLED FILTERS

OTA's are extremely useful for implementing voltage controlled filters, with the XR-13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation, where g_m is again 19.2 $\times$ I_B at room temperature.

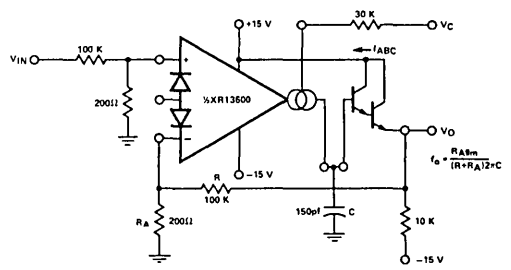


Figure 11. Voltage Controlled Low-Pass Filter

Figure 12 shows a voltage controlled high-pass filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

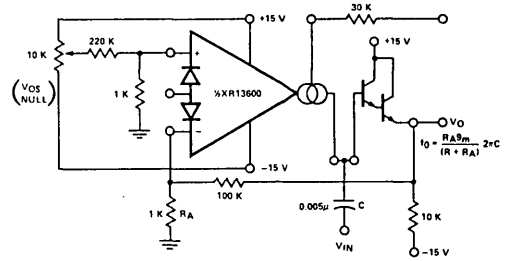


Figure 12. Voltage Controlled High-Pass Filter

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth lowpass filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

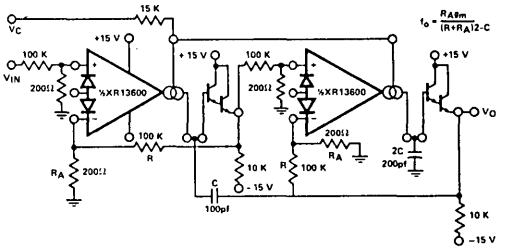


Figure 13. Voltage Controlled 2-Pole Butterworth Low-Pass Filter

VOLTAGE CONTROLLED OSCILLATORS (VCO)

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the XR-13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1mA to 10nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5 volts to prevent zenering the inputs.

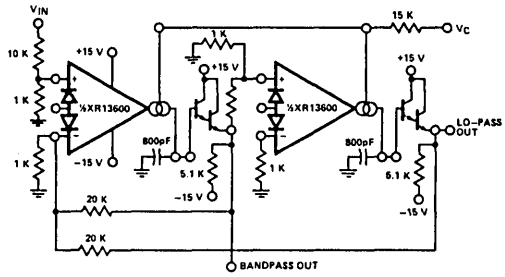


Figure 14. Voltage Controlled State Variable Filter

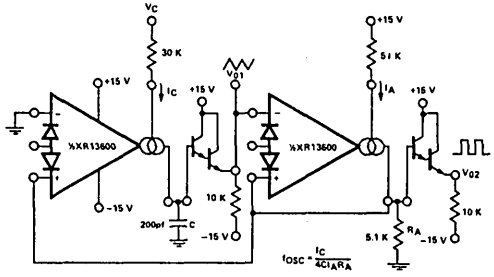


Figure 15. Triangular/Square-Wave VCO

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

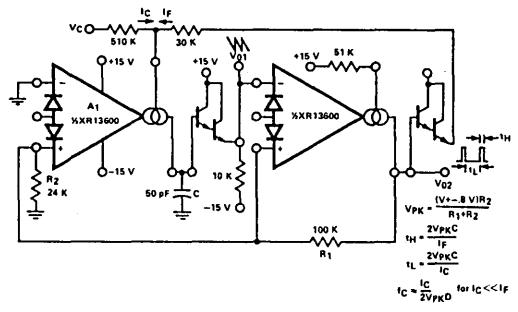


Figure 16. Ramp/Pulse VCO

The voltage-controlled low-pass filter of Figure 11 may be used to design a high-quality sinusoidal VCO. The circuit of Figure 17 employs two XR-13600 packages, with three of the amplifiers configured as low-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

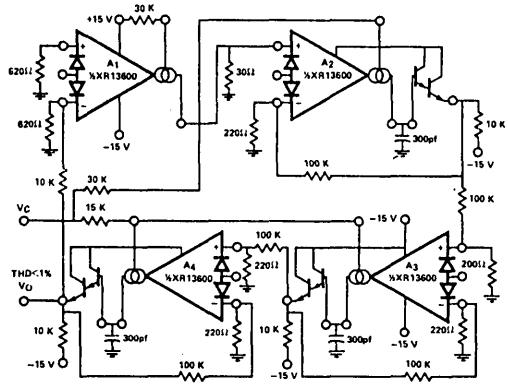


Figure 17. Sinusoidal VCO Using Two XR-13600 Circuits

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

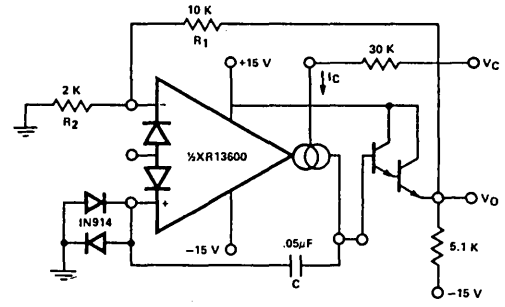


Figure 18. Single Amplifier VCO

ADDITIONAL APPLICATIONS

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches it output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_1 when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

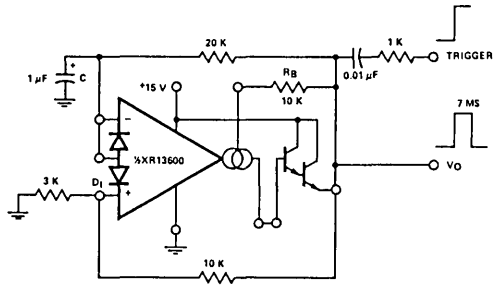


Figure 19. Timer With Zero Stand-By Power

The operation of the multiplexer of Figure 20 is very straight-forward. When A_1 is turned on it holds V_O equal to V_{IN1} and when A_2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A_1 and A_2. The maximum clock rate is limited to about 200 kHz by the XR-13600 slew rate into 150 pF when the ($V_{IN1} - V_{IN2}$) differential is at its maximum allowable value of 5 volts.

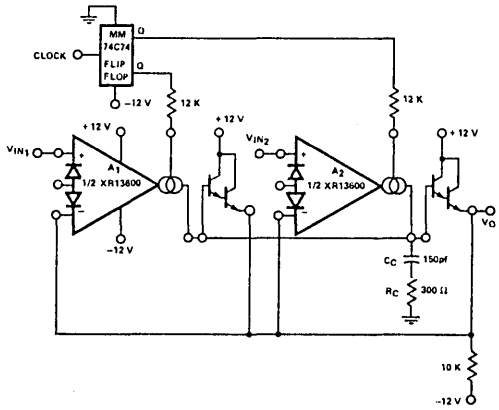


Figure 20. Multiplexer

The phase-locked loop of Figure 21 uses the four-quadrant multiplier of Figure 6 and the VCO of Figure 18 to produce a PLL with a ±5% hold-in range and an input sensitivity of about 300 mV.

The Schmitt trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$ will produce a Schmitt trigger with variable hysteresis.

Figure 23 shows a tachometer or frequency-to-voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H

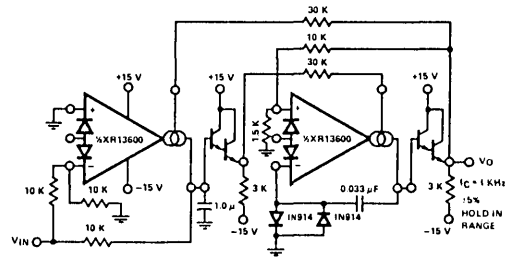


Figure 21. Phase-Locked Loop

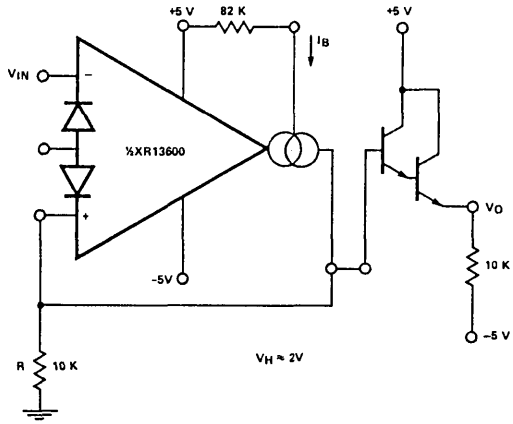


Figure 22. Schmitt Trigger

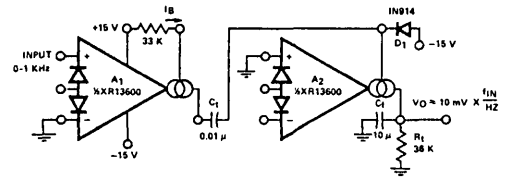


Figure 23. Tachometer

represent the maximum low and maximum high output voltage swing of the XR-13600. D1 added to provide a discharge path for C_t and A_1 switches low.

The sample-hold circuit of Figure 24 also requires that the Darlington buffer used be from the other (A_2) half of the package and that the corresponding amplifier be biased on continuously.

The peak detector of Figure 25 uses A_2 to turn on A_1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A_2 since the A_1 Darlington will be turned on and off with A_1. Pulling the output of A_2 low through D_1 serves to turn off A_1 so that V_O remains constant.

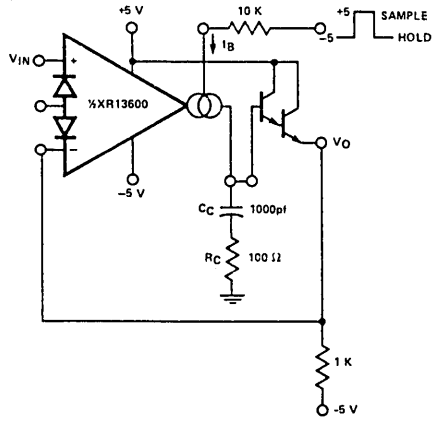


Figure 24. Sample-Hold Circuit

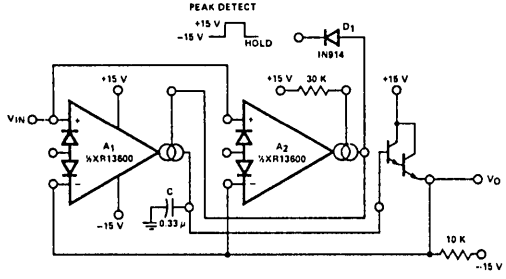


Figure 25. Peak Detector and Hold Circuit

The ramp-and-hold of Figure 26 sources I_B into capacitor C whenever the input to A_1 is brought high, giving a ramp-rate of about IV/ms for the component values shown.

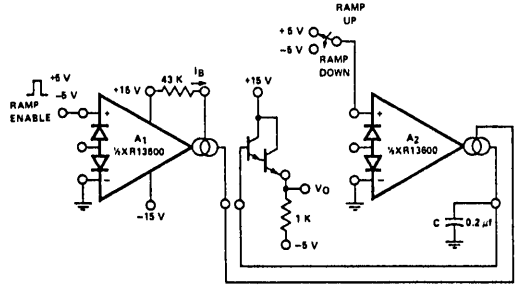


Figure 26. Ramp and Hold Circuit

The true RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A_1 is constant. The output power of amplifier A_1 is monitored by squaring amplifier A_2 and the average compared to a reference voltage with amplifier A_3. The output of A_3 provides bias current to the diodes of A_1 to attenuate the input signal. Because the output power of A_1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A_4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A_4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

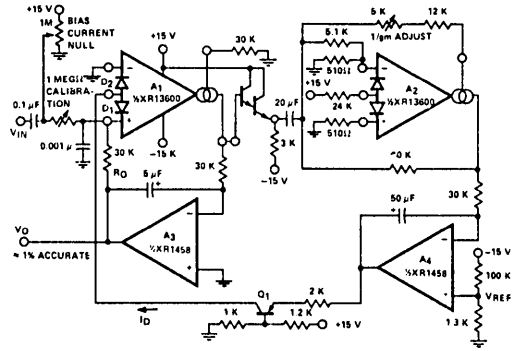


Figure 27. True RMS Converter Circuit

The circuit of Figure 28 is a voltage reference of variable Temperature Coefficient. The 100 KΩ potentiometer adjusts the output voltage which has a positive TC above 1.2 volts, zero TC at about 1.2 volts and negative TC below 1.2 volts. This is accomplished by balancing the TC of the A_2 transfer function against the complementary TC of D_1.

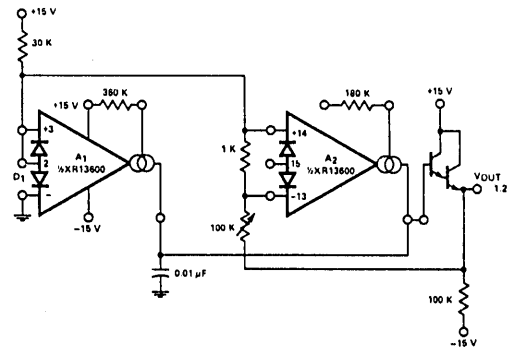


Figure 28. Delta V_{BE} Reference

The log amplifier of Figure 29 responds to the ratio of current thru buffer transistors Q_3 and Q_4. Zero temperature dependence for V_{OUT} is ensured in that the TC of the A_2 transfer function is equal and opposite to the TC of the logging transistors Q_3 and Q_4.

The wide dynamic range of the XR-13600 allows easy control of the output pulse width in the pulse-width modulator of Figure 30.

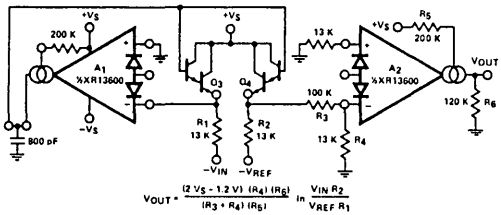


Figure 29. Log Amplifier

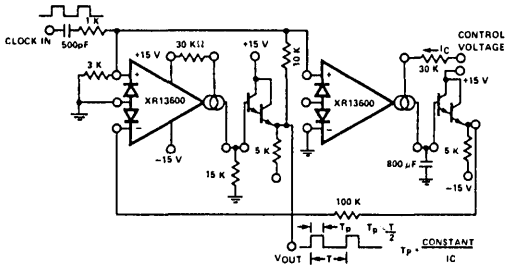


Figure 30. Pulse Width Modulator

For generating I_B over a range of 4 to 6 decades of current, the system of Figure 31 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A_2 is held equal to Oy, the output current of A_1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q_1 and Q_2 is attenuated by the R_1, R_2 network so that A_1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A_1 is:

$$V_{IN1} = \frac{-2KTI_3}{qI_2} = \frac{2KTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1 + R_2)\,V_{IN1}}{R_1}$$

The ratio of the Q1 to Q2 collector currents is defined by:

$$V_{B1} = \frac{KT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{KT}{q} \ln \frac{I_B}{I_1}$$

Combining and solving for I_B yields:

$$I_B = (I_1) \exp\left[\frac{2(R_1 + R_2)\,V_C}{I_2R_1R_C}\right]$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

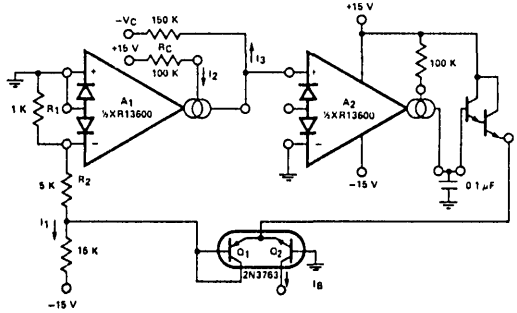
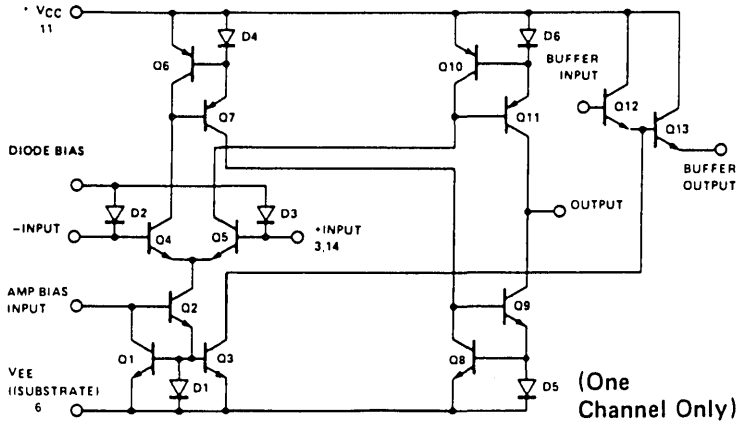


Figure 31. Logarithmic Current Source



EQUIVALENT SCHEMATIC DIAGRAM

EXAR

Section 9 – User Specific Linear ICs – Full Custom/Semi-Custom

SEMI-CUSTOM DESIGN CONCEPT

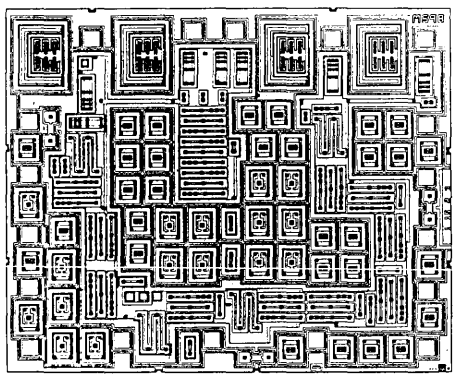
Traditionally, the development of custom IC's has been a long and costly undertaking. The development time would normally run in excess of one year, design changes are slow and costly, and it may take a long time to get from the prototype stage to full production. Because of these difficulties, the use of custom IC's could be economically justified only when a very large quantity of circuits, i.e., several hundred-thousand units, were required during the life of the end product. In the past, these drawbacks have severely limited the use of custom monolithic IC's.

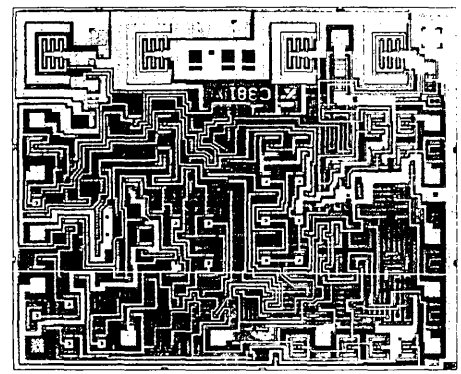
The semi-custom design concept, pioneered by Exar, now overcomes this traditional problem. Exar makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection which metalizes all selected components together in the required circuit configuration. This enables an engineer to design a metal mask based on his circuit which will interconnect the uncommitted components on the prefabricated wafers, and thus convert them into customized chips corresponding to the customer's design. This unique method of IC design and development allows one to develop an almost unlimited variety of custom linear or digital integrated circuits at very substantial cost savings.

The semi-custom program is intended for those customers seeking cost effective methods of reducing component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turnaround time of several weeks, at approximately 10% to 20% of the development costs for tooling associated with the conventional full custom designs. The semi-custom design concept is an interactive or cooperative development effort between Exar and the customer. In most cases, the cost and development time for the program can be reduced even further, if the customer does the design and breadboarding of his own semi-custom IC, using Exar Design Kits, instruction manuals and layout sheets.

The semi-custom design approach is based on a number of standardized IC chips with fixed component locations. These standardized IC chips, called Master-Chips, contain a large number of undedicated active and passive components (i.e., transistors, resistors, logic gates, etc.). These integrated components can be interconnected in thousands of different ways with a customizing interconnection pattern. Each different metal interconnection pattern creates a new custom IC. The figures below show the magnified photograph of a Master-Chip, both in its prefabricated form and after its customization with a special interconnection pattern. This method is called semi-custom rather than full custom, since only the last layer of tooling is changed to customize an IC chip, and rest of the layers are standard. As a result, the development phase is very short, far less expensive and risk free, compared to conventional full or dedicated custom IC's. Similarly, if a design change or iteration is necessary, it can be readily accommodated within a matter of weeks by simply generating a new or modified interconnection pattern.

Exar offers a wide choice of Master-Chips for linear and digital semi-custom design. Presently, Master-Chips are available in linear bipolar, linear compatible I^2L and CMOS technologies. Additional chips are under development for a variety of special applications. The details of each of the presently available chips are discussed in the later section of this book.





Magnified Photograph of a Linear Master-Chip Before and After Customizing

DESIGN KITS

Exar offers three Design Kits: One for linear bipolar, one for I^2L and one for CMOS. Since the general approach to semi-custom design is the same as that for full custom, these design kits are valuable tools for both full custom and semi-custom design work. This is especially true in the case of linear design. Each of these kits contain a comprehensive design manual, a set of semi-custom layout sheets and a P.C. board, IC sockets and other hardware for building your breadboard. The only active components in these kits, that are meant for use in breadboarding, are the transistor arrays found in the linear bipolar and I^2L design kits. The logic blocks found in the I^2L design kit is meant to be used for process evaluation. Digital breadboarding can be done using the appropriate logic family such as 74LXX, 74CXX or 4XXX. The kits are designed so that an engineer, armed only with a background in discrete design, a calculator and a pencil, can design his own customized integrated circuit. The technical material is presented in a straight forward, no-nonsense format with lots of illustrative figures and all of the pertinent equations.

After the circuit is designed, and before it is breadboarded, it is recommended that the customer send Exar a schematic and a circuit description for an engineering evaluation. Normally, there is no charge for such an evaluation. Exar has successfully completed well over 850 custom design programs and our experience can provide valuable guidelines. Exar's Applications Engineering department is ready and able to help our semi-custom design program customers in both the breadboard and layout stage. We can provide immediate answers to your circuit design or testing questions, and speed your custom design on its way.

YOUR FIRST STEP

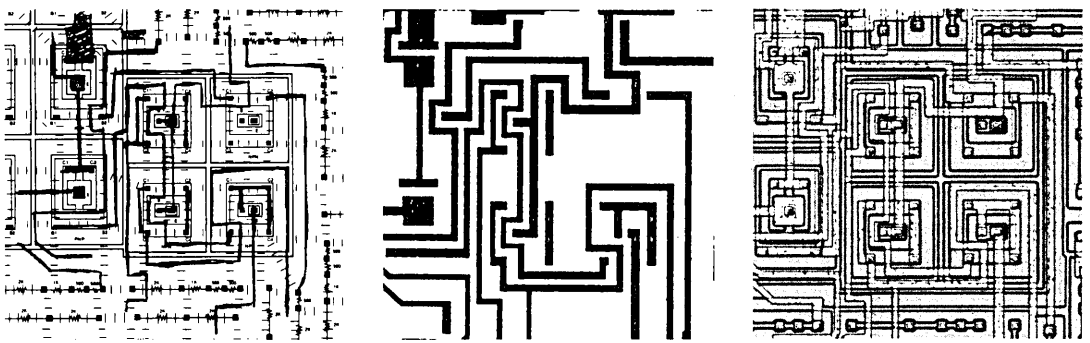
Your very first step, at the start of a semi-custom program, should be to contact Exar for a preliminary analysis and discussion of your needs. This can be done even while the program is still at the thought stage. This initial review by Exar is performed at no cost to the customer and is essential to the success of the program. It avoids any possible design pitfalls or misunderstandings. This early interaction also allows you to find out some of the options or variations available in Exar's semi-custom programs and choose the one which is best suited to your needs.

The following is required by Exar's technical staff to provide you with an accurate feasibility study of your project. and a budgetary estimate of the development costs, timetables and production pricing.

- A block diagram of circuit function and input/output interface requirements.
- A circuit schematic or logic diagram of your circuit.
- Preliminary or objective performance specifications and limits on critical circuit parameters (also possible tradeoffs which may be allowed).
- Test specifications
- Packaging requirements.
- Production quantity requirements.
- Desired development and production timetables.
- An indication of how much of the breadboarding, layout, etc., can be done by you, the customer, using Exar's Design Kits or standard logic blocks (74LXX, 74CXX or 4XXX).

Once the above data package is submitted to Exar, we would review it and respond to you within a few days.

Normally, the test system development effort is initiated in parallel with chip development. Exar has a complete computer controlled IC test facility and offers complete IC testing capability for production units.



Steps of Semi-Custom Design

FREQUENTLY ASKED QUESTIONS AND THEIR ANSWERS

Based on our long experience with Exar's semi-custom Master-Chips, we have compiled a comprehensive glossary of the most often asked questions concerning the program. The following is a list of these questions and their answers.

WHAT IS THE COST OF THE BASIC PROGRAM?

The cost of the semi-custom development program depends on how much of the design and layout is done by the customer. In general, the basic semi-custom program is where the customer does the design, breadboard evaluation and pencil layout on the Master-Chip worksheet; and Exar does only the IC tooling and prototype fabrication. This is the most economical and cost effective approach.

For bipolar semi-custom designs, the development cost of the basic program is in the range of $2,000 to $8,000, starting with an accurate layout supplied by the customer. The above prices also include the cost of 50 monolithic prototypes delivered at the completion of the program. Additional prototypes are available at a nominal cost, in minimum lots of 200 units.

In the case of I^2L or CMOS semi-custom designs, the basic development program costs are in the range of $4,200 to $8,500, depending on the layout complexity and the particular Master-Chip used. This development cost also includes 25 monolithic prototypes. Additional prototypes are available at a nominal cost, in minimum lots of 200 units each.

WHAT IS THE DEVELOPMENT TIME?

Typical development time for the basic bipolar semi-custom program is four to six weeks, starting with the customer's pencil layout and ending with the monolithic prototypes. If Exar is required to do the IC layout or breadboard evaluation, several additional weeks may be required to complete the development program.

In the case of I^2L or CMOS semi-custom development programs, the typical development time is eight to ten weeks, starting with the pencil layout of the Master-Chip worksheet. The I^2L semi-custom program takes slightly longer than bipolar or CMOS because it requires three layers of custom tooling, rather than one, to customize a prefabricated Master-Chip.

WHAT IF ADDITIONAL DESIGN CYCLES ARE NEEDED?

If the customer desires to modify the design or layout after evaluation of the initial prototypes, a new design iteration cycle can be completed within five weeks for the bipolar and CMOS designs, and within eight to ten weeks for the I^2L designs. Cost for this iteration is dependent on the complexity of modification.

WHAT ABOUT PRODUCTION PRICING?

The production pricing of monolithic IC's depends upon a number of important factors such as:

a) Master-Chip type.

b) Circuit complexity (i.e., yield).

c) Device performance and test requirements.

d) Special environmental screening requirements (burn-in, hermeticity tests, etc.).

e) Package type required.

In the case of a custom IC, it is impossible to anticipate the impact of these factors without detailed knowledge about the circuit and its application. Each custom IC, by definition, has some unique requirement or feature associated with it. After reviewing your specific needs, particularly with regard to the circuit performance and quality requirements, Exar can provide you with a detailed proposal outlining the development costs and production pricing for your particular circuit.

WHAT ABOUT THE TESTING OF SEMI-CUSTOM IC's?

Exar will develop test software and fixtures to provide fully tested production IC's. All production devices receive 100% electrical test and screening to a mutually agreed upon device specification. In addition to the complete electrical testing, all of the production devices are screened by Exar's Quality Assurance department to assure compliance with the agreed upon Acceptable Quality Level (AQL) standards.

Exar can perform two basic types of tests for production IC's: (1) parametric testing which measures a specific parameter value (normally current or voltage) and compares it against pre-established limits; (2) functional testing which applies a series of operating conditions and compares the circuit under test with a known good device. These two types of tests can be performed both as steady state (dc) or dynamic (ac) measurements.

ECONOMICS OF SEMI-CUSTOM DESIGN

In developing either linear or digital custom circuits, one is always confronted with the following key question: for a given product type and production requirement, is it cheaper to develop a semi-custom or full custom IC? Since the functional requirements of each custom IC program vary greatly, there is no general answer to the above question. However, based on Exar's long experience in both full and semi-custom IC design and depending on the overall production requirements, it is possible to establish some sound economic guidelines for choosing the most cost effective approach.

COST FACTORS INVOLVED

Any custom IC development, whether full or semi-custom, involves similar types of cost factors. These are:

1. Non recurring engineering (NRE) or development costs.

2. Cost or unit price of the product in production quantities.

In the case of monolithic IC's, particularly those which have relatively limited production volume, the development costs may be a significant factor in the cost of the end product. Therefore, when discussing the economics of custom IC's for medium to low production quantities, it is best to consider the cost tradeoffs in terms of the amortized unit price of the IC at a given production volume. This amortized unit price is defined as the actual cost of each unit including its share of the development cost. As an example, a full custom IC may cost $50,000 to develop and may be priced at $2.90 each at a 50,000 piece total production level. Then, its true amortized unit price including development costs will be $2.90 plus $1.00, or $3.90. Similarly, an equivalent semi-custom IC may cost $5,000 to develop and be priced at $3.20 each, at the same 50,000 production level. Then, its amortized per unit price will be $3.30, or approximately 20% cheaper than a full custom.

The figure below gives a comparative graph of the amortized unit price for a typical full custom design, along with the equivalent in semi-custom form for various production quantities. For comparison purposes, the relative ratio of the amortized unit price is plotted along the vertical axis. If this ratio is greater than 1.0 then the semi-custom method is the more cost effective solution.

NO TWO IC's ARE THE SAME

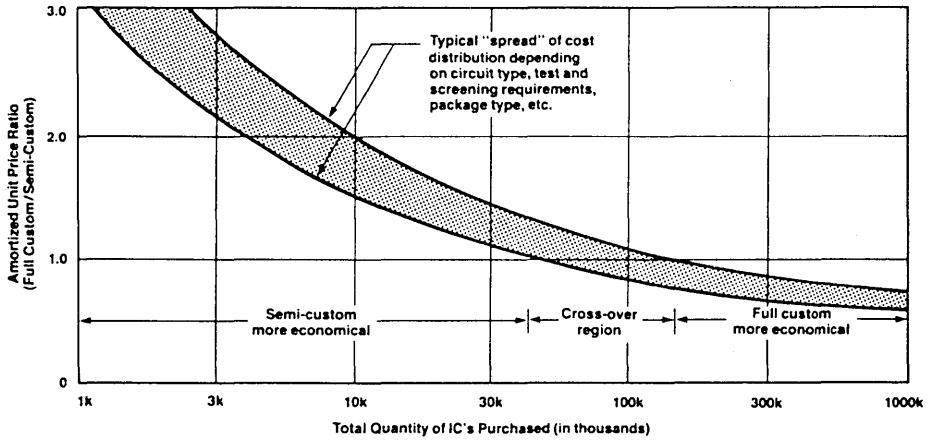
By definition, each custom IC type is unique. Therefore, the cost comparison curve given below is shown as a spread rather than a single line. This is because, in addition to the production quantity, the cost of monolithic IC's also depends on the circuit complexity, special test requirements and the IC package type.

The key information contained in the relative cost vs. quantity figure can be summarized as follows:

1. For a total production requirement of 50,000 pieces or less, the semi-custom approach is definitely the most economical.

2. For a production requirement of 200,000 pieces or more, the full custom design is more cost effective.

3. For production quantity requirements in the 50,000 to 200,000 piece range, the crossover point for the most economical approach will depend strongly on the specifics of a particular IC function; i.e., its special test, environmental screening, and package requirements.



TYPICAL COST VS QUANTITY COMPARISON OF FULL CUSTOM AND SEMI-CUSTOM DESIGNS

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

Exar can offer you the combined advantages of semi-custom and full custom design programs. This is because Exar has a complete semiconductor manufacturing facilities. This unique capability allows Exar to state a custom development program using a combination of semi-custom Master-Chips during the initial phases of a customer's product, taking full advantage of the low tooling cost and short development cycle. As the product matures and its market expands (resulting in higher volume production run rates) Exar can convert the multiple semi-custom chip approach into a single custom IC, thus achieving a cost reduction and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced. The IC design approach has been proven, production "bugs" are out of the product and your production line continues to flow during the full custom chip development. Once the custom chip is completely characterized and found acceptable, the semi-custom IC system in your product can be phased out while the full custom IC is being phased in.

SEMI- AND FULL CUSTOM COMBINATION: THE TWO-STEP DEVELOPMENT

In many custom development programs one is faced with very short development times and a rapid transfer into high volume production. Such a requirement does not leave room for lengthy development and design change or iteration cycles associated with conventional full custom IC design.

Exar combines full and semi-custom design capabilities, and a complete wafer fabrication facility under one roof, therefore, providing a unique solution to this problem; initially developing the prototypes in a semi-custom form, and then converting them to full custom.

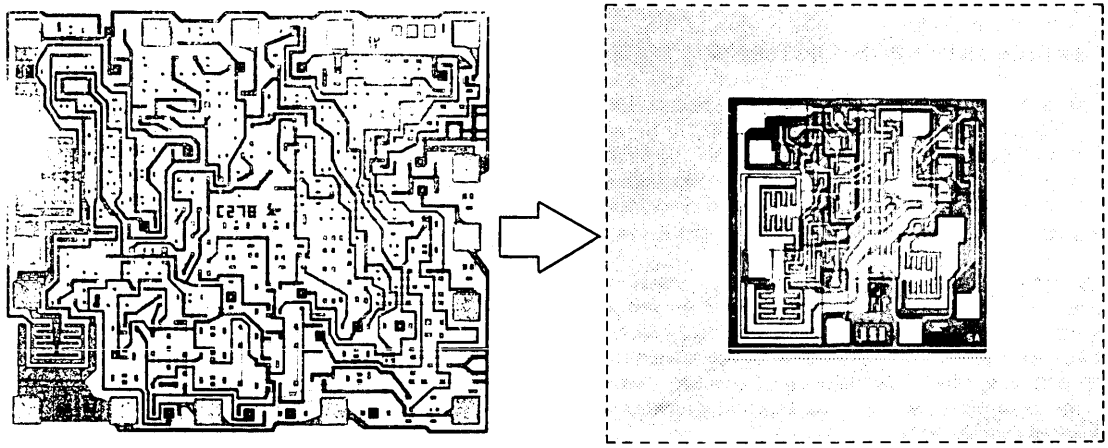
In this manner, the customer has the best of both worlds with the combination of these two technologies. The quick turnaround advantage of semi-custom Master-Chips provide prototypes and initial production units, while the subsequent full custom design provides cost savings at high volume production. During this transition, the customer is assured of a continuous flow of product through its production line.

In such a two-step development, the semi-custom prototypes often serve as a monolithic breadboard to optimize and debug the final design. This allows design iterations or changes to be made quickly and inexpensively. In fact, the only difference between the semi-custom and full custom chip is the actual size of the silicon chip.

Once the design is satisfactory, conversion of a semi-custom to a full custom chip is very straight forward and relatively risk free. We simply remove the unused electrical components from the chip to reduce the chip size and pass the resulting cost savings on to you in the form of a reduced unit price.

The two-step development capability; i.e., start as semi-custom and finish as full custom, is a very powerful design technique. It avoids the risks associated with a conventional black box type of custom design where one does not know until the very last day of development whether the circuit works or if it can be manufactured.

The two-step program is faster and less expensive than the conventional full custom development, since it avoids costly and lengthy design iteration or modification cycles for a full custom IC. In addition, it gives the customer a very high degree of assurance that the final full custom unit will work the first time.



SEMI-CUSTOM DESIGN AND ITS FULL CUSTOM EQUIVALENT

ADVANTAGES OF SEMICUSTOM DESIGN

Significant lower costs	Hybrids and discretes are quite expensive as compared to semicustom ICs. Less inventory cost also.
Higher reliability	Than hybrids and discretes. Because one semicustom IC replaces many components.
Quick turnaround	Semicustom protos are delivered in less than seven (7) weeks.
Lower development cost	Less than half the full custom cost.
Iterations	Are quick and less expensive than full custom because only one mask needs to be changed.
Reduced real estate & power	Because one IC is replacing many components. Therefore, your PC board may shrink 60-80%. Consequently, less power too.
Quick production ramp up	Need 200,000 units in less than 12 weeks? Exar can deliver using its semicustom **Master-Chip®** approach.
Product security	Semicustom IC is specifically designed for you; it is not available to your competitors as an off-the-shelf ITEM.
Reduced power, inventory cost, and production cost	Because one custom IC replaces many discrete components.

FULL CUSTOM DEVELOPMENT

Exar offers a complete design and production capability for full custom IC development. This provides an excellent complement to Exar's unique semi-custom capability. Exar's full custom IC development and production capabilities offer complete flexibility to meet changing customer needs or design problems. We can develop a complete custom IC starting from your black box specifications, or reduce your working breadboard prototype to a monolithic chip. Alternately, if you have the facilities and resources to do the IC design and layout, Exar will provide you with the device characteristics and IC layout rules for the particular process suitable to your design and review your IC layout for you. Then, Exar can generate the IC tooling and fabricate your IC prototypes.

YOUR FIRST STEP FOR FULL CUSTOM DESIGN

The following technical data package is required in order for Exar to provide you with a quotation for your full custom development program:

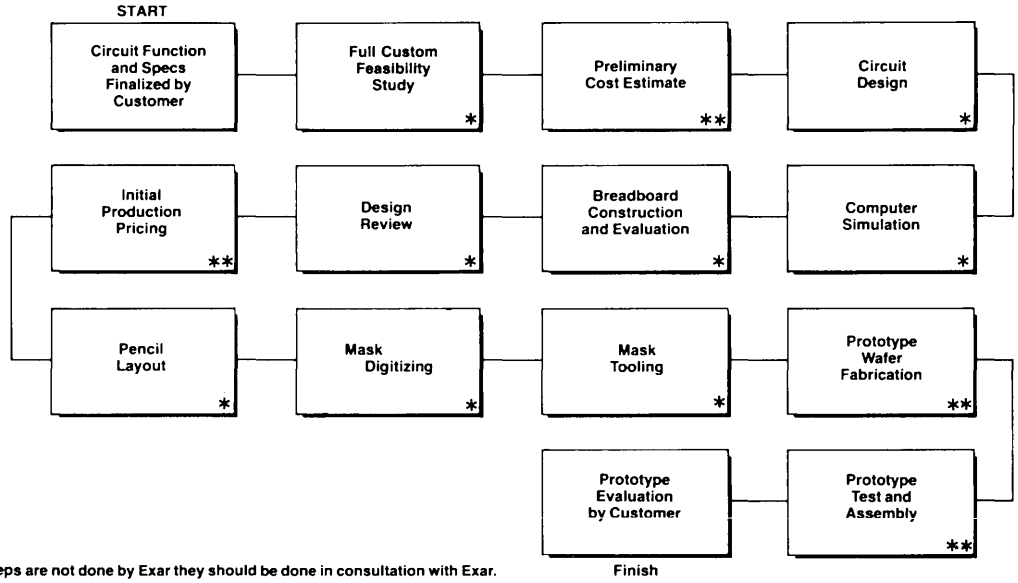
1. Circuit block diagram with subblocks.
2. Circuit schematic or logic diagram.
3. Description of circuit operation and pertinent application information.
4. Preliminary or objective device specification indicating min/max conditions and limits for the critical parameters; i.e., input/output voltage and current levels, operating frequency, timing diagrams, input/output impedances, power dissipation, etc.
5. Production requirements and the desired development timetable.
6. Packaging requirements.
7. Level of screening required.

IC FABRICATION FROM CUSTOMER'S TOOLING

Exar has a complete in-house silicon wafer fabrication and processing line at its main manufacturing plant in Sunnyvale, California. This facility currently runs 3-inch silicon wafers and will soon add 4-inch capability, and is also available for manufacturing custom IC's directly from a set of customer supplied IC tooling, in coordination with Exar's Mask Design department.

If you have a set of IC tooling (masks and composite overlays) or are contemplating having one designed for you, Exar's technical staff will be glad to review it for you to assure compatibility with Exar's technology and layout tolerances. Our wafer processing technology and capabilities are compatible with the industry standards, and with the technologies of other leading IC manufacturers.

For additional information on Exar's wafer fabrication services, contact Exar directly. We pride ourselves in our flexibility and quick response to your needs.



*If these steps are not done by Exar they should be done in consultation with Exar.

**These steps must be done by Exar.

FLOW CHART OF TYPICAL FULL CUSTOM DEVELOPMENT

TESTING OF SEMI-CUSTOM IC's

All production units of semi-custom IC's are 100% electrically tested and screened to test specifications which have been mutually agreed upon between Exar and the customer, using one of Exar's several computerized test systems. In addition, Exar's Quality Assurance department performs an independent set of electrical tests on randomly selected samples of production units, prior to shipment, to assure conformity with Exar's Acceptable Quality Level (AQL) standards.

EXAR's TEST CAPABILITIES

Exar can perform two basic types of tests for production IC's: (1) parametric testing which measures a specific parameter value (normally current or voltage) and compares it against pre-established limits; (2) functional testing which applies a series of operating conditions and compares the circuit under test with a known good device. These two types of tests can be performed both as steady state (dc) or dynamic (ac) measurements.

Exar provides 100% electrical testing of IC chips in wafer form, using automated wafer probe stations, and in packaged form, using automatic handlers. Exar's test facility currently has fifteen independent computer controlled test systems, with more being added as we grow. Exar's automated test system compliment is comprised of:

- Teradyne A311
- Teradyne A312
- Teradyne A360
- Teradyne J273
- Fairchild 5000C

Testing is one of the most critical steps in IC production. Therefore, to insure efficient and cost effective testing of production IC's, it is essential that a preliminary test plan be prepared jointly between the customer and Exar at an early stage of the custom development. This preliminary test plan will lead to the final detailed test specifications, once the development prototypes are fully evaluated and characterized and the circuit is ready to release to production.

TEST INTERFACE DEVELOPMENT

The performance and characterization data derived from careful prototype evaluation is the basis upon which test hardware and software is developed. Exar and the customer will jointly determine the performance expectations to be placed on this new IC, and once these specifications are agreed upon, Exar will proceed with test development.

Test development involves the design and construction of a test interface circuit, probe card and automatic handler hardware as well as writing the software which allows Exar's test system to perform the desired electrical tests. All these elements are then brought together under actual production conditions for evaluation and system debugging. This process can take from four to six weeks to complete, depending on the sophistication and complexity of the test plan under development. Test development begins concurrently with the start of production wafers (which require approximately 6 weeks to process).

SPECIFICATION AGREEMENT LETTER

With each new custom IC Exar issues a Specification Agreement Letter. This specification states precisely the test conditions, performance levels and environmental requirements which each production IC must meet before it can leave our factory, and is the document upon which acceptability of the IC is judged. It is issued in duplicate and signed by responsible representatives from both companies prior to beginning production. One copy is retained by the customer, the other is returned to Exar.

If, for some reason, changes in the IC's specification are required, a new Specification Agreement Letter will be issued by Exar reflecting these changes. No change, however, will be put into effect until both companies have signed the new agreement. This document will then supercede all prior agreements and remain in effect until both firms, again agree, a change is required.

LINEAR SEMI-CUSTOM DESIGN

COMPONENT UTILIZATION

The total number of components on the Exar Linear Master-Chips range from 110 on the XR-C100A to 882 on the XR-W100. However, the number of these components that are actually usable depends upon many considerations. The first thing that must be evaluated is the general requirements of the finished circuit. Factors such as the number of pins that are required, breakdown voltage as well as die size limitation imposed by packaging requirements, determine which of the Master-Chips are suitable. This can impose limitations on the number of available components.

Circuit characteristics also impose limitations upon the number of usable components. For example, a circuit whose package pin configuration can be chosen freely, that handles small signals, low supply voltages, is insensitive to dc offset voltages, and whose various circuit blocks follow one another with a minimum of interconnections between blocks, may be able to use over 90% of the components on the selected Master-Chip.

On the other hand, in more complex designs requiring special layout or design considerations, the component utilization may be as low as 50%. Examples of such cases are those where the package pin-outs are predetermined, or the choice of component locations on the die may be fixed due to thermal consideration, circuitry symmetry or offset requirements. In certain cases the series or parallel connection of several resistors to obtain a predetermined value, or paralleling several transistors to increase their current handling capability, may also limit the total component utilization.

Over 850 custom programs have been completed to date, using Exar's bipolar Master-chips. Thus, Exar's Engineering department has a great wealth of experience concerning the layout techniques utilizing the Master-Chips. In many cases, it is advantageous for the customer to call Exar for a free consultation regarding the choice of a particular Master-Chip which may be best suited for his application.

The bipolar Master-Chips are laid out to provide easy routing of metal interconnection paths. In addition, a multiplicity of low resistance crossunders are provided on the chip to simplify the interconnection layout.

LINEAR MASTER DESIGN KIT

A Linear Master Design KIT, containing a wealth of IC design and layout knowledge, is available from Exar for $59.00. This design KIT shows a step-by-step approach to convert your existing discrete linear circuits into a CUSTOM IC.

This design manual explains in detail the Bipolar Technologies employed. Component characteristics are clearly detailed to assist you during your paper design. In addition to circuit design and layout examples this KIT includes Testing, Quality Assurance and Packaging information.

Also included in the Master Design KIT are breadboarding components (KIT parts). These KIT parts come from the same Bipolar Process (20V, 36V, 75V) that will be used to integrate your circuit, thus minimizing any unforeseen processing risks.

The KIT parts included in the Master Design KIT are for your preliminary survey. After you have selected a particular Master-Chip for your design, then appropriate KIT parts will be mailed to you upon receipt of your order.

TECHNICAL ASSISTANCE

If any special or unusual circuit design or layout problems are encountered in the preparation of your semi-custom IC layout, Exar's technical staff will be glad to review your design problem and provide technical guidance. In many cases, it is beneficial to call Exar for a preliminary discussion of your custom IC needs even before you decide to buy a design kit.

BREADBOARDING

After a circuit has been designed and analyzed on paper, it is time to reduce the theoretical design to a functioning circuit that will duplicate, as closely as possible, the operation of the finished integrated circuit. This is the purpose of breadboarding. A great deal of care needs to be taken during this phase of IC development. Accurate breadboarding will not only allow you to gain an accurate assessment of the performance you can expect from the finished IC, but it will also allow you to discover circuit design flaws. A correctly connected, nonfunctional breadboard is a very vivid indication that something has been overlooked. Changes can be made

on a breadboard in a couple of minutes with a pair of pliers and a hot soldering iron. Changes on an IC are much more expensive and time consuming. The breadboard can be tested over temperature in a temperature chamber and circuit performance can be measured with worst case resistor values. Preliminary test specifications can also be readily developed from a properly functioning breadboard. Next to the initial paper design, breadboarding is the most important step in IC development.

KIT PARTS

Since the purpose of breadboarding is to build a circuit that will duplicate, as closely as possible, the performance of the finished IC, Exar has included with this design kit a generous supply of kit parts. These kit parts are the same integrated components that you will find on the finished IC. They are metalized and brought out individually so that you can use them to connect your circuit.

Generally speaking, the integrated resistor arrays need only be used in circuits where certain characteristics of these resistors, such as high frequency response or temperature coefficients, are critical to circuit performance. In most cases, standard off-the-shelf carbon film resistors are entirely adequate for breadboarding.

LINEAR SEMI-CUSTOM DESIGN CYCLE: SIX SIMPLE STEPS

The basic linear semi-custom design program involves only *6 single steps*, from the beginning of circuit design to the completion of monolithic prototypes. The first four of these steps can be done by either the customer in consultation with Exar or by Exar. The last two are performed by Exar.

Step 1	
Circuit design and breadboard using Linear Design Kit.	Customer purchases Exar's Linear IC Design Kit, made up of a comprehensive Design Manual and monolithic kit parts. The circuit is designed, breadboarded and its performance evaluated using these kit parts. The electrical characteristics of the kit parts Are virtually identical to the component which will be on the finished IC chip. Thus, this step provides a true simulation of the final IC performance.
Step 2	
Circuit layout is prepared	After the completion of breadboard evaluation, a layout of the circuit on the selected Master Chip by following the basic layout rules given in the Design Manual. The layout is done simply by interconnecting appropriate device terminals with pen or pencil lines on oversize drawings of the Master Chips supplied with the kit.
Step 3	
Layout review	Exar reviews the circuit layout and schematic to check the following: a) That basic circuit function is feasible b) No layout rules are violated c) Circuit layout accurately represents the circuit schematic. *NOTE: Exar offers consulting service and design advice during these first three steps.*
Step 4	
Exar generates custom interconnection pattern.	Using the completed Master-Chip layout sheet, Exar generates a custom interconnection pattern, or metal mask to be applied to pre-fabricated Master-Chip wafers.
Step 5	
Exar fabricates customized IC wafers.	Exar applies the custom interconnection patterns to pre-fabricated Master-Chip wafers. During this customization process, the hardware and software necessary to test the prototypes is made ready. After the wafers are customized, each die is tested by an automatic tester.
Step 6	
Exar assembles and delivers monolithic prototypes.	The customized IC wafers are scribed or cut into individual IC chips. After a visual inspection, several die that tested "good" are assembled in cerdip packages. These packaged devices are then tested again before shipment. Fifty assembled IC's, and test data for correlation purposes, are sent to the customer in a prototype package that includes a die photo, device schematic test details and a layout sheet.

▶ FULL CUSTOM DESIGNS

EXAR offers direct full custom designs to its customers. However, recognizing the risks, costs, and longer turnaround times involved in full custom development, EXAR also provides full custom conversions.

Full custom conversion is a two-step approach that provides the best of both worlds; quick turnaround time with minimum risk of semi-custom arrays, and the efficient use of silicon with full custom which invariably means reduced unit costs.

The first step is to implement customer's design on one of EXAR's **Master-Chips** to take advantage of the fast integration times as well as very easy, fast and low risk design iteration cycle in comparison to full custom. This enables customers to design and penetrate their product into the market in a short time frame and qualify the product for production rapidly. In addition, any application or production problems that may require design iterations can be implemented at a low cost and with a fast turn-around time. This way, all production oriented problems are fully debugged and the device is production proven in semi-custom form.

The second step, then, would consist of a straightforward full custom conversion to minimize the chip size and hence the unit cost when the device is in full production. This ensures a risk free and a very smooth transition to shipping cost effective, high volume products.

▶ STANDARD CELL LIBRARY

EXAR has developed an extensive library of fully characterized linear standard cells, and is in the process of expanding the library continuously. EXAR presently has over 100 different, fully characterized linear standard cells.

Linear standard cell technique allows customers to design an entire integrated circuit from base layer up, similar to a full custom development without suffering from some of its disadvantages. Please contact EXAR for further information on its Standard Cell Library.

Again, EXAR's state-of-the-art in-house wafer fabrication facility is a key factor in providing highly reliable full custom and standard cell products.

▶ DESIGN MANUALS AND KIT PARTS

A Linear Master-Chip Design Manual is available from EXAR for $59. This manual shows a step-by-step approach to the design and layout of circuits. It covers one of the most comprehensive and useful analog circuit design aids in the industry, including extensive device characterization, modelling, predesigned circuit examples and circuit building blocks as well as layout examples. Also contained in this manual are breadboard kit parts which will be used to prove the performance of your circuit. These kit parts come from the same bipolar process that will be used to integrate your circuit. Additional kit parts are available at $2.50 each.

▶ THREE STEPS TO SUCCESS

Get EXAR To Work For You

Step 1: Discuss Your Needs With EXAR

We are proud of our quick and flexible response to your needs. During the conception stage of your project, our highly talented Design Engineers can go through the technical options and variations available to you through EXAR. This is done at absolutely no cost to you.

Step 2: Get a Quotation From EXAR

To help us get an accurate and complete quotation to you faster, your request for quotation (RFQ) should contain:

☐ A block diagram of your application
☐ A schematic at discrete or transistor level
☐ The circuit specifications
☐ Your volume requirements

The more information you supply us, the sooner we can respond. EXAR can also assist you in compiling this information.

Step 3: Relax and Enjoy The Services Offered by EXAR

Depending on your requirements, a project may be started with EXAR at YOUR desired level of involvement. EXAR engineering having successfully completed over 1000 user specific projects (automotive, industrial control, telecom, modems, computer peripherals, medical and switch capacitor filter applications), has the necessary expertise to be involved in system design, IC design, layout or integration level. YOUR CHOICE. In either case, throughout the development process, a close contact is maintained between EXAR and your staff. NO SURPRISES.

In addition to our extensive engineering expertise in various user specific applications, as a standard IC manufacturer, EXAR brings years of accumulated engineering know-how and expertise in telecommunications, computer peripherals, data communications, including switch capacitor filters and modems, industrial control, and instrumentation to our customers. All this design expertise is available to you. Make use of our easily acessible wealth of valuable engineering resources now.

EXAR also offers a variety of DIGITAL GATE-arrays. These include state-of-the-art dual metal 3μ Si-GATE arrays for high speed applications and metal gate CMOS arrays for high voltage applications.

▶ SERVICES OFFERED

Depending on the annual volume requirements of the customer and the selectivity criteria, EXAR offers a wide variety of Engineering services. These services are briefly outlined below:

1. System Design: This type of design service evolves from the conceptual system description and specification. It requires EXAR to come up with the system design using a block diagram approach. It requires definition of the functional blocks and system implementation with discrete IC blocks to verify the performance, as per the objective specs. Discrete IC implementation of each functional block and determination of the product or circuit specifications required to meet the system performance concludes the System Design.

2. Circuit Design: In this type of service, the system is well-defined by the customer in block diagrams and at the discrete IC level. EXAR determines the partitioning of the system and the definition of the product and objective specs. Then the transistor level design of the circuit is implemented to meet the IC specs. For circuit simulation, EXAR's **Master-Chip** models with SPICE/ASPEC programs are also available.

The circuit is breadboarded using the kit parts of the appropriate **Master-Chip**. A fully evaluated and finalized breadboard is submitted to the customer together with the evaluation results and performance characteristics for approval.

3. Design Assistance: This service is intended as a joint effort between EXAR and the customer's engineering staff. EXAR's Engineering Staff will work very closely with the customer to define the system and the objective IC specs to achieve the desired performance. EXAR's Engineering Staff will then provide the customer with a conceptual transistor level paper design of the circuit. It will be the customer's responsibility to breadboard and troubleshoot the circuit. EXAR will provide "handholding" during this stage, and assist the customer in determining the test specs and layout of the circuit (optional).

4. Layout: After the transistor level circuit schematic of the breadboard is finalized, the 200X **Master-Chip** layout sheets or Electronic Layout Sheets are used to do the interconnect. Since the interconnections of the circuit on the Master-Chip is an integral part of the design and can have a significant effect on the performance of the circuit, all critical paths and matched circuit components must be identified and taken into consideration in achieving an optimum layout. This layout sheet along with the test specification of the circuit, provided by the customer, and the pin-out (bonding diagram) form the integration package.

5. Integration: This service involves generating silicon from the layout sheet. After the Integration Package is ready, EXAR will take the layout sheet and digitize it. At this stage, EXAR will check the digitized plots versus transistor level circuit schematic. After digitization, Design Rule Check (DRC) is performed to eliminate any violations. The final digitized plots are then used to generate masks (working plates) using automated techniques.

Finally, metallization and passivation (glass or nitride) masking steps are performed on EXAR's premises to finish fabrication of the **Master-Chip** wafers. After the wafer fabrication is completed, prototypes are built at EXAR's in-house Hi-Rel assembly facility.
The prototypes are then fully evaluated and sent to the customer along with a prototype binder which includes all pertinent information. These prototypes are for electrical evaluation purposes only.

6. Wafer Foundry: In addition to all the services mentioned above, EXAR offers wafer foundry services utilizing its in-house state-of-the-art wafer fabrication line which includes all diffusion processes, epi, ion implantation, and a wide variety of deposition processes. Technologies offered cover all bipolar processes, including I^2L and high voltage, as well as metal and silicon gate CMOS. Services are also available for partial or full processing of wafers using customer owned emulsion or chrome tooling.

▷ CAE/CAD CAPABILITIES

For years EXAR has been using CAE/CAD design tools extensively for digital gate arrays. Capitalizing on this expertise and implementing technical innovations, we are proud to be the first to introduce design automation utilizing CAE/CAD tools into the area of linear semi-custom arrays. The linear CAE workstation concept, by eliminating the handcrafted layout methods, takes the black magic out of linear semi-custom design. This new, fully-automated linear, semi-custom design methodology utilizes CAE/CAD Daisy "Gate Master" workstations and dual layer metal linear semi-custom arays.

Auto placement and auto routing workstations drastically reduce the layout and digitizing turnaround times with added reliability. This built-in "correct by construction concept" is attained through on-line layout versus schematic (LVS) check, design rule check (DRC), and electrical rule check (ERC) features included in the design automation software. An additional benefit of design automation is the achievement of higher packing density (higher percent utilization) which enables EXAR to use smaller **Master-Chips** and to pass the cost savings on to our customers.

▷ MODELS AVAILABLE

For running simulations, SPICE model parameters (AC/DC) are available on bipolar (20V, 36V and 75V) and Bi-FET (36V, ion implant) processes. Contact EXAR for further information.

EXAR LINEAR MASTER-CHIPS

The following section profiles the available Exar linear Master-Chips.

INDUSTRY STANDARD (20V) ARRAYS

	A-100	B-100	C-100A	D-100	E-100	F-100	G-100	H-100	J-100	L-100	M-100
Transistors											
NPN, small	58	69	23	50	48	93	58	73	36	76	137
NPN, 100mA								2	2	2	4
NPN, 200mA	2					4	2			2	4
NPN, low noise											4
PNP, single collector	18	12	8								
PNP, dual collector				16	15	36	18	22	12	22	44
PNP, quad collector										4	8
PNP, vertical											4
Schottky Diodes	15	16	6								
15 N + Resistors								4		8	15
Base Resistors											
200Ω	16	28	8	15	6	18	19	33	8	27	60
450Ω	43	44	18	30	41	88	68	87	34	106	188
900Ω	43	46	20	28	34	68	65	81	30	78	140
1.8KΩ	29	39	13	29	27	61	44	60	24	53	104
3.6KΩ	28	36	12	24	30	61	27	36	20	36	84
Total Base Resistance	214K	266K	94K	178K	206K	433K	266K	356K	159K	348K	712K
Pinch Resistors											
30KΩ	4	6	2		5	9					
100KΩ	4										
60KΩ				2			8	8	4	10	16
90KΩ		6									
Pads	16	16	14	16	18	24	18	18	18	24	28
Die Size (mils)	73x83	85x85	56x62	80x81	82x82	98x115	90x90	95x80	R0x75	102x85	176x121

HIGH VOLTAGE (75V) ARRAY

	X-100
Transistors	
NPN, small	30
NPN, 100mA	
NPN, 200mA	4
PNP, dual collector	16
20Ω XU	1
Base Resistors	
500Ω	64
1KΩ	27
2KΩ	58
5KΩ	12
Total Base Resistance	234K
N+ Resistors	
5Ω	14
10Ω	7
20Ω	7
Pinch Resistors	
100K Ω Pinched	3
30K Ω Pinched	3
Pads	18
Die Size (mils)	115x95

BI-FET ARRAYS

	U-100	V-100	W-100
Transistors			
NPN, small	94	140	192
Supermatched small NPN's			16
NPN, 100mA	2		
NPN, 200mA		4	4
J-FET (P-channel)	4	4	8
PNP, dual collector	40	56	60
PNP, (med. vertical)	2	4	4
PNP, vertical	8	4	10
Base Resistors			
280Ω	40	40	24
450Ω	158	112	100
900Ω	56	72	100
1.8KΩ	32	64	88
3.6KΩ	32	56	72
Total Base Resistance:	305K	443K	559K
Implant Resistors			
1KΩ			32
5KΩ	16	32	32
10KΩ	16	32	32
20KΩ	16	32	32
50KΩ	16	32	28
Total Implant Resistance	1.36M	2.72M	2.55M
Cross Unders			
15Ω XU	9	4	
5Ω XU		8	
30Ω LVXU (5V max)		8	
15Ω LVXU	4	4	
Capacitors			
MOS capacitors (10pF max)	4	4	8
Pads	28	28	40
Die Size (mils)	110x110	146x113	163x133

NOTE: LV—low voltage (5V max. to substrate). *XU—N+ cross under*

CELLULAR ARRAY

	CA-100
Transistors	
NPN, small	96
NPN, 100mA	
NPN, 200mA	2
NPN, low noise	4
PNP, large	2
PNP, dual collector	60
8Ω LV XU (5V Max) to substrate	16
28Ω N+ Resistors	22
16Ω N+ Resistors	18
20Ω N+ Resistors	20
30Ω N+ Resistors	4
Base Resistors	
400Ω	80
800Ω	42
2KΩ	42
2.4KΩ	32
Total Base Resistance	226K
Implant Resistors	
3KΩ	28
9KΩ	38
27KΩ	38
36KΩ	28
Total Implant Resistors	2.46M
Capacitors	
Junction Cap (5V diff max 25pf)	4
MOS Capacitor (Max 10pf)	2
Pads	28
Die Size (mils)	122x77

I²L ARRAYS

Array-Name	Gate Count*	Schottky Bi-Polar I/O Interfaces	Bonding Pads	Operating Voltage	Max. Toggle Frequency	Internal Delay/Gate	Note Ij = Injector Current
XR-200	192	24	30	7V	60 KHz	0.6μs	@ Ij = 1μA
XR-300	288	28	34	7V	400 KHz	100ns	@ Ij = 10μ
XR-400**	256	18	40	7V			
XR-500	520	40	42	7V	2 MHz	50 ns	@ Ij = 100μA

*5 Output I²L gates

**XR-400 also has PNP, NPN devices and diffused resistors to allow analog and digital functions on the same chip.

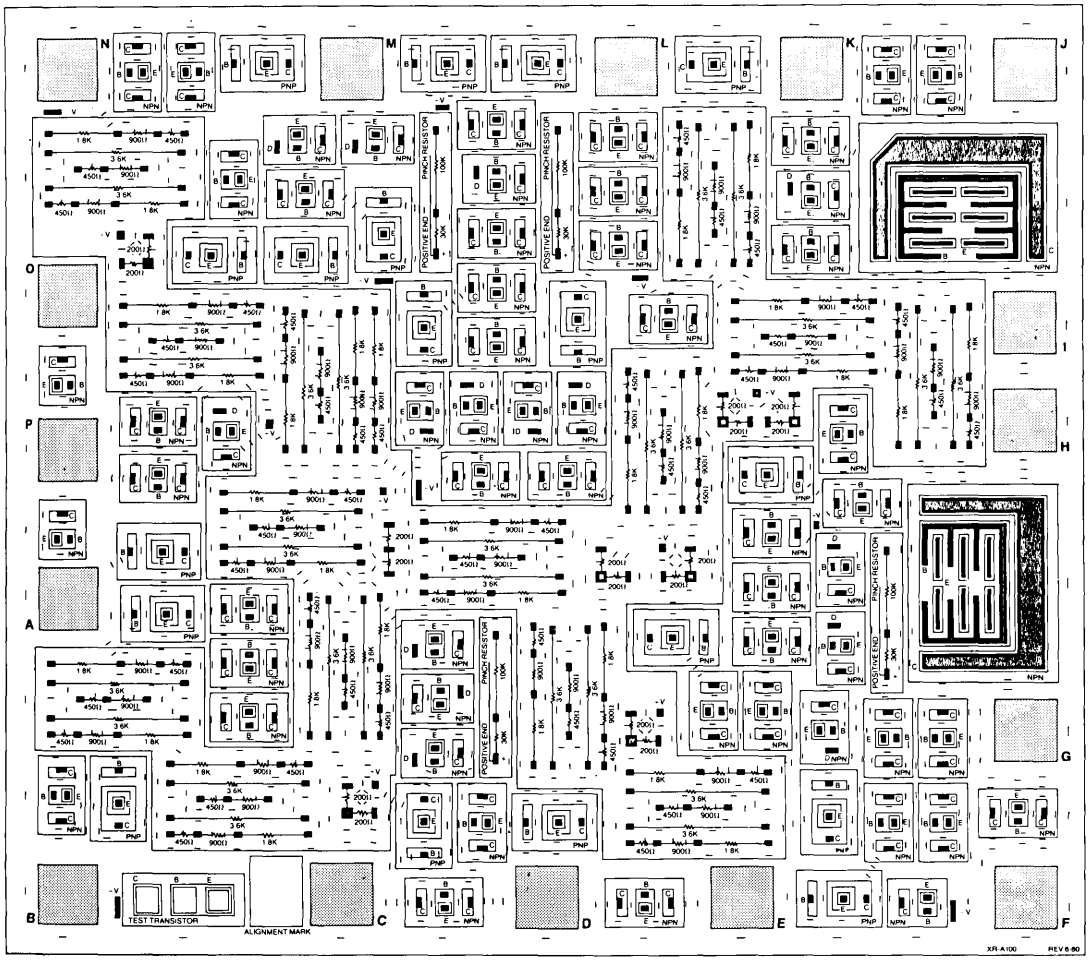
EXAR Master-Chips™

XR-A100 Master-Chip™

Chip Size: 73 × 83 mils
Total Components: 276
Bonding Pads: 16
Max. Operating Voltage: 20V

NPN Transistors
  Small Signal: 58
  High Current: 2 (200 mA)
PNP Transistors: 18
Schottky Diodes: 15

Pinch Resistors
  30kΩ: 4
  100kΩ: 4
Diffused Resistors
  200Ω: 16 1.8kΩ: 29
  450Ω: 43 3.6kΩ: 28
  900Ω: 43
Total Base Resistance: 214kΩ



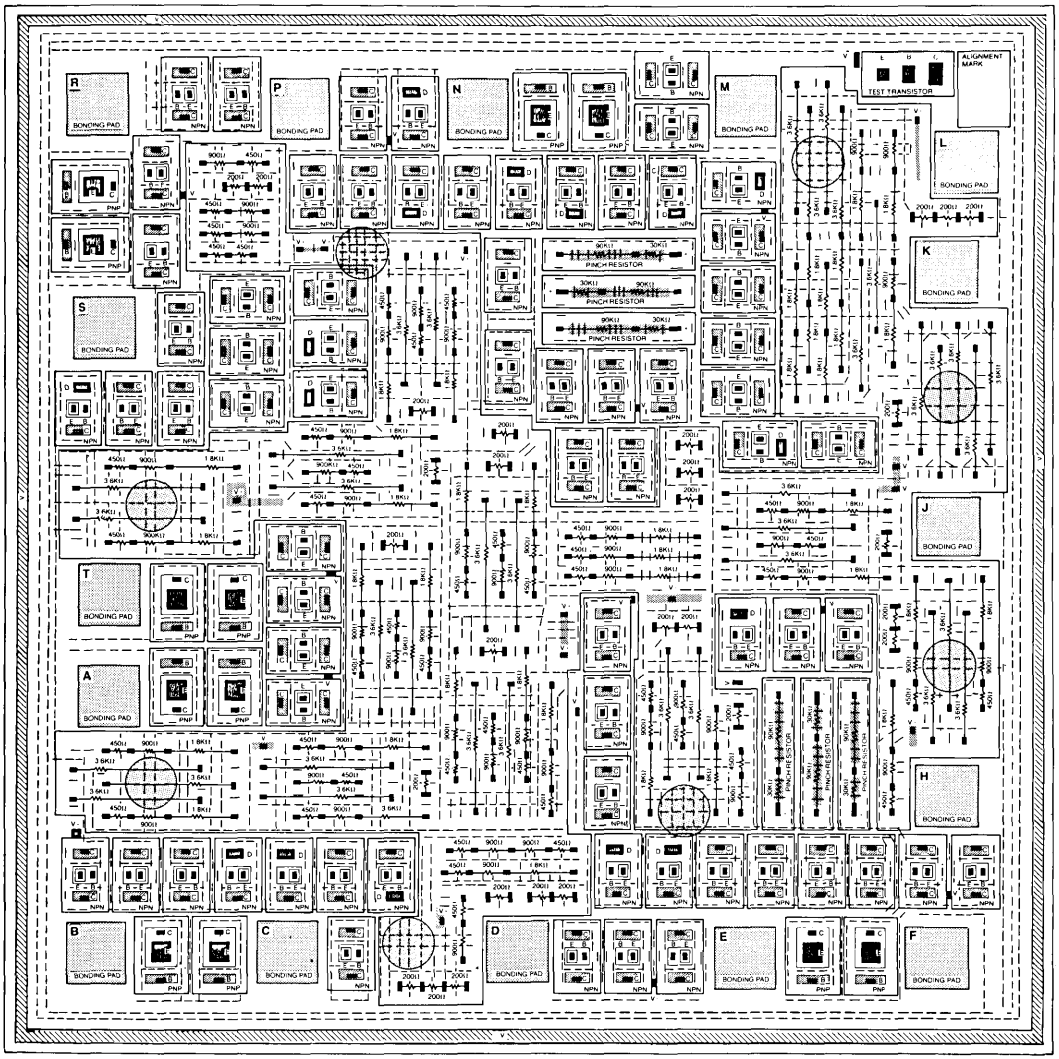
XR-A100

XR-B100 Master-Chip™

Chip Size: 85 × 85 mils
Total Components: 318
Bonding Pads: 16
Max. Operating Voltage: 20V

NPN Transistors
Small Signal: 69
High Current: None
Dual PNP Transistors: 12
Schottky Diodes: 16

Pinch Resistors
30kΩ: 6
90kΩ: 6
Diffused Resistors
200Ω: 28 1.8kΩ: 39
450Ω: 44 3.6kΩ: 36
900Ω: 46
Total Base Resistance: 266kΩ



XR-B100

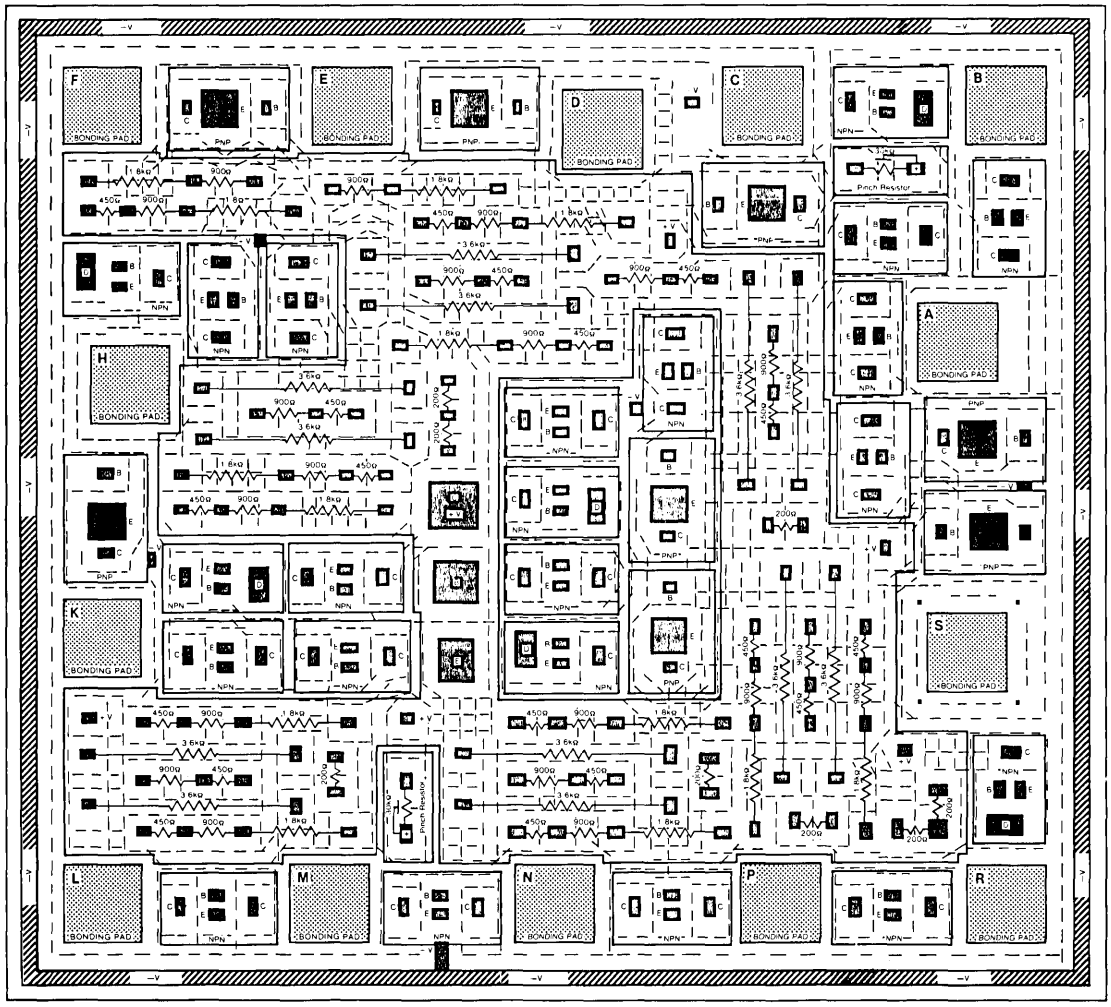
9

XR-C100A Master-Chip™

Chip Size: 56 × 62 mils
Total Components: 124
Bonding Pads: 14
Max. Operating Voltage: 20V

NPN Transistors
Small Signal: 23
High Current: None
PNP Transistors: 8
Schottky Diodes: 6

Pinch Resistors
30kΩ: 2
Diffused Resistors
200Ω: 8 1.8kΩ: 13
450Ω: 18 3.6kΩ: 12
900Ω: 20
Total Base Resistance: 94kΩ



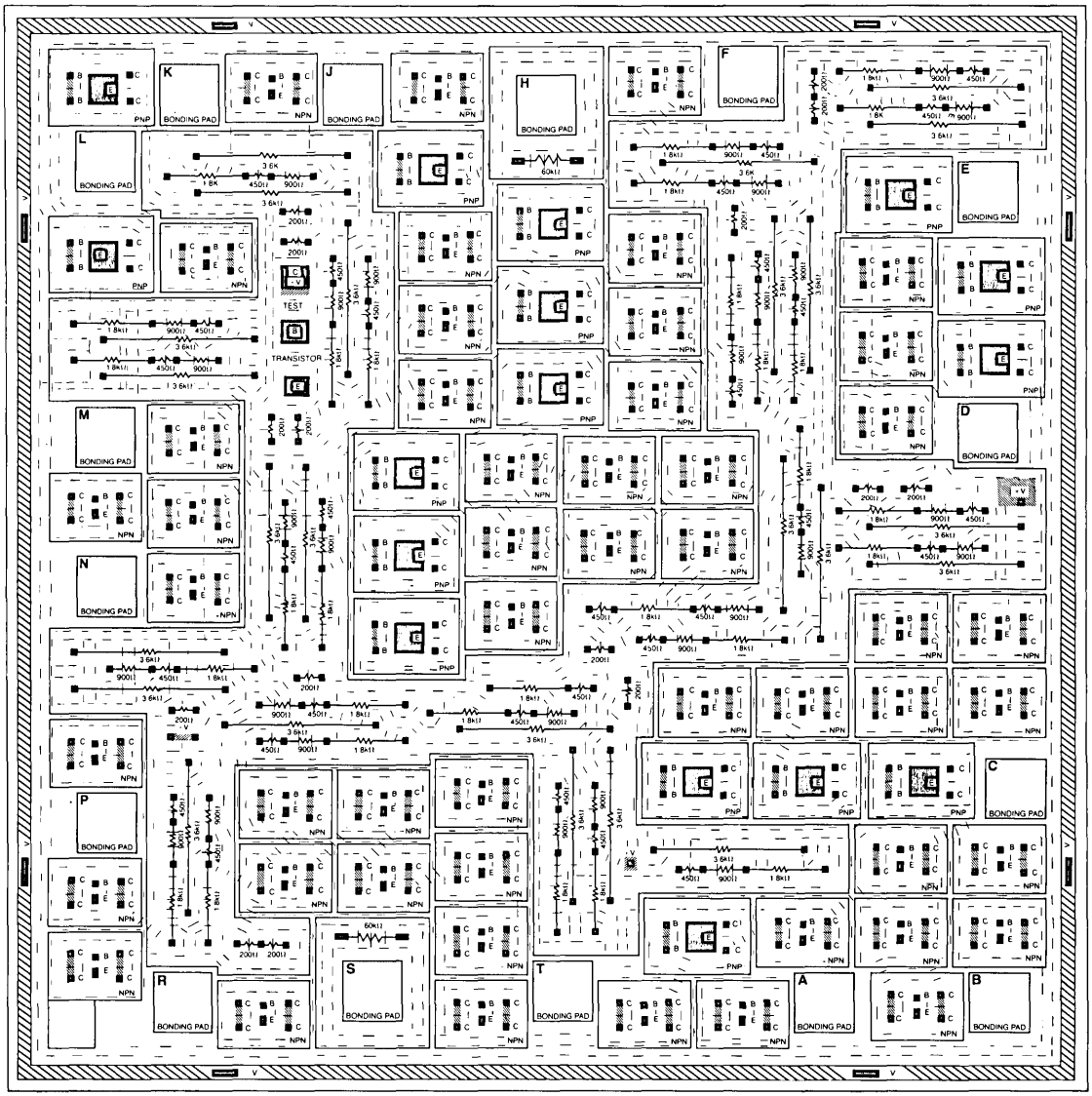
XR-C100A

XR-D100 Master-Chip™

Chip Size: 80 × 81 mils
Total Components: 210
Bonding Pads: 16
Max. Operating Voltage: 36V

NPN Transistors
  Small Signal: 50
Dual PNP Transistors: 16

Pinch Resistors
  60kΩ: 2
Diffused Resistors
  200Ω: 15 1.8kΩ: 29
  450Ω: 30 3.6kΩ: 24
  900Ω: 28
Total Base Resistance: 178kΩ



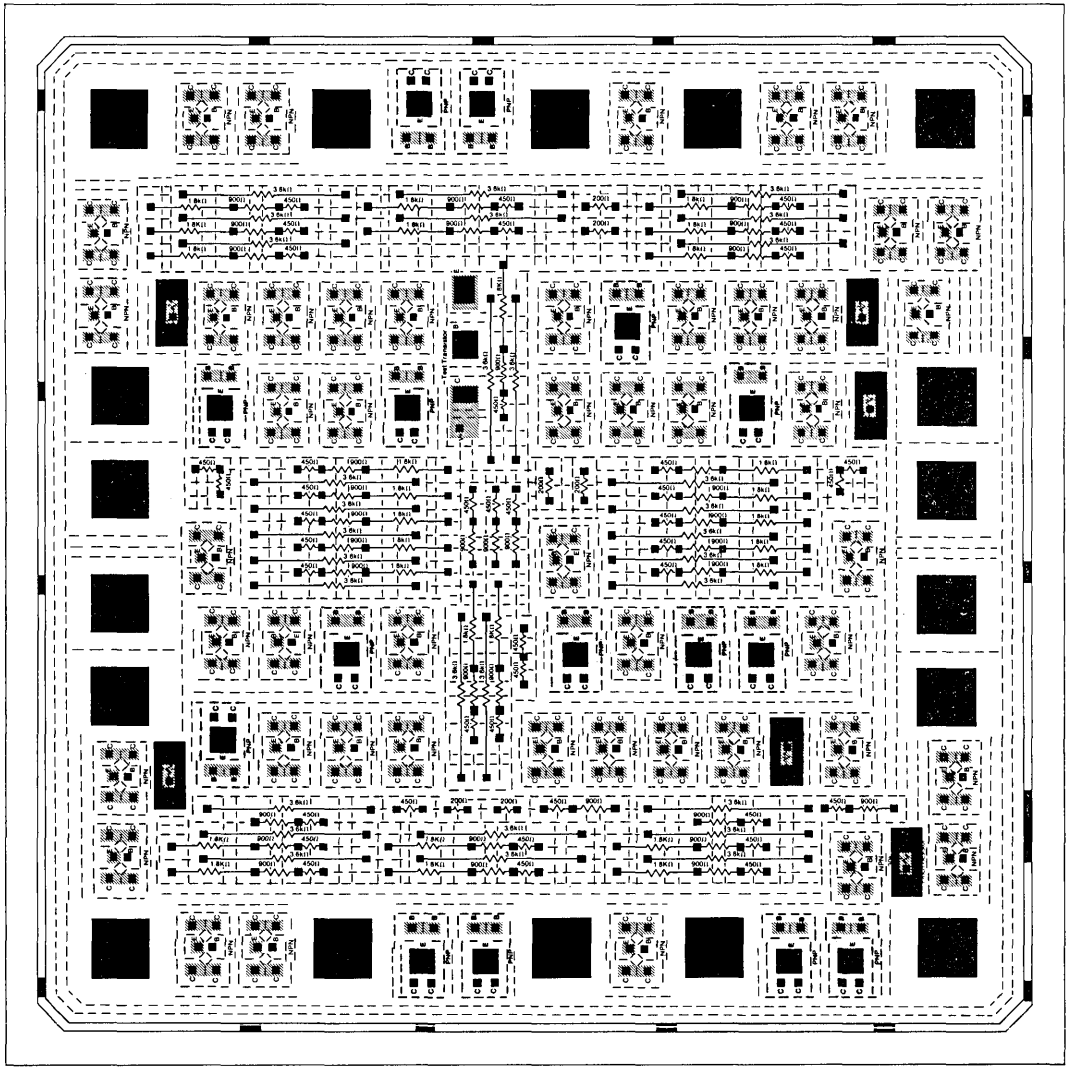
XR-D100

XR-E100 Master-Chip™

Chip Size: 82 × 82 mils
Total Components: 224
Bonding Pads: 18
Max. Operating Voltage: 20V

NPN Transistors
Small Signal: 48
Dual PNP Transistors: 15

Pinch Resistors
30kΩ: 5
Diffused Resistors
200Ω: 6 1.8kΩ: 27
450Ω: 41 3.6kΩ: 30
900Ω: 34
Total Base Resistance: 206kΩ



XR-E100

XR-F100 Master-Chip™

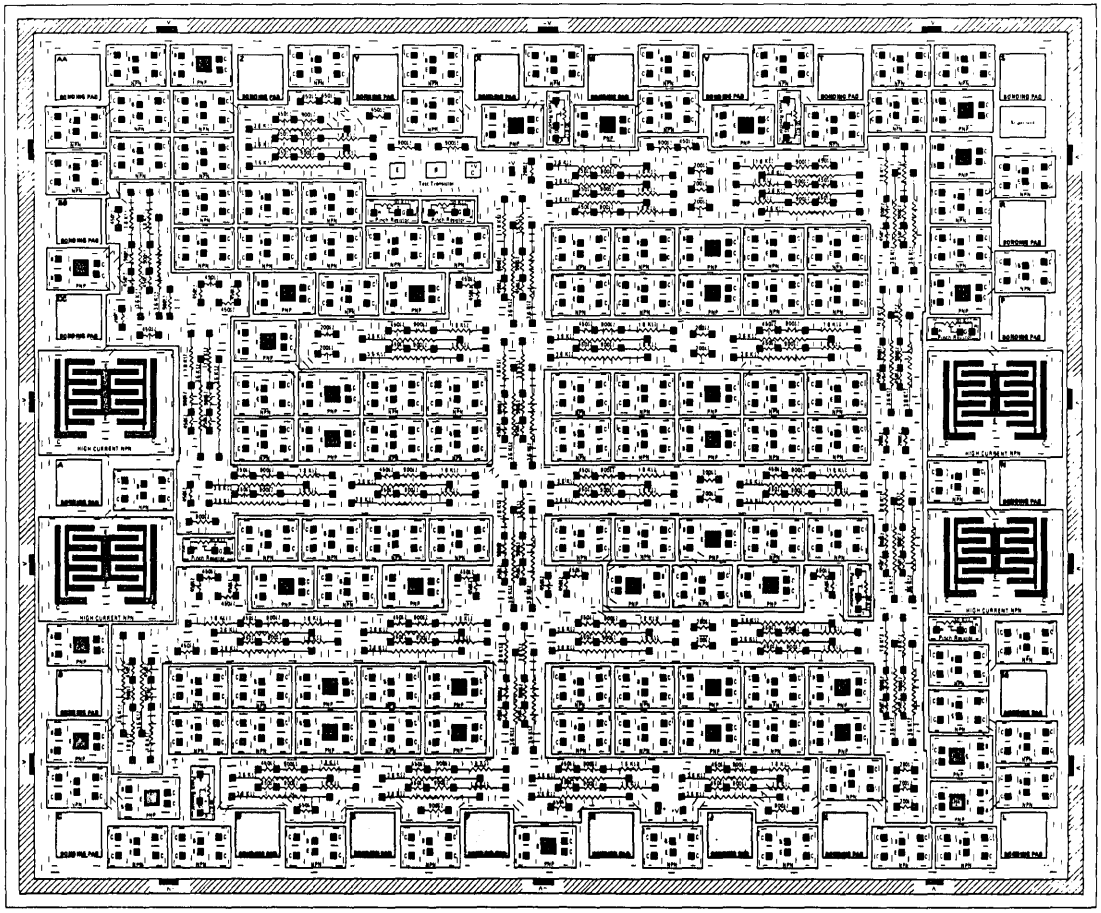
Chip Size: 98 × 115 mils
Total Components: 462
Bonding Pads: 24
Max. Operating Voltage: 20V

NPN Transistors
Small Signal: 93
High Current: 4
Dual PNP Transistors: 36

Pinch Resistors
30kΩ: 9

Diffused Resistors
200Ω: 18
450Ω: 88
900Ω: 68
1.8kΩ: 61
3.6kΩ: 61

Total Base Resistance: 433kΩ



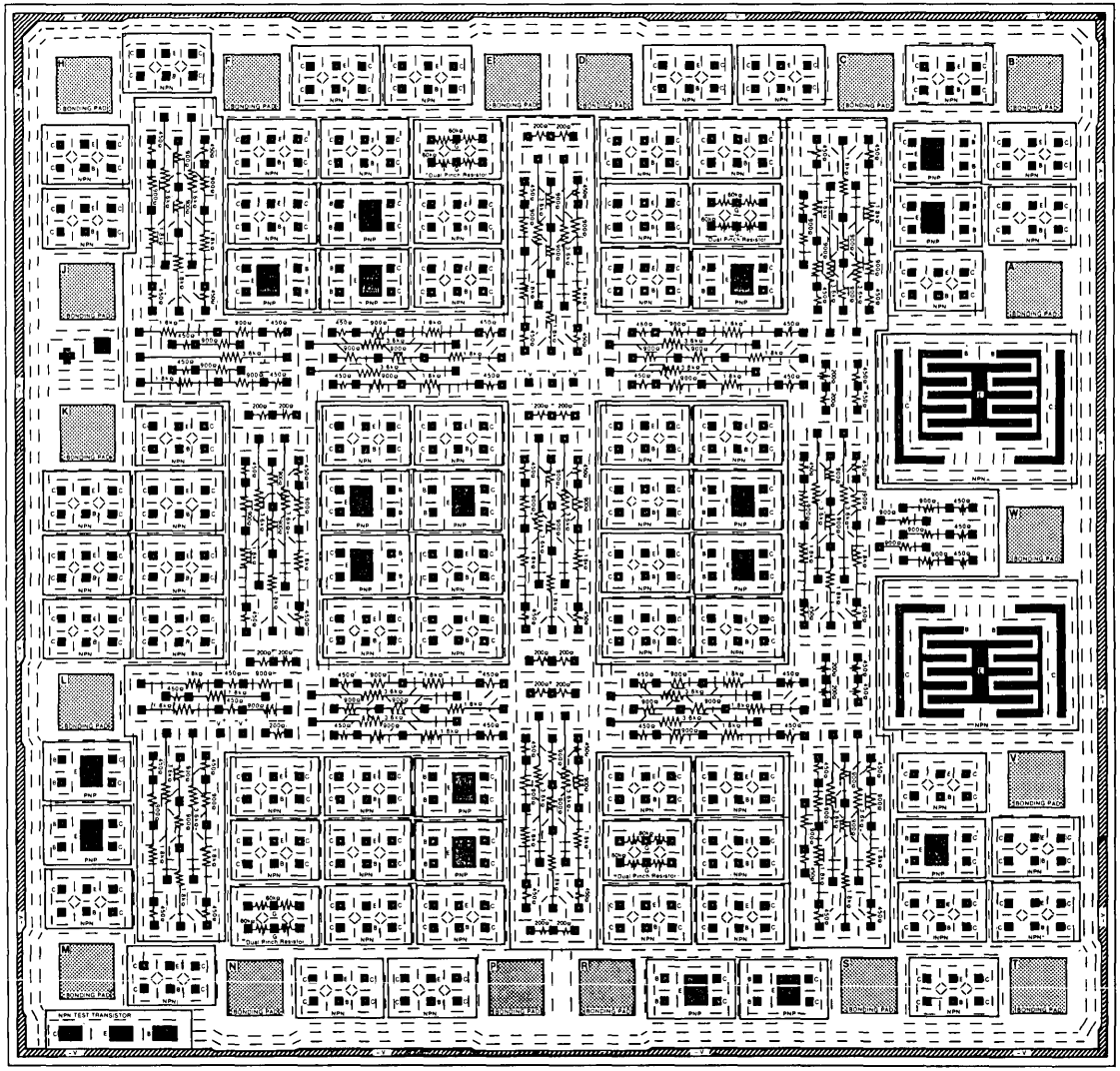
XR-F100

XR-G100 Master-Chip™

Chip Size: 90 × 90 mils
Total Components: 327
Bonding Pads: 18
Max. Operating Voltage: 20V

NPN Transistors
  Small Signal: 58
  High Current: 2
PNP Transistors: 18
Schottky Diodes: None

Pinch Resistors
  60kΩ: 8
Diffused Resistors
  200Ω: 19 1.8kΩ: 44
  450Ω: 68 3.6kΩ: 27
  900Ω: 65
Total Base Resistance: 266kΩ



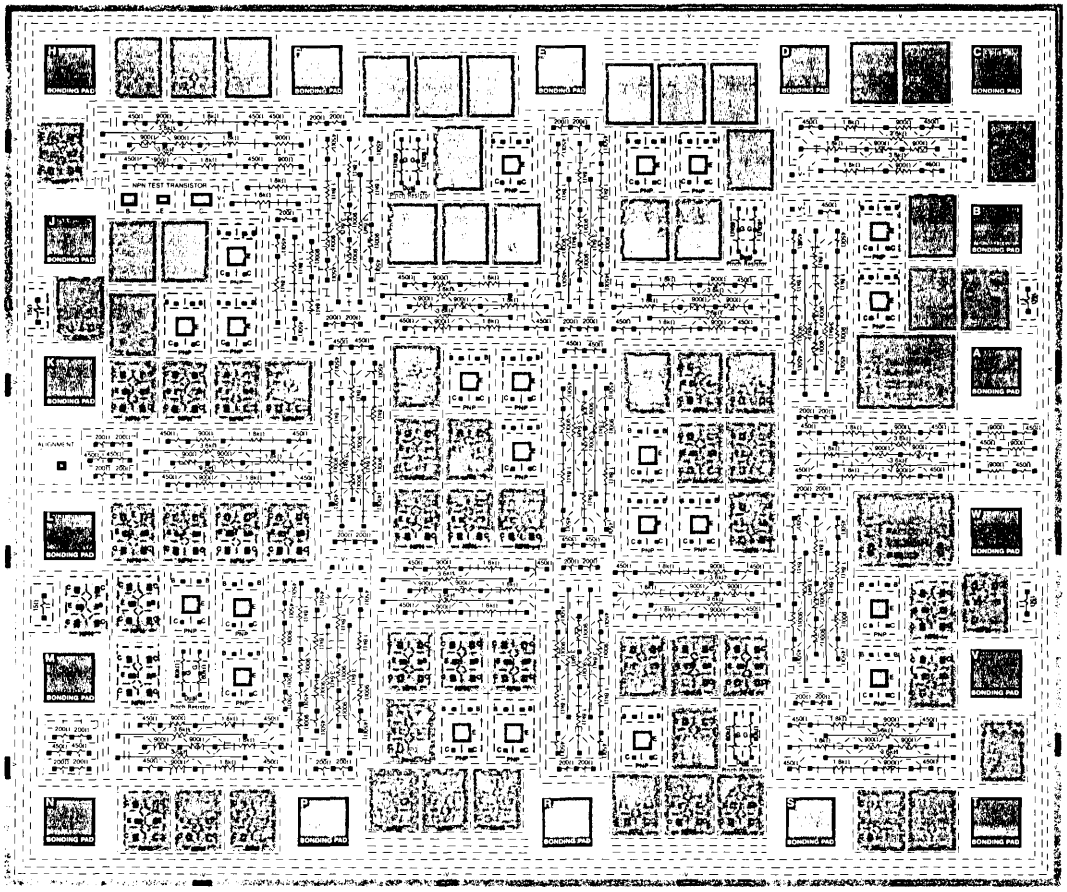
XR-G100

XR-H100 Master-Chip™

Chip Size: 95 × 80 mils
Total Components: 424
Bonding Pads: 18
Max. Operating Voltage: 20V

NPN Transistors
Small Signal: 73
Medium: 2
PNP Transistors
Lateral: 22

Pinch Resistors
60kΩ: 8
Diffused Resistors
200Ω: 33 1.8kΩ: 60
450Ω: 87 3.6kΩ: 36
900Ω: 81 15Ω (N^+): 4
Total Diffused Resistor: 356kΩ



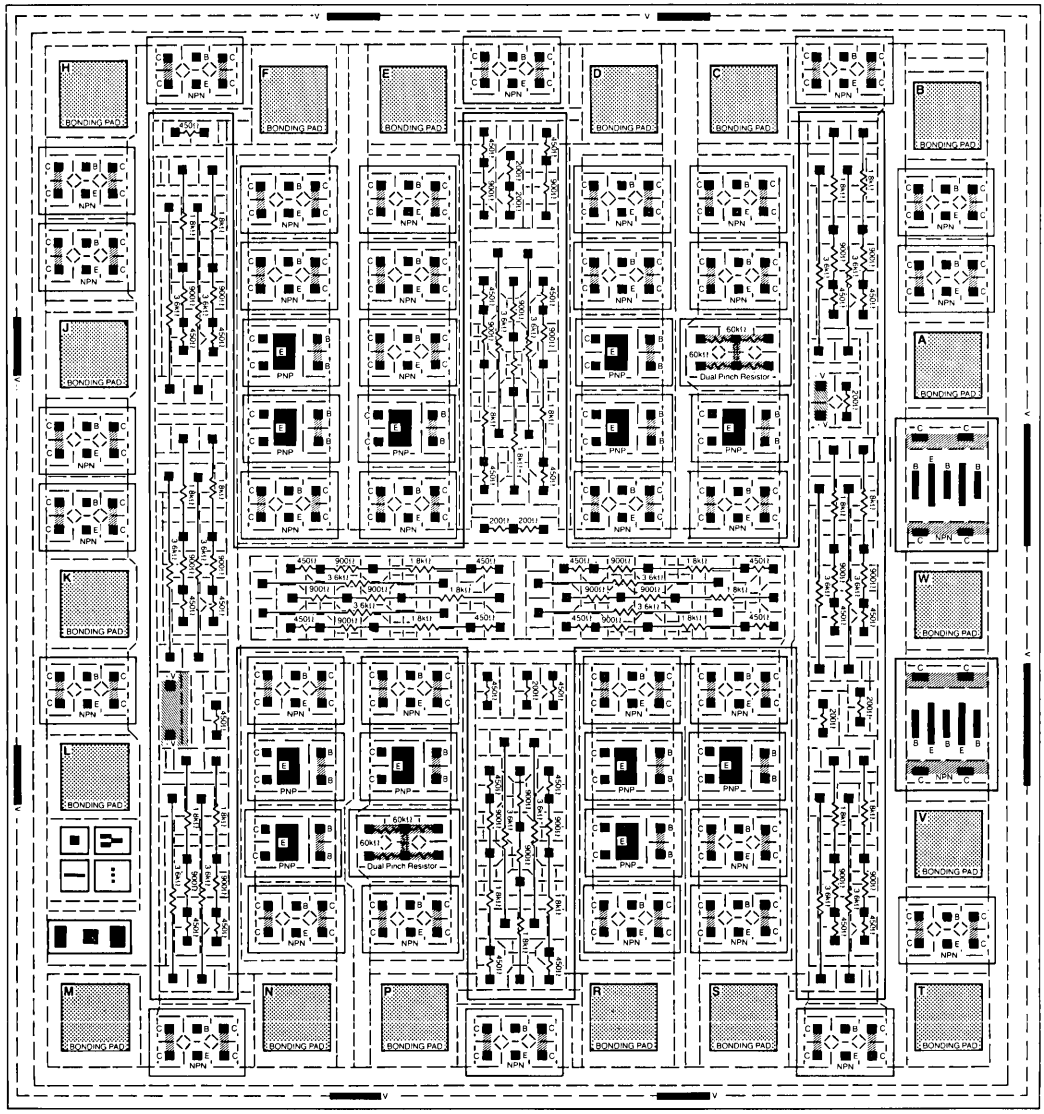
XR-H100

XR-J100 Master-Chip™

Linear, bipolar
Chip Size: 80 × 75 mils
Total Components: 188
Bonding Pads: 18
Max. Operating Voltage: 20V

NPN Transistors
Small Signal: 36
Medium: 2
Dual PNP Transistors: 12

Pinch Resistors
60kΩ: 4
Diffused Resistors
200Ω: 8 1.8kΩ: 24
450Ω: 34 3.6kΩ: 20
900Ω: 30
Total Base Resistance: 159kΩ



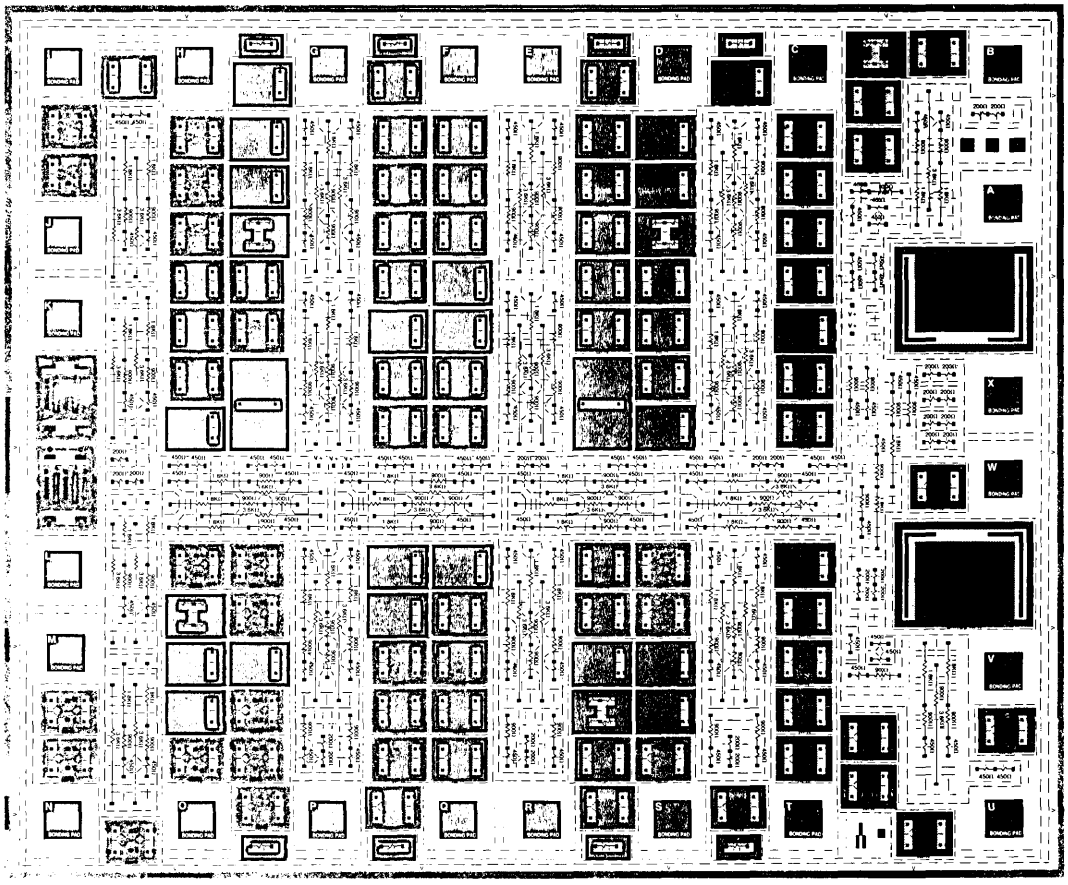
XR-J100

XR-L100 Master-Chip™

Chip Size: 102 × 85 mils
Total Components: 448
Bonding Pads: 24
Max. Operating Voltage: 20V

NPN Transistors
Small Signal: 76
Medium: 2
Large: 2
PNP Transistors
Lateral: 22
Quad Collector: 4

Pinch Resistors
60kΩ: 10
Diffused Resistors
200Ω: 27 1.8kΩ: 53
450Ω: 106 3.6kΩ: 36
900Ω: 78 15Ω (N^+): 8
Total Base Resistance: 348kΩ



XR-L100

XR-M100 Master-Chip™

Chip Size: 176 × 121 mils
Total Components: 840
Bonding Pads: 28
Max. Operating Voltage: 20V

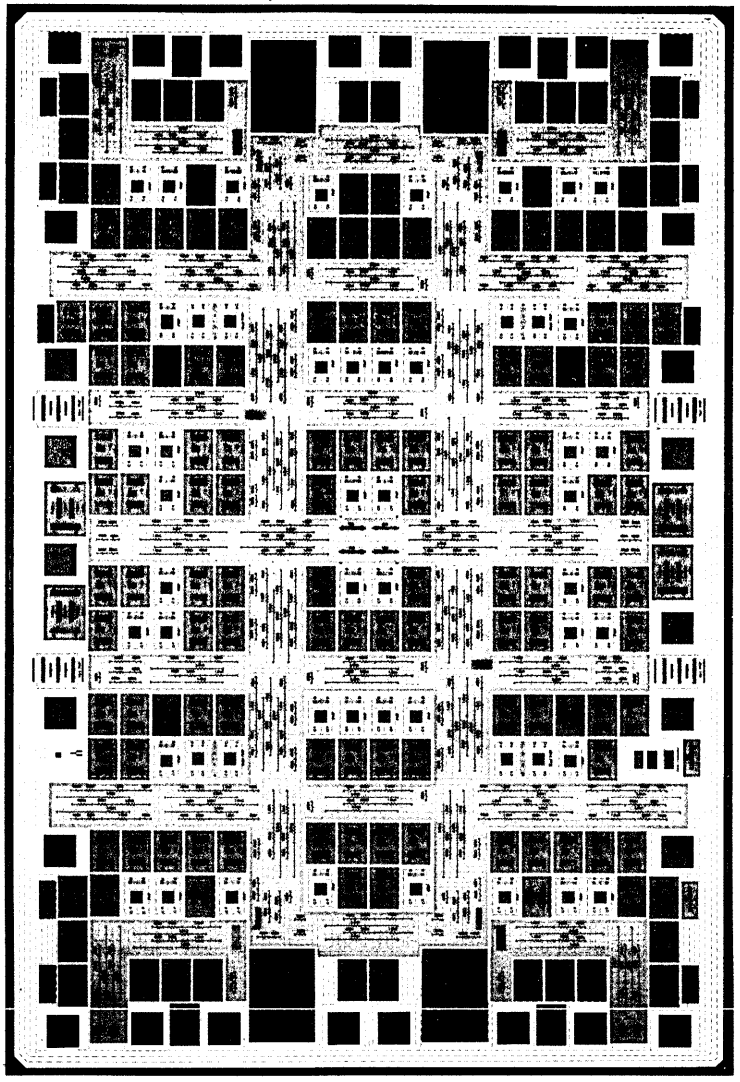
NPN Transistors
- Small Signal: 137
- Low Noise: 4
- Medium: 4
- Large: 4

PNP Transistors
- Lateral: 44
- Quad Collector: 8
- Large Vertical: 4

Pinch Resistors
- 60kΩ: 16

Diffused Resistors
- 200Ω: 60
- 450Ω: 188
- 900Ω: 140
- 1.8kΩ: 104
- 3.6kΩ: 84
- 15Ω (N^+): 15

Total Base Resistance: 712kΩ



XR-M100

XR-U100 Master-Chip™

Transistors
Total Components: 577
NPN, small: 94
NPN, 100 mA: 2
J-FET (P-channel): 4
PNP, dual collector: 40
PNP, med. vertical: 2
PNP, vertical: 8

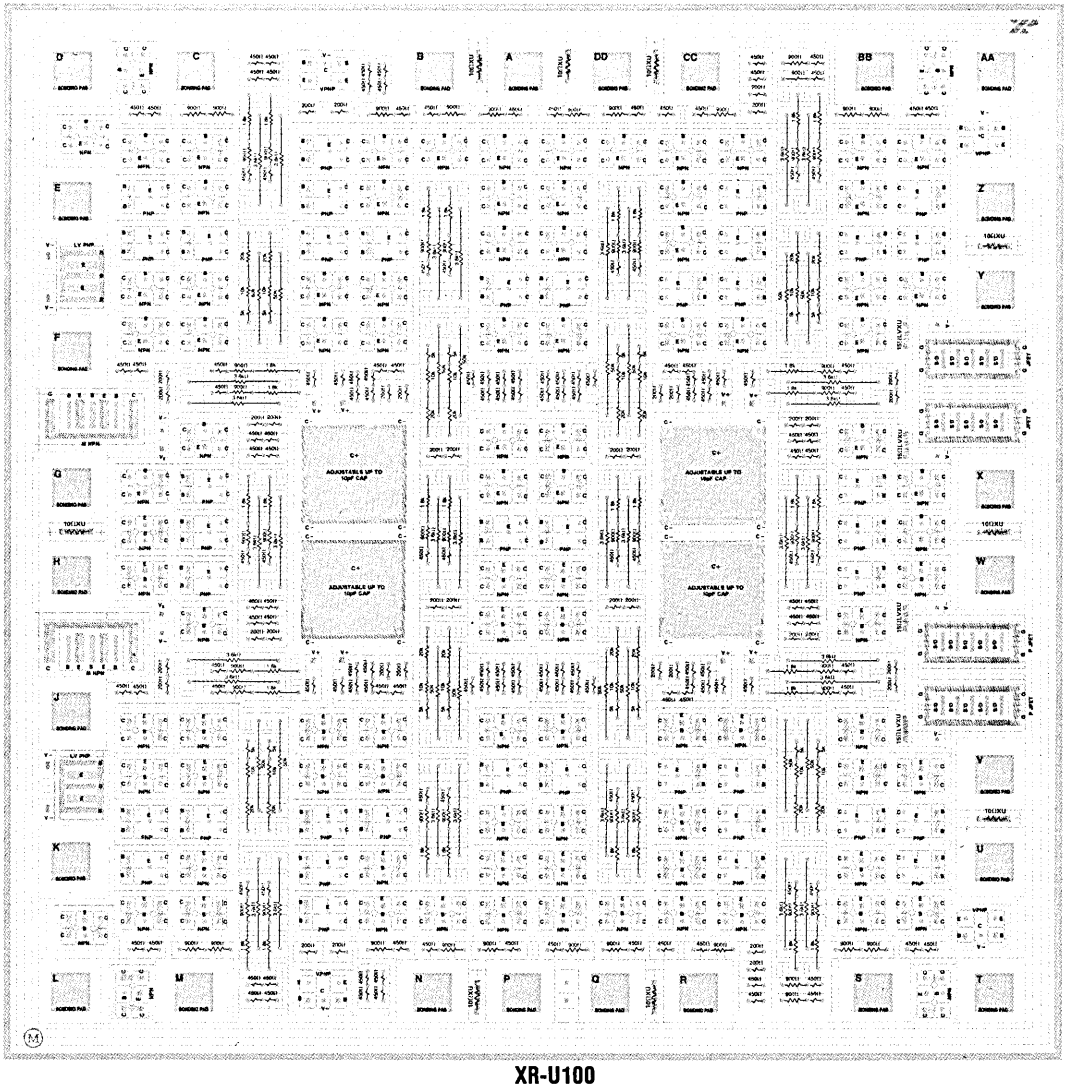
Implant Resistors
5kΩ: 16
10kΩ: 16
20kΩ: 16
50kΩ: 16
Total Implant Resistance: 1.36MΩ

Base Resistors
280Ω: 40
450Ω: 158
900Ω: 56
1.8kΩ: 32
3.6kΩ: 32
Total Base Resistance: 305kΩ

Cross Unders (N^+)
15Ω XU: 9
15Ω LVXU: 4

Capacitors
MOS Capacitors (10pF max): 4
Pads: 28
Die Size (mils): 110 × 110

NOTE: LV – low voltage (5V max. to substrate). XU – N + cross under.



XR-U100

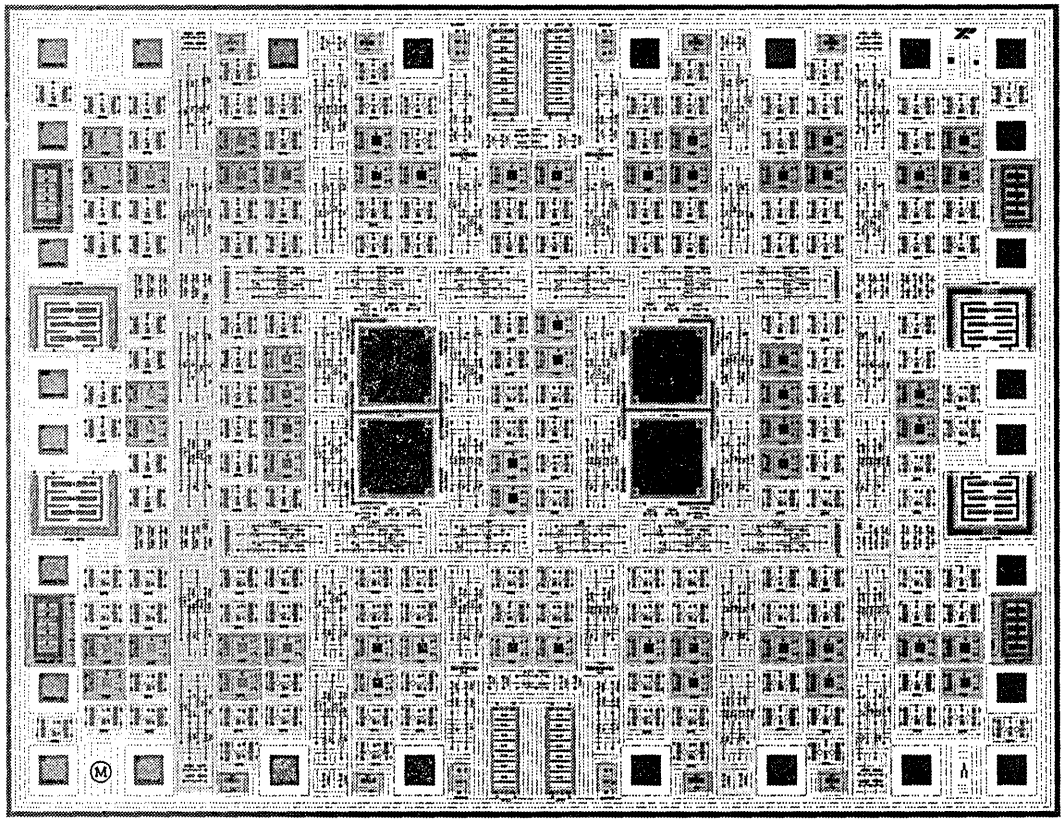
XR-V100 Master-Chip™

Chip Size: 113 × 146 mils
Total Components: 740
Bonding Pads: 28
Max. Operating Voltage: 36V

NPN Transistors
  Small Signal: 140
  Large: 4
PNP Transistors
  Lateral: 56
  Small Vertical: 4
  Medium Vertical: 4
JFET Transistors
  P-Channel: 4

Diffused Resistors
  280Ω: 40 3.6kΩ: 56
  450Ω: 112 1.8kΩ: 64
  900Ω: 72
Total Resistance: 443kΩ
Ion Implant
  50kΩ: 32 5kΩ: 32
  20kΩ: 32 10kΩ: 32
Total Resistors: 2.72 MΩ
Cross Under Resistors (N^+)
  5Ω: 8
  15Ω: 4
  LVXU (5V) 15Ω: 4
  LVXU (5V) 30Ω: 8

Oxide Capacitor: 4 × 10 pF



XR-V100

XR-W100 Master-Chip™

Chip Size: 163 × 133 mils
Total Components: 882
Bonding Pads: 40
Max. Operating Voltage: 36V

NPN Transistors
- Small Signal: 196
- Supermatched Small Signal: 16
- Large: 4

PNP Transistors
- Lateral: 60
- Small Vertical: 10
- Large Vertical: 4

Diffused Resistors
- 200Ω: 24
- 450Ω: 100
- 900Ω: 100
- 1.8kΩ: 88
- 3.6kΩ: 72

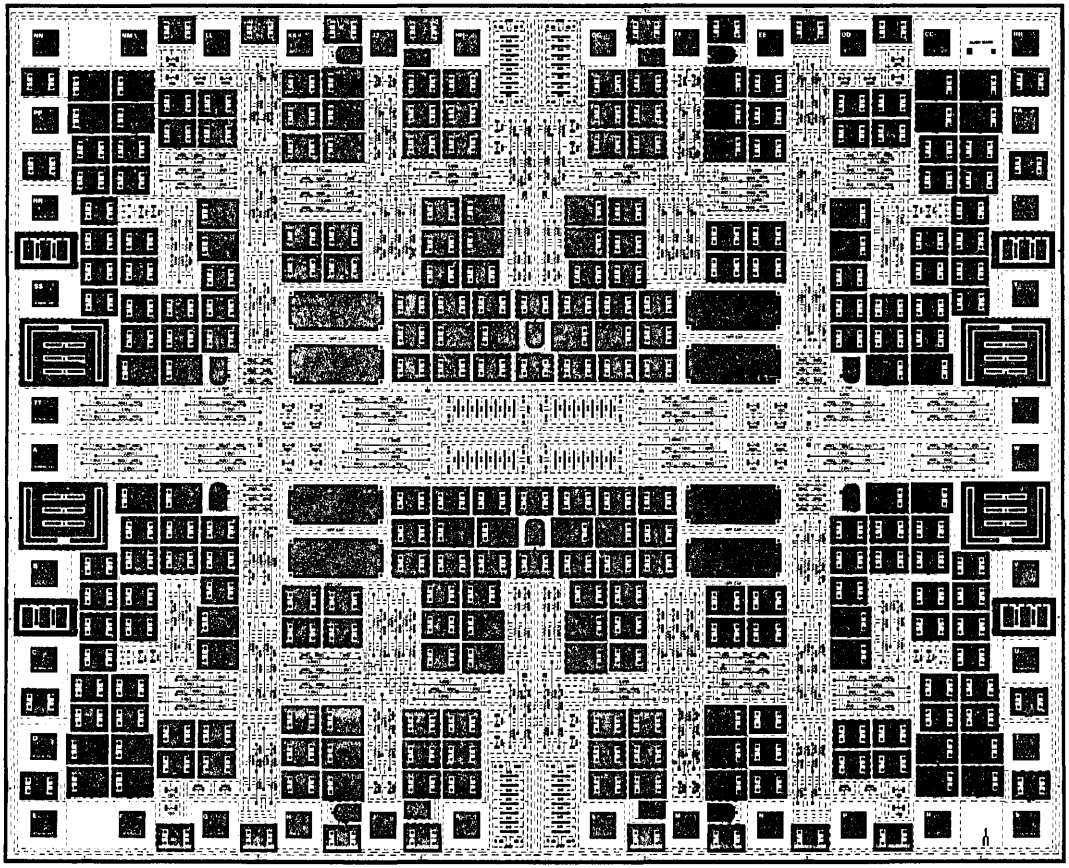
Total Resistance: 559kΩ

Ion Implant
- 50kΩ: 28
- 20kΩ: 32
- 10kΩ: 32
- 5kΩ: 32
- 1kΩ: 32

Total Implant Resistors: 2.55 MΩ

Cross Under Resistors (N^+)
- 5Ω: 4

Oxide Capacitor: 8 × 10 pF



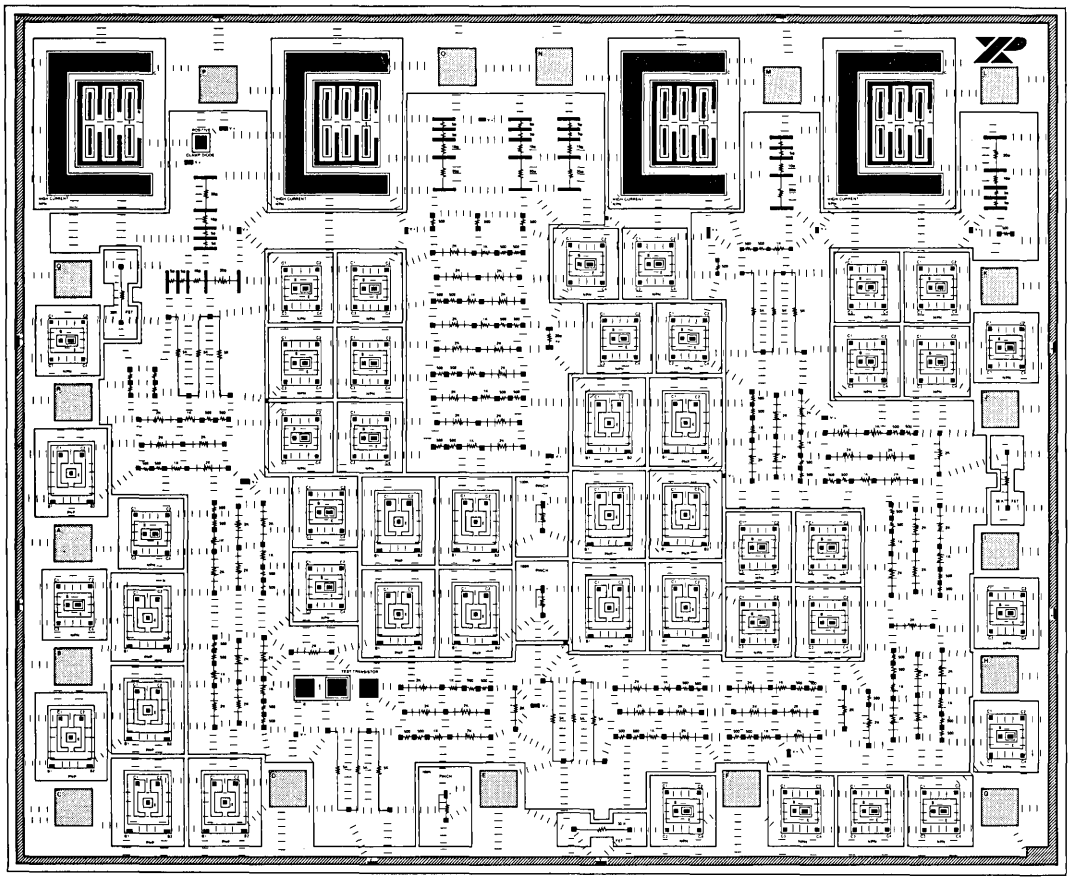
XR-W100

XR-X100 Master-Chip™

Chip Size: 115 × 95 mils
Total Components: 293
Bonding Pads: 18
Max. Operating Voltage: 75V

NPN Transistors
Small Signal: 30
High Current: 4
PNP Dual Collector
Transistors: 46

Pinch Resistors
30kΩ: 3
100kΩ: 3
Diffused Resistors
(N+) 5Ω: 14 1kΩ: 27
(N+) 10Ω: 7 2kΩ: 58
(N+) 20Ω: 7 5kΩ: 12
500Ω: 64
Total Base Resistance: 234kΩ



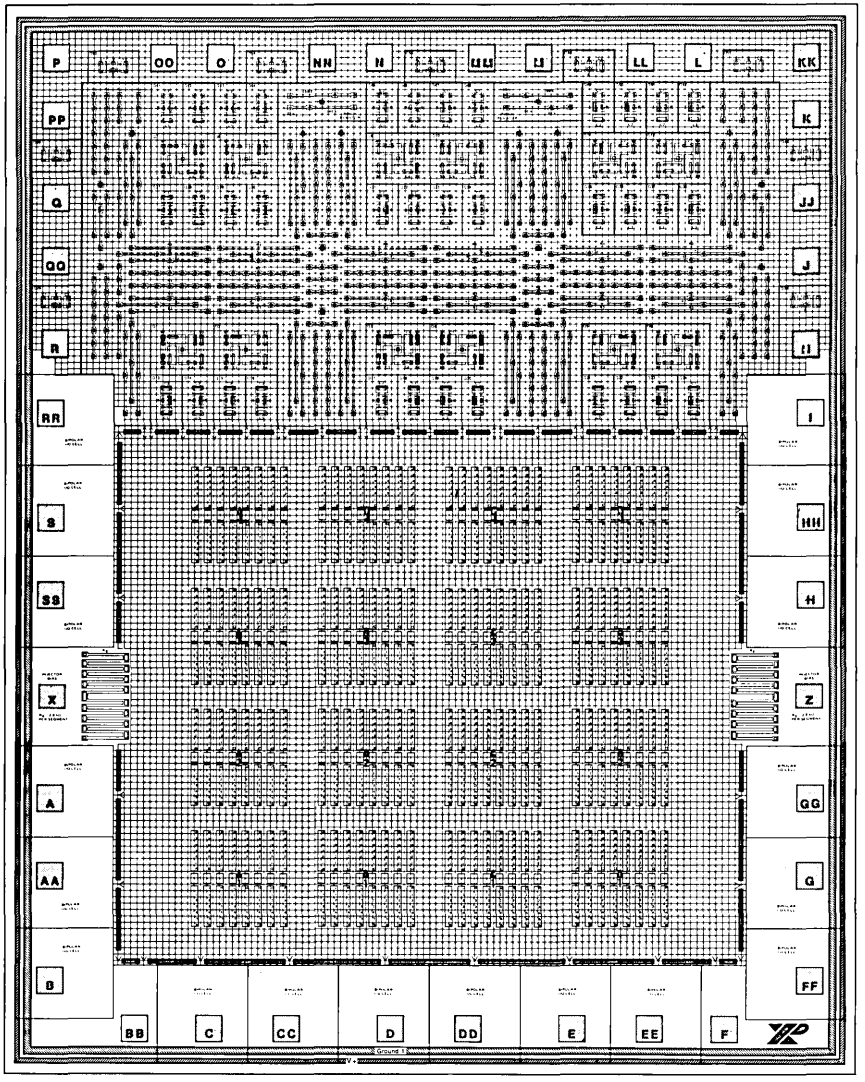
XR-X100

XR-400 I2L Master-Chip™

Chip Size: 119 × 149 mils
5-Output I^2L Gates: 256
Bonding Pads: 40
Max. Operating Voltage: 7V

NPN Transistors: 45
4-Collector PNP
Transistors: 12
Schottky-Bipolar I/O
Interfaces: 18

Diffused Resistors
700Ω: 200
2.5kΩ: 116
5kΩ: 20
Total Resistance: 530k



XR-400 I^2L

ELECTRICAL CHARACTERISTICS OF LINEAR MASTER-CHIP COMPONENTS

The following tables list the electrical characteristics of the circuit components available on Exar's linear Master-Chips. Whenever applicable, the "worst case" tolerances and the parameter distributions are also listed.

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
Small-Signal NPN Transistors			
Current gain (h_{FE}) @ 1 mA, 5V	180	—	80–300
Temperature Coefficiency of h_{FE}			
−55°C to 25°C	+0.5%/°C	—	—
25°C to 125°C	+1%/°C	—	—
Matching of h_{FE}	—	3%	10%
Breakdown voltage (LV_{CEO})			
20-V Master-Chips	23V	—	20–30V
36-V Master-Chips	40V	—	36–50V
Collector-Base Leakage Current @ 20 V	1 nA	—	0.1–50 nA
Cutoff Frequency (f_T) @ 5 mA	500 MHz	—	—
Storage Time (t_S)	50 nsec	—	—
Saturation Resistance (All except D100)			
One collector contact	100 Ohms	±50 Ohms	60–160 Ohms
Two collector contacts	50 Ohms	±20 Ohms	30–80 Ohms
Saturation Resistance (D100 chip)			
One collector contact	300 Ohms	±100 Ohms	150–480 Ohms
Two collector contacts	150 Ohms	±50 Ohms	75–240 Ohms
High-Current NPN Transistors			
Current Gain (h_{FE})			
@ 1 mA, 5V	180	—	80–300
@ 100 mA, 5V	100	—	50–200
Temperature Coefficient of h_{FE}			
−55°C to 25°C	+0.5%/°C	—	—
25°C to 125°C	+1%/°C	—	—
Matching h_{FE}	—	3%	10%
Breakdown Voltage (LV_{CEO})	23V	—	20–35V
Collector-Base Leakage Current @ 20V	20 nA	—	1–500 nA
Cutoff Frequency (f_T)	100 MHz	—	—
Storage Time (t_S)	200 nsec	—	—
Saturation Resistance	5 Ohms	±1 Ohm	3–8 Ohms
Lateral PNP Transistors			
Current Gain (h_{FE}) @ 100 μA, 5V	20	—	5–80
Temperature Coefficient of h_{FE}	±1.0%/°C	—	—
Matching of h_{FE}	—	5%	15%
Breakdown Voltage (LV_{CEO})			
20-V Master Chips	35V	—	25V − 40V
36-V Master Chips	45V	—	36 − 60V
Collector-Base Leakage Current @ 20V	5 nA	—	0.1 to 100 nA
Cutoff Frequency (f_T)	5 MHz	—	—
Storage Time (t_S)	500 nsec	—	—
Saturation Resistance	600 Ohms	±100 Ohms	300–900 Ohms
TRANSISTORS CONNECTED AS DIODES (Collector and Base Shorted)			
Small NPN			
Forward Voltage Drop @ 1 mA, 25°C	0.74V	±200 mV	0.68–0.8V
Forward Voltage Matching	—	2 mV	6 mV
Forward Voltage Tracking	—	5μV/°C	15μV/°C
Lateral PNP			
Forward Voltage Drop @ 200 μA, 25°C	0.70V	±200 mV	0.62–0.76V
Forward Voltage Matching	—	3 mV	5 mV
Forward Voltage Tracking	—	8 μV/°C	25 μV/°C

PARAMETERS	TYPICAL VALUES	σ-LIMIT	WORST CASE TOLERANCE
NPN Base-Emitter Junctions Used as Zener Diodes			
Small NPN Transistors			
Breakdown Voltage @ 100 μA			
20-V Master Chips	6.35V	±0.15V	5.9–6.8V
36-V Master Chips	6.7V	±0.2V	6.0–7.2V
Temperature Coefficient	+2.5 mV/°C	±0.3 mV/°C	1.8–3.1 mV/°C
Schottky-Barrier Diodes (A100/B100/C100 Only)			
Forward Voltage Drop @ 10 μA	0.36V	±0.02V	0.22 to 0.44V
Temperature Coefficient of Forward Voltage Drop	−1.5 mV/°C	±0.1 mV/°C	±0.3 mV/°C
Reverse Breakdown Voltage	30V	—	20–40V
Leakage Current @ 20V	200 nA	—	1 nA–1 μA
Diffused Resistors (All Master-Chips)			
Absolute Values	—	±10%	±25%
Temperature Coefficients			
−55°C to −25°C	−650 ppm/°C	±100 ppm	—
−25°C to 0°C	+150 ppm/°C	±40 ppm	—
0°C to 25°C	+680 ppm/°C	±40 ppm	—
25°C to 75°C	+1040 ppm/°C	±20 ppm	—
75°C to 125°C	+1400 ppm/°C	±40 ppm	—
Matching Between Resistors			
Identical Values	—	±0.8%	±2.4%
Non-Identical Values			
200–450	—	±1.6%	±4.8%
200–900	—	±1.7%	±5.1%
200–1.8K	—	±1.9%	±5.7%
200–3.6K	—	±2.0%	±6.0%
450–900	—	±1.5%	±4.5%
450–1.8K	—	±1.7%	±5.1%
450–3.6K	—	±1.9%	±5.7%
900–1.8K	—	±1.5%	±4.5%
900–3.6K	—	±1.7%	±5.1%
1.8K–3.6K	—	±1.5%	±4.5%
Pinch-Resistors			
Absolute Value Tolerance	±50%	—	+100% to −50%
Matching Between Identical Resistors	±20%	—	—
Breakdown Voltage	6.4V	—	—
Temp. Coefficient	+6,000 ppm/°C	—	8,000 ppm/°C

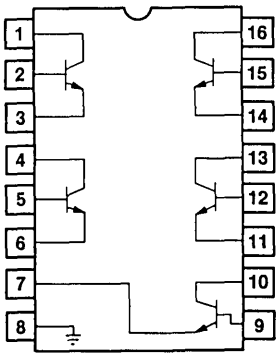
KIT PARTS

Please Note: Large NPN ≡ 200 ma
Medium NPN ≡ 100 ma
Small NPN ≡ 10 ma
* Absolute maximum ratings

Item	Kit Part No.	Description	Max Voltage	Applicable for Master-Chip
1.	XR-A103	Two 200 ma, & 3 Schottky transistors	20V	A-100, B-100, C-100
2.	XR-B101	5 small NPNs	20V	A-100, B-100, C-100
3.	XR-B202	5 lateral PNPs single collector	20V	A-100, B-100, C-100
4.	XR-F101	5 small NPNs	20V	All of these kit parts are useable for breadboarding the following Chips: E-100, F-100, G-100, H-100, J-100, L-100, and M-100.
5.	XR-F108	Four 200 ma NPNs	20V	
6.	XR-F206	4 lateral PNPs dual collector	20V	
7.	XR-J114	7 small NPNs – common base	20V	
8.	XR-J117	3 Wilson current sources NPNs	20V	
9.	XR-J215	7 PNPs common base	20V	
10.	XR-J216	3 Wilson current source PNPs	20V	
11.	XR-M111	4 small NPNs	20V	
12.	XR-M112	2 medium NPNs, 2 large vertical PNPs, 1 small NPN	20V	
13.	XR-M210	2 quad collector PNPs	20V	
14.	XR-D101	5 small NPNs	36V	D-100
15.	XR-D206	4 lateral PNPs dual collector	36V	D-100
16.	XR-W101	5 small NPNs	36V	U-100, V-100, W-100
17.	XR-W108	Four 200 ma NPNs	36V	U-100, V-100, W-100
18.	XR-W111	4 small NPNs	36V	U-100, V-100, W-100
19.	XR-W206	4 lateral PNPs dual collector	36V	U-100, V-100, W-100
20.	XR-W213	5 small, 2 large vertical PNPs	36V	U-100, V-100, W-100
21.	XR-W421	4 P channel, JFets	36V	U-100, V-100, W-100
22.	XR-CA111	4 small NPNs	20V	CA-100
23.	XR-CA118	2 large NPNs 2 large PNPs	20V	CA-100
24.	XR-CA206	4 dual collector PNPs	20V	CA-100
25.	XR-CA101	5 small NPNs	20V	CA-100
26.	XR-RN1	Resistor network		Applicable to all Master-Chips except U, V, and W100
27.	XR-RN2	Resistor network		Applicable to all Master-Chips except U, V, and W100
28.	XR-X101	5 small NPNs	75V	X-100
29.	XR-X108	Four 200 ma NPNs	75V	X-100
30.	XR-X206	4 lateral PNPs dual collector	75V	X-100

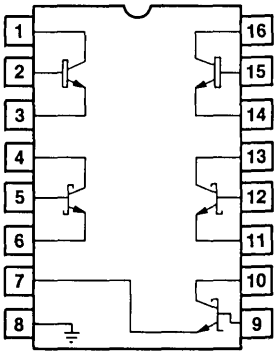
EXAR LINEAR KIT PARTS

101



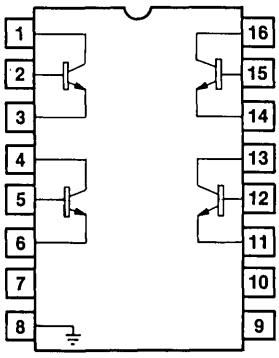
B-101
F-101
D-101
W-101
X-101

103



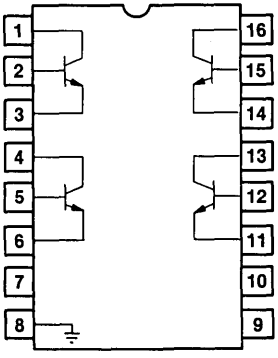
A-103

108



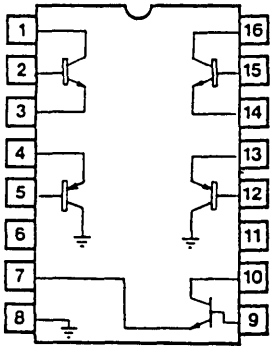
F-108
W-108
X-108

111



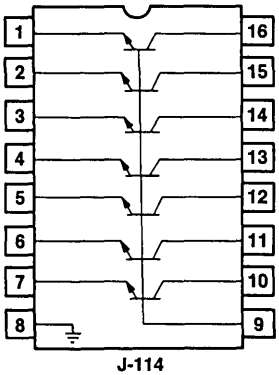
M-111
W-111

112



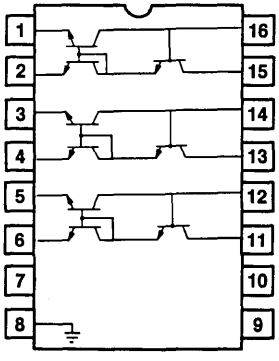
M-112
2 Medium NPNs
2 Large Vertical PNPs
1 Small NPN

114

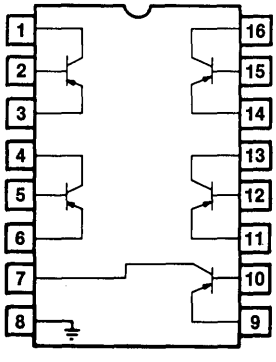


J-114

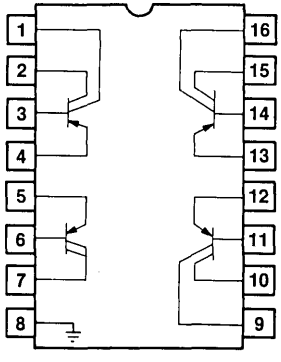
117



202

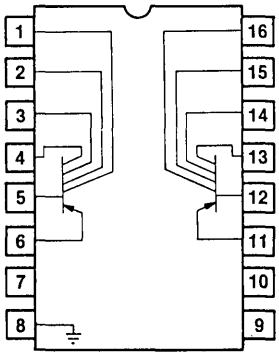


206



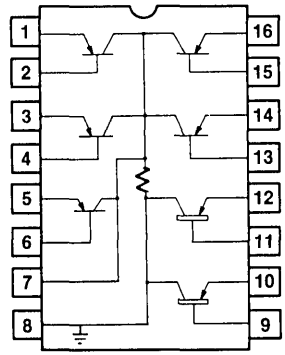
EXAR LINEAR KIT PARTS

210



M-210

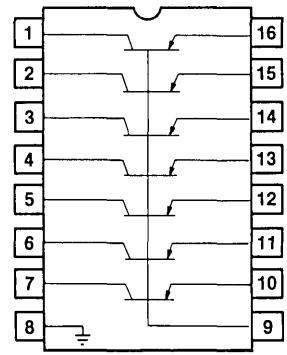
213



W-213

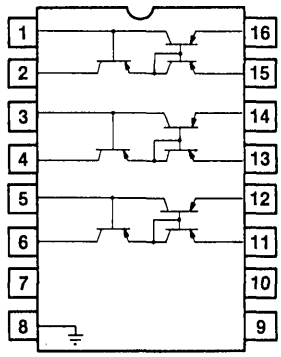
NOTE: 5 Small & 2 Large Vertical PNPs. Resistance shown is substrate resistance between middle and edge of die.

215



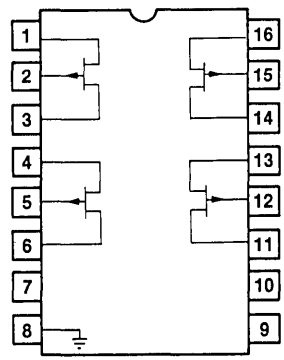
J-215

216



J-216

421

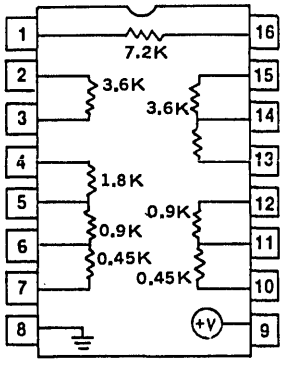


W-421

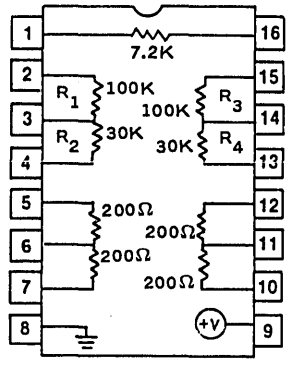
NOTE: *Drain and Source* are interchangeable.

Resistor Networks

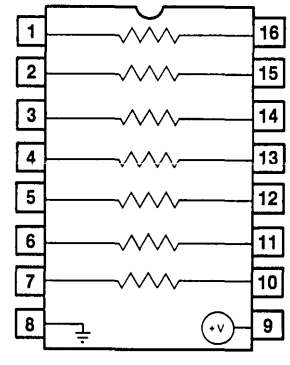
RN1



RN2

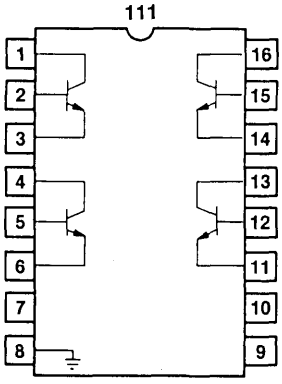


RN3

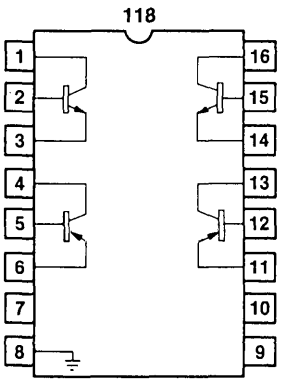


NOTE: All resistors are the same value

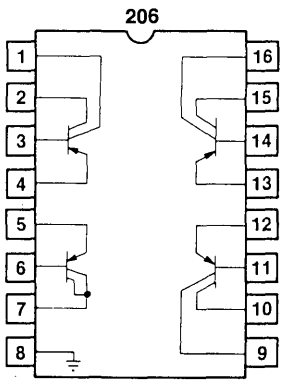
EXAR LINEAR KIT PARTS



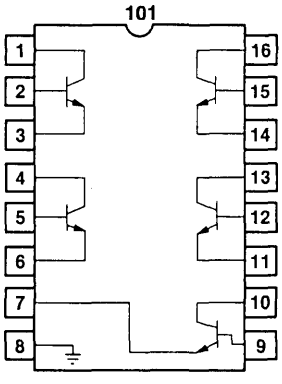
CA-111



CA-118



CA-206



CA-101

9

I^2L SEMI-CUSTOM DESIGN

Integrated Injection Logic (I^2L) technology extends the capabilities of semi-custom design to high complexity digital or combined analog/digital systems. Exar has made this possible by the development of a family of I^2L Master-Chips which combine a large number of I^2L gates and Schottky bipolar transistors on the same chip. Similar to its bipolar counterpart, Exar's I^2L semi-custom program also utilizes partially fabricated silicon wafers which are then customized by the application of special mask patterns.

Exar's I^2L Master-Chips utilize bipolar input/output (I/O) interface circuitry on the same chip with the high density I^2L logic arrays. Thus, outwardly the I^2L semi-custom chip looks and performs exactly as a bipolar LSI chip, which can readily interface with TTL level signals. In other words, these gate array Master-Chips combine the high functional density advantages of I^2L technology with the interface and load drive capability of the bipolar circuitry on the same IC. This feature makes it very convenient to retrofit I^2L LSI designs into existing TTL type logic systems.

ACHIEVING HIGH COMPLEXITY

Traditionally, the application of semi-custom technology to complex digital systems has been somewhat limited due to one key factor; in order to be economically feasible, a complex digital LSI circuit must achieve a high functional density on the chip (high gate count per unit of chip area). This requirement is not compatible with the random interconnection concept which is key to the semi-custom or Master-Chip design technique. Exar's approach overcomes this limitation, by making use of the unique layout and interconnection properties of I^2L gates, and by extending the customizing steps to mask layers. In addition to the metal interconnection pattern, Exar can achieve high packing density and still retain the quick turnaround features and low cost of semi-custom.

Exar's I^2L Master-Chips are customized by not one but three mask layers:

1. A custom diffusion pattern to define gate outputs and custom underpasses for interconnection.
2. A custom contact mask which opens contact windows or activates only those devices actually used in the design.
3. A custom metal interconnection mask which interconnects all the activated devices.

FULLY AUTOMATED MASK GENERATION

Exar has developed a fully automated mask generation technique which allows all three custom mask layers used with I^2L Master-Chips to be generated simultaneously from a customer's pencil layout on the Master-Chip worksheet. This unique mask generation technique, and the three-mask customizing method, are the heart of Exar's I^2L semi-custom program. In this manner, one is able to combine low cost, quick turnaround capabilities of semi-custom designs with the high functional density of I^2L technology, and still make very efficient use of the chip area.

WHEN TO USE DIGITAL SEMI-CUSTOM

The key application of I^2L semi-custom design is to replace complex blocks of random logic with a single monolithic chip. An entire digital subsystem comprised of many SSI or MSI chips, or discrete components, can be put on a single I^2L Master-Chip. This can provide significant cost and space savings and greatly improve system reliability. The availability of bipolar input/output interface circuitry on the same chip with the high density I^2L logic makes it very convenient to retrofit I^2L designs into existing TTL logic systems. Therefore, semi-custom I^2L LSI designs provide cost effective solutions for complex custom LSI requirements, even at production volumes as low as a few thousand pieces.

FEATURES OF I^2L TECHNOLOGY

High Functional Density: I^2L logic gates offer a much smaller size than their bipolar counterparts. Thus, a much higher degree of logic complexity or functional density can be achieved on a given IC chip.

Easy to Interconnect: Unique structure and geometry of I^2I gates make them ideal for semi-custom design. An entire array of gates can be easily customized and interconnected using only three masks without sacrificing high functional density.

Bipolar Compatible Processing: I^2L is a direct derivative of conventional bipolar IC technology. Therefore, one can combine bipolar devices on the same chip as I^2L gates. This feature has the following key advantages:

- Input/output section of I^2L chips are bipolar. Thus, they can readily interface with existing logic families or retrofit into existing systems.
- Analog and digital functions can be combined on the same chip. One of Exar's Master-Chips, the XR-400, is specifically designed for such an application.

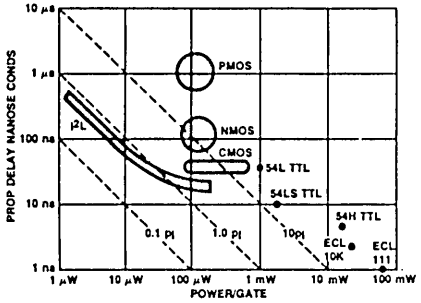
Low Voltage Operation: I^2L gates can operate with supply voltages as low as one volt, and require only a single power supply.

Low Current and Low Power Operation: Depending on speed requirements, I^2L gates can operate with current

levels in the nanoampere range. This feature, along with its low voltage operation makes it ideal for applications in low power, battery operated systems.

Higher Reliability Than MOS: Since I^2L gates have the same basic features as bipolar transistors, they are not subject to electrostatic burn-out problems associated with MOS transistors and do not require special handling precautions.

Wide Operating Temperature: I^2L gates are not seriously affected by leakage currents as are their MOS counterparts. Thus, they can accommodate the full military temperature range.



COMPARISON OF SPEED AND POWER CAPABILITIES OF VARIOUS LOGIC FAMILIES

THE BASIC I^2L GATE

The I^2L logic technology is derived from the basic single input, multiple output inverter circuit shown below. The logic functions are performed in a manner similar to the conventional open-collector logic. The outputs of various gates are interconnected together in a wired-AND configuration. Many sections of the I^2L gate share common semi-conductor regions. For example, the collector of the pnp is the same as the base of the npn, and the emitter of the npn is the same as the base of the pnp. This leads to a very compact device structure which occupies a correspondingly small chip area. As a result, the functional density of I^2L gates is comparable to that of some MOS technologies and is approximately 5 times higher than conventional TTL logic.

LOGIC CONVERSION TO I^2L GATES

Converting conventional logic diagrams from their NAND/NOR gate equivalents to I^2L gates is a simple and straightforward procedure. This information is contained in the I^2L Design Manual, which is available as a part of Exar's I^2L Design Kit. In addition, Exar has developed a large library of I^2L logic subblocks corresponding to popular logic functions, such as decoders, flip-flops and counters, which greatly simplifies this conversion process.

DESIGNING WITH I^2L MASTER-CHIPS

Exar currently has four I^2L Master-Chips in production. These are the XR-200, XR-300, XR-400 and the XR-500 Master-Chips. The XR-200, XR-300 and the XR-500 are designed for digital systems. The XR-400 Master-Chip is intended for systems requiring both analog and digital functions.

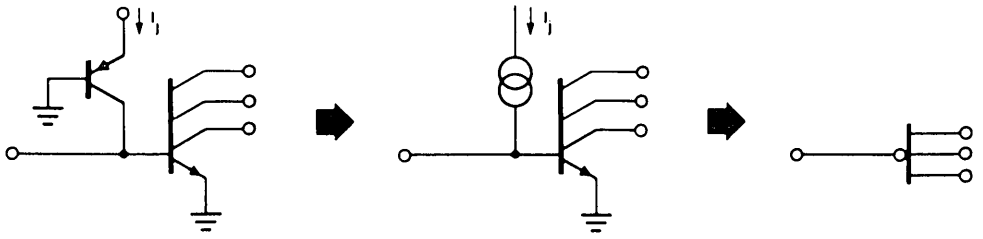
All four of these Master-Chips are fabricated with the same manufacturing process. They differ only in their architecture and in the number of components. All of these chips are especially designed for Exar's unique three-mask customization process using fully automated mask generation techniques.

XR-200, XR-300 and XR-500 MASTER-CHIPS

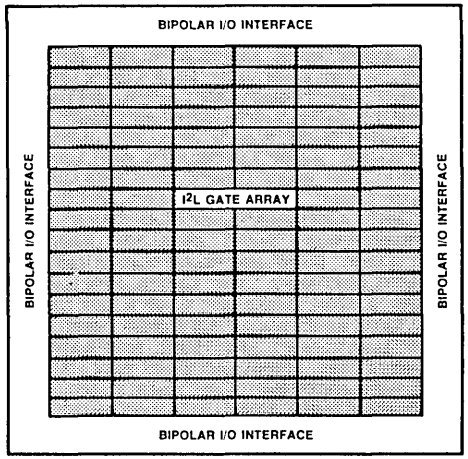
These Master-Chips are primarily designed for applications requiring only digital signal processing. They contain a large number of multiple output I^2L gates along with Schottky bipolar input/output buffers. Except for the difference in size, all three chips have the same architecture shown below. The I^2L gates are arranged in array form at the center of the chip and the input/output buffers are located along the periphery of the chip. The bipolar I/O sections of the chips contain two identical sets of resistor arrays located at opposite ends of the chip which are used for biasing the injectors of the I^2L gates. The XR-200 contains 192 five-output I^2L gates and 24 I/O buffers. The XR-300 contains 288 five-output I^2L gates and 28 I/O buffers. The XR-500 contains 520 five-output I^2L gates and 40 I/O buffers. A detailed description of the bipolar input/output interface circuitry is given further on in the text.

9

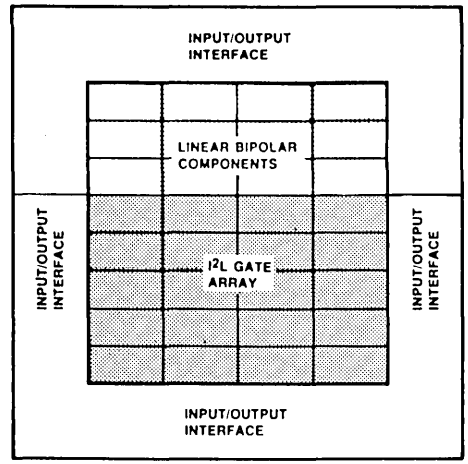
THE BASIC I^2L GATE



(a) Actual Gate (b) Equivalent Circuit (c) Logic Symbol



BASIC LAYOUT OF XR-200, XR-300 AND XR-500 MASTER CHIPS



BASIC LAYOUT OF XR-400 MASTER CHIP

XR-400 MASTER-CHIP

The XR-400 Master-Chip is designed primarily for applications requiring the combination of analog and digital functions on the same chip. Thus, it is made up of both a linear and a digital section. The digital section of the chip has the same basic architecture as the XR-300. It contains 256 five-output I^2L gates and 18 Schottky bipolar I/O interface sections. The linear section of the chip is made up of an array of npn and pnp transistors and resistors and is very similar to Exar's bipolar Master-Chips.

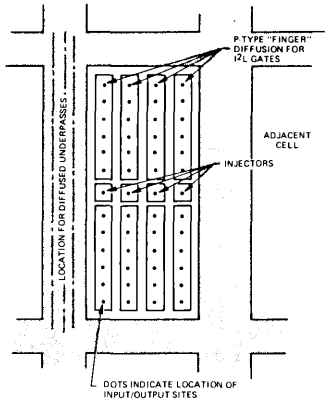
COMPONENT UTILIZATION

The unique three-mask customizing technique used in Exar's I^2L Master-Chips makes them very efficient for both ease of logic layout and component utilization. One of the three customizing mask steps is a custom diffusion step which allows the placement of low resistance crossunders, or underpasses, selectively on the chip. This technique provides the designer with virtually two layers of interconnection on the chip and, thus, greatly simplifies the logic layout and improves the component utilization efficiency. Normally, in the case of random combinational logic, one can easily utilize 60% to 80% of the total gates available on a given I^2L Master-Chip. In the case of sequential and repetitive logic circuits, the gate utilization is normally as high as 80% to 100%.

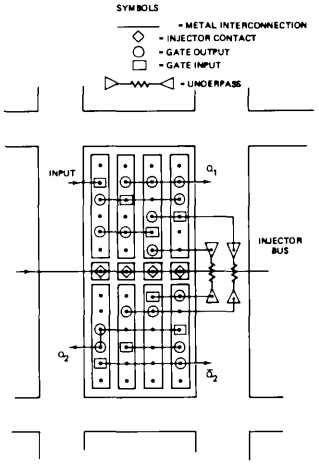
In the case of the XR-400 Master-Chip, which combines analog circuit components and digital gates on the same chip, the three-mask customizing technique is applicable to the digital section, while the analog section of the chip is customized with one mask in the same way as the linear Master-Chips.

Components on XR I^2L Master-Chips

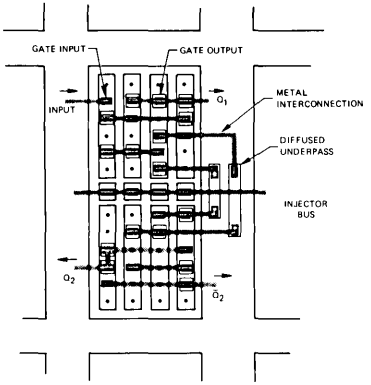
Component Type	Quantity			
	XR-200	XR-300	XR-400	XR-500
5-Output I^2L Gates	192	288	256	520
Schottky-Bipolar I/O Interfaces	24	28	18	40
Max Operating Voltage	7V	7V	7V	7V
NPN Transistors	0	0	45	0
4-Collector PNP Transistors	0	0	12	0
Diffused Resistors 700Ω 2.5 K 5 K	 0 0 0	 0 0 0	 200 116 20	 0 0 0
Bonding Pads	30	34	40	42
Chip Size (mils)	98 x 119	106 x 144	119 x 149	122 x 185



BASIC 8 GATE CELL PRIOR TO CUSTOMIZATION



SAMPLE PENCIL LAYOUT ON MASTER CHIP WORKSHEET



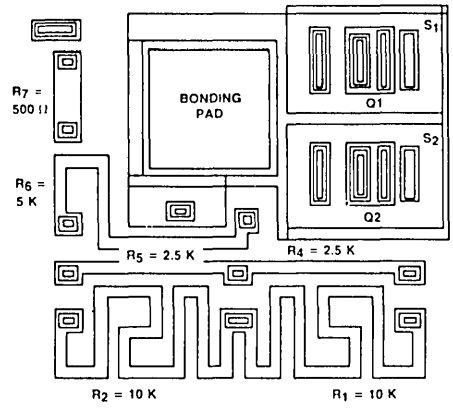
SAMPLE LAYOUT OF 8 GATE CELL AFTER CUSTOMIZING WITH N+ COLLECTOR DIFFUSION, CONTACT MASK AND METAL INTERCONNECTION PATTERN

THE I^2L GATE ARRAY SECTION

This section of the I^2L Master-Chip is made up of logic cells which contain a number of multiple output I^2L inverters grouped together. The figure below shows a typical layout of such a cell made up of eight multiple output inverters which share a common set of four injectors. The basic gate cells forming the I^2L gate array are made up of p-type injectors and p-type gate fingers which serve as the base regions of the I^2L gates. The six dots on each gate area indicate the possible locations (or sites) for gate inputs or outputs. The particular use of these sites as an input or output is determined by two custom masks. An n-type collector diffusion mask defines the locations of outputs and a custom contact mask opens the appropriate input and output contacts. Finally, a third custom mask is applied to form the metal interconnections between the gates and the gate cells. The custom n-type diffusion step, which determines the locations of gate outputs, is also used for forming low resistivity underpasses between the gate cells. The area between each of the gate cells can accommodate two or three parallel underpasses in the horizontal or vertical direction. Since the n-type diffusion which forms these underpasses is a part of the customizing step, the location and length of each underpass can be chosen to fit a given interconnection requirement. This method provides the designer with virtually all of the advantages and capabilities of multilayer interconnection paths on the surface of the chip and allows approximately 80% of the gates on the chip to be utilized in a typical logic layout.

The custom logic interconnections can be easily laid out in pencil on a layout sheet by simply interconnecting the desired gate sites with a pencil line and appropriately defining the function of the site as an input, output, injector contact or an underpass. The function of each of the potential sites is defined by simply drawing an appropriate symbol on it, such as a circle for an output and a square for an input, as defined in the example below.

9

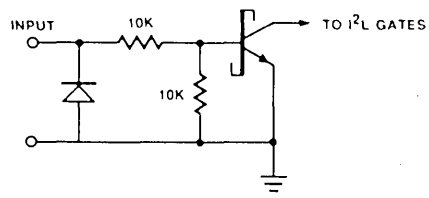


A TYPICAL SCHOTTKY-BIPOLAR INPUT/OUTPUT INTERFACE CELL

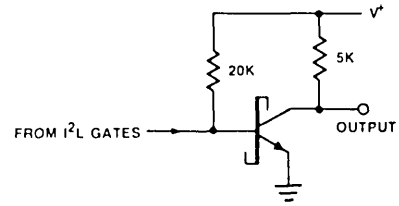
BIPOLAR INPUT/OUTPUT INTERFACE SECTION

The bipolar input/output interface sections of the I^2L Master-Chips are located along the periphery of the chips. The component locations in a typical I/O cell are shown in the adjacent figure. Each I/O cell is designed to be either an input or an output interface depending on the choice of the metal interconnection pattern applied to the cell. Furthermore, two adjacent cells can be combined together to provide a three-state type output buffer. Some of the basic input and output circuit configurations available from the I/O interface are shown below. In the case of a three-state output configuration, one would also utilize several gates from the I^2L logic section to perform the necessary gating functions.

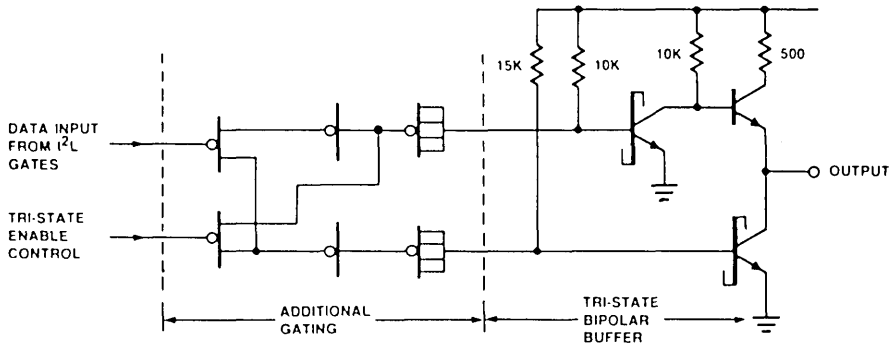
Each input/output interface cell contains one bonding pad, several resistors of varying values, a clamp diode to substrate and two npn transistors with optional Schottky diode clamps. Each npn transistor is capable of sinking 5 mA of current with Schottky diode clamps and 10 mA of current without, at a saturation voltage of $\leq$ 0.5V. The breakdown voltage of the bipolar I/O section is 7V.



(a) Input Interface Circuit



(b) Output Interface Circuit



(c) Tri-State Output Interface Circuit

TYPICAL BIPOLAR INPUT/OUTPUT INTERFACE CIRCUITS AVAILABLE FROM I/O INTERFACE CELL

EXAR

Section 10 – User Specific Digital ICs – Full Custom/Semi-Custom

SEMI-CUSTOM SOLUTIONS (Gate Arrays)

Designing USICs using semi-custom approach is a well-known way to achieving cost-effective product with a quick turn-around. A CMOS semi-custom solution for USICs can be approached in two ways.

In one case, a customer may already have a working system on which it is necessary, for example, to reduce the manufacturing costs by incorporating a CMOS gate-array to simplify a complex printed circuit board. The task in this case is to determine what portion, if not all, of this PC board can be incorporated into an array. EXAR offers a very wide range of arrays to accomplish this.

The partitioning of the system and the choice of which array to use must be carefully considered with cost, packaging, versatility and testability in mind. EXAR's custom-engineering department will be happy to assist a customer in his selection, or perform a design review of the system at no cost and suggest array and partitioning alternatives. This design review will include a quotation for the development charges and production pricing of the array, as well as an approximation of the development time that will be required to build the prototypes.

In the second case, a design engineer may be in the process of designing a completely new system. In this case, the system can be designed in such a way that it can be easily partitioned into one or more arrays. Once again, EXAR's custom-engineering department will be happy to provide assistance in selecting the appropriate array along with price and delivery information. EXAR plans to offer its soft macro library in both a PC-like environment and on popular workstations so that the schematic-capture can be performed electronically, thereby eliminating chances of an error and expediting the development cycle. Dial-up services will be available to help perform logic and circuit analysis using our powerful CAD/CAE tools in-house.

Also, if a customer so desires, the breadboards can be built using SSI and MSI packages from one of the popular logic families such as 74LXX, 74CXX or 4XXX. These logic families are recommmended for breadboarding due to their standard nature as well as their universal availability. EXAR custom-engineering will, once again, be happy to assist in translating these into EXAR's soft-macro library.

A typical semi-custom development flow is shown in the figure 1. Listed below are the steps to be performed at each stage.

System Design	Logic Design	Logic Simulation	Layout	Integration
☐ Conceptualization	☐ System Partitioning	☐ Schematic Capture	☐ Auto-Place	☐ PG Tape
☐ System-Block Diagram	☐ Logic Design	☐ Logic Simulation	☐ Auto-Route	☐ Working Plates
	☐ Objective Specs	☐ Fault Simulator	☐ Timing Verification	☐ Wafer Processing
		☐ Netlist Generation	☐ DRC/ERC/LVS	☐ Packaging
				☐ Testing

Figure 1. Semi-Custom Development Flow

ADVANTAGES OF A SEMI-CUSTOM SOLUTION:

Lower Product Cost: With greater design integration, product costs are reduced.

Reduced Chip Count: Standard SSI and MSI parts are incorporated into a single chip, significantly reducing the chip count.

Improved Reliability: Fewer pins and solder joints improve the reliability.

Improved Speed: Reduced junction and node capacitances allows circuits to run at higher clock speeds.

Reduced Power Consumption: Reduced capacitive loads and CMOS technology also means the power consumption is significantly lower.

Smaller Products: Reduced chip count also means less parts and less board space. The result is a physically smaller product which offers the same solution.

Design Integrity: A User Specific IC provides protection against improper and unauthorized copying of the final product.

30,000 SERIES

The XR-30,000 series of silicon-gate CMOS gate-arrays has been developed for high speed digital applications, with clock speeds as high as 25 MHz.

The series is composed of six different arrays ranging in gate-count from 156 to 3025 gates. The number of I/O pins on these arrays range from 22 to 98 and these are all tri-statable.

The 30,000 series are implemented using a state-of-the-art 3 micron Si-gate CMOS, p-well processing technology. Special features like dual metal layers allow improved routability and impressive performance gains in both functionality and percentage utilization of the array.

The arrays use a set of common base layers, so the customization begins with the first contact and metal mask layers. This allows stocking of the wafers, finished until just before the first contact mask. Implementation is geared to provide a short turn-around time.

XR-30,000 SERIES

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$-0.3 \sim 6.5$	V
Input Voltage	V_{in}	$-0.3 \sim V_{DD} + 0.3$	V
Output Voltage	V_{out}	$-0.3 \sim V_{DD} + 0.3$	V
Storage Temperature	T_{stg}	$-55 \sim 150$	°C

OPERATING RANGE

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	5 ± 0.25	V
Input Voltage	V_{in}	$0 \sim V_{DD}$	V
Output Voltage	V_{out}	$0 \sim V_{DD}$	V
Operating Temperature	T_{opr}	$0 \sim 75$	°C

I/O CHARACTERISTICS: V_{DD} = 5V; T_A = 25°C

ITEM	SYMBOL	MIN	RATING TYP	MAX	UNIT	CONDITION
Input Voltage	V_{IL}			0.8	V	
	VIH	2.0			V	
Output Voltage	V_{OL}			0.8	V	I_{OL} = 2 mA
	V_{OH}	2.4			V	I_{OH} = 0.4 mA*

AC CHARACTERISTICS: (T_A = 25°C)

ITEM	SYMBOL		RATING TYP		UNIT	CONDITION
Average Propagation Delay	t_{pd}		3.0		ns	Inverter with fanout = 2; V_{DD} + 5V
Toggle Frequency	f_t		25		MHz	V_{DD} = 5V

ARRAY NAME	GATE COUNT*	TOTAL I/O	TRISTABLE	BONDING	MAX OPERATING	TOGGLE	INTERNAL
30015	156	22	22	24			
30030	288	30	30	32			
30045	460	38	38	40	5V	35 MHz	<3 nS
30080	793	50	50	52			
30155	1548	70	70	72			
30300	3025	98	98	100			

* 2 input NAND equivalent

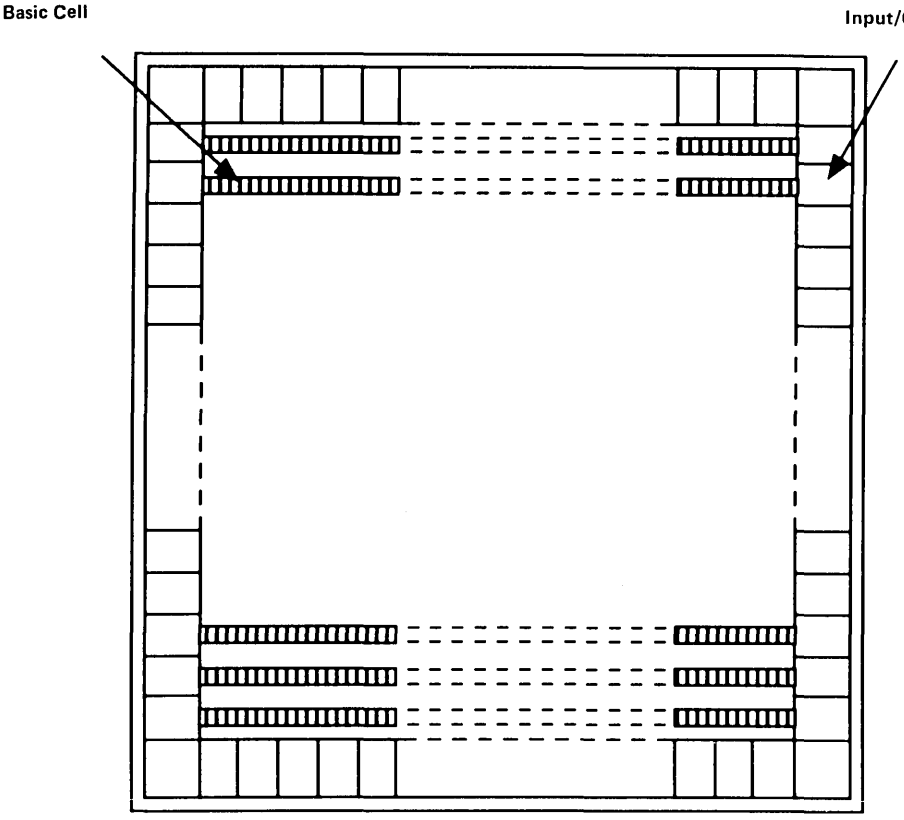


Figure 2. Chip Layout

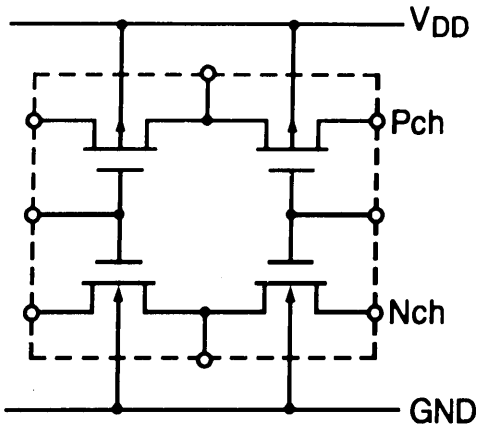


Figure 3. Basic 2-input Gate Cell

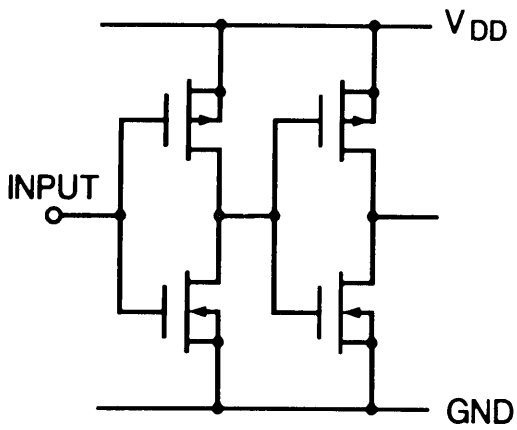


Figure 4. Input Buffer

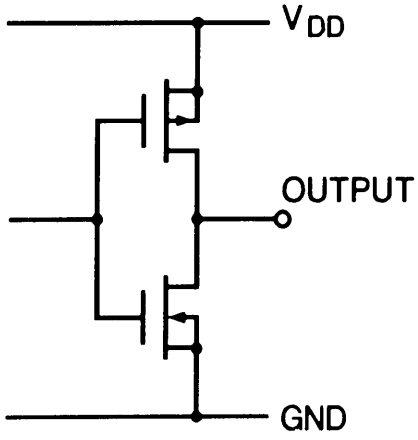


Figure 5. Output Buffer

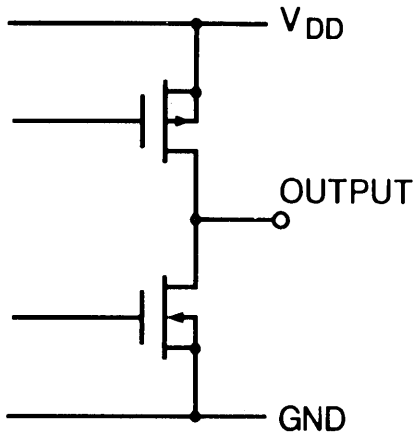


Figure 6. Tristate Output Buffer

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*Input and output buffers have other possible configurations also.

XR-30,000 SOFT-MACROS LIST

FUNCTION

Single Inverter
Double Inverter
Single Buffer
Double Buffer
AND Buffer
OR Buffer

2 Input NOR Gate
3 Input NOR Gate
4 Input NOR Gate
6 Input NOR Gate
8 Input NOR Gate
9 Input NOR Gate
12 Input NOR Gate
16 Input NOR Gate

2 Input NAND Gate
3 Input NAND Gate
4 Input NAND Gate
6 Input NAND Gate
8 Input NAND Gate
9 Input NAND Gate
12 Input NAND Gate
16 Input NAND Gate

2-AND-NOR
2-OR-NAND
2-2-AND-NOR
2-2-OR-NAND

Exclusive OR Gate
Exclusive OR Buffer
Exclusive NOR Gate
Exclusive NOR Buffer

RS Latch (NAND)
RS Latch (NOR)
R1R2S1S2 Latch (NAND)
R1R2S1S2 Latch (NOR)

D Latch
D Latch with Reset
D Latch with Set and Reset
D Flip-Flop
D Flip-Flop with Reset
D Flip-Flop with Set and Reset

Non-Inverting Input Buffer
Inverting TTL Compatible Input Buffer
Input Protection
Inverting Input Buffer
Schmitt-Trigger Non-Inverting Input Buffer
Schmitt-Trigger Non-Inverting Input Buffer
With Pull-Up Resistance

Inverting Output Buffer
Non-Inverting Output Buffer
Tri-State Output Buffer
Inverting Open Drain Output Buffer
NAND Output Buffer

Bidirectional Tri-State I/O Buffer
Unused I/O Cell
Inverting Bidirectional Buffer
Bidirectional Buffer with Tri-State Output

Schmitt-Trigger
2 to 1 Multiplexer
Open Drain N Channel Transistor
Open Drain P Channel Transistor

CM SERIES

EXAR's CM series of digital gate-arrays is composed of four members: CMA, CMB, CMC and CMD – these range in size from 140 to 460 gates.

Each of the CM series array is completely prefabricated just like the 30,000 series, except for the final fabrication step of device interconnection.

The CM series is implemented using an 8 micron metal-gate CMOS, p-well processing technology. Implementation is geared to provide a short turn-around time.

As compared to 30,000 series, CM series can operate over a much wide supply range, V_{DD} = 3-15V. The clock speeds though, because of the larger geometries, are slower than the XR-30,000 series.

XR-CM SERIES

ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	−0.3 to +15.0	V
Input Voltage	V_{in}	−0.3 to V_{DD} + 0.5 V_{dc}	V
Output Voltage	V_{out}	−0.3 to V_{DD} + 0.5 V_{dc}	V
Storage Temperature	T_{stg}	−55 ~ 150	°C

OPERATING RANGE

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	3 – 15	V
Input Voltage	V_{in}	0 – V_{DD}	V
Output Voltage	V_{out}	0 – V_{DD}	V
Operating Temperature	T_{opr}	0 ~ 75	°C

I/O CHARACTERISTICS: V_{DD} = 5V; T_A = 25°C

ITEM	SYMBOL	MIN	RATING TYP	MAX	UNIT	CONDITION
Output Voltage (Low Level)	V_{OL}		0	0.1	V	V_{DD} = 5.0V
			0	0.1	V	V_{DD} = 10.0V
			0	0.1	V	V_{DD} = 15.0V
Output Voltage (High Level)	V_{OH}	4.95	5.0		V	V_{DD} = 5.0V
		9.95	10.0		V	V_{DD} = 10.0V
		14.95	15.0		V	V_{DD} = 15.0V

AC CHARACTERISTICS: (T_A = 25°C)

ITEM	SYMBOL		RATING TYP		UNIT	CONDITION
Average Propagation Delay (Inverter with fanout = 2)	t_{pd}		21		ns	V_{DD} = 5.0
			11		ns	V_{DD} = 10.0
			8		ns	V_{DD} = 15.0
Toggle Frequency	f_t		2.5		MHz	V_{DD} = 5.0
			5.0		Mhz	V_{DD} = 10.0
			8.0		MHz	V_{DD} = 15.0

ARRAY NAME	GATE COUNT*	TOTAL I/O	TRISTABLE I/O	BONDING PADS
CMA	140	29	15	32
CMB	202	34	16	38
CMC	270	40	22	44
CMD	416	46	30	50

* 2 input NAND equivalent

FULL-CUSTOM SOLUTIONS (Standard Cells)

Full-custom solutions offer the ultimate in design flexibility and cost reductions. This approach allows single-chip integrations of diverse function types that cannot be realized using any other approach. In addition, the die-size and hence the unit-cost for the final product is considerably lower than a semi-custom design. However, since the development cost and lead times are longer, this approach is better suited for large production quantities or designs that cannot be realized using the semi-custom approach.

A typical full-custom development flow is shown in Figure 1. Listed below are the steps to be performed at each stage. It should be noted that in full-custom developments, working plates (masks) must be generated for all layers, unlike semi-custom, where only the interconnect layers need to be generated.

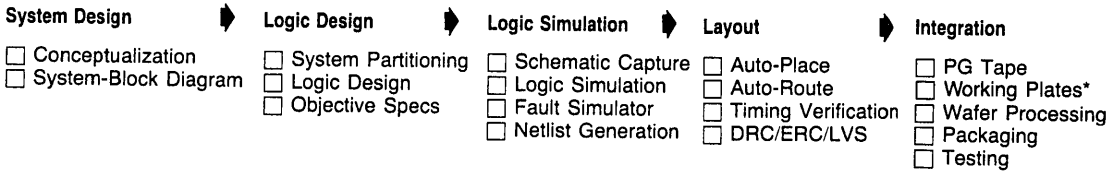

Figure 1. Full-Custom Development Flow

*(All Levels)

ADVANTAGES OF FULL-CUSTOM SOLUTION:
(Standard Cell Approach)

Flexibility in Design: Layout customized from bottom layer up.

Improved Turnaround: Predefined cells and auto placement/routing.

Higher Success Rate: Sophisticated CAD software eliminates missing or incorrect connection. Guaranteed functionality of the predefined cells.

Lower Product Cost: For higher production quantities the product cost in even lower than the gate arrays, this in spite of the higher NRE charges.

Macro Cells: The ultimate in the flexibility and integration is the ability to incorporate proven macro functions in the standard cells.

A3000 STANDARD CELLS

A3000 STANDARD-CELLS

EXAR has developed an extensive library of full-characterized standard cells. Standard cell technique allows the design of an entire integrated circuit from base layer up, similar to a hand-crafted full-custom development without suffering from some of its severe disadvantages.

The design can be fully simulated on EXAR's in-house VAX system. Placement, routing and timing verification is performed using state-of-the-art CAD/CAE tools.

The dual-metal layer capability gives a significant performance advantage by reducing RC delays on signal lines. In addition, smaller die-size also gives the customer a reduced unit cost.

The standard cell library is undergoing continual expansion and upgrade. Further enhancements under development include analog functions, a micro-controller macro-cell, EEPROM cells and many additional digital functions.

A3000 SERIES

ABSOLUTE MAXIMUM RATINGS = T_A = 25°C

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	$-0.3 \sim 6.5$	V
Input Voltage	V_{in}	$-0.3 \sim V_{DD} + 0.3$	V
Output Voltage	V_{out}	$-0.3 \sim V_{DD} + 0.3$	V
Operating Temperature	T_{opr}	$-20 \sim 75$	°C
Storage Temperature	T_{stg}	$-55 \sim 150$	°C

OPERATING RANGE

ITEM	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	5 ± 0.25	V
Input Voltage	V_{in}	$0 \sim V_{DD}$	V
Output Voltage	V_{out}	$0 \sim V_{DD}$	V
Operating Temperature	T_{opr}	$0 \sim 75$	°C

I/O CHARACTERISTICS: V_{DD} = 5V; T_A = 25°C

ITEM	SYMBOL	MIN	RATING TYP	MAX	UNIT	CONDITION
Input Voltage	V_{IL}			0.8	V	
	VIH	2.0			V	
Output Voltage	V_{OL}			0.8	V	I_{OL} = 2 mA
	V_{OH}	2.4			V	I_{OH} = 0.4 mA*

1. 2 Input AND – 2 Input OR – Invert
2. 2 Input AND
3. 3 Input AND
4. 4 Input AND
5. 5 Input AND
6. Bidirectional Buffer with Pad
7. Buffered Enable Transmission Gate
8. Schmitt-Trigger Buffer
9. Tri-State Buffer
10. Tri-State Buffer with Inverted Enable
11. Clock Buffer
12. Clock with Reset Flip-Flop
13. D Flip-Flop with Reset
14. D Flip-Flop with Reset and Set
15. D Flip-Flop with Set
16. D Flip-Flop
17. 2 Input Exclusive OR
18. 2 Input Exclusive NOR
19. Input Buffer, Input Normally Low
20. Schmitt-Trigger Input Buffer
21. Input Buffer with Pad
22. Tri-State Inverter
23. Tri-State Inverter with Inverted Enable
24. Inverter
25. Inverting Clock Buffer
26. Inverted Enable Transmission Gate
27. Latch
28. Latch with Reset
29. Latch with Reset and Set
30. Left End Cell
31. 2 Input MUX
32. 2 Input NAND, One Input Inverted
33. NAND Set-Reset Latch
34. 2 Input NAND
35. 3 Input NAND
36. 4 Input NAND
37. 5 Input NAND
38. 2 Input NOR, One Input Inverted
39. NOR Set-Reset Latch
40. 2 Input NOR
41. 3 Input NOR
42. 4 Input NOR
43. Output Buffer with Pad
44. Output Buffer with Test Pad
45. Output Buffer with Test Pad
46. 2 Input AND – 2 Input OR – Invert
47. 2 Input OR
48. 3 Input OR
49. 4 Input OR
50. Right End Cell
51. T Flip-Flop with Reset
52. Vertical Route Through
53. V_{DD} Pad
54. V_{SS} Pad
55. Op Amp

FULL-CUSTOM CONVERSIONS (Two Step Approach)

Recognizing the risk, cost and longer turn-around times involved in a full-custom development, EXAR also offers full-custom conversion to its customers.

Using this approach, the design is first implemented on one of EXAR's numerous arrays to bring the product to market in a short time-frame and qualify for production. In addition, any design iterations, if required, can be implemented at a low cost.

The second step then consists of a straightforward full-custom conversion to minimize the chip size and unit cost when the device is in full production. This ensures a risk free and smooth transition to shipping cost-effective, high volume products.

Full-custom conversion thus is a two-step approach that provides the best of both worlds: quick turn-around time (with minimum risk) of gate-arrays and the silicon efficiency of full-custom solution (standard-cell approach) with lower unit cost.

EXAR

Section 11 – Application Notes

Applications Guide

Exar's line of monolithic IC products cover a wide range of applications. This *Applications Guide* is intended as a brief selection guide for the IC user, to assist him in finding the Exar product most suited to his application.

The application categories, or classes, are listed in alphabetical order, dictionary style, to allow the user to locate the product he needs at a glance. In certain applications, *two* of Exar's products used in combination may be necessary to perform the complete function. In such a case, these products are grouped together as a pair. For example, to make a complete FSK modem may require the XR-2206 Modulator and the XR-2211 Decoder. Thus, in the Applications Guide shown below, both of these products will be grouped under the Modem category as XR-2206/XR-2211.

In many of the applications, more than one product type is recommended. In such cases, the user can choose the device best suited to his specific application by either consulting with Exar's Applications department, or by reviewing the electrical specifications of the individual devices involved.

***ADVANCED INFORMATION**

A

Active Filters	XR-084, XR-094, XR-096, XR-346, XR-3403, XR-4202
Acoustical Couplers (See Modems)	XR-2206, XR-2207, XR-2211
A/D Conversion (Pulse Counting Type)	XR-2240
Amplitude Detection	
Phase-Locked AM Detection	XR-215/XR-2228, XR-2212/XR-2228
Synchronous AM Detection	XR-S200, XR-2208, XR-2228
Amplitude Level Detection	XR-2276, XR-2277, XR-2278, XR-2279
Amplitude Modulated Oscillator	XR-205, XR-2206
Crystal Controlled AM Oscillator	XR-S200, XR-205
Amplitude Modulation	XR-2206, XR-2208, XR-2228, XR-13600
Analog Computation	
Analog Multiplication/Division	XR-2208, XR-2228
Analog Square/Square-Root Operation	XR-2208
Analog-To-Frequency Conversion	XR-2209, XR-4151
Analog Sample-Hold	XR-13600/XR-082
Analog Semi-Custom Design (Master Chips)	XR-A100, XR-B100, XR-C100, XR-D100, XR-F100, XR-G100, XR-X100
Appliance Timing	XR-555, XR-556, XR-558, XR-559, XR-2240, XR-2242, XR-2243
Audio Amplifier/Preamp	XR-5532, XR-5534
Audio Level Detector	XR-2276, XR-2279
Automatic Gain Control (AGC)	XR-2208, XR-2216, XR-2228, XR-13600

B

Bar-Graph Display	XR-2276, XR-2277, XR-2278, XR-2279
Battery Charger Timing	XR-2242, XR-2243
Battery Operated Instruments (Low-Power)	
Timing	XR-L555, XR-L556, XR-2243
Tone Detection	XR-L567
Bit-Pattern Generation	XR-2240

C

Carrier Detection (See AM and Tone Detection)	
High-Frequency (>1 MHz)	XR-215/XR-2228
Low-Frequency (<1 MHz)	XR-567A, XR-2211, XR-L567
Low-Power	XR-L567
Carrier-Tone Transceiver	XR-2567
Clock Generation (See Oscillators)	
Low-Frequency (<1 MHz)	XR-555, XR-2209, XR-2242
Low-Power	XR-L555, XR-L556, XR-2243
High-Frequency	XR-205
Phase Locked	XR-215, XR-2212, XR-2213
Clock Extraction	
Phase Locked	XR-210, XR-215, XR-2212, XR-2213
PCM Signal Clock	XR-C262, XR-C277
Clock Pattern Generation	XR-2240
Clock Synchronization	
High-Frequency (>1 MHz)	XR-210, XR-215
Low-Frequency (<1 MHz)	XR-2212, XR-2213
Commandor (Speech/Data)	XR-2216
Current-to-Frequency Converter	XR-2206, XR-2207, XR-2209
Current Drive	XR-2247, XR-2247A

D

Darlington Arrays (High-Current, High-Voltage)	XR-2200, XR-2201, XR-2202, XR-2203, XR-2204, XR-2001, XR-2002, XR-2003, XR-2004, XR-2011, XR-2012, XR-2013, XR-2014
Data Synchronization	
High-Frequency (>1 MHz)	XR-210, XR-215
Low-Frequency (<1 MHz)	XR-2212, XR-2213
DC/DC Converter (See Switching Regulators)	XR-1524, XR-2524, XR-3524, XR-1525A, XR-1527A, XR-2525A, XR-3525A, XR-2527A, XR-3527A

E

F

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W

Stable FSK Modems featuring the XR-2207, XR-2206 and XR-2211

INTRODUCTION

Frequency-shift keying (FSK) is the most commonly used method for transmitting digital data over telecommunications links. In order to use FSK, a modulator/demodulator (modem) is needed to translate digital 1's and 0's into their respective frequencies and back again. This application note describes the design of a modem using state-of-the-art Exar devices specifically intended for modem application.

The devices featured in this application note are the XR-2206 and XR-2207 FSK Modulators, and the XR-2211 FSK demodulator with carrier detect capability. Because of the superior frequency stability of these devices (typically 20 ppm/°C), a properly designed modem will be virtually free of the temperature and voltage-dependent drift problems associated with many other designs. In addition, the demodulator performance is independent of incoming signal strength variation over a 60 dB dynamic range. Because bias voltages are generated internally, the external parts count is much lower than in most other designs. The modem designs shown in this application note can be used with mark and space frequencies, anywhere from several Hz to 100 kHz.

PRINCIPLES OF OPERATION

THE XR-2206 FSK MODULATOR

FEATURES

Typically 20 ppm/°C Temperature Stability
Choice of 0.5% THD Sine Wave, Triangle, or Square Wave Output
Phase-Continuous FSK Output
Inputs are TTL and CMOS Compatible
Low-Power Supply Sensitivity (0.01%)

Low-Power Supply Sensitivity (0.01%/V)
Split or Single Supply Operation
Low External Parts Count

The XR-2206 is ideal for FSK applications requiring the spectral purity of a sinusoidal output waveform. It offers TTL and CMOS compatibility, excellent frequency stability, and ease of application. The XR-2206 can typically provide a 3-volt p-p sine wave output. Total harmonic distortion can be trimmed to 0.5%. If left untrimmed, it is approximately 2.5%.

The circuit connection for the XR-2206 FSK Generator is shown in Figure 1. The data input is applied to Pin 9. A high-level signal selects the frequency ($1/R_6C_3$) Hz; a low level signal selects the frequency ($1/R_7C_3$) Hz, (resistors in ohms and capacitors in farads). For optimum stability, R_6 and R_7 should be within the range of 10 kΩ to 100 kΩ. The voltage applied to Pin 9 should be selected to fall between ground and V+.

Note: Over and under voltage may damage the device.

Potentiometers, R_8 and R_9, should be adjusted for minimum total harmonic distortion. In applications where minimal distortion is unnecessary, Pins 15 and 16 may be left open-circuited and R_8 may be replaced by a fixed 200Ω resistor.

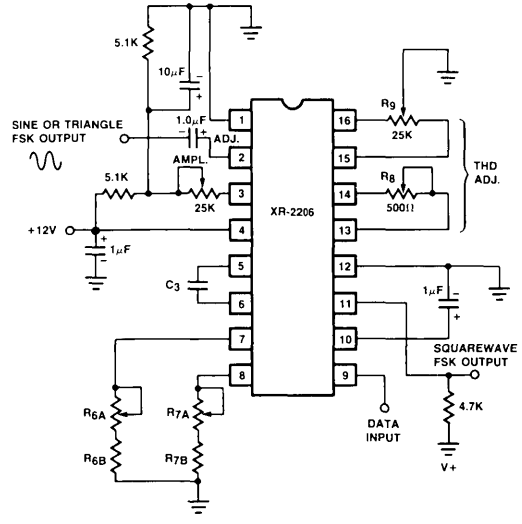


Figure 1. The XR-2206 Sinusoidal FSK Generator.

In applications where a triangular output waveform is satisfactory, Pins 13 through 16 may be left open-circuited.

The output impedance at Pin 2 is about 600Ω, with ac coupling normally being used.

AN-01

THE XR-2207 FSK MODULATOR

FEATURES

Typically 20 ppm/°C Temperature Stability
Phase-Continuous FSK Output
Provides Both Triangle and Square Wave Outputs
Operates Single-Channel or Two-Channel Multiplex
Inputs are TTL and CMOS Compatible
Split- or Single-Power Supply Operation
Low-Power Supply Sensitivity (0.15%/V)
Low External Parts Count

The XR-2207 is a stable FSK generator which is designed for those applications where only a triangle or square wave output is required. It is capable of either single-channel or two-channel multiplex operation, and can be used easily with either split- or single-power supplies.

Figure 2 shows the XR-2207 using a single-supply and Figure 3 shows split-supply operation. When used as an FSK modulator, Pin 8 and 9 provide the digital inputs. When the 2207 is used with a split-supply, the threshold at these pins is approximately +2 volts, which is a level that is compatible with both TTL and CMOS logic forms. When used with a single-supply, the threshold is near mid-supply and is CMOS compatible. Table 1 shows how to select the timing resistors, R_1 through R_4, to determine the output frequency based on the logic levels applied to Pin 8 and 9. For optimum stability, the values of R_1 and R_3 should be selected to fall between 10 kΩ and 100 kΩ.

With Pin 8 grounded, Pin 9 serves as the data input. A high-level signal applied to Pin 8 will disable the oscillator. When used in this manner, Pin 8 of the XR-2207 serves as the channel select input. For two-channel multiplex operation, Pin 4 and 5 should be connected as shown by the dotted lines. (For single channel operation, Pin 4 and 5 should be left open-circuited.)

The XR-2207 provides two outputs: a square wave at Pin 13 and a triangle wave at Pin 14. (For safe operation, current into Pin 13 should be limited to 20 mA.) When used with a split-supply, the triangle wave peak-to-peak amplitude is equal to V^- and the dc level is near ground. Direct coupling is usually used. With a single-supply, the peak-to-peak amplitude is approximately equal to one-half/V^+, the dc level is approximately at mid-supply, and ac coupling is usually necessary. In either case, the output impedance is typically 10Ω and is internally protected against short circuits.

The square wave output has an npn open-collector configuration. When connected as shown in Figure 2 and 3, this output voltage will swing between V^+ and the voltage at Pin 12.

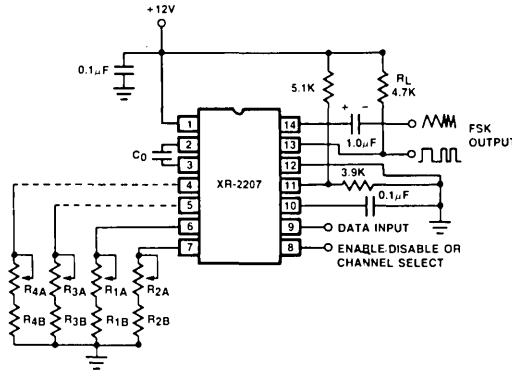


Figure 2. The XR-2207 FSK Modulator Single-Supply Operation.

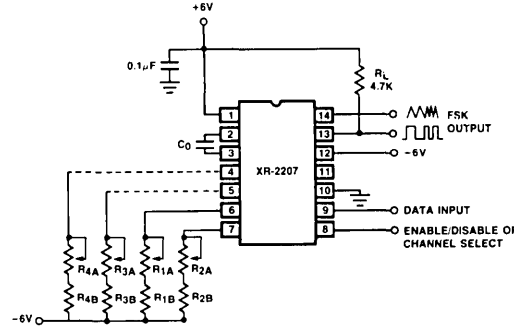


Figure 3. The XR-2207 FSK Modulator Split-Supply Operation.

Table 1.
XR-2207 FSK Input Control Logic

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pins 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pin 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

Units: Resistors — Ohms; Capacitors — Farads; Frequency — Hz

The XR-2211 FSK DEMODULATOR

FEATURES

Typically 20 ppm/°C Temperature Stability
Simultaneous FSK and Carrier-Detect Output
Outputs are TTL and CMOS Compatible
Wide Dynamic Range (2 mV to 3V rms)
Split or Single Supply Operation
Low-Power Supply Sensitivity (0.05%/V)
Low External Parts Count

The XR-2211 is an FSK demodulator which operates on the phase-locked loop principle. Its performance is virtually independent of input signal strength variations, over the range of 2 mV to 3V rms.

Figure 4 shows the circuit connection for the XR-2211. The center frequency is determined by $f_0 = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. Calculation for f_0 should fall mid-way between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain lock with a swept input signal. This range is determined by the formula: $\Delta f = (R_4 f_0/R_5)$ Hz. Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, choose an R_4 between 10 kΩ and 100 kΩ.

The capture range ($\pm\Delta f_C$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop filter time constant. In most modem applications, Δf_C = (80%—99%) Δf.

The loop-damping factor (ζ) determines the amount of overshoot, undershoot, or ringing present in the phase-locked loop's response to a step change in frequency. it is determined by $\zeta = 1/4\sqrt{C_1/C_2}$. For most modem applications, choose $\zeta \approx 1/2$.

The FSK output filter time constant (τ_F) removes chatter from the FSK output. The formula is: $\tau_F = R_F C_F$. Normally calculate τ_F to be approximately equal to [0.3/(baud rate)] seconds.

The lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510 kΩ, the minimum value of C_D can be determined by: $C_D(\mu f) \approx$ 16/capture range in Hz.

Note: Excessive values of C_D will unnecessarily slow the lock-detect response time.

The XR-2211 has three npn open-collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, Pin 5 is the Q lock-detect output which goes low when a carrier is detected, and Pin 6 is the Q lock-detect output which goes high when lock is detected. If Pin 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied, and will be LOW when no carrier is present.

If the lock-detect feature is not required, Pins 3, 5 and 6 may be left open-circuited.

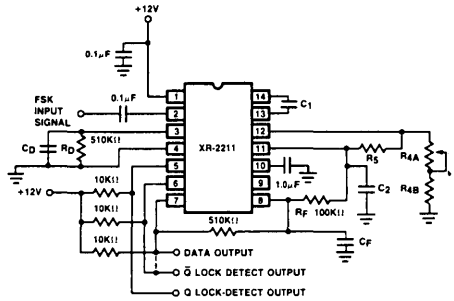
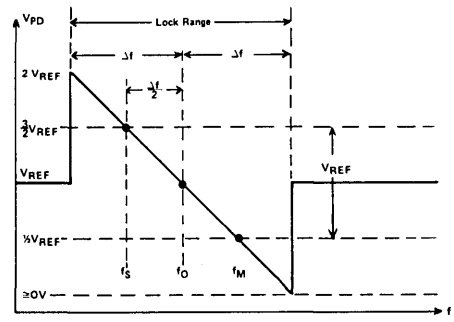


Figure 4: The XR-2211 FSK Demodulator with Carrier Detect



XR-2211 TRACKING CHARACTERISTICS

As seen above, the XR-2211 produces at its phase detector output a voltage V_{PD}, which has a peak to peak value equal to about V_{REF} for a frequency swing from f_M (mark) to F_S (space). The DC level V_{PD} will be about $V_{REF}\left(\frac{V+}{2} - .65\right)$.

CIRCUIT DESIGN

Table 2 shows recommended component values for the three most commonly used FSK bands. In many instances, system constraints dictate the use of some non-standard FSK bands. The XR-2206/XR-2207/XR-2211 combination is suitable for any range of frequencies from several Hertz to 100 kiloHertz.

Here are several guidelines to use when calculating non-standard frequencies:

- For maximum baud rate, choose the highest upper frequency that is consistent with the system bandwidth.
- The lower frequency must be at least 55% of the upper frequency (less than a 2:1 ratio).
- For minimum demodulated output pulse-width jitter, select an FSK band whose mark and space frequencies are both high, compared to the baud rate. (i.e., for a 300 baud channel, mark and space frequencies of 2025 Hz and 2225 Hz would result in significantly less pulse-width jitter than 300 Hz and 550 Hz).
- For any given pair of mark and space frequencies, there is a limit to the baud rate that can be achieved. When maximum spacing between the mark and space frequencies is used (where the ratio is close to 2:1) the relationship

$$\frac{\text{mark-space frequency difference (Hz)}}{\text{maximum data rate (baud)}} \geq 83\%$$

should be observed.

For narrower spacing, the minimum ratio should be about 67%.

The values shown in Table 2 may be scaled proportionately for mark and space frequencies, maximum baud rate, and (inversely) capacitor value. It is best to retain (approximately) the resistor values shown.

DESIGN EXAMPLES

I. Design a modem to handle a 10 kilobaud data rate, using the minimum necessary bandwidth.

A. Frequency Calculation
Because we want to use the minimum possible bandwidth (lowest possible upper frequency) we will use a 55:100 frequency ratio. The frequency difference, or 45% of the upper frequency, will be 83% of 10,000. We therefore chose an upper frequency:

$$\frac{83 \times 10{,}000}{45} = 18.444 \text{ kHz} \approx 18.5 \text{ kHz}.$$

and the lower frequency:

$$0.55 \times 18.5 \text{ kHz} = 10.175 \text{ kHz}.$$

B. Component Selection
1. For the XR-2207 FSK modulator, set $R_1 \approx 30$ kΩ. Now, select a value of C_O to generate 10.175 kHz with R_1:

$$10.175 \text{ kHz} = 1/(C_O \times 30{,}000);\ C_O = 3300\text{pF}.$$

To choose R_2:

$$18.500 \text{ khz} - 10.175 \text{ kHz} = 8.325 \text{ kHz} = 1/C_O R_2;\ R_2 = 36 \text{ k}\Omega.$$

A good choice would be to use 10 kΩ potentiometers for R_{1A} and R_{2A}, and to set $R_{1B} = 24$ kΩ and $R_{2B} = 30$ kΩ.

2. For the XR-2206, we can make R_7 equal to R_1, and C_3 equal to C_O above. To determine R_6:

$$18.5 \text{ kHz} = 1/R_6 C_3;\ R_6 = 16 \text{ k}\Omega$$

Use at 10 kΩ potentiometer for R_{6A} and set $R_{6B} = 13$ kΩ.

Table 2.
Recommended Component Values for Typical FSK Bands

FSK Band			XR-2207					XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{1A} R_{3A}	R_{1B} R_{3B}	R_{2A} R_{4A}	R_{2B} R_{4B}	C_O	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_{4A}	R_{4B}	R_5	C_1	C_2	C_F	C_D
300	1070	1270	10	20	100	100	.039	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
300	2025	2225	10	18	150	160	.022	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05
1200	1200	2200	20	30	20	36	.022	10	16	20	30	.022	10	18	30	.027	.0033	.0022	.01

Units: Frequency — Hz; Resistors — kΩ; Capacitors — μF

3. For the XR-2211 demodulator, we need to first determine R_4 and C_1. First, $f_0 = (f_L + f_H)/2 = (10.175 + 18.500)/2 = 14.338$ kHz. If we make $R_4 = 25$ kΩ, then $1/(C_1 \times 25{,}000) = 14{,}338$; $C_1 = 2790$ pF ≈2700 pF. With that value of C_1, the precise value of R_4 is now 25.8 kΩ. Select $R_{4B} = 18$ kΩ and use a 10 kΩ for R_{4A}.

C. Frequency Component Selection

1. To calculate R_5, we first need our Δf, which is 18,500 — 10.175, or 8.325 kHz:

$$8325 = (25{,}800 \times 14{,}338)/R_5$$
$$R_5 = 44.4\ \text{k}\Omega \approx 47\ \text{k}\Omega.$$

2. To determine C_2 use $\zeta = 1/2 = 1/4\ \ C_1/C_2$. Then, $C_2 = 1/4C_1$; $C_2 = 670$ pF:

3. To select C_F, we use τ_F = [0.3/(baud rate)] seconds:

$$\tau_F = 0.3/10{,}000 = 30\ \mu\text{sec}.$$

with

$$R_F = 100\ \text{k}\Omega,\ C_F = 300\ \text{pF}$$

D. Lock Range Selection

To select C_D, let us start with the actual lock range:

$$\Delta f = R_4 f_0/R_5\ \text{Hz} = 7870\ \text{Hz}$$

If we assume a capture range of 80%:

$$\Delta f_C = 6296\ \text{Hz}$$

therefore, our total capture range of $\pm\Delta f_C$ is 12,592 Hz. Our minimum value for C_D is (16/12,592) μf or 0.0013 μf.

E. Completed Circuit Example

See Figure 5.

II. Design a 3 kilobaud modem to operate with low output jitter. The bandwidth available is 13 kHz.

For this modem, we can take the values from two for the 300 baud modem operating at 1070 Hz and 1270 Hz, multiply our baud rate and mark and space frequencies by ten, and divide all capacitor values on the table by ten. Resistor values should be left as they are.

III. Design a 2 channel multiplex FSK modulator to operate at the following pairs of mark and space frequencies: 600 Hz and 900 Hz, and 1400 and 1700 Hz (each of these channels could handle about 400 baud).

For this task, we will use the XR-2207. The only real consideration here is that, if possible, we want to keep the following resistances all between 10 kΩ and 100 kΩ: R_1, R_1/R_2, R_3 and R_3/R_4. The ratio between the maximum and minimum frequencies is less than 3:1, so we should have no trouble meeting this criterion. If we set our maximum frequency with an R of about 20 kΩ, we have: $1700 = 1/(C_0 \times 20{,}000)$; $C_0 = 0.029$ μf which is approximately equal to 0.033 μf.

Calculating R_1 using 600 Hz and 0.033 μf, we get $R_1 = 50{,}5$ kΩ. We can use $R_{1B} = 47$ kΩ and $R_{1A} = 10$ kΩ. For R_2, we get 101 kΩ. Use $R_{2B} = 91$ kΩ and $R_{2A} = 20$ kΩ. To determine R_3, use: $1400\ \text{Hz} = 1/R_3C_0$, which gives us $R_3 = 21.6$ kΩ. Use $R_{3B} = 18$ kΩ and $R_{3A} = 5$ kΩ. R_4 must generate a 300 Hz shift in frequency, the same as R_2. Therefore, set R_4 equal to R_2.

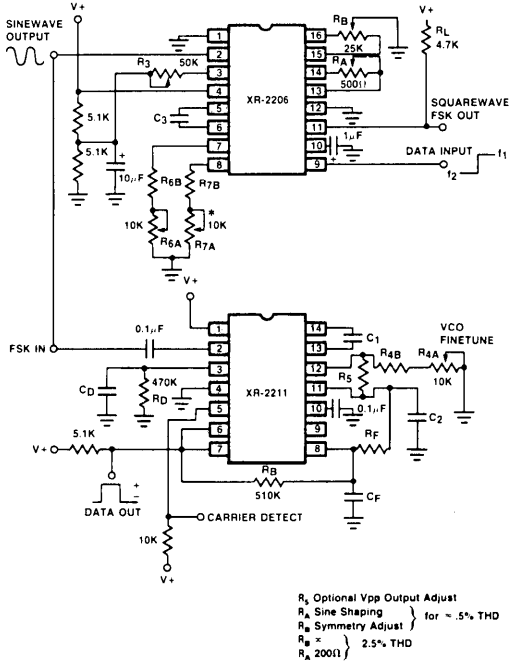


Figure 5: Full Duplex FSK Modem Using XR-2206 and XR-2211. (See Table 2 for Component Values.)

Adjustment Procedure

The only adjustments that are required with any of the circuits in this application note are those for frequency fine tuning. Although these adjustments are fairly simple and straightforward, there are a couple of recommendations that should be followed.

The XR-2207: Always adjust the lower frequency first with R_{1B} or R_{3B} and a low level on Pin 9. Then with a high level on Pin 9, adjust the high frequency using R_{2B} or R_{4B}. The second adjustment affects only the high-frequency, whereas the first adjustment affects both the low- and the high-frequencies.

The XR-2206: The upper and lower frequency adjustments are independent, and the sequence is not important.

The XR-2211: With the input open-circuited, the loop-phase detector output voltage is essentially undefined and VCO frequency may be anywhere within the lock range. There are several ways that f_o can be monitored:

1. Short Pin 2 to Pin 10 and measure f_o at Pin 3 with C_D disconnect;
2. Open R_5 and monitor Pin 13 or 14 with a high-impedance probe; or
3. Remove the resistor between Pin 7 and 8, and find the input frequency at which the FSK output changes state.

Note: Do NOT adjust the center frequency of the XR-2211 by monitoring the timing capacitor frequency with everything connected and no input signal applied.

For further information regarding the use of the XR-2207, XR-2206 and XR-2211 refer to the individual product data sheets.

XR-C240 Monolithic PCM Repeater

INTRODUCTION

The XR-C240 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Mega bits per second (Mbps) data rates on T-1 type PCM lines. The device is packaged in hermetic 16-pin DIP package and is designed to operate over a temperature range of −40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities. Compared to conventional repeater designs using discrete components, the XR-C240 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

THE T-1 REPEATER SYSTEM:

The T-1 Repeater Line is designed to provide a transmission capability for 24 two-way voice frequency signals which are transmitted digitally using a Pulse-Code Modulation (PCM) technique. The system operates at a data rate of 1.544 Mbps, with bipolar data pulses. It can operate on either pulp- or polyethylene-insulated paired cable that is either pole mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772 kHz is less than 36 dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end crosstalk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The details of the T-1 type PCM systems are well covered in the literature listed in References 1 through 5.

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The dc power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator.

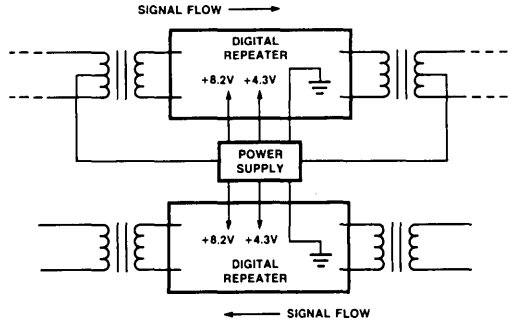


Figure 1. Block Diagram of a Bi-directional Digital Repeater System.

The XR-C240 monolithic IC replaces about 90% of the electronic components and circuitry within the "digital repeater" sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C240 ICs, one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C240 monolithic IC.

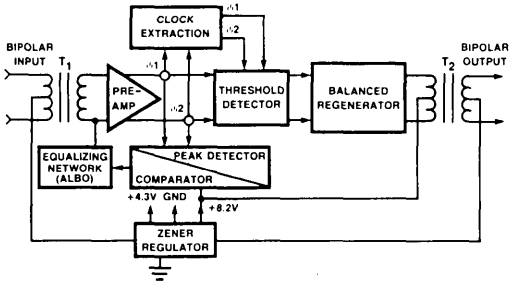


Figure 2. Functional Block Diagram of a Digital PCM Repeater Section.

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In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization and, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544 MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse is in turn applied to a discrete switch which is used to drive the next section of the paired cable.

REFERENCES ON PCM REPEATERS:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25-97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99-143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1-25.
4. Fultz, K. E., and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405-1452.
5. Tarbox, R. A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 — 46-10.

OPERATION OF THE XR-C240

The XR-C240 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line (DIP) package.

The circuit is designed to operate with two positive supply voltages, V^{++} and V^{+} which are nominally set to be 8.2V and 4.3V, respectively. Figure 4 gives a typical recommended power supply connection for the circuit.

The supply currents I_A and I_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 8.2V supply voltage, I_A:

$$1.1mA \leq I_A \leq 2.5mA$$

b. Current from 4.3V supply voltage, I_B:

$$6mA \leq I_B \leq 11mA$$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the

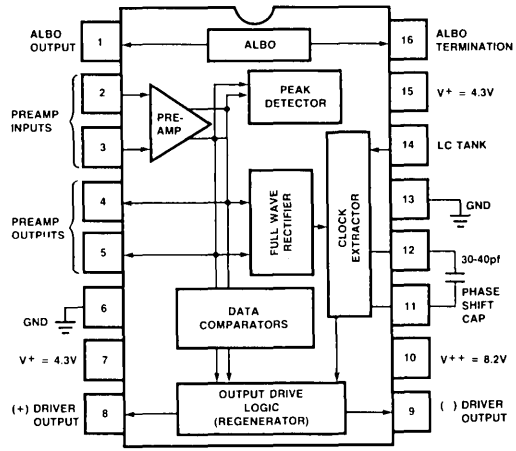


Figure 3. Package Diagram of XR-C240 Monolithic PCM Repeater.

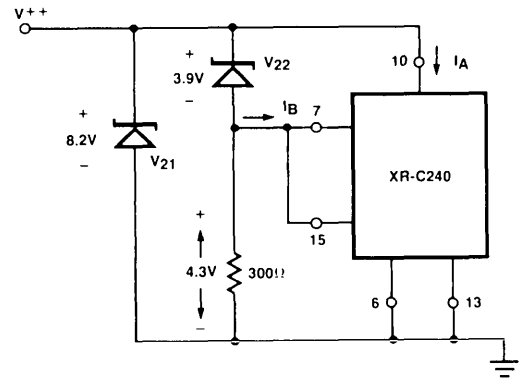


Figure 4. Recommended supply Voltage Connection for XR-C240 (Note: See Figure 6 for Recommended bypass capacitors).

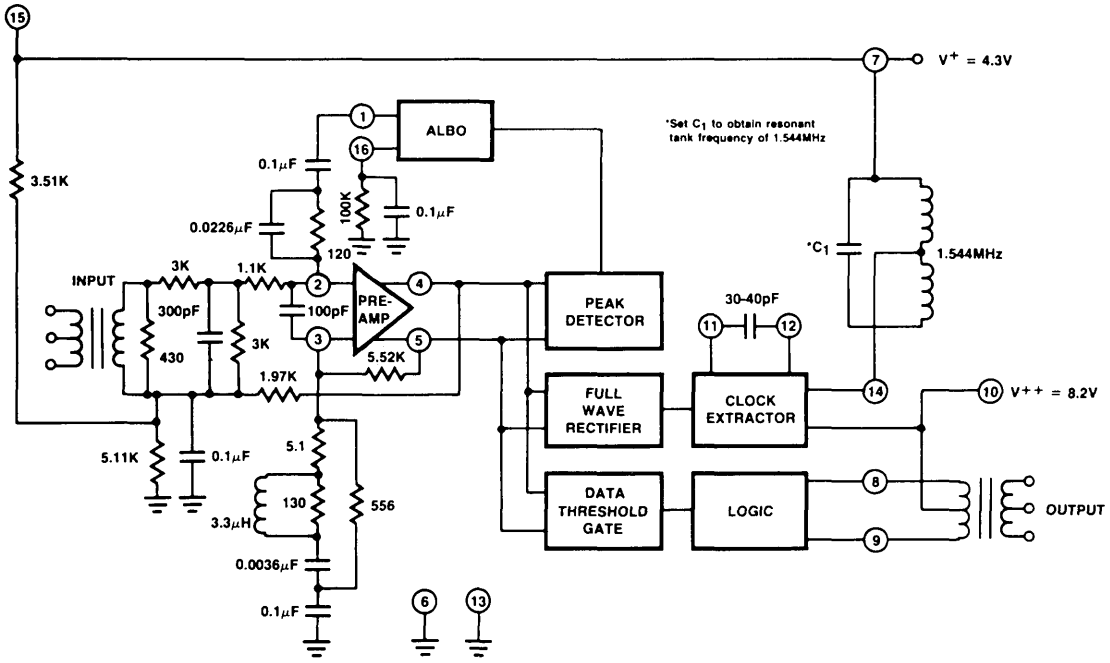


Figure 5. External Components Necessary for Circuit Operation.

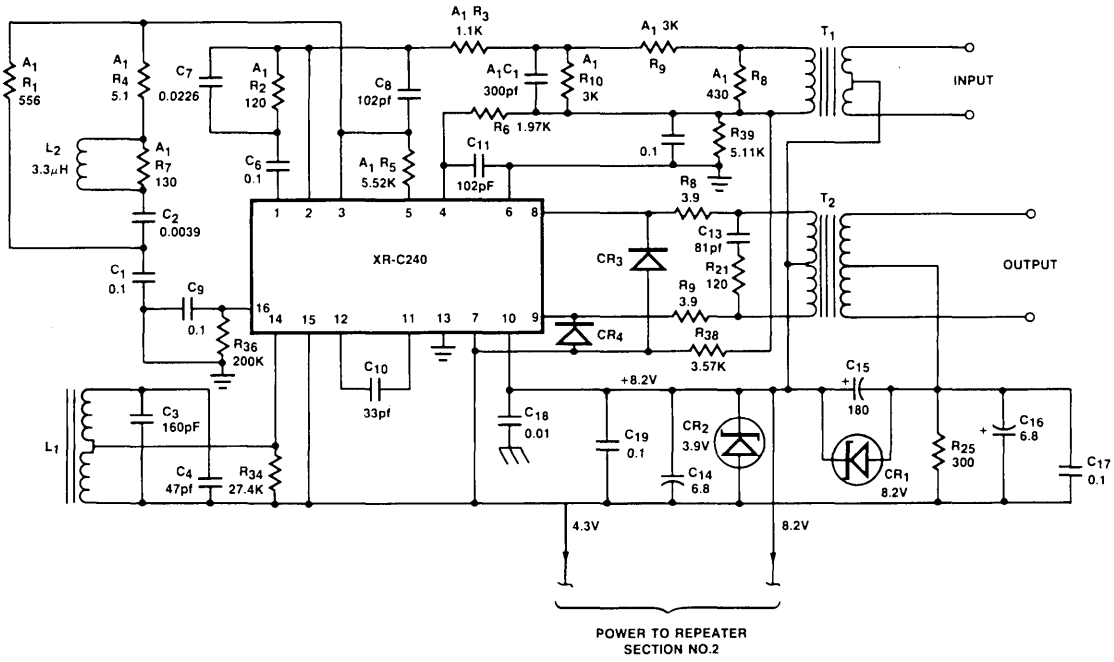


Figure 6. A Typical Circuit Connection for XR-C240 in 1.544 MHz T-1 Repeater System.

system block diagram. Note that all the blocks shown in Figure 6 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 4).

Figure 6 shows a practical circuit connection for the XR-C240 in an actual PCM repeater application for 1.544 Mbps T-1 Repeater application. For simplification purposes, the lightening protection circuitry and the second repeater section are not shown in the figure.

DESCRIPTION OF CIRCUIT OPERATION:

This section gives a brief description of the internal circuitry contained within the XR-C240 monolithic IC.

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband voltage gain of 52db. The differential outputs of the preamplifier (Pins 4 and 5) are internally connected to the peak-detector,

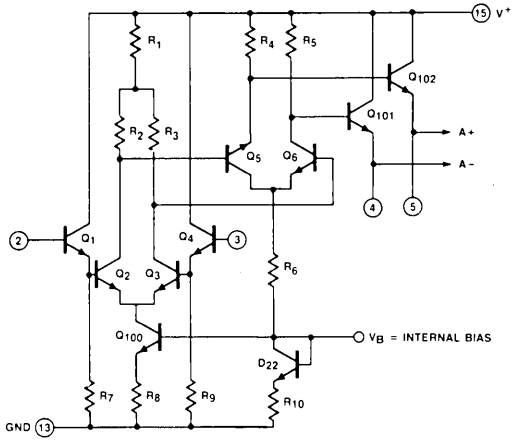


Figure 7. Circuit Diagram of Preamplifier Section.

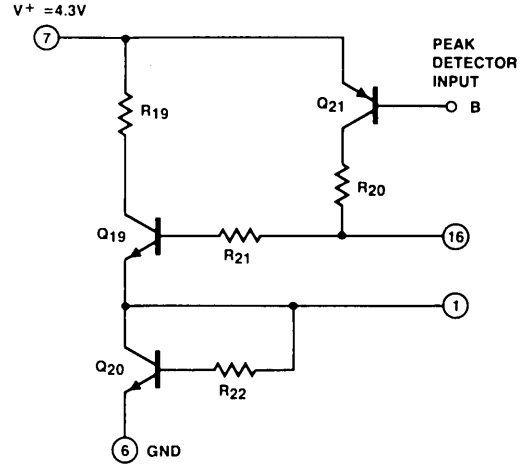


Figure 9. Automatic Line Build-Out (ALBO) Section.

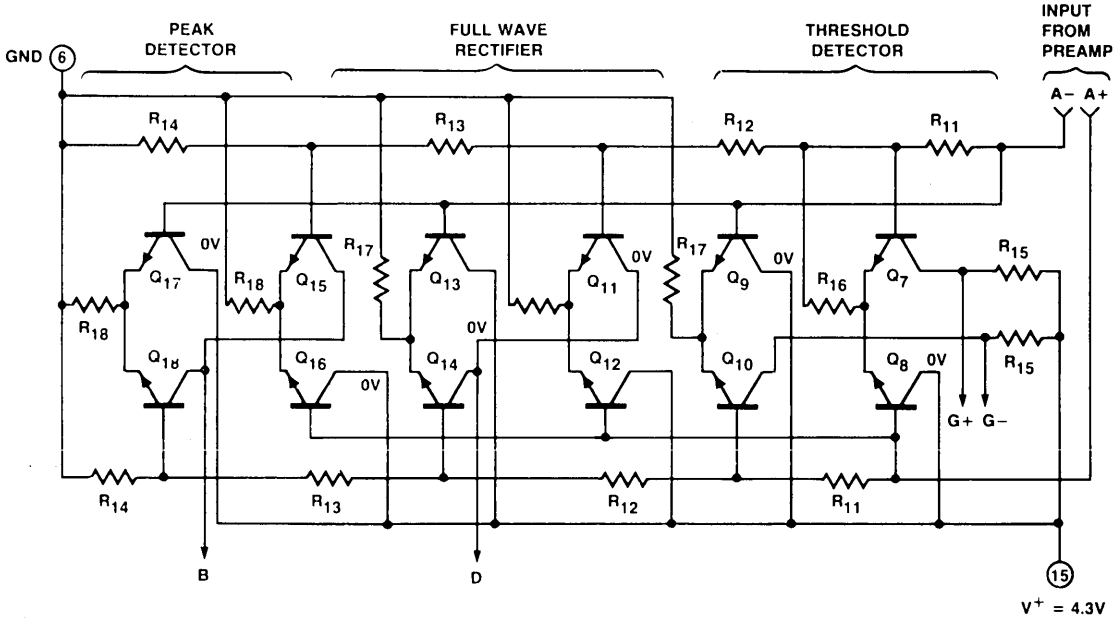


Figure 8. Circuit Diagram of Threshold-Detector, Full-Wave Rectifier and Peak-Detector Sections.

full-wave rectifier and the threshold detector sections of the XR-C240 as shown in Figure 8.

The peak-detector output (terminal B of Figure 8) is internally connected to the Automatic Line Build-out (ALBO) section of the circuit and controls the DC bias current through the ALBO diodes Q_{19} through Q_{20}, as shown in Figure 9.

The full-wave rectifier output (output D of Figure 8) is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (Pin 14) of the injection locked oscillator. The threshold-detector outputs (G+ and G− of Figure 8) provide the differential logic drive to the data latches of the logic section of XR-C240.

The clock-extractor section of XR-C240 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{23}, through terminal D which is internally connected to the output of the threshold comparator. This signal in turn controls the current in the resonant L-C tank circuit connected to Pin 14. The sinusoidal waveform across the tank is then amplified and squared through the cascaded differential gain stages made up of Q_{31}, Q_{32} and Q_{35}, Q_{36}. The output swing of the second gain stage is "integrated" by the phase-shift capacitor, C_1, externally connected to Pins 11 and 12. (See timing diagrams of Figure 13.) The nominal value of this capacitor is in the 30 to 40pf range. The triangular waveform across Pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the "strobe" signal, C_p, and the clock pulse C_ϕ, which is applied to the data latches of the logic section.

The strobe and clock pulses out of the clock-regenerator section are applied to the output data latches shown in Figure 11. The two parallel output R-S flip-flops are driven by the differential inputs (G+ and G−) from the data comparator of Figure 8. The two sets of differential data signals, F_1, $\overline{F_1}$ and F_2, $\overline{F_2}$ are then applied to the output driver amplifier shown in Figure 12. The high-current outputs of the driver stage (Pins 8 and 9) are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage spread, i.e.:

Peak Output Swing = $(V^{++}) - (V^{+}) - (V_{BE}) \simeq 3.2V$

The output stage is designed to work into a nominal load impedance of 100 ohms, and can handle peak load currents of 30mA.

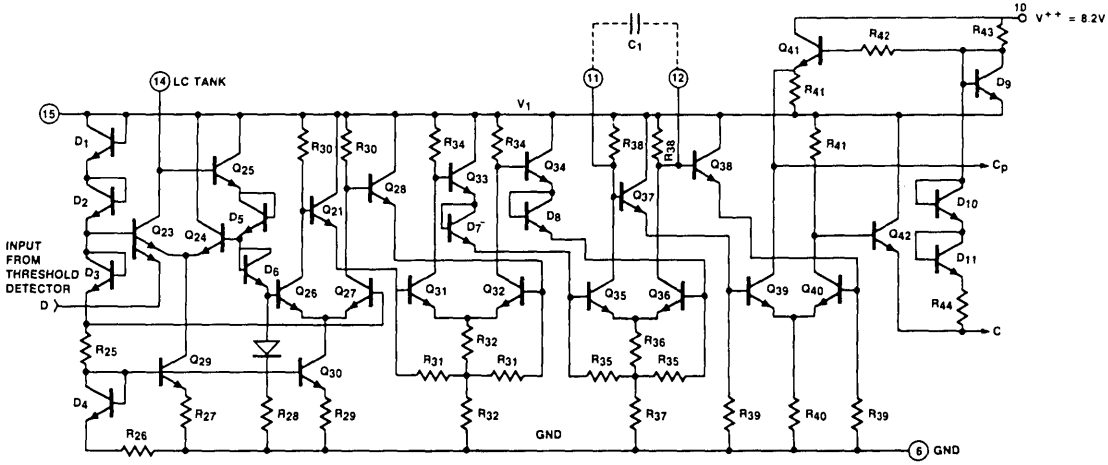


Figure 10. Circuit Diagram of Clock Extractor Section.

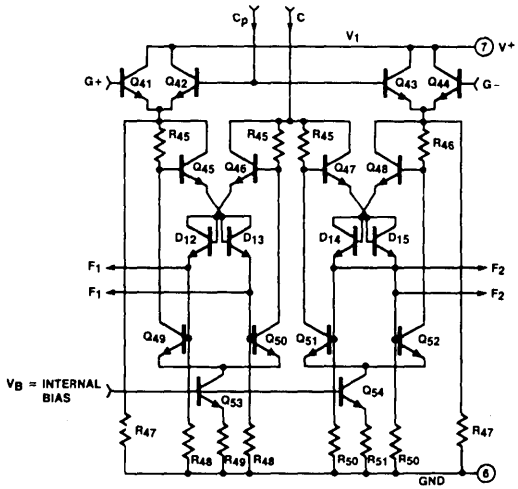


Figure 11. Data Output Latches (Logic Section).

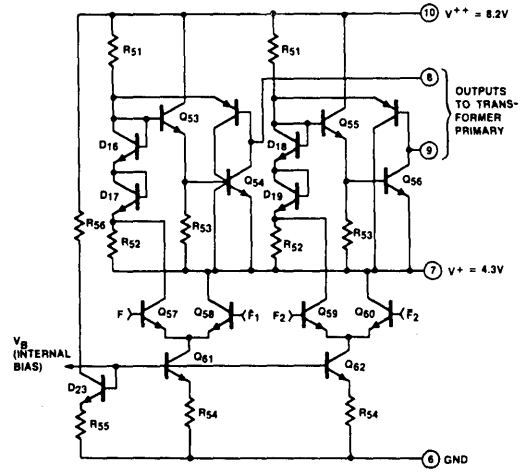


Figure 12. Output Driver Section.

ELECTRICAL CHARACTERISTICS
(Measured at 25°C with V++ = 8.2V, V+ = 4.3 V, unless specified otherwise.)

PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
Supply Voltage:				
$V++$	7.79	8.61	V	Measured at Pin 10
$V+$	4.085	4.515	V	Measured at Pins 7 and 15
Supply Current:				See Figure 4
I_A	1.1	2.5	mA	Supply = 8.2V
I_B	6	11	mA	Supply = 4.3V
Total Current	7.1	13.5	mA	
Preamplifier				
Input Offset Voltage, V_{OS}		15	mV	
Open Loop Differential Gain, A_O	50	54	db	
Input Bias Current, I_B		4	μA	
Input Offset Current, I_{OS}		2	μA	
Input Impedance, R_{in}	50		kΩ	
Comparator Thresholds				See Figure 8 Measured Differentially Across Pins 4 and 5
Peak Detector (ALBO) Threshold	±1.3	±1.6	V	
Full-Wave Rectifier Threshold	±0.9	±1.15	V	
Data Threshold	±0.28	±0.48	V	
Clock Extractor Section				See Figure 10
Tank Drive Impedance	50		kΩ	At Pin 14
Tank Drive Current				
"Zero" Signal Current	12	24	μA	
"One" Signal Current	80	220	μA	
Recommended Tank Q	100			
Phase Shifter Offset Voltage	−18	+18	mV	Voltage applied to Pins 7 and 14 to reduce differential voltage across Pins 11 and 12 to zero.
Output Drive Section				See Figure 12 Voltage levels referenced to Pin 7
Output Voltage Swing	3.0		V	R_L = 100 Ω

Active Filter Design with IC OP Amps

INTRODUCTION

This application note will assist the designer in selecting the optimum filter for his application. It begins with a table of transfer functions, and network defining equations, for the high-pass, low-pass, bandpass, and band-reject filters. A guide to the three types of filter responses will be presented, along with illustrations of several filter realizations, with their respective merits and limitations. Finally, the entire contents are brought together, to provide the designer a complete working schematic of an active filter in a modem configuration, utilizing the XR-4202 Quad Programmable Operational Amplifier, along with the XR-2206 Waveform generator, and the XR-2211 Precision Tone Decoder.

PRINCIPLES OF OPERATION

The XR-4202 Quad Programmable Operational Amplifier is a basic building block for active filters, and is ideally suited for most filter applications. The XR-4202 provides the user the flexibility to externally program the gain-bandwidth product, the supply current, the input bias current, the input offset current, the input noise, and the slew rate. The user, therefore, can trade-off bandwidth for supply current or optimize the noise figure. Likewise, other amplifier characteristics can be programmed for a specific need.

Since the operational amplifier plays such a key role in the active filter, its characteristics are of prime importance. By using operational amplifiers as the basic gain stage of the active filter, problems previously encountered due to low-input impedance, high-output impedance and low-gain are virtually eliminated. Operational amplifiers provide the required response for various filter types. Some of the more popular filters are multiple feedback, state variable, bi-quad and Sallen Key, which can be used to obtain high-pass, bandpass and low-pass filter functions. They are capable of giving the designer all of the standard filter responses, i.e., Butterworth, Chebychev, and Bessel.

There are many single, dual, and quad operational amplifiers that can be used to implement the filters discussed. Table 1 lists some standard operational amplifiers and compares their important characteristics. Table 2 gives the designer a brief review of the basic transfer functions and network defining equations. Note that a family of curves exists for all filters except first order low-pass and high-pass. This is due to the presence of loop damping. This point will be expanded upon in the next section on filter responses.

Table 1.

DEVICE CHARACTERISTICS	XR-4202	XR-3403	XR-4136	XR-4558	741	UNITS
Slew Rate	1.5	.6	1.6	1	.5	V/μS
Gain-Bandwidth Product	3.5	1	3	3	1	MHz
Input Offset Current	10	30	10	5	20	nA
Input Bias Current	80	200	80	40	80	nA
Supply Current (max)	6.0	7.0	4.0	5.7	2.8	mA

Note: All values typical unless otherwise specified.

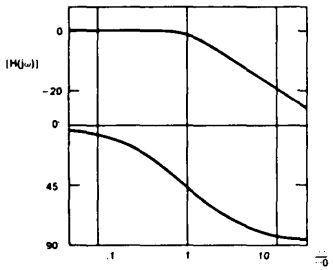
Table 2.
Transfer Functions and Equations

Low Pass

$$H(s) = \frac{H_0\omega_0}{s + \omega_0}$$

$$|H(j\omega)| = \left[\frac{H_0{}^2\omega_0}{\omega^2 + \omega_0{}^2}\right]^{1/2}$$

$$\phi = \text{Tan}^{-1}\frac{\omega}{\omega_0}$$

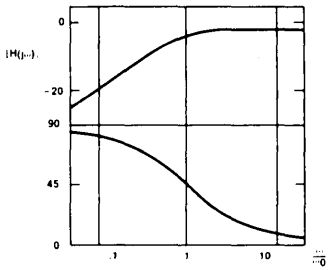


High Pass

$$H(s) = \frac{H_0 s}{s + \omega_0}$$

$$|H(j\omega)| = \left[\frac{H_0{}^2\omega_0{}^2}{\omega^2 + \omega_0{}^2}\right]$$

$$\phi = \frac{\pi}{2} - \text{Tan}^{-1}\frac{\omega}{\omega_0}$$



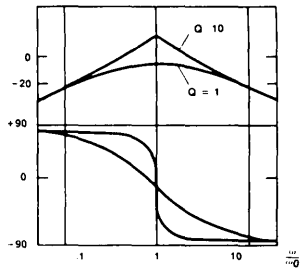
Band Pass

$$H(s) = \frac{H_0\,\alpha\,\omega_0 s}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

$$|H(j\omega)| = \left[\frac{H_0{}^2\alpha^2\omega_0{}^2\omega^2}{\omega^4 + \omega^2\omega_0{}^2(\alpha^2 - 2) + \omega_0{}^2}\right]$$

$$\phi = \frac{\pi}{2} - \text{Tan}^{-1}\left(\frac{2Q\omega}{\omega_0} + \sqrt{4Q^2 - 1}\right)$$

$$-\text{Tan}^{-1}\left(\frac{2Q\omega}{\omega_0} - \sqrt{4Q^2 - 1}\right)$$



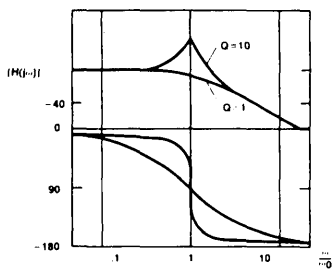
Low Pass Second Order

$$H(s) = \frac{H_0\omega_0{}^2}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

$$|H(j\omega)| = \left[\frac{Ha^2\omega_0{}^4}{\omega^4 + \omega^2\omega_0{}^2(\alpha^2 - 2) + \omega_0{}^4}\right]$$

$$\phi = -\text{Tan}^{-1}\left[\frac{1}{\alpha}\,2\frac{\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right]$$

$$-\text{Tan}^{-1}\left[\tfrac{1}{2}\,\frac{2\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right]$$



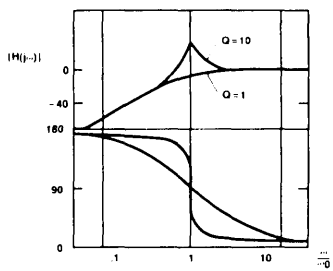
High Pass Second Order

$$H(s) = \frac{H_0 s^2}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

$$|H(j\omega)| = \left[\frac{H_0{}^2\omega^4}{\omega^4 + \omega^2\omega_0{}^2(\alpha^2 - 2) + \omega_0{}^4}\right]$$

$$\phi = \pi - \text{Tan}^{-1}\left[\frac{1}{\alpha}\left(2\frac{\omega}{\omega_0} + \sqrt{4 - \alpha^2}\right)\right]$$

$$-\text{Tan}^{-1}\left[\frac{1}{\alpha}\,2\left(\frac{\omega}{\omega_0} - \sqrt{4 - \alpha^2}\right)\right]$$



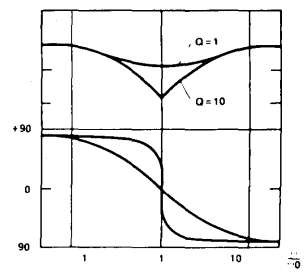
Band Reject

$$H(s) = \frac{(s^2 + \omega_0{}^2)H_0}{s^2 + \alpha\omega_0 s + \omega_0{}^2}$$

$$|H(j\omega)| = \left[\frac{H_0{}^2\omega^4 + \omega_0{}^4}{\omega^4 + \omega^2\omega_0(\alpha^2 - 2) + \omega_0{}^4}\right]$$

$$\phi = \frac{\pi}{2} - \text{Tan}^{-1}\,\frac{2Q\omega}{\omega_0} + \sqrt{4Q^2 - 1}$$

$$-\text{Tan}^{-1}\left(\frac{2Q\omega}{\omega_0} - \sqrt{4Q^2 - 1}\right)$$



Definition of terms:

ω_0 = Cutoff frequency $2\pi f_0$
α = Loop damping
$s = \sigma + j\omega$ complex frequency

ω_c = Center frequency
ω_1 = Lower cutoff frequency
ω_2 = Upper cutoff frequency

$Q = 1/\alpha = \dfrac{\omega c}{\omega_2 - \omega_1}$
ϕ = Phase
$|H(j\omega)|$ = Magnitude response
$H(s)$ = Transfer function

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Filter Responses

Once the transfer function has been determined, the next step in filter design is to decide upon the desired response. As previously mentioned, the damping of the filter determines its characteristics near cutoff. There are three basic types of responses which are depicted in Table 3, along with their characteristics. In the case of Butterworth and Bessel, the response has been fixed. However, for the Chebychev the α is chosen for the particular response desired. This is done by using a nomograph such as the one shown in Figure 1. To use a nomograph the information required is: A_{max} (maximum ripple in the passband), A_{min} (minimum attenuation in the stop band), and Ω_S (ratio of the A_{min} bandwidth to the A_{max} bandwidth). These terms are illustrated in Figure 2. Once these terms are known, the nomograph is used by locating A_{max}, and drawing a straight line through A_{min} to the left-hand side of the graph. From this point, a horizontal line is drawn to the intersection of Ω_S. The minimum order of the transfer function will be the number of the curve passing above this point. Once this is done, the α and ω_o for each stage is found by consulting the Chebychev network parameter tables for the desired passband ripple, and the number of poles. Such tables can be found in standard filter handbooks.

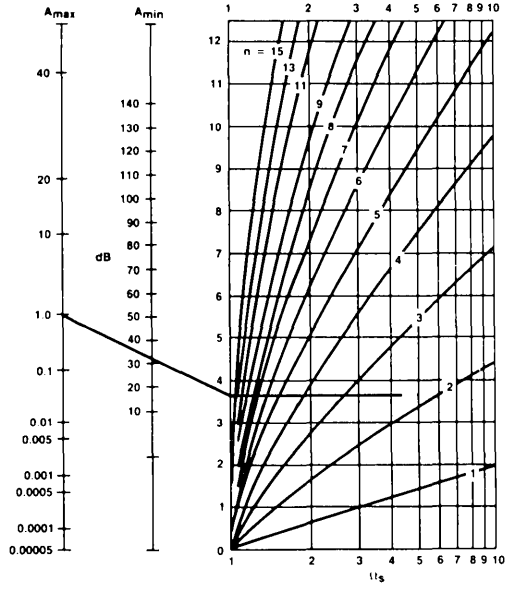

Figure 1. Nomograph to Select Desired Response.

Filter Realizations

There are numerous ways of realizing the transfer functions discussed. Each method has its own relative merit. The configuration selected depends primarily on the specific application and the desired sensitivity parameters. Sensitivity parameters are a means of relating the resultant change in a transfer function, due to an element change. Although these parameters are only directly applicable to an infinitesimal change, they are easily used to evaluate performance for 1% changes, and many times are used for element changes up to 10%. Examples will be given later in this section that will help clarify this parameter.

Table 3.

FILTER TYPE	α	BASIC FEATURES	AMP. RESPONSE
Bessel	$\sqrt{3}$	Best time delay Smoothest phase response	
Butterworth	$\sqrt{2}$	Maximally flat amplitude response	
Chebychev	Can Vary	Passband ripple Fast cutoff slope	

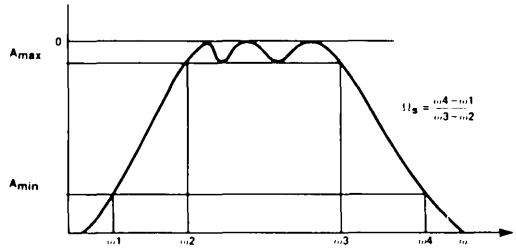

Figure 2. Ratio of A_{min} Bandwidth to A_{max} Bandwidth.

The filter realizations presented here are to be used as a basic guide to help the designer become more adept at designing filters. State-variable and multiple feedback filters will be discussed, and the relative merits of each will be given. It will also be shown that many of the commonly used filters are actually specific cases for the filters mentioned.

Figure 3 illustrates a typical multiple feedback connection with the non-inverting input grounded. To minimize offset, this point should be returned to ground via a resistor whose value is equal to the impedance at the inverting input. The transfer function for this circuit is given by Eq. 1. Each element represents a single resistor or capacitor. To realize the transfer function, each admittance parameter is replaced by 1/R for a resistor and SC for a capacitor. An example will help to clarify this point. If the desired response is a high pass, the form of the characteristic equation is given in Table 2. To transform Eq. 1 into the high-pass characteristic, then Y_1, Y_3, and Y_4 become capacitors and Y_2 and Y_5 resistors. (It should be obvious that a low-pass function could have been fabricated by letting Y_2 and Y_5 be capacitors, and similarly, a bandpass function could have been realized by making Y_3 and Y_4 capacitors.) The terms of the network function, for the high-pass filter shown in Figure 4, are given in Table 4 along with their sensitivity parameters. The transfer function for Figure 4 is given by Eq. 2.

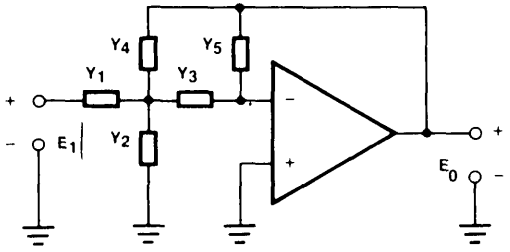

Figure 3. Multiple Feedback Connection with Noninverting Input Grounded.

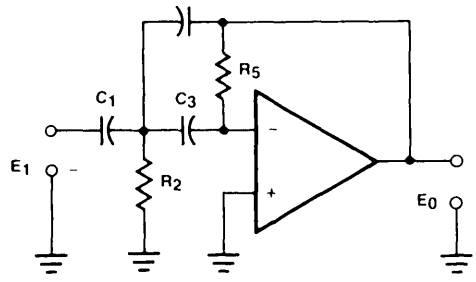

Figure 4. Network Function for the High-Pass Filter.

Eq. 1 $$\frac{E_0}{E_1}(s) = \frac{-Y_1Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3Y_4}$$

Eq. 2

$$\frac{E_0}{E_1}(s) = \frac{-(C_1/C_4)s^2}{s^2 + s(1/R_5)(C_1/C_3C_4 + 1/C_4 + 1/C_3) + 1/R_2R_5C_3C_4}$$

As can be seen from the sensitivity parameters, there is a high degree of circuit sensitivity due to the component tolerances. Due to the interaction of components, the tuning of this circuit may be rather involved. However, with tight component tolerances, these circuits give the designer very predictable results. Due to the high input impedance and low-output impedance, several of these stages may easily be cascaded to achieve a higher order function. What is desired is to have a lower sensitivity to component tolerances. The most commonly used filter for this purpose is the state-variable.

The state-variable synthesis approach is used in most present day Universal Active Filters (UAF). With this method, the actual n^{th} order polynominal of the transfer function is simulated as it would be with an analog computer. When using the state-variable approach, all three outputs (high-pass, low-pass, and bandpass) are available simultaneously. The sensitivities, with respect to component tolerances, are typically less than or equal to one, and the sensitivity of Q, with respect to amplifier gain, can equal zero with high amplifier gain. Because of the high amplifier gain requirement, these filters tend to be limited to the audio range. The cost of reducing the circuit element sensitivities is the need to use n+2 operational amplifiers to synthesize an n^{th} order transfer function. For this reason, this type of configuration may not be cost effective in the synthesis of low-Q, high-pass, and low-pass filters.

Table 4.

Parameter	Defining Equation	Sensitivity	
H_0	$= \frac{C_1}{C_4}$	$S_{C_1}^{H_0} = -S_{C_4}^{H_0} = 1$	
α	$= \sqrt{\frac{R_2}{R_5}}\left(\frac{C_1}{\sqrt{C_3C_4}} + \sqrt{\frac{C_3}{C_4}} + \sqrt{\frac{C_4}{C_3}}\right)$	$S_{C_3}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_0R_5C_3}\left(\frac{C_1}{C3} + 1\right)$ $S_{C_4}^{\alpha} = \frac{1}{2} - \frac{1}{\alpha\omega_0R_5C_4}\left(\frac{C_1}{C3} + 1\right)$ $S_{C_1}^{\alpha} = \frac{1}{\alpha\omega_0R_5}\frac{C_1}{C_3C_4}$ $S_{R_2}^{\alpha} = -S_{R_5}^{\alpha} = \frac{1}{2}$	Note: The sensitivity of H_0 with this implies that if C_1 changes by 1% H_0 will also change by 1%. The defining equation for a sensitivity parameter is: $S_xY = \frac{xdY}{Ydx}$
ω_o	$= \left(\frac{1}{R_2R_5C_3C_4}\right)^{1/2}$	$S_{R_2}^{\omega 0} = S_{R_5}^{\omega 0} = S_{C_3}^{\omega 0} = S_{C_4}^{\omega 0} = -\frac{1}{2}$	

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Table 5.

Output	Parameters	Defining Equation	Sensitivity
Low Pass Eq. 3	H_0	$\frac{1 + R_3/R_4}{1 + R_1/R_2}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1/(1 + R_2/R_1)$ $S_{R_3}^{H_0} = -S_{R_4}^{H_0} = \frac{1}{H_0}\left(\frac{R_3/R_4}{1 + R_1/R_2}\right)$
	ω_0	$\left(\frac{R_4}{R_3R_5R_6C_1C_2}\right)^{1/2}$	$S_{R_3}^{\omega 0} = S_{R_5}^{\omega 0} = S_{R_6}^{\omega 0} = S_{C_1}^{\omega 0} = S_{C_2}^{\omega 0} = -S_{C_4}^{\omega 0} = -1/2$
	α	$\frac{1 + R_4/R_3}{1 + R_2/R_1}\left(\frac{R_3R_6C_2}{R_4R_5C_1}\right)^{1/2}$	$S_{R_4}^{\alpha} = -S_{R_3}^{\alpha} = -1/2 + \frac{R_4/R_3}{R_5C_1\,\alpha\omega_0(1 + R_2/R_1)}$ $S_{R_1}^{\alpha} = -S_{R_3}^{\alpha} = \frac{1}{1 + R_1R_2}$ $S_{R_6}^{\alpha} = S_{C_2}^{\alpha} = -S_{R_5}^{\alpha} = -S_{C_1}^{\alpha} = 1/2$
High Pass Eq. 4	H_0	$\frac{1 + R_4/R_3}{1 + R_1/R_2}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1/(1 + R_2/R_1$ $S_{R_3}^{H_0} = -S_{R_4}^{H_0} = \frac{1}{H_0}\left(\frac{R_4/R_3}{1 + R_1/R_2}\right)$
	ω_0	SAME AS LOW PASS	
	α	$\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right)\left(\frac{R_3R_6C_2}{R_4R_5C_1}\right)^{1/2}$	$S_{R_4}^{\alpha} = -S_{R_3}^{\alpha} = -1/2 + \frac{R_4/R_3}{R_5C_1\,\alpha\omega_0(1 + R_2/R_1)}$ $S_{R_1}^{\alpha} = -S_{R_2}^{\alpha} = \frac{1}{1 + R_1R_2}$ $S_{R_6}^{\alpha} = S_{C_2}^{\alpha} = -S_{R_5}^{\alpha} = -S_{C_1}^{\alpha} = 1/2$
Band Pass Eq. 5	H_0	$\frac{R_2}{R_1}$	$S_{R_1}^{H_0} = -S_{R_2}^{H_0} = -1$
	ω_0	SAME AS LOW PASS	
	$Q = 1/\alpha$	$\left(\frac{1 + R_2/R_1}{1 + R_4/R_3}\right)\left(\frac{R_4R_5C_1}{R_3R_6C_2}\right)^{1/2}$	$S_{R_5}^{Q} = S_{C_1}^{Q} = -S_{R_6}^{Q} = -S_{C_2}^{Q} = 1/2$ $S_{R_4}^{Q} = S_{R_3}^{Q} = 1/2 - \frac{R_4/R_3}{R_5C_1\,\alpha\omega_0(1 + R_2/R_1)}$ $S_{R_2}^{Q} = -S_{R_1}^{Q} = \frac{1}{1 + R_1/R_2}$

Figure 5 shows a typical state-variable configuration whose characteristic equations are given by Eq. 3, Eq. 4, and Eq. 5. These equations all have the same denominator, and the numerator is determined by the point at which the output is taken. This form may also be used to simulate a band-reject function by summing the high-pass and low-pass outputs. The defining equations and sensitivity parameters are given in Table 5. It is noted here that the bi-quad is actually a slight variation of a second order state-variable.

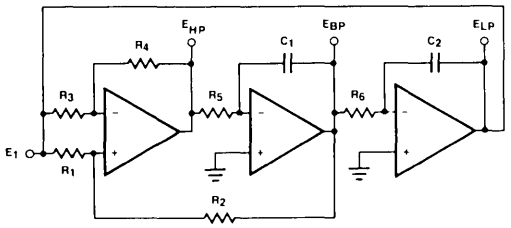

Figure 5. Typical State-Variable Configuration.

Eq. 3

$$\frac{E_{LP}}{E_i} = \frac{\left(\frac{1}{R_5R_6C_1C_2}\right)\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5R_6C_1C_2}\right)}$$

Eq. 4

$$\frac{E_{HP}}{E_i} = \frac{s^2\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5R_6C_1C_2}\right)}$$

Eq. 5

$$\frac{E_{BP}}{E_i} = \frac{-s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_1/R_2}\right)}{s^2 + s\left(\frac{1}{R_5C_1}\right)\left(\frac{1 + R_4/R_3}{1 + R_2/R_1}\right) + \frac{R_4}{R_3}\left(\frac{1}{R_5R_6C_1C_2}\right)}$$

Modem Filter

A typical application for an active filter is the input stage of a frequency demodulator. Any noise or spurious signals at this point would affect the overall quality of the output. A more specific example can be cited by considering the FSK system shown in Figure 6. (Frequency-shift keying is a means of transmitting digital information, primarily through telecommunications links.) This type of system is thoroughly covered in Exar's Application Note, AN-01, and will only be briefly discussed here.

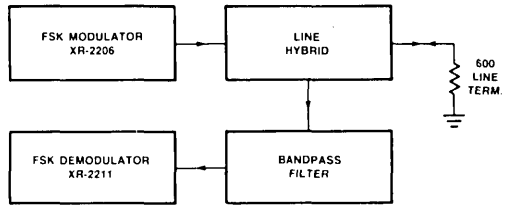

Figure 6. FSK System.

In this system, the digital data to be transmitted is used to key the XR-2206. The frequency-shift keyed output of the XR-2206 is then sent through the hybrid and out onto the line. (The hybrid is used to obtain isolation between data transmitted and data received, and may also be used to amplify the received signal.) In full duplex operation, this system must be able to receive and transmit, simultaneously. Due to line losses, the received signal may range from −12 dBm to −48 dBm. The output level of the transmitter is typically −6 dBm (allowing for a 6 dB loss in the hybrid). Due to line mismatch, the hybrid may only provide 10 dB of isolation to the filter. Therefore, the levels at the input of the filter, assuming a gain of 6 dB from the line through the hybrid, is −6 and −42 dBm for the desired signal, and −16 dBm from the local oscillator. This means that in a worst case situation, the input level of the received signal is −42 dBm, with the level of the local oscillator 26 dB above this. For the XR-2211 to operate with a low-bit error rate, the input should be 6 dB higher than the interfering signal. This implies that the stopband, A_{min}, from Figure 2 is 32 dB. The XR-2211 has an internal preamplifier with a dynamic range of greater than 60 dB, and requires a minimum input level of −38 dBm to cause limiting. If we choose a filter to have a passband ripple of 1 dB, and an overall gain of 5 dB, the input conditions of the XR-2211 will be satisfied. The filters introduce a phase shift that is only linear for approximately 1/2 and 1/3 of the passband; therefore, a bandwidth of 400 Hz is used for the filter. The general shape of the filter is shown in Figure 7.

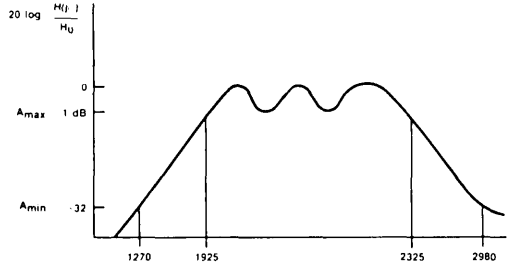

Figure 7. General Filter Shape.

Note: The values used in this filter are based on a modem using an XR-2206 as the modulator, and XR-2211 as the demodulator. If digital techniques are used, the filter parameters may be different, due to the harmonics generated by digital synthesis of a sine wave, and higher signal-to-noise requirements of the demodulator.

To find the minimum number of poles required for this response, the nomograph in Figure 1 is used. The point falls between a 2- and 3-pole filter. The values of $\omega_o + \alpha$ are determined from the tables, for a 3rd order Chebychev response with 1 dB ripple.

From the tables:

$\omega_0 = .997098$ complex pole
$\alpha = .495609$
$\omega_0 = .494171$ – real pole.

The geometric center is $\omega_0 = \sqrt{\omega_3\omega_2}$ or $\sqrt{f_3 f_2} = f_0$

The filter $Q_0 = \dfrac{f_0}{f_3 - f_2} = \dfrac{\sqrt{(1925)(2325)}}{2325 - 1925} = 5.28892$

The Q of each section of the filter is determined by Equation 6.

Eq. 6

$$Q_A = \frac{\left(\frac{\omega_1}{Q_0}\right)^2 + 4 + \sqrt{\left[\left(\frac{\omega_1}{Q_0}\right)^2 + 4\right]^2 - 4\left(\frac{\alpha_1\omega}{Q_0}\right)^2}}{2\frac{\alpha_1\omega_1}{Q_0}^2}$$

$Q_1 = 21.49 = Q_2$. Section two is a reflection of section one, about f_0. The center frequencies are found by Eq. 7.

Eq. 7

$$M = \frac{\alpha\omega_1 Q_1}{2Q_0} + \sqrt{\left(\frac{\alpha\omega_1 Q_1}{2Q_0}\right)^2 - 1}$$

Where $M = \dfrac{\omega_1}{\omega_0} = \dfrac{\omega_0}{\omega_2} = \dfrac{f_1}{f_0} = \dfrac{f_0}{f_2}$ $\quad M = 1.0955$, $f_1 = 2317.6$, $f_2 = 1931.1$

for Section 3 the real pole is transformed into a complex pole pair.

$$Q_3 = \frac{2Q_0}{\alpha\omega_B} = 10.7$$

and $f_3 = f_0$.

The 3 filter stages are now defined:

$f_1 = 2317.6$ $\quad Q_1 = 21.49$
$f_2 = 1931.1$ $\quad Q_2 = 21.49$
$f_3 = 2115.56$ $\quad Q_3 = 10.7$

In this example, the multiple feedback approach is used since 3-pole pairs can be generated with 3 op amps, 6 capacitors, and 9 resistors; an equivalent filter could have been designed with the state-variable, but this would have required 9 op amps to realize. The actual filter is shown in Figure 8. All capacitor values are chosen to be .01 μF (5%), and all resistors are 1%. The values for this filter and a low-band filter are shown in Table 6.

Figure 9 shows a complete Originate or Answer modem. The values for the XR-2206 and XR-2211 are given

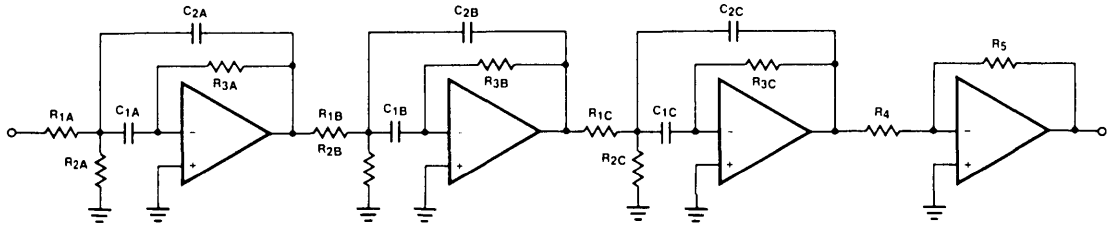

Figure 8. Modem Filter.

Table 6.

		f_0	ω_0	Q_0	R_1	R_2	R_2	C_1	C_2	H_0
Originate	A	1931.1	12.1335K	21.49	88.6K	192	354K	.01	.01	2
	B	2317.6	14.562K	21.49	74K	160	295K	.01	.01	2
	C	2115.6	13.293K	10.7	40K	355	161K	.01	.01	2
Answer	A	1362.26	10.115K	11.827	58.5K	421	234K	.01	.01	2
	B	975.51	6129.3	11.827	96.5K	421	386K	.01	.01	2
	C	1152.78	7.243K	5.832	40.3K	1219.5	161K	.01	.01	2

in Table 7. For an originate modem, the transmitting frequencies are 1070 and 1270, and the receiving frequencies are 2025 and 2225, for a space and mark, respectively.

The first op-amp is connected as an active hybrid which should supply a minimum of 10 dB isolation, from transmit to receive, while adding 6 dB from the line to the receiver.

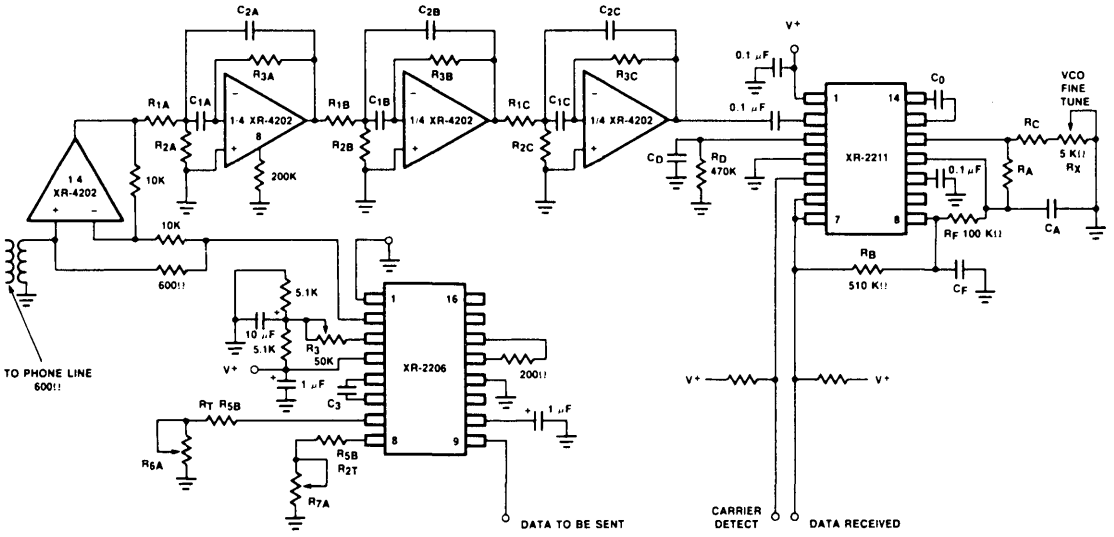

Figure 9. Originate or Answer Modem.

Table 7. Recommended Component Values for Typical FSK Bands

FSK Band			Component Values											
			XR-2206					XR-2211						
Baud Rate	f_L	f_H	R_{6A}	R_{6B}	R_{7A}	R_{7B}	C_3	R_X	R_C	R_A	C_0	C_A	C_F	C_D
Originate	1070	1270	10	18	10	20	.039	10	18	100	.039	.01	.005	.05
Answer	2025	2225	10	16	10	18	.022	10	18	200	.022	.0047	.005	.05

Units: Frequency — Hz; Resistors — kΩ; Capacitors — μF.

XR-C277 Low-Voltage PCM Repeater IC

INTRODUCTION

The XR-C277 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Mega bits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of −40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Build-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The key feature of the XR-C277 is its ability to operate with low supply voltages (6.3 volts and 4.4 volts) with a supply current of less than 13 mA. Compared to conventional repeater designs using discrete components, the XR-C277 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

FUNDAMENTALS OF PCM REPEATERS

Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator. The XR-C277 monolithic IC replaces about 90% of the electronic components and circuitry within the digital repeater sections of Figure 1. Thus, a bi-directional repeater system would require two XR-C277 IC's, one for each direction of information flow.

Figure 2 shows the functional block diagram of one of the digital repeater sections, along with the external zener regulator. The basic system architecture shown in the figure is the same as that utilized in the design of the XR-C277 monolithic IC.

In terms of the functional blocks shown in Figure 2, the basic operation of the repeater can be briefly explained as follows:

The bipolar signal, after traversing through a dispersive, noisy medium, is applied to a linear amplifier and automatic equalizer. It is the function of this circuit to provide the necessary amount of gain and phase equalization and, in addition, to band limit the signal in order to optimize the performance of the repeater for near-end crosstalk produced by other systems operating within the same cable sheath.

The output signals of the preamplifier which are balanced and of opposite phases are applied to the clock extraction circuit and also to the pulse regenerator. The signals applied to the clock extraction circuit are rectified and then applied to a high-Q resonant circuit. This resonant circuit extracts a 1.544 MHz frequency component from the applied signal. The extracted signal is first amplified and then used to control the time at which the output signals of the preamplifier are sampled and also to control the width of the regenerated pulse.

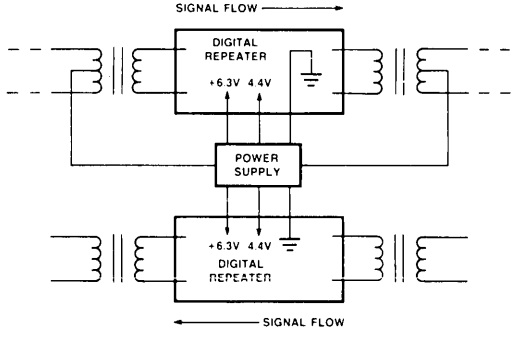

Figure 1. Block Diagram of a Bi-Directional Digital Repeater System

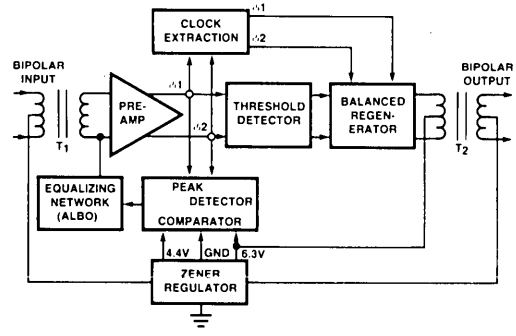

Figure 2. Functional Block Diagram of a Digital PCM Repeater System

It is the function of the pulse regenerator to perform the sampling and threshold operations and to regenerate the appropriate pulse. The regenerated pulse in turn applied to a discrete output transformer which is used to drive the next section of the paired cable.

Additional References on PCM Repeaters:

1. Mayo, J. S., "A Bipolar Repeater for Pulse Code Signals," B.S.T.J., Vol. 41, January, 1962, pp. 25-97.
2. Aaron, M. R., "PCM Transmission in the Exchange Plant," B.S.T.J., Vol. 41, January, 1962, pp. 99-143.
3. Davis, C. G., "An Experimental Pulse Code Modulation System for Short-Haul Trunks," B.S.T.J., Vol. 41, January, 1962, pp. 1-25.
4. Fultz, K. E. and Penick, D. B., "The T-1 Carrier System," B.S.T.J., Vol. 44, September, 1965, pp. 1405-1452.
5. Tarbox, R. A., "A Regenerative Repeater Utilizing Hybrid IC Technology," Proceedings of International Communications Conference, 1969, pp. 46-5 — 46-10.

OPERATION OF THE XR-C277

The XR-C 277 combines all the functional blocks of a PCM repeater system in a single monolithic IC chip. The pin connections for each of the functional circuits within the repeater chip are shown in Figure 3, for a 16-pin dual-in-line package.

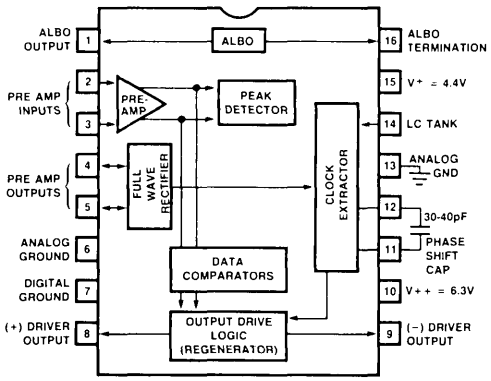

Figure 3. Package Diagram of XR-C277 Monolithic PCM Repeater

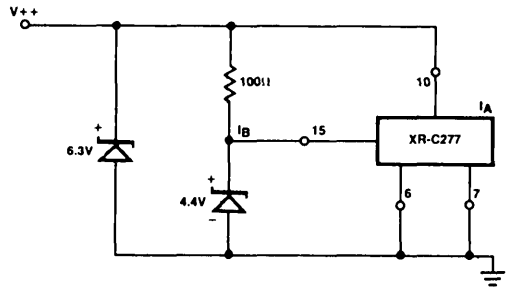

Figure 4. Recommended Supply Voltage Connection for XR-C277 (Note: See Figure 6 for Recommended Bypass Capacitors)

The circuit is designed to operate with two positive supply voltages, V^{++} and V^{+} which are nominally set to be 6.3V and 4.4V, respectively. Figure 4 gives the recommended power supply connection for the circuit.

The supply currents 1_A and 1_B drawn from the two supply voltages applied to the chip are specified to be within the following limits:

a. Current from 6.3V supply voltage, I_A:

$$2.5\ mA \leq I_A \leq 4.0\ mA$$

b. Current from 4.4V supply voltage I_B:

$$7\ mA \leq I_B \leq 9\ mA$$

The external components necessary for proper operation of the circuit are shown in Figure 5, in terms of the system block diagram. Note that all the blocks shown in Figure 5 are a part of the monolithic IC; and the numbered circuit terminals correspond to the IC package pins (see Figure 3).

Figure 6 shows a practical circuit connection for the XR-C277 in an actual PCM repeater application for 1.544 Mbps T-1 Repeater application. For simplification purposes, the lightning protection circuitry and the second repeater section are not shown in the figure.

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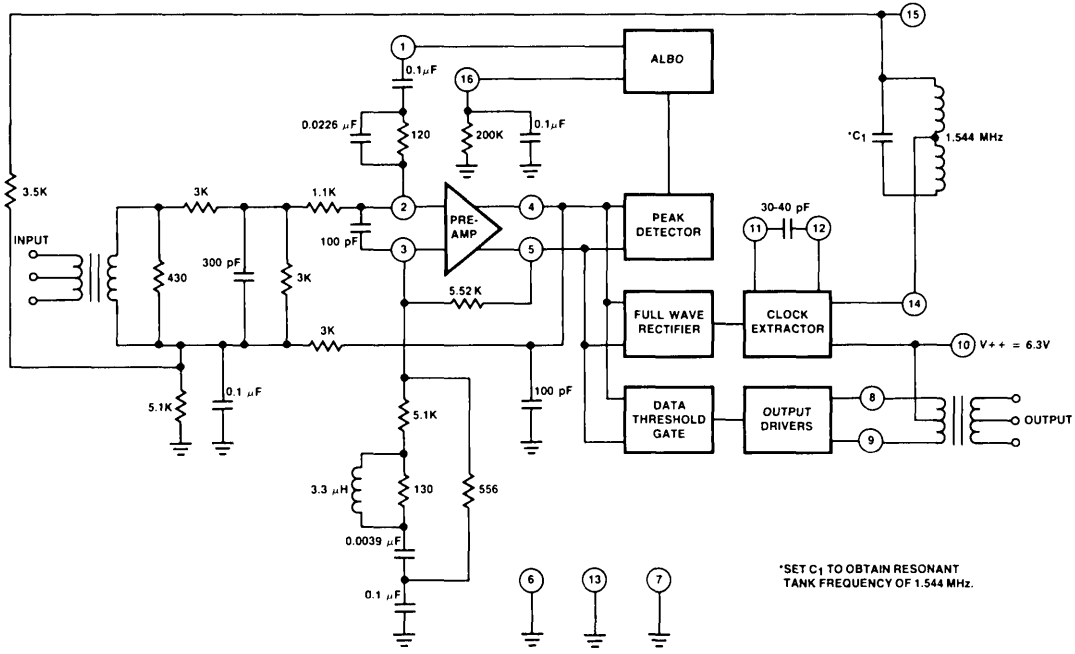

Figure 5. External Components Necessary for Circuit Operation in 1.544 MHz T-1 Repeater

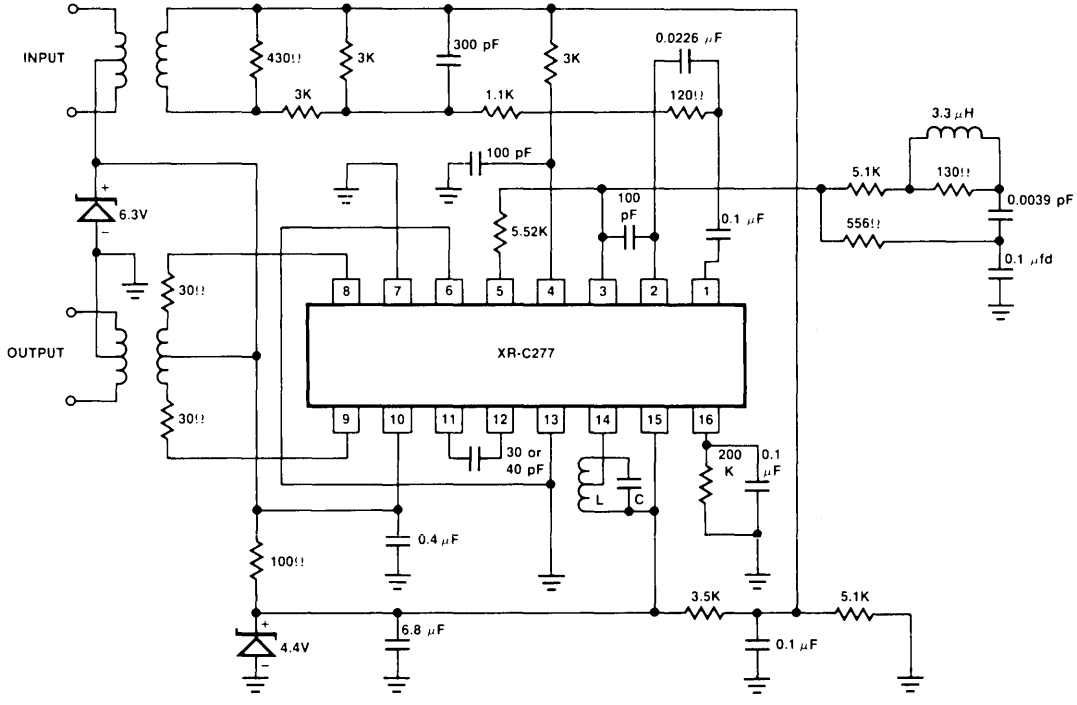

Figure 6. Typical Circuit Connection of XR-C277 in 1.544 MHz T-1 Repeater System. (Note: Set L and C to Form a High Q Tank Resonant at 1.544 MHz. It is Recommended that Q∂100, and C ≈ pF for most applications).

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Fig. 7):

The circuit diagram of the preamplifier section is shown in Figure 7. This section is designed as a two-stage differential amplifier with a broadband differential voltage gain of 52 dB. The differential outputs of the preamplifier, Pins 4 and 5, are internally connected to the peak-detector, full-wave rectifier and the data threshold detector sections of the XR-C277.

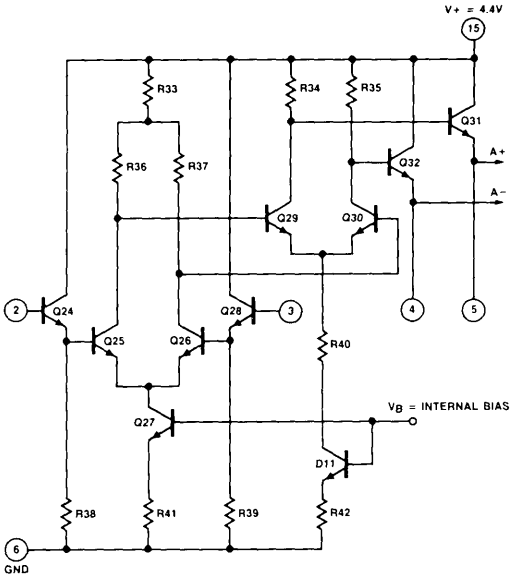

Figure 7. Circuit Diagram of Preamplifier Section

Automatic Line Build-Out (ALBO) Section (Fig. 8):

The ALBO function is achieved by controlling the dynamic impedance of ALBO diodes (Q_{21} and Q_{22}). The current which sets this dynamic impedance is supplied through Q_{21} and is controlled by the peak-detector output level applied to base of Q_{23}.

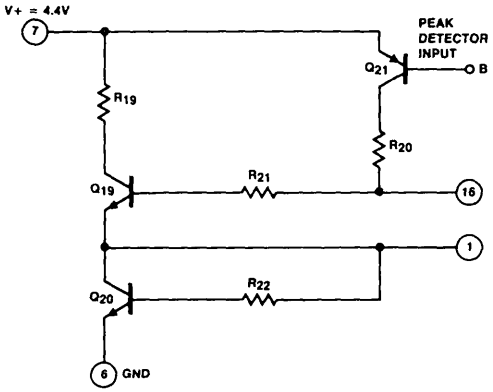

Figure 8. Automatic Line Build-Out (ALBO) Section

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Data-Threshold Detector; Full-Wave Rectifier and Peak Detector Sections (Figure 9):

The level detector and peak rectifier sections of the XR-C277 are made up of two sets of gain stages which are driven differentially with the (A^+) and (A020−) outputs of the preamplifier section. The outputs of the data threshold comparators, D^+ and D^- activate the data latches shown in Figure 11.

The peak-detector output, terminal B of Figure 9, is internally connected to the Automatic Line Build-Out (ALBO) section of the circuit and controls the dc bias current through the ALBO diodes Q_{21} through Q_{22}, as shown in Figure 8.

The full-wave rectifier output is internally connected to the clock-extractor section of the repeater and provides the excitation signal for the L-C tuned tank circuit (Pin 14) of the injection locked oscillator. The detection thresholds of the comparators are set by the resistor chains (R_{45}, R_{47}, R_{51}, R_{55}) and (R_{46}, R_{48}, R_{52}, R_{56}). The resistor ratios are chosen such that the data threshold is 50% of the ALBO threshold; and the clock extractor threshold is 73% of the ALBO threshold.

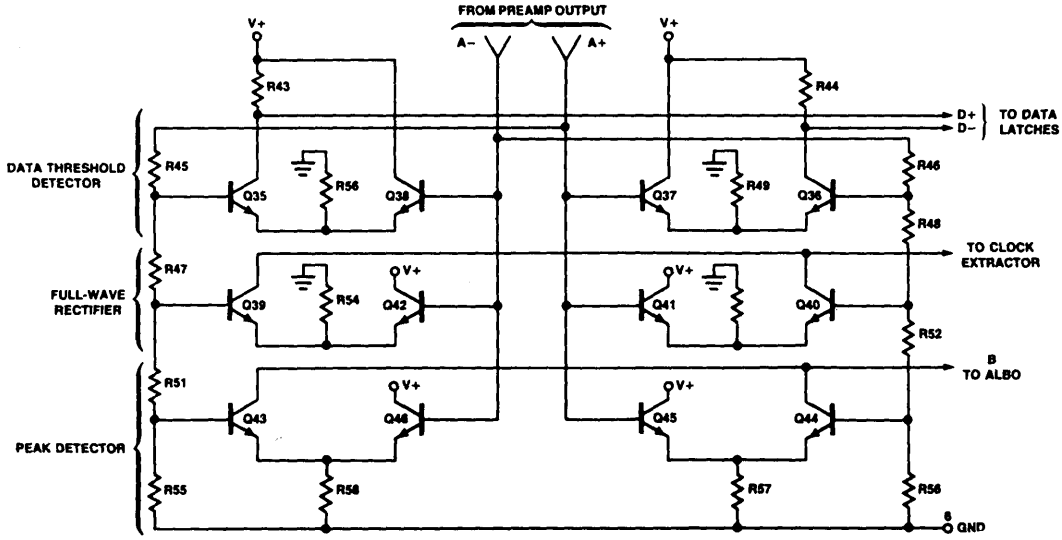


Figure 9. Data-Threshold Detector, Full-Wave Rectifier and The Peak Detector Sections of XR-C277

Clock Extractor Section (Figure 10):

The clock-extractor section of XR-C277 is designed as an injection locked oscillator as shown in the circuit schematic of Figure 10. The excitation is applied to the emitter of Q_{1B}, from the output of the full-wave rectifier. This signal in turn controls the current in the resonant L-C tank circuit connected to Pin 14. The sinusoidal waveform across the tank is then amplified and squared through two cascaded differential gain stages made up transistors Q_3 through Q_9. The output swing of the second gain stage is integrated by the phase-shift capacitor, C_1, externally connected to Pins 11 and 12. See timing diagrams of Figure 13. The nominal value of this capacitor is in the 30 to 40 pF range. The triangular waveform across Pins 11 and 12 is at quadrature phase with the sinusoidal voltage swing across the L-C tank circuit. This waveform is then used to generate the strobe signal, C_p, and the clock pulse C_ϕ, which are applied to the data latches of the logic section.

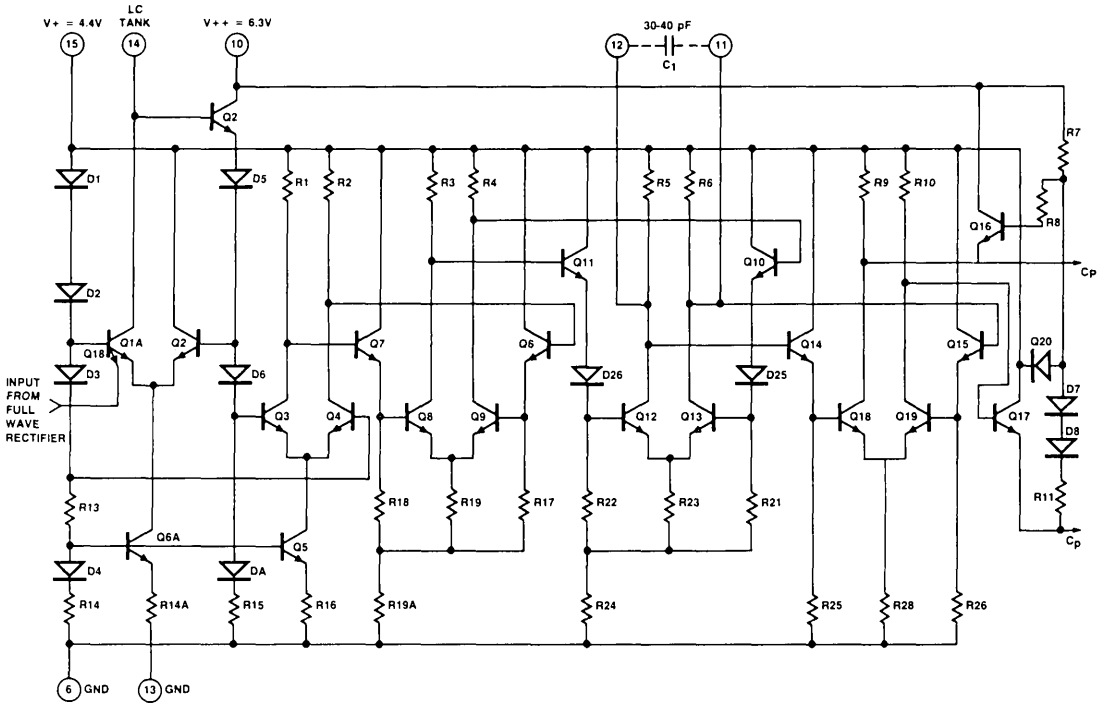


Figure 10. Circuit Diagram of Clock Extractor Section

Data-Latch and Output Driver Sections (Figures 11 and 12):

The data-latch section consists of two parallel flip-flops, driven by the D^+ and D^- inputs from the data-threshold detector. When the D^+ input is at a low state, the sampling or strobe pulse, C_p, is steered through Q_{47A} and sets Flip-Flop 1, on the leading edge of C_p. Conversely, when D^- input is at a low state, the sampling pulse is steered through Q_{47B} to set Flip-Flop 2. Each flip-flop section is then reset at the trailing edge of the clock pulse input, C_ϕ. The flip-flop outputs, (F_1, F_1) and F_2, F_2) are then used to drive the output drivers. This logic arrangement results in an output pulse width which is the same as the extracted clock pulse width (See timing diagram of Figure 13.)

The outputs of the two data latches drive the two output driver stages shown in Figure 12. The high-current outputs of the driver stage, Pins 8 and 9, are connected to the center-tapped output transformer as shown in Figure 5. The voltage swing across the output is one diode drop (V_{BE}) less than the supply voltage at Pin 10. The output stages are designed to work into a nominal load impedance of 100 ohms, and can handle peak load currents of 30 mA.

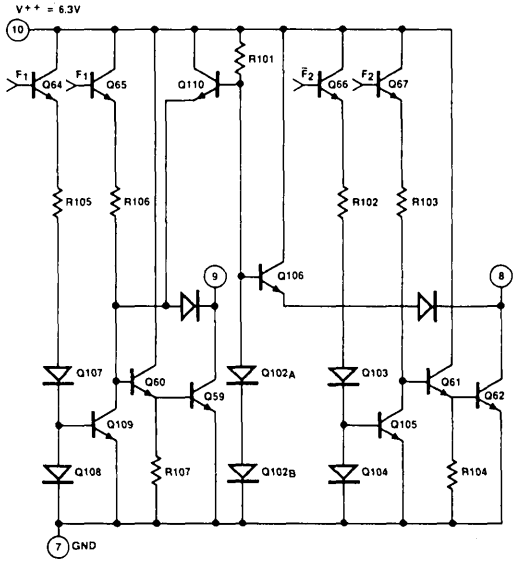


Figure 11. Data-Latch Section of XR-C277

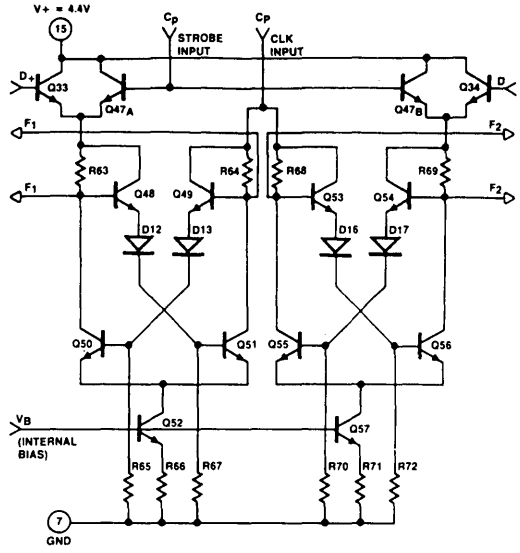


Figure 12. Output-Driver Section

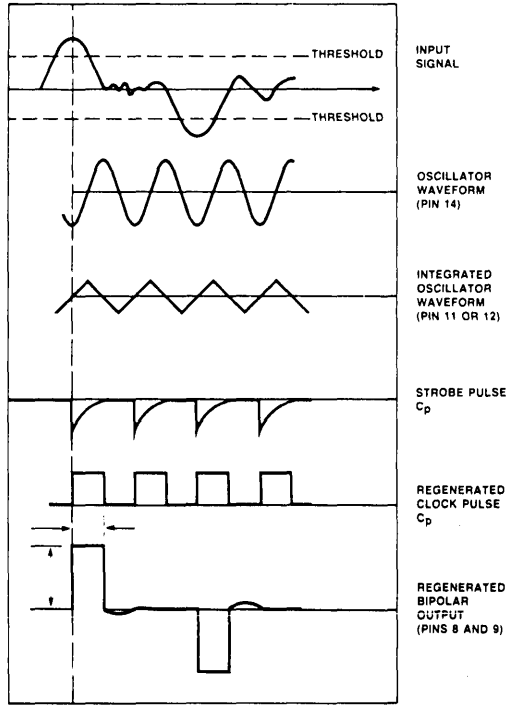


Figure 13. Typical Timing Waveforms for a 1—0—1 Input Data Pattern

Three-State FSK Modem Design using XR-2207 and XR-2211

INTRODUCTION

This application note describes the design principle, and the operation of three-state frequency-shift keyed (FSK) modems for industrial process control systems. Compared to conventional bi-state modems, which utilize only the mark and space frequencies, the three-state modems utilize a third frequency, the carrier signal, for additional command and control functions. This carrier-control feature allows each modem system connected to a central processor (CPU) to be interrogated or activated, one at a time, without interference from the other modem transmitters or receivers within the same system.

The design and operation of conventional bi-state FSK modems using the XR-2206 modulator, and the XR-2211 demodulator, are covered in Exar's Application Note, AN-01. This application note extends these basic concepts to the design of FSK modulators or demodulators with three-state operation capability.

PRINCIPLES OF OPERATION

In a wide variety of industrial process control applications, it is necessary to have a number of separate sensors and controllers activated by a centralized computer or processing unit (CPU). This can be achieved by operating a number of separate FSK modulator/demodulator (modem) stations over a common set of telephone lines, and address them one at a time from the CPU. The simplified block diagram of such a process controlled system is shown in Figure 1. In many such cases, such a process control system also makes use of the distributed-intelligence concept by employing a separate data acquisition system at each control station. Such an intelligent data acquisition system is normally made up of a microprocessor, along with its A/D and D/A converter circuitry, which will interface with the sensors and the control machinery. An FSK modem will interface with the telephone wires going back to the central command unit, the CPU.

In the conventional operation of FSK modems, they operate in their bi-state mode, i.e., the information to be transmitted or received is available in two states, corresponding to either a mark or a space frequency. In a complex process control system, such as the one shown in Figure 1, the versatility of the system can be greatly enhanced by operating the FSK modulator/demodulator in three-state mode, where the information to be transmitted or received is available in three states, i.e., a mark or space frequency, or a carrier signal, which is normally a tone having a frequency halfway between the mark and space frequencies.

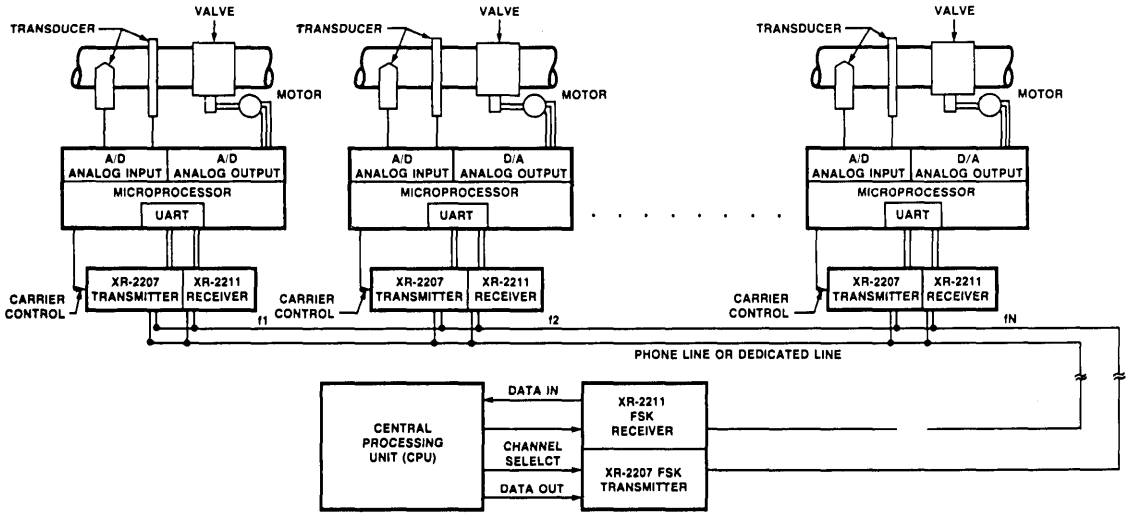


Figure 1. Simplified Block Diagram of a Complex Process Control System with Multiple FSK Modems.

Figure 2 shows a detailed block diagram of a complete three-state FSK modem system. The system is made up of five blocks:

(a) FSK transmitter or encoder which converts the input data or logic signals into transmitted mark, space, and carrier tones.

(b) FSK receiver or decoder which converts the frequency signals sent over the telephone lines into binary logic signals.

(c) Transmitter bandpass filter which band-limits the frequency output of the transmitter to the allocated transmitter bandwidth.

(d) Receiver bandpass filter which limits the incoming signals to those frequencies which fall within the allocated receiver bandwidth.

(e) A line hybrid, or a 4-wire to 2-wire transformer, which isolates or decouples the transmitter output from the receiver input.

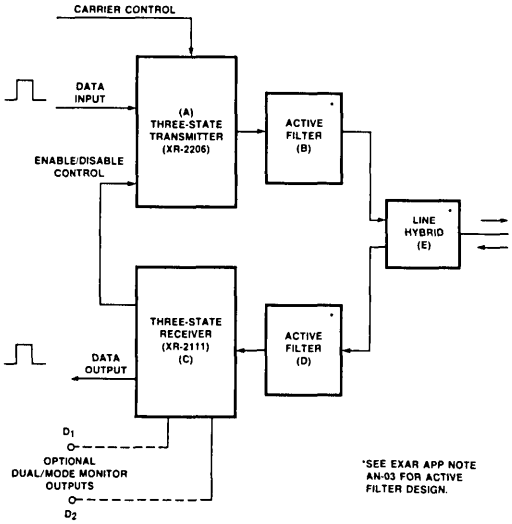


Figure 2. Block Diagram of a Three-State FSK Modem System.

The first 2 blocks, the FSK transmitter and the receiver, are the essential part of the modem system. The remaining three blocks, namely the active filters and the line-hybrid, are support circuits, depending on the frequency-band requirements or the necessary telephone line interconnections. Detailed descriptions and design examples for these active filters are given in Exar's Application Note, AN-03.

The three-state modem is designed to operate in two separate frequency bands: A transmit-band for the transmitted data, and a receive-band for the incoming frequencies. In certain operating modes, such as the half-duplex operation, these frequency bands may be one and the same. In its most general case, the frequency information associated with the three-state modem system (Figure 2) is concentrated in three discrete frequencies in each of the transmit- and receive-bands. These are:

Transmit-Band (transmitter output):

f_{T1} = Transmitter mark frequency

f_{T2} = Transmitter space frequency

f_{T0} = Transmitter carrier or center frequency

Receive-Band (receiver input):

f_{R1} = Receiver mark frequency

f_{R2} = Receiver space frequency

f_{R0} = Receiver carrier or center frequency

Normally, the mark and space frequencies are chosen to be near the opposite edges of the receive- or transmit-band, and the carrier frequency is chosen to be at the center of the corresponding band.

When activated by the enable/disable control, the three-state transmitter generates either the FSK mark/space frequencies, f_{T1} and f_{T2}, or the carrier frequency, f_{T0}. The carrier frequency is activated by the carrier control input, and can override the input data.

The three-state receiver provides two outputs: A binary data output, when activated by the input mark/space frequencies, f_{R1} and f_{R2}, and a logic signal, to control or enable the transmitter when the receiver-carrier frequency, f_{R0}, is present. As an option, it may have a dual-mode operation capability which can provide serial data outputs for half-bandwidth deviations of the input signal, i.e., for FSK signals comprised of center-to-mark or center-to-space frequency shifts. The data outputs corresponding to this mode of operation are shown as outputs, D_1 and D_2 of Figure 2.

CIRCUIT OPERATION

The generalized three-state modem system of Figure 2 can operate in a multiplicity of modes. Some of these are outlined below:

Answerback Under CPU Control

The modem will be in a standby mode with the transmitter disabled, and the receiver in a standby condition with its data output disabled. It will be activated only when an interrogate tone at the receiver center frequency, f_{R0}, is transmitted by the control modem unit associated with the CPU (see Figure 1). This tone is detected by the receiver; it activates the transmitter via its enable/disable control, and instructs the local microprocessor to transmit its status information via the local transmitter. This data is transmitted as an FSK signal made up of the transmit mark and space frequencies f_{T1} and f_{T2}. When the information transmission is complete, or when the interrogate tone is discontinued, the entire modem system again reverts back to its standby mode.

Receive Under CPU Control

In this mode of operation, the transmitter remains disabled, the receiver is at its standby mode with its data output disabled. When the FSK data is sent by the CPU modem transmitter, at the mark/space frequencies, f_{R1} and f_{R2}, the data output is enabled, and the decoded binary data is fed into the local microprocessor. Since the center receive-frequency, f_{R0}, is not transmitted, the transmitter remains disabled.

Priority-Transmit Request

In an emergency situation, the local transmitter can be activated by its carrier-control input, which causes it to transmit a tone, f_{T0}, at its center frequency. When this tone is received by the CPU, it will be treated as a priority request to transmit information; the CPU will immediately interrogate the corresponding local modem by sending out its address tone at frequency, f_{R0}.

Dual-Channel Receive

As an option, the receiver can provide serial data outputs, through separate terminals, D_1 and D_2 of Figure 2, for half-bandwidth deviations of the input FSK signals. In this mode, the input data will be in the form of center-to-mark frequency shifts for one channel, and center-to-space shifts for the other. This mode of operation allows two separate sets of data or control instructions to be transmitted within the same channel bandwidth, provided that only one of these channels is used at any one time.

Dual-Channel Transmit

As an option, the transmitter can also transmit two separate channels, using half-bandwidth deviations of the transmit signal. In this case, the outgoing data will be encoded with center-to-mark transitions of the transmitter frequency in one of the channels, and center-to-space transitions in the other. However, similar to the case of the receiver, only one or the other, and not both, of these half-bandwidth channels can be on at a given time.

XR-2207 As A Three-State FSK Transmitter

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) circuit with excellent temperature stability. It provides simultaneous triangle and square wave outputs, and can be keyed to any one of four preprogrammed frequencies by means of external logic signals. These four discrete frequencies are preprogrammed by the choice of four external timing resistors.

Figure 3 shows a functional block diagram of the XR-2207 monolithic FSK generator chip. The circuit is comprised of four functional blocks: A variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs, and buffer amplifiers for both the triangle and square wave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors, to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals.

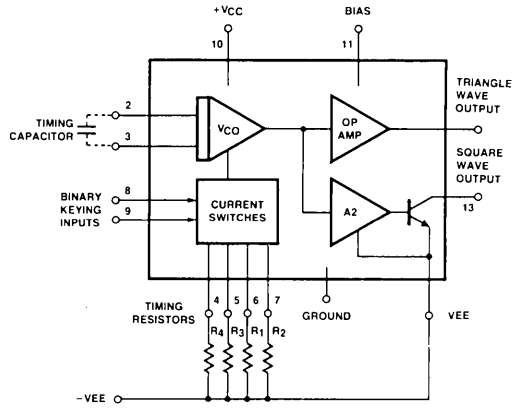


Figure 3. Functional Diagram of XR-2207 Monolithic FSK Generator.

The frequency of oscillation is set by an external timing capacitor, and by the combination of one or more of the external timing resistors, R_1 through R_4. The keying terminals switch these external resistors in and out of the circuit and thus control the operating frequency. Table 1 shows the four discrete frequencies which can be obtained as a function of four logic states at Pin 8 and 9. It should be noted that the frequency is inversely proportional to the timing resistor connected to the activated timing pin. For example, if only one of the timing pins, say Pin 5, is activated and its associated resistor, R_3, is left open-circuited (i.e., $R_3 = \infty$) the oscillator will be keyed OFF since this corresponds to a zero-frequency state.

Table 1.
Output Frequency of the XR-2207 as a Function of the Keying Logic.

Logic Level		Active Timing Resistor	Output Frequency
Pin 8	Pin 9		
L	L	Pin 6	$\frac{1}{C_0R_1}$
L	H	Pin 6 and 7	$\frac{1}{C_0R_1} + \frac{1}{C_0R_2}$
H	L	Pin 5	$\frac{1}{C_0R_3}$
H	H	Pin 4 and 5	$\frac{1}{C_0R_3} + \frac{1}{C_0R_4}$

(* Frequency in Hz, R in Ohms and C in Farads.)

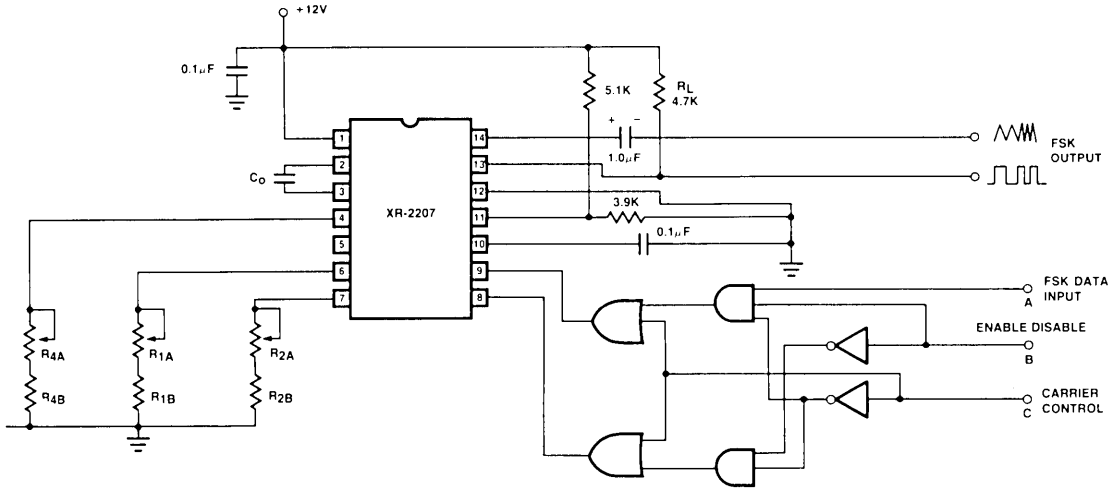


Figure 4. Three-State FSK Transmitter Using the XR-2207.

Figure 4 shows the recommended circuit connection of the XR-2207, for its operation as a three-state FSK transmitter. The three resistors, R_1, R_2 and R_4, are used to set the three discrete frequencies to be transmitted in accordance with the frequency expressions given in Table 1, where:

$$f_{T1} = \frac{1}{C_0R_1} \quad f_{T2} = \frac{1}{C_0R_1} + \frac{1}{C_0R_2} \quad f_{T0} = \frac{1}{C_0R_4}$$

It should be noted that Pin 5 is left open circuited (i.e., $R_3 = \infty$). This allows the circuit to be keyed OFF, or disabled, by applying a high-logic state to Pin 8, and a low-logic state to Pin 9 (see Table 1).

The functions of the three control terminals can be described as follows:

a. **FSK Data Input:** The serial binary data is applied to this terminal. With the carrier control at low- and enable/disable control at high-state, the binary data causes the transmitter to generate the mark and space frequencies, f_{T1} and f_{T2}.

b. **Enable/Disable Control:** When this input is at low-state, the transmitter is disabled.

c. **Carrier-Control:** When this terminal is at high-state, the transmitter generates a continuous tone at frequency, f_{T0}.

With the external logic circuitry shown in Figure 4, carrier-control can override both the enable/disable or the FSK data inputs. A detailed truth-table of the circuit outputs is given in Table 2, for various states of the three control inputs.

Table 2.
Three-State Transmitter Operating Modes as a Function of Control Inputs

Control Input States			Level at Pin 9	Level at Pin 9	Transmitter Output Frequency	Transmitter Operating Mode
A	B	C				
L	L	L	L	H	OFF	Transmitter Off
H	L	L	L	H	OFF	
L	H	L	L	L	f_{T1}	Transmit Data
H	H	L	H	L	f_{T2}	
L	L	H	H	H	f_{T0}	Transmit Carrier Only
L	H	H	H	H	f_{T0}	
H	H	H	H	H	f_{T0}	

XR-2211 As A Three-State Receiver

The XR-2211 is a monolithic FSK demodulator which operates on the phase-locked loop principle. In addition to the basic PLL system, the monolithic chip also contains a quadrature-detector circuit which produces a logic signal when a carrier signal, or tone, is present within the capture range of the PLL. A simplified functional block diagram of the circuit is shown in Figure 5.

Basic Bi-State Operation

The basic operation of the XR-2211, in conventional bi-state modems, is described in detail in Exar's Application Note, AN-01. It will be briefly reviewed below.

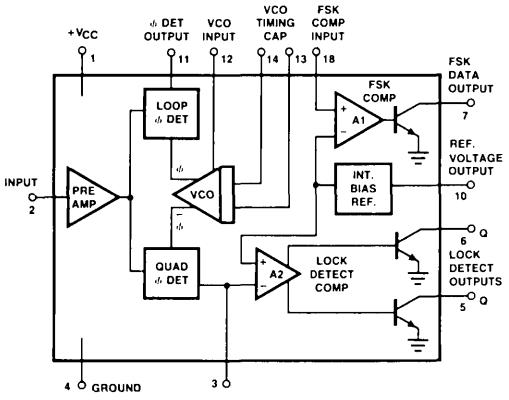


Figure 5. Functional Block Diagram of XR-2211 FSK and Tone Detector.

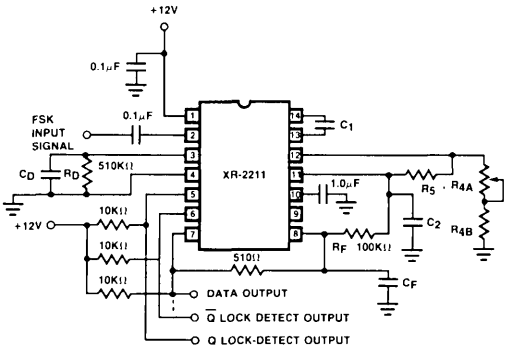


Figure 6. XR-2211 as a Bi-State Receiver with Tone-Detection Capability.

The basic circuit connection for the XR-2211 for bi-state FSK detection is shown in Figure 6. The center frequency is determined by $f_0 = (1/C_1R_4)$ Hz, where capacitance is in farads and resistance is in ohms. Calculations for f_0 should fall midway between the mark and space frequencies.

The tracking range ($\pm\Delta f$) is the range of frequencies over which the phase-locked loop can retain a lock with a swept input signal. This range is determined by the formula:

$$\Delta f = (R_4 f_0/R_5)\ \text{Hz}.$$

Δf should be made equal to, or slightly less than, the difference between the mark and space frequencies. For optimum stability, the recommended range of values for R_4 is between 10 kΩ and 100 kΩ.

The capture range ($\pm\Delta f_C$) is the range of frequencies over which the phase-locked loop can acquire lock. It is always less than the tracking range. The capture range is limited by C_2, which, in conjunction with R_5, forms the loop-filter time constant. In most modern applications, Δf_C is chosen to be ≈80% to 95% of the tracking range, Δf.

The bi-state FSK data filter, made up of R_F and C_F, removes the jitter from the demodulated FSK signal. Similarly, the lock-detect filter capacitor (C_D) removes chatter from the lock-detect output. With R_D = 510 kΩ, the minimum value of C_D can be determined by: $C_D(\mu f)$ ≈16/capture range in Hz. The XR-2211 has three npn open-collector outputs, each of which is capable of sinking up to 5 mA. Pin 7 is the FSK data output, Pin 5 is the Q lock-detect output which toes low when a carrier is detected, and Pin 6 is the Q lock-detect output which goes high when lock is detected. If Pin 6 and 7 are wired together, the output signal from these terminals will provide data when FSK is applied, and will be low when no carrier is present.

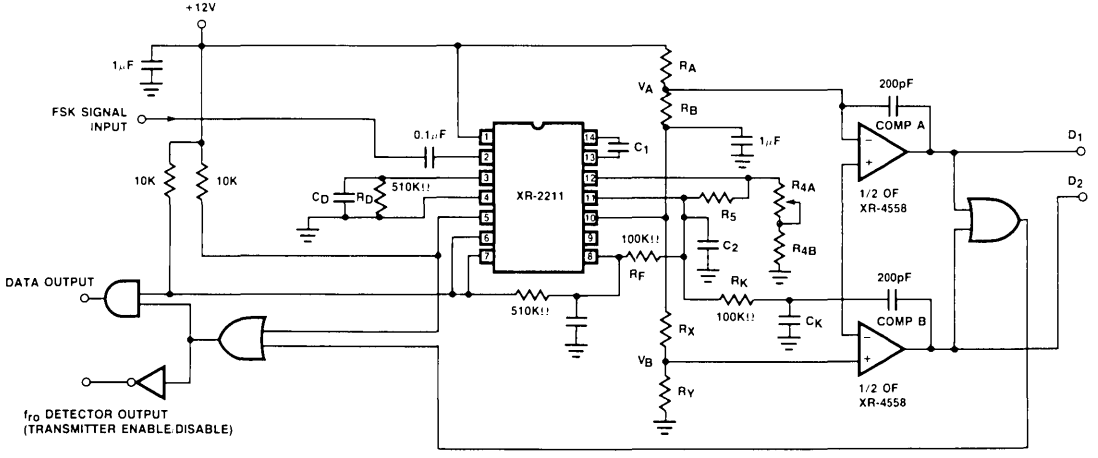


Figure 7. Circuit Connection for Operating XR-2211 as a Three-State FSK Receiver.

Three-State Operation

The XR-2211 FSK demodulator circuit can be made to operate as a three-state receiver (see Block B of Figure 2), using the circuit configuration shown in Figure 7. With reference to the Figure, the basic operation of the circuit can be described as follows: The basic FSK decoding function, converting the incoming mark and space signals at frequencies f_{R1} and f_{R2}, is performed in the same manner as in the bi-state case, and the resulting output is available at Pin 7 of XR-2211. Pin 7 is connected to the tone-detect output, and then gated by the complement of the carrier-detect output. Thus, the data output terminal will be enabled only when the mark and space frequencies are present, but not when the receive-carrier, f_{R0}, is present.

The external voltage comparators shown in Figure 7 are added to the circuit to distinguish PLL output voltage levels corresponding to various input frequencies. The function of the XR-2211 frequency-to-voltage transfer characteristics can be understood by referring to Pin 11 in Figure 8. The voltage levels and polarities shown are relative to the XR-2211 internal reference voltage, V_{10}, at Pin 10. The mark and space frequencies, f_{R1} and f_{R2}, generate the maximum dc level shifts. V_{R1} and V_{R2}, sensed by the internal FSK comparator (see Figure 5) which is internally biased from the reference voltage, V_{10}.

The external comparators, Comp. A and Comp. B of Figure 7, are biased at voltage levels, V_A and V_B, approximately halfway between V_{R1} and V_{R2}, to trip at frequencies f_A and f_B, which are halfway between mark-to-center and space-to-center frequency shifts. This biasing is achieved with the external resistive dividers, R_A, R_B, R_X, and R_Y of Figure 7, which generate the reference voltage levels, V_A and V_B, with respect to the XR-2211 internal reference at Pin 10. It should be noted that the value of the resistors (R_A + R_B) and (R_X + R_Y) must be as large as possible (typically in excess of 100 kΩ) to avoid disturbing the voltage level at Pin 10.

The output of Pin 11 is filtered by R_K and C_K, and is used to drive the external voltage comparators. The outputs of these comparators are then connected through the external logic gates, to produce the carrier-detect or the enable/disable signal. The resulting logic output will be noramlly at a low state, and will go high only when the carrier signal, f_{R0}, is present. This logic signal is normally used for transmitter enable/disable control, as shown in Figure 2.

The logic level changes, at the external comparator outputs, correspond to mark-to-carrier or space-to-carrier frequency shifts (see Figure 8); thus, these outputs can be utilized as optional dual-mode monitor outputs, D_1 and D_2 of Figure 2.

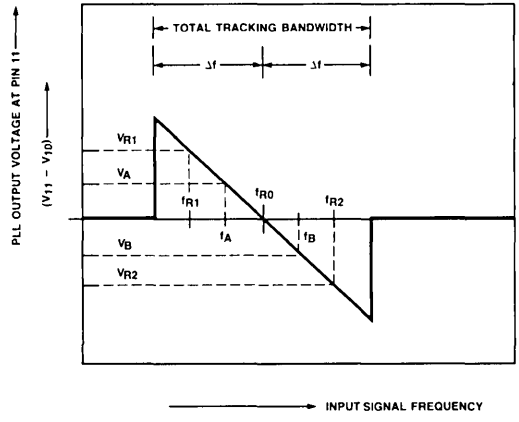


Figure 8. XR-2211 Frequency-to-Voltage Transfer Characteristics. (Note: V_{11} and V_{10} are the dc voltage levels at Pins 11 and 10, respectively.)

Precision PLL System using the XR-2207 and the XR-2208

INTRODUCTION

The phase-locked loop (PLL) is a versatile system block, suitable for a wide range of applications in data communications and signal conditioning. In most of these applications, the PLL is required to have a highly stable and predictable center frequency and a well-controlled bandwidth. Presently available monolithic PLL circuits often lack the frequency stability and the versatility required in these applications.

This application note describes the design and the application of two-chip PLL system using the XR-2207 and the XR-2208 monolithic circuits. The XR-2207 is a precision voltage controlled oscillator (VCO) circuit with excellent temperature stability (±20 ppm/°C, typical) and linear sweep capability. The XR-2208 is an operational multiplier which combines a four quadrant multiplier and a high gain operational amplifier in the same package. Both circuits are designed to interface directly with each other with a minimum number of external components. Their combination functions as a high performance PLL, with the XR-2207 forming the VCO section of the loop, and the XR-2208 serving as the phase-detector and loop amplifier.

As compared with the presently available single-chip PLL circuits such as the XR-210 or the Harris HI-2820, the two-chip PLL system described in this paper offers approximately a factor of 10 improvement in temperature stability and center frequency accuracy. The system can operate from 0.01 Hz to 100 kHz, and its performance characteristics can be tailored to given design requirements with the choice of only four external components.

DEFINITIONS OF PLL PARAMETERS

The phase-locked loop (PLL) is a unique and versatile feedback system that provides frequency selective tuning and filtering without the need for coils or inductors. It consists of three basic functional blocks; phase comparator, low-pass filter, and voltage-controlled oscillator, interconnected as shown in Figure 1. With no input signal applied to the system, the error voltage, V_d, is equal to zero. The VCO operates at a set "free-running" frequency, f_0. If an input signal is applied to the system, the phase comparator compares the phase and frequency of the input signal with the VCO frequency and generates an error voltage, $V_e(t)$, that is related to the phase and frequency difference between the two signals. This error voltage is then filtered and applied to the control terminal of the VCO. If the input signal frequency, f_S, is sufficiently close to f_0, feedback causes

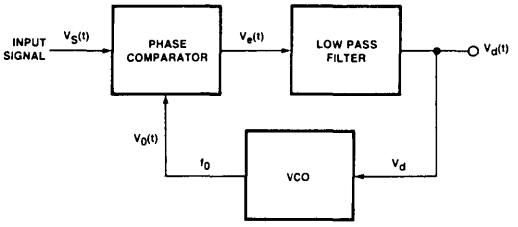


Figure 1. Block Diagram of a Phase-Locked Loop.

the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference.

Two key parameters of a phase-locked loop system are its "lock" and "capture" ranges. These can be defined as follows:

Lock Range = The band of frequencies in the vicinity of f_0 over which the PLL can *maintain lock* with an input signal. It is also known as the "tracking" or "holding" range. Lock range increases as the overall loop gain of the PLL is increased.

Capture Range = The band of frequencies in the vicinity of f_0 where the PLL can *establish* or *acquire lock* with an input signal. It is also known as the "acquisition" range. The capture is always smaller than the lock range. It is related to the low pass filter bandwidth and decreases as the low pass filter time constant increased.

The PLL responds to only those input signals sufficiently close to the VCO frequency, f_0, to fall within the "lock" or "capture" ranges of the system. Its performance characteristics, therefore, offer a high degree of frequency selectivity, with the selectivity characteristics centered about f_0. Figure 2 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly, over a broad frequency range covering both the "lock" and the "capture" ranges of the PLL. The vertical scale corresponds to the filtered loop error voltage, V_d, appearing at the VCO control terminal.

As the input frequency, f_S, is swept up (Figure 2(a)) the system does not respond to the input signal until the input frequency reaches the lower end of capture range, f_{CL}. Then, the loop suddenly locks on the input signal, causing a positive jump in the error voltage V_d. Next, V_d varies at a slope equal to the reciprocal of VCO

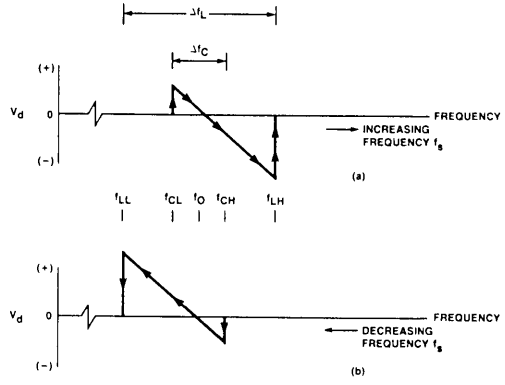


Figure 2. Frequency to Voltage Transfer Characteristics of a PLL System; (a) Increasing Input Frequency; (b) Decreasing Input Frequency.

voltage-to-frequency conversion gain, (K_V), and goes through zero at $f_S = f_0$. The loop tracks the input frequency until f_S reaches the upper edge of the lock range, f_{LH}. Then the PLL loses lock, and the error voltage drops to zero. If the input frequency is swept back slowly, from high towards low frequencies the cycle repeats itself, with the characteristics shown in Figure 2(b). The loop captures the signal at the upper edge of the capture range, f_{CH}, and tracks it down the lower edge of the lock range, f_{LL}. With reference to the figure, the "lock" and the "capture" ranges can be defined as:

$$\text{Lock Range} = \Delta f_L = f_{LH} - f_{LL}$$
$$\text{Capture Range} = \Delta f_C = f_{CH} - f_{CL}$$

The gain parameters associated with the PLL are defined as follows:

Phase Detector Gain, $K\phi$: Phase detector output per unit of phase difference between the two signals appearing at the phase detector inputs. It is normally measured in volts per radian.

VCO Conversion Gain, K_V: VCO frequency change per unit of input voltage. It is normally measured in radians/sec./volt.

Loop Gain, K_L: Total d_c gain around the feedback loop. It is equal to the product of $K\phi$ and K_V.

Loop Damping Factor, ζ: Defines the response of the loop error voltage V_d, to a step change in frequency. If $\zeta < 1$, the loop is underdamped; and the error voltage V_d will exhibit an underdamped response for a step change of signal frequency.

The lock range of the phase-locked loop is controlled by the loop gain, K_L. The capture range and the damping factor are controlled by both the loop gain and the low pass filter.

PRECISION PLL USING XR-2207 AND XR-2208

The XR-2207 VCO and the XR-2208 operational multiplier can be inter-connected as shown in Figure 3, to form a highly stable PLL system. The circuit of Figure 3 operates with supply voltages in the range of +12V to +26V; and over a frequency range of 0.01 Hz to 100 kHz. In the PLL system of Figure 3, all the basic performance characteristics of the PLL can be controlled and adjusted by the choice external 4 components identified as resistors R_0 and R_1, and the capacitors C_0 and C_1, C_0 and R_0 control the VCO center frequency; R_1 and C_1 determine the tracking range and the low pass filter characteristics. The two-chip PLL system can be readily converted to split supply operation by inter-connecting the circuit as shown in Figure 4. The PLL circuit of Figure 4 operates over a supply voltage range of ±6 volts to ±13 volts.

For best results, the timing resistor R_0 should be in the range of 5k to 100k, and $R_1 > R_0$. Under these conditions, the basic parameters of the PLL can be easily calculated from the design equations listed in Table 1.

Design Example

As an example, consider the design of a PLL system using the circuit of Figure 3, to meet the following nominal performance specifications:

a) Center Frequency = 10 kHz
b) Tracking Range = 20% (9 kHz to 11 kHz)
c) Capture Range = 10% (9.5 kHz to 10.5 kHz)

Solution:

a) Set Center Frequency:
Choose R_0 = 10k (Arbitrary choice for $5k < R_0 < 100k$)

Then, from equation 1 of Table 1:

$C_0 = (1/f_0R_0) = 0.01\ \mu F$

b) Set Lock Range:
From equation 2 of Table 1:

$R_1 = (0.45)\ R_0 = 45k$

c) Set Capture Range:
Since capture range is significantly smaller than Lock range, equation 8(a) applies.

Solving equation 8(a) for C_1, one obtains:

$C_1 = 0.032\ \mu F$

PRECISION SINE WAVE OUTPUT PLL USING XR-2208 AND XR-2206

The interconnection of the XR-2208 and XR-2206 as shown in Figure 5 forms a precision phase-locked loop system with a sine wave output. The phase-locked loop

characteristics are adjusted with the same four external components as previously described. Equation 2 in Table 1 is modified to:

(2) Lock Range $(\Delta f_L/f_0) = (0.5)(R_0/R_1)$

This change is because the reference of the XR-2206 is internally set. The clamp network with Q_1 has been added to adjust the swing to the VCO to compensate for this reference. The sine wave characteristics are adjusted by R_4 and R_5, which adjust sine-shaping and symmetry respectively. Sine wave distortion levels are typically 2.5% unadjusted with R_4 = 200Ω and R_5 open, and 0.5% adjusted using R_4 and R_5. Sine wave amplitude is adjusted by R_3 with the conversion gain equalling typically:

$$\frac{60mV_{P\text{-}P}}{K\Omega \text{ of } R_3}$$

The phase-locked loop input characteristics allow locking to input signal levels of 50 mV RMS to 2V RMS.

Table 1
Phase-Locked Loop Design Equations*

(1) Center Frequency: $f_0 = \frac{1}{R_0C_0}$ Hz	(7) Loop Damping: $= \frac{1}{2\sqrt{\tau K_L}} = \sqrt{\frac{2\,C_0}{C_1}}$
(2) Lock Range: $(\Delta f_L/f_0) = (0.9)(R_0/R_1)$	(8) Capture Range:
(3) Phase Detector Gain: $K\phi = 0.5\ V_{CC}$ volts/radian Where $V_{CC} = V^+$ for split supply; $V_{CC} = V^+/2$ for single supply.	a) Underdamped Loop ($\zeta < 1/2$): $(\Delta f_C/f_0) = \frac{0.8R_0}{R_1}\ \frac{C_0}{C_1}$
(4) VCO Conversion Gain: $K_V = \frac{1}{2\ V_{CC}C_0R_1}$ rad/sec/volt	b) Overdamped Loop ($\zeta > 1$): $(\Delta f_C/f_0) = 0.8(R_0/R_1)$
(5) Loop Gain: $K_L = K\phi K_V = \frac{0.25}{C_0R_1}$ sec^{-1}	*See Figures 3 and 4 for component designation.
(6) Low Pass Filter Time Constant: $\tau = \frac{C_1R_1}{2}$ sec.	

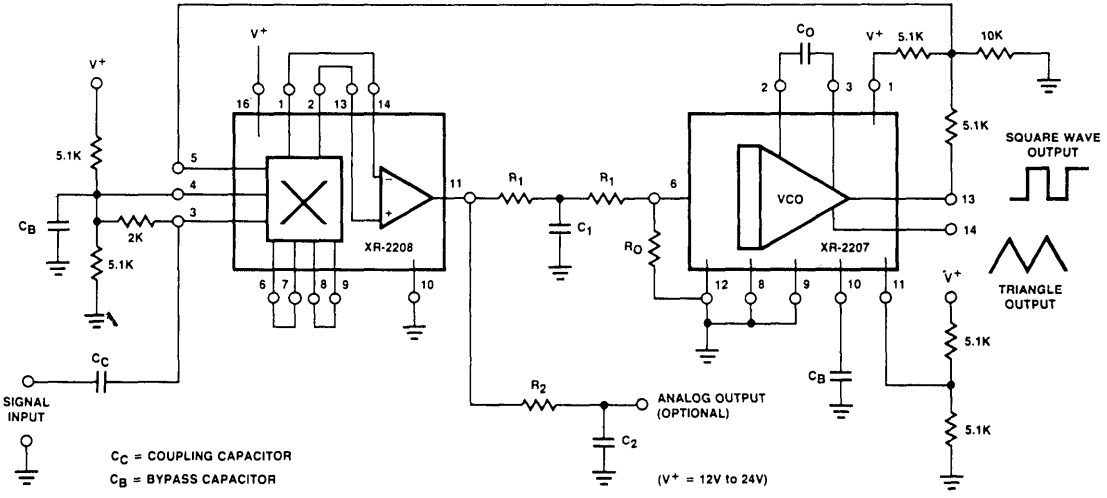


Figure 3. Circuit Interconnections for Single Supply Operation.

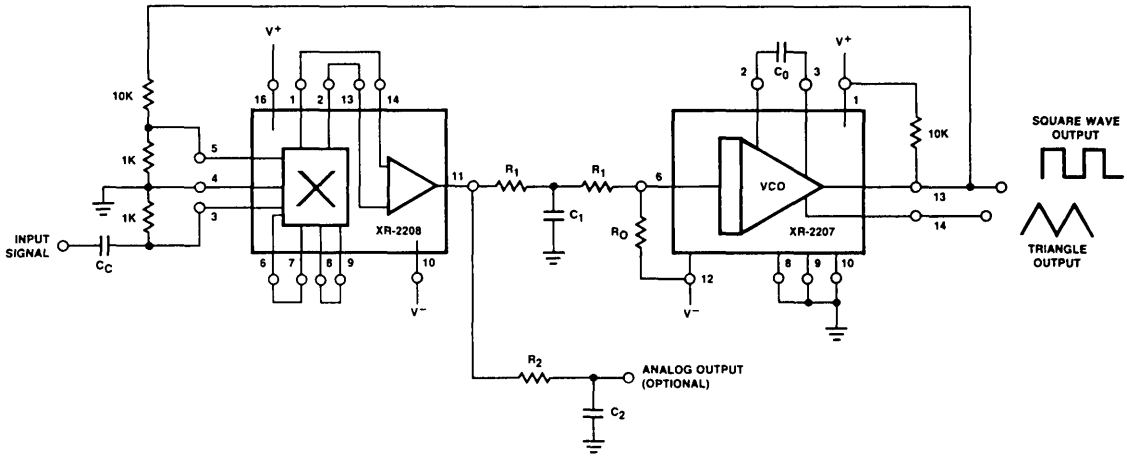


Figure 4. Circuit Interconnections for the Precision PLL System using the XR-2207 and the XR-2208 Monolithic Circuits. (Split-Supply operation, ±6V to ±13V.

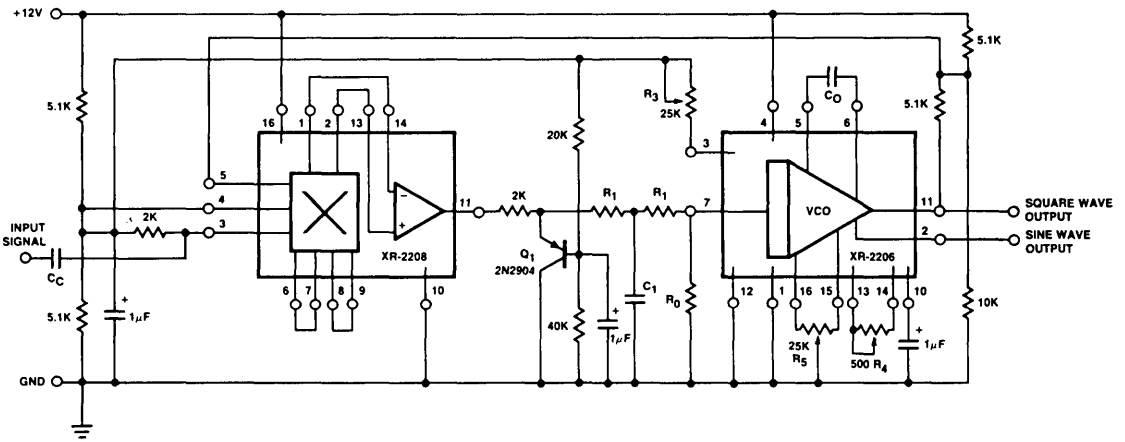


Figure 5.

Single-Chip Frequency Synthesizer Employing the XR-2240

INTRODUCTION

The XR-2240 monolithic timer/counter contains an 8-bit programmable binary counter and a stable time-base oscillator in a single 16-pin IC package. Although the circuit was originally designed as a long-delay timer capable of generating time delays from microseconds to weeks, it also offers a wide range of other applications beyond simple time-delay generation. One such unique application is its use as a single-chip, frequency synthesizer, where it can generate over 2,500 discrete frequencies from a single reference frequency input.

The operation of the XR-2240 as a frequency synthesizer is possible because of the ability of the circuit to both *multiply* and *divide* the input frequency reference. It can, simultaneously, multiply the input frequency by a factor, "M," and divide it by a factor "N + 1," where both M and N are adjustable integer values. Therefore, the circuit can produce an output frequency, f_O, related to the input reference frequency f_R as:

$$f_O = f_R \frac{M}{1 + N}$$

Figure 1 shows the circuit connection for operating the XR-2240 timer/counter as a self-contained frequency synthesizer. The integer values M and N can be externally adjusted over a broad range:

$$1 \leq M \leq 10 \quad 1 \leq N \leq 225$$

The multiplication factor M is obtained by locking on the harmonics of the input frequency. The division factor N is determined by the pre-programmed count in the binary counter section. The principle of operation of the circuit can be best understood by briefly examining its capabilities for frequency division and multiplication separately.

Frequency Division by (1 + N):

When there is no external reference input, f_R, the time-base oscillator section of the XR-2240 free-runs at its set frquency, f_S (f_S = 1/RC), where R and C are the external components at pin 13. The 8-bit binary counter can be programmed to divide the time-base frequency by an integer count, N, and generate an output pulse train whose frequency is:

$$f_O = f_S \frac{1}{1 + N}$$

Frequency Multiplication by "M":

Frequency multiplication is achieved by synchronizing the time-base oscillator with the *harmonics* of the input sync or reference signal. Thus, if the time-base oscillator is made to free-run at "M" times the input frequency, it can be made to synchronize the "M"th harmonic of the input reference signal. Typical capital range of the circuit is better than ±3%, for values of $1 \leq M \leq 10$; and since the time-base is accurate to within ±0.5% of the external R-C setting, lock-up does not present a problem for a given harmonic lock setting.

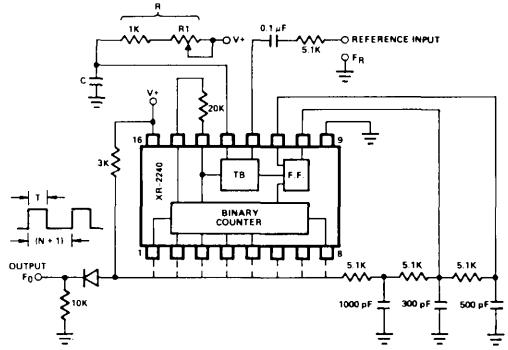


Figure 1

Circuit Operation:

With reference to Figure 1, the operation of the synthesizer circuit can be briefly explained as follows: The reference input frequency, f_R, is applied to the time-base sync terminal (pin 12) through a 5.1 KΩ series resistance and a coupling capacitor. The recommended waveform for the input frequency, f_R, is a 3 Vpp pulse train with a pulse width in the range of 30% to 80% of the time-base period, T. The multiplication factor M is chosen by the potentiometer R_1 which sets the time-base period T (T = RC). If no external reference is used, then M is automatically equal to 1.

The divider modulus, N, is chosen by shorting various counter outputs to a 3K common pull-up resistor. The output waveform is a pulse train with a fixed pulse width, T = RC, and a period T_O = (N + 1)RC.

The external R-C network between the output and the trigger and reset terminals of the XR-2240 is a non-critical delay network which resets and re-triggers the circuit to maintain a periodic output waveform. For the component values shown in Figure 1, the circuit can operate with the timing components R and C in the range of:

$$0.005\ \mu F \leq C \leq .1\ \mu F;\ 1\ K\Omega \leq R \leq 1\ M\Omega$$

The XR-2240 is a low-frequency circuit. Therefore, the maximum output frequency is limited to ≈200 kHz, by the frequency capability of the internal time base oscillator.

A particularly useful application of the simple synthesizer circuit of Figure 1 is to generate stable clock frequencies which are synchronized to an external reference, such as the 60 Hz line frequency. For example, one can generate a 100 Hz reference synchronized to 60 Hz line frequency simply by setting M = 5 and N = 2 such that:

$$f_O = f_R \frac{M}{1 + N} = (60)\frac{5}{1 + 2} = 100\ Hz$$

Dual Tone Decoding with XR-567 and XR-2567

INTRODUCTION

Two integrated tone decoders, XR-567 units, can be connected (as shown in Figure 1A) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R'_1C'_1$ are chosen, respectively, for Tones 1 and 2. If sequential tones (1 followed by 2) are to be decoded, then C_3 is made very large to delay turn-off of Unit 1 until Unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since Unit 2 will turn off before Unit 1 comes on. Figure 1B shows a circuit variation which eliminates the NOR gate. The output is taken from Unit 2, but the Unit 2 output stage is biased off by R_2 and CR_1 until activated by Tone 1. A further variation is given in Figure 1C. Here, Unit 2 is turned on by the Unit 1 output when Tone 1 appears, reducing the standby power to half. Thus, when Unit 2 is on, Tone 1 is or was present. If Tone 2 is now present, Unit 2 comes on also and an output is given. Since a transient output pulse may appear

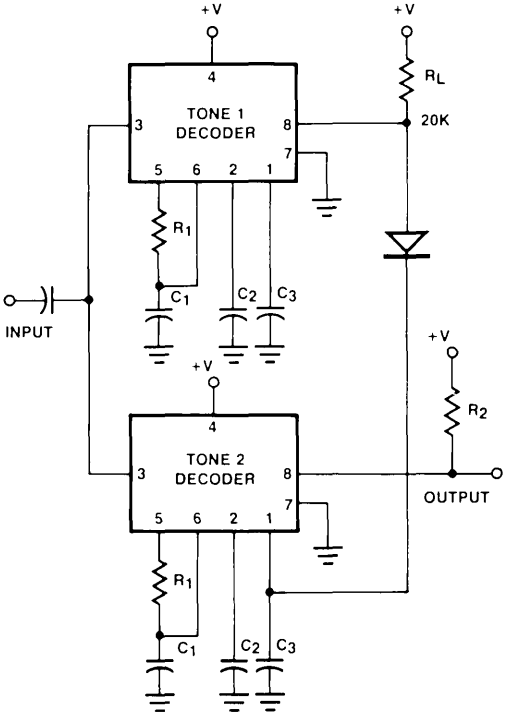


Figure 1B

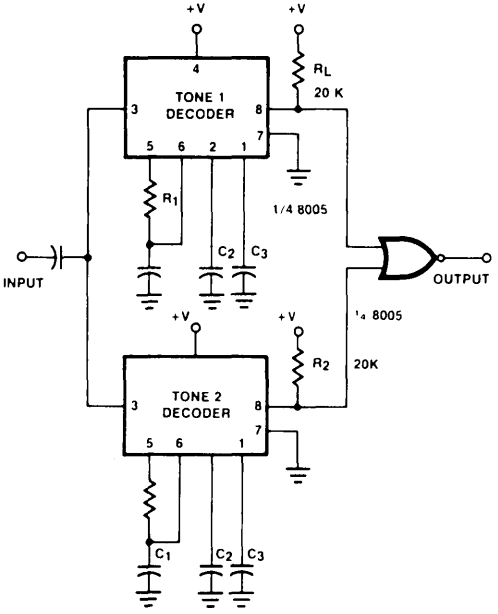


Figure 1A. Detection of Two Simultaneous or Sequential Tones

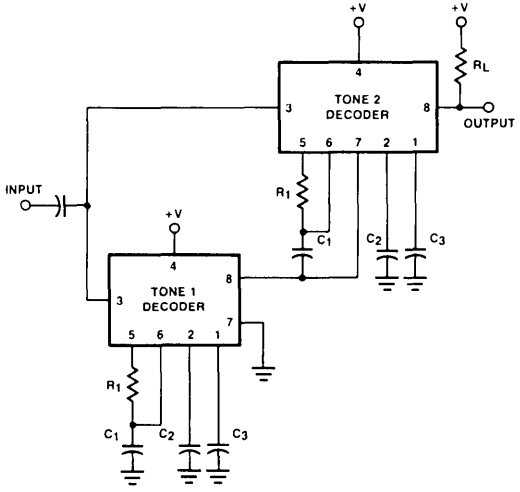


Figure 1C

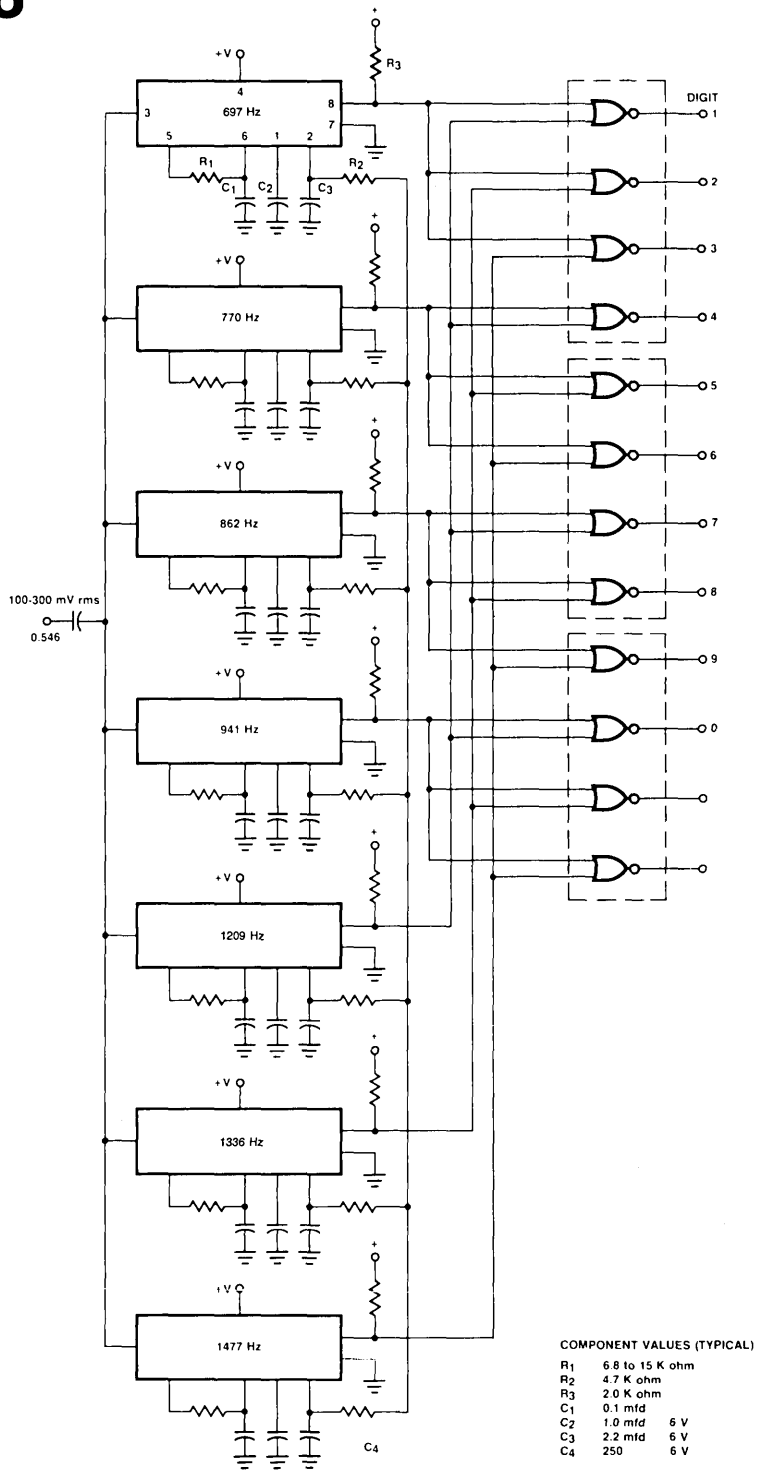


Figure 2. Low-Cost Touch Tone® Decoder

during Unit 1 turn-on, even if Tone 2 is not present, the load must be slow in response to avoid a false output due to Tone 1 alone.

The XR-2567 Dual Tone Decoder can replace two integrated tone decoders in this application.

HIGH SPEED, NARROW BAND TONE DECODER

The circuit of Figure 1 may be used to obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70 mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_o$ and $1300/f_o$ mfd where f_o is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

TOUCH-TONE DECODER

Touch-Tone decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every tone. A low-cost decoder can be made as shown in Figure 2. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% of 100 mV and 5% at 50 mV rms. Capacitor C_4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltages (50 to 10 mV rms), the bandwidth can be controlled in the normal manner by selecting C_2, thereby eliminating the seven R_2 resistors and C_4. In this case, C_2 would be 4.7 mfd for the three lower frequencies or 2.2 mfd for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. As shown in the 567 data sheet under Alternate Method of Bandwidth Reduction, the external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R_2 resistors. In effect, the five 567's which are not being activated during the decoding process serve bias voltage sources for the R_2 resistors of the two 567's which are being activated. Capacitor C_4 (optional) decouples the ac currents at the common point.

LOW COST FREQUENCY INDICATOR

Figure 3 shows how two tone decoders set up with overlapping detection bands can be used for a go/no/go frequency meter. Unit 1 is set 6% above the desired sensing frequency and Unit 2 is set 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either Unit 1 or Unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

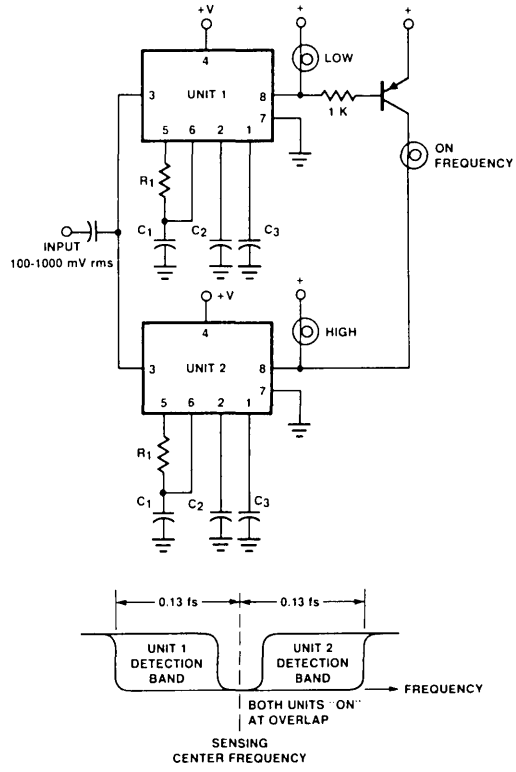


Figure 3. Frequency Meter with Low-Cost Lamp Readout

Sinusoidal Output from XR-215 Monolithic PLL Circuit

INTRODUCTION

In a wide range of communication or signal conditioning applications, it is necessary to obtain a sinusoidal output signal which is synchronized to a desired reference or clock input. This can be achieved by using the XR-215 type monolithic PLL circuit and an additional sine-shaping network.

When a periodic input signal is present within the capture range of the XR-215 PLL, the system will lock on the input; and the VCO section of the PLL will synchronize with the input frequency. The output of the oscillator section of the PLL can then be converted to a low distortion sine wave by a relatively simple sine-shaping circuit.

GENERAL DESCRIPTION

Figure 1 contains a functional block diagram of the XR-215 monolithic PLL system. The circuit consists of a balanced phase comparator, a highly stable voltage-controlled oscillator (VCO) and high speed operational amplifier. The phase comparator outputs are internally connected to the VCO inputs and to the non-inverting input of the operational amplifier. A self-contained PLL system is formed by simply ac coupling the VCO output to either of the phase comparator inputs and adding a low-pass filter to the phase comparator output terminals. The XR-215 can operate over a large choice of power supply voltages ranging from 5 volts to 26 volts and a wide frequency band of 0.5 Hz to 35 MHz. It can accommodate analog signals between 300 microvolts and 3 volts and can interface with conventional DTL, TTL and ECL logic families.

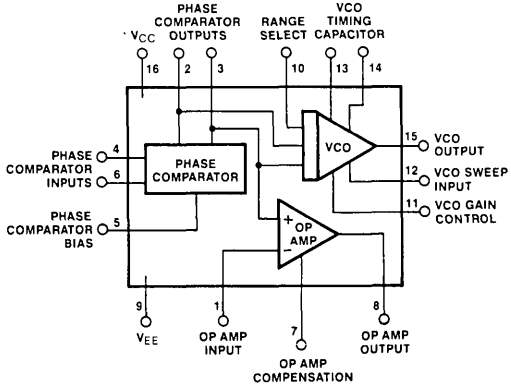


Figure 1. Functional Block Diagram of XR-215 Monolithic PLL Circuit

Figure 2 shows the simplified circuit schematic of the XR-215 phase-locked loop IC. The VCO part of XR-215, shown in the center section of Figure 2, is an emitter-coupled multivibrator circuit, whose frequency is set by an external capacitor, C_0, connected across the timing terminals (Pins 13 and 14). In this type of an oscillator, the differential voltage waveform across the timing capacitor, C_0, is a linear triangle, with a peak-to-peak amplitude of 1.4 volts. This output amplitude across the timing capacitor is independent of supply voltage.

This triangular waveform can be shaped into a low distortion sine wave by passing it through a simple differential gain stage, as shown in Figure 3. By adjusting the potentiometer R_g of Figure 3, the input transistors T_1 and T_2 of the differential stage can be brought to the verge of cutoff at the positive and the negative extremities of the input triangle wave. This causes the peaks of the triangle waveform to be rounded, resulting in a nearly sinusoidal output waveform from the differential stage. If the transistor characteristics and the current levels in the differential gain stage are well matched, one can reduce the total harmonic distortion (THD) of the sinusoidal output waveform to less than 3%.

The sine-shaper circuit of Figure 3 can be designed by using the XR-D101 NPN transistor array, which provides five identical NPN transistors in a single IC package. Figure 4 shows the package diagram of XR-D101 chip, in terms of its 16-pin DIP package.

The five independent transistors contained in the XR-D101 transistor array can be interconnected, as shown in Figure 5, to form the differential sine wave-shaping circuit of Figure 3. The inputs of the sine-shaper can be directly connected to the timing capacitor terminals (Pins 13 and 14) of the XR-215 PLL.

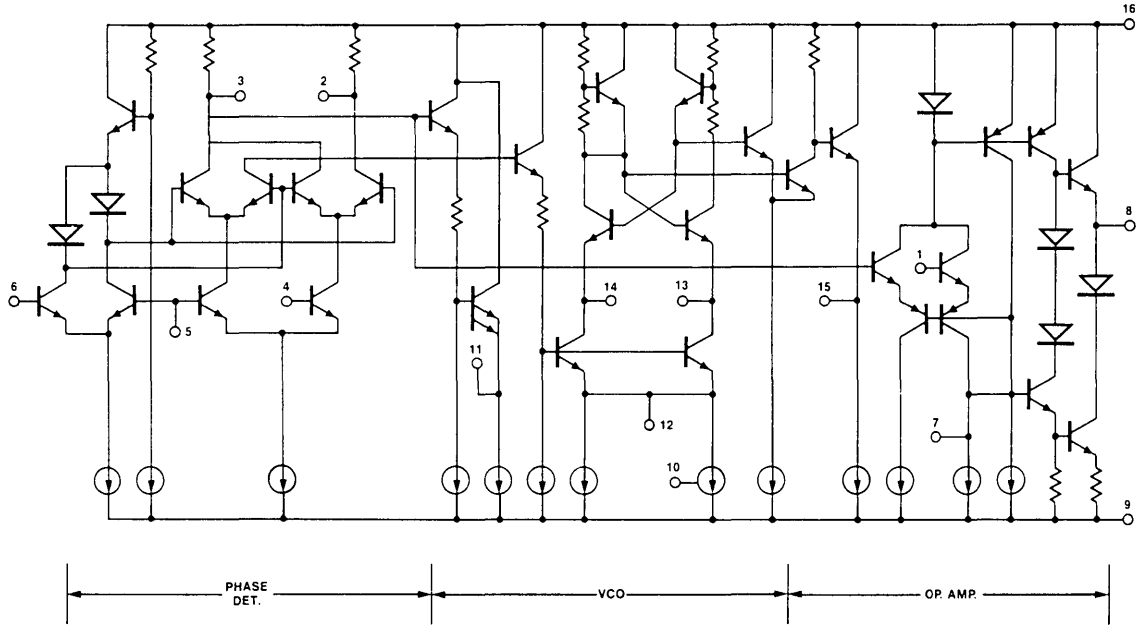


Figure 2. Simplified Schematic of XR-215

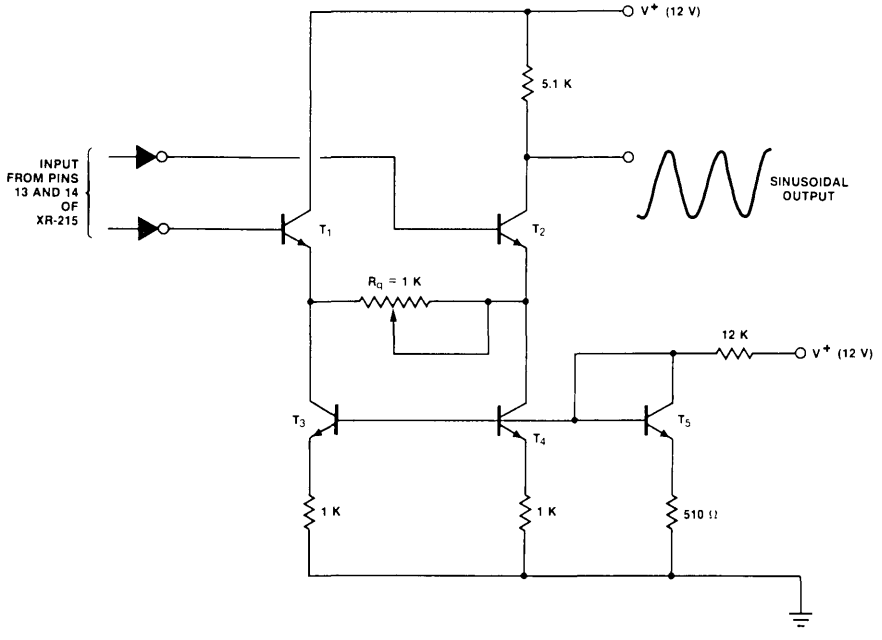


Figure 3. A Simple Triangle-to-Sine Wave Converter Using a Differential Gain Stage

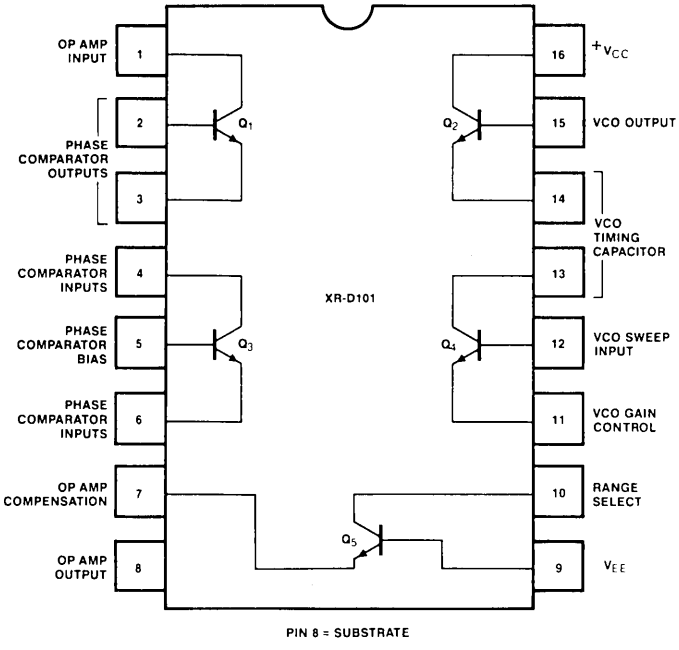
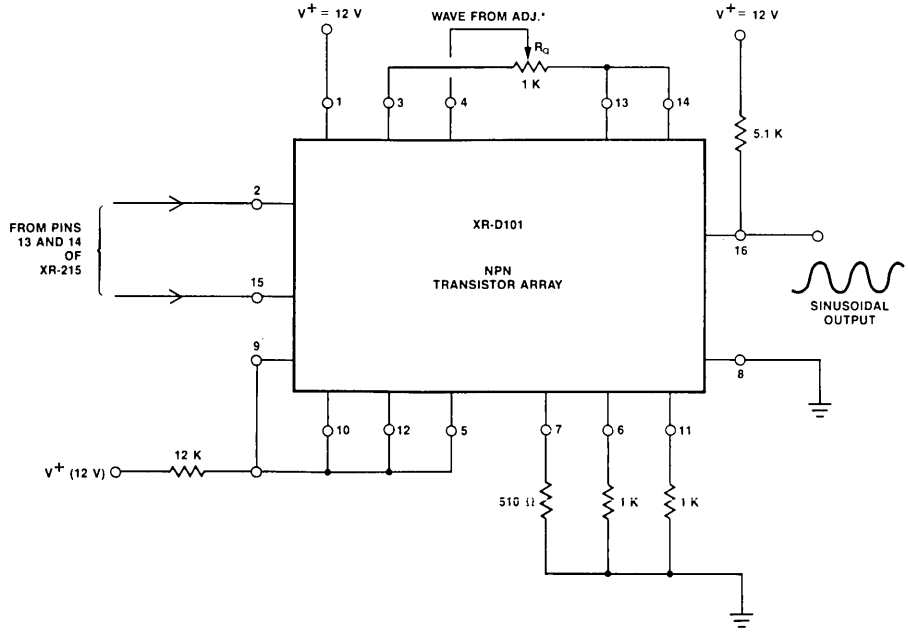


Figure 4. Package Diagram for XR-D101 Matched NPN Transistor Array



*ADJUST R_G FOR MINIMUM HARMONIC DISTORTION.

Figure 5. Use of XR-D101 Transistor Array to Obtain Sinusoidal Output from XR-215 PLL

XR-C262 High-Performance PCM Repeater IC

INTRODUCTION

The XR-C262 is a monolithic repeater circuit for Pulse-Code Modulated (PCM) telephone systems. It is designed to operate as a regenerative repeater at 1.544 Megabits per second (Mbps) data rates on T-1 type PCM lines. It is packaged in a hermetic 16-pin CERDIP package and is designed to operate over a temperature range of -40°C to +85°C. It contains all the basic functional blocks of a regenerative repeater system including Automatic Line Built-Out (ALBO) and equalization, and is insensitive to reflections caused by cable discontinuities.

The XR-C262 operates with a single 6.8-volt power supply, and with a typical supply current of 13 mA. It provides bipolar output drive with high-current handling capability. The clock extractor section of XR-C262 uses the resonant-tank circuit principle, rather than the injection-locked oscillator technique used in earlier monolithic repeater designs. The bipolar output drivers are designed to go to "off" state automatically when there is no input signal present. Compared to conventional repeater designs using discrete components, the XR-C262 monolithic repeater IC offers greatly improved reliability and performance and provides significant savings in power consumption and system cost.

This application note outlines the basic design principles and the electrical characteristics of the XR-C262 monolithic repeater IC. In addition, circuit connections and applications information are provided for its utilization in T-1 type 1.544 Megabit PCM repeater systems.

FUNDAMENTALS OF PCM REPEATERS

The Pulse-Code Modulation (PCM) telephone systems are designed to provide a transmission capability for multiple-channel two-way voice frequency signals which are transmitted in a digital PCM format. In order to minimize error rates, and provide transmission over long distances, this digital signal must be regenerated at periodic intervals, using a regenerative repeater system. Figure 1 shows the block diagram of a bi-directional PCM repeater system consisting of two identical digital regenerator or repeater sections, one for each direction of transmission. These repeaters share a common power supply. The DC power is simplexed over the paired cable and is extracted at each repeater by means of a series zener diode regulator.

In the United States, the most widely used PCM telephone system is the T-1 type system which operates at a data rate of 1.544 Mbps, with bipolar data pulses. It

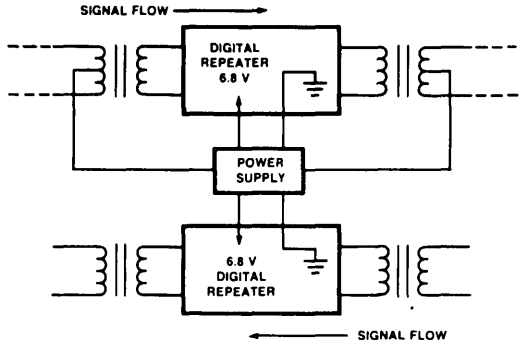


Figure 1. Block Diagram of a Bi-Directional Digital Repeater System.

can operate on either pulp- or polyethylene-insulated paired cable that is either pole-mounted or buried. Operation is possible with a variety of wire gauges, provided that the total cable loss at 772 kHz is less than 36 dB. Thus, the system can operate satisfactorily on nearly all paired cables which are used for voice frequency trunk circuits.

The T-1 type transmission system is designed to operate with both directions of transmission within the same cable sheath. The system performance is limited primarily by near-end cross-talk produced by other systems operating within the same cable sheath. In order to insure that the probability of a bit error is less than 10^{-6}, the maximum allowable repeater spacing, when used with 22-gauge pulp cable, is approximately 6000 feet.

The XR-C262 monolithic IC replaces about 90% of the electronic components and circuitry within the digital repeater sections of Figure 1. Thus, a bi-directional repeater system should require two XR-C262 ICs, one for each direction of information flow.

OPERATION OF THE XR-C262

The XR-C262 monolithic repeater is packaged in a 16-pin dual-in-line hermetic package, and is fabricated using bipolar process technology. The functions of the circuit terminals are defined in Figure 2, in terms of the monolithic IC package.

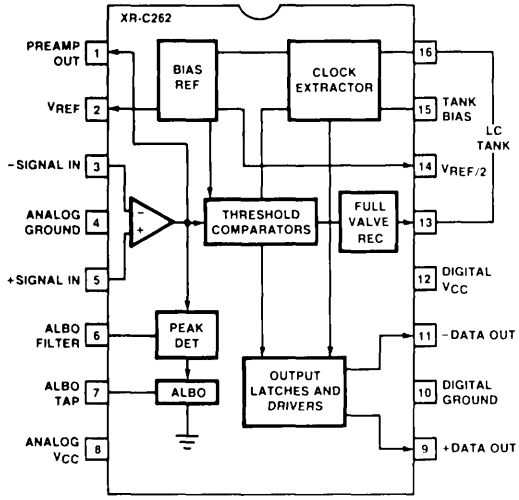


Figure 2. Package Diagram of XR-C262 Monolithic PCM Repeater.

A more detailed system block diagram for the monolithic repeater system is given in Figure 3. The system blocks shown within the dotted area are included on the monolithic chip. The numbers on the circuit terminals correspond to the pin numbers of the 16-pin IC package containing the repeater chip. In terms of the system block diagram of Figure 3, the overall repeater operation can be briefly explained as follows.

The bipolar PCM signals which are attenuated and distorted due to the preceding transmission medium are applied to the input of a preamplifier (Block 1) through an Automatic Line Build-Out (ALBO) circuit. The impedance, Z_1, corresponds to the passive section of the ALBO network. The preamplifier section, along with the passive equalizer networks Z_2 and Z_3 connected in feedback around it, provides gain to compensate for line losses and band-limiting to reject unwanted noise as well as gain and phase equalization to shape received pulses.

The ALBO circuitry provides attenuation and shaping to automatically adjust for varying cable characteristics. The output of the preamplifier is controlled to swing between two established peak levels. This is accomplished by feedback circuitry, and is similar in concept to automatic gain control. When the preamplifier output passes through the peak thresholds it is detected by the peak detector (Block 2) and produces a signal which is used to control a feedback loop establishing

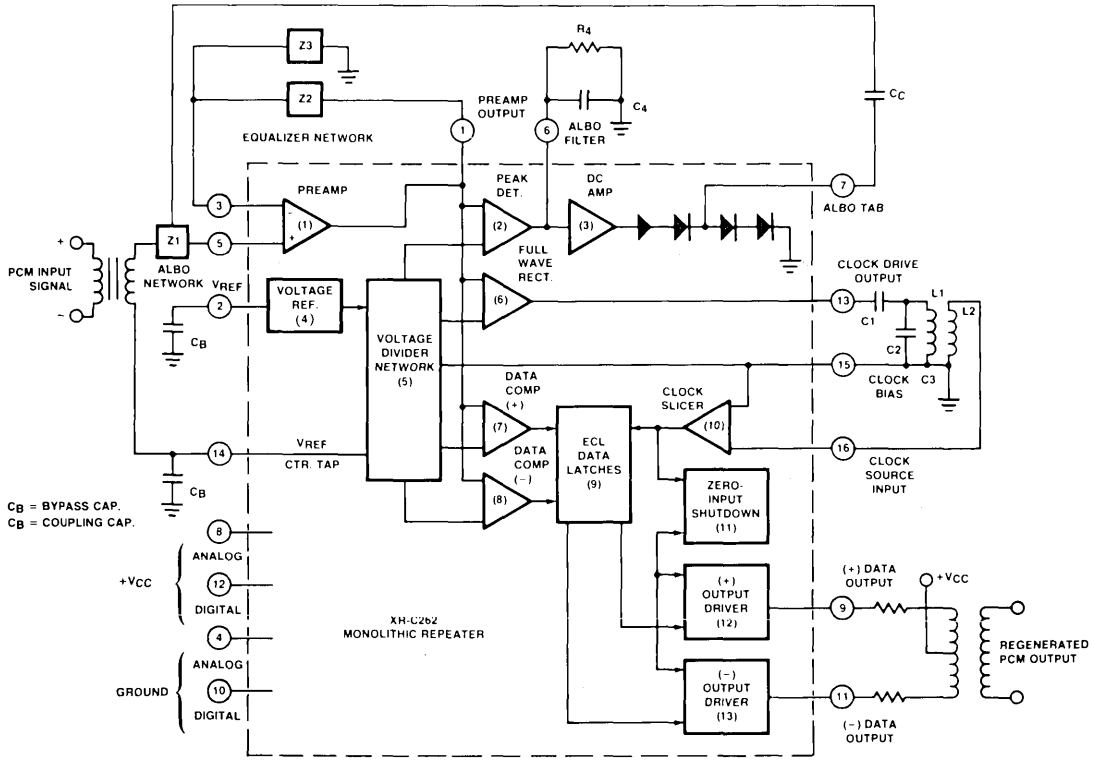


Figure 3. Detailed Block Diagram of the XR-C262 Monolithic Repeater System.

the attenuation and shaping of the ALBO network. The actual circuit design associated with this function is described in more detail in the discussion of peak detection and ALBO circuitry.

The output of the preamplifier drives a set of data comparators which are internally biased from a voltage reference (Block 4) and the precision voltage divider network (Block 5). Thus, the preamplifier output is "sliced" at various voltage levels to eliminate the effects of the baseline noise. This output is full-wave rectified and amplified through Block 6 of Figure 3. The resulting signal has a strong Fourier component at the clock frequency and is used to drive a high Q (≈ 100) resonant circuit tuned to that frequency. The output of the resonant circuit is transformer-coupled to a zero-crossing detector and clock limiter (Block 10). The resultant output is the desired recovered timing. This resonant circuit is driven by a low impedance amplifier, and the resulting clock edges are in phase with the peak of the received pulses.

The regeneration of the data is achieved through the two data comparators (Blocks 7 and 8) and the ECL latches (BLock 9) which function as tracking flip-flops. The positive and negative data paths are separate; and, with the exception of the data limiter and slicer levels, identical in design. The preamplifier output is sliced at about 45 percent of the peak voltage and its amplitude is limited to provide digital data pulses. The data is applied to one of the inputs to the tracking flip-flop, whose state is latched and unlatched by the clock. During acquisition, the flip-flop acquires data; during hold, further data transitions are ignored and the state of the flip-flop output determines whether an output pulse is transmitted. The implication of using the clock to perform data sampling is that path delays of the data and clock must be controlled to be equal. The monolithic integrated circuit technology affords this control. The advantage of this technique is that the need for clock shifting or strobe pulse generating circuitry for accurate sampling alignment is eliminated. Actual circuit implementation resulted in a 40-nsec misalignment of clock and data. This 40-nsec error in sampling time amounts to less than 0.4 dB degradation in SNR performance. Figure 4 shows the idealized timing and signal waveforms within the circuit.

The output drivers use latched data and clock to produce an output pulse-width which is accurately controlled by the duration of the clock. Non-saturating output drivers (Blocks 12 and 13) insure that output pulse rise and fall times are less than 100 nsec. The zero input shut-down circuitry (Block 11) guarantees that in the event incoming data disappears, the output switches will not latch in the "on" state. When no input signal is present, the absence of clock is sensed and the output drivers are held in the "off" state.

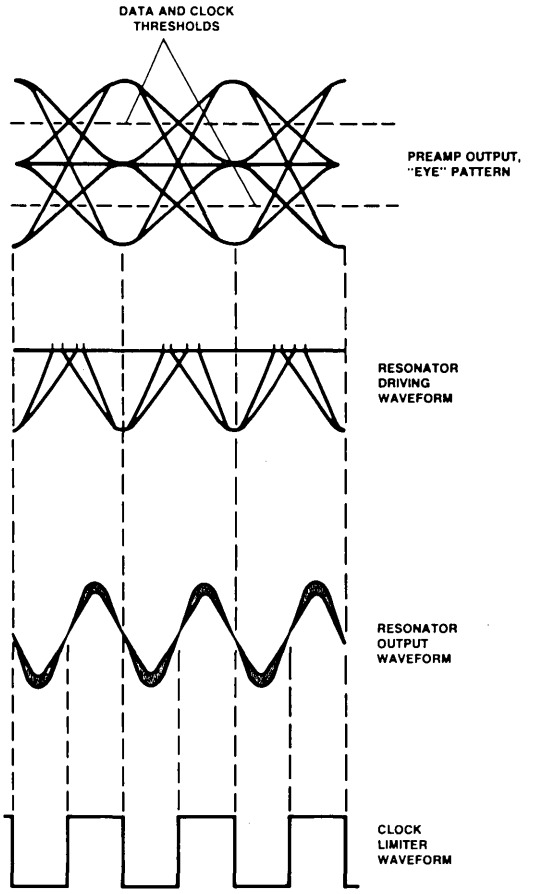


Figure 4. Timing Diagrams of Voltage Waveforms within the Clock Regeneration Section.

Figure 5 shows a practical circuit connection for the XR-C262 in an actual PCM repeater application for 1.544 Mbps T-1 repeater system. For simplification purposes, the lightening protection circuitry and the second repeater section for the reverse channel are not shown in the figure.

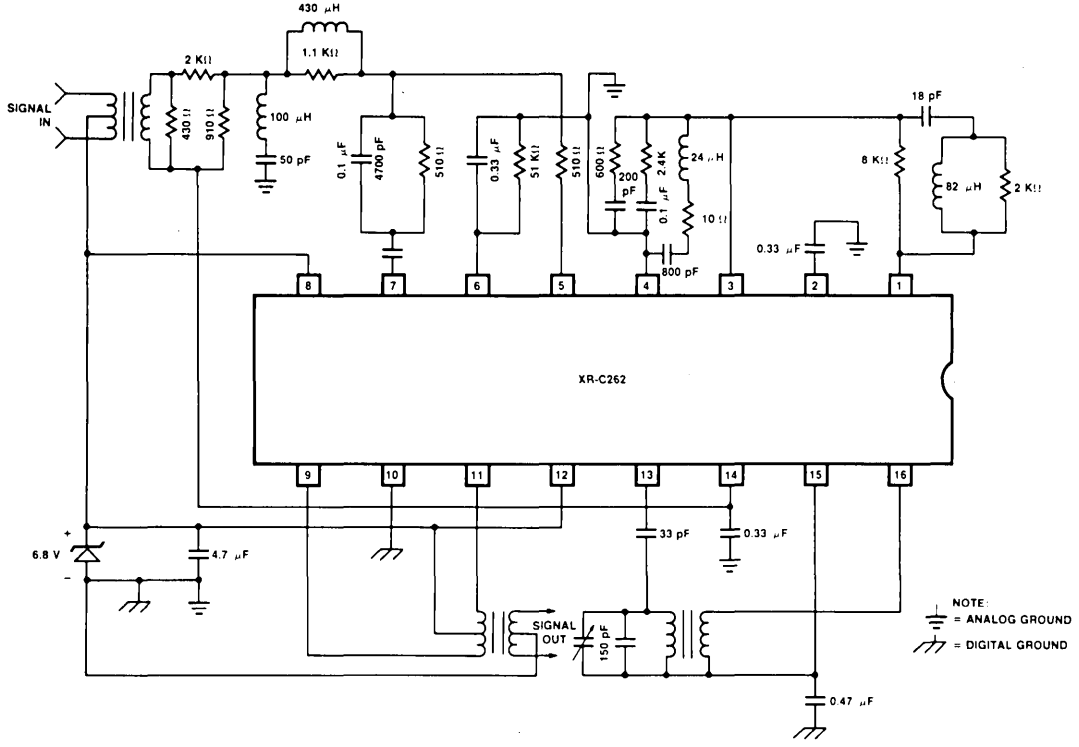


Figure 5. A Recommended Circuit Connection Diagram for T-1 Type Repeater Application.

DESCRIPTION OF CIRCUIT OPERATION

Preamplifier Section (Figure 6):

The circuit diagram of the preamplifier section is shown in Figure 6. This section is designed as a single-stage high-gain amplifier with differential inputs and a single-ended output. The amplifuer output is internally connected to the peak-detector, full-wave rectifier and the data-comparator sections. The circuit exhibits a high differential input resistance ($\approx 10^6$ ohms) and a low output impedance (≈ 80 ohms). It has a nominal voltage gain of 69 dB at DC and ≥ 50 dB at 1 MHz. The frequency response of the circuit exhibits a single-pole roll-off characteristic.

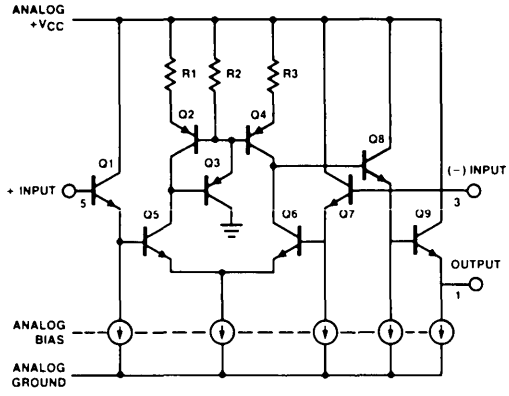


Figure 6. Circuit Diagram of Preamplifier Section.

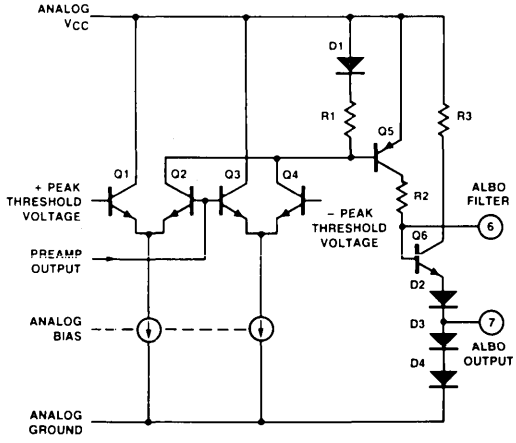


Figure 7. Circuit Diagram of the Peak-Detector and the ALBO Sections.

Peak-Detector and ALBO Section (Figure 7):

The peak-detector circuit is designed to detect the peaks of the preamplifier output, provided that these peaks exceed the internal detection threshold levels. This peak information is then low-pass filtered and is used to control the current in a diode string which acts as a variable-loss or "variolosser' element in a feedback path. In the circuit, the comparators conduct whenever the preamp output exceeds the (+) threshold in a positive direction or the (-) threshold in a negative direction. Transistor Q_5 then injects a pulse of current into the ALBO filter. In the steady state, DC level across the ALBO filter controls the current through the diode string; and the dynamic resistance of the diodes acts as the variolosser element. The usable linear resistance range in this application is almost three orders of magnitude ranging from 11 Ω to ≈ 6 KΩ.

Data Latches (Figure 8):

The data latches are required to be impervious to data transitions in the latch mode, and to be "transparent," (i.e., tracking the input data) during the tracking mode. Figure 8 shows the basic circuit configuration used in the XR-C262, which meets the above-mentioned performance requirements. During the time when the clock pulse is high, the acquisition transistors Q_1 and Q_2 are differentially switched with data transitions, and the data is coupled to the respective bases of Q_3 and Q_4. When the clock pulse goes low at the sample time (see Figure 4), the information is regeneratively latched into Q_3 and Q_4. While the clock is low, further data transitions have no effect upon the state of the flip-flop. A more detailed description of the timing waveforms is given in Figure 13.

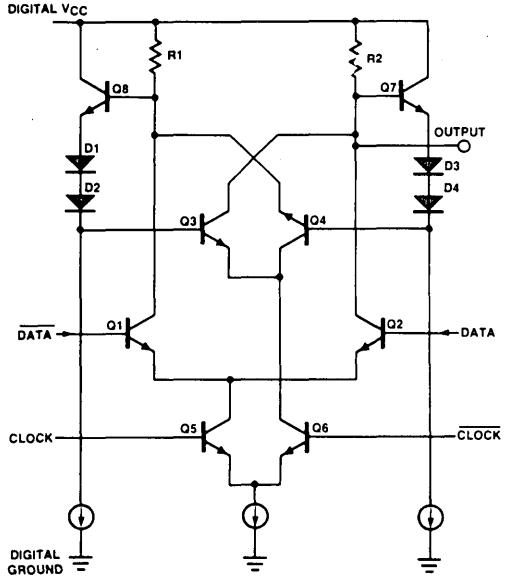


Figure 8. Circuit Configuration for Tracking Data Latches.

Threshold Circuitry (Figure 9):

Threshold circuitry is a low impedance voltage-divider circuit corresponding to Block 5 of Figure 3, and it establishes the fixed levels required for data, clock and peak detection. It is important that the thresholds are insensitive to temperature variations, and that they are of sufficiently low impedance to guarantee that there is no threshold variation due to changing signal conditions. The reference voltages of the peak-detector, data, and clock thresholds are set by a resistor chain which divides down the voltage of the on-chip zener diode. The ratios of data threshold to peak-detector threshold and that of clock threshold to peak-detector threshold are both set at 45 percent. In the actual circuit implementation, as shown in Figure 10, a compound connection of PNP's and NPN's are used to reduce the output impedance of the reference levels. The currents through the NPN and PNP transistor strings are set so as to insure that the base emitter voltage drops of the NPN's and PNP's are nominally the same. The output impedance of the resulting reference voltage taps are about 300 ohms. The center tap of the buffered divider is brought to a separate package terminal (Pin 14 of Figure 3) for biasing the preamplifier input.

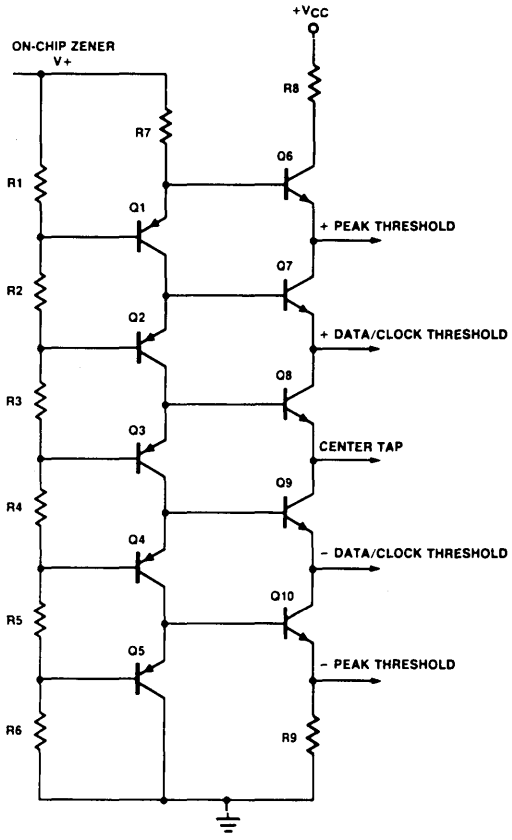


Figure 9. Internal Voltage-Divider Network for Comparator Threshold Setting.

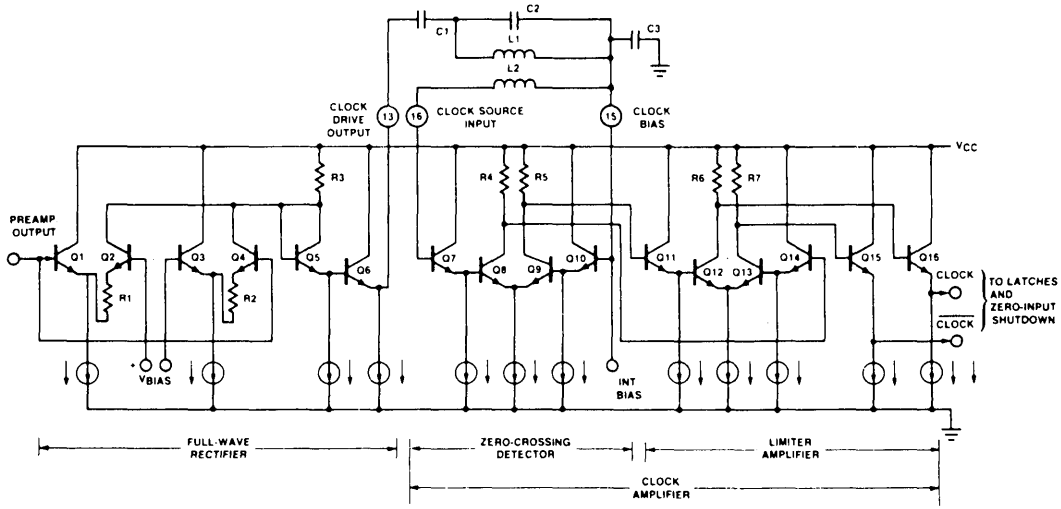


Figure 10. Circuit Diagram of the Clock Recovery Section.

Clock Recovery Section (Figure 10):

Clock recovery circuity consists of a full-wave rectifier, an external L-C resonant circuit, a zero crossing detector, and limiting amplifier, as shown in Figure 10. The full-wave rectifier circuit, comprising of cross-coupled transistor pairs Q_1 through Q_4 has a net voltage gain of 2, which is obtained by setting $R_1 = R_2 = (1/2)R_3$. The rectified output is then buffered by the Darlington emitter-follower stage made up of Q_5 and Q_6, and applied to the external L-C resonant circuit. Q_6 is operated at a high bias current level to provide an output impedance of less than 15Ω. This low impedance is required to insure that the L-C tank-drive circuitry looks like a voltage source.

The inductor of the resonant tank circuit is also a transformer which couples the sine wave signal to the zero crossing detector and limiting amplifier. The zero crossing detector is a differential amplifier with a nominal voltage gain of 20 and input impedance of 4 MΩ. The sine wave from the resonant circuit is sliced to produce a square wave with sharp transitions at the zero crossings. This eliminates timing variations that may be caused by amplitude changes of the sine wave signal. The output of the zero crossing detector is further enhanced by the limiter which is another differential pair with a nominal voltage gain of 30. The output of this amplifier is a 1.5 V peak-to-peak square wave clock which drives the data latches and the output drivers.

Zero-Input Protection Circuit (Figure 11):

The zero input protection circuitry accomplishes the dual task of preventing the output switches from latching in an "on" state, as well as reducing the likelihood of output pulses with no input signal. The data, clock, and regenerator circuitry are all balanced DC coupled circuits. Controlling the steady state, no-signal condition of these circuits without building an unacceptable offset into the path is not practical. Instead, a retrigerable one-shot that uses the saturation characteristics of PNP transistors is used to control the level of the clock into the output switches. This technique uses the bandpass characteristics of the timing recovery resonant circuit to reject out of band signals, thus minimizing the chance of producing output pulses with no input signal and the presence of noise. Figure 11 shows the basic implementation of the zero-input protection circuit. $Q_1$and Q_2 function as a simple retriggerable one-shot. The transistor Q_2 is a lateral PNP device with a limited frequency capability and long storage-time delay. The existence of the 1.544 MHz clock causes Q_2 to saturate and remain in saturation while clock pulses are present. The comparatively long time constant associated with Q_2 coming out of saturation (≈ 5 μsec) insures that, when data is present, the zero input protection has no effect upon operation. When data disappears there is no clock to retrigger the one-shot, thus Q_2 comes out of saturation, causing Q_3 to saturate which pulls the respective clock lines high, and disables both output drivers in their "off" state.

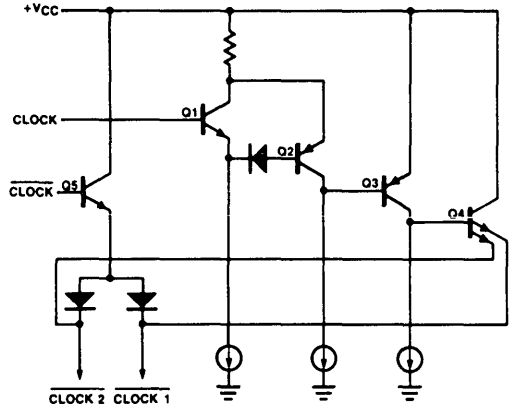


Figure 11. Zero-Input Shutdown Circuit for Output Protection.

Output Drive Circuitry (Figure 12):

The output drive circuitry is made up of two identical channels as indicated in the block diagram of Figure 2. The circuit configuration for each of these driver sections is shown in Figure 12. The output would follow the data input from the latches only when the clock input is at a "high" state, i.e., with Q_2 off and Q_3 on. In this manner, the output pulse-width is controlled by the clock. To provide the fast turn-on and turn-off of the output drivers, all the transistors operate in a nonsaturating state. Q_4 forms an active clamp to reduce voltage swing at the base of Q_6, and the clamp diode D_5 prevents the saturation of the output driver Q_7. Because of the biasing scheme mentioned above, the amplitude of the clock and the latched data are insensitive to supply voltage and temperature changes. Thus, the variations of the regenerated pulse-width over temperature and supply are minimized.

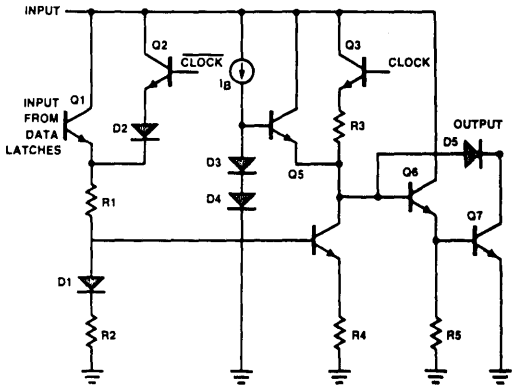


Figure 12. Circuit Configuration for the Output Drivers.

Timing Waveforms (Figure 13):

Figure 13 illustrates the relative time and phase relationships between the signal levels at various points within the circuit. For the purpose of illustration an input data pattern comprised of a string of "ONE"s is assumed, which looks like a nearly sinusoidal input after having traveled through a dispersive transmission medium such as a long cable. Waveform (1) is the output of the preamplifier; Waveforms (2) through (5) are the outputs of the two data comparators driven by the preamplifier output (see Figure 3). Waveform (6) is the low-level clock signal obtained from the resonant tank circuit, at Pin 16 which is then amplified and sliced by the clock-recovery circuit (see Figure 11) and appears as the internal clock signals shown as Waveforms (7) and (8). Waveform (9) shows the output of one of the data latches (Figure 8) as a function of the clock and data inputs. The output of the latch tracks +DATA when the clock is low, and stays latched in that condition when the block goes high. The output drive at Pin 9, which is shown as Waveform (10) will then go low only when the Waveforms (8) and (9) are low. Waveform (11) shows the second output available at Pin 11. These two outputs are then differentially combined by the output transformer (see Figure 3) to provide the regenerated bipolar output pulses shown in Waveform (12) of Figure 13.

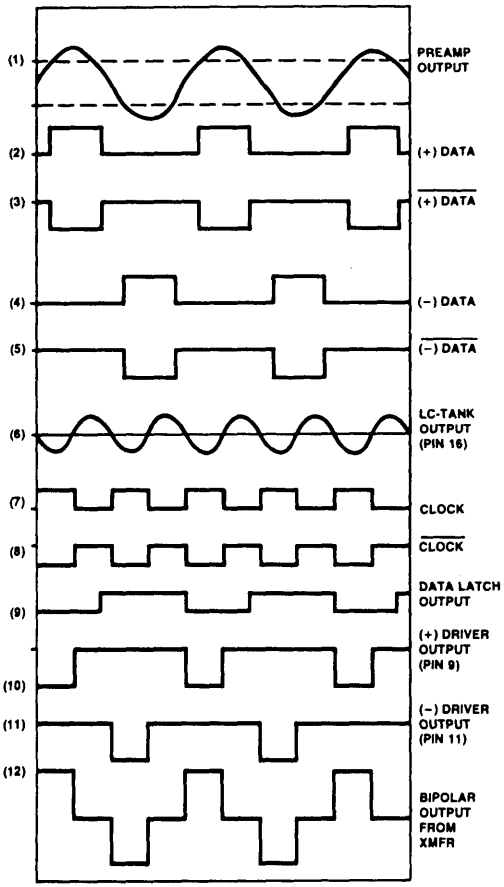


Figure 13. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern.

AN-10

ELECTRICAL CHARACTERISTICS $+V_{CC}$ = 6.8 Volts, T_A = −40°C to +85°C.

CHARACTERISTICS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
Supply Current					
Digital Current	7	10	13	mA	Measured at Pin 12
Analog Current	2	3.5	5	mA	Measured at Pin 8
Total Current		13	17	mA	
Preamplifier					
Input Offset Voltage	−15		+15	mV	Measured between Pins 3 and 5
DC Gain	60	69	74	dB	
Output High Level	4.3			V	Measured at Pin 1
Output Low Level			0.5	V	Measured at Pin 1
Clock Recovery Section					
Clock Drive Swing (High)	5.1			V	Measured at Pin 13
Clock Drive Swing (Low)			3.8	V	Measured at Pin 13
Clock Bias	3.8	4	4.2	V	Measured at Pin 15
Clock Source Input Current		0.5	4	μA	Measured at Pin 16
Comparator Thresholds					Measured at Pin 1 relative to Pin 14
ALBO Threshold	0.75	0.9	1.1	V	
Clock Threshold	0.323	0.4	0.517	V	
Internal Reference Voltages					
Reference Voltage	5.2	5.45	5.55	V	Measured at Pin 2
Divider Center Tap	2.6	2.78	2.85	V	Measured at Pin 14
ALBO Section					
Off Voltage		10	75	mV	Measured at Pin 7
On Voltage	1.2		1.7	V	Measured at Pin 7
On Impedance			15	Ω	Measured at Pin 7
Filter Drive Current	0.7	1	1.5	mA	Drive current available at Pin 6
Output Driver Section					Measured at Pins 9 and 11
Output High Swing	5.9	6.8		V	R_L = 400 Ω
Output Low Swing	0.6	0.7	0.9	V	I_L = 15 mA
Leakage Current			100	μA	Measured with output in off state
Output Pulse Width	294	324	354	nsec	
Output Rise Time			100	nsec	
Output Fall Time			100	nsec	
Pulse Width Unbalance			15	nsec	

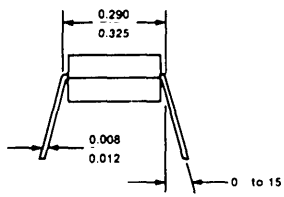
ABSOLUTE MAXIMUM RATINGS

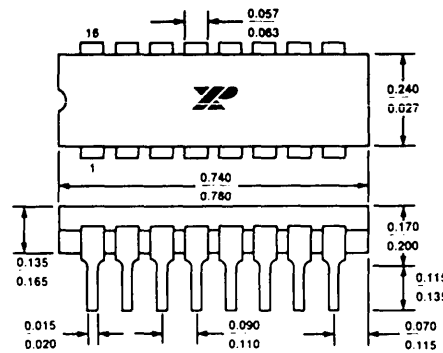
Supply Voltage	+10 V
Power Dissipation	750 mW
Derate above +25°C	6 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-C262	CERDIP	−40°C to +85°C

PACKAGE INFORMATION





A Universal Sine Wave Converter using the XR-2208 and the XR-2211

INTRODUCTION

A universal sine wave converter is a system block which can convert *any* periodic input signal waveform to a low-distortion sine wave, whose frequency is identical to the repetition rate of the periodic input signal. Such universal sine wave converters find applications in communications and telemetry systems. They are particularly useful for converting transducer output waveforms, or pulses, into clean sine wave signals over a band of frequencies. This conversion to sine wave is often necessary to reduce the required system bandwidth for signal transmission by eliminating the harmonic frequencies of the signal.

In the cases where the input frequency is known, and does not change, the universal sine wave converter can be replaced by a simple high-Q filter, tuned to the input frequency. However, in many cases the input frquency, or the repetition rate, is *not* constant, but varies as a function of time or input data. In such cases a fixed-frequency filter is not feasible, and one is forced to use a universal sine wave converter which is essentially a *"tracking regenerative filter"*.

In this application note, the design principle and the performance characteristics of a regenerative sine wave converter circuit is described. The circuit operates on the phase-locked loop (PLL) principle and can be implemented using the XR-2211 monolithic PLL tone decoder and the XR-2208 multiplier IC.

PRINCIPLES OF OPERATION

Figure 1 shows the functional block diagram of a regenerative sine wave converter system, comprised of four functional blocks: (1) a phase-locked loop (PLL), (2) a sine-shaper, (3) a keyed amplifier, and (4) a lock-detect circuit. With reference to the figure, the principle of operation of the entire system can be briefly explained as follows:

When a periodic input signal is present at the input, within the tracking range of the PLL, the circuit would "lock" to the input signal; and the output of the voltage-controlled oscillator (VCO) section of the PLL will duplicate the frequency of the input signal. However, the VCO output waveform will have a fixed wave shape (normally a triangle wave) independent of the input waveform or amplitude. The output of the oscillator section then can be connected to a triangle-to-sine wave converter which converts it to a low-distortion sine wave. The output of the triangle-to-sine converter is then applied to a variable-gain amplifier which sets the desired output amplitude. Since the oscillator section of the PLL is always running, the circuit also contains a "lock-detect" section which *enables* the output amplifier only when there is an input signal. Thus, with no input signal present within the bandwidth of the PLL, the lock-detect section will keep the output amplifier in the "off" state, and the circuit will not produce an output signal.

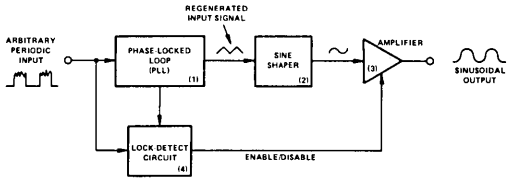


Figure 1. Basic Concept of a Regenerative Sinewave Converter.

CIRCUIT DESIGN

The basic regenerative sine wave converter system of Figure 1 can be easily implemented using the XR-2211 monolithic tone decoder and the XR-2208 monolithic multiplier IC's, with only a minimum number of external components.

The XR-2211 is a monolithic PLL circuit especially designed for FSK and tone detection. Thus, it contains the complete PLL and lock-detect sections (Blocks 1 and 4 of Figure 1) on the same chip. Its overall block diagram is shown in Figure 2. The circuit is packaged in a 14-pin dual-in-line package; and the functions of the circuit terminals are given in Figure 3 in terms of the monolithic IC package. In the sine wave converter application, the FSK detector portion of the circuit is not used; only the basic phase-locked loop and the lock-detector sections are utilized. Figure 4 illustrates the necessary external components for its application in the sine wave converter system. The oscillator section of the XR-2211 is an emitter-coupled multivibrator which oscillates by charging and discharging the external timing capacitor,

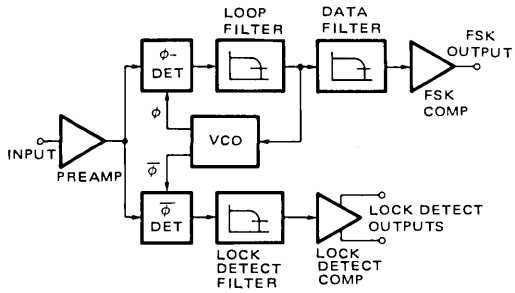


Figure 2. Block Diagram of XR-2211 Phase-Locked Loop FSK and Tone Decoder IC.

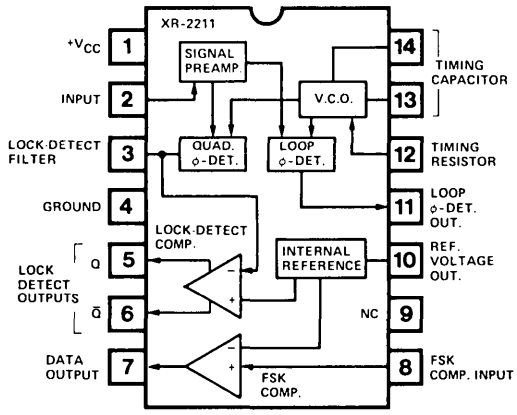


Figure 3. Package Diagram of XR-2211 PLL Circuit.

C_O, (connected across pins 13 and 14) through internal constant-current stages. Thus, the output waveform, taken differentially across the timing capacitor, is a linear triangle wave. This waveform can then be converted to a low-distortion sine wave by the XR-2208 multiplier.

The XR-2208 is a monolithic multiplier circuit which contains a four-quadrant analog multiplier, an op amp, and a unity-gain buffer amplifier in a 16-pin dual-in-line package. Its functional block diagram and equivalent circuit schematic are given in Figures 5 and 6, respectively.

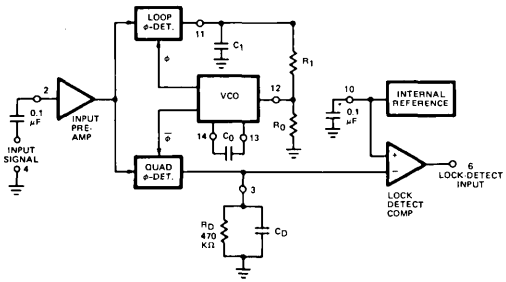


Figure 4. External Circuit Connections for XR-2211 for Sine-wave Converter Application.

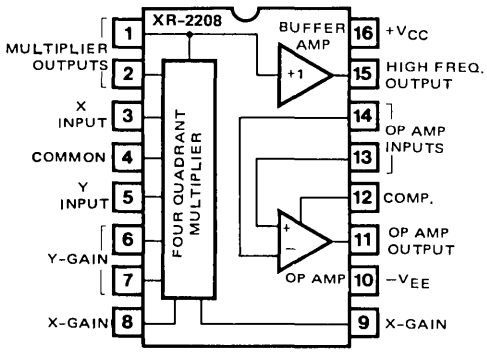


Figure 5. Diagram of XR-2208 Operational Multiplier.

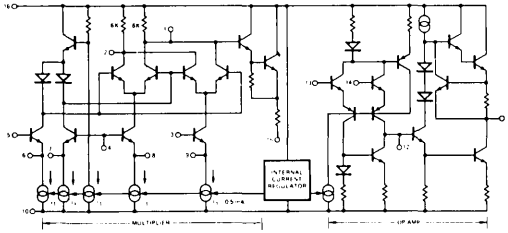


Figure 6. Simplified Circuit Schematic of the XR-2208 Operational Multiplier.

Figure 7 shows the recommended circuit connection of the XR-2211 and the XR-2208 to form a universal sine wave converter circuit. In the figure, a non-crital zener diode ($V_Z \approx$ 6V to 7V) is used to reduce the supply voltage applied to XR-2211, to facilitate DC coupling between the two chips. The frequency of the VCO section of the XR-2211 is set by the timing components R_O and C_O. In this application, a fixed value of R_O = 10KΩ is recommended, giving a center frequency, f_O value of:

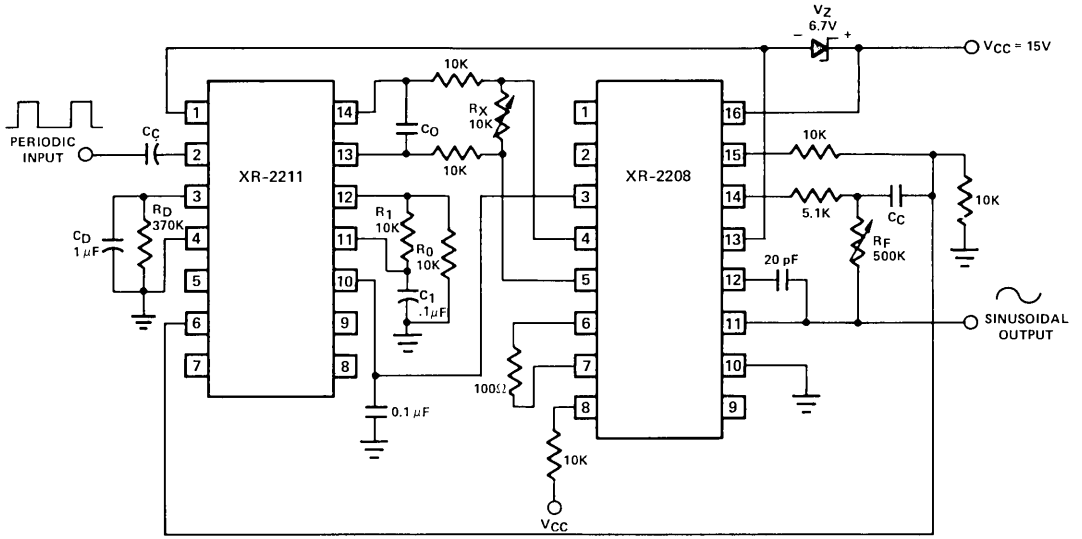
$$f_O = \frac{100}{C_O\ (\mu F)} Hz$$

The triangle wave oscillator output of the XR-2211 PLL is attenuated through a resistive divider made up of two 10KΩ resistors, and a variable 10KΩ potentiometer, R_X. The attenuated triangle wave across R_X is then applied differentially to the X-input (pins 4 and 5) of the XR-2208. The 100Ω external resistor across Y-gain setting terminals (pins 6 and 7) causes the Y-input of the multiplier to be slightly overdriven, and thus causes the peaks of the triangle input rounded into a low-distortion sine wave.

The distortion of the sine wave is minimized by adjusting R_X, which sets the traingle wave amplitude. The output is available at the unity-gain buffer terminal (pin 15) of the XR-2208. This output is then level-shifted toward ground, through two 10KΩ resistors, and is AC coupled to the inverting input of the op amp section of XR-2208. The gain of the op amp is externally adjusted by means of the 500 kΩ potentiometer, R_F. The DC voltage level of the op amp output is set at the reduced supply voltage (i.e., $V_{CC} - V_Z$).

The lock-detect output of the XR-2211 (pin 6) is shorted to the mid-point of the resistive divider at pin 15 of the XR-2208. With no input signal present at the input within the lock range of the XR-2211, pin 6 is at a "low" state. Thus it acts as a shorting switch to ground and disables the op amp section of the XR-2208. When a periodic input signal appears at the circuit input and the XR-2211 establishes lock with the signal; the lock-detect output at pin 6 goes to a "high" or nonconducting state and enables the output op amp of the XR-2208; and a low-distortion sine wave output is obtained at the output (pin 11 of XR-2208).

The circuit of Figure 7 can operate as a sine wave converter, over a frequency band between two frequencies f_H and f_L corresponding to the upper and lower lock ranges of the PLL. With the components shown in the figure, this corresponds to approximately ±30% bandwidth around the center frequency, f_O, for inputs with close to 50% duty cycle. For periodic inputs with less than 50% duty cycle, this lock range is reduced further. For example, for inputs with 20% duty cycle, this bandwidth drops to about ±10% of center frequency. The operation of the circuit with input signals having less than 10% (or more than 90%) duty cycle is not practical. The minimum input level required for circuit operation is 10 mV rms. The circuit can generate a nearly sinusoidal output with input signals from very low



R_X = Distortion Adj. Potentiometer
R_F = Output Amplitude Adj. Pot.

C_C = Coupling Capacitor ($\geq$0.1 μF)

Figure 7. Recommended Circuit Connection for the Regenerative Sinewave Converter.

frequencies up to 100 kHz. Typical distortion characteristics of the output are shown in Figure 8, as a function of frequency of operation. Figure 9 shows a typical example of input and output waveforms for sine converter circuit of Figure 7, operating at 1 kHz input repetition rate, with a noisy input signal.

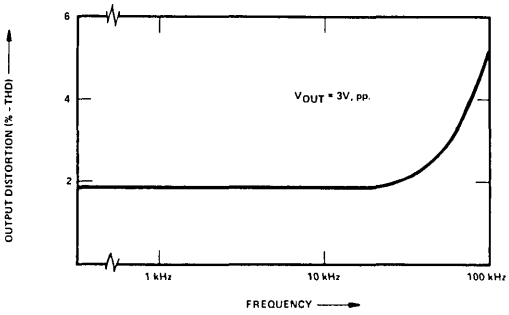


Figure 8. Output Distortion vs Frequency.

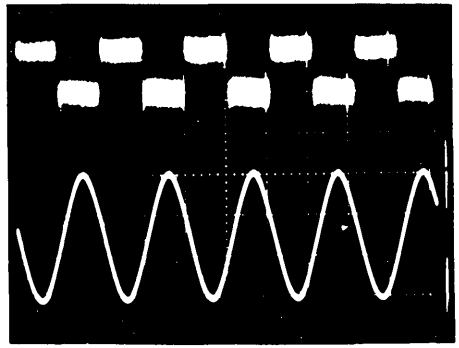


Figure 9. Typical Input-Output Waveforms.

(Top: Noisy Input Signal; Bottom: Sinusoidal Output.)
Scale: Vertical: 1 Volt/Div.
Horizontal: 1 m Sec./Div.

Designing High-Frequency Phase-Locked Loop Carrier-Detector Circuits

INTRODUCTION

The phase-locked loop (PLL) system can be converted to a frequency-selective tone- or carrier-detection system by the addition of a quadrature detector section to the basic PLL. Such a carrier-detect system serves as a lock indicator for the PLL and produces a logic signal at its output when there is a tone or a carrier signal present within the lock range of the phase-locked loop.

A number of monolithic tone-decoder ICs have been developed which implement the quadrature-detection technique for detection of low frequency tones, such as those used for telephone dialing or ultrasonic remote control. However, because of the particular PLL designs used in these monolithic detectors, their applications are limited to frequencies below 100 kHz. This application note describes a circuit approach, using the XR-210 or the XR-215 high frequency PLLs, along with the XR-2228 monolithic multiplier/detector, which extends phase-locked loop tone detection capabilities to frequencies up to 20 MHz.

PRINCIPLES OF OPERATION

The basic block diagram of a phase-locked loop tone detector system is shown in Figure 1. Such a detector system produces a logic-level signal at its output, when the PLL is locked on an input signal. It is made up of two main sections:

1. A PLL section which synchronizes or locks on the input signal.
2. A quadrature detector section made up of a phase-detector, a low-pass filter and a voltage-comparator.

The principle of operation can be briefly described as follows: When the PLL is locked on an input signal, its voltage-controlled oscillator (VCO) section produces a set of input signals, Φ_1 and Φ_1, which are 90° apart in phase, but have the same frequency as the input signal to be detected. One of these signals, Φ_1, is used to drive the PLL phase detector; the other output, which is called the "quadrature output" is used to drive a quadrature phase-detector, as shown in Figure 1. If the PLL is locked on the input signal, then the input signal and the VCO signal applied to the quadrature phase-detector are coherent in phase and frequency. This causes a DC level shift at the low-pass filtered output of the quadrature phase-detector and makes the voltage comparator output change its output logic state. Thus, an output logic signal is produced indicating the lock condition of the PLL.

This type of tone detection technique is a special case of the synchronous AM detection principle, discussed in detail in Exar's Application Note AN-13. The key difference between the tone detection and the synchronous AM detection application is that, in the case of the tone detection, a binary logic output is produced, corresponding to the *presence* or the *absence* of the desired input tone, rather than an analog demodulated signal.

XR-210 and XR-215 HIGH FREQUENCY PLL CIRCUITS

The XR-210 and the XR-215 are high frequency phase-locked loop detector and demodulator circuits. Their functional block diagrams are shown in Figures 2 and 3. Both circuits are packaged in 16-pin dual-in-line packages and contain high frequency VCO and phase-detector sections. The XR-215 chip also contains an operational amplifier. In the case of the XR-210, this op amp section is replaced by a high-gain voltage comparator which drives an open-collector type logic output. The XR-210 is particularly intended for FSK demodulation and can operate up to 20 MHz. The XR-215 is designed for linear FM detection and is suitable for frequencies up to 35 MHz. Except for the frequency capability of the VCO, the oscillator and the phase-comparator sections of both circuits are quite similar.

The VCO section of the XR-210 or the XR-215 does not provide a separate quadrature output, which is 90° phase-shifted with respect to the basic VCO output (Pin 15). However, the triangular output available across the VCO timing capacitor terminals (Pins 13 and 14) can

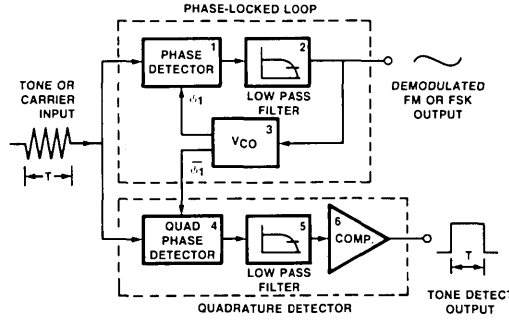


Figure 1. Functional Block Diagram of a PLL Tone- or Carrier-Detector System.

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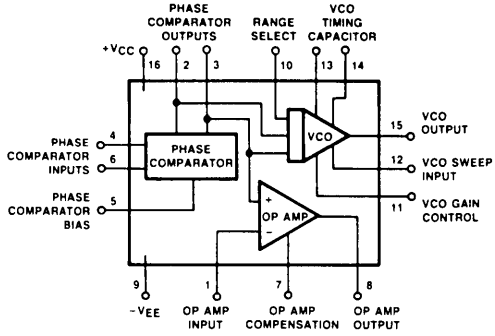

Figure 2. Functional Block Diagram of XR-210 High-Frequency FSK Modulator/Demodulator.

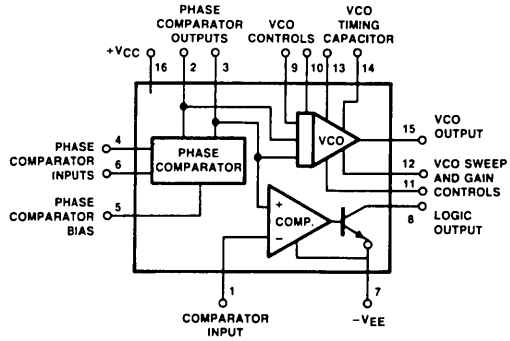

Figure 3. Functional Block Diagram of XR-215 High-Frequency Phase-Locked Loop.

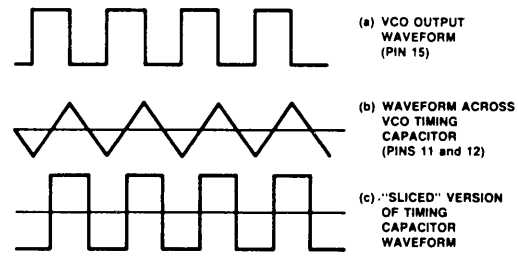

Figure 4. Timing Diagram of VCO Output Waveforms Available from XR-210 or XR-215 High-Frequency PLL Circuits.

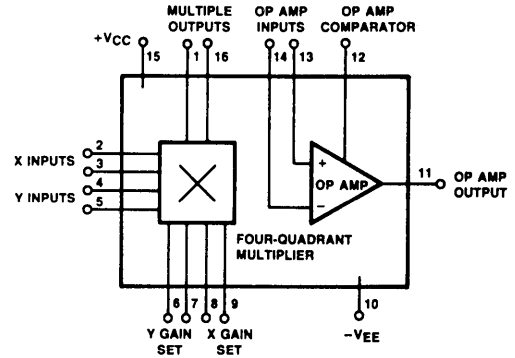

Figure 5. Functional Block Diagram of XR-2228 Multiplier/Detector.

serve as such a quadrature output if it is amplified and "sliced" externally, as shown in the timing diagram of Figure 4.

XR-2228 MULTIPLIER/DETECTOR CIRCUIT

The XR-2228 is comprised of a four-quadrant multiplier and a high-gain op amp on a single monolithic chip. It is packaged in a 16-pin dual-in-line package and has the functional block diagram shown in Figure 5. It contains independent and fully differential X- and Y-inputs which makes it easy to interface with the XR-210 or the XR-215 type PLL circuit for carrier-detection applications. In the tone- or carrier-detect application, the multiplier section of the XR-2228 is used as the quadrature phase-detector section of the block diagram of Figure 1. The op amp is used as a high-gain voltage comparator which converts the differential voltage level changes at the multiplier outputs into logic level output signals.

CIRCUIT OPERATION

Figure 6 shows the generalized circuit connection of the XR-2228, along with either the XR-210 or the XR-215 high frequency PLL IC, for tone- or carrier-detection application. Since the external connections for the XR-210 or the XR-215 are the same as those given in their respective data sheets, only the external circuitry associated with the XR-2228 is shown in the figure. The circuit, as shown, can operate with a single power supply, from 10 V to 20 V, or with split supplies in the range of ± 5 V to ± 10 V. In the case of split power supplies, the resistor string biasing the input terminals of the XR-2228 is not necessary and can be eliminated by connecting node A of Figure 6 to ground.

The input signal is AC coupled, with separate coupling capacitors, both to the input of the particular PLL circuit to be used, and to the X-input terminal (Pin 2) of the XR-2228.

The Y-inputs (Pins 4 and 5) are driven differentially from the VCO timing capacitor signal (available at Pins 13 and 14 of the PLL IC) which is AC coupled to Pins 4 and 5 of the XR-2228 multiplier input. The multiplier input stage "slices" this signal to produce the quadrature frequency waveform shown in Figure 4(c).

The differential DC voltage level at the multiplier output terminals (Pins 1 and 6) is offset by means of an external resistor, R_A, as shown in Figure 6. This initial offset causes the op amp output of the XR-2228 to settle to a known state when there is no carrier or tone signal to be detected. With the op amp input connections as shown in Figure 6, the op amp output (Pin 11) would be

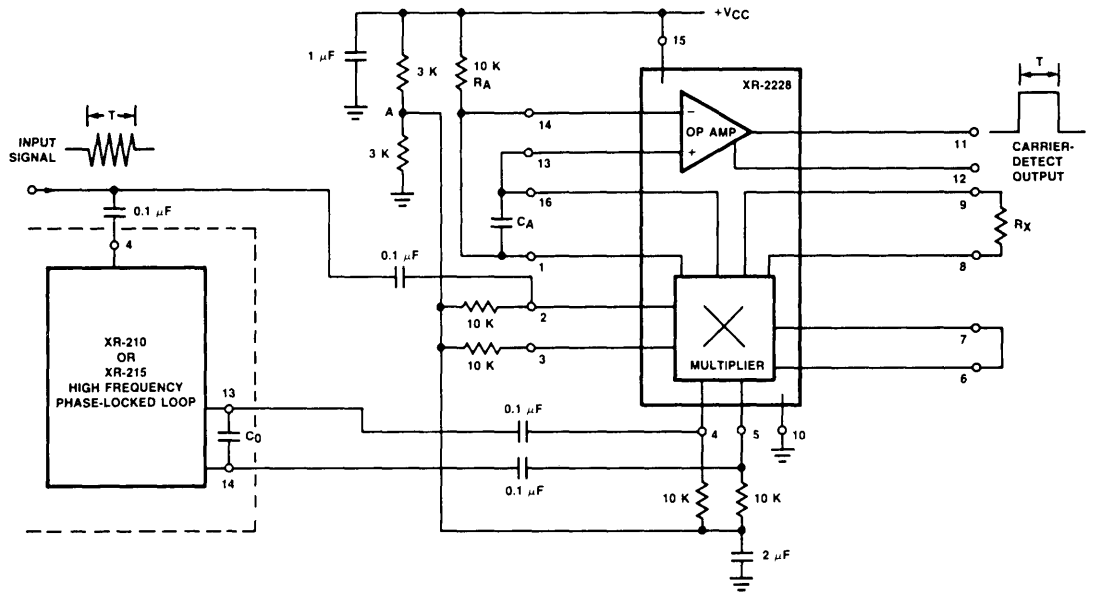

Figure 6. Recommended Circuit Connection of the XR-2228 with the XR-210 or the XR-215 High-Frequency Phase-Locked Loops for Tone- or Carrier-Detector Application.

at a "low" state when the PLL is not locked on a tone, and goes to a "high" state (near $+V_{CC}$) when the PLL circuit is locked on to an input tone. The output logic polarity can be reversed simply by reversing the op amp inputs.

The filter capacitor, C_A, connected across Pins 1 and 16 of the multiplier outputs, serves as the post-detection low-pass filter (Block 5 of Figure 1). The time constant of this filter is equal to (C_A R_B where R_B (≈ 8 KΩ is the internal resistance of the IC at Pins 1 and 16. The value of C_A is chosen to provide a compromise between the response time and the spurious noise rejection characteristics of the circuit: increasing C_A improves the noise rejection characteristics of the circuit, but slows down the response time.

The detection threshold (minimum detectable input signal amplitude) varies inversely with the multiplier gain-setting resistor R_X. Figure 7 shows the typical detectable signal level, as a function of R_X, with the output offset resistor, R_A, equal to 10 KΩ. Note that the minimum detectable input signal, with $R_X = 0$, is approximately 100 mV, rms.

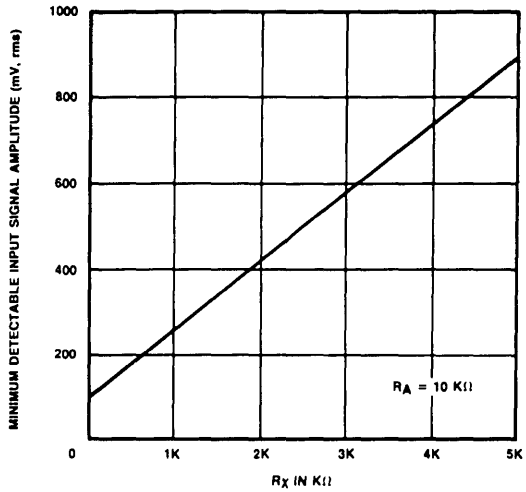

Figure 7. Minimum Detectable Input Carrier Level, as a Function of Multiplier Gain Setting Resistor, R_X.

Frequency-Selective AM Detection using Monolithic Phase-Locked Loops

INTRODUCTION

This application note describes the use of monolithic phase-locked loop (PLL) circuits in detection of amplitude-modulated (AM) signals. The detection capabilities of a PLL system, which is a frequency-selective FM demodulator, can be extended to cover AM signals simply by the addition of an analog multiplier (or mixer) and a low-pass filter to the basic phase-locked loop. This technique of AM demodulation, which is called synchronous AM detection, offers significant performance advantages over conventional peak-detector type AM demodulators, in terms of its dynamic range and noise characteristics.

This application note outlines some of the fundamental principles of synchronous AM detectors, and gives design examples using the XR-2228 multiplier/detector IC in conjunction with the XR-215 and the XR-2212 monolithic PLL circuits.

PRINCIPLES OF OPERATION

The phase-locked loop AM detector circuits operate on the so-called "coherent AM detection" principle, where the amplitude modulated input signal is mixed with an unmodulated "coherent" carrier signal, and then low-pass filtered to produce the desired demodulated output signal. Figure 1 gives a simplified block diagram of such a detector system.

The amplitude-modulated input signal can be described by an expression of the form:

$$\text{Input Signal} = V_m(t) \cos \omega_0 t$$

where $V_m(t)$ is the modulated amplitude of the input signal and ω_0 is the input signal frequency expressed in radians. If this signal is linearly multiplied with an *unmodulated* signal which has the *same* frequency and phase as the input signal, then the output of the multiplier, $V_0(t)$, is a composite signal of the form:

$$V_0(t) = K_0 V_m(t) [1 + \cos (2 \omega_0 t)]$$

where K_0 is the gain of the multiplier circuit. If the above signal is then passed through a low-pass filter, to eliminate the double-frequency term, the resulting output signal is:

$$V_{out} = \text{Output Signal} = K_0 V_m(t)$$

which corresponds to the detected AM information.

The phase-locked loop AM detectors also operate on a similar principle: the PLL is made to "lock" on the carrier frequency of the input AM signal; then the VCO output of the PLL will regenerate the unmodulated coherent carrier signal necessary for detection. When this signal is mixed with the input AM signal and the resulting composite signal is passed through a low pass filter, one obtains the demodulated output. Figure 2 gives a block diagram of such an AM detector system. Compared to the basic synchronous AM detector system of Figure 1, the phase-locked loop AM detector of Figure 2 also has one added feature: the output of the PLL control voltage (i.e., output of the PLL low-pass filter) can be used as an FM detector or a frequency discriminator. Thus, such a system is capable of simultaneous AM and FM detection. In other words, the frequency and the amplitude modulation information present on the input signal can be *separately* and *simultaneously* demodulated. The particular design and application examples given in this application note fall into this category.

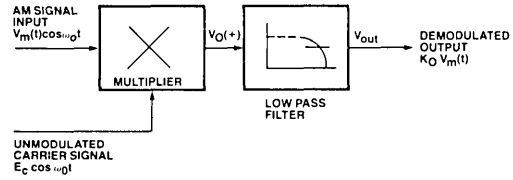

Figure 1 Block Diagram of a Synchronous AM Detector.

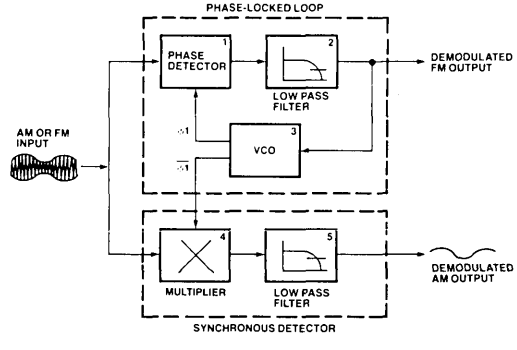

Figure 2. The Basic Phase-Locked Loop AM Detector.

XR-2212 AND XR-2228 MONOLITHIC CIRCUITS

The XR-2212 monolithic PLL is made up of an input preamplifier, a phase-detector, a high-gain differential amplifier and a stable voltage-controlled oscillator (VCO) as shown in Figure 3. The key feature of the XR-2212 PLL is the temperature stability and the frequency accuracy of its VCO section; it offers 20 ppm/°C typical temperature stability and a frequency accuracy of ± 1% for an external RC setting. The oscillator section of the XR-2212 contains a separate "quadrature output" terminal (Pin 15) which is particularly intended for interfacing with a synchronous AM detector such as the XR-2228.

The XR-2228 multiplier/detector IC is specifically intended as a basic building block for synchronous AM detection. It contains a four-quadrant analog multiplier and a high-gain op amp on the same chip, as shown in the functional block diagram of Figure 4.

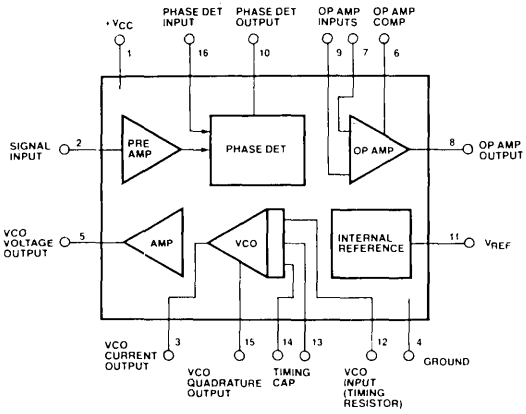

Figure 3. Functional Block Diagram of XR-2212 Precision Phase-Locked Loop.

XR-215 HIGH FREQUENCY PHASE-LOCKED LOOP

The XR-215 is a high frequency phase-locked loop circuit capable operating with input signal frequencies up to 35 MHz. It is comprised of a high frequency VCO, a phase-detector and an op amp section, as shown in the block diagram of Figure 5.

Unlike the XR-2212 PLL, the VCO section of the XR-215 does not have a separate quadrature output terminal. However, such a quadrature oscillator signal can be obtained by amplifying and "slicing" the triangle waveform available across the timing capacitor (Pins 13 and 14) of the XR-215 oscillator section. Figure 6 shows the relative phase relationship of these oscillator waveforms available from the circuit. The desired quadrature output signal (curve C of Figure 6) can be obtained by directly connecting one pair of the differential inputs of the XR-2228 directly across the timing capacitor terminals of the XR-215.

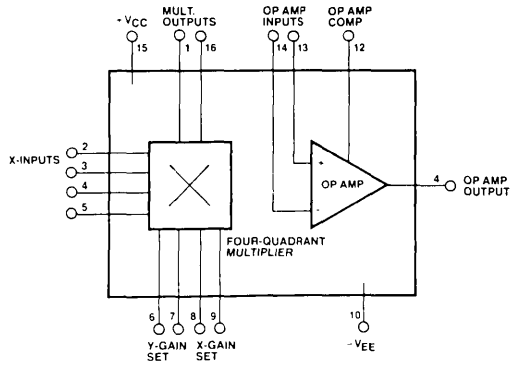

Figure 4. Functional Block Diagram of XR-2228 Multiplier/Detector IC.

AM/FM DETECTION USING THE XR-2212 PLL

Figure 7 shows a generalized circuit connection diagram for a two-chip AM and FM detection system, utilizing the XR-2212 PLL and the XR-2228 multiplier/detector. The XR-2212 section serves as the basic FM detector. The quadrature output of its VCO (Pin 15) is AC coupled to the Y input of the XR-2228.

The Y input of the XR-2228 is operated in its switching mode, with the Y gain terminals (Pins 6 and 7) shorted together. The AM and/or FM signal is simultaneously applied to both circuits through coupling capacitors; and all the mutliplier inputs are DC biased from the internal reference output of the XR-2212 (Pin 11). The output of the multiplier, at Pin 16, is AC coupled to the op amp section of the XR-2228, which serves as the post-detection amplifier for the demodulated AM signal.

The circuit configuration shown in Figure 7 can operate with a single power supply, over the supply voltage range, of 10V to 20V. Its operation or performance can be tailored for any particular AM and FM detection application by the choice external components shown in the figure, over a carrier frequency band of 1 kHz to

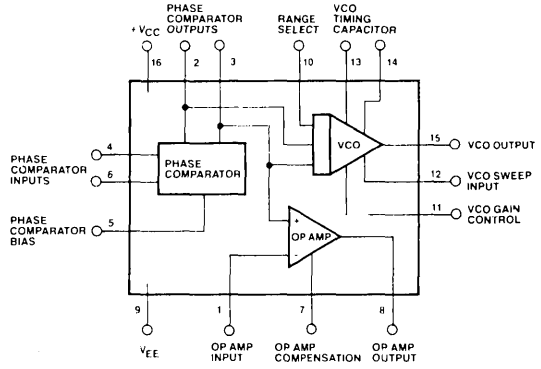

Figure 5. Functional Diagram of XR-215 High-Frequency Phase-Locked Loop.

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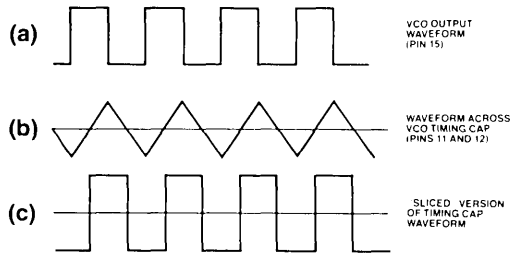


Figure 6. Timing Diagrams of VCO Output Waveforms from XR-215 Monolithic Phase-Locked Loop.

300 kHz. The functions of these external components are as follows:

a) R_0 and C_0 set the VCO center frequency for the XR-2212 PLL circuit. The center frequency, f_o, is given as:

$$f_0 = \frac{1}{R_0 C_0}$$

The VCO frequency f_0 is chosen to be equal to the carrier frequency of the input signal. R_0 is normally chosen to be in the range of 10 kΩ to 100 kΩ. This choice is arbitrary. For most applications $R_0 \approx 20$ kΩ is recommended. Once f_0 is given and R_0 is chosen, the C_0 can be calculated from the above equation.

b) R_1 determines the tracking bandwidth of the PLL. For a required tracking bandwidth, Δf (see Figure 9 of XR-2212 data sheet) and f_0, R_1 can be calculated as:

$$R_1 = R_0 \frac{f_0}{\Delta f}$$

This tracking bandwidth, Δf, is the band of frequencies in the vicinity of f_0, over which the PLL can maintain lock.

c) C_1 sets the loop-damping factor for the PLL. For most applications, C_1 is chosen to be equal to one-half of C_0.

d) R_2 and C_2 form a low-pass filter for the detected FM signal. The 3 dB frequencing, f_2, of this low-pass filter is:

$$f_2 = \frac{1}{2\pi R_2 C_2}$$

Normally, f_2 is chosen to be equal to the demodulated FM information bandwidth.

e) R_C and R_{F1} set the gain of the op amp section of the XR-2212 as:

$$A_V = 1 + \frac{R_{F1}}{R_C}$$

This op amp section serves as the post-detection amplifier for the demodulated FM signals.

f) R_X sets the multiplier gain for the X input and R_{F2} sets the gain of the op amp section of the XR-2228. Thus, the demodulated AM signal output swing, V_{out}, for a given input signal of peak amplitude of V_M and modulation index of m ($0 \leq m \leq 1$) can be approximated as:

$$V_{out} = \frac{(V_M)m}{4} \frac{R_{F2}}{R_X}$$

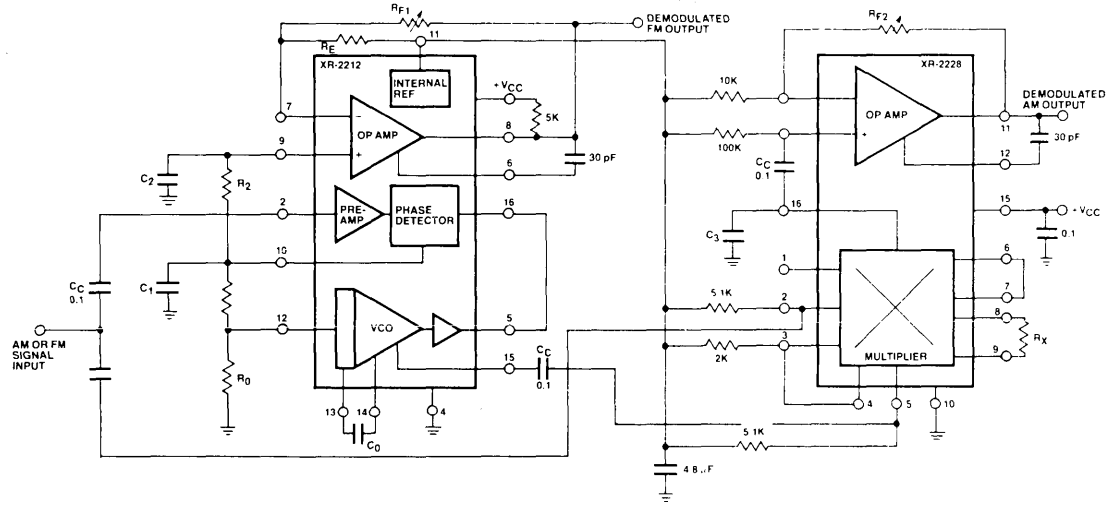


Figure 7. A Two-Chip AM/FM Detector System Using the XR-2212 Phase-Locked Loop and the XR-2228 Multiplier/Detector.

Thus, for example, a 100 mV peak input signal with 30% AM modulation (m = 0.3) will give a demodulated output of 150 mV peak, with R_{F2} = 100 kΩ and R_X = 5 kΩ, at Pin 11 of the XR-2228.

g) C_3, in conjunction with the 5 kΩ internal impedance of the multiplier output (Pin 16) serves as the low-pass post-detection filter for the demodulated AM signal.

For further explanation and description for the system design equations, the reader is referred to the XR-2212 and the XR-2228 data sheets.

Design Example

Design an AM demodulator for 100 kHz carrier frequency with a detection (tracking) bandwidth of ±4%. The demodulated information bandwidth is 3 kHz and an output level of one volt peak is required for a one volt peak input with 30% modulation.

Using the circuit of Figure 7, one proceeds as follows: Since FM detection is not required in this example, components R_2, C_2, R_C and R_{F1} are not essential to circuit operation. R_2 and R_C can be short-circuited, C_2 and R_{F1} can be left open-circuited. The rest of the component values are calculated as follows:

Step 1) Set f_0 = 100 kHz by choosing R_0 = 20 kΩ and calculating C_0 from paragraph (a) above.

$$C_0 = \frac{1}{R_0 f_0} = 500 \text{ pF}$$

Step 2) Determine R_1 to set tracking bandwidth to ± 4%, from paragraph (b): R_1 = 500 kΩ.

Step 3) Calculate C_1:$C_1 \approx C_0/2 \approx 250$ pF.

Step 4) From paragraph (f), calculate the value of R_X and R_{F2}. For a typical choice of R_X = 5 kΩ, and m = 0.3 (30% modulation) with one volt input carrier level, the value of R_{F2} to get one volt demodulated output is: R_{F2} = 67 kΩ.

Step 5) Calculate C_3 to get 3 kHz bandwidth for post-detection filter: $C_3 \approx 0.01$ μF.

AM DETECTION USING THE XR-215 PLL

Figure 8 shows the circuit connection diagram for a two-chip AM and FM detection system, using the XR-215 high-frequency PLL in conjunction with the XR-2228 multiplier/detector. Because of the high-frequency capability of the XR-215, the circuit of Figure 8 is useful as a phase-locked AM detector for carrier frequencies up to 20 MHz, and operates over a supply voltage range of 10V to 20V.

The VCO section of XR-215 does not have a separate quadrature output. However, this problem can be overcome by driving the XR-2228 multiplier directly from the timing capacitor terminals (Pins 13 and 14) of XR-215. The Y input of the XR-2228 is operated with maximum gain, since the Y gain control terminals (Pins 6 and 7) are shorted together. This causes the triangular waveform across C_0 to be converted to an effective quadrature drive as indicated by the timing diagram of Figure 6. The modulated input signal is simultaneously applied to both circuits through coupling capacitors. The phase-detector inputs of the XR-215, as well as the multiplier X inputs of the XR-2228, are biased at approximately one-half of V_{CC}, by means of an external resistive divider.

In Figure 8, C_0 sets the VCO frequency of the XR-215. In the case of FM demodulation, R_1 and C_1 serve as the post-detection filter for the detected FM signal and R_{F1} sets the gain of the FM post-detection amplifier.

The mode of operation of the XR-2228 is virtually the same as that described in connection with Figure 7: R_X sets the multiplier demodulation gain; C_3 serves as the low-pass post-detection filter. The values of R_X, R_{F2} and C_3 are calculated as given in paragraphs (f) and (g).

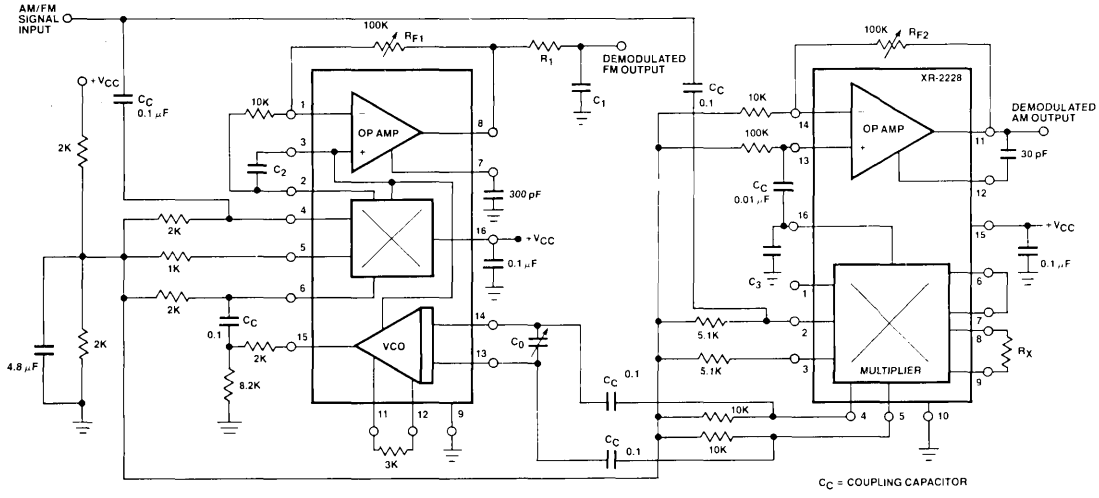


Figure 8. Circuit Connection for a High-Frequency AM and FM Detector Using the XR-215 and XR-2228.

High-Quality Function Generator System with the XR-2206

INTRODUCTION

Waveform or function generators capable of producing AM/FM modulated sine wave outputs find a wide range of applications in electrical measurement and laboratory instrumentation. This application note describes the design, construction and the performance of such a complete function generator system suitable for laboratory usage or hobbyist applications. The entire function generator is comprised of a single XR-2206 monolithic IC and a limited number of passive circuit components. It provides the engineer, student, or hobbyist with a highly versatile laboratory instrument for waveform generation at a very small fraction of the cost of conventional function generators available today.

GENERAL DESCRIPTION

The basic circuit configuration and the external components necessary for the high-quality function generator system is shown in Figure 1. The circuit shown in the figure is designed to operate with either a 12 V single power supply, or with ±6 V split supplies. For most applications, split-supply operation is preferred since it results in an output dc level which is nearly at ground potential.

The circuit configuration of Figure 1 provides three basic waveforms: since, triangle and square wave. There are four overlapping frequency ranges which give an overall frequency range of 1 Hz to 100 kHz. In each range, the frequency may be varied over a 100:1 tuning range.

The sine or triangle output can be varied from 0 to over 6 V (peak to peak) from a 600 ohm source at the output terminal.

A squarewave output is available at the sync output terminal for oscilloscope synchronizing or driving logic circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

The performance characteristics listed below are not guaranteed or warranted by Exar. However, they represent the typical performance characteristics measured by Exar's application engineers during the laboratory evaluation of the function generator system shown in Figure 1. The typical performance specifications listed below apply only when all of the recommended assembly instructions and adjustment procedures are followed:

(a) Frequency Ranges: The function generator system is designed to operate over four overlapping frequency ranges:

1 Hz to 100 Hz
10 Hz to 1 kHz
100 Hz to 10 kHz
1 kHz to 100 kHz

The range selection is made by switching in different timing capacitors.

(b) Frequency Setting: At any range setting, frequency can be varied over a 100:1 tuning range with a potentiometer (see R_{13} of Figure 1).

(c) Frequency Accuracy: Frequency accuracy of the XR-2206 is set by the timing resistor R and the timing capacitor C, and is given as:

$$f = 1/RC$$

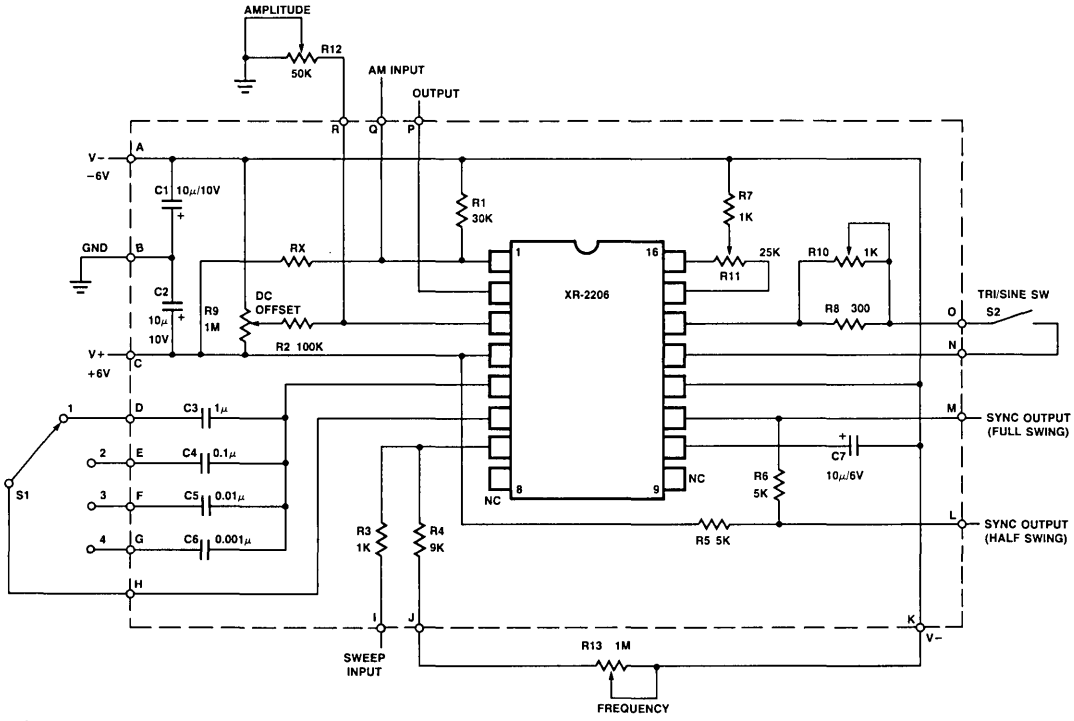
The above expression is accurate to within ±5% at any range setting. The timing resistor R is the series combination of resistors R_4 and R_{13} of Figure 1. The timing capacitor C is any one of the capacitors C_3 through C_6, shown in the figure.

(d) Sine and Triangle Output: The sine and triangle output amplitudes are variable from 0 V to 6 V_{pp}. The amplitude is set by an external potentiometer, R_{12} of Figure 1. At any given amplitude setting, the triangle output amplitude is approximately twice as high as the sinewave output. The internal impedance of the output is 600 Ω.

(e) Sinewave Distortion: The total harmonic distortion of sinewave is less than 1% from 10 Hz to 10 kHz and less than 3% over the entire frequency range. The selection of a waveform is made by the triangle/sine selector switch, S_2.

(f) Sync Output: The sync output provides a 50% duty cycle pulse output with either full swing or upper half swing of the supply voltage depending on the choice of sync output terminals on the printed circuit board (see Figure 1).

(g) Frequency Modulation (External Sweep): Frequency can be modulated or swept by applying an external control voltage to sweep terminal (Terminal I of Figure 1). When not used, this terminal should be left open-



NOTE:

1. For Single Supply Operation Lift GND Connection Keeping R12 Across Terminals R and B Intact, and Connect Terminal A to GND.

2. For Maximum Output, R_X may be open. R_X = 68 KΩ is Recommended for External Amplitude Modulation.

Figure 1. Circuit Connection Diagram for Function Generator. (See Note 1 for Single Supply Operation.)

circuited. The open circuit voltage at this terminal is approximately 3V above the negative supply voltage and its impedance is approximately 1000 ohms.

(h) Amplitude Modulation: The output amplitude varies linearly with modulation voltage applied to AM input (terminal Q of Figure 1). The output amplitude reaches its minimum as the AM control voltage approaches the half of the total power supply voltage. The phase of the output signal reverses as the amplitude goes through its minimum value. The total dynamic range is approximately 55 dB, with AM control voltage range of 4V referenced to the half of the total supply voltage. When not used, AM terminal should be left open-circuited.

(i) Power Source: Split supplies: ±6 V, or single supply: + 12 V. Supply Current 15 mA (see Figure 3).

EXPLANATION OF CIRCUIT CONTROLS:

Switches

Range Select Switch, S1: Selects the frequency range of operation for the function generator. The frequency is inversely proportional to the timing capacitor connected across Pins 5 and 6 of the XR-2206 circuit. Nominal capacitance values and frequency ranges corresponding to switch positions of S1 are as follows:

Position	Nominal Range	Timing Capacitance
1	1 Hz to 100 Hz	1 μF
2	10 Hz to 1 kHz	0.1 μF
3	100 Hz to 10 kHz	0.01 μF
4	1 Hz to 100 kHz	0.001 μF

If additional frequency ranges are needed, they can be added by introducing additional switch positions.

Triangle/Sine Waveform Switch, S2: Selects the triangle or sine output waveform.

Trimmers and Potentiometers

Dc Offset Adjustment, R9: The potentiometer used for adjusting the dc offset level of the triangle or sine output waveform.

Sinewave Distortion Adjustment, R10: Adjusted to minimize the harmonic content of sinewave output.

Sinewave Symmetry Adjustment, R11: Adjusted to optimize the symmetry of the sinewave output.

Amplitude Control, R12: Sets the amplitude of the triangle or sinewave output.

Frequency Adjust, R13: Sets the oscillator frequency for any range setting of S1. Thus, R13 serves as a frequency dial on a conventional waveform generator and varies the frequency of the oscillator over an approximate 100 to 1 range.

Terminals

A. Negative Supply -6V
B. Ground
C. Positive Supply +6V
D. Range 1, timing capacitor terminal
E. Range 2, timing capacitor terminal
F. Range 3, timing capacitor terminal
G. Range 4, timing capacitor terminal
H. Timing capacitor common terminal
I. Sweep Input
J. Frequency adjust potentiometer terminal
K. Frequency adjust potentiometer negative supply terminal
L. Sync output (1/2 swing)
M. Sync output (full swing)
N. Triangle/sine waveform switch terminals
O. Triangle/sine waveform switch terminals
P. Triangle or sinewave output
Q. AM input
R. Amplitude control terminal

PARTS LIST

The following is a list of external circuit components necessary to provide the circuit interconnections shown in Figure 1.

Capacitors:

C1, C2, C7	Electrolytic, 10 μF, 10V
C3	Mylar, 1 μF, nonpolar, 10%
C4	Mylar, 0.1 μF, 10%
C5	Mylar, 0.01 μF, 10%
C6	Mylar, 1000 pF, 10%

Resistors:

R1	30 KΩ, 1/4 W, 10%
R2	100 KΩ, 1/4 W, 10%
R3, R7	1 KΩ, 1/4 W, 10%
R4	9 KΩ, 1/4 W, 10%
R5, R6	5 KΩ, 1/4 W, 10%
R8	300 KΩ, 1/4 W, 10%
RX	62 KΩ, 1/4 W, 10% (RX can be eliminated for maximum output)

Potentiometers:

R9	Trim, 1 MΩ, 1/4 W
R10	Trim, 1 KΩ, 1/4 W
R11	Trim, 25 KΩ, 1/4 W

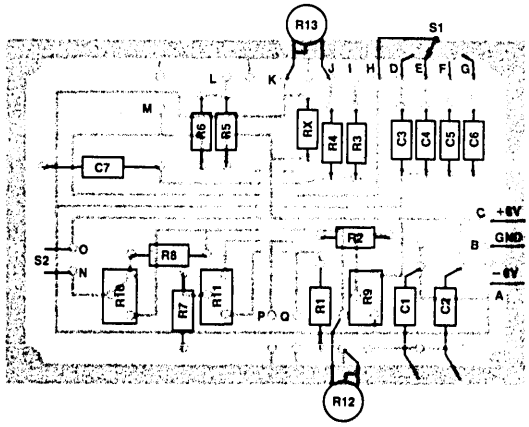
The following additional items are recommended to convert the circuit of Figure 1 to a complete laboratory instrument:

Potentiometers:

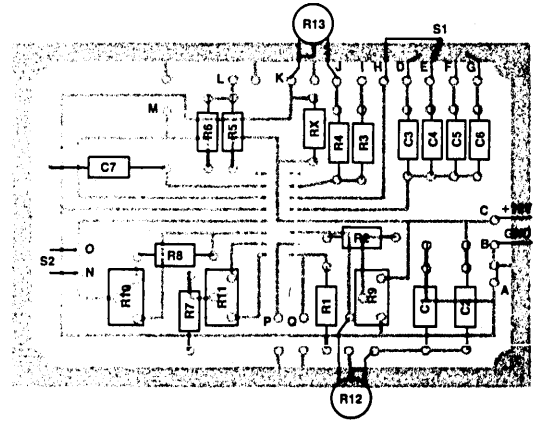
R12	Amplitude control, linear, 50 KΩ
R13	Frequency control, audio taper, 1 MΩ

Switches:

S1	Rotary switch, 1-pole, 4 positions
S2	Toggle or slide, SPST



(a) Split Supply PC Board Layout



(b) Single Supply PC Board Layout

Figure 2. Recommended PC Board Layout for Function Generator Circuit of Figure 1.

Case:

7″ × 4″ × 4″ (approx.) Metal or Plastic
(See Figures 4(a) and 4(b).)

Power Supply:

Dual supplies ±6 V or single +12 V
Batteries or power supply unit
(See Figures 3(a) and 3(b).)

Miscellaneous:

Knobs, solder, wires, terminals, etc.

BOARD LAYOUT

Figures 2(a) and 2(b) show the recommended printed-circuit board layout for the function generator circuit of Figure 1.

RECOMMENDED ASSEMBLY PROCEDURE

The following instructions and recommendations for the assembly of the function generator assume that the basic PC board layout of Figure 2(a) or 2(b) is used in the circuit assembly.

All the parts of the generator, with the exception of frequency adjust potentiometer, amplitude control potentiometer, triangle/sine switch and frequency range select switch, are mounted on the circuit board.

Install and solder all resistors, capacitors and trimmer resistors on the PC board first. Be sure to observe the polarity of capacitors C1, C2, C7. The timing capacitors C3, C4, C5 and C6 must be non-polar type. Now install IC1 on the board. We recommend the use of an IC socket to prevent possible damage to the IC during soldering and to provide for easy replacement in case of a malfunction.

The entire generator board along with power supply or batteries and several switches and potentiometers will fit into a case of the type readily available at electronic hobby shops. It will be necessary to obtain either output jacks or terminals for the outputs and am and frequency sweep inputs.

Install the frequency adjust pot, the frequency range select switch, the output amplitude control pot, the power switch, and the triangle/sine switch on the case. Next, install the PC board in the case, along with a power supply.

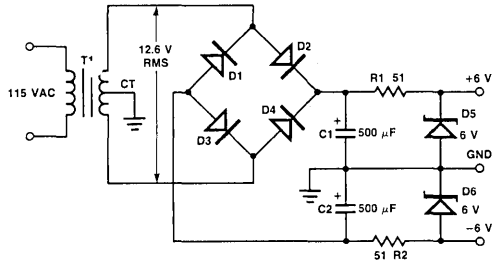
Any simple power supply having reasonable regulation may be used. Figure 3 gives some recommended power supply configurations.

Precaution: Keep the lead lengths small for the range selector switch.

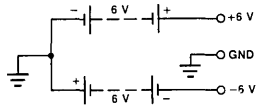
ADJUSTMENT PROCEDURE

When assembly is completed and you are ready to put the function generator into operation, make sure that the polarity of power supply and the orientation of the IC unit are correct. Then apply the dc power to the unit.

To adjust for minimum distortion, connect the scope probe to the triangle/sine output. Close S2 and adjust the amplitude control to give non-clipping maximum swing. Then adjust R10 and R11 alternately for minimum distortion by observing the sinusoidal waveform. If a distortion meter is available, you may use it as a final check on the setting of sine-shaping trimmers. The minimum distortion obtained in this manner is typically less than 1% from 1 Hz to 10 kHz and less than 3% over the entire frequency range.



(a) Zener Regulated Supply



(b) Battery Power Supply

T1: Filament Transformer
Primary 115V/Secondary 12.6 VCT, 0.5A
D1 — D4: IN4001 or Similar
D5, D6: IN4735 or similar
R1, R2: 51Ω, 1/2W, 10%

Figure 3. Recommended Power Supply Configurations.

An Electronic Music Synthesizer using the XR-2207 and the XR-2240

INTRODUCTION

This application note describes a simple, low-cost "music synthesizer" system made up of two monolithic IC's and a minimum number of external components. The electronic music synthesizer is comprised of the XR-2207 programmable tone generator IC which is driven by the pseudo-random binary pulse pattern generated by the XR-2240 monolithic counter/timer circuit.

PRINCIPLES OF OPERATION

All the active components necessary for the electronic music synthesizer system is contained in the two low-cost monolithic IC's, the XR-2207 variable frequency oscillator and the XR-2240 programmable counter/timer. Figure 1 shows the functional block diagram of the XR-2207 oscillator. This monolithic IC is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal current switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The XR-2240 programmable counter/timer is comprised of an internal time-base oscillator, a control flip-flop and a programmable 8-bit binary counter. Its functional block diagram is shown in Figure 2, in terms of the 16-pin IC package. The eight separate output terminals of the XR-2240 are "open-collector" type outputs which can either be used individually, or can be connected in a "wired-or" configuration.

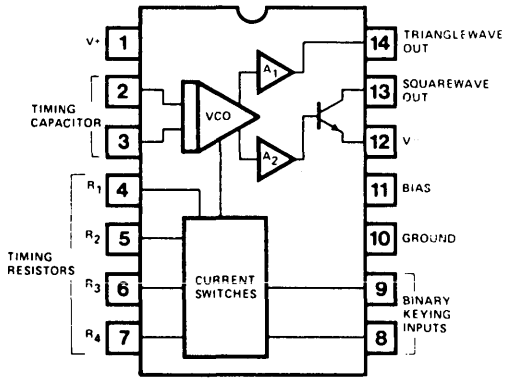


Figure 1. Functional Block Diagram of XR-2207 Oscillator Circuit.

Figure 3 shows the circuit connection for the electronic music or time synthesizer system using the XR-2207 and the XR-2240. The XR-2207 produces a sequence of tones by oscillating at a frequency set by the external capacitor C_1 and the resistors R_1 through R_6 connected to Pins 4 through 7. These resistors set the frequency or the "pitch" of the output tone sequence. The counter/timer IC generates the pseudo-random pulse patterns by selectively counting down the time-base frequency. The counter outputs of XR-2240 (Pins 1 through 8) then activate the timing resistors R_1 through R_6 of the oscillator IC, which converts the binary pulse patterns to tones. The time-base oscillator frequency of the counter/timer sets the "beat" or the tempo of the music. This setting is done through C_3 and R_0 of Figure 3.

The pulse sequence coming out of the counter/timer IC can be programmed by the choice of counter outputs (Pins 1 through 8 of XR-2240 connected to the programming pins (Pins 4 through 7) of the XR-2207 VCO. The connection of Figure 3 is recommended since it gives a particularly melodic tone sequence at the output.

The pseudo-random pulse pattern out of the counter-timer repeats itself at 8-bit (or 256 count) intervals of the time-base period. Thus, the output tone sequence continues for about 1 to 2 minutes (depending on the "beat") and then repeats itself. The counter/timer resets to zero when the device is turned on; thus, the music, or the tone sequence, always starts from the same point when the synthesizer is turned on.

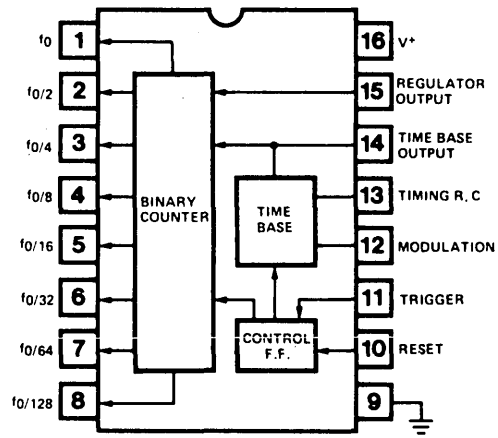


Figure 2. Functional Block Diagram of XR-2240 Counter/Timer.

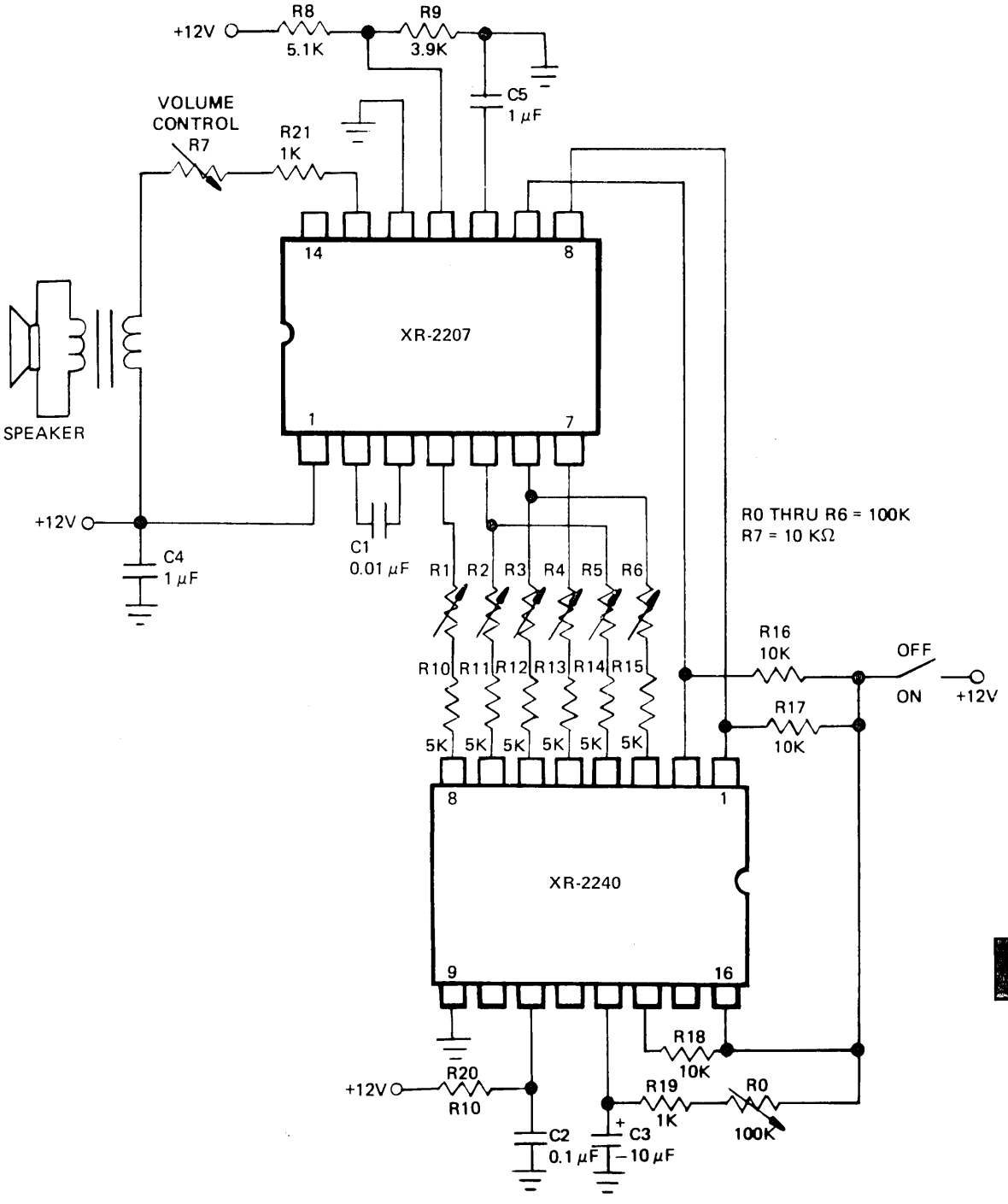


Figure 3. Circuit Connection Diagram for the Music Synthesizer.

Semi-Custom LSI Design with I^2L Gate Arrays

INTRODUCTION

In designing semi-custom monolithic LSI, one uses a partially fabricated silicon wafer which is "customized" by the application of one or more special mask patterns. This technique greatly reduces the design and tooling cost and the prototype fabrication cycle associated with the conventional *full-custom* IC development cycle; and thus makes custom IC's economically feasible even at low production volumes.

Until recently, the application of semi-custom design technology to complex digital systems has been somewhat limited due to one key factor: to be economically feasible, a complex digital LSI chip must achieve a high functional density on the chip (i.e., high gate count per unit chip area). Traditionally, this requirement is not compatible with the random interconnection concept which is key to the semi-custom or master-slice design approach. This paper describes a *new* approach to the master-slice concept which overcomes this age-old problem. It achieves packing densities approaching those of full-custom digital LSI layout while still maintaining the low-cost and the quick turn-around attributes of semi-custom IC design. This is achieved by making use of unique layout and interconnection properties of I^2L gates, and by extending the mask-programming to additional mask layers besides the metal interconnection.

FEATURES OF I^2L TECHNOLOGY

Integrated Injection Logic (I^2L) is one of the most significant recent advances in the area of monolithic LSI technology. Compared to other monolithic LSI technologies, I^2L offers the following unique advantages:

- High Packing Density
- Bipolar Compatible Processing
- Low Power and Low Voltage Operation
- Low (Power x Delay) Product

Figure 1 gives a comparison of the speed and power capabilities of various logic families, including I^2L. Since I^2L technology is a direct extension of the conventional bipolar IC technology, it readily lends itself to combining high-density digital functions on the same chip along with conventional Schottky-bipolar circuitry. The availability of bipolar input-output interface on the same chip along with the high-density I^2L logic makes it very convenient to retrofit custom I^2L designs into many existing logic systems.

The I^2L logic technology is developed around the basic single-input, multiple-output inverter circuit shown in Figure 2. A recommended circuit symbol for this gate circuit is also defined in the figure. Most terminals of the I^2L gate share the same semi-conductor region (for example, the collector of the PNP is the same as the base of the NPN; and the emitter of the NPN is the same as the base of the PNP). This leads to a very compact device structure, and results in very high packing density in monolithic device fabrication. Figure 3 illustrates the basic device structure and the cross-section for a bipolar-compatible I^2L gate. Since the individual I^2L gates do not require separate P-type isolation diffusions, they can be placed in a common N-type tub. This feature greatly enhances the packing density on the chip since it eliminates the need for separate isolation pockets for individual gates. With conventional photomasking and diffusion tolerances, gate densities of greater than 200 gates/mm^2 can be readily achieved in full-custom layout. Using the semi-custom approach which is outlined in this paper, one can maintain a packing density of greater than 120 gates/mm^2 even with random metallization or interconnection requirements. This offers at least a factor of four improvement over conventional bipolar master-slice technology and approximately a factor of two improvement over MOS master-slice approach in terms of gate-density and chip area utilization.

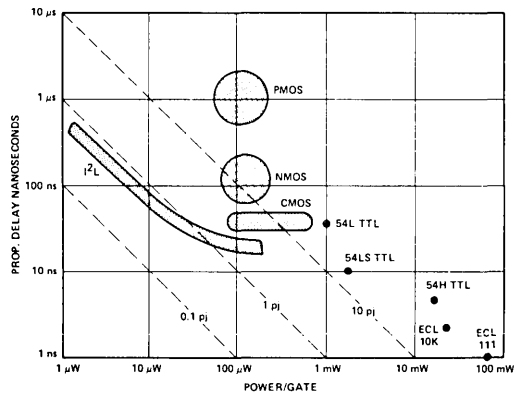


Figure 1. Comparison of Speed and Power Capabilities of Various Logic Families.

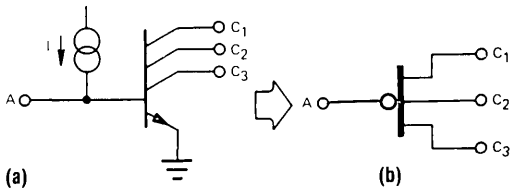


Figure 2. Equivalent Circuit (a), and a Recommended Symbol (b) for an I^2L Gate.

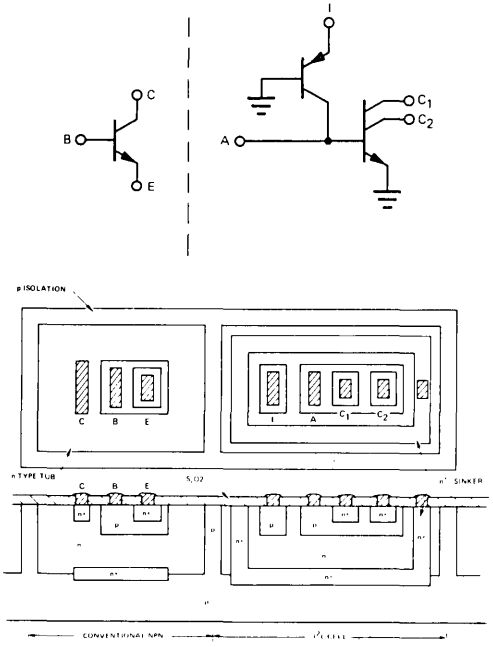


Figure 3. Basic Device Structure for Bipolar Compatible I^2L.

DESIGNING WITH I^2L GATE ARRAYS

A number of I^2L gate arrays have been developed at Exar utilizing bipolar-compatible integrated injection logic technology. The most recent additions to this family of products are the XR-300 and the XR-500 gate array chips which are specifically intended for semi-custom IC designs involving complex digital systems. These chips contain a large number of multiple-output I^2L gates along with Schottky-bipolar input/output buffers. Table I gives a summary of the components available on each of these chips.

Figure 4 shows the basic layout architecture of the XR-300 and the XR-500 gate array chips. As indicated in the figure, each chip is made up of two sections: (a) the I^2L gate matrix; and (b) the Schottky-bipolar input/output interface. In addition, the bipolar I/O section contains two identical sets of resistor arrays, located at opposite ends of the chip, which are used for biasing the injectors of the I^2L gates. The basic features of each of the sections of the gate array chips are outlined below:

Table 1
List of Components on XR-300 and XR-500 Semi-Custom Chips

Component Type	Chip Type XR-300	XR-500
Multiple Output I^2L Gates	288	520
Input/Output Buffers	28	40
Schottky – NPN Transistors	56	80
Resistors	168	240
Bonding Pads	34	42
Chip Size (mils)	104 x 140	122 x 185

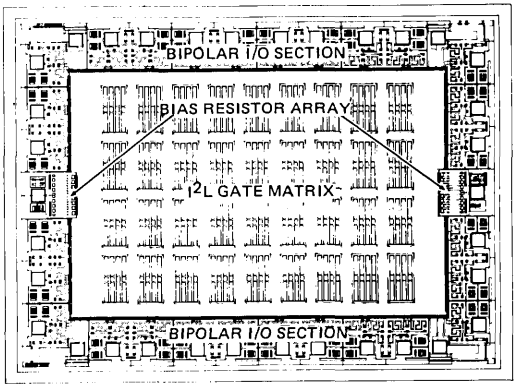


Figure 4. Basic Architecture of XR-300 and XR-500 I^2L Gate Arrays.

a) The I^2L Gate Matrix:

This section of the I^2L gate array is made up of 8-gate "cells." These cells contain eight multiple-output I^2L inverters which share a common set of four injectors. Figure 5 shows a basic 8-gate cell section within the I^2L gate section, prior to customization. The basic 8-gate cells forming the I^2L gate matrix are made up of P-type injectors and gate-*fingers* which serve as the base regions of the I^2L gates. The six dots on each gate area indicate the possible locations or sites for gate input or outputs. The particular use of these sites as an input or an output is determined by two custom masks: an N-type collector diffusion mask which defines the locations of outputs, and a custom contact mask which opens the appropriate input and output contact. Finally, a third custom mask is applied to form the metal interconnections between the gates, and the gate cells. The custom N-type diffusion step, which determines the locations of gate outputs, is also used for forming low-resistivity underpasses between the gate-cells. The area between each of the gate cells can accommodate two or three parallel underpasses in the horizontal and the vertical directions, respectively. Since the N-type diffusion which forms these underpasses is a part of the customizing step, the location and the length of each underpass can be chosen to fit a given interconnection require-

ment. This method provides the designer with virtually all the advantages and capabilities of multi-layer interconnection paths on the surface of the chip; and allows approximately 80% of the gates on the chip to be utilized in a typical random-logic layout.

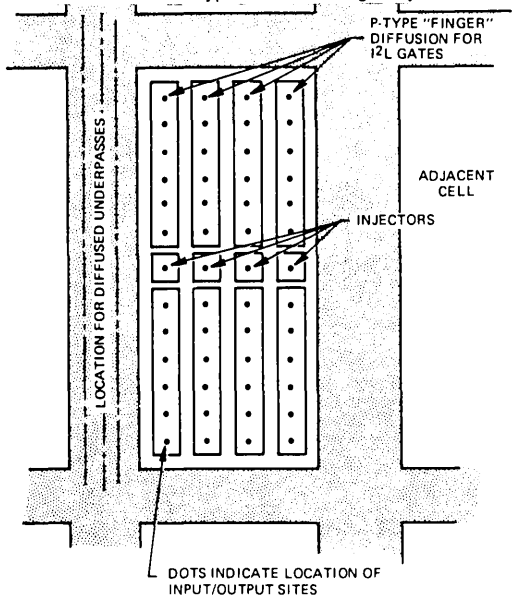


Figure 5. Basic 8-Gate Cell Before Customization.

The custom logic interconnections can be easily laid out in pencil on a layout sheet by simply interconnecting the desired gate "sites" with a pencil line and appropriately defining the function of the site as an input, output, injector contact or an underpass. Figure 6 shows a typical example of such a logic layout. The corresponding symbols defining the function of the sites on the layout are also identified in the figure. For convenience, an underpass is indicated with a resistor symbol, connecting two triangles corresponding to the terminal points of the underpass.

Figure 7 shows the sample layout of the same 8-gate cell, after its customization with a selective N-type collector diffusion, contact-window cut and the metal interconnection patterns.

Typical electrical characteristics of the I^2L gates within the gate matrix are listed in Table 2. Typical operating characteristics of the gates are given in Figures 8, 9 and 10, as a function of the injector current per gate. As indicated in Figure 8, the average power-delay product for a four-output gate is approximately 0.5 pJ at low currents; and the typical propagation delay, t_{pd}, at injector currents in excess of 100μA/gate is approximately 50 nsec for the output furthest from the injector. Figure 9 shows the two components of the total propagation delay, namely the turn-on and turn-off delay, as a functon of the injector bias. At low injector currents (i.e., $I_I \leq 10\mu A$), turn-on delay is the dominant factor. For high-speed

Table 2
Typical Characteristics of I^2L Gates

Parameter	Typical Characteristics at Various Injector Currents			
	I_I=100 nA	I_I=1 μA	I_I=10 μA	I_I=100 μA
Output Sink Current, I_O	300 nA	8 μA	80 μA	600 μA
Output Sat. Voltage, V_{OL}	3 mV	3 mV	4 mV	10 mV
Input Threshold	0.48 mV	0.54 mV	0.60 mV	0.66 mV
Pwr.-Delay Product (V^+ = 1V)	0.6 pJ	0.6 pJ	1.0 pJ	3 pJ
Average Prop Delay	6 μsec	0.6 μsec	200 nsec	50 nsec
Max. Toggle Freq (D F/F)	6 kHz	60 kHz	400 kHz	3 MHz
Input OFF Current (V_{IN}=0)	150 nA	1.5 μA	15 μA	130 μA
Output Breakdown Voltage	3V	3V	3V	3V

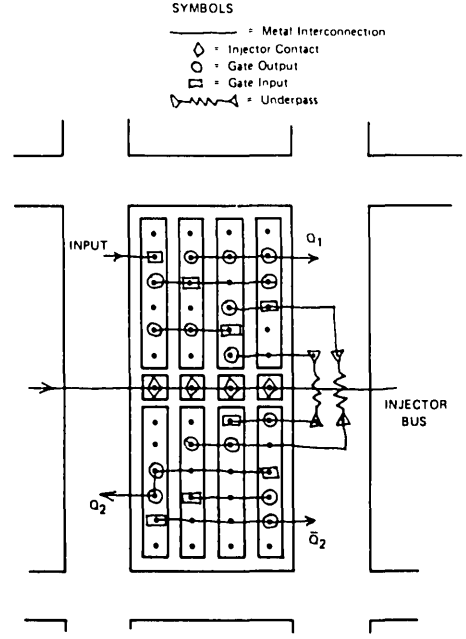


Figure 6. Sample Pencil Layout on a Logic Cell.

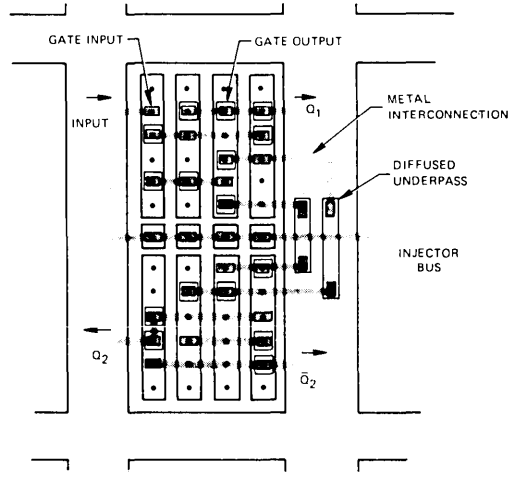


Figure 7. Sample Layout of 8-Gate Cell After Customizing it with N+ Collector Diffusion, Contact Mask and Metal Interconnection Pattern.

operation with $I_j \leq 50\ \mu A$, turn-off delay becomes the dominant limitation in speed. Typical toggle rate of a D-type flip-flop as a function of injector current is shown in Figure 10. As indicated in the figure, toggle rates of 3 MHz are obtained at injector current levels of approximately 100 μA per gate.

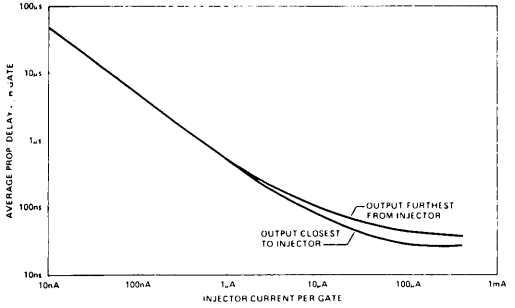


Figure 8. Propagation Delay Characteristics of 1_2L Gates as a Function of Injector Current.

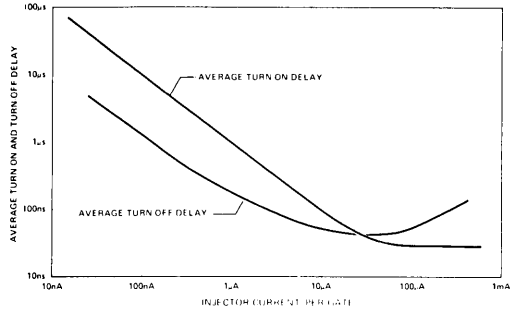


Figure 9. Average Turn-On and Turn-Off Delay vs. Injector Current.

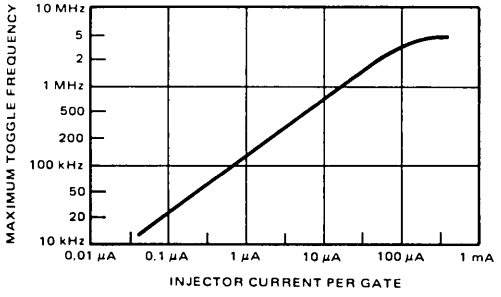


Figure 10. Maximum Toggle Rate of D-Type Flip-Flop as a Function of Injector Current.

b) Schottky-Bipolar I/O Section:

The Schottky-bipolar input/output interface sections are located along the periphery of the XR-300 and the XR-500 gate array chips. In addition, this bipolar section of the chip contains two sets of resistor arrays located at opposite ends of the chip (see Figure 4) for programming or setting the injector current levels for the I^2L gates. By proper tapping of these resistor arrays, the injector currents of the gates can be set to any value between 1 μA to 100 μA per gate.

For operating with current levels below 1 μA/gate, an external current setting resistor can also be used.

The component layout of a typical bipolar input/output interface cell is shown in Figure 11. Such an I/O interface cell contains one bonding-pad, several diffused resistors of varying values, two Schottky-clamped NPN transistors and a clamp diode to the substrate. Each of the NPN bipolar transistors are capable of sinking 10mA of output current, with typically a saturation voltage of 0.5V. The breakdown voltage of the bipolar output transistors is 6V; however, modified versions of the XR-300 and XR-500 I^2L gate arrays are also available with output breakdown voltage in excess of 15V. Figure 12 shows some of the most commonly used input and output

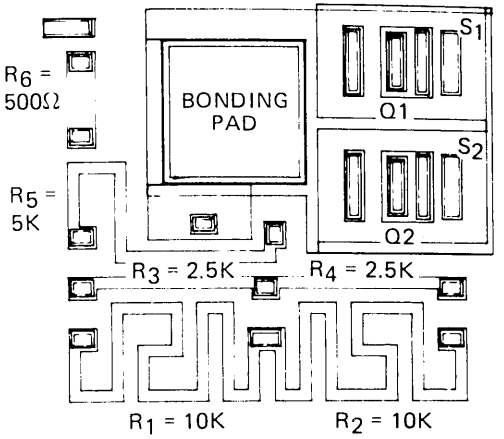


Figure 11. A Typical Schottky-Bipolar Input/Output Interface Cell.

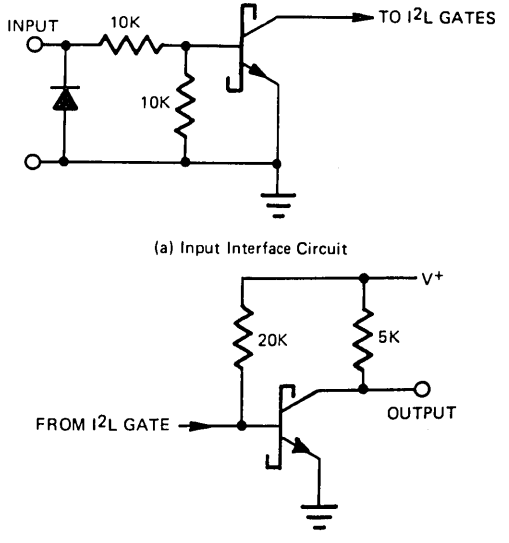


Figure 12. Tyipcal Bipolar I/O Interface Circuits.

11

interface circuit configurations available from the basic bipolar I/O cell.

SEMI-CUSTOM DESIGN CYCLE

The semi-custom LSI design program utilizing the XR-300 and XR-500, is devised for maximum versatility, to suit varying customer needs or capabilities. Figure 13 gives an outline of the six basic steps associated with a typical I^2L semi-custom program. The sequence of these steps are also outlined below:

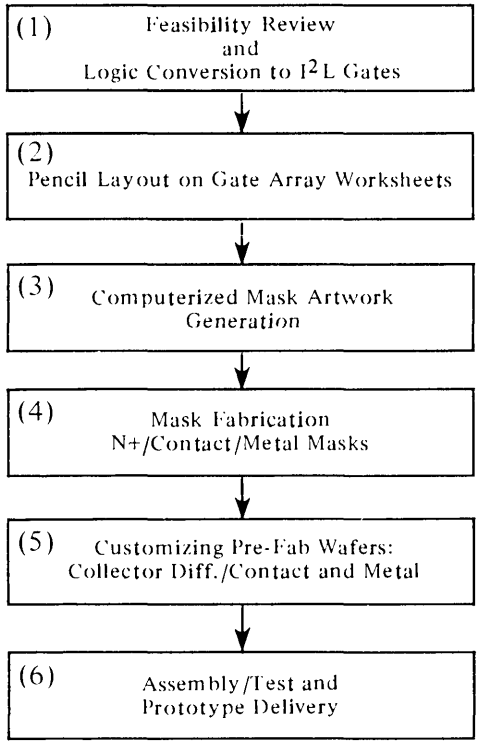


Figure 13. Sequence of Steps Associated with a Semi-Custom LSI Development Cycle.

Step 1. Feasibility Review and Logic Conversion:

Starting with the customer's logic diagram (preferably reduced to flip-flops and gates) the first step is a detailed review of the system requirements with regards to the overall gate count, I/O requirements, operating speeds, etc., to assure feasibility of integration, and to choose the most economical gate array chip to be used. If the results of this review indicate feasibility, the next step is to convert the logic diagram into I^2L gates. At this state, a computer simulation of the logic diagram may also be performed, if deemed necessary.

Step 2. Pencil Layout on Gate Array Worksheets:

Once the logic diagram is converted to I^2L gates, the next step will be to make a pencil layout of the circuit on the appropriate array worksheet. This pencil layout is done on a blank worksheet where the gate input and output locations are shown as target dots (see Figure 5). During the layout, an appropriate symbol is placed over the corresponding dot on the gate outline, and the interconnections and the underpasses between the gates are indicated by pencil lines and with the symbols defined in the layout example of Figure 6. In this layout, the bipolar I/O cells do not need to be internally interconnected. Since these cells are standardized, it is only necessary for the designer to specify if a particular I/O cell is to be used as an input or an output.

Step 3. Computerized Mask Artwork Generation:

Using a specially developed computerized mask generation technique, the three layers of necessary custom IC tooling (i.e., for custom N-type diffusion, contact window cut; and the metal interconnections) can be automatically generated by a single "digitizing" step from the pencil layout. This simultaneous and automated generation of the three custom mask layers greatly reduces the tooling cost and turnaround time, and avoids mask errors.

Step 4. Mask fabrication:

The photographic tooling plates, or "masks," are fabricated by a pattern-generation technique from the digitized coordinate information stored in the computer.

Step 5. Customizing Prefabricated Wafers:

The prefabricated I^2L wafers containing the P-type base diffusion and the gate "fingers" (see Figure 5) are customized into completed monolithic LSI chips using the custom IC tooling generated in Steps 3 and 4.

Step 6. Assembly/Test and Prototype Delivery:

The completed monolithic chips are first evaluated on the finished IC wafer, and later assembled, electrically tested and delivered as the completed prototypes.

In many cases, the first two steps indicated in the flow chart of Figure 13, can be done by the customer, in consultation with Exar, using Exar's I^2L Design Kit and the design instruction manual. Whenever possible, such an approach is recommended, since it greatly reduces the development costs and the turnaround time.

Typical development cycle containing all the steps outlined in the flow chart of Figure 13, takes about 8 to 12 weeks, depending on the circuit complexity, and whether the customer or Exar does the logic conversion and pencil layout.

Figure 14 shows the photo-micrograph of a typical semicustom LSI chip, fabricated using the technology outlined in this paper. As indicated in the figure, the use of 3-mask customization step results in an efficient layout and utilization of the available active devices within the I^2L gate array.

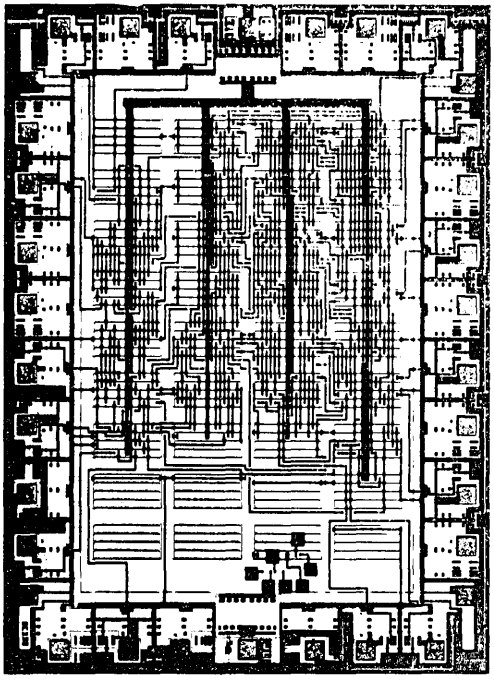


Figure 14. Photo-Micrograph of a Typical Semi-Custom I^2L LSI Chip.

ECONOMICS OF SEMI-CUSTOM DESIGN

In developing custom LSI circuits, one is confronted by the following key question: for a given production requirement, is it cheaper to develop a full or semi-custom IC? Since the performance and functional requirements of custom IC's vary greatly, there is no general answer to the above question. However, based on the overall production requirements it is possible to establish some economic guidelines for deciding which custom IC technology to use, and when.

One of the main advantages of semi-custom LSI design over conventional full custom IC development is the greatly reduced development cost. This development cost generally amounts to 10% to 30% of that required for a complete custom IC design. However, since the semi-custom design technique tends to waste some of the IC chip area due to random interconnections, the unit price of a semi-custom LSI chip in volume production is slightly higher (approximately 10% to 30%) then a full or complete custom design. Therefore, to decide which is the most economical approach, it is best to compare the estimated amortized unit cost per device for various production quantities. Figure 15 gives such a comparison for a "typical" custom LSI chip, as a function of total production requirement. The total amortized cost per unit is defined as the total cost of the development plus the production purchase, divided by the total number or quantity of units purchased. The extremely high development costs (typically in the range of $50,000 to $100,000) associated with full custom designs make the amortized unit cost of full custom IC's far more expensive than semi-custom designs, at low production quantities. Similarly, for the lower chip cost of full custom IC's make this approach more economical for high production volumes. Typical cross-over point between the economics of the full or semi-custom technology comes about in the quantity range of 50,000 pieces to 150,000 pieces, as implied by the illustration of Figure 15. However, it should be noted that Figure 15 is only a typical "case study," and that the actual cross-over point for a given program will depend on the circuit complexity, performance and test requirements, and the type of IC package used.

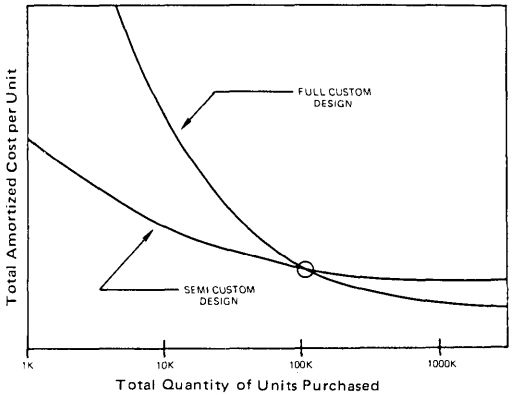


Figure 15. A Comparison of Relative Cost Advantages of Semi-Custom and Full Custom LSI Products. (NOTE: Amortized cost per unit includes the development cost.)

CONVERTING SEMI-CUSTOM TO FULL CUSTOM

It is often possible to start a development program using the semi-custom technology, such as the I^2L gate arrays described in this paper, and later change to a full custom design when the production quantities increase beyond the cost cross-over point illustrated in Figure 15. Such two-phase approach often combines the best advantages of each of the semi- and full custom technologies. For example, the initial development can be done in a semi-custom manner, using Exar's I^2L gate arrays, and thus take full advantage of the low tooling cost and the short development cycle. As a customer's product matures and its market expands, resulting in higher volume production run rates, Exar can convert the multiple semi-custom chip approach into a single custom IC, achieving a cost reduction and in many cases a performance improvement. The significant advantage of this type of program is that the risk associated with a custom development is greatly reduced; the IC design approach has been proven, and the design "bugs" are removed at the semi-custom stage thus eliminating the need for lengthy re-design cycles at the full custom level. Once the semi-custom chip is completely characterized in the user's system, and is used for the initial production runs, it can be gradually "phased-out" by a full custom design without interrupting the user's production line.

XR-C409 Monolithic I²L Test Circuit

INTRODUCTION

The XR-C409 monolithic IC is a test circuit for evaluation of speed and performance capabilities of Exar's Integrated Injection Logic (I^2L) technology. It is intended to familiarize the I^2L user and the digital system designer with some of the performance features of I^2L, such as its high-frequency capability and power-speed tradeoffs.

Figure 1 shows the package diagram of the XR-C409 I^2L test circuit. It is comprised of five separate evaluation blocks as shown in the figure. Blocks 1 and 2 are D-type flip-flops which are internally connected as frequency dividers. Each of these dividers provide buffered open-collector outputs. Blocks 3, 4, and 5 are 8-stage ring-oscillators with buffered outputs to be used for measuring gate propagation delays at different injector current levels.

FREQUENCY DIVIDER SECTION

The frequency divider sections of XR-C409 test circuits are made up of two D-type flip-flops internally connected in the (÷2) mode. These frequency dividers are operated with *serial* clocking and *parallel* reset controls.

The internal interconnections of these D-type flip-flop sections are shown in Figure 2. The corresponding package terminals are also identified in the figure. The flip-flops operate on the negative-transitions of the clock input, and reset with the reset at a "high" logic state. When the circuit is reset, all the outputs go to a "low" state. The logic polarities and the timing sequence of the circuit waveforms are given in Figure 3.

Evaluating the Frequency Divider Section

Figure 4 shows the circuit connection for the frequency divider section of the XR-C409. The recommended clock input level is 0V and +1V for the "low" and "high" levels. For optimizing high frequency performance, a square wave clock input is recommended with a source impedance $\leq 100\Omega$.

Biasing of Injectors

All of the 16 I^2L gates forming the frequency divider sections are biased by the total injector current, I_T, applied to the injector terminal (Pin 1) as shown in Figure 4. The total injector current, I_T, applied to the flip-flop sections of XR-C409 is set by the external bias resistor, R_B, as:

$$I_T = \frac{V^+ - V_{be}}{R_B} \qquad (1)$$

where V_{be} ($\approx$ 0.7V) is the transistor base-emitter voltage drop.

The total injector current, I_T, is shared among 16 individual I^2L gates forming the frequency-divider sections. Thus, the operating current of each gate, I_j, is equal to 1/16 of the total injector bias, or:

$$I_j = I_T/16 \qquad (2)$$

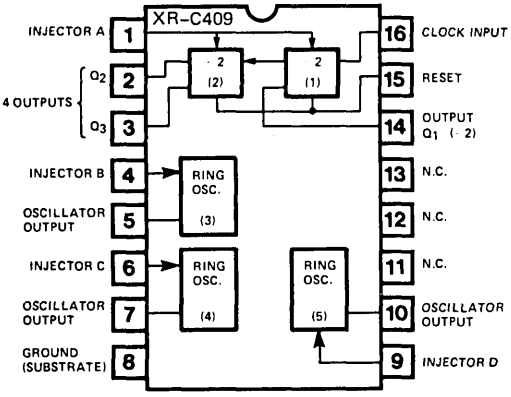


Figure 1. Package Terminals for XR-C409 Test IC.

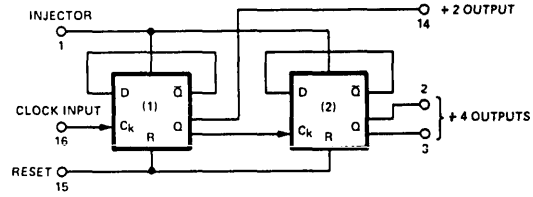


Figure 2. Block Diagram of Frequency Divider Section.

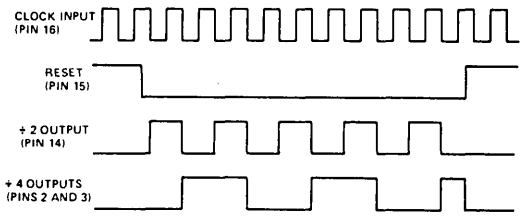


Figure 3. Timing Diagram for Frequency Divider Section.

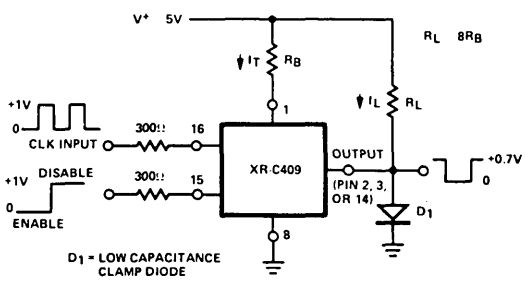


Figure 4. Test Circuit for Frequency Divider Section.

Measuring Output Waveforms

Each of the output terminals of XR-C409 frequency-divider are open-collector type terminals which require a pull-up resistor to positive supply voltage. Thus, the output rise-time is limited by the external RC time constant due to the load resistance, R_L, and the parastic and/or load capacitance, C_L.

Figure 5 shows a recommended circuit connection to test the output swing at high frequencies, using a low-capacitance clamp-diode, D_1, to clamp the output swing to $\approx +0.7V$ above ground.

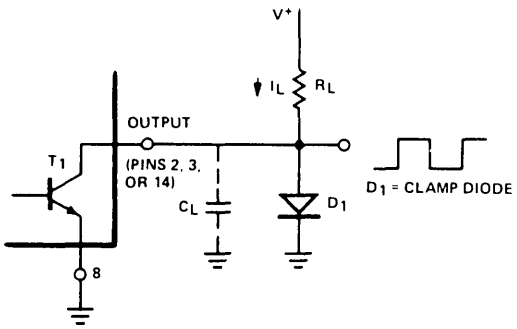


Figure 5. Recommended External Connections to Measure Output Waveforms.

The value of the load resistor, R_L, is determined by the current sinking capability of the output transistor, T_1, internal to the chip. Since T_1 is the output of an I^2L gate, its worst case sinking current is limited to the individual gate current, i.e.:

$$I_L \leq I_j = \frac{I_T}{16} \quad (3)$$

This current-sinking capability in turn limits the minimum value of load resistance R_L to:

$$R_L \geq 16\, R_B \quad (4)$$

The peak output swing is limited to approximately 3 volts due to the collector-base breakdown of the I^2L gate output, i.e., transistor T_1 of Figure 5.

High Frequency Capability

The maximum operating frequency of I^2L frequency-divider circuits is a function of the total injector current. For low-current operation, the maximum toggle-frequency of the flip-flops forming the frequency-divider section increases linearly with increasing injector current. Typical maximum toggle frequency vs. injector

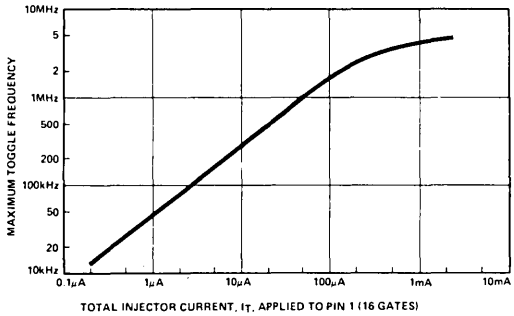


Figure 6. Typical Maximum Toggle Frequency vs. Injector Current Characteristics for XR-C409 Frequency Divider Section

(NOTE: Clock Input: 1V $_{p\text{-}p}$ Square Wave)

current characteristics are shown in Figure 6. Note that the maximum toggle-rate obtainable is in the range of 3 to 5 MHz, at a total injector current level of 1 to 2 mA, which corresponds to individual injector currents of approximately 60 μA to 120 μA per gate.

RING-OSCILLATOR SECTIONS

The ring-oscillator sections of XR-C409 test circuit are intended for measurement of propagation delays associated with I_2L gates. Each of these oscillators are made up of a cascade of 8 four-output I^2L gates. Figure 7(a) shows the basic electrical equivalent circuit of a four-output I^2L gate. Its corresponding logic symbol is shown in Figure 7(b). The basic gate operates as an inverter with single input and four outputs.

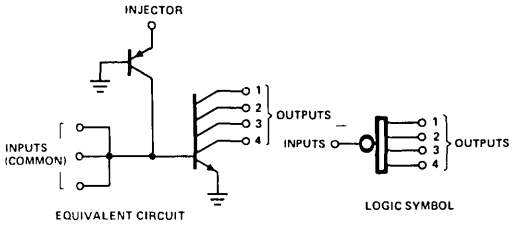


Figure 7. Four-Output I^2L Gate

The propagation delay through an I^2L gate depends on the following sets of parameters:

1. Device design: (i.e., manufacturing methods and device layout used in fabrication process).
2. Injector current level: (gate switching speed increases with increasing current, until a maximum is reached).
3. Choice of outputs used: (the output closest to the injector has minimum propagation delay at high currents).
4. Number of outputs used: (if fewer outputs are used and the unused outputs left open, the gate delay is Lower at low currents. However, at high currents, i.e., $I_j \geq 100\mu A$/gate, gates with fewer outputs left unused show lower delays. This is due to excess storage-time effects due to open-circuited gate outputs. See Figure 10.)

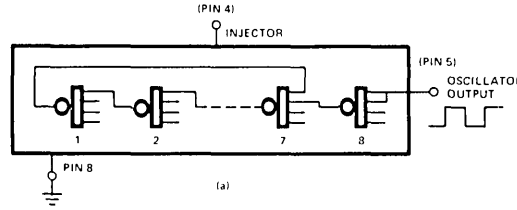
Figure 8 shows the basic seven-stage ring-oscillator circuits included on the XR-C409 chip to evaluate the propagation delay characteristics of I^2L gates. Since the delay characteristics depend on the choice and the number of gate outputs used, the test IC includes three separate ring oscillator sections. The ring oscillator of Figure 8(a) corresponds to section (3) in the package diagram of XR-C409 shown in Figure 1. This oscillator uses only one gate-output per gate. The output used is the one closest to the injector, with the remaining outputs left open-circuited.

The ring-oscillator of Figure 8(b) uses two gate outputs per stage. The outputs used are the two closest to the injector. The ring oscillator of Figure 8(c) has all four outputs shorted together.

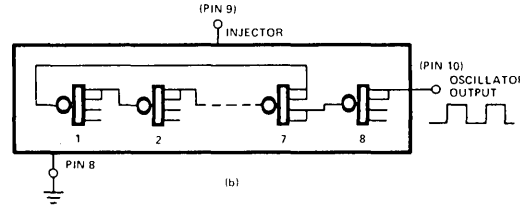
All three oscillator sections of XR-C409 have *separate* injectors, but share a common ground (pin 8). Each oscillator also has a separate output buffer stage.

Figure 9 shows a recommended test circuit for evaluating gate delay vs. gate current characteristics using the ring oscillator sections of XR-C409. Since each ring-oscillator section is comprised of 8 gates, the actual injector current per gate, I_j, is 1/8 of the total injector current, I_T:

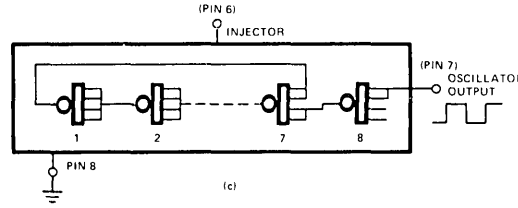
$$I_j = \text{injector current/gate} = \frac{I_T}{8} \qquad (5)$$



Ring Oscillator Using Single Gate Output per Stage (Section 3)



Ring Oscillator Using Two Gate-Outputs per Stage (Section 5)



Ring Oscillator Using Four Gate-Outputs per Stage (Section 4)

Figure 8. Equivalent Circuits of the 7-Stage Ring Oscillator Section.

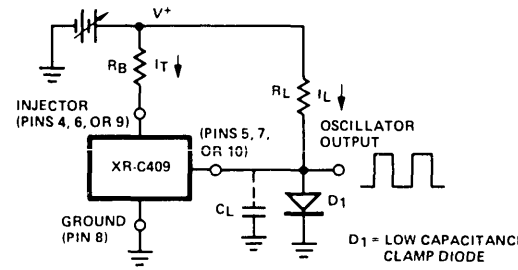


Figure 9. Recommended Test Circuit for Evaluating Power-Delay Characteristics of I^2L Gates Using Ring Oscillator Sections of XR-C409.

The total injector current, I_T, is determined by the external bias resistor, R_Bm as given by equation (1).

Measuring Output Waveforms

The output terminals of XR-C409 ring counter sections are open-collector type terminals, similar to the outputs of the frequency divider sections. Thus, the outputs require pull-up resistors to the positive supply voltage. The output rise-time is strongly affected by the external RC time constant due to the load resistance, R_L, and the parasitic load capacitance, C_L. In the test circuit of Figure 9, a low-capacitance clamp diode, D_1 is used to limit the output swing and thus minimize the slow rise-time effects.

The minimum value of load resistance, R_L, is determined by the current sinking capability of the output I^2L gate. For proper operation of the ring-oscillator circuits, the load current, I_L, should be limited to:

$$I_L \leq \frac{I_T}{4} \qquad (6)$$

which limits the output load resistance, R_L, for ring-oscillator sections to:

$$R_L \geq 4\, R_B \qquad (7)$$

Calculating Propagation Delays

The average propagation delay τ_d per gate can be calculated from the ring oscillator frequency, f_o as:

$$\tau_d = \frac{1}{2Nf_o} \text{sec} \qquad (8)$$

where N is the number of stages in the ring oscillator.

For the case of the 7-stage oscillator circuits in the XR-C409 test chip, τ_d can be calculated from equation (8) by setting N = 7.

Figure 10 shows the typical gate-delay vs. injector current characteristics measured from the three ring-oscillator sections of XR-C409. In the figure, the gate delay is plotted as a function of the injector current per gate. The gate geometry layout of XR-C409 ring-oscillator sections is not optimized for high frequency operation.

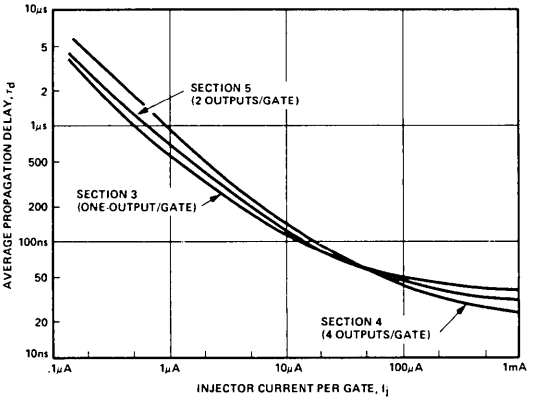


Figure 10. Typical Propagation Delay vs. Injector Current Characteristics as Measured from 7-Stage Ring Oscillator Section of XR-C409.

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Designing Wide-Tracking Phase-Locked Loop Systems

INTRODUCTION

Phase locked-loops with their excellent frequency tracking characteristics have found their way into many applications where synchronizing or synthesizing of signals is required. Although they do have the ability to track an incoming signal very well, the actual tracking range is quite limited by the nature of PLL's to less than 2:1. This range of less than 2:1 must be observed if harmonic locking, a plague to the designer, is to be avoided.

This application note describes the design of tracking PLL with a tracking range of greater than 100:1, with no harmonic locking problems. This design uses the XR-2212 Precision Phase-Locked Loop in conjunction with the XR-320 Monolithic Timer and an XR-084 Quad BiFet Operational Amplifier to form a wide range PLL with automatic tuning.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the tracking PLL. The circuit is comprised of three blocks: the PLL, the Frequency to Voltage Converter, and Precision Clamping Circuit. The blocks operate as follows. The PLL locks onto the incoming frequency and produces an output frequency identical to that of the input, but phase shifted. The center of the lock range is controlled by V_1. V_1 is derived from the F/V converter, which produces a voltage proportional to the incoming frequency. This voltage, V_1, thus provides an automatic PLL center frequency tuning signal. The swing of the phase detectors filtered voltage, V_2, controls the amount the VCO can be moved about its center frequency. The precision clamp fixes the swing on V_2 to a fixed percentage of V_1, keeping the tracking range of the PLL constant as its center frequency is varied.

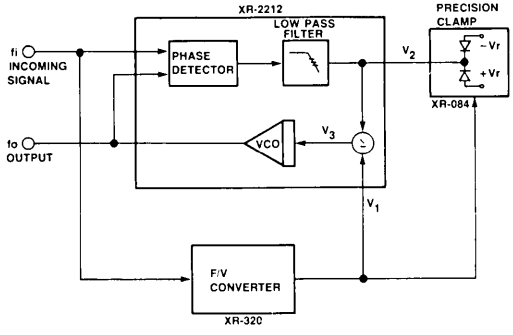


Figure 1. Tracking PLL Block Diagram.

The actual driving voltage for the VCO is now a voltage proportional to fi which can be varied a fixed percentage by the phase detector.

CIRCUIT DESIGN

The heart of the circuit is the XR-2212 Precision Phase-Locked Loop. Figure 2 shows the XR-2212's internal blocks and necessary external components. The VCO in the XR-2212 is actually a current controlled oscillator. Pin 12 is fixed at the reference voltage, $V_r \simeq \frac{V+}{2}$, and the current drawn from this terminal controls the frequency of oscillation of the VCO, f_0. With R_0 grounded, as shown, the VCO's free running or center frequency is:

$$f_0 = \frac{1}{R_0 C_0}$$

R_0 and C_0 are calculated using this relationship at f_0 maximum. With the PLL locked on its center frequency, the phase detector's dc output, Pin 10, is also at V_r and the current flowing in R_0 is proportional to f_0. If the bottom end of R_0 is now raised above ground, the current in R_0 will change linearily with the voltage, as will f_0 thus providing the voltage control input for the VCO. If R_0 is left at zero volts and fi is moved, the dc voltage at Pin 10 will inversely follow fi, increasing fi decreases the voltage at Pin 10, modulating the current from Pin 10 and thus f_0. The maximum swing of Pin 10 is $\simeq \pm Vr$, giving the following relationship:

$$\pm\frac{\Delta f}{f_0} = \frac{\frac{\pm V_r}{R_1}}{\frac{V_r}{R_0}} = \frac{R_0}{R_1} \pm \frac{(V_r R_0)}{V_r R_1} = \pm\frac{R_0}{R_1}$$

Δf being the PLL's tracking range.

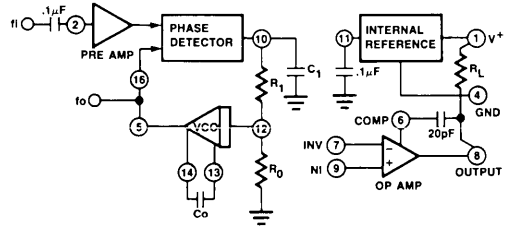


Figure 2. XR-2212 Internal Blocks with External Components.

In our application a constant $\frac{\Delta f}{f_0}$ is desired, so if the output of the phase detector, Pin 10, is clamped to $-V_{R0}$, the voltage across R_0, a constant tracking range will be maintained. C_1 serves as the loop, low pass filter, and is made to equal $\frac{C_0}{4}$ for a damping of ½.

The voltage driving R_0 comes from the F/V converter which is formed by the XR-320 Monolithic Timer. The internal blocks and external components of the XR-320 are shown in Figure 3. The input to the F/V is brought to the trigger input, Pin 6, which, when driven above the threshold, triggers the F/F and opens the internal switch transistor, S_1. The voltage on C_T will linearily rise, at a rate set by R_T until V_r is reached at which time the comparator resets the F/F and closes S_1, waiting now for the next rising edge on Pin 6. Once triggered the output, Pin 12, will go low for the timing period defined by the relationship:

$$T_{low} = 2R_TC_T$$

Since Pin 12 will now have a constant low time and a repetition rate equal to that of the incoming signal, fi, it can be filtered to provide a voltage proportional to fi.

Figure 4 shows the complete tracking PLL circuit. The precision clamp is formed by A_1-A_3 which samples the voltage across R_0 and clamps the XR-2212's phase detectors output to $\pm V_{R0}$. With the given values, the tracking range of the circuit is one kHz to 100 kHz, with the XR-2212's tracking range set at approximately ± 0.33 f_0. The input frequency voltage range is 10 mV RMS to 3 V RMS with the output producing a 10 V P-P square wave. Calibration is done by first applying 100 kHz to the input and adjusting P_1 for f_0 equal to fi in frequency but shifted in phase by approximately 90°, then with fi = 1 kHz P_2 is adjusted again for equal frequencies with 90° of phase shift.

WIDE RANGE SYNTHESIZER USING RR-2212 PLL

This same technique of automatic tuning can be used to form a wide range synthesizer as shown in the block diagram of Figure 5. Here a programmable frequency divider has been put into the loop between the VCO output and the phase detector input. Since the PLL will drive the VCO until its two inputs are at the same frequency, the VCO will be at:

$f_{VCO} = Nf_r$ where N in the binary number applied to the programmable divider ($N \geq 1$)

The F/V converter used in the previous application to drive R_0, or tune the PLL, is now replaced with a digital-to-analog converter, DAC. Its digital inputs come from the same lines which control N. The DAC's output voltage, which drives R_0, will now vary proportionally with N, or retuning the PLL with each new N. The same clamping network is used on the phase detectors output as discussed earlier.

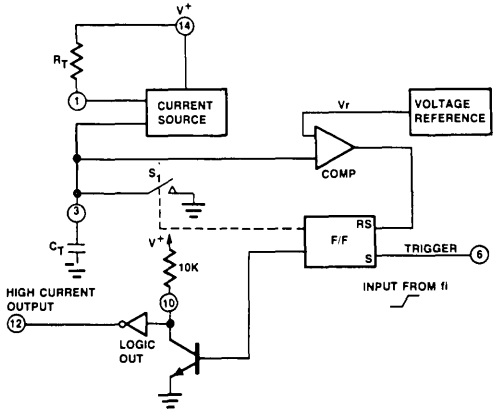


Figure 3. XR-320 Internal Blocks with External Components.

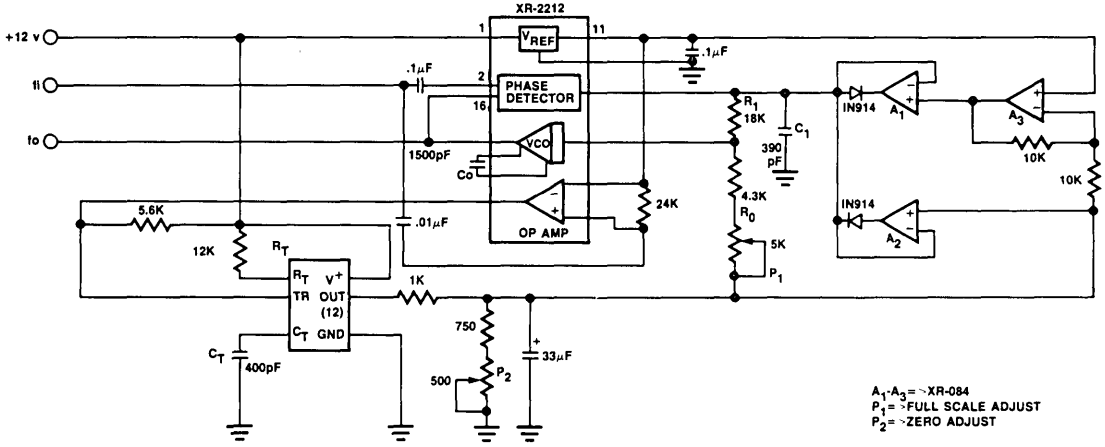


Figure 4. Wide Range Tracking PLL.

Figure 6 shows the complete wide range synthesizer circuit. The two 4-bit binary counters, 74161, and magnitude comparator, 8130, form the programmable divider. The output of the divider is a variable duty cycle pulse so that the flip-flop, 7474, was added so that phase detector was always presented with a square wave. Since the flip-flop also divides by two, the minimum value for the divider will be 2 or the actual N of the overall divider will be the binary input times two, 2N. The DAC uses the reference voltage of the XR-2212 as its reference with amplifier A_4 used to scale the voltage to R_0 correctly. C_1 provides loop compensation and its value will determine not only the response of the circuit but the short term frequency stability of f_0. A trade off must be made here as decreasing C_1 will provide for a faster responding loop but decrease the short term stability of f_0. It is probably most desirable to have a highly stable output frequency and slower responding loop, which the values in Figure 6 provide for.

With the values shown, f_0 will be one kHz to 100 kHz with f_{ref} = 500 Hz and N = 1 to 100. The reference input voltage range is 10 mV RMS to 3 V RMS with the output providing a T^2L compatible square wave.

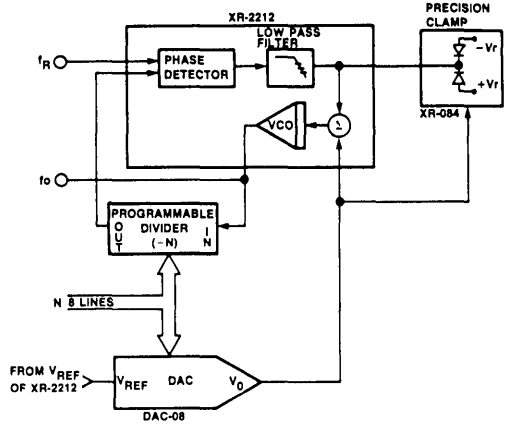


Figure 5. Wide Range Synthesizer Block Diagram.

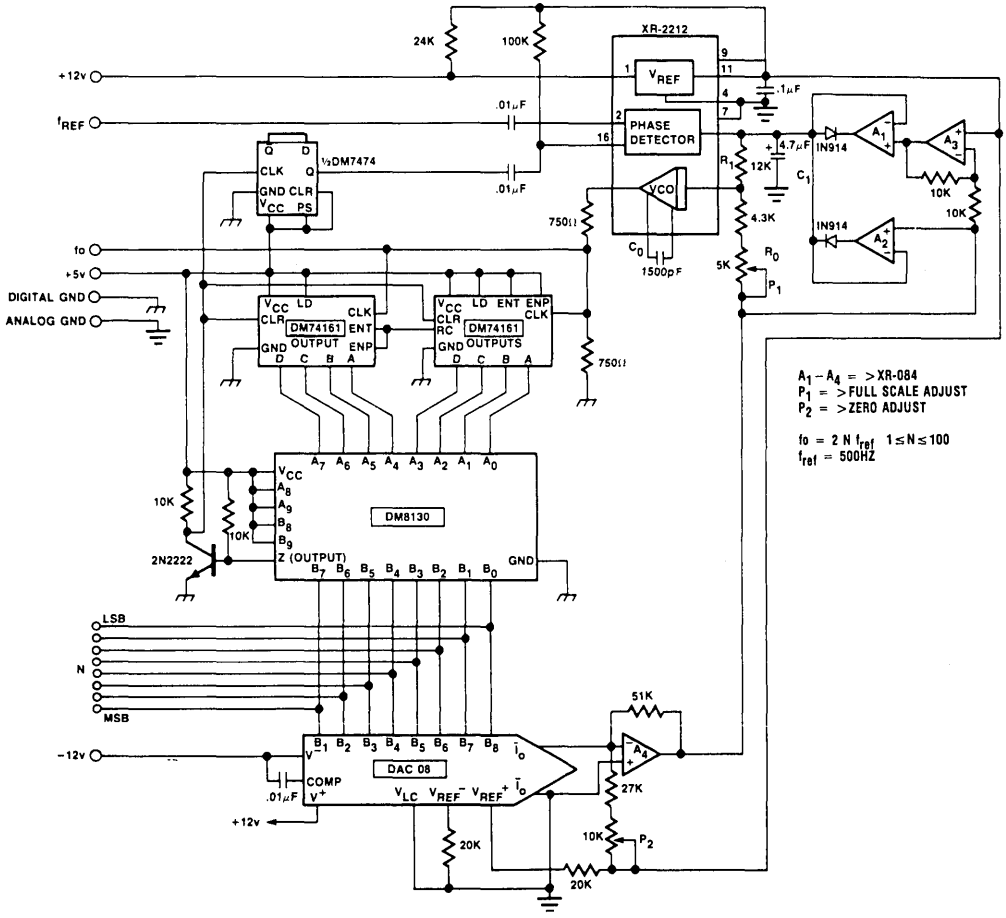


Figure 6. Wide Range Synthesizer.

Calibration is done by first adjusting P_1 for a 100 kHz output with N = 100 and then adjusting P_2 for a one kHz output with N = 1.

Typical input and output waveforms for r_{ref} = 500 Hz, top trace, and f_o, bottom trace, with N switching from 40 to 8 are shown in Figure 7.

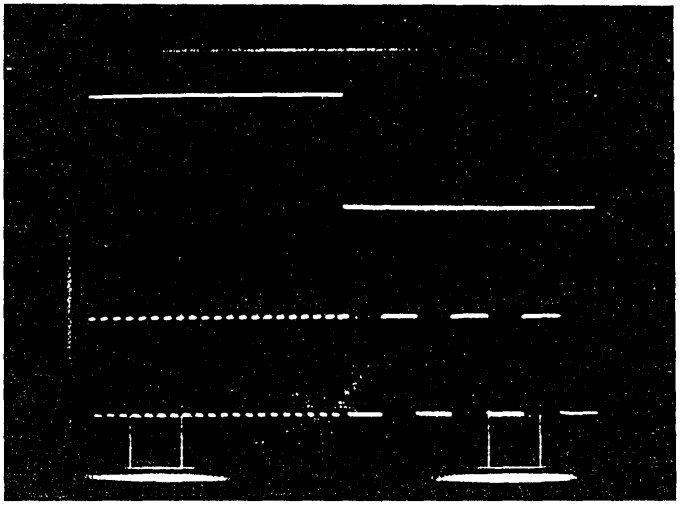


Figure 7. Typical Input and Output Waveform.

Clock Recovery System

INTRODUCTION

Recovering encoded serial data from floppy disk systems poses a major design problem as the synchronized clock used to encode data is embedded within the data stream. The clock cannot be readily extracted using common phase-locked loop techniques as the actual clock may appear for only short periods of time in a common encoding format such as NRZI. This clock is necessary to decode the serial data and retrieve the original data.

This application note describes the design of a PLL (phase-locked loop) system which can be used to recover the clock from a serial data stream using NRZI protocol with very excellent stability. The design utilizes the XR-2212 Precision Phase-Locked Loop in conjunction with the XR-320 Monolithic Timer to form the heart of the system. The system also uses a 74123 Dual One-Shot and 398/13333 for timing and sample and hold purposes.

PRINCIPLES OF OPERATION

Figure 1 shows a data stream and clock using a typical NRZI protocol. In this protocol changes in levels represents a binary zero, while no transitions a binary one. From the figure it can be seen that the data stream can have a maximum rate of change corresponding to a frequency equal to one half the clock frequency with the actual data being a string of zeros. This format guarantees that there will be no more than five ones in a row. The slowest rate of change will then be a frequency corresponding to one twelfth the clock.

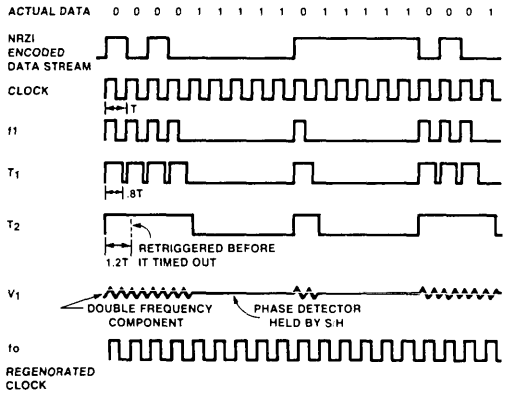


Figure 1. System Timing Diagram.

Figure 2 shows the block diagram of the clock recovery system. The XR-320 forms a bi-directional one-shot. It will produce a positive output pulse for both rising and falling edges on its input. The period of these output pulses is set equal to one half the total period of clock. This is used to provide a frequency component in the data stream equal to the clock even under worst case data conditions of five ones, zero, five ones, zero. (Seen in Figure 1.) This can also be seen to double the frequency of the data stream which is desirable as the PLL will now be able to lock to the original clock. The XR-2212 forms the PLL which, when the actual clock appears in the data stream, locks to and produces a frequency at its VCO output equal to and synchronized with the clock. The PLL's phase detector output is connected to the input of a sample and hold (S/H) as well as the S/H's output through a switch. This switch is held open by the 74123 as long as the clock appears in the data stream. Whenever a one is present the clock will not appear in the data stream and the 74123 places the sample and hold in the hold mode and closes the switch. This holds the voltage at the phase detector and keeps the proper driving voltage to the VCO, thus maintaining the frequency at the output of the VCO equal to and synchronized with the clock.

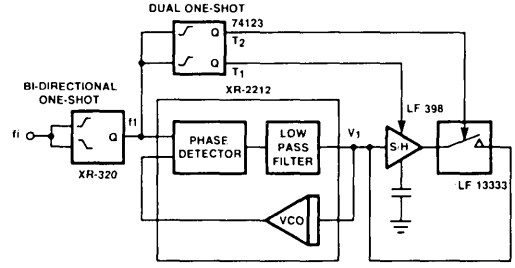


Figure 2. Clock Regenerator Block Diagram.

When the clock reappears in the data stream the 74121 drives the switch open and S/H to the sample mode with the PLL once again tracking the clock in the data stream. The length of T_1 is made equal to slightly less than the period of the clock so that the S/H is always ready in the event the clock is not in the data stream and any sample to hold glitches will not be transmitted to the phase detector's output. The length of T_2 is made slightly longer than the clock period which will cause the switch to close immediately after one clock pulse is missed. With a clock period T, these times, T_1 and T_2, are set equal to 0.8 T and 1.2 T, respectively.

CIRCUIT DESIGN

The heart of the circuit is the XR-2212 Precision Phase-Locked Loop. Figure 3 shows the XR-2212's internal blocks and necessary external components. The phase detector output is a high impedance current source output so it can be forced or held at a particular voltage easily, as by the S/H. The PLL's center frequency is equal to:

$$f_o = \frac{1}{R_0 C_0}$$

R_0 and C_0 are calculated using the data stream's clock frequency set equal to f_o. The tracking range of PLL is given by the following relationship:

$$\Delta f = f_o \frac{R_1}{R_1} \quad \Delta f \Rightarrow \text{tracking range}$$

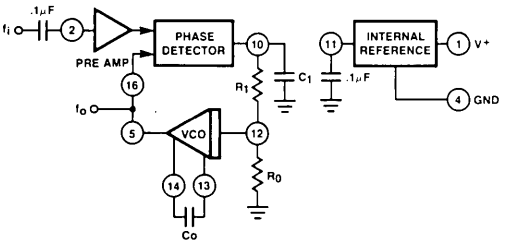


Figure 3. XR-2212 Internal Blocks with External Components.

The phase relationship between the incoming signal, f_i, and the output signal, f_o, will be 90° if f_i is equal to f_o and will vary up 90° or down 90° from this nominal if f_i is at either end of the tracking range. The voltage at the output of the phase detector will also vary linearly with these phase relationships. These relationships are shown in Figure 4. The tracking range is made very large since a constant phase relationship between the recovered clock is desirable. Therefore, any errors in the S/H or drops through the switch will not significantly alter this phase relationship. Δf is made equal to approximately 0.8 f_o, and R_1 is calculated accordingly. C_1 is used to remove the double frequency component from the phase detectors output and also in conjunction with C_0 controls the PLL transient response characteristics, according to the following relationship:

$$\xi = \tfrac{1}{4}\sqrt{\frac{C_0}{C_1}}$$

for a loop damping of ½, $C_1 = \frac{C_0}{4}$

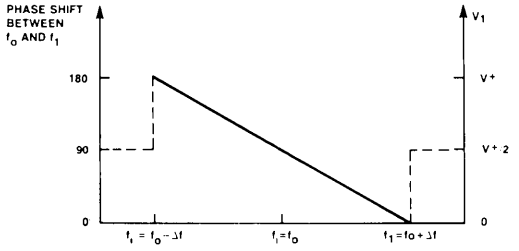


Figure 4. PLL In/Out Phase Relationships.

The XR-320 Monolithic Timer used for the bi-directional one-shot is shown in block form with its external components in Figure 5. The control flip-flop can be triggered by either positive or negative edges on its inputs, which are tied together for this application to provide bi-directional triggering. Once triggered, the output will provide a low level signal for a period defined by:

$$T_{LOW} = 2\,R_T C_T$$

These components are calculated with T_{LOW} set equal to one half the clock period.

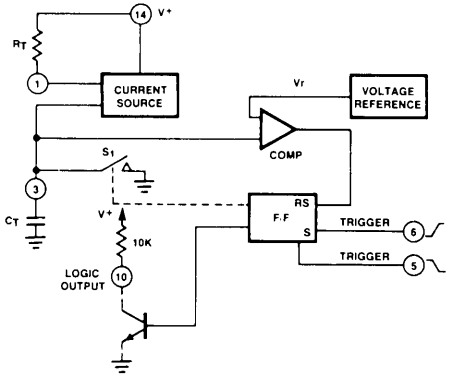
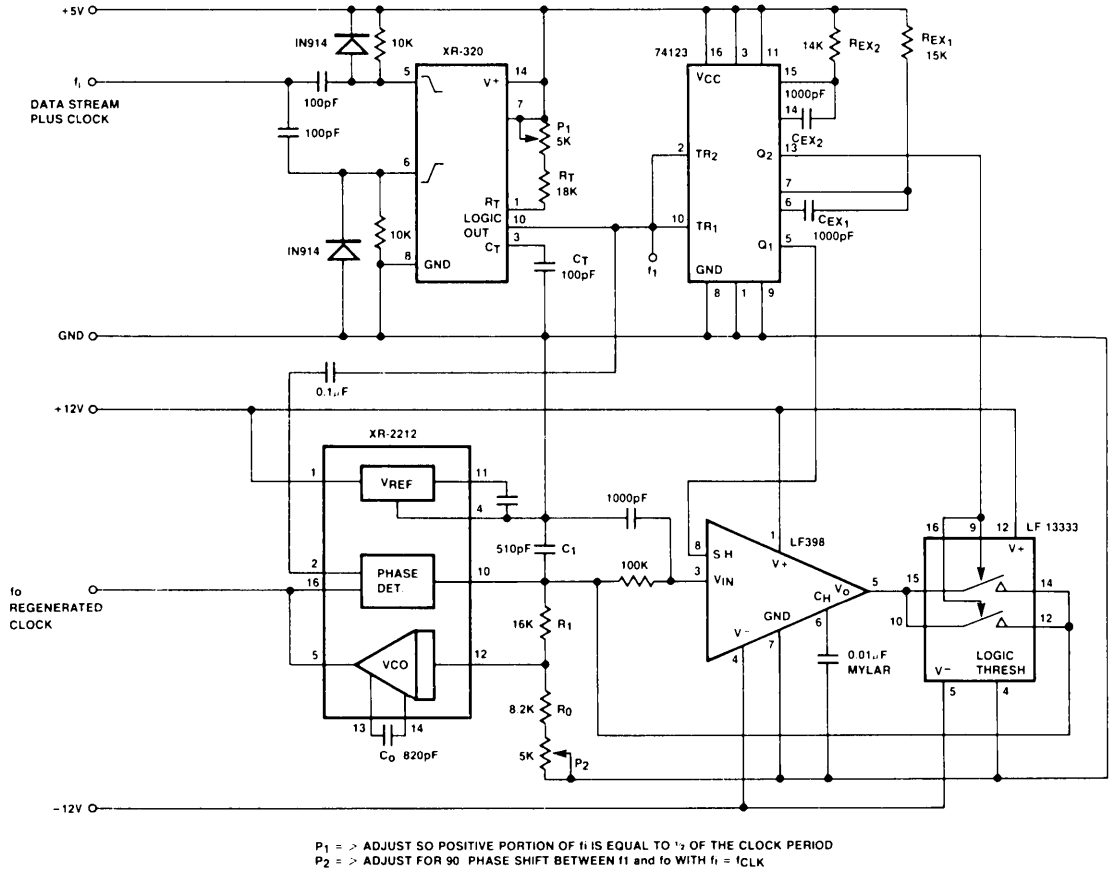


Figure 5. XR-320 Internal Blocks with External Components.

Table 1 summarizes the previously described formulas as well as those for the 74121 Dual One-Shot.

Table 1

FOR XR-2212	FOR XR-320	FOR 74123
(1) $R_0C_0 = \frac{1}{f_{CLK}}$	(4) $R_TC_T = \frac{1}{2\,f_{CLK}}$	(5) $R_{EX_1}C_{EX_1} = \frac{1}{0.8\,f_{CLK}\ln 2}$
(2) $R_1 = 1.2\,R_0$		(6) $R_{EX_2}C_{EX_2} = \frac{1}{1.2\,f_{CLK}\ln 2}$
(3) $C_1 = \frac{C_0}{4}$		



P1 = > ADJUST SO POSITIVE PORTION OF fi IS EQUAL TO ½ OF THE CLOCK PERIOD
P2 = > ADJUST FOR 90° PHASE SHIFT BETWEEN fi and fo WITH fi = fCLK

Figure 6. Complete Clock Regenerator.

Figure 6 shows the complete clock recovery circuit with values designed for a clock of 122 kHZ. The input to the system will accept input low levels from 0 V to 0.5 V levels and high levels from 1.5 V to 5 V. The output provides a 10 V P-P square-wave. Calibration is accomplished by adjusting P_1 for the output of the XR-320 to equal exactly one half of the clock period and P_2 for a 90° phase shift between f_i and f_o with a constant string of zeros applied at f_i.

The oscilloscope photograph in Figure 7 shows the system waveforms with the input data stream on top and f_o on the bottom.

The same circuit can be used to regenerate or clean up a clock with occasional missing cycles by applying it to the point labeled f_i and eliminating the XR-320 from the circuit.

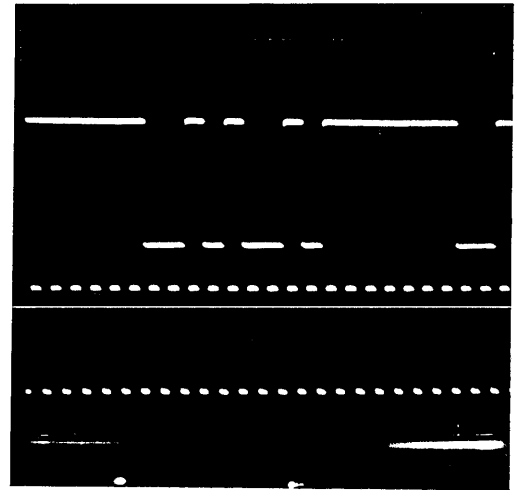


Figure 7. System Waveforms.

Building a Complete FSK Modem Using XR-2211 and XR-2206

INTRODUCTION

With the number of digital systems and equipment growing so rapidly, the need for a method of moving data has also become a fast growing field. This application note describes the construction of a modem system using frequency shift keying, FSK, for serial data transmission. The system utilizes the XR-2206 as a modulator, the XR-2211 as a demodulator, and an XR-084 op amp as a bandpass filter. These three IC's make up a complete working 300 baud, full duplex, FSK modem.

GENERAL DESCRIPTION

Figure 1 shows the block diagram of an FSK system. The complete system is comprised of an answer and originate modem. The answer modem will convert input data to either 1070 Hz or 1270 Hz and send it to the phone line, while it will decode to "1's" and "0's" 2025 Hz and 2225 Hz received from the line. The originate modem simply reverses the frequencies for send and receive. The sinewave modulator will produce two discrete frequencies at its output corresponding to a "1" or a "0" at its data input. The line hybrid will steer these frequencies to the phone line while causing received frequencies to go to the bandpass filter and demodulator. This block will therefore provide isolation between modulator and demodulator at each end. The bandpass filter is used to remove unwanted signals and noise received from the phone line before they reach the demodulator.

The PLL demodulator will lock onto incoming frequencies at its input and produce "1's" or "0's" at its output. The carrier detect output will produce a low, "0" signal out when valid data is being received.

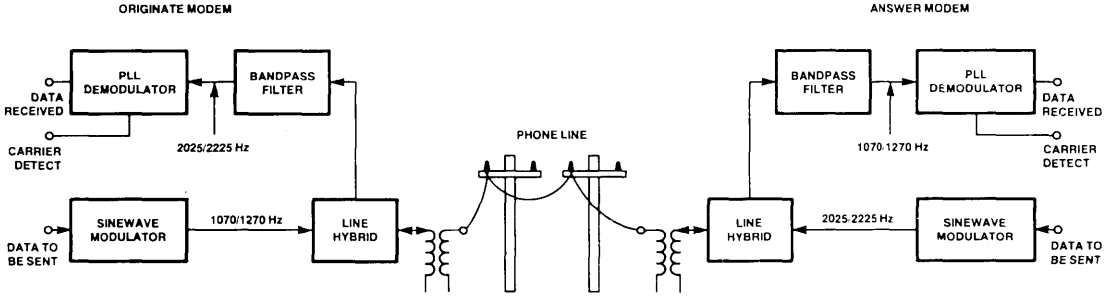


Figure 1. Block Diagram of FSK Modem System.

OPERATION AND CALIBRATION

The circuit has been designed for +12 volt operation. The data inputs accept TTL compatible signal levels, while the outputs provide 0V to +12V signal levels.

Calibration is done by first adjusting the modulator. With a low signal on its input, R_{21} is adjusted for 1270 Hz or 2225 Hz for originate and answer respectively. Then with a high signal in, R_{22} is adjusted for 1070 Hz or 2025.

The demodulator is easiest adjusted by feeding into the modem input an alternating 1070 Hz/1270 Hz or 2025 Hz/2225 Hz signal in a square-wave fashion. The modulating frequency should be 150 Hz, which is one-half the system baud rate of 300. The baud rate refers to the number of bits per second which can be sent and received. The answer can be used to drive the originate and vice-versa. R_{19} is then adjusted for a square-wave on the data received output.

R_{20} is used to set the modulator output level. With the modulator output set at −6 dBm, the system will operate with an input signal range of +10 dBm to −48 dBm.

CIRCUIT CONSTRUCTION

Figures 2 and 3 show the circuit schematic and component layout. One PC board is used for answer or originate and should use the appropriate components as listed in Table 1.

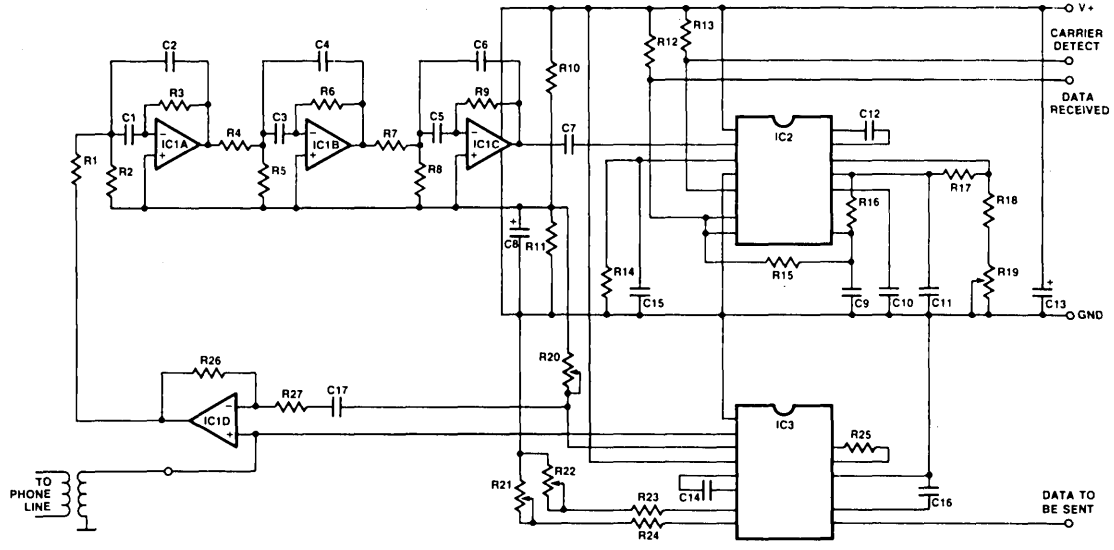


Figure 2. Complete FSK Modem Using XR-2211 and XR-2206.

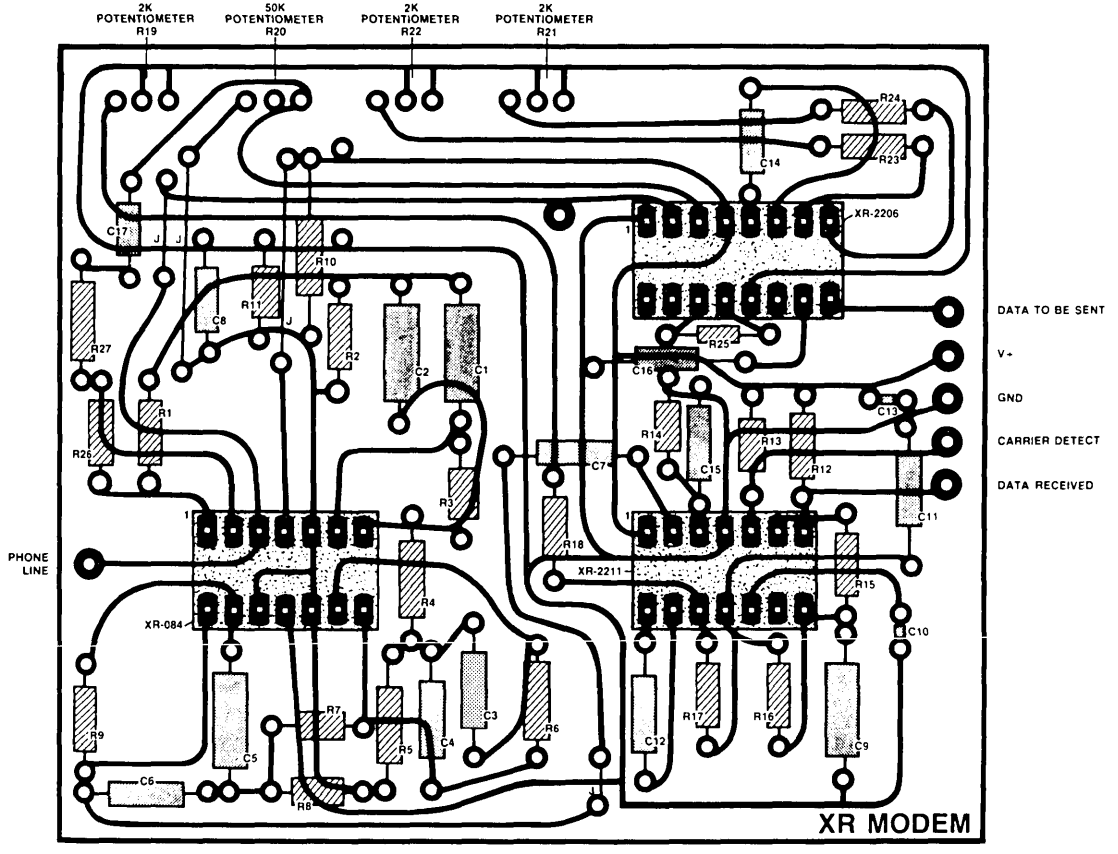


Figure 3. XR Modem Foil Side Shown (Not to Scale).

Table 1. Modem Parts List

IC1A-D	XR-084	
IC2	XR-2211	
IC3	XR-2206	
	ANSWER	**ORIGINATE**
R_1*	40.2K	47.5K
R_2*	499	191
R_3*	270K	357K
R_4*	60.4K	39.4K
R_5*	680	160
R_6*	383K	270K
R_7*	24.9K	20K
R_8*	1.21K	360
R_9*	160K	160K
R_{10}	1K	1K
R_{11}	1K	1K
R_{12}	5.1K	5.1K
R_{13}	5.1K	5.1K
R_{14}	510K	510K
R_{15}	510K	510K
R_{16}	100K	100K
R_{17}	47K	100K
R_{18}	7.5K	9.1K
R_{19}	2K	2K
R_{20}	50K	50K
R_{21}	2K	2K
R_{22}	2K	2K
R_{23}	3.9K	8.2K
R_{24}	3.6K	6.8K
R_{25}	200	200
R_{26}	1M	1M
R_{27}	1M	1M
C_1-C_6*	0.01	0.01
C_7	0.1	0.1
C_8	22	22
C_9	0.01	0.01
C_{10}	0.1	0.1
C_{11}	0.022	0.01
C_{12}	0.1	0.047
C_{13}	1	1
C_{14}	0.1	0.1
C_{15}	0.1	0.1
C_{16}	1	1
C_{17}	1	1

All resistors are 1/4 watt −5% tolerance, except as marked with (*) which are 1% tolerance. Values given in (Ω).

All capacitors are 5% tolerance, except as marked with (*) which are 1% tolerance. Values given in μF.

Precision Narrow-Band Tone Detector

INTRODUCTION

The Phase-Locked Loop (PLL) is a very versatile building block with a wide range of applications in signal processing and communication systems. As a tone detector or tone discriminator, the PLL is accurate and stable enough for most applications not requiring very narrow bandwidths. The smallest, practical detection band is limited by the temperature stability of the PLL center frequency and accuracies of external components. For example, designing a tone detector using a single PLL to discriminate a 10 Hz tone out of 100 kHz can present great difficulty. A PLL with center frequency of 100 kHz can drift by 2 Hz/°C given a typical center frequency drift of 20 ppm/°C. A slight change in ambient temperature can cause the PLL to unlock. On the other hand, there are various applications involving pressure transducers and crystal oscillators that require a very stable system capable of detecting a small change in frequency over a wide frequency spectrum.

This application note describes the use of the XR-2213 PLL in conjunction with the XR-2208 analog multiplier as a frequency mixer. It is capable of detecting a 1 Hz tone out of a frequency spectrum greater than 1 MHz. It can accept almost any periodic waveform including sine, square, and triangular waves. Error due to temperature drift is typically 0.2 %/°C. The tone detector output changes to a high state when the input is within the detection band.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the narrow-band tone detector using the XR-2208 and XR-2213. The XR-2208 is being operated as a balanced modulator or frequency mixer. It "mixes" the input frequency, f_{IN}, with a stable frequency source, f_C, to produce the sum and difference frequencies of f_{IN} and f_C. The low pass filter removes the higher frequency component ($f_{IN} + f_C$) and passes the difference frequency to the XR-2213 PLL. The input signal is "mixed-down" in frequency in this manner, allowing the PLL center frequency, f_o, to be set at a much lower frequency than the input signal. With a lower f_o, the PLL drift (Hz/°C) becomes less, making the tone detector less susceptible to ambient temperature changes.

The input signal to the XR-2208 is a periodic waveform with frequency of:

$$f_{IN} \pm \Delta f_{IN}$$

where Δf_{IN} is the detection range. The range of frequencies for detection is between $f_{IN} - \Delta f_{IN}$ and $f_{IN} + \Delta f_{IN}$. It is necessary to band-limit the input frequency for proper operation of the tone detector. Since the XR-2208 takes the "absolute" difference in frequency between f_{IN} and f_C, it is possible to obtain the same output frequency with different values for f_{IN}, causing the tone detector to lock onto the "wrong" frequencies.

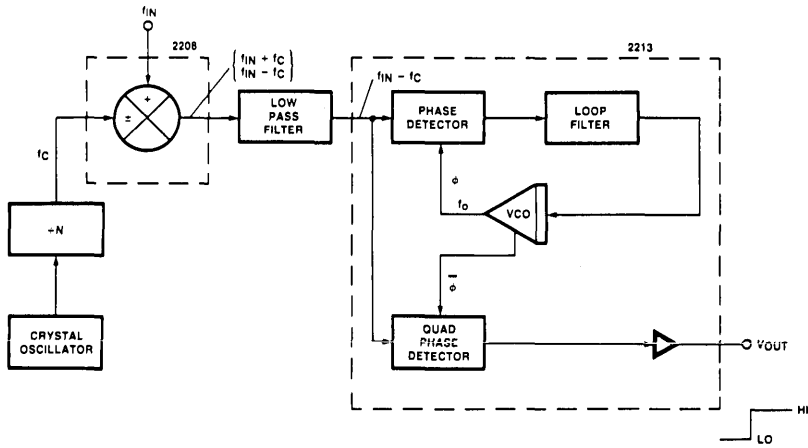


Figure 1. Functional Diagram of Narrow Band Tone Decoder.

In order to band-limit the input frequencies, a low pass filter with very sharp roll-off (6th order or higher) with the corner frequency around f_{IN} can be used. For high frequency applications (f_{IN} > 100 kHz), a bandpass crystal filter can be used. Crystal filters have stable frequency characteristics and very high Q's (Q > 1000) making very sharp bandpass filters. Crystal filters are commercially available through various manufacturers.

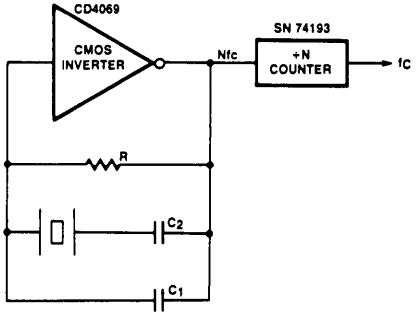
The control frequency, f_C, must come from a very stable and accurate source since any error in f_C will directly affect the tone decoder. A crystal oscillator with a "divide-by-N" counter as shown in Figure 2 can generate a very stable frequency, with temperature stability in the range of 1 ppm/°C.

The control frequency is given by:

$$f_C = f_{IN} + f_o$$

where f_o is the PLL center frequency in Hz. the Choice of f_o is arbitrary, however the larger f_o is, the more the PLL becomes susceptible to temperature variations but the better the acquisition time or "pull-in" time becomes. One the other hand, if f_o is small, then temperature variation has less effect but acquisition time becomes worse. Table 1 shows the relative performances of the tone decoder with respect to the ratio of $\Delta f_{IN}/f_o$.

The output of the low pass filter is fed into the pre-amp of the XR-2213 PLL. When this frequency falls within the detection band or the PLL ($f_o \pm \Delta f_C$), the voltage comparator goes to a high state and remains there until the input frequency falls outside the detection band; the output voltage then goes to a low state. when there is no input signal applied to the XR-2208, the PLL output remains low.



R = 5 MΩ ~ 10 MΩ

C_2 = 20 pF

C_1 = 1 pG ~ 30 pF

C_1 Pulls the crystal down (lower frequency)

C_2 Pulls the crystal up (higher frequency)

Figure 2. Crystal Oscillator.

Table 1. Tone Decoder Performance vs. $\Delta f_{IN}/f_o$

$\pm\Delta f_{IN}/f_o$	TYPICAL PLL f_o STABILITY (Hz/°C)	NORMALIZED RELATIVE ACQUISITION TIME	MAXIMUM f_{IN} ALLOWED (Hz)
0.1 %	0.02 × Δf_{IN}	0.1	$f_{IN} + \Delta f_{IN}(1999)$
0.5 %	0.004 × Δf_{IN}	0.5	$f_{IN} + \Delta f_{IN}(399)$
1.0 %	0.002 × Δf_{IN}	1.0	$f_{IN} + \Delta f_{IN}(199)$
5.0 %	0.0004 × Δf_{IN}	5.0	$f_{IN} + \Delta f_{IN}(39)$
10.0 %	0.0002 × Δf_{IN}	10.0	$f_{IN} + \Delta f_{IN}(19)$
20.0 %	0.0001 × Δf_{IN}	20.0	$f_{IN} + \Delta f_{IN}(9)$

f_{IN}, Δf_{IN} f_o in Hz. f_o = PLL center frequency

$f_{IN} \pm \Delta f_{IN}$ = input frequency range

DESIGN EQUATIONS (All R's in ohms; all C's in farads)

1. The XR-2208 control frequency, f_C, is given by:

$$f_C = f_{IN} + f_o$$

2. The maximum input frequency allowed is:

$$f_{IN}(max) \leq f_{IN} + 2f_o - \Delta f_C$$

Where $\pm\Delta f_C$ is the capture range of the PLL.

3. The capture range, $\pm\Delta f_C$, is set as:

$$\pm\Delta f_C = \pm\Delta f_{IN}$$

Where $\pm\Delta f_{IN}$ is the input frequency variation.

4. The lock range, $\pm\Delta f_L$, is set equal to $\pm\Delta f_C$:

$$\frac{\Delta f_C}{f_o} \quad \frac{R_0}{R_1} \qquad \text{(Hz)}$$

5. The loop damping factor, δ, is set to 0.63:

$$\delta = \frac{1}{4}\sqrt{\frac{C_0}{C_1}}$$

6. The PLL center frequency, f_o, is given by:

$$f_o = \frac{1}{R_0 C_0} \text{ (Hz)}$$

7. Loop detect filter capacitor, C_d, is given by:

$$C_d(\mu F) \geq 16/\Delta f_C \qquad \Delta f_C \text{ in Hz}$$

R_D is set to 470 kΩ.
Increasing C_d slows down the logic output response time.

8. The low pass filter time constants, C_F and R_F:

$$R_F C_F = \frac{1}{f_o} \qquad R_F \leq 20\ k\Omega$$

Where f_o is the PLL center frequency.

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DESIGN EXAMPLE

Consider the design of a narrow-band tone detector with frequency detection range of 111.7 kHz ± 10 Hz ($f_{IN} \pm \Delta f_{IN}$).

1. Choose the PLL center frequency to be 100 Hz.

$$f_C = 111.8 \text{ kHz}$$

f_C can be produced by using a 3.58 MHz crystal (adjusted to 3.5776 MHz) and using a divide-by-32 counter in a crystal oscillator.

2. Maximum input frequency allowed is:

$$f_{IN}(max) = 111{,}890 \text{ Hz}$$

3. Capture range, $\pm\Delta f_C$ is:

$$\pm\Delta f_C = \pm 10 \text{ Hz}$$

4. PLL center frequency is 100 Hz (f_o):
Choose R_o = 10 KΩ (choice is arbitrarily set between 10 KΩ ≤ R_o ≤ 100 KΩ)

$$C_o = 1/f_o R_o = 1.0\ \mu F$$

5. $\pm\Delta f_C = \pm\Delta f_L = \pm 10$ Hz

$$R_1 = R_o f_o/\Delta f_C = 100 \text{ K}\Omega$$

6. The damping factor is set to 0.63:

$$C_1 = C_o \left(\frac{1}{4\delta}\right)^2 = 0.16\ \mu F$$

7. Loop detect filter constants:

Choose R_D = 75 KΩ to prevent harmonic locking.

$$C_d = 16/20 \text{ Hz} = 0.8\ \mu F$$

8. Low pass filter time constants, C_F and R_F:

$$R_F = 20 \text{ K}\Omega$$

$$C_F = 1/f_o R_o = 0.5\ \mu F$$

A circuit schematic for the above tone detector is shown in Figure 3.

Typical acquisition time for this circuit is less than 100 msec.

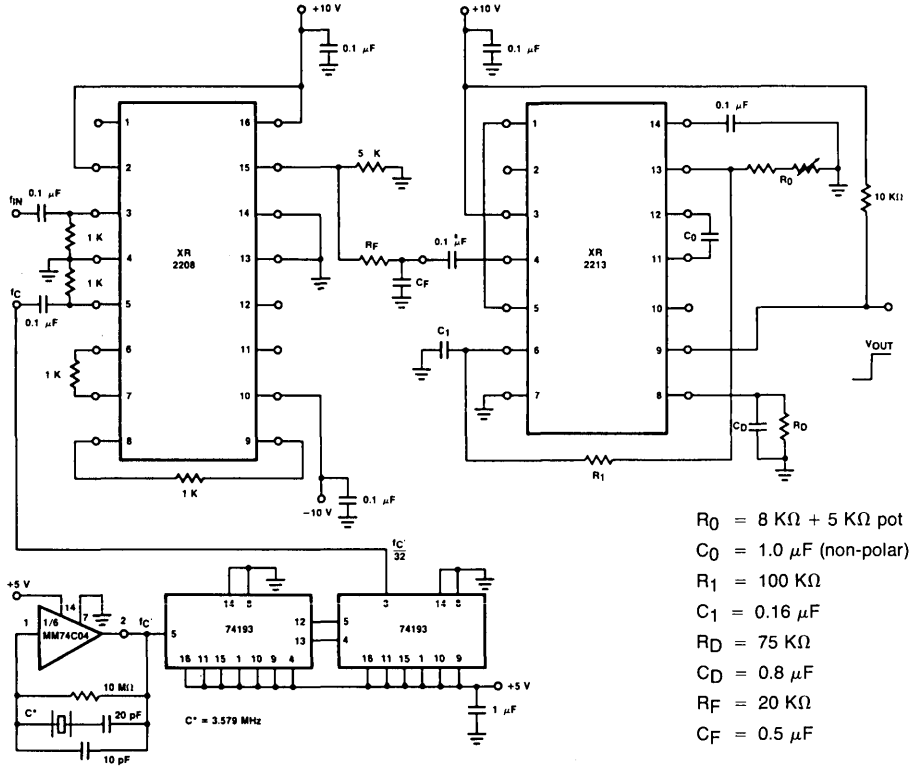


Figure 3. Circuit Schematic of Narrow Band Tone Decoder.

XR-210/XR-215/XR-S200 Phase-Locked Loops

INTRODUCTION

This Application Note discusses the various parameters and equations used in applying the XR-210, XR-215, and XR-S200 Phase Lock Loop (PLL) successfully. It describes the operation of the phase detector and the voltage controlled oscillator as well as a discussion on phase comparator gain, VCO gain, lock range, capture range and free running frequency. A section on low pass filters contains most common RC filters and a discussion on damping factor. Finally, a summary of PLL parameters and a design example are included.

XR-210

The functional diagram of the XR-210 Phase Locked Loop (PLL) is shown in Figure 1. The phase comparator produces a dc voltage which is directly proportional to the phase difference between the two input signals. This error voltage, V_{OUT}, is then filtered and applied to the voltage controlled oscillator (VCO), which in turn produces a periodic signal whose frequency is proportional to the error voltage. The VCO is actually a "current" controlled oscillator (ICO) in the sense that it is the current derived from V_{OUT} that actually controls the frequency of oscillation.

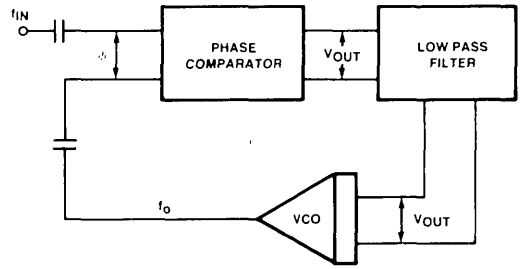


Figure 1. Phase Locked Loop Functional Diagram.

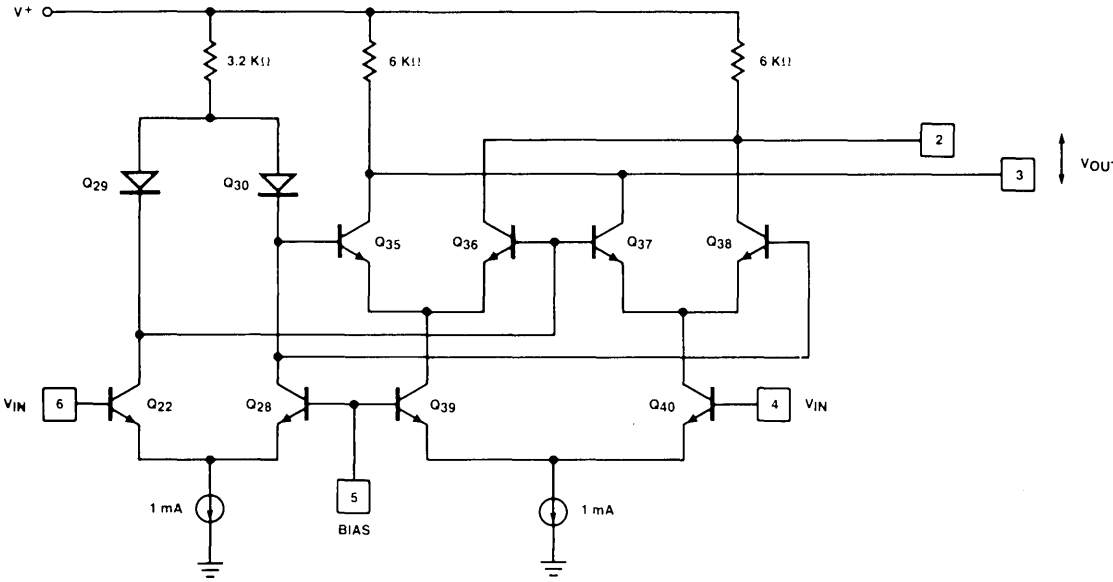


Figure 2. XR-210/XR-215 Phase Comparator.

AN-22

PHASE COMPARATOR

The circuit diagram of the XR-210 phase comparator is shown in Figure 2. The input pins (4 and 6) and the bias pin (5) are externally biased to approximately ½ V^+ to insure proper operation. The input signals must be capacitively coupled to Pins 4 and 6.

The output voltage on Pins 2 and 3, V_{OUT}, depends on the relative phase, ϕ, of the iput signals. The change of V_{OUT} with respect to the change in ϕ is defined as the phase comparator conversion gain and is given by:

$$K\phi = \frac{\Delta V_{OUT}}{\Delta\phi} \frac{\text{VOLTS}}{\text{RADIAN}} \qquad (1)$$

To examine how V_{OUT} changes with ϕ, consider the following three cases. It is assumed that the input voltage is large enough (> 50 mV_{RMS}) to cause limiting in the differential stage. All calculations are done at $V^+ = 12$ volts.

Case 1: Input voltages are equal to the bias voltage.

The operating current is shared equally between transistors Q_{22}, Q_{28}, Q_{39}, and Q_{40}. This causes approximately 0.5 mA to flow through the output resistor (6 KΩ) and hence $V_{OUT} = 0$ volts. The voltage on Pin 2 and Pin 3 is approximately equal to:

$$V^+ - (0.5\text{ mA})(6K\Omega) = 9\text{ volts.}$$

Case 2: Input voltages are both greater than the bias.

Q_{22} and Q_{40} conduct 1 mA each, causing Q_{38} to conduct 1 mA. Therefore $V_2 \cong 6$ volts, $V_3 \cong 12$ volts and hence $V_{OUT} \cong -6$ volts.

The same output conditions are obtained if the input voltages were both less than the bias.

Case 3. Input voltages are out of phase and V_{IN} (Pin 6) is greater than the bias.

Q_{22} and Q_{39} conduct 1 mA each, causing Q_{35} to conduct 1 mA. Therefore, $V_3 \cong 6$ volts, $V_2 \cong 12$ volts and hence $V_{OUT} \cong +6$ volts.

The same output conditions are obtained if V_{IN} (Pin 4) were greater than the bias.

Figure 3 shows the output voltage wave form when the input signals are 90° and 45° out of phase.

Notice that the duty cycle of the output waveform changes as the phase difference of the input signals change. For illustration purposes, square waves are shown as input signals, however, other periodic waveforms would produce similar output waveforms.

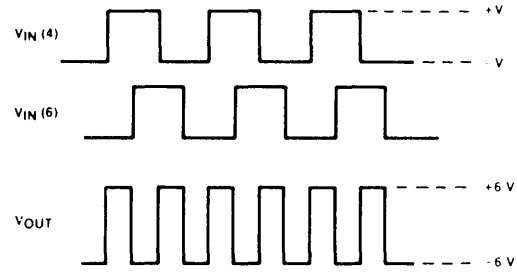


Figure 3a. 90° Out of Phase.

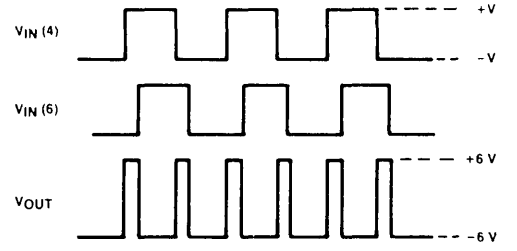


Figure 3b. 45° Out of Phase.

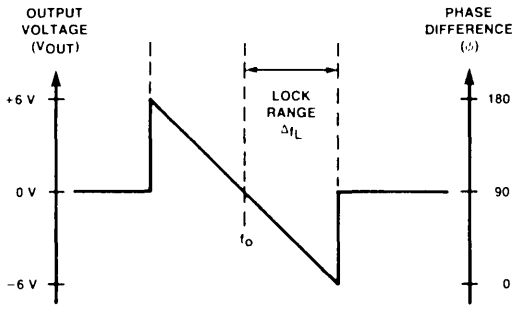


Figure 4a. Phase Detector With No Saturation.

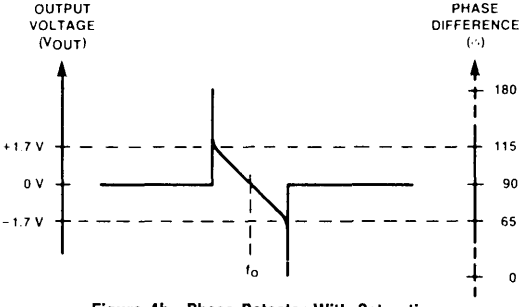


Figure 4b. Phase Detector With Saturation.

The output of the phase detector is connected to a low pass filter which converts the square wave output to an approximate dc voltage. The relationship of this dc voltage, V_{OUT}, with respect to the input phase difference, ϕ, is shown graphically in Figure 4a. Assuming no saturation occurs in the internal circuitry, a PLL can lock onto an input signal with maximum difference of 180° to 0° with respect to the VCO signal.

Due to internal saturation of the output, the maximum phase difference the XR-210 can track is approximately 50° or 90° ±25°. This is because the output transistors of the phase detector saturate at approximately 8.3 volts and the maximum output voltage, V_{OUT}, obtainable is about ±1.7 volts. Figure 4b shows the phase detector characteristic of the XR-210.

It is possible to obtain a tracking range close to 90° ± 90° by connecting an external resistor network to the phase detector output as shown in Figure 5. This circuitry limits the output swing to 10 ± 1 volt and prevents the internal circuitry from saturating at extreme phase conditions.

The phase comparator gain for the XR-210 is approximately given by:

$$K\phi \cong 4.0 \frac{\text{VOLTS}}{\text{RADIAN}} \qquad (2)$$

With the external bias network, it is approximately:

$$K\phi \cong \frac{\text{VOLTS}}{\text{RADIAN}} \qquad (3)$$

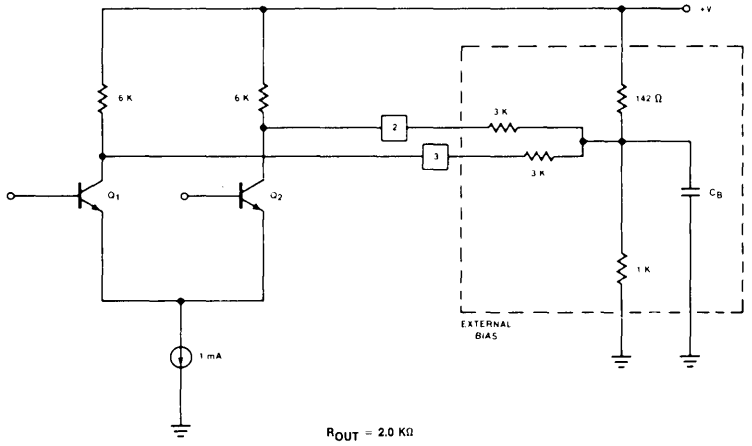


Figure 5. External Resistor Bias Network.

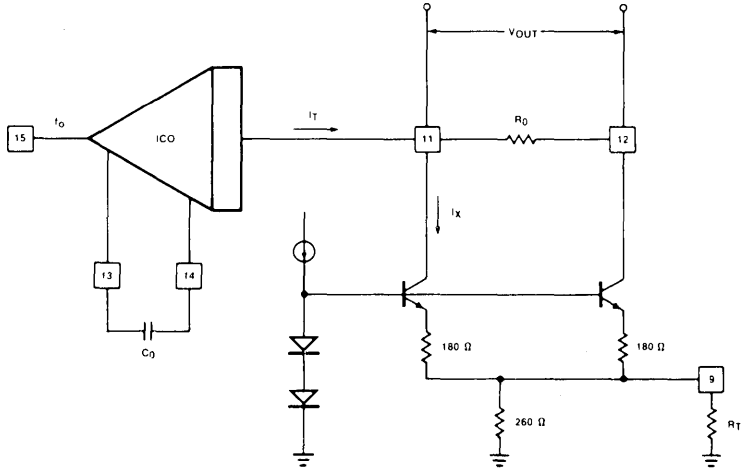


Figure 6. XR-210 Current Controlled Oscillator.

CURRENT CONTROLLED OSCILLATOR (ICO)

The functional diagram of the ICO is shown in Figure 6. The output frequency, f_o, is directly proportional to the total timing current, I_T, seen by the ICO.

$$f_o \alpha I_T \quad (4)$$

Any change in output voltage of the phase comparator causes a change in f_o as follows:

$$\Delta f_o \alpha \frac{\Delta V_{OUT}}{R_0} \quad (5)$$

where R_0 is the external resistor between Pins 11 and 12. It will be shown in the following section how R_0 sets the lock range of the PLL.

Combining equations 4 and 5 yields:

$$\frac{\Delta F}{\Delta V_{OUT}} = \frac{f_o}{R_0 I_T} \quad (6)$$

where I_T is the total timing current with V_{OUT} = 0 volt. In this case, $I_T = I_X \cong 1$ mA. Substituting this into equation 6 yields the ICO conversion gain:

$$K_0 = \frac{\Delta\omega}{\Delta V_{OUT}} \cong \frac{2\pi f_o}{R_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (7)$$

where R_0 is in KΩ.

The minimum value of R_0 should be approximately 1.7 KΩ. This is because the maximum current through R_0 must be limited to 1 mA and since V_{OUT} has a maximum range of approximately ±1.7 volts, R_0 must be limited to greater than 1.7 KΩ.

The free running frequency of the PLL is given by:

$$f_o \cong \frac{200}{C_0} \quad C_0 \text{ is in } \mu F. \quad (8)$$

Substituting this into ICO gain equation 7 yields:

$$K_0 \cong \frac{1256}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (9)$$

where R_0 is in KΩ and C_0 is in μF.

Experimental data yields:

$$K_0 \cong \frac{910}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (10)$$

The above equations were calculated without the ICO tuning resistor, R_T, connected to Pin 9. Adding R_T increases the timing current and hence increases the free running frequency. f_o:

The change in timing current with R_T is given by:

$$\Delta I_T \cong \frac{0.17}{R_T} \text{ mA} \quad (11)$$

The free running frequency can now be given by:

$$f_o \cong \frac{200}{C_0}\left(1 + \frac{0.17}{R_T} \text{ Hz}\right) \quad (12)$$

where R_T is in KΩ and C_0 is in μF.

The ICO gain is now:

$$K_0 = \frac{\Delta\omega}{\Delta V_{OUT}} = \frac{2\pi f_o}{R_0 I_T} \cong \frac{2\pi\left(\frac{200}{C_0} 1 + \frac{0.17}{R_T}\right)}{R_0 I_T} \quad (13)$$

However, the timing current is now:

$$I_T \cong \left(I_X + \frac{0.17}{R_T}\right) \text{ mA} = \left(1 + \frac{0.17}{R_T}\right) \text{ mA} \quad (14)$$

Substituting this into the ICO equation yields:

$$K_0 \cong \frac{200(2\pi)}{C_0 R_0} = \frac{1256}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (15)$$

and remains unchanged with the addition of R_T.

Note: The discrepancy between the calculated and measured K_0 can be attributed to tolerances of internal resistors and errors in approximating I_X.

LOCK RANGE

The lock range of a PLL, $\pm\Delta\omega_L$, is given by:

$$\pm\Delta\omega_L = (K\phi)(K_0)(\theta_E) \frac{\text{RADIANS}}{\text{SEC}} \quad (16)$$

where θ_E is the maximum phase difference at the detector inputs in radians. θ_E is approximately equal to 0.43 radians (25°).

Using measured values for $K\phi$ and K_0 yields:

$$\pm\Delta\omega_L \cong \frac{1565}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}} \quad (17)$$

where R_0 is in KΩ and C_0 is in μF.

XR-215

The XR-215 PLL is basically the same as the XR-210. The major difference is in the ICO section which is described below.

PHASE COMPARATOR

The phase comparator conversion gain is given by:

$$K\phi \cong 3.6 \frac{\text{VOLTS}}{\text{RADIAN}} \quad (18)$$

Saturation of the internal circuitry occurs limiting the tracking range of the phase detector to about 90° ± 25°.

An external resistor network shown in Figure 5 can increase the range to about 90° ± 90°. The corresponding conversion gain becomes:

$$K\phi \cong 1.3 \frac{\text{VOLTS}}{\text{RADIAN}} \quad (19)$$

ICO

The current controlled oscillator of the XR-215 is shown in Figure 7. The ICO conversion gain is given by:

$$K_0 = \frac{2\pi f_o}{R_0 I_X} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (20)$$

Since $I_X = 1.1$ mA and $f_o = \frac{220}{C_0}$,

$$K_0 \cong \frac{1256}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (21)$$

where R_0 is in KΩ and C_0 is in μF.

Experimental data yields:

$$K_0 \cong \frac{1140}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (22)$$

With the ICO tuning resistor, R_X, connected to Pin 10, the free running frequency is increased by a factor proportional to the change in timing current:

$$\Delta f \propto \Delta I_T \cong \frac{0.7}{R_X} \quad (23)$$

The ICO free running frequency is given by:

$$f_o \cong \frac{220}{C_0}\left(1 + \frac{0.7}{R_X}\right) \quad (24)$$

where R_X is in KΩ and C_0 is in μF.

$$K_0 \cong \frac{1140}{R_0 C_0} \frac{\text{RADIANS/SEC}}{\text{VOLT}} \quad (25)$$

and remains unchanged with the addition of R_X.

LOCK RANGE

The lock range of the XR-215, $\pm\Delta\omega_L$, is given by:

$$\pm\Delta\omega_L = (K\phi)(K_0)(\theta_E) \quad (26)$$

where θ_E is approximately equal to 0.43 radians (25°). Using measured values for $K\phi$ and K_0 yields:

$$\pm\Delta\omega_L \cong \frac{1765}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}} \quad (27)$$

where R_0 is in KΩ and C_0 is in μF.

Note: Using the external bias network (Figure 5) does not change K_0. To calculate the lock range with this network, θ_E should be set to approximately $\pi/2$ radians (90°).

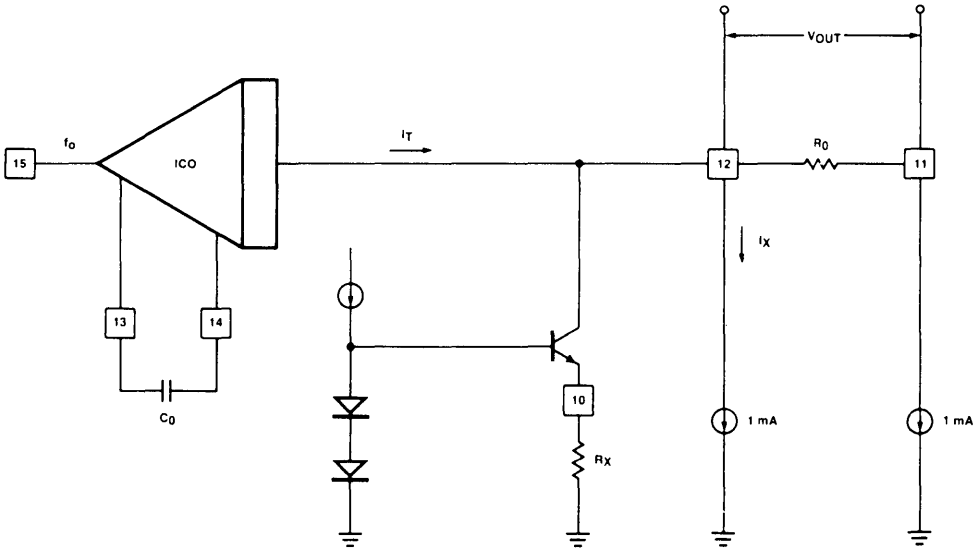


Figure 7. XR-215 ICO.

XR-S200

The XR-S200 PLL is basically the same as the XR-210 and 215 except that many of the interconnections are made external to the chip. These external connections can aid in the flexibility of the chip.

PHASE COMPARATOR

The phase comparator outputs are not tied internally to the ICO as the XR-210 and 215. The measured phase comparator gain is approximately:

$$K\phi \cong 4\,\frac{\text{VOLTS}}{\text{RADIAN}} \qquad (28)$$

Saturation of the internal circuitry occurs limiting the tracking range to about 90° ± 25°. This range can be increased by using the bias network shown in Figure 5.

ICO

The current controlled oscillator of the XR-S200 is shown in Figure 8. The ICO gain is given by:

$$K_O = \frac{2\pi\, f_o}{R_0\, I_T}\,\frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (29)$$

where I_T is the timing current when $V_{OUT} = 0$ volts.

The ICO free running frequency, f_o, can be modified by applying a digital pulse on Pins 15 and 16 through a diode and a 1 KΩ resistor. By changing the voltage states on these Pins, it is possible to obtain four discrete frequencies for f_o. By connecting a resistor from either Pin 15 or 16 to ground, it is also possible to modify the center frequency.

With Pins 15 and 16 open, f_o is given by:

$$f_o \cong \frac{200}{C_0}(I_X + I_1 + I_2) = \frac{500}{C_0}\ \text{Hz} \qquad (30)$$

since $I_X \cong 1$ mA, $I_1 \cong 0.5$ mA, $I_2 \cong 1$ mA.

With Pins 15 and 16 tied high, f_o is given by:

$$f_o \cong \frac{200}{C_0}(I_X) = \frac{200}{C_0}\ \text{Hz} \qquad (31)$$

where C_0 is in μF.

With Pins 15 and 16 open:

$$K_O = \frac{2\pi\, f_o}{R_0\, I_T} \cong \frac{3142}{R_0\, C_0\, I_T} \qquad (32)$$

where $I_T = I_X + I_1 + I_2 \cong 2.5$ mA, thus

$$K_O \cong \frac{1256}{R_0\, C_0}\,\frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (33)$$

where R_0 is in KΩ and C_0 is in μF.

With Pins 15 and 16 tied high:

$$K_O \cong \frac{1256}{R_0\, C_0\, I_T} \qquad (34)$$

where $I_T = I_X \cong 1$ mA. Thus

$$K_O \cong \frac{1256}{R_0\, C_0}\,\frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (35)$$

and remains unchanged.

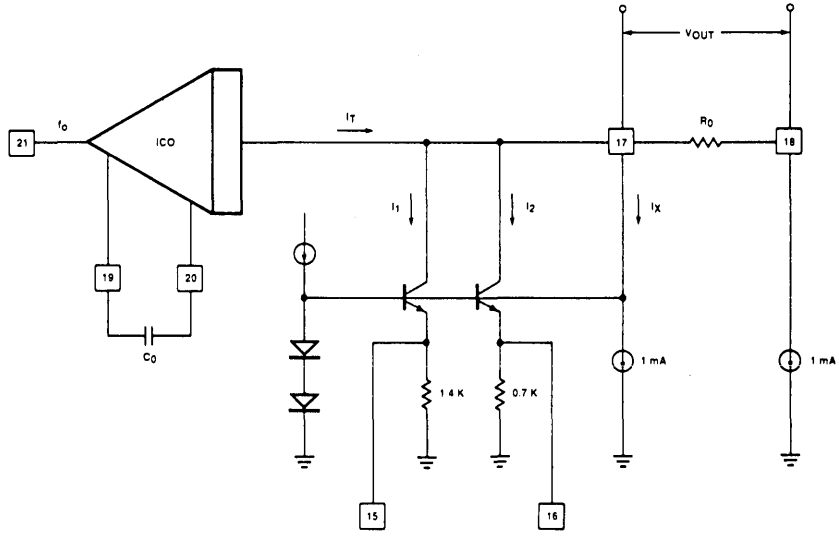


Figure 8. XR-S200 ICO.

LAG FILTER

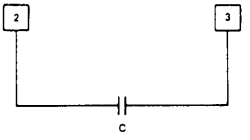
$$F(S) = \frac{1}{1 + \tau_1 S}$$

$$\tau_1 = R_1 C$$

$$\omega_\eta = \sqrt{\frac{K_V}{\tau_1}}$$

$$\delta = \frac{1}{2\sqrt{K_V \tau_1}}$$

LAG FILTER



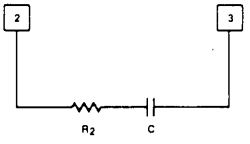
$$F(S) = \frac{1}{1 + 2\tau_1 S}$$

$$\tau_1 = R_1 C$$

$$\omega_\eta = \sqrt{\frac{K_V}{2\tau_1}}$$

$$\delta = \frac{1}{2\sqrt{2 K_V \tau_1}}$$

LAG-LEAD FILTER



$$F(S) = \frac{1 + \tau_2 S}{1 + S(2\tau_1 + \tau_2)}$$

$$\tau_1 = R_1 C; \tau_2 = R_2 C$$

$$\omega_\eta = \sqrt{\frac{K_V}{(2\tau_1 + \tau_2)}}$$

$$\delta = \frac{1}{2}\sqrt{\frac{K_V}{2\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K_V}\right)$$

FOR $\tau_1 \cdot \cdot \tau_2$

$$\delta = \frac{1}{2\sqrt{2K_V \tau_1}} \quad (1 + \tau_2 K_V)$$

LAG-LEAD FILTER

$$F(S) = \frac{1 + \tau_2 S}{1 + S(\tau_1 + \tau_2)}$$

$$\tau_1 = R_1 C; \tau_2 = R_2 C$$

$$\omega_\eta = \sqrt{\frac{K_V}{\tau_1 + \tau_2}}$$

$$\delta = \frac{1}{2}\sqrt{\frac{K_V}{\tau_1 + \tau_2}}\left(\tau_2 + \frac{1}{K_V}\right)$$

FOR $\tau_1 > > \tau_2$

$$\delta = \frac{1}{2\sqrt{K_V \tau_1}} \quad (1 + \tau_2 K_V)$$

Figure 9. Low Pass Filters.

Measured value for K_0 is approximately:

$$K_0 \cong \frac{1262}{R_0\,C_0}\,\frac{\text{RADIANS/SEC}}{\text{VOLT}} \qquad (36)$$

LOCK RANGE

Using measured values for $K\phi$ and K_0 yields:

$$\pm\Delta\omega_L \cong \frac{2170}{R_0\,C_0}\,\frac{\text{RADIANS}}{\text{SEC}} \qquad (37)$$

where R_0 is in KΩ, and C_0 is in μF.

LOW PASS FILTER

The low pass filter section for the XR-210/215/S200 is formed by connecting an external capacitor or RC network across the output of phase comparator section. Most common passive low pass filters are shown in Figure 9. R_1 is the internal resistor with nominal value of 6 KΩ. If an external bias network as shown in Figure 5 is used, R_1 = 2 KΩ. Pin numbers shown in Figure 9 apply to the XR-210 and XR-215.

The term K_V shown in the filters is the total forward gain of the PLL and is equal to the product of $K\phi$ and K_0.

CAPTURE RANGE

The capture or acquisition range of the PLL, $\pm\Delta\omega_C$, can be approximated as:

$$\pm\Delta\omega_C \cong \pm\Delta\omega_L\,|F(j\,\Delta\omega_C)| \qquad (38)$$

where $|F(j\,\Delta\omega_C)|$ is the magnitude of the low pass filter evaluated at $\omega = \Delta\omega_C$. Since $|F(j\,\Delta\omega_C)|$ is always less than unity, the capture range is always smaller than the lock range.

There is no explicit relationship for calculating $\Delta\omega_C$, however for a *simple lag* filter, it can be expressed as:

$$\pm\Delta\omega_C \cong \sqrt{\frac{K_V}{\tau_1}}\,\frac{\text{RADIANS}}{\text{SEC}} \qquad (39)$$

For lag-lead filters, capture range can be roughly estimated by ω_η. (See Figure 9.) Actual data indicates that capture range is larger than ω_η and approaches the lock range.

DAMPING FACTOR

The advantage of using a lag-lead filter is that generally speaking, it gives better stability due to the extra zero. The damping factor can be adjusted without necessarily changing the capture range. With a simple lag filter, however, by adjusting τ, the damping factor as well as the capture range is changed. These two parameters can be individually controlled in a lag-lead filter.

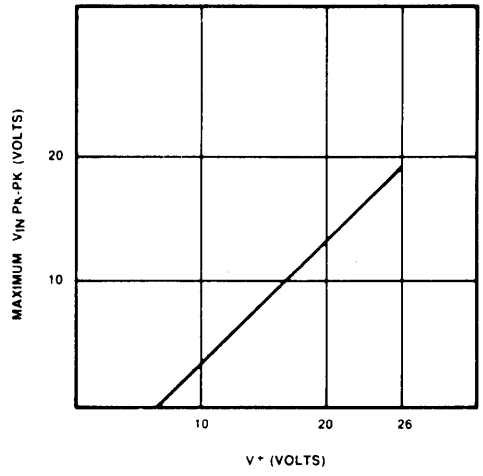


Figure 10. Maximum Input Voltage vs. Supply Voltage.

General systems and control theory indicates that for maximum stability the damping factor, δ, must be greater than 0.7. In many FSK demodulation circuits using Exar PLLs, it was found that with δ as low as 0.2, the circuit functions properly at high baud rates.

DESIGN EXAMPLE

Design an FSK demodulator using the XR-210 with the following specifications:

Mark frequency: 1070 Hz
Space frequency: 1270 Hz
V_{CC}: +12 volts

1. f_0 = 1170 Hz

   $$C_0 = \frac{200}{f_0} \cong 0.2\ \mu F$$

   Adjust R_T (Pin 9 to GND) for correct f_0.

2. $\Delta\omega_L = 2\pi\,(\Delta f_L) = 2\pi\,(200\text{ Hz}) = 1256$ RAD/SEC

   $$R_0 = \frac{1565}{\Delta\omega_L\,C_0} = 6.23\ K\Omega$$

3. Set capture range, $\Delta\omega_C$, equal to $\Delta\omega_L$. Using a lag-lead filter, $\Delta\omega_C$ can be approximated by:

$$\Delta\omega_C \cong \omega_\eta = \sqrt{\frac{K_V}{2\tau_1 + \tau_2}}$$

$K_V = K_0 K\phi \cong 2921$

Let $R_2 = 50\ \Omega$. Thus $\tau_1 \gg \tau_2$

$C_1 = 0.15\ \mu F$

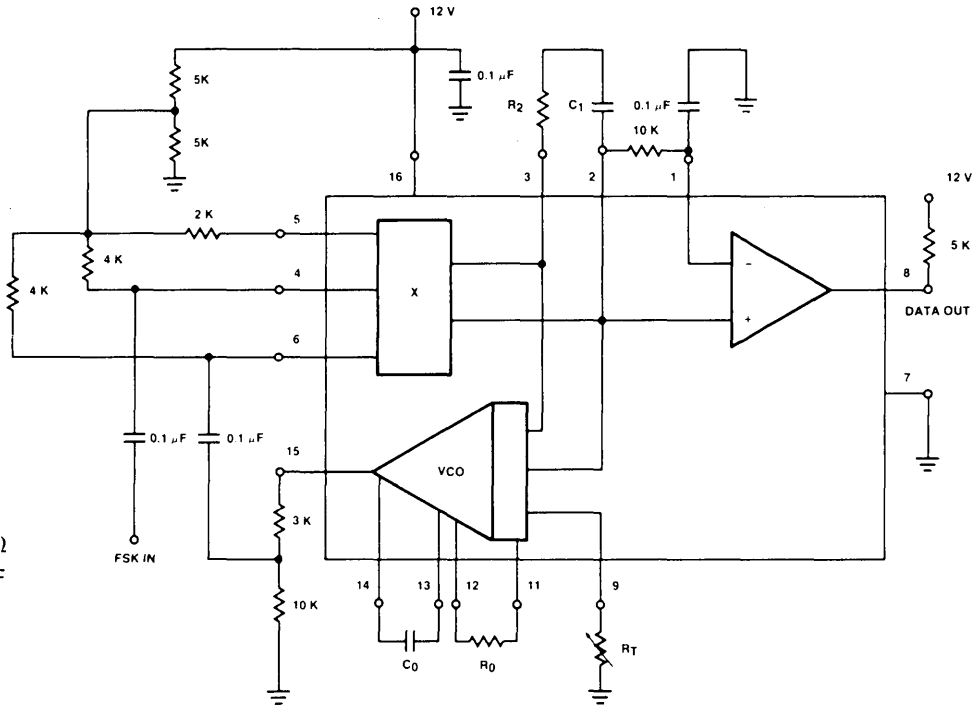
4. The damping factor is given by:

$$\delta = \frac{1}{2}\frac{1}{\sqrt{2\,K_V\,\tau_1}}\,(1 + \tau_2 K_V) \cong 0.22$$

Even with critical damping ($\delta < 1.0$), the XR-210 functions properly as an FSK demodulator with baud rate of 300 BPS.

5. For V^+ of 12 volts, the input voltage should be limited to 5 volts PK-PK to avoid internal saturation (see Figure 10).

6. Schematic for the above example is shown in Figure 11.



$C_0 = 0.2\ \mu F$
$R_0 = 6.23\ K\Omega$
$C_1 = 0.15\ \mu F$
$R_2 = 50\ \Omega$
$R_T = 10\ K\Omega$

Figure 11. XR-210 FSK Demodulation.

Table 1. Summary of PLL Parameters (1)

PARAMETER	XR-210	XR-215	XR-S200
Phase Comparator $K\phi$	$4.0 \frac{\text{VOLTS}}{\text{RADIAN}}$	$3.6 \frac{\text{VOLTS}}{\text{RADIAN}}$	$4.0 \frac{\text{VOLTS}}{\text{RADIAN}}$
VCO K_0	$\frac{910}{R_0 C_0} \frac{\text{RAD/SEC}}{\text{VOLT}}$	$\frac{1140}{R_0 C_0} \frac{\text{RAD/SEC}}{\text{VOLT}}$	$\frac{1262}{R_0 C_0} \frac{\text{RAD/SEC}}{\text{VOLT}}$
Lock Range $\pm\Delta\omega_L$	$\frac{1565}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}}$	$\frac{1765}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}}$	$\frac{2170}{R_0 C_0} \frac{\text{RADIANS}}{\text{SEC}}$
Free Running Frequency f_0	$\frac{200}{C_0}\left(1 + \frac{0.17}{R_T}\right)$ Hz	$\frac{200}{C_0}\left(1 + \frac{0.7}{R_T}\right)$ Hz	$\frac{500}{C_0}$ Hz (2)
Capture Range $\pm\Delta\omega_C$ (Simple Lag) (3)	$\sqrt{\frac{K_0 K\phi}{\tau_1}}$	$\sqrt{\frac{K_0 K\phi}{\tau_1}}$	$\sqrt{\frac{K_0 K\phi}{\tau_1}}$
Damping Factor δ (Simple Lag)	$\frac{1}{2}\sqrt{\frac{1}{K_0 K\phi \tau_1}}$	$\frac{1}{2}\sqrt{\frac{1}{K_0 K\phi \tau_1}}$	$\frac{1}{2}\sqrt{\frac{1}{K_0 K\phi \tau_1}}$

(1) R_0, R_T, R_X in KΩ
C_0 in μF

(2) f_0 shown for Pins 15 and 16 open

(3) For other filter configurations, refer to the filter section. $\tau_1 = R_1 C_1$.

High-Performance Frequency-To-Voltage Converter using the XR-2211

INTRODUCTION

A stable highly linear f/v converter can be easily designed using the XR-2211 phase locked loop. The f/v can be used for a dynamic range from ±1% to ±80% over a frequency range of .01 Hz to 1 MHz.

The block diagram of the f/v is shown in Figure 1. The circuit will perform f/v conversion according to the relationship

$$f_{IN} = -K_1 V_O + K_2$$

where K_1 and K_2 are set by the designer.

The transfer function relating V_O to f_{IN} is shown in Figure 2. The carrier detect output, Q, (Pin 5) which goes high over the tracking range is shown in Figure 3.

The basic circuit diagram is shown in Figure 4. The slope K_1 is determined by the relationship

$$K_1 = \frac{-1}{V_R C_0 R_1}$$

where $V_R = V_{CC}/2 - V_{BE}$

The x intercept or upper frequency, K_2 is determined by the relationship

$$K_2 = \frac{R_0 + R_1}{R_0 R_1 C_0} = f_{MAX}$$

DESIGN EXAMPLE

Design a f/v converter for the frequency range 100 Hz to 600 Hz.

The first step is to calculate the center frequency f_o, (Figure 2) in

$$f_o = \frac{f_L + f_H}{2} = \frac{100 + 600}{2} = 350 \text{ Hz}$$

Supply voltage is directly proportional to the degree of resolution obtainable.

In order to obtain a greater resolution a higher supply voltage is used. For this design an 18 V supply is used giving us a resolution of approximately

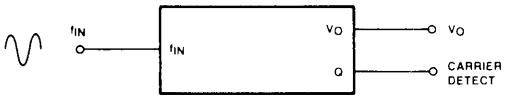


Figure 1. F/V Block Diagram.

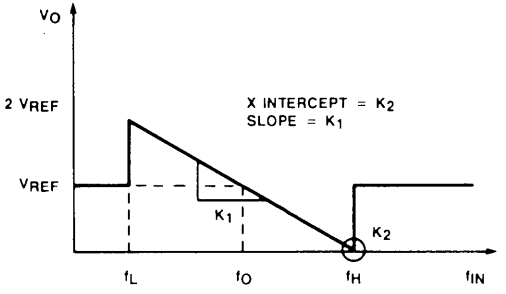


Figure 2. F/V Transfer Function.

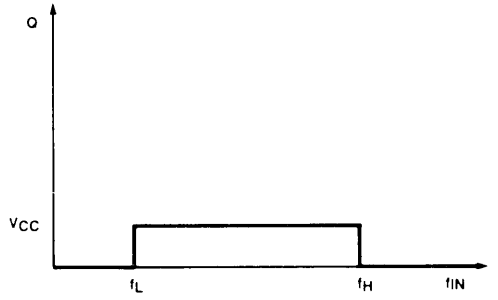


Figure 3. F/V Carrier Detect Output.

$$\text{resolution} \approx \frac{V_{CC} - V_{BE}}{f_H - f_L} = \frac{18 - 1.3}{600 - 100} = \frac{33.4 \text{ mV}}{\text{Hz}}$$

for V_{CC} = 18 V

We can now calculate V_{REF}

$$V_{REF} = V_{CC}/2 - V_{BE} = 9 \text{ V} - .65 \text{ V} = 8.35 \text{ V}$$

The center frequency is given by

$$f_o = \frac{1}{R_0 C_0}$$

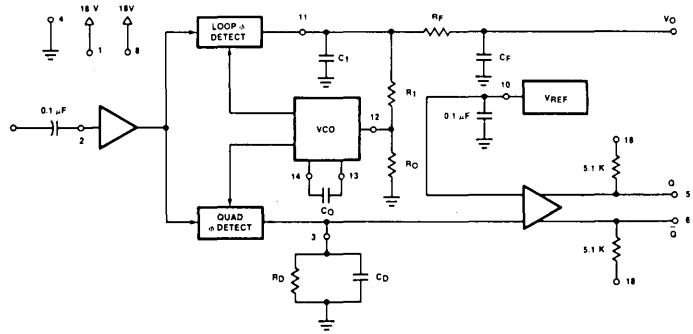


Figure 4. F/V Circuit Diagram.

choosing R_0 = 20 K and rearranging

$$C_0 = \frac{1}{R_0 F_0} = \frac{1}{(20\ K\Omega)\ (350\ Hz)}$$

$$= .143\ \mu F$$

Since $$\frac{R_0}{R_1} = \frac{(f_H - f_L)}{2\ f_0}$$

$$R_1 = \frac{2\ f_0\ R_0}{(f_H - f_L)} = \frac{2\ (350\ Hz)\ (20K)}{(600 - 100)\ Hz}$$

$$= 28\ K$$

The selection of C_1, the loop filter capacitor has a degree of flexibility in its value. For a damping coefficient of .5.

$$C_1 \approx \frac{C_0}{4} = \frac{.143\ \mu F}{4} = .035\ \mu F$$

It should be noted that an increased value of C_1 will increase response time but reduce ripple, while a decreased value of C_1 will reduce response time, increase capture range, but increase ripple.

The slope K_1 can now be calculated

$$K_1 = \frac{1}{V_R C_0 R_1} = \frac{1}{(8.35)\ (.143\ \mu F)\ (28\ K)}$$

$$= 29.91\ \frac{Hz}{V}$$

and since $K_2 = f_{MAX} = 600$ Hz

The transfer function is then given by

$$f_{IN} = -29.91\ V_0 + 600$$

The filter $R_F\ C_F$ forms a one-pole post detection filter, with a time constant

$$\tau = R_F\ C_F$$

and a cut-off frequency

$$f_C = \frac{1}{2\mu R_F C_F}$$

Selecting R_F = 100, K, C_F is then given by

$$C_F \approx \frac{3}{\Delta f/\Delta t}\ \mu F$$

where $\frac{\Delta f}{\Delta t}$ = maximum expected rate of change of input frequency

for $$\frac{\Delta f}{\Delta t} = 300\ cycles/sec$$

$$C_F = \frac{3}{300}\ \mu F = .01\ \mu F$$

giving τ = 1 μsecs F_C = 160 Hz

A carrier detect output is available at Pins 5 and 6 (Q and $\overline{Q}$). The components C_D and R_D comprise the lock-detect filter. For R_D = 470 K, and a capture range approaching the lock range, a minimum value of C_D is given by

$$C_D(\mu F) \geq \frac{16}{f_H - f_L} = \frac{16}{500} = .032\ \mu F$$

$$R_D = 470\ K$$

TEMPERATURE STABILITY

The XR-2211 is characterized by excellent temperature stability, in the order of 50 ppm/°C. The output voltage temperature coefficient can be calculated by

$$\frac{V}{°C} = \frac{1}{K_1} \times \frac{50\ ppm}{°C} \times (f_H - f_L)$$

substituting

$$= \frac{33.4\ mV}{Hz} \times 50\ ppm \times (600 - 100)\ Hz$$

$$= \frac{.8\ mV}{°C}$$

Digitally Programmable Phase-Locked Loop

INTRODUCTION

Most phase-locked loops require manual potentiometer adjustment if the center frequency of the circuit is critical. Also, once adjusted, if ambient temperature changes cause the PLL's VCO or center frequency to shift, the potentiometer would have to be readjusted if the accurate center frequency was to be maintained. Readjustments are, of course, an impractical solution.

This application note describes the design of a digitally programmable PLL. Being digitally controlled, a microprocessor or other digital circuitry could easily tune or retune the VCO when necessary. The design uses the XR-215 monolithic PLL together with the XR-9201 D/A converter, which provides the tuning function.

PRINCIPLES OF OPERATION

Figure 1 shows the block diagram of the digitally programmable PLL. The circuit is comprised of two blocks: the PLL and the D/A converter. The PLL is used for FM demodulation, synchronizing signals, or frequency synthesis. It processes these signals, which are centered around its free-running frequency, f_o. This f_o is set by the internal voltage-controlled oscillator, VCO, in the PLL. The VCO within the XR-215 is really a current-controlled oscillator, ICO. This is, the frequency of oscillation of the ICO is directly proportional to the timing current, I_T. I_T is made up of two components: an internal fixed current and an externally programmable current, $I_{PIN\ 10}$. This $I_{PIN\ 10}$ control current is provided by a D/A converter with a current output. Since the D/A provides an output current that is directly set by an input digital code, this code will actually control the center frequency of the PLL's ICO, f_o.

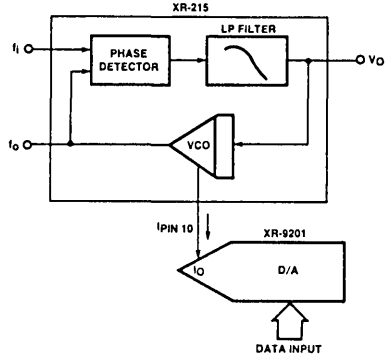


Figure 1. Programmable PLL Block Diagram.

CIRCUIT DESIGN

Figure 2 shows the XR-215 internal blocks and necessary external components. The VCO center frequency, f_o, is calculated by the formula:

$$f_o = \frac{200}{C_O}\left(1 + \frac{0.6}{R_X}\right) \frac{C_O \text{ in } \mu F}{R_X \text{ in } K\Omega} \qquad (1)$$

In this application it is desirable to have a variable current drawn from Pin 10, and R_X omitted. Equation 1 is then modified to equation 2 is a current instead of a resistor is used at Pin 10.

$$f_o = \frac{200}{C_O}(1 + I_{PIN\ 10}) \frac{C_O \text{ in } \mu F}{I_{PIN\ 10} \text{ in mA}} \qquad (2)$$

Equation 2 can now be used to determine $I_{PIN\ 10}$ for a given f_o adjustment range. Once the center frequency has been set, R_O can be calculated to adjust the tracking range using the relationship:

$$\pm\Delta W_L = 2\pi\Delta f_L \simeq \frac{1565}{R_O C_O} \frac{\text{rad}}{\text{sec}} \frac{R_O \text{ in } K\Omega}{C_O \text{ in } \mu F} \qquad (3)$$

or

$$R_O = \frac{1565}{2\pi\Delta f_L C_O} \quad R_O \text{ in } K\Omega,\ C_O \text{ in } \mu F \qquad (4)$$

Now with R_O calculated for Δf_L, the capture range, Δf_C is set using the loop time constant capacitors C_1:

$$\pm\Delta W_C = \sqrt{\frac{K_O K_\phi}{\tau_1}} = 2\pi\Delta F_C \qquad (5)$$

τ_1 = Loop Time Constant
K_O = VCO Conversion Gain
$K\phi$ = Phase Detector Conversion Gain

Substituting the values for $K_O K\phi$ and solving for F_C:

$$\Delta F_C = \frac{1}{2\pi}\sqrt{\frac{0.684}{R_O C_O C_1}} \qquad (6)$$

or

$$C_1 = \frac{0.017}{\Delta f_C^2 R_O C_O} \quad R_O \text{ in } K\Omega,\ C_O \text{ in } \mu F \qquad (7)$$

The resistors R_I and R_F are used to set the gain of the op amp when used for FM demodulation. C_C is op amp compensation and is in the range of 300 pF for unity gain to 50 pF for a gain of 10 and up. The resistors going to Pins 4, 5, and 6 are used to dc-bias the phase detector inputs at half supply, with their actual value not critical. The capacitors C_2 and C_1 are used for capacitive coupling.

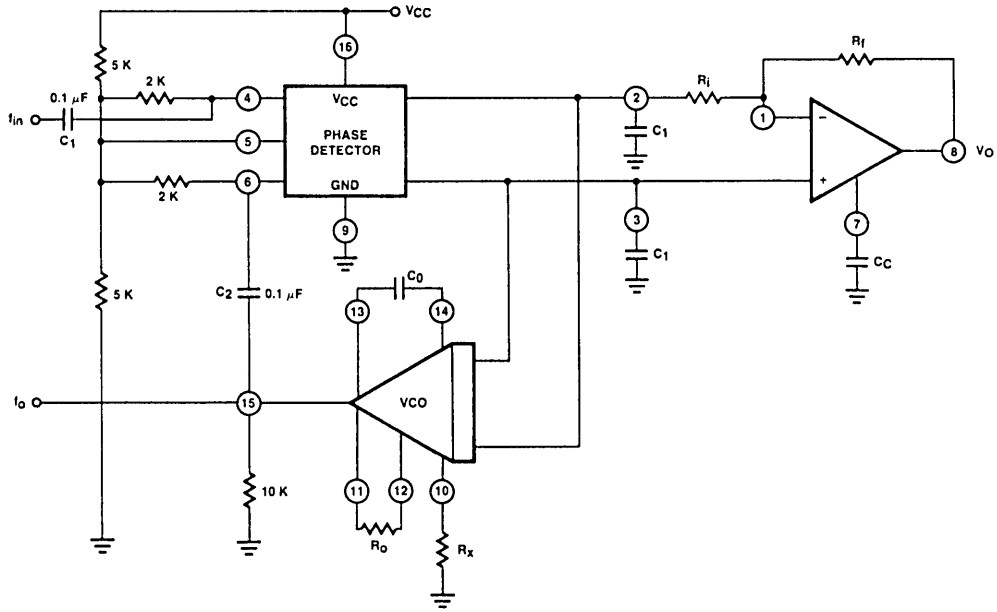


Figure 2. XR-215 with External Components.

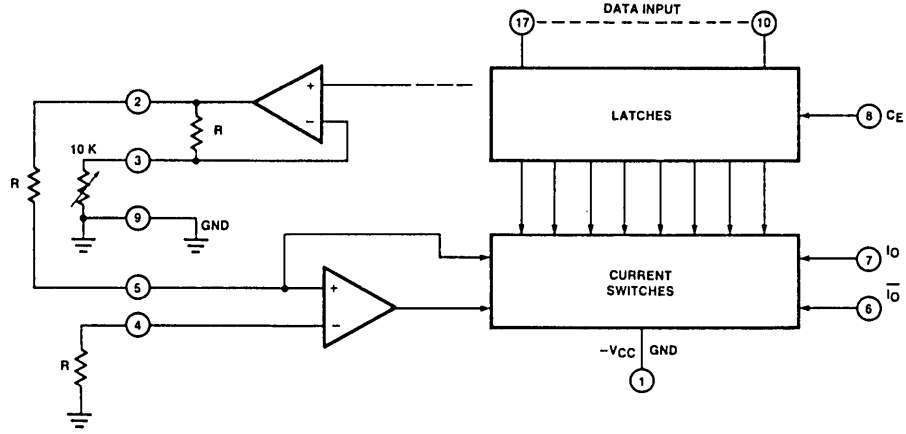


Figure 3. XR-9201 D/A with External Components.

Figure 3 shows the D/A converter internal blocks with external circuitry. Data is fed into the input latches, which will allow data to flow through to the current switches when C_E is high and hold data when C_E is low. The output currents are related to the digital inputs by:

$$I_O = 2\, I_{REF}\left[\frac{B_7}{2}+\frac{B_6}{4}+\frac{B_5}{8}+\frac{B_4}{16}+\frac{B_3}{32}+\frac{B_2}{64}+\frac{B_1}{128}+\frac{B_0}{256}\right] \quad (8)$$

where B_N = 1 if bit N is high
B_N = 0 if bit N is low
B_7 = MSB
B_0 = LSB

Also: $I_O + \overline{I_O} = I_{FS}$ = Full-scale Current (9)

$$I_{FS} = 2\, I_{REF}\left(\frac{255}{256}\right) \quad (10)$$

The full-scale current is set using R by the relationship:

$$R = \frac{V_{REF}}{I_{REF}} \quad V_{REF} \simeq 2\ V \quad (11)$$

The 10 KΩ potentiometer from Pin 3 to ground is used to fine-adjust the internal reference to exactly 2.00 V.

Full-Duplex 1200 BPS/300 BPS Modem System

INTRODUCTION

This application note describes the construction of a full-duplex modem system which operates at either 1200 BPS with phase shift keying encoding (PSK) or 300 BPS with frequency shift keying (FSK). The 1200 BPS is in a synchronous format or 300 BPS asynchronous.

This system is not intended to be directly connected to the telephone network as this requires FCC approval.

PRINCIPLES OF OPERATION

The heart of this system is three LSI integrated circuits. The XR-2120 is a switched-capacitor filter (SCF) to provide precise bandpass filtering at 1200 Hz and 2400 Hz. The XR-2123 performs the 1200 BPS PSK modulation/demodulation and the XR-14412 the 300 BPS FSK modulation/demodulation. These three devices are shown with the necessary external functions to perform a 212A type synchronous modem in Figure 1. These other functions are described as follows:

LINE INTERFACE. Provide DC isolation between modem and telephone network. This section, known as a direct-access arrangement, must be approved by the FCC for direct connection to the telephone network.

AGC. Automatic gain control to provide a constant signal level to other portions of the circuit. Its received signal range can vary from about 0 dBm to −45 dBm.

DEMUX. Demultiplexer to switch transmitted carrier (Txc) and received data (Rxd) between 300 BPS and 1200 BPS.

AUTO SPEED SELECT. Automatically senses whether 300 BPS or 1200 BPS information is being received and controls the demux with this information.

SLICER. A voltage comparator used to convert analog receive carriers (Rxcar) into digital signals suitable for the XR-2123 and XR-14412 Rxcar inputs.

CARRIER DETECT (CD). A level sensor with a digital output to indicate when a Rxcar is present.

TIMING CIRCUIT. This circuit extracts a 600 Hz receive signal timing from the Rxcar for synchronization purposes in the XR-2123.

SCRAMBLER/DESCRAMBLER. These sections scramble the data to be transmitted (Txd) while descrambling the received data (Rxd).

DELAY CIRCUIT. To provide a delay between the request to send (RTS) data and clear to send (CTS) data commands.

Figure 2 shows the complete circuit implementation of modem, with Table 1 listing the recommended circuit values.

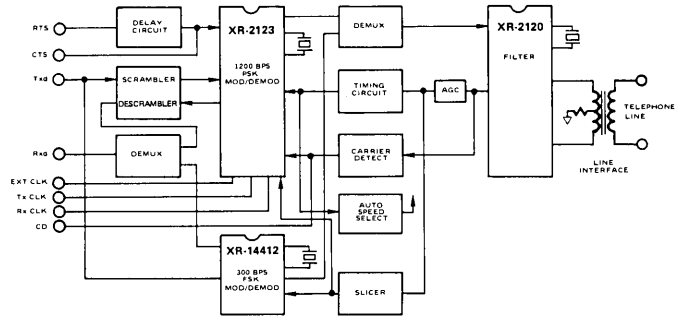


Figure 1. 212A Type Modem System.

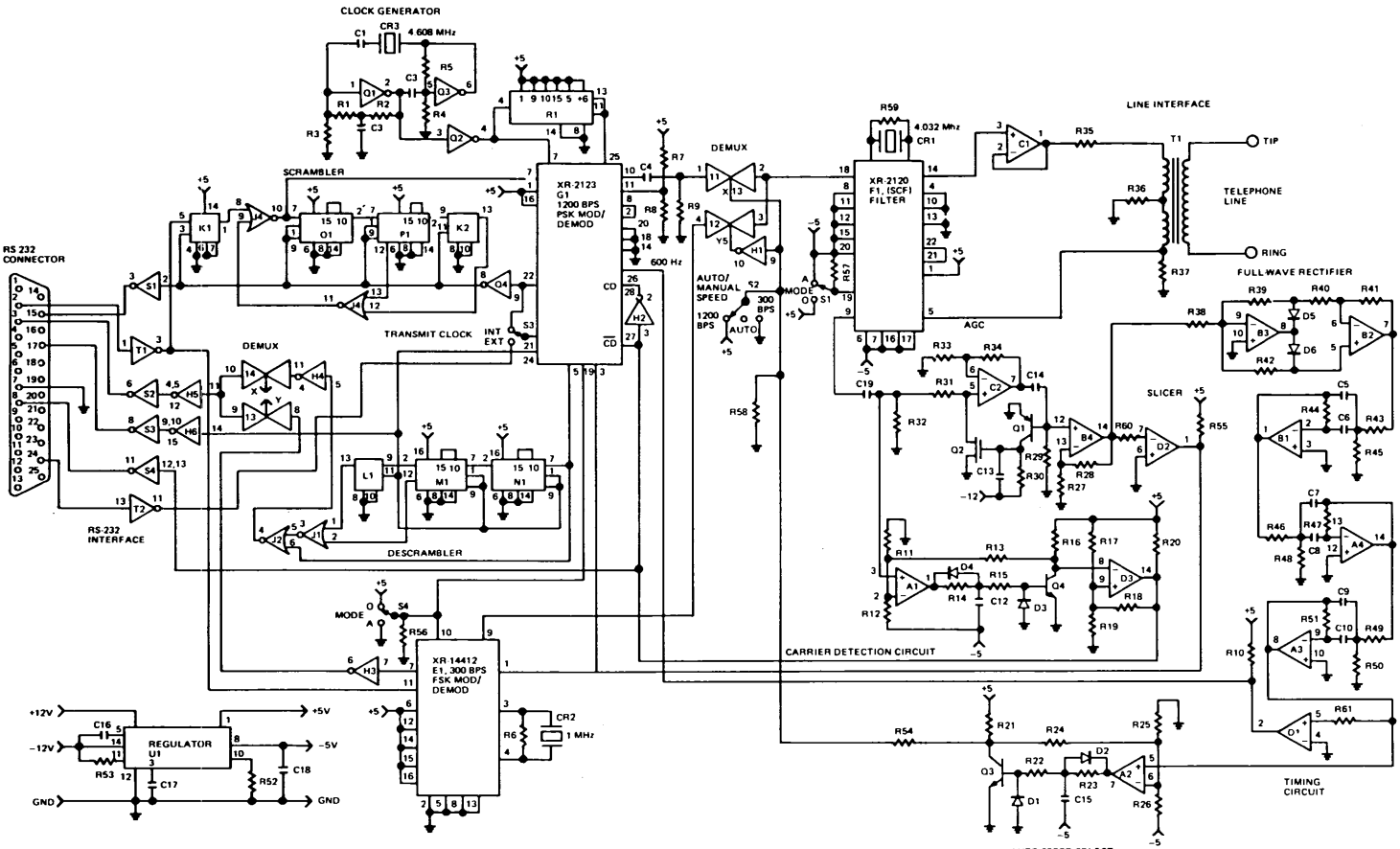


Figure 2. XR-212A Type Modem.

DESIGN EXAMPLE

Design a digitally programmable PLL with a center frequency, f_o, equal to 20 kHz. Provide for a 10% digital tuning range. The circuit shall also have the following lock and capture ranges:

$$\pm\Delta f_L = 5 \text{ kHz}, \pm\Delta f_C = 4 \text{ kHz}$$

1. Using equation 2, first with $I_{PIN\ 10} = 0$ (digital inputs all zeros) C_O can be determined.

$$f_o = \frac{200}{C_O} \qquad C_O = 0.01\ \mu F$$

2. This same equation is used to determine the maximum value of $I_{PIN\ 10}$ for a 10% change in f_o. Rearranging equation 2 yields:

$$I_{PIN\ 10\ (max)} = \frac{f_o C_O}{200} - 1 = \frac{22\text{ K } (0.01)}{200} - 1 = 0.1 \text{ mA}$$

$$f_o = 20 \text{ K} + 2 \text{ K Adjustment Range}$$

3. R_O is now calculated from equation 4:

$$R_O = \frac{1565}{(2\pi)\ (5\text{ K})\ (0.01)} \simeq 5\ \text{K}\Omega$$

4. C_1 is determined by equation 7:

$$C_1 = \frac{0.017}{(4\text{ K})^2\ (5)\ (0.01)} \simeq 0.022\ \mu F$$

5. The D/A components can now by specified, first using equation 10 and the previously calculated $I_{PIN\ 10}$ maximum current:

$$I_{PIN\ 10\ max} = I_{FS}\ 2\ I_{REF}\left(\frac{255}{256}\right)$$

$$I_{REF} \simeq 50\ \mu A$$

6. The reference current setting resistor, R, is now determined using equation 11:

$$R = \frac{2.00}{50\ \mu A} = 40\ \text{K}\Omega$$

7. Calibration of the system is accomplished by adjusting potentiometer R_3 for V_{REF} on the XR-9201 to exactly 2.00 V.

Figure 4 shows the completed design example.

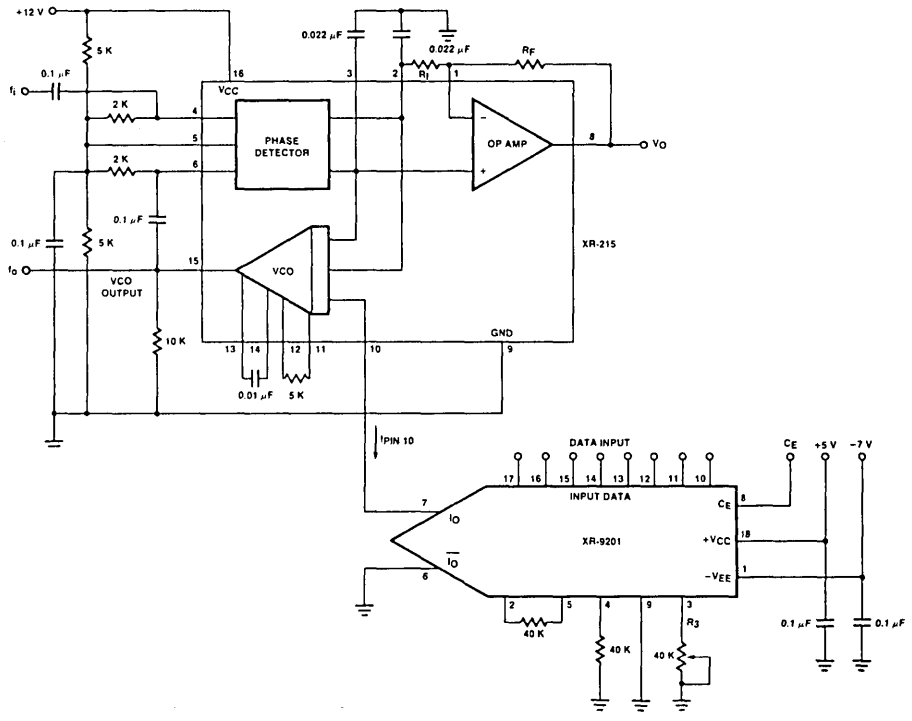


Figure 4. Digitally Programmable PLL.

A.	XR-4741 Quad Op Amp
B.	XR-4741 Quad Op Amp
C.	XR-1458 Dual Op Amp
D.	LM-339 Quad Comparator
E.	XR-14412 FSK Mod/Demod 300 BPS
F.	XR-2120 Filter-Switched Cap
G.	XR-2123 PSK Mod/Demod 1200 BPS
H.	CD-4049 Hex Inverter
I.	CD-4016 Quad B1-Lateral Switch
J.	CD-4030 Quad Exclusive-OR Gate
K.	CD-4013 Dual D Flip-Flop
L.	CD-4013 Dual D Flip-Flop
M.	Dual 4 Bit Static Register 4015
N.	Dual 4 Bit Static Register 4015
O.	Dual 4 Bit Static Register 4015
P.	Dual 4 Bit Static Register 4015
Q.	MM7404 Hex Inverter
R.	DM74193 Synchronous Up/Down Counter
S.	XR-1488 Quad Line Driver
T.	XR-1489 Quad Line Receiver
U.	XR-4194 Dual Tracking Regulator

R_1	2.2K	R_2	2.2K	R_3	2.2K
R_4	2.2K	R_5	1.2K	R_6	1M
R_7	10K	R_8	10K	R_9	1M
R_{10}	10K	R_{11}	1K	R_{12}	62K
R_{13}	100K	R_{14}	47K	R_{15}	62K
R_{16}	10K	R_{17}	100K	R_{18}	470K
R_{19}	100K	R_{20}	10K	R_{21}	10K
R_{22}	62K	R_{23}	47K	R_{24}	100K
R_{25}	18K	R_{26}	62K	R_{27}	1K
R_{28}	4.7K	R_{29}	10K	R_{30}	1M
R_{31}	120K	R_{32}	10K	R_{33}	1K
R_{34}	68K	R_{35}	600	R_{36}	300
R_{37}	600	R_{38}	10K	R_{39}	10K
R_{40}	10K	R_{41}	10K	R_{42}	10K
R_{43}	39K*	R_{44}	180K*	R_{45}	392*
R_{46}	39K*	R_{47}	180K*	R_{48}	392*
R_{49}	39K*	R_{50}	464*	R_{51}	180K*
R_{52}	13K	R_{53}	71.5K	R_{54}	10K
R_{55}	10K	R_{56}	10K	R_{57}	10K
R_{58}	10K	R_{59}	1M	R_{60}	10K
R_{61}	10K				

All resistor values are in ohms.
* = >1% tolerance.

C_1	82 pF	C_{14}	1 μF
C_2	.033 μF	C_{15}	.1 μF
C_3	.022 μF	C_{16}	.001 μF
C_4	.1 μF	C_{17}	.001 μF
C_5	.033 μF	C_{18}	4.7 μF
C_6	.033 μF	C_{19}	2.2 μF
C_7	.033 μF	C_{20}	4.7 μF
C_8	.033 μF	C_{21}	4.7 μF
C_9	.033 μF	C_{22}	.1 μF
C_{10}	.033 μF	C_{23}	.1 μF
C_{11}	.1 μF	C_{24}	4.7 μF
C_{12}	0.22 μF	C_{25}	4.7 μF
C_{13}	4.7 μF	C_{26}	4.7 μF

Crystals

CR1 — 4.032 MHz	MTRON
CR2 — 1,000 MHz	FOX
CR3 — 4.608 MHz	X-TRON

Transformer

T1 — T2220 MICROTRAN

Transistors

Q1 — A854	ROHM
Q3 — C1741	ROHM
Q4 — C1741	ROHM

FETs

Q2 — 2N4861

Component List for 212A Type Modem System

High-Speed FSK Modem Design

INTRODUCTION

As the need for transmitting data increases, some applications require data to be sent faster than the conventional telephone line modems. This application note describes the design and construction of a high speed full-duplex, FSK modem using XR-2206 as a modulator and XR-210 as the demodulator transmitting data at the rate of 100 Kilobaud.

PRINCIPLES OF OPERATION

The block diagram in Figure 1 describes the basic building block in any FSK modem system. The major difference is that in high speed applications, data is transmitted over a twisted pair wire or coaxial cable instead of the telephone line with its limited bandwidth. The complete system is comprised of an answer and originate modem. Simply stated, the modulator converts the input data to two discrete frequencies corresponding to its 1's and 0's and is then sent over a line or cable. The line hybrid steers these frequencies to the bandpass filter, where it will remove any unwanted signals that might have gotten through due to the line or cable before reaching the demodulator. The demodulator, which is a phase locked loop, will lock onto the incoming frequencies and produce 1's and 0's on its output. A detailed description on FSK techniques is given in the EXAR MODEM DESIGN HANDBOOK.

DESIGN EQUATIONS — Refer to Figure 6

1. The frequency of oscillation of the XR-2206 when used as a modulator, with the FSK input (Pin 9) is high is:

$$\frac{1}{R7A + R7B\ C_3}$$

When the FSK input (Pin 9) is low the frequency equals

$$\frac{1}{R8A + R8B\ C_3}$$

2. The filter best suited for modem applications is the butterworth filter due to its linear phase response within the passband. Table 1 shows the normalized capacitor values for butterworth filters up to fifth order.

Table 1

ORDER NO.	C1	C2	C3
2	1.414	.7071	
3	3.546	1.392	.2024
4	1.082	.9241	
	2.613	.3825	
5	1.753	1.354	.4214
	3.235	.3090	

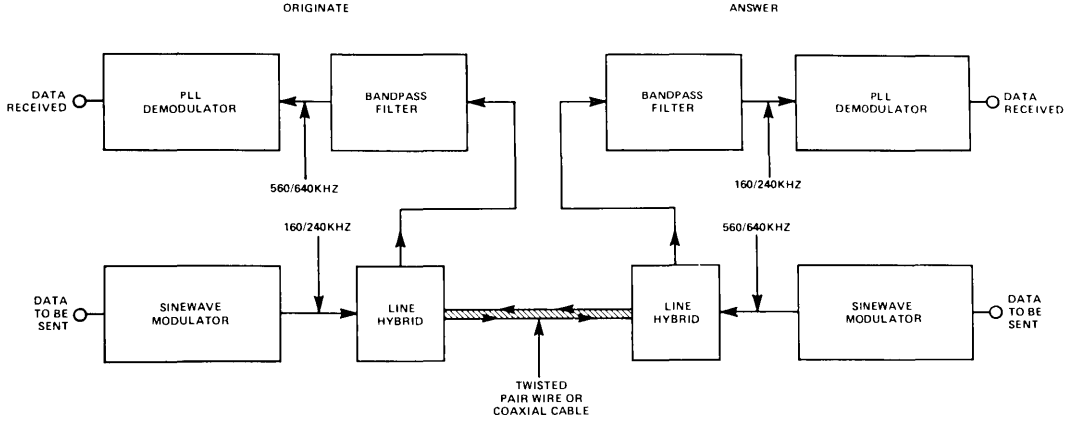


Figure 1. Block Diagram of High Speed FSK Modem System

Figure 3 shows a third order active high pass filter. To solve for the actual resistor values we use the formula:

$$R = \frac{1}{W_C\, CN\, C}$$

Where CN is the normalized capacitor and $W_C = 2\pi F_C$. In this equation, make all capacitors equal.

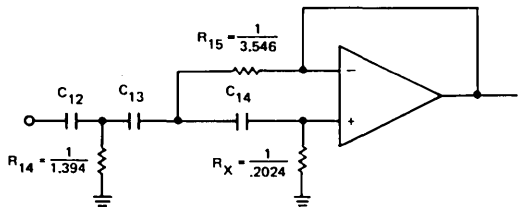


Figure 3.

After calculating R_X remember for single supply operation the op amp must be biased at 1/2 V_{CC}; therefore take twice the calculated value for R_X and configure as shown in Figure 4.

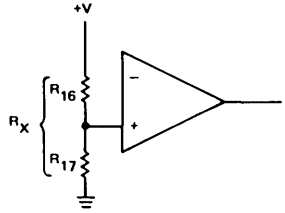


Figure 4.

Figure 5 shows a third order active butterworth low pass filter. To convert from the normalized capacitor values to the actual capacitor values, we use the formula:

$$C = \frac{CN}{W_C R}$$

Where CN is the normalized capacitor value and $W_C = 2\pi F_C$. In this equation, make all resistors equal.

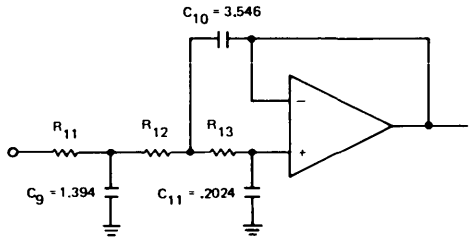


Figure 5.

The equations for using the XR-210 as an FSK demodulator are as follows:

$$\Delta F_L = (2)\Delta F$$

$$\Delta F = F_{mark} - F_{space}$$

$$\Delta F_L = 2(F_{mark} - F_{space})$$

$$F_0 = \frac{F_{mark} + F_{space}}{2}$$

$$F_0 = \frac{234}{C_0}\left(1 + \frac{.1}{R_T}\right) \quad \begin{array}{l} C_0 \text{ is in } \mu f \\ R_T \text{ is in K}\Omega \end{array}$$

$$C_0 = \frac{234}{F_0}$$

$$\Delta W_C = \sqrt{\frac{\Delta WL}{6KC1}}$$

$$\Delta W_L = 2\pi\, \Delta F_L$$

$$C_1 = \frac{\Delta WL}{6K\Delta W_C{}^2}$$

$$R_0 = \frac{2(1565)}{\Delta WLC_0} \qquad R_0 \text{ is in K}\Omega$$

$$C18 = \frac{10^{-4}}{2\pi\,(\text{Baud Rate})}$$

$$C19 = \frac{10^{-4}}{3\pi\,(\text{Baud Rate})}$$

DESIGN EXAMPLE

Design a FSK Demodulator with the following specification:

$F_0 = 200$ kHz

$\Delta F_L = 160$ kHz

Baud Rate = 100 Kilobaud

In this example, we **must** know the mark and space frequencies. If $F_{mark} = 160$ kHz and $F_{space} = 240$ kHz, the free running frequency is equal to

$$\frac{F_{mark} + F_{space}}{2}$$

$$= 200 \text{ kHz}$$

In order to calculate the free running frequency, we use the formula:

$$F_0 = \frac{234}{C_0}$$

In this example we will use a variable resistor (R_T) in order to fine tune F_0 to exactly 200 kHz, therefore:

$$F_0 = \frac{234}{C_0}\left(1 + \frac{.1}{R_T}\right)$$

The lock range (ΔF_L) is equal to twice the difference of the mark and space frequencies, so

$$\Delta F_L = 2(F_{space} - F_{mark})$$

R_0, which sets the lock range equals:

$$R_0 = \frac{2(1565)}{\Delta WLC_0} \qquad \Delta WL = 2\pi F_L = 6.28\,(160\times10^3) = 1004800$$

$$= \frac{2(1565)}{1004800.0015} \qquad \text{Where } C_0 \text{ is in } \mu f \text{ and } R_0 \text{ is in K}\Omega$$

$$= 2.0\ K\Omega$$

The Capture Range (ΔF_C) is equal to:

$$\Delta W_C = \sqrt{\frac{\Delta WL}{6K\ C17}} \qquad \Delta W_C = 2\pi\Delta F_C \qquad \Delta W_L = 2\pi\Delta F_L$$

In order to solve for C17 we rearrange the equation to read.

$$C17 = \frac{\Delta WL}{(6K)\ W_C{}^2}$$

$$= \frac{1004800}{(6K)\ 753600^2} = 300\times10^{-12}$$

therefore:

$$\Delta W_C = \sqrt{\frac{1004800}{(6\times10^3)\ 300\times10^{-12}}}$$

$$= 118.97\ kHz$$

It is important to note C17 and 6K set the loop time constant. When used as an FSK Demodulator, the XR-210 has post detection filtering on the output of the phase detector. In order to calculate the values for C18 and C19 we use the relationships:

$$C18 = \frac{10^{-4}}{2\pi\ (Baud\ Rate)}$$

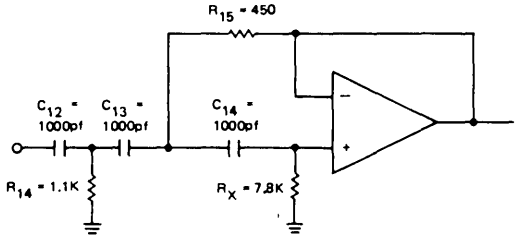
$$= \frac{10^{-4}}{6.28\ (100\times10^3)} = 160\times10^{-12} \text{ or } 160\ pf$$

$$C19 = \frac{10^{-4}}{9.42\ (100\times10^3)} = 106\times10^{-12} \text{ or } 106\ pf$$

For the filter, 18 dB of attenuation should be sufficient; therefore:

Design a third order high pass butterworth filter with f_C = 100 kHz.

1) In order to solve for actual resistor values use Table 1 and set all capacitors equal. The design example is shown below:



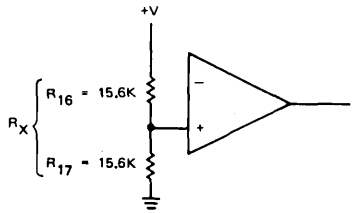
$$R = \frac{1}{W_C CN\ C}$$

$$R15 = \frac{1}{(6.28\times100\times10^3)3.546(1000\times10^{-12})} = 450\Omega$$

$$R14 = \frac{1}{(6.28\times100\times10^3)1.392(1000\times10^{-12})} = 1.1K\Omega$$

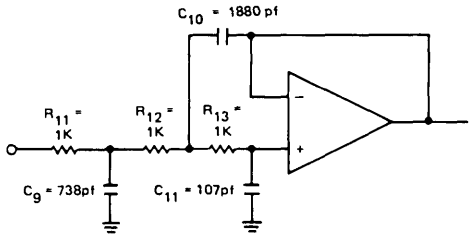
$$R_X = \frac{1}{(6.28\times100\times10^3).2024(1000\times10^{-12})} = 7.8K\Omega$$

After calculating R_X take twice the value and configure as shown below:



Design a third order lowpass butterworth filter with F_C = 300 kHz.

2) In order to solve the actual capacitances, use Table 1 and set all resistors equal. The design example is shown below:



$$C = \frac{CN}{W_C R} \qquad W_C = 2\pi F_C$$

$$C = \frac{3.546}{2\pi(300\times10^3)\ 1\times10^3} = 1880\ \text{pf}$$

$$C10 = \frac{3.546}{1884000000} = 1880\ \text{pf}$$

$$C9 = \frac{1.392}{1884000000} = 738\ \text{pf}$$

$$C11 = \frac{.2024}{1884000000} = 107\ \text{pf}$$

Design an FSK modulator with F_{mark} = 560 kHz and F_{space} = 640 kHz. The frequency of oscillation with the FSK input (Pin 9) is high is equal to:

$$F_{mark} = \frac{1}{R7A + R7B\ C3}$$

$$= \frac{1}{1\ K + 785\Omega.001\mu f} = 560\times10^3 \text{ or } 560\ \text{kHz}$$

When FSK input (Pin 9) is low the frequency is equal to:

$$F_{space} = \frac{1}{R8A + R8B\ C3}$$

$$= \frac{1}{1\ K + 562\Omega.001\mu f} = 640\times10^3 \text{ or } 640\ \text{kHz}$$

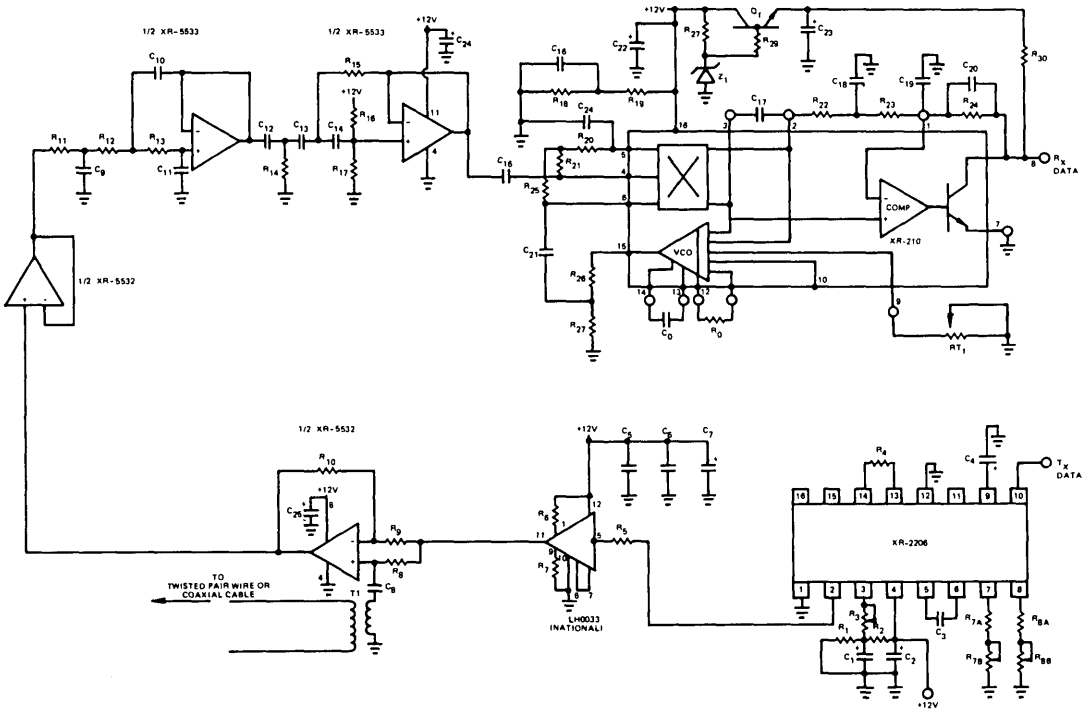


Figure 6. Complete Schematic for 100 Kilobaud FSK Modem

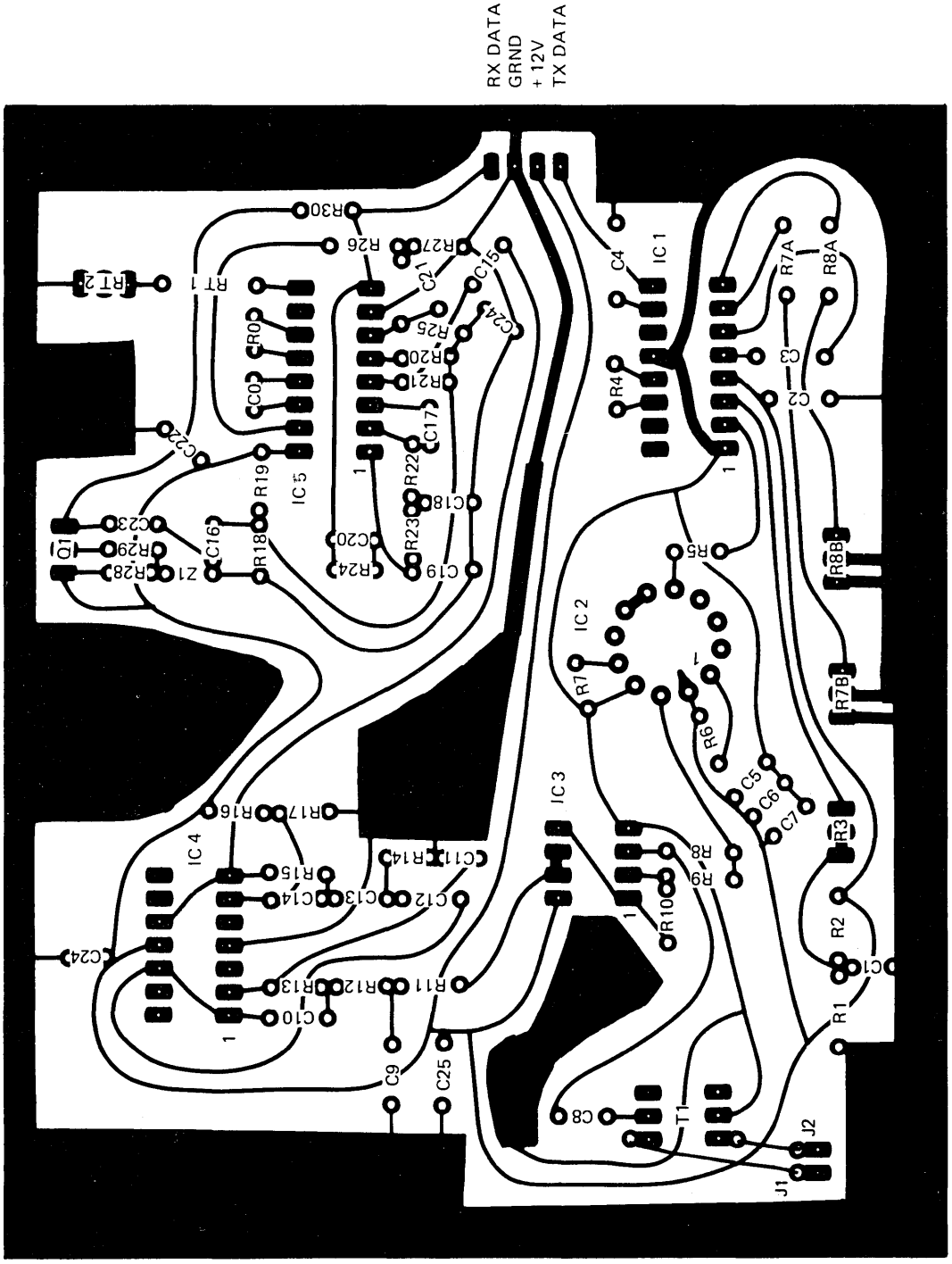


Figure 7. P.C. Board Layout for 100 Kilobaud FSK Modem–Component Side

PART NO.	ANSWER	ORIGINATE	PART NO.	ANSWER	ORIGINATE
R1-R2	5.1K	5.1K	C1	47 μf	47 μf
R3	50KΩ Pot	50KΩ Pot	C2	4.7 μf	4.7 μf
R4	200Ω	200Ω	C3	.001 μf	.001 μf
R5	51Ω	51Ω	C4	4.7 μf	4.7 μf
R6-R7	100Ω	100Ω	C5-C6	.1 μf	.1 μf
*R8	75Ω	75Ω	C7	4.7 μf	4.7 μf
R9-R10	10 KΩ	10 KΩ	C8	1 μf	1 μf
R11-R13	1 KΩ	1 KΩ	C9	738 pf	317 pf
R14	1.1 KΩ	228Ω	C10	1800 pf	807 pf
R15	450Ω	90Ω	C11	107 pf	46 pf
R16-R17	16 KΩ	3 KΩ	C12-C14	1000 pf	1000 pf
R18-R19	5 KΩ	5 KΩ	C15	.22 μf	.22 μf
R20	2 KΩ	2 KΩ	C16	1 μf	1 μf
R21	4 KΩ	4 KΩ	C17	300 pf	300 pf
R22	10 KΩ	10 KΩ	C18	150 pf	150 pf
R23	5 KΩ	5 KΩ	C19	106 pf	106 pf
R24	249 KΩ	249 KΩ	C20	10 pf	10 pf
R25	4 KΩ	4 KΩ	C21	.1 μf	.1 μf
R26	3 KΩ	3 KΩ	C22-C25	4.7 μf	4.7 μf
R27	10 KΩ	10 KΩ	Q1	2N2222A	2N2222A
R28	5 KΩ	5 KΩ	T1	PE-5760**	PE-5760**
R29	562Ω	562Ω	Z1	1N5232	1N5232
R30	1.3 KΩ	1.3 KΩ	IC 1	XR-2206	XR-2206
RO	2.4 KΩ	7.4 KΩ	IC 2	LH0033†	LH0033†
RT2	1 KΩ Pot	1 KΩ Pot	IC 3	XR-5532	XR-5532
R7A	1.4 KΩ	562Ω	IC 4	XR-5533	XR-5533
R7B	1 KΩ Pot	1 KΩ Pot	IC 5	XR-210	XR-210
R8A	750Ω	3.3 KΩ	*150Ω		
R8B	1 KΩ Pot	1 KΩ Pot	J1-J2	JUMPER	JUMPER
RT1	50Ω	100Ω		WIRE	WIRE

*Twisted Pair Wire
**Pulse Engineering
‡National

Figure 8. Component List for 100 Kilobaud FSIC Modem

High-Frequency TTL Compatible Output from the XR-215 Monolithic PLL Circuit

INTRODUCTION

With digital circuitry as common as it is, it is necessary to be able to interface analog signals to digital systems. This can be done by using the XR-215, a monolithic PLL circuit, and an additional buffer circuit.

When an input signal is present within the capture range of the PLL system, the XR-215 will lock on the input signal and the VCO section of the PLL will synchronize with the input frequency. The VCO output can then be buffered in order to produce a TTL compatible output.

PRINCIPLES OF OPERATION

Figure 1 shows a functional block diagram of the XR-215 monolithic PLL system. The circuit contains a phase comparator, a voltage controlled oscillator (VCO), and an operational amplifier. A complete phase locked loop system can be made by simple ac coupling the VCO output to either of the phase comparator inputs, and by adding a low pass filter to the phase comparator outputs.

The VCO output can be buffered in order to produce a TTL compatible output at high frequencies by the simple common emitter circuit shown in Figure 2. The amplitude of VCO degrades as frequency increases and at 21 MHz, the amplitude is reduced from approximately 2.5 Vpp to 400 mVpp. The dc output level is 2 volts below V_{CC} so with V_{CC} equal to ±5 volts, the dc level is approximately 3 volts. The VCO output is ac coupled in order to block this dc level. The input signal causes Q_1 to be overdriven, where the amplitude is 400 mVpp offsetted at approximately 0.769 Vdc. When Q_1 is in the offstate, the collector voltage will be forced high and when this voltage exceeds 0.7 Vdc, Q_2 will turn on and the collector of Q_1 will be clamped at 0.7 Vdc. The output of the VCO at the TTL buffered output will be in phase.

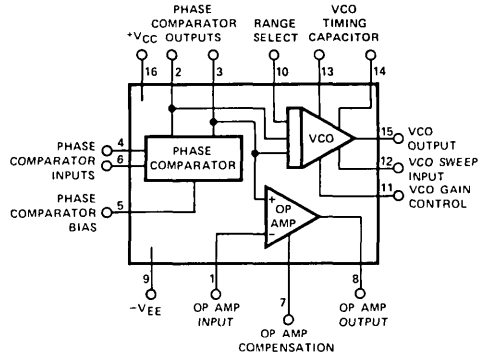


Figure 1. Functional Block Diagram of XR-215 Monolithic PLL Circuit.

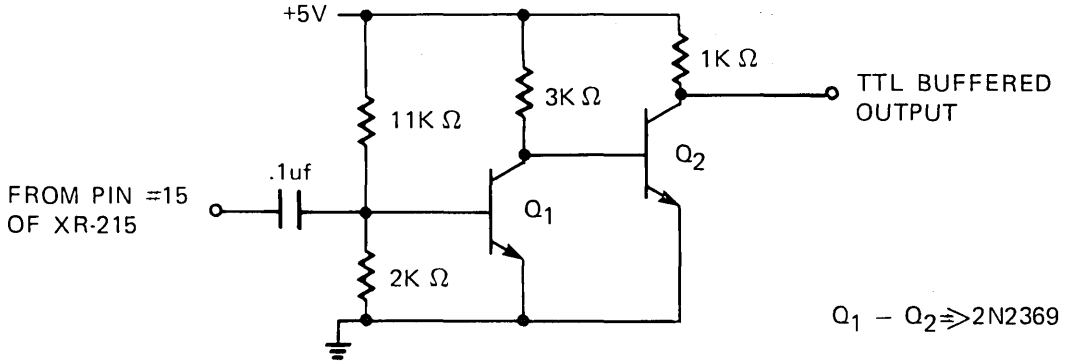
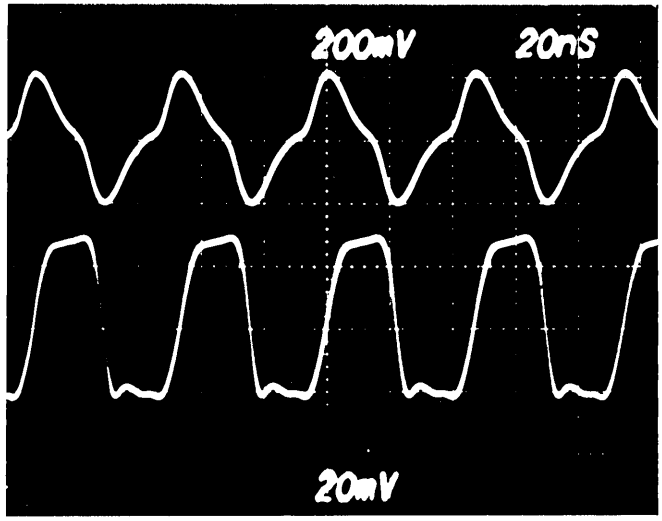


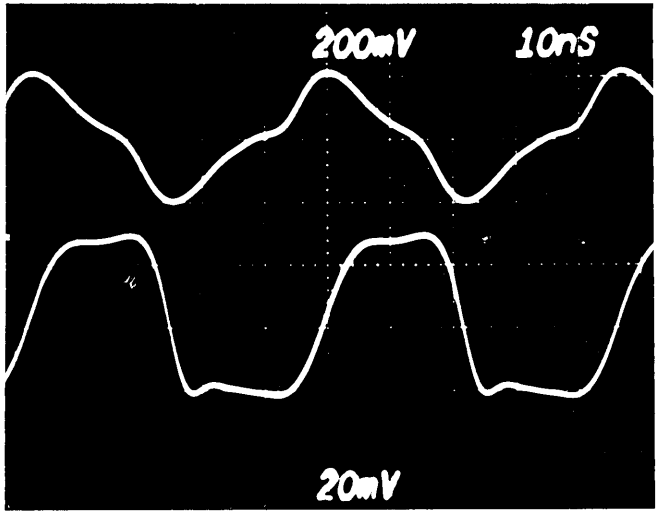
Figure 2. Common Emitter Buffer Circuit.

AN-27



VCO OUTPUT (PIN 15)
OF XR-215

TTL BUFFERED OUTPUT
AT 21 MHz MEASURED
WITH X100 PROBE.



PROPAGATION DELAY IS
APPROXIMATELY 5 ns

HIGH FREQUENCY SYNTHESIS

An application where a high frequency TTL compatible output would be useful is in high frequency synthesis, as shown in Figure 3. The output of the buffer, which can produce a high frequency TTL compatible output, is divided down the divider modulus N. When the entire system is synchronized to an input signal at frequency fs, the VCO output (pin 15) is at frequency Nfs, where N is the divider modulus. This is useful because a large number of discrete frequencies can be synthesized from a given reference frequency.

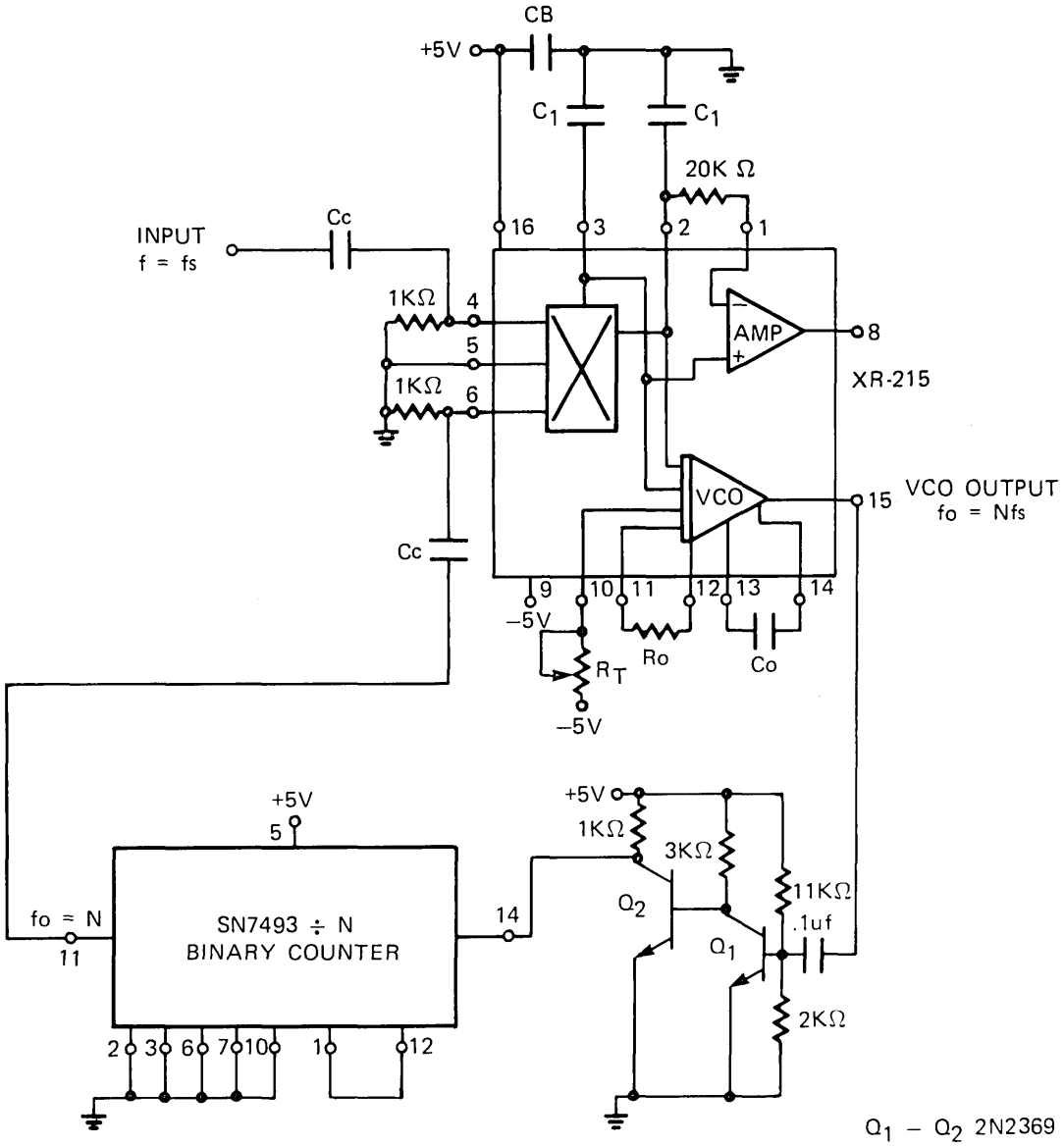


Figure 3. High Frequency Synthesis Circuit.

XR-212AS Modem System

INTRODUCTION

This application note describes a four-chip modem set designed to perform the complete Bell 212A type modem function. Described are the functions of each device, the connection of the four together, and testing procedures with performance data.

PRINCIPLES OF OPERATION

The basic characteristics of the 212A type modem are listed in Figure 1. As seen, this type of system is basically a dual modem. It can communicate with either low speed FSK modems (Bell 100 Series) or at 1200 BPS to PSK modems.

Figure 2 illustrates the major components of most modem systems. The four sections are:

1. **Modem Signal Processor (MSP):** This is the heart of the modem. It contains the modulator, demodulator, and filtering functions.

2. **Data Coupler:** This section in the 212A is a direct access arraignment (DAA). This type is directly connected to the switched telephone network. The DAA serves to protect the phone network from modem and vice versa.

3. **UART:** Performs serial to parallel conversion and timing functions.

4. **Handshaking Controls:** Timing functions for signals such as clear to send (CTS) and request to send (RTS).

The XR-212A consists of the following four devices which perform the complete MSP function.

XR-2120 PSK Modem Filter: This is a switched capacitor type filter for providing precise filtering and equalization for both 300 BPS FSK and 1200 BPS PSK carrier signals.

XR-2121 - PSK/FSK Modulator: Complete modulation functions are performed by this device for both 300 BPS FSK and 1200 BPS PSK.

XR-2122 - PSK/FSK Demodulator: Demodulation of FSK or PSK encoded carriers is performed by the XR-2122.

XR-2125 - Data Buffer: Performs asynchronous to synchronous and synchronous to asynchronous conversion.

MAJOR 212A TECHNICAL SPECIFICATIONS

DATA RATES:
- Low Speed Mode:
  - 0-300 BPS Asynchronous Format
- High Speed Mode:
  - 1200 BPS Character-Asynchronous Format
  - 1200 BPS Synchronous Format

ENCODING FORMATS:
- Low Speed Mode:
  - FSK (Frequency Shift Keying)
- High Speed Mode:
  - PSK (Phase Shift Keying)

OPERATING MODE:
- Full-Duplex at all Speeds

LINE REQUIREMENT:
- Two-Wire Switched Network

Figure 1. Major 212A Technical Specifications

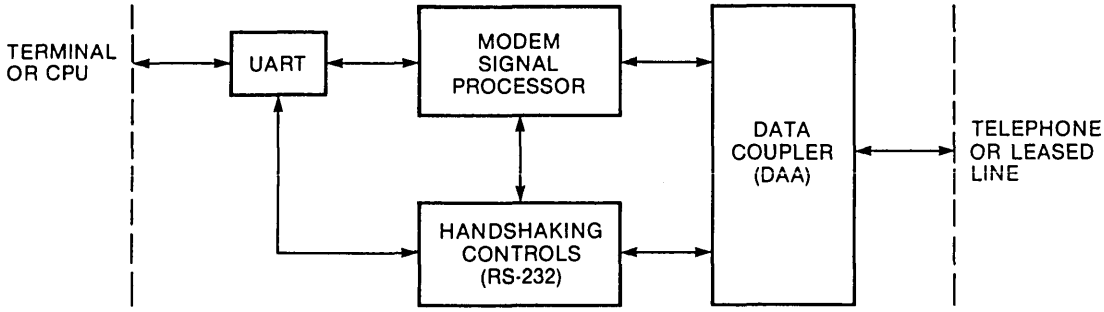


Figure 2. Modem Architecture

COMPLETE SYSTEM

Figure 3 is a simplified schematic intended to illustrate the complexity of the system.

Figure 5 illustrates the complete schematic diagram of the XR-212AS.

A performance test set-up is illustrated in Figure 4 The data error analyzers send a known data pattern and analyze whether this data was correctly received and demodulated. These analyzers give a quantitative number for errors received. On the line side of the modems there is a line simulator to introduce amplitude and group delay characteristics to the transmission channel as in an actual phone line. Most testing would include performance data for three different lines, C2 - nominal or normal line, C0 (3002) - worst case line, and back-to-back - no line. The XR-212AS is optimized for C2 line conditions (fixed compromise equalization in the XR-2120, however, it is important to know performance over other line conditions which may occur in an actual telephone link. The last piece in the test set-up is the line impairment simulator which can add impairments to the carrier signal which may exsist in the telephone channel. These impairments include noise and frequency offset.

The major specification often used to judge a modem's quality is its bit error rate (BER) as a function of interfering noise or signal to noise ratio (S/N).

Figures 6, 7, and 8 illustrate the typical BER vs. S/N performance for the XR-212AS operating at 1200 BPS for the three different line conditions. The data taken for these figures is under the following conditions:

R_{XC} = −40 dBM
T_{XC} = −10 dBM
511 Random Data Pattern

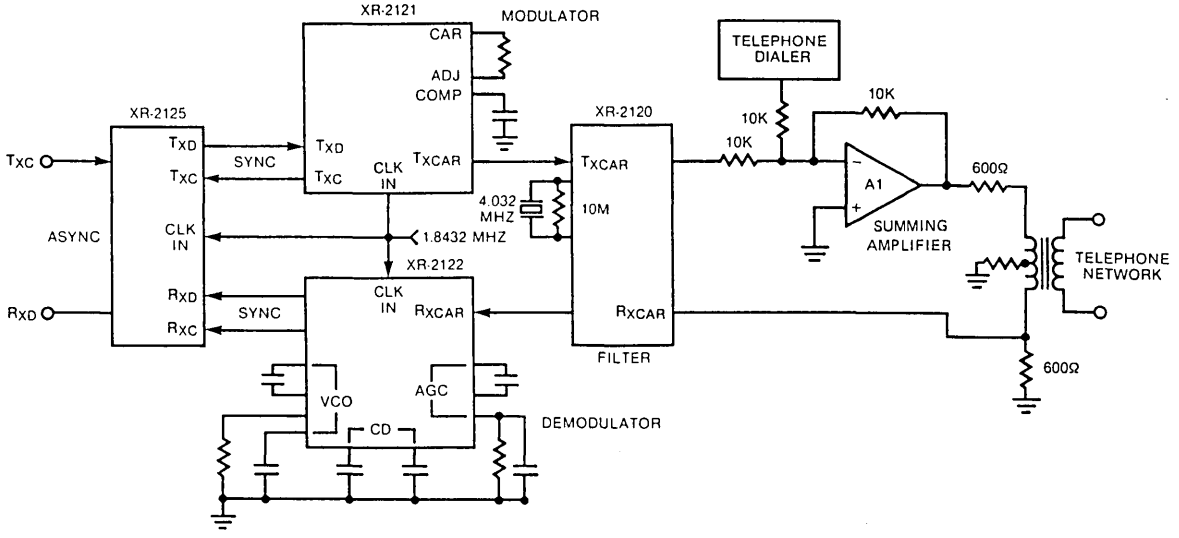


Figure 3. Complete Modem Signal Processor

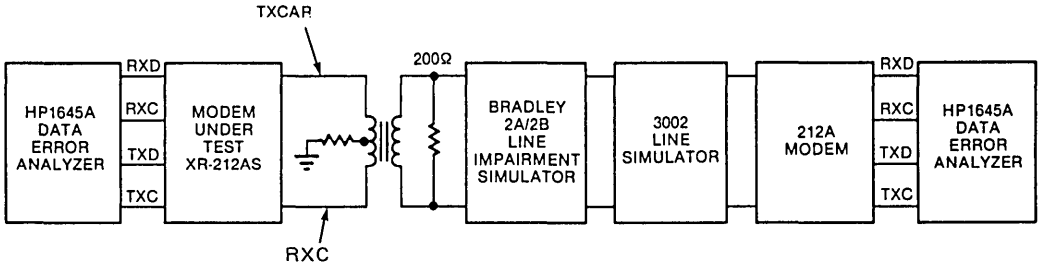


Figure 4. Performance Test Set-Up

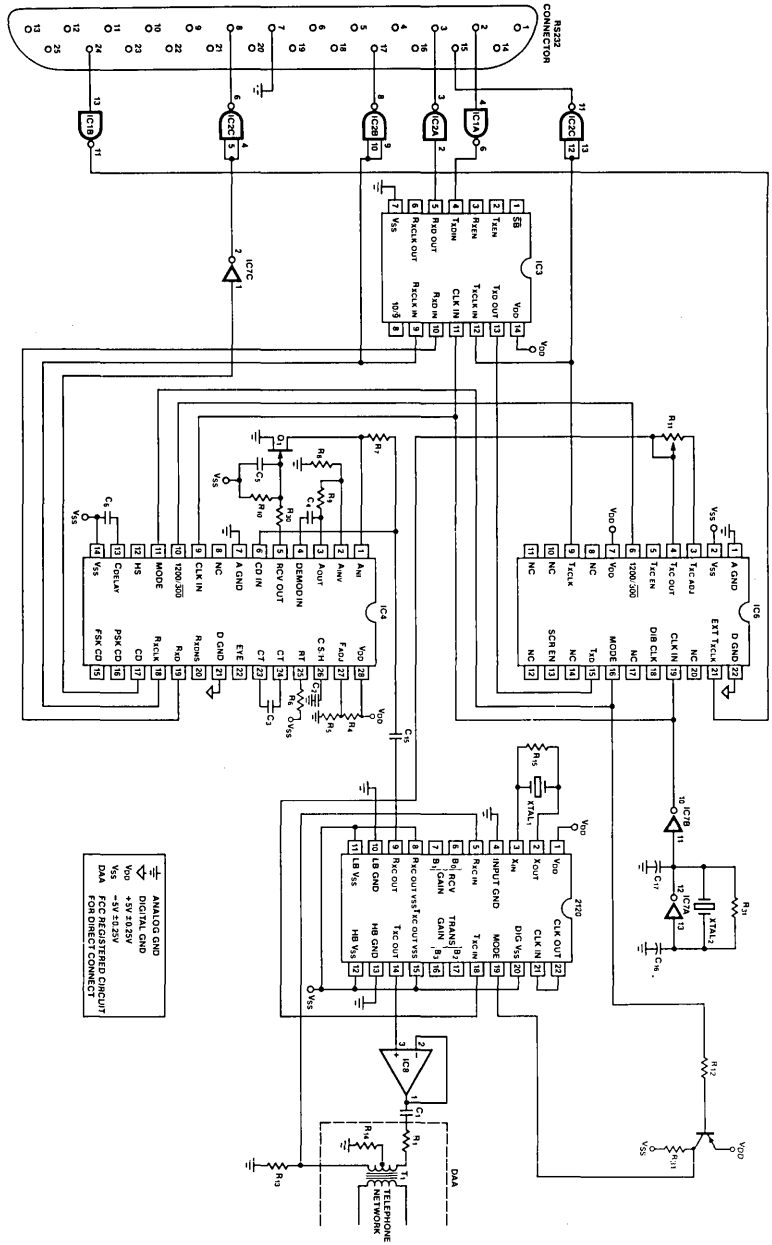


Figure 5. Complete 212AS Schematic

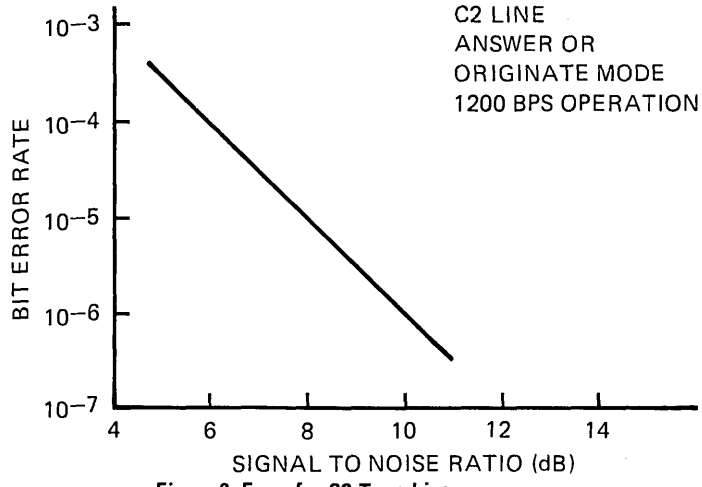


Figure 6. Error for C2 Type Line

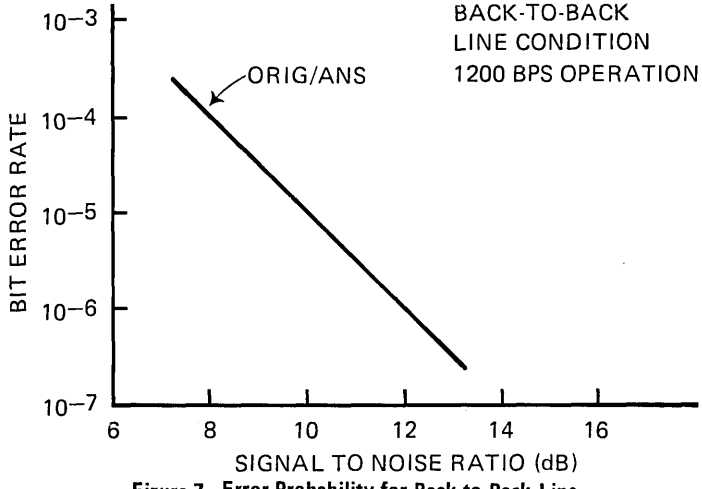


Figure 7. Error Probability for Back-to-Back Line

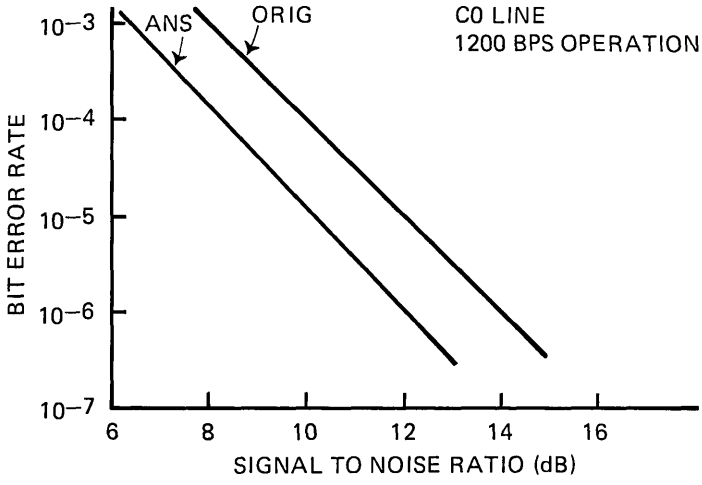


Figure 8. Error Probability for C0 Type Line

XR-212ACS Performance Testing

INTRODUCTION

The task of testing the performance of a modem is quite often at best a difficult one. To simulate in the laboratory, conditions that may exist on actual phone lines is not only difficult but requires special test equipment. However, to predict actual operating performance, this testing is necessary. This application note describes the test method and actual data on a 300 BPS/1200 BPS full duplex modem system.

The modem acts as the link between the digital, data side, and analog, line side, mediums as shown in Figure 1.

TEST INFORMATION

The performance or quality of the modem is measured by its' ability to send and receive data accurately. This is usually specified as its bit error rate (BER). The BER is specified as the number of errors for a given number of data bits received. For example, a BER of 1/10-5 states that one error may be seen for every 100,000 data bits received. The BER is usually given as a function of various impairments which may occur on the analog (phone) transmission medium.

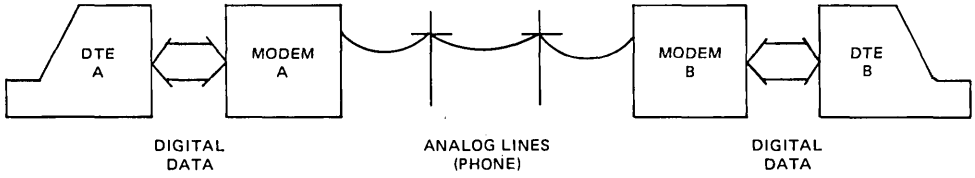


Figure 1. Modem Data Link

The testing here will be done for the following conditions:

1. BER versus signal to noise ratio (S/N). This test is the specification which best describes a modem's actual performance in operating environments. The modem's transmitted carrier, $T_{X\ car}$, and received carrier $R_{X\ car}$, are set to fixed levels while noise is added to the $R_{X\ car}$. Figure 2 illustrates such a condition.

   The data error analyzers are used to both send a predictable data pattern as well as verifying if it is received properly. It will count errors for a given number of data bits.

2. BER vs. $R_{X\ car}$ level. The $T_{X\ car}$ is set to a fixed level and the $R_{X\ car}$ level is decreased while BER is measured at various levels.

3. BER vs. frequency offset. Frequency offset represents a shift in the frequency of the $R_{X\ car}$ due to the analog medium. For example, an $R_{X\ car}$ may be received with a frequency of 1203 Hz although it was originally transmitted at 1200 Hz.

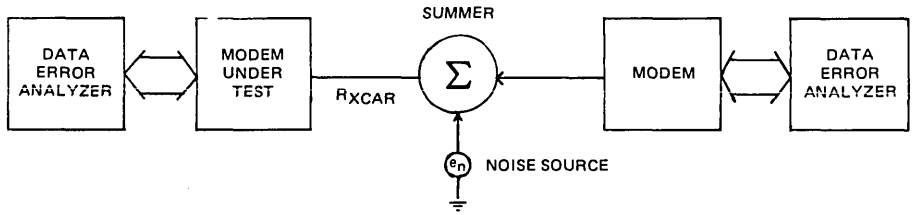


Figure 2. BER vs. S/N

Speakerphone Design using XR-T6420-1 and XR-T6421

INTRODUCTION

A general circuit, showing the major stages within the speakerphone, is shown in Figure 1. It consists of two audio channels (T_X and R_X), a control circuit, and a hybrid interface circuit. The gain of each audio channel is controlled by the control circuitry with the use of a voltage controlled amplifier (VCA). The inputs to the control circuit are obtained from each of the audio channels.

The hybrid interface circuit performs three important functions. First, it couples the T_X channel signal to the telephone line. Second, it couples the signal on the telephone line to the R_X channels. And, finally, it cancels a majority of the T_X signal that can couple into the R_X channel. The amount of T_X signal that appears on the R_X channel is called sidetone.

CIRCUIT OPERATION

Adjusting speakerphones for proper operation is a difficult task. There really are not any specifications for the system, except that during operation, the system must sound right—a highly subjective requirement.

The method used in designing the speakerphone was to first adjust the gain for each audio path separately with the VCA set to maximum gain. After the levels have been set, then the frequency response can be adjusted to the designer's requirements.

The next step is to determine the operating point of the VCAs. For the system described here, it was decided to have the sum of the attenuations introduced by both VCAs to be equal to -50 dB, and the idle state for each VCA to be -25 dB. The idle state is the condition where the control logic has not determined which channel should be on and has placed the system in a wait state with both channels partially on until a decision has been made.

The "gain" of the control voltage (IC1 and IC2 in Figure 3) amp can be calculated because both the input and output voltage swings are known. The input swing is the control voltage output from the control circuit XR-T6421, pin 1. The output swing can then be determined using the control voltage versus gain for the VCAs from the data sheet for XR-T6420-1.

The control voltages for the VCAs in the idle state is then adjusted by the addition of a resistance to the inverting input (R_{VCTX} and R_{VCRX}, Figure 3).

The attack and release time constants for the VCAs are then determined. The release time constant which is defined as the time for the VCAs to switch from ON to IDLE state (can be 2-3 seconds) is set by the parallel resistance of the two control voltage amplifier input resistances and a capacitor.

Once the capacitor is selected, the attack time is calulated. This is normally fast to prevent missing the first part of the signal. This is determined by the RC product of the previously selected capacitor and the series resistor from the capacitor to pin 1 of the control circuit. The output impedance of the control circuit is low for both the T_X and R_X state, and is high impedance for the idle state.

The final step in the design procedure is to adjust the four rectifiers in the control circuitry. The effect of the noise circuitry can be disabled by connecting pin 6 to V_{REF}, pin 18, or by increasing the RC time constant on pin 6. Since both channels must be functional for this adjustment, there will be interaction between the rectifiers during adjustment. This is where understanding the system to determine which rectifier is causing the problem is helpful. This can be a long and tedious process because the system must work for a variety of line conditions as well as for different people using the system.

RESULTS

The finalized schematic for the system is shown in Figure 4. The frequency response and gain for both channels are plotted in Figure 2. Figure 3 is the component stuffing diagram.

SET-UP PROCEDURES

Step 1 — Preliminary Set-Up

Connect the junction of C1 and R1 to ground. Adjust R2 to make the voltage on Pin 9 of the XR-T6420-1 between +80 and +90 mV. Adjust R3 to make the voltage on Pin 19 of the XR-T6420-1 between -80 and -90 mV.

Step 2 — Transmit Channel Adjustments

Connect the junction of C1 and R1 to V_{CC}. Adjust R4 and R5 to obtain proper levels on the telephone line according to system requirements. Normal gains for the microphone amplifier are in the range of +35 to +45 dB. The frequency response of the transmit channel can be adjusted at this time.

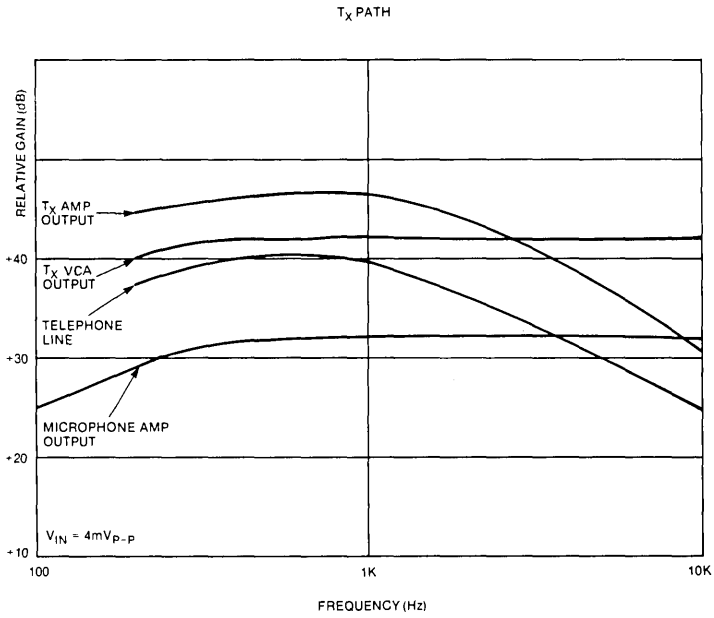


Figure 2. Frequency Response and Gain

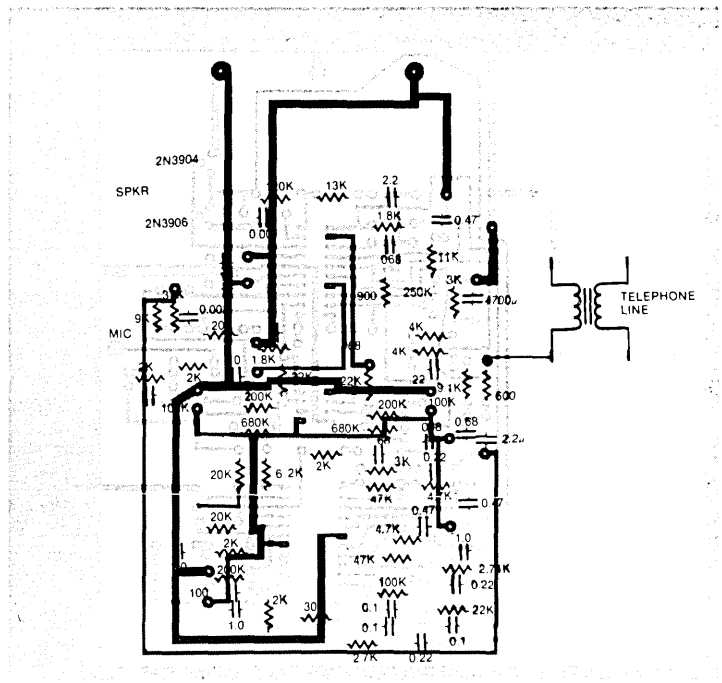


Figure 3. Component Stuffing Diagram

PCM Line Interface

INTRODUCTION

The XR-T5680 is a Monolithic PCM Transceiver. It is designed primarily for short line (<10 dB) PCM transmission applications such as in digital Private Branch Exchange (PBX) environment, Digital Multiplexed Interface (DMI) and standard PCM data interface circuits. The maximum frequency of operation is 10 MBits/s so it covers T1, T1C, T2 and Europe's CEPT 2048K and 8448K Bits/s data rates. The device is packaged in a hermetic 18 Pin CERDIP and is designed such that there is no phase difference between the extracted clock and data outputs at the receiver.

PRINCIPLES OF OPERATION

Figure 1 contains a Functional Block Diagram of the XR-T5680. The circuit consists of two separate sections: one is the line receiver, and the other is the line transmitter. The receiver accepts incoming bipolar signals and converts them into TTL D+ and D– data streams. It also produces a clock output from the input data. In the transmit direction, full width, TTL compatible D+ and D– signals at the inputs and a 50% duty cycle clock are combined to form the bipolar line signal at the outputs of a transformer. The power supplies for the two sections of the circuit are internally isolated to avoid crosstalk problems.

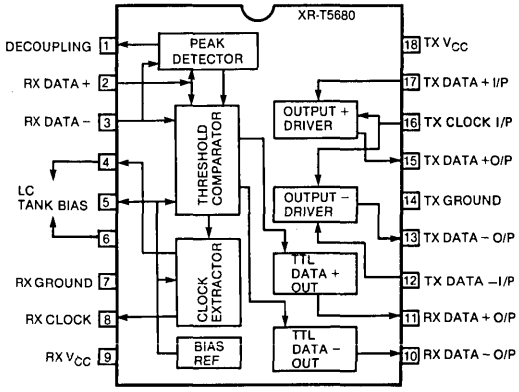


Figure 1. Functional Block Diagram

Receiver Circuit Description:

The receiver is designed to handle a maximum of 10 dB line attenuation. This condition allows the design to adopt a relatively simple approach as compared with long transmission line receivers which usually require ALBO circuits and equalization networks to function properly.

The successful operation of this receiver relies on the peak detector which converts the incoming signal amplitude into a DC variable threshold. The variable threshold is arranged to slice the input signal at half amplitude point at the data comparator (see Figure 3), so that D+ and D– data can be accurately extracted under the worst expected condition. It also ensures a nominal ouput pulse width change at different input signal levels. The D+ and D– data both go through similar level shifting circuits to be converted into TTL compatible output signals.

Clock Extraction and Timing:

Since the input spectrum does not carry any frequency components around the transmission rate, input waveform is full wave rectified and applied to an external L-C resonant circuit for clock extraction. The amplitude modulated sine wave at the resonant circuit is coupled through a capacitor to a zero crossing detector before applied to the input of a ECL/TTL converter as shown in Figure 2.

To convert the half-width data at the receiver outputs into full width signals for digital processing, it is common practice to use positive edge triggered D/FFs. This requires the mid-point of the data to be aligned with the rising edge of the clock so that no error will result should the data be jittered with a max. amplitude of ±0.25 UI relative to the clock (see Figure 5). The disadvantage of this scheme is additional hardware is needed to ensure that the two signals have the correct timing relationship. It is possible by means of an alternative retiming circuit as shown in Figure 6 to perform the same function while still keeping the data and the clock in the same phase. This circuit has twice the jitter tolerance under the same condition as compared with a single D-type counterpart and is recommended to be used with the XR-T5680. It is anticipated that no glitches due to crosstalk, etc., should exist at the receiver data output terminals under the intended short line applications.

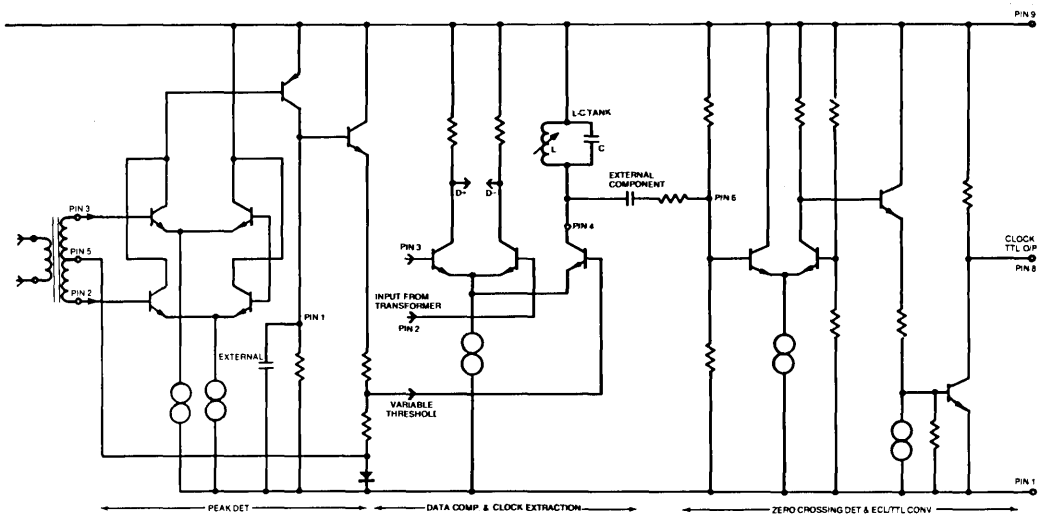
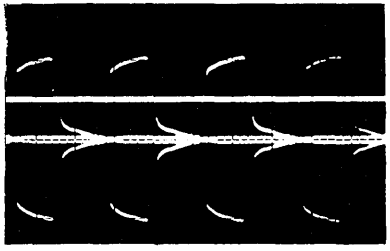
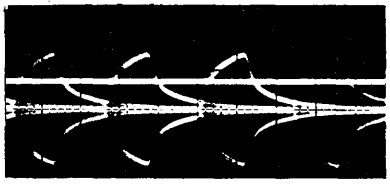


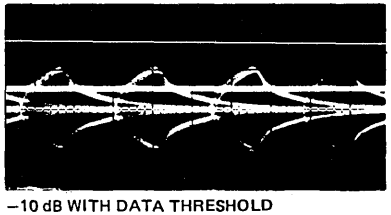
Figure 2. Simplified Circuit of XR-T5680 Receiver



–3 dB VERT = 1V/CM
HORZ = 200 nS/CM

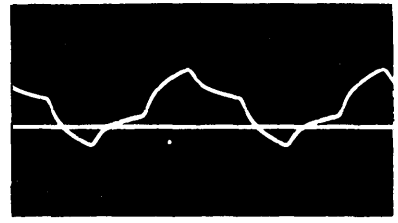


–6 dB WITH DATA THRESHOLD

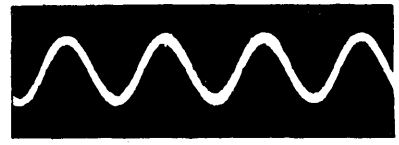


–10 dB WITH DATA THRESHOLD

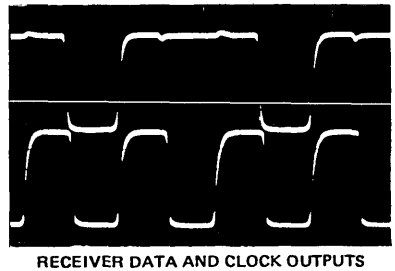
Figure 3. Typical Eye Pattern Obtained at Pin 2 or 3 for Coaxial Cable at Various Line Length. Bit Rate = 2048 KBits/S



–10 dB (1-1-1 Pattern) WITH DATA THRESHOLD



TANK CIRCUIT WAVEFORM AT PIN 4



RECEIVER DATA AND CLOCK OUTPUTS

Figure 4. Timing Diagram of Circuit Waveforms for a 1-1-1 Input Data Pattern

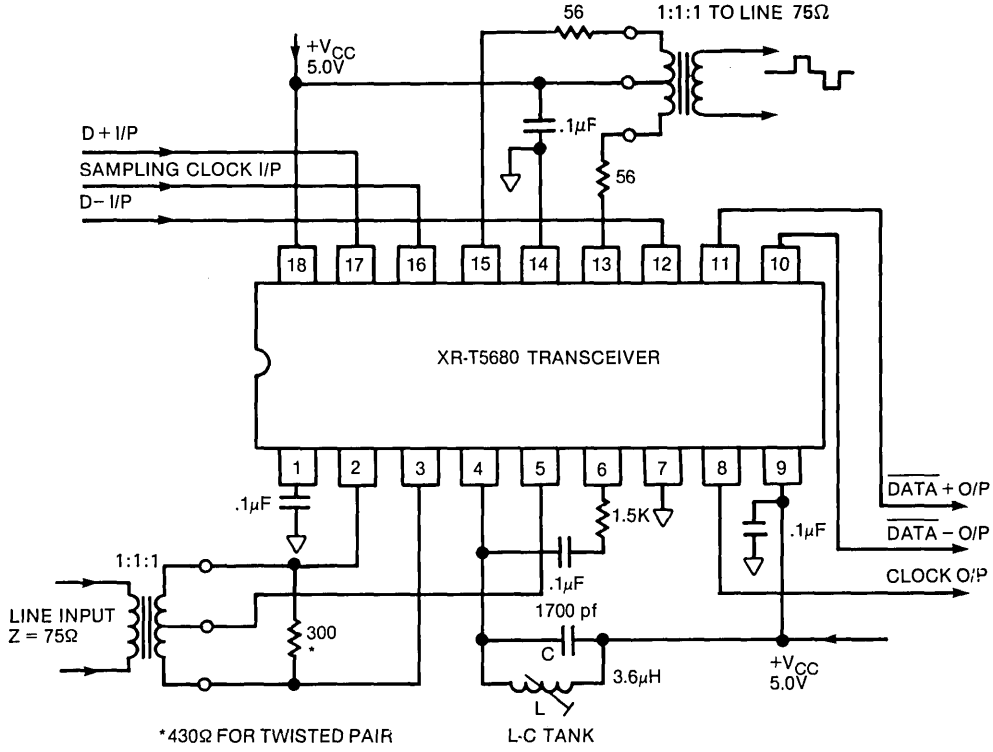


Figure 8. A Recommended Circuit Diagram Connection For 2048K Bits/s Line Interface Application

ELECTRICAL CHARACTERISTICS

Test Conditions: $+V_{CC}$ = 5.0 V, operating temperature 0°C to +70°C.

PARAMETERS	PIN NO.	MIN	TYP	MAX	UNITS	CONDITIONS
DC Supply	14	4.75	5.0	5.25	V	
Supply Current	9,14		35.0	45.0	mA	Transmitter Drivers Open
Tank Drive Current	9	1.7	2.0	2.3	mA	Pin 8 & 11 = 0 V, Supply 3.0 V to Pin 6
Clock Output Low	13		0.3	0.8	V	I_{OL} =1.0 mA
Clock Output High	13	3.0	4.3		V	I_{OH}= −400μA
D+, D− Output Low	12,10		0.4	0.8	V	I_{OL} = 1.0 mA
D+, D− Output High	12,10	3.0	4.5		V	I_{OH} = 400μA
Driver Low Voltage	17,18	0.6		0.05	V	I_{OL} = 40 mA
Driver Sinking Current	17,18			40	mA	V_{OL} = 0.95 V
Driver Output Rise Time	17,18		20	30	nS	With 150Ω Pull-Up to +5.0 V, CL = 15 pF
Driver Output Fall Time	17,18		20		nS	With 150Ω Pull-up to +5.0 V, CL = 15 pF
Pulse Width at 2048K	17,18	219	244	269	nS	With 150Ω Pull-Up to +5.0 V
Pulse Width Imbalance at 2048K	17,18		5	10	nS	At 50%
Clock Duty Cycle at 2048K	13	40	50	60	nS	%
Clock Rise Time	13		25		nS	10-90%

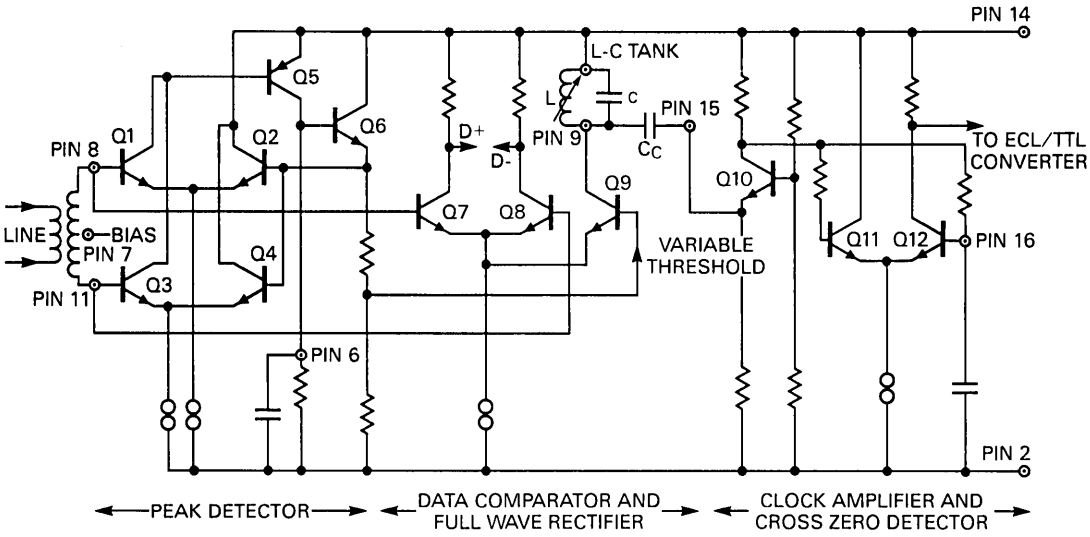


Figure 4. Simplified Schematic of XR-T5681 Receiver

TRANSMITTER

The transmitter consists of two identical TTL input open collector NAND gates. The output driver has a nonsaturating stage and can handle a maximum current of 40 mA. If the inputs are half width signals, Pin 5 should be returned to $+V_{CC}$ via a 1KΩ resistor. If the input data are full width signals, a synchronized 50% duty cycle TTL clock is needed at Pin 5 to obtain a bipolar signal at the output of a center tapped transformer (See Figure 5). The output pulse conforms to CCITT G.703 recommendation. A circuit connection diagram for 1.5Mb/s line interface is shown in Figure 6.

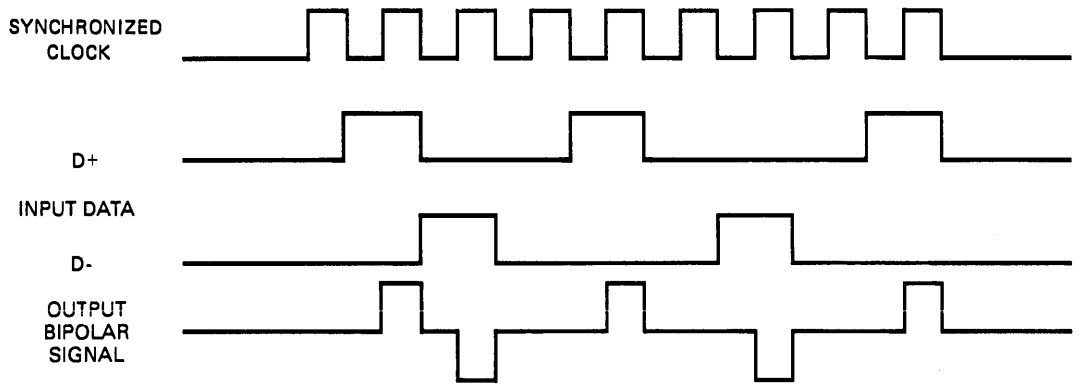


Figure 5. XR-T5681 Transmitter Section Timing Diagram

Implement Bell T1C PCM repeater using just two ICs

Because T-carrier lines will be an essential part of tomorrow's data-communication networks, it's imperative that you learn how to interface your communication systems with these lines. Two ICs let you implement a T1C repeater that contains all the circuitry necessary for pulse-code-modulation (PCM) transmission.

M Kursat Kimyacioglu, *Exar Corp*

Once the exclusive province of a select community of telephony engineers, the techniques involved in Bell T1C transmission and repeaters are now required knowledge for anyone transmitting data along twisted-pair cables. You can use two ICs to implement—economically—a T1C repeater that includes all the active circuit functions necessary to accommodate pulse-code-modulation (PCM) transmission.

Repeaters are essential for PCM transmission over more than 6000 ft of cable. When a pulse travels along a cable, it gets distorted in shape, dispersed in time, and subjected to crosstalk and random noise. By repeating the signals at frequent intervals, a repeater constructs an accurate reproduction of the original digital pulse train. Typically, you insert repeaters in twisted-pair lines at approximately 6000-ft (1.8 km) intervals.

The function of a repeater can be summarized as reshaping, regenerating, and retiming ("the three Rs").

- *Reshaping* means to restore a pulse to its original width (but not necessarily to its original shape). It's essential that a pulse be reshaped so it won't spill over into an adjoining time slot and interfere with the detection process.
- *Regenerating* means deciding whether each arriving signal is a zero or a one. To make this logical decision, the repeater adjusts the decision threshold of its comparator circuit to the middle of the pulse amplitude.
- *Retiming* means synchronizing clock signals. To retime, the repeater must extract the clock signal from this incoming pulse train by sampling the comparator output. It must sample the output at a rate that ensures it will recover with a minimum number of errors, so the signals the repeater transmits will have correct spacing, pulse width, and rise and fall times.

T1C systems must accommodate the same transmission distances between repeaters as T1 systems do—a nominal maximum of 6300 ft over 22-gauge pulp- or plastic-insulated cable. As a result, the repeaters for

TABLE 1—LINE REQUIREMENTS FOR T1 AND T1C SYSTEMS

PARAMETER	REQUIREMENT	
	T1	T1C
SYSTEM TYPE	REGENERATIVE BASEBAND, DIGITAL	REGENERATIVE BASEBAND, DIGITAL
MEDIA	TWISTED-PAIR CABLE	TWISTED-PAIR CABLE
TRANSMISSION RATE	1.544M BPS (24 DIGITIZED VOICE CIRCUITS)	3.152M BPS (48 DIGITIZED VOICE CIRCUITS)
RECOMMENDED RANGE	50 REGENERATIVE SECTIONS (90 km)	50 REGENERATIVE SECTIONS (90 km)
PAIR LOSS	7 TO 35 dB	9 TO 54 dB
REPEATER/REGENERATOR	AMI-BIPOLAR, AUTOMATIC-LINE-BUILD-OUT, SELF-TIMED CIRCUIT	AMI-BIPOLAR, AUTOMATIC-LINE-BUILD-OUT, SELF-TIMED CIRCUIT
MAXIMUM NUMBER OF NO-PULSE SYMBOL INTERVALS	15	132
TIMING CIRCUIT Q FACTOR	LOW Q 50 TO 100	HIGH Q > 1000
REPEATER SPACING	6300 FT MAX WITH 22-GAUGE COPPER PULP-INSULATED CABLE	6300 FT MAX WITH 22-GAUGE COPPER PULP-INSULATED CABLE
FAULT DETECTION	BIPOLAR VIOLATION AND TRIO-PULSE FAULT-LOCATION CONFIGURATION	BIPOLAR VIOLATION AND TRIO-PULSE FAULT-LOCATION CONFIGURATION
LINE CURRENT	60 mA	60 mA

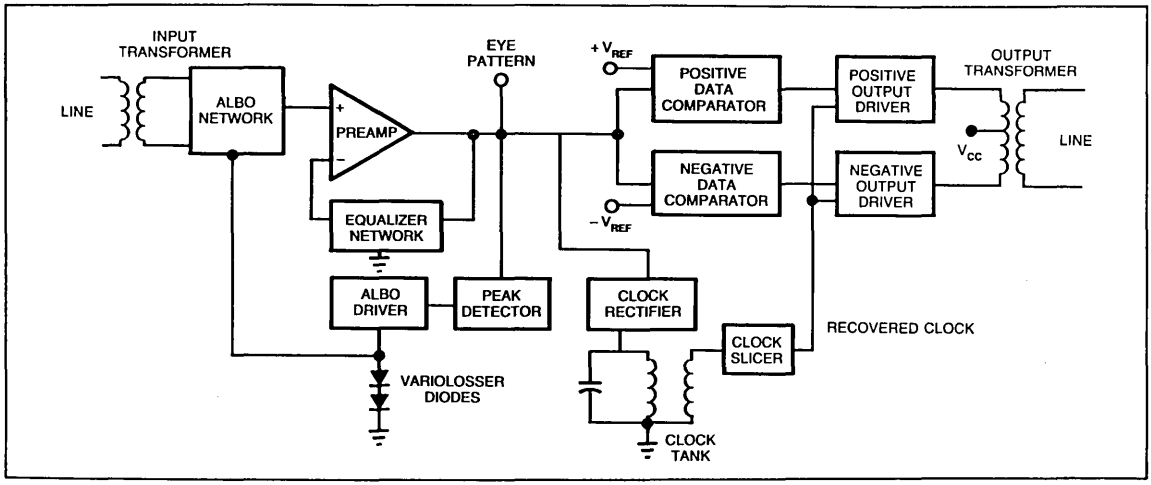


Fig 1—To provide automatic gain control, an Albo (automatic line-build-out) network usually precedes the repeater's preamp.

line-voltage drop within preset limits.

The transmission requirements for T1 and T1C repeater designs are approximately the same. However, the T1C line loss may be as high as 54 dB. In addition, T1C's higher transmission rate makes it more susceptible to performance degradations induced by variations between the cables in an installed system. Thus, T1C is much harder to implement than T1 is.

A T1C system, which consists of two multiplexed T1 channels, has a bit rate of 3.152M bps. This figure is slightly more than twice the T1 rate since synchronization and control bits have been added to the stream. Now, the power output's spectral density peaks at 1.576 MHz. In a T1C system, you can't approximate the line-loss characteristics with a single pole—you'll need at least two poles and maybe three.

Remember that transmission-cable characteristics are frequency dependent. Theoretically, the equalization process establishes the exact inverse of the cable characteristics to reshape transmitted pulses. In practice, however, equalization almost exactly compensates cable loss vs frequency characteristics, but it only partially corrects phase distortion.

In existing systems, cable lengths are governed by the distance between repeaters, while cable characteristics vary according to temperature and humidity conditions. Because of these factors, the repeater must have a variable-slope transfer function that will match any cable length and also respond continually to changing environmental conditions.

Realizing a repeater

As **Fig 1** illustrates, an automatic-line-build-out (Albo) network usually precedes the preamp. In addi-

The repeater must have a variable-slope transfer function that responds continually to changing environmental conditions.

line code for PCM transmission. When you use AMI, you transmit successive ones in opposite (bipolar) directions. AMI also offers a means of detecting single-bit errors.

The circuit in **Fig 1** employs a full-wave rectifier to extract the network clock signal; it rectifies the equalized signal at about 50% of its peak value and drives a tank circuit with this signal. The rectifier's clipping level changes the amplitude and phase of the recovered clock. This scheme is susceptible to variations in pulse amplitude and density, so it results in timing jitter, most of which is caused by mistiming in the clock extraction circuit. When there are no marks on the line, the recovered clock will drift toward the self-oscillating frequency of the tuned circuit. A new mark will return the clock to the data-repetition rate. The jitter will be dependent upon the degree of mistuning and the spectral density of the data signal. Local noise and crosstalk will also affect the jitter.

In practice, when both high-Q and low-Q clock-extraction techniques are employed, high-Q techniques result in more accurate extraction. You can implement high-Q extraction circuits using passive quartz crystal filters or crystal-controlled phase-locked loops. For low-Q circuits, you can get by with conventional RLC tuned circuits.

An equalized signal is applied to a pair of comparators to detect positive and negative pulses. Two data-latch circuits store the detected pulses on the positive-going edge of the clock. Data-latch outputs and the clock signal are then gated and amplified to produce regenerated and retimed pulses for transmission over the next 6000 ft of cable.

The complete T1C repeater design is shown in **Fig 3.** The bipolar PCM signal, attenuated and distorted by the transmission medium, is applied through a pulse-shaping network to a preamp. This network, along with variolosser diodes, forms the Albo circuit, which pro-

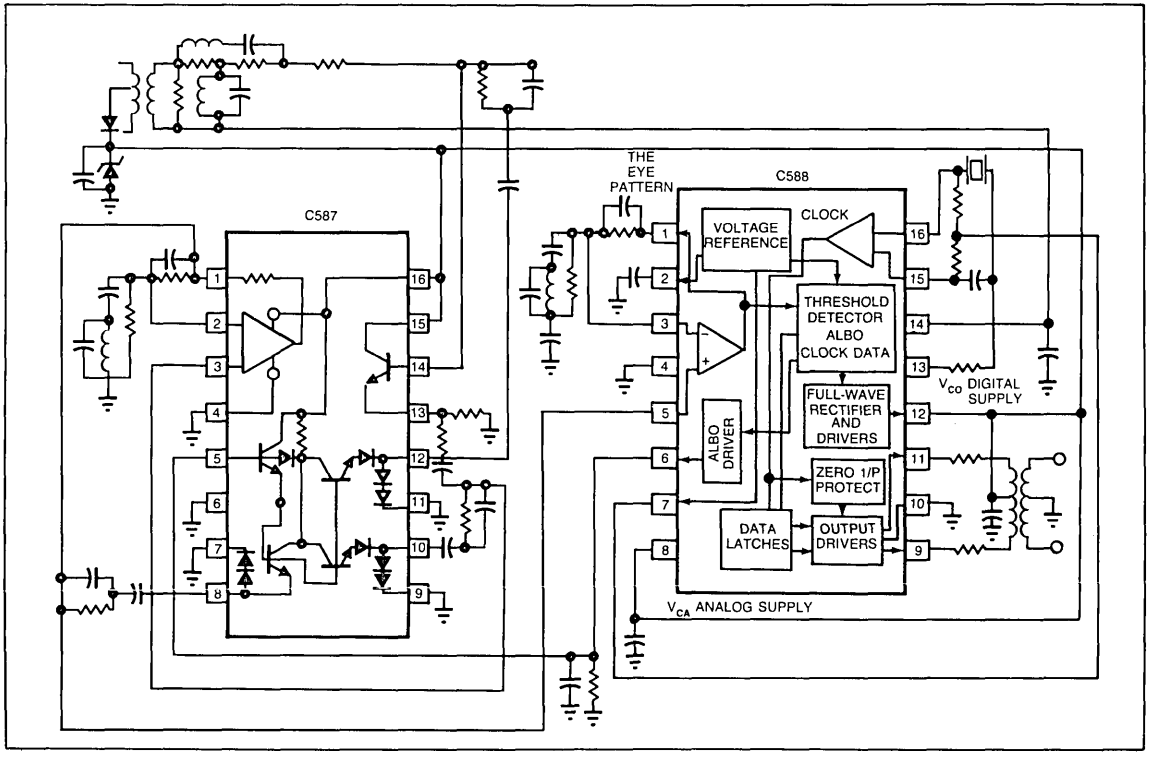


Fig 3—The Albo network automatically adjusts *for varying cable characteristics. The network comprises the variolosser diodes and the pulse-shaping network/preamp.*

EXAR'S COMMITMENT TO QUALITY AND RELIABILITY

First the terms Quality and Reliability must be defined.

Quality is conformance to requirements, i.e., meets specification requirements, adheres to procedure, etc. Quality must be measurable, thus it must be defined in measurable terms. Quality is measurable in many ways, a common one being Average Outgoing Quality Level (AOQL) generally stated in Parts Per Million (PPM).

Reliability is length of time product conforms. This is also a measurable quantity and is generally expressed as Mean Time Between Failures (MTBF) or Failures in Time (FIT). The relationship between MTBF (or failure rate) and time is illustrated in the bathtub curve.

EXAR is committed to achieving high levels of Quality and Reliability. To achieve this goal, we design and build quality and reliability into all our products. Each EXAR employee is committed to assuring this goal by diligent adherence to the quality first concept.

EXAR continuously monitors the Quality and Reliability levels of its products via AOQL sampling plans and periodic reliability testing programs. Monitoring alone is not sufficient. At EXAR any reject discovered at the monitoring level is scrutinized by extensive failure analysis and corrective action taken to prevent recurrence.

Reliability, primarily a function of device design, fabrication, and assembly methods and materials, cannot be tested into ICs. However, EXAR proposes combinations of specific environmental tests designed to accelerate failures of marginal devices, thereby eliminating early life failures. By choosing the desired combination of environmental tests, you can choose the reliability level that fits your need.

Benefits Every Step of the Way

Devices that undergo the specifically designed environmental tests begin paying dividends the moment you receive them and continue doing so for the life of the system.

Your circuit board testing is also reduced along with your test equipment costs. Since more of the components on a board are higher quality, the quality of the entire board is better.

There is less board rework for the same reason.

Even traditional burn-in can be reduced substantially, improving the flow of work in process.

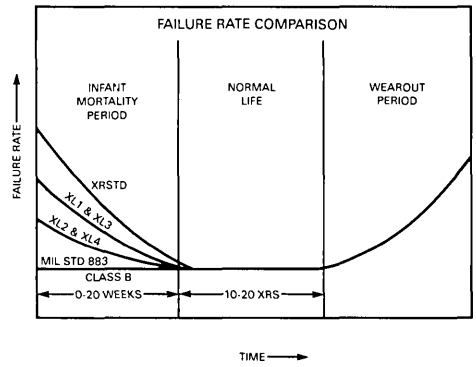
Finally, performance in the field is improved. Fewer field failures result in fewer service problems and, more important, fewer dissatisfied customers.

A Modest Investment

EXAR's Standard and Excel™ screening methods are virtually identical to those used in compliance with military specifications.

Yet, because there is no extensive military documentation involved, EXAR can pass these savings on to you.

The result is that you receive almost mil-grade parts at lower prices.



EXAR's Reliability Program Summary

EXAR's reliability program is designed for the evaluation of high-density complex integrated circuits which require greater attention than simple conventional reliability tests. EXAR believes in producing excellent reliability (XR) by building the quality and reliability into the products. Once raw silicon is transferred to a complex integrated circuit, through quality conscious people, it needs to satisfy the increasingly stringent requirement of the QA Reliability Department to ensure that the products demonstrate the acceptable level of quality and reliability.

Reliability Testing

Reliability is defined as "the probability of an item to perform a required function under stated conditions for a stated period of time." EXAR performs the reliability testing on a sample of 100 pieces and the flow being used is detailed in Table 1. There are monitoring programs at EXAR to assure high product reliability.

Based on the data available from reliability experiments, MTBF, and failure rate are computed using the Arrhenius equation. Results of recently completed reliability experiments are summarized in Table 2.

*QUALIFICATION & QUALITY CONFORMANCE PROCEDURES

Screen	Mil-Std, Method 5005, Class B Test Conditions	Requirement
Group A	Final electrical repeated on sampling basis (sub group 1 thru 11)	Each sublot sampling basis.
Group B	Package construction & function related tests (dimensions, resistance to solvent, solderability, int. visual, bond strength, seal & EDS)	Each sublot sampling basis except subgroup 6. Subgroup 8 only for initial qualification.
Group C	Die related tests (life test, temp cycling, const. acceleration & seal tests)	Performed every 3 month interval for each micro circuit group.
Group D	Package related tests (dimensions, lead integrity, seal tests, thermal shock, temp. cycle, moisture test, mechanical shock, vibration, const. acceleration & salt atmosphere)	Performed every 6 month interval for each package type.

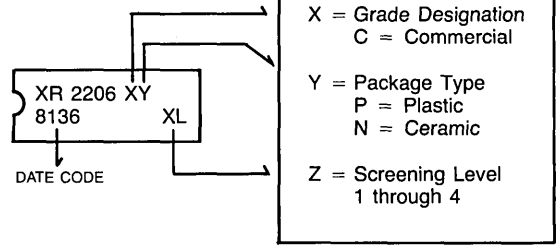
EXAR'S EXCEL™ PROGRAM

SCREENING	PLASTIC (P)		CERAMIC (N)		COMMENTS
	XL[1]	XL[2]	XL[3]	XL[4]	
Pre cap. Internal Visual	QCI 2006	Method 2010	QCI 2004	Method 2010 Cond. B	100%
Sta. Bake	6 hrs @ 175°C	6 hrs @ 175°C	6 hrs @ 175°C	6 hrs @ 175°C	100%
Temp. Cycling			−65°C to +150°C	−65°C to +150°C	10 Cycles 100%
Const. Accel.			30,000 gm Y_1 axis	30,000 gm Y_1 axis	.65% AQL
Fine Leak			.65% AQL	.65% AQL	.65%
Gross Leak			100%	100%	
Pre Burn-in Electrical	100%	100%	100%	100%	Per Device Spec
Burn-in	48 hrs	160 hrs	48 hrs	160 hrs	
Final Electrical	100%	100%	100%	100%	Per Device Spec
AQL Sample	.065%	.065%	.065%	0.65%	Mil Std 105 D
External Visual	Per XR Std	Per XR Std	Per XR Std	Per XR Std	100%
QA Plant Clearance	100%	100%	100%	100%	

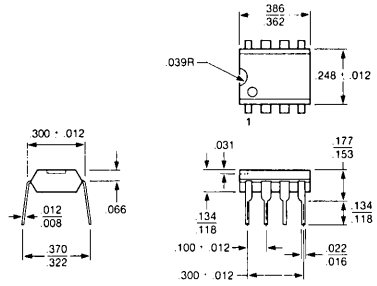
PRICING

CONSULT FACTORY

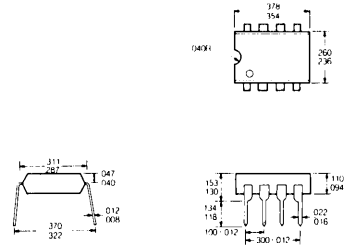
MARKING EXAMPLE



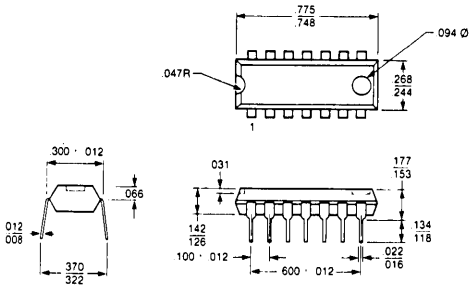
Package Information
(Plastic)



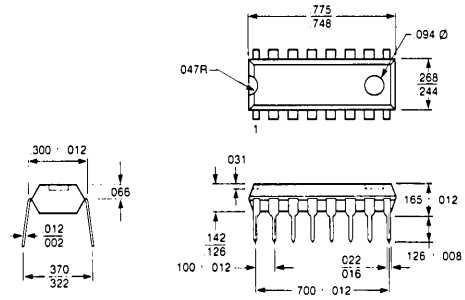
8 PIN MOLDED PLASTIC DIP



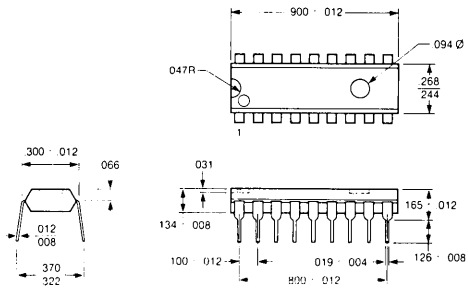
8 PIN MOLDED PLASTIC DIP (JAPAN)



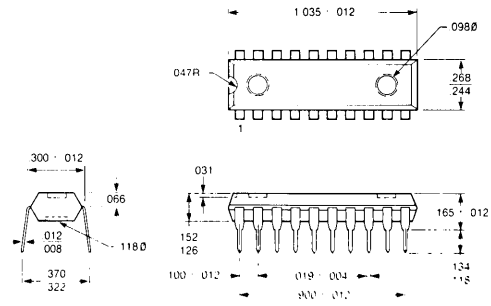
14 PIN MOLDED PLASTIC DIP



16 PIN MOLDED PLASTIC DIP

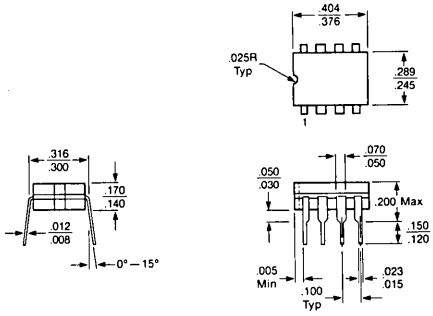


18 PIN MOLDED PLASTIC DIP

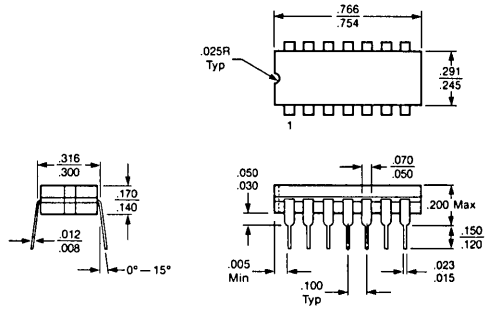


20 PIN MOLDED PLASTIC DIP

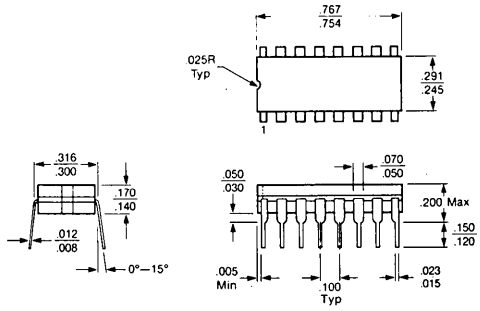
Package Information
(Cerdip)



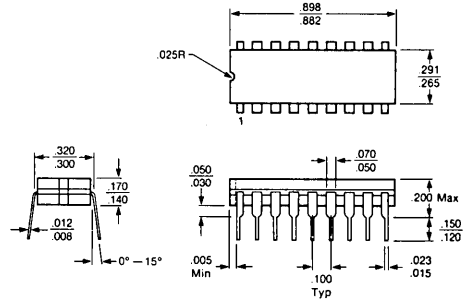
8 PIN CERAMIC CAVITY DIP



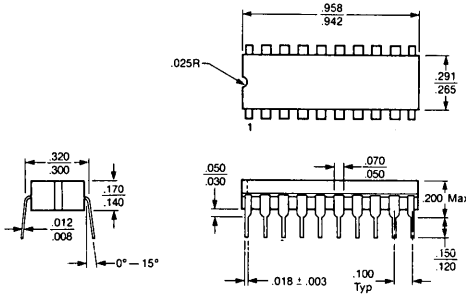
14 PIN CERAMIC CAVITY DIP



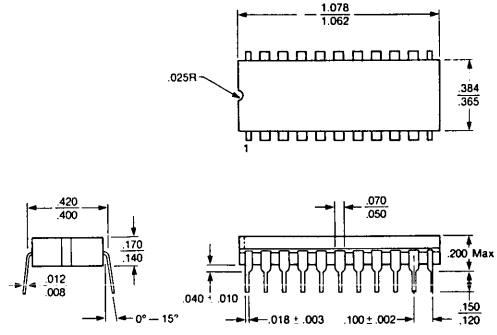
16 PIN CERAMIC CAVITY DIP



18 PIN CERAMIC CAVITY DIP

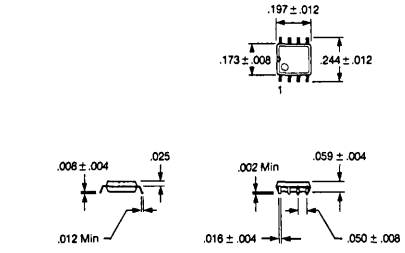


20 PIN CERAMIC CAVITY DIP

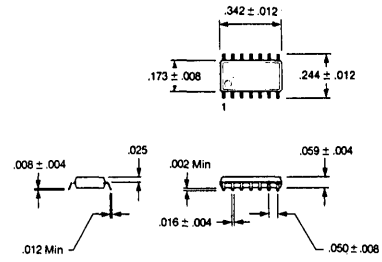


22 PIN CERAMIC CAVITY DIP

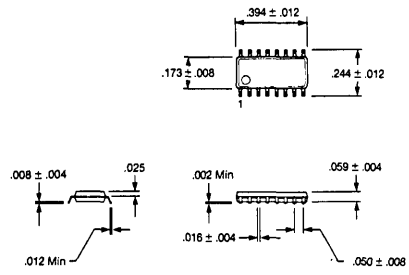
Package Information
(Plastic Small Outline)



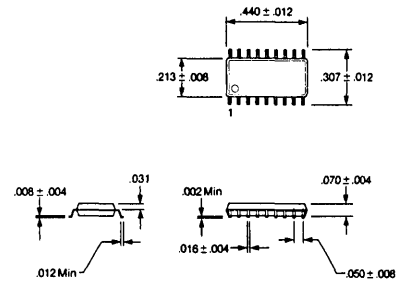
8 PIN S.O.T. PACKAGE (M.D.P.)



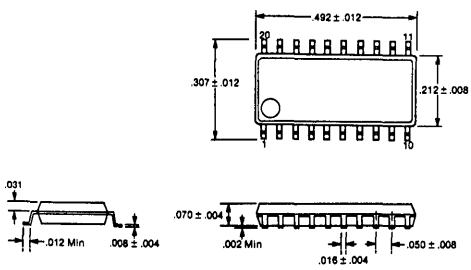
14 PIN S.O.T. PACKAGE (M.D.P.)



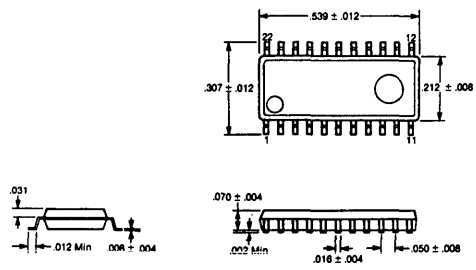
16 PIN S.O.T. PACKAGE (M.D.P.)



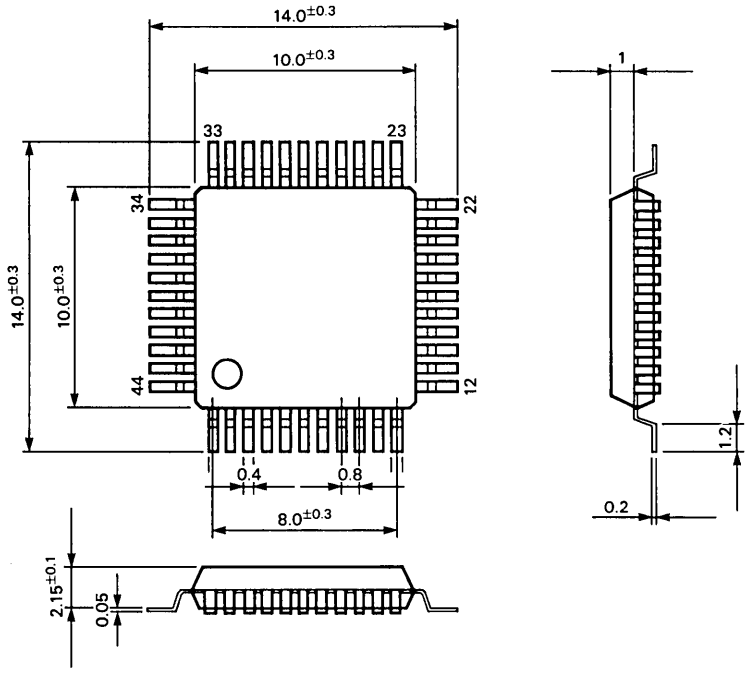
18 PIN S.O.T. PACKAGE (M.D.P.)



20 PIN S.O.T. PACKAGE (M.D.P.)



22 PIN S.O.T. PACKAGE (M.D.P.)



44 PIN QUAD PACKAGE

The Benefits of Surface Attachment

Surface mounting identifies a technique for mounting ICs and other devices of like geometries in a low-profile package on the surface of a printed-circuit board. These devices are today known as SO (Small Outline) devices. Unlike plated-through-hole technology in which the leads of devices are inserted in holes perpendicular to the board surface, the leads of the SO devices solder to circuit board pads that lie on the board surface.

Both the surface area and the profile (height of the package above the board) are reduced. As an example, a 14-pin SO package has an overall height of .067-inch, whereas a conventional DIP is .177-inch high. The SO package leads are spaced on 0.50-inch centers, rather than 0.100-inch centers, as is the case with the traditional DIP package.

Other benefits include:

- **Reduces Assembly Costs**–By utilizing the new pick-and-place equipment, board assembly can be fully automated. Components are available on reels which dramatically reduce storage and handling costs.

- **Smaller Boards**–Because the SO package sizes are approximately 30% to 50% smaller in size than their DIP counterparts, printed-circuit boards can be reduced in size by 50% or more.

- **Less Complex Circuit Boards**–Since SO-packaged ICs mount on the surface, rather than in relatively large (.035-inch) plated-through holes, both rigid and flexible circuit boards require fewer and smaller holes. Where interconnections are required between layers, vias, typically 0.018-inch in diameter, are employed. This enables designs to employ fewer circuit board layers and hence less costly circuit boards per square inch.

- **Higher Performance**–Because boards are smaller and IC lead inductances are less, distributed reactances are reduced and signal paths are shortened. This raises performance in high-speed, digital systems, and in r-f systems.

- **Cost-Effective On-Shore Assembly**–Because the SO components enhance the appeal of on-shore, automated assembly, they can eliminate the severe logistic demands and extended cycle times of off-shore assembly.

Typical Surface Mounting Applications...
In consumer products where compact assemblies are essential–hand-held cameras, toys, audio equipment. In automotive equipment... engine and climate controls.

In Telecommunications... modems, active filter networks, speech processors, PBXs and voice-recognition units.

In Computer Peripherals... Disk Drives, Winchester Drives, and thermal and impact printers.

Exar's Surface-Mountable Package Devices Exhibit Extraordinary Reliability

Exar's SO package, using a unique nitride passivation, has shown itself able to survive highly stressful environmental conditions. Which is why Exar's SO devices are as reliable as any 0.300-inch spaced, conventional DIP.

Here is some typical test data:

Reliability Data

Test	Condition	Sample Size	XR2004 Rejects	XR3403 Rejects	XR4558 Rejects
External Visual	Per MIL STD 883, method 2009.	200	0	0	0
High Temp. Storage	48 Hr. at 150°C	200	0	0	0
Temperature Cycling	10 cycles– −65°C to 150°C per MIL STD 883, method 1010, condition C.	200	0	0	0
Electrical Tests	Per Exar Data Sheet.	200	0	0	0
Lot Sample Burn-in	48 Hr. Max. Elect. Tests per MIL STD 883, method 1015 at 125°C for 48 hours; end point electrical tests per Exar Data Sheet.	55	0	0	0
Autoclave (Pressure Cooker)	100 Hr. 121°C, 15 p.s.i.g.; electrical tests per Exar Data Sheet.	25	1*	0	0
Steady State Life	1000 Hr. T_A = 125°C per MIL STD 883, method 1015. (See Note)	55	0	0	0
Biased Moisture Life	1000 Hr. T_A = 85°C, R.H. = 85%; electrical tests per Exar Data Sheet.	55	0	0	0

**Note:* One electrical failure at post burn-in after 500 hours.

Surface-Mounting Manufacturing Techniques...

Component Handling
Exar can supply ICs in both antistatic tubes and various tape and reel options, including EIA standard RS-481 specified taping (see bibliography page 7). This taping is compatible with automated assembly equipment such as Panasonic's Panaplace "M", Universal Instrument's Onserter, and adaptable to many others such as Dynapert, Zevatech, Celmacs, Fuji, and MCT.

Component Placement
Typically pick-and-place equipment uses a vacuum mechanism to hold the device on its vacuum placement probe. Placement equipment can place within ± 0.0005 inch from a fixed x-y position. Typical equipment places 800 to 8000 components per hour with some equipment placing surface-mounted devices at even much higher rates.

A standard technique is to tack the IC in place with solder paste, then dried in order to secure position prior to wave soldering.

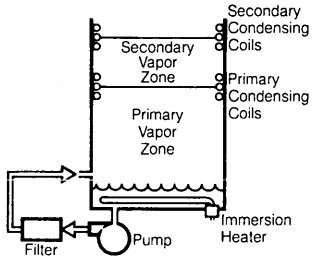
In practice, alignment can be off slightly due to the 'self-aligning' feature. For when the heat melts the solder, the leads are pulled laterally as well as down onto the pads.

Component Soldering
The SO package is designed primarily for reflow soldering—rather than wave soldering. Reflow techniques include:

- Infrared
- Hot Air
- Vapor Phase

Best results are obtained when the same solder is used on the leads and on the substrate metalization. Printed-circuit boards can be metalized by dipping in a solder bath, or by screening solder paste and then reflowing. Paste thickness should be typically 0.006 to 0.008 inch (150 to 200 micrometers) thick.

Batch Type VPS System



A Glossary of Surface Attachment Terms

Aspect Ratio
The ratio of the circuit board thickness to the smallest hole diameter.

Barrel
The cylinder formed by plating through a drilled hole.

Fluorinated Carbon
A fluid which when vaporized behaves as a highly-effective heat-transfer medium in vapor-phase soldering.

Hot-Air Soldering
A typical hot-air system employs a preheat and a soldering air jet. Preheat usually occurs at 110°C, followed by soldering at 260°C. Travel is typically 10 cm/minute (3.93 inches/minute). Air pressure must be monitored to make sure a device is not blown out of position or that molten solder does not bridge adjoining traces.

Infrared
Basically an oven technique for reflow soldering.

Mil
One-thousandth (0.001) of an inch.

Multilayer Printed-Circuit Board
A printed circuit board consisting of three or more conducting circuit planes separated by insulating material and bonded together with internal and external connections to each level of the circuitry as required.

Plated-Through Hole
A hole with the deposition of metal (usually copper) on its sides to provide electrical connections between conductive patterns at the levels of a printed circuit board.

Reflow Soldering
A technique employed in surface attachment to solder devices to printed circuit boards. It requires that leads and pads of boards already have solder in place.

SMD
Surface Mount Device—(same as SO)

SO Package
Small Outline Package (See SMD)

Solder Paste
Finely-powdered solder and flux suspended in a binder.

Solder Resists
Coatings which mask and insulate portions of a circuit pattern where solder is not desired.

Vapor-Phase Soldering
A technique employed in surface attachment technology to reflow solder devices to the foil pads on the printed circuit board. Heat is conducted through a gas, typically a boiling inert fluid usually 215°C blanketed with a vapor blanket to prevent loss of the inert fluid. This technique is significantly faster than other methods.

Via
A plated-through hole used as a through connection, but in which there is no intention to insert a component lead.

Wave Soldering
The traditional technique for soldering components to circuit boards. The bottom surface of the boards travels across the surface of a reservoir of molten solder and the solder is drawn up into each plated-through hole by capillary action.

Wetting
The formation of a relatively uniform, smooth, unbroken and adherent film of solder to a base material.

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