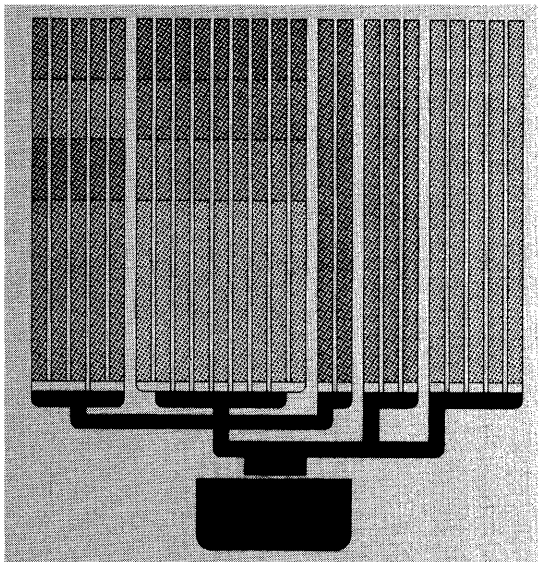


MSI
9300, 93L, 93S and
54/74 Series Data Sheets

TTL/MSI 9300
4-BIT UNIVERSAL SHIFT REGISTER

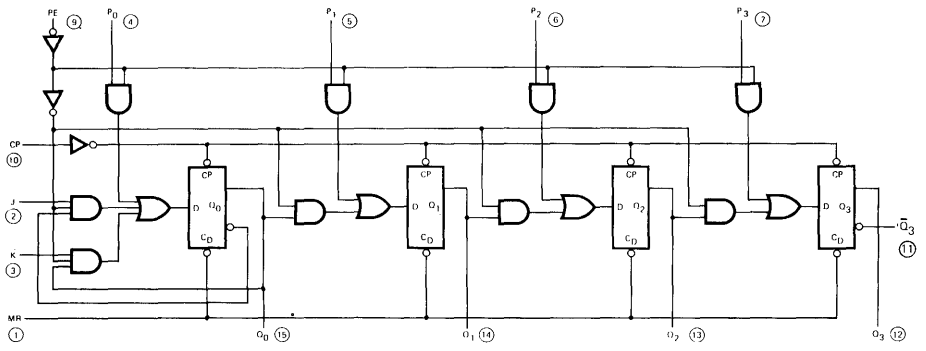
DESCRIPTION — The 9300 is a TTL/MSI 4-Bit Universal Shift Register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. This new 9300 replaces the earlier 9300 device in all applications. All requirements of the original 9300 specification are satisified with the minimum shift rate of 15 MHz being improved to 30 MHz.

- **38 MHz TYPICAL SHIFT FREQUENCY**
- **ASYNCHRONOUS COMMON RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **SYNCHRONOUS PARALLEL ENTRY**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
$\overline{PE}$	Parallel Enable (Active LOW) Input	2.3 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	1 U.L.
J	First Stage J (Active HIGH) Input	1 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	1 U.L.
CP	Clock (Active HIGH) Going Edge Input	2 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note b)	6 U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note c)	8 U.L.

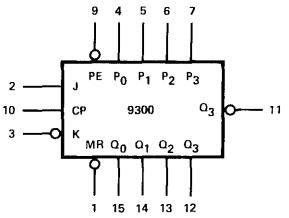
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 6 U.L. is the output LOW drive factor and 12 U.L. is the output HIGH drive factor.
c. 8 U.L. is the output LOW drive factor and 16 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



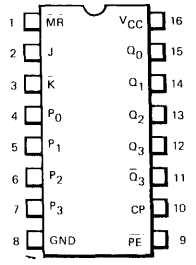
○ = Pin Numbers

LOGIC SYMBOL

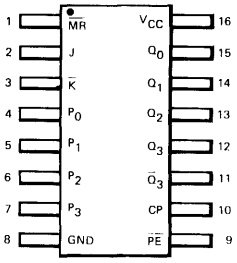


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION — The logic diagram indicates the functional characteristics of the 9300 4-bit shift register. Several special logic features of the 9300 design which increase the range of useful application are:

1. A J$\overline{K}$ input is provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the LOW voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for most general applications. At the same time the simple D type input most appropriate for a shift register can be easily obtained by tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logic operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the parallel enable input is LOW. With the parallel enable input LOW, the element appears as four common clocked D flip-flops. When the parallel enable is HIGH, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active HIGH output is provided for all four stages and an active LOW output is provided for the last stage.
6. A master asynchronous reset input allows the setting to zero of all stages independent of any other input condition.

TRUTH TABLES

TABLE I—SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TABLE II—SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J&$\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

TABLE III—PARALLEL ENTRY
($\overline{PE}$ = LOW, $\overline{MR}$ = HIGH)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or Q_3)
L	L
H	H

TABLE IV—MODE SELECTION

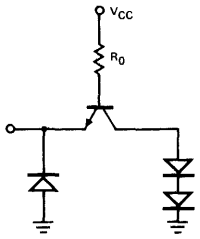
	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Entry	H	X	X	X	X	Refer to Table I & II		H
Parallel Entry	L	Refer to Table III				X	X	H

(n+1) = Indicates state after next clock

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

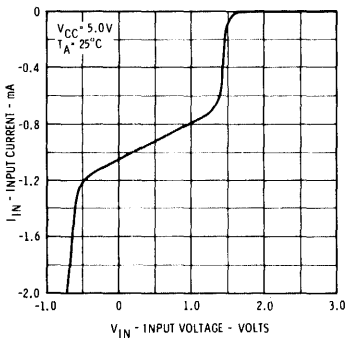
INPUTS

EQUIVALENT CIRCUIT

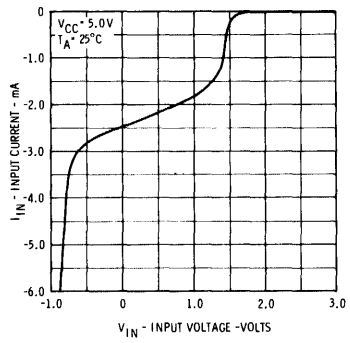


INPUT CURRENT VERSUS INPUT VOLTAGE

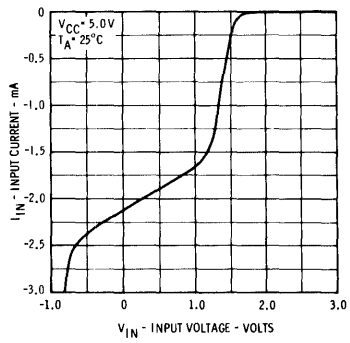
$\overline{MR}$, J, $\overline{K}$, P_0, P_1, P_2, & P_3



$\overline{PE}$

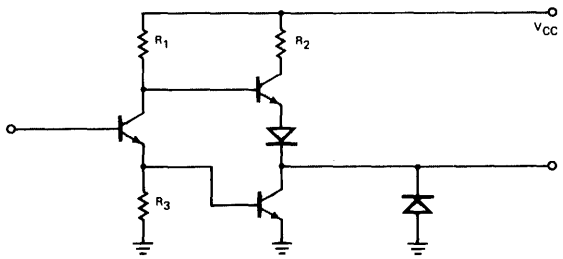


CP



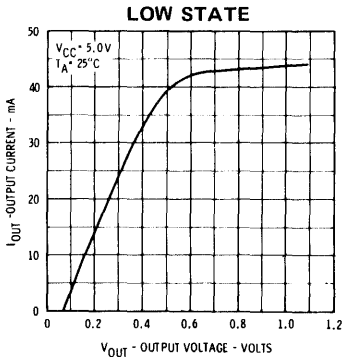
OUTPUTS

EQUIVALENT CIRCUIT

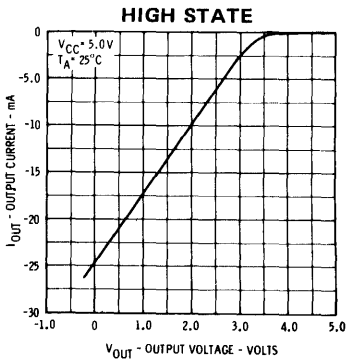


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (Q_0, Q_1, Q_2, Q_3 AND $\overline{Q_3}$)

LOW STATE



HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN.	TYP.	MAX.	
9300XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9300XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETERS	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −640 μA for $\overline{Q_3}$, and −480 μA for Q_0–Q_3; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 12.8 mA for $\overline{Q_3}$ and 9.6 mA for Q_0–Q_3; V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current					
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	CP		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	$\overline{PE}$		23	92	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current, all inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current					
	J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
	CP		−1.92	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
	$\overline{PE}$		−2.21	−3.7	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−80	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		60	86	mA	9300XM; V_{CC} = MAX. Inputs HIGH
			60	92	mA	9300XC; V_{CC} = MAX. Inputs HIGH

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
f_{sr}	Shift Right Frequency	30	38		MHz	See Fig. 1.	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH}	Turn Off Delay from Clock to Output		12	22	ns		
t_{PHL}	Turn On Delay from Clock to Output		19	26	ns		
t_{PHL} ($\overline{MR}$)	Turn On Delay from $\overline{MR}$ to OUTPUT (Except $\overline{Q_3}$)		26	37	ns	See Fig. 2.	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{pw} (CP)	Clock Pulse Width	17	11		ns	See Fig. 1	V_{CC} = 5.0 V
t_s (Data)	Set-up Time Data to Clock	20	13		ns	See Fig. 3.	
t_h (Data)	Hold Time Data to Clock	0	−11		ns		
t_s ($\overline{PE}$)	Set-up Time $\overline{PE}$ to Clock	39	24		ns	See Fig. 4	
t_h ($\overline{PE}$)	Hold Time $\overline{PE}$ to Clock	−10	−20		ns		
t_{pw} ($\overline{MR}$)	Master Reset Pulse Width	25	13		ns	See Fig. 2.	
t_{rec} ($\overline{MR}$)	Recovery Time Master Reset to Clock	25	12		ns		

DEFINITION OF TERMS

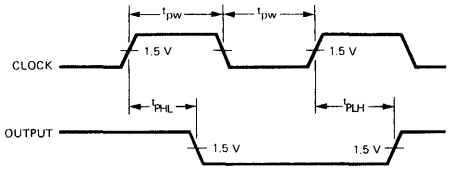
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the Reset pulse and the clock transistion from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SWITCHING TIME WAVEFORMS

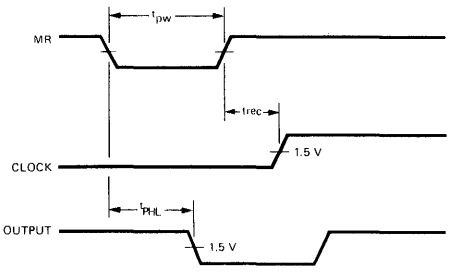
Clock to Output Delays and Clock Pulse Width.



OTHER CONDITIONS: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

Fig. 1.

Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time.

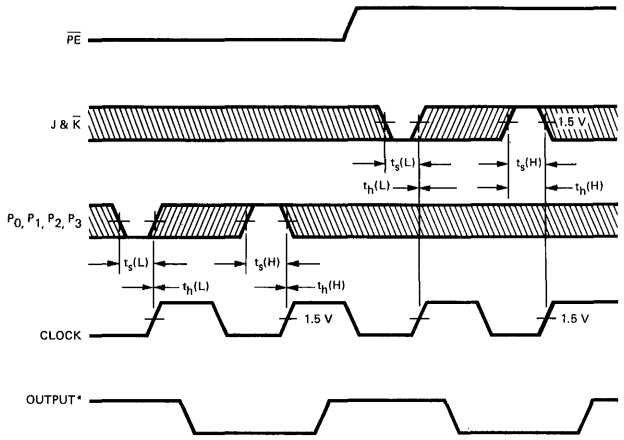


OTHER CONDITIONS: $\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3 = H$

Fig. 2.

SWITCHING TIME WAVEFORMS
(Cont't)

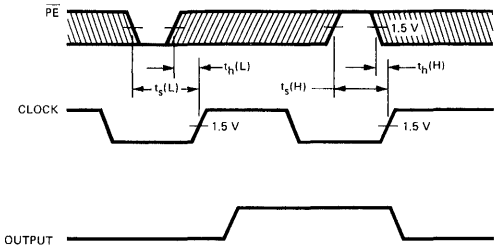
Set-up (t_s) and Hold (t_h) Time for Serial Data (J and $\overline{K}$) and Parallel Data (P_0, P_1, P_2 and P_3)



OTHER CONDITIONS: $\overline{MR}$ = H
*J & $\overline{K}$ SET-UP TIME AFFECTS Q_0 ONLY

Fig. 3.

Set-up (t_s) and Hold (t_h) Time for $\overline{PE}$ Input.



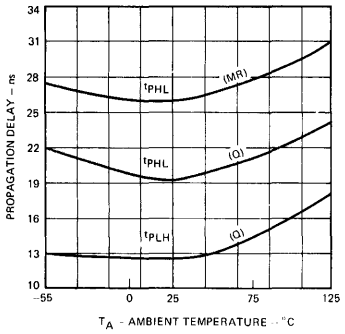
OTHER CONDITIONS: $\overline{MR}$ = H, J = $\overline{K}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 4.

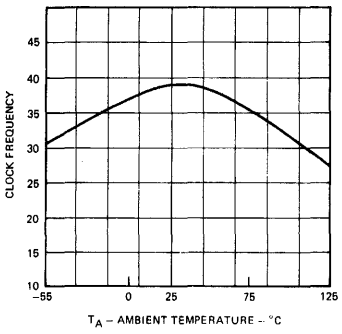
Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

TYPICAL SWITCHING CHARACTERISTICS

**SWITCHING PERFORMANCE
CLOCK TO OUTPUT (Q_3) DELAY
AND MASTER RESET TO OUTPUT DELAY
VERSUS TEMPERATURE**



**CLOCK FREQUENCY
VERSUS
AMBIENT TEMPERATURE**



8

TTL/MSI 93H00

HIGH SPEED UNIVERSAL 4-BIT SHIFT REGISTER

DESCRIPTION — The 93H00 is a TTL/MSI 4-Bit Universal Shift Register offering a typical shift frequency to 55 MHz and guaranteed minimum value of 45 MHz. These features make the 93H00 useful in a wide range of high speed register and counter applications. These include serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data registers.

The 93H00 is pin compatible with the 9300 and 93L00 shift registers. Major electrical differences are the speed of operation and resulting power dissipation.

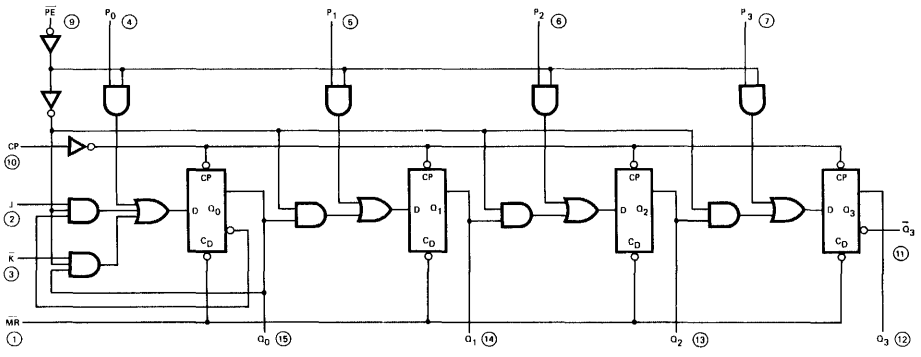
- **55 MHz TYPICAL SHIFT FREQUENCY**
- **ASYNCHRONOUS COMMON RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **SYNCHRONOUS PARALLEL ENTRY**
- **TYPICAL POWER DISSIPATION OF 350 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **PIN FOR PIN COMPATIBLE WITH 9300A AND 93L00 DEVICES**

PIN NAMES

		LOADING (Note a)
$\overline{PE}$	Parallel Enable (Active LOW) Input	1 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	1 U.L.
J	First Stage J (Active HIGH) Input	1 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	1 U.L.
CP	Clock (Active HIGH) Going Edge Input	2 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note b)	8 U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note b)	10 U.L.

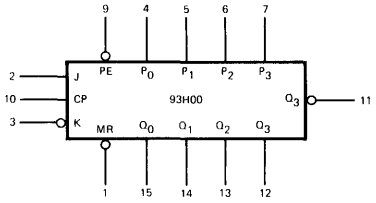
NOTES
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor

LOGIC DIAGRAM



○ = Pin Numbers

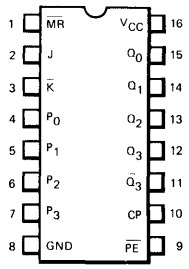
LOGIC SYMBOL



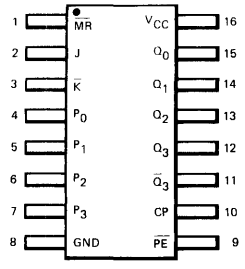
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION — The logic diagram indicates the functional characteristics of the 93H00 4-bit shift register. Special logic features of the 93H00 design which increase the range of application are described below:

1. A J$\overline{K}$ input is provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the LOW voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for most general applications. At the same time the simple D type input most appropriate for a shift register can be easily obtained by tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logic operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the Parallel Enable input is LOW. With the Parallel Enable input LOW, the element appears as four common clocked D flip-flops. When the Parallel Enable is HIGH, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active HIGH output is provided for all four stages and an active LOW output is provided for the last stage.
6. A master asynchronous reset input allows the setting to zero of all stages independent of any other input condition.

TRUTH TABLES

TABLE I — SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II — SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J&$\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

TABLE III — PARALLEL ENTRY
($\overline{PE}$ = LOW, $\overline{MR}$ = HIGH)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or Q_3)
L	L
H	H

(n+1) = Indicates state after next clock

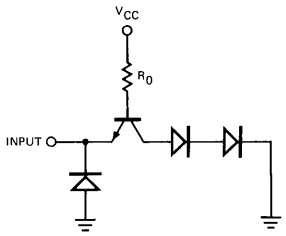
TABLE IV — MODE SELECTION

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Entry	H	X	X	X	X	Refer to Table I & II		H
Parallel Entry	L	Refer to Table III				X	X	H

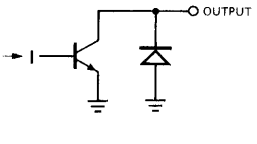
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CIRCUITS

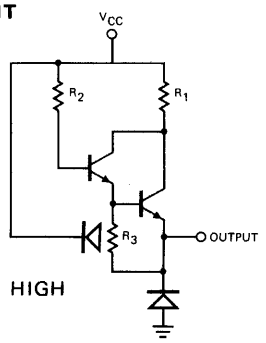
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUIT



LOW



HIGH

Fig. 1
INPUT CURRENT VERSUS INPUT VOLTAGE

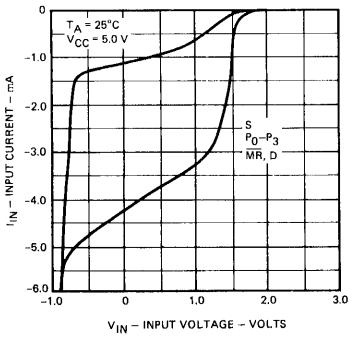


Fig. 2
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

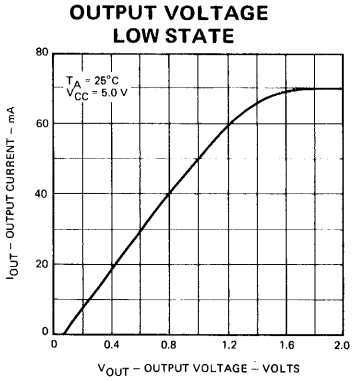
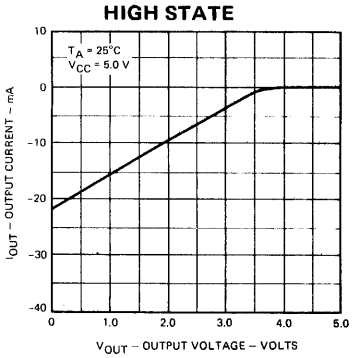


Fig. 3
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN.	TYP.	MAX.	
93H00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93H00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage		2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.64 mA (−0.8 mA, Pin 11) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage			0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 12.8 mA (16 mA, Pin 11) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage				−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
I_{IL}	Input LOW Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3, $\overline{PE}$ CP			 −0.96 −1.92	 −1.6 −3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current J, $\overline{K}$, $\overline{MR}$, P_0, P_1, P_2 & P_3, $\overline{PE}$ CP				 40 80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)		−30	−75	−100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current	93H00XM		65	102	mA	V_{CC} = MAX.
		93H00XC		65	112		

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
f_{sr}	Shift Right Frequency	45	55		MHz	Fig. 4	V_{CC} = 5.0 V, C_L = 15 pF
t_{PLH}	Turn Off Delay from Clock to Output		10	16	ns		
t_{PHL}	Turn on Delay from Clock to Output		14.5	21	ns		
t_{PHL} ($\overline{MR}$)	Turn on Delay from $\overline{MR}$ to Output (Except $\overline{Q}_3$)		21	28	ns	Fig. 5	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
t_{pw} (CP)	Clock Pulse Width	12	9.0		ns	Fig. 4	V_{CC} = 5.0 V
t_s (Data)	Set-Up Time Data to Clock	12	6.0		ns	Fig. 6	
t_h (Data)	Hold Time Data to Clock	0	−5.0		ns		
t_s ($\overline{PE}$)	Set-Up Time $\overline{PE}$ to Clock	15	8.0		ns	Fig. 7	
t_h ($\overline{PE}$)	Hold Time $\overline{PE}$ to Clock	0	−7.0		ns		
t_{pw} ($\overline{MR}$)	Master Reset Pulse Width	19	11		ns	Fig. 5	
t_{rec} ($\overline{MR}$)	Recovery Time Master Reset to Clock	7.0	3.0		ns		

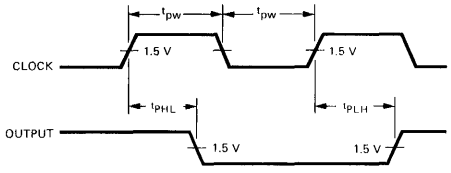
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH data to the Q outputs.

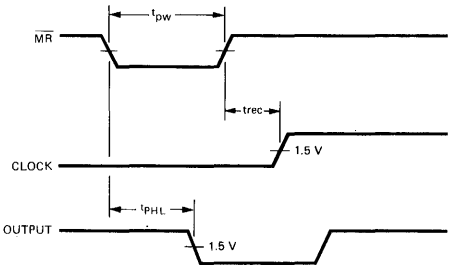
SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



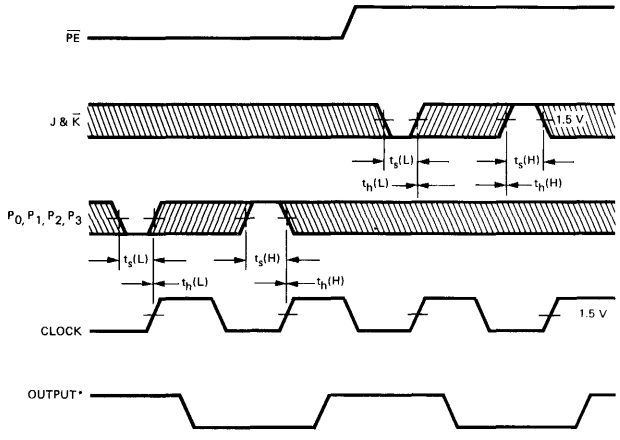
Other Conditions: $J = \overline{PE} = \overline{MR} = H$
$\overline{K} = L$

Fig. 4 – CLOCK TO OUTPUT DELAYS & CLOCK PULSE WIDTH



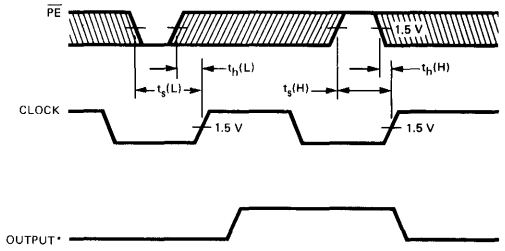
Other Conditions: $\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 5 – MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Other Conditions: $\overline{MR}$ = H
*J&$\overline{K}$ Set-Up Time Affects Q_0 Only

Fig. 6 – SET-UP (t_s) AND HOLD (t_h) TIME FOR SERIAL DATA (J&$\overline{K}$) AND PARALLEL DATA (P_0, P_1, P_2, P_3)



Other Conditions: $\overline{MR}$ = H, J = $\overline{K}$ = L
$P_0 = P_1 = P_2 = P_3$ = H
*t_s(H) and t_h(H) Affects Q_0 Only

Fig. 7 – SET-UP (t_s) AND HOLD (t_h) TIME FOR $\overline{PE}$ INPUT

LPTTL/MSI 93L00
LOW POWER 4-BIT SHIFT REGISTER

DESCRIPTION — The LPTTL/MSI 93L00 4-Bit Shift Register is a medium speed multi-functional sequential logic block, useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTL technology for high speed and high fanout capability, and is compatible with the Fairchild TTL family.

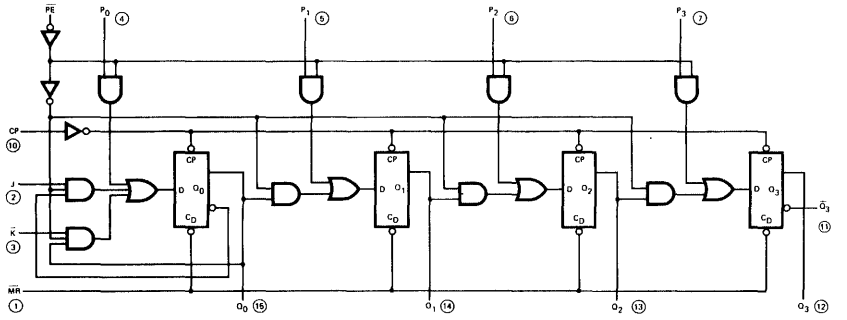
- 15 MHz TYPICAL SHIFT FREQUENCY
- ASYNCHRONOUS COMMON RESET
- J, $\overline{K}$ INPUTS TO FIRST STAGE
- SYNCHRONOUS PARALLEL ENTRY
- TYPICAL POWER DISSIPATION OF 75 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES

		LOADING HIGH	LOADING LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.15 U.L.	0.575 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
J	First Stage J (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{K}$	First Stage K (Active LOW) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	8.0 U.L.	2.0 U.L.
$\overline{Q}_3$	Complementary Last Stage Output	8.0 U.L.	2.0 U.L.

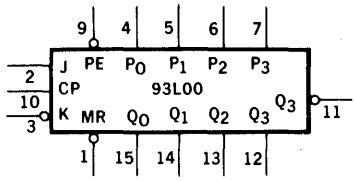
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



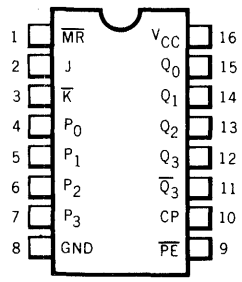
○ = PIN NUMBERS

LOGIC SYMBOL

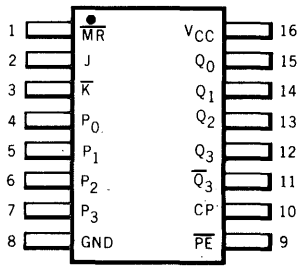


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION — The logic diagram indicates the functional characteristics of the 93L00 4-bit shift register. Special logic features of the 93L00 design increase the versatility of this shift register.

1. A $J\overline{K}$ input is provided to the first flip-flop in the register. This type of input is the same as the more common JK input except that the LOW voltage level activates the $\overline{K}$ input. This provides the greater power of the JK type input for most general applications. At the same time the simple D type input most appropriate for a shift register can be easily obtained by tying the two inputs together.
2. There is no restriction on the activity of the J or $\overline{K}$ inputs for logic operation—except for the set up and release time requirements.
3. Parallel inputs for all four stages are provided. These will determine the next condition of the shift register synchronous with the clock input, whenever the parallel enable input is LOW. With the parallel enable input LOW, the element appears as four common clocked D flip-flops. When the parallel enable is HIGH, or not connected, the shift register performs a one bit shift for each clock input. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.
4. An internal clock buffer provides both reduced clock input loading, and the ability to gate the clock with only a single NAND gate.
5. The active HIGH output is provided for all four stages and an active LOW output is provided for the last stage.
6. An asynchronous master reset input allows the setting to zero of all stages independent of any other input condition.

TRUTH TABLES

TABLE I – SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

TABLE II – SERIAL ENTRY
($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH)

J & $\overline{K}$ Connected	Q_0 at t_{n+1}
L	L
H	H

TABLE III – PARALLEL ENTRY
($\overline{PE}$ = LOW, $\overline{MR}$ = HIGH)

D-Input (P_0, P_1, P_2 or P_3)	Output Q at t_{n+1} (Q_0, Q_1, Q_2 or $\overline{Q}_3$)
L	L
H	H

(n+1 = Indicates state after next clock)

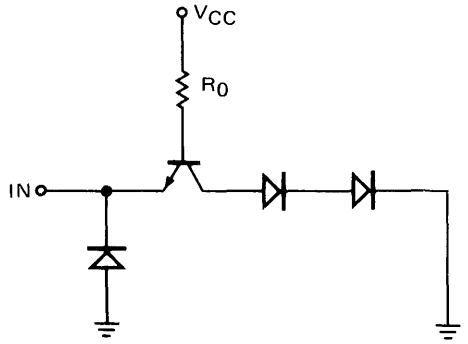
TABLE IV – MODE SELECTION

	$\overline{PE}$	P_0	P_1	P_2	P_3	J	$\overline{K}$	$\overline{MR}$
Serial Entry	H	X	X	X	X	Refer to Table I & II		H
Parallel Entry	L	Refer to Table III				X	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

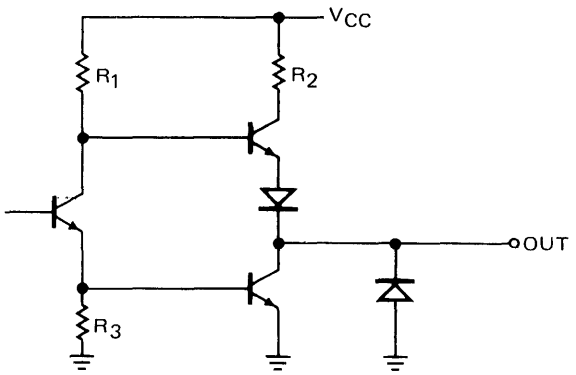
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT



TYPICAL RESISTORS
R_0 = 16 kΩ
R_1 = 6 kΩ
R_2 = 240 Ω
R_3 = 5 kΩ

OUTPUTS EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L00XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L00XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.1	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V
	J, $\overline{K}$, $\overline{MR}$, P_0,P_1,P_2 & P_3		−0.25	−0.40		
	CP		−0.50	−0.80		
	$\overline{PE}$		−0.58	−0.92		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	J, $\overline{K}$, $\overline{MR}$, P_0,P_1,P_2 & P_3		2.0	20		
	CP		4.0	40		
	$\overline{PE}$		5.0	46		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		15	23	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
f_{sr}	Shift Right Frequency	10	17		MHz	V_{CC} = 5.0 V, C_L = 15 pF (See Fig. 1c)
t_{PLH}	Turn Off Delay		23	35	ns	V_{CC} = 5.0 V, C_L = 15 pF (See Fig. 1a)
t_{PHL}	Turn On Delay		34	51	ns	
$t_{PHL}(\overline{MR})$	Reset Time for $\overline{MR}$		55	83	ns	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN	TYP	MAX			
$t_{pw}CP$	Clock Pulse Width	38	25		ns	Fig. 1c	V_{CC} = 5.0 V, C_L = 15 pF
t_s	Set-up Time	60	35		ns	Fig. 1a	
t_h	Hold Time	0	-22		ns		
$t_s(\overline{PE})$	Set-up Time for $\overline{PE}$	68	45		ns	Fig. 1b	
$t_h(\overline{PE})$	Hold Time for $\overline{PE}$	-20	-39		ns		
$t_{rec}(\overline{MR})$	Recovery Time for $\overline{MR}$	70	45		ns	Fig. 1a	
$t_{pw}\overline{MR}$	Min Reset Pulse Width	53	35		ns		

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the flip-flop(s) to respond.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME FOR MR: $t_{rec}(\overline{MR})$ is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order for the flip-flop(s) to respond to the clock.

Fig. 1a

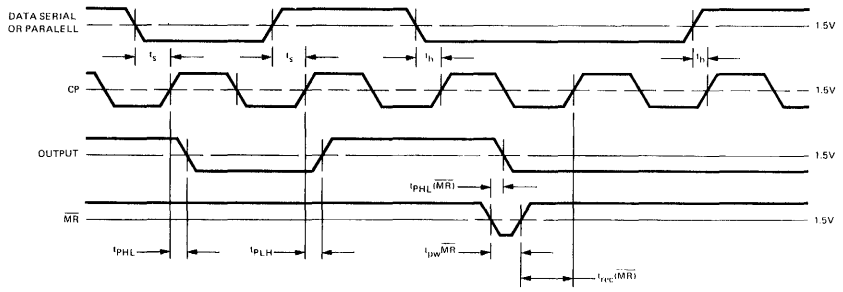


Fig. 1b

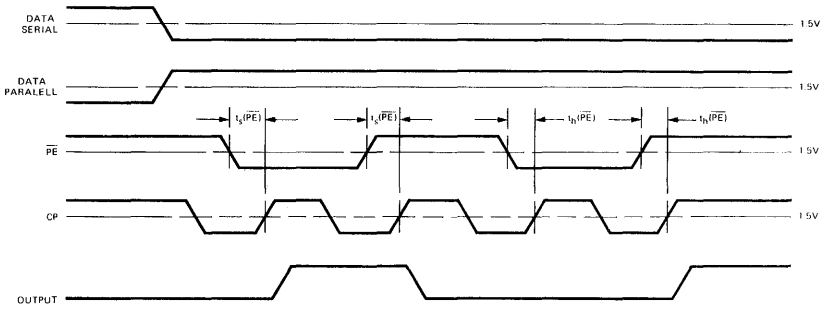


Fig. 1c

V_{OUT} Frequency = 1/2 X V_{IN} Frequency

J = HIGH, $\overline{K}$ = LOW, $\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH

Fig. 1 SWITCHING TIME & SHIFT RIGHT FREQUENCY WAVEFORM

TTL/MSI 93S00
4-BIT UNIVERSAL SHIFT REGISTER
TO BE ANNOUNCED

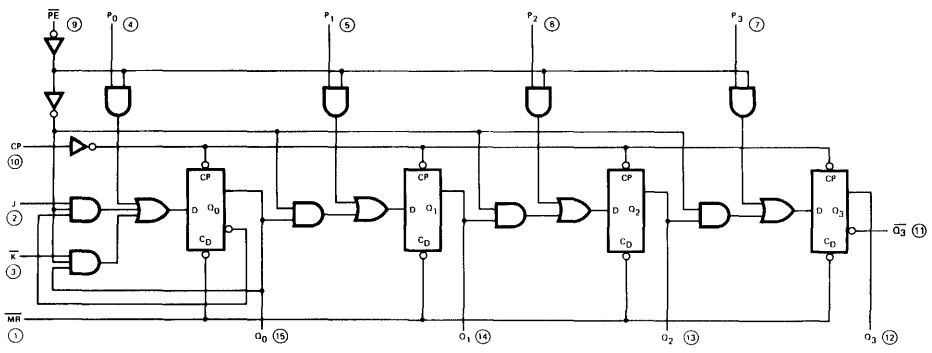
DESCRIPTION — The 93S00 is a TTL/MSI super high speed 4-Bit Universal Shift Register. It utilizes Schottky clamped diode technology to achieve its super high speeds. As a high speed multi-functional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

- **TYPICAL SHIFT RIGHT FREQUENCY OF 100 MHz**
- **ASYNCHRONOUS COMMON RESET**
- **J, $\overline{K}$ INPUTS TO FIRST STAGE**
- **SYNCHRONOUS PARALLEL ENTRY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

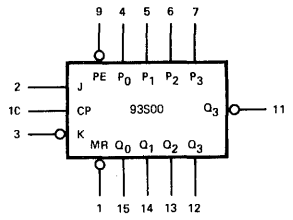
$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0, P_1, P_2, P_3	Parallel Inputs
J	First Stage J (Active HIGH) Input
$\overline{K}$	First Stage K (Active LOW) Input
CP	Clock (Active HIGH) Going Edge Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC DIAGRAM



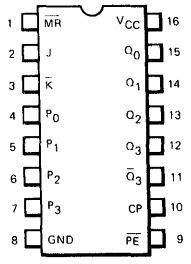
○ = Pin Numbers

LOGIC SYMBOL

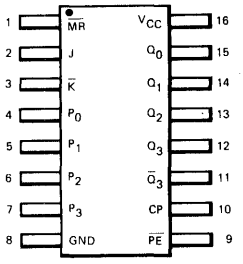


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



TTL/MSI 9301
ONE-OF-TEN DECODER

DESCRIPTION – The 9301 is a Multipurpose Decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTL for high speed and high fan out capability, and is compatible with all members of the Fairchild TTL family.

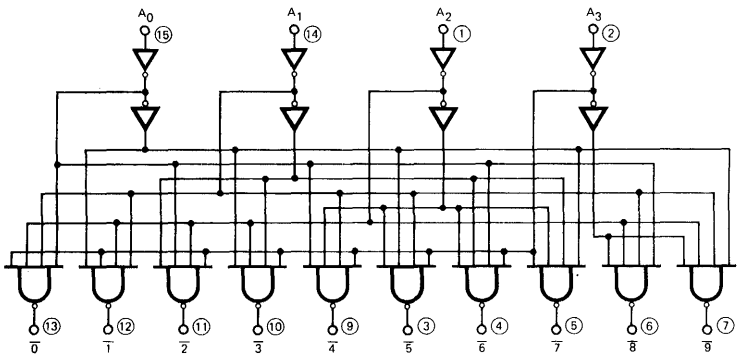
- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **GUARANTEED FANOUT OF 10 TTL LOADS OVER THE FULL TEMPERATURE RANGE AND SUPPLY VOLTAGE RANGES**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 145 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL AND TTL FAMILIES**
- **ALL CERAMIC "HERMETIC" 16 LEAD DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**

PIN NAMES

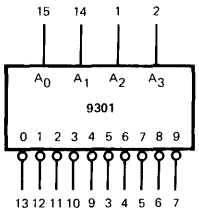
		LOADING (Note a)
A_0, A_1, A_2, A_3	Address Inputs	1 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.

NOTES:
a. Unit Load (U.L.) = 40μA HIGH/1.6mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

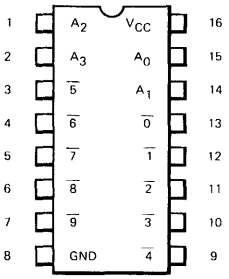


LOGIC SYMBOL

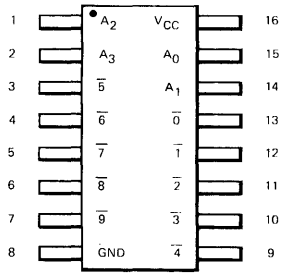


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The 9301 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by the logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enables.

The logic design of the 9301 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant A_3 input produces a useful inhibit function when the 9301 is used as a 1 of 8 decoder.

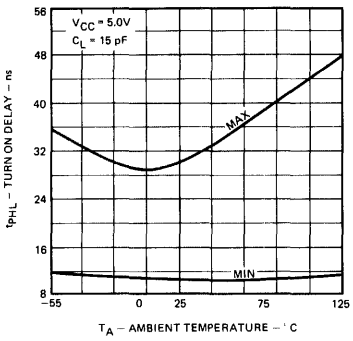
TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

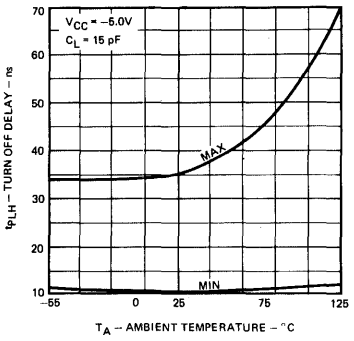
H = HIGH Voltage Level
L = LOW Voltage Level

SWITCHING PERFORMANCE

TYPICAL TURN ON DELAY VERSUS TEMPERATURE



TYPICAL TURN OFF DELAY VERSUS TEMPERATURE



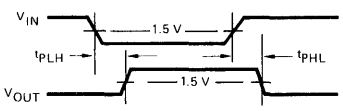
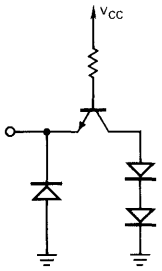


Fig. 1

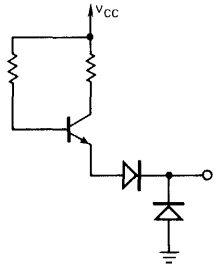
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT EQUIVALENT CIRCUIT

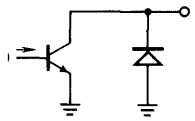


OUTPUT EQUIVALENT CIRCUIT

OUTPUT HIGH



OUTPUT LOW



INPUT CURRENT VERSUS INPUT VOLTAGE

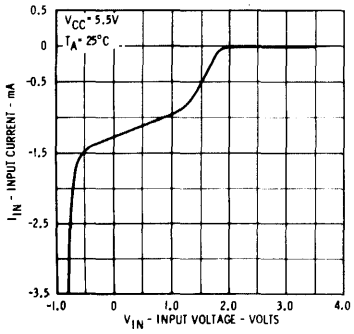


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

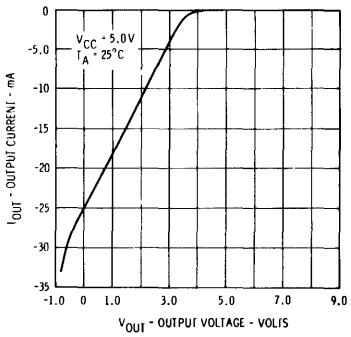


Fig. 3

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

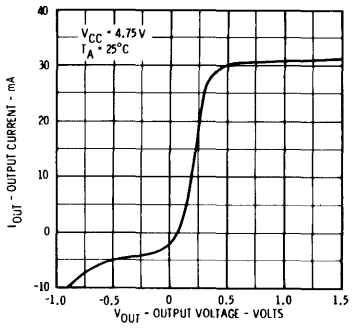


Fig. 4

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9301XM	4.5 V	5.0 V	5.5 V	-55°C to 125°C
9301XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC}= MIN, I_{IN} = -12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = -800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		-0.96	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-20	-40	-70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		29	44	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		23	35	ns	V_{CC} = 5.0V
t_{PHL}	Turn On Delay Input to Output		20	30	ns	C_L = 15pF (See Fig. 1)

8

LPTTL/MSI 93L01

LOW POWER ONE-OF-TEN DECODER

DESCRIPTION – The LPTTL/MSI 93L01 is a Multipurpose Decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL PROPAGATION DELAY OF 63 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

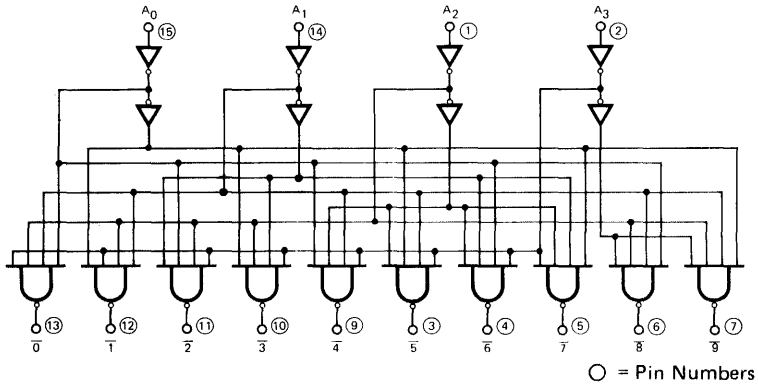
A_0, A_1, A_2, A_3	Address Inputs
$\overline{0}$ to $\overline{9}$	Outputs (Active LOW)

LOADING

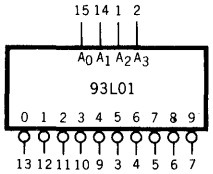
HIGH	LOW
0.5 U.L.	0.25 U.L.
10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

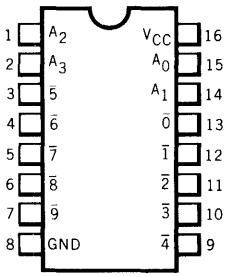


LOGIC SYMBOL

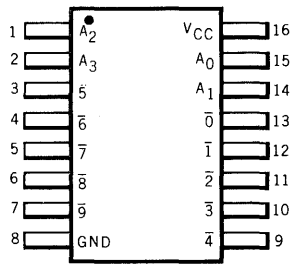


V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93L01 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the 93L01 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the 93L01 is used as a 1-of-8 decoder.

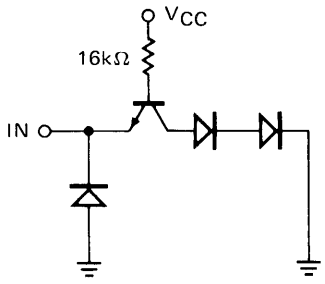
TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

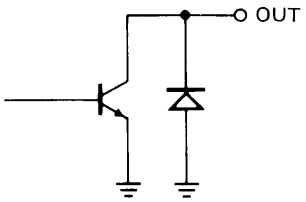
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

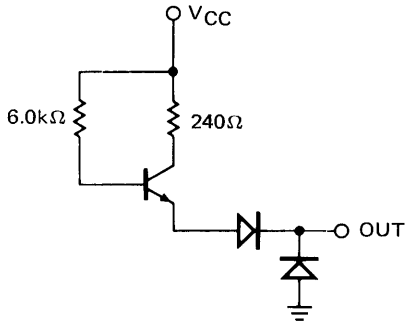


OUTPUTS
EQUIVALENT CIRCUITS

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L01XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L01XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V (Note 5)
I_{CC}	Power Supply Current		9.0	13	mA	V_{CC} = MAX., Inputs at GND

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output		32	50	ns	V_{CC} = 5.0 V See Fig. 1
t_{PHL}	Turn On Delay Input to Output		36	55	ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS

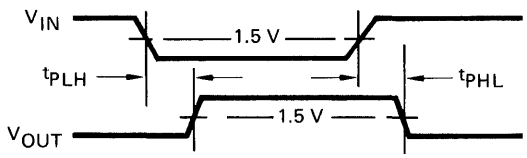


Fig. 1

TTL/MSI 9302
ONE-OF-TEN DECODER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION – The 9302 is a multipurpose Decoder designed to accept four inputs and provide 10 mutually exclusive outputs. The open collector outputs provide wired-OR capability which can be used for numerous summing, decoding and demultiplexing operations. The circuit uses TTL for high speed and high fan out capability, and is compatible with all members of the Fairchild TTL family.

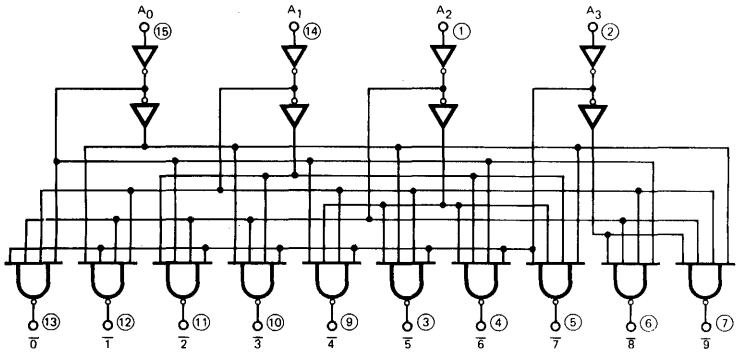
- **OUTPUTS HAVE WIRED-OR CAPABILITY**
- **PROVIDES CAPABILITY TO GENERATE AND SUM MINTERMS OF 3 OR 4 VARIABLES**
- **ACTIVE LOW OUTPUTS ARE USEFUL FOR DRIVING LOW VOLTAGE LAMPS AND RELAYS**
- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 145 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**

PIN NAMES

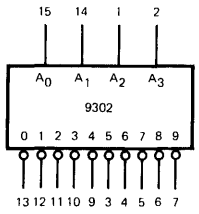
		LOADING (Note a)
A_0, A_1, A_2, A_3	Address Inputs	1 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.

NOTES:
a. Unit Load (U.L.) = 40μA HIGH/1.6mA LOW
b. An external pull-up resistor is needed to provide HIGH level drive capability. The outputs will sink a maximum of 16mA at V_{OUT} = 0.4 V.

LOGIC DIAGRAM

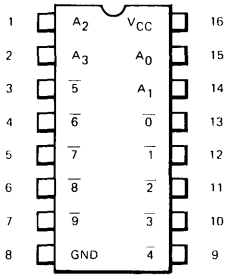


LOGIC SYMBOL

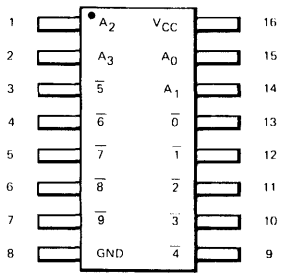


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The 9302 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by the logic symbol. The open collector outputs provide easy summing of input terms. The 9302 provides the capability in one package to generate and sum any or all of the minterms of three variables, or the first 10-of-16 minterms of four variables.

The logic design of the 9302 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input (A_3) produces a useful inhibit function when the 9302 is used as a 1-of-8 decoder.

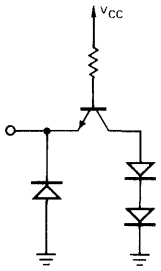
TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

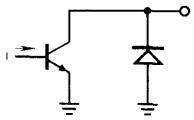
H = HIGH Voltage Level
L = LOW Voltage Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

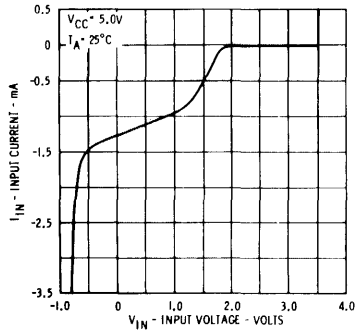
INPUT EQUIVALENT CIRCUIT



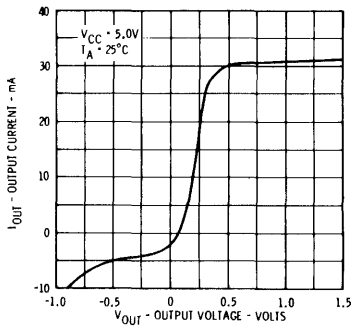
OUTPUT EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9302XM	4.5 V	5.0 V	5.5 V	-55°C to 125°C
9302XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC}= MIN, I_{IN} = -12mA, T_A = 25°C
I_{CEX}	Output HIGH Leakage Current			250	μA	V_{CC} = MIN., V_{CEX} = 5.5 V V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		-0.96	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{CC}	Power Supply Current		29		mA	V_{CC} = MAX.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0V, 25°C, and maximum loading.

TTL/MSI 9304
DUAL FULL ADDER

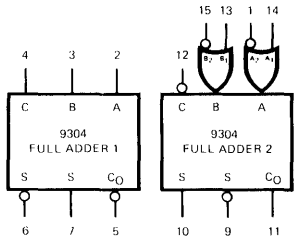
DESCRIPTION — The 9304 consists of two independent, high speed, binary Full Adders. The adders are useful in a wide variety of applications including multiple bit parallel add/serial carry addition, parity generation and checking, code conversion and majority gating. The circuit uses TTL for high speed, high fanout operation and is compatible with all members of the Fairchild TTL family.

- **MULTI-FUNCTION CAPABILITY**
- **8ns CARRY PROPAGATION DELAY**
- **COMPLEMENTARY INPUTS AND OUTPUTS AVAILABLE**
- **TYPICAL POWER DISSIPATION OF 150 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL AND TTL FAMILIES**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES		LOADING (Note a)
FULL ADDER 1		
A, B	Operand Inputs	4 U.L.
C	Carry Input	4 U.L.
S	Sum Output (Note c)	10 U.L.
$\overline{S}$	Complementary Sum Output (Note c)	10 U.L.
$\overline{C}_0$	Carry (Active LOW) Output (Note b)	7 U.L.
FULL ADDER 2		
A_1, B_1	OR Operand (Active HIGH) Input	1 U.L.
$\overline{A}_2$, $\overline{B}_2$	OR Operand (Active LOW) Input	4 U.L.
$\overline{C}$	Carry (Active LOW) Input	4 U.L.
S	Sum Output (Note c)	10 U.L.
$\overline{S}$	Complementary Sum Output (Note c)	10 U.L.
C_0	Carry (Active HIGH) Output (Note b)	7 U.L.

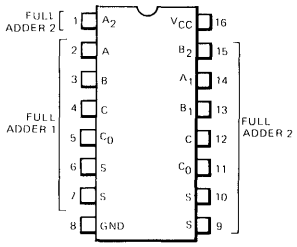
NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.
b. 7 U.L. is the output LOW drive factor and 14 U.L. is the output HIGH drive factor.
c. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC SYMBOL

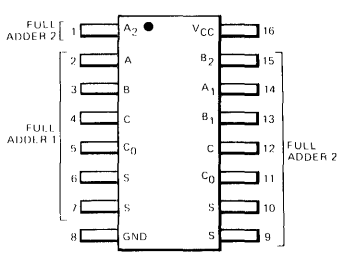


V_{CC} = Pin 16
GND = Pin 8

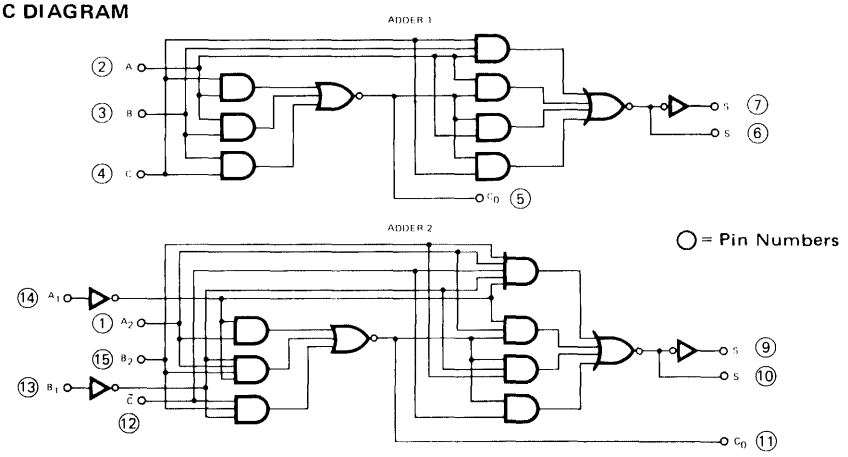
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The Fairchild 9304 logic block consists of two separate high speed carry dependent sum full adders. This design allows a minimum carry propagation time when the adders are used in ripple carry applications. The adders are identical except that adder 2 has provision for either active HIGH or active LOW inputs at the A and B terminals. The adders produce a LOW carry and both LOW and HIGH sum with active HIGH inputs, a HIGH carry and both HIGH and LOW sum when active LOW inputs are used. This principle of duality is shown below, where the adders are drawn as functional blocks.

TRUTH TABLES

ADDER 1

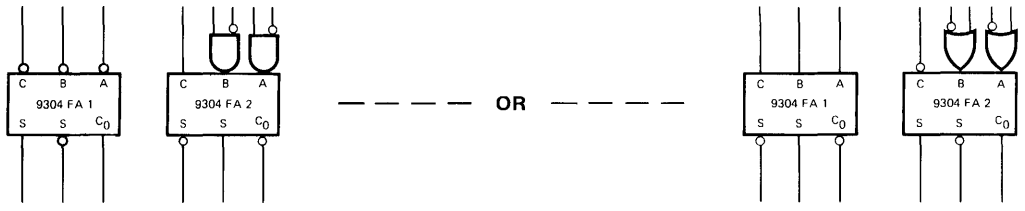
INPUTS			OUTPUTS		
C	B	A	$\overline{C}_0$	$\overline{S}$	S
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

ADDER 2

INPUTS					OUTPUTS		
$\overline{C}$	B_1	A_1	$\overline{B}_2$	$\overline{A}_2$	C_0	S	$\overline{S}$
L	L	L	L	L	H	H	L
L	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H
L	L	L	H	H	L	H	L
L	L	H	L	L	H	H	L
L	L	H	L	H	H	H	L
L	L	H	H	L	H	L	H
L	L	H	H	H	H	L	H
L	H	L	L	L	H	H	L
L	H	L	L	H	H	L	H
L	H	L	H	L	H	H	L
L	H	L	H	H	H	L	H
L	H	H	L	L	H	H	L
L	H	H	L	H	H	H	L
L	H	H	H	L	H	H	L
L	H	H	H	H	H	H	L
H	L	L	L	L	H	L	H
H	L	L	L	H	L	H	L
H	L	L	H	L	L	H	L
H	L	L	H	H	L	L	H
H	L	H	L	L	H	L	H
H	L	H	L	H	H	L	H
H	L	H	H	L	L	H	L
H	L	H	H	H	L	H	L
H	H	L	L	L	H	L	H
H	H	L	L	H	L	H	L
H	H	L	H	L	H	L	H
H	H	L	H	H	L	H	L
H	H	H	L	L	H	L	H
H	H	H	L	H	H	L	H
H	H	H	H	L	H	L	H
H	H	H	H	H	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

FUNCTIONAL BLOCK REPRESENTATION



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30mA to +5.0mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN.	TYP.	MAX.	
9304XM	4.5 V	5.0 V	5.5 V	-55°C to 125°C
9304XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage For All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage For All Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = -12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	I_{OH} = -560μA (Pins 5 & 11) V_{CC} = MIN., I_{OH} = -800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	I_{OL} = 11.2mA (Pins 5 & 11) V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current A_1 & B_1 (Pins 14 & 13) Other Inputs		 10 40	 40 160	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current A_1 & B_1 (Pins 14 & 13) Other Inputs		 -0.96 -3.84	 -1.6 -6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-30	-60	-100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current			55	mA	V_{CC} = MAX., Pins 13 & 14 = 0.0 V

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0V, 25°C, and maximum loading.

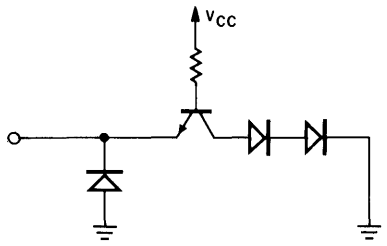
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETERS	9304XM			9304XC			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output A_1 to $\overline{S}$		28	40		28	45	ns	V_{CC} = 5.0 V C_L = 15pF See Fig. B
t_{PHL}	Turn On Delay Input to Output A_1 to $\overline{S}$		25	35		25	40	ns	

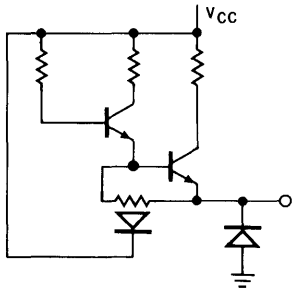
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS EQUIVALENT CIRCUIT

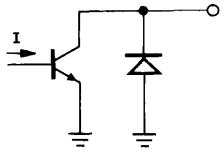


OUTPUTS EQUIVALENT CIRCUIT

OUTPUT HIGH

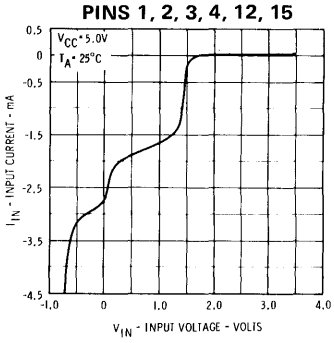


OUTPUT LOW

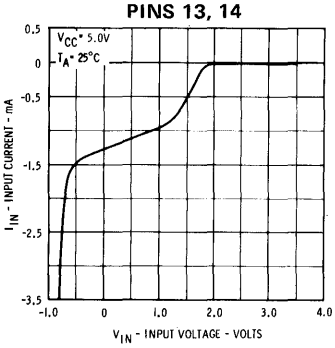


INPUT CURRENT VERSUS INPUT VOLTAGE

PINS 1, 2, 3, 4, 12, 15

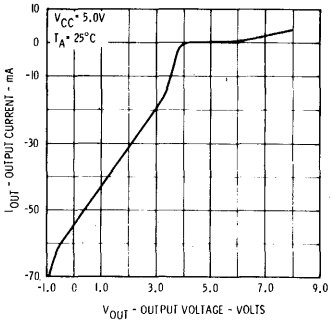


PINS 13, 14



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

HIGH STATE



LOW STATE

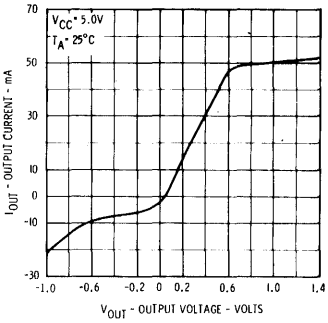
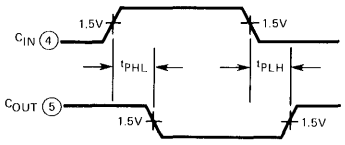
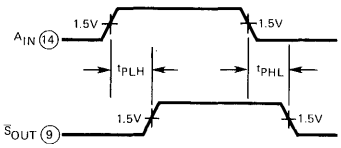


Fig. A

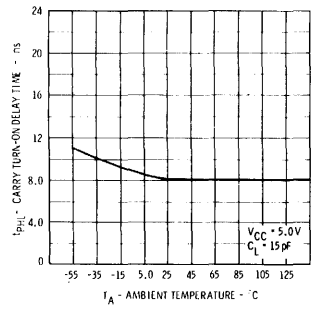
SWITCHING CHARACTERISTICS



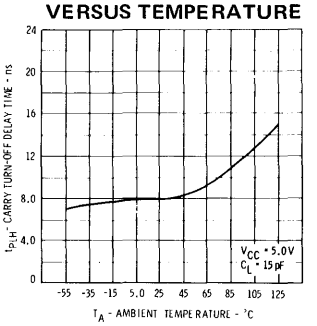
Note: ○ = PIN NUMBER



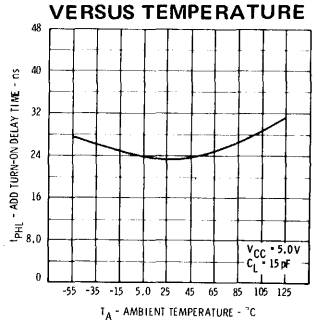
TYPICAL CARRY TURN ON DELAY TIME VERSUS TEMPERATURE



TYPICAL CARRY TURN OFF DELAY TIME VERSUS TEMPERATURE



TYPICAL ADD TURN ON DELAY TIME VERSUS TEMPERATURE



TYPICAL ADD TURN OFF DELAY TIME VERSUS TEMPERATURE

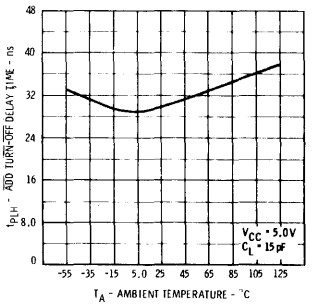


Fig. B

8

TTL/MSI 9305
VARIABLE MODULO COUNTER

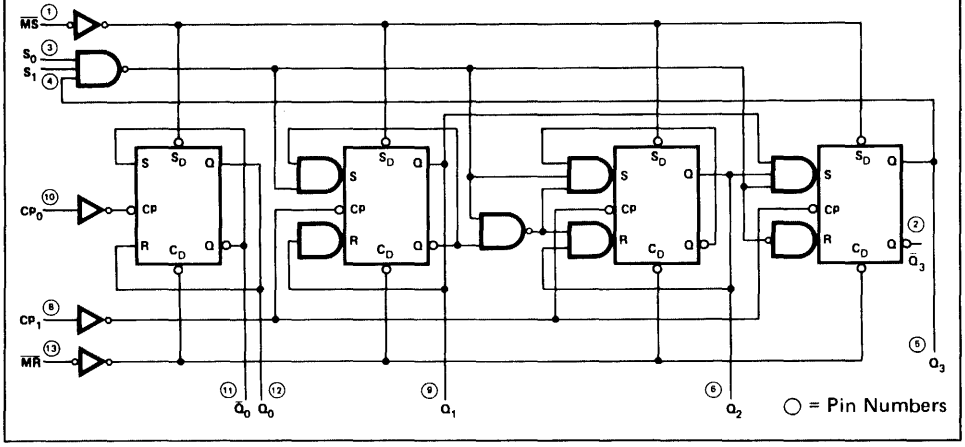
DESCRIPTION – The TTL/MSI 9305 is a monolithic, high speed, Variable Modulo Counter circuit, constructed with the Fairchild Planar* epitaxial process. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8, or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulos as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding master reset and set inputs and the negation output of the final flip-flop output which allows the cascading of stages. The circuit uses TTL for high speed, high fanout operation and is compatible with all other members of the TTL family of digital integrated circuits.

- **VARIOUS BINARY COUNTING MODES**
  –MODULO 2 AND MODULO 5, 6, 7, 8
  –MODULO 10 (8421 BCD), 12, 14, 16
- **VARIOUS FREQUENCY DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**
  –MODULO 8, 10, 12, 14, 16
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET AND SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**
- **TTL COMPATIBLE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

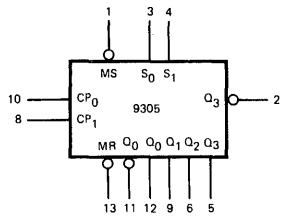
PIN NAMES		LOADING (Note a)
S_0, S_1	Select Inputs	1 U.L.
CP_0	First Stage Clock Active HIGH Going Edge Input	1 U.L.
CP_1	Three Stage Clock Active HIGH Going Edge Input	1 U.L.
$\overline{MS}$	Master Set (Active LOW) Input	1 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0	First Stage Output (Note b)	8 U.L.
$\overline{Q}_0$	Complementary First Stage Output (Note b)	8 U.L.
Q_1, Q_2, Q_3	Three Stage Counter Outputs (Note b)	8 U.L.
$\overline{Q}_3$	Complementary Last Stage Output (Note c)	10 U.L.

NOTES:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
(b) 8 U.L. is the output LOW drive factor and 16 U.L. is the output HIGH drive factor.
(c) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

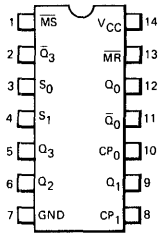


LOGIC SYMBOL

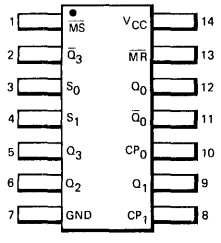


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



*Planar is a patented Fairchild process.

FUNCTIONAL DESCRIPTION – The MSI 9305 consists of four master-slave flip-flops which are separated into two functional units – a single toggle stage and a three stage synchronous counter. All four flip-flops change state on the LOW to HIGH transition of the clock. The three stage counter can be programmed with external connections as shown in the table below to provide modulo of either 5, 6, 7 or 8. This basic configuration allows synchronous binary counting by the last three stages and independent modulo 2 operation with the first single stage.

A four stage binary counter with a modulo of 10, 12, 14 or 16 is obtained by applying the incoming clock to the single toggle stage and feeding its negation output to the clock input of the three stage counter. A 4-stage divider with 50% duty cycle output is produced by feeding the incoming clock to the three stage counter and clocking the single stage with the $\overline{Q}_3$ output. In either the binary or 50% division mode the modulo (10, 12, 14, 16) is determined by the external programming connections for the three stage counter. These 4-stage counters or dividers are not fully synchronous (semisynchronous) but have only one flip-flop ripple delay in either configuration. Counter modulos other than 10, 12, 14, 16 can be formed with a few extra gates.

Several 9305 variable modulo counters programmed in any modulo can be connected together without extra logic to form asynchronous (ripple) type multistage counters. This is done by connecting the $\overline{Q}_3$ output of the less significant counter to the clock input of the following counter.

The Master Set and Reset will asynchronously set or reset all four stages when activated. The active LOW Reset input when LOW will clear the counter, overriding the clock and forcing the outputs (Q_{0-3}) LOW and outputs $\overline{Q}_0$, $\overline{Q}_3$ HIGH. The active LOW Set input when LOW will preset the counter, overriding the clock and forcing the outputs Q_{0-3} HIGH and outputs $\overline{Q}_0$, $\overline{Q}_3$ LOW. The master set provides a synchronous clear, since the first clock pulse following the asynchronous master set will reset all stages. This action is independent of the modulo programmed.

COUNTING MODE

The following are rules specifying the external connections required for various counter and divider modulos.

ASYNCHRONOUS MODE

$\overline{MS}$	$\overline{MR}$	Q_0	$\overline{Q}_0$	Q_1	Q_2	Q_3	$\overline{Q}_3$
L	H	H	L	H	H	H	L
H	L	L	H	L	L	L	H
H	H	COUNT*					

*As determined by programming connections.

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

S_0	S_1	MODULO
NC	NC	5
Q_1	NC	6
NC	Q_1	6
Q_2	NC	7
NC	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

NC = Not Connected

ALTERNATE** PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

S_0	S_1	MODULO
Q_3	Q_3	5
Q_1	Q_1	6
Q_2	Q_2	7
Q_1	Q_2	8
Q_2	Q_1	8

**The alternate programming connections program the counter and conveniently terminate unused select inputs (NC). Since these inputs form the inputs to a single NAND gate (see logic diagram), their connection to the counter outputs for the various count modulos provides the following output drive:

MODULO	OUTPUT	AVAILABLE OUTPUT FANOUT
5	Q_3	14/8
6	Q_1	14/7
7	Q_2	14/7
8	Q_1	15/7
8	Q_2	15/7

CONNECTIONS FOR MODULO 10, 12, 14, 16 BINARY COUNTERS AND 50% DUTY CYCLE DIVIDERS

For Binary Counting $\overline{Q}_0$ connected to CP_1 Incoming clock to CP_0
For 50% Duty Cycle Output $\overline{Q}_3$ connected to CP_0 Incoming Clock to CP_1

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9305XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9305XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	I_{OH} = −800 μA (Pin 2) V_{CC} = MIN., I_{OH} = −640 μA V_{IN} = V_{IH} or V_{IL} per Mode Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	I_{OL} = 16 mA (Pin 2) V_{CC} = MIN., I_{OL} = 12.8 mA V_{IN} = V_{IH} or V_{IL} per Mode Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		42	66	mA	V_{CC} = MAX.

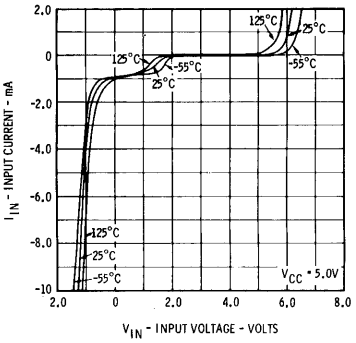
NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

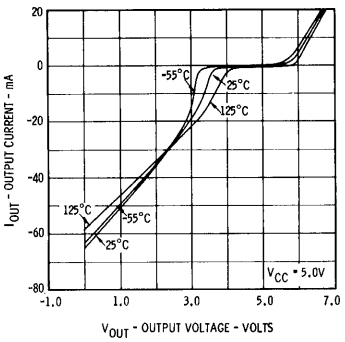
SYMBOL	PARAMETER	9305XM			9305XC			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
f_{COUNT}	Input Count Frequency	20	26		20	26		MHz	V_{CC} = 5.0 V, C_L = 15 pF Modulo 16 (S_0 to Q_1, S_1 to Q_2, $\overline{Q}_0$ to CP_1) Input CP_0
t_{PLH}	Turn-Off Delay Input to Output (CP_0 to Q_3, Modulo 16 Connection)		48	57		48	62	ns	
t_{PHL}	Turn-On Delay Input to Output (CP_0 to Q_3, Modulo 16 Connection)		44	53		44	58	ns	

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

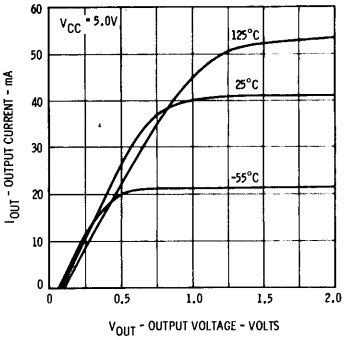
INPUT CURRENT VERSUS INPUT VOLTAGE



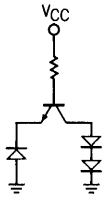
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



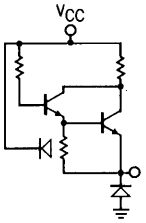
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



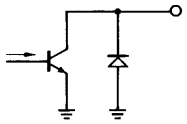
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)

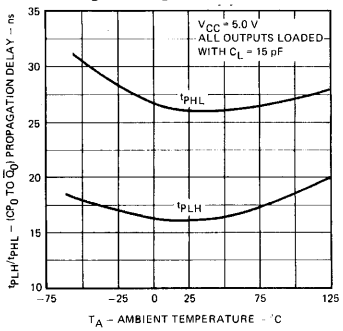


OUTPUT EQUIVALENT CIRCUIT (Output LOW)

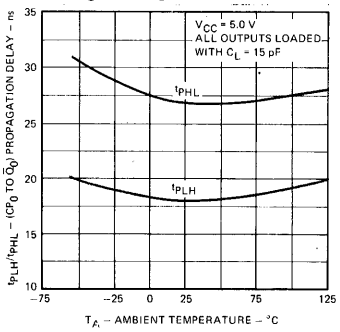


SWITCHING CHARACTERISTICS

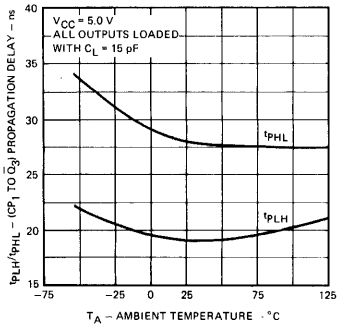
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_0 TO Q_0 MODULO 16

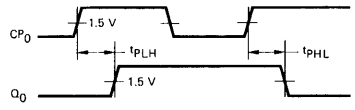


TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_0 TO $\overline{Q}_0$ MODULO 16

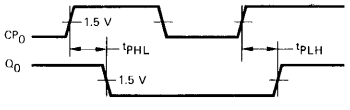


TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_1 TO Q_3 MODULO 8

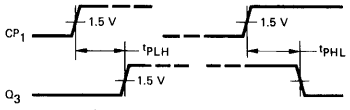




PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN



PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN

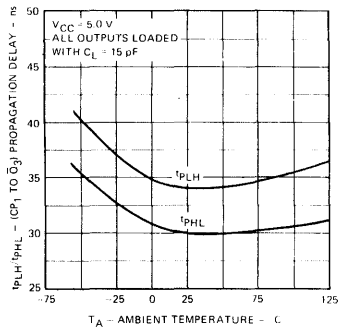


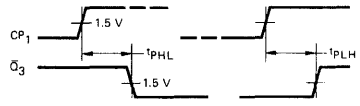
PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

8

SWITCHING CHARACTERISTICS (Continued)

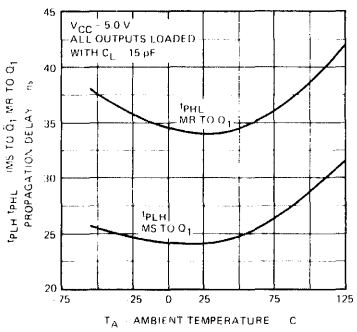
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE CP_1 TO $\overline{Q}_3$ MODULO

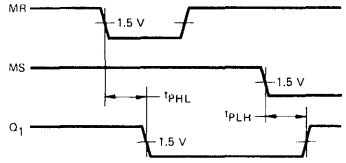




PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

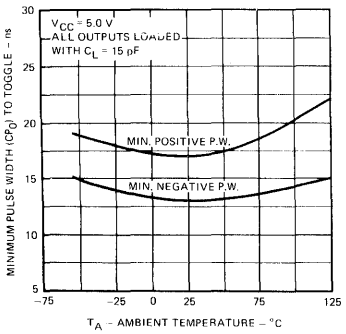
TYPICAL PROPAGATION DELAY VERSUS TEMPERATURE t_{PLH} $\overline{MS}$ TO Q_1 t_{PHL} $\overline{MR}$ TO Q_1 MODULO 8

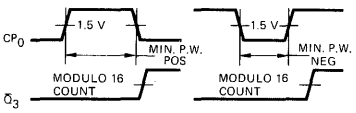




PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

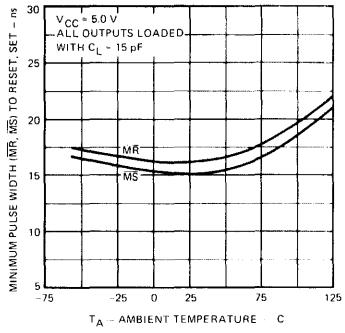
TYPICAL MINIMUM PULSE WIDTH TO TOGGLE VERSUS TEMPERATURE CP_0 MODULO 16

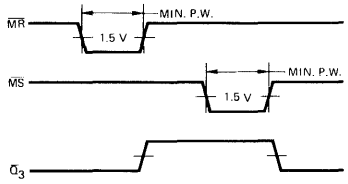




PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN

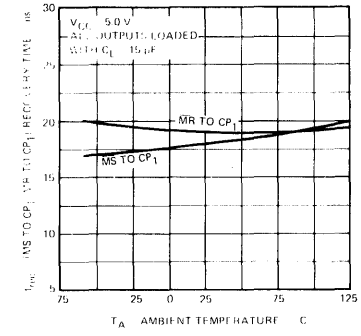
TYPICAL MINIMUM PULSE WIDTH TO RESET, SET VERSUS TEMPERATURE $\overline{MR}$, $\overline{MS}$ MODULO 16

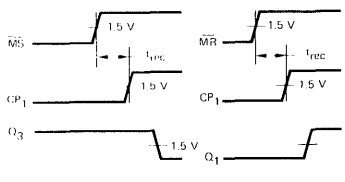




PIN 3 TO PIN 9, PIN 4 TO PIN 6
PIN 8 TO PIN 11, OTHERS OPEN

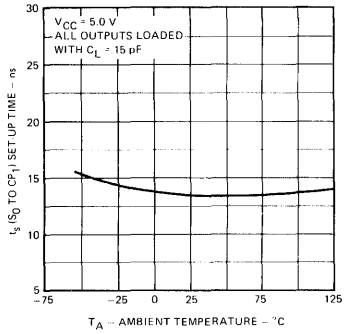
TYPICAL RECOVERY TIME VERSUS TEMPERATURE $\overline{MS}$ TO CP_1, $\overline{MR}$ TO CP_1 MODULO 8

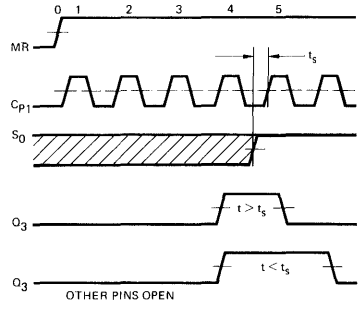




PIN 3 TO PIN 9, PIN 4 TO PIN 6
OTHERS OPEN

TYPICAL SET-UP TIME VERSUS TEMPERATURE S_0 TO CP_1 MODULO 6





t_s is the time required that S_0 must go HIGH before CP_1 clock goes HIGH, such that the circuit recognizes the S_0 as being HIGH. The graph above indicates that times greater than t_s will result in Modulo 5 operation, and that values less than t_s will result in Modulo 6 operation. The shaded area indicates when the input is permitted to change for predictable output performance.

t_{rec} is the time that the $\overline{MR}$ (or $\overline{MS}$) must go HIGH before the clock (CP_1) goes HIGH such that the circuit recognizes the clock (CP_1) pulse.

TTL/MSI 93S05
VARIABLE MODULO COUNTER

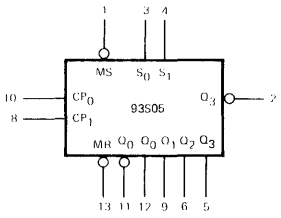
DESCRIPTION – The TTL/MSI 93S05 is a monolithic, high speed, Variable Modulo Counter circuit, constructed with the TTL Schottky Barrier Diode process. It is a semisynchronous counter which can be programmed without extra logic to provide division or counting by either 2 and 4, 5, 6, 7, 8, or 10, 12, 14, 16. A binary count sequence can be obtained for all of the preceding counter modulos as well as 50% duty cycle output for dividers of 8, 10, 12, 14, 16. The device also features asynchronous overriding master reset and set inputs and the negation output of the final flip-flop output which allows the cascading of stages. The circuit uses Schottky TTL for super high speed, high fanout operation and is compatible with all other members of the TTL family of digital integrated circuits.

- **VARIOUS BINARY COUNTING MODES**
  –MODULO 2 AND MODULO 5, 6, 7, 8
  –MODULO 10 (8421 BCD), 12, 14, 16
- **VARIOUS FREQUENCY DIVISION MODES WITH 50% DUTY CYCLE OUTPUT**
  –MODULO 8, 10, 12, 14, 16
- **LOGIC SELECTION OF COUNTING MODE**
- **ASYNCHRONOUS MASTER RESET AND SET INPUTS**
- **MULTISTAGE COUNTING OPERATION**
- **TYPICAL COUNTING FREQUENCY OF 100 MHz**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

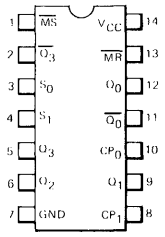
S_0, S_1	Select Inputs
CP_0	First Stage Clock Active HIGH Going Edge Input
CP_1	Three Stage Clock Active HIGH Going Edge Input
$\overline{MS}$	Master Set (Active LOW) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0	First Stage Output
$\overline{Q}_0$	Complementary First Stage Output
Q_1, Q_2, Q_3	Three Stage Counter Outputs
$\overline{Q}_3$	Complementary Last Stage Output

LOGIC SYMBOL

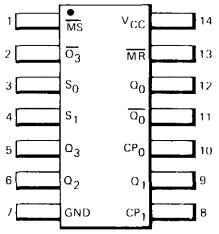


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)

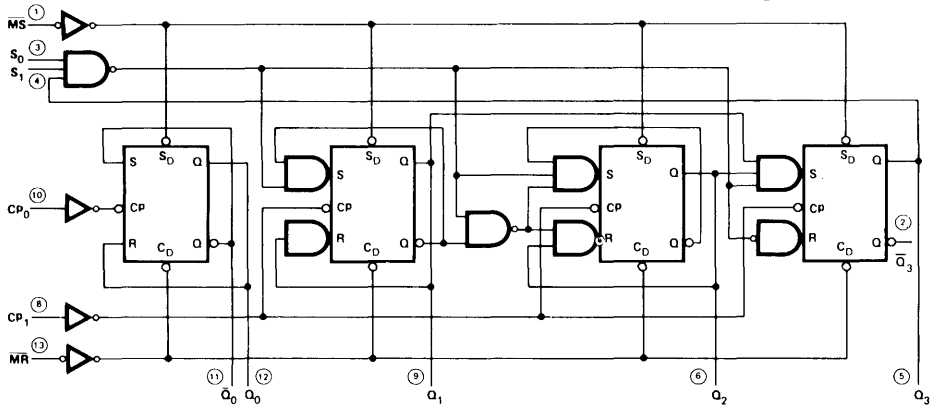


FLATPAK (TOP VIEW)



LOGIC DIAGRAM

○ = Pin Numbers



TTL/MSI 9307
SEVEN SEGMENT DECODER

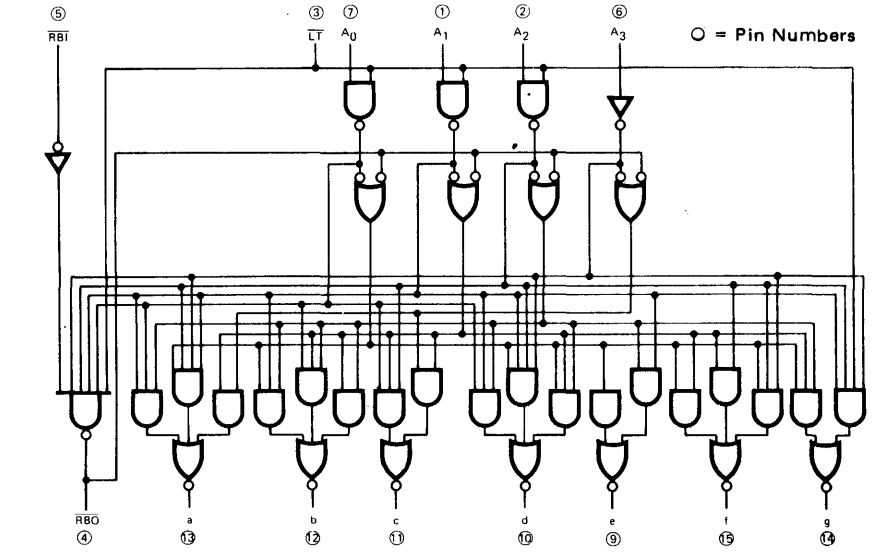
DESCRIPTION – The 9307 is a Seven Segment Decoder designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used with seven segment incandescent lamp, neon, electro-luminescent, or CRT numeric displays. The 9307 is compatible with all other Fairchild TTL devices.

- **TTL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROES**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE HIGH OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**

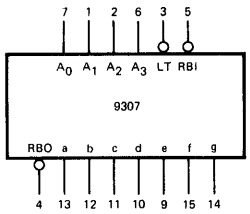
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} value
Input Voltage (dc)	−0.5 V to +5.5 V

LOGIC DIAGRAM

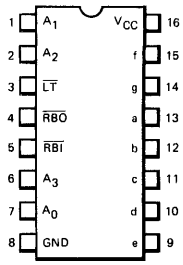


LOGIC SYMBOL

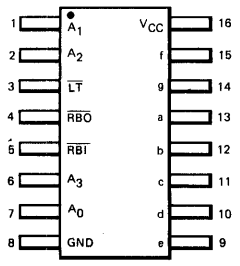


V_{CC}=PIN 16
GND=PIN 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



The 9307 seven segment decoder accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0–9. The seven outputs (a, b, c, d, e, f, g) of the decoder select the corresponding segments in the matrix shown in Figure 1. The numeric designations chosen to represent the decimal numbers are shown in Figure 3, together with the resulting displays for input code configurations in excess of binary nine.

The decoder has active HIGH outputs so that a buffer transistor may be used directly to provide the high currents required for incandescent displays. If additional base drive current is required external resistors may be added from the supply voltage to the seven segment outputs of the decoders. The value of this resistor is constrained by the 10 mA current sinking capability of the output transistors of the circuit.

The device has provision for automatic blanking of the leading and/or trailing edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed integer fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03 . Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeroes.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and enables a check to be made on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of DTL gates.

SEGMENT DESIGNATION

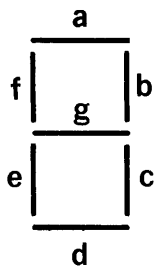


Fig. 1

TRUTH TABLE

$\overline{LT}$	$\overline{RB}$ IN	A_0	A_1	A_2	A_3	a	b	c	d	e	f	g	$\overline{RB}$ OUT	
L	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	L	L	L	L	L	L	L	L	L	L	L	L	L	0
H	H	L	L	L	L	H	H	H	H	H	H	L	H	0
H	X	H	L	L	L	L	H	H	L	L	L	L	H	1
H	X	L	H	L	L	H	H	L	H	H	L	H	H	2
H	X	H	H	L	L	H	H	H	H	L	L	H	H	3
H	X	L	L	H	L	L	H	H	L	L	L	H	H	4
H	X	H	L	H	L	H	L	H	H	L	H	H	H	5
H	X	L	H	H	L	H	L	H	H	H	H	H	H	6
H	X	H	H	H	L	H	H	H	L	L	L	L	H	7
H	X	L	L	L	H	H	H	H	H	H	H	H	H	8
H	X	H	L	L	H	H	H	H	H	L	H	H	H	9
H	X	L	H	L	H	L	L	L	H	H	L	H	H	10
H	X	H	H	L	H	L	L	L	H	L	L	H	H	11
H	X	L	L	H	H	L	H	H	L	L	H	H	H	12
H	X	H	L	H	H	H	L	H	H	L	H	H	H	13
H	X	L	H	H	H	L	L	L	H	H	H	H	H	14
H	X	H	H	H	H	L	L	L	L	L	L	L	H	15

H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

Fig. 2

NUMERICAL DESIGNATIONS

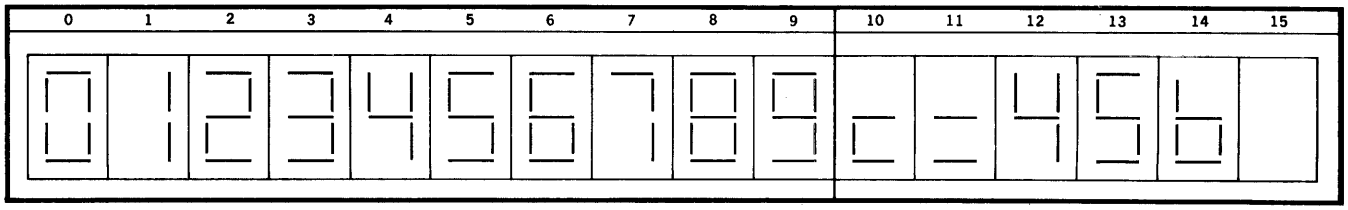


Fig. 3

Table 1 – LOADING RULES (1 U.L. = 1 DTL GATE INPUT LOAD)

Inputs	Loading (MIL & IND)	
	HIGH State	LOW State
A_0, A_1, A_2, A_3	1	1
$\overline{R}_{B(IN)}$	1	1/2
$\overline{LT}$	5	4.3

Outputs	Fan Out	
	MIL	IND
a, b, c, d, e, f, g	8	7
$\overline{R}_{B(OUT)}$	2.0	1.5

TABLE II – ELECTRICAL CHARACTERISTICS (T_A = –55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. 9307XM, see note)

SYMBOL	PARAMETER	LIMITS –55°C MIN.	LIMITS –55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	4.3 3.0		4.3 3.0	4.4 4.0		4.3 3.0		Volts	V_{CC} = 4.5 V I_{OH} = 0.0 mA (Pins 9-15) V_{CC} = 4.5 V I_{OH} = –70 μA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{OL}	Output LOW Voltage		0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V I_{OL} = 12.5 mA (Pins 9-15) I_{OL} = 3.1 mA (Pin 4) V_{CC} = 4.5 V I_{OL} = 10 mA (Pins 9-15) I_{OL} = 2.4 mA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{IH}	Input HIGH Voltage	2.1		1.9			1.7		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		1.4			1.1		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL} (Pin 3) I_{IL} (Pins 1, 2, 6, 7) I_{IL} (Pin 5)	Input LOW Current		–6.4 –1.5 –0.75			–6.4 –1.5 –0.75		–6.4 –1.5 –0.75	mA	V_{CC} = 5.5 V V_{IN} = 0.4 V Other Inputs = 5.5 V
I_{IH} (Pin 3) I_{IH} (Pins 1, 2, 5, 6, 7)	Input HIGH Current					10 2.0		25 5.0	μA	V_{CC} = 5.5 V V_{IN} = 4.5 V Ground on Other Inputs
I_A (Pins 9-15)	Available Output Current	–1.4		–1.4			–1.0		mA	V_{OUT} = 0.85 V V_{CC} = 4.5 V Inputs at Threshold Voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					–3.7			mA	V_{OUT} = 0.0 V V_{CC} = 5.5 V
I_{CC}	Supply Current		73			73		73	mA	V_{CC} = 5.5 V
t_{PLH}	Turn Off Delay					500			ns	V_{CC} = 5.0 V, See Fig. 5
t_{PHL}	Turn On Delay					500			ns	

TABLE III -- ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9307X C, see note)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	4.3 2.7		4.3 2.7	4.6 4.0		4.3 2.7		Volts	V_{CC} = 4.75 V I_{OH} = 0.0 mA (Pins 9-15) V_{CC} = 4.75 V I_{OH} = –70 μA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{OL}	Output LOW Voltage		0.45		0.21	0.45		0.45	Volts	V_{CC} = 5.25 V I_{OL} = 11.5 mA (Pins 9-15) I_{OL} = 2.75 mA (Pin 4) V_{CC} = 4.75 V I_{OL} = 10 mA (Pins 9-15) I_{OL} = 2.4 mA (Pin 4) Inputs at Threshold Voltages (V_{IL} or V_{IH})
V_{IH}	Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL} (Pin 3) I_{IL} (Pins 1, 2, 6, 7) I_{IL} (Pin 5)	Input LOW Current		–6.4 –1.5 –0.75			–6.4 –1.5 –0.75		–6.4 –1.5 –0.75	mA	V_{CC} = 5.25 V V_{IN} = 0.45 V Other Inputs = 5.25 V
I_{IH} (Pin 3) I_{IH} (Pins 1, 2, 5, 6, 7)	Input HIGH Current					25 5.0		50 10	μA	V_{CC} = 5.25 V V_{IN} = 4.5 V Ground on Other Inputs
I_A (Pins 9-15)	Available Output Current	–1.4		–1.4			–1.1		mA	V_{OUT} = 0.75 V V_{CC} = 4.75 V Inputs at Threshold Voltages (V_{IL} or V_{IH})
I_{SC} (Pins 9-15)	Short Circuit Current					–4.0			mA	V_{OUT} = 0.0 V V_{CC} = 5.25 V
I_{CC}	Supply Current		82			82		82	mA	V_{CC} = 5.25 V
t_{PLH}	Turn Off Delay					500			ns	V_{CC} = 5.0 V, See Fig. 5
t_{PHL}	Turn On Delay					500			ns	

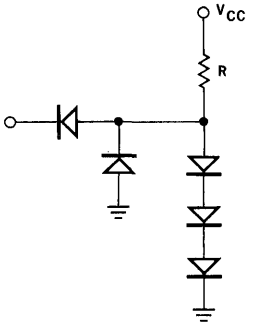
Note:
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

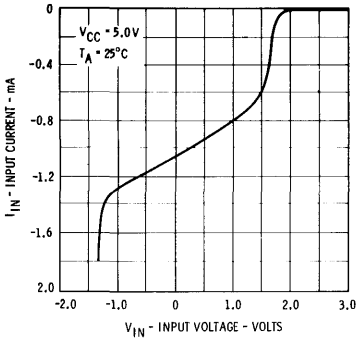
INPUTS

INPUT CURRENT VERSUS INPUT VOLTAGE

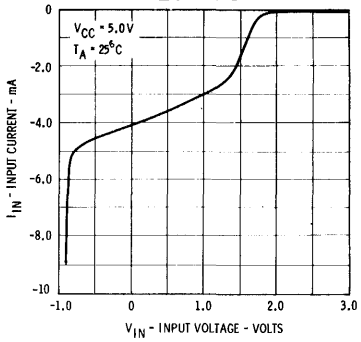
EQUIVALENT CIRCUIT



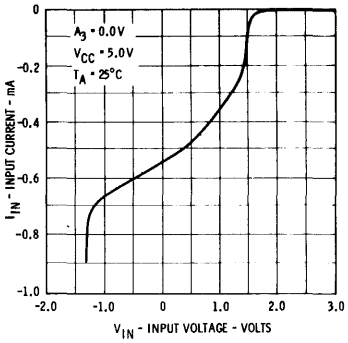
A_0, A_1, A_2, A_3 INPUTS



$\overline{LT}$ INPUT



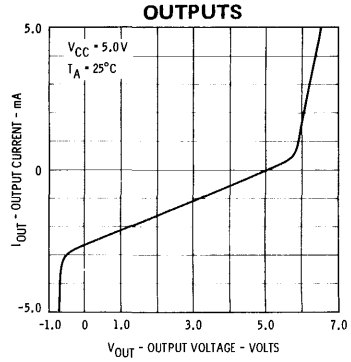
$\overline{RB}$(IN) INPUT



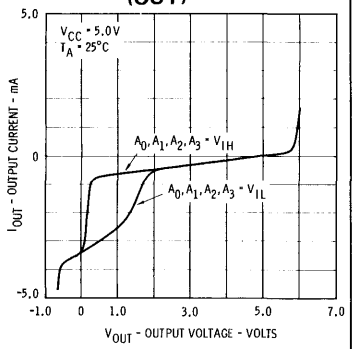
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

9307XM (−55°C to +125°C)
OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

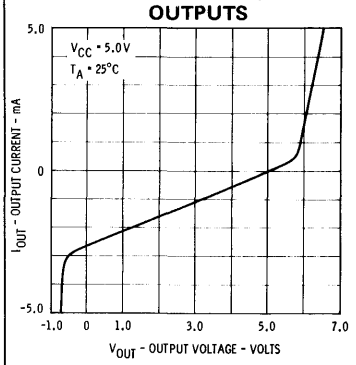


$\overline{RB}$(OUT) OUTPUT

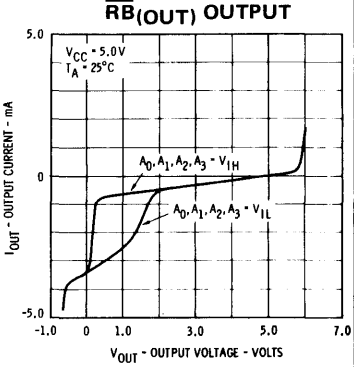


9307XC (0°C to +75°C)
OUTPUT IN HIGH STATE

a, b, c, d, e, f, g OUTPUTS

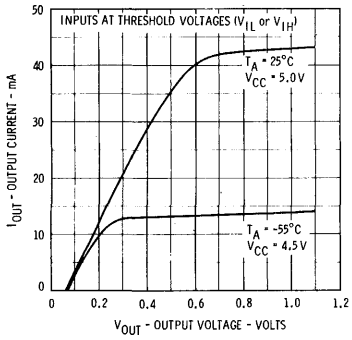


$\overline{RB}$(OUT) OUTPUT

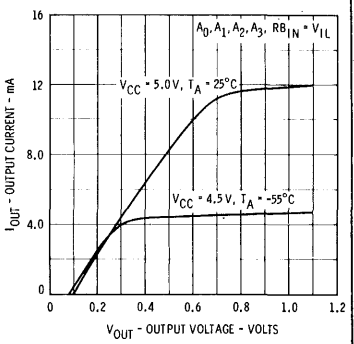


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS

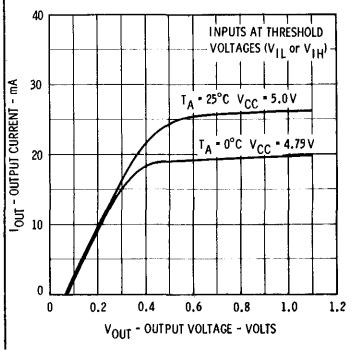


$\overline{RB}$(OUT) OUTPUT

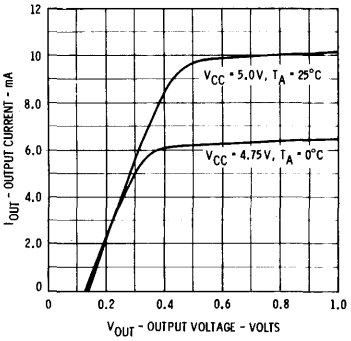


OUTPUT IN LOW STATE

a, b, c, d, e, f, g OUTPUTS



$\overline{RB}$(OUT) OUTPUT



OUTPUT

EQUIVALENT CIRCUIT

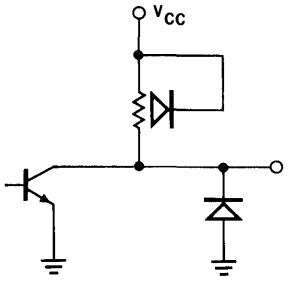


Fig. 4

SWITCHING WAVEFORMS

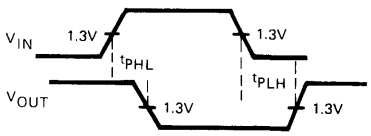


Fig. 5

8

TTL/MSI 9308
DUAL FOUR-BIT LATCH

DESCRIPTION — The MSI 9308 is a dual 4-Bit Latch designed for general purpose storage applications in high speed digital systems. The 9308 uses TTL technology and is compatible with DTL, TTL, and MSI families. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good ac noise immunity.

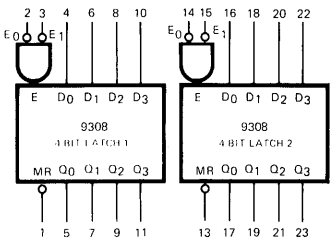
- ACTIVE LEVEL LOW ENABLE GATE INPUTS
- OVERRIDING MASTER RESET
- 25 ns THROUGH DELAY
- THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- HIGH CAPACITIVE DRIVE CAPABILITY
- ALL CERAMIC HERMETIC 24-LEAD DUAL IN-LINE PACKAGE

PIN NAMES

		LOADING (Note a)
D_0, D_1, D_2, D_3	Parallel Latch Inputs	1.5 U.L.
$\overline{E_0}, \overline{E_1}$	AND Enable (Active LOW) Inputs	1 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Latch Outputs (Note b)	9 U.L.

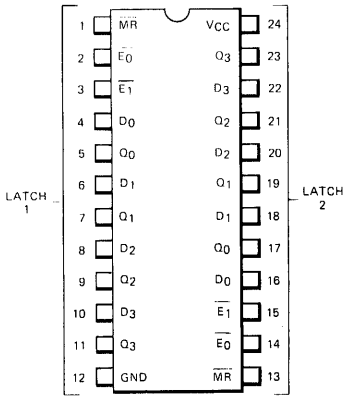
NOTES:
a. 1 unit load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. 9 U.L. is the output LOW drive factor and 18 U.L. is the output HIGH drive factor.

LOGIC SYMBOL

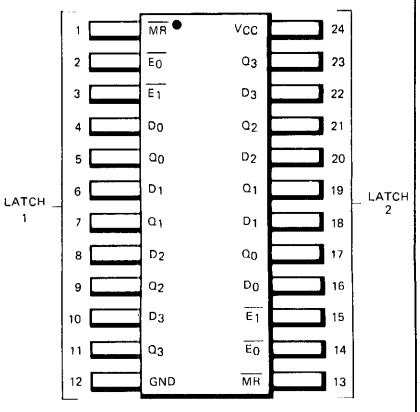


V_{CC} = Pin 24
GND = Pin 12

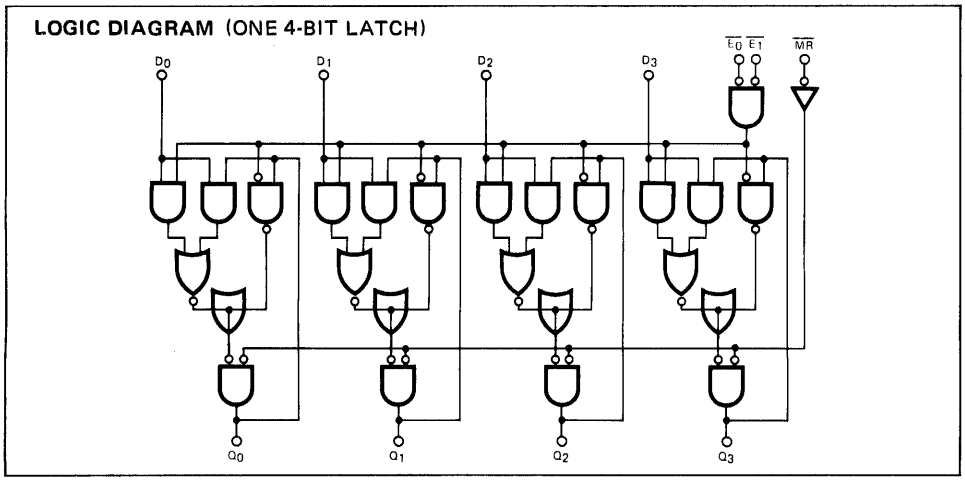
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM (ONE 4-BIT LATCH)



FUNCTIONAL DESCRIPTION

LATCH OPERATION – Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the master reset input.

TRUTH TABLE

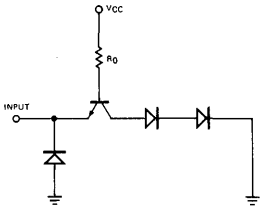
$\overline{MR}$	$\overline{E_0}$	$\overline{E_1}$	D	Q_n	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State
Q_n = Present Output State

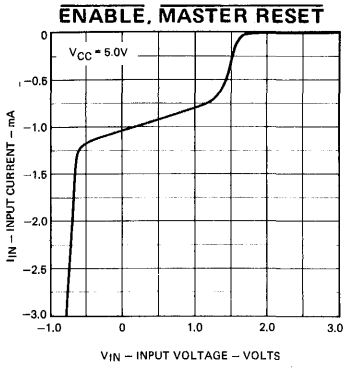
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

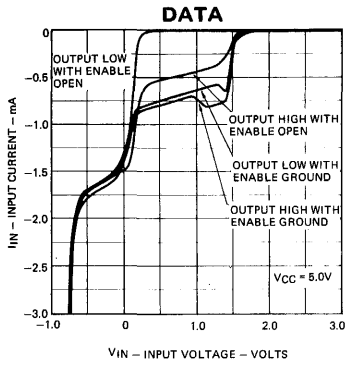
INPUTS

EQUIVALENT CIRCUIT



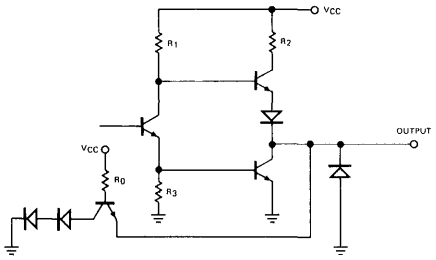
INPUT CURRENT VERSUS INPUT VOLTAGE



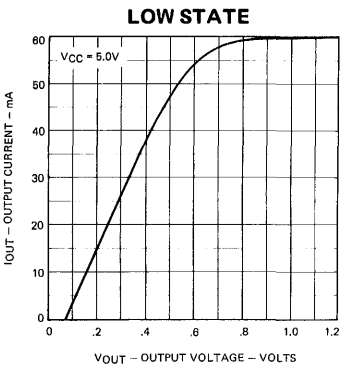


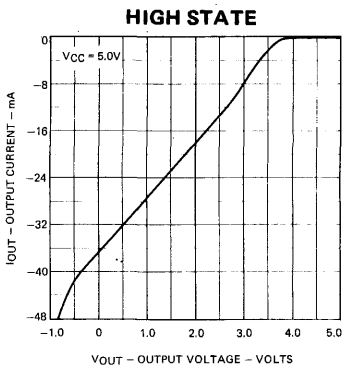
OUTPUTS

EQUIVALENT CIRCUIT



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE





8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9308XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9308XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −720 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 14.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current					V_{CC} = MAX., V_{IN} = 2.4V
	$\overline{E_0}$, $\overline{E_1}$ & $\overline{MR}$		10	40	μA	
	D_0, D_1, D_2 & D_3		15	60	μA	
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current					V_{CC} = MAX., V_{IN} = 0.4V
	$\overline{E_0}$, $\overline{E_1}$ & $\overline{MR}$		−0.96	−1.6	mA	
	D_0, D_1, D_2 & D_3		−1.44	−2.4*	mA	* Max Instantaneous Current Out of The D Inputs
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−70	mA	V_{CC} = MAX. V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		62	100	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9308XM(MIL)			9308XC(IND)			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX	MIN.	TYP.	MAX.			
t_{PLH}	Turn off Delay Enable to Output			30			35	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15pF
t_{PHL}	Turn on Delay Enable to Output			18			22	ns		
t_{PLH}	Turn off Delay Data to Output			20			23	ns	Fig. 2	
t_{PHL}	Turn on Delay Data To Output			18			20	ns		
t_{PHL}	Turn on Delay $\overline{MR}$ to Output			20			22	ns	Fig. 5	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	9308XM(MIL)			9308XC(IND)			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
t_s(H)	Set-up Time HIGH Data to Enable	6.0	1.0		10	1.0		ns	Fig. 3	V_{CC} = 5.0 V
t_h(H)	Hold Time HIGH Data to Enable	−4.0	-7.0		−2.0	-7.0		ns		
t_s(L)	Set-up Time LOW Data to Enable	10	7.0		12	7.0		ns		
t_h(L)	Hold Time LOW Data to Enable	4.0	-1.0		8.0	-1.0		ns		
t_{pw} $\overline{E}$	Enable Pulse Width	15			18			ns	Fig. 4	
t_{pw} $\overline{MR}$	Master Reset Pulse Width	15			18			ns	Fig. 5	
t_{rec}	Recovery Time Master Reset to Enable	10			12			ns	Fig. 6	

SET UP TIME: t_s is defined as the time required for the logic level to be present at the Data Input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.

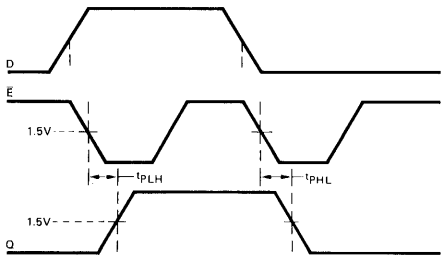
HOLD TIME: t_h is defined as the minimum time following the Enable transition from LOW to HIGH that the logic level must be maintained at the data input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable transition from LOW to HIGH and still be recognized.

RECOVERY TIME: t_{rec} is defined as the time that the Enable must remain LOW after the Master Reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data.

SWITCHING CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to Pin 24 and Pin 12 grounded. Outputs under test are loaded with 15 pF (includes jig and probe). Pins not referenced are not connected.

Fig. 1 – t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



OTHER CONDITIONS: $\overline{MR}$ = H

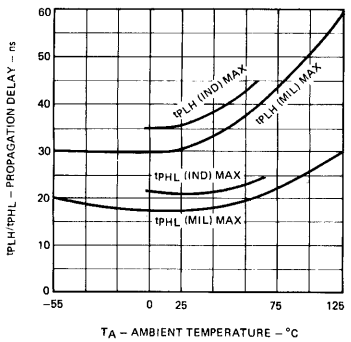
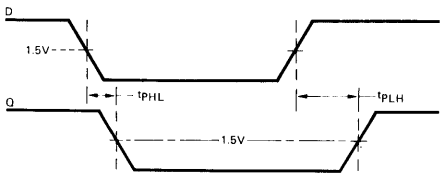
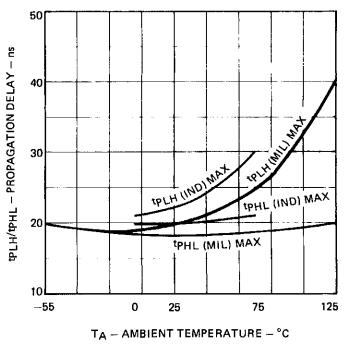


Fig. 2 – t_{PLH}/t_{PHL} (DATA TO OUTPUT)



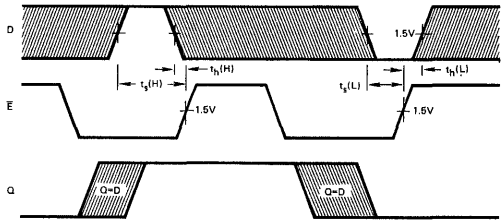
OTHER CONDITIONS $\overline{E}$ = L, $\overline{MR}$ = H



8

SWITCHING CHARACTERISTICS

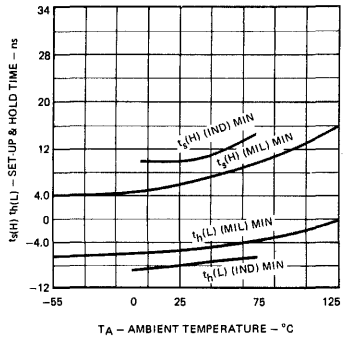
Fig. 3 – SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE



OTHER CONDITIONS: $\overline{MR}$ = H

The shaded areas indicate when the Data input is permitted to change for predictable output performance.

NOTE: The polarities of the t_h(H) and t_h(L) values are inverted on the graphs. This representation allows the graphs to show the true distribution of the $t_{(set\text{-}up)}$ parameters.



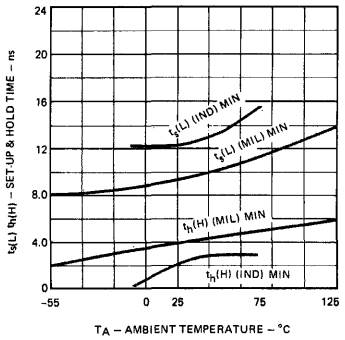
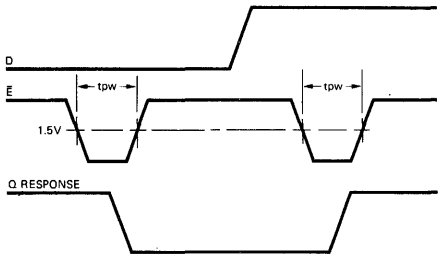


Fig. 4 – t_{pw} (MIN. ENABLE PULSE WIDTH)



OTHER CONDITION: $\overline{MR}$ = H

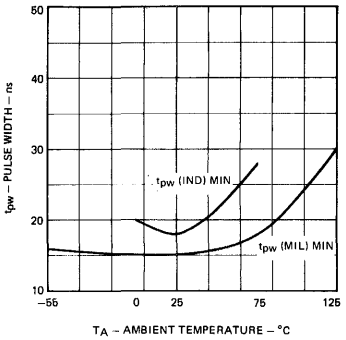
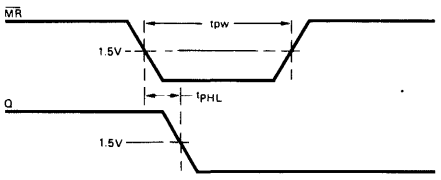


Fig. 5 – t_{pw} (MIN. MASTER RESET PULSE WIDTH) t_{PHL} (MASTER RESET TO OUTPUT)



OTHER CONDITIONS: D = H, Ē = L

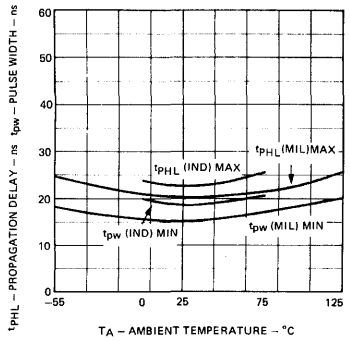
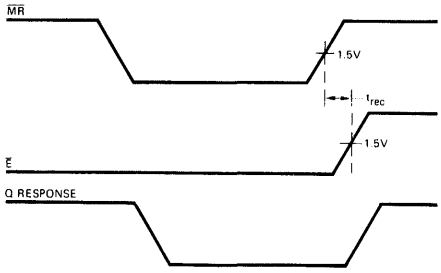
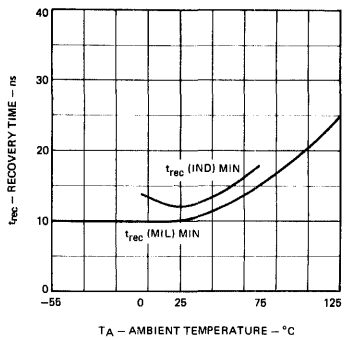


Fig. 6 – t_{rec} (MASTER RESET RECOVERY TIME)



OTHER CONDITIONS: D = H



LPTTL/MSI 93L08
LOW POWER DUAL FOUR-BIT LATCH

DESCRIPTION The LPTTL/MSI 93L08 is a Dual 4-Bit Latch designed for general purpose storage applications in medium speed digital systems. The 93L08 uses TTL technology and is TTL compatible. All inputs incorporate diode clamps to ground to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitive drive and low impedance outputs in both logic states to provide good ac noise immunity.

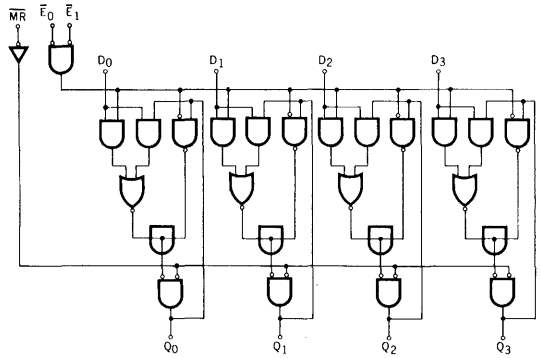
- **ACTIVE LEVEL LOW ENABLE GATE INPUTS**
- **OVERRIDING MASTER RESET**
- **TYPICAL PROPAGATION DELAY OF 53 ns**
- **TYPICAL POWER DISSIPATION OF 100 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 24-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

		LOADING HIGH	LOADING LOW
D_0, D_1, D_2, D_3	Parallel Latch Inputs	0.75 U.L.	0.375 U.L.
$\overline{E}$	AND Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Latch Outputs	9.0 U.L.	2.25 U.L.

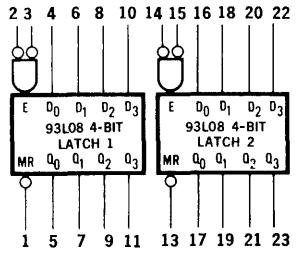
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM



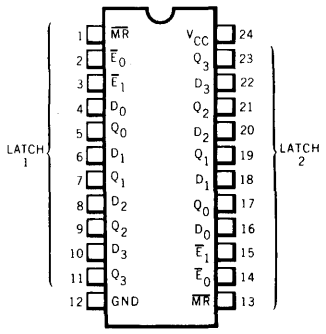
NOTE: Only one 4-Bit Latch shown.

LOGIC SYMBOL

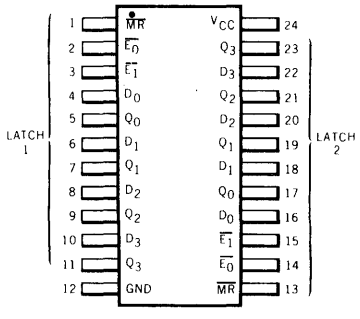


V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

LATCH OPERATION – Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the master reset input.

TRUTH TABLE

$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_0	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level

Q_{n-1} = Previous Output State
Q_n = Present Output State

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L08XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L08XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 5)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.36 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All INputs
I_{IL}	Input LOW Current $\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
	Input LOW Current D_0, D_1, D_2 & D_3		−0.38	−0.64	mA	V_{CC} = MAX., V_{IN} = 0 V (See Note 4)
I_{IH}	Input HIGH Current $\overline{E}_0$, $\overline{E}_1$ & $\overline{MR}$ D_0, D_1, D_2 & D_3		2.0 3.0	20 30	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 6)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		20	33	mA	V_{CC} = MAX., All Outputs LOW, Pins 2 & 14 GND, Other Inputs Open

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. This current is measured at V_{IN} = 0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.3 V is 0.6 mA.
5. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
6. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTIC	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
t_{PLH}	Enable to Output		35	60	ns	Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Enable to Output		30	50			
t_{PLH}	Data to Output		30	50	ns	Fig. 2	
t_{PHL}	Data to Output		35	55			
t_{PHL}	Master Reset to Output		31	55	ns	Fig. 5	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

t_s (H)	HIGH Data to Enable	25	15		ns	Fig. 3	V_{CC} = 5.0 V
t_s (L)	LOW Data to Enable	35	22				
t_h (H)	HIGH Data to Enable	0			ns	Fig. 3	
t_h (L)	LOW Data to Enable	0					
$t_{pw}\overline{E}$	Enable Pulse Width	45	30		ns	Fig. 4	
$t_{pw}\overline{MR}$	Master Reset Pulse Width	40	25		ns	Fig. 5	
t_{rec}	Master Reset Recovery Time	30			ns	Fig. 6	

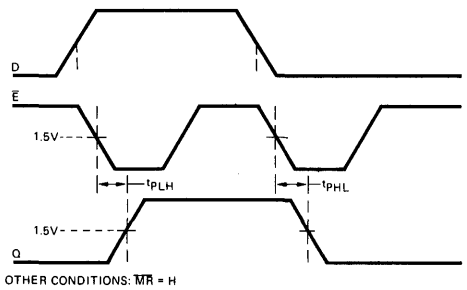
SET UP TIME: t_s is defined as the time required for the logic level to be present at the data input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.

HOLD TIME: t_h is defined as the minimum time following the Enable transition from LOW to HIGH that the logic level must be maintained at the data input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable transition from LOW to HIGH and still be recognized.

RECOVERY TIME: t_{rec} is defined as the time that the enable must remain LOW after the master reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data.

SWITCHING WAVEFORMS

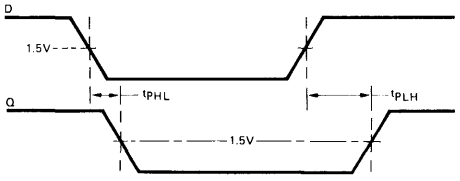
t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



OTHER CONDITIONS: $\overline{MR}$ = H

Fig. 1

t_{PLH}/t_{PHL} (DATA TO OUTPUT)

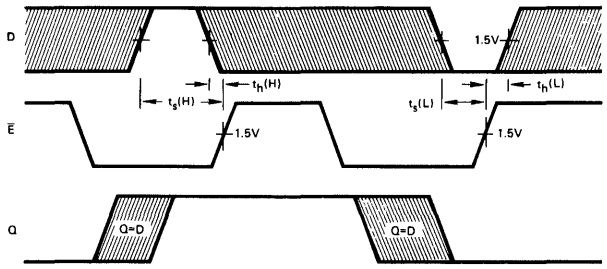


OTHER CONDITIONS: $\overline{E}$ = L, $\overline{MR}$ = H

Fig. 2

SWITCHING WAVEFORMS (Cont'd)

SETUP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE

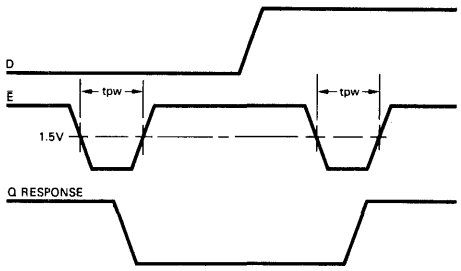


OTHER CONDITIONS: $\overline{MR}$ = H

The shaded areas indicate when the Data input is permitted to change to predictable output performance.

Fig. 3

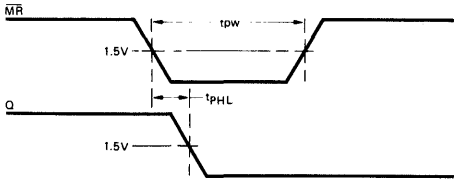
t_{pw} (MIN. ENABLE PULSE WIDTH)



OTHER CONDITIONS: $\overline{MR}$ = H

Fig. 4

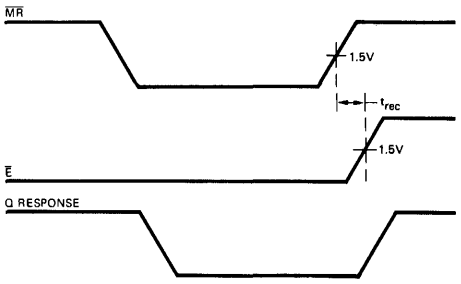
t_{pw} (MIN. MASTER RESET PULSE WIDTH)
t_{PHL} (MASTER RESET TO OUTPUT)



OTHER CONDITIONS: D = H, $\overline{E}$ = L

Fig. 5

t_{rec} (MASTER RESET RECOVERY TIME)



OTHER CONDITIONS: D = H

Fig. 6

TTL/MSI 9309
DUAL FOUR-INPUT MULTIPLEXER

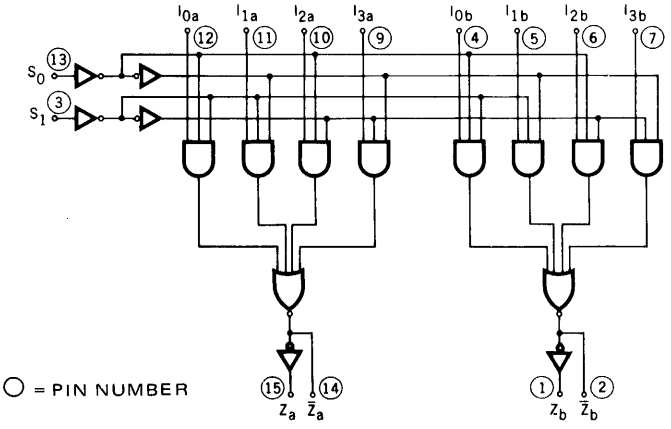
DESCRIPTION — The 9309 is a monolithic, high speed, Dual Four-Input digital Multiplexer circuit, consisting of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to multiplexer operation, the 9309 can generate any two function of three variables. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding, the 9309 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTL for high speed, high fan out operation and is compatible with all other members of the Fairchild TTL family.

- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

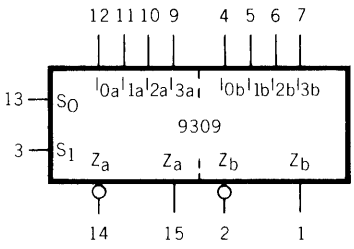
PIN NAMES		LOADING (Note a)
S_0, S_1	Common Select Inputs	1 U.L.
Multiplexer A		
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs	1 U.L.
Z_a	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}_a$	Complementary Multiplexer Output (Note c)	9 U.L.
Multiplexer B		
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs	1 U.L.
Z_b	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}_b$	Complementary Multiplexer Output (Note c)	9 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.
c. 9 U.L. is the output LOW drive factor and 18 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

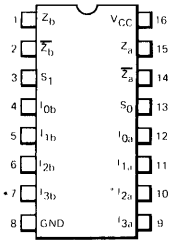


LOGIC SYMBOL

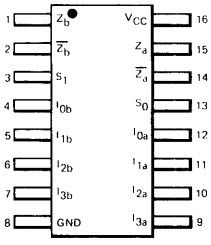


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The 9309 dual four-input multiplexer is a member of the Fairchild family of compatible medium scale integrated (MSI) digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 9309 dual four-input multiplexer is the logical implementation of a two-pole four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$Z_a = I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot S_1 \cdot S_0$

$Z_b = I_{0b} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot S_1 \cdot S_0$

A common use of the 9309 would be the moving of data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious use is as a function generator. The 9309 can generate any two functions of three variables. This is useful for implementing random gating functions.

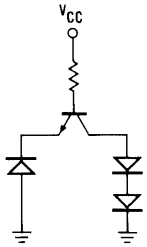
TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	$\overline{Z}_a$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	$\overline{Z}_b$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

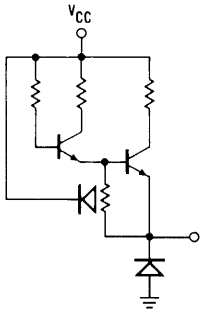
L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Logic Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

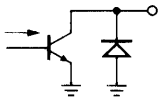
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

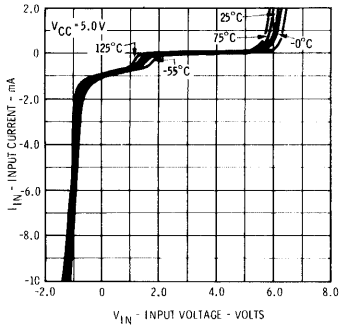


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

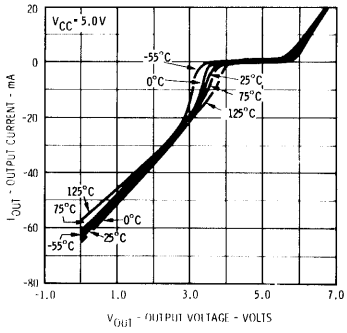


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

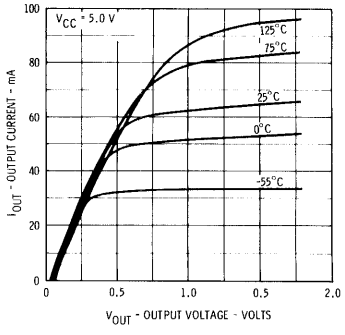


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30mA to +5.0mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9309XM	4.5 V	5.0 V	5.5 V	-55°C to 125°C
9309XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN	TYP (Note 4)	MAX		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = -12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = -800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		-0.96	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-20	-40	-70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		30	44	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0V, 25°C and maximum loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

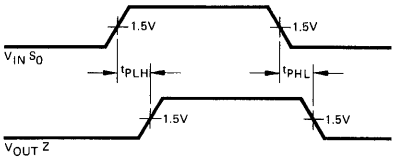
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output (S_0 to Z_a)		24	32	ns	V_{CC} = 5.0 V C_L = 15 pF (See Fig. 4)
t_{PHL}	Turn On Delay Input to Output (S_0 to Z_a)		24	32	ns	

8

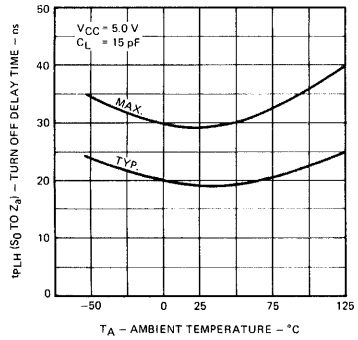
SWITCHING CHARACTERISTICS

Fig. 4

t_{PLH}/t_{PHL} S_0 to Z_a



TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to Z_a)



TURN ON DELAY TIME VERSUS TEMPERATURE (S_0 to Z_a)

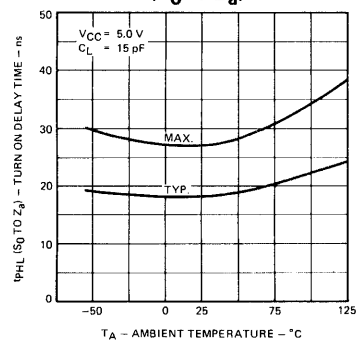
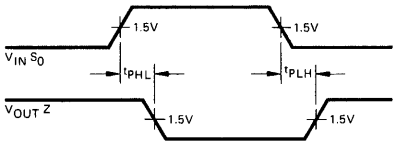
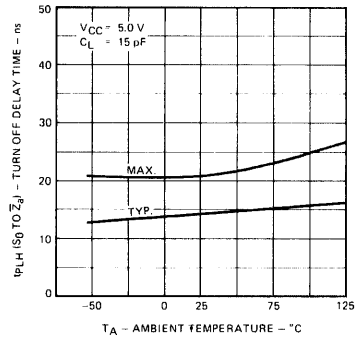


Fig. 5

t_{PLH}/t_{PHL} S_0 to $\bar{Z}_a$



TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\bar{Z}_a$)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S_0 to $\bar{Z}_a$)

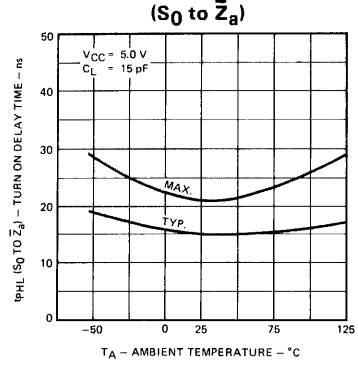
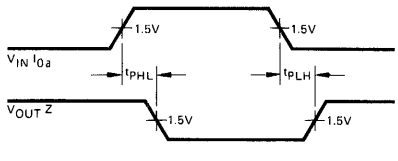
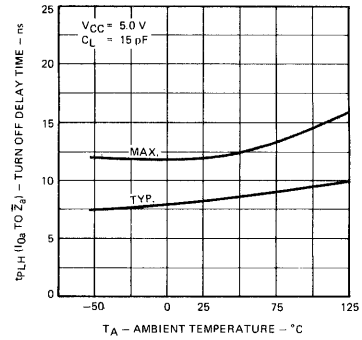


Fig. 6

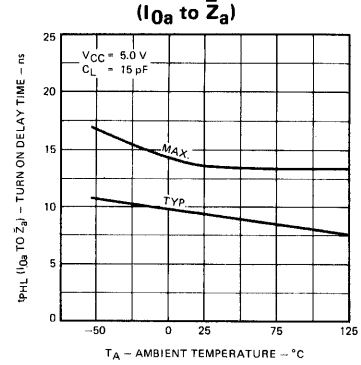
t_{PLH}/t_{PHL} I_{0a} to $\bar{Z}_a$



TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\bar{Z}_a$)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_{0a} to $\bar{Z}_a$)



LPTTL/MSI 93L09

LOW POWER DUAL FOUR-INPUT MULTIPLEXER

DESCRIPTION – The LPTTL/MSI 93L09 is a Monolithic, Medium Speed, Dual 4-Input Digital Multiplexer. It consists of two multiplexing circuits with common input select logic. Each circuit contains four inputs and fully buffered complementary outputs. In addition to operating as a multiplexer, the 93L09 can generate two functions of three variables. Active pullups in the outputs ensure good drive and speed performance. The 93L09 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output buss. The circuit uses TTL technology and is compatible with all other members of the TTL family.

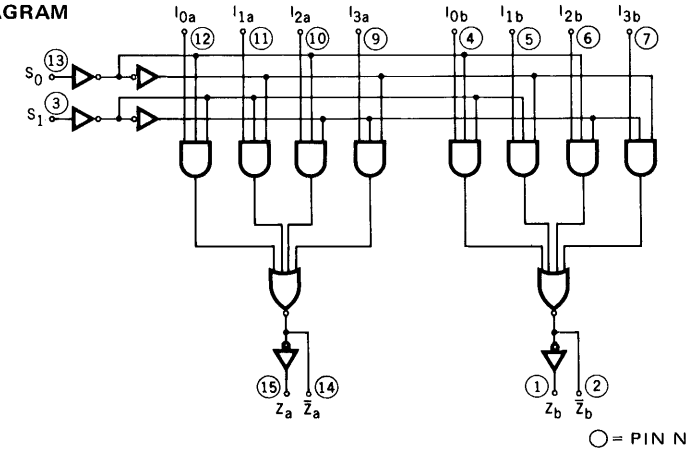
- MULTIFUNCTION CAPABILITY
- ON-CHIP SELECT LOGIC DECODING
- TYPICAL PROPAGATION DELAY OF 48 ns
- TYPICAL POWER DISSIPATION OF 40 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES

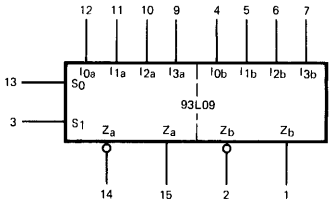
		LOADING	
		HIGH	LOW
S_0, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
Multiplexer A			
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_a	Multiplexer Output	10 U.L.	2.5 U.L.
$\overline{Z}_a$	Complementary Multiplexer Output	10 U.L.	2.25 U.L.
Multiplexer B			
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z_b	Multiplexer Output	10 U.L.	2.5 U.L.
$\overline{Z}_b$	Complementary Multiplexer Output	10 U.L.	2.25 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

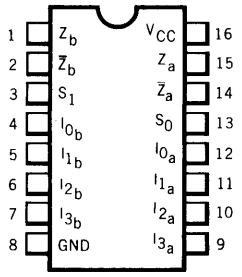


LOGIC SYMBOL

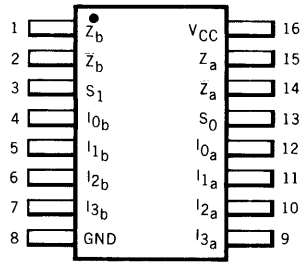


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION — The 93L09 dual 4-input multiplexer is a member of the Fairchild family of compatible low power medium scale integrated digital building blocks. It provides this family with the ability to select two bits of either data or control from up to four sources, in one package.

The 93L09 is the logical implementation of two-pole, four-position switch, with the position of the switch being set by the logic levels supplied to the two select inputs. Both assertion and negation outputs are provided for both multiplexers. The logic equations for the outputs are shown below:

$$Z_a = I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0$$
$$Z_b = I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0$$

The 93L09 is frequently used to move data from a group of registers to a common output buss. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The 93L09 can generate two functions of three variables. This is useful for implementing random gating functions.

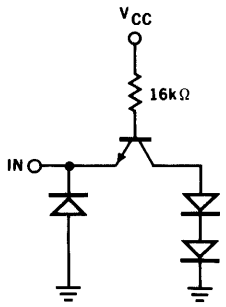
TRUTH TABLE

SELECT INPUTS		INPUTS				OUTPUTS	
S_0	S_1	I_{0a}	I_{1a}	I_{2a}	I_{3a}	Z_a	Z_a
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L
S_0	S_1	I_{0b}	I_{1b}	I_{2b}	I_{3b}	Z_b	Z_b
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

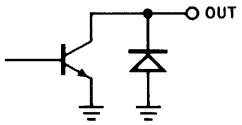
L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Logic Level

TYPICAL INPUT AND OUTPUT CIRCUITS

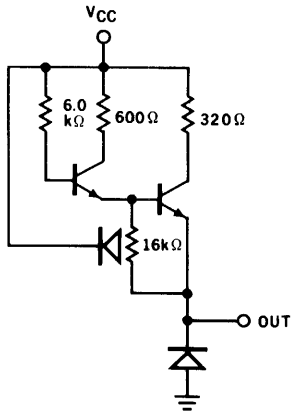
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L09XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L09XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pins 1 & 15) I_{OL} = 3.6 mA (Pins 2 & 14) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−10	−26	−40	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		7.5	11.5	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{PLH} (S_0 to Z_a)	Turn Off Delay Input to Output		35	55	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL} (S_0 to Z_a)	Turn On Delay Input to Output		32	50	ns	

8

TTL/MSI 9310•9316
BCD DECADE COUNTER/4-BIT BINARY COUNTER

DESCRIPTION — The 9310 is a High Speed Synchronous BCD Decade Counter and the 9316 is a High Speed Synchronous 4-Bit Binary Counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

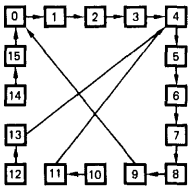
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **TYPICAL COUNTING FREQUENCY OF 45 MHz**
- **TYPICAL POWER DISSIPATION OF 325 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, AND TTL FAMILIES**
- **INPUT DIODE CLAMPING**
- **TTL COMPATIBLE**

PIN NAMES		**LOADING** (Note a)
$\overline{PE}$	Parallel Enable (Active LOW) Input	2 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	2/3 U.L.
CEP	Count Enable Parallel Input	1 U.L.
CET	Count Enable Trickle Input	2 U.L.
CP	Clock (Active HIGH Going Edge) Input	2 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs (Note b)	8 U.L.
TC	Terminal Count Outputs (Note c)	10 U.L.

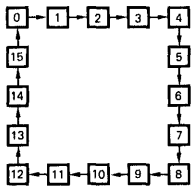
NOTES
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 8 U.L. is the output LOW drive factor and 16 U.L. is the output HIGH drive factor.
c. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

STATE DIAGRAM

9310



9316



LOGIC EQUATIONS

Count Enable = CEP • CET • PE

TC for 9310 = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3

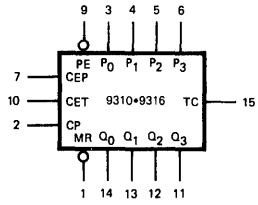
TC for 9316 = CET • Q_0 • Q_1 • Q_2 • Q_3

Preset = $\overline{PE}$ • CP+ (rising clock edge)

Reset = $\overline{MR}$

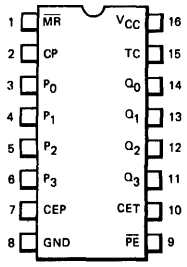
NOTE:
The 9310 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

LOGIC SYMBOL

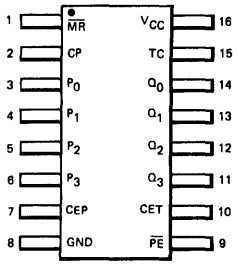


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 9310 is a high speed BCD decade counter, and the 9316 is a high speed binary counter. Both counters are fully synchronous with the clock pulse driving four master/slave flip-flops in parallel through a clock buffer. During the LOW to HIGH transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is HIGH, the masters are inhibited and the master/slave data path remains established. During the HIGH to LOW transition of the clock, the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic. (See Clock Pulse Characteristics Figure 7)

The three control inputs, Parallel Enable ($\overline{PE}$), Count Enable Parrallel (CEP), and Count Enable Trickle (CET), select the mode of operation as shown in the tables below. When the conditions for counting are satisfied, the rising edge of a clock pulse will change the counters to the next state of the count sequence shown in the State Diagram on the previous page. The Count Mode is enabled when CEP and CET inputs and $\overline{PE}$ are HIGH.

The 9310 and 9316 can be synchronously preset from the four Parallel inputs, (P_{0-3}) when $\overline{PE}$ is LOW. When the Parallel Enable and Clock are LOW, each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes HIGH, the masters are inhibited and this information is transferred to the slaves and reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when LOW.

Terminal count is HIGH when the counter is at terminal count (state 9 for 9310, and state 15 for 9316), and Count Enable Trickle is HIGH, as is shown in the logic equations. Without additional logic, multistage synchronous counting at high speeds is made possible with a high speed lookahead technique utilizing the count enable and terminal count logic. A multistage counter illustrating these techniques is shown and discussed in the application section.

When LOW, the asynchronous master reset overrides all other inputs resetting the four outputs LOW.

Conventional operation of the 9310 • 9316, as shown in the Mode Selection table, requires that the mode control inputs ($\overline{PE}$, CEP, CET) are stable while the clock is LOW. This is no constraint for a normal synchronous system where all signals are generated by the rising edge of the clock.

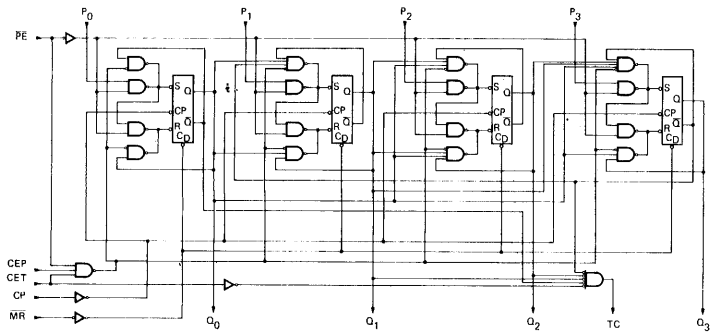
For some applications, the designer may want to change those inputs while the clock is LOW. In this case the 9310 • 9316 will behave in a predictable manner. For example:

If $\overline{PE}$ goes HIGH while the clock is LOW, but Count Enable is not active during the remaining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the $P_0 \ldots P_3$ data that existed at the set-up time before the rising edge of $\overline{PE}$.

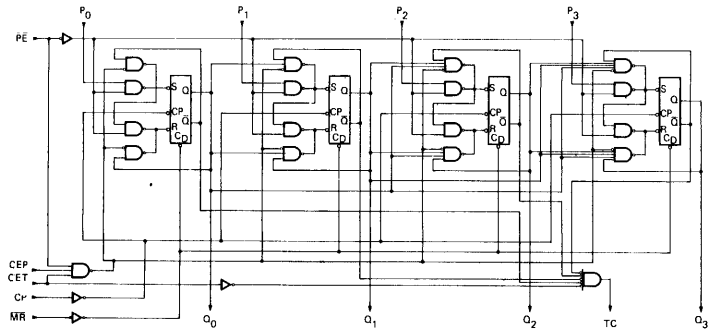
If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, but $\overline{PE}$ is HIGH (inactive) during the entire clock LOW period, the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the next count value.

If $\overline{PE}$ goes HIGH while the clock is LOW, but Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 9310 • 9316 will perform a mixture of counting and loading. On the LOW to HIGH clock transition, outputs $Q_0 \ldots Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

LOGIC DIAGRAM
9310



9316



9310 AND 9316
MODE SELECTION

$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

TERMINAL COUNT GENERATION

CET	9310 $(Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3)$	9316 $(Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3)$	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

$TC = CET \bullet Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$ (9310)

$TC = CET \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ (9316)

POSITIVE LOGIC = H = HIGH Voltage Level
L = LOW Voltage Level

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9310XM • 9316XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9310XC • 9316XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input Logical HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input Logical LOW Voltage for all Inputs	
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C	
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −640 μA for Q I_{OH} = −800 μA for TC V_{IN} = V_{IH} or V_{IL}	
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 12.8 mA for Q I_{OL} = 16 mA for TC V_{IN} = V_{IH} or V_{IL}	
I_{IH}	Input HIGH Current						
	$\overline{MR}$, CEP		10	40			
	CP, $\overline{PE}$, CET		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
	P_0, P_1, P_2 & P_3		7	27			
	Input HIGH Current all Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current						
	$\overline{MR}$, CEP		−0.96	−1.6			
	CP, $\overline{PE}$, CET		−1.92	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
	P_0, P_1, P_2 & P_3		−0.64	−1.07			
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−50	−80	mA	V_{CC} = MAX., V_{OUT} = 0 V	
I_{CC}	Power Supply Current		65	94	mA	9310XM • 9316XM	V_{CC} = MAX., MR = 0V
			65	100	mA	9310XC • 9316XC	Other Inputs HIGH

NOTES
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions testing, not shown in table, are chosen to guarantee operation under "worst case" conditions.
3. The Specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
t_{PLH}	Turn Off Delay CP to Q		12	20	ns	See Fig. 1	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn On Delay CP to Q		15	23	ns		
t_{PLH}	Turn Off Delay CP to TC		25	35	ns	See Fig. 4	
t_{PHL}	Turn On Delay CP to TC		13	22	ns		
t_{PLH}	Turn Off Delay CET to TC		13	19	ns	See Fig. 3	
t_{PHL}	Turn On Delay CET to TC		13	19	ns		
t_{PHL}	Turn On Delay $\overline{MR}$ to Q		30	45	ns	See Fig. 2	
f_{count}	Input Count Frequency	30	45		MHz	See Fig. 1	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
t_{rec}	Recovery Time for $\overline{MR}$	15	11		ns	See Fig. 2	V_{CC} = 5.0 V
$t_{pw}\overline{MR}$	Master Reset Pulse Width	30	23		ns		
$t_{pw}CP$	Clock Pulse Width	17	11		ns	See Fig. 1	
t_s(H) or (L)	Set-up Time Data to Clock	30	20		ns	See Fig. 5	
t_h(H) or (L)	Hold Time Data to Clock	0	−19		ns		
t_s(H)	Set-up Time (HIGH) CE to Clock	22	11		ns	See Fig. 6	
t_h(H)	Hold Time (HIGH) CE to Clock	See Note 6					
t_s(L)	Set-up Time (LOW) CE to Clock	See Note 6					
t_h(L)	Hold Time (LOW) CE to Clock	0	−10		ns		
t_s(H)	Set-up Time (HIGH) $\overline{PE}$ to Clock	See Note 7					
t_h(H)	Hold Time (HIGH) $\overline{PE}$ to Clock	− 7	−19		ns		
t_s(L)	Set-up Time (LOW) $\overline{PE}$ to Clock	30	20		ns		
t_h(L)	Hold Time (LOW) $\overline{PE}$ to Clock	See Note 7					

6. The Set-up Time "t_s(L)" and Hold Time "t_h(H)" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH to LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.
7. The Set-Up Time "t_s(H)" and Hold Time "t_h(L)" between the Parallel Enable (PE) and the Clock (CP) indicate that the LOW to HIGH transition of the PE must occur only while the Clock is HIGH for conventional operation.

DEFINITION OF TERMS:

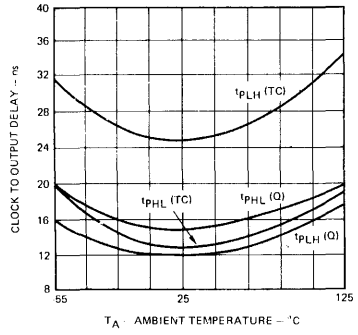
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

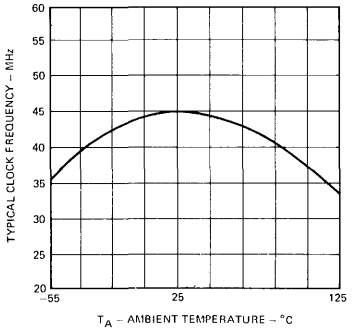
RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

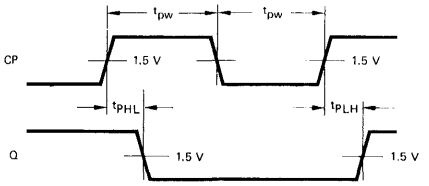
TYPICAL SWITCHING CHARACTERISTICS

PROPAGATION DELAY FROM CLOCK TO ANY OUTPUT VERSUS TEMPERATURE



FREQUENCY VERSUS TEMPERATURE

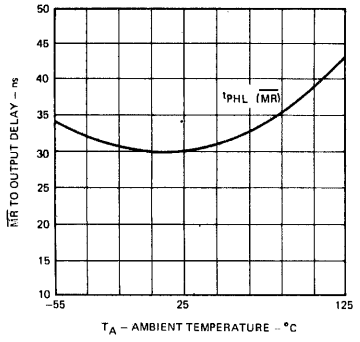


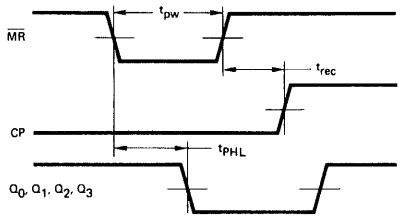


Other Conditions:
$\overline{PE}$ = $\overline{MR}$ = H
CEP = CET = H

Fig. 1 CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY AND CLOCK PULSE WIDTH

PROPAGATION DELAY FROM MASTER RESET TO OUTPUT VERSUS TEMPERATURE

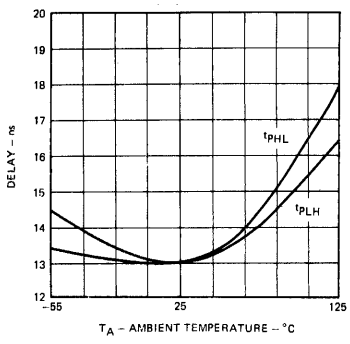


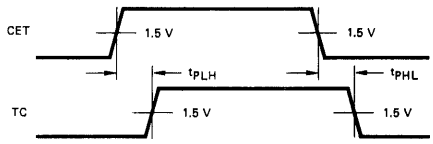


Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2. MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.

PROPAGATION DELAY COUNT ENABLE TERMINAL TO TERMINAL COUNT

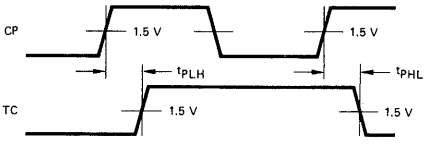




Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

The positive TC pulse occurs when the otuputs are in the ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) state for the 9310 and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the 9316.

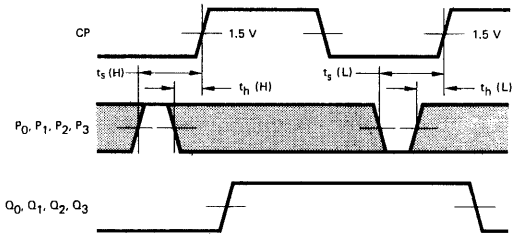
Fig. 3. COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS.



Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

The positive TC pulse is coincident with the output state ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) for the 9310 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the 9316.

Fig. 4. CLOCK TO TERMINAL COUNT DELAYS.



Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5. SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

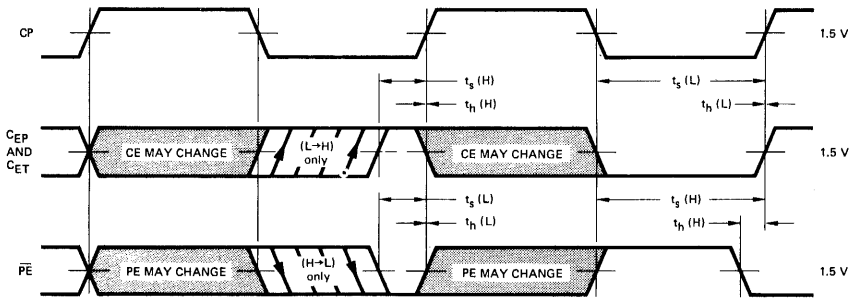
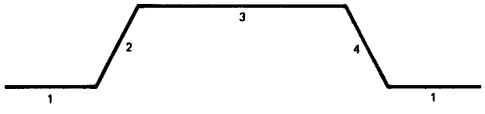


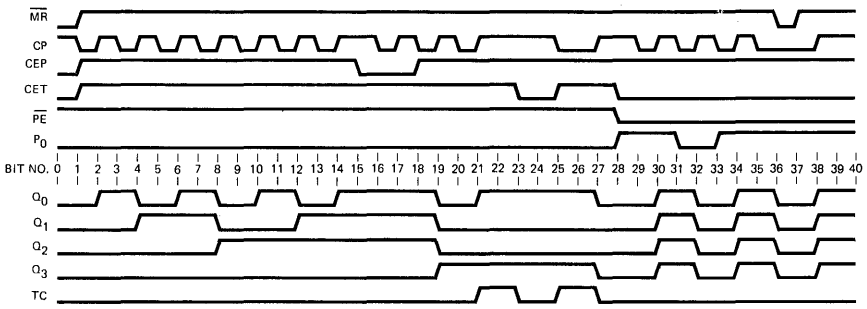
Fig. 6. SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

Fig. 7. CLOCK PULSE CHARACTERISTICS.



Region 1: Enter R&S data into master
Region 2: Inhibit R&S inputs, transfer data from master to slave
Region 3: Latch master and slave
Region 4: Isolate slave from master, enable R&S inputs

9310 GENERALIZED FUNCTION TEST



MULTISTAGE COUNTING — The 9310 • 9316 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in Figures 8 and 9.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The 9310 • 9316 internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, Figure 8. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in Figure 9 permits multistage counting up to 11 stages limited by the fan out of the terminal count. For an alternate scheme for more stages see Application Note 184.

The CEP input of the 9310 • 9316 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

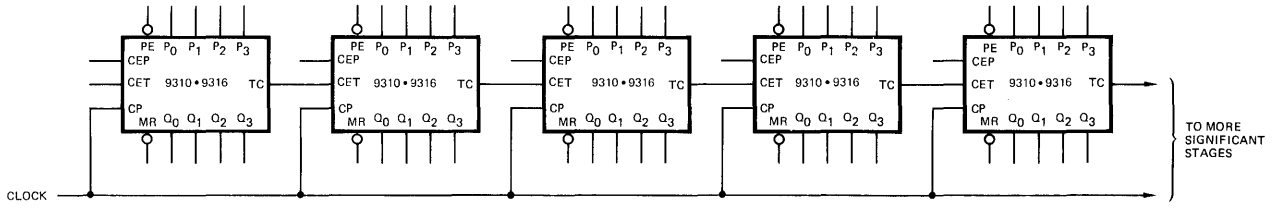


Fig. 8. SYNCHRONOUS MULTISTAGE COUNTING SCHEME (SLOW)

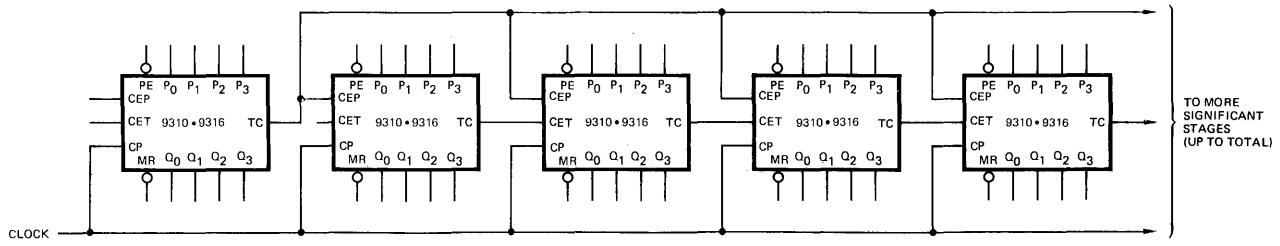


Fig. 9. SYNCHRONOUS MULTISTAGE COUNTING SCHEME (FAST)

LPTTL/MSI 93L10•93L16

LOW POWER BCD DECADE COUNTER/4-BIT BINARY COUNTER

DESCRIPTION – The **93L10** is a High Speed Synchronous BCD Decade Counter and the **93L16** is a High Speed Synchronous 4-Bit Binary Counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several stages of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **TYPICAL COUNTING FREQUENCY OF 20 MHz**
- **TYPICAL POWER DISSIPATION OF 85 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, AND TTL FAMILIES**
- **INPUT DIODE CLAMPING**
- **TTL COMPATIBLE**

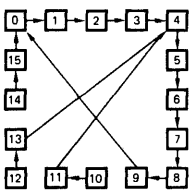
PIN NAMES

		LOADING HIGH	LOADING LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
P_0, P_1, P_2, P_3	Parallel Inputs	0.33 U.L.	0.17 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	1.0 U.L.	0.5 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	8.0 U.L.	2.0 U.L.
TC	Terminal Count Outputs	8.0 U.L.	2.0 U.L.

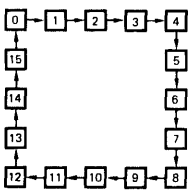
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

STATE DIAGRAM

93L10



93L16



LOGIC EQUATIONS

Count Enable = CEP • CET • PE

TC for 93L10 = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3

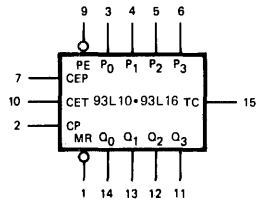
TC for 93L16 = CET • Q_0 • Q_1 • Q_2 • Q_3

Preset = $\overline{PE}$ • CP+ (rising clock edge)

Reset = $\overline{MR}$

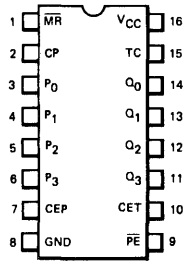
NOTE:
The **93L10** can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

LOGIC SYMBOL

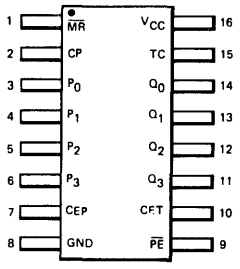


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION — The 93L10 is a high speed BCD Decade Counter, and the 93L16 is a high speed Binary Counter. Both counters are fully synchronous with the clock pulse driving four master/slave flip-flops in parallel through a clock buffer. During the LOW to HIGH transition of the clock, the master is inhibited from further change. After the masters are locked out, data is transferred from the master to the slaves and reflected at the outputs. When the clock is HIGH, the masters are inhibited and the master/slave data path remains established. During the HIGH to LOW transition of the clock, the slave is inhibited from further change, followed by the enabling of the masters for the acceptance of data from the counting logic or the parallel entry logic. (See Clock Pulse Characteristics **Figure 7.**)

The three control inputs, Parallel Enable ($\overline{PE}$), Count Enable Parrallel (CEP), and Count Enable Trickle (CET), select the mode of operation as shown in the tables below. When the conditions for counting are satisfied, the rising edge of a clock pulse will change the counters to the next state of the count sequence shown in the State Diagram on the previous page. The Count Mode is enabled when CEP and CET inputs and $\overline{PE}$ are HIGH.

The 93L10 and 93L16 can be synchronously preset from the four Parallel inputs, (P_{0-3}) when $\overline{PE}$ is LOW. When the Parallel Enable and Clock are LOW, each master of the flip-flops is connected to the appropriate parallel input (P_{0-3}) and the slaves (outputs) are steady in their previous state. When the clock goes HIGH, the masters are inhibited and this information is transferred to the slaves and reflected at the outputs. The parallel enable input overrides both count enable inputs, presetting the counter when LOW.

Terminal count is HIGH when the counter is at terminal count (state 9 for 93L10, and state 15 for 93L16), and Count Enable Trickle is HIGH, as is shown in the logic equations. Without additional logic, multistage synchronous counting at high speeds is made possible with a high speed lookahead technique utilizing the count enable and terminal count logic. A multistage counter illustrating these techniques is shown and discussed in the application section.

When LOW, the asynchronous master reset overrides all other inputs resetting the four outputs LOW.

Conventional operation of the 93L10•93L16, as shown in the Mode Selection table, requires that the mode control inputs ($\overline{PE}$, CEP, CET) are stable while the clock is LOW. This is no constraint for a normal synchronous system where all signals are generated by the rising edge of the clock.

For some applications, the designer may want to change those inputs while the clock is LOW. In this case the 93L10•93L16 will behave in a predictable manner. For example:

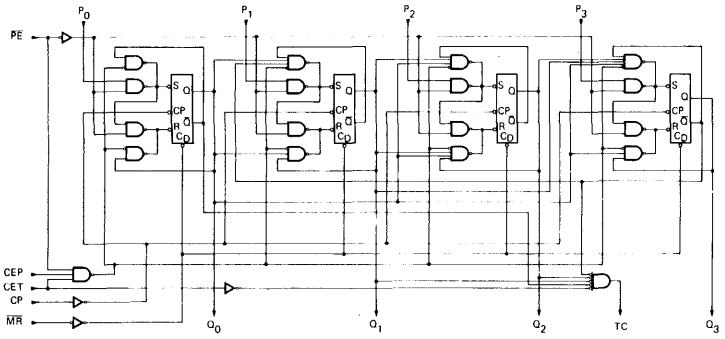
If $\overline{PE}$ goes HIGH while the clock is LOW, but Count Enable is not active during the remaining clock LOW period (i.e. CEP or CET are LOW), the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the $P_0 \ldots P_3$ data that existed at the set-up time before the rising edge of $\overline{PE}$.

If Count Enable is active (i.e. CEP and CET are HIGH) during some portion of the clock LOW period, but $\overline{PE}$ is HIGH (inactive) during the entire clock LOW period, the subsequent LOW to HIGH clock transition will change $Q_0 \ldots Q_3$ to the next count value.

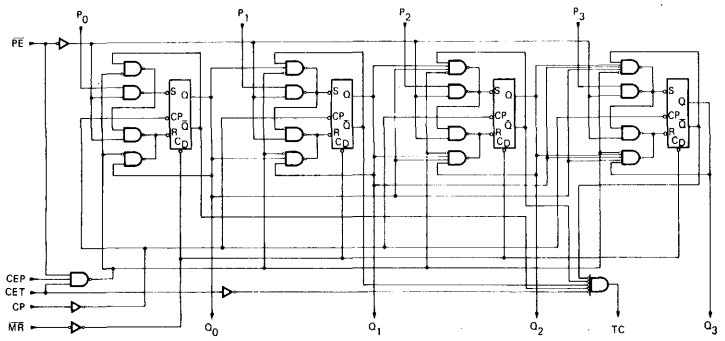
If $\overline{PE}$ goes HIGH while the clock is LOW, but Count Enable is active (CEP and CET are HIGH) during some portion of the remaining clock LOW period, the 93L10•93L16 will perform a mixture of counting and loading. On the LOW to HIGH clock transition, outputs $Q_0 \ldots Q_3$ will change as the count sequence or the loading requires. Only the outputs that would not change in the count sequence and are also reloaded with their present value stay constant.

LOGIC DIAGRAMS

93L10



93L16



93L10 AND 93L16
MODE SELECTION

$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

TERMINAL COUNT GENERATION

CET	93L10 ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$)	93L16 ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$)	TC
L	L	L	L
L	H	H	L
H	L	L	L
H	H	H	H

$TC = CET \bullet Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$ (93L10)

$TC = CET \bullet Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$ (93L16)

POSITIVE LOGIC = H = HIGH Voltage Level
L = LOW Voltage Level

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L10XM·93L16XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L10XC·93L16XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL}
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL}
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V
	$\overline{MR}$, CEP		−0.25	−0.40		
	CP, $\overline{PE}$, CET		−0.50	−0.80		
	P_0, P_1, P_2 & P_3		−0.13	−0.27		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	$\overline{MR}$, CEP		2.0	20		
	CP, $\overline{PE}$, CET		4.0	40		
	P_0, P_1, P_2 & P_3		1.0	13.3		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		17	27.5	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

COUNTING APPLICATIONS

For typical counting applications, see Multistage Counter and Synchronous Multistage Counting Scheme in 9310·9316 data sheet in TTL/ MSI section of this catalog.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
t_{PLH} t_{PHL}	Turn Off Delay CP to Q Turn On Delay CP to Q		20 26	32 39	ns ns	See Fig. 1	
t_{PLH} t_{PHL}	Turn Off Delay CP to TC Turn On Delay CP to TC		44 20	66 30	ns ns	See Fig. 4	V_{CC} = 5.0 V
t_{PLH} t_{PHL}	Turn Off Delay CET to TC Turn On Delay CET to TC		20 20	30 30	ns ns	See Fig. 3	C_L = 15 pF
t_{PHL}	Turn On Delay MR to Q		40	72	ns	See Fig. 2	
f_{count}	Input Count Frequency	13	23		MHz	See Fig. 1	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS	
t_{rec} $t_{pw}MR$	Recovery Time for MR Master Reset Pulse Width	30 35	20 20		ns ns	See Fig. 2	
$t_{pw}CP$	Clock Pulse Width	25	15		ns	See Fig. 1	
t_s(H) or (L) t_h(H) or (L)	Set-up Time Data to Clock Hold Time Data to Clock	75 0	50 −20		ns ns	See Fig. 5	
t_s(H)	Set-up Time (HIGH) CE to Clock	26	17		ns	See Fig. 6	V_{CC} = 5.0 V
t_h(H) t_s(L)	Hold Time (HIGH) CE to Clock Set-up Time (LOW) CE to Clock	See Note 6 See Note 6					
t_h(L)	Hold Time (LOW) CE to Clock	0	−17		ns		
t_s(H)	Set-up Time (HIGH) PE to Clock	See Note 7					
t_h(H)	Hold Time (HIGH) PE to Clock	0	−35		ns		
t_s(L)	Set-up Time (LOW) PE to Clock	53	35		ns		
t_h(L)	Hold Time (LOW) PE to Clock	See Note 7					

NOTES:

6. The Set-up Time "t_s(L)" and Hold Time "t_h(H)" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH to LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.
7. The Set-up Time "t_s(H)" and Hold Time "t_h(L)" between the Parallel Enable (PE) and the Clock (CP) indicate that the LOW to HIGH transition of the PE must occur only while the clock is HIGH for conventional operation.

DEFINITION OF TERMS:

SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

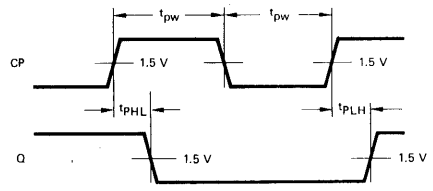
HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

8

SWITCHING CHARACTERISTICS

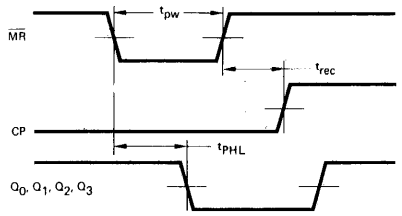
CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.



Other Conditions:
$\overline{PE}$ = $\overline{MR}$ = H
CEP = CET = H

Fig. 1

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME.



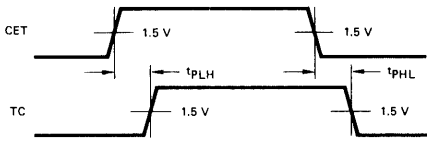
Other Conditions:
$\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

Fig. 2

SWITCHING CHARACTERISTICS (cont'd)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS.

The positive TC pulse occurs when the outputs are in the ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) state for the 93L10 and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the 93L16.

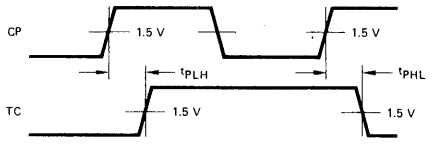


Other Conditions: CP = $\overline{PE}$ = CEP = $\overline{MR}$ = H

Fig. 3

CLOCK TO TERMINAL COUNT DELAYS.

The positive TC pulse is coincident with the output state ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) for the 93L10 and ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) for the 93L16.

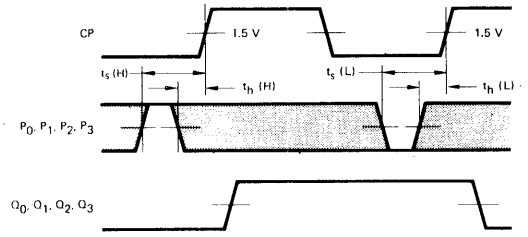


Other Conditions: $\overline{PE}$ = CEP = CET = $\overline{MR}$ = H

Fig. 4

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.



Other Conditions: $\overline{PE}$ = L, $\overline{MR}$ = H

Fig. 5

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE ($\overline{PE}$) INPUTS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

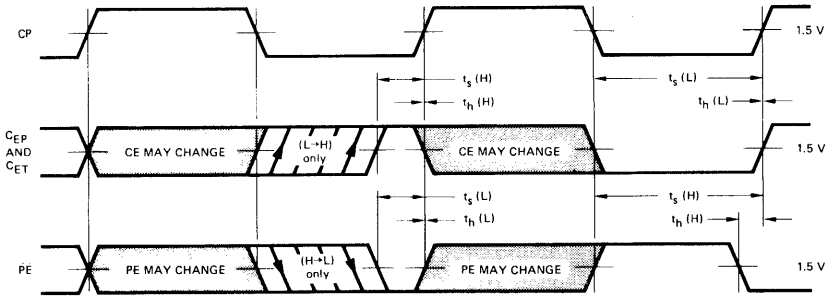


Fig. 6

CLOCK PULSE CHARACTERISTICS.

Region 1: Enter R&S data into master
Region 2: Inhibit R&S inputs, transfer data from master to slave
Region 3: Latch master and slave
Region 4: Isolate slave from master, enable R&S inputs

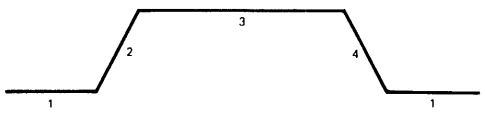


Fig. 7

TTL/MSI 93S10 •93S16

BCD DECADE COUNTER/4-BIT BINARY COUNTER

TO BE ANNOUNCED

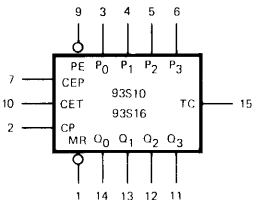
DESCRIPTION — The 93S10 is a super high speed synchronous BCD Decade Counter and the 93S16 is a super high speed synchronous 4-Bit Binary Counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several stages of sunchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique. Each device utilizes Schottky TTL processing to achieve the ultra high speeds.

- **TYPICAL COUNTING FREQUENCY OF 100 MHz**
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **THE INPUT/OUPTUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, AND TTL FAMILIES**
- **INPUT DIODE CLAMPING**

PIN NAMES

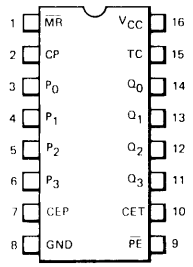
$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0, P_1, P_2, P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH) Going Edge Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
TC	Terminal Count Outputs

LOGIC SYMBOL

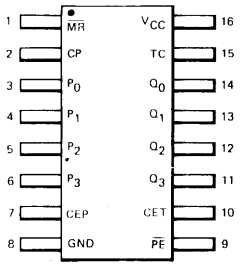


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)

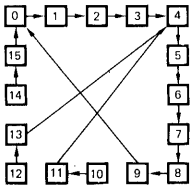


FLATPAK (TOP VIEW)

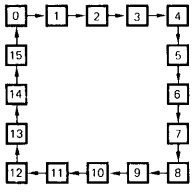


STATE DIAGRAM

93S10



93S16



LOGIC EQUATIONS

Count Enable = CEP • CET • PE

TC for 93S10 = CET • Q_0 • $\overline{Q}_1$ • $\overline{Q}_2$ • Q_3

TC for 93S16 = CET • Q_0 • Q_1 • Q_2 • Q_3

Preset = $\overline{PE}$ • CP+ (rising clock edge)

Reset = $\overline{MR}$

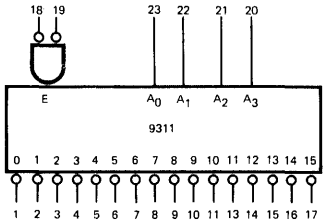
NOTE:
The 93S10 can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

TTL/MSI 9311
ONE-OF-SIXTEEN DECODER/DEMULTIPLEXER

DESCRIPTION — The 9311 is a TTL/MSI Multi-Purpose Decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTL for high speed and high fan out capability, and is compatible with all members of the Fairchild TTL family.

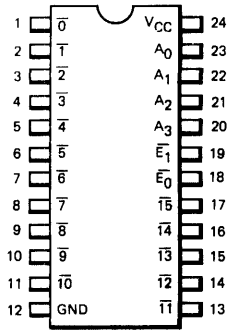
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 175 mW**
- **INPUT CLAMP DIODES**
- **2-INPUT ENABLE GATE**
- **TTL COMPATIBLE**

LOGIC SYMBOL



V_{CC} = PIN 24
GND = PIN 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)

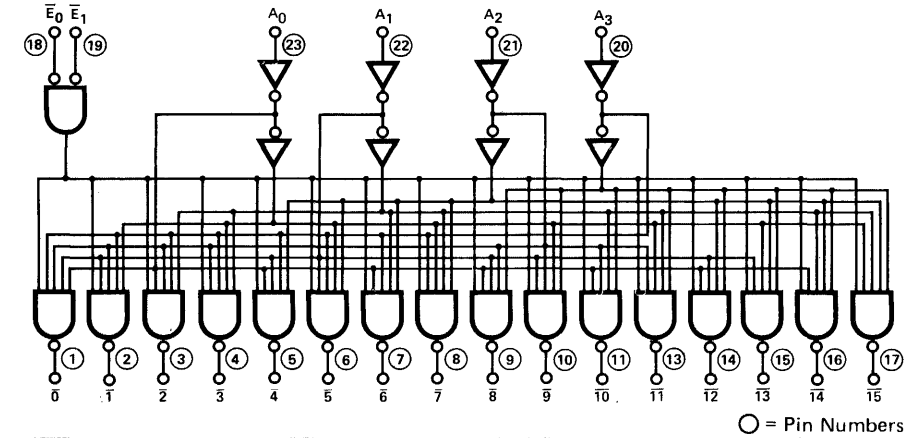


PIN NAMES

		LOADING (Note a)
A_0, A_1, A_2, A_3	Address Inputs	1 U.L.
$\overline{E}_0$, $\overline{E}_1$	AND Enable (Active LOW) Inputs	1 U.L.
$\overline{0}$ to $\overline{15}$	(Active LOW) Outputs (Note b)	10 U.L.

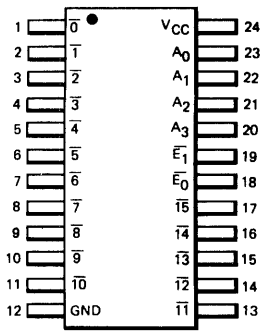
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



○ = Pin Numbers

FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION — The 9311 decoder accepts four inputs and provides 16 mutually exclusive active LOW outputs, as shown by the logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enable.

The 9311 can demultiplex data by routing it from one input to one of 16 possible decoder outputs. The desired output is addressed and the data is applied to one of the enable inputs. Providing that the other enable is LOW, the addressed output will follow the state of the applied data.

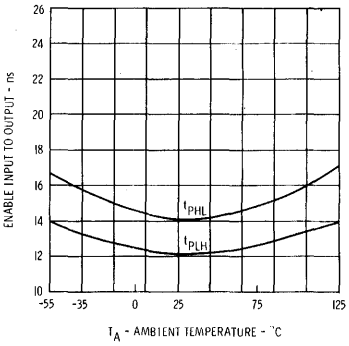
TRUTH TABLE

$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

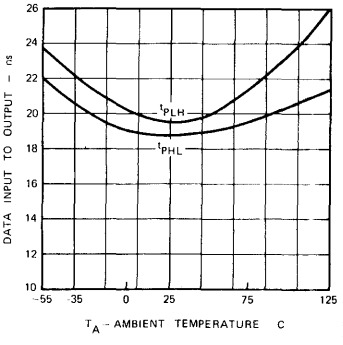
H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

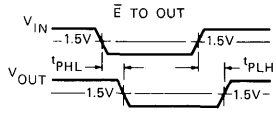
TYPICAL SWITCHING PERFORMANCE

PROPAGATION DELAY ENABLE INPUT TO OUTPUT VERSUS TEMPERATURE



PROPAGATION DELAY DATA INPUT TO OUTPUT VERSUS TEMPERATURE





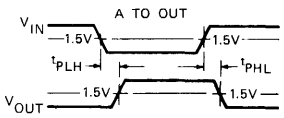
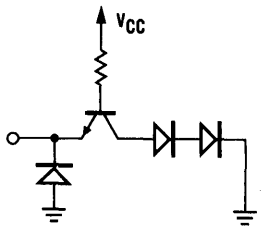


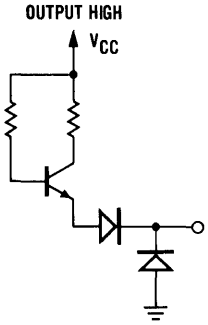
Fig. 1.

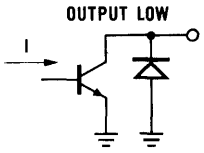
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUIT





INPUT CURRENT VERSUS INPUT VOLTAGE

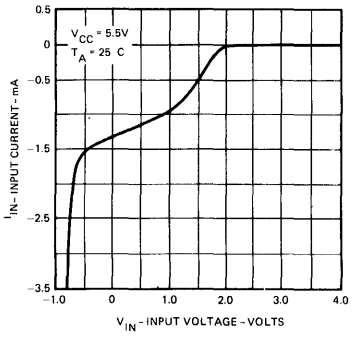


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

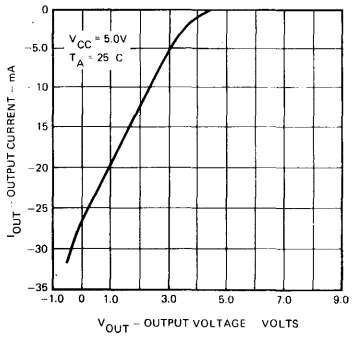


Fig. 3.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

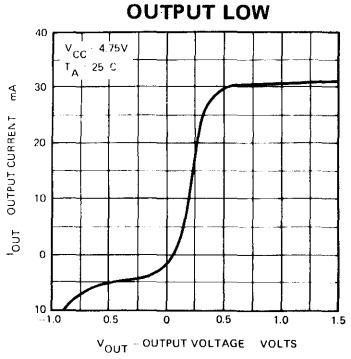


Fig. 4.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9311XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9311XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		35	62	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9311XM			9311XC			UNITS	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay A Input to Output		19	28		19	31	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay A Input to Output		19	25		19	28		C_L = 15 pF
t_{PLH}	Turn Off Delay $\overline{E}$ Input to Output		12	20		12	23	ns	Pin 12 = GND
t_{PHL}	Turn On Delay $\overline{E}$ Input to Output		14	21		14	24		(See Fig. 1)

LPTTL/MSI 93L11

LOW POWER ONE-OF-SIXTEEN DECODER

DESCRIPTION – The LPTTL/MSI 93L11 is a Multi-Purpose Decoder designed to accept four inputs and provide 16 mutually exclusive outputs. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

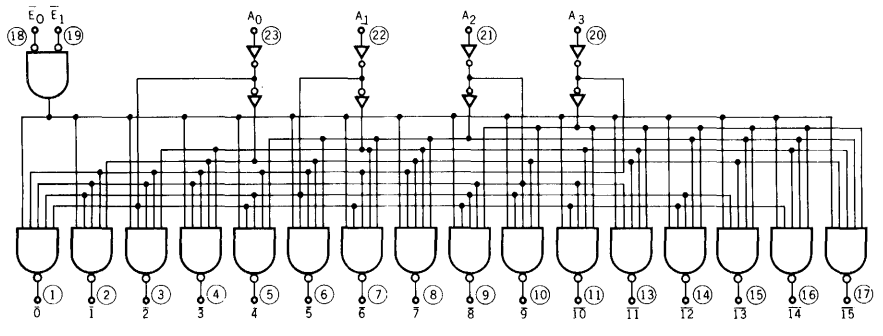
- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TWO INPUT ENABLE GATE**
- **TYPICAL PROPAGATION DELAY OF 70 ns**
- **TYPICAL POWER DISSIPATION OF 58 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 24-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

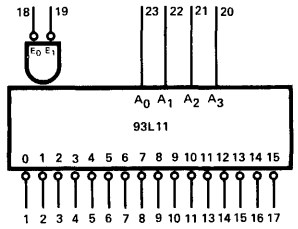
		LOADING	
		HIGH	LOW
A_0, A_1, A_2, A_3	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}_0$, $\overline{E}_1$	AND Enable (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{15}$	(Active LOW) Outputs	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM



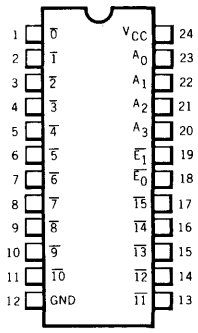
LOGIC SYMBOL



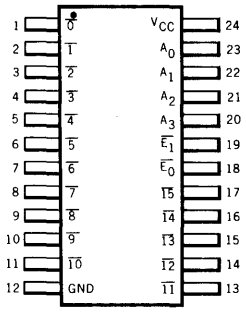
V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAMS

DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The 93L11 decoder accepts four active HIGH binary inputs and provides 16 mutually exclusive active LOW outputs, as shown by logic symbol. The active LOW outputs facilitate addressing other MSI units with active LOW enables.

The 93L11 can demultiplex data by routing it from one input to one of sixteen possible decoder outputs. The desired output is addressed and the data is applied to one of the enable inputs. When the other enable is LOW, the addressed output will follow the state of the applied data.

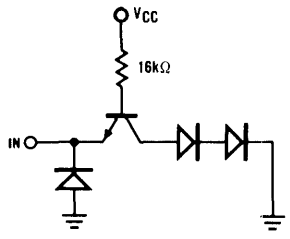
TRUTH TABLE

$\overline{E}_0$	$\overline{E}_1$	A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{10}$	$\overline{11}$	$\overline{12}$	$\overline{13}$	$\overline{14}$	$\overline{15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

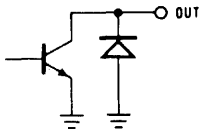
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

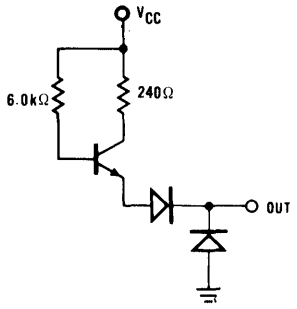


OUTPUTS
EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L11XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L11XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		11.5	16.5	mA	V_{CC} = MAX.

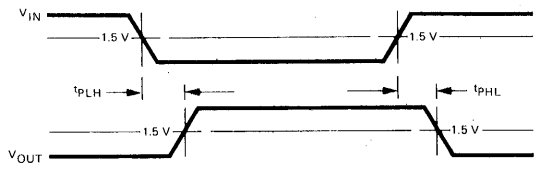
NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay A Input to Output		50	75	ns	V_{CC} = 5.0 V C_L = 15 pF See Fig. 1
t_{PHL}	Turn On Delay A Input to Output		60	85	ns	
t_{PLH}	Turn Off Delay $\overline{E}$ Input to Output		30	60	ns	
t_{PHL}	Turn On Delay $\overline{E}$ Input to Output		43	65	ns	

SWITCHING TIME WAVEFORMS

A INPUT TO OUTPUT



$\overline{E}$ INPUT TO OUTPUT

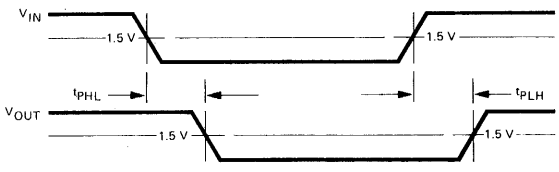


Fig. 1.

TTL/MSI 9312
EIGHT-INPUT MULTIPLEXER

DESCRIPTION — The 9312 is a monolithic, high speed, Eight-Input digital Multiplexer circuit. It provides in one package the ability to select one bit of data from up to eight sources. The 9312 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with all other members of the Fairchild TTL family.

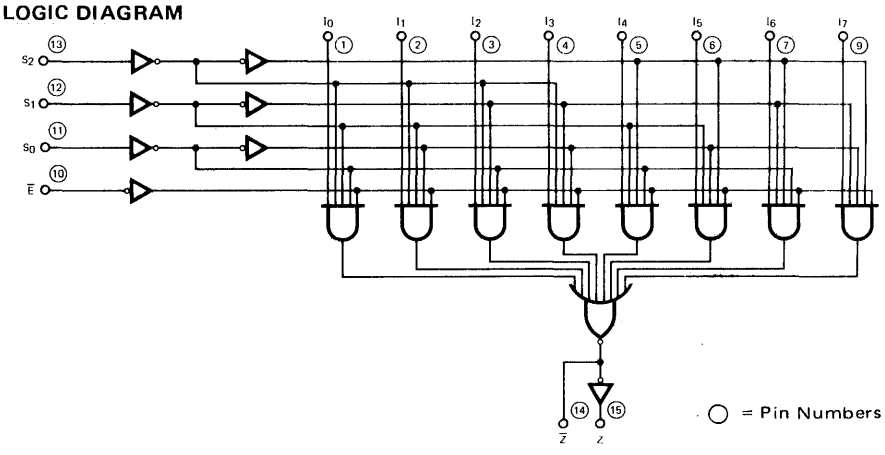
- **MULTIFUNCTION CAPABILITY**
- **25 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, and MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

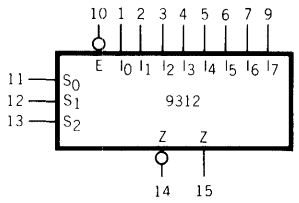
		LOADING (Note a)
S_0, S_1, S_2	Select Inputs	1 U.L.
$\overline{E}$	Enable (Active LOW) Input	1 U.L.
I_0 to I_7	Multiplexer Inputs	1 U.L.
Z	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}$	Complementary Multiplexer Output (Note b)	10 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

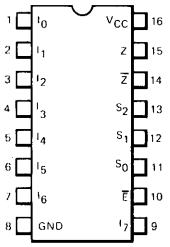


LOGIC SYMBOL

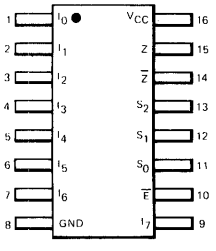


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 9312 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three Select Inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable Input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Z = E \cdot (I_0 \cdot \overline{S_0} \cdot \overline{S_1} \cdot \overline{S_2} + I_1 \cdot S_0 \cdot \overline{S_1} \cdot \overline{S_2} + I_2 \cdot \overline{S_0} \cdot S_1 \cdot \overline{S_2} + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S_2} + I_4 \cdot \overline{S_0} \cdot \overline{S_1} \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S_1} \cdot S_2 + I_6 \cdot \overline{S_0} \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The 9312 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9312 can provide any logic function of four variables and its negation. Thus any number of random logic elements used to generate unusual truth tables can be replaced by one 9312.

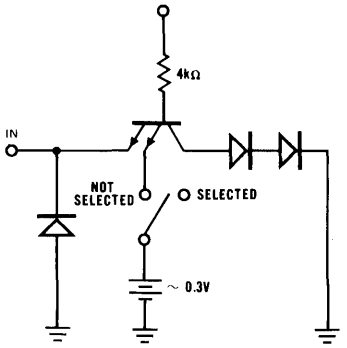
TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

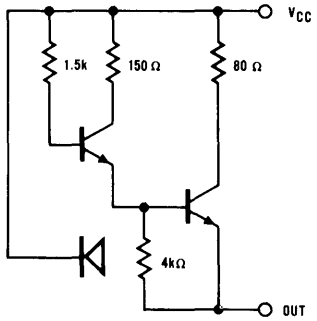
H = HIGH voltage level
L = LOW voltage level
X = Level does not affect output.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

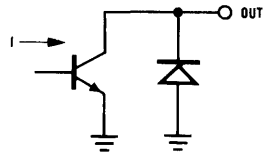
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

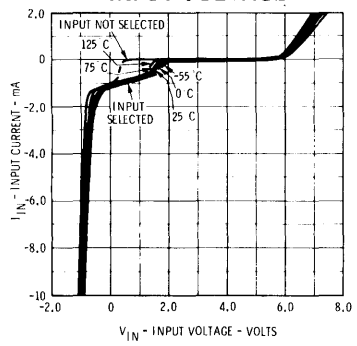


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

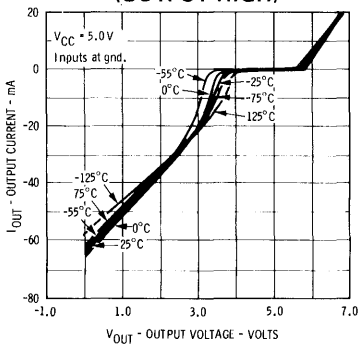


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

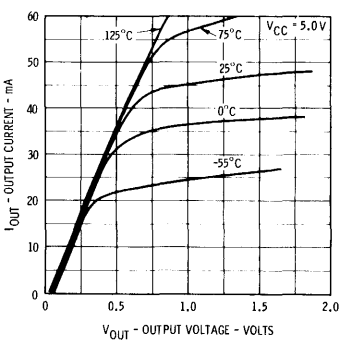


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30mA to +5.0mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9312XM	4.5V	5.0V	5.5V	-55°C to 125°C
9312XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC}=MIN., I_{IN}=-12mA, T_A=25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = -800μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0V
I_{IL}	Input LOW Current		-0.96	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-30	-60	-100	mA	V_{CC} = MAX., V_{OUT} = 0.0V
I_{CC}	Power Supply Current		27	44	mA	V_{CC} = MAX.

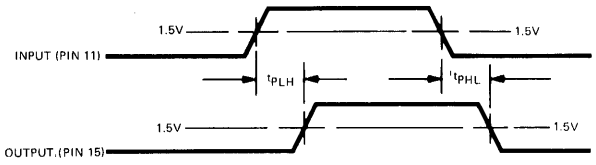
NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output (S_0 to Z)		23	34	ns	V_{CC} = 5.0V C_L = 15 pF (See following page)
t_{PHL}	Turn On Delay Input to Output (S_0 to Z)		25	36	ns	

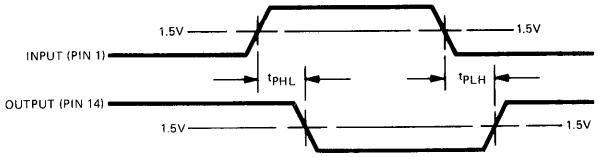
SWITCHING CHARACTERISTICS

t_{PLH}/t_{PHL} : S_0 to Z



OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1 kΩ
Pin 16 = V_{CC}

t_{PLH}/t_{PHL} : I_0 to $\bar{Z}$



OTHER CONDITIONS: Pins 8, 10, 11, 12, 13 = GND
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

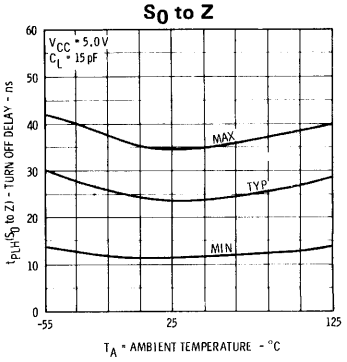


Fig. 4

TURN ON DELAY VERSUS AMBIENT TEMPERATURE: S_0 to Z

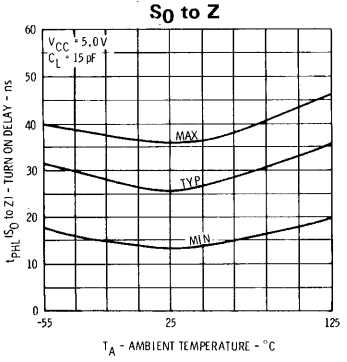


Fig. 5

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\bar{Z}$

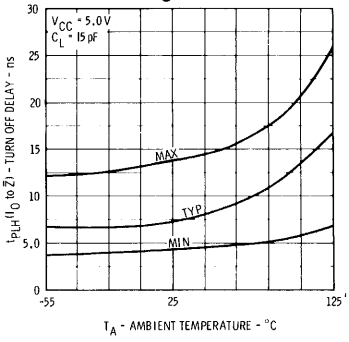


Fig. 6

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to $\bar{Z}$

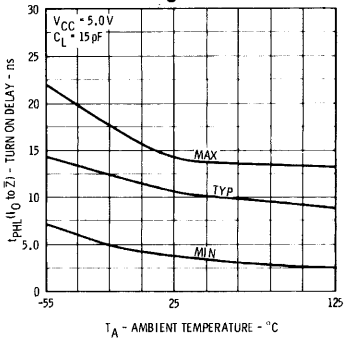
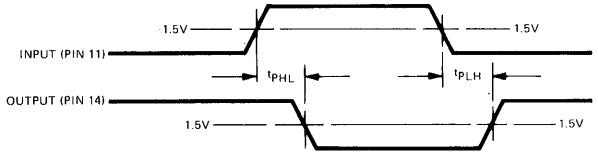


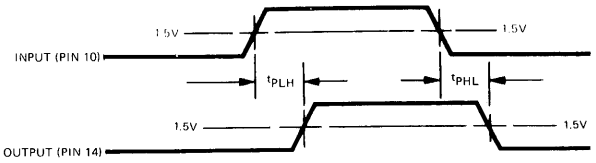
Fig. 7

t_{PLH}/t_{PHL}: S_0 to $\bar{Z}$



OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1 kΩ
Pin 16 = V_{CC}

t_{PLH}/t_{PHL}: $\bar{E}$ to $\bar{Z}$



OTHER CONDITIONS: Pins 8, 11, 12, 13 = GND
Pin 1 = V_{CC} through 1 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE: S_0 to $\bar{Z}$

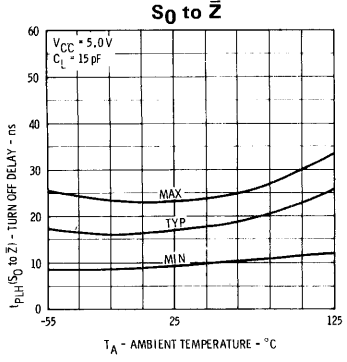


Fig. 8

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\bar{Z}$

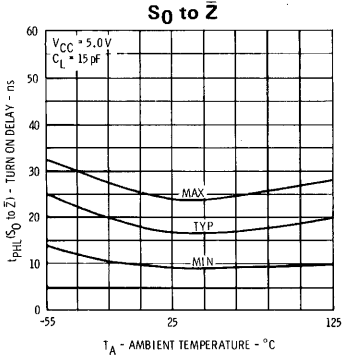


Fig. 9

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; $\bar{E}$ to $\bar{Z}$

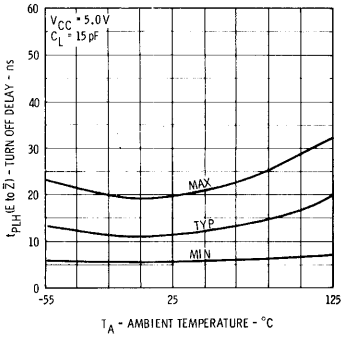


Fig. 10

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; $\bar{E}$ to $\bar{Z}$

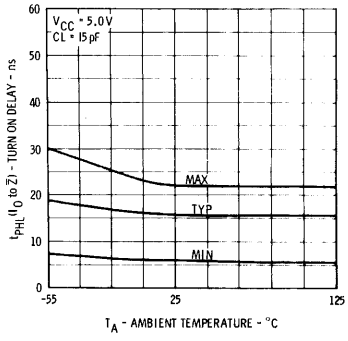


Fig. 11

8

LPTTL/MSI 93L12
LOW POWER EIGHT-INPUT MULTIPLEXER

DESCRIPTION — The LPTTL/MSI 93L12 is a monolithic, medium speed, eight input digital Multiplexer. It provides in one package the ability to select one bit of data from up to eight sources. The 93L12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fanout operation and is compatible with the Fairchild TTL family.

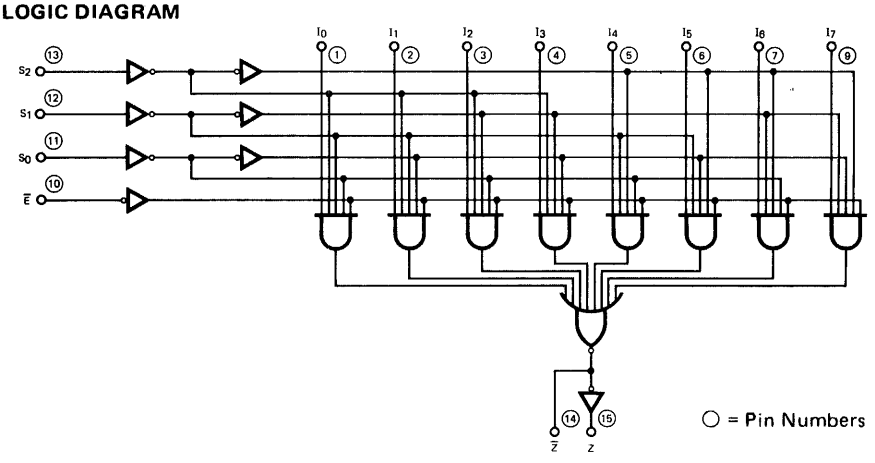
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **TYPICAL PROPAGATION DELAY OF 80 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIDOES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

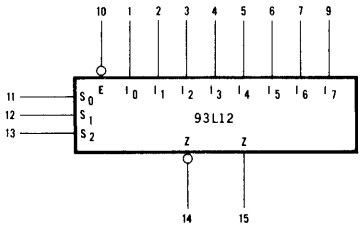
		LOADING HIGH	LOADING LOW
S_0, S_1, S_2	Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0 to I_7	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output	10 U.L.	2.5 U.L.
$\overline{Z}$	Complementary Multiplexer Output	10 U.L.	2.25 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

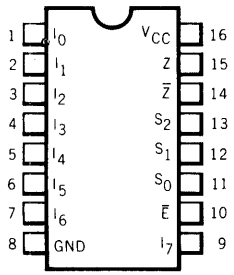


LOGIC SYMBOL

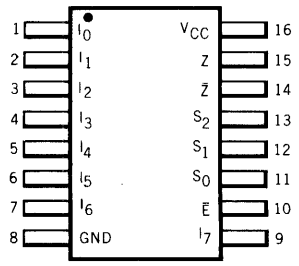


V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93L12 is a logical implementation of a single pole, eight position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = E\cdot(I_0\cdot\overline{S_0}\cdot\overline{S_1}\cdot\overline{S_2} + I_1\cdot S_0\cdot\overline{S_1}\cdot\overline{S_2} + I_2\cdot\overline{S_0}\cdot S_1\cdot\overline{S_2} + I_3\cdot S_0\cdot S_1\cdot\overline{S_2} + I_4\cdot\overline{S_0}\cdot\overline{S_1}\cdot S_2 + I_5\cdot S_0\cdot\overline{S_1}\cdot S_2 + I_6\cdot\overline{S_0}\cdot S_1\cdot S_2 + I_7\cdot S_0\cdot S_1\cdot S_2).$$

The 93L12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 93L12 can provide any logic function of four variables and its negation.

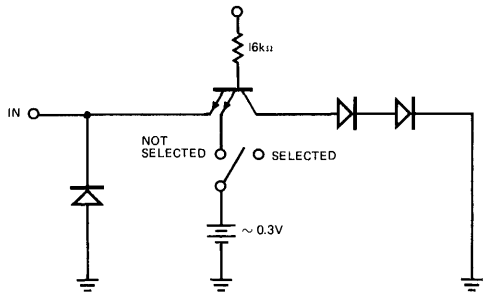
TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level does not affect output

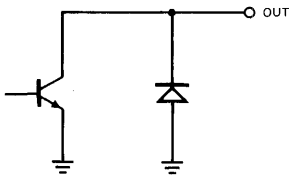
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT

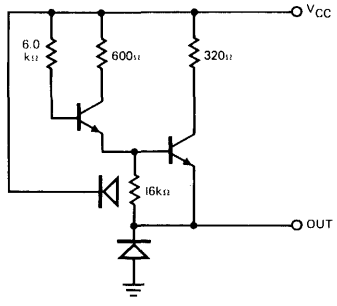


OUTPUTS
EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L12XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L12XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pin 15) 3.6 mA (Pin 14) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		9.0	13.3	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH} (S_0 to Z)	Turn Off Delay Input to Output		52	90	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL} (S_0 to Z)	Turn On Delay Input to Output		68	105	ns	V_{CC} = 5.0 V, C_L = 15 pF

TTL/MSI 93S12

EIGHT-INPUT MULTIPLEXER

TO BE ANNOUNCED

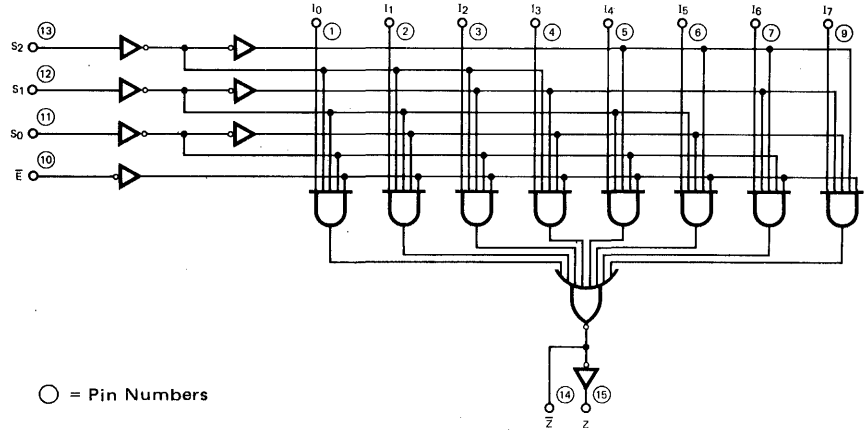
DESCRIPTION – The 93S12 is a monolithic, super high speed, 8-Input digital Multiplexer circuit utilizing the Schottky TTL process. It provides in one package the ability to select one bit of data from up to eight sources. The 93S12 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. TTL circuitry with active pullups on the outputs provides high speed, high fan out operation and is compatible with all other members of the Fairchild TTL family.

- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED COMPLEMENTARY OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, and MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

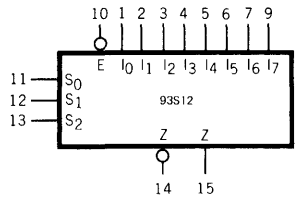
PIN NAMES

S_0, S_1, S_2	Select Inputs
$\overline{E}$	Enable (Active LOW) Input
I_0 to I_7	Multiplexer Inputs
Z	Multiplexer Output
$\overline{Z}$	Complementary Multiplexer Output

LOGIC DIAGRAM

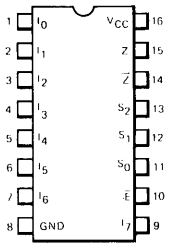


LOGIC SYMBOL

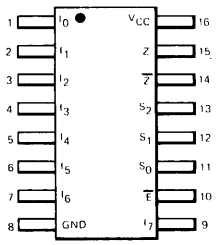


V_{CC} = pin 16
GND = pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

TTL/MSI 9313

EIGHT-INPUT MULTIPLEXER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION — The TTL/MSI 9313 is an 8-Input Multiplexer with open collector output. The 9313 has the same pinning and logic configuration as the 9312, but with an open collector $\overline{Z}$ output which allows for easy expansion of input terms. The device can select one bit of data from up to eight sources. It has an active LOW enable, and internal select decoding. The 9313 is fully compatible with all members of the Fairchild TTL family.

- **PIN FOR PIN REPLACEMENT FOR THE SIGNETICS 8231**
- **SAME PINNING AND LOGIC CONFIGURATION AS THE 9312 BUT WITH OPEN COLLECTOR OUTPUT**
- **OPEN COLLECTOR OUTPUT $\overline{Z}$ FOR EASY EXPANSION OF INPUT TERMS (WIRED-OR APPLICATIONS)**
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED Z OUTPUT**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

PIN NAMES		LOADING (Note a)
S_0, S_1, S_2	Select Inputs	1 U.L.
$\overline{E}$	Enable (Active LOW) Input	1 U.L.
I_0 to I_7	Multiplexer Inputs	1 U.L.
Z	Multiplexer Output (Note b)	10 U.L.
$\overline{Z}$	Complementary Open Collector Multiplexer Output (Note c)	10 U.L.

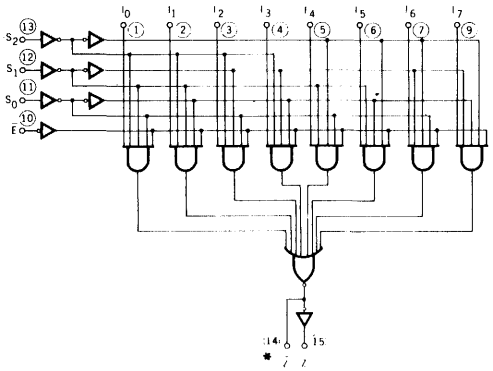
NOTES:

a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW

b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

c. An external pull-up resistor is needed to provide HIGH level drive capability. This output will sink a maximum of 16 mA at V_{out} = 0.4 V.

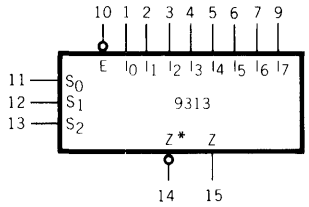
LOGIC DIAGRAM



○ = PIN NUMBERS

*OPEN COLLECTOR

LOGIC SYMBOL

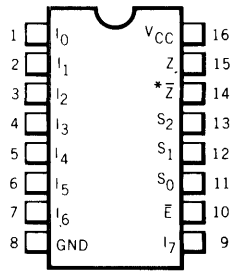


V_{CC} = 16

GND = 8

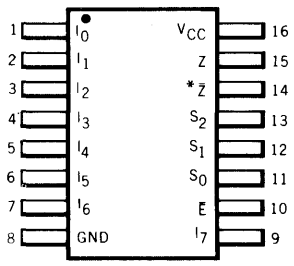
* OPEN COLLECTOR

CONNECTION DIAGRAMS
DIP (TOP VIEW)



* OPEN COLLECTOR

FLATPAK (TOP VIEW)



* OPEN COLLECTOR

FUNCTIONAL DESCRIPTION — The TTL/MSI 9313 is a logical implementation of a single pole, eight-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. An open collector output $\overline{Z}$ is provided for easy expansion of input terms. Also a fully buffered Z output is available. The Enable input ($\overline{E}$) is active LOW. When it is not activated the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$Z = E \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$.

The 9313 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 9313 can provide any logic function of four variables and its negation.

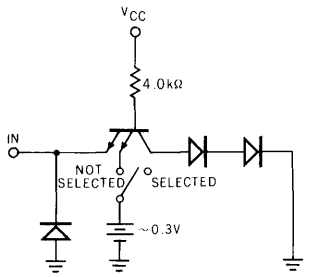
TABLE I TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

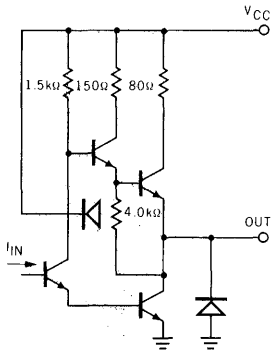
H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

TYPICAL INPUT AND OUTPUT CIRCUITS

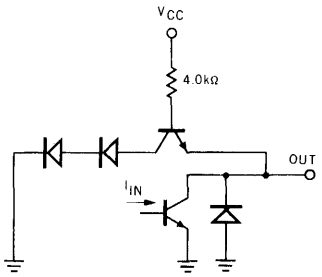
INPUTS
EQUIVALENT CIRCUIT



Z Output (Pin 15)
EQUIVALENT CIRCUIT



$\overline{Z}$ Output (Pin 14)
EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
*Input Voltage (dc)	-0.5V to +5.5V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

8

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9313XM	4.5V	5.0V	5.5V	-55°C to 125°C
9313XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage on Z (Pin 15)	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = -800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input logical HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input logical LOW voltage for all inputs
I_{IL}	Input LOW Current		-1.0	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{IH}	Input HIGH Current		5.0	40	μA	V_{CC} = MAX., V_{IN} = 2.4V
			0.02	1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{CEX}	Output HIGH Leakage Current on $\overline{Z}$ (Pin 14)		5.0	150	μA	V_{CC} = 4.5V, V_{OUT} = 4.5V, V_{IN} = 0.6V on Data Input V_{IN} (E & S Inputs) = V_{IL} or V_{IH} per Truth Table
I_{SC}	Output Short Circuit Current on Z (Pin 15)	−30	−75	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0V
I_{CC}	Power Supply Current		28	47	mA	V_{CC} = MAX., I_0-I_7 = GND
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = -12 mA, T_A = 25°C

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

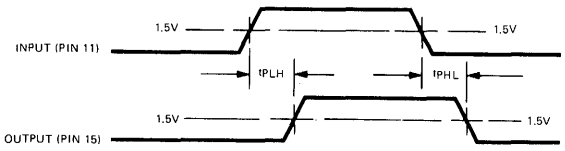
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS				UNITS	CONDITIONS
		9313XM(MIL)		9313XC(IND)			
		TYP.	MAX.	TYP.	MAX.		
t_{PLH} (S_0 to Z)	Turn Off Delay Input to Output	25	32	25	36	ns	V_{CC} = 5.0V C_T = C_L = 15 pF, R_X = 400 Ω to V_{CC}
t_{PHL} (S_0 to Z)	Turn On Delay Input to Output	33	40	33	45	ns	

SWITCHING CHARACTERISTIC CURVES

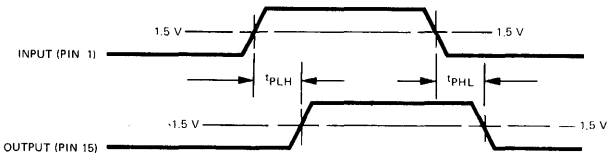
All measurements are made with V_{CC} = 5.0 V applied to pin 16 and with pin 8 grounded.

t_{PLH} / t_{PHL} : S_0 to Z



OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{PLH} / t_{PHL} : I_0 to Z



OTHER CONDITIONS: Pins 8, 10, 11, 12, 13 = GND
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

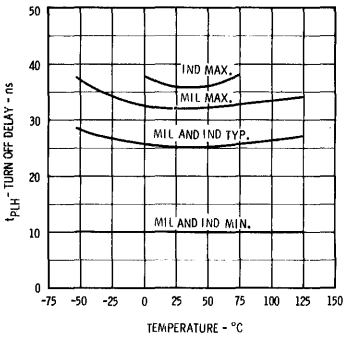


Fig. 1

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to Z

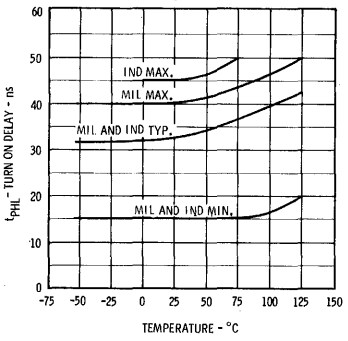


Fig. 2

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

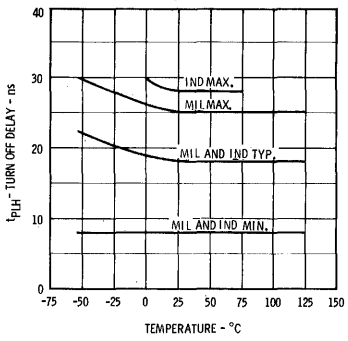


Fig. 3

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; I_0 to Z

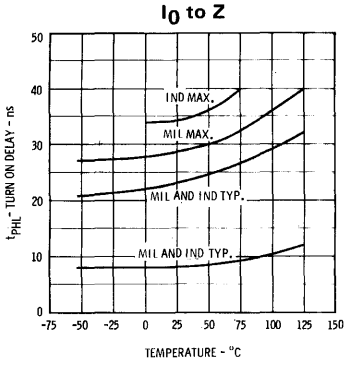
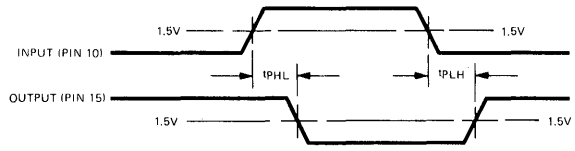


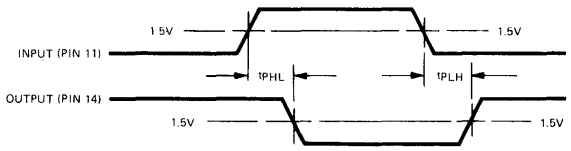
Fig. 4

t_{PLH} / t_{PHL} : $\overline{E}$ to Z



OTHER CONDITIONS: Pins 8, 11, 12, 13 = GND
Pin 1 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

t_{PLH} / t_{PHL} : S_0 to $\overline{Z}$



OTHER CONDITIONS: Pins 1, 8, 10, 12, 13 = GND
Pin 2 = V_{CC} through 1.0 kΩ
Pin 16 = V_{CC}

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; $\overline{E}$ to Z

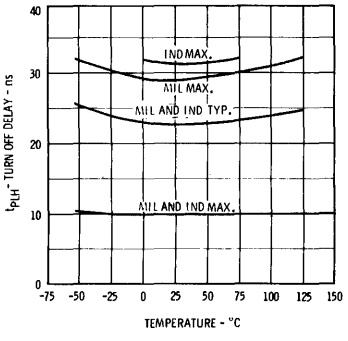


Fig. 5

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; $\overline{E}$ to Z

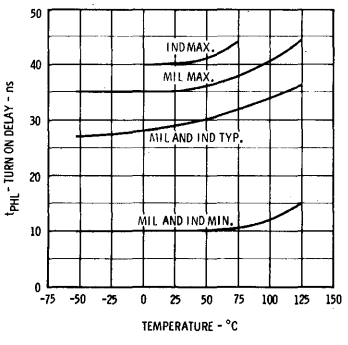


Fig. 6

TURN OFF DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

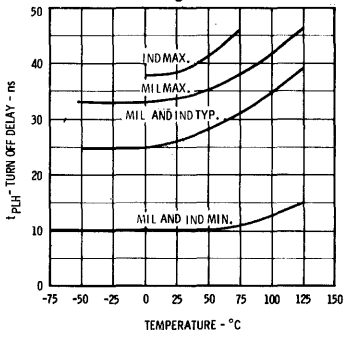


Fig. 7

TURN ON DELAY VERSUS AMBIENT TEMPERATURE; S_0 to $\overline{Z}$

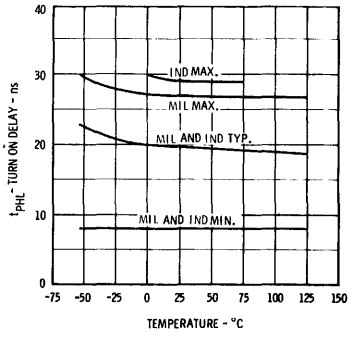


Fig. 8

8

WIRED-OR APPLICATIONS

It is possible to perform the "Wired OR" function by connecting the open collector $\overline{Z}$ outputs together and adding an external pull up resistor.

The value of the pull up is determined by considering the fanout of the "OR Tie" and the number of devices in the "OR Tie". The pull up resistor value is chosen from a range between a maximum value (determined such that the required V_{OH} is maintained with all the OR tied outputs off) and a minimum value (determined such that with only one output on in the "OR-Tie", its fanout is not exceeded.

Minimum and Maximum Pull up Values

$$R_X\ (\text{Min.}) = \frac{V_{CC}\ (\text{max.}) - V_{OL}}{I_{OL} - N_2\, I_{IL} - (N_1 - 1)\, I_{IL}}$$

$$R_X\ (\text{Max.}) = \frac{V_{CC}\ (\text{min.}) - V_{OH}}{N_1\, I_{CEX} + N_2\, I_{IH}}$$

Where

N_1 = Number of "Wired OR" Outputs
N_2 = Fanout of "OR Tie"
V_{CC} = Power Supply Voltage
R_X = External Pull-up Resistor
I_{CEX} = Output HIGH Leakage Current on $\overline{Z}$ (150 μA)
I_{IH} = Input HIGH Current (40 μA)
I_{IL} = Input LOW Current (1.6 mA)
V_{OL} = Output LOW Voltage (0.4 V)
V_{OH} = Output HIGH Voltage (2.4 V)
I_{OL} = Maximum Current Sinking Capability of Single Output (16 mA)

Example R_L (Min) and R_L (Max.) for four 9313's OR Tied and driving 1 TTL gate. (Industrial V_{CC} tolerances used)

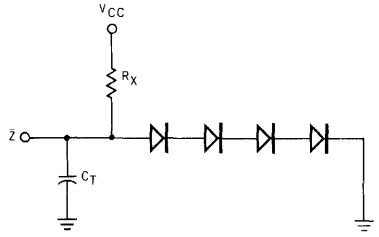
$$R_X\ (\text{Min.}) = \frac{5.25\ \text{V} - 0.4\ \text{V}}{16\ \text{mA} - 1\ (1.6\ \text{mA}) - (4-1)\ 1.6\ \text{mA}} = \frac{4.85\text{V}}{9.6\ \text{mA}} = 505\ \Omega$$

$$R_X\ (\text{Max.}) = \frac{4.75\ \text{V} - 2.4\ \text{V}}{4\ (150\ \mu\text{A}) + 1\ (40\ \mu\text{A})} = \frac{2.35\text{V}}{640\ \mu\text{A}} = 3.7\ \text{k}\Omega$$

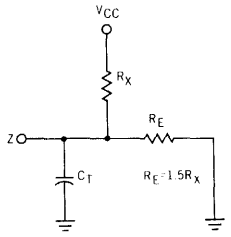
The pull up resistor value (± resistor tolerance) selected should be between these max. and min. values.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in circuit 1. Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor circuits 2 and 3 give progressively slower propagation delays. (See Figures 9 and 10.)

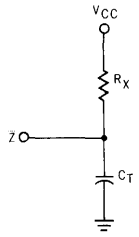
LOAD CIRCUIT 1



LOAD CIRCUIT 2



LOAD CIRCUIT 3



C_T = Total Capacitance at Output

SWITCHING DELTA FOR TURN OFF DELAY (Δt_{PLH}) ANY INPUT TO Z OUTPUT, VERSUS LOAD CAPACITANCE (C_T)

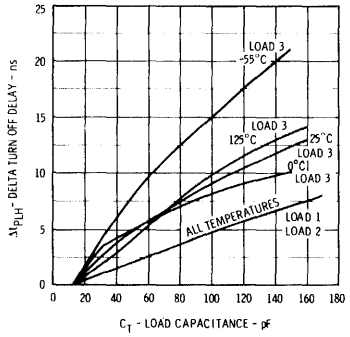


Fig. 9

SWITCHING DELTA FOR TURN ON DELAY (Δt_{PHL}) ANY INPUT TO Z OUTPUT, VERSUS LOAD CAPACITANCE (C_T)

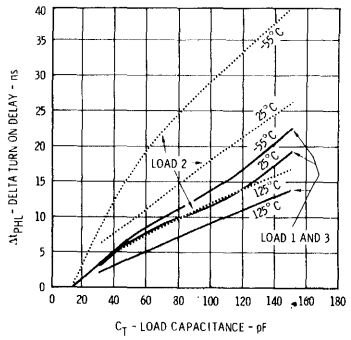


Fig. 10

TTL/MSI 9314
QUAD LATCH

DESCRIPTION – The MSI 9314 is a multifunctional 4-Bit Latch. The latch is designed for general purpose storage applications in high speed digital systems. All inputs feature diode clamping to reduce negative line transients. All outputs have active pull-up circuitry to provide high capacitance drive and to provide low impedance in both logic states for good ac noise immunity.

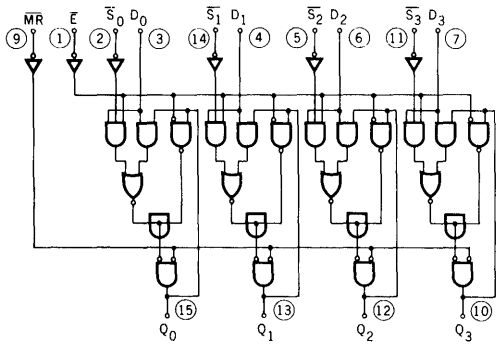
- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LEVEL LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**
- **25 ns THROUGH DELAY**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE DIRECT INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

PIN NAMES

		LOADING (Note a)
$\overline{E}$	(Active LOW) Enable Input	1 U.L.
D_0, D_1, D_2, D_3	Data Inputs	1.5 U.L.
$\overline{S}_0, \overline{S}_1, \overline{S}_2, \overline{S}_3$	Set (Active LOW) Inputs	1 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Latch Outputs (Note b)	10 U.L.

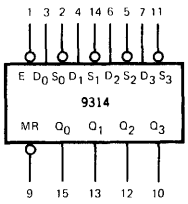
NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



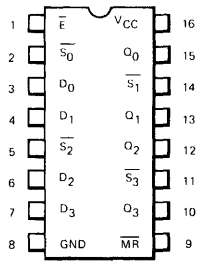
○ = PIN NUMBERS

LOGIC SYMBOL

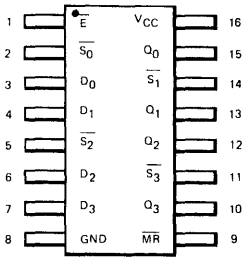


V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION

LATCH OPERATION – The 9314 consists of four latches with a common active LOW enable and active LOW master reset. When the common enable goes HIGH, data present in the latches is stored and the state of a latch is no longer affected by the $\overline{S}$ and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs LOW.

Each of the four latches can be operated in one of two modes:

D TYPE LATCH – For D type operation the $\overline{S}$ input of a latch is held LOW. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes HIGH.

SET/RESET LATCH – During set/reset operation when the common enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the enable goes HIGH, the latch remains in the last state prior to the LOW to HIGH transition.

The two modes of operation of the 9314 latches are shown in the Truth Table below.

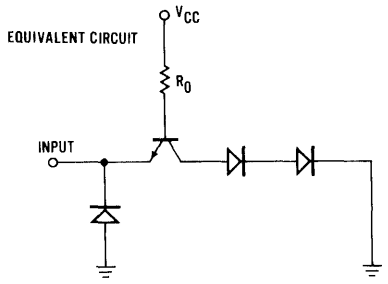
TRUTH TABLE

$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_N	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{N-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{N-1}	
H	H	X	X	Q_{N-1}	
L	X	X	X	L	RESET

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State
Q_N = Present Output State

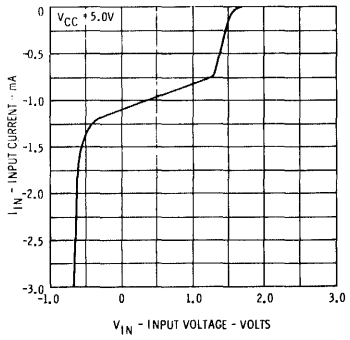
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS

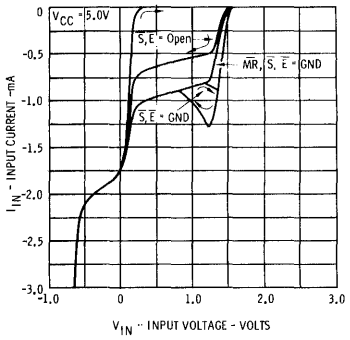


INPUT CURRENT VERSUS INPUT VOLTAGE

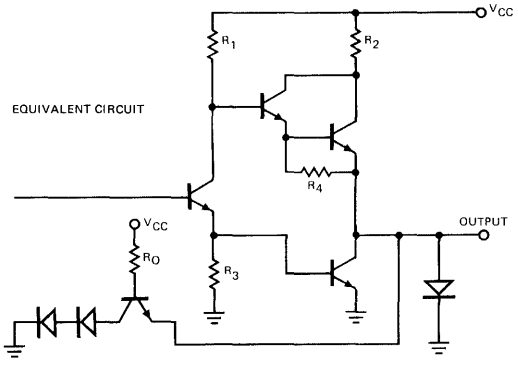
$\overline{MR}$, $\overline{E}$, $\overline{S}$



D

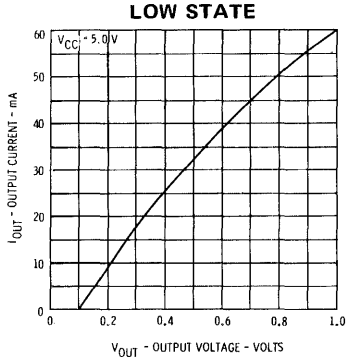


OUTPUTS

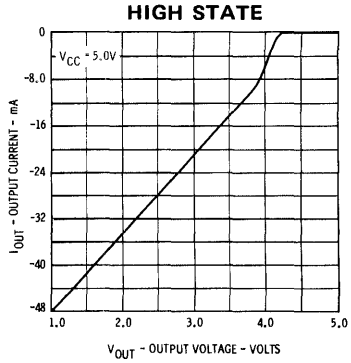


OUTPUT CURRENT VERSUS OUTPUT VOLTAGE

LOW STATE



HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
9314XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9314XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = -12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OL} = -800μA; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA; V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{MR}$, $\overline{E}$, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	D_0, D_1, D_2, D_3		15	60		
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current $\overline{MR}$, $\overline{E}$, $\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$		-0.96	-1.6	mA	V_{IN} = 0.4 V, V_{CC} = MAX.
	D_0, D_1, D_2, D_3		-1.9	-2.7	mA	V_{IN} = 0.0 V, V_{CC} = MAX. (Note 6)
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-20	−40	-70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		35	55	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.
(6) This current is measured at V_{IN} = 0.0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.4 V is 2.4 mA.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
t_{PLH}	Turn off Delay Enable to Output		18	24	ns	Fig. 1	V_{CC} = 5.0 V; C_L = 15 pF
t_{PHL}	Turn on Delay Enable to Output		18	24	ns		
t_{PLH}	Turn off Delay Data to Output		8	12	ns	Fig. 2	
t_{PHL}	Turn on Delay Data to Output		18	24	ns		
t_{PHL}	Turn on Delay MR to Output		12	18	ns	Fig. 5	
t_{PLH}	Turn off Delay Set to Output		18	24	ns	Fig. 7	

8

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
$t_s(H)$	Set-up Time HIGH Data to Enable	5.0	0		ns	Fig. 3	V_{CC} = 5.0 V
$t_h(H)$	Hold Time HIGH Data to Enable	0	−12		ns		
$t_s(l)$	Set-up Time LOW Data to Enable	18	13		ns		
$t_h(L)$	Hold Time LOW Data to Enable	5.0	1.0		ns		
$t_{pw}\overline{E}$	Enable Pulse Width	18	12		ns	Fig. 4	
$t_{pw}\overline{MR}$	Master Reset Pulse Width	18	7.0		ns	Fig. 5	
t_{rec}	Recovery Time Master Reset to Enable	0	−7		ns	Fig. 6	
$t_s(H)$	Set-up Time HIGH Data to Set Input	8.0	0		ns	Fig. 7	
$t_h(L)$	Hold Time LOW Data to Set Input	8.0	0		ns		

SET UP TIME: t_s is defined as the minimum time required for the logic level to be present at the Data Input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.

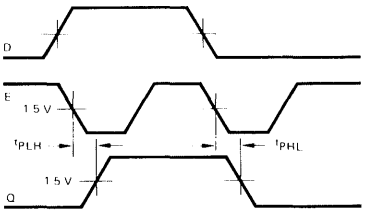
HOLD TIME: t_h is defined as the minimum time following the Enable (E) or Set (S) transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable (E) or Set (S) transition from LOW to HIGH and still be recognized.

RECOVERY TIME: t_{rec} is defined as the minimum time that the Enable must remain LOW after the Master Reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data.

SWITCHING CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. Outputs under test are loaded with 15 pF (includes jig and probe). Pins not reference are not connected.

t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H

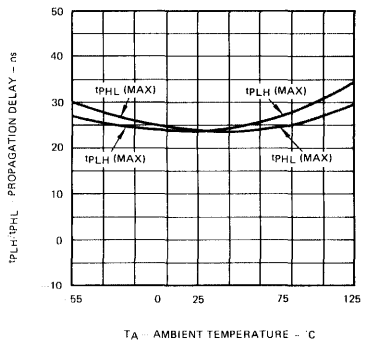
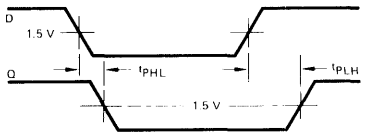


Fig. 1

t_{PLH}/t_{PHL} (DATA TO OUTPUT)



Other Conditions: $\overline{E}$ = L, $\overline{S}$ = L, $\overline{MR}$ = H

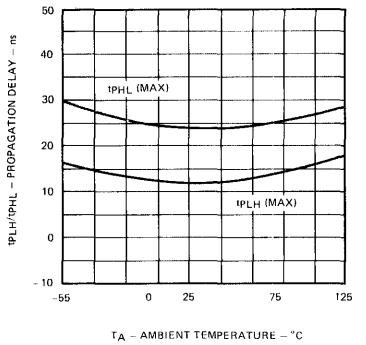
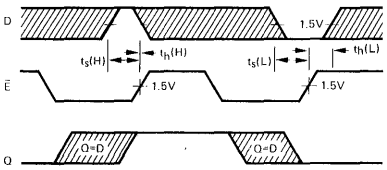


Fig. 2

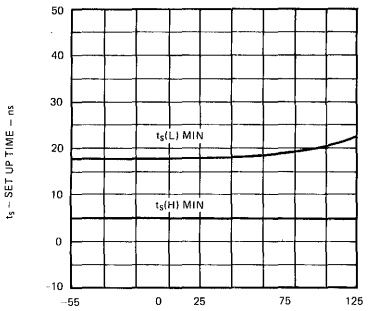
SWITCHING CHARACTERISTICS

SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE



OTHER CONDITIONS: $\overline{MR}$ = H, $\overline{S}$ = L

The shaded areas indicate when the Data input is permitted to change for predictable output performance.



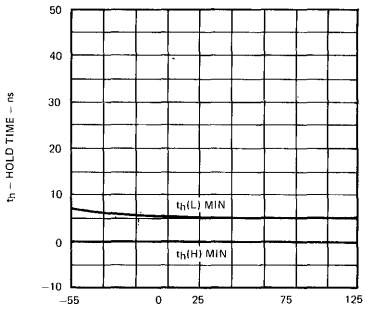
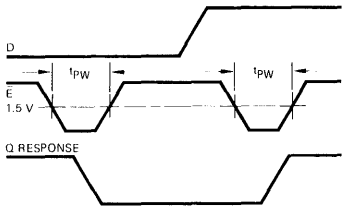


Fig. 3

t_{pw} (MIN. ENABLE PULSE WIDTH)



Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H

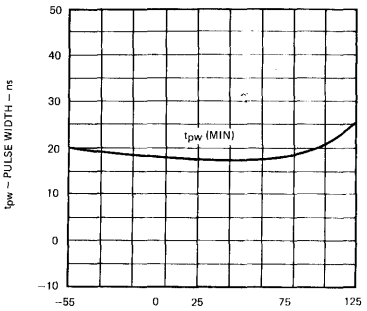
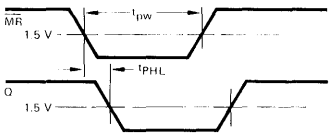


Fig. 4

t_{pw} (MIN. MASTER RESET PULSE WIDTH) t_{PHL} (MASTER RESET TO OUTPUT)



Other Conditions: $\overline{S}$ & $\overline{E}$ = L

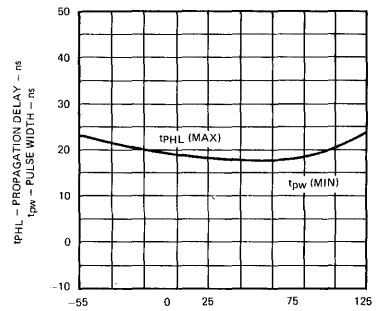
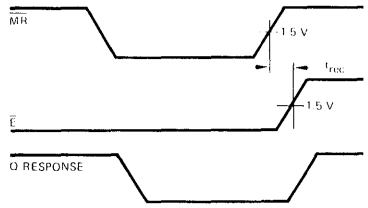


Fig. 5

t_{rec} (MASTER RESET RECOVERY TIME)



Other Conditions: $\overline{S}$ = L, D = H

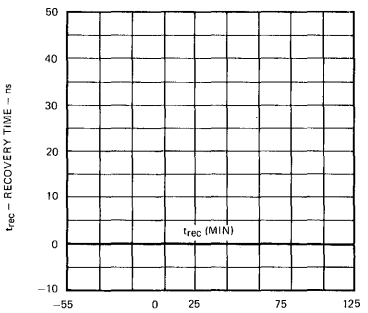
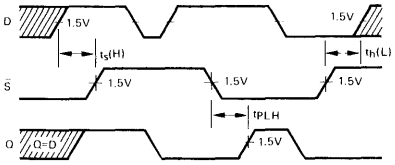


Fig. 6

SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO SET INPUT, AND SET TO OUTPUT DELAY.



OTHER CONDITIONS: $\overline{MR}$ = H, $\overline{E}$ = L

The shaded area indicates when the Data input is permitted to change for predictable output performance.

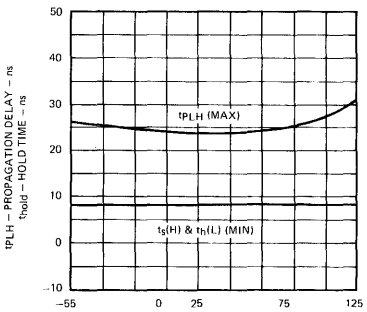


Fig. 7

8

LPTTL/MSI 93L14
LOW POWER QUAD LATCH

DESCRIPTION – The LPTTL/MSI 93L14 is a multifunctional 4-Bit Latch. The latch is designed for general purpose storage applications in high speed digital systems. The 93L14 uses TTL technology and is compatible with the Fairchild TTL family. All inputs feature diode clamping to reduce negative line transients. All outputs have active pull-up circuitry to provide low impedance in both logic states for good ac noise immunity.

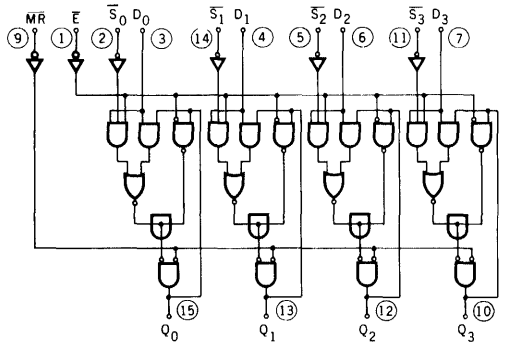
- **CAN BE USED AS SINGLE INPUT D LATCHES OR SET/RESET LATCHES**
- **ACTIVE LEVEL LOW ENABLE GATE INPUT**
- **OVERRIDING MASTER RESET**
- **TYPICAL PROPAGATION DELAY OF 68 ns**
- **TYPICAL POWER DISSIPATION OF 50 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

		LOADING HIGH	LOADING LOW
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
D_0, D_1, D_2, D_3	Data Inputs	0.75 U.L.	0.375 U.L.
$\overline{S}_0, \overline{S}_1, \overline{S}_2, \overline{S}_3$	Set (Active LOW) Inputs	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_0, Q_1, Q_2, Q_3	Latch Outputs	10 U.L.	2.25 U.L.

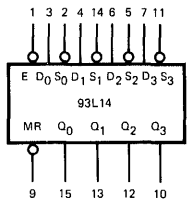
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



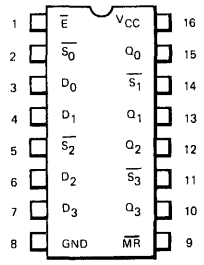
○ = Pin Numbers

LOGIC SYMBOL

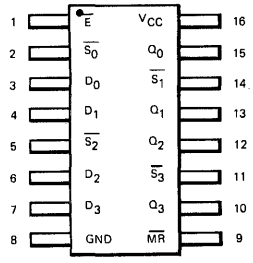


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION

LATCH OPERATION – The 93L14 consists of four latches with a common active LOW enable and active LOW master reset. When the common enable goes HIGH, data present in the latches is stored and the state of a latch is no longer affected by the $\overline{S}$ and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs LOW.

Each of the four latches can be operated in one of two modes:

D TYPE LATCH – For D type operation the $\overline{S}$ input of a latch is held LOW. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes HIGH.

SET/RESET LATCH – During set/reset operation when the common enable is LOW a latch is reset by a LOW on the D input, and can be set by a LOW on the $\overline{S}$ input if the D input is HIGH. If both $\overline{S}$ and D inputs are LOW, the D input will dominate and the latch will be reset. When the enable goes HIGH, the latch remains in the last state prior to disablement.

The two modes of operation of the 93L14 latches are shown in the Truth Table below.

TRUTH TABLE

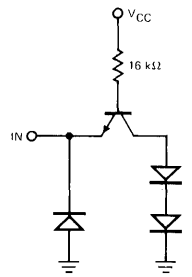
$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_n	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{n-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{n-1}	
H	H	X	X	Q_{n-1}	
L	X	X	X	L	RESET

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level

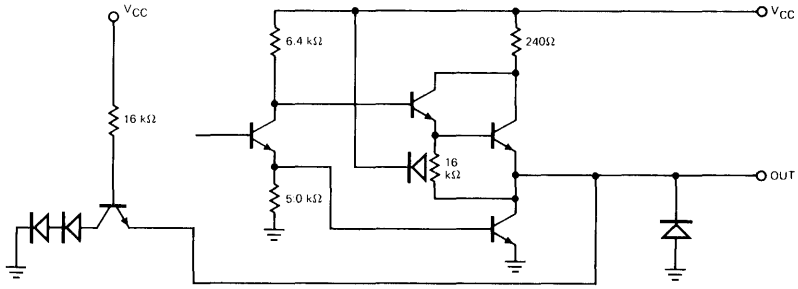
Q_{n-1} = Previous Output State
Q_n = Present Output State

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS
EQUIVALENT CIRCUIT



OUTPUTS
EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

8

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L14XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L14XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 5)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current $\overline{S}$, $\overline{E}$ & $\overline{MR}$		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
	Input LOW Current D Inputs		−0.38	−0.64	mA	V_{CC} = MAX., V_{IN} = 0.0 V (See Note 4)
I_{IH}	Input HIGH Current $\overline{S}$, $\overline{E}$ & $\overline{MR}$ D Inputs		2.0 3.0	20 30	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 6)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		10	16.5	mA	V_{CC} = MAX., All Outputs LOW, Inputs Disabled

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) This current is measured at V_{IN} = 0.0 V to insure that no current is being absorbed by the device internally. The maximum value given guarantees that the maximum instantaneous current that can flow out of the input at V_{IN} = 0.3 V is 0.6 mA.
(5) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
(6) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH}	Turn off Delay Enable to Output		46	80	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn off Delay Enable to Output		51	80	ns		
t_{PLH}	Turn off Delay Data to Output		24	40	ns	Fig. 2	
t_{PHL}	Turn on Delay Data to Output		45	70	ns		
t_{PHL}	Turn on Delay $\overline{MR}$ to Output		28	55	ns	Fig. 5	
t_{PLH}	Turn off Delay Set to Output		35	60	ns	Fig. 7	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

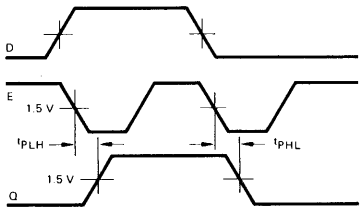
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
$t_s(H)$	Set-up Time HIGH Data to Enable	15	10		ns	Fig. 3	V_{CC} = 5.0 V
$t_h(H)$	Hold Time HIGH Data to Enable	−10	−20		ns		
$t_s(L)$	Set-up Time LOW Data to Enable	30	20		ns		
$t_h(L)$	Hold Time LOW Data to Enable	0	−10		ns		
$t_{pw}E$	Enable Pulse Width	50	30		ns	Fig. 4	
$t_{pw}MR$	Master Reset Pulse Width	45	25		ns	Fig. 5	
t_{rec}	Recovery Time Master Reset to Enable	−20	−40		ns	Fig. 6	
$t_s(H)$	Set-up Time HIGH Data to Set Input	15	10		ns	Fig. 7	
$t_h(L)$	Hold Time LOW Data to Set Input	0	−4		ns		

SET UP TIME: t_s is defined as the minimum time required for the logic level to be present at the Data Input prior to the enable transition from LOW to HIGH in order for the latch to recognize and store the new data.
HOLD TIME: t_h is defined as the minimum time following the Enable ($\overline{E}$) or Set ($\overline{S}$) transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the Enable ($\overline{E}$) or Set ($\overline{S}$) transition from LOW to HIGH and still be recognized.
RECOVERY TIME: t_{rec} is defined as the minimum time that the Enable must remain LOW after the Master Reset transition from LOW to HIGH in order for the latch to recognize and store HIGH data. A negative Recovery Time indicates that the Enable may go HIGH prior to the Master Reset transition from LOW to HIGH and still retain HIGH data.

TYPICAL SWITCHING CHARACTERISTICS

All delays are measured with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. Outputs under test are loaded with 15 pF (includes jig and probe). Pins not reference are not connected.

t_{PLH}/t_{PHL} (ENABLE TO OUTPUT)



Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H

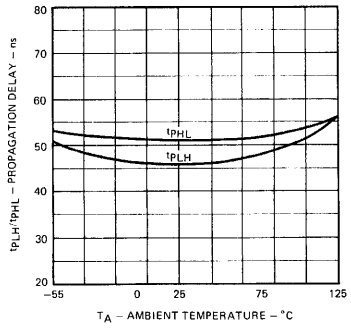
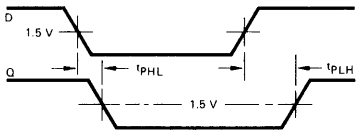


Fig. 1.

t_{PLH}/t_{PHL} (DATA TO OUTPUT)



Other Conditions: $\overline{E}$ = L, $\overline{S}$ = L, $\overline{MR}$ = H

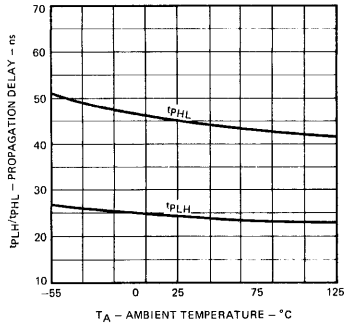
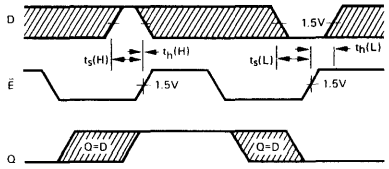


Fig. 2.

SWITCHING CHARACTERISTICS

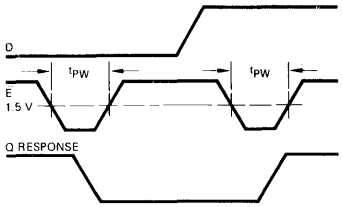
SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO ENABLE



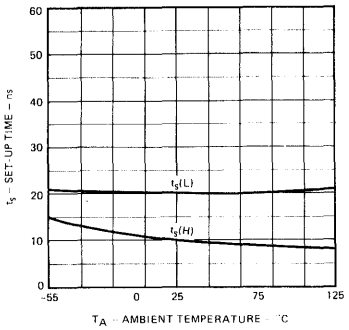
OTHER CONDITIONS: $\overline{MR}$ = H, $\overline{S}$ = L

The shaded areas indicate when the Data input is permitted to change for predictable output performance.

t_{pw} (MIN. ENABLE PULSE WIDTH)



Other Conditions: $\overline{S}$ = L, $\overline{MR}$ = H



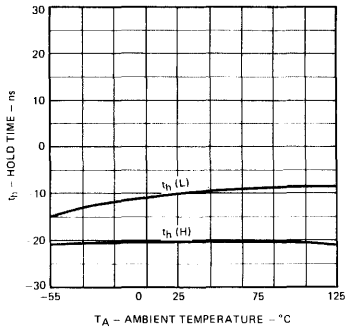


Fig. 3

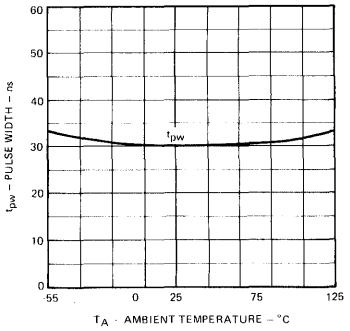
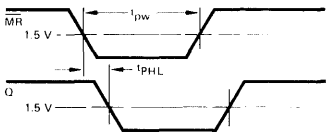


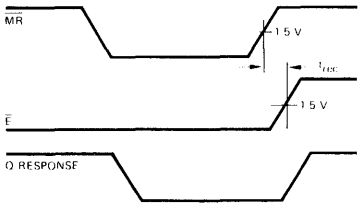
Fig. 4

t_{pw} (MIN. MASTER RESET PULSE WIDTH) t_{PHL} (MASTER RESET TO OUTPUT)



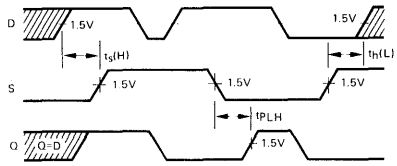
Other Conditions: $\overline{S}$ & $\overline{E}$ = L

t_{rec} (MASTER RESET RECOVERY TIME)



Other Conditions: $\overline{S}$ = L, D = H

SET-UP TIME (t_s) AND HOLD TIME (t_h) DATA TO SET INPUT, AND SET TO OUTPUT DELAY.



OTHER CONDITIONS: $\overline{MR}$ = H, $\overline{E}$ = L

The shaded area indicates when the Data input is permitted to change for predictable output performance.

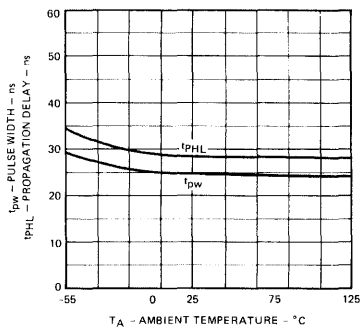


Fig. 5

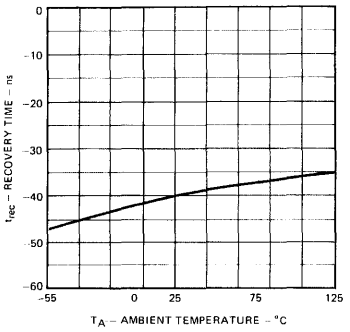


Fig. 6

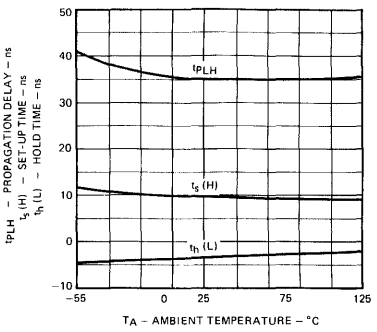


Fig. 7

TTL/MSI 9315 (7441)
1-OF-10 DECODER/DRIVER

DESCRIPTION – The TTL/MSI 9315 accepts 1-2-4-8 binary coded decimal inputs and provides ten mutually exclusive outputs to directly control the ionizing potentials of many gas filled cold cathode indicator tubes. The 9315 is similar in operation to the CμL9960, but the 9315 can be driven from any TTL or DTL product.

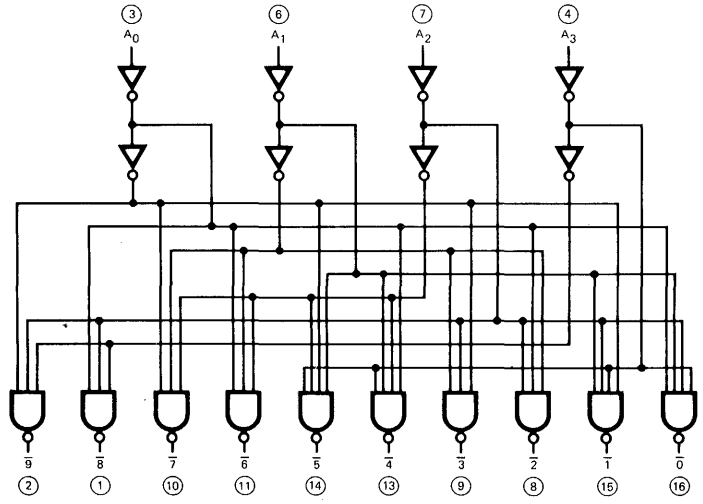
- **STABLE HIGH VOLTAGE OUTPUT CHARACTERISTICS**
- **DIRECT DISPLAY DRIVE CAPABILITY**
- **BCD ACTIVE LEVEL HIGH INPUTS**
- **BLANKING TEST MODE**
- **–55°C TO +125°C TEMPERATURE CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7 V
Input Voltage (dc) (See Note 1)	–1.5 V to +5.5 V
Input Current (dc) (See Note 1)	–10 mA to +1.0 mA
Current into output when output is LOW	10 mA
Current into each output when output is HIGH (See Note 2)	+1.5 mA

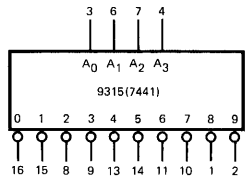
Note 1: Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
2: Total current through all 10 outputs in the HIGH state shall not exceed 2.0 mA.

LOGIC DIAGRAM



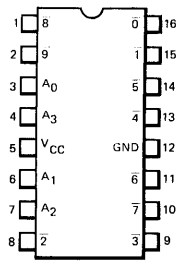
○ = Pin Numbers

LOGIC SYMBOL

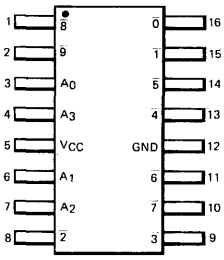


V_{CC} = PIN 5
GND = PIN 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The one-of-ten decoder/driver accepts BCD inputs from all TTL circuits and produces the correct output selection to directly drive gas filled cold cathode indicator tubes. The outputs are selected as shown in the Truth Table. It is capable of driving all known available cold cathode indicator tubes having 7 mA or less cathode current.

Unused input codes 12 and 13 cause all the outputs to remain HIGH, no cathode will be selected. This results in the indicator tube being blanked. Using this feature for blanking may cause a slight glow to appear in the tube.

TRUTH TABLE

	A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	H	L	L	L	H	L	H	H	H	H	H	H	H	H
2	L	H	L	L	H	H	L	H	H	H	H	H	H	H
3	H	H	L	L	H	H	H	L	H	H	H	H	H	H
4	L	L	H	L	H	H	H	H	L	H	H	H	H	H
5	H	L	H	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	H	H	H	L	H	H	H	H	H	H	H	L	H	H
8	L	L	L	H	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	L	H	L	H	H	H	L	H	H	H	H	H	L	H
11	H	H	L	H	H	H	H	L	H	H	H	H	H	L
12	L	L	H	H	H	H	H	H	H	H	H	H	H	H
13	H	L	H	H	H	H	H	H	H	H	H	H	H	H
14	L	H	H	H	H	H	H	H	H	H	L	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	L	H	H

H = HIGH voltage level
L = LOW voltage level

LOADING RULES

INPUTS	LOADING
All Inputs	1 U.L.

TTL INPUT LOAD

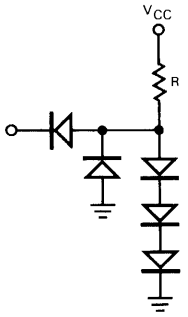
GRADE	INPUTS	LOADING
IND	All Inputs	1/9.4
MIL	All Inputs	2/9.4

OUTPUTS are designed to drive gas filled cold Cathode Indicator tubes

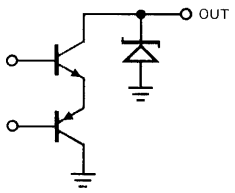
1 U.L. = 1 DTL Unit Load
1 U.L. is defined by the entries I_{IH} and I_{IL} in the table on following page.

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

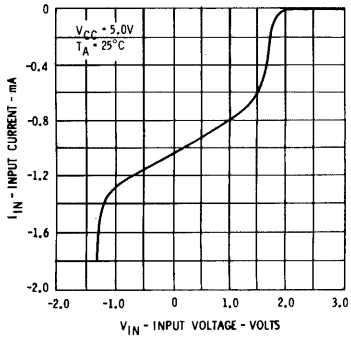
EQUIVALENT INPUT CIRCUIT



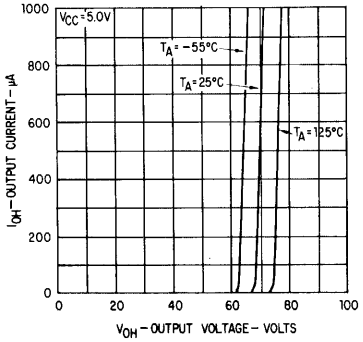
EQUIVALENT OUTPUT CIRCUIT



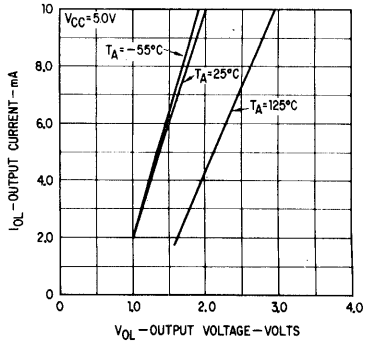
INPUT CURRENT VERSUS INPUT VOLTAGE A_0, A_1, A_2, A_3 INPUTS



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. 9315XM, see note)

SYMBOL	PARAMETER	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	61		70	75		70		Volts	V_{CC} = 5.5 V, Force 2.0 mA into HIGH Output
I_{OH}	Output HIGH Leakage Current					20		50	μA	V_{CC} = 5.5 V, V_{OUT} = 55 V Inputs at Threshold Voltages (V_{IL} = Gnd, V_{IH} = 4.5 V) as per Truth Table
V_{OL}	Output LOW Voltage		3.0			2.5		3.7	Volts	V_{CC} = 4.5 V, I_{OL} = 7.0 mA Inputs at Threshold Voltages (V_{IL} or V_{IH}) as per Truth Table
V_{IH}	Input HIGH Voltage	2.1		1.9			1.7		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		1.4			1.1		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−1.5		−1.3	−1.5		−1.5	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Inputs Open
I_{IH}	Input HIGH Current				0.02	2.0		5.0	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V Other Inputs Open
I_{CC}	Supply Current		29			29		29	mA	V_{CC} = 5.0 V, No Connection to Input or Output Pins

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9315XC, see note)

SYMBOL	PARAMETER	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	67		70	75		70		Volts	V_{CC} = 5.25 V, Force 2.0 mA into HIGH Output
I_{OH}	Output HIGH Leakage Current					40		50	μA	V_{CC} = 5.25 V, V_{OUT} = 55 V Inputs at Threshold Voltages (V_{IL} = Gnd, V_{IH} = 4.5 V) as per Truth Table
V_{OL}	Output LOW Voltage		3.2			3.0		3.6	Volts	V_{CC} = 4.75 V, I_{OL} = 7.0 mA Inputs at Threshold Voltages (V_{IL} or V_{IH}) as per Truth Table
V_{IH}	Input HIGH Voltage	2.0		2.0			2.0		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−1.5			−1.5		−1.5	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V Other Inputs Open
I_{IH}	Input HIGH Current					5.0		10	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V Other Inputs Open
I_{CC}	Supply Current		31			31		31	mA	V_{CC} = 5.0 V, No Connection to Input or Output Pins

NOTE:
X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

TTL/MSI 9317B • 9317C
SEVEN SEGMENT DECODER/DRIVER

DESCRIPTION — The 9317 is a TTL/MSI Seven Segment Decoder/Driver designed to accept four inputs in 8421 BCD code and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used to directly drive seven segment incandescent lamp displays and light emitting diode indicators (or indirectly drive neon, electro-luminescent, numeric displays). The 9317 is compatible with all members of the Fairchild TTL family.

The 9317 is available in two output current and latch voltage versions, the 9317B and C.

- **TTL COMPATIBLE**
- **AUTOMATIC RIPPLE BLANKING FOR SUPPRESSION OF LEADING EDGE ZEROS AND/OR TRAILING EDGE ZEROS**
- **LAMP INTENSITY MODULATION CAPABILITY**
- **LAMP TEST FACILITY**
- **BLANKING INPUT**
- **ACTIVE LOW OUTPUTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**
- **DRIVE LAMPS DIRECTLY**
- **CODES IN EXCESS OF BINARY 9 DISABLE OUTPUTS**
- **ENHANCED RELIABILITY WITH UNIQUE NUMERIC ONE DISPLAY POSITION**

PIN NAMES

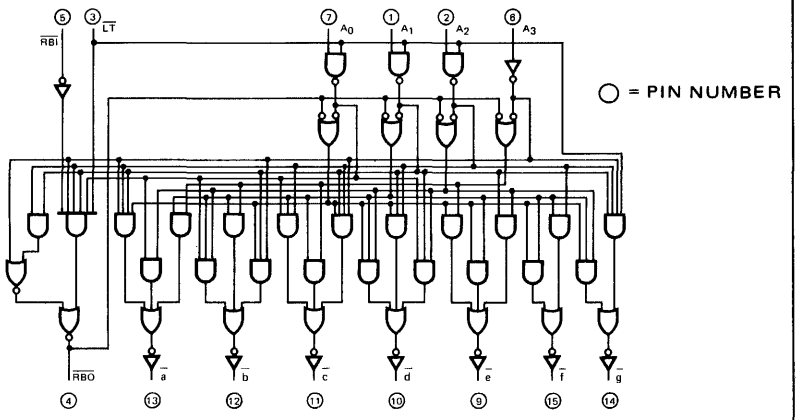
		LOADING HIGH	LOADING LOW
A_0, A_1, A_2, A_3	Address Inputs	1.0 U.L.	1.0 U.L.
$\overline{LT}$	Lamp Test (Active LOW) Input	5.0 U.L.	4.0 U.L.
$\overline{RBI}$	Ripple Blanking (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{RBO}$	Ripple Blanking (Active LOW) Output	1.5 U.L.	1.5 U.L.
$\overline{a}$, $\overline{b}$, $\overline{c}$, $\overline{d}$, $\overline{e}$, $\overline{f}$, $\overline{g}$	(Active LOW) Outputs	See Options	

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

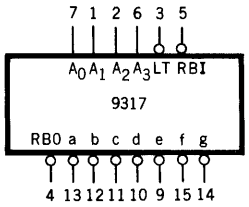
OPTIONS

PARAMETER	9317B	9317C
Latch Voltage	20 Volts	30 Volts
Output Current (Pins 9 through 15)	40 mA	20 mA

LOGIC DIAGRAM

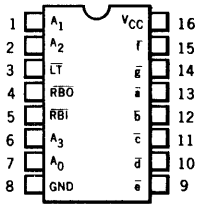


LOGIC SYMBOL

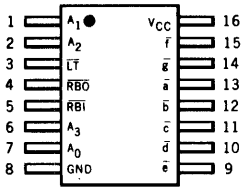


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 9317 seven segment decoder/driver accepts a 4-bit BCD 8421 code input and produces the appropriate outputs for selection of segments in a seven segment matrix display used for representing the decimal numbers 0–9. The seven outputs ($\bar{a}$,$\bar{b}$,$\bar{c}$,$\bar{d}$, $\bar{e}$,$\bar{f}$,$\bar{g}$,) of the decoder select the corresponding segments in the matrix shown in Figure 1. The numeric designations chosen to represent the decimal numbers are shown in Figure 3. Code configurations in excess of binary nine disable the outputs.

The decoder has active LOW outputs so that it may be used directly to drive incandescent displays or light emitting diode indicators.

The device has provision for automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an eight digit mixed interger fraction decimal representation, using the automatic blanking capability, 0060.0300 would be displayed as 60.03. Leading edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RBI}$ input grounded; and, since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing edge zeros.

The decoder has an active LOW input Lamp Test which overrides all other input combinations and allows checking on possible display malfunctions. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve pulse duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

TRUTH TABLE

$\overline{LT}$	$\overline{RBI}$	A_0	A_1	A_2	A_3	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	$\overline{RBO}$	DECIMAL OR FUNCTION
L	X	X	X	X	X	L	L	L	L	L	L	L	H	
H	L	L	L	L	L	H	H	H	H	H	H	L	0	
H	H	L	L	L	L	L	L	L	L	L	H	H	0	
|	X	H	L	L	L	H	H	H	L	L	H	H	1	
|	|	L	H	L	L	L	L	H	L	L	H	L	H	2
|	|	H	H	L	L	L	L	L	L	H	H	L	H	3
|	|	L	L	H	L	H	L	L	H	H	L	L	H	4
|	|	H	L	H	L	L	H	L	L	H	L	L	H	5
|	|	L	H	H	L	H	H	L	L	L	L	L	H	6
|	|	H	H	H	L	L	L	L	H	H	H	H	H	7
|	|	L	L	L	H	L	L	L	L	L	L	L	H	8
|	|	H	L	L	H	L	L	L	H	H	L	L	H	9
|	|	L	H	L	H	H	H	H	H	H	H	H	L	10
|	|	H	H	L	H	H	H	H	H	H	H	H	L	11
|	|	L	L	H	H	H	H	H	H	H	H	H	L	12
|	|	H	L	H	H	H	H	H	H	H	H	H	L	13
|	|	L	H	H	H	H	H	H	H	H	H	H	L	14
H	X	H	H	H	H	H	H	H	H	H	H	H	L	15

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition

Fig. 1
SEGMENT DESIGNATION

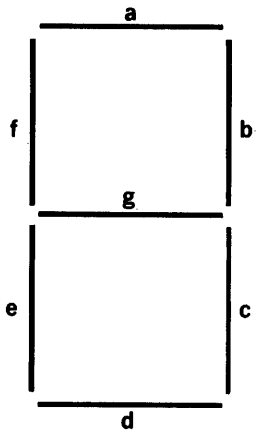


Fig. 2
SEVEN SEGMENT DECODER DRIVING INCANDESCENT LAMP DISPLAY

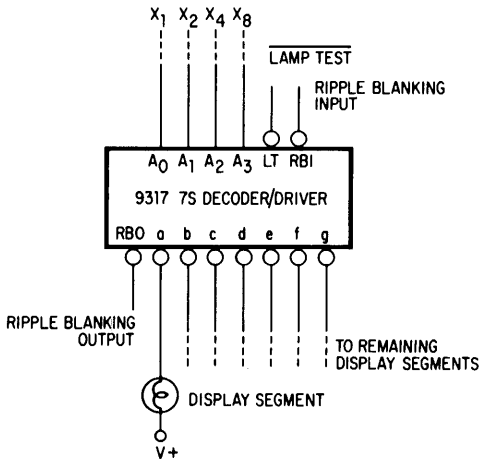
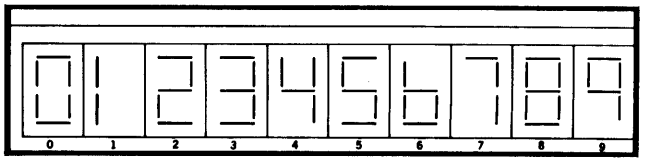


Fig. 3
NUMERICAL DESIGNATIONS



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature		−65°C to +150°C
Temperature (Ambient) Under Bias		−55°C to +125°C
V_{CC} Pin Potential to Ground Pin		−0.5 V to +7.0 V
Voltage Applied to Outputs for HIGH Output State		−0.5 V to +30 V
Input Voltage (dc)		−0.5 V to +5.5 V
Current Into Outputs		80 mA
Power Dissipation per Output	9317B	50 mW
	9317C	30 mW

ELECTRICAL CHARACTERISTICS (T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. 9317BXM • 9317CXM)*

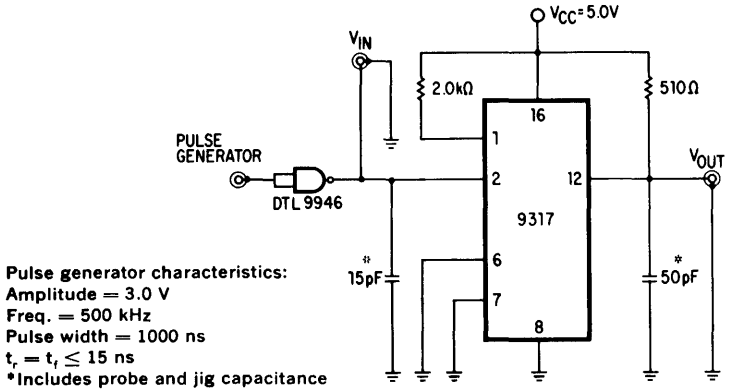
SYMBOL	PARAMETER		LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0	4.0		3.0		Volts	V_{CC} = 4.5 V, I_{OH} = −70 μA Pin 5 = V_{IH}, Pins 1, 2, 6, 7 = 0 V
I_{CEX}	Output HIGH Leakage Current					100	200		250	μA	V_{CC} = 5.5 V, V_{CEX} = 30 V (CXM), 20 V (BXM) Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.4		0.21	0.4		0.4	Volts	V_{CC} = 5.5 V, I_{OL} = 3.1 mA; Inputs at V_{IH} or V_{IL} per Truth Table
				0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 2.4 mA
V_{OL}	Output LOW Voltage	9317BXM		0.8		0.50	0.8		0.8	Volts	V_{CC} = 4.5 V, I_{OL} = 40 mA Pin 3 = 0 V
		9317CXM		0.4		0.21	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 20 mA Pin 3 = 0 V
V_{LATCH}	Output Latch Voltage	9317BXM	20		20			20		Volts	V_{CC} = 5.0 V, I_{OUT} = 10 mA
		9317CXM	30		30			30		Volts	Inputs = Open
V_{IH}	Input HIGH Voltage		2.1		1.9			1.7		Volts	Guaranteed Input HIGH Threshold for All Inputs
V_{IL}	Input LOW Voltage			1.4			1.1		0.8	Volts	Guaranteed Input LOW Threshold for All Inputs
I_{IL}	Input LOW Current $\overline{LT}$ A_0, A_1, A_2, A_3 $\overline{RBI}$			−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA mA mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V V_{IN} = 5.5 V on Other Inputs
I_{IH}	Input HIGH Current $\overline{LT}$ $\overline{RBI}$, A_0, A_1, A_2, A_3						200 40		200 40	μA μA	V_{CC} = 5.5 V, V_{IN} = 2.4 V GND on Other Inputs
t_{PLH} t_{PHL}	Turn Off Delay Turn On Delay						500 500			ns ns	V_{CC} = 5.0 V, See Figure 4

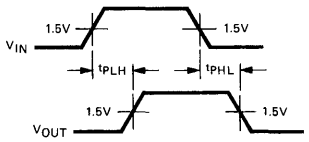
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9317BXC • 9317CXC)*

SYMBOL	PARAMETER		LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage on $\overline{RBO}$ Only		3.0		3.0	4.0		3.0		Volts	V_{CC} = 4.75 V, I_{OH} = −70 μA Pin 5 = V_{IH}, Pins 1, 2, 6, 7 = 0 V
I_{CEX}	Output HIGH Leakage Current					100	200		250	μA	V_{CC} = 5.25 V, V_{CEX} = 30 V (CXC), 20 V (BXC) Inputs at V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage on $\overline{RBO}$ Only			0.45		0.25	0.45		0.45	Volts	V_{CC} = 5.25 V, I_{OL} = 2.75 mA; Inputs at V_{IH} or V_{IL} per Truth Table
				0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 2.4 mA
V_{OL}	Output LOW Voltage	9317BXC		0.9		0.65	0.9		0.9	Volts	V_{CC} = 4.75 V, I_{OL} = 40 mA Pin 3 = 0 V
		9317CXC		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 20 mA Pin 3 = 0 V
V_{LATCH}	Output Latch Voltage	9317BXC	20		20			20		Volts	V_{CC} = 5.0 V, I_{OUT} = 10 mA
		9317CXC	30		30			30		Volts	Inputs = Open
V_{IH}	Input HIGH Voltage		2.0		2.0			2.0		Volts	Guaranteed Input HIGH Threshold for All Inputs
V_{IL}	Input LOW Voltage			0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold for All Inputs
I_{IL}	Input LOW Current $\overline{LT}$ A_0, A_1, A_2, A_3 $\overline{RBI}$			−6.4 −1.5 −0.75			−6.4 −1.5 −0.75		−6.4 −1.5 −0.75	mA mA mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V V_{IN} = 5.25 V on Other Inputs
I_{IH}	Input HIGH Current $\overline{LT}$ $\overline{RBI}$, A_0, A_1, A_2, A_3						200 40		200 40	μA μA	V_{CC} = 5.25 V, V_{IN} = 2.4 V GND on Other Inputs
t_{PLH} t_{PHL}	Turn Off Delay Turn On Delay						500 500			ns ns	V_{CC} = 5.0 V, See Figure 4

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

Fig. 4 – SWITCHING CIRCUIT AND WAVEFORMS

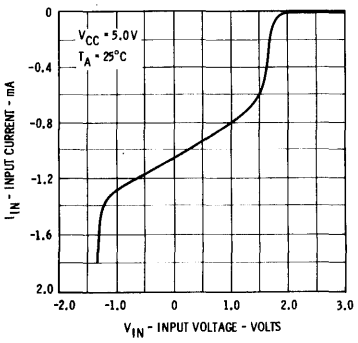




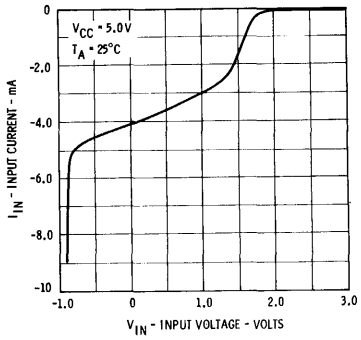
TYPICAL INPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE

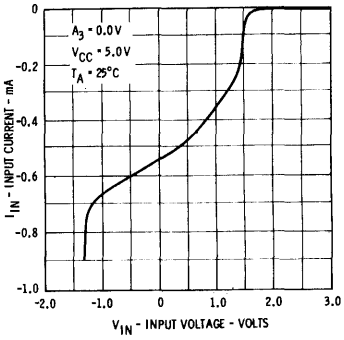
A_0, A_1, A_2, A_3 INPUTS



$\overline{LT}$ INPUT

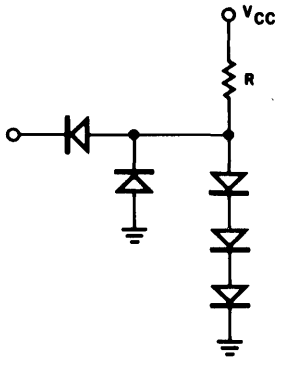


$\overline{RBI}$ INPUT



INPUTS

EQUIVALENT CIRCUIT



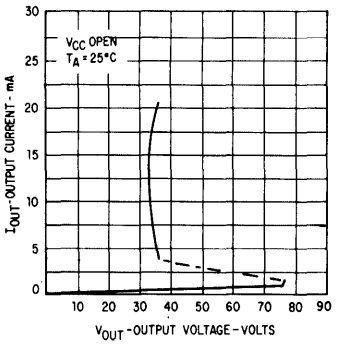
8

OUTPUT CHARACTERISTICS

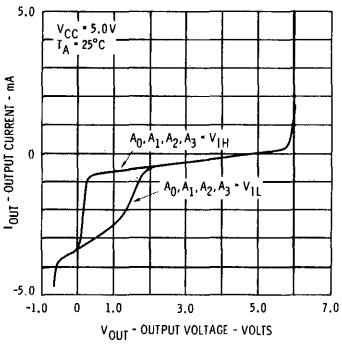
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE
9317BXM, 9317BXC

TYPICAL OUTPUT IN HIGH STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS

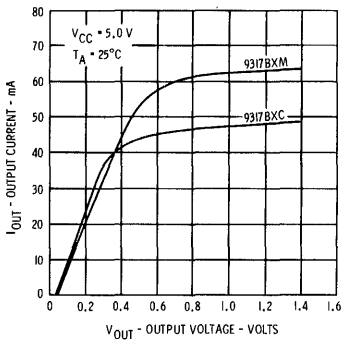


$\overline{RBO}$ OUTPUT

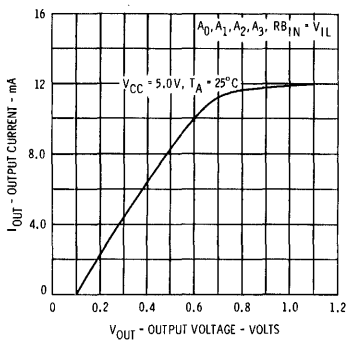


TYPICAL OUTPUT IN LOW STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS



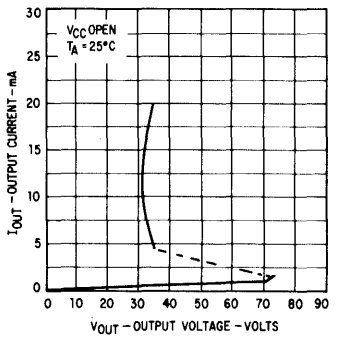
$\overline{RBO}$ OUTPUT



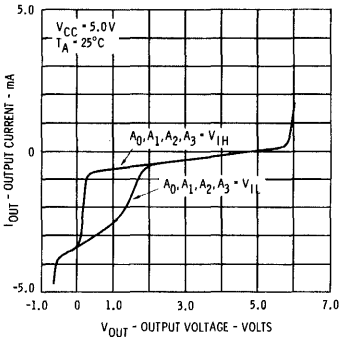
9317CXM, 9317CXC

TYPICAL OUTPUT IN HIGH STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS

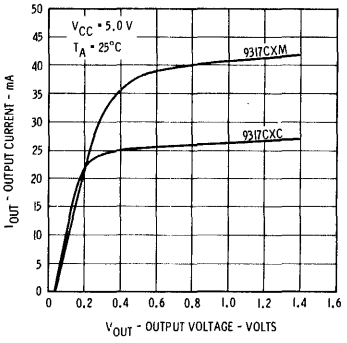


$\overline{RBO}$ OUTPUT

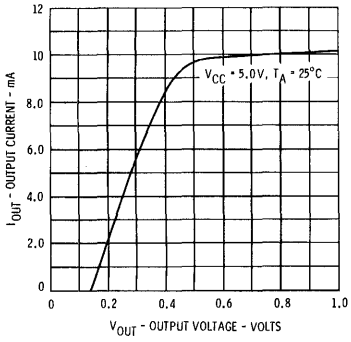


TYPICAL OUTPUT IN LOW STATE

$\overline{a}, \overline{b}, \overline{c}, \overline{d}, \overline{e}, \overline{f}, \overline{g}$ OUTPUTS

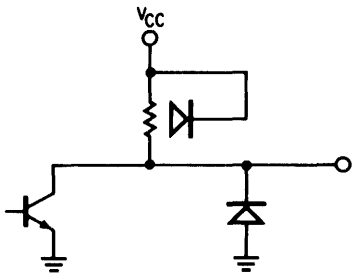


$\overline{RBO}$ OUTPUT

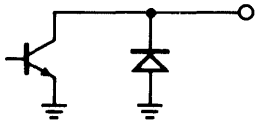


OUTPUTS

EQUIVALENT CIRCUIT (PIN 4)



EQUIVALENT CIRCUIT (Pins 9 thru 15)



TTL/MSI 9318
EIGHT-INPUT PRIORITY ENCODER

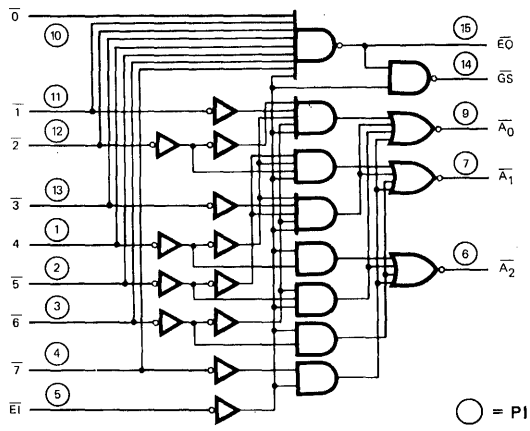
DESCRIPTION — The TTL/MSI 9318 is a Multipurpose Encoder designed to accept eight inputs and produce a binary weighted code of the highest order input. The circuit uses TTL for high speed and high fanout capability, and is compatible with all members of the Fairchild TTL family.

- **MULTI-FUNCTION CAPABILITY**
  - **CODE CONVERSIONS**
  - **MULTI-CHANNEL D/A CONVERTER**
  - **DECIMAL TO BCD CONVERTER**
  - **CASCADING FOR PRIORITY ENCODING OF N BITS**
- **INPUT ENABLE CAPABILITY**
- **PRIORITY ENCODING – AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE**
- **OUTPUT ENABLE – ACTIVE LOW WHEN ALL INPUTS HIGH**
- **GROUP SIGNAL OUTPUT – ACTIVE WHEN ANY INPUT IS LOW**
- **TYPICAL POWER DISSIPATION OF 250 mW**
- **INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **ALL CERAMIC HERMETIC 16-LEAD DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

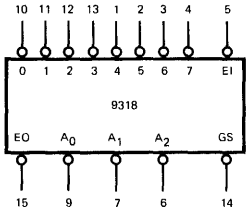
PIN NAMES		LOADING (Note a)
$\overline{0}$	Priority (Active LOW) Input	1 U.L.
$\overline{1}$ to $\overline{7}$	Priority (Active LOW) Inputs	2 U.L.
$\overline{EI}$	Enable (Active LOW) Input	2 U.L.
$\overline{EO}$	Enable (Active LOW) Output	10 U.L.*
$\overline{GS}$	Group Select (Active LOW) Output	10 U.L.*
$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$	Address (Active LOW) Outputs	10 U.L.*

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

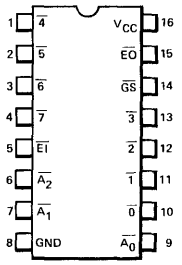


LOGIC SYMBOL

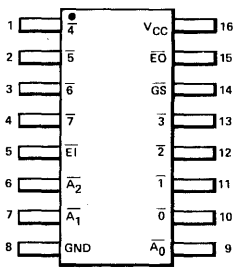


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The 9318 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

A HIGH on the Input Enable ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal output ($\overline{GS}$) and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active level LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are inactive HIGH when the input enable is HIGH.

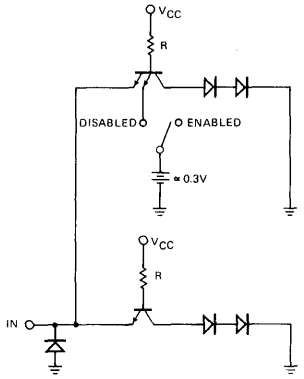
TABLE I – TRUTH TABLE

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

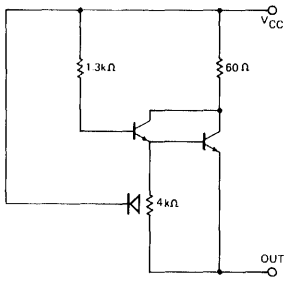
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

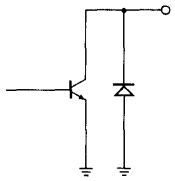
EQUIVALENT INPUT CIRCUIT



OUTPUT HIGH EQUIVALENT CIRCUIT



OUTPUT LOW EQUIVALENT CIRCUIT



INPUT CURRENT VERSUS INPUT VOLTAGE

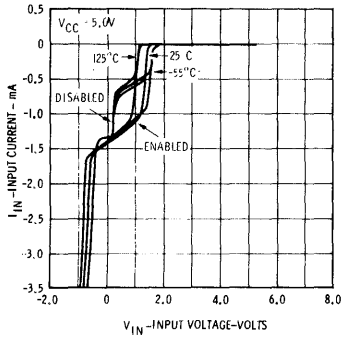


Fig. 1.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH STATE

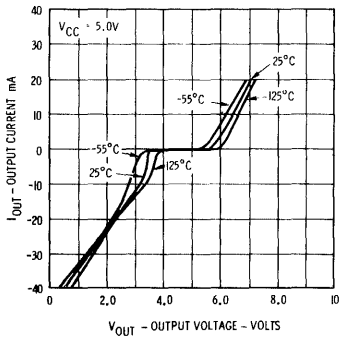


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW STATE

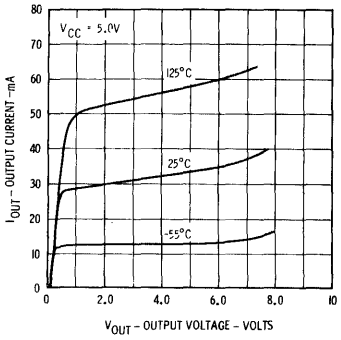


Fig. 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9318XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9318XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{I_0}$ (Pin 10) $\overline{EI}$, $\overline{I_1}$–$\overline{I_7}$		 10 20	 40 80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current $\overline{I_0}$ (Pin 10) $\overline{EI}$, $\overline{I_1}$–$\overline{I_7}$		 −0.96 −1.92	 −1.6 −3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		50	77	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

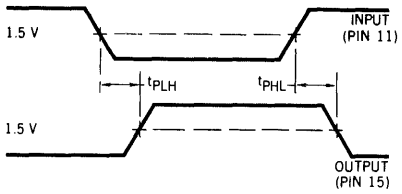
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9318XM(MIL)		9318XC(IND)		UNITS	CONDITIONS	
		MIN.	MAX.	MIN.	MAX.			
t_{PLH} t_{PHL}	Data Input to Enable Output		10 30		15 40	ns ns	See Figure 4	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Enable Input to Group Signal		16 25		20 31	ns ns	See Figure 5	
t_{PLH} t_{PHL}	Enable Input to Enable Output		15 40		21 45	ns ns	See Figure 6	
t_{PLH} t_{PHL}	Enable Input to Data Output		20 25		25 30	ns ns	See Figure 7	
t_{PLH} t_{PHL}	Data Input to Group Signal		40 25		45 30	ns ns	See Figure 8	
t_{PLH} t_{PHL}	Data Input to Data Output		30 30		38 38	ns ns	See Figure 9	

8

SWITCHING CHARACTERISTICS

DATA INPUT TO ENABLE OUTPUT



Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

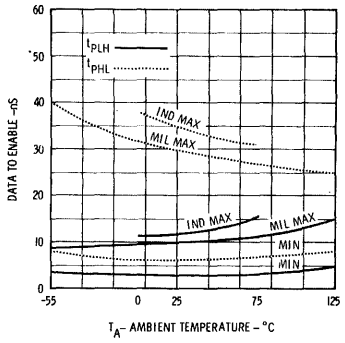
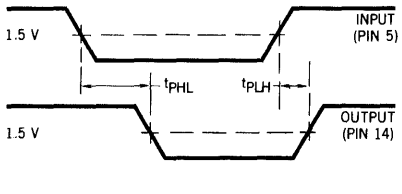


Fig. 4.

ENABLE INPUT TO GROUP SIGNAL



Other Conditions: Pin 10 - GND
Pins 1, 2, 3, 4, 11, 12, 13 =
V_{CC} through 750 Ω

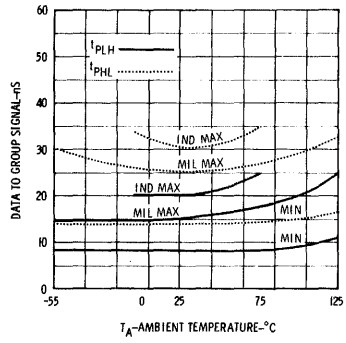
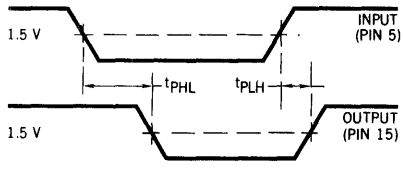


Fig. 5.

ENABLE INPUT TO ENABLE OUTPUT



Other Conditions:
Pins 1, 2, 3, 4, 10, 11, 12, 13 =
V_{CC} through 750 Ω

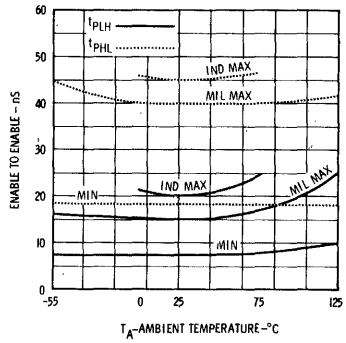
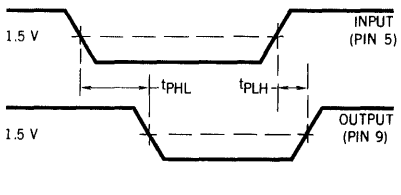


Fig. 6.

ENABLE INPUT TO DATA OUTPUT



Other Conditions: Pin 4 = GND
Pins 1, 2, 3, 10, 11, 12, 13 =
V_{CC} through 750 Ω

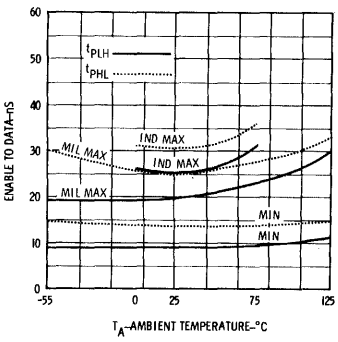
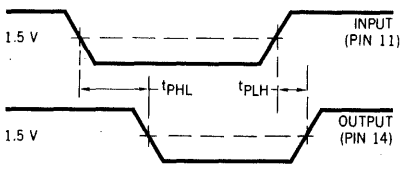


Fig. 7.

DATA INPUT TO GROUP SIGNAL



Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

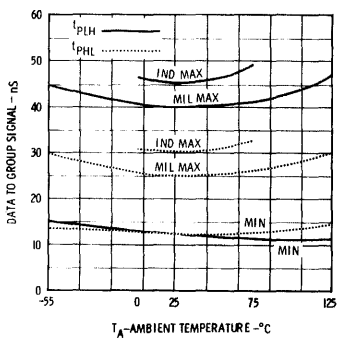
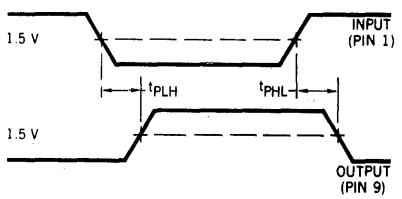


Fig. 8.

DATA INPUT TO DATA OUTPUT



Other Conditions: Pins 5, 11 = GND
Pins 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

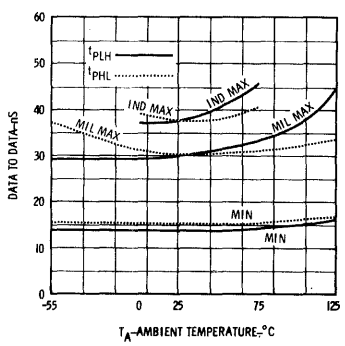


Fig. 9.

LPTTL/MSI 93L18
LOW POWER EIGHT-INPUT PRIORITY ENCODER

DESCRIPTION — The LPTTL/MSI 93L18 is a Multipurpose Encoder designed to accept eight inputs and produce a binary weighted code of the highest order input. The circuit uses TTL technology for high speed and high fanout capability, and is compatible with all Fairchild TTL families.

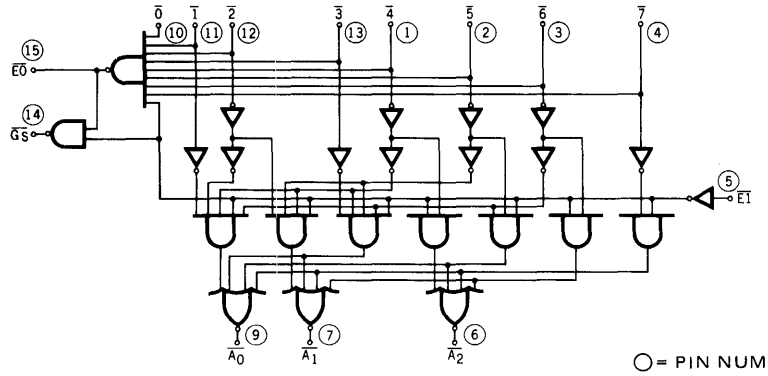
- **MULTI-FUNCTION CAPABILITY**
  - **CODE CONVERSIONS**
  - **MULTI-CHANNEL D/A CONVERTER**
  - **DECIMAL TO BCD CONVERTER**
  - **CASCADING FOR PRIORITY ENCODING OF N BITS**
- **INPUT ENABLE CAPABILITY**
- **PRIORITY ENCODING – AUTOMATIC SELECTION OF HIGHEST PRIORITY INPUT LINE**
- **OUTPUT ENABLE – ACTIVE LOW WHEN ALL INPUTS HIGH**
- **GROUP SIGNAL OUTPUT – ACTIVE WHEN ANY INPUT IS LOW**
- **TYPICAL PROPAGATION DELAY OF 55 ns**
- **TYPICAL POWER DISSIPATION OF 75 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC HERMETIC 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

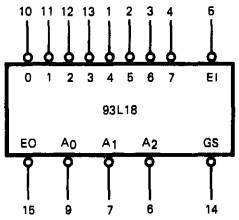
		LOADING	
		HIGH	LOW
$\overline{0}$	Priority (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{1}$ to $\overline{7}$	Priority (Active LOW) Inputs	1.0 U.L.	0.5 U.L.
$\overline{EI}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{EO}$	Enable (Active LOW) Output	10 U.L.	1.25 U.L.
$\overline{GS}$	Group Select (Active LOW) Output	10 U.L.	1.5 U.L.
$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$	Address (Active LOW) Outputs	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

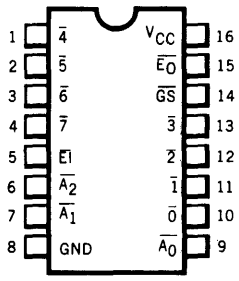


LOGIC SYMBOL

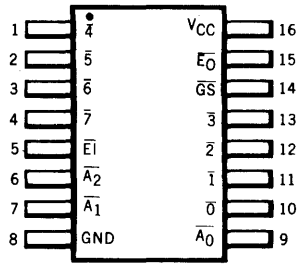


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The LPTTL/MSI 93L18 8-input priority encoder accepts data from eight active LOW inputs and provides a binary representation on the three active LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line 7 having the highest priority.

A HIGH on the input enable ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

Provided with the three data outputs are a group signal output ($\overline{GS}$) and an enable output ($\overline{EO}$). The $\overline{GS}$ is active level LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active level LOW when all inputs are HIGH. Using the output enable along with the input enable allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are inactive when the input enable is HIGH.

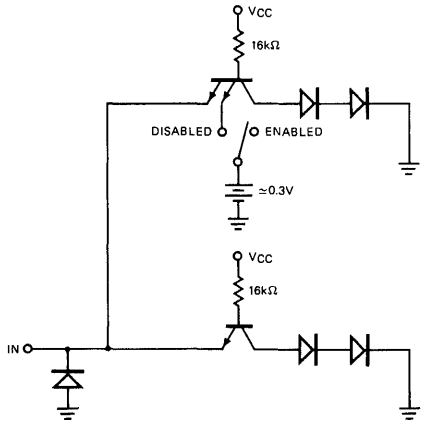
TRUTH TABLE

$\overline{EI}$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

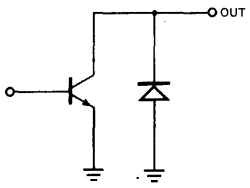
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

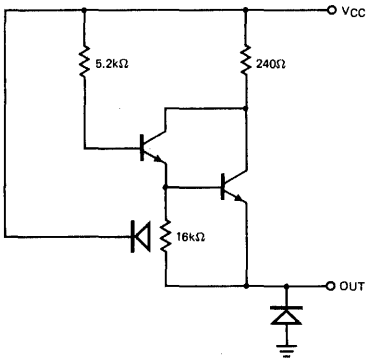


OUTPUTS EQUIVALENT CIRCUIT

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L18XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L18XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pins 6, 7, 9) I_{OL} = 2.4 mA (Pin 14) I_{OL} = 2.0 mA (Pin 15) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current Input $\overline{0}$ (Pin 10) Inputs $\overline{1}$ thru $\overline{7}$ & $\overline{EI}$		 −0.25 −0.50	 −0.4 −0.8	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current Input $\overline{0}$ (Pin 10) Inputs $\overline{1}$ thru $\overline{7}$ & $\overline{EI}$		 2.0 4.0	 20 40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		15	22	mA	V_{CC} = MAX., Pins 4 & 5 at GND

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 8 = GND)

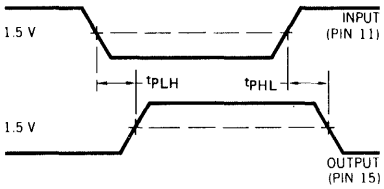
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH} t_{PHL}	Data Input to Enable Output Data Input to Enable Output		10 68	15 100	ns	See Figure 1
t_{PLH} t_{PHL}	Enable Input to Group Signal Enable Input to Group Signal		16 38	27 57	ns	See Figure 2
t_{PLH} t_{PHL}	Enable Input to Enable Output Enable Input to Enable Output		16 68	27 100	ns	See Figure 3
t_{PLH} t_{PHL}	Enable Input to Data Output Enable Input to Data Output		23 38	35 57	ns	See Figure 4
t_{PLH} t_{PHL}	Data Input to Group Signal Data Input to Group Signal		59 38	89 57	ns	See Figure 5
t_{PLH} t_{PHL}	Data Input to Data Output Data Input to Data Output		33 51	50 77	ns	See Figure 6

8

TYPICAL SWITCHING CHARACTERISTICS

All measurements are made with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTL gate. The input and output pins under test are loaded with 15 pF of capacitance. (This includes probe & jig capacitance.)

Fig. 1. Data Input to Enable Output



Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

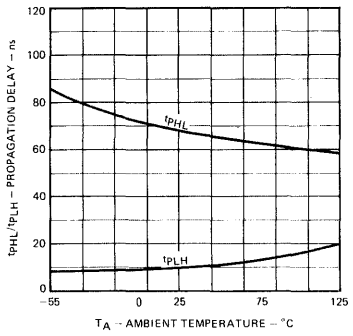
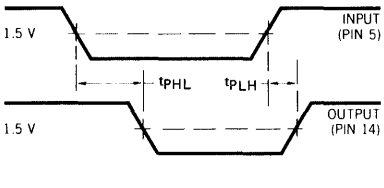


Fig. 2. Enable Input to Group Signal



Other Conditions: Pin 10 = GND
Pins 1, 2, 3, 4, 11, 12, 13 =
V_{CC} through 750 Ω

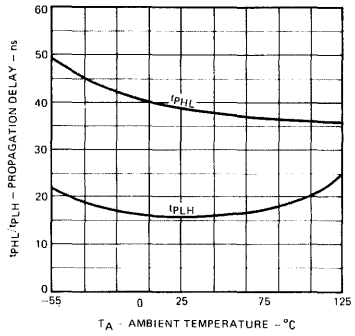
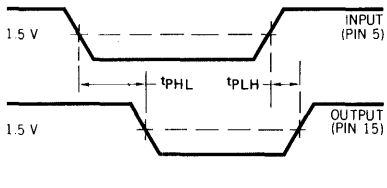


Fig. 3. Enable Input to Enable Output



Other Conditions:
Pins 1, 2, 3, 4, 10, 11, 12, 13 =
V_{CC} through 750 Ω

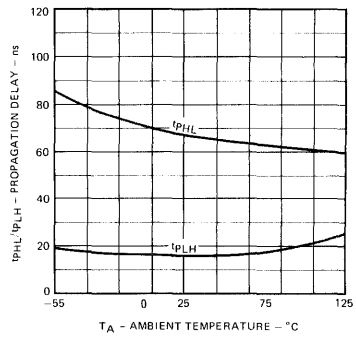
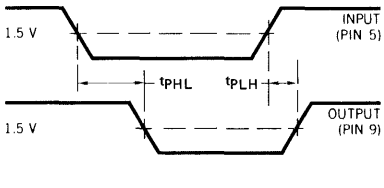


Fig. 4. Enable Input to Data Output



Other Conditions: Pin 4 = GND
Pins 1, 2, 3, 10, 11, 12, 13 =
V_{CC} through 750 Ω

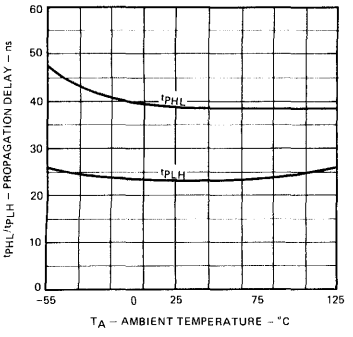
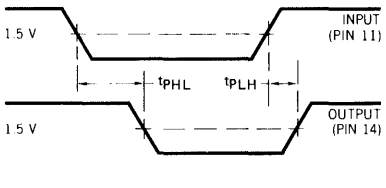


Fig. 5. Data Input to Group Signal



Other Conditions: Pin 5 = GND
Pins 1, 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

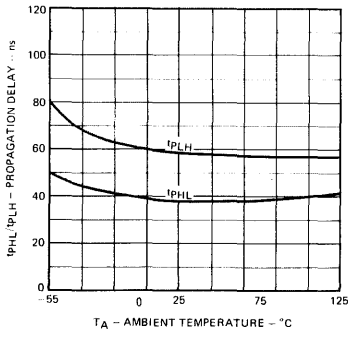
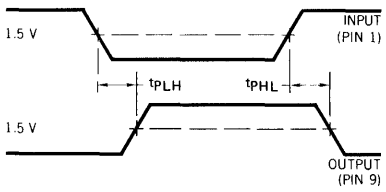
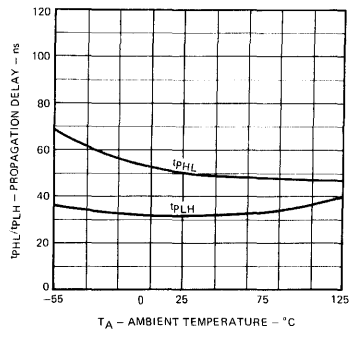


Fig. 6. Data Input to Data Output



Other Conditions: Pins 5, 11 = GND
Pins 2, 3, 4, 10, 12, 13 =
V_{CC} through 750 Ω

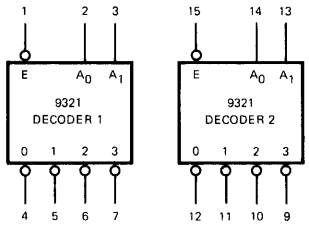


TTL/MSI 9321
DUAL ONE-OF-FOUR DECODER

DESCRIPTION — The TTL/MSI 9321 consists of two Independent Multipurpose Decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition, an active LOW enable input is provided for each decoder which gives demultiplexing capability. The circuit uses TTL for high speed and high fanout capability, and is compatible with all members of the Fairchild TTL family.

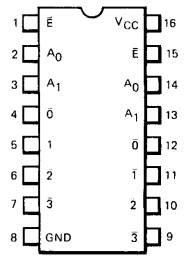
- **MULTI-FUNCTION CAPABILITY**
- **MUTUALLY EXCLUSIVE OUTPUTS**
- **GUARANTEED FANOUT OF 10 TTL LOADS OVER THE FULL TEMPERATURE RANGE AND SUPPLY VOLTAGE RANGES**
- **HIGH CAPACITIVE DRIVE CAPABILITY**
- **DEMULTIPLEXING CAPABILITY**
- **TYPICAL POWER DISSIPATION OF 150 mW**
- **THE INPUT / OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD MSI, DTL, LPDTL AND TTL FAMILIES**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS**
- **ACTIVE LOW ENABLE FOR EACH DECODER**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)

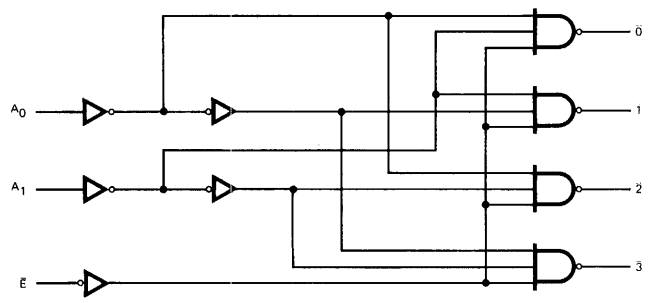


PIN NAMES

		LOADING (Note a)
Decoder 1 and 2		
$\overline{E}$	Enable (Active LOW) Input	1 U.L.
A_0, A_1	Address Inputs	1 U.L.
$\overline{0}$, $\overline{1}$, $\overline{2}$, $\overline{3}$	(Active LOW) Outputs (Note b)	10 U.L.

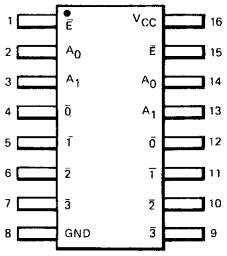
Notes:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



Note: Only one Decoder shown.

FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The 9321 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in logic symbol. Each decoder can be used as a 4-output demultiplexer by using the enable as a data input.

The active LOW outputs facilitate memory addressing for units such as the 93402 associative memory. The active LOW outputs are also compatible with the active LOW enables of other MSI elements making the 9321 useful in logic selection schemes.

TRUTH TABLE

DECODER 1 & 2

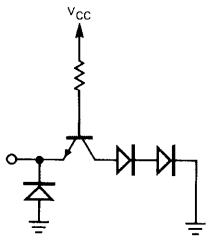
$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

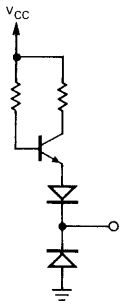
INPUTS

EQUIVALENT CIRCUIT

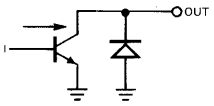


OUTPUTS

EQUIVALENT CIRCUIT OUTPUT HIGH



EQUIVALENT CIRCUIT OUTPUT LOW



INPUT CURRENT VERSUS INPUT VOLTAGE

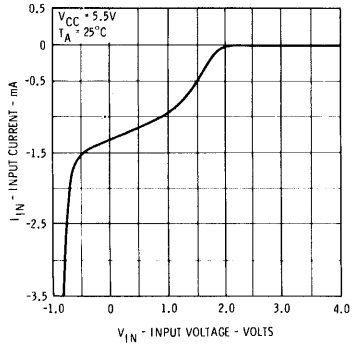


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT HIGH

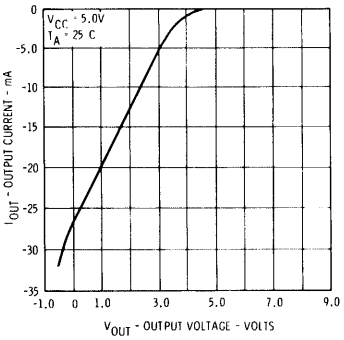


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE OUTPUT LOW

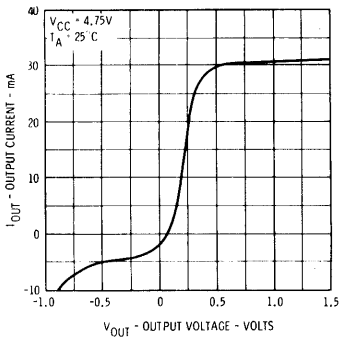


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9321XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9321XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA., T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−40	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		30	50	mA	V_{CC} = MAX.

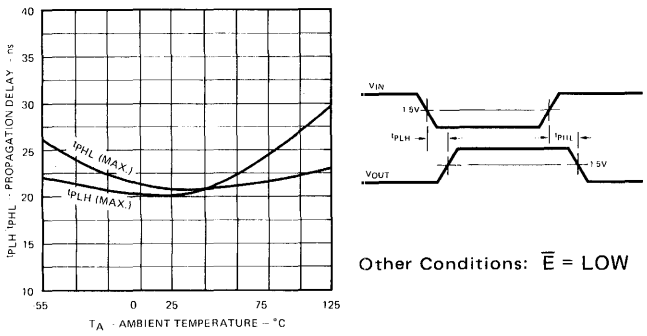
NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH} t_{PHL}	Turn Off Delay A Input to Output Turn On Delay A Input to Output		13 14	20 21	ns ns	See Figure 4	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Turn Off Delay E Input to Output Turn On Delay E Input to Output		9 12	14 18	ns ns	See Figure 5	

SWITCHING CHARACTERISTICS

ADDRESS INPUT TO OUTPUT



Other Conditions: $\overline{E}$ = LOW

Fig. 4.

ENABLE INPUT TO OUTPUT

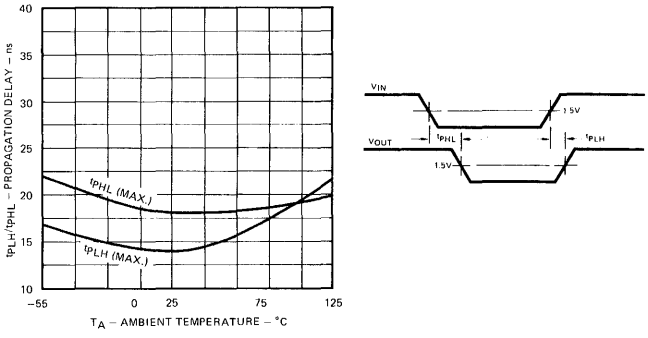


Fig. 5.

LPTTL/MSI 93L21

LOW POWER DUAL ONE-OF-FOUR DECODER

DESCRIPTION – The LPTTL/MSI 93L21 consists of two independent multipurpose decoders, each designed to accept two inputs and provide four mutually exclusive outputs. In addition an active LOW enable input is provided for each decoder which gives demultiplexing capability. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

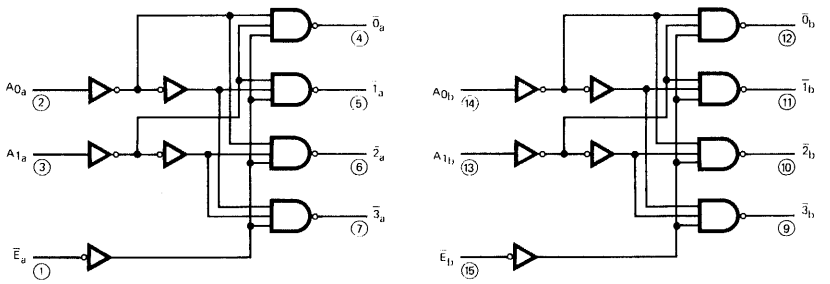
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- HIGH CAPACITIVE DRIVE CAPABILITY
- DEMULTIPLEXING CAPABILITY
- ACTIVE LOW ENABLE FOR EACH DECODER
- TYPICAL PROPAGATION DELAY OF 50 ns
- TYPICAL POWER DISSIPATION OF 45 mW
- INPUT CLAMP DIODES LIMIT HIGH SPEED LINE TERMINATION EFFECTS
- ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES
- TTL COMPATIBLE

PIN NAMES
Decoder 1 and 2

		LOADING HIGH	LOADING LOW
$\bar{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\bar{0}$, $\bar{1}$, $\bar{2}$, $\bar{3}$	(Active LOW) Outputs	10 U.L.	2.5 U.L.

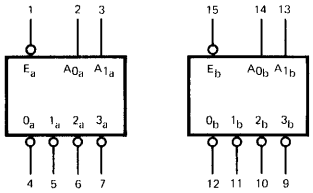
1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



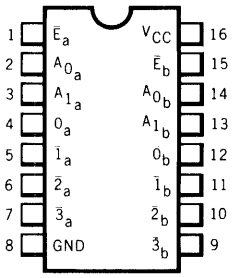
○ = PIN NUMBERS

LOGIC SYMBOL

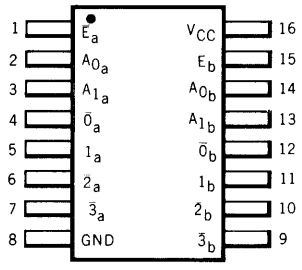


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93L21 consists of two separate decoders each designed to accept two binary weighted inputs and provide four mutually exclusive active LOW outputs as shown in logic symbol. Each decoder can be used as a four output demultiplexer by using the enable as a data input.

The active LOW outputs facilitate memory addressing for units such as the 93402 associative memory. The active LOW outputs are also compatible with the active LOW enables of other LPTTL/MSI elements making the 93L21 useful in logic selection schemes.

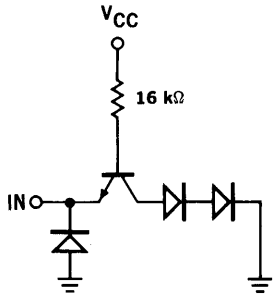
TRUTH TABLE
DECODER I & II

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Level Does Not Affect Output

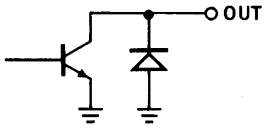
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

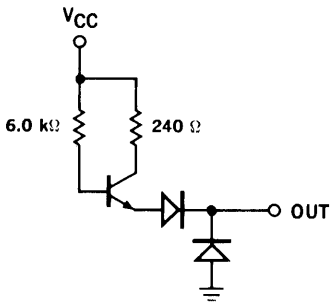


OUTPUTS EQUIVALENT CIRCUITS

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L21XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L21XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		9.0	13.2	mA	V_{CC} = MAX., All Inputs at GND

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

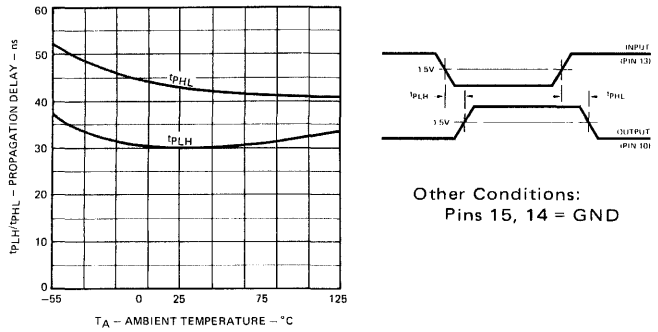
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay A Input to Output		30	50	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay A Input to Output		43	65	ns	C_L = 15 pF, (See Fig. 1)
t_{PLH}	Turn Off Delay E Input to Output		23	40	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay E Input to Output		34	52	ns	C_L = 15 pF, (See Fig. 2)

SWITCHING TIME AND WAVEFORMS

All measurements are made with V_{CC} = 5.0 V applied to Pin 16 and Pin 8 grounded. The active input is driven by a 9002 TTL gate. The input and output pins under test are loaded with 15 pF of capacitance (this includes probe and jig capacitance).

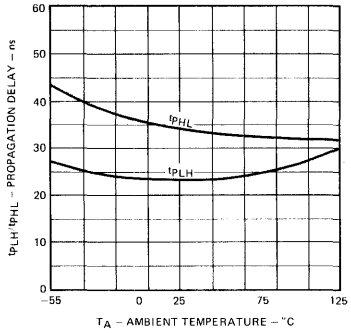
ADDRESS INPUT TO OUTPUT

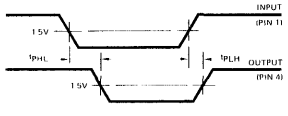


Other Conditions:
Pins 15, 14 = GND

Fig. 1.

ENABLE INPUT TO OUTPUT





Other Conditions:
Pins 2, 3 = GND

Fig. 2.

TTL/MSI 9322
QUAD TWO-INPUT MULTIPLEXER

DESCRIPTION – The TTL/MSI 9322 is a Monolithic, High Speed, Quad Two-Input Digital Multiplexer Circuit, constructed with the Fairchild Planar* epitaxial process. It consists of four multiplexing circuits with common select and enable logic; each circuit contains two inputs and one output. The circuit uses TTL for high speed, high fan out operation and is compatible with all other members of the Fairchild TTL family.

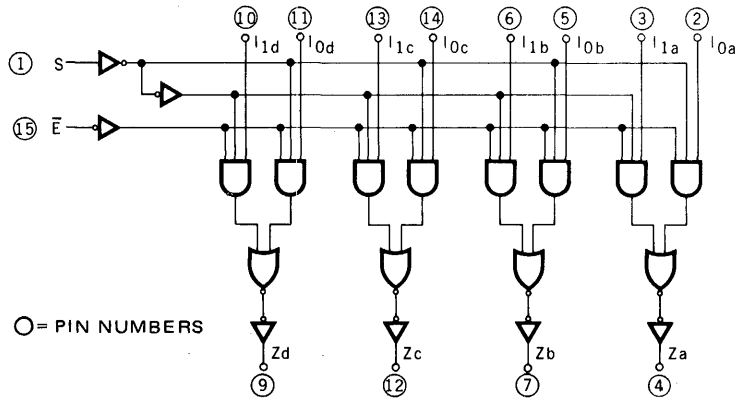
- **MULTIFUNCTION CAPABILITY***
- **20 ns THROUGH DELAY**
- **ON-CHIP SELECT LOGIC DECODING**
- **FULLY BUFFERED OUTPUTS**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATIONS EFFECTS**

PIN NAMES

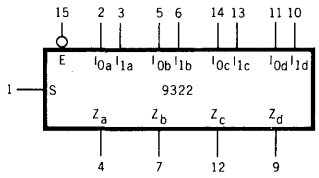
		LOADING (Note a)
S	Common Selected Input	1 U.L.
$\overline{E}$	Enable (Active LOW) Inputs	1 U.L.
$I_{0a}, I_{1a}, I_{0b}, I_{1b}, I_{0c}, I_{1c}, I_{0d}, I_{1d}$	Multiplexer Inputs	1.U.L.
Z_a, Z_b, Z_c, Z_d	Multiplexer Output (Note b)	10 U.L.

Notes:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

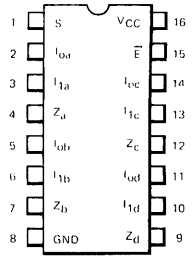


LOGIC SYMBOL

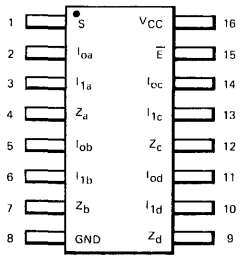


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



*Planar is a patented Fairchild process.

8

FUNCTIONAL DESCRIPTION — The 9322 quad 2-input multiplexer is a member of the Fairchild family of compatible Medium Scale Integrated (MSI) digital building blocks. It provides this family with the ability to select four bits of either data or control from two sources, in one package. The Enable input ($\overline{E}$) is active LOW. When not activated all outputs (Z) are LOW regardless of all other inputs.

The 9322 quad 2-input multiplexer is the logical implementation of a four-pole, two position switch, with the position of the switch being set by the logic levels supplied to the one select input. The logic equations for the outputs are shown below:

$$Z_a = E \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = E \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = E \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = E \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

A common use of the 9322 is the moving of data from a group of registers to four common output busses. The particular register from which the data comes is determined by the state of the select input. A less obvious use is as a function generator. The 9322 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

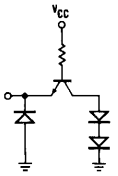
TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S	I_{0X}	I_{1X}	Z_X
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

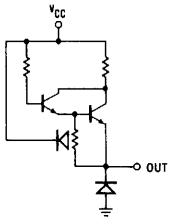
H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Logic Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

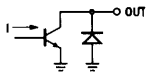
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

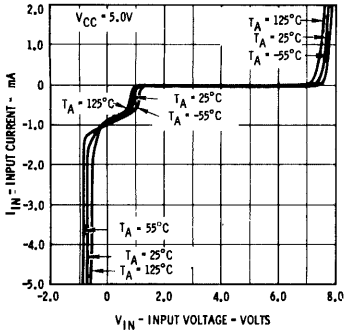


Fig. 1.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

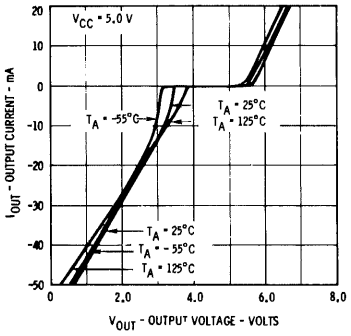


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

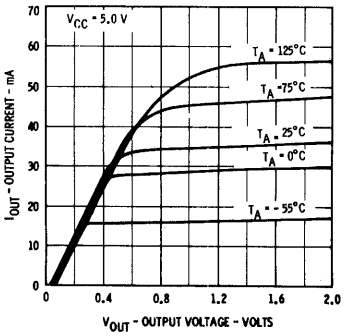


Fig. 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9322XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9322XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		−0.96	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	-30	-60	-100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		30	47	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9322XM(MIL)			9322XC(IND)			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output (S to Z)		17	25		17	30	ns	V_{CC} = 5.0 V C_L = 15 pF	See Figure 4
t_{PHL}	Turn On Delay Input to Output (S to Z)		20	27		20	31	ns		

SWITCHING CHARACTERISTICS

Fig. 4.

t_{PLH}/t_{PHL} – S to Z

Other Conditions: $\overline{E}$ = L, I_0 = L, I_1 = H

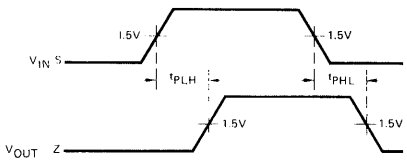


Fig. 5.

t_{PLH}/t_{PHL} – $\overline{E}$ to Z

Other Conditions: All Other Inputs HIGH

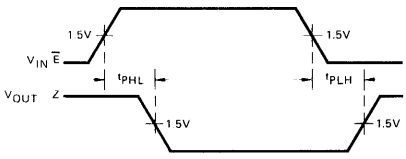
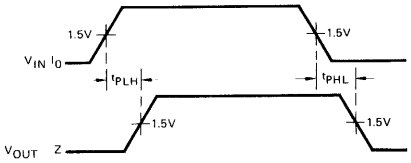


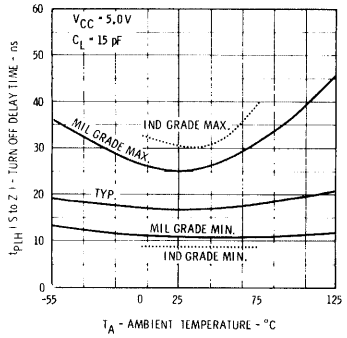
Fig. 6.

t_{PLH}/t_{PHL} – I_0 to Z

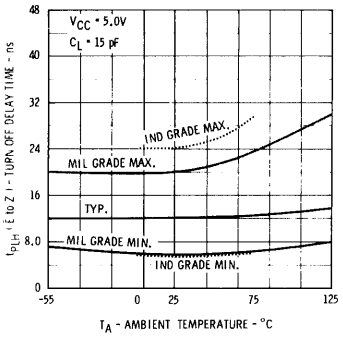
Other Conditions: $\overline{E}$ = L, S = L



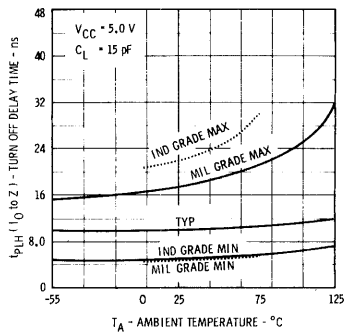
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z)



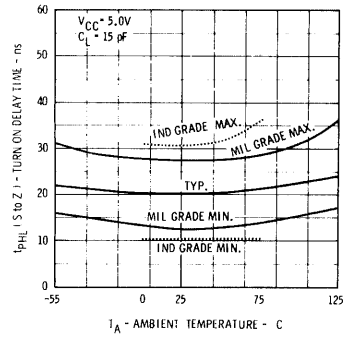
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z)



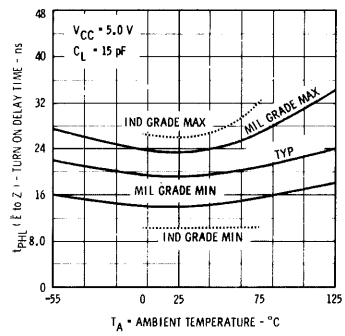
TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (I_0 to Z)



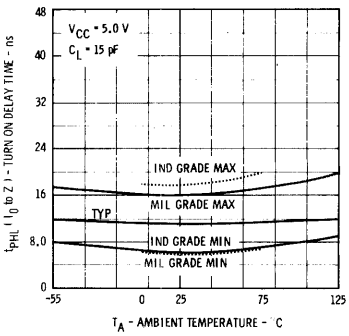
TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (S to Z)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\overline{E}$ to Z)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (I_0 to Z)



LPTTL/MSI 93L22
LOW POWER QUAD TWO-INPUT MULTIPLEXER

DESCRIPTION – The LPTTL/MSI 93L22 is a monolithic, medium speed, Quad Two-Input Digital Multiplexer, constructed with the Fairchild Planar* epitaxial process. It consists of four multiplexing circuits with common select and enable logic. Each circuit contains two inputs and one output. The circuit uses TTL technology and is compatible with the Fairchild TTL family.

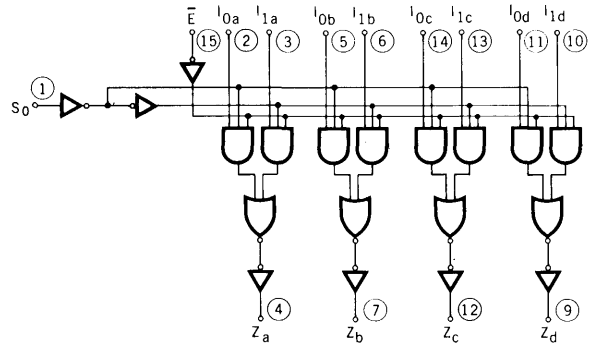
- **MULTIFUNCTION CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **TYPICAL PROPAGATION DELAY OF 44 ns**
- **TYPICAL POWER DISSIPATION OF 45 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

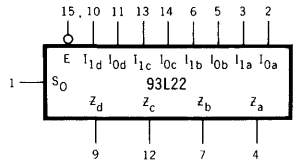
		LOADING HIGH	LOADING LOW
S_0	Common Select Input	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
I_0, I_1	Multiplexers Inputs	0.5 U.L.	0.25 U.L.
Z	Multiplexer Output	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

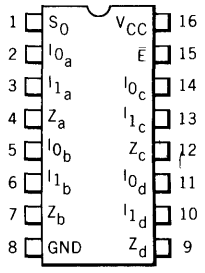


LOGIC SYMBOL

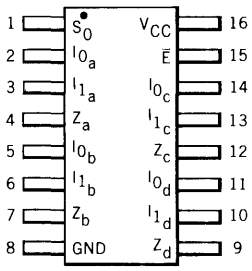


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



*Planar is a patented Fairchild process.

8

FUNCTIONAL DESCRIPTION – The 93L22 quad two-input multiplexer is a member of the Fairchild family of low power medium scale integrated digital building blocks. It provides, in one package, the ability to select four bits of either data or control from four 2-bit sources. The enable input ($\overline{E}$) is active LOW. When not activated all outputs (Z) are LOW regardless of all other inputs. The 93L22 quad two input multiplexer is the logical implementation of a four-pole two position switch, with the position of the switch being set by the logic level supplied to the one select input. The logic equations for the outputs are shown below:

$$Z_a = E \cdot (I_{1a} \cdot S_0 + I_{0a} \cdot \overline{S_0}) \quad Z_b = E \cdot (I_{1b} \cdot S_0 + I_{0b} \cdot \overline{S_0}) \quad Z_c = E \cdot (I_{1c} \cdot S_0 + I_{0c} \cdot \overline{S_0}) \quad Z_d = E \cdot (I_{1d} \cdot S_0 + I_{0d} \cdot \overline{S_0})$$

A common use of the 93L22 is the moving of data from two registers to common output busses. The particular register from which the data came would be determined by the state of the select input. A less obvious use is a function generator. The 93L22 can generate four functions of two variables with one variable common. This is useful implementing gating functions.

TRUTH TABLE

Identical for Each Multiplexer

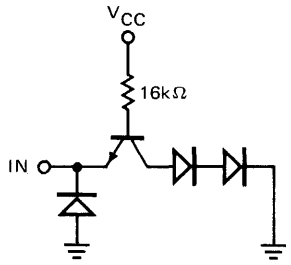
ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{E}$	S_0	I_{0Y}	I_{1Y}	Z_Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level X = Level does not affect output

L = LOW voltage level Y = a, b, c, d

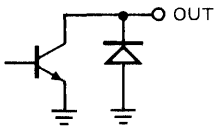
TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUTS
EQUIVALENT CIRCUIT

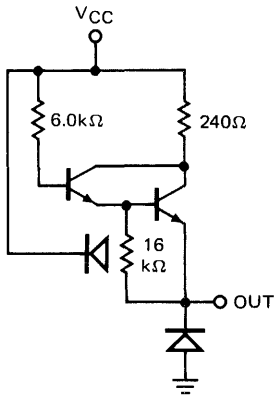


OUTPUTS
EQUIVALENT CIRCUITS

OUTPUT LOW



OUTPUT HIGH



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
*Input Voltage (dc)	–0.5V to +5.5V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
93L22XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L22XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH voltage for all inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed input LOW voltage for all inputs
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3V
I_{IH}	Input HIGH Current		2.0	20	μA	V_{CC} = MAX., V_{IN} = 2.4V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{SC} (Note 5)	Output Short Circuit Current	−10	−21	−40	mA	V_{CC} = MAX., V_{OUT} = 0.0V
I_{CC}	Power Supply Current		9.0	13.2	mA	V_{CC} = MAX.

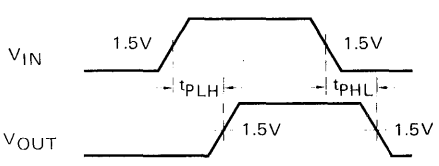
NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{PLH} (S_0 to Z)	Turn Off Delay Input to Output		26	36	ns	V_{CC} = 5.0 V
t_{PHL} (S_0 to Z)	Turn On Delay Input to Output		36	49	ns	C_L = 15 pF

SWITCHING TIME WAVEFORMS

S_0 to Z

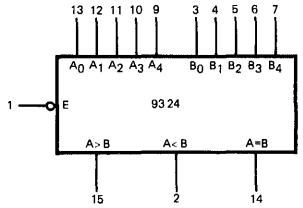


TTL/MSI 9324
5-BIT COMPARATOR

DESCRIPTION — The TTL/MSI 9324 is a High Speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than" and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

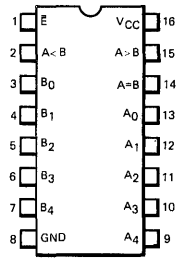
- **THREE SEPARATE OUTPUTS . . . A < B, A > B, A = B**
- **EASILY EXPANDABLE**
- **ACTIVE LOW LEVEL ENABLE INPUT**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED**
- **TERMINATION EFFECTS**
- **COMPATIBLE WITH FAIRCHILD DTL, LPDTL, TTL, AND MSI FAMILIES**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)

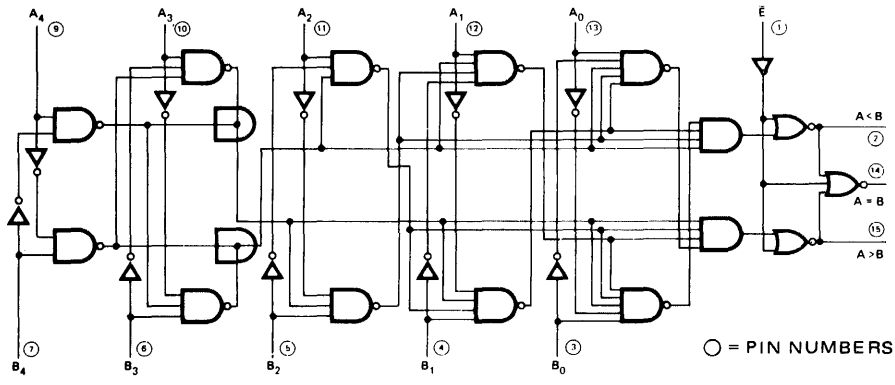


PIN NAMES

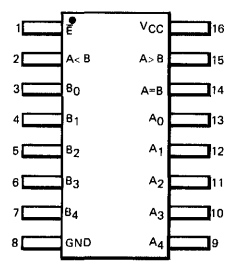
		LOADING (Note a)
$\bar{E}$	Enable (Active LOW) Input	2 U.L.
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs	2 U.L.
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs	2 U.L.
A < B	A Less Than B Output (Note b)	10 U.L.
A > B	A Greater Than B Output (Note b)	10 U.L.
A = B	A Equal to B Output (Note b)	10 U.L.

Notes:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor

LOGIC DIAGRAM



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 9324 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW Enable input ($\bar{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\bar{E}$.

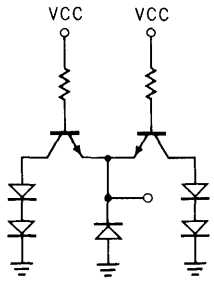
TRUTH TABLE

$\bar{E}$	Ay	By	A < B	A > B	A = B
H	X	X	L	L	L
L	Word A =	Word B	L	L	H
L	Word A >	Word B	L	H	L
L	Word B >	Word A	H	L	L

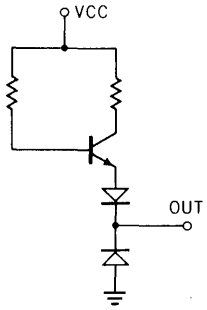
H = HIGH Voltage Level
L = LOW Voltage Level
X = Either HIGH or LOW Voltage Level

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

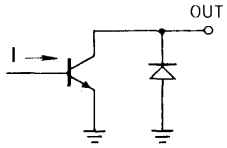
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

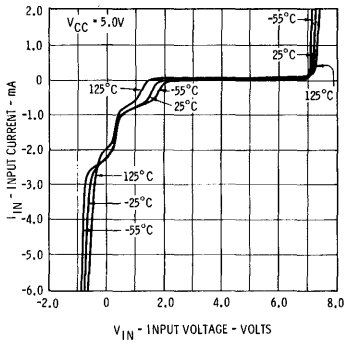


Fig. 1.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

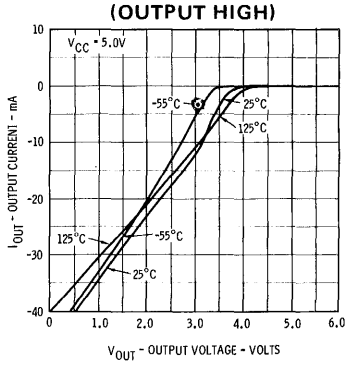


Fig. 2.

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

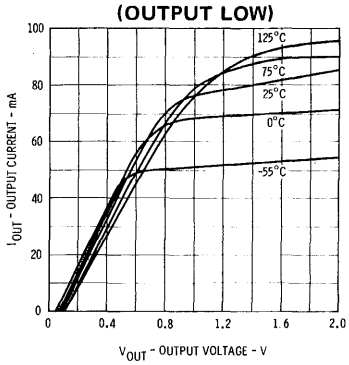


Fig. 3.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9324XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9324XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		−1.92	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−50	−70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		40	81	mA	V_{CC} = MAX.

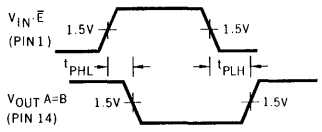
NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	9324XM			9324XC			UNITS	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output (A_2 to A = B)		40	45		40	48	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay Input to Output (A_2 to A = B)		35	42		35	45	ns	

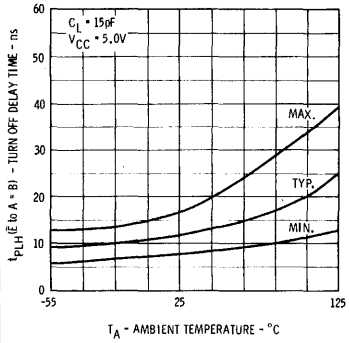
SWITCHING CHARACTERISTICS

t_{PLH}/t_{PHL} – $\bar{E}$ to A = B



Other Conditions:
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE ($\bar{E}$ TO A = B)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE ($\bar{E}$ TO A = B)

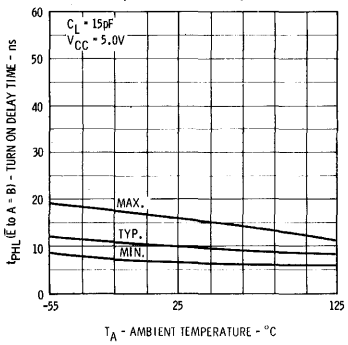
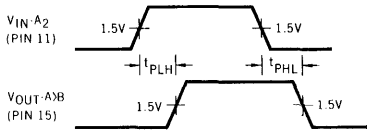


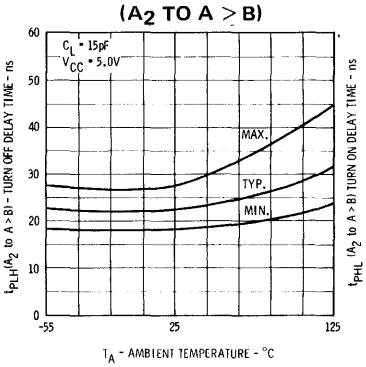
Fig. 4.

t_{PLH}/t_{PHL} – A_2 to A > B



Other Conditions: Pin 1, 5 = GND
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A > B)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A > B)

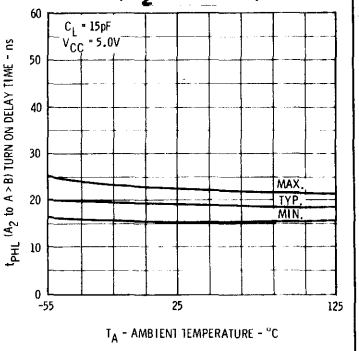
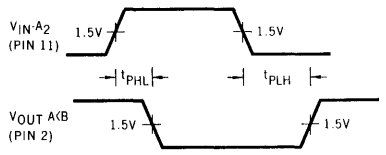


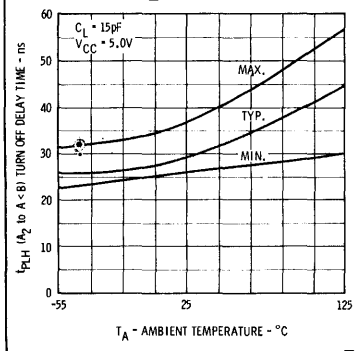
Fig. 5.

t_{PLH}/t_{PHL} – A_2 to A < B



Other Conditions: Pin 1 = GND
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A < B)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A < B)

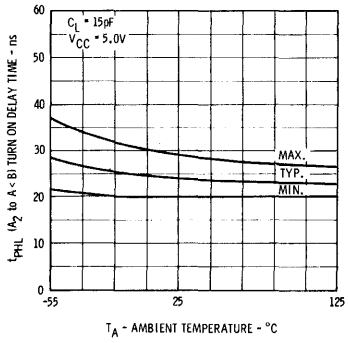
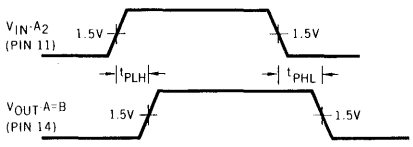


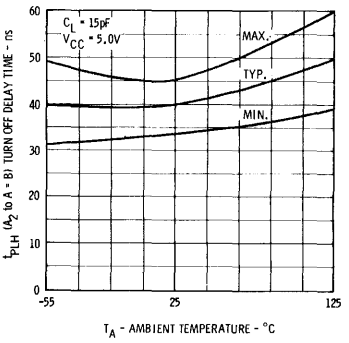
Fig. 6

t_{PLH}/t_{PHL} – A_2 to A = B



Other Conditions: Pin 1 = GND
All Other Inputs HIGH

TURN OFF DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A = B)



TURN ON DELAY TIME VERSUS AMBIENT TEMPERATURE (A_2 TO A = B)

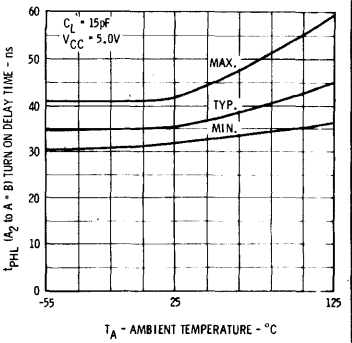


Fig. 7.

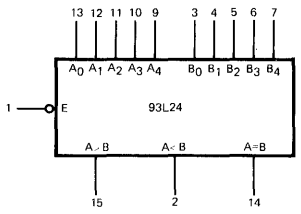
8

LPTTL/MSI 93L24
LOW POWER 5-BIT COMPARATOR

DESCRIPTION — The LPTTL/MSI 93L24 is a Medium Speed Expandable Comparator which provides comparison between two 5-bit words and gives three outputs, "less than", "greater than", and "equal to". A HIGH level on the active LOW enable input forces all three outputs LOW.

- **THREE SEPARATE OUTPUTS . . . A < B, A > B, A = B**
- **EASILY EXPANDABLE**
- **ACTIVE LOW-LEVEL ENABLE INPUT**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **TYPICAL PROPAGATION DELAY OF 55 ns (A > B)**
- **TYPICAL POWER DISSIPATION OF 52 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

LOGIC SYMBOL

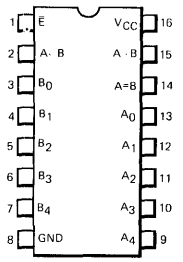


V_{CC} = Pin 16
GND = Pin 8

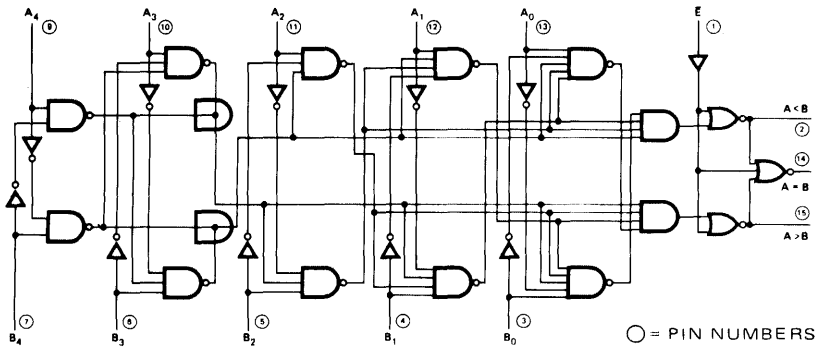
PIN NAMES		LOADING HIGH	LOADING LOW
$\overline{E}$	Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs	1.0 U.L.	0.5 U.L.
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs	1.0 U.L.	0.5 U.L.
A < B	A Less than B Output	9 U.L.	2.25 U.L.
A > B	A Greater than B Output	9 U.L.	2.25 U.L.
A = B	A Equal to B Output	10 U.L.	2.5 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

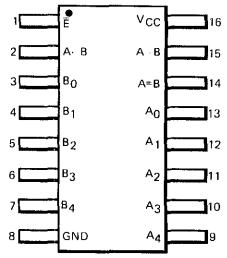
CONNECTION DIAGRAMS
DIP (TOP VIEW)



LOGIC DIAGRAM



FLATPAK(TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93L24 5-bit comparator uses combinational circuitry to directly generate "A greater than B" and "A less than B" outputs. As evident from the logic diagram, these outputs are generated in only three gate delays. The "A equals B" output is generated in one additional gate delay by decoding the "A neither less than nor greater than B" condition with a NOR gate. All three outputs are activated by the active LOW enable input ($\bar{E}$).

Tying the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion as shown in Figure 1.

The A_4 and B_4 inputs are the most significant inputs and A_0, B_0 the least significant. Thus if A_4 is HIGH and B_4 is LOW, the A > B output will be HIGH regardless of all other inputs except $\bar{E}$.

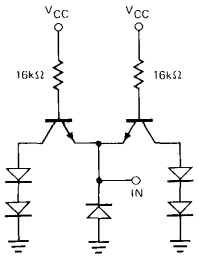
TRUTH TABLE

$\bar{E}$	A B	A < B	A > B	A = B
H	X X	L	L	L
L	Word A = Word B	L	L	H
L	Word A > Word B	L	H	L
L	Word A < Word B	H	L	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Either HIGH or LOW Voltage Level

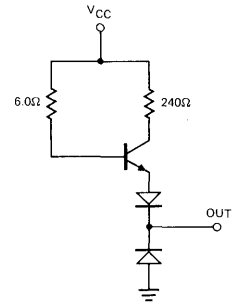
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT

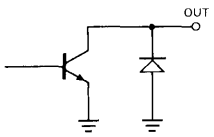


OUTPUTS EQUIVALENT CIRCUITS

OUTPUT HIGH



OUTPUT LOW



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L24XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93L24XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

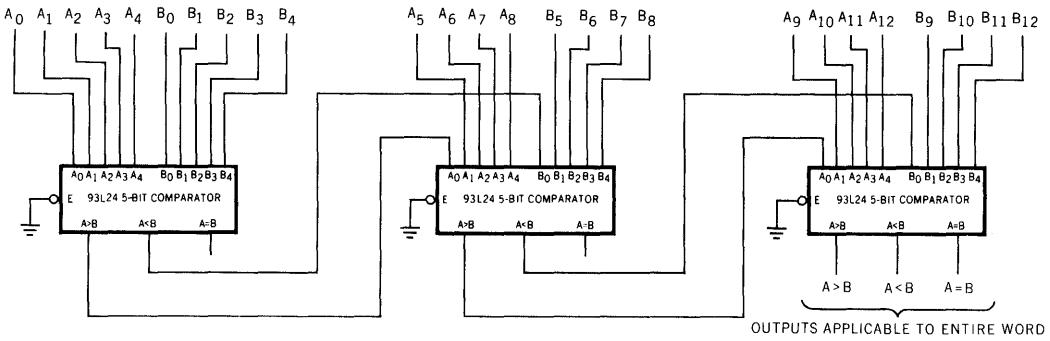
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC}=MIN., I_{OH}= -0.4mA(Pin 14), I_{OH}= -0.36mA(Pin 2&15), V_{IN}=V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.0 mA (Pin 14) I_{OL} = 3.6 mA (Pins 2 & 15) V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
I_{IL}	Input LOW Current		−0.5	−0.8	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{IH}	Input HIGH Current		4.0	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−10	−22	−40	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		10.4	21	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH}	Enable to Output		21	32	ns	
t_{PHL}	($\overline{E}$ to A = B)		22	35	ns	
t_{PLH}	Data to Output		35	54	ns	
t_{PHL}	(A_2 to A > B)		50	75	ns	C_L = 15 pF
t_{PLH}	Data to Output		46	70	ns	V_{CC} = 5.0 V
t_{PHL}	(A_2 to A < B)		51	77	ns	
t_{PLH}	Data to Output		65	100	ns	
t_{PHL}	(A_2 to A = B)		68	102	ns	

SERIAL EXPANSION OF 93L24 FOR LONGER WORD LENGTHS



For each additional 93L24 added four extra bits can be accommodated.

Fig. 1.

TTL/MSI 9328
DUAL 8-BIT SHIFT REGISTER

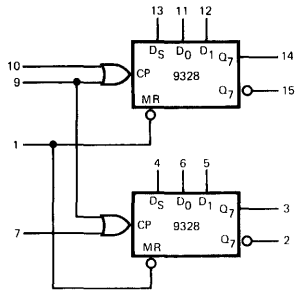
DESCRIPTION — The 9328 is a high speed serial storage element providing 16 bits of storage in the form of two 8-bit registers that will shift at greater than 20 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is provided at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each 8-bit register, and both registers may be master cleared from a common input.

- **20 MHz SHIFT FREQUENCY**
- **TWO INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**
- **TYPICAL POWER DISSIPATION OF 300 mW**
- **TTL COMPATIBLE**
- **INPUT DIODE CLAMPING**

PIN NAMES		LOADING (Note a)
D_S	Data Select Input	2 U.L.
D_0, D_1	Data Inputs	1 U.L.
CP	Clock (Active HIGH) Going Edge Input	
	Common (Pin 9)	3 U.L.
	Separate (Pins 7 and 10)	1.5 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	1 U.L.
Q_7	Last Stage Output (Note b)	10 U.L.
$\overline{Q_7}$	Complementary Output (Note b)	10 U.L.

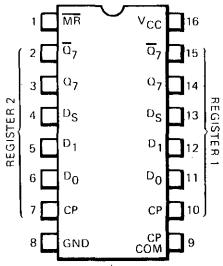
NOTES
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor

LOGIC SYMBOL

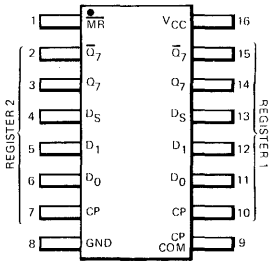


V_{CC} = Pin 16
Gnd = Pin 8

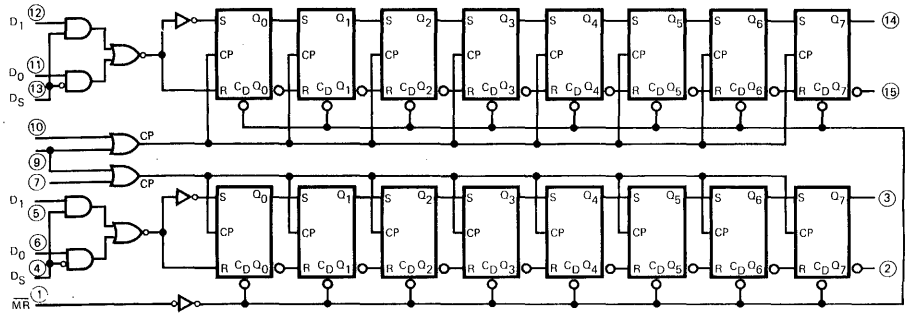
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 and 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW to HIGH transition of either, or both simultaneously, of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master; then the now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH to LOW transition of the last remaining HIGH clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a two input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input (D_S) following the Boolean expression:

Serial data in: $S_D = \overline{D}_S D_0 + D_S D_1$

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all sixteen stages independently of any other input signal.

TRUTH TABLE

SHIFT SELECTION

D_S	D_0	D_1	Q_7 (t_{n+8})
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

n+8 = Indicates state after eight clock pulse
L = LOW voltage level
H = HIGH voltage level
X = Either HIGH or LOW voltage level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9328XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9328XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current $\overline{MR}$, D_0, D_1 CP (Pins 7 & 10) D_S CP (Pin 9)		 10 15 20 30	 40 60 80 120	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current all inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current $\overline{MR}$, D_0, D_1 CP (Pins 7 & 10) D_S CP (Pin 9)		 −0.96 −1.44 −1.92 −2.88	 −1.6 −2.4 −3.2 −4.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−20	−50	−70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		60	77	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
t_{PLH}	Turn Off Delay Clock to Output		13	20	ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay Clock to Output		22	35	ns		
t_{PHL}	Turn On Delay Master Reset to Q Output		35	50	ns	Fig. 2	
f_{sr}	Shift Right Frequency	20	30		MHz	Fig. 1	

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
t_{pw} (CP)	Clock Pulse Width	25	17		ns	Fig. 1	V_{CC} = 5.0 V
t_{pw} ($\overline{MR}$) (CPH)	Master Reset Pulse Width with Clock HIGH	30	20		ns	Fig. 2	
t_{pw} ($\overline{MR}$) (CPL)	Master Reset Pulse Width with Clock LOW	40	24		ns		
t_s (Data)	Set-up Time Data to Clock	20	10		ns	Fig. 3	
t_h (Data)	Hold Time Data to Clock	0			ns		
t_{rec} ($\overline{MR}$)	Recovery Time Master Reset to Clock	33	19		ns	Fig. 2	

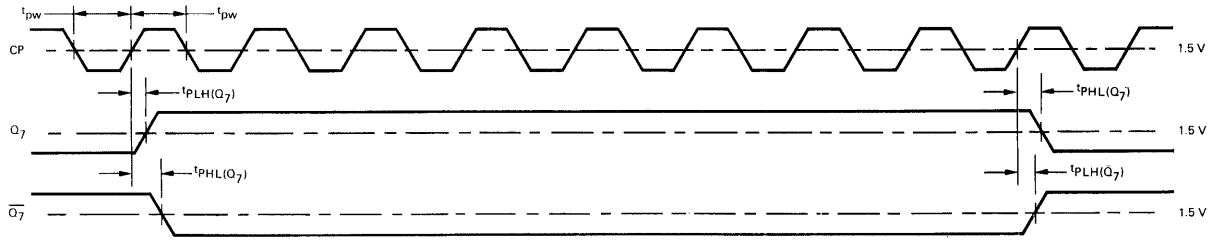
SET-UP TIME (t_s) is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative Hold Time indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

SWITCHING WAVEFORMS

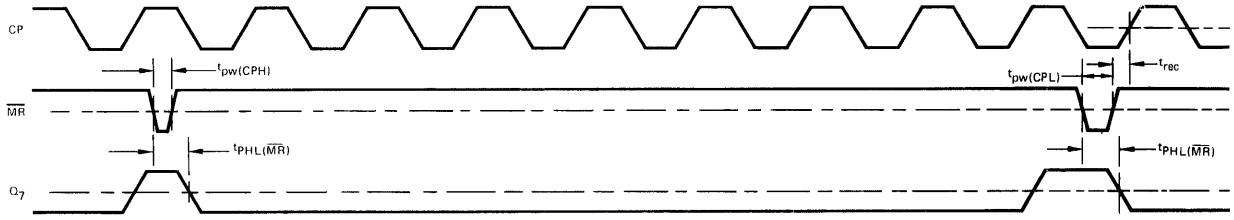
CLOCK TO OUTPUT DELAYS AND MINIMUM CLOCK PULSE WIDTH



OTHER CONDITIONS: $\overline{Q}_7$ is connected to D_1. Other clock is LOW.

Fig. 1

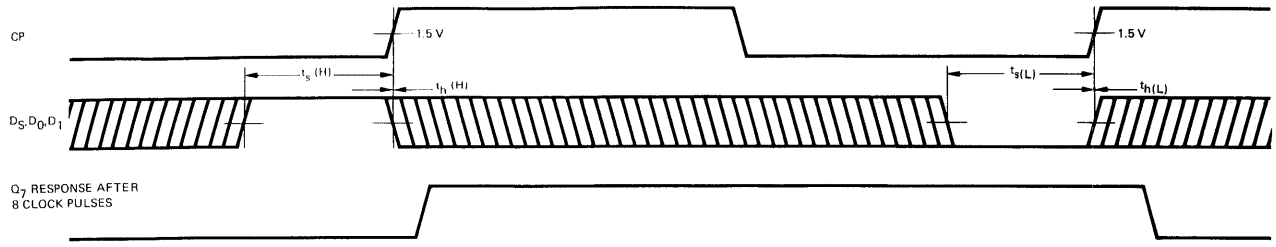
MASTER RESET TO OUTPUT TURN ON DELAY AND MINIMUM MASTER RESET PULSE WIDTHS



OTHER CONDITIONS: D_S, D_1, D_0 are HIGH. Other clock input is LOW.

Fig. 2

SET-UP TIME (t_s) AND HOLD TIME (t_h) FOR DATA INPUTS



NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

OTHER CONDITIONS: $\overline{MR}$ = HIGH, other clock input is LOW.

Fig. 3

LPTTL/MSI 93L28

LOW POWER DUAL 8-BIT SHIFT REGISTER

DESCRIPTION — The LPTTL/MSI 93L28 is a medium speed Serial Storage Element providing sixteen bits of storage in the form of two 8-bit registers that will shift at greater than 5 MHz rates. The multi-functional capability of this device is provided by several features: 1) Additional gating is at the input to both shift registers so that the input is easily multiplexed between two sources. 2) The clock of each register may be provided separately or together. 3) Both the true and complementary outputs are provided from each 8-bit register, and both registers may be master reset from a common input.

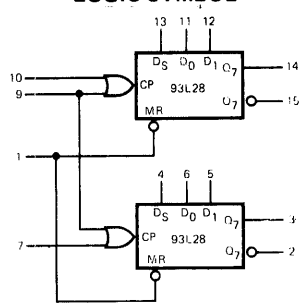
- **10 MHz TYPICAL SHIFT FREQUENCY**
- **TWO-INPUT MULTIPLEXER PROVIDED AT DATA INPUT OF EACH REGISTER**
- **GATED CLOCK INPUT CIRCUITRY**
- **BOTH TRUE AND COMPLEMENTARY OUTPUTS PROVIDED FROM LAST BIT OF EACH REGISTER**
- **ASYNCHRONOUS MASTER RESET COMMON TO BOTH REGISTERS**
- **TYPICAL POWER DISSIPATION OF 80 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **TTL COMPATIBLE**

PIN NAMES

		LOADING	
		HIGH	LOW
D_S	Data Select Input	1.0 U.L.	0.5 U.L.
D_0, D_1	Data Inputs	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input		
	Common	1.5 U.L.	0.75 U.L.
	Separate	0.75 U.L.	0.375 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
Q_7	Last Stage Output	8.0 U.L.	2.0 U.L.
$\overline{Q_7}$	Complementary Output	8.0 U.L.	2.0 U.L.

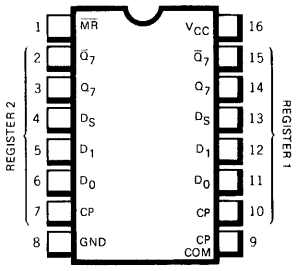
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL

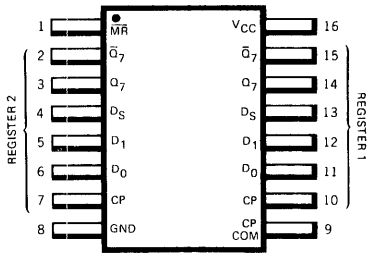


V_{CC} = PIN 16
GND = PIN 8

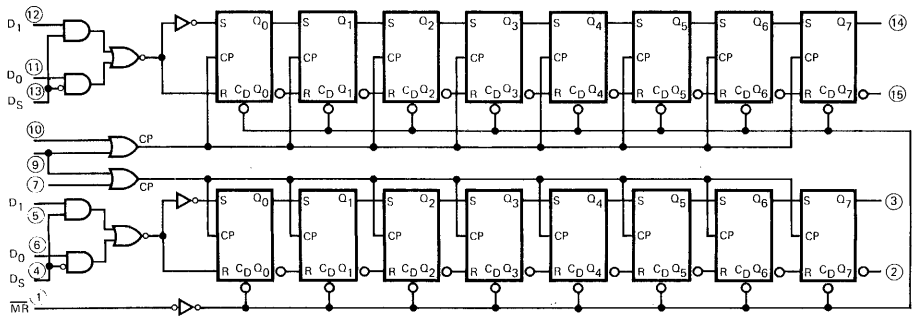
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



○ = PIN NUMBERS

8

FUNCTIONAL DESCRIPTION – The two 8-bit shift registers have a common clock input (pin 9) and separate clock inputs (pins 10 & 7). The clocking of each register is controlled by the OR function of the separate and the common clock input. Each register is composed of eight clocked RS master/slave flip-flops and a number of gates. The clock OR gate drives the eight clock inputs of the flip-flops in parallel. When the two clock inputs (the separate and the common) to the OR gate are LOW, the slave latches are steady, but data can enter the master latches via the R and S input. During the first LOW to HIGH transition of either or both of the two clock inputs, the data inputs (R and S) are inhibited so that a later change in input data will not affect the master. The now trapped information in the master is transferred to the slave. When the transfer is complete, both the master and the slave are steady as long as either or both clock inputs remain HIGH. During the HIGH to LOW transition of the last remaining high clock input, the transfer path from master to slave is inhibited first, leaving the slave steady in its present state. The data inputs (R and S) are enabled so that new data can enter the master. Either of the clock inputs can be used as clock inhibit inputs by applying a logic HIGH signal. Each 8-bit shift register has a two-input multiplexer in front of the serial data input. The two data inputs D_0 and D_1 are controlled by the data select input D_S following the Boolean expression:

Serial data in: $S_D = \overline{D}_S D_0 + D_S D_1$.

An asynchronous master reset is provided which, when activated by a LOW logic level, will clear all sixteen stages independently of any other input signal.

TRUTH TABLE

SHIFT SELECTION

D_S	D_0	D_1	$Q_7(t_{n+8})$
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

n+8 = indicates state after eight clock pulse
L = LOW voltage level
H = HIGH voltage level
X = Either HIGH or LOW voltage level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93L28XM	4.5V	5.0V	5.5V	-55°C to 125°C
93L28XC	4.75V	5.0V	5.25V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −0.32 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.15	0.3	Volts	V_{CC} = MIN., I_{OL} = 3.2 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage For All Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Voltage For All Inputs
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.3 V
	$\overline{MR}$, D_0 & D_1		−0.25	−0.4		
	CP (Pins 7 & 10)		−0.38	−0.6		
	D_S		−0.50	−0.8		
	CP (Pin 9)		−0.75	−1.2		
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	$\overline{MR}$, D_0 & D_1		2.0	20		
	CP (Pins 7 & 10)		3.0	30		
	D_S		4.0	40		
	CP (Pin 9)		6.0	60		
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC} (Note 5)	Output Short Circuit Current	−2.5	−16	−25	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		16	25.3	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

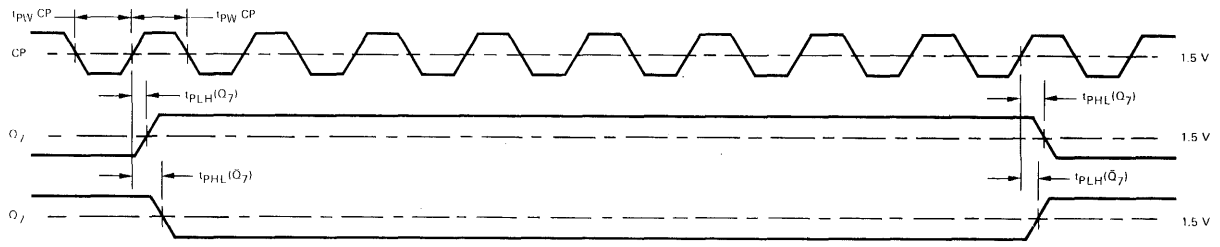
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PLH} (Q_7 & $\overline{Q}_7$)	Turn-Off Delay (clock to output)		30	45	ns	V_{CC} = 5.0V, C_L = 15pF Fig. 1
t_{PHL} (Q_7 & $\overline{Q}_7$)	Turn-On Delay (clock to output)		55	80	ns	
t_{PHL} ($\overline{MR}$)	Turn-On Delay (Master reset to output)		72	110	ns	V_{CC} = 5.0V, C_L = 15pF,

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PW} CP	Min. Clock Pulse Width	55	30		ns	V_{CC} = 5.0V, C_L = 15pF Fig. 1
t_{PW} $\overline{MR}$ (CPH)	Min. Master Reset Pulse Width with Clock HIGH	60	28		ns	V_{CC} = 5.0V, C_L = 15pF
t_{PW} $\overline{MR}$ (CPL)	Min. Master Reset Pulse Width with Clock LOW	70	38		ns	V_{CC} = 5.0V, C_L = 15pF

SWITCHING WAVEFORMS



NOTE: $\overline{Q}_7$ is connected to D_1. Other clock is grounded.

Fig. 1

TTL/MSI 9334
8-BIT ADDRESSABLE LATCH

DESCRIPTION — The TTL/MSI 9334 is a high speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level HIGH outputs. The device also incorporates an active level LOW common clear for resetting all latches, as well as, an active level LOW enable. The 9334 is compatible with all members of Fairchild's TTL family.

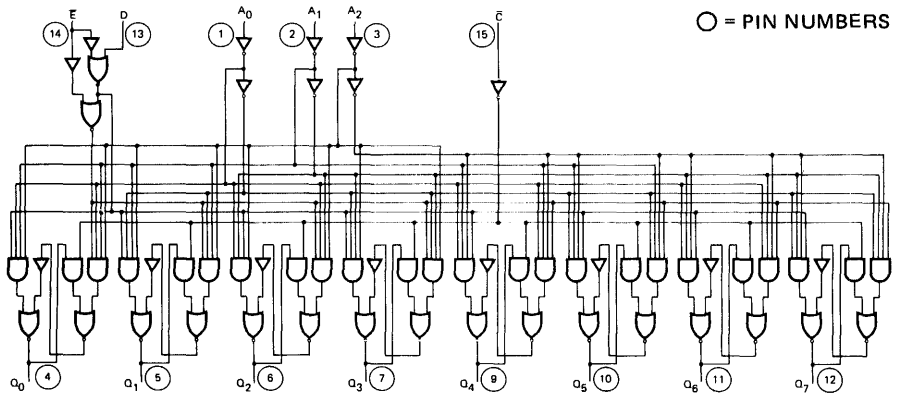
- **SERIAL TO PARALLEL CAPABILITY**
- **8-BITS OF STORAGE WITH OUTPUT OF EACH BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **ACTIVE HIGH DEMULTIPLEXING OR DECODING CAPABILITY**
- **EASILY EXPANDABLE**
- **COMMON CLEAR**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**

PIN NAMES

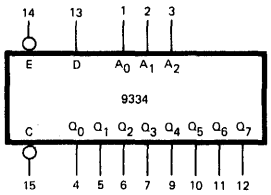
		LOADING (Note a)
A_0, A_1, A_2	Address Inputs	1 U.L.
D	Data Input	1 U.L.
$\overline{E}$	Enable (Active LOW) Input	1.5 U.L.
$\overline{C}$	Clear (Active LOW) Input	1 U.L.
Q_0 to Q_7	Parallel Latch Outputs (Note b)	6 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. 6 U.L. is the output LOW drive factor and 18 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

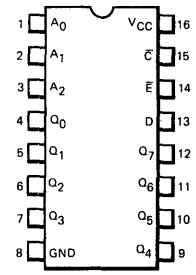


LOGIC SYMBOL

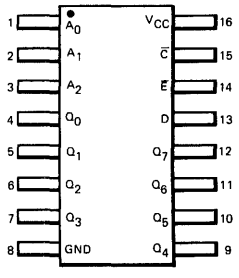


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION — The TTL/MSI 9334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the 9334 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The truth table below summarizes the operations of the 9334.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

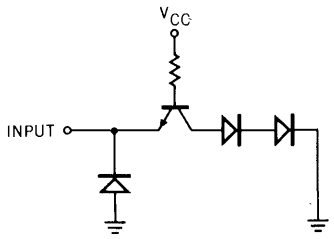
TRUTH TABLE

						PRESENT OUTPUT STATES								
$\overline{C}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	X	L	L	L	L	L	L	L	L	CLEAR
L	L	L	L	L	L	L	L	L	L	L	L	L	L	DEMULTIPLEX
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1} →								MEMORY
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					ADDRESSABLE
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						LATCH
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

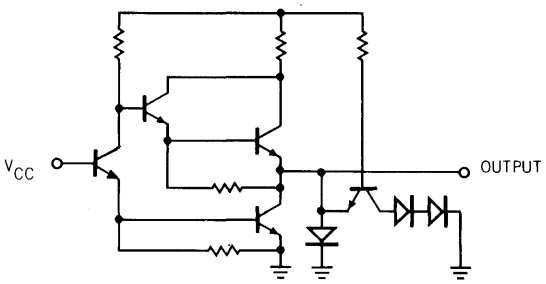
X = Don't Care Condition
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{n-1} = Previous Output State

TYPICAL INPUT AND OUTPUT CIRCUITS

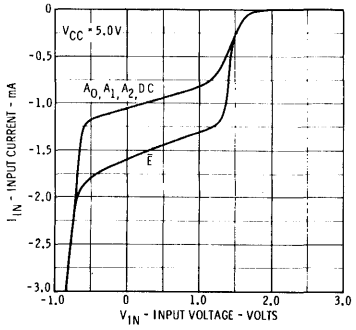
INPUTS EQUIVALENT CIRCUIT



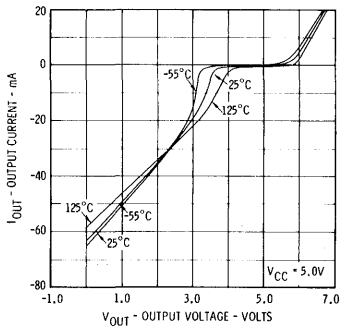
OUTPUTS EQUIVALENT CIRCUIT



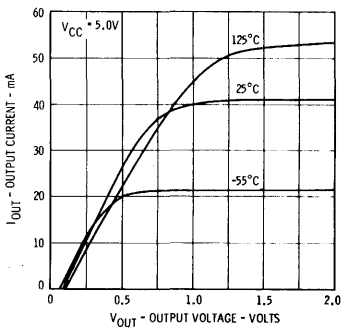
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to + 150°C
Temperature (Ambient) Under Bias	-55°C to + 125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to + 7.0 V
*Input Voltage (dc)	-0.5 V to + 5.5 V
*Input Current (dc)	-30 mA to + 5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to + V_{CC} value
Output Current (dc) (Output LOW)	+ 30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9334XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9334XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −720 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 9.6 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Level	2.0			Volts	Guaranteed Input Logical HIGH Voltage for all Inputs
V_{IL}	Input LOW Level			0.8	Volts	Guaranteed Input Logical LOW Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
I_{IL}	Input LOW Current A_0, A_1, A_2, D, $\overline{C}$ $\overline{E}$		 −0.96 −1.44	 −1.6 −2.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current A_0, A_1, A_2, D, $\overline{C}$ $\overline{E}$		 10 15	 40 60	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		56	86	mA	V_{CC} = MAX.

NOTES:

(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.

(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.

(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.

(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

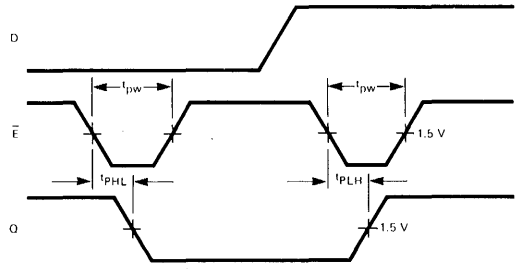
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH}	Turn-Off Delay Enable to Output		19	23	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay Enable to Output		16	24	ns	Fig. 1
t_{PLH}	Turn-Off Delay Data to Output		28	35	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay Data to Output		16	24	ns	Fig. 2
t_{PLH}	Turn-Off Delay Address to Output			35	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay Address to Output			35	ns	Fig. 3
t_{PHL}	Turn-On Delay Clear to Output		21	25	ns	V_{CC} = 5.0 V, C_L = 15 pF Fig. 5

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_s (H)	Set-up Time HIGH Data to Enable	20	13		ns	
t_h (H)	Hold Time HIGH Data to Enable	0	-10		ns	V_{CC} = 5.0 V
t_s (L)	Set-up Time LOW Data to Enable	17	10		ns	Fig. 4
t_h (L)	Hold Time LOW Data to Enable	0	-13		ns	
t_s (A-$\overline{E}$)	Set-up Time Address to Enable (See Note 6)	5	0		ns	V_{CC} = 5.0 V Fig. 6
t_{pw} ($\overline{E}$)	Enable Pulse Width	17	11		ns	V_{CC} = 5.0 V Fig. 1

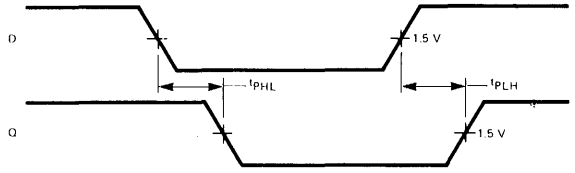
NOTES:
(6) The Address to Enable Set-up Time is the time before the HIGH to LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
(7) The shaded areas indicate when the inputs are permitted to change for predictable output performance.

Fig. 1 TURN-ON & TURN-OFF DELAYS ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



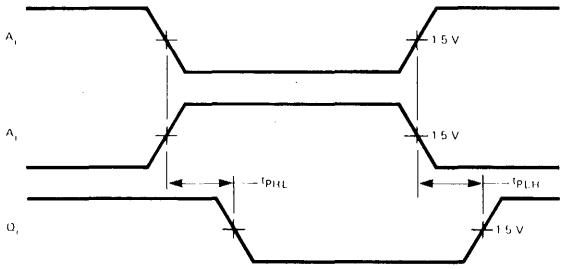
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 2 TURN-ON & TURN-OFF DELAYS DATA TO OUTPUT



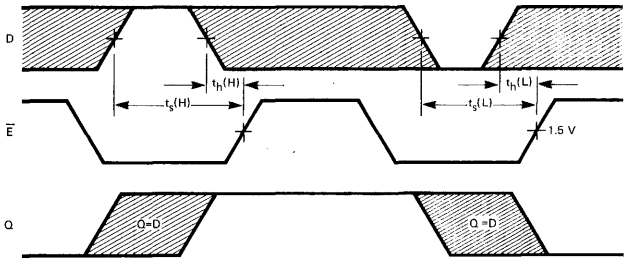
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = H, A = STABLE

Fig. 3 TURN-ON & TURN-OFF DELAYS ADDRESS TO OUTPUT



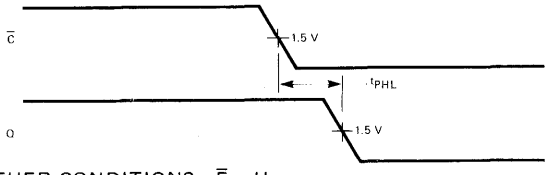
OTHER CONDITIONS: $\overline{E}$ = L, $\overline{C}$ = L, D = H

Fig. 4 SET-UP AND HOLD TIME DATA TO ENABLE



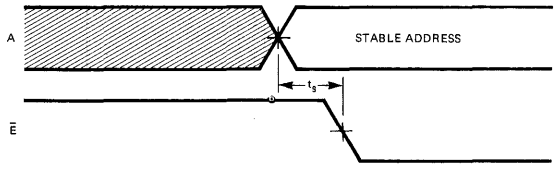
OTHER CONDITIONS: $\overline{C}$ = H, A = STABLE

Fig. 5 TURN-ON DELAY CLEAR TO OUTPUT



OTHER CONDITIONS: $\overline{E}$ = H

Fig. 6 SET-UP TIME ADDRESS TO ENABLE (SEE NOTES 6 & 7)



OTHER CONDITIONS: $\overline{C}$ = H

8

TTL/MSI 9338
8-BIT MULTIPLE PORT REGISTER

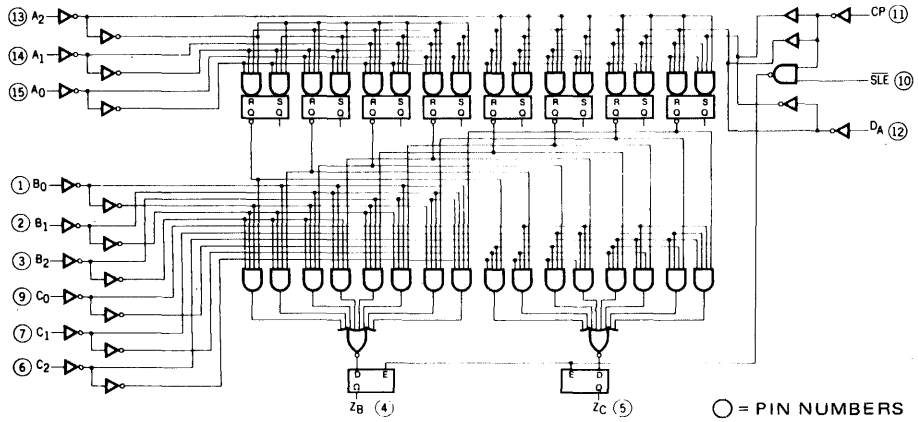
DESCRIPTION – The TTL/MSI 9338 is an 8-Bit Multiple Port Register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of the eight bits and read from any two of the eight bits simultaneously. The circuit uses TTL technology and is compatible with all members of Fairchild's TTL family.

- **MASTER/SLAVE OPERATION PERMITTING SIMULTANEOUS WRITE/READ WITHOUT RACE PROBLEMS**
- **SIMULTANEOUSLY READ TWO BITS AND WRITE ONE BIT IN ANY ONE OF EIGHT BIT POSITIONS**
- **READILY EXPANDABLE TO ALLOW FOR LARGER WORD SIZES**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **ALL CERAMIC "HERMETIC" 16 LEAD DUAL IN-LINE AND FLATPAKS**
- **TTL COMPATIBLE**

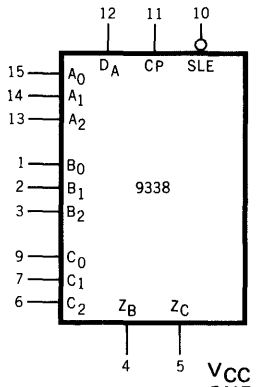
PIN NAMES		LOADING (Note a)
A_0, A_1, A_2	Write Address Inputs	2/3 U.L.
D_A	Data Input	2/3 U.L.
B_0, B_1, B_2	B Read Address Inputs	2/3 U.L.
Z_B	B Output (Note b)	10 U.L.
C_0, C_1, C_2	C Read Address Inputs	2/3 U.L.
Z_C	C Output (Note b)	10 U.L.
CP	Clock Pulse Input	2/3 U.L.
$\overline{SLE}$	Slave Enable (Active LOW) Input	2/3 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

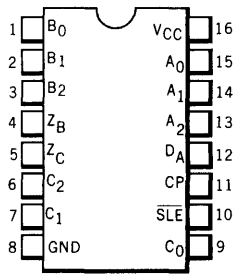
LOGIC DIAGRAM



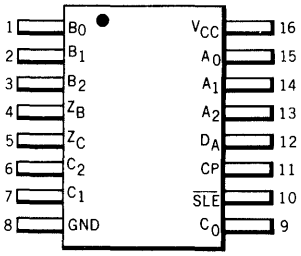
LOGIC SYMBOL



CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



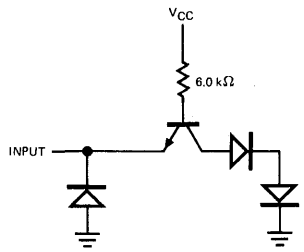
FUNCTIONAL DESCRIPTION – The 9338 8-bit multiple port register may be considered as a 1-bit slice of eight high speed working registers. Data may be written into any one of eight storage locations and read out from any two of the eight storage locations simultaneously. Master/slave operation eliminates all race problems associated with simultaneous writing in and reading from the same location.

The timing of this data transfer is similar to that of a standard master/slave flip-flop. While the clock is LOW the slaves are held steady, but the information on the D (data) input is permitted to enter the selected master. The next clock transition from LOW to HIGH locks the masters in their present states making them insensitive to the D input and write address inputs. This rising clock edge also connects each of the two slaves to the selected masters causing their contents to be reflected on the outputs. Outputs change, therefore, following the LOW to HIGH transition of the clock as on almost all Fairchild TTL/MSI devices and TTL flip-flops.

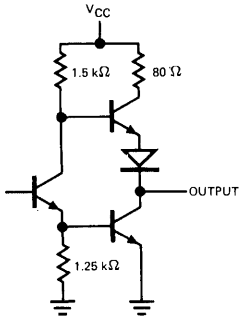
The Slave Enable ($\overline{SLE}$) input may be used to defeat the master/slave operation. If the Slave Enable ($\overline{SLE}$) line is held LOW, the slaves are continuously enabled allowing immediate transfer of information from the selected masters to the outputs.

TYPICAL INPUT AND OUTPUT CIRCUITS

INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE $D_A A_2 A_1 A_0 C_2 C_1 C_0 B_2 B_1 B_0$ CP

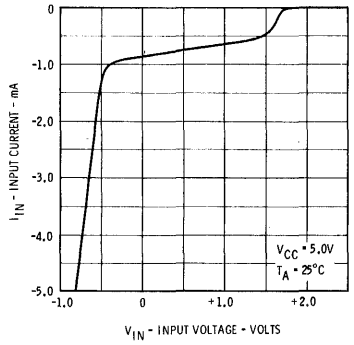


Fig. 1

INPUT CURRENT VERSUS INPUT VOLTAGE $\overline{SLE}$

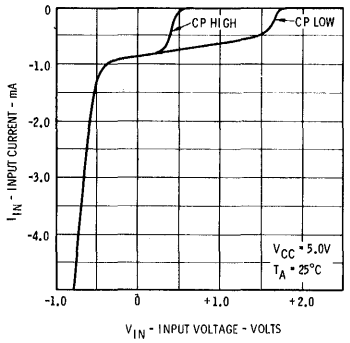


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE Z_B AND Z_C (LOW STATE)

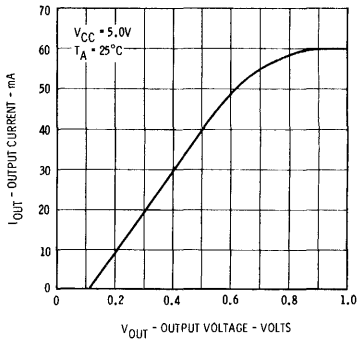


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC}
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9338XM	4.50 V	5.0 V	5.50 V	–55°C to +125°C
9338XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = -12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = -0.8mA V_{IN} = V_{IH}
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			27	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		-0.64	-1.1	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 5)	-10	-50	-70	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		85	135	mA	V_{CC} = MAX.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.

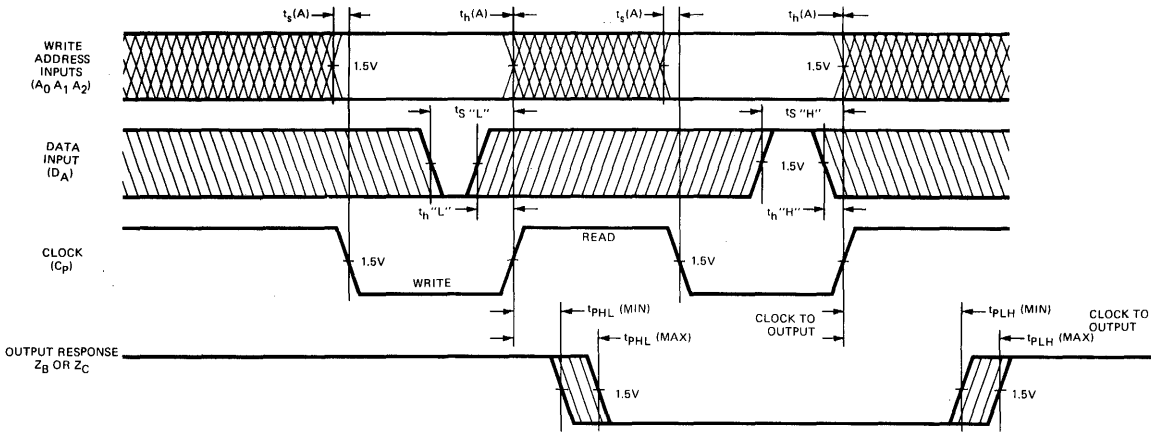
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_{PLH}	Turn-Off Delay Address to Output	13	25	40	ns	See Fig. 6	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn-On Delay Address to Output	18	27	35	ns		
t_{PLH}	Turn-Off Delay Data to Output	25	33	45	ns	See Fig. 5	
t_{PHL}	Turn-On Delay Data to Output	25	37	50	ns		
t_{PLH}	Turn-Off Delay Clock to Output	18	26	35	ns	See Fig. 4	
t_{PHL}	Turn-On Delay Clock to Output	13	21	30	ns		

SWITCHING SET-UP REQUIREMENTS (T_A = 25°C)

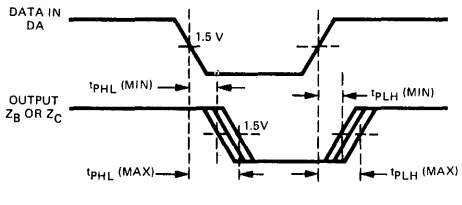
SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS	
		MIN.	TYP.	MAX.			
t_s"H"	Set-up Time HIGH Data to Clock	20	14		ns	See Fig. 4	V_{CC} = 5.0 V
t_h"H"	Hold Time HIGH Data to Clock	0	-7		ns		
t_s"L"	Set-up Time LOW Data to Clock	12	7		ns		
t_h"L"	Hold Time LOW Data to Clock	-8	-14		ns		
t_s(A)	Set-up Time (A) Address to Clock	10	5		ns		
t_h(A)	Hold Time (A) Address to Clock	0			ns		
t_{CP}"L"	Clock LOW Time Required to Write	13	7.0		ns	See Fig. 7	
t_{CP}"H"	Clock HIGH Time Required to Read	23	15		ns	See Fig. 8	

SWITCHING WAVEFORMS



The crosshatched areas of the input waveforms indicate when inputs are permitted to change. The crosshatched areas on the output response waveforms indicate minimum and maximum propagation delays.

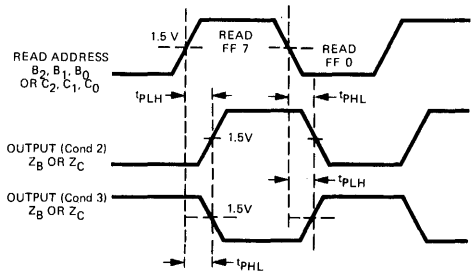
Fig. 4 DATA AND WRITE ADDRESS SETUP TIMES; READ TIME (CLOCK PULSE TO OUTPUT)



OTHER CONDITIONS

1. CP = LOW
2. $\overline{SLE}$ = LOW
3. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_2, C_1, C_0$

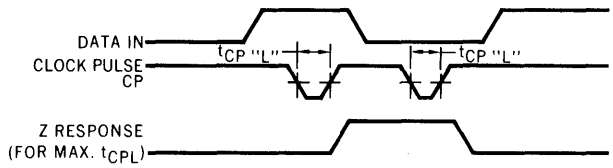
Fig. 5 t_{PLH}/t_{PHL} (DATA INPUT TO OUTPUT)



OTHER CONDITIONS

1. CP = HIGH
2. Master FF 7 = H
3. Master FF 0 = L
   Master FF 7 = L
   Master FF 0 = H

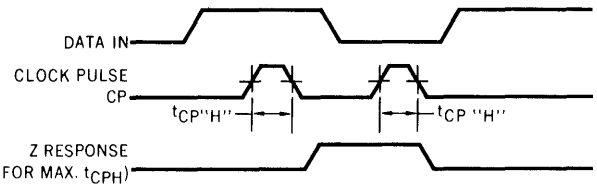
Fig. 6 t_{PLH}/t_{PHL} (READ ADDRESS TO OUTPUT)



OTHER CONDITIONS

1. $\overline{SLE}$ = LOW
2. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_2, C_1, C_0$

Fig. 7 t_{CP}"L" (CLOCK LOW TIME REQUIRED TO WRITE)



OTHER CONDITIONS

1. $\overline{SLE}$ = HIGH
2. $A_2, A_1, A_0 = B_2, B_1, B_0 = C_0, C_1, C_2$

Fig. 8 t_{CP}"H" (CLOCK HIGH TIME REQUIRED TO READ)

DEFINITION OF TERMS

DATA SET UP TIME (t_s) — Is defined as the time required for a HIGH (t_s "H") or a LOW (t_s "L") logic level to be present at the data input prior to the clock transition from LOW to HIGH, in order for the master to recognize and store the new data.

t_{CP} "L" (CLOCK LOW TIME REQUIRED TO WRITE) — This parameter is defined as the minimum LOW clock pulse width required to write information into the master.

t_{CP} "H" (CLOCK HIGH TIME REQUIRED TO READ) — This parameter is defined as the minimum HIGH clock pulse width required to store information in the slaves.

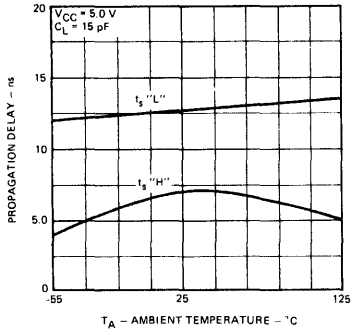
WRITE ADDRESS SET-UP TIME t_s(A) — Is the time required for the write address to be present before the HIGH to LOW clock transition so that the correct master is addressed and other masters are not disturbed. When writing data into the 9338, the write address inputs should be stable at t_s(A) before the HIGH to LOW transition of the clock and while the clock is LOW but they may change simultaneously with the LOW to HIGH clock transition.

HOLD TIME (t_h) is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to insure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

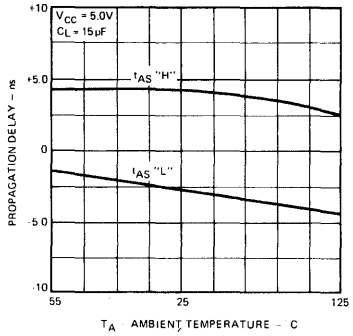
8

TYPICAL SWITCHING CHARACTERISTICS

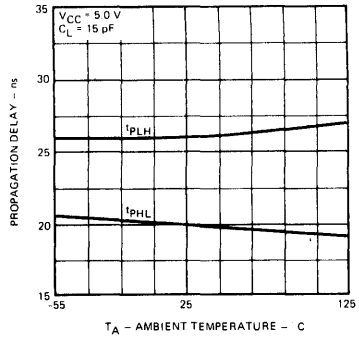
DATA SETUP TIME VERSUS AMBIENT TEMPERATURE



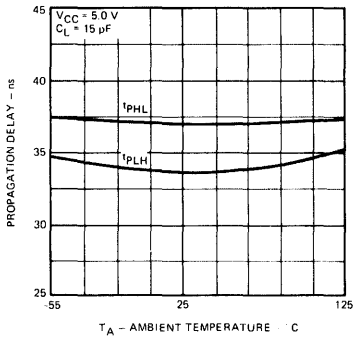
WRITE ADDRESS SETUP TIME VERSUS AMBIENT TEMPERATURE



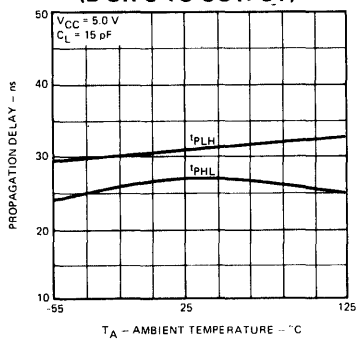
READ TIME VERSUS AMBIENT TEMPERATURE (CLOCK TO OUTPUT)



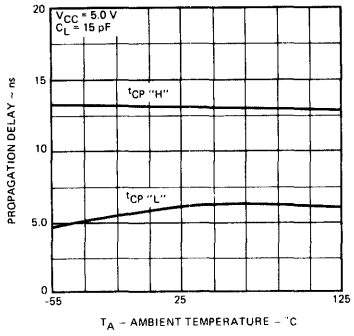
DELAY TIME VERSUS AMBIENT TEMPERATURE (D_A TO Z_B OR Z_C)



READ TIME VERSUS AMBIENT TEMPERATURE (B OR C TO OUTPUT)



CLOCK TIME REQUIRED TO READ OR WRITE VERSUS AMBIENT TEMPERATURE



APPLICATIONS

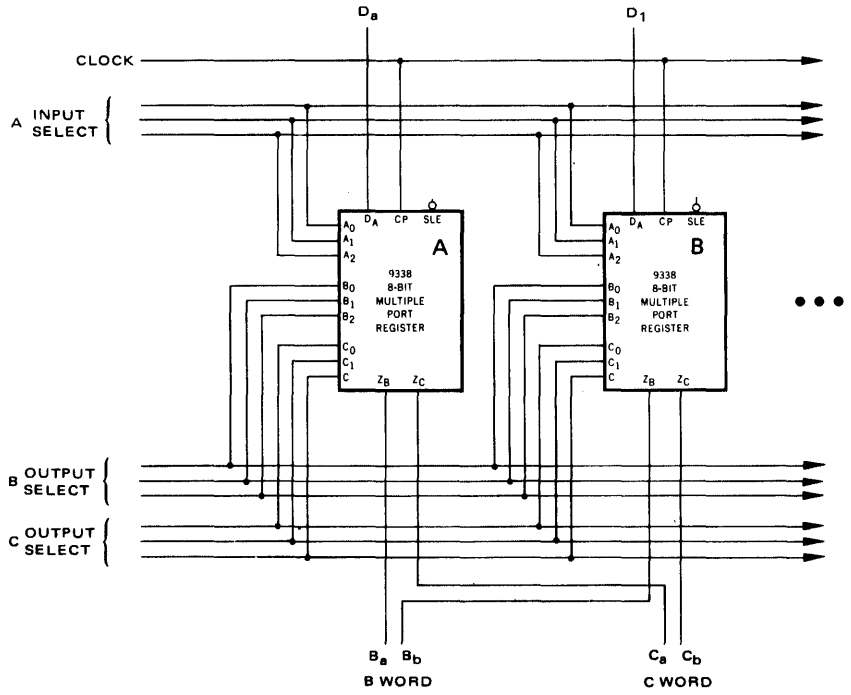


Fig. 9 PARALLEL EXPANSION

One 9338 is needed for each bit of the required word length. The read and write input lines should be connected in common on all of the devices. This register configuration provides two words of n-bits each at one time as is illustrated above, where n devices are connected in parallel.

TTL/MSI 93S39

8-BIT EDGE TRIGGERED MULTIPLE PORT REGISTER

TO BE ANNOUNCED

DESCRIPTION — The TTL/MSI 93S39 is an 8-bit, edge triggered, multiple port register designed with the super high speed Schottky-barrier diode clamp circuit. It is organized as a 1-bit slice of eight storage registers for use as accumulators, data registers, or scratch pad memory. It is primarily intended to be used with an arithmetic logic unit (ALU) such as the 93S41/74S181 to provide very high speed arithmetic operations.

The 93S39 is essentially an 8-bit register having one input data line and three output ports. Data can be written into any one of eight locations, selected by address lines A_0 thru A_2. Because of the master/slave design, the previous data can be read out of that same location simultaneously on output Z_A. In addition data can be read out from any other location on output Z_B, under control of the second output multiplexer, addressed by B_0 thru B_2. Individual multiplexer enable controls to the Z_A and Z_B outputs allow for easy expansion to more than eight registers. A separate Z_0 output is provided which continuously displays the contents of location 0, which can be used as a P register.

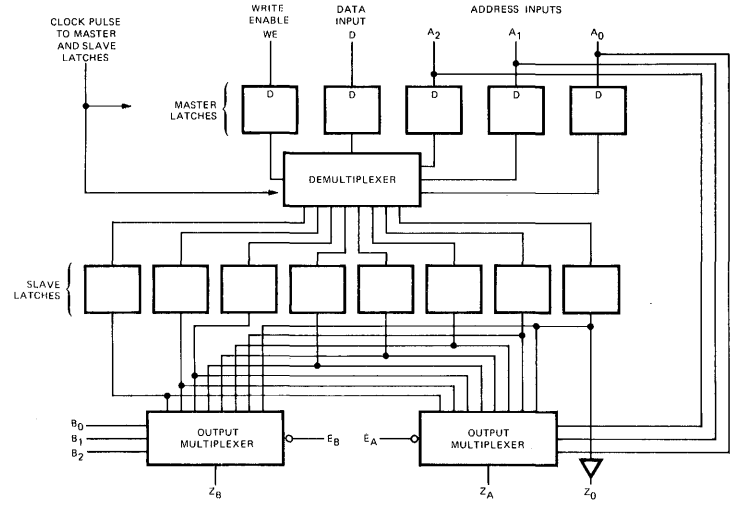
The 93S39 features edge triggered inputs on the write enable, data, and write address lines, which respond only to the LOW to HIGH transition of the clock. This insures the longest possible time for propagation of signals through external combinatorial logic, as the stability of the input address, the new data, and the write enable must be controlled only within the set-up time requirements of the rising edge of the clock. The outputs Z_A and Z_B are asynchronous, depending only on the delay of the multiplexer address and enable controls. The output enables are designed to permit OR-tying the outputs for easy expansion to more than eight registers.

- **THE WRITE CONTROLS (WRITE ENABLE, WRITE ADDRESS, AND DATA) ARE EDGE TRIGGERED—RESPONDING ONLY TO THE POSITIVE TRANSITION OF THE CLOCK PULSE**
- **SCHOTTKY-BARRIER DIODE DESIGN FOR SUPER HIGH SPEED OPERATION**
- **ASYCHRONOUS CONTROL OF OUTPUT DATA MULTIPLEXERS**
- **OUTPUT MULTIPLEXER DESIGN PROVIDES FOR EASY REGISTER EXPANSION**
- **CONTINUOUS OUTPUT FROM BIT LOCATION "000" FOR MEMORY ADDRESS REGISTER APPLICATIONS**

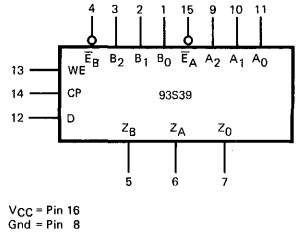
PIN NAMES

A_0, A_1, A_2	Write Address and "A" Multiplexer Address Inputs	WE	Write Enable Input
$\overline{E}_A$	"A" Multiplexer Enable (Active LOW) Input	CP	Clock Pulse (Active HIGH going edge) Input
B_0, B_1, B_2	"B" Multiplexer Address Inputs	Z_0	Output from Bit Location "000"
$\overline{E}_B$	"B" Multiplexer Enable (Active LOW) Input	Z_A	Output from "A" Multiplexer
D	Data Input	Z_B	Output from "B" Multiplexer

LOGIC DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
Gnd = Pin 8

TTL/MSI 9340

4-BIT ARITHMETIC LOGIC UNIT WITH CARRY LOOKAHEAD

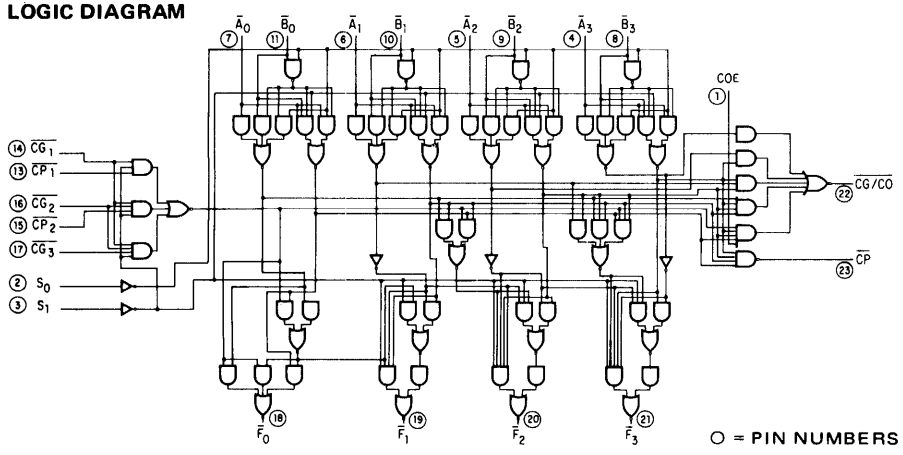
DESCRIPTION – The 9340 is a TTL/MSI high speed Arithmetic Logic Unit with full on chip carry lookahead circuitry. It can perform the arithmetic operations add or subtract in parallel, or either of six logic functions on two 4-bit binary words. The internal carry lookahead provides either a ripple carry output or carry lookahead outputs. An internal carry input network accepts carry lookahead outputs from up to three other packages producing a 16-bit full carry lookahead ALU without additional gates. Ripple carries can be used between additional blocks of 12 bits to further expand the word length. A low power version of the 9340 is available as the 93L40, dissipating only 110 mW.

- **MULTIFUNCTION CAPABILITY**
  Two Arithmetic Operations – Add, Subtract
  Six Logic Functions – A Ex or B, A and B, Plus Four Others
- **ADD TWO 4-BIT WORDS IN 23 ns TYPICAL**
- **SUBTRACT TWO 4-BIT WORDS IN 28 ns**
- **LOOKAHEAD CARRY INPUT AND OUTPUT NETWORKS ON CHIP**
- **EASILY EXPANDABLE TO LONGER WORD LENGTHS**
- **TYPICAL POWER DISSIPATION OF 425 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**

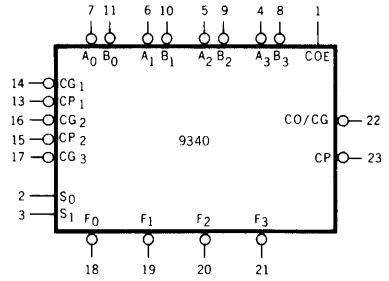
PIN NAMES		LOADING (Note a)
$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand Active LOW Inputs	3 U.L.
S_0, S_1	Mode Select Inputs	1 U.L.
$\overline{CG}_1$	Active LOW Carry Generate Input from immediately preceding stage	3 U.L.
$\overline{CP}_1$	Active LOW Carry Propagate Input from immediately preceding stage	1 U.L.
$\overline{CG}_2$	Active LOW Carry Generate Input from second preceding stage	2 U.L.
$\overline{CP}_2$	Active LOW Carry Propagate Input from second preceding stage	1 U.L.
$\overline{CG}_3$	Active LOW Carry Generate Input from third preceding stage	1 U.L.
$\overline{COE}$	Carry Out Enable Input	1.5 U.L.
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$	Function (Active LOW) Outputs (Note b)	10 U.L.
$\overline{CO/CG}$	Carry Out/Carry Generate (Active LOW) Output (Note b)	10 U.L.
$\overline{CP}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.

Notes: a. 1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

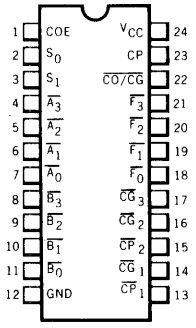


LOGIC SYMBOL

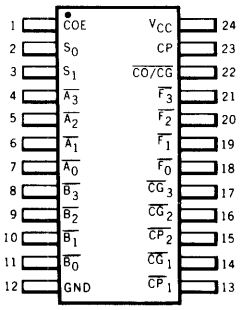


V_{CC} = Pin 24
Gnd = Pin 12

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 9340 accepts two 4-bit words, A_0, A_1, A_2, A_3 (A_{0-3}) and B_0, B_1, B_2, B_3 (B_{0-3}), and produces a 4-bit output, F_0, F_1, F_2, F_3 (F_{0-3}). The output function is determined by the states on the control lines S_0 and S_1. The inputs and outputs of the 9340 may be considered to be active level LOW or active level HIGH. Logic equivalents for four representations of the 9340 are shown in Figure 1a, b, c, and d.

The add and subtract operations are performed on the entire word, with carries or borrows propagated between bits of different weight. The arithmetic may be performed in 1's complement, 2's complement, or sign-magnitude notation. In the logic modes, carries are inhibited and the device acts like four gates of the type shown in Figure 1.

To achieve high speed operation, the 9340 is designed to be used in a carry lookahead system. Full carry lookahead is used inside the device to propagate carries between bits. Carry lookahead functions over the 4-bit block are available as outputs. These outputs are labeled $\overline{CO/CG}$ (Carry Out/Carry Generate) and $\overline{CP}$ (Carry Propagate) on the logic symbol. The carry in to the device is formed from a set of Carry Generate and Carry Propagate inputs (equation 1) so that three 9340's can be interconnected without any additional gates to form a 12-bit full carry lookahead ALU with a carry in. The pin labeled COE (Carry Out Enable) controls the $\overline{CO/CG}$ output according to equation 2. When COE is HIGH, $\overline{CO/CG}$ becomes a Carry Out which can be used to ripple carries between blocks of 12 bits. The $\overline{CG}_1$ input can be used for a ripple carry input, since this signal is sufficient to produce a carry in.

EQUATION:

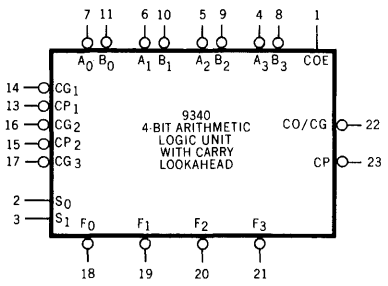
(1) $(\overline{CG_1}) + (\overline{CP_1})(\overline{CG_2}) + (\overline{CP_1})(\overline{CP_2})(\overline{CG_3}) = C_{in}$ (internal)

(2) $\overline{CO/CG} = (\overline{CG}) + (\overline{CP})(C_{in})(COE)$

Fig. 1–FUNCTION TABLES FOR LOGIC EQUIVALENTS OF THE 9340

Note that when the input operants are defined as active HIGH, the carry lookahead inputs and outputs are not formally carry generate and carry propagate. Consequently, these pins have been relabeled CX and CY in the active HIGH cases. However, the signals are connected in the same manner as $\overline{CG}$ and $\overline{CP}$.

ACTIVE LOW OPERANDS

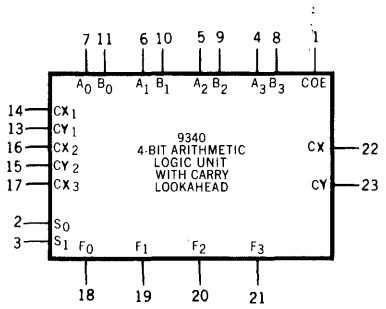


V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EX OR B	
H	H	A AND B	

Fig. 1a

ACTIVE HIGH OPERANDS

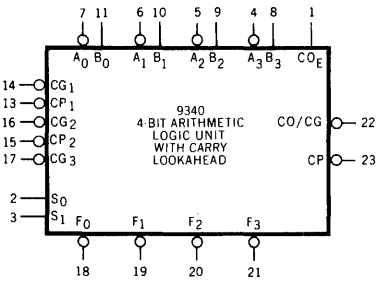


V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A SUBTRACT B	
H	L	A ADD B	
L	H	A EQUIV B	
H	H	A OR B	

Fig. 1b

ACTIVE LOW OPERANDS WITH INVERTED B

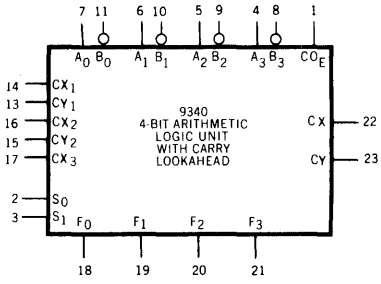


V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EQUIV B	
H	H	A AND $\overline{B}$	

Fig.1c

ACTIVE HIGH OPERANDS WITH INVERTED B



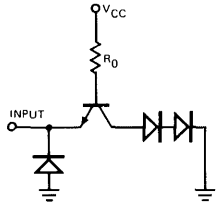
V_{CC} = Pin 24
Gnd = Pin 12

CONTROL INPUTS S_0	CONTROL INPUTS S_1	OPERATION	EQUIVALENT LOGIC
L	L	A ADD B	
H	L	A SUBTRACT B	
L	H	A EX OR B	
H	H	A OR $\overline{B}$	

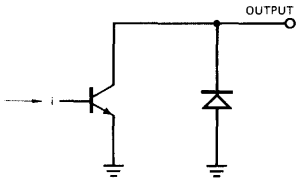
Fig.1d

TYPICAL INPUT AND OUTPUT CIRCUITS

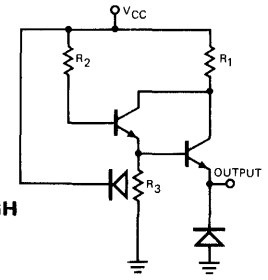
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUITS

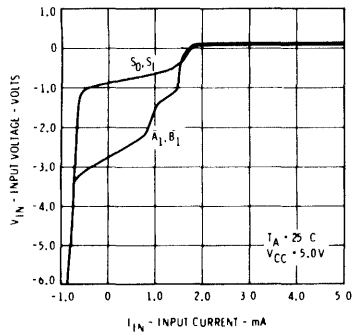


LOW

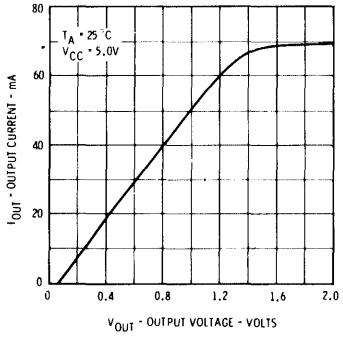


HIGH

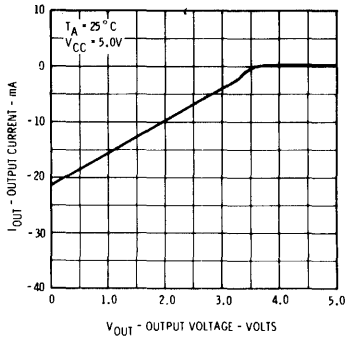
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC}) MIN.	TYP.	MAX.	TEMPERATURE
9340XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9340XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	TYP. (Note 4)	MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC}=MIN., I_{IN}=−12mA, T_A=25°C
V_{OH}	Output HIGH Voltage	2.4	3.6		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.4 V
	$S_0, S_1, \overline{CP}_1, \overline{CP}_2, \overline{CG}_3$		10	40		
	COE		15	60		
	$\overline{CG}_2$		20	80		
	$\overline{A}_0$ to $\overline{A}_3, \overline{B}_0$ to $\overline{B}_3, \overline{CG}_1$		30	120		
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.4 V
	$S_0, S_1, \overline{CP}_1, \overline{CP}_2, \overline{CG}_3$		−0.96	−1.6		
	COE		−1.44	−2.4		
	$\overline{CG}_2$		−1.92	−3.2		
	$\overline{A}_0$ to $\overline{A}_3, \overline{B}_0$ to $\overline{B}_3, \overline{CG}_1$		−2.88	−4.8		
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−30	−65	−100	mA	V_{CC} = MAX. V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		85	135	mA	9340XM, V_{CC} = MAX.
			85	146	mA	9340XC

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS (Add Mode) MIN.	TYP.	MAX.	LIMITS (Subtract Mode) MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
t_{PLH}	Turn off delay } Data Input to Data		23	30		28	37	ns	See Table 1 and Fig. 3	V_{CC} = 5.0V, C_L = 15pF
t_{PHL}	Turn on delay } Output ($\overline{B}_0$ to $\overline{F}_3$)		23	30		25	32	ns		
t_{PLH}	Turn off delay } Data Input to Carry		15	20		18	25	ns	See Table 1 and Fig. 3	
t_{PHL}	Turn on delay } Output ($\overline{B}_0$ to $\overline{CO/CG}$)		16	20		17	22	ns		
t_{PLH}	Turn off delay } Carry Input to Carry		15	19		15	19	ns	See Table 1 and Fig. 4	
t_{PHL}	Turn on delay } Output ($\overline{CG}_3$ to $\overline{CO/CG}$)		15	19		15	19	ns		
t_{PLH}	Turn off delay } Carry Input to Data		23	31		23	31	ns	See Table 1 and Fig. 4	
t_{PHL}	Turn on delay } Output ($\overline{CG}_3$ to $\overline{F}_3$)		22	29		22	29	ns		

TABLE I SWITCHING TEST CONDITIONS

PARAMETER	OPERATION	INPUTS AT 4.5V	INPUTS AT GND	WAVEFORM
t_{PLH} ($\overline{B}_0$ $\overline{F}_3$) t_{PHL} ($\overline{B}_0$ $\overline{F}_3$)	Add	$S_0, \overline{CG}_1, \overline{CP}_1, \overline{B}_1, \overline{B}_2$	$S_1, \overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3, \overline{B}_3$	1
t_{PLH} ($\overline{B}_0$ $\overline{F}_3$) t_{PHL} ($\overline{B}_0$ $\overline{F}_3$)	Subtract	$\overline{CG}_1, \overline{CP}_1, \overline{B}_3$	$S_0, S_1, \overline{A}_0, \overline{A}_1, \overline{A}_2, A_3$ $\overline{B}_1, \overline{B}_2$	2
t_{PLH} ($\overline{B}_0$ $\overline{CO/CG}$) t_{PHL} ($\overline{B}_0$ $\overline{CO/CG}$)	Add	$S_0, \overline{CG}_1, \overline{CP}_1, \overline{B}_1, \overline{B}_2, \overline{B}_3$	S_1, COE, $\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$	1
t_{PLH} ($\overline{B}_0$ $\overline{CO/CG}$) t_{PHL} ($\overline{B}_0$ $\overline{CO/CG}$)	Subtract	$\overline{CG}_1, \overline{CP}_1$	S_0, S_1, COE, $\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$ $\overline{B}_1, \overline{B}_2, \overline{B}_3$	2
t_{PLH} ($\overline{CG}_3$ $\overline{CO/CG}$) t_{PHL} ($\overline{CG}_3$ $\overline{CO/CG}$)	Add	$S_0, \overline{CG}_1, \overline{CG}_2,$ COE, $\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$	$S_1, \overline{B}_0, \overline{B}_1, \overline{B}_2, \overline{B}_3$ $\overline{CP}_1, \overline{CP}_2$	1
t_{PLH} ($\overline{CG}_3$ $\overline{F}_3$) t_{PHL} ($\overline{CG}_3$ $\overline{F}_3$)	Add	$S_0, \overline{CG}_1, \overline{CG}_2, \overline{B}_3$ $\overline{A}_0, \overline{A}_1, \overline{A}_2, \overline{A}_3$	S_1, B_0, B_1, B_2 $\overline{CP}_1, \overline{CP}_2$	1

SWITCHING WAVEFORMS

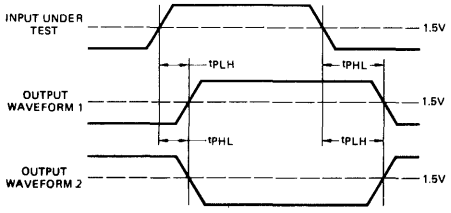


Fig. 2

TYPICAL PROPAGATION DELAYS DATA INPUT TO DATA OUTPUT AND DATA INPUT TO CARRY OUTPUT (ADD MODE)

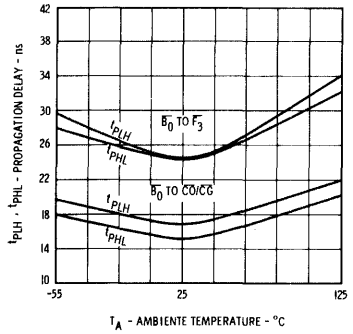


Fig. 3

TYPICAL PROPAGATION DELAYS CARRY INPUT TO CARRY OUTPUT AND CARRY INPUT TO DATA OUTPUT (ADD MODE)

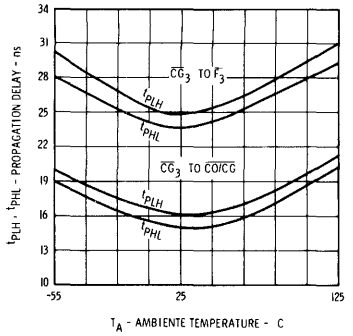


Fig. 4

TTL/MSI 9341/54181, 74181
4-BIT ARITHMETIC LOGIC UNIT

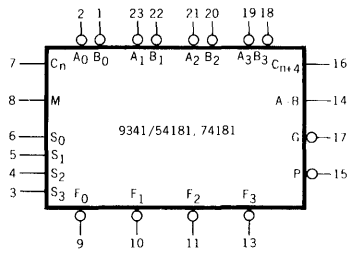
DESCRIPTION – The TTL/MSI 9341/54181, 74181 is a 4-bit high speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The ALU is fully compatible with all members of the Fairchild TTL family.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE,
  PLUS TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS
  TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

PIN NAMES		LOADING (Note a)
$\overline{A_0}$ to $\overline{A_3}$, $\overline{B_0}$ to $\overline{B_3}$	Operand (Active LOW) Inputs	3 U.L.
S_0, S_1, S_2, S_3	Function - Select Inputs	4 U.L.
M	Mode Control Input	1 U.L.
C_n	Carry Input	5 U.L.
$\overline{F_0}$, $\overline{F_1}$, $\overline{F_2}$, $\overline{F_3}$	Function (Active LOW) Outputs (Note b)	10 U.L.
A = B	Comparator Output	Open Collector
$\overline{G}$	Carry Generate (Active LOW) Output (Note b)	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.
C_{n+4}	Carry Output (Note b)	10 U.L.

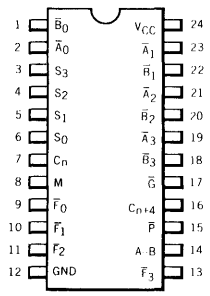
NOTES:
a. 1 Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC SYMBOL

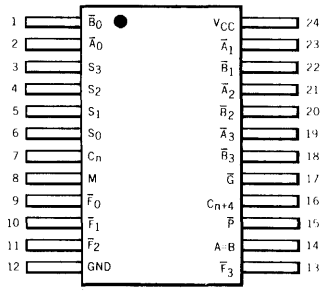


V_{CC} = Pin 24
GND = Pin 12

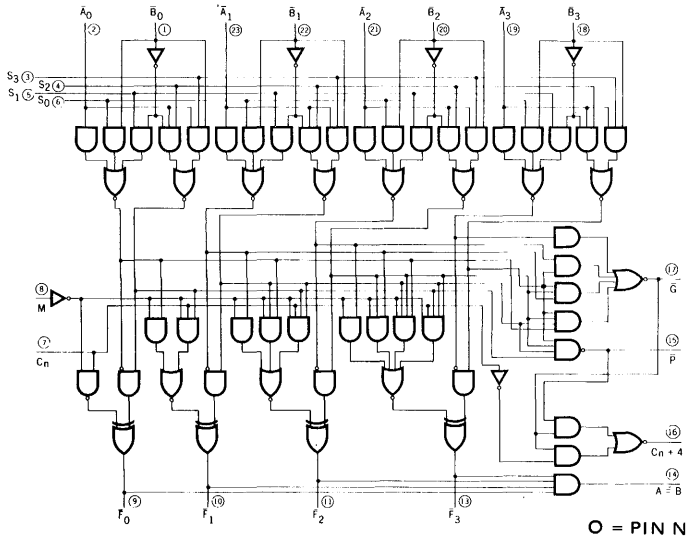
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



O = PIN NUMBERS

8

FUNCTIONAL DESCRIPTION – The TTL/MSI 9341/54181, 74181 is a 4-bit, high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs Logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs Arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals P (carry propagate) and G (carry generate). P and G are not affected by carry in. When speed requirements are not stringent, the 9341/54181, 74181 can be used in a simple ripple carry mode by connecting the carry out (C_{n+4}) signal to the carry input (C_n) of the next unit. For high speed operation the 9341/54181, 74181 is used in conjunction with the 9342/54182, 74182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 9341/54181, 74181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the 9341/54181, 74181 goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A = B output is open collector and can be wire ANDed with other A = B outputs to give a comparison for more than 4-bits. The A = B signal can also be used with the carry out signal to indicate A > B and A < B.

The Function Table lists the Arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus Select Code LHHL generates A minus B minus 1 (2's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1's complement), a CARRY OUT means BORROW; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

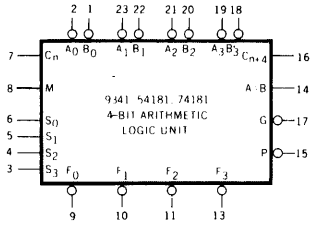
As indicated the 9341/54181, 74181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

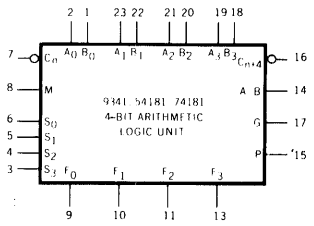
MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L L H L	$\overline{A+B}$	$A\overline{B}$ minus 1	$A\overline{B}$	$A+\overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A+B}$	A plus $(A+\overline{B})$	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus $(A+\overline{B})$	$\overline{B}$	$(A+B)$ plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H H H	$A+\overline{B}$	$A+\overline{B}$	$A\overline{B}$	$A\overline{B}$ minus 1
H L L L	$\overline{A}B$	A plus $(A+B)$	$\overline{A}+B$	A plus AB
H L L H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus $(A+B)$	B	$(A+\overline{B})$ plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$(A+B)$ plus A
H H H L	AB	$A\overline{B}$ plus A	$A+B$	$(A+\overline{B})$ plus A
H H H H	A	A	A	A minus 1

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



H = High Voltage Level
L = Low Voltage Level

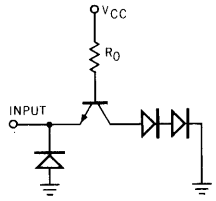
V_{CC} = Pin 24
GND = Pin 12

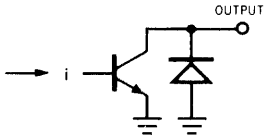
*Each bit is shifted to the next more significant position

**Arithmetic operations expressed in 2's complement notation

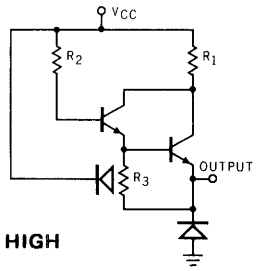
TYPICAL INPUT AND OUTPUT CIRCUITS

INPUTS EQUIVALENT CIRCUIT





OUTPUTS EQUIVALENT CIRCUITS



HIGH

INPUT CURRENT VERSUS INPUT VOLTAGE

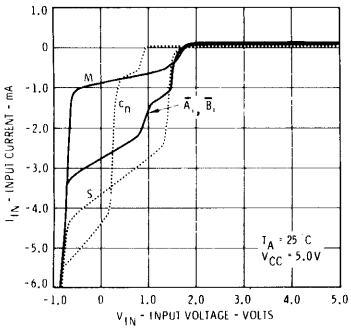


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

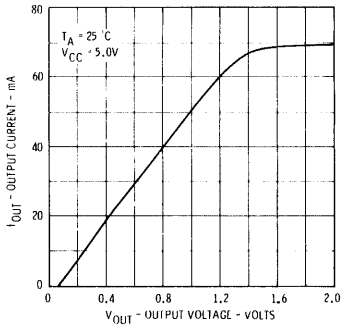


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE

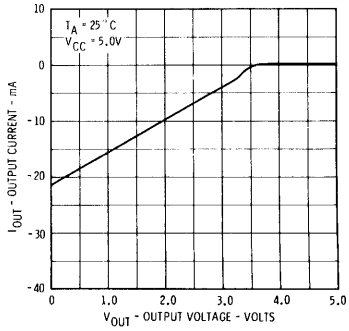


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9341XM/54181XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9341XC/74181XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS	
V_{IH}	Input HIGH Voltage	2.0		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		0.8	V	Guaranteed Input LOW Voltage for all Inputs	
V_{CD}	Input Clamp Diode Voltage		−1.5	V	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C	
I_{CEX}	A = B Output Leakage Current (Open Collector)		250	μA	V_{CC} = MIN., V_{OUT} = 5.5 V	
V_{OH}	Output HIGH Voltage	2.4		V	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.4	V	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table	
I_{IH}	Input HIGH Current M $\bar{A}_0\ \bar{A}_1\ \bar{A}_2\ \bar{A}_3\ \bar{B}_0\ \bar{B}_1\ \bar{B}_2\ \bar{B}_3$ $S_0\ S_1\ S_2\ S_3$ C_n		 40 120 160 200	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
	Input HIGH Current All Inputs		1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current M $\bar{A}_0\ \bar{A}_1\ \bar{A}_2\ \bar{A}_3\ \bar{B}_0\ \bar{B}_1\ \bar{B}_2\ \bar{B}_3$ $S_0\ S_1\ S_2\ S_3$ C_n		 −1.6 −4.8 −6.4 −8.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{SC} (I_{OS})	Output Short Circuit Current (Note 4)	−20	−55	mA	XM	V_{CC} = MAX., V_{OUT} = 0.0 V
		−18	−57	mA	XC	
I_{CC}	Power Supply Current		127	mA	XM	V_{CC} = MAX. C_n = B_0 = B_1 = B_2 = B_3 = GND All Other Inputs = 4.5 V
			140	mA	XC	
			135	mA	XM	V_{CC} = MAX. M = S_0 = S_1 = S_2 = S_3 = 4.5 V All Other Inputs = GND
			150	mA	XC	

8

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND)

SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH} t_{PHL}	(C_n to C_n + 4)	12 13	16 17	ns	M = OV, (Sum or Diff Mode) See Fig. 4 and Tables I & II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ outputs)	15 14	17 17	ns	M = OV, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	16 9	19 12	ns	M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	18 13	22 17	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	16 11	19 15	ns	M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	17 14	21 21	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs)	19 19	26 26	ns	M = S_1 = S_2 = OV, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs)	20 26	26 32	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_{i+1}$ outputs)	23 19	29 25	ns	M = OV, S_0 = S_3 = 4.5 V, S_1 = S_2 = OV (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_{i+1}$ outputs)	23 24	29 30	ns	M = OV, S_0 = S_3 = OV, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{F}$ outputs)	18 19	24 24	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	16 26	21 30	ns	M = OV, S_0 = S_3 = 4.5 V, S_1 = S_2 = OV (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	19 26	25 30	ns	M = OV, S_0 = S_3 = OV, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to A = B output)	33 34	40 42	ns	M = S_0 = S_3 = OV, S_1 = S_2 = 4.5 V, R_o = 400 Ω to 5.0 V (Diff Mode) See Fig. 5 and Table II

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Note more than one output should be shorted at a time.

SWITCHING TIME WAVEFORMS

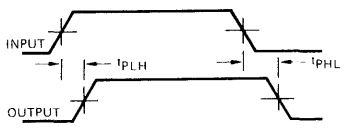


Fig. 4

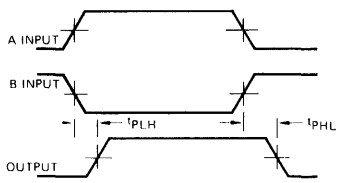


Fig. 5

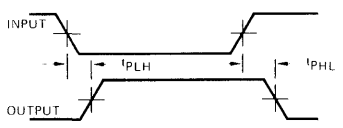


Fig. 6

SUM MODE TEST TABLE I — **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or $C_n + 4$

DIFF MODE TEST TABLE II — **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_i + 1$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	$C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V

TTL/MSI 93S41

4-BIT ARITHMETIC LOGIC UNIT

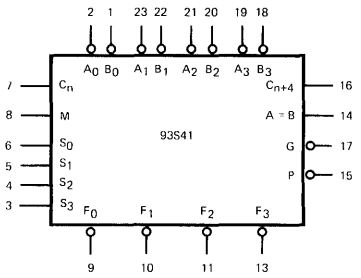
DESCRIPTION – The TTL/MSI 93S41 is a 4-bit high speed Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the Add and Subtract modes are the most important. The ALU is fully compatible with all members of the Fairchild TTL family and incorporates the Schottky TTL process to achieve super high speeds.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS
  TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE–OR, COMPARE, AND, NAND, OR, NOR, PLUS
  TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION ON LONG WORDS**
- **INPUT CLAMP DIODES**
- **TYPICAL ADD TIME FOR 16-BITS IS 19ns**
- **TYPICAL POWER DISSIPATION OF 500mW**

PIN NAMES

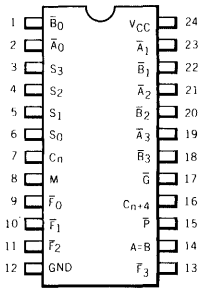
$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand (Active LOW) Inputs
S_0, S_1, S_2, S_3	Function – Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$	Function (Active LOW) Outputs
A = B	Comparator Output
$\overline{G}$	Carry Generate (Active LOW) Output
$\overline{P}$	Carry Propagate (Active LOW) Output
$C_n + 4$	Carry Output

LOGIC SYMBOL

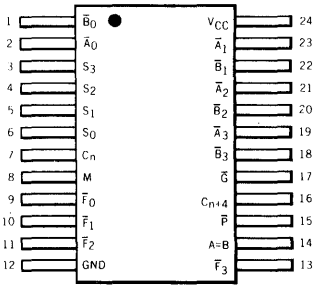


V_{CC} = PIN 24
GND = PIN 12

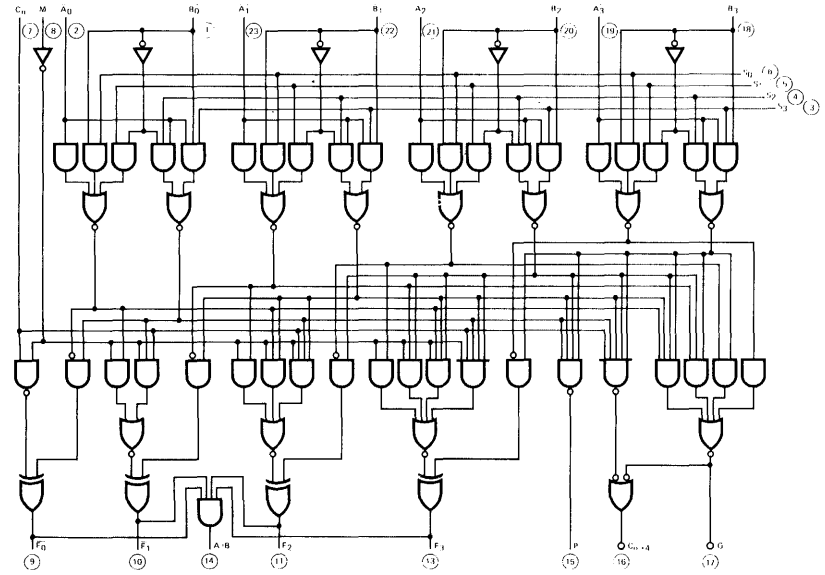
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The TTL/MSI 93S41 is a 4-bit super high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table below lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs Logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs Arithmetic operations on the two, 4-bit words. The device incorporates full internal look-ahead carry and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals P (carry propagate) and G (carry generate). P and G are not affected by carry in. When speed requirements are not stringent, the 93S41 can be used in a simple ripple carry mode by connecting the carry out (C_{n+4}) signal to the carry input (C_n) of the next unit. For high speed operation the 93S41 is used in conjunction with the 93S42 carry look-ahead circuit. One carry look-ahead package is required for each group of four 93S41 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the 93S41 goes HIGH when all four F outputs are HIGH and can be used to indicate logic equivalence over 4-bits when the unit is in the subtract mode. The A = B output is open collector and can be wire ANDed with other A = B outputs to give a comparison for more than 4-bits. The A = B signal can also be used with the carry out signal to indicate A > B and A < B.

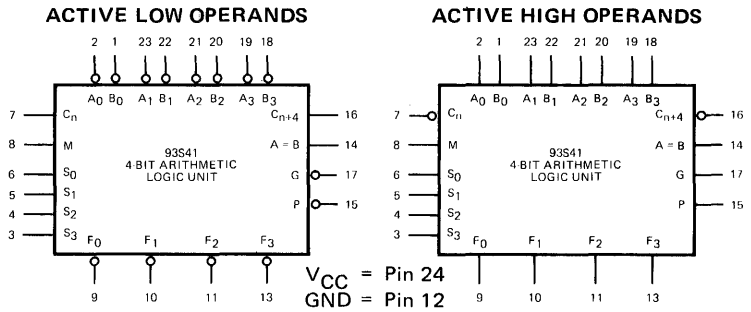
The Function Table lists the Arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus Select Code LHHL generates A minus B minus 1 (2's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1's complement), a CARRY OUT means BORROW; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated the 93S41 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

MODE SELECT INPUTS	ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
S_3 S_2 S_1 S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L L H L	$\overline{A+B}$	$A\overline{B}$ minus 1	$\overline{A}B$	A + $\overline{B}$
L L H H	Logical 1	minus 1	Logical 0	minus 1
L H L L	$\overline{A+B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
L H L H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	A ⊕ B	A minus B minus 1
L H H H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	AB minus 1
H L L L	$\overline{A}B$	A plus (A + B)	$\overline{A+B}$	A plus AB
H L L H	A ⊕ B	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H L H H	A + B	A + B	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H H H L	AB	$A\overline{B}$ plus A	A + B	(A + $\overline{B}$) plus A
H H H H	A	A	A	A minus 1

LOGIC SYMBOLS



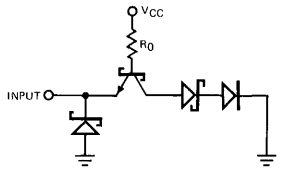
L = LOW Voltage Level H = HIGH Voltage Level

*Each bit is shifted to the next more significant position

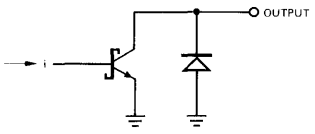
**Arithmetic operations expressed in 2's complement notation

TYPICAL INPUT AND OUTPUT CIRCUITS

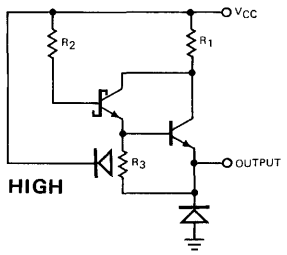
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUITS



LOW



HIGH

INPUT CURRENT VERSUS INPUT VOLTAGE

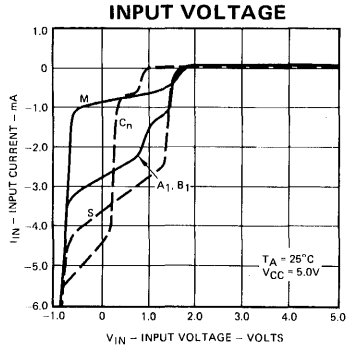


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE

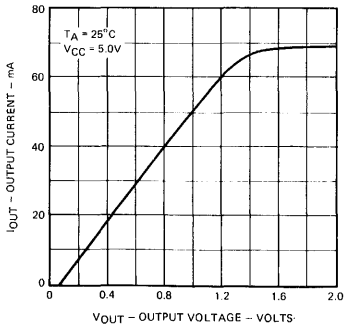


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE

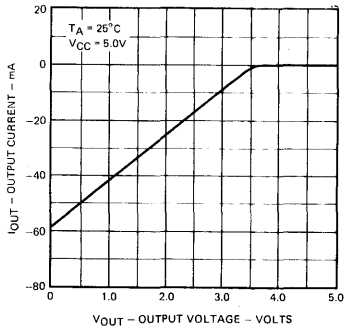


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93S41XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
93S41XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage for all Inputs
V_{CD}	Input Clamp Diode Voltage			−1.2	Volts	V_{CC} = MIN., I_{IN} = −18 mA, T_A = 25°C
I_{CEX}	A = B Output Leakage Current (Open Collector)			250	μA	V_{CC} = MIN., V_{OUT} = 5.5 V
V_{OH}	Output HIGH Voltage	2.5			Volts	XM: V_{CC} = MIN., I_{OH} = −1.0 mA; V_{IN} = V_{IH} or V_{IL} per Truth Table
		2.7				XC: V_{CC} = MIN., I_{OH} = −1.0 mA; V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage			0.5	Volts	V_{CC} = MIN., I_{OL} = 20 mA; V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				μA	V_{CC} = MAX., V_{IN} = 2.7 V
	M			50		
	$\overline{A}_0$ $\overline{A}_1$ $\overline{A}_2$ $\overline{A}_3$ $\overline{B}_0$ $\overline{B}_1$ $\overline{B}_2$ $\overline{B}_3$			150		
	S_0 S_1 S_2 S_3			200		
	C_n			300		
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current				mA	V_{CC} = MAX., V_{IN} = 0.4 V
	M			−1.6		
	$\overline{A}_0$ $\overline{A}_1$ $\overline{A}_2$ $\overline{A}_3$ $\overline{B}_0$ $\overline{B}_1$ $\overline{B}_2$ $\overline{B}_3$			−4.8		
	S_0 S_1 S_2 S_3			−6.4		
	C_n			−9.6		
I_{SC} (I_{OS})	Output Short Circuit Current (Note 4)	−40		−100	mA	V_{CC} = MAX., V_{OUT} = 0 V
I_{CC}	Power Supply Current		95	125	mA	XM: V_{CC} = MAX., C_n = B_0=B_1=B_2=B_3=GND; All Other Inputs = 4.5 V
			95	140	mA	XC: V_{CC} = MAX., C_n = B_0=B_1=B_2=B_3=GND; All Other Inputs = 4.5 V
			105	135	mA	XM: V_{CC} = MAX., M = S_0=S_1=S_2=S_3=4.5 V; All Other Inputs = GND
			105	150	mA	XC: V_{CC} = MAX., M = S_0=S_1=S_2=S_3=4.5 V; All Other Inputs = GND

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, Pin 12 = GND)

SYMBOL	PARAMETER	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH} t_{PHL}	(C_n to C_{n+4})	7.0 7.0	12 12	ns	M = 0 V, (Sum or Diff Mode) See Fig. 4 and Tables I & II
t_{PLH} t_{PHL}	(C_n to $\overline{F}$ outputs)	7.0 7.0	12 12	ns	M = 0 V, (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	9.5 7.0	14 14	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output)	9.5 9.0	15 15	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	8.5 8.0	14 14	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output)	8.5 10	15 15	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to any $\overline{F}$ output)	15 9.0	20 20	ns	M = S_1 = S_2 = 0 V, S_0 = S_3 = 4.5 V (Sum Mode) See Fig. 4 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to any $\overline{F}$ output)	14 11	21 21	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode) See Fig. 5 and Table II
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to $\overline{F}$ outputs)	10 10	20 20	ns	M = 4.5 V (Logic Mode) See Fig. 4 and Table III
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	10 13	18.5 18.5	ns	M = 0 V, S_0 = S_3 = 4.5 V, S_1 = S_2 = 0 V (Sum Mode) See Fig. 6 and Table I
t_{PLH} t_{PHL}	($\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output)	12 13	23 23	ns	M = 0 V, S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V (Diff Mode)
t_{PLH}	($\overline{A}$ or $\overline{B}$ inputs to A = B output)	13	23	ns	M = S_0 = S_3 = 0 V, S_1 = S_2 = 4.5 V, R_o = 400 Ω to 5.0 V
t_{PHL}		13	23		(Diff Mode) See Fig. 5 and Table II

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Not more than one output should be shorted at a time.

SWITCHING TIME WAVEFORMS

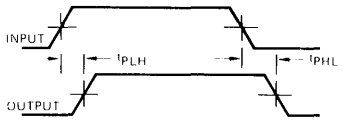


Fig. 4

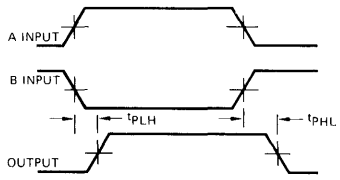


Fig. 5

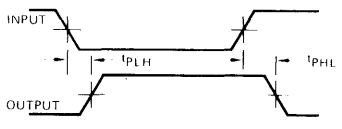


Fig. 6

SUM MODE TEST TABLE I — **FUNCTION INPUTS:** $S_0 = S_3 = 4.5$ V, $S_1 = S_2 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	C_n	Remaining $\overline{A}$ and $\overline{B}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II — **FUNCTION INPUTS:** $S_1 = S_2 = 4.5$ V, $S_0 = S_3 = M = 0$ V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{B}$, C_n	Remaining $\overline{A}$	$\overline{F}_{i+1}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$	$S_1 = S_3 = M = 4.5$ V $S_0 = S_2 = 0$ V

TTL/MSI 9342/54182, 74182
LOOKAHEAD CARRY GENERATOR

DESCRIPTION – The TTL/MSI 9342/54182, 74182 is a high speed Lookahead Carry Generator. It is generally used with the 9341/54181, 74181 4-Bit Arithmetic Logic Unit to provide high speed lookahead over word lengths of more than four bits. The lookahead carry generator is fully compatible with all members of the Fairchild TTL Family.

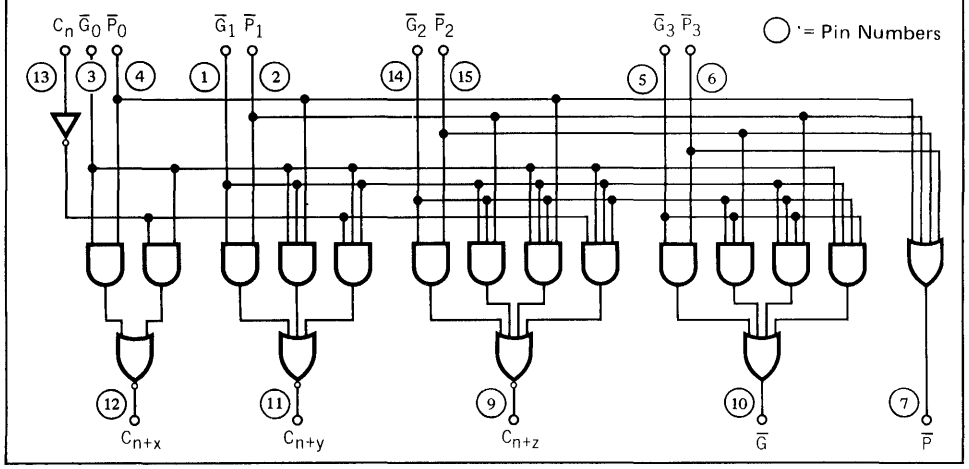
- **PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

PIN NAMES

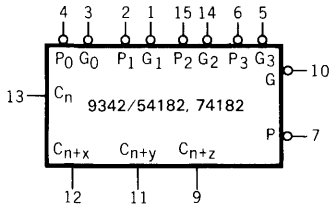
		LOADING (Note a)
C_n	Carry Input	1 U.L.
$\overline{G}_0$, $\overline{G}_2$	Carry Generate (Active LOW) Inputs	7 U.L.
$\overline{G}_1$	Carry Generate (Active LOW) Input	8 U.L.
$\overline{G}_3$	Carry Generate (Active LOW) Input	4 U.L.
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate (Active LOW) Inputs	4 U.L.
$\overline{P}_2$	Carry Propagate (Active LOW) Input	3 U.L.
$\overline{P}_3$	Carry Propagate (Active LOW) Input	2 U.L.
C_{n+x}, C_{n+y}, C_{n+z}	Carry Outputs (Note b)	10 U.L.
$\overline{G}$	Carry Generate (Active LOW) Output (Note b)	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output (Note b)	10 U.L.

Notes:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

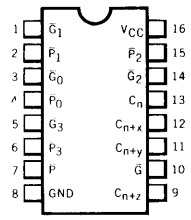


LOGIC SYMBOL

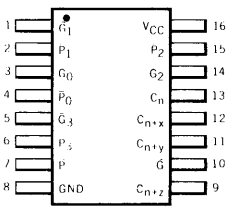


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



FUNCTIONAL DESCRIPTION—The TTL/MSI 9342/54182, lookahead carry generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$) and Carry Generate ($\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$) signals and an active HIGH Carry Input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 9342/54182, 74182 also has active LOW Carry Propagate (P) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.
The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Also, the 9342/54182, 74182 can be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the lookahead carry generator are identical in both cases.

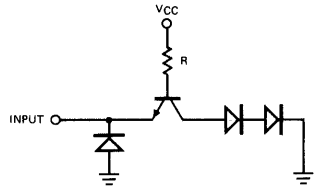
TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	X	H	X	X				H	
	H		X	H	X	H	X	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

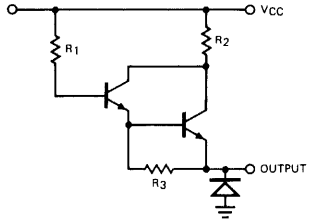
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

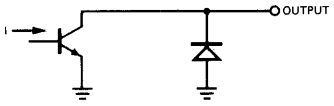
EQUIVALENT INPUT CIRCUIT



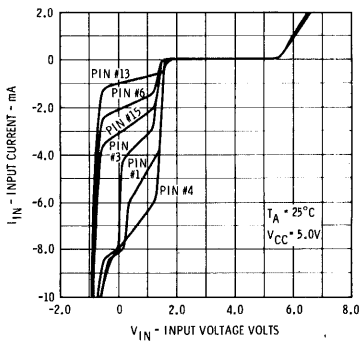
OUTPUT HIGH EQUIVALENT CIRCUIT



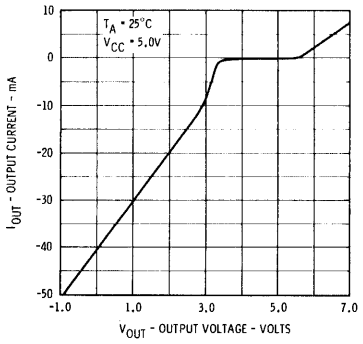
OUTPUT LOW EQUIVALENT CIRCUIT



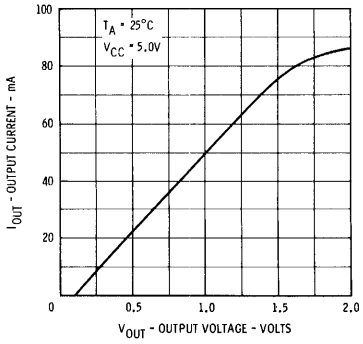
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9342XM/54182XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9342XC/74182XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS MAX.	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	2.4		Volts	V_{CC} = MIN., I_{OH} = −800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage		0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{IH}	Input HIGH Voltage	2.0		Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage		0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{CD}	Input Clamp Diode Voltage		−1.5	Volts	V_{CC} = MIN., I_{IN} = −12 mA, T_A = 25°C
I_{IL}	Input LOW Current $\overline{C_n}$ $\overline{P_3}$ $\overline{P_2}$ $\overline{P_0}$, $\overline{P_1}$ or $\overline{G_3}$ $\overline{G_0}$ or $\overline{G_2}$ $\overline{G_1}$		 −1.6 −3.2 −4.8 −6.4 −11.2 −12.8	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input HIGH Current $\overline{C_n}$ $\overline{P_3}$ $\overline{P_2}$ $\overline{P_0}$, $\overline{P_1}$ or $\overline{G_3}$ $\overline{G_0}$ or $\overline{G_2}$ $\overline{G_1}$		 40 80 120 160 280 320	μA	V_{CC} = MAX., V_{IN} = 2.4 V
	Input HIGH Current all inputs		1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{SC}	Output Short Circuit Current (Note 4)	−40	−100	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CCH}	Power Supply Current 9342XM/54182XM 9342XC/74182XC		 35 39	 mA mA	V_{CC} = MAX. All outputs HIGH
I_{CCL}	Power Supply Current 9342XM/54182XM 9342XC/74182XC		 65 72	 mA mA	V_{CC} = MAX. All Outputs LOW

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, Pin 8 = Gnd)

SYMBOL	PARAMETER	LIMITS		UNITS	CONDITIONS
		TYP.	MAX.		
t_{PLH} t_{PHL}	(C_n to C_{n+x}, C_{n+y}, C_{n+z})	12 15	16 19	ns	$\overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, $\overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5V Fig.1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, or $\overline{P}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})	8 9	10 11	ns	$\overline{P}_x$ = Gnd (If not under test), $C_n = \overline{G}_0 = \overline{G}_1 = \overline{G}_2$ = 4.5V, Fig.2
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, or C_{n+z})	8 9	10 11	ns	$\overline{G}_x$ = 4.5V (If not under test), $C_n = \overline{P}_0 = \overline{P}_1 = \overline{P}_2$ = Gnd, Fig.2
t_{PLH} t_{PHL}	($\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$ or $\overline{P}$)	12 15	16 19	ns	$\overline{P}_x$ = Gnd (If not under test), $\overline{G}_0 = \overline{G}_1 = \overline{G}_2 = \overline{G}_3 = C_n$ = 4.5 V Fig.1
t_{PLH} t_{PHL}	($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ or $\overline{G}_3$ to $\overline{G}$)	12 15	16 19	ns	$\overline{G}_x$ = 4.5V (If not under test), $\overline{P}_1 = \overline{P}_2 = \overline{P}_3$ = Gnd, Fig. 1
t_{PLH} t_{PHL}	($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{P}$)	12 15	16 19	ns	$\overline{P}_x$ = Gnd (If not under test), Fig. 1

SWITCHING TIME WAVEFORMS

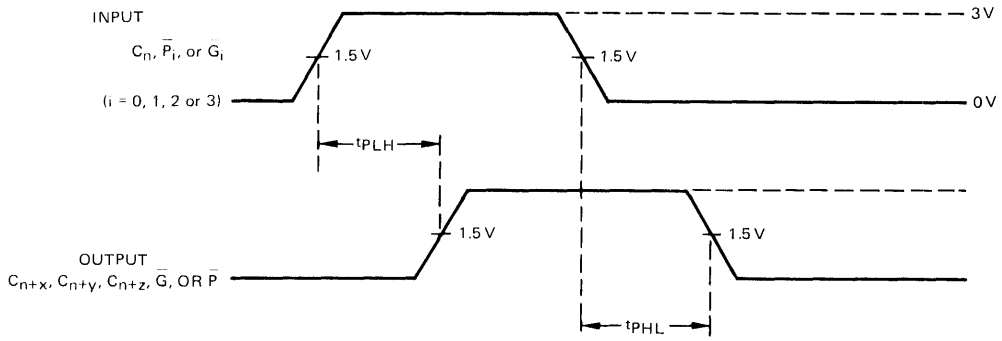


Fig. 1

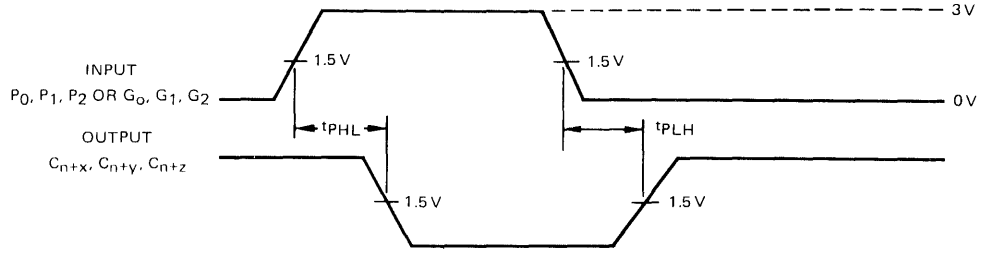


Fig. 2

TTL/MSI 93S42
LOOKAHEAD CARRY GENERATOR

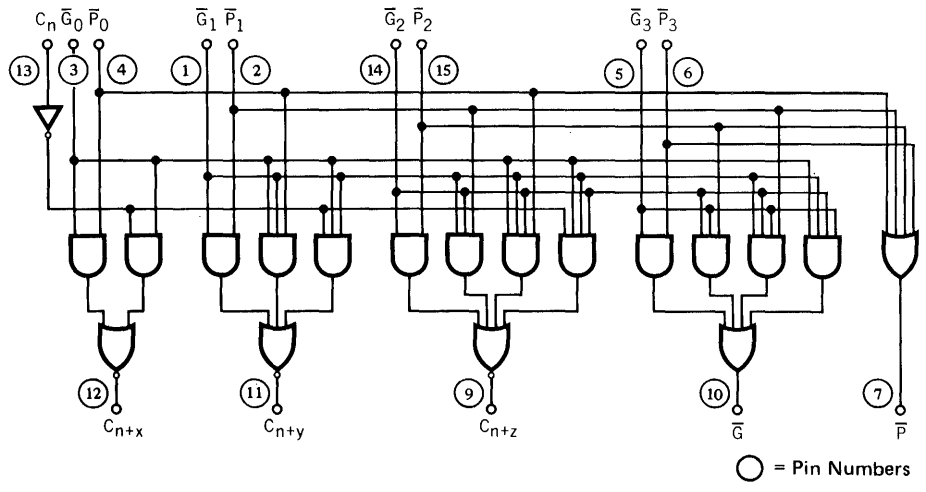
DESCRIPTION – The TTL/MSI 93S42 is a high speed Lookahead Carry Generator. It is generally used with the 93S41 4-Bit Arithmetic Logic Unit to provide super high speed lookahead over word lengths of more than four bits. The lookahead carry generator is fully compatible with all members of the Fairchild TTL Family.

- **TYPICALLY 4 ns DELAY FOR EACH LEVEL OF LOOKAHEAD**
- **PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**
- **INPUT CLAMP DIODES**
- **TTL COMPATIBLE**

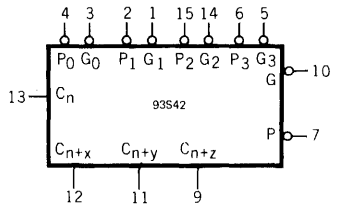
PIN NAMES

C_n	Carry Input
$\overline{G}_0$, $\overline{G}_2$	Carry Generate (Active Low) Inputs
$\overline{G}_1$	Carry Generate (Active Low) Input
$\overline{G}_3$	Carry Generate (Active Low) Input
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate (Active Low) Inputs
$\overline{P}_2$	Carry Propagate (Active Low) Input
$\overline{P}_3$	Carry Propagate (Active Low) Input
C_{n+x}, C_{n+y}, C_{n+z}	Carry Outputs
$\overline{G}$	Carry Generate (Active Low) Output
$\overline{P}$	Carry Propagate (Active Low) Output

LOGIC DIAGRAM

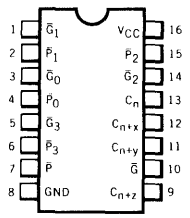


LOGIC SYMBOL

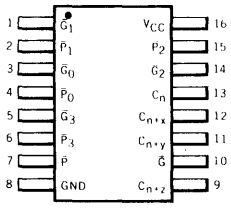


V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

TTL/MSI 9344

BINARY (4-BIT BY 2-BIT) FULL MULTIPLIER

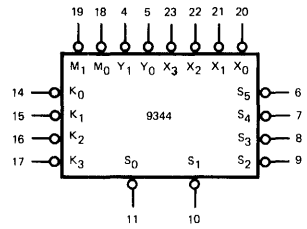
DESCRIPTION – The TTL/MSI 9344 is a 4-bit by 2-bit Full Multiplier building block. It multiplies two binary numbers and simultaneously adds two other binary numbers to the product. 9344's can be interconnected to form a high speed multiplier array of any size. The device is constructed with TTL compatible inputs and outputs. Inputs are buffered to reduce loading. The device is fully compatible with all members of the Fairchild TTL family.

- **PERFORMS DIRECT MULTIPLICATION**
- **EXPANDS TO ANY SIZE ARRAY WITHOUT ADDITIONAL COMPONENTS**
- **MULTIPLIES AND ADDS SIMULTANEOUSLY**
- **TTL COMPATIBLE**

PIN NAMES		LOADING
$\overline{X}_0, \overline{X}_1, \overline{X}_2, \overline{X}_3$	Multiplicand Inputs (Active LOW)	2/3 U.L.
$\overline{Y}_0, \overline{Y}_1$	Multiplier Inputs (Active LOW)	2/3 U.L.
$\overline{M}_1$	Additive	1.0 U.L.
$\overline{K}_0, \overline{M}_0$	Carry Inputs	4.0 U.L.
$\overline{K}_1, \overline{K}_2, \overline{K}_3$	(Active LOW)	2.0 U.L.
$\overline{S}_0, \overline{S}_1, \overline{S}_2, \overline{S}_3, \overline{S}_4, \overline{S}_5$	Outputs	10 U.L.

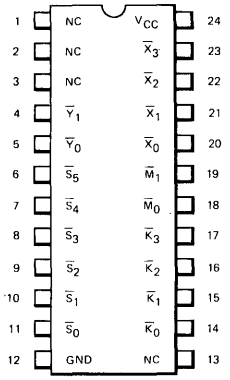
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL

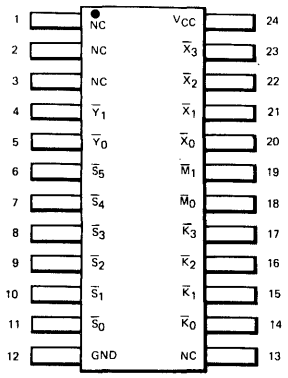


V_{CC} = PIN 24
GND = PIN 12
NC = PIN 1, 2, 3, 13

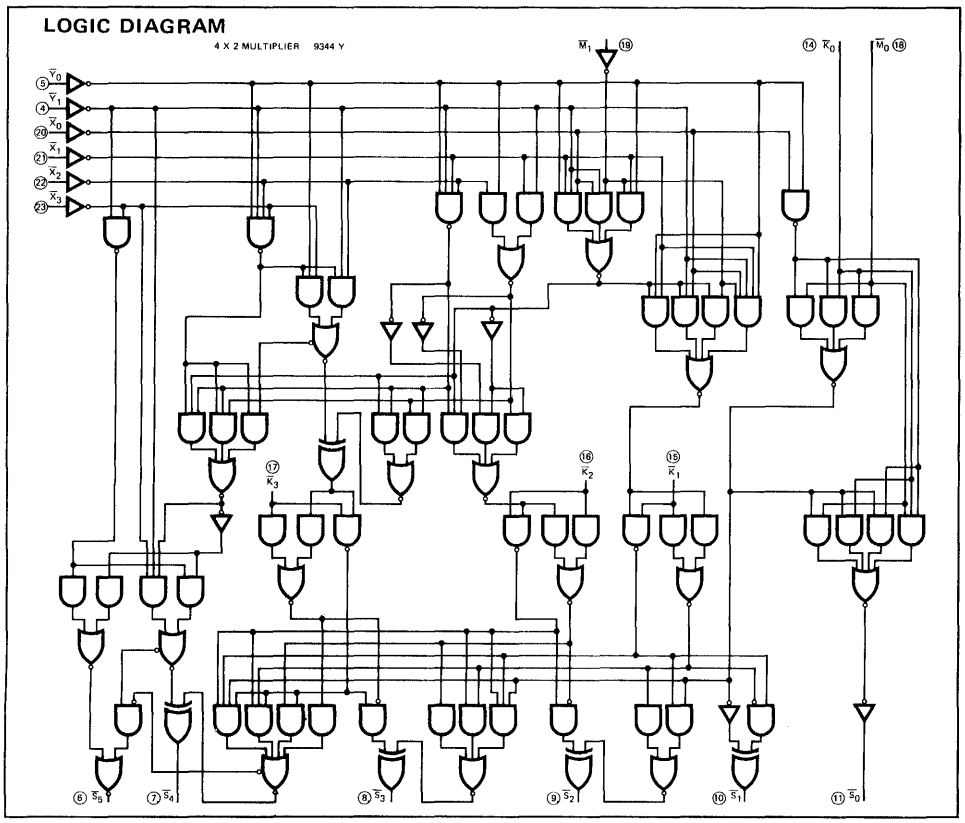
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION – The 9344 is a binary full multiplier for 4-bit by 2-bit words. It is easily expandable in an array to form a high speed parallel multiplier of any length.

The functional equation is illustrated below:

S(6-bits) = $\overline{X}$(4-bits) times $\overline{Y}$(2-bits) plus $\overline{M}$(2-bits) plus $\overline{K}$(4-bits)

Functionally the 9344 multiplies a 4-bit word ($\overline{X}_0 - \overline{X}_3$) by a two bit word ($\overline{Y}_0 - \overline{Y}_1$), generating eight partial products. Two other words, $\overline{K}_0 - \overline{K}_3$ and $\overline{M}_0 - \overline{M}_1$, are added to these partial products through a lookahead carry adder, generating a 6-bit product/sum.

The function can be described by the following equation (note that "+" means arithmetic addition) :

$$S = 2^0 (\overline{X}_0\overline{Y}_0 + \overline{M}_0 + \overline{K}_0) + 2^1 (\overline{X}_1\overline{Y}_0 + \overline{X}_0\overline{Y}_1 + \overline{M}_1 + \overline{K}_1) + 2^2 (\overline{X}_2\overline{Y}_0 + \overline{X}_1\overline{Y}_1 + \overline{K}_2) + 2^3 (\overline{X}_3\overline{Y}_0 + \overline{X}_2\overline{Y}_1 + \overline{K}_3) + 2^4 (\overline{X}_3\overline{Y}_1).$$

All inputs and outputs are active LOW; X and Y inputs are buffered to present only one TTL unit load.

The device operates only on positive numbers. If two's complement mutliplication is required, then the numbers must be changed to sign-magnitude before multiplication, or else the product must be corrected following multiplication of the two's complement numbers. The correction algorithm depends on whether X or Y or both are negative.

If X is negative:
Subtract Y from most significant half of product.

If Y is negative:
Subtract X from most significant half of product.

If both X and Y are negative:
Add X plus Y to most significant half of product.

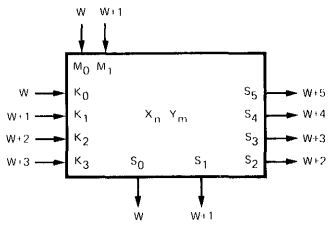
The result will be the correct two's complement product.

MULTIPLICATION TIME

NUMBER OF BITS	PACKAGES	TIME (ns)
8 x 8	8	150
12 x 12	18	260
16 x 16	32	350
24 x 24	72	550

Fig. 1

WEIGHTING FACTORS OF THE BASIC MULTIPLIER



This block represents the basic 4 by 2-bit multiplier, and indicates the weighting factors (power of two) attached to each of the inputs and outputs.

Fig. 2

8

SWITCHING CHARACTERISTICS

$\overline{M}_1$ TO $\overline{S}_3$

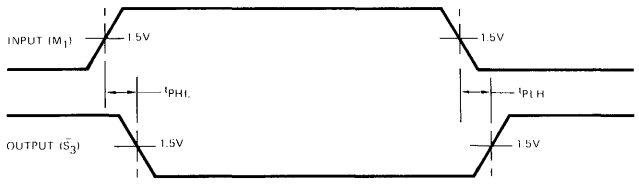


Fig. 3

$\overline{K}_0$ TO $\overline{S}_5$

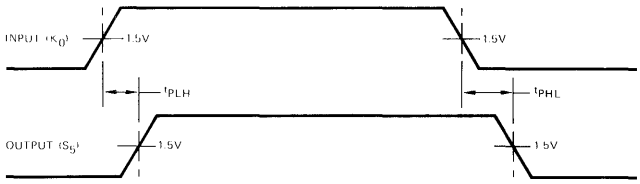


Fig. 4

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9344 XM	4.5 V	5.0 V	5.5 V	-55°C to 125° C
9344 XC	4.75 V	5.0 V	5.25 V	0°C to 75° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Votlage for All Inputs
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -800 μA, V_{IN} = V_{IH} or V_{IL}
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}
I_{IH}	Input HIGH Current $\overline{Y}_{0,1}$; $\overline{X}_{0,1,2,3}$ $\overline{M}_1$ $\overline{K}_{1,2,3}$ K_0, $\overline{M}_0$			 27 40 80 160	 μA	V_{CC} = MAX., V_{IN} = 2.4 V
I_{IL}	Input LOW Current $\overline{Y}_{0,1}$; $\overline{X}_{0,1,2,3}$ $\overline{M}_1$ $\overline{K}_{1,2,3}$ $\overline{K}_0$, $\overline{M}_0$			 -1.07 -1.6 -3.2 -6.4	 mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC}	Output Short Circuit Current (Note 5)	-20		-70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		110	150	mA	V_{CC} = MAX.
V_{CD}	Input Clamp Diode Voltage			-1.5	Volts	V_{CC} = MIN., I_{IN} = -12 mA, T_A = 25°C

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	CONDITIONS
t_{PLH}	Turn Off Delay Input to Output ($\overline{M}_1$ to $\overline{S}_3$)		40	51	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL}	Turn On Delay Input to Output ($\overline{M}_1$ to $\overline{S}_3$)		40	52	ns	
t_{PLH}	Turn Off Delay Input to Output ($\overline{K}_0$ to $\overline{S}_5$)		16	22	ns	
t_{PHL}	Turn On Delay Input to Output ($\overline{K}_0$ to $\overline{S}_5$)		30	39	ns	

TYPICAL MULTIPLICATION ARRAYS

The 9344 can be assembled in an iterative structure to perform multi-bit multiplication. The blocks are interconnected so that partial product sums generated in a particular 9344 are applied, if necessary, to equal weight carry inputs ($\overline{K}_{0,1,2,3}$ or $\overline{M}_{0,1}$) of succeeding stages.

In the iteritive multiplication arrays shown, weighting factors of the carry and sums between 9344's are indicated (i.e., $0 = 2^0$, $1 = 2^1$, $2 = 2^2$, etc.). Labels inside the blocks identify bits multiplied in that block. For instance 0–0 refers to multiplicand bits $B_{0,1,2,3}$ and multiplier bits $A_{0,1}$, while 4–2 would represent multiplicant bits $B_{4,5,6,7}$ and multiplier bits $A_{2,3}$.

8-BIT BY 5-BIT MULTIPLICATION ARRAY

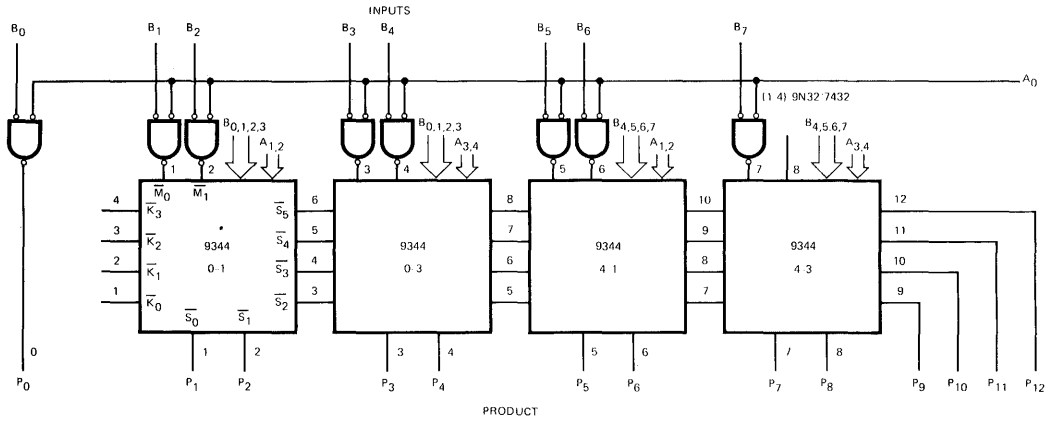


Fig. 5

8-BIT BY 8-BIT MULTIPLICATION ARRAY

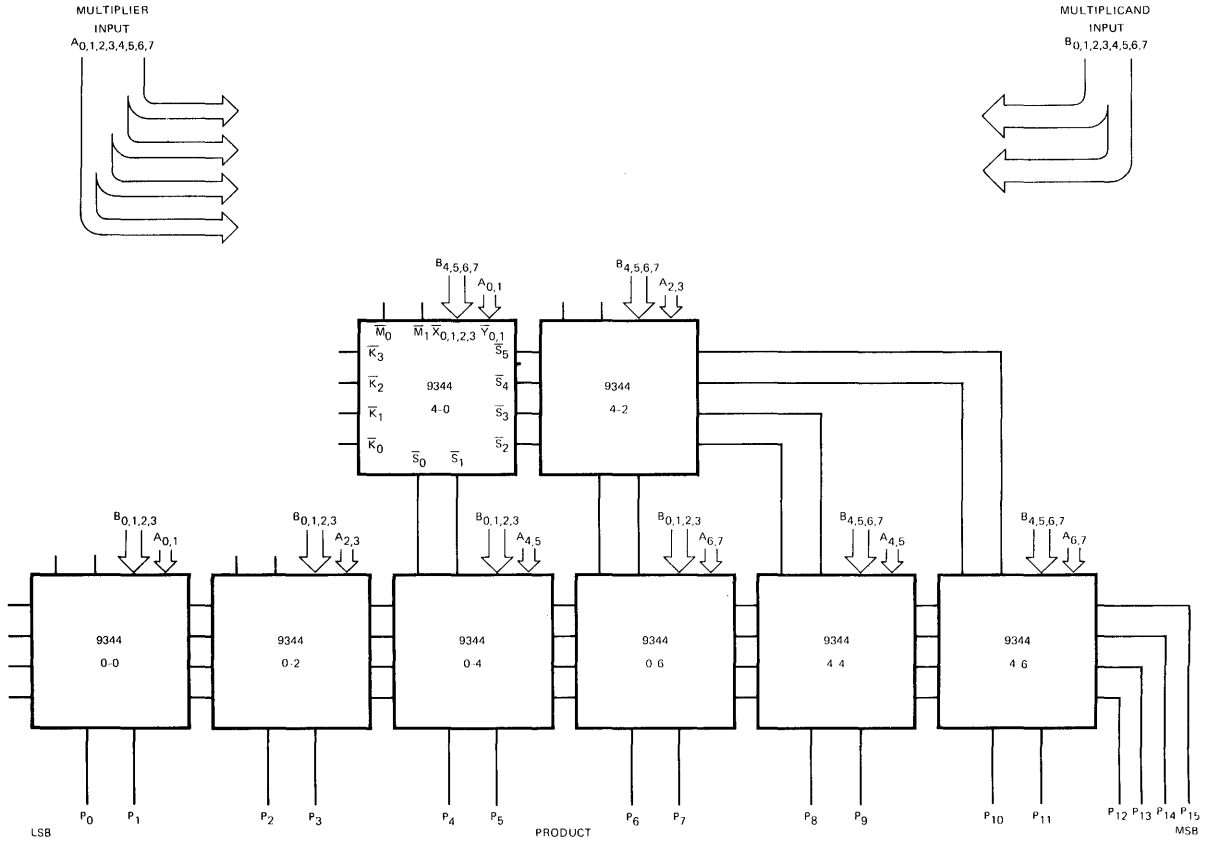
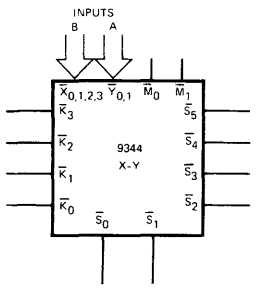


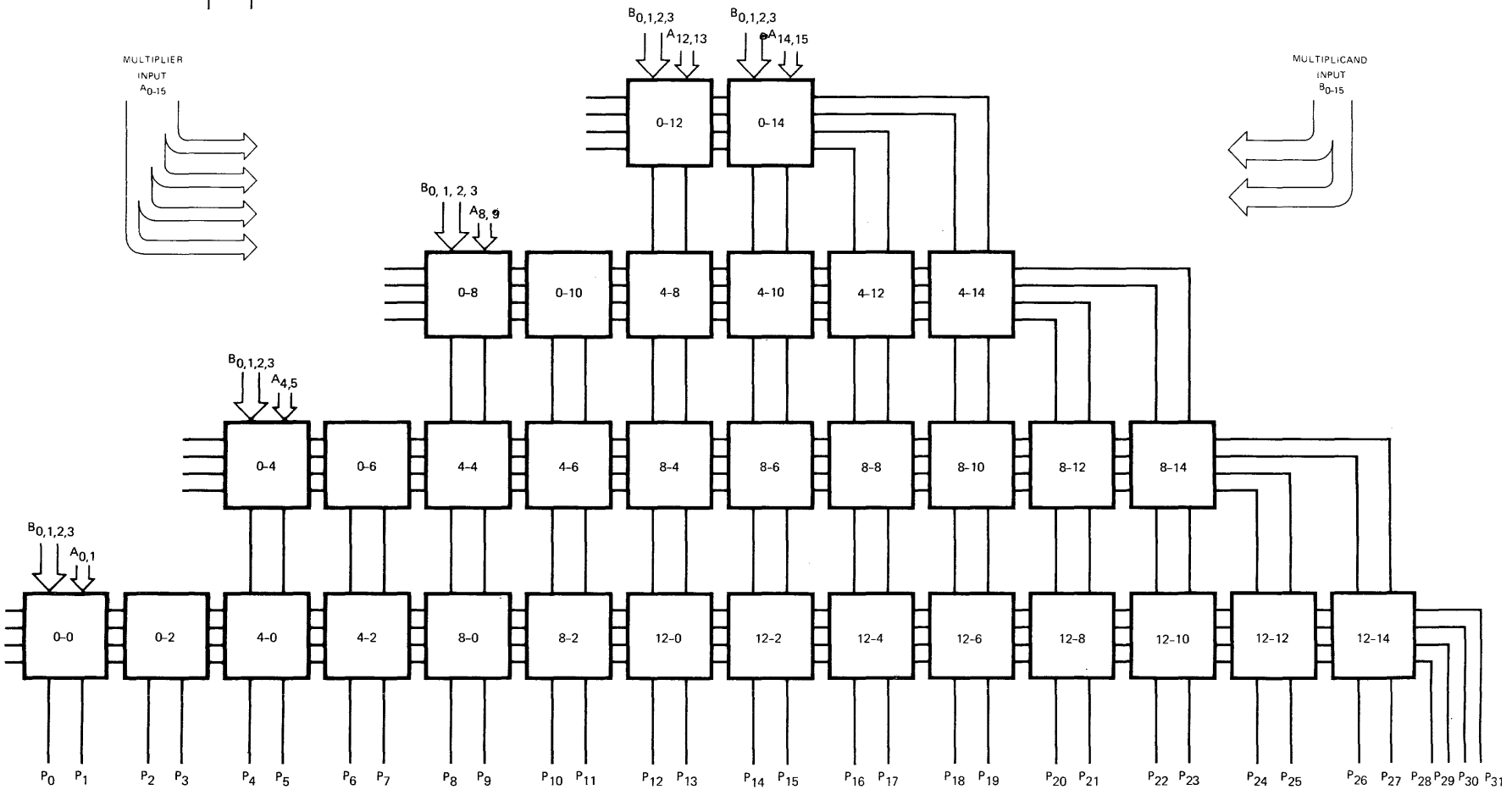
Fig. 6

TYPICAL MULTIPLICATION ARRAYS (Cont'd)

16-BIT BY 16-BIT MULTIPLICATION ARRAY



KEY:
X = 4 BIT MULTIPLICAND, INPUT B
Y = 2 BIT MULTIPLIER, INPUT A
ALL INPUTS ACTIVE LOW



Note: Each block represents one 9344. Labels inside the blocks identify bits multiplied in that block. The first number is the 4-bit B input, and the second number is the 2-bit A input. For instance, 12–0 refers to multiplicand bits $B_{12, 13, 14, 15}$ and multiplier bits $A_{0, 1}$.

Fig. 7

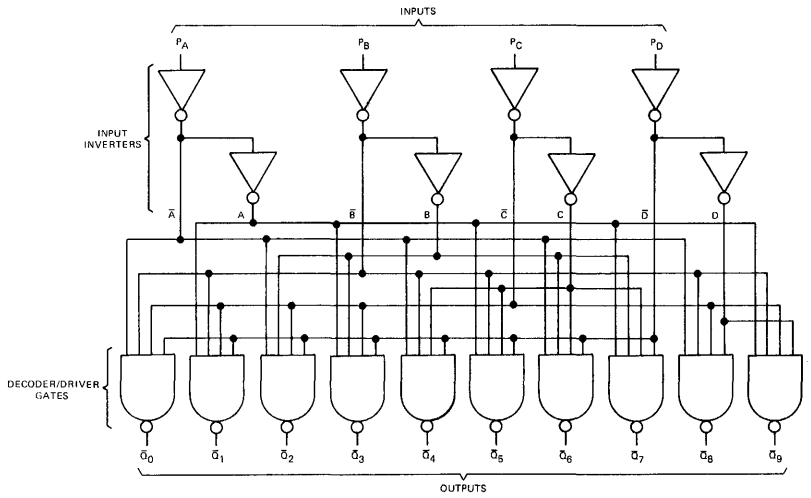
TTL/MSI 9345/5445, 7445
93145/54145, 74145
1-OF-10 DECODER/DRIVER

DESCRIPTION — The 9345/5445, 7445 and 93145/54145, 74145 1-of-10 Decoder/Drivers are designed to accept BCD inputs and provide appropriate outputs to drive 10 digit incandescent displays. All outputs remain off for all invalid binary input conditions. These devices are designed for use as indicator/relay drivers or as open-collector logic circuit drivers. Each of the high breakdown output transistors (9345/5445, 7445 = 30 V and 93145/54145, 74145 = 15 V) will sink up to 80 mA of current. Typical power dissipation is 215 mW.

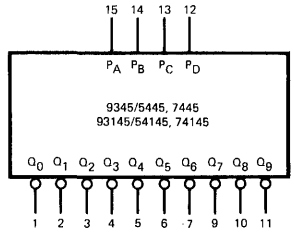
PIN NAMES		LOADING (Note a)
P_A, P_B, P_C, P_D	BCD Inputs	1 U.L.
$\overline{Q}_0$ to $\overline{Q}_9$	Outputs	(Note b)

NOTES:
a. 1 U.L. = 40 μA HIGH/1.6 mA LOW.
b. Output Characteristics.
MAX. Sinking current in LOW state 80 mA.
MIN. HIGH Voltage breakdown:
9345/5445, 7445 30 V
93145/54145, 74145 15 V

LOGIC DIAGRAM

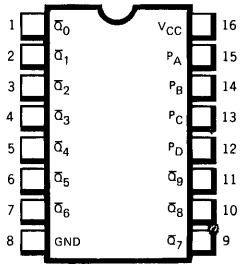


LOGIC SYMBOL

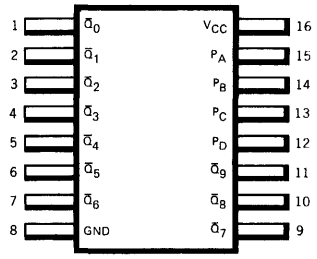


V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive Logic: See Truth Table.

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5V to +30V
Output Current (dc) (Output LOW)	+80 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9345XM/5445XM 93145XM/54145XM			9345XC/7445XC 93145XC/74145XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	-55	25	125	0	25	70	°C
PARAMETER	9345/5445, 7445			93145/54145, 74145			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Voltage on Any Output (See Note 4)			30			15	Volts

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage		1 & 2
V_{OL}	Output LOW Voltage		0.5	0.9	Volts	I_{OL} = 80 mA	V_{CC} = MIN.	1
				0.4	Volts	I_{OL} = 20 mA		
V_{OH}	Output HIGH Voltage	30			Volts	9345/5445, 7445	V_{CC} = MAX.	2
		15			Volts	93145/54145, 74145	I_{OH} = 250 μA	
I_{IH}	Input HIGH Current (Each Input)			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current (Each Input			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{CC}	Supply Current		43	62	mA	9345/5445, 93145/54145	V_{CC} = MAX.	4
			43	70	mA	9345/7445, 93145/74145		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output			50	ns	V_{CC} = 5.0 V, C_L = 5 pF, R_L = 100Ω	A
t_{PHL}	Turn On Delay Input to Output			50	ns		

NOTES:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C.
3. These voltage values are with respect to network ground terminal
4. This rating applies when the output is off.

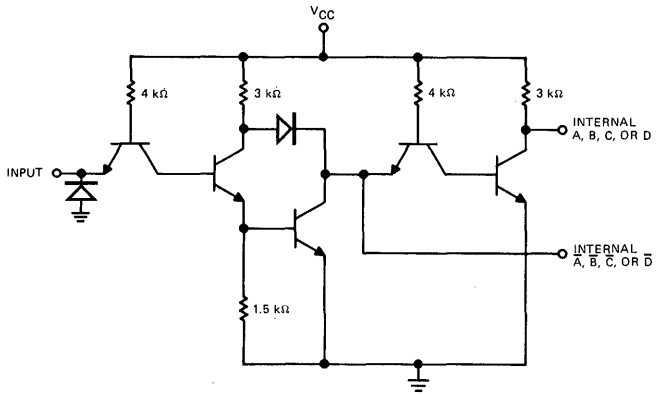
TRUTH TABLE

INPUTS				OUTPUTS									
P_D	P_C	P_B	P_A	$\overline{Q}_0$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

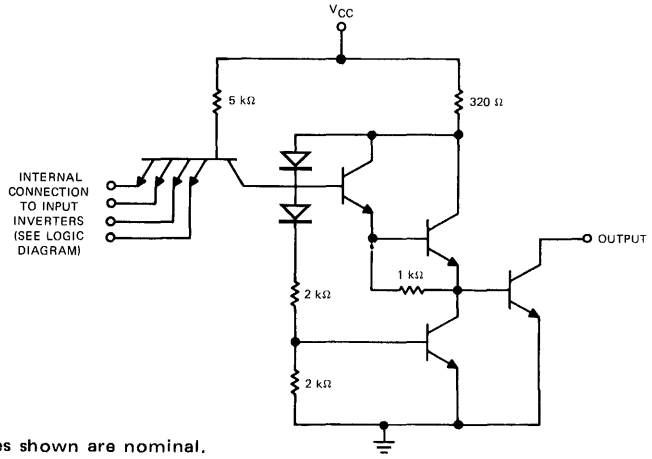
H = HIGH Voltage Level
L = LOW Voltage Level

SCHEMATIC DIAGRAMS

EACH PAIR OF INPUT INVERTERS



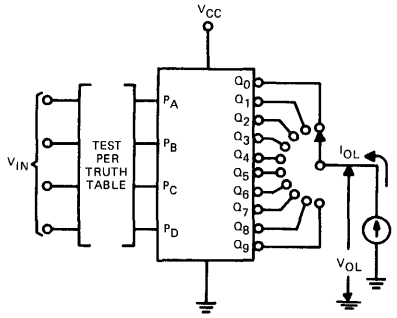
EACH DECODER/DRIVER GATE



NOTE: Component values shown are nominal.

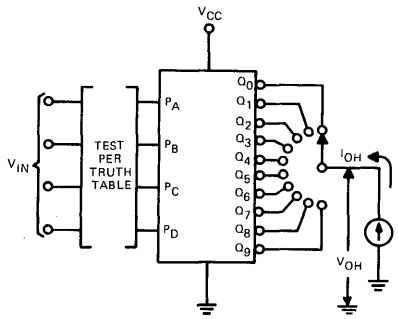
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



1. Each output is tested separately in the ON state.

Fig. 1



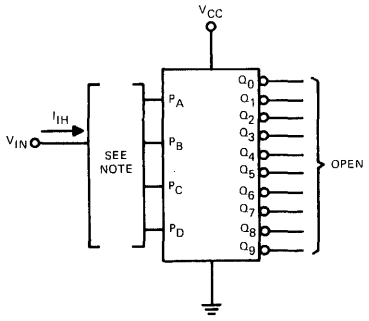
1. Each output is tested separately in the OFF state.

Fig. 2

*Arrows indicate actual direction of current flow.

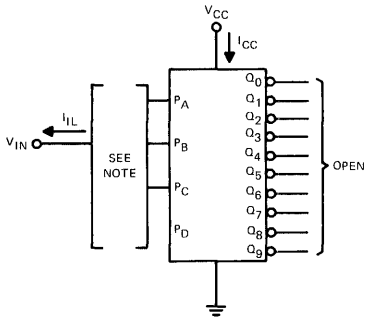
PARAMETER MEASUREMENT INFORMATION

D.C. TEST CIRCUITS* (Continued)



1. Each input is tested separately.

Fig. 3



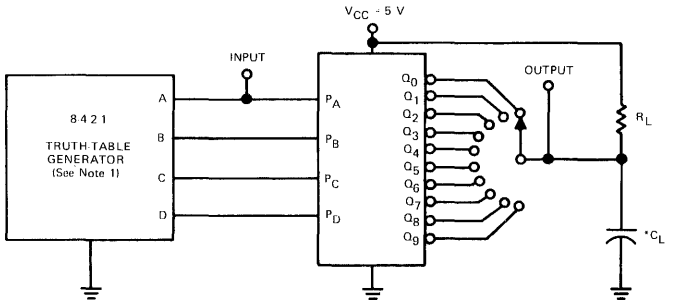
1. When testing I_{IL} each input is tested separately.
2. When testing I_{CC} all inputs are gounded and outputs are open.

Fig. 4

*Arrows indicate actual direction of current flow.

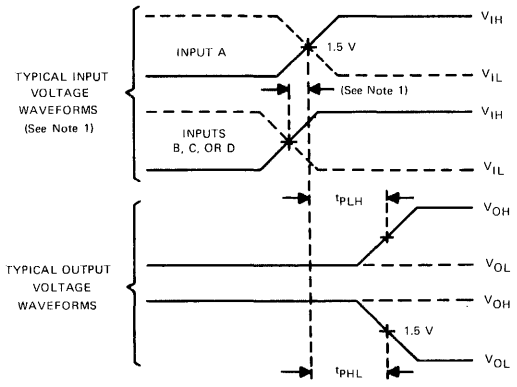
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



*Includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE:

1. The truth-table generator has the following charateristics: $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions.

Fig. A SWITCHING TIMES

TTL/MSI 9348
12-INPUT PARITY CHECKER/GENERATOR

DESCRIPTION – The TTL/MSI 9348 is a 12-Input Parity Checker/Generator generating odd and even parity outputs. It can be used in high speed error detection applications. The 9348 uses TTL technology for high capacitive drive capability, and provides low impedance in both logic states for good ac noise immunity. All inputs feature diode clamping to reduce negative line transients. This device is compatible with all members of the TTL family of digital integrated circuits.

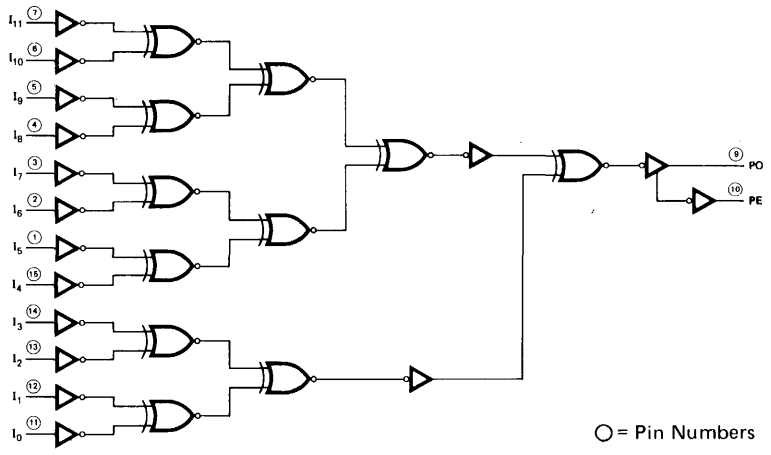
- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO 12 BITS**
- **CHECKS FOR PARITY ON UP TO 12 BITS**
- **EASILY EXPANDABLE**
- **HIGH DRIVE OUTPUT CIRCUITRY**
- **INPUT CLAMP DIODE LIMITS HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**

PIN NAMES

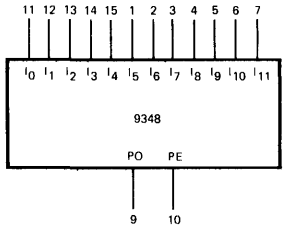
		LOADING (Note a)
I_0 to I_{11}	Parity Inputs	2 U.L.
PO	Odd Parity Output (Note b)	10 U.L.
PE	Even Parity Output (Note b)	10 U.L.

NOTES:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM

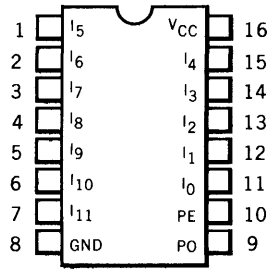


LOGIC SYMBOL

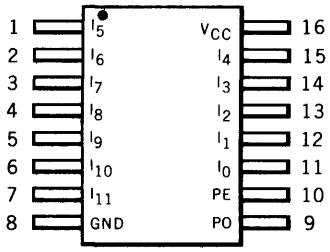


V_{CC} = Pin 16
Gnd = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The MSI 9348 is a 12-input parity generator. It provides odd and even parity for up to 12 data bits. The Even Parity output (PE) will be HIGH if an even number of logic ones are present on the inputs. The Odd Parity output (PO) will be HIGH if an odd number of logic ones are present on the inputs. The logic equations for the outputs are shown below.

$$PO = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$$

$$PE = \overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$$

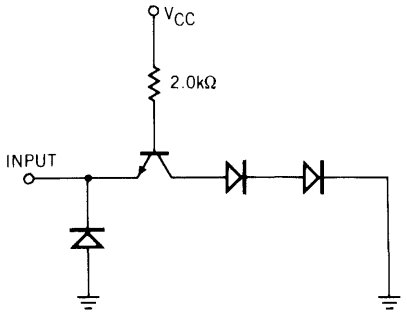
NOTE: Less through delay is encountered from the I_0, I_1, I_2, and I_3 inputs than I_4 thru I_{11} inputs. Therefore, if some signals are slower than others, the slower signals should be applied to these four inputs for maximum speed.

TRUTH TABLE

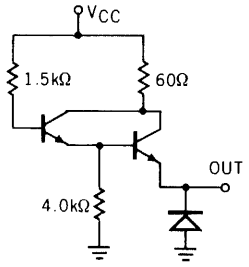
INPUTS		OUTPUTS	
$I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9, I_{10}, I_{11}$		P_O	P_E
All Twelve	Inputs LOW	0	1
Any One	Input HIGH	1	0
Any Two	Inputs HIGH	0	1
Any Three	Inputs HIGH	1	0
Any Four	Inputs HIGH	0	1
Any Five	Inputs HIGH	1	0
Any Six	Inputs HIGH	0	1
Any Seven	Inputs HIGH	1	0
Any Eight	Inputs HIGH	0	1
Any Nine	Inputs HIGH	1	0
Any Ten	Inputs HIGH	0	1
Any Eleven	Inputs HIGH	1	0
All Twelve	Inputs HIGH	0	1

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

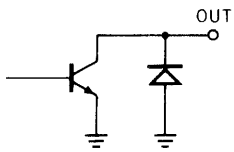
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT (Output HIGH)



OUTPUT EQUIVALENT CIRCUIT (Output LOW)



INPUT CURRENT VERSUS INPUT VOLTAGE

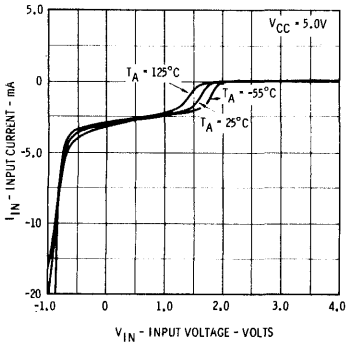


Fig. 1

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT HIGH)

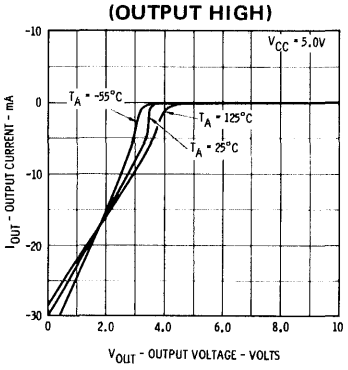


Fig. 2

OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (OUTPUT LOW)

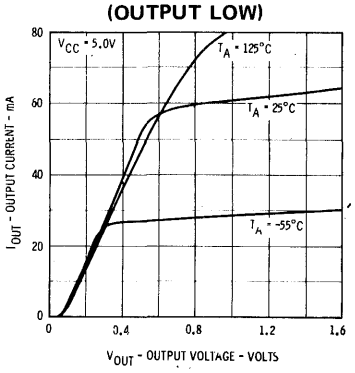


Fig. 3

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9348XM	4.5 V	5.0 V	5.5 V	–55°C to 125°C
9348XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = –800 μA V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} per Truth Table
I_{IH}	Input HIGH Current		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.0 V
I_{IL}	Input LOW Current		–1.92	–3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	–20	–50	–70	mA	V_{CC} = MAX., V_{OUT} = 0.0 V
I_{CC}	Power Supply Current		47	82	mA	V_{CC} = MAX.
V_{CD}	Input Clamp Diode Voltage			–1.5	Volts	V_{CC}=MIN., I_{IN}=–12mA, T_A=25°C

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIL LIMITS			IND LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{PLH}	Turn Off Delay Input to Output (I_4 to PO, Pin 15 to Pin 9)		40	46		40	48	ns	V_{CC} = 5.0 V, C_L = 15 pF Pins 3, 4, 13 & 14 = Gnd Others HIGH
t_{PHL}	Turn On Delay Input to Output (I_4 to PO, Pin 15 to Pin 9)		36	46		36	48	ns	
t_{PLH}	Turn Off Delay Input to Output (I_4 to PE, Pin 15 to Pin 10)		47	53		47	55	ns	
t_{PHL}	Turn On Delay Input to Output (I_4 to PE, Pin 15 to Pin 10)		41	48		41	50	ns	
t_{PLH}	Turn Off Delay Input to Output (I_3 to PO, Pin 14 to Pin 9)		20	27		20	29	ns	V_{CC} = 5.0 V, C_L = 15 pF Pins 1, 2, 4, 5, 6, 7, 11, 12, 13 & 15 = Gnd Pin 3 HIGH
t_{PHL}	Turn On Delay Input to Output (I_4 to PO, Pin 15 to Pin 9)		19	25		19	27	ns	V_{CC} = 5.0 V, C_L = 15 pF Pins 1, 2, 3, 4, 5, 6, 7, 11, 12, 13, 14 = Gnd

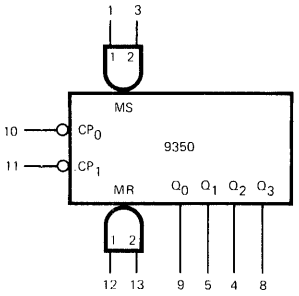
8

TTL/MSI 9350
DECADE® COUNTER

DESCRIPTION – The TTL/MSI 9350 is a Monolithic Decade Counter. This multifunctional MSI building block is capable of being used as a divide-by-two, divide-by-five or divide-by-ten counter. It is useful in a large number of counting applications in digital computer systems, data handling systems and control systems.

- **FUNCTIONALLY EQUIVALENT TO THE 7490**
- **STANDARD CORNER POWER PINS FOR EASY USE**
- **HIGH SPEED, 18 MHz TYPICAL**
- **TYPICAL POWER DISSIPATION OF 160 mW**
- **TTL COMPATIBLE**
- **ALL CERAMIC, HERMETIC 14-LEAD DUAL IN-LINE PACKAGE**
- **INPUT DIODE CLAMPING**

LOGIC SYMBOL



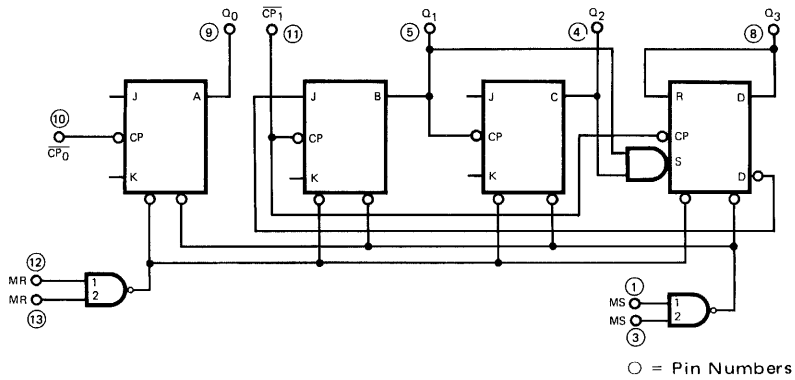
V_{CC} = Pin 14
GND = Pin 7
NC = Pins 2, 6

PIN NAMES

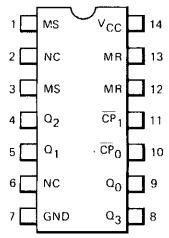
		LOADING (Note a)
$\overline{CP}_0$	Clock First Stage Negative Edge Input	2 U.L.
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input	4 U.L.
MR	"AND" Master Reset to Binary Zero (Asynchronous) Input	1 U.L.
MS	"AND" Master Set to Binary Nine (Asynchronous) Input	1 U.L.
Q_0,Q_1,Q_2,Q_3	Counter Outputs (Note b)	10 U.L.

NOTES:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NC – No internal connection

FUNCTIONAL DESCRIPTION

The 9350 is an up decade counter. It consists of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. A gated "AND" Master Reset is provided to inhibit counting and return all outputs to a LOW state. A gated "AND" Master Set is provided which will set the counter to a binary coded decimal count of nine (9), overriding all other count or reset conditions. Since the output from the first flip-flop is not internally connected to the succeeding stages, the device may be operated in three independent count modes:

A. BCD Decade Counter – The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Divide-By-Ten Counter – The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two & Divide-By-Five Counter – No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. (CP_0 as the input and Q_0 as the output.) The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_1, Q_2, and Q_3 outputs.

NOTE: The 9350 flip-flops change state after the HIGH to LOW transition of the clock.

MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X		COUNT		
X	L	X	L		COUNT		
L	X	X	L		COUNT		
X	L	L	X		COUNT		

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition

BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9350XC (IND)			UNITS
	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range	0	25	75	°C
Normalized Fan Out from Each Output, N			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9350XC*)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS & COMMENTS
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{OH}	Output HIGH Voltage	2.4	3.0		Volts	V_{CC} = 4.75 V, I_{OH} = −800 μA
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = 4.75 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current, MS, MR $\overline{CP}_0$ $\overline{CP}_1$		10 20 40	40 80 160	μA	V_{CC} = 5.25 V V_{IN} = 2.4 V
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = 5.25 V, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, MS, MR $\overline{CP}_0$ $\overline{CP}_1$		−1.0 −2.0 −4.0	−1.6 −3.2 −6.4	mA	V_{CC} = 5.25 V, V_{IN} = 0.4 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−18		−57	mA	V_{CC} = 5.25 V, V_{OUT} = 0V
I_{CC}	Power Supply Current		30	53	mA	V_{CC} = 5.25 V

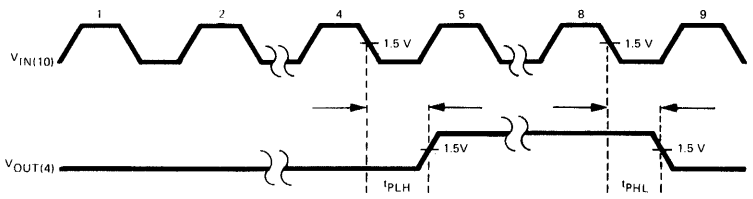
*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{PLH}	Turn-Off Delay $\overline{CP}_0$ to Output Q_2		60	100	ns	V_{CC} = 5.0 V, C_L = 15 pF Q_0 Output Connected to $\overline{CP}_1$ Input
t_{PHL}	Turn-On Delay $\overline{CP}_0$ to Output Q_2		60	100	ns	
f_{max}	Maximum Frequency of Input Count Pulses	10	18		MHz	

SWITCHING TIME WAVEFORMS



TTL/MSI 9352/5442, 7442
9353/5443, 7443 • 9354/5444, 7444
FOUR LINE TO TEN LINE DECODER (1-OF-10)

DESCRIPTION — These monolithic Decimal Decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic insures that all outputs remain off for all invalid input conditions.

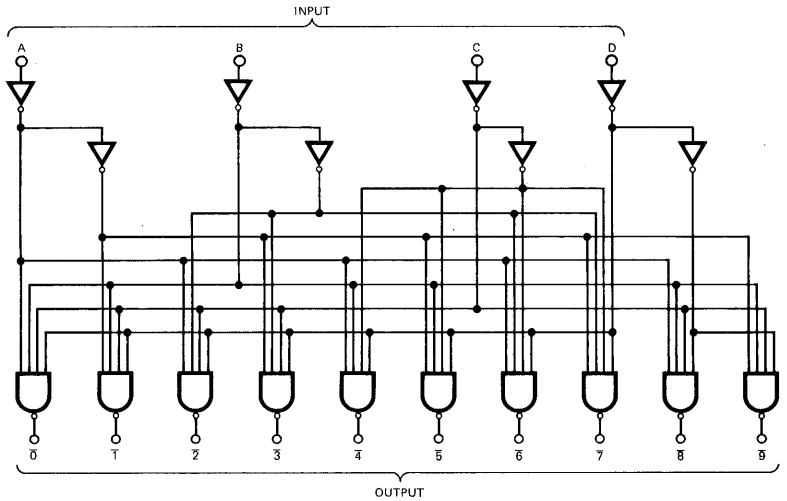
The TTL/MSI 9352/5442, 7442 BCD-to-decimal; TTL/MSI 9353/5443, 7443 excess 3-to-decimal; and TTL/MSI 9354/5444, 7444 excess 3 gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs compatible for use with other TTL and DTL circuits. The dc noise margins are typically 1.0V and power dissipation is typically 140 mW. Full fan out of 10 is available at all outputs.

PIN NAMES

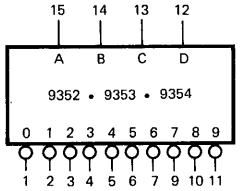
		LOADING
A, B, C, D	BCD Inputs (9352)	1 U.L.
A, B, C, D	Excess 3 Inputs (9353)	1 U.L.
A, B, C, D	Excess 3 Gray Inputs (9354)	1 U.L.
$\overline{0}$ to $\overline{9}$	Decimal Output	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM
9352/5442, 7442 BCD-TO-DECIMAL



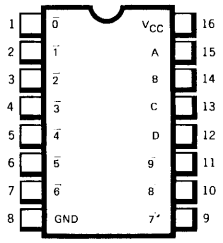
LOGIC SYMBOL



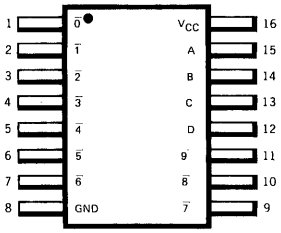
V_{CC} = Pin 16
GND = Pin 8

9352/5442, 7442
9353/5443, 7443
9354/5444, 7444

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



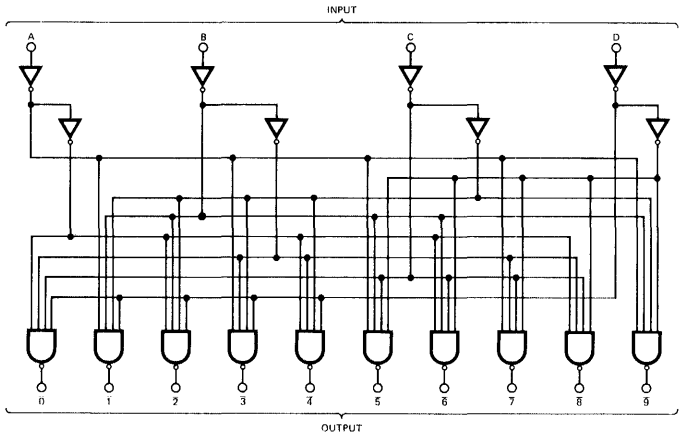
Positive logic: See truth table.

8

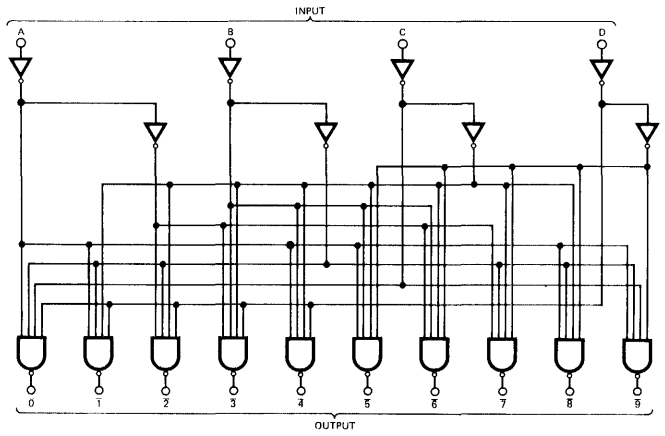
TRUTH TABLES

9352/5442, 7442 BCD INPUT				9353/5443, 7443 EXCESS 3 INPUT				9354/5444, 7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

LOGIC DIAGRAM
9353/5443, 7443 EXCESS 3-TO-DECIMAL



LOGIC DIAGRAM
9354/5444, 7444 EXCESS 3 GRAY-TO-DECIMAL



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9352XM/5442XM 9353XM/5443XM, 9354XM/5444XM			9352XC/7442XC 9353XC/7443XC, 9354XC/7444XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N			10			10	U.L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		1 & 2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	Each Input	4
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	9352/5442, 9353/5443, 9354/5444	V_{CC} = MAX.	5
		−18		−55	mA	9352/7442, 9353/7443, 9354/7444		
I_{CC}	Supply Current		28	41	mA	9352/5442, 9353/5443, 9354/5444	V_{CC} = MAX.	4
			28	56	mA	9352/7442, 9353/7443, 9354/7444		

SWITCHING CHARACTERISTICS (T_A = 25°C)

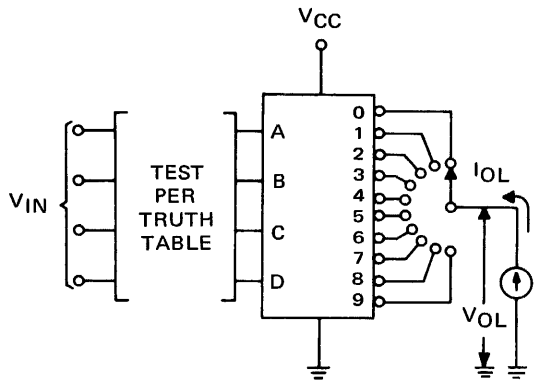
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PHL}	Turn On Delay Input to Output (Through Two Logic Levels)	10	22	30	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	A
t_{PHL}	Turn On Delay Input to Output (Through Three Logic Levels)		23	35			
t_{PLH}	Turn Off Delay Input to Output (Through Two Logic Levels)	10	17	25	ns		A
t_{PLH}	Turn Off Delay Input to Output (Through Three Logic Levels)		26	35			

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

8

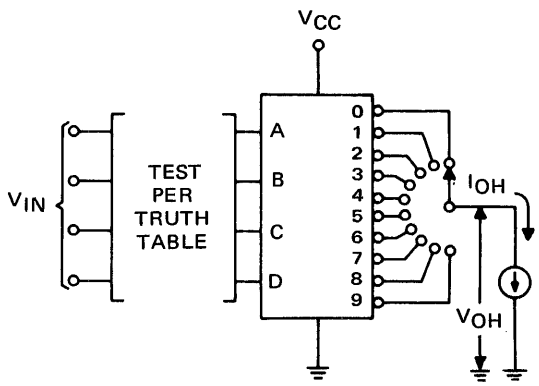
DC TEST CIRCUITS*

PARAMETER MEASUREMENT INFORMATION



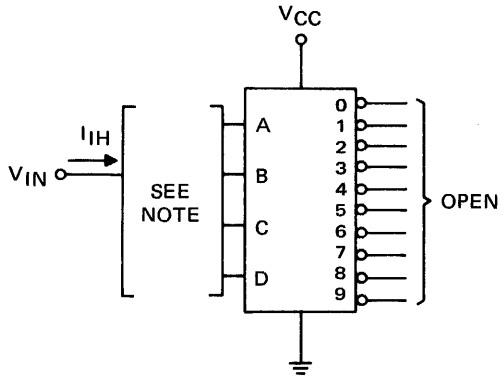
1. Each input is tested separately.

Fig. 1



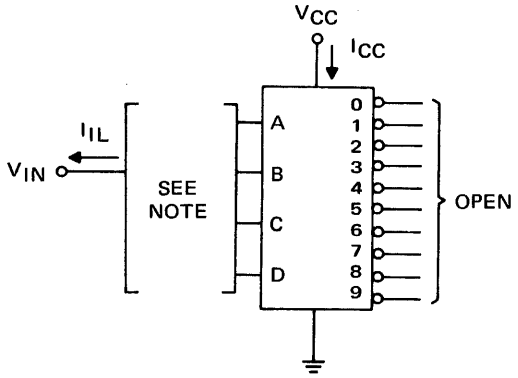
1. Each output is tested separately.

Fig. 2



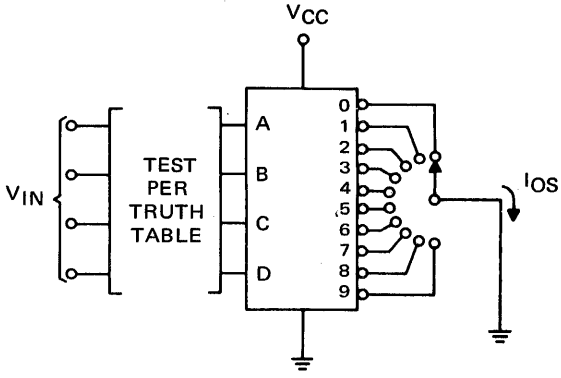
1. Each output is tested separately.

Fig. 3



1. When testing I_{IL} each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

Fig. 4



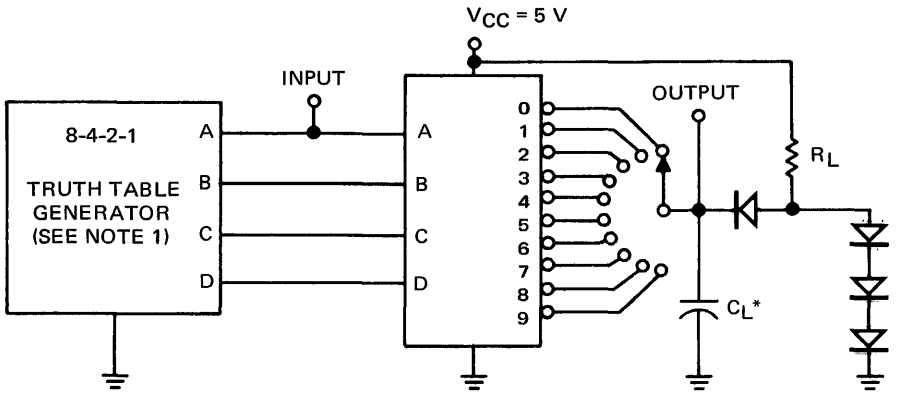
1. Each output is tested separately.

Fig. 5

*Arrows indicate actual direction of current flow.

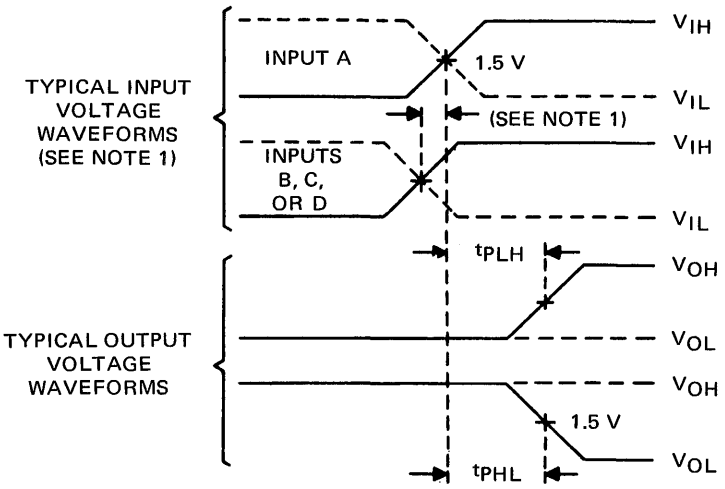
PARAMETER MEASUREMENT INFORMATION (Con't.)

SWITCHING CHARACTERISTICS



*C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE:
1. The truth table generator has the following characteristics: $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transitions.

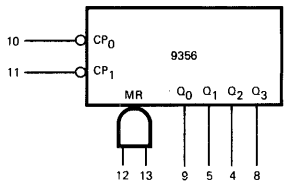
Fig. A SWITCHING TIMES

TTL/MSI 9356
4-BIT BINARY COUNTER

DESCRIPTION – The TTL/MSI 9356 is a monolithic 4-Bit Binary Counter. This device is capable of being used as a divided-by-two, divided-by-eight or a divided-by-sixteen counter. It is useful in a large number of counting applications in digital computer systems, data handling systems and control systems.

- **FUNCTIONALLY EQUIVALENT TO THE 7493**
- **STANDARD CORNER POWER PINS FOR EASY USE**
- **HIGH SPEED, 18 MHz TYPICAL**
- **TYPICAL POWER DISSIPATION OF 160 mW**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**
- **TTL COMPATIBLE**
- **ALL CERAMIC, HERMETIC 14-LEAD DUAL IN-LINE PACKAGE**

LOGIC SYMBOL

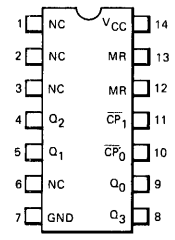


V_{CC} = Pin 14
Gnd = Pin 7
NC = Pins 1, 2, 3, 6

PIN NAMES		LOADING (Note a)
$\overline{CP}_0$	Clock First Stage Negative Edge Input	2 U.L.
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input	2 U.L.
MR	"AND" Master Reset to Binary Zero (Asynchronous) Input	1 U.L.
Q_0, Q_1, Q_2, Q_3	Counter Outputs (Note b)	10 U.L.

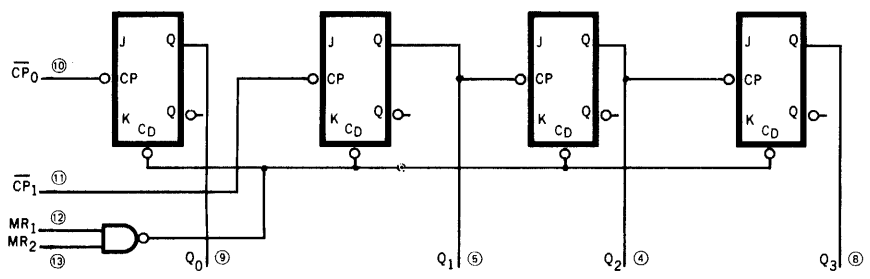
NOTES:
(a) 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
(b) 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC – No Internal Connection

LOGIC DIAGRAM



○ = Pin Numbers

FUNCTIONAL DESCRIPTION – The MSI 9356 is an 4-bit up binary counter. It consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated "AND" master reset is provided to inhibit the counting and return all outputs to a LOW state.* Since the output from the first flip-flop is not internally connected to the succeeding flip-flops, the device may be operated in two independent modes:

A. 4-Bit Ripple Counter – The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter – The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

*(i.e., When both inputs of the "AND" master reset are HIGH outputs Q_{0-3} will be forced LOW, resetting the flip-flops, regardless of all other input conditions.)

NOTE: The 9356 flip-flops change state after the HIGH to LOW transition of the clock.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition

TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	0°C to +75°C
V_{CC} Pin Potential to Ground Pin	–0.5 V to +7.0 V
*Input Voltage (dc)	–0.5 V to +5.5 V
*Input Current (dc)	–30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	–0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	LIMITS			UNITS
	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	0	25	75	°C
Normalized Fan Out from Each Output, N			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. 9356XC*)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS & COMMENTS
		MIN.	TYP. Note 4	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold for All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold for All Inputs
V_{OH}	Output HIGH Voltage	2.4	3.0		Volts	V_{CC} = 4.75 V, I_{OH} = −800 μA
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = 4.75 V, I_{OL} = 16 mA
I_{IH}	Input HIGH Current, MR		10	40	μA	V_{CC} = 5.25 V, V_{IN} = 2.4 V
	$\overline{CP}_0$, $\overline{CP}_1$		20	80		
	Input HIGH Current All Inputs			1.0	mA	V_{CC} = 5.25 V, V_{IN} = 5.5 V
I_{IL}	Input LOW Current, MR		−1.0	−1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.4 V
	$\overline{CP}_0$, $\overline{CP}_1$		−2.0	−3.2		
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−18		−57	mA	V_{CC} = 5.25 V, V_{OUT} = 0V
I_{CC}	Power Supply Current		30	53	mA	V_{CC} = 5.25 V

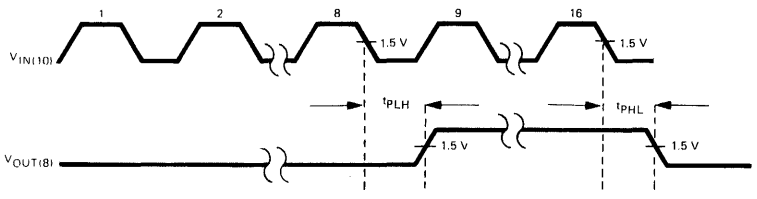
*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(1) The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
(2) Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
(3) The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating range.
(4) Typical limits are at V_{CC} = 5.0 V, 25°C, and max. loading.
(5) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{PLH}	Turn-Off Delay $\overline{CP}_0$ to Output Q_3		75	135	ns	V_{CC} = 5.0 V, C_L = 15 pF, Q_0 Output Connected To $\overline{CP}_1$ Input
t_{PHL}	Turn-On Delay $\overline{CP}_0$ to Output Q_3		75	135	ns	
f_{max}	Maximum Frequency of Input Count Pulses	10	18		MHz	

SWITCHING TIME WAVEFORMS



TTL/MSI 9357A/5446, 7446
9357B/5447, 7447
BCD TO 7-SEGMENT DECODER/DRIVER

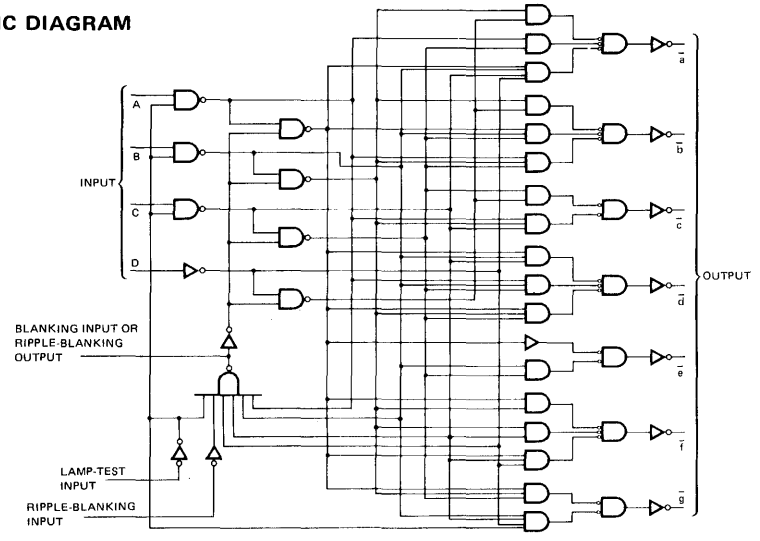
DESCRIPTION – The 9357A/5446, 7446 and 9357B/5447, 7447 are TTL, BCD to 7-segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the 9357A/5446, 7446; 9357B/5447, 7447 are designed to withstand the relatively high voltages required for 7-segment indicators. The 9357A/5446, 7446 outputs will withstand 30 V and the 9357B/5447, 7447 outputs will withstand 15 V with a maximum reverse current of 250 μA. Indicator segments requiring up to 20 mA of current may be driven directly from the 9357A/5446, 7446 or 9357B/5447, 7447 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

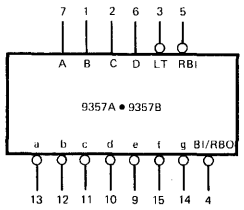
The 9357A/5446, 7446; 9357B/5447, 7447 incorporate automatic leading and/or trailing-edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) of these types may be performed at any time when the $\overline{BI/RBO}$ node is a HIGH level. Both contain an overriding blanking input ($\overline{BI}$) which can be used to control the lamp intensity or to inhibit the outputs.

PIN NAMES		LOADING
A, B, C, D	BCD Inputs	1 U.L.
$\overline{RBI}$	Ripple Blanking Input	1 U.L.
$\overline{LT}$	Lamp Test Input	1 U.L.
$\overline{BI/RBO}$	Blanking Input or	2.6 U.L.
	Ripple Blanking Output	5 U.L.
$\overline{a}$, to $\overline{g}$	Outputs	12.5 U.L.

LOGIC DIAGRAM

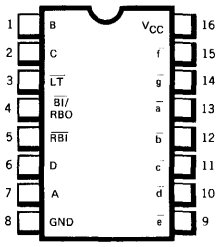


LOGIC SYMBOL

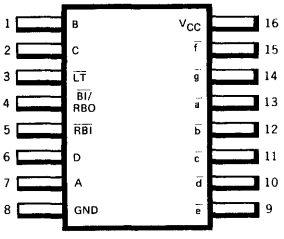


V_{CC} = Pin 16
GND = Pin 8
9357A/5446, 7446
9357B/5447, 7447

CONNECTION DIAGRAM
DIP (TOP VIEW)

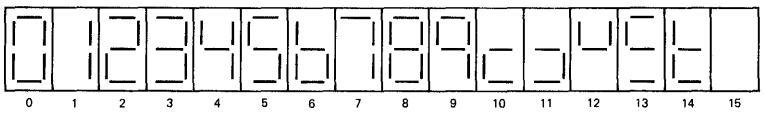


FLATPAK (TOP VIEW)



Positive logic: See truth table.

8



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE

	INPUTS							OUTPUTS							
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

NOTES:

(A) $\overline{BI/RBO}$ is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output ($\overline{RBO}$). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9357AXM/5446XM 9357BXM/5447XM			9357AXC/7446XC 9357BXC/7447XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out From Outputs $\overline{a}$ through $\overline{g}$ to Series 54/74 Loads				24			24	
Normalized Fan Out From $\overline{BI/RBO}$ Node to Series 54/74 Loads				5.0			5.0	
Output Sink Current, I_{OL}:	Outputs $\overline{a}$ through $\overline{g}$			40			40	mA
	$\overline{BI/RBO}$ Node			8.0			8.0	mA

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

PARAMETER	9357A/5446, 7446			9357B/5447, 7447			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Continuous Voltage at Outputs $\overline{a}$ through $\overline{g}$			30			15	Volts

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		1 & 2
V_{on}	On-State Output Voltage at Outputs $\overline{a}$ through $\overline{g}$		0.3	0.4	Volts	V_{CC} = MIN., I_{OL} = 40 mA		1
V_{OL}	Output LOW Voltage at $\overline{BI/RBO}$ Node		0.3	0.4	Volts	V_{CC} = MIN., I_{OL} = 8.0 mA		1
V_{off}	Off-State Output Voltage at Outputs $\overline{a}$ through $\overline{g}$	30			Volts	9357A/5446, 7446	V_{CC} = MAX., I_{off} = 250 μA	2
V_{off}	Off-State Output Voltage at Outputs $\overline{a}$ through $\overline{g}$	15			Volts	9357B/5447, 7447	V_{CC} = MAX., I_{off} = 250 μA	2
V_{OH}	Output HIGH Voltage at $\overline{BI/RBO}$ Node	2.4	3.7		Volts	V_{CC} = MIN., I_{OH} = −0.2 mA		2
I_{IL}	Input LOW Current at Any Input Except $\overline{BI/RBO}$ Node			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at $\overline{BI/RBO}$ Node			−4.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
I_{IH}	Input HIGH Current at Any Input Except $\overline{BI/RBO}$ Node			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{OS}	Output Short Circuit Current at $\overline{BI/RBO}$ Node			−4.0	mA	V_{CC} = MAX.		5
I_{CC}	Supply Current		64	85	mA	9357A/5446, 9357B/5447	V_{CC} = MAX.	4
			64	103	mA	9357A/7446, 9357B/7447		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) These voltage values are with respect to network ground terminal.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output A Input to Any Output			100	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 120Ω	A
t_{PHL}	Turn On Delay Input to Output A Input to Any Output			100	ns		A
t_{PLH}	Turn Off Delay Input to Output $\overline{RBI}$ Input to Any Output			100	ns		A
t_{PHL}	Turn On Delay Input to Output $\overline{RBI}$ Input to Any Output			100	ns		A

8

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

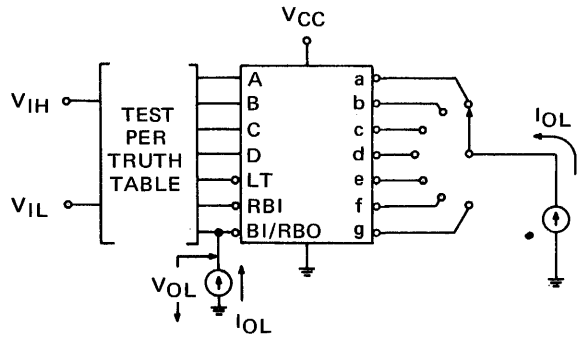


Fig. 1

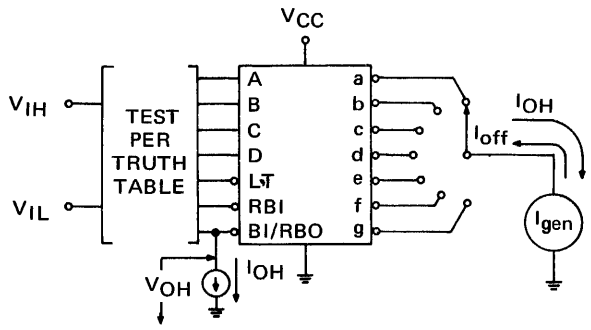
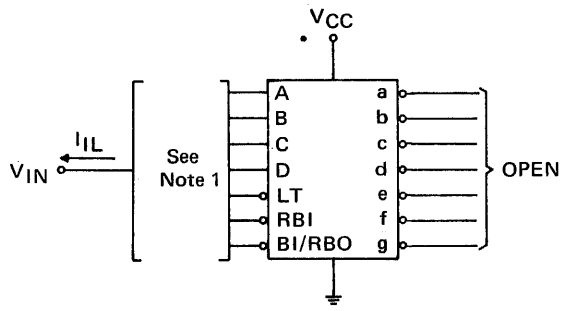
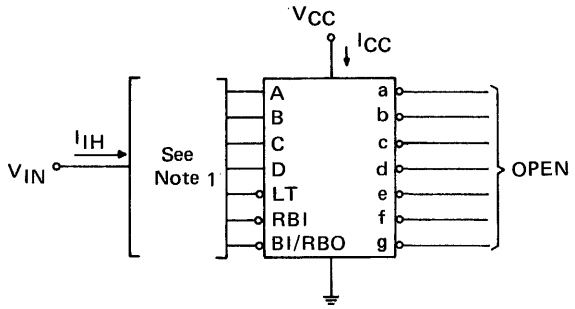


Fig. 2



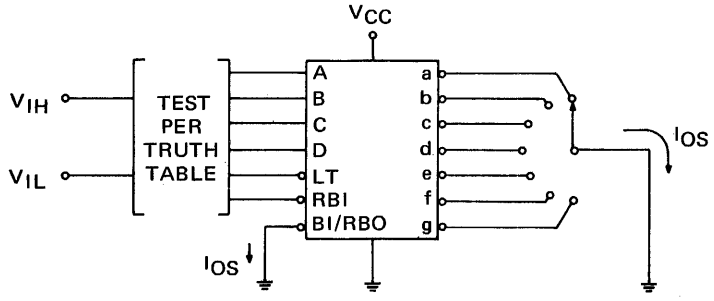
1. Each input is tested separately.

Fig. 3



1. Each input is tested separately for I_{IH}.

Fig. 4



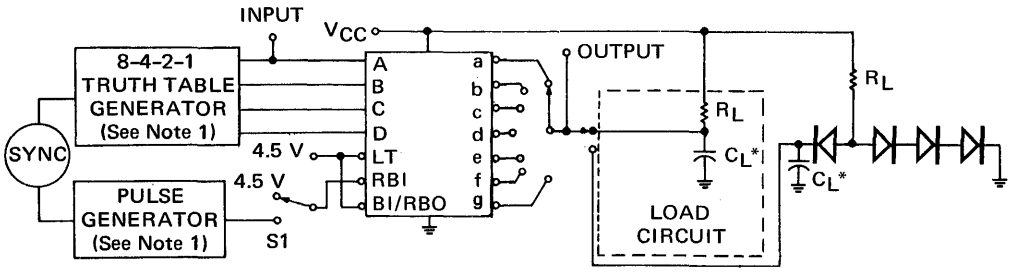
1. Each output is tested separately.

Fig. 5

*Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.

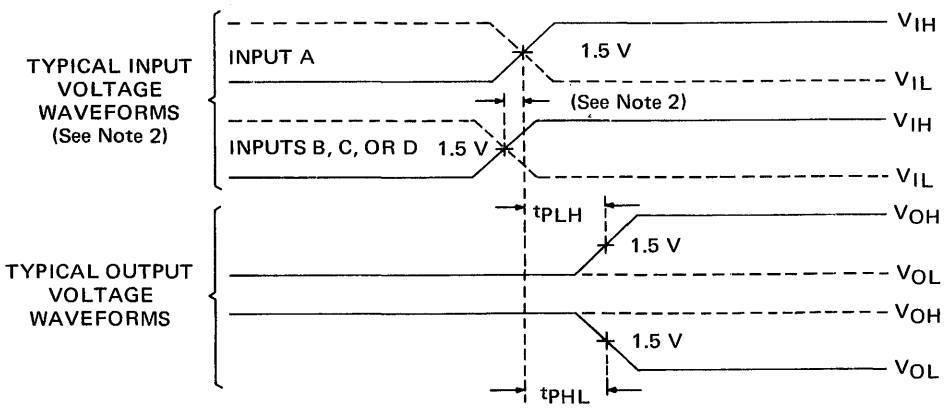
PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS

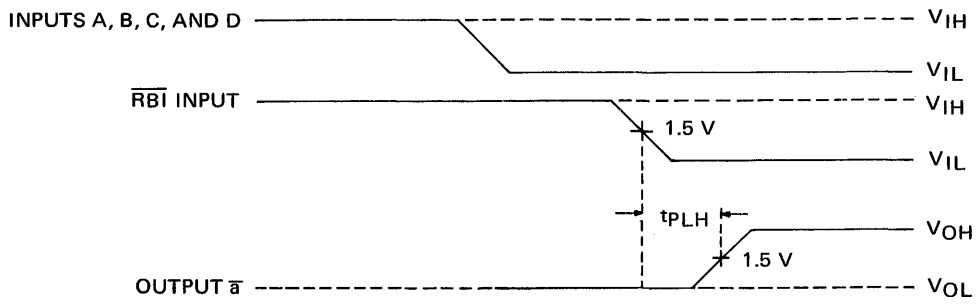


*C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS – A INPUT TO OUTPUTS



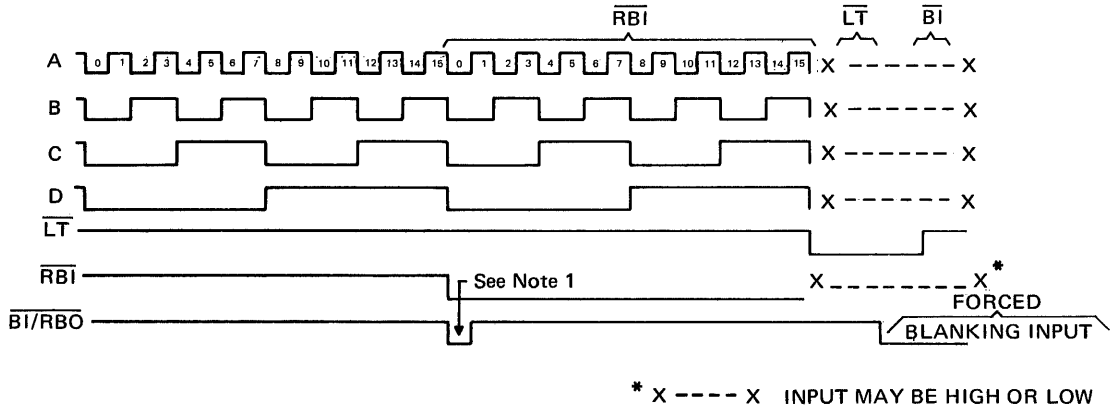
VOLTAGE WAVEFORMS – RBI INPUT TO OUTPUTS

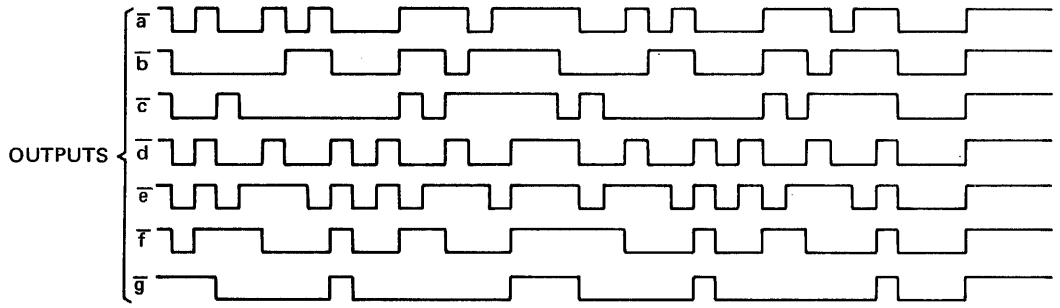
NOTES:
1. The truth table generator and pulse generator have the following characteristics: $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f \leq 10$ ns, and PRR = 1 MHz.
2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. $\overline{RBI}$ = 4.5 V.

Fig. A SWITCHING TIMES

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS

SWITCHING CHARACTERISTICS (Continued)





NOTE:
1. This LOW level represents the $\overline{RBO}$ response.

TTL/MSI 9358/5448, 7448
9359/5449, 7449
BCD TO 7-SEGMENT DECODER

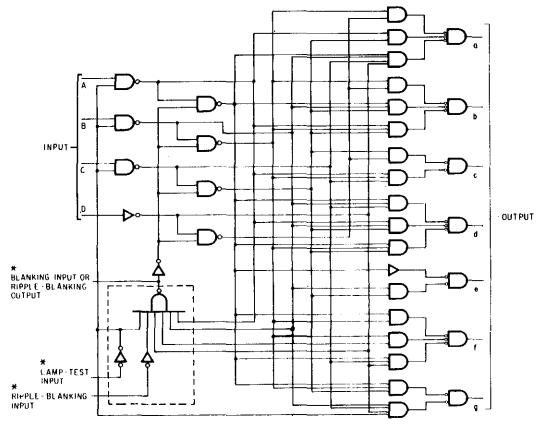
DESCRIPTION – The 9358/5448, 7448 and 9359/5449, 7449 are TTL, BCD to 7-Segment Decoders consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. The 9358/5448, 7448 offers active HIGH, open-collector outputs for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input for the 9358/5448, 7448. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the 9359/5449, 7449.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs are shown in the truth tables.

The 9358/5448, 7448 circuit incorporates automatic leading and/or trailing edge zero-blanking control ($\overline{RBI}$ and $\overline{RBO}$). Lamp test ($\overline{LT}$) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is a HIGH level. They contain an overriding blanking input ($\overline{BI}$) which can be used to control the lamp intensity or to inhibit the outputs.

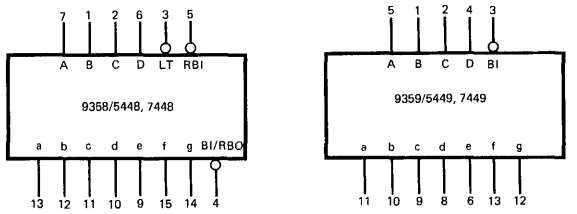
PIN NAMES		LOADING
A, B, C, D	BCD Inputs	1 U.L.
$\overline{RBI}$	Ripple Blanking Input	1 U.L.
$\overline{LT}$	Lamp Test Input	1 U.L.
$\overline{BI}/\overline{RBO}$	Blanking Input or	2.6 U.L.
	Ripple Blanking Output	5 U.L.
$\overline{BI}$	Blanking Input	1 U.L.
a to g	Outputs	6 U.L.

LOGIC DIAGRAM



* NOT INCLUDED WITH THE 9359/5449

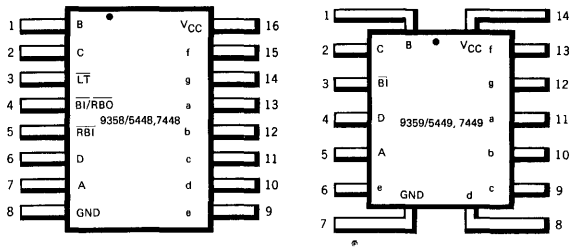
LOGIC SYMBOL



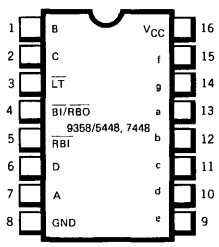
V_{CC} = Pin 16
GND = Pin 8

V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
FLATPAKS (TOP VIEW)

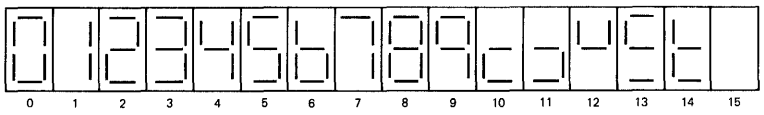


DIP (TOP VIEW)



Positive logic: See truth table

8



NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE 9358/5448, 7448

	INPUTS						OUTPUTS								
DECIMAL OR FUNCTION	$\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI/RBO}$	a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{RBI}$	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
$\overline{LT}$	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

(1) $\overline{BI/RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=input may be HIGH or LOW.

(2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

(3) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(4) When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

TRUTH TABLE 9359/5449, 7449

	INPUTS					OUTPUTS							
DECIMAL OR FUNCTION	D	C	B	A	$\overline{BI}$	a	b	c	d	e	f	g	NOTE
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	L	L	L	L	L	L	L	L	2

NOTES:

(1) The blanking input must be open or held at a HIGH level when output functions 0 through 15 are desired.

(2) When a LOW level is applied to the blanking input all segment outputs go to a LOW level regardless of the state of any other input condition. X = input may be HIGH or LOW.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9358XM/5448XM 9359XM/5449XM			9358XC/7448XC 9359XC/7449XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	–55	25	125	0	25	70	°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

PARAMETER		9358/5448, 7448			9359/5449, 7449			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Continuous Voltage at Outputs a through g							5.5	Volts
Normalized Fan Out From Outputs a through g to Series 54/74 Loads				4.0			6.0	
Normalized Fan Out From $\overline{BI}/\overline{RBO}$ Node to Series 54/74 Loads				5.0				
Output Sink Current, I_{OL}:	Outputs a through g			6.4			10	mA
	$\overline{BI}/\overline{RBO}$ Node			8.0				mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts			1 & 2
V_{IL}	Input LOW Voltage			0.6	Volts	9359/5449		1 & 2
				0.8		9358/5448, 7448; 9359/7449		
V_{on}	On-State Output Voltage		0.27	0.4	Volts	9359/5449, 7449	V_{CC} = MIN., I_{OL} = MAX.	1
V_{OL}	Output LOW Voltage		0.27	0.4	Volts	9358/5448, 7448	V_{CC} = MIN., I_{OL} = MAX.	1
V_{off}	Off-State Output Voltage	5.5			Volts	9359/5449, 7449	V_{CC} = MAX., I_{off} = 0.25 mA	2
V_{OH}	Output HIGH Voltage at $\overline{BI}/\overline{RBO}$ Node	2.4	3.7		Volts	9358/5448, 7448	V_{CC} = MIN., I_{OH} = –0.2 mA	2
	Output HIGH Voltage at Outputs a through g	2.4	4.2		Volts	9358/5448, 7448	V_{CC} = MIN., I_{OH} = –0.4 mA	2
I_{OH}	Output HIGH Current at Outputs a through g	–1.3	–2.0		mA	9358/5448, 7448	V_{CC} = MIN., V_{OUT} = 0.85 V	2
I_{IL}	Input LOW Current at Any Input Except $\overline{BI}/\overline{RBO}$ Node of 9358/5448, 7448			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at $\overline{BI}/\overline{RBO}$ Node			–4.2	mA	9358/5448, 7448	V_{CC} = MAX., V_{IN} = 0.4 V	3
I_{IH}	Input HIGH Current at Any Input			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		4
	Except $\overline{BI}/\overline{RBO}$ Node of 9358/5448, 7448			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{OS}	Output Short Circuit Current at Any Output Except Outputs a through g 9359/5449, 7449			–4.0	mA	V_{CC} = MAX.		5
I_{CC}	Supply Current		53	76	mA	9358/5448	V_{CC} = MAX.	4
			53	90	mA	9358/7448		
			33	47	mA	9359/5449		
			33	56	mA	9359/7449		

SWITCHING CHARACTERISTICS (T_A = 25°C)

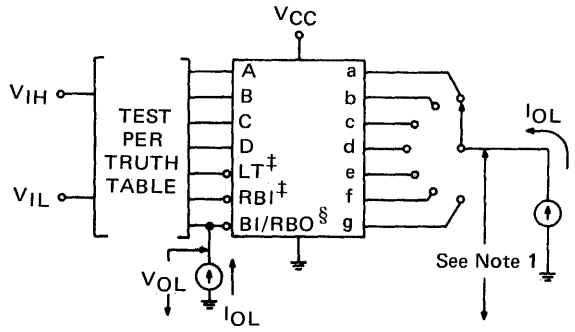
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PLH}	Turn Off Delay Input to Output A Input to Any Output			100	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L*	A
t_{PHL}	Turn On Delay Input to Output A Input to Any Output			100	ns		A
t_{PLH}	Turn Off Delay Input to Output $\overline{RBI}$ Input to Any Output			100	ns		A
t_{PHL}	Turn On Delay Input to Output $\overline{RBI}$ Input to Any Output			100	ns		A

*R_L = 1 kΩ for 9358/5448 and 9359/5449; R_L = 667Ω for 9358/7448 and 9359/7449.

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) These voltage values are with respect to network ground terminal.

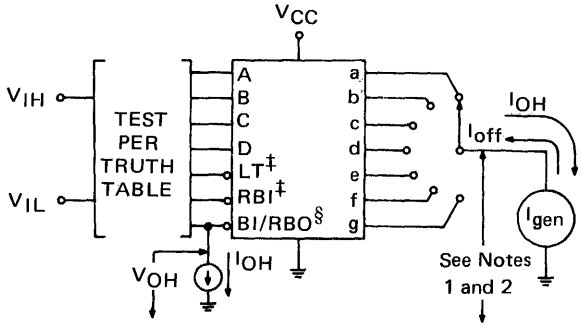
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



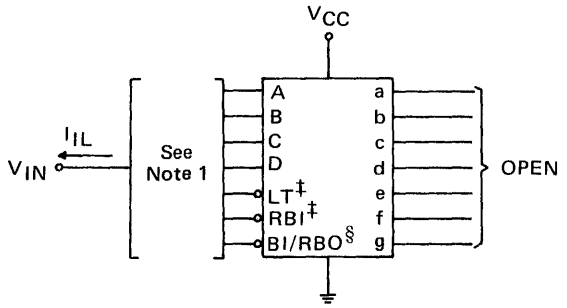
1. Measure V_{on} for 9359/5449, 7449.
   Measure V_{OL} for 9358/5448, 7448.

Fig. 1



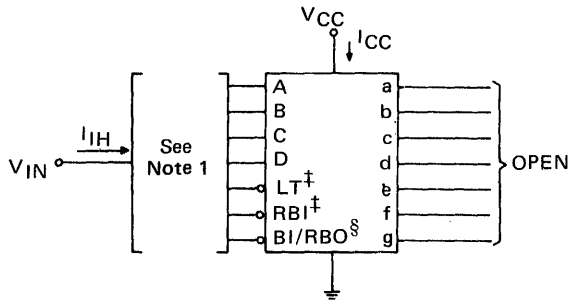
1. Measure V_{off} for 9359/5449, 7449.
2. Measure V_{OH} for 9358/5448, 7448.

Fig. 2



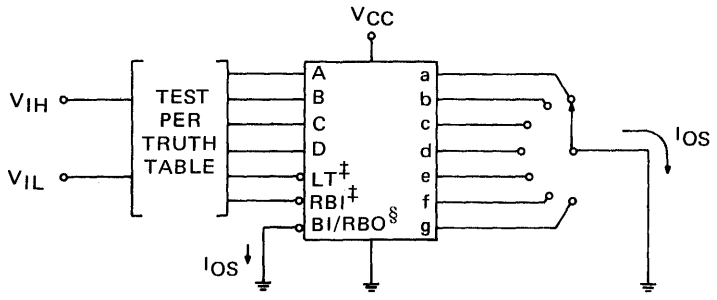
1. Each input is tested separately.

Fig. 3



1. Each input is tested separately for I_{IH}.

Fig. 4



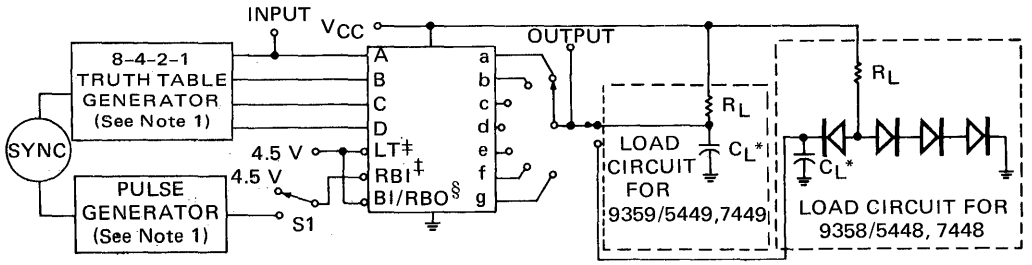
1. Each output is tested separately.

Fig. 5

*Arrows indicate actual direction of current flow. Logic symbol used is representative for all types.
‡Available on 9358/5448, 7448 only.
§BI is available on all types. RBO node is available on 9358/5448, 7448 only.

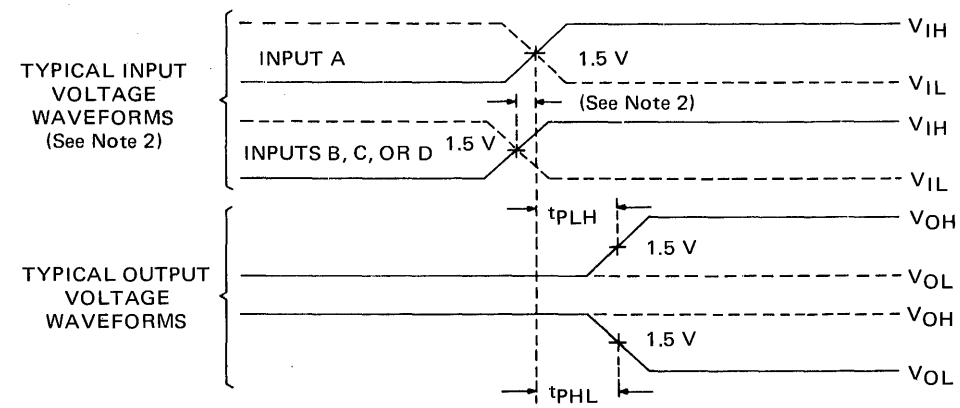
PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS

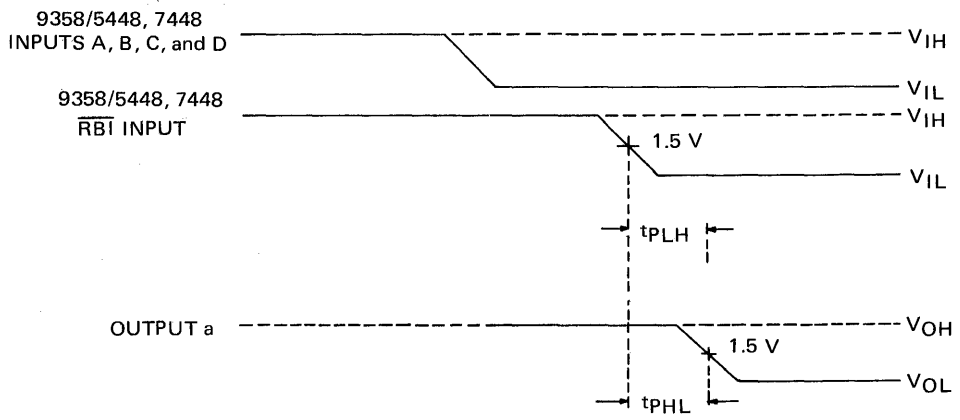


TEST CIRCUIT

*C_L includes probe and jig capacitance.



VOLTAGE WAVEFORMS – A INPUT TO OUTPUTS



VOLTAGE WAVEFORMS – RBI INPUT TO OUTPUTS

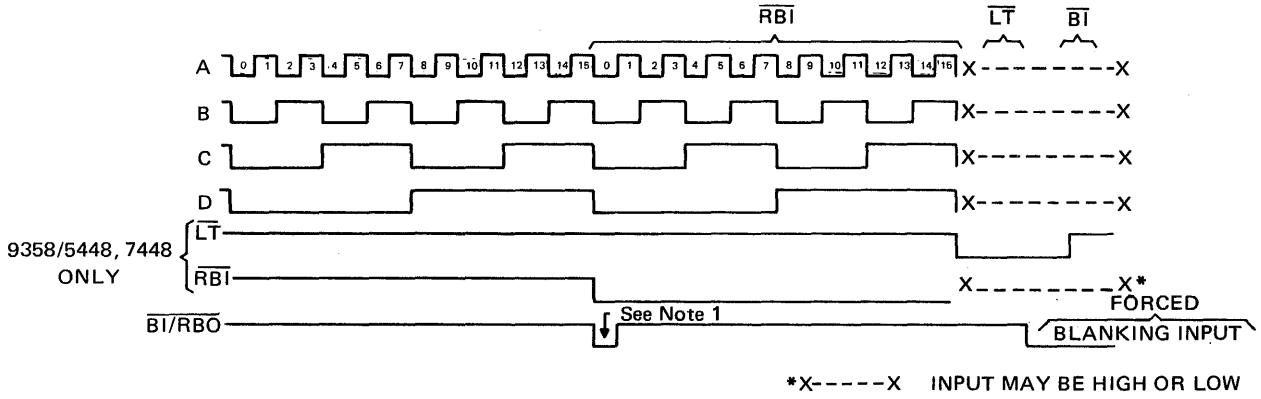
NOTES:
1. The truth table generator and pulse generator have the following characteristics: $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f \leq 10$ ns, and PRR = 1 MHz.
2. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI = 4.5 V.

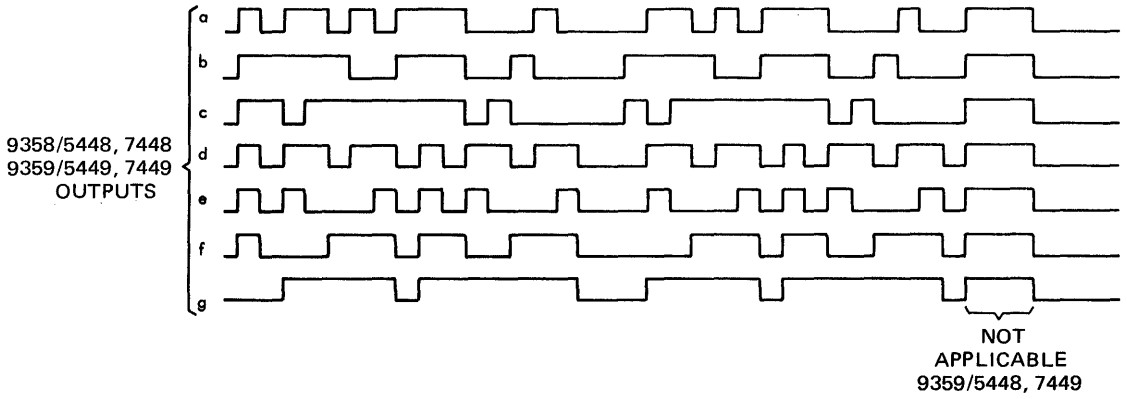
‡Available on 9358/5448, 7448 only.
§$\overline{BI}$ is available on all types. $\overline{RBO}$ node is available on 9358/5448, 7448 only.

Fig. A SWITCHING TIMES

TYPICAL INPUT/OUTPUT VOLTAGE WAVEFORMS

SWITCHING CHARACTERISTICS (Continued)





NOTE:

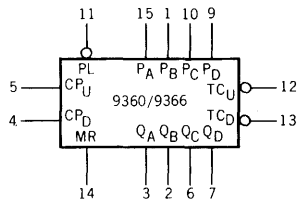
1. For the 9358/5448, 7448 this LOW level represents the $\overline{RBO}$ response. For the 9359/5449, 7449 a LOW level pulse is applied to the blanking input.

TTL/MSI 9360/54192, 74192
9366/54193, 74193
UP/DOWN DECADE AND BINARY COUNTERS

DESCRIPTION – The TTL/MSI 9360/54192, 74192 is a synchronous Up/Down BCD Decade Counter, and the TTL/MSI 9366/54193, 74193 is a synchronous Up/Down 4-Bit Binary Counter. Both counters have separate up/down clocks, parallel load facility, terminal count outputs for multidecade operation and an asynchronous overriding master reset. The circuits use TTL technology for high speed, and are compatible with the entire Fairchild TTL family.

- **SYNCHRONOUS OPERATION**
- **CASCADING CIRCUITRY INTERNALLY PROVIDED**
- **PARALLEL LOAD FACILITY**
- **ASYNCHRONOUS MASTER RESET**
- **30MHz TYPICAL COUNT FREQUENCY**
- **TYPICAL POWER DISSIPATION OF 300mW**
- **INPUT CLAMP DIODES**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE PACKAGE**
- **TTL COMPATIBLE**

LOGIC SYMBOL

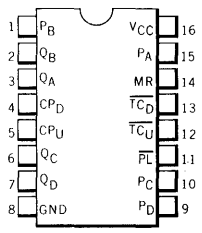


9360/54192, 74192 & 9366/54193, 74193

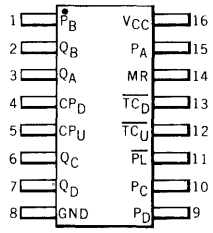
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
(TOP VIEWS)

DIP



FLATPAK

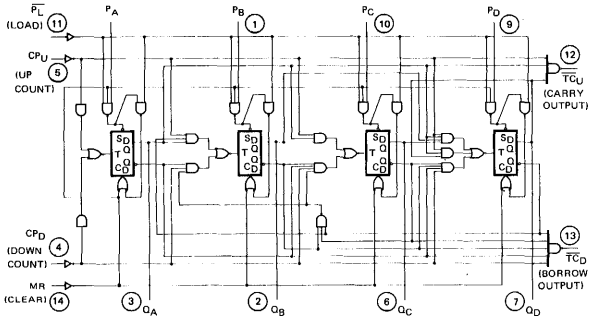


PIN NAMES		LOADING
$\overline{PL}$	Parallel Load (Active LOW) Input	1 U.L.
P_A, P_B, P_C, P_D	Parallel Data Inputs	1 U.L.
CP_U	Count Up Clock Pulse Input	1 U.L.
CP_D	Count Down Clock Pulse Input	1 U.L.
MR	Master Reset (Clear) Input (Asynchronous)	1 U.L.
Q_A, Q_B, Q_C, Q_D	Counter Outputs	10 U.L.
$\overline{TC_U}$	Terminal Count Up (Carry) Output	10 U.L.
$\overline{TC_D}$	Terminal Count Down (Borrow) Output	10 U.L.

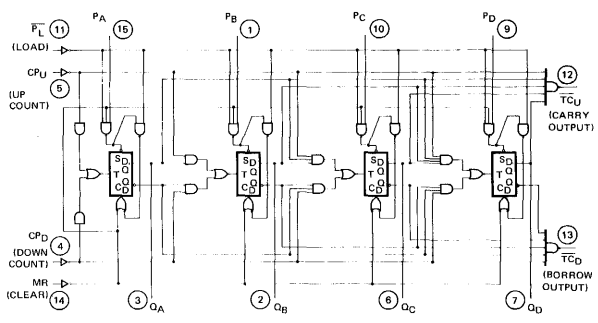
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAMS

9360/54192, 74192



9366/54193, 74193



◯ = PIN NUMBER

8

FUNCTIONAL DESCRIPTION – The 9360/54192, 74192 and 9366/54193, 74193 can be reset, preset and count up or down. These operating modes of the 9360/54192, 74192 and 9366/54193, 74193 are tabulated in Mode Selection table. The operating modes of the 9360/54192, 74192 and 9366/54193, 74193 are identical; the only difference between the devices is the count sequences.

Counting is synchronous, with the outputs changing state after the LOW to HIGH transition of either the Count-Up Clock (CP_U) or Count-Down Clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is HIGH. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are LOW simultaneously.) Both counters will respond to a clock pulse on either input by changing to the next appropriate state of the count sequence. (The state diagram for the 9360/54192, 74192 shows the regular sequence and in addition shows the sequence of states if a code greater than nine is present in the counter.

Both the 9360/54192, 74192 and the 9366/54193, 74193 have a parallel load (asynchronous) facility which permits the counter to be preset. Whenever the parallel load ($\overline{PL}$) input is LOW, and Master Reset is LOW, the information present on the Parallel Data inputs (P_A, P_B, P_C, P_D) will be loaded into the counters and appear on the outputs independent of the conditions of the clock inputs. When the Parallel Load Input goes HIGH this information is stored in the counters and when the counters are clocked they change to the next appropriate state in the count sequence. The Parallel Data inputs are inhibited when the Parallel Load is HIGH and have no effect on the counters.

The Terminal Count-Up ($\overline{TC}_U$) and Terminal Count-Down ($\overline{TC}_D$) outputs (carry and borrow respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down clock input of the following counter.

The terminal count-up outputs for the 9360/54192, 74192 and 9366/54193, 74193 are LOW when their count-up clock inputs are LOW and the counters are in state nine and state fifteen respectively. Similarly, the terminal count-down outputs are LOW when their count-down clock inputs are LOW and both counters are in state zero. Thus, when the 9360/54192, 74192 counter is in state nine and the 9366/54193, 74193 counter is in state fifteen and both are counting up, or both counters are in state zero and counting down, a clock pulse will change the counter's state on the rising edge and simultaneously clock the following counter through the appropriate active LOW terminal count output. There are two gate delays per state when these counters are cascaded.

The asynchronous Master Reset input (MR), when HIGH, overrides all input and clears the counters. Master reset overrides parallel load so that when both are activated the counters will be reset. (Obviously, both parallel load and master reset must not be deactivated simultaneously for predictable operation).

9360/54192, 74192 LOGIC EQUATIONS FOR TERMINAL COUNT

$$TC_U = Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3 \cdot \overline{CP_U}$$

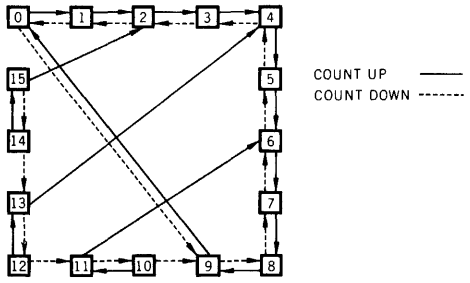
$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

9366/54193, 74193 LOGIC EQUATIONS FOR TERMINAL COUNT

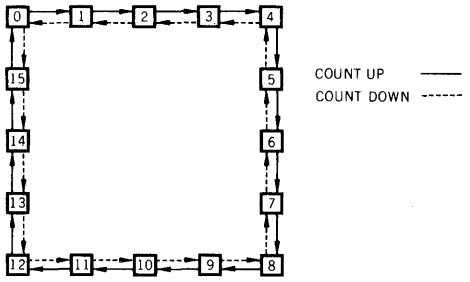
$$TC_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP_U}$$

$$TC_D = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot \overline{CP_D}$$

9360/54192, 74192 STATE DIAGRAM



9366/54193, 74193 STATE DIAGRAM



MODE SELECTION
(Both Counters)

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Preset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	CP	H	Count Up
L	H	H	CP	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care Condition
CP = Clock Pulse

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
9360XM/54192XM; 9366XM/54193XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
9360XC/74192XC; 9366XC/74193XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)
		MIN.	TYP. (Note 2)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed input HIGH Threshold voltage for all inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed input LOW Threshold voltage for all inputs
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -400μA, V_{IH} = 2.0 V, V_{IL} = 0.8V
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16mA, V_{IH} = 2.0V, V_{IL} = 0.8V
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5V
I_{IL}	Input LOW Current			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 3)	-18		-65	mA	V_{CC} = MAX.
I_{CC}	Power Supply Current		65	102	mA	V_{CC} = MAX.

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Input Count Frequency		30		MHz	V_{CC} = 5.0V, C_L = 15pF, R_L = 400Ω
t_{PLH}	Turn Off Delay, Count-Up Input (CP_U) to Carry Output ($\overline{TC_U}$)		22	26	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Turn On Delay, Count-Up Input (CP_U) to Carry Output ($\overline{TC_U}$)		18	24	ns	
t_{PLH}	Turn Off Delay, Count-Down Input (CP_D) to Borrow Output ($\overline{TC_D}$)		22	24	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Turn On Delay, Count-Down Input (CP_D) to Borrow Output ($\overline{TC_D}$)		18	24	ns	
t_{PLH}	Turn Off Delay, Either Count Input to Q Output		27	38	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω
t_{PHL}	Turn On Delay, Either Count Input to Q Output		37	47	ns	

8

TTL/MSI 93S62

9-INPUT PARITY CHECKER/GENERATOR

TO BE ANNOUNCED

DESCRIPTION — The TTL/MSI 93S63 is a very high speed 9-input parity checker/generator for use in error detection in data transmission applications. The 93S62 is implemented with Schottky barrier diode clamped TTL technology to insure high speed.

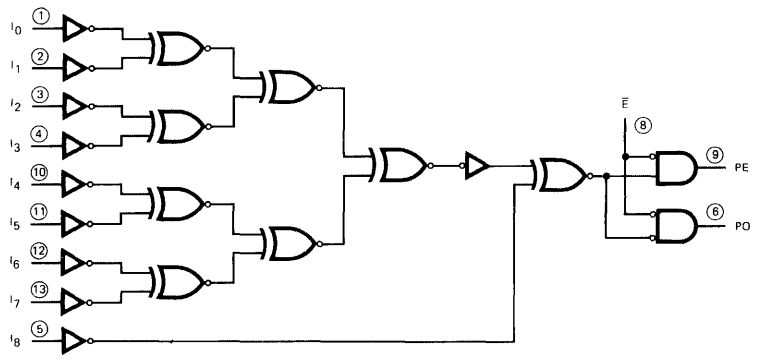
The 93S62 provides odd and even parity for up to nine data bits. The even parity output (PE) will be HIGH is an even number of logic ones are present on the inputs. The odd parity output (PO) will be HIGH if an odd number of logic ones are present. An enable input ($\overline{E}$) is provided which forces both outputs to a LOW level when the input is HIGH.

- **INPUT TO OUTPUT DELAY 16 ns**
- **OUTPUT ENABLE TERMINAL**
- **BOTH ODD AND EVEN PARITY OUTPUTS PROVIDED**
- **GENERATES A PARITY BIT FOR UP TO NINE BITS**
- **CHECKS FOR PARITY ON UP TO NINE BITS**
- **EASILY EXPANDABLE**
- **SCHOTTKY-CLAMPED TTL DESIGN**

PIN NAMES

I_0 to I_8	Data Inputs
$\overline{E}$	Output Enable
PO	Odd parity output
PE	Even parity output

LOGIC DIAGRAM

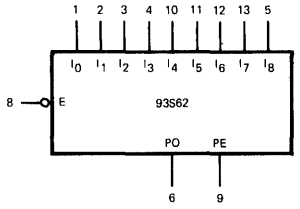


$PO = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8$

$PE = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8$

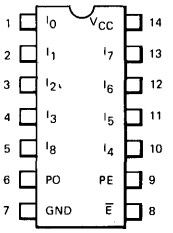
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = PIN 14
GND = PIN 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



TTL/MSI 93H72

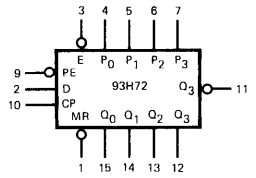
HIGH SPEED 4-BIT SHIFT REGISTER WITH ENABLE

DESCRIPTION — The 93H72 High Speed MSI 4-Bit Shift Register is a multifunctional sequential logic block which is useful in a wide variety of register applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial and parallel-parallel data transfers. The circuit is compatible with all Fairchild 9300 MSI/TTL Integrated circuits.

The 93H72 has three synchronous modes of operation: shift, parallel load and hold (do nothing). The hold capability permits information storage in the register independent of the clock.

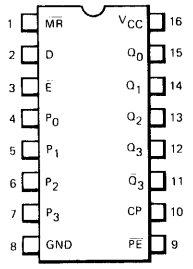
- **60 MHz TYPICAL SHIFT FREQUENCY**
- **SYNCHRONOUS PARALLEL ENTRY**
- **DATA HOLD (DO NOTHING) INDEPENDENT OF CLOCK**
- **FULLY SYNCHRONOUS WITH EDGE TRIGGERED TYPE CHARACTERISTICS ON INPUTS (EXCEPT $\overline{MR}$)**
- **ASYNCHRONOUS MASTER RESET**
- **TYPICAL POWER DISSIPATION OF 475 mW**
- **TTL COMPATIBLE**
- **ALL CERAMIC "HERMETIC" 16-LEAD DUAL IN-LINE AND FLAT PACKAGES**
- **INPUT CLAMP DIODES**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)

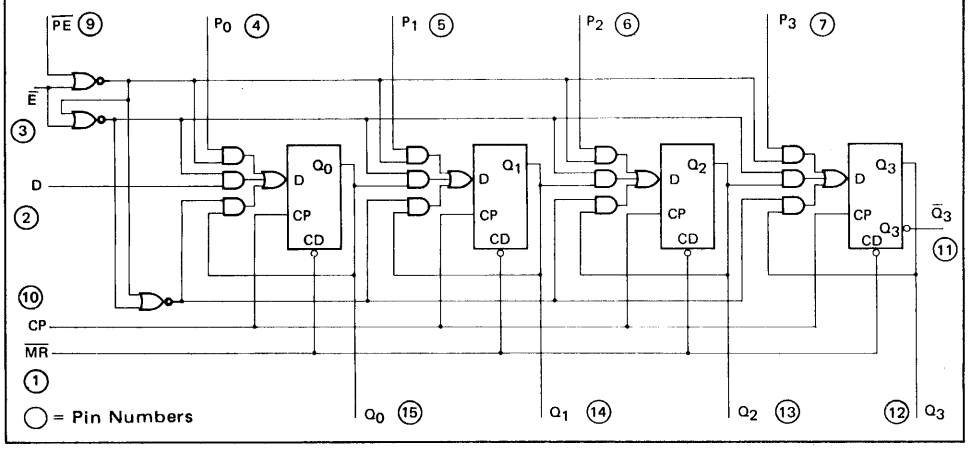


PIN NAMES

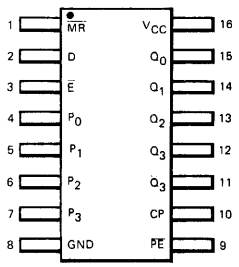
		LOADING (Note a)
$\overline{E}$	Active LOW Enable Input	2 U.L.
$\overline{PE}$	Active LOW Parallel Enable Input	1 U.L.
P_0, P_1, P_2, P_3	Parallel Data Inputs	1 U.L.
CP	Clock Input	2 U.L.
$\overline{MR}$	Active LOW Master Reset Input	1 U.L.
Q_0 to Q_3	Parallel Outputs (Note b)	10 U.L.
$\overline{Q}_3$	Last Stage Complementary Output (Note b)	10 U.L.
D	Serial Data Input	1 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. 10 U.L. is the output LOW drive factor and 20 U.L. is the output HIGH drive factor.

LOGIC DIAGRAM



FLATPAK (TOP VIEW)



8

FUNCTIONAL DESCRIPTION – The 93H72 is a 4-bit shift register with three modes of operation: shift, parallel load and hold (do nothing). The register is fully synchronous with any output change occuring after the rising clock edge. The 93H72 features edge triggered type characteristics on all inputs (except $\overline{MR}$) which means there are no restrictions on the activity of these inputs ($\overline{PE}$, $\overline{E}$, P_0, P_1, P_2, P_3, D) for logic operation except for the set up requirements prior to the LOW to HIGH clock transition.

The mode of operation of the 93H72 is determined by the two inputs, parallel enable ($\overline{PE}$) and enable ($\overline{E}$) as shown in Table I. The active LOW enable when HIGH, places the register in the hold mode with the register flip-flops retaining their information. When the enable is activated (LOW) the parallel enable ($\overline{PE}$) determines whether the register operates in a shift or parallel data entry mode.

When the enable is LOW and the parallel enable input is LOW the parallel inputs are selected and will determine the next condition of the register synchronously with the clock as shown in Table II. In this mode the element appears as four common clocked D flip-flops. With $\overline{E}$ LOW and the $\overline{PE}$ input HIGH the device acts as a 4-bit shift register with serial data entry through the D input shown in Table III. In both cases the next state of the flip-flops occurs after the LOW to HIGH transition of the clock input.

The asynchronous active LOW master reset overrides all inputs and clears the register forcing outputs Q_{0-3} LOW and $\overline{Q}_3$ HIGH.

To provide for left shift operation, P_3 is used as the serial data input and Q_0 is the serial data output. The other outputs are tied back to the previous parallel inputs, with Q_3 tied to P_2, Q_2 tied to P_1 and Q_1 tied to P_0.

TABLE I. MODE SELECTION

MODE		$\overline{MR}$	$\overline{E}$	$\overline{PE}$	P_0	P_1	P_2	P_3	D
Synchronous	Parallel Load	H	L	L	Parallel Data Entry				X
	Serial Shift	H	L	H	X	X	X	X	Serial Data Entry
	Hold	H	H	L	X	X	X	X	X
	Hold	H	H	H	X	X	X	X	X
Asynchronous	Reset	L	X	X	All Outputs Set LOW				

TABLE II. PARALLEL DATA ENTRY

P_0, P_1, P_2 OR P_3 INPUT AT t_n	Q at t_{n+1}
L	L
H	H

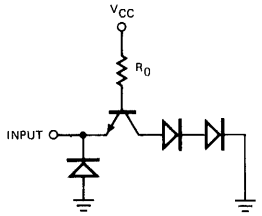
TABLE III. SERIAL DATA ENTRY

D INPUT AT t_n	Q_0 AT t_{n+1}
L	L
H	H

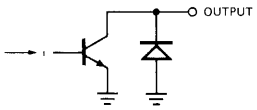
L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
t_n = Present State
t_{n+1} = State After Next Clock

TYPICAL INPUT AND OUTPUT CIRCUITS

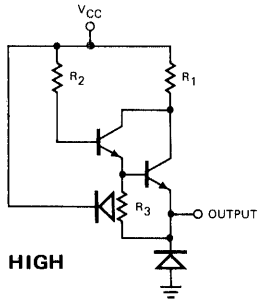
INPUTS EQUIVALENT CIRCUIT



OUTPUTS EQUIVALENT CIRCUITS

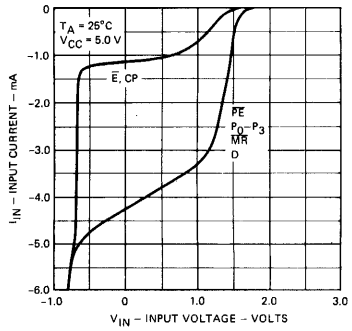


LOW

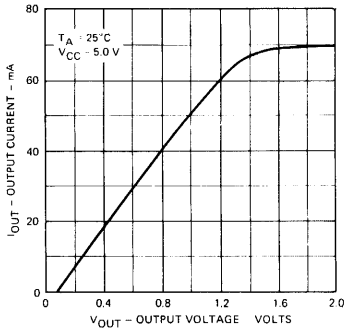


HIGH

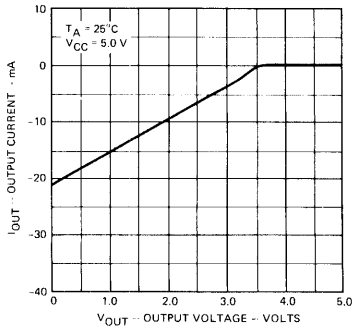
INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE LOW STATE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE HIGH STATE



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
93H72XM	4.5 V	5.0 V	5.5 V	-55°C to 125°C
93H72XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS (Over operating temperature ranges)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage For All Inputs
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold For All Inputs
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA, T_A = 25°C
V_{OH}	Output HIGH Voltage	2.4	2.7		Volts	V_{CC} = MIN., I_{OH} = -800 μA
V_{OL}	Output LOW Voltage		0.25	0.4	Volts	V_{CC} = MIN., I_{OL} = 16.0 mA
I_{IL}	Input Load Current $\overline{MR}$, D, P_0, P_1, P_2, P_3, $\overline{PE}$		-1.08	-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IL}	Input Load Current $\overline{E}$, CP		-2.16	-3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V
I_{IH}	Input Leakage Current $\overline{MR}$, D, P_0, P_1, P_2, P_3, $\overline{PE}$		10	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input Leakage Current $\overline{E}$, CP		20	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{CC}	Supply Current		95	120	mA	V_{CC} = MAX., 93H72XM
			100	135	mA	V_{CC} = MAX., 93H72XC
I_{SC}	Short-Circuit Output Current (Note 5)	30	75	100	mA	V_{CC} = MAX., V_{OUT} = 0.0V

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C and max. loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF)

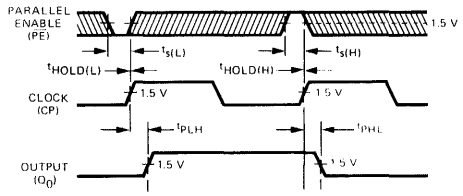
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
f_{sr}	Shift Right Frequency	45	60		MHz	
t_{PHL}	Turn On Delay from Positive Clock Edge to Any Output		14.5	21	ns	Fig. 1
t_{PLH}	Turn Off Delay from Positive Clock Edge to Any Output		10	16	ns	Fig. 1
t_{PHL} ($\overline{MR}$)	Delay from Master Reset to Any Output		19	26	ns	Fig. 4
t_s (Data)	Setup Time for Data (D, P_0, P_1, P_2, P_3)	7.0	3.5		ns	Fig. 3
t_s ($\overline{E}$)	Setup Time for Enable, $\overline{E}$ (H or L)	17	9.0		ns	Fig. 2
t_s($\overline{PE}$)	Setup Time for Parallel Enable, $\overline{PE}$	19	10		ns	Fig. 1
t_{rec}($\overline{MR}$)	Recovery Time for $\overline{MR}$	7.0	3.0		ns	Fig. 4
t_{pw} $\overline{MR}$	Required Pulse Width for $\overline{MR}$	19	11		ns	Fig. 4
t_{HOLD} (Data) ($\overline{E}$) or ($\overline{PE}$)	Hold Time for Data, $\overline{E}$, or $\overline{PE}$	0			ns	Fig. 1, 2 and 3

NOTES:
6. SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order for the register to respond.
7. HOLD TIME: t_{HOLD} is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained to insure continued recognition.
8. RECOVERY TIME FOR $\overline{MR}$: t_{rec} ($\overline{MR}$) is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order for the flip-flop(s) to respond to the clock.

SWITCHING TIME WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.

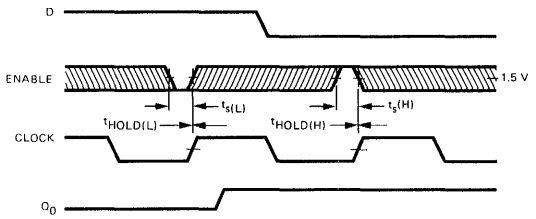
SET UP TIME (t_s) FOR PARALLEL ENABLE



Other Conditions: P_0 = H
$\overline{E}$ = L
D = L

Fig. 1

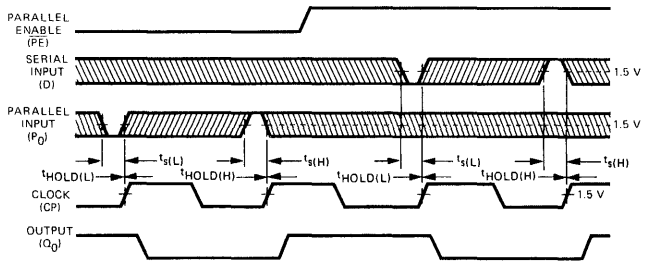
SET UP TIME (t_s) FOR ENABLE ($\overline{E}$)



Other Conditions: $\overline{PE}$ = H

Fig. 2

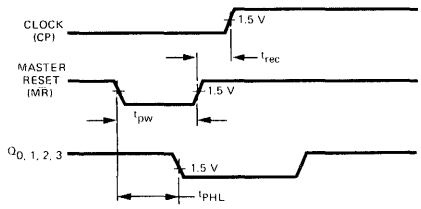
SET UP TIME (t_s) FOR DATA (D, $P_{0, 1, 2, 3}$)



Other Conditions: $\overline{E}$ = L

Fig. 3

DELAY FROM $\overline{MR}$ TO OUTPUT t_{PHL}
MASTER RESET RECOVERY TIME (t_{rec})
REQUIRED MASTER RESET PULSE WIDTH



Other Conditions: $\overline{E}$ = L, $\overline{PE}$ = L, $P_0 = P_1 = P_2 = P_3$ = H

Fig. 4

TTL/MSI 9375/5475, 7475
9377/5477, 7477
4-BIT LATCH

DESCRIPTION – The TTL/MSI 9375/5475, 7475 and 9377/5477, 7477 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is HIGH and the Q output will follow the data input as long as the clock remains HIGH. When the clock goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go HIGH.

The 9375/5475, 7475 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-lead packages. For higher component density applications the 9377/5477, 7477 4-bit latch is available in the 14-lead package with $\overline{Q}$ outputs omitted.

PIN NAMES		LOADING
D_1, D_2, D_3, D_4	Data Inputs	2 U.L.
$\overline{CP}_{1\text{-}2}$	Clock Input Latches 1 & 2	4 U.L.
$\overline{CP}_{3\text{-}4}$	Clock Input Latches 3 & 4	4 U.L.
Q_1, Q_2, Q_3, Q_4	Latch Outputs	10 U.L.
$\overline{Q}_1, \overline{Q}_2, \overline{Q}_3, \overline{Q}_4$	Complementary Latch Outputs	10 U.L.

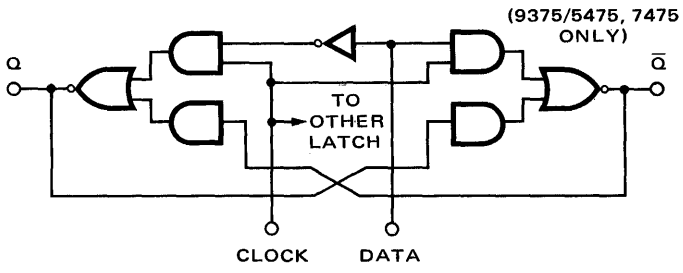
Note: 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE
(Each Latch)

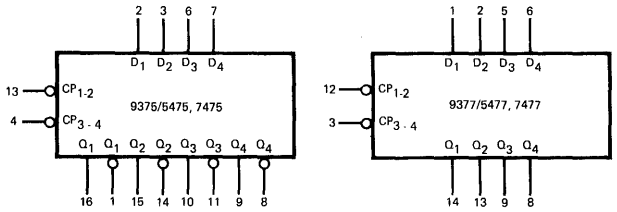
t_n	t_{n+1}
D	Q
H	H
L	L

NOTES:
t_n = bit time before clock negative-going transition.
t_{n+1} = bit time after clock negative-going transition.

LOGIC DIAGRAM
(EACH LATCH)



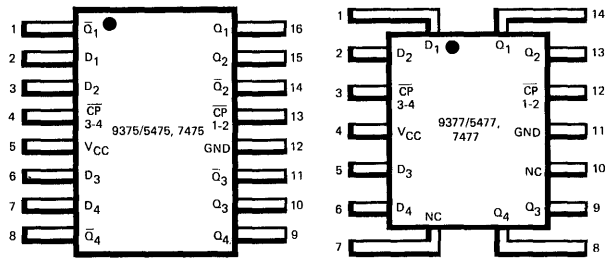
LOGIC SYMBOL



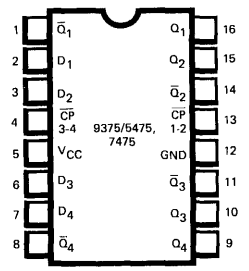
V_{CC} = Pin 5
GND = Pin 12

V_{CC} = Pin 4
GND = Pin 11
NC = Pin 7, 10

CONNECTION DIAGRAM
FLATPAKS (TOP VIEW)



DIP (TOP VIEW)



Positive logic: See truth table.
NC – No internal connection.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to + 150°C
Temperature (Ambient) Under Bias	−55°C to + 125°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0 V
*Input Voltage (dc)	−0.5V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9375XM/5475XM 9377XM/5477XM			9375XC/7475XC 9377XC/7477XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Outputs			10			10	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA		1 & 2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1 & 2
I_{IH}	Input HIGH Current at D			90	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Clock			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at D			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at Clock			−6.4	mA	V_{CC} = MAX.		3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9375/5475; 9377/5477	V_{CC} = MAX.	4
		−18		−57	mA	9375/7475; 9377/7477		
I_{CC}	Supply Current		32	46	mA	9375/5475; 9377/5477	V_{CC} = MAX.	5
			32	53	mA	9375/7475; 9377/7477		

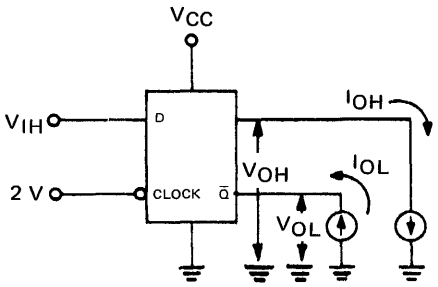
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{setupH}	At D Input		7.0	20	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	A
t_{setupL}	At D Input		14	20	ns		A
t_{holdH}	At D Input	0	15*		ns		A
t_{holdL}	At D Input	0	6.0*		ns		A
t_{PLH}	D to Q		16	30	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	A
t_{PHL}			14	25			
t_{PLH}	D to $\overline{Q}$ (9375/5475, 7475)		24	40	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	A
t_{PHL}			7.0	15			
t_{PLH}	$\overline{CP}$ to $\overline{Q}$		16	30	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	A
t_{PHL}			7.0	15			
t_{PLH}	$\overline{CP}$ to Q (9375/5475, 7475)		16	30	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	A
t_{PHL}			7.0	15			

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.
* These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5 V when data at the D input will still be recognized at stored.

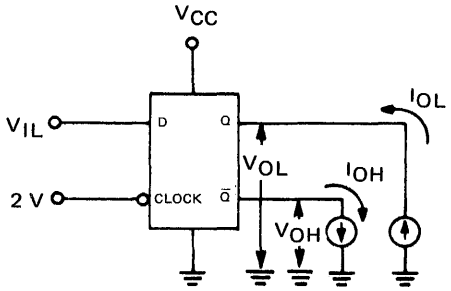
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



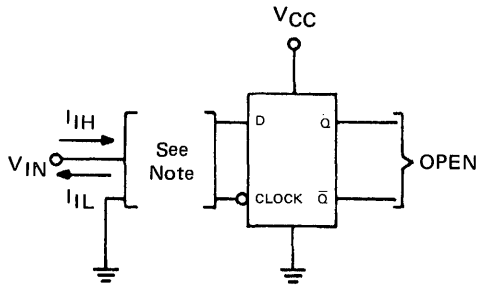
1. Each latch is tested separately.

Fig. 1



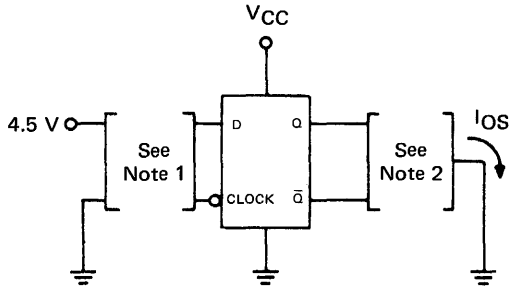
1. Each latch is tested separately.

Fig. 2



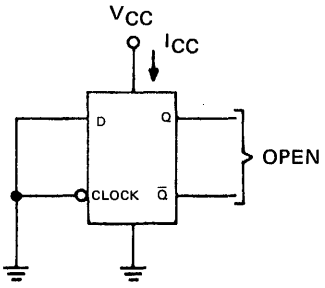
1. Each input is tested separately.
2. When testing I_{IH} at D ground clock.
3. When testing I_{IH} at clock ground all D inputs.

Fig. 3



1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

Fig. 4



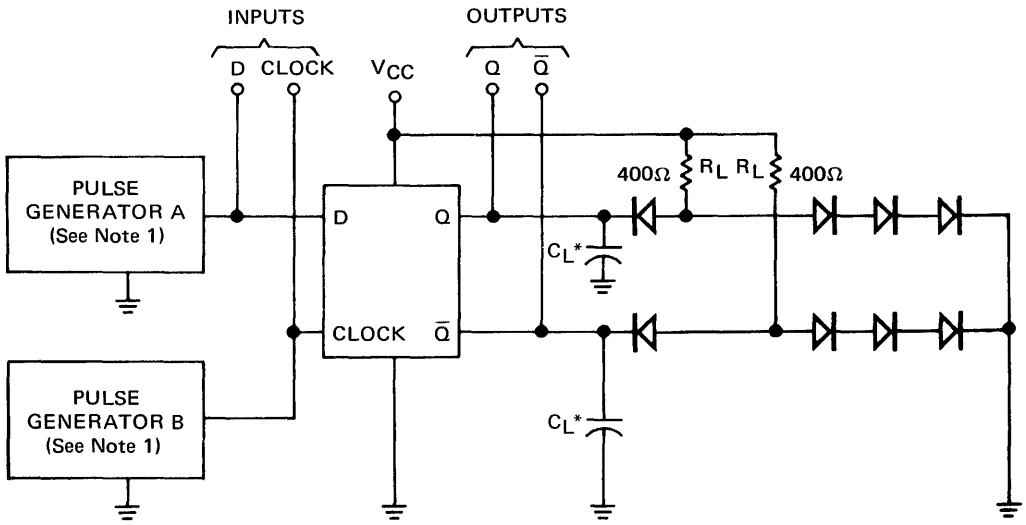
1. All latches are tested simultaneously.

Fig. 5

*Arrows indicate actual direction of current flow. Complementary $\overline{Q}$ outputs are available on the 9375/5475, 7475.

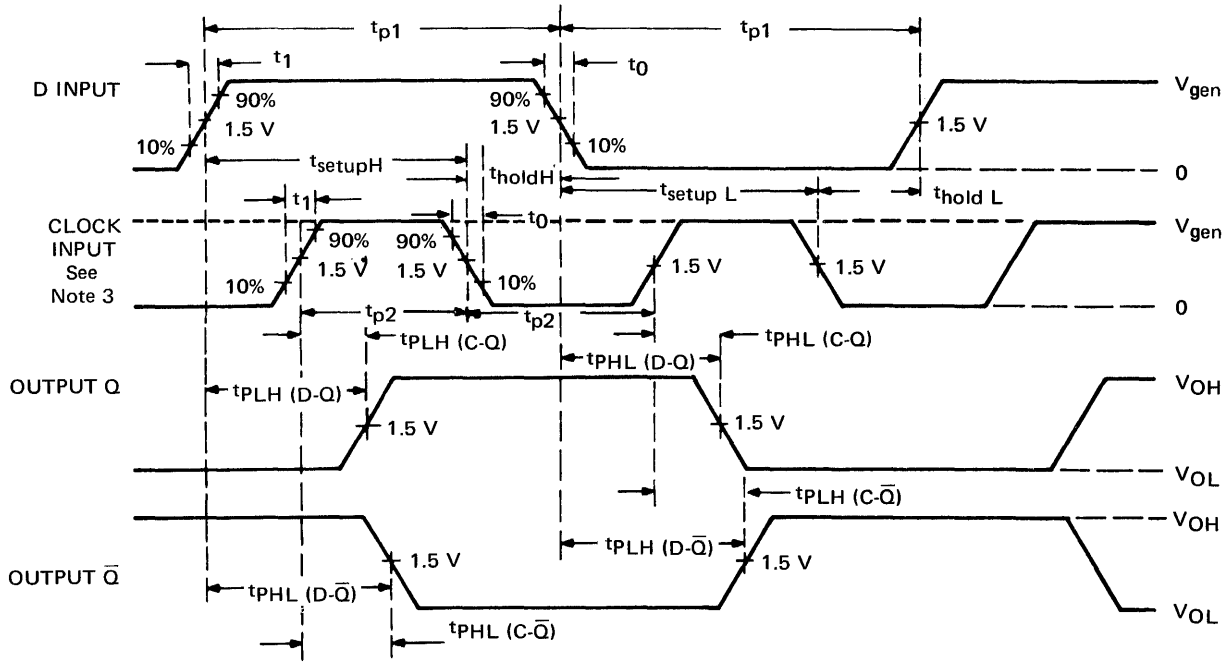
PARAMETER MEASUREMENT INFORMATION (con't)

SWITCHING CHARACTERISTICS*



*C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. When measuring t_{PLH} (D-Q) and t_{PHL} (D-Q) or t_{PHL} (D-Q) and t_{PLH} (D-$\overline{Q}$) for the 9375/5475, 7475, clock input must be held at high level.

Fig. A SWITCHING TIMES

*Complementary Q outputs are on the 9375/5475, 7475.

TTL/MSI 9380/5480, 7480
GATED FULL ADDER

DESCRIPTION – The TTL/MSI 9380/5480, 7480 is a single-bit, high speed, Binary Full Adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. It is designed for medium and high speed, multiple-bit, parallel-add/serial-carry applications. The circuit utilizes DTL for the gated inputs and high speed, high fan out TTL for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

PIN NAMES		LOADING
A_1, A_2, B_1, B_2	Non Inverting Data Inputs	1 U.L.
A^*, B^*	Inverting Data Inputs	1.65 U.L.
A_C, B_C	Control Inputs	1 U.L.
C_n	Carry Input	5 U.L.
$\overline{C_{n+1}}$	Carry Output	5 U.L.
$\Sigma, \overline{\Sigma}$	Sum Outputs	10 U.L.
A^*, B^*	When Used as Outputs	3 U.L.

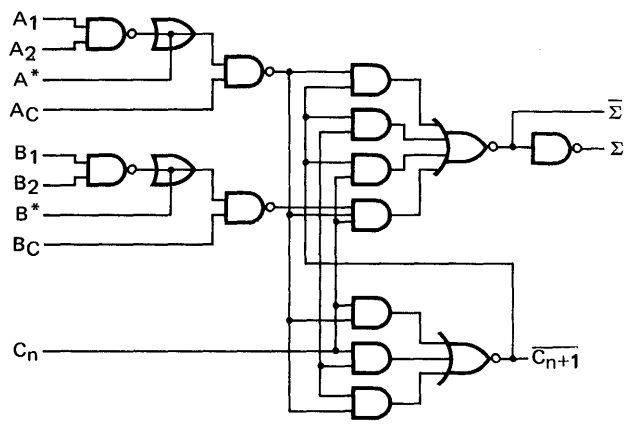
1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

TRUTH TABLE

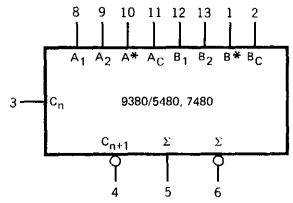
C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

NOTES:
1. $A = \overline{A^* \cdot A_C}$, $B = \overline{B^* \cdot B_C}$ where $A^* = \overline{A_1 \cdot A_2}$. $B^* = \overline{B_1 \cdot B_2}$
2. When A^* or B^* are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, A^* or B^* respectively must be open or used to perform Dot-OR logic.

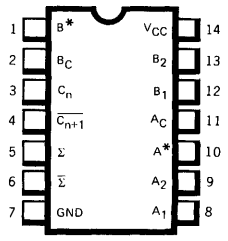
LOGIC DIAGRAM



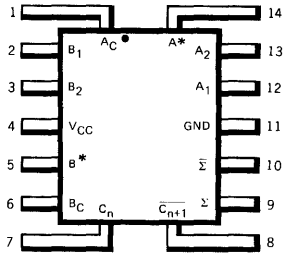
LOGIC SYMBOL



CONNECTION DIAGRAM DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic: See truth table

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9380XM/5480XM			9380XC/7480XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Outputs	$\overline{C_{n+1}}$, N			5.0			5.0	
	Σ or $\overline{\Sigma}$, N			10			10	
	A* or B*, N			3.0			3.0	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		1 & 2
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN.		2
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at A_1, A_2, B_1, B_2, A_c or B_c			15	µA	V_{CC} = MAX., V_{IN} = 2.4 V		5
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at C_n			200	µA	V_{CC} = MAX., V_{IN} = 2.4 V		6
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at A_1, A_2, B_1, B_2, A_c, or B_c			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at A* or B*			−2.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at C_n			−8.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current at Σ or $\overline{\Sigma}$ (Note 3)	−20		−57	mA	9380/5480	V_{CC} = MAX.	7
		−18		−57	mA	9380/7480		
	Output Short Circuit Current at $\overline{C_{n+1}}$ (Note 3)	−20		−70	mA	9380/5480	V_{CC} = MAX.	7
		−18		−70	mA	9380/7480		
I_{CC}	Supply Current		21	31	mA	9380/5480	V_{CC} = MAX.	8
			21	35	mA	9380/7480		

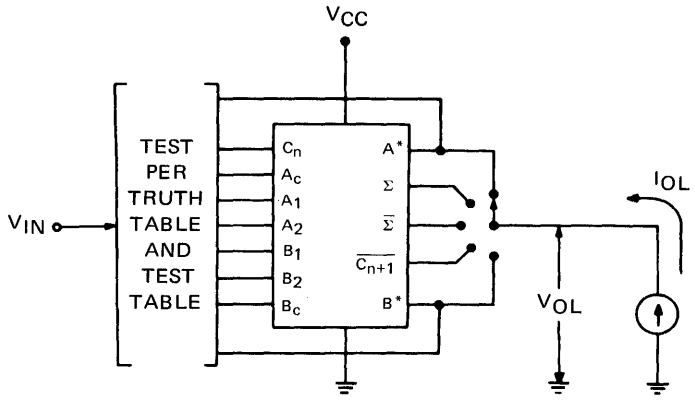
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	FIGURE A TEST NO.
t_{PLH}	(C_n to $\overline{C_{n+1}}$)		13	17	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 780Ω	1
t_{PHL}			8.0	12			2
t_{PLH}	(B_c to $\overline{C_{n+1}}$)		18	25	ns		3
t_{PHL}			38	55			4
t_{PLH}	(A_c to Σ)		52	70	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	5
t_{PHL}			62	80			6
t_{PLH}	(B_c to $\overline{\Sigma}$)		38	55	ns		7
t_{PHL}			56	75			8
t_{PLH}	(A_1 to A*)		48	65	ns	V_{CC} = 5.0 V, C_L = 15 pF	9
t_{PHL}			17	25			10
t_{PLH}	(B_1 to B*)		48	65	ns		11
t_{PHL}			17	25			12

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

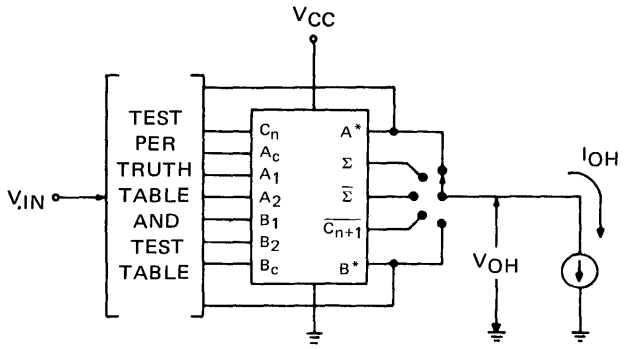


TEST TABLE

Output Under Test	I_{OL} (Min)
Σ or $\overline{\Sigma}$	16 mA
$\overline{C_{n+1}}$	8 mA
A* or B*	4.8 mA

1. Each input or output is tested separately.
2. When A* is tested A_1 and A_2 are at GND. When B* is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A* or B* respectively, is open.

Fig. 1



TEST TABLE

Output Under Test	I_{OH} (Min)
Σ or $\overline{\Sigma}$	-400 μA
$\overline{C_{n+1}}$	-200 μA
A* or B*	-120 μA

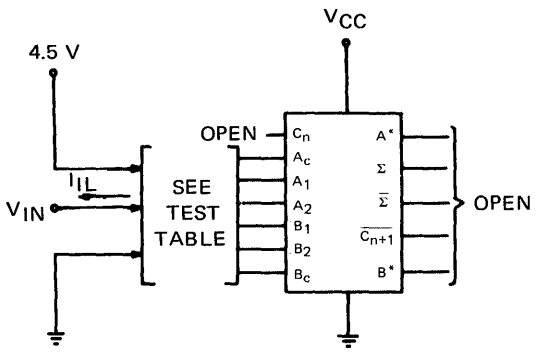
1. Each input or output is tested separately.
2. When A* is tested A_1 and A_2 are at GND. When B* is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A or B , respectively, is open.

Fig. 2

* Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (continued)

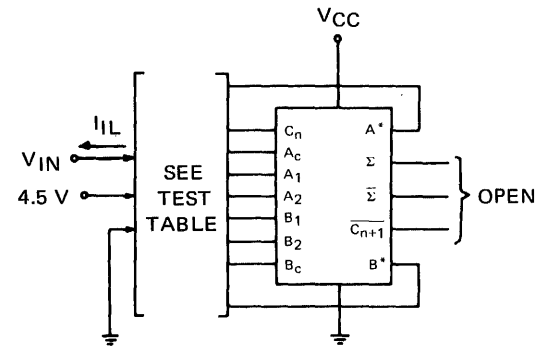


TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_c	None	A_1 and A_2
B_c	None	B_1 and B_2

1. Each input is tested separately.

Fig. 3



TEST TABLE

Apply V_{IN} (Test I_{IL})	Apply 4.5 V	GND
A*	A_c	A_1 and A_2
B*	B_c	B_1 and B_2
C_n	None	None

Unused inputs are open.

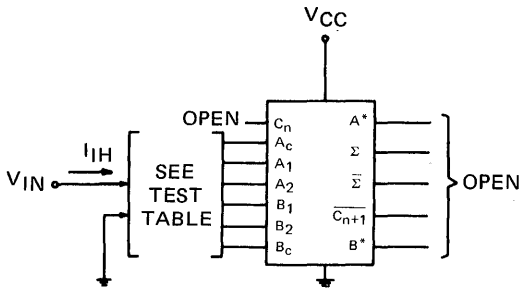
1. Each input is tested separately.

Fig. 4

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (continued)



TEST TABLE

Apply V_{IN} (Test I_{IH})	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A^*
B_c	B^*

1. Each input is tested separately.

Fig. 5

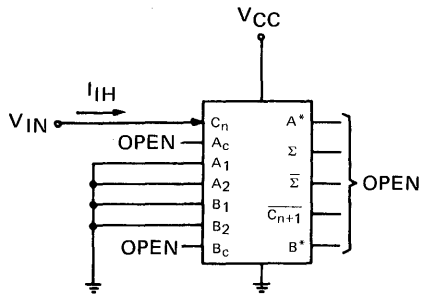
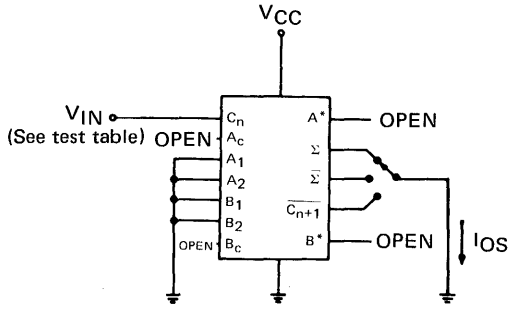


Fig. 6



1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{IN} Value
Σ	V_{CC}
$\bar{\Sigma}$ or $\overline{C_{n+1}}$	GND

Fig. 7

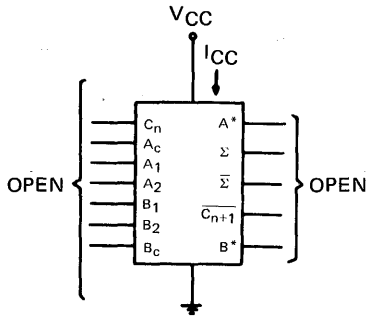
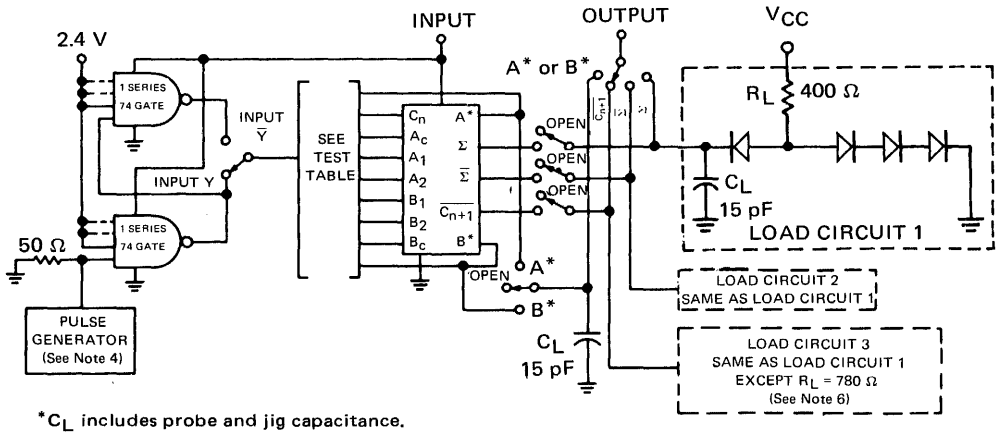


Fig. 8

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

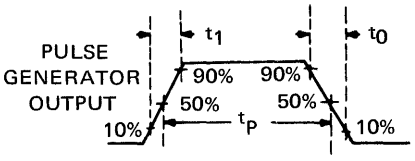
SWITCHING CHARACTERISTICS

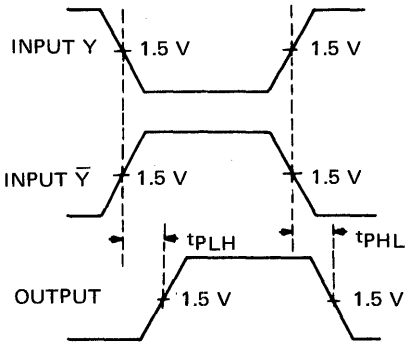


*C_L includes probe and jig capacitance.

NOTES:
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. Load circuit 2 simulates output load of 5.

TEST CIRCUIT





VOLTAGE WAVEFORMS

TEST TABLE (SEE NOTE 5)

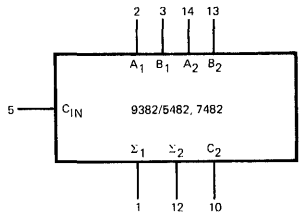
TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY +2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	$\overline{\Sigma}$ (N = 10) Σ (N = 10) $\overline{C_{n+1}}$ (N = 5)
6	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A*	None	A_1	A_2	None	A* (C_L = 15 pF)
10	A*	None	A_1	A_2	None	A* (C_L = 15 pF)
11	B*	None	B_1	B_2	None	B* (C_L = 15 pF)
12	B*	None	B_1	B_2	None	B* (C_L = 15 pF)

Fig. A – SWITCHING TIMES

TTL/MSI 9382/5482, 7482
2-BIT FULL ADDER

DESCRIPTION – The TTL/MSI 9382/5482,7482 is a Full Adder which performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilized high speed, high fan out TTL. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

LOGIC SYMBOL

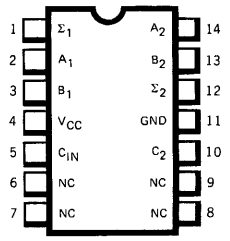


V_{CC} = Pin 4
GND = Pin 11
NC = Pin 6, 7, 8, 9

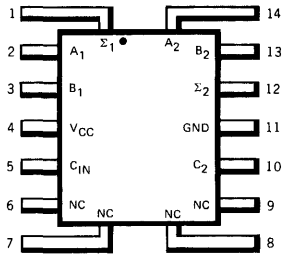
PIN NAMES		LOADING
A_1,B_1	Data Inputs	4 U.L.
A_2,B_2	Data Inputs	1 U.L.
C_{IN}	Carry Input	4 U.L.
Σ_1	Sum Output Bit 1	10 U.L.
Σ_2	Sum Output Bit 2	10 U.L.
C_2	Carry Output Bit 2	5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

CONNECTION DIAGRAM
DIP (TOP VIEW)

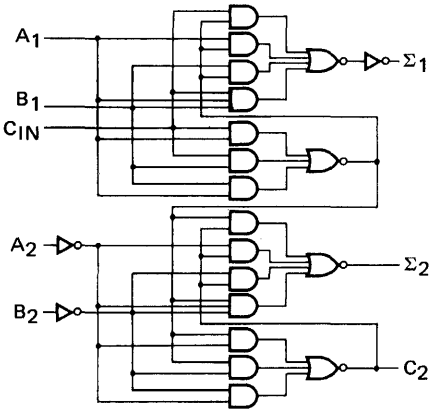


FLATPAK (TOP VIEW)



Positive logic: See truth table
NC – No internal connection

LOGIC DIAGRAM



TRUTH TABLE

INPUT				OUTPUT					
				WHEN C_{IN} = 0			WHEN C_{IN} = 1		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9382XM/5482XM			9382XC/7482XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Output	C_2			5.0			5.0	
	Σ_1 or Σ_2			10			10	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		1 & 2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −400 μA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at A_1, B_1 or C_{IN}			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at A_2 or B_2			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at A_1, B_1 or C_{IN}			−6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at A_2 or B_2			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
I_{OS}	Output Short Circuit Current at Σ_1 or Σ_2 (Note 3)	−20		−55	mA	9382/5482	V_{CC} = MAX.	4
		−18		−55	mA	9382/7482		
	Output Short Circuit Current at C_2 (Note 3)	−20		−70	mA	9382/5482	V_{CC} = MAX.	4
		−18		−70	mA	9382/7482		
I_{CC}	Supply Current		35	50	mA	9382/5482	V_{CC} = MAX.	3
			35	58	mA	9382/7482		

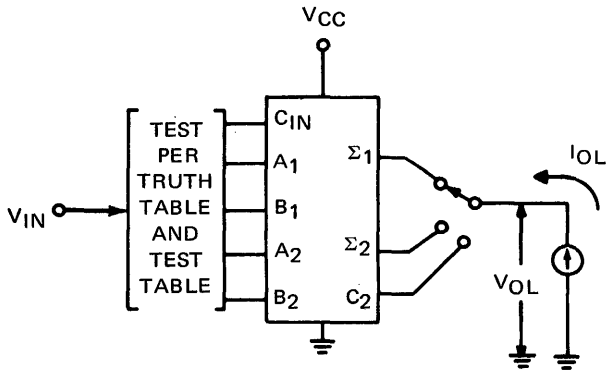
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	FIGURE A TEST NO.
t_{PLH}	C_{IN} to Σ_1			34	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	1
t_{PHL}				40			2
t_{PLH}	B_2 to Σ_2			40	ns		3
t_{PHL}				35			4
t_{PLH}	C_{IN} to Σ_2			38	ns		5
t_{PHL}				42			6
t_{PLH}	C_{IN} to C_2		17	27	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 780Ω	7
t_{PHL}			12	19			8

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

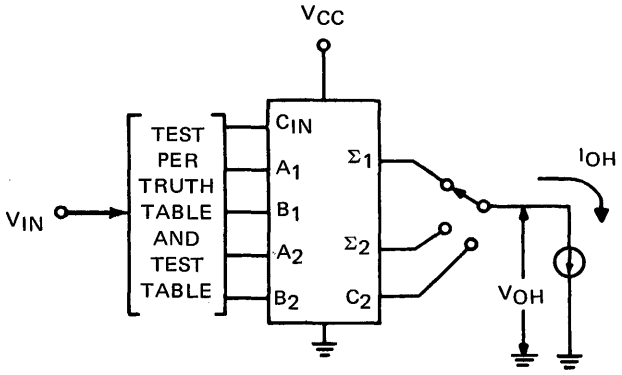


1. Each input or output is tested separately.

TEST TABLE

OUTPUT UNDER TEST	I_{OL}
Σ_1 or Σ_2	16 mA
C_2	8 mA

Fig. 1

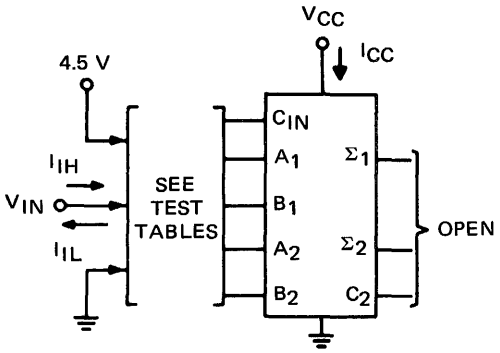


1. Each input or output is tested separately.

TEST TABLE

OUTPUT UNDER TEST	I_{OH}
Σ_1 or Σ_2	–400 μA
C_2	–200 μA

Fig. 2



I_{IL} TEST TABLE

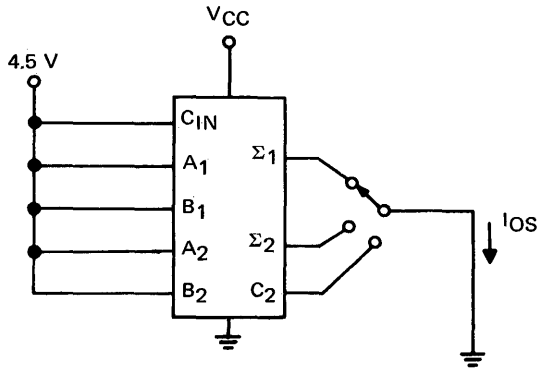
APPLY V_{IN} TEST I_{IN}	APPLY 4.5 V
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None

I_{IH} TEST TABLE

APPLY V_{IN} TEST I_{IN}	GND
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_{IN}; and ground B_1 and B_2.

Fig. 3



1. Each output is tested separately.

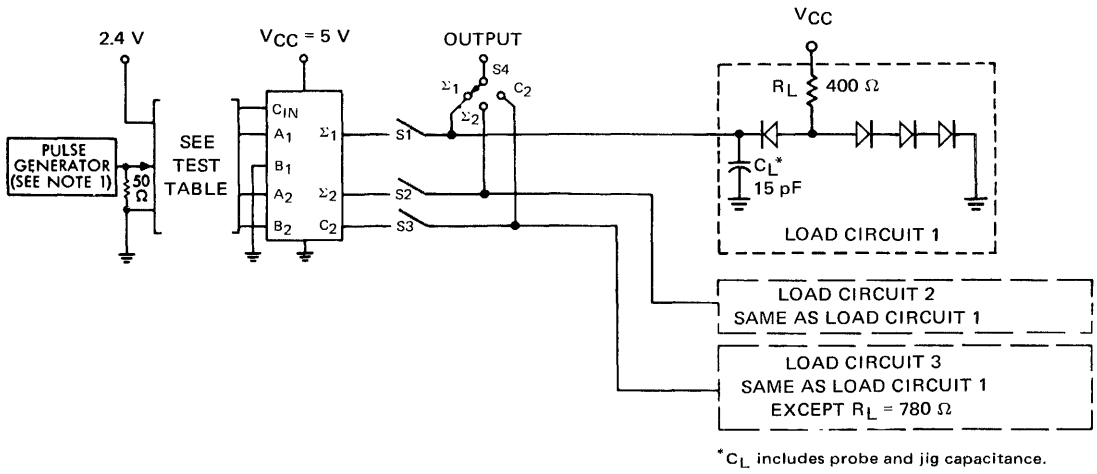
Fig. 4

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

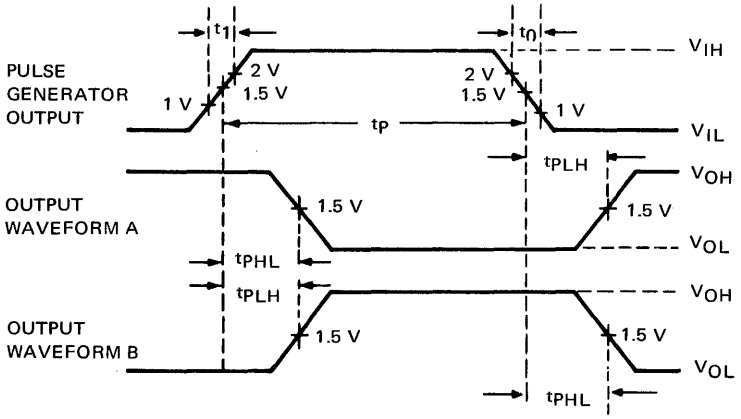
SWITCHING CHARACTERISTICS

TEST CIRCUIT



*C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS



SWITCHING TIMES TEST TABLE (SEE NOTE 5)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S4)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3
1	t_{PLH}	C_{IN}	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
2	t_{PHL}							
3	t_{PLH}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2 and C_{IN}	OPEN	CLOSED	OPEN
4	t_{PHL}							
5	t_{PLH}	C_{IN}	Σ_2 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
6	t_{PHL}							
7	t_{PLH}	C_{IN}	C_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
8	t_{PHL}							

NOTES:

1. The generator has the following characteristics: $V_{IH} \geq 2.4$ V, $V_{IL} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. Inputs and outputs not otherwise specified are open.

Fig. A – SWITCHING TIMES

TTL/MSI 9383/5483, 7483
4-BIT BINARY FULL ADDER

DESCRIPTION – The TTL/MSI 9383/5483,7483 is a Full Adder which performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilized high speed, high fan out TTL. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

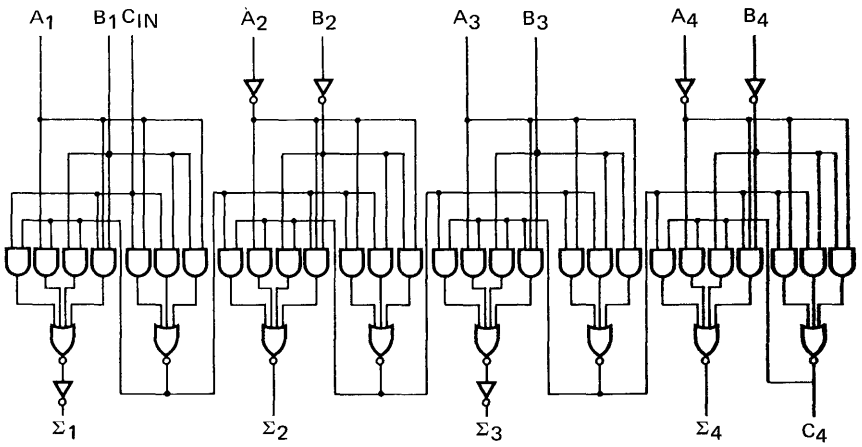
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

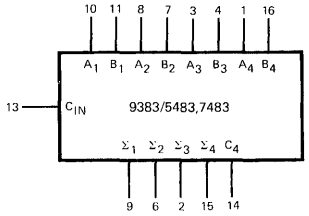
PIN NAMES		LOADING
A_1,B_1,A_3,B_3	Data Inputs	4 U.L.
A_2,B_2,A_4,B_4	Data Inputs	1 U.L.
C_{IN}	Carry Input	4 U.L.
$\Sigma_1,\Sigma_2,\Sigma_3,\Sigma_4$	Sum Outputs	10 U.L.
C_4	Carry Out Bit 4	5 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

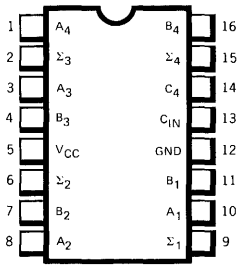


LOGIC SYMBOL

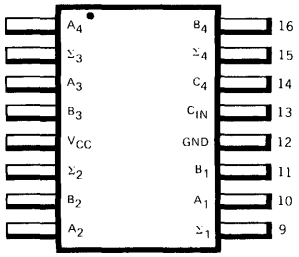


V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic: See truth table

TRUTH TABLE (See Note 1)

INPUT				OUTPUT					
				WHEN $C_{IN}=0$			WHEN $C_{IN}=1$		
				WHEN $C_2=0$			WHEN $C_2=1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_3	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE:
1. Input conditions at A_1, A_2, B_1, B_2 and C_{IN} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4 and C_4.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9383XM/5483XM			9383XC/7483XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Outputs	C_4,			5.0			5.0	U. L.
	Σ_1, Σ_2, Σ_3 or Σ_4			10			10	U. L.

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		1 & 2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = See Fig.2		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = See Fig.1		1
I_{IH}	Input HIGH Current at A_1, A_3, B_1, B_3 or C_{IN}			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at A_2, A_4, B_2 or B_4			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at A_1, A_3, B_1, B_3, or C_{IN}			−6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
	Input LOW Current at A_2, A_4, B_2 or B_4			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
I_{OS}	Output Short Circuit Current at Σ_1, Σ_2, Σ_3 or Σ_4 (Note 3)	−20		−55	mA	9383/5483	V_{CC} = MAX.	4
		−18		−55	mA	9383/7483		
	Output Short Circuit Current at C_4 (Note 3)	−20		−70	mA	9383/5483	V_{CC} = MAX.	4
		−18		−70	mA	9383/7483		
I_{CC}	Supply Current		78	110	mA	9383/5483	V_{CC} = MAX.	3
			78	128	mA	9383/7483		

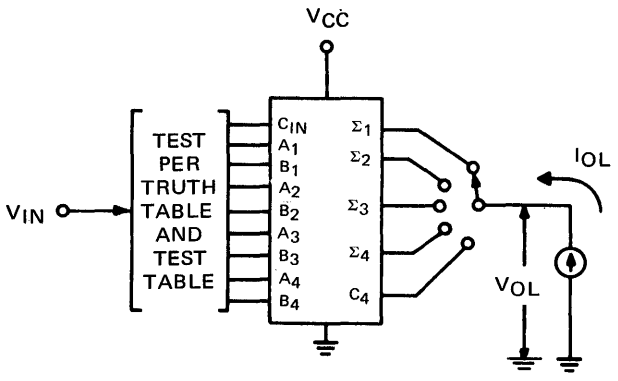
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	FIGURE A TEST NO.
		MIN.	TYP.	MAX.			
t_{PLH}	C_{IN} to Σ_1			34	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	1
t_{PHL}				40			2
t_{PLH}	C_{IN} to Σ_2			38	ns		3
t_{PHL}				42			4
t_{PLH}	C_{IN} to Σ_3			50	ns		5
t_{PHL}				60			6
t_{PLH}	C_{IN} to Σ_4			55	ns		7
t_{PHL}				55			8
t_{PLH}	C_{IN} to C_4		35	48	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 780Ω	9
t_{PHL}			22	32			10
t_{PLH}	A_2 or B_2 to Σ_2			40	ns	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	11 & 13
t_{PHL}				35			12 & 14
t_{PLH}	A_4 or B_4 to Σ_4			40	ns		15 & 17
t_{PHL}				35			16 & 18

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT*

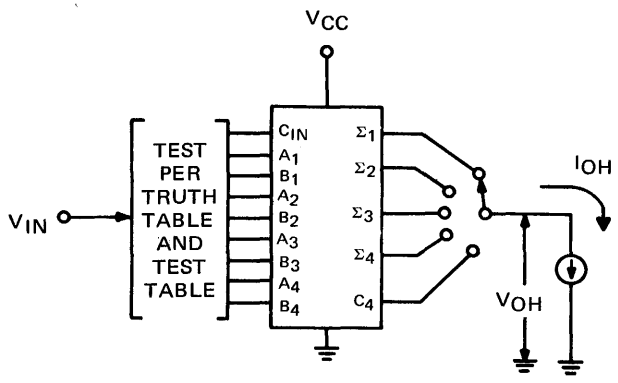


1. Each input or output is tested separately.

TEST TABLE

OUTPUT UNDER TEST	I_{OL}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

Fig. 1



1. Each input or output is tested separately.

TEST TABLE

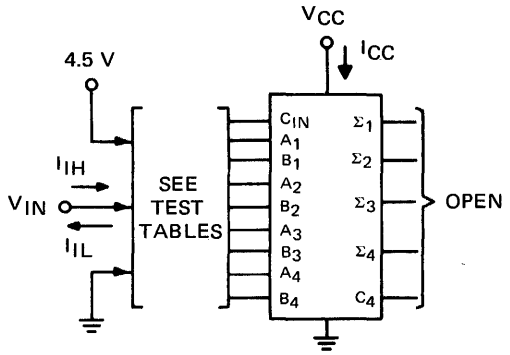
OUTPUT UNDER TEST	I_{OH}
Σ_1, Σ_2, Σ_3, or Σ_4	–400 μA
C_4	–200 μA

Fig. 2

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (continued)



I_{IL} TEST TABLE

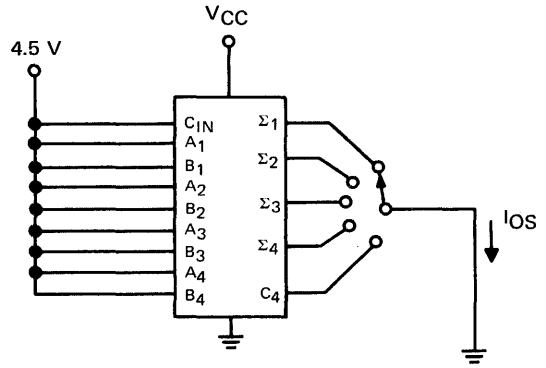
APPLY V_{IN} TEST I_{IN}	APPLY 4.5 V
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

I_{IH} TEST TABLE

APPLY V_{IN} TEST I_{IN}	GND
C_{IN}	A_1 and B_1
A_1	C_{IN} and B_1
B_1	C_{IN} and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_{IN}; and ground B_1, B_2, B_3, and B_4.

Fig. 3



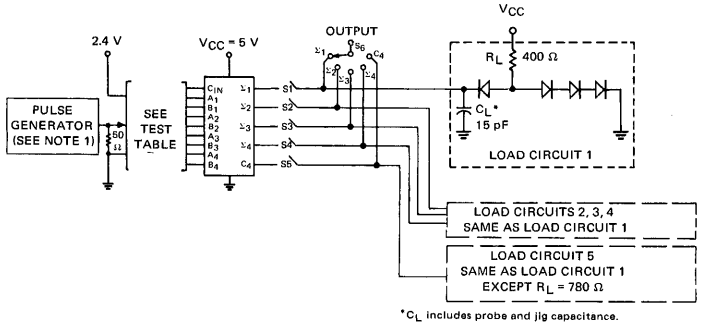
1. Each output is tested separately.

Fig. 4

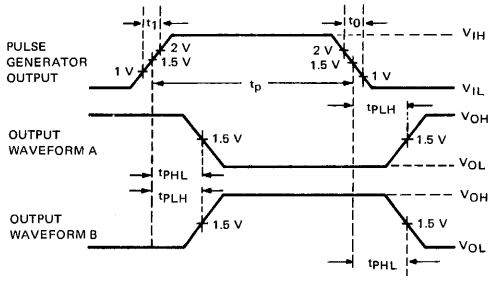
*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE (SEE NOTE 5)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{PLH}	C_{IN}	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{PHL}									
3	t_{PLH}	C_{IN}	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{PHL}									
5	t_{PLH}	C_{IN}	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{PHL}									
7	t_{PLH}	C_{IN}	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{PHL}									
9	t_{PLH}	C_{IN}	C_4 (WAVEFORM B)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{PHL}									
11	t_{PLH}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_{IN}	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{PHL}									
13	t_{PLH}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_{IN}	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{PHL}									
15	t_{PLH}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{PHL}									
17	t_{PLH}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{PHL}									

NOTES:
1. Pulse generator output pulse characteristics: $V_{IH} \leq 2.4$ V, $V_{IL} \leq 0.4$ V, $t_1 = 8$ to 15 ns, $t_0 = 3$ to 5 ns, PRR = 1 MH_z, $t_P = 200$ ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. Inputs and outputs not otherwise specified are open.

Fig. A – SWITCHING TIMES

TTL/MSI 9386
4-BIT QUAD EXCLUSIVE-NOR

DESCRIPTION — The 9386 consists of four independent Exclusive-NOR gates with open collector outputs. Single 1-bit comparisons may be made with each gate, or multiple bit comparisons may be made by connecting the outputs of the four gates together. Typical power dissipation is 170 mW.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

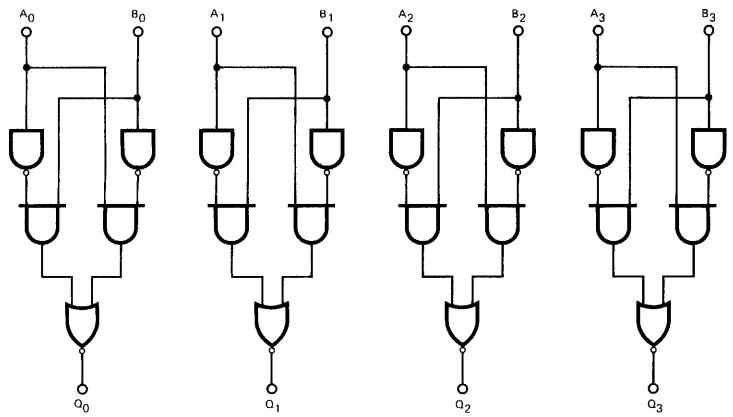
PIN NAMES		LOADING
A_0 to A_3, B_0 to B_3	Inputs	2.0 U.L.
Q_0 to Q_3	Outputs	15 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

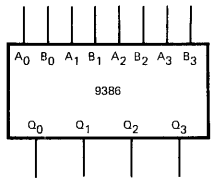
TRUTH TABLE

INPUTS A	INPUTS B	OUTPUT Q
L	L	H
H	L	L
L	H	L
H	H	H

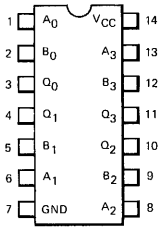
LOGIC DIAGRAM



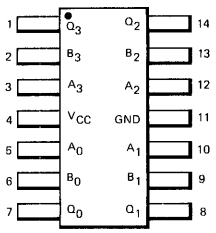
LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	9386XM			9386XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	-55	25	125	0	25	70	°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

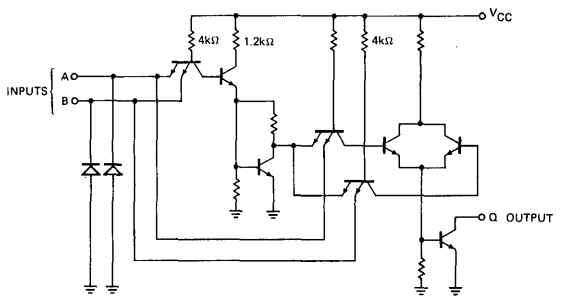
SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 4)	LIMITS MAX.	UNITS	CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage
I_{CEX}	Output HIGH Leakage Current				150	μA	V_{CC} = MIN., V_{IN} = V_{IH} V_{OUT} = 4.5 V
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., V_{IN}(A) = 2.0 V, V_{IN}(B) = 0.8 V, I_{OL} = 25 mA (Note 3)
I_{IH}	Input HIGH Current				80	μA	V_{CC} = MAX., V_{IN}(A) = V_{IN}(B) = 4.5 V (Note 4)
I_{IL}	Input LOW Current		-0.1		-3.2	mA	V_{CC} = MAX., V_{IN}(A) = V_{IN}(B) = 0.4 V (Note 5)
I_{CC}	Supply Current			32	47.5	mA	V_{CC} = 5.25 V, V_{IN}(A) = V_{IN}(B) = 0.4 V
V_{LV}	Input Latch Voltage	A Input	5.5			Volts	$I_{IN(A)}$ = 10 mA, $V_{IN(B)}$ = 0 V
		B Input	5.5			Volts	$V_{IN(A)}$ = 0 V, $I_{IN(B)}$ = 10 mA (Note 6)

SWITCHING CHARACTERISTICS (T_A = 25°C)

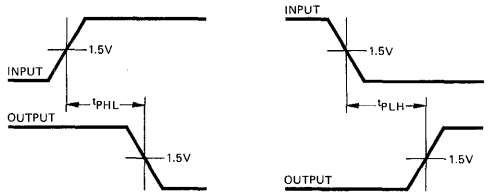
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay Input to Output		18	25	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay Input to Output		18	25	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Output sink current is supplied through a resistor to V_{CC}.
(4) A and B are tested separately. When A is 4.5 V, B is 0 V, and vice versa.
(5) A and B are tested separately. When A is 0.4 V, B is 5.25 V, and vice versa.
(6) This test guarantees operation free of input latch-up over the specified operating supply voltage range.

SCHEMATIC DIAGRAMS



SWITCHING CHARACTERISTICS



8

TTL/MSI 93H87/54H87, 74H87

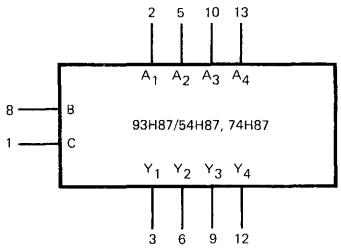
HIGH SPEED 4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT

DESCRIPTION — The 93H87/54H87, 74H87 will perform four functions; use of the B and C control inputs determine the function performed. A 4-bit binary number (A) can be transferred to the output (Y) in either true or complementary form. In addition the control inputs can also set all outputs to LOW or HIGH independent of the state of the data inputs.

PIN NAMES		LOADING
A_1, A_2, A_3, A_4	Data Inputs	1.0 U.L.
B, C	Control Inputs	1.0 U.L.
Y_1, Y_2, Y_3, Y_4	Outputs	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL

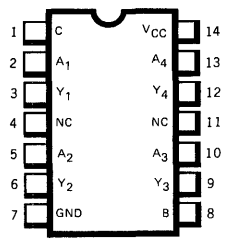


V_{CC} = PIN 14
GND = PIN 7

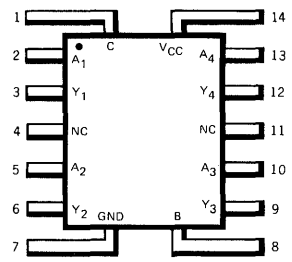
TRUTH TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y_1	Y_2	Y_3	Y_4
L	L	$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$
L	H	A_1	A_2	A_3	A_4
H	L	H	H	H	H
H	H	L	L	L	L

CONNECTION DIAGRAM
DIP (TOP VIEW)

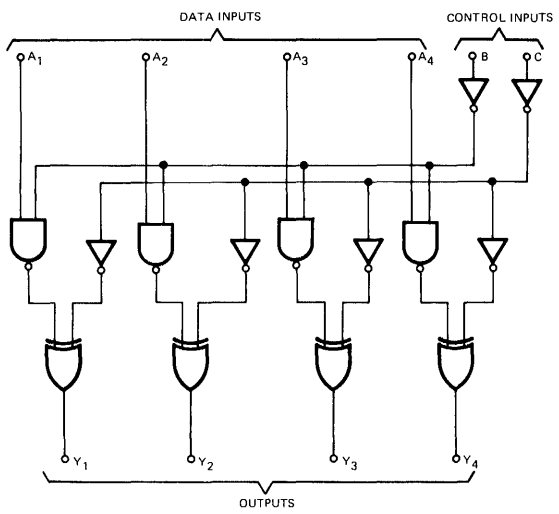


FLATPAK (TOP VIEW)



NC — No Internal Connection
Positive Logic: See Truth Table

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either input voltage or input current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93H87XM/54H87XM			93H87XC/74H87XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	LOW Level			10			10	U.L.
	HIGH Level			20			20	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage		1
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -1.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
I_{IH}	Input HIGH Current			50	μA	V_{CC} = MAX., V_{IN} = 2.4 V	Each Input	2
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			-2.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Each Input		3
I_{OS}	Output Short Circuit Current (Note 3)	-40		-100	mA	V_{CC} = MAX., V_{OUT} = 0 V		4
I_{CC}	Supply Current		54	78	mA	93H87/54H87	V_{CC} = MAX.	5
			54	89	mA	93H87/74H87		

SWITCHING CHARACTERISTICS (T_A = 25°C)

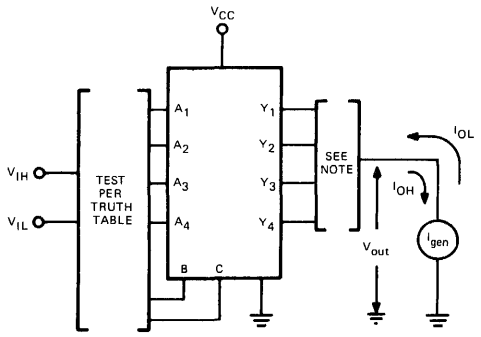
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output (Data Inputs to Outputs)		14	20	ns	V_{CC} = 5.0 V C_L = 25 pF R_L = 280 Ω	A
t_{PHL}	Turn On Delay Input to Output (Data Inputs to Outputs)		13	19	ns		
t_{PLH}	Turn Off Delay Input to Output (Control Inputs to Outputs)		17	25	ns		
t_{PHL}	Turn On Delay Input to Output (Control Inputs to Outputs)		17	25	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

8

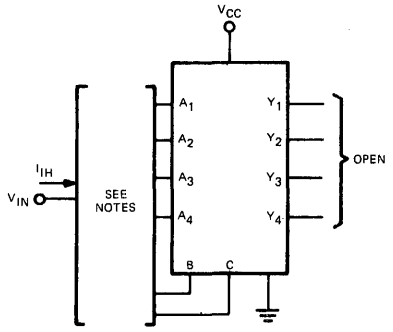
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



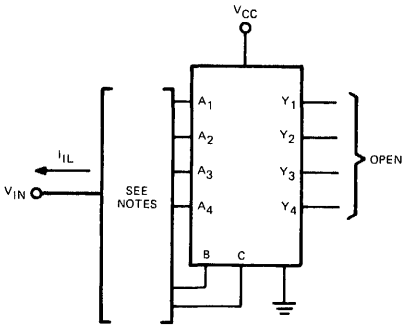
1. Each output is tested separately.

Fig. 1



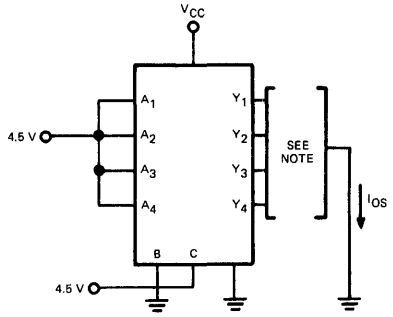
1. Each input is tested separately.
2. When testing A_1, A_2, A_3 or A_4 input B is at 4.5 V.

Fig. 2



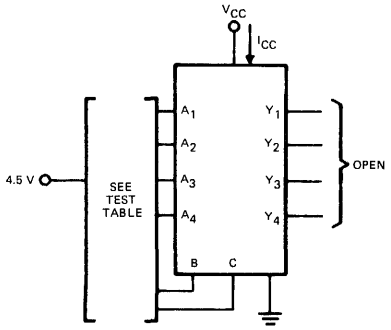
1. Each input is tested separately.
2. When testing A_1, A_2, A_3 or A_4 input B is grounded.

Fig. 3



1. Each output is tested separately.

Fig. 4



TEST TABLE

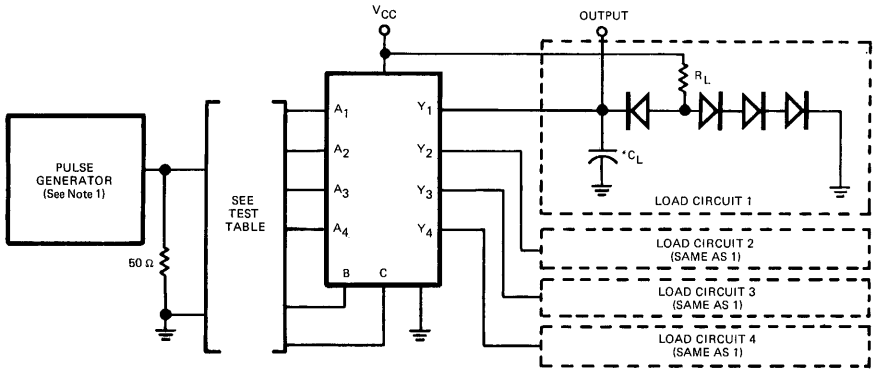
TEST NO.	APPLY 4.5 V	GROUND
1	A_1, A_2, A_3, A_4	B,C,
2	B, C	A_1, A_2, A_3, A_4

Fig. 5

*Arrows indicate actual direction of current flow.

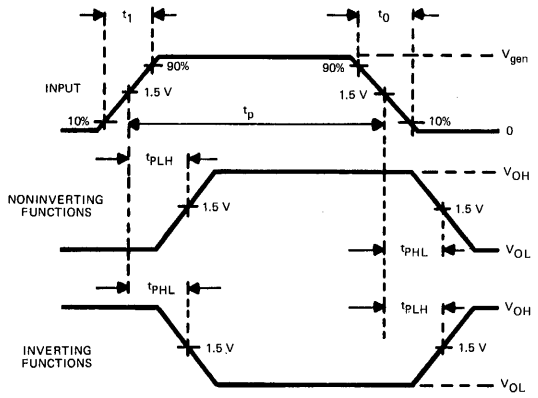
PARAMETER MEASUREMENT INFORMATION (cont'd)

SWITCHING CHARACTERISTICS



*C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

TEST TABLE (See Note 2)

GND	INPUT	OUTPUT
B, C	A1	Y1
B, C	A2	Y2
B, C	A3	Y3
B, C	A4	Y4
C	B	Y1
C	B	Y2
C	B	Y3
C	B	Y4
B	C	Y1
B	C	Y2
B	C	Y3
B	C	Y4

NOTES:
1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 7 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
2. Inputs not specified are open.

Fig. A – SWITCHING TIMES

TTL/MSI 9390/5490, 7490
DECADE COUNTER

DESCRIPTION – The TTL/MSI 9390/5490, 7490 is a Decade Counter which consists of four dual rank, master slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Count inputs are inhibited, and all outputs are returned to logical zero or a binary coded decimal (BCD) count of 9 through gated direct reset lines. The output from flip-flop A is not internally connected to the succeeding stages, therefore the count may be separated into these independent count modes:

A. If used as a binary coded decimal decade counter, the $\overline{CP}_{BD}$ input must be externally connected to the Q_A output. The $\overline{CP}_A$ input receives the incoming count, and a count sequence is obtained in accordance with the BCD count for nine's complement decimal application.

B. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the Q_D output must be externally connected to the $\overline{CP}_A$ input. The input count is then applied at the $\overline{CP}_{BD}$ input and a divide-by-ten square wave is obtained at output Q_A.

C. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The $\overline{CP}_{BD}$ input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

PIN NAMES		LOADING
R_0	Reset-Zero Inputs	1 U.L.
R_9	Reset-Nine Inputs	1 U.L.
$\overline{CP}_A$	Clock Input	2 U.L.
$\overline{CP}_{BD}$	Clock Input	4 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

BCD COUNT SEQUENCE (Note 1)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

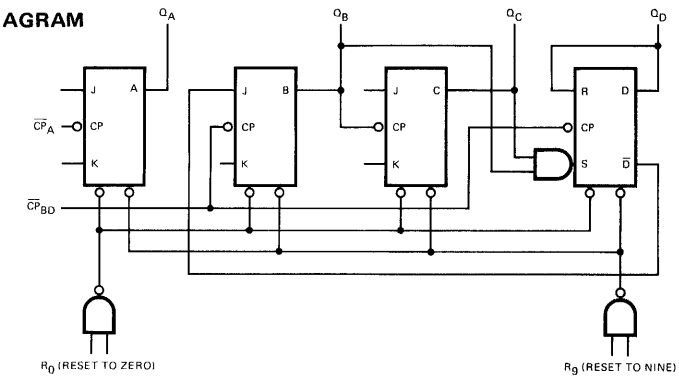
TRUTH TABLES

RESET/COUNT (see Note 2)

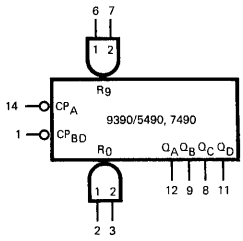
RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D Q_C Q_B Q_A
H	H	L	X	L L L L
H	H	X	L	L L L L
X	X	H	H	H L L H
X	L	X	L	COUNT
L	X	L	X	COUNT
L	X	X	L	COUNT
X	L	L	X	COUNT

NOTES:
1. Output Q_A connected to input CP_{BD} for BCD count.
2. X indicates that either a HIGH level or a LOW level may be present.

LOGIC DIAGRAM

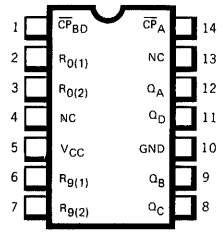


LOGIC SYMBOL

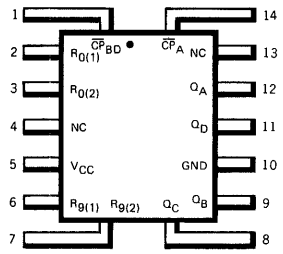


V_{CC} = Pin 5
GND = Pin 10
NC = Pin 4, 13

CONNECTION DIAGRAM DIP (TOP VIEW)



FLAT PAK (TOP VIEW)



Positive logic: See Truth Table.
NC – No internal connection.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9390XM/5490XM			9390XC/7490XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N (Note 5)			10			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			50			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -0.4 mA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_A$			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_{BD}$			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_A$			-3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_{BD}$			-6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current (Note 3)	-20		-57	mA	9390/5490	V_{CC} = MAX.	5
		-18		-57	mA	9390/7490		
I_{CC}	Supply Current		32	46	mA	9390/5490	V_{CC} = MAX.	3
			32	53	mA	9390/7490		

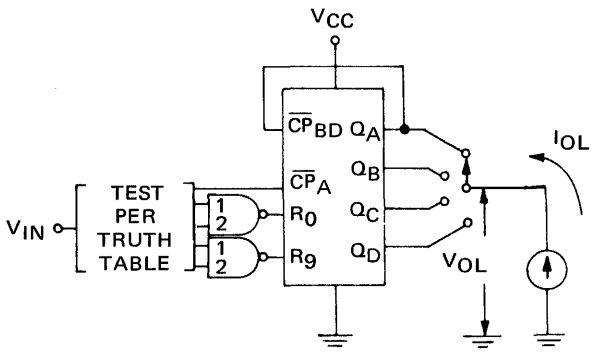
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Frequency of Input Count Pulse	10	18		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	
t_{PLH}	Turn Off Delay from Input Count Pulse to Output Q_C		60	100	ns		A
t_{PHL}	Turn On Delay from Input Count Pulse to Output Q_C		60	100	ns		A

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.
(5) Fan out from output Q_A to input $\overline{CP}_{BD}$ and to 10 additional series 54/74 loads is permitted.

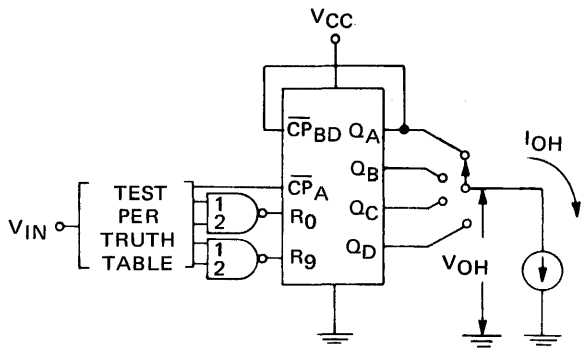
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT*



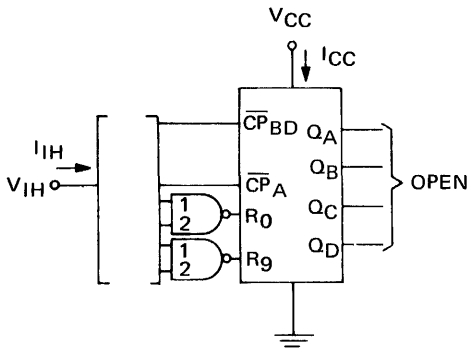
1. Each output is tested in the LOW level state.

Fig. 1



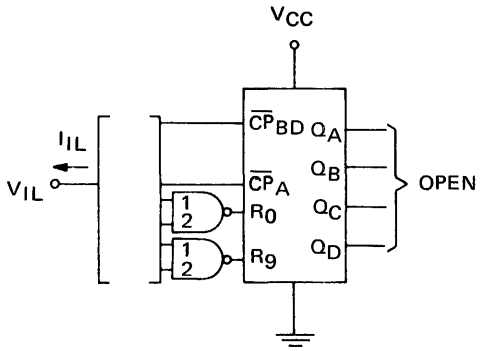
1. Each output is tested in the HIGH level state.

Fig. 2



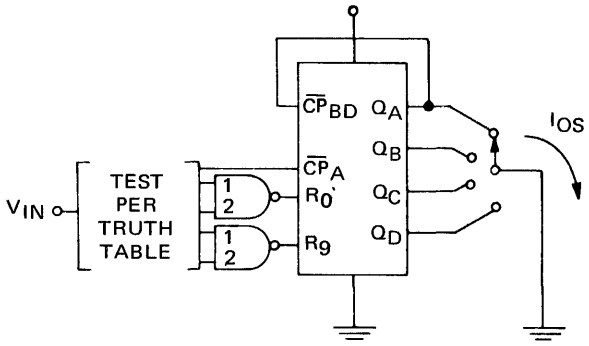
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$.
4. When testing I_{CC} reset all outputs to LOW level, ground all inputs, then measure I_{CC}.

Fig. 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5 V to $R_{0(1)}$ or $R_{9(1)}$.

Fig. 4



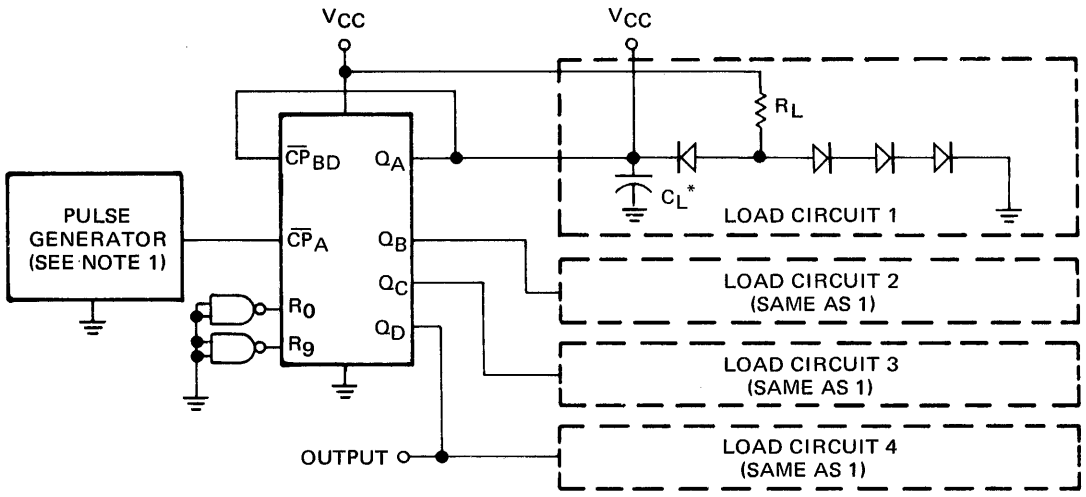
1. Each output is tested in the HIGH level state.

Fig. 5

*Arrows indicate actual direction of current flow.

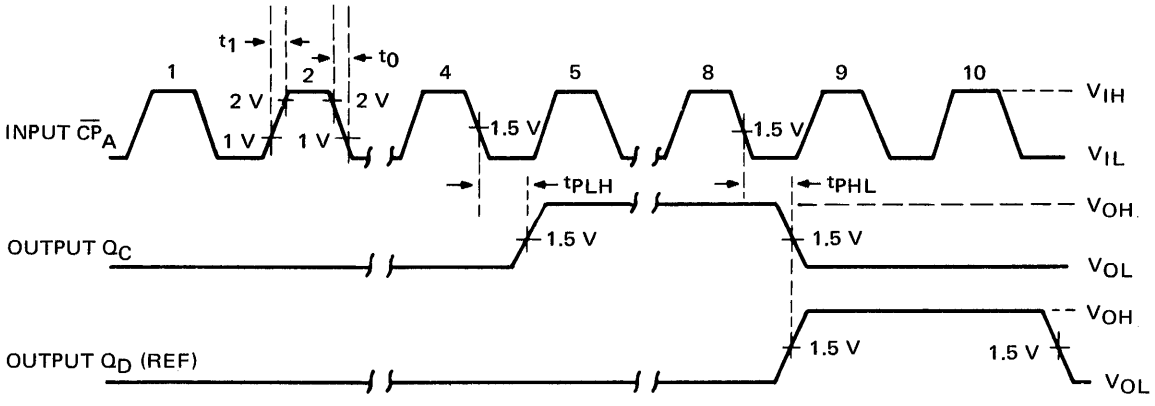
PARAMETER MEASUREMENT INFORMATION (Con't.)

SWITCHING CHARACTERISTICS



*C_L includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation Delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. Voltage values are with respect to ground terminal.

Fig. A – SWITCHING TIMES

8

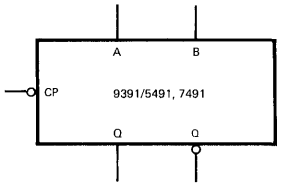
TTL/MSI 9391/5491, 7491
8-BIT SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9391/5491, 7491 is a serial-in, serial-out, 8-Bit Shift Register utilizing TTL technology. It is composed of eight RS master/slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1.0V. Power dissipation is typically 175 mW; a full fan out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.

LOGIC SYMBOL



PIN NAMES		LOADING
A, B	Data Inputs	1 U.L.
Q, $\overline{Q}$	Data Output	10 U.L.
$\overline{CP}$	Clock Input	1 U.L.

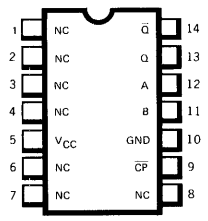
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE

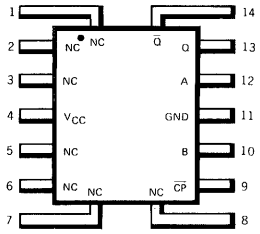
t_n		t_{n+8}
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

NOTES:
t_n = Bit time before clock pulse.
t_{n+8} = Bit time after 8 clock pulses.

CONNECTION DIAGRAM
DIP (TOP VIEW)



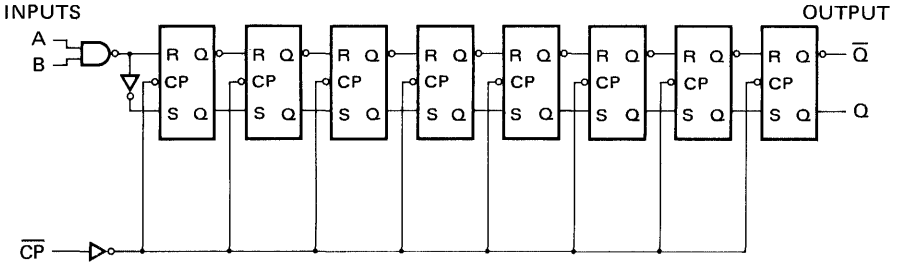
FLATPAK (TOP VIEW)



NC—No Internal Connection

Positive logic: See truth table.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9391XM/5491XM			9391XC/7491XC			UNITS
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Outputs			10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$ (See Fig. A)	25			25			ns
Input Setup Time, t_{setup} (See Fig. A)	25			25			ns
Input Hold Time, t_{hold} (See Fig. A)	0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		2
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA		1
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		2
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		4
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4V		3
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9391/5491	V_{CC} = MAX.	5
		−18		−57	mA	9391/7491	V_{OUT} = 0V	
I_{CC}	Supply Current		35	50	mA	9391/5491	V_{CC} = MAX.	6
			35	58	mA	9391/7491	V_{IN} = 4.5 V	

SWITCHING CHARACTERISTICS (T_A = 25°C)

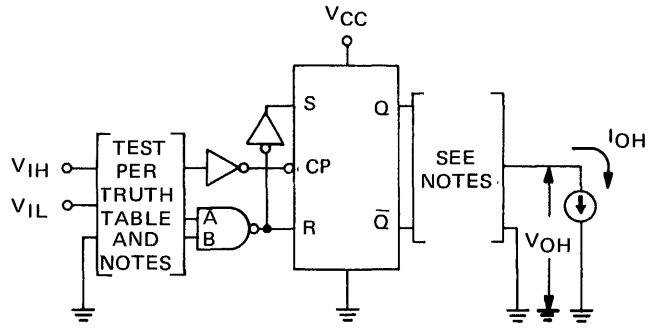
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	10	18		MHz	V_{CC} = 5.0 V	
t_{PLH}	Turn Off Delay from Clock to Output		24	40	ns	C_L = 15 pF	A
t_{PHL}	Turn On Delay from Clock to Output		27	40	ns	R_L = 400Ω	A

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

8

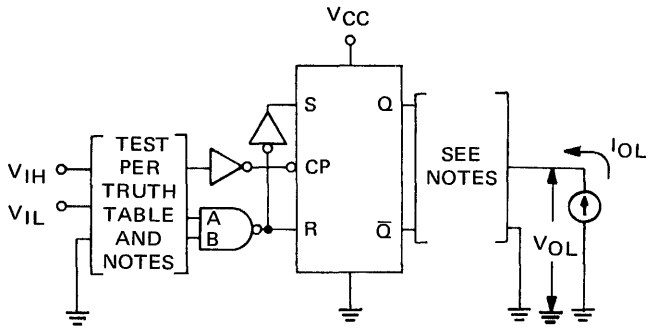
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



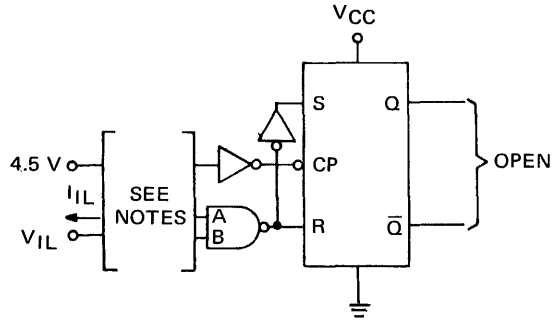
1. Each output is tested separately.
2. When testing V_{OH} and I_{OH} ground all inputs and the unused output, then measure parameters specified.

Fig. 1



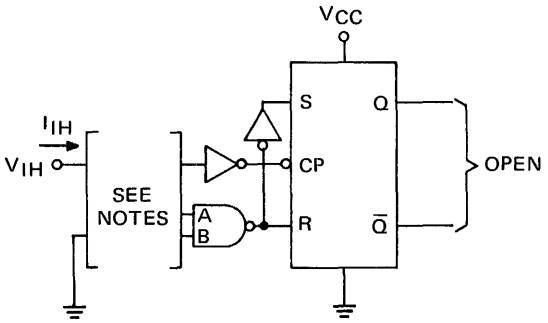
1. Each output is tested separately.
2. When testing V_{OL} and I_{OL} ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified.

Fig. 2



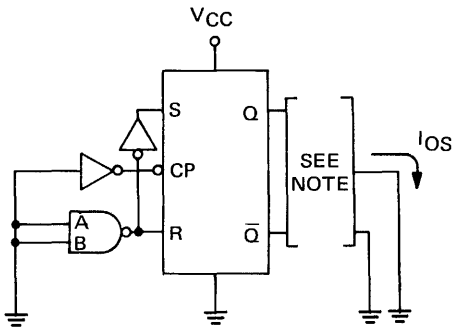
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

Fig. 3



1. When testing input A ground input B.
2. When testing input B ground input A.

Fig. 4



1. Ground the unused output then measure parameter specified.

Fig. 5

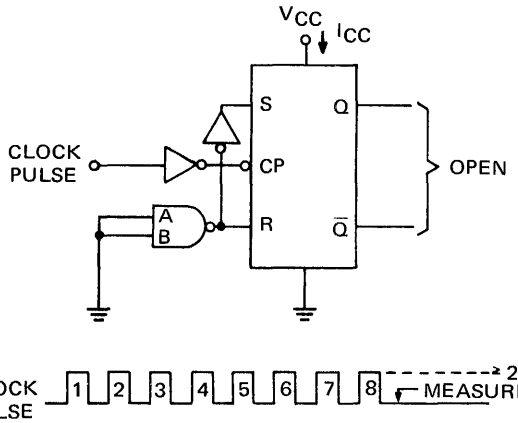
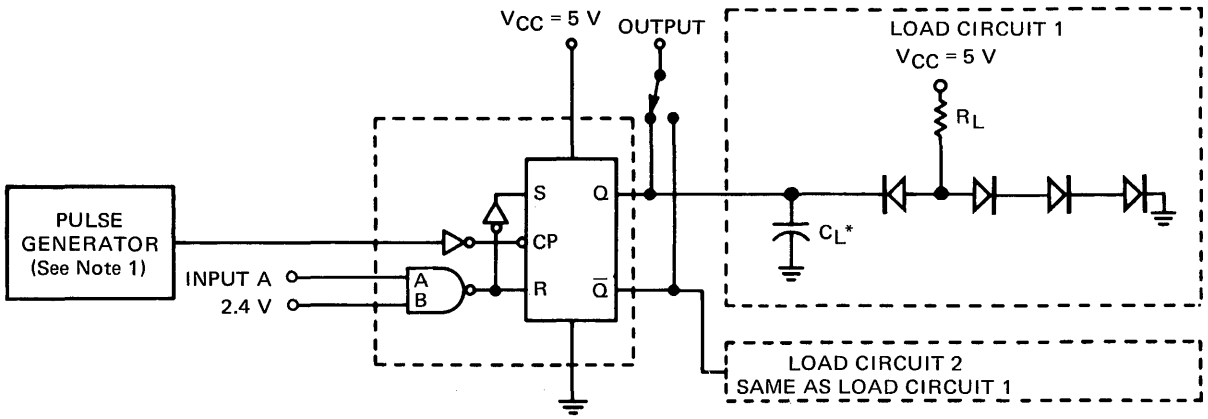


Fig. 6

*Arrows indicate actual direction of current flow.

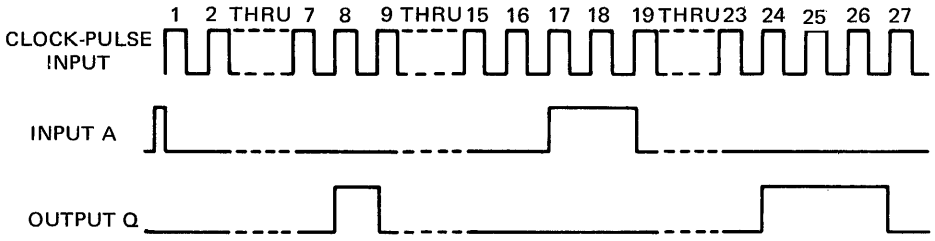
PARAMETER MEASUREMENT INFORMATION (Con't)

SWITCHING CHARACTERISTICS

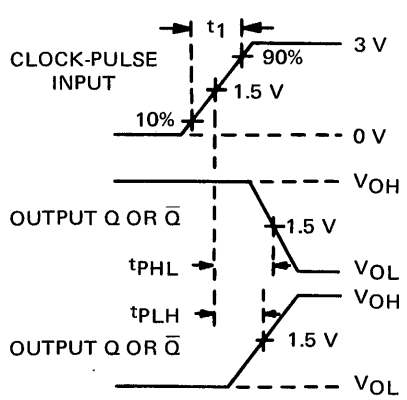


*C_L includes probe and jig capacitance

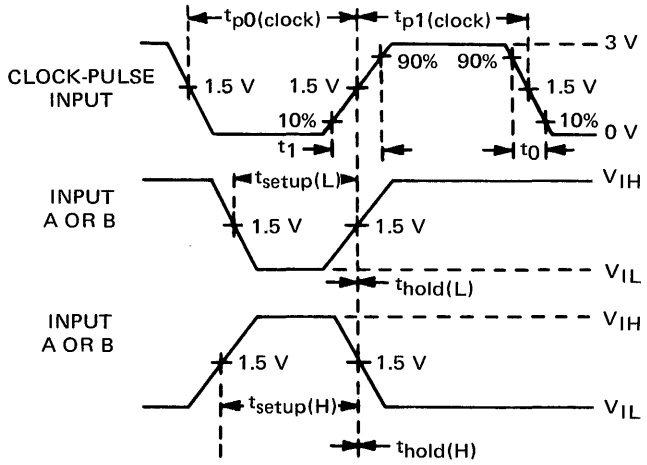
TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORM



SWITCHING TIME VOLTAGE WAVEFORM

NOTES:
1. The generator has the following characteristics: $V_{IL} \leq 0.3$ V, $V_{IH} \geq 2.4$V, $t_1 = t_0 = 10$ ns, $t_{p1(clock)} = 500$ ns, $t_{p0(clock)} = 500$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\Omega$.
2. Each output is tested separately.
3. Voltage values are with respect to network ground terminal.

Fig. A 9391/5491, 7491 SWITCHING TIMES

8

TTL/MSI 9392/5492, 7492

DIVIDE-BY-TWELVE COUNTER (DIVIDE-BY-TWO AND DIVIDE-BY-SIX)

DESCRIPTION – The TTL/MSI 9392/5492, 7492 is a 4-Bit Binary Counter consisting of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A grated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

A. When used as a divide-by-twelve counter, output Q_A must be externally connected to input $\overline{CP}_{BC}$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneous divisions of 2, 6 and 12 are performed at the Q_A, Q_C and Q_D outputs as shown in the truth table.

B. When used as a divide-by-six counter, the input count pulses are applied to input $\overline{CP}_{BC}$. Simultaneously, frequency divisions of 3 and 6 are available at the Q_C and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES		LOADING
R_0	Reset-Zero Inputs	1 U.L.
$\overline{CP}_A$	Clock Input	2 U.L.
$\overline{CP}_{BC}$	Clock Input	4 U.L.
Q_A, Q_B, Q_C, Q_D	Count Outputs	10 U.L.

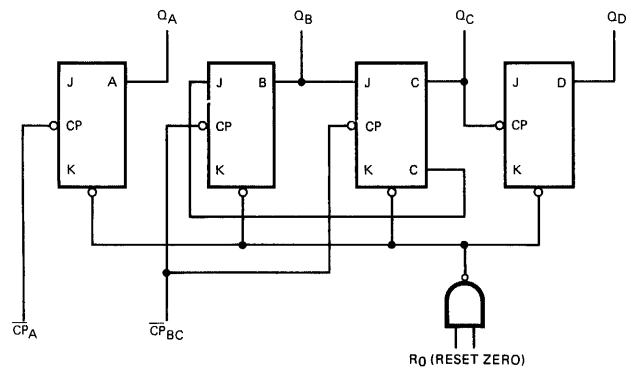
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.

TRUTH TABLE
(See Notes 1, 2 and 3)

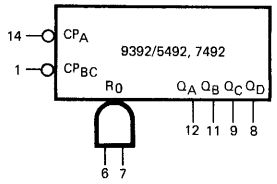
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

NOTES:
1. Output Q_A connected to input $\overline{CP}_{BC}$.
2. To reset all outputs to LOW level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a LOW level to count.

LOGIC DIAGRAM

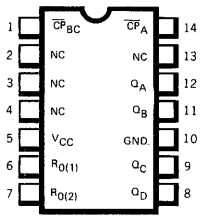


LOGIC SYMBOL

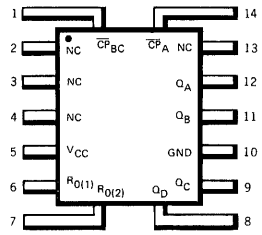


V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 2, 3, 4, 13

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic: See truth table.

NC – No internal connection.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9392XM/5492XM			9392XC/7492XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N (Note 5)			10			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			50			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_A$			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Input $\overline{CP}_{BC}$			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_A$			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Input $\overline{CP}_{BC}$			−6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9392/5492	V_{CC} = MAX.	5
		−18		−57	mA	9392/7492	V_{OUT} = 0 V	
I_{CC}	Supply Current		31	44	mA	9392/5492	V_{CC} = MAX.	3
			31	51	mA	9392/7492	V_{IN} = 4.5 V	

SWITCHING CHARACTERISTICS (T_A = 25°C)

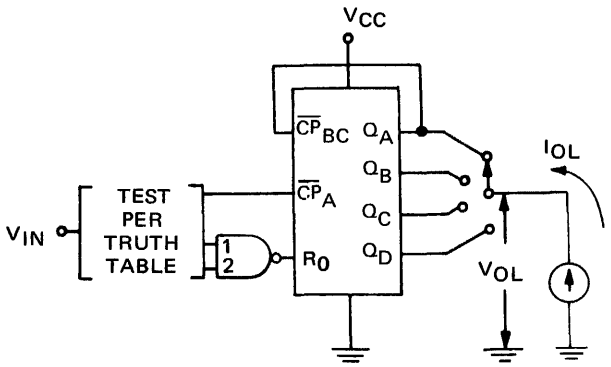
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Frequency of Input Count Pulse	10	18		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	
t_{PLH}	Turn Off Delay from Input Count Pulse to Output Q_D		60	100	ns		A
t_{PHL}	Turn On Delay from Input Count Pulse to Output Q_D		60	100	ns		A

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.
(5) Fan-out from output Q_A to input $\overline{CP}_{BC}$ and to 10 additional series 54/74 loads is permitted.

8

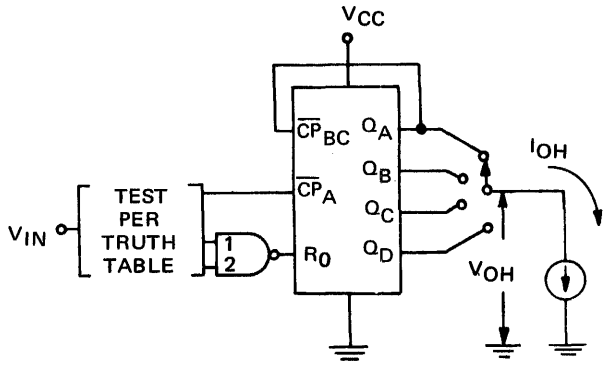
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUIT*



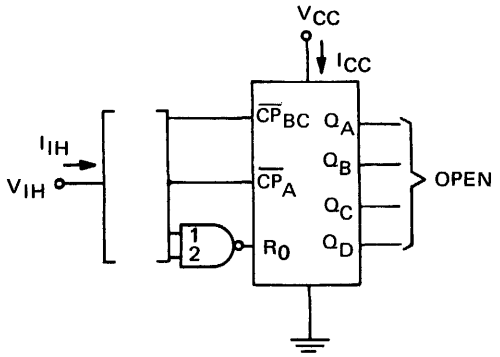
1. Each output is tested in the LOW level state.

Fig. 1



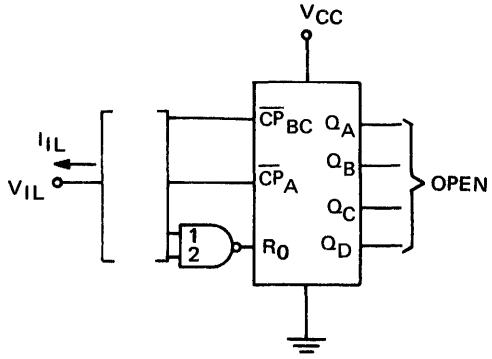
1. Each output is tested in the HIGH level state.

Fig. 2



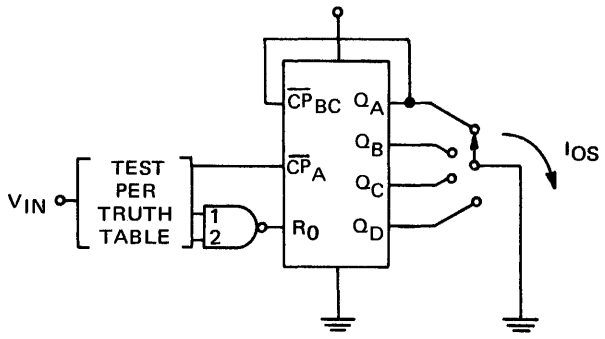
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} reset all outputs to LOW level, ground all inputs, then measure I_{CC}.

Fig. 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

Fig. 4



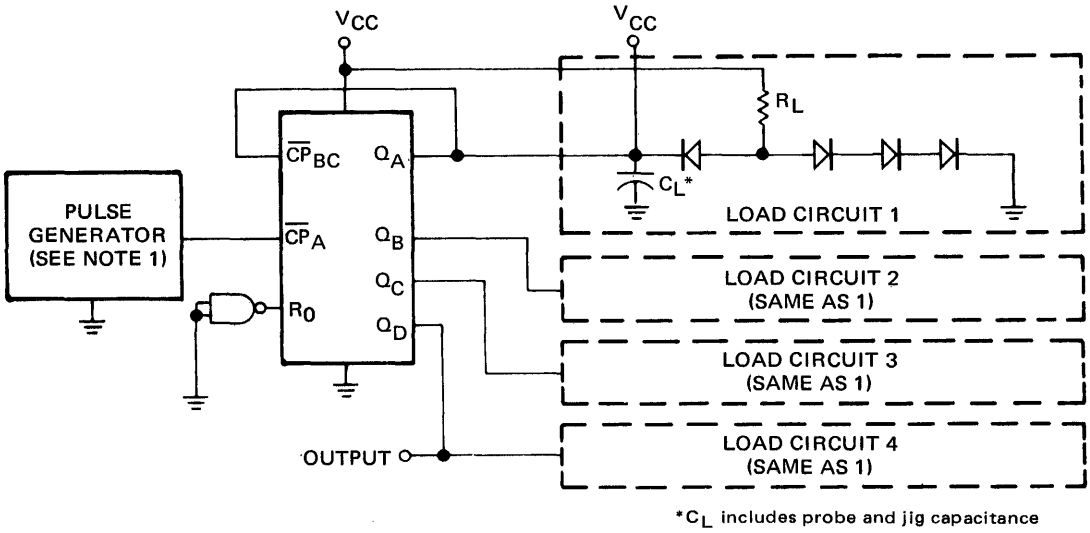
1. Each output is tested in the HIGH level state.

Fig. 5

*Arrows indicate actual direction of current flow.

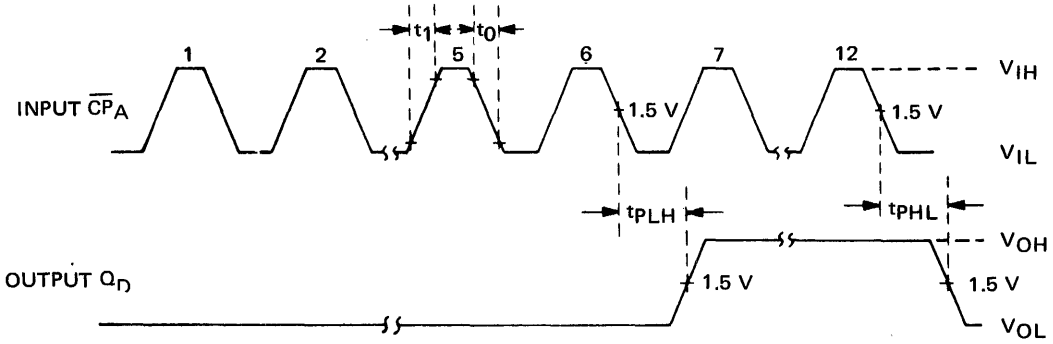
PARAMETER MEASUREMENT INFORMATION (Con't.)

SWITCHING CHARACTERISTICS



*C_L includes probe and jig capacitance

TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. Voltage values are with respect to ground terminal.

Fig. A – SWITCHING TIMES

TTL/MSI 9393/5493, 7493
4-BIT BINARY COUNTER

DESCRIPTION – The TTL/MSI 9393/5493, 7493 is a 4-Bit Binary Counter consisting of four master/slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output Q_A must be externally connected to input $\overline{CP}_B$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneously divisions of 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the truth table.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input $\overline{CP}_B$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES

		LOADING
R_0	Reset-Zero Input	1 U.L.
$\overline{CP}_A$	Clock (Active LOW going edge) Input	2 U.L.
$\overline{CP}_B$	Clock (Active LOW going edge) Input	2 U.L.
Q_A, Q_B, Q_C, Q_D	Outputs	10 U.L.

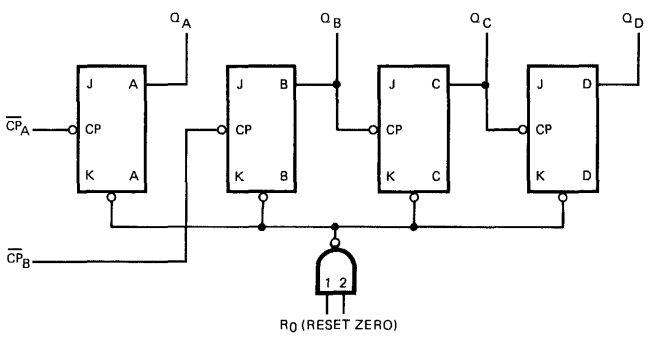
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE (See Notes 1, 2 and 3)

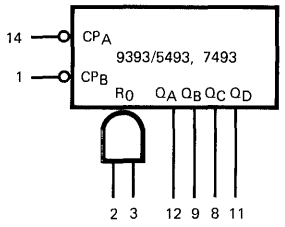
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTES:
1. Output Q_A connected to input $\overline{CP}_B$.
2. To reset all outputs to LOW level both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a LOW level to count.

LOGIC DIAGRAM

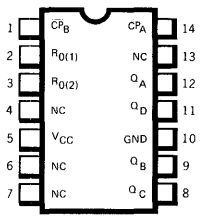


LOGIC SYMBOL

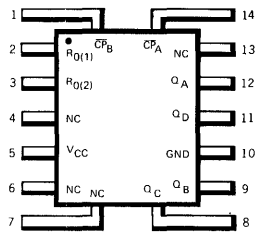


V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 4, 6, 7, 13

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



NC – No Internal Connection
Positive logic: See Truth Table

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9393XM/5493XM			9393XC/7493XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Normalized Fan-Out from Each Output, N (Note 5)			10			10	U.L.
Width of Input Count Pulse, $t_{p(in)}$	50			50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			50			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts			1
V_{IL}	Input LOW Voltage			0.8	Volts			2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA		2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA		1
I_{IH}	Input HIGH Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
	Input HIGH Current at Inputs $\overline{CP}_A$ or $\overline{CP}_B$			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at $R_{0(1)}$ or $R_{0(2)}$ Inputs			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
	Input LOW Current at Inputs $\overline{CP}_A$ or $\overline{CP}_B$			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		4
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9393/5493	V_{CC} = MAX. V_{OUT} = 0 V	5
		−18		−57	mA	9393/7493		
I_{CC}	Supply Current		32	46	mA	9393/5493	V_{CC} = MAX. V_{IN} = 4.5 V	3
			32	53	mA	9393/7493		

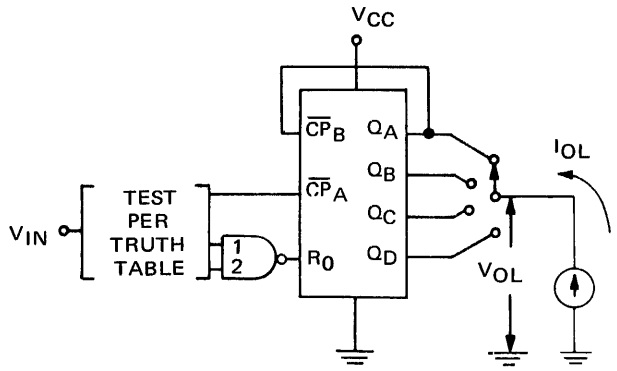
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Frequency of Input Count Pulse	10	18		MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω	
t_{PLH}	Turn Off Delay from Input Count Pulse to Output Q_D		75	135	ns		A
t_{PHL}	Turn On Delay from Input Count Pulse to Output Q_D		75	135	ns		A

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.
(5) Fan-out from output Q_A to input $\overline{CP}_B$ and to 10 additional series 54/74 loads is permitted.

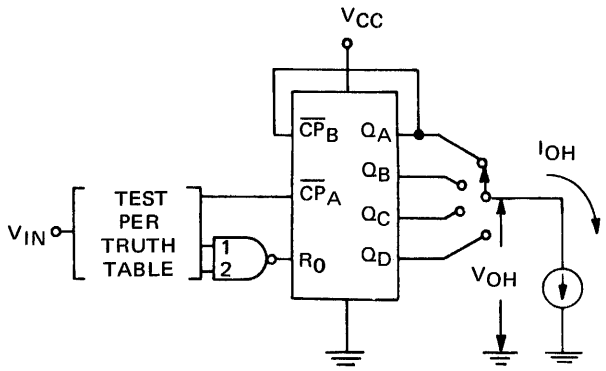
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



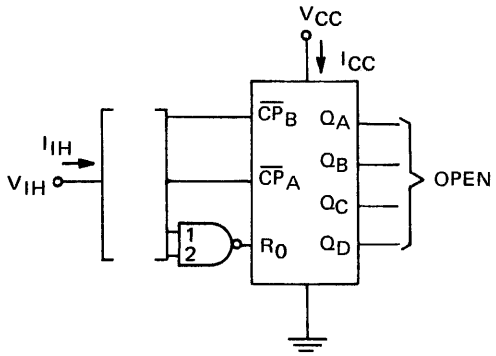
1. Each output is tested in the LOW level state.

Fig. 1



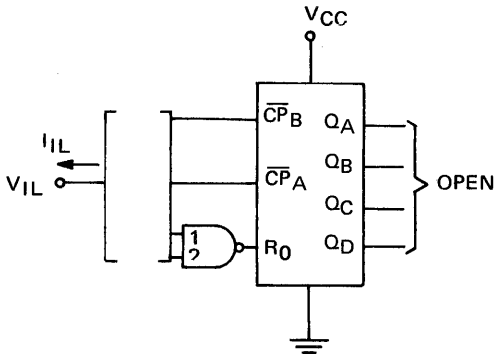
1. Each output is tested in the HIGH level state.

Fig. 2



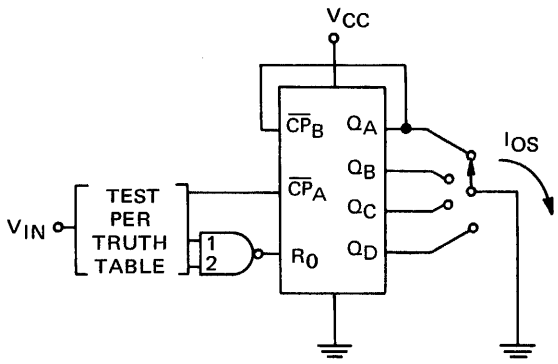
1. Each input is tested separately.
2. When testing $R_{0(1)}$ ground $R_{0(2)}$.
3. When testing $R_{0(2)}$ ground $R_{0(1)}$.
4. When testing I_{CC} all inputs and outputs are open.

Fig. 3



1. Each input is tested separately.
2. When testing $R_{0(1)}$ apply 4.5 V to $R_{0(2)}$.
3. When testing $R_{0(2)}$ apply 4.5 V to $R_{0(1)}$.

Fig. 4



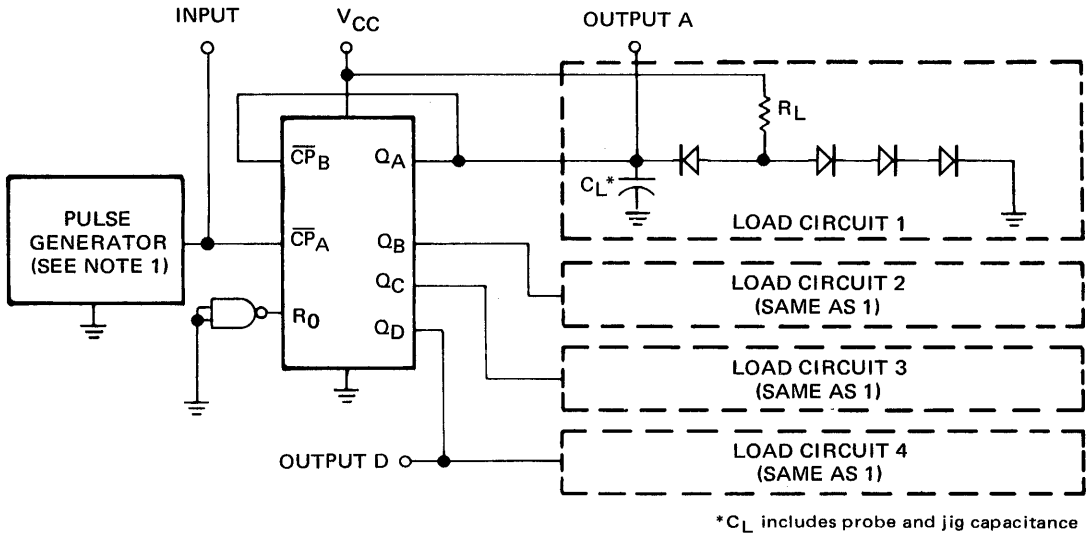
1. Each output is tested in the HIGH level state.

Fig. 5

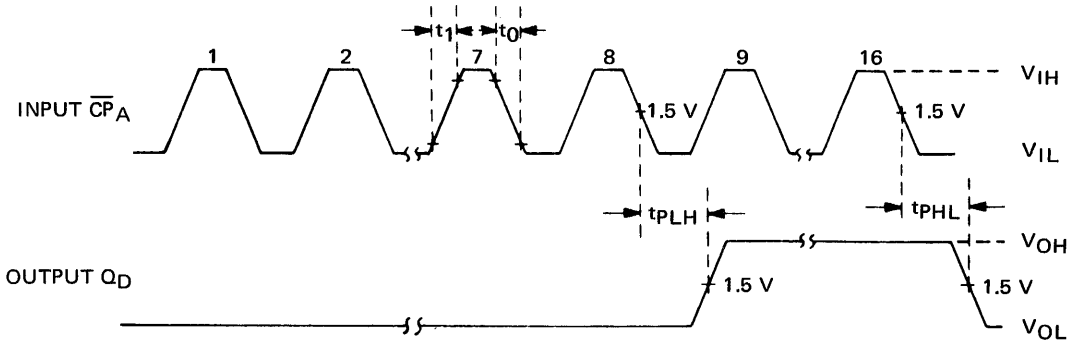
*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS



TEST CIRCUIT



VOLTAGE WAVEFORMS

1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_0 = t_1 \leq 15$ ns, t_p = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\Omega$.
2. Propagation delay = $\frac{t_{PHL} + t_{PLH}}{2}$
3. Voltage values are with respect to ground terminal.

Fig. A — SWITCHING TIMES

8

TTL/MSI 9394/5494, 7494
4-BIT SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9394/5494, 7494 is composed of four RS master/slave flip-flops, four AND-OR-INVERT gates and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the LOW state by applying a HIGH level voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the HIGH state from either of two preset input sources. Preset inputs P_{1A} through P_{1D} are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a LOW level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs P_{2A} through P_{2D} are active.

Transfer of information to the outputs occurs when the clock input goes from a LOW to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input, preset 1, and preset 2 must be at a LOW state when clocking occurs.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

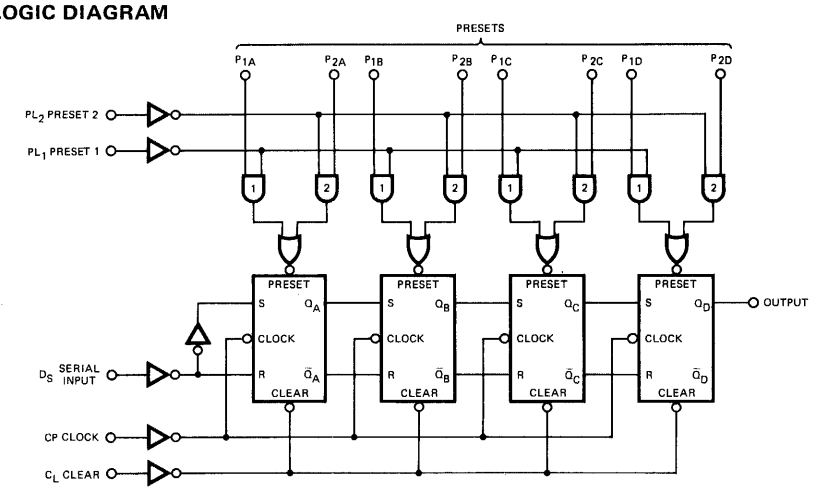
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

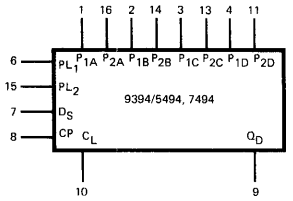
PIN NAMES		LOADING
$P_{1A} - P_{2D}$	Preset Inputs	1 U.L.
PL_1	Preset 1 Input	4 U.L.
PL_2	Preset 2 Input	4 U.L.
D_S	Serial Data Inputs	1 U.L.
CP	Clock Input	1 U.L.
C_L	Clear Input	1 U.L.
Q_D	Serial Data Output	10 U.L.

1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

LOGIC DIAGRAM

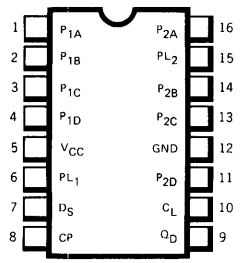


LOGIC SYMBOL

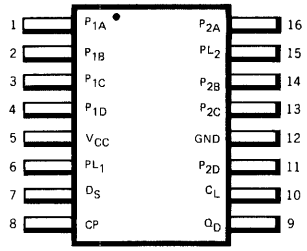


V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



FLAT PAK (TOP VIEW)



Positive Logic: HIGH input to clear sets Q_A, Q_B, Q_C and Q_D to LOW level.

TRUTH TABLE

CLOCK INPUT	CLEAR INPUT	COMMON PRESETS		BIT PRESETS		Q_D
		1	2	1A–1D	2A–2D	
X	H	L	L	Inhibit	Inhibit	L
X	X	H	L	Active	Inhibit	Follows 1D
X	X	L	H	Inhibit	Active	Follows 2D
Active	L	L	L	Inhibit	Inhibit	Follows Serial Input by 4 Bits

Common Presets (PL_1, PL_2) not activated (H) simultaneously X-either H or L.

States of internal Flip-Flops Q_A, Q_B, Q_C, will follow either 1A – 1C or 2A – 2C depending upon common preset condition.

Serial input is overridden except when clocking.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9394XM/5494XM			9394XC/7494XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.5	Volts
Operating Free-Air Temperature Range		–55	25	125	0	25	70	°C
Normalized Fan Out from Output				10			10	U.L.
Width of Clock Pulse, $t_{p(clock)}$		35			35			ns
Width of Preset Pulse, $t_{p(preset)}$		30			30			ns
Width of Clear Pulse, $t_{p(clear)}$		30			30			ns
Serial Input Setup Time,	t_{setup} (HIGH)	35			35			ns
	t_{setup} (LOW)	25			25			ns
Serial Input Hold Time, t_{hold}		0			0			

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = –0.4 mA	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	
I_{IH}	Input HIGH Current at Any Input Except Preset 1 and Preset 2			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Preset 1 and Preset 2			160	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at Any Input Except Preset 1 and Preset 2			–1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
	Input LOW Current at Preset 1 and Preset 2			–6.4	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	–20		–57	mA	9394/5494	V_{CC} = MAX., V_{OUT} = 0 V
		–18		–57	mA	9394/7494	
I_{CC}	Supply Current		35	50	mA	9394/5494	V_{CC} = MAX.
			35	58	mA	9394/7494	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency	10			MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω
t_{PLH}	Turn Off Delay Clock to Output		25	40	ns	
t_{PHL}	Turn On Delay Clock to Output		25	40	ns	
t_{PLH}	Turn Off Delay Preset to Output			35	ns	
t_{PHL}	Turn On Delay Clear to Output			40	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

TTL/MSI 9395/5495, 7495
4-BIT RIGHT-SHIFT, LEFT-SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9395/5495, 7495 Shift Register is composed of four RS master/slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate and six inverters-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logic input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

When a LOW level is applied to the mode control input, the number 1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the RS inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

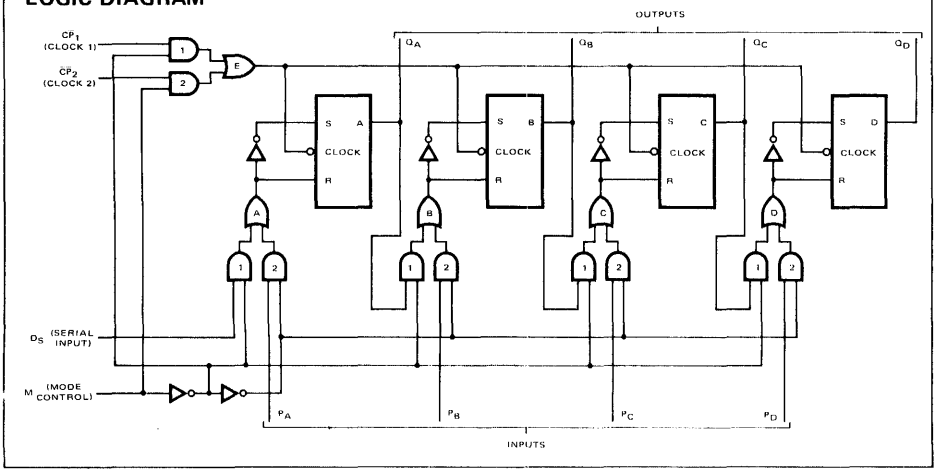
When a HIGH level is applied to the mode control input, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding RS inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a HIGH to a LOW level.

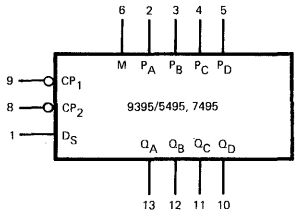
PIN NAMES		LOADING
$\overline{CP}_1$	Clock 1 Input	1 U.L.
$\overline{CP}_2$	Clock 2 Input	1 U.L.
M	Mode Control Input	2 U.L.
P_A, P_B, P_C, P_D	Parallel Data Inputs	1 U.L.
Q_A, Q_B, Q_C, Q_D	Parallel Data Outputs	10 U.L.
D_S	Serial Data Input	1 U.L.

1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW

LOGIC DIAGRAM

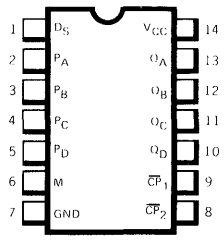


LOGIC SYMBOL

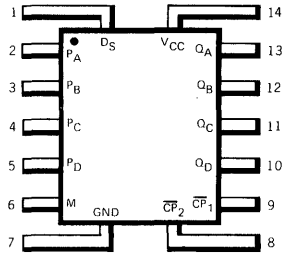


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic:
Mode control = LOW for right shift
Mode control = HIGH for left shift or parallel load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pi n Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9395XM/5495XM			9395XC/7495XC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Width of Clock Pulse $t_{p(clock)}$ (See Fig. A)		20	10		15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Fig. A)		10			10			ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Fig. A)		0			0			ns
LOW Level Setup Time Required at Mode Control (t_1 in Fig. B) (With Respect to Clock 1 Input)		15			15			ns
HIGH Level Setup Time Required at Mode Control (t_2 in Fig. B) (With Respect to Clock 2 Input)		15			15			ns
LOW Level Setup Time Required at Mode Control (t_3 in Fig. B) (With Respect to Clock 2 Input)		5.0			5.0			ns
HIGH Level Setup Time Required at Mode Control (t_4 in Fig. B) (With Respect to Clock 1 Input)		5.0			5.0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	1 & 3
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	2 & 4
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -0.8 mA	1 & 3
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	2 & 4
I_{IH}	Input HIGH Current at Any Input Except Mode Control			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	6
				1.0	mA	V_{CC} = MAX., V_{IN} = 2.4 V	
	Input HIGH Current at Mode Control			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	6
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at Any Input Except Mode Control			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	5
	Input LOW Current at Mode Control			-3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	5
I_{OS}	Output Short Circuit Current (Note 3)	-18		-57	mA	V_{CC} = MAX.	7
I_{CC}	Supply Current	39		63	mA	V_{CC} = MAX.	8

NOTES:

(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.

(2) Typical limits are at V_{CC} = 5.0 V, 25°C.

(3) Not more than one output should be shorted at a time.

(4) Voltage values are with respect to network ground terminal.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
f_{max}	Maximum Clock Frequency	25	36		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω	A
t_{PLH}	Turn Off Delay Clock 1 or Clock 2 to Outputs		18	27	ns		A
t_{PHL}	Turn On Delay Clock 1 or Clock 2 to Outputs		21	32	ns		A

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

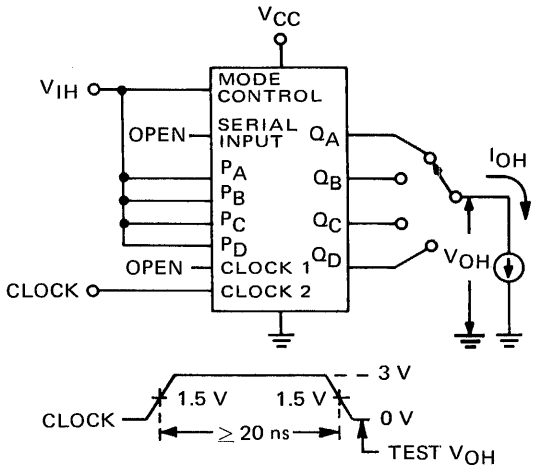


Fig. 1

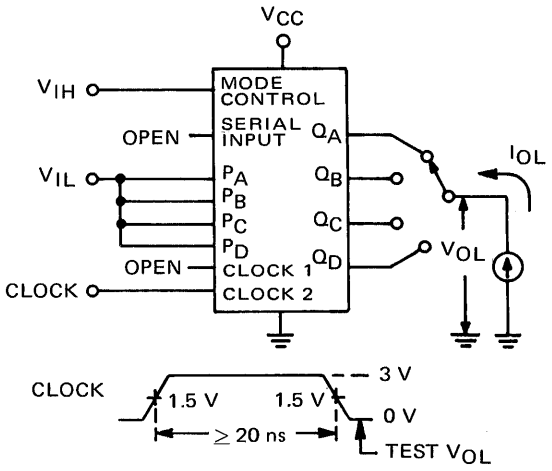


Fig. 2

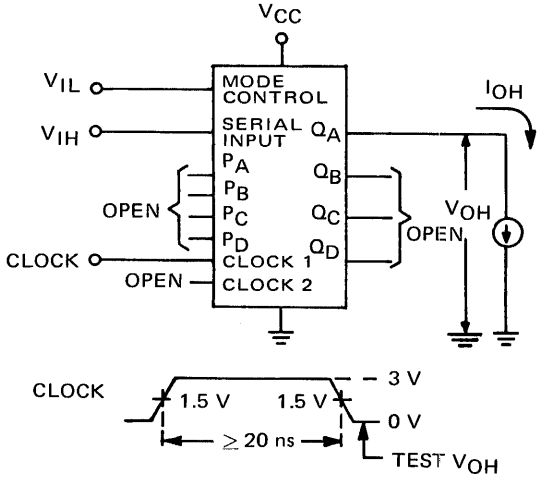


Fig. 3

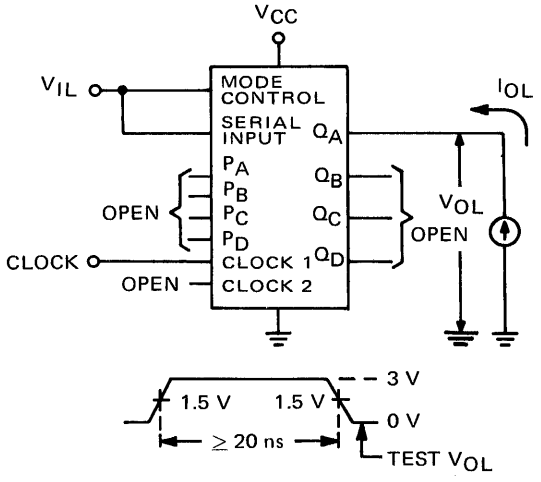
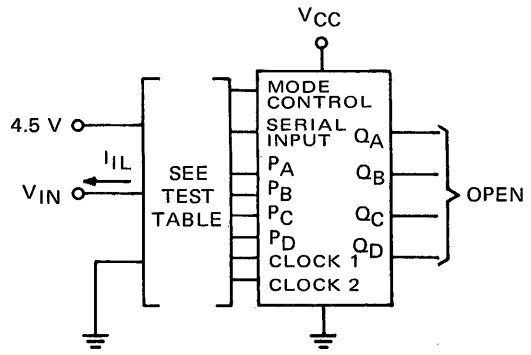


Fig. 4

*Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION (con't.)

DC TEST CIRCUITS*(Continued)

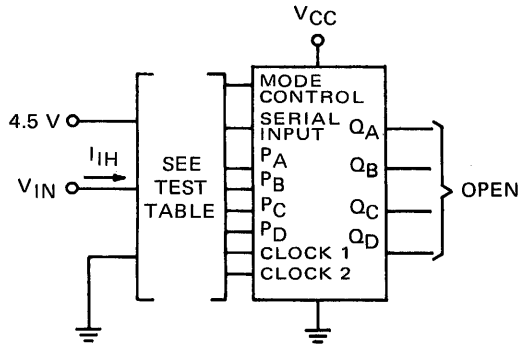


1. Each Input is tested separately.

TEST TABLE

Test	Apply 4.5 V	Apply GND
Mode Control	Clock 2	None
Serial Input	None	Mode Control
Input P_A	Mode Control	None
Input P_B	Mode Control	None
Input P_C	Mode Control	None
Input P_D	Mode Control	None
Clock 1	None	Mode Control
Clock 2	Mode Control	None

Fig. 5



TEST TABLE

Test	Apply 4.5 V	Apply GND
Mode Control	None	Clock 2
Serial Input	Mode Control	None
Input P_A	None	Mode Control
Input P_B	None	Mode Control
Input P_C	None	Mode Control
Input P_D	None	Mode Control
Clock 1	Mode Control	None
Clock 2	None	Mode Control

Fig. 6

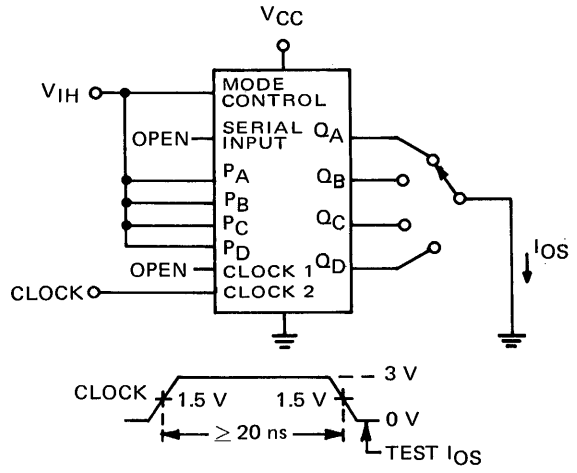


Fig. 7

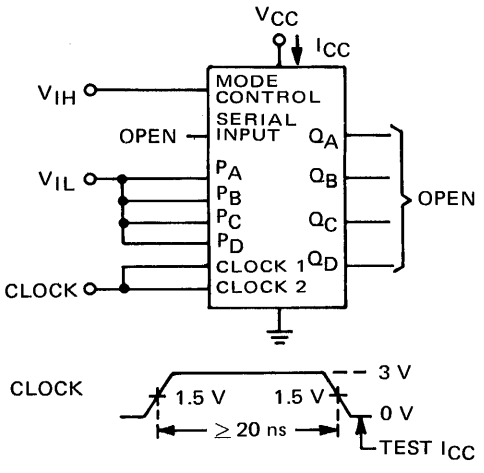
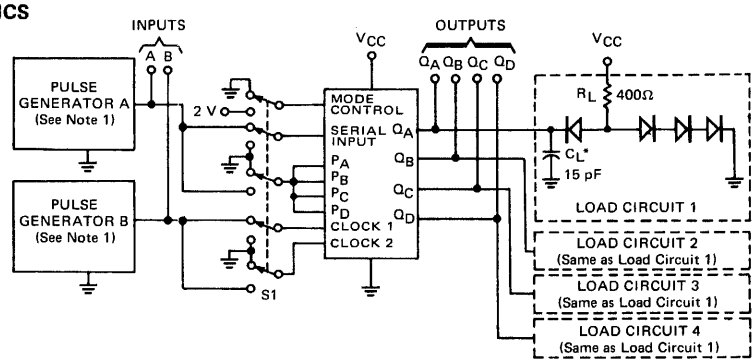


Fig. 8

*Arrows indicate actual direction of current flow.

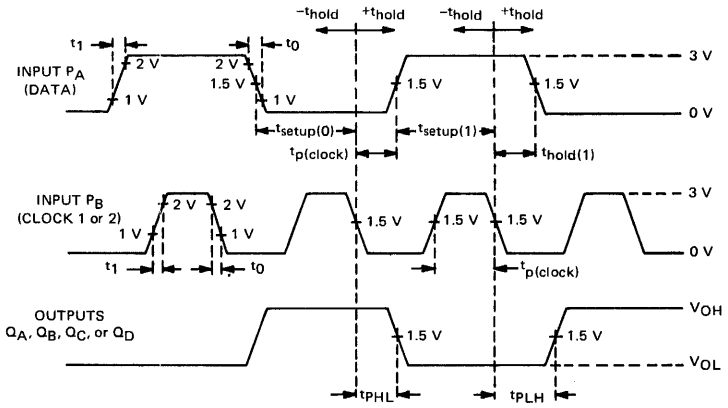
PARAMETER MEASUREMENT INFORMATION (con't.)

SWITCHING CHARACTERISTICS



*C_L includes probe and jig capacitance.

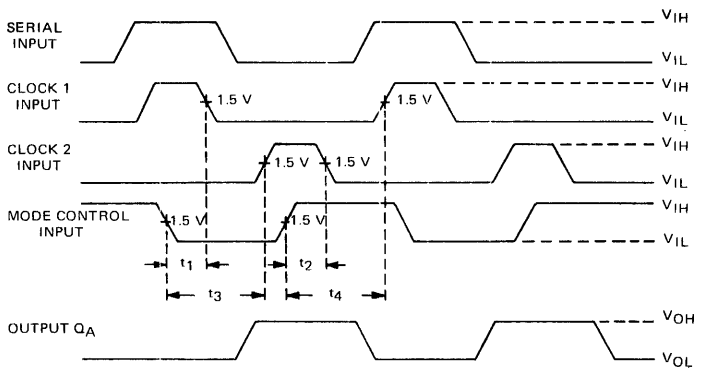
TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generators having the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\Omega$. For pulse generator A: $t_p \geq 20$ ns and PRR = 500 kHz. For pulse generator B: $t_p \geq 15$ ns and PRR = 1 MHz. When testing f_{max} vary PRR.
2. Voltage values are with respect to network ground terminal.

Fig. A SWITCHING TIMES



Note: Input P_A is at V_{IL}.

Fig. B RECOMMENDED MODE CONTROL SETUP TIMES

TTL/MSI 9396/5496, 7496
5–BIT SHIFT REGISTER

DESCRIPTION – The TTL/MSI 9396/5496, 7496 5-Bit Shift Register consists of five RS master/slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the LOW state by applying a low level voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the HIGH state by applying a high level voltage to both the preset input of the specific flip-flop and the common preset input. The parallel enable input is provided to allow setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a LOW level to a HIGH level. Since the flip-flops are RS master/slave circuits, the proper information must appear at the RS inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining RS inputs. The clear input must be at a HIGH level and the preset input must be at a LOW level when clocking occurs.

PIN NAMES		LOADING
PL	Parallel Load Input	5 U.L.
P_A, P_B, P_C, P_D, P_E	Parallel Data Inputs	1 U.L.
D_S	Serial Data Input	1 U.L.
CP	Clock Input	1 U.L.
$\overline{C}_L$	Clear Input	1 U.L.
Q_A, Q_B, Q_C, Q_D, Q_E	Parallel Data Outputs	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

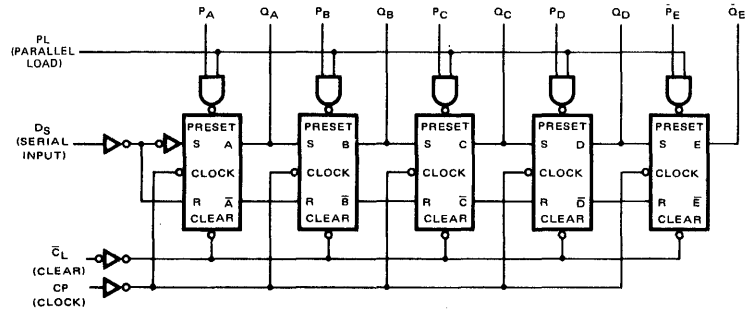
TRUTH TABLE

PRESET COMMON	BIT	$\overline{\text{CLEAR}}$	SERIAL INPUT	CLOCK	OUTPUT	
L	X	L	X	X	L	Clear all output to logical "L".
H	H	H	X	X	H	Preset outputs to 1 input
H	L	H	X	X	L	bit configuration.
L	X	H	H	enable	H	Serial input shift right.
L	X	H	L	enable	L	Serial-to-parallel conversion.

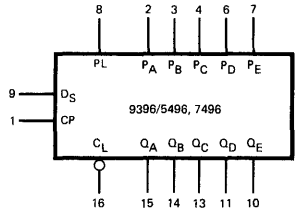
NOTES:
(a) After loading data, set clear to "H" and preset to "L" clock to give parallel to serial conversion.
(b) Information transferred on rising edge of clock pulse.

(c) Do not enable preset and clear simultaneously.
Preset – "H" Clear – "L" = undefined output. Dependent upon which enable is removed first.
(d) X Either logical "L" or logical "H".

LOGIC DIAGRAM

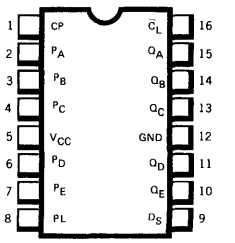


LOGIC SYMBOL

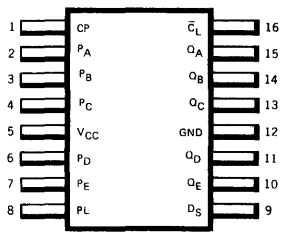


V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive Logic: LOW input at clear sets all outputs to LOW level.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	9396XM/5496XM			9396XC/7496XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C
Width of Clock Pulse, $t_{p(clock)}$	35			35			ns
Width of Preset Pulse, $t_{p(preset)}$	30			30			ns
Width of Clear Pulse, $t_{p(clear)}$	30			30			ns
Serial Input Setup Time, t_{setup}	30			30			ns
Serial Input Hold Time, t_{hold}	0			0			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise noted)

SYMBOL	PARAMETER	LIMITS TYP.			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	(Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	
V_{OH}	Output HIGH Voltage	2.4	3.5		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA	
V_{OL}	Output LOW Voltage		0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	
I_{IH}	Input HIGH Current at Any Input Except Parallel Load			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at Parallel Load			200	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current at Any Input Except Parallel Load			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
	Input LOW Current at Parallel Load			−8.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	9396/5496	V_{CC} = MAX., V_{OUT} = 0 V
		−18		−57	mA	9396/7496	
I_{CC}	Supply Current		48	68	mA	9396/5496	V_{CC} = MAX.
			48	79	mA	9396/7496	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Maximum Clock Frequency	10			MHz	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400Ω
t_{PLH}	Turn Off Delay Clock to Output		25	40	ns	
t_{PHL}	Turn On Delay Clock to Output		25	40	ns	
t_{PLH}	Turn Off Delay Preset or Parallel Load to Output		28	35	ns	
t_{PHL}	Turn On Delay Clear to Output			55	ns	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) This voltage value is with respect to network ground terminal.

TTL/MSI 93141/74141
1-OF-10 DECODER/DRIVER (NIXIE)

DESCRIPTION — The 93141/74141 is a BCD-to-Decimal Decoder Driver that is designed to take a 4-bit BCD code input and drive cold-cathode indicator tubes. This decoder utilizes design improvements that minimize switching transients in order to maintain a stable display.

The segments and numeric designations chosen to represent the decimal numbers are shown below. For binary inputs 10 through 15, the outputs are off. These invalid codes can be used in blanking leading or trailing-edge zeros in a display.

The ten high performance, NPN output transistors have a maximum reverse current of 50μA at 55V. Typical power dissipation is 55 mW.

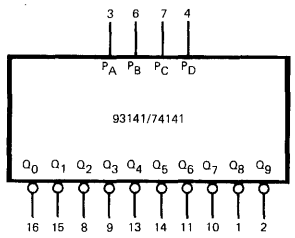
PIN NAMES

		LOADING
P_A	Address Input	1 U.L.
$\overline{P_B}$, P_C, $\overline{P_D}$	Address Input	2 U.L.
$\overline{Q_0}$ to $\overline{Q_9}$	Outputs	*

*See output characteristics.
Max. Current Into Output During "ON" state 7 mA
Output Leakage at 55 V 50 μA

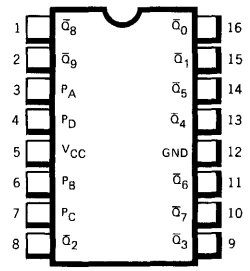
1 U.L. = 40 μA HIGH/1.6 mA LOW.

LOGIC SYMBOL



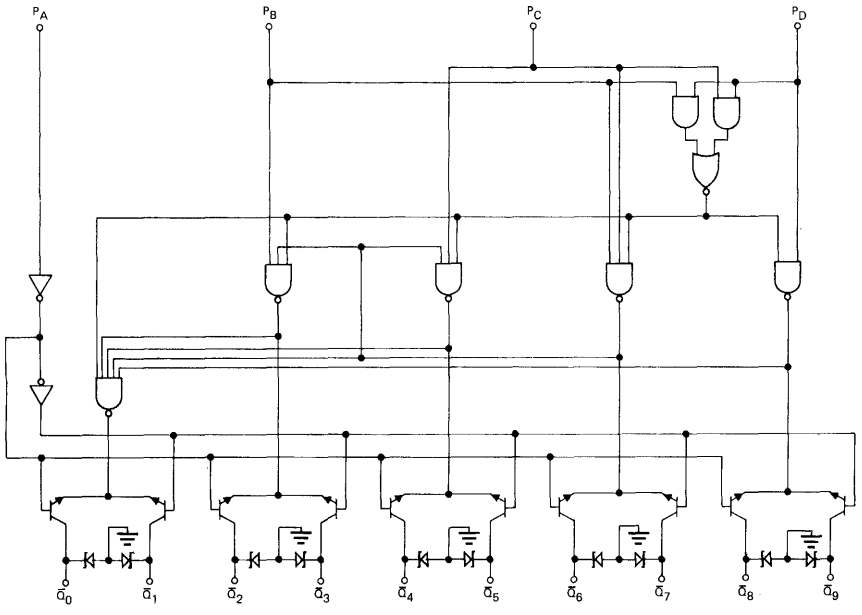
V_{CC} = PIN 5
GND = PIN 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



Positive Logic: See Truth Table

LOGIC DIAGRAM



TRUTH TABLE

INPUT				OUTPUT
P_D	P_C	P_B	P_A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = HIGH level,
L = LOW level.
†All other outputs are off

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	0°C to 70°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	93141XC/74141XC			UNITS
	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 3)	4.75	5.0	5.75	Volts
Operating Free Air Temperature Range	0	25	70	°C
Output Voltage (See Notes 3 & 4)			65	V

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

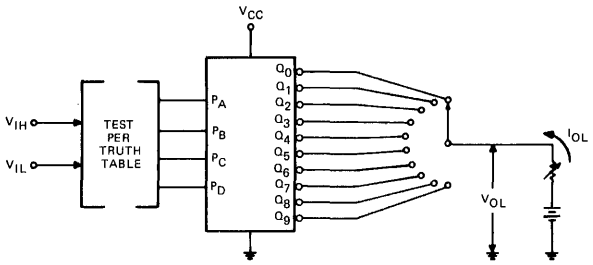
ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	1 & 2
V_{OL}	Output LOW Voltage			2.5	Volts	V_{CC} = MIN., I_{OL} = 7.0 mA	1
V_{OH}	Output HIGH Voltage for input counts 0 thru 9	60			Volts	V_{CC} = MAX., I_{OH} = 0.5 mA	2
I_{OH}	Output HIGH Current			50	µA	V_{CC} = MAX., V_{OUT} = 55 V	2
	Output HIGH Current for input counts 10 thru 15			5.0	µA	V_{CC} = MAX., V_{OUT} = 30 V	2
I_{IH}	Input HIGH Current at P_A			40	µA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
	Input HIGH Current at P_B, P_C, or P_D			80	µA	V_{CC} = MAX., V_{IN} = 2.4 V	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current Into P_A			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	4
	Input LOW Current Into P_B, P_C, or P_D			-3.2	mA		
I_{CC}	Supply Current		16	25	mA	V_{CC} = MAX.	3

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Voltage values are with respect to network ground terminal.
(4) This is the maximum voltage which should be applied to any output when it is in the off state.

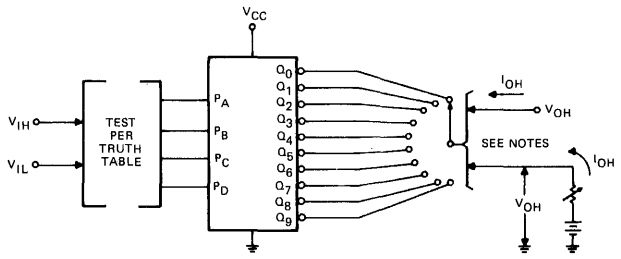
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



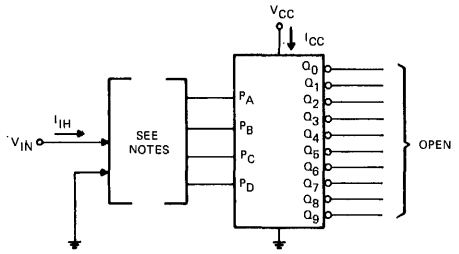
Each output is tested separately.

Fig. 1 V_{IH}, V_{IL}, V_{OL}



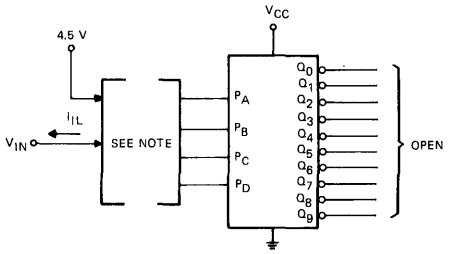
1. Each output is tested separately.
2. V_{OH} is tested at I_{OH} = 0.5 mA and I_{OH} is tested at V_{OH} = 55 V for all inputs counts. I_{OH} is tested also at V_{OH} = 30 V for input counts 10 through 15.

Fig. 2 V_{IH}, V_{IL}, I_{OH}, V_{OH}



1. When testing I_{IH}, each input is tested separately with all other inputs grounded.
2. When testing I_{CC}, all inputs are grounded.

Fig. 3 I_{IH}, I_{CC}



Each input is tested separately, with all other inputs at 4.5 V.

Fig. 4 I_{IL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

APPLICATIONS

GENERAL – When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

DRIVING INDICATOR TUBES – As shown in Figure 5, the 93141/74141 requires no external components for driving cold-cathode indicator tubes. The versatility here is limited only by the system capability to control the data inputs.

A suggested method for blanking extraneous zeros is shown in Figure 6. Any input count above decimal 9 may be used for blanking. In the following application decimal 12 is used. When the most significant bit (MSB) or the least significant bit (LSB) is decimal 0(0000), that indicator is blanked while decimal 12 (binary 1100) is applied to the 93141/74141 inputs causing all the outputs to be off. If the MSB or LSB is decimal 0 and being blanked, this signal is gated with and blanks the next smaller digit. This scheme is easily expandable to n digits.

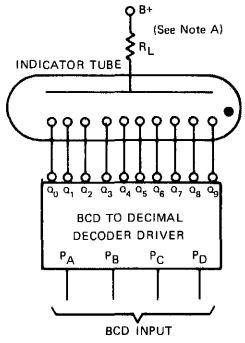
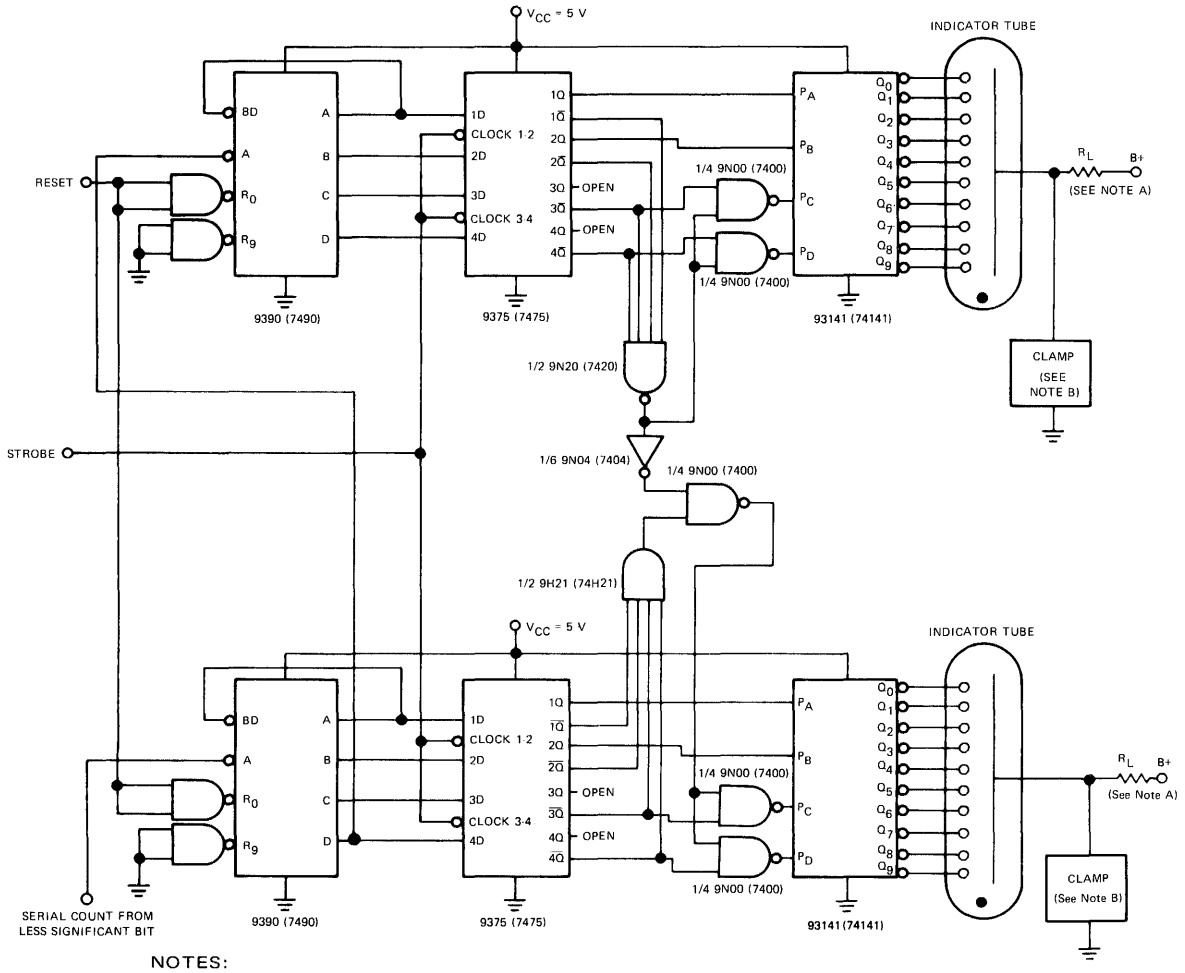


Fig. 5



NOTES:

A. Values for B+ and R_L are as specified by the tube manufacturer.

B. Blanking is assured only if the anode of the indicator tube is clamped at 150 volts maximum.

Fig. 6

TTL/MSI 93150/54150, 74150
93151/54151, 74151•93152/54152, 74152
16-INPUT AND 8-INPUT MULTIPLEXER

DESCRIPTION – The 93150/54150, 74150 is a 16-Input Multiplexer which features active LOW strobe and internal select decoding. A HIGH at the strobe input forces the output HIGH regardless of input conditions.

The 93151/54151, 74151 is an 8-Input Multiplexer with active LOW strobe, internal select decoding and complementary outputs.

The 93152/54152, 74152 is an 8-Input Multiplexer with internal select decoding and a single inverted output.

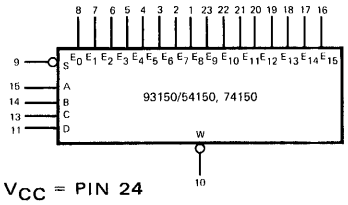
In each of the multiplexers data is routed from a particular input to the output according to the binary code applied to the select inputs.

Typical power dissipations are: 93150/54150, 74150 – 200 mW; 93151/54151, 74151 – 145 mW; 93152/54152, 74152 – 130 mW.

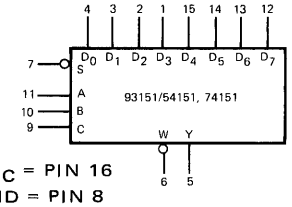
PIN NAMES		LOADING
E_0 to E_{15}	Data Inputs	1 U.L.
D_0 to D_7	Data inputs	1 U.L.
$\overline{S}$	Strobe (Enable) Input	1 U.L.
A, B, C, D	Data Select Inputs	1 U.L.
$\overline{W}$	Data Output	10 U.L.
Y	Data Output	10 U.L.

NOTE: 1 U.L. = 40 μA HIGH/1.6 mA LOW.

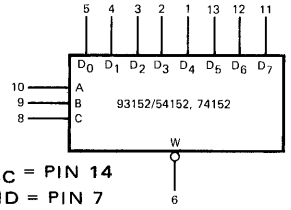
LOGIC SYMBOLS



V_{CC} = PIN 24
GND = PIN 12

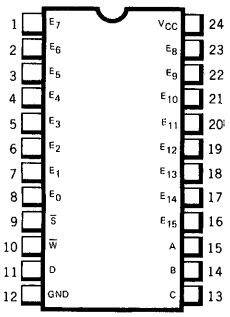


V_{CC} = PIN 16
GND = PIN 8

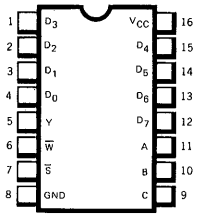


V_{CC} = PIN 14
GND = PIN 7

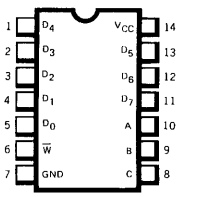
CONNECTION DIAGRAMS
DIP (TOP VIEWS)*



93150/54150, 74150



93151/54151, 74151

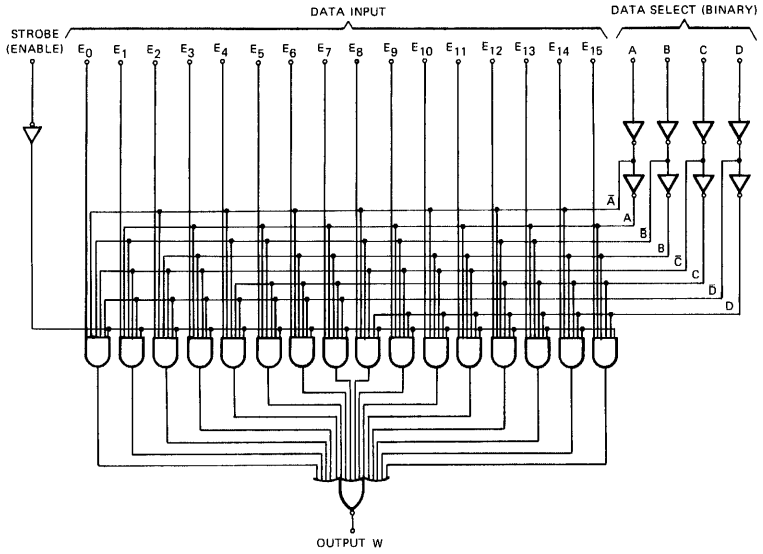


93152/54152, 74152

*Pin assignments for these circuits are the same for all packages.

LOGIC DIAGRAMS

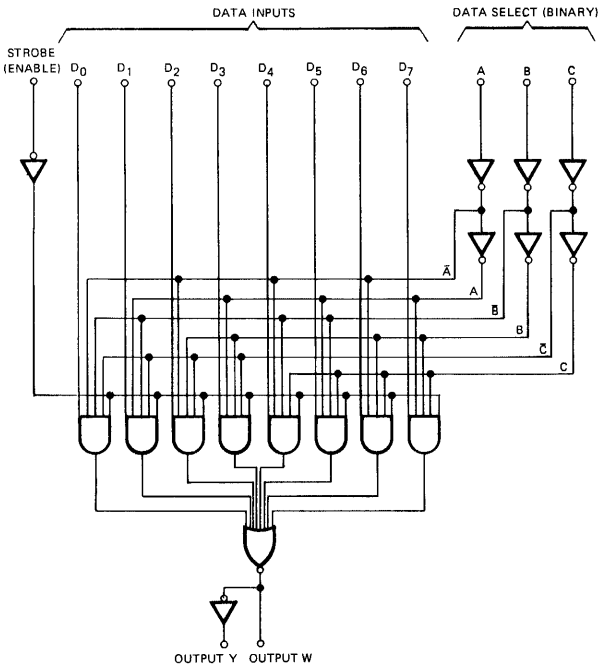
93150/54150, 74150



Positive Logic

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7 + \bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

93151/54151, 74151

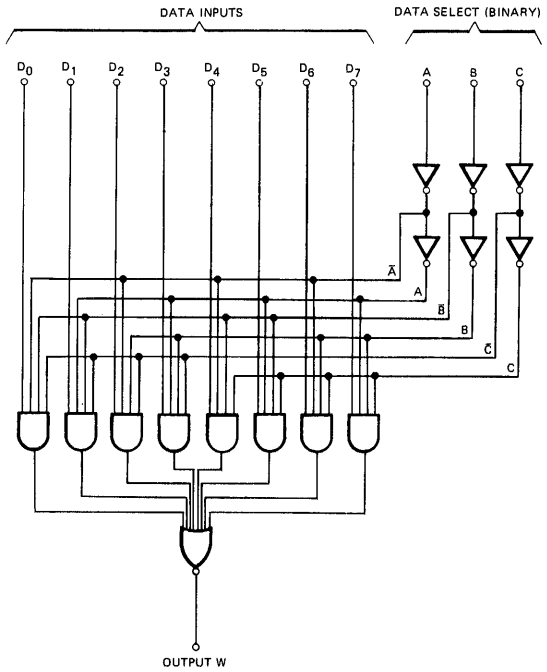


Positive Logic

$$Y = \bar{S}(\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}B\bar{C}D_2 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7)$$

$$W = \bar{Y}$$

93152/54152, 74152



Positive Logic

$$W = (\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7)$$

TRUTH TABLES

93150/54150, 74150

INPUTS																		OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

When used to indicate an input condition, X = LOGICAL H or LOGICAL L.

93151/54151, 74151 AND 93152/54152, 74152

INPUTS											OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	H	X	X	X	X	X	X	X	X	L	H
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

NOTES:
1. 54151, 74151 only.
2. When used to indicate an input, X = irrelevant.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93150XM/54150XM 93151XM/54151XM 93152XM/54152XM			93150XC/74150XC 93151XC/74151XC 93152XC/74152XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	LOW Level			10			10	U.L.
	HIGH Level			20			20	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage		2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = -800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1 & 2
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1 & 2
I_{IH}	Input HIGH Current (Each Input)			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current (Each Input)			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		3
I_{OS}	Output Short Circuit Current (Note 3)	-20		-55	mA	93150/54150, 93151/54151, 93152/54152, V_{CC}=MAX., V_{out}=0V		4
		-18		-55	mA	93150/74150, 93151/74151, 93152/74152, V_{CC}=MAX., V_{out}=0V		
I_{CC}	Supply Current		40	68	mA	93150/54150, 74150	V_{CC} = MAX. V_{IN} = 4.5 V	5
			29	48	mA	93151/54151, 74151		
			26	43	mA	93152/54152, 74152		

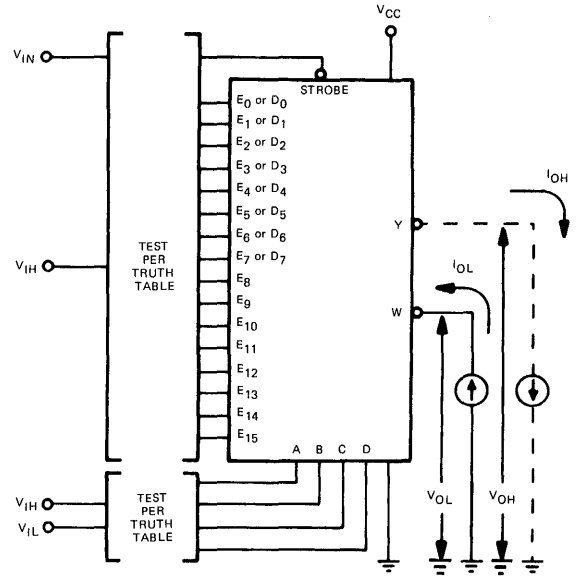
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	TEST FIGURE
t_{PHL}	A, B, or C Input to Y Output,		20	30	ns	V_{CC} = 5.0 V, C_L = 15 pF, R_L = 400 Ω	A
t_{PLH}	4 Levels		35	52	ns		
t_{PHL}	A, B, C, or D Input to W		22	33	ns		
t_{PLH}	Output, 3 Levels		22	35	ns		
t_{PHL}	Strobe Input to Y Output		19	30	ns		
t_{PLH}			35	52	ns		
t_{PHL}	Strobe Input to W Output		21	30	ns		
t_{PLH}			15.5	24	ns		
t_{PHL}	D_0 thru D_7 Input to Y		16	24	ns		
t_{PLH}	Output		19	29	ns		
t_{PHL}	E_0 thru E_{15}, D_0 thru D_7		8.5	14	ns		
t_{PLH}	Input to W Output		13	20	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommmended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output of the 93151/54151, 74151 should be shorted at a time.

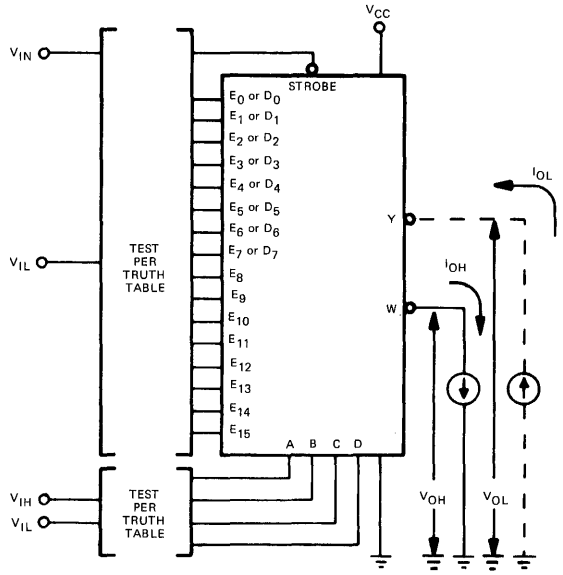
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



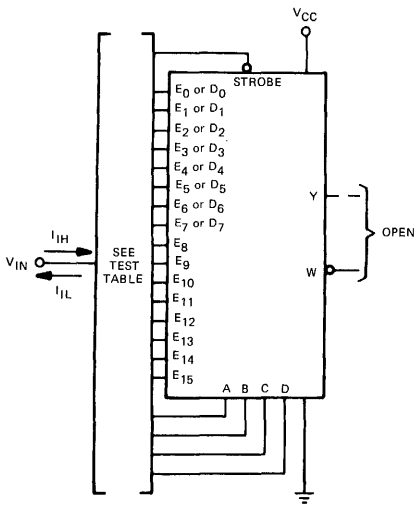
1. V_{IL} is applied to STROBE; 8-4-2-1 code is applied to A, B, C, D; and input/output condition is tested for each step of the code.
2. V_{IH} is applied to STROBE at which time V_{OL} is measured at Y and V_{OH} is measured at W.

Fig. 1



1. V_{IL} is applied to STROBE; 8-4-2-1 is applied to A, B, C, D; and input/output condition is tested for each step of the code.

Fig. 2



INPUT CONDITIONS				TEST	
A	B	C	D	I_{IL}	I_{IH}
L	L	L	L	E_0 or D_0	E_{15} or D_7
H	L	L	L	E_1 or D_1	E_{14} or D_6
L	H	L	L	E_2 or D_2	E_{13} or D_5
H	H	L	L	E_3 or D_3	E_{12} or D_4
L	L	H	L	E_4 or D_4	E_{11} or D_3
H	L	H	L	E_5 or D_5	E_{10} or D_2
L	H	H	L	E_6 or D_6	E_9 or D_1
H	H	H	L	E_7 or D_7	E_8 or D_0
L	L	L	H	E_8	E_7
H	L	L	H	E_9	E_6
L	H	L	H	E_{10}	E_5
H	H	L	H	E_{11}	E_4

INPUT CONDITIONS				TEST	
A	B	C	D	I_{IL}	I_{IH}
L	L	H	H	E_{12}	E_3
H	L	H	H	E_{13}	E_2
L	H	H	H	E_{14}	E_1
H	H	H	H	E_{15}	E_0
L				A	
	L			B	
		L		C	
			L	D	
H					A
	H				B
		H			C
			H		D

1. When testing strobe input, all other inputs are open.

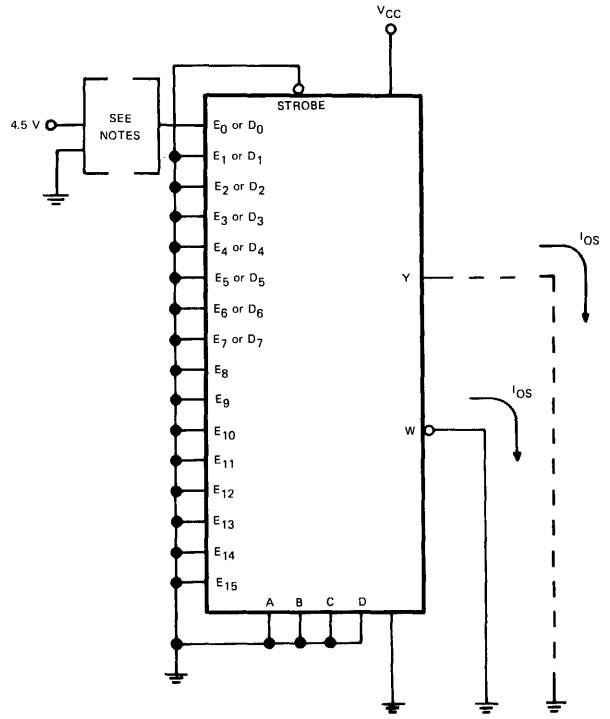
Fig. 3

*Arrows indicate actual direction of current flow. Tests as shown, are for the 93150/54150, 74150. Identical tests as applicable are performed for the 93151/54151, 74151 and 93152/54152, 74152.

8

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS* (Continued)



1. When testing W output, apply GND to D_0 and E_0 input.
2. When testing Y output of 93151/54151, 74151 apply 4.5 V to D_0 and measure I_{OS}.

Fig. 4

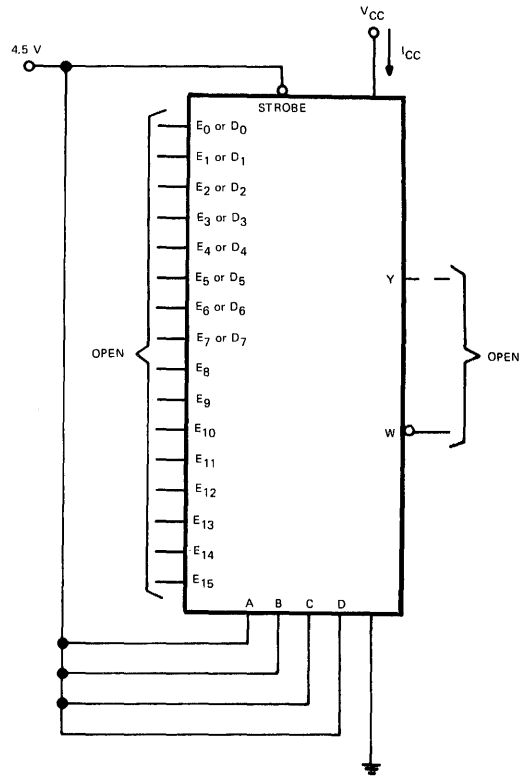
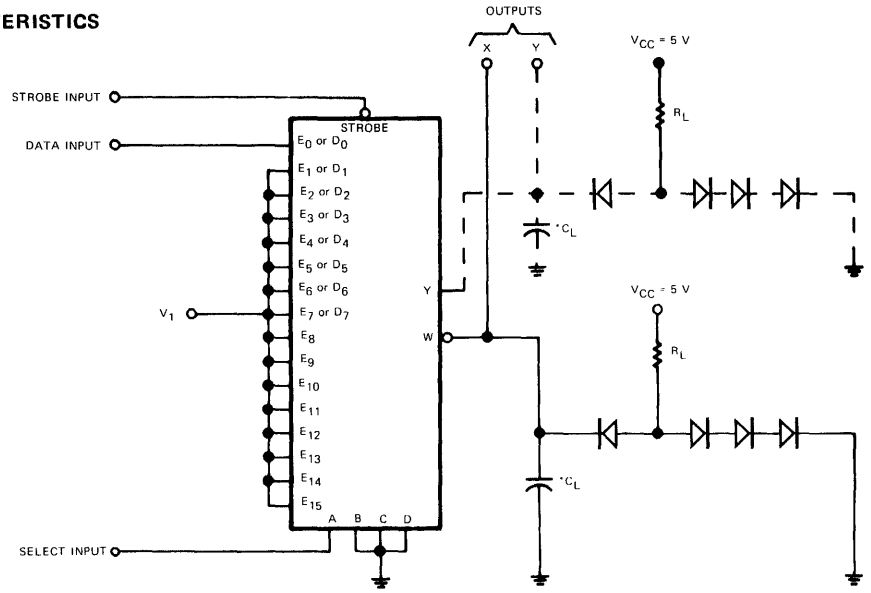


Fig. 5

*Arrows indicate actual direction of current flow. Tests as shown, are for the 93150/54150, 74150. Identical tests as applicable are performed for the 93151/54151, 74151 and 93152/54152, 74152.

SWITCHING CHARACTERISTICS

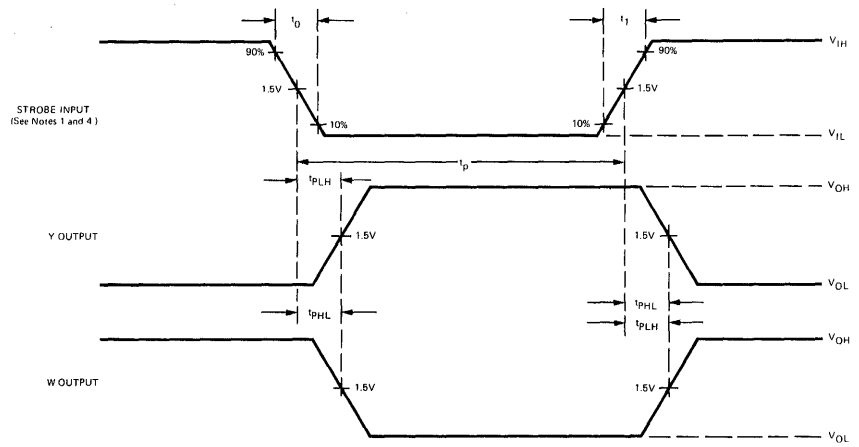


*C_L Includes probe and jig capacitance.

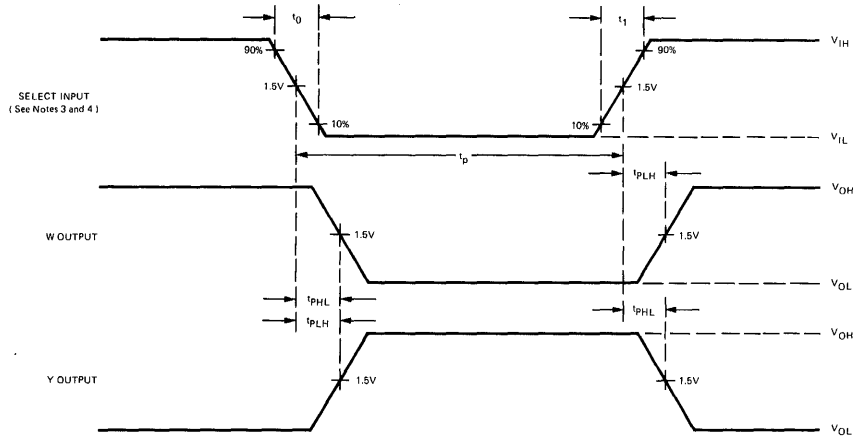
Fig. A SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

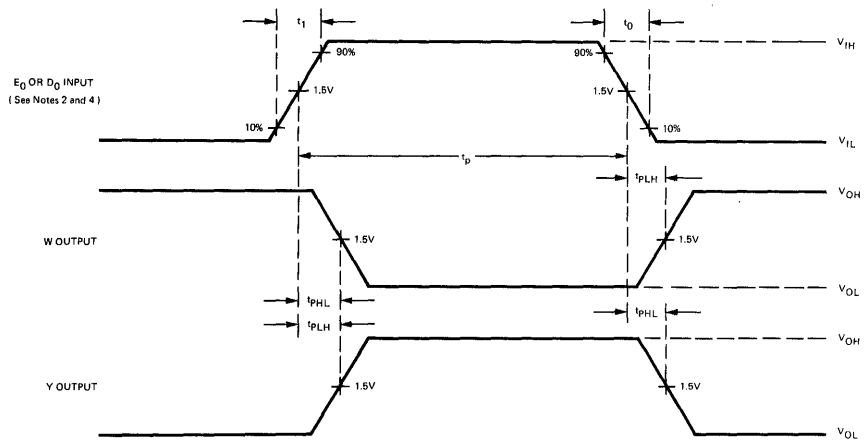
SWITCHING CHARACTERISTICS (cont'd)



STROBE-TO-OUTPUT VOLTAGE WAVEFORMS



SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS



DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

NOTES:

1. When measuring strobe to output times select input is at a LOW level, E_0 or D_0 is at a HIGH level, V_1 = 4.5 V.
2. When measuring dtat input-to-output times strobe and select inputs are at a LOW level and V_1 = 4.5 V.
3. When measuring select input-to-output times strobe input is at a LOW level, data input is at a HIGH level and V_1 = 0.
4. The input pulse has the following V_{IL} characteristics: V_{IH} = 3 V, V_{IL} = 0 V; $t_1 = t_0$ = 10 ns, PRR = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 50\Omega$.

Fig. A SWITCHING TIMES

†Tests, as shown, are for the 93150/54150, 74150. Identical tests as spplicable are performed for the 93151/54151, 74151 and 93152/54152, 74152.

TTL/MSI 93153/54153, 74153
DUAL 4-INPUT DATA SELECTOR/MULTIPLEXER

DESCRIPTION — The 93153/94153, 74153 is a monolithic, high speed, Dual 4-Input Digital Multiplexer. It consists of two multiplexing circuits with separate strobe inputs for each of the two 4-line sections, and with common input select logic. Active pull up outputs ensure high drive and high speed performance with a full fan out of 10 unit loads in the LOW state. Typical power dissipation is 180 mW.

PIN NAMES		LOADING
1G, 2G, $1C_{0-3}$, $2C_{0-3}$, A, B	Inputs	1 U.L.
1Y, 2Y	Outputs	10 U.L.

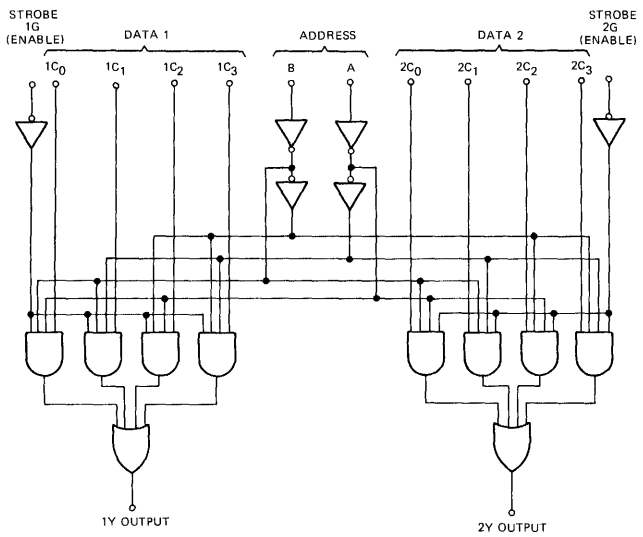
1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE

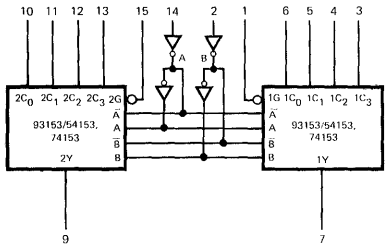
ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C_0	C_1	C_2	C_3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs A and B are common to both sections
H = HIGH level, L = LOW level, X = irrelevant

LOGIC DIAGRAM

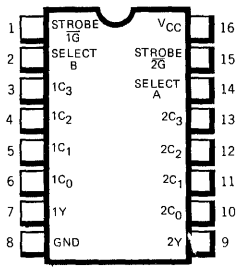


LOGIC SYMBOL

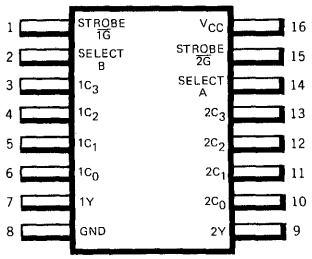


V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAM DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive Logic: See Truth Table.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93153XM/54153XM			93153XC/74153XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage		1 & 2
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage		1 & 2
V_{OH}	Output HIGH Voltage	2.4	3.1		Volts	V_{CC} = MIN., I_{OH} = -800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
V_{OL}	Output LOW Voltage		0.2	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		2
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 (each input)		3
I_{OS}	Output Short Circuit Current (Note 3)	-20		-55	mA	93153/54153	V_{CC} = MAX.	4
		-18		-57	mA	93153/74153		
I_{CCL}	Supply Current LOW		36	52	mA	93153/54153	V_{CC} = MAX.	5
			36	60	mA	93153/74153		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Data Input to Y Output		12	18	ns	V_{CC} = 5.0 V, C_L = 30 pF, R_L = 400 Ω	A
t_{PHL}			15	23			
t_{PLH}	Address Input to Y Output		22	34	ns		
t_{PHL}			22	34			
t_{PLH}	Strobe Input to Y Output		19	30	ns		
t_{PHL}			15	23			

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*

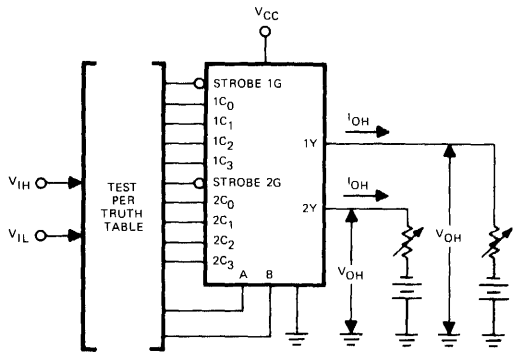


Fig. 1 V_{IH}, V_{IL}, V_{OH}

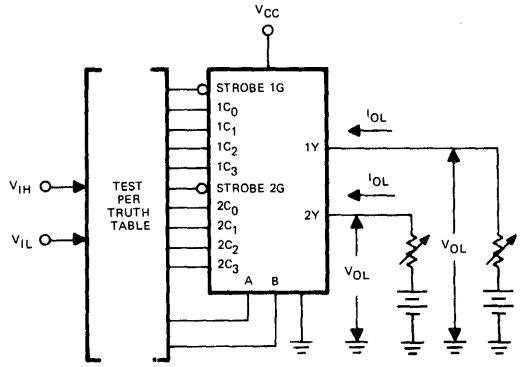
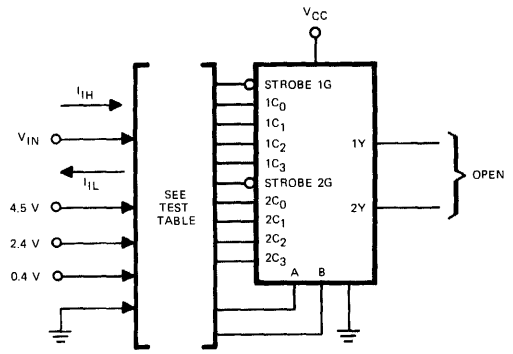


Fig. 2 V_{IH}, V_{IL}, V_{OL}



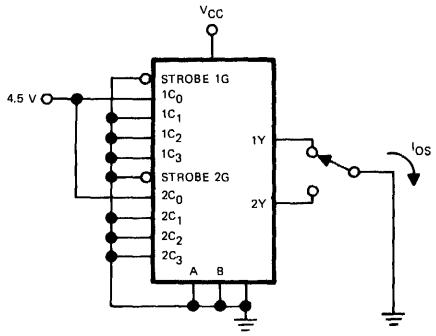
TEST TABLE

INPUT CONDITIONS				APPLY V_{IN}	
B	A	1G	2G	TEST I_{IL}	TEST I_{IH}
L	L	H	H		$1C_3$, $2C_3$
L	H	H	H		$1C_2$, $2C_2$
H	L	H	H		$1C_1$, $2C_1$
H	H	H	H		A,B, 1G, 2G, $1C_0$, $2C_0$
L	L	L	L	A,B, 1G, 2G, $1C_0$, $2C_0$	
L	H	L	L	$1C_1$, $2C_1$	
H	L	L	L	$1C_2$, $2C_2$	
H	H	L	L	$1C_3$, $2C_3$	

H = 2.4 V, L = 0.4 V

Note: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

Fig. 3 I_{IH}, I_{IL}



Note: Each output is tested separately.

Fig. 4 I_{OS}

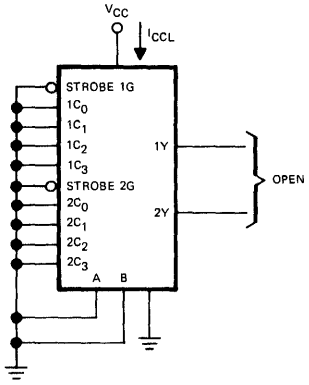
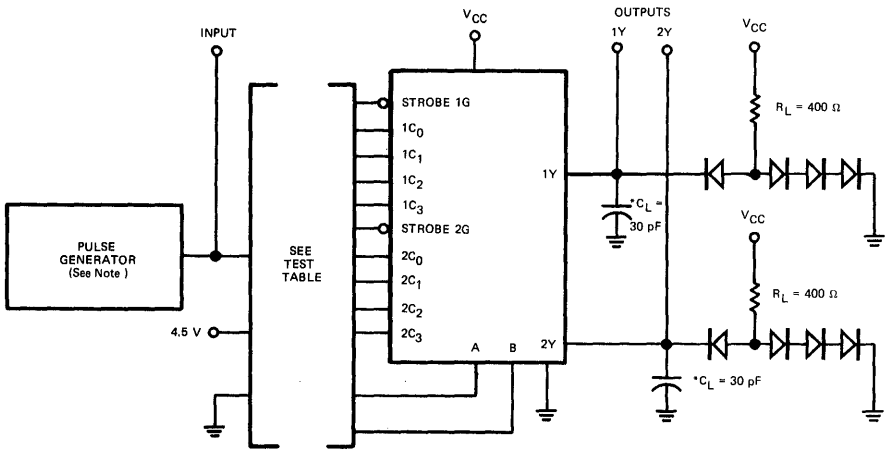


Fig. 5 I_{CCL}

*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

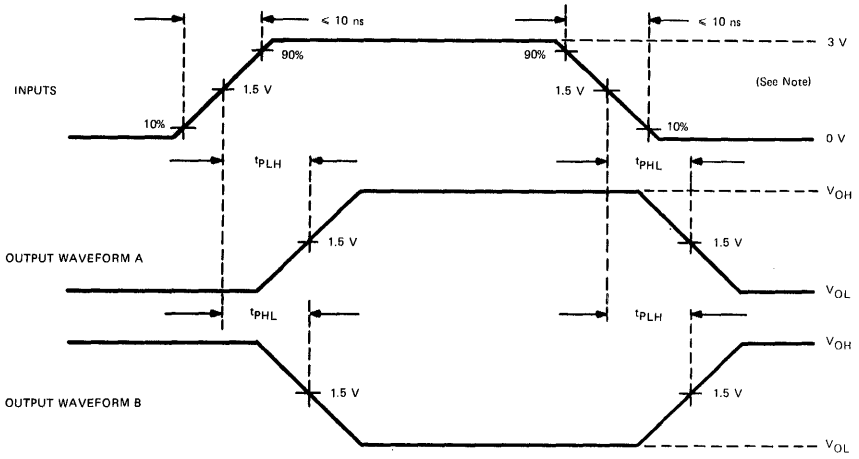
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



*Includes probe and jig capacitance.

TEST CIRCUIT



NOTE: The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.

VOLTAGE WAVEFORMS

TEST TABLE

INPUTS							OUTPUT Y WAVEFORM
B	A	C_0	C_1	C_2	C_3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5V	X	INPUT	X	X	GND	A
4.5V	GND	X	X	INPUT	X	GND	A
4.5V	4.5V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5V	X	X	GND	A
INPUT	GND	GND	X	4.5V	X	GND	A
GND	GND	4.5V	X	X	X	INPUT	B

X = irrelevant

Fig. A SWITCHING TIMES

TTL/MSI 93164/54164, 74164

8-BIT SERIAL TO PARALLEL CONVERTER

TO BE ANNOUNCED

DESCRIPTION – The 93164/54164, 74164 are 8-Bit Shift Registers with gated serial inputs and an asynchronous clear facility. The gated serial inputs (A and B) permit control over incoming data, as a LOW at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the LOW level at the next clock pulse. A HIGH level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is HIGH, but only information meeting the setup requirements will be entered. Clocking occurs on the LOW to HIGH level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects and are buffered to present one TTL load.

PIN NAMES		LOADING
CP	Clock Pulse Input	1 U.L.
$\overline{C}_L$	Clear Input	1 U.L.
A, B	Serial Inputs	1 U.L.
Q_A to Q_H	Parallel Outputs	5 U.L.

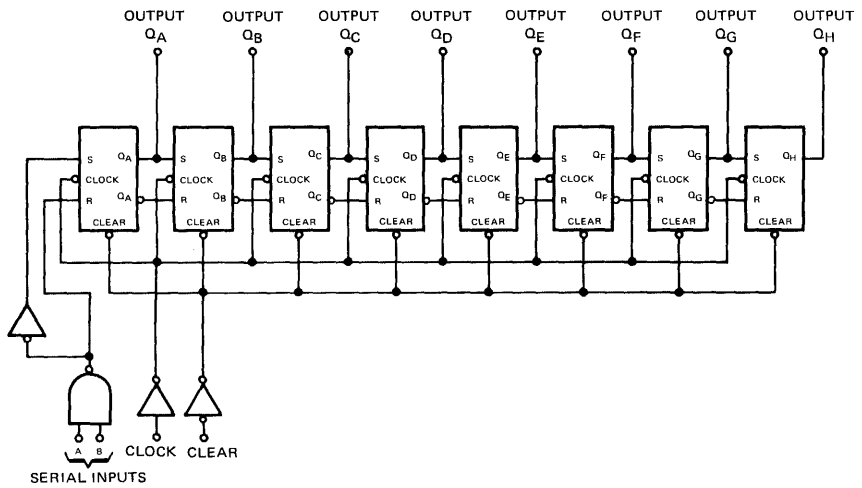
1 Unit Load (U.L.) = 40μA HIGH/1.6mA LOW.

TRUTH TABLE

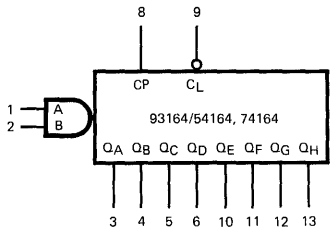
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

LOGIC DIAGRAM

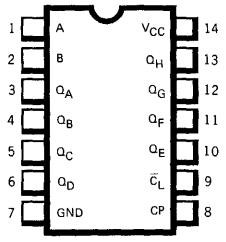


LOGIC SYMBOL

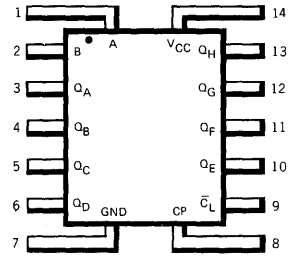


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOW input to clear resets all outputs to the LOW level.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93164XM/54164XM			93164XC/74164XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Logic Level			10			10	U.L.
	LOW Logic Level			5.0			5.0	
Input Clock Frequency, f_{CLOCK}		0		25	0		25	MHz
Width of Clock or Clear Input Pulse t_{PW}		20			20			ns
Data Setup Time, t_{setup} (See Fig. A)		15			15			ns
Data Hold Time, t_{HOLD} (See Fig. A)		0			0			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

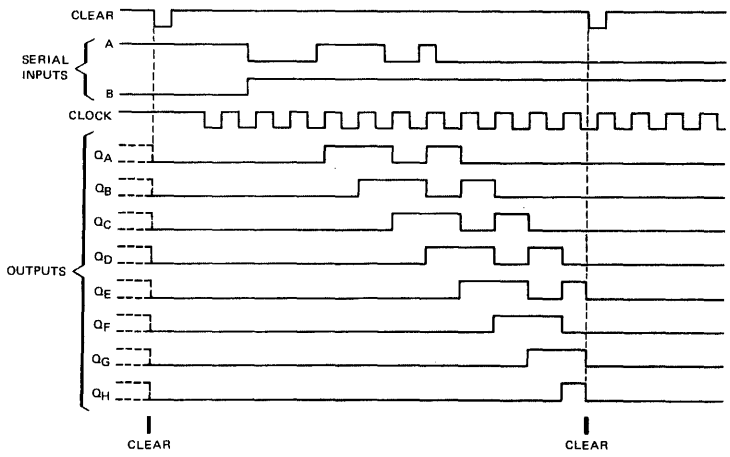
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed V_{IH}	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed V_{IL}	
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MAX., I_{IN} = −12 mA	
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −0.4 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 8.0 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at Maximum Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	−10		−27.5	mA	93164/54164	V_{CC} = MAX.
		−9.0		−27.5	mA	93164/74164	
I_{CC}	Supply Current		30		mA	V_{IN}(clock) = 0.4V	V_{CC} = MAX. (Note 4)
			37	54	mA	V_{IN}(clock) = 2.4V	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN.	TYP.	MAX.			
f_{max}	Maximum Input Count Frequency	25	36		MHz	C_L = 15 pF	V_{CC} = 5.0 V, R_L = 800Ω (See Fig. A)
t_{PHL}	Turn On Delay Clear to Outputs		24	36	ns	C_L = 15 pF	
			28	42		C_L = 50 pF	
t_{PLH}	Turn Off Delay Clock to Outputs	8.0	17	27	ns	C_L = 15 pF	
		10	20	30		C_L = 50 pF	
t_{PHL}	Turn On Delay Clock to Outputs	10	21	32	ns	C_L = 15 pF	
		10	25	37		C_L = 50 pF	

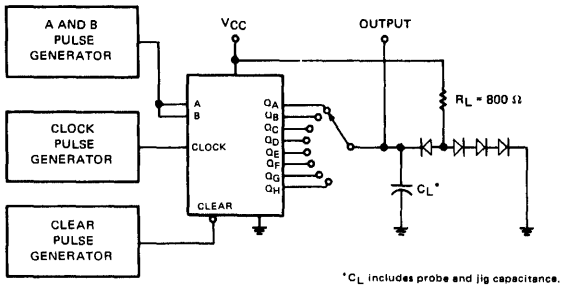
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than two outputs should be shorted at a time.
(4) Measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR AND INHIBIT SEQUENCES

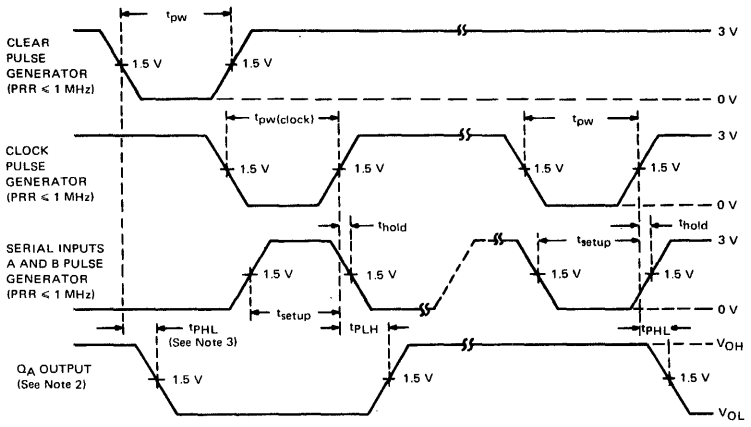


PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generators have the following characteristics: $t_r \leq 10$ns, $t_f \leq 10$ns, duty cycle ≤ 50%, $Z_{OUT} = 50\Omega$.
2. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
3. Outputs are set to the HIGH level prior to the measurement of t_{PHL} from the clear input.

Fig. A SWITCHING TIMES

TTL/MSI 93165/54165, 74165
8-BIT PARALLEL TO SERIAL CONVERTER

DESCRIPTION — The 93165/54165, 74165 is an 8-Bit Serial Shift Register which features parallel-in access to each stage, gated clock input, complementary outputs from the last stage and input clamp diodes. Parallel-in access to each stage is made possible by eight individual direct data inputs which are enabled by a LOW level at the shift/load input.

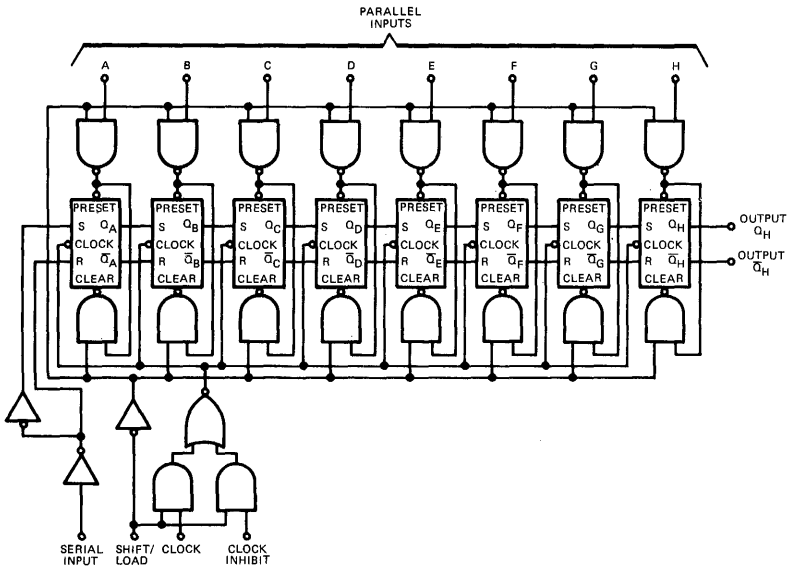
Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs HIGH inhibits clocking, and holding either clock input LOW with the load input HIGH enables the other clock input. The clock-inhibit input should be changed to the HIGH level only while the clock input is HIGH. Parallel loading is inhibited as long as the load input is HIGH. When taken LOW, data at the parallel inputs are loaded directly into the register independently of the state of the clock.

Typical power dissipation is 210 mW and maximum input clock frequency is typically 26 MHz.

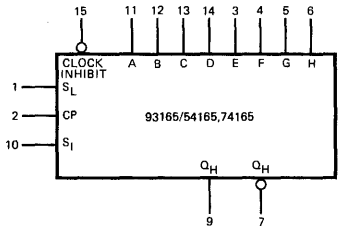
PIN NAMES		LOADING
A to H	Parallel Inputs	1 U.L.
S_I	Serial Input	1 U.L.
CP	Clock Input	1 U.L.
S_L	Shift Load	2 U.L.
$\overline{\text{CLOCK INHIBIT}}$	Clock Inhibit	1 U.L.
Q_H, $\overline{Q}_H$	Outputs	10 U.L.

NOTE: 1 U.L. = 40 μA HIGH/1.6 mA LOW.

LOGIC DIAGRAM

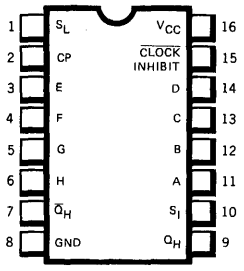


LOGIC SYMBOL

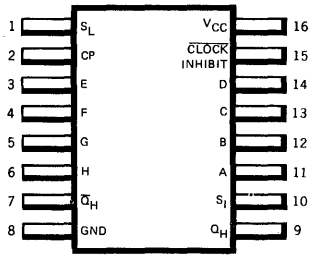


V_{CC} = PIN 16
GND = PIN 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive Logic: See Description.

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93165XM/54165XM			93165XC/74165XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		-55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		15			15			ns
Clock-enable setup time, t_{setup} (See Fig. 1)		30			30			ns
Parallel input setup time, t_{setup} (See Fig. 1)		10			10			ns
Serial input setup time, t_{setup} (see Fig. 2)		20			20			ns
Shift setup time, t_{setup} (See Fig. 2)		45			45			ns
Hold time at any input, t_{hold}		0			0			ns

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

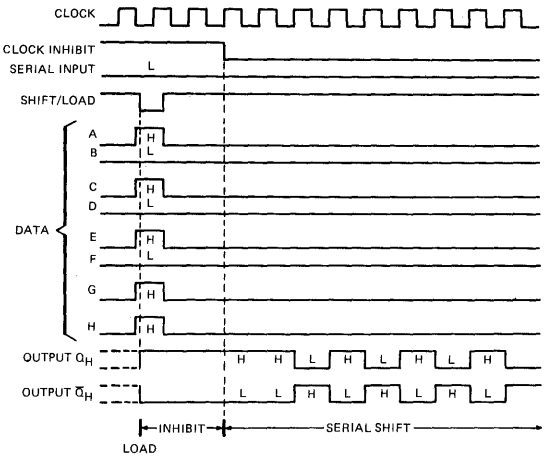
SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Threshold Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Threshold Voltage	
V_{CD}	Input Clamp Diode Voltage				-1.5	Volts	V_{CC} = MAX., I_{IN} = -12 mA	
V_{OH}	Output HIGH Voltage		2.4			Volts	V_{CC} = MIN., I_{OH} = -800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at MAX. Input Voltage				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current	Other Inputs			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
		Load Inputs			80			
I_{IL}	Input LOW Current	Other Inputs			-1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
		Load Inputs			-3.2			
I_{OS}	Output Short Circuit Current (Note 3)		-20		-55	mA	93165/54165	V_{CC} = MAX.
			-18		-55	mA	93165/74165	
I_{CC}	Supply Current (Note 4)			42	63	mA	V_{CC} = MAX.	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

SWITCHING CHARACTERISTICS (T_A = 25°C)

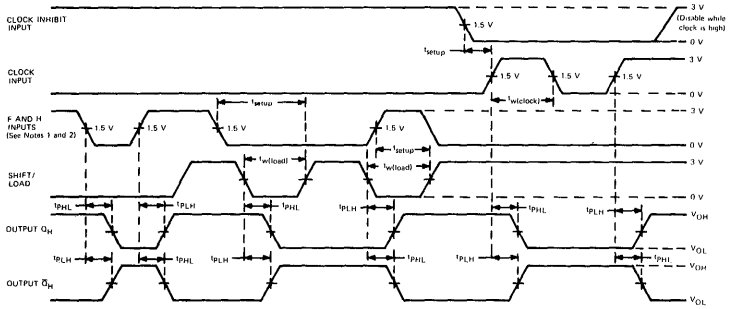
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
f_{max}	Max. Input Count Frequency	20	26		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω (See Figs. 1 Thru 3)
t_{PLH} t_{PHL}	Load Input to Any Output		21 27	31 40	ns	
t_{PLH} t_{PHL}	Clock Input to Any Output		16 21	24 31	ns	
t_{PLH} t_{PHL}	H Input to Q_H Output		11 24	17 36	ns	
t_{PLH} t_{PHL}	H Input to $\overline{Q}_H$ Output		18 18	27 27	ns	

TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES



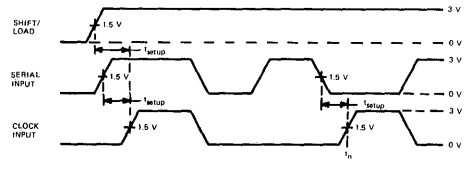
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



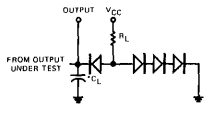
NOTES:
1. The remaining six data inputs and the serial input are LOW.
2. Prior to test, HIGH level data is loaded into H input.
3. The input pulse generators have the following characteristics:
   $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$. When testing f_{max}, vary clock PRR.

Fig. 1 VOLTAGE WAVEFORMS



NOTES:
1. The eight data inputs and the clock-inhibit input are LOW. Results are monitored at output Q_H at $t_n + 7$.
2. The inputs pulse generators have the following characteristics:
   $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.

Fig. 2 VOLTAGE WAVEFORMS



*C_L includes probe and jig capacitance.

Fig. 3 LOAD CIRCUIT FOR SWITCHING TESTS

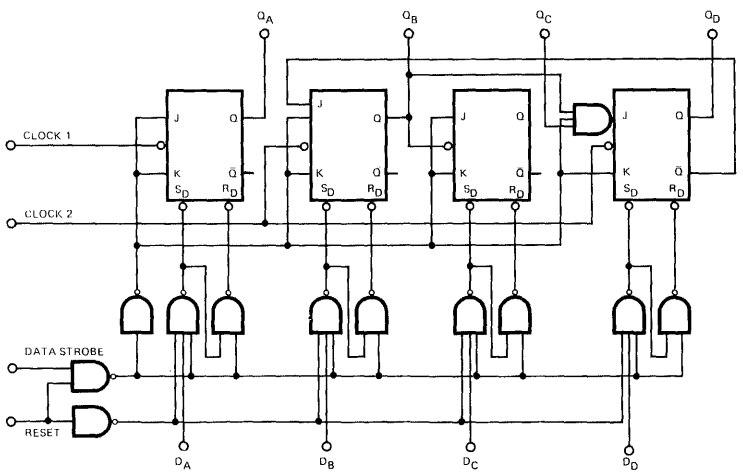
TTL/MSI 93176/54176, 74176
93177/54177,74177
BCD DECADE/4-BIT BINARY COUNTER

TO BE ANNOUNCED

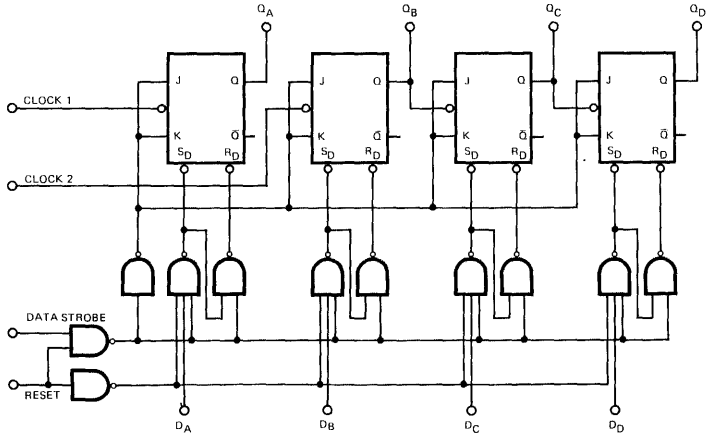
DESCRIPTION – The 93176/54176, 74176 is a Decade Counter that can be connected in BCD counting mode, in a divide-by-two and divide-by-five configuration, or in the bi-quinary mode. The 93177/54177, 74177 can be connected as a divide-by-two, eight, or sixteen counter. Both counters feature strobed parallel-entry capability. A LOW at the Data Strobe inputs transfers the data at the parallel inputs to the outputs. Each counter is provided with a reset input, which when LOW resets the outputs to LOW state. The counting operation is performed on the negative going edge of the clock pulse.

LOGIC DIAGRAM

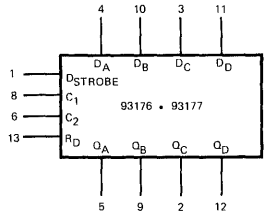
93176/54176, 74176



93177/54177, 74177

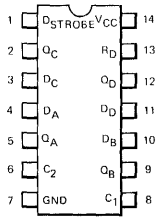


LOGIC SYMBOL

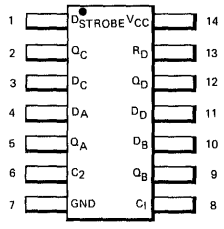


Pin numbers are shown for DIP only.

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



TTL/MSI 93178/54178, 74178
93179/54179, 74179
4-BIT SHIFT REGISTERS

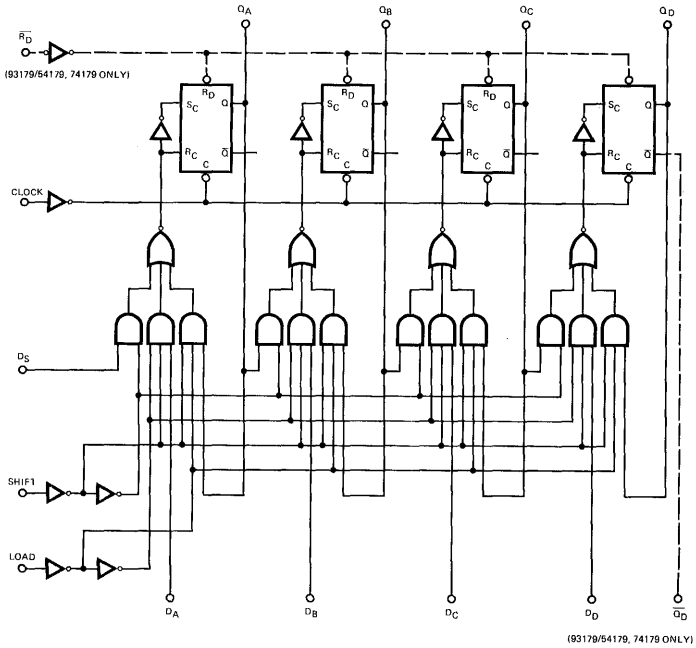
TO BE ANNOUNCED

DESCRIPTION – The 93178 and 93179 are 4-Bit Shift Registers with both serial and parallel data entry capability. The 93179 features a direct reset (R_D), and a $\overline{D}_{out}$ line in addition to the available outputs of the 93178. The truth table below indicates the three possible control states: shift right, parallel entry and hold. The clock line is buffered to minimize input clock loading. All changes occur on the negative-going clock transition. Since data transfer is synchronous with the clock, data may be transferred in any serial/parallel input/output relationship.

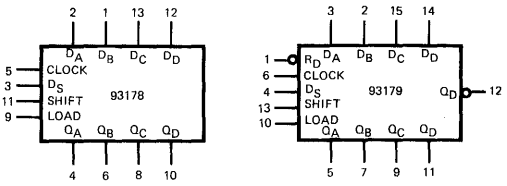
TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Shift Right	L	H
Shift Right	H	H

LOGIC DIAGRAM

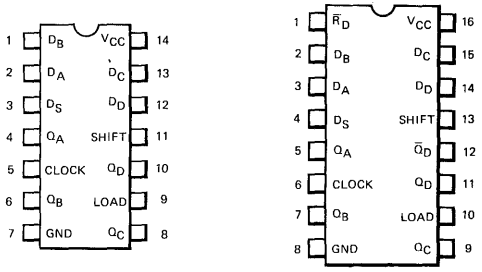


LOGIC SYMBOL



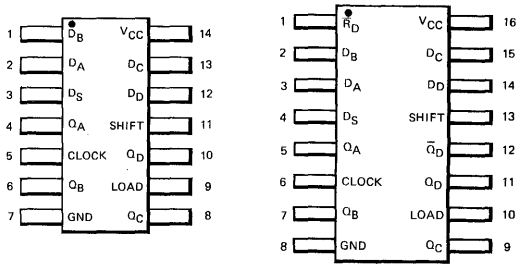
Pin numbers are shown for DIP only.

CONNECTION DIAGRAM
DIP (TOP VIEW)



93178/54178, 74178 **93179/54179, 74179**

FLATPAK (TOP VIEW)



93178/54178, 74178 **93179/54179, 74179**

TTL/MSI 93180/54180, 74180
8-BIT PARITY GENERATOR/CHECKER

DESCRIPTION – The 93180/54180 or 74180 are monolithic, 8-Bit Parity Check/Generators which feature control inputs and even/odd outputs to enhance operation in either odd or even parity applications. Cascading these circuits allows unlimited word length expansion. Typical application would be to generate and check parity on data being transmitted from one register to another. Typical power dissipation is 170 mW.

As with all Fairchild TTL products, all inputs are diode-clamped to minimize transmission-line effects and simplify system design.

PIN NAMES		LOADING
I_0 to I_7	Parity Inputs	1 U.L.
P_O	Odd Parity Input	2 U.L.
P_E	Even Parity Input	2 U.L.
ΣO_O	Sum Odd Outputs	10 U.L.
ΣO_E	Sum Even Outputs	10 U.L.

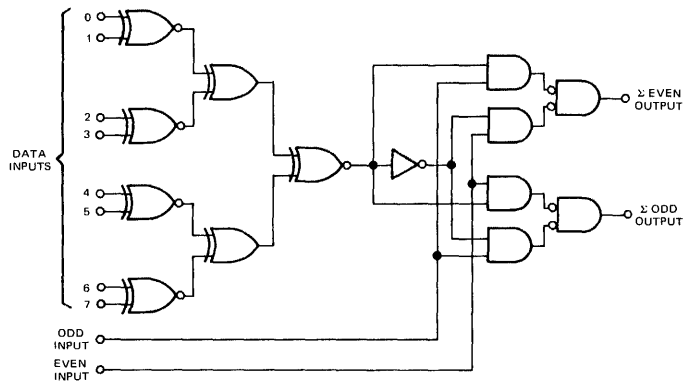
Note: 1 U.L. = 40 μA HIGH/1.6 mA LOW

TRUTH TABLE

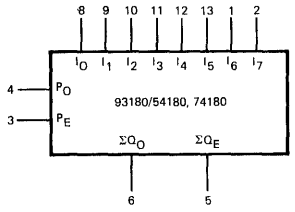
INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

X = irrelevant

LOGIC DIAGRAM

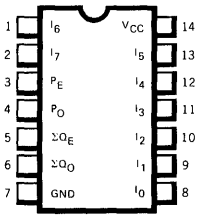


LOGIC SYMBOL

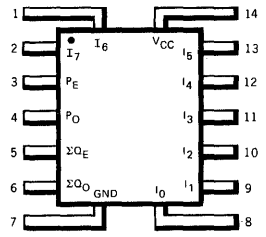


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic: See truth table.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93180XM/54180XM			93180XC/74180XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	LOW Level			10			10	U.L.
	HIGH Level			20			20	

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)		TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.				
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage		1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage		1
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V		1
I_{IH}	Input HIGH Current at Each Data Input			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V		2
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IH}	Input HIGH Current at Even or Odd Input			80	μA	V_{CC} = MAX., V_{IN} = 2.4 V		2
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V		
I_{IL}	Input LOW Current at Each Data Input			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V		2
I_{IL}	Input LOW Current at Even or Odd Input			−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V		2
I_{OS}	Output Short Circuit Current (Note 3)	−20		−55	mA	93180/54180	V_{CC} = MAX.	3
		−18		−55	mA	93180/74180		
I_{CC}	Supply Current		34	49	mA	93180/74180	V_{CC} = MAX.	3 & 4
			34	56	mA	93180/54180		

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Data Input to		40	60	ns	V_{CC} = 5.0 V	A
t_{PHL}	Σ Even Output		45	68		C_L = 15 pF	
t_{PLH}	Data Input to		32	48	ns	R_L = 400Ω	
t_{PHL}	Σ Odd Output		25	38		Odd Input Ground	
t_{PLH}	Data Input to		32	48	ns	V_{CC} = 5.0 V	A
t_{PHL}	Σ Even Output		25	38		C_L = 15 pF	
t_{PLH}	Data Input to		40	60	ns	R_L = 400Ω	
t_{PHL}	Σ Odd Output		45	68		Even Input Ground	
t_{PLH}	Even or Odd Input to Σ Even or Σ Odd Output		13	20	ns	V_{CC} = 5.0 V	A
t_{PHL}	Even or Odd Input to Σ Even or Σ Odd Output		7.0	10	ns	C_L = 15 pF, R_L = 400Ω	

NOTES
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the particular circuit type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) These voltage values are with respect to network ground terminal.

8

PARAMETER MEASUREMENT INFORMATION

dc TEST CIRCUITS*

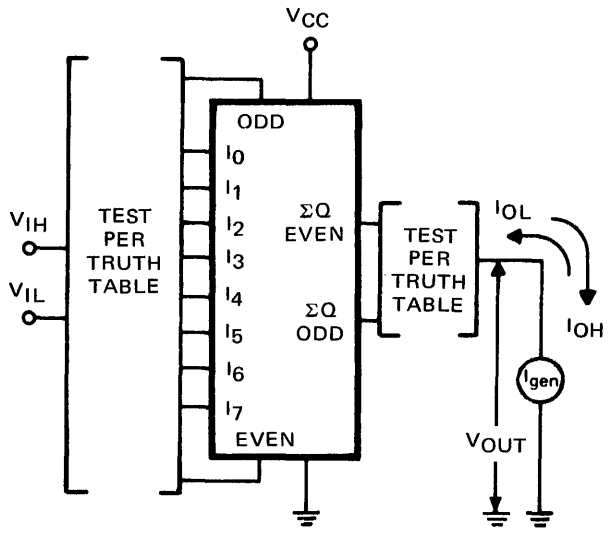
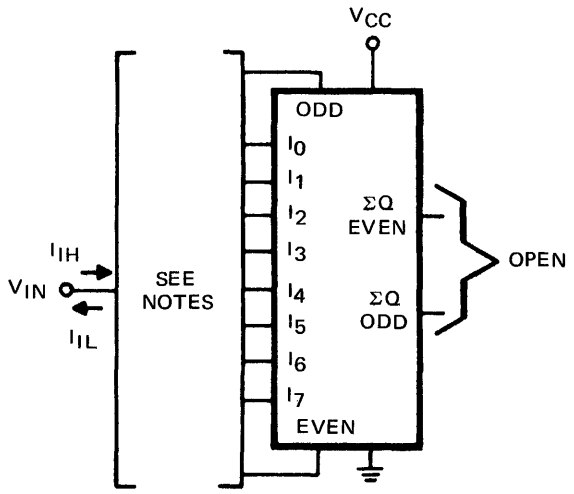
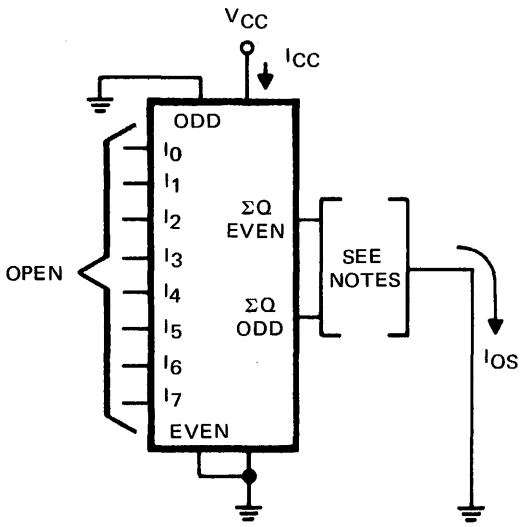


Fig. 1



NOTES:
1. Each output is tested separately.
2. Odd and even inputs are each tested for I_{IH} and I_{IL} with both an even-code and an odd-code applied at the data inputs.

Fig. 2



NOTES:
1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

Fig. 3

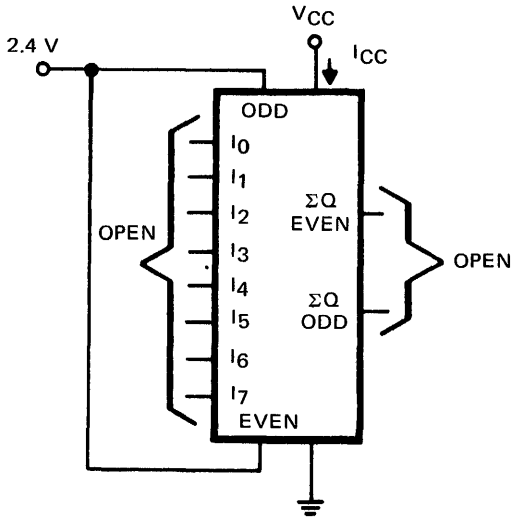
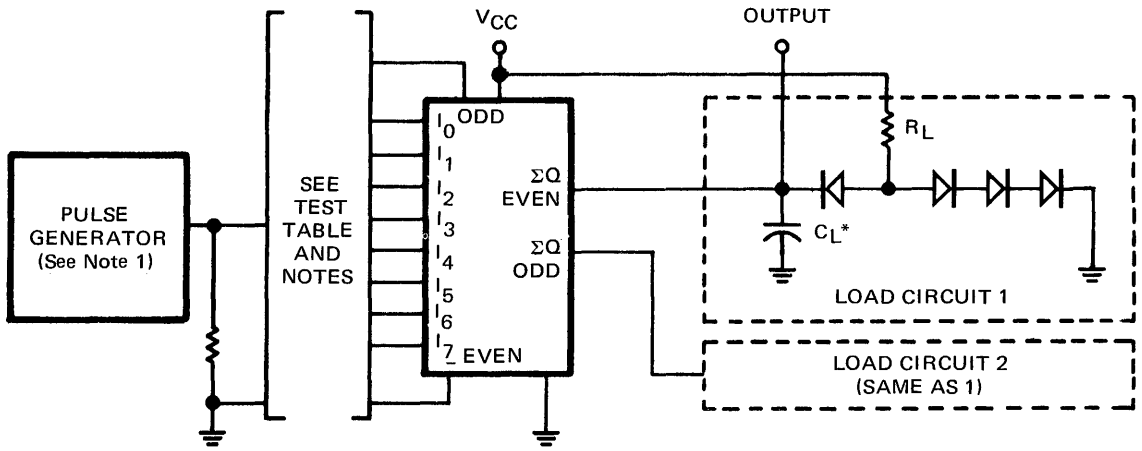


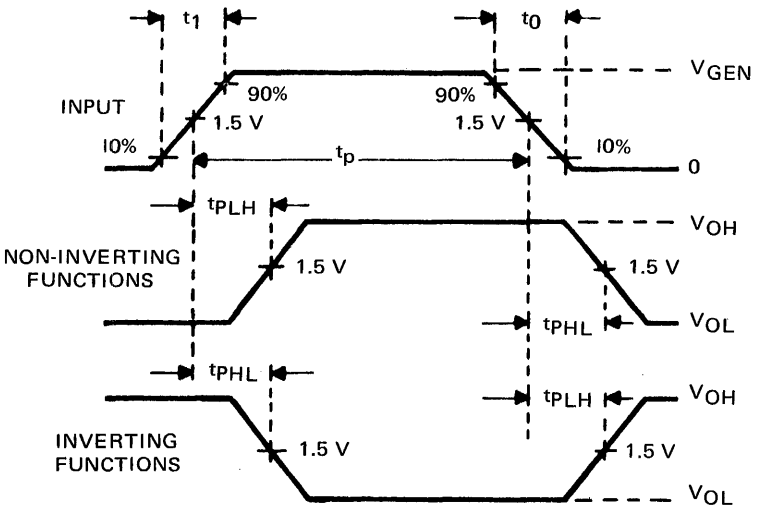
Fig. 4

PARAMETER MEASUREMENT INFORMATION (con't)

SWITCHING CHARACTERISTICS



*C_L includes probe and jig capacitance.



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generator has the following characteristics: V_{gen} = 3V, $t_1 = t_0$ = 10 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{OUT} \approx 50\ \Omega$.
2. Inputs not specified are open.

TEST TABLE†

INPUT CONDITIONS		OUTPUT TESTED
APPLY PULSE	GND	
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	0	Σ EVEN
ODD	NONE	Σ EVEN
EVEN	NONE	Σ ODD
ODD	0	Σ ODD

†Repeat all but the last 4 tests with the even input grounded.

Fig. A – SWITCHING TIMES

8

TTL/MSI 93H183/54H183, 74H183
HIGH SPEED DUAL CARRY/SAVE FULL ADDER

DESCRIPTION – The 93H183/54H183, 74H183 features two independent, high speed, Full Adders. Typical average sum and carry propagation delay times are 11 ns. Each adder has an individual carry output from each bit for use in multiple-input, carry/save techniques to produce the true sum and true carry outputs.

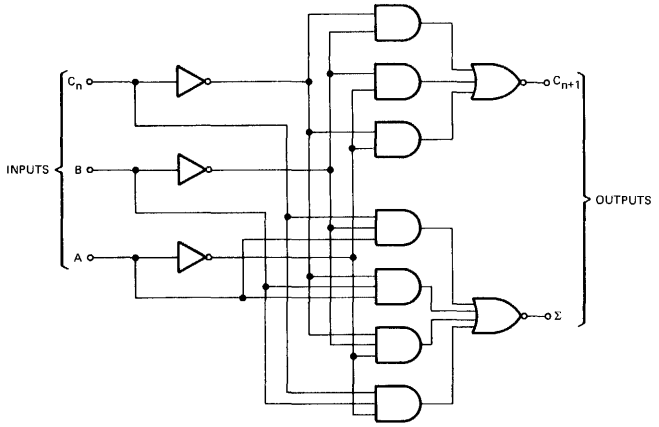
PIN NAMES		**LOADING** (Note a)
1A, 1B, $1C_n$, 2A, 2B, $2C_n$	Inputs	3.75 U.L.
$1C_{n+1}$, 1Σ, $2C_{n+1}$, 2Σ	Outputs (Note b)	12.5 U.L.

NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. 12.5 U.L. is the LOW drive factor and 25 U.L. is the HIGH drive factor.

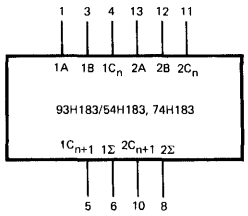
TRUTH TABLE

INPUTS			OUTPUTS	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

LOGIC DIAGRAM
(EACH ADDER)

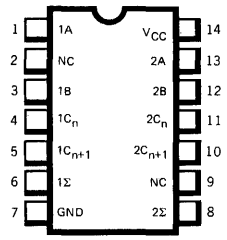


LOGIC SYMBOL

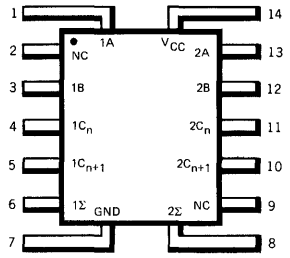


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



NC – No internal connection
Positive logic: See truth table

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	93H183XM/54H183XM			93H183XC/74H183XC			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC} (See Note 4)	4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range	−55	25	125	0	25	70	°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	TEST FIGURE
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage	1
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Threshold Voltage	2
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −1 mA, V_{IH} = 2.0 V	1
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 20 mA, V_{IL} = 0.8 V	2
I_{IH}	Input HIGH Current			150	μA	V_{CC} = MAX., V_{IN} = 2.4 V; Any Input	3
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V; Any Input	
I_{IL}	Input LOW Current			−6.0	mA	V_{CC} = MAX., V_{IN} = 0.4 V, Any Input	3
I_{OS}	Output Short Circuit Current (Note 3)	−40		−100	mA	V_{CC} = MAX.	4
I_{CCH}	Supply Current HIGH		40		mA	V_{CC} = MAX., V_{IN} = 4.5 V, All Outputs HIGH	5
I_{CCL}	Supply Current LOW		48	69	mA	93H183/54H183; V_{CC} = MAX., V_{IN} = 0 V, All Outputs LOW	5
			48	75	mA	93H183/74H183; V_{CC} = MAX., V_{IN} = 0 V, All Outputs LOW	

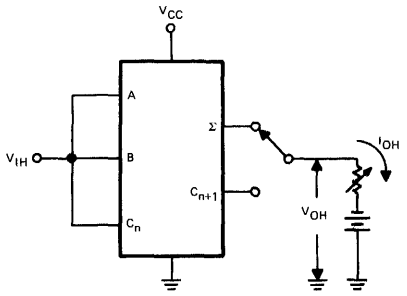
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	TEST FIGURE
		MIN.	TYP.	MAX.			
t_{PLH}	Turn Off Delay Input to Output		10	15	ns	V_{CC} = 5.0 V, C_L = 25 pF, R_L = 280Ω	A
t_{PHL}	Turn On Delay Input to Output		12	18	ns		

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time, and duration of short-circuit test should not exceed 1 second.
(4) Voltage values, except interemitter voltage, are with respect to network ground terminal.

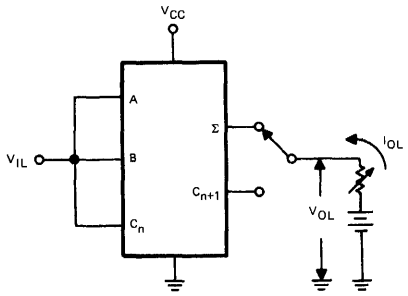
PARAMETER MEASUREMENT INFORMATION

DC TEST CIRCUITS*



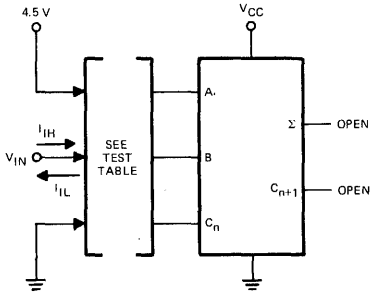
Each output is tested separately.

Fig. 1 – V_{IH}, V_{OH}



Each output is tested separately.

Fig. 2 – V_{IL}, V_{OL}

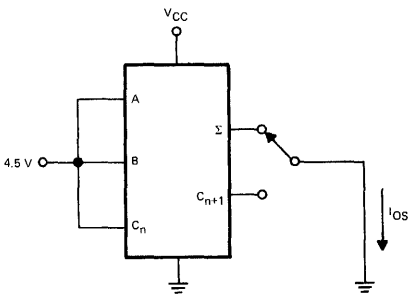


Each input is tested for both combinations of states of the other inputs.

Fig. 3. – I_{IH}, I_{IL}

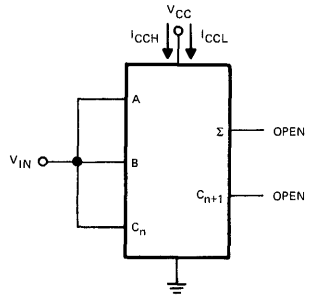
TEST TABLE

APPLY V_{IN}, MEASURE I_{IH}/I_{IL}	CONDITIONS ON OTHER INPUTS	
	4.5 V	GND
A	B, C_n	NONE
	B	C_n
	C_n	B
	NONE	B, C_n
B	A, C_n	NONE
	A	C_n
	C_n	A
	NONE	A, C_n
C_n	A, B	NONE
	A	B
	B	A
	NONE	A, B



Each output is tested separately.

Fig. 4 – I_{OS}



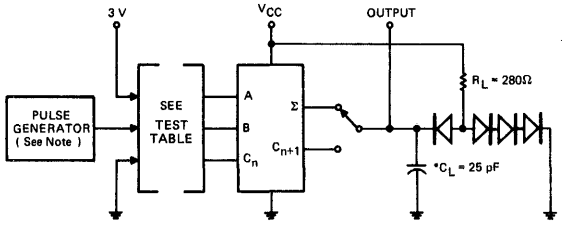
Both adders are tested simultaneously.

Fig. 5 – I_{CCH}, I_{CCL}

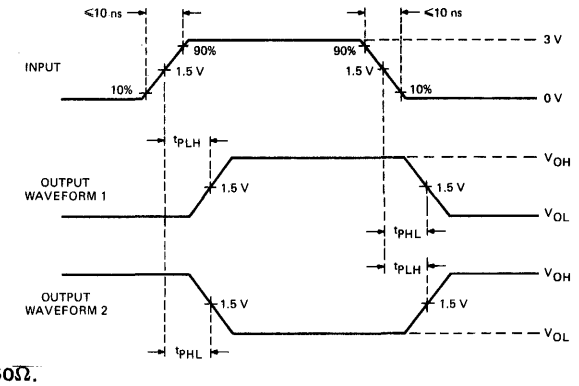
*Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



*C_L inclues probe and jig capacitance.



NOTE:
The generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\Omega$.

TEST CIRCUIT **VOLTAGE WAVEFORMS**

Fig. A – SWITCHING TIMES

TEST TABLE FOR FIG. A (EACH ADDER)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR	APPLY 3V	APPLY GND	OUTPUT UNDER TEST	OUTPUT WAVEFORM
1	t_{PLH}	A	B, C_n		Σ	1
2	t_{PHL}					
3	t_{PLH}	A	B	C_n	Σ	2
4	t_{PHL}					
5	t_{PLH}	A	C_n	B	Σ	2
6	t_{PHL}					
7	t_{PLH}	A		B, C_n	Σ	1
8	t_{PHL}					
9	t_{PLH}	A	B	C_n	C_{n+1}	1
10	t_{PHL}					
11	t_{PLH}	A	C_n	B	C_{n+1}	1
12	t_{PHL}					
13	t_{PLH}	B	A, C_n		Σ	1
14	t_{PHL}					
15	t_{PLH}	B	A	C_n	Σ	2
16	t_{PHL}					
17	t_{PLH}	B	C_n	A	Σ	2
18	t_{PHL}					
19	t_{PLH}	B		A, C_n	Σ	1
20	t_{PHL}					
21	t_{PLH}	B	A	C_n	C_{n+1}	1
22	t_{PHL}					
23	t_{PLH}	B	C_n	A	C_{n+1}	1
24	t_{PHL}					
25	t_{PLH}	C_n	A, B		Σ	1
26	t_{PHL}					
27	t_{PLH}	C_n	A	B	Σ	2
28	t_{PHL}					
29	t_{PLH}	C_n	B	A	Σ	2
30	t_{PHL}					
31	t_{PLH}	C_n		A, B	Σ	1
32	t_{PHL}					
33	t_{PLH}	C_n	A	B	C_{n+1}	1
34	t_{PHL}					
35	t_{PLH}	C_n	B	A	C_{n+1}	1
36	t_{PHL}					

TTL/MSI 93190/54190, 74190
93191/54191, 74191
UP/DOWN DECADE AND BINARY COUNTER

DESCRIPTION – The 93190/54190, 74190 and 93191/54191, 74191 are Synchronous Up/Down Counters with enable control presetting facility, single line up/down control, cascading for multi-decade operation and buffered inputs. The 93190/54190, 74190 is a BCD counter, while the 93191/54191, 74191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met. This mode of operation will eliminate the output counting spikes which are normally associated with asynchronous (ripple clock) counters.

A HIGH at the enable input inhibits counting. A LOW at the enable input and a LOW-to-HIGH clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is HIGH. The down/up input determines the direction of the count. When LOW, the count goes up; when HIGH, the count goes down.

These counters are fully programmable. The outputs may be preset to any state by placing a LOW on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

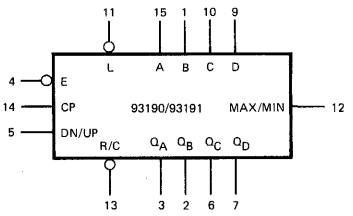
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a HIGH level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a LOW level output pulse equal in width to the LOW level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish lookahead for high speed operation.

Power dissipation is typically 325 mW for either the decade or binary version. Maximum input clock frequency is typically 25 MHz and is guaranteed to be at least 20 MHz.

PIN NAMES		LOADING
$\overline{L}$	Load Input	1 U.L.
A, B, C, D	Parallel Input	1 U.L.
$\overline{E}$	Enable Input	3 U.L.
CP	Clock Input	1 U.L.
DN/UP	Down/Up Input	1 U.L.
$\overline{R/C}$	Ripple Clock Output	10 U.L.
Q_A, Q_B, Q_C, Q_D	Parallel Output	10 U.L.
Max/Min	Max./Min. Output	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

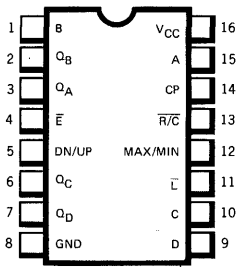
LOGIC SYMBOL



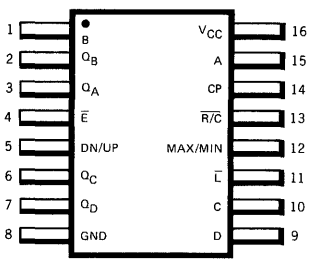
V_{CC} = Pin 16
GND = Pin 8

93190/54190, 74190
93191/54191, 74191

CONNECTION DIAGRAM
DIP (TOP VIEW)

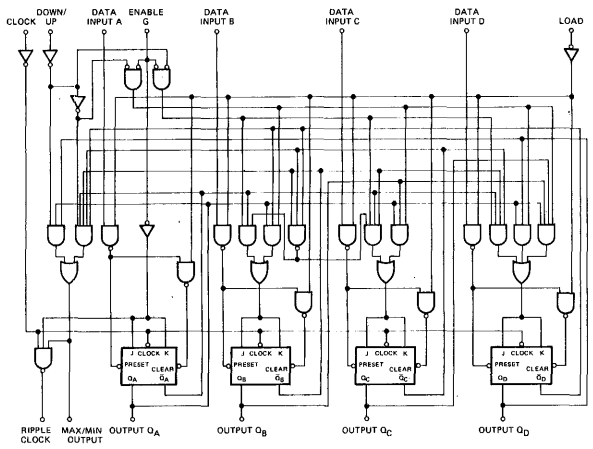


FLATPAK (TOP VIEW)

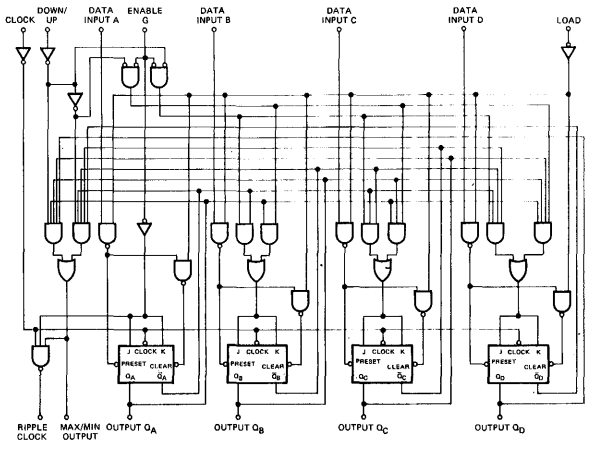


Asynchronous inputs:
LOW input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

LOGIC DIAGRAMS

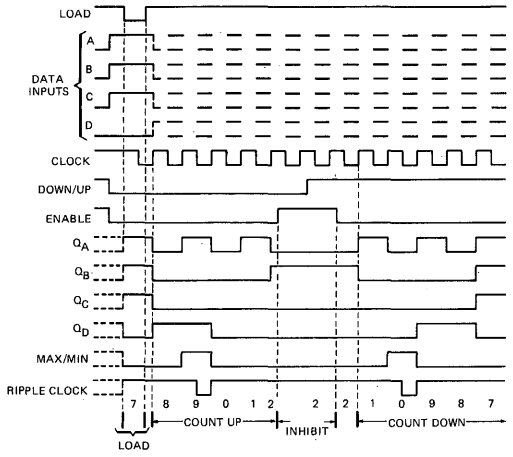


DECADE COUNTER
93190/54190, 74190



BINARY COUNTER
93191/54191, 74191

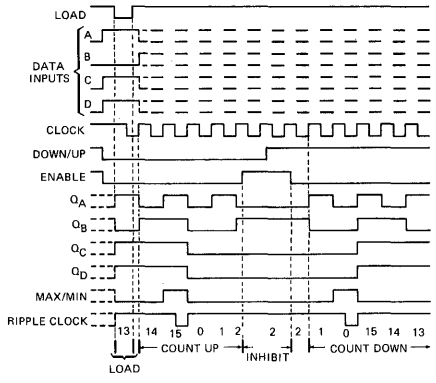
TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCE



The following sequence is illustrated:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

DECADE COUNTER
93190/54190, 74190



The following sequence is illustrated:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.

BINARY COUNTER
93191/54191, 74191

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93190XM/54190XM 93191XM/54191XM			93190XC/74190XC 93191XC/74191XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Input Clock Frequency, f_{clock}		0		20	0		20	MHz
Width of Clock Input Pulse, $t_{w(clock)}$		25			25			ns
Width of Load Input Pulse, $t_{w(load)}$		35			35			ns
Data Setup Time, t_{setup} (See Fig. 1 and 2)		20			20			ns
Data Hold Time, t_{hold}		0			0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Threshold Voltage
V_{CD}	Input Clamp Diode Voltage				−1.5	Volts	V_{CC} = MIN., I_{IN} = −12mA
V_{OH}	Output HIGH Voltage		2.4			Volts	V_{CC} = MIN., I_{OH} = −800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V
I_I	Input Current at Max Input Voltage				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IH}	Input HIGH Current	Other Inputs			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V
		Enable Input			120		
I_{IL}	Input LOW Current	Other Inputs			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V
		Enable Input			−4.8		
I_{OS}	Output Short Circuit Current (Note 3)		−20		−65	mA	93190/54190; 93191/54191; V_{CC} = MAX.
			−18		−65		93190/74190; 93191/74191; V_{CC} = MAX.
I_{CC}	Supply Current (Note 4)			65	105	mA	V_{CC} = MAX.

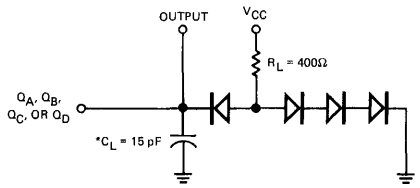
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) I_{CC} is measured with all inputs grounded and all outputs open.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	A TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{max}	Max. Input Clock Frequency	20	25		MHz	V_{CC} = 5.0 V C_L = 15 pF R_L = 400Ω (See Fig. 1 and Fig. 3 thru 7)
t_{PLH} t_{PHL}	Load Input to Q_A, Q_B, Q_C, Q_D Output		22 33	33 50	ns	
t_{PLH} t_{PHL}	Data Input A, B, C, D, to Q_A, Q_B, Q_C, Q_D Output		14 35	22 50	ns	
t_{PLH} t_{PHL}	Clock Input to Ripple Clock Output		13 16	20 24	ns	
t_{PLH} t_{PHL}	Clock Input to Q_A, Q_B, Q_C, Q_D Output		16 24	24 36	ns	
t_{PLH} t_{PHL}	Clock Input to Max./Min. Output		28 37	42 52	ns	
t_{PLH} t_{PHL}	Down/Up Input to Ripple Clock Output		30 30	45 45	ns	
t_{PLH} t_{PHL}	Down/Up Input to Max./Min. Output		21 22	33 33	ns	

PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS



*C_L includes probe & jig capacitance.

Fig. 1 – LOAD CIRCUIT FOR SWITCHING TIME MEASUREMENT

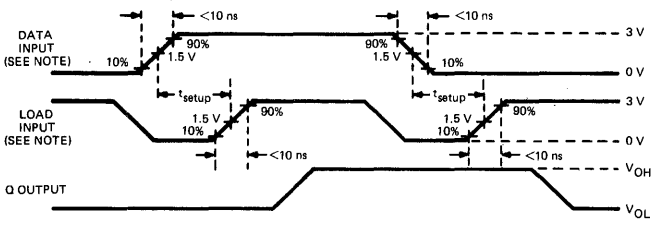
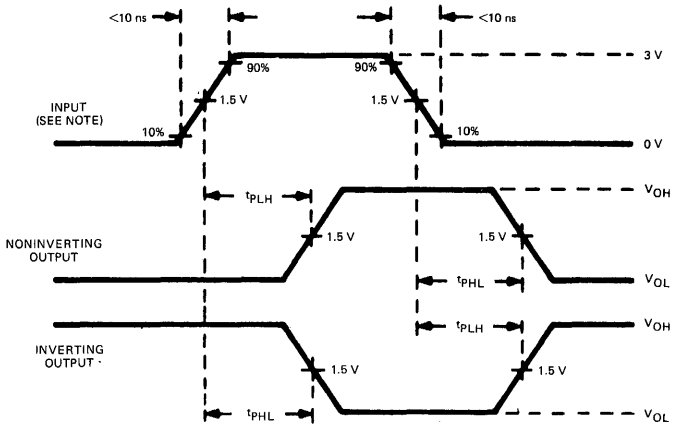


Fig. 2 – SETUP TIME VOLTAGE WAVEFORMS



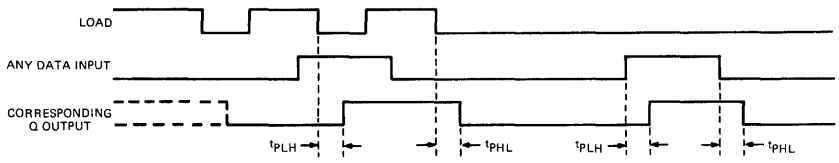
See waveform sequences in Figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in Figures 4 through 7.

Fig. 3 – GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTE:
The input pulses are supplied by generators having the following characteristics: Z_{out} = 50Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.

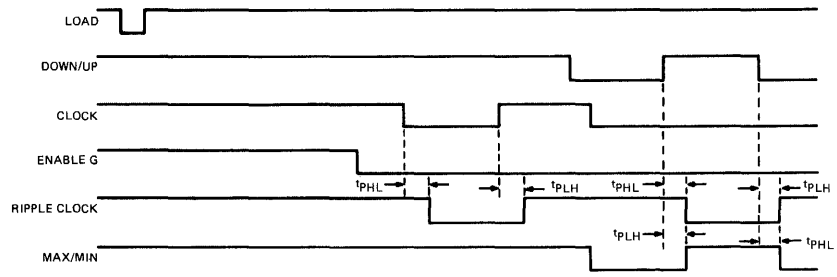
PARAMETER MEASUREMENT INFORMATION

SWITCHING CHARACTERISTICS (cont'd)



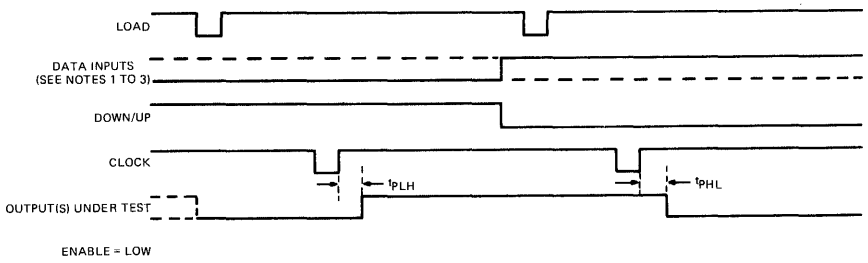
NOTE: Conditions on other inputs are irrelevant.

Fig. 4 – LOAD TO OUTPUT AND DATA TO OUTPUT



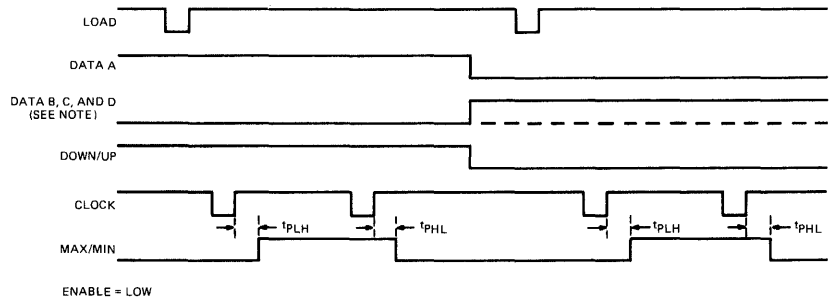
NOTE: All data inputs are LOW.

Fig. 5 – ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN



NOTES:
1. To test Q_A, Q_B, and Q_C outputs of 93190/54190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
2. To test Q_D output of 93190/54190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the LOW logic level.
3. To test Q_A, Q_B, Q_C, and Q_D outputs of 93191/54191: All four data inputs are shown by the solid line.

Fig. 6 – CLOCK TO OUTPUT



NOTE: Data inputs B and C are shown by the dashed line for 93190/54190 and the solid line for 93191/54191. Data input D is shown by the solid line for both devices.

Fig. 7 – CLOCK TO MAX/MIN

TTL/MSI 93196/54196, 74196
93197/54197, 74197
HIGH SPEED DECADE AND BINARY COUNTER

TO BE ANNOUNCED

DESCRIPTION – The 93196/54196, 74196 and 93197/54197, 74197 High Speed Counters will provide either a divide-by-two and a divide-by-five counter (93196/54196, 74196) or a divide-by-two and a divide-by-eight counter (93197/54197, 74197). The counters are fully presettable to any output state by placing a LOW on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs regardless of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is LOW, but will remain unchanged when the count/load is HIGH and the clock inputs are inactive.

These high speed counters will accept count frequencies of 0 to 50 MHz at the clock 1 input and 0 to 25 MHz at the clock 2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken LOW, sets all outputs LOW regardless of the states of the clocks.

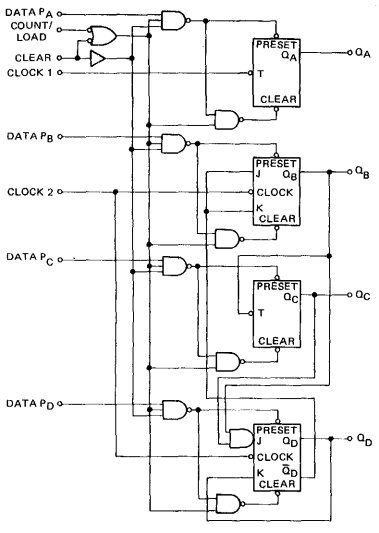
All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 240 mW.

PIN NAMES		LOADING (Note a)
$\overline{P_A}$, $\overline{P_B}$, P_C, P_D	Parallel Inputs	1 U.L.
$\overline{CP_1}$, $\overline{CP_2}$	Clock Inputs (Note b)	2 U.L.
$\overline{CLEAR}$	Clear Input	2 U.L.
$\overline{COUNT/LOAD}$	Count Load Input	1 U.L.
Q_A, Q_B, Q_C, Q_D	Parallel Outputs	10 U.L.

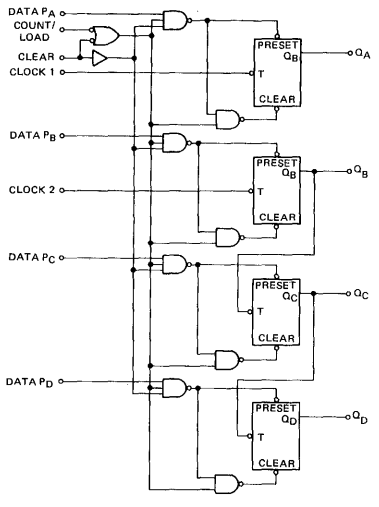
NOTES:
(a) 1 U.L. = 40 μA HIGH/1.6 mA LOW
(b) $\overline{CP_2}$ – 3 U.L. on 93196

LOGIC DIAGRAM

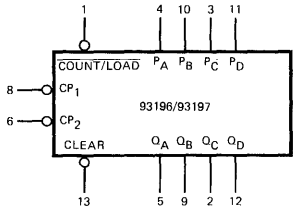
93196/54196, 74196



93197/54197, 74197

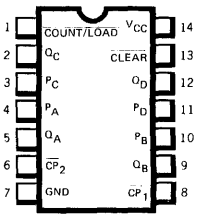


LOGIC SYMBOL

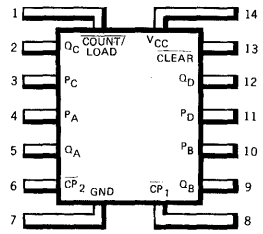


V_{CC} = Pin 14
Gnd = Pin 7

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Asynchronous input: LOW input to clear sets Q_A, Q_B, Q_C and Q_D LOW.

8

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93196XM/54196XM 93197XM/54197XM			93196XC/74196XC 93197XC/74197XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N HIGH Logic/LOW Logic				20/10			20/10	U.L.
Count Frequency (See Fig. 1) $\overline{CP}_1/\overline{CP}_2$		0/0		50/25	0/0		50/25	MHz
Pulse Width, t_w (See Fig. 1)	$\overline{CP}_1/\overline{CP}_2$	10/20			10/20			ns
	Clear/Load	15/20			15/20			
Input Hold Time, t_{hold} (See Fig. 1)	HIGH & LOW Level Data	tw (Load)			tw (Load)			ns
Input Setup Time, t_{setup} (See Fig. 1)	HIGH Data/LOW Data	10/15			10/15			ns
Count Enable Time, t_{enable}* (See Fig. 1)		20			20			ns
Clock Input Pulse Fall Time t_f (See Fig. 1)				75			75	ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

*Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must be both HIGH to ensure counting.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	
V_{IH}	Input HIGH Voltage		2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage				−1.5	Volts	V_{CC} = MAX., I_{IN} = −12 mA	
V_{OH}	Output HIGH Voltage		2.4			Volts	V_{CC} = MIN., I_{OH} = −800 μA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
V_{OL}	Output LOW Voltage				0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, (Note 4) V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at Max. Input Voltage				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current	Data, $\overline{Count/Load}$			40	μA		V_{CC} = MAX. V_{IN} = 2.4 V
		$\overline{Clear}$, $\overline{CP}_1$			80	μA		
		$\overline{CP}_2$			120	μA	93196/54196, 74196	
					80	μA	93197/54197, 74197	
I_{IL}	Input LOW Current	Data, $\overline{Count/Load}$			−1.6	mA		V_{CC} = MAX. V_{IN} = 0.4 V
		$\overline{Clear}$			−3.2	mA		
		$\overline{CP}_1$			−4.8	mA		
		$\overline{CP}_2$			−6.4	mA	93196/54196, 74196	
					−3.2	mA	93197/54197, 74197	
I_{OS}	Output Short Circuit Current (Note 3)		−20		−57	mA	93196/54196, 93197/54197	V_{CC} = MAX.
			−18		−57	mA	93196/74196, 93197/74197	
I_{CC}	Supply Current (Note 5)			48	59	mA	V_{CC} = MAX.	

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0V, 25°C.
(3) Not more than one output should be shorted at a time.
(4) Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock 2 input. This permits driving the clock 2 input while fanning out to 10 Series 54/74 loads.
(5) I_{CC} is measured with all inputs grounded and all outputs open.

TYPICAL COUNT CONFIGURATIONS

93196/54196, 74196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a BCD decade counter, the clock 2 input must be externally connected to the Q_A output. The clock 1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown at the right.
2. If a symmetrical divide-by-ten count is desired for any application requiring division of a binary count by a power of ten, the Q_D output must be externally connected to the clock 1 input. The input count is then applied at the clock 2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table shown at the right.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock 2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

93196/54196, 74196 TRUTH TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES:
A. Output Q_A connected to clock 2 input.
B. Output Q_D connected to clock 1 input.

93197/54197, 74197

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high speed 4-bit ripple counter, output Q_A must be externally connected to the clock 2 input. The input count pulses are applied to the clock 1 input. Simultaneous divisions by 2, 4, 8 and 16 are performed at the Q_A, Q_B, Q_C, Q_D output as shown in the truth table at the right.
2. When used as a 3-bit ripple counter, the input count pulses are applied to the clock 2 input. Simultaneous frequency divisions by 2, 4 and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple counter.

93197/54197, 74197 TRUTH TABLE

(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE:
A. Output Q_A connected to clock 2 input.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

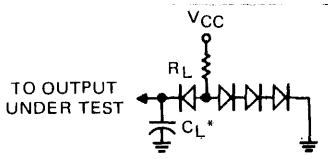
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

SWITCHING CHARACTERISTICS (T_A = 25°C) (see Fig. 1)

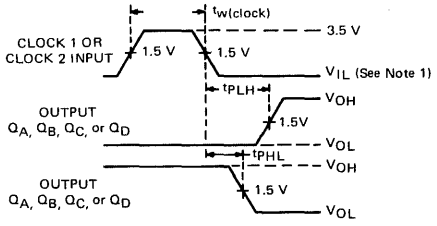
SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS	
f_{MAX}	(MAX. Input Count Frequency)	50	70		MHz		V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF
t_{PLH} / t_{PHL}	$\overline{\text{Clock 1}}$ Input to Q_A Output		7.0 / 10	12 / 15	ns		
t_{PLH} / t_{PHL}	$\overline{\text{Clock 2}}$ Input to Q_B Output		12 / 14	18 / 21	ns		
t_{PLH} / t_{PHL}	$\overline{\text{Clock 2}}$ Input to Q_C Output		24 / 28	36 / 42	ns		
t_{PLH}	$\overline{\text{Clock 2}}$ Input to Q_D Output		14	21	ns	93196/54196, 74196	
			36	54	ns	93197/54197, 74197	
t_{PHL}			12	18	ns	93196/54196, 74196	
			42	63	ns	93197/54197, 74197	
t_{PLH} / t_{PHL}	A, B, C, D Inputs to Q_A, Q_B, Q_C, Q_D Outputs		16 / 25	24 / 38	ns		
t_{PLH} / t_{PHL}	Load Input to Any Output		22 / 24	33 / 36	ns		
t_{PHL}	$\overline{\text{Clear}}$ Input to Any Output		25	37	ns		

PARAMETER MEASUREMENT INFORMATION

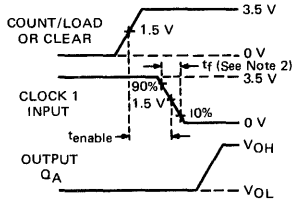


*C_L includes probe and jig capacitance.

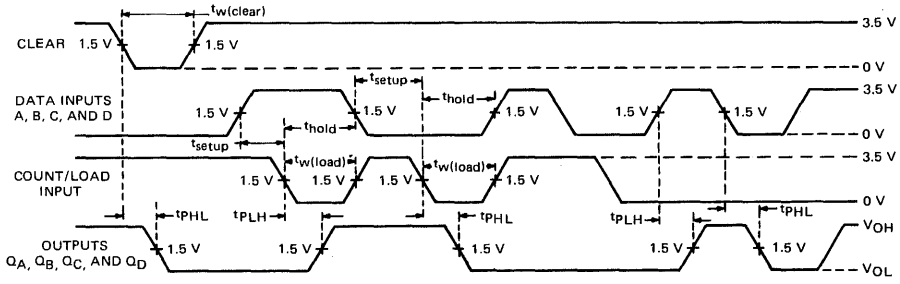
LOAD CIRCUIT



CLOCK-MODE VOLTAGE WAVEFORMS



CLOCK ENABLE TIME VOLTAGE WAVEFORMS



CLEAR AND LOAD VOLTAGE WAVEFORMS

NOTES:
1. The input pulse generator has the following characteristics: for testing f_{max}, V_{IL} = 0.3 ± 0.1 V, duty cycle = 50%, t_r < 5 ns, and t_f < 5 ns; for all other measurements V_{IL} = 0, PRR ≤ 1 MHz, duty cycle ≤ 50%, t_r < 5 ns, and unless otherwise specified, t_f < 5 ns.
2. Fall time of clock 1 is measured with count/load and clear high. When measuring clock enable time, t_f < 5 ns.
3. Unless otherwise specified, Q_A is connected to Clock 2.

Fig. 1

TTL/MSI 93198/54198, 74198

8-BIT SHIFT REGISTER

TO BE ANNOUNCED

DESCRIPTION – The 93198/54198, 74198 are Bidirectional Registers that are designed to incorporate virtually all of the features a system designer may want in a shift register. The 93198/54198, 74198 feature 35 MHz shift frequency, parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating mode-control inputs and a direct overriding clear line. The register has four distinct modes of operation: (1) parallel (broadside) load, (2) shift right (in the direction Q_A toward Q_H), (3) shift left (in the direction Q_H toward Q_A), (4) inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S_0 and S_1, HIGH. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is HIGH and S_1 is LOW. Serial data for this mode is entered at the shift-right data input. When S_0 is LOW and S_1 is HIGH, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are LOW. The mode controls should be changed only while the clock input is HIGH.

Typical power dissipation is 360 mW and all inputs are diode-clamped.

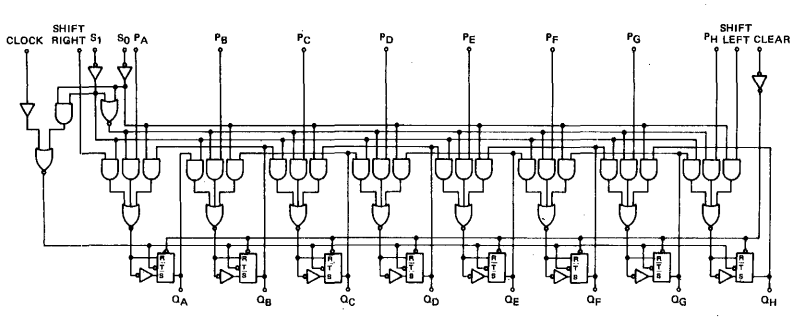
PIN NAMES		LOADING
P_A to P_H	Parallel Data Inputs	1 U.L.
S_0, S_1	Mode Control Inputs	1 U.L.
L	Shift Left Serial Input	1 U.L.
R	Shift Right Serial Input	1 U.L.
CP	Clock (Active HIGH Going Edge) Input	1 U.L.
$\overline{CL}$	Clear (Active LOW) Input	1 U.L.
Q_A to Q_H	Data Outputs	10 U.L.

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

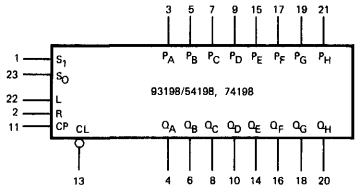
TRUTH TABLE OPERATION OF MODE CONTROL

INPUTS		MODE
S_1	S_0	
L	L	INHIBIT CLOCK
L	H	SHIFT RIGHT
H	L	SHIFT LEFT
H	H	PARALLEL LOAD

LOGIC DIAGRAM

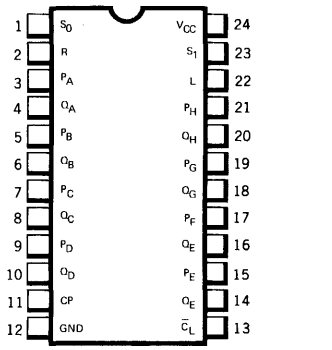


LOGIC SYMBOL

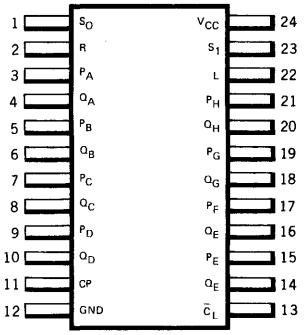


V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



Positive logic: See truth table for mode control (S_0, S_1)

8

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		93198XM/54198XM			93198XC/74198XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N	HIGH Level			20			20	U.L.
	LOW Level			10			10	
Input Count Frequency, f_{count}		0		25	0		25	MHz
Width of Clock or Clear Pulse, t_W (See Fig. 1)		20			20			ns
Mode-Control Setup Time, t_{setup}		30			30			ns
Data Setup Time, t_{setup} (See Fig. 1)		20			20			ns
Hold Time at Any Input, t_{hold} (See Fig. 1)		0			0			ns

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

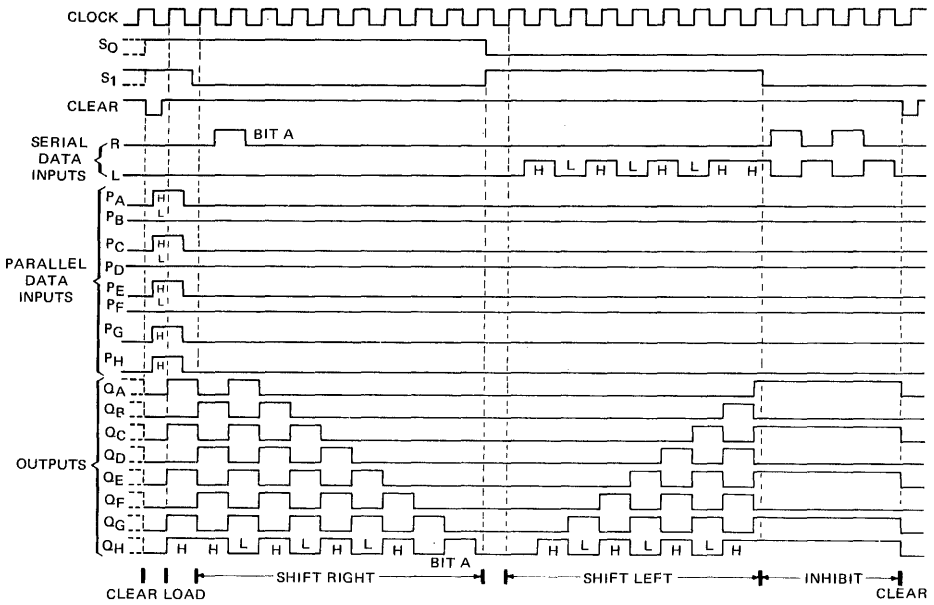
SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS (Note 1)	
		MIN.	TYP. (Note 2)	MAX.			
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage	
V_{CD}	Input Clamp Diode Voltage			−1.5	Volts	V_{CC} = MAX., I_{IN} = −12 mA	
V_{OH}	Output HIGH Voltage	2.4			Volts	V_{CC} = MIN., I_{OH} = −800 μA, V_{IH} = 2.0 V, VIL = 0.8 V	
V_{OL}	Output LOW Voltage			0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	
I_I	Input Current at MAX. Input Voltage			1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IH}	Input HIGH Current			40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	
I_{IL}	Input LOW Current			−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)	−20		−57	mA	93198/54198	V_{CC} = MAX.
		−18		−57	mA	93198/74198	
I_{CC}	Supply Current		72	104	mA	93198/54198	V_{CC} = MAX., S_0, S_1 = 4.5 V; CP = Momentary GND then 4.5 V; $\overline{CL}$, P_A to P_H = GND; All Outputs are Open
			72	116	mA	93198/74198	

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN.	TYP.	MAX.		
f_{MAX}	Maximum Input Count Frequency	25	35		MHz	V_{CC} = 5.0 V; C_L = 15 pF; R_L = 400 Ω; (see Fig. 1)
t_{PHL}	Turn On Delay Clear to Output		23	35	ns	
t_{PLH}	Turn Off Delay Clock to Output	8	17	26	ns	
t_{PHL}	Turn On Delay Clock to Output	8	20	30	ns	

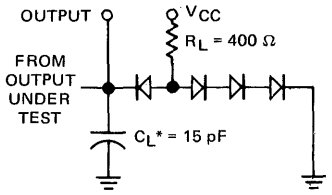
NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT, AND CLEAR SEQUENCES



SWITCHING PARAMETER MEASUREMENT INFORMATION

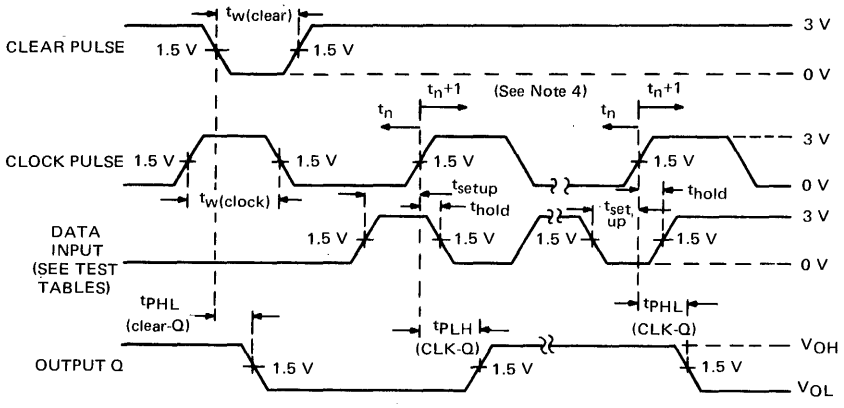
LOAD FOR OUTPUT UNDER TEST



*C_L includes probe and jig capacitance.

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE 3)
P_A	4.5 V	4.5 V	Q_A at t_n+1
P_B	4.5 V	4.5 V	Q_B at t_n+1
P_C	4.5 V	4.5 V	Q_C at t_n+1
P_D	4.5 V	4.5 V	Q_D at t_n+1
P_E	4.5 V	4.5 V	Q_E at t_n+1
P_F	4.5 V	4.5 V	Q_F at t_n+1
P_G	4.5 V	4.5 V	Q_G at t_n+1
P_H	4.5 V	4.5 V	Q_H at t_n+1
L Serial Input	4.5 V	0 V	Q_A at t_n+8
R Serial Input	0 V	4.5 V	Q_H at t_n+8



VOLTAGE WAVEFORMS

NOTES:
1. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and $t_{hold} = 0$ ns. When testing f_{MAX}, vary the clock PRR.
2. A clear pulse is applied prior to each test.
3. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_n+1. Proper shifting of data is verified at t_n+8 with a functional test.
4. t_n = bit time before clocking transition
   t_n+1 = bit time after one clocking transition
   t_n+8 = bit time after eight clocking transitions

Fig. 1

8